Embedding and assembly of ultrathin chips in multilayer flex boards

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Abstract

Purpose – The purpose of this paper is to present results from the EC funded project SHIFT (Smart High Integration Flex Technologies) on the embedding in and the assembly on flex substrates of ultrathin chips.

Design/methodology/approach – Methods to embed chips in flex include flip-chip assembly and subsequent lamination, or the construction of a separate ultra-thin chip package (UTCP) using spin-on polyimides and thin-film metallisation technology. Thinning and separation of the chips is done using a "dicing-by-thinning" method.

Findings – The feasibility of both chip embedding methods has been demonstrated, as well as that of the chip thinning method. Lamination of four layers of flex with ultrathin chips could be achieved without chip breakage. The UTCP technology results in a 60 μm package where also the 20 μm thick chip is bendable.

Research limitations/implications – Further development work includes reliability testing, embedding of the UTCP in conventional flex, and construction of functional demonstrators using the developed technologies.

Originality/value – Thinning down silicon chips to thicknesses of 25 μm and lower is an innovative technology, as well as assembly and embedding of these chips in flexible substrates.

Keywords Assembly, Integrated circuits, Silicon, Laminates

Paper type Research paper

Introduction

In electronic circuit technology there is a clear trend towards mechanically flexible circuits, mainly for portable applications where high compactness and reduced weight are important. Furthermore, chips need to be assembled in bare die format to reduce the size of the resulting circuit. Flip-chip is a quite well known technology in this respect. In order to make use of the 3D, embedding of components, especially chips is the next step. Within the framework of the EC funded project "SHIFT", IMEC and TUB are developing two different approaches to embed ultrathin active components on and in multilayer flex boards (www.shift-project.org).

At TUB an ultra thin flip-chip is embedded into a build-up layer of a flexible printed circuit (FPC).

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Circuit World
34/3 (2008) 3–8
 [ISSN 0305-6120]
[DOI 10.1108/03056120810896209]

The approach of IMEC is to provide an interposer, permitting the testing of the chip before embedding and providing a contact fan out with more relaxed pitches, thus eliminating the need for precise placement and ultra high-density printed circuit boards. Of course, in order to be able to embed chip and interposer in the inner PCB or FPC layers, the unit itself has to be extremely thin, using ultrathin interposer layers and chips.

Fraunhofer-IZM thins dies by a Dicing-by-Thinning (DbyT) process: chips are separated by grooves before thinning. The thickness of the ultra-thin chips is in the range 20-30 μm.

Flip chip in flex (FCF) technology

The flip chip in flex (FCF) technology of TUB aims at very high-integration of electronic systems by:

- reduction of the chip thickness; and
- shortening of the interconnect length between components using a 3D architecture of the wiring.

This work was carried out under the EC IST funded project IP-SHIFT (contract number 507745).

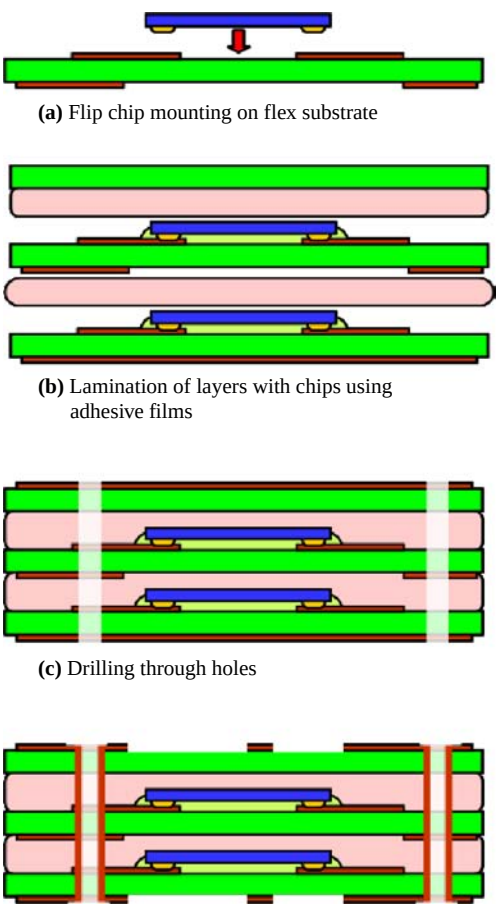
The FPC used are made from commercial materials consisting of 25 μm polyimide and 17 μm copper wiring. Onto the substrates 20 μm thin flip chips are mounted. The electical interconnect is established using an anisotropic conductive adhesive (ACA). Multiple flex boards with assembled chips and adhesive foils can be stacked together and laminated in a conventional stack press. Subsequently, the layers of the board are interconnected by metallized through holes or alternatively by micro vias. The process flow is shown in Figure 1.

Prior to the embedding of thin chips into build-up layers, bond pads on the chip have to be pre-conditioned. In the present case this was acheived by deposition of 3 μm thick electroless Ni/Au bumps. Wafers were subsequently thinned/diced (for process details see below).

The chips are assembled onto the flexible circuit, which was structured by photolithography and etching. The polyimide was 25 μm and the Cu was 17 μm thick. The thermode bonding was performed with commercial flip chip bonder. ACA was used to interconnect the chips electrically to the substrate. A major challenge was the dispensing of a suitable volume of ACA. A too large amount results in an undesired spill-over of material to the side of the chip, see Figure 2.

Although, the electrical and mechanical properties of the build-up are not impacted if ACA is spilled, heavy bond tool

Figure 1 Process flow for FCF technology



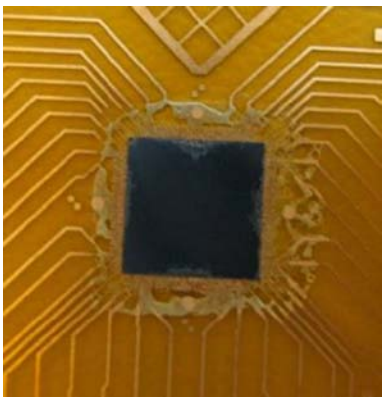
(a) Flip chip mounting on flex substrate

(b) Lamination of layers with chips using adhesive films

(c) Drilling through holes

(d) Metallization of through holes and structuring of outer layers

Figure 2 Thin chip after thermode bonding with ACA spilled around the chip



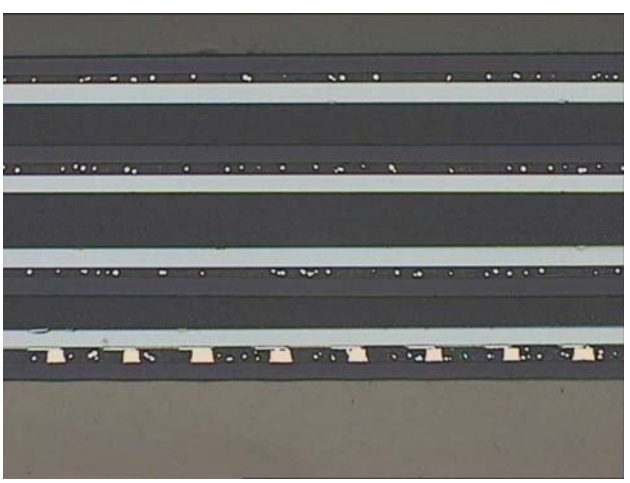
contamination and process disturbance are a consequence. Too small an amount fails to fill the gap between chip and substrate. The latter may result in opens between chip and substrate and therefore has to be avoided. The bonding temperature at its maximum was 230°C and was held for 20 s, followed by cooling at a rate of 10°C/s. An 8.8 kg force during bonding was applied before the maximum temperature was reached and released when the temperature had dropped below 100°C.

Multiple flex sheets, each with assembled thin chips, can then be laminated together using acrylic adhesive laminate. The press parameters were set to the conditions specified by the supplier (~ 190°C and 15 bar for 2 h). The press book was extremely hard to realize a smooth surface on the embedded stack. No chip damage was observed with these conditions, see Figure 3. In order to avoid warpage the depicted stack is laminated so as to realize a symmetric build up. Contacts between layers were established by through holes.

Ultra-Thin chip package (UTCP)

IMEC, together with the University of Ghent, has developed a new concept for packaging ultra-thin chips: the UTCP. The UTCP is based on embedding of ultra-thin chips

Figure 3 Four layers of FPC with ultra thin flip chips symmetrically laminated. White dots are the filler particles of the ACA



(with thickness below 30 μm) in polyimide. An overview of the process flow for the UTCP is shown in Figure 1. The base substrates are a polyimide layer spin coated on a rigid glass carrier. For the fixation and the placement of the chips a benzocyclobutene (BCB) is used as adhesive. The chip is covered with the next polyimide layer. For the contacting to the chip, contact openings to the bumps of the chips are laser drilled and a TiW/Cu layer is sputtered and photolithographically patterned. This metal layer provides a fan out to the contacts of the chips. Finally, the whole package can be released from the rigid carrier.

Typical thicknesses for the different layers are:

- polyimide: 20 μm;
- BCB: < 5 μm;
- chip: 20-30 μm; and
- metallisation: $< = 1$ μm.

This results in a very thin flexible chip package (down to 50-60 μm thickness) (Figure 4).

The base substrate is a 20 μm polyimide layer spincoated on a rigid glass carrier. The polyimide used for this is PI 2611, HD Microsystems.

After processing, the package has to be released from the rigid carrier. An easy release of the package from the rigid substrate is obtained in a special way: before spinning the first polyimide layer, the four edges of the square glass substrate are coated with an adhesion promoter. The consequence of this is that the first layer of polyimide adheres well to the edges of the substrates, and has marginal adhesion strength to the centre of the substrate. However, the adhesion to the edges is sufficient to allow for the whole process cycle 1-6 as shown in Figure 1. After processing the package can be cut out in the area of marginal adhesion and thus peels off easily from the rigid substrate.

An adhesive material is needed for fixation of the ultra-thin chips on the base polyimide layer. The adhesive has to be resistant to the high-curing temperature of the top polyimide, PI 2611 (350°C). Several polymers were already compared for full wafer bonding (Niklaus *et al.*, 2001), in that study BCB bonding offers the highest bond strengths. BCB is used as bonding material.

It is very important to prevent void formation at the bond interface. Voids can be caused by small air bubbles trapped between the adhesive layer and the surface of the chip. These bubbles can be prevented by placing the chips in a vacuum environment during bonding. Another possible solution could be found in dispensing a well-controlled amount of the adhesive. While placing the chip the dispensed adhesive flows from the middle of the surface to the edges of the chip without air at the interface (Figure 5).

Figure 4 Overview UTCP process flow

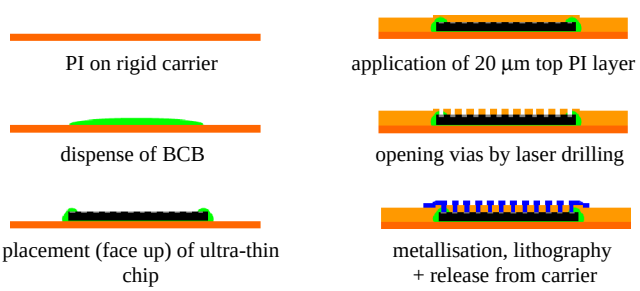
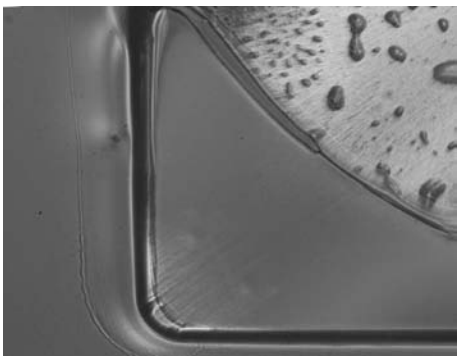


Figure 5 Air bubble under the chip, after cure of BCB



After curing the BCB at 350°C, the chip is fixed on the polyimide layer. Then a covering polyimide (PI 2611) layer is spincoated on this fixed die, with a thickness of 20 μm. In order to obtain a good adhesion between the top polyimide layer and the (cured) base polyimide, this cured polyimide has to be pre-treated. Before spin coating of the top polyimide layer the cured layer is first plasma-treated for 2 min in a CHF_3/O_2 plasma followed by 2 min in an oxygen plasma treatment.

The cross section below was made after the cure of the top polyimide: it is shows the good edge-coverage of the spincoated top polyimide layer (Figure 6).

Contact openings to the bumps of the chips are laser drilled through the top polyimide layer.

The best results are achieved using the tripled YAG-laser with a shaped beam. Beam-shaping optics transform the natural Gaussian irradiance profile to a near-uniform "top hat" profile. This imaged beam removes the polyimide material uniformly across the via, without creating undesirable underlying metal damage at the centre of the imaged spot (which is difficult to control with a Gaussian beam). It is also found that substantially less irradiance dose is required for drilling when using the reshaped beam profile. A lower irradiance dose reduces considerably the thermal load on the material and improves dramatically the overall hole quality (and reduces the debris). Owing to the uniform profile of the beam the tapering can also be better controlled (Karnakis *et al.*, 2001).

Via diameters with a top diameter down to 35 μm can be realized with a shaped beam.

Next, a top metal layer is sputtered, metallizing the contacts to the chip and providing a fan-out (Figures 3 and 7).

Metallisation is realised by sputtering a 1 μm TiW/Cu layer. In order to have optimum adhesion strength of the sputtered

Figure 6 Cross section of embedded chip

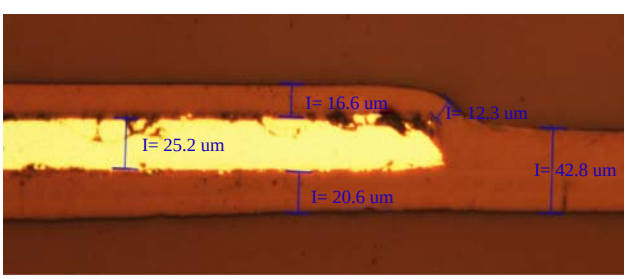
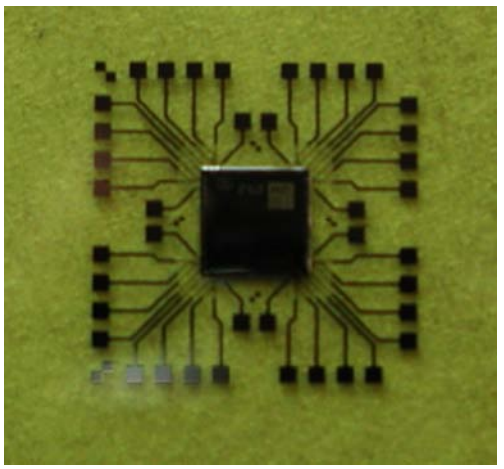


Figure 7 Fan out metallization



TiW/Cu layer on the top polyimide, reactive ion etching was tested on spincoated polyimide layers as pre-metallization surface treatment. We tested three different plasma treatments:

1 CHF_3/O_2 (4/1) gas mixture;
2 O_2 plasma; and
3 CHF_3/O_2 plasma + O_2 plasma.

Polyimide was spincoated on glass-substrates, cured, plasma treated and then metallized with a 1 μm sputtered TiW/Cu layer.

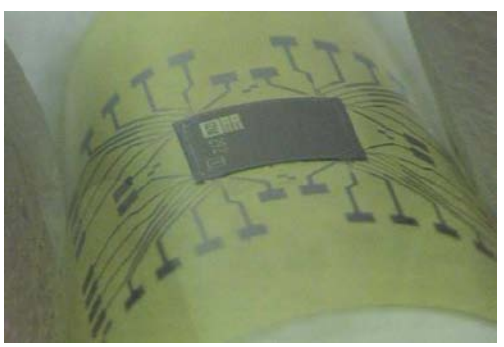
All the samples passed the Scotch-tape test. In order to perform a peel strength test the copper had to be plated up. The sputtered copper was plated to a 25 μm copper thickness and then photolithographically patterned. The measured peel strength on the samples treated with a CHF_3/O_2 plasma and O_2 plasma was higher than 1.6 N/mm and the peel strength of the metallisation on the oxygen treated polyimide was even higher than 2 N/mm.

Finally, the whole package (polyimide layers + embedded chip + fan-out metallization) is released from the rigid substrate. Chip, PI layers and metal are so thin, that the whole package is bendable (Figure 8).

Typical thicknesses for the different layers are:

- polyimide: 20 μm;
- BCB: < 5 μm;
- chip: 20-30 μm; and
- metallisation: $< = 1$ μm.

Figure 8 Bended chip



This results in a very thin flexible chip package (down to 60 μm thickness) (Figure 9).

Wafer thinning and singularization into chips

Wafer thinning has become a key technology for the semiconductor industry during recent years (Savioustok *et al.*, 1998). Most modern packaging technologies require ICs to be thinner than the original wafer thickness. To reach this goal, suitable processes have been developed, and efficient thinning equipment is available. Recently, the chip thickness of semiconductor products like smart cards, contactless labels or power devices is below 150 μm, and will be reduced further.

This section explains the process chain from the wafer output of the semiconductor manufacturer up to the separated chips ready for pick and place. Standard wafer thinning procedures consist of a sequence of grinding, fine grinding and etching, which are well adjusted to each other to deliver the required final thickness, minimum thickness variation and best surface quality. Details of the thinning process are described in Balde (2002). The first step from ultra thin wafers to ultra thin chips is an adequate dicing process. Normal sawing with a diamond blade can be used, but sawing causes damage at the chip edge and seriously reduces fracture resistance of the die, an issue which is rather important for integration in flexible systems. Therefore, a process called "dicing by thinning" is a better approach for thin ICs.

This method starts already before the thinning procedure. In a first step, trenches are sawn or etched in the scribe lines of the wafer with a depth of the final chip thickness. After bonding the device wafer to its handling substrate, thinning is performed until the trenches are opened during the final spin-etching process. If chip separation takes place during backside spin-etching, the grooves are rounded by the etching medium and possible residual micro-cracks are removed. In consequence, such ICs show much higher fracture resistance than chips sawed after thinning (Landesberger *et al.*, 2001). Etching of the scribe lines leads to the best results looking at fracture resistance and additionally offers the freedom of design of chip geometry (Figure 10).

For optimum results and simple processing steps, the scribe lines should be pure silicon and should be free of additional pattern and materials. This is mostly not the case for

Figure 9 Showing bendability of packaged chip

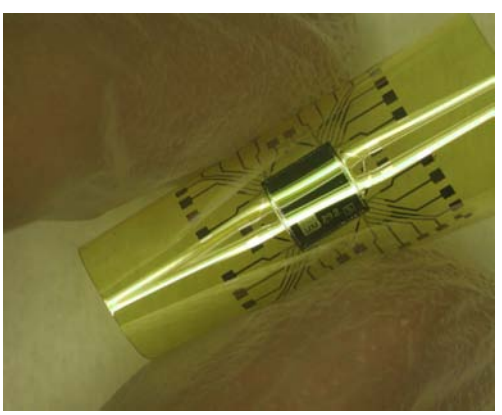
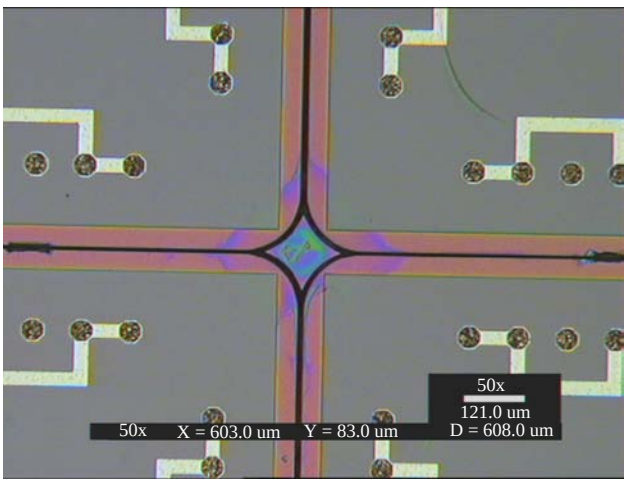


Figure 10 Rounded corners of a 25 μm thin chip; prepared by dry etched grooves at front side of wafer and subsequent backside thinning



commercial available wafers. Therefore, a modified DbyT process was developed where a good edge quality is achieved by a combination of sawing and etch processes (Feil *et al.*, 2004).

After thinning, the wafer is separated into single chips, which have then to be transferred from the handling substrate to a second carrier, e.g. a so-called "blue tape" or other kind of carrier material, from which the pick and place process can start. This process chain, up to pick and place, is schematically shown in Figure 11.

For the purpose of demonstrating the functionality of ultra thin chips, an indicator system on foil was developed by Fraunhofer IZM. A polyimide substrate material with an adhesive-less Cu plating was used. The circuit consists of an electroluminescent indicator, two resistors, a driver IC and a battery as power supply. The indicator is built up by several screen printing steps and the resistors are also screen printed. The driver IC is a charge pump and converts the battery DC voltage of 3.7 V into an AC voltage of about 100 V. The frequency depends on the external resistor value. The second resistor is needed for turning the system on.

The chip size of the driver IC is 2.45 × 1.6 mm. As shown in Figure 12, the contact pads of 100 μm by 100 μm size are in some cases close to one another. The minimum distance is only 60 μm. Since, the IC is flip chip bonded, this value corresponds with a minimum distance on the substrate side of 40 μm for the I/O-pattern.

For the thinning and bonding process the contact pads of a whole wafer get an additional protective metallization layer of electroless Ni/Au. Then the wafer was thinned down to about 25 μm corresponding to the described process. The chips are mounted directly on the substrate by ACA flip chip bonding.

A lighting example is shown in Figure 13.

Conclusion

Two new embedding technologies for thin chips have been developed: the FCF technology from TUB and the UTCP from IMEC. IZM is thinning silicon wafers down to 20-30 μm. Before thinning, trenches are defined: this is the DbyT.

Figure 11 Schematic view of DbyT process and chip transfer to pick and place tape

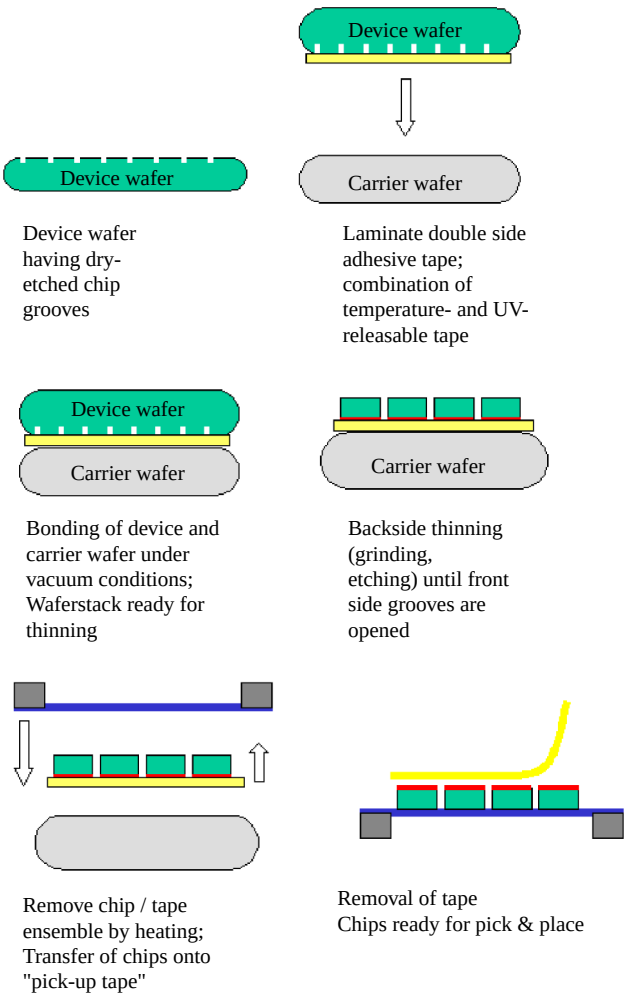
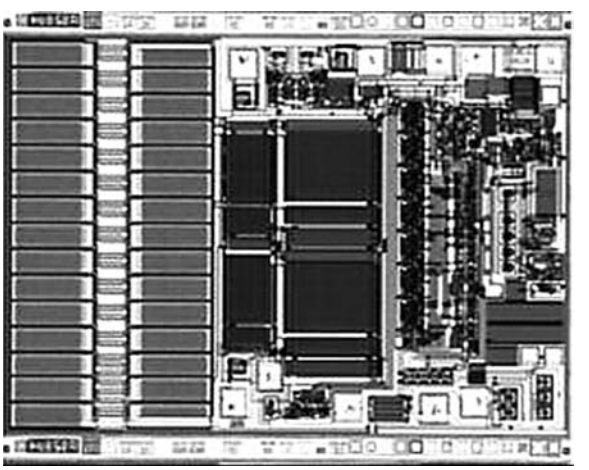
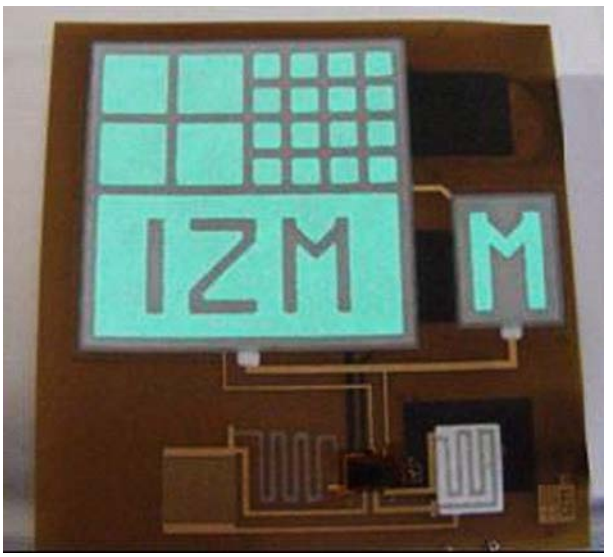


Figure 12 Driver IC



Note: Reproduced from the only available original

Figure 13 Lighting indicator on foil



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T. Loeher studied Physics at University Göttingen and Technical University of Berlin, and gained a Diploma in Surface Physics in 1992. In 1995, he was awarded a PhD from Freie Universität Berlin, in physical chemistry for a work on heterogeneous semiconductor interfaces. From 1996 to 1999 he held a post-doctoral position at the University of Tokyo. He joined TU Berlin Center for electronic packaging and interconnection in 2002. His activities focus around embedding technologies in flexible (EU Project SHIFT), stretchable materials (EU Project STELLA) and ultra thin package stacking (EU Project T I P S).

B. Pahl received the MS Degree in Material Science from the Technical University Berlin (Germany) in 1999. In 2000, she joined the Centre of Microperipheric Technologies and Fraunhofer IZM Berlin. She is working as a Research Scientist within the group of "System Integration on Flex". Her major interest is in fine pitch thermode bonding technologies on flexible substrates focused on process development and metallurgy of ultrathin soldered contacts. She is engaged in chip integration in flexible substrates and responsible for basic research projects in the field of carbon nanotubes and their applications.

M. Feil studied Physics at the Technical University of Munich. After five years with Siemens, he has been with the Fraunhofer Society since 1981. In the past, he was involved in the fields of thick and thin film technology, assembly and packaging techniques for electronics and MEMS. At the moment, he is a Senior Researcher at the Fraunhofer-Institute for Reliability and Microintegration (IZM) Munich Division, Department Polytronic Systems. In 2002, he was starting the reel-to-reel application center for the development of production principles for thin flexible electronic systems. He holds a series of patents in the field of packaging technologies.

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J. Vanfleteren obtained his PhD in Electronic Engineering from the University of Gent (Belgium) in 1987. He is currently a Senior Engineer and Project Manager at IMEC (CMST group) and is involved in the development of novel interconnection, assembly and substrate technologies, especially in the field of flexible and stretchable electronics. In 2004 he was appointed as part time professor at the University of Gent. He is a member of IMAPS and IEEE and (co)-author of over 100 papers in International Journals and Conferences and he holds six tents/patent applications.