Development and study of AlGaN/GaN microwave transistors for high power operation

Vorgelegt von
M.Sc Electronics
Nidhi Chaturvedi
Ferdinand-Braun-Institute für Höchstfrequenztechnik
Berlin, Germany

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Berichter: Prof. Dr. Tränkle
Berichter: Prof. Dr.-Ing. Reichl

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A dissertation submitted By

Nidhi Chaturvedi
M.Sc Electronics
Ferdinand-Braun-Institute-für-Höchstfrequenztechnik
Berlin, Germany

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Faculty of Electrical Engineering
Technical University Berlin, Germany

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Dr. Ing.

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Promotion committee:

Prof. Dr. Tränkle  (Director, FBH, Berlin))
Prof. Dr.-Ing. Reichl (Director, IZM, Berlin)
Prof. Dr.-Ing. Böck  (Prof., TU, Berlin)

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Dedicated to my inspirations

My respected parents
Mrs. Usha Chaturvedi and Mr. N.C Chaturvedi

&

My loving
Nitin, Nikesh and Ajay
Development and study of AlGaN/GaN microwave transistors for high power operation

Executive summary

Power transistors based on (AlGa)N materials are the most emerging and demanding devices of this era for high power, high temperature and high frequency microwave applications. The outstanding properties of AlGaN/GaN heterostructures such as high sheet carrier concentration, high electron mobility, large electron saturation velocity and in particular high breakdown voltage make AlGaN/GaN high electron mobility transistors (HEMTs) promising candidates for these applications. However before tremendous commercialization of AlGaN/GaN HEMTs, more work is needed to improve device technology, epitaxy, design and other performance limiting factors.

This thesis focuses on the development and investigations of AlGaN/GaN high electron mobility transistor for high power operation at 2 GHz.

Technology stabilization process included introduction of nitride passivation layer, ohmic contact and Schottky contact optimizations. A 3-fold increase in output power was achieved using nitride passivation layer. A 2x50 µm device delivered a power density of 5.2 W/mm @ 2 GHz.

Low resistant (0.3 Ω-mm) ohmic contact with good surface morphology and proper line edge definition was achieved, enabling high current, finer gate alignment, low source gate distance, low source resistance and therefore high-speed operation.

Schottky contacts were tested for low leakage, high barrier height, low ideality factor and high temperature stability.

To achieve high power output, epitaxy design was optimized. Increasing Al content of AlGaN layer and introducing AlN interface layer improved device performance.

Despite much progress and improvement in technology and epitaxy designs, current collapse continued to be a big limiting factor that contributed to compromised power performance.

Current slump was studied using pulse current-voltage measurements and its effects on RF properties were examined.

To solve the problem of current collapse, advanced processing issues such as development of embedded gate technology, implementation of field plate structure and optimization of passivation layer are discussed.

In order to increase power level, large periphery devices having different gate widths of 100 µm (2x50 µm), 1 mm (8x125 µm), 2 mm (16x125 µm) and 4 mm (16x250 µm) were designed, fabricated and characterised. A maximum power level of 13.8 W was recorded on a 4 mm wide device.

Design of large periphery devices was modified using a new feed line and feed plate structure to solve the problem of current collapse and design parasitics.

A newly designed (feed plate design) power cell consisting of 8 fingers each having 500 µm gate widths, yielded a saturated output power of 42.3 dBm (17 Watt) at a drain voltage of 30 V. Linear gain of this power device was 21.6 dB and power added efficiency increased up to 46 %.

These power cells were then grouped together to form power bars and were packaged into a commercial CuW-package. A very high power output of 50 dBm (101 W) @ 2 GHz, a PAE of 40 % and a gain of 14 dB was recorded on an 11x8x500 µm packaged power bar. Thermal simulations were performed to study the thermal issues in large periphery devices.
# Development and study of AlGaN/GaN microwave transistors for high power operation

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Chapter 1

Introduction

1.1 Motivation

Over the past years, semiconductor device researchers have proposed many competing devices and technologies in order to satisfy the growing demands for high power, high frequency, high temperature, high linearity and high efficiency communication system in commercial as well as in military applications. Si transistors, GaAs high electron mobility transistors (HEMTs) and heterostructure bipolar transistors (HBTs), SiGe HBTs and SiC metal semiconductor field effect transistors (MESFETs) have established a well-reputed position in these areas.

However, in recent years AlGaN/GaN high electron mobility transistor (HEMT) technology has attracted a lot of interest for these applications. It has emerged as a very promising, long-term contender to other viable technologies for high power solid-state amplifiers. Many active research groups are intensively working and reporting worldwide on AlGaN/GaN high electron mobility transistors [1-9].

The capability of AlGaN/GaN HEMTs to deliver high power, high frequency, high temperature, high linearity and high efficiency performance motivated us to invest years of research on these very demanding devices of this era.

These devices are highly compact due to the possibility of achieving high power levels from small chip area. High frequency and high linearity operations support digital modulation techniques. Operation in rugged environment is favourable due to the stability of these devices at high temperatures. Moreover, high efficiency factor of the devices helps in reducing the complexity of the system and hence the overall cost.

Combining all these remarkable characteristics (sketched in Fig. 1), the AlGaN/GaN HEMT devices have broad application areas covering commercial and military market.

1.1.1 Application and need of power devices

The military employs RF transmitters and receivers for a plethora of applications, which include all-weather radar, surveillance, reconnaissance, electronic attack and communications systems. Strategic military communications systems range from 7 to 44 GHz and beyond. Radar traditionally requires very high pulse powers in the microwave bands from UHF to X-band (8-12 GHz) and beyond. Power amplifiers (PAs) in many systems still use vacuum tubes. However, GaN transistors aimed at uses in future high-performance millimetre-wave (MMW) military communications links and X-band radar have been reported by a number of groups.

The commercial application areas include base stations, satcom and digital radios etc. Satellite-based communications transceivers need efficient, robust and reliable transistors that can act as power amplifiers at MMW frequencies. Rapidly growing market of mobile phones has increased the need to reduce power consumption and space per channel of mobile phone base stations and wireless communication system. GaN based HEMTs are competent to provide precise response to this market demand.
1.1.2 Material properties (GaN)

The band gap energy, breakdown voltage, peak carrier velocity and thermal conductivity are the most important material traits determining the HEMT device characteristics. Large band gap, high breakdown voltage and a high saturation or peak carrier velocity are responsible for high power and high efficiency performance.

High frequency and high temperature operations are mainly a function of high peak carrier velocity, good thermal conductivity and wide band gap respectively (see Fig. 2).
The GaN has attractive material properties such as large band gap (3.4 eV comparing with 1.4 eV of GaAs), high breakdown voltage (3 MV/cm compared to 0.4 MV/cm of GaAs), high peak carrier velocity (3.2 x 10^7 cm/s compared to 2.1 x 10^7 cm/s of GaAs) and good thermal conductivity (1.3 W/cm-k compared to 0.5 W/cm-k of GaAs).

For GaN, the Johnson figure of merit ($\alpha V_{br}^2 x V_{sat}^2$) is 70 times that of GaAs. Therefore, it is definitely a very adequate and outstanding candidate for high performance HEMT.

Table 1 compares the basic material properties of GaN with other well-known semiconductors.
<table>
<thead>
<tr>
<th>Material properties</th>
<th>Si</th>
<th>GaAs</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>AlN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band gap (eV)</td>
<td>1.1</td>
<td>1.4</td>
<td>3.0</td>
<td>3.2</td>
<td>3.4</td>
<td>6.2</td>
</tr>
<tr>
<td></td>
<td>Indirect</td>
<td>Direct</td>
<td>Indirect</td>
<td>Indirect</td>
<td>Direct</td>
<td>Direct</td>
</tr>
<tr>
<td>Electron mobility (cm$^2$/V-s)</td>
<td>1500</td>
<td>8500</td>
<td>250</td>
<td>700</td>
<td>800</td>
<td>300</td>
</tr>
<tr>
<td>Breakdown voltage (MV/cm)</td>
<td>0.3</td>
<td>0.4</td>
<td>2.4</td>
<td>2.0</td>
<td>3.3</td>
<td>11.7</td>
</tr>
<tr>
<td>Saturation velocity (x10$^7$ cm /s)</td>
<td>1.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.7</td>
<td>2.0</td>
</tr>
<tr>
<td>Thermal conductivity (W/cm-K)</td>
<td>1.5</td>
<td>0.5</td>
<td>4.5</td>
<td>4.5</td>
<td>1.3</td>
<td>2.5</td>
</tr>
<tr>
<td>Operating temperature (°C)</td>
<td>300</td>
<td>300</td>
<td>&gt; 500</td>
<td>&gt; 500</td>
<td>750</td>
<td>&gt; 500</td>
</tr>
<tr>
<td>Melting temperature (°K)</td>
<td>1690</td>
<td>1510</td>
<td>&gt; 2100</td>
<td>&gt; 2100</td>
<td>&gt;1700</td>
<td>3000</td>
</tr>
<tr>
<td>Johnson figure of merit</td>
<td>1</td>
<td>11</td>
<td>260</td>
<td>180</td>
<td>760</td>
<td>5100</td>
</tr>
</tbody>
</table>

Table 1. Material properties of GaN and other competitors

### 1.2 Basics of AlGaN/GaN HEMTs

#### 1.2.1 AlGaN/GaN HEMT structure

Different names used interchangeably for HEMT (origin-Fujitsu) devices are ‘MODFET’-modulation doped FET (origin-Cornell, Univ. of Illinois, Rockwell), 'TEGFET'-two dimensional electron gas FET (origin-Thomson CSF), 'SDHT'-selectively doped heterostructure transistor (origin-AT & T bell labs) and 'HFET'-heterojunction FET.

The unique property of the HEMT structure is the possibility of building very high channel charge and high carrier mobility due to the formation of high quality abrupt heterojunctions between semiconductors of different compositions and band gaps, e.g. AlGaN/GaN and AlGaAs/GaAs.

With heterojunction, device designer can vary the band structure (and hence the electric field) as well as the doping level and type in various portion of the device. Significant improvement in the charge transport properties is possible through innovative use of this additional degree of freedom [10-11].

As shown in Fig.3, the AlGaN/GaN HEMT structure is typically composed of

1. Undoped GaN cap
2. AlGaN barrier and supply layer
3. Undoped AlGaN spacer
4. Undoped GaN channel
5. GaN buffer
6. Semi-insulating substrate

<table>
<thead>
<tr>
<th>Layer sequence</th>
<th>Design (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN Cap</td>
<td>2 nm</td>
</tr>
<tr>
<td>AlGaN Barrier</td>
<td>10 nm</td>
</tr>
<tr>
<td>AlGaN Supply</td>
<td>10 nm, _5x10$^{18}$</td>
</tr>
<tr>
<td>AlGaN Spacer</td>
<td>5 nm</td>
</tr>
<tr>
<td>GaN Channel</td>
<td></td>
</tr>
<tr>
<td>GaN Buffer</td>
<td>2700</td>
</tr>
<tr>
<td>Substrate</td>
<td>360000</td>
</tr>
</tbody>
</table>

Fig. 3. AlGaN/GaN HEMT structure
The GaN cap layer protects the AlGaN barrier layer from oxidation. The AlGaN donor/supply layer is typically uniformly doped with Si at a very high doping level of approximately $5 \times 10^{19} - 3 \times 10^{20}$/cm$^3$. This high doping level makes possible a small separation between the gate and the channel in a HEMT. A high doping level in the AlGaN donor layer results high sheet charge density in the channel, providing a high value of $g_m$, $f_T$ and current density.

The AlGaN supply/donor layer should be depleted both from the AlGaN/GaN heterostructure and the Schottky gate to eliminate the parallel conduction of the AlGaN. The AlGaN barrier layer spatially separates the donor layer from Schottky gate metal. Another important parameter in the Al$_x$Ga$_{1-x}$N is the Al mole fraction $x$. The conduction band discontinuity, at the AlGaN/GaN interface is directly related to $x$. A higher Al mole fraction results in an increase in the total carrier sheet charge density. It also reduces the real space transfer of carriers from channel to the AlGaN layer and minimizes the excess modulation of this layer. The high Al mole fraction however leads to the presence of DX centres responsible for the I-V collapse in HEMTs.

In a HEMT, even though the electrons and donors are separated spatially, their close proximity allows an electrostatic interaction called coulomb scattering. By setting the donors away from the interface, coulomb scattering can be reduced. This is done by inserting a thin undoped AlGaN spacer layer between the AlGaN donor layer and the GaN channel to separates the negatively charged 2 deg from the ionized dopant atoms. The reduced scattering helps in increasing the mobility of electrons in 2 deg [12].

High resistivity GaN buffer layers are used to suppress leakage current and thereby providing excellent isolation between devices.

Many of the advantages offered by the HEMT structure are listed in Table 2 below.

<table>
<thead>
<tr>
<th>Advantages of the HEMT structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>High electron mobility</td>
</tr>
<tr>
<td>Small source resistance</td>
</tr>
<tr>
<td>High $f_T$ due to high electron velocity in large electric fields</td>
</tr>
<tr>
<td>High transconductance due to small gate to channel separation</td>
</tr>
<tr>
<td>High output resistance</td>
</tr>
<tr>
<td>Higher schottky barrier height due to deposition of schottky metal on AlGaN</td>
</tr>
</tbody>
</table>

Table 2. Advantages of the HEMT structure

In AlGaN/GaN HEMT structure, the electrons are donated to the crystal by the impurity atoms in AlGaN. These electrons accumulate in the region of lowest potential, just beneath the AlGaN/GaN interface as shown in band diagram of Fig. 4.

Also, due to the lower electron affinity of AlGaN compared to the adjacent GaN region and the offset in the conduction band edges, free electrons diffuse from the AlGaN in to the GaN and form a two dimensional electron gas (2-deg) at the heterointerface.

A potential barrier confines the free electrons in GaN to a very thin sheet. The transport properties of this 2 deg are superior to those of free electrons in conventional MESFET where the channel region must be doped to obtain the charge carriers.
Due to the absence of ionized donors in the channel of a HEMT, electrons forming the 2 deg suffer little coulomb scattering and enjoy high mobility. Having the channel in the form of a 2 deg increases the conductivity by increasing the carrier concentration without suffering the mobility degradation effect. Hence this structure delivers both high sheet carrier densities as well as high electron mobility.

Originally, neither the AlGaN nor the GaN layers were doped. However it was observed that, despite the lack of electrons from intentionally doping, a 2 deg was established at the heterointerface. A sheet charge density of $10^{13}/\text{cm}^2$ was recorded in 2 deg, which is factor of five greater than produced in the AlGaAs/GaAs system.

Since there were no intentionally introduced impurity atoms to supply electrons, the source of electrons forming 2 deg was questionable which is argument as below.
1.2.2 Formation of two dimensional electron gas (2-deg)

Strong spontaneous and piezoelectric polarization effects induce the 2-deg. Spontaneous polarization is polarization on heterointerface at zero strain, which is due to polar AlGaN and GaN layers. Piezoelectric polarization comes from the difference between lattice constants at the heterostructure, thus it increases as the strain at the interface increases.

GaN is a strongly polar material, that is, it possesses a spontaneous polarization that leads to sheet charge accumulation on the end faces of the crystal. These sheet charges are of course, equal in magnitude and opposite in sign to maintain overall charge neutrality. AlGaN also has a spontaneous polarization, similar to GaN but of different magnitude (in fact, a function of the Al content of the ternary). As a result there is a discontinuity of the spontaneous polarization vector at the AlGaN/GaN heterointerface (charge neutrality is not maintained due to different electronegativity of AlGaN, GaN compound).

This discontinuity results in an interface charge proportional to the polarization difference. Furthermore, the strain resulting from growing lattice mismatched AlGaN on GaN induces a piezoelectric charge which supplies additional electrons to the HEMT channel. Conclusively, this total channel charge is the result of total polarization of GaN and AlGaN layer, which is the summation of spontaneous polarization and piezoelectric polarization.

This polarization effect is however quite different due to the different surface termination of the heterostructure. The Ga face and N face surface of GaN are non-equivalent and different chemically and physically. Therefore if due to different face, direction of polarization changes and sometimes in opposite direction, polarization effect can be compensated.

Fig. 5 shows the dependence of polarization direction and charge on the type of crystalline face (either N or Ga face) and strain (either compressive or tensile). It can be seen in case of Ga face, the spontaneous polarization is pointing towards the substrate. Whereas in case of N face, it is pointing in opposite direction (Ambacher et al. [13]). The piezoelectric polarization vector is negative for tensile strained and positive for compressive strained AlGaN layers.

Case 1 is showing the 2 deg formations in Ga face, tensile strained AlGaN over GaN layer. Here both of the piezoelectric and spontaneous polarization vectors are in the same direction. The net positive sheet charge induced at the bottom end face of AlGaN attracts electrons at the interface and results in 2 deg formation.

The N face, compressive strained GaN over AlGaN layer results in positive sheet charge which attracts electrons at the interface and forms 2 deg as depicted in case 2.

Hence, in order to form 2 deg at the interface, the tensile strain is needed to the Ga face (case 1) and compressive strain is required to the N face (case 2). In case 2, due to the opposite polarization directions, the sheet carrier concentrations are as low as \(10^6\) / cm\(^2\) compared to \(10^{13}\) / cm\(^2\) in case 1.

By Si doping AlGaN, a contraction of the wurtzite unit cell can occur leading to strain in doped HEMT. The magnitude of the strain increases as the Si doping concentration increases and the AlN mole fraction in the AlGaN decreases.
In addition to the unique properties of Al(Ga)N material and HEMT structure, adopted strategies and manual efforts improve the overall device behaviour. This research work is exploring the strategies, adopted to boost up the performance of AlGaN/GaN HEMT devices.

**Fig. 5.** Dependence of polarization charge on crystalline faces and strain

$q$: Charge contributed from spontaneous and piezoelectric polarization

$\sigma$: Net induced charge
1.3 Strategies for boosting the AlGaN/GaN HEMTs device performance

The AlGaN/GaN high electron mobility transistors have demonstrated respectable device performance and recently, there has been considerable progress in developing these devices for high temperature/high power microwave applications. In spite of the impressive microwave performance delivered by these devices over the years, there are still many open problems and limiting factors that must be addressed in order to make this technology commercially viable. These fundamental limiting factors are as follows:

- Device technology and epitaxy related issues
- Current collapse problem
- Current collapse suppression methods
- Device layout, packaging and thermal issues

These critical factors and problems put a big question mark on the maturation of AlGaN/GaN HEMT devices. Therefore specific strategies need to be adopted to handle with these problems. We adopted two strategies namely device intern related strategies and device extern related strategies. This research work details the study and implementation of device intern and device extern related strategies to boost up the overall performance of AlGaN/GaN high electron mobility transistor.

1.3.1 Device intern related strategies

Device intern related strategies are technology optimization, epitaxy optimization, current collapse investigations and surface passivation. Main attention in these strategies is given to the internal device structure and related phenomenon shown in Fig. 6. These strategies are explored in two chapters discussed here in brief.

- Optimization of AlGaN/GaN HEMT technology and epitaxy

Device technology optimization and epitaxy design changes are explained in chapter 2. Both of these factors are the basic internal building blocks of AlGaN/GaN HEMT device. The critical layers of AlGaN/GaN HEMT device structure such as ohmic contact metal, Schottky contact metal and mesa isolation geometry are optimized. Measurements results (d.c and r.f) on the wafers processed with standard technology are shown.

A new Embedded gate technology is developed in which the nitride is deposited at an early stage of processing and gates are defined by nitride etching. The embedded gate technology and the standard technology are compared.

Effect of changes in epitaxy design and Al content on the device performance is studied. Impact of introducing AlN interface layer between AlGaN and GaN is sketched.
Main obstacle in the progress of AlGaN/GaN HEMT device performance is the current collapse effect where the measured r.f power density is lower than what is calculated from static I-V characteristics. Study of this effect points towards trap related phenomenon associated with deep centres in AlGaN barrier, surface or in GaN buffer. Important aspects of the current collapse such as gate lag, drain lag, role in power reduction, effect of different bias points, gate widths, pulse duration and pulse separation etc. are elaborated in chapter 3. The methods tested to solve this problem are also listed.

**Current collapse suppression methods**

Direct exposure of device surface to environment gives rise to many problems such as surface damage, inhomogenity, current collapse, leakage current etc. Passivating the device surface solved these problems. Significant improvement in the device performance using SiNx and SiO2 surface passivation films, comparison of nitride deposition methods, optimization of pcvd SiNx deposition process, embedded gate technology and field plate structures are covered in chapter 4.
1.3.2 Device extern related strategies

Device extern related strategies deal with device design changes, thermal problems and packaging that are more sensitive to the device outer surroundings as shown in Fig. 7.

These schemes are compactly discussed in chapter 5 titled as below:

- **Layout optimization, packaging and thermal simulation**

  Device external aspects such as its dimension, connection to outer world through packaging and type of heat sinking could severely degrade or enhance the device performance. Device packaging and variation in the device design to achieve high power levels and high breakdown voltages are stated in this part of research.

  Non-linear scaling of device gate width with device performance is analyzed. Finally, the thermal problems due to type of heat sink are studied.

![Device extern related strategies](image)

<table>
<thead>
<tr>
<th>Device extern strategies</th>
<th>Related strategies</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device geometry/Size</td>
<td>Layout optimisation &amp; packaging</td>
</tr>
<tr>
<td>Heat sink Sapphirel/SIC/Packag</td>
<td>Study of thermal aspects</td>
</tr>
</tbody>
</table>

**Fig. 7.** The AlGaN/GaN HEMT device extern related strategies
Chapter 2

Optimization of AlGaN/GaN HEMT technology and epitaxy

2.1 AlGaN/GaN HEMT standard process technology

The Al$_{0.25}$Ga$_{0.75}$N/GaN HFET structures used in the processing were grown by MOCVD on 2” SiC and sapphire wafers. The epitaxy growth sequence started with the deposition of a 500 nm thick AlGaN layer followed by a 2.7 µm thick highly insulating GaN buffer layer, 3 nm Al$_{0.25}$Ga$_{0.75}$N spacer, 12 nm Si-doped Al$_{0.25}$Ga$_{0.75}$N supply layer, 10 nm Al$_{0.25}$Ga$_{0.75}$N barrier layer and a 5 nm thick GaN cap layer.

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Reflector deposition_Alignement marks</td>
</tr>
<tr>
<td>2</td>
<td>Ohmic contacts_Ti/Al/Ti/Au/WSiNx</td>
</tr>
<tr>
<td>3</td>
<td>Reflector etching and RTP</td>
</tr>
<tr>
<td>4</td>
<td>Schottky contacts_Pt/Ti/Au</td>
</tr>
<tr>
<td>5</td>
<td>Mesa isolation</td>
</tr>
<tr>
<td>6</td>
<td>Interconnect metal_Ti/Au</td>
</tr>
<tr>
<td>7</td>
<td>Air bridge formation Plating base and plating process</td>
</tr>
<tr>
<td>8</td>
<td>Air bridge formation Plating process</td>
</tr>
<tr>
<td>9</td>
<td>Characterization</td>
</tr>
</tbody>
</table>

Fig. 8. The AlGaN/GaN HEMT device fabrication steps
A 25 nm thick AlGaN layer on the top of GaN buffer formed a two-dimensional electron gas (2 deg) at the AlGaN/GaN interface. A very similar design was adopted for Sapphire where the epitaxy structure started with a 25 nm thick low temperature GaN nucleation layer to reduce the misfit between Sapphire and GaN.

The Al$_{0.25}$Ga$_{0.75}$N/GaN HEMT device fabrication was accomplished in eight lithography steps shown in Fig. 8. It started with the deposition of backside and front side Ti reflector layers (Z-layer) on transparent wafers for ease of handling, recognition and exposure using wafer stepper.

The front side Ti layer was structured and alignment marks were defined by stepper lithography. A sophisticated Ti/Al/Ti/Au/WsiN$_x$ metallization scheme was employed for the fabrication of ohmic contacts (B-layer). The reflector was then removed (Y-layer) and wafers were annealed in N$_2$ ambient to achieve low contact resistance.

Gate contacts (C-layer) were made in next step using Pt/Ti/Au metallization. A gate length of 0.5 µm was defined with stepper lithography. The mesa isolation was done (A-layer) by reactive ion etching RIE (BCl$_3$/Cl$_2$/Ar). Gate fingers and drain fingers were interconnected (D-layer) using Ti/Au.

Source pads were connected using Au air bridges in two steps. First the plating base (F1-layer) was defined using Ti/Au/Ti metal and then the air bridges were made using Au Galvanic method (F2-layer).

All these layers were aligned using i-line wafer stepper. A fully processed 2" wafer and a 12-finger AlGaN/GaN HEMT device (an example) are shown in Fig. 9.

![Wafer and Device](image)

**Fig. 9.** A fully processed 2" wafer and an AlGaN/GaN HEMT device

Wafers were characterized after successful fabrication of AlGaN/GaN HEMT devices. Both d.c and r.f characterizations were performed to check the over all device performance.

### 2.1.1 Device characterization and results

Typical d.c measurements on 2x40 µm devices (2 gate fingers and 80 µm unit gate width) revealed a saturated drain current of $I_{DSS} = 0.7$ A/mm ($V_G = +1$ V). The contact resistance
(R_c) was 0.4-0.6 Ωmm and the normalized source-gate resistance (R_{source}) was generally 0.85-0.9 Ωmm. From this the intrinsic g_{m,max} was calculated to be 340 mS/mm (extrinsic g_{m,max} 260 mS/mm) using the formula g_{m,int} = g_{m,ext} / (1 - R_s g_{m,ext}).

A Schottky barrier height (\Phi_b) of 0.5 eV was measured along with an ideality factor (n) of 3. A typical d.c-IV output and transfer characteristics are shown in Fig. 10.

\[
g_m = 260 \text{ mS/mm} \\
V_p = -2.5 \text{ V} \\
2x40_0.5 \text{ µm}
\]

Transconductance

\[I_{ds} = 0.7 \text{ A/mm} \\
\text{At } V_{gs} = +1.0 \text{ V} \\
2x40_0.5 \text{ µm}
\]

Output characteristics

**Fig. 10.** D.C characteristics of AlGaN/GaN HEMT device

Summary of overall device performance is given in Table 3. Fig. 11 indicates important points (points to ponder) of standard technology, which needed modification and optimization to achieve betterment in device performance.

<table>
<thead>
<tr>
<th>Performance parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{ds,max} (A/mm)</td>
<td>0.7</td>
</tr>
<tr>
<td>R_c (Ω-mm)</td>
<td>0.4-0.6</td>
</tr>
<tr>
<td>R_{source} (Ω-mm)</td>
<td>0.85-0.9</td>
</tr>
<tr>
<td>g_m extrinsic (mS/mm)</td>
<td>260</td>
</tr>
<tr>
<td>g_m intrinsic (mS/mm)</td>
<td>340</td>
</tr>
<tr>
<td>Barrier height (\Phi_b) (eV)</td>
<td>0.5</td>
</tr>
<tr>
<td>Ideality factor (n)</td>
<td>3</td>
</tr>
<tr>
<td>Maximum power density (W/mm) @ 2 GHz</td>
<td>0.625</td>
</tr>
<tr>
<td>PAE (%)</td>
<td>14</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>18</td>
</tr>
</tbody>
</table>

**Table 3.** Summary of device performance_2x40 µm device
2.2 AlGaN/GaN HEMT technology modifications and results

2.2.1 Introducing SiN\textsubscript{x} passivation layer

As a first step in technology modification, we introduced SiN\textsubscript{x} passivation layer [50-54] (see Fig. 12) to protect the device surface from surface contamination and possible damage during device processing. We believed to achieve betterment in the device performance through surface passivation. Deposition conditions of PECVD SiN\textsubscript{x} are given in Table 4.

<table>
<thead>
<tr>
<th>Thickness (nm)</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power (W)</td>
<td>100</td>
</tr>
<tr>
<td>Pressure (Pa)</td>
<td>80</td>
</tr>
<tr>
<td>Refractive Index</td>
<td>1.9</td>
</tr>
<tr>
<td>Temperature (°K)</td>
<td>345</td>
</tr>
<tr>
<td>SiH\textsubscript{4} (sccm)</td>
<td>100</td>
</tr>
<tr>
<td>NH\textsubscript{3} (sccm)</td>
<td>12</td>
</tr>
<tr>
<td>Ar (sccm)</td>
<td>140</td>
</tr>
<tr>
<td>Deposition time (s)</td>
<td>300</td>
</tr>
</tbody>
</table>

Table 4. Deposition conditions of PECVD SiN\textsubscript{x}
Also we interchanged the order of mesa isolation and gate deposition layers in lithography to avoid the possibility of gate leakage current flowing due to etched mesa after gate deposition.

Fig. 12. The AlGaN/GaN HEMT modified device fabrication steps

2.2.1.1 Characterization of SiNx passivated HEMTs

- D.C-Characteristics

D.C measurements on SiNx passivated 2x50 μm devices (2 gate fingers and 100 μm unit gate width) revealed a saturated drain current of $I_{DSS} = 1.2 \text{ A/mm}$ ($V_G = +2 \text{ V}$). Due to the excellent contact resistance (0.3-0.6 Ωmm), the normalized source-gate resistance was generally 0.85-0.9 Ωmm. From this the intrinsic $g_{m,\text{max}}$ was calculated to be 360 mS/mm
(extrinsic 275 mS/mm) and the minimum on-resistance was $R_{on} = 2 \, \Omega \text{mm}$. A typical d.c.-I-V output and transfer characteristics are shown in Fig. 13.

![D.C characteristics of SiN$_x$ passivated AlGaN/GaN HEMT device](image)

**Fig. 13.** D.C characteristics of SiN$_x$ passivated AlGaN/GaN HEMT device

- Small signal parameters

S-parameters of the microwave power transistors were measured up to 50 GHz. The gain vs. frequency curve (see Fig. 14) followed the 20-dB/decade roll off indicating a good agreement with common device understanding.

For the $L_G = 0.5 \, \mu \text{m}$ gates a typical current gain cut-off frequency $f_t$ of 21 GHz was obtained. Therefore, the $L_G \times f_t$ product was around 10 GHz$\times\mu \text{m}$.

Devices having 0.5 $\mu \text{m}$ gate length and 100 $\mu \text{m}$ gate width revealed a maximum frequency of oscillation $f_{\text{max}} = 79 \, \text{GHz}$. 

20
Fig. 14. The gain vs. frequency curve of a SiN$_x$ passivated 2x50 µm device
($V_{gs} = -3$ V, $V_{ds} = 20$ V)

- Load pull

Large signal microwave measurements were made at 2 GHz using passive load pull system. The highest power density measured on a SiN$_x$ passivated AlGaN/GaN HEMT device having unit gate width of 100 µm (2x50 µm) was 5.3 W/mm. The power added efficiency was 45 %. The linear gain was 25 dB, which decreased to 21 dB in saturation. Load pull measurement of 2x50 µm device is shown in Fig. 15.

Fig. 15. Load pull measurement at 2 GHz
Summary of d.c and r.f results are given in Table 5. A direct comparison of non-passivated devices with passivated devices is discussed in chapter 4.

After achieving high power and high current levels by introducing SiNₓ passivation layer and thereby modifying standard technology, we moved forward in the direction of optimizing ohmic and Schottky contacts.

<table>
<thead>
<tr>
<th>Performance parameters</th>
<th>Values</th>
<th>Points to ponder</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_dsmax (A/mm)</td>
<td>1.2</td>
<td>Increase in current levels</td>
</tr>
<tr>
<td>R_c (Ω-mm)</td>
<td>0.4-0.6</td>
<td>Trouble in achieving defined source gate distance and recognition of alignment marks due to poor line edge definitions</td>
</tr>
<tr>
<td>R_source (Ω-mm)</td>
<td>0.85-0.9</td>
<td></td>
</tr>
<tr>
<td>g_m extrinsic (mS/mm)</td>
<td>275</td>
<td>Increase in g_m</td>
</tr>
<tr>
<td>g_m intrinsic (mS/mm)</td>
<td>360</td>
<td></td>
</tr>
<tr>
<td>Barrier height Φ_b (eV)</td>
<td>0.5</td>
<td>High leakage and low breakdown due to low barrier, need to check different Schottky metals</td>
</tr>
<tr>
<td>Ideality factor (n)</td>
<td>3</td>
<td>High ideality factor indicates the need to improve surface conditions</td>
</tr>
<tr>
<td>P_out (W/mm) @ 2 GHz</td>
<td>5.2</td>
<td>Increase in P_out</td>
</tr>
<tr>
<td>PAE (%)</td>
<td>45</td>
<td>Increase in PAE</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>21</td>
<td>Increase in gain</td>
</tr>
<tr>
<td>F_max (GHz)</td>
<td>79</td>
<td></td>
</tr>
<tr>
<td>F_t (GHz)</td>
<td>22</td>
<td></td>
</tr>
</tbody>
</table>

Table 5. Summary of d.c and r.f results
Parameters mainly influenced by SiNₓ passivation are indicated in bold

2.2.2 Optimization of ohmic contacts

Low resistance ohmic contacts are essential for the efficient operation of high power electronic devices, in particular to achieve high current densities, higher extrinsic gain and low Joule heating loss to allow high temperature operation. Due to the wide band gap of the AlGaN-GaN system, it is difficult to realise ohmic contacts with low specific contact resistance. Additionally the diffusion of metals and out flowing of their liquid phases because of thermal annealing makes it difficult to achieve good surface morphology and good line edge definition. Therefore optimization of the ohmic contacts for low contact resistance, good surface morphology and good line edge definition is an important issue.

Many metallization schemes have been proposed worldwide. Motayed et al. [14] used traditional Ti/Al/Ti/Au contact, which delivered specific contact resistance of 3x10⁻⁶ Ω.cm². A value of 7x10⁻⁷ Ω.cm² was obtained on n-GaN by Bright et al. [15]. Boudart et al. [16] recorded a specific contact resistance value of 8x10⁻⁶ Ω.cm².

In order to prevent the reaction between Al and Au, metals having comparatively high melting points (Mo, Pt and Ni) were interposed in between. A specific contact resistance of 7.3 x 10⁻⁷ Ω.cm² was measured on Ti/Al/Ni/Au contact, proposed by Jacob et al. [17]. Ti/Al/Pt/Au contacts were realised by Lou et al., on which they measured specific contact resistance of 8.89 x 10⁻⁶ Ω.cm².
Low contact resistance of 0.38 Ω-mm was measured by Selvanathan et al. [18] on Ti/Al/Mo/Au based contact. Nebauer et al. [19] developed Ti/Al/Ti/Au/WSiNx scheme delivering low contact resistance of 0.5 Ω-mm. Although many groups recorded very low contact resistances, thickness of the metallization stack was found to be a very critical parameter to obtain good surface morphology together with good line edge definition.

We realised the scheme proposed by Nebauer et al. [19] as shown in Fig. 16 using metallization thickness of 10/50/20/30/140 nm.

![Fig. 16. SEM picture of Ti/Al/Ti/Au/WSiNx contact](image)

This metallization system however suffered from the edge delineation problem (see arrow). The overlap length of WSiNx was 0.5 µm. This led to difficulties in achieving a defined source-gate distance and finer gate alignment, thereby deteriorating the performance of high speed HEMT.

In order to develop ohmic contacts with good edge definition and good electrical properties, we tested different metallization stacks including Ni, Pt and Mo as intermediate layers in between Al and Au.

### 2.2.2.1 Experiments, electrical and morphological results

Ti, Al, Au, Ni, Mo and Pt contact metals were deposited by electron beam evaporation and WSiNx was deposited by sputtering. Contact systems were annealed at 830° for 15 s. The electrical characterization was performed using transmission line method (TLM) on 150 x 100 µm pads with the spacing of 2, 4, 8 and 16 µm. These contacts were tested on samples having AlGaN supply layer doping = 3 x 10\(^{19}\) /cm\(^3\). Fig. 17 shows the contact properties (quantitative and qualitative) of tested metallization systems.

Table 6 is listing the tested contact metal stacks and their corresponding contact properties. Straight line fitted to measured data in resistance-length curve showed good measurement quality. Based on these contact properties in table, the results can be summarized as follows:

- We obtain almost similar values of contact resistance ranging from 0.3-0.5 Ω-mm from various metallization schemes. Hence any combination out of them can be used if the low \(R_c\) is the only demanding factor.
• A significant difference is observed in morphology and line edge definition of the used ohmic metal contacts, although the internal Ti/Al layers in intimate contact with the semiconductor are the same.

• Molybdenum based contacts are the preferable choice in terms of low contact resistance as well as good morphology and line edge definition.

• This implies that the intermediate metal in between Au and Ti/Al plays an important role in determining the contact behaviour. Therefore, we focus our attention on understanding the role of this intermediate layer influencing the mechanism of contact formation.

<table>
<thead>
<tr>
<th>Metal stacks</th>
<th>$R_c$ (Ω-mm)</th>
<th>Line/Edge definition</th>
<th>Morphology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti/Al/Ti/Au/WSiNx 10/50/20/30/140</td>
<td>0.510 ± 0.021</td>
<td>--</td>
<td>++</td>
</tr>
<tr>
<td>Ti/Al/Mo/Au 10/50/20/30</td>
<td>0.429 ± 0.04</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Ti/Al/Ti/Au/Mo 10/50/20/30/140</td>
<td>0.416 ± 0.11</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Ti/Al/Mo/Au 10/50/40/30</td>
<td>0.420 ± 0.01</td>
<td>+</td>
<td>++ bad adhesion</td>
</tr>
<tr>
<td>Ti/Al/Ti/Au 10/50/20/30</td>
<td>0.502 ± 0.11</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Ti/Al/Ni/Au 10/50/20/30</td>
<td>0.371 ± 0.03</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Ti/Al/Pt/Au 10/50/20/30</td>
<td>0.410 ± 0.03</td>
<td>+</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 6. Quantitative

| Qualitative |

Morphology and line edge definition are indicated by signs ++, --, + and – for best, worst, good and bad respectively

(*) Indicates the thicker metal

Fig. 17. Contact properties of tested metallization systems

2.2.2.2 Contact formation and surface morphology

During contact annealing, metals react with each other and with the semiconductor to form several intermediate phases. We adopted models for each metallization system, which were based on the literature available [14 to 19] on these reactions. These models were then verified and supported by the X-ray microanalysis (EDS) and X-ray diffraction analysis (XRD) as explained below:

• Ti/Al/Ti/Au

The model adopted for this metallization system is shown in Fig. 18. Literature survey showed that the formation of TiN, TiAl, AlN and Al$_2$Au phases due to both in and out diffusion of Ti and Al are responsible for the contact properties. Formation of these phases generates N vacancies that are known to act as n-type dopant atoms [20]. The interfacial region (between metal and semiconductor) thus becomes heavily doped, providing the configuration needed for tunnelling contacts.
Luther et al. [21] proposed that the process of AlN formation results in N vacancies, which yields a heavily doped interface, resulting in a tunnelling current responsible for the ohmic contact formation.

TiN exhibits metallic conductivity and has a work function < 4 eV, which supports easy tunnelling due to lowering of the barrier. The Al diffusion in Ti gave rise to Ti-Al phase, which has resistivity lower than that of Ti. Because of all these mentioned points, low value of the contact resistance was recorded from this contact.

![Fig. 18. Reactions among different metals and semiconductor](image)

We performed energy dispersive X-ray microanalysis (EDS) on Ti/Al/Ti/Au deposited wafer, for element localization. It detected the Ti, Al and N on the same location shown by fitted window in Fig. 19.

![Fig. 19. EDS detection of Ti, Al and N location](image)

This confirmed the formation of TiAl, AlN and TiN phases. We detected the formation of Al$_2$Au phase (purple plague) using X-ray diffraction (XRD) structural analysis. This phase was responsible for the type of rough surface morphology shown in Fig. 20. That confirms Ti as a bad diffusion barrier for Al and hence Al flow (due to its very low melting point of 660° C) in both directions and react with Ti and Au, which are having melting points of around 1600° and 1060° respectively.
Fig. 20. SEM picture of Ti/Al/Ti/Au contact

- **Ti/Al/Mo/Au**

  X-ray microanalysis (EDS) was performed on Ti/Al/Mo/Au deposited wafer, to detect the location of elements present in this metallization stack after annealing. Fig. 21a, b, c and d are showing the EDS detected positions of Ti, N, Al, Ga, Mo and Au.

  The availability of Ti, N and Al on the same positions indicated the formation of Ti-N, Al-N and Ti-Al phases. Additionally the strong overlapping areas of Mo and Al showed the formation of Al-Mo phase.

Fig. 21. EDS detection of Al-Mo, Ti-N, Ti-Al and Al-Au phases
The formation of Al-Mo phase in addition to TiN, AlN and TiAl phases seemed to be responsible for typical behaviour of this contact. Furthermore, X-ray diffractograms \(I(2\theta)\) (\(I\) x-ray intensity, \(2\theta\) scanning angle) were measured with a Philips thin film diffractometer (Cu K\(\alpha\), incidence angle \(\theta_i = 3^\circ\) (for comparison \(8^\circ\)), \(2\theta\) scan in the range 20 to 100° or 120°) using nearly the full area of the sample. The diffractogram recorded the peaks of GaMo\(_3\) and Al\(_2\)Au as shown in Fig. 22. The first row of diffractogram is showing the experimental peaks. Second and third rows are showing the fitted peaks of GaMo\(_3\) and Al\(_2\)Au respectively.

**Fig. 22. XRD analysis of Ti/Al/Mo/Au contacts**

Detection of the Al\(_2\)Au phase should theoretically result in rough surface morphology as was seen for the Ti/Al/Ti/Au based contacts. However, amazingly, a very good surface morphology with proper line edge definition was obtained shown in Fig. 23. The reason behind was the formation/co-existence of GaMo\(_3\) phase along with the Al\(_2\)Au phase. A very high melting point of GaMo\(_3\) phase (\(\approx 3000\) °K) helped in compensating the adverse effect of Al\(_2\)Au on surface morphology.

**Fig. 23. SEM picture of Ti/Al/Mo/Au contacts**

Based on the results obtained from X-ray diffraction and microanalysis, we developed a modified model for this particular metallization system shown in Fig. 24. The model indicated the reaction between Al and Mo, which resulted in Al-Mo phase formation.

The Al metal of the Mo-Al phase exchanged with Ga of the AlGaN, during an exchange reaction (Swenson et al [22]). The Ga diffused throughout the metal films.
leaving behind an Al rich AlGaN interface and reacted with Mo (due to its high reactivity with Mo) forming Ga-Mo$_3$ phase.

![Exchange reaction diagram](image)

**Fig. 24.** The model of Ti/Al/Mo/Au contact

As a result of Ga out diffusion, Ga vacancies ($V_{Ga}$) were supposed to be created in the material causing a charge imbalance in the lattice. To relax this imbalance, the nearby N atoms moved to the vacant Ga sites creating N vacancies ($V_{N}$) as explained by Mohammad et al. This high concentration of N vacancies led to heavy doping and hence reduction in contact resistance.

- **Ti/Al/Ti/Au/Mo**

The contact properties of this particular metal stack were found to be very similar to the Ti/Al/Mo/Au.

X-ray diffraction confirmed the presence of GaMo$_3$, Al$_{3-x}$Mo$_{1+y}$ and Mo due to in and out diffusion of Mo, shown in Fig. 25.

![X-ray diffraction peaks](image)

**Fig. 25.** X-ray diffraction peaks of Ti/Al/Ti/Au/Mo
Effect of GaMo$_3$, Al$_{3-x}$Mo$_{1-x}$ and Mo on the surface morphology and the contact resistance has already been discussed. Due to high melting point and robustness of the Mo and its compounds, good surface morphology shown in Fig. 26 was observed.

![Fig. 26. Surface morphology of Ti/Al/Ti/Au/Mo](image)

- **Ti/Al/Ni/Au**

Formation of NiAl phase in addition to the TiN, TiAl and AlN was believed to be responsible for the different nature of this contact than others. X-ray diffraction confirmed the formation of NiAl and Al rich phases shown in Fig. 27. Being highly oxidation resistant, the NiAl phase protected the contact from degradation [23].

![Fig. 27. X-ray diffraction peaks of Ti/Al/Ni/Au](image)

X-ray microanalysis (EDS) was performed to detect the element locations, which confirmed the formation of TiN and TiAl phases. Absence of Au on Al rich positions (see Fig. 28) showed that they did not react with each other. Hence, Ni proved as a good barrier between Al and Au, which restricted the formation of highly resistive purple plague. Detection of Ga on the surface confirmed its out diffusion.
Random distribution of different elements such as Ti, Ni, Ga and Al in different locations was responsible for the type of semiconductor surface morphology shown in Fig. 28.

| Semiconductor | Ga | Al | Au |

Fig. 28. EDS detection of Ga, Al and Au

- **Ti/Al/Pt/Au & Ti/Al*/Pt/Au**

Due to non-availability of Pt element in the software, the Pt and related compounds were not detected. Therefore X-ray microanalysis (EDS) was performed which indicated the presence of Pt and Ga on the surface shown in Fig. 29. Patched surface morphology was the result of different positions of Ga and Pt on the surface. Pt-Au formed a robust compound that protected the Ti/Al from oxide degradation. In this way, it helped in improving the contact resistance.

- **Ti/Al/Ti/Au/WSiNₓ**

This contact behaves very similarly to the Ti/Al/Ti/Au contact, in terms of contact resistance. The formation of extra W-N phase observed by Nebauer et al. resulted in further lowering of contact resistance. Moreover sputtered layer of WSiNₓ restricted the outflowing of internal metal layers, especially Al-Au phase. Hence very smooth surface morphology was obtained.

Fig. 29. Surface morphology of Ti/Al/Pt/Au

In summary, the formation of GaMo₃ compound and Al-Mo phase were responsible not only for low contact resistance and sharp line/edge definition but also for the good surface morphology of Ti/Al/Mo/Au contacts. Types of intermetallic layers in between
Ti/Al and Au mainly determined the contact properties of particular metallization system.

A long series of experiments confirmed the optimized ohmic metallization scheme to be taken in to modified technology. However, the low barrier height and high leakage current remained an important question of concern. Therefore we worked towards the optimization of Schottky contacts.

### 2.2.3 Optimization of Schottky contacts

It is a crucial step in the HEMT device technology to develop stable, reliable and high performance Schottky contacts. Moreover, a full understanding of thermal behaviour of these contacts is required for high temperature applications. The Schottky barrier height is one of the most important parameter of Schottky contacts. A large barrier height improves transconductance, maximum drain current and breakdown voltage of device, corresponding to the increase in power and high voltage performance. It also results in small leakage current, thus reducing the noise level.

Since the Schottky barrier height is defined by the work function of metals and the electron affinity of semiconductor, multilayer contacts having high work function metals (Pt, Ni, Ir, Pd, Au etc.) covered by a high conductive top metallization (usually gold) have been reported by many groups.

Monroy et al. [24] obtained a barrier height of 1.18 eV and 1.05 eV using Pt/Ti/Au and Pt/Au contacts respectively on GaN. Ni/Ti/Au and Ni/Au Schottky contacts delivered a barrier height of 1.02 eV and 1.04 eV respectively. Würfl et al. [25] checked the thermal stability of Pt contacts on AlGaN/GaN, which were found to start degrading even before 400°C. Ni based contact were found to be thermally stable up to 450 and 500°C reported by Arulkumaran [26] and Liu [27]. Pt-Si contacts delivered a barrier height of 0.85 eV and started degrading at 600°C reported by Liu.

Venugopalan et al. [28] showed that the Ni/Ga/Ni contacts delivered a barrier height of 0.75 eV and were thermally stable upto 700°C. A barrier height of 0.82 eV was recorded on Re contacts, which were thermally stable up to 600°C.

Khan et al. [29] achieved a barrier height of 0.91 eV using Au Schottky contact on GaN. Binari et al. [30] obtained a barrier height of 0.59 eV and 1.19 eV using Ti and Au Schottky contacts on GaN respectively.

Wu et al. [31] mentioned Au, Al and Mg contacts on GaN possessing a barrier height of 0.89 eV, 0.60 eV and 0.62 eV respectively. Kuznetzova et al. [32] used Ni and Mo contacts on AlGaN where they recorded 1.1 eV and 1.4 eV respectively with ideality factor of 1.1. Polyakov et al. [33] obtained a barrier height of 1.1 eV using Au on AlGaN. As deposited Ir contacts on AlGaN/GaN showed a barrier height of 0.68 eV (Lee et al. [34]). This increased to 1.07 eV after 24 hrs annealing at 500°C.

Lee et al. obtained a barrier height of 0.59 eV using Pt based contacts on AlGaN/GaN. This increased to 0.78 eV and 0.84 eV as a result of premetallization O₂ annealing and aqua regia treatment.

In order to optimize Schottky contacts in our technology, we compared the performance of Pt, Ir and Ni based Schottky contacts covered with highly conductive layer of Au. Ti was used as an intermediate metal to avoid reaction between Au and other contact metals. The properties of these metals are given in Table 7.
<table>
<thead>
<tr>
<th>Metal properties</th>
<th>Pt</th>
<th>Ni</th>
<th>Ir</th>
<th>Ti</th>
<th>Au</th>
</tr>
</thead>
<tbody>
<tr>
<td>Work function (eV)</td>
<td>5.6</td>
<td>5.15</td>
<td>5.27</td>
<td>4.33</td>
<td>5.1</td>
</tr>
<tr>
<td>Melting point (T°C)</td>
<td>1772</td>
<td>1453</td>
<td>2443</td>
<td>1660</td>
<td>1064</td>
</tr>
<tr>
<td>Thermal conductivity (W/cm-K)</td>
<td>0.72</td>
<td>0.90</td>
<td>1.47</td>
<td>0.22</td>
<td>3.17</td>
</tr>
</tbody>
</table>

Table 7. Properties of Schottky contact metals

2.2.3.1 Comparison of Pt, Ni and Ir Schottky contacts

The Schottky metallization schemes used for comparison are shown in Table 8.

<table>
<thead>
<tr>
<th>Schottky metallizations</th>
<th>Pt/Ti/Au</th>
<th>Ni/Ti/Au</th>
<th>Ir/Ti/Au</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness (nm)</td>
<td>30/20/400</td>
<td>30/20/400</td>
<td>30/20/400</td>
</tr>
</tbody>
</table>

Table 8. Schottky metallization schemes

Schottky parameters such as barrier height and ideality factors were extracted from I-V characteristics of diode on a log\(_{10}\) scale as shown in Fig. 30. The characteristic of Pt based contact showed high leakage current compared to Ni and Ir where almost no leakage was seen. Therefore, a barrier height of 0.9 eV and 0.8 eV along with an ideality factor of 1.4 and 1.5 was recorded on Ir and Ni based contacts respectively.

Fig. 30. Forward I-V characteristics of as deposited Schottky diodes

Pt/Ti/Au contact delivered a barrier height of 0.6 eV and an ideality factor of 3.6. This high value of ideality factor clearly indicated the bad interface properties of Pt/semiconductor and a large deviation from TE behaviour. Pt reacts with Ga to form gallides, which deteriorate its performance (Preble et al.). These contacts were also found to be highly sensitivity to
surface conditions and very prone to the formation of bubbles due to high diffusivity of certain gases in Pt [24].

The barrier height and ideality factor are listed in Table 9.

<table>
<thead>
<tr>
<th>Schottky metal</th>
<th>Pt/Ti/Au</th>
<th>Ni/Ti/Au</th>
<th>Ir/Ti/Au</th>
</tr>
</thead>
<tbody>
<tr>
<td>Barrier (eV)</td>
<td>0.6</td>
<td>0.8</td>
<td>0.9</td>
</tr>
<tr>
<td>Ideality</td>
<td>3.6</td>
<td>1.5</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Table 9. Barrier height and ideality factor of Schottky diodes

Three terminal breakdown voltage was measured on these contacts using slope measurement method (gate was set to near pinch off condition and drain voltage was increased until the growth of drain current between two consecutive measurement points was bigger than 1.3).

This method enabled to distinguish between diode and channel breakdown since increase in both \( I_d \) (drain current) as well as \( I_g \) (gate current) was measured shown in Fig. 31. Simultaneous increase in gate and drain leakage current indicated diode breakdown. The highest breakdown voltage was measured on Ir based contacts compared to Ni and Pt, which could directly be correlated to low leakage current.

Very few studies have been found in the literature on the comparative effect of different gate metallization on breakdown voltage. Lu et al. [35] wrote that due to variation in the degree of strong coupling between electrons in different metals and the AlGaN surface donor electrons, the 2 deg sheet carrier concentration varies. Accordingly, different Schottky devices break down at different voltages. Fay et al. studied the gate sinking effect in case of Pt based Schottky contacts on InGaP/InGaAs/GaAs pHEMTs.

![Fig. 31. Breakdown voltage of as deposited Schottky diodes](image)

Since the Pt based contacts delivered poor performance and the literature survey remarked over their sensitivity to surface conditions [22], we carefully examined the surface preparations before the deposition of Pt based Schottky contacts.
2.2.3.2 Dependence of Pt based contacts on surface preparation

A fresh HCl / H₂O (1:10) pre-metallization dip was performed on wafer No. 1. On the other hand, wafer No. 2 was dipped in a few days stored HCl / H₂O (1:10) solution before the deposition of Pt based Schottky contacts. A significantly large value of Schottky barrier height (1.0 eV) along with low leakage current was recorded on wafer No. 1. On the contrary, a low value of barrier height (0.6 eV) and high leakage current was recorded on the wafer No. 2 shown in Fig. 32.

![Fig. 32. Effect of surface preparation on Pt based Schottky contacts](image)

This proved the fact that the Pt based contacts are very sensitive to the semiconductor surface conditions. These contacts deliver comparatively poor performance than Ni and Ir base contacts if the semiconductor surface is not well prepared before the contact deposition. However if the proper pre-metallization surface treatments are performed, Pt based contacts are capable of delivering noticeable performance similar to Ni and Ir contacts.

In all of the above-discussed Schottky metallization schemes, Ti was used as an intermediate layer to avoid reaction between Schottky contact metal and Au. In order to check the effect of different intermediate layers, we compared the performance of Ti with Mo intermediate layer. Mo was chosen due to its high melting point. The idea behind was also to improve high temperature performance of the device using Mo.

2.2.3.3 Comparison of Ti and Mo intermediate layers

- Pt/Ti/Au vs Pt/Mo/Au

These Schottky contacts were characterized before and after annealing at 600°C for 5 minutes. Schottky parameters were extracted from the forward I-V characteristics of as deposited (straight line graph) and annealed diodes (dotted line graph) drawn in Fig. 33. Both type of contacts showed leakage current which increased after annealing. Pt/Mo/Au contact showed a slightly greater value of leakage than the Pt/Ti/Au contact. However no significant difference in the barrier height and ideality factor was observed.
Fig. 33. Forward I-V characteristics of as deposited and annealed Schottky diodes

The barrier height and ideality factor before and after annealing are given in Table 10.

<table>
<thead>
<tr>
<th>Schottky metal</th>
<th>Pt/Ti/Au</th>
<th>Pt/Mo/Au</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Barrier (eV)</td>
<td>Ideality</td>
</tr>
<tr>
<td>As deposited</td>
<td>0.7</td>
<td>2.2</td>
</tr>
<tr>
<td>Annealed</td>
<td>0.6</td>
<td>2.3</td>
</tr>
</tbody>
</table>

Table 10. Barrier height and ideality of as deposited and annealed Schottky diodes

Effect of annealing on three terminal breakdown voltages was also checked and compared. Example of one device out from a bunch of measurements is given in Fig. 34.

The as deposited Pt/Mo/Au contact showed a slightly lower breakdown voltage (see Fig. 34a) compared to Pt/Ti/Au. This could be correlated with slight difference observed in leakage current.

As a result of annealing at 450°C (see Fig. 34b), breakdown voltage increased amazingly in both cases. This increment was larger in case of Pt/Mo/Au contact. After annealing at 600°C (see Fig. 34c), a further increase in breakdown voltage was recorded on the Pt/Ti/Au contact whereas a decrease was noticed on the Pt/Mo/Au contact. This showed the stability of Pt/Ti/Au contacts up to 600°C and the stability of Pt/Mo/Au contacts only up to 450°C. Hence, intermediate layers play an important role in determining the thermal stability of contacts.

A significant increase in breakdown voltage after annealing, regardless of any change in the barrier height and leakage current is still questionable.
Fig. 34. Breakdown voltage of as deposited and annealed Schottky diodes

- Ni/Ti/Au vs Ni/Mo/Au

Unlike Pt based contacts, use of different intermediate layers in Ni based contacts resulted different barrier heights. The forward Schottky diode characteristics of as deposited (straight line graph) and annealed contacts (dotted line graph) are shown in Fig. 35. These contacts did not suffer with the leakage current problem.

Fig. 35. Forward I-V characteristics of as deposited & annealed Schottky diodes

Extracted barrier height and ideality factor from the slope and intercept of curves are listed in Table 11.
Ni/Mo/Au contact showed greater value of barrier height than the Ni/Ti/Au contact, clearly indicating the effect of different intermediate layer. No significant difference was observed after contact annealing. Three terminal breakdown voltages was measured on as deposited as well as on annealed sample shown in Fig. 36.

<table>
<thead>
<tr>
<th>Schottky metal</th>
<th>Ni/Ti/Au</th>
<th>Ni/Mo/Au</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Barrier (eV)</td>
<td>Ideality</td>
</tr>
<tr>
<td>As deposited</td>
<td>0.7</td>
<td>1.7</td>
</tr>
<tr>
<td>Annealed</td>
<td>0.6</td>
<td>1.7</td>
</tr>
</tbody>
</table>

Table 11. Barrier height and ideality factor of as deposited and annealed Ni contacts

The breakdown voltage of as deposited Ni/Mo/Au contact was greater than Ni/Ti/Au, which was probably due to better diode characteristics.

However, as a result of annealing at 450°C and 600°C, a drastic decrease in breakdown voltage was recorded on the Ni/Mo/Au contact. This showed poor thermal stability of the contact. On the other hand, the breakdown voltage of Ni/Ti/Au contact increased after 450°C and decreased as a result of further annealing at 600°C. Therefore Ni/Ti/Au contact was stable up to 450°C.

Hence, these observations confirmed that the Schottky properties and thermal stability of Schottky contacts are very much dependent on the type of intermediate layer used.

Mechanism by which these intermediate layers influence the Schottky contact properties is questionable and needs to be analyzed.

In this way, we modified standard AlGaN/GaN HEMT technology by optimizing and modifying critical technology factors such as ohmic contacts, Schottky contacts and surface protection. We then compared the results of modified technology with standard technology to observe its contribution in the betterment of device performance.
2.3 Comparison of standard technology with modified technology

A comparison of standard technology with modified technology (summarized in Table 12) clearly shows the enhancement in device performance and very positive results of our efforts in technology optimization and modifications. The epitaxy design 1 given in Table 13 was used for comparison.

<table>
<thead>
<tr>
<th>Performance parameters</th>
<th>Standard technology</th>
<th>Modified technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Values</td>
<td>Remarks</td>
<td>Values</td>
</tr>
<tr>
<td>$I_{ds\text{max}}$ (A/mm)</td>
<td>0.7</td>
<td>Low current</td>
</tr>
<tr>
<td>$R_c$ ($\Omega$-mm)</td>
<td>0.4-0.6</td>
<td>Poor line edge definitions</td>
</tr>
<tr>
<td>$R_{source}$ ($\Omega$-mm)</td>
<td>0.85-0.9</td>
<td></td>
</tr>
<tr>
<td>$g_m$ extrinsic (mS/mm)</td>
<td>260</td>
<td></td>
</tr>
<tr>
<td>$\Phi_b$ (eV)</td>
<td>0.5</td>
<td>High leakage current and low barrier height</td>
</tr>
<tr>
<td>$n$</td>
<td>3</td>
<td>High ideality factor</td>
</tr>
<tr>
<td>$P_{out}$ (W/mm) @ 2 GHz</td>
<td>0.625</td>
<td>Low power levels</td>
</tr>
<tr>
<td>PAE (%)</td>
<td>14</td>
<td>Low power added efficiency</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>18</td>
<td></td>
</tr>
</tbody>
</table>

Table 12. A comparison of standard technology with modified technology

We succeeded in achieving high current and high power levels using SiN$_x$ surface passivation. The problem of proper gate alignment and alignment marks recognition due to poor line edge definition and surface morphology was solved by using Mo based ohmic contacts. Improving the semiconductor surface conditions using fresh HCl/H$_2$O dip before Schottky contact deposition solved the problem of high diode leakage current, high ideality factor and low barrier height.

We checked and achieved very good reproducibility of these results by running several process runs of modified technology.

Results obtained using modified technology compared very well with other groups [2,3], however serious efforts were needed to achieve the state of art performance. A state of art recess FP-FET demonstrated 12.0 W/mm output power, 21.2 dB linear gain and 48.8 % power added efficiency at 2 GHz [36].

After optimizing the device technology, next we tried to optimize the epitaxy design since the device performance depends very much on the type of epitaxy.

2.4 Optimization of epitaxy design

The Al$_{0.25}$Ga$_{0.75}$N/GaN HFET structures used in the processing were grown by MOCVD on 2" SiC and Sapphire wafers (courtesy of IAF, Freiburg). The epitaxy growth sequence started with the deposition of a 500 nm thick AlGaN layer followed by a 2.7 µm thick highly insulating GaN buffer layer, 3 nm Al$_{0.25}$Ga$_{0.75}$N spacer, 12 nm Si-doped Al$_{0.25}$Ga$_{0.75}$N supply layer, 10
nm Al<sub>0.25</sub>Ga<sub>0.75</sub>N barrier layer and a 5 nm thick GaN cap layer. A 25 nm thick AlGaN layer on the top of GaN buffer formed a two-dimensional electron gas (2 deg) at the AlGaN/GaN interface. A very similar design was adopted for Sapphire where the epitaxy structure started with a 25 nm thick low temperature GaN nucleation layer to reduce the misfit between Sapphire and GaN.

Hall data from the samples grown on semi-insulating SiC exhibited a sheet charge density of \( n_{2\text{DEG}} = 0.5 \times 10^{13} - 1 \times 10^{13} \text{ cm}^{-2} \) and a mobility of \( \mu_n = 1400 - 1500 \text{ cm}^2/\text{Vs} \) at RT (IAF, Freiburg).

We used two different epitaxy designs for processing. Design 1 was having a high-doped AlGaN layer compared to design 2 (see Table 13). Performance comparison of these two designs showed that the high-doped design resulted in higher output current and hence higher power output than the low-doped design. However, a trade off between high power output and high breakdown voltage proved the application specific importance of epitaxy designs.

<table>
<thead>
<tr>
<th>Layer sequence</th>
<th>Material</th>
<th>Design 1 (nm)</th>
<th>Design 2 (nm)</th>
<th>Design 3 (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cap</td>
<td>GaN</td>
<td>2</td>
<td>5</td>
<td>-</td>
</tr>
<tr>
<td>Barrier</td>
<td>AlGaN</td>
<td>10</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>Supply</td>
<td>AlGaN:Si</td>
<td>10: 3x10&lt;sup&gt;19&lt;/sup&gt;</td>
<td>12: 5x10&lt;sup&gt;18&lt;/sup&gt;</td>
<td>30: n.i.d</td>
</tr>
<tr>
<td>Spacer</td>
<td>AlGaN</td>
<td>5</td>
<td>3</td>
<td>-</td>
</tr>
<tr>
<td>Channel</td>
<td>GaN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Buffer</td>
<td>GaN</td>
<td>2700</td>
<td>2700</td>
<td>1200</td>
</tr>
<tr>
<td>Nucleation</td>
<td>AlGaN→GaN</td>
<td>500</td>
<td>500</td>
<td>-</td>
</tr>
<tr>
<td>Substrate</td>
<td>S.I. SiC</td>
<td>360000</td>
<td>360000</td>
<td>-</td>
</tr>
<tr>
<td>Al %</td>
<td>Al</td>
<td>25 %</td>
<td>25 %</td>
<td>30 %</td>
</tr>
</tbody>
</table>

Table 13. Epitaxy designs

Both designs contained the aluminium content (% Al) of 25 %. Increase in Al content of AlGaN theoretically results in an increase in channel sheet carrier density. This is due to an increase in the band gap discontinuity as well as spontaneous and piezoelectric polarization effect. Also, the large band gap of the AlGaN layer promises a large breakdown field. Therefore, in order to optimize epitaxy design, we studied the effect of change in Al content on the device performance. Design 2 was used for this study.

### 2.4.1 Effect of increase in the Al content

Increase in the Al content from 25 % to 30 % and 35 % resulted in an increase in the sheet carrier concentration from \( 0.4 \times 10^{13} \text{ cm}^{-2} \) to 1.0 and \( 1.5 \times 10^{13} \text{ cm}^{-2} \) (see Fig. 37). The mobility increased initially from 1400 cm<sup>2</sup>/Vs to 1500 cm<sup>2</sup>/Vs with an increase in Al content from 25 % to 30 %. However, it decreased to 1300 cm<sup>2</sup>/Vs as a result of further increase from 30 % to 35 %. This was perhaps the outcome of poor layer quality and the cracks generated due to increased tensile strain in the AlGaN layer.
Table 14 compares the d.c and r.f parameters of wafers having different Al contents. An increase in output power density from 4.2 W/mm to 6.4 W/mm was recorded as the Al content increased from 25 % to 30 % (see Fig. 38). This gain was the result of increased sheet carrier concentration and mobility due to increased Al content. However, output power density dramatically decreased to 3.5 W/mm with further increase in Al content to 35 %. We correlated this decrease with the decrease in mobility (see Fig. 37).

<table>
<thead>
<tr>
<th>Performance parameters</th>
<th>25 % Al</th>
<th>30 % Al</th>
<th>35 % Al</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{dsmax}$ (A/mm)</td>
<td>1.0</td>
<td>1.2</td>
<td>0.9</td>
</tr>
<tr>
<td>$V_p$ (V)</td>
<td>-5.0</td>
<td>-6.0</td>
<td>-5.0</td>
</tr>
<tr>
<td>$R_c$ (Ω-mm)</td>
<td>0.4</td>
<td>0.4</td>
<td>0.7</td>
</tr>
<tr>
<td>$g_m$ extrinsic (mS/mm)</td>
<td>230</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>$P_{out}$ (W/mm) @ 2 GHz</td>
<td>4.2</td>
<td>6.4</td>
<td>3.5</td>
</tr>
<tr>
<td>PAE (%)</td>
<td>30</td>
<td>50</td>
<td>35</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>18</td>
<td>21</td>
<td>19</td>
</tr>
</tbody>
</table>

Table 14. Effect of Al content on d.c and r.f parameters
2.4.2 Introducing AlN interface layer

An AlN interface layer of approximately 1 nm thickness was grown in between GaN buffer and composite AlGaN layers of design 3 (see table 13). This AlGaN/AlN/GaN HEMT structure was then compared with AlGaN/GaN HEMT structure (design 3, table 13). Introducing AlN interface layer resulted in an increase in power output from 5.0 W/mm to 7.5 W/mm as shown in Fig. 39. The AlN interlayer improved the electron mobility by reducing alloy related scattering at the heterointerface (Mishra et al.). In this way it contributed in power enhancement.

Table 15 shows the effect of AlN interface layer on d.c and r.f parameters.

<table>
<thead>
<tr>
<th>Performance parameters</th>
<th>With AlN layer</th>
<th>Without AlN layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{dsmax}$ (A/mm)</td>
<td>1.54</td>
<td>1.13</td>
</tr>
<tr>
<td>$V_p$ (V)</td>
<td>-7.1</td>
<td>-5.1</td>
</tr>
<tr>
<td>$R_c$ (Ω-mm)</td>
<td>0.45</td>
<td>0.53</td>
</tr>
<tr>
<td>$g_{m extrinsic}$ (mS/mm)</td>
<td>231</td>
<td>243</td>
</tr>
<tr>
<td>$P_{out}$ (W/mm) @ 2 GHz</td>
<td>7.5</td>
<td>5.0</td>
</tr>
<tr>
<td>PAE (%)</td>
<td>39</td>
<td>36</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>24</td>
<td>21</td>
</tr>
</tbody>
</table>

Table 15. Effect of AlN interface layer on d.c and r.f parameters
Fig. 39. Impact of introducing an AlN interface layer on output power

Conclusively, our adopted device intern related strategies, which dealt mainly with device technology and epitaxy design related issues, proved very promising. This approach benefited the overall device performance significantly.

Side by side, we tried to get deep insight into the peculiar problem of low recorded r.f power output on our wafers compared to high calculated d.c power (refer points to ponder in Fig. 11). Worldwide researchers facing the same problem named it current collapse. We thoroughly analyzed the problem on our wafers discussed in following chapter.
Chapter 3

Current collapse

Current collapse in AlGaN/GaN HEMT has been one of the most exciting topics in recent years. This is basically an observation in which the output power achieved from a device at microwave frequency of interest is considerably smaller than the expected one based on d.c characterization. The presence of surface and epitaxy related defects, traps or deep levels in the device structure are responsible for this observation.

The charge transfer process in these levels are too slow to follow high frequency signal therefore the electrons get trapped in them [37]. This disturbs the balanced charges in 2 deg and reduces the number of electrons available for current conduction. As a result of which the drain current reduces with an increase in knee voltage, thereby limiting the device power output. Hence this current collapse problem is a major obstacle in boosting up the overall device performance.

Intensive research works and studies have been performed worldwide to analyse and to solve this problem. Wu [38] was the first one to detect the problem of current collapse. Vetury proposed the possible locations of traps, which were responsible for current collapse. He first directly measured the negative surface potential between gate and drain. This suggested the presence of net negative charge on the surface. This negatively charged region therefore acts as a second gate or a virtual gate and limits the drain current conduction in the channel.

Shawn T. Bradley [39] used the low energy electron excited nanoscale luminescence (LEEN) to detect the defects in each layer of AlGaN/GaN HEMT and to correlate their effect with 2 deg confinement.

Ibbeston [40] proposed the theory of surface states as the origin of 2 deg.

S.C Binari [41] presented the current collapse effect attributed to surface and buffer layer trapping.

Many groups (U.C.S.B, University of south Carolina, Cornell university etc.) observed reduction in interface states after the deposition of high quality insulating silicon dioxide and silicon nitride layers on the surface of AlGaN.

Toshiba, Fujitsu and NEC groups proposed field plate structure to remove collapse.

Joshin et al. [42] introduced an n-type doped GaN cap layer in AlGaN/GaN HEMT and controlled the polarization induced surface charge. They observed reduction in the current collapse.

Ando et al. [43], [44] used recess gate and field plate structure in AlGaN/GaN HEMT to reduce the collapse effect. They observed an improvement in collapse factor from 22 % to 5 % using these structures.

We are presenting here our focused investigations and study on important aspects of current collapse problem. Dynamic I-V analyser (DIVA, details in appendix D) was used to perform the analysis.
3.1 Current collapse: A trap related phenomenon

Fig. 40. is showing a comparison of output characteristics at d.c (black curve) and at microwave frequency of interest (grey curve).

![Diagram showing current collapse](image)

**Fig. 40. Current collapse**

The expected power output (class A operation) at d.c \(P_{\text{out}}\) = \(\frac{1}{8} \times I_{\text{dsmax}} \times (V_{\text{br}} - V_{\text{knee}})\)

But at microwave frequency of interest,

\[I_{\text{dsmax}} < I_{\text{dsmax}} \text{ and } V_{\text{knee}} > V_{\text{knee}}\]

Hence the power output \(P_{\text{out}}\) at microwave frequency of interest is smaller than the power output \(P_{\text{out}}\) at d.c.

This phenomenon is named as current collapse, which originates due to deep levels, defects and traps. Impurity addition during growth, threading dislocation due to lattice mismatch, excess of carrier gases, uncontrolled growth parameters, increasing Al mole fraction, AlGaN relaxation, surface exposure and damage during device processing are the possible factors responsible for defects and deep levels. Fig. 41. is showing the possible trapping areas in device namely

I. Ungated AlGaN surface / interface
II. AlGaN layer
III. GaN buffer
IV. Interface area between substrate and buffer

![Diagram showing trapping regions](image)

**Fig. 41. Trapping regions in AlGaN/GaN HEMT structure**
Since the definition of current collapse stated a reduction in device power output, we studied its effect on our wafers.

3.2 Decisive role of current collapse in power reduction

In order to check if current collapse plays a decisive role in power reduction, we compared the static and dynamic characteristics of our three different devices using Dynamic I-V analyzer shown in Fig. 42. These three different devices were taken from three different wafers (IAF1, IAF2 and IAF3) having same epitaxy design but different epitaxy runs.

![Dynamic I-V Characteristics](image)

**Device D1**
- Current collapse = 11%
- 2x50 _ 0.5 µm _ IAF1
- Epitaxy run 1
- \( P_{\text{out}} = 5.2 \text{ W/mm @ 2 GHz} \)
- Load pull bias points:
  - \( V_{\text{gs}} = -3.7 \text{ V}, V_{\text{ds}} = 26.0 \text{ V} \)

**Device D2**
- Current collapse = 40%
- 2x50 _ 0.5 µm _ IAF2
- Epitaxy run 2
- \( P_{\text{out}} = 3.9 \text{ W/mm @ 2 GHz} \)
- Load pull bias points:
  - \( V_{\text{gs}} = -2.8 \text{ V}, V_{\text{ds}} = 26.0 \text{ V} \)

**Device D3**
- Current collapse = 67%
- 2x50 _ 0.5 µm _ IAF3
- Epitaxy run 3
- \( P_{\text{out}} = 1.8 \text{ W/mm @ 2 GHz} \)
- Load pull bias points:
  - \( V_{\text{gs}} = -2.6 \text{ V}, V_{\text{ds}} = 26.0 \text{ V} \)

**Fig. 42. Effect of current collapse on device power**

Static characteristics (showing thermal effects) are shown with black lines and dynamic characteristics are shown with grey lines. Pulses of 0.2 µs length and 1 ms width were used for the measurements. The devices were having a gate length of 0.5-µm and unit gate width of 100 µm.

Dynamic characteristics of device D1, D2 and D3 were measured at bias points \( V_{\text{gs}} = -3.7 \text{ V}, V_{\text{ds}} = 26.0 \text{ V} \); \( V_{\text{gs}} = -2.8 \text{ V}, V_{\text{ds}} = 26.0 \text{ V} \); \( V_{\text{gs}} = -2.6 \text{ V}, V_{\text{ds}} = 26.0 \text{ V} \) respectively. These operating points are shown by square. The percentage current collapse was calculated at \( V_{\text{ds}} = 10.0 \text{ V} \) and \( V_{\text{gs}} = 0.0 \text{ V} \) by using following formula:

\[
\text{Current collapse (\%)} = \frac{(I_{\text{static}} - I_{\text{Dynamic}})}{I_{\text{Static}}} \times 100
\]

Characteristics comparison of these three devices revealed the truth that device D3 suffered most with current collapse problem and therefore it delivered low power output of 1.8 W/mm @ 2 GHz. Whereas the device D1 which suffered least with this problem delivered high power output of 5.2 W/mm @ 2 GHz. Hence, it was clear that the current collapse plays a decisive role in power reduction.
This high percentage of the current collapse was either due to the surface related defects or epitaxy related defects [9]. So in order to find a way to differentiate between the two, we investigated current response to change in gate and drain bias conditions. A low quality wafer was selected to observe the clear effect. On the basis of these investigations and results analysis, we defined surface defect related anomalies as gate lag and epitaxy defect related anomalies as drain lag effect [45].

3.3 Gate lag

Gate lag is a significant reduction in the drain current when the gate voltage is changed abruptly. In order to observe this effect we compared the two characteristics curves measured under two different biasing conditions. One at $V_{ds} = 0.0$ V, $V_{gs} = 0.0$ V and other at $V_{ds} = 0.0$ V, $V_{gs} = -7.0$ V as shown in Fig. 43. Pulsing from steady state biasing points $V_{ds} = 0.0$ V, $V_{gs} = 0.0$ V resulted in an ideal I-V characteristics shown with black lines, whereas we observed a drastic decrease in drain current at steady state biasing points $V_{ds} = 0.0$ V, $V_{gs} = -7.0$ V as shown with grey lines. Therefore this phenomenon was named as gate lag.

![Fig. 43. Gate lag – An experimental observation](image)

Fig. 44a and b are indicating the corresponding internal device operation at these bias points. The channel was open and effect of access region was stronger at $V_{ds} = 0.0$ V, $V_{gs} = 0.0$ V shown in Fig. 5a. Whereas at $V_{ds} = 0.0$ V, $V_{gs} = -7.0$ V depletion region formed and this negative gate bias resulted in electrons leaking from the gate.

![Fig.44. Gate lag - Theoretical explanation](image)
These electrons got trapped in surface interface states, which were unable to follow the fast changes.
That’s how the surface became rich in negative charge and behaved like a virtual gate, which modulated the 2 deg. Hence, the drain current reduced as a result of expanded depletion region shown in Fig. 44b. The gate lag effect was attributed to surface states.

3.4 Drain lag

Drain lag is a combined effect of change in gate bias and drain bias voltages on current response. In order to observe this effect we compared again the two characteristics curves measured under two different biasing conditions.
One at $V_{ds} = 0.0 \, V$, $V_{gs} = -7.0 \, V$ and other at $V_{ds} = 20 \, V$, $V_{gs} = -7.0 \, V$ shown in Fig. 45.
Pulsing from biasing points $V_{ds} = 0.0 \, V$, $V_{gs} = -7.0 \, V$ resulted in I-V characteristics effected by gate lag shown with black lines.
Pulsing $V_{ds}$ from 0.0 V to 20.0 V at same pinch off condition resulted in significant decay in drain current as shown with grey lines. Therefore the phenomenon was named as drain lag or backgating.

Fig. 45. Drain lag – An experimental observation

Fig. 46a and b are indicating the corresponding internal device operation at these bias points. The gate lag effect (discussed in previous section) at $V_{ds} = 0.0 \, V$, $V_{gs} = -7.0 \, V$ is shown in Fig. 46a. At $V_{ds} = 20 \, V$, $V_{gs} = -7.0 \, V$, the electrons in the channel got excited due to high value of $V_{ds}$.

Defects in buffer layer trapped these excited electrons from channel, which produced backgating effect. Hence the depletion region expanded as shown in Fig. 46b and drain current reduced.
This drain lag effect was attributed to material related defects, epitaxy design and surface defects.
Fig. 46. Drain lag - Theoretical explanation

We believed that increase in device gate widths probably increase the defect density and hence current collapse percentage. Large area devices are needed in order to achieve high power levels. We tried to scale device periphery with power output and observed non-linear behaviour after a certain point. The increase in dislocation density and therefore the current collapse with increase in device size was considered as one reason for this non-linear scaling. In order to check this, we characterised devices of different gate widths on the same wafer as detailed here.

3.5 Effect of increase in gate width on current collapse

We measured the current collapse on 2 x 50 (D1), 8 x 125 (D2) and 16 x 125 (D3) μm devices. Static and dynamic characteristic comparison of these 3 different devices is shown in Fig. 47. The black and grey lines are corresponding to the static and dynamic characteristics respectively. The percentage current collapse was calculated at \( V_{ds} = 10.0 \text{ V} \) and the bias points are shown by squares.

Current collapse of 23 %, 16 % and 19 % was calculated on 2 x 50, 8 x 125 and 16 x 125 devices respectively.

Difference in above 3 values of collapse was not so pronounced that means an increase in the device periphery did not increase dislocation densities & current collapse percentage. Hence non-linear scaling was not the result of increased current collapse with device size.

In order to choose and stabilise the best Dynamic IV pulse analyzer (DIVA, details in appendix D) measurement parameters, we characterized our devices at different gate bias & drain bias voltages. Effect of change in pulse duration [39] and pulse separation was also checked. We are discussing these factors in details.
3.6 Effect of variation in pulse duration on current response

We used pulse duration of 0.2 µs for our normal investigation. In order to observe the effect of variation in pulse length on current response, we measured the dynamic drain current characteristics by pulsing the device with various pulse lengths ranging from 0.2 µs to 1000 µs. These were then compared with static characteristics as shown in Fig. 48.

The Grey, black lines and star sign curves are corresponding to static, dynamic measured at $L_g = 0.2 \mu s$ and at $1000 \mu s$ respectively.

We observed a 58% increase in drain current as a result of increase in pulse length from 0.2 µs to 1000 µs. That means the pulses of longer pulse duration provided sufficient time for trapped electrons to release and to participate in current conduction. Hence the current was recovered.
3.7 Effect of variation in pulse separation on current response

We used a pulse separation of 1 ms for our normal investigation. In order to observe the effect of variation in pulse separation on current response, we measured the dynamic drain current characteristics by pulsing the device with various pulse separations ranging from 1 ms to 20 ms.

These were then compared with static characteristics as shown in Fig. 49. The Grey, black and star sign curves are corresponding to static, dynamic measured at W = 1.0 ms and 20 ms respectively.
We observed a 10% increase in current as a result of increase in pulse separation from 1.0 ms (1 KHz) to 20 ms (50 Hz). This implies that there exist some traps, which charge up with very slow rate and therefore resulted in current increment. Effect of change in pulse duration on occupancy of traps was much more pronounced as compared to pulse separation.

### 3.8 Effect of variation in the bias points on current collapse

To observe the effect of variation in the bias points on current collapse, we measured the drain current at different gate-source and source-drain bias voltages. Fig. 50a is showing the dynamic characteristics comparison of the two curves measured at two different gate-source bias points keeping the source-drain bias voltage same. The black and grey lines are showing the dynamic characteristics measured at $V_{gs} = -0.7$ V, $V_{ds} = 26$ V and $V_{gs} = -2.7$ V, $V_{ds} = 26$ V respectively.

We obtained a 14% increase in gate lag value as a result of change in gate-source bias points. This was due to the fact that making gate-source bias voltage more negative resulted in increase trapping problem on the surface. Hence the depletion region extended, which reduced, even further the drain current and therefore gate lag increased.

![Fig. 50. Comparison of dynamic characteristics measured at different bias conditions.](image)

Fig. 50b is showing the dynamic characteristics comparison of the two curves measured at two different source-drain bias points keeping the gate-source bias voltage same. The black and grey lines are showing the dynamic characteristics measured at $V_{gs} = -2.7$ V, $V_{ds} = 26.0$ V and $V_{gs} = -2.7$ V, $V_{ds} = 34.0$ V respectively.

An increment of 11% in drain lag value was measured as a result of change in drain-source bias voltage. Increase in drain source bias voltage excited channel electrons, which were perhaps scattered in buffer layer and got trapped in material defects. Hence drain lag effect increased.
Based on our complete study and investigations, we concluded that the current collapse is the major limiting factor in boosting the microwave power of HEMT. Therefore we focused all our efforts to solve this problem.

3.9 Methods to check and solve the problem of current collapse

One of the major defect affected region in AlGaN / GaN HEMT lies in between gate and drain. Therefore modifying this area and thereby suppressing these surface and substrate defects could further enhance the overall microwave performance of device. Current collapse could be recovered by following ways.

A. Methods implemented at FBH

- Surface passivation

We passivated the channel i.e. the area between source and drain with thin layer of plasma enhanced chemical vapour deposited SiNx and thereby tried to suppress the surface/interface related traps [46]. As a result of which we were able to solve the current collapse problem to a greater extent. Effect of surface passivation is shown in Fig. 51.

The static and dynamic characteristics comparison in the left view graph shows that the current collapse before passivation was 44 %. After surface passivation this was 100% recovered as shown in right side view graph. Hence surface passivation proved to be one of the possible way to solve the current collapse problem. Effect of surface passivation on d.c characteristics is detailed in chapter 4 (sec. 4.1.1).

Fig. 51. Effect of surface passivation – An experimental observation
Trapped electrons between gate and drain region of device form a sort of virtual gate, which widen the depletion layer (see Fig. 52a). Hence current reduces and collapse increases. Surface passivation with thin layer of SiNx reduces this trapping and prevents virtual gate formation. This leads to depletion region narrowing (see Fig. 52b), therefore carriers move easily and collapse reduces.

![Diagram showing the effect of passivation on device behavior](image)

**Fig. 52.** Effect of passivation – Internal device behavior

The role that SiNx plays is not well understood. Different explanations given by different authors are still questionable. Vetury et al. believes that deposition of SiNx results in incorporation of Si as shallow donors at the AlGaN surface, which suppress the surface donors and reduce collapse.

According to Dang et al. [47], the observed increase in carrier concentration after SiNx passivation is consistent with a shift in the Fermi level at AlGaN surface towards the conduction band edge in the presence of SiNx compared to its position for free AlGaN surface. That means AlGaN/SiNx interface has a lower density of electronics states compared to free surface.

The piezoelectric induced charges due to change in stress (from passivation layer) between the gate and drain region has been proposed as a mechanism to change the surface charge and hence the channel conduction by Davis et al.

- Field plate structure

We compared the devices with and without field plate structure shown in Fig. 53. We recorded the percentage collapse of 43 % on the device without field plate. It reduces to 12 % as a result of field plate structure. Details on field plate structures are given in chapter 4 (sec. 4.3).
The field plate functions by reducing the electric field at the edge of the gate on the drain side (see Fig. 54), which prevents electron emission and electron trapping. In this way it helps in reducing the current collapse effect.

Mishra et al. recorded an increase in power density from 5.2 W/mm to 12 W/mm on Sapphire and from 8 W/mm to 18.8 W/mm on SiC along with reduced dispersion and increased PAE as a result of F.P structures. Wu et al. [48] demonstrated 32 W/mm @ 4 GHz by optimizing the field plate structure.
Light illumination

Light illumination helps in de-trapping the carriers and reduces the collapse effect. For an example, we measured 2x50 µm device (design 2, table 13) in dark as well as in light. We observed a dramatic increase in drain current as a result of light illumination shown in Fig. 55.

![Graph showing O/P Characteristics without and with light illumination](image)

**Fig. 55.** Effect of light illumination on traps – An experimental observation

This was a clear indication of de-trapping under light illumination.

Energy of incident photons in our experiment was approximately 3.1-1.7 eV (light wavelength between 400 to 700 nm), which was clearly less than the energy of AlGaN-GaN band gap. That means the possibility of intrinsic transition (band to band) was hindered.

Therefore extrinsic transition (see Fig. 56) was probably responsible in detrapping. Incident photons (of E<E<sub>g</sub>) were absorbed due to available energy states in the forbidden band gap (traps). These photons excited trapped electrons that moved out and contributed in conduction. Hence the drain current improved.

![Diagram showing de-trapping](image)

**Fig. 56.** De-trapping as a result of light illumination
B. Other methods from literature

- **n-type GaN cap**

Introducing n-doped GaN cap layer over AlGaN/GaN could also prevent virtual gate formation. Fujitsu Lab in Japan has demonstrated 174 W @ 2 GHz high efficiency HEMT using this technique to reduce the current collapse [49]. The n-doped cap layer flattened the valence band and reduced the conduction band edge (see Fig. 57), which therefore reduced the electric field between gate and drain region. Hence current collapse reduced.

![Fig. 57. Effect of n type GaN cap](image)

- **Recessed gate process**

The recess gate separates the channel from the surface traps. Since the gate is not directly placed upon the surface, there occurs no effective charging of the surface traps. So the virtual gate formation does not take place. Only the actual gate modulates the channel (see Fig. 58). Hence the collapse effect minimise. NEC corporation in Japan [50] has demonstrated recessed gate HEMT delivering 12 W/mm @ 2GHz with 21 dB gain and 48% PAE.
Fig. 58. Effect of recessed gate process

Beside these above discussed ways, some material & growth related issues that could also help in reducing the collapse effect are mentioned below.

- **LT – GaN multi interlayer buffer**

In order to get better quality buffer, successive growth of thick GaN layers separated by either LT- GaN or LT- AlN were investigated by M.Benamara et al. The method reduces the dislocation density at the intermediate buffer layers that act as barrier to dislocation propagation.

LT- AlN layer favours the generation of edge dislocations, leading to a highly defective GaN layer. On the other hand, use of LT- GaN as intermediate buffer layer appears as promising to obtain high quality buffer layer. The dislocation density reduced from $10^{11}/\text{cm}^2$ to $10^9/\text{cm}^2$.

- **Lateral epitaxial overgrowth**

In this method, the seed GaN layer grown on lattice-mismatched substrate is partially masked by an amorphous layer of SiN$_x$ or SiO$_2$. Regrowth occurs through opening in the masking layer such that threading dislocations are prevented from propagating by the masking layer. So the laterally overgrown GaN on the masked area is dislocation free. This helps in suppressing the material related defects density from $10^8 – 10^9$ to $10^6$ as mentioned by Vetury.

- **Controlled growth parameter**

By controlling various growth parameters such as temperature, pressure, gas flow etc., defect density could be well controlled. For example, increasing temperature and NH$_3$ flow result in less trap formation.

As already noticed in Fig. 51 and table 5 (chapter 2), the r.f power out increased and current collapse reduced after surface passivation. We are therefore dedicating the next chapter to the optimization and study of different surface passivation films.
Chapter 4

Current collapse suppression methods

4.1 Surface passivation

Many attempts were made to improve the surface condition by depositing thin passivation layers (discussed in Sec.2.2.1). These passivation layers mitigate current slump and microwave power degradation. Hence, surface passivation is surely a promising way to high power performance.

Luo et al. [51] from Florida university tested 3 different passivation layers (SiN$_x$, MgO and Sc$_2$O$_3$) to check their effectiveness in mitigating surface state induced current collapse. PECVD deposited SiN$_x$ produced a drain-source current recovery of 80-85 %. MgO and Sc$_2$O$_3$ produced essentially complete recovery of the current in GaN cap HEMT structures and 80-95 % recovery in AlGaN cap structures.

Ducatteau et al. [52] from IEMN-TIGER France recorded a power density of 2.9 W/mm before passivation. After SiO$_2$/Si$_3$N$_4$ passivation, it increased to 6.3 W/mm with 36 % PAE at 10 GHz.

Lee et al. [53] from Daimler Chrysler AG, Ulm showed that the drain current and transconductance of AlGaN/GaN increased from 610 mA/mm to 690 mA/mm and 150 mS/mm to 170 mS/mm as a result of SiN$_x$ passivation. Output power increased from 0.59 W/mm to 1.45 W/mm.

Green et al. [54] from Cornell University demonstrated at 4 GHz, an increase in saturated output power from 1.0 W/mm to 2.0 W/mm with an increase in PAE from 36 % to 46 % on AlGaN/GaN Sapphire based HEMT. Breakdown measurement data showed a 25% average increment in breakdown voltage.

Deposition of PECVD SiO$_2$ layer induced a significant increase in carrier concentration and decrease in mobility observed by Dang et al. [55] from University of California. Results indicated that the electronic density of states at the AlGaN surface is altered significantly and possibly reduced, in the presence of the SiO$_2$ passivation layer.

Our work concentrates on the optimization of passivation layers and deposition conditions to improve leakage current, power output and breakdown voltage of the device.

4.1.1 Surface passivation by PECVD SiN$_x$

The most trap-affected region is the device channel, more precisely the area between gate and drain. Therefore we passivated our device channel with a 100 nm SiN$_x$ layer deposited by plasma enhanced chemical vapour deposition (PECVD) technique.

This technique produces stable, well-adhered and reproducible nitride layers. Deposition conditions are given in Table 16.
Table 16. Deposition conditions of PECVD SiN$_x$

Silicon nitride was chosen for passivation because it is an electrical insulator having high strength over a wide range of temperature, high hardness and good chemical resistance. Properties of SiN$_x$ are listed in Table 17.

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness (nm)</td>
<td>100</td>
</tr>
<tr>
<td>Power (W)</td>
<td>100</td>
</tr>
<tr>
<td>Pressure (Pa)</td>
<td>80</td>
</tr>
<tr>
<td>Refractive Index</td>
<td>1.9</td>
</tr>
<tr>
<td>Temperature ($^\circ$K)</td>
<td>345</td>
</tr>
<tr>
<td>SiH$_4$ (sccm)</td>
<td>100</td>
</tr>
<tr>
<td>NH$_3$ (sccm)</td>
<td>12</td>
</tr>
<tr>
<td>Ar (sccm)</td>
<td>140</td>
</tr>
<tr>
<td>Deposition time (s)</td>
<td>300</td>
</tr>
</tbody>
</table>

Table 17. Properties of SiN$_x$

We characterized AlGaN/GaN HEMT devices before and after passivation. To check the clear effect of surface passivation, we compared the measurement results before and after passivation.

A drastic increase in maximum drain current density from 0.75 A/mm to 1.10 A/mm at $V_{gs} = +1.0$ V was recorded after passivation (see Fig. 59). That means the electron trapping effect minimized as a result of surface passivation, which increased electrons concentration in the channel and hence the output current.

We observed an increase in transconductance from 190 mS/mm to 220 mS/mm and an increase in pinch off voltage from – 2.7 V to – 3.1 V after surface passivation, as shown in transfer characteristics (see Fig. 60).

Reason behind was the decrease in source gate resistance after surface passivation. A normalized source-gate resistance was generally 1.1-1.2 $\Omega$mm before surface passivation. From this the intrinsic $g_{m,max}$ was calculated to be 247 mS/mm (extrinsic 190 mS/mm). A normalized source-gate resistance value of 0.85-0.9 $\Omega$mm was recorded after surface passivation. From this the intrinsic $g_{m,max}$ was calculated to be 285 mS/mm (extrinsic 220 mS/mm).
Fig. 59. Comparison of output characteristics before and after passivation

Device: 2 x 50_0.5 µm
Before passivation

Device: 2 x 50_0.5 µm
After passivation

$I_{ds} = 0.75 \text{ A/mm at } V_{gs} = +1.0 \text{ V}$

$I_{ds} = 1.10 \text{ A/mm at } V_{gs} = +1.0 \text{ V}$

Fig. 60. Comparison of transfer characteristics before and after passivation

Device: 2 x 50_0.5 µm
Before passivation

Device: 2 x 50_0.5 µm
After passivation

$g_m = 190 \text{ mS/mm at } V_{gs} = -1.9 \text{ V}$

$V_p = -2.7 \text{ V}$

$g_m = 220 \text{ mS/mm at } V_{gs} = -1.9 \text{ V}$

$V_p = -3.1 \text{ V}$
A 3-fold increment in maximum r.f-power was recorded on passivated HEMT indicated in Fig. 61. At 2 GHz, the maximum power density increased from 0.92 W/mm to a remarkable value of 3.1 W/mm. In addition, PAE reached to a value of 30 % from 12 % and gain benefited to 19 dB from 14 dB.

![Fig. 61. R.F characteristics before and after passivation](image)

An improvement in d.c and r.f characteristics was the result of current collapse recovery after surface passivation, shown in Fig. 62.

A current collapse value of 90 % was recorded before passivation which reduced to 42 % after passivation. Although SiN₅ passivation did not completely solve the current collapse problem, but it significantly reduced this adverse effect.

The mechanism behind was the suppression of surface/interface related traps by thin film of passivation layer. Trapping effect minimization facilitated increased number of electrons in the channel and reduction in source-gate resistance, hence the output current and r.f power increased.

Small signal r.f measurements after nitride passivation revealed a slight change in current gain cut-off frequency \( f_c \) from 11 GHz to 17 GHz but a noticable rise in maximum oscillation frequency \( f_{\text{max}} \) from 34 GHz to 54 GHz. An increase in \( f_{\text{max}} \) after passivation can be very well correlated with decrease in source resistance as according to the equation given below.

\[
F_{\text{max}} = f_c \sqrt{4 \left\{1 + \left[R_s + R_g g_0\right] + 2 \left(C_{gd}/C_{gs}\right) [C_{gd}/C_{gs} + g_m (R_s + 1/g_0)]\right\}}
\]
Fig. 62. Effect of surface passivation on current collapse

Remarkable enhancement in device performance proved the effectiveness and importance of SiN$_x$ surface passivation in HEMT device technology. However, a reduction in breakdown voltage (see Fig. 63) and a sharp rise in the gate leakage current (see Fig. 64) greatly diminishes its popularity.

Parasitic depletion caused by the trapping of electrons increases the breakdown voltage (decrease the drain current) before surface passivation. On the other hand, after surface passivation, this parasitic depletion region is removed which increases the electric field crowding near the gate edge. Hence the breakdown voltage decreases.

Fig. 63. Effect of PECVD SiN$_x$ passivation on breakdown voltage
Increase in the leakage current after surface passivation severely deteriorates the noise performance of the device. Origin of this leakage current and its type (surface (lateral) or a bulk (vertical)) has been a big question of debate.

Tan et al. [56] introduced test structures to differentiate between surface and bulk leakage components. They observed reduction in surface conduction due to effective passivation of electrical states along the ungated AlGaN surface by SiNx, which was accompanied by improved current collapse. Therefore, they concluded that the rise in the leakage was a consequence of increased bulk leakage contribution and not surface conduction. Increase in the bulk leakage was attributed to the result of increased edge leakage injection at the gate periphery.

On the other hand, the surface leakage current was found to be higher in high refractive index (Si-rich) SiNx compared to standard SiNx. Its effectiveness in mitigating current collapse suggested that surface leakage was not due to conduction along the surface state, but due to enhanced hopping conduction within Si rich dielectric film. They observed an increase in surface leakage current using low quality SiNx. Thus the quality of SiNx layer and the deposition conditions affected leakage current and breakdown voltage.

![Graph](image)

**Fig. 64.** Effect of PECVD SiNx passivation on three terminal gate leakage current

A recent literature survey showed that due to the use of SiH₄ and NH₃ gases in PECVD process, nitrides were detected to have a high hydrogen concentration (Li et al. [57]). This hydrogen content might be released and migrated into AlGaN and gate metallization through the subsequent device processes, thus creating defects and degrading device performance. Hydrogen plasma treatment was also found to produce nitrogen vacancy related defect levels on GaN and AlGaN surface. Excess leakage current based on the Fowler-Nordheim tunneling was observed in the SiNx/AlGaN structure, due to relatively small conduction band offset, $\Delta E_c$, of 0.7 eV between them (Hashizume et al. [58]).

It has also been accepted (IBM group in 1989) that the Pt and Pd used gate structure converts atomic hydrogen into molecular one by catalytic reaction. This molecular hydrogen is very easy to diffuse into the channel under the gate to compensate the donors and thus to cause hydrogen poisoning effect. Its known from the DRAM technology that H ions enhance the electric field and causes early breakdown.

Pearton et al. [59] showed that the PECVD deposited SiNx at 125°C incorporates H content of $3 \times 10^{19}$ cm$^{-3}$ to a depth of 0.6 µm. This high concentration of H was similar to that of Si.
which suggested the possibility of Si-H pair formation. Therefore the passivation of donors (electrical deactivation) was found to be the main effect of hydrogen.

We tried to improve the quality of PECVD nitride films by optimizing deposition parameters and by introducing pre passivation surface treatments to clean the semiconductor surface before nitride deposition.

4.1.2 Quality improvement of pcvd SiNₓ films

- **Optimization of deposition power**

One of the main parameter which influences the deposition rate and the density of the PECVD deposited layer is applied r.f power. In order to optimize it, we changed r.f power in the chamber, keeping the other parameters fixed.

We diced a wafer in two samples (sample 1 and sample 2). Nitride was deposited on sample 1 using a 100 W r.f power (our standard deposition parameter).

Since high power levels degrade device surface through high energy electrons, we deposited nitride on sample 2 using a reduced r.f power of 80 W.

A 3.4-fold increase in power output was recorded on sample 1 (100 W), whereas a 2.3-fold increase was recorded on sample 2 (80 W).

Since the silicon nitride film, deposited using a 100 W r.f power showed better performance. We adopted this optimized r.f power as a standard deposition parameter.

Unfortunately, the breakdown voltage decreased in both of the cases. Results are given in Table 18.

<table>
<thead>
<tr>
<th>R.F power</th>
<th>Increase in P&lt;sub&gt;output&lt;/sub&gt;</th>
<th>Change in breakdown voltage (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 W</td>
<td>3.4 times</td>
<td>-11</td>
</tr>
<tr>
<td>80 W</td>
<td>2.3 times</td>
<td>-22</td>
</tr>
</tbody>
</table>

Table 18. Effect of nitride deposition power on output power and breakdown

- **Pre passivation O₂ treatment**

The O₂ treatment has been traditionally used in device processing to clean the semiconductor surface. We introduced O₂ treatment before nitride deposition so that a good quality nitride layer can be grown on an impurity free surface.

We deposited silicon nitride directly on sample 1. Sample 2 was treated with O₂ plasma before nitride deposition. Table 19 lists the parameters used for O₂ surface treatment.

<table>
<thead>
<tr>
<th>Power (Watt)</th>
<th>Pressure (Pa)</th>
<th>Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>100</td>
<td>120</td>
</tr>
</tbody>
</table>

Table 19. Parameters used for O₂ treatment

Both samples showed an increase in current density after passivation. A 3.6-fold increase in output power was measured on sample 2 (O₂ treated sample) and a 3.2-fold increase was recorded on sample 1.
Oxygen treated sample delivered a slightly high value of drain current and r.f power output.

Due to high reactivity of oxygen with Al, oxygen incorporated probably in AlGaN and resulted in Al-O bond formation. The degenerated AlGaN layer produced by the oxygen donors caused tunneling assisted transport of electrons at the AlGaN/metal interface. This increased the sheet carrier concentration and hence the drain current (Jang et al. [60]).

Breakdown voltage increased after passivation as a result of pre-passivation O$_2$ treatment shown in Fig. 65. This increase was perhaps due to high availability of oxygen contents on the surface which suppressed the adverse effect of hydrogen contents present in silicon nitride films. Formation of Al-O compound could also be the another possible reason since the breakdown field of Al-O compound is greater than the breakdown field of SiNx.

![Fig. 65. Effect of O$_2$ treatment on breakdown voltage](image)

Results are summarized in Table 20. An optimization of parameters used for O$_2$ treatment could lead to even better device performance.

<table>
<thead>
<tr>
<th>Pre passivation treatment</th>
<th>Increase in $P_{\text{output}}$</th>
<th>Recovery in current collapse (%)</th>
<th>Change in breakdown voltage (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>With O$_2$ treatment</td>
<td>3.6 times</td>
<td>59</td>
<td>+12</td>
</tr>
<tr>
<td>With out O$_2$ treatment</td>
<td>3.2 times</td>
<td>50</td>
<td>-11</td>
</tr>
</tbody>
</table>

Table 20. Effect of O$_2$ treatment on device performance

- **Pre passivation NH$_3$ treatment**

In order to observe the effect of pre passivation NH$_3$ treatment on device performance, one part of a wafer (test sample) was treated with NH$_3$ before nitride deposition. Parameters used for this treatment are given in Table 21. Another part of the wafer was used as a reference sample on which the nitride was deposited directly without any pre treatment.
Table 21. Parameters used for NH₃ treatment

<table>
<thead>
<tr>
<th>Power (Watt)</th>
<th>Pressure (Pa)</th>
<th>Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>60</td>
<td>120</td>
</tr>
</tbody>
</table>

Both samples were characterized and compared. An equal increase in power output was noticed on these two samples. On the other hand, a 12 % increment in breakdown voltage was recorded on test sample (NH₃ treated) opposite to a 11 % decrease recorded on the reference sample (non NH₃ treated). Results are listed in Table 22.

<table>
<thead>
<tr>
<th>Pre passivation treatment</th>
<th>Increase in $P_{output}$</th>
<th>Change in breakdown voltage (%)</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>With NH₃ treatment</td>
<td>3.7 times</td>
<td>+12</td>
<td>Homogenous increase in $V_{br}$</td>
</tr>
<tr>
<td>With out NH₃ treatment</td>
<td>3.7 times</td>
<td>-11</td>
<td></td>
</tr>
</tbody>
</table>

Table 22. Effect of NH₃ treatment on device performance

Degradation in power output was expected due to the presence of hydrogen content in NH₃. However, experimental data amazingly did not show any reduction in power output. This observation led to the conclusion that the nitrogen content of NH₃ affected the device performance dominantly. Pre passivation NH₃ treatment resulted a nitrogen rich semiconductor surface which reduced the hydrogen migration in AlGaN during pecvd nitride deposition.

Homogenity in results confirmed the clear dominant effect of nitrogen content since nitrogen treated AlGaN or GaN normally exhibits very smooth and stoichiometric surface shown by Hashizume et al.

Increase in the breakdown voltage was perhaps due to the reaction of N with Al of AlGaN to form AlN. Breakdown field of AlN (15 MV/cm) is higher than SiNx (10 MV/cm) due to its large bandgap (6.2 eV) compared to SiNx (5.0 eV).

Hence, pre passivation surface treatments before nitride deposition effectively improved the nitride quality and device performance. We are using pre passivation NH₃ treatment in our process runs for better device performance.

Although the SiNx passivation layers have been proven effective, in reducing the effects of surface states, long term reliability studies demonstrating the stability of these layers have not been discussed much. High concentration of hydrogen in these layers can migrate into GaN or into gate metallization and deteriorate its performance. Therefore we investigated hydrogen free passivation materials namely Al₂O₃, SiO₂ and Ta₂O₅. Details are discussed in the following section.

4.1.3 Surface passivation by oxides

- Aluminum oxide (Al₂O₃)

Al₂O₃ is one of the native oxide of AlGaN. Due to its large bandgap (7-9 eV), a high dielectric constant (9-10) and a high breakdown field (> 10 MV/cm), it is surely a very attractive candidate for surface passivation. Therefore we passivated our devices using a sputtered thin film of Al₂O₃. Deposition conditions are given in Table 23.
Table 23. Deposition conditions of sputtered Al$_2$O$_3$

<table>
<thead>
<tr>
<th>Thickness (nm)</th>
<th>Power (W)</th>
<th>Pressure (mbar)</th>
<th>Refractive Index</th>
<th>Deposition Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>200</td>
<td>$5 \times 10^{-3}$</td>
<td>1.65</td>
<td>1900</td>
</tr>
</tbody>
</table>

We recorded a 4.5-fold increase in power output after Al$_2$O$_3$ passivation which was slightly higher as compared to 3.7-fold increase obtained after pecvd SiN$_x$ passivation (summarized in Table 24). Hence Al$_2$O$_3$ passivation proved to be very effective in suppressing the defects.

<table>
<thead>
<tr>
<th>Passivation material</th>
<th>Increase in $P_{\text{output}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pecvd SiN$_x$</td>
<td>3.7 times</td>
</tr>
<tr>
<td>Sp. Al$_2$O$_3$</td>
<td>4.5 times</td>
</tr>
</tbody>
</table>

Table 24. Effect of different passivation materials on power output

Three terminal gate leakage current characteristics before and after Al$_2$O$_3$ passivation are shown in Fig. 66. We did not observe increase in gate leakage current after passivation. Hence Al$_2$O$_3$ passivation solved the problem of leakage current normally observed after PECVD nitride passivation.

A sufficiently large conduction band offset ($\Delta E_c$) of 2.1 eV between Al$_2$O$_3$ and AlGaN compared to a small $\Delta E_c$ of 0.7 eV between SiN$_x$ and AlGaN was believed to be the possible reason. This large value of $\Delta E_c$ prevents Fowler Nordheim tunneling which is responsible for leakage current in SiN$_x$ films (Hashizume et al.)

![Fig. 66. Three terminal gate leakage current before and after Al$_2$O$_3$ passivation](image)

The breakdown voltage decreased after sp. Al$_2$O$_3$ passivation (see Fig. 67). Hence Al$_2$O$_3$ passivation solved the problem of leakage current, however a decrease in breakdown voltage after surface passivation still remained a question of concern.
Silicon oxide has already proven a very valuable material in Si business due to a low dielectric constant of 3.9, a large energy bandgap of 9.0 eV and a high breakdown field of 10 MV/cm. In order to check its effect on our devices, we deposited sputtered SiO$_2$ as another alternative passivating film. Deposition conditions are given in Table 25.

<table>
<thead>
<tr>
<th>Thickness (nm)</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power (W)</td>
<td>450</td>
</tr>
<tr>
<td>Pressure (mbar)</td>
<td>$4.2 \times 10^{-3}$</td>
</tr>
<tr>
<td>Bias (V)</td>
<td>400</td>
</tr>
<tr>
<td>Refractive index</td>
<td>1.47</td>
</tr>
<tr>
<td>O$_2$ (sccm)</td>
<td>0.4</td>
</tr>
<tr>
<td>Ar (sccm)</td>
<td>50</td>
</tr>
<tr>
<td>Deposition time (s)</td>
<td>1160</td>
</tr>
</tbody>
</table>

**Table 25. Deposition conditions of sputtered SiO$_2$**

The power output decreased by 31 % after silicon oxide passivation, listed in Table 26. Doubling the nitride thickness reduced this number to 16 %. Surface damage due to sputtering was perhaps one of the possible reasons responsible for power degradation.

<table>
<thead>
<tr>
<th>Passivation material</th>
<th>Reduction in $P_{out}$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sp. SiO$_2$ _ 100 nm</td>
<td>31</td>
</tr>
<tr>
<td>Sp. SiO$_2$ _ 200 nm</td>
<td>16</td>
</tr>
</tbody>
</table>

**Table 26. Effect of SiO$_2$ thickness on power output**

Fig. 67. Breakdown voltage before and after Al$_2$O$_3$ passivation
However, opposite to the power results, the majority of devices showed an increase in breakdown voltage after SiO$_2$ passivation (see Fig. 68).

![Fig. 68. Breakdown voltage before and after sp. SiO$_2$ passivation](image)

In addition, a sputtered Ta$_2$O$_5$ and a sputtered stack of SiO$_2$/SiN$_x$ were also investigated. Resulting data did not show any betterment in device characteristics.

Hence, Al$_2$O$_3$ established its image as an alternative passivation material to pecvd SiN$_x$ for delivering good device performance, by mainly solving the problem of leakage current.

Furthermore, we tried to achieve betterment in the overall device performance by passivating the device surface at quite an earlier stage in technology. A new technology developed using this approach was named as embedded-gate technology. This technology differed from our modified process technology (discussed in section 2.2) in the way the gates were fabricated. In addition, we passivated the device at quite an earlier stage to protect it from the possible damage produced by subsequent processing steps.

Implementing embedded gate technology is an effective way to solve the problem of current collapse. Embedded gate coming over the nitride layer acts as a field plate, which helps in reducing the current collapse. Pecvd SiN$_x$ was used instead of sp. Al$_2$O$_3$ due to the ease of SiN$_x$ etching process.
4.2 Embedded-gate AlGaN/GaN HEMT process technology

The detailed embedded gate technology is sketched in Fig. 69. From the step of reflector deposition to mesa isolation, we processed the device in the same manner as in modified process technology (see Fig. 12). This device was then covered by a 200 nm SiN$_x$ layer, which was structured using PMMA. An opening of 400 nm was defined in between source and drain using e-beam.

Through this opening, we anisotropically etched the first nitride layer in SF$_6$ and He plasma using ICP/RIE method. Etch selectivity ratio between PMMA and SiN$_x$ was 2.5. The etching parameters are given in Table 27.

<table>
<thead>
<tr>
<th>Process parameters</th>
<th>SF$_6$ Sccm</th>
<th>He Sccm</th>
<th>O$_2$ Sccm</th>
<th>Power ICP/RIE</th>
<th>Bias Volt</th>
<th>Pressure Pa</th>
<th>Time Sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiN$_x$ (I) etch</td>
<td>20</td>
<td>10</td>
<td>300/30</td>
<td>96</td>
<td>0.3</td>
<td>0.3</td>
<td>55</td>
</tr>
<tr>
<td>Rest resist etch</td>
<td>20</td>
<td>40</td>
<td>300/30</td>
<td>81</td>
<td>0.5</td>
<td>0.3</td>
<td>30</td>
</tr>
</tbody>
</table>

Table 27. Etching parameters used in embedded gate technology

PMMA was removed in O$_2$ and He (produce less surface damage) plasma which defined completely the gate foot of typical dimensions ranging from 350-400 nm shown in Fig. 70.
Fig. 69. Embedded – Gate AlGaN/GaN HEMT process technology
Fig. 70. Embedded – Gate foot (symmetrical structure)

In order to define the gate head, a bi-layer of PMMA was coated and structured. A 600 nm head was defined in this resist. Gate was then metallized and inspected in scanning electron microscope. A typical gate head dimension ranging from 740-800 nm was recorded shown in Fig. 71.

Fig. 71. Embedded – Gate head

In this way, a complete embedded-gate was defined with a foot of 350-400 nm and a head of 740-800 nm. Further processing included the removal of SiN, from rest of the device area and deposition of interconnect layer.

After these steps, we characterized the wafers and compared their performance with the wafers processed using modified technology.

4.2.1 Device characterization and comparison with modified technology

We compared output (Fig. 72), transfer (Fig. 73) and load pull (Fig. 74) characterization results of wafer No. 1 (modified technology processing) with wafer No. 2 (embedded gate technology processing).

Both wafers were having the same epitaxy design and same processing batch. These results are summarized in Table 28.
Fig. 72. Output characteristics (embedded gate technology vs. modified technology)

- **Wafer No. 1**
  - Modified technology
  - 2x125_0.6 µm

- **Wafer No. 2**
  - Embedded gate technology
  - 2x125_0.35 µm

- $I_{ds} = 1.2 \text{ A/mm at } V_{gs} = +1.5 \text{ V}$

- $V_p = -8.0 \text{ V}$

- $g_m = 170 \text{ mS/mm, } V_{ds} = 15.0 \text{ V}$

- $I_{ds} = 1.2 \text{ A/mm at } V_{gs} = +1.5 \text{ V}$

- $V_p = -6.3 \text{ V}$

- $g_m = 230 \text{ mS/mm, } V_{ds} = 15.0 \text{ V}$

Fig. 73. Transfer characteristics (embedded gate technology vs. modified technology)
Devices (gate length = 0.6 µm and gate width = 2 x 125 µm) on wafer No. 1 (modified technology) delivered a saturated drain current density of $I_{DS} = 1.2$ A/mm ($V_G = +1.5$ V), a transconductance of 170 mS/mm and a pinch off voltage of - 8.0 V.

A normalized source-gate resistance was generally 1.7 Ωmm. From this the intrinsic $g_{m, \text{max}}$ was calculated to be 236 mS/mm (extrinsic 170 mS/mm).

A similar value of $I_{DS}$ was recorded on devices (gate length = 0.35 µm and gate width = 2 x 125 µm) of wafer No. 2 (embedded gate technology). However a high transconductance value of 230 mS/mm was noted along with a positively shifted pinch off value of - 6.3 V.

This high value of transconductance was due to small gate length of embedded gates, reduced distance between gate and channel and the reduced source-gate resistance value of 1.4 Ωmm. From this the intrinsic $g_{m, \text{max}}$ was calculated to be 330 mS/mm (extrinsic 230 mS/mm).

Relationship between transconductance ($g_m$), gate length ($L_g$) and the distance between gate and channel ($a$) is given below.

$$g_m = \frac{(\varepsilon \cdot V_{\text{sat}} \cdot W)}{a} = \frac{(V_{\text{sat}} \cdot C_{gs})}{L_g}$$

Where $W$ is the channel width, $a$ the distance between gate and channel, $V_{\text{sat}}$ the saturation velocity, $\varepsilon$ the dielectric constant of semiconductor, $C_{gs}$ the gate source capacitance and $L_g$ is the gate length.

Reduction in the distance between gate and channel was due to slight etching of GaN surface. We calculated an etching of 4.0 nm.

Following formula was used for the calculation:

$$V_p = \left(\frac{q \cdot N_d \cdot a^2}{2 \cdot \varepsilon}\right)$$

Where $q = 1.602 \times 10^{-19}$ C, $N_d$ is doping density, $a$ the distance between gate and channel, $V_p$ the pinch off voltage and $\varepsilon$ is the dielectric constant of semiconductor.

<table>
<thead>
<tr>
<th>D.C and R.F parameters</th>
<th>Modified technology (Wafer No. 1)</th>
<th>Embedded gate technology (Wafer No. 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturation drain current density (A/mm)</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>Transconductance (mS/mm)</td>
<td>170</td>
<td>230</td>
</tr>
<tr>
<td>Pinchoff voltage (V)</td>
<td>- 8.0</td>
<td>- 6.3</td>
</tr>
<tr>
<td>Output power (W/mm)</td>
<td>2.7</td>
<td>4.5</td>
</tr>
<tr>
<td>Power added efficiency (%)</td>
<td>27</td>
<td>47</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>15</td>
<td>18</td>
</tr>
</tbody>
</table>

Table 28. Comparison of modified technology with embedded gate technology
An output power density of 4.5 W/mm and a PAE of 47 % was recorded on wafer No. 2 (embedded gate technology). These values were greater than the power density of 2.7 W/mm and a PAE of 27 % recorded on wafer No. 1 (modified technology). Reason behind was the field plate structure formed by embedded gate over nitride.

S-parameters were also measured up to 50 GHz. On wafer No. 1 (modified technology), we recorded $f_T$ value of 16 GHz and $f_{\text{max}}$ value of 27 GHz. On wafer No. 2 (embedded gate technology), an increase in $f_T = 30$ GHz and $f_{\text{max}} = 48$ GHz was measured. This increase in $f_T$ and $f_{\text{max}}$ is related with the small gate length and low source resistance in case of embedded gate technology.

Three terminal gate leakage current characteristics of wafer No. 1 and wafer No. 2 are drawn in Fig. 75. Characteristics of wafer No. 2 (embedded gate processing techno.) showed an improvement compared to wafer No. 1 (modified processing techno.). This could be due to the fact that the flow of the leakage current around the gate is prohibited by the pre deposited nitride.

**Fig. 74. Load pull results**

![Graphs showing load pull results for wafer No. 1 and wafer No. 2 with specific parameters listed.]
Fig. 75. Three terminal gate leakage current characteristics

These results confirmed that the embedded gate technology worked quite well and is surely a way to achieve betterment in device performance.

Additionally, we introduced different types of field plate structures to solve the problem of current collapse. We also checked the effect of variation in the field plate length.
4.3 Introducing field plate structures

The gate breakdown occurs at the drain side edge of the gate electrode due to high electric field. This electric field at the gate edge can be relaxed and shaped by the field plate (F.P) structures. The field plate changes the distribution of electric field at the edge of the gate on the drain side and reduces its peak value, which helps in increasing the breakdown voltage.

Therefore, we introduced three different types (type1, type2 and type3) of field plate structures in layout shown in Fig.76. Type 1 was a gate overlapped field plate structure. The field plate was connected to the gate through the common path of the gate feeder and pads in the extrinsic device region. The starting point of type 2 field plate was in between source and gate. Type 3 structure was having a F.P connected to the source.

We evaporated (e-beam) field plate metal as a second gate on top of the SiNx passivation layer. The F.P termination point was in between gate and drain. Field plate length was defined from drain side edge of the gate to F.P termination point. Effect of change in F.P length on device performance was also studied.

Fig. 76. Field plate structures

We compared the HEMT structures with and without these three types of field plates (fabricated on the same wafer). The effect of field plates on device output power is shown in Fig. 77a and 77b.

Devices used in Fig. 77a were having a source-drain distance of 4.5 µm, a gate length of 0.5 µm, source-gate distance of 1.0 µm and F.P lengths of 1.5 µm, 1.0 µm, 0.5 µm and 0.0 µm (no F.P).

Devices used in Fig. 77b were having a source-drain distance of 6.5 µm, a gate length of 0.5 µm, source-gate distance of 1.0 µm and F.P lengths of 2.5 µm, 2.0 µm, 1.0 µm, 0.5 µm and 0.0 µm (no F.P).

All the three types of field plate structures showed similar values of output power, which were greater than the power output recorded on HEMT structures without F.P.
Change in field plate length did not affect the power results significantly.

In order to know the reason behind the high power output recorded on F.P HEMT structures, we measured current collapse effect on both field plated and non field plated HEMT structures. Comparison of static vs. dynamic characteristics of two structures is shown in Fig. 78. A current collapse of 43 % was measured on device without F.P and only 12 % was measured on the device with F.P.

**Fig. 77. Effect of field plate structures on power output**

**Fig. 78. Effect of field plate structure on current collapse**
That means the F.P structures solved the current collapse problem and high field trapping effect. As a result of which, they delivered high power output.

Effect of field plate structures and field plate lengths on breakdown voltage is shown in Fig. 79a and 79b.

Devices used in Fig. 79a were having a source-drain distance of 4.5 µm, a gate length of 0.5 µm, source-gate distance of 1.0 µm and F.P lengths of 1.5 µm, 1.0 µm, 0.5 µm and 0.0 µm (no F.P).

Devices used in Fig. 79b were having a source-drain distance of 6.5 µm, a gate length of 0.5 µm, source-gate distance of 1.0 µm and F.P lengths of 2.5 µm, 2.0 µm, 1.0 µm, 0.5 µm and 0.0 µm (no F.P).

![Graph showing effect of field plate structure on breakdown voltage](image)

**Fig. 79.** Effect of field plate structure on breakdown voltage

Amazingly, as compared to non field plate HEMTs, lower values of breakdown voltage were recorded on the F.P HEMT structures having large field plate lengths. These observations were contrary to our expectations. However field plates having a length of 1.0 µm and 0.5 µm for a source drain distance of 6.5 µm delivered higher breakdown voltages compared to non field plated HEMT structure (see Fig. 79b).

That means a critical ratio between field plate length, source-drain distance and SiNx thickness must be optimized and attained [61-62], so that the electric field distributes optimally around the gate edge to deliver high breakdown voltages. We will devote our future efforts in this optimization process.

The breakdown voltages increased with decrease in field plate lengths. Since $L_{F.P.D}$ (see Fig. 76) increased with decrease in field plate length, the electric field reduced ($E \propto 1/d$) and hence the breakdown voltage increased.

Field plate structures result increase in gate-drain capacitance, which translates to reduction in $f_T$ and $f_{max}$ values ($f_T$ and $f_{max}$ are inversely proportional to gate-drain and gate-source capacitance).
Therefore F.P HEMT showed lower $f_r$ and $f_{\text{max}}$ values compared to non-F.P HEMTs shown in Fig. 80a and 80b.

**Fig. 80.** Effect of field plate structure on $f_r$ and $f_{\text{max}}$

Source connected field plate structure added extra gate-source capacitance which resulted further decrease in $f_r$. However, this capacitance reduces with decrease in field plate length, which resulted improvement in $f_r$ and $f_{\text{max}}$ values. Since the field plate adds to the input capacitance, it is favourable to minimize field plate length for high frequency response.

After implementing the device intern related strategies, we worked towards implementation of device extern related strategies to further strengthen the device results. These strategies are explored in next chapter.
Chapter 5

Layout optimizations, packaging and thermal issues

After technology optimization and stabilization, next we modified our layout/design to boost up the device output power. In simple terminology, the device output power is depending upon breakdown voltage and output current. Therefore, both of these factors must be increased in order to increase the output power. Distance between source and drain was optimized to increase the breakdown voltage. Since devices operated at high voltages are more prone to damage, we gave emphasis on increasing the device current. We introduced large periphery devices to increase output current. Additionally large devices were packaged for high power operations. These design modifications are discussed below.

5.1 Large periphery devices and packaging

In order to increase output current and output power performance, we introduced large periphery devices in design.

Device periphery was enlarged using following methods:

1. Increase in gate width
2. Increase in number of gate fingers
3. Grouping various transistor sub cells together to make a complete device on a single chip

In the first instance, we simultaneously increased the gate width and number of fingers to increase the device size.

Devices having unit gate width of 100 µm (2x50 µm), 1 mm (8 x 125 µm), 2 mm (16 x 125 µm) and 4 mm (16 x 250 µm) are shown in Fig. 81.

Fig. 81. Large and small periphery devices in design

Large signal on-wafer microwave measurements were made at 2 GHz using passive load-pull systems. On a device with a gate width of 4 mm (16x250 µm), we recorded a maximum output power of 13.8 W @ 2GHz. The corresponding efficiency (PAE) was 53 %, gain was 25 dB and decreased to 21 dB in saturation. The output power characteristic of a 16x250 µm device is shown in Fig. 82.
Next, we sketched scaling of $f_T$, $f_{\text{max}}$, and power densities with device gate widths.

Scaling of $f_T$, $f_{\text{max}}$, and maximum available gain with gate widths at $L_G = 0.5 \, \mu m$ is given in Fig. 83. A minor change in $f_T$ and maximum available gain was observed for the different devices. However, for $f_{\text{max}}$, a decrease can be observed with increase in gate width from 100 $\mu m$ to 4 mm. Since the source resistance (given in table 32) reduced with increased gate width, this degradation in $f_{\text{max}}$ may be explained by increased gate source capacitance with gate width.

**Fig. 82.** Output power characteristics of a 16x250 $\mu m$ device

**Fig. 83.** Scaling of $f_T$, $f_{\text{max}}$, and maximum available gain with gate width
Table 29. Effect of device gate width on $R_S$ and $C_{GS}$

<table>
<thead>
<tr>
<th>Device gate width (mm)</th>
<th>Source resistance ($R_S$) ($\Omega$)</th>
<th>Gate-source capacitance ($C_{GS}$) (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 µm</td>
<td>5.917</td>
<td>214</td>
</tr>
<tr>
<td>4 mm</td>
<td>0.231</td>
<td>6517</td>
</tr>
</tbody>
</table>

A scaling curve between power densities and device gate widths is shown in Fig. 84.

![Graph showing scaling curve between power density and gate width](image)

**Fig. 84.** Scaling of power density with device gate width

The power density of 5.2 W/mm scaled linearly with gate widths ranging from 100 µm width up to 2 mm. 4 mm wide devices deviated from this linear scaling and delivered a 66% reduced output power value than the expected value.

Some possible reasons behind this non-linear scaling at large periphery are as follows:

An increase in the gate fingers laterally increased the device size, as a result of which more phase delay and signal losses were introduced for signals to reach each gate finger. Activity and contribution of all gate fingers were therefore questionable, perhaps some fingers remained inactive due to signal loss and phase delay. The signal leaking to the underneath active device even further increased the loss.

Probably, the gate width of power transistors was already above its useful limit at which the losses imposed by the gate metal resulted in a loss of power density (i.e. power per gate width).

Reduction in output power due to current collapse problem (detailed in chapter 3) was considered as another possible reason of improper scaling at large periphery.

We therefore corrected our design first by reducing the number of gate fingers. Limiting the number of gate fingers to a value of 8, we introduced 8x125 µm (1 mm), 8x250 µm (2 mm) and 8x500 µm (4 mm) devices.
In addition gate design was modified using field plate structure to solve the current collapse problem (detail in chapter 4, sec.4.3) and feed line. This modified design was named as feed plate design (see Fig. 85), in which, the total finger width was segmented in parts of 125 µm widths [63].

Each of the segments had its own mesa isolation and a feeding connection to the gate was provided between each segment.

The passivation layers that also served as a mechanical support for the feed-plate-structure covered the gate structure and the transistor channel. Outside the mesa area at locations of the outer and intermediate gate-pads the insulating layers were fully removed.

![Fig. 85. Sketch of the feed plate design](image)

At the top a cross sectional view shows the feed-plate placed above the passivation layer. View from top reveals the connection of the feed-plate to the gate at locations between the mesas.

The feed-plate structure was located above the gate line at a distance according to the total thickness of the passivation layers. On each of the openings in the passivation layer a connection was provided from the feed-plate to the gate-pads.
The idea behind feed-plate design was to provide multiple gate access points and to reduce gate access resistance and inductance.

Now we tried again to scale power densities with respect to gate widths of newly designed large periphery devices. Fig. 86 shows that power density scaled linearly with device gate widths. A power density of 4 W/mm was observed for all 3 devices (8x125 µm, 8x250 µm and 8x500 µm). Reason behind the linear scaling of power density at large periphery was the reduction in gate resistance due to new feed-plate design. We calculated the gate resistance of 16x250 µm devices (4 mm, old design) and 8x500 µm devices (4 mm, new design). A simple formula used for this calculation is given below.

\[ R_g = \rho \frac{W}{3hL_g} \]

Where \( hL_g \) is the gate cross-sectional area, \( W \) the gate width, \( h \) the gate height and \( \rho \) is the resistivity.

We calculated a gate resistance value of 0.14 Ω/mm for 16x250 µm device. As a result of feed-plate design, a low gate resistance value of 0.09 Ω/mm was calculated for 8x500 µm device.

A power cell consisting of 8 fingers each having 500 µm gate width (new design) yielded a saturated output power of 42.3 dBm (17 Watt) at a drain voltage of 30 V. Linear gain of this power device was 21.6 dB and power added efficiency increased up to 46 %.

Next we designed power bars, which consisted of numbers of power cells grouped together. As an example power bar consisted of 5 individual power cells of type 8x250 µm grouped together is shown in Fig. 87.
Fig. 87. A 5x8x250 µm power bar design

Power bars were diced and packaged into commercial CuW-package (see Fig. 88). Packaging of the chips was accomplished by Au/Sn-soldering using solder preform of 25 µm thickness. Each power cell was connected to the package by wire bonding. Drain pads of all power cells were interconnected using wire bonding. Similar was done with gate pads. Source pads of each power cell were individually grounded rather than interconnection to avoid oscillations.
Load pull measurements on packaged power bar having a total width of 5x8x250 µm revealed 20 dB linear gain, 54 % PAE and output power of 44.5 dBm (28 W).

Measurements on a 5x8x500 µm power bar having 40 transistor fingers of 500 µm width showed a power level of 47.8 dBm (60 W) with PAE of 45 %.

A very high power output of 50 dBm (101 W) @ 2 GHz, a PAE of 40 % and a gain of 14 dB was recorded on an 11x8x500 µm packaged power bar shown in Fig. 89.
Another limiting factor in the performance of large periphery devices was thermal problem. We performed thermal simulations to study thermal issues.

### 5.2 Thermal simulations

Thermal simulations were performed using a three-dimensional finite-element model in the Nastran-Patran software package. The GaN chip dimensions used for simulation were $1.5 \times 2$ mm² with a device layout using parallel gate fingers. The active element of heat dissipation was represented by a 2-D planar heat source at each of the gate fingers, between gate and drain. For better comparison, the different device geometries used the same dissipated heat per gate width (5 W/mm) and a reference temperature of 27°C.

The simulation results (Table 30) of 4 mm (16x250 µm) and 1 mm (8x125 µm) devices showed a channel temperature of 92 and 77°C respectively. These simulations were performed under ideal conditions. During practical conditions air gap in between wafer chuck and wafer results in even higher temperatures. So the actual value of channel temperatures was perhaps even higher than the simulated ones. Therefore, the increase in channel temperature with device gate width was also believed to be the reason of non-linear scaling at large periphery.

Effect of packaging on channel temperature is shown in Fig. 90. The chip package was a standard CuW r.f power transistor package with a thermal conductivity of 180 W/mK. For die attachment a Au/Sn eutectic solder was used.

A higher channel temperature value of 143°C recorded on packaged 4 mm (16x250 µm) device compared to 92°C recorded on unpackaged 4 mm (16x250 µm) device proved that the simulation results were very much dependent on the heat sinking conditions. Also the thermal resistance of the chip package cannot be neglected.
Furthermore, in order to optimize device designs, we simulated the devices having different gate-drain distance, substrate thickness and substrate type. The effect of substrate type on channel temperature was studied by simulating 8x125µm and 16x250 µm devices. The simulation results in Table 31 shows the high channel temperature recorded on Sapphire due to its low thermal conductivity.

<table>
<thead>
<tr>
<th>Device size (µm)</th>
<th>Substrate</th>
<th>Package</th>
<th>Channel temperature (° C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16x250 (4mm)</td>
<td>SiC</td>
<td>Yes</td>
<td>143</td>
</tr>
<tr>
<td>16x250 (4mm)</td>
<td>SiC</td>
<td>No</td>
<td>92</td>
</tr>
<tr>
<td>8x125 (1mm)</td>
<td>SiC</td>
<td>No</td>
<td>77</td>
</tr>
</tbody>
</table>

**Table 30.** Simulated channel temperatures of 1mm and 4mm devices

<table>
<thead>
<tr>
<th>Device size (µm)</th>
<th>Substrate</th>
<th>Channel temperature (° C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16x250 (4mm)</td>
<td>SiC</td>
<td>92</td>
</tr>
<tr>
<td>16x250 (4mm)</td>
<td>Sapphire</td>
<td>679</td>
</tr>
<tr>
<td>8x125 (1mm)</td>
<td>SiC</td>
<td>77</td>
</tr>
<tr>
<td>8x125 (1mm)</td>
<td>Sapphire</td>
<td>361</td>
</tr>
</tbody>
</table>

**Table 31.** Effect of substrate type on channel temperature

**Fig. 90.** Effect of packaging on channel temperature
Decrease in the substrate thickness resulted slight decrease in channel temperature as shown in Table 32. Thinner substrates allow better heat removal, which results decrease in thermal resistance and hence decrease in channel temperature.

<table>
<thead>
<tr>
<th>Substrate thickness (µm)</th>
<th>Channel temperature (° C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>77</td>
</tr>
<tr>
<td>100</td>
<td>70</td>
</tr>
<tr>
<td>50</td>
<td>65</td>
</tr>
</tbody>
</table>

Table 32. Effect of substrate thickness on channel temperature_8x125 µm device

Increase in the gate drain distance provides increased area for the heat to spread in a more uniform manner. Hence thermal resistance and channel temperature reduce. We observed a slight decay in channel temperature as a result of increasing the gate drain distance from 1 µm to 5.5 µm (see Table 33).

<table>
<thead>
<tr>
<th>Gate-drain distance (µm)</th>
<th>Channel temperature (° C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>77</td>
</tr>
<tr>
<td>3.0</td>
<td>70</td>
</tr>
<tr>
<td>5.5</td>
<td>64</td>
</tr>
</tbody>
</table>

Table 33. Effect of gate-drain distance on channel temperature_8x125 µm device

Next, we tried to increase the device breakdown voltage as it also contributes in high power operation of the device. Distance between source and drain was optimized to increase the breakdown voltage.
5.3 Change in source-drain distance

We increased the source-drain distance from 2.5 µm to 4.0 and 7 µm, which resulted in an increase in breakdown voltage from 80 V to 150 V shown in Fig. 91a. On resistance increased from 2.3 Ω-mm to a value of 5.3 Ω-mm (see Fig. 91b).

An increase in breakdown voltage with source-drain distance was due to the extension of gate depletion region, which leads to the alleviation of the electric field peak at the gate edge.

The on resistance of a HEMT device may be represented as:

\[
R_{on} = \frac{(L_{ds})^2}{q\mu_n n_s} = \frac{(V_{BR})^2}{q\mu_n n_s (E_c - E_p)}
\]

Where

- \(L_{ds}\): Drain-source distance
- \(\mu_n\): Mobility
- \(n_s\): 2 deg density
- \(V_{BR}\): Breakdown voltage
- \(E_p\): Polarization field
- \(E_c\): Critical field

Above formula states that the on resistance follows a square rate with breakdown voltage and the source drain distance. Therefore it increased as a result of increase in the source drain distance.
Chapter 6

Conclusion

6.1 Summary

Base stations, which play a key role in wireless communication, operate at 2 GHz. The performance requirements for the output stage of third generation wireless base station are challenging for any device technology. The application requires that the devices operate at high efficiency and high power levels. AlGaN/GaN HFETs are beginning to show their supremacy and capabilities to satisfy these stringent requirements. Therefore our efforts in this thesis are focused on the development and investigations of AlGaN/GaN high electron mobility transistors (HEMT) for high power operations at 2 GHz.

To achieve high power levels at 2 GHz, we optimized device technology, epitaxy design and device layout/design. Also device performance limiting factor namely current collapse was thoroughly studied and different methods to solve this problem were implemented.

The Al\textsubscript{0.25}Ga\textsubscript{0.75}N/GaN HEMT structures were grown in a multiwafer MOCVD (6x2") reactor yielding high throughput and reproducibility. We started fabricating 2x50 µm devices on Sapphire and SiC using i-line stepper lithography. Technology maturation steps included contacts (ohmic and Schottky) optimizations and surface passivation. A nitride passivated 2x50 µm HEMT device delivered a power density of 5.2 W/mm at 2 GHz. DC characterization yielded a saturated drain current of 1.2 A/mm and an intrinsic transconductance of 360 mS/mm. For the gate length (L\textsubscript{G}) of 0.5 µm, a typical current gain cut-off frequency f\textsubscript{t} of 21 GHz was obtained. Therefore, the L\textsubscript{G} × f\textsubscript{t} product was around 10 GHz×µm. Devices having a 0.5 µm gate length and a 100 µm gate width revealed a maximum frequency of oscillation f\textsubscript{max} = 79 GHz.

Ohmic contacts were modified and a new scheme based on Mo based contact was realized. Ti/Al/Ti/Au/WSiN contacts possessed excellent surface morphology and low contact resistance (0.3 Ω-mm) but suffered with improper line edge definition. Mo based contact not only delivered good surface morphology and low contact resistance but also proper line edge definition. This allowed us to reduce the source-gate distance to achieve high-speed operation. We found that the formation of Al-Mo phase and GaMo\textsubscript{3} compound was the key factor responsible for the remarkable performance of Mo based contacts.

As an effort in the direction of optimizing Schottky contacts in our technology, we compared the performance of Pt, Ir and Ni based Schottky contact covered with highly conductive layer of Au. Ir based contact showed best performance in terms of barrier height and ideality factor. Pt based contact showed best performance in terms of thermal stability.

Device epitaxy design was next optimized to improve device performance. Increase in Al content from 25 % to 30 % resulted an increase in sheet carrier concentration from $0.4 \times 10^{13}$ cm\textsuperscript{-2} to $1.0 \times 10^{13}$ cm\textsuperscript{-2} with an increase in mobility from 1400 cm\textsuperscript{2}/Vs to 1500 cm\textsuperscript{2}/Vs. Output power density increased from 4.2 W/mm to 6.4 W/mm. Introducing AlN interface layer between AlGaN and GaN resulted increase in power output from 5.0 W/mm to 7.5 W/mm.

In spite of high power density recorded on our devices, current collapse remained a major limiting factor in device performance. We thoroughly studied current collapse effect using Dynamic I-V pulse analyser. Dynamic I-V pulse measurements proved that the current
collapse effect (trap related anomalies) was one of the major hindrances in boosting up the
device performance.
We implemented different methods to solve the current collapse problem.

Silicon nitride surface passivation proved its importance in HEMT device technology by
suppressing current collapse problem and remarkably enhancing device performance. However, a reduction in breakdown voltage and a sharp rise in the gate leakage current
greatly diminished its popularity.

Passivating the device surface with Al$_2$O$_3$ not only increased the power output but also
solved the problem of three terminal gate leakage current.

We developed a new embedded gate technology, which differed from our modified process
technology in the way the gates were fabricated. In addition, we passivated the device at
quite an earlier stage to protect it from the possible damage produced by subsequent
processing steps. Embedded gate coming over the nitride layer acted as a field plate, which
helped in reducing the current collapse.
Furthermore we introduced different types of field plate structures, which mitigated trap
related anomalies and provided potential enhancements in power performance capability of
device.

In order to boost up the power levels, we designed and fabricated large periphery devices
having different gate widths of 100 µm (2x50 µm), 1 mm (8x125 µm), 2 mm (16x125 µm) and
4 mm (16x250 µm). A maximum power level of 13.8 W was recorded on a 4 mm wide device.

The current collapse, design parasitic and thermal problems were supposed to limit the
performance of large periphery devices. Therefore we modified design of large periphery
devices using a new feed line and feed plate structure to solve the problem of current
collapse and design parasitic.
A newly designed (feed plate design) power cell consisting of 8 fingers each having 500 µm
gate widths, yielded a saturated output power of 42.3 dBm (17 Watt) at a drain voltage of 30 V.
Linear gain of this power device was 21.6 dB and power added efficiency increased up to 46 %.

These power cells were then grouped together to form power bars and were packaged into a
commercial CuW-package. A very high power output of 50 dBm (101 W) @ 2 GHz, a PAE of
40 % and a gain of 14 dB was recorded on an 11x8x500 µm packaged power bar.

Based on the outcomes of this research work, future efforts are suggested in the following
areas.

**6.2 Future work**

- Maturing the embedded gate technology
- Introducing single and multiple field plate structures in embedded technology
- Optimizing the ratio of F.P length and passivation thickness
- Recess gate process
- Testing n type GaN cap to reduce current collapse
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Appendix A

Measurement method

Measurement set up consists of AVT 110 probe station having 16 pins probing card. Hp 16058A test fixture provides current and voltage sources. S.C parameter analyzer 4145B displays the resulting ohmic/rectifying characteristics and extracts I, V and R values.

We patterned our contacts in TLM structures, which consisted of 4 contact pads separated by distances of 2, 4, 8 and 16 µm. These test structures were used in pairs to test the ohmic/rectifying nature of metal-semiconductor contacts. Injecting upto ± 50 mA current and measuring the voltage across same pairs of TLM pads drew I-V characteristics shown in Fig. 92.

![Fig 92. I-V characteristics showing rectifying and ohmic nature of contacts](image)

Resistance R between two contacts was measured using 4-point probe method. This resistance included the resistance of contact metallization and the semiconductor layer underneath the contacts shown in Fig. 93.

Therefore \( R = 2R_c + pL/W \)

Since \( p = R_{sh} \times h \)

This implied \( R = 2R_c + R_{sh} \times L/W \) \hspace{1cm} (1)
Fig 93. TLM structure

Where $R_c$ is the contact resistance, $\rho$ is the resistivity of semiconductor, $R_{sh}$ is the sheet resistance, $h$ is the mesa height, $L$ is the spacing between TLM pads and $W$ is the width of the pad.

$R$ was plotted against the contact gap spacing. Then a straight line was fitted to these experimental data using the method of least square (see Fig. 94).

This fitting program delivered a value of slope ($A$) and intercept ($B$) of the line, crossing the resistance axis at $2R_c$ point and an intercept distance axis at $-2L_t$ point.

Fig. 94. Total resistance $R$ vs. contact gap spacing $L$

Comparing eq$n$ of straight line ($R = AL + B$) with eq$n$ 1, we obtained

$A = R_{sh}/W$ and $B = 2R_c$

$\Rightarrow R_{sh} = A \times W$ in $\Omega/\square$ and $R_c = B/2 \Omega$
In order to normalize $R_c$, we multiplied it with 0.15 mm and obtained the value in $\Omega\cdot$mm.

Specific contact resistance or contact resistivity ($r_c$) is the contact resistance of a unit area for current flowing perpendicular to the contact.

Example:

$R_c = 0.5\ \Omega\cdot$mm (Ti/Al/Ti/Au/WsiNx)

$\Rightarrow r_c = 0.5 \times 150\ \mu$m $\times$ 2 $\mu$m
$= 1.5 \times 10^{-6}$ $\Omega\cdot$cm$^2$

$R_c = 0.3\ \Omega\cdot$mm (Ti/Al/Pt/Au)

$\Rightarrow r_c = 0.3 \times 150\ \mu$m $\times$ 2 $\mu$m
$= 0.9 \times 10^{-6}$ $\Omega\cdot$cm$^2$
## Appendix B

### Worldwide research on ohmic contacts

<table>
<thead>
<tr>
<th>Metal</th>
<th>Material</th>
<th>$R_c$ ($\Omega$-mm)</th>
<th>$\rho_c$ ($\Omega$·cm$^2$)</th>
<th>By</th>
<th>Techniques</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti/Al/Pd/Au$^+$ 25/220/60/160</td>
<td>n-GaN</td>
<td>4.21 x $10^{-8}$</td>
<td>Chor 500°, 8 min, N$_2$</td>
<td>Annelaing</td>
<td></td>
</tr>
<tr>
<td>Ti/Al</td>
<td>n-GaN</td>
<td>4.6 x $10^{-6}$</td>
<td>Chor 700°, 2 min, N$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pd/Ni/Au 20/30/200</td>
<td>p-GaN</td>
<td>5.03 x $10^{-4}$</td>
<td>Chor 450°, 2 min, N$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al/Ir/Au$^+$ 30/200/50/20</td>
<td>AlGaN/GaN</td>
<td>4.6 x $10^{-5}$</td>
<td>Fitch 850, 30 s, N$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al/Ni/Au 30/200/50/20</td>
<td>AlGaN/GaN</td>
<td>2 x $10^{-4}$</td>
<td>Fitch 850, 30 s, N$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al/Ni/Au$^+$ 30/180/40/150</td>
<td>AlGaN/GaN</td>
<td>0.2</td>
<td>7.3 x $10^{-7}$</td>
<td>Jacob 900, 30 s, N$_2$</td>
<td></td>
</tr>
<tr>
<td>Ru/Ni (5/5nm)$^+$</td>
<td>p-GaN</td>
<td>4 x $10^{-6}$</td>
<td>Jang 500, 1 min., O$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ir/Ni (5/5nm)$^+$</td>
<td>p-GaN</td>
<td>4 x $10^{-6}$</td>
<td>Jang 500, 1 min., O$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al$^0$</td>
<td>n-GaN</td>
<td>3 x $10^{-4}$</td>
<td>Lin 300, 3 min.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al$^0$ (35/115)</td>
<td>n-GaN</td>
<td>2 x $10^{-5}$</td>
<td>Kwak 600, 15 s.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ta/Ti/Al$^0$</td>
<td>n-AlGaN/GaN</td>
<td>5.3 x $10^{-7}$</td>
<td>Lim 950, 4 min</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Ta/Al$^0$</td>
<td>n-AlGaN/GaN</td>
<td>5.1 x $10^{-4}$</td>
<td>Lim 950, 4 min, N$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al/Pt/Au$^+$ 20/100/45/55</td>
<td>AlGaN/GaN</td>
<td>1.5-0.7</td>
<td>Bardwell 700, 30 s, N$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al/Pt/Au$^+$ 30/80/120/55</td>
<td>AlGaN/GaN</td>
<td>2.3-0.8</td>
<td>Bardwell 700, 30 s, N$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al/Pt/Au$^+$ 25/100/45/80</td>
<td>n-GaN</td>
<td>5.7 x $10^{-6}$</td>
<td>Lou 850,30s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al/Pt/Au$^+$ 25/100/45/80</td>
<td>n-AlGaN</td>
<td>8.89 x $10^{-9}$</td>
<td>Lou 850,120s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al/Ti/Au$^+$ 20/100/60/300</td>
<td>AlGaN/GaN</td>
<td>μ-structural analysis</td>
<td>Fay Ohmic after 750</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al/Pd/Au$^+$ 10/220/200/200</td>
<td>AlGaN/GaN</td>
<td>μ-structural analysis</td>
<td>Fay Ohmic after 750</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al$^+$ 20/100</td>
<td>AlGaN/GaN</td>
<td>8x10$^{-6}$, lowest value</td>
<td>Boudart 900,30s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al/Ni/Au$^+$ 15/220/40/50</td>
<td>n-GaN</td>
<td>8.9x10$^{-5}$</td>
<td>Boudart 900,30s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al$^+$ 20/200</td>
<td>n-GaN</td>
<td>7x10$^{-7}$</td>
<td>Bright 550, 1 min in argon</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al$^+$ 30/100/30/30</td>
<td>n-GaN</td>
<td>3x10$^{-6}$</td>
<td>Motayed 850, 30s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Pd/Al$^+$ 20/200</td>
<td>n-AlGaN/GaN</td>
<td>4.1x10$^{-6}$</td>
<td>Murai 600, 30s, N$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Pt/Al$^+$ 20/5/200</td>
<td>n-AlGaN/GaN</td>
<td>3.8x10$^{-5}$</td>
<td>Murai 650, 30s, N$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al$^+$ 16/200</td>
<td>n-AlGaN/GaN</td>
<td>5.9x10$^{-4}$</td>
<td>Murai 650, 30s, N$_2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ti/Al$^+$ 25/150</td>
<td>n-AlGaN/GaN</td>
<td>1.2x10$^{-5}$</td>
<td>Papanicolaou 950, 2 min</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal</td>
<td>Material</td>
<td>$R_c$ (Ω-mm)</td>
<td>$P_c$ (Ω.cm²)</td>
<td>By</td>
<td>Annealing</td>
</tr>
<tr>
<td>---------------------</td>
<td>----------------</td>
<td>--------------</td>
<td>---------------</td>
<td>------------</td>
<td>----------------</td>
</tr>
<tr>
<td>Ti/Al/Ni/Au</td>
<td>n-AlGaN/GaN</td>
<td>1.3x10⁻⁵</td>
<td>1.3x10⁻⁵</td>
<td>Papanicolaou</td>
<td>1100, 2 min</td>
</tr>
<tr>
<td>Cr/Al</td>
<td>n-AlGaN/GaN</td>
<td>3.8x10⁻⁵</td>
<td></td>
<td>Papanicolaou</td>
<td>700</td>
</tr>
<tr>
<td>Cr/Al/Ni/Au</td>
<td>n-AlGaN/GaN</td>
<td>2.3x10⁻⁵</td>
<td></td>
<td>Papanicolaou</td>
<td>950</td>
</tr>
<tr>
<td>Ti/Al/Re/Au</td>
<td>n-GaN</td>
<td>1.3x10⁻⁶</td>
<td></td>
<td>Reddy</td>
<td>750, 1min.</td>
</tr>
<tr>
<td>Ti/Al/Pl/Au</td>
<td>n-AlGaN/GaN</td>
<td>1.6x10⁻⁴</td>
<td></td>
<td>Shen</td>
<td>850, 5min.</td>
</tr>
<tr>
<td>Ti/Al/Ti/Au/WSiN</td>
<td>n-AlGaN/GaN</td>
<td>0.5</td>
<td>6 x 10⁻⁶</td>
<td>Nebauer</td>
<td>750, 30s</td>
</tr>
<tr>
<td>Mo/Al/Mo/Au</td>
<td>n-AlGaN/GaN</td>
<td>0.38</td>
<td></td>
<td>Selvanathan</td>
<td>800</td>
</tr>
<tr>
<td>V/Al/Mo/Au</td>
<td>n-AlGaN/GaN</td>
<td>0.22</td>
<td></td>
<td>Selvanathan</td>
<td>700</td>
</tr>
</tbody>
</table>
# Appendix C

## Worldwide research on Schottky contacts

<table>
<thead>
<tr>
<th>Metal</th>
<th>Material</th>
<th>(I-V) $\Phi_b$ eV</th>
<th>(C-V) $\Phi_b$ eV</th>
<th>By</th>
<th>Treatments/remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pt_50 nm</td>
<td>AlGaN/GaN</td>
<td>0.59</td>
<td>1.70</td>
<td>Lee</td>
<td>Without</td>
</tr>
<tr>
<td>Pt_50 nm</td>
<td>AlGaN/GaN</td>
<td>0.78</td>
<td>3.74</td>
<td>Lee</td>
<td>Pre metallization O$_2$ annealing</td>
</tr>
<tr>
<td>Pt_50 nm</td>
<td>AlGaN/GaN</td>
<td>0.84</td>
<td>2.69</td>
<td>Lee</td>
<td>Aqua regia treatment</td>
</tr>
<tr>
<td>Pt</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8</td>
</tr>
<tr>
<td>Ni</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Thermaly stable upto 400</td>
</tr>
<tr>
<td>PtSi</td>
<td></td>
<td>0.85</td>
<td></td>
<td>Liu</td>
<td>Degrades at 600</td>
</tr>
<tr>
<td>PdIn</td>
<td></td>
<td>0.84</td>
<td>1.09</td>
<td></td>
<td>Venugopalan Stable upto 650</td>
</tr>
<tr>
<td>Ni/Ga/Ni</td>
<td>15/15/26 nm</td>
<td>0.75</td>
<td>1.07</td>
<td></td>
<td>Venugopalan Stable after 700 for 10 min.</td>
</tr>
<tr>
<td>Rhenium(Re)</td>
<td>GaN</td>
<td>0.82</td>
<td>1.13</td>
<td></td>
<td>Venugopalan Stable upto 600</td>
</tr>
<tr>
<td>Ni/Au</td>
<td>30/100 nm</td>
<td>GaN</td>
<td>1.04 ± 0.05</td>
<td>Monroy</td>
<td></td>
</tr>
<tr>
<td>Ni/Ti/Au</td>
<td>30/5/100 nm</td>
<td>GaN</td>
<td>1.02 ± 0.03</td>
<td>Do</td>
<td></td>
</tr>
<tr>
<td>Pt/Au</td>
<td>30/100 nm</td>
<td>GaN</td>
<td>1.05 ± 0.05</td>
<td>Do</td>
<td></td>
</tr>
<tr>
<td>Pt/Ti/Au</td>
<td>30/5/100 nm</td>
<td>GaN</td>
<td>1.18 ± 0.07</td>
<td>Do</td>
<td></td>
</tr>
<tr>
<td>Pt/Ti/Au</td>
<td>30/5/100 nm</td>
<td>AlGaN</td>
<td>2 ± 0.1</td>
<td>Do</td>
<td></td>
</tr>
<tr>
<td>Ni/Au</td>
<td>20/200 nm</td>
<td>GaN</td>
<td>0.84</td>
<td>Qiao</td>
<td></td>
</tr>
<tr>
<td>Ni/Au</td>
<td>20/200 nm</td>
<td>Al$_{1-x}$Ga$_x$N</td>
<td>0.94</td>
<td>Qiao</td>
<td></td>
</tr>
<tr>
<td>Ni/Au</td>
<td>100 nm</td>
<td>Al$_{1-x}$Ga$_x$N</td>
<td>1.04</td>
<td>Qiao</td>
<td></td>
</tr>
<tr>
<td>Ni/Au</td>
<td>100 nm</td>
<td>Al$_{2-x}$Ga$_x$N</td>
<td>1.02</td>
<td>Qiao</td>
<td></td>
</tr>
<tr>
<td>Ni/Au</td>
<td>100 nm</td>
<td>Al$_{3-x}$Ga$_x$N</td>
<td>1.1</td>
<td>Karrer</td>
<td></td>
</tr>
<tr>
<td>Ni/Au</td>
<td>30/5/100 nm</td>
<td>GaN</td>
<td>0.92</td>
<td>Zhang</td>
<td></td>
</tr>
<tr>
<td>Ni/Au</td>
<td>30/5/100 nm</td>
<td>GaN</td>
<td>1.009</td>
<td>Lee</td>
<td>(NH$_4$)$_2$S$_x$ pre metal-lisation</td>
</tr>
<tr>
<td>Ni/Au</td>
<td>20/200 nm</td>
<td>GaN</td>
<td>0.856</td>
<td>Lee</td>
<td></td>
</tr>
<tr>
<td>Au</td>
<td>GaN</td>
<td>0.94</td>
<td>1.20</td>
<td>Noh</td>
<td></td>
</tr>
<tr>
<td>Ir_50 nm</td>
<td>AlGaN/GaN</td>
<td>0.68</td>
<td></td>
<td>Lee</td>
<td>As deposited</td>
</tr>
<tr>
<td>Ir_50 nm</td>
<td>AlGaN/GaN</td>
<td>1.07</td>
<td></td>
<td>Lee</td>
<td>500°C for 24 h</td>
</tr>
<tr>
<td>Au</td>
<td>GaN</td>
<td>0.84</td>
<td>0.94</td>
<td>Hacke</td>
<td></td>
</tr>
<tr>
<td>Au</td>
<td>GaN</td>
<td>1.19</td>
<td>1.15</td>
<td>Binari</td>
<td></td>
</tr>
<tr>
<td>Au</td>
<td>GaN</td>
<td>0.87</td>
<td>1.04</td>
<td>Schmitz</td>
<td></td>
</tr>
<tr>
<td>Pd_100 nm</td>
<td>GaN</td>
<td>0.94</td>
<td>1.04</td>
<td>Schmitz</td>
<td></td>
</tr>
<tr>
<td>Ni_100 nm</td>
<td>GaN</td>
<td>0.95</td>
<td>1.04</td>
<td>Schmitz</td>
<td></td>
</tr>
<tr>
<td>Pt_100 nm</td>
<td>GaN</td>
<td>1.01</td>
<td>1.05</td>
<td>Schmitz</td>
<td></td>
</tr>
<tr>
<td>Au</td>
<td>GaN</td>
<td>0.8</td>
<td></td>
<td>Polyakov</td>
<td></td>
</tr>
<tr>
<td>Au</td>
<td>AlGaN</td>
<td>1.1</td>
<td></td>
<td>Polyakov</td>
<td></td>
</tr>
<tr>
<td>Ni</td>
<td>AlGaN</td>
<td>1.1</td>
<td>1.1</td>
<td>Kuznetzova</td>
<td></td>
</tr>
<tr>
<td>Mo</td>
<td>AlGaN</td>
<td>1.4</td>
<td>1.1</td>
<td>Kuznetzova</td>
<td></td>
</tr>
<tr>
<td>Metal</td>
<td>Material</td>
<td>(I-V)</td>
<td>(C-V)</td>
<td>By</td>
<td>Treatments/remark</td>
</tr>
<tr>
<td>-------</td>
<td>----------</td>
<td>-------</td>
<td>-------</td>
<td>-----</td>
<td>-------------------</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\Phi_b$ eV</td>
<td>n</td>
<td>$\Phi_b$ eV</td>
<td>n</td>
</tr>
<tr>
<td>Au</td>
<td>GaN</td>
<td>0.89</td>
<td>1.11</td>
<td></td>
<td>Wu</td>
</tr>
<tr>
<td>Al</td>
<td>GaN</td>
<td>0.60</td>
<td>1.58</td>
<td></td>
<td>Wu</td>
</tr>
<tr>
<td>Mg</td>
<td>GaN</td>
<td>0.62</td>
<td>1.61</td>
<td></td>
<td>Wu</td>
</tr>
<tr>
<td>Ir</td>
<td>AlGaN/GaN</td>
<td>1.12</td>
<td></td>
<td></td>
<td>Lu</td>
</tr>
<tr>
<td>Ni</td>
<td>AlGaN/GaN</td>
<td>1.27</td>
<td></td>
<td></td>
<td>Lu</td>
</tr>
<tr>
<td>Re</td>
<td>AlGaN/GaN</td>
<td>1.68</td>
<td></td>
<td></td>
<td>Lu</td>
</tr>
<tr>
<td>Ag</td>
<td>GaN</td>
<td>0.82</td>
<td>1.01</td>
<td></td>
<td>Kampen</td>
</tr>
<tr>
<td>Pb</td>
<td>GaN</td>
<td>0.73</td>
<td>1.01</td>
<td></td>
<td>Kampen</td>
</tr>
<tr>
<td>Au</td>
<td>GaN</td>
<td>0.91</td>
<td></td>
<td></td>
<td>Khan</td>
</tr>
<tr>
<td>Ti</td>
<td>GaN</td>
<td>0.59</td>
<td></td>
<td></td>
<td>Binari</td>
</tr>
<tr>
<td>Au</td>
<td>GaN</td>
<td>1.19</td>
<td></td>
<td></td>
<td>Binari</td>
</tr>
</tbody>
</table>
Appendix D

Applications of dynamic I-V analysis (DIVA)

The major applications of dynamic I-V measurements are improvement of large signal model for r.f circuit design and analysis, technology development, process diagnosis, device design and optimization, heat sink design, manufacturing process control and production testing.

1 Improving large signal model

Device modeling traditionally starts from sets of measured static I-V characteristics. It is assumed that the transconductance and output conductance associated with these characteristics are also applicable at low and intermediate frequencies. But the models based on these static measurements provide a poor description of high frequency behavior because the static current voltage characteristics are the result of both fast and slow processes, but the slow processes do not respond to high frequency excitation.

The fast and slow processes have widely separated time scales. Fast processes are usually associated with carrier transport within the device. The charge transit time in modern high frequency devices are typically a few picoseconds. The most important slow processes are charge exchange with deep levels (traps) and self-heating. The time constants of these processes are typically in the range of microseconds to milliseconds.

Dynamic I-V measurement provides an effective solution to this problem. Dynamic I-V measurements are performed from a well-defined quiescent bias condition. The device temperature and deep level trap occupancies are determined by this quiescent condition. A dynamic IV characteristic is constructed from the currents that are obtained from pulsing to different temporary operating conditions.

The simplest modeling approach is to use dynamic IV data instead of static IV data in small signal and large signal device models, thereby using r.f values for transconductance and output conductance. This type of model replicates exactly what the practical device does at high frequency of operations.

2 Device design

Even a well-designed process will introduce some surface damage and a potential sensitivity of device performance to deep levels (traps). The sensitivity can be reduced by appropriate device design, e.g. of gate recess depths and widths. The difference between dynamic and static I-V measurements is an indication of the sensitivity of a particular device structure to deep level traps, and thereby provides a basis for differentiating between different device designs.

3 Process development

During processing, different etches, different dielectric films and different thermal processing steps can all leads to different amounts of damage in the region of semiconductor surfaces. Increased damage may have associated with it increased concentration of deep levels, and an increased sensitivity to the deleterious effects associated with charge exchange between free carriers and deep levels (traps).

The difference between dynamic and static IV measurements provides a useful diagnosis of the relative importance of deep levels and hence the amount of surface damage introduced by a particular process.
4 Manufacturing control

Dynamic IV measurements are useful for process control and production testing. When a production process goes out of specification, as much information as possible is required as soon as possible to diagnose the cause of problem. Dynamic IV measurements provide diagnostic information about the degree of surface damage. The information is related with static and other electrical measurements. Since dynamic IV measurements eliminate the low frequency response to self-heating and charge exchange with deep levels, they correspond exactly to the conduction characteristics a device will exhibit at r.f.

5 New technologies

New material systems invariably suffer from non-optimum technology that masks the true potential of devices constructed in the new material. Dynamic IV measurements contribute valuable insights into the performance potential of new technologies. These measurements allow the technologist to do is to see what the IV characteristics would look like if the process technology were advanced enough to have eliminated the surface state problem, and hence to determine the r.f power potential.

6 Heat sink design

Dynamic IV measurements allow the heat sink designer to optimize the r.f behavior at the operating temperature.
Appendix E

DIVA measurement set up and measurement method

1 DIVA instrument

An Accent model D225 dynamic IV analyzer (or DIVA hardware) instrument connected to a J micro technology personal probe station is used for pulse measurements. D225 is a single polarity instrument giving +25 V, 1 A output, capable of measuring all the FET’s and BJT’s devices except PNP bipolar.

The system runs from a standard IBM PC or compatible using the DIVA operating software. For probe station use, dc needle probes are not acceptable due to inductive loading they create on the pulse measurement. Instead microwave ground signal ground probes are used to make on wafer device connection.

The software has a graphical user interface through which the user sets up various parameters of the measurements. Input for FET / HEMT measurements include the minimum and maximum values for static or instantaneous voltages (minimum $V_{ds}$ is always zero and the $V_{gs}$ can range from negative to positive), the maximum static or instantaneous drain current and the maximum instantaneous power dissipated allowed.

Stability and ringing are the two practical considerations.

Parasitic in the fixturing and connections needs to be minimized to avoid instabilities. Undesired oscillation can occur in high gain devices even under resistive loading presented by the configuration of the measurement set up.

Long cables cause reactive loading of the pulse measurement, which can decrease device stability or cause ringing in the pulse waveform. Hence, cable length (more than 3 m) should be kept to minimum.

2 Set up information for static and dynamic IV measurements

I. $V_{ds}$ and $V_{gs}$: Maximum values of $V_{gs}$ and $V_{ds}$ are chosen on the basis of measured d.c and r.f characteristics. Maximum value of $V_{ds}$ is normally restricted to the breakdown voltage. In our measurements, we changed $V_{gs}$ from pinch off to +1.0 V and $V_{ds}$ from 0.0 V to 26.0 V.

II. $I_{dmax}$: This is the maximum drain current that the instrument will allow the device to pass. It is set depending upon the values of maximum voltages. It may as well be set to the instrument’s rating, which is 500 mA, 1 A or 2 A depending upon the DIVA variant. We selected a maximum value of 120 mA for our measurements.

III. Instantaneous power limit: To protect the device from destruction by self heating, a limit must be set for the instantaneous power the instrument will permit the device to dissipate. A reasonable rule is to take $(V_{ds} \times I_{max})/3$ to $(V_{ds} \times I_{max})/2$. We used a range of 5-8 W/mm.

IV. Average over: This is the number used to reduce the noise in the measured current by averaging over that number of samples. We used 32 points in our measurements.

V. Sweep rate: Sweep rate refers to the rate at which $V_{ds}$ is increased (in volt per second) to make a static IV measurement. This number sets the rate at which the drain source voltage is applied to the device as a continuous sweep. The value should be set so that a thermal steady state must be reached. We used 10 V/s.
In addition, following parameters must also be set for dynamic measurements.

VI. Bias point: This is the bias point about which the dynamic characteristics are to be measured. It can be anywhere in the \((V_{ds}, V_{gs})\) range of values that does not destroy the device. We used load pull bias points for dynamic measurements.

VII. \(V_{ds}\) step size: The no. is decided by how smooth the displayed curve needs to be. The graphic routine in DIVA simply connect the measured points with straight line segment, so the density of points in \(V_{ds}\) affect the smoothness of the measured curves. We selected a value of 0.5 V in standard measurements.

VIII. Pulse shape: There exists diverse range of pulse length (pulse duration) and pulse width (pulse separation) combinations to investigate the dispersion phenomenon. We used a pulse length of 0.2 µs and a pulse width of 1ms for our investigation.

3 The pulse measurement method

Fig. 95. shows the measurement set up which could be used for static as well as dynamic measurements.

![Fig. 95. Measurement set up]

D.C sources are connected at the gate and the drain terminal of the device. If the drain characteristics of the device are measured with steady static bias applied, a set of curves denoted by \(I_d\) \((V_{ds}, V_{gs})\) is obtained. If the characteristics are measured with fast voltage pulses (pulse of sub micron duration) applied synchronously to the drain-source and gate-source, a set of characteristics denoted by \(i_d\) \((v_{ds}, v_{gs})\) is obtained. This set includes trapping and heating effects and hence are different from \(I_d\) \((V_{ds}, V_{gs})\).

Fig. 96. is a diagrammatic representation of how the dynamic measurement instrument functions. The device is biased at a steady point with dc voltages indicated by the symbol A. The bias point may be set anywhere on the \(I_d\) \((V_{ds}, V_{gs})\) characteristics. The dynamic characteristics are then measured by pulsing both the gate-source voltage and drain source voltage synchronously away from this bias point to the point where the current is to be measured.
A complete set of dynamic IV characteristics is drawn by applying pulse voltages to the device from a quiescent bias condition to a temporary condition, and then backs to the quiescent condition. The result of measurement is a current that is measured while the device is at the temporary condition.

![Graph of dynamic IV characteristics with annotations for bias point and load line.](image)

**Fig. 96.** Measurement method
Appendix F

Worldwide research status of current collapse

1. Wu et al. detected firstly, the problem of current collapse.

2. Vetury et al.:

According to them, surface states are the localized states in forbidden energy gap, which appears due to modification of band structure. The presence of dangling bonds on the surface and its ionic or covalent nature modify the band structure. The experiments revealed the fact that the nature of bond in between constituent atoms of GaN is ionic and therefore crystal is less likely to have surface states. That means there is some other hidden factor responsible for surface of GaN. This unconsidered factor is the existence of polarization-induced fields in AlGaN/GaN heterostructure. This polarization field necessarily leads to existence of positively charged donor like surface states at the free surface.

Using floating gate as potential probe, they measured negative surface potential between gate and drain. This suggested the presence of net negative charge on the surface. This negatively charged region therefore acts as second gate or virtual gate and limits the drain current conduction in the channel. This virtual gate is formed due to the reduction in amount of net positive charge on the surface. This can occur by trapping of electrons on surface in donor like states. These electrons come from the gate metal and the gate–drain field, limits their supply. As the gate is biased more and more in reverse direction, leakage current increase and hence more and more electron get trapped to extend the depletion region under virtual gate. As a result of this, the electric field peak shifts and reduces at the actual gate edge. Hence the leakage current also reduces.

3. Bradley et al.:

They used the low energy electron excited nanoscale luminescence (LEEN) to detect the defects in each layer of AlGaN/GaN HEMT and to correlate them with 2 deg confinement. They analysed two samples, one with 2 deg (s1) and another without 2 deg (s2). Strong defect luminescence at 2.34 eV was localized in the AlGaN layer of s2 specimen, while the defect luminescence at 2.18 eV was localized in the GaN buffer layer of both samples. The presence of the intense 2.34 eV AlGaN defect emission was correlated with the absence of the 2 deg measured electrically. The absence of 2 deg was linked to high \((10^{17} / \text{cm}^2)\) defect densities of deep levels in the AlGaN and not to defects in the GaN surface or bulk layers.

4. Ibbeston et al.:

They proposed the theory of surface states as the origin of 2 deg. On ideal surface with no surface defects, increase in the thickness of AlGaN results in accumulation of hole or positive sheet charge due to shifting of valence band near to fermi level. And this positive hole charge sheet gives rise to 2 deg. Whereas on non-ideal surface with surface defects, surface states with net positive charge is formed. And this positive surface states results in the formation of negative 2 deg at the heterointerface.

5. Binari et al.:

They presented in details the effect of buffer and surface trapping on AlGaN/GaN HEMT device performance. The current collapse was attributed to buffer layer trapping, which was related to buffer layer resistivity.
6. Joshin et al.:
They introduced n-type doped GaN cap layer over AlGaN/GaN HEMT structure and controlled the polarization induced surface charge and hence the current collapse.

7. Ando et al.:
They proposed recess gate and field plate structure in AlGaN/GaN HEMT to reduce collapse effect. Collapse factor improved from 22 % to 5 % as a result of using these structures.

8. Parker et al.:
They studied the dispersion in HEMT and related charge trapping with impact ionization and gate leakage current. As the drain–gate potential increased, so did the drain–gate current and hence the negative trap potential, which therefore reduced the drain current. An increase in hole trap occupancy had the effect of increasing drain current. This occupancy depended on impact ionization and hence on drain bias.

They detected deep traps responsible for current collapse in GaN MESFET using a spectroscopic technique that employed the optical reversibility of collapse to determine the photo ionization spectra of the trap involved. In the n-channel device investigated, two electron traps observed were found to be very deep and strongly coupled to the lattice. Photo ionization threshold for these traps were determined at 1.8 V and at 2.85 eV.

10. Klein et al.:
They detected two deep traps responsible for current collapse in AlGaN/GaN HEMT grown by MOVPE using photo ionization spectroscopy. Varying the growth pressure of high resistivity GaN buffer layer resulted a change in the deep trap incorporation that was reflected in the observed current collapse. Variation in the deep trap concentration with growth pressure and carbon incorporation indicated that the deepest trap was a carbon related defect, while the mid-gap trap may be associated with grain boundaries or dislocations.

11. Mazzanti et al.:
They investigated the physical origin of the kink and its dynamic in AlGaAs/GaAs doped channel heterostructure field effect transistors both through measurements and 2D device simulations. The kink at large $V_{ds}$ was shown to arise from the interaction of surface deep acceptors with impact ionization generated holes, the latter partially discharging the deep levels and therefore leading to conductive channel widening and to drain current increase. Under pulsed operation, kink dynamics was governed by hole emission and capture phenomena, prevailing at low and high drain source voltages respectively. Current mode DLTS measurement revealed the presence of surface deep levels characterized by an activation energy of 0.36 eV. Since a comparison between d.c measurement and simulation suggested that ungated surfaces were negatively charged, deep levels were defined to be acceptor like.

12. Marso et al.:
They investigated the traps that were located between the substrate and the two-dimensional electron gas channel by observing the influence of a substrate voltage on the dc
characteristics of an AlGaN/GaN HEMT on Si. The transient of the drain current after applying a negative substrate voltage was evaluated in the temperature range from 30 to 100° C. With this method known as backgating current deep level transient spectroscopy, majority carrier traps with activation energy of 200 meV as well as minority carrier traps at 370 meV were identified.

13. Benamara et al.:

They investigated successive growth of thick GaN layers separated by either LT-GaN or LT-AlN to obtain high quality buffer layer. Use of LT-GaN as intermediate buffer layer appeared very promising and reduced the dislocation density from $10^{11}/\text{cm}^2$ to $10^9/\text{cm}^2$.

14. Amano et al.:

They investigated an improvement in crystalline quality of group III nitrides on sapphire using low temperature interlayer.

15. Jimenez et al.:

They proposed the effectiveness of p-doped cap over layer introduced in GaN JFET, in suppressing the current collapse. It screened the channel from surface state variations.

16. Miller et al.:

They studied the gate–drain transconductance and capacitance dispersion in HEFT.

17. Kohn et al.:

They studied the large signal frequency dispersion in AlGaN/GaN HEMT.

18. Khan et al.:

They suggested following solutions to the problem of current collapse:
Use of pulsed atomic layer epitaxy for depositing AlN and AlN/AlGaN multilayer with reduced density of dislocation of high Al concentration III-N structures, reduction of interface states by deposition of high quality insulating silicon dioxide and silicon nitride layers on the surface of AlGaN and development of a new MISDHEFT structures on sapphire substrate employing AlInGaN/InGaN (channel layer)/GaN double heterostructure.

19. Emcore:

They described the deep levels and surface states responsible for current collapse.

20. Germany research centre in Jülich

They explored the use of photo ionization spectroscopy and DLTS to study the traps in HEMT. Photo ionization measurement revealed traps with activation energy of 3.2 eV and 2.9 eV for heterostructure grown on sapphire and 1.85 eV for HFET grown on Si. Backgating current DLTS was used to identify minority (0.54 eV) and majority (0.44 eV) traps near the heterointerface.

21. Toshiba, Fujitsu and NEC:

They proposed field plate structure to remove collapse.
22. ATMI Inc, USA:

They reported an improvement in AlGaN/GaN HEMT structures by employing a delta doped AlGaN layer.

23. Microelectronics group of Padova University:

They hypothesised the presence of negative surface states due to hole traps (negative charge when empty, neutral charge when filled) in the ungated region.

24. Kim et al.:

They observed the existence of electron traps associated with surface and bulk defects. These electron traps were responsible for a decrease in transconductance and drain current.

25. Kim et al.:

They observed severe trapping problem in wafers having high Al mole fraction (42 % compare to 25 %). These trap states were believed to be generated from pinhole type defects.

26. Mitani et al.:

They performed two-dimensional analysis of breakdown characteristics in a narrow recessed gate GaAs MESFET. They showed that the breakdown voltage could be raised when moderate densities of surface states are included. However it was also suggested that with relatively high densities of surface states, the breakdown voltage could be drastically lowered when introducing the narrowly recessed gate structure.

27. Borgarino et al.:

They studied the hot electron degradation in AlGaAs/InGaAs/GaAs PHEMTs. The short gate needed for microwave operation and the low band gap energy of InGaAs channel made electron heating and impact ionization an important issue to be taken into account. As a consequence of the hot electron stressing, dc characteristics showed transconductance compression, threshold voltage instability, breakdown walkout and power slump. These effects were attributed to trap creation and charge accumulation under the gate or at the interface between semiconductor and passivation in the gate drain region.
Appendix G

Worldwide research on surface passivation of AlGaN/GaN HEMT

1. Ducatteau et al. from IEMN-TIGER France:

At 10 GHz, an increase in power density from 2.9 W/mm to 6.3 W/mm was obtained after \( \text{SiO}_2/\text{Si}_3\text{N}_4 \) passivation.

2. Anderson et al. from university of Florida:

The near lattice matched MgCaO grown via a digital alloy approach was proven to be more thermally stable than MgO oxides. The approach of using a reduced defect density single crystal MgCaO interfacial layer capped with a polycrystalline \( \text{Sc}_2\text{O}_3 \) layer appeared to represent the most stable heterostructure for passivation.

3. Hampson et al. from university of Illinois:

They reported on the successful use of spin deposited polyimide for the passivation of nitride HEMTs. The investigated devices were having a 0.23-\( \mu \)m gate length, two-finger geometry and a 2x75 \( \mu \)m total gate width. At 18 GHz, the passivation scheme yielded an improvement in power density from 2.14 W/mm to 4.02 W/mm and an improvement in PAE from 12.5 % to 24.47 %. Additionally, the passivated devices demonstrated a peak r.f power density of 7.65 W/mm with a peak PAE of 22.58 %, which demonstrated the promise of this technology.

4. Luo et al. from Florida university:

Three different passivation layers (\( \text{SiN}_x \), MgO and \( \text{Sc}_2\text{O}_3 \)) were examined for their effectiveness in mitigating surface state induced current collapse in AlGaN/GaN HEMTs. PECVD deposited \( \text{SiN}_x \) produced 80-85 % recovery of the drain-source current. Both the MgO and \( \text{Sc}_2\text{O}_3 \) produced essentially 100 % recovery of the current in GaN cap HEMT structures and 80-95 % recovery in AlGaN cap structures. The \( \text{Sc}_2\text{O}_3 \) had superior long-term stability, with no change in HEMT behaviour over 5 months aging.

5. Lee et al. from Daimler Chrysler AG, Ulm:

Drain current and transconductance of AlGaN/GaN increased from 610 mA/mm to 690 mA/mm and 150 mS/mm to 170 mS/mm as a result of \( \text{SiN}_x \) passivation. Out put power dramatically increased from 0.59 W/mm to 1.45 W/mm.

6. Shapoval S. et al. from institute of microelectronics technology:

Interface properties of \( \text{Si}_3\text{N}_4/\text{GaN} \) structures by capacitance voltage methods were studied, paying attention to semiconductor surface treatments before insulator deposition. ECR plasma deposition of \( \text{Si}_3\text{N}_4 \) and ECR plasma treatments of semiconductor surfaces were introduced. The interface state density depended on the hydrogen incorporation in ECR silicon nitride and its composition, which were found to be the function of ECR deposition parameters. Optical properties and H-content of the films were characterized by ellipsometry and Fourier transform infrared (FTIR) spectroscopy, respectively. Minimum interface state density (1x10\(^{11}\) cm\(^{-2}\) eV\(^{-1}\)) was recorded after optimization of \( \text{Si}_3\text{N}_4 \) films and ECR \( \text{O}_2 \) and \( \text{CF}_4 \) plasma treatment of GaN. Surface passivation using optimized \( \text{Si}_3\text{N}_4 \) films resulted an improvement in breakdown voltage along with an increase in saturation current, output power and power added efficiency.
7. Vitusevich et al. from Forschungszentrum Jülich, Germany:

They investigated low-frequency noise in passivated and nonpassivated AlGaN/GaN high electron mobility transistor (HEMT) grown on SiC substrate. The heterostructure layers were grown without intentionally doping the barrier material and two-dimensional gas appeared at the interface only due to polarization effects. Transmission line model structures with different lengths of the conducting channel were studied in a wide range of temperatures. The magnitude of the noise and Hooge parameter demonstrated a strong dependence on the distance between contacts. A reduction in noise factor was observed after passivation.

8. Green et al. from Cornell university:

Surface passivation of undoped AlGaN/GaN HEMT's reduced the surface effects responsible for limiting both the r.f current and breakdown voltages of the devices. Power measurements on a 2×125×0.5 μm AlGaN/GaN HEMT on sapphire demonstrated an increase in saturated output power from 1.0 W/mm (36 % PAE) to 2.0 W/mm (46 % peak PAE) at 4 GHz after passivation. Breakdown measurement data showed a 25 % average increase in breakdown voltage. Finally, 4 GHz power sweep data for a 2×75×0.4 μm AlGaN/GaN HEMT on sapphire produced 4.0 W/mm saturated output power and 41 % PAE (25 V drain bias) after surface passivation.

9. Zhang et al. from General Electric Global Research centre, Niskayuna, NY:

Correlation of device performance and defects in AlGaN/GaN HEMTs was investigated. Surface passivation using SiNx and Sc₂O₃ mitigated the surface trap related problems.

10. IMEC

They developed in-situ passivated Si₃N₄/AlGaN/GaN HEMT epiwafers, to increase the carrier density in the transistor. As a result of in-situ passivation, the source-drain (I_{ds}) current for a positive gate voltage of 2 V increased from 0.5 A/mm to 1.2 A/mm, while the maximum trans-conductance (g_m) improved from 130 mS/mm to 200 mS/mm. Small-signal r.f measurements revealed a current gain cut-off frequency (f_t) of 24 GHz and a maximum oscillation frequency (f_{max}) of 68 GHz without in-situ passivation layer. Whereas with in-situ passivation, f_t of 35 GHz and f_{max} value of 70 GHz were measured. Large-signal measurements performed on small devices showed a power-added-efficiency close to 50 % and a maximum output power of 3.8 W/mm at 4 GHz.

11. Hashizume et al. from Hokkaido university, Japan

They investigated effects of plasma processing, Si based dielectric and thin Al₂O₃ films on the chemical and electronics properties of GaN and AlGaN/GaN HEMT. The surface treatment in H₂ plasma excited by ECR source, produced nitrogen vacancy related defect levels at GaN and AlGaN surface, while the ECR N₂ plasma treatment improved electronic properties of the surface. The deposition of SiO₂ film on GaN and AlGaN surface was found to induce high-density interface states due to unexpected and uncontrollable oxidation reactions on the surface during the deposition process. The SiNₓ/GaN passivation structure showed good interface properties with the minimum interface density of 1x10¹¹ cm⁻² eV⁻¹. Due to relatively small conduction band offset of 0.7 eV between SiNₓ and AlGaN, an excess leakage current governed by Fowler Nordheim tunneling were observed. The Al₂O₃ passivation structure showed a good gate control of drain current due to large conduction band offset of 2.1 eV between Al₂O₃ and AlGaN.
12. Li et al. from University of California:

They developed high-density nitride with gaseous species of SiH₄ and N₂ process (NH₃ free) for GaAs PHEMT MMIC manufacturing. The breakdown voltage with high-density nitride (ICP source) showed an improvement of 50-70 % over standard PECVD films. The results indicated that a better nitride quality could be achieved with HD-ICP-CVD process.

13. Gillespie et al. from Air force research lab, Ohio:

They developed a novel process by depositing Si₃N₄ on the surface of AlGaN prior to device processing. In addition to improved dispersion, resulting devices showed an increase in drain current, reduction in gate leakage and over 3.5 times improvement in power measurements.

14. Dang et al. from University of California:

Deposition of a SiO₂ layer by PECVD induced a significant increase in carrier concentration and decrease in mobility that was largely reversed upon removal of the SiO₂ layer by wet etching. The observed increase in carrier concentration and reduction in mobility were quantitatively consistent with an approx. 1 eV shift in the Fermi level towards the conduction band edge in the presence of SiO₂ layer compared to its position for the free AlGaN surface. These results indicated that the electronic density of states at the AlGaN surface was altered significantly and possibly reduced, in the presence of the SiO₂ passivation layer.

15. Gregusova et al. from Institute of Electrical engineering, Bratislava, Slovakia:

D.C performance of the AlGaN/GaN HEMTs improved significantly as the stress in the passivation layer increased from compressive to tensile. It resulted changes in the sheet carrier concentration. Unlike d.c properties, r.f properties of the HEMT were found to be less sensitive to the stress.
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Nidhi
Vita

Nidhi Chaturvedi was born in 1977 in India. She received her M.Sc degree in Electronics from Banasthali vidyapith, India.

In 1998, she received Gold medal by prime minister of India Dr. Manmohan Singh (Ex-finance minister) for achieving top rank in university examinations.

Ministry of human resources and development, department of education, government of India for her studies, awarded her with scholarship.

From 1999-2001, she worked at the Central electronics engineering research institute, Pilani (CSIR) in India on design and development of GaAs MESFET and WDM devices based upon silica on silicon technology. She was involved in the projects sponsored by Indian space research organization (ISRO), Ahmedabad and MIT Delhi.

She was selected as a young scholar of the year in 2000 and was awarded with Arvind prem smriti award-2000 in India.

Since 2001, she is working as a Research scientist in Ferdinand-Braun-Institut für Höchstfrequenztechnik (FBH), Berlin, Germany and pursuing her PhD degree in Electrical Engineering from Technical University, Berlin.

Her research activities at FBH, Berlin, Germany involve design, fabrication and characterization of AlGaN/GaN HEMT devices.

She is coauthor of the best GAAs-2002 paper, which was awarded, in 10th European Gallium Arsenide and other semiconductors Application Symposium Conference, GAAS 2002, Milan, Italy.