Study on Resistive Mixer Circuits in Reconfigurable Mobile Communication Systems

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Zusammenfassung

Innerhalb des letzten Jahrzehntes haben mobile Kommunikationssysteme ein enormes Wachstum erfahren. Diese Entwicklung wird durch die Einführung neuen Kommunikation Standards unterstützt, die die Audio- und die Datenübertragungsqualität erheblich verbessern. Leider erfüllt jedoch noch immer kein drahtloses Kommunikationssystem alle Erwartungen hinsichtlich einer höheren Mobilität bei gleichzeitig größerer Datenrate. Genauso wenig gibt es ein Standard, der eine komplette Verfügbarkeit auf allen Kontinenten gewährleistet. Dieser Mangel eines universellen Standards erfordert die Entwicklung neuer rekonfigurierbarer Geräte, die in der Lage sind, mehrere Kommunikations Standards zu unterstützen.

Diese Entwicklung eines rekonfigurierbaren mobilen Empfangsgeräts, das die Kommunikationsstandard der dritten Generation UMTS, der amerikanische WLAN Standard IEEE 802.11a und die europäische Entwicklung HIPERLAN/2 zusammenführt, stellte den Ausgangspunkt für die folgende Arbeit dar. Das Front-end des Empfängers ist eine Kombination aus Super-heterodyne und Zero-IF Architektur und wurde durch eine systematische Analyse der Eigenschaften der eingesetzten Standards ausgewählt.

Um die praktische Umsetzbarkeit der untersuchten Prinzipien zur Rekonfigurierbarkeit zu demonstrieren, wurden die Schlüsselfunktionsblöcke des Front-Ends in einem hybriden Empfangsdemonstrators integriert, dessen Funktionalität eingehend untersucht worden ist.

Die Funktionsblockanalyse wird auf die Blöcke zur Frequenzumsetzung eingeschränkt. Ein breiter Überblick über den unterschiedlichen Mischerlösungen wird dargestellt. Der passive Mischer hat sich angesichts seiner Linearität- und Rauschperformance gegenüber allen anderen Mischerarten durchgesetzt. Die Schaltungsentwicklung, die Implementierung und

die Performancecharakterisierung eines solchen Mischers sind in diesem Dokument ausführlich beschrieben. Neben der praktischen Implementierung, wurden auch theoretische Aspekte, wie das Intermodulationsverhalten und die Abhängigkeit dieses Verhaltes von der Amplitude des LO (local oscillator) Signals, oder der Transistorsvorspannung untersucht.

Abstract

In the past decade, portable mobile communication systems have experienced a tremendous growth. This development is fully supported by the introduction of new communication standards that push the voice and data transmission quality to new limits. Unfortunately, still no wireless standard can fulfill all the expectations concerning a higher mobility and superior data rates. Neither is there a standard that offers a complete coverage on all continents. These realities create the necessity for new reconfigurable devices able to support several communication standards.

A reconfigurable mobile terminal, which supports the third generation Universal Mobile Telecommunication System UMTS, the American wireless LAN standard IEEE 802.11a and its European counterpart – HIPERLAN/2 represented the motivation for the following work. Its receiver front-end is a combination of heterodyne and zero-IF architectures and was chosen based on a systematic analysis of the standards employed.

The functional block analysis is restricted to the frequency conversion blocks. An extended overview over the different mixer solutions is presented. The most suitable mixer solution for the present project was considered to be the resistive mixer whose design, implementation and measurement is described in detail along the document. In extension to the practical implementation, a theoretical investigation of the intermodulation behavior is present. The theory explains the dependency between the mixer intermodulation performance and the transistor biasing.

In order to demonstrate the applicability of the reconfiguration principle, the key functional blocks of the receiver have been developed, implemented and tested in a hybrid front-end, which is fully described together with some of the measurement results.

Contents

List of Tables

List of Figures

Abbreviations

3GPP	Third generation partnership project
P1dBCP	1-dB compression point
ACS	Adjacent channel selectivity
ADC	Analog-to-digital converter
ADS	Advanced Design System
AP	Access point
ARIB	Association of Radio Industries and Broadcasting
ATM	Asynchronous Transfer Mode
BB	Baseband
BER	Bit error rate
BRAN	Broadband Radio Access Networks
BPSK	Binary phase shift modulation
BS	Base station
CDMA	Code division multiply access
CC	Central controller
CG	Coding gain
CMOS	Complementary metal-oxide silicon

CSF	Channel select filter
CSMA	Carrier sense multiple access
DC	Direct current
DCR	Direct conversion receiver
DL	Downlink
DLC	Data link control
DPDCH	Dedicated physical data channel
DPCCH	Dedicated physical control channel
DR	Dynamic range
DSP	Digital signal processor
ETSI	European Telecommunication Standard Institute
FDD	Frequency division duplex
FE	Front-end
FFT	Fast Fourier transformation
GSM	Global System for Mobile Communications
HIPERLAN	High Performance Radio LAN
ICI	Inter carrier interference
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate frequency
IP	Internet protocol
IIP2	Input referred second-order intercept point
IIP3	Input referred third-order intercept point
IMD	Intermodulation distortion
IMT 2000	Mobile Telecommunications 2000

ISI	Inter-symbol interference
ISM	Industrial Scientific and Medical frequency allocated spectrum
ITU	International Telecommunication Union
LAN	Local area network
LNA	Low noise amplifier
LO	Local oscillator
MAC	Media access control
MFSK	Multiple frequency shift keying
MMAC	Multimedia Mobile Access Communication
MT	Mobile Terminal
OCNS	Orthogonal channel noise simulator
OFDM	Orthogonal frequency division multiplex
PAR	Peak to average power ratio
PER	Packet error rate
PDU	Packet data unit
PHY	Physical layer
PPP	Point to Point Protocol
PSD	Power spectrum density
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift modulation
RF	Radio frequency
RFVGA	Radio frequency variable gain amplifier
RTT	Radio Transmission Technology
SAW	Surface acoustic wave

SDR	Software defined radio
SF	Spreading factor
SG	Spreading gain
SNR	Signal to noise ratio
SPI	Seria
SPO	Signal path optimization
TDD	Time division duplex
TDMA	Time domain multiple access
UE	User equipment
UL	Uplink
UMTS	Universal mobile telecommunication system
UNII	Unlicensed National Information Infrastructure
U-SDU	User service data units
UTRA	Universal terrestrial radio access
VCO	Voltage controlled oscillator
VGA	Variable gain amplifier
WLAN	Wireless local area network
ZIF	Zero intermediate frequency

Introduction

There is a great diversity of wireless communication standards existent on the market today, covering all spectrums of applications. This diversity expresses itself not only technologically but also geopolitically, each region developing its own standards. Such multitude of communication standards leads to increased development effort for both stationary and mobile equipment. Multi-standard devices emerged as a viable solution to some of the problems generated by this diversity. One can classify three main directions in the development of reconfigurable multi-standard terminals, each having its own requirements and particularities.

The first type of reconfigurable terminals came as a necessity dictated by the differences in standards and spectrum allocation in different geographical regions. These systems aim to provide coverage and accessibility to people that are traveling from one continent to another and do not require simultaneously support of more standards.

The second direction is economically motivated and acts as a path-smoother for new emerging standards and technologies. The best example is the development of GSM/UMTS multi-standard terminals that take advantage of superior data rates of UMTS and full coverage of GSM. Such devices are seen as temporary solutions until the new standard is fully deployed and market accepted. A mark of quality for these terminals is the ability to handover from one standard to the other, meaning that the change is made without interaction of the user.

The third direction is the one extensively treated in the present work and relate to the implementation of complementary communication standards, for example between wireless LAN standards and digital cellular telephony. The clear advantage of such reconfigurability option is the fulfillment of requirements such as superior data rates and high mobility in one single device even if such properties are not simultaneously present. This document discusses various solutions of bringing together the third generation mobile communication system UMTS and the wireless network standards like the IEEE 802.11a and the HIPERLAN/2, with the focus on RF front-end receiver for mobile terminals.

The goal of realizing such a reconfigurable RF front-end leads to the development of a new concept, which combines two different receiver architectures, like super-heterodyne and direct conversion, into the same hardware. The chosen solution is based on a careful analysis of different receiver architectures available today and their capability to suit the particularities of each of the implemented standards. However, this is a very complex task because the most important RF requirements like spurious rejection, gain, noise and linearity are very different between the standards. Moreover, in order to reduce power consumption and chip area of the front-end receiver, new state of the art functional blocks that are reconfigurable and/or reusable have been developed. These functional blocks need control and configuration signals in order to operate in accordance with the current standard. Furthermore, the reusable functional blocks must be able to fulfill the requirements of all standard they support. Therefore, a careful analysis of the system general requirements and the founded architecture selection significantly contributed to the success of the project.

Thesis Organization

The structure of the thesis follows the “general to particular” approach not only considering the content of each chapter but also in the organization of the subjects to be treated. Because the project, which forms the basis of the thesis, was focused on a practical outcome, it is more or less unavoidable that also this document will deal with practical aspects

of the design process. Nevertheless, there was a sustained effort to overcome this focus and to treat some of the subjects from a more theoretical point of view.

The first chapter of the thesis summarizes the process of design and characterization of a reconfigurable receiver front-end. This process was applied to a particular combination of wireless communication standards: the third generation Universal Mobile Telecommunication System UMTS, the American wireless LAN standard IEEE 802.11a and the European counterpart – HIPERLAN/2. Each of these standards is extensively analyzed and the most important characteristics concerning the receiver front-end are identified. Further on, the relevant front-end requirements like noise figure, intermodulation products and filter selectivity are derived for each particular standard based on their characteristics. An important part of the first chapter accounts for the selection process of the most suitable receiver architecture that would combine the standards nominated above. This part provides an overview on the most used receiver architectures today with their pros and cons and motivates the selection of that specific architecture to be implemented. The last part of the first chapter presents this particular solution and explains its functionality.

Once the reconfigurable receiver front-end architecture was chosen and specified, it is time to concentrate on specific functional blocks of this architecture. The focus moves in the second chapter from system design to functional block design. The functional block analysis is restricted in this thesis to the frequency conversion blocks. Given a specific technology (CMOS), an extended overview over the different mixer solutions is presented. The most suitable mixer solution for the present project was selected to be the resistive mixer.

The third chapter focuses on the development of the mixing blocks that fulfill the requirements of the reconfigurable front-end. The schematic and layout design process is described in depth and is followed by a complete measurement stage. In this way, the performance of both mixers present in the front-end is fully characterized, together with a detailed description of the measurement methods.

The forth chapter is the most theoretical one. The fact that the small signal distortion analysis of resistive mixers is relatively less approached in literature offered a new direction to research on. The chapter begins with a short introduction in the classical mixer large signal – small signal analysis. An extension to this theory through the Taylor series method was considered and mathematically grounded. Finally, dependencies between the intermodulation products and the setting parameters like gate and drain bias or LO signal amplitude were demonstrated.

The last chapter returns to the practical implementation of the reconfigurable receiver closing in this way the circle of theory and praxis. In order to demonstrate the applicability of the reconfiguration principle presented in this thesis, the key functional blocks of the receiver have been developed, implemented, and tested. The demonstrator board contains the RF mixer and both IQ demodulator mixers developed by the author together with the low noise amplifiers that were also developed for this project as monolithic circuits. The functionality of the receiver solution was demonstrated and a few measurements to characterize the non-idealities of the demonstrator circuit were realized.

The thesis concludes with a summarization of the present achievements and a presentation of the possible future developments on this subject.

Chapter 1.

Reconfigurable Receiver Architectures

1.1. General Considerations

The requirements of a new wireless communication standard resides from a unique set of objectives like desired data rate, signal coverage, receiver mobility or interoperability. Given these objectives and taking into account the limitations imposed by the transmission environment, the available power or the limited frequency bandwidth, the standard creators choose the appropriate signal processing methods that make the transmission possible. In the process of defining a communication standard, one has to counteract all spurious elements that can influence the quality of the transmission through proper measures like signal modulation, interleaving, forward error correction, multiplexing etc.

Generally, every signal-processing element has two constitutive parts, one at the transmitter and one at the receiver side. The frequency up-conversion is followed by frequency down-conversion, coding by decoding, interleaving by de-interleaving and so on. Concerning the implementation of these signal-processing methods, one can separate the processing chain into a digital and an analog part. Even if these two branches normally carry out separate tasks, sometimes the digital part can take over some of the analog tasks and vice-versa. Nowadays, the digital segment tends to conquer more and more terrain against the analog one, but there is a limit imposed by the carrier frequency of the modulated signal

that cannot be controlled by the digital processing technology available today. The separation between the two segments is made by the digital-to-analog converter on the transmitter side and the analog-to-digital converter at the receiver side. The communication nomenclature for the two processing blocks was defined as the *front-end* for the analog part and the *back-end* for the digital one.

The selection process of the desired receiver front-end architecture is particularly difficult. It implies the examination of all available architectures concerning their achievable performance given a specific system requirement. Important criteria for the selection of the most suited receiver front-end are not only the performance potential but also the production costs, integration capability or the consumed power. A zero-IF receiver front-end architecture needs far less functional blocks compared with the super-heterodyne solution, but lacks the selectivity performance of the last one. There is always a compromise between the functional performance and the "economical" parameters (cost, power, integration). Some of these performance drawbacks can be avoided with the present technology progress, fact that also make possible the actual trend towards the zero-IF architecture in all communication fields.

1.2. UMTS Standard Specifications

The Universal Mobile Telecommunication System (UMTS) was developed upon a request from the International Telecommunication Union (ITU) that created the International Mobile Telecommunications 2000 (IMT 2000) project to help the standardization of third generation (3G) mobile systems. UMTS was standardized in Europe by the European Telecommunication Standard Institute (ETSI) as the European contribution to the IMT 2000 standards. Along with UMTS, other standards were developed by countries like China, USA, Japan and South Korea.

The intention of ITU was to organize the implementation of a unique standard that would allow worldwide coverage with a single radio interface. That vision was not realizable for

3G systems due to political debates concerning the choice of the best standard implementation. Moreover, the frequency allocation in each of the important world regions was different, requiring appropriate signal modulation techniques and frequency band handling strategies. Anyway, the vast majority of the submitted proposals were based on the W-CDMA (Wideband Code Division Multiple Access) technique. This technique improves the tolerance of the system against interferences and noise of both the air channel and the front-end circuitry.

The key factors and main objectives of IMT 2000 for the 3G systems can be summarized as follows [1]:

- Minimum 144 kbps (preferably 384 kbps) in all radio environments (full coverage and high mobility), up to 2 Mbps in low-mobility and indoor environments.
- Support of symmetrical and asymmetrical traffic, high capacity and spectrum efficiency.
- Packet switched communication must be provided in addition to a circuit switched mode.
- Multimedia service capability and voice quality comparable to wire-line quality.
- World-wide coverage and roaming including a satellite component.
- High flexibility, beginning with the evolution from 2G systems and to future developments. Applications independent on the underlying support layers.

The UMTS standard was submitted and accepted by ITU in 1998 under the name UTRA (UMTS Terrestrial Radio Access) and belongs along with other nine Radio Transmission Technology (RTT) standards to the IMT 2000 project.

ETSI has integrated under the name UTRA two different types of UMTS standards. The first one, closer to the practical implementation on the market is based on the Frequency Division Duplex (FDD) technique. It ensures optimal conditions for voice transfer and

other symmetrical traffic communication. The frequency band allocation of the UTRA FDD depicted in Figure 1.1 shows two different bands for up-link and down-link respectively. The UTRA TDD standard is based on the Time Division Duplex technique and is very well suited for asymmetrical communication. Even if there are also two communication bands as shown in Figure 1.1, there is no frequency separation between the up-link (UL) and down-link (DL) both directions existing simultaneously in one band. The other two bands depicted in Figure 1.1 represent the Mobile Satellite Service bands and does not make the object of UTRA standards but are important for their definition and parameter specifications.

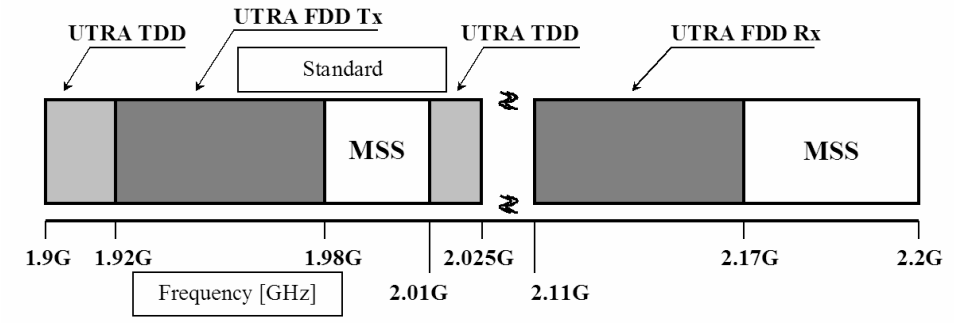


Figure 1.1. IMT 2000 frequency band allocation in Europe

Both TDD and FDD UTRA standards share the same upper layers, only the physical layer is different from one standard to the other. This fact ensures optimum service for all environments, from high mobility in macro-cells to low mobility in pico-cells in out- and indoor scenarios.

The description of the UMTS standard will further be restricted to the characteristics of the physical layer that is the only relevant layer concerning front-end receiver specification. Furthermore, only the FDD option of the UTRA is analyzed in the design process of the reconfigurable receiver architecture. The TDD standard is the subject of another type of receiver architecture, where the antenna duplexer is replaced with a switch, which will not be covered in this work. The third limitation is the consideration of only the user equip-

ment (shortly UE in UTRA terminology) receiver specifications in this work that is enough for the design and implementation of the front-end receiver.

The RF characteristics and test cases to be fulfilled by the UE are defined in [2]. In general, the transmitter and receiver characteristics are specified at the antenna connectors of the UE and base station (BS or node B specifically named). The allowed test tolerances are defined in [3].

1.2.1. Characteristics of the standard

The transmission of information is organized in logical data flows. Depending on the nature of information and their destination, these streams (known as logical channels) are packed in different physical bit streams (or physical channels). In UMTS, two main physical channels are defined, the dedicated physical data channel DPDCH and the dedicated physical control channel DPCCH. The term “dedicated” refers to the fact that the channel is not shared between several terminals but is transmitted from UE to BS or vice versa. The transmission from BS to the UE is labeled as down-link (DL) transmission and the transmission from UE to BS is known as up-link (UL). For the present work, only the DL transmission and the corresponding DL-DPDCH and DL-DPCCH are of interest.

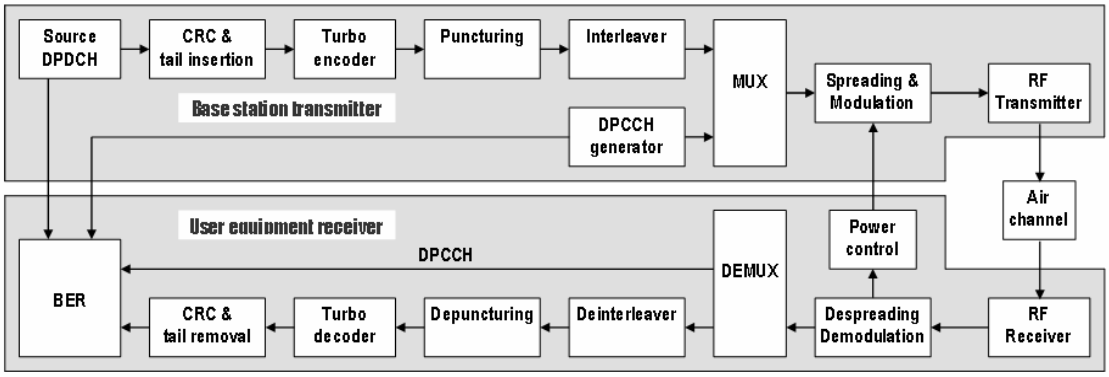


Figure 1.2. UMTS transmission chain – test-case implementation

The Figure 1.2 depicts the UMTS down-link transmission chain. In this implementation example, the transmission integrity deteriorated by the front-end non-idealities and the air channel is tested by means of the bit error rate BER.

The DL-DPDCH is prepared for the transmission being packed with different correction and protection codes and then time-multiplexed with the DL-DPCCH. The obtained data flow is then spread by multiplication with a special orthogonal code of constant rate. The term “spreading” refers to the frequency domain representation of the signal, whose fre-

quency band is widened proportionally with the increase in its data rate. The data rate increase , also known as spreading factor SF, varies from 4 for a high data rate channel (video channel for example) up to 512 for a lower data rate channel. The constant code rate or chip rate as it is named in the UMTS standard is set to 3.84 Mcps, which will create a RF signal bandwidth of approx. 3.84 MHz. The advantage of the orthogonal spreading codes is given by the possibility to recover integrally the data after it was impaired by other similar channels, transmitted on the same frequency.

The digital processing methods applied to the UMTS signal will not make further the object of this work. The precedent paragraphs have only justified some of the characteristics of the RF signal and briefly illustrated the complexity of the transmission chain.

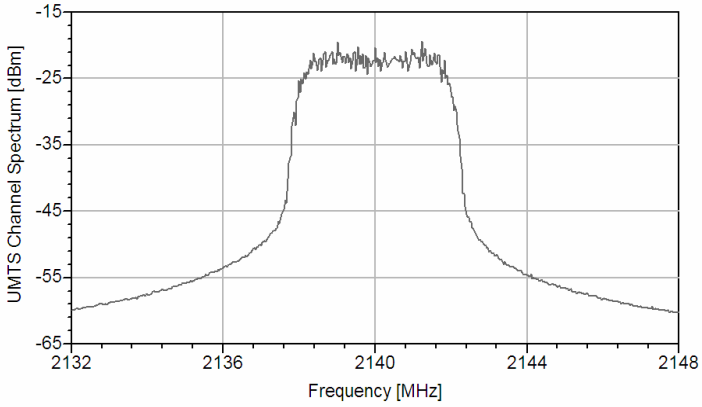


Figure 1.3. UMTS channel frequency spectrum as depicted by the spectrum analyzer during measurements

The UTRA FDD communication between the base station and the UE takes place in paired frequency bands. In Europe these bands are:

- 1920 – 1980 MHz for the UL and
- 2110 – 2170 MHz for the DL

With UTRA FDD, both fixed and variable duplex distances are possible. The fixed duplex distance is 190 MHz and the variable duplex distance can vary between 134.8 MHz and 245.2 MHz [2].

The nominal channel spacing is 5 MHz but this can be adjusted to for a particular deployment scenario. The channel carrier frequency raster is 200 KHz, which means that the center frequency must be an integer multiple of 200 KHz. The actual UMTS channel occupies only 3.84 MHz as depicted in Figure 1.3, which allows a guard interval between two channels of about 1.16 MHz.

1.2.2. UMTS Receiver Requirements

The UMTS receiver requirements defined in [2] are mainly based on experimental tests. The results of these tests are expressed as bit error rates (BER) achieved under specific conditions. The requirements state that a similar BER should be achievable under the same or worse conditions as the ones defined in the document. These conditions mean an extremely low or an extremely high signal level, a large adjacent channel or an in-band or out of band interferer. Based on these requirements, one can derive a new set of performance parameters like noise figure, linearity or intermodulation intercept points that characterize the receiver front-end. The most suitable receiver architecture that promises to fulfill the requirements can be designed starting with these parameters. Following, the extraction of the main performance parameters from the UMTS receiver requirements will be described.

Noise Figure

The reference sensitivity level minimum requirement defined in [2] states that a BER<10^{-3} must be achieved during simultaneous operation of several UE transmitters at maximum output power. The characteristics of the received signal for the sensitivity level test-case are defined in Table 1.1.

The power levels are defined for a measurement interval of 3.84 MHz. P_{ME} is the received power spectral density of the DL as measured at the UE antenna connector and E_c is the average energy per chip of the Dedicated Physical Channel DPCH.

E_c	-117 dBm/3.84 MHz
P_{ME}	-106.7 dBm/3.84 MHz

Table 1.1. Test parameters for reference sensitivity level test-case

The required noise figure NF of the whole receiver can be computed according to [1]:

$$NF = E_c + G_p + G_c - \left(\frac{E_b}{N_t}\right)_{eff} - P_N, \qquad 1.1$$

Where: NF – receiver noise figure,
E_c – average energy per bit of the DPCH,
G_p – processing gain through de-spreading of the received signal
G_c – coding gain through baseband processing
E_b/N_t – ratio of energy per bit to the total effective noise,
P_N – thermal noise power in the 3.84 MHz channel bandwidth

The thermal power noise level is calculated with the formula:

$$P_N = 10\log(kTB) = -108\,\text{dBm}, \qquad 1.2$$

Where: k – Boltzmann constant k=1.38·10^{-23} W/KHz,
T – noise temperature T=300 K,
B – UMTS channel bandwidth B=3.84 MHz

If an implementation loss in the baseband of 1 - 2 dB is considered, an effective value of E_b/N_t=7.2 dB can be adopted. For a spreading factor (SF) of 128 as defined in the sensitivity level test-case it will result a processing gain of:

$$G_p = 10\log(128) = 21\,\text{dB}, \tag{1.3}$$

The estimation of the gain due to convolutional coding is relatively complex. A value for G_c of 4 dB is rather conservative and was also assumed in [1]. Now that all values in Equation 1.3 are defined, one can calculate the *NF* of the whole system:

$$NF = -117\,\text{dBm} + 108\,\text{dBm} + 21\,\text{dB} + 4\,\text{dB} - 7.2\,\text{dB} = 8.8\,\text{dB}, \tag{1.4}$$

In [4], a value of 9 dB was assumed for the noise figure of the whole system, fact that also validates the above estimate.

1 dB Compression Point

The high peak to average power ratio (PAR) of the UMTS signal has a great influence on the linearity requirements of the receiver front-end [5]. In the case of ten or more users that share the same channel, the PAR can be above 12 dB. High linearity requirements for the receiver front-end cause high current consumption of the circuits comprising the receiver.

The 1 dB compression point (P1dBCP) requirement of the UMTS receiver states how close a multi-user W-CDMA signal strength may approach this point causing only modest degradations of the BER. The characteristics of the received signal for the maximum input level test-case are defined in Table 1.2:

The E_c/P_{BS} represents the average energy per chip of the user channel (DPCH) reported to the total power spectral density measured at the base-station antenna connector. Only the interferences introduced by the orthogonal channels of other users are taken into account in this ratio. The thermal noise added in the air link between the base station and the mobile equipment is ignored because of the high level of the input signal. This difference of 19 dB between the user channel energy and the total signal power is much larger than the value of 10.3 dB defined in [3] for all other test-cases. This difference comes from additional user channels coded in the same signal-band by the base-station. These channels are orthogonal to the DPCH channel, which leads to a special type of influence that is different from the influence of an AWGN (Average Gaussian Noise) source. In UMTS simulations, this type of interference is modeled with an OCNS (Orthogonal Channel Noise Simulator) signal. This interference signal consists of 16 dedicated data channels uncorrelated to each other and coded with orthogonal spreading codes.

E_c/P_{BS}	-19 dB
P_{ME}	-25 dBm/3.84 MHz

Table 1.2. Test parameters for maximum input level test-case

The BER dependency on the receiver P1dBCP can be simulated by using a parametrical amplifier with variable linearity and the UMTS source described above. Such simulations [1] show a sharp drop of the coded BER for a P1dBCP between –25 dBm and –15 dBm. For an UMTS signal modeled as one DPCH channel impaired by RRC filtered Gaussian noise, the dependency is not as strong as for OCNS. Both dependencies are depicted in Figure 1.4.

According to these results, we can conclude that the P1dBCP of the receiver should be 10 dB higher than the maximum input signal level to prevent any degradation of the BER due to the nonlinearity effects in the receiver front-end. That gives a value of –15 dBm for the P1dBCP parameter.

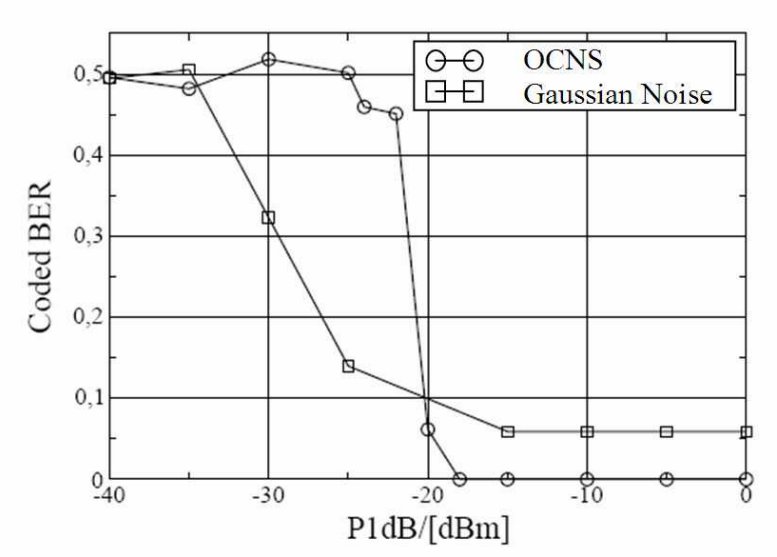


Figure 1.4. Coded BER versus P1dBCP for OCNS and for RRC filtered Gaussian noise interference

Several effects in the UMTS receiver degrade the orthogonality between different user channels and introduce in-band distortions of the signal. A major source of such in-band distortions is the channel selection filter at the baseband or at the IF in the case of heterodyne receiver. The distortions are caused by amplitude and phase nonlinearity in the filter and can be visualized as dependency between the BER and the peak-to-peak amplitude ripple in a Chebyshev band pass filter [1]. Ripple amplitudes of up to 1.1 dB will introduce no critical BER degradation, but higher values should be avoided.

Channel Filter Selectivity

The selection of the wanted channel from the received frequency band includes filtering at the intermediate frequency (IF), analog baseband and digital baseband. The selectivity requirements are defined in the adjacent channel selectivity test case specified in [2] and represented in Table 1.3:

P_{ch} is the interference signal at frequencies situated at 5 MHz offset on both sides of the received channel. This modulated signal consists of common channels needed for tests and 16 dedicated data channels. For the specified strength of this interference signal, the BER of the received data channel should not be above 0.001.

E_c	-103 dBm/3.84 MHz
P_{ME}	-92.7 dBm/3.84 MHz
P_{ch}	-52 dBm/3.84 MHz at ±5 MHz offset

Table 1.3. Test parameters for adjacent channel selectivity test-case

Since the level of *Ec* is 14 dB above the sensitivity limit, the noise is of minor importance. From this test-case, the selectivity of the receiver filter can be derived such the signal to interference ratio E_b/N_t be large enough also for the adjacent channel. The acceptable interference level N_t, is determined with the formula:

$$N_t = E_c + G_p + G_c - \left(\frac{E_b}{N_t}\right)_{eff}, \qquad 1.5$$

Where: E_c – average energy per bit of the DPCH,
G_p – processing gain by dispreading the received signal,
G_c – coding gain by signal decoding in the baseband,
E_b/N_t – ratio of energy per bit to the total effective noise.

If we consider the adjacent channel signal as AWGN noise, we can accept an effective E_b/N_t level of 7.2 dB as considered for the noise figure calculation. Under this condition:

$$N_t = -103\,\text{dBm} + 21\,\text{dB} + 4\,\text{dB} - 7.2\,\text{dB} = -85.2\,\text{dBm}, \qquad 1.6$$

The condition defined in the adjacent channel selectivity test case of a BER<0.001 can surely be satisfied if the selectivity of the channel filter will attenuate the power level of the adjacent channel at this interference noise level defined in Equation 1.7. The adjacent channel selectivity will then be:

$$Att_{5MHz} = P_{ch} - N_t = -52\,\text{dBm} + 85.2\,\text{dBm} = 33.2\,\text{dBm}, \qquad 1.7$$

Where: $Att_{5\,MHz}$ – adjacent channel attenuation for a BER<10^{-3}.

Second Order Intercept Point

Signals with time varying envelopes like the W-CDMA signals create critical second-order distortions of the baseband signal. Second-order nonlinearities in the receiver processing chain produce a spurious baseband signal proportional to the squared envelope of the signal. From the multitude of signals that can create such distortions, the in-band neighbor channels and the transmission leakage are the most important. The problem of the unwanted neighbor channels in the receive band is defined in the in-band blocking characteristics test-case of [2] whose parameters are depicted in Table 1.4.

E_c	-114 dBm/3.84 MHz
P_{ME}	-103.7 dBm/3.84 MHz
P_{block}	-44 dBm/3.84 MHz at ±15 MHz offset

Table 1.4. Test parameters for in-band blocking characteristics test-case

The generation mechanism of second order distortions stemming from a neighbor channel under the conditions defined in the in-band blocking characteristics (Table 1.4) is depicted in Figure 1.5.

After down-conversion of the RF signal together with the in-band neighbor channel, a significant DC component is present in the baseband signal. This DC component resides from the squared function of the second-order distortion and represents around 50% from the entire energy of the in-band neighbor channel. The same in-band channel will also produce a component that lands over the baseband signal that is broader than the sideband of the user channel. The third spurious component, at 15 MHz, is the down-converted in-band channel. The last two spurious signals equally share the rest of 50% from the in-band channel energy.

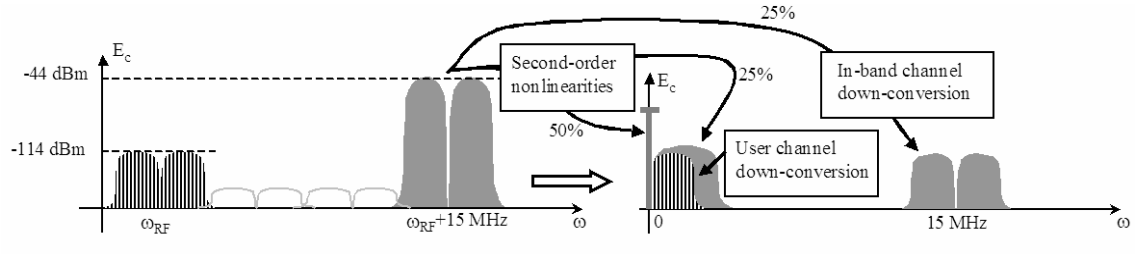


Figure 1.5. In-band blocking spectral representation with second order nonlinearity effects

Returning to the in-band blocking test-case, the input referred second-order intercept point of the receiver can be determined from the condition of BER<10^{-3}, under the conditions defined in Table 1.4. This condition can again be translated in the power ratio E_b/N_t as defined in the noise figure paragraph. Defining this condition for the present test-case results:

$$N_t = E_c + G_p + G_c - \left(\frac{E_b}{N_t}\right)_{eff} = -114 + 25 - 7.2 = -96.2\,\text{dBm}, \qquad 1.8$$

Where: N_t – total noise and interference power spectral density,

E_c – average energy per bit of the DPCH,

G_p – processing gain by dispreading the received signal,

G_c – coding gain by signal decoding in the baseband,

E_b/N_t – ratio of energy per bit to the total effective noise.

A maximal noise and interference power spectral density of -96.2 dBm can be present at the receiver antenna that will not distort the wanted channel. The interference in this test-case comprises only the second-order distortions of the in-band channel together with its down-converted part and the DC component. Since the power of the desired signal (-114 dBm/3.84 MHz) in this test is 3 dB higher than for the sensitivity test (-117 dBm/3.84 MHz), it is assumed that noise constitutes 50% of the total disturbing power [6]. It results then:

$$N_t = P_N + P_I , \tag{1.9}$$

$$P_N = P_I = N_t - 3\,\mathrm{dB} = -99.2\,\mathrm{dBm} , \text{ and} \tag{1.10}$$

$$P_I = P_{DC} + P_{SOD} + P_{BLeak} , \tag{1.11}$$

Where:
- N_t – total noise and interference power spectral density,
- P_N – noise power spectral density in dBm/3.84 MHz,
- P_I – interference power spectral density in dBm/3.84 MHz,
- P_{DC} – DC power level in dBm,
- P_{SOD} – second order distortion power spectral density of the in-band channel in dBm over the expanded frequency range,
- P_{BLeak} – power spectral density of the down-converted in-band channel in dBm/3.84 MHz.

A combination of high pass and low pass filtering in the baseband can suppress the DC component together with the in-band leakage but can not eliminate the second order distortion that falls on the user signal. Therefore, the entire interference power level is given by the second order interference distortion:

$$P_I = P_{SOD} = -99.2\,\text{dBm}\,, \tag{1.12}$$

Knowing the input level of the in-band interferer, and the acceptable level of distortion it can cause, the input second order intercept point of the receiver can be simply derived. It is presumed that the receiver has no system gain.

$$IIP2_{15} \geq 2P_{block} - P_{SOD} \geq -88\,\text{dBm} + 99.2\,\text{dBm} \geq 11.2\,\text{dBm}\,, \tag{1.13}$$

Where: $IIP2_{15}$ – second order intercept point, input referred, in dBm,
P_{Block} – in-band channel power spectral density in dBm/3.84 MHz,
P_{SOD} – second order distortion power spectral density of the in-band channel in dBm over the expanded frequency range,

The worst-case scenario of the second-order distortion is determined by the transmitter leakage level at the receiver input. The disturbance mechanisms are the same as those shown previously but the in-band signal is replaced by the transmitter leakage signal. Since the duplex distance can vary between 134.8 MHz and 245.2 MHz, the direct transmitter leakage through the receiver to the demodulator can be rejected very efficiently and its influence is insignificant.

Since the transmitter signal is always present, the second-order products should be sufficiently suppressed, even 10 dB under the acceptable noise level. A rough estimate of IIP2 is then determined by:

$$IIP2_{Tx} \geq 2P_{TxLeak} - (P_{SOD} - 10\,\text{dB})\,, \tag{1.14}$$

Where: $IIP2_{Tx}$ – second order intercept point determined by the leakage of the transmitter signal through the receiver, input referred, in dBm,

P_{TxLeak} – power spectral density level of the transmitter leakage as defined in the out of band blocking test case for Band 2 in dBm/3.84 MHz,

P_{SOD} – second order distortion power spectral density of the in-band channel in dBm over the expanded frequency range,

For a power level of –30 dBm of the P_{TxLeak} as defined in the out of band blocking characteristics test case [2], we will obtain:

$$IIP2_{TxLeak} \geq 2(-30)\,\text{dBm} - (-99.2 - 10)\,\text{dBm} \geq 49.2\,\text{dBm}, \quad 1.15$$

Third-Order Intercept Point

The third-order intercept point requirement can be derived from the intermodulation test case defined in [2]. The intermodulation test parameters are listed in: Table 1.5

P_{CW} is the power level of a continuous wave (CW) interferer at 10 MHz offset from the user channel carrier frequency and P_{mod} is the power spectral density of a modulated channel that contains 16 user dedicated physical channels and the usual common physical channels, all spread with different codes, at 20 MHz offset from the user channel carrier frequency.

E_c	-114 dBm/3.84 MHz
P_{ME}	-103.7 dBm/3.84 MHz
P_{CW}	-46 dBm at ±10 MHz offset
P_{mod}	-46 dBm/3.84 MHz at ±20 MHz offset

Table 1.5. Test parameters for the intermodulation characteristics test-case

As depicted in Figure 1.6, the interferers showed in the left side of the figure will generate third order intermodulation products at the following frequencies:

$$f_{IP3}^{1} = 2(f_{RF} + 20\,\text{MHz}) - (f_{RF} + 10\,\text{MHz}) - f_{LO} \approx 30\,\text{MHz}\,, \text{ and} \qquad 1.16$$

$$f_{IP3}^{2} = 2(f_{RF} + 10\,\text{MHz}) - (f_{RF} + 20\,\text{MHz}) - f_{LO} \approx 0\,\text{MHz}\,, \qquad 1.17$$

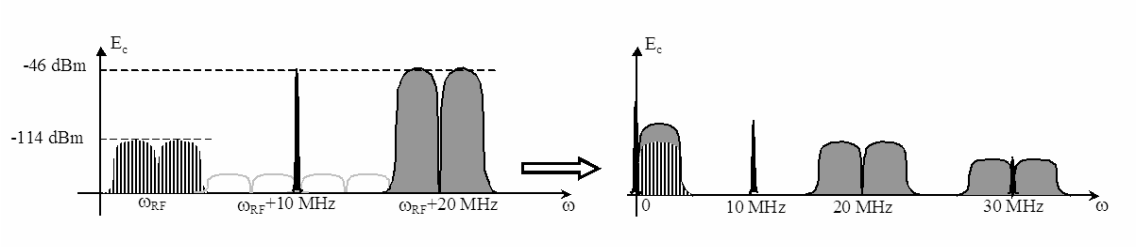


Figure 1.6. Intermodulation test-case spectral representation with third order nonlinearity effects

Together with the intermodulation products described above, there will be also some leakage signals around 20 MHz and 10 MHz respectively.

The acceptable noise and interference level for which the BER<10^{-3} condition is fulfilled can be derived in the same manner as for the noise figure test-case:

$$N_t = E_c + G_p + G_c - \left(\frac{E_b}{N_t}\right)_{eff} = -114 + 25 - 7.2 = -96.2\,\text{dBm}\,, \qquad 1.18$$

Where: N_t – total noise and interference power spectral density,
E_c – average energy per bit of the DPCH,
G_p – processing gain by dispreading the received signal,
G_c – coding gain by signal decoding in the baseband,
E_b/N_t – ratio of energy per bit to the total effective noise.

As the desired signal is close to the minimum sensitivity level, both noise and interference must be taken into account. The assumed power distribution is then [6]:

- noise, 50% of power, -3 dB
- intermodulation, 15% of power, -8 dB
- CW interferer's blocking effect, 15% of power, -8 dB
- modulated interferer's blocking effect, 15% of power, -8 dB
- oscillator noise, 5% of power, -13 dB
- second order distortion products will be neglected

Regarding the interference level produced by the third order intermodulation distortion P_{TOD}, it will be then 8 dB lower than the minimum acceptable noise and interference level conducting to a minimum receiver *IIP3*:

$$IIP3 \geq P_{\text{mod}} + \frac{1}{2}\left(P_{\text{mod}} - \left(N_t - 8\,\text{dB}\right)\right) = -16.9\,\text{dBm}, \qquad 1.19$$

Where: N_t – total noise and interference power spectral density,

P_{mod} – power spectral density of a modulated channel that contains 16 user dedicated physical channels and the usual common physical channels, all spread with different codes, at 20 MHz offset from the user channel carrier frequency.

Conclusion

The precedent considerations focus on the UMTS receiver front-end characteristics, which establish the achievable performance given the conditions defined in the test-cases defined in [2]. These characteristics are: the noise figure, 1 dB compression point, channel filter selectivity, second and third order intercept points as enumerated in the Table 1.6. All these characteristics describe the receiver front-end as one entity, independently on the

chosen architecture. In the practical case, when the receiver architecture is established, these characteristics can be distributed to the different functional blocks.

The test-cases that lead to the founding of system characteristics represent worst case scenarios in the functionality of the receiver like a very weak or a very strong input signal, a strong adjacent channel or a strong interferer. Therefore, the defined characteristics must hold for these particular situations. In the same time, the total amplification of the front-end must be adapted to the strength of the input signal in order to have a relatively constant power level at the analog-to-digital converter (ADC). Therefore, the distribution of the noise figure, amplification or intermodulation performance over the front-end is dependent on the input signal characteristics..

Noise Figure	*NF*	8.8 dB
1 dB Compression Point	*P1dBCP*	-15 dBm
Adjacent Channel Selection	Att_{5MHz}	33.2 dBm
Input Referred Second Order Intercept Point	*IIP2*	49.2 dBm
Input Referred Third Order Intercept Point	*IIP3*	-16.8 dBm

Table 1.6. UMTS receiver system characteristics

1.3. WLAN Standards Specifications

A Wireless Local Area Network (WLAN) is a data transmission system designed to provide location-independent network access to or between computing devices by using radio waves rather than a cable infrastructure. WLAN standards are intended for high data rates, and support architectures with an infrastructure as well as “ad-hoc” architectures, whereby terminals communicate directly with each other without the mediation of a fixed base station. With their relatively low infrastructure costs, compared to cellular or point-to-multipoint distribution systems, the WLAN networks provide a good fit for the usage model aimed at high-bandwidth consumers. They can be easily adapted for business or residential use, and for low-mobility environments like airports, hotels and other locations where there exists a need for broadband Internet access.

Standards are being developed for wireless LANs, under different standardization bodies on the European, Asian and the American continent. In USA, the Institute of Electrical and Electronics Engineers (IEEE) droved the development of multiple WLAN technologies and standards under the generic name IEEE 802.11. After the definition of the IEEE 802 WLAN standard in 1997, the IEEE issued two of its most successful supplements in 1999: IEEE 802.11a and IEEE 802.11b. The specifications of IEEE 802.11 [7] define two layers: layer one, called Physical Layer (PHY) and layer two, called Media Access Control (MAC) layer. The first layer specifies the modulation scheme and signaling characteristics for the transmission through the air channel, whereas the second layer defines a way to access the physical layer. The specifications of the IEEE 802.11 MAC layer [8], define also services related to the radio resource and the mobility management. Both 802.11a and 802.11b standards use the MAC layer already specified for the Industrial Scientific Medical (ISM) band. The IEEE 802.11b supports data rates up to 11 Mbit/s and operates in the 2.4 GHz band(ISM) which provides only 83 MHz of spectrum to accommodate a variety of other radiating products, including cordless phones and microwave ovens. The susceptibility to interferences of the 802.11b standard makes the 802.11a alternative more attrac-

tive for the multi-standard implementation, and therefore will not be further regarded in this work. On the other side, the IEEE 802.11a standard development, even if much slowly due to its complexity, proved to offer some advantages like its intrinsic ability to handle delay spread or multi-path reflection effects which qualify it for mobile multi-standard receivers. The standard uses 300 MHz of bandwidth in the 5 GHz Unlicensed National Information Infrastructure (UNII) band [9].

In Europe, the Broadband Radio Access Networks (BRAN) project of the European Telecommunications Standards Institute (ETSI) has defined the *High Performance Radio Local-Area Network, type 2* shortly named HIPERLAN/2 [10], [11]. The standard specifies a radio-access network that can be used with a variety of core networks. The access is provided by several convergence layers defined in this scope, which links the HIPERLAN/2 standard with the following services [12]:

- Internet Protocol (IP) networks (Ethernet and Point to Point Protocol, PPP),
- Asynchronous Transfer Mode (ATM) based networks,
- third-generation core networks and
- networks that use IEEE 1394 (Fireware) protocols and applications.

The HIPERLAN/2 standard provides a flexible architecture that besides the convergence layers enumerated above defines network independent physical (PHY) [13] and data-link-control (DLC) layers. The data units that are transmitted within the core networks can differ in length, type and content. A specific convergence layer in HIPERLAN/2 segments the data units into fixed-length DLC User Service Data Units (U-SDU). These units are then transmitted to their destination by means of DLC and PHY data transport services. The HIPERLAN/2 standard supports terminal mobility of up to 10 m/s and bit rates of up to 54 Mbit/s.

In Japan, a system that is very similar to HIPERLAN/2 has also been specified by the Multimedia Mobile Access Communication (MMAC) association within the Association of Radio Industries and Broadcasting (ARIB) [9]. The main difference between it and

HIPERLAN/2 is that the spectrum-sharing rule of the Japanese system introduces a carrier-sensing mechanism.

Close cooperation between ETSI BRAN, ARIB MMAC and IEEE 802.11 has ensured that the PHY layers of the various 5 GHz WLAN standards are broadly harmonized. The main differences between the IEEE 802.11a and HIPERLAN/2 standards occur at the MAC layer [14], [15]. In HIPERLAN/2, the medium access is based on a Time Domain Multiple Access/ Time Domain Duplex (TDMA/TDD) approach using a fixed length MAC frame with a period of 2 ms [10]. This frame comprises uplink (mobile terminal, MT to access point, AP), downlink (AP to MT) and direct link (between two MT in ad-hoc networks) segments. The communication is always controlled by an AP or and central controller CC for ad-hoc networks, that schedules the length of each communication segment in the MAC frame. IEEE 802.11a uses a variable length MAC frame based on a carrier sense multiple access with collision avoidance (CSMA/CA) protocol, [9], [10]. The MT must sense the radio channel before transmitting. If the channel is free, transmission begins; otherwise, an exponential back-off period is implemented before the channel is sensed once more. The use of distributed MAC makes IEEE 802.11a more suitable for ad-hoc networks and non-real-time applications, whereas the HIPERLAN/2 MAC is designed to provide quality of service support for multimedia and real-time applications.

1.3.1. WLAN Physical Layer Characteristics

As stated before, both European and American WLAN standards occupy the frequency band between 5 and 6 GHz. The exact spectrum allocation is depicted in Figure 1.7. A first segment of 150 MHz between [5.15 – 5.35] GHz is used by both standards. In the superior frequency domain, the HIPERLAN/2 takes the frequency band between [5.47 – 5.725] GHz and the IEEE 802.11a the band between [5.725 – 5.825] GHz.

The standards developed by both IEEE 802.11 and ETSI/BRAN bodies for the 5.2 GHz band uses the Orthogonal Frequency Division Multiplexing (OFDM) modulation for their physical layer. OFDM has been designed to utilize the frequency spectrum more efficiently

than spread spectrum techniques. In both standards, 48 active sub-carriers plus 4 sub-carriers for pilot symbols are used, along with a 64-point FFT.

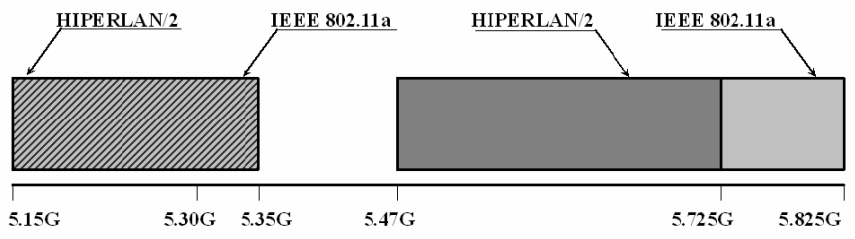


Figure 1.7. WLAN frequency band allocation in Europe and USA

Since, both standardization bodies have worked together in order to harmonize the physical layer of these two standards, the main differences between these two standards are in the MAC and DLC layers. However, there are some relatively minor differences between IEEE 802.11a and HIPERLAN/2 standards also concerning their physical layer. As shown in Table 1.7, each standard uses different modulation schemes and coding rates. More specifically the differences exist in the cases of 16-QAM (Quadrature Amplitude Modulation) and 64-QAM schemes. HIPERLAN/2 supports seven modes, while IEEE 802.11a supports eight modes.

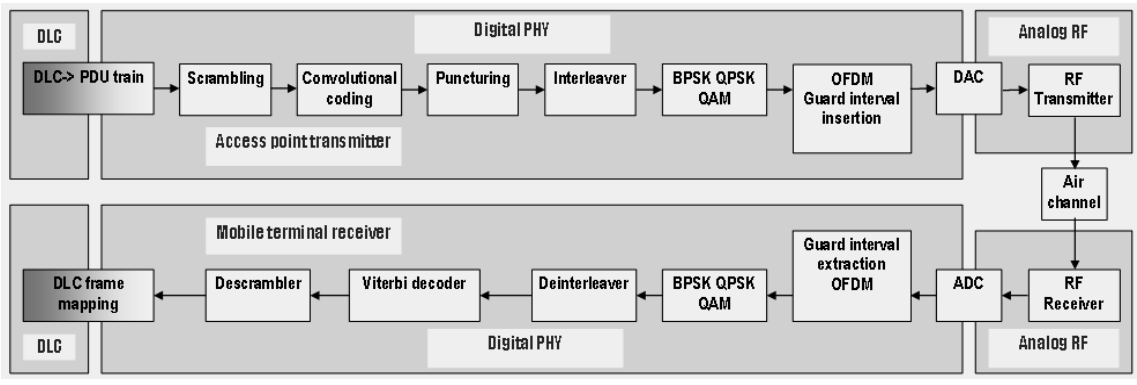


Figure 1.8. WLAN frequency band allocation in Europe and USA

Figure 1.8 shows the reference configuration of the transmission chain common to the both IEEE 802.11a and HIPERLAN/2 standards. Data for the transmission is supplied to the PHY layer in form of an input Packet Data Unit (PDU) frame.

Standard Im-plement	Modulation scheme	Coding rate	Physical data Rate [Mbps]	Data bits per symbol[Mbps]
Both standards	BPSK	1/2	6	24
	BPSK	3/4	9	36
	QPSK	1/2	12	48
	QPSK	3/4	18	72
IEEE802.11a	16-QAM	1/2	24	96
HIPERLAN/2	16-QAM	9/16	27	108
Both standards	16-QAM	3/4	36	144
IEEE802.11a	64-QAM	2/3	48	192
Both standards	64-QAM	3/4	54	216

Table 1.7. Modulation schemes for HIPERLAN/2 and IEEE 802.11a

The PDU train is input to a scrambler to avoid long trains of zeros or ones in the input data. The data is subsequent coded and punctured to obtain a constant data rate and finally interleaved in order to hinder error bursts from being input to the convolutional decoding process in the receiver. The interleaved data is then mapped to data symbols according to BPSK, QPSK, 16-QAM or 64-QAM constellation. OFDM modulation is implemented by means of an inverse fast Fourier transformation (FFT). In order to prevent inter-symbol interference (ISI) and inter-carrier interference (ICI) due to the delay spread, a guard interval is implemented after the OFDM modulation by a periodic extension of the symbol itself. This guard interval must be eliminated at the reception before OFDM demodulation. The signal obtained after OFDM modulation and digital to analog conversion occupies a band of 16.6 MHz. The RF transmitter prepares the analog converted signal for wireless transmission by frequency translation, filtering and amplification. The frequency spectrum of the signal that contains 48 data carriers and 4 pilot carriers is shown in Figure 1.9. The

transmission channels are spaced 20 MHz apart and the carrier frequencies are defined at integral multiples of 5 MHz above 5 GHz.

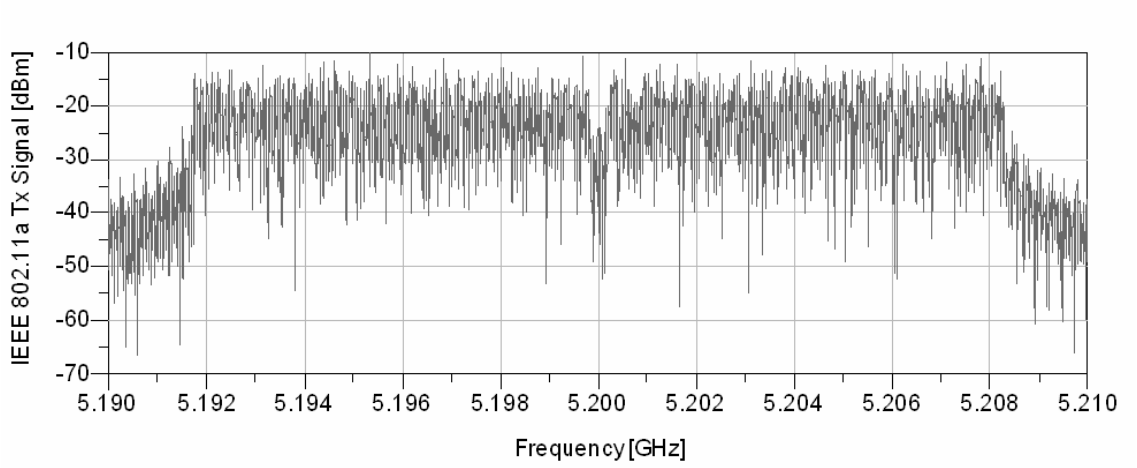


Figure 1.9. WLAN channel frequency spectrum as observed on a spectrum analyzer

As in the UMTS requirements case, there is a set of receiver system test-cases for each of the WLAN standards that can make the system design of the receiver front-end much easier. These test-cases refer mainly to the receiver sensitivity, maximum input level and adjacent and non-adjacent channel selectivity.

1.3.2. WLAN Receiver Requirements

Noise Figure

The total noise figure of the WLAN receiver front-end can be derived from the sensitivity test cases defined in [7] and [11] for IEEE 802.11a and HIPERLAN /2 respectively.

In both test-cases a Packet Error Rate (PER) of less then 10% is required at a PDU length of 1000 bytes for input power levels at the antenna connectors as defined in the Table 1.8 below.

Data Rate (Mbps)	Minimum Sensitivity (dBm)	
	IEEE 802.11a	HIPERLAN/2
6	-82	-85
9	-81	-83
12	-79	-81
18	-77	-79
24	-74	
27		-75
36	-70	-73
48	-66	
54	-65	-68

Table 1.8. Receiver sensitivity requirements for IEEE 802.11a and HIPERLAN/2

The required system noise figure can be derived from an equivalent formulation of the Equation 1.1 used for the UMTS standard:

$$NF = P_{\min} - P_N - C/I\,, \tag{1.20}$$

Where: NF – noise figure of the whole receiver,

P_{min} – sensitivity at the receiver antenna as defined in Table 1.8,

P_N – thermal noise power in the 16.6 MHz bandwidth,

C/I – carrier to interference ratio, equivalent here with the signal to noise ratio (SNR), for which the PER degradation is les then 10%.

The thermal noise power level for the WLAN channel is again calculated as:

$$P_N = 10\log(kTB) = -101.6\,\text{dBm}\,, \tag{1.21}$$

Where: k – Boltzmann constant k=1.38·10^{-23} W/KHz,

T – noise temperature T=300 K,

B – UMTS channel bandwidth B=16.6 MHz

An evaluation of the baseband processing chain capability to reconstruct the original signal from the received one in the presence of a Gaussian noise channel is represented in Figure 1.10. It was observed in [15] that both IEEE802.11a and HIPERLAN/2 standards exhibit the same PER performance due to their similar PHY layers.

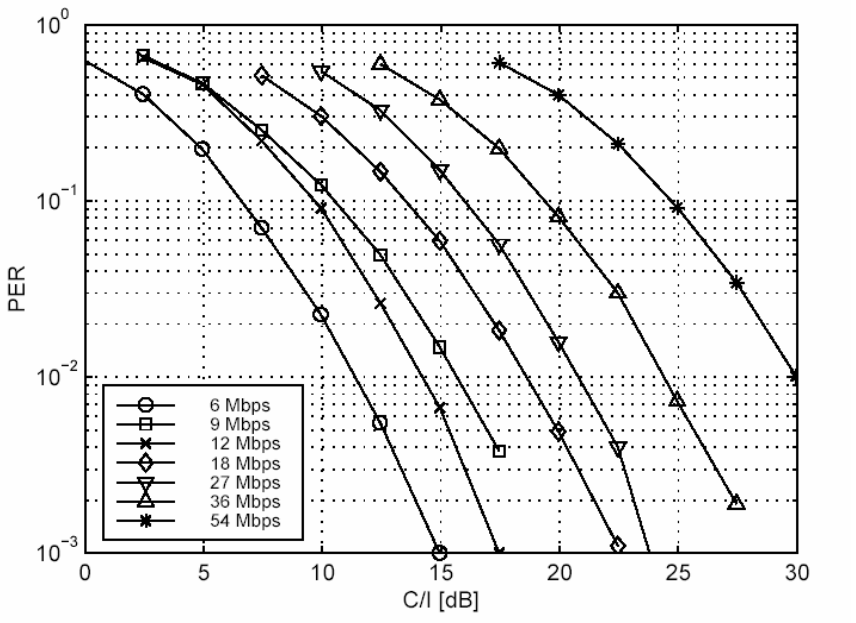


Figure 1.10. Dependence of the Packet Error Rate (PER) to the Carrier to Interference (C/I) for different data rates and modulation types in a WLAN channel

The required point of operation as defined in Table 1.8 is a PER of 10% that implies a C/I between 7 and 25 dB depending on the modulation type. The system noise figure can now be calculated for each transmission mode as depicted in the next examples below.

$$NF_{6Mbps} = -85\,\text{dBm} + 101.6\,\text{dBm} - 7\,\text{dB} = 9.6\,\text{dB}, \qquad 1.22$$

$$NF_{654\,Mbps} = -65\,\text{dBm} + 101.6\,\text{dBm} - 25\,\text{dB} = 11.6\,\text{dB}, \quad 1.23$$

Intermodulation performance

The ability of an RF system to reject the interference emanating from adjacent channels is highly dependent upon the receiver architecture. It is well known that the super-heterodyne receiver has a better selectivity performance than the direct conversion receivers at the price of supplemental filters. Nevertheless, there are two critical functional blocks in the receiver chain, independently of the chosen architecture, that can seriously accentuate the adjacent channel rejection (ACR) problem. The first functional block is the low noise amplifier (LNA) that saturates at an input level around -15 to -20 dBm. In the presence of a strong in-band signal above this level, the LNA will inject non-linear distortion into the user channel. At the other end of the receiver is the analog-to-digital converter (ADC) that also has a limited dynamic range.

Data rate [Mbps]	Adjacent channel rejection [dB]	Non-adjacent channel rejection [dB]
6	21	40
9	19	38
12	17	36
18	15	34
24	13	29
27	11	30
36	9	28
48	5	21
54	4	23

Table 1.9. Adjacent channel rejection requirements for HIPERLAN/2 and IEEE802.11a

The adjacent and non-adjacent channel rejections are summarized in Table 1.9 for both IEEE 802.11a and HIPERLAN/2 standards. The values represent the difference between

the interfering and the user channel power. In both [7] and [11] specifications, the desired signal strength is 3 dB above the sensitivity level. For the level differences given in the Table 1.9, the Packet Error Rate PER should not rise above 10%.

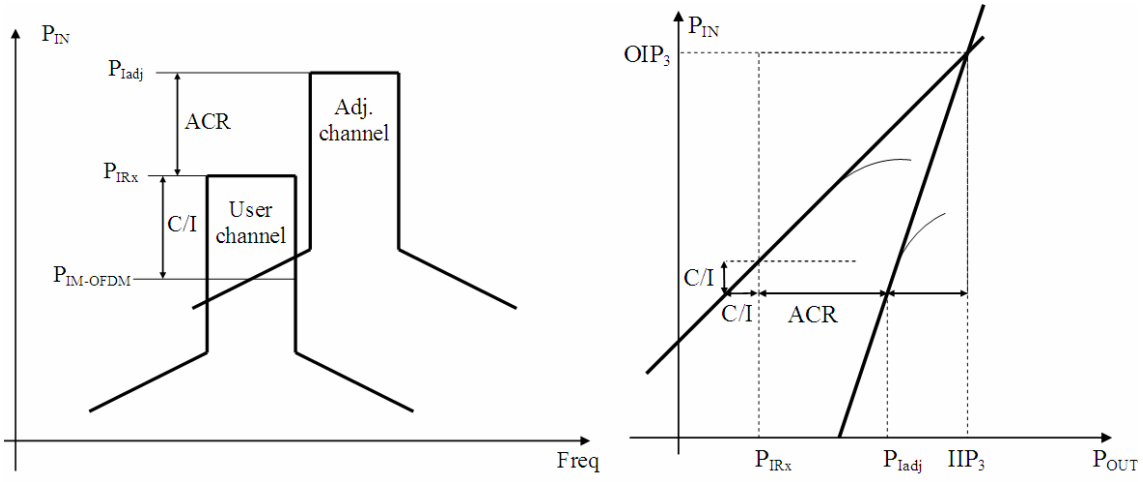


Figure 1.11. Estimation of the system third order intercept point IP3 from adjacent channel rejection specification

The degradation of the user channel signal in the presence of a strong adjacent channel is depicted in the left side of Figure 1.11. Here, the user channel has a lower input power P_{IRx} than the adjacent channel P_{Iadj}, the difference is the ACR defined in Table 1.9. System non-linearities like the third order intermodulation generate interference products (shoulders) in the user channel. When these shoulders rise above the acceptable carrier to interference ratio (7 – 25 dB depending on the data rate) the PER specifications are not fulfilled anymore. The same condition is depicted in the right side of Figure 1.11 using the well-known two-tone intercept point diagram.

The adjacent channel intermodulation power level is with *C/I* lower than the user channel input power. Mathematically, the condition is given as:

$$P_{IM-OFDM} = P_{IRx} - C/I\,, \qquad 1.24$$

Where: $P_{IM\text{-}OFDM}$ – adjacent channel intermodulation level for a OFDM signal,
P_{IRx} – input signal power level,
C/I – carrier to interference ratio.

Considering the intermodulation of a two tone signal, the relation that defines the input referred third order intercept point is well known:

$$IIP3 = \frac{3 \cdot P_{Iadj} - P_{IM-2Tones}}{2}, \qquad 1.25$$

Where: $P_{IM\text{-}2Tones}$ – intermodulation level of a two tones signal of power P_{Iadj},
P_{Iadj} – adjacent channel input power level,
$IIP3$ – input referred third order intercept point.

It can be demonstrated [16], that an OFDM signal like the WLAN signals will exhibit an intermodulation product power level, which is up to 6 dB higher than the IM level of a simple two-tone signal. Then, for a given P_{Iadj}:

$$P_{IM-OFDM} = P_{IM-2Tones} + 6\,\text{dB}, \qquad 1.26$$

Where: $P_{IM\text{-}OFDM}$ – adjacent channel intermodulation level for a OFDM signal,
$P_{IM\text{-}2Tones}$ – intermodulation level of a two tones signal of power P_{Iadj}.

From Equations 1.25, 1.26 and replacing P_{Iadj} with $P_{IRx} + ACR$, results:

$$IIP_3 = \frac{2 \cdot P_{IRx} + 3 \cdot ACR + C/I + 6\,\text{dB}}{2}, \qquad 1.27$$

Where: $IIP3$ – input referred third order intercept point,
P_{IRx} – input signal power level,

ACR – adjacent channel power ratio as defined in Table 1.9,

C/I – carrier to interference ratio whose dependence on the PER is shown in Figure 1.11.

On the same basis, one can define a similar relation for the Input Referred Second Order Intercept Point *IIP2* for which we have:

$$IIP2 = 2 \cdot P_{Iadj} - P_{IM-2Tones}, \quad 1.28$$

Where: *IIP2* – input referred second order intercept point,

P_{Iadj} – adjacent channel input power level,

$P_{IM\text{-}2Tones}$ – intermodulation level of a two tones signal of power P_{Iadj}.

Taking into account the difference between the second order intermodulation power of an OFDM signal and the second order intermodulation power of a two tone signal that can be as high as 17 dB [17], it results than:

$$IIP_2 = P_{IRx} + 2 \cdot ACR + C/I + 17\,\text{dB}, \quad 1.29$$

Where: *IIP2* – input referred second order intercept point,

P_{IRx} – input signal power level,

ACR – adjacent channel power ratio as defined in Table 1.9,

C/I – carrier to interference ratio whose dependence on the PER is shown in Figure 1.11.

Conclusion

Depending on the receiver front-end architecture, the effect of the second order intermodulation product is more or less important. Anyway, the effect of the intermodulation products cannot be independently defined. There are also other impairments of the front-end

like the IQ mismatch, the phase noise and so on that changes the linearity requirements of the system. The sum of impairments creates the need of a guard interval in terms of dB over the calculated worst case IIP3 and IIP2 for the given specifications. It was considered then that an IIP3 value of -15 dBm and an IIP2 value of 0 dBm is enough in order to achieve a 10% PER in the presence of an adjacent channel [18].

The 1 dB compression point can be deduced in several ways. There is a mathematical dependence between the third order intercept point and the P1dBCP. For a receiver modeled as an amplifier the P1dBCP should be about 9.6 dB lower then the IIP3. In the practical case, this rule does not apply always so the absolute value of the P1dBCP is hard to evaluate. Another method to establish the minimal value of the P1dBCP is to consider the maximum input level for operation test case described in [7] and [11]. For the first class receivers, the maximum input level has a value of -20 dBm in the case of HIPERLAN/2 standard and -30 dBm for the IEEE802.11a. Applying a guard interval of about 5 dB above the maximum input level for the P1dBCP, one can be sure that the receiver is still in its linear range also for the highest input power levels. With this assumption, the P1dBCP value would lay at -15 dBm at least. All system parameters analyzed in this chapter are enumerated together with their worst-case values in the Table 1.10.

Noise Figure	*NF*	9.6 dB
1 dB Compression Point	*P1dBCP*	-15 dBm
Input Referred Second Order Intercept Point	*IIP2*	0 dBm
Input Referred Third Order Intercept Point	*IIP3*	-15 dBm

Table 1.10. WLAN receiver system characteristics

1.4. Receiver Architectures

1.4.1. Heterodyne Receiver

In the heterodyne receiver, the frequency band is translated to an intermediate frequency (IF), which is usually much lower than the initially received signal frequency. Before this frequency translation, the signal is first filtered (band filtering) and amplified. After the translation, a channel filtering and the IQ demodulation follows. Alternatively, the signal at IF frequency is directly digitalized and the IQ demodulation is made in the digital domain.. The entire process is depicted in Figure 1.12

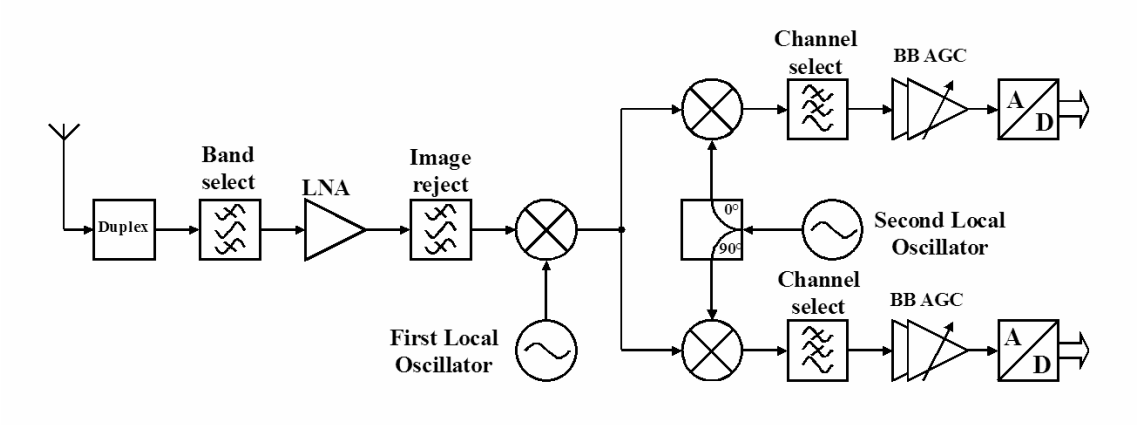


Figure 1.12. Heterodyne receiver architecture

It is important to distinguish between the signal *band* that includes the entire spectrum in which the users of a particular standard are allowed to communicate and the *channel* that refers to the signal bandwidth actually used by a single user in the system. The terms “band selection” and “channel selection” refer to the operations that reject out-of-band interferers and out-of-channel (usually in-band) interferers, respectively.

The first block in the receiver is the band selection filter that rejects the out of band interferers from the received signal, postponing the channel selection to the other point in the receiver. There is always a trade-off between the selectivity of this filter and its transfer

loss. Considering that the filter loss decreases the sensitivity of the entire receiver, one has to consider very carefully the choice of the out of band rejection parameters for the band select filter. Even a very selective band selection filter cannot reject the in-band interferers. For these interferers, the linearity of the LNA (low noise amplifier) is very important, particularly the odd-order non-linearity that yield intermodulation products that fall in the desired band. As third order distortion is usually dominant, the IIP3, of each stage must be sufficiently high to avoid corruption of the signal by the intermodulation products.

As the first mixer down-converts frequency bands symmetrically located below and above the local oscillator (LO) frequency to the same intermediate frequency, an image reject filter is necessary in front of the mixer in order to exclude the unwanted band (also known as image frequency band).

The choice of intermediate frequency (IF) strongly depends on both the characteristics of the received signal and of the type of filters used for image rejection and channel selection. Another criterion is the availability and the physical size of the filters. Today's wireless communication systems use external acoustic wave (SAW) filters, because the implementation of active RC filters would need too much power for the required performance.

Concerning the image reject filter and the channel filter, there is a trade-off between the rejection of the image frequency and the selectivity of the channel selection filter [19]. For a higher IF frequency (see Figure 1.13 (a)), the distance $2\omega_{IF}$ between the RF and the image frequency allows a better image rejection. On the other hand, the channel select filter whose resonance frequency is centered on ω_{IF} must have a very good selectivity in order to filter the in-band spurious signals. The low IF heterodyne receivers offer the advantage of good channel selectivity but the specifications for the image reject filter are very tight. To minimize the image, one can either increase the IF or tolerate greater loss in the image reject filter while increasing its Q. This fact is presented in Figure 1.13 (b) where the in-band spurious signal are better filtered at the lower IF but the image interference is stronger.

The choice of the intermediate frequency is therefore dictated by the frequency spectrum and the characteristics of the signal to be received. The level of the in-band spurious signals and the influence of the image band are the two factors that must be taken into account for the choice of the intermediate frequency.

Concerning the local oscillator (LO) frequency, it can be higher or lower than the center of the desired band. In Figure 1.13 is presented the first case known also as "high-side injection". The second case where $\omega_{RF}>\omega_{LO}$ known as "low-side injection" have the advantage of a lower LO frequency that simplify the design of the local oscillator, but this situation is not always desirable hence the image bands below and above the desired band exhibit different amounts of noise. The ω_{LO} must be chosen to avoid the noisy image band.

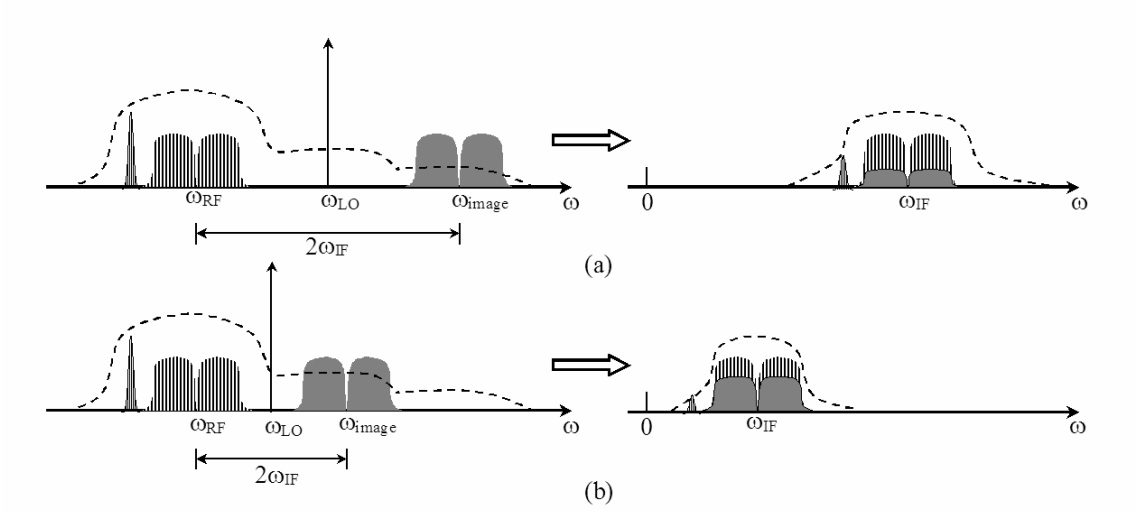


Figure 1.13. Rejection of the image vs. suppression of interferers for (a) high IF and (b) low IF

In addition to the mixer linearity case, the choice of the intermediate frequency may also be critical to the performance of the heterodyne receive. More exactly, the second order distortion products can contribute to the signal degradation. This effect in the heterodyne receivers is known as the *half-IF* problem [20]. Considering the "high-side injection" case, an interferer at $(\omega_{RF}+\omega_{LO})/2$, i.e. at the equal distance from both the ω_{RF} and ω_{LO} as depicted in Figure 1.14 will be transferred at the $|(\omega_{RF}+\omega_{LO})-2\omega_{LO}|=\omega_{IF}$ by a mixer that ex-

periences a strong second order distortion if the LO contains a significant second harmonic as well.

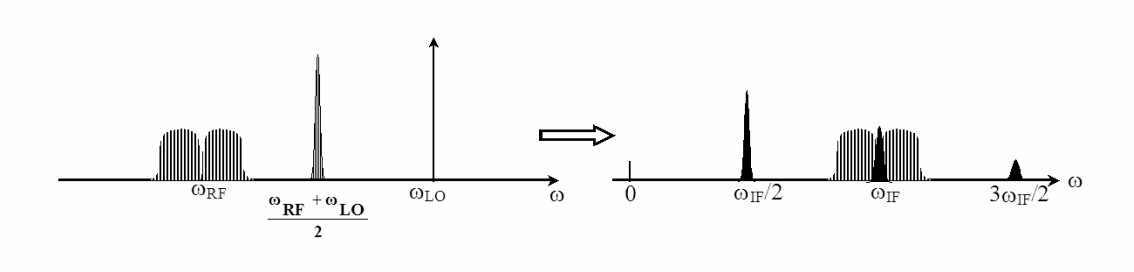


Figure 1.14. Problem of half-IF in heterodyne receivers

The super-heterodyne receiver proves to be a viable solution taking into consideration system requirements like selectivity, dynamic range or third order intercept point. In fact, all these parameters are strongly interconnected. The dynamic range of the system is defined as the ratio between the maximum power a receiver can handle and the minimum detectable received signal power [21]. Referring to the third order intercept point IIP3, the dynamic range of the system is defined as the ratio between the IIP3 and the receiver sensitivity S. A system with the total IIP3 of –5 dBm for example, and the sensitivity level at –105 dBm, will have a dynamic range DR equal with 100 dB. The total IIP3 of the system depends strongly on the selectivity of the channel filter. Therefore, the heterodyne receiver has a strong advantage against the other types of receiver architectures that do not possess such selectivity.

On the other hand, the filters that confer the selectivity are very difficult to integrate on chip. Such external filters are generally optimized for a certain mode of operation resulting in a fixed bandwidth and center frequency. For that reason, once designed, the system is difficult to reconfigure. That represents an important disadvantage of the heterodyne receiver. The mobile communication standards of third generation as the UMTS include the possibility of additional chip rates to the base chip rate of 3.84 Mcps in future releases [3]. Such rates like 0.96 Mcps, 7.68 Mcps or 15.36 Mcps (multi-band operation) cannot be supported by a heterodyne receiver with an external SAW filter.

The difficulties of multi-band operation remain also critical for the multi-standard operation of the heterodyne receiver. A WLAN/UMTS reconfigurable receiver would require a receiver front-end that can handle both 20 MHz and 5 MHz signals. The multi-band and multi-standard capabilities can only be implemented by using separate IF sections for each mode. This represents a clear drawback that together with the complexity of the system and the large number of components will increase the costs of such receiver architecture.

1.4.2. Zero IF Receiver

The Zero-IF receiver, also known as direct conversion or homodyne receiver is the most direct implementation of an RF receiver. As shown in Figure 1.15 the zero-IF receiver is a much simpler structure compared with the heterodyne receiver. The signal is first filtered by a band pass filter that is usually off-chip and amplified before is down-converted by an IQ demodulator to the baseband. The mixers that form the IQ demodulator will generate also some higher order harmonic products that must be filtered with the low pass filters also presented in the figure. The baseband signal is finally amplified and digitalized by two analog-digital converters, one on each branch.

The zero-IF receiver offers a low cost alternative to the heterodyne receiver but have to overcome some disadvantages like flicker noise, DC offset, LO re-radiation or poor dynamic range. These aspects put until recently very difficult problems but progress in the IC design made the implementation of zero-IF receiver a more and more accessible solution [22].

Nevertheless, the zero-IF receiver suits very well for the implementation in reconfigurable systems through the absence of the external IF filter. Another clear advantage is the practical possibility to integrate the whole receiver (with the exception of the RF band select filter) on-chip. This possibility drastically reduces not only the producing costs but also the consumed power. Moreover, a zero-IF receiver does not have the image problem that is inherent in a heterodyne receiver. All these arguments led to the explosion of zero-IF re-

ceiver implementation on the market and the tendency is to replace the heterodyne receiver for all mobile communication standards.

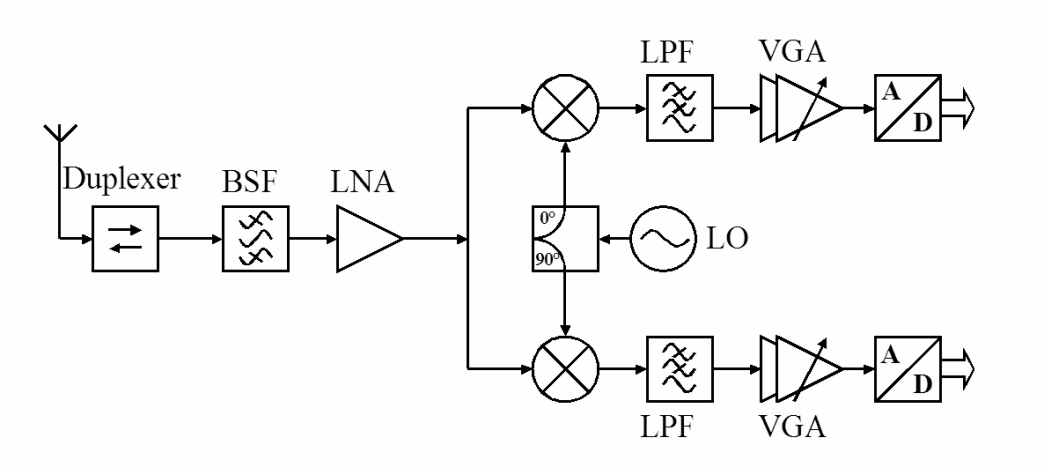


Figure 1.15. Zero IF receiver architecture

The simplicity of the zero-IF receiver comes with a price, namely the difficulty to achieve in only one stage a high dynamic range and a low noise figure concomitantly. The zero-IF receiver is also very sensitive at LO re-radiation and flicker noise. The LO re-radiation effect is given by the leakage of the LO signal towards antenna where is radiated in the air and finally reflected back by the multi-path fading. The re-radiated LO signal produces a self-interference effect, resulting a DC offset and with it the desensitization of the whole receiver.

Modern communication standards like the UMTS, specifies a very large dynamic range for their compliant receivers. Most of the amplification in such cases is contributed by the baseband amplifiers. That means that even small DC-offsets (in range of several mV) at the mixer outputs may lead to DC levels sufficient to saturate the analog to digital converter (ADC) [23].

The grade of re-radiation is given by the isolation between the signal path and the radiating elements in the receiver, the most important radiating element being the antenna. Very im-

portant is also the LO-RF isolation of the mixer and the reflection factor at the LNA output. The band pass filter at the input of the receiver allows the propagation of the LO frequency and therefore cannot contribute to the limitation of the re-radiation effect. The DC offset generated in this way is a time varying effect and is more difficult to be cancelled than a constant DC offset.

The same type of self-mixing phenomena occurs if a large interferer from the LNA leaks towards the LO input of the mixer. This unwanted effect will produce a constant DC offset that is easier to reject in the digital back-end of the receiver. All these leakage effects are depicted in Figure 1.16.

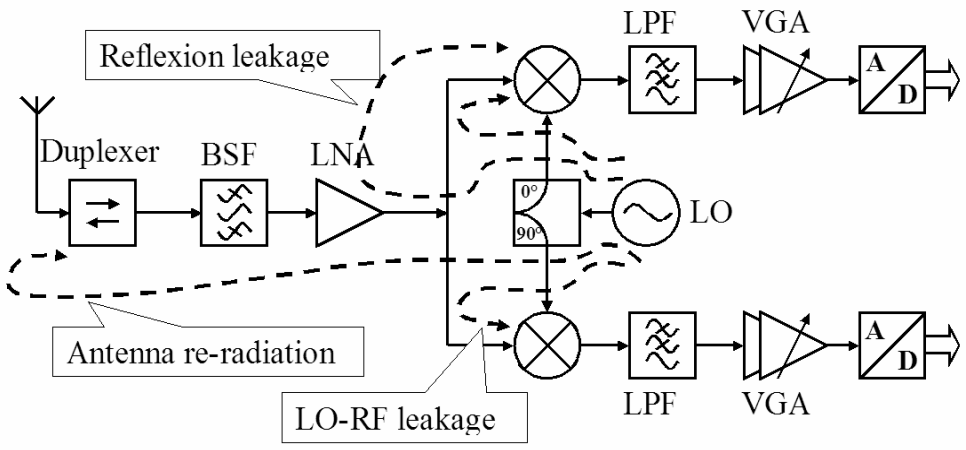


Figure 1.16. DC offset sources in Zero-IF receiver

An important low frequency interference source in zero-IF receivers is given by the second-order non-linearity in circuit elements, which behave like a squaring function. Given that the LO frequency equals the carrier frequency, any signal passing through a second-order non-linearity appears at the output of the receiver as a low frequency component plus a second order harmonic. The latter can be filtered out by the analog low pass filter, but the former is much more difficult to eliminate because the baseband signal generally has sig-

nificant spectral content near DC. Therefore, a large mixer IIP2 is needed to minimize the effect of a second-order non-linearity [24], [25].

One solution to overcome the DC offset problem is to apply a large enough AC capacitor so that the DC offset is blocked. Anyway, this solution can be applied only in systems whose distribution of energy in the frequency domain is diverted to the higher frequencies like MFSK. In such systems, the AC capacitor must be so large that the corner frequency would be at most 1% of the signal bandwidth [22]. For PSF or QAM systems, which have a strong DC content, line coding, may be used to introduce correlation in the modulated signal so that the DC energy is diverted to the higher frequencies. There are two problems resulting from the employment of AC capacitors in zero-IF receivers. In order to obtain lower corner frequencies on has to use very large capacitors in the order of nF or µF. Such capacitors are too large to be integrated on chip. Moreover, the large capacitors cause long recovery time due to the large time constant, which can be in the order of a few milliseconds. This can be critical for packet switched systems causing substantial over-the-air overhead.

Another solution to the DC offset problem is to use differential circuits through the RF receiver. Such balanced circuits have a high IIP2 and reject the DC component from the RF signal. In addition, DC offsets due to the re-radiation has equal power on both signal lines of the differential circuit and therefore can be cancelled out. However, the disadvantage of this solution is the increased complexity of the circuitry that will conduct to higher power dissipation also.

Finally, he DC offset can be estimated and cancelled either digitally or with specialized analog circuits. Digital offset cancellation requires a higher resolution of the ADC to provide a high dynamic range, since the cancellation happens only after the ADC. The optimum solution is a compromise between the digital and analog DC cancellation.

The Zero-IF receiver is also sensitive to the flicker noise generated by the mixer or the baseband circuits. This problem becomes more critical with the progress in Metal Oxide

Semiconductor (MOS) transistor technology because the continuously smaller transistor gate induces a higher level of flicker noise. The LNA circuit is not critical concerning this type of noise because its frequency band is much higher than the corner frequency of the flicker noise. Much more important is the mixer whose output is in the baseband frequency. The high impedance matching demanded by the LNA output to the input of the mixer imposes the use of smaller gate transistors for the mixer circuit. This restriction has as effect an increase of the flicker noise level in the baseband signal and can conduct to the desensitization of the zero-IF receiver. The low frequency circuits like the channel filters and the variable gain amplifier (VGA) are not so critical for the baseband processing chain if the active gate area of the transistors is sufficiently large to keep a low flicker noise level.

The effect of flicker noise can be reduced by a combination of techniques. For example, the use of resistive mixers instead of active may reduce considerably the level of flicker noise generated by the mixer. Moreover, periodic offset cancellation also suppresses low-frequency noise components through correlated double sampling [22].

1.4.3. Low IF Receiver

This receiver architecture was developed as a compromise solution to the Zero IF receiver. As depicted in Figure 1.17, the architecture is very similar with the one described in the precedent paragraph. Anyway, the RF signal is not more IQ demodulated directly into the baseband but at an intermediate frequency slightly higher than the half bandwidth of the user channel. In this way, the down-converted channel will land near the DC but with the entire frequency channel into the positive frequency axis and not half positive half negative as in the Zero IF receiver case. The advantage of this solution is obvious: one can filter the received channel with a channel select filter (CSF – see Figure 1.17) with a pass band characteristic instead of a low pass. The DC offset produced by the re-radiation effects described before can be here minimized by the channel select filter. The flicker noise becomes also a non-critical aspect in the low IF receiver because the intermediate frequency

can be chosen so that the lower channel frequencies are higher than the corner frequency of the flicker noise.

The disadvantage of the Low IF receiver against the Zero IF is that the suppression of the mirror signal must be higher. In Zero IF receivers, the mirror signal is the same as the wanted signal, and this means that a 40 dB suppression of the mirror signal does result in a carrier to interference ratio of 40 dB for the wanted signal. In low IF receivers, the mirror signal can be much higher than the wanted signal because at the origin they stem from different frequencies. A mirror signal suppression of 70 dB is required for a carrier to interference ratio of 40 dB when the mirror signal can be 30 dB higher than the wanted signal. A careful choice of the IF, so that the mirror frequency is situated between two transmission channels can be a solution to this problem. In this way, the suppression specs can be lowered with 50-60 dB.

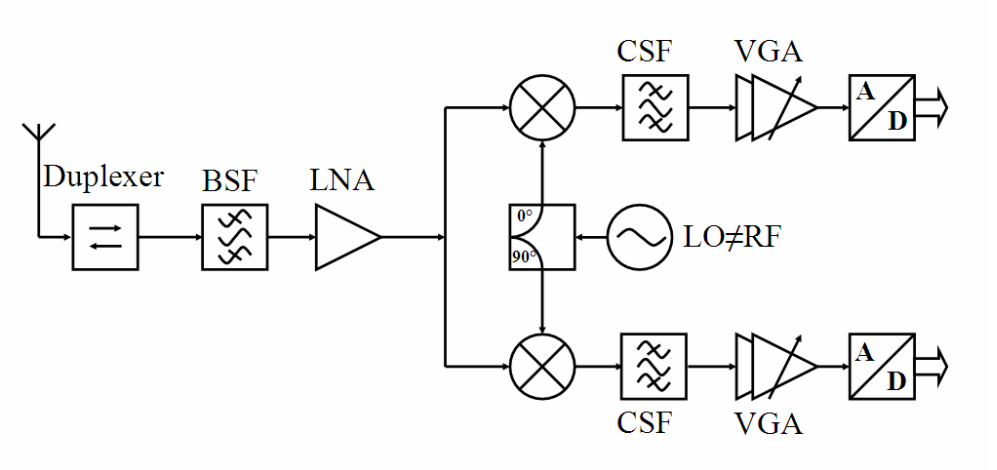


Figure 1.17. Low-IF receiver architecture

1.4.4. Direct Sampling Receiver

To achieve multi-standard ability, the analog-to-digital converter (ADC) should be placed as near the antenna as possible in the chain of RF components in the front-end. This solution is depicted in Figure 1.18 where the filtered frequency band received at the antenna is

amplified and delivered to the ADC [27]. The second condition is to process the resulting samples on a programmable micro or signal processor. Designing of analog functional blocks can be often expensive, while the digital programming is usually convenient and cheaper.

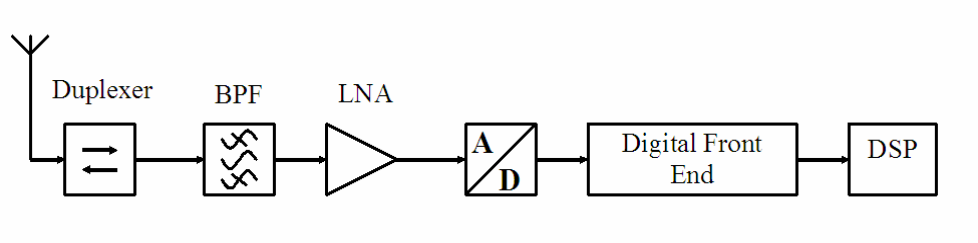


Figure 1.18. Direct sampling receiver architecture

Efforts are made to move the analog-digital converter (ADC) closer to the antenna but such approach has some serious drawbacks [28], [29]. Because the ADC would be exposed to numerous interferences, it must have a very wide dynamic range. That means that the resolution for the UMTS standards for example should be more than 16 bits. This huge dynamic range must be implemented at a carrier frequency around 2 GHz, requirement that not seems to be achievable in the near future.

One possible solution would be to include one or more frequency translations stages. However, this adds additional hardware between the antenna and ADC, adding in complexity and lowering the performance. A second option, which does adhere to the design goals, is the utilization of band-pass sampling.

Band-pass sampling is the intentional aliasing of the information bandwidth of the signal [30], [31]. The sampling frequency requirement is no longer based on the frequency of the RF carrier, but rather on the information bandwidth of the signal. Thus, the resulting processing rate can be significantly reduced. The drawback of this method is the overlapping of the frequency bands that requires a very good filtering and lowers the sensitivity of the receiver.

1.4.5. Half-IF Receiver

This type of receiver architecture was first presented in [32]. Until now was little researched, hence it appears only referenced in few other publications but no other authors seem to have experienced it. This architecture combines the advantages of both direct conversion and heterodyne receivers but, on the other hand, has its own characteristics that must be taken into account.

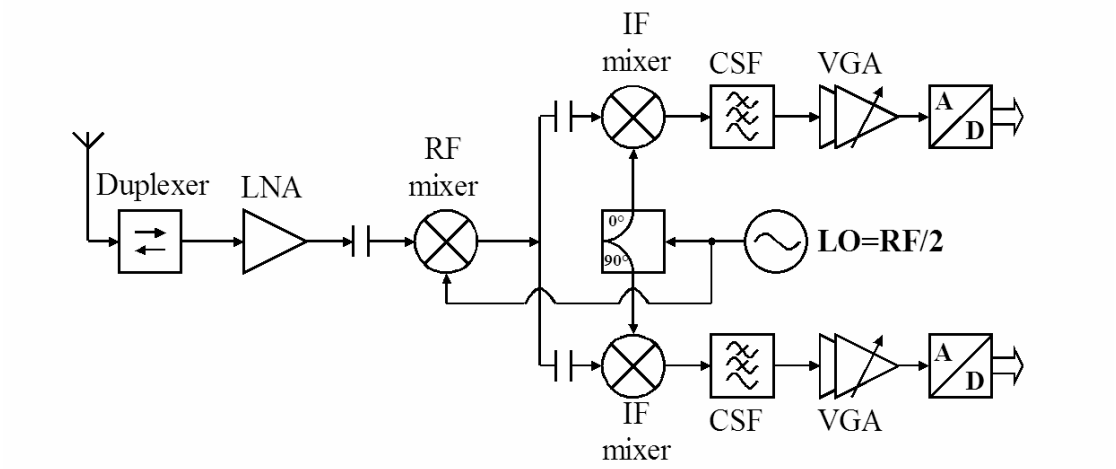


Figure 1.19. Half-IF receiver architecture

The circuit performs a first frequency translation from the RF frequency to an intermediate frequency that is half the RF frequency. Subsequently, the IF signal is translated directly into the baseband by an IQ demodulator driven by the same LO frequency as for the first frequency translation. As a result, we can realize the receiver with only a frequency synthesizer, although there is a double conversion of the signal. The receiver architecture is depicted in Figure 1.19.

The chosen frequency planning offers several advantages over that of conventional heterodyne or image reject architectures. Considering the architecture, the half-IF receiver looks like a high IF receiver because the intermediate frequency is rather high at the half the RF frequency. This solution eliminates the need of an image reject filter and therefore is well

suited for on-chip integration. The LO frequency needed for the first mixer is relatively low compared with the conventional heterodyne architecture, only at the half of the RF frequency, and therefore relaxes the requirements of the local oscillator. Another advantage is the image frequency, which is located around the DC point and therefore very efficiently rejected by the antenna and the LNA selectivity. Compared to the direct conversion architecture, the half-IF architecture creates less leakage at the antenna, also because the high difference between the RF and LO frequencies. Such leakage from the LO is rejected by the LNA and the antenna. Furthermore, unlike other image-reject receivers [33], it does not require extremely accurate phase and gain matching.

The half-IF architecture has also some issues to deal with, which are not so critical in other receiver architectures. Perhaps the most important is the flicker noise problem generated by the LNA and the input circuit of the first mixer. The small transistor dimensions cause flicker noise corner frequencies of up to several MHz, which can degrade considerably the sensitivity of the receiver. As depicted in Figure 1.20, the flicker noise generated by the LNA and the input circuit of the mixer is up-converted by the first mixer directly into the IF band without any attenuation.

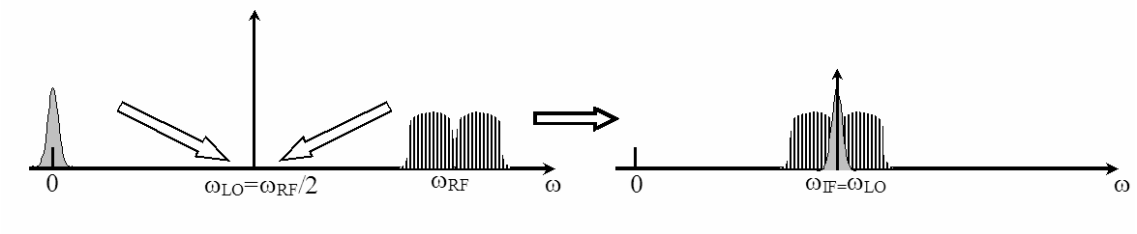


Figure 1.20. Up-conversion of the flicker noise at the IF frequency

Another spurious signal that land in the IF band resides from the LO-IF leakage of the first mixer. Because the leaked LO carrier may be considerably stronger than the RF signal, it may drive the mixer into saturation and create unwanted intermodulation effects. Moreover, the leaked LO signal will mix again with the same LO frequency in the IQ demodulator and create a critical DC offset for the ADC that will desensitize the whole receiver.

The compromise between the image rejection and channel selection presented for the heterodyne receiver is very important in the half-IF receiver. Here, the image band is pushed to the extreme and therefore very easy to filter. On the other side, the high IF frequency makes a channel select filter almost impossible to implement, even as external component. This compromise requires therefore a high linearity in the IF mixers to overcome the possible in-band blocking interferers.

1.5. UMTS-WLAN Reconfigurable Receiver

After extensive studies of the possible receiver front-end architectures, one can now make the choice of the best combination of architectures that would receive both UMTS and WLAN standards. In the present project, the main purpose is to demonstrate the reconfiguration principle both in the front-end as in the back-end of the UMTS-WLAN receiver. In this scope, the simultaneously reception of both standards was not part of the projects desiderates. Instead, it was specified a possible “cold” or “warm” switch between the received standards, meaning that during the standard switch, the user equipment should be switched off or remain on, respectively. This basis specification offered the freedom to maximize the principle of re-configurability and to introduce a new concept in the design of multi-standard receivers, the principle of reusability. This means, that functional blocks or entire paths of the receiver can be active during the reception of each of the standards. The reusable functional blocks are therefore designed to comply with signals stemming from both UMTS and WLAN standards. There are two possibilities to design such reusable functional blocks. The first one is to design a parametrical functional block, whose characteristics change depending on the input signal. The second solution is applicable only for some of the functional blocks and implies that they are designed to be un-sensitive to the input signal, meaning that these functional blocks would be able to process the signals independently of the active standard.

The complete consideration of the entire signal path for both standards makes obvious that the most desirable segment to reuse is the final one, meaning the IQ demodulator, the auto-

mated gain control block, the channel filter and the analog-to-digital converter. Even if the channel bandwidth of both standards is different, it is possible to modify the functional block parameters to comply with them. The most important fact is that the carrier frequency along the defined path remains the same for both standards. This condition is fulfilled by the IQ demodulator that translates the received signals into the baseband. As the first functional block in the common processing path, the IQ demodulator has to meet very high requirements concerning the linearity, input frequency range and noise figure.

The selected common architecture is shown in Figure 1.21. For the UMTS standard, a direct conversion receiver solution was chosen. As explained before, this solution offers the best control of the frequency conversion and the highest integration percent. For the WLAN standards, the Half-RF receiver solution promises the most advantages in combination with the direct conversion solution for UMTS. The most important advantage is the translation of the intermediate frequency IF in a domain near the UMTS RF frequency band, which allows the use of a single voltage controlled oscillator VCO for both standards. As stated before, the WLAN standards are transmitted at frequencies between 5.15 and 5.825 GHz. Halved will result an intermediate frequency range between 2.5 and 2.9 GHz that together with the frequencies around 2.1 GHz of the UMTS standard must be addressed by the IQ demodulator. The entire IF frequency range will be about 700 MHz wide that is a challenge for the voltage-controlled oscillator. Anyway, this frequency band is not continuous but comprised of relative narrow segments spread over the entire band. This gives the possibility to realize a reconfigurable common VCO that can switch between these frequency segments.

The IQ demodulator mixers are also very challenging to design. Their input port must be matched for the entire frequency range of 700 MHz of the IF signal. As stated in 1.4.2, the port-to-port isolation is a critical aspect because of the Zero-IF architecture for the UMTS standard. Concerning the WLAN standard, from the Half-RF receiver characteristics described in 1.4.5, the mixers will have to exhibit a very low flicker noise level. A double

balanced solution for these mixers will improve both requirements but a careful design of the layout symmetry is very important in order to achieve the desired characteristics.

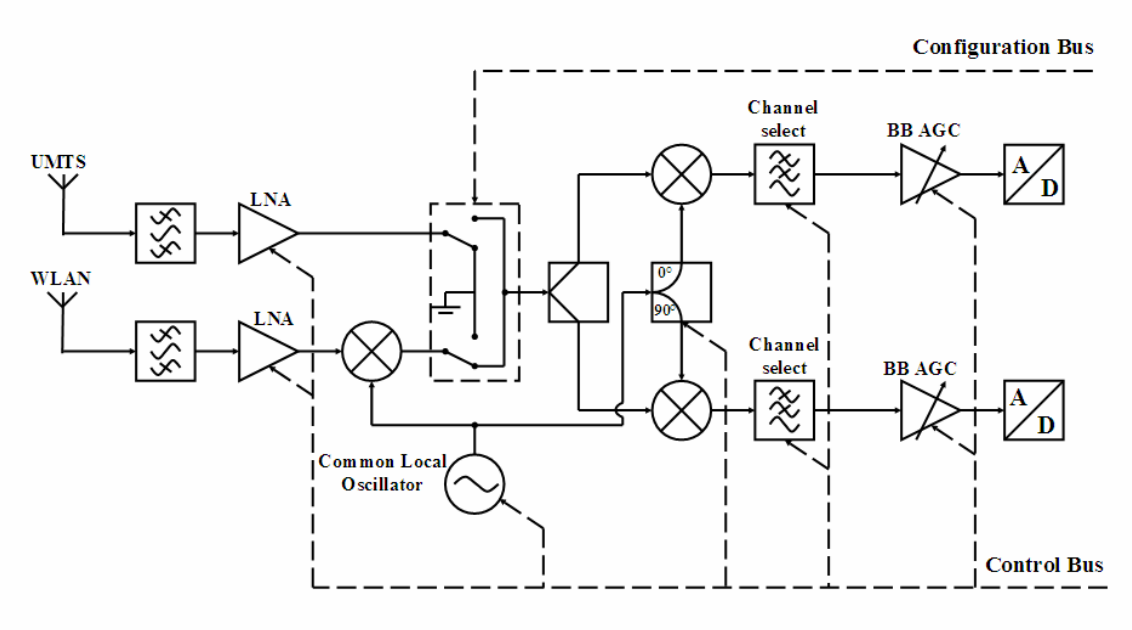


Figure 1.21. UMTS-WLAN reconfigurable receiver architecture

The central block of the front-end receiver is the standard switch, also presented in Figure 1.21. The standard switch is controlled by the configuration bus, a signal coming from the digital back-end that controls the standard being received both in the analog and digital domain. The switch links the RF signal path of the standard being received with the common baseband path. The signal path of the idle standard is isolated and the active components like the LNA are switched off. The control bus is the second path of communication between the digital back-end and the analog front-end. Its task is to adapt the functionality of the functional blocks in the front-end to the characteristics of the signal being received. This implies also to switch off the active functional blocks that are not used for one particular standard reception, which is very important in order to reduce the power consume and to isolate the signal paths. The control bus will be a digital signal comprised from several bits that along with the switch of the unused functional blocks will also control the

amplification of the baseband amplifier, the oscillation frequency of the voltage controlled oscillator or the pass-band of the low pass filter.

Concerning the system specification for the combined receiver architecture, the requirements defined in 1.2.2 and 1.3.2 must be tightened to address the possible leakages from one path to the other.

Chapter 2.

Comparison of Different FET Mixer Circuits

2.1. Overview of Existent FET Mixers

For most types of communication receivers, a mixer must have a low noise figure and adequate, but not excessive, conversion gain. In a FET mixer, these two properties are more or less independent. This is somewhat different from the Schottky diode mixer where the minimum noise and conversion loss usually occur together. Concerning the resistive mixers that have a conversion loss instead of gain, they present the advantage of generating exclusively thermal noise and are not subject to shot-noise like the diode mixers. As the gate length of standard CMOS processes achieves sub-micron orders, RF performance is becoming accessible for CMOS transistors. These processes offer a much higher integration density for much less power consumption and production costs.

Several of the circuit elements of a FET transistor are bias dependent. Hence, when a low level signal is applied to a FET pumped with a strong LO signal, the modulated circuit elements, will cause signal power to be converted to other frequencies.

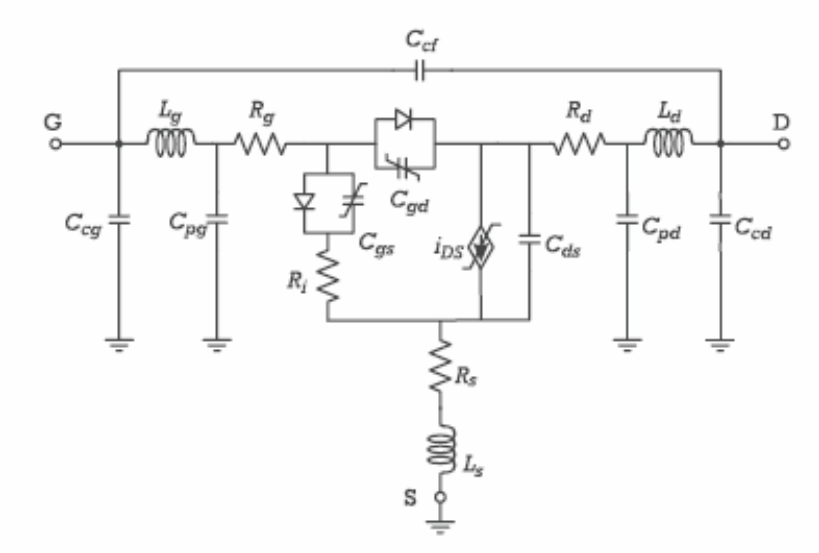


Figure 2.1. Large-signal equivalent circuit of a FET with the dominating nonlinear circuit elements

Figure 2.1 shows an equivalent circuit of a FET, indicating which circuit parameters are voltage-dependent. R_g, R_s and R_d are the parasitic resistances; L_g, L_s and L_d are the parasitic inductances (bond wire inductances) in the gate, source and drain respectively.

One can classify the simple, one-transistor, FET mixers into three categories:

- **Gate pumped transconductance mixers**: operate by changing the gate-source voltage, which swings the FET from the saturation region into the cutoff region. The gate pumped transconductance mixer is usually biased at the threshold voltage and is operated with a 50% duty cycle, which results in maximum conversion gain.
- **Drain pumped transconductance mixers**: operate by a drain fed LO modulating the drain-source voltage of the device. This voltage swings the FET from the linear region into the saturation region.
- **Resistive mixers**: operate by modulating the channel resistance (resistance between source and drain) with a large LO signal while keeping the FET in the linear region of operation. The FET channel is switched between fully depleted

and fully inverted regions of operation. To keep the FET in the linear region of operation no drain-source bias is applied.

The bias points for each of the described mixers are depicted in Figure 2.2.

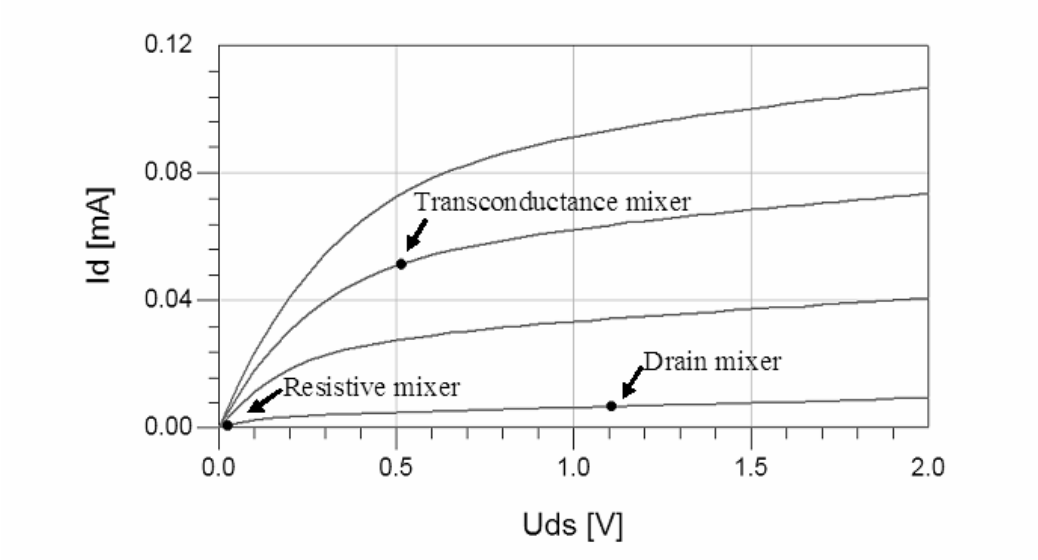


Figure 2.2. Bias points for gate pumped, drain pumped and resistive mixers

Each of the above-described mixers possesses particular advantages and disadvantages that qualify them or not for integration in the reconfigurable mobile receiver described in the first chapter. Further, each of these mixers will be considered and their characteristics and performance will be analyzed.

2.1.1. Gate Pumped Transconductance Mixer

The gate pumped transconductance mixer exists in several constructive variants, as single or multiple gate transistor mixer. The common characteristic is, that the LO signal is delivered at the gate of the transistor. The block diagrams of such mixers in their most simple form are shown in Figure 2.3. For the left variant, where both RF and LO signals are delivered at the gate of the same transistor, some filtering is necessary in order to isolate the

signals. The depicted filter blocks present the proper terminations to the FET's gate and drain at unwanted mixing frequencies, and provide port-to-port isolation. The bias voltages also depicted in Figure 2.3 drive the transistor in the saturation region.

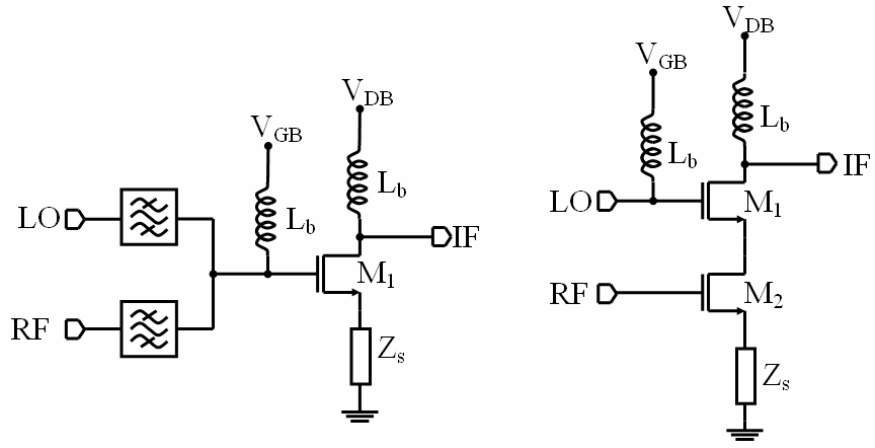


Figure 2.3. Single (left) and dual (right) gate pumped transconductance mixers

The mechanism of these mixers and optimization principles were extensively explained in [34] – [37] so it will not be treated here anymore. The most used solution on the mixer field today, proved by the huge number of publications written in the last ten years seams to be given by the more complex single and double balanced (Gilbert Cell) gate transconductance mixer that will be shortly analyzed in the next paragraphs. These mixers belong also to the gate pumped transconductance mixer although they contain three to five transistors. Both mixers are depicted in Figure 2.4.

A single balanced active mixer is shown in the left side of Figure 2.4. The transistor M_3 acts as a trans-conductor that converts the RF signal v_{RF} into a current of magnitude $g_{m3}v_{RF}(1+sg_{m3}L_s)^{-1}$. Transistors M_1 and M_2 act as current switches that steer the current depending on the polarity of the LO signal v_{LO}. The overall effect of current steering is mixing the current through M_1 with a square wave, which has a fundamental frequency at ω_{LO} with the associated odd harmonics. The desired frequency component is obtained by properly filtering the mixer output, usually with the tuned load Z_L.

The feed-through of the LO signal to the mixer output can be reduced with a double balanced configuration shown in the right side of the Figure 2.4. Since the drain current in M_3 (in the left side) is a function of $g_{m3}v_{RF}$, the mixer response can become non-linear at higher RF signal levels. To linearize the mixer, the source degeneration inductor is selected such that $\omega g_{m3} L_G >> 1$ thereby making the current independent of the transistor transconductance g_{m3}.

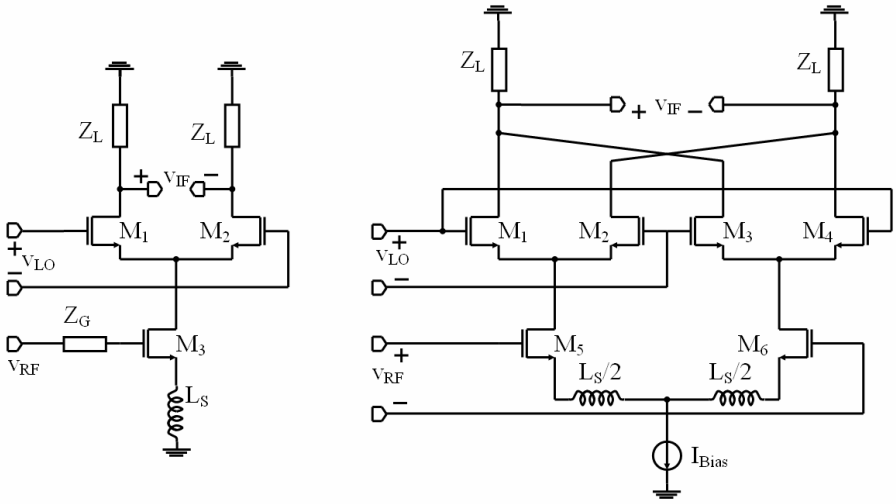


Figure 2.4. Single balanced (left) and double balanced (right) gate transconductance mixer

A study on the most recent publications that describe the realization of some gate pumped transconductance mixers (mostly of them as double balanced solutions) was brought together in Table 2.1. Even if not all publications describe the same mixer parameter suite, one can extract some trends and limitations of this type of mixers. For example, one can observe that all mixers exhibit very high levels of noise figure NF that overstep the value of 10 dB. The conversion gain CG, on the other side, spread over a wide range of values. One can clearly remark a trade off between the conversion gain of the mixer and its consumed power. The input referred third order intercept point IIP3 represent a critical point in the design of such mixers. Their values hardly fulfill the specifications of the reconfigurable UMTS-WLAN receiver front-end. In addition, the input referred 1 dB compression point P1dBCP, exhibit relatively low values over the entire table. Another aspect that

must be taken into consideration is the consumed power that for some of the mixer solutions proves to be relative high. As a conclusion, the gate trans-conductance mixer solution has the singular advantage of presenting a conversion gain that is directly proportional with the consumed DC power.

Ref.	Tech. [µm]	V_{DD} [V]	I_{DD} [mA]	f_{RF} [MHz]	f_{IF} [MHz]	P_{LO} [dBm]	CG [dB]	CP_{1dB} [dBm]	IIP3 [dBm]	NF_{SSB} [dB]
[39]	0.18	1	0.18	-	-	-	12	-	4	22
[40]	0.8	3	2.3	1900	250	5	0	-10	2	13.6
[41]	0.35	2.7	6	900	0	-	18	-	-4	18
[42]	0.35	2	5	3000	100	-	9	-	5	18
[43]	0.35	0.9	5.2	900	100	-12	3	-8	3.5	13.5
[44]	0.25	1	4.5	1900	210	-15	3.6	-	-1	12.5
[45]	0.35	2	4.7	2400	100	-5	9.48	-8.7	3	17.7
[46]	0.18	0.8	0.5	1900	250	0	3	-	-11	10

Table 2.1. Performance comparison for several recently published gate transconductance mixers

2.1.2. Drain Pumped Transconductance Mixer

The fundamental block diagram of the drain pumped transconductance mixer is depicted in Figure 2.5. For this constructive solution, the LO signal will be applied at the drain of the transistor and the transconductance will be a nonlinear function of V_{ds}. This mixer type present an important advantage compared with the gate pumped mixer. The RF and LO signals are injected at different ports, simplifying the filtering and improving the LO-RF isolation. This advantage qualifies the drain transistor for direct conversion receivers where the LO-RF isolation plays an important role in the overall system performance.

The FET transistor must be biased at the transition between the linear and the saturation regions where the maximum level of non-linearities are generated and the g_m will have the

maximum amplitude variation. For aggressively down-scaled FET's, the drain saturation voltage $V_{ds,sat}$ is very small, and a zero DC voltage in the transistor drain will permit the mixer to function with relatively low deterioration of the conversion gain. In this case, the V_{gs} must be large enough ($V_{gs}>V_{th}$) to provide adequate magnitude to g_m, Otherwise, the g_m will be too small, in which case the R_{ds} element would dominate.

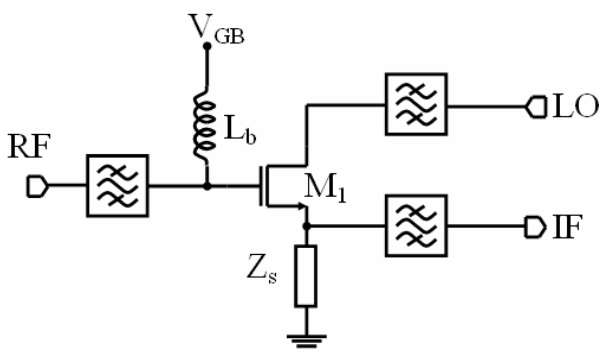


Figure 2.5. Single balanced drain pumped transconductance mixer

If the biasing conditions were met, the transconductance g_m would show a time characteristic that can be approximate through a sine function with 50% duty cycle (only the positive wave part would exist, the rest of time being zero). For higher values of V_{gs} the g_m will converge more and more to a step function and introduce increasingly stronger intermodulation products.

Another constructive solution of the drain pumped transconductance mixer is given by the distributed mixer depicted in Figure 2.6. This solution, which offers an ultra-wideband performance was firstly proposed in [47]. The idea derives from the distributed amplifiers. The key to the design of a distributed mixer is to allow the RF and LO signals to propagate along the transmission lines also depicted in Figure 2.6 with minimum attenuation, as well as to ensure that all the IF output currents generated at the drain of each transistor propagate and arrive at the forward drain output termination in phase. In essence, the concept of distributed mixing is based on the idea of separating the input as well as output capacitan-

ces of the transistors connected in parallel by means of artificial transmission lines, while effective adding their conversion trans-conductances.

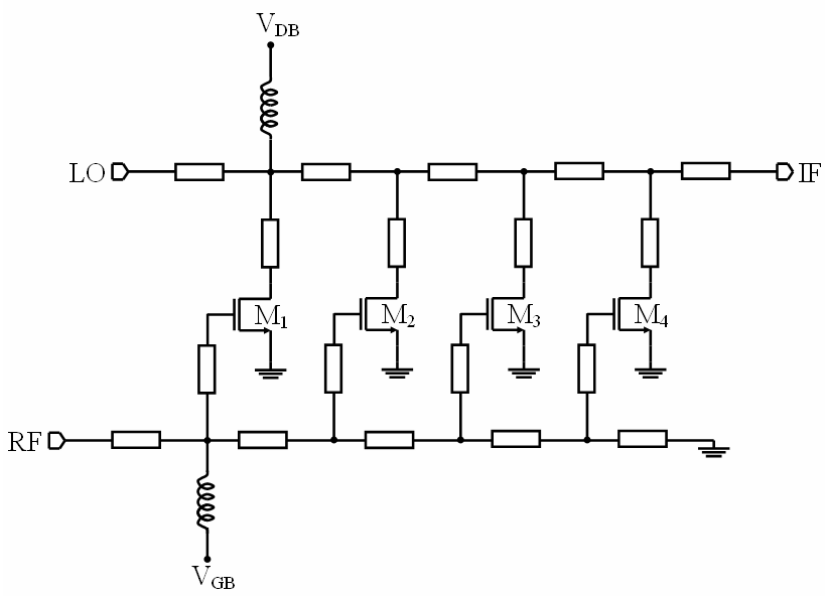


Figure 2.6. Distributed drain pumped transconductance mixer

The Table 2.2 offers again an overview of the most recent realized mixers with this architecture. One can already observe the wideband mixers in distributed variants from their up to one decade RF input [49], [50].

Ref.	Tech. [µm]	V_{DD} [V]	I_{DD} [mA]	f_{RF} [GHz]	f_{IF} [MHz]	P_{LO} [dBm]	CG [dB]	CP_{1dB} [dBm]	IIP3 [dBm]	NF_{SSB} [dB]
[48]	0.09	-	-	35	2500	7.5	-4.6	-6	2	7.9
[49]	0.15	1.1	-0.7	3-33	100	13	-1	0	10	-
[50]	0.18	-	-	25-40	100	18	-2	0	-	-
[51]	0.2	0.3	0.2	60	-	10	3.7	-	-	7.8
[52]	0.2	0.6	-	14-16	1000	15	2	-	2	7.6

Table 2.2. Performance comparison for several recently published drain pumped trans-conductance mixers in plain and distributed form

Concerning the used technology, with the exception of the first mixer [48], that is realized in an advanced CMOS process, all other mixers are realized in GaAs HEMT technologies. The drain transconductance mixers seem to be used almost exclusively for millimeter wave applications where they are a good alternative to the active mixer topologies. Even if the conversion gain is for most of them negative, or very small compared with the active mixers, they tend to have also very good noise figure (NF) values.

Unfortunately, the published papers failed to present very much results concerning the intermodulation behavior of these mixers, but they usually present a good performance concerning the LO RF isolation. It is obvious that this fact resides from the separation of the two signals at the transistor inputs. As a conclusion, the drain pumped mixers seem to be a good alternative that qualify them for a reconfigurable mobile terminal, but they do present some problems concerning the relatively low intermodulation performance and the fact that they need prohibitively high LO power values.

2.1.3. Resistive Mixer

The third constructive solution for the FET mixers is the resistive mixer. The fundamental difference against the previously described mixer topologies is given by the fact that the channel conductance is the primary nonlinear element, which realizes the mixing process. In the current topology, no DC bias is applied at the drain of the transistor, which will transform the FET into a voltage-controlled resistance. This constructive solution in its most simple form is presented in Figure 2.7.

The gate bias is set near the threshold voltage V_{th}, in order to provide the dynamic range of the channel conductance necessary to minimize the conversion loss. The channel conductance performs in this situation as a voltage controlled switch controlled by the large signal LO supplied at the transistor gate. The RF small signal delivered to the transistor drain determines the mixed current that flows through the channel. As in the drain pumped transconductance mixer, the LO and RF signals are better isolated from each other because are supplied at different ports of the transistors. Anyway, for a single balanced mixer structure,

this isolation is still to low, so a supplemental filtering is necessary. Together with filtering, also matching networks are needed do provide the maximum signal strength at the mixer inputs.

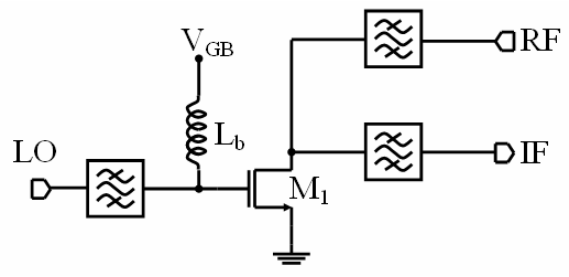


Figure 2.7. Unbalanced resistive FET mixer

A better isolation against the LO coupling problem can be offered by a single balanced mixer topology as presented in Figure 2.8. For this solution, the LO signal is provided in a balanced form to the gates of the transistors. In the positive stage of its duty cycle, the transistor M_1 is closed and the transistor M_2 is open. For the negative stage, the conduction inverts, so the both transistors will function only for one half of the period. The RF signal is provided at the common gate of the transistors and the balanced IF signal is present at the both sources. In the unbalanced topology, a part of the LO voltage can leak over the C_{gs} and C_{gd} capacitances to the transistors source and drain, respectively.

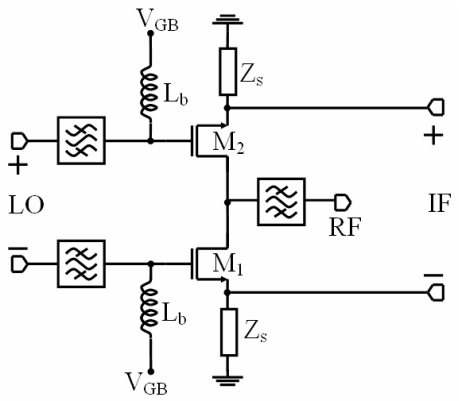


Figure 2.8. Single balanced resistive FET mixer

The advantage of this topology, is that the LO voltage will evanish at the IF output of the mixer. This will dramatically increase the LO-IF isolation compared with the unbalanced mixer. The second advantage is represented by the suppression of all other odd harmonics of the LO signal because of the balanced topology. Not only the LO-IF leakage can be very disturbing for our mobile terminal but also the LO-RF leakage, especially for the direct conversion branch. In order to solve this problem a double balanced mixer topology may be proposed as the one depicted in Figure 2.9.

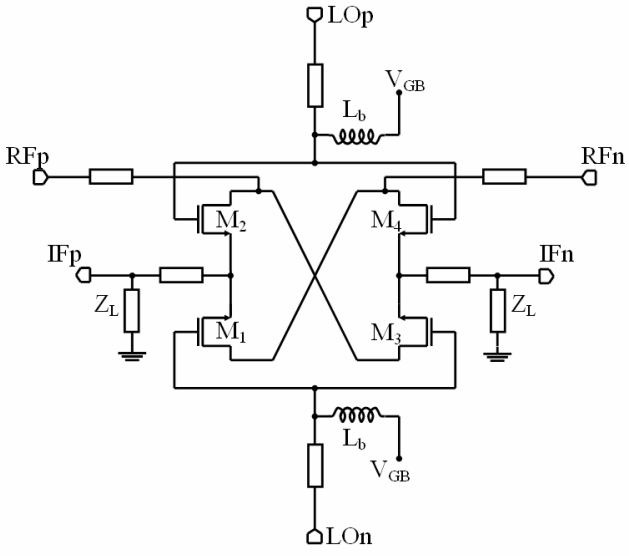


Figure 2.9. Double balanced resistive FET mixer

The functional principle of the double balanced mixer is exactly the same as for the single balanced solution, only that this time, always two transistors are in conduction and the other two are closed in one half of the LO duty cycle. For the positive stage of the LO wave, the transistors M_2 and M_4 are on conduction and $M_1$and M_3 are on high impedance.

The balanced RF input assures that the odd harmonics of the LO signals that leak through the C_{gd} will be attenuated not only at the IF port but also at the RF port. The same thing happened also with the odd harmonics of the RF signal. That topology will improve dramatically the intermodulation distortion (IMD) performance of the mixer.

Table 2.3 offers an overview of the most recent publications implying resistive mixers. The suite of publications is intended to be a homogenous collection with similar values of frequency, but with different fabrication processes and usable power levels. In this way, one can extract some characteristics of the mixers that are independent on the above mentioned parameters. The technologies spread from the digital CMOS processes through GaAs high power MESFET. Compared with the previous enumerated transconductance mixers, the resistive mixer topologies are characterized by the relative high levels of LO power needed. The mixers developed for mobile terminal applications, will need a level of available LO power between 0 and 7 dBm, whereas the base station mixers will need more LO power in order to provide the required high linearity. The conversion gain has, as expected, negative values between -5 and -8 dBm because of the passive nature of the mixers. This relative disadvantage compared with its active counterparts, is well balanced by the exceptional linearity, these mixers offer. Input referred third order intercept points (IIP3) of up to 20 dBm are very usual values among them. The second strong argument for the use of resistive mixers in the UMTS-WLAN receiver constitutes the low levels of noise figure published in these papers and the exceptional isolation performance of the double balanced solutions.

Ref.	Tech. [µm]	V_{DD} [V]	I_{DD} [mA]	f_{RF} [GHz]	f_{IF} [MHz]	P_{LO} [dBm]	CG [dB]	CP_{1dB} [dBm]	IIP3 [dBm]	NF_{SSB} [dB]
[53]	0.35	2	100	7	-5.5	5	15	62	62	11
[54]	0.6	5.2	950	0	-7.4	4	13	17	14	7.9
[55]	0.25	1.8	170	14	-5.8	10	19.5	43	-	-
[56]	0.3	5.8	100	4	-7.8	-	12	60	50	-
[57]	0.5	2	300	5	-8	-	-	-	-	-

Table 2.3. Performance comparison for several recently published resistive mixers

2.1.4. Conclusion

After this thorough study of the different mixer topologies proposed in the literature a decision has been made in favor of a resistive mixer as the best solution with respect to the UMTS-WLAN system requirements. Because of the mentioned advantages compared to their active counterpart, resistive FET mixers seem to be well suited candidates especially for direct conversion receivers. Besides of no DC power consumption passive FET mixers show very good performance with respect to port isolations, second and third order intermodulation and low frequency noise. These are key parameters of direct conversion receivers. Concerning the super-heterodyne branch of the UMTS-WLAN receiver, an IF amplifier can successfully balance the loss of RF power due to the resistive mixer. Another argument to the employment of the resistive mixer in the reconfigurable receiver is its exceptional constancy over wide frequency ranges. The resistive mixer topology proves to be very insensitive at process variations and mismatches. Concerning all these aspects, the resistive mixer confirms to be the best solution for the reconfigurable receiver architecture being capable to fulfill the system requirements.

Chapter 3.

Resistive Mixer Design and Measurement

3.1. Introduction

There are two particular mixers that were developed for the reconfigurable mobile terminal. The first one is employed in the super-heterodyne branch and down-converts the WLAN signal to the half frequency. The second will form, in a double configuration, together with a 90° phase shifter the IQ demodulator and will function for both super-heterodyne and direct conversion branches. These mixers will be identified after their purpose in WLAN mixer and IQ demodulator mixer respectively.

Both mixers are realized in a double balanced resistive topology and are different only concerning the frequencies of operation and consequently, the matching networks at the input ports. The WLAN mixer will have the LO and IF signals of similar frequency values whereas the IQ demodulator mixer will have comparable RF and LO signal frequencies.

The IQ demodulator mixer was realized in two different processes: 0.35 µm BiCMOS and 0.13 µm HCMOS, both from ST Microelectronics. The WLAN mixer was designed only in the 0.13 µm HCMOS process. The first design of the IQ demodulator was made to test the topology performances and to get accustomed with the design environment. In the reconfigurable demonstrator, the 0.13 µm technology mixer was employed because it offered

better performance with regard to the conversion loss, noise figure, port-to-port isolation and required available LO power. The description of the IQ demodulator mixer design process will imply the newest process involved, the 0.13 µm HCMOS. Anyway, because there are some differences in the schematics of the two IQ demodulator mixers, some indications to the first mixer design will also be made.

Concerning the differences between the two variants of the IQ demodulator mixer, the older 0.35 µm BiCMOS mixer used a higher LO available power (6 dBm) than the 0.13 µm HCMOS mixer (0 dBm). Consequently, the P1dBCP performance was better, even if the newer mixer fulfills the system requirement concerning this parameter. Enhancements concerning the geometrical symmetry of the 0.13 µm HCMOS transistor ring and the parasitic capacitances at the crossover of two transmission lines on the chip have brought a qualitative increase in the port-to-port isolation performance. The smaller transistor gate in the 0.13 µm technology determines a much smaller C_{gs} capacitance, which minimize the leaked LO, current at the transistor gate. This allowed us to let aside the matching network used to block this current at LO port and therewith to improve the constancy of the conversion gain over the LO frequency range.

Along with the mixer structures, several transistor test structures in common source topology were also tested on wafer. These structures were used for the characterization of the current-voltage (I/V) characteristics of the transistors modeled as BSIM3 models in the ADS design environment. The same structures were used to measure the low frequency noise performance of the particular transistors used in the mixer design.

In the next paragraphs, the schematic principle of the designed mixers will be described. The requirements of the IQ demodulator mixer and the WLAN mixer defined for the UMTS-WLAN reconfigurable receiver are listed in Appendix A, in Table A.1 and Table A.2 respectively. After a thoughtful analysis of the mixers schematic, the layout particularities will be described, followed by the post layout-processing procedures. Closing the chapter, a complete synthesis of the mixer performance will also be done.

3.2. Schematic Design

All mixer schematics were simulated using the Advanced Design System (ADS2003) application from Agilent. The transistor, inductance, capacitor and resistance models were provided by ST Microelectronics as design kits for both 0.35 µm and 0.13 µm processes. The simulations were made using the harmonic balance and the S-parameter simulation tool integrated in ADS. All components provided in the design kits have included parasitic elements. The transistors were modeled as BSIM3v3.2 models in both processes. Simulations of the static I/V characteristics together with their transconductance and drain conductance derivates showed a great difference in the models quality of the two processes. As it will be explained later, the higher order derivatives of the transconductance and drain conductance of the transistors are very important for the accuracy of the mixer intermodulation behavior. If these parameters are not well modeled, the intermodulation performance of the mixers cannot be foreseen. The simulation made on the 0.35 µm transistors showed discontinuities starting with the second derivative of the channel conductance. This poor approximation was the cause of inadvertences between the simulation and measurement results for the first realized IQ demodulator mixer, concerning the third order intercept point. On the other side, the model used for the 0.13 µm HCMOS process showed an exceptional accuracy of the simulated values of the I/V characteristics up to the fifth derivative of the channel conductance. This allowed a very good prediction the intermodulation behavior of the designed mixers.

The schematic of the IQ demodulator mixer is depicted in Figure 3.1. As already mentioned in the introduction, the matching network at the gates of the transistors was implemented only for the 0.35 µm BiCMOS process. This network acts as a band stop filter that provide a high impedance input at the LO frequency. Due to the resistive part of the integrated inductance, the band stop filter was not as efficient as desired. For this reason, in the 0.13 µm process, the filter was not used anymore.

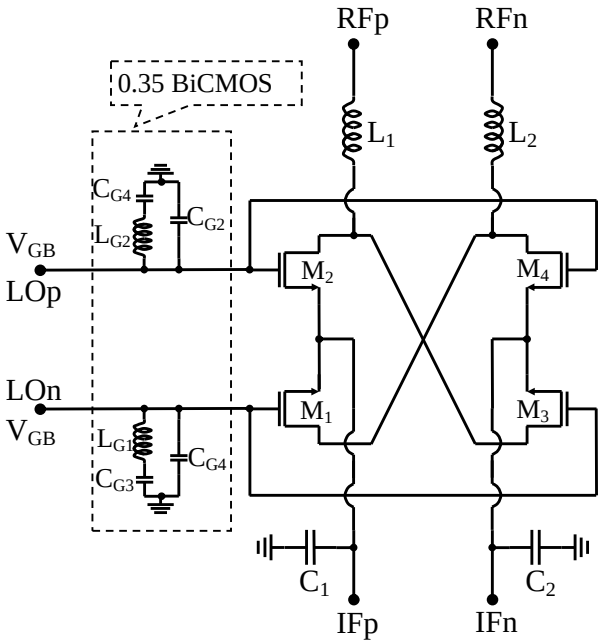


Figure 3.1. IQ Demodulator mixer schematic for the 0.35 µm BiCMOS and 0.13µm HCMOS processes

The entire circuit around the IQ demodulator mixer is represented in Figure 3.2. Single ended, 50 Ω referred power sources were used for the RF and LO ports. For the higher frequency ports (RF and LO) of the IQ demodulator mixer we have used S-parameter models of 180° hybrids as unbalanced-balanced transformers. These models are realistic S-parameter representations of the devices later used for on-waver measurements. In the IF port (0-100 MHz) we have also used an S-parameter model of a real coiled impedance transformer as used for the measurements. The bias-Ts were ideal models of DC block and DC feed elements taken from ADS.

The bulk ports of the mixer transistors were grounded, so the drain current shows only a bi-dimensional dependence (V_{GS}, V_{DS}), not being dependent on any bulk voltage. This measure has simplified the design of the mixers given the experience of the MESFET transistor designs in optimizing the mixer schematics.

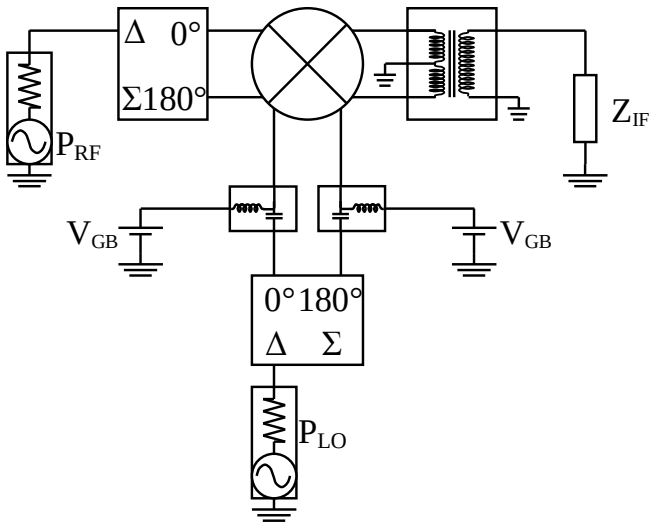


Figure 3.2. IQ demodulator mixer simulation bench

The sources of the transistors were also grounded with concern of the RF and LO signal through the RF coupling capacitances C_1 and C_2 on both IF branches (see Figure 3.1). The RF signal is injected into the transistors drains through the matching inductances L_1 and L_2. The value of these inductances was chosen in concordance with the input impedance of the common drains of the transistors as to match the RF input of the mixer to 50 Ω. The gate bias voltage V_{GB} was supplied to the gates at the same input lines as the LO signals. The separation between the RF and DC paths was realized before the circuit through some bias-Ts as depicted in Figure 3.2. The output impedance of the mixer depends on the transistor width and length. For the 0.35 µm mixer, an output impedance of 150 Ω was reached, fact that made necessary the use of a 3:1 impedance transformer at the IF port in order to realize the output matching. For the 0.13 µm IQ demodulator mixer, we were able, through proper optimization of the transistor dimension, to achieve an output impedance of 50 Ω in the IF ports, so another 1:1 transformer was used.

3.3. Layout Implementation

The mixer layouts were implemented using the Virtuoso tool from Cadence instead of ADS. This solution was imposed by the design kit HCMOS9GP that was better supported in Cadence than in ADS. Features like layout vs. schematic verification (LVS) and parasitic extraction were implemented for Cadence but not for ADS. However, the schematic optimization and post layout simulations were still made in ADS. The transfer of information between the two applications was possible using the RFIC Dynamic Link feature.

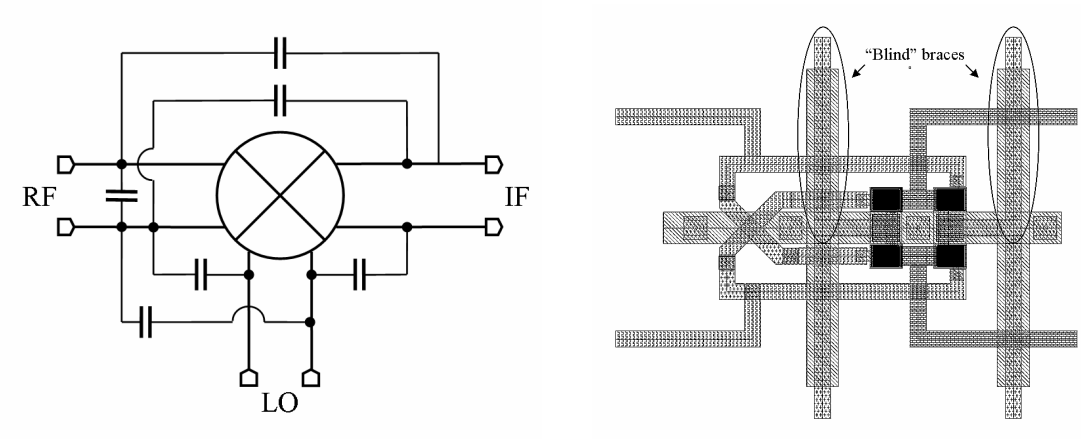


Figure 3.3. Capacitive couplings between the transmission lines (left) and methods of minimization with grounded shields and blind traces (right)

The layout design was done with special attention to the physical and geometrical symmetry. This condition guarantees a high level of isolation between the LO and RF/IF signals. The four transistors that make the kernel of the mixer were fused together in the middle of the chip. The transistor mismatch was minimized in this way, assuring again the symmetry of the mixed signals. The LO and RF signal routings are orthogonal to each other in order to prevent any on-chip magnetic coupling between the lines, although the magnetic on-chip coupling can be considered almost insignificant at used frequencies. Concerning the capacitive couplings between the LO and RF signals, grounded isolation surfaces were designed between all intersections of these signals.

To further avoid the capacitive coupling of the LO signal into the RF and IF ports, the intersections between these lines were replicated with some blind traces on the opposite polarity lines as depicted in Figure 3.3. The blind traces provide the same voltage potential as the signal lines although only the coupling currents flow through them. At the mixer output, through the 180° couplers, these leakage currents will destructively add and therefore the LO signal at the RF and IF outputs will be strongly attenuated.

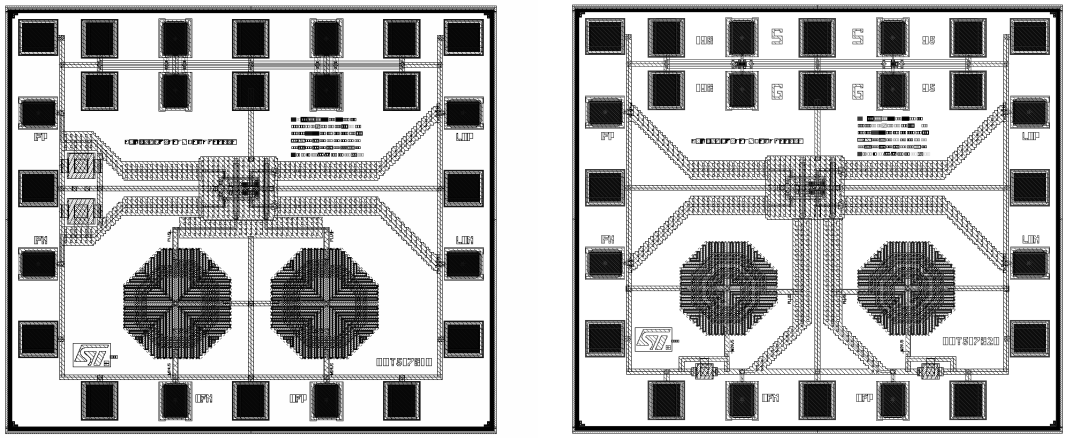


Figure 3.4. IQ demodulator mixer layout (left) and WLAN mixer layout (right)

The both mixers were realized using the above-described methods. Post layout simulations showed an important improvement in the port-to-port isolation, fact that validates these measures.

The mixer layouts are depicted in Figure 3.4. Each of them occupies a surface of about 1 mm^2 imposed by the pad ring. On the upper side of each mixer are test structures containing singular transistors of different dimensions for further tests and transistor characterization.

The four transistors of the mixers are identical, with a width of 95 µm for the IQ demodulator mixer (left in Figure 3.4) and 139 µm for the WLAN mixer (right in Figure 3.4). For both structures, the transistors have 12 fingers, which provide the best performance at the working frequency.

In the case of the IQ demodulator mixer, two supplementary capacitances were needed to filter out the higher frequency spurious components at the differential IF port. These capacitances have a value of 5.0 pF and a width of 50 µm. In order to maximize the transferred RF power at the RF port, two matching inductances with a value of 1.35 nH and 2.5 turns were also used.

For the WLAN Mixer, only the matching network at the differential RF port was needed. Therefore, a shunt LC tank was implemented in the layout, where the inductances have a value of 2 nH with 3.75 turns and the capacitances 1.8 pF.

3.4. Measurement Results

The characterization of the IQ demodulator mixer performance was made with direct "on-wafer" measurements, where the measurement probes were calibrated at the chip level with a calibration substrate. Mixer characterization includes the port impedance measurements, conversion loss, noise figure, saturation power, intermodulation behavior and port-to-port isolation. All these performance characteristics are of great importance concerning the overall receiver performance. For some measurements, the available LO power or the gate bias voltage V_{GB} was slightly varied in order to observe the sensitivity of the mixer to these parameters and to identify possible ways to optimize its performance.

Because the measurement process for the WLAN mixer was similar, only the IQ demodulator mixer will be extensively characterized. However, at the end of the chapter, a performance table of both of the mixers will be presented.

3.4.1. Measurement of the Port Impedances

The measurement bench for the port impedance measurements is depicted in Figure 3.5. As the LO port is known to be of high impedance, limited only by the C_{gs} capacitance, only the RF and IF ports were characterized as functions of either the available LO power or the gate bias voltage V_{GB}.

The differential impedances were measured as double single ended ports in order to eliminate the errors caused by the 180° couplers and IF transformer. During one measurement, all free output ports were closed with 50 Ω terminations. The available LO power was measured through a directional coupler as shown in Figure 3.5.

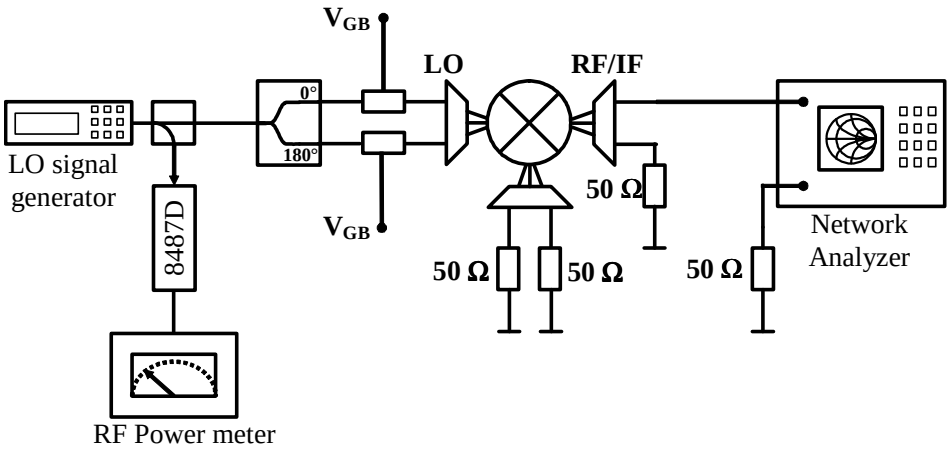


Figure 3.5. Port impedance measurement system

The measurement results are depicted in Figure 3.6.

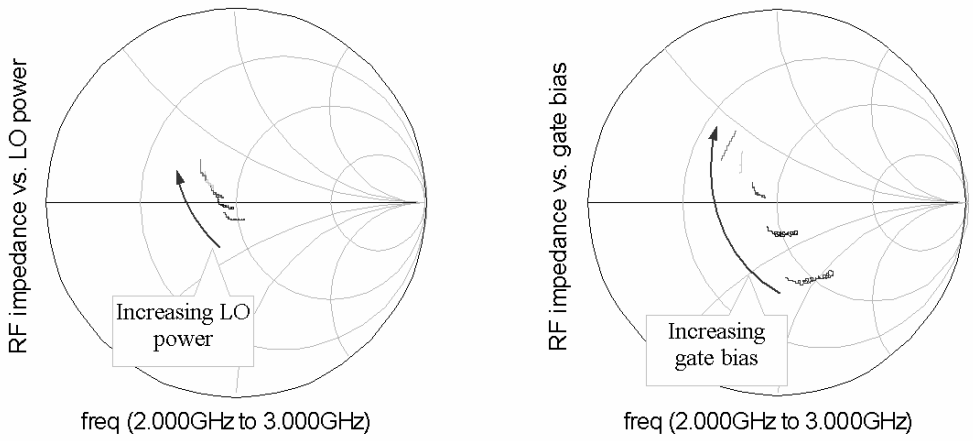


Figure 3.6. RF impedance vs. available LO power and gate bias, sweeps according to Table 3.1

Parameter	Value	Remarks
Frequency domain	[2…3] GHz	401 points
Available LO power sweep	[-4…4] dBm	5 points @ VG=3 V
V_{GB} voltage sweep	[0.1…0.5] V	5 points PLO=0 dBm

Table 3.1. Measurement parameters for RF port impedance

As can be observed, the mixer RF port impedance is more dependent on the V_{GB} bias voltage than on the available LO power. Anyway, at the middle values of both sweeps, which where also used in normal use (P_{LO}=0 dBm, V_{GB}=0.3 V), the RF port impedance is 50 Ω over the entire frequency domain.

The same measurements are made at the IF port for the frequency domain depicted in Table 3.2.

The measurement results are depicted in Figure 3.7.

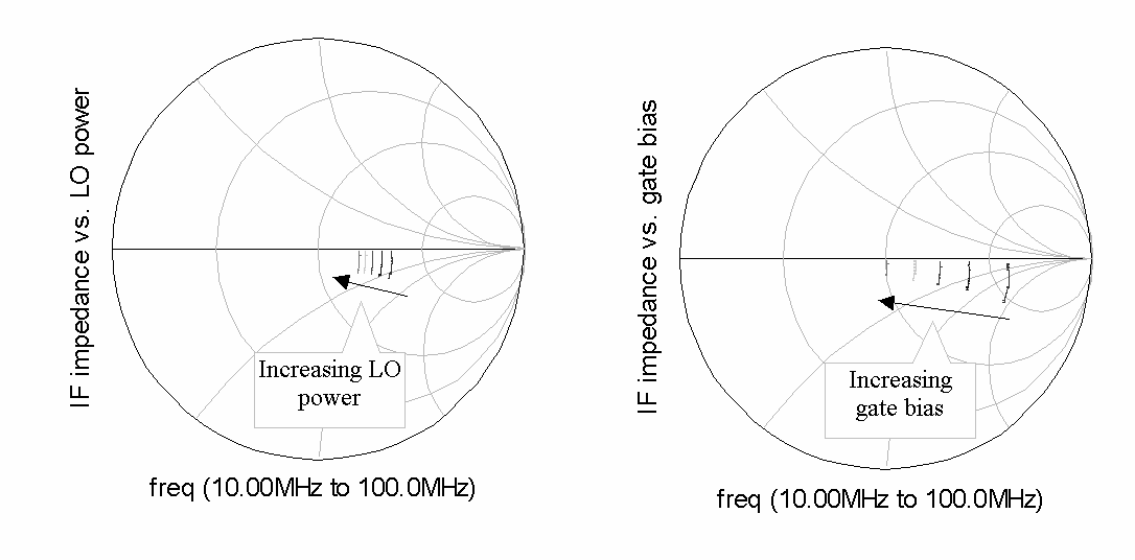


Figure 3.7. IF impedance vs. available LO power and gate bias, sweeps according to Table 3.2

Parameter	Value	Remarks
Frequency domain	[10…100] MHz	401 points
Available LO power sweep	[-4…4] dBm	5 points @ VG=3 V
V_{GB} voltage sweep	[0.1…0.5] V	5 points PLO=0 dBm

Table 3.2. Measurement parameters for IF port impedance

Here is observed a stronger dependence on the gate bias voltage then on the available LO power, which means that the output impedance of the transistors is more dependent on the middle value of the gate voltage then on the amplitude of the large signal present at the LO port. Anyway, the impedance is slightly higher than 50 Ω, but with very small reactive components which shows a good optimization of the transistor gate width.

3.4.2. Conversion Loss Measurements

The measurement system for this parameter is depicted in the Figure 3.8. The available LO and RF power levels are observed during the measurement, which assure more reliable and repeatable results. The blocks 8482A, 8487D and 8487A are power sensors that together with the power meters show the signal level at each port. The power sensors are different concerning the sensitivity and the working frequency. The signal level at the RF and LO ports are measured by extracting the available power through a directional coupler. At the RF port we have also used an attenuator in order to diminish the strength of the reflected power at the source. The losses introduced by these components together with the losses from cables and measurement probes are de-embedded from the conversion loss determination.

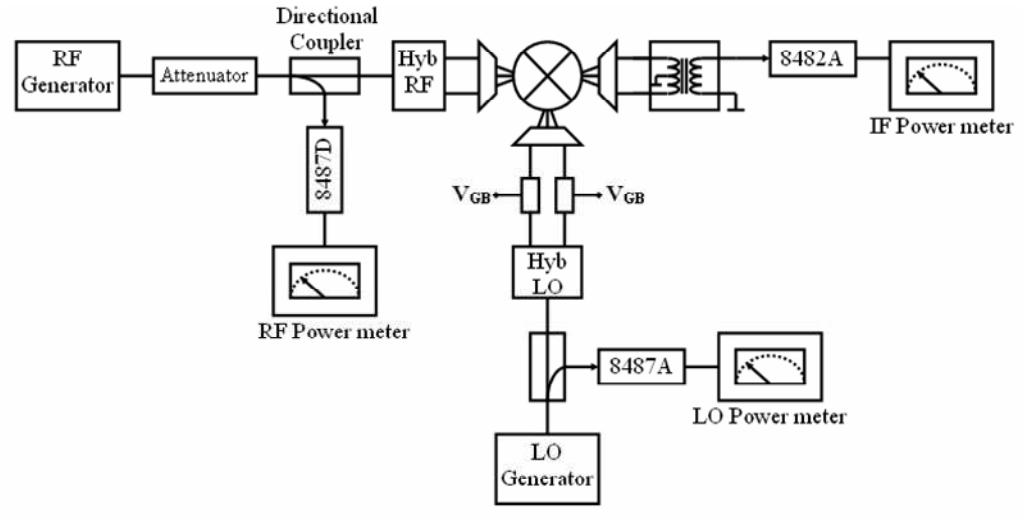


Figure 3.8. Conversion loss measurement system

The variation of the LO power with the frequency was also extracted from the conversion loss. This procedure of de-embedding the LO was possible because we have also measured the available LO power for all measured points.

As listed in Table 3.3 the measurements are made at a constant output frequency of 40 MHz, which is relatively high for UMTS or WLAN baseband signals but still relevant concerning the low frequency output domain. The available LO power and the gate bias voltage V_{GB} were chosen as optimum values given by the precedent measurements. The RF power was chosen well below the simulated saturation point of the mixer but high enough to provide accurate measurements results.

Parameter	Value	Remarks
RF frequency domain	[2…3] GHz	21 points
LO frequency domain	[1.96…2.96] GHz	21 points
IF frequency	40 MHz	constant
RF power	-20 dBm	
Available LO power	0 dBm	
Gate bias voltage V_{GB}	0.3 V	

Table 3.3. Measurement parameters for conversion loss

The conversion loss performance is depicted in Figure 3.9. The mean value of 5.7 dB is identical with the simulated conversion loss for this circuit. Over the entire frequency range of 1 GHz, the conversion loss variation is less than 0.5 dB, which simplifies the signal path optimization in the reconfigurable system design.

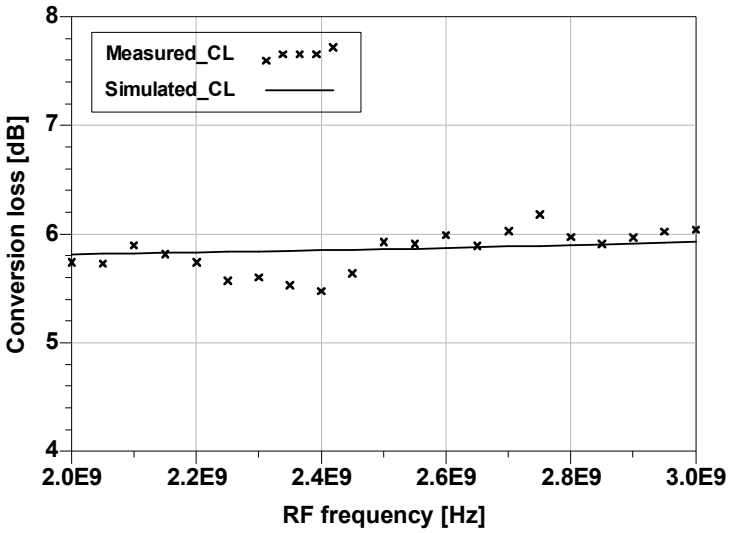


Figure 3.9. Measured conversion loss vs RF frequency, sweep parameters according to Table 3.3

3.4.3. Noise Figure Measurements

The noise figure measurement was made using a wide band noise source at the RF input port and measuring the noise level at the IF port with a noise figure meter. In order to increase the measurement sensitivity, a low noise amplifier between the mixer and the noise figure meter has amplified the weak output signal as depicted in Figure 3.10.

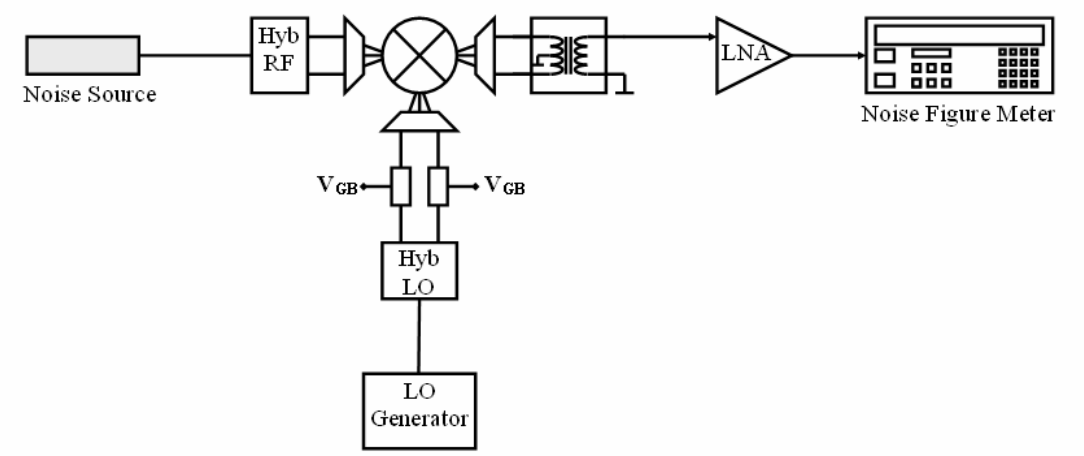


Figure 3.10. Noise figure measurement system

The measurement parameters are enumerated in Table 3.4 below:

Parameter	Value	Remarks
RF frequency domain	[2…3] GHz	81 points
LO frequency domain	[1.99…2.99] GHz	81 points
IF frequency	10 MHz	constant
Available LO power	0 dBm	
Gate bias voltage V_{GB}	0.3 V	

Table 3.4. Measurement parameters for noise figure

In the calibration stage, the measurement chain without the mixer was evaluated in order to extract the measurement set-up induced noise from the final result. The mixer converts the noise from both RF and image frequencies, so the single-side band noise figure will be about 3 dB lower than the result displayed by the noise meter. The result shown in Figure 3.11 is relative constant over the entire frequency domain and has a value of approx. 6.5 dB.

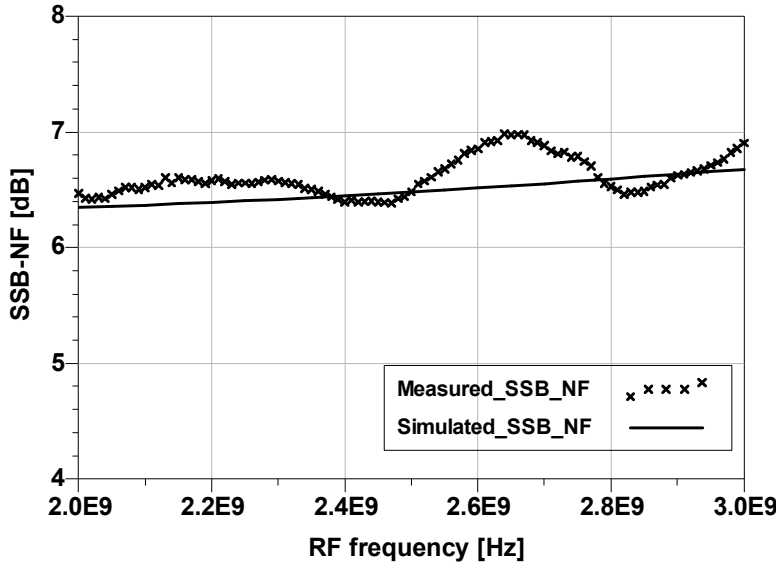


Figure 3.11. Single side-band noise figure and the conversion loss over the RF frequency domain, sweep parameters according to Table 3.4

3.4.4. Compression Point Measurements

Measurement parameters:

Parameter	Value	Remarks
RF frequency	2.35 GHz	constant
LO frequency	2.31 GHz	constant
IF frequency	40 MHz	constant
RF power sweep	[-10…10] dBm	21 points
Available LO power	0 dBm	
Gate bias voltage V_{GB}	0.3 V	

Table 3.5. Measurement parameters for compression points

The compression point measurement was made in the same way as the conversion loss, this time varying the RF power at a constant RF and LO frequency. The same de-

embedding methods were used for the compression point measurement. We have made the measurement at different RF working frequencies, but the result remained unchanged.

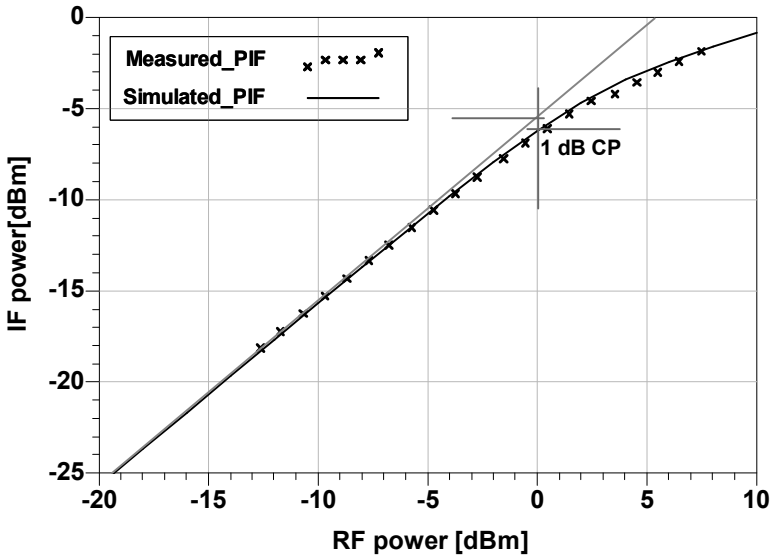


Figure 3.12. Compression point measurement, sweep parameters according to Table 3.5

The input 1 dB compression point was measured for the given conditions at 0 dBm input (RF) power. This result coincides with the simulation too.

3.4.5. Intermodulation Measurements

For intermodulation measurements, a slightly different measurement system with two RF signal generators was used as depicted in Figure 3.13. Because we had to measure the power level at an intermodulation product frequency, also in a very narrow frequency band, we used a spectrum analyzer to measure the intermodulation power level instead of the power meter.

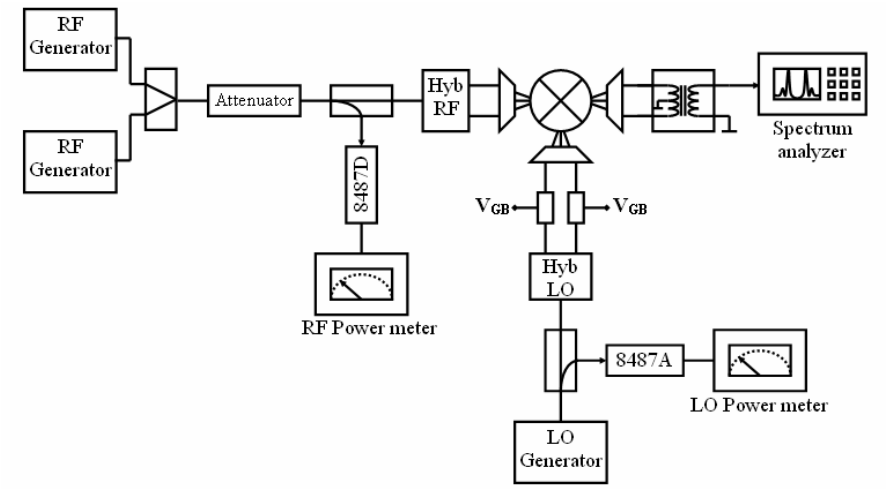


Figure 3.13. Noise figure measurement system

As showed in Figure 3.14, a third order intercept point of 10 dBm input power and a second order intercept point at 65 dBm input power was measured under the conditions listed in Table 3.6.

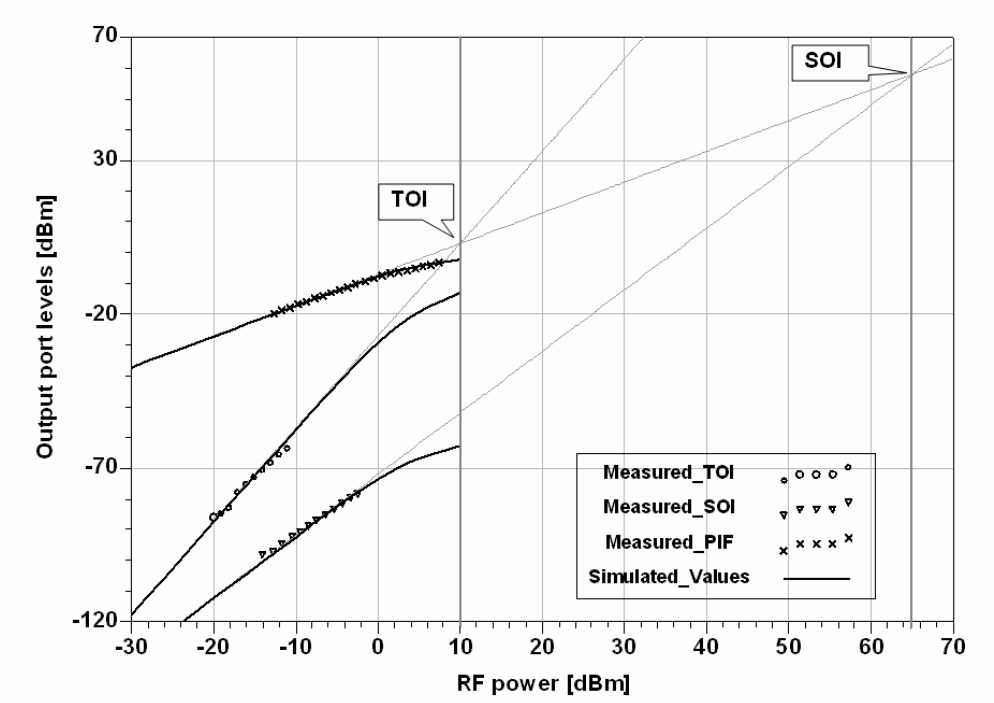


Figure 3.14. Intermodulation products measurement, sweep parameters according to Table 3.6

Parameter	Value	Remarks
RF frequency 1	2349.9 MHz	constant
RF frequency 2	2350.1 MHz	constant
LO frequency	2310 MHz	constant
IF frequency 1	39.9 MHz	constant
IF frequency 2	40.1 MHz	constant
3^{rd} order IM frequency 1	39.7 MHz	constant
3^{rd} order IM frequency 2	40.3 MHz	constant
2^{nd} order IM frequency	200 KHz	constant
RF total power sweep	[-20…0] dBm	
Available LO power	0 dBm	
Gate bias voltage V_{GB}	0.3 V	

Table 3.6. Measurement parameters for intermodulation products

The dependence of the third order intercept point on the available LO power was also measured. The measurement system is the same as the one depicted in Figure 3.14. For the measurement, we have swept the available LO power in the [-7.5…7.5] dBm domain and kept all other parameters as defined for the precedent measurement.

Figure 3.16 shows the dependence of the input TOI on the RF frequency. For this measurement we have swept the RF frequency (both branches concomitantly) in the [2000…3000] MHz range and measured the input TOI for each frequency point.

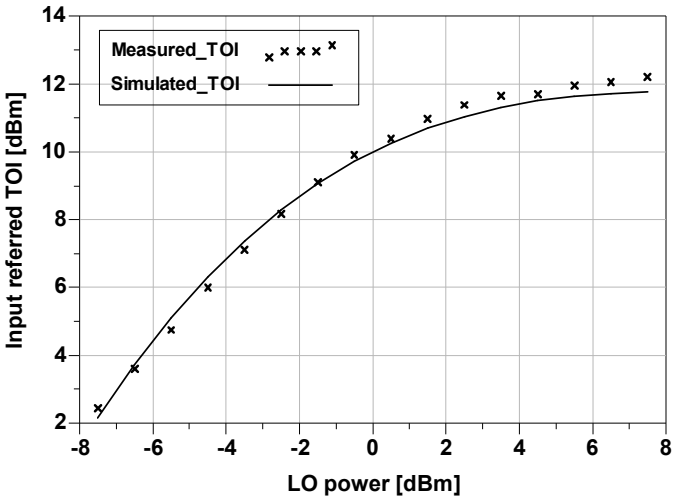


Figure 3.15. Input TOI versus the available LO power, measurement parameters according to Table 3.6, excepting LO power swept by [-7.5 … 7.5] dBm and constant RF power at -20 dBm

The LO frequency was also swept concordantly in order to keep the intermediate and intermodulation products constant around 40 MHz as defined for the first intermodulation measurement. All other parameters remain unchanged. As we can see, the input TOI remains relatively constant with the frequency, as does the conversion loss.

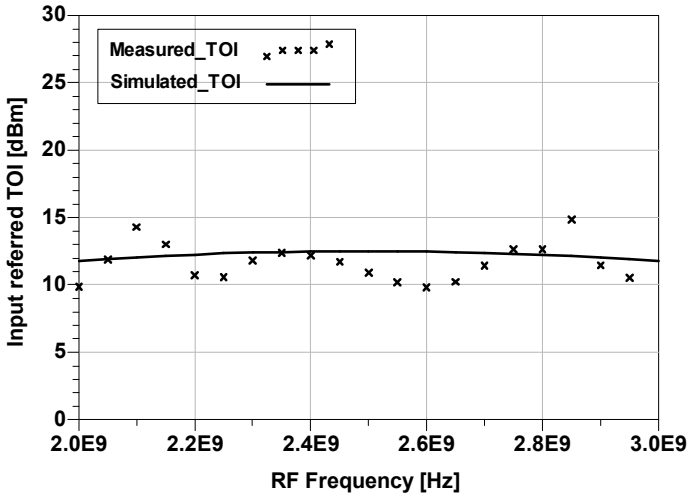


Figure 3.16. Input TOI versus the RF frequency, parameters according to Table 3.6, except the RF frequency swept for both tones by [2000 … 3000] MHz at a RF power of -20 dBm

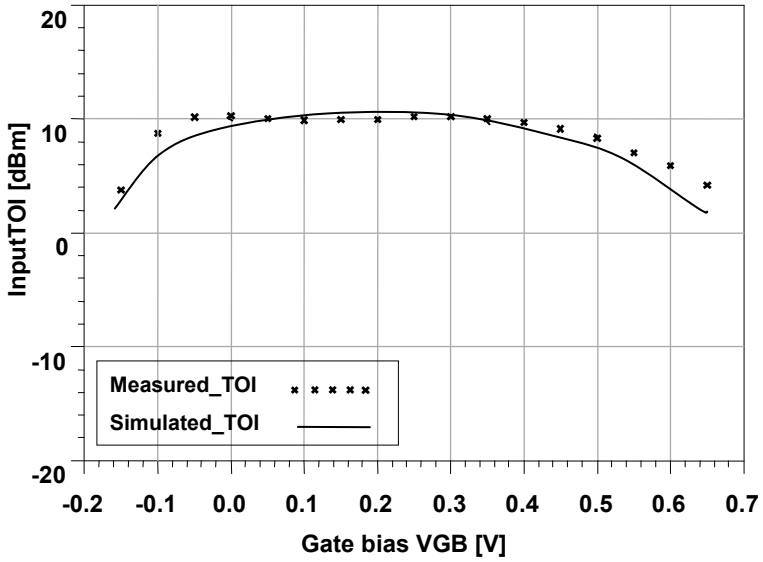


Figure 3.17. Input TOI versus the gate bias $V_{GB,}$ parameters according to Table 3.6, except the gate Bias swept by [-0.2 … 0.7] V at a RF power of -20 dBm

Figure 3.17 shows the dependence of the input third order intercept point of the gate bias. Here, we swept the gate bias V_{GB} in the range [-0.15…0.65] V and measured the input TOI for each of these points. All other parameters remained unchanged as defined at the beginning of this subchapter. We can observe that the ITOI is not critical dependent from the gate bias in a relative large voltage range (between 0.05 and 0.4 V) but is strongly influenced outside this voltage range.

3.4.6. Port Isolation Measurements

We have measured the leakage of the LO signal in RF and IF ports. The measurements were done at large signal (0 dBm LO power). The measurement system is depicted in Figure 3.18 and show the leakage measurement from LO to RF port. The IF port is terminated in 50 Ω. The same measurement system was used also for the LO-IF leakage. The

isolation results are strongly influenced by the amplitude and phase imbalance of the hybrids and we expect superior isolation values for the mixer alone.

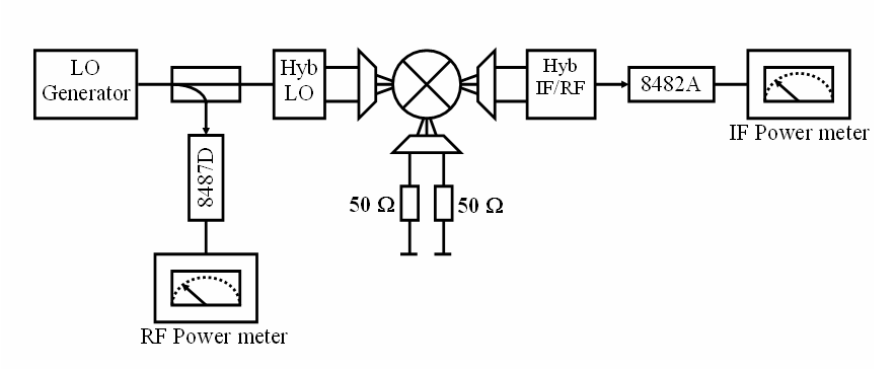


Figure 3.18. Noise figure measurement system

Parameter	Value	Remarks
LO frequency	[2…3] GHz	21 points
Available LO power	0 dBm	
Gate bias voltage V_{GB}	0.3 V	

Table 3.7. Measurement parameters for LO power leakage at the RF and IF ports

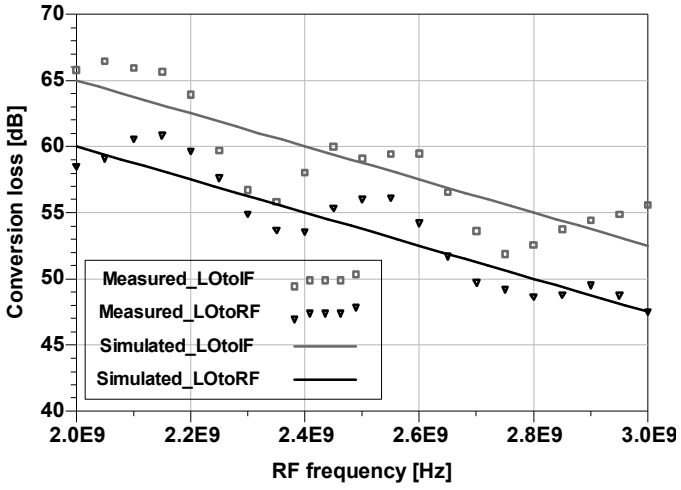


Figure 3.19. LO-IF and LO-RF port isolations, measurement parameters according to Table 3.7

Parameter	IQ Demodulator	WLAN mixer
RF frequency [MHz]	[2000…3000]	[5000…6000]
LO frequency [MHz]	[2000…3000]	[2000…3000]
IF frequency [MHz]	[0…30]	[2000…3000]
Available LO power [dBm]	0	0
Gate bias voltage V_{GB} [V]	0.3	0.3
Conversion loss [dB]	~5.7	~7
Single sideband noise figure [dB]	~6.5	~8
1 dB compression point [dBm]	0	0
Input third order intercept point [dBm]	10	10
Input second order intercept point	65	60
LO-IF isolation [dB]	>55	>55
LO-RF isolation [dB]	>50	>50

Table 3.8. Measurement results for IQ demodulator mixer and the WLAN mixer

The measurement values depicted in Figure 3.19 show a very good isolation between the LO and RF and IF ports, respectively. These values reflect the measures taken with respect to the layout symmetry and signal isolation, and demonstrate their efficiency.

3.5. Conclusions

The extensive measurements have demonstrated that the performance of a passive mixer is high enough in order to fulfill the requirements of a complex receiver as the one presented in this document. A summary of measurement results is presented in Table 3.8 for both mixers.

Chapter 4.

Intermodulation Analysis in Resistive FET Mixers

4.1. Introduction

The intermodulation distortion and the noise interference are constantly addressed subjects in the design process of a receiver front-end. The intermodulation distortion is becoming even more important with the development of multi-tone digital telecommunication systems demanding very high dynamic range amplifiers, mixers and switches. Since the field effect transistors are increasingly common in all these active blocks, nonlinear characterization of these devices has become an important issue.

The empirical models usually adopted to represent FET devices cannot be used to produce accurate intermodulation distortion (IMD) calculations, although they can predict gain or conversion loss very well for different applications. They are usually designed to reproduce the FETs static current-voltage (I/V) and charge-voltage (Q/V) characteristics, when in fact, as it will be demonstrated; the derivatives of those characteristics are dominant in determining the intermodulation levels. Numerical derivation of the drain current after its measurement is generally impractical because the FETs drain current is very small and is often lost its nonlinearity within measured tolerances.

In the last decade, a continuous effort was directed toward an accurate model to characterize the intermodulation distortion. Most of the models reproduce the drain current and its derivatives up to at least the third order with respect to the gate and drain voltages in the saturated region, although they do not perform well in the linear region or with varying load conditions ([61] – [63]). Others, e.g. [65] directly model the transistor nonlinear conductances and capacitances instead of the drain current and charge, using special measurement procedures in order to increase the model precision. A few number of publications, however offer models specifically fitted for the cold FET operation, oriented on resistive mixer applications ([66], [69] and [71]).

The accuracy of the intermodulation distortion evaluation depends not only on the chosen transistor model but also on the nonlinear analysis technique used to characterize the device. Depending on the direction wherefrom the analysis is made – analytical or numerical, two important methods can be identified: Volterra series method and the harmonic balance method.

The Volterra series method is an analytical procedure that extends the Taylor series approximation method to dynamic systems. By substituting the circuit's nonlinearities by Taylor series approximations of nth degree, it gives a solution to that nth-order problem by recursively solving n times the same linear circuit. Therefore, and contrary to any other nonlinear method, it provides closed-form expressions for the sought nonlinear solutions. Behaving this way, it offers detailed qualitative information on the system's properties, enabling analysis, performance optimization, and design tasks. Since it can operate entirely in the frequency-domain, it imposes no restrictions on the excitation signal spectrum, making it the ideal method for multi-tone distortion analysis.

Despite these benefits, Volterra series suffers from an important disadvantage: it cannot be applied to strongly nonlinear problems. Actually, either because the series simply does not converge or requires an intractable number of terms for required accuracy, Volterra series is usually limited to quite smooth nonlinearities subject to small amplitude signals. These are the so-called mildly nonlinear problems. In practice, the series' range of applicability

becomes restricted to signal levels comfortably behind the 1-dB compression point. Moreover, even in the case of a mildly nonlinear circuit, although Volterra series can handle the nonlinear effects pressed onto the signal, it cannot cope with the strong nonlinearities usually associated with the time-variant quiescent point calculation as is the case of the LO excitations in mixers. For example, despite Volterra series being the best method to predict distortion behavior of mixers, it can only be applied after the local oscillator pumping has been determined by some other nonlinear analysis technique. Finally, it should be also stressed that only the engineer's intuition and experience can tell him when the series' results are no longer useful, since there is no such indication available from the method. That is, one may perform a power sweep simulation up to a stimulus level where the series no longer produce any useful results without the slightest error or warning [72].

The harmonic balance analysis method is a numerical iterative method that does not provide symbolic expressions for the solutions. Although it is classified as a frequency-domain technique, because it solves the circuit for the Fourier coefficients of the voltages and currents, it still requires time domain calculations. Actually, a harmonic balance engine relies on balancing the harmonic levels of node currents arising from the circuit's linear-dynamic and nonlinear-memory less elements. Having an estimate of the node voltage, it must find a way to determine those levels in the linear (simply by admittance representation) and nonlinear elements. For the nonlinear elements, the HB machine converts the voltage into time-domain, using the inverse discrete Fourier transform, computes the nonlinear algebraic currents in a time sample per time-sample basis, and then converts again this time-domain current back into the frequency-domain using the DFT. The harmonic balance method is therefore, mainly constrained by that Fourier transform. The handled signals must be periodic and their spectra truncated up to a convenient number of harmonics. If those two conditions are not met, the results' accuracy becomes severely compromised by spectral leakage or aliasing errors. Moreover, if the number of harmonics is too small, then convergence problems may be faced and the HB routine may never reach a solution. Nevertheless, a great research effort has been continuously put into the HB method for the last 20 years, which permitted to overcome some of these limitations. With

these modifications, the harmonic balance becomes indeed a very powerful tool even for distortion analysis. There are various commercially available nonlinear simulators using this method, among them also the ADS from Agilent, which was used to design the presented mixers.

Concerning the resistive mixer, its mechanism can be shortly formulated as a voltage controlled channel conductance whose value varies with the LO frequency and which is loaded with the RF signal voltage. The current that flows through this time-variant conductance will have frequency components not only at RF and LO frequencies but also at combinations of these. Distortion analysis in mixers is significantly more complex than in amplifiers, due to the time-varying nature of the circuit. The RF signal is treated as a small deviation of the large-signal, time-varying drain current which is controlled by the LO signal. Hence, the intermodulation products can be fond by a Volterra (or Taylor if the system is considered memoryless) series expansion using the LO voltage as a central "point". The resulting series coefficients are time-varying ([61]). The frequency spectrum of the mixer output is formulated as: $f_{out}=\pm m \cdot f_{LO} \pm n \cdot f_{RF}$. For a RF input signal which contain two harmonics at the frequencies f_{RF1} and f_{RF2}, the nonlinearity of the drain conductance will produce mixing products at frequencies like: $f_{out}=\pm f_{LO}-2f_{RF1}+f_{RF2}$ known as the third order intermodulation product. This frequency is very close to the intermediate frequency IF and cannot be rejected producing self-interference or adjacent channel interference in multitone modulated signals like OFDM.

The qualitative analysis of the resistive mixer will begin with the simple one-transistor mixer topology presented in Figure 2.7. Because of the normally much lower RF signal amplitude compared with the LO driving, the mixer can be analyzed as a time-varying mildly non-linear system. For such systems, the conversion matrix method for the analysis of the large signal non-linearities followed by a Taylor series approximation to characterize the small signal distortions will be derived.

4.2. Large and small signal analysis for resistive mixers

A typical cold FET nonlinear equivalent circuit is shown in

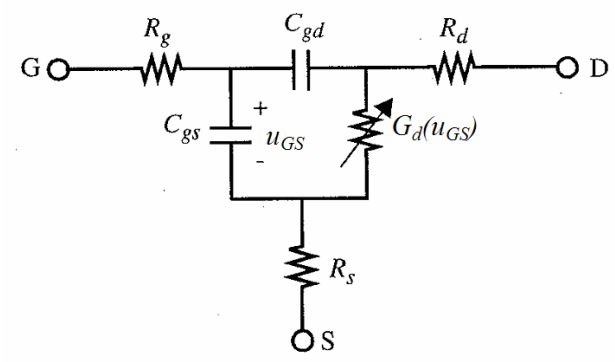


Figure 4.1. The most nonlinear element in this equivalent circuit is the channel conductance G_d. Frequency mixing occurs due to its functional dependence on the gate voltage.

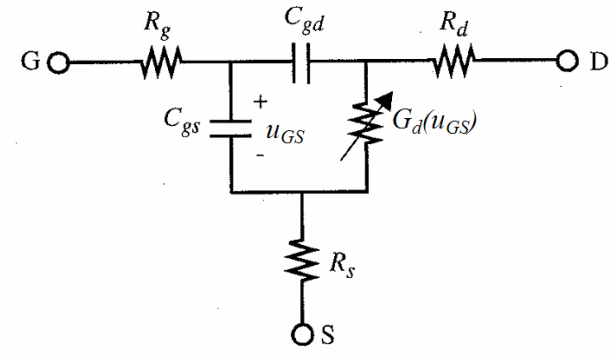


Figure 4.1. A typical FET nonlinear equivalent circuit with no drain bias.

If the capacitances C_{gs} and C_{gd}, in the equivalent circuit of the transistor, would be considered non-linear dependent on the gate voltage, the transistor should be analyzed as a mildly-nonlinear, time-variant, *dynamic* system. The nonlinear transfer function of these systems is much more complex than the one for memoryless systems. The Taylor series expansion applied later to the time-variant drain conductance must, in such case, be generalized to a Volterra series ([59], [72]). It is common knowledge that for the mildly-nonlinear *memoryless* system, it is enough to characterize the systems impulse response in

order to determine the output of the system for any input signal [67]. A power series expansion of the impulse response (or of the harmonic excitation if the analysis is made in the frequency domain) will lead to the analytical approximation of the transfer function of such a system. The impulse response characterization is not sufficient anymore in the case of *dynamic* systems. One must characterize the system response to one, two and up to *n* independent impulses and build a system of ordinary differential equations which are expandable with Taylor series [73]. This process can be very laborious and unnecessary for the understanding of the resistive mixer behavior. Therefore, in the following analysis, the nonlinear capacitances were considered linear and the nonlinear circuit was treated as a *memoryless* one.

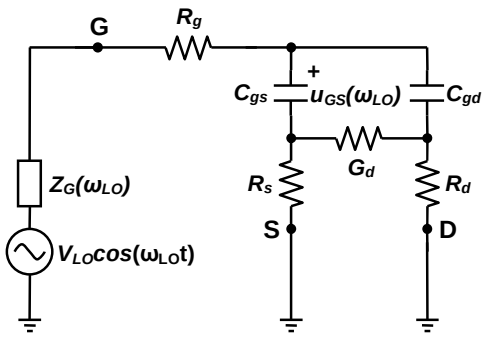


Figure 4.2. Large signal equivalent circuit of the resistive gate mixer

The first step of the analysis is the separation of the large signal, which forces the time variation of the drain conductance from the small signal, which introduces only the mildly non-linear behavior. In this scope, only the LO signal is applied to the gate, and the drain is connected to the ground. The large signal equivalent circuit is depicted in Figure 4.2.

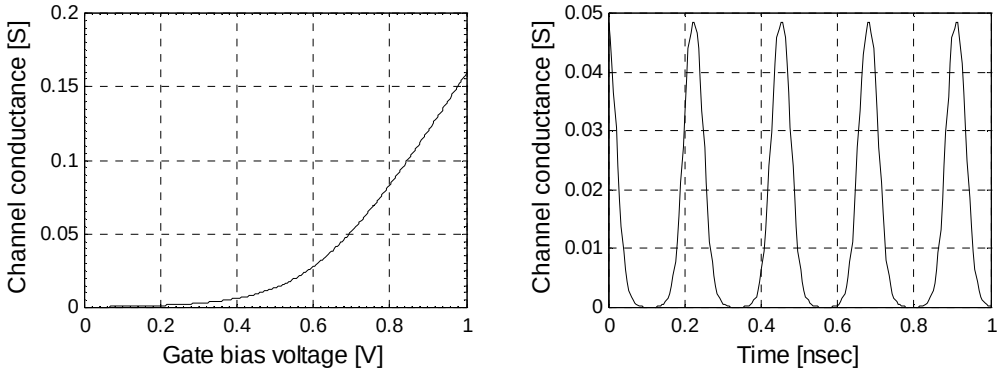


Figure 4.3. Measured channel conductance vs. gate bias voltage (left) and its time variation (right) for a harmonic excitation of a HCMOS transistor gate with L=0.13 µm and W=40 µm

Applying a large harmonic signal at the transistor gate, will produce a periodic variation of the channel conductance of this transistor. The nonlinear transfer characteristic G-V for the particular case of the HCMOS transistor in 0.13 µm technology used for the resistive mixer described in the third chapter is depicted in Figure 4.3. The harmonic signal applied at the transistor gate is of very low frequency (several MHz) in order to minimize the parasitic effects due to the reactance characteristics of the gate-source junction.

In order to determine the frequency dependent system response of the circuit, the voltage at the gate-source junction $u_{GS}(t)$ must be determined for the circuit excited only with the harmonic gate voltage of LO frequency and the LO bias ($u_{LO}(t)=U_{LO}+u_{lo}cos(\omega_{LO}t)$). This determination equals the solution of the quiescent point equation in non-linear amplifiers. In the mixer case, this quiescent point is composed by the voltage and currents forced by the local oscillator, or pumping signal, plus any possible dc value. The methods of determination of the time variant quiescent point are various, but the most suitable seems to be the non-linear numerical iteration methods like Newton-Raphson. The method is extensively described in [72] and will not be further detailed here.

The next step after the time variant quiescent point solution was found is the determination of the time variation of the channel conductance. This step is very simple if the channel

conductance variation with the LO voltage as presented in Figure 4.3 is known and mathematically modeled. This variation is surely periodical as the LO signal, so it can be expressed as a Fourier series expansion with known G_{d_k} coefficients:

$$g_D\left[\hat{u}_{GS}(t)\right] = \sum_{k=-\infty}^{\infty} G_{d_k} e^{jk\omega_{LO}t}, \qquad 4.1$$

Where: g_D – channel conductance variation with the LO harmonic excitation,

G_{d_k} – frequency conductance coefficient of the Fourier series,

ω_{LO} – frequency of the LO signal.

The equivalent circuit presented in Figure 4.4 can be adopted if the transistor is excited with the small signal of RF frequency applied at the drain and the channel conductance exhibit a frequency dependent value as expressed in (4.1).

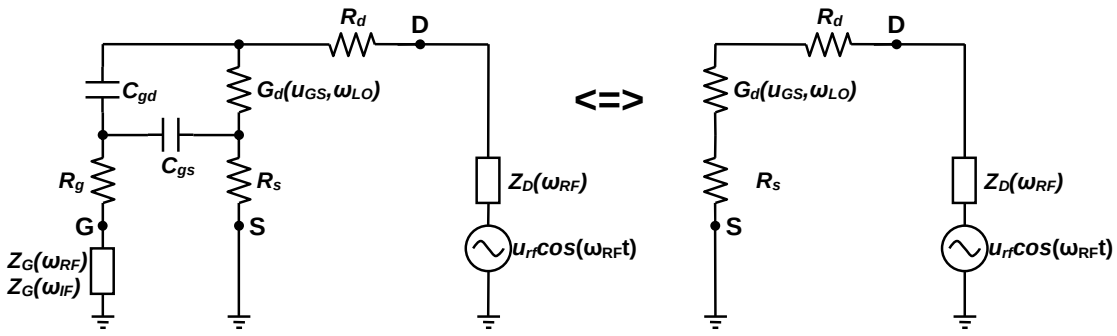


Figure 4.4. Small signal equivalent circuit of the resistive gate mixer

When a small-signal single-tone voltage at the frequency ωRF is applied at the channel conductance, currents and voltages are generated in the circuit at all $k{\cdot}\omega_{LO}+\omega_{IF}$ frequencies, were ω_{IF} are the frequencies closest to DC arising from direct down-conversion of the

RF excitation. At each of these frequencies, phasors represent these voltages and currents. The sum of these voltage phasors on the channel conductance is:

$$\hat{u}_{DS}(t) = \sum_{k=-\infty}^{\infty} U_{ds_k} e^{j(k\omega_{LO}+\omega_{IF})t}, \qquad 4.2$$

Where: $\hat{u}_{DS}(t)$ – total small-signal voltage on the time varying conductance,

U_{ds_k} – voltage component at the mixing frequency $k\omega_{LO+}\omega_{IF}$,

ω_{LO} – frequency of the LO signal.

ω_{IF} – frequency of the IF signal.

The sum depicted in 4.2 is not a Fourier series but a sum of phasor components. Expressed in this way, $\hat{u}_{DS}(t)$ is complex, not a real function of time, and the circumflex is used to emphasize this point. For the currents, the same holds true. The drain current can be therefore expressed as:

$$\hat{i}_D(t) = \sum_{k=-\infty}^{\infty} I_{d_k} e^{j(k\omega_{LO}+\omega_{IF})t}, \qquad 4.3$$

Where: $\hat{i}_D(t)$ – total small-signal current through the time varying conductance,

I_{d_k} – current component at the mixing frequency $k\omega_{LO}+\omega_{IF}$.

ω_{LO} – frequency of the LO signal.

ω_{IF} – frequency of the IF signal.

Although the summations in (4.2) and (4.3) are over an infinite number of terms, the circuit will only produce a limited number of mixing products with significant amplitudes. The summation will be further limited to $k \in [-N,N]$.

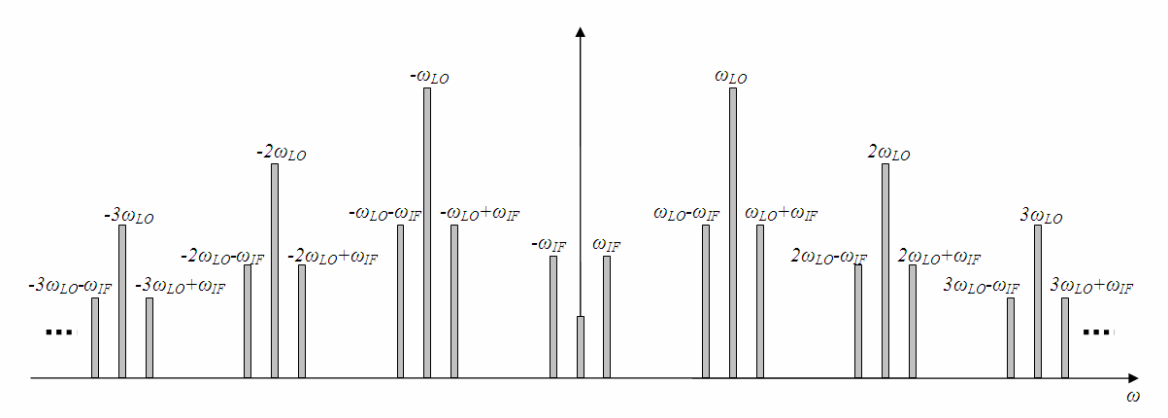


Figure 4.5. Complete spectrum of voltage and currents in the circuit for *N*=3

Figure 4.5 represents the entire spectrum of frequencies, which are generated in the circuit considering the RF signal so small in the amplitude that the mixer can be considered a *linear* time varying device. The intermediate frequency ω_{IF} is preferred over the ω_{RF} for simplicity.

When the RF excitation is small enough, the currents and voltages on the drain conductance will contain no higher harmonics of the RF frequency. If the amplitude of the RF signal increases, the mixer will exhibit a *mildly non-linear* behavior. Concomitantly, higher harmonics of the RF frequency will be generated in combination with the higher harmonics of the LO frequency. Considering for the moment that this is not the case, one can express the relation between the current and the voltages as related by the drain conductance:

$$\hat{i}_D(t) = g_D[\hat{u}_{GS}(t)] \cdot \hat{u}_{DS}(t), \qquad 4.4$$

Substituting the equations (4.2) and (4.3) into (4.4) gives the relation:

$$\sum_{l=-N}^{N} I_{d_l} \cdot e^{j(l\omega_{LO}+\omega_{IF})t} = \sum_{\mu=-N}^{N} \sum_{\nu=-N}^{N} G_{d\mu} \cdot U_{ds\nu} \cdot e^{j((\mu+\nu)\omega_{LO}+\omega_{IF})t}, \qquad 4.5$$

Separating the terms at the same frequency on each side and expressing them in matrix form gives:

$$\begin{bmatrix} I_{-N} \\ I_{-N+1} \\ \vdots \\ I_{-1} \\ I_0 \\ I_1 \\ \vdots \\ I_{N-1} \\ I_N \end{bmatrix} = \begin{bmatrix} G_0 & G_{-1} & \cdots & G_{-N} & G_{-N-1} & \cdots & G_{-2N} \\ G_1 & G_0 & \cdots & G_{-N+1} & G_{-N} & \cdots & G_{-2N+1} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ G_{N-1} & G_{N-2} & \cdots & G_{-1} & G_{-2} & \cdots & G_{-N-1} \\ G_N & G_{N-1} & \cdots & G_0 & G_{-1} & \cdots & G_{-N} \\ G_{N+1} & G_N & \cdots & G_1 & G_0 & \cdots & G_{-N+1} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots \\ G_{2N-1} & G_{2N-2} & \cdots & G_{N-1} & G_{N-2} & \cdots & G_{-1} \\ G_{2N} & G_{2N-1} & \cdots & G_N & G_{N-1} & \cdots & G_0 \end{bmatrix} \cdot \begin{bmatrix} U_{-N} \\ U_{-N+1} \\ \vdots \\ U_{-1} \\ U_0 \\ U_1 \\ \vdots \\ U_{N-1} \\ U_N \end{bmatrix}, \qquad 4.6$$

In the above equation, the indexes "*d*" and "*ds*" were omitted from the currents, conductances and voltages to facilitate the reading. The terms in the two dimensional matrix are the Fourier series components of the conductance waveform between DC and $2N^{th}$ harmonic.

Currents and voltages at the same frequency are related by G_0, the DC component of the Fourier series, which is obviously a real component. All other conductance components can be complex values. The matrix in equation (4.6) is called the *conversion matrix* of the time varying conductance.

One can recognize a clear regularity in the position of the terms of the conversion matrix ***G***. They are all located as if the matrix was filled by simply horizontally shifting to the right the *4N+1* vector [G_{2N} G_{2N-1} … G_0 … G_{-2N+1} G_{-2N}] and retaining only the middle 2N+1 positions. A matrix in which the elements verify the relation $a_{ij}=t_{i-j}$, where the t_{i-j} are the elements of a line vector, as is the case of ***G***, is called a Toeplitz matrix and can be used to represent a linear convolution by a matrix-vector product.

Linking the conversion matrix formalism with the right side equivalent circuit in Figure 4.4, we can now write the global relationship of the drain current for all involved frequencies:

$$\mathbf{I_D} = \mathbf{G_d} \cdot \mathbf{U_{ds}} \left[\mathbf{1} + \mathbf{G_d}\left(\mathbf{R_d} + \mathbf{R_s} + \mathbf{Z_{d_{RF}}}\right)\right]^{-1}, \qquad 4.7$$

where all linear elements of the circuit are expressed as diagonal matrixes with the values at each frequency written on the main diagonal. Solving this system of equations, one can estimate the conversion loss of the mixer and all other terms implying superior harmonics of the LO signal. Still, the intermodulation behavior of the mixer is impeded by the assumption that the transistor is linear concerning the RF excitation. This assumption will be abandoned in the next subchapter, the transistor being considered as having a *mildly nonlinear* dependence on the RF excitation.

4.3. Mixer Small-Signal Distortion Analysis

As stated before, the resistive mixer is principally a voltage controlled (time variant) conductance. The current that flows through this conductance was considered linearly dependent on the drain-source voltage. However, as one can observe in the V-I diagram in Figure 4.6, this linearity condition is limited for small amplitudes of the input voltage.

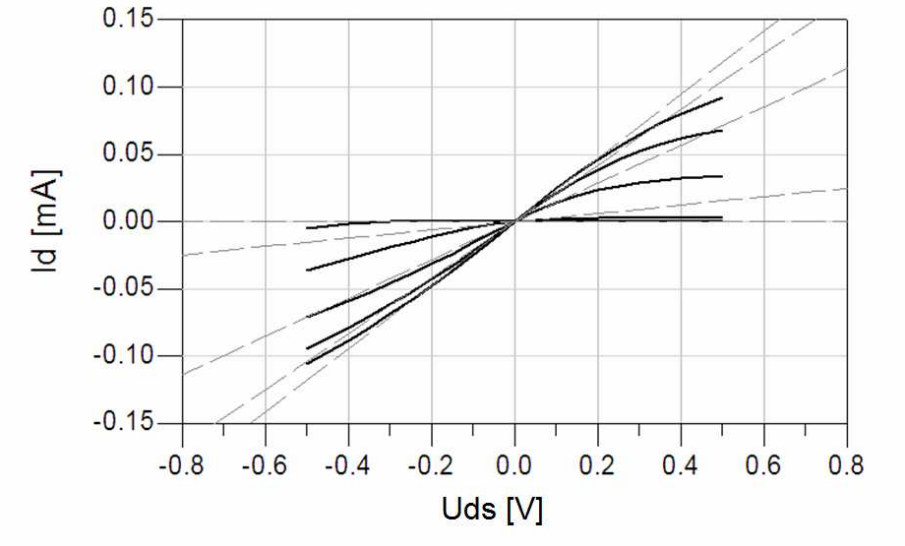


Figure 4.6. Measured channel current as function of both drain and gate bias voltage for the HCMOS transistor with L=0.13 µm, W=40 µm and 10 fingers

If the RF signal amplitude increases, the linear approximation become inaccurate and a Taylor series approximation must be applied. The time dependent relation in equation 4.4 can be now written as:

$$\hat{i}_D(t) = g_D[\hat{u}_{GS}(t), \hat{u}_{DS}(t)] \cdot \hat{u}_{DS}(t), \qquad 4.8$$

where the channel conductance g_D dependes now not only on the LO excitation but also on the momentary amplitude of the RF signal.

In this situation the channel conductance becomes a time variant non-linear element that can be approximated with a Taylor series expansion [61]. If the measured channel conductance can be mathematically modeled with enough accuracy up to a high enough order (three for weakly non-linear systems, as in this case), than the intermodulation behaviour of the mixer can be correctly estimated ([58]).

The channel conductance g_D and all its differentiated components in the Taylor series expansion will fluctuate with the ω_{LO} frequency. The Taylor series can be written as:

$$g_D[\hat{u}_{GS}(t),\hat{u}_{DS}(t)] = g_D[\hat{u}_{GS}(t),0] + \frac{\partial g_D[\hat{u}_{GS}(t),\hat{u}_{DS}(t)]}{\partial \hat{u}_{DS}(t)}\Big|_{\hat{u}_{DS}(t)=0} \cdot \hat{u}_{DS}(t) + \\ + \frac{1}{2!}\frac{\partial^2 g_D[\hat{u}_{GS}(t),\hat{u}_{DS}(t)]}{\partial \hat{u}_{DS}^2(t)}\Big|_{\hat{u}_{DS}(t)=0} \cdot \hat{u}_{DS}^2(t) + \ldots \\ \ldots + \frac{1}{n!}\frac{\partial^n g_D[\hat{u}_{GS}(t),\hat{u}_{DS}(t)]}{\partial \hat{u}_{DS}^n(t)}\Big|_{\hat{u}_{DS}(t)=0} \cdot u_{DS}^n(t) \quad , \qquad 4.9$$

or in compact form:

$$g_D(t) = g_{D,1}(t) + g_{D,2}(t)\cdot\hat{u}_{DS}(t) + g_{D3}(t)\cdot\hat{u}_{D,S}^2(t) + \ldots , \qquad 4.10$$

where

$$g_{D,n}(t) = \frac{1}{n!}\frac{\partial^n \hat{i}_D[\hat{u}_{GS}(t),\hat{u}_{DS}(t)]}{\partial \hat{u}_{DS}^n(t)}\Big|_{\hat{u}_{DS}(t)=0} , \qquad 4.11$$

i.e., the derivatives are time-varying with $\hat{u}_{GS}(t)$ and their waveforms, not their static values are of primary concern.

The very first component in the series $g_{D,1}(t) = g_D[\hat{u}_{GS}(t),0]$ is the one expressed in equation (4.1) through its Fourier expansion and used for the entire conversion matrix formulation.

The conductance current in equation (4.8) can be now expressed based on the new formulation:

$$\hat{i}_D(t) = g_{D,1}(t) \cdot \hat{u}_{DS}(t) + g_{D,2}(t) \cdot \hat{u}_{DS}^2(t) + g_{D,3}(t) \cdot \hat{u}_{DS}^3(t) + \ldots, \qquad 4.12$$

In the equation (4.2) the drain-source voltage $\hat{u}_{DS}(t)$ was defined as a sum of harmonics at frequency combinations of $k \cdot \omega_{LO} + \omega_{IF}$ which can be described as intermodulation products of first order. The same voltage in the Equation (4.12) will consist of intermodulation products of all orders at frequencies like $k \cdot \omega_{LO} + n \cdot \omega_{IF}$.

In order to further simplify the intermodulation analysis, it will be assumed that all voltage products for which $n \geq 2$ are shortcircuited at the load so that the excitation voltage will be limited to first order intermodulation products like $k \cdot \omega_{LO} + \omega_{IF}$.

The second-order components of the drain current, $\hat{i}_{D,2}$ contain frequencies like $k \cdot \omega_{LO} + 2 \cdot \omega_{IF}$ and are synthesized from:

$$\hat{i}_{D,2}(t) = g_{D,1}(t) \cdot \hat{u}_{DS,2}(t) + g_{D,2}(t) \cdot \hat{u}_{DS,1}^2(t), \qquad 4.13$$

The second order excitation $\hat{u}_{D,2}$ is considered short-circuited as assumed above, so that only the second term in Equation (4.13), i.e. $g_{D,2}(t) \cdot \hat{u}_{DS,1}(t)$ will remain. This means that the second order intermodulation performance of the transistor mixer depends exclusively on the time variation of the second-order derivative of the drain conductance represented in Figure 4.7.

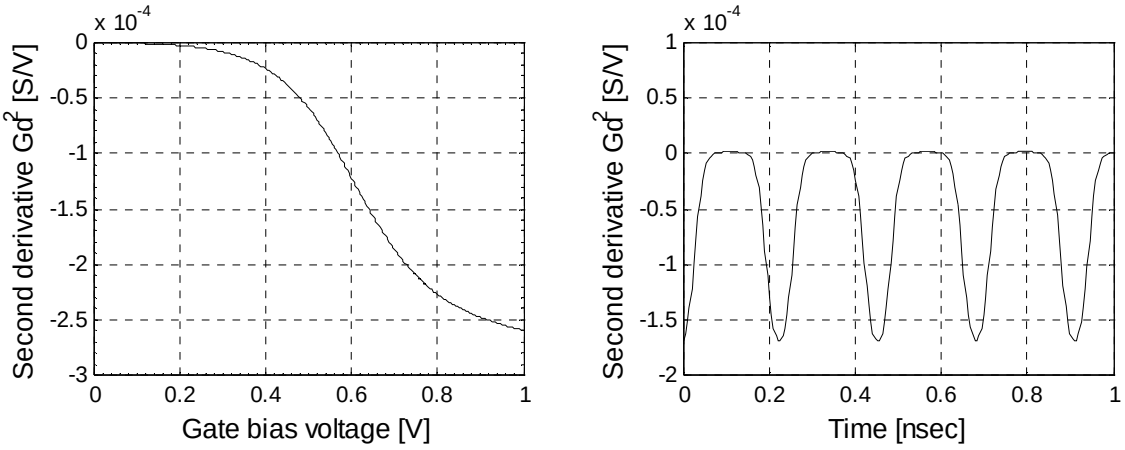


Figure 4.7. Second derivative of the channel conductance vs. gate bias voltage (left) and its time variation (right) for a harmonic excitation of a HCMOS transistor gate with L=0.13 µm and W=40 µm

Like in the large signal analysis of the transistor mixer, the second derivative of the channel conductance can be expressed as a Fourier series:

$$g_{D,2}\left[\hat{u}_{GS}(t),0\right]=\sum_{k}^{K} G_{d,2_k}\, e^{jk\omega_{LO}t}, \qquad 4.14$$

Where: $g_{D,2}$ – second derivative of the channel conductance variation with the LO harmonic excitation,

G_{d_k} – frequency coefficient of the Fourier series expansion of the second derivative of the channel conductance,

ω_{LO} – frequency of the LO signal.

On the other side, the square of the drain voltage first-order excitation can be expressed as a double sum:

$$\hat{u}_{DS,1}^{2}(t)=\frac{1}{4}\sum_{k1}^{K}\sum_{k2}^{K}U_{ds_{k1}}\cdot U_{ds_{k2}}e^{j\left((k1+k2)\omega_{LO}+(\omega_{IF}\pm\omega_{IF}\right)t}, \qquad 4.15$$

Where: $\hat{u}_{DS,1}^{2}(t)$ – square of the first-order voltage on the time varying conductance,

$U_{ds_{ki}}$ – voltage component at the mixing frequency $k\omega_{LO}+\omega_{IF}$,

ω_{LO} – frequency of the LO signal.

ω_{IF} – frequency of the IF signal.

It can be easily observed that the terms of this sum will contain either the double of the IF frequency $k\cdot\omega_{LO}+2\cdot\omega_{IF}$ or only harmonics of the ω_{LO} without any ω_{IF} components.

The second order component of the drain current, $\hat{i}_{D,2}$ can now be expressed like in Equation (4.5)

$$\sum_{l=-N}^{N}I_{d,2_l}\cdot e^{j(l\omega_{LO}+(\omega_{IF}\pm\omega_{IF})t}=\frac{1}{4}\sum_{k1}^{K}\sum_{k2}^{K}\sum_{k3}^{K}\left(\begin{matrix}G_{d,2_{k1}}\cdot U_{ds_{k2}}\cdot U_{ds_{k3}}\cdot\\ e^{j\left((k1+k2+k3)\omega_{LO}+(\omega_{IF}\pm\omega_{IF})\right)t}\end{matrix}\right), \qquad 4.16$$

Another separation on terms with same frequency will permit a tri-dimensional conversion matrix representation similar with the one expressed in Equation (4.6). The IF frequency terms in Equation (4.16) are those for which $k1+k2+k3=0$. In the case of the FET mixer circuit, the dominant terms are those for which the k terms are relatively small (e.g. $\{k1,k2,k3\}=\{0,1,-1\}$), therefore the first two lower harmonics of the channel conductance derivative accounts for the second order intermodulation performance. In very strongly nonlinear circuits like the diode mixer, the higher harmonics of the channel conductance derivation may become significant though.

The third order terms of the drain current, $\hat{i}_{D,3}$ are found similarly. Its expression is:

$$\hat{i}_{D,3}(t) = g_{D,1}(t) \cdot \hat{u}_{DS,3}(t) + 2 \cdot g_{D,2}(t) \cdot \hat{u}_{DS,2}(t) \cdot \hat{u}_{DS,1}(t) + g_{D,3}(t) \cdot \hat{u}^3_{DS,1}(t), \quad 4.17$$

whereas the last term is the dominant one and the first term can be ignored because the $\hat{u}_{DS,3}(t)$ is considered short-circuited at the load. The second term describes the third-order IM distortion resulting from second-order voltage components at the gate; these result from the feedback and are likely to be so small that again can be ignored. The remaining third term contains the third derivative of the channel conductance with the gate voltage. This dependence together with its waveform is depicted in Figure 4.8

Again, can be observed a periodical variation of the third derivative of the channel conductance with the LO excitation. This fact permits the Fourier series expansion like in the precedent case:

$$g_{D,3}[\hat{u}_{GS}(t),0] = \sum_{k}^{K} G_{d,3_k} e^{jk\omega_{LO}t}, \quad 4.18$$

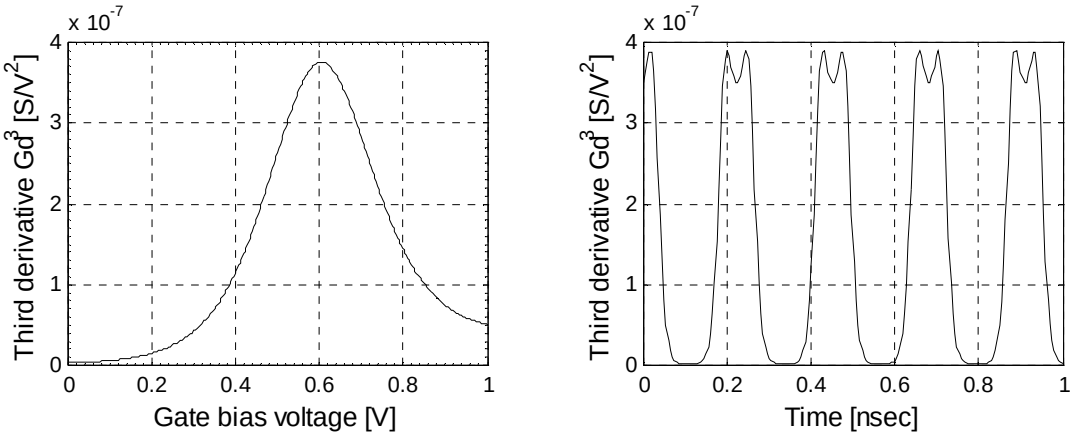


Figure 4.8. Third derivative of the channel conductance vs. gate bias voltage (left) and its time variation (right) for a harmonic excitation of a HCMOS transistor gate with L=0.13 µm and W=40 µm

The third order drain currents arising from the above expressions are:

$$\hat{i}_{d,3}(t)=\frac{1}{8}\sum_{k1}^{K}\sum_{k2}^{K}\sum_{k3}^{K}\sum_{k4}^{K}\begin{pmatrix} G_{d,3k1}\cdot U_{dsk2}\cdot U_{dsk3}\cdot U_{dsk4}\cdot \\ e^{j((k1+k2+k3+k4)\omega_{LO}+(\omega_{IF}\pm\omega_{IF}\pm\omega_{IF}))t} \end{pmatrix}, \qquad 4.19$$

The frequency components resulting from Equation (4.19) contain the combinations: $k\cdot\omega_{LO}+3\cdot\omega_{IF}$ and $k\cdot\omega_{LO}+\omega_{IF}$ whereas the last combination is of great importance for the intermodulation analysis representing the frequency where the third order intermodulation performance is evaluated. All the theory developed until now started from the simple supposition that the drain of the transistor is excited with a single-tone signal at the frequency ω_{RF}. Supposing that there is a two-tones excitation present at the transistor drain at the frequency combination $\omega_{RF1}+\omega_{RF2}$, the third order drain currents will contain the unwanted frequency combinations $2\cdot\omega_{IF1}-\omega_{IF2}$, which will fall in the IF band and cannot be filtered away.

In order to probe the above presented theory, a transistor model was numerically implemented and simulated. For this scope, the general-purpose numerical computing environment Matlab from MathWorks has been used. The transistor model is based on the work published in [64], which was modified to fit the I/V characteristics of the measured HCMOS 0.13 µm transistor used in the mixer circuit.

The junction capacitances C_{GS} and C_{GD} were considered linear and were not modeled for the simulation. The simulations were made with very low frequency excitation signals (50 MHz and below) in order to avoid the influence of the junction capacitances. The simulation results were compared with measurements made at the same frequencies. The test transistor mixer was not optimized with respect to conversion gain or input/output impedance matching. For measurement purposes, the test structure containing singular transistors on the mixer chip where used.

The simulation program written in Matlab calculates the Fourier transformation of the channel conductance and its derivatives with the gate bias voltage, where the channel con-

ductance and its derivatives was modulated by a LO excitation with the voltage amplitude of about 0.5 [V] and a variable DC bias in the range [0…1] [V]. The higher harmonic components of the drain-source voltage $\hat{u}_{DS}(t)$, containing frequency terms like $k{\cdot}\omega_{LO}{+}n{\cdot}\omega_{IF}$, where $n \geq 2$ were not considered during the simulation. The first three harmonics of the channel conductance derivative were added in magnitude considering that their phase remains constant with the bias voltage or LO amplitude.

Based on this simulation, the conversion loss and the third order intermodulation products were estimated. A comparison between the simulation and the measurement results is depicted in Figure 4.10. The comparison shows a good consistence between the third derivative channel conductance variation with the gate bias and the third order intermodulation power of the measured one transistor mixer.

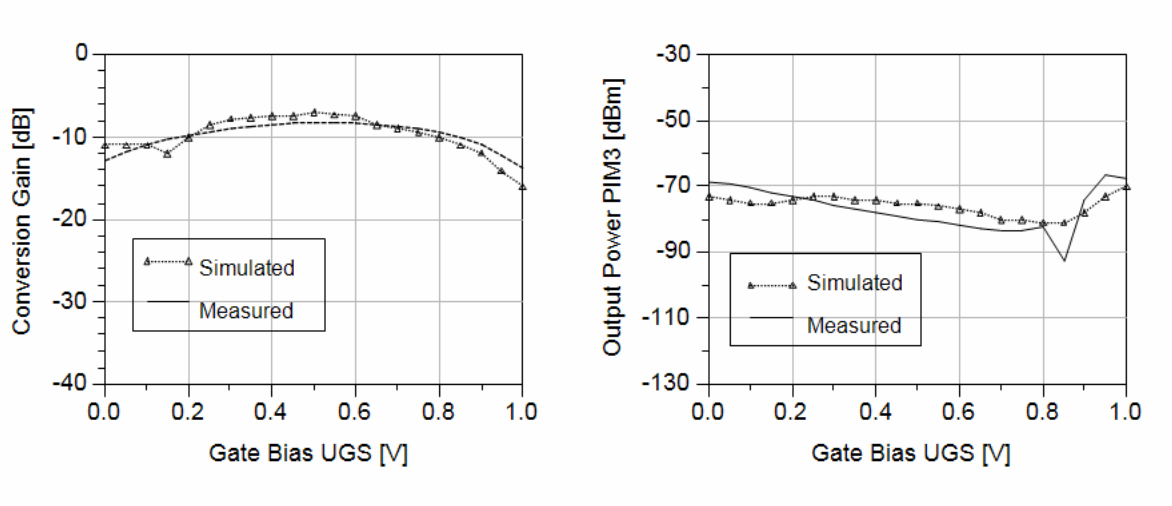


Figure 4.9. Conversion gain (left) and third order intermodulation output power (right) of the one transistor mixer vs. the gate bias voltage, simulated and measured values

In a second stage, the dependency of the channel conductance and its derivatives with the LO amplitude was simulated. The gate bias was kept at a constant value of 0.34 [V] and the LO amplitude was swept so that the available power varies in the range [-10…10] [dBm]. The simulated and measured results are depicted in Figure 4.10. Again, a

good agreement can be observed between the third derivative of the channel conductance and the third order intermodulation power over the LO power range.

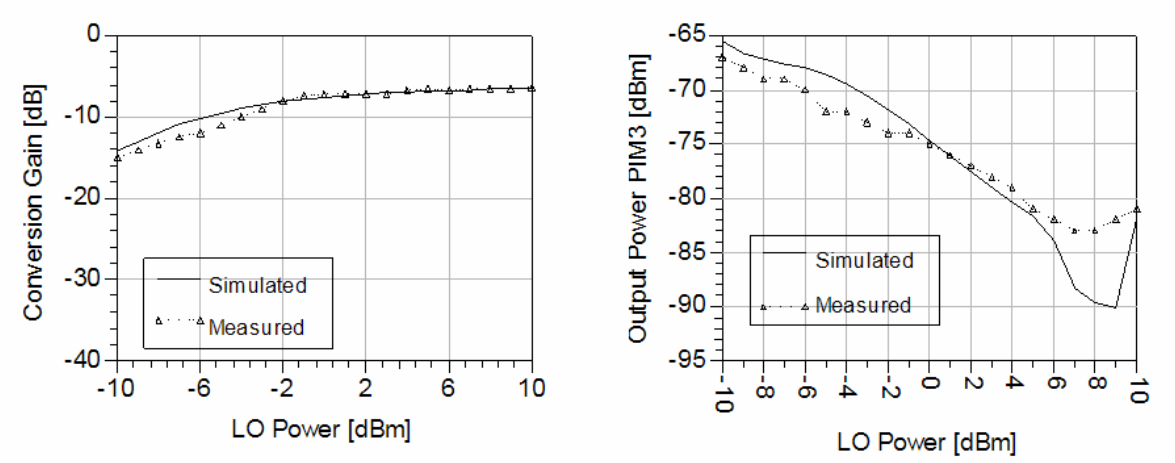


Figure 4.10. Conversion gain (left) and third order intermodulation output power (right) of the one transistor mixer vs. the LO available power, simulated and measured values

The above-depicted comparisons demonstrate the correctitude of the theoretical approach described here. Nevertheless, the method of intermodulation performance evaluation described here is either complete, nor it provides closed solutions for the mixer optimization. The only objective of the method is to demonstrate the dependence between the channel conductance derivations and the intermodulation behavior of the transistor mixer.

Chapter 5.

Reconfigurable Receiver Demonstrator

5.1. Introduction

The present chapter describes the concept and the properties of the reconfigurable receiver demonstrator realized within the “Mobile, reconfigurable multi-standard terminal for UMTS and WLAN” project. The demonstrator is able to receive RF signals belonging to the UMTS or wireless LAN standards and to transform them in base-band signals ready to be digitized by an AD Converter. The demonstrator is not meant to be a fully functional receiver front-end, but rather a system that demonstrates the principles of reconfigurability and reusability. It is also meant as a test board for some of the key functional blocks that were developed within this project in line with the specifications defined for a real receiver. In addition to the reconfigurability principle, the demonstrator means also to prove the possibility of combining two different receiver architectures like direct conversion and half-frequency super-heterodyne in the same system and to point out the relevant problems of this solution. Except for the key functional blocks developed within this project (WLAN mixer and LNA, UMTS LNA and the IQ demodulator mixers), all other functional blocks used in the demonstrator are purchased components and therefore not always fully matched to the receiver specifications.

Concerning the principle of reconfigurability, it was from the beginning defined as the capacity of *alternatively (*and not *concomitantly* receiving one of the above mentioned standards. This definition provides the possibility to optimize the signal processing path applying the principle of reusability.

The combination of two different receiver architectures in the same system creates new problems that are accentuated by the reusability of some functional blocks. The signal isolation between the different receiver paths or the disconnection of the temporarily not used functional blocks are examples of such problems that are open to further examinations.

The demonstrator is able to down-convert signals in the frequency band between 2.11 and 2.17 GHz belonging to the UMTS standard, and both American and European WLAN standards IEEE 802.11a and HIPERLAN/2 that occupy the frequency band between 5.15 and 5.825 GHz. The frequency allocation is graphically displayed in Figure 5.1 below.

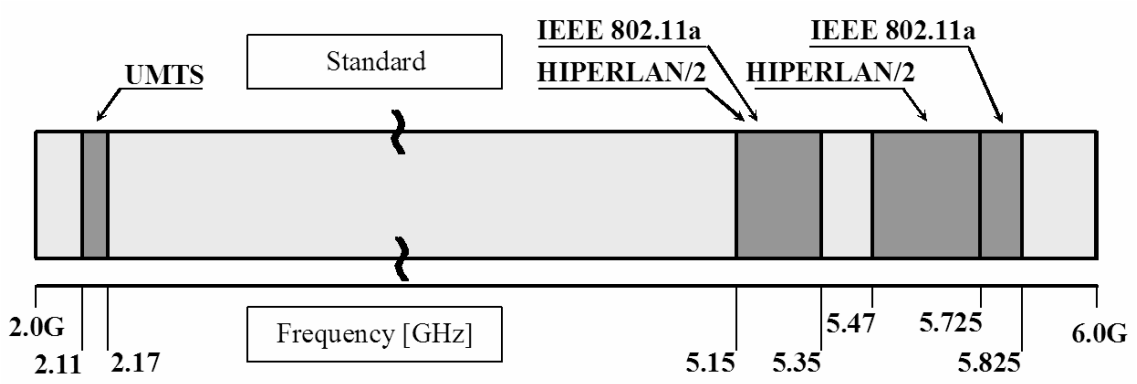


Figure 5.1. Frequency allocation for UMTS and WLAN standards

5.2. Demonstrator Concept

The architecture of the demonstrator is based on the combination of a zero IF receiver for UMTS signals and a half-IF super-heterodyne receiver for WLAN signals. This hybrid architecture provides the maximum number of reusable functional blocks by setting the IF

band of the WLAN receiver very close to the RF band of the UMTS receiver. This way, the receiver chain behind the first WLAN mixer can use the same functional blocks provided by the direct conversion receiver. As one can observe in Figure 5.2, beginning with the power divider, all functional blocks are common for both architectures.

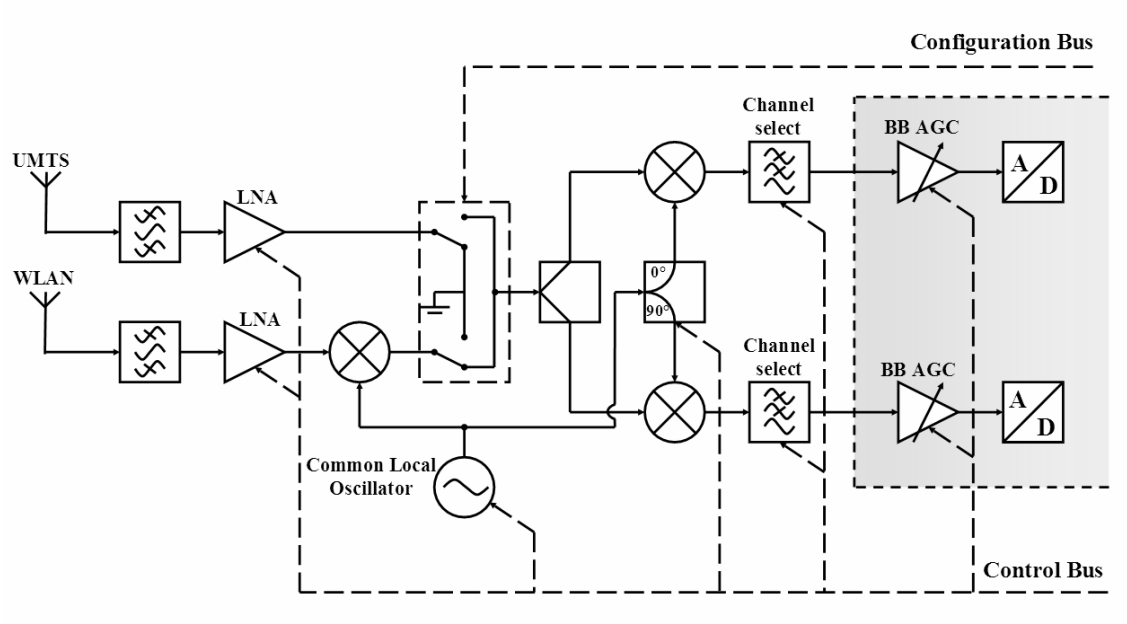


Figure 5.2. Demonstrator architecture (the shaded blocks are not on the experimental board)

The central functional block represents the Standard Switch that determines which signal will be processed at a time. On the other side, most of the functional blocks are controlled in order to establish an optimal path of the signal and to increase the isolation between the different standard signals. The receiver will process only one standard at a time, either UMTS or WLAN. When the receiver down-converts the signal coming from the UMTS board input, the WLAN path is idled. The same happens for the WLAN signal reception. The idling means that the LNA and the mixer in the reception path of the unused standard are not getting any DC power nor an LO signal (the mixer). In order to further separate the signals coming from the two antennas, a RF switch is put in place that brings a further 30 dB isolation between the path from the unused standard signal and the working receiver path. The variable gain baseband amplifiers together with the AD Converters have not

been implemented on the test board, but used separately for measurements, therefore they are separated by a dashed line in Figure 5.2

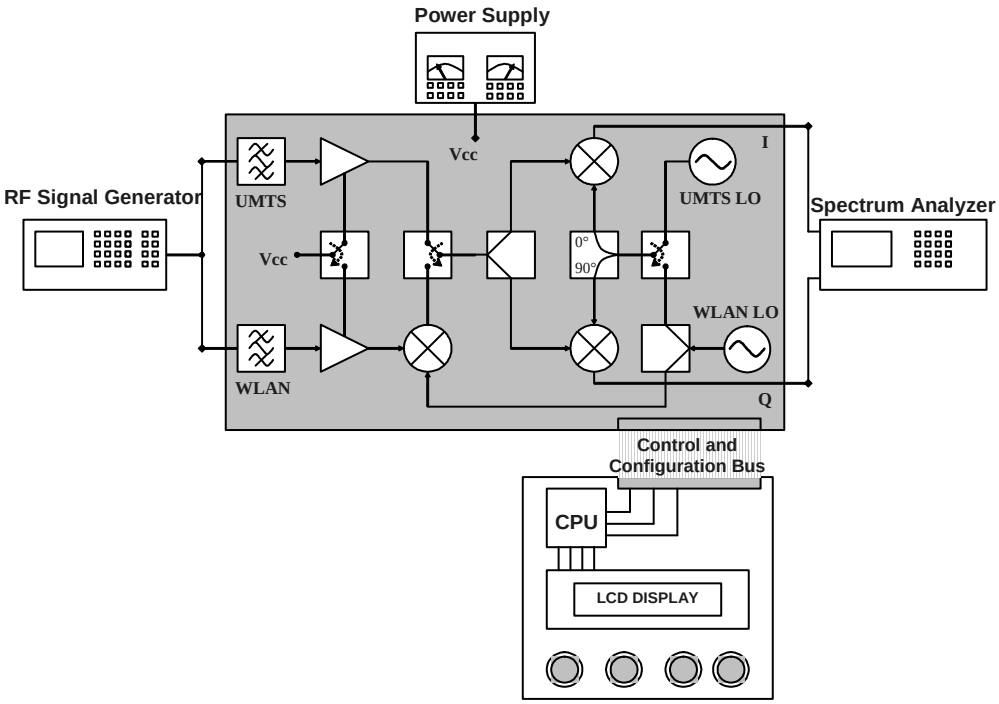


Figure 5.3. Demonstrator concept

The concept of standard switching implies three different processes. The first takes action in the RF path and switches the link between the power divider on the common path and the UMTS LNA or the WLAN mixer respectively. The second process implies switching off the active functional blocks belonging to the not used receiver path. This assures a greater isolation between standard signals and reduces the current consumption. The third process establishes the frequency of the local oscillators used for the system mixers. All three processes take place simultaneously. The configuration is responsible only for the first process, the control bus, on the other side is responsible for the off switching and for the control of the LO frequency. The demonstrator offers the possibility of switching not only between the two types of standards but also choosing a specific channel within one

standard type. The channel selection is made with the same control bus and is commanded with a special hardware present on a separate board, as also depicted in Figure 5.3.

The measurement signals were generated using a RF signal generator and delivered to the test board through coaxial cables. Each transmission standard follows at the beginning a separate path in which the signal is amplified and filtered. After the standard switch, the RF UMTS signal or the IF WLAN signal, both amplified and filtered, are delivered to a common wide-band IQ demodulator. The obtained in-phase and quadrature signals were analyzed with a signal vector analyzer or with the signal spectrum analyzer.

5.3. Practical Realization of the Experimental Board

5.3.1. PCB Layer Structure

The demonstrator board was realized on a four layer PCB whose dimensions are approximately 15x10 cm. The upper layer is based on a high frequency RO4003 substrate material with a dielectric constant ε_r of 3.38. On this layer are driven all high frequency paths. The lower substrates are made from the usual FR4 material that is not critical for low frequency circuitry. The substrate dimensions, along with the entire board layer structure, are depicted in Figure 5.4.

The high frequency lines are designed as 50 Ω microstrip lines with circa 0.43 mm width. In order to avoid coplanar coupling effects we have kept a large distance between the RF lines and isolated them from the other DC lines through ground vias along their sides. The first middle metal layer was defined as ground plane and covers the whole layer surface excepting the vias of the signal and supply lines. The second middle layer is defined as a power plane and is splat into several regions depending on the voltage level needed for the components above. Totally, there are five regions corresponding to the 20, 12, 7, 5 and 3.3 V. All vias in the demonstrator board are through-vias (from one side to the other of the circuit board), fact that simplify the fabrication process and reduce the total cost.

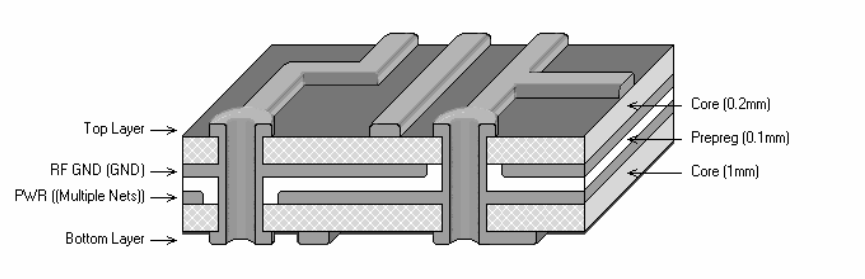


Figure 5.4. Board layer structure

The demonstrator is supplied with two different voltage levels at 20 and 7 V respectively. All other voltage levels needed by different components are obtained through voltage regulators. The supply voltages are DC coupled with RC filters at the input so the actual voltage coming from the supply sources must be slightly larger than 20 and 7 V respectively in order to overcome the voltage fall on the resistance of the filters.

5.3.2. Mixer Bonding Structures

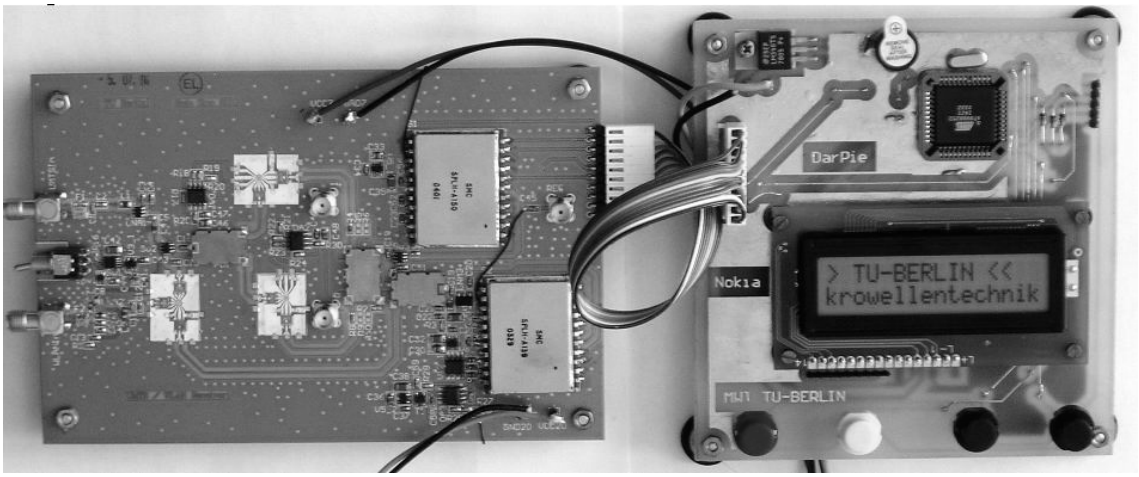


Figure 5.5. Demonstrator board

The bright color structures depicted on the left board in Figure 5.5 are the support structures for the mixers together with the baluns and the bias networks. These structures were

separately developed as bonding structure for a simpler change in case that one of the mixers does not function as expected

The bounding structures (Figure 5.6) are double layer circuits created on the same RO4003 substrate as for the high frequency materials on the main board. The structures are gold plated for a better bonding with gold wires. Because the mixers are balanced circuits and the input and output circuits are single ended elements, we have used Baluns like FB850 (WLAN RF) and FB650 (WLAN IF, UMTS RF) from Anaren.

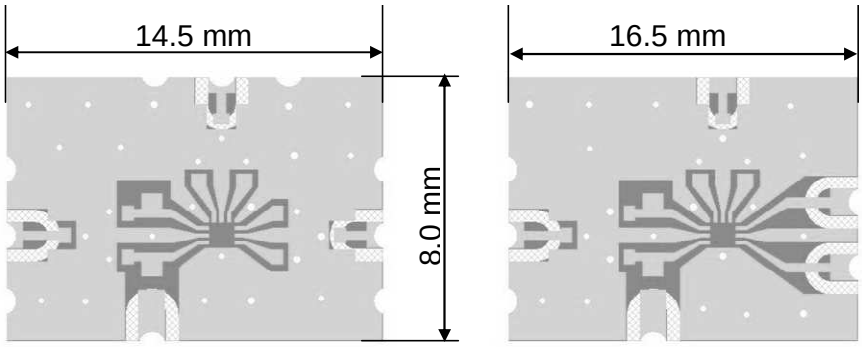


Figure 5.6. Bonding structures for WLAN Mixer (left) and IQ Demodulator Mixer (right)

5.3.3. RF Test-Board Description

Considering the fact that the LO baluns are realized with transmission lines that act as short circuit at DC, we have realized the bias network using only one voltage divider as depicted in Figure 5.7.

As already described in the previous chapter, the UMTS receiver part corresponds to an zero-IF architecture. Along the receiver path, the signal is first filtered with a SAW filter from EPCOS with a center frequency of 2140 MHz and a pass-band of 60 MHz. The signal is afterward amplified and delivered to the IQ demodulator that down-converts it into the baseband. The WLAN signal goes through a little more complicated path, being after the filtering and amplification process, first down-converted to a intermediate frequency be-

fore being delivered to the IQ demodulator. The intermediate frequency is exactly the half frequency of the WLAN RF frequency and is in the frequency domain between 2.5 and 2.9 GHz. That fact eliminate the need of a image frequency filter before the WLAN mixer because the image frequency is in the baseband and is filter by the AC coupling capacitors and the band filter at the input of the receiver. The standard switch assures a signal isolation of about 30 dB between UMTS and WLAN signals and a DC switch at the supply voltage of the LNA's that switches off the unused amplifier will further increase this isolation. Both switches are controlled with a mechanical switch that is placed between the two WLAN and UMTS input connectors. In the assembly process of the demonstrator, we had great difficulties to mount the WLAN amplifier on the board. That fact was due to the UCSP package of the amplifier that needs about 300° C in the area where the chip is located in order to make its solder balls to flow. At such higher temperature, our board bent because of its relatively unsymmetrical layer structure and formed blisters at the lower layer. After few try and error cycles we had to give up for a new redesign of the board and replaced the amplifier with a simple 0 Ω resistance. A new redesign of the demonstrator should include the self-designed WLAN amplifier which will be bounded on test structures like the mixer circuits.

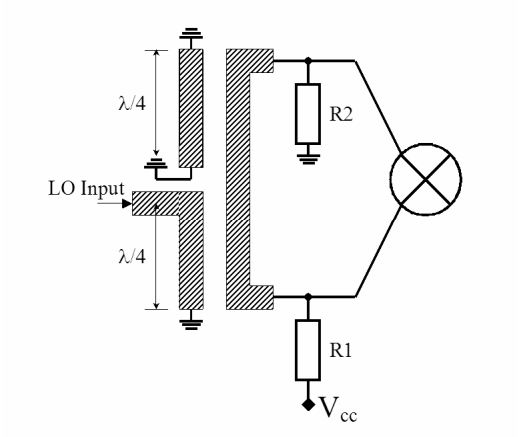


Figure 5.7. The LO input balun together with the bias network

The LO signals for the IQ demodulator and the WLAN mixers are delivered by two synthesizers from Synergy. Although the original receiver architecture includes only one wide range synthesizer, there was no synthesizer available on the market that can cover the entire frequency domain between 2.1 and 2.9 GHz. The LO signal delivered by the UMTS signal coincides with the carrier frequency of the UMTS RF signal and corresponds to the frequency domain between 2.11 and 2.17 GHz. The signal will be amplified through an amplifier and delivered directly to the LO switch that separate the LO signal coming from the UMTS synthesizer from the LO signal coming from the WLAN synthesizer. This switch is controlled also as the standard switch and the DC switch for the LNA's by the mechanical switch presented on the board. The WLAN LO signal will correspond to a frequency band of [2.59 … 2.902] GHz and each frequency is equal to the half carrier frequency of the WLAN RF signal. Totally, the WLAN LO signals can produce 23 different frequency signals corresponding to both IEEE 802.11a and HIPERLAN/2 standards. The LO signal delivered by the WLAN synthesizer is also amplified with the same type of amplifier and afterward splat in two. One part of the signal is delivered to the WLAN mixer and the second part is inputted into the LO switch. The two synthesizers need different supply voltages for their function. The UMTS synthesizer needs 20 V and 5 V supplies and the WLAN synthesizer need 12 V and 5 V supplies. The 20 V supply voltage is delivered directly on the board as described above, and the 12 V voltages is extracted from the 20 V voltage source with a voltage regulator. The 5 V voltage level is also obtained from the 7 V voltage level through a voltage regulator. Beside the supply voltages, the synthesizers also need some reference and control signals. The reference signal has a frequency of 10 MHz but have different forms for UMTS and WLAN synthesizers. For the UMTS synthesizer we need a 5 V square wave and for WLAN synthesizer we need a 1 V_{pp} sinus wave. The reference signal is externally provided from the backside of the signal generator through a SMA connector on the board and has exactly the form needed from the WLAN synthesizer. The digitalization of the reference signal for the UMTS synthesizer is done with an operational amplifier and a Schmidt trigger. All other control signals like Data In, Latch Enable and Clock In are provided through a special interface through the Control Board that will be described later in this chapter.

From the LO switch, depending on the standard that is currently in use, the LO signal of UMTS or WLAN type will enter into a 90° phase shifter. In order to minimize the phase imbalance produced by the phase shifter we have designed the LO lines of the IQ demodulator as variable length lines whose length are determined through the proper placement of a 0 Ω jumper.

The LO signal and the UMTS RF or WLAN IF signals are mixing into the IQ demodulator, resulting a low frequency balanced signal. In conformity with the standard definition, this resulted baseband signal carry the information in the 2.48 MHz band for the UMTS standard and in approximately 10 MHz band for the WLAN signal. Concerning this fact we have used operational amplifiers to transform the balanced signals into single ended signals and to add some amplification to the baseband signal. The resulted signal is outputted through SMA connectors that can be observed in the middle of the board in Figure 5.5.

5.3.4. Control Board

The core of the control board is the microcontroller AT89S8252 from Atmel. Its 64 kB FlashRom program memory is enough for the whole program; therefore, no external program memory is needed. The FlashRom is written through the serial programming interface SPI only once. Afterwards, the functionality of the board remains unchanged until a new upgrade to the board software is made.

The meaning of the SPI port signals is:

- SCK– clock signal,
- MOSI– data in signal for the controller during programming,
- MISO– data out signal for the controller during programming,
- RESET– reset signal for the microcontroller.

In order to program the microcontroller, one has to connect the RS232 port of the computer to the JP2 port on the board. Because the hardware components that transform voltage levels are placed on the board (DZ1-DZ3, R2-R4), there is no need for any adapter between the computer and the control board. During normal operation, the SPI port of the Atmel

microcontroller is used for communication with RF demonstrator board. There is also an LCD display (W1, DEM16217 from Hitachi) on the board that informs the user about the current state of the demonstrator and the LO frequency.

The user can change the operation frequency and demonstrator status (idle/ active) by using four keys (SW1 – SW4).

The supply voltage for the board is of 7 V. This value has been chosen to keep compatibility with the values present on the demonstrator board. However, the digital components placed on the board need 5 V. For this reason, a voltage stabilizer (U2), together with some capacitors is used.

5.4. Performance measurements

In order to prove the functionality of the demonstrator, the measurement system showed in Figure 5.3 was used. The ESG Vector Signal Generator E4438C from Agilent that can generate RF signals for both UMTS and WLAN standards was used as signal source.

In order to determine the dynamic range of the receiver front-end, an UMTS signal with variable power was applied at the receiver input port. The frequency of the signal was arbitrary chosen as the first carrier in the UMTS band (2112.5 MHz), although no difference was observed for all other carriers in the entire UMTS band concerning the performance of the demonstrator. The same LO frequency (2112.5 MHz) was set through the control board for the UMTS synthesizer. The input signal contained a control channel and several data channels. Because the baseband amplifiers and the AD converters are idealized functional blocks integrated in the measurement instrumentation, the dynamic range of the receiver front-end is determined exclusively by the total noise figure and linearity of the LNA and IQ demodulator. The measured dynamic range of the demonstrator ranged from -90 dBm/3.84 MHz (Sensitivity) up to -20 dBm/3.84 MHz (Maximum input power). These values doesn’t fulfill the UMTS requirements but provide a first figure of merit for the embedded functional blocks developed for the present project. In order to determine the above

values, the IQ demodulated signal at the output of the demonstrator was introduced into the PSA Series Spectrum Analyzer E4440A from Agilent. This spectrum analyzer can depict along with the frequency spectrum of the input signal also the code domain spectrum or the IQ diagram of the same signal. As depicted in Figure 5.8, the code domain spectrum of the IQ demodulated signal with the correspondent data and control channels. The input power was varied until the control channel was not recognized anymore in order to determine the sensitivity and the saturation point of the receiver.

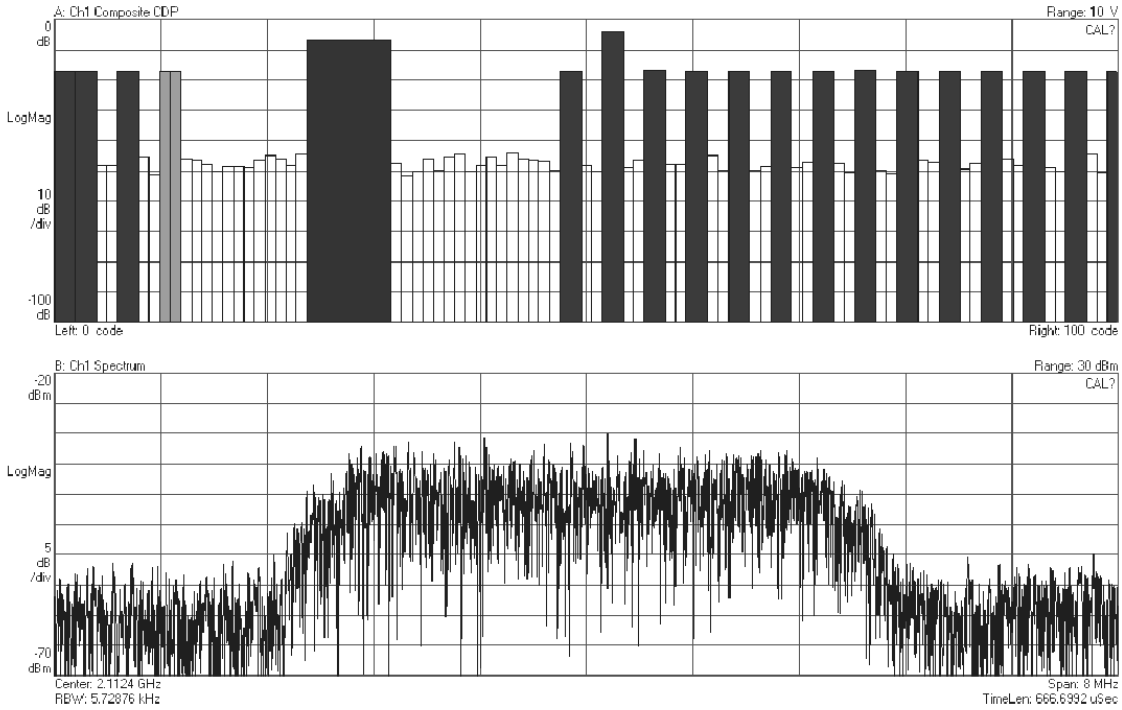


Figure 5.8. UMTS code domain and frequency domain spectrum at the demonstrator output

The same procedure was used also in the WLAN case, with the input signals containing information on only several of the 48 sub-carrier frequencies. After demodulation, the IQ signal was depicted by the spectrum analyzer and as shown in Figure 5.9.

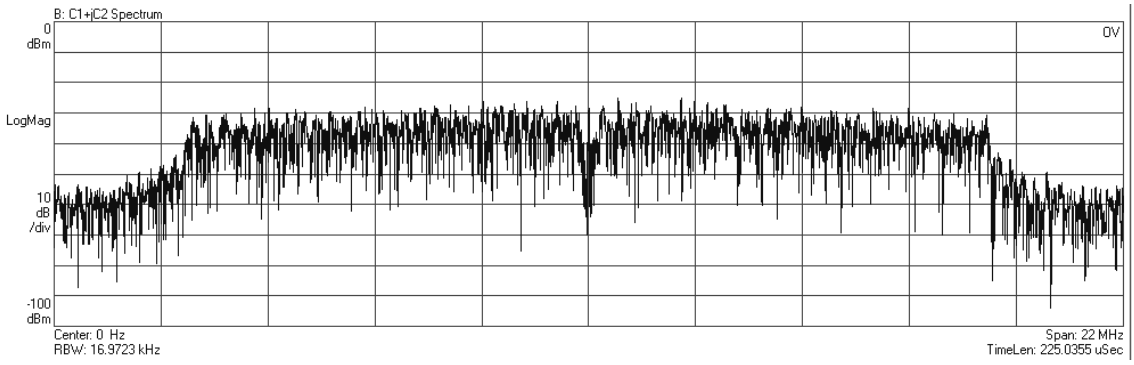


Figure 5.9. WLAN frequency domain spectrum at the demonstrator output

Anyway, there were difficulties in the phase synchronization procedure and unacceptable phase and amplitude imbalances in the IQ demodulator. These unwanted effects that distort the IQ diagram of the demodulated signal appear because not all components in the demonstrator fulfill the specifications defined for this receiver. These non-idealities can though be eliminated with a redesign of the demonstrator that will contain balancing circuits. Some of the non-idealities were also partially eliminated through some patches made on the demonstrator board, but more measures are needed for a better functionality of the demonstrator.

Conclusions and future work

The present thesis focused on conceptual solutions for reconfigurable receiver analog front-ends with special focus on the mixer circuit development and its performance evaluation. The reason for this thesis is the development of a reconfigurable receiver front-end demonstrator, which is able to process signals belonging to the UMTS and WLAN standards. This demonstrator was developed during a collective project between Nokia and the Technical University of Berlin, Karlsruhe University and Dortmund University, which aimed to develop a reconfigurable mobile terminal able to communicate in both UMTS and WLAN networks.

The first chapter of the thesis is dedicated to the theoretical overview of both standard specifications and receiver front-end solutions. Concerning the standard specification, the description was restricted to front-end relevant characteristics, which permitted the derivation of the front-end requirements for both UMTS and WLAN standards. Particularly, the noise figure, intermodulation performance, channel selectivity and saturation level were the main front-end characteristics derived from the standard specifications. There were three methods used to achieve these requirements: publication research, theoretical calculus and system simulation done with the ADS tool from Agilent.

The second part of the first chapter is dedicated to the analysis of different receiver front-end solutions, which can be used for the standards of interest. The chapter provides an overview of the advantages and disadvantages each of these possible solutions provide and deliver the arguments for the choice of the particular solution adopted for implementation.

The chapter concludes with the presentation of the chosen reconfigurable receiver front-end, which is a combination of a Zero-IF architecture for the UMTS standard and a Half-RF architecture with direct-conversion in the second stage for WLAN. While the Zero-IF receiver architecture is already a very popular solution with many advantages and proved implementations, the Half-RF architecture still has to demonstrate its potential. The work presented here was the first known attempt to use this architecture in combination with the Zero-IF architecture. Even if considerably work amount was invested to define the front-end specifications, only a further research can prove if these specifications provide a solid ground for a high-quality receiver. One possible direction of further research is the signal path optimization with accent on the path isolation between the two united architectures. A good balance of gain, noise figure and intermodulation performance along the receiving path is crucial in order to maximize the receiver performance. Further methods for the suppression of the DC offset and flicker noise, but also the IQ amplitude and phase balance should still be taken into consideration for a further development of the presented reconfigurable architecture.

The focus moves in the second chapter from system design to functional block design. The functional block analysis is restricted in this thesis to the frequency conversion blocks. Given a specific technology (CMOS) an extended overview over the different mixer solutions is presented. The most suitable mixer solution for the present project proved to be the resistive mixer. The advantages of this solution compared to the transconductance mixer are its high linearity and the low noise figure, whereas the conversion loss instead of gain proved not to be so important for the present receiver solution.

The third chapter focuses on the development of the mixing blocks that fulfill the requirements of the reconfigurable front-end. The schematic and layout design process is described in depth and is then followed by a complete measurement stage. In this way, the performance of both mixers present in the front-end is fully characterized, together with a detailed description of the measurement methods.

The fourth chapter takes a more theoretical approach to the resistive mixer performance analysis. The one transistor mixer is thoroughly analyzed with respect to the intermodulation behavior. It was analytically demonstrated that the dependence of the derivatives of channel conductance on the drain voltage is responsible for the intermodulation performance of the mixer. This demonstration was based on the Taylor series approximation of the time-variant channel conductance. The analytical approach is further grounded with measurement and simulation comparisons. These comparisons show that the theory developed for the one transistor mixer concerning the intermodulation behavior is true. Further work would imply the single and double balanced transistor mixer analysis. It is easily demonstrable that such circuits exhibit a common channel conductance which is symmetrically identical over the gate voltage (LO pump). This characteristic leads to an isolation on odd harmonics of the LO signal at the IF output and therefore a much better linearity performance.

In the last chapter, a receiver demonstrator, which practically proves the viability of the reconfigurable receiver solution is presented. In the present form, the demonstrator proves the principle of reconfigurability and demonstrates the functionality of the receiver. Moreover, the functionality of several functional blocks developed during the project has been tested and their performance was evaluated under realistically conditions. On the other side, some non-idealities present in the receiver front-end have been identified. These non-idealities represent path-to-path isolations, matching problems and IQ imbalances and all have to be addressed in the subsequent designs.

Appendix A. Mixer Requirements

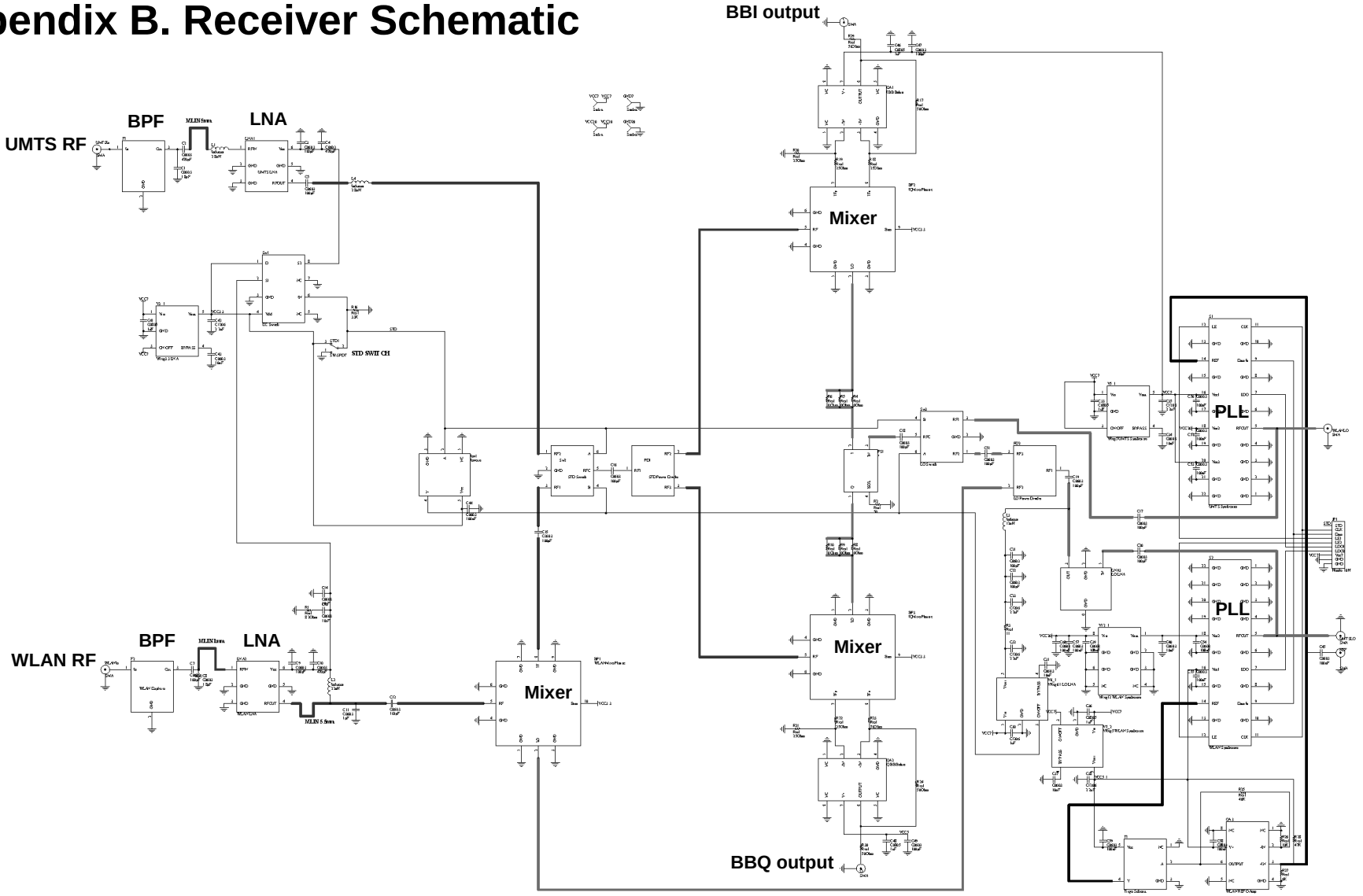
Parameter	Value	Unit	Remarks
RF frequency	2110 … 2170 2560 …2690 2720 … 2875 2852.5 … 2922.5	MHz	UMTS WLAN WLAN WLAN
LO frequency	2112 … 2168 2590 … 2660 2750 … 2850 2872.5 … 2902.5	MHz	UMTS WLAN WLAN WLAN
IF frequency	~0 … 20	MHz	
RF input power	-80 … -18	dBm	-64 … -19 WLAN -80 … -18 UMTS
LO input power	0	dBm	
Conversion gain	-6	dB	
Noise figure	7	dB	
IIP3	2	dBm	
IIP2	22	dBm	
P1dBCP	-8	dBm	-9 WLAN -8 UMTS
Isolation: LO-RF	50	dB	
Isolation: LO-IF	50	dB	
Input / Output type	Differential		

Table A.1. Performance specifications for the IQ demodulator mixer

Parameter	Value	Unit	Remarks
RF frequency	5150 ... 5350 5470 … 5725 5725 … 5825	MHz	Europe/USA Europe USA
LO frequency	2590 … 2660 2750 … 2850 2872.5 … 2902.5	MHz	Europe/USA Europe USA
IF frequency	2560 …2690 2720 … 2875 2852.5 … 2922.5	MHz	
RF input power	-75 ... -10	dBm	
LO input power	0	dBm	
Conversion gain	-6	dB	
Noise figure	7	dB	
IIP3	10	dBm	
IIP2	30	dBm	
P1dBCP	0	dBm	
Isolation: LO-RF	50	dB	
Isolation: LO-IF	50	dB	
Input / Output type	Differential		

Table A.2. Performance specifications for the WLAN mixer

Appendix B. Receiver Schematic



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