# Characterization of Gate Controlled Diodes for IGCT Applications

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# Abstract

The scope of this research work is mainly to characterize and evaluate prototypes of a newly developed device called 'Gate Controlled Diode' (GCD), manufactured and preliminary tested by ABB, Switzerland for steady state operating conditions- forward conducting and reverse blocking mode and transient operation- turn-off mode. The experimental test results are analyzed and evaluated. Furthermore, the prime application of the GCD - the series connection of IGCTs is investigated.

In medium voltage applications, to achieve higher output voltages on the basis of a three level NPC voltage source converter, the series connection of IGCTs is a simple solution. For the effective series connection of IGCTs, the voltage balancing has to be maintained during the blocking mode as well as during the turn-on and turn-off transients. Presently, simple RC or RCD snubbers offer a straight forward solution to maintain the voltage symmetry between the series connected IGCTs and its anti-parallel diodes. However, these conventional snubber networks lead to unwanted effects such as increased losses, space and costs.

The content of this thesis is the introduction of a new device called 'Gate Controlled Diode', which offers an effective solution for the voltage balancing of series connected IGCTs without passive sunbber networks. In this three terminal p+nn+ diode, with an additional gate terminal a positive gate current injection can adjust the voltage balancing between IGCTs and its anti-parallel diodes by changing the resulting leakage current distribution among the series connected devices. First time it has been experimentally analyzed in this thesis that a small gate current (some mA) is required to maintain the static voltage balancing, while for dynamic voltage balancing a sufficient amount of gate charge, which has to be impressed during the turn-off transient of the IGCTs is necessary. Due to the press pack case of the GCD, it offers advantages regarding space and mounting compared to passive networks.

The reverse recovery behavior of the GCD can be influenced by impressing a positive gate current. This feature could also be applied in fast medium voltage diodes (e.g 10 kV diodes).

In normal converter operation the GCD, which is connected anti-parallel to the IGCT can operate as a normal free-wheeling diode. By injecting a gate current into the GCD in its blocking mode, the turn-off current of the IGCT can be reduced. This application of the GCD has also been experimentally investigated.

The experimental results and analysis show that GCD can be a promising solution for an IGCT series connection in voltage source converters.

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# Nomenclature

$\eta_Q$ Charge efficiency

$C_{CL}$ Clamp capacitance

$D_{snub}$ Snubber diode

$I_{A,GCD}$ Anode current of the GCD

$I_{A,IGCT}$ Anode current of the IGCT

$I_{DR}$ Leakage current of the GCD/Diode

$I_{FRMS}$ Maximum rms on-state current of the GCD/Diode

$I_{FVAM}$ Maximum average on-state current of the GCD/Diode

$I_{G,GCD}$ Gate current of the GCD

$I_L$ Load current

$I_{rr}$ Diode/GCD Reverse recovery peak current

$I_{SC}$ Short-circuit current

$L_{CL}$ Clamp inductance

$L_H$ Load inductance

$P_{off}$ Turn-off power loss

$Q_{Gate}$ Impressed gate charge of the GCD

$Q_{rr}$ Diode/GCD Reverse recovery charge

$r_F$ On-state resistance of the GCD/Diode

$R_{CL}$ Clamp resistance

$R_{off}$ Off resistance of the device

$R_{snub}$ Snubber resistor

$T_j$ Junction temperature

$t_{delay}$ Gate current pulse delay of the GCD

$t_f$ Fall time

$T_{j,GCD}$ Junction temperature of GCD

$T_{j,IGCT1}$ Junction temperature of IGCT1

$T_{j,IGCT2}$ Junction temperature of IGCT2

$t_{pulse}$ Width of the Gate current of the GCD

$t_{rr}$ Reverse recovery time of Diode/GCD

$t_s$ Storage time

$V_{AC,GCD}$ Anode to cathode voltage of the GCD

$V_{AC,IGCT}$ Anode to cathode voltage of IGCT

$V_{AK}$ Anode to cathode voltage

$V_{DC}$ DC-link voltage

$V_{FO}$ On-state voltage of the GCD

$V_{GC}$ Gate to cathode voltage

$V_{RRM}$ Repetitive peak reverse voltage of the GCD

$V_{T0}$ Turn-on threshold voltage

$W_{off,GCD}$ Turn-off Energy loss of the GCD

A Anode terminal of the GCD/Diode/IGCT

C Capacitance

D Diode

G Gate terminal of the GCD/IGCT

I, i Current

j Junction

K Cathode terminal of the GCD/Diode/IGCT

L Inductance

n+ Highly n doped semiconductor

n- Lightly n doped semiconductor

P Power

| | |
|---|---|
| p+ | Highly p doped semiconductor |
| p- | Lightly p doped semiconductor |
| Q,q | Electrical charge |
| R,r | Resistance |
| T | Temperature |
| t | Time |
| V, v | Voltage |

# Chapter 1

# Introduction

The task of power electronics is to control the flow of active and reactive power by shaping the voltage and current waveforms using power semiconductor devices. In recent years, the field of power electronics has experienced a substantial growth due to a fast technological development of power semiconductors, which leads to a steadily increasing ratio of performance versus costs. Furthermore, a modification and development of the semiconductor design and the manufacturing technology made it possible to raise the voltage and current ratings of these devices. Today, power semiconductor devices control the parameters of electrical power from few watts to megawatts in a wide range of applications e.g. Industry application, Traction, Power Generation, Transmission and Distribution etc. [23].

According to their device structures and switching conditions, power semiconductor devices can be divided into diodes, transistors and thyristors (Figure 1.1) [23].

1. *Diodes.* On and off state controlled by the power circuit
2. *Thyristors.* Latched on by a control signal but must be turned off by the power circuit
3. *Controllable switches.* Turned on and off by control signal ( devices like BJT, IGBT, GTO, MOSFET )

Figure 1.2 shows the maximum blocking voltages and currents of the available power semiconductors [42].

As mentioned in the reference [23], diodes are mainly classified in Schottky diodes, Epitaxial and Double diffused pin diodes. With reference to the voltage application range, Schottky diodes dominate at low voltages ( $V_{AK} \leq$100 V ) and high switching frequencies, while the fast switching epitaxial ( $V_{AK} \leq$600 - 1200 V ) and double diffused pin diodes ( $V_{AK} \geq$ 1200 V ) are applied at higher voltages. Due to the excellent material properties, SiC power semiconductors have gained more and more importance during the last few years. Today there are ( 300V, 10A ) and ( 600V, 4A-12A ) SiC Schottky diodes available. However, high material and manufacturing costs, slow development of new devices and improved material characteristics are severe limitations of SiC devices today. Therefore, Silicon will be the most extensively used semiconductor material for high power devices in the next years.

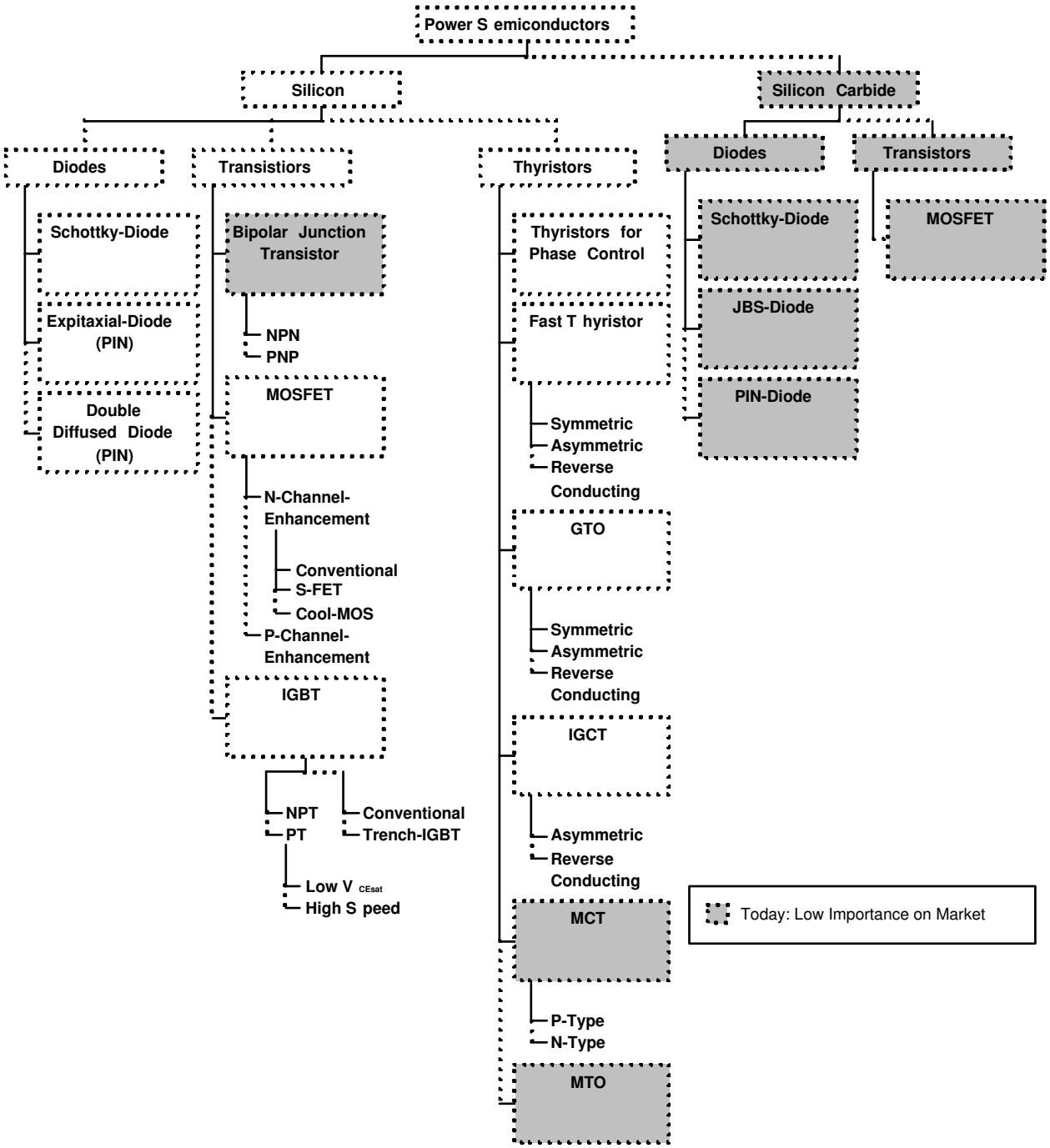



Figure 1.1: Classification of the state of the art power semiconductors [23]

Considering diodes for medium voltage applications ( $V_{AK} \geq 2.5$kV ), the main electrical requirements are

1. low on-state voltages
2. low leakage currents
3. low turn-off losses

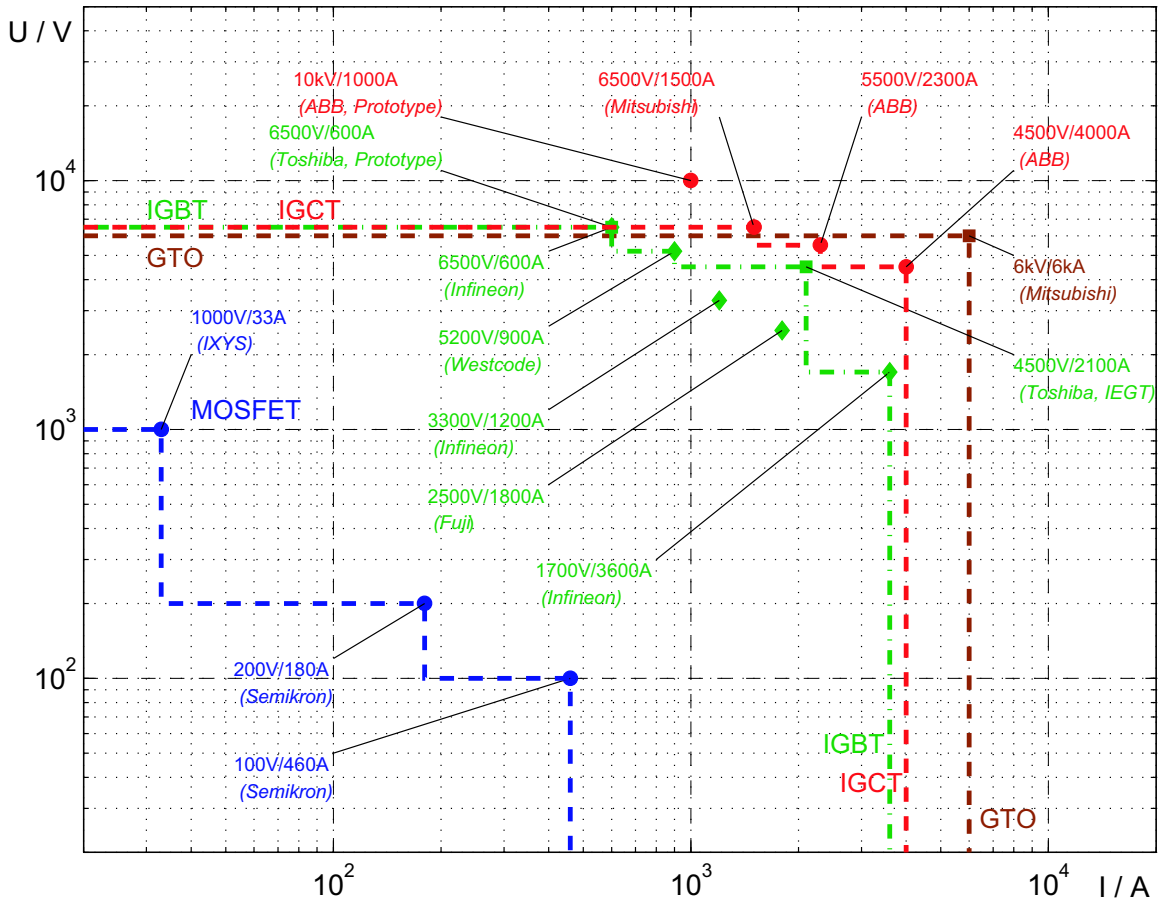



Figure 1.2: Power range of commercially available power semiconductors [42]

4. soft-reverse recovery behavior

The soft reverse recovery behavior for a wide current and junction temperature range is one of the most important requirements at turn-off transients since a sudden drop off of the reverse recovery current at its tail during turn off will cause a substantial over voltage in the circuit. This snappy reverse recovery behavior has to be avoided. It took a comparatively long time until a sufficient solution for a soft reverse recovery was found. Diodes with life time profile control, or p emitter efficiency control are meanwhile established [21]. However, for medium voltage applications the trade-off between on-state losses, turn-off losses and sufficient soft reverse recovery behavior becomes difficult. Still today the diode design has a substantial potential for improvements.

To improve the IGCT series connection and the reverse recovery behavior of fast 10kV diodes, the new concept *'Gate Controlled Diode'*(GCD) was developed. A GCD is a three terminal device with pnp structure. In addition to anode and cathode emitters, it has an extra gate terminal, which affects the reverse recovery behavior of the diode. By injection of holes via the gate to the cathode emitter during blocking state, the leakage current of the GCD can be influenced. The invention and the development of the GCD is certainly an interesting attentive development of new diode concepts.

The idea and design of the GCD was initiated by ABB. The first routine tests (e.g on-state tests, mechanical testing etc) were carried out on the samples of the GCD. These preliminary tested samples have been further investigated for electrical characterizations ( blocking mode and turn-off measurements) and for its application for series connected IGCTs at Berlin University of Technology within this thesis.

Due to the possibility of changing the leakage current of a GCD via its gate emitter in blocking state and the reverse recovery charge during turn-off, the GCD can also be applied for obtaining the voltage symmetry of series connected IGCT switch positions (consisting of one IGCT and one inverse diode (GCD) respectively). This IGCT series connection is a potentially interesting application, since the use of passive elements for voltage balancing could be avoided [6],[10].

To evaluate the technical potential of a GCD for medium voltage applications, this dissertation presents essential characteristics of this new device concept by an investigation of first device samples.

In this dissertation, 4.5 kV GCDs are analyzed and characterized for the first time. In chapter 2 the basic structural details of the GCD are studied. The physics of operation of the GCD in its on-state and blocking mode and also turn-off mode is explained. Finally, an overview of the design details and the manufacturing process of the GCD are carried out briefly.

In chapter 3 the static characteristics in on-state and blocking mode as well as the dynamic behavior at turn-off transients for GCD prototypes are characterized.

The aim of the turn-off mode investigation is to achieve a soft reverse recovery at the tail of the reverse current of the GCD by injecting a specific gate current pulse during the period of reverse recovery time. A simple prototype gate unit is developed for testing purpose. The different parameters of the gate current like delay in injection, pulse length and amplitude are studied and experimentally demonstrated at low (500A) and high (1300A) load currents. The effect of different junction temperatures is also investigated.

To enable an increase of output voltage of a given voltage source converter topology a series connection of IGCTs can be used. In Chapter 4 the requirements for an effective series connection of IGCTs are studied. The conventional methods such as RC and RCD snubbers and regenerative snubbers to ensure a static and dynamic voltage symmetry IGCTs are explained.

In chapter 5 the series connection of IGCTs with conventional RC-snubber is experimentally analyzed for asymmetrical IGCT junction temperatures and different turn-off time delays. The conventional RC-snubbers suffer disadvantages like an increase in losses, space and costs. As an alternative the 'GCD' can be used in parallel to series connected IGCTs to maintain the voltage symmetry during blocking turn-off transients of IGCTs. The results of series connected IGCTs with RC snubbers are compared with series connected IGCTs with anti parallel GCDs.

# Chapter 2

# Structure, Function and Design of a Gate Controlled Diode

## 2.1 Introduction

This chapter describes the basic structure and physics of operation of the Gate Controlled Diode (GCD). After that, the operation of the GCD under two steady state conditions, the forward conducting and the reverse blocking state are considered. These are followed by the structural design details and specification of the prototypes of the GCD prototypes.

## 2.2 Basic structure of the GCD

The GCD features a stationary on-state characteristic, which is basically identical to the characteristic of a conventional fast diode. When the GCD is forward biased, it begins to conduct with only a small forward voltage. However, in contrast to a conventional diode, the additional gate control of a GCD enables the injection of a gate current during turn-off transients or during the blocking state, which leads to an adjustment of the reverse recovery behavior and the leakage current.

This operational features are achieved by the design as shown in Figure 2.1. It shows the structural details of the GCD prototype, which enables a DC blocking voltage of 4500V. Obviously, the GCD has a standard p+ n n+ structure but furthermore, there is an additional lateral p doped layer, which acts as a gate emitter of the device. This gate emitter is used to influence the reverse recovery behavior of the GCD. The vertical cross section of generic GCD with approximate thickness of each doped layer and doping concentration is also shown.

Similar to the conventional fast medium voltage diode structure, the n- layer, which is also termed as the 'Drift region', enables to absorb the depletion layer of the reverse biased p+n- junction during the blocking state. Both doping and thickness of the drift region determine the breakdown voltage of the device. In the GCD, in between n+ and n- layers a small n buffer layer is also added for a moderate lateral cathode conductivity and a good gate sensitivity.

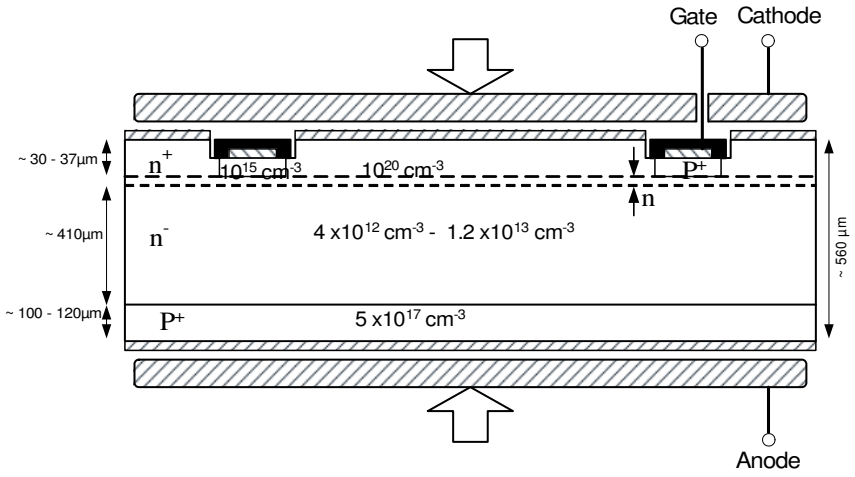



Figure 2.1: Vertical cross section indicating
the dimensions and doping level of a 4.5kV Gate Controlled Diode

The circuit symbol for the GCD is shown in Fig. 2.2. It is essentially the symbol of a conventional diode with a third terminal - the 'Gate'. The voltage and current conventions for the GCD are given in the figure, where $v_{AK}$ is the voltage between anode and cathode, $i_A$ is the anode current and $i_{G,GCD}$ is the impressed gate current.

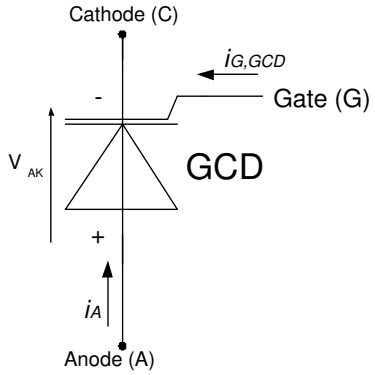



Figure 2.2: Circuit symbol of a GCD

## 2.3 Principle of Operation

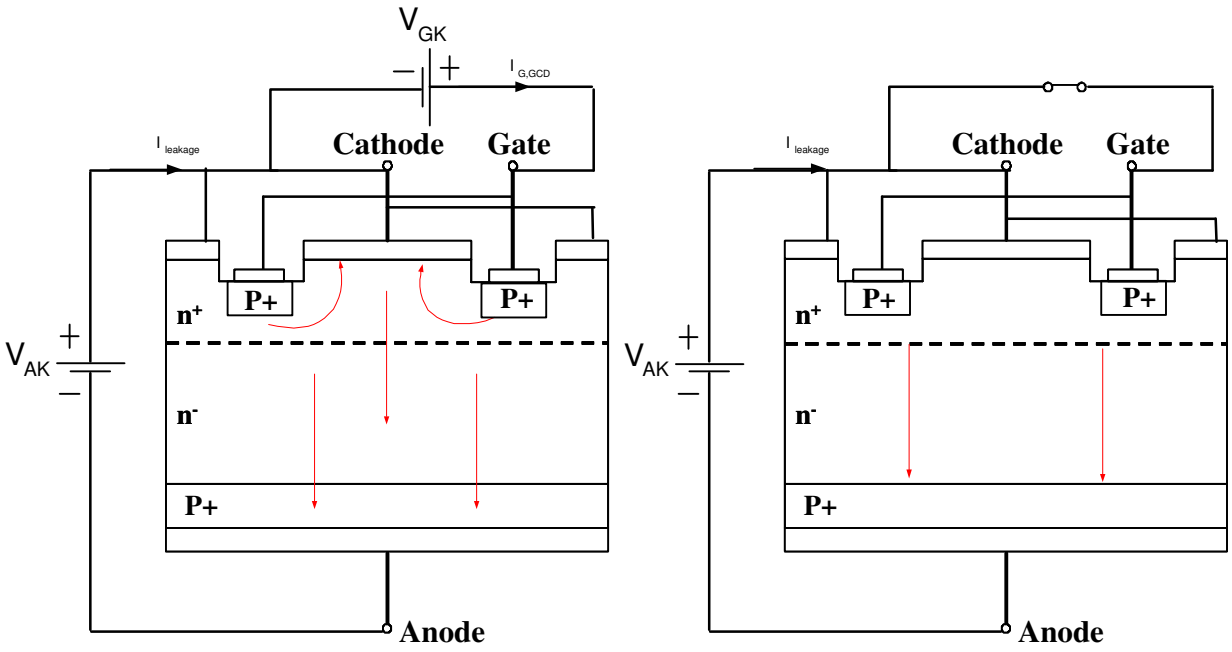
The on-state current - voltage characteristic of a GCD is very similar to that of a conventional diode. However, in the GCD the introduction of the gate emitter enables to influence the reverse recovery process and the leakage current of the reverse blocking state. The gate electrode is not designed to switch on or to switch off the GCD actively.

### 2.3.1 Blocking state

If the anode is set to a negative voltage with respect to the cathode of the GCD, the anode side p-n junction becomes reverse biased. The blocking state must be considered for two cases

1. The cathode side pn junction is forward biased ($V_{GK} \geq V_{FO}$, $I_{G,GCD} > 0$)
2. The cathode side pn junction is short circuited or negative biased ($V_{GK} \leq 0$, $I_{G,GCD} \leq 0$).

Fig.2.3(a) and 2.3(b) illustrate the operational mechanism of the GCD in these two modes of operation.




(a) Blocking mode of operation of GCD (Gate-Cathode pn-junction forward biased)

(b) Blocking mode of operation of GCD (Gate-Cathode pn-junction short circuited)

Figure 2.3: Blocking mode of operation of GCD

If the effect of the gate terminal is prevented by a short circuit between gate and cathode (Fig 2.3(b)) or a negative gate cathode voltage ($V_{GK} \leq 0$) similar to a conventional fast diode in the reverse blocking mode, the negative anode-cathode $V_{AK}$ leads to a space charge region of the anode side pn-junction. Because of the lower doping of the n- base compared to the p+ doped anode, the main part of the space charge extends into the n-base region. This leads to an increase of the potential barrier across the junction, which drastically reduces the probability of any carrier diffusing across the junction. Therefore, the leakage current is caused by the electrons and holes generated in the space charge region by thermal ionization process.

In the blocking mode a variation of the leakage current is possible by the impression of a positive gate current (Fig 2.3(a)). In this mode of operation, two p-n junctions are active, one between p+ anode emitter and n-base and another between p+ doped gate and n+ doped cathode emitter. Most of the holes injected from the gate emitter recombine with the electrons at

the n buffer layer as shown in Fig.2.3(a). However, a small part of these injected holes reach the space charge region via the n+ doped layer. These holes are dropped down to the anode side pn-junction and increase the leakage current through the device. The doping profile is realized in such a way that the increase in total leakage current is almost proportional to the injected gate current.

Obviously the trade off between gate sensitivity and lateral conductivity of the cathode emitter is achieved by a specific design of cathode and gate emitter.

### 2.3.2 On-state

Assuming short circuited gate and cathode terminals, the on-state behavior of the GCD is basically equivalent to that of a conventional fast diode without gate-cathode pn-junction.

In the on-state ($V_{AK} \geq V_{FO}$), the forward bias of anode side p-n junction leads to a hole injection by the anode and to an electron injection by the cathode. In this case, the cathode has a negative potential with respect to the anode emitter. The holes and electrons generate a storage charge mainly in the n- region and thus cause a low on-state resistance. Thus, the on-state current-voltage characteristic is corresponds to that of an equivalent conventional fast diode. Fig.2.4 shows the current flow during the on-state mode of operation of the GCD.

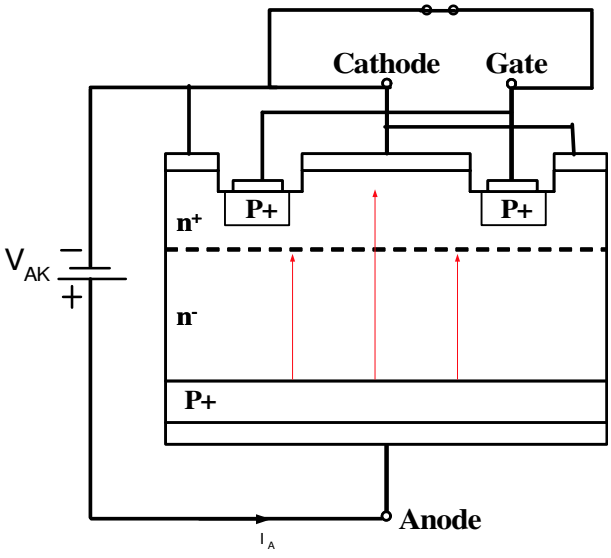



Figure 2.4: On-state operation of GCD

In the designed and manufactured GCD prototypes the injection of a positive gate current (i.e. holes via gate) has no considerable effect on the voltage drop in the on-state.

### 2.3.3 Reverse recovery behavior

The physics of the reverse recovery operation of the GCD is considered in two conditions such as without the gate current impression and with the gate current impression in the GCD. The operation of the GCD without gate current impression is similar to a conventional fast diode operation in the turn-off transient while with the gate current impression it differs. Thus, the understanding of the turn-off process of a conventional diode is necessary.

**Analogy of the turn-off mode of the GCD with conventional fast diode turn-off operation**

To understand the behavior of the GCD, it is useful to describe the basics of a snappy and a soft recovery behavior of a conventional p-i-n diode. Figure 2.5 shows the reverse recovery waveform, the doping profile and the simulated charge carrier distribution of a conventional pn-n+-diode with snappy reverse recovery behavior [21], [42].

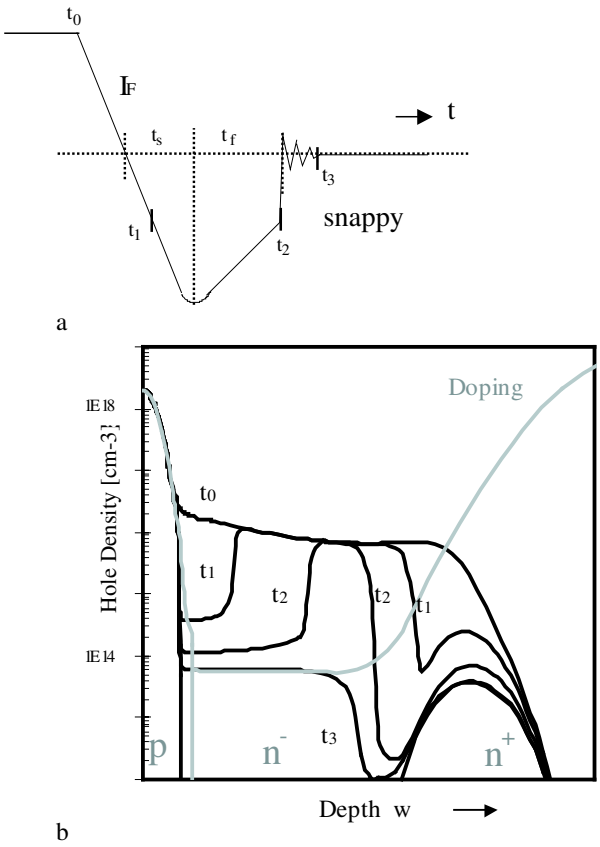



Figure 2.5: Conventional Diode with snappy recovery behavior
(a) turn-off current (b) hole density at different points in time [21]

The time point $t_0$ indicates the distribution of the electrons and hole plasma during the on-state. In the low doped base region, the electrons equal to the hole charge density. During the reverse recovery process, holes are removed to the left side and electrons are removed to the right side and the plasma is feeding the reverse current. The flowing reverse recovery current leads to

a decrease of the excess charge carriers close to the p+ and the n+ region. Immediately after reaching the time point $t_2$, both fronts of the plasma meet and suddenly the source of the charge carriers for the reverse current vanishes. Thus, the reverse current is interrupted abruptly, leading to a snappy recovery behavior at its tail as shown in Figure 2.5(a)[21].

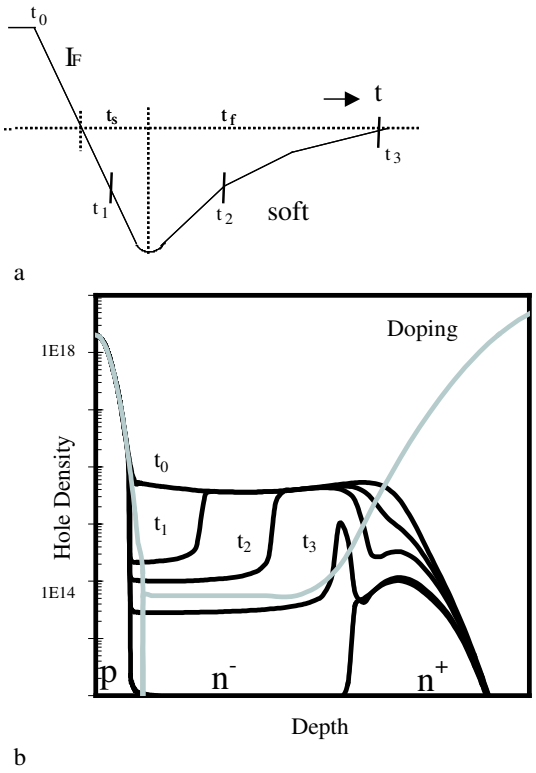



Figure 2.6: Conventional Diode with soft recovery behavior
(a) turn-off current (b) hole density at different points in time [21]

In a conventional p+n-n+ diode with soft reverse recovery behavior (Fig.2.6), there is still enough plasma in the diode at the time point $t_2$ to enable a soft decay of the reverse recovery current. In that case, the transition from the time point $t_2$ to the time point $t_3$ is slow. If the width between p-n junction and plasma is sufficient to take the voltage until the end of the reverse recovery process, snappiness can be avoided. It is worth to be noted that whether the recovery behavior is soft or snappy depends on the dynamic distribution of the plasma. To avoid a snappy behavior, a sufficiently large plasma should be close to the n-n+ border in the time interval between $t_2$ and $t_3$.

An alternative concept is the injection of an external gate current during the reverse recovery process in a gate controlled diode. It should be close to the n-n+ border. That means, in the gate controlled diode, if the gate current injection takes place between $t_2$ and $t_3$, additional charge carriers should enable a soft reverse recovery behavior.

Thus, a GCD could have analogous operational features and a similar structure like a conventional diode. The soft reverse recovery of a conventional diode mentioned above can be considered as a reference for the soft reverse recovery of a GCD. Referring the doping profile of the GCD in Fig.2.13, Fig.2.14, Fig.2.15, it can be clearly understood that the injection of holes is done via the gate emitter, which is located close to the cathode side n-n+ junction.

It should be noted that a gate current could be impressed in the GCD before or during the reverse recovery process of the diode to soften the interruption of the reverse current.

If the injection of holes via the gate is done at $t_1$, then from the diagram (Fig. 2.6) it can be imagined that the plasma distribution at the n-n+ border, which is the cause of the change of the recovery behavior will change slightly. Thus a small variation of the interruption of the reverse recovery current can be expected. In contrast, an impression of a gate current close to n-n+ border between the time $t_2$ and $t_3$ could lead to a notable change of the charge carrier distribution during the interruption of the reverse recovery current. In this case a more efficient shaping of the decaying reverse recovery current can be expected.

**Analysis of the GCD reverse recovery behavior assuming short circuited gate-cathode terminals**

The turn-off transient of a GCD with short circuited gate-cathode terminals is analogous to the reverse recovery behavior of an equivalent conventional diode.

The turn-off waveforms of the GCD are investigated by considering a buck converter circuit. Figure 2.7 shows the a buck converter circuit configuration assuming an IGCT as an active switch and a GCD as free- wheeling diode.

For the commutation of the load current $I_L$ from the GCD to the IGCT after an active turn-on transient, the rise of current is limited by the clamp inductance. In the entire commutation process, the load current $I_L$ is assumed to be constant.

Figure 2.8 shows the basic current and voltage waveforms during the natural commutation in the buck converter i.e. the waveforms during the turn-on of the IGCT and the turn-off of the GCD.

Initially the GCD is on and carries the load current i.e. $I_{A,GCD}$ = $I_L$. The IGCT is then turned on and the GCD is turned off. Assuming a low IGCT voltage during the current rise there is an almost linear decrease of the GCD current $I_{A,GCD}$,

$$-\frac{di_{A,GCD}}{dt} = \frac{V_{DC}}{L_{CL}} \tag{2.1}$$

where, $V_{DC}$ is the applied DC voltage, $I_{A,GCD}$ is the GCD anode current and $L_{CL}$ is the clamp inductance.

As $I_{A,IGCT}$ + $I_{A,GCD}$ = $I_L$ (constant) the above equation can be written as

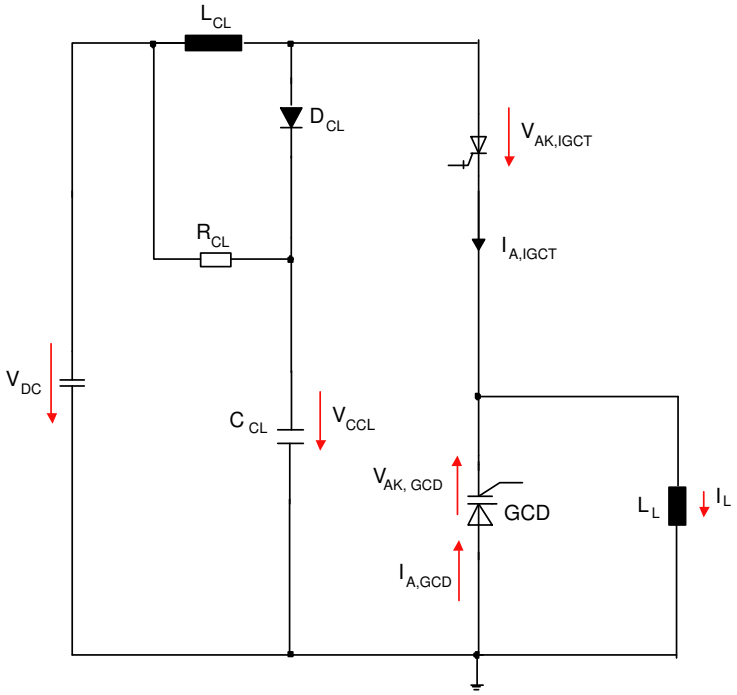



Figure 2.7: Test circuit for the investigation of the diode reverse recovery behavior

$$\frac{di_{A,IGCT}}{dt} = -\frac{di_{A,GCD}}{dt} \tag{2.2}$$

Obviously the reverse recovery of the GCD will also flow through the turning on IGCT.

As explained before the excessive storage charge carriers in the n- and p+ region are the reasons for the presence of reverse recovery current during the reverse recovery time $t_{rr}$. The definition of characteristic values of the reverse recovery process of the GCD (or a conventional diode) is shown in Fig. 2.9.

In the reverse recovery process, when the anode current is negative and the carrier sweep out has proceeded for a sufficient time ($t_s$) to reduce the excess-carrier density at one or both of the junctions to zero, the junction becomes reversed biased. At this point, the GCD voltage goes negative and rapidly acquires a substantial negative value, as the depletion regions from the two junctions expand into the drift region towards each other. At this time, the negative GCD current demanded by the stray inductance of the external circuit cannot be supported by excess charge carriers because too few carriers remain. The diode current ceases its growth in the negative direction and quickly falls, becoming zero after a time $t_f$. The reverse current has its maximum reverse value $I_{rr}$ at the end of the interval $t_s$. The complete process of the commutation is finished when the GCD reverse recovery current reaches zero and the GCD blocks the DC voltage $V_{CCL}$.

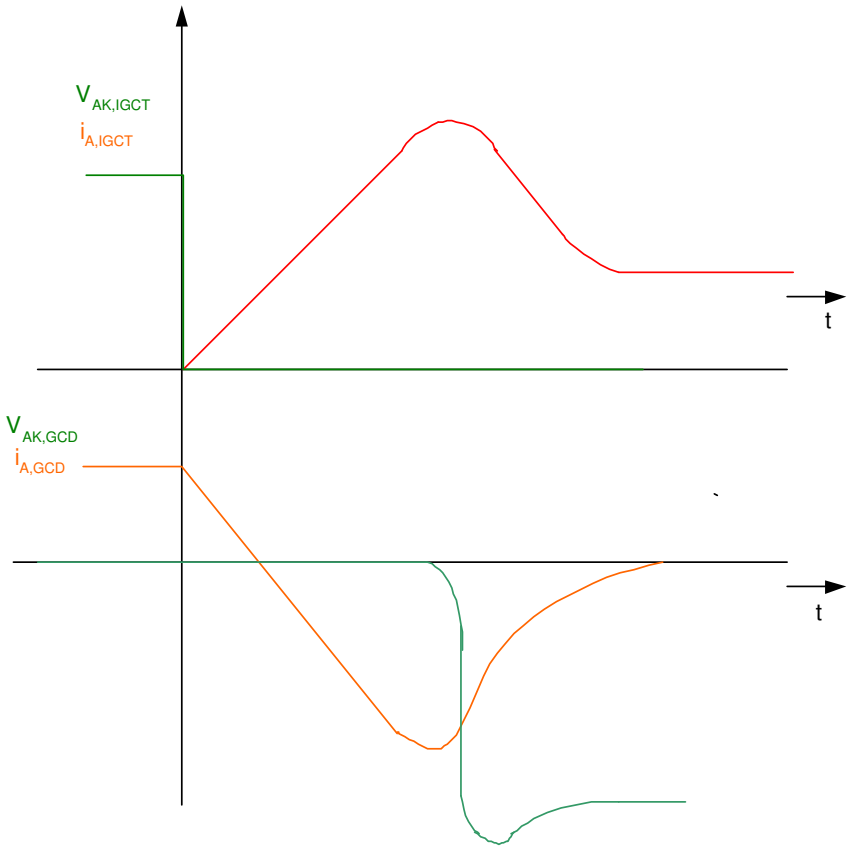



Figure 2.8: Voltage and current waveforms of natural commutation of IGCT and GCD ( Turn-on of IGCT / Turn-off of Diode)

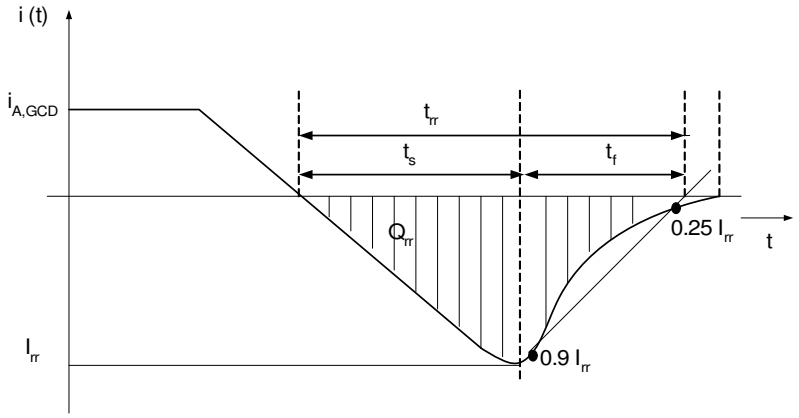



Figure 2.9: Current waveform of the GCD during the turn-off transient

**Analysis of the reverse recovery behavior assuming a forward biased gate-cathode ($I_{G,GCD}$ > 0)**

Before the zero crossing of $I_{A,GCD}$, the gate emitter of the GCD can be forward biased with respect to the cathode terminal. The hole injection via the gate emitter deviates the turn-off behavior of the GCD. The investigation presented in chapter 3 will show that especially the interruption of the reverse recovery current can be influenced by the impressed gate current. The

effect of injection of the gate current can be analyzed by considering the role of the p+n- and n+n- junctions. The reason for the formation of the second n-n+ depletion region (right side of the cathode) is the fast extraction of electrons through the cathode in the case of high di/dt and high dv/dt during turn-off. The operation in this transient state is highly affected by how fast the two space charge regions across these junctions during reverse biased mode expand. During the reverse recovery process, the higher mobility of electrons compared to that of holes results in faster expansion of the space charge region at the p-n junction than at the n-n+ junction. The build up of a second space charge region is highly undesirable as it reduces the effective n- base width. The reduction in n-base width due to the second space charge region is the reason for the snappy behavior of the reverse recovery current. By injecting holes from p+ doped gate emitter from cathode side, the width of the depletion region at the n-n+ junction is controlled by allowing recombination of holes and electrons at the gate cathode junction. The goal of the gate current injection is a soft reverse recovery of the current in the tail region. In brief, the gate emitter junction controls how fast the excessive reverse recovery charges are removed and the reverse recovery current falls to zero.

Chapter 3 shows the results of the experimental investigation of the turn-off behavior of different GCD prototypes considering the effect of gate current during the reverse recovery process.

It is expected that a negative gate cathode voltage leads to a similar behavior, like at short circuited gate-cathode pn-junction since in both cases, the cathode side pn-junction is not effective.

## 2.4 Design details and built-up process of the GCD

### 2.4.1 Design details

The GCD prototype body is mainly subdivided into two different doped levels (p doped and n doped) similar to the conventional diode structure. Fig.2.10 shows the three dimensional view of the GCD prototype under test. It consists of a heavily doped p+ substrate, which acts as an anode emitter. On top of this, a lightly doped n- type epitaxial layer is grown with a specific thickness (For the exact dimensions of the prototype refer to Fig.2.1). This layer is called as 'Drift region'. It has a high ohmic resistance. This layer determines the breakdown voltage of the GCD and it influences also the on-state and turn-off losses of the device. A trade-off has to be done between the on-state power losses and the blocking voltage capability while deciding the thickness of the n- layer. The cathode emitter is formed by doping a n+ layer on top of a n-layer. This constructional design is advantageous, possessing high switching frequency and current capacity. In between the n+ cathode layer and the n- drift region, a very thin n- buffer layer is formed.

The p+ doped gate electrode is etched into the n+ doped cathode. The etching is done into the n+ cathode layer till it touches the n- buffer layer. The etching of the gate emitter is achieved in a specified manner to avoid any high current densities and to maintain good gate sensitivity. The fine structural design and homogeneity of the gate emitter depends on the required gate current.

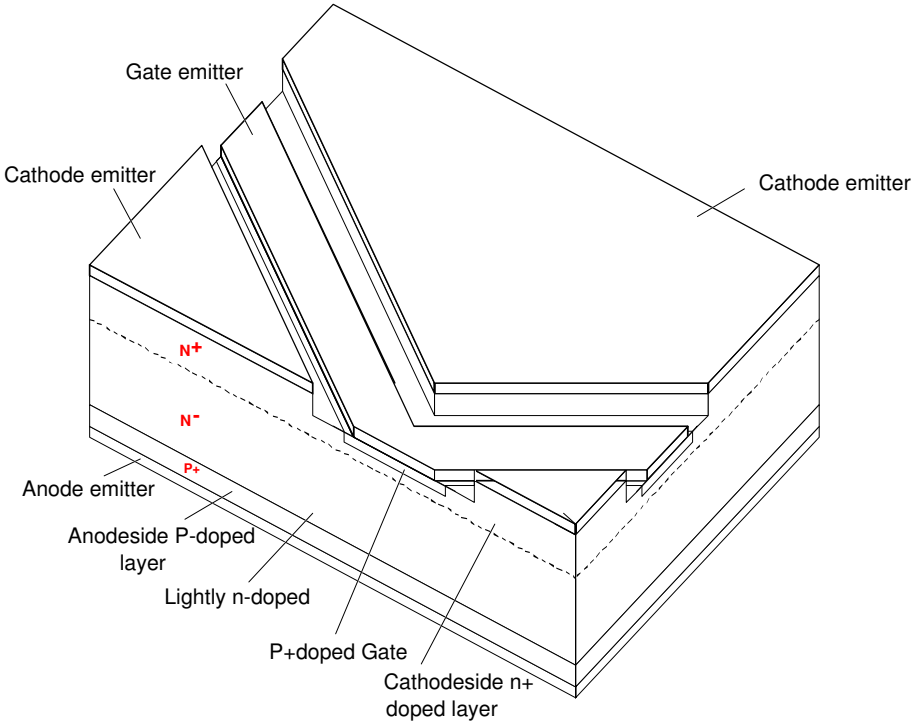



Figure 2.10: 3-dimensional view of a GCD prototype

Two different structures of gate cathode layouts are shown in Fig.2.11. In Fig. 2.11 (a) it can be seen that the entire structure has divided cathode segments. The gate emitter connection is formed in between the cathode segments.

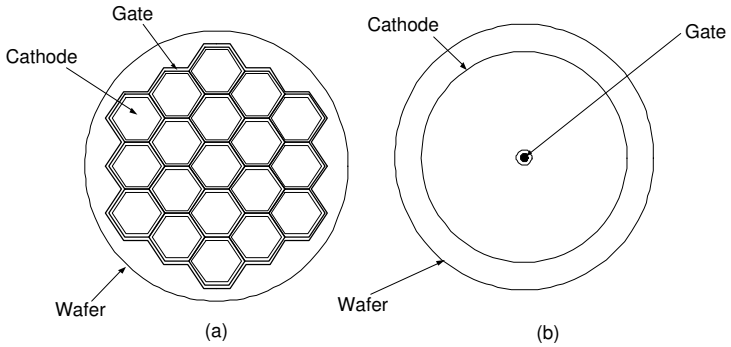



Figure 2.11: Two gate and cathode layouts of a GCD

Fig.2.11(a) shows the hexagonal cathode islands are surrounded by the gate emitter layer. This is a well preferred geometry for gate cathode layouts. The size and thickness of the gate emitter of the hexagon depends on how much current needs to be injected. An alternative design shown is in Fig.2.11(b). The cathode area is bigger than the gate, which is located in the center of the wafer. The larger surface area of the cathode is required as it carries the entire load current.

The lateral structure design of the cathode is similar to the design used in the GTO or GCT. However, the difference in the design can be clearly distinguished. In the GCD prototypes, p+ doped gate segments are equally divided into the n+ cathode, unlike GTO structure, where n+ cathode segments are divided by p+ doped gate layers.

From the previous section, which explains the operational features of the GCD, it is understood that an injection of the current into the space charge region during the blocking state means an injection of holes from the cathode side. The same effect could be realized by injecting electrons from the anode side. However, in this thesis only the cathode side gate design is considered. The considered device structure is advantageous due to to several reasons such as

- The soft reverse recovery behavior of the p+ n n+ structure favors a very high cathode emitter efficiency and moderate anode emitter efficiency. A cathode side gate is easier to integrate without affecting the on-state characteristic.
- Regarding the blocking capacity of the device, the main junction on the anode side has to be a deep diffused junction, preferably with a large space constant. On the other hand, the buffer layer design on the cathode side could be rather shallow, which is better suited for an injecting gate structure.
- Lifetime engineering of the diode favors a high recombination on the anode side and a high carrier lifetime on the cathode side, making the cathode side more suitable for an injection of gate current.

### 2.4.2 Manufacturing process of the GCD

To obtain the desired static and dynamic properties certain parameters have to be adjusted during the physical built-up process of GCD prototypes

- Carrier life time which is adjusted by electron, H+ or He++ irradiation
- Axial or lateral structure of carrier life time
- Special control of carrier life time at the etches
- Homogeneous emitter engineering to affect the plasma distribution in the on-state condition

Fig.2.12 explains in brief the process to built up GCD prototypes.

To get a brief overview of the process of manufacturing GCD prototypes, in the first stage of the manufacturing process, the p+ doped anode is implanted via boron implantation on the base of resistivity of 328 Ohm-cm. Later, the aluminum anode implantation is followed by a boron drive-in at 1250°C for 38 hrs.

The drive-in process allows the deposited Boron to diffuse into the wafer. In this process the Boron moves from the high-concentration region (near the surface) to the low-concentration region (in the bulk). This produces a concentration variation as a function of depth as shown in

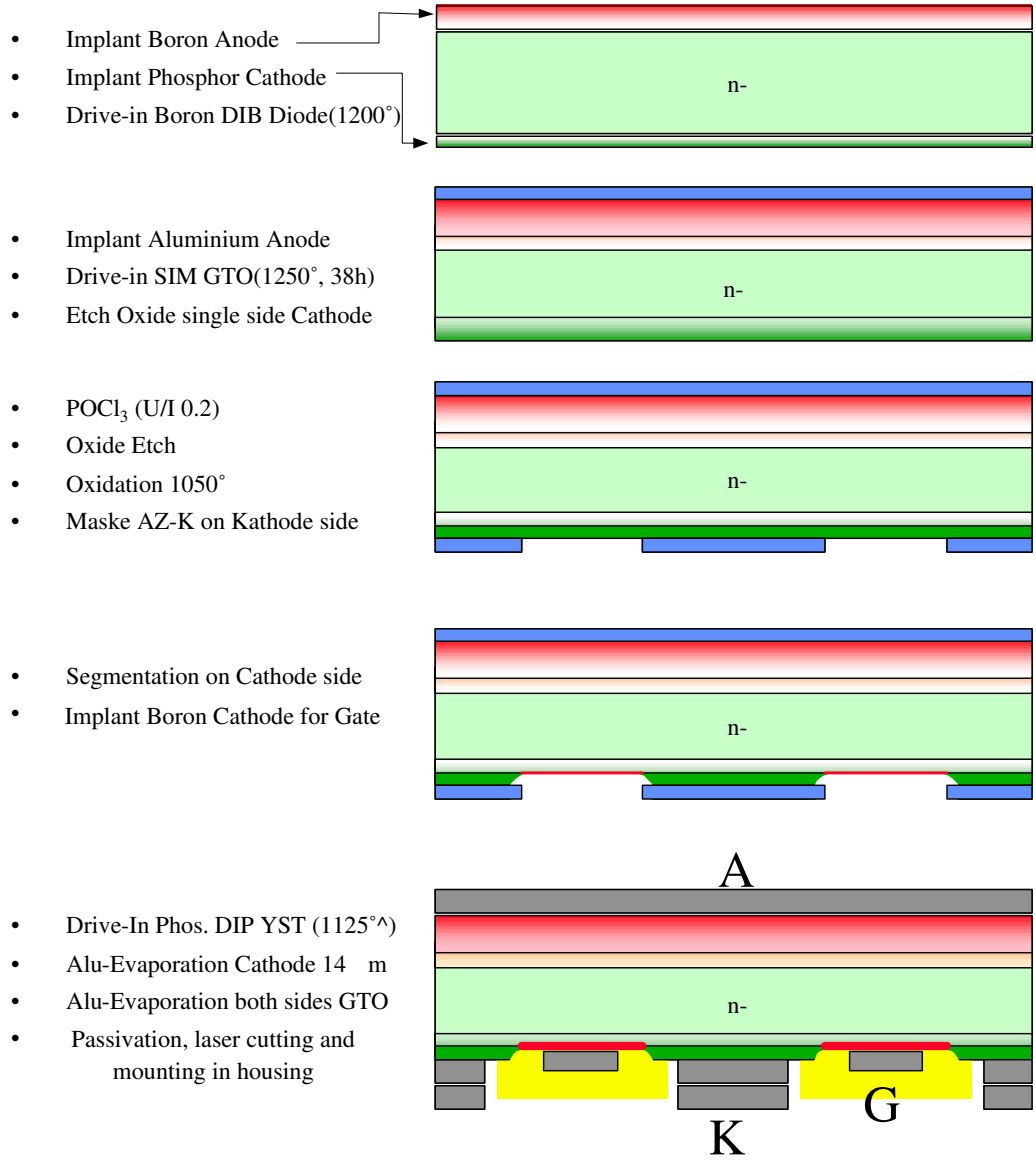



Figure 2.12: Brief overview of the manufacturing phases of a GCD

the profile diagram of the GCD in Fig.2.13, Fig.2.14, Fig.2.15.

At last, the oxidation of the anode emitter is done for its protection. As shown in the Fig.2.12, on the cathode side, phosphorous glass deposition is done at 1125°C for 2 hrs to get a n+ doped layer. After the oxidation at the cathode side, silicon etching (sometimes called as Segmentation or Mesa etching) is done from the cathode side into the n+ doped layer. The etching is done in the n+ cathode layer up to the depth, where it touches the n buffer layer. The approximate depth of etching is around 12$\mu$m. To process the gate emitter, boron implantation is done again from the cathode side. The complete embedding of the p doped gate emitter layer by etching out the n + doped cathode layer offers an essential feature of the new diode structure. The desired gate sensitivity and injection efficiency can be achieved by this construction. After two steps of metalization on the cathode, the passivation, laser cutting and housing for mounting are done to

give the product its final version.

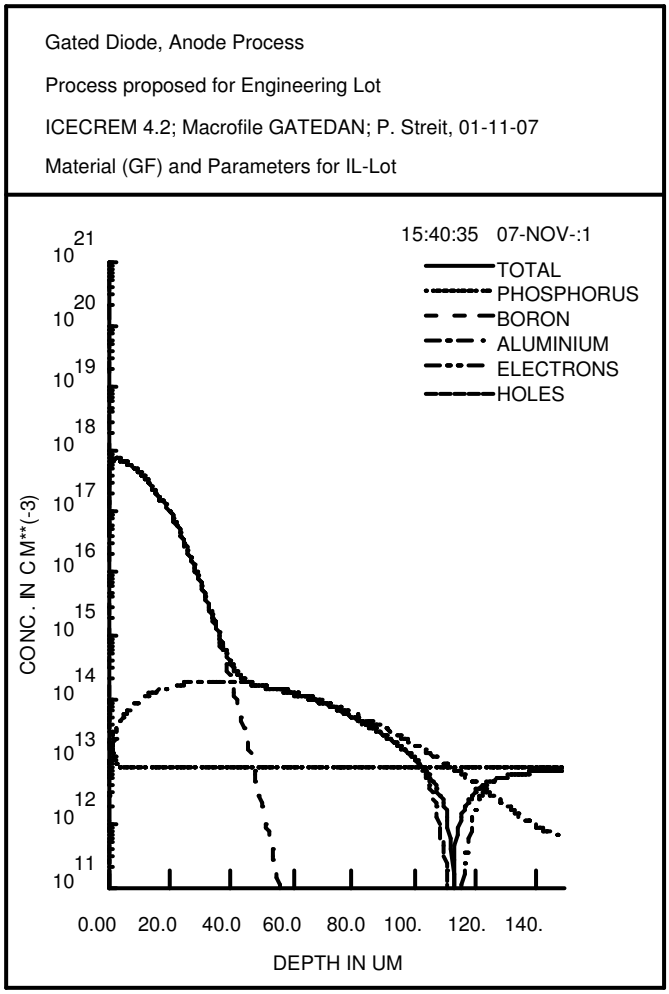



Figure 2.13: Structure of the doping profile at the cross section of the Anode

Fig.2.13, Fig.2.14, Fig.2.15 show the doping profile of the GCD at the cross section of anode, cathode and gate respectively. The anode and cathode of the GCD prototypes have a double profile. The gate doping profile depends on the sensitivity of the gate emitter. Fig. 2.15 shows the doping profile of the gate, which has an intermediate sensitivity. All prototypes of the investigated GCD provided by ABB possess intermediate sensitivity.

## 2.5 Specification of prototypes

The GCD samples for the experimental investigation have been provided by ABB, Switzerland. The following two samples are tested.

- IL226.10 - Non-irradiated type with intermediate gate sensitivity

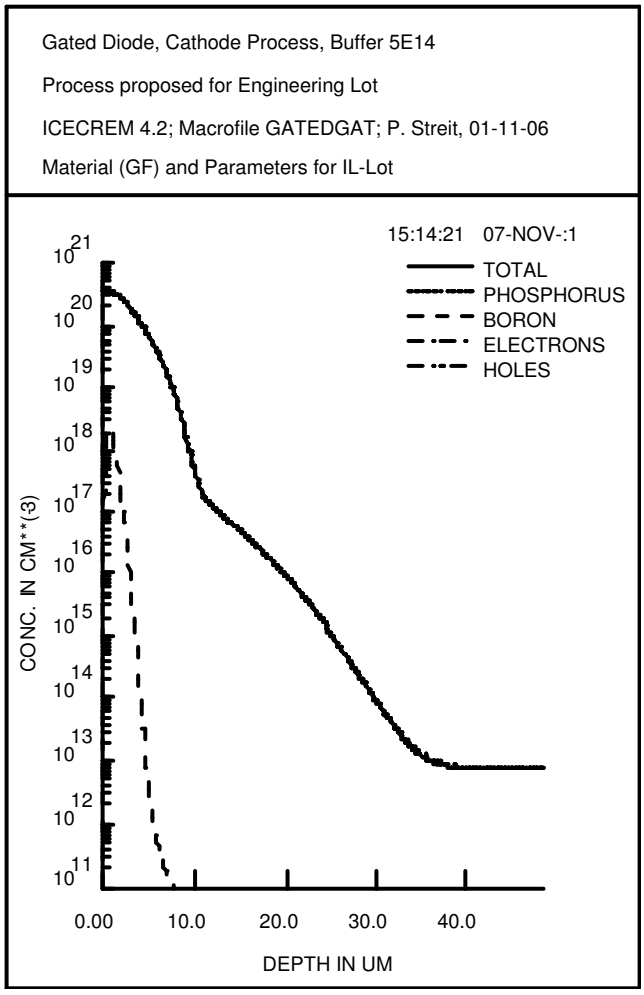



Figure 2.14: Structure of the doping profile at the cross section of the Cathode

- IL 226.13 - Irradiated type with intermediate gate sensitivity

Due to the irradiation, the life time of the minority charge carriers are adjusted. It is clear that the life time adjustment by irradiation influences the reverse recovery time of the GCD. The results in chapter 3 exhibit the difference of the reverse recovery times of the two samples because of their different irradiations.

All GCD prototypes are manufactured through punch through technology. The main electrical characteristics of the investigated GCD samples are

- Repetitive peak reverse voltage ($V_{RRM}$) = 4500 V
- Maximum average on-state current ($I_{FAVM}$) = 1300 A
- Maximum RMS on-state current ($I_{FRMS}$) = 2000 A
- Threshold voltage ($V_{F0}$) = 2.00 V
- On-state resistance ($r_F$) = 0.55 m $\Omega$

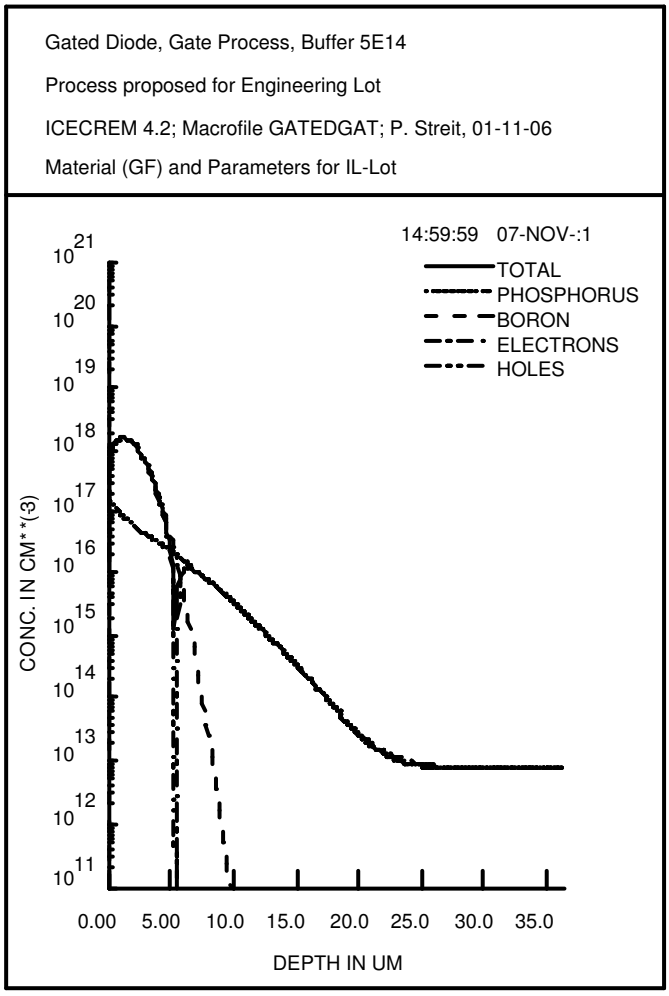



Figure 2.15: Structure of the doping profile at the cross section of the Gate

- Maximum permanent DC voltage ($V_{DClink}$) = 2800 V

Fig. A.1 and Fig. 2.17 show the physical structure of one sample of the GCD using a low inductive gate unit.

## 2.6 Summary

Chapter 2 discussed the structural details of the GCD, its physics of operation during the on-state, blocking state and during turn-off transients. The on-state operation of the GCD is similar to that of a conventional fast diode. The blocking mode of the GCD with inactive gate is comparable to the blocking operation of the conventional diode. During the blocking mode of the GCD, the leakage current of the GCD can be altered by impressed gate current. During the turn-off transient the reverse recovery behavior of the GCD can be influenced by the impression of a gate current.

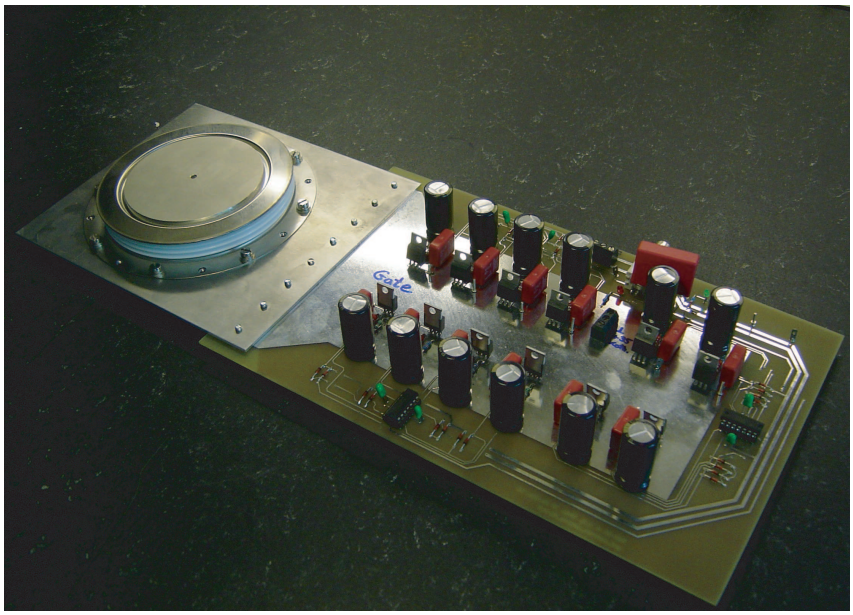



Figure 2.16: Photo of 91mm GCD with universal low inductive gate unit

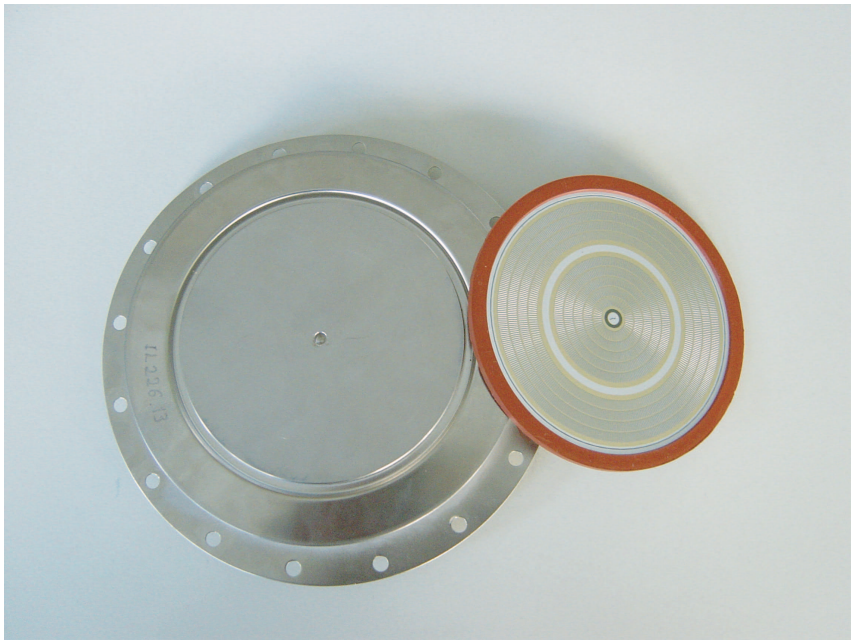


Figure 2.17: Photo of a GCD wafer with press pack case (diameter 85 mm)($V_{RRM}$ = 4.5 kV, $I_{FAVM}$ = 1300A)

# Chapter 3

# Experimental characterization of GCD prototypes

In this chapter, the experimental setups and tests for the electrical characterization of different GCD prototypes are described. Furthermore, these tests results are analyzed. Section 3.1 highlights the key parameters of the specification of the prototypes under test. Section 3.2 describes the test results and the behavior of the GCD prototypes in the on-state. Two given GCD samples are characterized in the blocking mode. The respective test setup and results are explained in section 3.3. These are followed by the results of the investigation of the turn-off behavior in section 3.4.

## 3.1 Specification of GCD prototypes

The samples for the experimental investigation are listed in Table 3.1.

| | Intermediate gate sensitivity |
|---|---|
| Irradiated | IL226.13 |
| Non-irradiated | IL226.10 |

Table 3.1: Irradiation and gate sensitivity of GCD prototype devices

The key parameters of the specification of the GCD samples mentioned in the table 3.1 are

- Repetitive peak reverse voltage $V_{RRM}$ = 4500 V
- Maximum average on-state current $I_{FAVM}$ = 1300 A
- Maximum RMS on-state current $I_{FRMS}$ = 2000 A
- Threshold voltage $V_{F0}$ = 2.00 V
- Slope resistance $r_F$ = 0.55 m $\Omega$
- Permanent DC voltage $V_{DClink}$ = 2800 V
- Maximum gate current $I_{G,GCDM}$ = 400A

## 3.2 On-state behavior of the GCD

The physics of the on-state operation has been already discussed in the previous chapter. It was explained that the on-state operation of a GCD without active gate is similar to that of a conventional fast diode (Figure 3.1). It has been explained that the influence of an additional positive gate current can be neglected. Thus, the on-state characteristic of a GCD can be described by the linear approximation

$V_F = V_{FO} + r_F . I_F$
where, $V_{FO}$ : On-state threshold voltage, $r_F$ : On-state forward resistance

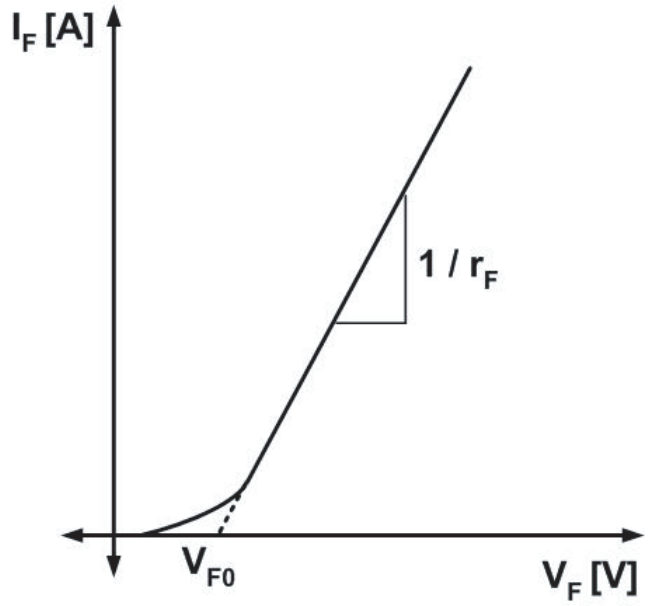



Figure 3.1: On-state characteristic and linear approximation of a GCD

The nature of the plot in Figure 3.1 is well related to the physical structure of a power diode. In the discussion of the on-state characteristics, the width of the n-base region (also called as 'drift region') plays a significant role. The voltage drop $V_F$ during the on-state consists of the sum of the voltage drops of $V_{diff}$ and $V_{ohm}$. The p-n junction diffusion voltage $V_{diff}$ depends on the doping of both the pn-junction sides. In the case of the 4.5kV GCD, the ohmic part prevails like in conventional medium voltage fast diodes. The ohmic resistance ($r_F$) results basically from the thickness of the lightly doped n-drift region. To achieve a low ohmic voltage drop a high injection efficiency and the smallest possible base width structure have to be chosen for a given blocking voltage [1],[10].

As mentioned in the previous chapter, several methods like charge carrier life time control, emitter efficiency control or specific doping techniques are used to adjust the steady and dynamic characteristics of a medium voltage diode [10]. Similar methods can be applied to the GCD to achieve a good performance in steady and dynamic states. Electron irradiation is a commonly applied technique to adjust the turn-off switching speed of the device by generating recombination centers in the material. The two samples under test differ with respect to

their irradiation level. The generation of more recombination centers with an electron irradiation controls mainly the lifetime of the minority charge carriers and ultimately the switching time. A trade-off in the effect of the irradiation process has to be achieved between the leakage current, the forward voltage drop and the desired switching time for a fast diode. The sample IL226.13, which is irradiated has a higher on-state voltage drop and shorter turn-off times than the non-irradiated sample IL226.10.

### 3.2.1 Results of measurements

Due to the similar device and mechanical structure, the on-state characteristics of the GCD sample IL226.10 and IL226.13 are very similar to that of a corresponding irradiated 91mm (4500V,1300A) diode 5SDF 16L4502.

Appendix B contains the data sheet of the commercially available diode 5SDF 16L4502.

Characteristics of the on-state behavior of both GCD samples are summarized in Table 3.2 and 3.3.

| On-state | IL 226.13 (Irradiated) | | | |
|---|---|---|---|---|
| $V_F$ | Forward voltage drop | $\leq$ 5.0 V | $I_F$ = 3000A | $T_j$ = 115 °C |
| $V_{FO}$ | Threshold voltage | 3.0 V | Approximation for | |
| $r_F$ | Slope resistance | 0.55 m$\Omega$ | $I_F$ = 1000...3000A | |

Table 3.2: On-state data of irradiated GCD prototype IL226.13 (at $I_{G,GCD}$ = 0)

| On-state | IL 226.10 (Non-irradiated) | | | |
|---|---|---|---|---|
| $V_F$ | Forward voltage drop | $\leq$ 3.0 V | $I_F$ = 3000A | $T_j$ = 115 °C |
| $V_{FO}$ | Threshold voltage | 1.0 V | Approximation for | |
| $r_F$ | Slope resistance | 0.55 m$\Omega$ | $I_F$ = 1000...3000A | |

Table 3.3: On-state data of non-irradiated GCD prototype IL226.10 (at $I_{G,GCD}$ = 0)

## 3.3 Blocking behavior of the GCD

When the GCD is reverse biased and the gate is not effective ($I_{G,GCD} \leq 0$, $V_{GK} \leq 0$), only a negligible small leakage current ($I_{DR}$) flows through the device, similar to that of a conventional power diode. The leakage current at a given blocking voltage and junction temperature is determined by the structure of the device, the doping profile and the edge passivation. The basic effect of the influence of a positive impressed gate current $I_{G,GCD}$ in the blocking state is explained in chapter 2.

### 3.3.1 Experimental set up and test procedure

Figure 3.2 shows the test circuit for the characterization of the GCD prototypes during the blocking state. A photograph of the physical test setup is shown in Figure 3.3.

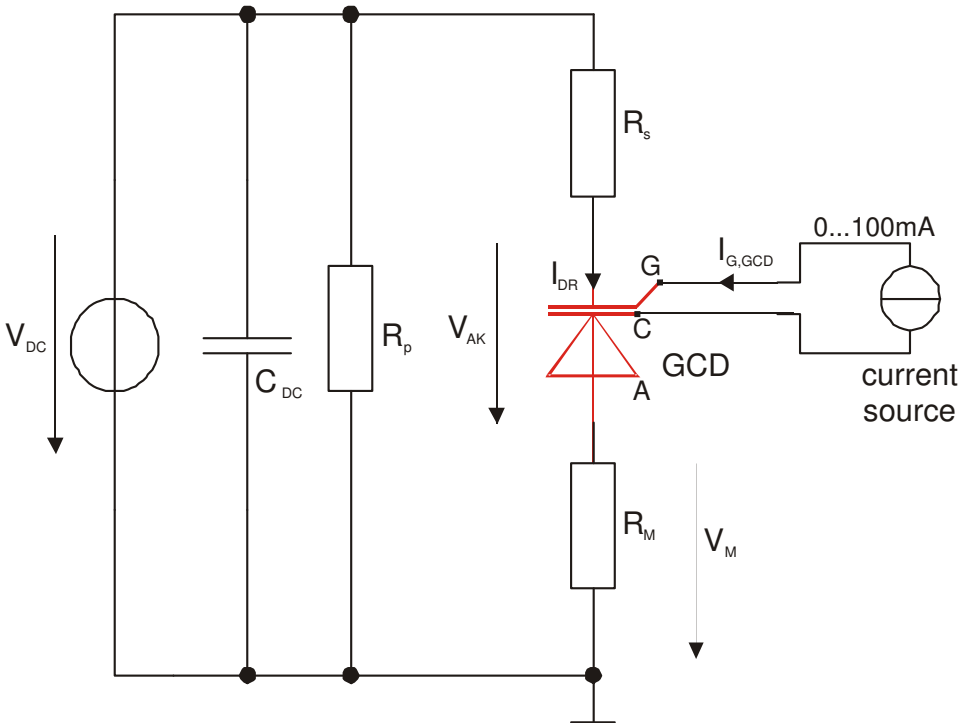



Figure 3.2: Test circuit for the measurement of leakage currents ($V_{DC}$ = 2kV, $R_p$ = 10 kΩ , $R_s$ = 10 kΩ, $R_M$ = 1 kΩ, $I_{G,GCD}$ = 0 to 100 mA)

As depicted in Fig. 3.2, a high voltage power supply charges the DC link capacitor $C_{DC}$ to the desired blocking voltage $V_{DC}$. Since the charging device is unable to discharge the capacitor after the measurement of the blocking current, a resistor $R_P$ ($10k\Omega$) is connected in parallel to the DC link capacitor. The value of this resistance is a trade-off between the charging and discharging time. The resistance $R_S$ (e.g. $10k\Omega$) is connected in series to the GCD to limit the short circuit current in the event of a failure of the GCD. The value of $R_S$ is chosen to be less than 10 % of the blocking resistance of the GCD under test.

The leakage current is measured using a shunt resistor $R_M$ connected in series to the GCD. The value of $R_M$ ($1k\Omega$ or $10k\Omega$) is selected such that there will be a voltage drop across it, which can be measured by the applied storage oscilloscope. During the measurement of the leakage current of the GCD, the temperature of the device is controlled by two temperature controlled isolated cylindrical heaters as shown in Fig. 3.3.

As explained earlier the leakage current $I_{DR}$ is dependent on the injected gate current $I_{G,GCD}$, the junction temperature $T_j$ and the diode voltage $V_{AK}$. To analyze the behavior of the GCD in its blocking mode, both prototypes are tested for junction temperatures $T_j$ of 25°C, 85°C and

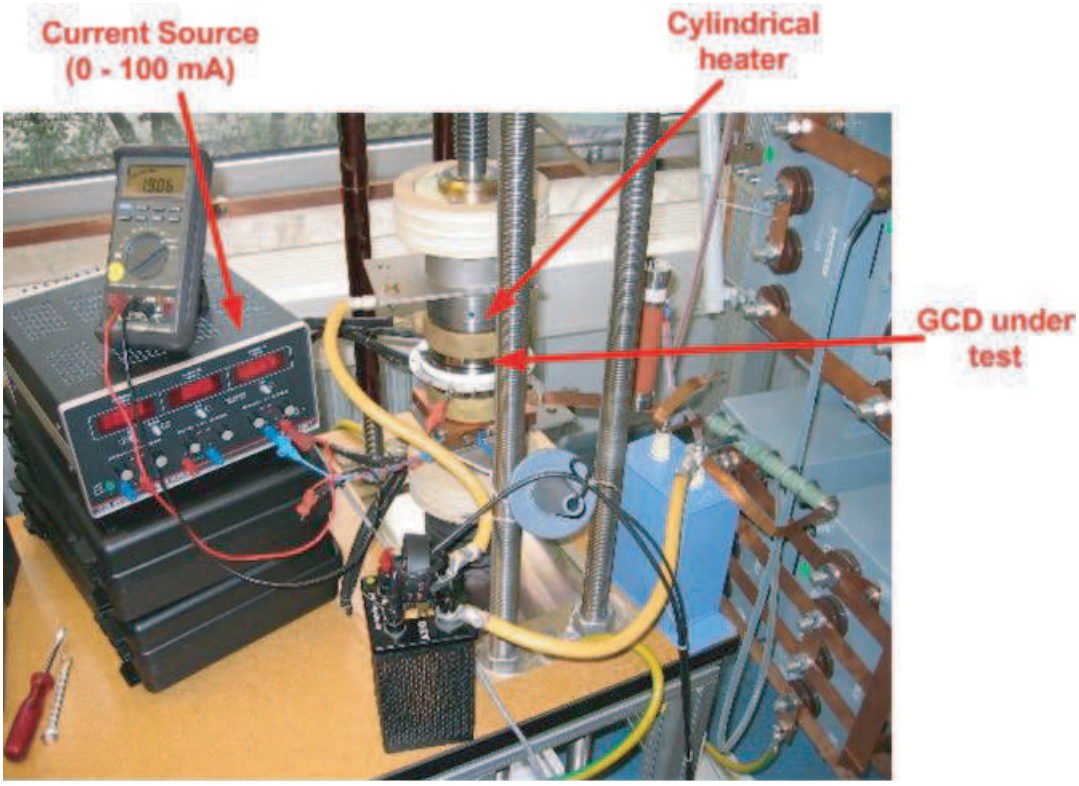



Figure 3.3: Photograph : Test setup for Blocking behavior measurements of the GCD

115°C in a blocking voltage range of $V_{KA}$ = 500V to 2.4 kV. For all predefined temperatures and voltages, a set of leakage current measurements has been carried out with different values of injected gate currents $I_{G,GCD}$ ranging from 0 mA to 100 mA.

### 3.3.2 Test results - Blocking behavior

Figures 3.4(a) to 3.4(c) and Figures 3.5(a) to 3.5(c) depict the leakage current variation for the respective device voltage $V_{AK}$ at different junction temperatures for both GCD samples. Figure 3.4(d) and Figure 3.5(d) show the leakage current $I_{DR}$ as a function of the gate current $I_{G,GCD}$ for a device voltage of $V_{AK}$ = 2.4 kV.

It can be seen from Figure 3.4 and Figure 3.5 that without any GCD gate current injection ($I_{G,GCD}$ = 0), the leakage current $I_{DR}$ is similar to that of the power diode 5SDF 16L4502. For example a leakage current of $I_{DR} \leq$ 50 mA is specified for the diode 5SDF 16L4502 at $T_j$ = 115°C, $V_{AK}$ = 4.5 kV. The GCD samples GCD IL226.10 and GCD IL226.13 have leakage currents of $I_{DR} \leq$ 10 mA and $I_{DR} \leq$ 40 mA at $T_j$ = 115°C and $V_{AK}$ = 2.4 kV if the gate is not effective ($I_{G,GCD}$ = 0)

As the temperature increases, the leakage current of a conventional power diode also increases [22]. It can been seen from the GCD results shown in the figures 3.4 and 3.5 , that as the temperature increases with zero gate current injection, the leakage current also increases. Figure

3.4 and Figure 3.5 clearly show that also the leakage currents of GCDs increases with and without the impression of additional gate currents. Like expected the GCD leakage currents also increase with increasing gate currents in the applied investigated voltage and junction temperature range. The function $I_{DR}$ = f($I_{G,GCD}$) for different junction temperatures in Figure 3.4(d) and Figure 3.5(d) are almost linear for $I_{G,GCD} \geq$ 10-20 mA. The influence of the junction temprature on the leakage current is drastically higher in the irradiated GCD IL226.13. The leakage current gain

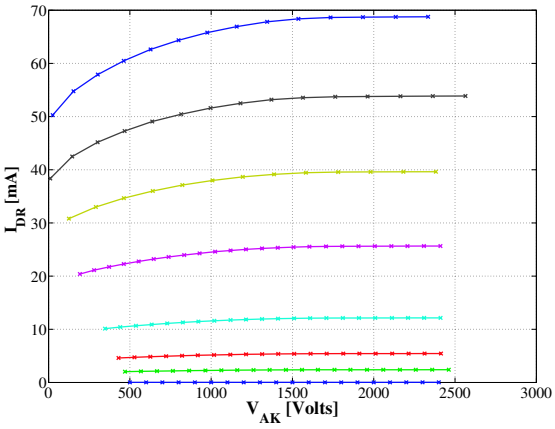
$$\beta = \Delta I_{DR} / \Delta I_{G,GCD} \tag{3.1}$$

for both GCDs are summarized in Table 3.4. It can been seen that the current gain factor ($\beta$) is in a range of 0.68 - 0.82 and 0.58 - 1 for the non-irradiated and irradiated GCDs respectively. Obviously the gate sensitivity is comparable for both samples of the GCDs.

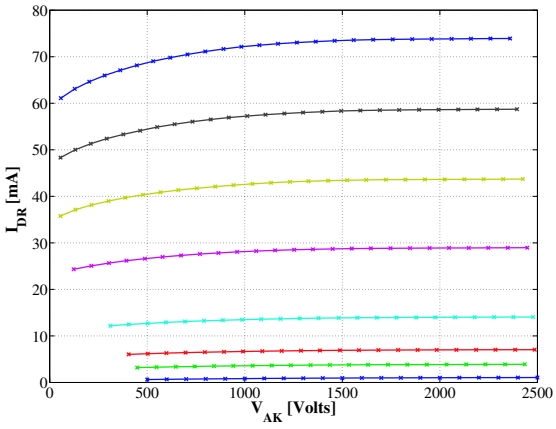
Maximum leakage currents of 69 to 82 mA and 56 to 111 mA appeared for the non irradiated GCDs IL226.10 and irradiated GCD IL226.13 in junction temperature range of $T_j$ = 25° - 115°C at a maximum impressed gate current of $I_{G,GCD}$ = 100 mA respectively.

| | Leakage current gain $\beta$ | |
|---|---|---|
| $T_j$ (° C) | IL226.10 | IL226.13 |
| 25 | 0.68 | 0.58 |
| 85 | 0.74 | 0.68 |
| 115 | 0.82 | 1 |

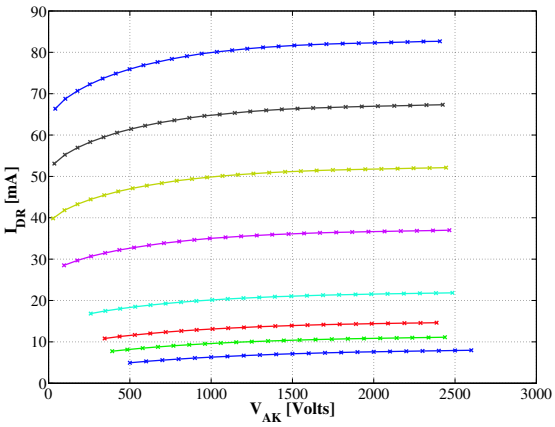
Table 3.4: Leakage current gains of GCDs. (10 mA $\leq I_{G,GCD} \leq$ 100mA)



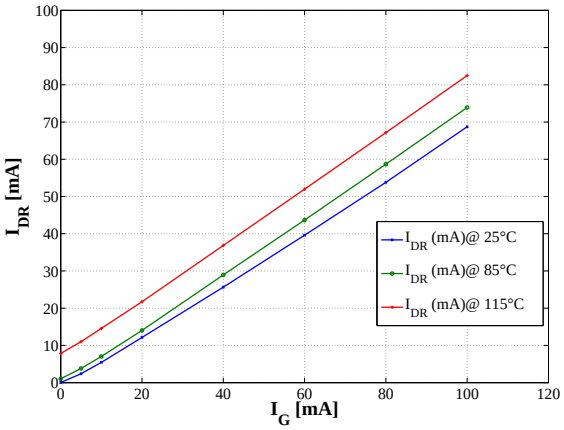

(a) $I_{DR}$ Vs $V_{AK}$ @ $T_j$ = 25°C




(b) $I_{DR}$ Vs $V_{AK}$ @ $T_j$ = 85°C




(c) $I_{DR}$ Vs $V_{AK}$ @ $T_j$ = 115°C




(d) $I_{DR}$ Vs $I_{G,GCD}$ @ $V_{DC}$ = 2kV, $T_j$ = 25°C, 85°C, 115°C

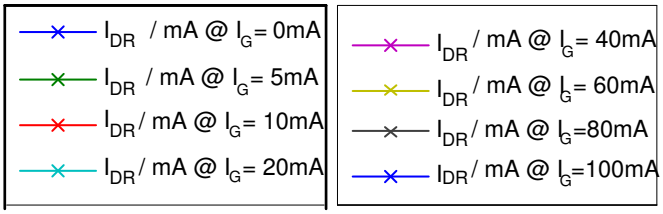
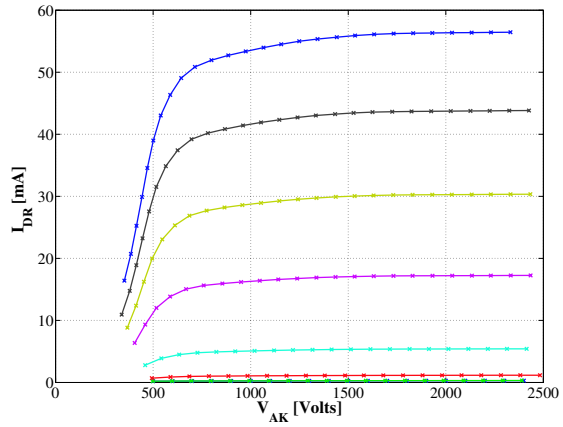


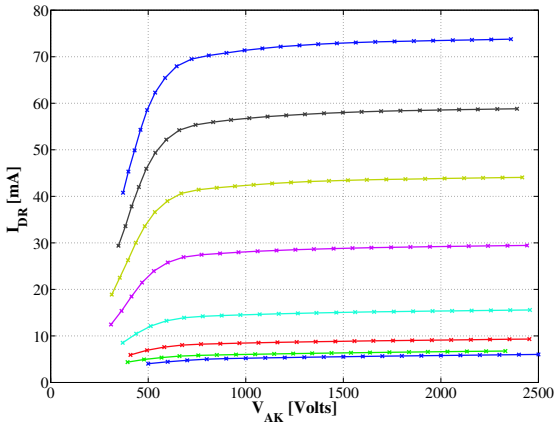

Figure 3.4: Leakage currents of the non irradiated GCD IL226.10 as a function of the device voltage (a-c) and gate current (d) @ $T_j$ = 25°C, 85°C, 115°C

## 3.4 Reverse recovery behavior of GCDs

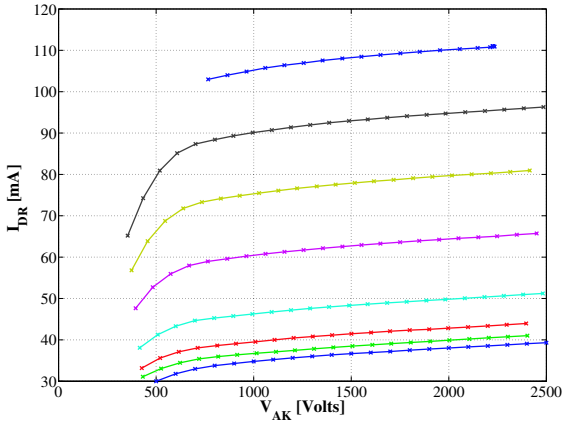
The diode internal physical effects of the reverse recovery during the transition from the conduction state to the blocking state of the GCD is explained in chapter 2. This chapter presents results of the experimental investigation of the GCD reverse recovery process. Especially, the influence of an impressed gate current is investigated. The investigation and analysis are explained for the GCD IL226.10. For the sample IL 226.13 identical measurements are carried



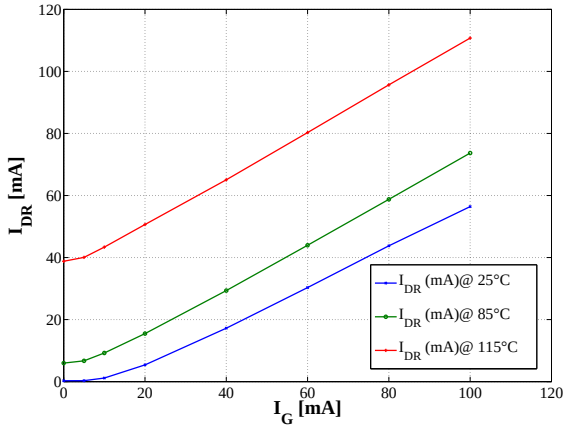

(a) $I_{DR}$ Vs $V_{AK}$ @ $T_j$ = 25°C




(b) $I_{DR}$ Vs $V_{AK}$ @ $T_j$ = 85°C




(c) $I_{DR}$ Vs $V_{AK}$ @ $T_j$ = 115°C




(d) $I_{DR}$ Vs $I_{G,GCD}$ @ $V_{DC}$ = 2kV, $T_j$ = 25°C, 85°C, 115°C

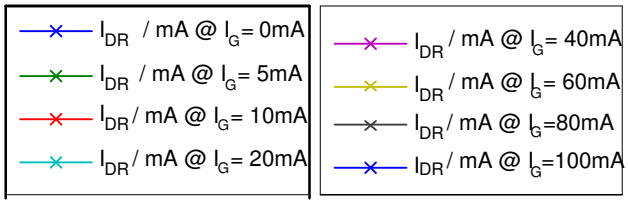



Figure 3.5: Leakage currents of the irradiated GCD IL226.13 as a function of the device voltage (a-c) and gate current (d) @ $T_j$ = 25°C, 85°C, 115°C

out. The complete test results of both the samples in tabular form are incorporated in Appendix C.

### 3.4.1 Experimental set up and test conditions

The test circuit for the investigation of the reverse recovery behavior of the GCD is shown in Fig. 3.6. Figure 3.7 shows the physical arrangement of the test setup for the turn-off measure-

ments of the GCD.

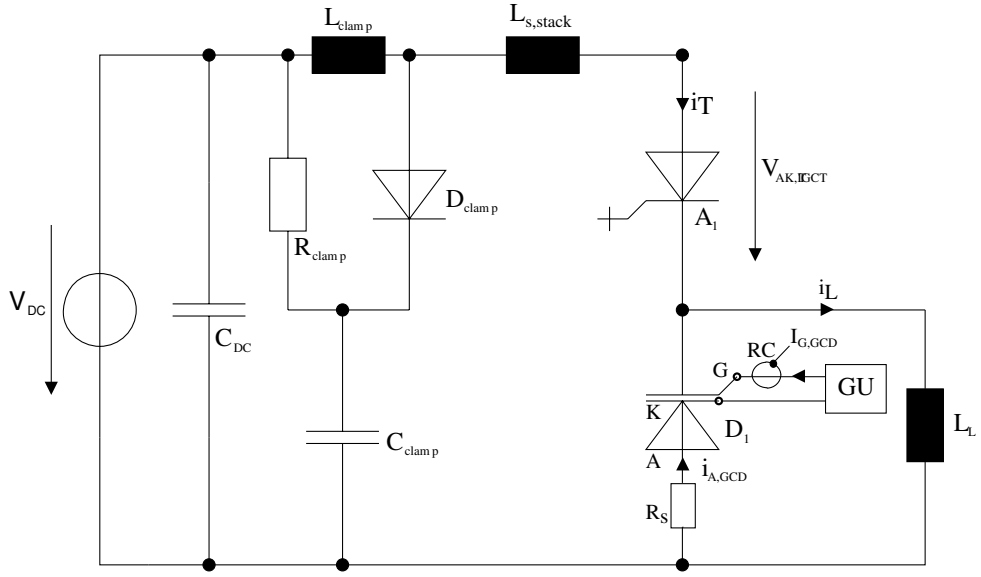



Figure 3.6: Test circuit for the investigation of the reverse recovery behavior of the GCD ($V_{DC}$ = 2kV, $I_L$ = 500A, 1300A, $L_{clamp}$ = 5.6 $\mu$ H , $R_{clamp}$ = 1.25 $\Omega$, $C_{clamp}$ = 2.5 $\mu$ F , $L_L$ = 1 mH, IGCT - 4.5 kV/5SHY35L4503 , GCD - IL226.10 / IL226.13)

The test circuit is basically a buck converter with an IGCT (4.5kV / 5SHY 35L4503) as active switch. The GCD replaces the conventional free-wheeling diode. For the commutation of $I_L$ from the GCD to the IGCT after an active turn-on transient, the rise of current was limited to rate of current rise of $di_T/dt$ = 350 A / $\mu$s by selecting the value of the clamp inductance to $L_{clamp}$ = 5.6 $\mu H$. The size of the load inductance is selected to ensure nearly a constant load current during the commutation. The chosen value of $L_H$ = 1 mH yields a rate of current rise of $di_L/dt$ = 2 A / $\mu$s during the ramp up of the load current.

During the reverse recovery process of the GCD, a specific shaped gate current pulse is injected by the gate unit into the GCD. To enable the impression of different gate current shapes and durations, a low inductive universal gate unit contains a voltage controlled current source. To simplify the investigation basically a rectangular (or trapezoidal) gate current pulse is considered. A rectangular gate current waveform was chosen as a reference waveform, since investigations of different gate current waveforms (e.g. triangular, sawtooth) showed that basically the impressed charge amount and the time point of the charge impression related to the interruption of the reverse recovery current are the most important gate current parameters. Obviously, a rectangular gate current enables a simple and linear adjustment of these parameters while it can be generated using a simple current source. Figure 3.9 shows the impact of different shaped gate currents on the reverse recovery behavior of the GCD.

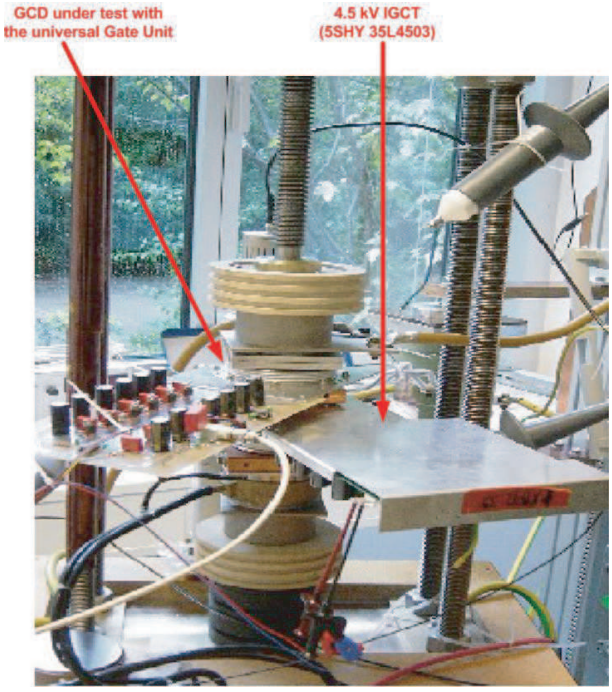



Figure 3.7: Physical stack test setup for reverse recovery measurements of GCDs

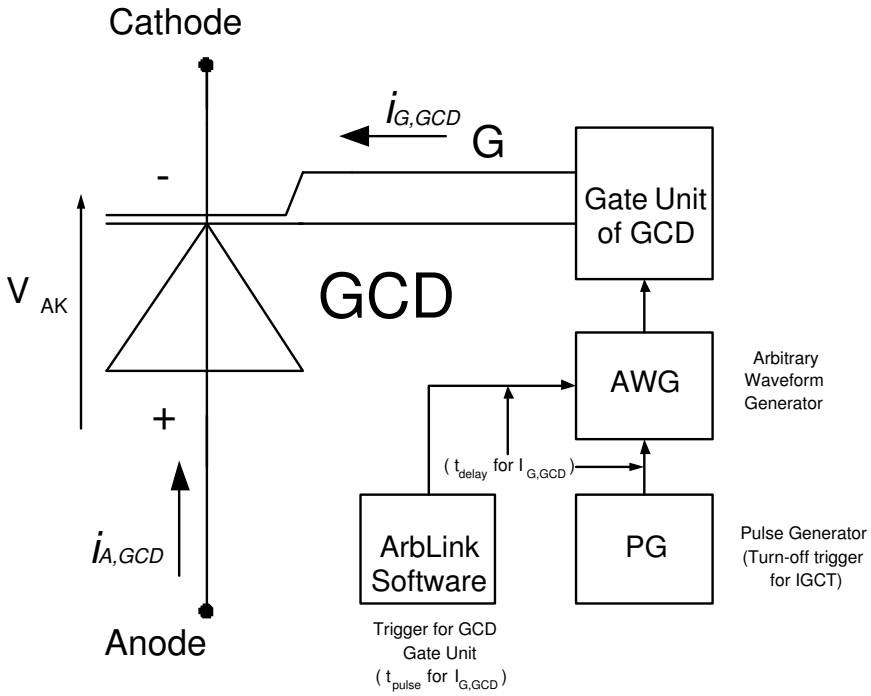



Figure 3.8: Block diagram : Gate current injection of GCD

Figure 3.8 shows the block diagram of the gate current generation. Figure 3.10 shows the turn-off current waveform of the GCD explaining the parameters used in association with a rectangular gate current such as $t_{pulse}$ and $t_{delay}$. It can be seen from the block diagram in Figure 3.8 that at first a rectangular input gate current with a desired pulse length $t_{pulse}$ is generated.

This pulse is generated by the ArbLink software program on the PC. Then it is transmitted to the arbitrary waveform generator (AWG) for the adjustment of the amplitude of the gate current ($I_{G,GCD}$). The trigger pulse for the turn-on of IGCT is generated by the pulse generator (PG). The synchronization of the pulse generation for the IGCT and the GCD enables an adjustment of the time interval $t_{delay}$, which is between the time when the IGCT is turned on (i.e. the time when the IGCT gets the turn-on trigger pulse) and the time, when the gate current of the GCD is injected. The adjustment of the IGCT turn-on signal and the GCD turn-on signal also enables an adjustment of the time interval $t_{delay}$ between the zero crossing of the GCD anode current and the impression of the GCD gate current. This way a simple open-loop control for the GCD gate current pulse is achieved. The influences of the parameters delay time $t_{delay}$, pulse length $t_{pulse}$ and pulse amplitude of impressed rectangular (or trapezoidal) gate current $I_{G,GCD}$ on the reverse recovery behavior of the GCD are investigated.

The physical arrangement of the gate unit is shown in Figure 2.10. The key parameters of the gate unit of the GCD prototype are

- range of gate unit input voltage $V_{GU}$ = 0 - 5 V (of desired waveform)
- range of gate current $I_{G,GCD}$ = 0 - 228 A
- conversion factor F = $I_{G,GCD}$ / $V_{GU}$ = 45 A / V
- maximum rate of rise of gate current (d$i_G$ / $dt$) = 550 A / $\mu s$
- maximum gate current $I_{G,GCDM}$ = 390 A
- delay time of the gate unit $t_d$ = 300 ns

Appendix [A] summarizes a sample measurement of the gate unit, its physical layout and the connection details to the gate unit of the GCD prototype. It also shows the circuit diagram and the PCB layout for the gate unit.

To analyze the effect of an injected gate current on the reverse recovery behavior, characteristic parameters are defined with reference to the reverse recovery process of a conventional diode. Fig. 3.10 shows the principle reverse recovery waveform including different time interval specifications. Like mentioned before the impression of a rectangular gate current is assumed.

The definitions of the selected characteristic parameters are given below :

- $t_{pulse}$ ($\mu s$) : Duration of the impressed rectangular gate current pulse
- $t_{delay}$ ($\mu s$) : Delay time between the zero crossing of the anode current (t = 0) and the impression of the gate current pulse
- $t_s$ : Time interval between zero crossing of the anode current and maximum peak reverse recovery current.
- $t_f$ : Time interval between the maximum reverse recovery current to the end of the reverse recovery time

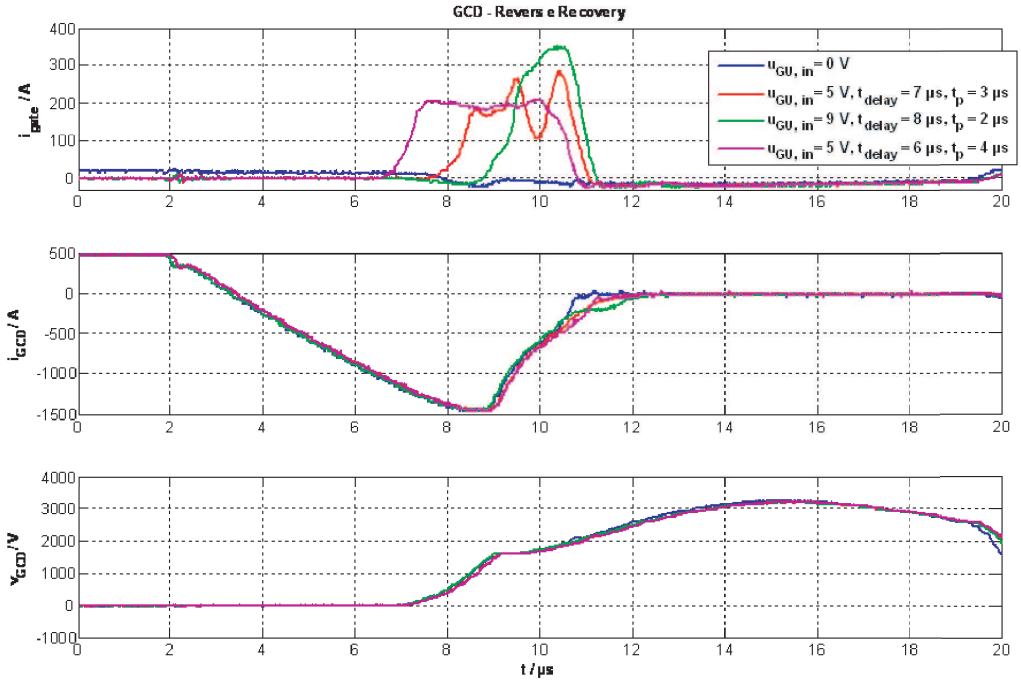



Figure 3.9: GCD reverse recovery behavior at different injected gate current shapes ($V_{DC}$ = 2kV, $I_L$ = 500A, $T_j$ = 25°C, GCD IL226.10)

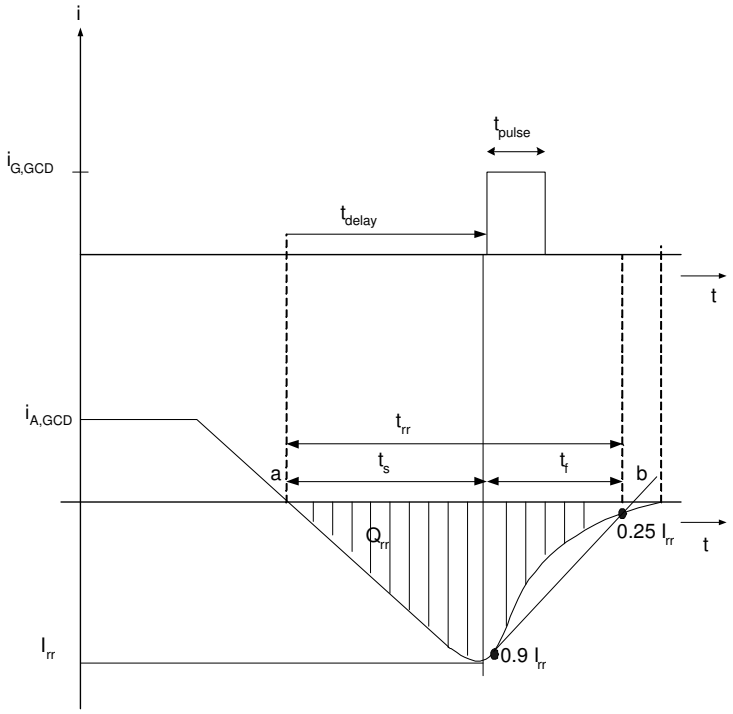



Figure 3.10: Specification of characteristic values for the investigation of the reverse recovery behavior of a GCD

- $t_{rr}$ : ($t_{rr}$ = $t_S$ + $t_f$) Reverse recovery time. It is defined as the time interval between the

anode current zero crossing and the time between 0.9 $I_{rr}$ and 0.25 $I_{rr}$.

- Softness factor S : Measure of the softness of the reverse recovery behavior of the GCD

$$S = \frac{t_f}{t_s} \tag{3.2}$$

- $I_{A,GCD}$ (A) : Anode current of the GCD
- $I_{G,GCD}$ (A): Impressed GCD gate current (A)
  $I_{G,GCD} \cong 45$ . Gate unit input voltage ($V_{GU}$)
- $Q_{rr}$ (mAs): Reverse recovery charge of the GCD

$$Q_{rr} = \int_0^{t_{rr}} I_{rr} dt \tag{3.3}$$

- $Q_{rr,NOGU}$ (mA) : Reverse recovery charge of the GCD without impressed gate current($I_{G,GCD}$ = 0)
- $Q_{rr,Difference}$ (mAs) : Difference between the reverse recovery charges of the GCD with and with out impressed gate currents (i.e.$Q_{rr,Difference}$ = $Q_{rr}$ - $Q_{rr,NOGU}$)
- $Q_{Gate}$ (mAs) : Impressed gate unit charge

$$Q_{Gate} = \int_{t_{delay}}^{t_{delay}+t_{pulse}} I_{G,GCD} dt \tag{3.4}$$

- $\eta_Q$ : Charge efficiency ( $\eta_Q$ = $Q_{rr,Difference}$ / $Q_{Gate}$)
- $W_{off,GCD}$ (Ws) : Turn-off losses of the GCD

Referring to the above definitions, the samples are tested under the following test conditions.

- Prototypes under measurement : IL 226.10, IL 226.13
- DC Link Voltage : $V_{DC}$ = 2kV
- Anode current of GCD : $I_{A,GCD}$ = 500A, 1300A
- Junction temperatures : $T_j$ = 25°C, 85°C, 115°C
- Impressed gate currents of the GCD : $I_{G,GCD}$ = 200A, 300A
- Gate current pulse lengths : $t_{pulse}$ = 1$\mu s$,2$\mu s$,5$\mu s$,10$\mu s$
- Gate current pulse delays : $t_{delay}$ = - 0.2$\mu s$ to 4$\mu s$
- Shape of gate current regulated voltage : rectangular
- Values of clamp : $R_{clamp}$ =1.25$\Omega$, $C_{clamp}$ = 2.5$\mu F$, $L_{clamp}$ = 5.6$\mu H$,
- Load : $L_L = 1mH$

### 3.4.2 Experimental investigation of the reverse recovery behavior

In this section selected results of the experimental investigation of the sample IL226.10 are described. The effect of various parameters like DC voltage, load current, junction temperature and the gate current is investigated. The experimental results of both samples are summarized in tabular form in Appendix [C].

The measurement data during the turn-off of the GCD were stored and analyzed by MATLAB.

**Effect of $t_{delay}$ on $Q_{rr,Difference}$**

Fig 3.11 shows the turn-off waveform at 2kV, 1300A. It shows the effect of an injected gate current at different delay times on the reverse recovery charge at $T_j$ = 25°C for the sample IL226.10.

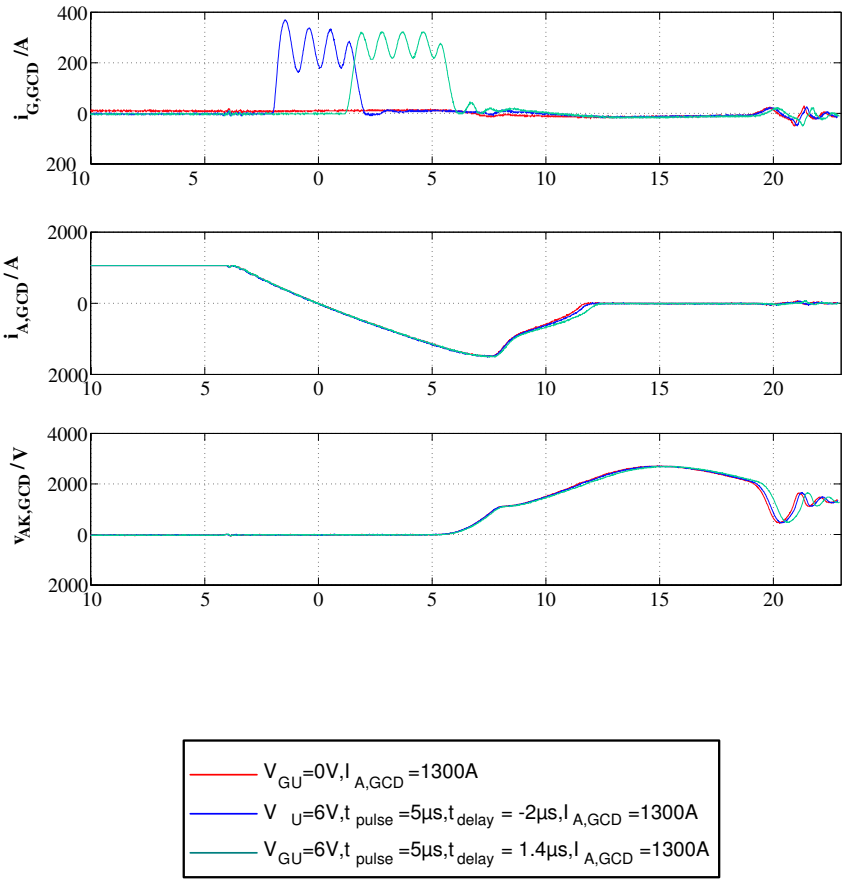
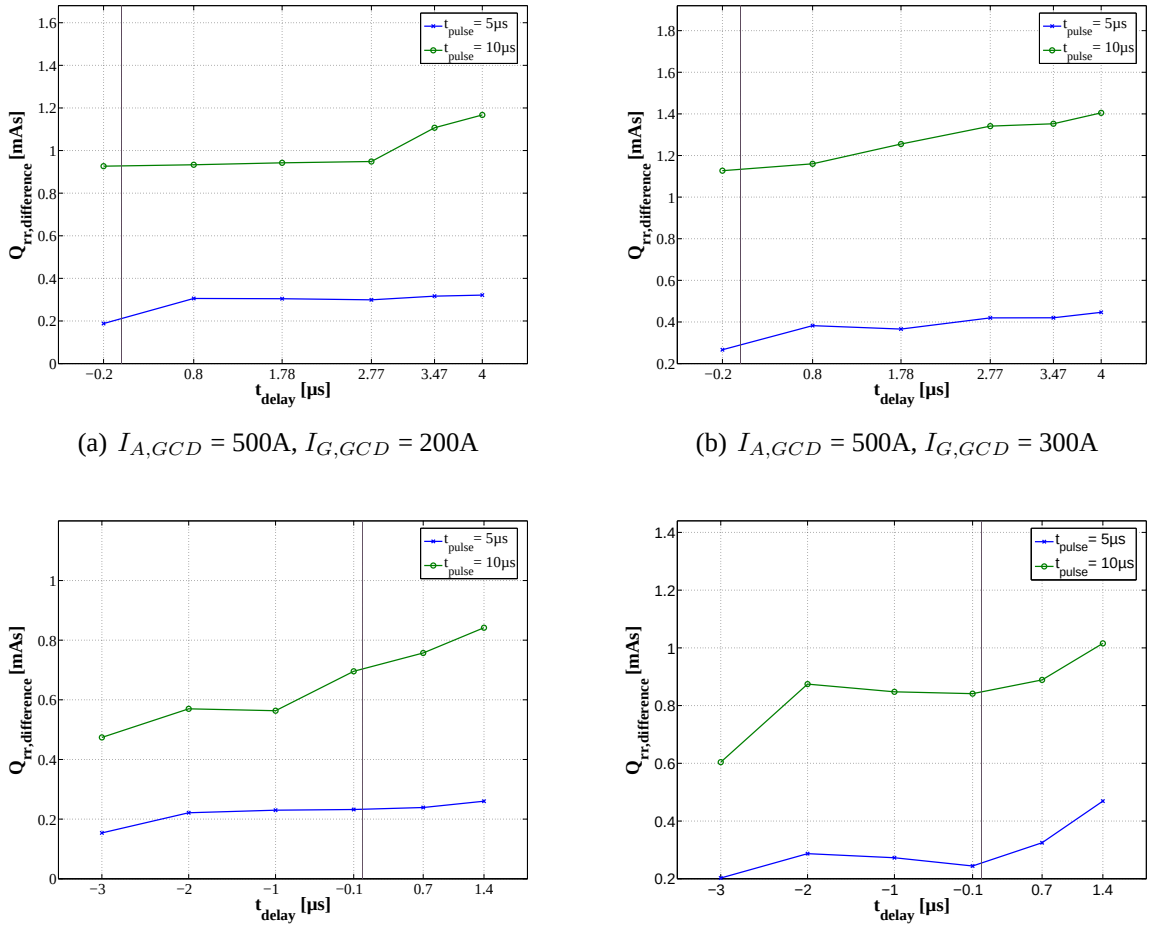



Figure 3.11: GCD Turn-off current and voltage waveforms (Device : IL226.10, $V_{DC}$ = 2kV, $I_L$ = 1300A, $T_j$ = 25°C, $I_{G,GCD}$ = 300A, $t_{pulse}$ = 5$\mu$s, $t_{delay}$ = -2 $\mu$ s, 1.4 $\mu$ s)

The waveforms of Figure 3.11 show that the impression of an external gate current smooths the reverse recovery current during the last part of the interval $t_f$. The impression of the gate current at $t_{delay}$ = 1.4 $\mu$ s influences the reverse recovery current more than at the delay time $t_{delay}$

= -2 $\mu$ s. Although, the gate current is impressed before the reverse recovery current reaches its peak, the maximum reverse recovery current $I_{rr}$ is not influenced by the impression of the gate current.

Figure 3.12 shows the function of $Q_{rr,Difference}$ = f($t_{delay}$) for a load currents of $I_L$ = 500A and 1300A and gate currents of $I_{G,GCD}$ = 200A and 300A. The reverse recovery charge $Q_{rr}$ and the charge $Q_{rr,Difference}$ increase with the increasing parameter $t_{delay}$.




(a) $I_{A,GCD}$ = 500A, $I_{G,GCD}$ = 200A

(b) $I_{A,GCD}$ = 500A, $I_{G,GCD}$ = 300A

(c) $I_{A,GCD}$ = 1300A, $I_{G,GCD}$ = 200A

(d) $I_{A,GCD}$ = 1300A, $I_{G,GCD}$ = 300A

Figure 3.12: IL226.10 - $Q_{rr,Difference}$ = f($t_{delay}$) ($V_{DC}$ = 2 kV, $I_{A,GCD}$ = 500A / 1300A, $T_j$ = 25°C)

The charge efficiency, which quantifies the effectiveness of the injection of the gate current for getting a soft tail of the reverse recovery current is shown in Table 3.5. Obviously, the charge efficiency is increased by 20 %, if the gate current pulse is identical at $t_{delay}$ = 1.4 $\mu$ s compared to $t_{delay}$ = -2 $\mu$ s assuming an identical gate current pulse.

The reason for the less efficient gate current injection at negative or low delay times is the

| $t_{delay}$ | $Q_{rr,Diff}$ | $Q_{Gate}$ | charge efficiency ($\eta$ = $Q_{rr,Diff}$ / $Q_{Gate}$ ) |
|---|---|---|---|
| -2$\mu$s | 0.287 $\mu$As | 0.903 $\mu$As | 31% |
| 1.4$\mu$s | 0.469 $\mu$As | 0.903 $\mu$As | 51% |

Table 3.5: Charge efficiency with different $t_{delay}$ for IL226.10
($V_{DC}$ = 2kV, $I_{A,GCD}$ = 1300A, $T_j$ = 25°C, $I_{G,GCD}$ = 300A, $t_{pulse}$ = 5$\mu$s, $t_{delay}$ = -2 $\mu$ s, 1.4 $\mu$ s)

increased recombination of charge carriers until the time point, where the interruption of the reverse recovery current is smoothed ( approx. 0.6. $I_{rr}$ in Figure 3.10). It can be concluded that the impression of a GCD gate current is most effective immediately before the time point, when the smoothing effect of the reverse recovery current appears. If the GCD gate unit should automatically detect a suitable time point of a gate current injection, then the rise of the diode voltage $V_{AK}$ or the appearance of the peak reverse recovery current could be detected.

**Effect of $t_{pulse}$ on $Q_{rr,Difference}$**

Figure 3.13 shows a GCD turn-off waveform at $V_{DC}$ = 2 kV, $I_L$ = 1300 A and $T_j$ = 25°C for the prototype IL226.10 at different pulse lengths of the injected gate current $I_{G,GCD}$.

Among the affecting parameters of the impressed gate current on the soft reverse recovery behavior, $t_{pulse}$ is a very important factor. The softness factor, which describes the softness of a recovery process, changes in the turn-off transients from S = 0.4 ($I_{G,GCD}$ = 0) to S = 0.42 ($t_{pulse}$ = 5 $\mu$ s) and S = 0.5 ($t_{pulse}$ = 10 $\mu$ s).

Figure 3.14 shows the relation between $Q_{rr,Difference}$ and the gate current pulse duration $t_{pulse}$ for different delay times $t_{delay}$ and load currents $I_L$ = 500A and 1300A.

An increase of the gate current pulse length leads to an increase of the reverse recovery charges $Q_{rr}$ and $Q_{rr,Difference}$. Since an increase of $t_{pulse}$ almost linearly increases the additional impressed gate charge at the n-n+ border, it causes an increasing softening of the interruption of the reverse recovery current.

To analyze quantitatively the effect of change of the reverse recovery charge due to impressed gate current at different pulse lengths charge efficiency ($\eta$) is calculated. Table 3.6 shows the corresponding values for waveforms of $t_{pulse}$ of 5 $\mu$s and 10 $\mu$s at $V_{DC}$ = 2kV, $I_L$ = 1300A at a junction temperature of 25 °C. It can be seen from the results that the charge efficiency increases by 15% if the pulse length is increased from 5 $\mu$s to 10 $\mu$s.

| $t_{pulse}$ | $Q_{rr,Diff}$ | $Q_{Gate}$ | %charge efficiency ($\eta$) |
|---|---|---|---|
| 5$\mu$s | 0.287$\mu$As | 0.903$\mu$As | 31% |
| 10$\mu$s | 0.874$\mu$As | 1.887$\mu$As | 47% |

Table 3.6: Charge efficiency at different $t_{pulse}$ for IL226.10
($V_{DC}$ = 2kV, $I_{A,GCD}$ = 1300A, $I_{G,GCD}$ = 300A, $t_{delay}$ = -2$\mu$s, $T_j$ = 25°C)

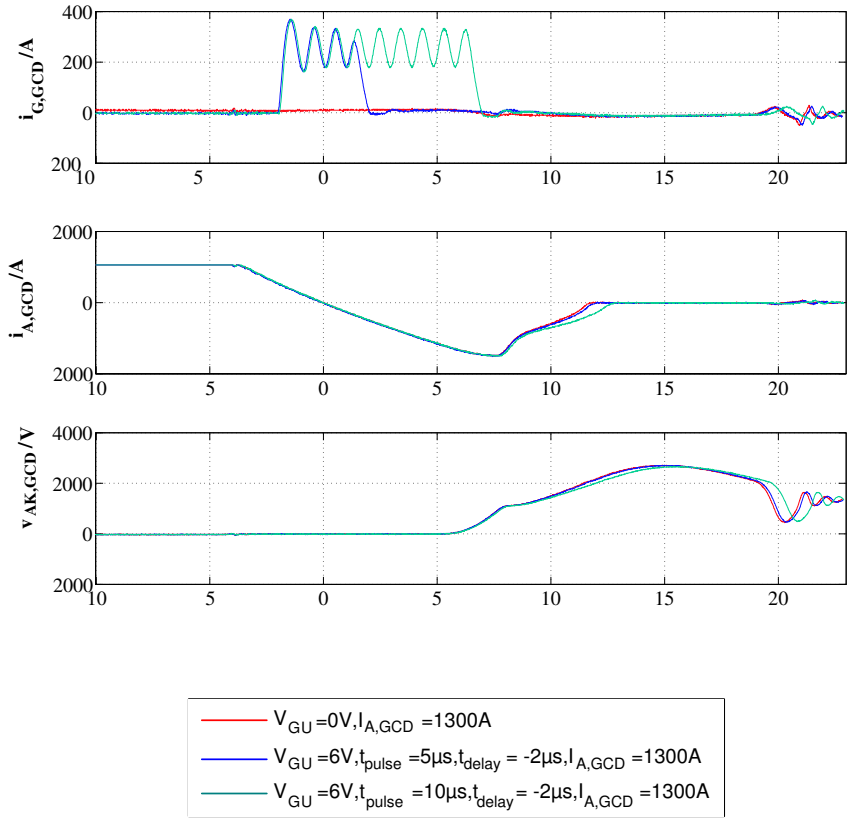
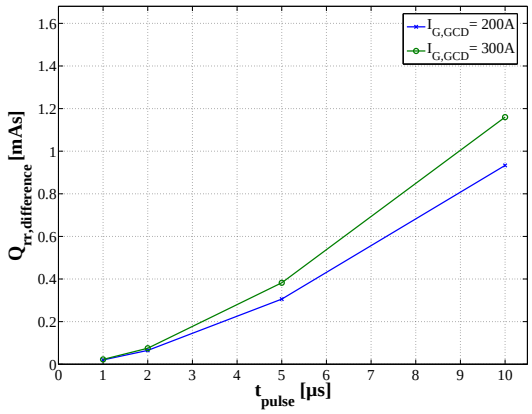



Figure 3.13: GCD Turn-off waveform (Device : IL226.10, $V_{DC}$ = 2kV, $I_L$ = 1300A, $T_j$ = 25°C, $I_{G,GCD}$ = 300A, $t_{delay}$ = -2 $\mu$ s, $t_{pulse}$ = 5 $\mu$ s, 10 $\mu$ s)

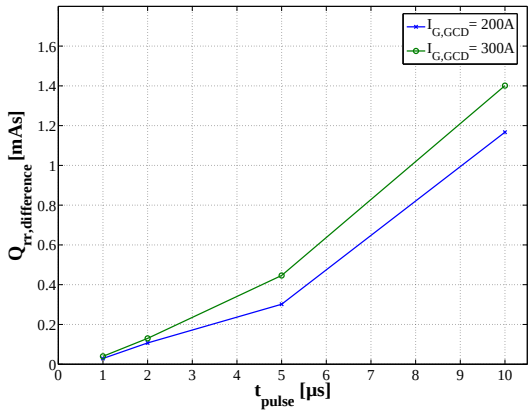
The reason for the lower charge efficiency at $t_{pulse}$ of 5 $\mu$s is the increase recombination of charge carriers before the smoothing of the reverse recovery current compared to the injected gate current with $t_{pulse}$ of 10 $\mu$s.

**Effect of $I_{G,GCD}$ on $Q_{rr,Difference}$**

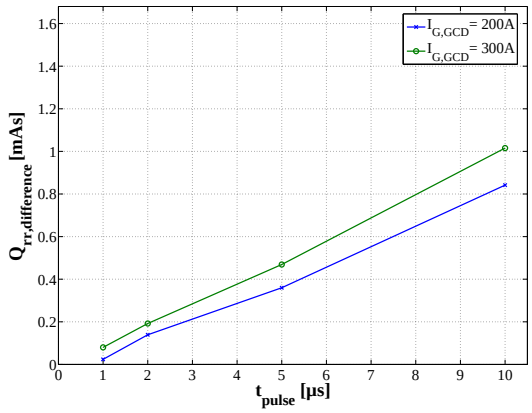
Another parameter of the gate current, which influences the softness of the recovery behavior is the amplitude of the gate current $I_{G,GCD}$. The GCD turn-off waveform shown in Figure 3.15 at $V_{DC}$ = 2kV, $I_L$ = 1300A, $T_j$ = 25°C, $t_{pulse}$ = 10 $\mu$s, $t_{delay}$ = 1.4 $\mu$s shows the effect of varying $I_{G,GCD}$ from 200A to 250A on the reverse recovery behavior. The increase in $I_{G,GCD}$ at fixed parameters $t_{delay}$ and $t_{pulse}$, increases the total injected charge via the gate into the device. A variation of the gate current amplitude changes the storage charge at n-n+ border and thus, the process of the interruption of the reverse recovery current. A higher gate current amplitude increases the charge density at the n-n+ region and leads therefore to an increased softening of the interruption of the reverse recovery current. Figure 3.16 shows the relation between the charge $Q_{rr,Difference}$ and the gate current amplitude $I_{G,GCD}$. Like expected the reverse recovery charge $Q_{rr}$ and $Q_{rr,Difference}$ as well as the softening of the reverse recovery process increases with increasing gate current amplitudes for all investigated delay times and pulse lengths.



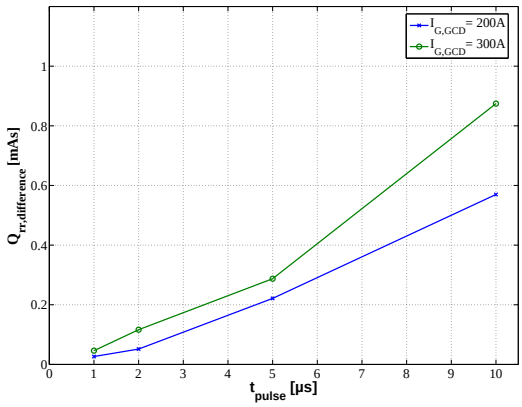

(a) $I_{A,GCD}$ = 500A, $t_{delay}$ = 0.8$\mu s$




(b) $I_{A,GCD}$ = 500A, $t_{delay}$ = 4$\mu s$




(c) $I_{A,GCD}$ = 1300A, $t_{delay}$ = 1.4$\mu s$




(d) $I_{A,GCD}$ = 1300A, $t_{delay}$ = -2$\mu s$

Figure 3.14: $Q_{rr,Difference}$= f($t_{pulse}$) of IL226.10 ($V_{DC}$ = 2 kV, $I_{A,GCD}$ = 500A / 1300A, $T_j$ = 25°C
)

Table 3.7 shows the change of the charge efficiency due to the change of the gate current for the sample measurement waveform. The charge efficiency increases by 5 % for a change of $I_{G,GCD}$ from 200 to 250A at fixed pulse delay, pulse length, applied voltage and load current. It can be also observed from the waveform shown in Fig. 3.15 that change of the softness factor is small. It increases from 0.5 to 0.52 for change of $I_{G,GCD}$ from 200 to 250A respectively.

The maximum injected gate current $I_{G,GCD}$ is limited to 300 A due to the specification of the gate unit and also due to the the GCD prototype design constraints.

### Effect of $T_j$ on $Q_{rr,Difference}$

In a conventional power diode, the amount of the reverse recovery charge $Q_{rr}$ depends on the junction temperature. Usually an increase of the junction temperature, increases the storage

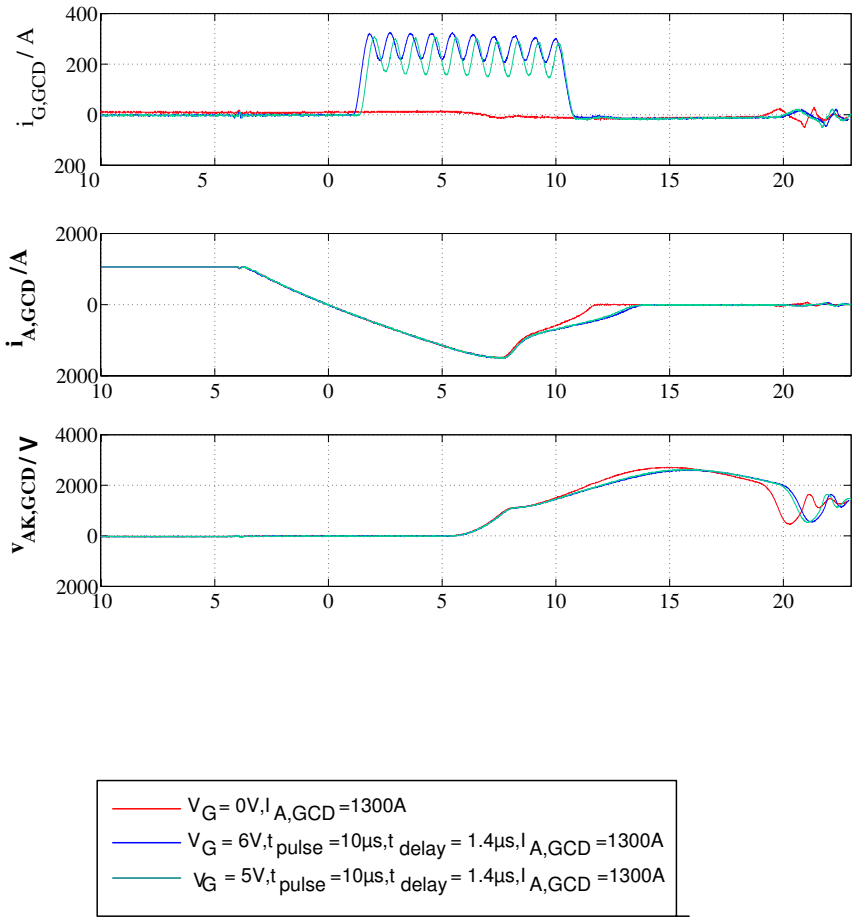



Figure 3.15: GCD Turn-off waveform (Device : IL226.10, $V_{DC}$ = 2kV, $I_L$ = 1300A, $T_j$ = 25°C, $t_{pulse}$ = 10$\mu$s, $t_{delay}$ = 1.4 $\mu$ s, $I_{G,GCD}$ = 200A, 300A)

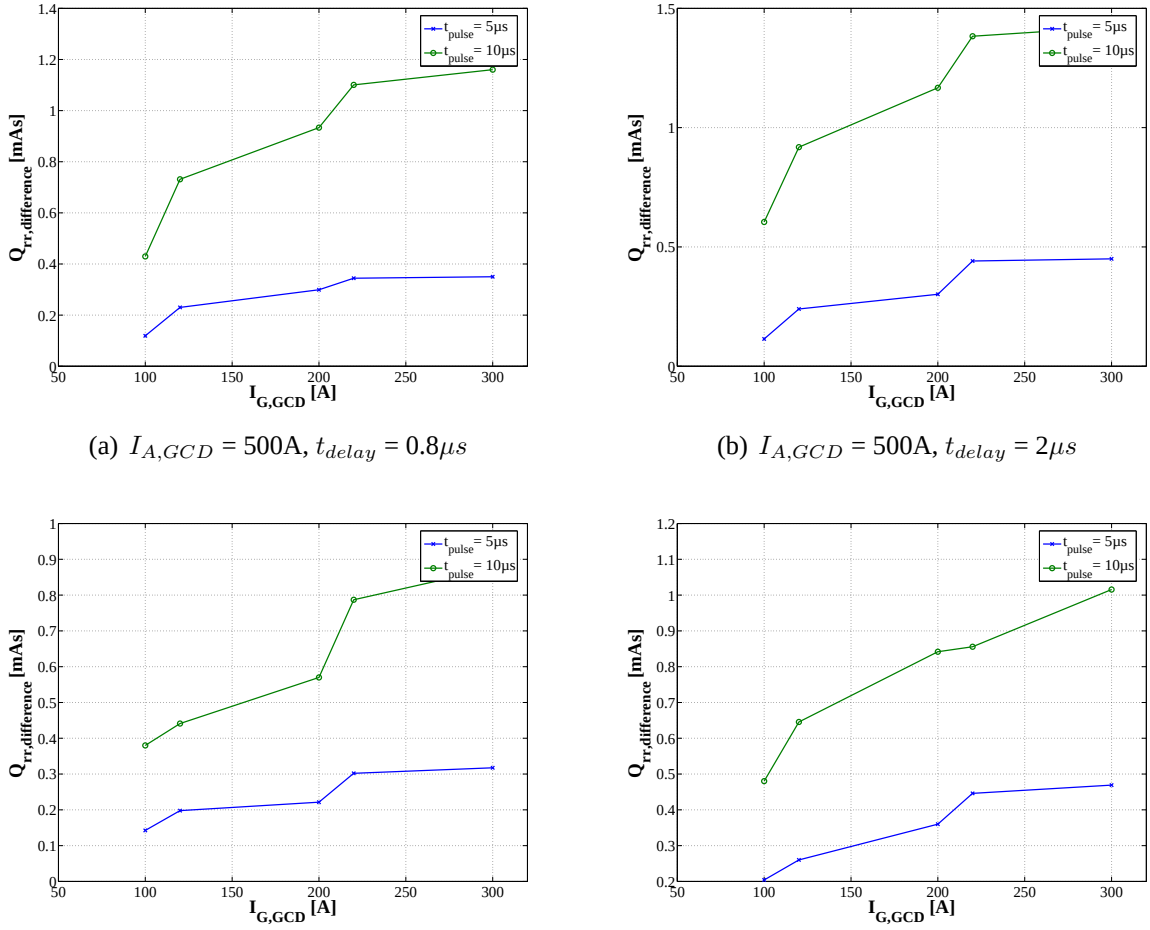
| $I_{G,GCD}$ | $Q_{rr,Diff}$ | $Q_{Gate}$ | %charge efficiency |
|---|---|---|---|
| 200A ($V_{GU}$ = 5V) | 0.221$\mu$As | 0.800$\mu$As | 27% |
| 250A ($V_{GU}$ = 6V) | 0.287$\mu$As | 0.903$\mu$As | 31% |

Table 3.7: Charge efficiency at different $I_{G,GCD}$ for IL226.10
($V_{DC}$ = 2kV, $I_{A,GCD}$ = 1300A, $t_{delay}$ = 1.4$\mu$s, $t_{pulse}$ = 10$\mu$s, $T_j$ = 25°C)

charge and also the reverse recovery time $t_{rr}$ to sweep out the increased reverse recovery charge by an increased reverse recovery current [41].

In the GCD, in addition to the change of the junction temperature, the reverse recovery charge $Q_{rr}$ gets affected due to the impressed gate current. Thus, it is necessary to analyze the effect of $T_j$ on the reverse recovery charge difference $Q_{rr,Diff}$ by considering additionally injected gate current parameters such as $t_{delay}$, $t_{pulse}$ and $I_{G,GCD}$ at different temperatures.

Figure 3.17 shows a turn-off waveform for different junction temperatures for a fixed delay, pulse length and gate current amplitude. As discussed before, there is an increase in $t_{rr}$ due to




(a) $I_{A,GCD}$ = 500A, $t_{delay}$ = 0.8$\mu s$

(b) $I_{A,GCD}$ = 500A, $t_{delay}$ = 2$\mu s$

(c) $I_{A,GCD}$ = 1300A, $t_{delay}$ = -2$\mu s$

(d) $I_{A,GCD}$ = 1300A, $t_{delay}$ = 1.4$\mu s$

Figure 3.16: $Q_{rr,Difference}$ = f($I_{G,GCD}$) (Device : IL226.10, $V_{DC}$ = 2 kV, $I_{A,GCD}$ = 500A / 1300A, $T_j$ = 25°C)

the increase of the junction temperature.

Table 3.8 shows the quantitative effect of the junction temperatures of $T_j$ on the charge efficiency and therefore also on $Q_{rr,Diff}$ experimentally for the turn-off conditions $V_{DC}$ = 2kV, $I_{A,GCD}$ = 1300A.

From the tabular results it is clear that the charge efficiency remains almost constant for different junction temperatures. Thus, the effect of the junction temperature on the increased reverse recovery charge $Q_{rr,Diff}$ is small for the investigated non-irradiated sample IL226.10.

**Effect of $t_{pulse}$ on $W_{off,GCD}$**

This section describes the switching losses of the GCD due to the impression of gate currents. Fig.3.18(a) and Fig.3.18(b) show the switching losses of the GCD as a function of the gate

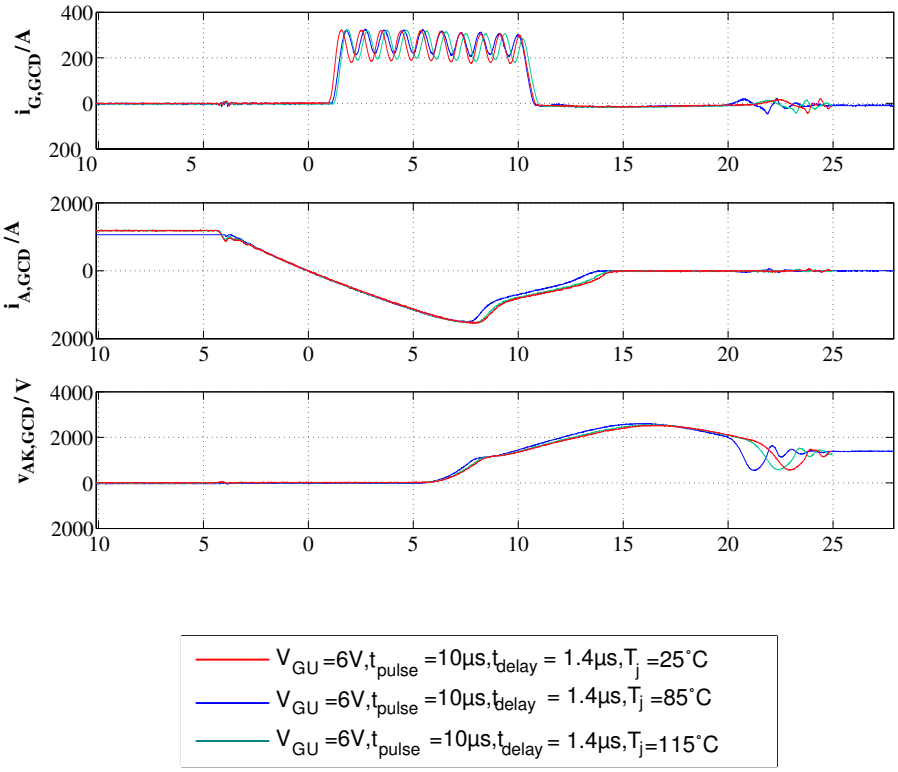


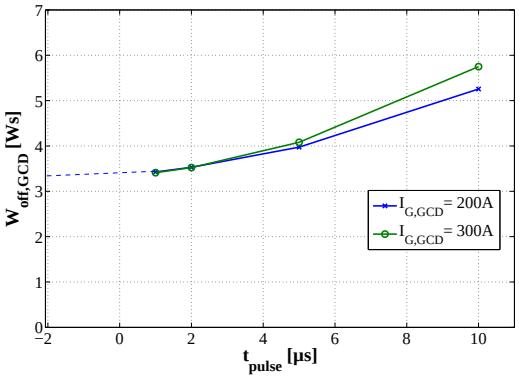

Figure 3.17: GCD Turn-off waveform at different junction temperatures (Device : IL226.10, $V_{DC}$ = 2kV, $I_L$ = 1300A, $I_{G,GCD}$ = 300A, $t_{pulse}$ = 10 $\mu$ s, $t_{delay}$ = 1.4 $\mu$ s, $T_j$ = 25°C/85°C/115°C)

| | $\eta$ @ $t_{pulse}$ = 5$\mu$s | | $\eta$ @ $t_{pulse}$ = 10$\mu$s | |
|---|---|---|---|---|
| | $t_{delay}$ = -2$\mu$s | $t_{delay}$ = 1.4$\mu$s | $t_{delay}$ = -2$\mu$s | $t_{delay}$ = 1.4$\mu$s |
| $T_j$ = 25°C | 31.8% | 51.9% | 46.3% | 57.9% |
| $T_j$ = 85°C | 31% | 51% | 46.05% | 57% |
| $T_j$ = 115°C | 30% | 50.5% | 45% | 56.8% |

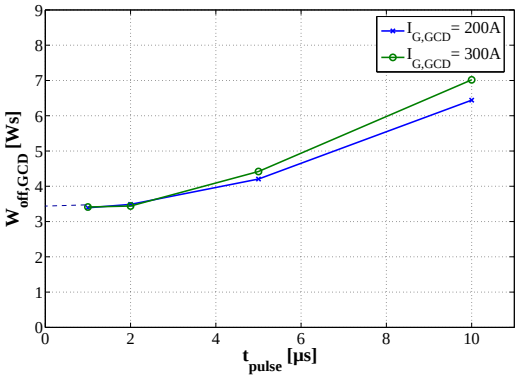
Table 3.8: Charge efficiency at different $T_j$ for the GCD IL226.10
($V_{DC}$ = 2kV, $I_{A,GCD}$ = 1300A, $I_{G,GCD}$ = 300A)

pulse length at $I_{A,GCD}$ = 500A for two different delays. In a similar manner Fig. 3.18(c) and Fig.3.18(d) show the switching loss of the GCD as a function of gate pulse length at $I_{A,GCD}$ = 1300A.

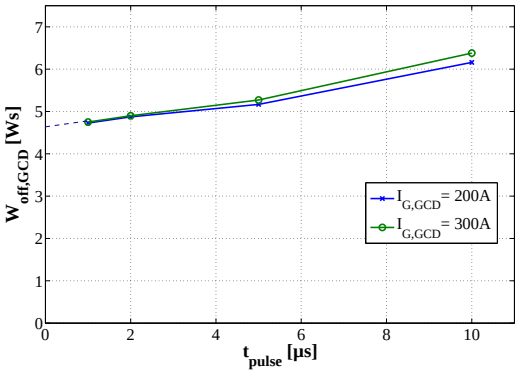
The GCD exhibits losses at $t_{pulse}$ = 0 $\mu s$, which are similar to the switching losses of a comparable conventional power diode. If the gate currents are impressed during the reverse recovery process, the switching losses increase like expected with increasing gate current amplitude and gate pulse durations. The switching losses range from 3.5 Ws to 7 Ws for $I_{A,GCD}$ = 500A and from 4.7 Ws to 6.4 Ws for $I_{A,GCD}$ = 1300A load current respectively. Compared to the switching losses when the gate is not active ($I_{G,GCD}$ = 0A), the switching losses are increased by 80% for $I_L$ = 500A, $t_{delay}$ = 0.8 $\mu$ s and 20% for $I_L$ = 1300A, $t_{delay}$ = -2 $\mu$ s at $I_{G,GCD}$ = 300A respectively.



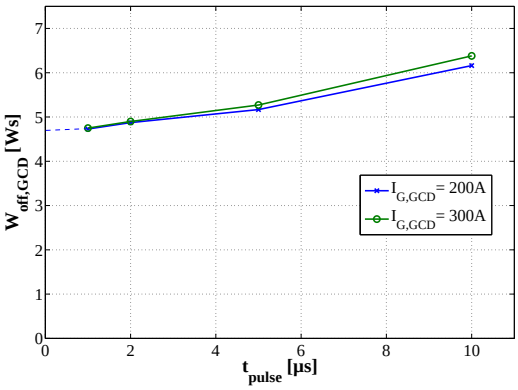

(a) $I_{A,GCD}$ = 500A, $t_{delay}$ = 0.8$\mu s$




(b) $I_{A,GCD}$ = 500A, $t_{delay}$ = 2$\mu s$




(c) $I_{A,GCD}$ = 1300A, $t_{delay}$ = -2$\mu s$




(d) $I_{A,GCD}$ = 1300A, $t_{delay}$ = 1.4$\mu s$

Figure 3.18: IL226.10 - $W_{off,GCD}$ = f($t_{pulse}$) ($V_{DC}$ = 2 kV, $I_{A,GCD}$ = 500A / 1300A, $T_j$ = 25°C)

## 3.5 Reduction of the IGCT turn-off current $I_{TQ}$ by the anti-parallel GCD

It has been already discussed that the leakage current of the GCD in the blocking mode can be influenced by the impression of a gate current. In addition to the snubberless series connection of the IGCTs, another application of the GCD could be as a free-wheeling diode in converter applications. As an example a 10 kV GCD could be realized easily using the existing diode design techniques. It has been explained in chapter 2 that during natural commutations with inductive load the current commutates between the IGCT and the diode. During forced commutation, the turn-off current of the IGCT can be reduced if the gate of the anti-parallel GCD of a switch position in a voltage source converter is turned-on during the IGCT is turning off. In that case, the total branch current, which has to be turned off is distributed between the turning off IGCT and the GCD. Therefore the IGCT turn-off current is reduced.

Figure 3.19 shows the test circuit for the reduction of the turn-off current $I_{TQ}$ of the IGCT by an impression of the gate current in the anti-parallel connected GCD.

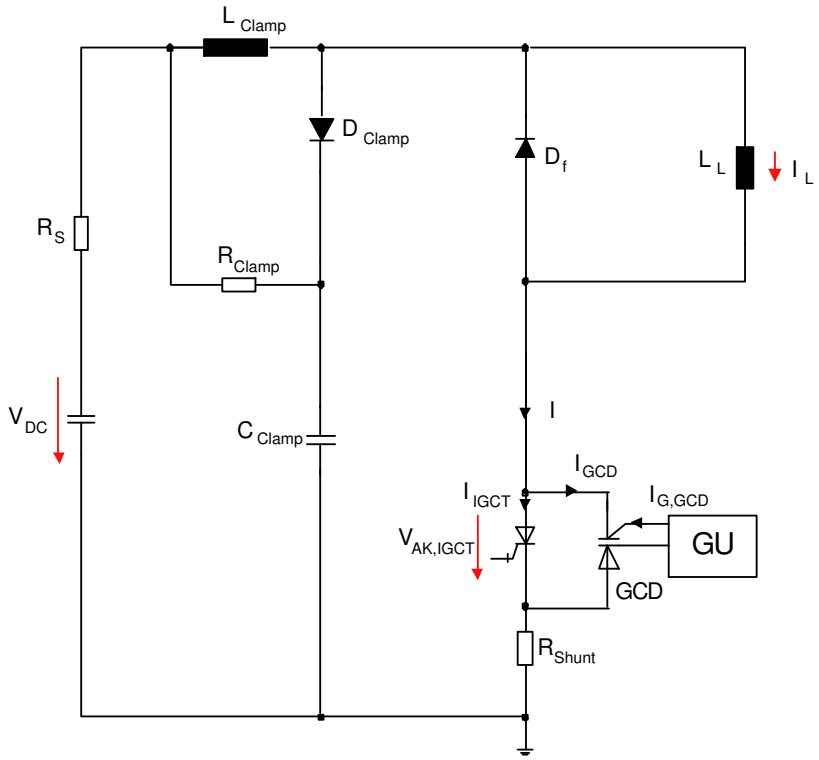



Figure 3.19: Test circuit for experimental investigation of the IGCT turn-off current reduction of IGCT by an anti-parallel GCD ($V_{DC}$ = 2kV, $I_L$ = 1kA, $L_{clamp}$ = 5.6 $\mu$ H , $R_{clamp}$ = 1.25 $\Omega$, $C_{clamp}$ = 2.5 $\mu$ F, $R_S$ = 0.2 $\Omega$, $L_L$ = 1 mH, IGCT - 4.5 kV/5SHY35L4503 , GCD - IL226.10)

A corresponding measurement is realized at $V_{DC}$ = 2kV and $I_L$ = 1kA to investigate the aforementioned principle. Figure 3.20 shows the waveforms of an IGCT turn-off transient without the impression of a GCD gate current. The GCD operates in the blocking mode when IGCT takes over voltage. The total 2kA load current flows through the IGCT. The measured GCD current, which charges the GCD capacitance is small.

Figure 3.21 shows the waveforms, where a positive gate current of $I_{G,GCD}$ = 200A is impressed in the GCD before and during the IGCT turn-off transient. It can be seen that the IGCT current $I_{IGCT}$ is reduced by almost 200A while the current through the GCD increases by almost 200A keeping the total current to be turned off constant. Figure 3.21 shows that the IGCT turn-off current is reduced by about the same GCD current $I_{G,GCD}$. The reason therefore that the GCD current $I_{GCD}$ is almost equivalent to the GCD gate current $I_{G,GCD}$ is that the leakage current gain of the GCD is about 1 (See chapter section 3.3).

Figure 3.22 depicts the instantaneous values of turn-off switching losses of the IGCT. Without the gate current impression of the GCD, the maximum instantaneous switching losses are 1.7 MW. These instantaneous peak losses are reduced to 1.2 MW by the impression of a GCD gate current of $I_{G,GCD}$ = 200A at $V_{DC}$ = 2kV, $I_L$ = 1kA. Depending on the leakage current gain of the GCD an effective reduction of the IGCT turn-off current and the maximum instantaneous IGCT trun-off power losses can be achieved. Therefore an increase of the turn-off capability of the series connection IGCT and GCD can be extended.

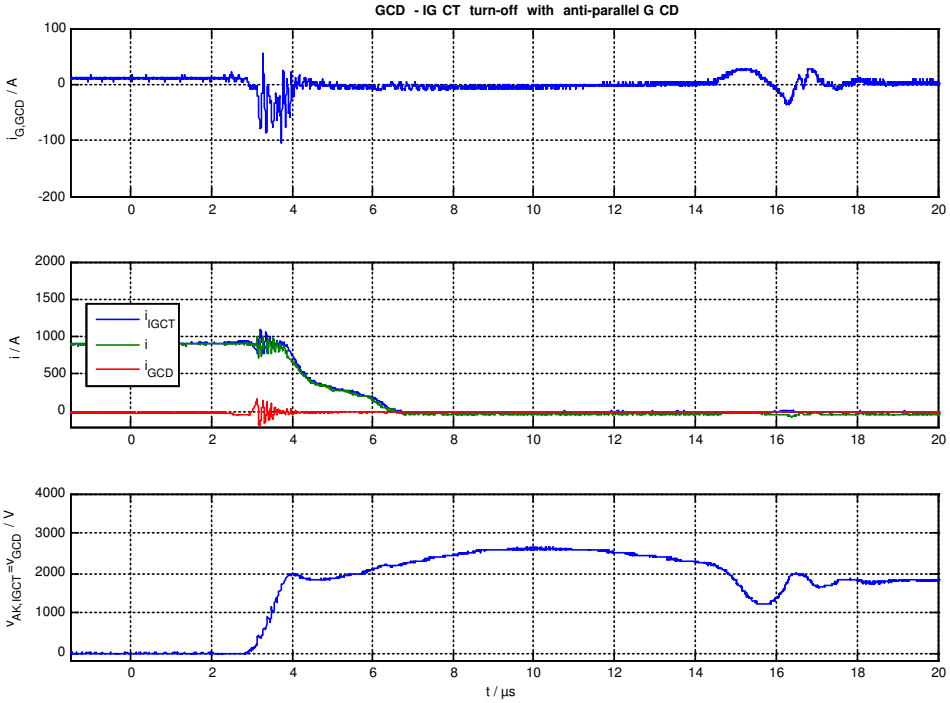



Figure 3.20: Turn-off waveforms of the IGCT and GCD ($V_{DC}$ = 2kV, $I_L$ = 1kA, $T_j$ = 25°C, $I_{G,GCD}$ = 0A)

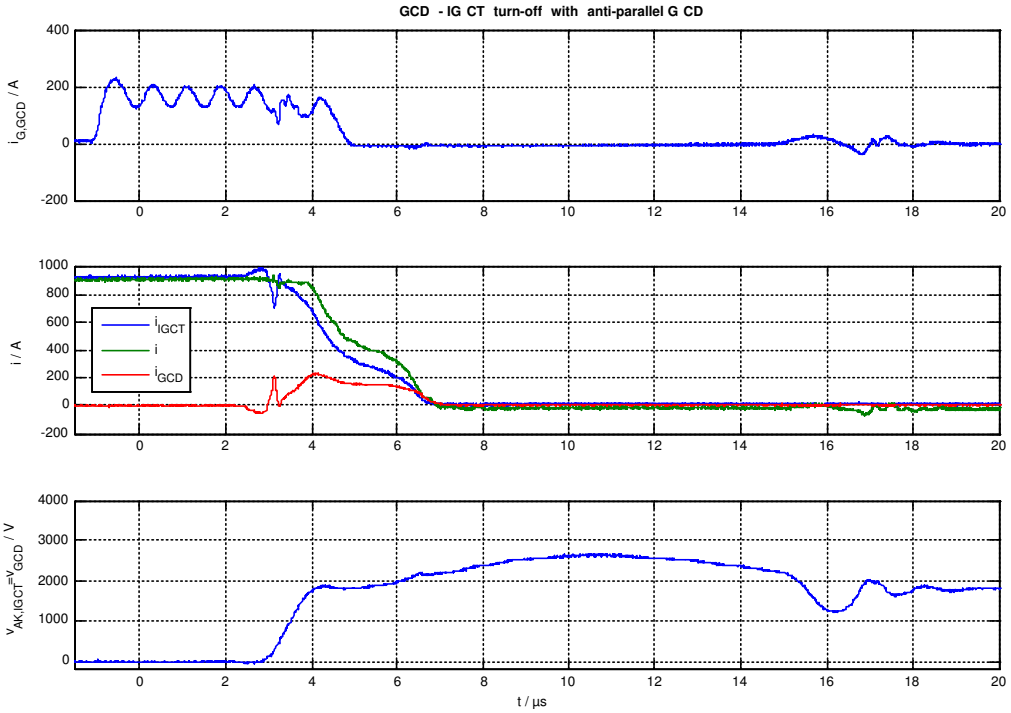



Figure 3.21: Turn-off waveforms of the IGCT and GCD ($V_{DC}$ = 2kV, $I_L$ = 1kA, $T_j$ = 25°C, $I_{G,GCD}$ = 200A)

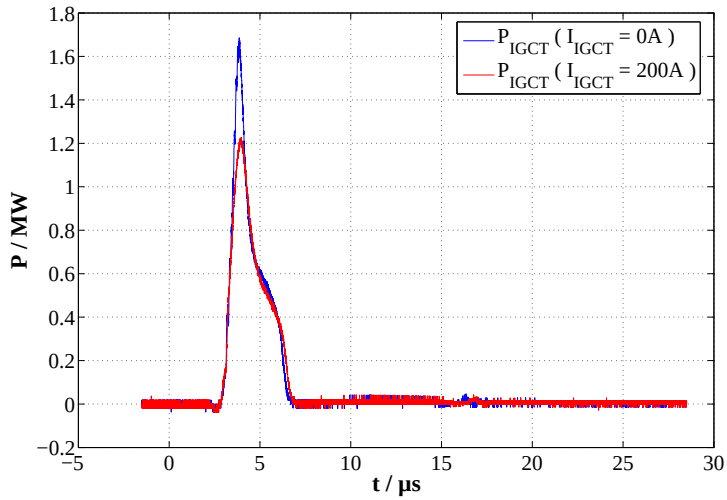



Figure 3.22: Instantaneous IGCT turn-off losses ($V_{DC}$ = 2kV, $I_L$ = 1kA, $T_j$ = 25°C, $I_{G,GCD}$ = 0A / 200A)

## 3.6 Summary

Chapter 3 has discussed the characterization of GCD samples during static and dynamic operation. The experimental investigations showed that both the static behavior as well as the reverse recovery behavior can be influenced by the impression of a gate current.

During the blocking state, the impression of a gate current leads to an increase of the leakage current. For GCD sample IL226.10, the impression of a gate current in a range of $I_{G,GCD}$ = 0 mA to 100 mA causes an increase of the leakage current from 0 mA to 67 mA at $T_j$ = 25°C and 7 mA to 82 mA at $T_j$ = 115°C. For the GCD sample IL226.13, the impression of a gate current in a range of $I_{G,GCD}$ = 0 mA to 100 mA causes an increase of the leakage current from 0 mA to 57 mA at $T_j$ = 25°C and 40 mA to 100 mA at $T_j$ = 115°C.

The investigation of the reverse recovery current showed that the impression of a gate current during the diode turn-off transient, makes the interruption of reverse recovery current softer. As an example for a GCD turn-off transient (GCD: IL226.10, $V_{DC}$ = 2kV, $I_L$ = 1300A, $T_j$ = 25°C) the softness factor can be increased from S = 0.4 ($I_{G,GCD}$ = 0 A) to S = 0.48 ($I_{G,GCD}$ = 300A, $t_{delay}$ = 1.4 $\mu$ s, $t_{pulse}$ = 5 $\mu$ s).

Assuming rectangular gate currents, the influence of the parameters gate current pulse duration ($t_{pulse}$), placement($t_{delay}$) and the gate current pulse amplitude on the reverse recovery process is investigated for the two GCD samples at different anode currents and junction temperatures. It is concluded that the gate current impression is most effective immediately before or during the interruption of the revers recovery current. If an autonomous GCD gate unit shall detect the impression of the gate current the rise of the diode voltage could be sensed.

The adjustment of the reverse recovery current and the softness factor by the gate current could be used in applications, where a soft recovery diode design is difficult to achieve without sub-

stantial negative consequences for other diode characteristics (e.g. on-state voltage, turn-off losses etc). 10 kV diodes are one example for such an application.

A second application, where the adjustment of leakage currents and the reverse recovery charge by the gate current are very advantageous, is the series connection of IGCTs with anti-parallel GCDs. This application is considered in chapter 4.

# Chapter 4

# State of the art series connection of IGCTs

This chapter shortly explains the basic operation of IGCTs. Furthermore the requirements and the application of series connected IGCTs are described. The conventional methods like RC-RCD snubber and regenerative snubber to achieve the series connection of IGCTs by maintaining the voltage symmetry between each of the series connected devices are explained. The basic principle of operation of these methods and their limitations are discussed.

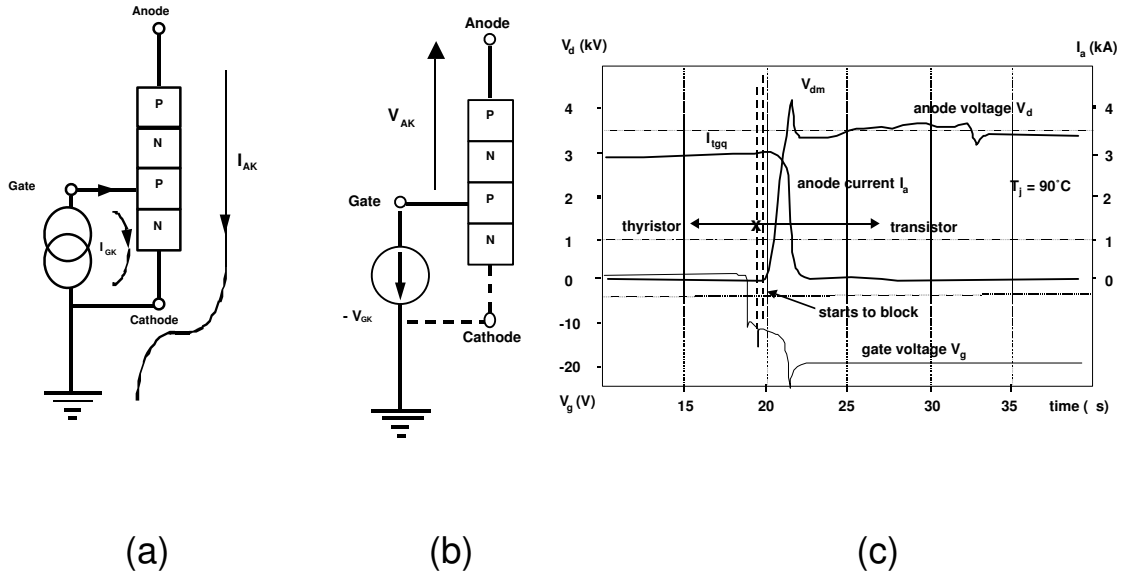
## 4.1 Structure, Function and characteristics of IGCT

The IGCT is a drastically improved GTO. The fundamental difference between a conventional GTO and an IGCT lies in the very low inductance gate drive system, which is inherent to the IGCT. The very low inductance in the gate current path has been achieved by the development of a new optimized housing and an integrated gate drive concept. In contrast to the GTO, where device and gate unit are connected via gate wires, the connection between gate unit and power semiconductor in the 'Gate commutated thyristor' (GCT) is realized by a plate construction. The resulting device is called 'Integrated Gate Commutated Thyristor'(IGCT). Fig. 4.1 shows the physical structure of an IGCT.

Figure 4.1: Physical arrangement of IGCT

Fig.4.2 (a) shows the equivalent circuit of an IGCT during the on-state operation. It is a device that has an on-state operation, which is equivalent to that of a GTO or thyristor [12],[13],[16].

The same is true for the blocking mode, where a negative gate-cathode voltage of $V_{GK}$ = -20V enables a high d$v$/d$t$ withstand capability (Fig.4.2(b)) [12,13,16].




(a) (b) (c)

Figure 4.2: Function of IGCT (a) On-state equivalent circuit (b) blocking mode equivalent circuit(c) Turn-off waveform of IGCT [13]

At turn-off transients the complete anode current is commutated to the gate before the anode-cathode voltage starts rising. Thus, there will be no longer any cathode current and cathode side transistor does not operate anymore when the IGCT takes blocking voltage. After the commutation of the anode current to the gate the IGCT turns off as pnp-transistor with open base. Since the pnp transistor is a high voltage, high current transistor with a thick n-base containing a large amount of space charge, it takes few microseconds to remove this storage charge by the anode current before the anode-cathode voltage can rise. Since the turn-off transient of the pnp transistor is homogeneous, the d$v$/d$t$ does not have to be limited.

Fig.4.2(C) shows an IGCT turn-off oscillogram and Fig.4.3 shows the stylized waveforms from which, it can be seen that a high rate-of-change of gate current(e.g d$i$/d$t$ $\geq$ 3kA/$\mu$ s) will allow the cathode current to fall to zero before the anode-cathode voltage rises [13].

The condition for "hard" or "unity gain" turn-off is that a dead-time $t_{desat}$ > 0 has to be achieved between the cathode current falling to zero and the appearance of anode voltage, as depicted in Fig.4.3. Fig. 4.4 shows the equivalent IGCT turn-off circuit, which commutates the anode current from the cathode to the gate during the interval $t_{comm}$ at turn-off.

A low gate-circuit stray inductance is necessary to achieve a "hard" or "unity gain" turn-off for the GCT ($t_{desat}$ > 0). The capacitor voltage is limited to about 20V by the gate-to-cathode avalanche voltage. The gate-circuit inductance is determined mainly by the GCT housing and the parasitic inductances of the turn-off circuit components [13].

The active turn-on transient of the IGCT at inductive loads is equivalent to that of GTOs. How-

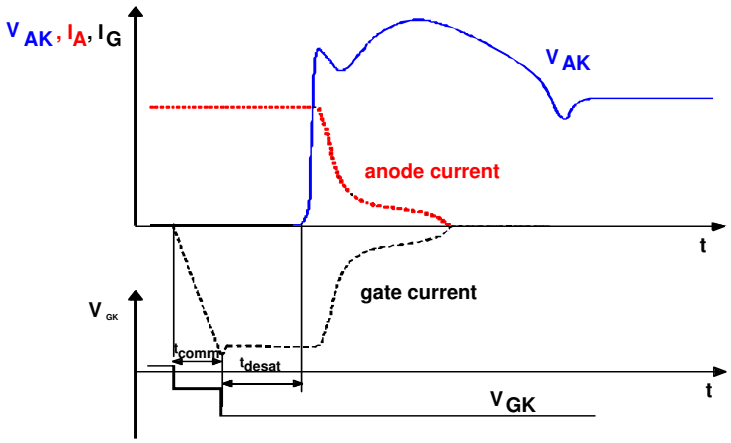



Figure 4.3: Stylized IGCT turn-off waveform showing the condition for "hard" turn-off transients $t_{desat} > 0$ [13]

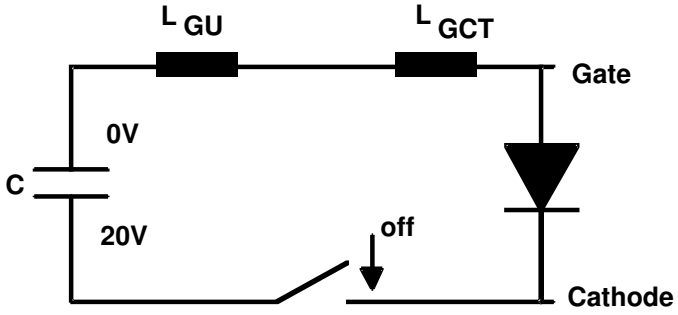



Figure 4.4: Equivalent gate-drive turn-off circuit with GCT gate-cathode junction represented as a diode. ($L_{GU}$ and $L_{GCT}$ represent the inductance of the gate circuit divided between the gate-unit and the GCT housing. [13])

ever, it is also improved by the low inductive gate drive. The fast impression of the positive gate current leads to a more homogeneous turn-on transient. In experiments no inhomogeneities have been observed at a rate of current rise of $\mathrm{d}i_A/\mathrm{d}t \geq 3000\mathrm{A}/\mu\,\mathrm{s}$. However, to keep the turning off diode within the safe operating area, the $\mathrm{d}i/\mathrm{d}t$ must be limited during the turn-on transient of the IGCT. Due to the latching during the turn-on transient the IGCT can not provide $\mathrm{d}i_A/\mathrm{d}t$ or $\mathrm{d}v/\mathrm{d}t$ control. Instead, a small turn-on snubber ( also called clamp) consisting of an inductor, a free-wheeling diode, a resistor and a clamp capacitor is required to limit the $\mathrm{d}i/\mathrm{d}t$ of the turning-off diodes.

The basic features of IGCTs can be summarized [12,13,16] :

- Requirement of clamp circuit due to
  - limitation of $\mathrm{d}i/\mathrm{d}t$ during IGCT turn-on transients to enable diode turn-off transients within the safe operating area (SOA) and homogeneous IGCT turn-on transients
  - limitation of short circuit peak currents
- Low on-state voltages

- Low turn-on losses
- Moderate turn-off losses
- Clamp losses
- Press pack case :
  - short circuit failure mode
    - Possibility of a redundant converter design (e.g. n+1)
    - explosion free
  - Higher reliability at thermal and power cycling than modules
  - More expensive mounting and cooling in a stack (for low power applications (e.g. $S_c \leq$ 3MVA) than modules

## 4.2 Basic considerations for the series connection of IGCTs

Today the maximum achievable converter output voltage of a three-level neutral point clamped voltage source inverter (3L NPC VSI) using 5.5 kV IGCTs is limited to 4.16kV. To achieve higher output voltages the series connection of semiconductors is necessary ( e.g. two 4.5kV IGCTs for a 6kV drive)[6]. Figure 4.5 shows a 3L NPC VSI with an IGCT series connection.

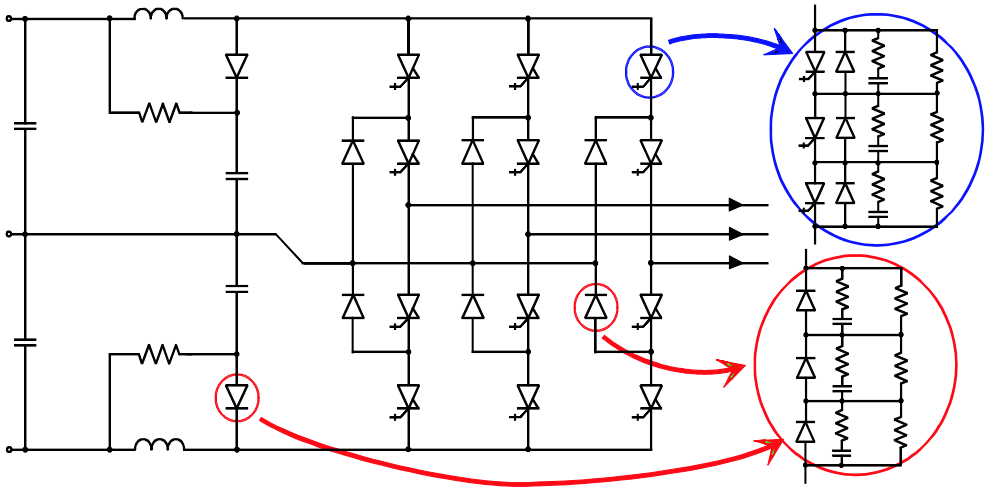


Figure 4.5: Schematic of an 24MVA 3L NPC VSI with 9kV output voltage [6]

For the effective series connection of semiconductor devices the voltage balancing has to be maintained for the

- blocking mode as well as
- the turn-on and turn-off switching transients.

The voltage symmetry during the blocking mode can be achieved by using a simple balancing resistor in parallel to the device. The critical points of operation are the switching transients. In this case the voltage sharing of the series connection is compromised due to

- time deviations of the switching signals (e.g. variation of the process times of the gate units) and
- the different switching characteristics of the power semiconductor itself.

Two different types of Snubber networks - RC and RCD snubber - are used in the IGCT series connection for voltage balancing. Figure 4.6(a) shows the RCD network and Figure 4.6(b) shows the RC-snubber voltage balancing network. RCD-snubbers have the following drawbacks [6]:

- Fast, expensive diodes have to be used, because a turn-on transient of the IGCT while current is still flowing into the snubber diode will cause a substantial di/dt and dv/dt stress of the rapidly turning off diode, requiring an extended safe operating area (SOA).
- The necessary adherence of a minimum turn-on time to discharge the snubber capacitor limits the dynamics of the converter.

However, if large snubber capacitors are required, the RCD snubber is the most effective solution. If selected IGCTs are used, small snubber capacitors are required. In that case a simple RC-snubber is an effective solution (Fig. 4.6(b)[4]).

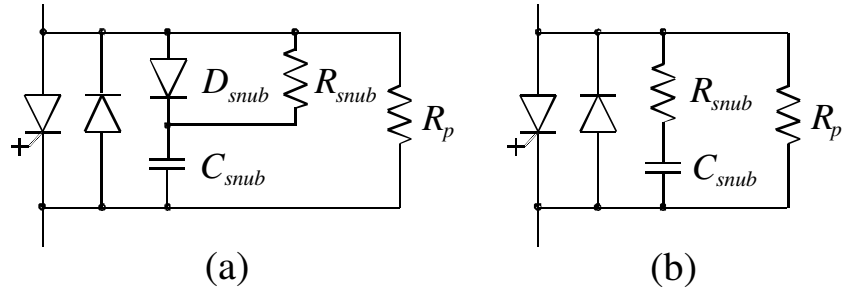



Figure 4.6: Series connection of IGCTs with RCD-snubber (a) and RC-snubber (b) [6,4]

Figure 4.7 shows the photo of a RC snubber, which is used in experiments to analyze its effect on the series connection of IGCTs.

### 4.2.1 Series connection of the IGCTs with the RC snubber

In Fig. 4.8 a simple circuit with series connected IGCTs is depicted for understanding the basic function of the RC Snubber network. The circuit is a buck converter consisting of two series connected IGCTs, one free wheeling diode ($D_f$), one clamp circuit and the voltage balancing RC snubber in parallel to the IGCTs. The parallel resistors $R_{P1}$ and $R_{P2}$ are the the static voltage balancing resistors.

To simplify the analysis of the RC-snubber , it was assumed that there is only one freewheeling and clamp diode in the circuit. It should be noted that, in a converter using a series connection of devices both diode positions (free wheeling diode and clamp diode) must be realized by a

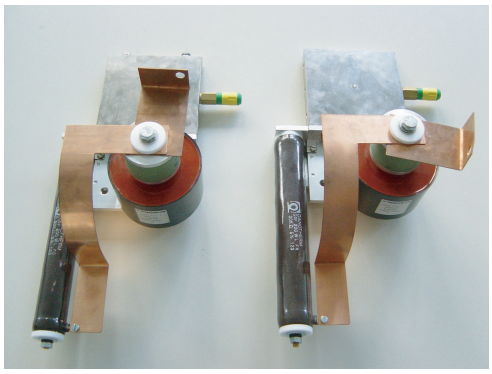


Figure 4.7: Physical arrangement of RC Snubber ($R_S$ = 1 Ω, $C_S$ = 500 nF)

series connection of two devices. In that case also the series connected diodes require voltage balancing RC networks.

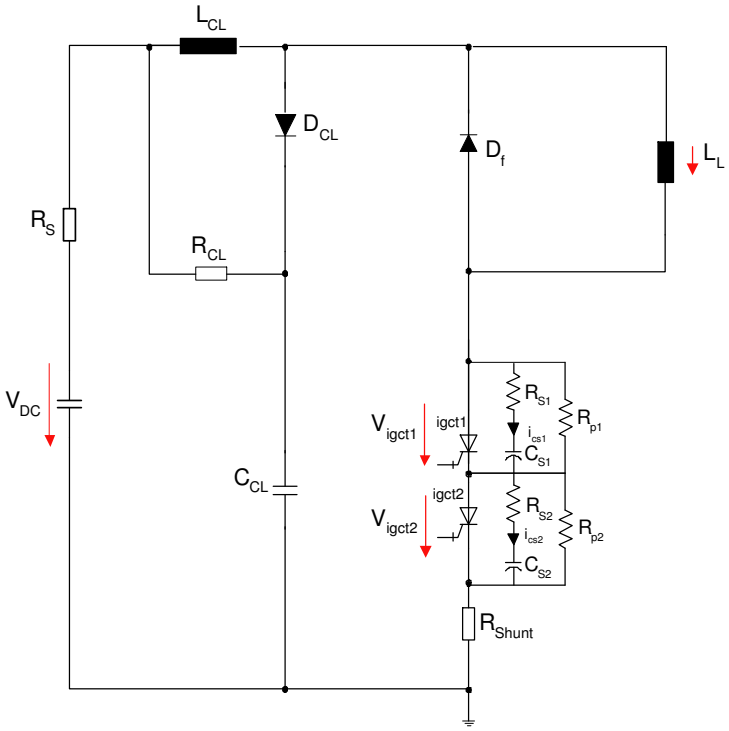



Figure 4.8: Test circuit of IGCT series connection with RC snubber

To analyze the behavior of the RC snubber, it is assumed that the load current is constant during commutations. Initially, IGCT1 and IGCT2 are turned on and $C_{S1}$ and $C_{S2}$ are completely discharged. The load current flows through IGCT1 and IGCT2.

### A. Turn-off transients of IGCTs (IGCT1 and IGCT2)

The currents in both IGCTs drop at splitting speed (e.g. due to the different device characteristics) after some delay when the gate signals are given. At the same time the currents in the

RC snubber increase at the same speed since the load current is assumed to be constant and the freewheeling diode turns on only when the sum of the voltages $V_{IGCT1}$ and $V_{IGCT2}$ reaches the DC voltage. When IGCT1 and IGCT2 are completely switched off, both $C_{S1}$ and $C_{S2}$ are charged with the constant load current. In this process, the voltages across IGCT1 and IGCT2 can be described as

$$V_{igct1} = i_{CS1} \cdot R_{S1} + \frac{1}{C_{S1}} \cdot \int_0^t i_{CS1}\, dt \tag{4.1}$$

$$V_{igct2} = i_{CS2} \cdot R_{S2} + \frac{1}{C_{S2}} \cdot \int_0^t i_{CS2}\, dt \tag{4.2}$$

where, $V_{igct1,2}$ are the voltages across IGCT1 ad IGCT2 and $i_{CS1,2}$ are the currents which flow through $C_{S1}$ and $C_{S2}$. After the occurrence of an over voltage across the capacitors due to the clamp circuit, the turn-off transient is completed when the sum of the IGCT and the capacitor voltages reach the dc link voltage.

**B. Turn-on transients of IGCTs (IGCT1 and IGCT2)**

The voltages of the IGCTs drop rapidly to the dynamic on-state voltage when the drive signals are given. Once the voltage across IGCT1 and IGCT2 are lower than those across $C_{S1}$ and $C_{S2}$, the snubber capacitors will be discharged through the loop $C_{S1}$ - $R_{S1}$ - IGCT1 and $C_{S2}$- $R_{S2}$ - IGCT2. After a certain time interval ($\approx 5.\ R_S, C_S$), the capacitors $C_{S1}$ and $C_{S2}$ are almost completely discharged. Obviously, the complete stored energy of the snubber capacitors is converted into heat in the snubber resistor and the turning-on IGCTs.

**Selection of $R_S$ and $C_S$**

To determine the design of the RC-snubber the following basic considerations are important:

- The capacitor value can be chosen quite small, due to well defined fast switching transients of IGCTs. However, to improve the voltage sharing during turning-off transients of non identical devices and to reduce the IGCT turn-off losses a large snubber capacitor as well as small snubber resistor are chosen. In contrast, large values of snubber capacitance cause a substantial turn-on losses in the IGCT as well as additional losses in the snubber network.

- Another important parameter the stray inductance of the RC snubber network affects the voltage sharing, turn-on and turn-off losses. The stray inductance of the RC snubber should be as small as possible in principle

It is necessary to select snubber values with the best trade-off of snubber capacitor, snubber resistor and leakage inductance. To find a suitable value combination of $R_{snub}$, $C_{snub}$, $L_{\sigma,snub}$ the following parameters, which influence the voltage balancing within a series connection have been taken into account :

- DC-link voltage

- Output phase current
- switching behavior of the IGCTs
- delay time between gate signals
- device junction temperatures
- snubber component tolerances

Table 4.1 shows the influence of the selection of the snubber parameters qualitatively.

| | voltage deviation $\Delta$ V | IGCT turn-on losses $E_{on,IGCT}$ | IGCT turn-off losses $E_{off,IGCT}$ | Snubber losses $E_{snub}$ |
|---|---|---|---|---|
| $C_{Snub} \uparrow$ | $\downarrow$ | $\uparrow$ | $\downarrow$ | $\uparrow$ |
| $R_{Snub} \uparrow$ | $\uparrow$ | $\downarrow$ | $\uparrow$ | - |
| $L_{\sigma,Snub} \uparrow$ | $\uparrow$ | $\downarrow$ | $\uparrow$ | - |

Table 4.1: Design trade-offs for RC Snubber [6]

Reference[6] shows that a RC-snubber of the values of $R_S$ = 1 $\Omega$, $C_S$ = 500 nF are suitable for the series connection of selected 91mm 4.5kV IGCTs and 68mm diodes.

**Selection of $R_p$ for static symmetry**

The value of the parallel resistor $R_p$ should be selected such that the voltage deviation in the steady state condition should not cause a violation of the border of the static DC blocking capacity of the device.

From Figure 4.9, a simple approximation for the calculation of $R_p$ can be described [14]. Assuming the worst steady state unbalance in 'n' series connected IGCTs, if $V_{DC}$ is the applied DC voltage and $V_m$ is the maximum allowed blocking voltage of each switch , it will be considered that only one IGCT is blocking the maximum voltage $V_m$. All other (n-1) switches are blocking a voltage of $V_m$ - $\Delta$ V. Thus,

$$V_{DC} = V_m + (n-1)(V_m - \Delta V) \tag{4.3}$$

where, $\Delta$ V is the maximum voltage deviation.

By defining 'm' as the percentage of the maximum voltage unbalance ( i.e. m = 10 means that the maximum voltage unbalance is 10 %), $\Delta$ V can be defined as

$$\Delta V = (\frac{m}{100}) \cdot V_m \tag{4.4}$$

The resistance $R_p$ is calculated assuming the worst case of the leakage current distribution. Leakage current and resistance have an inverse ratio. When the leakage current flowing through the device under blocking condition is the lowest, its blocking resistance is the highest among the blocking resistances of the other switches and thus it shares the highest voltage drop with

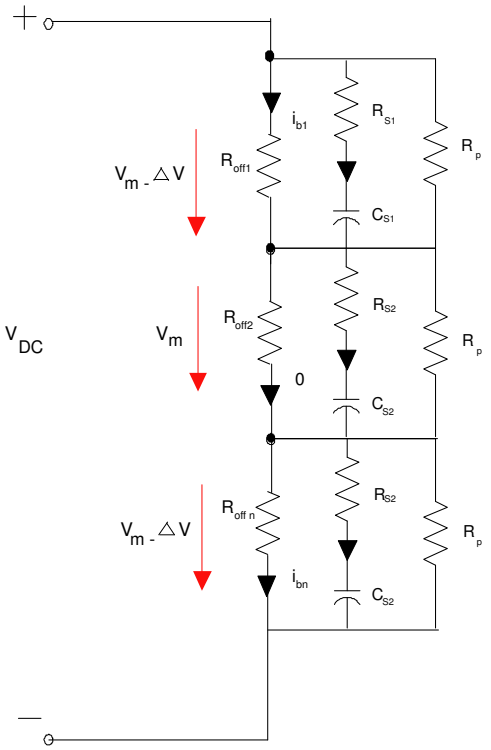



Figure 4.9: IGCT blocking voltage and leakage current distribution for steady-state operation

respect to the series connected switches. The situation is shown in Fig. 4.9. The leakage current of the middle resistor is assumed to be zero ( $R_{off2} = \infty$ ). Thus the middle resistor blocks the maximum voltage $V_m$. For the remaining resistors (top and bottom resistors), it is assumed that, their leakage current is equal to the maximum leakage current $I_b$ ( $I_{b1} = I_{b3} = I_b$)[14]. Therefore, it follows the equation :

$$\frac{V_m}{R_P} = I_b + \frac{V_m - \Delta V}{R_P} \tag{4.5}$$

Combining the equations (4.4) and (4.5) it gives,

$$R_P = \frac{(mV_m)}{(100I_b)} \tag{4.6}$$

as approximate value of the parallel resistor $R_P$.

### Evaluation of RC Snubber networks

The references [6],[7] show, that a RC snubber is a simple, straight forward solution for a series connection of IGCTs and diodes. However, the RC snubber has the following disadvantages :

- Voltage derating of IGCTs/diodes by the remaining voltage unbalance of selected devices ( e.g. by 15%)

- increase of the converter losses by the snubber losses
- selection and classification of devices like $t_{off}$, leakage current etc.
- increased size and complexity of mechanical structure
- increased costs ( material and manufacturing)
- reduced reliability due to increase of part count

### 4.2.2 Series connection of the IGCTs with Regenerative snubber

The references [3],[4] propose regenerative snubbers for the series connection of IGCTs. In this networks a supply of IGCT gate units on potential and a feedback of the remaining part of the stored energy into DC voltage link ( Figure 4.10) is possible.

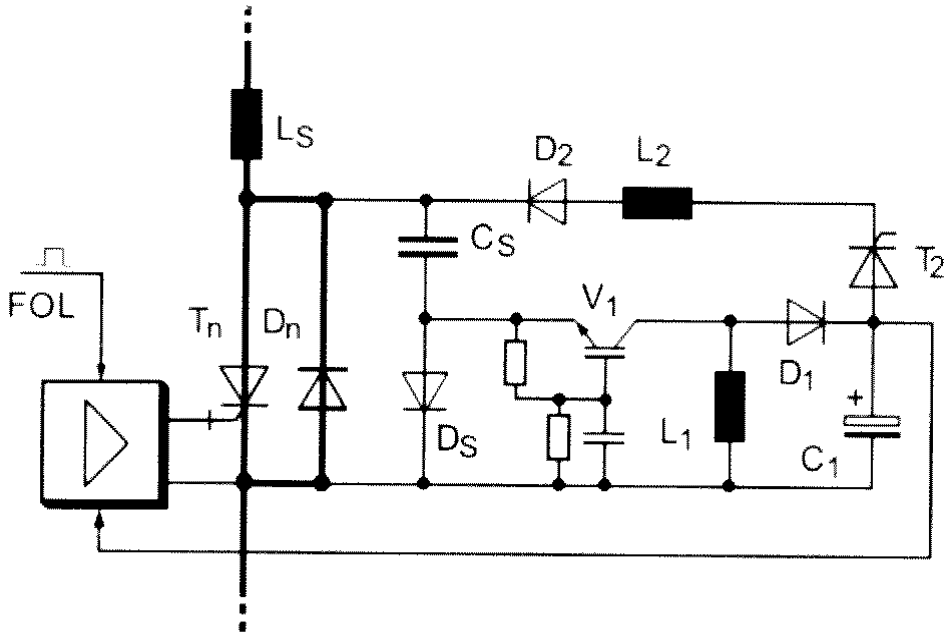



Figure 4.10: Circuit diagram of one switching cell of regenerative snubber [4]

However the substantial part count and complexity of the snubber are the main reasons, that this regenerative snubber network has not been applied in products or systems on the market so far.

## 4.3 Summary

The chapter 4 has shown, that the state of the art series connection of IGCTs and diodes requires external voltage balancing network. Various voltage balancing networks like RC-snubber, RCD-snubber and regenerative snubbers are shortly described. However, additional costs, losses, size, complexity and a reduced reliability limit the effectiveness of these solutions. Therefore, chapter 5 describes a new approach, which enables a series connection of IGCTs by the use of Gate Controlled Diodes.

# Chapter 5

# Experimental investigation of the IGCT series connection with GCD

This chapter focuses on the experimental test setups and test results of both - an IGCT series connection with RC snubber network and IGCT series connection with anti-parallel connected GCDs, to obtain a voltage symmetry across the series connected IGCTs. The main goal of these investigations is the experimental verification that a useful voltage symmetry of the series connected IGCTs with anti-parallel GCDs can be achieved by the impression of suitable gate currents in the blocking state and during the IGCT turn-off transients. Section 5.1 describes the test setup and the test conditions for obtaining the static symmetry between series connected IGCTs with an anti-parallel GCD. These are followed by the measurement results of static symmetry. Section 5.2 deals with experimental setups and results of an IGCT series connection with GCDs for maintaining the voltage symmetry during their turn-off transients. Strongly different junction temperatures and substantial time delays of the gate signals of the series connected IGCTs are used in the experimental investigations to model a very different switching behavior of IGCTs. The chapter concludes with test results of achieving a voltage symmetry between series connected IGCTs with conventional RC snubber networks. These results are compared with the test results of series connected IGCTs with anti-parallel GCD.

## 5.1 Static Voltage Balancing

The static voltage sharing of series connected devices in the blocking mode is important to achieve a high reliability regarding cosmic rays. Therefore, the static device voltage must fulfill the requirement : $V_{AK} \leq V_{DC,LINK}$ (100FIT).

Without an additional circuitry, the blocking voltage of series connected IGCTs (with or without anti-parallel diodes) could be very different due to deviating device leakage currents. The leakage currents of power semiconductors like e.g. IGCTs or diodes, are caused not only by the behavior of pn-junctions, but also by side effects like passivation. Thus, slight parameter changes during the manufacturing of power semiconductors (e.g. radiation, passivation) will cause different device leakage currents at constant conditions (e.g.$V_{AK}$, $T_j$, gate-cathode circuitry). Furthermore, the leakage currents are strongly dependent on the junction temperature of the device. This correlation is device specific and dependent on the level and type of irra-

diation. Thus, also junction temperature differences of series connected devices will cause an unequal voltage distribution of series connected devices.

### 5.1.1 Experimental Set-up

Figure 5.1 shows the test setup with two series connected IGCTs in their blocking mode. A GCD is connected anti-parallel to one of the IGCTs. A DC Voltage ($V_{DC}$) of 1kV to 2KV is applied across the series connection of IGCTs. The voltage across each of the IGCTs, $V_{IGCT1}$ and $V_{IGCT2}$ is measured with high voltage differential probes. A gate current impression via the gate ($I_{G,GCD}$) of the GCD is done by a simple current source generator.

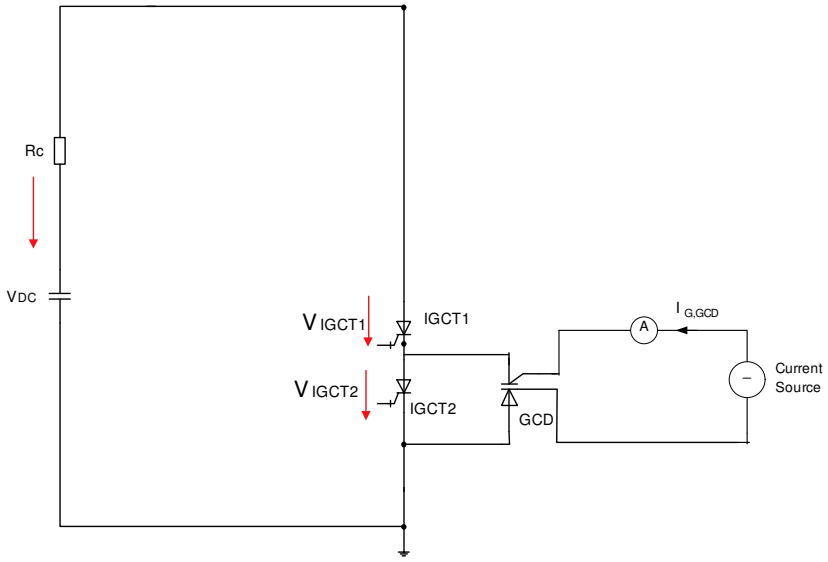



Figure 5.1: Test circuit for static voltage symmetry investigation of series connected IGCTs ($V_{DC}$= 1kV, 2kV, $R_C$ = 0.2 Ω, IGCT1, IGCT2: 4.5kV/4000A ABB device (5SHY 35L4503), GCD : IL226.13)

Figure 5.2 shows the physical arrangement of the test setup to investigate the static voltage distribution of series connected IGCTs.

To investigate the behavior of series connected IGCTs and diodes with different leakage currents very different junction temperatures $T_{j,IGCT1}$ = 85°C and $T_{j,IGCT2}$ = $T_{j,GCD}$ = 25°C were realized. While IGCT1 was heated by an isolated cylindrical heater placed around the device, a heat isolating sheet between IGCT1 and IGCT2 / GCD maintains the junction temperature difference. A DC voltage of $V_{DC}$ = 1kV, 2 KV is applied across the series connection.

### 5.1.2 Experimental Results

Figure 5.3 depicts the test results for the investigation of the static symmetry of a series connected IGCTs according to Figure 5.1.

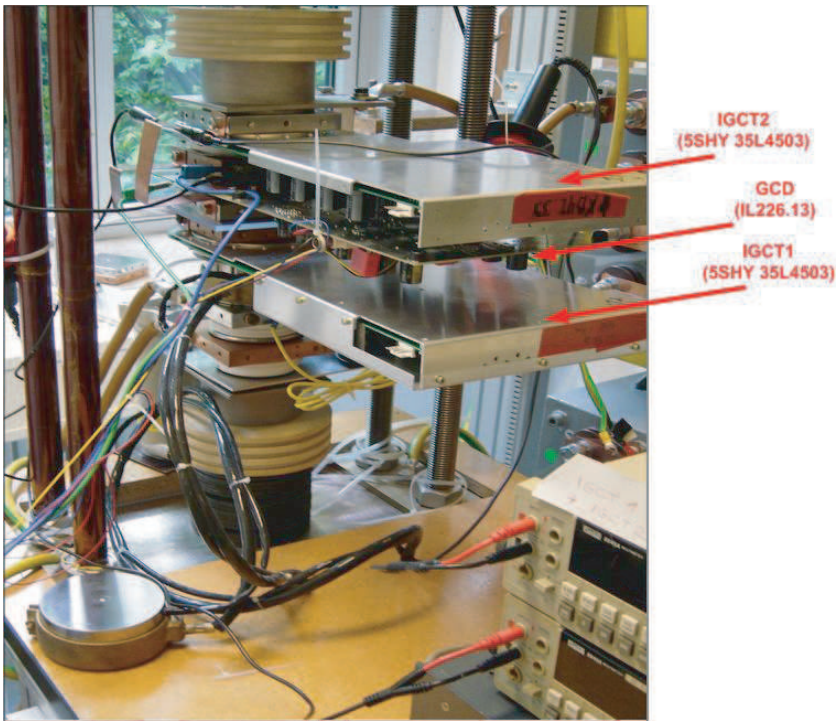



Figure 5.2: Physical arrangement of the stack of an IGCTs series connection according to the circuit of Figure 5.1

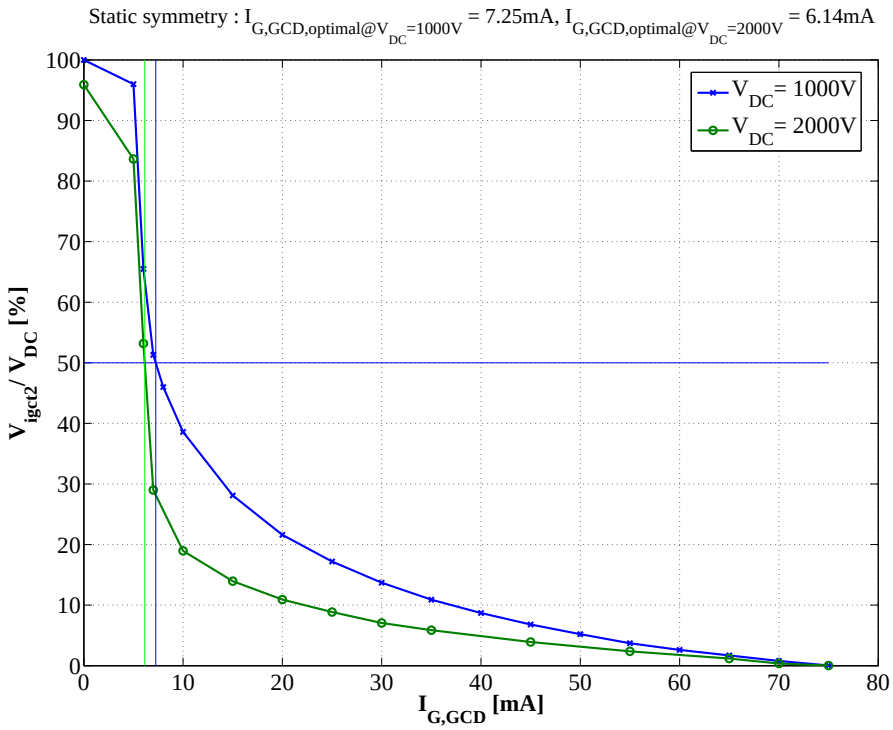



Figure 5.3: Voltage distribution ratio of the IGCT2 Vs Gate current $I_{G,GCD}$ of the GCD ($T_{j,IGCT1}$ = 85°C, $T_{j,IGCT2}$ = $T_{j,GCD}$ = 25°C)

For analyzing the test results, a ratio between $V_{IGCT2}$ and $V_{DC}$ is calculated for various impressed gate currents. The substantially higher junction temperature of IGCT1 compared to IGCT2 ($T_{j,IGCT1}$ = 85°C, $T_{j,IGCT2}$ = $T_{j,GCD}$ = 25°C) causes a substantially lower blocking resistance (high leakage current) of IGCT1 compared to that of IGCT2 and its anti-parallel GCD. Thus, IGCT2 will take over a higher share of the DC voltage if no gate current is impressed in the GCD. Since the impressed gate current $I_{G,GCD}$ enables an adjustment of the GCD leakage current and of the blocking resistance of this switch position, the voltage distribution of $V_{IGCT1}$ and $V_{IGCT2}$ varies with the changing gate current of the GCD.

It is worth to be noted that, to achieve the static voltage symmetry by an impression of a GCD gate current, only the difference in the leakage currents of the two series connected switch positions needs to be compensated by the gate current controlled leakage current of the GCD. Figure 5.3 shows that the substantially colder IGCT2 takes over almost the entire dc-link voltage if no gate current is impressed in the GCD. Like expected, an increase of the impressed gate current $I_{G,GCD}$ increases the leakage current of the GCD and therefore decreases the voltage of the IGCT2 $V_{IGCT2}$. A voltage symmetry of IGCT1 and IGCT2 is achieved at a gate current of about $I_{G,GCD}$ = 6mA and $I_{G,GCD}$ = 8mA at dc-link voltages of $V_{DC}$ = 2kV, 1kV respectively. A further increase of the impressed gate current further decreases the blocking resistance of the GCD till the condition :

$$R_{block,IGCT2}.R_{block,GCD}/R_{block,IGCT2} + R_{block,GCD} < R_{block,IGCT1} \tag{5.1}$$

where, $R_{block,IGCT1}$, $R_{block,IGCT2}$ are the blocking resistances of IGCT1 and IGCT2 respectively and $R_{block,GCD}$ is the blocking resistance of the GCD.

is fulfilled. Therefore, the voltage share of the IGCT2 falls below 50 % and reaches to a value of less voltage than 10 % $V_{DC}$ for about $I_{G,GCD}$ > 22 mA ($V_{DC}$ = 2kV) and $I_{G,GCD}$ > 37 mA ($V_{DC}$ = 1kV).

## 5.2 Dynamic Voltage Balancing

### 5.2.1 Experimental Set-up

It was explained in chapter 4 that basically different device switching characteristics (e.g. storage charge) and non identical gate unit delay times are the main reasons for an unequal voltage distribution of series connected IGCTs during turn-off transients. It can be taken from the reference [6], that the turn-on transients of the series connected IGCTs usually do not cause substantial voltage unbalances. To investigate an IGCT series connection with GCDs deviating device characteristics are achieved by the operation of series connected IGCTs at very different junction temperatures ($T_{j,IGCT1}$ = 75°C, $T_{j,IGCT2}$ = $T_{j,GCD}$ = 25°C). Furthermore, time difference between the turn-off signals ( gate to cathode voltages) of the IGCT gate units of $t_{delay}$ = 50 ns, 100ns were realized. Figure 5.4 shows the test circuit to investigate the series connection of IGCTs with anti-parallel GCDs during turn-off transients.

The main reason for the different turn-off switching behavior of series connected IGCTs is the variation of irradiation, which results in a different amount of storage charge within the device during the on-state, which has to be evacuated during the turn-off transient. The relation of this storage charge and its effect on the voltage deviation is explained in reference [6]. The amount of charge, which is stored in the IGCT is an excellent indicator for selecting devices to achieve an equal dynamic voltage sharing. However, this charge is difficult to measure and not available in actual production data. However, the on-state voltage, which also strongly depends on the storage charge could be used as a parameter to select and specify IGCTs for a series connection. As mentioned before, the storage charge is strongly dependent on the junction temperature of the device.

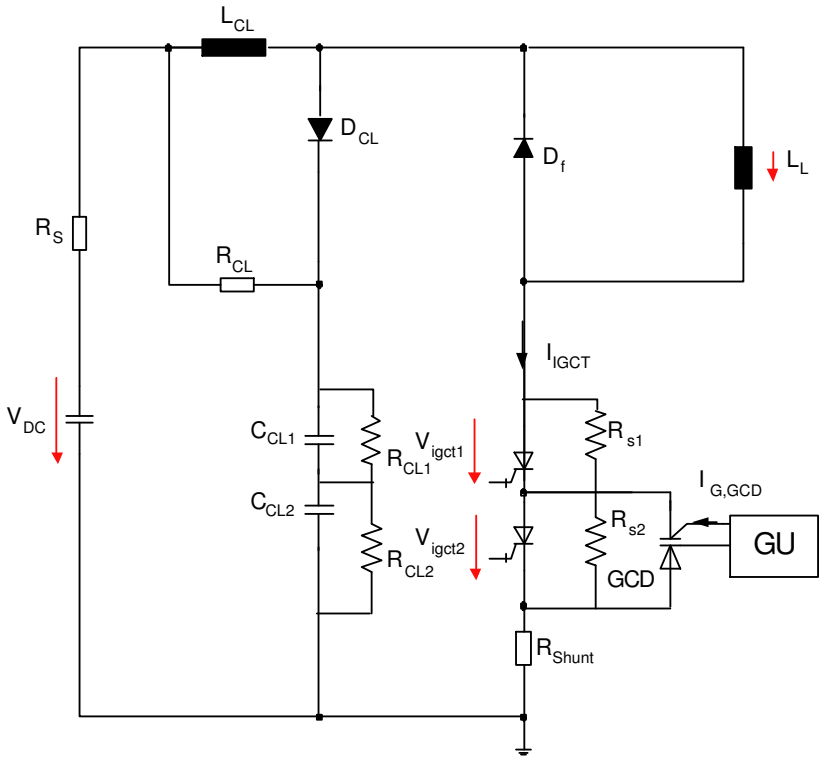



Figure 5.4: Test circuit for the investigation of the dynamic voltage symmetry of series connected IGCT switch positions ($V_{DC}$ = 2kV, 4kV, $I_L$ = 500A, 1kA, 2kA, $R_{CL}$ = 1.25 $\Omega$, $L_{CL}$ = 5.6 $\mu H$, $C_{CL1,2}$ = 1 $\mu F$, $R_{S1,2}$ = 30 k$\Omega$, $R_S$ = 0.2 $\Omega$, $L_L$ = 0.5 mH, IGCT1,2 : 5SHY 35L4503, GCD : IL226.10)

To investigate the voltage distribution of the depicted series connected IGCT switch positions the measurements are conducted at the following conditions

- Applied DC link voltage $V_{DC}$ = 2kV, 4kV
- Load current $I_L$ = 500A, 1kA, 2kA
- Clamp circuit : $R_{CL}$ = 1.25 $\Omega$, $L_{CL}$ = 5.6 $\mu H$, $C_{CL1,2}$ = 1 $\mu F$
- $R_{S1,2}$ = 30 k$\Omega$, $R_S$ = 0.2 $\Omega$, $L_L$ = 0.5 mH

- $T_{j,IGCT1}$ = 75°C, $T_{j,IGCT2}$ = $T_{j,GCD}$ = 25°C
- Turn-off time differences between the IGCT1 and IGCT2 $t_{delay}$ = 50ns, 100ns
- Devices under tests
  IGCT1,2 - 5SHY 35L4503, GCD - IL226.10

Figure 5.5 shows the physical arrangement of the stack with two series connected IGCTs and the GCD.

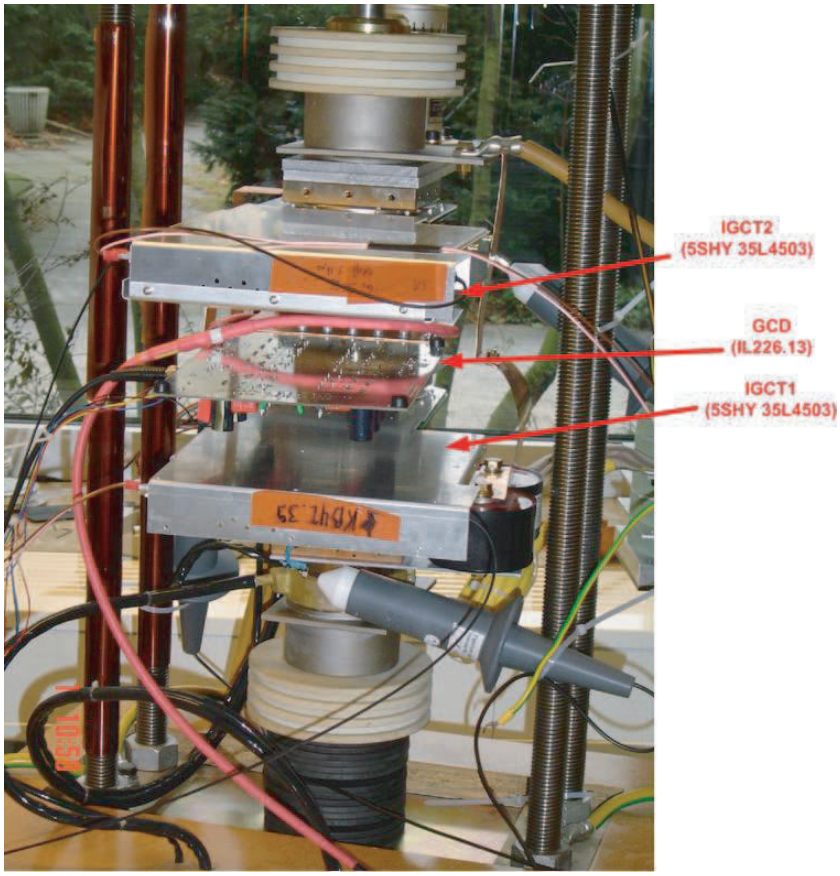



Figure 5.5: Physical test set-up for the voltage symmetry of IGCTs with GCD

The test circuit consists of two IGCTs (4.5kV / 5SHY 35L4503) in series. A GCD is connected anti-parallel to IGCT2, which is operated at substantially lower junction temperature. For a commutation of $I_L$ from the freewheeling diode $D_f$ to the IGCTs after active turn-on transients, the rise of current was limited to a maximum value of about $di/dt$ = 700 A / $\mu$s by selecting the value of the clamp inductance to $L_{clamp}$ = 5.6 $\mu H$. The size of the load inductance ($L_L$) is selected to ensure a quasi steady state charge carrier distribution in the IGCT while the load current increases. The clamp inductance $L_{CL}$ limits the short circuit current in the event of a failure of the IGCTs and diodes. The two clamp capacitors $C_{CL1,2}$ required for the 4kV measurements are symmetrically balanced by two parallel resistors. The static voltage symmetry of the IGCTs is achieved by connecting parallel resistors across each of the series connected switch positions.

A set of measurements is carried out to investigate if a GCD is able to balance the voltage symmetry of series connected IGCTs in principle. To achieve a very different switching behavior of IGCTs, the series connected devices are operated at very different junction temperatures. Furthermore, the operation of the IGCT series connection with the introduction of delay times of the IGCT turn-off signals is investigated. For the difference of the junction temperature of IGCTs, the temperatures of the two IGCTs are maintained at a certain defined value mentioned in the above test conditions by the use of heat sinks and one heater. Since the junction temperature of the IGCT2 ($T_{j,IGCT2}$ = 25°C) is substantially lower than that of the IGCT1 ($T_{j,IGCT1}$ = 75°C), the storage charge of the IGCT2 is smaller and it switches faster than IGCT1. Thus, the IGCT2 will take over a higher share of the blocking voltage compared to the IGCT1. However, the variation of the impressed gate current of the GCD will influence the blocking voltage of the IGCT2 $V_{IGCT2}$ such that a more equal voltage distribution can be achieved.

To clarify the effect of the voltage asymmetry due to a delay time interval between the gate unit signals, the IGCT2 is turned off before the IGCT1. Thus, IGCT2 takes a higher voltage share compared to the IGCT1.

To analyze the effect of the GCD on the voltage symmetry of the series connected IGCTs during their turn-off operation, initially measurements are carried out without any gate current impression in the GCD. Thus, at first a simple hard turn-off of series connected IGCTs is realized. After these measurements, different rectangular gate currents with different amplitudes and pulse durations were impressed into the GCD to determine a gate current amplitude and duration, which leads to an equal voltage distribution across both series connected switches. An input gate current with a desired pulse length and delay time is generated by the ArbLink software program on the computer and then transmitted to the arbitrary waveform generator (Fig. 3.8) for the adjustment of the amplitude of the gate current. With an impression of the gate current via the gate of the GCD a comparable procedure is carried out for the investigation of the influence of different delay times.

### 5.2.2 Results of experimental investigations

Assuming that the delay times between the turn-on signals of the series connected devices are sufficiently small, a turn-on transient of series connected IGCTs is uncritical compared to turn-off transients [6]. Thus the effect of the GCD is investigated for the series connection of IGCTs with very different storage charges caused by different junction temperatures and different gate signals delay times at turn-off transients respectively.

**Experimental investigation of series connected IGCTs with different switching behavior caused by different junction temperatures**

Figures 5.6 and 5.7 show the plot of turn-off voltages and currents of series connected IGCTs without and with GCD in operation respectively.

The operating conditions are characterized by a DC voltage of $V_{DC}$ = 2kV, a load current of $I_L$

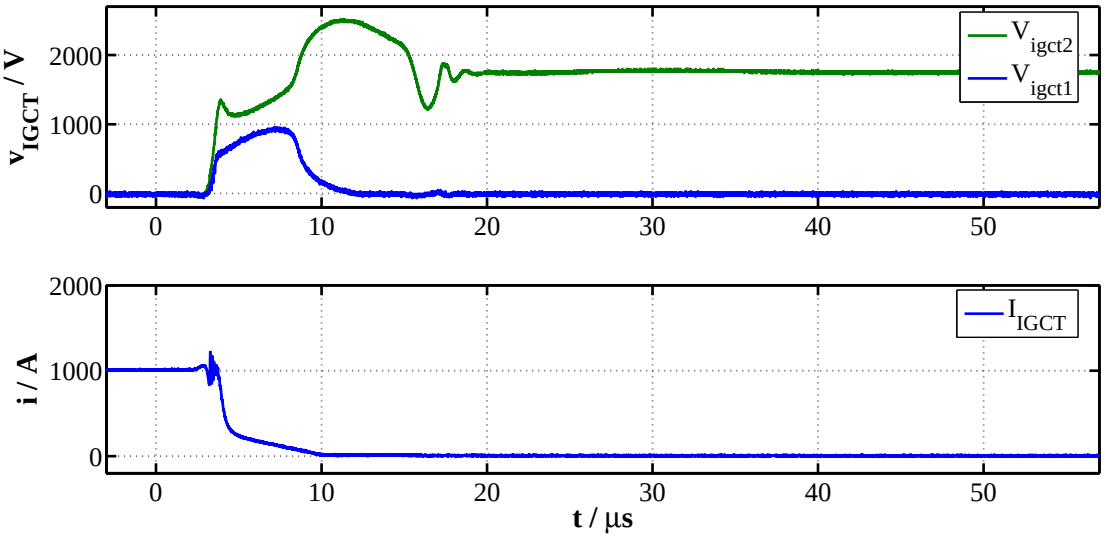



Figure 5.6: Turn-off waveform of an IGCT series connection without the impression of a gate current of GCD ($V_{DC}$ = 2kV, $I_L$ =1kA, $I_{G,GCD}$ = 0A, $T_{j,IGCT1}$ =75°C, $T_{j,IGCT2}$ = 25°C)

= 1kA and a junction temperature of $T_{j,IGCT1}$ = 75°C and $T_{j,IGCT2}$ = $T_{j,GCD}$ = 25°C. A GCD gate current of $I_{G,GCD}$ = 0A is the reason therefore that the GCD is not effective during the turn-off transient of Figure 5.6. During the turn-off transient of Figure 5.6 the storage charge of the device IGCT2 with the lower junction temperature is substantially smaller than that of the IGCT1 with the higher junction temperature. Thus, the storage charge of the IGCT2 is evacuated faster and it takes a higher blocking voltage especially at the end of the turn-off transient. Initially, both devices take over blocking voltages. Obviously, the device resistance of the IGCT2 increases faster compared to hotter device IGCT1 during the decay of the tail current. Thus, IGCT2 takes over almost the complete DC voltage at the end of the turn-off transient.

Figure 5.7 shows the turn-off IGCT voltage and current waveforms at comparable test conditions with an impression of a gate current in the GCD. It can be seen that the impression of a rectangular gate current with an amplitude of $I_{G,GCD}$ = 150A and a pulse length of $t_{pulse}$ = 5 $\mu s$ during the tail current interval enables a symmetrical voltage distribution at the end of the turn-off transients.

Figure 5.8 and Figure 5.9 show the corresponding waveforms at $V_{DC}$ = 2kV, $I_L$ = 2kA. In that

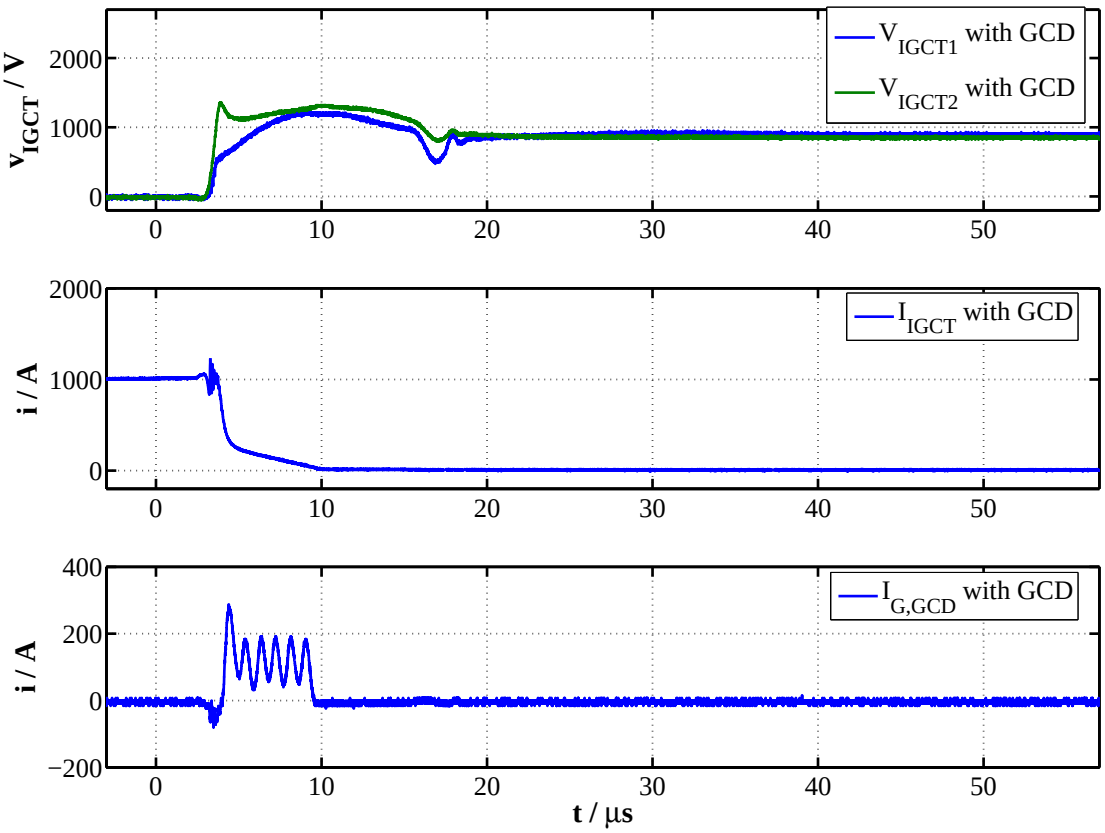



Figure 5.7: Turn-off waveform of an IGCT series connection with GCD gate current injection ($V_{DC}$ = 2kV, $I_L$ =1kA, $I_{G,GCD}$ = 150A, $t_{pulse}$ = 5 $\mu s$, $T_{j,IGCT1}$ =75°C, $T_{j,IGCT2}$ = 25°C, $Q_{Gate}$ = 0.81 mAs )

case the impression of a rectangular gate current with an amplitude of about $I_{G,GCD}$ = 200A and a pulse duration of $t_{pulse}$ = 5 $\mu s$ during the tail current interval is required to achieve a symmetrical voltage distribution of both series connected switches.

**Experimental investigation of series connected IGCTs with a delay time of the turn-off signals**

Figures 5.10 and 5.11 show the turn-off transients of IGCTs at an applied DC voltage of $V_{DC}$ = 2kV and a load current of $I_L$ = 1kA with a delay of the gate unit signals of 100ns.

In that case, the junction temperatures of both IGCTs are constant ($T_{j,IGCT1}$ = $T_{j,IGCT2}$ = 25°C). Figure 5.10 shows that IGCT2 turns off about 100ns before IGCT1. Although an equal voltage sharing of the both IGCTs is achieved at the end of the tail current, IGCT2 takes over almost the entire DC voltage at the end of the turn-off transient. It is suspected that, after the decay of the tail current the effective device resistance of IGCT2 (which was turned off 100 ns before IGCT1) is drastically higher than that of IGCT1.

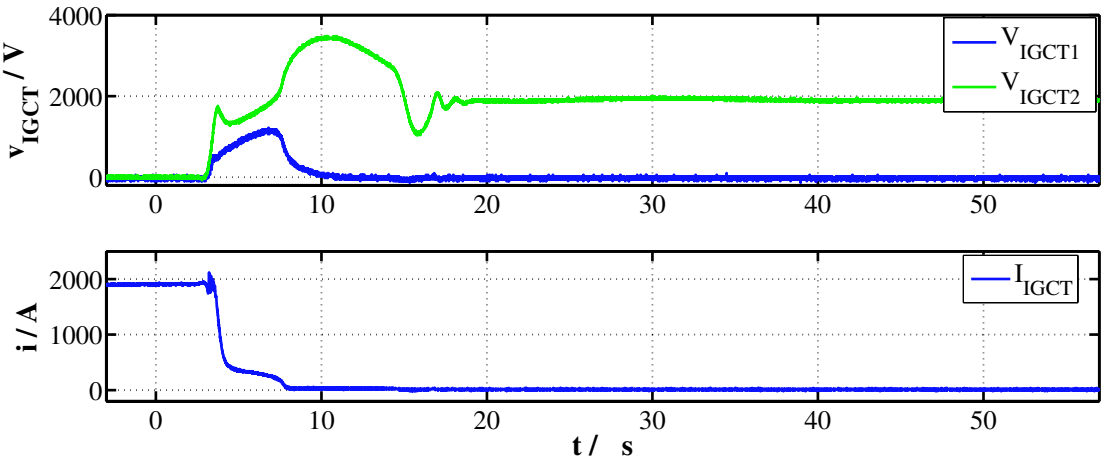



Figure 5.8: Turn-off waveform of an IGCT series connection without GCD gate current impression ($V_{DC}$ = 2kV, $I_L$ =2kA, $I_{G,GCD}$ = 0A, $T_{j,IGCT1}$ =75°C, $T_{j,IGCT2}$ = 25°C)

Figure 5.11 shows the corresponding waveforms of the IGCT series connection in which, a rectangular gate current with an amplitude of $I_{G,GCD}$ = 50A and a pulse duration of $t_{pulse}$ = 5 $\mu s$ is impressed in the GCD during the tail current interval. In that case, an almost equal voltage sharing of both series connected switch positions is achieved.

Figure 5.12 and 5.13 show the corresponding waveforms at $V_{DC}$ = 2kV, $I_L$ = 2kA and $T_{j,IGCT1}$, $T_{j,IGCT2}$ = 25°C. Again IGCT1 is turned off 100ns after IGCT2. It can be seen from Figure 5.13, that the impression of a rectangular gate current with an amplitude of $I_{G,GCD}$ = 50A and a pulse duration of $t_{pulse}$ = 5 $\mu s$ during the tail current interval enables an almost symmetrical voltage distribution.

The two series connected IGCTs are turned off at DC voltage of $V_{DC}$ = 4kV and a load current of $I_L$ = 1kA with the gate unit turn-off signal delay of 400ns in Figure 5.14 and Figure 5.15. In that case, the impression of a gate current with an amplitude of about $I_{G,GCD}$ = 200A and a pulse duration of $t_{pulse}$ = 2 $\mu s$ leads to a symmetrical voltage distribution of both series connected IGCTs.

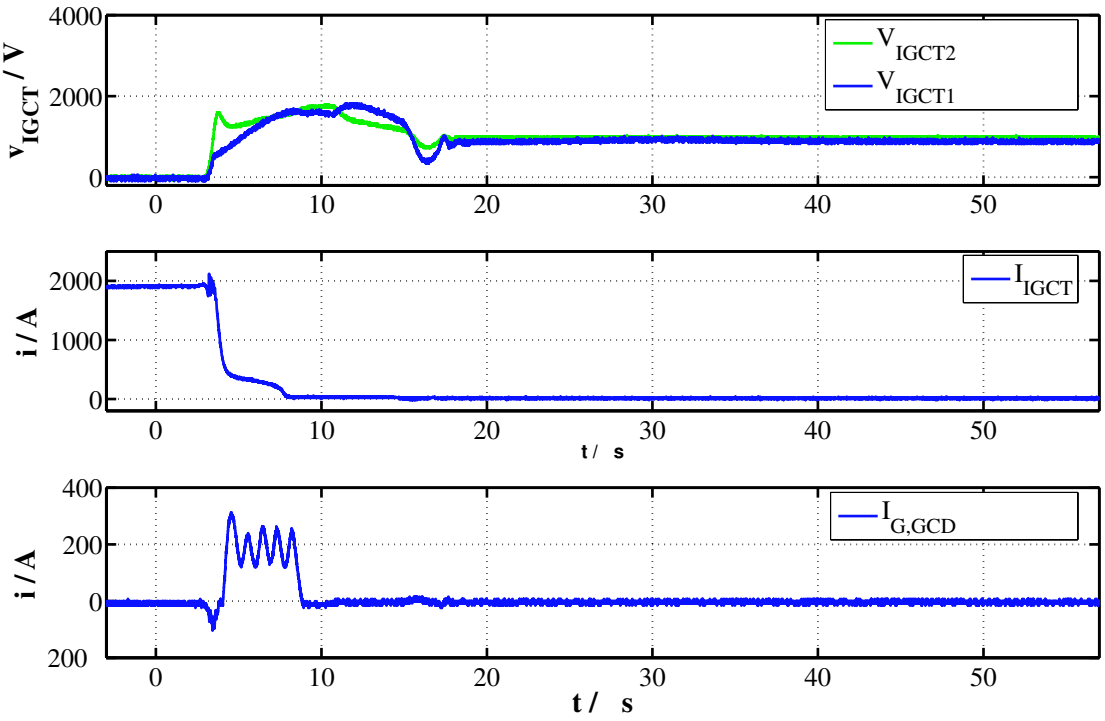



Figure 5.9: Turn-off waveform of an IGCT series connection with GCD gate current injection ($V_{DC}$ = 2kV, $I_L$ =2kA, $I_{G,GCD}$ = 200A, $t_{pulse}$ = 5 $\mu s$, $T_{j,IGCT1}$ =75°C, $T_{j,IGCT2}$ = 25°C, $Q_{Gate}$ = 0.81 mAs )

## 5.3 Comparison of series connected IGCTs with RC snubber and GCD

It has been already mentioned in chapter 4 that RC or RCD snubbers are the conventional voltage balancing networks, which can be used to enable a series connection of IGCTs. To compare the series connection of IGCTs with RC-snubber and a GCD a test setup analyzing a RC snubber voltage balancing network according to the reference [6] was realized ( Figure 5.16). The test circuit comprises the snubber components $R_{S1,2}$ = 1 Ω, $C_{S1,2}$ = 0.5 $\mu$ F, $R_{P1,2}$ = 30 kΩ. Figure 5.17 shows the physical structure of the IGCT stack with the RC snubber network.

Figure 5.18 shows the turn-off waveforms of IGCTs with RC voltage balancing network of the above mentioned values at $V_{DC}$ = 2kV, $I_L$ =2kA, $T_{j,IGCT1}$,$T_{j,IGCT2}$ = 25°C, $t_{IGCT1}$ = $t_{IGCT2}$ +100ns. It can be seen from figure 5.18 that a voltage deviation of the series connected IGCTs of about 500V is obtained.

Figure 5.19 shows that by the use of a GCD in a circuit configuration according to Figure 5.4, a voltage difference of only 100V can be achieved at comparable conditions, if a gate current of $I_{G,GCD}$ = 50A and a pulse duration of $t_{pulse}$ = 5 $\mu s$ is impressed in the GCD during the tail current interval. Obviously, the RC snubber can be avoided, if GCDs are applied instead of conventional diodes.

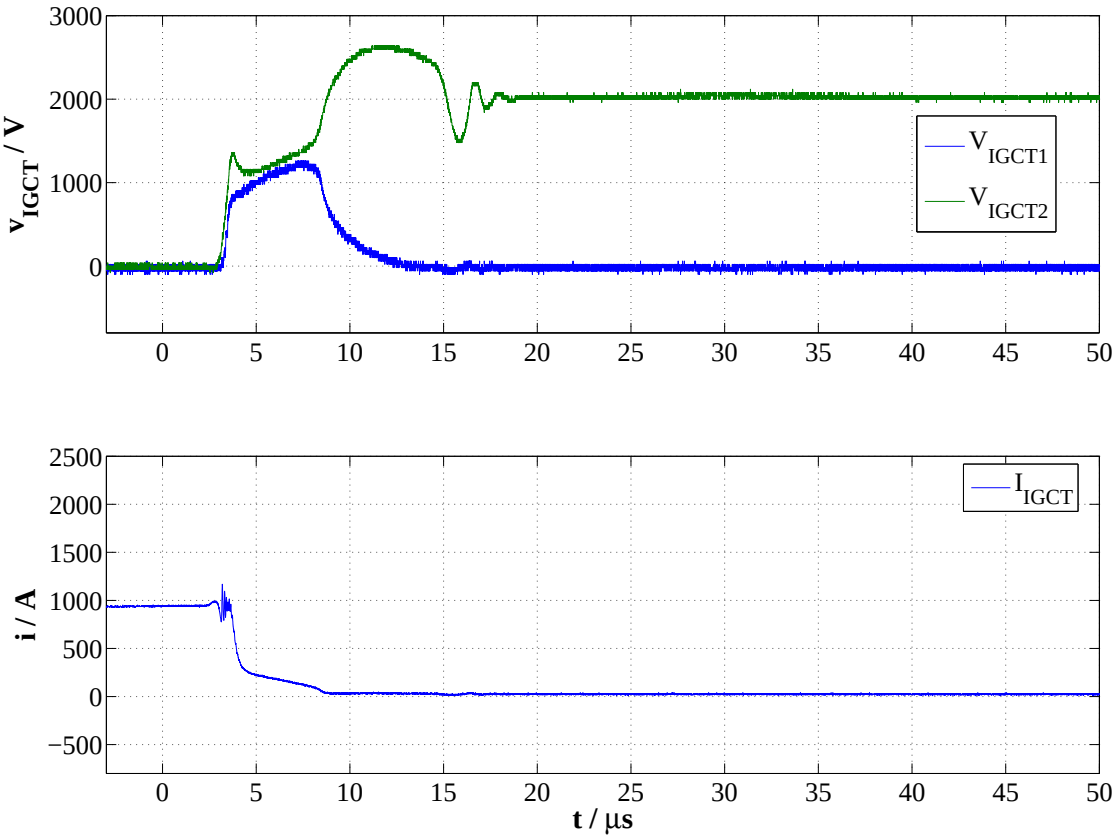



Figure 5.10: Turn-off waveform of an IGCT series connection without GCD gate current injection ($V_{DC}$ = 2kV, $I_L$ =1kA, $I_{G,GCD}$ = 0A, $T_{j,IGCT1}$,$T_{j,IGCT2}$ = 25°C, $t_{IGCT1}$ = $t_{IGCT2}$ +100ns)

Although an extra gate unit and its control is necessary for an optimum gate current value of the GCD, the achieved results are promising. The results of the experimental investigation of a series connection of IGCTs with anti-parallel GCDs showed that GCDs can control the voltage distribution of a series connected IGCT switch position during static and dynamic states. However, a GCD gate unit, which impresses the required gate current to achieve a symmetrical voltage distribution is an important requirement for such a new snubberless concept. Figure 5.20 shows a possible general block diagram of such a gate unit.

Figure 5.21 depicts a schematic of the voltage waveform of two series connected IGCTs. It shows the main requirements for the turn-off transients in which $V_{DRM}$ is the maximum repetitive voltage of IGCTs. During the voltage rise and the demagnetization of the clamp, the gate unit must make sure that the maximum blocking voltage of the device is not exceeded. After that, the impression of a gate current must guarantee that the device voltage stays below the 100 FIT device blocking voltage.

One concept to realize such a gate unit requires the measurement of the IGCT voltage $V_{AK}$ and

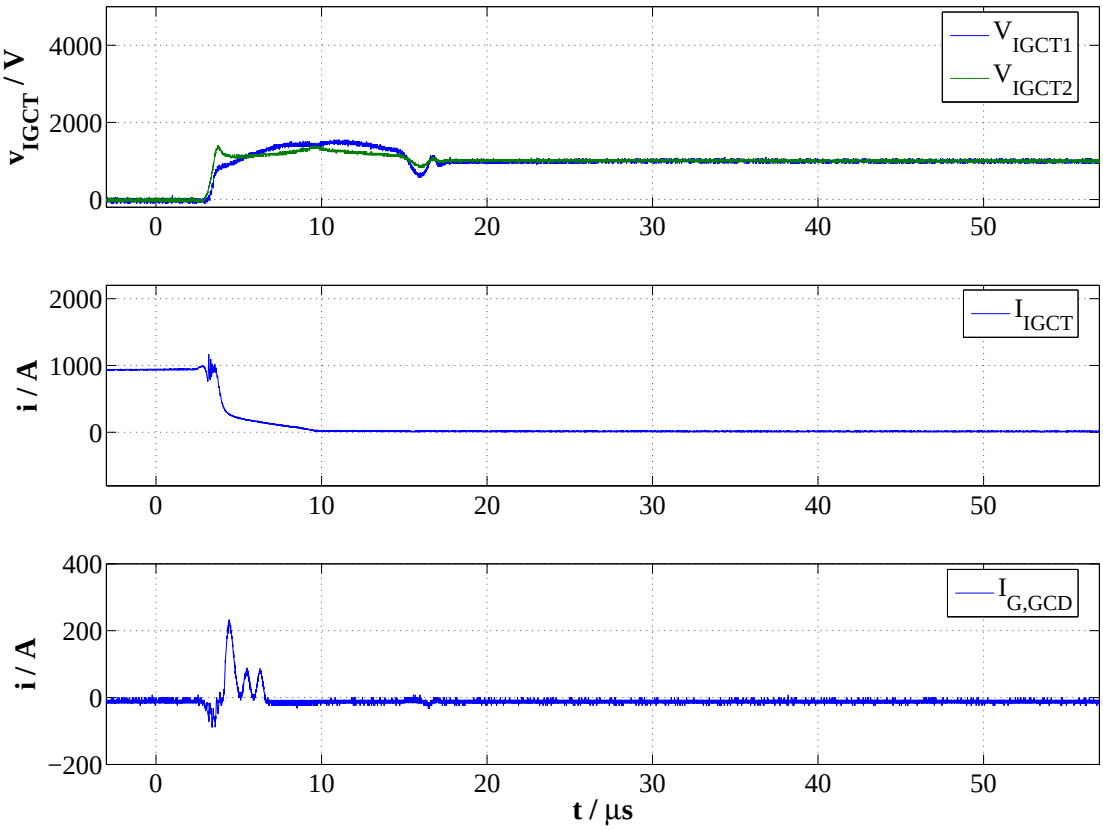



Figure 5.11: Turn-off waveform of an IGCT series connection with GCD gate current injection ($V_{DC}$ = 2kV, $I_L$ =1kA, $I_{G,GCD}$ = 50A, $t_{pulse}$ = 5 $\mu s$, $T_{j,IGCT1}$,$T_{j,IGCT2}$ = 25°C, $t_{IGCT1}$ = $t_{IGCT2}$ +100ns, $Q_{Gate}$ = 0.31 mAs)

the communication of the ideal blocking voltage to the GCD gate unit from the converter or the Power Electronic Building Blocks (PEBB) control [24]. The realization of the requirement ($V_{AK} \leq V_{DRM}$) could be realized by the GCD gate unit independently. The adjustment of the stationary device blocking voltage ($V_{AK} \leq V_{AK,100FIT}$) could be realized according to a reference value, which is sent by the converter control. However, the additional fiber optic cable for the communication of a reference value for the stationary device blocking voltage is certainly a disadvantage.

## 5.4 Summary

Chapter 5 has discussed the experimental investigation of the static and dynamic voltage distribution of series connected IGCTs with anti-parallel GCDs.

During the blocking state an equal voltage distribution of the series connection of IGCTs can be achieved by the injection of a suitable low GCD gate current. For the GCD sample IL226.10,

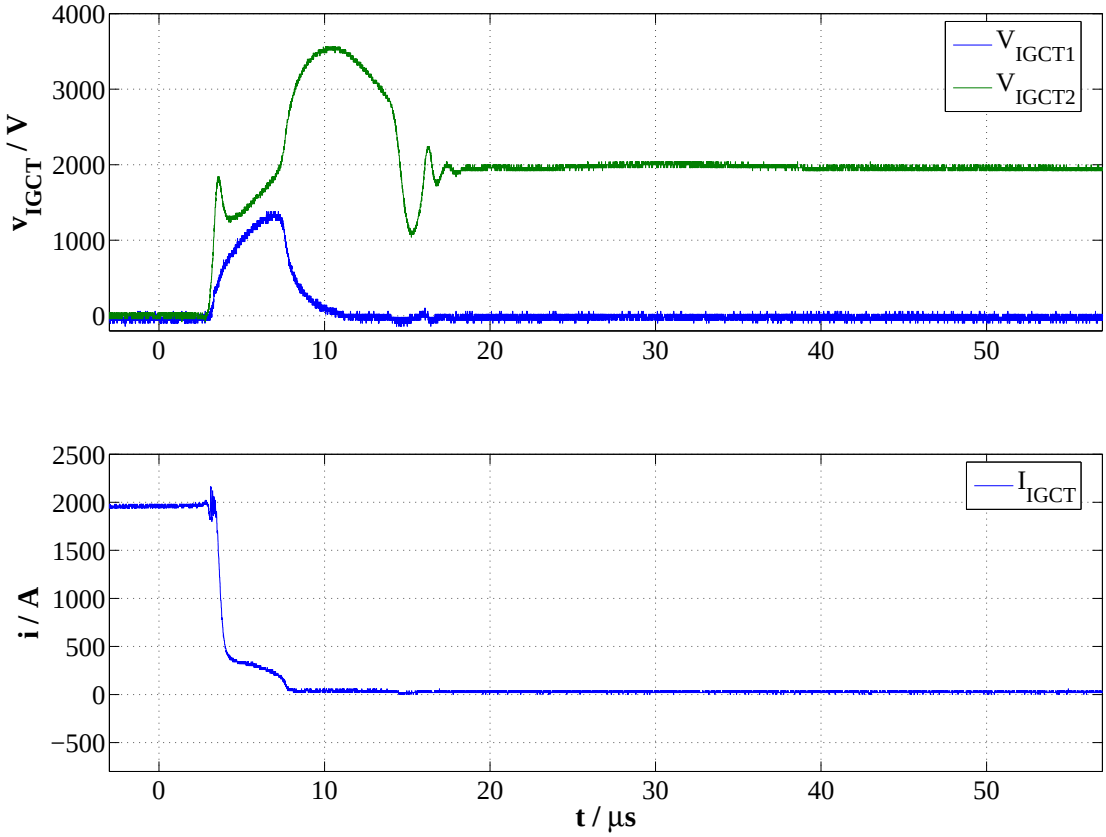



Figure 5.12: Turn-off waveform of an IGCT series connection without GCD gate current injection ($V_{DC}$ = 2kV, $I_L$ =2kA, $I_{G,GCD}$ = 0A, $T_{j,IGCT1}$, $T_{j,IGCT2}$ = 25°C, $t_{IGCT1}$ = $t_{IGCT2}$ +100ns)

the impression of a gate current of $I_{G,GCD}$ = 6 mA at $V_{DC}$ = 1000V and $T_{j,IGCT1}$ = 25°C, $T_{j,IGCT2}$ = 115°C enables an equal static voltage distribution of the series connected IGCTs, while for $V_{DC}$ = 2000V and $T_{j,IGCT1}$ = 25°C, $T_{j,IGCT2}$ = 115°C equal static voltage distribution is achieved by the impression of a gate current of $I_{G,GCD}$ = 8 mA.

During turn-off transients an equal dynamic voltage distribution of $\Delta$ V $\leq$ 100 V can be achieved by the impression of rectangular GCD gate currents $I_{G,GCD}$ = 50 A to 200A with pulse durations of $t_{pulse}$ = 5 $\mu$ s at $V_{DC}$ = 2000V, $I_L$ = 2000A for series connected IGCTs with extreme different operating temperatures ($T_{j,IGCT1}$ = 25°C, $T_{j,IGCT2}$ = 75°C) and for large turn-off time delay differences (e.g. 100ns and 400ns) respectively.

Thus it has been proved that a GCD is able to achieve a symmetrical voltage distribution of a series connected IGCT switch positions in principle. This concept can be developed further for a closed loop control of the GCD .

The application of the GCD in series connected IGCTs switch positions is interesting since it can replace the use of conventional snubber network and avoid the associated drawbacks.

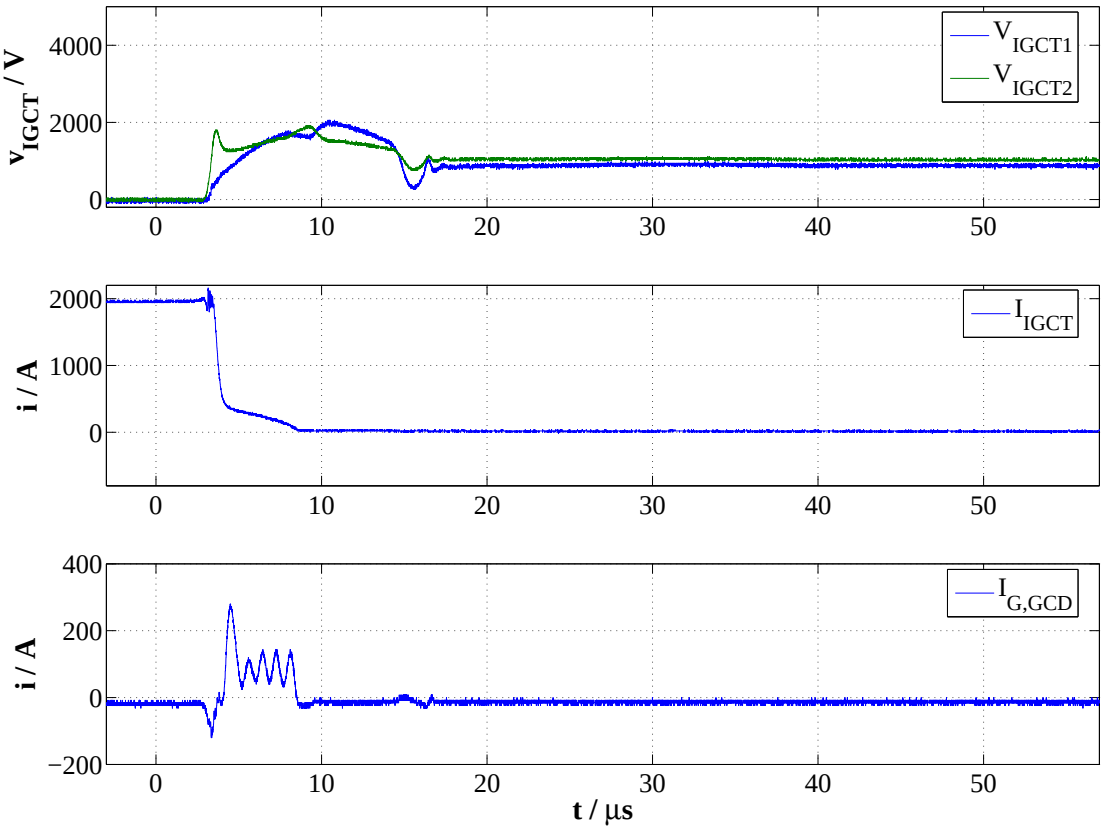



Figure 5.13: Turn-off waveform of an IGCT series connection with GCD gate current injection ($V_{DC}$ = 2kV, $I_L$ =2kA, $I_{G,GCD}$ = 50A, $t_{pulse}$ = 5 $\mu s$, $T_{j,IGCT1}$,$T_{j,IGCT2}$ = 25°C, $t_{IGCT1}$ = $t_{IGCT2}$ +100ns, $Q_{Gate}$ = 0.31 mAs)

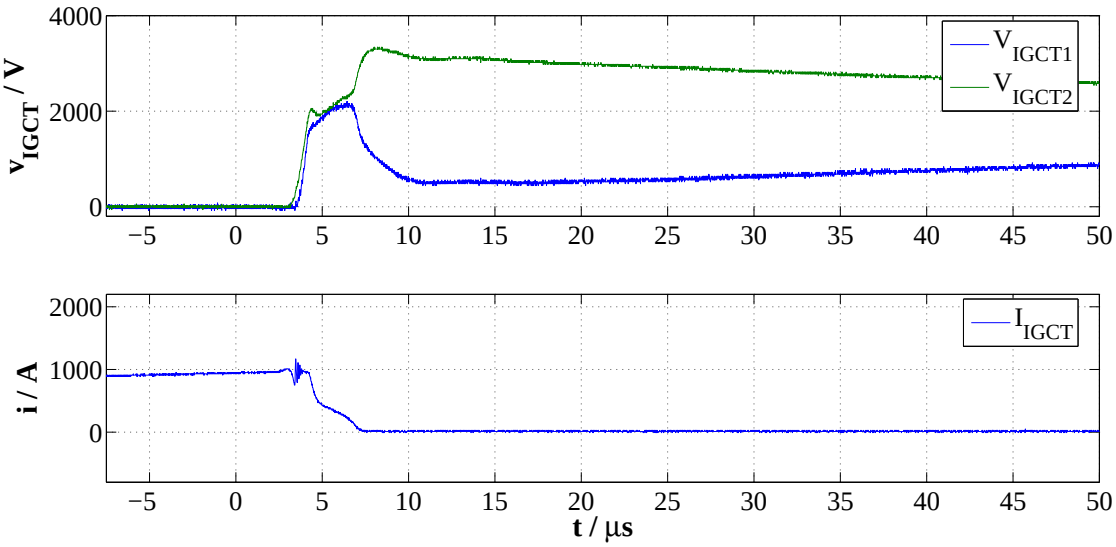



Figure 5.14: Turn-off waveform of an IGCT series connection without GCD gate current impression ($V_{DC}$ = 4kV, $I_L$ = 1kA, $I_{G,GCD}$ = 0A, $T_{j,IGCT1}$,$T_{j,IGCT2}$ = 25°C, $t_{IGCT1}$ = $t_{IGCT2}$ +400ns)

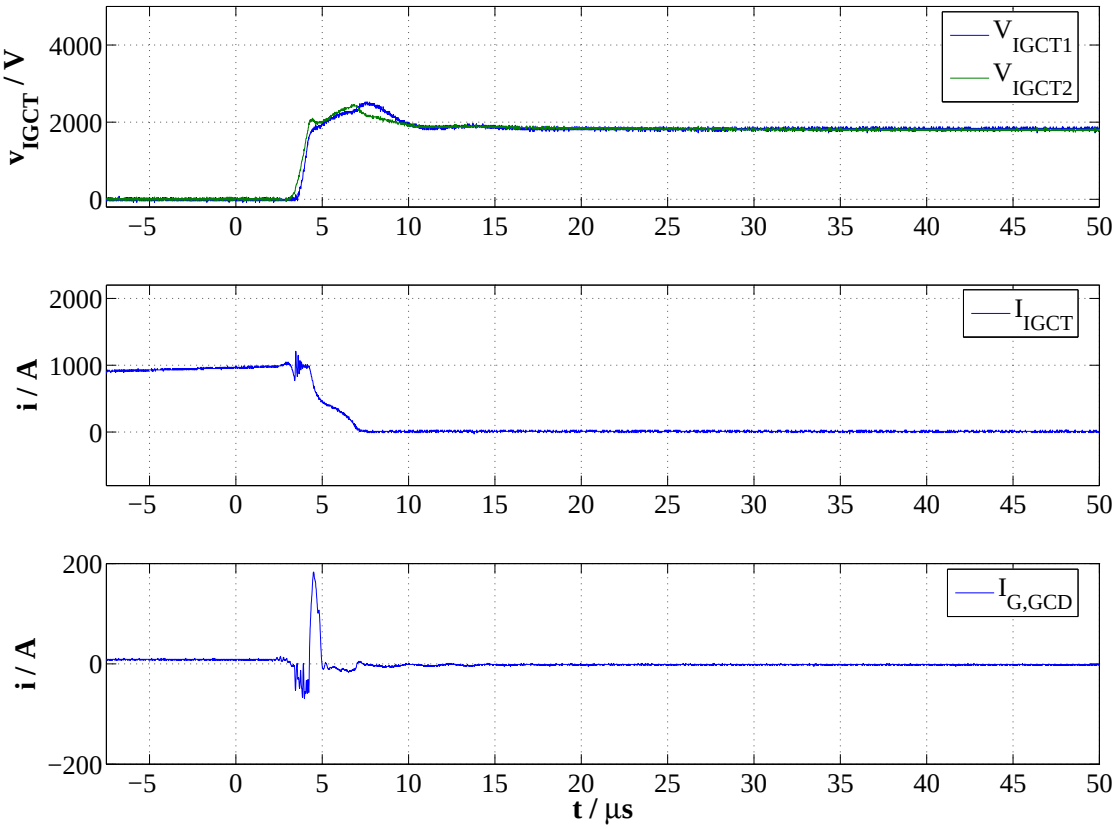



Figure 5.15: Turn-off waveform of an IGCT series connection with GCD gate current impression ($V_{DC}$ = 4kV, $I_L$ = 1kA, $I_{G,GCD}$ = 200A, $t_{pulse}$ = 2 $\mu s$, $T_{j,IGCT1}$,$T_{j,IGCT2}$ = 25°C, $t_{IGCT1}$ = $t_{IGCT2}$ +400ns, $Q_{Gate}$ = 0.25 mAs)

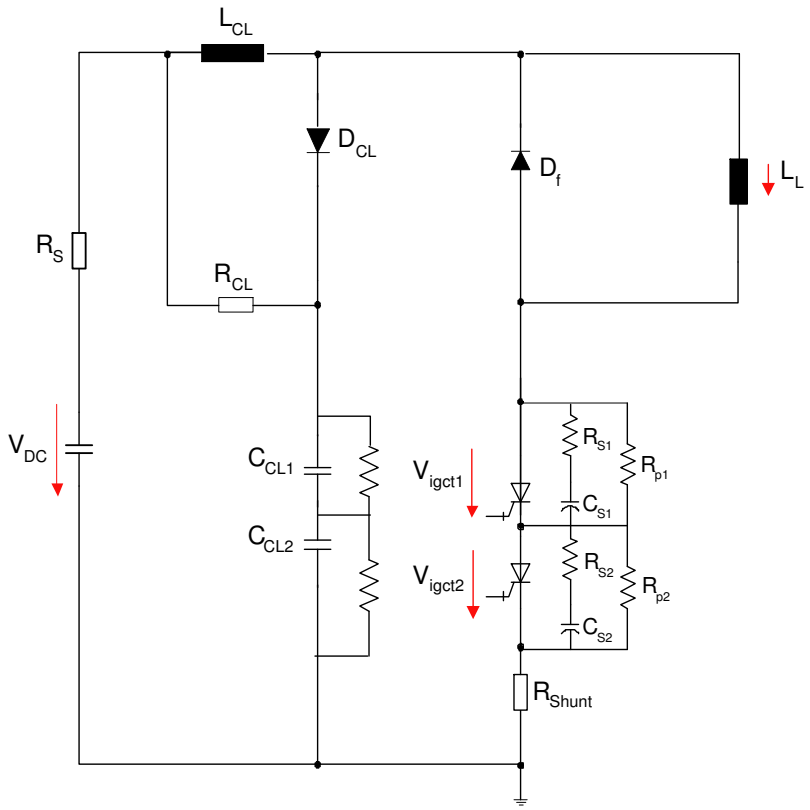



Figure 5.16: Test circuit of IGCT series connection with RC snubber ($V_{DC}$ = 2 kV, $I_L$ = 2 kA, $T_{j,IGCT1,IGCT2}$ = 25°C, $L_L$ = 0.5 mH, $R_S$ = 0.2 Ω, $R_{CL}$ = 1.25 Ω, $C_{CL}$ = 1 $\mu$ F, $L_{CL1,2}$ = 5.6 $\mu$ F, $R_{S1,2}$ = 1 Ω, $C_{S1,2}$ = 0.5 $\mu$ F, $R_{P1,2}$ = 30 kΩ)

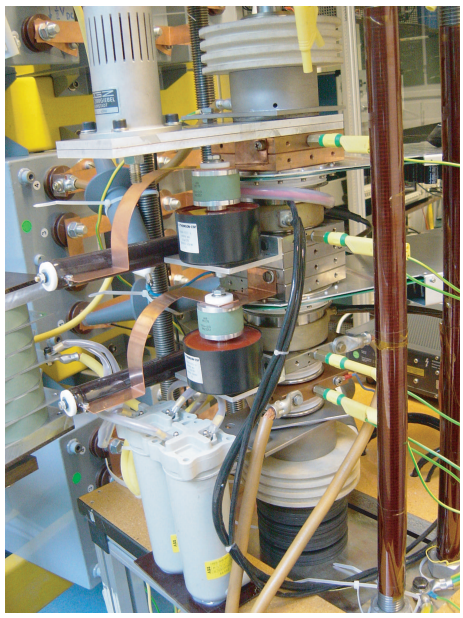


Figure 5.17: Physical arrangement of an IGCT series connection with RC snubber

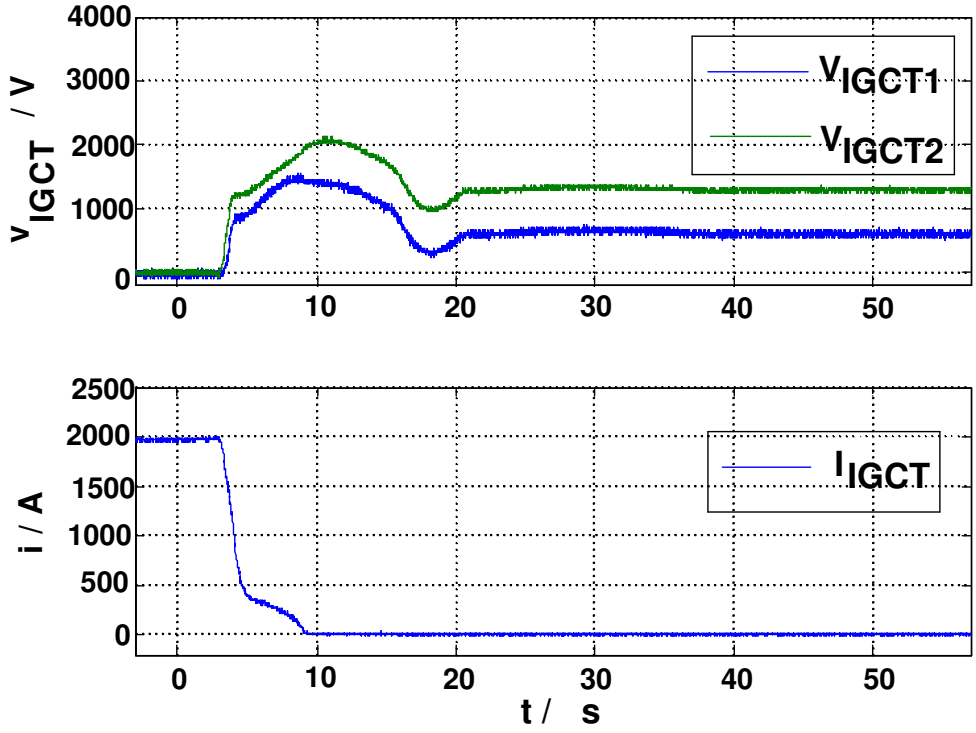



Figure 5.18: Turn-off waveform of an IGCT series connection with RC snubber ($V_{DC}$ = 2kV, $I_{IGCT}$ =2kA, $T_{j,IGCT1,2}$ = 25°C, $t_{IGCT1}$ = $t_{IGCT2}$ +100ns, $R_{S1,2}$ = 1 Ω, $C_{S1,2}$ = 0.5 $\mu$ F , $R_{S1,2}$ = 30 kΩ)

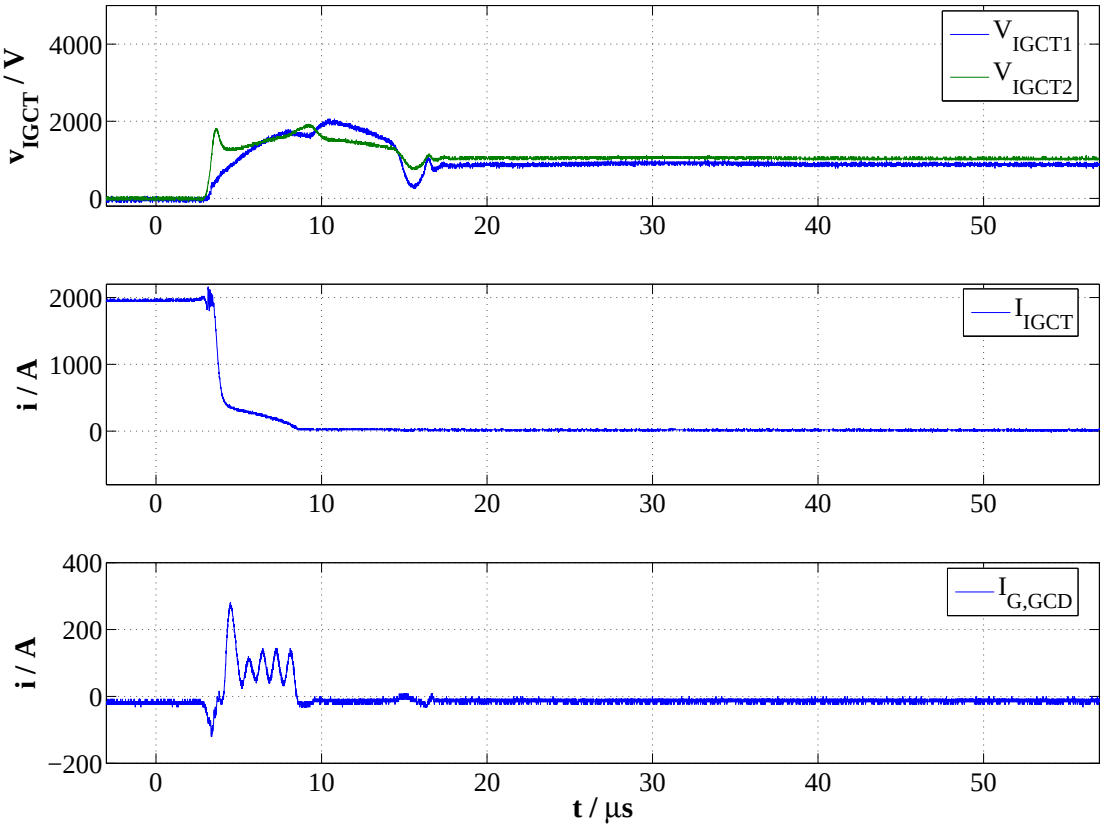



Figure 5.19: Turn-off waveform of an IGCT series connection with GCD gate current impression ($V_{DC}$ = 2kV, $I_{IGCT}$ =2kA, $I_{G,GCD}$ = 50A, $I_{G,GCD}$ = 5 $\mu s$, $T_{j,IGCT1,2}$ = 25°C, $t_{IGCT1}$ = $t_{IGCT2}$ +100ns, $Q_{Gate}$ = 0.31 mAs)

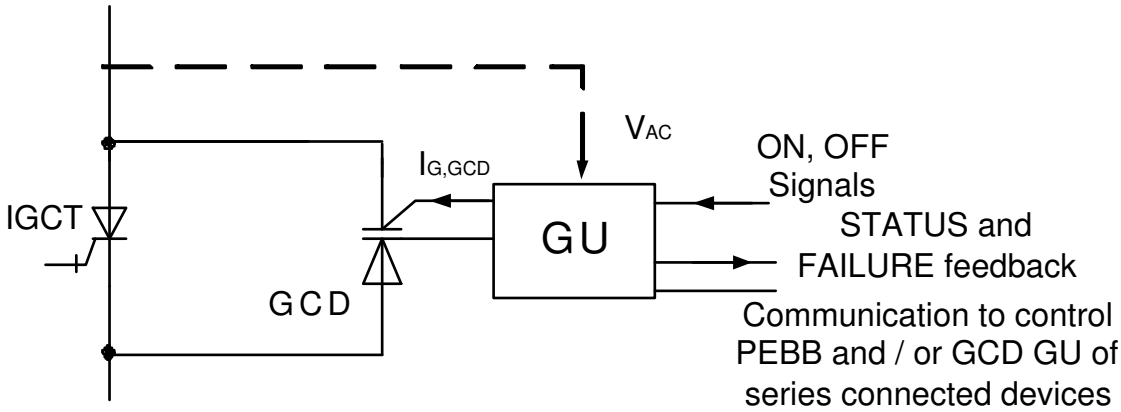



Figure 5.20: Block diagram of the GCD gate unit concept

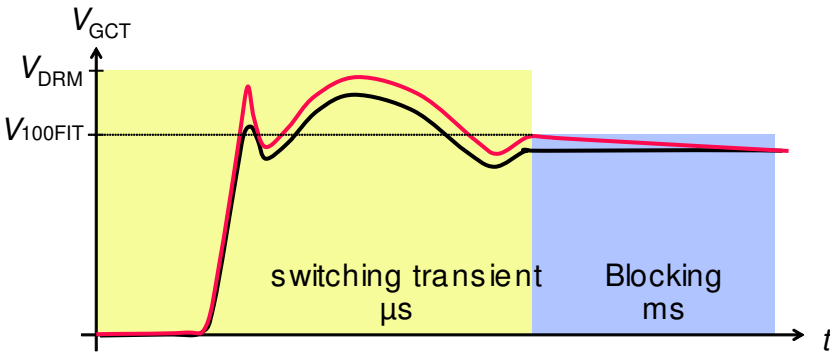



Figure 5.21: Schematic of Voltage waveform and requirements of two IGCT switch positions

# Chapter 6

# Conclusion

In this thesis the new diode concept called Gate Controlled Diode (GCD) is discussed. The world's first prototypes of GCDs are characterized and investigated for the IGCT series connection. The basic concept of this p+nn+ diode resulted from the idea of a snuberless IGCT series connection. The samples provided and preliminarily tested by ABB, Switzerland are further investigated experimentally at Berlin University of Technology.

Generally, to achieve a higher output voltage in medium voltage drives a series connection of IGCTs is a straight forward solution. However, the IGCT device characteristics require external networks to achieve a symmetrical static and dynamic voltage distribution. Disadvantages of voltage balancing networks, which include passive energy storages (e.g. capacitors) are increased losses, space and part count.

In the GCD, a gate current impression enables an adjustment of the leakage current during the blocking state. The leakage current of the GCD in the blocking mode depends on the junction temperature and the applied DC voltage. For a specified applied voltage and temperature, the leakage current poses an almost linear relation with the impressed gate current i.e. the current ratio of the impressed gate current and the leakage current of the GCD is about unity.

In the turn-off mode, the impression of the gate current influences the reverse recovery behavior. The soft reverse recovery behavior of a GCD depends on several parameters of the gate current like gate current shape and gate current charge. Assuming a rectangular gate current the gate current pulse duration $t_{pulse}$, delay time $t_{delay}$ referring the zero crossing of the anode current and the gate current amplitude $I_{G,GCD}$ are important parameters. Like in conventional diode, the reverse recovery behavior of a GCD also depends on the anode current, the rate of current fall, the commutation voltage, the commutation inductance and the junction temperature. The influences of these parameters were investigated in detail. The experimental investigation of a GCD at different operating points (e.g. $V_{DC}$, $I_L$, $T_j$) and parameters (e.g. $t_{pulse}$, $t_{delay}$, $I_{G,GCD}$) showed that the impression of a gate current influences the interruption of the reverse recovery current and therefore the reverse recovery charge $Q_{rr}$, the diode fall time $t_f$ and the softness factor of a GCD. Like expected the most effective gate current impression is close to the occurrence of the peak reverse recovery current $I_{rr}$. Furthermore, it also showed that the impression of a large gate current has a stronger effect on the change in the reverse recovery behavior than a smaller gate current. The adjustable reverse recovery current was the basis for an investigation

of a series connection of IGCTs with anti-parallel GCDs without additional snubber networks.

In the blocking state of series connected IGCT switch positions the impression of a low gate current (e.g. 6 to 10 mA) is required to achieve static voltage symmetry. However, the achievement of an effective dynamic voltage symmetry during IGCT turn-off transients at different device junction temperatures and turn-off time delays requires larger gate current pulses of short durations during the IGCT tail currents. As an example gate currents of $I_{G,GCD}$ = 50 to 300 A with a pulse duration of $t_{pulse}$ 5 to 10 $\mu$s were required to enable an equal voltage sharing of two series connected IGCTs operating at a junction temperature difference of $\Delta\ T_j$ = 50°K and turn-off time delay deviation of $\Delta$ t = 100ns. The snuberless IGCT series connection was verified at several operating points.

Furthermore it was shown that an anti-parallel GCD can also reduce the IGCT turn-off current. The experimental results showed that the instantaneous losses of an IGCT were reduced by almost 500 KW at $V_{DC}$ = 2kV, $I_L$ = 1kA, $T_j$ = 25°C by the impression of the gate current $I_{G,GCD}$ = 200A in the GCD during the IGCT turn-off transient

The results of the characterization of a GCD and the investigation of a GCD for the snubberless IGCT series connection shows promising results. Assuming that a suitable, reliable and low cost GCD gate unit can be developed, this new device concept could replace the conventional snubber networks in a series connection of IGCT switch positions or it could be used in the development of a fast high voltage soft recovery diode (e.g. 10 kV GCD).

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# Appendix

# Appendix A

# GCD Gate unit details

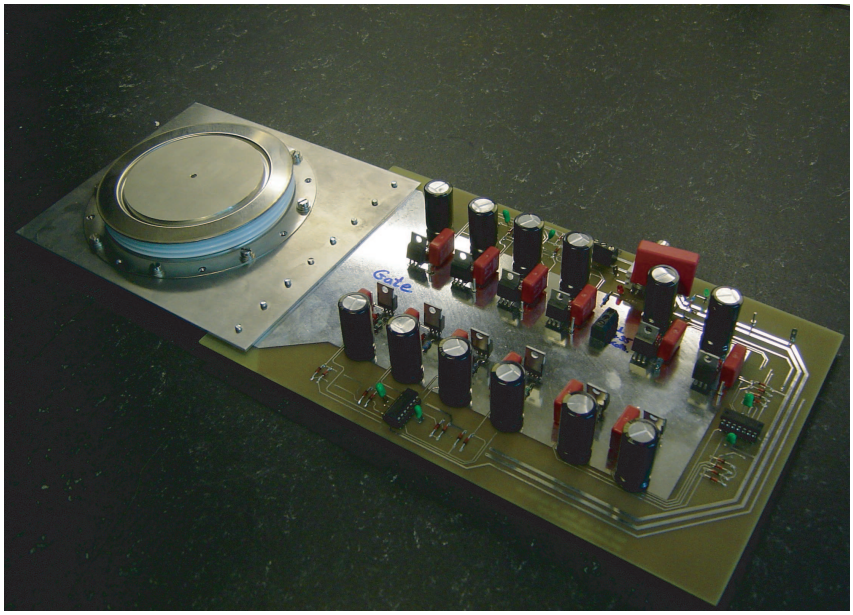



Figure A.1: Photo of 91mm GCD with universal low inductive gate unit

## A.1 Connection details

The gate unit with gate contact on the top side and cathode contact on the bottom side is contacted to the GCD terminals. Table A.1 shows the details of the connection of the terminals. Plots A.5 and A.6 show the measurement test results of the gate unit with rectangular and sine wave inputs and corresponding current output.

During the experimental investigation of the GCD, an oscillation in the gate current is observed. This oscillations are caused by the oscillation of the series resonant circuit formed by the stray inductance of the GCD gate circuit and the capacitance of the gate cathode junction.

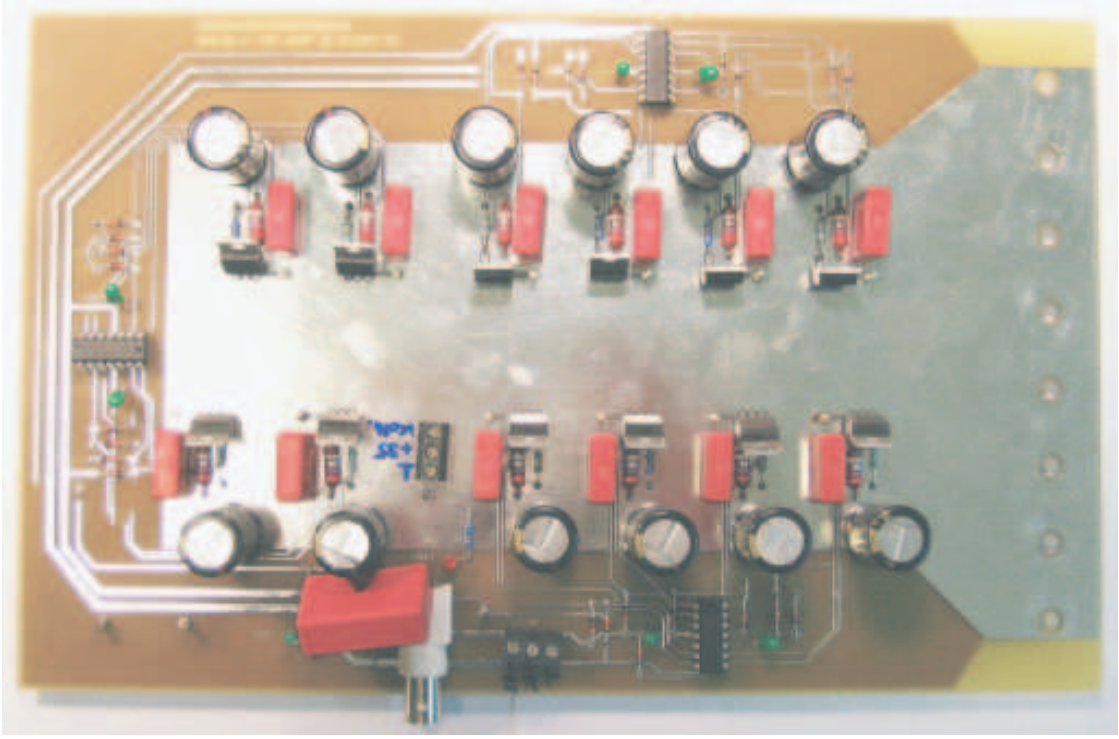


Figure A.2: Gate unit-Photo

| Contact Pin | Singal | Function |
|---|---|---|
| X1-1 | GND | Ground |
| X1-2 | +15V | OP supply |
| X1-3 | -15V | OP supply |
| X2-1 | GND | Ground |
| X2-2 | +35V | End stage supply |
| X2-3 | Cathode | Cathode diode connection |
| | $u_{in}$ | input signal |

Table A.1: Gate unit connection

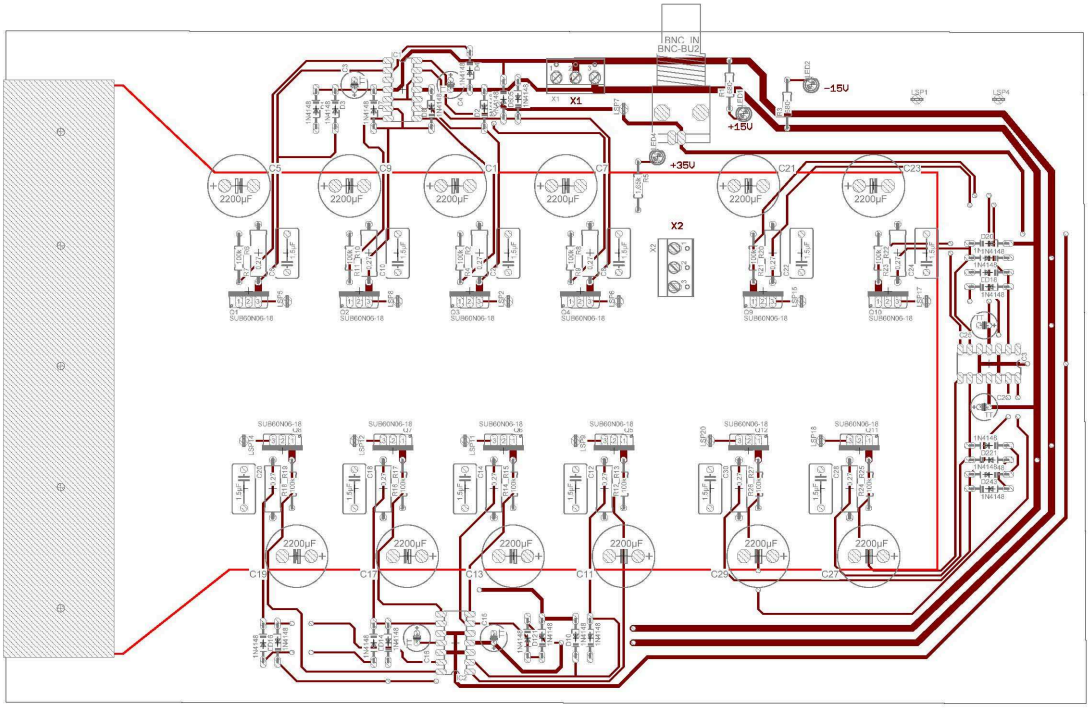
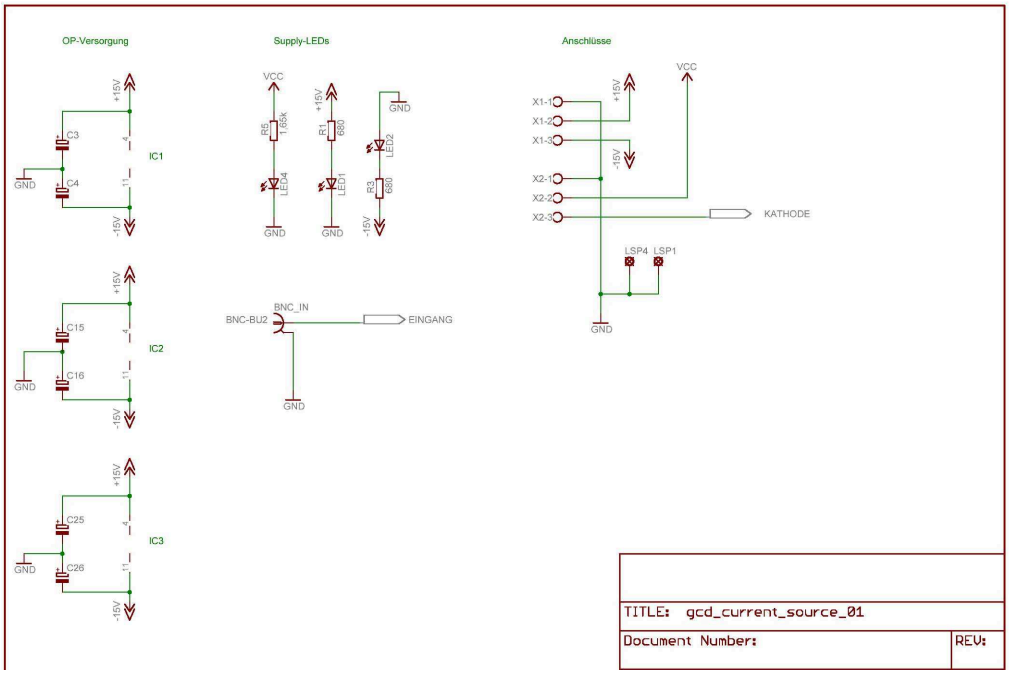



Figure A.3: Universal GCD gate unit- PCB Layout



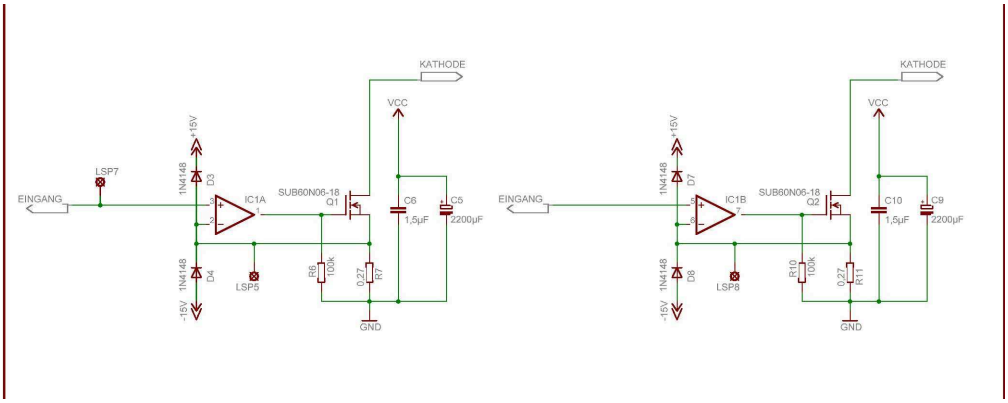



Figure A.4: Circuit diagram of universal gate unit

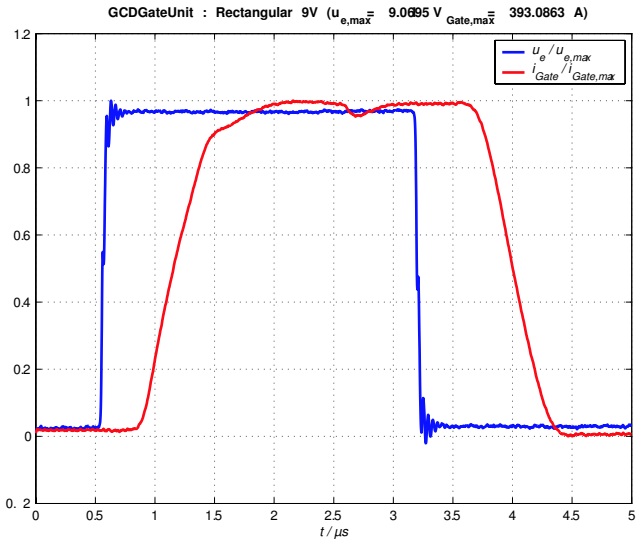



Figure A.5: Gate unit Measurement with 9V Rectangular voltage input

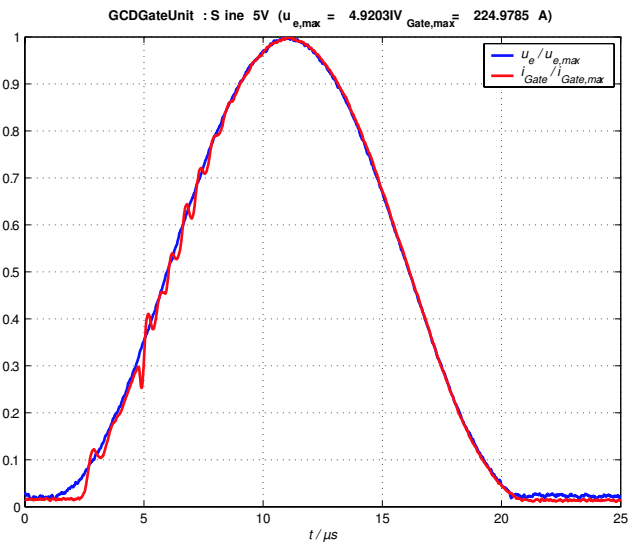



Figure A.6: Gate unit Measurement with 5V Sine voltage input

# Appendix B

# Data Sheets

- Data sheet of ABB Diode - 5SDF 16L4502
- Data sheet of ABB 4.5kV IGCT - 5SHY 35L4503

**Key Parameters**

| | | |
|---|---|---|
| $V_{RRM}$ | = | 4500 V |
| $I_{FAVM}$ | = | 1300 A |
| $I_{FRMS}$ | = | 2000 A |
| $I_{FSM}$ | = | 33 kA |
| $V_{F0}$ | = | 2.00 V |
| $r_F$ | = | 0.55 mΩ |
| $V_{DClink}$ | = | 2800 V |

# Fast Recovery Diode for IGCT applications

# 5SDF 16L4502

## MARKETING INFORMATION

Doc. No. 5SYA 1153-00 Feb. 99

### Features

- **Patented free-floating silicon technology**
- **Industry standard housing**
- **Cosmic radiation withstand rating**
- **Low on-state and switching losses**
- **Optimized to use in snubberless operation**

### Blocking

| | | | | | |
|---|---|---|---|---|---|
| $V_{RRM}$ | Repetitive peak reverse voltage | 4500 | V | Half sine wave, $t_P$ = 10 ms, f = 50 Hz | |
| $I_{RRM}$ | Repetitive peak reverse current | ≤ 50 | mA | $T_j$ = 115 °C | $V_R = V_{RRM}$ |
| $V_{DClink}$ | Permanent DC voltage for 100 FIT failure rate | 2800<br>3200 | V<br>V | 100% Duty<br>5% Duty | Ambient cosmic radiation at sea level in open air. |

### Mechanical

| | | | |
|---|---|---|---|
| $F_M$ | Mounting force | min. | 36 kN |
| | | max. | 70 kN |
| a | Acceleration:<br>Device unclamped<br>Device clamped | | <br>50 $m/s^2$<br>200 $m/s^2$ |
| m | Weight | | 1.45 kg |
| $D_S$ | Surface creepage distance | | 35 mm |
| $D_a$ | Air strike distance | | 14 mm |

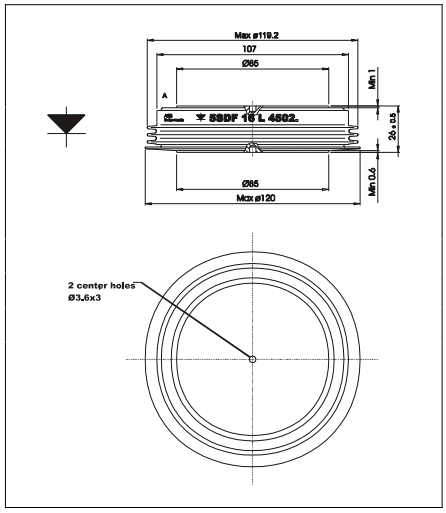



**Fig. 1**
Outline drawing.
All dimensions are in millimeters and represent nominal values unless stated otherwise.

ABB Semiconductors AG

## On-state

| | | | | | |
|---|---|---|---|---|---|
| $I_{FAVM}$ | Max. average on-state current | 1300 A | Half sine wave, $T_c$ = 70 °C | | |
| $I_{FRMS}$ | Max. RMS on-state current | 2000 A | | | |
| $I_{FSM}$ | Max. peak non-repetitive surge current | 33 kA | $t_p$ = | 10 ms | Before surge |
| | | 115 kA | $t_p$ = | 1 ms | $T_j$ = 115 °C |
| $\int I^2dt$ | Max. surge current integral | $5.45 \cdot 10^6$ $A^2s$ | $t_p$ = | 10 ms | After surge: |
| | | $6.6 \cdot 10^6$ $A^2s$ | $t_p$ = | 1 ms | $V_R \approx 0V$ |
| $V_F$ | Forward voltage drop | ≤ 4.20 V | $I_F$ = | 4000 A | |
| $V_{F0}$ | Threshold voltage | 2.00 V | Approximation for | | $T_j$ = 115 °C |
| $r_F$ | Slope resistance | 0.55 mΩ | $I_F$ = 800…5000 A | | |

## Turn-on

| | | | |
|---|---|---|---|
| $V_{fr}$ | Peak forward recovery voltage | ≤ 30 V | di/dt = 500 A/µs, $T_j$ = 115 °C |

## Turn-off

| | | | | |
|---|---|---|---|---|
| $di/dt_{crit}$ | Max. decay rate of on-state current | ≤ 1000 A/µs | $I_F$ = 4000 A, $T_j$ = 115 °C<br>$V_{DClink}$ = 2700 V | |
| $I_{rr}$ | Reverse recovery current | ≤ 1500 A | $I_F$ = 4000 A, | $V_{DClink}$ = 2700 V |
| $Q_{rr}$ | Reverse recovery charge | ≤ 7000 µC | di/dt = 1000 A/µs, | $T_j$ = 115 °C |

## Thermal

| | | | | |
|---|---|---|---|---|
| $T_j$ | Operating junction temperature range | -40...115 °C | | |
| $T_{stg}$ | Storage temperature range | -40…125 °C | | |
| $R_{thJC}$ | Thermal resistance junction to case | ≤ 18 K/kW | Anode side cooled | $F_M$ = 36…44 kN |
| | | ≤ 18 K/kW | Cathode side cooled | |
| | | ≤ 9 K/kW | Double side cooled | |
| $R_{thCH}$ | Thermal resistance case to heatsink | ≤ 5 K/kW | Single side cooled | |
| | | ≤ 2.5 K/kW | Double side cooled | |

## On-state characteristics

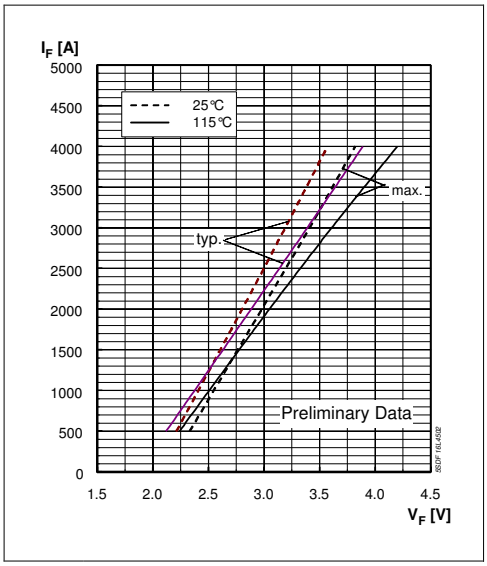



**Fig. 2** Forward current vs. forward voltage (typ. and max. values).

## Surge current characteristics

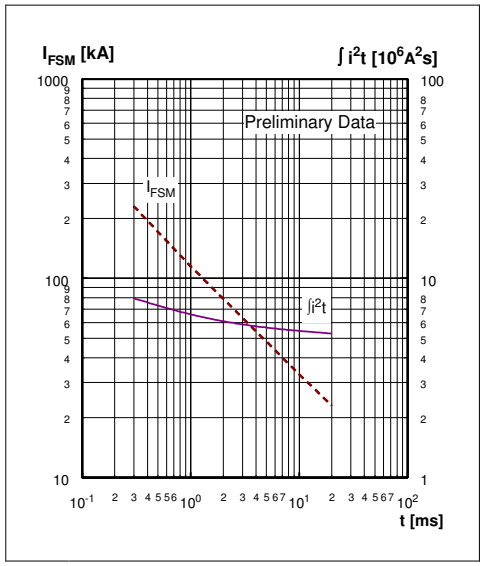



**Fig. 3** Surge current and fusing integral vs. pulse width (max. values) for non-repetitive, half-sinusoidal surge current pulses.

## Turn-on characteristics

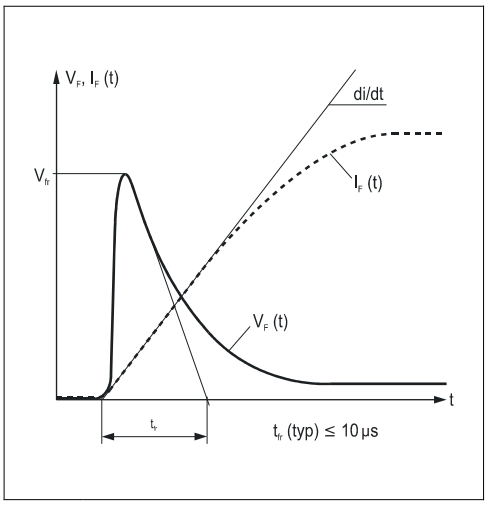



**Fig. 4** Typical forward voltage waveform when the diode is turned on with a high di/dt

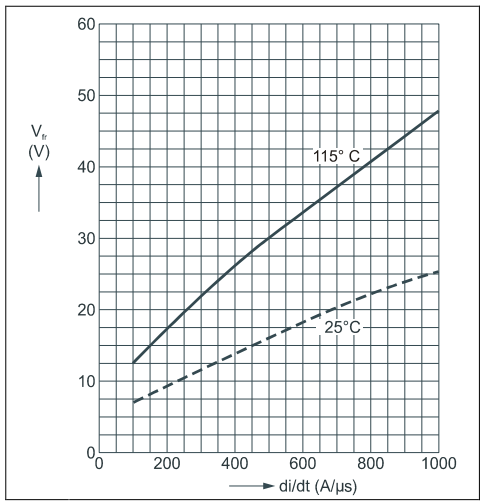



**Fig. 5** Forward recovery voltage vs. turn-on di/dt (max. values)

| | | |
|---|---|---|
| $V_{DRM}$ | = | 4500 V |
| $I_{TGQM}$ | = | 4000 A |
| $I_{TSM}$ | = | 32 kA |
| $V_{T0}$ | = | 1.40 V |
| $r_T$ | = | 0.325 mΩ |
| $V_{DClink}$ | = | 2800 V |

# Asymmetric Integrated Gate-Commutated Thyristor

# 5SHY 35L4503

Doc. No. 5SYA1228-01 Jan. 01

- **Highest snubberless turn-off rating**
- **Suitable for series connection**
- **Fast response ($t_{don}$ < 3 µs, $t_{doff}$ < 6 µs)**
- **High reliability**
- **Very high EMI immunity**
- **Simple fibre optic control interface and status feedback**
- **Cosmic radiation withstand rating**

## Blocking

| | | | | | |
|---|---|---|---|---|---|
| $V_{DRM}$ | Repetitive peak off-state voltage | | 4500 | V | $V_{GR} \geq 2V$ |
| $I_{DRM}$ | Repetitive peak off-state current | ≤ | 50 | mA | $V_D = V_{DRM}$ $V_{GR} \geq 2V$ |
| $V_{DClink}$ | Permanent DC voltage for 100 FIT failure rate | | 2800 | V | Ambient cosmic radiation at sea level in open air. |

## Mechanical data (see Fig. 8)

| | | | | | |
|---|---|---|---|---|---|
| $F_m$ | Mounting force | min. | 36 | kN | |
| | | max. | 44 | kN | |
| $D_p$ | Pole-piece diameter | | 85 | mm | ±0.1 mm |
| H | Housing thickness | | 26 | mm | ±0.5 mm |
| m | Weight IGCT | | 3.30 | kg | |
| $D_s$ | Surface creepage distance | ≥ | 33 | mm | Anode to Gate |
| $D_a$ | Air strike distance | ≥ | 13 | mm | Anode to Gate |
| l | Length IGCT | | 451 | mm | ±1.0 mm |
| h | Height IGCT | | 40 | mm | ±1.0 mm |
| w | Width IGCT | | 213 | mm | ±1.0 mm |

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## GCT Data

### On-state (see Fig. 2, 3 ,4)

| | | | | |
|---|---|---|---|---|
| $I_{TAVM}$ | Max. average on-state current | 1345 A | Half sine wave, $T_C$ = 85 °C | |
| $I_{TRMS}$ | Max. RMS on-state current | 2110 A | | |
| $I_{TSM}$ | Max. peak non-repetitive surge current | 32 kA | $t_p$ = 10 ms | $T_j$ = 125 °C |
| | | 47 kA | $t_p$ = 1 ms | After surge: $V_D = V_R$ = 0V |
| $I^2t$ | Limiting load integral | $5.1 \cdot 10^6$ $A^2s$ | $t_p$ = 10 ms | |
| | | $1.1 \cdot 10^6$ $A^2s$ | $t_p$ = 1 ms | |
| $V_T$ | On-state voltage | ≤ 2.70 V | $I_T$ = 4000 A | $T_j$ = 125 °C |
| $V_{T0}$ | Threshold voltage | 1.40 V | $I_T$ = 1000 - 4000 A | |
| $r_T$ | Slope resistance | 0.325 mΩ | | |

### Turn-on switching

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $di/dt_{crit}$ | Max. rate of rise of on-state current | 1000 A/µs | f = 500 Hz | | $T_j$ = 125 °C | | |
| | | | $I_T$ = 4000 A | | $V_D$ = 2500 V | | |
| $t_{don}$ | Turn-on delay time | ≤ 3 µs | $V_D$ = 2500 V | | $T_j$ = 125 °C | | |
| $t_r$ | Rise time | ≤ 1 µs | $I_T$ = 4000 A | | | | |
| $t_{on\ (min)}$ | Min. on-time | 10 µs | $R_s$ = 0.8 Ω | | $L_i$ = 2.2 µH | | |
| $E_{on}$ | Turn-on energy per pulse | ≤ 1.5 J | $C_{CL}$ = 6.0 µF | | $L_{CL}$ = 0.3 µH | | |

### Turn-off switching (see Fig. 5, 6)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_{TGQM}$ | Max. controllable turn-off current | 4000 A | $V_{DM}$ ≤ $V_{DRM}$ | | $T_j$ = 125 °C | | |
| | | | $V_D$ = 2500 V | | $L_{CL}$ = 0.3 µH | | |
| $t_{doff}$ | Turn-off delay time | ≤ 6.0 µs | $V_D$ = 2500 V | | $V_{DM}$ ≤ $V_{DRM}$ | | |
| $t_f$ | Fall time | ≤ 1.0 µs | $T_j$ = 125 °C | | $R_s$ = 0.8 Ω | | |
| $t_{off\ (min)}$ | Min. off-time | 10 µs | $I_{TGQ}$ = 4000 A | | $L_i$ = 2.2 µH | | |
| $E_{off}$ | Turn-off energy per pulse | ≤ 19.5 J | $C_{CL}$ = 6.0 µF | | $L_{CL}$ = 0.3 µH | | |

## Gate Unit

| | | | |
|---|---|---|---|
| **Power supply** (see Fig. 7 to 9) | | | |
| $V_{GDC}$ | Gate Unit voltage | 20 ±0.5 $V_{DC}$ | Without galvanic isolation to power circuit. |
| $P_{Gin}$ | Gate Unit power consumption | ≤ 52 W | $f_S$ = 500 Hz, $I_{TGQ\ AV}$ = 1000 A, δ = 0.5 |
| X1 | Gate Unit power connector | AMP, Type 640389-4, MTA 156, friction lock, right angle Note 1 | |
| **Optical control input/output** (see Fig. 8 to 10) | | | |
| $P_{on\ CS}$ | Optical input power | > -21 dBm | Valid for 1mm plastic optical fibre (POF) |
| $P_{off\ CS}$ | Optical noise power | < -40 dBm | |
| $P_{on\ SF}$ | Optical output power | > -19 dBm | |
| $P_{off\ SF}$ | Optical noise power | < -50 dBm | |
| $t_{GLITCH}$ | Pulse width threshold | ≤ 300 ns | Max. pulse width without response |
| CS | Receiver for command signal | Agilent, Type HFBR-2528 Note 2 | |
| SF | Transmitter for status feedback | Agilent, Type HFBR-1528 Note 2 | |

Note 1: AMP, www.amp.com
Note 2: Agilent Technologies, www.semiconductor.agilent.com

## Thermal

| | | | | | |
|---|---|---|---|---|---|
| $T_j$ | Operating junction temperature range | | 0…125 | °C | |
| $T_{stg}$ | Storage temperature range | | -40…85 | °C | |
| $T_{amb}$ | Ambient operational temperature range | | 0…50 | °C | |
| $R_{thJC}$ | Thermal resistance junction to case | ≤ | 12 | K/kW | Double side cooled |
| | | ≤ | 20 | K/kW | Anode side cooled |
| | | ≤ | 30 | K/kW | Cathode side cooled |
| $R_{thCH}$ | Thermal resistance case to heatsink | ≤ | 6 | K/kW | Double side cooled |
| | | ≤ | 3 | K/kW | Single side cooled |

Analytical function for transient thermal impedance.

$$Z_{thJC}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/\tau_i})$$

| i | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| $R_i$(K/kW) | 5.4 | 4.5 | 1.7 | 0.4 |
| $\tau_i$(s) | 1.2 | 0.17 | 0.01 | 0.001 |
| $F_M$ = 36… 44 kN Double side cooled | | | | |

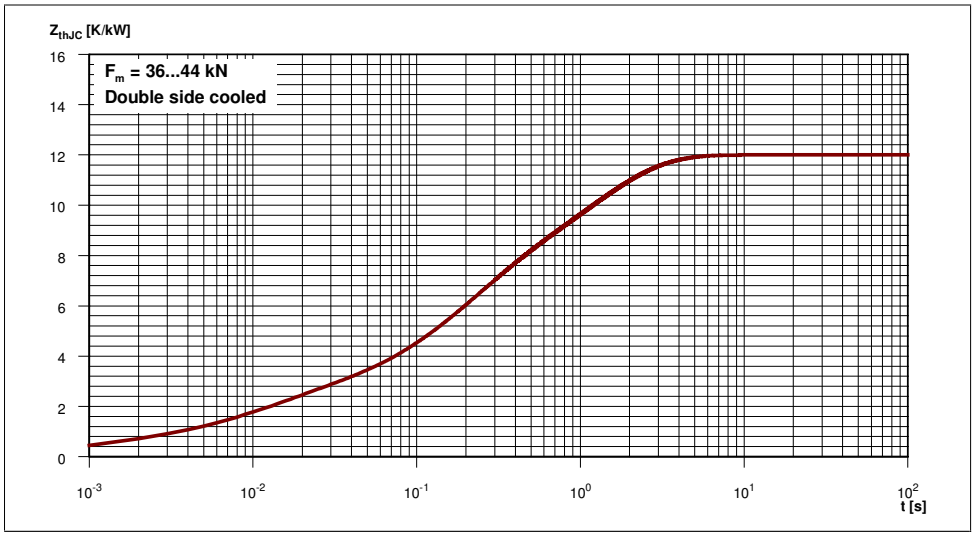


Fig. 1 Transient thermal impedance (junction-to-case) versus time (max. values).

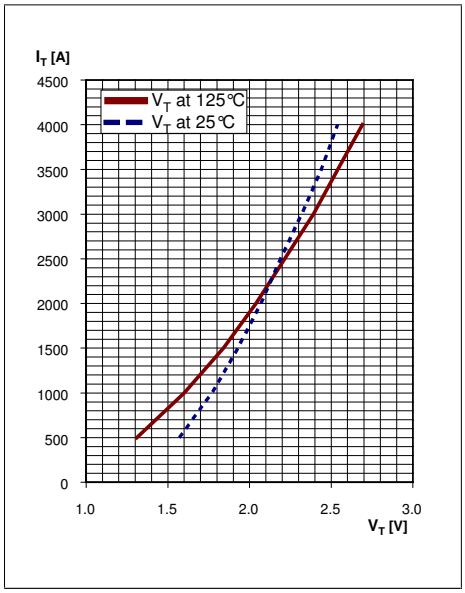


Fig. 2 GCT on-state characteristics.

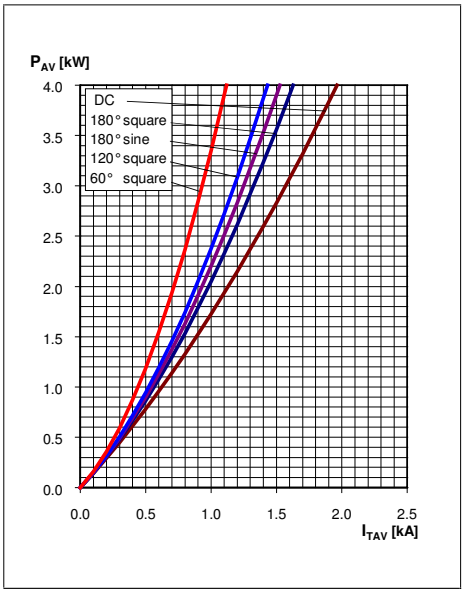


Fig. 3 Average on-state power dissipation versus on-state current.

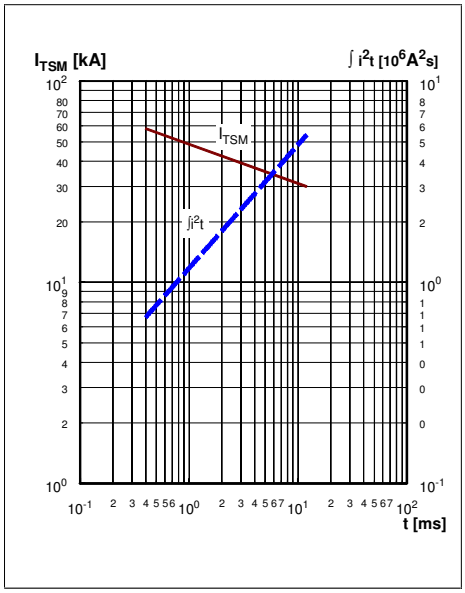


Fig. 4 Surge current and fusing integral versus

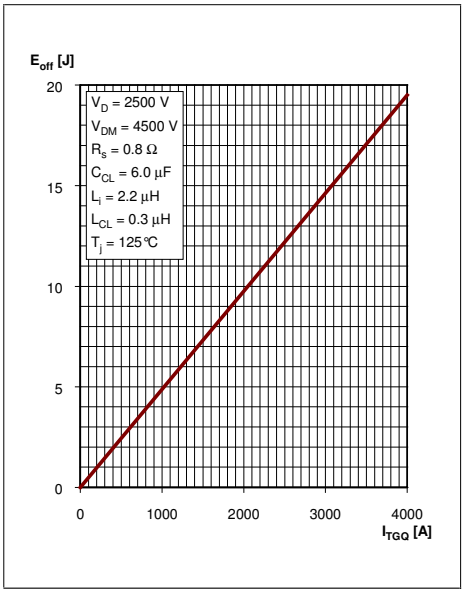


Fig. 5 GCT turn-off energy per pulse versus

pulse width.

turn-off current.

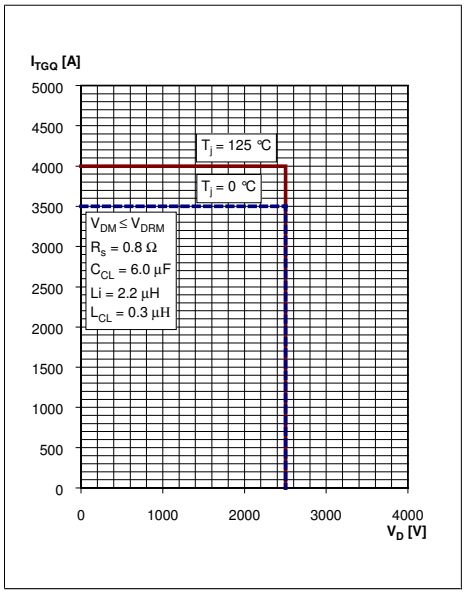


Fig. 6 Max. repetetive turn-off current versus turn-off voltage.

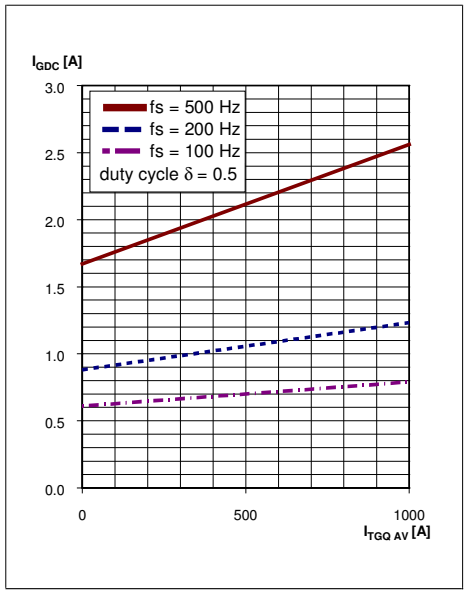


Fig. 7 Gate Unit Supply current.

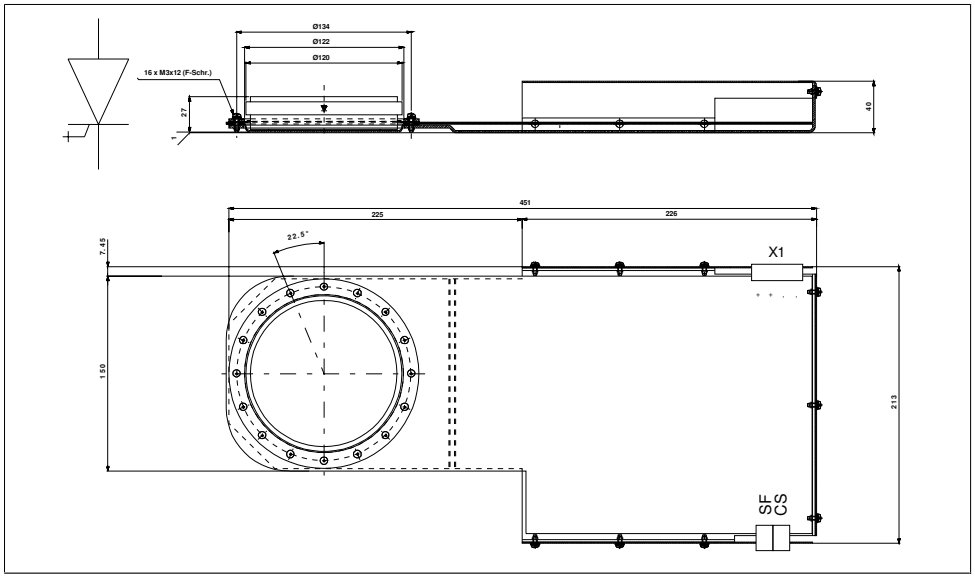


Fig. 8 Outline drawing. All dimensions are in millimeters and represent nominal values unless stated otherwise.

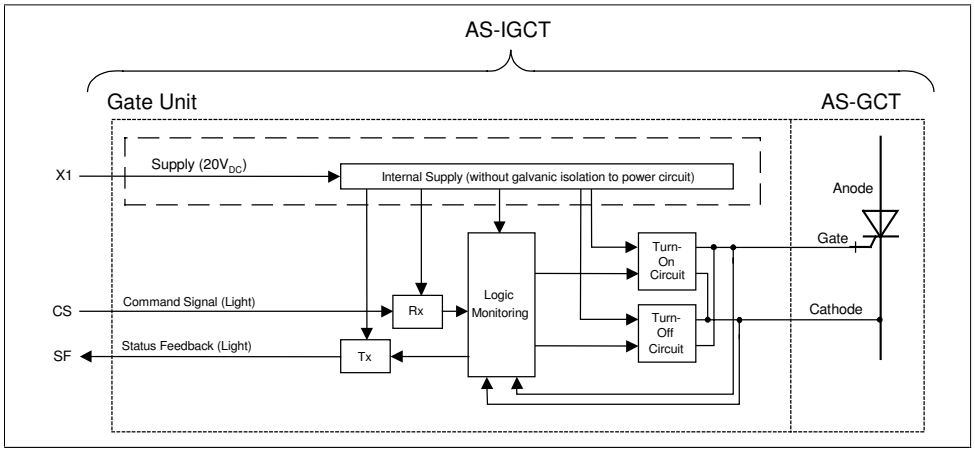


Fig. 9 Block diagram.

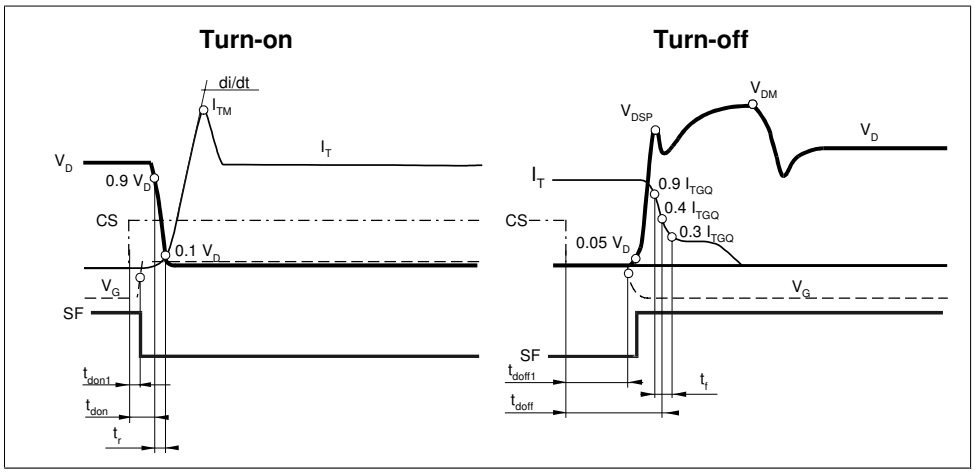


Fig. 10 General current and voltage waveforms with IGCT - specific symbols.

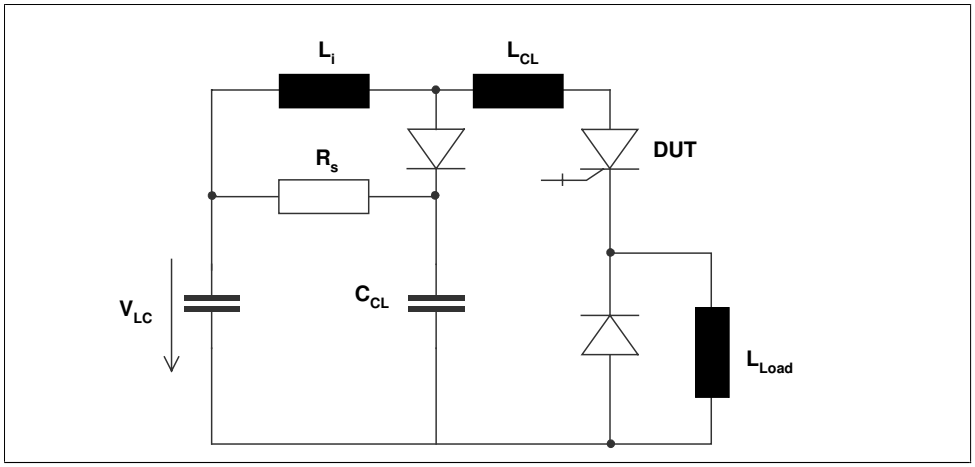


Fig. 11 Test circuit.

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# Appendix C

# Reverse recovery Measurement Results

**Device : IL226.10**

**Reverse Recovery Measurements at $T_{j,GCD}$ = 25℃**

**Table 1 : $Q_{Gate}$ function of $t_{pulse}$**

$T_{j,GCD}$ = 25℃, $V_{DC}$ = 2 kV

| $t_{pulse}$ (µs) | $Q_{Gate}$ (mAs) | | $Q_{Gate}$ (mAs) | |
|---|---|---|---|---|
| | $I_L$ = 500A | | $I_L$ = 1300A | |
| | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | |
| 1 | 0.065 | 0.074 | 0.138 | 0.143 |
| 2 | 0.250 | 0.278 | 0.331 | 0.371 |
| 5 | 0.805 | 0.926 | 0.913 | 1.047 |
| 10 | 1.758 | 2.189 | 1.845 | 2.226 |

**Table 2 : $Q_{rr}$ function of $t_{delay}$**

$T_{j,GCD}$ = 25℃, $V_{DC}$ = 2 kV

| | $Q_{rr}$(mAs) | | | $Q_{rr}$(mAs) | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | $I_L$ = 1300A | | |
| $t_{pulse}$ (µs) | $t_{delay}$ (µs) @ $I_L$ = 500A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$ = 1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 5 | -0.2 | 6.248 | 6.326 | -3.0 | 9.493 | 9.542 |
| 10 | | 6.986 | 7.187 | | 9.813 | 9.944 |
| | | | | | | |
| 5 | 0.8 | 6.366 | 6.442 | -2.0 | 9.561 | 9.627 |
| 10 | | 6.993 | 7.222 | | 9.903 | 10.187 |
| | | | | | | |
| 5 | 1.8 | 6.368 | 6.452 | -1.0 | 9.570 | 9.612 |
| 10 | | 7.000 | 7.315 | | 9.909 | 10.201 |
| | | | | | | |
| 5 | 2.8 | 6.369 | 6.479 | -0.1 | 9.572 | 9.584 |
| 10 | | 7.080 | 7.401 | | 10.035 | 10.233 |
| | | | | | | |
| 5 | 3.5 | 6.377 | 6.480 | 0.7 | 9.579 | 9.664 |
| 10 | | 7.167 | 7.412 | | 10.097 | 10.289 |
| | | | | | | |
| 5 | 4.0 | 6.382 | 6.506 | 1.4 | 9.600 | 9.809 |
| 10 | | 7.227 | 7.750 | | 11.368 | 10.350 |

**Table 3 : $Q_{rr}$ function of $I_{G,GCD}$**

$T_{j.GCD}$ = 25°C, $V_{DC}$ = 2 kV

| $t_{delay}$ (µs) | $t_{pulse}$ (µs) | $Q_{rr}$(mAs) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$=500A | | | | |
| | | $V_{GU_i/p}$ = 2,5V ($I_{G,GCD}$ = 100A) | $V_{GU,i/p}$ = 3,5V ($I_{G,GCD}$ = 120A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 5,5V ($I_{G,GCD}$ = 220A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 0.8 | 5 | 6.174 | 6.290 | 6.366 | 6.404 | 6.442 |
| | 10 | 6.490 | 6.791 | 6.993 | 7.161 | 7.222 |
| | | | | | | |
| 4.0 | 5 | 6.179 | 6.302 | 6.382 | 6.501 | 6.506 |
| | 10 | 6.664 | 6.978 | 7.227 | 7.481 | 7.750 |
| | | $I_L$=1300A | | | | |
| -2.0 | 5 | 9.403 | 9.481 | 9.493 | 9.516 | 9.542 |
| | 10 | 9.702 | 9.782 | 9.813 | 9.905 | 9.944 |
| | | | | | | |
| 1.4 | 5 | 9.510 | 9.544 | 9.600 | 9.786 | 9.809 |
| | 10 | 9.820 | 9.986 | 10.180 | 10.195 | 10.350 |

**Table 4 : $Q_{rr}$ function of $t_{pulse}$**

Tj = 25°C, $V_{DC}$ = 2 kV

| | | $Q_{rr}$ (mAs) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | | $I_L$ = 1300A | |
| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 0.8 | 1 | 6.091 | 6.127 | -2.0 | 9.366 | 9.386 |
| | 2 | 6.127 | 6.135 | | 9.391 | 9.456 |
| | 5 | 6.366 | 6.442 | | 9.561 | 9.627 |
| | 10 | 6.993 | 7.222 | | 9.903 | 10.182 |
| | | | | | | |
| 4.0 | 1 | 6.129 | 6.141 | 1.4 | 9.369 | 9.420 |
| | 2 | 6.187 | 6.299 | | 9.479 | 9.532 |
| | 5 | 6.382 | 6.506 | | 9.600 | 9.809 |
| | 10 | 7.227 | 7.750 | | 10.180 | 10.350 |

$Q_{rr}$ (mAs) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) = 5.905 mAs
$Q_{rr}$ (mAs) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 9.30mAs

**Table 5 : $W_{off,GCD}$ function of $t_{pulse}$**

**Tj = 25°C**

| | | $W_{off,GCD}$ (Ws) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | | $I_L$ = 1300A | |
| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | | | |
| 0.8 | 1 | 3.391 | 3.410 | -2.0 | 4.682 | 4.684 |
| | 2 | 3.486 | 3.524 | | 4.766 | 4.790 |
| | 5 | 3.973 | 4.080 | | 4.925 | 4.993 |
| | 10 | 5.255 | 5.748 | | 5.520 | 5.754 |
| | | | | | | |
| 4.0 | 1 | 3.426 | 3.428 | 1.4 | 4.727 | 4.757 |
| | 2 | 3.520 | 3.550 | | 4.873 | 4.891 |
| | 5 | 4.200 | 4.479 | | 5.168 | 5.271 |
| | 10 | 6.479 | 7.018 | | 6.160 | 6.379 |

**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) = 3.2 Ws**
**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 4.45 Ws**

## Device : IL226.10

**Reverse Recovery Measurements at $T_{j,GCD}$ = 85°C**

### Table 1 : $Q_{Gate}$ function of $t_{pulse}$

$T_{j,GCD}$ = 85°C

| $t_{pulse}$ (µs) | $Q_{Gate}$ (mAs) | | $Q_{Gate}$ (mAs) | |
|---|---|---|---|---|
| | $I_L$ = 500A | | $I_L$ = 1300A | |
| | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | |
| 1 | 0.065 | 0.074 | 0.138 | 0.143 |
| 2 | 0.250 | 0.278 | 0.331 | 0.371 |
| 5 | 0.805 | 0.926 | 0.913 | 1.047 |
| 10 | 1.758 | 2.189 | 1.845 | 2.226 |

### Table 2 : $Q_{rr}$ function of $t_{delay}$

$T_{j,GCD}$ = 85°C

| | $Q_{rr}$(mAs) | | | $Q_{rr}$(mAs) | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | $I_L$ = 1300A | | |
| $t_{pulse}$ (µs) | $t_{delay}$ (µs) @ $I_L$ = 500A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$ = 1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 5 | -0.2 | 6.994 | 7.088 | -3.0 | 10.271 | 10.289 |
| 10 | | 7.349 | 7.562 | | 10.686 | 10.730 |
| | | | | | | |
| 5 | 0.8 | 6.996 | 7.000 | -2.0 | 10.277 | 10.290 |
| 10 | | 7.493 | 7.740 | | 10.653 | 10.870 |
| | | | | | | |
| 5 | 1.8 | 6.991 | 7.022 | -1.0 | 10.324 | 10.320 |
| 10 | | 7.544 | 7.663 | | 10.859 | 10.935 |
| | | | | | | |
| 5 | 2.8 | 6.994 | 7.012 | -0.1 | 10.343 | 10.350 |
| 10 | | 7.541 | 7.729 | | 10.809 | 10.965 |
| | | | | | | |
| 5 | 3.5 | 6.996 | 7.000 | 0.7 | 10.433 | 10.444 |
| 10 | | 7.552 | 7.785 | | 10.953 | 11.130 |
| | | | | | | |
| 5 | 4.0 | 6.975 | 7.068 | 1.4 | 10.367 | 10.439 |
| 10 | | 7.679 | 7.905 | | 11.067 | 11.355 |

**Table 3 : $Q_{rr}$ function of $I_{G,GCD}$**

$T_{j.GCD}$ = 85°C

| $t_{delay}$ (µs) | $t_{pulse}$ (µs) | $Q_{rr}$(mAs) $I_L$=500A $V_{GU_i/p}$ = 2,5V ($I_{G,GCD}$ = 100A) | $V_{GU,i/p}$ = 3,5V ($I_{G,GCD}$ = 120A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 5,5V ($I_{G,GCD}$ = 220A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
|---|---|---|---|---|---|---|
| 0.8 | 5 | 6.910 | 6.950 | 6.977 | 6.988 | 7.000 |
| | 10 | 7.067 | 7.139 | 7.493 | 7.653 | 7.740 |
| | | | | | | |
| 4.0 | 5 | 6.927 | 6.974 | 6.996 | 6.997 | 7.068 |
| | 10 | 7.180 | 7.485 | 7.679 | 7.850 | 7.905 |
| | | $I_L$=1300A | | | | |
| -2.0 | 5 | 10.200 | 10.200 | 10.227 | 10.266 | 10.290 |
| | 10 | 10.497 | 10.594 | 10.653 | 10.789 | 10.870 |
| | | | | | | |
| 1.4 | 5 | 10.350 | 10.351 | 10.367 | 10.489 | 10.439 |
| | 10 | 10.530 | 10.693 | 11.067 | 11.084 | 11.355 |

**Table 4 : $Q_{rr}$ function of $t_{pulse}$**

Tj = 85°C $Q_{rr}$ (mAs)

| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $Q_{rr}$ (mAs) $I_L$ = 500A $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $I_L$ = 1300A $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
|---|---|---|---|---|---|---|
| 0.8 | 1 | 6.905 | 6.920 | -2.0 | 10.199 | 10.197 |
| | 2 | 6.910 | 6.935 | | 10.228 | 10.231 |
| | 5 | 6.996 | 7.000 | | 10.277 | 10.290 |
| | 10 | 7.493 | 7.740 | | 10.653 | 10.870 |
| | | | | | | |
| 4.0 | 1 | 6.920 | 6.980 | 1.4 | 10.199 | 10.234 |
| | 2 | 6.925 | 6.960 | | 10.198 | 10.230 |
| | 5 | 6.975 | 7.068 | | 10.367 | 10.439 |
| | 10 | 7.679 | 7.905 | | 11.067 | 11.355 |

$Q_{rr}$ (mAs) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) = 6.900 mAs
$Q_{rr}$ (mAs) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 10.196mAs

**Table 5 : $W_{off,GCD}$ function of $t_{pulse}$**

**Tj = 85°C**

| | | $W_{off,GCD}$ (Ws) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | | $I_L$ = 1300A | |
| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | | | |
| 0.8 | 1 | 4.541 | 4.637 | -2.0 | 6.034 | 6.041 |
| | 2 | 4.714 | 4.778 | | 6.057 | 6.058 |
| | 5 | 4.800 | 4.829 | | 6.208 | 6.244 |
| | 10 | 5.998 | 6.522 | | 6.885 | 6.997 |
| | | | | | | |
| 4.0 | 1 | 4.372 | 4.579 | 1.4 | 5.608 | 5.685 |
| | 2 | 4.434 | 4.602 | | 5.659 | 5.727 |
| | 5 | 4.842 | 5.136 | | 5.983 | 6.026 |
| | 10 | 7.036 | 7.525 | | 6.987 | 7.443 |

**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) = 4.52 Ws**
**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 6.03 Ws**

**Device : IL226.10**

**Reverse Recovery Measurements at $T_{j,GCD}$ = 115°C**

**Table 1 : $Q_{Gate}$ function of $t_{pulse}$**

$T_{j,GCD}$ = 115°C

| $t_{pulse}$ (µs) | $Q_{Gate}$ (mAs) | | $Q_{Gate}$ (mAs) | |
|---|---|---|---|---|
| | $I_L$ = 500A | | $I_L$ = 1300A | |
| | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | |
| 1 | 0.065 | 0.074 | 0.138 | 0.143 |
| 2 | 0.250 | 0.278 | 0.331 | 0.371 |
| 5 | 0.805 | 0.926 | 0.913 | 1.047 |
| 10 | 1.758 | 2.189 | 1.845 | 2.226 |

**Table 2 : $Q_{rr}$ function of $t_{delay}$**

$T_{j,GCD}$ = 115°C

| | $Q_{rr}$(mAs) | | | $Q_{rr}$(mAs) | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | | $I_L$ = 1300A | |
| $t_{pulse}$ (µs) | $t_{delay}$ (µs) @ $I_L$ = 500A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$ = 1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 5 | -0.2 | 7.006 | 7.043 | -3.0 | 10.672 | 10.684 |
| 10 | | 7.499 | 7.545 | | 11.078 | 11.163 |
| | | | | | | |
| 5 | 0.8 | 7.012 | 7.085 | -2.0 | 10.721 | 10.709 |
| 10 | | 7.506 | 7.572 | | 11.079 | 11.253 |
| | | | | | | |
| 5 | 1.8 | 7.028 | 7.115 | -1.0 | 10.730 | 10.720 |
| 10 | | 7.510 | 7.679 | | 11.178 | 11.326 |
| | | | | | | |
| 5 | 2.8 | 7.048 | 7.120 | -0.1 | 10.737 | 10.734 |
| 10 | | 7.517 | 7.727 | | 11.288 | 11.302 |
| | | | | | | |
| 5 | 3.5 | 7.071 | 7.109 | 0.7 | 10.747 | 10.922 |
| 10 | | 7.629 | 7.856 | | 11.301 | 11.403 |
| | | | | | | |
| 5 | 4.0 | 7.149 | 7.176 | 1.4 | 10.782 | 10.949 |
| 10 | | 7.711 | 7.921 | | 11.368 | 11.496 |

**Table 3 : $Q_{rr}$ function of $I_{G,GCD}$**

$T_{j.GCD}$ = 115°C

| $t_{delay}$ (µs) | $t_{pulse}$ (µs) | $Q_{rr}$(mAs) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$=500A | | | | |
| | | $V_{GU_i/p}$ = 2,5V ($I_{G,GCD}$ = 100A) | $V_{GU,i/p}$ = 3,5V ($I_{G,GCD}$ = 120A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 5,5V ($I_{G,GCD}$ = 220A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 0.8 | 5 | 6.979 | 7.002 | 7.012 | 7.072 | 7.115 |
| | 10 | 7.093 | 7.249 | 7.506 | 7.512 | 7.572 |
| | | | | | | |
| 4.0 | 5 | 6.994 | 7.048 | 7.149 | 7.162 | 7.186 |
| | 10 | 7.211 | 7.560 | 7.711 | 7.836 | 7.921 |
| | | $I_L$=1300A | | | | |
| -2.0 | 5 | 10.690 | 10.648 | 10.741 | 10.756 | 10.799 |
| | 10 | 10.808 | 10.910 | 11.179 | 11.199 | 11.253 |
| | | | | | | |
| 1.4 | 5 | 10.664 | 10.692 | 10.782 | 10.913 | 10.949 |
| | 10 | 10.829 | 11.000 | 11.268 | 11.321 | 11.496 |

**Table 4 : $Q_{rr}$ function of $t_{pulse}$**

Tj = 115°C  $Q_{rr}$ (mAs)

| | | $Q_{rr}$ (mAs) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | | $I_L$ = 1300A | |
| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 0.8 | 1 | 6.970 | 6.946 | -2.0 | 10.691 | 10.701 |
| | 2 | 6.973 | 6.960 | | 10.698 | 10.709 |
| | 5 | 7.012 | 7.115 | | 10.741 | 10.709 |
| | 10 | 7.506 | 7.572 | | 11.179 | 11.253 |
| | | | | | | |
| 4.0 | 1 | 6.995 | 6.992 | 1.4 | 10.658 | 10.655 |
| | 2 | 6.992 | 6.998 | | 10.713 | 10.730 |
| | 5 | 7.149 | 7.076 | | 10.782 | 10.949 |
| | 10 | 7.711 | 7.921 | | 11.268 | 11.496 |

$Q_{rr}$ (mAs) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) = 6.905 mAs
$Q_{rr}$ (mAs) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 10.670mAs

**Table 5 : $W_{off,GCD}$ function of $t_{pulse}$**

**Tj = 115°C**

| | | $W_{off,GCD}$ (Ws) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | | $I_L$ = 1300A | |
| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | | | |
| 0.8 | 1 | 4.640 | 4.686 | -2.0 | 5.571 | 5.532 |
| | 2 | 4.651 | 4.755 | | 5.642 | 5.668 |
| | 5 | 4.881 | 5.048 | | 5.781 | 5.812 |
| | 10 | 5.943 | 6.151 | | 6.316 | 6.584 |
| | | | | | | |
| 4.0 | 1 | 4.625 | 4.709 | 1.4 | 6.049 | 6.045 |
| | 2 | 4.864 | 4.709 | | 6.126 | 6.135 |
| | 5 | 5.261 | 5.152 | | 6.352 | 6.533 |
| | 10 | 7.014 | 7.508 | | 7.139 | 7.547 |

**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) = 4.62 Ws**
**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 6.03 Ws**

## Device : IL226.13

**Reverse Recovery Measurements at $T_{j,GCD}$ = 25°C**

**Table 1 : $Q_{Gate}$ function of $t_{pulse}$**

$T_{j,GCD}$ = 25°C

| $t_{pulse}$ (µs) | $Q_{Gate}$ (mAs) | | $Q_{Gate}$ (mAs) | |
|---|---|---|---|---|
| | $I_L$ = 500A | | $I_L$ = 1300A | |
| | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | |
| 1 | 0.065 | 0.074 | 0.138 | 0.143 |
| 2 | 0.250 | 0.278 | 0.331 | 0.371 |
| 5 | 0.805 | 0.926 | 0.913 | 1.047 |
| 10 | 1.758 | 2.189 | 1.845 | 2.226 |

**Table 2 : $Q_{rr}$ function of $t_{delay}$**

$T_{j,GCD}$ = 25°C

| | $Q_{rr}$(mAs) | | | $Q_{rr}$(mAs) | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | $I_L$ = 1300A | | |
| $t_{pulse}$ (µs) | $t_{delay}$ (µs) @ $I_L$ = 500A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$ = 1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 5 | -0.2 | # | # | # | # | # |
| 10 | | # | # | # | # | # |
| | | | | | | |
| 5 | 0.8 | 1.346 | 1.435 | -2.0 | 1.439 | 1.491 |
| 10 | | 1.800 | 2.070 | | 1.822 | 2.010 |
| | | | | | | |
| 5 | 1.8 | 1.374 | 1.474 | -1.0 | 1.479 | 1.600 |
| 10 | | 1.925 | 2.170 | | 1.972 | 2.027 |
| | | | | | | |
| 5 | 2.8 | 1.382 | 1.490 | -0.1 | 1.556 | 1.604 |
| 10 | | 2.004 | 2.218 | | 2.081 | 2.168 |
| | | | | | | |
| 5 | 3.5 | 1.399 | 1.540 | 0.7 | 1.584 | 1.688 |
| 10 | | 2.032 | 2.239 | | 2.089 | 2.261 |
| | | | | | | |
| 5 | 4.0 | 1.460 | 1.542 | 1.4 | 1.655 | 1.721 |
| 10 | | 2.085 | 2.298 | | 2.097 | 2.274 |

**Table 3 : $Q_{rr}$ function of $I_{G,GCD}$**

$T_{j.GCD}$ = 25°C

| $t_{delay}$ (µs) | $t_{pulse}$ (µs) | $Q_{rr}$(mAs) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$=500A | | | | |
| | | $V_{GU_i/p}$ = 2,5V ($I_{G,GCD}$ = 100A) | $V_{GU,i/p}$ = 3,5V ($I_{G,GCD}$ = 120A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 5,5V ($I_{G,GCD}$ = 220A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 0.8 | 5 | 1.180 | 1.327 | 1.416 | 1.443 | 1.435 |
| | 10 | 1.640 | 1.780 | 1.801 | 2.040 | 2.070 |
| | | | | | | |
| 4.0 | 5 | 1.270 | 1.450 | 1.460 | 1.531 | 1.539 |
| | 10 | 1.611 | 1.714 | 1.985 | 2.183 | 2.198 |
| $I_L$=1300A | | | | | | |
| -2.0 | 5 | 1.354 | 1.437 | 1.529 | 1.506 | 1.600 |
| | 10 | 1.690 | 1.815 | 1.822 | 2.047 | 2.049 |
| | | | | | | |
| 1.4 | 5 | 1.554 | 1.613 | 1.655 | 1.752 | 1.721 |
| | 10 | 1.805 | 1.852 | 2.097 | 2.195 | 2.274 |

**Table 4 : $Q_{rr}$ function of $t_{pulse}$**

Tj = 25°C $Q_{rr}$ (mAs)

| | | $Q_{rr}$ (mAs) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | | $I_L$ = 1300A | |
| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 0.8 | 1 | 0.970 | 1.020 | -2.0 | 1.220 | 1.400 |
| | 2 | 1.102 | 1.025 | | 1.236 | 1.485 |
| | 5 | 1.416 | 1.435 | | 1.529 | 1.600 |
| | 10 | 1.800 | 2.070 | | 1.822 | 2.041 |
| | | | | | | |
| 4.0 | 1 | 1.011 | 1.010 | 1.4 | 1.240 | 1.243 |
| | 2 | 1.010 | 1.059 | | 1.378 | 1.387 |
| | 5 | 1.466 | 1.539 | | 1.655 | 1.721 |
| | 10 | 1.985 | 2.198 | | 2.097 | 2.274 |

$Q_{rr}$ (mAs) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) = 0.850 mAs
$Q_{rr}$ (mAs) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 1.21 mAs

**Table 5 : $W_{off,GCD}$ function of $t_{pulse}$**

**Tj = 25°C**

| | | $W_{off,GCD}$ (Ws) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | | $I_L$ = 1300A | |
| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | | | |
| 0.8 | 1 | 1.204 | 1.350 | -2.0 | 1.100 | 1.214 |
| | 2 | 1.850 | 1.962 | | 1.662 | 1.687 |
| | 5 | 2.015 | 2.179 | | 1.851 | 1.733 |
| | 10 | 3.009 | 3.079 | | 2.312 | 2.639 |
| | | | | | | |
| 4.0 | 1 | 1.264 | 1.432 | 1.4 | 1.228 | 1.327 |
| | 2 | 1.887 | 2.253 | | 1.874 | 1.921 |
| | 5 | 2.190 | 2.408 | | 1.933 | 2.159 |
| | 10 | 3.389 | 3.780 | | 2.790 | 3.091 |

**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) = 0.88 Ws**
**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 1.1 Ws**

## Device : IL226.13

**Reverse Recovery Measurements at $T_{j,GCD}$ = 85°C**

### Table 1 : $Q_{Gate}$ function of $t_{pulse}$

$T_{j,GCD}$ = 85°C

| $t_{pulse}$ (µs) | $Q_{Gate}$ (mAs) | | $Q_{Gate}$ (mAs) | |
|---|---|---|---|---|
| | $I_L$ = 500A | | $I_L$ = 1300A | |
| | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | |
| 1 | 0.065 | 0.074 | 0.138 | 0.143 |
| 2 | 0.250 | 0.278 | 0.331 | 0.371 |
| 5 | 0.805 | 0.926 | 0.913 | 1.047 |
| 10 | 1.758 | 2.189 | 1.845 | 2.226 |

### Table 2 : $Q_{rr}$ function of $t_{delay}$

$T_{j,GCD}$ = 85°C

| | $Q_{rr}$(mAs) | | | $Q_{rr}$(mAs) | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | $I_L$ = 1300A | | |
| $t_{pulse}$ (µs) | $t_{delay}$ (µs) @ $I_L$ = 500A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$ = 1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 5 | -0.2 | # | # | -3.0 | # | # |
| 10 | | # | # | | # | # |
| | | | | | | |
| 5 | 0.8 | 1.628 | 1.787 | -2.0 | 1.898 | 2.019 |
| 10 | | 2.160 | 2.412 | | 2.484 | 2.588 |
| | | | | | | |
| 5 | 1.8 | 1.686 | 1.798 | -1.0 | 1.965 | 2.023 |
| 10 | | 2.305 | 2.506 | | 2.528 | 2.612 |
| | | | | | | |
| 5 | 2.8 | 1.799 | 1.824 | -0.1 | 2.083 | 2.166 |
| 10 | | 2.338 | 2.535 | | 2.567 | 2.615 |
| | | | | | | |
| 5 | 3.5 | 1.799 | 1.852 | 0.7 | 2.085 | 2.187 |
| 10 | | 2.479 | 2.551 | | 2.580 | 2.664 |
| | | | | | | |
| 5 | 4.0 | 1.800 | 2.075 | 1.4 | 2.085 | 2.198 |
| 10 | | 2.482 | 2.561 | | 2.693 | 2.712 |

**Table 3 : $Q_{rr}$ function of $I_{G,GCD}$**

$T_{j.GCD}$ = 85°C

| $t_{delay}$ (µs) | $t_{pulse}$ (µs) | $Q_{rr}$(mAs) $I_L$=500A $V_{GU_i/p}$ = 2,5V ($I_{G,GCD}$ = 100A) | $V_{GU,i/p}$ = 3,5V ($I_{G,GCD}$ = 120A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 5,5V ($I_{G,GCD}$ = 220A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
|---|---|---|---|---|---|---|
| 0.8 | 5 | 1.500 | 1.580 | 1.628 | 1.758 | 1.787 |
| | 10 | 1.885 | 2.049 | 2.160 | 2.362 | 2.412 |
| | | | | | | |
| 4.0 | 5 | 1.562 | 1.657 | 1.790 | 1.824 | 2.019 |
| | 10 | 1.960 | 2.170 | 2.382 | 2.484 | 2.588 |
| $I_L$=1300A | | | | | | |
| -2.0 | 5 | 1.769 | 1.884 | 1.998 | 2.004 | 2.075 |
| | 10 | 2.095 | 2.260 | 2.484 | 2.493 | 2.501 |
| | | | | | | |
| 1.4 | 5 | 1.945 | 2.007 | 2.048 | 2.151 | 2.198 |
| | 10 | 2.244 | 2.351 | 2.693 | 2.700 | 2.712 |

**Table 4 : $Q_{rr}$ function of $t_{pulse}$**

Tj = 85°C $Q_{rr}$ (mAs)

| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $Q_{rr}$ (mAs) $I_L$ = 500A $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $I_L$ = 1300A $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
|---|---|---|---|---|---|---|
| 0.8 | 1 | 1.292 | 1.311 | -2.0 | 1.741 | 1.752 |
| | 2 | 1.382 | 1.401 | | 1.779 | 1.788 |
| | 5 | 1.628 | 1.787 | | 1.898 | 2.019 |
| | 10 | 2.160 | 2.412 | | 2.488 | 2.588 |
| | | | | | | |
| 4.0 | 1 | 1.328 | 1.359 | 1.4 | 1.743 | 1.749 |
| | 2 | 1.395 | 1.445 | | 1.775 | 1.807 |
| | 5 | 1.799 | 2.075 | | 2.085 | 2.198 |
| | 10 | 2.482 | 2.501 | | 2.693 | 2.712 |

$Q_{rr}$ (mAs) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) = 1.272 mAs
$Q_{rr}$ (mAs) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 1.733 mAs

**Table 5 : $W_{off,GCD}$ function of $t_{pulse}$**

**Tj = 85°C**

| | | $W_{off,GCD}$ (Ws) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | | $I_L$ = 1300A | |
| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | | | |
| 0.8 | 1 | 1.241 | 1.387 | -2.0 | 1.244 | 1.392 |
| | 2 | 1.936 | 2.171 | | 1.987 | 2.200 |
| | 5 | 2.199 | 2.259 | | 2.196 | 2.310 |
| | 10 | 3.348 | 3.712 | | 2.951 | 3.052 |
| | | | | | | |
| 4.0 | 1 | 1.288 | 1.335 | 1.4 | 1.451 | 1.563 |
| | 2 | 2.128 | 2.352 | | 2.226 | 2.412 |
| | 5 | 2.587 | 2.725 | | 2.335 | 2.502 |
| | 10 | 3.993 | 4.043 | | 3.135 | 3.998 |

**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) = 0.975 Ws**
**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 1.1 Ws**

**Device : IL226.13**

**Reverse Recovery Measurements at $T_{j,GCD}$ = 115°C**

**Table 1 : $Q_{Gate}$ function of $t_{pulse}$**

$T_{j,GCD}$ = 115°C

| $t_{pulse}$ (µs) | $Q_{Gate}$ (mAs) | | $Q_{Gate}$ (mAs) | |
|---|---|---|---|---|
| | $I_L$ = 500A | | $I_L$ = 1300A | |
| | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | |
| 1 | 0.065 | 0.074 | 0.138 | 0.143 |
| 2 | 0.250 | 0.278 | 0.331 | 0.371 |
| 5 | 0.805 | 0.926 | 0.913 | 1.047 |
| 10 | 1.758 | 2.189 | 1.845 | 2.226 |

**Table 2 : $Q_{rr}$ function of $t_{delay}$**

$T_{j,GCD}$ = 115°C

| | $Q_{rr}$(mAs) | | | $Q_{rr}$(mAs) | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | $I_L$ = 1300A | | |
| $t_{pulse}$ (µs) | $t_{delay}$ (µs) @ $I_L$ = 500A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$ = 1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 5 | -0.2 | | | -3.0 | | |
| 10 | | | | | | |
| | | | | | | |
| 5 | 0.8 | 1.848 | 1.880 | -2.0 | 2.238 | 2.285 |
| 10 | | 2.303 | 2.507 | | 2.668 | 2.735 |
| | | | | | | |
| 5 | 1.8 | 1.875 | 1.928 | -1.0 | 2.338 | 2.422 |
| 10 | | 2.381 | 2.617 | | 2.674 | 2.782 |
| | | | | | | |
| 5 | 2.8 | 1.968 | 2.131 | -0.1 | 2.369 | 2.467 |
| 10 | | 2.525 | 2.589 | | 2.750 | 2.786 |
| | | | | | | |
| 5 | 3.5 | 1.982 | 2.182 | 0.7 | 2.387 | 2.531 |
| 10 | | 2.533 | 2.645 | | 2.756 | 2.827 |
| | | | | | | |
| 5 | 4.0 | 2.126 | 2.245 | 1.4 | 2.391 | 2.583 |
| 10 | | 2.626 | 2.714 | | 2.865 | 2.986 |

**Table 3 : $Q_{rr}$ function of $I_{G,GCD}$**

$T_{j.GCD}$ = 115°C

| $t_{delay}$ (µs) | $t_{pulse}$ (µs) | $Q_{rr}$(mAs) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$=500A | | | | |
| | | $V_{GU_i/p}$ = 2,5V ($I_{G,GCD}$ = 100A) | $V_{GU,i/p}$ = 3,5V ($I_{G,GCD}$ = 120A) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 5,5V ($I_{G,GCD}$ = 220A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 0.8 | 5 | 1.636 | 1.761 | 1.848 | 1.866 | 1.880 |
| | 10 | 2.008 | 2.116 | 2.303 | 2.465 | 2.507 |
| | | | | | | |
| 4.0 | 5 | 1.816 | 1.958 | 2.126 | 2.195 | 2.245 |
| | 10 | 2.160 | 2.264 | 2.626 | 2.669 | 2.714 |
| | $I_L$=1300A | | | | | |
| -2.0 | 5 | 2.099 | 2.103 | 2.228 | 2.274 | 2.285 |
| | 10 | 2.299 | 2.518 | 2.668 | 2.720 | 2.735 |
| | | | | | | |
| 1.4 | 5 | 2.281 | 2.347 | 2.397 | 2.400 | 2.583 |
| | 10 | 2.463 | 2.592 | 2.865 | 2.874 | 2.986 |

**Table 4 : $Q_{rr}$ function of $t_{pulse}$**

Tj = 115°C  $Q_{rr}$ (mAs)

| | | $Q_{rr}$ (mAs) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | | $I_L$ = 1300A | |
| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| 0.8 | 1 | 1.501 | 1.510 | -2.0 | 1.945 | 1.949 |
| | 2 | 1.514 | 1.520 | | 1.962 | 1.991 |
| | 5 | 1.848 | 1.880 | | 2.228 | 2.285 |
| | 10 | 2.303 | 2.507 | | 2.668 | 2.735 |
| | | | | | | |
| 4.0 | 1 | 1.501 | 1.511 | 1.4 | 1.955 | 1.958 |
| | 2 | 1.520 | 1.525 | | 2.123 | 2.040 |
| | 5 | 2.126 | 2.245 | | 2.341 | 2.383 |
| | 10 | 2.626 | 2.714 | | 2.865 | 2.986 |

$Q_{rr}$ (mAs) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) = 1.455 mAs
$Q_{rr}$ (mAs) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 1.86 mAs

**Table 5 : $W_{off,GCD}$ function of $t_{pulse}$**

**Tj = 115°C**

| | | $W_{off,GCD}$ (Ws) | | | | |
|---|---|---|---|---|---|---|
| | | $I_L$ = 500A | | | $I_L$ = 1300A | |
| $t_{delay}$ (µs) @ $I_L$=500A | $t_{pulse}$ (µs) | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) | $t_{delay}$ (µs) @ $I_L$=1300A | $V_{GU,i/p}$ = 5V ($I_{G,GCD}$ = 200A) | $V_{GU,i/p}$ = 6V ($I_{G,GCD}$ = 300A) |
| | | | | | | |
| 0.8 | 1 | 2.226 | 2.584 | -2.0 | 2.421 | 2.884 |
| | 2 | 2.653 | 2.888 | | 4.174 | 4.519 |
| | 5 | 4.881 | 5.048 | | 5.781 | 5.812 |
| | 10 | 5.943 | 6.151 | | 6.316 | 6.584 |
| | | | | | | |
| 4.0 | 1 | 3.111 | 3.560 | 1.4 | 3.770 | 3.870 |
| | 2 | 4.000 | 4.389 | | 4.759 | 5.200 |
| | 5 | 5.261 | 5.152 | | 6.352 | 6.533 |
| | 10 | 7.014 | 7.508 | | 7.139 | 7.547 |

**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 500A with $I_{G.GCD}$ = 0A ) =2 Ws**
**$W_{off,GCD}$ (Ws) ( @ $I_L$ = 1300A with $I_{G.GCD}$ = 0A ) = 2.23 Ws**