# RF-MEMS Switch Module
# in a 0.25 µm SiGe:C BiCMOS Process

vorgelegt von
M.Sc.
Mehmet Kaynak
aus Antalya

von der Fakultät IV - Elektrotechnik und Informatik
der Technischen Universität Berlin
zur Erlangung des akademischen Grades

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| Vorsitzender: | Prof. Dr.-Ing. | Roland Thewes |
| Berichter: | Prof. Dr.rer.nat. | Bernd Tillack |
| Berichter: | Prof. Dr.-Ing. | Hermann Schumacher |
| Berichter: | Prof. Dr. | Thomas Otto |

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*I lovingly dedicate this thesis to my beloved wife, Canan,*
*who supported me each step of the way.*

# Abstract

Wireless communication technologies have continuously advanced for both performance and frequency aspects, mainly for the frequencies up to 6 GHz. The results of Moore's law now also give the opportunity to design mm-wave circuits using advanced CMOS technologies. The introduction of SiGe into CMOS, providing high performance BiCMOS, has also enhanced both the frequency and the power performance figures. The current situation is that the active devices of both CMOS and BiCMOS technologies can provide performance figures competitive with III-V technologies while having still the advantage of low cost. However, similar competition cannot be pronounced for the passive components considering the low-resistive substrates of BiCMOS technologies. Moreover, both III-V and BiCMOS technologies have the lack of low-loss and low-power consumption, as well as highly linear switching and tuning components at mm-wave frequencies.

RF-MEMS switch technologies have been well-known with excellent RF-performance figures. The power consumption of electrostatic RF-MEMS switches is negligible and they can handle higher power levels compared to their semiconductor counterparts. However, RF-MEMS switches have been mostly demonstrated as standalone processes and have started to be used as commercial off-the-shelf (COTS) devices recently. The full system integration is typically done by a System-in-Package (SiP) approach. Although SiP is suitable for lower frequencies, the packaging parasitics limit the use of this approach for the mm-wave frequencies.

In this thesis, a fully BiCMOS embedded RF-MEMS switch for mm-wave applications is proposed. The design, the implementation and the experimental results of the switch are provided. The developed RF-MEMS switch is packaged using different packaging approaches. To actuate the RF-MEMS switch, an on-chip high voltage generation circuit is designed and characterized. The robustness and the reliability performance of the switch are also presented. Finally, the developed RF-MEMS switch is successfully demonstrated in re-configurable mm-wave circuits.

# Zusammenfassung

Drahtlose Kommunikationstechnologien im Frequenzbereich bis 6 GHz wurden in der Vergangenheit in Bezug auf Leistungsfaehigkeit und Frequenzbereich kontinuierlich verbessert. Aufgrund der Skalierung nach dem Mooreschen Gesetz koennen heutzutage mm-Wellen Schaltkreise in CMOS-Technologien hergestellt werden. Durch die Einfuehrung von SiGe zur Realisierung einer leistungsfaehigen BiCMOS-Technologie wurde ebenfalls eine Verbesserung der Frequenzeigenschaften und Ausgangsleistungen erreicht, wodurch aktive CMOS- oder BiCMOS-Bauelemente vergleichbare Leistungsparameter zu III-V Technologien bei geringeren Kosten bereitstellen koennen. Bedingt durch das niederohmige Silizium-Substrat der BiCMOS-Technologie weisen vor allem passive Komponenten hoehere Verluste auf und weder III-V- noch BiCMOS-Technologien bieten hochlineare Schaltkomponenten mit geringen Verlusten und geringen Leistungsaufnahmen im mm-Wellen Bereich.

RF-MEMS Schalter sind bekannt fuer ihre ausgezeichneten HF-Eigenschaften. Die Leistungsaufnahme von elektrostatisch angetriebenen RF-MEMS Schaltern ist vernachlaessigbar und es koennen im Vergleich zu halbleiter-basierten Schaltern hoehere Leistungen verarbeitet werden. Nichtsdestotrotz wurden RF-MEMS Schalter hauptsaechlich als eigenstaendige Komponenten entwickelt. Zur Systemintegration wird meist ein System-in-Package (SiP) Ansatz angewandt, der fuer niedrige Frequenzen geeignet ist, aber bei mm-Wellenanwendungen durch parasitaere Verluste an seine Grenzen stoesst.

In dieser Arbeit wird ein in eine BiCMOS-Technologie integrierter RF-MEMS Schalter fuer mm-Wellen Anwendungen gezeigt. Das Design, die Integration und die experimentellen Ergebnisse sowie verschiedene Packaging-Konzepte werden beschrieben  Zur Bereitstellung der hohen Auslenkungs-Spannungen wurde eine Ladungspumpe auf dem Chip integriert. Zum Schluss werden verschiedene, rekonfigurierbare mm-Wellen Schaltkreise zur Demonstration der Leistungsfaehigkeit des Schalters gezeigt.

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My gratitude goes to my colleague, Matthias Wietstruck, for his boundless support of RF-MEMS in IHP. His contribution to this thesis is much appreciated. I have had the pleasure to work with my very experienced colleagues Karl-Ernst Ehwald and Dieter Knoll and would like to thank them for very fruitful technical discussions. Special thanks go to Christine Richter who supports me for everything and shows me the friendly environment of IHP. I would also like to acknowledge my colleagues J. Drews, F. Koerndorfer, K. Schulz and Dr. R. Scholz for their support. Starting from the colleagues in RF-MEMS group of IHP, I appreciate the excellent support from Process Integration, Process Research, Clean Room and Electrical Characterization groups, as well as all the other colleagues in IHP. I would also like to thank my former colleagues from Sabanci University, Prof. Ibrahim Tekin and Prof. Yasar Gurbuz for their very valuable support.

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*Mehmet Kaynak*
*September, 2013*

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# 1 Introduction

Chapter 1 starts with a general overview of the main motivation and the goal of the thesis. The latest developments and the state-of-the art of SiGe BiCMOS and RF-MEMS technologies are presented in sections 1.2 and 1.3, respectively. Chapter 1 is concluded with the organization of the thesis in section 1.4.

## 1.1 Motivation and Objective

During the past years, the rapid growth of the wireless communication market up to frequencies of 100 GHz and beyond has been the main driver for the development of multi-band RF front-end systems. However, RF communication and sensing systems are facing the demands of increased complexity, number of frequency bands and standards, as well as increased bandwidths and higher frequencies. The current solution of using multiple RF front-ends for different frequency bands may no longer be cost effective for the increasing number of bands. Especially when considering the increased demands on size and cost reduction, re-configurable or tunable systems are perhaps the only viable solution with respect to achieving further miniaturization and complex functionality. For such re-configurable systems, low loss, low power and highly linear switching/tuning components for building integrated adaptive RF circuits and front-ends are highly required. Nowadays, switches can be realized using different solid-state technologies, namely ferrite technologies and PIN diodes [1]. The former provide the lowest RF insertion losses but the devices are bulky and not cost effective. On the other hand, the latter provide low cost fabrication, but the insertion losses are relatively high and they consume significant power, thus are not suitable for low power or highly dense array applications.

RF-MEMS technologies are well known for their excellent RF properties, very low power consumption, wide bandwidths and IC compatibility [2]. Therefore, they are ideal components for realization of re-configurable RF circuits and systems. In addition, they are also considered as the key components to fulfill the beam steering and phase array antenna requirements of mm-wave applications [2, 3], such as imaging and sensor applications at 94, 120 and 140 GHz [4, 5]. For such high frequency

applications, a monolithic, embedded integration of the switch into a high-performance CMOS or BiCMOS platform would be advantageous over any heterogeneous integration with the basic IC process because it provides the shortest connection paths between the switch and the circuitry resulting in the lowest parasitics.

In this thesis, the main motivation is the need of the market for a high performance switching component at mm-wave frequencies. The objectives of the thesis can be summarized as follows:

- Integration of a high performance mm-wave packaged RF-MEMS switch technology into a SiGe BiCMOS process with minimum number of additional process steps and effort.
- No violation of qualified process specifications due to the additional or modified process steps of the RF-MEMS switch module.
- Electromechanical and electromagnetic (EM) optimization of the mm-wave RF-MEMS switch in order to achieve performance figures beyond state-of-the-art.
- Development of a low-loss, high throughput packaging process for the RF-MEMS switches without changing any specifications of the BiCMOS process.
- Study of the robustness and the reliability of the developed RF-MEMS switch.
- Use of the developed RF-MEMS switches in passive and active circuits.

## 1.2 SiGe BiCMOS Technologies for mm-wave ICs

Monolithic microwave integrated circuits (MMICs) have been dominated by III-V semiconductor technologies for a long time. While III-V semiconductor components continue to lead the way in terms of noise figure (NF) and maximum output power performances, an increasing number of Silicon based circuits appear in laboratories as well as in the marketplace. The introduction of the Silicon-Germanium (SiGe) Heterojunction-Bipolar-Transistor (HBT) in the late eighties was a major step. Since the BiCMOS processes can be achieved by adding only the bipolar part as a module to baseline CMOS, therefore it does not need a complete technology development. The true advantage of SiGe is the combination of SiGe HBT and CMOS, i.e. the SiGe HBT for analog/RF and ultrafast digital, CMOS for ultra-dense circuitry, memory, and certain analog primitives.

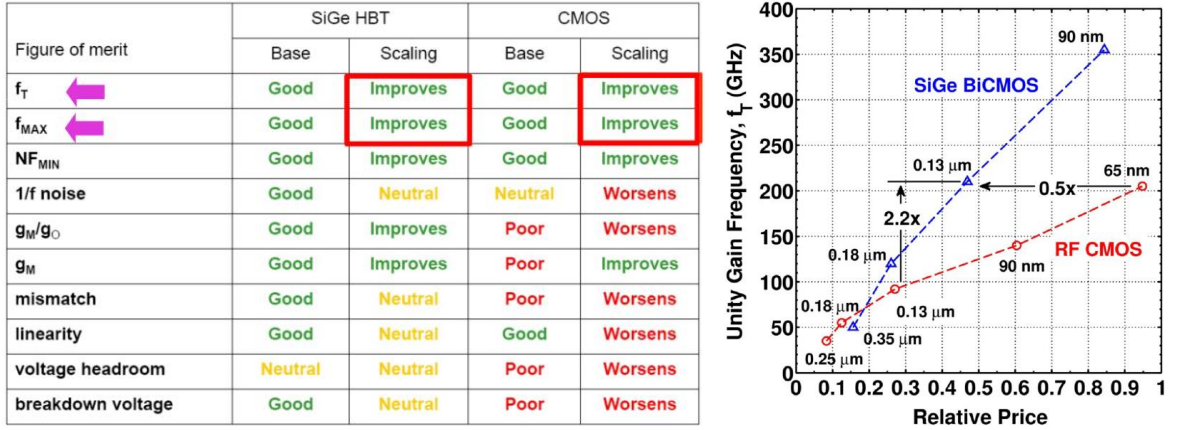| Figure of merit | SiGe HBT | | CMOS | |
|---|---|---|---|---|
| | Base | Scaling | Base | Scaling |
| $f_T$ | Good | Improves | Good | Improves |
| $f_{MAX}$ | Good | Improves | Good | Improves |
| $NF_{MIN}$ | Good | Improves | Good | Improves |
| 1/f noise | Good | Neutral | Neutral | Worsens |
| $g_M/g_O$ | Good | Improves | Poor | Worsens |
| $g_M$ | Good | Improves | Poor | Improves |
| mismatch | Good | Neutral | Poor | Worsens |
| linearity | Good | Neutral | Good | Worsens |
| voltage headroom | Neutral | Neutral | Poor | Worsens |
| breakdown voltage | Good | Neutral | Poor | Worsens |

Figure 1.1 The comparison of SiGe BiCMOS and CMOS processes for different performance figures (left). The relative cost comparison is also given for different technology nodes (right) [6].

Nowadays, $f_{max}$ values of 300 GHz are commercially available, and HBTs with 500 GHz $f_{max}$ are also provided as an early access [7]. Similar performance parameters can also be achieved by pure CMOS processes with 3 to 4 times smaller technology nodes; however, the cost of the process increases drastically. Furthermore, beyond the 90 nm technology node, the breakdown voltages rapidly decrease and the mask cost and gate leakage currents strongly increase. These limitations make BiCMOS still a powerful competitor to RFCMOS, especially for small to medium scale markets. Figure 1.1 summarizes the comparison between SiGe BiCMOS and pure CMOS technologies for base and scaling cases [6].

Despite the fact that there is an endless technology node improvement of pure CMOS technologies, SiGe BiCMOS technologies always find a market place due to their excellent performance parameters, such as high power handling and low noise figure. Automotive radar application at 77 GHz is now the most important market for SiGe and taking the market load from III-V technologies. Any mm-wave application over 60 GHz is also a potential market for SiGe since operation frequencies up to 600 GHz have already been demonstrated [8, 9]. However, the advantage of the higher level of integration of SiGe comes with a drawback of thermal issues since SiGe provides significant power in very small transistor footprint. The new phased array applications need several transceiver cores on a single chip; thus making the thermal management very challenging [10]. For those applications, SiGe technologies with higher $f_{max}$ can provide significant benefit because the same performance can be achieved with much less power consumption which makes the thermal management easier. Figure 1.2 shows

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the state-of-the-art SiGe technologies from different foundries [11]. 500 GHz $f_{max}$ has been achieved by IHP in the DOTFIVE project [12, 13] and the research is still on-going in the DOTSEVEN project which has a target $f_{max}$ of 700 GHz [14].
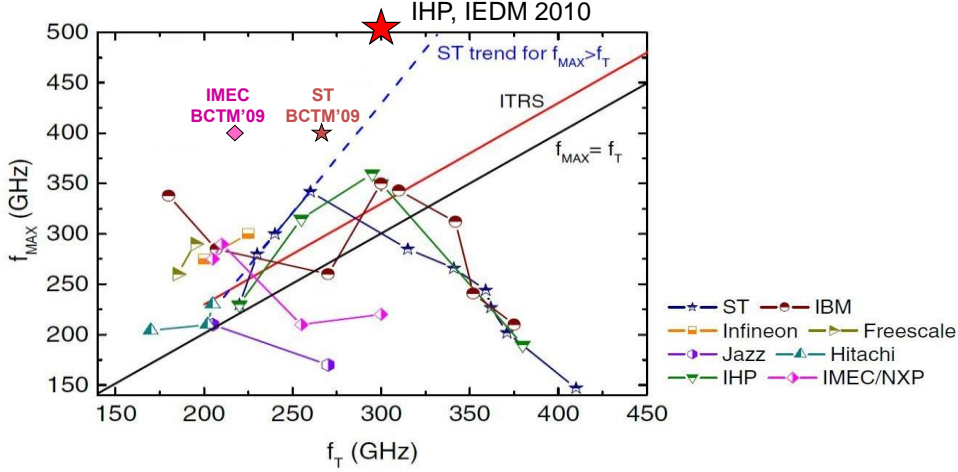


Figure 1.2 The performance comparison of the state-of-the-art SiGe BiCMOS technologies provided by different foundries [11].

Increase of $f_{max}$ has opened another potential market for SiGe BiCMOS technologies, namely the passive and active imaging systems at 94 and 140 GHz [15, 16, 17, 18]. The passive imaging systems at 94 GHz are mainly realized using InP and GaAs based technologies due to their excellent noise figure parameters. Passive imaging systems need very low noise amplifiers and noise figures of 2.5 to 3 dB can easily be achieved using these III-V technologies at these frequencies, with a drawback of high cost. However, the cost intensive III-V technologies are not the best candidates for multi-element imaging systems. The increase of $f_{max}$ values of SiGe HBTs also decreases the minimum noise figure and allows designing amplifiers with lower noise figures. The latest results show that LNAs at around 110 GHz with a noise figure of 4 dB can be achieved using a SiGe BiCMOS technology with an $f_{max}$ of 500 GHz [19]. Considering the additional analog/digital circuitry that can be integrated together with the LNA in BiCMOS and the potential increase of the number of elements in the system due to the lower cost per chip, SiGe technology is very promising for imaging applications at 94 and 140 GHz and can be a replacement of cost intensive III-V technologies in the near future.

As a conclusion, SiGe BiCMOS technologies are still very promising for many applications from radar to imaging systems as well as sensor applications at mm-wave frequencies. The active devices can provide very competitive performance against III-V technologies; however, this is not the case for the passive part. The low-resistive Silicon limits the quality factor of the transmission lines and inductors. Moreover, there is no real switching component in both CMOS and BiCMOS processes, especially beyond 60 GHz. Therefore, any additional module to BiCMOS which enhances the performance of the passive components or provides a switching component, can significantly improve the overall circuit and system performance. This would make the BiCMOS process more competitive against III-V or high-end CMOS technologies.

## 1.3 RF-MEMS Switch Technologies

- *Types of Electrostatically Actuated RF-MEMS Switches*

RF-MEMS switches can be summarized under two main categories considering the type of the contact; namely capacitive (Figure 1.3, left) and resistive (Figure 1.3, right).
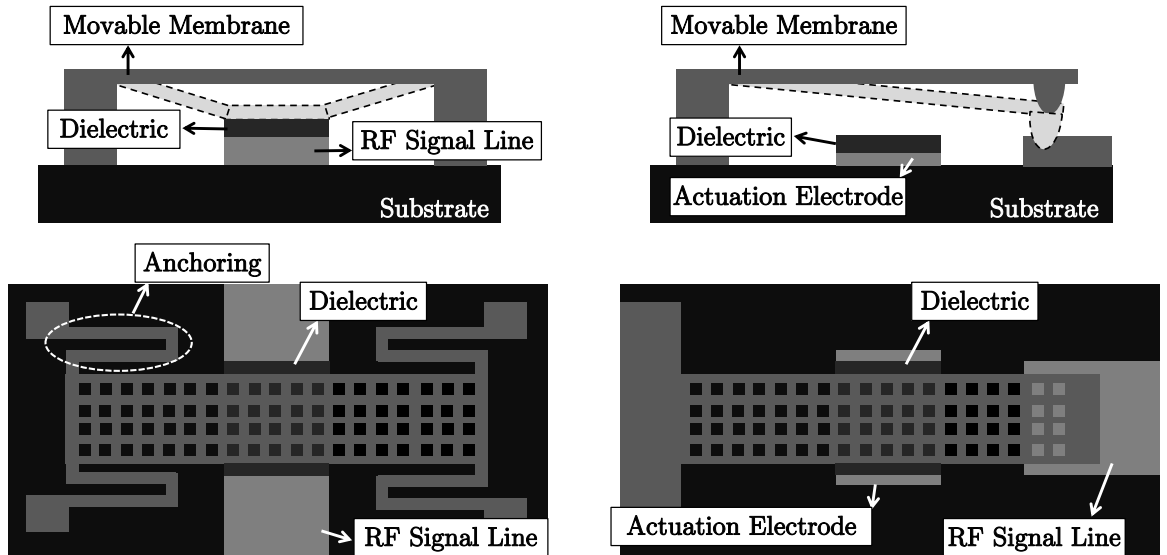


Figure 1.3 Capacitive (left) and resistive (right) types of RF-MEMS switches.

In capacitive contact type of RF-MEMS switches, the RF signal is switched on and off by the help of low and high capacitance at the contact region. In up-state, the switch provides low capacitance which behaves like an open circuit for RF signal. However, in down state, the contact capacitance is high and it provides a series LC resonance, together with the movable membrane inductance. The most common actuation principle for the capacitive type of RF-MEMS switches is performed by applying a high voltage difference between the RF signal line and the movable membrane (Figure 1.3, left). The dielectric on top of the RF signal line is used in order to isolate the DC values of RF signal line and the movable membrane, as well as to achieve high capacitance at down-state. The typical circuit configuration to use the capacitive type of RF-MEMS switches is the shunt configuration; however, it can also be used in a series configuration.

The second type of RF-MEMS switch is the resistive type RF-MEMS switches (Figure 1.3, right). In resistive type RF-MEMS switches, the RF signal is switched on and off by having a low and high ohmic contacts. In up-state, the switch provides an open circuit between the movable membrane and the RF signal line. However, in down-state, the contact resistance is very low; thus the movable membrane and the RF signal line is shorted. The most common actuation principle for resistive type of RF-MEMS switches is the separated high voltage electrode, as given in Figure 1.3, right. The typical circuit configuration to use the resistive type RF-MEMS switch is the series configuration; however, it can also be used in a shunt configuration.

In general, the performance of the resistive type RF-MEMS switches is limited by the contact resistance, which is more significant at higher frequencies. On the other side, the down-state capacitance of the capacitive type RF-MEMS switches is the main limitation factor because in order to provide better short circuit at lower frequencies, higher capacitance values have to be achieved. Considering these facts, it can be concluded that the capacitive type RF-MEMS switches are more suitable for high frequency applications (i.e. > 40 GHz) while the resistive ones are more convenient at lower frequencies. Therefore, in this thesis capacitive type of RF-MEMS switch is chosen since the expected operating frequencies are at mm-waves frequencies.

The main challenge of capacitive type RF-MEMS switches is the charging of the dielectric at the contact region. In most common approach, the high voltage is applied between the RF signal line and the movable membrane. The dielectric is charged under the applied high electric field and it causes stiction (Figure 1.4).
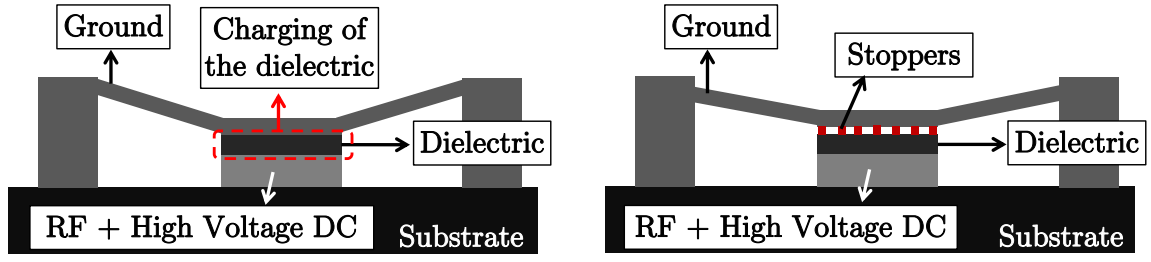
Figure 1.4 Charging of the dielectric in capacitive type of RF-MEMS switches (left) and method of "stoppers" to prevent stiction.

Stiction of the capacitive type RF-MEMS switches is known to be the most common failure mode. It is mainly related to the charging of the dielectric. However, many other conditions have also effect on stiction such as moisture, surface roughness or charging of the substrate. One of the common approaches to prevent stiction is using stoppers at the contact region. It apparently decreases the down-state capacitance; however, significantly minimize stiction probability due to two main reasons. Firstly, it increases the distance between the movable membrane and the RF signal line; thus decreases the force in between them at down-state. Secondly, the touching area at the contact region is smaller which reduces the stiction due to moisture. However, the charging of the dielectric still occurs and creates risk of stiction for high number of switching cycles.

In order to achieve reliable capacitive type RF-MEMS switches, the charging of the dielectric needs to be minimized. One of the easiest methods to prevent charging of dielectric is using separated electrodes. With this technique, the applied high actuation voltage is completely isolated from the RF signal line where the contact occurs. However, the pull-in voltage of capacitive type of RF-MEMS switch, which means the minimum voltage required to move the membrane from up-state to down-state, increases. A further improvement is achieved if the actuation electrodes are placed lower elevation than the contact. In this case, the pull-in voltage again increases but the interaction between the high voltage electrodes and the movable membrane is minimized. The main bottleneck of applying these techniques is the requirement of larger area. The need of additional actuation electrodes significantly increases the required area on the chip. Figure 1.5 shows these two proposed techniques to prevent stiction. In this thesis, the configuration proposed in Figure 1.5, the capacitive type shunt RF-MEMS switch with separated and lowered electrodes is used.
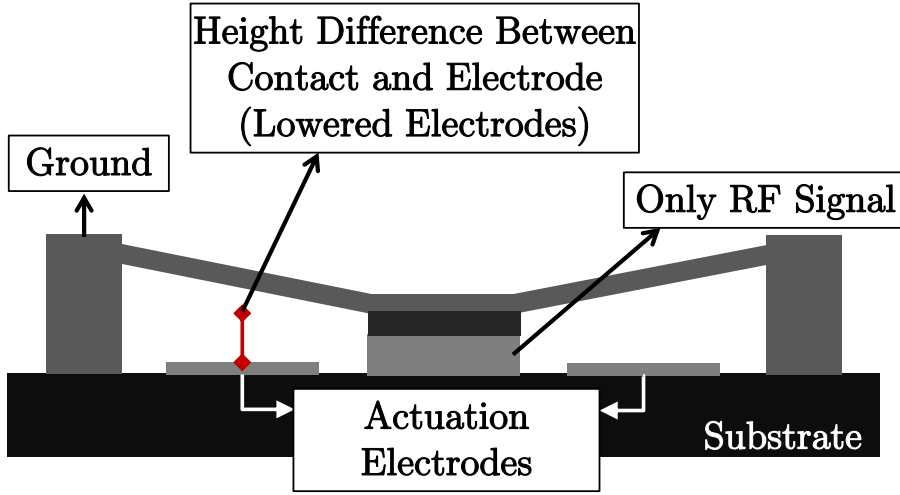
Figure 1.5 The proposed RF-MEMS switch configuration for reliable operation: Capacitive type shunt RF-MEMS switch with separated and lowered actuation electrodes.

Figure 1.6 shows a typical capacitance versus voltage (C-V) curve of a capacitive type RF-MEMS switch. The switch provides an up-state capacitance ($C_{up-state}$) when no electrode voltage is applied. When the voltage of actuation electrode is increased, the movable membrane starts to bend down and the contact capacitance starts to increase. After a specific voltage, $V_{pull-in}$, the membrane snaps down and the maximum capacitance, $C_{down-state}$ is achieved. To release the movable membrane again, the electrode voltage is decreased and after a specific voltage, $V_{pull-out}$, the movable membrane releases and takes its initial up-state position. The dielectric charging phenomena can be easily observed by the help of C-V curve since the dielectric charging affects the $V_{pull-in}$ and $V_{pull-out}$.

The voltage gap between the pull-in and pull-out voltages is an important parameter and strongly affected by the design of the switch. The proposed technique in this thesis (Figure 1.5) has the advantage of narrow gap between the pull-in and pull-out voltages, as can be seen by blue curve in Figure 1.6. First of all, the stiction due to the dielectric charging occurs at higher number of cycles compared to the red curve, which is a typical C-V curve of a capacitive type RF-MEMS switch. Secondly, as can be seen in Figure 1.6, the RF-MEMS switch cannot provide all the capacitances between up-state and down-state capacitances; thus cannot be used as a variable capacitor device. However, the proposed technique in this thesis provides wider range of available capacitances; hence allows the device use as a tunable capacitor.
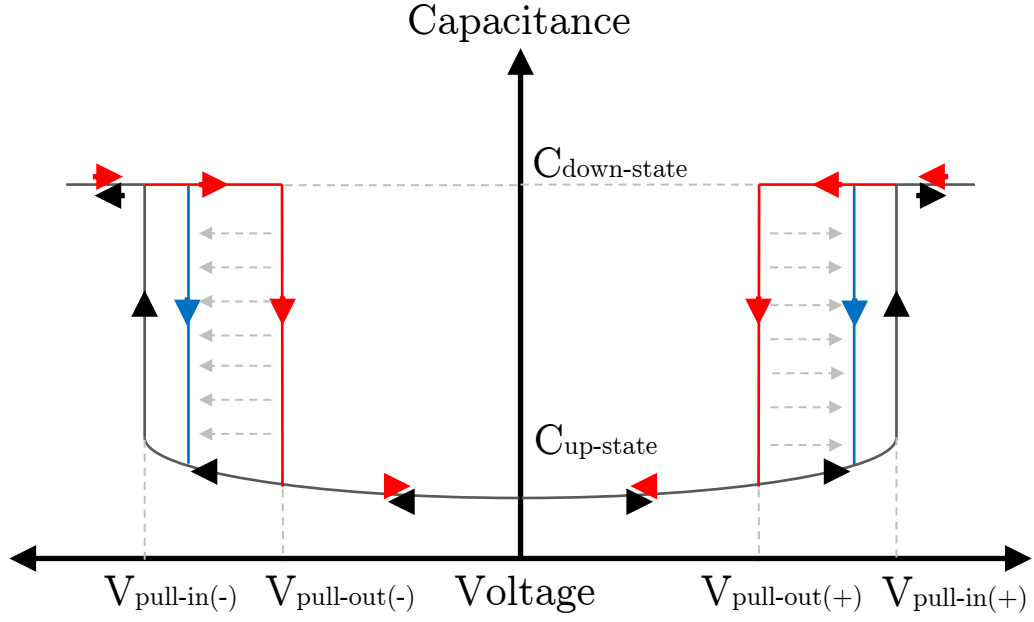
Figure 1.6 A typical C-V curve of a capacitive type RF-MEMS switch. Red curve shows a typical release while the blue curve shows the release characteristics of the proposed technique in this thesis.

- *Commercial RF-MEMS Switches*

According to ITRS and EPoSS, RF-MEMS technologies have a crucial role for the development of tunable filters, matching networks and re-configurable transceiver ICs [20, 21]. In the US, RF-MEMS switch/tuner technologies have reached a high level of technical maturity. Companies such as Radant, WiSpry and MEMtronics are offering discrete packaged components up to 40 GHz [22, 23, 24]. Re-configurable impedance tuners enabled by RF-MEMS switched capacitors are commercialized by WiSpry for low cost, high volume antenna tuning networks in mobile phones [22]. Similar tuner products are also being developed by Cavendish Kinetics [25] and DelfMEMS [26]. Another very high performance and very reliable ohmic type of RF-MEMS switch is provided by OMRON [27].

Currently, the long-term reliability problems associated with RF-MEMS devices have been almost solved. However, packaging and reliability are still most challenging concerns for the commercialization of any new RF-MEMS device. The next section gives an overview of technology and material evaluation of capacitive type RF-MEMS switch technologies which have a significant impact on the way to commercialization.

- *Technology and Materials Evolution of Capacitive Type RF-MEMS Switches*

RF-MEMS technologies are much simpler and have a lower number of process steps than any CMOS or BiCMOS process. A state-of-the-art CMOS process can have more than 30 masks; however, most of the RF-MEMS processes have 5 to 10 masks in total only. Moreover, a typical CMOS process has 500 to 1000 process steps whereas it is below 100 for RF-MEMS. At first sight, the general impression about RF-MEMS development is quite optimistic. However, there are still many other challenges for RF-MEMS technologies that differ from CMOS processes.

CMOS processes have reached a mature and stable condition, so that the microelectronics community has already discriminated materials using the terms *"CMOS compatible"* and *"CMOS incompatible"*. However, it is not the case for RF-MEMS technologies. As an example, all the aforementioned commercial RF-MEMS products use different materials, showing that there is no standard material combination providing the best performance for RF-MEMS devices.

An RF-MEMS process development starts with the appropriate substrate choice. Many different materials can be used as the substrate material such as glass, ceramic, silicon or polymer. In between these materials, the most promising one is silicon due to the well-known processing techniques and the low cost. However, if the RF-MEMS process is to be integrated into a CMOS process, one of the main difficulties is the low resistivity of the silicon substrate. Different techniques have been proposed to prevent substrate losses. In [28], a simple technique of backside etching is proposed and applied in order to prevent this. Another way to diminish high substrate loss is making it more conductive and using it as a ground shield plane. It has been demonstrated by a highly doped region which can be realized using poly-silicon [29] or additional implantation steps [30]. Nevertheless, the first step before starting the process development should be the selection of the substrate with respect to the application frequency and the performance specifications.

The next important step is the selection of the MEMS processing technology. Both surface micromachining and bulk micromachining processing techniques have been successfully demonstrated in the literature. However, surface micromachining is by far the dominating one for RF-MEMS since it is the simplest way to obtain suspended membranes with small size. Bulk micromachining might be chosen if the size and the cost are not the first concerns [31, 32].

The actuation principle is a fundamental choice for RF-MEMS devices. In the literature electrostatic, piezoelectric, electrothermal and electromagnetic actuation principles have been studied. Most of the RF-MEMS switches use the electrostatic actuation principle since the required technology is simple and it provides fast switching speed as well as very low power consumption [33, 34]. Series type designs have been demonstrated in [35] up to 94 GHz by Bosch and in [36] by CNRS-IEMN using the electrostatic actuation principle.

Significant efforts have been spent to prevent dielectric charging of capacitive RF-MEMS switches and to decrease the pull-in voltage [37, 38]. One of the easiest techniques is the separation of the high voltage electrodes from the RF line to prevent the charging of the dielectric. However, results have shown that the separation of the high voltage electrodes increase the voltage requirement because the effective area for the actuation gets smaller. As a result, attempts have started to decrease the required voltage by reducing the stiffness of the membrane, as demonstrated in [39] and [40]. But, the reduced stiffness has caused reliability problems because the restoring force of the membrane also gets smaller; thus increasing the probability of stiction. These results have shown the strong trade-off between the pull-in voltage and the reliability.

On the other side, it is also shown that very stiff membranes have been affected by temperature effects. In [41], a fixed-fixed beam was demonstrated by Daimler-Chrysler but it was strongly influenced by temperature variations. A huge effort was spent on designing a stress compensated anchoring in [35, 42, 43]. In [43], a method of different thicknesses for anchoring and the membrane has also been shown with remarkable results. Consequently, an increase of the spring constant not only increases the required actuation voltage but also makes the switch more sensitive against temperature changes.

Besides complicated RF-MEMS process approaches, very simple processes have also been proposed and successfully demonstrated. In [44], curled up cantilevers have been shown with a very stable performance up to 120 °C by EADS. Actuation by using fringing electrostatic fields between the curled up fingers has been demonstrated in [45], by IMEC. Another promising approach is the application of bidirectional actuation which allows actuating the membrane from both top and bottom. By using this approach, the stiffness of the movable membrane can be decreased without any negative impact, as demonstrated in [46]; however, the process to realize such a device is relatively complex. The references [47, 48, 49, 50] can be given as examples for piezoelectric, electrothermal and electromagnetic actuation principles.

The selection of materials has also significant importance for the RF-MEMS devices. The choice for the RF signal line is relatively easy. Highly conductive metal with a thickness larger than the skin depth in the frequency range of interest can satisfy the requirements for the RF signal line. Most of the studies have been done using Al, Au or Cu. Power handling of Al and Au is limited due to electromigration, while Cu can offer higher conductivity and better electromigration stability.

The type of the dielectric material for the capacitive type of RF-MEMS switches is another important aspect since it strongly affects the unwanted charging of the dielectric during the operation. In general, $SiO_2$, $Si_3N_4$, AlN, $Ta_2O_5$ and $Al_2O_3$ are the materials that have been investigated as a dielectric material for capacitive type RF-MEMS switch. In addition, the type of the voltage polarity and the type of the substrate affect the charging of the dielectric, as studied in [51] and [52], respectively. Furthermore, the humidity has also effect on charging [53]. The different types of charging mechanisms have been extensively examined in [54] and [55]. Dielectric-less capacitive switches have also been proposed by [56] and [57].

Although the type of the material for the sacrificial layer looks not critical, it has a significant effect on the final reliability of the device and the yield of the process. Using photoresists as the sacrificial layer is the simplest and the cheapest technique but its dry removal leaves some residuals which degrade the performance and decrease the yield of the process. However, wet release has also some disadvantages since a $CO_2$ supercritical drying is necessary after the release process, which is a low throughput and cost intensive step. Beside photoresist, materials like silicon dioxide, poly-silicon, and copper have been also investigated as sacrificial layer. Electroplated copper is widely used by Intel [58], Teravicta [59], IBM [60] and Radant [61]. Oxides have also been used with wet and gas phase release techniques [62, 63, 64].

The last important selection is the material type of the movable membrane since it should exhibit large yield strength and low sensitivity to creep. Both oxides and metals can be used as the movable part of the switch. The simplest way is to use a metal such as Al, Au, Ni or Cu. However, using single layer metals for the membrane increases the influence of the temperature induced stress. Al alloys can provide very good mechanical properties but resistivity may increase due to the alloying [33]. As a result, the material of the movable membrane should be thick enough and have well defined stress. Thicker layers with higher conductivity have advantages both in mechanical and electrical respects. Multi-stack layers are also more robust against temperature variations if enough attention is given to the stress control.

In conclusion, there are many ways and different materials to realize RF-MEMS switches. However, the type of the process and the materials needs to be decided with respect to the specifications coming from the application. Therefore, the application has a strong effect on both selection of the materials and the process types.

- *Integration of RF-MEMS into a CMOS/BiCMOS Platform*

In the 1990s, sub-micron CMOS technologies have started to show up with limited RF performance. They provided high performance digital and logic; however, they were not fast enough for RF. The more common approach at that time was the System-in-Package (SiP) approach, which combines the best technologies for different parts of the system in a single package. SiP provided the best performance systems but the total cost and size was dominated by the packaging and integration. Starting with years 2000, the CMOS technology node has gone below 130 nm and then System-on-Chip (SoC) approach has started to be pronounced and dominated many applications. Since that time, RF front-end has still been following the digital and the logic part with the best available technology node. However, starting with 45 nm and below, the logic part of the systems has started to operate with very low $V_{dd}$, which is not the best choice for RF front-ends. Furthermore, technology nodes such as 32 or 22 nm have been realized with many limitations in Back-End-off-Line (BEOL), making the RF designs more challenging. Now, heterogeneous integration is the new trend developed by chipset providers. Similar to SiP, it is again the combination of different technologies in a package/system with a very small footprint. It is almost the same approach as 20 years ago; however, the integration methods now are much more advanced which allows minimizing the overall size of the systems.

The incredible shrinking of CMOS, known as the *"More Moore"* approach is still the hottest and most challenging topic for the microelectronic industry, especially for the digital part of the system. On the other side, adding different functionalities to CMOS such as high voltage/power devices, sensors or actuators is known as the *"More than Moore"* approach. Next generation mobile systems are expected to provide not only more processing power, but also interaction with people and the environment. Following the *More than Moore* approach is one of the best choices to realize such smart systems together with the new heterogeneous integration platforms. Figure 1.7 shows different approaches from technology and system perspectives [20, 65].
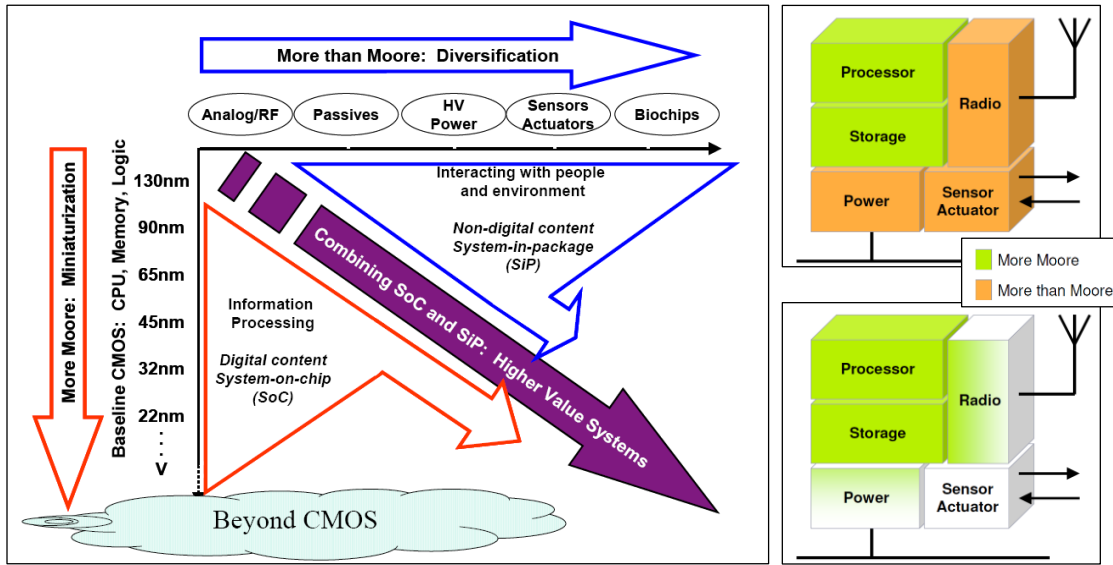
Figure 1.7 *"More Moore"* and *"More than Moore"* approaches from the technology and system perspectives [20, 65].

One of the main functionality modules which can be added to CMOS or BiCMOS platforms is the RF-MEMS switch module. As indicated in Figure 1.8 (left), there are three main drivers for the MEMS industry; namely the performance, cost and form factor. The type of the driver has a great importance for the process development. The decision for CMOS+MEMS integration or heterogeneous integration strongly depends on the driver type of the application; thus the size of the market. Figure 1.8 (right) shows that there should be a clear decision in terms of the integration scheme before starting the process development [66].
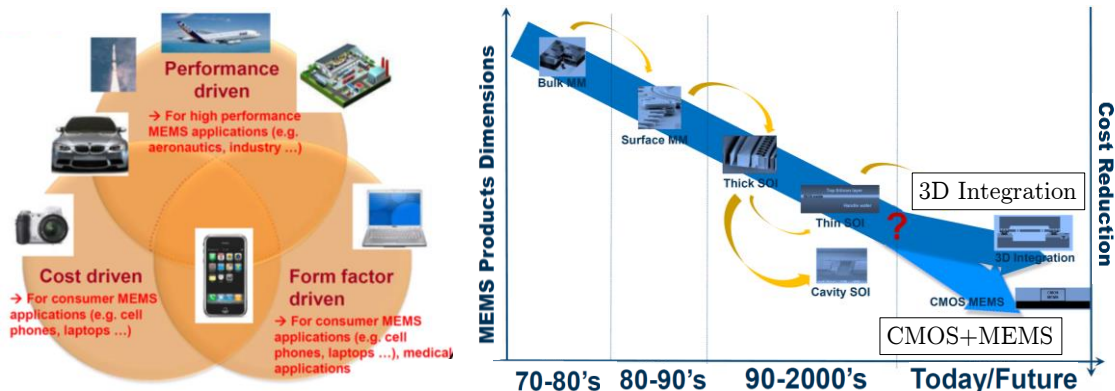


Figure 1.8 Main drivers of the MEMS industry (left) and the evaluation of the different processing and the integration techniques for MEMS processes [66].

In the literature, several methods have been suggested to integrate MEMS components into semiconductor die using hybrid, monolithic, and post-processing techniques. The fabrication techniques in MEMS and semiconductor processes are similar but low throughput, difficult repeatability and low yield of MEMS processes make the combination very challenging. Moreover, the high yield requirement of CMOS processes which allows decreasing the cost are highly threatened by integrated MEMS devices. All these bottlenecks force the industry to use the heterogeneous integration techniques as an intermediate solution. In these days, chip stacking using Through-Silicon-Vias (TSVs) and interposer techniques have become popular to combine different dies together. Figure 1.9 summarizes the basic integration techniques of MEMS into a CMOS platform.
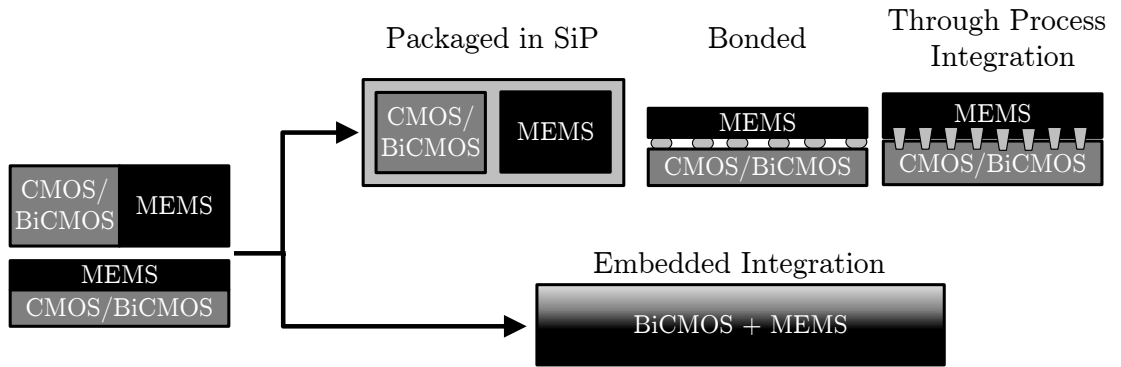


Figure 1.9 Different concepts for MEMS and IC integration.

Significant numbers of research works have been carried out to this date; however, most of them lacked real demonstration of monolithic integration of active circuits and RF-MEMS switches. So far, RF-MEMS together with active RF circuits have been realized mostly as hybrid circuits [67, 68, 69]. The X-band switched dual-path PAs and LNAs reported by the US Company Rockwell Scientific are the first real examples of a successful monolithic integration of active devices with RF-MEMS switches into a GaAs MMIC foundry process [70]. Many attempts have been also tried within the FP7 project MEMS-4-MMIC, utilizing prototype RF-MEMS switches on-chip integrated on the MMIC GaAs technology but the maturity of the developed technologies could not achieve commercialization levels [71, 72].

By using the hybrid and heterogeneous integration techniques, different products have already taken their place in the market. The interconnect losses from these integration methods are in an acceptable range for the frequencies up to 40 GHz. However, for the higher frequencies, interconnect losses become more important and define the overall system performance. Due to the significant effect of interconnect losses in interposer or chip stacking techniques, embedded integration of RF-MEMS components into the semiconductor technologies are necessary especially for mm-wave applications.

## 1.4 Dissertation Organization

In this thesis, the embedded integration of the capacitive RF-MEMS switch into a BiCMOS process is proposed for mm-wave applications. The fully embedded nature of integration helps to minimize the parasitic losses at mm-wave frequencies. Throughout the thesis, process integration, device simulation and characterization are described. Furthermore, packaging of the RF-MEMS switch, on-chip high voltage generation, robustness and reliability tests are also studied. Lastly, the developed module is demonstrated with different passive and active mm-wave circuit examples.

The thesis is organized as follows: In Chapter 2, the general introduction to technology is given and process integration of the RF-MEMS switch is detailed. In Chapter 3, the RF-MEMS switch modeling and characterization is studied with the experimental results and the performance figures. The requirements of the packaging process and two different packaging approaches are described in Chapter 4. In Chapter 5, the on-chip high voltage generation circuit design and the results are given. The robustness and reliability of the RF-MEMS switch is studied in Chapter 6. Finally, different circuit demonstrations realized by using the developed RF-MEMS switch are described in Chapter 7 and the thesis is concluded in Chapter 8 with general remarks and future directions.

# 2 Technology

## 2.1 Introduction

RF-MEMS switch development requires stable process conditions. As extensively studied in Chapter 1, the demonstration of RF-MEMS devices is a big step, but considering the whole value chain, there is still much remaining work to replace any electronic component with an RF-MEMS counterpart. It should be emphasized that the first and the most important step is to have a stable process condition. Therefore, CMOS/BiCMOS processes can be very good candidates as a platform for RF-MEMS devices, since these processes are very mature and exhibit good yield. The only open point is the cost of these technology platforms, since CMOS cost drops sharply only if it is in mass production, i.e. > 10 M units per year due to the high mask costs.

Currently, monolithic integration of an RF-MEMS device into a BiCMOS platform is done in two different ways: above-IC technique and BEOL integration. Both techniques have some advantages and limitations. In this thesis, the BEOL integration is chosen in order to minimize the parasitics and the cost of the fabrication

There is an obvious advantage of using CMOS platforms to build RF-MEMS devices but there are also some limitations. These platforms are optimized in order to increase the yield of the CMOS devices. Therefore, even the smallest change can degrade the yield. Most of the RF-MEMS devices can be built using the available metals and other layers of CMOS process, but the main limitation is the residual stress of these layers. In CMOS processes, the stress levels are optimized in order to compensate the complete stress of the full stack, including FEOL and BEOL. This is a physical limitation for RF-MEMS devices because they need suspended parts with low residual stress. Therefore, the main challenge is not only building an RF-MEMS device in CMOS but also keeping the CMOS process qualified maintaining high yield.

Chapter 2 provides a general overview of the used BiCMOS technology and the stress characterization of metallization layers in BEOL. It starts with a brief introduction of IHP's different technologies in 0.25 μm node in section 2.2. The stress control of the metal stacks and the integration scheme of the RF-MEMS switch into the BEOL of the BiCMOS process are given in sections 2.3 and 2.4, respectively. In

addition to the process flow of the MEMS module, the formation of the contact of the RF-MEMS switch is also given in section 2.4. Chapter 2 is concluded with some achievements and general remarks in section 2.5.

## 2.2 IHP's 0.25 $\mu$m SiGe:C BiCMOS Technologies

The integration of the RF-MEMS switch has been done into the 0.25 µm BiCMOS node. IHP's 0.25 µm node has three main BiCMOS technologies, namely SGB25V, SG25H3 and SG25H1. SGB25V is the basic low cost technology and includes 3 different HBTs with maximum $f_{max}$ of 95 GHz. SG25H3 technology offers HBTs with an $f_{max}$ of up to 180 GHz while the highest performance SG25H1 offers HBTs with $f_{max}$ values of 220 GHz. Table 2.1 summarizes the main performance parameters of the HBT transistors for the different 0.25 µm technologies [7].

Table 2.1 Performance parameters of HBT transistors for different 0.25 µm technologies of IHP [7].

|  | SGB25V | | |
| --- | --- | --- | --- |
|  | High Performance | Standard | High Voltage |
| $f_{max}$ (GHz) | 95 | 90 | 70 |
| $f_t$ (GHz) | 75 | 45 | 25 |
| $BV_{CEO}$ (V) | 2.4 | 4 | 7 |
|  | SG25H3 | | |
|  | High Performance | Standard | High Voltage |
| $f_{max}$ (GHz) | 180 | 140 | 80 |
| $f_t$ (GHz) | 110 | 45 | 30 |
| $BV_{CEO}$ (V) | 2.3 | 5 | 7 |
|  | SG25H1 | | |
|  | High Performance | | Standard |
| $f_{max}$ (GHz) | 220 | | 190 |
| $f_t$ (GHz) | 180 | | 190 |
| $BV_{CEO}$ (V) | 1.9 | | 1.9 |

All 0.25 µm BiCMOS technologies have 5 aluminum metallization layers in BEOL. Three thin metallization layers for digital signal routing and two thick metals with thicknesses of 2 µm and 3 µm for high-Q passive components are offered. A metal-insulator-metal (MIM) type of capacitor is also available between Metal2 (M2) and Metal3 (M3). The thin $Si_3N_4$ dielectric layer with an approximate thickness of 55 nm is placed between M2 and M3 in order to achieve a high capacitance density of ~1.15 $fF/µm^2$. All the available passive components and their performance parameters are given in Table 2.2.

Table 2.2 Performance parameters of different passive components in 0.25 µm technologies offered by IHP [7].

| Passives | | |
|---|---|---|
| | SG25H1/H3 | SGB25V |
| MIM Capacitor $(fF/µm^2)$ | 1.15 | 1.15 |
| N+ Poly Resistor $(\Omega/\square)$ | 210 | 210 |
| P+ Poly Resistor $(\Omega/\square)$ | 280 | 310 |
| High Poly Resistor $(\Omega/\square)$ | 1600 | 2000 |
| Varactor $(C_{max}/C_{min})$ | 3 | 3 |
| Inductor Q @ 5 GHz | 18 (1 nH) | 18 (1 nH) |

SG25H1 and SG25H3 technologies offer the same BEOL while SGB25V technology has a slightly different BEOL than the others in terms of the metallization and the $SiO_2$ thicknesses. SG25H1 and SG25H3 technologies are chosen for the integration of RF-MEMS switch module considering the expected high frequency performance of the RF-MEMS switches because these two technologies can provide mm-wave circuits up to 100 GHz and above.

The cross section of the BEOL of the SG25H1/H3 technologies is seen in Figure 2.1. All the aluminum metallization layers are covered by TiN/Ti layers from both top and bottom sides as a barrier layer between the aluminum and $SiO_2$. The connection vias between different metallization layers are filled with tungsten and are isolated from the $SiO_2$ by TiN. The $SiO_2$ dielectric layer is used to isolate the metallization layers. The top passivation layer includes 1.5 µm $SiO_2$ and 400 nm $Si_3N_4$. The approximate thickness values of each layer are also indicated in Figure 2.1 [73].
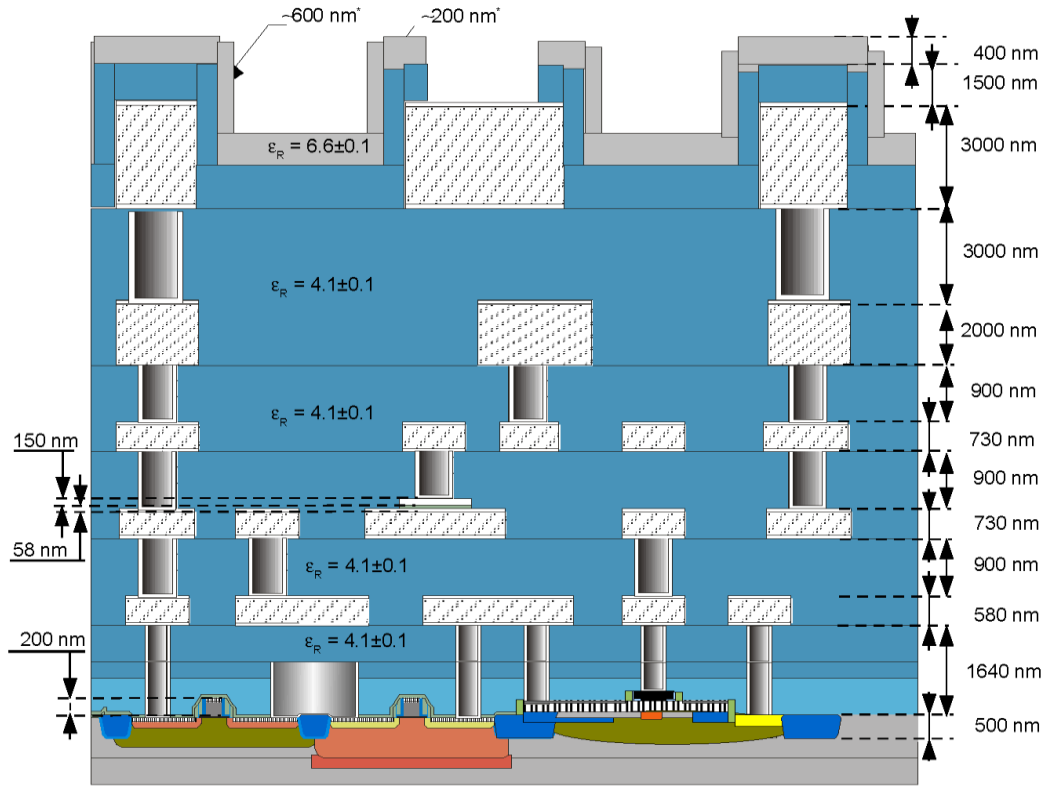
Figure 2.1 Generic cross-section view of SG25H1/H3 BEOL [73].

## 2.3  Stress Control of the BiCMOS Metallization Layer Stack

Multi-layer processes, such as BiCMOS, are optimized to control the total stress of the entire BEOL and FEOL layers. The stress in aluminum metallization layers is generally tensile which makes it challenging to be used for RF-MEMS applications. Although certain designs may benefit from such stress effects [74], uniformity over the wafer, reliability and repeatability remain problematic in case of such high residual stresses and prevent easy commercialization of RF-MEMS devices. Mechanical, electrical and RF performance parameters of an RF-MEMS switch are influenced by the residual stress of the movable membrane as well. Furthermore, the residual stress of the membrane has to be well controlled in order to have repeatable and reliable structures. Figure 2.2 shows the cross section of the M3 stack of the SG25H1/H3 BEOL.
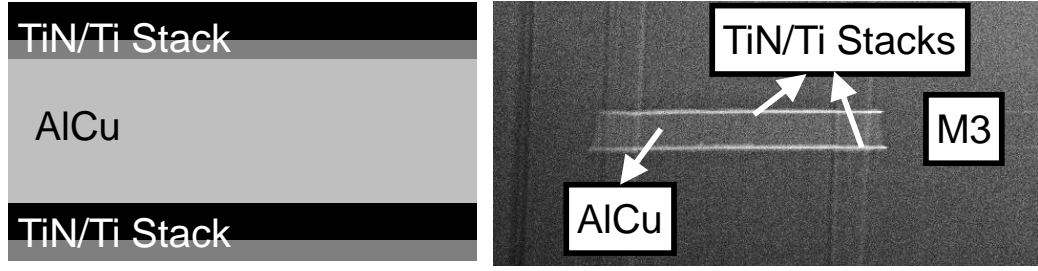
Figure 2.2 Generic cross-section (left) and FIB cut (right) of the M3 layer in SG25H1/H3 BEOL.

TiN/Ti stacks are mainly used as barrier layer between aluminum and the $SiO_2$ layers. The TiN/Ti stacks, with an effective Young's modulus of ~410 GPa, are much tougher than aluminum, therefore the total stress characteristics of the whole TiN/Ti/AlCu/TiN/Ti stack can be controlled by the TiN/Ti stacks. In this thesis, the bottom TiN/Ti stack is selected to control the overall stress gradient of M3.

Figure 2.3 shows the measurements of four different cantilevers fixed from one side. The cantilevers were fabricated using 4 different recipes. The recipes are developed by changing the deposition conditions and the thickness of the TiN and Ti layers. The bending of the cantilevers was characterized by a White-Light Interferometer (WLI) in order to determine the type of the stress gradient. The numbers in each picture show the bending of the tip of the cantilever in *z* direction.
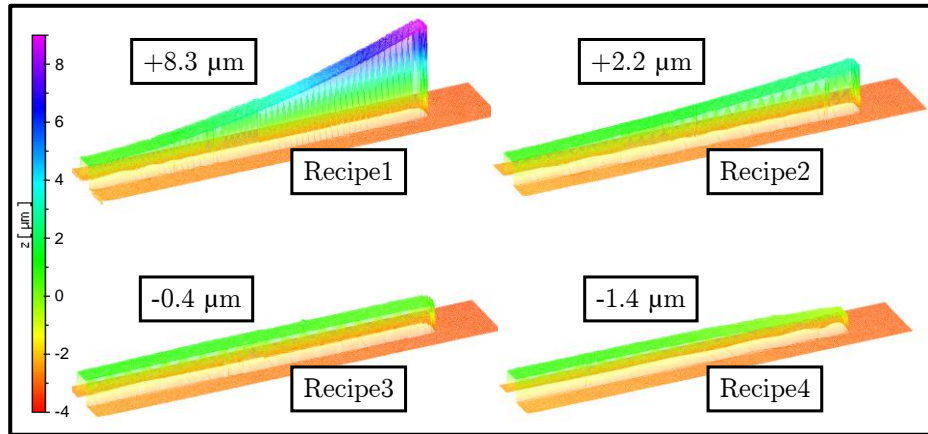


Figure 2.3 WLI measurements of 4 different cantilevers using four different recipes for the bottom TiN/Ti stack. The numbers in every picture show the bending of the tip of cantilever in z direction.

As seen in Figure 2.3, the stress gradient of the whole M3 stack can be controlled from tensile to compressive by using different recipes of bottom TiN/Ti stack. Note that the recipes used do not cause any violation of the original M3 process specifications, such as sheet resistance (Figure 2.4). In this work, Recipe3 was chosen to improve the reliability of the switch by decreasing the contact area when the switch is in the down-state. The preferred stress characteristic for improved reliability decreases the down-state capacitance. This is extensively studied in Chapter 3 by simulations and measurements.

## 2.4 Process Integration of the MEMS Module

The RF-MEMS module integration starts after finalizing the BiCMOS process. As explained in the previous section, the BiCMOS process is finished with only a small modification of the M3 deposition recipe. This small change of the recipe slightly decreases the sheet resistance of M3. However, it should be noted that the achieved sheet resistance value is still in the specification limits of the process. Figure 2.4 shows the sheet resistance values of a production lot which has wafers for both Multi-Project-Wafer (MPW) production and MEMS process development.
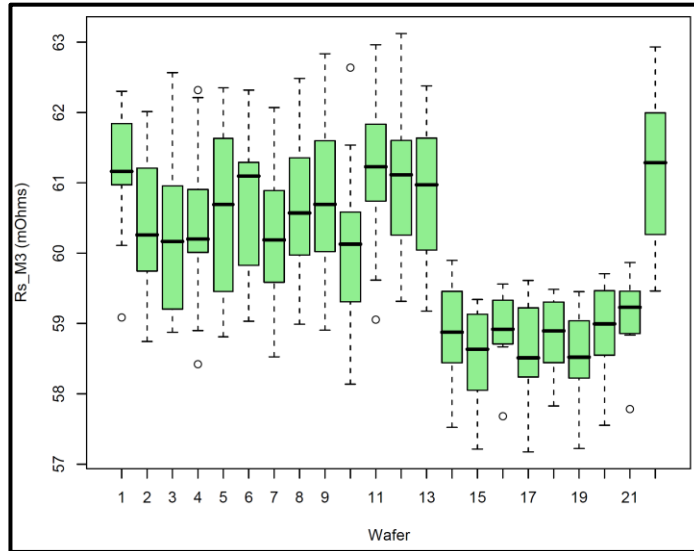


Figure 2.4 Sheet resistance variation of M3 for different wafers in a lot. Wafers 1 to 13 and 24 are processed with standard recipe while wafers 14 to 21 are with Recipe3.

The wafers numbered from 1 to 13 and 24 are for MPW production and the standard M3 deposition recipe was used. The wafers numbered from 14 to 21 are the MEMS process wafers which use the special developed recipe for the stress control of M3. In Figure 2.4, it can be clearly seen that the sheet resistance of the MEMS wafers are slightly lower than for the MPW production wafers. However, the process specifications define the minimum sheet resistance for M3 to be 40 mΩ, and the maximum 70 mΩ. Therefore, it can be concluded that the small change of the M3 recipe does not significantly affect the M3 sheet resistance and the requirements of the process specifications are still fulfilled. Figure 2.5 shows the additional MEMS process flow to the BiCMOS process.
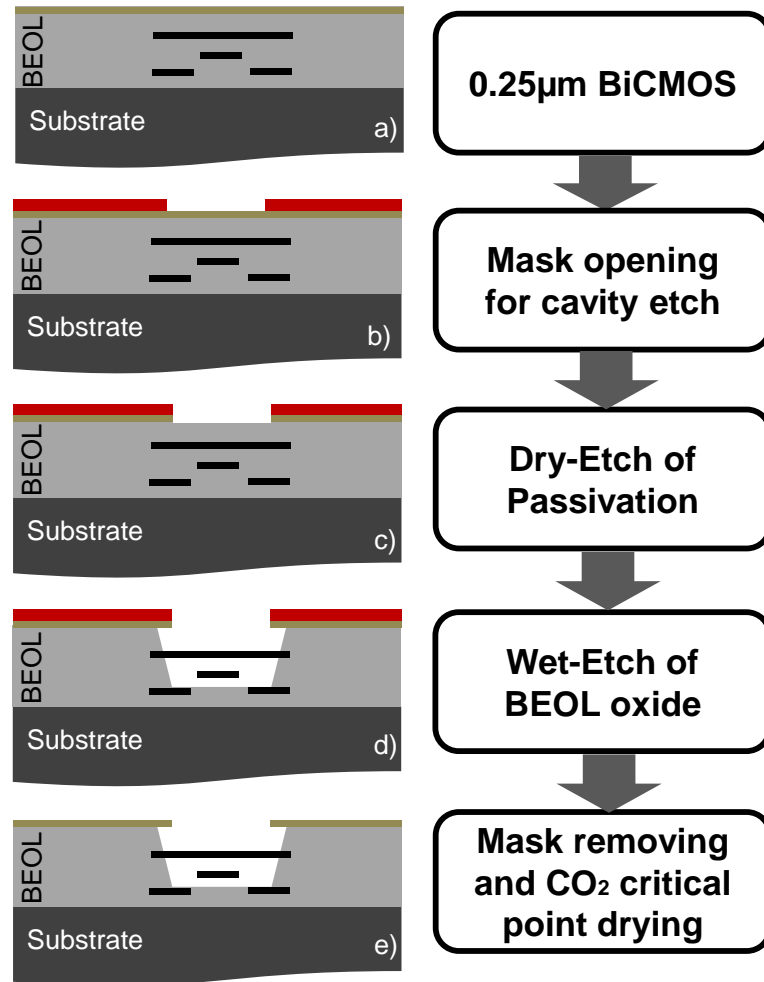


Figure 2.5 The complete process flow of RF-MEMS module added to 0.25 μm BiCMOS technology [75].

After finalizing the BiCMOS process (Figure 2.5a), a lithography step (Figure 2.5b) is followed by an RIE process step to remove the passivation of the RF-MEMS switch cavities (Figure 2.5c). This step also helps to decrease the time required for the wet etch release. After the dry etching of the passivation layer, the BEOL oxide is etched down to M1 using 10 % buffered HF solution (Figure 2.5d). The solution is mixed with glycerol in order to increase the selectivity to AlCu which helps to minimize the AlCu under-etch of M3. The wafer is cleaned and rinsed after the wet-etch. Finally, the $CO_2$ critical point drying step is applied to prevent unwanted stiction of the MEMS devices after the suspended membranes are released (Figure 2.5e). The process flow of the MEMS module integration adds only one extra mask to the BiCMOS flow [75]. The RF-MEMS module embedded in the BiCMOS process is completed on 200 mm (8-inch) wafer level.

The capacitive type RF-MEMS switch is built between M1 and M3 layers of the BEOL using the developed RF-MEMS module process flow. High voltage electrodes are formed using M1 while M2 is used as the RF signal line. A thin $Si_3N_4$/TiN stack, which is a part of the BiCMOS MIM capacitor, forms the switch contact region and provides DC isolation between the movable membrane (M3) and the signal line (M2). This configuration also provides a height difference between the high voltage electrode and the signal line; hence the signal line serves simultaneously as a stopping layer for the switch membrane. The process integration scheme of the switch after applying the aforementioned RF-MEMS module is presented in Figure 2.6. Figure 2.7 shows SEM view of a fabricated RF-MEMS switch device [75].
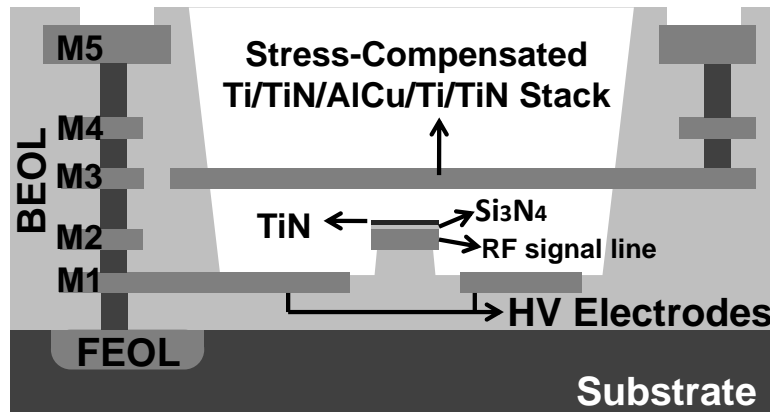


Figure 2.6 Generic cross section of embedded RF-MEMS switch integration into the BEOL of BiCMOS technology [75].
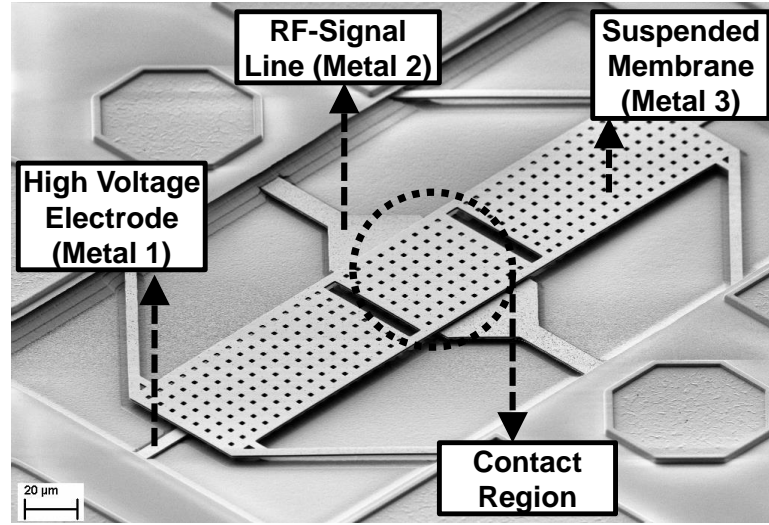
Figure 2.7 SEM view of the RF-MEMS switch [75].

At down-state, the bottom TiN layer of M3 touches the TiN layer on top of the MIM dielectric (Figure 2.8). Due to the high contact resistance between the conductive TiN layers (~4-5 KΩ), the down-state capacitance is dominated by the air-gap capacitance that occurs in the contact area. The air-gap capacitance can be well controlled by optimizing the stress gradient of M3, as explained in previous sections. The MIM capacitor between the membrane and the signal line is used to achieve DC isolation only. The cross-section, as well as the RLC model of the contact region are given in Figure 2.8 for the down-state [76].
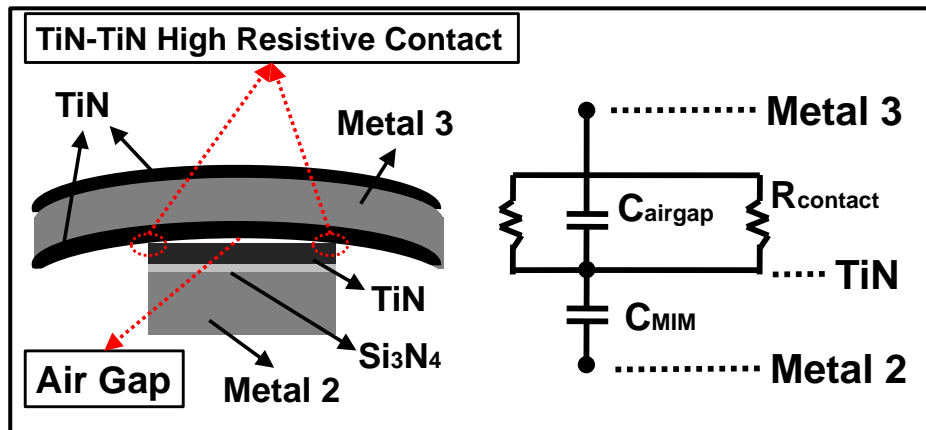


Figure 2.8 Cross-section of contact region for down-state (left). Lumped-element model of the contact when the membrane is in down-state (right) [76].

The WLI measurements of the RF-MEMS switch are depicted in Figure 2.9. Figure 2.9 (left) shows that the RF-MEMS switch is below the surface of the BiCMOS wafer. The slightly stressed membrane shape is also seen in Figure 2.9 (right) which helps to understand the phenomena in Figure 2.8. The z-level of the middle of the membrane is approximately 1.5 µm higher than the edge of the membrane, using the Recipe3.
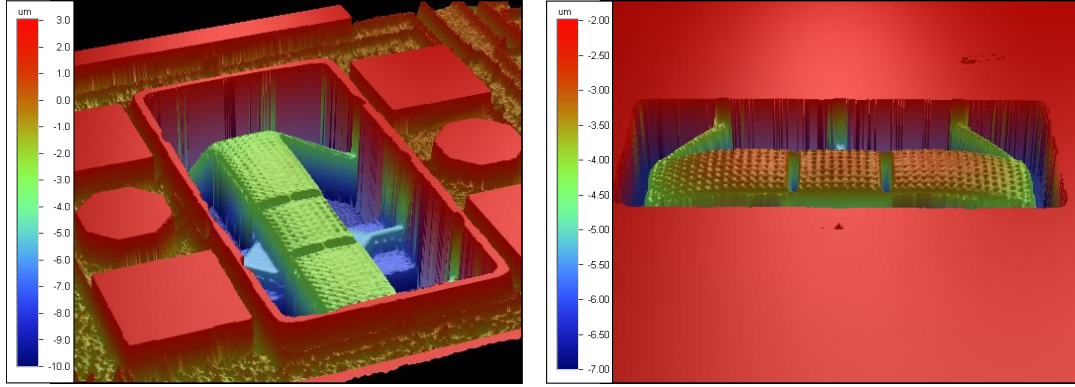


Figure 2.9 WLI measurements of fabricated RF-MEMS switch. The RF-MEMS switch is below the surface of BiCMOS wafer (left). Slightly stressed membrane, middle part of the membrane is at higher z-level than the sides (right).

## 2.5  Conclusion

In Chapter 2, an introduction to the technology used in this thesis has been given. The underlying BiCMOS process has been detailed. The required changes in order to realize RF-MEMS devices in BiCMOS process has been explained by means of stress control of the metallization layers. Finally, the additional process steps and the process flow for the integration of the RF-MEMS switch into the BEOL of the BiCMOS process have been studied. The significant effect of the stress gradient of the movable membrane, especially at down-state, has been also detailed at the end of the chapter.

After the processing of every 200-mm wafer for the RF-MEMS devices, it is not surprising that most devices work perfectly on some parts of the wafer accompanied with non-functional ones on the other parts of the same wafer due to the non-uniform deposition and etch steps. However, the main issue is repeating the same process with similar device performance parameters from wafer to wafer and lot to lot, which can be defined as the first critical term for fabrication: *Repeatability*.

Over a 200-mm wafer, there can be many different types of stress gradients due to non0unifirm deposition and etch steps which strongly change the performance of the device over the wafer. This can be the main obstacle for industrialization of the process and causes the second critical term for fabrication: *Uniformity*.

The aforementioned uniformity issue over the wafer is always a bottleneck for the process engineers since the device performance can significantly change over wafer due the lack of good uniformity which decrease the number of good devices per wafer; hence increase the cost per device. This is the last critical term for fabrication: *Yield*.

To conclude Chapter 2, technology of an RF-MEMS device is the most important point and needs to be carefully planned before any RF-MEMS device development. Serious device developments can only be pronounced when these three important terms are started to be discussed; repeatability, uniformity and yield.

# 3 Modeling and Characterization

## 3.1 Introduction

While the RF-MEMS module integration explained in Chapter 2 provides functional RF-MEMS switch structures, a special design effort is necessary to obtain high performance parameters at mm-wave frequencies. The mechanically movable switch structures need to be optimized in mechanical, electrical and RF domains.

The mechanical domain is one of the most important domains and is closely related to the processing capabilities. First of all, mechanical simulations are more challenging than other simulation domains because the material properties required for mechanical simulations are not well known for every material and may significantly change depending on the process conditions [77]. The extraction of these parameters is not straightforward and needs stable process conditions and substantial effort.

The second simulation domain of RF-MEMS switches is the electrical domain. The electrical domain plays an important role in two different ways. The first is the electrical coupled mechanical (electromechanical) domain which needs to be modeled together with mechanical simulations. The second role of the electrical domain is to set the biasing conditions and the isolation of high actuation voltage from the radio frequency (RF) signal.

The last simulation domain required for optimizing an RF-MEMS device is the electromagnetic domain, where modeling is relatively easier and more straightforward by the help of mature EM simulators. However, one of the most important domains in this thesis is the electromagnetic domain due to the relatively large size of the RF-MEMS devices with respect to the other BiCMOS components such as transistors, capacitors and resistors.

In addition to simulation and modeling, appropriate characterization methods need to be used to obtain accurate, reliable and time-efficient measurements. RF measurement techniques are well developed up to mm-wave frequencies by the help of Vector Network Analyzers (VNA). At mm-wave frequencies, special calibration and de-embedding techniques are required; however, many different techniques are

available and provided by VNA suppliers. Low frequency capacitance measurements, which have also importance in predicting the RF behavior, are also relatively easier. Using an impedance analyzer, capacitance values with an accuracy of around 1 fF can be detected [78]. The most challenging domain for characterization is the mechanical domain. Although well-established characterization techniques such as White-Light-Interferometer (WLI) and Laser-Doppler-Vibrometer (LDV) exist, they need special effort in order to characterize a specific RF-MEMS device.

Chapter 3 starts with the characterization of the material properties to provide accurate information for mechanical simulations. Section 3.3 gives the electromechanical modeling and optimizations. Measurements results of dynamic behavior and comparison of them with the simulated ones are also given in this section. RF modeling and characterization is given in section 3.4. Chapter 3 is concluded with section 3.5 in which general comments about the modeling, characterization and performance figures are given.

## 3.2 Process Dependent Material Characterization

In order to use the exact process parameters in FEM simulations, the Young's modulus and the residual stresses of the layers in the M3 stack are calculated by utilizing the measured frequency-response-functions (FRF) of cantilever test structures. FRF of different length cantilevers are extracted from the measurement results of mechanical responses using LDV (MSA-500, Polytec) [79]. After having the approximate Young's modulus values, the total residual stress of M3 is calculated and compared with the measurements done using an in-line wafer curvature method. Extracted material properties are inserted into the FEM solver in order to achieve a similar bended membrane shape as in measurements. A method to distinguish between the temperature-induced stress and the intrinsic stress is also presented. Finally, the measurement data of membrane topography taken from WLI is compared with the FEM model constructed by making use of the extracted process parameters.

## 3.2.1 Extraction of Young's Modulus and Residual Stress

- *Determination of Young's Modulus*

The knowledge of mechanical material parameters is mandatory for FEM simulators in order to develop RF-MEMS devices due to their influence on device performance and reliability [80]. Different types of methods like mechanical resonance, pull-down voltage and load-deflection method are proposed in the literature in order to estimate the mechanical material parameters [81, 82]. Out of these characterization methods, the determination of the specific mechanical material properties in this thesis is achieved using the method based on mechanical resonance and load-deflection method combined with FEM simulations and statistical methods.

The mechanical resonance frequency and the load-dependent deflection of a mechanical system strongly depend on the material parameters, such as Young's modulus. These two main properties of the specific test structures are simulated using an FEM solver. A multivariate linear regression (MLR) is used to determine a correlation between measurement and simulations of the related material parameters. The method is resulting in different sets of material parameters which show the lowest deviation to measurement results. The proposed calculation method is schematically represented in Figure 3.1.



**FEM Simulation**
- Convergence Study
- Estimate measurement values with different sets of material parameters

**Multivariate Linear Regression**
- Determine correlation between measurement values and material parameters
- Control of sensitivity and linear regression

**Least-Square Method**
- Estimate material parameters
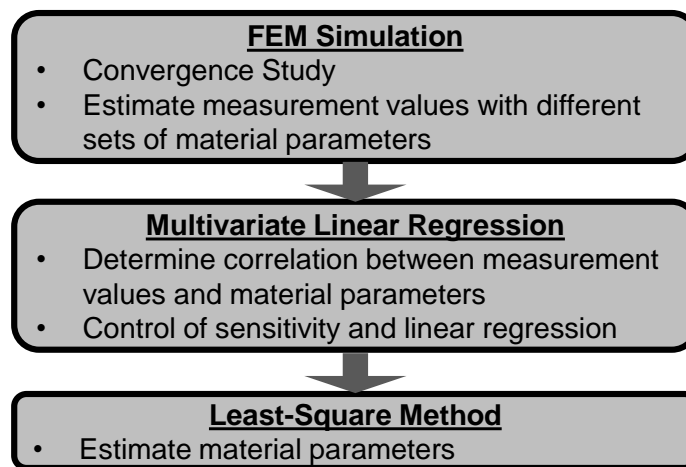
Figure 3.1 The estimation flow for Young's modulus and residual stress [83].

As given in Chapter 2, the movable part of the RF-MEMS switch is realized using the M3 layer of the BiCMOS BEOL stack. M3 consists of a TiN/Ti/AlCu/TiN/Ti material stack. TiN/Ti stacks are used as a barrier and adhesion layer between AlCu and the BEOL SiO$_2$ whereas AlCu (99.5 % Al) is used as the main conductive part of M3. The mechanical properties of the suspended M3 layer are mainly dominated by the Young's modulus of TiN, AlCu and the residual stresses of these layers. Total residual stress in a thin film is a combination of temperature-induced stress and intrinsic stress [84]. Temperature-induced stress is a result of cooling down from deposition temperature to room temperature during the process. Intrinsic stress is mainly determined by crystallographic defects and the grain boundaries [85]. The material parameters are strongly affected by the type of deposition and the deposition conditions, e.g., temperature and pressure. The estimation of Young's modulus and residual stress are done with different types of structures using the method given in Figure 3.1. In order to determine the Young's modulus, clamped beams with different lengths and widths are fabricated and measured (Figure 3.2).
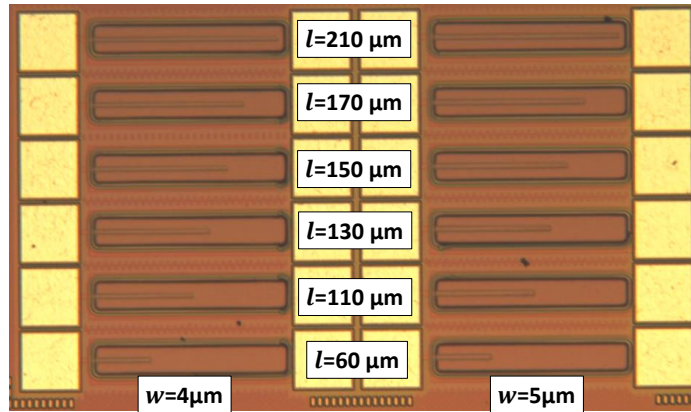


Figure 3.2 Fabricated clamped beams with different lengths and widths for the estimation of Young's modulus with different widths and lengths [83].

The FRF of a simple clamped beam depends on the Young's modulus. The first eigenfrequency can be calculated by equation (3.1) and shows a dependency on the length ($l$), the thickness ($t$), the material density ($\rho$) and the Young's modulus ($E$).

$$f_r = \frac{1}{2\pi * l^2} * \sqrt{\frac{4*E*t^2}{\rho}} \qquad\qquad (3.1)$$

The fabricated test structures are investigated by Focused-Ion-Beam (FIB) to consider process specific characteristics like under etching of the cavity mask (lateral etch of $SiO_2$) and unwanted etching of AlCu (Figure 3.3). The FEM simulations are very sensitive to these geometry changes, therefore the exact dimensions of fabricated structure have to be used for the simulations.
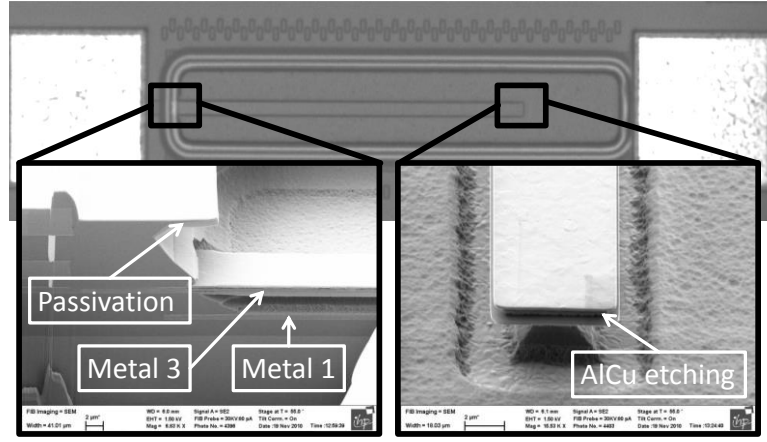


Figure 3.3 FIB cut of the clamped beam showing lateral under-etch and AlCu etch [83].

FRF is independent from residual stress and therefore it is defined by geometry and the effective Young's modulus of the metal stack only. The FRF is detected by electrostatic actuation with a noise-like broadband signal and observing the mechanical response with the LDV. The FRF of a 210 µm beam is shown in Figure 3.4 as an example and provides 6 detectable eigenfrequencies at the maximum frequency value of 2.5 MHz. Due to the low actuation amplitude the total displacement is too small. Considering the large distance between M1 and M3, no influence of squeeze-film damping is expected. Otherwise, damping may introduce a shift of the FRF leading to a significant measurement and calculation error.
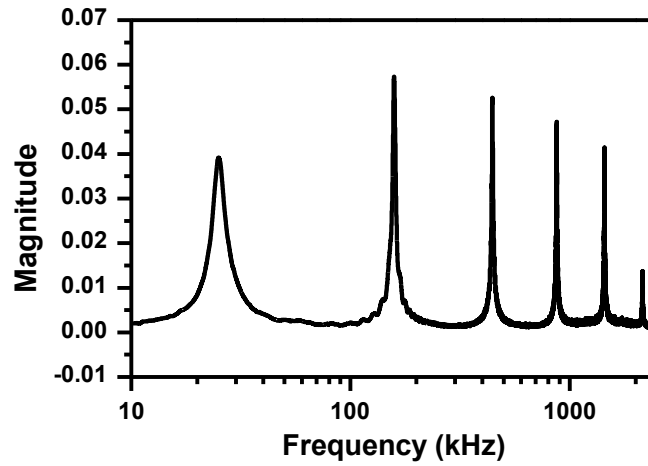
Figure 3.4 FRF graph of a 210 µm clamped beam shows the first 6 eigenfrequencies [83].

The calculated "coefficient-of-determination", which indicates how well the simulated results fit to the measurements, is higher than 0.998 for every eigenfrequency, showing that the linear type of multivariate regression is suitable. The most accurate results of the least-square method with lowest deviation to measurement are shown in Table 3.1.

Table 3.1 Results for determination of Young's modulus [83].

| $E_{AlCu}$ (GPa) | $E_{TiN}$ (GPa) | Maximum Deviation $f_{1-6}$ |
|---|---|---|
| 65 | 410 | 3.0 % |

The Young's modulus of 65 GPa for AlCu and 410 GPa for TiN are in a very good agreement with the literature [86, 87] and the simulated FRF with the estimated material properties shows a small deviation of 3 % compared to the measured FRF. For further analysis of the residual stress, the achieved Young's moduli are applied to RF-MEMS switch structure to analyze the residual stress characteristics of the AlCu and TiN layers in the next section.

- *Determination of Residual Stress*

Residual stress in suspended structures results in membranes bent up or down and strongly influences the performance of the switch. Strong residual stress in thin layers is not only limiting the mechanical performance, but also resulting in poor electrical and RF performance. Furthermore, reliability of the RF-MEMS switch is also affected by the residual stress considering the change of the restoring force of the membrane. By knowing the approximate residual stress, design optimization time can be significantly reduced and the yield of the process can also be increased by optimizing the process flow less sensitive to the residual stress variations.

The residual stress in the suspended membrane is the result of temperature-induced stress during the fabrication process steps and the intrinsic stress of the different layers. The total residual stress of a single layer can be extracted using wafer curvature method. However, the measured stress out of wafer curvature method is the combination of temperature-induced stress and the intrinsic stress.

In order to distinguish between these two different kinds of stress, firstly the aforementioned calculation method in Figure 3.1 is used to estimate the total residual stress. The MLR shows a high sensitivity to residual stress but it has to be considered that the "coefficient-of-determination" varies for different locations in x-direction. Only points with a high "coefficient-of-determination" have been taken into account. The most accurate results of the least-square method out of all calculations are given in Table 3.2. The extracted results from simulations of single layers are in good agreement with in-line stress measurements using wafer curvature method. Characterization of stand-alone layers using wafer curvature method is only possible for the bottom TiN and AlCu layers. Residual stress values in Table 3.2 are used in FEM simulations to obtain the initial stressed case of the membrane.

Table 3.2 Calculated and measured results of residual stress for different layers [83].

| Layer | Residual Stress (MPa) (Calculation) | Residual Stress (MPa) (Wafer Curvature Measurements) |
|---|---|---|
| TiN-Top | - 514 (compressive) | - |
| AlCu | 494 (tensile) | 432 (tensile) |
| TiN-Bottom | -964 (compressive) | - 860 (compressive) |

In fact, the values in Table 3.2 can always be measured for every layer and inserted into the FEM simulator for very accurate mechanical simulations. However, as mentioned before the initial deflection is caused by two effects: temperature-induced stress and intrinsic stress. In order to distinguish between these two effects, firstly the temperature-induced stress is simulated by the thermal expansion coefficients taken from [88] using the "zero-stress temperature" option, provided by the FEM solver, CoventorWare. Using this option, the zero-stress temperature is defined as the material deposition temperature. Then, the structure is cooled down to room temperature which introduces the temperature-induced stress into the metallization stack. The extracted Young's modulus values in the previous section are used in this simulation. The view of the membrane after applying the temperature-induced stress is shown in Figure 3.5.
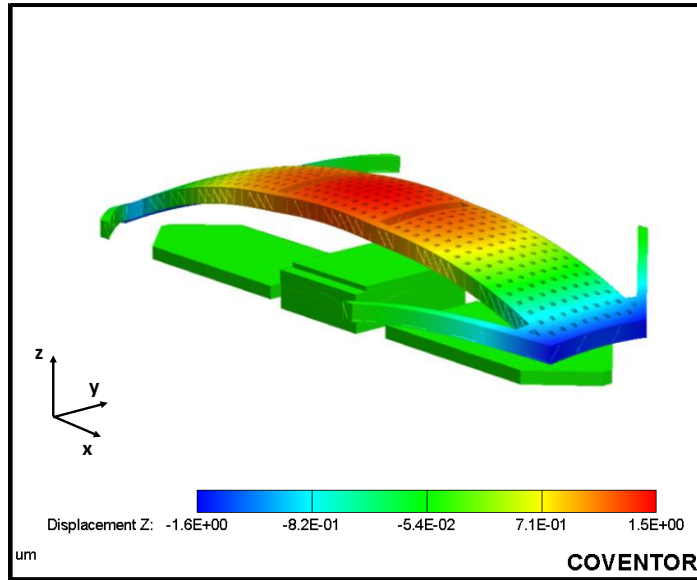


Figure 3.5 Simulation result of the stressed membrane after applying temperature-induced stress. The center of the membrane bends up approximately 1.5 µm [83].

As can be seen from Figure 3.5, the center of the suspended membrane is bent up compared to the anchors whereas the edges are bent down. It is noted that the stress behavior of the membrane in Figure 3.5 includes the temperature-induced stress only and does not include the intrinsic stress of the individual layers of the metal stack. To achieve the final stressed shape of the membrane, the intrinsic stress values for different layers should also be included into the FEM simulator which is done and detailed in the next section.

## 3.2.2 Experimental Data: Topography Measurements

For the topography measurements, the WLI option of the MSA500 from Polytec is used. The measured surface topography of the membrane is given in Figure 3.6.
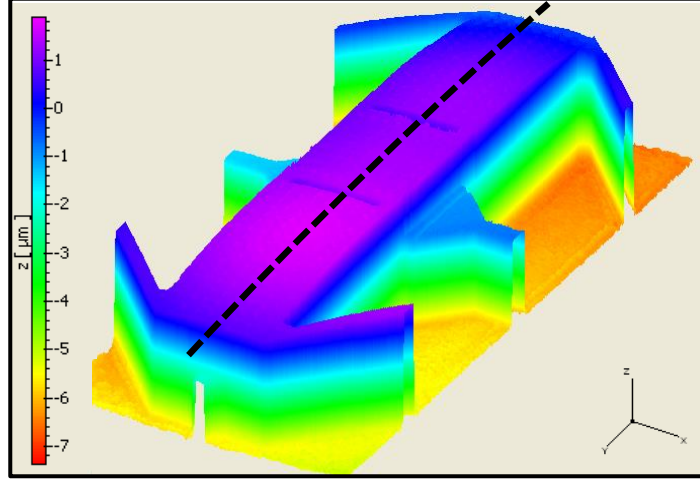


Figure 3.6 Surface topography measurement of the membrane using WLI.

In order to compare the surface topography of the membrane with simulations, the initial deflection of the switch is simulated with the calculated total residual stress (including both temperature-induced stress and the intrinsic stress) and extracted along the black dashed line in Figure 3.6. Figure 3.7 shows the deflection of the membrane at initial state for both measurements and simulations cases. It can be easily seen in Figure 3.7 that very good agreement is achieved using the total residual stress value. The zero-level of initial deflection in Figure 3.7 shows the position of the clamped anchors.

A further investigation is done to distinguish the intrinsic stress from the temperature-induced stress. As mentioned in the previous section, the temperature-induced stress is also simulated in Figure 3.5. As can be seen from Figure 3.5, temperature-induced stress leads to a deflection status higher than measured which shows that intrinsic stress partly compensates the temperature-induced stress and has a significant importance. Without any compensating intrinsic stress, the distance between the grounded membrane in M3 and the high voltage electrodes in M1 is about 1.5 µm which increases the risk for an electrical short between M1 and M3.
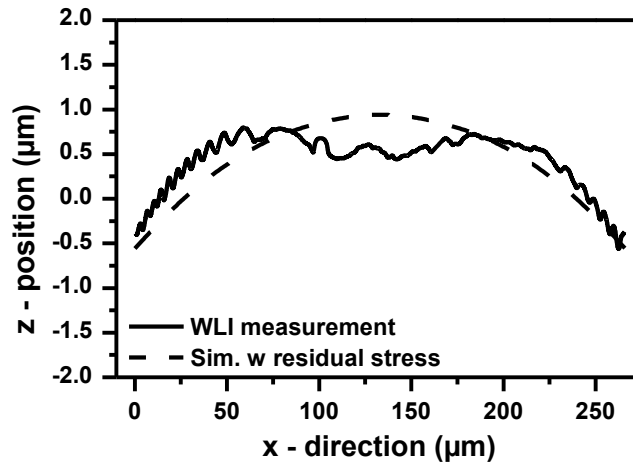
Figure 3.7 Initial deflection of the membrane: Measurement and simulation with total residual stress.

The estimation of intrinsic stress is achieved by adding intrinsic compressive and tensile stress combinations to the different layers. Final values used in simulations are given in Table 3.3. It is noted that the intrinsic values in Table 3.3 are achieved by fitting the initial deflection to the measurements by considering the expected types (compressive or tensile) and values of intrinsic stress of the different layers from the literature.

Table 3.3 Results for determination of intrinsic stress [83].

| Layer | Intrinsic stress MPa (Calculation) |
|---|---|
| TiN-Top | -1240 (compressive) |
| AlCu | -240 (compressive) |
| TiN-Bottom | -1460 (compressive) |

The initial deflection of the switch is again simulated with the resulting temperature-induced stress and intrinsic stress together. The results are given in Figure 3.8 for the following cases: Measurement, simulation with total residual stress, simulation with only temperature-induced stress and simulation with temperature-induced stress together with intrinsic stress.
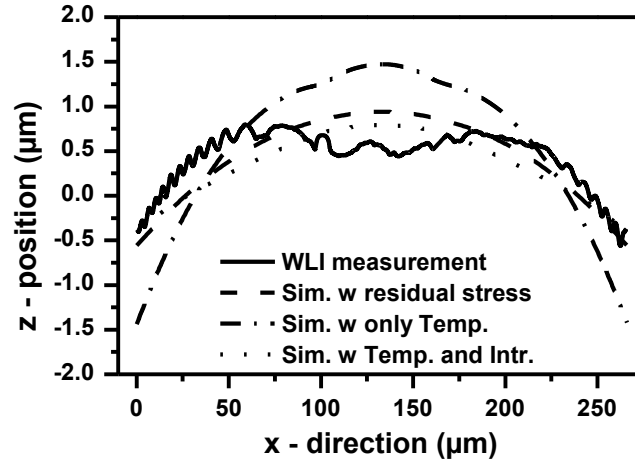
Figure 3.8 Initial deflection of the membrane: Measurement, simulation with total residual stress, simulation with only temperature-induced stress and simulation with both temperature-induced and intrinsic stress [83].

It can be concluded that the total residual stress including both temperature-induced stress and the intrinsic stress can be calculated or measured. Using this value, very accurate FEM simulations are possible. However, it needs a special effort to extract these values because special test structures and characterization techniques are necessary. If there is a need to distinguish between intrinsic stress and the temperature-induced stress, the fitting method can be used. All the results achieved in this section significantly help to model the initial condition of the RF-MEMS switch for FEM simulations in the next section.

## 3.3  Electromechanical Modeling

The electromechanical response of the RF-MEMS switch is simulated using CoventorWare [89]. The performance figures of interest are pull-in voltage, displacement and up- and down-state capacitances. Therefore, the static displacement and capacitance versus voltage are simulated and optimized. The mechanical response to an applied voltage is determined using the MemMech module. The contact capacitance is calculated using the MemElectro module by taking the deformed mesh as the initial state. The material parameters and the residual stress values calculated in the previous section are used to achieve the initial stressed membrane.

### 3.3.1 FEM Model of the RF-MEMS Switch

Electromechanical modeling of the RF-MEMS switch is started with the definition of residual stress in order to achieve the initial bent shape of the membrane. The initial state of the membrane significantly affects the dynamics of the RF-MEMS switch because it changes the initial gap between the high voltage electrodes and the movable membrane. A careful optimization is necessary to achieve the exact initial position of the membrane. Figure 3.9 shows the initial state of the model before applying the electrode voltage. Due to the residual stress in the membrane, the membrane is bent up which is studied in previous sections. From the same figure, the elevation of approximately 0.5 µm at the contact region can be easily seen. At a first glance, one can say that the expected pull-in voltage should be higher than the non-stressed case. However, the sides of the membrane are at lower position compared to the non-stressed case due to the bent up of the middle part. Therefore, a detailed FEM analysis is necessary in order to understand the electromechanical response of the RF-MEMS switch.

The electromechanical simulations are started using the stressed membrane at the initial state. Figure 3.10 shows the z-displacement of the membrane for different electrode voltages; 0, 28, 34 and 40 V. Pull-in of the membrane occurs approximately at 32 V, while 40 V electrode voltage provides a very stable contact.
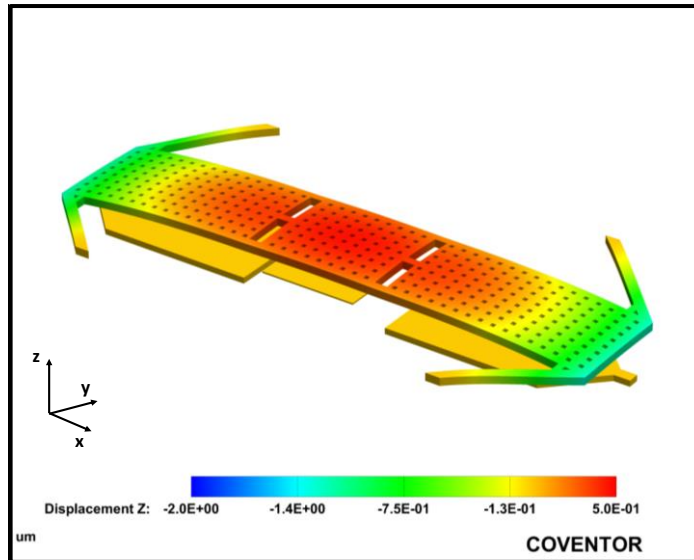


Figure 3.9 FEM model of the RF-MEMS switch after applying the residual stress values. It shows the initial case before applying an electrode voltage.
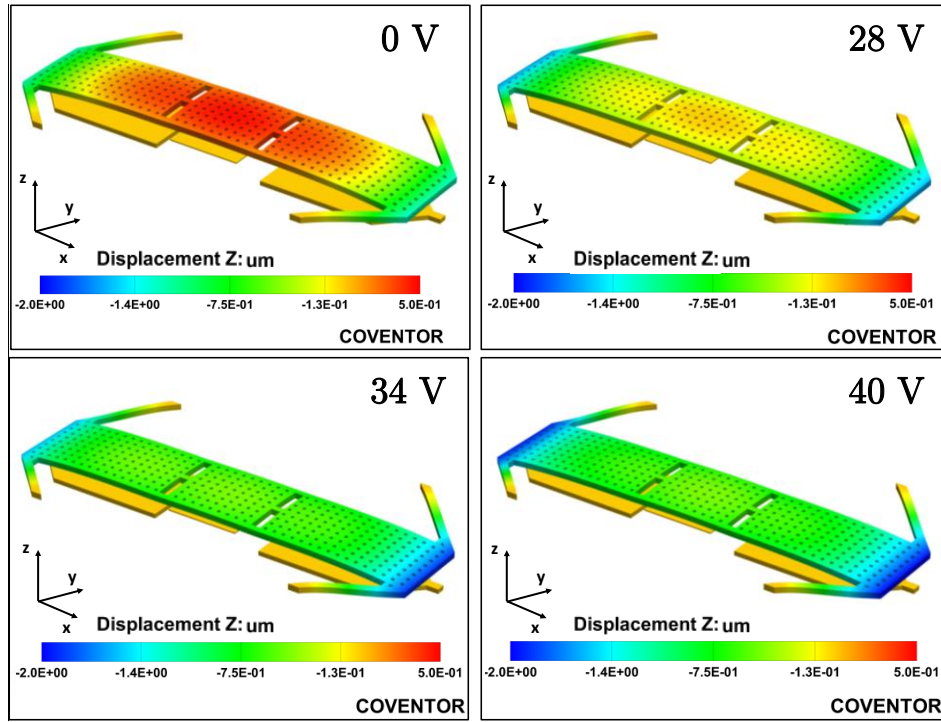
Figure 3.10 Steady-state FEM simulation results of the RF-MEMS switch under electrode voltages of: 0, 28, 34 and 40 V. Pull-in occurs at around 32 V.

As studied in section 2.4, the contact occurs only at four points due to the stressed membrane. This effect should also be seen during FEM simulations to be able to simulate the real contact capacitance. Figure 3.11 shows the close view of the contact when the membrane is actuated with 40 V of electrode voltage. Four contact points of the membrane with the contact pressure values of approximately 10 - 14 MPa can also be seen in Figure 3.11 (right).
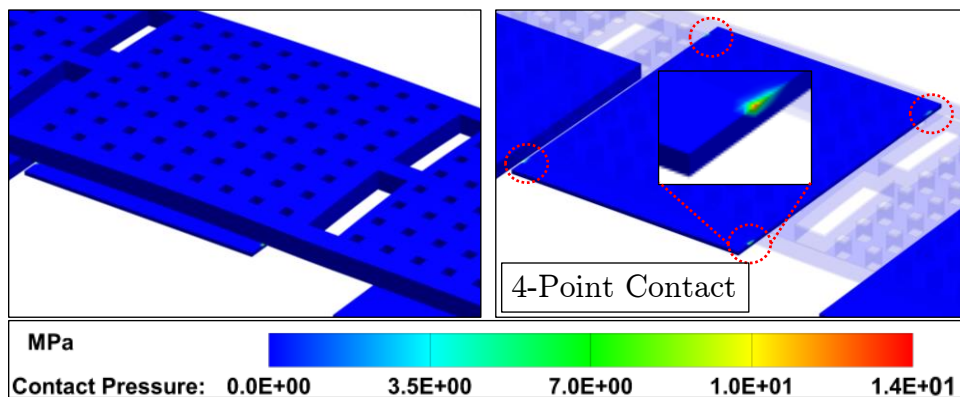


Figure 3.11 Close view of the contact region when 40 V electrode voltage is applied.

Figure 3.12 shows the simulation results of displacement and contact capacitance versus electrode voltage of the RF-MEMS switch. The pull-in occurs at around 32 V with a total displacement of approximately 1.1 µm at the contact region. The up-state capacitance is simulated as 20 fF whereas the down-state capacitance is approximately 120 fF which provides a capacitance ratio of 6.
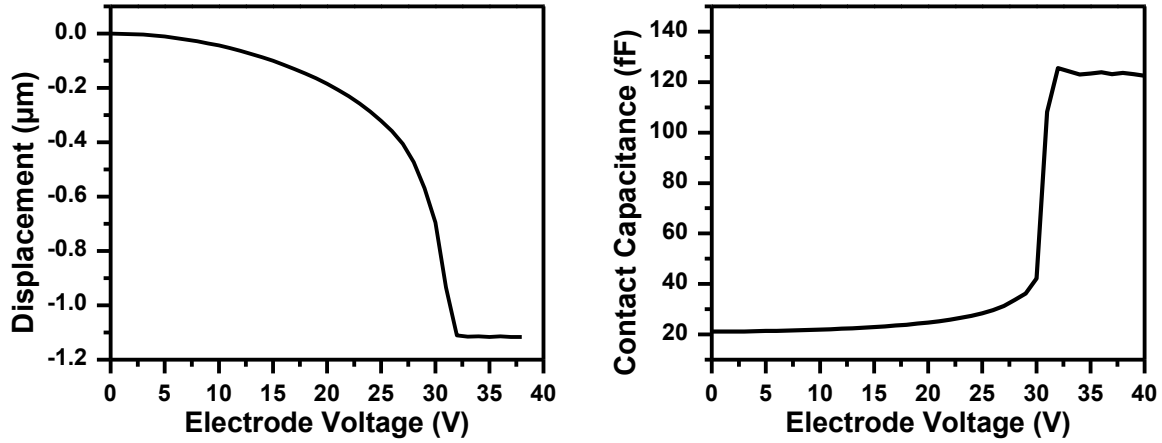


Figure 3.12 FEM simulation results of the RF-MEMS switch: Displacement versus electrode voltage (D-V) and capacitance versus electrode voltage (C-V).

## 3.3.2 Experimental Data: Low Frequency and Dynamic Measurements

The dynamic behavior of the switch is characterized by LDV to measure the total displacement and the dynamic response of the RF-MEMS switch. The low frequency electrical measurements are performed by an Agilent 4294A impedance analyzer to measure the on- and off-state capacitances.

LDV measures the velocity of the moving structures, while displacement data can be extracted by integrating the velocity over time. By scanning different points, it can be used to show the displacement of the entire membrane. Figure 3.13 shows an RF-MEMS switch under LDV measurement. The measurement point is shown as green while blue points are additional scanning points. A high voltage pulse of 40 V is applied at the time of 50 µs with duration of 500 µs. In a few microseconds the membrane goes down and forms the contact with a total displacement of 1.1 µm.
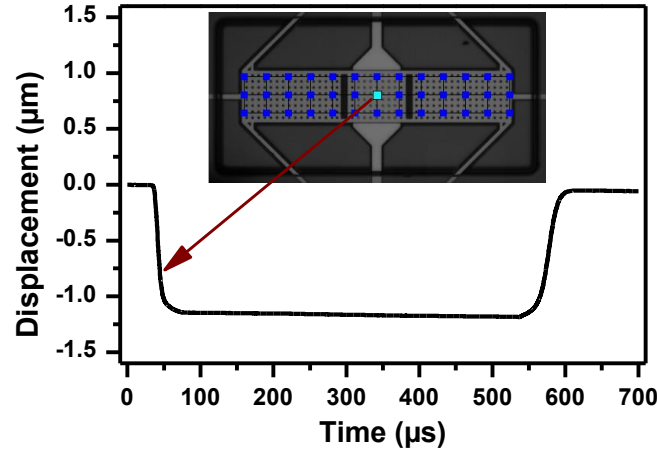
Figure 3.13 RF-MEMS switch under LDV measurement and the measurement result showing the displacement versus time.

To compare the FEM simulation results with the measurement results, electrode voltage is swept from 0 V to 40 V. Figure 3.14 shows the displacement of the membrane for different electrode voltages. The figure on the left hand side shows that the pull-in occurs at the voltage values between 30 and 34 V. The figure on the right hand side shows the comparison for simulation and measurement cases. A very good agreement is achieved between the simulated and the measured data using the extracted material parameters (section 3.2).
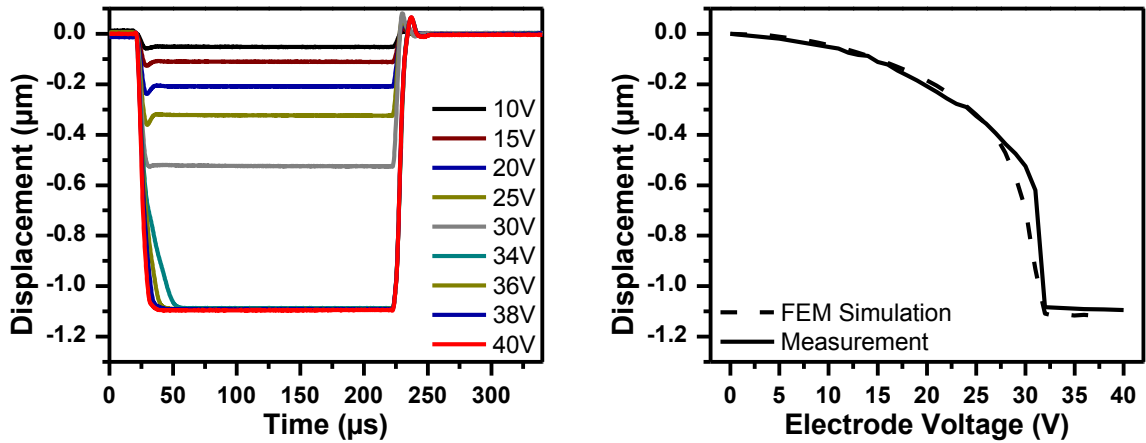


Figure 3.14 Measurement results of displacement versus time for different electrode voltages (left). Comparison of simulation and measurement cases (right).

Figure 3.15 shows the switch-on and -off times of the RF-MEMS switch for different electrode voltage cases. The switch-on time is decreased with increased electrode voltage as expected due to the higher electrostatic force. The switch-on time changes from 50 µs for the 34 V case to 10 µs for 40 V. Switch-off time is approximately 10 µs for all the cases since it is mainly defined by the spring constant of the movable membrane. Dynamic measurements using LDV technique are concluded with the extraction of the switch-on and -off responses of the RF-MEMS switch.
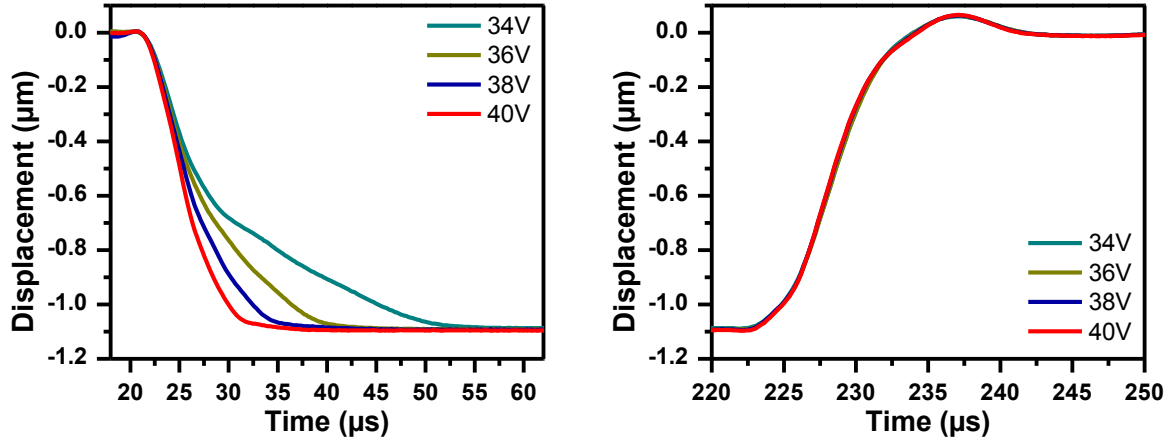


Figure 3.15 The switch-on (left) and -off (right) responses of the RF-MEMS switch for different electrode voltage actuation cases.

The low frequency response of the RF-MEMS switch is characterized by using an impedance analyzer. The contact capacitance of the RF-MEMS switch is measured with respect to the electrode voltage in order to extract the off- and on-state capacitances. The measurements are performed at 1 MHz and the total capacitance from the RF signal line to ground is measured. In order to acquire the pure contact capacitance, the additional parasitic capacitance from the RF signal line to ground is also measured using a separate de-embedding structure with removed membrane. Figure 3.16 shows the measured and the simulated contact capacitance versus electrode voltage. The contact capacitance is acquired by subtracting the parasitic capacitance from the total capacitance. The same figure also shows the good agreement between the simulation and the measurement results. The specific RF-MEMS switch provides approximately 20 fF off-state and 120 fF on-state capacitances, resulting in an on/off capacitance ratio of 6.
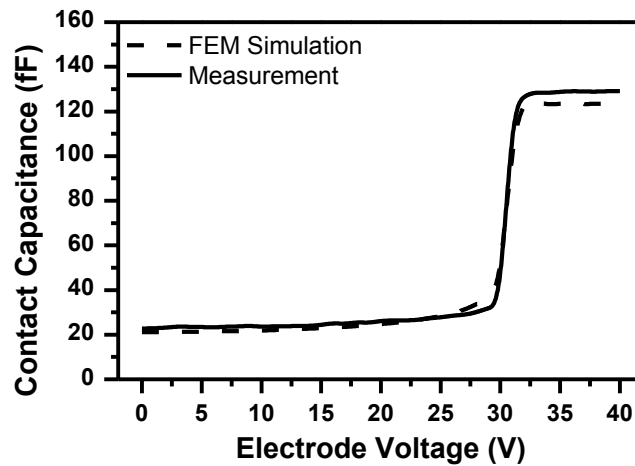
Figure 3.16 Simulation and measurement results for the contact capacitance versus electrode voltage of the RF-MEMS switch.

## 3.4 RF Modeling

The EM simulation domain is more mature than the electromechanical one by the help of powerful 2.5D or 3D EM solvers. The material properties required for the EM simulations are mostly well-known material parameters such as conductivity, dielectric constant and loss tangent. All these parameters can be found in the literature for various materials and do not significantly change with the process conditions. Additionally, these parameters can be easily measured and extracted using simple test structures. However, most of the EM simulators do not have an option to include the bending of different layers due to stress or surface roughness in order to calculate the contact capacitances. Furthermore, the MEMS devices are relatively large devices compared to the typical semiconductor devices. The large size of these devices has a significant effect at mm-wave frequencies. Therefore, a careful design methodology is used in order to understand the importance of different effects such as bending of suspended layers, non-flat contacts, and the effect of the small release-holes on the membrane. Some of these effects and the optimization of the RF-MEMS switch for mm-wave applications are detailed in next sections with a unique design methodology using the SONNET 2.5D EM solver [90].

### 3.4.1  EM Model of the RF-MEMS Switch

An RF-MEMS switch operating at 80 GHz is chosen for the EM setup in order to investigate the effect of different simulation cases. The simulations are performed using SONNET. The substrate file for EM simulation is defined in SONNET according to IHP's 0.25 μm SG25H1 BiCMOS process flow. Prior to the full switch model simulations, some approximations are done in order to simplify the model. Without any simplification, the simulation time of a single switch can take several hours which limits the optimization. Therefore, first of all the effect of the small release holes on the membrane is investigated. By omitting these holes, the number of mesh elements can be significantly reduced. In order to optimize the RF performance, the effect of the signal line width and GND ring are also investigated. After well understanding the different effects, the full RF-MEMS switch is simulated to extract the insertion loss and the isolation of the switch in up and down states, respectively. A simplified RLC model of the RF-MEMS switch is also developed to predict the high frequency behavior of the switch. Lastly, an inductive loading technique which allows tuning the frequency of maximum isolation of the switch from 30 to 100 GHz is studied.

- *Effect of the Release Holes: Model Simplification*

Although EM simulations provide very accurate solutions for the high frequency response, due to the large number of mesh elements, in some cases very long simulation times are required. The maximum solution frequency, the smallest feature size and the overall dimension of the model strongly affect the total number of mesh elements. The mentioned problems occur in mm-wave RF-MEMS switch structures since the frequency of interest is high, the minimum feature size is less than a micron and the dimensions of the whole structure is few hundred of microns. One of the main reasons which increases the number of mesh elements are the small release-holes on the membrane. These holes need to be taken into account during mechanical simulations because the effect of the holes on the stress gradient of the movable membrane is significant and cannot be neglected. However, considering the fringing effects at high frequencies, the effect of the holes at high frequencies needs to be investigated and if the results are not affected considerably, they should be omitted. Such simplification significantly helps to decrease the simulation time, hence allows doing several simulations/iterations in a short time.

In order to clarify the effect of the release-holes on the membrane, three different cases of switch are simulated. In these three cases, all the parts of the switch are identical except the movable membrane. In the first case, no release-holes are used for both on the sides and on the contact area of the membrane. Second one includes release-holes only on the contact area and the third one includes release-holes both on the sides and on the contact area. All these three cases are presented in Figure 3.17.
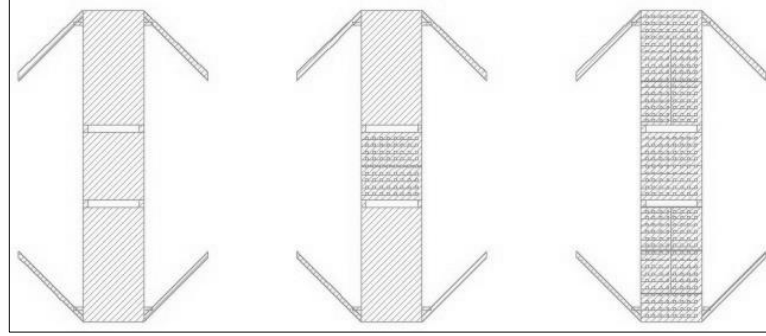


Figure 3.17 The view of the membrane for different membrane cases: Without holes (left), with holes only at the contact area (middle) and with holes at contact and side areas (right).

EM simulations for all three cases are performed and the insertion loss and the return loss parameters are extracted. The contact region is more sensitive than the sides since the gap between the membrane and the signal line is smaller (~1 μm) than the gap between the membrane and the electrode (~3 μm). However, it is not easy to predict the fringing effect since such coupling between the membrane and the signal line both affect the insertion loss and the return loss of the switch. Figure 3.18 shows the comparison between these three configurations for both insertion loss and return loss when the membrane is in up-state. It can be easily seen that the first case gives very different results than the second and the third case, especially considering the input impedance. These results also show that the input matching is very sensitive to the up-state capacitance. However, the second and the third cases provide very similar results, showing the minor effect of the capacitance from the membrane to high voltage electrodes at the sides of the membrane. The simulation time of second case is approximately four times shorter than the third case and two times longer than the first case. Therefore, the second case, which includes release-holes only in the contact region, is selected to do further optimizations.
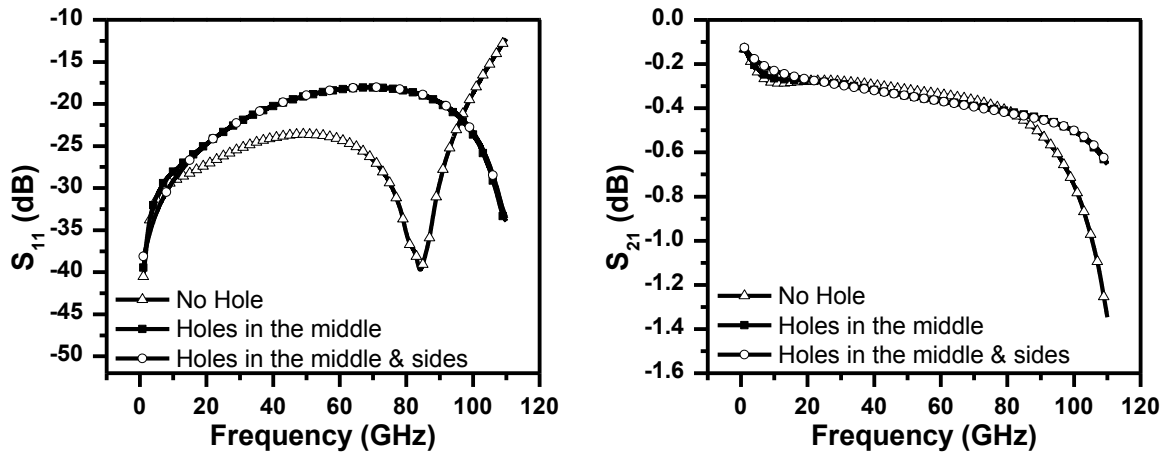
Figure 3.18 EM Simulation results of the switch for up-state: Return loss (left) and insertion loss (right) for three different cases at up-state.

- *Signal Line Optimization*

After finalizing the simplification of the model, the EM simulations are done in order to optimize the high frequency response of the switch. Insertion loss, return loss and isolation are the main interesting parameters of the switch at mm-wave frequencies. The total loss of the switch mainly occurs due to the resistive loss and the reflection loss considering the very small effect of radiation loss. Resistive loss mainly comes from the limited conductivity of the aluminum signal line and can only be decreased by thicker and wider signal lines. However, the line should also be matched to 50 $\Omega$ to minimize the reflection loss. Therefore, the most important parameter to minimize the reflection loss is the width of the signal line, assuming that the contact region of the signal line needs to be kept constant to provide a constant contact capacitance and the stable mechanical contact formation (Figure 3.19). Similar to the contact region, the total length of the signal line is also kept constant.



Figure 3.19 Generic view of the signal line of RF-MEMS switch and the design parameter: Width of the RF signal line, "w".

Figure 3.20 shows the EM simulation results of $S_{21}$ versus signal line width for the selected RF-MEMS switch at 80 GHz. Due to the mismatch and resistive losses, the insertion loss of the switch changes between 0.8 dB to 0.45 dB for different signal line widths. The minimum insertion loss is achieved with a signal line width of 30 μm for the specific switch working at 80 GHz.
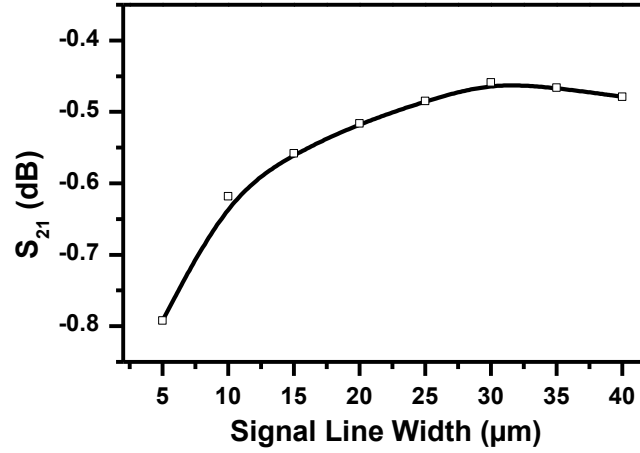


Figure 3.20 EM simulation results of $S_{21}$ versus signal line width for 80 GHz RF-MEMS Switch at up-state. The lowest insertion loss is achieved using a signal line width of 30 μm.

- *GND Ring Optimization*

RF grounding of high frequency circuits is always one of the main critical points for the circuit designers and needs a special attention. Underestimated parasitic components coming in between circuit ground node and the real ground always create problems and mismatch between simulations and measurements. Therefore, mm-wave circuits need a very well defined ground plane to operate properly. In addition, the size of the RF-MEMS switch is one of the main limitations at high frequencies because the parasitic components have a significant effect on the switch performance.

In order to obtain the best RF behavior, the RF-MEMS switch structure needs a ground ring surrounding it since the movable membrane has four arms. The RF-MEMS switch needs a proper RF ground at the end of all four arms which is realized using two half-rings, as shown in Figure 3.21. These two half-rings should be well grounded and should also provide the same RF ground to the four arms of the switch.
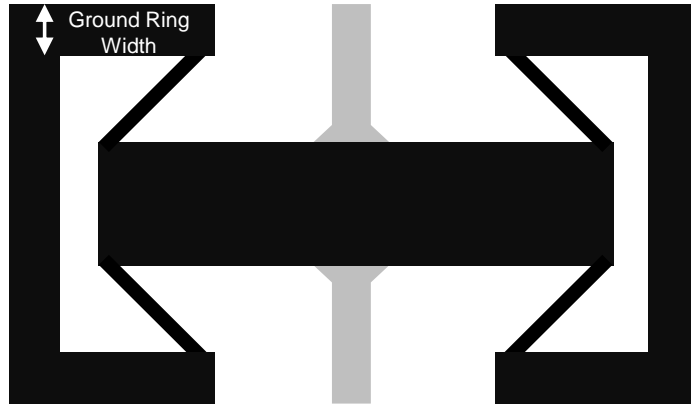
Figure 3.21 Generic view of the ground ring of RF-MEMS switch and the design parameter: "Ground Ring Width".

In contrast to III-V technologies, CMOS/BiCMOS technologies have lower resistive substrates, e.g., 10 to 100 $\Omega$-cm. The real RF ground of the circuit mostly comes from the top of the chip via bondwires or solder-bumps. This RF ground is shorted to the silicon substrate over metallization layers, vias between metals and contact via from lowest metal to highly doped silicon substrate region. Therefore, the silicon surface can be assumed as the ground level but with limited conductivity. As a result, the best way to define the RF ground of the switch is connecting the ground half-rings to the real RF ground of the circuit and to the silicon substrate through contact vias.

In order to realize the aforementioned concept, the two half-rings are realized by stacking all available 5 metal layers using vias. Furthermore, these half-rings are shorted to the highly doped region of the silicon substrate over contact vias. In fact, the stacked ring structure together with membrane at M3 form the RF ground of switch. As can be clearly seen on Figure 3.21, the size of the ring is comparable with the size of the switch which shows a potential effect of the ring on the RF performance of the RF-MEMS switch. It is also noted that the big size of the ground ring behaves like distributed impedance considering the high frequency of operation. Therefore, the influence of the ground ring on RF performance of the switch also needs to be investigated.

The width of the ground ring is varied from 10 to 25 μm by keeping the inner size constant. The insertion loss and isolation performances are compared and given in Figure 3.22.
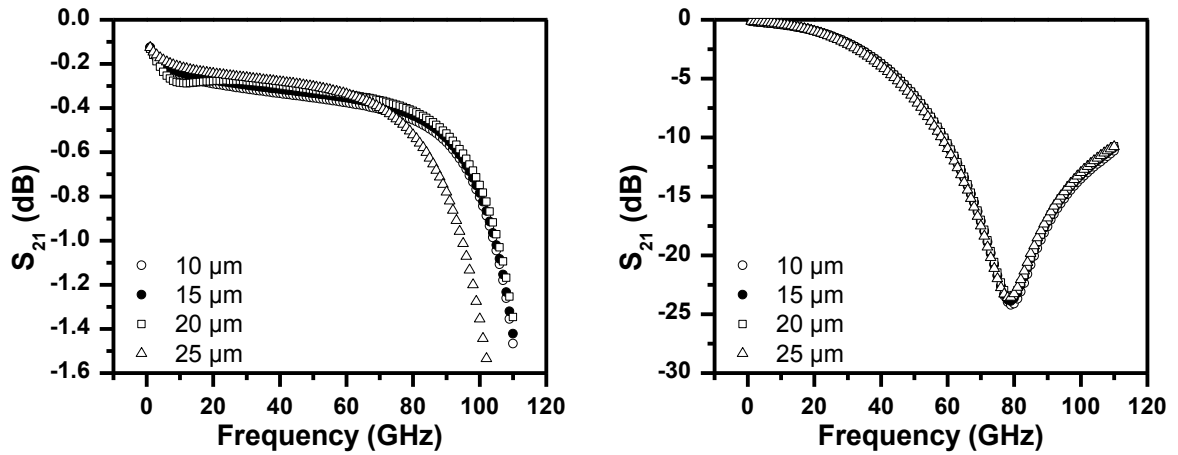
Figure 3.22 Insertion loss at up-state (left) and isolation at down-state (right) of RF-MEMS switch for different ground ring widths. The best performance is achieved width a ground ring width of 20 μm.

From Figure 3.22, it can be clearly seen that the ground ring has a very small effect on isolation as expected because in down state, the RF signal is shorted to the ground and ground ring is considered as the part of the resonance in down-state. However, the width of the ground ring has a significant effect on insertion loss at up-state, especially for higher frequencies. An optimum value of 20 μm ring width is chosen for the further optimizations of the RF-MEMS switch.

- *RF-MEMS Switch Simulation*

After simplifying and optimizing the EM model of the RF-MEMS switch, the entire structure is simulated using the SONNET EM solver. The main difficulty of simulating RF-MEMS structures is the process dependent contact parameters. RF-MEMS devices are significantly affected by the process dependent parameters such as residual stresses or surface roughness. The down-state capacitance of a capacitive type RF-MEMS switch is mainly related to the residual stress of the movable membrane. Likewise, the up-state capacitance is also varying with the initial gap between the signal line and the membrane which is again related to the bending of the membrane. Therefore, the RF behavior of the switch is very sensitive to the contact parameters for both up and down states.

Accurate simulation of the air capacitance in the down-state is not possible with planar EM solvers. Furthermore, the simulation of the air-gap capacitance using FEM solvers is also not straightforward and strongly depends on the stress gradient of the membrane. An accurate switch model needs precise contact parameters, especially at down-state. The simulated contact capacitances of 20 fF for up-state and 120 fF for down-state are used to model the contact region. It is noted that the capacitance values achieved by FEM simulations are also verified with the measured results before inserting into the EM simulations. The "via-port" option in SONNET is very helpful in using the RLC based contact model between M2 and M3. Suspended membrane, RF signal line and high voltage electrodes are simulated together in a single EM model, and S-parameter files are extracted. The extracted S-parameter files are revised with the extracted contact model. The RLC based contact model includes only contact air capacitance for the up-state and contact air capacitance, contact inductance as well as the contact resistance for the down-state. Figure 3.23 shows the EM simulation setup and the contact parameters used in the final model.
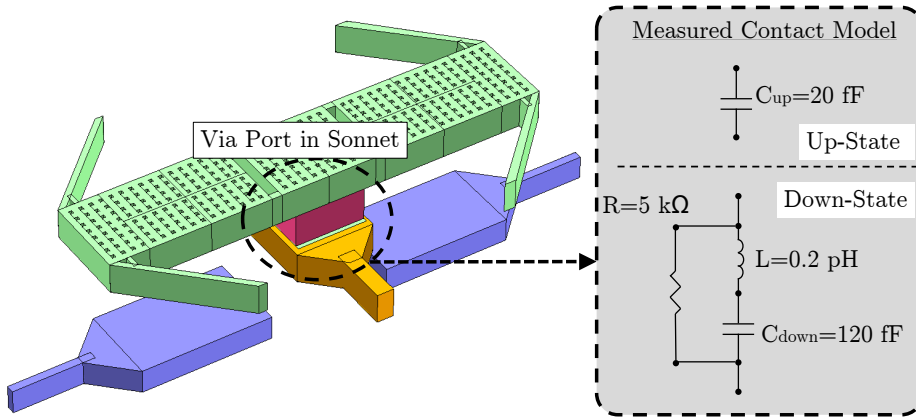


Figure 3.23 Simulation setup in Sonnet and the lumped element contact model for up and down states.

After including the extracted contact capacitance parameters, the S-parameter simulations of the RF-MEMS switch are performed. The return loss, insertion loss and the isolation parameters are given in Figure 3.24. The simulation results show that the switch provides an insertion loss of less than 1 dB and return loss lower than 20 dB in up-state (left). The isolation is simulated as better than 20 dB at the target frequency of 80 GHz in down-state for the specific switch under optimization (right).
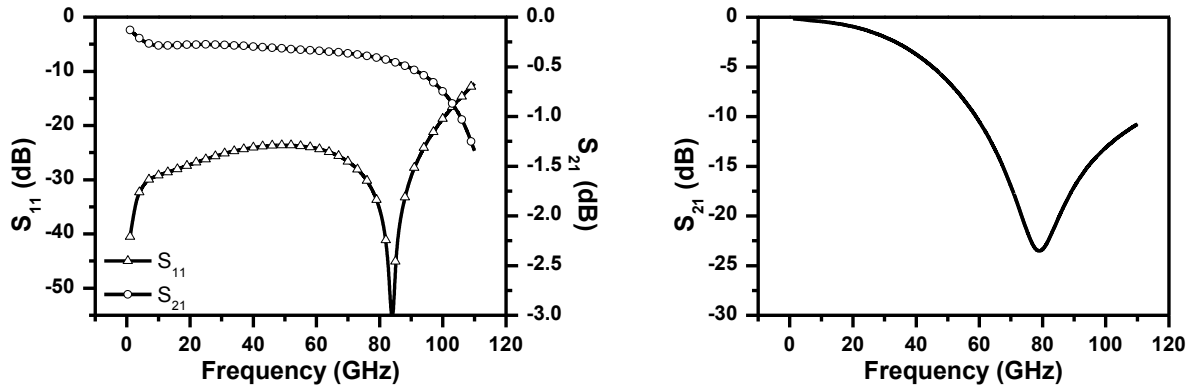
Figure 3.24 Simulated S-parameter of the switch: $S_{11}$ and $S_{21}$ at up-state (left) and $S_{21}$ at down-state (right).

The EM simulations in this section are used as the first approximations for the initial fabrication runs. It shows an EM optimization flow of a specific 80 GHz RF-MEMS switch. Since it is difficult to simulate all the effects in advance, a rough estimation is necessary before starting the fabrication. Therefore, these simulations are taken as the initial simulations and the optimization of the RF-MEMS switch is continued with back and forth measurements and simulations using the developed EM model in order to achieve the best performance parameters. However, the measurement results in the next sections show that the estimated values provide very similar results to the measurements, and they are taken as the final design parameters.

-   *RLC Modeling of the RF-MEMS Switch*

Although EM simulations are mandatory for the design and process optimization of RF-MEMS devices and provide very accurate data, the extracted format from such simulators is typically limited with S-parameter data or behavioral SPICE (Simulation Program with Integrated Circuit Emphasis) models. Such data are useful for high frequency simulations but mostly not well suited for fast DC or low frequency simulations. A lumped-element model based on RLC components is preferred for DC simulations, especially considering the sensitive biasing conditions of the RF-MEMS switch in order to prevent self-biasing or latching effects. Furthermore, such lumped-element models are very convenient for system level simulations considering the simulation speed.

Figure 3.25 shows the lumped-element model of the switch for up and down states. Similar to EM modeling in the previous section, the contact model is simulated using extracted contact parameters for an RF-MEMS switch optimized for 94 GHz. The signal line is simulated using a lossy transmission line model (TL1 and TL2) while the membrane is modeled as a lossy inductor ($L_1$ and $L_2$). $C_1$ and $C_2$ are the parasitic capacitances between the movable membrane and the high voltage electrodes. $L_1$ and $L_2$ are the inductances of the narrow arms while $L_3$ and $L_4$ are the inductances from the HV electrodes to RF ground. The transmission line models used to model the signal line can be easily replaced by an RLC equivalent one, if necessary.
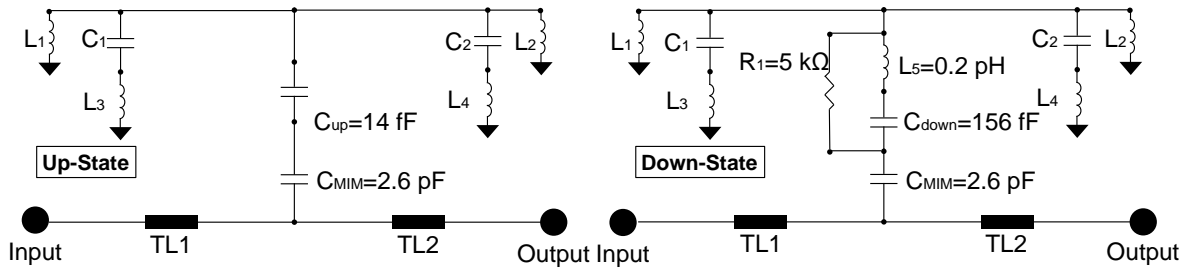


Figure 3.25 Lumped-element models of the RF-MEMS switch for up-state (left) and down-state (right).

Figure 3.26 shows the comparison between the EM simulated and the lumped-element models of an RF-MEMS switch optimized for 94 GHz. The lumped-element model gives very similar results to the EM model, however, the high frequency resonance in up-state cannot be observed. This effect is associated with the effect of the substrate which can be taken into account in EM but not in the lumped-element model. The substrate effect has less influence in down-state because the main resonance is defined by the contact capacitance and the capacitance between electrode and membrane. Since the weak resonance occurs in up-state outside of the band of interest, no further optimization is done for the up-state.

It is noted that two main issues during optimizations which help to achieve such accurate results are the well-defined contact parameters and taking the coupling capacitance between membrane and electrode into account ($C_1$ and $C_2$). Although the latter one is not so important for low frequencies, it has a significant effect at high frequencies, especially in down-state due to the less distance between the membrane and the high voltage electrode.
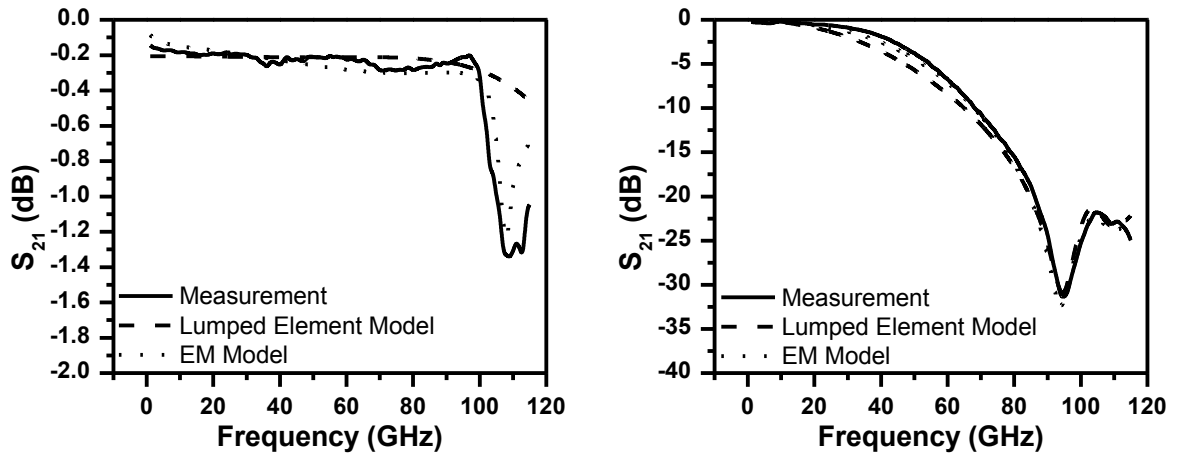
Figure 3.26 Comparison of the measurement, EM simulated and the lumped-element simulated models: Insertion loss at up-state (left) and isolation at down-state (right).

- *Further Optimizations and Inductive Loading for Frequency Tuning*

The last section of the RF modeling part is the final optimization to improve the performance and the frequency tuning of the RF-MEMS switch for different frequency bands. RF-MEMS switches can be used for many different mm-wave applications such as satellite and space communication (30 - 50 GHz), E-band communication (60 - 90 GHz), and imaging systems (94 - 140 GHz). All these different band applications show the need for RF-MEMS switches in different frequency bands.

Operation at different frequency bands can be achieved by tuning the resonance frequency of the capacitive switch at down-state. The contact capacitance and the membrane inductance form the main series resonance frequency of the switch at down-state and the highest isolation is achieved at the resonance frequency, as follows:

$$2\pi f = \frac{1}{\sqrt{L*C}} \qquad (3.2)$$

The typical method in use for frequency tuning of capacitive type RF-MEMS switches is changing the contact capacitance, which, however, leads to a change in the mechanics of the system [91]. There are two disadvantages of this method. Firstly, optimizing the mechanics for any new frequency band needs additional effort and is very time consuming. Secondly, every change in the system mechanics requires repetitions of reliability and qualification tests, making the development cost intensive.

In contrast to the straightforward approaches, an integrated inductive loading technique is used to tune the operating frequency of the BiCMOS embedded, capacitive RF-MEMS switch. Figure 3.27 illustrates the concept of the inductive loading technique, which is applied to the developed BiCMOS embedded RF-MEMS switch.
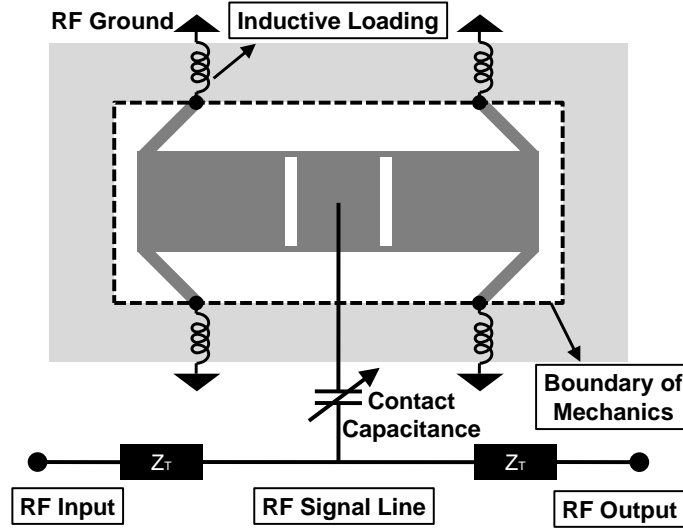


Figure 3.27 Conceptual figure of inductive loading technique. Additional inductors are outside of the mechanical boundary (in BEOL oxide) and have no effect on the mechanics of the movable membrane [92].

The additional inductors, realized in the BiCMOS BEOL, are added between the movable membrane and the RF ground ring in order to change the total inductance to ground. It results in a change of switch resonance frequency without having an effect on the switch mechanics. Figure 3.28 shows the realized switches for four different frequency bands with the same movable membrane but different inductive loads. By the help of the developed technique, the center frequency of the switch at down-state can be tuned from 30 to 100 GHz.

Since one of the most important performance parameter of the switch is the insertion loss, further optimization to minimize the insertion loss is performed. One of the easiest ways to decrease the insertion loss is decreasing the resistive loss. Therefore, parts of the signal line which are out of the contact region are formed by the stack of M2 and M3 (Figure 3.29, top).
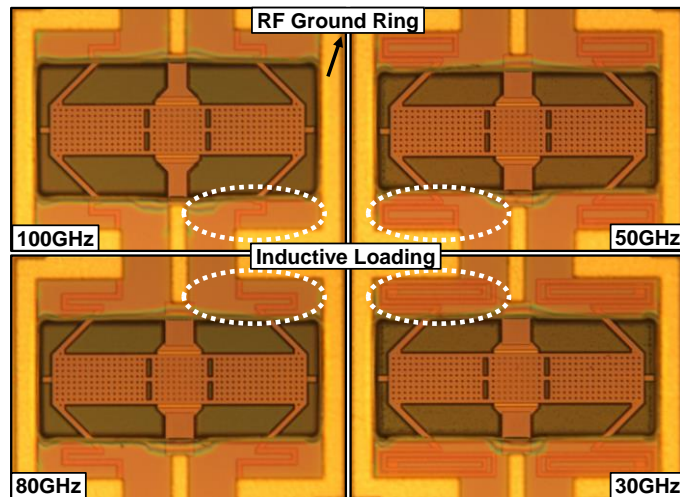
Figure 3.28 Microphotographs of RF-MEMS switches for four different frequencies: 100, 80, 50, and 30 GHz [92].

The maximum isolation is mainly limited by the Q-factor of the additional inductors. Therefore, the inductor spirals are formed by stacking M3 and M4 layers to maximize the Q-factor (Figure 3.29, bottom). Using the mentioned technique, the insertion loss and the isolation of the switch is significantly improved. The comparison of different cases is given with experimental results in the next section.
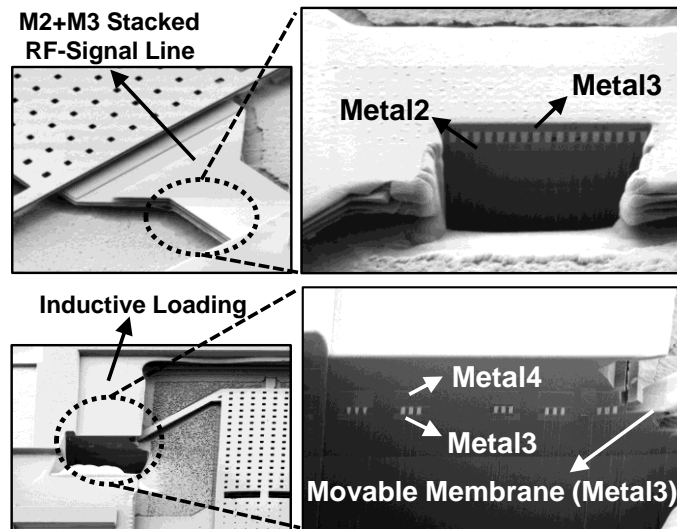


Figure 3.29 Signal line and additional inductor: M2+M3 stacked layer is used as signal line except contact region (top). Additional inductors are realized using the M3+M4 stack to increase the Q-factor of the inductor (bottom) [92].

## 3.4.2 Experimental Data: S-Parameter Measurements

The high frequency characterization of the switch is done by measuring the S-parameter response both in up and down states. An Agilent 8510 network analyzer is used to measure the S-parameters up to 110 GHz. Since the interested frequency band is high, the effect of the measurement pads is significant. Therefore, open-short de-embedding technique is used in order to remove the shunt (open de-embedding) and series (short de-embedding) components of the measurement pads. An example of an RF-MEMS switch with "open" and "short" de-embedding structures is given in Figure 3.30. The S-parameter results of the switch are shown in Figure 3.31 for not de-embedded, only open de-embedded and open/short de-embedded cases. As it can be seen from Figure 3.31, the de-embedded insertion loss parameter significantly changes.
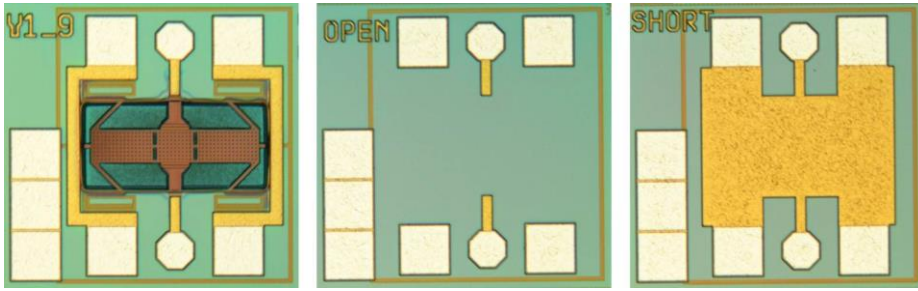


Figure 3.30 RF-MEMS switch with open and short de-embedding test structures.
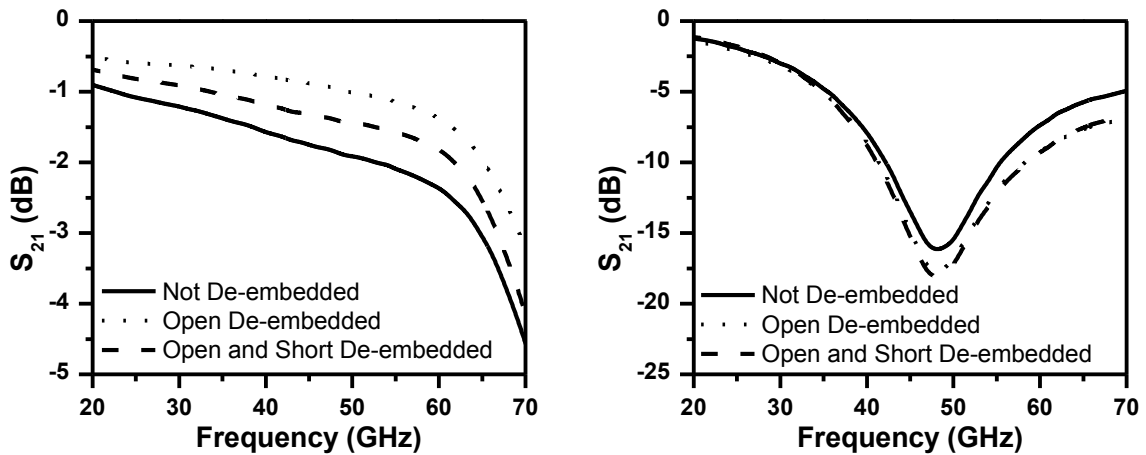


Figure 3.31 Insertion loss (left) and isolation (right) of a 50 GHz RF-MEMS switch for not de-embedded, only open de-embedded and open/short de-embedded cases.

Figure 3.32 shows an open/short de-embedded measurement results of an 80 GHz optimized RF-MEMS switch together with the simulation results achieved in the previous section for $S_{21}$ and $S_{11}$. Although the simulation results are very similar to the measured ones, there is obviously a mismatch above 80 GHz. This mismatch is correlated to the substrate effects which are difficult to simulate since they strongly depend on the wafer thickness and relative permittivity of the silicon at these frequencies which is known to be changing with increasing frequency. Better optimizations can be done at higher frequencies using full 3D FEM solvers to see the effect of the substrate.
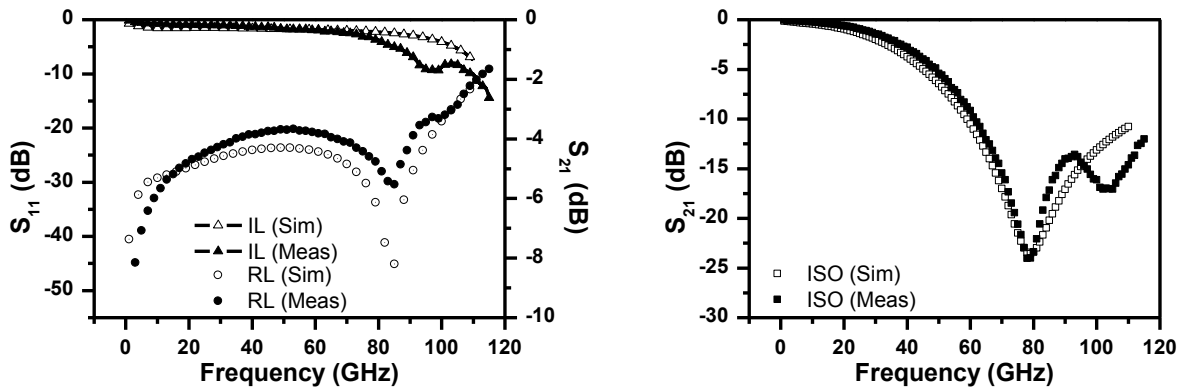


Figure 3.32 S-parameter measurement and simulation results of 80 GHz RF-MEMS switch for up (left) and down (right) states.

As explained in the previous section, the switch is optimized for different frequency bands starting from 30 GHz up to 100 GHz. Figure 3.33 shows the measured performance parameters of the RF-MEMS switches optimized for 30, 50, 80 and 100 GHz, respectively. The techniques to improve the performance explained in previous sections are useful for all different types of RF-MEMS switches. The comparisons of the results with and without applying these techniques are also given in Figure 3.33. After applying the aforementioned techniques, the insertion loss can be kept below 0.25 dB, while the isolation is better than 20 dB at all targeted frequencies. The lowest insertion losses of all investigated RF signal line variants are achieved for a signal line width of 30 µm, except at 100 GHz. For this case, a width of 20 µm provides the best performance. Figure 3.33 also demonstrates that increasing Q-factor of the inductive loads by metal layer stacking improves the isolation by more than 5 dB in all cases.
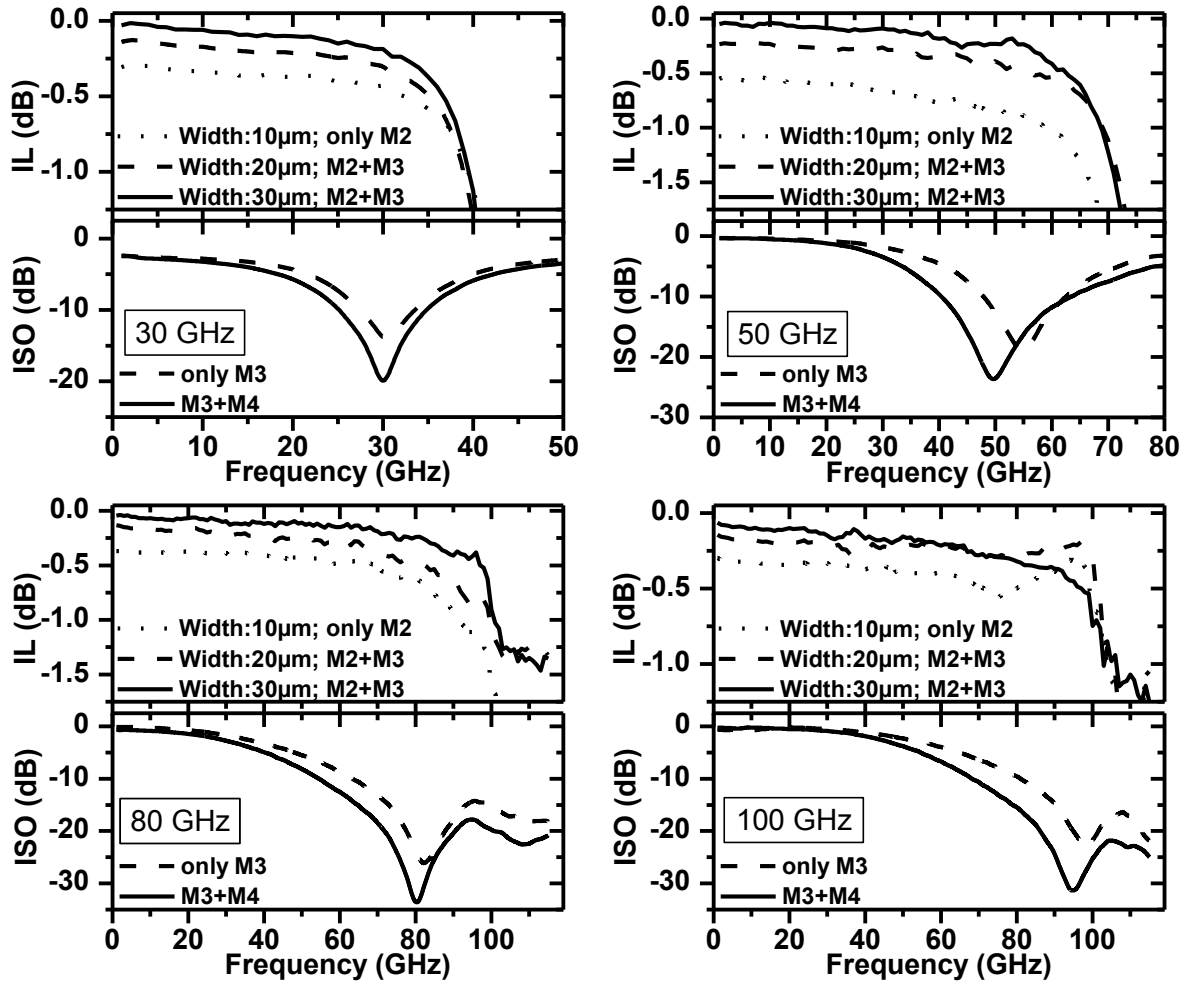
Figure 3.33 Measured (de-embedded) insertion loss and isolation of RF-MEMS switches with different signal line conditions and different inductor metal stacks [92].

## 3.5 Conclusion

In Chapter 3, the modeling and characterization of the RF-MEMS switch has been given. The process dependent material parameters such as Young's modulus and residual stress have been extracted as an input parameter for electromechanical FEM simulations. Electromechanical modeling has been followed by the electromagnetic modeling which is one of the most important domains since the RF-MEMS switch is expected to operate at mm-wave frequencies. Initial model simplifications have been done in order to decrease the simulation time. The simplified model has been

optimized to get the best RF performance at desired frequency. A special design methodology has been created which uses the measured contact lumped element model in order to accurately simulate the entire structure. The simulated results have been compared with the experimental data after every section.

The fabrication of the RF-MEMS devices in BiCMOS process is costly and one of the best ways to decrease the cost is the accurate modeling of the devices before the fabrication. However, if the modeling period takes too long, time to commercialization can significantly increase. Therefore, a clear and effective modeling strategy is needed in order to minimize the cost of the development and shorten the time to market.

The modeling strategy is strongly related to the application. For the specific application in this thesis, the requirements are more challenging on the RF than the electrical or mechanical side because the expected operating frequency is very high and the performance figures are very challenging. However, the application does not require high power handling, which makes the electromechanical design simpler. Therefore, the initial step of modeling strategy should be the definition of the most challenging domains with respect to the applications requirements and choosing the appropriate FEM solver to model the desired physical effects.

Electromechanical simulations should be considered together with the material properties extraction. The electromechanical simulations should start with the material characterization and extraction of the critical material properties. If the correct geometry and the appropriate physical models are used, electromechanical FEM simulations are very straightforward and can provide accurate solutions. In principle, the well agreement between the simulations and the measurement are based on how good the material properties are extracted and inserted to the simulator.

Regarding EM simulations, the RF-MEMS structures have some challenges such air cavities, under-etching due to the isotropic etch processes and bending of layers due to residual stress. These effects can significantly change the final RF response of the switch; therefore should be taken into account. With respect to the importance of different effects, an appropriate choice between 2.5D or 3D EM solver should be done.

To conclude Chapter 3, modeling of the RF-MEMS devices has also significant effect on the final cost and development time of the device. It should be done by continues back and forth iterations between modeling and fabrication. A perfect match between the initial model and the fabricated device is almost impossible. However, the best performance RF-MEMS devices have always strong and accurate models behind which could take many years to develop and stabilize.

# 4 Packaging

## 4.1 Introduction

In the last years, the commercialization of RF-MEMS is mainly hampered by two critical factors; namely, the appropriate packaging technology and reliability problems. Similar to all other electronic components, the package has a great importance on both the performance and the final cost of the device. However, packaging of RF-MEMS devices is more complex than that of the other electronic components since there is a need for a cavity inside the package and higher degree of hermeticity is required. Moreover, the type of package has also a significant effect on long term reliability of RF-MEMS devices. A good RF-MEMS package should not only provide the interface to the next level, but needs to be also cost effective. Furthermore, it should be preferably fabricated using wafer level processes to increase the throughput since thousands of RF-MEMS devices can be fabricated on a single 8-inch wafer.

Several methods have been proposed and demonstrated in the literature to package RF-MEMS devices such as cap-to-wafer packaging, wafer-to-wafer packaging or wafer level encapsulation [93, 94, 95]. Some of these methods use polyimide based materials for bonding and some of them use hermetic sealing by fusion, anodic, eutectic or thermal compression bonding techniques. At first look, it seems that there are many solutions for packaging; however, high performance and packaged RF-MEMS devices can only be realized by considering the packaging process in advance, preferably before or during the design phase of the RF-MEMS device. Similar to many microwave components, most of the RF-MEMS devices provide very high performance without a package but significant performance degradation occurs after the packaging process.

Numerous limitations have been pronounced regarding the packaging processes. The first and the most crucial question is the requirement of hermeticity. Commonly, the RF-MEMS community claims that hermetic package is necessary for all kind of RF-MEMS devices, to be on the safe side. Using hermetic package is the most appropriate environment for RF-MEMS devices against humidity, which can be considered as the main reason for the failure of capacitive type RF-MEMS switches. However, depending

on the contact type (resistive or capacitive), RF-MEMS devices may show very different requirements.

For commercial RF-MEMS products, different packaging approaches are used. For instance WiSpry is using a wafer level encapsulation technique to release the MEMS device through small holes which are then filled and closed in the process flow, under a controllable pressure environment [96]. This approach provides very low loss and cost effective packaging solution with a hermetic package environment. A relatively more expensive wafer-level capping process is being used by Radant in order to achieve a hermetic package [97]. Another example, which is also being commercialized, is from MEMtronics [98]. MEMtronics uses a unique packaging process which provides non-hermetic wafer level micro-encapsulation using BCB spin-on process. This process has several advantages such as a small and thin package, no additional wafer bonding requirements and low package parasitics. The reliability tests of this device with non-hermetic BCB package have shown a very high performance which proves fully hermetic packaging is not mandatory for all the MEMS devices [99, 100]. Lastly, an extensive study about the packaging of RF-MEMS devices has been done in another EU supported project, called MEMSPACK [101]. Many different approaches for RF-MEMS packaging have been tested in MEMSPACK.

In this thesis, hermetic package is not considered as the first choice because the interested frequency band of the RF-MEMS switches is quite high. It is also well known that the degradation of the performance due to hermetic packages is more significant at higher frequencies. Furthermore, most of the hermetic packages need high process temperatures for final bonding steps which are not compatible with the CMOS processes due to the temperature budget of less than ~400 °C of aluminum BEOL. Two different approaches are developed to package the developed RF-MEMS switch. The first approach uses a cap-to-wafer process and provides a non-hermetic package. Due to the basic limitations of the cap-to-wafer packaging process, a wafer-to-wafer non-hermetic packaging process is developed and applied to the same RF-MEMS devices, as the second packaging approach.

In Chapter 4, firstly the limitations of the thermal budget of packaging process are investigated due to the significant effect on the performance of BiCMOS devices. By using the achieved results, two different packaging processes are developed and detailed in sections 4.3 and 4.4. Section 4.5 concludes the packaging chapter. All the packaging process developments under Chapter 4 are done together with Fraunhofer IZM, Berlin.

## 4.2  Definition of Thermal Conditions for the Packaging Process

Before packaging an RF-MEMS switch, the maximum process temperature not yet affecting the behavior of the switch should be investigated. Common packaging technologies require process temperatures in the range of 200 - 450 °C [102]. Therefore significant thermo-mechanical stress is induced after these high temperature processes. Not only the mismatch of thermal expansion coefficients but also the residual stress and the stress relaxation need to be considered. High temperature post-processing steps can affect the performance of RF-MEMS devices and either improve or deteriorate the system performance.

In [103], it is shown that stress relaxation of aluminum thin films with a thickness of 205 nm already starts at low annealing temperatures of 50-100 °C and strongly depend on the annealing time. The stress relaxation rate is sensitive to the metal thickness and thinner metal layers show a higher stress relaxation rate. In [103], it is also shown that relatively thick metal layers with a thickness of 1 µm show stress relaxation at 150°C. Due to the high stress sensitivity of the BiCMOS embedded switch, stress relaxation during packaging can significantly influence the switch performance; hence needs to be carefully analyzed.

To model the effect of a high temperature stress, non-packaged RF-MEMS switch samples are heated up from room temperature to the maximum temperature of test and kept at this temperature for 20 minutes. This long time period can be required to package several switches with caps on a full 8-inch wafer. After cooling down, the samples are allowed to settle enough to ensure that the stress relaxation process is finished and static deformation of the membrane is achieved. In Figure 4.1, the off and on state capacitances for six stress cases for six different stress temperatures are shown. It is noted that all the measurements are done at room temperature. Up to 300 °C, the up-state capacitance ($C_{off}$) slightly increases. At 350 °C, it increases from 13 fF to 36 fF [104]. Compared to $C_{off}$, $C_{on}$ is constantly increasing over the temperature with a highest change of 25 % at 350 °C. Stress relaxation changes the membrane shape; therefore the formation of the contact differs. This leads to an increased on-state capacitance.
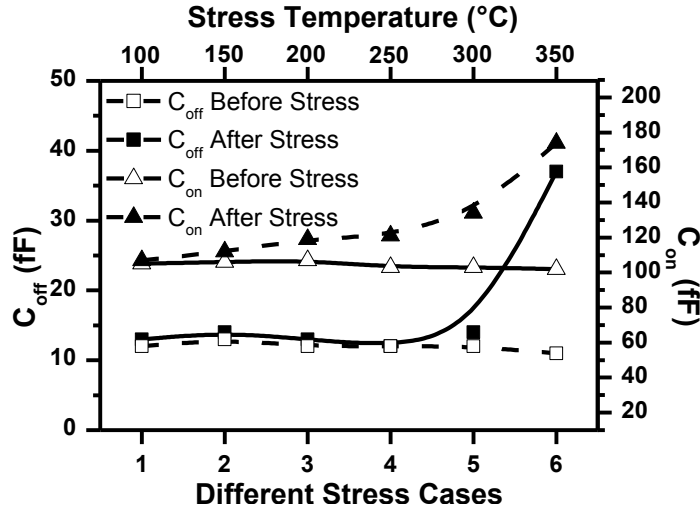
Figure 4.1 Change of up-state ($C_{off}$) and down-state ($C_{on}$) capacitances with respect to different temperature stress [104]. All the measurements are done at room temperature.

To better understand the increase of $C_{off}$ after annealing at 350 °C, the mechanical movement of the switch is analyzed by LDV measurements (Figure 4.2). The initial distance between membrane and contact region in non-actuated state can be estimated by the maximum displacement. Before annealing the maximum displacement is measured as 1.3 µm while after annealing, it decreases to 400 nm. This indicates that stress relaxation occurs and the effective residual stress of the M3 layer changes.
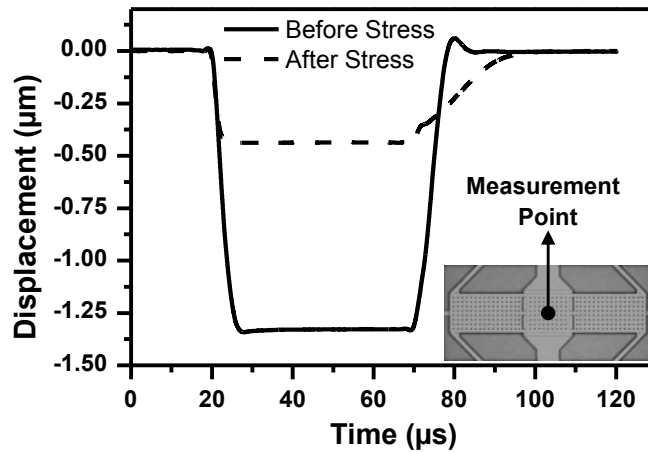


Figure 4.2 Displacement versus time response; before and after stressing at 350 °C [104].

In Figure 4.3, the calculated on/off state capacitance ratio is illustrated for the same six different stress cases. Up to 200°C, the variation of capacitance ratio is not significant. At 250 °C, the capacitance ratio can be improved from 8.5 to 10.1. At 350 °C, the capacitance ratio reduces approximately by 50 %, from 9.3 to 4.7 [104]. As a result, high temperature stress of the switch with temperatures up to 200 °C has negligible effect on the performance of RF-MEMS switch. Temperatures in the range of 250 to 300 °C can help to improve the performance and temperatures of 350 °C lead to a significant performance degradation. It is noted that the capacitance ratio before stressing the samples varies between 8 and 9 due to the position of the measured chip over the wafer.
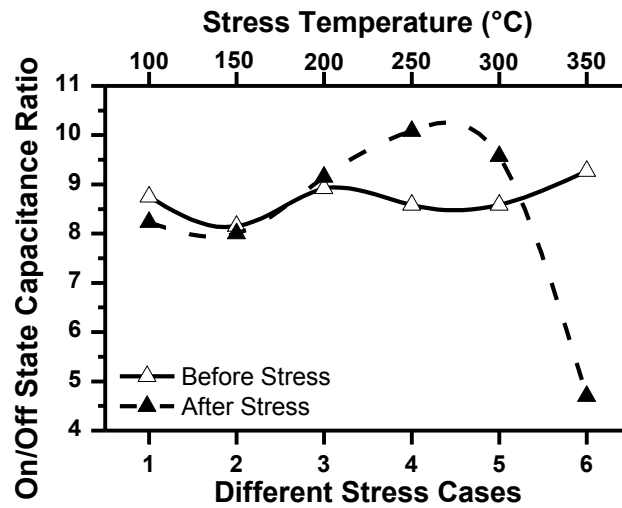


Figure 4.3 On/off state capacitance ratio with respect to stress temperature; before and after stressing [104]. All the measurements are done at room temperature.

In [103], it has been shown that stress relaxation in metal layers is a time-dependent process. Therefore, the influence of high temperature cycles is also analyzed. Repeating temperature cycles from 25 to 250 °C with a heating/cooling rate of ~20 °C/min are applied. After reaching the maximum temperature, the temperature is kept constant for 1 minute then the sample is cooled down to 25 °C and $C_{off}$ and $C_{on}$ are again measured. After every cycle, the impedance analyzer is recalibrated to prevent measurement errors due to high temperatures. It is again noted that all the measurements are done at room temperature after applying the stress.
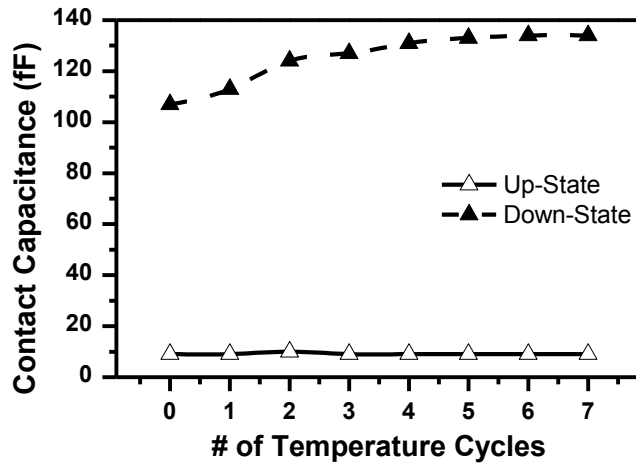
Figure 4.4 Contact capacitance with respect to different number of high temperature cycles for up and down states [104]. The temperature is swept from 25 to 250 ˚C with a heating/cooling rate of 20 ˚C/min for each cycle. All the measurements are done at room temperature.

Figure 4.4 shows the change of the up and down state contact capacitances with respect to the number of temperature cycles. $C_{off}$ is constant over the whole number of high temperature stress cycles; however, $C_{on}$ increases. After 6 annealing cycles, $C_{on}$ becomes constant. Therefore, stress relaxation for the specific temperature finishes and the maximum on/off state capacitance ratio is achieved. The result shows that the stress relaxation is strongly depending to the duration of the high temperature process. Consequently, shorter high-temperature packaging processes provide better stress control than the longer high-temperature processes.

To conclude, mechanical and electrical parameters of the RF-MEMS switch are influenced by high temperature stress steps which need to be taken into account during the packaging process development. High temperature stress steps can be either used for performance optimization and adjustments but can also lead to performance degradation if temperature limitations are not taken into account. The achievements in this section are extensively used during the development of different packaging processes in next sections.

## 4.3 Cap-to-Wafer Packaging

Cap-to-wafer packaging is used as the initial packaging approach of the RF-MEMS switch. Although the limitations of this method such as low-throughput, non-flexible package size and high cost are obvious, using glass as the cap material provides the advantage of further optical characterization after the packaging process.

The cap-to-wafer packaging process starts with the fabrication of glass caps. This process starts with bonding of a glass wafer to a silicon wafer (Figure 4.5a) and thinning the silicon wafer down to 50 μm of thickness (Figure 4.5b). The silicon frames are formed by deep reactive ion etching with a final thickness of 50 μm and a width of 30 μm (Figure 4.5c). Then, the polyimide adhesive is applied to the silicon frame surface and the glass caps are diced (Figure 4.5d, e). Lastly, a cap-to-wafer bonding process is performed with a temperature of less than 300 °C, compatible with the underlying BiCMOS structures (Figure 4.5f).
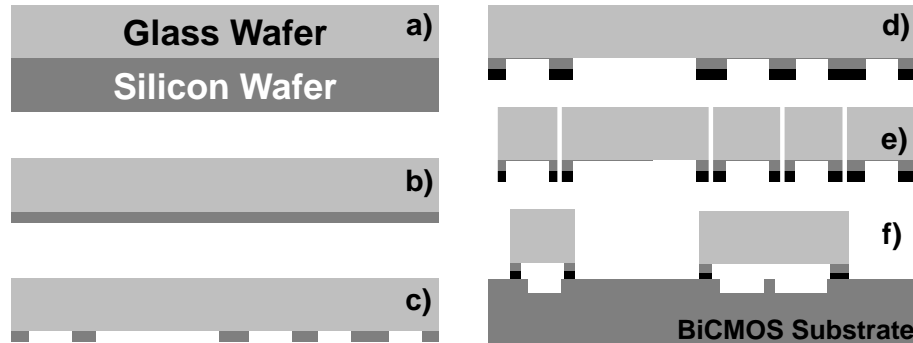


Figure 4.5 Process flow of cap-to-wafer packaging of RF-MEMS switches [92].

The upside down view of the glass cap is given in Figure 4.6 (left). There is a trade-off between the adhesion of the cap and the RF performance degradation with the width of the bonding frame. As can be seen, the silicon bonding cap has a width of 30 μm. This width provides enough adhesion between the cap and the BiCMOS wafer. Furthermore, it is also expected that the RF performance degradation is negligible due to the small overlap of the package and the RF signal line. Figure 4.6 (right) shows the cross-section of the cap. The silicon frame has a thickness of 50 μm.
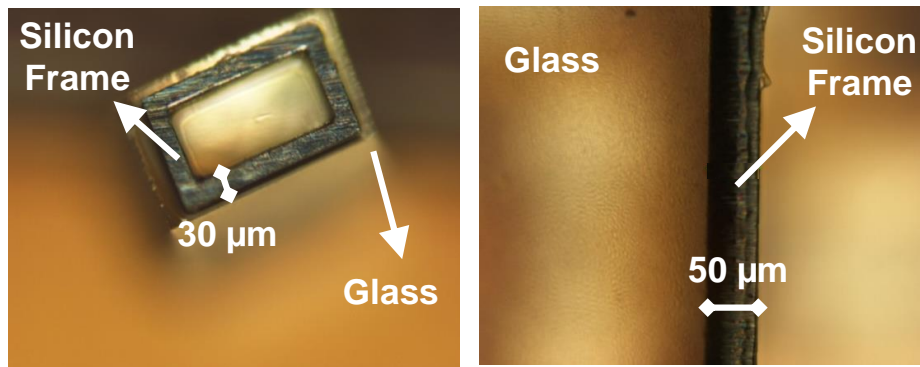
Figure 4.6 Closer view of the glass caps used for packaging of the switches. The caps have a bonding frame with a width of 30 µm (left) and a height of 50 µm (right) [92].

Figure 4.7 shows two bonded caps on to BiCMOS wafer. Closer views of the caps are also given in Figure 4.7 (right). It can be easily seen that the thickness of the glass caps is relatively big (~500 µm) which is another limitation considering the next level of integration into any other system. However, Figure 4.7 shows the successful bonding of the glass caps on top of two RF-MEMS switches next to each other.

The view of an RF-MEMS switch through the glass cap is shown in Figure 4.8 (left). Although the package height is high, the lateral dimensions of the package are small. Figure 4.8 (right) shows that the dynamic behavior of the switch remains the same after the packaging. It should be noted that the first tests with higher bonding temperatures have resulted in with different stress gradients in the membrane. However, keeping the bonding temperature below 300 ˚C provides similar results to the measurements before packaging.
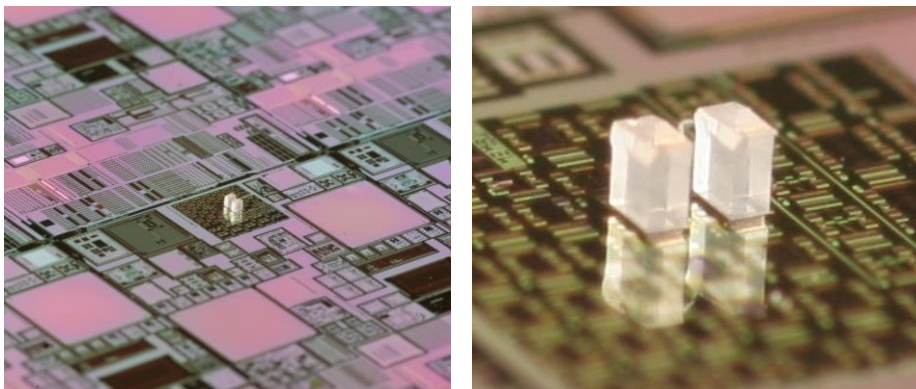


Figure 4.7 Packaged RF-MEMS switches using cap-to-wafer packaging process.
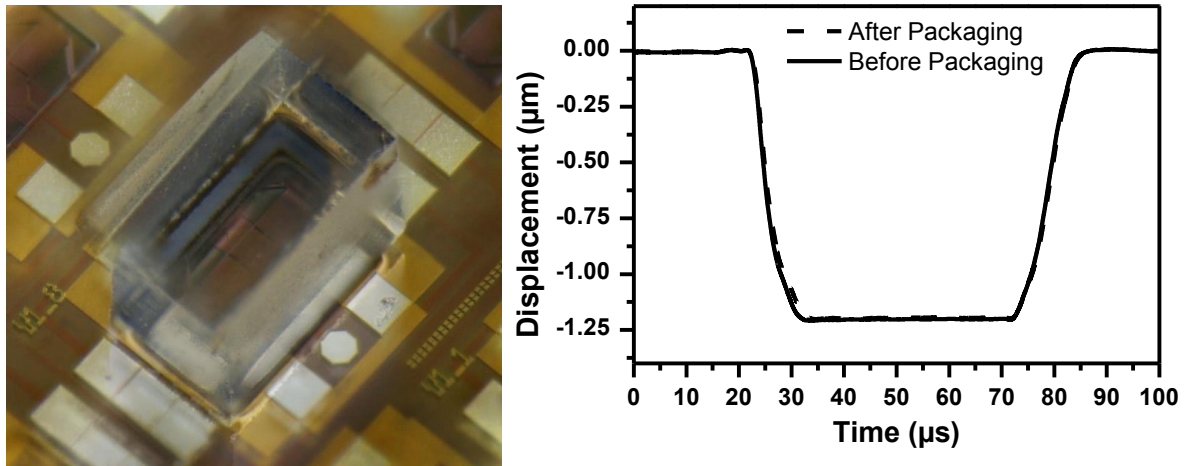
Figure 4.8 View of a packaged switch with glass cap (left) and switch displacement (contact region) versus time before and after packaging by LDV (right) [92].

The same cap-to-wafer type packaging process can also be applied to package several RF-MEMS devices in the same package. This has a significant advantage considering the small size of the mm-wave circuits. Figure 4.9 shows two different mm-wave circuits with two packaged RF-MEMS switches using the developed cap-to-wafer process. Figure 4.9 (left) shows a 24 - 77 GHz dual band re-configurable LNA and Figure 4.9 (right) shows a 60 - 80 GHz dual band re-configurable VCO. Detailed information about these re-configurable circuits is given in Chapter 7.
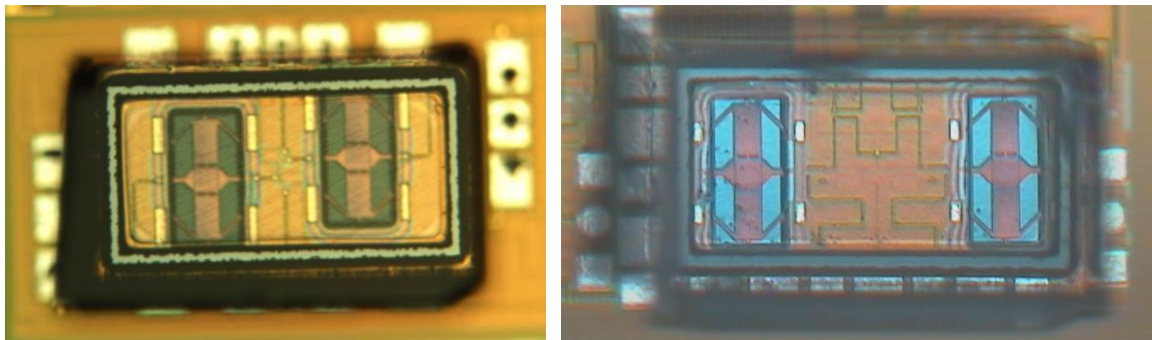


Figure 4.9 Top views of the packaged mm-wave LNA (left) and VCO (right). Both circuits include two RF-MEMS switches.

As mentioned at the beginning of this chapter, the main expectation out of the cap-to-wafer packaging process is the optical characterization of the suspended membrane after the packaging. The most important observation from these optical measurements is the change of the total displacement after the packaging process which shows the change of the stress behavior of the membrane. As a result of all these different experiments, in order to keep the stress behavior same as before packaging, the bonding temperature should be kept below 300 ˚C. The duration of the packaging process is also critical. Furthermore, the thickness and the residual stress of the membrane in use for the RF-MEMS device also influence the effect of the temperature induced stress during the bonding process.

## 4.4 Wafer-to-Wafer Packaging

Due to the aforementioned limitations of the cap-to-wafer packaging technique, a wafer-to-wafer packaging technique is developed to achieve higher throughput and flexible package size. Although the proposed method can also be used to hermetically package the RF-MEMS devices, in this study BCB material is used to achieve a permanent bond of the two wafers. The process flow of wafer-to-wafer packaging process is given in Figure 4.10. The process flow starts with the temporary bonding of a carrier wafer to the silicon wafer (Figure 4.10a, b). The silicon wafer is thinned down to 50 μm which is the final thickness of the package (Figure 4.10c). The next step is the spin coating and structuring of the BCB to form the bond frames (Figure 4.10d, e). In order to create different sizes of packages defined by the designer, an Reactive-Ion-Etch (RIE) process is applied to the silicon wafer and the different sizes of packages are realized (Figure 4.10f). Lastly, the wafer stack is bonded to the BiCMOS wafer at the process temperature of less than 300 ˚C (Figure 4.10g) and the temporary carrier wafer is de-bonded using a laser release technique. One of the main advantages of using laser de-bonding technique is the low process temperature which is very critical, as mentioned before.
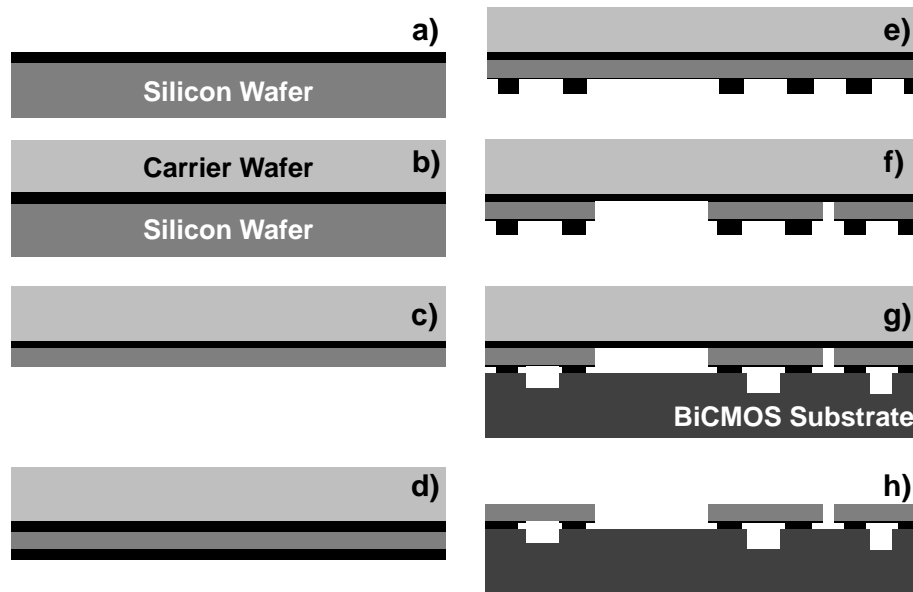
Figure 4.10 Process flow of wafer-to-wafer packaging of RF-MEMS switches.

Figure 4.11 and Figure 4.12 show the process of the wafer-to-wafer packaging process at different steps. Figure 4.11 (left) shows the BCB frame for bonding while Figure 4.11 (right) shows the package caps after RIE process. The alignment of two wafers before bonding is also given in Figure 4.12 (left). A glass wafer is used as the carrier wafer. Therefore, the silicon caps can be seen through the glass wafer in the same figure. The view of the wafer after de-bonding of the carrier wafer with many packaged devices is given in Figure 4.12 (right).
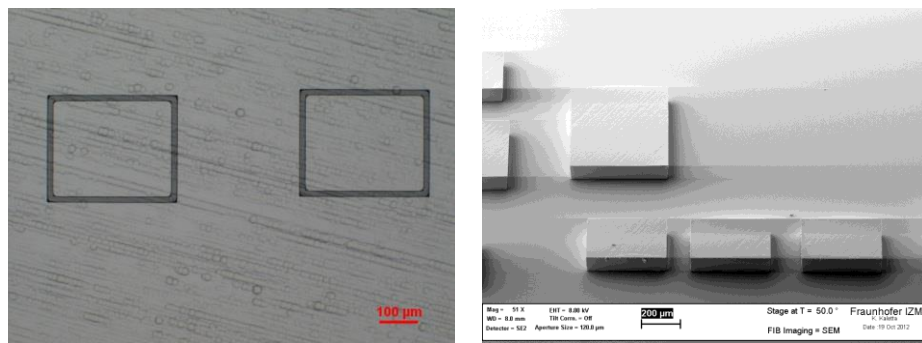


Figure 4.11 Microscopic and SEM views of the package wafer in between different steps of wafer-to-wafer packaging process: After BCB structuring (left) and after deep silicon RIE step (right).

As can be seen from Figure 4.12 (right), many switches can be packaged using the developed wafer-to-wafer packaging process. However, as it has to be applied to MPW wafers, the density of RF-MEMS devices is limited. Therefore, many dummy packages are also necessary to stabilize the bonding and de-bonding processes.
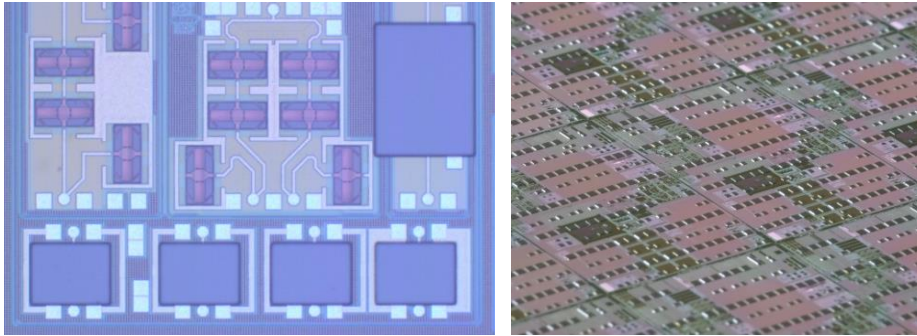


Figure 4.12 Different views of the packaging process: During the alignment of BiCMOS and carrier wafers (left) and after de-bonding process (right).

Figure 4.13 shows the SEM view of packaged devices after de-bonding of the carrier wafer. Figure 4.13 (left) shows several RF-MEMS devices packaged very close to each other while the thickness of the package height can be seen in Figure 4.13 (right).
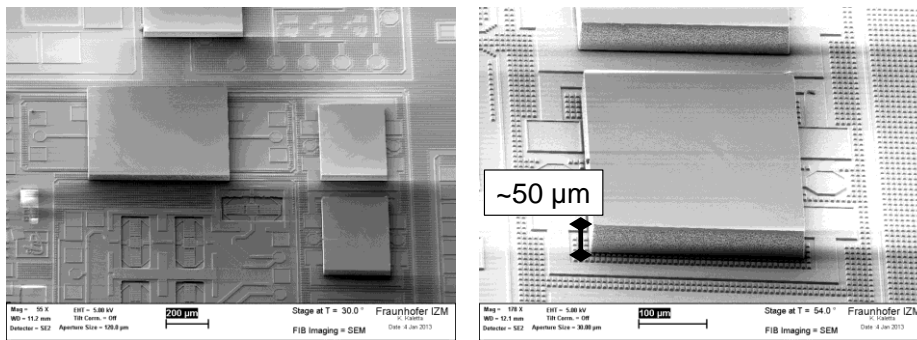


Figure 4.13 SEM view of packaged RF-MEMS devices using different sizes of silicon caps (left) and close view of a packaged single RF-MEMS switch (right).

A further analysis of the wafer-to-wafer packaging is done using a FIB technique. The package is cut by FIB to analyze the BCB frame after the packaging. Figure 4.14 shows the cross section of the BCB frame. A distance of 30 µm is used to prevent the leaking of BCB into the RF-MEMS device cavity on both sides of the BCB frame.
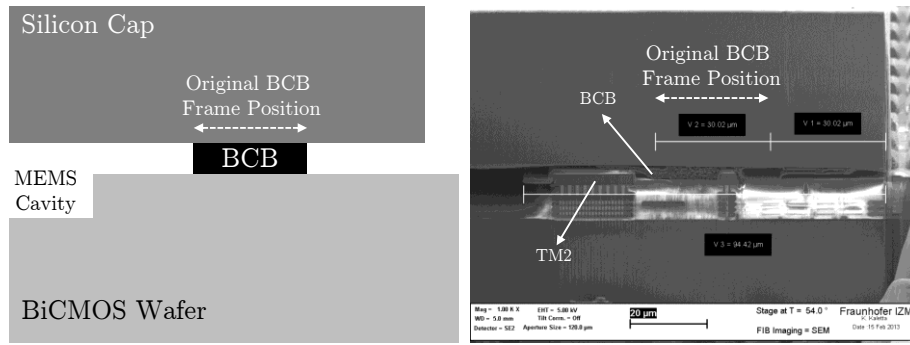
Figure 4.14 Generic view (left) and FIB cut view (right) of a packaged RF-MEMS switch using wafer-to-wafer packaging process. The original BCB frame with a width of 30 μm is indicated.

The original BCB frame is also indicated on Figure 4.14 with a 30 μm width. Another 30 μm distances on both sides can also be seen. The BCB material slightly leaked toward the RF-MEMS device cavity but no BCB arrived in the cavity. In general, 15 - 20 μm distance from BCB frame to cavity is enough to prevent unwanted leakage of the BCB into the cavities and 20 μm is taken as the design rule for further packaging processes.

## 4.5  Conclusion

In Chapter 4, different approaches for RF-MEMS switch packaging have been discussed. The thermal budget of the packaging process has been investigated and a reliable process temperature has been defined. Two different types of packaging process have been studied; cap-to-wafer and wafer-to-wafer. The process flows for both techniques have been provided. Packaging process flows have been optimized to keep the underlying BiCMOS process without any change.

The development of RF-MEMS devices in last few years has shown that the most efficient substrate size of RF-MEMS devices is 8-inch in order to decrease the price per device, especially for medium/large level production. The need of using RF-MEMS devices with CMOS circuits has increased the CMOS+MEMS platforms which add temperature limitation for packaging.  In this thesis, it has been found that temperatures less than 300 °C have no significant effect on the stress characteristic of

the movable membranes for the specific example. However, it should be noted that the allowable thermal budget is strongly influenced by the material, thickness and the spring constant of the membrane. The maximum available temperature should be investigated before the optimization of the packaging process.

To conclude Chapter 4, RF-MEMS devices cannot be considered real devices without a package. Appropriate packages with low cost and low parasitics are required. The commercial RF-MEMS devices show that the special wafer-to-wafer packaging techniques can be used for niche markets with low-volume production. However, wafer-level encapsulation techniques are more promising considering the shorter process time and lower cost for mass production applications.

# 5 On-Chip High Voltage Generation

## 5.1 Introduction

Recently, an entirely CMOS embedded RF-MEMS tuner has been introduced by WiSpry for mobile communication applications [23], showing that RF-MEMS technologies can fulfill the market needs with respect to reliability, yield and cost perspectives. At first look, it shows that finally RF-MEMS devices are combined with high frequency circuits in a CMOS platform. However, the main reason for the CMOS integration of RF-MEMS tuner is not the high level of integration to RF front-end, but the necessity of high voltage for the actuation of the RF-MEMS devices and the control circuits in order to control many RF-MEMS devices in a smart way to achieve the desired performance figures.

Most of the commercial and research based RF-MEMS components show the need of high voltage operation (i.e. 40 to 100 V) to provide sufficient reliability. Several studies have also shown that such high voltages can be generated using charge pump circuits in a CMOS environment. Standalone RF-MEMS switch providers offer high voltage generation circuits separately while the CMOS embedded RF-MEMS tuner technology from WiSpry comes with internal high voltage generation circuits together with control circuits. Although high voltage generation using different techniques has been studied by several groups [76, 105, 106, 107], the dynamic behavior of such high voltage generation circuits has not yet been widely studied since the requirements of these parameters strongly depend on the application.

In general, the mechanical domain is much slower than the electrical domain. However, the time required to generate high voltages (e.g. > 50 V) can take up to few microseconds. It is also similar for reducing of the voltage from 50 to 0 V. Therefore, it is not easy to predict the main limitation of the speed of the RF-MEMS device. It is always the combination of electrical and mechanical domains. High voltage generation circuits should be designed by taking this effect into account and the circuits need to be optimized together with the RF-MEMS devices as well.

In Chapter 5, the details of the CMOS based high voltage generation circuit are given. Firstly, the optimization of the technology in order to stand such high voltages is explained in section 5.2. Then, the circuit blocks; namely ring oscillator, 20-stage charge pump and discharge resistor are given. Lastly, the electrical simulation/measurements and the LDV results are provided and discussed. The electrical and the mechanical time limitations are discriminated by using simultaneous electrical and the optical characterization techniques. Chapter 5 is concluded with section 5.4.

## 5.2 High Voltage Generation Circuits and Sub-Blocks

IHP's 0.25 μm SG25H1 BiCMOS technology is used to design the on-chip high voltage generation circuit. In contrast to fast CMOS operation requirements, the charge pump circuit in this study needs PMOS transistors with a high breakdown voltage between N-well and surrounding P-well regions in order to retain the high voltage in the N-well. Therefore, the width of the P-well block layer surrounding the PMOS transistor, is increased. Figure 5.1 shows the breakdown voltage from N-well to substrate for different widths of P-well block. In this study, 2.2 μm width of P-well block is used. The expected N-well to substrate breakdown voltage is more than 50 V.
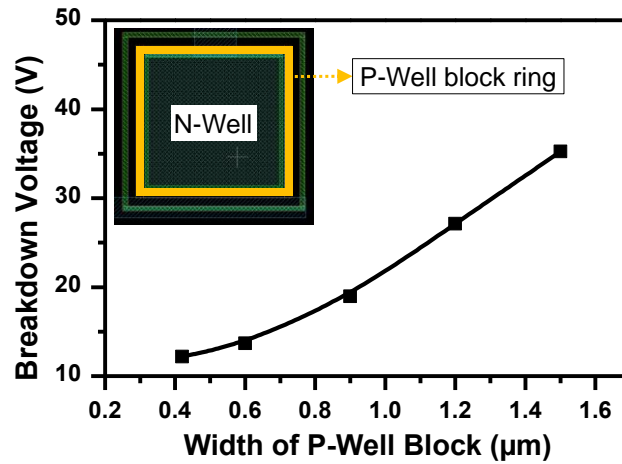


Figure 5.1 Layout view of the P-well block ring of PMOS transistor and the measured N-well to substrate breakdown voltage for different widths of P-well block ring [108].

The sub-blocks of the complete high voltage generation circuit are given in Figure 5.2. A ring oscillator with a frequency of 20 MHz is used to provide the required positive and negative clock signals (CLK+ and CLK-) to the charge pump. A 20 stage charge pump is realized by PMOS transistors. Lastly, a discharge resistor is used to accelerate the discharge of the charge pump.
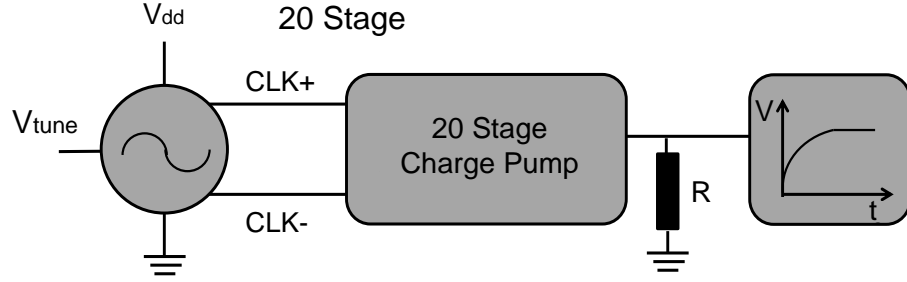


Figure 5.2 Sub-blocks of high voltage generation circuit [108].

A seven stage ring oscillator is used to generate the required CLK signals for the charge pump (Figure 5.3). The amplitude of the output is mainly controlled by the supply voltage while the frequency is controlled by the varactors, added between the inverter stages. Two additional inverters with larger transistor width are used at the output to correct the distorted output signal and to create the CLK- signal. The peak-to-peak amplitude of the oscillator varies from 1.5 to 4 V by changing the supply voltage ($V_{dd}$) of the ring oscillator. The output frequency can be controlled between 15 to 25 MHz by tuning the $V_{tune}$ from -1.5 to 1.5 V.
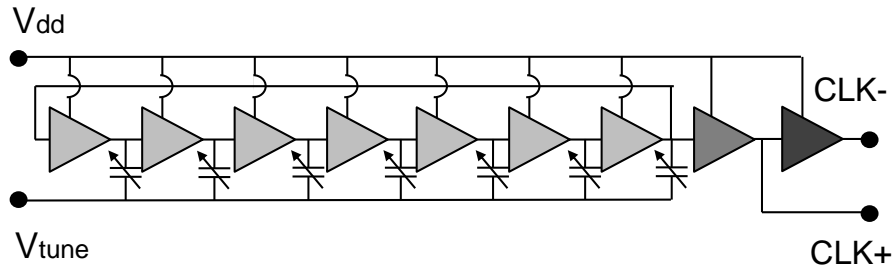


Figure 5.3 The block diagram of the seven stage ring oscillator [108].

Transient output of the ring oscillator is given in Figure 5.4 under the biasing condition of $V_{dd}$=2.5 V and $V_{tune}$=-1.5 V. It shows that the output oscillation signal has a peak-to-peak voltage of 2.5 V and the frequency of oscillation is approximately 22 MHz.
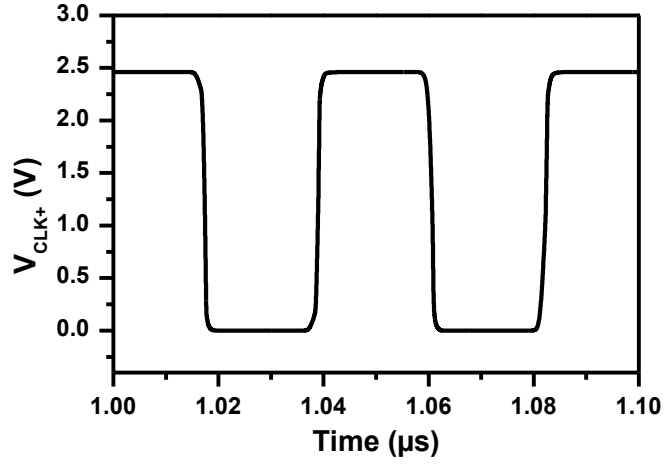


Figure 5.4 Transient output of the ring oscillator (only CLK+) with $V_{dd}$=2.5 V and $V_{tune}$=-1.5 V.

A 20-stage charge pump circuit is realized using "charge transfer blocks" (CTB) which consists of diode-connected PMOS transistors (Figure 5.5), as comprehensively studied in [106].
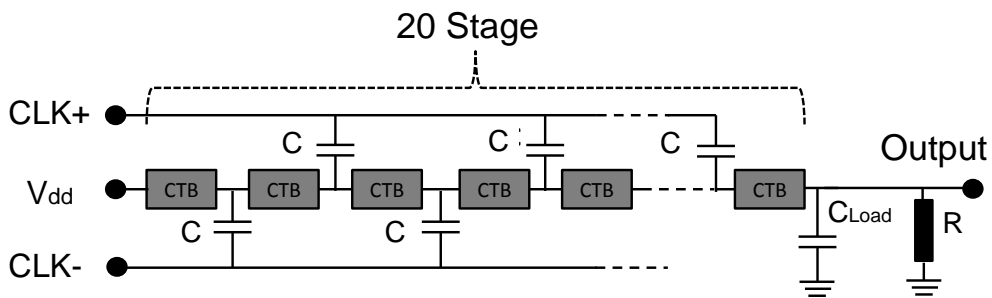


Figure 5.5 Block diagram of 20-stage charge pump circuit [108].

The coupling capacitors (C) after every CTB have a value of 2.5 pF which is a result of two series-connected 5 pF capacitors. Series-connected capacitors are used in order to stay below from the breakdown voltage of single MIM capacitors, which is around 30 V. Instead of a one single capacitor, using of two series capacitors helps to prevent MIM breakdown and therefore improves the long term reliability. The load capacitor ($C_{Load}$) only affects the ripple of the output signal. Therefore, it is chosen as 1 pF to achieve a ripple of less than 2 V at the output.

The discharging speed of the charge pump is another important specification in this design, especially for use in fast operating systems, such as in T/R antenna switches. Without using a discharge circuit, discharge of the output from 40 to 0 V can take more than 200 μs which is several orders of magnitude longer than the mechanical release time of the RF-MEMS switch (< 10 μs). Although more advanced CMOS based stacked discharge circuits can be designed, in this thesis a simple discharge resistor is used. It is clear that the discharge resistor comes with the drawback of lower output voltage for the same supply voltage. In other words, to achieve the required output voltage, a higher supply voltage is necessary which increases the total power consumption.

## 5.3 Simulation Results and Experimental Data

In this section, the simulation results are given together with the measurement results. The simulation of the high voltage generation circuit is done by using Agilent ADS. Although electrical results provide detailed information about the amplitude, rise time and fall time of the output voltage, it is not easy to extract the pure circuit performance since the dynamic behavior of the circuit is significantly affected by the measurement system parasitics, e.g. oscilloscope input capacitance and resistance. Therefore, the real case scenario, using the high voltage generation circuit together with RF-MEMS switch, is characterized by using LDV which does not affect the circuit performance and therefore provides a platform independent from the parasitic components.

- *Electrical Simulations and Measurement Results*

Figure 5.6 and Figure 5.7 show the simulation and measurement results of the output voltage for different supply voltages. The rise and fall times of the generated high voltage waveform are relatively large ($> 150$ µs and $> 500$ µs, respectively) due to the system parasitics ($> 150$ pF) which are also considered during the simulations.
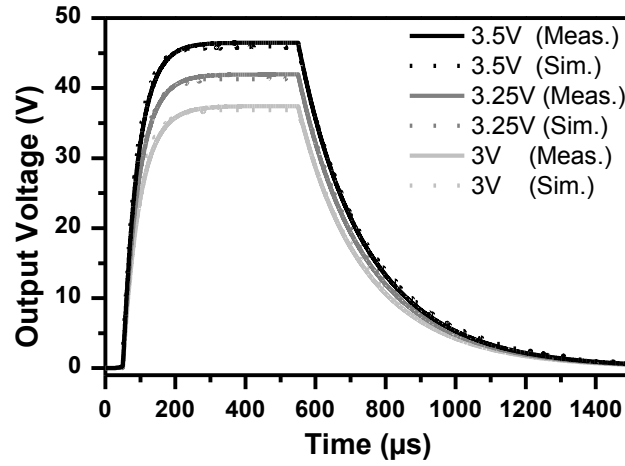


Figure 5.6 Simulation and measurement results of the transient behavior of the output voltage for different $V_{dd}$ ($C_{Load} = 1$ pF and R $= 1$ MΩ). Simulations are done by considering 150 pF measurement system parasitic capacitance [108].
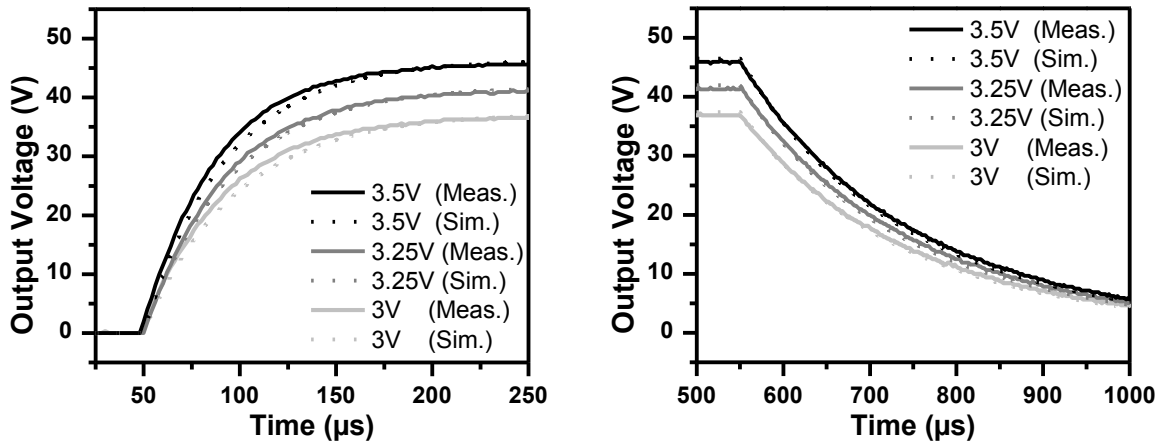


Figure 5.7 Close view of switch-on (left) and switch-off (right) transient behavior of the output voltage for different $V_{dd}$ ($C_{Load}=1$ pF and a 1 MΩ discharge resistor) [108].

After achieving good agreement between the simulation and measurement results, the circuit is simulated without taking the parasitic capacitances into account. In this case, the simulation results show the real case scenario if the charge pump is connected to the RF-MEMS switch, since the high voltage electrode of the RF-MEMS switch behaves like an open circuit.

Figure 5.8 shows the simulation results for different discharge resistors. As mentioned in previous sections, the discharge resistor decreases the output voltage. To achieve the required output voltage (> 40 V), $V_{dd}$ is changed for different resistor cases. Figure 5.8 shows the transient behavior of the output for 5 MΩ, 1 MΩ and 250 KΩ. To achieve the 40 V output voltage, 2.75 V, 3.25 V and 4.25 V were applied for 5 MΩ, 1 MΩ and 250 KΩ, respectively.
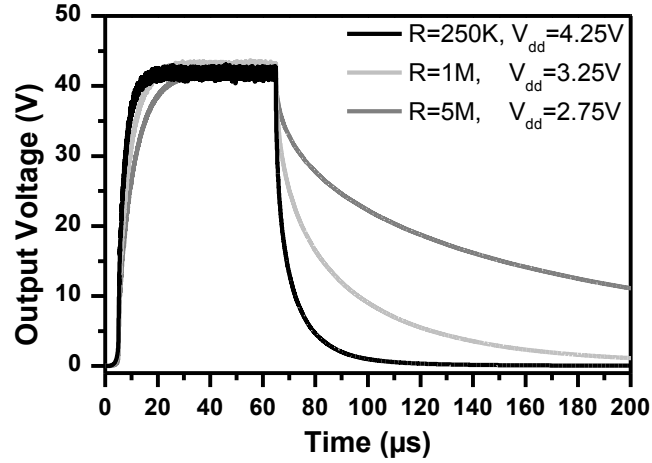


Figure 5.8 Simulation results of the transient behavior of output voltage for different discharge resistors when there are no parasitic capacitances at the output [108].

Figure 5.9 shows that the rise time of the output is simulated as less than 10 μs for all the cases while the fall time varies from 10 μs to a few hundred μs, depending on the output resistor. Figure 5.9 also shows the ripples at the output, especially for the case of 5 MΩ output resistor. The complete circuit occupies 0.3 mm$^2$ chip area and consumes 12 mW power for 5 MΩ, 27 mW power for 1 MΩ and 75 mW power for 250 KΩ discharge resistor cases to generate the required 40 V output voltage. Table 5.1 summarizes the performance parameters of the high voltage generation circuit.
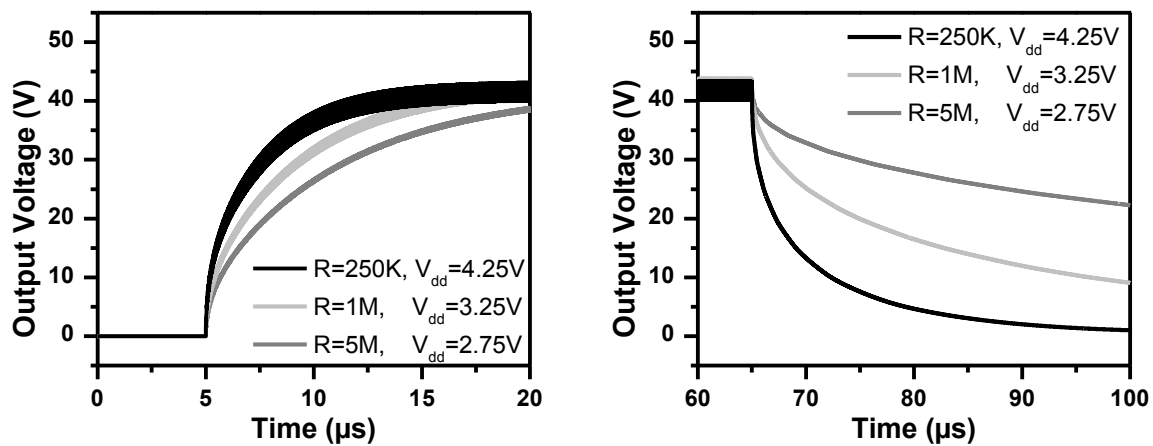
Figure 5.9 Close view to the transient behavior of output voltage for different discharge resistors without parasitic capacitances at the output node [108].

Table 5.1 Performance parameters of the high voltage generator.

| Discharge resistor value | $V_{dd}$ for 40 V output | Power Consumption |
| --- | --- | --- |
| 5 MΩ | 2.75 V | 12 mW |
| 1 MΩ | 3.25 V | 27 mW |
| 250 kΩ | 4.25 V | 75 mW |

- *Optical Results and Validation of Electrical Results*

In order to validate the electrical simulation results, the high voltage generation circuit is connected to the RF-MEMS switch on chip (Figure 5.10) and the dynamic behavior of the switch is analyzed using the LDV technique.
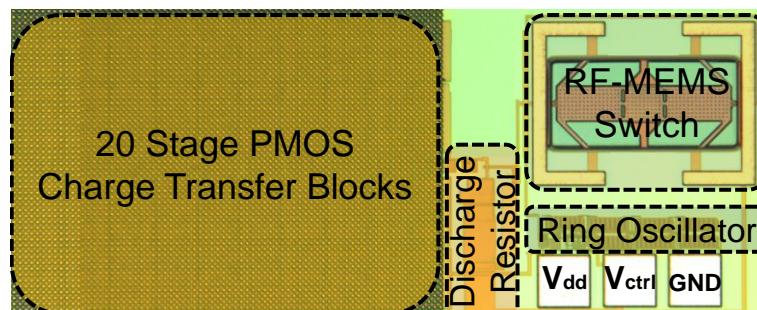


Figure 5.10 Micrograph of high voltage generation circuit with RF-MEMS switch [108].

Figure 5.11 shows the results of 3 different discharge resistor cases. The simulated transient output voltage can also be seen in the same figure.
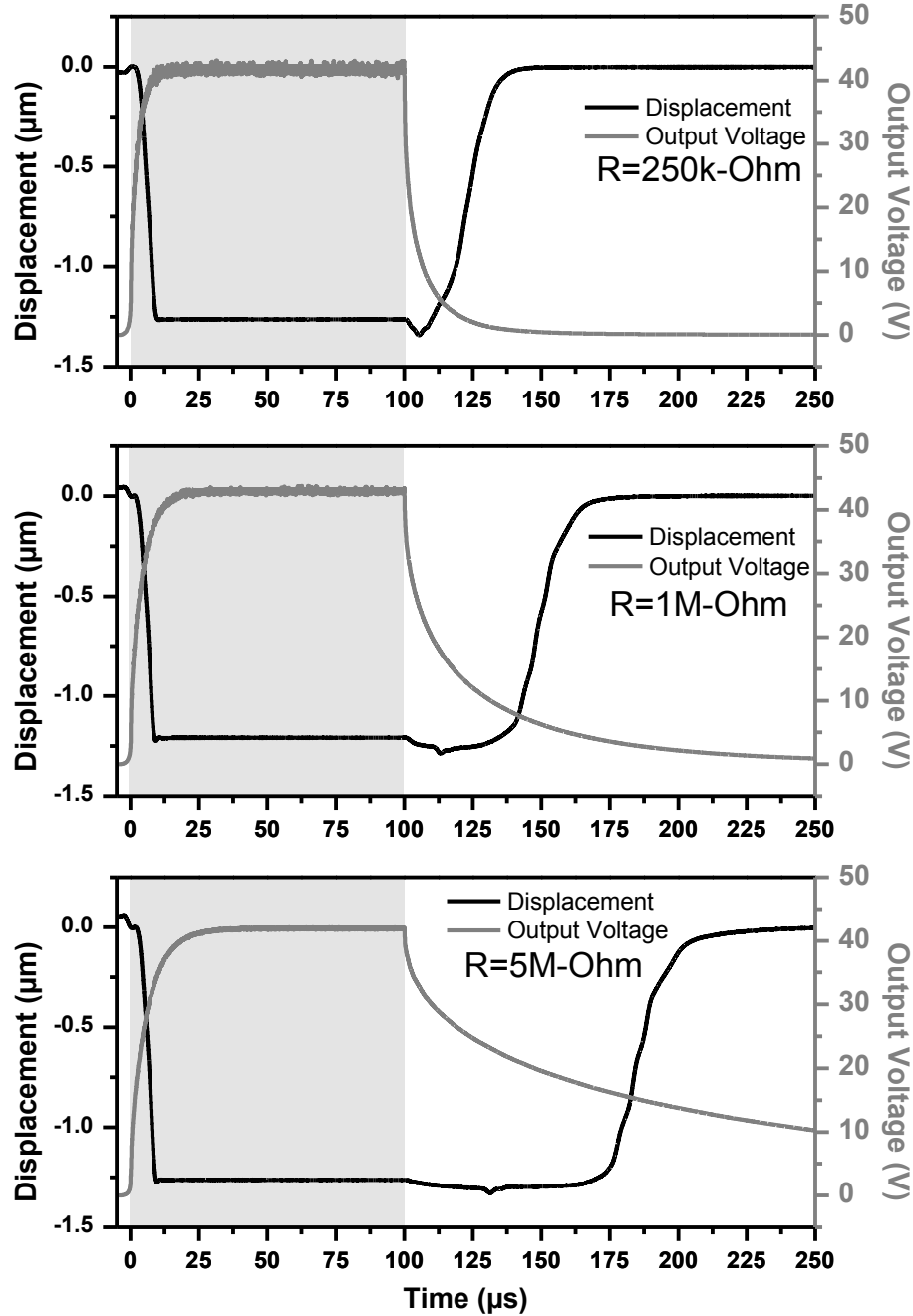


Figure 5.11 Measurement results for displacement of the membrane together with the simulated high voltage pulse. There different cases for three different output resistors; 250 KΩ, 1 MΩ and 5 MΩ [108].

The gray region in Figure 5.11 shows the duration of the applied 100 μs high voltage pulse. It can be seen that the switch-on time can be kept below 10 μs for all the cases (with different power consumption) while the release time strongly depends on the discharge resistor. For the 5 MΩ case, the release starts after 60 μs, when the output voltage goes below 20 V. The release starts after 25 μs for 1 MΩ case while for 250 KΩ, the release of the membrane starts after 10 μs and mechanical release takes additional 15-20 μs.

## 5.4 Conclusion

In Chapter 5, high voltage generation circuit for RF-MEMS switch actuation has been presented. The circuit is fully realized in IHP's 0.25 μm SG25H1 technology; thus allows actuating the embedded RF-MEMS switch without a need for an external high voltage supply. The sub-blocks of the high voltage generation circuitry have been explained and the optimization process of the PMOS transistor layout to achieve high breakdown voltages has been illustrated. The measurement and the simulated results have been compared. Finally, the RF-MEMS switch is actuated by the on-chip high voltage generation circuit and the optical measurements are combined with the electrical ones in order to analyze the influence on real switch-on and -off times of the switch for different discharge resistors.

To have an RF-MEMS product, it is not necessarily required that the RF-MEMS device provides the best performance. It is well known that RF-MEMS devices come with many non-uniformity and yield problems. To minimize these effects, serious process development effort is necessary which would increase the research and development cost. However, the power of the CMOS processing can significantly help RF-MEMS devices to compensate these effects. Most of the applications working with many RF-MEMS devices need strong processing capabilities. These strong processing capabilities such as on-chip detection of the contact capacitance or pull-in voltage can be easily done using CMOS based circuits. Therefore, adding the CMOS processing capabilities to RF-MEMS is now a "must" for the many RF-MEMS companies which look for medium or large scale commercial markets.

To conclude Chapter 5, RF-MEMS devices are excellent devices but the strong processing power of CMOS makes them useful as a product. There are many ways to create high voltage in a CMOS environment and special high voltage technologies such as LDMOS or SOI can play an important role to decrease the area of the high voltage generation circuits. Another uncertainty is the RF front-end technologies of mobile applications. If industry continues with high-end and expensive technology nodes for the RF front-ends, then the CMOS or BiCMOS platform for RF-MEMS integration can be chosen independently for high voltage generation and control circuits. However, if heterogeneous integration processing techniques grow fast, RF front-end node can detach from the digital node and goes back to 90 nm or higher nodes. This would certainly increase the interest of having RF front-end together with the RF-MEMS devices, high voltage generation and control circuits integrated on the same die.

# 6 Robustness and Reliability

## 6.1 Introduction

Most of the RF-MEMS studies start with the explanation of the advantages of RF-MEMS technologies over the other semiconductor technologies. The comparison list typically includes more than ten items in which RF-MEMS technology prevails at least in eight of them. However, the reliability issue is always stressed by the community as one of the main bottleneck. We can clearly state that the main obstacle in RF-MEMS technologies in these days is the reliability.

To understand the reliability evaluation of different technologies, one of the most prevalent semiconductor technologies, CMOS, can be given as an example. The field effect transistor was first proposed in 1925 by J, Lilienfield and first CMOS logic gate was patented in 1963 by F. Wanlass. Twenty-five years later, CMOS had become the predominant technology in digital integrated circuits. Early CMOS circuits were very susceptible to electrostatic discharge (ESD) and many other reliability problems; however, they were solved by different techniques in the last decades [109]. After few decades, we have come to a point where we can clearly define the reliability and the qualification test procedures for CMOS. However, even for one of the most important semiconductor technologies, CMOS, it took a few decades to define the reliability and the test procedures.

The history of RF-MEMS technology is not so different from that of the CMOS industry with the exception of the importance of the technology during the years it was invented. RF-MEMS technologies came into their own as a promising industry in the early 90's, mainly for defense applications. Until 2000-2002, many different kinds of RF-MEMS devices had been demonstrated with very promising performance figures. However, the RF-MEMS technology was almost killed during these years because of its terrible reliability. Although it has been very promising technology in 2000s, the need of the market for this technology was not high enough. As a result, industry has not invested to solve the reliability problems. The main difference was done by DARPA in the US and a program on RF MEMS reliability was created [110]. Finally, first commercial products were on the market right after couple of years.

Considering the RF-MEMS switches specifically, one of the major problems is the thermally induced stress. It results in a change of the key performance parameters such as pull-in voltage and "on-state"/ "off-state" capacitances with the temperature, which can strongly limit the switch operation temperature range. Several methods have been used to prevent temperature change effects, such as realizing the suspended membrane with a temperature-resistant material or using a membrane material which has a similar thermal expansion coefficient as the substrate [111, 112]. A further method is modifying the geometry and compensating the stress within the suspended part of the MEMS component [42].

Another important robustness figure of the RF-MEMS switch is the power handling capability. Although the power levels of mm-wave applications are limited to a few hundred mWs, self-actuation and latching of the switch also need to be analyzed. Biasing conditions and RF power levels of an RF-MEMS switch should be taken into account during the mm-wave circuit design.

Beside high performance and robustness, switch reliability is another very important issue. Typically, reliability tests need significant effort and time. Furthermore, it is not easy to predict the degradation of the switch from typical life-time tests, especially if the switch operates without any failure up to several billion cycles of operation. In addition to the electrical and material science domain, mechanical domain also comes with the needs of new reliability investigations and protocols.

Chapter 6 covers the robustness and the reliability investigations of the RF-MEMS switch, realized in this thesis. Section 0 starts with the basic study about the influence of the temperature. In this section, the change of the performance parameters with the temperature is investigated in the range of -30 to 150 °C. In section 6.3, the power handling capability is investigated with respect to self-actuation and latching performance. Finally, results of reliability tests using LDV technique are presented in section 6.4. Chapter 6 is concluded with some general remarks under section 6.5.

## 6.2  Temperature Dependency

To evaluate the temperature dependency of the performance change, non-packaged switches are tested on a probe station equipped with a temperature controller which is capable of controlling the chuck temperature over a range of -30 to 150 °C. The contact capacitance measurements are done at 1 MHz using an impedance analyzer. The equipment is controlled by a program that can measure up- and down-state capacitances and automatically detects the pull-in voltage. The down-state capacitance ($C_{down}$) is measured at 40 V actuation voltage independently from the pull-in voltage of the switch. The duration of the excitation pulse is taken as 400 ms. Tests are performed over an 8-inch wafer for more than 50 different sites.

Figure 6.1 shows the up-state capacitance ($C_{up}$) of the switch as a function of temperature. The mean value of $C_{up}$ decreases with increasing temperature, from 16 fF at -30 °C to 8 fF at 150 °C. This can be explained by the increase of compressive stress in the suspended membrane which results in an increase of the initial gap between membrane and contact layer. $C_{up}$ variations over the wafer are indicated in Figure 6.1 by the error bars. These variations result from the process variations across the wafer.
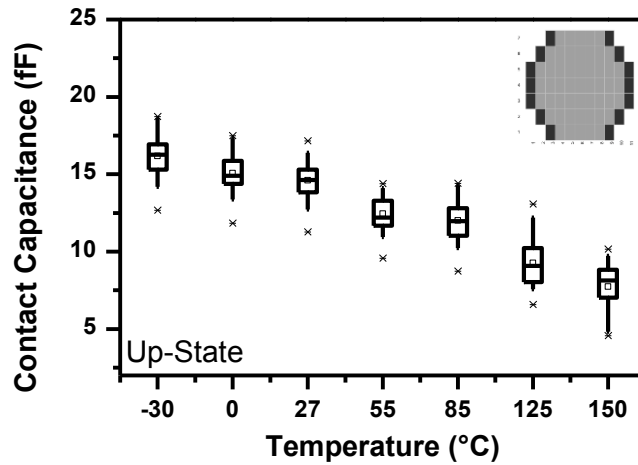


Figure 6.1 Switch up-state capacitance versus temperature, measured for an 8-inch wafer including more than 50 wafer sites. Gray marked chips are measurement chips while black ones are omitted [113].

At first sight, a decrease by factor of 2 of $C_{up}$ between -30 and 150 °C seems to argue against switch robustness. However, it is found by the simulations that for frequencies up to 90 GHz, the insertion loss ($S_{21}$) is influenced by three main factors, with the following rough percentages of impact: Finite conductivity of M2 (50 %); capacitive coupling to the substrate (35 %) and capacitive coupling to the M3 over $C_{up}$ (15 %). Clearly, due to the relatively low impact of factor (3), a $C_{up}$ variation does not affect the total insertion loss much; thus a decrease even by a factor of 2 over the full temperature range does not really argue against switch robustness.
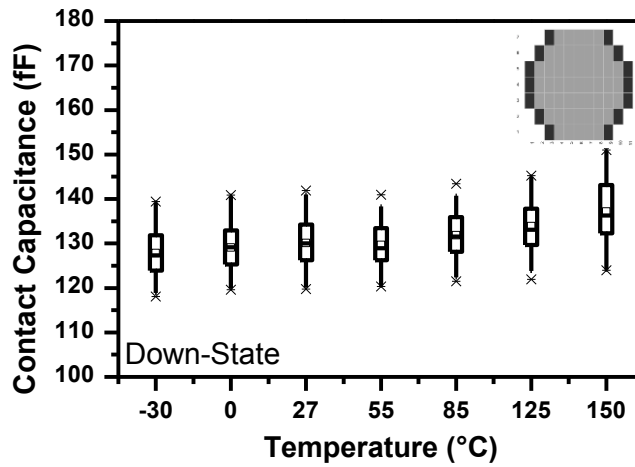


Figure 6.2 Switch down-state capacitance versus temperature measured for an 8-inch wafer including more than 50 wafer sites. The gray marked chips are the measured chips while the black ones are omitted [113].

Figure 6.2 shows the temperature behavior of $C_{down}$. Clearly, the temperature impact is much lower compared to the $C_{up}$ case. $C_{down}$ increases by only about 6 % over the full temperature range.

The temperature impact on the pull-in voltage is given in Figure 6.3. Obviously, there is no significant change of the pull-in voltage due to the temperature change. A low effect of the temperature can be explained by the particular switch geometry which compensates the thermally induced stress. The extra compressive stress from the temperature increase causes the suspended membrane to bend up more, but due to the operating principle of the switch, the distance between high voltage electrodes and the suspended membrane (i.e. between M1 and M3) does not significantly change.
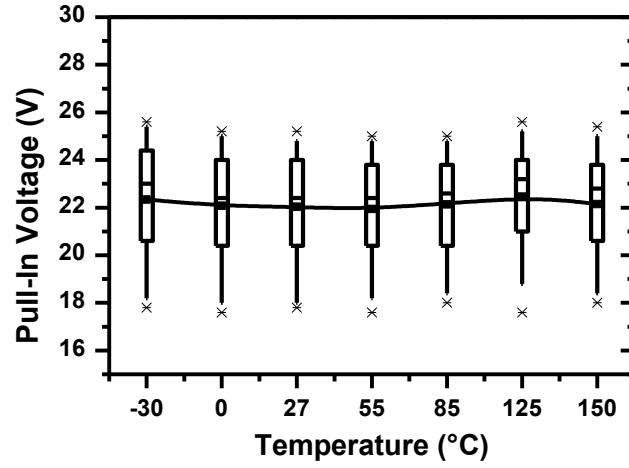
Figure 6.3 Switch pull-in voltage versus temperature measured for an 8-inch wafer including more than 50 wafer sites. Bars show the change of pull-in voltage over 8-inch wafer and the curve shows the change of the mean value of pull-in voltage [113].

## 6.3 Power Handling

RF-MEMS switches are used under different RF and DC bias conditions strongly depending on the application. Mm-wave circuit design with embedded RF-MEMS switches needs special considerations. For instance, the biasing conditions should be considered in advance, during the circuit design stage as the RF-MEMS switch is connected to the other components on chip. There are mainly two types of failure modes due to non-accurate biasing or too high RF power; namely self-actuation and latching. These two effects are investigated using LDV in the next section.

### 6.3.1 Self-Actuation

Self-actuation is one of the failure modes of RF-MEMS switches, where the high level of DC or root mean square (rms) of RF signals on the signal line generate enough force to pull down the membrane without any electrode voltage. To characterize the performance of the switch, a DC voltage difference is applied only between the signal line (M2) and the membrane (M3) and no voltage is applied to electrode (M1). Figure 6.4 shows the displacement of the membrane due to the DC voltage drop between the movable membrane and the RF signal line.
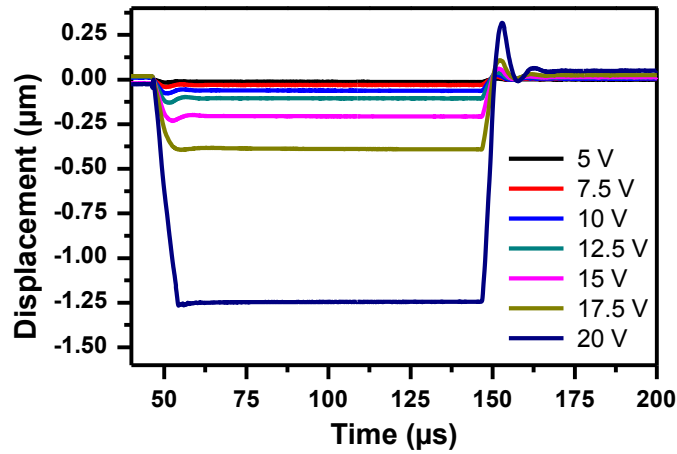
Figure 6.4 The displacement of the switch membrane versus time under the different DC potential differences between the signal line (M2) and the membrane (M3) [113].

The deflection of the membrane is below 100 nm up to 10 V. However, self-actuation occurs at 20 V difference between M2 and M3 which is quite far from the typical biasing conditions of mm-wave circuits, i.e. 0 to 5 V. Similarly, rms of typical RF power levels at mm-wave frequencies is far lower than the values which cause self-actuation. Out of these tests, it can be concluded that the self-actuation is not a significant problem for the RF-MEMS switch under investigation.

## 6.3.2  Latching

Latching is another failure mode which the DC level or rms value of applied RF signal level on the signal line has enough force to hold the membrane at down position. Latching typically occurs when the RF signal is applied as continues wave (CW) or if there is a DC potential difference between signal line and membrane. To investigate the effect, the switch is actuated by applying a high voltage to the electrode (M1) and a DC pulse is applied to the signal line (M2), while the DC level of the membrane (M3) is taken as ground. Then, the high voltage on the electrode (M1) is taken back to 0 V and releasing of the movable membrane is observed. The results are given in Figure 6.5. A DC level on the signal line up to 1 V only increases the releasing time of the RF-MEMS switch. However, at 1.2 V the switch cannot release anymore. This result shows that the DC potential difference between signal line and the membrane should be kept below 1.2 V for the safe operation.
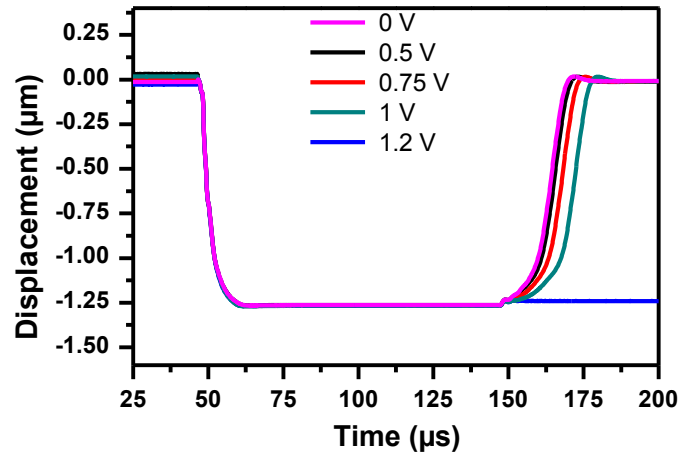
Figure 6.5 Displacement of the switch membrane versus time for different DC voltages applied on the signal line. No RF signal is applied [113].

A further test is carried out using RF signal on the signal line. RF power levels are swept from -17 to 15 dBm at 10 GHz. The release time of the switch increases with higher RF power, as can be seen in Figure 6.6. The switch membrane keeps its down position at 15 dBm RF power. This power level should be taken into account when the application needs CW operation.
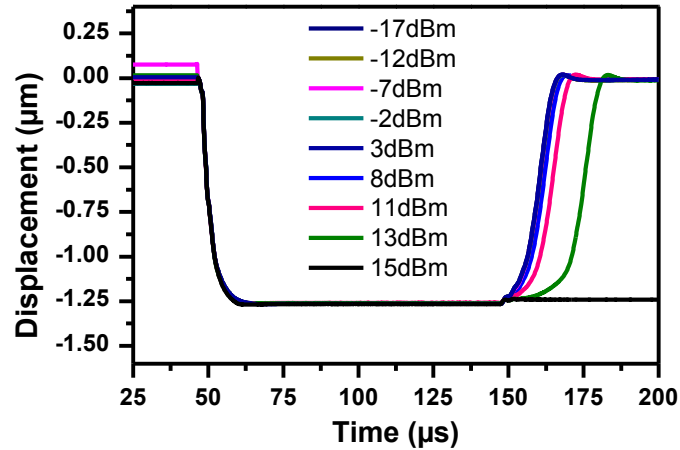


Figure 6.6 Displacement of the switch membrane versus time for different RF power levels applied at 10GHz. No DC bias is applied to the RF signal line [113].

## 6.4 Reliability

The reliability tests of the developed RF-MEMS switch are done using the on-wafer measurement techniques on the non-packaged devices in an ambient environment. The tests are performed based on the optical measurement techniques in order to better understand the mechanical behavior of the RF-MEMS switch. These tests cannot be considered as qualification tests because the technology development and the optimization are still ongoing during these tests. Therefore, the results of these tests should be used as a starting point in order to help the process optimization before freezing the technology.

Reliability tests of RF-MEMS switches are mostly done by measuring the electrical performance during billion times of operations. Although the expected operation of the switch is in the electrical domain, observing the dynamic behavior of the switch after billions of cycles also gives very important hints to understand the failure mechanism of the RF-MEMS switches. During the reliability tests, the on-wafer measurement techniques under ambient conditions are used together with the LDV technique for twelve structures working in parallel. The switches are actuated with a frequency of 33.3 kHz and an electrode voltage of 45 V. The dynamic behavior of all the single switches is detected and saved every 10 minutes which means every 20 million switching cycles. Total membrane displacements, switch-on and -off times are extracted from the saved data. Figure 6.7 shows the twelve test switches used for the reliability tests.
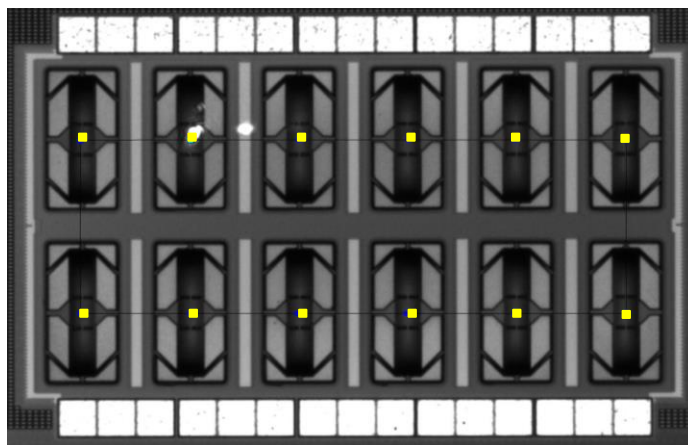


Figure 6.7 Micrograph of the RF-MEMS switches for reliability measurements [113].

The yellow nodes in Figure 6.7 indicate the measurement point of LDV. Figure 6.8 shows the membrane displacement versus time curves of the switches up to 50 billion times of switching which takes approximately 18 days. The measurement results of the twelve RF-MEMS switches are appended on Figure 6.8.
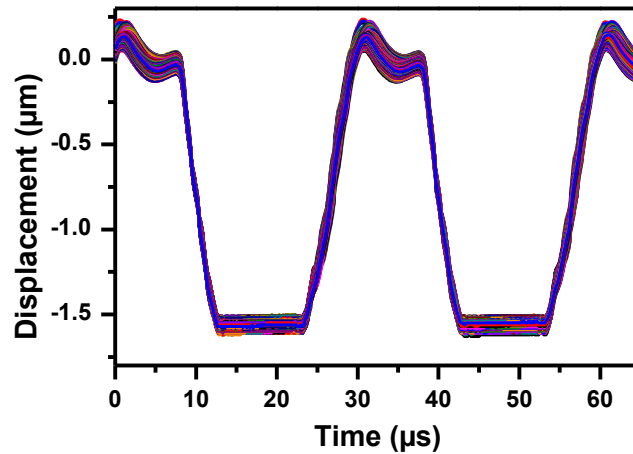


Figure 6.8 Displacement of the membrane versus time curves of the twelve RF-MEMS switches after every 20 million times of switching, up to 50 billion time operation. The curves are extracted after every 20 million and the graph shows the overlay of all the curves for different number of cycles of all 12 RF-MEMS switches [113].

The membrane displacement and the switch-off time versus number of switching cycle data are given in Figure 6.9. Figure 6.9 clearly shows that the switch starts with an initial displacement of around 1.55 µm and after 20 billion of switching; the displacement decreases approximately 25 nm and achieves its final value of 1.525 µm. After this burn-in effect, it provides very reliable switch behavior up to 50 billion switching cycles.

The switch-off or release time of the RF-MEMS switch also gives very important information because a potential stiction can be foreseen with the increase of the release time of the switch which helps to eliminate many unnecessary reliability tests. The release time performance of the switch can also be seen in Figure 6.9. Similar burn-in effect can also be pronounced up to 20 billion of switching cycles. After this value, RF-MEMS switch again provides stable release time performance, below 5 µs.
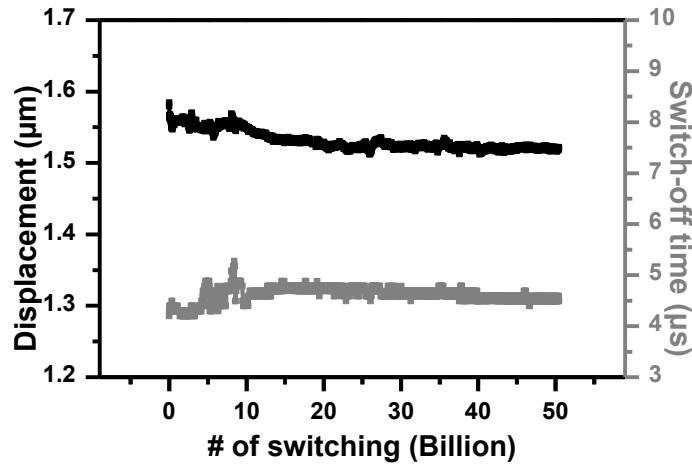
Figure 6.9 The membrane displacement and the switch-off time versus number of switching cycles of single RF-MEMS switch [113].

A further reliability test is performed to investigate the impact of actuation pulse duration on switch-off time. Every application has a specific requirement, i.e. T/R switch applications need very short pulse durations and very high switching speeds but imaging applications may need longer pulse durations and slower operation. Therefore, the release time of the switch is also investigated for the different length of the pulses. Figure 6.10 shows that the raise of the pulse duration slightly increases the switch-off time and it does not significantly change the release performance.
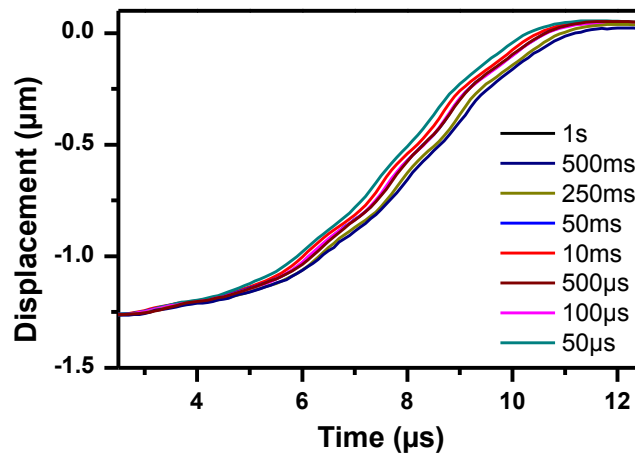


Figure 6.10 Displacement of the membrane versus time curves for different pulse durations between 50 µs to 1 s [113].

## 6.5 Conclusion

In Chapter 6, the robustness and the reliability of the embedded RF-MEMS switch have been presented. The change of the contact capacitance at up and down states is characterized with respect to the temperature, between -30 and 150 °C. The effect of the temperature on pull-in voltage has also been studied. No significant change has been observed for these three performance figures. As another robustness performance figure, the power handling of the switch has been investigated. Self-actuation of the switch under DC signal condition has been examined. The maximum DC biasing levels and RF power handling parameters have been extracted to prevent latching. Lastly, the reliability tests have been performed using the optical measurement technique to better understand the behavior of the switch. Different conditions such as fast cycling or longer pulses have been applied and the displacement information with contact capacitance value has been monitored. The switch provides almost the same performance parameters up to 50 billion cycles. In similar case, the long duration pulses have not changed the release characteristic of the switch.

In this thesis, optical techniques have been used for reliability tests. The main advantage of the using optical measurement technique is the full information of the dynamic behavior of the RF-MEMS switch. Such measurements provide information about not only the failure case but also potential degradation which can occur in early phase of cycling; e.g. increase of the release time of the switch or decrease of the total displacement.

The configuration of separated electrode and the dielectric-less actuation used in this study significantly helped to achieve the presented reliable operation. The height difference between the contact and the high voltage electrodes, which is studied in Chapter 2, provides a specific gap between the membrane and the high voltage electrode. By the help of this gap, no dielectric layer is necessary to isolate the high voltage. Therefore, the potential failures due to the charging of the dielectrics are prevented.

All the robustness and reliability tests need significant investment and huge effort. In order to decrease the development time and cost, all these tests need to be done as a qualification tests after packaging the device. Nevertheless, tests during the process development also provide valuable information to fine tune the device before finalizing the process development.

To conclude Chapter 6, most of the problems related to reliability issues have been solved for the last 10 years. Many new materials and different concepts have been used in RF-MEMS switches to improve the reliability. There is no RF-MEMS switch which can satisfy all the reliability specifications of different applications. The reliability requirements of every application are different. Therefore, it is very important to define the reliability requirements before the development of the process to decrease the cost and the effort for the process development.

# 7 Mm-wave Design Examples

## 7.1 Introduction

The BiCMOS embedded RF-MEMS switches have opened the way for many high performance and re-configurable mm-wave circuits that cannot be realized using standard BiCMOS components. Re-configurability may allow a mm-wave system to assume different functions. For instance, a system could work as a car-to-infrastructure transceiver at 60 GHz while a vehicle is in motion, but it could act as a close range radar system at 79 GHz during slow-moving or parking. Likewise, a system could be optimized to work in both bands of the E-band "wireless fiber" allocation now becoming increasingly popular for LTE (Long-Term Evaluation) base station backbone links. Or, re-configurability could result in commodity building blocks for mm-wave systems, addressing a wide spectrum of frequencies or applications [114].

The main advantage of having the RF-MEMS switches in a BiCMOS environment is the easy integration with the other circuit components such as transistors, resistor and capacitors. This allows designing RF circuits in a BiCMOS environment using the RF-MEMS switch as a standard circuit component that can be picked up easily from the design kit of the foundry. It literally paves the way for re-configurable mm-wave circuits in the BiCMOS environment; hence opens many different new system concepts for mm-wave applications. Many problems and limitations of RF-MEMS devices can only be recognized when they are used in circuits and systems. However, it is very challenging to design RF-MEMS embedded circuits considering the preliminary inaccurate RF-MEMS models.

The integration of a new device model into a design-kit is a straightforward task as long as the technology of the device is stabilized. Since the RF-MEMS devices can be easily affected by the process conditions, providing a stable RF-MEMS device model is not easy and can take long time. Furthermore, the device is endlessly under optimization and the model of the device changes after every process update. This makes the design of RF-MEMS embedded circuits very challenging. Therefore, the basic know-how of the circuit designer on RF-MEMS devices is very important to design RF circuits with sufficient RF performance using conservative device models.

Chapter 7 summarizes the passive and active mm-wave circuits realized using the developed RF-MEMS switch. Section 7.2 starts with the passive design examples such as absorptive single-pole-single-throw (SPST) and reflective single-pole-double-throw (SPDT) switches. The way of preparing the test circuits in order to check the device model together with accurate simulation methods are also provided in section 7.2. Section 7.3 gives the design examples of the active circuits including the RF-MEMS switches. The design of all the active circuits has been done by Dr. A. Cagri Ulusoy and Dr. Gang Liu under the supervision of Prof. Dr.-Ing. Hermann Schumacher, University of Ulm (UUlm), Germany. The initial RF-MEMS switch models have been provided to the UUlm group and the circuits have been designed based on the initial models. Section 7.4 concludes the chapter and summarizes the main achievements.

## 7.2 Passive Circuits

The development of RF-MEMS devices have been mostly done using pure MEMS processes, means without any active device. Therefore, most of the circuit examples using RF-MEMS switches in the literature are based on passive circuits such as SPSTs, SPDTs, single-pole-multi-throws (SPnT), passive phase-shifters and impedance tuners.

Microwave and mm-wave SPnT switches have been traditionally designed using PIN diodes or FETs, but both technologies have some drawbacks such as high power consumption or cost intensive production. RF-MEMS switches are well suited to realize SPnTs at higher frequency applications. In this section, two circuits are given as design examples: Absorptive SPST at 50 GHz and reflective SPDTs at 30, 50, 80 and 100 GHz.

### 7.2.1 The Absorptive SPST

Q-band satellite communication is one of the most interesting applications where absorptive SPnTs are required. Several absorptive switches are realized at lower frequencies with insertion loss values of 1 to 2 dB using RF-MEMS on high resistive silicon substrates [115], PIN diodes [116] or active devices [117, 118].

By the help of the inductive loading technique, the RF-MEMS switch with a maximum isolation at 45 - 50 GHz frequency band is achieved, as explained in section 3.4.2. The RF-MEMS switch provides approximately 1 dB insertion loss and 20 dB isolation in the desired frequency band (Figure 3.31). Although similar switches have provided less than 0.5 dB insertion losses using the same technology [92], the substrate conditions dominate the capacitive loss for this run which is detailed as follows.

The integration of the RF-MEMS switch module into the BiCMOS process is realized using the BEOL metallization layers of the BiCMOS process. Therefore, for *"BEOL-only"* short runs, processing of BEOL is enough to have the RF-MEMS switch structures. However, for absorptive SPST, a 50 Ω resistor with very low parasitics is required, means the full BiCMOS process needs to be run. The main difference between the *"BEOL-only"* short run and the full BiCMOS run is the substrate conditions, particularly the resistivity of the substrate. The BiCMOS processes include several implantation steps to control the resistivity. The typical resistivity of a blank silicon substrate is around 50 Ω-cm, which is the resistivity of the substrate for the *"BEOL-only"* runs (Figure 7.1). However, the resistivity value can vary between 50 Ω-cm and few tens of mΩ-cm, depending on the used implantation steps in the full BiCMOS process. One of the most critical implantation steps which dominate the substrate resistivity is the p-well implantation. Although the p-well implantation changes only the resistivity of the first 1 to 2 μm depths from the surface (Figure 7.1), the resistivity levels of the substrate can decrease by several orders of magnitude which significantly changes the RF performance of the switch. The effect of the p-well can easily be avoided by using the *"p-well block"* mask. This mask is already included into the p-cell of the switch in the design-kit for future runs but has not been included for the process run which is used in this particular absorptive SPST fabrication.
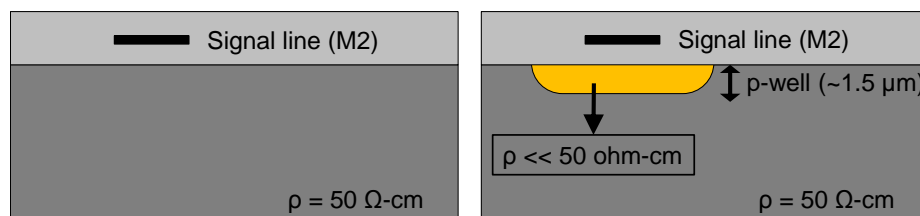


Figure 7.1 The substrate conditions for the short flows (left) and the full BiCMOS process flow (right) when the *"p-well block"* mask is not used [119].

To validate the RF-MEMS switch model, the simple reflective SPST switch is also designed and fabricated. The simulation setup in Agilent ADS and the fabricated reflective SPST switch is given in Figure 7.2. The transmission lines are simulated using 2.5D momentum solver. The measured and open/short de-embedded RF-MEMS switch model is used in simulations. The microstrip type transmission lines are realized using TopMetal2 as the signal line and Metal1 as the ground plane, in the BEOL stack of IHP's SG25H1 process. The width of the microstrip is taken as 15 μm to obtain 50 Ω line impedance at the desired frequency band [119].
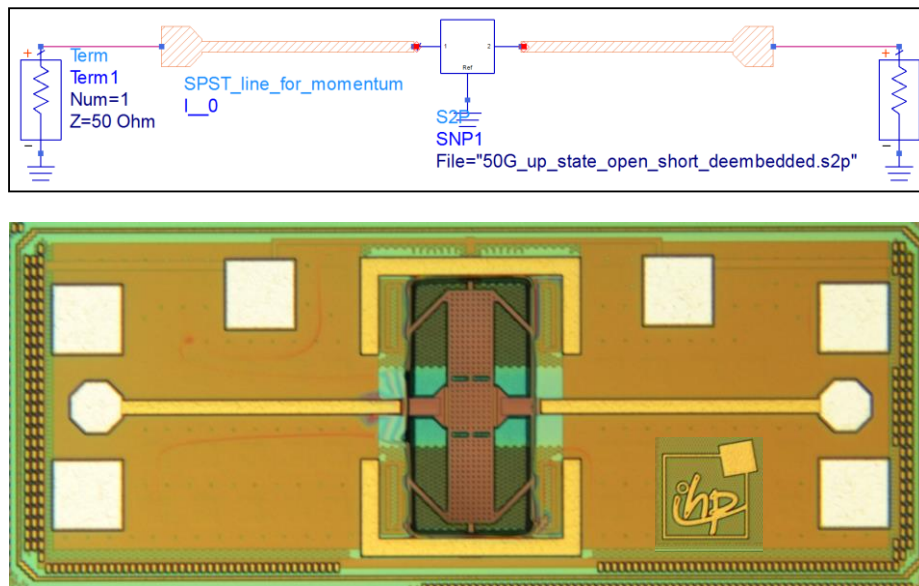


Figure 7.2 The simulation setup in Agilent ADS (top) and the microphotograph of the fabricated 50 GHz reflective SPST switch (bottom) [119].

Figure 7.3 shows the measured results of the reflective SPST switch for 10 different chips over 8-inch wafer. The results show 1.3 dB insertion loss and 15 dB isolation at 45 GHz. As expected, the insertion loss value of the reflective SPST is approximately 0.3 dB higher than the standalone RF-MEMS switch due to the additional loss coming from the transmission lines with a total length of 600 μm. As can be seen from Figure 7.3, the simulated results are in a good agreement with the measured ones, especially up to 60 GHz.
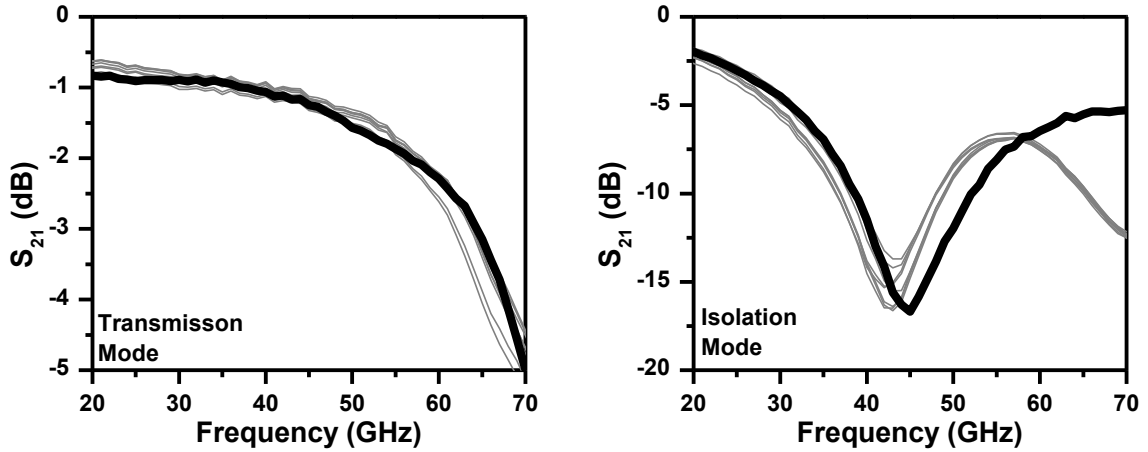
Figure 7.3 The measured and the simulated results of the reflective SPST. The gray curves are the measured samples and the black curves are the simulated results using the measured RF-MEMS switch model [119].

After having a good agreement between the simulated and the measured results of the reflective SPST, the absorptive SPST design and the simulation setup is initiated. The schematic view of the absorptive SPST switch is given in Figure 7.4. The switch provides a short between in and out (transmission mode) when the switch-1 is open (up-state) and the switch-2 and the switch-3 are shorted (down-state). The switch-2 and the switch-3 together with the transmission lines in the lower branches provide an open circuit since the $\lambda/4$ transmission lines are shorted to ground by RF-MEMS switches. Although these lower branches are supposed to provide open circuits, due to the non-optimized transmission line lengths, a specific loss always occurs in these branches. In the second state, the switch provides open between in and out (isolation mode) when the switch-1 is in short (down-state) and the switch-2 and the switch-3 are in open (up-state). In this state, the input and the output are isolated by the help of $\lambda/4$ transmission lines and the switch-1 in the upper branch. 50 $\Omega$ impedance matching for both the input and the output is provided by on-chip 50 $\Omega$ resistors, at the end of switch-2 and switch-3. This topology provides flexibility to match or un-match the input and the output for both the transmission and the isolation modes.
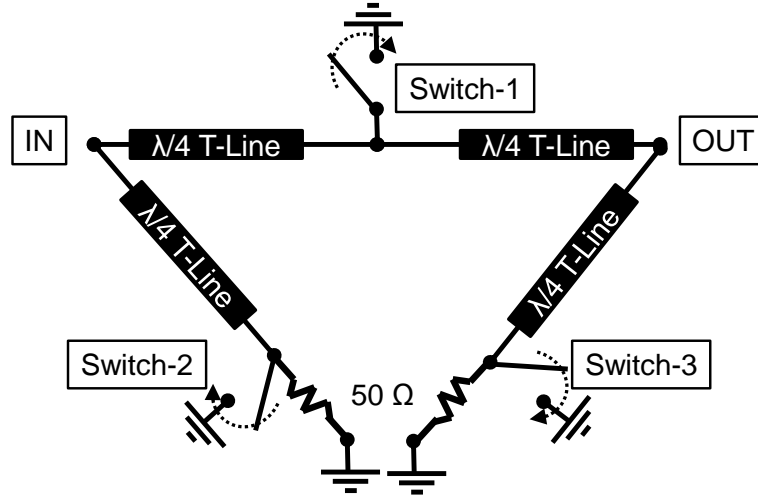
Figure 7.4 The schematic view of the absorptive SPST using capacitive type RF-MEMS switches [119].

The simulation setup of the absorptive SPST is given in Figure 7.5. The measured and open/short de-embedded RF-MEMS switch models are used during the simulations, as shown in Figure 7.5. A poly-silicon type of resistor in the BiCMOS process is used to realize the 50 Ω resistor, optimized for minimum parasitic capacitances to ground. The fabricated chip photo of the absorptive SPST is given in Figure 7.6.
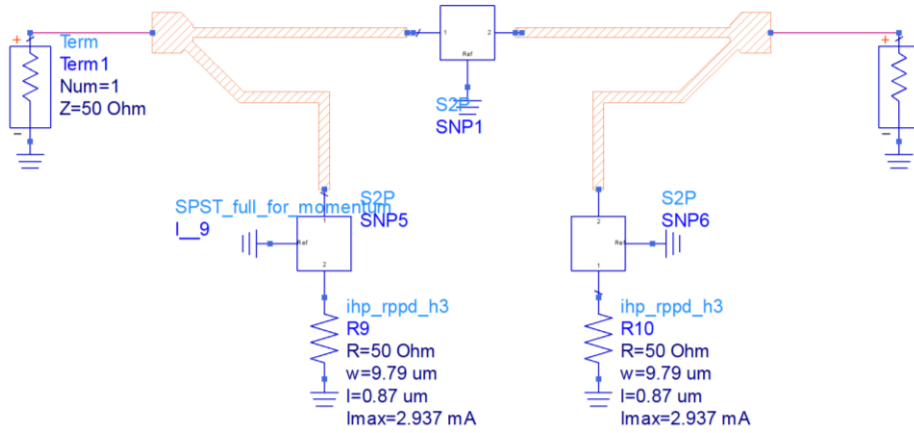


Figure 7.5 The simulation setup of the absorptive SPST in Agilent ADS [119].
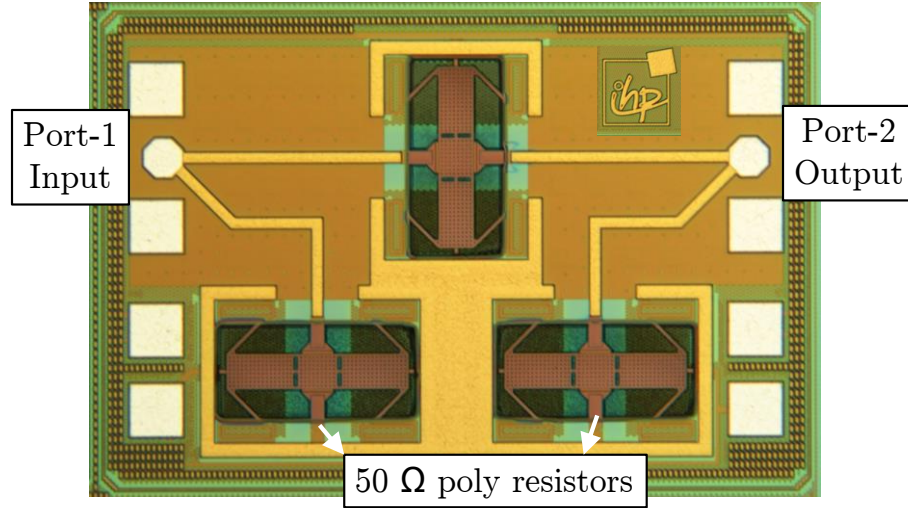
Figure 7.6 The microphotograph of the fabricated 50 GHz absorptive SPST switch [119].

Figure 7.7 shows the measured and the simulated S-parameter results of the absorptive SPST switch. In the transmission mode, 2.5 dB insertion loss is measured (Figure 7.7a). For this mode, both the input and the output are well matched to 50 $\Omega$ (Figure 7.7b, c). As previously explained, the standalone RF-MEMS switch has 1 dB insertion loss and the reflective SPST switch with the same transmission line length has a loss of 1.3 dB which is 1.2 dB lower than the absorptive SPST switch. These results show that additional 1.2 dB loss comes from the lower branches. These lower branches are expected to be open circuit at this frequency but the experimental data show an additional loss at these branches. The reason of the unexpected loss can be explained with the non-optimized transmission lines in the lower branches. It is possible to minimize the loss at these lower branches by optimizing the transmission lines using a better model of the RF-MEMS switch.

In the isolation mode, the absorptive SPST provides better than 20 dB isolation at the interested frequency band (Figure 7.7d). In this mode, the input and the output are well matched to 50 $\Omega$, demonstrating the absorptive behavior of the SPST switch (Figure 7.7e, f). The input or the output can be used as reflective or absorptive by the help of RF-MEMS switches at the lower branches. Although a small frequency shift is observed between the simulated and the measured results of $S_{11}$ and $S_{22}$, in general they are in a good agreement.
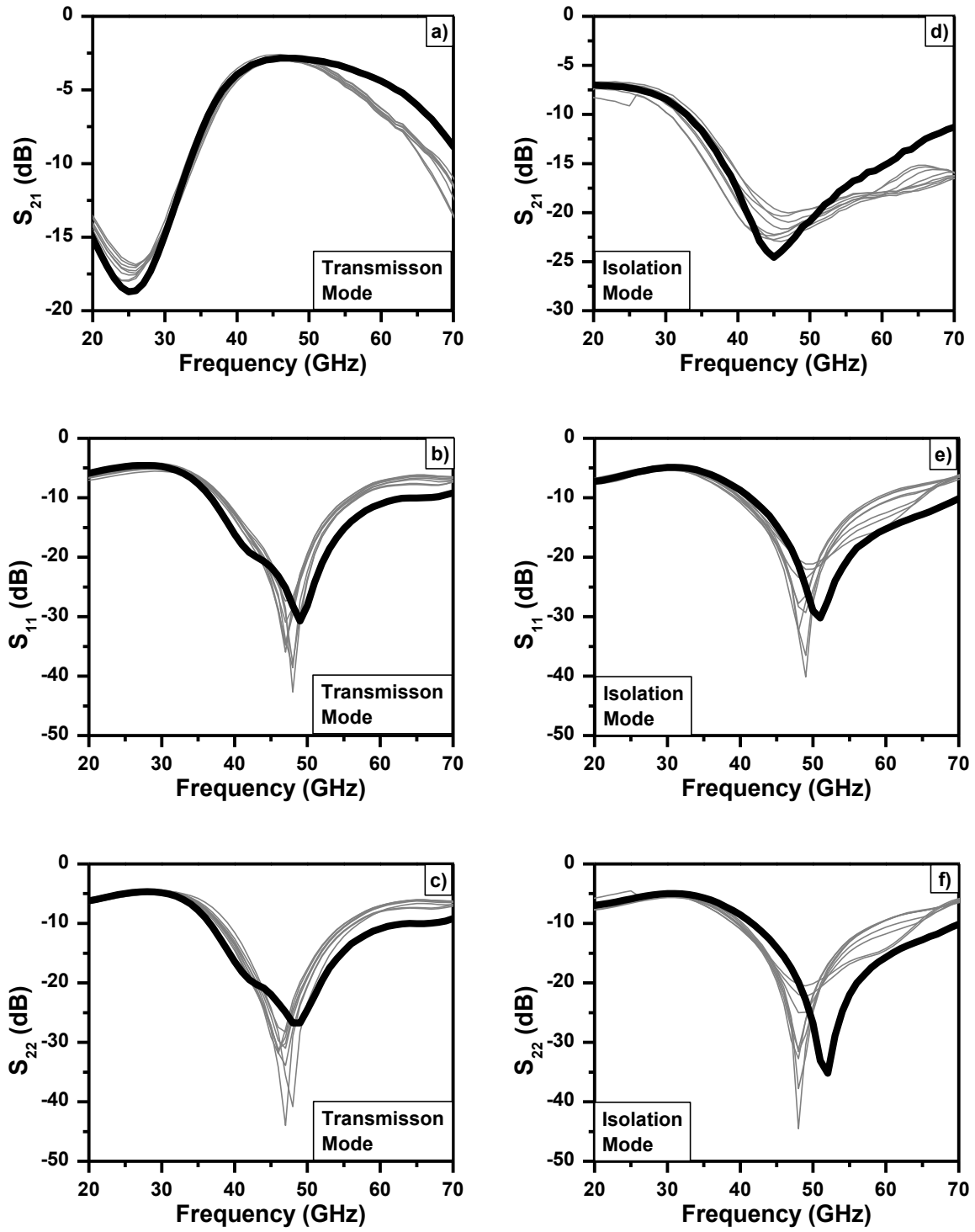
Figure 7.7 The measured and the simulated results of the absorptive SPST switch. The gray curves are the measured samples and the black curves are the simulated results using the measured RF-MEMS switch model [119]. Transmission mode (a, b and c) and isolation mode (d, e and f).

## 7.2.2 The SPDTs

Apart from the absorptive SPST, reflective SPDT switches for different frequency bands have also been designed using the developed RF-MEMS switches. The SPDTs have been formed by two quarter-wavelength transmission lines terminated by the RF-MEMS switches, similar to the absorptive SPST explained in section 7.2.1. Figure 7.8 shows the SPDTs fabricated for four different frequency bands: 30, 50, 80 and 100 GHz. Since the SPDTs do not need any resistor or active device, the fabrication of these circuits has been done using the BEOL run (short flow).
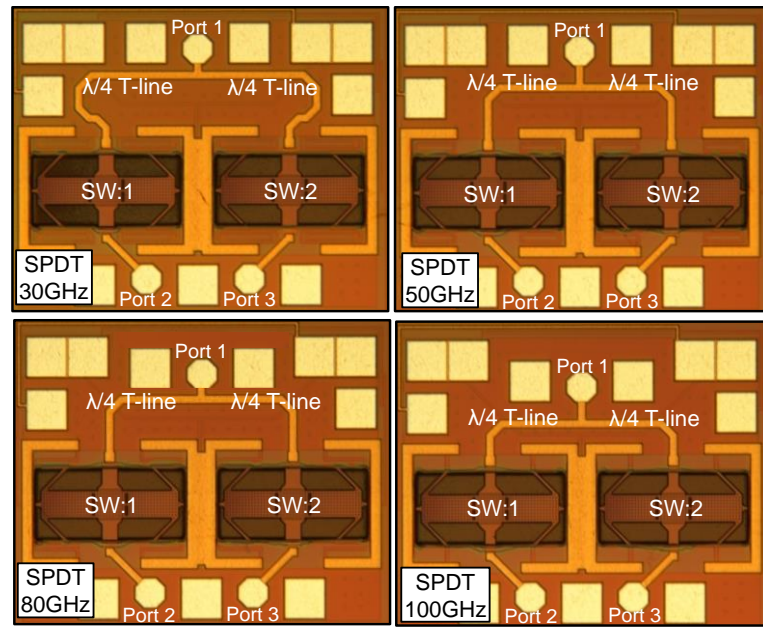


Figure 7.8 The microphotographs of the SPDTs for 30, 50, 80 and 100 GHz. Every SPDT uses the appropriate RF-MEMS switch at the desired frequency [92].

Figure 7.9 gives the measurement results of the SPDTs. The results show excellent RF performance parameters, such as less than 1 dB insertion loss and better than 20 dB isolation. The achieved results are far beyond those of the state-of-the-art SPDTs based on the silicon technologies [120, 121, 122]. Furthermore, the results can be still improved in future designs by further optimization of the transmission lines if a better RF-MEMS switch model with more accurate phase information is used.
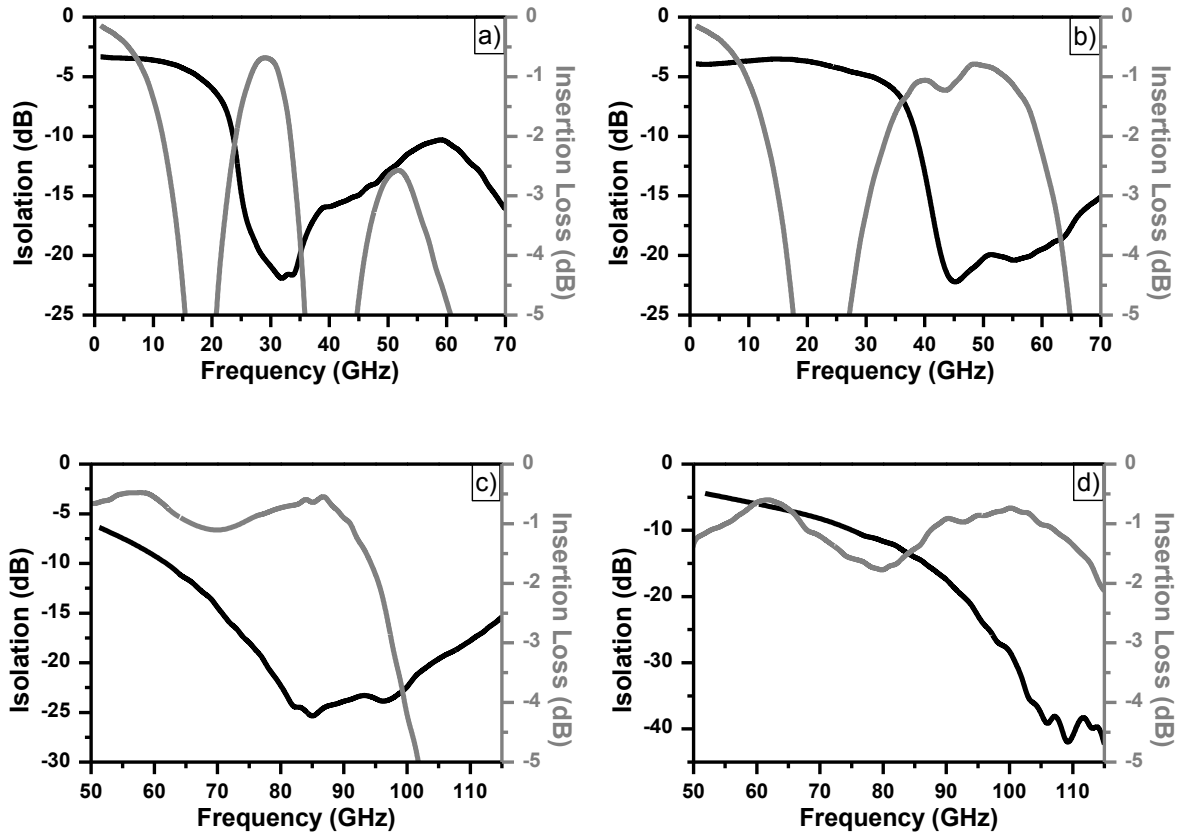
Figure 7.9 The measured (de-embedded) S-parameters of the SPDTs tuned for 30 (a), 50 GHz (b), 80 GHz (c) and 100 GHz (d) [92].

## 7.3 Re-configurable Active Circuits

Design of passive circuits using RF-MEMS switches significantly helps to understand limitations and high voltage biasing conditions of RF-MEMS switches. It also shows the importance of the RF-MEMS switch model in the final circuit. However, these passive circuits mostly do not include any internal biasing conditions. In contrast, the active circuits need DC biasing and this might change the performance of the RF-MEMS switches, as studied in Chapter 6. In this section, the dual-band LNA switching between 24 and 77 GHz and the dual-band VCO switching between 50 and 70 GHz are demonstrated.

## 7.3.1 The Dual Band mm-wave LNA

RF circuits can be re-configured between different bands with a significant frequency offset. To switch from one frequency to another, there is a need for a switching component in the circuit to re-configure the load, the input matching and the output matching of the circuit. This particular circuit is motivated by the fact that short range radars for automotive applications now employ two different bands - around 24 and 79 GHz. The low-noise amplifier shall address both bands, using a switched resonant load. Therefore, the SiGe BiCMOS dual-band LNA using the RF-MEMS switches has been designed [123].
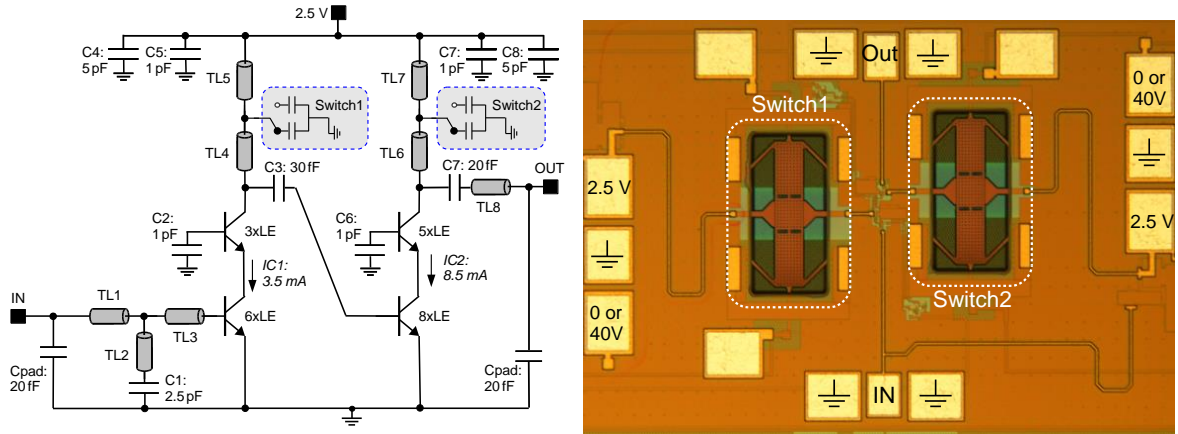


Figure 7.10 The 24/77 GHz band-switched low noise amplifier. The schematic diagram (left) and the chip micrograph (right) [123].

The LNA is realized using a two-stage cascode topology (Figure 7.10, left). The input circuit has been chosen such that it provides reasonable power and noise match both at 24 and 79 GHz. Thus, only the loads have to be switched. The loads are resonant circuits formed by the thin-film microstrip transmission lines [123].

The fabricated circuit (Figure 7.10, right) has shown experimental results quite close to the simulation, and featured 25 dB gain with 4.3 dB noise figure at 24 GHz, and 18 dB gain with 8.3 dB noise figure at 77 GHz. The S-parameter performance distribution of the LNA over 8-inch wafer is shown in Figure 7.11. The small variance shows the good uniformity of the BiCMOS embedded MEMS process.
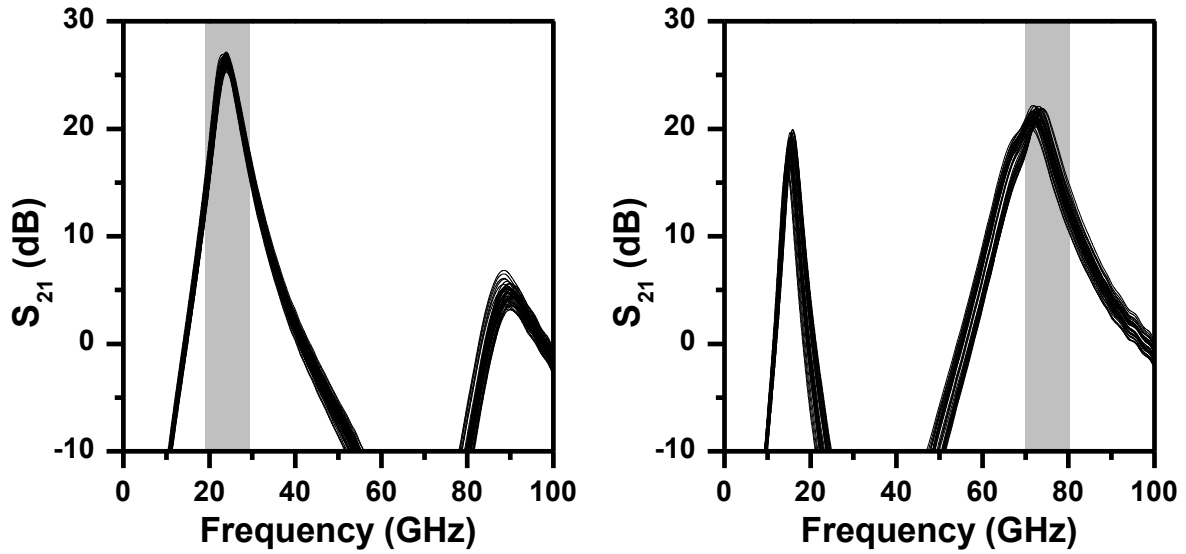
Figure 7.11 The measured $S_{21}$ versus frequency curves for up (left) and down (right) states of the LNA with variation of > 45 samples over an 8-inch substrate. The gray regions indicate the interested frequency bands [123].

## 7.3.2 The Dual Band mm-wave VCO

As a second example, a dual-band VCO has been designed. The circuit is a Colpitts-type differential VCO. As Figure 7.12 (left) shows, it includes a differential common base buffer stage and a divide-by-64 block on-chip, facilitating the measurements of phase noise as well as transient frequency switching behavior. The base inductors are modified by the introduction of the two RF-MEMS switches.

In the absence of a design-kit, the switch parameters have been obtained by the help of EM simulations and the preliminary measurements. Figure 7.12 (right) shows the chip micrograph, indicating the large size of the RF-MEMS switches. The relatively large size of the RF-MEMS switch creates a layout challenge for mm-wave circuits. The overall chip dimensions, however, are still reasonable (1 x 0.86 mm$^2$) [124].
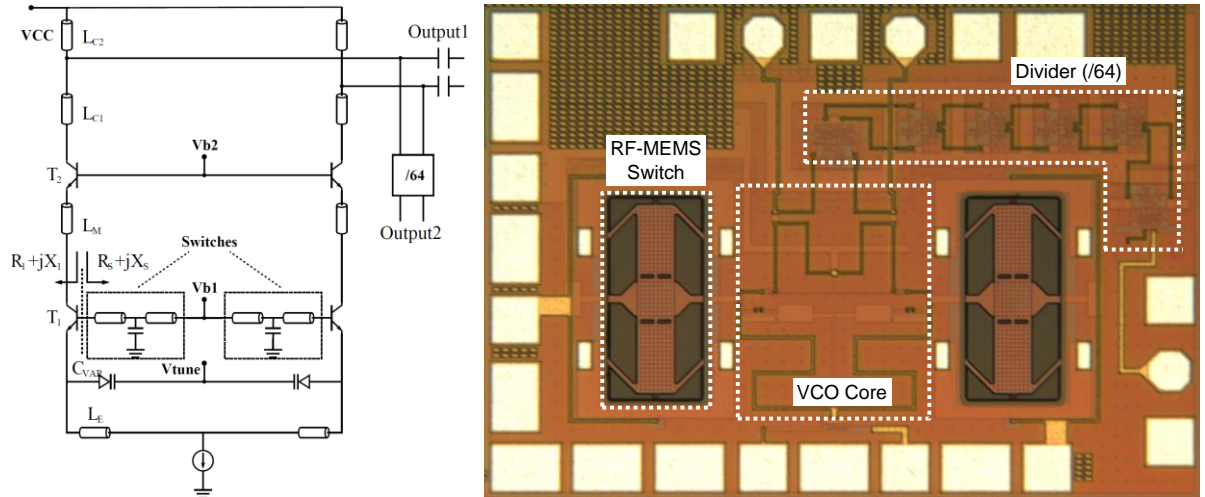
Figure 7.12 The schematic diagram of the mm-wave Colpitts oscillator (left) and the micrograph of the fabricated chip (right) [124]

Figure 7.13 shows the VCO tuning characteristics for the lower band (both switches are in up-state) and the upper band (both switches are in down-state). Compared to the simulations, the tuning range in each band is shifted downward, as a result of switch parasitics which have not been taken into account for the initial model. The phase noise has been measured at the divide-by-64 port, and determined to be -82 dBc/Hz at 1 MHz offset in the lower band, and -84 dBc/Hz in the upper band, after correcting the shift introduced by the divider (Figure 7.14).
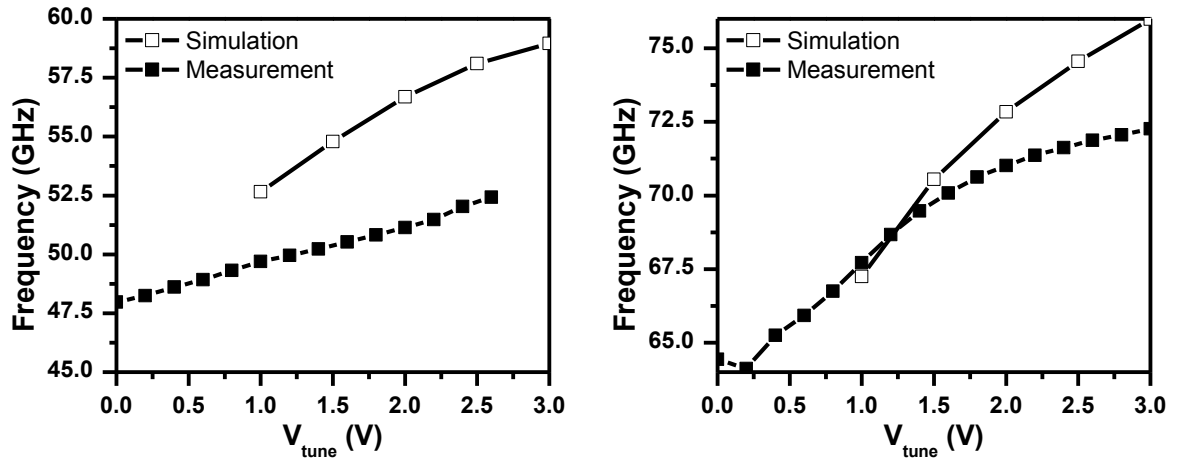


Figure 7.13 The simulated and measured tuning ranges of the re-configurable VCO. The RF-MEMS switches are in the up-state (left) and in the down-state (right) [124].
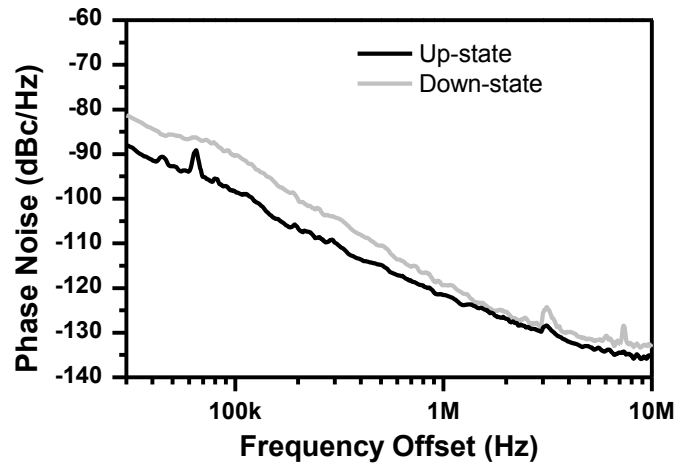
Figure 7.14 The measured phase noise from the divided output [124].

To analyze the dynamic behavior of the circuit and the RF-MEMS switch, rectangular pulses (50 % duty cycle, below 10 ns rise/fall time) have been applied to the high voltage electrode of the switch. The divided output is monitored using a signal source analyzer. Figure 7.15 shows the measurement result of the divided oscillation frequency versus time behavior. As the switch is continuously switched "on" and "off", the divided frequency also switches periodically between 800 MHz (51.2 GHz fundamental frequency) and 1.125 GHz (72.04 GHz fundamental frequency).
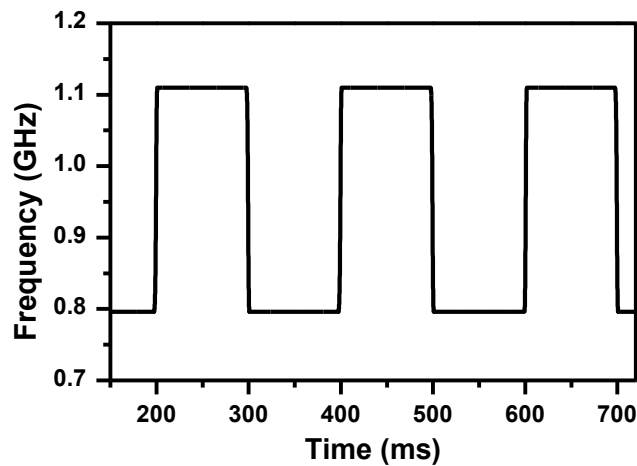


Figure 7.15 The measured oscillation frequency of the VCO from the divided output when periodic pulses are applied to the switch [124].

To better understand the behavior of the VCO and the RF-MEMS switch, the LDV has been used and the movement of the membrane has been monitored (Figure 7.16).
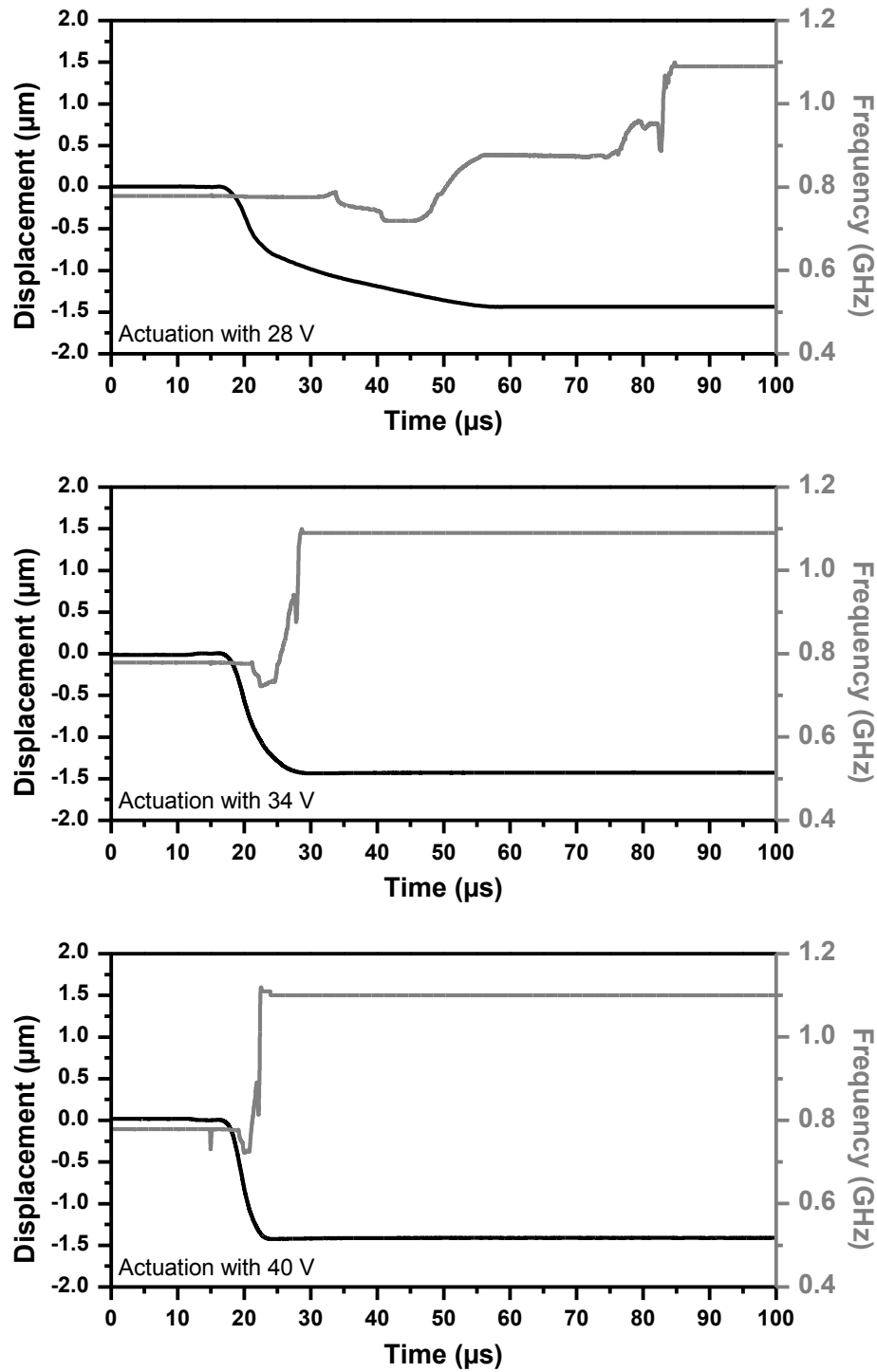


Figure 7.16 The measured displacement of the membrane and the divided output frequency for different electrode voltages. The total deflection is around 1.4 μm [124].

Figure 7.16 shows the measured membrane displacement and the oscillation frequency (divided) versus time for different actuation pulse voltages. For 28 V pulse, the switching time is roughly 40 µs and it decreases to 10 µs for 34 V pulse and 4 µs for 40 V actuation pulse. When the membrane starts to move down, the output frequency first decreases to the self-oscillation frequency of the frequency divider, because the VCO output power at the switching transient is not sufficient to drive the frequency divider. Then, the output frequency follows the VCO and starts to increase, as the membrane continues to move down. When the membrane is completely down, the output frequency remains constant, showing that the VCO operation is very stable.

## 7.4  Conclusion

In Chapter 7, the mm-wave circuit design examples using the developed RF-MEMS switch has been presented. The design flow of the absorptive SPST has been given and the importance of the accuracy of the RF-MEMS switch model has been shown. The SPDTs at 30, 50, 80 and 100 GHz have also been shown with the performance figures of less than 1 dB insertion loss and more than 20 dB isolation. The re-configurability using the RF-MEMS switches has been demonstrated by the active circuits; namely the dual-band LNA and the VCO. By the help of the RF-MEMS switches, the operating frequency of the LNA has been shifted from 24 to 77 GHz, without any additional external component. Similarly, oscillation frequency of a VCO has also been switched between 50 to 70 GHz. The circuits have shown the easy use of BiCMOS embedded RF-MEMS switches in the mm-wave circuits.

The first DC latching problem of the RF-MEMS switch was observed during the characterization of the dual-band VCO, designed in this chapter. The VCO could be switched from low-to-high frequency but not vice versa. However, after switching off and on the supply voltage of the VCO, the oscillation frequency has come back to higher frequency. The reason of the latching was the 2 V DC voltage at the signal line of the RF-MEMS switch since the switch is connected to the oscillation node of the VCO.

To conclude Chapter 7, the best way to investigate the problems and the limitations of a new device is to use it in circuits as early as possible. Many different effects such as latching due to the DC voltage can only be seen with the help of the circuits. The

size of the switch in newer versions is tried to be minimized which make the use of it easier. As a final remark, the most important point is providing not only the best performance device but also a useful device from the circuit design point of view.

# 8  Conclusions and Future Directions

## 8.1  General Remarks

In this section, general achievements and remarks for the each chapter is given. The main challenges and the potential solutions are also provided in this section.

### 8.1.1  Technology

- Considering high processing and engineering costs of developing any RF-MEMS device, the strategy of the development needs to be well organized in advance. The first rule is to define the fabrication platform of the device, whether it is a standalone platform or CMOS/BiCMOS integration. The size and the type of the market (mass production, niche application and etc…) as well as the requirements of the RF-MEMS device (need of high voltage, low parasitic connection to CMOS and etc…) are the most important points to decide about the integration platform.

- Repeatability issues can only be solved by stable fabrication environments. Most of the excellent RF-MEMS devices are fabricated in unstable production environments which make the commercialization very challenging. Therefore, before starting the RF-MEMS device development, stable and well-controlled fabrication environments should be chosen. CMOS and BiCMOS platforms are evidently among the most stable environments for RF-MEMS fabrication, as preferred in this thesis as well.

- Uniformity issues strongly depend on the way of fabrication of the device. There can be several different process flows to realize the same RF-MEMS device; however, some of them are more robust against process variations than others. Therefore, the process flow of any RF-MEMS device needs to be optimized by a process specialist in advance and critical/sensitive steps should be eliminated from the beginning of the development.

- The yield problems are always pronounced in CMOS processes. In order to minimize the cost of a single RF-MEMS device or a more complex circuit including RF-MEMS device, the yield needs to be very high, i.e. more than 95 %. The yield is mostly related to the uniformity of the process steps and can be increased by less sensitive and more uniform process steps. If the device is integrated into a CMOS or BiCMOS platform, then another point which needs to be taken into account is the effect of the additional MEMS process steps on standard CMOS devices. Therefore, the yield can be considered as a single device yield for standalone RF-MEMS processes but it should be considered as a CMOS and RF-MEMS yield for BiCMOS integrated RF-MEMS devices.

## 8.1.2  Modeling and Characterization

- In most of the studies, the material properties are taken from the literature as a fixed value and the FEM simulations are performed based on these values. However, most of the material properties are dependent on the process conditions and need to be extracted specifically to the each process.

- RF-MEMS switch modeling is a multi-disciplinary study and needs to couple the following domains: electrical, mechanical and RF. There are only few FEM solvers which can couple those domains. However, it is not the optimum way to model all the domains in a single model. Therefore, the modeling strategy is very essential and appropriate simulation tools should be used for different domains. In this thesis, the material/fabrication domain has been separated from the others. Electrical and mechanical domains have been coupled to analyze the static and dynamic behavior of the switch. The RF domain is also separated as a standalone domain because the very high frequency of operation needs a special attention.

- The electromechanical domain is one of the most difficult domains simulate due to the non-exact material properties. However, if enough attention is given to extract these parameters, very accurate FEM simulation results can be achieved.

- EM simulations are more straightforward than the electromechanical ones since the required material parameters are simpler than that of the electromechanical ones. Basic information such as conductivity, dielectric constant and loss tangent are enough to do EM simulations.

- If the frequency of interest is beyond 60 GHz, serious electromagnetics knowledge is necessary to optimize RF-MEMS devices because the dimensions of the devices are comparable with the wavelength of the operating frequency, making the modeling very difficult. In addition, the substrate in use has also a very significant effect. Highly resistive substrates provide very good RF performance and it helps to achieve more accurate simulation result. However, using of low resistive substrates, which is required for the existing BiCMOS technology, can degrade the RF performance and it makes the simulations more complicated at mm-waves due to the undesired substrate modes.

- Planar EM solvers, which are also known as 2.5D simulators, can provide very accurate data for RF-MEMS devices up to specific frequencies depending on the substrate and on the model but air cavities of RF-MEMS devices create a non-uniform horizontal plane which makes it very difficult to simulate using planar EM solvers. The effect of the non-uniformity at horizontal plane becomes more significant at frequencies beyond 80 GHz. Therefore, 3D EM solvers are recommended for mm-wave, especially if a low resistive ($< 100$ $\Omega$-cm) substrate is used.

## 8.1.3 Packaging

- Packaging of RF-MEMS devices is one of the most critical steps of entire process flow development. Therefore, the complete process flow development of the device should be done by considering the packaging of the RF-MEMS device.

- The effect of the package becomes more significant as the operating frequency of the device increases due to the fact that the loss coming from the package has more effect.

- It is noted that if the RF-MEMS device is realized in a CMOS or BiCMOS environment, an additional limitation for packaging arises from the thermal budget of these technologies.

- Most of the RF-MEMS devices need hermetic packages and having a hermetic package helps to stay on the safe side. However, with respect to the expected performance and reliability figures, required hermeticity levels can change.

- The RF-MEMS device type is defined by application, and has in turn an important impact on the packaging requirements. For instance, the hermeticity is very crucial for ohmic type of switches. However, humidity and hence the level of the hermeticity are also critical effects for the capacitive type of switches.

- Cap-to-wafer type of packaging has the disadvantage of low throughput. If the application is medium or high volume of production, cap-to-wafer type of packaging process cannot be a good choice.

- Wafer-to-wafer packaging process looks very promising with high throughput. The initial tests show a very successful packaging of RF-MEMS devices. However, a detailed yield analysis should be done in order to see the quality of bonding process over the wafer. Any small yield drop due to the packaging process can significantly affect the final cost.

## 8.1.4 On-Chip High Voltage Generation

- Latest RF-MEMS products have shown the importance of the high voltage generation and control circuits such as SPI and I2C. Despite the fact that the community has been expecting the combination of RF tuners with high performance front-end technologies (90nm and below), the integration of RF-MEMS tuners to a CMOS platform has been realized with a 0.35 μm BiCMOS platform to get the advantage of high voltage operation.

- Most of the products are still using a charge-pump approach to achieve high voltages in a CMOS environment. This approach is quite suitable; especially considering that RF-MEMS devices need no current, behave like an open circuit. However, in order to increase the voltage up to 50 V or more circuits, many stages (e.g. > 20 stages) are necessary which increases the area; thus the cost.

- Similar to the other CMOS based products, one of the main obstacles for the RF-MEMS devices is the cost per chip, which is mainly related to the chip area. Although RF-MEMS devices are larger devices compared to the other semiconductor devices, the need for a charge-pump and control circuitries increases the total required area and cost. Therefore, large area charge-pumps can satisfy the current requirements but there might be a need for smaller area charge pumps and control circuits in near future.

- One way to decrease the area of the high voltage generation circuits is use of high breakdown voltage transistors, e.g. LDMOS, because the high drain to source breakdown of these transistors can increase the voltage larger in each stage, thus, the number of stages of charge pumps can be significantly reduced. Such transistor can be achieved with special process development in BiCMOS. SOI technologies are also promising to provide high voltage operation. Therefore, in future there might be a need of LDMOS based high voltage generation circuits with smaller areas or RF-MEMS integration to SOI technologies.

- The speed of on-chip charge-pumps does not create a significant limitation. However, the final speed of the system should be optimized taking into account both the electrical and the mechanical domains.

## 8.1.5 Robustness and Reliability

- One of the main reliability concerns for the RF-MEMS switches is the temperature dependency. Since the residual stress in the thin metals can be affected by the temperature, it is well known that the performance of the RF-MEMS switches is strongly depending on the temperature.

- The effect of the temperature in RF-MEMS switches can only be compensated by controlling the stress of the membrane; thus keeping the position of the suspended part as same as at the room temperature. Basically, there are two well-known techniques to do that; namely compensating the stress with different spring combinations or using multi-layer suspended membranes.

- Some of the spring combinations, particularly the ones with lower spring constant, are less influenced by the temperature changes. The RF-MEMS switch developed in this thesis can be an example of them. The contradictory example can be a fixed-fixed beam which is strongly affected by temperature changes.

- The second method to achieve a robust switch against temperature is using multi-layer stacks in which the temperature induced stress can be compensated. The RF-MEMS switch in this thesis can also be an example for this approach since the suspended membrane of the switch is a combination of AlCu sandwiched by TiN/Ti layers.

- Power handling capability of an RF-MEMS switch is another important figure of robustness. As most of the RF-MEMS devices are electrostatically actuated, the

level of RF power or DC biasing can also affect the mechanical domain. Power handling requirements coming from the application have a significant effect on the mechanical design of the RF-MEMS switch.

- In this thesis, the interested frequency bands are at mm-wave frequencies. Therefore, the power handling has not a primary importance. The level of the RF signal that can be generated in SiGe BiCMOS process at mm-wave frequencies cannot easily go beyond 20 - 25 dBm. The only risk with these levels of power is the latching due to the high rms of RF power if a CW type of application is required.

- However, another important concern is the biasing of the RF-MEMS switches. In this thesis, the high voltage for actuation is applied to a separate electrode. Therefore, the DC level of the RF signal line has an importance for both self-actuation and latching cases.

- If a standalone RF-MEMS switch is used in systems, the biasing point of all terminals can be controlled during the systems integration. However, if the switch is used in a BiCMOS circuit, the biasing conditions need to be decided in the design phase. Therefore, DC and RF signal levels causing self-biasing and latching need to be characterized and provided to the circuit/system designers.

- There are many different reasons of non-reliable RF-MEMS devices such as dielectric charging, contact degradation, creep or fatigue in thin layers. Dielectric charging is one of the main bottlenecks of capacitive type RF-MEMS switches. However, separating the high voltage electrode from the signal line can almost solve the problem of dielectric charging by paying the cost of larger device area.

- Reliability tests are done mainly by monitoring the electrical performance of the switch such as up- and down-state capacitance or insertion loss and isolation performance. Indeed, both techniques provide information at steady state positions meaning either at up-state or down-state. However, no dynamic degradation can be observed out of these techniques. Therefore, optical measurement techniques can provide valuable information in order to foresee the potential reliability problems in early stages.

## 8.1.6  Mm-wave Design Examples

- Having the RF-MEMS switches integrated in the BiCMOS process helps significantly to design re-configurable circuits because there is no real alternative to RF-MEMS switch in BiCMOS processes at mm-wave frequencies beyond 60 GHz.

- The VCO example in Chapter 7 shows the importance of accurate models since the provided model for simulations has differed from the fabrication run. Therefore, the simulation results have differed from the measurement results. However, the absorptive switch example shows that if a very accurate model is used, very good agreement can be achieved between the simulation and the measurements.

- During the circuit designs, it is observed that one of the main limitations of using the RF-MEMS switch at mm-wave frequencies is the relatively large size of the device. The advantage of high performance can easily vanish during routing of the large device. Therefore, a careful layout routing is necessary to get full benefit from mm-wave RF-MEMS switches.

- Another important observation is the biasing conditions of the RF-MEMS switch. The RF-MEMS switches are connected to different nodes of the circuit, such as oscillation node in the VCO example. Therefore, the RF signal line can have a DC voltage if it is not blocked by a capacitor. Such DC signal levels can easily cause latching failures, as studied in Chapter 6.

## 8.2  Future Directions

All the achievements and the remarks from the different chapters summarize that the application has the most importance on the development strategy of an RF-MEMS switch. Most of the problems in different domains have been solved, but the requirements need to be well defined in advance. However, the decision on packaging seems to be the most critical factor for both time-to-market and cost aspects. Fast and temporary packaging solutions can help in a short time but they will definitely kill the mass production possibilities. The main reason for that is the necessity of repeating the full process development from the beginning if the package type needs to be changed.

For any kind of integration technique as CMOS+MEMS or heterogeneous integration, one of the most promising techniques is the wafer-level encapsulation which provides the sealing of RF-MEMS devices in a clean-room environment. The potential integration of wafer-level encapsulation technique into CMOS+MEMS platform is given in Figure 8.1 for IHP's high performance 0.13 µm technologies.
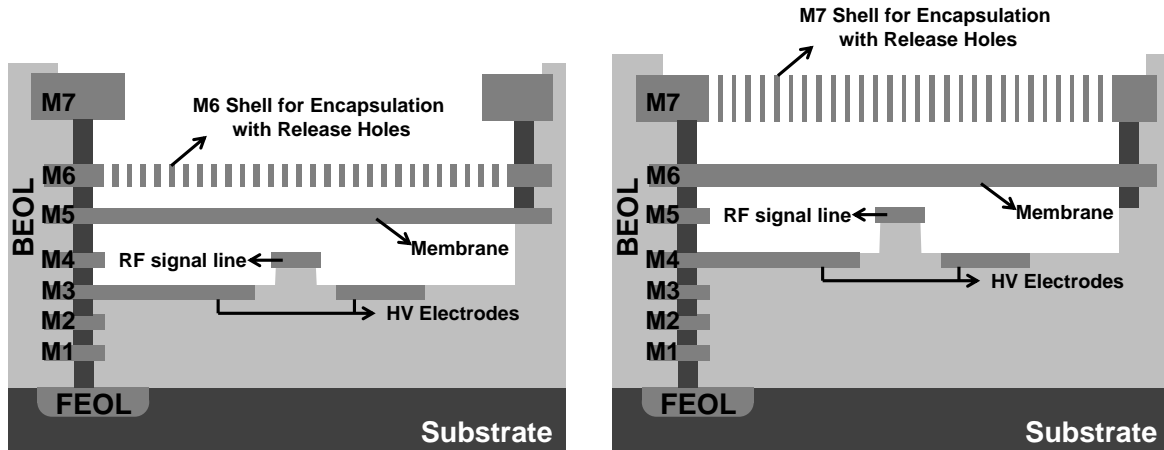


Figure 8.1 The potential integration of wafer-level encapsulation technique into 0.13 µm technology node of IHP.

Depending on the requirements of the application, two different types of wafer-level encapsulation are proposed. The first one seen in Figure 8.1 (left) shows that the shell layer for encapsulation is M6 while the membrane is realized using thin M5 (~500nm) layer. The second solution in Figure 8.1 (right) uses the M7 as shell layer for wafer-level encapsulation and thick M6 (~2 µm) is used as membrane.

Figure 8.2 shows the very initial tests of the proposed techniques. As can be seen in Figure 8.2 (left), the shell layer covers all of the RF-MEMS switch regions and includes small holes for the HF vapor release. The cross-section FIB cut is also given in Figure 8.2 (right).
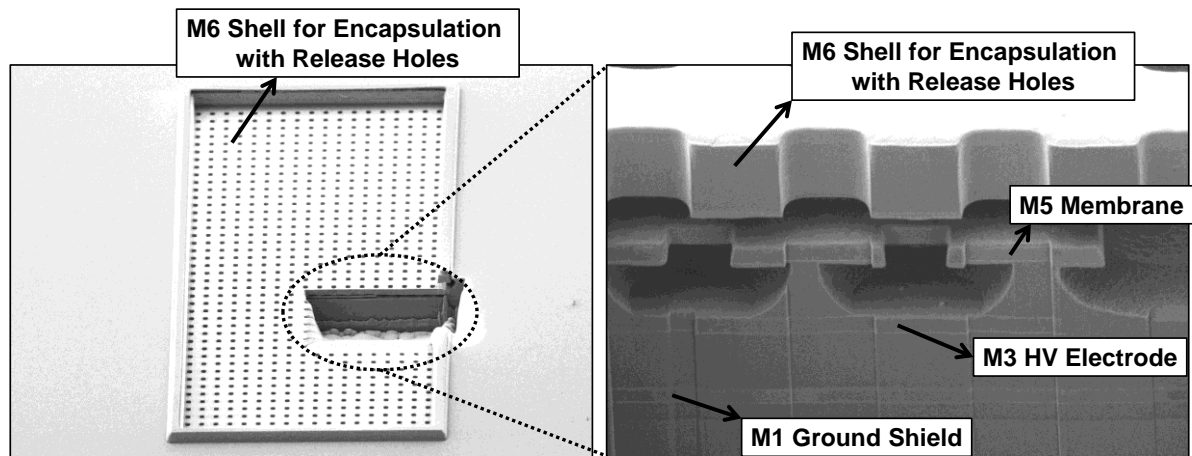
Figure 8.2 FIB images of initial attempts for wafer-level encapsulation technique.

Figure 8.2 (right) shows that there is still oxide between membrane and the high voltage electrode; thus the RF-MEMS switch is not full released. Nevertheless, the initial results are very promising indications that the RF-MEMS switch can be released using the proposed technique and the small holes of shell layer can be filled with a dielectric or metal in the clean-room environment.

In conclusion, the wafer-level encapsulation technique can provide very cost-effective packaging solutions with a very high throughput. It also allows packaging of the sensitive RF-MEMS devices in the same clean-room environment as the fabrication. It is apparently one of the most promising techniques for the applications requiring mass production.

# List of Abbreviations

| | |
|---|---|
| **ADS** | Advanced Design System |
| **BCB** | Benzocyclobutene |
| **BEOL** | Back-End-of-Line |
| **BiCMOS** | Bipolar Complementary Metal-Oxide-Semiconductor |
| **CLK** | Clock |
| **CMOS** | Complementary Metal-Oxide-Semiconductor |
| **COTS** | Commercial off the shelf |
| **CTB** | Charge Transfer Block |
| **CW** | Continues Wave |
| **DC** | Direct Current |
| **EM** | Electromagnetic |
| **ESD** | Electrostatic Discharge |
| **FEM** | Finite Element Method |
| **FEOL** | Front-End-of-Line |
| **FIB** | Focused-Ion-Beam |
| **FRF** | Frequency Response Function |
| **HBT** | Heterojunction Bipolar Transistor |
| **IC** | Integrated Circuits |
| **ISM** | International Scientific Medical Band |
| **ITRS** | International Technology roadmap for Semiconductors |
| **LDMOS** | Laterally Diffused Metal Oxide Semiconductor |
| **LDV** | Laser Doppler Vibrometer |
| **LNA** | Low Noise Amplifier |
| **LTE** | Long-Term Evaluation |
| **MIM** | Metal Insulator Metal |
| **MLR** | Multivariate Linear Regression |
| **MMIC** | Monolithic Microwave Integrated Circuit |
| **MPW** | Multi Project Wafer |
| **M1** | Metal 1 |
| **M2** | Metal 2 |
| **M3** | Metal 3 |

| | |
|---|---|
| **M4** | Metal 4 |
| **M5** | Metal 5 |
| **M6** | Metal 6 |
| **M7** | Metal 7 |
| **NF** | Noise Figure |
| **RF-MEMS** | Radio Frequency Micro-electromechanical Systems |
| **RIE** | Reactive Ion Etching |
| **RLC** | Resistor-Inductor-Capacitor |
| **RMS** | Root Mean Square |
| **SiGe** | Silicon Germanium |
| **SiP** | System in Package |
| **SoC** | System on Chip |
| **SOI** | Silicon on Insulator |
| **SPDT** | Single Pole Double Throw |
| **SPICE** | Simulation Program with Integrated Circuit Emphasis |
| **SPnT** | Single Pole Multiple Throw |
| **SPST** | Single Pole Single Throw |
| **TL** | Transmission Line |
| **TSV** | Through-silicon via |
| **VNA** | Vector Network Analyzer |
| **WLI** | White Light Interferometer |
| **T/R** | Transmit/Receive |

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