Analysis and Design of 40 GHz Frequency Generation Circuits in 90 nm CMOS Technology

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To my parents and my wife

for their love, support and encouragement

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Abstract

Millimeter-wave (mm-wave) CMOS transceivers have attracted increasingly interest in recent years, especially in the 60 GHz band. The 60 GHz band shows the potential to achieve high-data-rate short-range wireless communication up to multi-Gbps. As indispensable building blocks in a wireless transceiver, frequency generation circuits are confronted by many design challenges. At mm-wave frequencies, the voltage controlled oscillator (VCO) suffers from a poor phase noise and a limited tuning range, while the frequency divider is usually accompanied by a small locking range and high power consumption. As for the complete generation of a LO signal, the design of a mm-wave frequency synthesizer encounters greater difficulties. At such a high frequency, achieving the frequency synthesizer with perfect frequency alignment in a closed-loop is much more challenging than connecting individual blocks.

In this dissertation, novel techniques and optimized topologies are proposed to improve the performance of mm-wave frequency generation circuits. Employing a resonated negative-conductance cell, a 40 GHz VCO was designed using 90 nm CMOS technology. It achieves an 8.9 % tuning range and a -96.7 dBc/Hz phase noise at 1 MHz offset, while consuming only 1.65 mW power. Two other designs of the mm-wave frequency divider have also been presented. One design is a Q-band injection locked frequency divider in 90 nm CMOS technology. A 30 % locking range from 36 GHz to 49 GHz has been realized by adopting a transformer-based dual-path injection technique. The other design is an 8:1 static divider with 130 nm CMOS technology. By using a specific design flow, the 8:1 static divider without broadband techniques is capable of operating up to 34 GHz.

Eventually, a complete 40 GHz frequency synthesizer is demonstrated in 90 nm CMOS technology. It is targeted at a 60 GHz super-heterodyne transceiver for high-data-rate communication application. Measurement results show that it achieves a 38.7 – 43.3 GHz LO signal with -89 dBc/Hz phase noise at 1 MHz offset, and reference spurs smaller than -50 dBc. This performance compares favorably with the state-of-the-art developments. This wideband and low-noise LO signal satisfies the 60 GHz high-data-rate communication application of IEEE standard 802.15.3c.

Zusammenfassung

Millimeter-Welle CMOS Transceivers haben in den letzten paar Jahren zunehmend Interesse, besonders im 60 GHz Band, auf sich gezogen. Das 60 GHz Band hat das Potenzial, um hohe Datenraten in der Kurzstreckenkommunikation bis hin zu multi-Gbps zu erreichen. Unentbehrlich bei einer solchen Transceiver-Entwicklung bleibt die LO-Frequenzgeneration, die hohen Anforderungen unterliegt. Im Millimeterwellen-Frequenzbereich leidet der Spannungsgesteuerte Oszillator (VCO) unter einem schlechten Phasenrauschen und einem beschränkten Abstimmbereich, während der Frequenzteiler normalerweise durch eine kleine Locking-Range und hohen Stromverbrauch begrenzt wird. Das Design eines Millimeterwellen-Frequenzsynthesizers für die LO-Signalgeneration ist eine größere Herausforderung. Bei einer so hohen Frequenz ist es erheblich schwieriger einen Frequenzsynthesizer mit perfekter Frequenzausrichtung in einem geschlossenen Regelkreis zu realisieren, als mehreren unabhängigen Blöcken zusammen zuschalten.

In dieser Doktorarbeit werden neuartige Techniken und optimierte Topologie vorgeschlagen, um die Leistung der Frequenzgenerations-Schaltungen zu verbessern. Mit einem mitschwingenden negativen Leitwert wurde ein 40 GHz VCO in 90 nm CMOS Technologie entworfen. Er erreicht einen 8,9 % Abstimmbereich und ein -96,7 dBc/Hz Phasenrauschen (1 MHz Träger Offset), bei einer Leistungsaufnahme von lediglich 1,65 mW. Des Weiteren wurde ein Q-Band Injection-Locked Frequenzteiler ebenfalls in 90 nm CMOS Technologie entwickelt. Eine 30 % Locking-Range von 36 GHz bis 49 GHz ist durch Dual-Injection Technik erreicht worden. Ein weiteres Beispiel ist ein 8:1 statische Frequenzteiler in 130 nm CMOS Technologie. Durch die Verwendung eines spezifischen Entwurfsablaufs funktioniert dieser Teiler ohne Breitbandtechniken bis zu 34 GHz.

Schließlich wird ein kompletter 40 GHz Frequenzsynthesizer in 90 nm CMOS Technologie vorgestellt. Er wird in einem 60 GHz Überlagerungs-Transceiver verwendet. Messergebnisse zeigen, dass der Frequenzsynthesizer ein 38,7 - 43,3 GHz LO-Signal mit -89 dBc/Hz Phasenrauschen (1 MHz Träger Offset) und Referenz Spur kleiner als -50 dBc erreicht. Diese Leistung ist vergleichbar mit den modernsten Entwicklungen. Das breitbandige und rauscharme LO-Signal genügt den Anforderungen des IEEE Standards 802.15.3c für die schnelle 60 GHz Kommunikation.

Contents

List of Tables

List of Figures

List of Symbols

cos	Cosine
C	capacitance
dB	decibel
dBc	decibels referenced to the carrier
dBm	decibels referenced to milliwatt
f	frequency
f_t	cut-off frequency of transistor
f_{max}	maximum oscillation frequency
GHz	gigahertz
Gbps, Gb/s	gigabit per second
g_m	transistor's transconductance
k	Boltzmann's constant
L	Inductance
mA	milliampere
MHz	megahertz
P	power
Q, Q-factor	quality factor
sin	sine
t	time
T	absolute temperature
V	voltage
Y	conductance
Z	impedance

ϕ	phase
λ	wave length
γ	channel thermal noise coefficient of CMOS transistor
ω	angular frequency
Ω	ohm
%	percent

Chapter 1.
Introduction

In the last two decades, mobile communication technology has developed greatly, with the advance of semiconductor industry. People all over the world can now communicate freely in a variety of ways. In addition, more and more customer electronics products have appeared, like laptops, smart phones, music players and video players. Finding way for these products to communicate with each other has also attracted heightened interest. Wireless personal area networks (WPAN) are built up by targeting such radio links operating over short ranges. A number of communication standards have been announced for the WPAN application, such as Bluetooth, WiFi, Zigbee, and Ultra-wideband (UWB). The Bluetooth (IEEE 802.15) made its first appearance at only 1 - 2 Mb/s data-rate. The WiFi is designed and optimized for long ranges, while the Zigbee is known as the so-called low rate WPAN. It is designed for low-rate, low-power application with a very long battery life. The standard IEEE 802.15.3, known as UWB, employing 7 GHz bandwidth is utilized for WPAN application. However, with a low transmit power, it is difficult to achieve a high signal-to-noise ratio (SNR) at the receiver for UWB communications. Therefore, high data-rate communication up to multi-Gb/s is a target which has not yet been achieved.

Recently, the standard IEEE 802.15.3c provides an unlicensed spectrum at around 60 GHz. It is quite suitable for high data-rate WPAN applications. Firstly, it has an ultra-wide 7 GHz bandwidth with a maximum channel bandwidth of 2.16 GHz. Additionally, unlike UWB, the transmitted power level could be as high as 40 dBm. Besides, there has been almost no interference around 60 GHz so far. It seems fairly promising to achieve multi-Gb/s data-rate communication through the 60 GHz frequency band. Since 2003, the IEEE 802.15.3 task group has investigated the use of the 60 GHz spectrum as the physical layer (PHY) for the high data-rate WPAN [1]. Up to now, the standard IEEE 802.15.3c has been granted about the millimeter-wave (mm-wave) WPAN PHY at 60 GHz. In Europe, the mm-wave PHY at 60 GHz

employs 9 GHz bandwidth from 57 GHz to 66 GHz. It has three different PHY modes, single carrier (SC) PHY, high speed interfere (HSI) PHY and audio/visual (AV) PHY. For high rate applications, the whole spectrum could be divided into 4 channels, each one with 2.16 GHz bandwidth. It is targeted for high data-rate communication up to 2 - 4 Gb/s.

The benefits of mm-wave application come at a cost. The realization of mm-wave PHY encounters several difficulties, such as device modeling, circuit design, antenna integration and so on. Up to now, most of the commercial mm-wave products are realized with non-silicon technology, such as GaAs MHEMT, PHEMT, InP HBT. Clearly, these technologies offer a better ability for high frequency and high power operation. So they are naturally better options for the mm-wave design. However, some of these basic disadvantages prevent them being widely used in the costumer market. Firstly, they could not achieve a high volume due to their low manufacturing yields. Secondly, there is no possibility to integrate these technologies with CMOS technology, which is widely used in costumer products for the baseband circuits. Moreover, silicon technology enjoys significant benefits from continuing scaling down. The cut-off frequency f_t and maximum oscillation frequency f_{max} experience a considerable improvement following the technology scales down. Silicon technology has already shown a promising capability for the mm-wave design. Compared with CMOS, Bipolar technology offers superior performances at high speed, low noise and high power operation, which make itself go ahead in mm-wave design. Besides, the silicon-germanium (SiGe) technology gives Bipolar a second life. In 2006, the world's first 60 GHz transceiver chipset was reported by IBM, using 0.13 μm SiGe BiCMOS technology [2]. Following that, integrated phase array transmitters at 77 GHz [3] and beyond 100 GHz [4] have been realized.

Compared with Bipolar technology, CMOS suffers from more difficulties. Firstly, the model of CMOS transistor is always a problem because it is basically developed for the digital design. The model is supposed to be optimized for high frequency design. Besides, the resistivity of CMOS substrate is pretty low, normally $< 10\ \Omega$-cm. This would induce great coupling between circuits as well as losses in passive devices. So it is hard to achieve passive devices with a high Q-factor in CMOS technology. In addition, the natural drawbacks of CMOS technology still exist,

such as low break-down voltage and high noise. Theoretically, the CMOS transistor is unable to produce high power because of its low break-down voltage. The poor noise performance makes the design of low-noise circuits pretty difficult. Two examples of these circuits are the low-noise amplifier (LNA) and the voltage controlled oscillator (VCO).

Currently, the performance of 65 nm CMOS technology is comparable with 130 nm BiCMOS. At the same time, the mask price of 65 nm CMOS is a little higher. However, after the chip manufacture volume is increased significantly, the cost per chip will decrease. When considering a complete integration solution, CMOS technology is the only choice. If a BiCMOS transceiver is integrated with a CMOS baseband circuit, the cost will rise. Thus, the CMOS technology is quite suitable for customer electronic applications, like the 60 GHz band communication. The history of the semiconductor industry has shown that, any wireless application for customer electronics always begins with Bipolor or BiCMOS technology, but it will be finally replaced by CMOS technology. It is believed that the drawbacks of CMOS technology will be overcome in near future. It has been proven that the 130 nm CMOS process has the ability to create some building blocks even a receiver front-end [5] operating at 60 GHz . Many 60 GHz frond-end have also been reported using 90 nm CMOS technology [6][7][8]. But 65 nm CMOS is considered a better choice for completely integrated 60 GHz transceiver design [9][10][11][12]. It offers a higher gain at 60 GHz. Also, it facilitates the design of the power amplifier (PA) for high power and high efficiency [13][14].

The radio system enables information transmission from one place to another through air or cables. In the modern wireless communication system, the original information must firstly be modulated and then transmitted by a high frequency carrier signal to combat noises and attenuations through the transmission. This high frequency carrier is usually called the local oscillator (LO) signal. The frequency synthesizer is designed to generate this LO signal, and at the same time select the communication channel. Examples of this application include cellular phones, wireless local area network (WLAN) and the recently announced 60 GHz WPAN application.

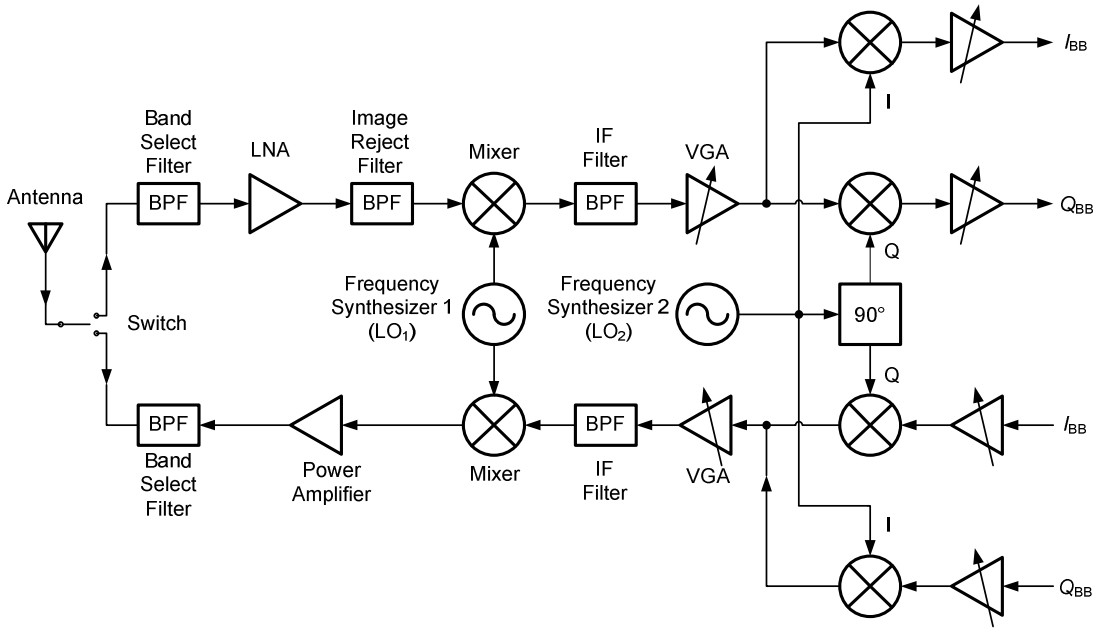


Figure 1.1 Typical architecture of a super-heterodyne transceiver

Figure 1.1 shows a typical architecture of a super-heterodyne transceiver [15]. The modulated signal is transmitted and received at the same frequency. The radio frequency (RF) signal is transmitted through the atmosphere and received by the antenna. Then it will pass through a band pass filter (BPF) to remove interference. At the same time the desired RF band will be selected. Then it will be amplified to an acceptable power level by a LNA and filtered by an image reject filter to remove the image signal. The signal will then be down-converted in the Mixer to the intermediate frequency (IF). In the Mixer, the received RF signal is mixed with the LO signal generated by the frequency synthesizer, generating IF signal. The frequency relation between them is given by

$$f_{IF} = \left| f_{RF} - f_{LO} \right| \tag{1.1}$$

The frequency of the LO signal can be higher or lower than that of the RF signal, corresponding to high side or low side conversion. After down-conversion to the IF, an IF filter is usually used to remove the unwanted signal. The signal could be further amplified by a variable gain amplifier (VGA) to keep a constant signal level for the

second conversion. A second synthesizer is needed to generate a second LO signal, which will mix with the IF signal and generate the baseband signal. An I/Q down-conversion architecture may be required to build the phase information of the received signal, if a complex baseband demodulation scheme is adopted.

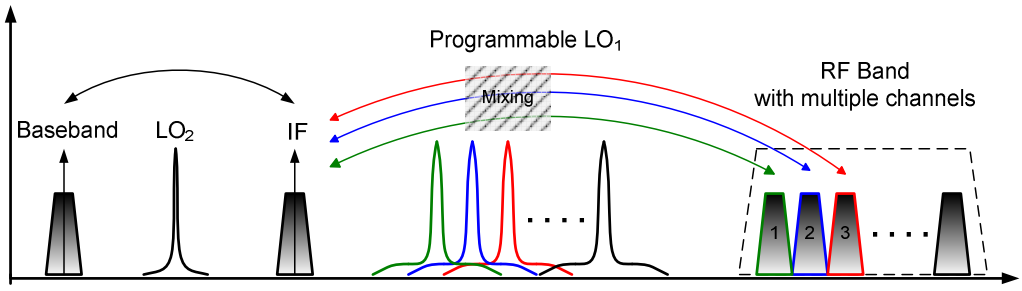


Figure 1.2 Frequency synthesizer in FDMA radio systems

Let's investigate the function of a frequency synthesizer in the frequency domain with Figure 1.2. For most modern radio systems, frequency division multiple access (FDMA) is employed. It means the whole communication band is divided into multiple channels, and each channel is allocated to only one user at one time. Therefore, when RF signal is received, the receiver selects the targeted channel and down-converts it to the baseband for demodulation. Channel selection is accomplished by the frequency synthesizer. The frequency synthesizer adjusts the LO frequency corresponding to the desired RF channel. Then all RF channels are down-converted to the constant IF frequency. This process is illustrated in Figure 1.2. The IF signal will further mix with a second LO signal, which has a fixed frequency, eventually generating the baseband signal.

The transmitter operates in almost the same way, but in the reverse direction. The difference is that after up-conversion to the RF, a PA is designed to boost the power level of the RF signal for the transmission through the antenna. The important performance specifications of the frequency synthesizer are listed below.

Acquisition range: Acquisition means the frequency synthesizer switches on from a random frequency and finally locks to the desired frequency. The acquisition range refers to the frequency range where the frequency synthesizer could achieve phase

locking. In theory, the PLL-based frequency synthesizer employing a phase frequency detector (PFD) has an infinite acquisition range. When the PLL is unlocked, the frequency detector will first push the VCO frequency closer to the targeted frequency. After the frequency difference is reduced to a sufficiently low value, the phase detector would take over and finally drive the VCO's frequency exactly the same as the wanted frequency. Practically, the acquisition range depends upon the tuning range of VCO and the locking range of the frequency divider chain. This issue will be discussed in detail in chapter 2.

Settling time: When the modulus of the programmable divider in a frequency synthesizer is reprogrammed, the output frequency of this synthesizer will experience a dynamic process and eventually stabilize to the desired frequency. The duration of this dynamic process is called the settling time. In some applications such as the frequency hopping system, the settling time of the synthesizer is limited significantly [15].

Spectrum purity: In the frequency domain, there are many unwanted frequency components around the desired carrier tone. These unwanted frequency components should be suppressed in the design. The spectrum skirt of unwanted frequency components around the carrier is called 'phase noise'. In the time domain, it can be considered as the jitter at the zero crossing of the waveform.

Spurious frequency components: In the integer-N frequency synthesizer, when the loop is locked, there is a periodic cripple on the control line of the VCO. This cripple has the same frequency as the reference frequency f_{ref}. Then spurious frequency components are created in the frequency domain. They are located at $\pm f_{ref}$ with respect to the LO carrier, and are called the 'reference spur'. In the fractional-N frequency synthesizer, the fractional spur replaces the reference spur. The amplitude of this spur should be several decibels lower than the desired carrier, depending on different applications.

Output power: The frequency synthesizer should provide sufficient power to allow the switching operation of the transistors in the Mixer.

Power consumption: The total power consumption of the frequency synthesizer should be kept low. It is critical in modern communication systems which are designed for a long battery life.

Since the LO generation plays a critical role in a wireless transceiver, the performance of the frequency synthesizer has a great influence on the performance of the whole system. Here we focus on the two factors (phase noise and reference spur) in order to investigate how they affect the performance of the system.

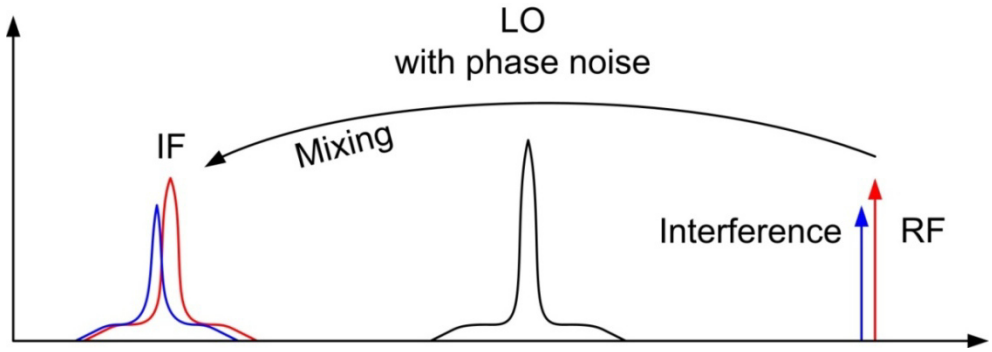


Figure 1.3 Influences from LO phase noise

Receiver sensitivity is defined as the minimum signal level that the receiver can detect with the accepted SNR [15]. In the receiver system, the phase noise of the LO signal will cause the degradation of the SNR. This phenomenon is same in both the single-carrier and multicarrier systems. However, phase noise would also lead to inter-carrier interferences in a multicarrier system, like Orthogonal Frequency Division Multiplexing (OFDM) system. OFDM is a multicarrier modulation which has been implemented for many high data-rate wireless communications due to its great ability to alleviate the multipath effects. In an OFDM system the spectrum associated to each elemental data is a small portion of the total bandwidth, which is divided in many sub-channels. Each of them is modulated with one information symbol and they are all multiplexed in frequency [16]. To increase the bandwidth efficiency, the number of the sub-channels could be as much as thousand. As a result, the channel spacing could be quite small, even several MHz. As described in Figure 1.3, the real LO carrier with the phase noise down-converts both the desired

RF channel and the adjacent channel interference to the IF. Consequently, the SNR of the IF signal is increased. In a digital demodulator, it is judged by the bit error rate (BER). The effect of phase noise on the BER in a OFDM system is given in [17]. It is observed that the system performance is very sensitive to the phase noise. System's BER increases greatly as the degradation of the phase noise. In brief, the phase noise of the frequency synthesizer's output degrades the receiver sensitivity.

Receiver selectivity specifies the ability of the receiver to select the targeted communication channel against the adjacent channel [15]. As to an integer-N frequency synthesizer, the reference frequency f_{ref} equals the channel spacing, while the reference spur is located at the f_{ref} offset with respect to the carrier. Therefore, when the LO signal is mixed with the RF signal, the reference spur will translate some energy in the adjacent channel to the IF signal, as shown in Figure 1.4. Thus, the existence of a reference spur reduces the receiver selectivity.

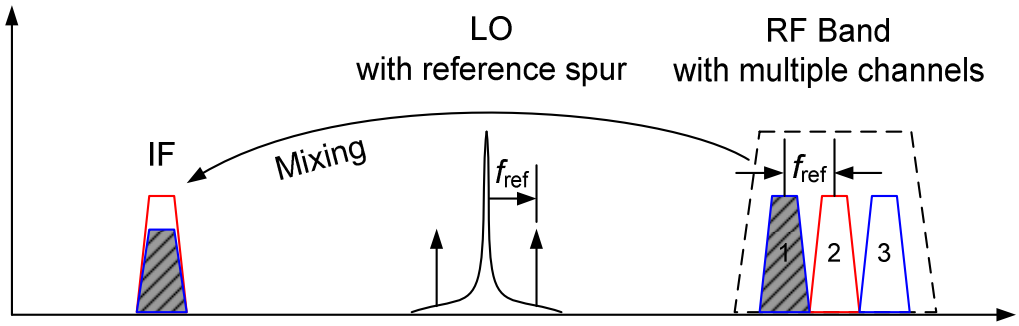


Figure 1.4 Influences from LO reference spur

This dissertation will focus on analysis, design and implementation of mm-wave frequency generation circuits in CMOS technology. It will be organized as follows. Since the frequency synthesizer is widely used for the LO frequency generation in the wireless transceiver, its fundamentals will be presented first in chapter 2. Its theory of operation, basic architectures, each building block and the whole loop performance will be analyzed. Chapter 3 discusses design issues of the mm-wave frequency generation circuits, especially focusing on the mm-wave VCO and the 2:1 frequency divider. In chapter 4, the design of a 40 GHz VCO is presented

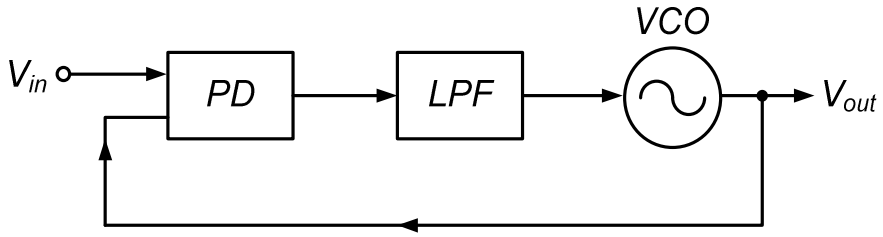
in 90 nm CMOS technology. Two design examples of mm-wave frequency dividers will then be demonstrated in chapter 5. One is a 40 GHz injection locked frequency divider with a locking range improvement. The other is an 8:1 static frequency divider operating up to 32 GHz. Chapter 6 will present the complete design of a 40 GHz frequency synthesizer for 60 GHz WPAN applications. It includes the completed design flow and detailed measurement results. A short conclusion will be made in chapter 7.

Chapter 2.

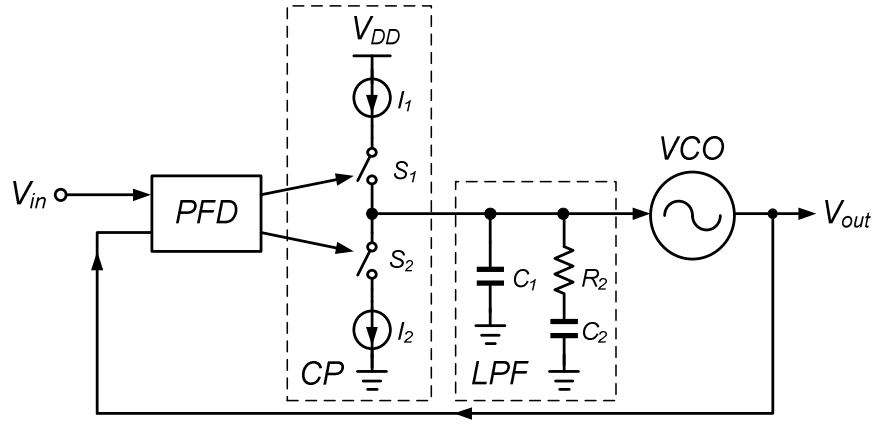
Frequency Synthesizer Fundamentals

The fundamentals of the frequency synthesizer will be introduced in this chapter. Since the PLL-based synthesizer has become the most practical and widely used solution for high frequency LO generation in communication systems, the discussion begins with a brief review of the phase locked loop (PLL). The introduction of each building block in a PLL-based synthesizer will then be presented. Distinct architectures of the frequency synthesizer and the design of the loop performance are further analyzed.

2.1. Phase Locked Loop Basics



(a)



(b)

Figure 2.1 Simplified block diagram of (a) basic PLL and (b) CP-PLL

The concept of phase locking was developed in the 1930s. After that, it was widely used in fields such as electronics, electrical engineering and communication systems [18]. The block diagram of a basic PLL is shown in Figure 2.1 (a). The PLL operates as a closed-loop feedback system.

The phase detector (PD) compares the phase difference between V_{in} and V_{out}, further generating a dc voltage to adjust the frequency of the oscillator. Finally, when the PLL gets locked, the phase of the VCO's output V_{out} will be identical to the input V_{in} if the loop gain is infinite. Consequently, the frequencies of the input and output will be exactly the same. However, since the loop gain is finite, the phase difference between the input and output is actually not zero, but keeps constant when the loop becomes stable. The low pass filter (LPF) is used to remove unwanted high frequency noise from the PFD output, which is critical for VCO's noise performance.

The basic PLL architecture has obvious drawbacks. Firstly, the 'acquisition' is a problem for the basic PLL without a frequency detector (FD). Since the basic PLL only employs the PD, the PLL would fail to stabilize the loop if the frequency difference between the V_{in} and V_{out} is too large when the PLL turns on. In theory, its acquisition range is proportional to the bandwidth of the LPF [15]. To achieve a large acquisition range, a large LPF bandwidth is required, which is unfavorable to noise performance. Furthermore, the basic PLL cannot achieve an absolutely synchronized phase between V_{in} and V_{out}. That is to say, the phase error at the PD input could not become zero when the PLL becomes locked. It gives a poor performance for phase tracking [19].

To overcome the shortcomings of the basic architecture, the architecture of the charge pump (CP) PLL was developed, as shown in Figure 2.1 (b). In a standard topology, the CP-PLL employs a phase frequency detector (PFD) instead of a PD. When the frequency difference is larger, the frequency detector will first push the f_{out} closer to f_{in}. The phase detector then operates to achieve the loop locking. Thus, the acquisition ability of the PLL is improved considerably. In practice, the acquisition range of the CP-PLL is basically limited to the tuning range of the VCO and the locking range of the frequency divider. In addition, employing the circuit combination of the charge pump, PFD and LPF, the loop offers an infinite gain. The charge pump

circuit operates like a voltage-to-current convertor. It pumps the current into or out of the LPF according to the phase error at the input of the PFD. This infinite gain of the loop makes the phase error at PFD input tend to zero when the loop gets locked, assuming that all the circuits operate ideally [19].

In a classic design, the LPF employs a 2nd order filter, which has a shunt capacitor connected to the ground. This capacitor will induce a pole at the origin. Together with the one pole generated by the VCO, the whole loop would have two poles at the origin. This type of the PLL is usually called type-II PLL [15]. The basic PLL belongs to the type-I PLL, which possesses only one pole at the origin. For the type-II PLL, a zero should be added to ensure the stability of the loop. The high-order LPF (order ≥ 3) is highly recommended when the suppression to spurious frequency components is required. The LPF design and PLL stability will be discussed in detail in the following chapter 2.3.

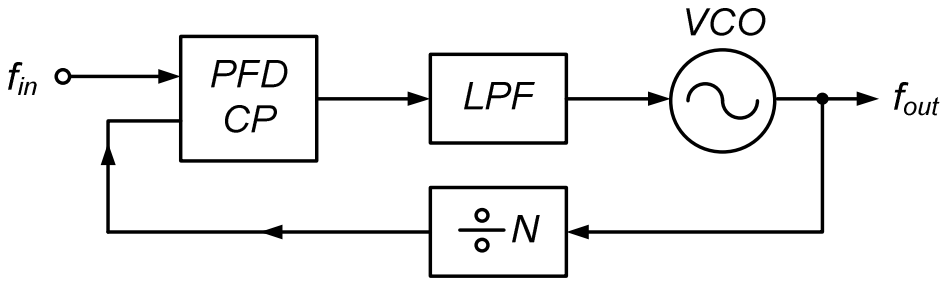


Figure 2.2 Simplified block diagram of PLL-based frequency synthesizer

To realize a frequency synthesizer, a frequency divider is usually designed in the feedback path of the PLL, as shown in Figure 2.2. Then the output frequency f_{out} is equal to the multiplication of the input frequency f_{in}, which is

$$f_{out} = f_{in} \cdot N \tag{2.1}$$

In this way, a high frequency output is available from a low frequency reference. If the divider ratio N of the frequency divider is adjustable, then a frequency-programmable LO could be generated. This PLL-based frequency synthesizer is a critical building block in the FDMA wireless system for the channel selection. Basically, Figure 2.2 shows the basic architecture of the frequency synthesizer for LO frequency generation in the wireless transceiver.

2.2. Building Blocks

2.2.1. Voltage Controlled Oscillator

Principle model

The oscillator is one of the most important building blocks in the frequency synthesizer. It generates a periodic signal as the LO signal for the transceiver. In theory, the RF oscillator could be analyzed by two types of models: feedback system and one-port network.

Feedback system

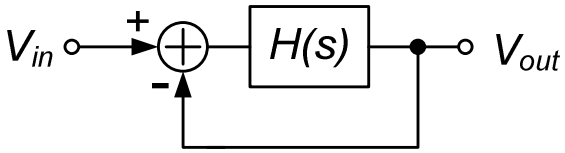


Figure 2.3 Linear feedback system

The oscillator could be viewed as a simple linear feedback system depicted in Figure 2.3. Its transfer function is expressed by

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 + H(s)} \tag{2.1}$$

To start a self-oscillation without the input, the loop gain $H(s)$ of the system might be -1 at the oscillation frequency ω_{osc}. It implies that the loop is supposed to include a frequency selective network, resulting in the following two conditions at ω_{osc}.

Loop gain at ω_{osc}: $|H(j\omega_{osc})| = 1$

Loop phase shift at ω_{osc}: $\angle H(j\omega_{osc}) = 180^\circ$

Any feedback system could oscillate if its loop gain and loop phase shift are designed for this purpose. In most of RF oscillators, a LC tank is usually employed as the frequency selective network.

One-port oscillator

The feedback model discussed above is actually a two-port model, since the $H(s)$ is a two-port block in a closed-loop. Figure 2.4 describes the one-port model of an oscillator. From the LC resonator side, the equivalent resistor R will prevent the resonator from oscillating since the energy is dissipated in the resistor R. To compensate for energy loss, a negative resistor equal to $-R$ could be connected in parallel to the R. From the perspective of energy conservation, the energy lost in the LC resonator is replenished by the negative resistor. The negative resistor is implemented typically by an active circuit network. The oscillator which could be analyzed as a one-port network is called the one-port oscillator.

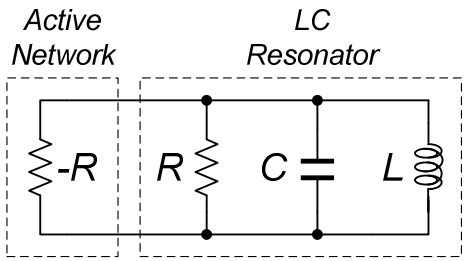


Figure 2.4 One-port model of an oscillator

The category of oscillators

Typically, there are three categories of oscillators: RC oscillator, ring oscillator, and LC oscillator. The RC oscillator is implemented practically using the discrete devices. With today's Silicon technology, the integrated oscillators are mainly implemented as the ring oscillator or the LC oscillator. These two types of oscillators are concerned in the following introduction.

Ring oscillator

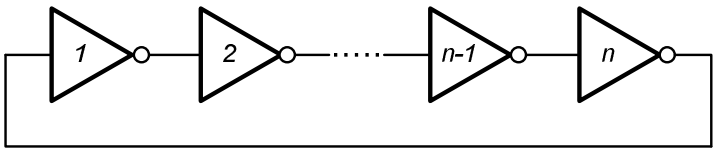
Basically, the concept of the ring oscillator is to build a feedback system through several gain stages in the loop, as shown in Figure 2.5 (a). For the single-ended gain stage, there must be an odd number of gain stages. As a result, when the

total phase shift along the loop reaches 180º at a desired frequency, and loop gain is more than unity, the circuit starts to oscillate.

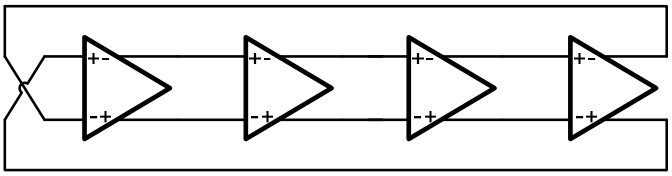
If a ring oscillator employs n stages while the delay of the each stage is τ_d, the oscillation frequency is calculated as

$$f_{osc} = \frac{1}{2n\tau_d} \tag{2.2}$$

The number of the gain stages depends on the specified oscillation frequency, power consumption and jitter performance. Normally, n is between 3 and 5. The ring oscillator could also be achieved with the differential topology. This is preferable because of its better common-mode rejection and noise performance. With the differential gain stage, there could be an even number of gain stages. The circuit is able to oscillate provided the input and output of one gain stage are not inverted. Figure 2.5 (b) shows a ring oscillator with 4 differential gain stages.



(a)



(b)

Figure 2.5 Ring oscillators with (a) single-ended stages and (b) differential stages

The design of a ring oscillator does not normally need large passive devices e.g. monolithic inductor. So it is easy to design a compact layout. Furthermore, the ring oscillator is able to achieve a large tuning range. However, poor phase noise

performance has become the most crucial drawback of the ring oscillator, because of the large number of active devices.

LC oscillator

With the continuing progress of semiconductor technology, today's CMOS technology is capable of implementing monolithic inductors with a high *Q*-factor. It makes the design of a high quality LC oscillator possible. Figure 2.6 shows two widely used topologies of the LC oscillator: cross-coupled oscillator and Colpitts oscillator. They can both be analyzed as the one-port oscillator. Detailed analysis is given in chapter 3.

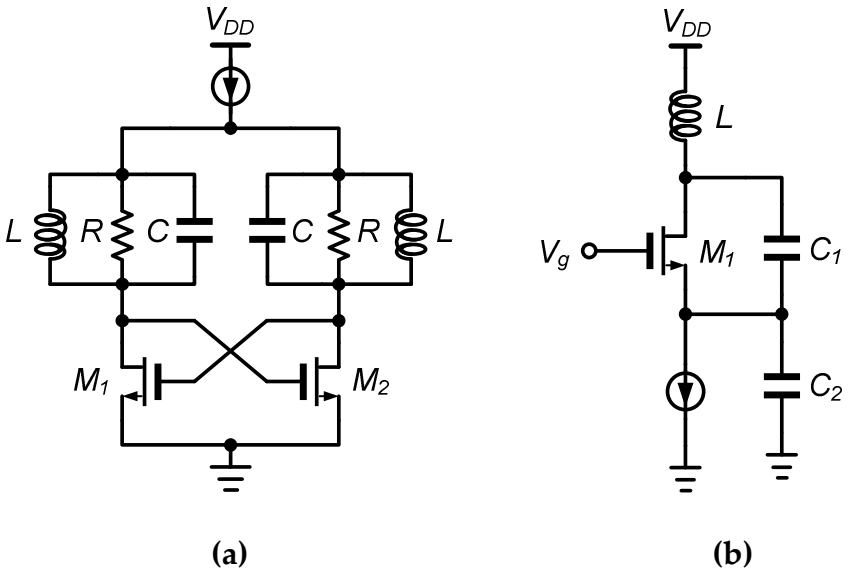


Figure 2.6 (a) Cross-coupled oscillator and (b) Colpitts oscillator

Compared with the ring oscillator, the LC oscillator has a simpler topology and uses much less active devices. Theoretically, the LC oscillator offers better phase noise performance. Additionally, since the parasitic capacitance in the LC oscillator is much less than in the ring oscillator, the former is easier to operate at high frequencies. Therefore, the LC oscillator is the most popular choice for the LO signal generation in wireless communication systems.

Performance Specification

Here the important performance specifications of the VCO are summarized.

Tuning range: It is defined by the difference between the maximum and the minimum oscillation frequencies. To overcome the process-voltage-temperature (PVT) variations, the tuning range of the VCO should be wide enough to cover the targeted LO frequency range.

Tuning Sensitivity: The tuning sensitivity is specified as the variation of the oscillation frequency induced by per unit voltage. If the control voltage varies from V_1 to V_2, and at the same time the oscillation frequency is tuned from f_1 to f_2, then the tuning sensitivity is derived as

$$K_{VCO} = \frac{f_2 - f_1}{V_2 - V_1} \tag{2.3}$$

K_{VCO} is also called the gain of the VCO. It has a unit of Hz/Volt. For a large tuning range, a large K_{VCO} will be required. However, a large *Kvco* would make the VCO more sensitive to the amplitude modulation (AM) noise. As a result, AM noise from the supply voltage or control line could significantly degrade the phase noise performance [20].

Phase noise:

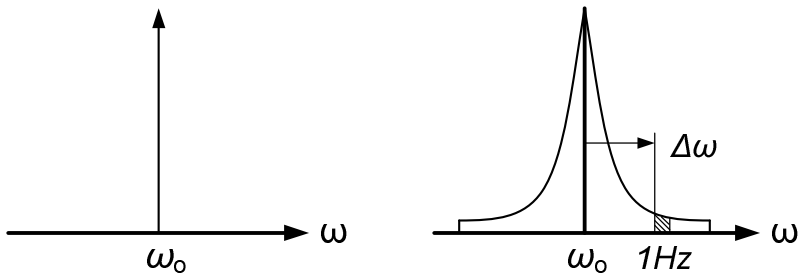


Figure 2.7 Output spectrum of (a) ideal oscillator and (b) real oscillator

The spectrum purity of the oscillator's output signal is specified by the phase noise. An ideal oscillator would generate a pure sine wave, whose spectrum assumes

the shape of an impulse. However, real oscillators have phase noise components, which spread a noise skirt around the carrier frequency, as shown in Figure 2.7. The phase noise of a unit bandwidth at an offset $\Delta\omega$ with respect to the carrier frequency ω_o is calculated by the ratio of the noise power in this unit bandwidth to the power of the carrier signal, which is

$$L\{\Delta\omega\} \approx 10 \log_{10}\left[\frac{P_{sideband}\ (\omega_o + \Delta\omega, 1Hz)}{P_{carrier}}\right] \tag{2.4}$$

The phase noise is expressed in units of dBc/Hz.

Jitter: The Jitter is the manifestation of the phase noise in the time domain. The jitter at the zero crossing of the waveform could be characterized as an indicator of the VCO's noise performance. But it is usually used in the evaluation of clock and data recovery circuits. In principle, the phase noise and the jitter are equivalent.

Power consumption: The VCO design is challenged by serious trade-offs between the tuning range, noise property and power consumption, which makes the low-power VCO design difficult.

2.2.2. Phase Frequency Detector and Charge Pump

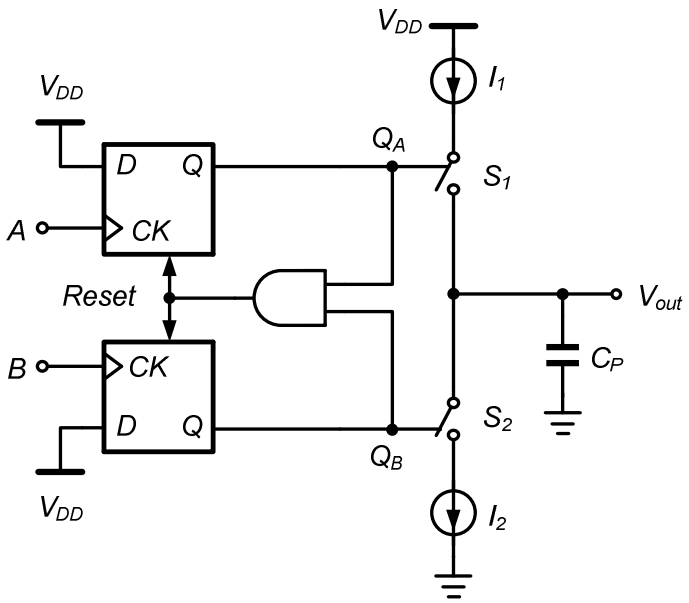
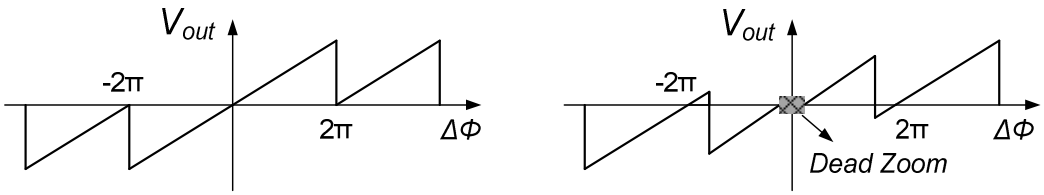


Figure 2.8 Basic architecture of PFD and charge pump

Figure 2.8 shows the basic realization of the PFD and charge pump circuit in the PLL. The PFD is composed of two edge-triggered D-type flipflops and a AND gate. The outputs of the PFD control the operation of two switches in the charge pump. The charge pump has two current sources, which pump the current into or out of the loop filter, according to the logic input from the PFD. Normally, a small capacitor C_p is added at the output terminal to remove the voltage jump generated when the current is periodically pumped into the LPF.

The charge pump circuit responds to the rising edge of two inputs and creates a three-state output. When Q_A=1, Q_B=0, the switch S_1 is turned on and S_2 is turned off. The current is pumped into the filter, increasing the output voltage. When Q_A=0, Q_B=1, S_1 switches off and S_2 switches on. The current is pumped out of the filter. When Q_A=Q_B=0 which is called the 'ground' state, both S_1 and S_2 switch off. The output presents a high-impedance state. When the Q_A and Q_B are simultaneously high, the AND gate in the reset path forces the PFD to change to 'ground' state. Normally, the size of switch S_1 and S_2 are the same.

Dead zoom of PFD



(a) **(b)**

Figure 2.9 Input-output characteristics of (a) ideal PFD and (b) real PFD

Figure 2.9 (a) shows the input-output characteristic of an ideal PFD. The output is defined as the difference between the average values of Q_A and Q_B. The output varies symmetrically with the phase difference $|\Delta\phi|$. The PFD has an ideal

phase detect range from -2π to 2π, where the output and input have a linear relationship. However, in reality this is not the case.

When the phase difference between A and B is very small, the pulse width of Q_A and Q_B would be extremely short. Because of the parasitic capacitance at the gate of the switches in the charge pump, these short pulses could not turn on or off the switches completely. As a result, the circuit in Figure 2.8 cannot detect small phase differences and give the correct voltage output. This small phase range which the PFD could not detect is called 'dead zoom'. The dead zoom should be minimized in the design. A simple approach is to increase the delay of the reset path. Apart from the AND gate, a number stages of invertors could be added after the AND gate to increase the delay. Consequently, the pulse width of Q_A and Q_B are increased. However, the existence of the delay in the reset path would decrease the phase detect range of the PFD. As illustrated in Figure 2.9 (b), the phase detect range of a real PFD would be much less than 4π.

Design issues of charge pump

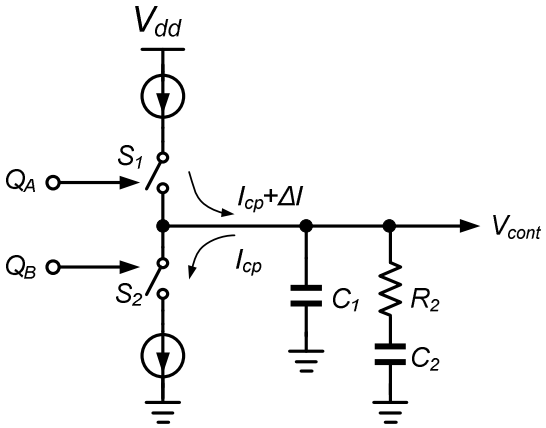


Figure 2.10 Current mismatch of charge pump

As discussed above, the delay in the reset path of the PFD is supposed to be long enough to remove the dead zoom. Consequently, two pulses at Q_A and Q_B overlap. Even so, the two current sources in the charge pump cannot provide two identical currents, because of the process variation. Typically there would be a small

current difference ΔI between the two current sources, as shown in Figure 2.10. This effect is called 'current mismatch'. Even if the pulses at Q_A and Q_B are overlapped perfectly, the net current into or out of the LPF is not zero. As a result, the VCO's control voltage V_{cont} is changed by a constant value in every period. In order to remove this effect caused by the current mismatch, the loop would enforce a phase difference between the input and output, after the PLL becomes stable. Finally, the net current generated by the charge pump becomes zero. Because of the current mismatch in the charge pump circuit, the stable phase error when PLL gets locked is no longer zero in the CP-PLL. The amount of mismatched currents depends on the device parameters and process variations [21]. Design of symmetric schematic and layout could diminish the current mismatch to some extent.

In addition to the current mismatch, the clock feed through and charge injection will cause more ripples and disturbances on the V_{cont} [21], further degrading the noise performance.

Topology of charge pump

Three typical topologies of the charge pump circuit are depicted in Figure 2.11, developed from its function as a voltage-to-current convertor displayed in Figure 2.8.

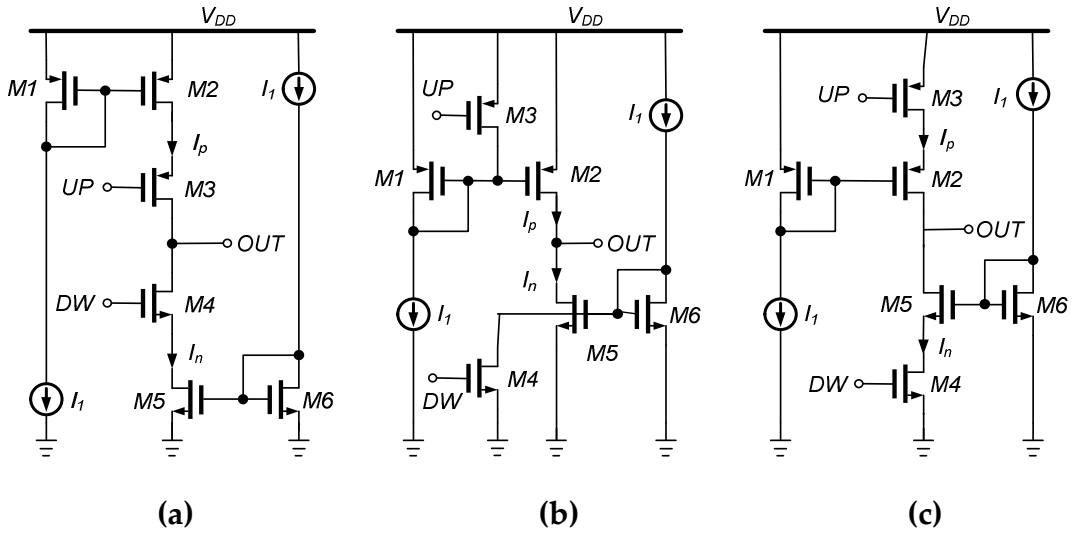


Figure 2.11 Topologies of charge pump with (a) switches at drain, (b) switches at gate, and (c) switches at source of current mirrors

The first one displayed in (a) is the most conventional charge pump with the switches at the drain of the current mirror. This topology is created directly from the function of a voltage-to-current converter, as described in Figure 2.8. Its drawbacks are obvious. When switch M_4 is switched on and off, the voltage at the drain of M_5 would vary between zero and the loop filter voltage held by the PLL. Therefore, M_5 does not operate in the saturation region until the voltage at the drain rises higher than the threshold voltage. The same situation occurs at the PMOS current mirror for the transistor M_2. Meanwhile, since the operation of switches M_3 and M_4 are influenced significantly by the loop filter voltage, which is fixed by the loop, these two switches definitely cannot operate synchronously even when controlled by the same pulses. These factors in this topology would make the current mismatch considerable and uncontrollable. Additionally, this topology is clearly difficult to achieve with a low supply voltage.

As shown in Figure 2.11 (b), moving the switches to the gate of the current mirror [22], M_2 and M_5 would operate mostly in the saturation region if the filter voltage is not close to V_{DD} or ground. In the meantime, the switching of M_3 and M_4 would not be affected by the loop filter voltage. Thus, basically the topology (b) is superior to topology (a) in terms of the current mismatch. However, substantial parasitic capacitance at the gate of the current mirror restricts the switching speed of switches M_3 and M_4. This problem is crucial, especially when long channel devices are employed for better current match. This restriction could be overcome simply by designing switches at the source of the current mirror [23], as shown in Figure 2.6 (c). Unlike topology (b), topology (c) requires large voltage headroom, which makes it difficult to design with a low supply voltage.

There is a shortcoming common to the above three topologies. The current mismatch between I_p and I_n is affected significantly by the voltage of the output terminal fixed by the loop. When the current mirror is forced to operate in a nonlinear region by the voltage at the output terminal, the current mismatch would increase significantly. This effect could be suppressed by introducing the feedback to the current mirror through an operational amplifier (op-amp) [24][25], as shown in Figure 2.12 (a). The op-amp compares the voltage at the output, and at the drain of the

current mirror. The gate voltage of M_1 and M_2 may increase or decrease according to the voltage difference at the op-amp input. Consequently, the currents through M_2 and M_7 are almost the same, regardless of the voltage at the output terminal. Figure 2.12 (b) shows a similar realization of the charge pump with switches at the gate of the current mirror.

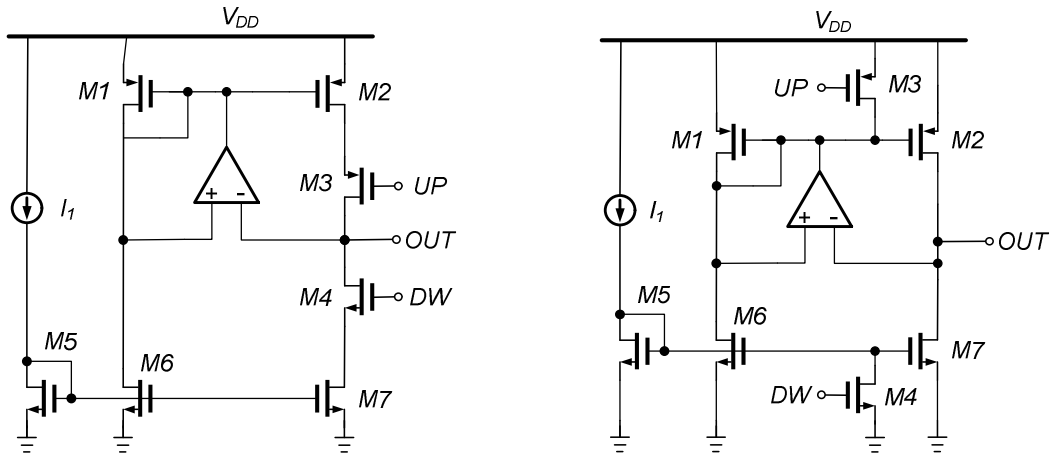


Figure 2.12 Charge pump with a feedback employing switches at (a) the drain of current mirror and (b) the gate of current mirror

A recently proposed topology is presented in Figure 2.13. It is based on the differential source coupled logic (SCL) gate as the input stage [26][27].

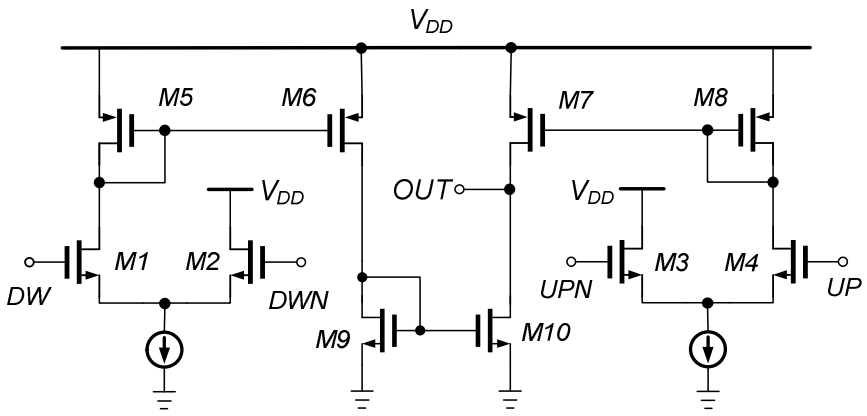


Figure 2.13 Charge pump based on SCL topology

When the input becomes high, the SCL input pairs (M_1 and M_2, M_3 and M_4) steer the current to the current mirrors (M_5 and M_6, M_7 and M_8). The up and down currents will be compared though the current mirror M_9 and M_{10}. Finally, the net current is pumped into or out of the loop filter. Because of the differential input pairs, this topology experiences a faster switching speed. Meanwhile, it is fully symmetric. Thus it has the potential to achieve a better current match. However, it might not be as power efficient as the topologies discussed above, because it has static currents.

2.2.3. Programmable Divider

The programmable divider is critical for the frequency synthesis. In the FDMA wireless system, various LO frequencies are achieved by adjusting the division ratio of the programmable divider. Basically, there are two different architectures of the programmable divider. One is based on a two-modulus prescaler and the other is composed of multiple stages 2/3 divider cells.

Programmable divider based on two-modulus prescaler

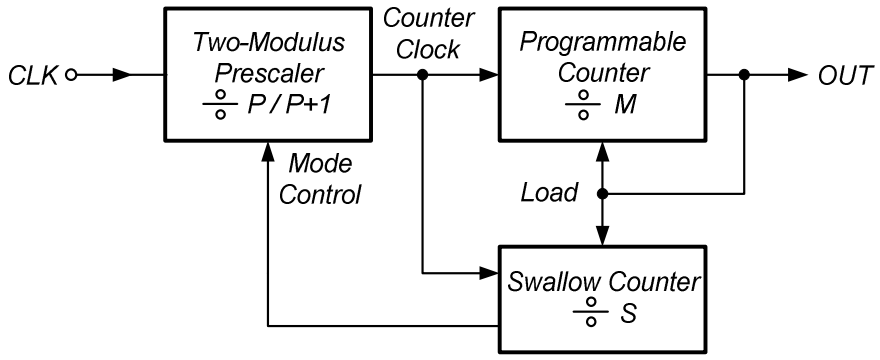


Figure 2.14 Programmable divider based on two-modulus prescaler

Figure 2.14 illustrates the conventional programmable divider based on a two-modulus prescaler [28]. The two-modulus prescaler is a frequency divider whose division ratio can be switched from one value to another by an external control signal, called 'Mode Control'. When the system turns on, the programmable counter is set to M while the swallow counter is set to S. S must be smaller than M. The prescaler

divides by P+1. At the same time, the programmable counter and swallow counter both count down, employing the prescaler output as the clock input. When the swallow counter times out, it generates a control signal 'Mode Control' to the prescaler, switching the prescaler to divider-by-P. The programmable counter continues counting down, using the prescaler output as the clock. In the whole procedure, the output of the programmable divider always gives a low level. When the programmable counter finishes, it generates a high-level pulse as the output of the whole programmable divider. In the meantime, the programmable counter and the swallow counter are reloaded to their original values, ready for the next divider period.

According to the operation process, the total periods of the input clock included in one output period is

$$N = (P + 1) \cdot S + P \cdot (M - S) = PM + S \tag{2.5}$$

which is also the division ratio of the programmable divider. To ensure the continuous integer step for N, the following conditions must be satisfied:

$$S \leq P - 1, \; S \leq M$$

Then the smallest possible division ratio is given by

$$N_{\min} = PM_{min} + S_{min} = P(P - 1) + 0 = P^2 - P \tag{2.6}$$

The highest division ratio is given by:

$$N_{\max} = PM_{max} + S_{max} \tag{2.7}$$

Here the $M_{\max}$ and $S_{\max}$ are determined by the size of the programmable counter and swallow counter. Considering an 8/9 two-modulus prescaler with a 3-bit swallow counter and an 8-bit programmable counter, a continuous division range of 56~2047 could be achieved. As can be seen, the programmable divider based on the two-modulus prescaler is capable of realizing a quite wide continuous division range. However, its complex architecture brings difficulties to the designers. Furthermore, high power consumption is also a disadvantage.

Programmable divider based on 2/3 divider cells

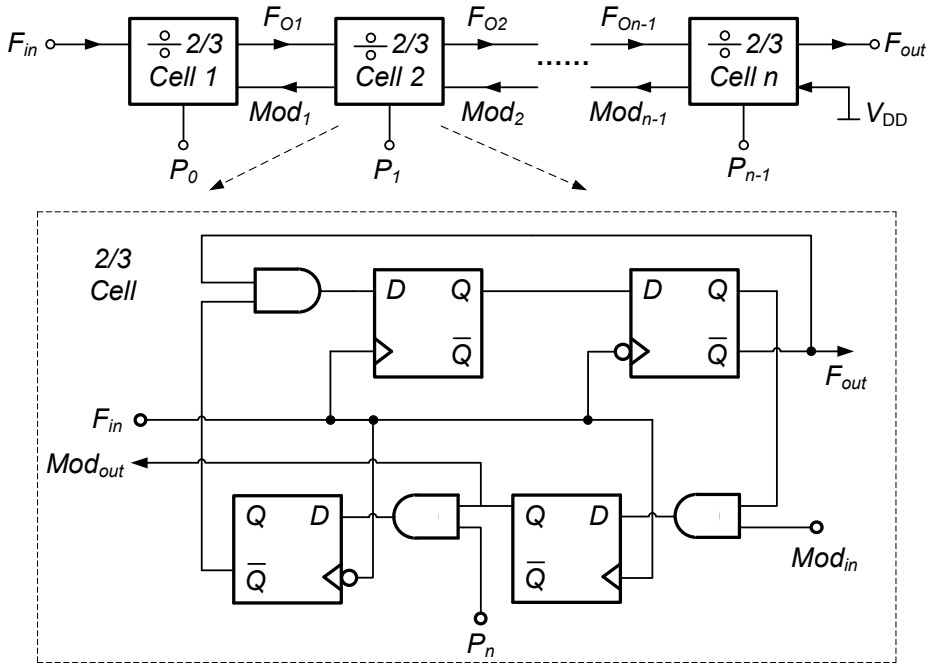


Figure 2.15 Programmable divider based on 2/3 divider cells

Another approach to designing the programmable divider is to use multiple cascaded stages of 2/3 divider cells [29][30], as described in Figure 2.15. The 2/3 cell is a frequency divider which can switch its division ratio between 2 and 3 according to the control input P_n. Once the mod signal from the next stage cell becomes high in a division cycle, the cell can divide by 3 depending on the state of its control input. If the P_n is '1', division-by-3 occurs. If the P_n is 0, the cell divides by 2 as usual. Unlike the architecture in [31], a common strobe signal is not required in this case, which makes the low-power design possible [29]. In this way, a chain of n-stage cascaded 2/3 cells could provide this division ratio

$$N = 2^n + P_{n-1} \cdot 2^{n-1} + P_{n-2} \cdot 2^{n-2} + \cdots\cdots + P_1 \cdot 2^1 + P_0 \cdot 2^0 \qquad (2.8)$$

It can achieve a continuous division range from 2^n to $2^{n+1}+1$. If this division range is not sufficient, it can be extended by combining this architecture with a programmable counter [29].

The programmable divider based on 2/3 divider cells has a modular architecture. The size of each 2/3 cell is supposed to be optimized for low power consumption according to different operation frequencies, but they could share the same layout. Compared with the architecture based on the two-modulus prescaler, it clearly has a simpler structure. The only drawback might be the difficulty in achieving a wide division range.

2.3. Frequency Synthesizer Architecture

Three basic architectures of frequency synthesizers will be introduced briefly.

2.3.1. Integer-N Architecture

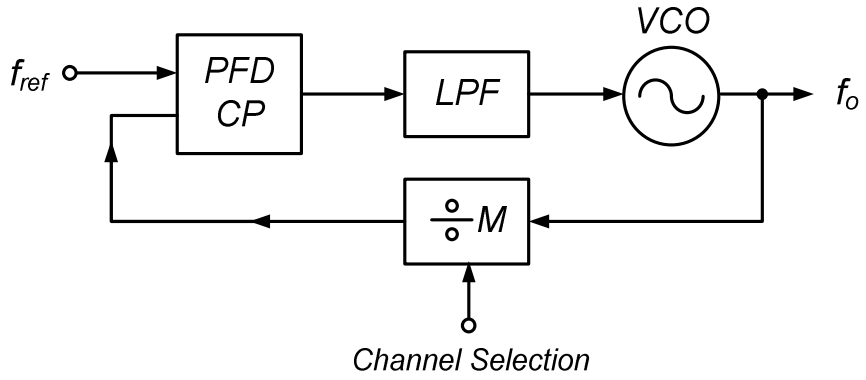


Figure 2.16 Integer-N frequency synthesizer

Employing an integer programmable divider in the feedback path, a CP-PLL is able to accomplish frequency synthesis, as shown in Figure 2.16. A number of various output frequencies f_{out} could be generated by selecting a different division ratio N. The following frequency relationship is established

$$f_{out} = f_{in} \cdot N \tag{2.9}$$

In this architecture, since the division ratio of the programmable divider varies with integer steps, the reference frequency must be equal to or smaller than the channel spacing in order to select all channels in the FDMA radio system. For most GHz

wireless applications, the channel spacing is usually less than 100 kHz. With such a low-frequency reference, a very large division ratio is required to generate a GHz LO signal.

As for the GSM-900 application, 25 MHz bands are allocated for transmit band 890 – 915 MHz and receive band 935 – 960 MHz. For the transmit band, the frequency synthesizer should generate 124 LO carriers for 124 channels with 200 kHz channel spacing. Employing a 200 kHz reference signal, integer-N synthesizer must achieve a continuous division range of 4450 ~ 4574. Such a large division ratio contributes a considerable phase noise multiplication to the synthesizer's out-band phase noise. In theory, this noise contribution could be equal to $20\log(4450) \approx 73$ dB.

Additionally, the reference spur is a critical issue. Since the reference frequency equals to the channel spacing, the reference spur of the LO signal would simultaneously down-convert the information in the adjacent channel to the baseband. This degrades the system's BER. In other words, the reference spur from the integer-N architecture would greatly worsen the selectivity of the receiver.

Besides, such a low-frequency reference restricts the use of a large loop bandwidth. Typically, the loop bandwidth is limited to less than one tenth of the reference frequency for stability consideration. Consequently, the frequency synthesizer is unable to achieve a fast loop settling.

2.3.2. Fraction-N Architecture

As discussed above, a number of drawbacks in the integer-N frequency synthesizer stem from the low reference frequency, which must equal to the channel spacing. These problems could be overcome by adopting a fractional frequency divider in the feedback loop, instead of an integer frequency divider.

In a simple fractional-N synthesizer as shown in Figure 2.17, the two-modulus divider is toggled by a modulus control signal, varying its division ratio between two integer values. As a result, a 'time-average' fractional divider ratio could be realized at the divider output. If the divider divides by N for K output pulses and by N+1 for F-

K pulses, then it can assumed that the equivalent division ratio at the divider output is equal to

$$\frac{K \cdot N + (N+1) \cdot (F-K)}{F} = N + \frac{F-K}{F} \tag{2.10}$$

N is the integer division ratio while the $(F\text{-}K) / F$ is a fractional value. The modulus control of the divider could be achieved by an accumulator. F is the size of the accumulator fixed by the number of bits. The programmable input K determines the fractional division value. Whenever the overflow occurs, the carry-out bit of the accumulator will toggle the modulus of the divider.

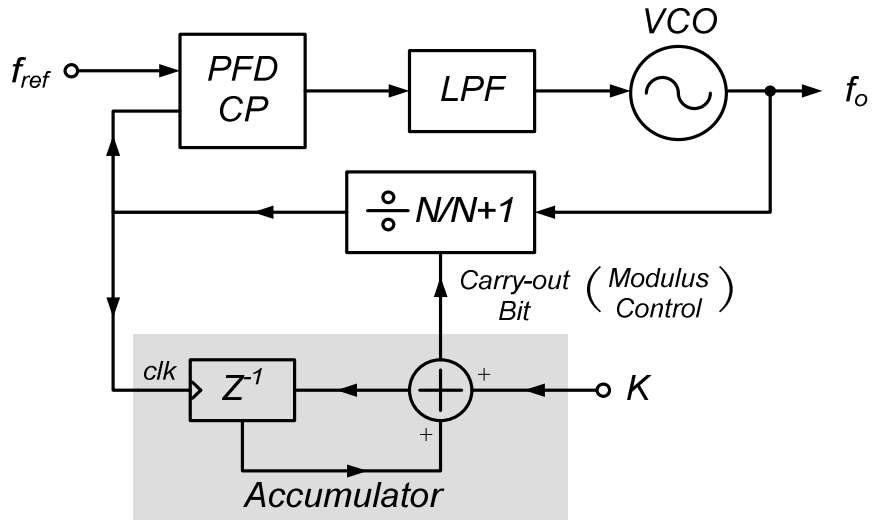


Figure 2.17 Simple fractional-N synthesizer with two-modulus divider

Let's analyze the GSM-900 application illustrated above. The transmit band from 890 MHz to 915 MHz includes 124 channels with 200 kHz spacing. Employing 51.2 MHz as reference frequency f_{ref}, in order to realize 200 kHz step, the size of the accumulator is equal to

$$F = \frac{51.2MHz}{200kHz} = 256 \tag{2.11}$$

It can be achieved through an 8-bit accumulator. The 124 LO frequencies from 890 MHz to 915 MHz could be synthesized as

$$f_o = 51.2MHz \cdot \left(17 + \frac{K}{256}\right) \tag{2.12}$$

where the integer number *N* equals 17, while the programmable input K = 98, 99,⋯ , 223 for channel selection. When the loop gets stable for a programmed input *K*, the feedback loop is divided by 17 for *K* reference cycles and by 18 for the rest 256-*K* reference cycles. Consequently, the equivalent time-average division ratio is equivalent to (17+*K*/256). Compared with the integer-N solution, the fraction-N synthesizer could use higher reference frequency and a smaller loop division ratio. The high-frequency reference allows a large loop bandwidth, finally yielding a fast loop transient as well as suppression to close-in phase noise. Besides, a small division ratio indicates less phase noise additions from the dividers.

For the above example, a 17/18 two-modulus prescaler is used to create the desired fractional division ratio. Similarly, the fraction function could also be realized by the use of a multi-modulus divider with the accumulator [21].

Unfortunately, the fractional architecture produces unwanted spurious frequency components close to carrier. In the operation of the fraction divider, the module of the divider is toggled once the overflow occurs in every *F* cycles. This periodic change of the divider ratio would generate spurious components in the frequency domain, which are located at the multiple harmonics of $f_{ref} \cdot (K/F)$ with respect to the carrier frequency. These spurs are usually called the fractional spur. Theoretically, these spur tones could be suppressed by employing a high-order loop filter. However, the fraction-N architecture is designed specifically for small frequency steps as well as a large loop bandwidth. Therefore, it is practically impossible to suppress the fractional spur through the design of a high-order loop filter.

A practical method to remove the spur is by the use of fractional compensation [15]. But it would easily fail when a current mismatch exists. This

method would be influenced by process variations. Sometimes, external adjustments are necessary for the accurate compensation. To avoid generating the fractional spur, many other techniques have been introduced, such as Phase interpolation [32] and Wheatley random jittering [32]. To implement the former, a D/A convertor is required. For this reason, it may suffer high power consumption and hardware complexity. As for the latter, it would introduce broadband noises to the divider, degrading phase noise performance.

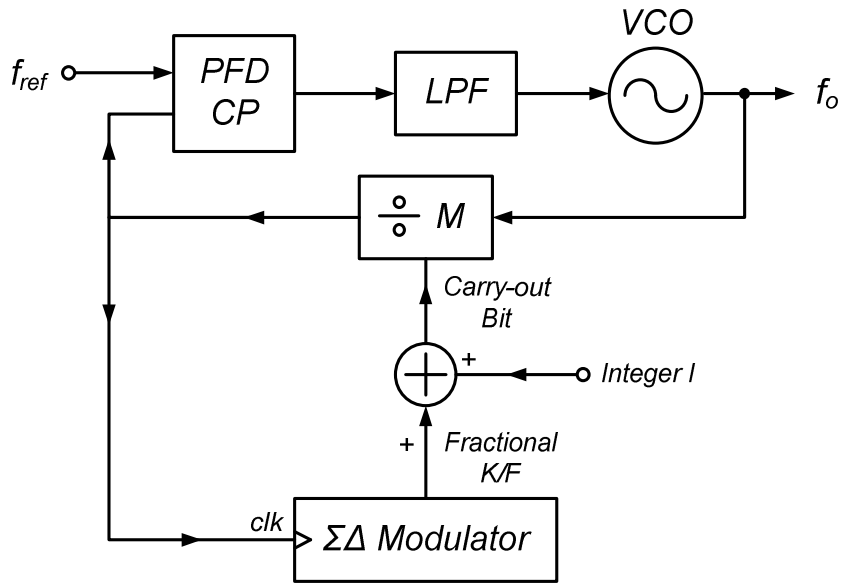


Figure 2.18 Fractional-N frequency synthesizer with ΣΔ modulator

In terms of noise performance, the best choice is to generate the modulus controlling signal from a ΣΔ modulator [33][34]. The ΣΔ modulator could manipulate randomly the modulus of the divider without affecting the average division ratio. This technique actually breaks up the periodic change of the divider modulus. Consequently, the spur tone is converted to the random noise, namely the quantization noise. Meanwhile, thanks to the noise shaping function of the ΣΔ modulator, the power spectrum of generated quantization noises is concentrated at high frequencies. Accordingly, the noise of the divided carrier is spread mostly in the area of the large frequency offset with respect to the divided carrier. The noise in the vicinity of the divided carrier is small. Finally, the noise at the large frequency offset is suppressed

by the LPF. Figure 2.18 shows a simplified block diagram of a ΣΔ modulator-based fractional-N frequency synthesizer. The ΣΔ modulator generates the fractional division ratio together with the integer division ratio, to manipulate the multi-modulus divider.

In brief, thanks to the ΣΔ modulator, the constructed fractional-N synthesizer is capable of providing a low phase noise carrier signal with small spurious frequency components. A large loop bandwidth would also be designed for a fast loop transient response. The problem with this solution may be the slightly higher power consumption and increased design complexity.

2.3.3. Direct Digital Synthesis

The frequency synthesizer based on phase locking is the most widely used frequency-synthesis technique. Through the phase locking between the input and output, a frequency relationship between the carrier and the reference signal could be built. The PLL-based synthesizer is capable of generating a high-frequency carrier with low phase noise from a low-frequency reference. Unlike the PLL-based frequency synthesizer operating in the analog domain, the direct digital synthesis (DDS) is another frequency-synthesis technique based on digital circuits.

The basic concept of the DDS is to generate, sample and modulate a signal in the digital domain, then eventually employ a digital-to-analog convertor (DAC) and a filter to reconstruct the signal in the analog domain. Figure 2.19 describes a conventional architecture for DDS. The tuning word (TW), which is a binary number, is the main input of the DDS. The phase accumulator generates the phase information of a sine wave based on the TW stored in the frequency register. The phase-to-amplitude converter creates the amplitude of the sine wave according to the phase information generated by the phase accumulator. A practical achievement of a phase-to-amplitude converter is the read-only memory (ROM) sine lookup table. The phase accumulator computes the phase address for the ROM lookup table, which stores the amplitude information of the sine wave. Accordingly, the DAC generates the analog

voltage of a sine wave, matching the digital amplitude value in the ROM lookup table. Eventually, a smoothing LPF is used to suppress the high-frequency components.

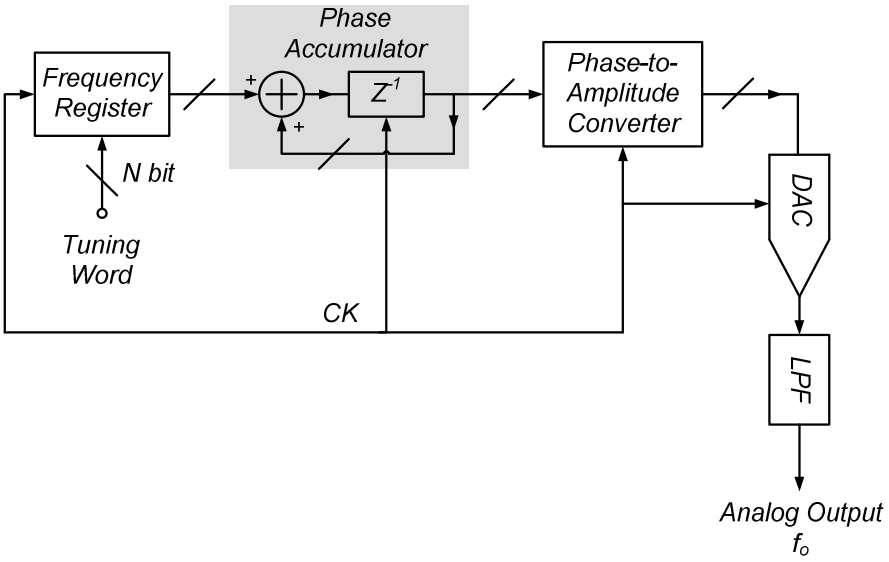


Figure 2.19 Direct digital synthesis

The phase accumulator operates as an adder. It adds the TW stored in the frequency register in each clock cycle. Once the overflow occurs, the phase accumulator completes an equivalent period of the sine wave. The phase increment step is defined by the TW according to desired output frequency. If the phase increment is larger, so is the step of the phase accumulator, which implies a higher frequency sine wave. On the contrary, a low frequency sine wave would be generated with a small phase increment. The DDS output frequency is thus represented as [15]

$$f_{out} = \frac{TW}{2^N} \cdot f_{ck} \tag{2.13}$$

N is the bit number of the adder. As the main input, the TW directly determines the output frequency of the DDS.

Except for the LPF, the other blocks of the DDS need to be clocked with a very precise, low-jitter waveform. From the Nyquist sampling theory, the clock frequency f_{ck} must be at least twice the output frequency f_{out}. In practice, f_{ck} should be much larger than the Nyquist-frequency for better noise performance. Meanwhile, the

phase noise of the output is significantly affected by the jitter of the clock. The requirement of a low-jitter high frequency clock with respect to the output signal, restricts the extensive use of the DDS.

Compared with the PLL-based frequency synthesizer, DDS presents a number of advantages. Due to the digital operation, DDS could achieve a fast frequency tuning as well as a fine frequency solution. For this reason, it allows direct frequency and phase modulations in the digital domain [21]. With the rapid advance of digital CMOS technology, today's DDS becomes more compact and consumes less power.

2.4. Loop Performance

As a feedback system, the PLL operates in the closed-loop mode. Thus, the loop design is of great significance for the overall performance. The function of the PLL-based frequency synthesizer is to generate a low phase noise LO carrier at the desired frequency. The output frequency of the loop has to stably experience a dynamic transient to reach the desired frequency. Therefore, the stability of the loop must be guaranteed, meanwhile the transient response of the loop must be convergent. Additionally, the noise property of the loop is considerable for low output phase noise.

In this part, the behavior model of each building block in the PLL is introduced first. Then the stability, dynamic performance and noise property of the loop are further analyzed.

2.4.1. Transfer Function

Unlike the amplifier, the object that the PLL processes is not the signal amplitude but the phase. Therefore, the model of circuits in the PLL refers to the phase-based small signal linear transfer function. This section concerns the derivation of the transfer function for the VCO, frequency divider and charge pump. Together with the transfer function of the loop filter, a linear model of the frequency synthesizer could be constructed, and then used for the design of the loop performance.

Voltage controlled oscillator

The output frequency of the VCO is determined by the control voltage, which is $\omega_{out} = \omega_o t + 2\pi \cdot K_{VCO} \cdot V_{cont}$. The Unit of the K_{VCO} is Hz/Volt. Then the total phase of the output signal is

$$\phi_{out} = \int \omega_{out} dt = \omega_o t + 2\pi \cdot K_{VCO} \int V_{cont} dt \tag{2.14}$$

The second term of the right side is called excess phase [18], which is $\phi_{ex} = 2\pi \cdot K_{VCO} \int V_{cont} dt$. In the linear model of the PLL, the VCO is regarded as a system, whose input is the control voltage V_{cont} and the output is the excess phase ϕ_{ex} [18]. Its transfer function is expressed as

$$\frac{\Phi_{ex}}{V_{cont}}(s) = \frac{2\pi \cdot K_{VCO}}{s} \tag{2.15}$$

Therefore, the model of the VCO in the PLL is an ideal integrator.

Frequency divider

We suppose a frequency divider with a division ratio of *N*. In other words, the frequency relationship of the input frequency ω_o and output frequency ω_{div} is given by

$$\omega_{div} = \frac{\omega_o}{N} \tag{2.16}$$

Similarly, the total phase of the output signal is

$$\phi_{total} = \int \omega_{div} dt = \frac{\int \omega_o dt}{N} \tag{2.17}$$

while the $\int \omega_o dt$ is the total phase of the input signal. Thus, the transfer function of a frequency divider by *N* is

$$\frac{\Phi_{out}}{\Phi_{in}}(s) = \frac{1}{N} \tag{2.18}$$

Charge pump and phase frequency detector

The transfer function of the charge pump and PFD is derived for the simple structure shown in Figure 2.8. When a phase difference exists at the input, the charge pump provides current pulses with I_{cp} mA magnitude. Obviously, the charge pump is a discrete-time system. However, if the loop bandwidth is much less than the reference frequency, the PLL would seem to be a continuous-time system [15]. The discrete current pulses of the charge pump could be seen approximately as a continuous signal, which has the same average value as the discrete signal. Since the time-averaged current output of the charge pump is $(I_{cp}/2\pi)$ mA/radian, the PFD and charge pump could be regarded as a phase-to-current convertor with a gain of $(I_{cp}/2\pi)$ mA/radian. As a result, the transfer function is expressed as

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_{cp}}{2\pi} \tag{2.19}$$

where the $\Delta\phi$ corresponds to the input phase difference. The continuous-time approximation would become unacceptable when the operation frequency of the PDF approaches the loop bandwidth. As a rule of thumb, the loop bandwidth is typically designed to be less than one tenth of the reference frequency.

2.4.2. Loop Stability

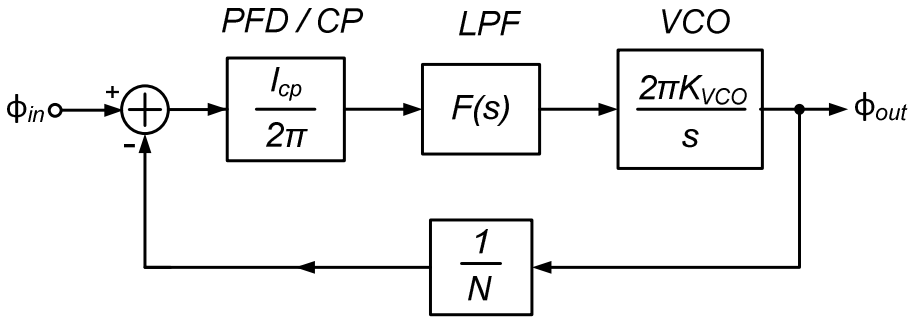


Figure 2.20 Linear model of the PLL-based frequency synthesizer

Based on the transfer function of each building block already discussed, a linear model of the PLL-based frequency synthesizer is created as Figure 2.20. When the loop becomes stable, the current mismatch, clock feedthrough and charge injection would cause voltage jumps and ripples on the control voltage of the VCO [21]. The simplest approach for removing voltage jumps and high frequency noises is to use a shunt capacitor in the LPF, as shown in Figure 2.8. As a result, the open-loop gain would have two poles at the origin, expressed as

$$H(s)_{open} = \frac{I_{cp} K_{VCO}}{N C_p s^2} \tag{2.20}$$

As mentioned at the beginning of the chapter, it is called type-II PLL. Because of these two poles at the origin, the loop would not stabilize. Because each pole contributes a -90º phase shift, the open-loop gain results a total of -180º phase shift at the gain crossover, forcing the system to oscillate. On the other hand, the zero would induce a +90º phase shift to the loop. Therefore, the zero could be added to the loop, driving the total phase shift to less than -180º at the gain crossover. It leads to the linear model of the desired PLL as shown in Figure 2.21.

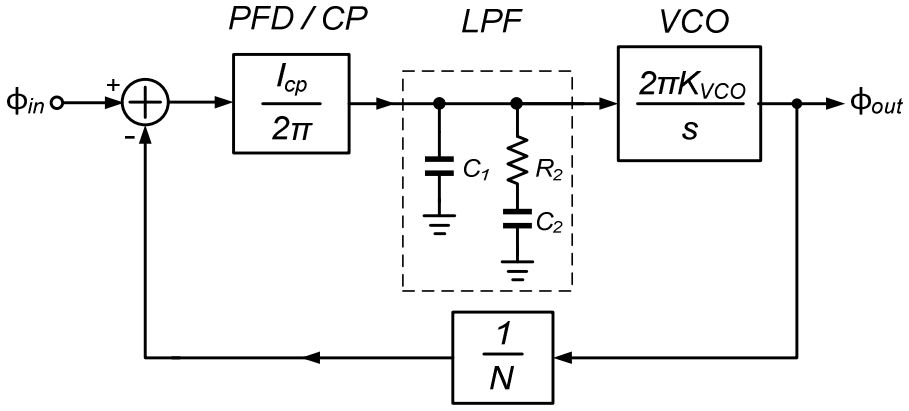


Figure 2.21 Linear model of the PLL-based frequency synthesizer with a 2nd order LPF

Apart from two poles at the origin, the employed 2nd order LPF provides another pole and a zero. The time constant of the 3rd pole and the zero are equal to

$$T_{pole} = R_2 \cdot \frac{C_1 C_2}{C_1 + C_2} \tag{2.21}$$

$$T_{zero} = R_2 \cdot C_2 \tag{2.22}$$

Obviously, the frequency of the zero is smaller than that of the 3rd pole. The open-loop gain is further given by

$$H(s)_{open} = \frac{I_{cp} K_{VCO} (1 + sT_{zero})}{NC_1 s^2 (1 + sT_{pole})} \tag{2.23}$$

The PLL has one zero and three poles, two of which are at the origin. It is a 3rd order system.

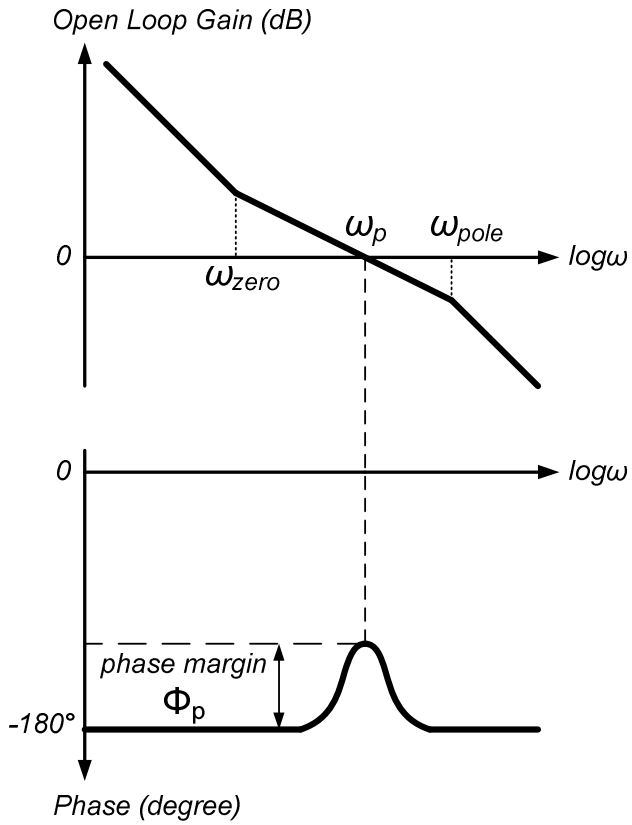


Figure 2.22 Bode plot of open-loop gain frequency response

As shown in the Bode plot of Figure 2.22, the phase of the open-loop gain begins with -180° from the origin. Afterwards, the zero induces a 90º phase shift,

stabilizing the loop. However, the 3rd pole provides a negative phase shift as well, making the loop total phase tend to be -180º. Therefore, the relative positions of the 3rd pole and the zero influence the phase margin and the bandwidth of the open-loop. To ensure stability, the frequency of the zero ω_{zero} must be much smaller than that of the pole. As a rule of thumb, the value of C_2 is designed to be 5 or even 10 times greater than the C_1.

For the stability design, the phase margin of the open-loop gain must be specified. The designed phase margin should be between 60° and 80° to ensure loop stability. Meanwhile, we hope that the smallest phase shift occurs at the gain crossover. That is to say, the gain crossover is located between the zero and the 3rd pole. In the meantime the phase margin reaches maximum when the magnitude of the open-loop gain reaches unity, as illustrated in Figure 2.22. Based on these two relationships, the calculation of time constant T_1 and T_2 results in [35]

$$T_1 = \frac{sec\phi_p - tan\phi_p}{\omega_p} \tag{2.24}$$

$$T_2 = \frac{1}{\omega_p^2 \cdot T_1} \tag{2.25}$$

Here the ω_p is the gain crossover frequency, which is also named the open-loop bandwidth. As already discussed, relative positions of the 3rd pole and the zero of the LPF determine the loop bandwidth and the phase margin. Given the open-loop bandwidth and the phase margin in turn, the frequency of the 3rd pole and the zero would be calculated. Eventually, values of LPF parameters C_1, C_2 and R_2 are fixed as [35]

$$C_1 = \frac{T_1}{T_2} \cdot \frac{I_{cp} \cdot K_{VCO}}{\omega_p^2 \cdot N} \sqrt{\frac{1+(\omega_p \cdot T_2)^2}{1+(\omega_p \cdot T_1)^2}} \tag{2.26}$$

$$C_2 = C_1 \cdot \left(\frac{T_2}{T_1} - 1 \right) \tag{2.27}$$

$$R_2 = \frac{T_2}{C_2} \tag{2.28}$$

After the design of the VCO and the charge pump, the parameters of 2nd order LPF could be set with a specified open-loop bandwidth and a phase margin. The value of I_{cp} clearly influences the design of LPF.

2.4.3. Dynamic Performance

Stability is the first consideration for the design of whole loop performance. The dynamic performance of the loop is also of importance. As mentioned above, the phase tracking and locking acquisition is no longer a design issue for the CP-PLL. Hence, the discussion of the loop dynamic performance mainly concerns the transient response of the loop.

For the PLL-based frequency synthesizer, a loop transient response occurs if a different carrier frequency is selected by changing the division ratio of the programmable divider. It has been proven that the transient response caused by the change of the divider modules is the same as the step response produced through a change of the reference frequency [15]. Unlike the stability design which is related to the open-loop property, the analysis of the PLL dynamic performance concerns the step transient response of the closed-loop system. For the linear system shown in Figure 2.21, the closed-loop transfer function is expressed as

$$H(s)_{close} = \frac{NK\frac{1}{C_1}\left(s + \frac{1}{T_{zero}}\right)}{s^3 + \left(\frac{1}{T_{pole}}\right)\cdot s^2 + \left(\frac{K}{C_1}\right)\cdot s + \frac{K}{C_1 \cdot T_{zero}}} \tag{2.29}$$

$$K = \frac{I_{cp}K_{VCO}}{N} \tag{2.30}$$

It is difficult to derive directly the step response for this 3rd order system. Remember that the 3rd pole produced by the LPF is designed at a very high frequency. It is normally located quite far from the zero and beyond the gain crossover in order to

ensure stability. If the 3rd pole is 5 to 10 times larger than the zero frequency, this 3rd order system could be simplified to a 2nd order system, which has a similar closed-loop response [36]. As a result, the analysis of the closed-loop transient response focuses on the PLL system as shown in Figure 2.23.

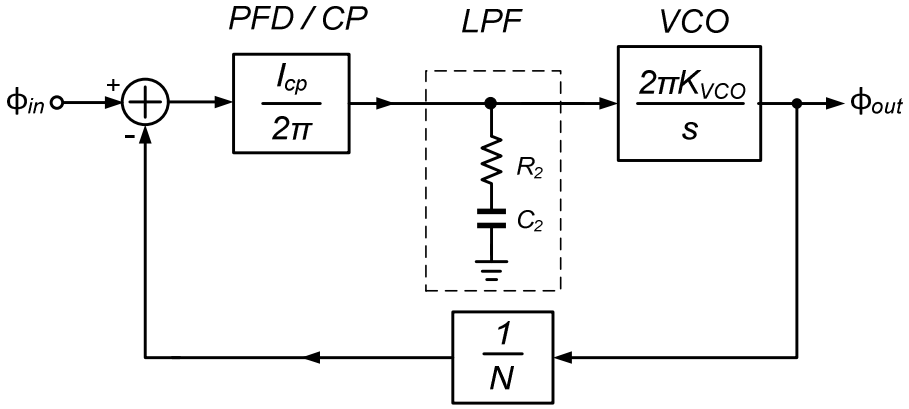


Figure 2.23 Linear model of the frequency synthesizer with a series-RC LPF

The LPF is composed of a series combination of a resistor and a capacitor. It provides a pole at the origin and a zero with the time constant equals to

$$T_{zero} = R_2 \cdot C_2 \tag{2.31}$$

Its transfer function is given by

$$F(s) = \frac{R_2 C_2 s + 1}{C_2 s} \tag{2.32}$$

And the closed-loop transfer function is simplified to be

$$H(s)_{close} = \frac{NKR_2\left(s + \frac{1}{T_{zero}}\right)}{s^2 + (KR_2)s + \frac{K}{C_2}} = \frac{2N\zeta\omega_n\left(s + \frac{\omega_n}{2\zeta}\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.33}$$

$$K = \frac{I_{cp} K_{VCO}}{N} \tag{2.34}$$

where the K refers to the DC open-loop gain. The natural frequency ω_n and the damping factor ζ are given by

$$\omega_n = \sqrt{\frac{K}{C_2}} \tag{2.35}$$

$$\zeta = \frac{\omega_n}{2} R_2 C_2 \tag{2.36}$$

The damping factor ζ is a measure of the overshoot and the ringing of the transient response. If $\zeta > 1$, the closed-loop function has only real poles, leading to an over-damped transient response. However, when $\zeta < 1$, poles of the function are complex. Consequently, the system experiences a damped oscillation. If the value of ζ is too small, the loop would have a long settling time or even be unable to stabilize. Meanwhile, the closed-loop frequency response would have a peak and the loop would need the design of stability. Typically, ζ is designed to be larger than 0.5 and preferably equal to $\sqrt{2}/2$, in order to achieve a flat frequency response. For the 2rd system with the $\zeta < 1$, the transient response stimulated by a step input of the reference signal is given by [15]

$$y(t) = \left[1 - \frac{1}{\sqrt{1-\zeta^2}} \exp(-\zeta \omega_n t) \times \sin\left(\omega_n \sqrt{1-\zeta^2}\, t + \Psi \right) \right] \tag{2.37}$$

where $\Psi = sin^{-1}\sqrt{1-\zeta^2}$. An approximation of the settling time is derived as [15]

$$t_s \approx \frac{1}{\zeta \omega_n} \ln \frac{k}{M |\alpha| \sqrt{1-\zeta^2}} \tag{2.38}$$

The parameter α refers to the settling accuracy of the transient response, representing how close the transient response is to the final value. As we can see, the settling time t_s is inversely proportional to the product ($\zeta\omega_n$). Good dynamic performance requires a fast and stable transient response. If ζ is set to be the ideal value $\sqrt{2}/2$, then ω_n

should be as large as possible, in order to achieve a fast settling of the loop. Thus, the loop natural frequency ω_n is a measure of the response time.

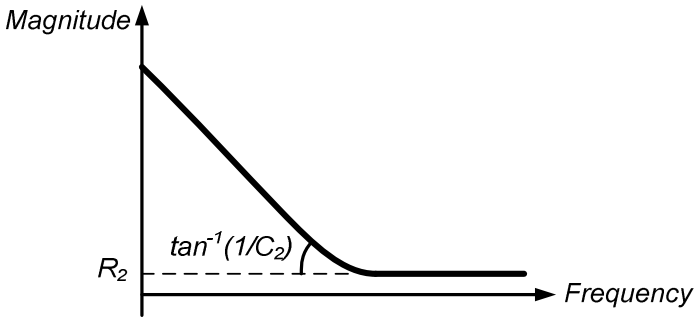


Figure 2.24 Magnitude response of the series-RC LPF

Figure 2.24 gives a sketch of the magnitude response of the LPF. As already mentioned, the LPF has a zero and a pole at the origin. At high frequencies, the magnitude response tends to be flat. $1/C_2$ actually represents the gradient of the magnitude decrease. Therefore, $1/C_2$ is proportional to the bandwidth of the LPF ω_{LPF}. Then the equation (2.35) could be altered to

$$\omega_n \propto \sqrt{K\omega_{LPF}} \tag{2.39}$$

Briefly, a large DC open-loop gain and large LPF bandwidth lead to a fast transient response. That is the reason why the loop gain is also regarded as one of the definitions of the loop bandwidth in the [37]. However, since the expression of ω_n and ζ are really connected, it is impractical to design their values independently. The simple analysis of the transient response is useful to obtain an intuitive understanding. Accurate simulation is definitely required in the practical design.

2.4.4. Noise Property

Noise property is the most important concern for the PLL design. As for the frequency synthesizer, good phase noises and low reference spurs need to be achieved at the output. In this section, we analyze how the loop design would influence the noise performance.

So far as is known, each building block would contribute phase noises at the output. In order to achieve good phase noises at the output, each block should be carefully designed in terms of phase noise performance. However, how the phase noise of each building block contributes to the total output phase noise depends upon the loop property. The noise transfer function is analyzed through the linear small-signal phase model as described in Figure 2.25.

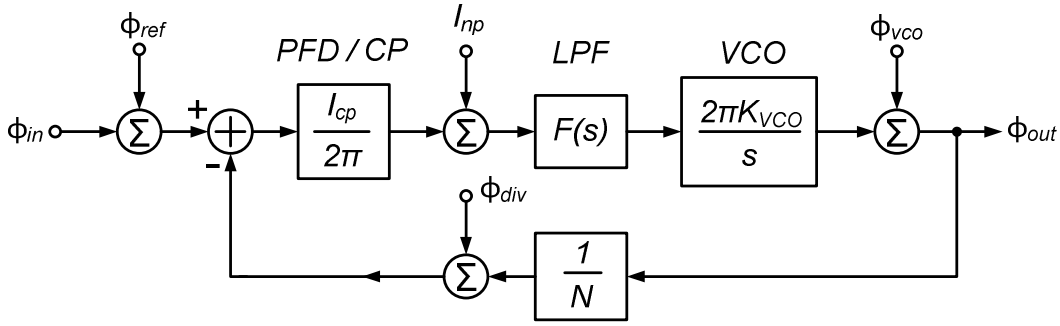


Figure 2.25 Linear small-signal phase model with noise additions

ϕ_{ref}, ϕ_{div} and ϕ_{VCO} represent the phase noise from the reference, frequency divider and VCO respectively. I_n is the noise current generated by the charge pump. As far as we know, the transfer function from one point in a feedback system to the output is calculated as

$$H(s)=\frac{ForwardGain}{1+LoopGain} \tag{2.40}$$

Accordingly, the noise transfer function from ϕ_{ref}, ϕ_{div} I_n and ϕ_{VCO} to the output are given by

$$H(s)_{ref}=\frac{\phi_{out}}{\phi_{ref}}=\frac{G(s)}{1+\frac{1}{N}G(s)} \tag{2.41}$$

$$H(s)_{div} = \frac{\phi_{out}}{\phi_{div}} = \frac{G(s)}{1+\frac{1}{N}G(s)} \tag{2.42}$$

$$H(s)_{np} = \frac{\phi_{out}}{I_{np}} = \frac{2\pi}{I_{cp}} \cdot \frac{G(s)}{1+\frac{1}{N}G(s)} \tag{2.43}$$

The transfer function of ϕ_{VCO} has a slightly different expression, which is

$$H(s)_{VCO} = \frac{\phi_{out}}{\phi_{VCO}} = \frac{1}{1+\frac{1}{N}G(s)} \tag{2.44}$$

$$\text{where} \quad G(s) = \frac{I_{cp}K_{VCO}}{s}F(s)$$

Note that except for the VCO noise, the noise transfer function of the other three noises all contain a common factor, which is

$$\frac{G(s)}{1+\frac{1}{N}G(s)} = \frac{1}{\frac{1}{G(s)}+\frac{1}{N}} \tag{2.45}$$

Its frequency response is shown in Figure 2.26. It shows a low-pass property with a -3 dB bandwidth ω_c. When the frequency is much lower than ω_c, it shows a level equal to N.

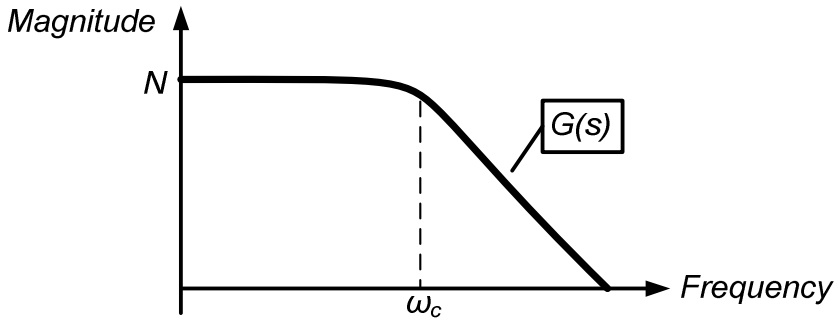


Figure 2.26 Frequency response of the common factor in noise transfer functions of reference, frequency divider and charge pump

On the contrary, the noise transfer function of the VCO's phase noise shows a high-pass characteristic, as displayed in Figure 2.27. Its magnitude reaches the maximum outside the -3 dB bandwidth. As a result, according to the noise transfer functions of different noises in the loop, it is deduced that the output phase noise inside the closed-loop bandwidth is determined by the phase noise from the reference, frequency divider and charge pump, while the phase noise contribution from the VCO would dominate the output phase noise, which is located outside the closed-loop bandwidth. The VCO noise contribution is usually called out-band noise, while the other noise contribution in the loop called in-band noise. Furthermore, notice that the noise transfer function for the in-band noise has an in-band flat with a magnitude of N. It leads to a 20logN noise addition when the phase noise of the frequency divider and the reference contributes to the output phase noise. This noise addition would be considerable if the division ratio is large.

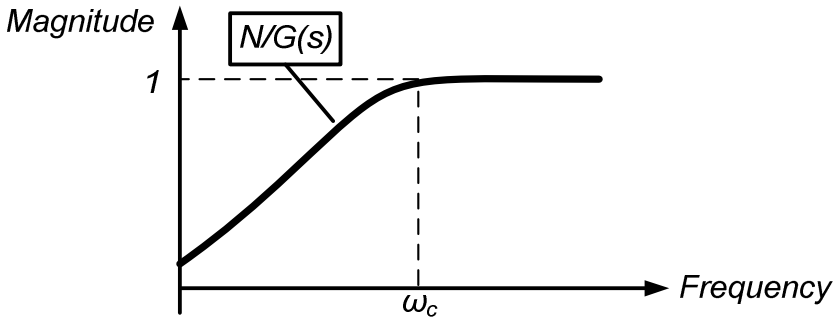


Figure 2.27 Frequency response of noise transfer function of VCO

The analysis of the noise transfer function provides a profound understanding about how the noise sources in the loop contribute to the total phase noise at the output. A good estimate of the output phase noise of the PLL certainly requires careful simulations. However, it is pretty difficult to accomplish the direct simulation for the whole PLL with the transistor-level circuits. This is because the simulator needs to use a time step small enough to reach a stable state. Meanwhile, if the division ratio N is large, the simulator would need a long simulation time to evaluate

the output spectrum. So the direct simulation consumes both time and memory, and is inefficient. The Ref [38] offers a approach to simulate the output phase noise with a phase domain model. Firstly, the noise performance of each block is simulated from the transistor-level schematic. The phase domain model is then built for each block. Eventually, the output phase noise could be simulated considering the contribution from each noise source.

Spurious frequency components could be seen in the spectrum of the output signal. It is caused by noises and disturbances on the VCO control line. There are many causes for the disturbance on the control line, such as clock feed-through, charge injection and current mismatch in the charge pump. Suppose that the disturbance is a continuous narrow pulse with Δt width and V_o height. It has been proven that the power level of the reference spur is proportional to ($V_o \cdot K_{VCO}$) [21]. To suppress the spur level, the frequency synthesizer could use a shunt capacitor in the LPF to reduce V_o and employ a switched-capacitor array for frequency tuning to minimize K_{VCO} [20].

A more useful approach to suppress the reference spur is to employ a high order LPF (order > 3). A typically solution is a 3rd order LPF as shown in Figure 2.28.

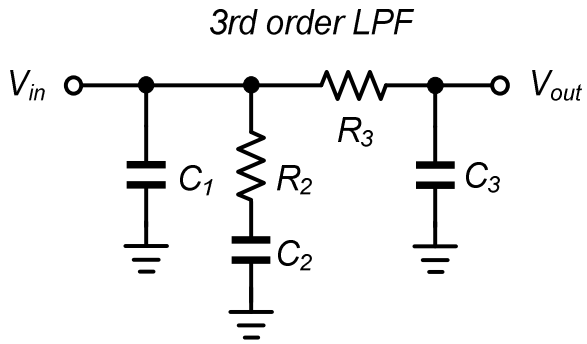


Figure 2.28 3rd order LPF

Compared with the 2nd order LPF, a high frequency pole is added to the loop. If the frequency of the 3rd pole is smaller than the reference frequency, the attenuation produced to the spur is calculated as [35]

$$ATTEN = 20\log\left[\left(2\pi \cdot f_{ref} \cdot R_3 \cdot C_3\right)^2 + 1\right] \tag{2.46}$$

But at the same time, the additional 3rd pole would alter the loop transfer function and the transient response, or even cause stability issues. Therefore, the 3rd pole of the LPF is usually designed to be far enough from the 2nd pole. As a rule of thumb, the product of R_3 and C_3 should be at least 1/10 the product of C_2 and R_2.

Based on the above analysis, a simple conclusion is given here. Principally, three most basic parameters are closely connected to the loop performance. They are the phase margin of the open-loop gain, the damping factor of the closed-loop response and the loop bandwidth. The phase margin of the open-loop gain is a direct indicator of the loop stability. It should be larger than 60° to ensure stability. Damping factor is a measure of closed-loop transient response. The ideal design value is $\sqrt{2}/2$ for a flat closed-loop frequency response. The loop bandwidth is actually the most important parameter. It determines directly the settling time of a step response, as well as the loop phase noise property. A large loop bandwidth leads to a fast transient response and a high suppression to VCO's close-in phase noise. This makes the total output phase noise dominated by the phase noise contribution from the reference, frequency divider and charge pump. Ref [37] gives there different definitions for loop bandwidth: open-loop bandwidth, closed-loop bandwidth and DC loop gain. Essentially, these three definitions are closely related and have the same significance for the loop design.

Chapter 3.
Millimeter-wave Frequency Generation Circuits

In chapter 2, the basic architecture of the PLL-based frequency synthesizer was introduced. A programmable divider is usually designed in the feedback loop, fulfilling the multiplication and adjustment of the output frequency. Generally, the programmable frequency divider has a complicated structure, composed of multiple building blocks. It is difficult to construct the programmable divider to operate at very high frequencies. Hence, to synthesize a mm-wave signal, the output frequency has first to be decreased to a relatively low frequency range, so that it can be applied to the programmable divider. This function could be achieved by multi-stage divide-by-2 circuits, as illustrated in Figure 3.1.

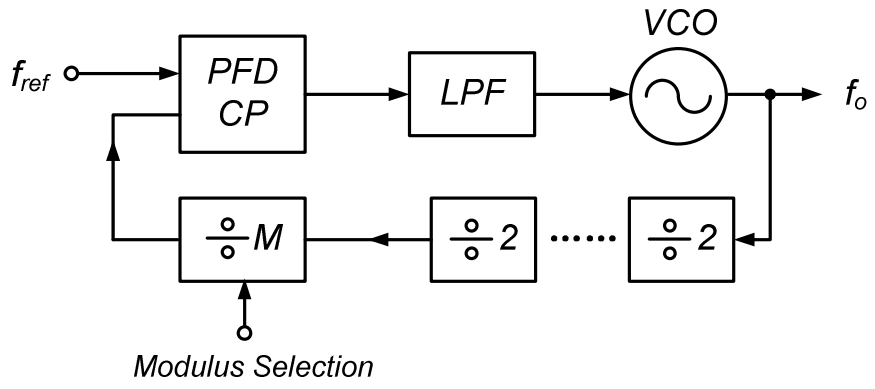


Figure 3.1 Frequency synthesizer for mm-wave signal generation

For a mm-wave frequency synthesizer as shown in Figure 3.1, the operation frequency decreases along the loop. Only the VCO and a few stages of 2:1 frequency dividers may operate at mm-wave frequencies. The remaining circuits actually operate at much lower frequencies. This chapter discusses design issues of the mm-wave frequency generation circuits, especially focusing on the VCO and the 2:1

frequency divider. Topologies of the mm-wave VCO are introduced first. Detailed analysis is applied specifically to the cross-coupled VCO to examine the theory of operation and noise properties. Finally, design issues of the mm-wave 2:1 frequency divider are discussed.

3.1. Millimeter-wave VCO Topology

As discussed in chapter 2, generally there are two categories of the integrated oscillator: ring oscillator and LC oscillator. Compared with the ring oscillator, the LC oscillator could operate at a higher frequency and provide a better phase noise performance. Thus, nearly all the mm-wave oscillators are LC oscillators. Four typical topologies of the mm-wave VCO are analyzed below.

3.1.1. Cross-coupled Oscillator

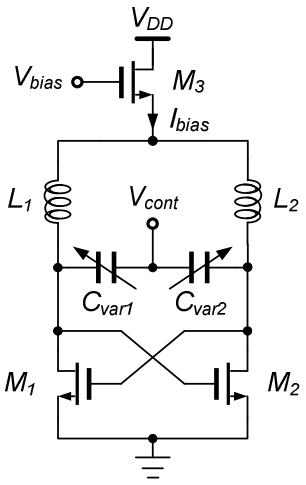


Figure 3.2 Cross-coupled VCO

The cross-coupled oscillator has been proved to be the most popular oscillator topology in the integrated RF transceiver. It comprises a cross-coupled transistor pair and a LC resonator, as depicted in Figure 3.2. Typically, MOS-varactors or pn-junction varactors are employed in the LC tank for frequency tuning. From the concept of the one-port oscillator, the cross-coupled transistor pair provides a negative

resistor to compensate the energy loss in the LC tank, maintaining the oscillation. The use of the current source brings two benefits. Firstly, it decreases the sensitivity to the supply voltage, suppressing the common-mode noise coupling. Additionally, it offers a high-impedance at the common-mode point, which is critical for the differential operation. The oscillation frequency is determined by

$$f_o = \frac{1}{\sqrt{L \cdot (C_v + C_p)}} \tag{3.1}$$

where the C_v and C_p correspond to the varactor capacitance and parasitic capacitance respectively. As for the type of cross-coupled and current source transistors, they could be either NMOS or PMOS transistors. As a result, four different topologies are built, as shown in Figure 3.3.

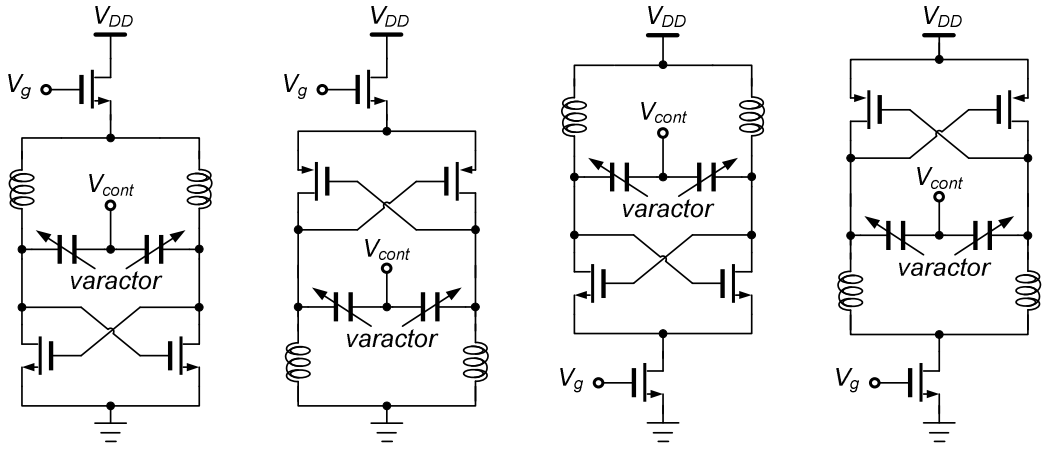


Figure 3.3 Different topologies of cross-coupled VCO

Basically, the PMOS transistor produces less noise than the NMOS transistor, but provides less gain. Therefore, in theory the VCO topology employing PMOS cross-coupled transistors and a PMOS current source would present the best phase noise performance. But due to the low gain of PMOS transistors, a large dc current or a large size of transistors is necessary to start the oscillation. The former means high power consumption. The latter will reduce the frequency tuning range. In general, the topology with a PMOS current source and a NMOS cross-coupled pair is preferable.

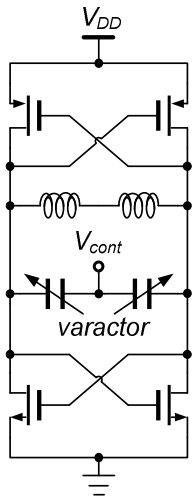


Figure 3.4 Complementary cross-coupled VCO

On the other hand, the oscillator could also employ a complementary cross-coupled pair, illustrated in Figure 3.4. In this case, the current source is usually removed to save the voltage headroom. Thanks to negative impedance provided by the additional cross-coupled pair, this topology theoretically reduces half the power consumption.

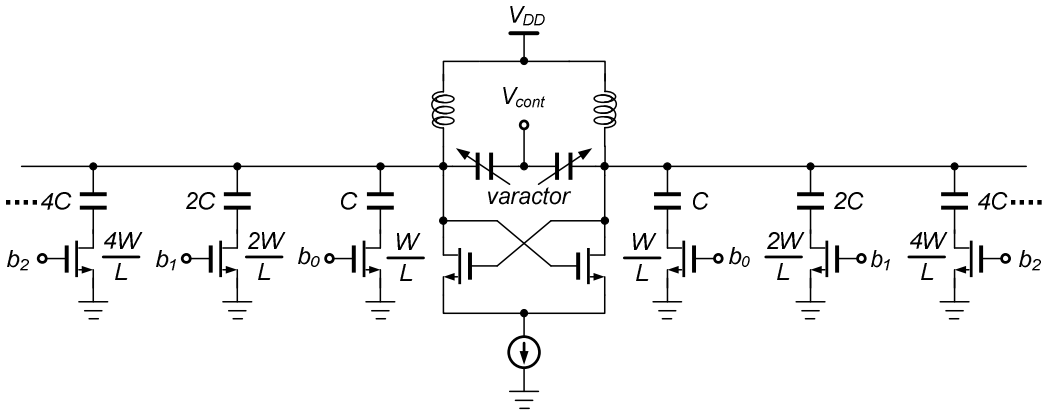


Figure 3.5 Wideband cross-coupled VCO with switched-capacitor array

Frequency tuning range is an important performance specification of the VCO. A large tuning range could be achieved simply by employing a large size varactor. In this way, the VCO would have a large tuning sensitivity, which leads to a high

sensitivity to AM noises and common-mode noises, finally degrading phase noise. A better method is to use the switched tuning technique [39]. Figure 3.5 shows a VCO with a switched-capacitor array. With this topology, the total band of interest is divided into multiple sub-bands and the varactor needs only to provide frequency tuning in the single sub-band. This approach achieves both a large tuning range and low tuning sensitivity.

3.1.2. Colpitts Oscillator

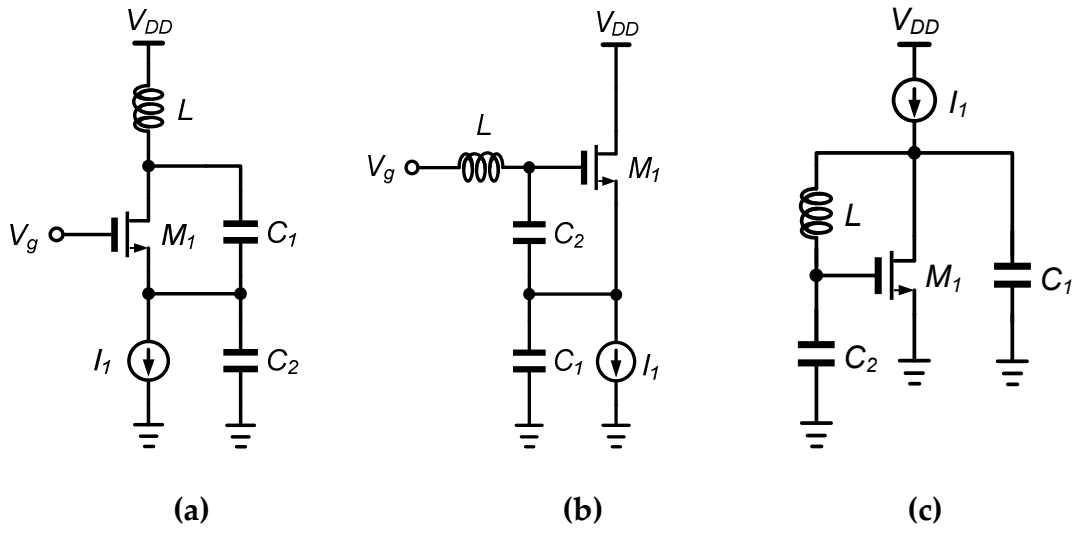


Figure 3.6 Colpitts oscillator [40]

The Colpitts oscillator, shown in Figure 3.6 (a), was invented in 1918 by American engineer Edwin H. Colpitts. Unlike the cross-coupled topology, the feedback for the active device in the Colpitts oscillator is taken from a voltage divider composed of two capacitors (C_1 and C_2 in Figure 3.6 (a)). From the concept of the one-port oscillator, the negative impedance of the Colpitts oscillator is built by a positive feedback through a capacitor voltage divider. As illustrated in Figure 3.7, the impedance Z_m is calculated as [18]

$$Z_m = -\frac{g_m}{C_1 C_2 \omega^2} + \frac{1}{C_1 s} + \frac{1}{C_2 s} \tag{3.2}$$

As a result, the negative resistor is equal to $g_m / C_1 C_2 \omega^2$.

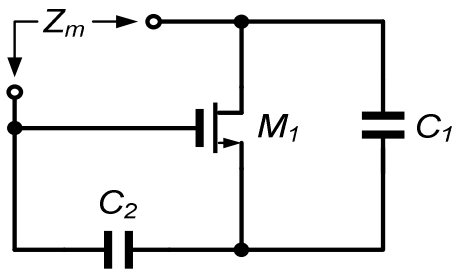


Figure 3.7 Negative impedance generation in Colpitts oscillator

As for the topology in Figure 3.6 (a), the bias is given at the gate, which is actually regarded as the ac ground. This topology is similar to the common-gate amplifier. Resembling the topologies of the common-source and common-drain amplifiers, two other topologies of the Colpitts oscillator could be constructed, as shown in Figure 3.6 (b) and (c). Figure 3.8 shows a differential topology of the Colpitts oscillator [41]. The varactor could be added in parallel with the inductor to achieve frequency tuning.

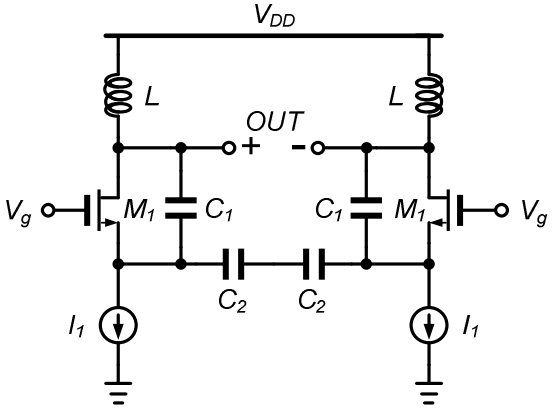


Figure 3.8 Colpitts oscillator with differential topology [41]

The Colpitts oscillator employs only one active device. In principle it contributes less noise than the cross-coupled oscillator. So generally, the Colpitts oscillator would achieve a lower phase noise than the cross-coupled one. But the

Colpitts oscillator needs nearly a quadruple gain of the cross-coupled oscillator to start oscillating [18]. Therefore, it is quite difficult to implement the Colpitts oscillator with CMOS technology due to the low gain of the CMOS transistor. It is more common to use Bipolar or GaAs technology to design the Colpitts oscillator.

3.1.3. Push-push Oscillator

The so called push-push oscillator refers to the oscillator that is oscillating at frequency f_o, but delivers its 2nd harmonic signal as the output. As a result, the oscillator operates at half of the output frequency. Meanwhile, taking the 2nd harmonics as the output, the frequency tuning range can easily be doubled. With this topology, the oscillator is capable of generating ultra-high frequency signals, even above 100 GHz. However, since the push-push oscillator actually outputs the 2nd harmonics, low output power is one of its drawbacks. As for the oscillator topology, it could be any category.

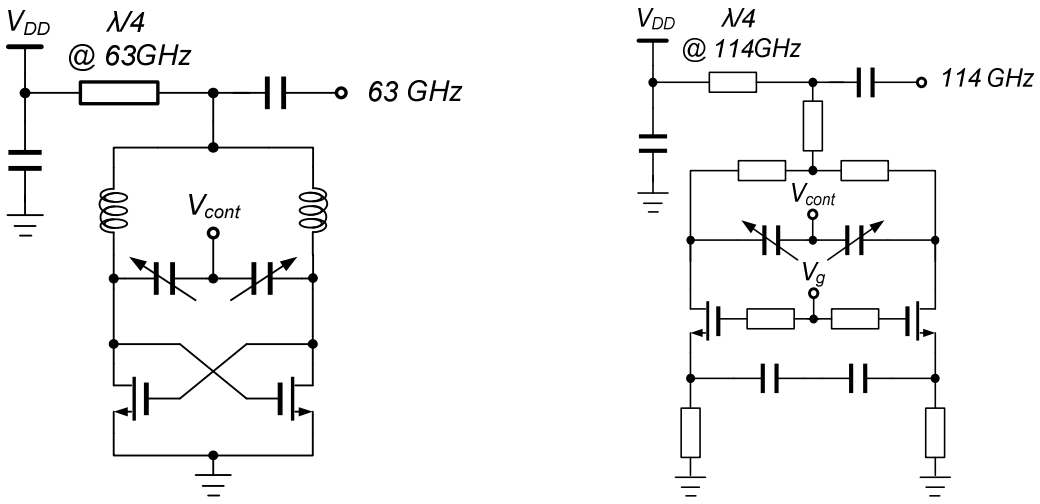


Figure 3.9 Push-push VCO

Figure 3.9 (a) presents a 63 GHz push-push VCO [42]. It employs the cross-coupled topology. The 2nd harmonic signal is extracted from the common-mode point.

A quarter wavelength transmission line at the 2nd harmonic frequency transfers the short circuit to open at the common-mode point. Consequently, the power of extracted 2nd harmonic signals is increased, while the fundamental signal is suppressed. Another example in Figure 3.9 (b) is a 114 GHz push-push VCO, using the topology of a differential Colpitts oscillator [43].

3.1.4. Distributed Oscillator

According to the oscillator model based on a feedback system, the cross-coupled oscillator is actually established by two stage amplifiers. Similarly, an oscillator could be realized as a feedback system composed of the distributed amplifier. This type of oscillator is called the 'distributed oscillator'. Figure 3.10 shows a basic architecture [44]. With the distributed architecture, it is capable of operating at high frequencies, even close to the cut-off frequency of active devices. Since the distributed oscillator usually employs a long transmission line, it would be area-consuming. To establish the feedback, the output is connected to the input of the distributed amplifier. This long connection line would bring a substantial resistance loss, degrading the phase noise. Besides, frequency tuning is also difficult to achieve [44].

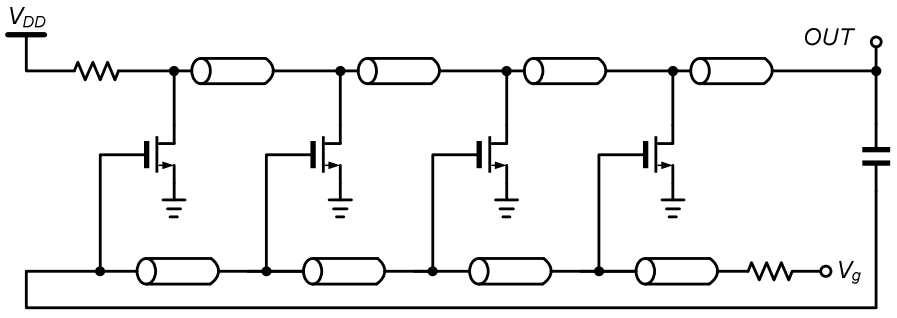


Figure 3.10 Basic architecture of the distributed oscillator

In the architecture shown in Figure 3.10, the signal is travelling between the input and output of the distributed amplifier. So it is called a travelling wave

oscillator [45]. A more efficient and simple architecture is the standing wave oscillator [46][47]. Figure 3.11 describes a λ/4 standing wave oscillator constructed by a differential transmission line and a cross-coupled transistor pair. The cross-coupled pair generates a negative impedance to maintain oscillation. The standing wave occurs in case $l = (\lambda/4) \times n \ \ (n = 1, 3, 5 \cdots)$, and the oscillation frequency is calculated as

$$f_o = \frac{n}{4l\sqrt{LC}} \tag{3.3}$$

where the l is the length of the transmission line, while the L and C are the inductance and capacitance per unit length of the transmission line. When a standing wave occurs, the voltage amplitude is at a maximum at the drain of the cross-coupled pair and a minimum at the common-mode point, as illustrated in Figure 3.11. A λ/2 standing wave oscillator could also result by simply combining two λ/4 standing wave oscillators [48].

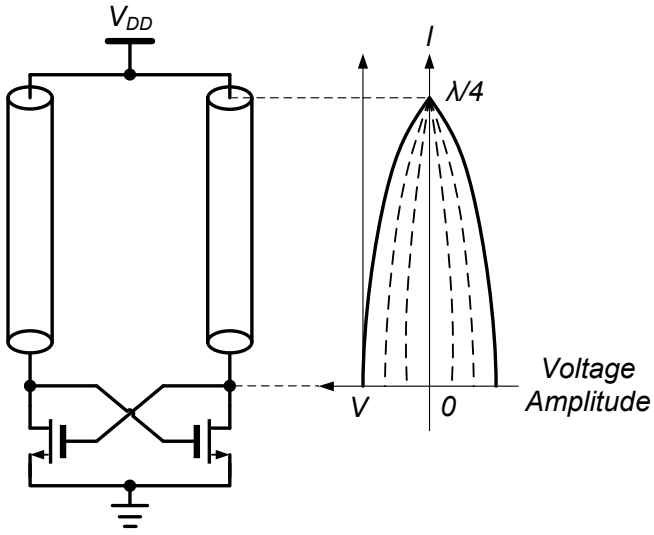
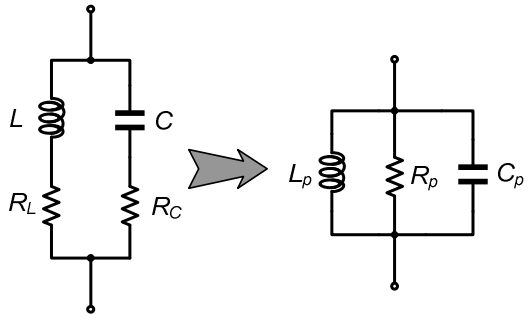


Figure 3.11 λ/4 standing wave oscillator

3.2. Analysis of Cross-coupled VCO

In principle, the cross-coupled VCO is the most popular topology used in frequency synthesizers. Understanding the theory of its operation is of great importance for a good design. The analysis is given to the conventional architecture as shown in Figure 3.2. The NMOS cross-coupled differential pair (M_1 and M_2) provides a negative impedance to maintain oscillation. The LC tank acts as the frequency selective network while the PMOS current source maintains a constant current for stable operation. The property of the LC tank circuit will be investigated first. Some theories of operation are further introduced, concerning the condition for starting oscillations, operation mode and output amplitude. Finally, the discussion focuses on the phase noise model and the noise mechanism in the cross-coupled VCO.

3.2.1. Property of LC Tank



(a) **(b)**

Figure 3.12 (a) Parallel LC resonator and (b) Equivalent LC resonator

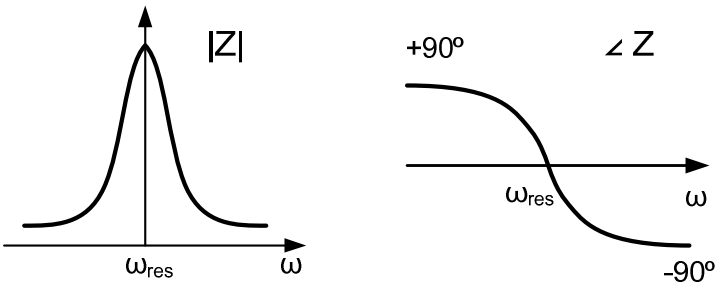
Figure 3.12 (a) describes a LC tank circuit employed in the RF oscillator. R_L and R_C are the series loss of the inductor L and capacitor C respectively. It could be proved that this network is equivalent to the network shown in Figure 3.12 (b), where L_p, C_p and R_p are the equivalent inductor, capacitor and loss of the whole LC tank respectively. The expression of L_p, C_p and R_p is given by

$$L_p = L \cdot \left(1 + \frac{1}{Q_L^2}\right) \tag{3.4}$$

$$C_p = C \cdot \left(1 + \frac{1}{Q_C^2}\right) \tag{3.5}$$

$$R_p = \left[R_L \cdot \left(1 + Q_L^2\right)\right] // \left[R_C \cdot \left(1 + Q_C^2\right)\right] \tag{3.6}$$

where the $Q_L = \omega L / R_L$ and $Q_C = 1/\omega C R_C$ are the Q-factor of L and C. If the Q_L and Q_C are larger then 3, then $L_p \approx L$, $C_p \approx C$.



(a) **(b)**

Figure 3.13 (a) Magnitude response and (b) phase response of the LC tank around the resonant frequency ω_{res}

The LC tank will be resonating at the frequency $\omega_o \approx 1/\sqrt{LC}$. Figure 3.13 describes the magnitude response and the phase response of the LC tank around the resonant frequency. At this frequency, the phase shift becomes zero and the magnitude reaches a peak, which is dominated by the equivalent resistance R_p. A large Q_L and Q_C results in a large equivalent resistance R_p, implying that less current is required to start oscillations. When the oscillation occurs, the Q-factor of the LC tank could be expressed by

$$\frac{1}{Q_{\tan k}} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{3.7}$$

Apparently, the value of Q_{tank} depends on Q_L and Q_C. An increase of Q_{tank} directly improves the phase noise performance of the oscillator. In reality, as for the LC tank

in the RF VCO, the capacitor C is made up of the varactor and the parasitic capacitance. Therefore, the Q-factor of the inductor and varactor are critical for low-power low-noise VCO design. The Q_L of a well-designed inductor at 3 GHz is between 5 and 10. As for the Q-factor of a varactor, it could be as high as 100 at 2 GHz. Hence, Q_L will dominate the Q_{tank}. However, Q_L rises with the frequency, and will be higher than Q_C when the frequency increases to the mm-wave frequency. The varactor becomes the main loss and noise source of the LC tank. In 90 nm CMOS technology, Q_L is normally larger than 20 at 40 GHz, while the Q-factor of varactor decreases to approximately 10. Furthermore, the output buffer and parasitic elements will definitely contribute losses to the oscilator, further degrading the Q-factor of the total tank.

3.2.2. Theory of Operation

Conditions for starting oscillations

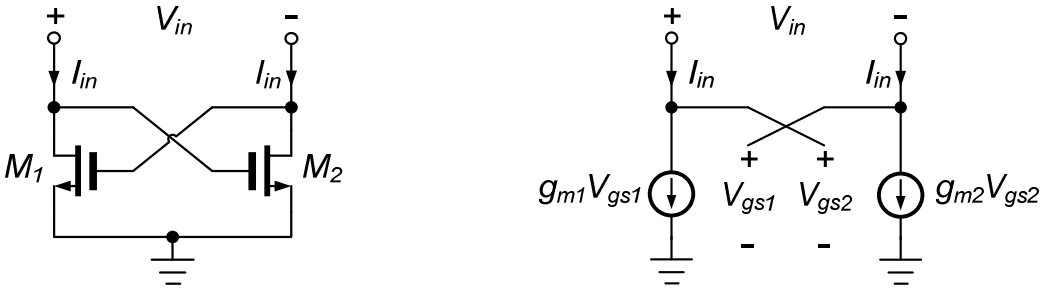


Figure 3.14 (a) Negative resistor cell and (b) simplified small-signal model

Firstly, let's evaluate the negative resistor generated by the cross-coupled pair. The negative resistor cell and its simplified small-signal model are displayed in Figure 3.14. The following equations could be constructed.

$$V_{in} = V_{gs2} - V_{gs1} \qquad I_{in} = g_{m1} V_{gs1} = -g_{m2} V_{gs2}$$

Then

$$V_{in} = V_{gs2} - V_{gs1} = -I_{in}\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right) \tag{3.8}$$

Typically $g_m = g_{m1} = g_{m2}$, the equivalent resistance at input port can be derived as

$$R_{in} = \frac{V_{in}}{I_{in}} = -\frac{2}{g_m} \tag{3.9}$$

The equation (3.9) gives the expression of the negative resistor from the cross-coupled pair. But this expression does not take the channel length modulation effect and parasitic elements into account. In the design, the absolute value of R_{in} is supposed to be as small as possible. Accordingly, a large negative conductance is achieved to start oscillations. Because of the parasitic elements, the absolute value of the negative resistor increases with operation frequency. Eventually the oscillator may fail to oscillate at mm-wave frequencies.

Based on the model of the one-port oscillator, oscillations start if $2R_p - 2/g_m > 0$. R_p is the equivalent parallel resistor of the LC tank in the half circuit, so the total equivalent resistor of the VCO LC tank is $2R_p$. Typically, a well-designed VCO must satisfy the following condition to ensure oscillation.

$$g_m \cdot R_p \geq \alpha \tag{3.10}$$

The value of α is usually chosen to be between 2 to 3, in order to counter PVT variations.

Operation mode and output amplitude

The voltage amplitude of the oscillating signal depends on the mode of operation. After the VCO starts oscillating, the voltage amplitude continues to increase. It will be suppressed by the nonlinearity of the oscillator and finally become stable. When the cross-coupled VCO, described in Figure 3.2, operates in the current-limited mode, the output amplitude grows with the increase of bias current I_{bias} until the VCO becomes voltage-limited. In the voltage-limited mode, the current I_{bias} is too large, so that the current source transistor operates in the triode region and the output amplitude is limited by the supply voltage.

When the VCO is current-limited, the cross-coupled transistors (M_1 and M_2) operate like switches, as long as the voltage amplitude is large enough. The single-ended voltage amplitude of the oscillating signal grows with the bias current, shown as

$$V_{amp} \approx \frac{2}{\pi} R_p I_{bias} \tag{3.11}$$

where I_{bias} corresponds to the bias current and R_p is the equivalent resistor of the LC tank in the half circuit. As can be seen in the following analysis of the phase noise model, phase noise improves with the increase of the carrier power. Thus, the phase noise could be reduced by increasing the bias current when the VCO operates in the current-limited mode. However, it is not case when the VCO goes into the voltage-limited mode. The best operation point is at the boundary of these two modes, in terms of phase noise performance.

3.2.3. Phase Noise Property

An ideal oscillator would generate a pure sine wave, whose spectrum assumes the shape of an impulse. However, the real oscillators have phase noise components, which spread a noise skirt around the carrier frequency. The phase noise model will be introduced briefly. It is helpful to understand how the phase noise is generated in the VCO. Consequently, some noise conversion mechanism will be investigated.

Phase noise model

Figure 3.15 represents the equivalent circuit for an ideal one-port oscillator. Suppose that the active circuit is noiseless. It only generates the negative resistor to compensate for the consumed energy in the LC tank circuit. R is the equivalent loss from the LC tank. It is the unique noise source in the ideal one-port oscillator. The spectral density of its current noise is known as

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4KT}{R} \tag{3.12}$$

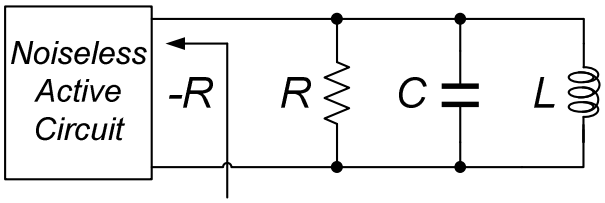


Figure 3.15 Ideal one-port oscillator

At the frequency offset $\Delta\omega$ with respect to the carrier frequency ω_o, the impedance of the LC tank is shown as [49]

$$Z\left|(\omega_o+\Delta\omega)\right| \approx \frac{R\omega_o}{2Q\cdot\Delta\omega} \tag{3.13}$$

The spectral density of the voltage noise at $\Delta\omega$ offset is further given as

$$\frac{\overline{v_n^2}}{\Delta f}=\frac{\overline{i_n^2}}{\Delta f}\cdot Z\left|(\omega_o+\Delta\omega)\right| \approx 4KTR\left(\frac{\omega_o}{2Q\cdot\Delta\omega}\right)^2 \tag{3.14}$$

According to the definition, phase noise refers to the ratio of single-sideband noise power in a unit bandwidth at offset $\Delta\omega$ over the carrier power, which is given in the dB form as

$$L\{\Delta\omega\}=10\log\left[\frac{\frac{1}{2}\cdot 4KTR\left(\frac{\omega_o}{2Q\cdot\Delta\omega}\right)^2}{\left(\frac{V_{amp}}{\sqrt{2}}\right)^2}\right]=10\log\left[\frac{2KT}{P_{carrier}}\left(\frac{\omega_o}{2Q\cdot\Delta\omega}\right)^2\right] \tag{3.15}$$

The $P_{carrier}$ represents the carrier power equal to $V_{amp}^2/2R$ and V_{amp} is the amplitude of the oscillating signal. This expression of phase noise gives us an intuitive feeling about the phase noise. The phase noise is proportional to $1/(\Delta\omega)^2$, making the single-sideband phase noise decrease by -20 dBc/dec. Meanwhile, increasing the carrier power and Q-factor of the LC tank could directly improve phase noise. Significantly, phase noise is inversely proportional to the square of the Q-factor.

Obviously, this expression is not accurate enough. Actually, there are many other noise sources in the VCO apart from the loss of the LC tank. Thus the phase

noise in the $1/(\Delta\omega)^2$ region is much larger than expected. On the other hand, concerning a real single-sideband phase noise spectrum, a $1/(\Delta\omega)^3$ region exists in the vicinity of the carrier, and phase noise becomes flat at a large frequency offset, as illustrated in Figure 3.16.

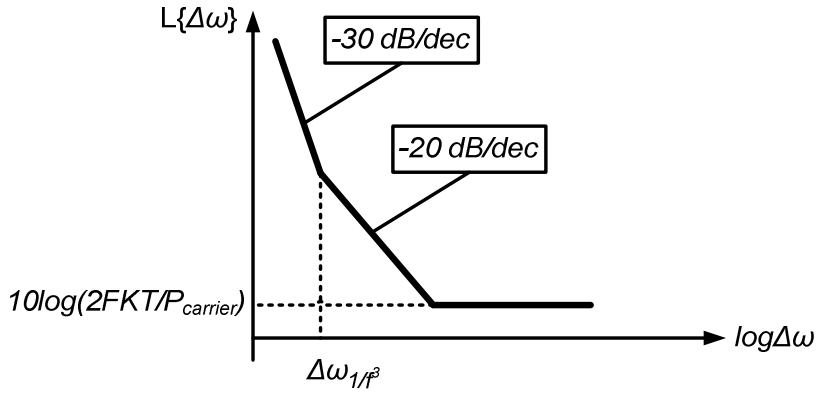


Figure 3.16 Leeon's model for real single-sideband phase noise

Based on the observation of a real phase noise, D.B.Leeon established an semi-empirical model in 1965 as [50]

$$L\{\Delta\omega\} = 10\log\left\{\frac{2FKT}{P_{carrier}}\cdot\left[1+\left(\frac{\omega_o}{2Q\cdot\Delta\omega}\right)^2\right]\cdot\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \tag{3.16}$$

where F is an empirical parameter, often called the "device excess noise number", k is Boltzmann's constant. T is the absolute temperature. The $\Delta\omega_{1/f}^3$ refers to the corner frequency between $1/(\Delta\omega)^3$ region and $1/(\Delta\omega)^2$ region. Compared with the expression resulting from an ideal one-port oscillator, three modifications are made in the Leeon's model. An empirical parameter F is added to model the noise contribution from the other noise sources. Secondly, an added factor of unity is given to fit the noise floor equal to $2FKT/P_{carrier}$. Additionally, the factor $\left(1+\Delta\omega_{1/f^3}/|\Delta\omega|\right)$ is employed to account for the $1/(\Delta\omega)^3$ region.

A number of research projects have been carried out to give the expression of *F*. Considering both the noise in the LC tank and the white noise from the cross-coupled pair, F is calculated as [51]

$$F \approx 1 + \gamma_{ccp} \tag{3.17}$$

γ_{ccp} is the channel thermal noise coefficient of the CMOS transistor. The white noise of two cross-coupled transistors is uncorrelated in this calculation. Furthermore, taking the white noise of the current source transistor into account, the expression F is [52]

$$F = 1 + \gamma_{ccp} + \frac{4}{9}\gamma_{bias} g_{mbias} R \tag{3.18}$$

where γ_{bias} is the channel thermal noise coefficient, while g_{mbias} corresponds to transconductance of the current source transistor. *R* is the equivalent impedance of the LC tank.

Leeon's model is based on the empirical modification of the ideal phase noise model. After that, the phase noise model of the VCO has continued to be a popular research topic [53][54][55][56]. However, most of the analysis is based on the assumption that the VCO is a linear time-invariant (LTI) system. Actually, any oscillator is a periodically time-varying system. A linear time-variant (LTV) phase noise model was eventually built by Hajimiri [57]. It is capable of analyzing the complete mechanism of phase noise generation.

Noise conversion mechanism

The foregoing analysis of the phase noise model gives a general understanding of the oscillator's phase noise. Focusing here on the cross-coupled VCO, its noise sources and noise conversion mechanism will be investigated. It is helpful to conduct the optimization of the VCO's phase noise performance.

Noise sources

In a cross-coupled VCO shown in Figure 3.2, basically there are four noise sources: resistor thermal noise of the LC tank, cross-coupled pair (M_1 and M_2) noise,

current source (M_3) noise and external noise. On the other hand, all the noises could be divided into two categories: white noise and 1/*f* noise. Noise from the LC tank is attributed into the white noise. The 1/*f* noise includes the 1/*f* noise of the cross-coupled pair (M_1 and M_2) and the current source transistor M_3's 1/*f* noise. In the meantime, the cross-coupled pair and current source transistor would also contribute white noises, which stem from channel current thermal noises. The external noise corresponds to the noise and disturbance from the supply voltage, substrate and control voltage.

The white noise from the LC tank and the cross-coupled pair at carrier frequency ω_o could modulate directly the zero crossing instants of the oscillating signal, contributing to the $1/(\Delta\omega)^2$ region of the phase noise spectrum. As for the other noise sources, the mechanism of phase noise generation is complicated and will be discussed in the following.

AM-PM conversion

The amplitude modulation (AM) noise exists in any topology of the VCO. The external noise and disturbance from the supply voltage, substrate and control line all produce AM noise through the LC tank. The influence of external noise to the phase noise is ignored in the previous analysis of the phase noise model. The AM-PM conversion in the VCO could transform the AM noise to the phase noise. The AM-PM conversion occurs because of the nonlinear operation of some devices in the VCO, such as varactors and cross-coupled transistors.

When the AM noise exists in the control voltage of the varactors, it would change their equivalent capacitance. Eventually it results in the variation of oscillation frequency, leading to the degradation of the phase noise. The effect of AM-PM conversion induced by the varactors could be characterized by a sensitivity parameter as [52]

$$K_{AM\text{-}FM} = \frac{\partial \omega}{\partial V}\Big|_{\omega=\omega_o} \approx \frac{\partial}{\partial V}\left(\frac{1}{\sqrt{LC_{\text{var}}}}\right) \tag{3.19}$$

It indicates the sensitivity of the oscillation frequency to the voltage disturbance. Clearly, the value of $K_{AM\text{-}FM}$ is related to the C-V curve of the varactor. Decreasing $K_{AM\text{-}FM}$ could be achieved by simply reducing the tuning ratio of the varactor and the tuning sensitivity of the VCO. But this conflicts with wide frequency tuning. The switched tuning technique [39] might be used to resolve this problem.

Another AM-PM conversion process comes from the nonlinear operation of the cross-coupled pair. As far as we know, the cross-coupled transistors are acting as switches since the oscillating signal has a large amplitude. It operates like a single-balanced mixer. If the AM noise modulates the operation point of the cross-coupled transistors, the high frequency harmonics would be modulated as well because of its mixing operation [52]. The modulated harmonics will change the phase shift of the LC tank, thereby generating phase noise [52]. To overcome this effect, the mixing operation and total harmonic distortion of the cross-coupled pair must be suppressed either by improving the linear region, namely V_{gs}-V_{th}, or by improving the cut-off frequency of the cross-coupled transistor. For the cross-coupled transistor, the expression of V_{gs}-V_{th} and the cut-off frequency are given as

$$V_{gs} - V_{th} = \sqrt{\frac{2I_{bias}L}{\mu C_{ox}W}} \propto \frac{1}{\sqrt{W}} \tag{3.20}$$

$$f_t = \frac{g_m}{C_{gs}} \approx \frac{\sqrt{2I_{bias}\mu C_{ox}\frac{W}{L}}}{\frac{2}{3}WL} \propto \frac{\sqrt{W}}{W} = \frac{1}{\sqrt{W}} \tag{3.21}$$

Apparently, they are both proportional to $1/\sqrt{W}$. In reality, the smallest process size is selected for the transistor length L. Providing the VCO could start oscillating, the finger width W of the cross-coupled transistor should be as small as possible in order to suppress the AM-PM conversion.

Noise conversions

As we know, under the condition of the large-signal nonlinear operation, M_1 and M_2 are switching on and off alternately. They operate like a single-balanced

mixer, which will commutate and up-convert the low-frequency 1/*f* noise in the cross-coupled pair and current source into two correlated AM sidebands around the carrier [52]. The 1/*f* noise at frequency $\Delta\omega$ is up-converted to frequency $\omega_o+\Delta\omega$ near the carrier. But it forms only the AM noise, not the phase noise. It will not affect the phase at the zero crossing instants [52]. But ultimately it will be transformed to the phase noise through the AM-PM conversion. Meanwhile, the white noise around the even harmonic frequency of the carrier is down-converted to the carrier frequency ω_o, contributing to the phase noise. The white noise of the cross-coupled pair at carrier frequency ω_o could modulate directly the zero crossing instants, creating phase noise.

Obviously, the noise conversion in the cross-coupled VCO is closely related the switching behavior of the cross-coupled pair. It behaves as a mixer which converts the noise at a different frequency to the phase noise around the carrier frequency. The linear operation of the cross-coupled pair is critical to suppress this mixing effect. On the other hand, it must be emphasized that only the white noise at even harmonic frequencies of the carrier creates phase noise [58]. The current source transistor only needs to provide a high impedance at the even harmonics frequency, to stop the cross-coupled transistors in the triode region loading the LC tank [58].

The bias current transistor is a great contributor to phase noise, especially phase noise in the $1/(\Delta\omega)^3$ region. High close-in phase noise is fatal for wireless applications with a narrow channel bandwidth. Generally, a quite large size is chosen for the current source transistor to reduce its 1/*f* noise.

3.3. Design Issues of Millimeter-wave Frequency Divider

3.3.1. Design Consideration

A high frequency 2:1 divider is a design challenge for mm-wave LO generation. A well-designed divider should provide correct divide-by-2 function in the whole band of interest, while consuming low power and contributing negligible noise. The locking range corresponds to the frequency range where the divider is functional with a specified input power. Generally, the locking range of the frequency

divider improves with the increase of the input power. The locking range with 0 dBm input power is usually compared between designs. The input sensitivity of a frequency divider is also of concern as well. It describes the change of the locking range when varying input power. As analyzed in chapter 2, the phase noise generated by the divider is a considerable contributor to the PLL's in-band phase noise. For an ideal divider chain with division ratio N, its output spectrum is supposed to be $20\log N$ lower than the input. Additionally, the power consumption is an important design criterion as well. The power dissipated by the first several stages 2:1 frequency dividers, which operate at the highest frequencies, has dominated the total power consumption of a mm-wave frequency synthesizer.

Typically, the locking range, input sensitivity, phase noise and power consumption are the four most significant specifications for the design of a 2:1 frequency divider. For the mm-wave application, the design of divide-by-2 circuits is confronted by great difficulties.

3.3.2. Topology of 2:1 Frequency Divider

For the high frequency application in the mm-wave band, there are typically three basic topologies of a divide-by-2 circuit: static divider, Miller divider and injection locked frequency divider.

Static divider

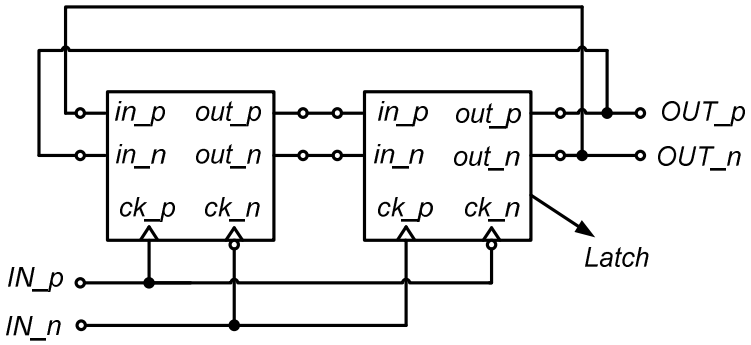


Figure 3.17 Static frequency divider

A simple approach to achieve divide-by-2 circuit is through an edge-triggered flipflop in a negative feedback loop, called 'static divider'. As illustrated in Figure 3.17, the static frequency divider is composed of two latches within an inverse feedback from the output of the second latch to the input of the first latch. Note that the two outputs of the two latches are actually quadrature. It gives the static divider another application for quadrature signal generation.

There are various topologies to implement the latch, such as clocked CMOS (C^2MOS) latch, True Single-Phase Clocked (TSPC) latch, and current mode logic (CML) latch. The C^2MOS implementation is typically applied to digital circuits. The TSPC latch achieves a good balance between the operating speed and the dissipated power. Built in 90 nm CMOS, it could operate in mixed signal mode up to GHz frequency. But its single-ended topology limits the scope of its applications. Also, its correct operation requires a tail-to-tail full-swing clock signal. The CML latch provides the highest operating speed, while consuming moderate power. This is preferable for the design of a high frequency divider. In addition, the differential topology is favored for superior suppression to common-mode noises. According to recently published literature, the CML-based static divider implemented with 90 nm CMOS technology is capable of operating above 30 GHz [59].

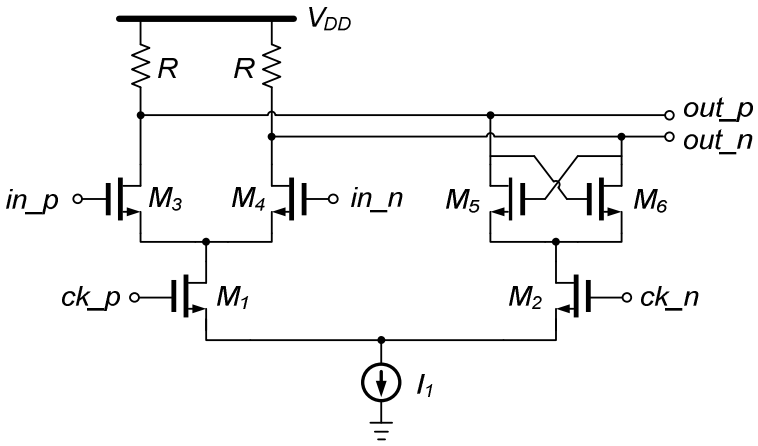


Figure 3.18 Conventional CML latch

Figure 3.18 shows the conventional architecture of a CML latch. At the rising edge of the clock signal, the tail current flows into the input differential pair. At the same time, the input data is sampled. When the clock is falling, the cross-coupled pair starts operating to hold the output level. Meanwhile, the information at the output goes into the next stage latch. In theory, the cross-coupled pair could hold the information forever. Thus the CML-based latch could be functional to a pretty low frequency, even DC. For the design of the conventional latch, three factors should be considered specifically: output amplitude, maximum operation frequency and voltage gain. When the latch is driven by a full-swing clock signal, M_1 and M_2 would experience the complete switching, providing a gain of $2/\pi$. The amplitude of the output signal is shown as [60]

$$V_{amp} \approx \frac{2}{\pi} \cdot I_1 \cdot R \tag{3.22}$$

On the other hand, the operation speed of the CML latch is limited by the RC load at the output terminal. The maximum operation frequency of the latch is derived by

$$f_{max} \leq \frac{1}{a \cdot R \cdot C_p} \tag{3.23}$$

where the C_p is the total parasitic capacitance at the output terminal. The parameter '*a*' is a parameter larger than unity, implying that the practical maximum operation frequency is actually lower than the cut-off frequency of the RC load at the output terminal. In reality, it is better to select the value of '*a*' larger than two, ensuring that the latch is functional in the whole band of interest [60]. A series combination of inductor and resistor could be employed as the load to improve the operation frequency [59][61]. In addition, when the static divider operates at high frequencies, the assumption does not hold that output characteristics only depend on the RC time constant at the output terminal. The rising and falling time of the output signal also rely on the voltage gain of input differential pair (M_3 and M_4), which is given by

$$A_{v\text{-}in} \approx g_{m3,4} R \tag{3.24}$$

$A_{v\text{-}in}$ must be larger than unity [60]. Similarly, the loop gain of positive feedback built by the cross-coupled pair (M_5, M_6) and load R should also exceed unity.

When the operation frequency increases, the operation mode of the static divider might change. It would operate in a self-oscillation condition. It acts like a two-stage ring oscillator with a negative feedback. The divide-by-2 function is actually achieved through an injection locking mechanism. Under this circumstance, the operation frequency depends on its self-oscillation frequency. Using 65 nm SOI CMOS, a CML-based static divider operating at 94 GHz has been reported [62]. In the meantime, the static divider is no long capable of operating at an arbitrary low frequency. A design of such a static divider in self-oscillation mode will be demonstrated in chapter 5.

Miller divider

First proposed by Miller in 1939, the Miller divider mixes the input with the feedback signal and applies the result to a low-pass filter (LPF), described in Figure 3.19. It is also known as the regenerative divider.

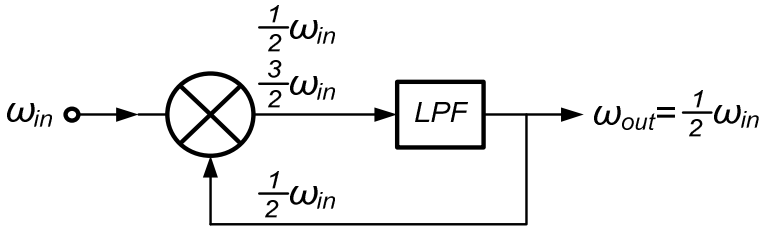


Figure 3.19 Model of the Miller divider

It is stated that the correct operation of the Miller divider requires the appropriate phase shift around loop or enough suppression to the third harmonics of input signal [63]. Meanwhile, the loop gain at $1/2\ \omega_{in}$ must be at least unity.

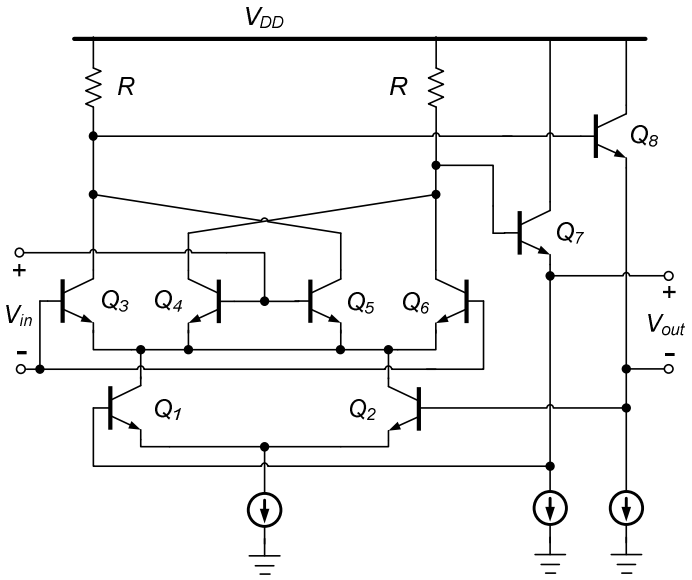


Figure 3.20 Bipolar Miller divider

A realization of the bipolar Miller divider is shown in Figure 3.20 [63]. The Mixer in Figure 3.19 is achieved as a double-balanced Gilbert cell Mixer. The resistor *R* and the parasitic capacitance together comprise a LPF load. The output emitter follower (Q_7 and Q_8) provides enough phase shift in the loop to ensure the correct operation.

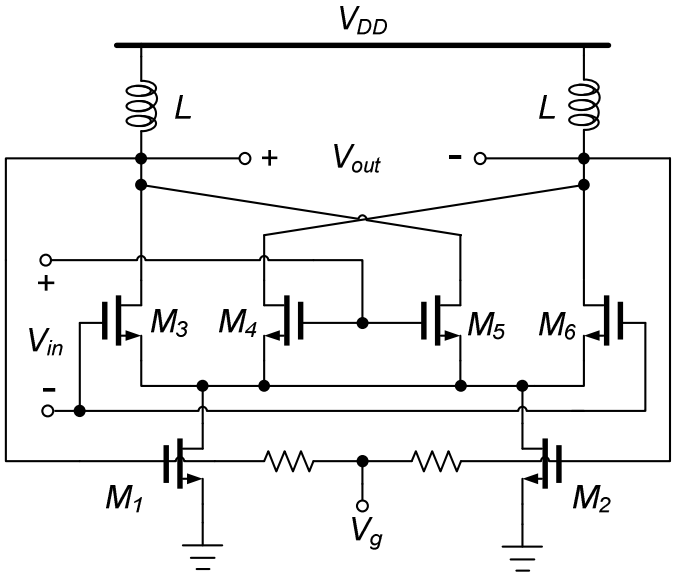


Figure 3.21 CMOS Miller divider

However, the architecture in Figure 3.20 is difficult to achieve using CMOS technology, because of the poor performance of the CMOS source follower. It would reduce the loop gain and prevent the circuit from operating at high frequencies [63]. The CMOS Miller divider has a slightly different architecture [63]. As shown in Figure 3.21, the inductor L replaces the resistor to build a band-pass filter (BPF) load instead of the LPF in the bipolar counterpart. Unlike the bipolar Miller divider, the CMOS realization achieves the divide-by-2 function by suppressing the third harmonics. Choosing the appropriate frequency range of the BPF, the signal at $3/2\ \omega_{in}$ frequency could be sufficiently attenuated while the desired $1/2\ \omega_{in}$ signal is kept as the output. The output signal is fed back to the RF port of the double-balanced Mixer. For this topology, its locking range is derived as [63]

$$\Delta\omega \approx \frac{\omega_c}{Q}\left(\frac{2}{\pi} g_m R\right)^2 \tag{3.25}$$

where ω_c is the corner frequency of the BPF load. It is equal to $1/\sqrt{LC}$ and C represents the equivalent capacitance. Q and R are the Q-factor and the equivalent parallel resistor of the load. g_m corresponds to the transconductance of transistors M_1, M_2. Typically, $2\omega_c$ is designed in the middle of the desired input frequency range to cover the whole band of interest. The load with a low Q-factor results in a larger locking range. This is not surprising because a lower Q-factor implies a relatively wider pass band of the BPF, and then a larger operation range. The part $(2/\pi)\cdot g_m R$ on the right side of the equation (4.4) actually corresponds to the loop gain, which indicates that a higher loop gain contributes to a larger locking range.

Injection locked frequency divider

The injection locked frequency divider (ILFD) is operating based on the locking phenomenon of the oscillator. Suppose that a well-behaved oscillator is free running at frequency ω_o. If an external signal at frequency ω_{inj} is injected into the oscillator core with a proper phase and amplitude, the oscillator might be locked to any harmonic frequency of ω_{inj}, rather than ω_o. One of the key factors for the locking

phenomenon is that a phase difference must exist between the injected signal and the internal signal, so that the total phase shift of the loop remains 0º at the new oscillation frequency [64].

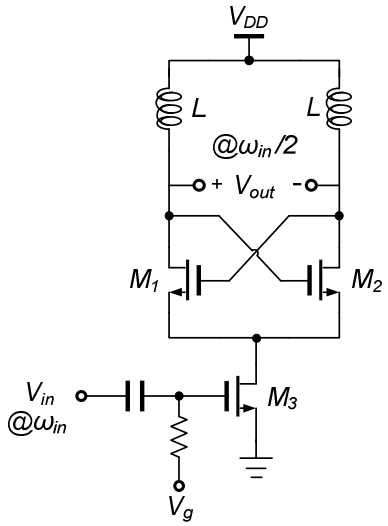


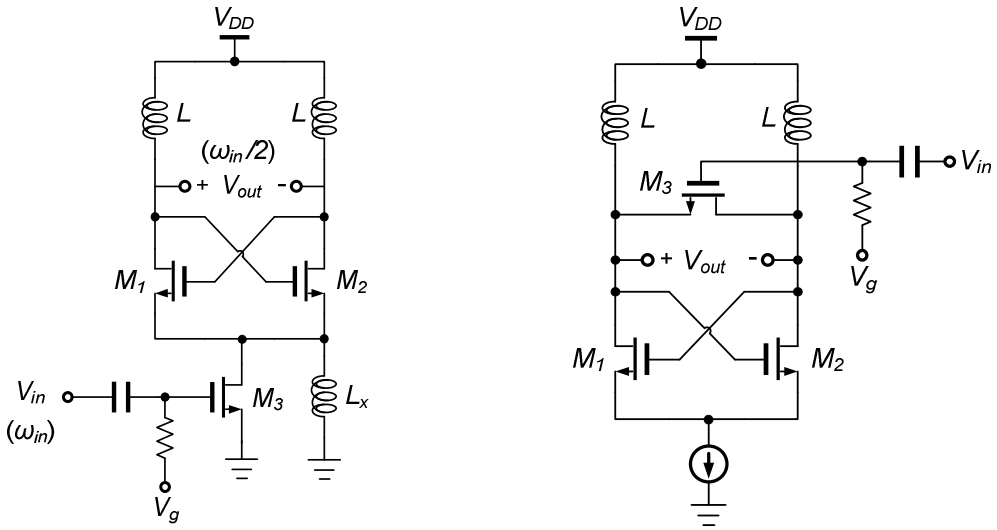
Figure 3.22 Conventional injection locked frequency divider

Figure 3.22 is a conventional implementation of such idea. The cross-coupled oscillator is oscillating close to $\omega_{in}/2$ frequency. The input signal is injected into the oscillator through the tail current transistor M_3, the oscillator could locked at exactly $\omega_{in}/2$. Because of its simple topology, the ILFD could operate at very high frequencies, even above 100 GHz. Meanwhile, its power consumption is pretty low. The only shortcoming is the limited locking range. It has been concluded that the normalized locking range of the ILFD is given by [64]

$$\frac{\Delta\omega}{\omega_o} \approx \frac{1}{Q} \cdot \frac{I_{inj}}{I_{osc}} \tag{3.26}$$

where I_{inj} and I_{osc} are the injected current and the oscillator current respectively. Apparently, the locking range could be improved by increasing the injected current. Furthermore, the Q-factor of the tank could be artificially decreased, as long as the oscillation is guaranteed.

As for the topology in Figure 3.22, it is actually difficult to increase the injected current. A large size of M_3 might be required to raise the I_{inj}. However, the size of M_3 is limited since it provides the dc current of the oscillator. On the other hand, considerable parasitic capacitance at the drain of M_3 would attenuate the injected signal significantly. To resolve this problem, an inductor could be employed to construct the shunt-peaking [65], as illustrated in Figure 3.23 (a). As a result, the inductor resonates with the parasitic capacitance at the frequency of the input signal. The injected current will see an impedance peak at the drain of M_3, leading to the increase of the injected power. But the injection of the input signal through M_3 is not an efficient injection path after all. The injected current eventually has to flow into the oscillator core over the cross-coupled pair M_1 and M_2.



(a) **(b)**

Figure 3.23 (a) ILFD with shunt-peaking, (b) Direct ILFD

A preferable approach is to inject the signal directly into the oscillator core [66]. Figure 3.23 (b) shows the simplified schematic of this design. The bias circuit is not included here. Consequently, the output signal is directly locked by the injected input signal. The injection efficiency of the input signal is greatly enhanced. Compared with the static divider and the Miller divider, the ILFD is superior because of its higher operation frequency and low power consumption. Its simple topology is

also an advantage. The narrow locking range is the most serious design issue. Therefore, ILFD has always been a hot research topic in recent years concerning the locking range enhancement.

3.3.3. Topology Comparison

Here we make a simple comparison of these three topologies.

As discussed above, the operation of a high frequency static divider could be designed as a two-stage ring oscillator. It presents the injection locking property at high frequencies like the ILFD. Based on this property, the static divider is capable of realizing frequency division in the W-band [62]. In principle, the locking of the oscillator most easily occurs when the input frequency is near the oscillation frequency. That is to say, the closer the input frequency is to the oscillation frequency, the less input power is required for the locking. Therefore, as for the high frequency static divider and ILFD, their locking range is sensitive to various input power, as described in Figure 3.24.

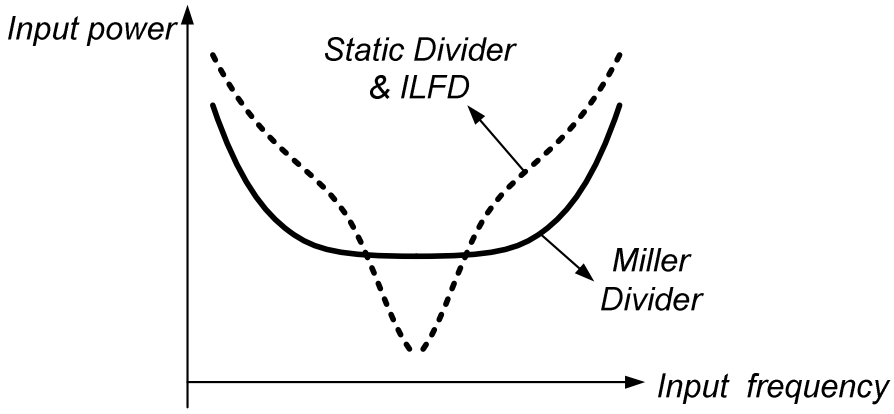


Figure 3.24 Input sensitivity of different frequency dividers

But for the Miller divider, the situation is slightly different. Recall that the loop gain of the Miller divider is required to be in excess of unity at frequency $\omega_{in}/2$. The required minimum amplitude of the input signal could be derived as [63]

$$A \geq \frac{2}{\beta}\sqrt{1+\left(\frac{\omega_{in}}{2\omega_c}\right)^2} \geq \frac{2}{\beta} \tag{3.27}$$

where β is the gain of the double-balanced Mixer of the Miller divider. ω_c is the corner frequency of the BPF load. Thus, the Miller divider shows a relatively flat input sensitivity with respect to the input power, as shown by the solid curve in Figure 3.24.

Beside the static divider, the Miller divider has also a strong link to the ILFD. Figure 3.21 shows a topology of the Miller divider with the feedback to the RF port of the double-balanced Mixer. Another possible realization is through the feedback to the LO port of the double-balanced Mixer, like the topology in Figure 3.25.

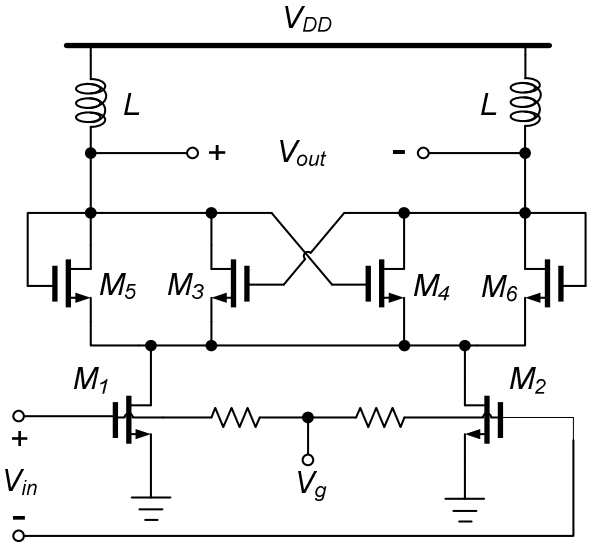


Figure 3.25 Miller divider with the feedback to LO port

This topology actually resembles the ILFD, but with a differential input stage (M_1 and M_2). The M_3 and M_4 are connected cross-coupled like the ILFD. The two diode-connected transistors M_5, M_6 actually provide two resistors to the load. They reduce the total *Q*-factor of the load, resulting in a locking range improvement. Compared with the conventional ILFD in Figure 3.22, it has two injection paths of the

input signal as well as a relatively low Q-factor load. Thus, theoretically it is capable of achieving a larger locking range, but the price for this is dissipating more power.

However, the input signal is actually injected through the tail current transistor to the common-mode in the topology of Figure 3.25. As analyzed above, it is not an efficient injection path. The injected signal is attenuated by the parasitic capacitance at the common-mode point. The Miller divider may achieve a larger locking range, but the additional power consumption fails to play a full role in the locking range enhancement. It is essentially an inefficient topology.

Chapter 4.
Design of 40 GHz VCO

In chapter 3, design issues of the mm-wave VCO were discussed. With CMOS technology, the design of the mm-wave VCO for a large tuning range and good noise performance is a challenging task. This chapter presents a complete design of a 40 GHz VCO with 90 nm CMOS technology. On-chip inductors are designed first because of their great significance for VCO design. A topology of a resonated negative-conductance cell is proposed to alleviate the difficulties in the mm-wave VCO design. According to measurement results, it achieves an excellent balance between all critical performances, resulting in a figure-of-merit of -185.4 dBc/Hz.

4.1. On-chip Inductors Design for mm-wave Application

Passive devices such as the inductor are critical for the VCO's design. For the RF integrated circuit design, the on-chip inductor usually has a low *Q*-factor and occupies a large area. As frequency grows to the mm-wave band, the on-chip inductor becomes quite small in size, meanwhile presenting a much higher *Q*-factor. For instance, the *Q*-factor of a 100 pH inductor could be higher than 25 at 60 GHz. Therefore, they are employed extensively in mm-wave circuit design.

Since the spiral inductor is integrated to the SI process, its equivalent circuit model has always been a popular research topic. The conventional equivalent-circuit models the inductor using a lumped single-π circuit [67][68][69]. The single-π model has apparent disadvantages. It employs frequency-independent elements which is incompatible with the transient simulation and broadband design. Meanwhile, it lacks a distributed characteristic to match the high frequency behavior. Later, some double-π equivalent circuits are created [70][71], which is considered to be a better solution. The model of the on-chip inductor will not be discussed in this chapter. The discussion in this section is applied to some design issues for mm-wave applications.

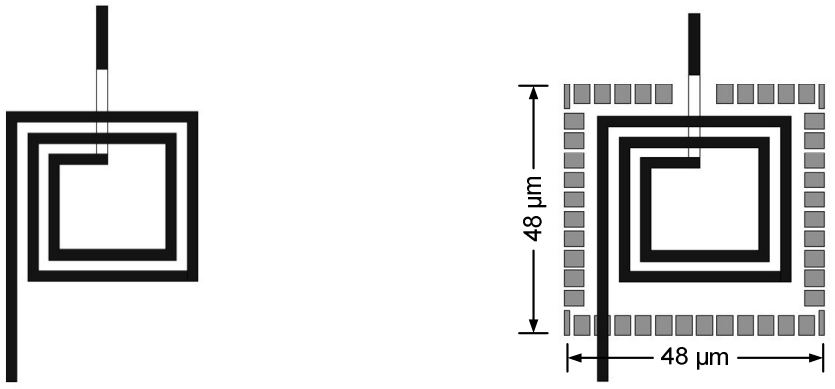
4.1.1. Spiral Inductor

Generally, the *Q*-factor of an inductor is of great importance, especially for VCO design. The design of inductors for the radio frequency range emphasized the use of wide metal wires to reduce the series resistance of the inductor. As the *Q*-factor of an inductor increases with frequency, it is not the main concern for inductor design in the mm-wave band. The *Q*-factor of an inductor does not depend on resistance loss of metal wires, but is dominated by the loss from the substrate. On the other hand, the mm-wave application demands a high self-oscillation frequency (SRF) of an inductor to ensure the correct behavior in the band of interest. Therefore, design considerations should be given to diminishing the coupling to substrate, in order to reduce loss and increase the SRF. For this result, the square spiral inductor with a minimum wire space would be a favorable topology for the mm-wave application. It is capable of attaining the largest possible inductance with the smallest area. It implies the reduced coupling and loss from the substrate, consequently leading to the increase of SRF.

A library of square inductors is designed in TSMC 90 nm CMOS technology with the assistance of Ansoft HFSS. To reduce the series resistance of the inductor, the top metal layer is used for the inductor design. It is an ultra-thick metal layer, which is 3.4 μm thick. All spiral inductors share a similar topology, as shown in Figure 4.1 (a). They are designed with the minimum wire space, in order to achieve a small area. Employing different radius, square spiral inductors with 1-3 turns are capable of providing inductance between 80 pH and 350 pH. This inductance value satisfies most of the circuit design from 20 GHz to 60 GHz. On the other hand, these inductors can be achieved in an area smaller than 40 μm × 40 μm. Such a small area implies little coupling to the substrate.

For today's sub-micron CMOS technologies, metal dummy fills are required to insert on every metal layer to ensure uniformity of the metal density. However, as the frequency becomes high, eddy currents in the dummy fills create losses in the nearby metal wire, consequently decreasing the *Q*-factor. Furthermore, it also increases the coupling capacitor, resulting in a smaller SRF. The existence of dummy fills brings great challenges to the inductor design for mm-wave application. In the

TSMC 90 nm CMOS technology, the metal density of metal 1 to metal 7 must be higher than 15%, while the metal density of metal 8 needs to be higher than 20%. The metal density is checked in every 50 μm × 50 μm area in the layout design. Recall that the most designed square inductors for mm-wave application have an area smaller than 40 μm × 40 μm. As shown in Figure 4.1 (b), a patterned placement of dummy metal fills is created to satisfy the specified metal density in the 50 μm × 50 μm area of the square inductor. In other words, with the patterned dummy fills, the density of the metal 1 to metal 7 reaches 15%, while the density of metal 8 becomes 20% in the 50 μm × 50 μm area covering the spiral inductor. To make sure that the metal density is completely satisfactory, the size of the whole patterned dummy fills is designed to be slightly smaller than the check window, at 48 μm × 48 μm. With this configuration, if some area still has metal density problems, additional dummy fills could be placed close to the patterned dummy fills, with 1 μm space. As a result, the specific metal density in the desired 50 μm × 50 μm area will be completely satisfied.



(a) **(b)**

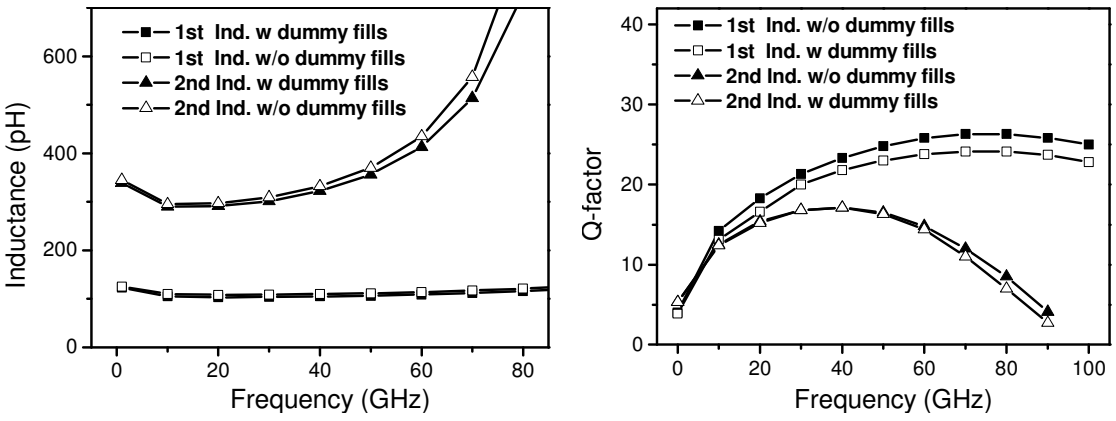
Figure 4.1 (a) Spiral inductor, (b) Spiral inductor with patterned dummy fills

Since the patterned dummy fills are completely outside the inductor wires, they offer little influence to the inner inductor wires. In the case of a small inductor, the distance between the outer wire and dummy fills is large. Then the influences from the dummy fills could be negligible. In Figure 4.2, the inductance and the *Q*-

factor of two designed spiral inductors are plotted. The results of two cases, with and without dummy fills, are compared. The data is extracted from the one-port s-parameter simulated by Ansoft HFSS. Thanks to this patterned placement, the influence from the dummy fills is very small. The change in the inductance caused by dummy fills can be negligible. The influence on the *Q*-factor is also limited, and the degradation of the *Q*-factor is acceptable.

Table 4.1 Design parameters of two spiral inductors

	Turn	Inner Radius	Width	Space
1st spiral Ind.	1	9 μm	3 μm	2 μm
2nd spiral Ind.	3	10 μm	2 μm	2 μm



(a) **(b)**

Figure 4.2 Simulated (a) inductance and (b) *Q*-factor of two spiral inductors

4.1.2. Symmetric Inductor

The above implementations of spiral inductors achieve the largest possible inductance with the smallest area. As a result, little coupling to substrate and a high SRF are attained. Nevertheless, due to skin effect, square spiral inductors with the minimum wire width might suffer from high resistance loss in the mm-wave band. Their *Q*-factor is not sufficiently high in some cases, for instance, the tank inductor of the VCO. The *Q*-factor of the tank inductor is quite critical for the VCO's phase noise

performance. From the previous analysis of the phase noise model, we can see that the phase noise is inversely proportional to the square of tank's Q-factor. Taking the differential property into account, the symmetric inductor is obviously a better choice for the VCO design. When the symmetric inductor is used in the differential circuits, it is capable of providing more inductance because of mutual coupling. That is to say, the symmetric inductor covers a smaller area for a specific inductance. Meantime, wide metal wires could be designed to reduce the resistance loss. Therefore, the symmetric inductor has the potential to provide a much higher Q-factor than the spiral inductor at high frequencies. However, the symmetric inductor used for the differential circuit usually needs an area larger than 50 μm × 50 μm. The patterned dummy fills proposed above as Figure 4.1 (b) could not be used for a symmetric inductor. To satisfy specific metal density, dummy fills must be placed inside the inductor wire, or even under the metal wire. This would lead to the decrease of the Q-factor.

In a test tape-out, two symmetric inductors were designed for performance evaluation [72]. Figure 4.3 shows the micrograph. Their small-signal S-parameter was measured through on-wafer probing. The S-parameter of the RF feeding structure is extracted and de-embeded from the results [73].

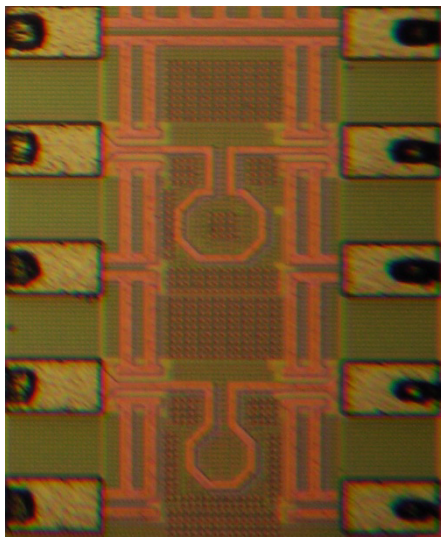
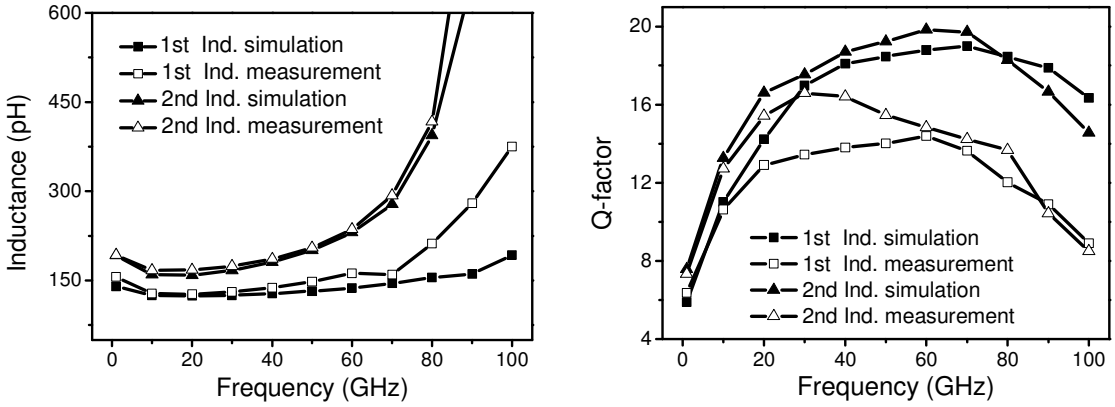


Figure 4.3 Micrograph of symmetric inductors



(a) **(b)**

Figure 4.4 Measured (a) inductance and (b) *Q*-factor of two symmetric inductors with evenly distributed dummy fills

The square-shaped dummy fills were evenly placed under the symmetric inductor. They have 3 μm × 3 μm size and 1 μm space. The inductance and *Q*-factor of these two inductors are extracted from the measured s-parameter and plotted in Figure 4.4. Apparently, the evenly distributed dummy fills cause great degradation of the *Q*-factor. Also, the SRF is decreased noticeably. It has been proved that the closer the dummy fills are to the inductor wire, the larger influence would be induced to the SRF and *Q*-factor of the inductor [74][75]. One approach to reduce the effect of dummy fills is to increase their metal density and place them in the center of the symmetric inductor. In this way, the dummy fills might be distant from the inductor wire. Consequently, the effect from the eddy current of the dummy fills is diminished.

As shown in Figure 4.5 (b), a patterned topology of dummy fills is used to increase their metal density, similar to the desgn in Ref [76]. Suppose that the width and space of the square-shaped dummy fills in Figure 4.5 (a) are w and s respectively. Then the metal density of evenly distributed dummy fills is given by

$$MD_{square} = \left(\frac{w}{w+s} \right)^2 \times 100\% \tag{4.1}$$

If w and s respectively are equal to 3 μm and 1 μm as our design, 56% metal density is achieved. As for the proposed topology in Figure 4.5 (b), metal density is

$$MD_{patterned} = \frac{w}{w+s} \times 100\% \tag{4.2}$$

Choosing the same value for w and s, the achieved metal density could reach 75%. Eventually, for the metal density demanded, the dummy fills could be placed in the center of the symmetric inductor. The dummy fills are distant from the inductor wire, preventing the great decrease of the *Q*-factor.

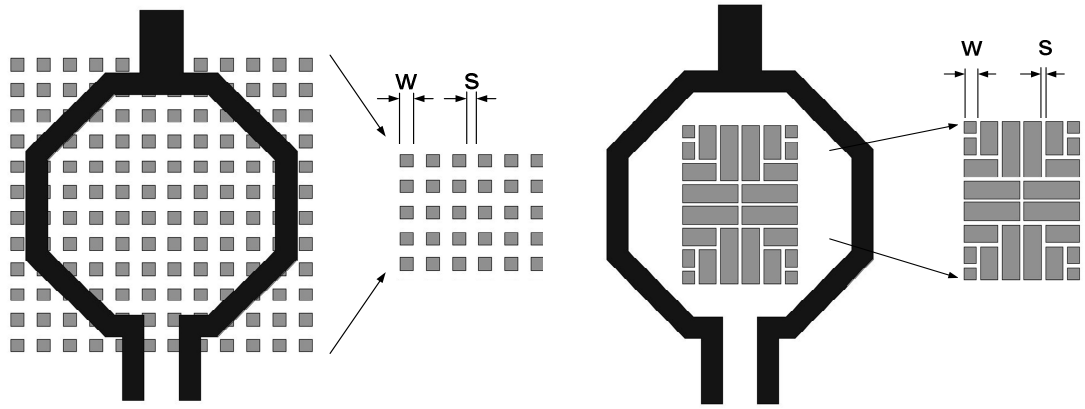
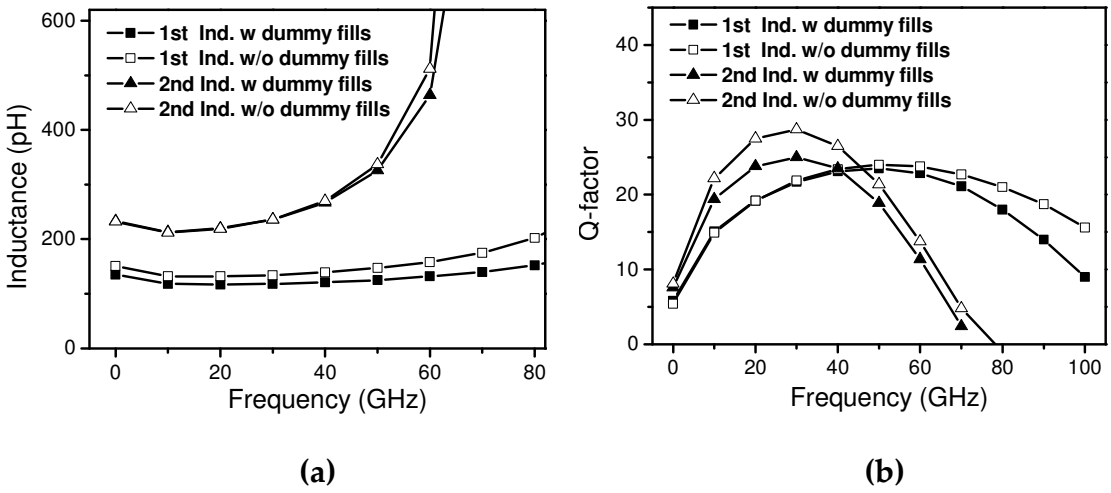


Figure 4.5 Symmetric inductor with (a) evenly distributed dummy fills and (b) patterned dummy fills

Through the EM simulation by Ansoft HFSS, the influence from this dummy pattern is evaluated. Two one-turn symmetric inductors are designed. Their design parameters are listed in Table 4.2. The width w and space s are 4 μm and 1 μm for the patterned dummy fills. The metal density of these dummy fills reaches 80%. As shown in Figure 4.6, with the proposed dummy fills pattern, the decrease of the *Q*-factor is much less than the case with evenly distributed dummy fills.

Table 4.2 Design parameters of two symmetric inductors

	Type	Turn	Radiu	Width
1st symmetric Ind.	Symmetric	1	32 μm	5 μm
2nd symmetric Ind.	Symmetric	1	50 μm	8 μm



(a) **(b)**

Figure 4.6 Simulated (a) inductance and (b) *Q*-factor of two symmetric inductors with patterned dummy fills

4.2. Design Challenges of Cross-coupled VCO for mm-wave Application

Figure 4.7 (a) describes the classic topology of a cross-coupled VCO. The equivalent half circuit is given in Figure 4.7 (b). The cross-coupled pair operates as a negative-conductance cell (N-cell) to compensate dissipated energy in the LC tank. This N-cell is equivalent to a negative conductance $-G_N$ with a parallel parasitic capacitance C_N. The tunable LC tank, which is composed of an inductor and a varactor, could be replaced by a parallel combination of an ideal inductor L_t, a tunable capacitor C_t and a conductance G_t.

Basically, the design of the cross-coupled VCO for the mm-wave band encounters three major challenges. The first challenge stems from some process-related issues. Distinct from the RF VCO, the *Q*-factor of the varactor would be

inferior to the inductor's *Q*-factor in the mm-wave band, at the same time dominates the total *Q*-factor of the LC tank. The *Q*-factor of the MOS varactor will be under 10 at around 60 GHz. Meanwhile, the parasitic capacitance also presents a low *Q*-factor. These capacitance elements in the VCO have become the main source of losses and phase noise. In addition, VCO design in the mm-wave band is pretty sensitive to the parasitic elements and loading effects. Considering a 60 GHz VCO, 30 fF parasitic capacitances would result in nearly a 10% shift of oscillation frequency. Overloading from the VCO's output buffer would greatly degrade the performance, even stop the VCO oscillating.

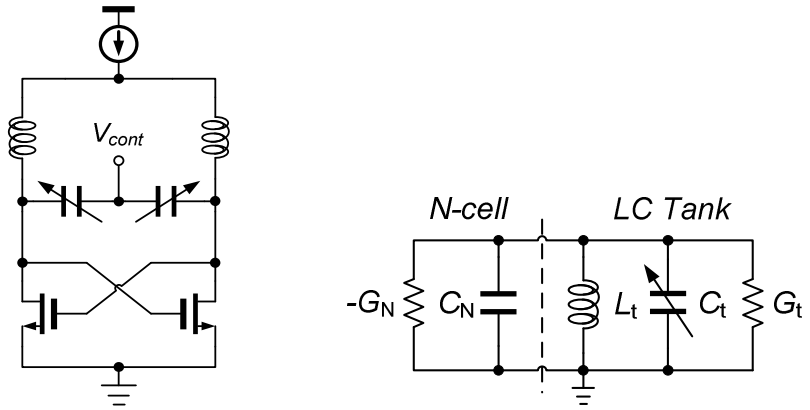


Figure 4.7 (a) Conventional cross-coupled VCO (b) equivalent half circuit

The second challenge is related to the tuning range. Based on the equivalent circuit in Figure 4.7 (b), the tuning range of the VCO depends on the following ratio η

$$\eta = \frac{C_{t,\max} - C_{t,\min}}{C_N + \dfrac{C_{t,\max} + C_{t,\min}}{2}} = \frac{2\left(\dfrac{C_{t,\max} - C_{t,\min}}{C_{t,\max} + C_{t,\min}}\right)}{2\left(\dfrac{C_N}{C_{t,\max} + C_{t,\min}}\right) + 1} = \frac{2\alpha}{2\beta + 1} \tag{4.3}$$

$$\alpha = \frac{C_{t,\max} - C_{t,\min}}{C_{t,\max} + C_{t,\min}}, \qquad \beta = \frac{C_N}{C_{t,\max} + C_{t,\min}}$$

where the $C_{t,max}$ and $C_{t,min}$ respectively correspond to the maximum and minimum values of the varactor. C_N is the parasitic capacitance of the VCO, mainly from the cross-coupled pair and output buffer. Accordingly, the parameter α represents the varactor's tuning ratio, while β is actually the ratio of the parasitic capacitance over the varactor capacitance. VCO's tuning range could be improved by either increasing α or decreasing β. The design of α is confronted with an inherent physical trade-off between the tuning ratio and the Q-factor. That is to say, increasing α will result in the degradation of the varactor's Q-factor. The Q-factor of the total tank consequently will be deteriorated, as well as the phase noise. β might be decreased by reducing the size of either cross-coupled transistors or output buffers. Cross-coupled transistors with a small size may not start oscillating. A small output buffer leads to inadequate output power. An additional amplifier stage may be needed.

The third challenge is the serious AM-PM convention in the mm-wave cross-coupled VCO. In the previous analysis, the AM-PM convention is essentially caused by the nonlinear operation of the varactor and cross-coupled transistors. When a large varator is employed for a wide tuning range, its low Q-factor and high non-linearity would make the VCO quite sensitive to AM noises. Considering the 60 GHz application for IEEE802.15.3c, a VCO with a 9 GHz tuning range is required. With 1.2 V supply voltage, the tuning sensitivity of the VCO is as high as 7.5 GHz/V. As for the cross-coupled transistors, they operate close to the intrinsic frequency f_t and f_{max}. When a large size is required to satisfy oscillation conditions, cross-coupled transistors may have a very limited linear region. Thus, the mm-wave VCO suffers from extreme sensitivity to AM noises, such as flicker noises in the current source and external noises from the supply voltage. This effect will also make phase noise measurement pretty difficult.

Therefore, CMOS VCO design in the mm-wave band is confronted by serious trade-offs between tuning range, phase noise, and oscillation start-up. Suppose that a large tuning range is specifically required, which is true for most high speed communication applications. Then a varactor with a large size is needed, whose low Q-factor will in turn degrade the Q-factor of the whole tank significantly and makes the oscillation start-up more difficult. Furthermore, its high C/V ratio makes the VCO

sensitive to AM noises, external noises and disturbances. It is definitely a disaster for mm-wave VCO design. In the meantime, parasitic capacitance generated by cross-coupled transistors would further reduce tuning range and degrade phase noise.

4.3. Resonated Negative-conductance Cell

Since the *Q*-factor of the on-chip inductor is improved considerably in the mm-wave band, the mm-wave VCO design briefly concerns the optimization of the varactor and active devices. In this work, a reconfigured topology of a resonated negative-conductance cell is proposed to relieve the design trade-off. Firstly, let's look into the *Q*-factor of the LC Network.

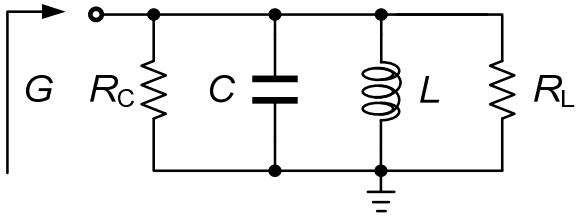


Figure 4.8 LC parallel network

Figure 4.8 displays a LC parallel network. R_L and R_C correspond to the equivalent parallel loss of the inductor and capacitor respectively. The *Q*-factor of the inductor and capacitor is equal to

$$Q_L = \frac{R_L}{\omega L} \qquad Q_C = \omega C R_C \tag{4.4}$$

The equivalent conductance and *Q*-factor of the network is given by

$$Y = G + jB = \frac{1}{R_L} + \frac{1}{R_C} + j\left(\omega C - \frac{1}{\omega L}\right) \tag{4.5}$$

$$Q_T = \left| \frac{\omega C - \frac{1}{\omega L}}{\frac{1}{R_L} + \frac{1}{R_C}} \right| \tag{4.6}$$

Clearly, when $\omega < 1/\sqrt{LC}$, then $B < 0$, the total network is inductive. It is essentially a parallel combination of a conductance and an inductor. The relation of Q_T and Q_C is investigated by

$$Q_T - Q_C = \frac{\frac{1}{\omega L} - \omega C}{\frac{1}{R_L} + \frac{1}{R_C}} - \omega C R_C = \frac{\frac{C}{L} R_C^2 R_L - \omega^2 C^2 R_C^2 R_L - R_C - R_L}{\omega C R_C (R_C + R_L)} \tag{4.7}$$

Further concluding that

$$\text{When } \omega < \sqrt{\frac{1}{LC} - \frac{1}{C^2 R_C R_T}} \ (R_T = \frac{R_C R_L}{R_C + R_L}), \quad Q_T > Q_C$$

R_T corresponds to the equivalent parallel resistor of the network. In other words, paralleling an inductor with a capacitor, the total Q-factor could be improved at low frequencies. But unfortunately, the network no longer acts as a capacitor, but as an inductor. On the contrary, when $\omega > 1/\sqrt{LC}$, then $B > 0$, the total network is capacitive. It follows that

$$Q_T - Q_C = \frac{\omega C - \frac{1}{\omega L}}{\frac{1}{R_L} + \frac{1}{R_C}} - \omega C R_C = \frac{\omega^2 C^2 R_C^2 R_L - \frac{C}{L} R_C^2 R_L - R_C - R_L}{\omega C R_C (R_C + R_L)} \tag{4.8}$$

$$\text{When } \omega > \sqrt{\frac{1}{LC} + \frac{1}{C^2 R_C R_T}} \ (R_T = \frac{R_C R_L}{R_C + R_L}), \quad Q_T > Q_C$$

That is to say, the parallel inductor is capable of improving the Q-factor of the capacitor at the frequency range higher than $\sqrt{1/LC + 1/C^2 R_C R_T}$. In the meantime, the total network still maintains the capacitive characteristic. In brief, paralleling an inductor with a capacitor and carefully selecting the resonant frequency of the LC parallel network, the Q-factor of the capacitor could be increased in the frequency range of interest.

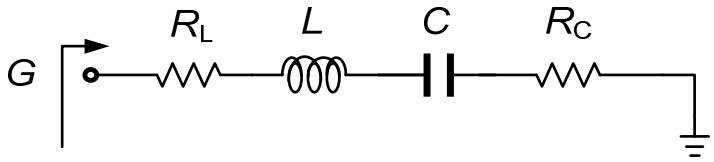


Figure 4.9 LC series network

The situation changes with the LC series network, described in Figure 4.9. Its equivalent conductance and *Q*-factor is expressed as

$$Y = G + jB = \frac{R_L + R_C}{(R_L + R_C)^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} + j\frac{\left(\frac{1}{\omega C} - \omega L\right)}{(R_L + R_C)^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} \tag{4.9}$$

$$Q_T = \left|\frac{\frac{1}{\omega C} - \omega L}{R_L + R_C}\right| \tag{4.10}$$

It could be concluded that when $\omega < 1/\sqrt{LC}$, Q_T is always smaller than Q_C. When $\omega > 1/\sqrt{LC}$,

$$Q_T - Q_C = \frac{\omega L - \frac{1}{\omega C}}{R_L + R_C} - \frac{1}{\omega C R_C} = \frac{\omega^2 LCR_C - 2R_C - R_L}{\omega C R_C (R_C + R_L)} \tag{4.11}$$

$$\text{When } \omega > \sqrt{\frac{1}{LC} \cdot \left(2 + \frac{R_L}{R_C}\right)}, \qquad Q_T > Q_C$$

It implies that the parallel inductor could be used to improve the *Q*-factor of the capacitor in the specified frequency range, which is much higher than the resonant frequency. In the meantime, the whole network presents an inductive characteristic. Recall that the *Q*-factor of the varactor becomes low in the mm-wave band. This technique could be used to increase the *Q*-factor of the varactor [77][78]. Consequently, the series combination of inductor and varactor behaves like a tunable inductor, whose inductance could be varied by the control voltage.

In the following we apply this LC series network to the cross-coupled pair. Suppose that the capacitive element in the LC series network is generated by the cross-coupled transistor. In this case, $R_C < 0$. The capacitor *C* represents the parasitic capacitance generated by the cross-coupled pair. For this application, the design concern is no longer the *Q*-factor, but the equivalent negative conductance. Recall the equivalent conductance of the network

$$Y = G + jB = \frac{R_L + R_C}{(R_L + R_C)^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} + j\frac{\left(\frac{1}{\omega C} - \omega L\right)}{(R_L + R_C)^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} \qquad (4.12)$$

Suppose $R_L + R_C < 0$, then $G < 0$, implying that the series network still behaves as a negative-conductance cell. Generally, this condition is easy to achieve, since the *Q*-factor of the inductor is much higher than the parasitic capacitance in mm-wave frequencies. It follows that

$$\frac{1}{G} - R_C = R_L + \frac{\left(\omega L - \frac{1}{\omega C}\right)^2}{R_L + R_C} \qquad (4.13)$$

When the frequency ω is close to $1/\sqrt{LC}$, $1/G - R_C \approx R_L > 0$, and hence, in the frequency range around the resonant frequency $1/\sqrt{LC}$, $|G| > |1/R_C|$.

The total series network provides more negative conductance than the cross-coupled pair alone. Besides, the network is transformed from capacitive to inductive across the resonant frequency point $\omega = 1/\sqrt{LC}$. Below the resonant frequency, the network presents a small capacitance, while it offers a small inductance above the resonant frequency. To ensure the correct operation of the VCO, the network should keep a capacitive character in the frequency range of interest. In a word, the series combination of an inductor and the cross-coupled pair could be designed to increase the negative conductance, meanwhile presenting a capacitive characteristic.

4.4. Circuit Design

The technique discussed above is used in the design of a 40 GHz CMOS VCO to enhance the negative conductance. In the reconfigured topology of the N-cell, the inductors L_1, L_2 are employed to resonate with cross-coupled transistors, as shown in Figure 4.10. With these inductors, the N-cell shows a similar characteristic to a resonator. As analyzed above, this reconfigured topology has the potential to improve the negative conductance of the cross-coupled pair.

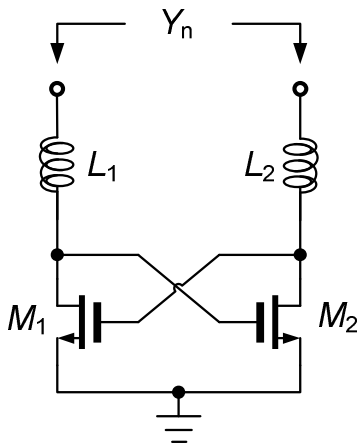


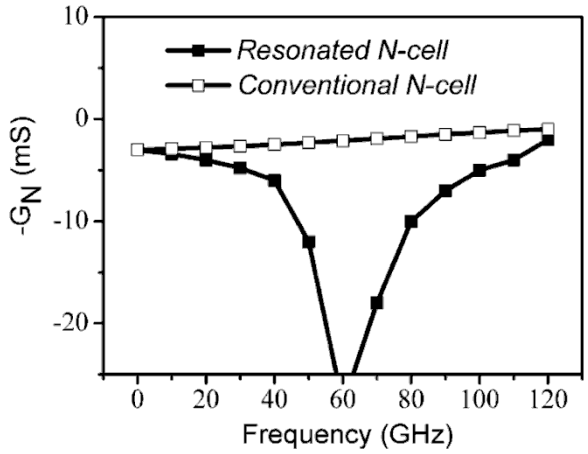
Figure 4.10 Reconfigured negative conductance cell

In chapter 3, the negative conductance generated by the cross-coupled pair is calculated. But the conclusion is tenable only at the low frequency, since the parasitic element has not been considered in the derivation. When the frequency becomes high, the generated negative conductance may reduce. The accurate evaluation of the negative conductance and parasitic capacitance requires simulations. The design is carried out with the help of s-parameter simulations. As shown in Figure 4.10, a differential port is given at the two terminals of the proposed N-cell. The negative conductance $-G_N$ and parasitic capacitance C_N are extracted as

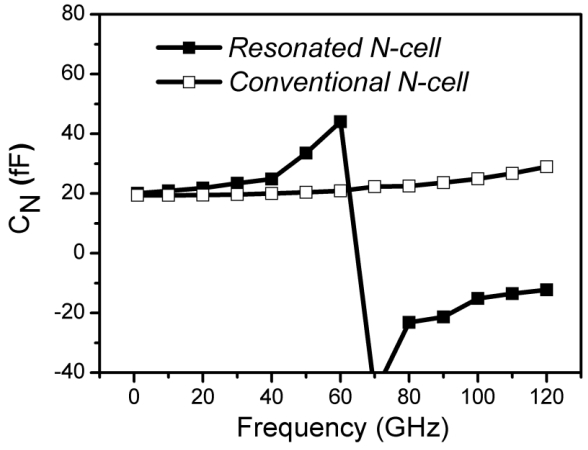
$$-G_N = real\ (Y_n) \tag{4.14}$$

$$C_N = \frac{imag(Y_n)}{\omega} \tag{4.15}$$

They are plotted in Figure 4.11. As we can see, $-G_N$ reaches a peak at the resonant frequency. C_N increases with the frequency and would shift to be inductive above the resonant frequency. As a result, by choosing the location of the resonant frequency carefully, it is possible to increase the negative conductance $-G_N$, and at the same time keep its parasitic capacitance C_N in the interested frequency range.



(a)



(b)

Figure 4.11 Simulated (a) negative conductance $-G_N$ and (b) parasitic capacitance C_N

Considering the targeted tuning range, the resonant frequency of the reconfigured N-cell is designed to be 63 GHz for a 40 GHz VCO. With a cross-

coupled transistor size of 8 μm/100 nm, this resonated N-cell achieves -6 mS negative conductance, while generating only 22 fF parasitic capacitances. The varactor with a size of 7 × 1.6 μm / 400 nm is large enough to attain approximately 10 % tuning range. Its comparatively high *Q*-factor and good linearity will lessen the design challenge for oscillation start-up and low phase noise.

Table 4.3 Design parameters of 40 GHz VCO

$M_{1\text{-}2}$	8 × 1 μm / 100 nm	$L_{1\text{-}2}$	170 pH @ 40 GHz
$M_{3\text{-}4}$	6 × 1 μm / 100 nm	$L_{3\text{-}4}$	330 pH @ 40 GHz
$M_{5\text{-}6}$	8 × 2.5 μm / 100 nm	C_{var1}, C_{var2}	7 × 1.6 μm / 400 nm
L_t	140 pH @ 40 GHz	$C_{1\text{-}2}$	40 fF

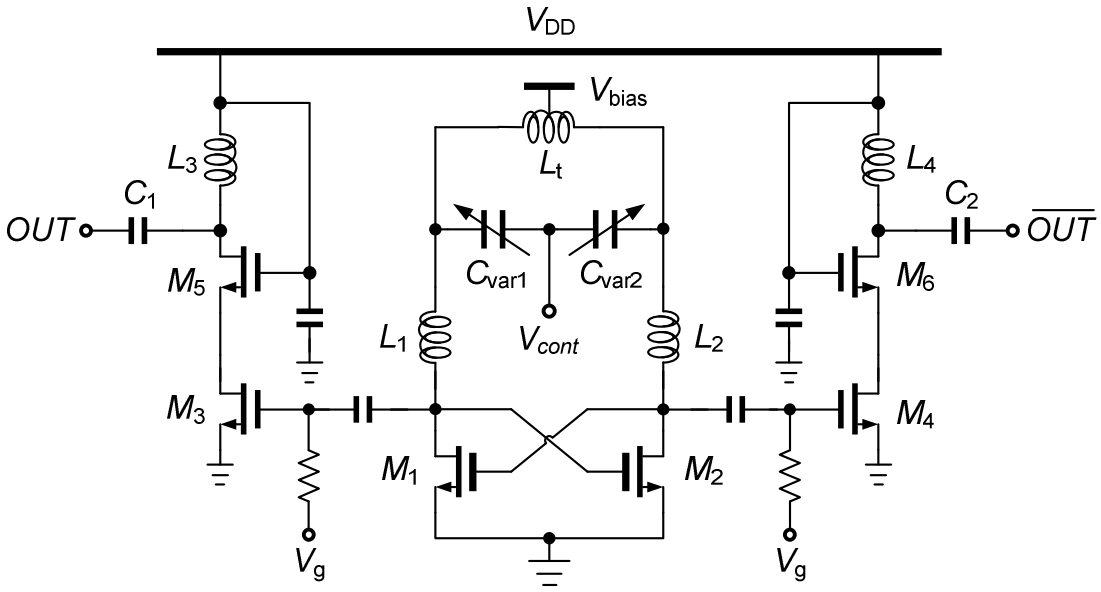


Figure 4.12 40 GHz VCO with resonated negative-conductance cell

Employing the resonated N-cell, a 40 GHz VCO has been designed in 90 nm CMOS technology. Figure 4.12 shows the schematic, where the current source is removed to suppress the effect of the AM-PM conversion. This topology is usually called the voltage biased oscillator [77]. The VCO is biased at 0.75 V (V_{bias}) where the

transistor has the minimum noise figure. The tank inductor L_t is implemented by a differential symmetric inductor for a higher Q-factor. The specific metal density is achieved in the area of the inductor using the proposed patterned dummy fills. From the EM-simulation by Ansoft HFSS, the inductor L_t is 140 pH with a Q-factor of 25 at 40 GHz. The inductors $L_{1\text{-}4}$ are designed as the square spiral inductor discussed above. To avoid the loading effect, a cascade output buffer with an inductive load was incorporated for 50 Ω measurement purposes.

In addition to boosting the negative conductance, the resonated N-cell also has a positive influence on the phase noise performance. Figure 4.13 shows the simulated voltage swing at the drain of cross-coupled transistors in the conventional N-cell and the resonated N-cell. Obviously, the voltage swing in the resonated N-cell is significantly increased. According to the LVT phase noise model [57], a large voltage swing could improve the switching speed of the cross-coupled transistor, weakening the AM-PM conversion. Therefore, this technique is able to improve the linearity of cross-coupled transistors and suppress AM-PM effects.

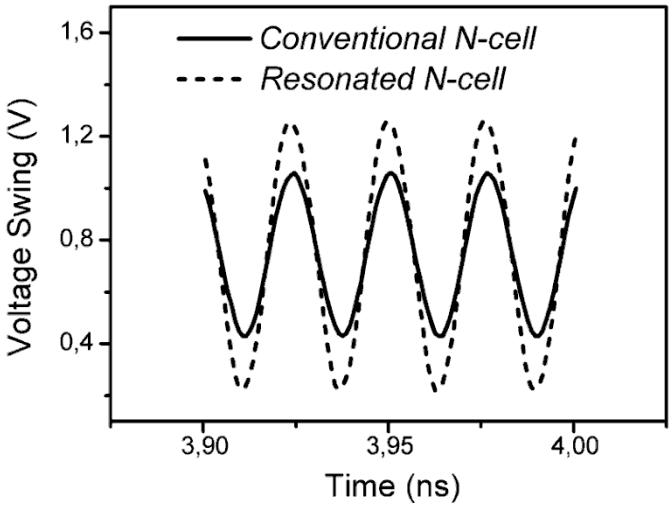


Figure 4.13 Simulated voltage swing at the drain of cross-coupled transistors

4.5. Experiment Results

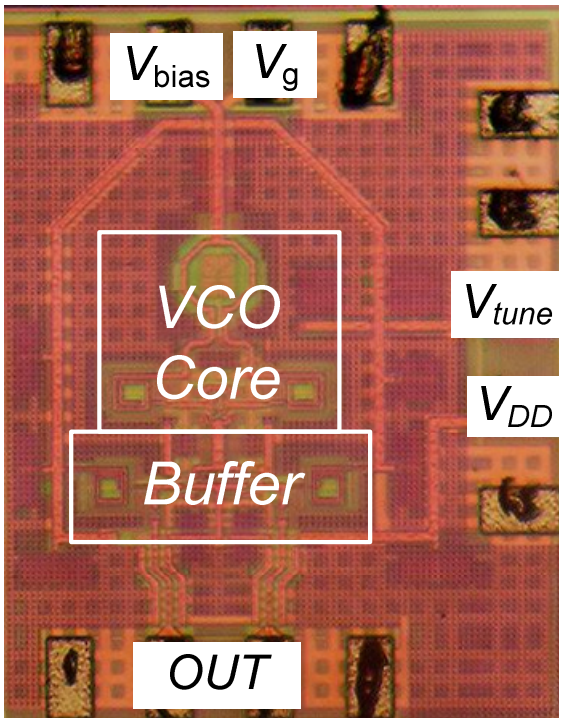


Figure 4.14 Micrograph

The chip photograph is shown in Figure 4.14. It has an area of 0.7×0.55 mm^2 including the pads. The chip was on-wafer measured using the Rohde&Schwarz (R&S) FSU67 spectrum analyzer. Only one single-ended output signal is delivered to the spectrum analyzer, and the other one connects to a 50 Ω terminal. When the VCO is biased with V_{bias} 0.75 V, it consumes 2.2 mA dc current. Sweeping the tuning voltage V_{tune} from 0 to 1.2 V, a frequency tuning range from 37.5 GHz to 41 GHz is measured. In Figure 4.15, the simulated and measured tuning range are plotted. In the design phase, interconnection wires of the layout were EM-simulated fully by the Ansoft HFSS. The s-parameters of the interconnection wires were used in the circuit simulation to characterize the parasitic elements in the layout. Therefore, a good agreement is achieved between simulation and measurement results.

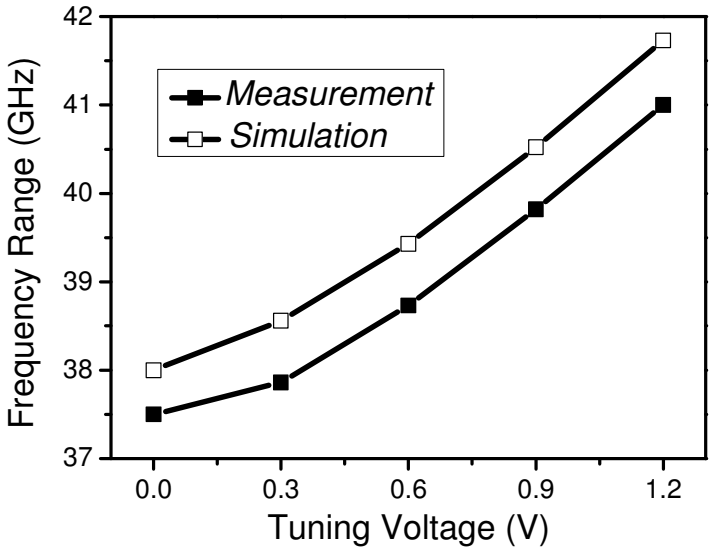
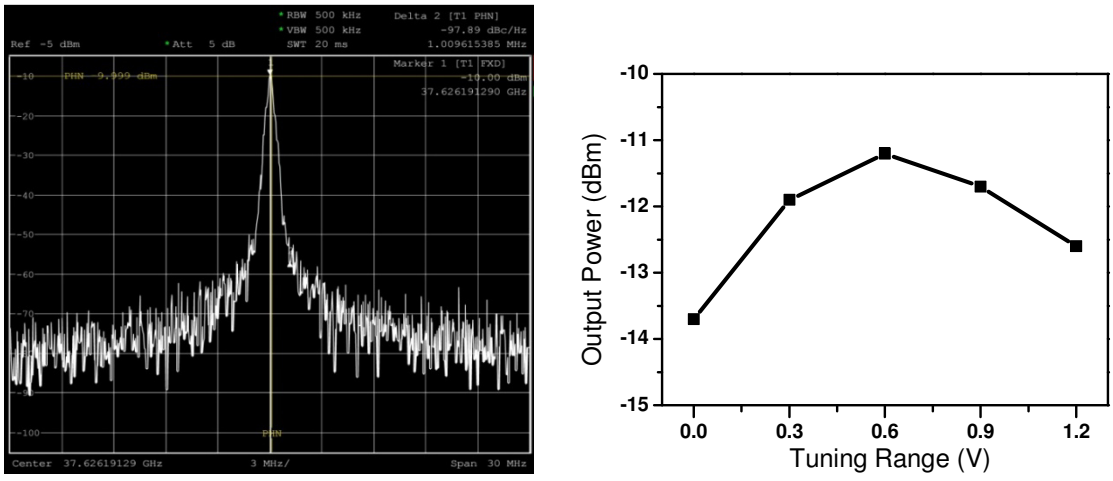


Figure 4.15 Measured and simulated tuning range

Figure 4.16 (a) presents a screenshot of the measured spectrum at 38 GHz. The measured output power is plotted in Figure 4.16 (b). The losses from probe heads, cables and connecters have been carefully de-embedded. In this work, a small output buffer is designed, to prevent overloading the VCO. The output power is therefore not high.



(a) **(b)**

Figure 4.16 Measured (a) output spectrum and (b) output power

The phase noise measurement for the mm-wave VCO is quite challenging, especially for a free-running VCO. The free-running VCO at the mm-wave frequency is pretty sensitive to the external noise sources. A tiny noise and disturbance from the voltage supply or tuning voltage could shift the oscillation frequency significantly. The condition might be more serious when the free-running VCO has a large tuning sensitivity. To generate stable and clean voltage biases, a circuit board employing batteries and potentiometer was used for the VCO measurements. Figure 4.17 shows the simplified environment of the phase noise measurement setup. Since the bias of V_{bias} and V_{tune} are directly given to the VCO core, they bring the largest influences on the noise measurement. Therefore, they are generated from the batteries. The potentiometer helps to vary the bias voltage.

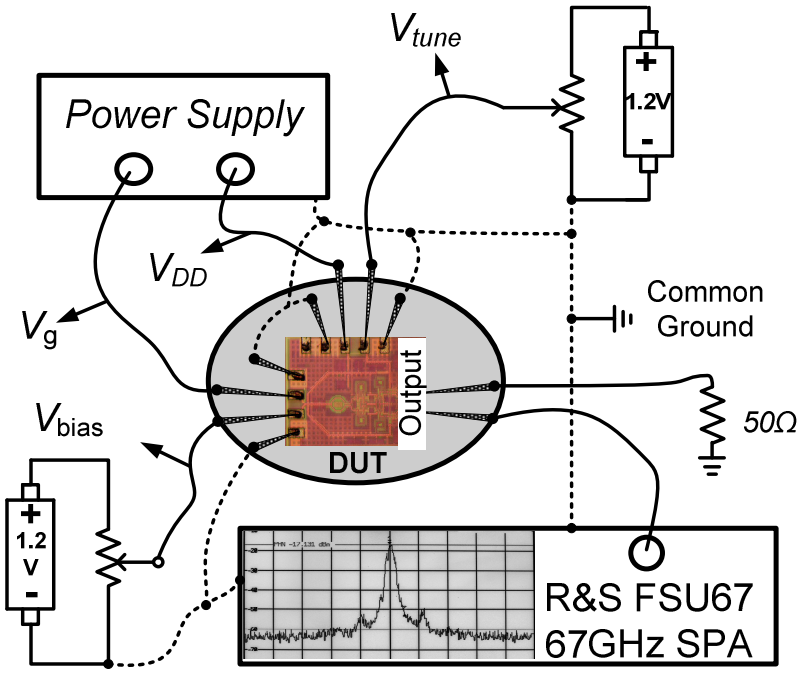
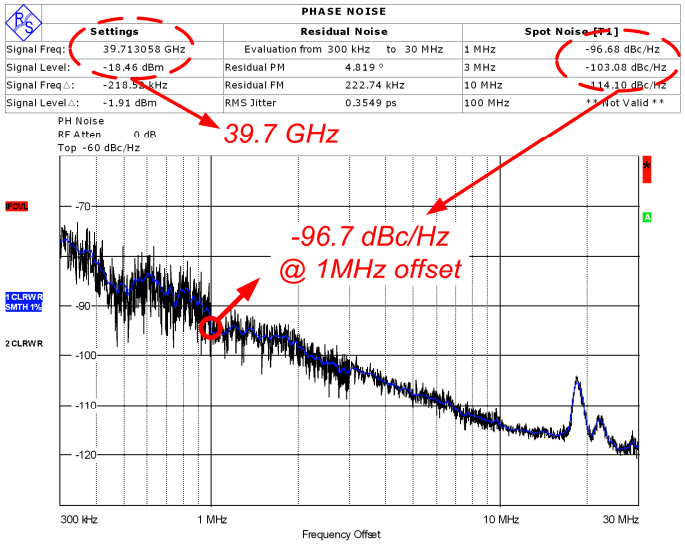


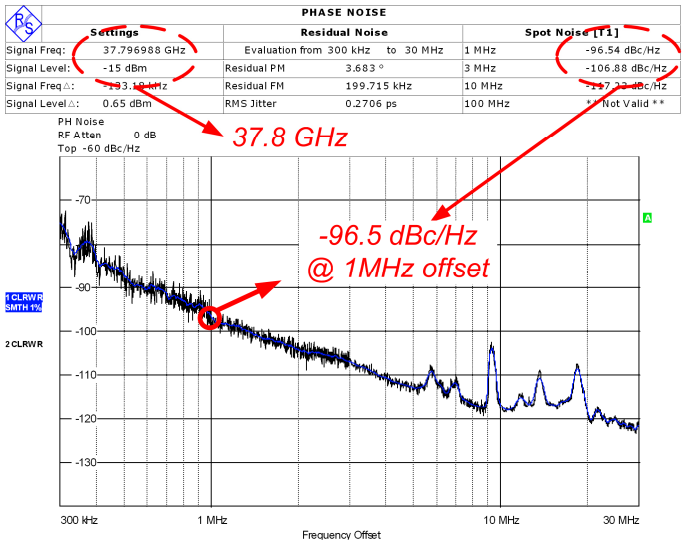
Figure 4.17 Phase noise measurement setup

Figure 4.18 shows two screenshots of the phase noise measurement results at 37.8 GHz and 39.7 GHz respectively. The phase noise performance at the 1 MHz frequency offset with respect to the carrier is of greatest concern. The phase noise at

this point is usually compared between various designs. As can be seen, lower than -96 dBc/Hz phase noises have been observed at 1 MHz frequency offset.



(a)



(b)

Figure 4.18 Screenshot of measured phase noise at (a) 39.7 GHz and (b) 37.8 GHz

4.6. Discussion

In Table 4.4, the performance of the designed VCO is summarized and compared with the reported mm-wave VCOs. As can be seen, most research work achieves improvement in only one performance for the mm-wave VCO design. Regarding the three most important performances, the tuning range, phase noise and power consumption, one of them might be improved at the price of degrading the other two. For instance, Ref [78] achieves a -101 dBc/Hz phase noise at 1 MHz offset but consumes too much power. The work in [79] presents a good phase noise, but 3.15 % tuning range is definitely unacceptable. On the contrary, the 40 GHz VCO in this work was not optimized for one particular performance specification. It achieves an excellent balance between these three performances. With the proposed resonated N-cell, the trade-off between the tuning range, phase noise and oscillation start-up in the mm-wave VCO design was lessened. A good figure-of-metric (FOM_T) of -185 dBc/Hz has been attained.

Table 4.4 Performance summary of mm-wave VCOs

Ref.	f_o (GHz)	FTR (%)	PHN@1MHz (dBc/Hz)	P_{DISS} (mW)	FoM_T* (dBc/Hz)	Tech.
[77]	58.4	9.32	-91	8.1	-176.6	90 nm CMOS
[80]	64	8.75	-95	3.16	-185	90 nm CMOS
[78]	49	1.6	-101	45	-162.4	0.18 μm CMOS
[79]	55.63	3.15	-94.8	8.25	-176.5	0.13 μm CMOS
[81]	44	9.8	-101	7.5	-184.8	0.12 μm SOI CMOS
This Work	39.25	8.9	-96.7	1.65	-185.4	90 nm CMOS

* $FOM_T=PHN-20\log((f_0/\Delta f)*(FTR/10))+10\log(P_{DISS}/1mW)$

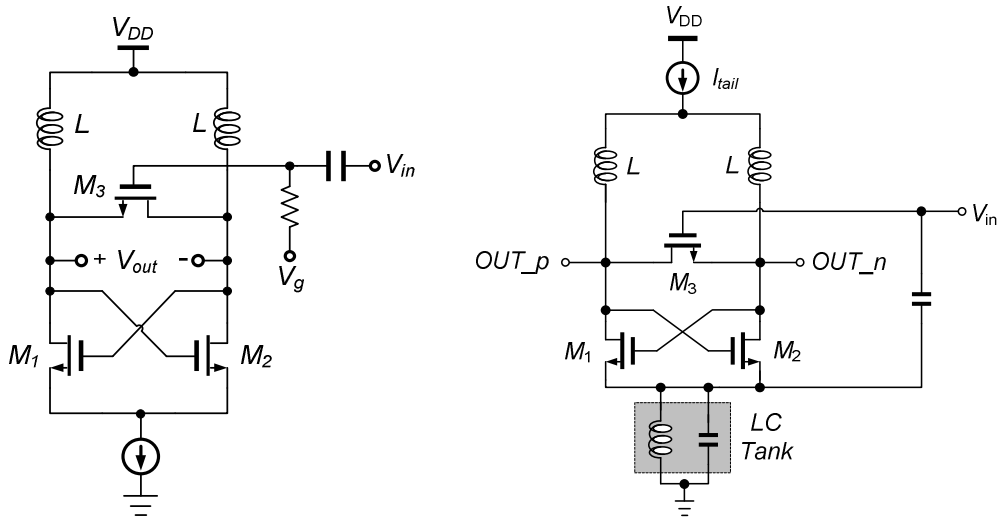
In this work, a 40 GHz VCO has been designed with 90 nm CMOS technology. An optimized topology of a resonated negative-conductance cell was proposed to amend the conventional cross-coupled VCO for mm-wave application. From On-wafer measurement results, the 40 GHz VCO achieves 8.9 % frequency tuning range and -96.7 dBc/Hz phase noise at 1 MHz offset, while consuming only 1.65 mW dc power. An excellent balance of all critical performance specifications has been achieved, resulting in a FOM_T of -185.4 dBc/Hz.

Chapter 5.
Design of Millimeter-wave Frequency Dividers

Three typical topologies of the 2:1 frequency divider are discussed in chapter 2. Their advantages and drawbacks have been analyzed. Compared with the ILFD and Miller divider, the static divider actually lacks operating capability at mm-wave frequencies. But with the specific design method, the static divider presents potential for achieving the divide-by-2 function at very high frequencies with the injection locking technique. Although the Miller divider would accomplish a larger locking range than the ILFD, analysis proves that the Miller divider operates inefficiently. The ILFD however suffers from a limited locking range. In recent research, most efforts have been focused on the static divider for the higher operation frequency, and the ILFD for the larger locking range. This chapter will emphasize these two aspects. Two demonstrations of mm-wave frequency dividers are presented. One is the design of a Q-band ILFD with 90 nm CMOS technology. An ILFD topology of transformer-based dual-path injection was proposed to maximize the injected power of the input signal and improve the locking range of the ILFD. The measurement result shows a 30.5 % locking range from 36 GHz to 49 GHz with 0 dBm input power. The other design is about an 8:1 static divider chain using 130 nm CMOS technology. A design process which highlights the balance between optimum operation frequency and output power has been proposed. By using this design flow, the 8:1 static divider chain is capable of operating up to 32 GHz with 0 dBm input power.

5.1. Design of Q-band Injection Locked Frequency Divider with Transformer-based Dual-path Injection

As introduced above, the locking range of the conventional ILFD shown in Figure 3.22 is limited at high frequencies due to the inefficient injection of the input signal. Since the locking range is proportional to the signal power injected into the oscillator core, it can be enhanced by maximizing the power gain of the injection path [65]. The direct injection-locking technique was proposed to improve the injection efficiency [66]. Figure 5.1 (a) shows a simplified version of this circuit. As illustrated, the direct ILFD provides a more efficient injection path, through M_3 directly to the oscillator core. Shortly afterwards, many techniques have been proposed to improve the injected power of the input signal and further locking range [82][83][84]. However, these techniques are primarily based on the optimization of the single injection path through M_3.



(a) **(b)**

Figure 5.1 (a) Direct ILFD and (b) Dual injection-locked frequency divider

In Ref. [85], a dual-injection-locked frequency divider (dual-ILFD) was demonstrated and achieved a wide-locking-range of more than 10 GHz. Figure 5.1 (b) presents its simplified schematic. The bias circuit of the input transistor M_3 is not

shown here. Besides the injection path through transistor M_3, the input signal is injected into the source node of the cross-coupled pair as well. Like the topology in [65], the LC shunt-peaking is constructed at the common-mode point of the cross-coupled pair to improve injection efficiency. However, the injected power is not maximized due to the absence of conjugate matching in the injection path. In other words, the injected power of the input signal could be increased through the input and inter-stage power matching in the injection path.

5.1.1. ILFD with Transformer-based Dual-path Injection

To continually improve the injected power, a topology with the transformer-based dual-path injection is proposed in this work. The schematic of the proposed ILFD is presented in Figure 5.2.

M_1, M_2	M_3	L_{tank}	C_{in}	I_{tail}
9 μm / 100 nm	14 μm / 100 nm	495 pH @ 20 GHz	60 fF	2.2 mA

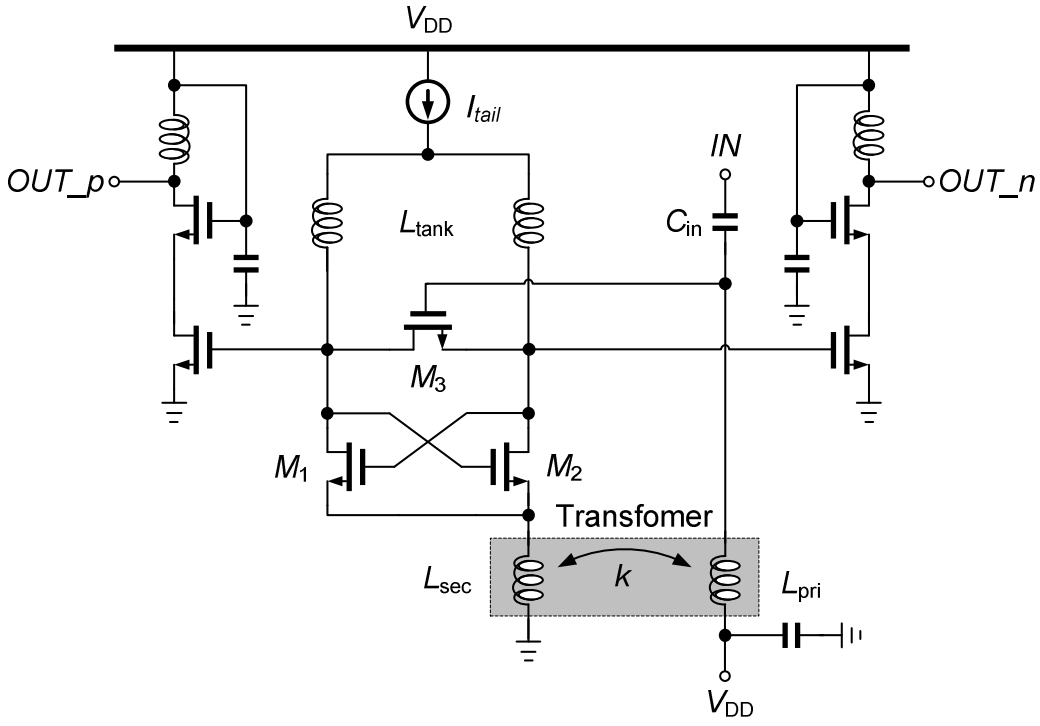


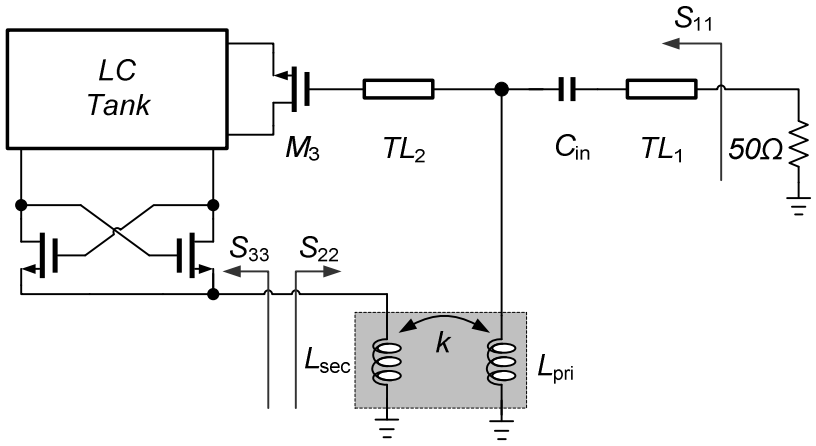
Figure 5.2 ILFD with transformer-based dual-path injection

The design starts from the conventional topology shown in Figure 5.1 (a). The free-running oscillator is designed to oscillate at around 20 GHz. As for the design of the tank inductor, a large inductance is preferable. The larger is the inductance, the smaller is the current required for oscillation start-up. From the equation (3.26), the decrease of I_{osc} results in locking range enhancement. Meanwhile, the cross-coupled pair (M_1 and M_3) with a same size could satisfy the condition for oscillation start-up. It implies that a smaller parasitic capacitance will exist at the injection point. From the EM simulation of Ansoft HFSS, the designed L_{tank} realizes 495 pH inductance and a Q-factor of 15 at 20 GHz. A cross-coupled pair with the size of 9 μm / 100 nm could start the oscillation. The proposed ILFD is represented in Figure 5.2.

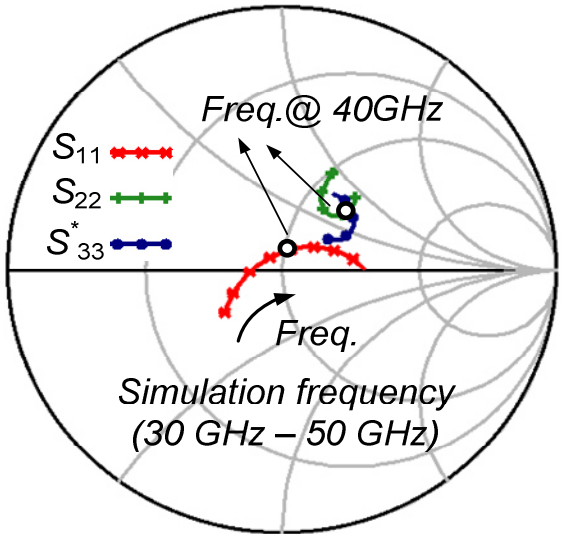
The topology of dual-path injection is preferred in this design. The first injection path is through transistor M_3. The design of M_3 size encounters a trade-off between the injection gain of the input signal and the parasitic capacitance introduced. It is carefully optimized resulting in a size of 10 × 1.4 μm / 0.1 μm. It is biased at V_{DD} for high injection gain. To prevent the loading effect, a one-stage cascode output buffer with the inductive load is also incorporated into the design. The output is matched to 50 Ω for measurement purposes. However, distinct from the topology in Figure 5.1, the second injection path of the input signal is through a transformer coupled to the source node of the cross-coupled transistors. The input matching and inter-stage matching of these injection paths are of great concern for the purpose of the locking range enhancement.

In the Ref.[85], the voltage and current injections of the input signal have been analyzed. However, the injected signal in each injection path is not always mixed with the intrinsic signal, only in the voltage or current domain [65]. Additionally, the power is clearer and preferable in the high-frequency design. Therefore, the power gain of the injection path is considered to be more significant. A transformer is introduced in the second injection path to achieve power matching in the proposed topology. As depicted in Figure 5.3 (a), the design process starts from the interface between the transformer and the source node of the cross-coupled transistor pair,

followed by the transformer design. Finally, 50 Ω matching is performed at the input terminal.



(a)

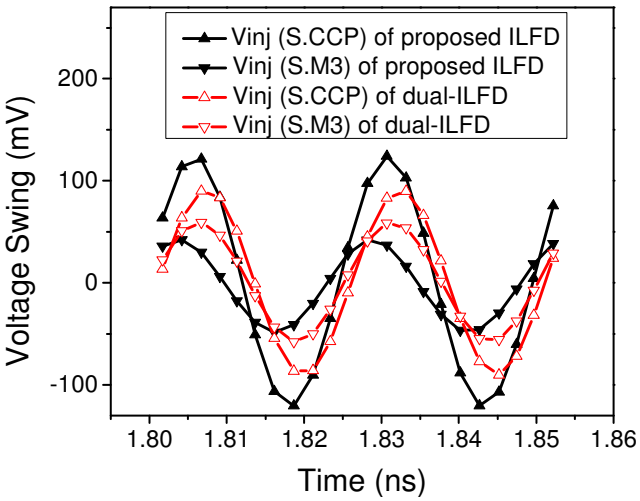


(b)

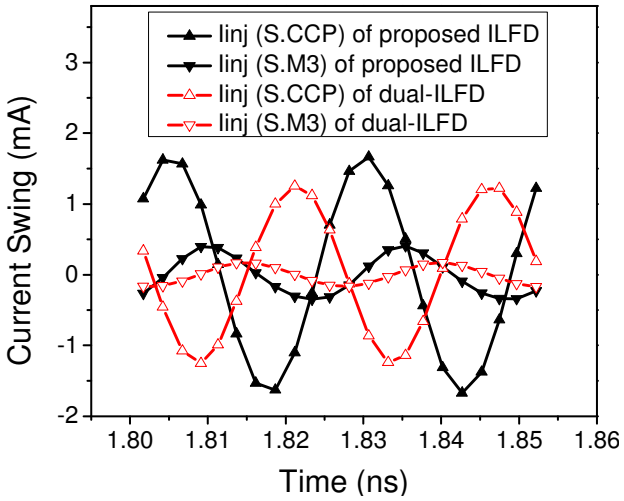
Figure 5.3 Power matching of proposed ILFD

The size of the transformer was designed to match the impedances between the secondary inductor L_{sec} and the source node of the cross-coupled pair. The S-parameter simulation results are illustrated in the Smith chart of Figure 5.3 (b). As we can see, looking into the L_{sec}, the impedance S_{22} is matched to the conjugate impedance at the source node of the cross-coupled pair (S^*_{33}), at around 40 GHz. The

matching at the input terminal is achieved by the capacitor C_{in} (60 fF) and primary inductor L_{pri} of the transformer. The transmission lines TL_1 and TL_2 which are used for interconnections, have also been absorbed into the matching network. The S_{11} curve in the Smith chart, representing the input matching, shows a wideband matching to 50 Ω from 30 GHz to 50 GHz. Due to the mutual coupling between the two inductors of the transformer, the input matching and inter-stage matching would affect each other. Thus the design is actually an iterative process.



(a)



(b)

Figure 5.4 Simulated (a) voltage swing and (b) current swing of injected signal in dual-ILFD and proposed ILFD

Since it is difficult to test injected power in the simulation, both voltage and current swing of the injected signal at the source node of transistor M_3 (S.M3) and the source node of the cross-coupled pair (S.CCP) are simulated and displayed in Figure 5.4. In the simulation, the input signal is at 40 GHz with -5 dBm power. For the simulation of dual-ILFD as shown in Figure 5.1 (b), the parameters of the LC tank are 120 pH and 100 fF respectively, which result in a LC resonator at 40 GHz together with the parasitic capacitance. As can be seen, through power matching in the proposed ILFD, the current swing in both two injection paths and voltage swing in the injection path of the cross-coupled pair are increased significantly.

5.1.2. Transformer Design

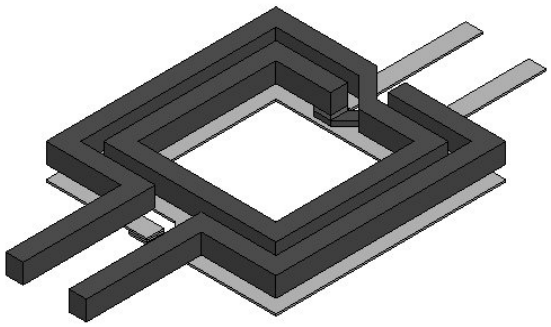


Figure 5.5 Transformer with stacked structures

The designed transformer has a stacked structure. As can be seen from Figure 5.5, the transformer is constructed by stacking vertically two symmetrical inductors, each one with two turns. The primary inductor is designed in metal 9 with metal 8 crossovers, while the secondary one is formed by metal 7 with metal 6 crossovers. It is designed with the assistance of Ansoft HFSS. It has been proven that the transformer with vertically stacked structures could achieve a higher coupling coefficient than the planar transformer [86]. According to the following equation [87]

$$k = \sqrt{\frac{(imag(Z_{12}))^2}{imag(Z_{11}) \cdot imag(Z_{22})}} \tag{5.1}$$

the coupling coefficient k is extracted from the simulated s-parameter data by Ansoft HFSS, and plotted in Figure 5.6. The coupling coefficient is higher than 0.6 at 40 GHz.

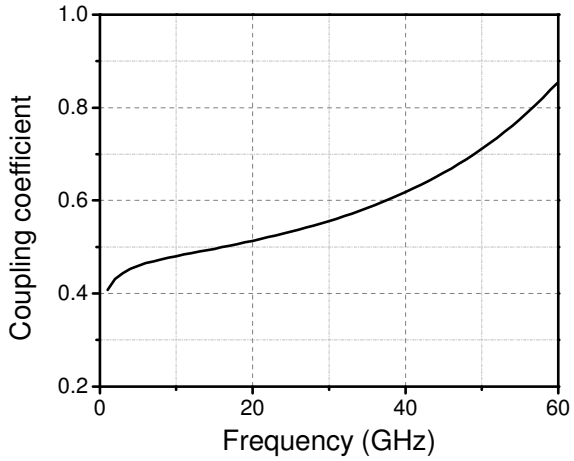


Figure 5.6 Coupling coefficient of transformer

5.1.3. Measurement Results

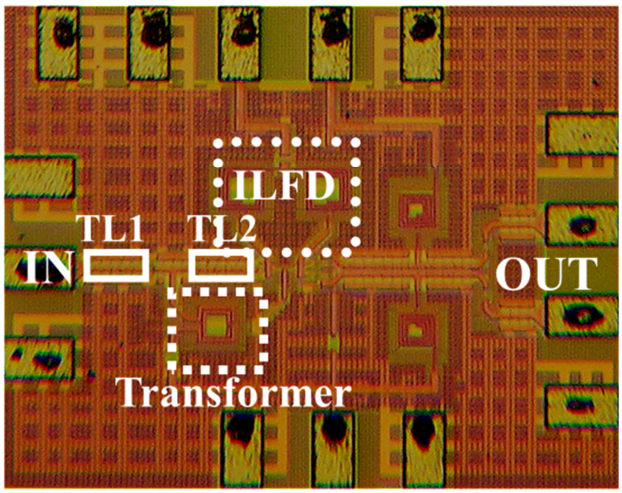


Figure 5.7 Chip micrograph

The proposed ILFD was implemented in 90 nm CMOS technology. Figure 5.7 shows the chip micrograph. It has an area of 0.7×0.53 mm^2 including the pads. The measurement was performed on-wafer with a 1.2 V supply voltage. The input signal is attained from the Agilent 83650B 50 GHz signal generator and the output signal is measured by the R&S FSU67 spectrum analyzer. The losses of cables, connectors and probe heads have been carefully calibrated from the measurement results.

Figure 5.8 displays the measured free-running spectrum and locked spectrum together. The ILFD is oscillating freely at 21.8 GHz. The locked output spectrum is measured with a -5 dBm input signal at 44 GHz. Obviously, the output signal presents a better phase noise after locking.

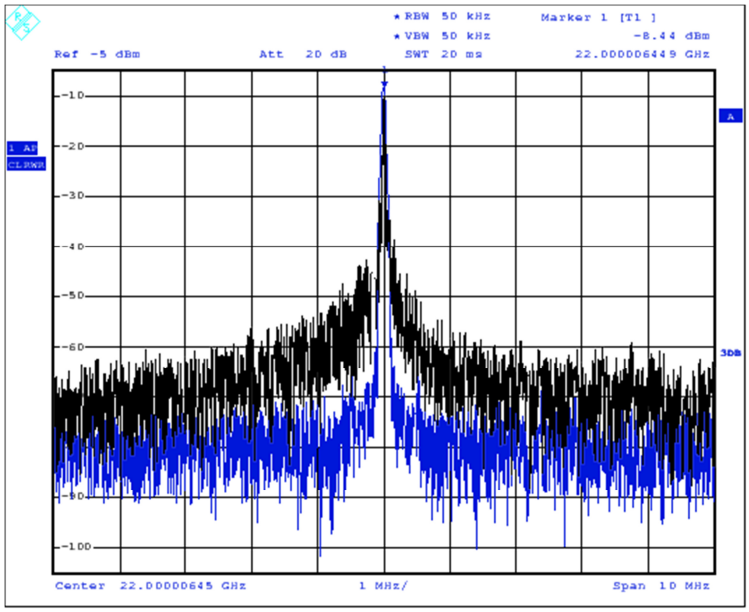


Figure 5.8 Output spectrum

In Figure 5.9, the simulated and measured input sensitivity are plotted. The ILFD dissipates 2.2 mA dc current under a 1.2 V supply voltage. Measurement results showed that with 0 dBm input power, the proposed ILFD achieved a wide locking range from 36 GHz to 49 GHz. Even with -5 dBm input power, it still functions from 38 GHz to 47 GHz. This is still a 21% locking range. This result is of great significance when the ILFD is integrated into the PLL system. Actually, it is quite

difficult for an mm-wave VCO to delivery 0 dBm power, even with a one-stage buffer. The power of the ILFD's input signal is usually between -5 dBm and -10 dBm. This is a more reasonable condition when the ILFD is integrated into an mm-wave PLL.

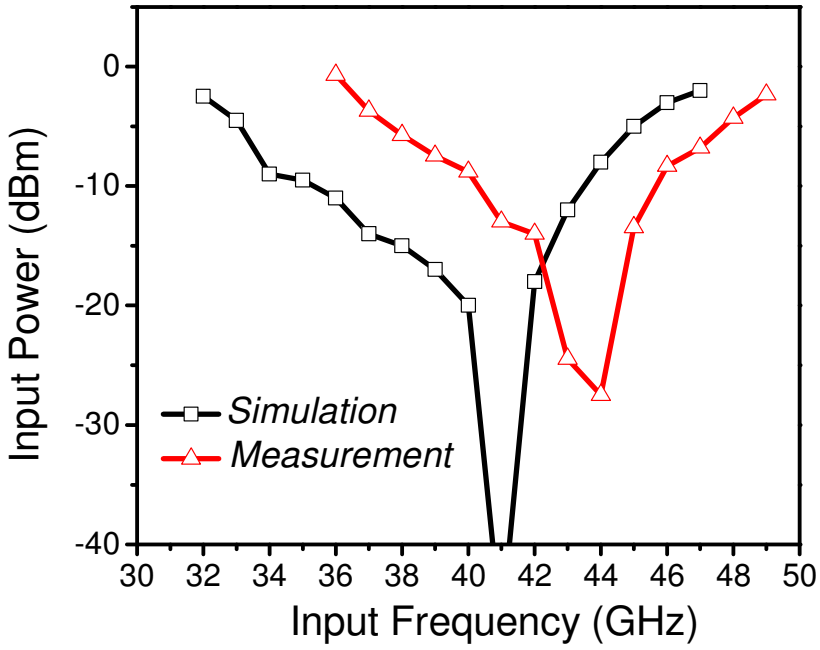


Figure 5.9 Measured and simulated input sensitivity

5.1.4. Discussion

Table 5.1 summarizes the performance of the designed ILFD and compares it with the reported mm-wave ILFDs. As we can see, the ILFD achieving a 30.5 % locking range is one of the best implementations presented so far. With the proposed transformer-based dual-path injection, the injected power was increased, resulting in a wider locking range. Some reported designs employ a very low supply voltage, in order to reduce the total power consumption. But it is not normal, and it does not really make sense. These designs without a standard supply voltage actually cannot be used in practice. Considering further integration into a PLL circuit, the proposed ILFD is designed with a normal 1.2 V supply voltage.

Table 5.1 Performance comparison of published ILFDs

Ref.	Technology	V_{DD} (V)	Locking range (GHz) @ 0 dBm input	P_{dc} (mW)	Area (mm^2)
[85]	90 nm CMOS	0.8	39 – 51 (26.7 %)*	0.8	0.385
[84]	0.13 μm CMOS	1	67 – 75.3 (11.7 %)	4.4	N/A
[82]	0.13 μm CMOS	0.9	49 – 62 (23 %)	10.8	0.325
[83]	0.13 μm CMOS	0.7	53 – 62.4 (16.3 %)	3.93	0.325
[88]	90 nm CMOS	N/A	55.5 – 60 (6.9 %)	5	0.15
[89]	0.18 μm CMOS	1	38.6 – 49.2 (24 %)	6	0.42
This work	90 nm CMOS	1.2	36 – 49 (30.5 %)	2.64	0.37

* The percentage locking range is defined as LR (%) = $2*(f_{max}-f_{min})/(f_{max}+f_{min})$

In this work, a Q-band ILFD has been demonstrated using 90 nm CMOS technology. An ILFD topology of transformer-based dual-path injection was proposed to maximize the power gain of the injection path and to improve the locking range of the ILFD. On-wafer measurements showed that with 0 dBm input power, the proposed ILFD achieves a 30.5 % locking range from 36 GHz to 49 GHz and consumes only 2.64 mW with a 1.2 V supply voltage. The proposed ILFD compares the best solutions so far achieved.

5.2. Design of 8:1 Static Divider Chain using 130 nm CMOS Technology

This work concerns the design of a 3-stage static divider chain using 130 nm CMOS technology. In reality, the static divider with the conventional CML latch, shown in Figure 3.18, is unable to operate at mm-wave frequencies. The design here is still based on the topology of the conventional CML latch, but without the tail current source, as shown in Figure 5.10. Removing the current source saves the voltage headroom. In this topology, the operating current of the latch is not determined by the tail current source. So it is no longer the current mode logic. When the rising edge of the clock signal comes, more current would flow into the differential pair $M_{3\text{-}4}$, improving the operation speed of the latch. The clock transistors $M_{1\text{-}2}$ experience a sort of class-AB operation, like the class-AB amplifier [89]. Thus, this latch is also called the 'class-AB latch'.

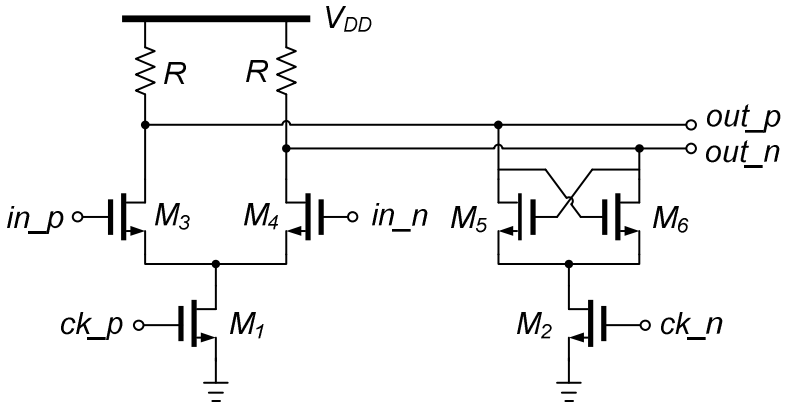


Figure 5.10 Latch without current source

The inductor peaking [59], or any other broadband technique, is not used in this design. A specific design flow for the 2:1 mm-wave static divider is proposed, which emphasizes the balance between the operation frequency and the output power. By using this design flow, the designed 8:1 static divider chain operates correctly up to 32 GHz with 0 dBm input power.

5.2.1. Design of 2:1 mm-wave static divider based on self-oscillation

As for the first stage divider as shown in Figure 5.11, the resistor load is replaced by a PMOS load $M_{13\text{-}16}$ operating in the deep triode region, since it achieves a higher *Q*-factor and is more tolerant towards process variation.

$M_{1\text{-}4}$	$M_{5\text{-}8}$	$M_{9\text{-}12}$	$M_{13\text{-}16}$	C_1	V_g
$\frac{35\ \mu m}{120\ nm}$	$\frac{3\ \mu m}{120\ nm}$	$\frac{60\ \mu m}{120\ nm}$	$\frac{13\ \mu m}{120\ nm}$	1 pF	600 mV

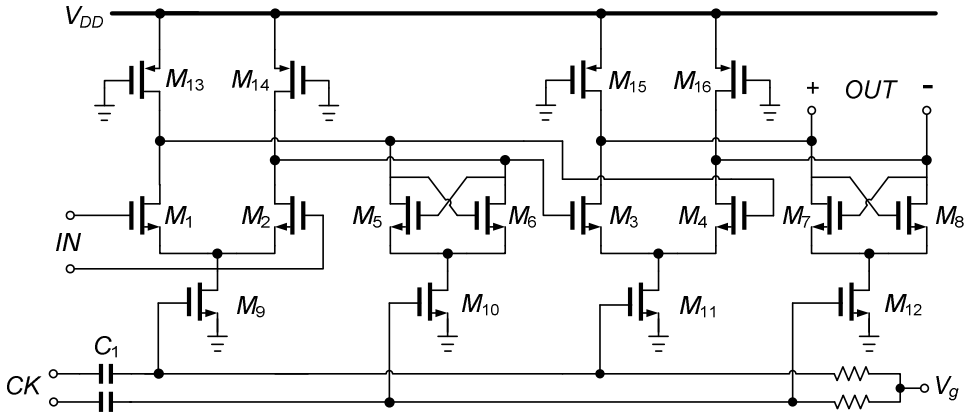


Figure 5.11 First stage static divider

Design considerations focus on the first stage static divider because of the highest operation frequency. In order to make it function in the mm-wave frequency band, a standard design process is to design it as a ring-oscillator [59][90]. The condition for starting oscillation is

$$g_{m,ccp} \cdot R_p \geq 1 \tag{5.2}$$

Its self-oscillation frequency f_o depends upon the delay τ_{ed} at output, given by

$$f_o \propto \frac{1}{\tau_{ed}} = \frac{1}{C_{tot} \cdot R_p} \tag{5.3}$$

where the $g_{m,ccp}$ is the transconductance of the cross-coupled pair $M_{5\text{-}8}$. R_p is the equivalent resistance of the PMOS load, C_{tot} is the total capacitance at the output

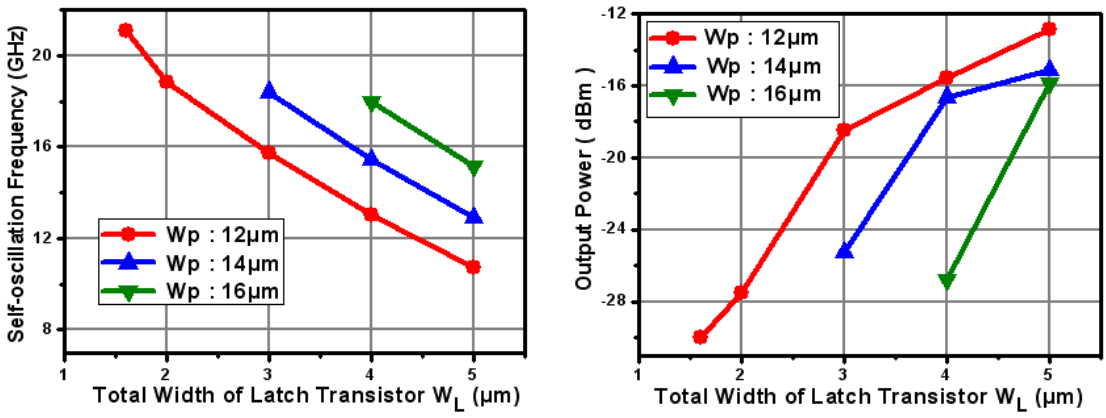
terminal, including the parasitic capacitance from the differential pair $M_{1\text{-}4}$, the cross-coupled pair $M_{5\text{-}8}$ and the input capacitance of the next stage. The highest operation frequency of the 2:1 static divider is around $2f_o$. A higher self-oscillation frequency f_o leads to a higher operation frequency of the static divider. Therefore, a small size of $M_{5\text{-}8}$ and a large size of $M_{13\text{-}16}$ are preferred.

In addition to the target for a high operation frequency, the design for enough output swing is also required. This ensures the correct operation of the next stage static divider. When the divider operates like a ring oscillator, the voltage swing at the output of each latch would rise at the beginning of the oscillation, and then stabilize to a saturation value limited by the nonlinearity of the circuit. In this condition, the differential pair $M_{1\text{-}4}$ are switching fully and the output swing V_{sw} is given by

$$V_{sw} = I_{tail} \cdot \left(R_p \,//\, R_L\right) \tag{5.4}$$

Here I_{tail} corresponds to the current of the latch, and R_L is the negative resistance provided by the cross-coupled latch $M_{5\text{-}8}$. This situation is similar when it operates as a static divider. Therefore, the output power of the self-oscillation is considered as an estimate for divider's output swing in the design phase. For a large output swing, small PMOS transistors $M_{13\text{-}16}$ should be designed, since the load resistance is inversely proportional to the size of $M_{13\text{-}16}$. The latch transistor should be large for a large negative resistor. This finding is obviously inconsistent with above design for the high f_{so}. The requirement for transistors $M_{1\text{-}4}$ is to achieve full switching. Thus, they have little effect on the output swing.

From the above analysis, it can be seen that the size of the PMOS load $M_{13\text{-}16}$ and latch transistors $M_{5\text{-}8}$ have the largest impact on the divider's performance. They require careful designs. In the initial simulation, the sizes of $M_{1\text{-}4}$ and $M_{9\text{-}12}$ are fixed at 5 μm. The simulated self-oscillation frequency f_{so} is shown in Figure 5.12 (a) as the function of total width W_L of $M_{5\text{-}8}$ and total width W_p of $M_{13\text{-}16}$. As can be seen, the self-oscillation frequency f_{so} rises by increasing the W_p and decreasing the W_L. When transistor $M_{5\text{-}8}$ is too small, the oscillation condition of equation (5.2) is not satisfied. Figure 5.12 (b) shows the output power level of the self-oscillation. It can be seen that the design for a high operation frequency is at the cost of sacrificing the output power.



(a) **(b)**

Figure 5.12 (a) Oscillation frequency f_{so} and (b) output power of self-oscillation as a function of width W_L(M_{5-8}), width W_P (M_{13-16})

After choosing the size of transistors M_{5-8} and M_{13-16}, the size of transistors M_{1-4} also requires optimization. In Figure 5.13, the simulated f_{so} and output power are presented as varying the total width W_D of the drive transistors M_{1-4}, while the size of PMOS load M_{13-16} is fixed at 12 μm. Clearly, the decrease of W_D improves the linearity of M_{1-4}, gradually leading to the full switching operation. Eventually, the output power becomes constant which is irrelevant with W_D. In addition, the size of M_D has little impact on the f_{so}, in accordance with the above analysis.

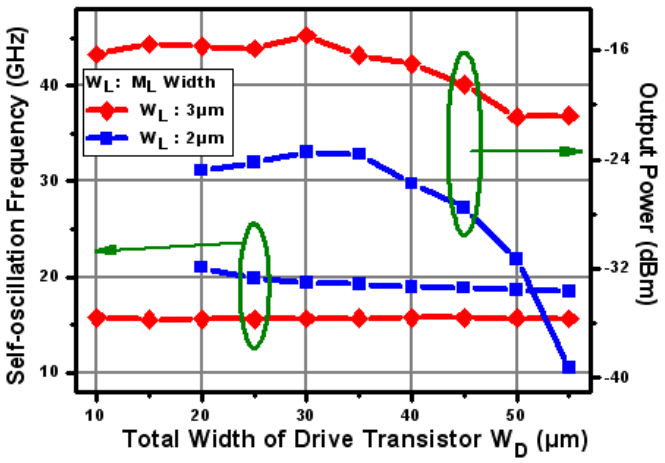


Figure 5.13 Oscillation frequency and output power of self-oscillation as a function of width (W_D) of transistors M_{1-4}

Apart from the high operation frequency and large output swing, and taking the power consumption into account, the final design size for M_D, M_L and M_P are 35 μm, 3 μm and 13 μm respectively. The clock transistor $M_{1\text{-}4}$ is large enough to achieve high input sensitivity, which is 60 μm in this design.

5.2.2. Design of 8:1 Static Divider Chain

The design of the first stage 2:1 static divider is carried out with the specific design flow, as discussed above. It is based on the self-oscillation operation mode of the static divider at high frequencies. This approach helps to improve the operation frequency of the static divider. In the meantime, the output power has also been seriously considered for this one-stage divider. It is regarded as a measure of the output amplitude in the design phase. Enough output power of the first stage 2:1 static divider would ensure the correct operation of next stage divider, and allow the construction of a static divider chain. A 3-stage static divider chain is further designed, employing the above 2:1 divider as its first stage. Its block diagram is described in Figure 5.14. A simple differential amplifier is designed at the output for measurement purposes.

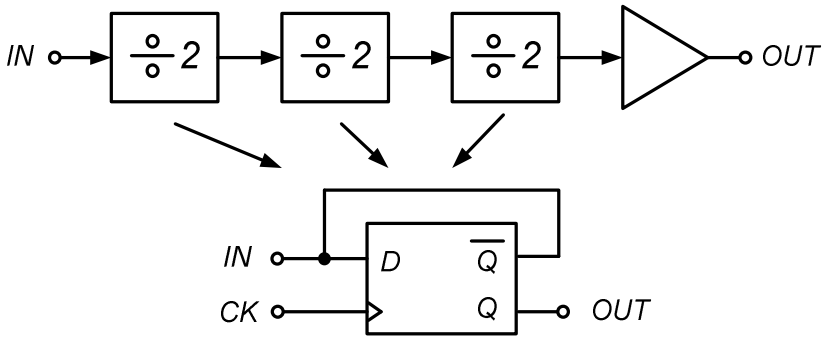


Figure 5.14 Block diagram of the 8:1 static divider

Because of different operation frequencies, distinct topologies are selected for these three stage divider-by-2 circuits. Figure 5.15 displays the design of the second stage 2:1 static divider.

$M_{1\text{-}4}$	$M_{5\text{-}8}$	$M_{9\text{-}12}$	R_{load}	C_1	V_g
$\frac{30\ \mu m}{120\ nm}$	$\frac{6\ \mu m}{120\ nm}$	$\frac{10\ \mu m}{120\ nm}$	550 Ω	1pF	600 mV

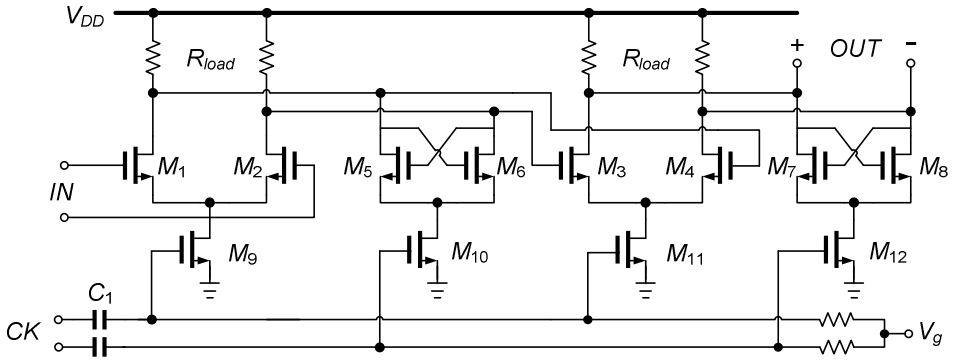


Figure 5.15 Second stage static divider

For the third stage 2:1 static divider, the frequency is around several-GHz and the design becomes much more relaxed. Therefore, it is implemented as a standard CML static divider with an optimized power and bandwidth, as shown in Figure 5.16.

$M_{1\text{-}4}$	$M_{5\text{-}8}$	$M_{9\text{-}12}$	R_{load}	$I_{1\text{-}2}$
$\frac{28\ \mu m}{120\ nm}$	$\frac{7\ \mu m}{120\ nm}$	$\frac{15\ \mu m}{120\ nm}$	650 Ω	0.8 mA

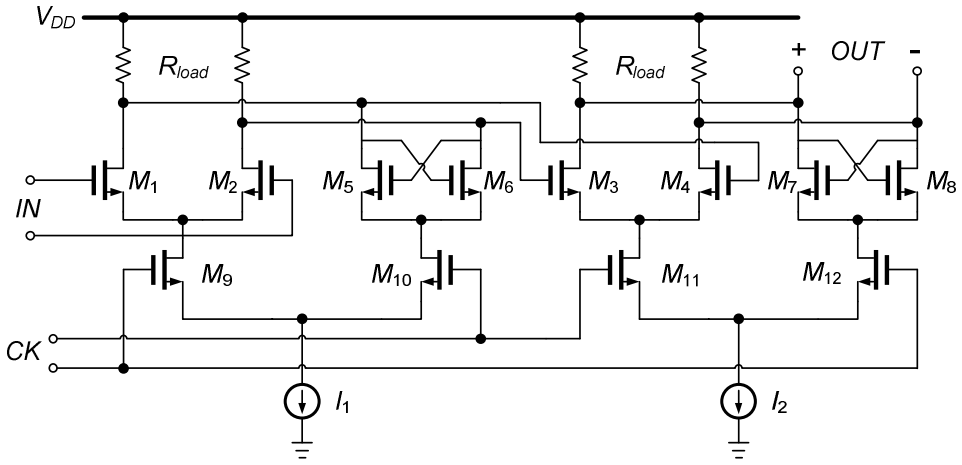


Figure 5.16 Third stage static divider

5.2.3. Experiment Results

The micrograph of the chip is shown in Figure 5.17. In this chip, an 8:1 static divider chain is implemented using 0.13 μm CMOS technology. To facilitate on-chip measurement, an on-chip wideband passive balun was also designed to generate the differential input signal. The area of active circuit is only 200 μm × 100 μm. In this measurement, a 40 GHz signal generator is used to generate the input signal. The output signal is measured with the Agilent Spectrum Analyzer E4440A. With a 1.2 V supply voltage, the whole circuit consumes 14.5 mA current, including 3 mA for the output buffer. The first 2:1 static divider dissipates only 6 mA current.

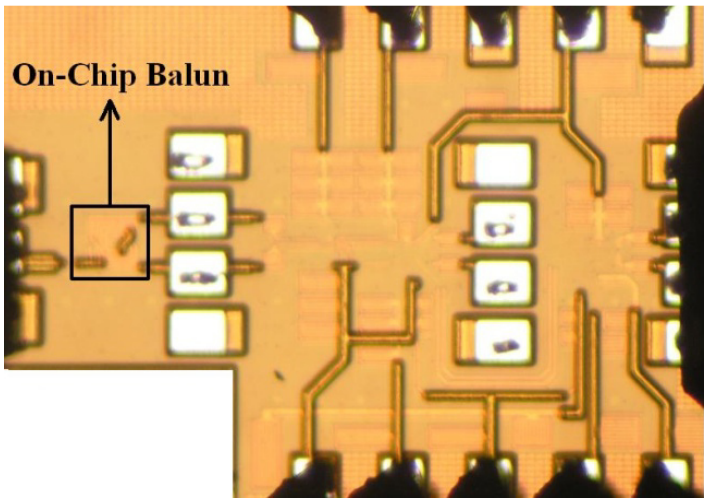


Figure 5.17 Micrograph of the fabricated chip

The measured and simulated input sensitivity of the 8:1 static divider is shown in Figure 5.18. The losses of cables, probes and the on-chip balun have been de-embedded from the input power. With 0 dBm input power, the circuit can operate up to 34 GHz. Since the loss of the on-chip passive balun is too large at low frequencies, the static divider cannot get enough input power and stop operating below 9 GHz. Measurements showed approximately 12 dB loss for the balun at 8 GHz.

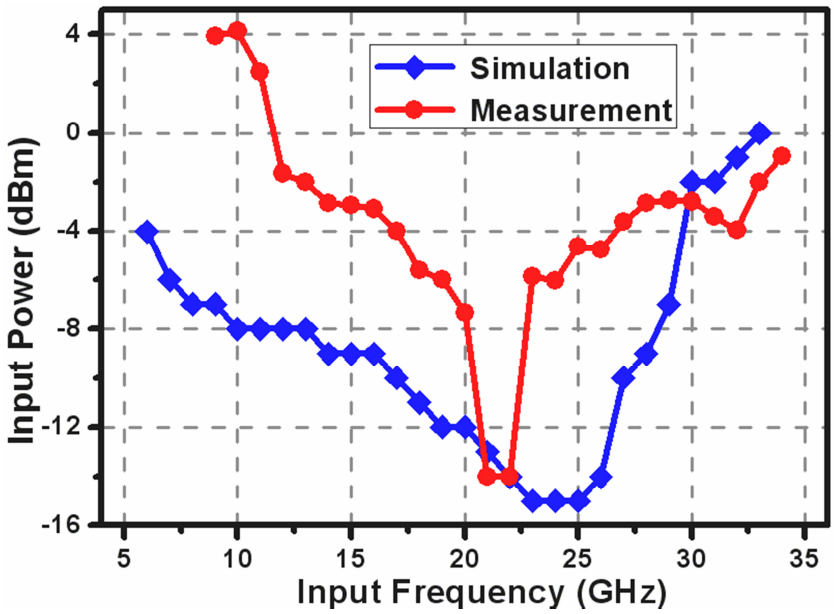


Figure 5.18 Measured and simulated input sensitivity of 8:1 static divider

Figure 5.19 shows a screenshot of the output spectrum when the 8:1 static divider operates with a 24 GHz input signal. Both input and output signals are observed in the spectrum. Since the output buffer is not matched to 50 Ω, the output power is low.

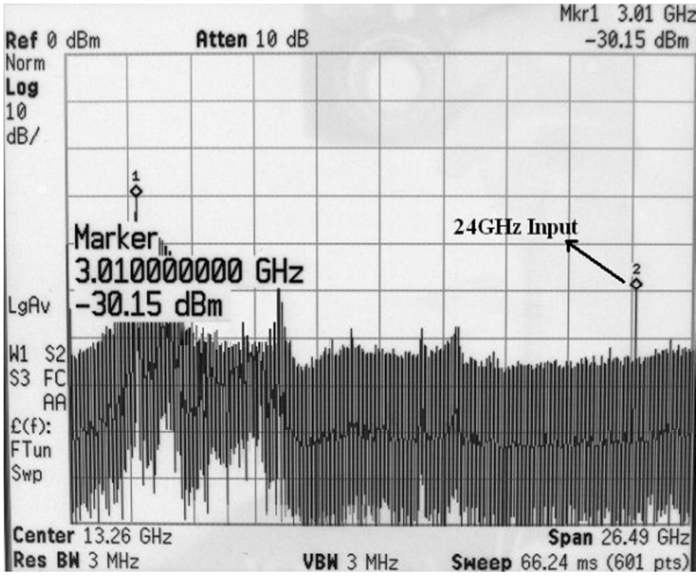


Figure 5.19 Output spectrum with 24 GHz input signal

5.2.4. Discussion

Table 5.2 summarizes the performance of the designed static divider and compares it with the recently published static dividers. As can be seen for the first stage 2:1 static divider, its power consumption is less than that of the other 2:1 static dividers, which can operate in the mm-wave frequency range. It is more important that the first 2:1 static divider delivers enough output power for the next stages, guaranteeing a correct divide-by-8 operation up to 34 GHz.

Table 5.2 Performance comparison of static dividers

Ref.	V_{DD} (V)	Division Ratio	Input Power (dBm)	Maximum Operation Freq. (GHz)	DC Power (mW)	Technology
[91]	2.4	2:1	-6	33	22.1	0.12 μm SOI CMOS
[92]	1.8	2:1	-2	40	12	0.13 μm CMOS
[93]	1.5	2:1	10	27	45*	0.12 μm CMOS
[94]	1.5	32:1	0	26	9	0.13 μm CMOS
This Work	1.2	2:1	0	34	7	0.13 μm CMOS
		8:1			17.5*	

* Including power consumption of output buffers.

In this work, a specific design process was proposed for CMOS mm-wave static dividers. It is based on the self-oscillation operation mode of the high-frequency static divider. Meanwhile, it highlights the balance between optimum operation frequency and output power. By using this design flow, an 8:1 static divider has been devised using 0.13 μm CMOS technology. Without employing the inductor peaking or any other broadband technique, the 3-stage 8:1 static divider is capable of operating up to 32 GHz with 0 dBm input power. The performance achieved compares well with the best reported state-of-the-art developments.

Chapter 6.

Design of 40 GHz Frequency Synthesizer for IEEE Standard 802.15.3c

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As introduced in chapter 1, the recently announced IEEE standard 802.15.3c is capable of short-range high speed communication up to Gbps. In Europe, it offers an unlicensed 9 GHz spectrum from 57 GHz to 66 GHz. According to specific applications, this standard provides various modes of the physical layer (PHY), such as the single-carrier (SC) PHY, the high speed interface (HSI) PHY and the audio visual (AV) PHY. For high data-rate applications, HIS PHY specifies multiple carriers with a large channel bandwidth. It includes three different channel plans, with 500 MHz, 1 GHz and 2 GHz channel bandwidths respectively. In order to achieve the highest data-rate transmission, the 2 GHz channel plan is chosen in this work.

Table 6.1 Channel bandwidth and carriers

	Channel 1	Channel 2	Channel 3	Channel 4
Bandwidth (GHz)	57.24 – 59.4	59.4 – 61.56	61.56 – 63.72	63.72 – 65.88
Center Freq. (GHz)	58.32	60.48	62.64	64.8

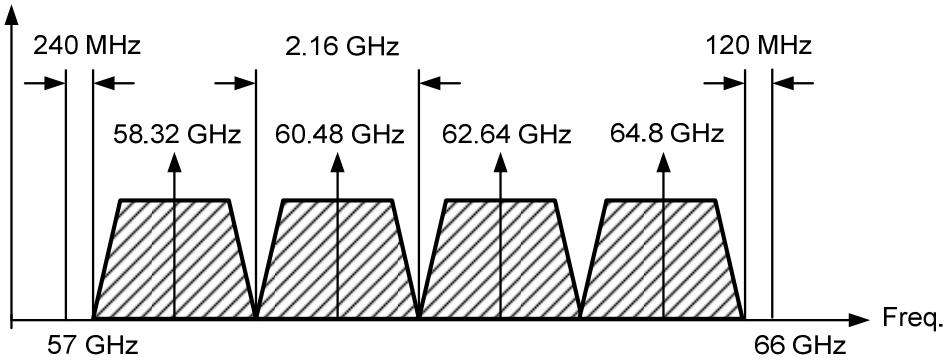


Figure 6.1 Spectrum and channel for 60 GHz application

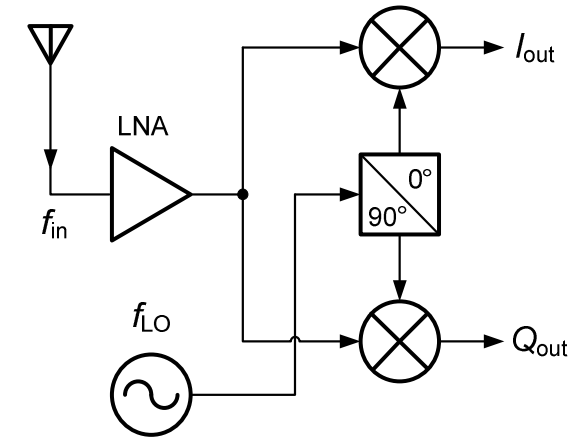
The whole spectrum is divided into four channels. The plan of the channel and carrier frequencies are summarized in Table 6.1 and illustrated in Figure 6.1. This solution provides four carriers for indoor short-range communication, which is enough in most conditions.

6.1. Frequency Plan

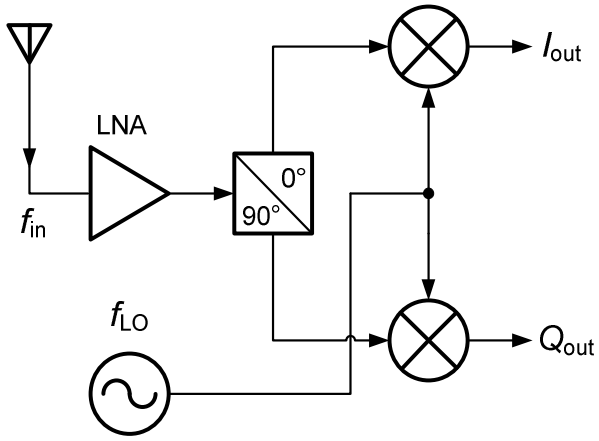
After fixing the communication channels for the 60 GHz application, the next question arises. How much is the LO frequency, and what does the transceiver look like?

In a conventional wireless transceiver, a frequency-programmable LO signal with good noise property is required. The choice of transceiver architecture affects the LO frequency and synthesizer design. Some design issues deserve careful consideration. Firstly, LO frequency directly determines the image frequency. High IF frequency is advantageous, making the image signal further away from the RF signal. It also facilitates the design of the image-filter. Furthermore, to achieve the complex modulation scheme in the baseband such as QPSK or OFDM, the generation of I/Q baseband signals are required. In the absence of I/Q baseband signals, the transceiver can only operate with amplitude-modulated signals. The I/Q signals could be generated at either the RF port or the LO port, which are both quite challenging. Therefore, the selection of LO frequency and transceiver architecture must consider carefully the image rejection, the synthesizer design and the generation of baseband I/Q signals.

Let's look first into the simple 60 GHz zero-IF architecture in Figure 6.2. Apart from the problem of DC-offset in all zero-IF transceivers, it is difficult to generate I/Q signals at 60 GHz, both at the LO port as shown in Figure 6.2 (a), and at the RF port as shown in Figure 6.2 (b). I/Q generation at such a high frequency result in great noises and large phase errors. And the distribution of the 60 GHz quadrature phase over a large layout also proves to be difficult. On the other hand, 60 GHz synthesizer design is a challenging task. The synthesizer design and I/Q generation could be made easier by opting for the super-heterodyne architecture.



(a)



(b)

Figure 6.2 Zero-IF architecture with I/Q generation at (a) LO port and (b) RF port

Figure 6.3 illustrates a universal case of a super-heterodyne receiver. This architecture can also be applied to the transmitter. With the LO signal at the frequency f_{LO} , the super-heterodyne architecture achieves the first down-conversion at $M \cdot f_{LO}$ and the second conversion at f_{LO}/N . Concludes that

$$f_{in} - M \cdot f_{LO} = f_{LO} / N \tag{6.1}$$

$$M \cdot f_{LO} - f_{img} = f_{LO} / N \tag{6.2}$$

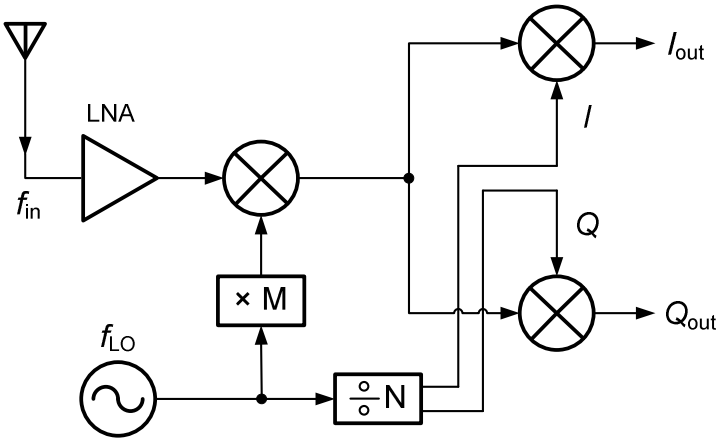


Figure 6.3 Super-heterodyne architecture

where f_{img} is the frequency of the image signal. The expressions of f_{LO} , f_{IF}, f_{img} are further derived as

$$f_{LO} = \frac{N}{1+MN} f_{in} \tag{6.3}$$

$$f_{IF} = \frac{1}{1+MN} f_{in} \tag{6.4}$$

$$f_{img} = \frac{MN-1}{MN+1} f_{in} \tag{6.5}$$

Based on real building blocks, the $\times M$ multiplier can be achieved by a doubler or tripler, while the $1/N$ cell could be several stage frequency dividers. Hence, the value of M might be 1, 2 or 3. N could be 2 or 4. More than two stage frequency dividers are unnecessary in practice, and they would increase the complexity of the system. The resulting possible frequency plans are summarized in Table 6.2. The analysis focuses on the highest and lowest RF frequencies, which are 66 GHz and 57 GHz respectively.

Table 6.2 Frequency plan for 60 GHz super-heterodyne transceiver

Plan	a	b	c	d	e	f
M	1	1	2	2	3	3
N	2	4	2	4	2	4
f_{in} (GHz)	57 66	57 66	57 66	57 66	57 66	57 66
f_{LO} (GHz)	38 44	45.6 52.8	22.8 26.4	25.3 29.3	16.28 18.86	17.5 20.3
f_{IF} (GHz)	19 22	11.4 13.2	11.4 13.2	6.3 7.3	8.1 9.4	4.38 5.08
f_{img} (GHz)	19 22	34.2 39.6	34.2 39.6	44.3 51.3	40.7 47.1	48.2 55.8

The work in [95] selects Plan ′e′ with M=3, N=2. With this configuration, the operation frequency range of the frequency synthesizer reduces to 16.2 – 18.8 GHz. Lower operation frequencies and narrower bandwidths make the design of the synthesizer easier. However, this plan suffers from a very low IF frequency. As discussed above, high f_{IF} indicates a great distance between f_{RF} and f_{LO}, simplifying the design of the image-filter. As we can see, the front-end has to accommodate the lowest RF signal at 57 GHz, at the same time attenuating the image signal at 47 GHz. It is very difficult to design the image-filter with a high Q-factor at such high frequencies. Concerning adequate image rejection, small M and small N are preferred. On the other hand, a tripler is required in Plan ′e′. The 60 GHz tripler is usually accompanied by additional phase noises, low output power and large power consumption. Actually, from the perspective of system cost, it is better to remove the $\times M$ cell.

When M equals 1, two choices exist for the value of N. Making comparison between Plan ′a′ and Plan ′b′, two advantages allow Plan ′a′ to succeed over Plan ′b′. Firstly, Plan ′a′ obviously has a much higher f_{IF}, which is good for image rejection. Moreover, Plan ′b′ requires an almost fundamental LO from 45.6 GHz to 52.8 GHz. Requiring a LO signal with higher operation frequencies and wider bandwidths than

Plan′a′, Plan′b′ certainly becomes a more difficult design. The only benefit of Plan′b′ might exist in the generation of I/Q signals at the LO port. Since there are two stage frequency dividers before the second mixer, I/Q signals of the second LO could easily be created through the second stage static frequency divider at around 12 GHz.

The other frequency plan is to employ a 30 GHz LO signal, which is at around half of the input frequency f_{in}. The resulting architecture is depicted in Figure 6.4. This approach incorporates the lowest f_{LO}, and places the image signal around zero frequency. Unfortunately, this architecture suffers from a third harmonics issue [96]. In other words, the signal at the third harmonics of f_{LO} would also be down-converted to the IF signal. Furthermore, since f_{LO} is equal to f_{IF}, the LO-IF feed-through of the first mixer might be extremely serious.

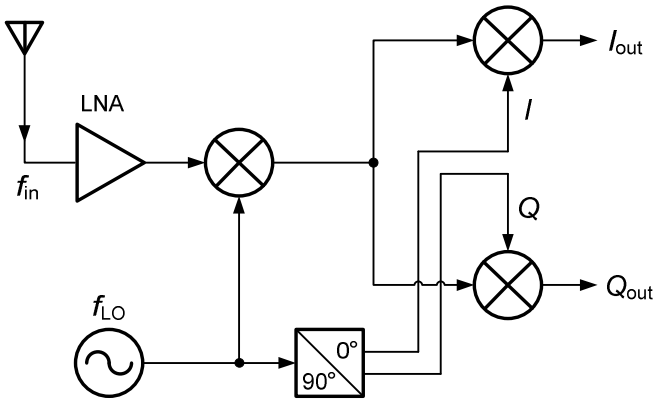


Figure 6.4 Super-heterodyne architecture with 30 GHz LO

Apart from the zero-IF and super-heterodyne architectures, another possible solution is the low-IF transceiver [97][98], as shown in Figure 6.5. The 60 GHz RF input is first converted to a low IF frequency (several GHz) by a single-carrier LO. The channel selection and I/Q generation could then be accomplished by the second LO. Since f_{IF} is as low as several GHz, the image signal is located in the band of RF signals. The in-band image noises generated by the antenna, LNA and mixer, increase the SNR of the receiver [96].

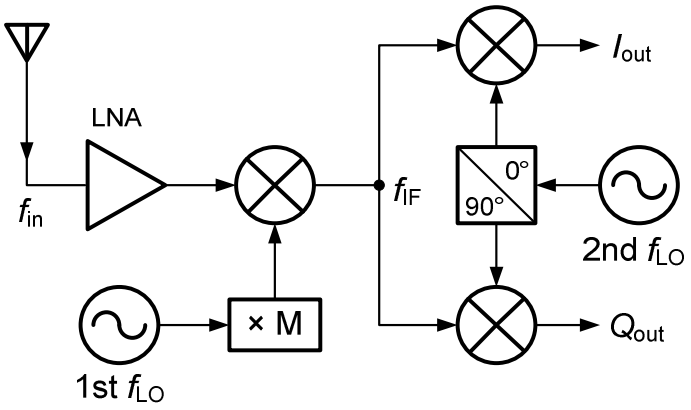


Figure 6.5 Low-IF transceiver

Based on the above analysis, the super-heterodyne transceiver architecture with Plan ′a′ is preferred in this work. Figure 6.6 illustrates the complete block diagram of the targeted transceiver for 60 GHz application.

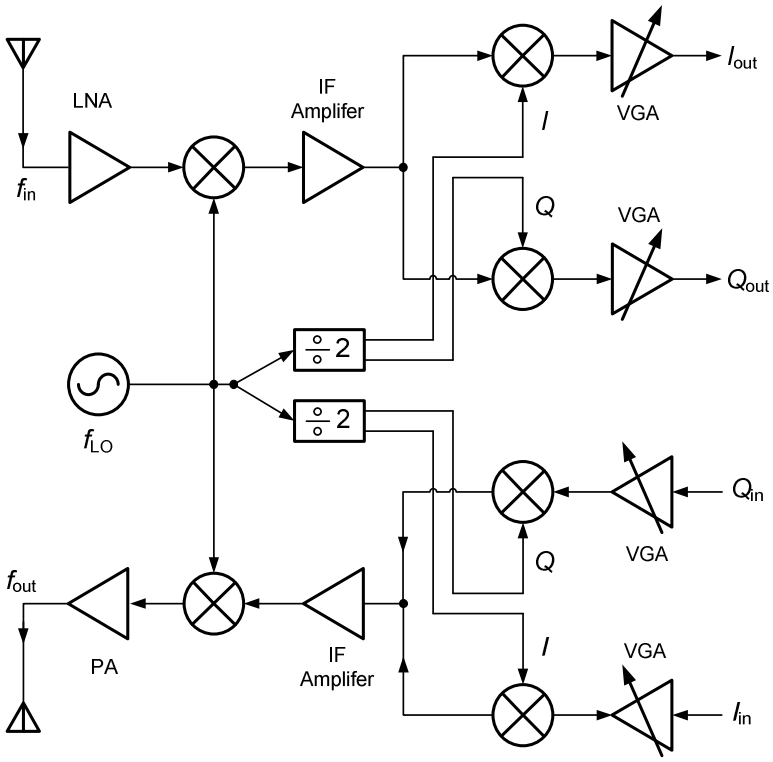


Figure 6.6 Targeted 60 GHz transceiver

It can be seen in Figure 6.6 that a one-stage amplifier operating at IF frequency is placed after the first mixer to improve the gain of the front-end. It also boosts the power of the IF signal for the operation of next stage mixer. The variant gain amplifier (VGA) is designed to ensure enough gain of the total link. Two identical 2:1 static dividers are used to generate I/Q signals of the second LO for the transmitter and the receiver respectively. According to the proposed spectrum and channels at 60 GHz in Table 6.1, the frequency plan for the targeted 60 GHz transceiver is summarized below.

Table 6.3 Frequency plan of targeted 60 GHz transceiver

	Channel 1	Channel 2	Channel 3	Channel 4
RF Bandwidth (GHz)	57.24 – 59.4	59.4 – 61.56	61.56 – 63.72	63.72 – 65.88
RF (GHz)	58.32	60.48	62.64	64.8
LO (GHz)	38.88	40.32	41.76	43.2
IF (GHz)	19.44	20.16	20.88	21.6

6.2. Synthesizer Architecture

PLL-based LO generation is indispensable in the wireless transceiver system. It should achieve accurate frequency synthesis for multiple LO carriers as well as a good noise property.

As the frequency becomes higher, the design of the frequency synthesizer encounters many challenges. To achieve frequency synthesis for multiple carriers, the VCO and whole frequency divider chain require a wideband operation. In the PLL loop, the operation range of each stage circuit is supposed to cover the operation range of the last stage. In other words, beginning from the VCO, the locking range of the next stage frequency divider has to cover the tuning range of the VCO. Meanwhile, each following stage divider is required to cover the locking range of the last stage divider. But, the operation frequency range of the VCO and frequency divider is quite

sensitive to parasitic elements and process variation at such high frequencies. Hence, in practice, it is very hard to achieve the correct and wideband operation for whole circuits. On the other hand, since the conventional programmable frequency divider is unable to operate in the mm-wave band, the feedback signal has to be divided firstly to the GHz frequency range, which could apply to the programmable divider. Consequently, the VCO's output signal must be divided by a large ratio, which could be even as large as one thousand. As a result, this large division ratio would lead to a great phase noise addition to the out-band phase noise of the synthesizer. Furthermore, because of the high frequency operation, the noise in the analog and digital circuit of the synthesizer is apt to couple to the high frequency circuits, thereby degrading the noise performance.

Confronted with so many design issues, the frequency synthesizer is no longer an indispensable building block in a mm-wave transceiver. In the low-IF receiver, the RF signal is converted first to a low IF frequency (several GHz) by a LO signal close to the fundamental frequency [97][98]. Channel selection is accomplished at the IF frequency. In this way, only a single LO frequency is required in the front-end circuit. The frequency synthesizer is replaced by a PLL circuit without the programmable divider. Meanwhile, since the synthesizer is locked to only one frequency point, the wideband operation of the VCO and the whole divider chain are not required. It would also reduce total power consumption. But this architecture may lead to an in-band image because of the low IF frequency.

Certainly, channel selection is always better at the RF frequency, since it simplifies the system complexity and reduces power consumption. To simplify the design, it is a better idea is to achieve the synthesizer at a relative lower frequency, then boost the frequency by some frequency multiplication technique. From recent published work, three general approaches have been applied to accomplish this idea.

In the [99][100][101], a push-push VCO is employed in the frequency synthesizer, as illustrated in Figure 6.7. Thanks to the frequency-double nature of the push-push VCO, the frequency synthesizer actually operates at half of the LO

frequency. However, the low output power of the push-push VCO creates difficulties for the design of LO distribution.

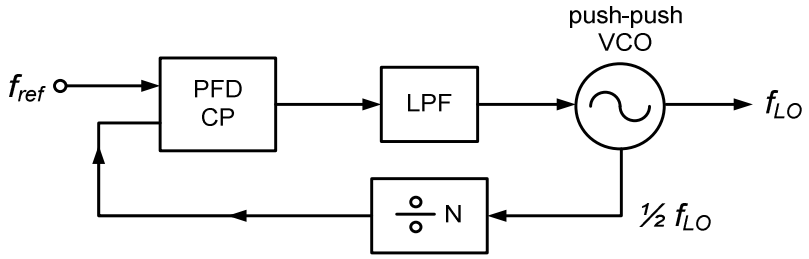


Figure 6.7 Frequency synthesizer with push-push VCO

Another way to multiply frequency is to use a doubler or a tripler following the frequency synthesizer [102][95]. The frequency synthesizer then operates at a much lower frequency than f_{LO} . The disadvantage of this approach stems from the design of the doubler or the tripler at mm-wave frequencies. They usually induce great attenuations and noises at such high frequencies, and dissipate too much dc power.

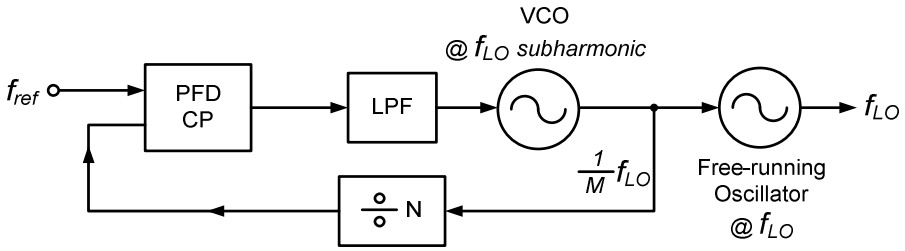


Figure 6.8 LO generation through injection locking technique

In chapter 4, the injection locking property of the oscillator is analyzed. This property could be used for mm-wave signal generation [103][104]. A frequency synthesizer operating at the sub-harmonic of the LO frequency would be achieved first. For example, for a 60 GHz LO, the sub-harmonic synthesizer could operate at 20 GHz or 30 GHz. The output of the sub-harmonic synthesizer is injected into a free-running oscillator operating close to the LO frequency f_{LO} . Using the injection

locking technique, the oscillation frequency of the free-running oscillator could be locked to f_{LO} and programmed by changing the frequency of the sub-harmonic synthesizer. This approach is illustrated in Figure 6.8. The difficulty of this architecture is in designing the injection locked oscillator. Its injection locking property would determine directly the bandwidth and noise of the LO signal. To improve the locking range, the quadrature phase of the sub-harmonic synthesizer might be required [104].

With the three techniques introduced above, the operation frequency of the synthesizer is reduced and design issues of the synthesizer design are alleviated. However, these three approaches all have disadvantages, which would worsen the performance of LO signal. As for the targeted 60 GHz transceiver, shown in Figure 6.6, it has a super-heterodyne architecture. The input 60 GHz signal will be converted to the baseband after two down-conversions. Channel selection must be achieved in the transceiver. In other words, LO generation should be capable of achieving the frequency-program. The frequency synthesizer is required to provide four carriers from 38.88 GHz to 43.2 GHz. The operation bandwidth is 10.5%, centered at 41 GHz. The design will be carried out using the TSMC 90 nm CMOS technology. 90 nm CMOS is an ideal process node for the design of 40 GHz circuits. The gain and operation speed of the 90 nm CMOS transistor are sufficiently competent for the design of a 40 GHz frequency synthesizer. On the other hand, the target of a 10.5% frequency range is also not beyond the capability. All in all, the planed frequency synthesizer will employ a fundamental VCO at around 40 GHz.

The corresponding division ratio and reference frequency could be derived, according to required RF resolution. For the targeted frequency plan, the relationship of the input frequency f_{RF} and the LO frequency f_{LO} is given as

$$f_{RF} = \frac{3}{2} \cdot f_{LO} \tag{6.6}$$

Because of the linear frequency synthesis, then

$$\Delta f_{RF} = \frac{3}{2} \cdot \Delta f_{LO} = \frac{3}{2} \cdot \Delta N \cdot f_{ref} \tag{6.7}$$

where f_{ref} is the reference frequency, and Δf_{RF} corresponds to the RF signal resolution. This is actually the channel spacing of the system, equal to 2.16 GHz in this design. Typically, the division resolution ΔN in a RF synthesizer is unity, which is achieved by an integer programmable divider. However, this architecture cannot be achieved at 40 GHz since the conventional programmable divider is unable to operate at mm-wave frequencies. In this work, the VCO's 40 GHz output will be delivered to a 32:1 divider chain. The frequency drops to around 1.25 GHz, which is appropriate for the programmable divider's operation. Consequently, the equation (5.7) changes to

$$\Delta f_{RF} = \frac{3}{2} \cdot \Delta f_{LO} = \frac{3}{2} \cdot 32 \cdot \Delta P \cdot f_{ref} = 2.16 GHz \tag{6.8}$$

$$\Delta P = 1 \text{, then } f_{ref} = 45\ MHz \tag{6.9}$$

ΔP corresponds to the step of an integer programmable divider. Based on the proposed architecture, the LO frequency f_{LO} is configured as

$$f_{LO} = 16 \cdot P \cdot f_{ref} = 16 \cdot P \cdot 45\ MHz \tag{6.10}$$

Targeting for the desired 4 carriers at 38.88 GHz, 40.32 GHz, 41.76 GHz and 43.2 GHz, the division ratio P of the programmable divider is supposed to be between 27 and 30. The complete plan for the frequency synthesis is summarized in Table 6.4. The total division ratio of the frequency synthesizer is achieved by a 32:1 frequency divider chain and a programmable divider with a division range of 27-30.

Table 6.4 Complete plan for frequency synthesis

	Channel 1	Channel 2	Channel 3	Channel 4
RF Bandwidth (GHz)	57.24 – 59.4	59.4 – 61.56	61.56 – 63.72	63.72 – 65.88
RF (GHz)	58.32	60.48	62.64	64.8
LO (GHz)	38.88	40.32	41.76	43.2
Total division ratio	32 × 27	32 × 28	32 × 29	32 × 30

Based on the above analysis, the 40 GHz synthesizer for the 60 GHz super-heterodyne transceiver is illustrated in Figure 6.9. In chapter 4 it was shown that the locking range of the frequency divider improves as the input power increases. A buffer tree will be designed to boost the power of the VCO's output, ensuring the correct operation and a wide locking range of the following frequency dividers. Meanwhile, this buffer tree also provides a very high isolation for the VCO, which prevents the following circuit from overloading the VCO. The 32:1 divider chain is composed of a one-stage ILFD at 40 GHz and 4-stage static frequency dividers. Since the ILFD has only a single-ended input, the other output of the buffer tree is delivered to a dummy ILFD. As a result, the symmetry of the layout is maintained. A simple buffer chain operating at around 1.25 GHz is added at the output of the 32:1 divider chain. It enables the measurement of the output of the divider chain. This design gives the opportunity to assess the performance of the whole divider chain. The loop filter is targeted to be off-chip. It would bring much more flexibility to the design and measurement of the loop property. To provide a reliable reference input, a simple divide-by-2 circuit is designed at the reference input. The frequency of the reference signal is 90 MHz in this work.

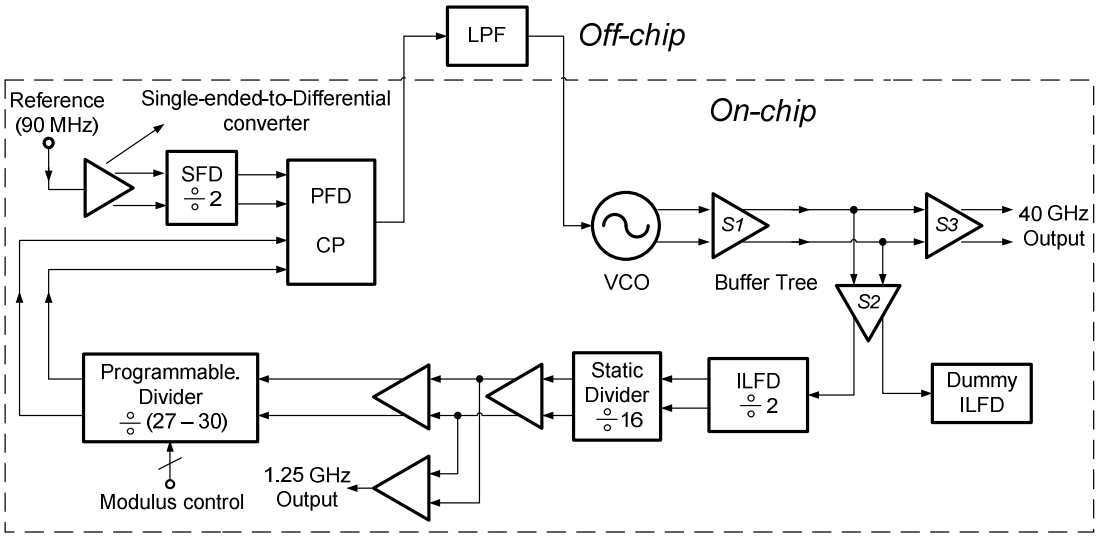


Figure 6.9 Block diagram of designed 40 GHz frequency synthesizer

The targeted 40 GHz frequency synthesizer will adopt the integer-N architecture. Recall the analysis of the fractional-N architecture in chapter 2. The fractional-N synthesizer is used widely to resolve the design issue of the integer-N architecture where the reference frequency must be identical to the channel spacing. Employing a fractional divider in the feedback loop, the reference frequency could be set much higher than the channel spacing. This modification decreases the total division ratio of frequency dividers, meanwhile making a large loop bandwidth possible. The decreased division ratio theoretically leads to a reduction of in-band phase noises, while a large loop bandwidth results in a fast loop settling. Turning to the targeted 40 GHz synthesizer, the situation is completely different. For the targeted frequency plan, the channel spacing is as high as 2.16 GHz. For the proposed synthesizer architecture, the reference frequency is much smaller than the channel spacing. The design of the loop bandwidth is not limited by the reference frequency. In addition, the fractional divider does not help to reduce the total division ratio. Therefore, the fractional-N architecture is not vital in the design of the mm-wave frequency synthesizer, which usually has a large RF resolution.

6.3. Circuit Design

6.3.1. Voltage Controlled Oscillator

As analyzed in chapter 3, the proposed VCO topology with resonated N-cell is able to improve the negative-conductance of the cross-couple transistors greatly. But unfortunately, it also induces considerable parasitic capacitance, which limits the frequency tuning range. To cover 10.5% tuning range from 38.88 GHz to 43.2 GHz, the classic cross-coupled topology is adopted for this design, due to its simple structure. On the other hand, the design procedure of the VCO with resonated N-cell is much more complicated than that of the classic topology. It would be easier to achieve expected results by designing a VCO with classic topology. Especially for mm-wave circuit design, the operation frequency is often shifted because of some unexpected effects.

Thus As can be seen in Figure 6.10, the NMOS cross-coupled pair is selected because of its higher gain compared with its PMOS counterpart. The accumulation-mod MOS varactor is employed for frequency tuning. A symmetric inductor with a center tap is designed as the tank inductor. Based on the approach proposed in chapter 3, the patterned dummy fills are placed inside the symmetric inductor to increase the metal density. Through the EM simulation of Ansoft HFSS, the symmetric inductor presents 250 pH inductances at 40 GHz with a Q-factor of 25. As analyzed in chapter 3, the mm-wave cross-coupled VCO suffers from severe AM-PM conversion. Hence, the flicker noise from the current source transistor would contribute considerable close-in phase noise. In this design, this effect is alleviated by replacing the current source transistor with a resistor.

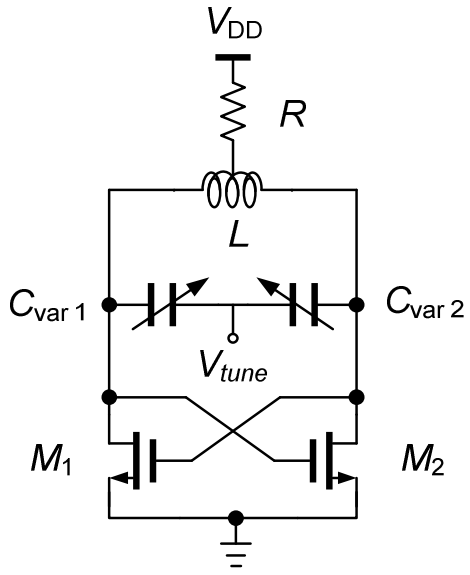


Figure 6.10 40 GHz VCO

Table 6.5 Design parameters of 40 GHz VCO

R	95 Ω
L	250 pH
Q (inductor)	25 @ 40 GHz
C_{var1}, C_{var2}	9 × 1.6 μm × 400 nm
Q (varactor)	12 @ 40 GHz
M_1, M_2	7 × 2 μm × 100 nm

The size of the inductor, varactor and cross-coupled transistors is carefully designed to achieve the specification of the phase noise and tuning range. In the TSMC CMN90 90 nm CMOS technology, the width and the length of a varactor are fixed. Only the number of the transistor fingers could be designed. To reduce the loss of the varactor and improve its Q-factor, it is designed with a multi-finger layout. In

the simulation, the *Q*-factor of the designed varactor is 12 at 40 GHz. Increasing the tuning voltage V_{tune} from 0 to 1.2 V, the VCO is oscillating from 36.8 GHz to 42.6 GHz. To isolate the VCO with the coupling noise from other circuit blocks, the bias of the VCO is supplied separately. With a 1.2 V supply voltage, the VCO dissipates 4.6 mA dc current. The detailed simulation and measurement results will be presented in Chapter 6.5.

6.3.2. VCO Buffer Tree

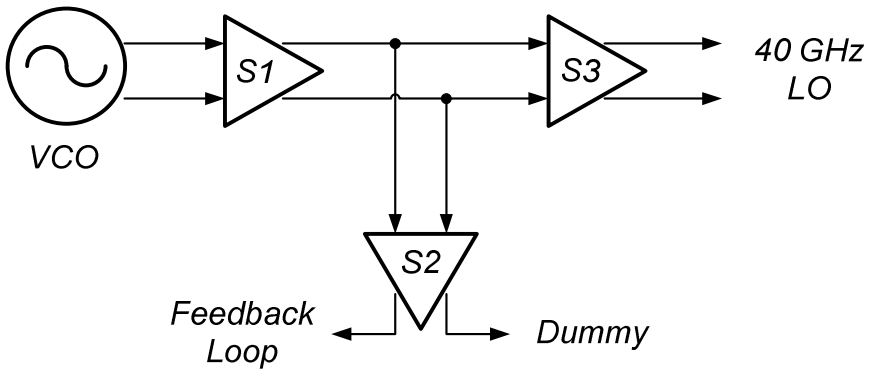


Figure 6.11 Block diagram of buffer tree

In practice, the VCO is supposed to deliver two outputs. One output is for the feedback loop of the frequency synthesizer, the other one goes to the transceiver. In order to provide a differential signal at both outputs, a VCO buffer tree is designed. On the other hand, it also helps to boost the signal power. It is of great significance since the correct operation of frequency dividers in the synthesizer and the mixer in the transceiver both require a high power LO signal. Its simplified block diagram is shown in Figure 6.11. All the amplifiers in the buffer tree are built with the cascode topology. The cascode topology could offer sufficient reverse isolation to the VCO, to ensure its stable operation.

The schematic and design parameters of the buffer tree are illustrated in Figure 6.12. All amplifiers are differential, but only the half-circuit is shown. The first stage buffer S1 employs a small size in order to prevent overloading the VCO. Following S1, two buffer amplifiers S2 and S3 have the same size, giving two

differential outputs. Buffer S3 is designed for outputs delivered to the transceiver. Its output impedance is matched to 50 Ω for measurement purposes. Another buffer S2 provides outputs for the 32:1 divider chain. Its output impedance is matched to the conjugate impedance of the ILFD's input impedance. Since the ILFD only has a single-ended input, another output of buffer S2 is connected to a dummy network which has the same impedance with the ILFD's input impedance.

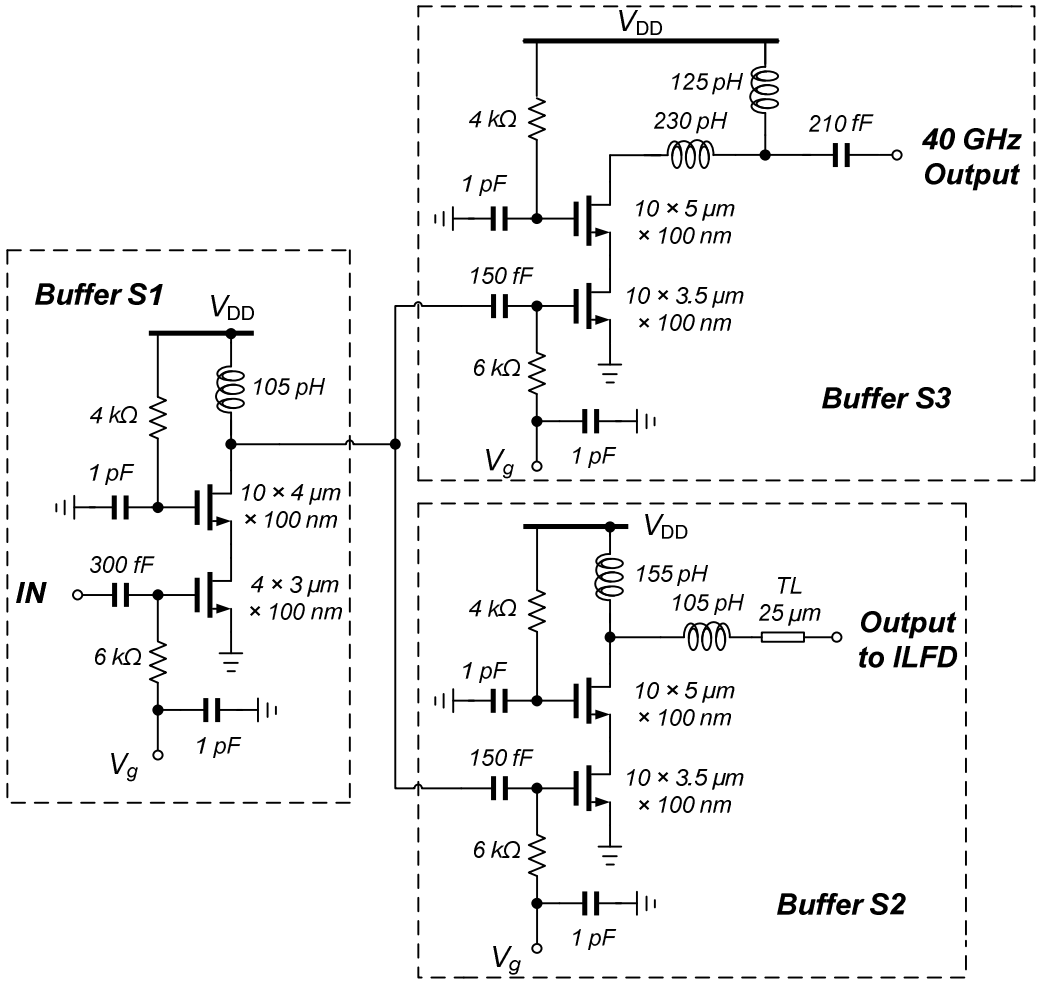


Figure 6.12 Half-circuit of the buffer tree

From past knowledge of this technology, the amplifier would experience a frequency shift to higher frequencies, when it is measured. Thus in the design phase, the peak of the output power is deliberately designed to be around 38 GHz. Hopefully

when it is measured, the operation bandwidth of this buffer tree is centered on 41 GHz. Meanwhile the maximum output power exists at around 40 GHz. The simulated performance of the designed buffer tree is characterized in Table 6.6. The simulated and measured output power will be presented in the following chapter.

Table 6.6 Simulated Performance of buffer tree

Power supply	1.2 V
Vg	0.75 V
Current consumption	4.5 mA (S1)
	12.5 mA (S2)
	12.5 mA (S3)
Output power (output of Buffer S3)	≥ -6 dBm

6.3.3. 32:1 Frequency Divider Chain

40 GHz injection locked frequency divider

The first stage frequency divider of the 32:1 divider chain is built as an injection locked frequency divider. At 40 GHz frequency range, the injection locked frequency divider achieves a good balance between the locking range and power consumption. Figure 6.13 shows the simplified schematic of the circuit. The bias circuit for the input transistor M_3 is not included here. It uses the topology of a direct injection locked divider. The input signal is injected directly into the oscillator core through the transistor M_3. The frequency of the output signal is locked at half the frequency of the input signal.

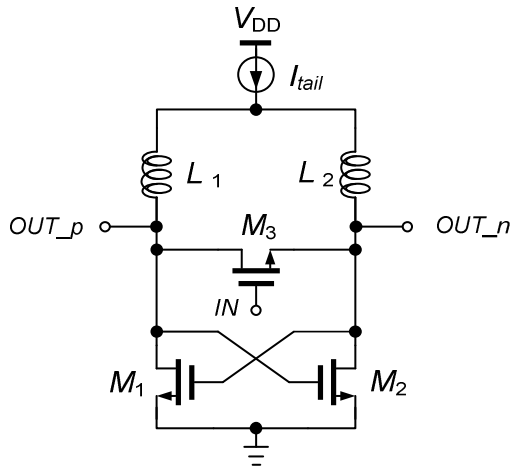


Figure 6.13 40 GHz ILFD

Table 6.7 Design parameters of 40 GHz ILFD

I_{tail}	3 mA
L_1, L_2	460 pH
Q-factor (inductor)	15 @ 40 GHz
M_3	7 × 2 μm × 100 nm
M_1, M_2	5 × 2.1 μm × 100 nm

The design begins with a free-running oscillator at 20 GHz. It has been proved that the wide locking range of the ILFD requires a large tank inductor with a low Q-factor [84]. From EM simulations, the tank inductors (L_1 and L_2) are 460 pH at 20 GHz with a Q-factor of 15. The choice of M_3 size is a compromise between the gain of the injection path and the induced parasitic elements. High injection gain requires a large M_3. However, its large parasitic capacitance would in turn attenuate

the injected power. By careful simulations, the size of M_3 is fixed at 14 μm / 100 nm. It is also biased with supply voltage V_{DD} for the highest gain.

4-stage static dividers

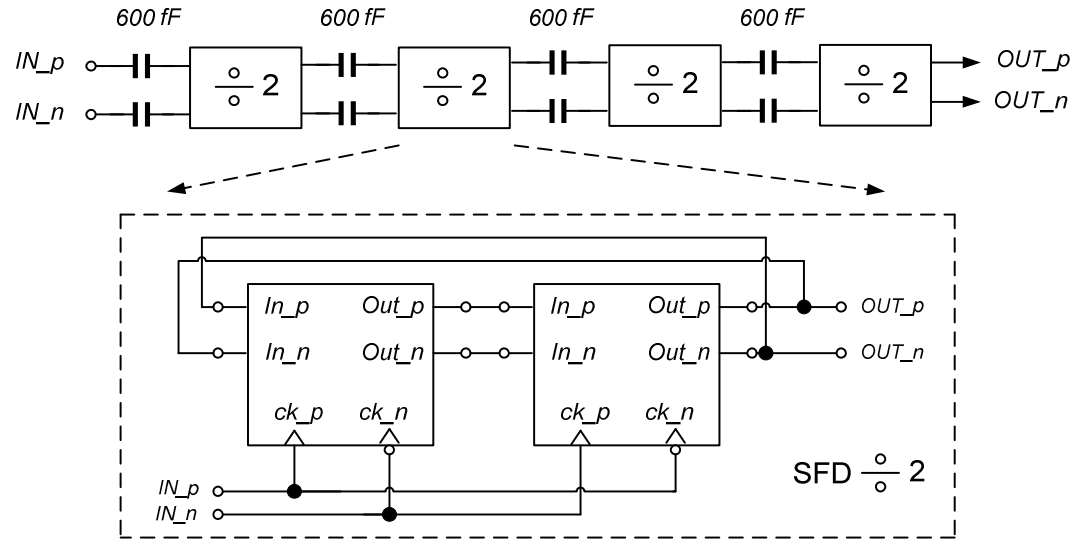


Figure 6.14 Block diagram of the 16:1 SFD

The 4-stage static frequency divider (SFD) follows the 40 GHz ILFD to achieve the division-by-16 from 20 GHz to 1.25 GHz. Each stage SFD is composed of two cascaded CML latches with a reversed feedback, as shown in Figure 6.14.

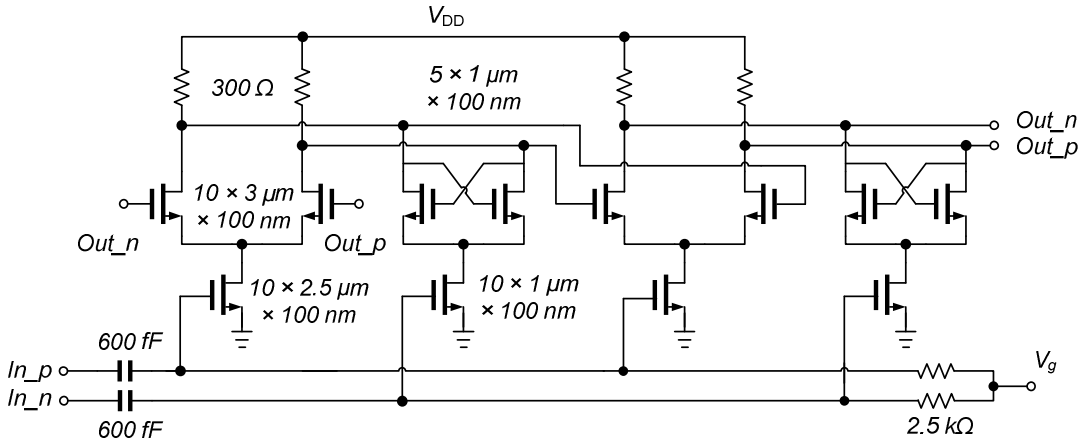


Figure 6.15 First stage static divider

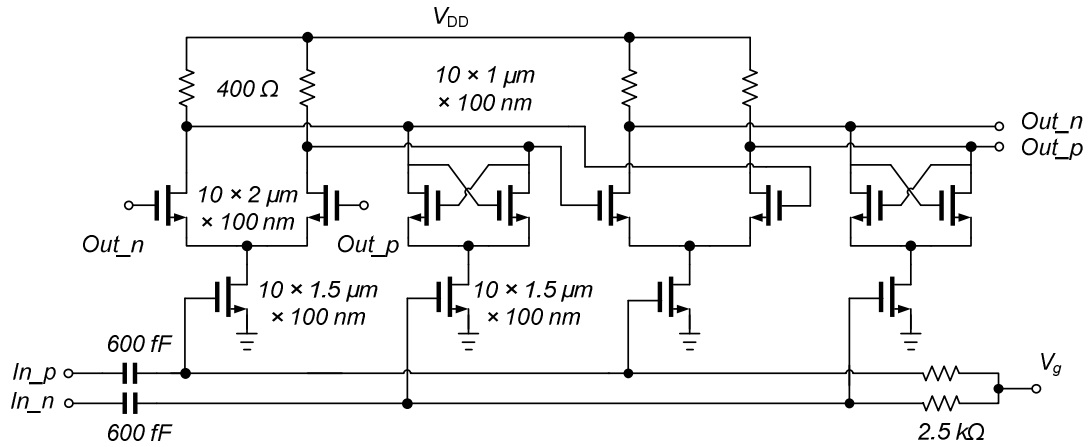


Figure 6.16 Second stage static divider

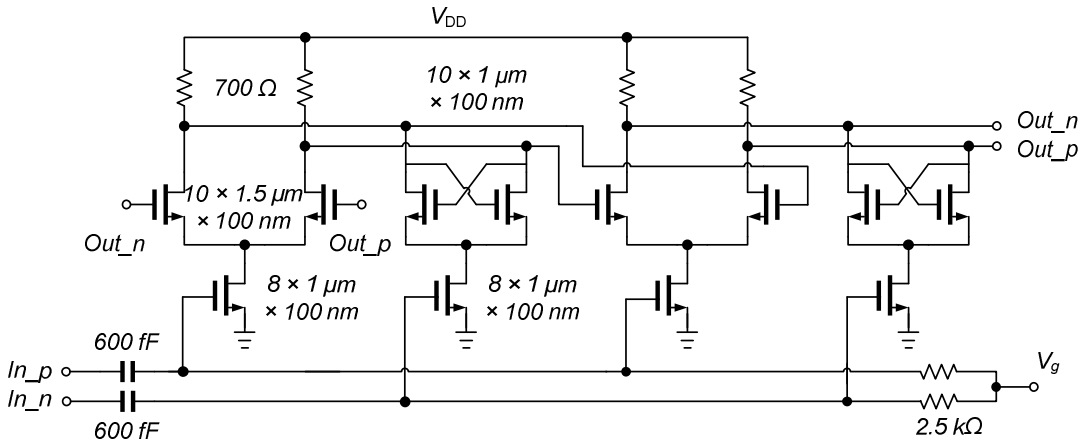


Figure 6.17 Third and fourth stage static divider

To speed up the operation of the latch, the current source transistor in the conventional CML latch is removed. This topology is usually called the 'class-AB' latch. It provides two upsides. Firstly, it saves voltage head-room under a 1.2 V supply voltage. Furthermore, the input transistors operate in a sort of class-AB mode, like the class-AB power amplifier. When the rising edge of the input signal comes, more current flows into the latch. It is helpful to speed up the switching operation of the latch. The four stage static dividers are shown respectively in Figure 6.15, Figure 6.16 and Figure 6.17. The power consumption of the each stage divider is scaled down with decreased operation frequency. Similarly, the size of active devices

is scaled up. They are designed with optimized power and bandwidth with respect to the corresponding operation frequency. After the second stage static divider, the operation frequency decreases to 5 GHz. The last two stage static dividers share the same design.

Simulated performance

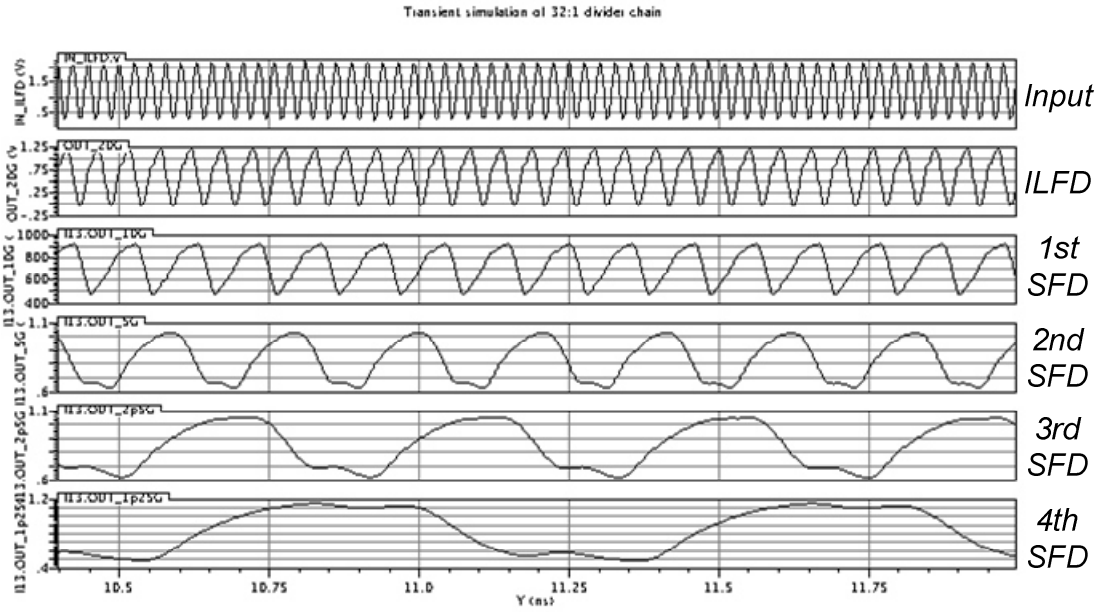


Figure 6.18 Simulated transient output of 32:1 frequency divider chain

The whole divider chain circuit is simulated with simulator goldengate in cadence. The interconnection wires in the layout have been EM-simulated with the Ansoft HFSS. By using the s-parameter data of these interconnection wires in the schematic design, the parasitic components of the layout were taken into account. This is of great importance to achieve the correct operation of frequency dividers in the interested band. Figure 6.18 shows the simulated output signal of each stage frequency divider. The power of the input signal is -2 dBm, which is the estimated output power of the VCO's buffer tree. Apparently, the function of the 32:1 frequency division is achieved. Its performance is summarized in Table 6.8.

Table 6.8 Performance summary of 32:1 divider chain

Power supply	1.2 V
Input power	-2 dBm
Current consumption	3.6 mA (ILFD)
	4.2 mA (1st stage SFD)
	3.4 mA (2nd stage SFD)
	1.7 mA (3rd, 4th stage SFD)
Locking range (40 GHz ILFD alone)	36 – 45 GHz
Locking range (32:1divider chain)	37 – 44 GHz

6.3.4. Programmable Divider

According to the above analysis of the synthesizer architecture, the programmable divider is required to provide an adjustable division ratio of 27 – 30. As briefly introduced in chapter 2, there are two approaches to constructing a programmable divider. One is based on the two-modulus prescaler, the other is built with multi-stage 2/3 divider cells. The conventional architecture, based on a two-modulus prescaler, is capable of achieving a wide continuous division range. But the price for this is complex architecture and high power consumption. In this case, since the whole spectrum includes 4 communication channels, the required division range is only 27 – 30, which is not wide. The programmable divider based on 2/3 divider cells is undoubtedly a superior choice over the conventional architecture. It has a simple and modular topology, employing the 2/3 divider cell as a standard building block. With careful design, it could achieve both high speed operation and low power consumption.

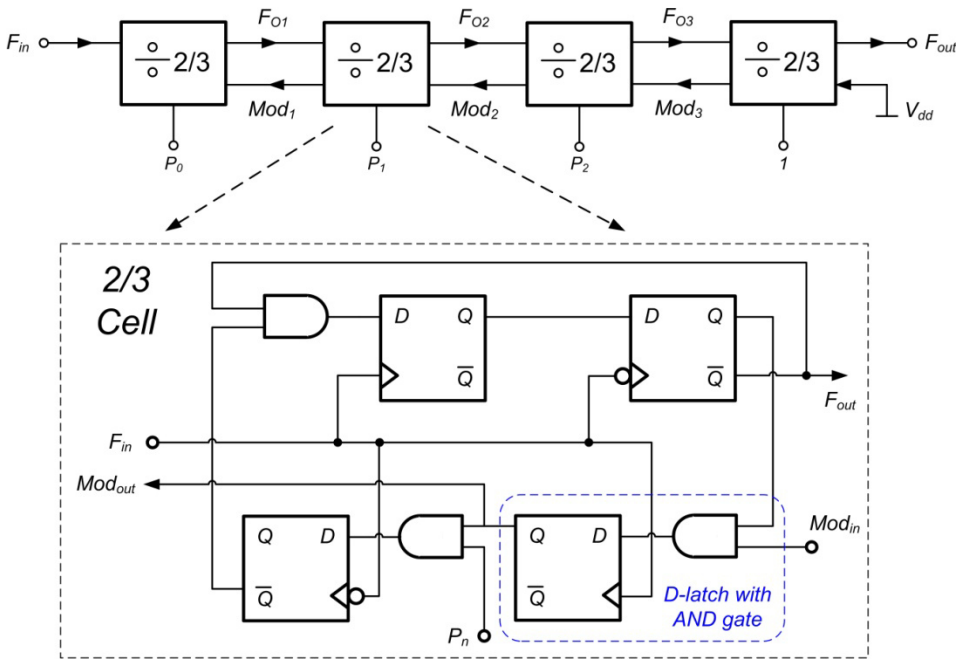


Figure 6.19 Block diagram of programmable divider

The proposed programmable divider based on the 2/3 divider cell is described in Figure 6.19. Programming the control bit of the 2/3 cells, the division ratio is determined by

$$N = 2^4 + 2^3 + P_2 \cdot 4 + P_1 \cdot 2 + P_0 \tag{6.11}$$

The desired LO frequency could be synthesized as in Table 6.9, corresponding to the programmed control bit P_0, P_1 and P_2.

Table 6.9 Programming of programmable divider

P_0	P_1	P_2	Division Ratio	LO Freq. (GHz)
1	1	0	27	38.88
0	0	1	28	40.32
1	0	1	29	41.76
0	1	1	30	43.2

The 2/3 cell is a frequency divider which can switch its division ratio between 2 and 3 according to the control input P_n. The block diagram of the 2/3 cell is shown in Figure 6.19. As we can see, when the P_n is set '1', the 2/3 cell operates as a

cascaded two-stage D-flipflops with a negative feedback, resulting in the divide-by-2 operation. If the P_n equals '0', the output stays at a high level for 3 periods of the input signal when a pulse comes at the Mod_n. For the design of the 2/3 cell, it could reuse the structure of the D-latch including a AND gate. The D-latch including the AND gate is the basic unit of the programmable divider. It is designed with a CML topology. The CML-based latch is better than the C^2MOS latch or TSPC latch, in both operation speed and noise property. Figure 6.20 presents the design of the D-latch including the AND gate. Resembling the 4-stage static divider, each stage 2/3 divider cell should be designed with optimized power and bandwidth because of different operation frequencies.

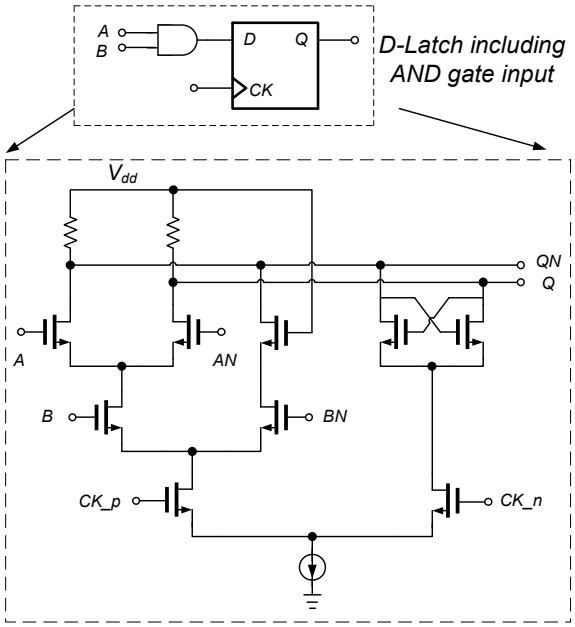


Figure 6.20 D-latch including AND gate

Table 6.10 Operating currents of each stage 2/3 divider cell

Block	DC Current
1st stage	1.111 mA
2nd stage	540 μA
3rd / 4th stage	430 μA

Figure 6.21 presents a simulated result of the designed programmable divider. The simulation is set up with a 1.5 GHz input signal. The control bit '$P_0P_1P_2$' of the programmable divider is given as '110' to realize the divide-by-27 operation. Let's examine the result following a reverse direction, from output to input. As can be seen, since the Mod_4 of the last stage 2/3 cell is set at '1', every period of the output signal

includes 3 pulses of the F_{o3}, which is the output signal of 3rd stage 2/3 cell. The 3rd 2/3 cell divides by 2 because the P_2 is '0'. In other words, every period of the F_{o3} comprises 2 F_{o2} periods. Then every period of the F_{out} comprises 6 periods of the F_{o2}. But for these 6 periods F_{o2}, 5 of them cover 2 F_{o1} pulses in one period, while the other one covers 3 F_{o1} pulses when Mod_2 is at a high level. As a result, these 6 F_{o2} pulses cover a total of 13 F_{o1} pulses. Similarly, the 13 F_{o1} pulses comprise 27 F_{in} pulses, which imply that the whole programmable divider achieves the divide-by-27 operation.

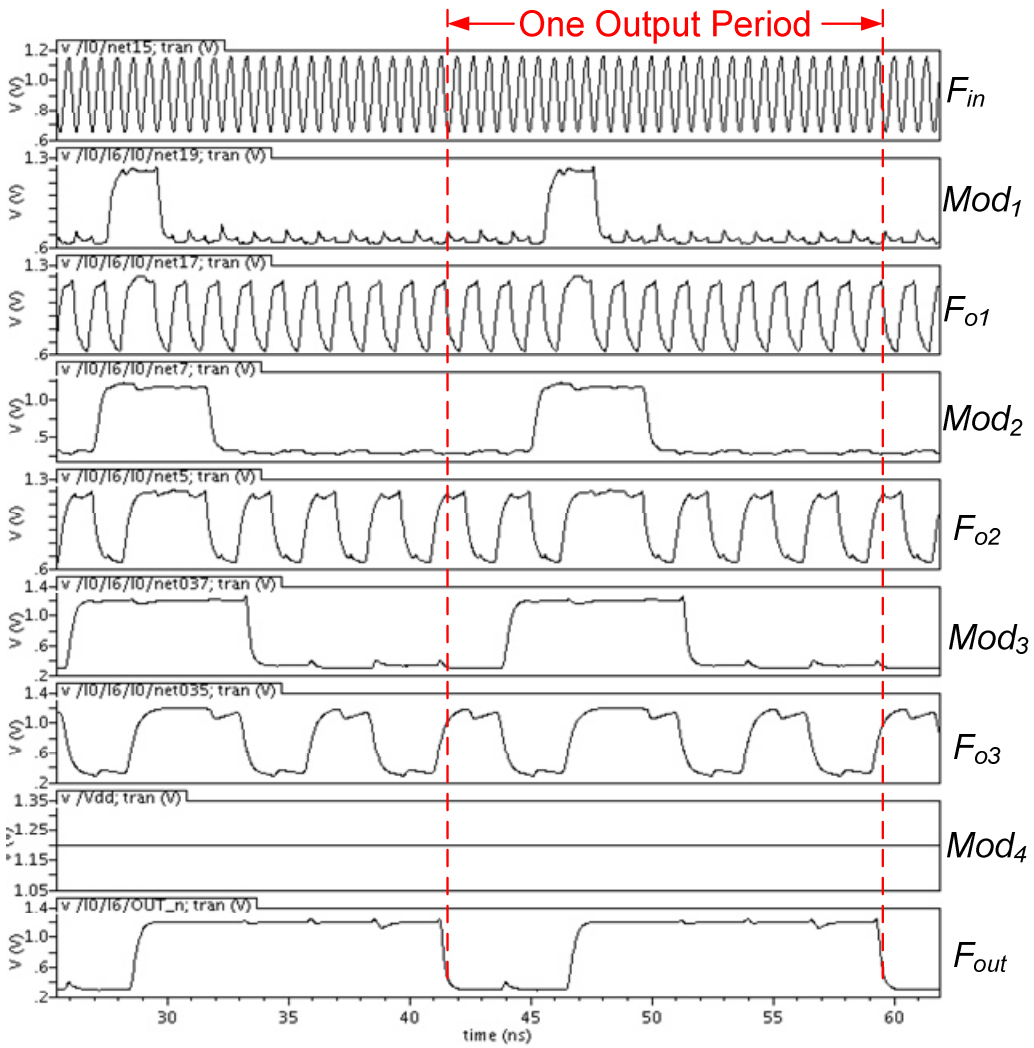


Figure 6.21 Simulation results of programmable divider

6.3.5. Buffer Chain for Divider Chain's Output

A buffer chain has been designed at the output of the 32:1 divider chain to increase the signal amplitude for driving the following circuits. In the meantime, a single-ended output is delivered to the pad for testing. With the measurement of this output, we could examine precisely the performance of the whole 32:1 frequency divider chain. Figure 6.22 shows its block diagram and schematics.

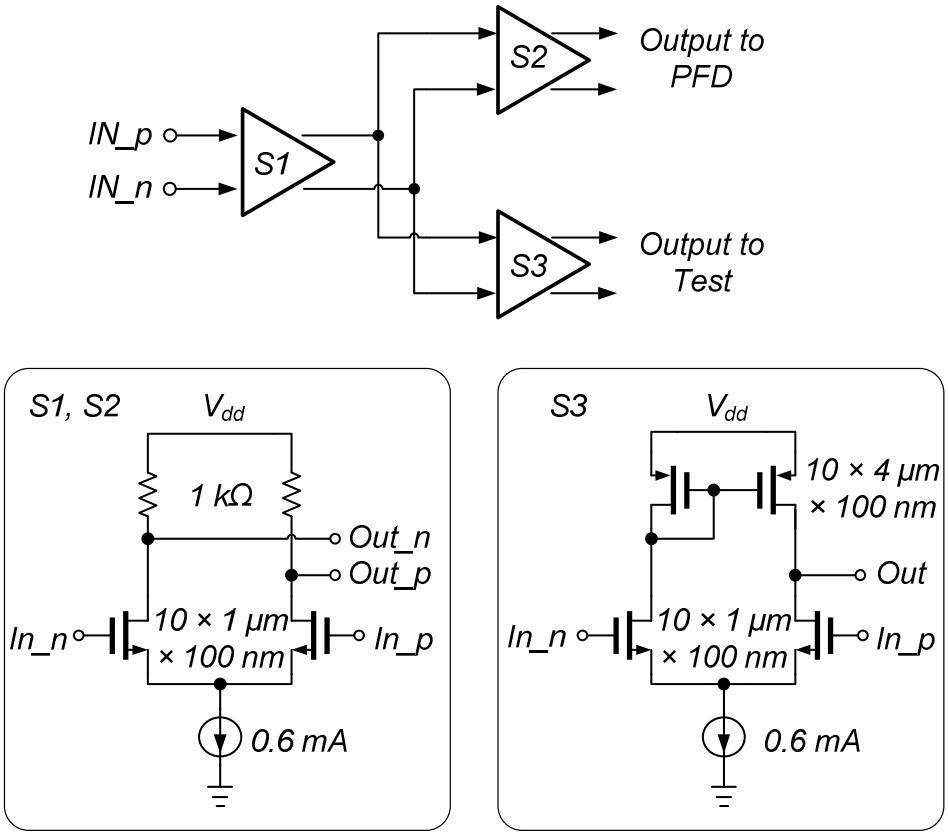


Figure 6.22 Buffer chain at output of 32:1 divider chain

To prevent overloading the last stage SFD, the buffer S1 is connected to the static divider alone. Following S1, an identical buffer S2 delivers the signal to drive the circuits which follow. Buffer S3 employs an active current mirror as a load to achieve the differential-to-single-ended function. Its output connects to the pad for testing.

6.3.6. Phase Frequency Detector and Charge Pump

Phase Frequency Detector

Through the PFD, the phase and frequency of the reference signal and the divided signal are compared, outputting the pulse signal 'Up' and 'Down' to control the switches in the charge pump. Figure 6.23 shows the diagram of the designed PFD. The main design issue is the dead zoom of PFD. As analyzed in chapter 2, the dead zoom could be narrowed by increasing the delay of the PFD's reset path. Two stage inverters are placed in the reset path to increase the delay. Consequently, the pulse width of the output signal is extended. In the simulation, if input signals are two in-phase signals at a same frequency, two overlapped pulse signal would be generated at the output with the pulse width of 1 ns. But at the same time, the phase detect range is reduced. In the simulation, the PFD presents a phase detect range of [-1.95π, 1.95π].

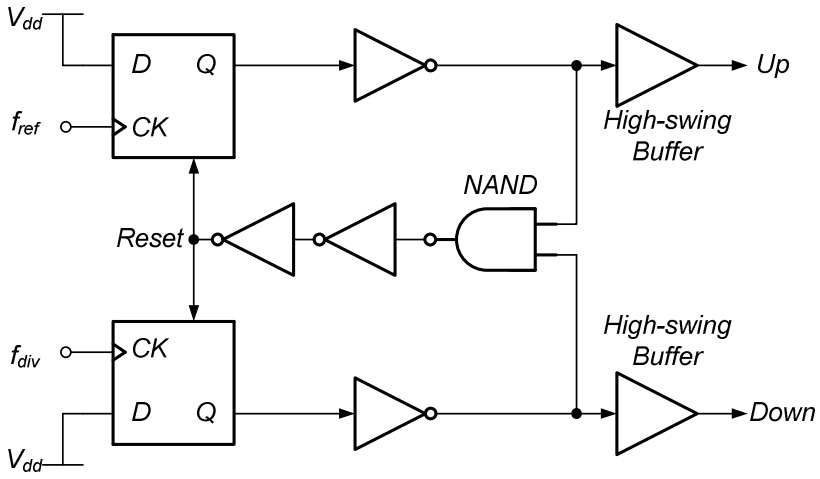


Figure 6.23 Diagram of the PFD

Similar to the programmable divider, circuit blocks of the PFD also have a differential CML topology for high-speed operation and low power consumption. Figure 6.24 shows the design of an edge-triggered D-flipflop with the reset function. It is the main building block of the PFD. In theory, the PFD operates at 90 MHz. Taking the layout parasitic element into account, the PFD is optimized to be able to

operate up to 500 MHz in the schematic design. Its function is finally verified in the post-layout simulation.

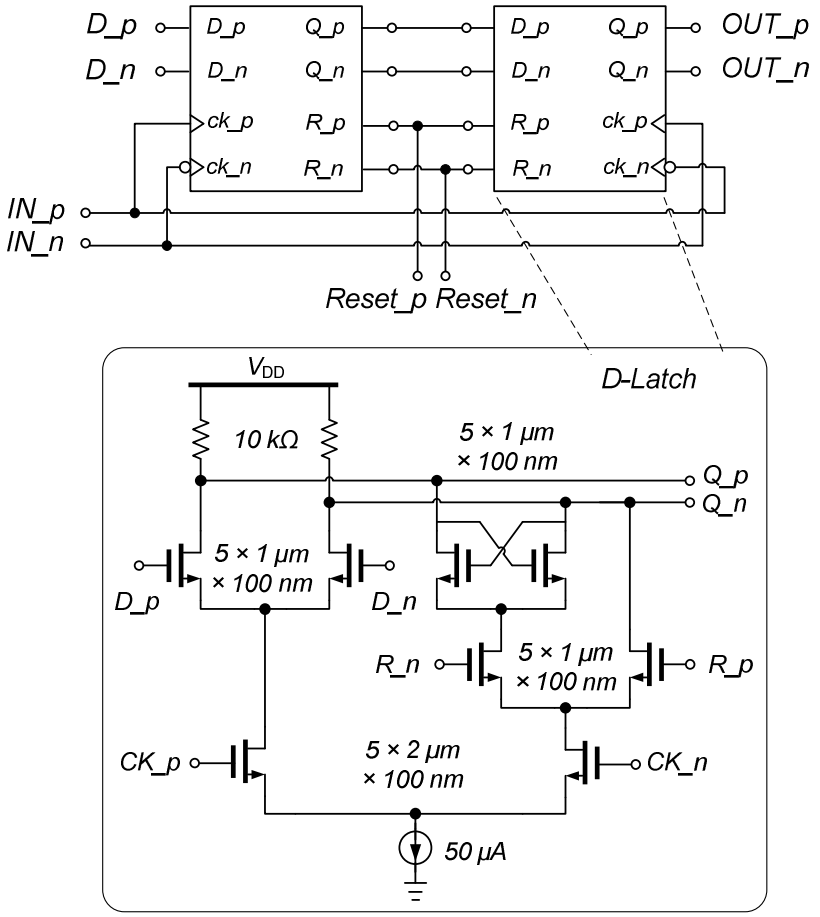


Figure 6.24 D-latch with reset function

Another interesting design in the PFD is a high-swing buffer at the output of the PFD. It is used to achieve the tail-to-tail high-swing signal as the output. It is of great importance for the high-speed operation of the switches in the charge pump circuit. High-speed switching operation leads to small ripples on the control line of the VCO, and further small spurious components. Figure 6.25 displays the design of the high-swing buffer. It has two stages. The first stage is a differential source follower. The differential output of the first stage is delivered to two PMOS differential amplifiers at the same time. The second stage PMOS amplifier employs the NMOS current-mirror ($M_{12\text{-}15}$) as the load to achieve the differential-to-single-

ended function. As a result, the second stage PMOS amplifier has only one output signal. Two PMOS amplifiers together provide a differential tail-to-tail output. In the simulation, it achieves a large voltage amplitude from 0 to 1.1 V.

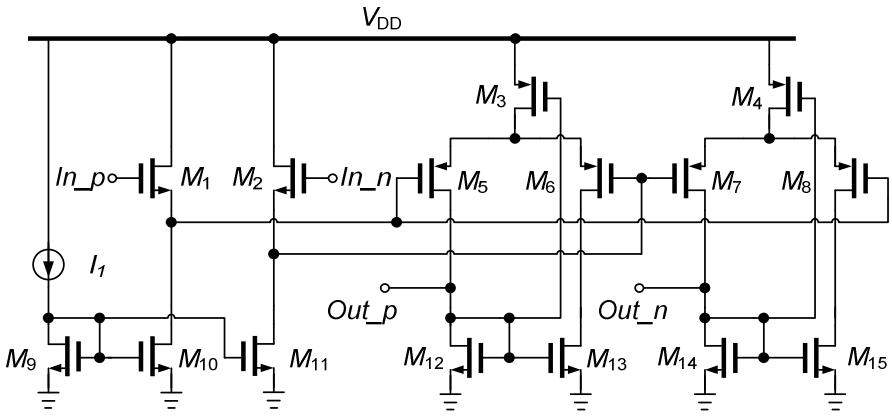


Figure 6.25 PFD high-swing Buffer

Table 6.11 Design parameter of devices in high-swing buffer

Component	Size	Component	Size
$M_{1\text{-}2}$	10 × 1.2 µm × 100 nm	$M_{12\text{-}15}$	2 × 2 µm × 500 nm
$M_{3\text{-}4}$	8 × 2 µm × 500 nm	$M_{9\text{-}11}$	2 × 2 µm × 500 nm
$M_{5\text{-}8}$	10 × 1.6 µm × 100 nm	I_1	50 µA

Charge pump

Driven by the pulse signal from the PFD, the charge pump circuit pumps the current into or out of the LPF, generating the control voltage of the VCO. Figure 6.26 shows the designed charge pump circuit. It is based on the source coupled logic (SCL) topology. Two SCL input pairs ($M_{16\text{-}17}$, $M_{18\text{-}19}$) are driven separately by the differential 'Up' and 'Down' signal. The output is generated through a common-source common-gate current mirror ($M_{11\text{-}12}$, $M_{28\text{-}29}$). A small current mirror composed of M_{24}, M_{25} (M_{26}, M_{27}) is designed to inject a small current to the PMOS current mirror M_{20}, M_{21} (M_{22}, M_{23}). It could help to raise the potential at the gate of M_{20}, M_{23}

when the SCL input pair switches on. Consequently, the operation of the SCL input differential pair is speeded up. The current of the charge pump is 50 μA, which is set after considering the whole loop performance. The transistors M_9 and M_{14} are used as the MOS capacitor to filter the coupling noises from the bias circuit. As we know, the current mismatch is the most important design issue for the charge pump circuit. The designed charge pump circuit has a fully symmetric architecture, which is good at suppressing the current mismatch. At the same time, the 'common-centroid' layout was designed for both current mirrors and input different pairs. Especially for the current mirror, a 'common-centroid' configuration of the layout is indispensable to diminish the current mismatch, since it reduces significantly the negative influence caused by process variations [18].

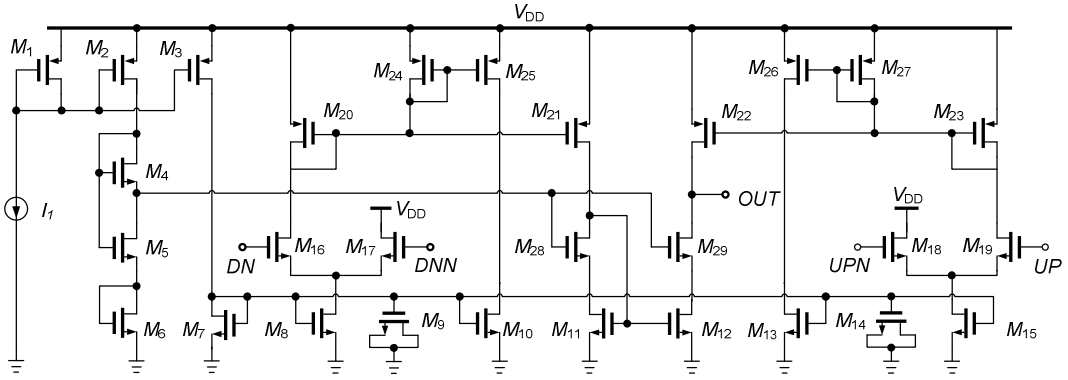


Figure 6.26 Charge pump circuit

Table 6.12 Design parameter of devices in charge pump

Component	Size	Component	Size
M_1	10 × 4 μm × 1 μm	$M_{11\text{-}12}$	3 × 1.5 μm × 100 nm
$M_{2\text{-}3}$	6 × 4 μm × 1 μm	$M_{16\text{-}19}$	8 × 1 μm × 100 nm
M_4	20 × 4 μm × 1 μm	$M_{20\text{-}23}$	4 × 2 μm × 100 nm
$M_{5\text{-}6}$	2 × 4 μm × 1 μm	$M_{25\text{-}26}$	8 × 3 μm × 1 μm
$M_{7\text{-}8}$, M_{15}	4 × 3 μm × 1 μm	M_{24}, M_{27}	2 × 3 μm × 1 μm
M_{10}, M_{13}	2 × 3 μm × 1 μm	$M_{28\text{-}29}$	4 × 1.5 μm × 100 nm
I_1	50 μA		

Figure 6.27 illustrates a transient simulation result of the PFD and charge pump. The 100 MHz reference signal and feedback signal are given as input. They have a 0.4π phase difference. The generated 'Up' and 'Down' signals are shown, which will control the operation of switches in the charge pump. In this simulation, a 50 pF capacitor is added at the output of the charge pump to generate the control voltage V_{cont} of the VCO. Thanks to the high-swing buffer at PFD output, the output signal achieves a large voltage amplitude from 0 to 1.1 V.

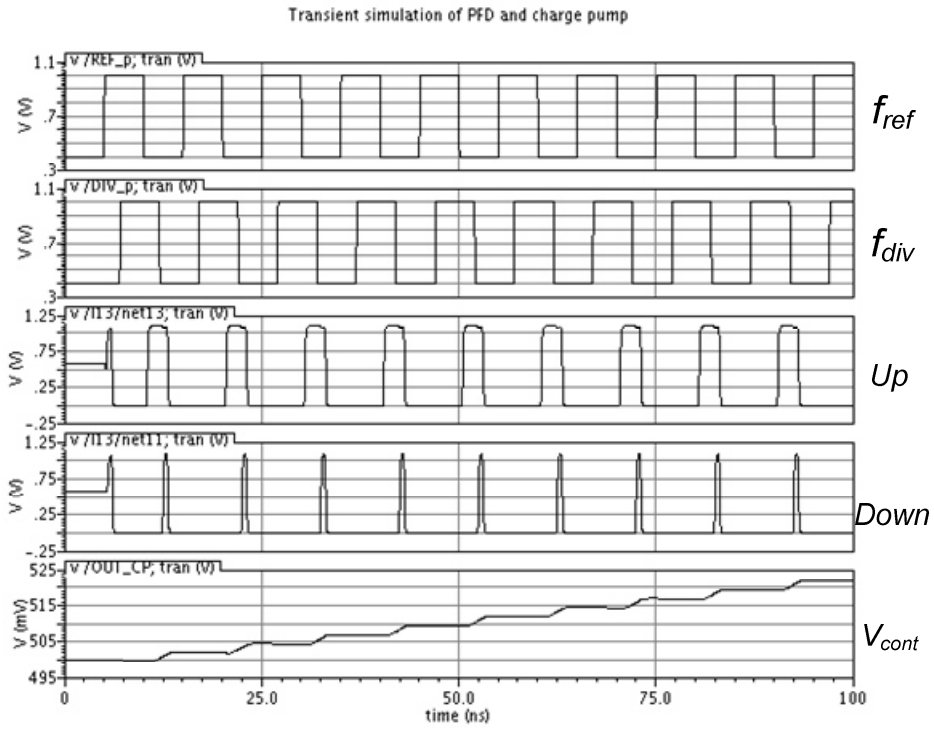


Figure 6.27 Transient simulation of PFD and charge pump

6.4. Design of Loop Performance

The frequency synthesizer's loop performance is of great importance since it is a closed-loop feedback system. As analyzed in chapter 2, the loop performance concerns three aspects: stability, transient response and noise property. Stability is the primary concern, which is mainly assessed by the phase margin of the open-loop gain. After the design of each circuit block, the total output phase noise of the frequency synthesizer is only affected by the loop bandwidth. The loop bandwidth would determine the on-band and in-band phase noise contributions from each block. The loop transient response is related to the bandwidth and the damping factor of the closed-loop gain. For the targeted 60 GHz application, the stability and noise property are the two primary considerations.

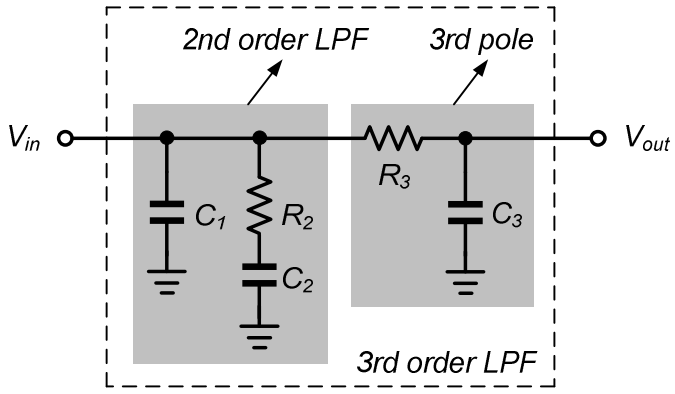
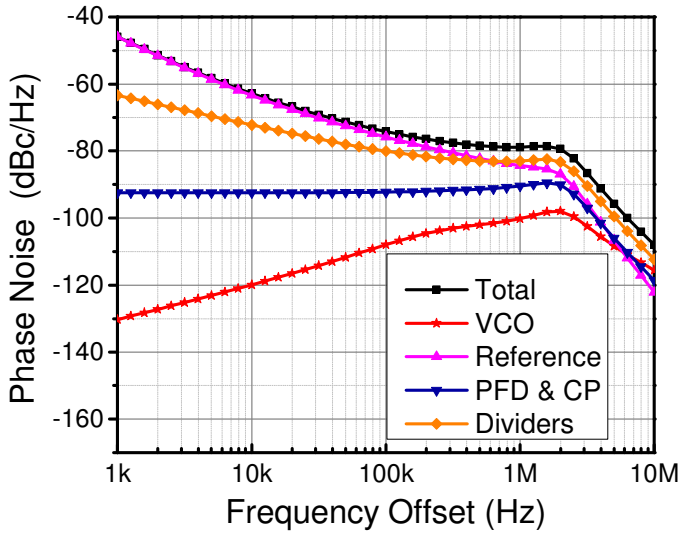


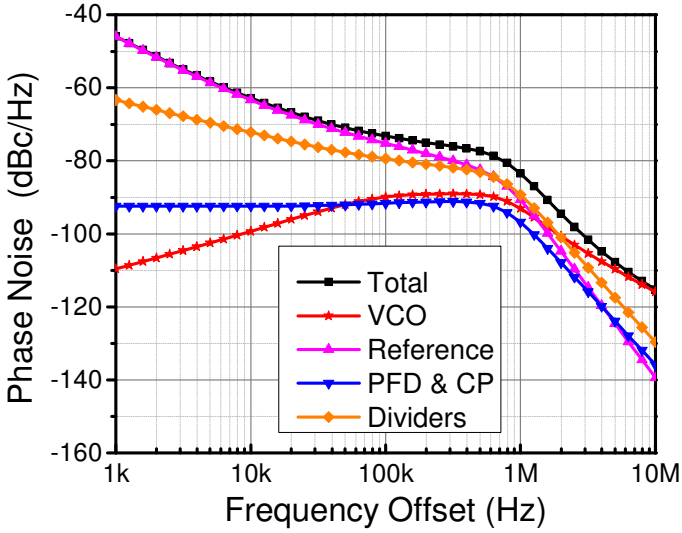
Figure 6.28 3rd order LPF

As shown in Figure 6.28, the 3rd order LPF is preferred to suppress the reference spur. The 3rd order LPF is composed of a 2nd order LPF with an additional 3rd pole. The small-signal phase domain model of the frequency synthesizer is built in the simulator ADS to perform the loop simulation. The model parameters of each circuit are attained from the simulation results of the transistor-level circuit. The design procedure starts with the 2nd order LPF design. Firstly, using the approach introduced in chapter 2, the value of C_1, C_2 and R_2 are calculated with respect to the desired 60º phase margin and the specified open-loop bandwidth. The designed 2nd

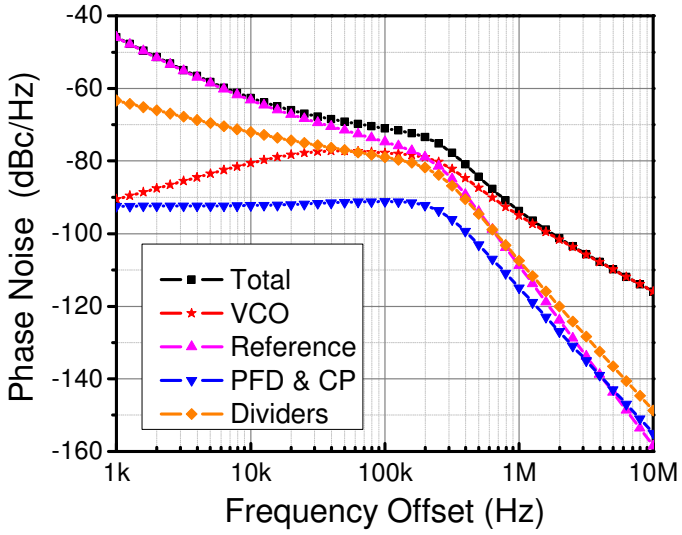
order LPF will be checked by ADS, to ensure loop stability. For the loop noise property, the phase noise performance of each block is first characterized by simulations of transistor-level circuits. Then the total output phase noise and phase noise contribution from each block are simulated and examined. In the design phase, various open-loop bandwidths (100 kHz, 300 kHz, 500 kHz, 1 MHz and 3 MHz) are designed with the identical 60º phase margin. The corresponding loop phase noise performances are simulated and compared.



(a) **1 MHz open-loop bandwidth**



(b) 300 kHz open-loop bandwidth



(c) 100 kHz open-loop bandwidth

Figure 6.29 Simulation of phase noise contribution from each blocks with different loop bandwidth

The loop phase noise simulation has been carried out with different open-loop bandwidths. Figure 6.29 shows the results for three different loop bandwidths, 1 MHz, 300 kHz and 100 kHz respectively. For each result, the total output phase noise and the phase noise contribution from each block (VCO, dividers, reference, PFD and charge pump) in the synthesizer are presented. A very important finding is that the noise contribution from the reference and dividers dominate the total phase noise. Essentially, it is distinct from the condition in the RF frequency range.

For the RF synthesizer, the phase noise contribution from the VCO is much larger than the contribution from the other blocks. Since the VCO contributes mainly to the out-band phase noise, it is better to design a large loop bandwidth for the RF synthesizer. At a frequency offset smaller than the loop bandwidth, the output would present a low phase noise. However, as for the mm-wave synthesizer, the in-band phase noise is no longer low. Firstly, the frequency dividers in the mm-wave synthesizer naturally have a poorer noise property than RF dividers. They operate at much higher frequencies. To reduce the power consumption, the multi-stage divider chain must employ the asynchronous architecture, in which jitter accumulates.

Moreover, when the noises of the reference and dividers contribute to the in-band phase noise, they would suffer from a noise addition. For our design, this noise addition is approximately equal to

$$20 \log N = 20 \log 960 \approx 60\ dB$$

where N is the total division ratio of the frequency synthesizer. This is a huge noise addition, which makes the in-band phase noise dominate the total output phase noise. The frequency divider and reference have become the primary noise sources in a mm-wave synthesizer.

Let's return to the results shown in Figure 6.29. Three different LPF designs all result in a 60° phase margin of the open-loop gain to ensure stability. The simulation was carried out for synthesizer performance at around 39 GHz. As we can see in Figure 6.29 (a), with 1 MHz open-loop bandwidth, the output phase noise at 1 MHz frequency offset is totally dominated by the in-band phase noise. Since a large loop bandwidth is employed, the phase noise contribution from the VCO is suppressed and is much less than that from the reference and dividers. Concerning the 1 MHz offset, -78 dBc/Hz phase noise is attained. Normally, the closed-loop bandwidth is slightly larger than the open-loop bandwidth. It can be observed in Figure 6.29 (a), that the closed-loop bandwidth is approximately 2 MHz.

As for the results shown in Figure 6.29 (b), a LPF with 300 kHz open-loop bandwidth is designed for the simulation. The in-band phase noise is restrained to some extent. But it is still higher than the phase noise contribution from the VCO. The simulation shows that the total output phase noise is -84 dBc/Hz at 1 MHz offset. The closed-loop bandwidth is roughly 500 kHz. When the open-loop bandwidth shrinks to 100 kHz, the phase noise contribution from the VCO starts to dominate the total phase noise. As shown in Figure 6.29 (c), a closed-loop bandwidth of about 200 kHz is observed. Beyond the closed-loop bandwidth, the total phase noise decreases dramatically following the VCO's phase noise characteristics. -94 dBc/Hz phase noise is achieved at 1 MHz frequency offset. All in all, a small loop bandwidth is required for good output phase noise. The same conclusion has also been drawn in Ref.[105].

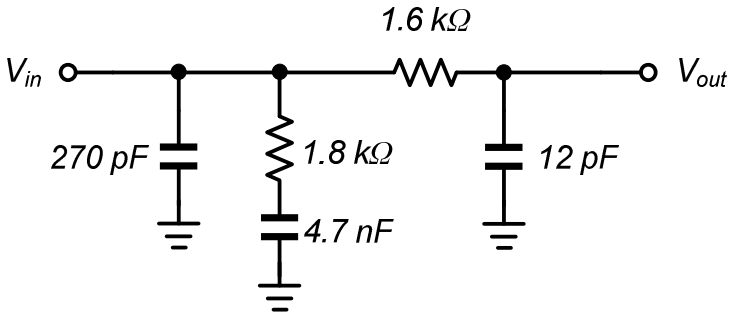


Figure 6.30 Design of 3rd-order LPF

After the value of C_1, C_2 and R_2 is fixed for best phase noise performance, the 3rd pole provided by R_3 and C_3 has to be designed further. Following the rule of thumb, the designed 3rd pole is greater than 10 times the 2nd pole. As a result, the change of the phase margin and loop bandwidth caused by the 3rd pole could be negligible. The final parameter of the 3rd-order LPF is displayed in Figure 6.30. The open-loop bandwidth is about 100 kHz. According to the equation (2.46), about 20 dB attenuations to the reference spur would be achieved by adding the 3rd pole.

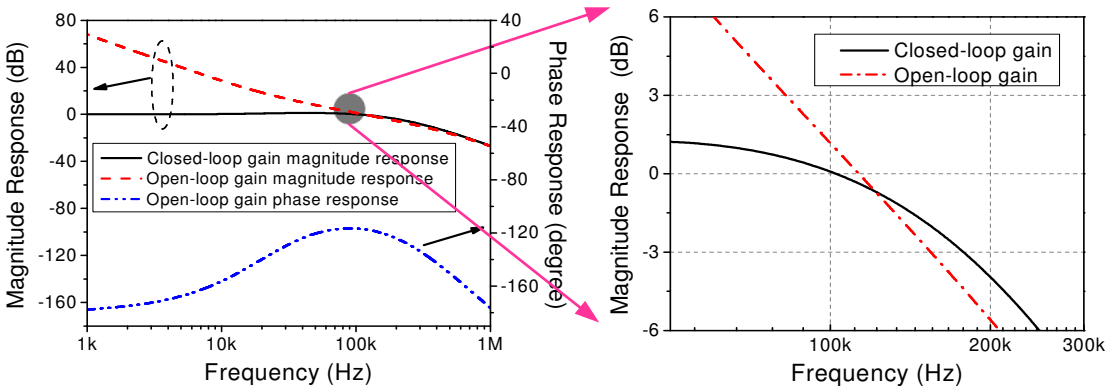


Figure 6.31 Loop stability simulation with 100 kHz open-loop bandwidth

Finally, the loop stability must be re-checked. Figure 6.31 shows the small-signal simulation results of open-loop and closed-loop responses. It can be seen from Figure 6.31 (a) that at the open-loop gain cross-over, the open-loop phase response is

about -120°, which indicates a 60° phase margin. Figure 6.31 (b) zooms in the magnitude response results around gain cross-over. As we can see, the resulting open-loop bandwidth is about 110 kHz, and -3 dB closed-loop bandwidth is approximately equal to 180 kHz. As a small loop bandwidth is designed, the loop would experience a long-time transient response. The simulated settling time for the phase locking could be as long as 100 μs.

6.5. Measurement and Discussion

The 40 GHz frequency synthesizer chip is fabricated in TSMC 90 nm CMOS technology. The micrograph of the chip is shown in Figure 6.32. It has an area of 0.95 $\times$0.85 mm^2 including all the pads.

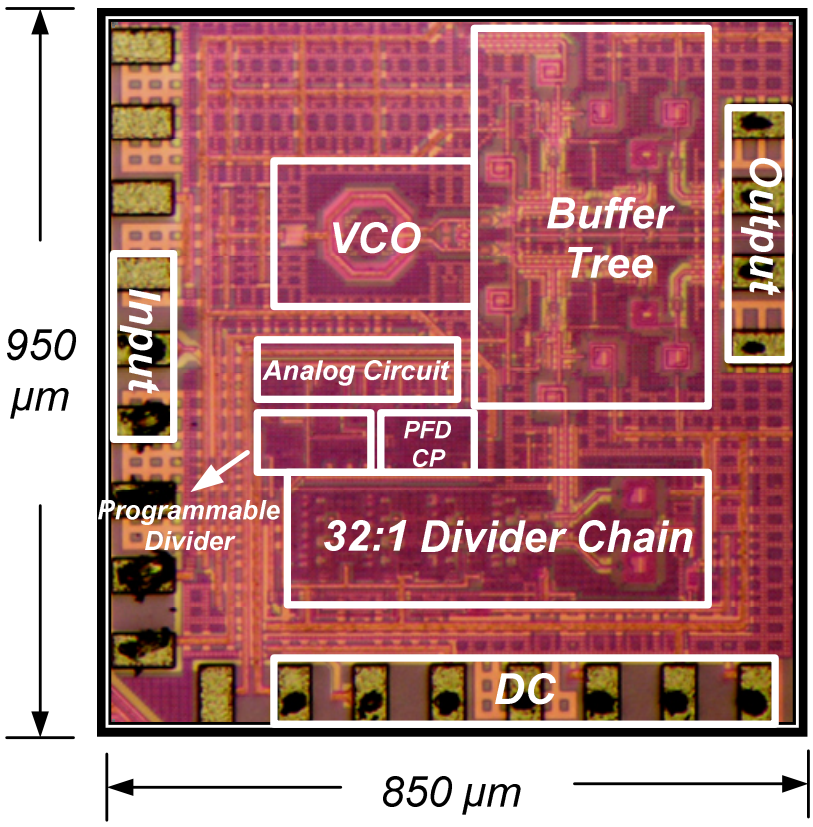


Figure 6.32 Chip micrograph

The measurement of the mm-wave frequency synthesizer is not easy. The synthesizer operates in the closed-loop mode. Its function of frequency synthesis and noise performance can only be evaluated when it is in the closed-loop operation. But actually the measurement of the open-loop operation is also important. In the open-loop mode, we get the chance to assess the performance of each circuit block. It is helpful to detect design faults when the closed-loop performance is not as good as expected. Additionally, since the loop filter is off-chip in this work, the measured results of circuit blocks in open-loop operation, such as the VCO and divider chain, could be used to optimize the LPF design.

In this work, the measurement of the chip is first carried out without LPF. The frequency synthesizer operates in the open-loop mode. The VCO and the whole 32:1 divider chain will be measured on-wafer respectively. Afterwards, a board with an on-board LPF is designed and fabricated. The chip is mounted on the board and the on-board LPF connects to the on-chip circuit through the wire-bonding. Eventually, the performance of the complete closed-loop frequency synthesizer is measured.

6.5.1. Free-running VCO

Given the control voltage of the VCO, the output signal of the buffer tree is measured with a differential GSSG probe setup. But only one single-ended output has been measured, and the other one is connected to a 50 Ω terminal. The frequency and power of the output signal are measured using the R&S FSU67 spectrum analyzer.

Results of the VCO's tuning range and output power of the buffer tree are attained with this measurement. As mentioned above, the supply voltage of the VCO is separated with the common supply voltage V_{DD}. With this 1.2 V supply, the designed VCO dissipated 4.6 mA, a little bit higher than the simulated value. Increasing the control voltage from 0 to 1.2 V, a frequency tuning range of 38.2 – 44.2 GHz has been measured, as shown in Figure 6.33 (a). A 1.4 GHz frequency shift to a higher frequency is observed. Indeed, frequency shift is quite common in mm-wave design since the expected parasitic elements and transistor model could not be accurate in such high frequencies. But based on our previous knowledge, this

frequency shift was expected in the design stage. The tuning range of the VCO is deliberately designed to be approximately 2 GHz lower than the desired tuning range. Eventually, the measured tuning range covers the whole frequency range of interest successfully, even though frequency shift occurs.

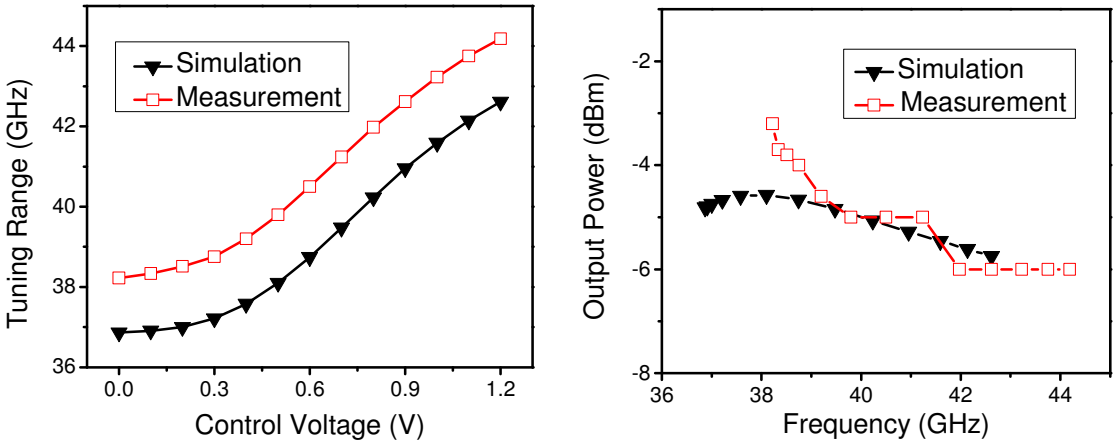
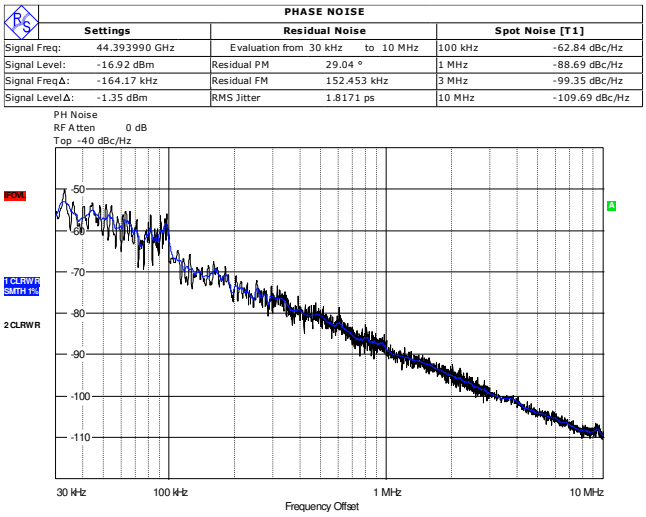


Figure 6.33 Measured and simulated (a) tuning range of VCO and (b) output power of buffer tree

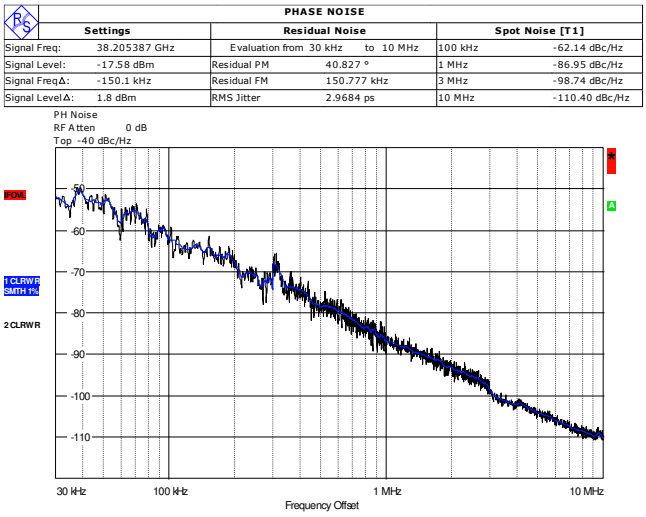
The simulated and measured output power is plotted in Figure 6.33 (b). The loss of probe, cables has been calibrated from the measurement results. As mentioned, the peak of the output power is designed to be at around 38 GHz. If the frequency shift occurs as expected, the peak of the output power might shift to 40 GHz, which is the center frequency. However, this frequency shift was not observed in the measurement. The output power of the frequency synthesizer is above -6 dBm over the whole band.

Phase noise of the free running VCO have also been measured. According to the measured tuning range of the VCO, the average tuning sensitivity of the designed VCO is as high as 4 GHz/V. This high tuning sensitivity would make the phase noise measurement of the free-running VCO extremely different. It is very hard to achieve state results. Figure 6.34 shows two screenshots of measured phase noise when the free-running VCO is oscillating at lowest frequency and highest frequency. The phase

noise at 1 MHz offset is closed to -90 dBc/Hz. As analysis in chapter 3, the AM-PM conversion is serious in mm-wave VCO. As can be seen, the phase noise from 1 MHz offset and 10 MHz offset follows a -20 dB/dec slope. In the frequency offest smaller than 1 MHz, the phase noise increases dramatically, which already goes into the $1/(\Delta\omega)^3$ region.



(a)

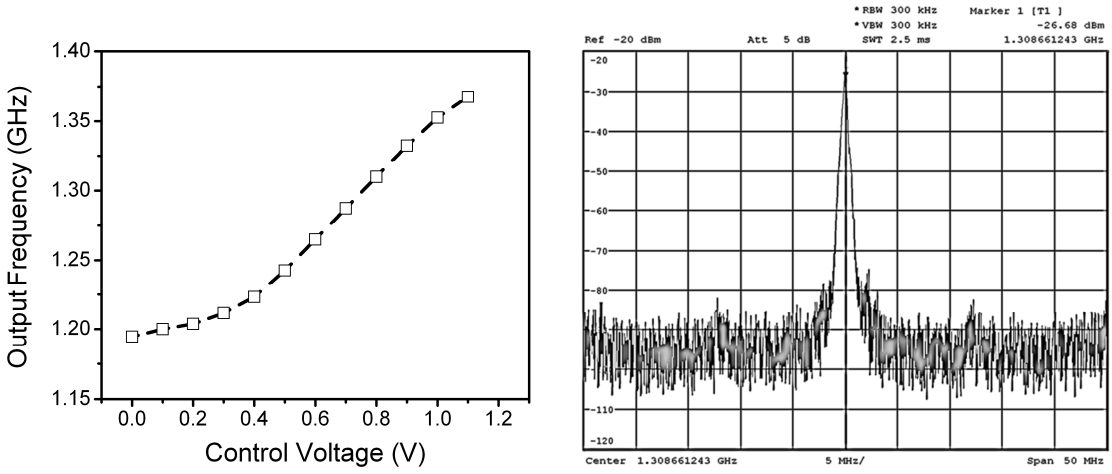


(b)

Figure 6.34 Measured phase noise of free-running VCO at around (a) 38 GHz and (b) 44 GHz

6.5.2. 32:1 Divider Chain

Thanks to the buffer chain at the output of the divider chain, it is possible to measure the performance of the 32:1 frequency divider chain. In this measurement, the frequency of the divider chain input is varied by sweeping the control voltage of the VCO. The output signal of the 32:1 divider chain is measured at the output of the 1.25 GHz buffer chain. Figure 6.35 (b) shows a screenshot of the measured spectrum around 1.3 GHz.



(a) **(b)**

Figure 6.35 (a) Frequency range and (b) spectrum of divider chain output

The measured frequency range of the divider chain output is plotted in Figure 6.35 (a). The locking range of the total divider chain could be attained by multiplying by 32. The divider chain operates correctly between 38.2 GHz and 43.8 GHz. Sweeping the control voltage, it could be observed that the frequency division is achieved from 0 to 1.1 V. Apparently, the locking range of the 32:1 divider chain failed to cover the whole tuning range of the VCO. But its locking range is wide enough to satisfy the desired bandwidth of the LO signal.

6.5.3. Closed-loop Measurement

After testing the VCO and divider chain, the closed-loop measurement of the frequency synthesizer is carried out. For this measurement, a board was designed and fabricated. The LPF is implemented on board. The chip is mounted on the board and connected to the LPF by wire-bonding. Figure 6.36 shows the board with the mounted chip. The reference input is given by a signal generator and the output signal is measured on-wafer using the R&S FSU67 spectrum analyzer.

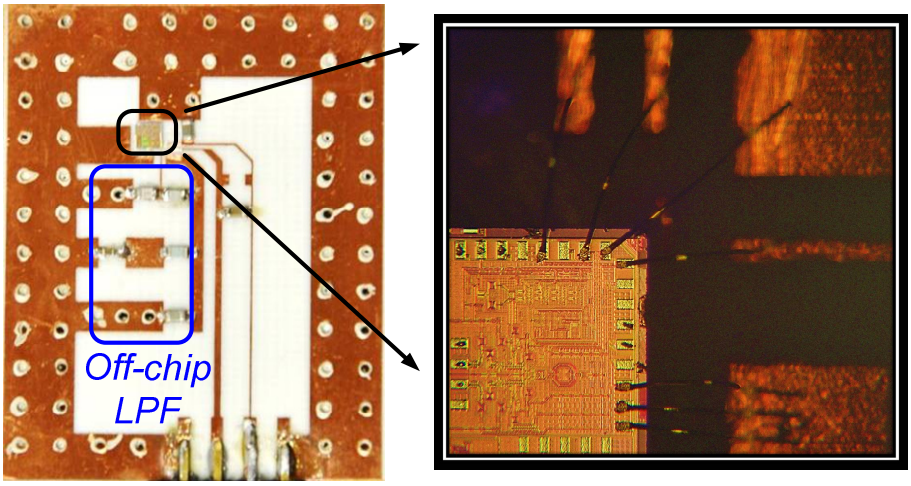


Figure 6.36 Implementation of measurement board

The circuit operates under a 1.2 V supply voltage. The whole synthesizer dissipates 63 mA dc current. Fixing the module of the programmable divider at 27 and sweeping the reference frequency, the synthesizer achieves the phase locking between 38.7 GHz and 43.3 GHz. This frequency range covers successfully the whole targeted band.

But the operation range of the synthesizer is much smaller than the measured VCO's tuning range and the locking range of the divider chain. This shrink of operation frequency range could be explained from the perspective of the control voltage of the VCO. The tuning range of the VCO is measured with a 0-1.2 V control voltage. By changing the control voltage, the input frequency of the divider chain is

varied. The divider chain only works with the control voltage between 0 and 1.1 V. As for the synthesizer's phase locking range, it can be seen that the charge pump only provides a control voltage from 0.3 V to 1 V. That is the reason why the synthesizer's operation range shrinks. The design of the charge pump circuit, as shown in Figure 6.26, is rechecked. The current mirrors $M_{20\text{-}23}$, $M_{11\text{-}12}$ in the charge pump were designed with the minimum channel width. The purpose of this choice is to reduce the parasitic capacitance, leading to a high-speed operation. However, when the control voltage of the VCO is close to 0 or to the supply voltage 1.2 V, a large voltage mismatch would occur at the drain of transistor M_{21} and M_{22}. As a result, severe current mismatch is caused and the net current of the charge pump cannot raise or decrease the control voltage of the VCO. If the long channel transistors are chosen, the current mismatch would be suppressed and the charge pump circuit would operate even when the control voltage of the VCO approaches 0 or 1.2 V.

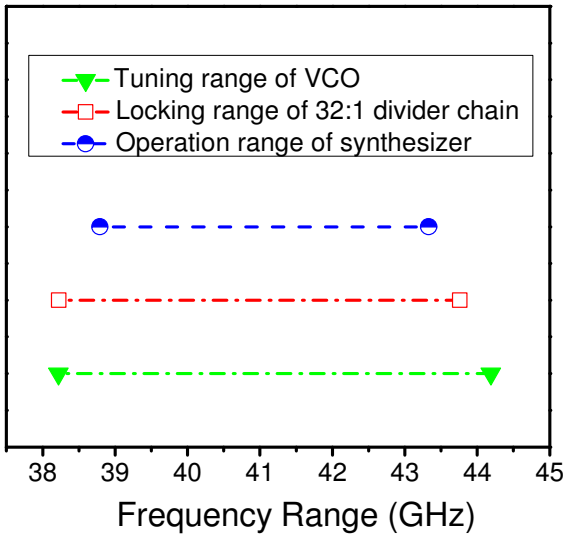
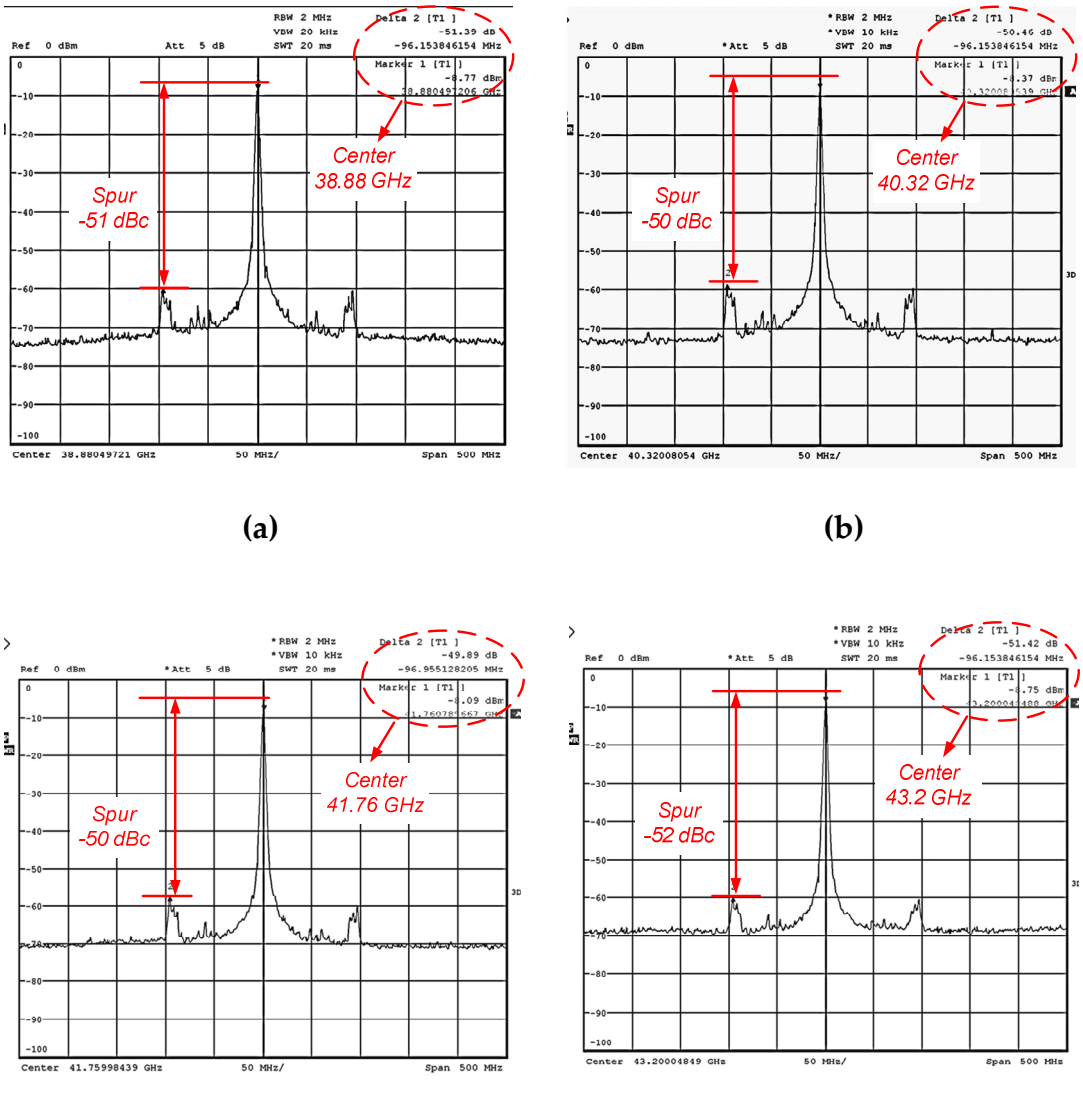


Figure 6.37 Frequency range of VCO, divider chain and frequency synthesizer

By toggling the modules of programmable dividers, 4 different LO frequencies have been synthesized successfully for the 4 channels of the IEEE standard 802.15.3c. Figure 6.38 shows the screenshots of the 4 synthesized LO

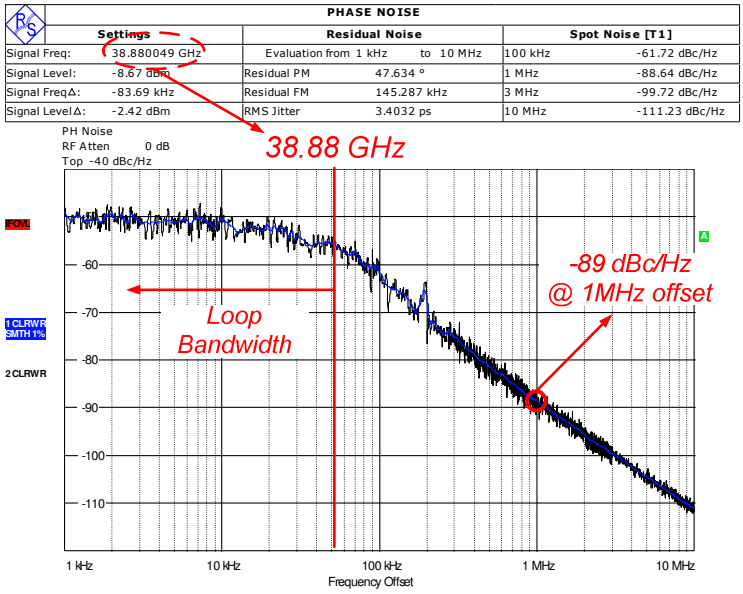
carriers, at 38.88 GHz, 40.32GHz, 41.76 GHz and 43.2 GHz. The reference spurs of the 4 LO carriers are all smaller than -50 dBc. However, it can be seen that the reference spur is not located exactly at 90 MHz offset, which equals the reference frequency. The observed spur has a frequency band around 90 MHz. This phenomenon might be caused by the FM broadcasting signal which is around 95 MHz. For mm-wave measurement, the FM signal could easily be coupled to circuits through voltage supply or substrate, eventually appearing at the output.



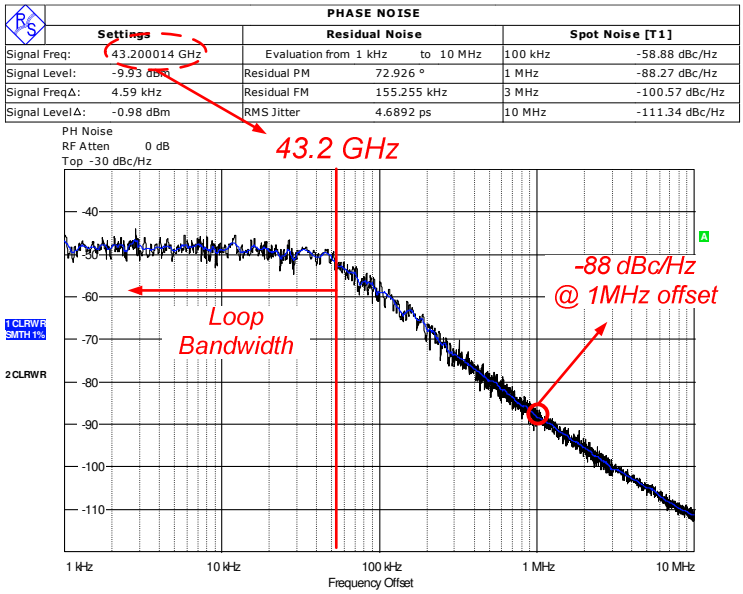
(a) **(b)**

(c) **(d)**

Figure 6.38 4 LO carriers output at (a) 38.88 GHz, (b) 40.32 GHz, (c) 41.76 GHz and (d) 43.2 GHz



(a)



(b)

Figure 6.39 Phase noise measurement with Phase Noise Unit at (a) 38.88 GHz and (b) 43.2 GHz

The phase noise performance is measured using the phase noise unit of the spectrum analyzer. The phase noise unit is a software, which could extend the capability of the spectrum analyzer by phase noise tests [106]. Figure 6.39 shows two

screenshots of the phase noise measurement, at the highest LO carrier 43.2 GHz and the lowest LO carrier 38.88 GHz. As we can see, the designed 40 GHz frequency synthesizer resulted in good phase noise performance at 1 MHz offset. At these two LO frequencies, close to -90 dBc/Hz phase noise has been observed at 1 MHz offset. The measurement results of the implemented 40 GHz frequency synthesizer are summarized in Table 6.13.

Table 6.13 Summary of measurement results

VCO's tuning range	38.2 – 44.2 GHz
32:1 divider chain's locking range	38.2 - 43.8 GHz
Synthesizer's operation range	38.7 - 43.3 GHz
Output power (dBm)	> -6 dBm
Phase noise @ 1MHz offset	-89 dBc/Hz
Reference spur	< -50 dBc
Power consumption	75 mW

In Table 6.14, the performance of the demonstrated 40 GHz frequency synthesizer is compared with the published works. As we can see, the designed frequency synthesizer achieves a wide frequency range from 38.7 GHz to 43.3 GHz. It has an 11.2% frequency range, centered on 41 GHz. The output frequency range has successfully covered the desired 4 LO carriers for the 60 GHz high-data-rate WPAN application. As for the noise performance, the designed frequency synthesizer achieves -89 dBc/Hz phase noise at 1 MHz frequency offset, and reference spurs smaller than -50 dBc. These are comparable with the best results achieved so far. It is interesting to find that synthesizers with a large loop bandwidth all have poor phase noise performance. But the power consumption is a little high. The VCO's buffer tree contributes most of the total power consumption. All in all, the performance of the 40 GHz frequency synthesizer compares well with most state-of-the-art versions.

Table 6.14 Performance comparisons of published mm-wave synthesizers

	[107]	[108]	[101]	[105]	[109]	[110]	This work
Output Freq. (GHz)	39.1-41.6 (6.2%)	45.9-50.6 (9.8%)	35-41.8 (17.7%)	70-78 (10.8%)	58-60.4 (4.1%)	61-63 (3.2%)	38.7-43.3 (11.2%)
Division Ratio	512-2032 (Fra.)	1024 (PLL)	640-1240 (Integer)	1024-1984 (Integer)	256-258 (Integer)	1024 (PLL)	864-960 (Integer)
LPF Type	3rd-order off-chip	2nd-order on-chip	2nd-order off-chip	2nd-order on-chip	3rd-order on-chip	2nd-order on-chip	3rd-order off-chip
Loop BW	200 kHz	400 kHz	100 kHz	1 MHz	N/A	1 MHz	100 kHz
Phase Noise (dBc/Hz)	-90 (1MHz)	-72 (1MHz)	-97 (1MHz)	-83 (1MHz)	-85 (1MHz)	-80 (1MHz)	-89 (1MHz)
Spur (dBc)	-54	-40	-50	-49	-50	-49	-50
Ref. Freq. (MHz)	50	45.1	36	50	234.1	60	90
Supply Voltage (V)	1.2	1.5	1.2	1	1.2	1.2	1.2
DC power (mW)	64	57	80	65	80	78	75
Tech.	90 nm CMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS	90 nm CMOS	90 nm CMOS	90 nm CMOS
Area (mm^2)	1.54 (Inc. pad)	0.87 (Inc. pad)	1.1 (core)	0.16 (core)	0.95 (Inc. pad)	0.36 (core)	0.8 (Inc.pad)

6.6. Conclusion

In this chapter, a 40 GHz frequency synthesizer for the 60 GHz communication application of IEEE standard 802.15.3c was demonstrated. The chip was designed using TSMC 90 nm CMOS technology. The complete top-down design flow was presented, beginning with the transceiver architecture and frequency plan,

then the architecture of the synthesizer, finally the design of each circuit block and the optimization of loop performance.

From the resulting measurements, this 40 GHz frequency synthesizer achieves 38.7 – 43.3 GHz LO signals with -89 dBc/Hz phase noise at 1 MHz offset and reference spurs smaller than -50 dBc. The total power consumption is 75 mW under a 1.2 V supply voltage. This performance compares favorably with the state-of-the-art results. What is more important is that this 40 GHz synthesizer has successfully achieved the desired 4 LO carriers with good noise performance, which satisfies the 60 GHz high-data-rate communication application IEEE 802.15.3c.

Chapter 7.
Conclusion and Prospect

With the great advances in CMOS technology, some mm-wave wireless applications like high data-rate communication, automobile radar and imaging have been developed, and received more and more attentions. As a vital function of the wireless receiver, mm-wave frequency generation faces many design challenges. This dissertation focuses on the analysis, design and implementation of integrated frequency generation circuits using CMOS technology for mm-wav applications.

The design of high performance mm-wave circuits requires passive devices with a high *Q*-factor. For deep-submicron CMOS technology, high metal density is required for each metal layer. Numerous metal dummy fills might be placed in the layout to achieve the specific metal density. These metal dummy fills can lead to great difficulties for mm-wave inductor design. In this dissertation, two kinds of patterned dummy fills are proposed for the design of spiral inductors and symmetric inductors respectively. With the proposed dummy patterns, designed spiral inductors achieve a high SRF, and symmetric inductors realize high *Q*-factor. The spiral and symmetric inductors together with the proposed dummy patterns are used extensively in the circuit design.

Compared with the RF CMOS VCO, the design of CMOS VCO for the mm-wave frequency encounters additional difficulties, such as low *Q*-factor varacor and high tuning sensitivity etc. Serious design trade-offs exist between the tuning range, the phase noise, and the oscillation start-up. A re-configured topology of a resonated negative-conductance cell has been proposed to boost the negative conductance of the conventional cross-coupled transistor pair. As a result, very small cross-coupled transistors could start oscillating. The design trade-off between tuning range and oscillation start-up is alleviated. This technique is utilized for the design of a 40 GHz VCO using 90 nm CMOS technology. From On-wafer measurement results, the 40 GHz VCO achieves 8.9% frequency tuning range and -96.7 dBc/Hz phase noise at

1 MHz offset, while consuming only 1.65 mW dc power. An excellent balance of all critical performance specifications has been realized. This VCO achieves a good figure-of-merit of -185.4 dBc/Hz, which is one of the best results so far.

Normally, multi-stage divide-by-2 circuits are required in the mm-wave frequency synthesizer. As the most popular topologies of the 2:1 frequency divider, the ILFD suffers from a limited locking range, while the CML-based static divider is difficult to operate at mm-wave frequencies. Design optimizations have been carried out to improve their performance. Firstly, a Q-band ILFD has been designed with 90 nm CMOS technology. A topology of transformer-based dual-path injection was proposed to maximize the power gain of the injection path and improve the locking range of the ILFD. On-wafer measurements showed that with 0 dBm input power, the proposed ILFD achieves a 30.5 % locking range from 36 GHz to 49 GHz. It consumes only 2.64 mW under a 1.2 V supply voltage. In terms of the locking range, this ILFD advances the state-of-the-art works. Another design example is given for the high frequency static divider. A design process which highlights the balance between optimum operation frequency and output power has been proposed. By using this design flow, an 8:1 static divider has been designed using 0.13 μm CMOS technology. Without employing the inductor peaking or any other broadband technique, the 3-stage 8:1 static divider is capable of operating up to 32 GHz with 0 dBm input power. Compared with state-of-the-art systems, the performance achieved compares favorably with the best results reported.

In chapter 5, a 40 GHz frequency synthesizer for high data-rate 60 GHz communication application of IEEE standard 802.15.3 was demonstrated. It will be used in a 60 GHz super-heterodyne two-convention transceiver to provide the LO signal. The complete top-down design flow was presented, beginning with the transceiver architecture and frequency plan, then the architecture of the synthesizer, finally the design of each block circuit and the optimization of loop performance. The chip was implemented with TSMC 90 nm CMOS technology. From the on-wafer measurement, the frequency synthesizer achieves a very wide frequency range from 38.7 GHz to 43.3 GHz. It is an 11.2% frequency range, centered on 41 GHz. What is most important is that the frequency range of the output signal has successfully

covered the desired 4 LO carriers of IEEE standard 820.15.3c. As for the noise property, the frequency synthesizer produces a -89 dBc/Hz phase noise at 1 MHz frequency offset and reference spurs smaller than -50 dBc. But the power consumption is a little bit high. Most dc power is consumed by the VCO's buffer tree. All in all, the performance of the 40 GHz frequency synthesizer compares well with the state-of-the-art results.

In this dissertation, design issues of the mm-wave frequency generation circuits are analyzed. Novel techniques and optimized topology are proposed for the design of VCO and frequency dividers in the mm-wave frequency band. With the proposed techniques and topologies, a 40 GHz VCO, a Q-band ILFD and a 32 GHz 8:1 static divider chain are achieved. From on-wafer measurement, they both achieve results comparable with the state-of-the-art developments. Finally, a complete 40 GHz frequency synthesizer is demonstrated for 60 GHz high data-rate communication application. It achieves a wideband 40 GHz LO signal with distinct noise performance, which satisfies the application of IEEE standard 802.15.3c.

Based on this 40 GHz frequency synthesizer, we discuss future work focusing on mm-wave LO generation. For the mm-wave LO signal at 40 GHz, 60 GHz or an even higher frequency, it can be synthesized by using a fundamental LO. But actually it is not the preferred solution. Firstly, the VCO operating at a fundamental frequency is very sensitive to external noise and disturbance, due to the large tuning sensitivity. It is hard for the VCO to maintain a stable operation at such high frequencies. The other shortcomings are related to the loop performance. From the foregoing analysis on the loop performance of the 40 GHz synthesizer, we conclude that the out-band phase noise contribution dominates the total phase noise of the synthesizer's output. To achieve a good phase noise at the output, a small loop bandwidth has to be used. It might yield acceptable results in the research work. But in practice it is not an ideal solution. There are two reasons for this. One is that small loop bandwidth results in a long-time transient response. Another reason is that a small loop bandwidth would make the total performance of the frequency synthesizer depend greatly on the VCO's characteristics. Meanwhile, since the VCO is the most sensitive circuit in the synthesizer, it is apt to be influenced by external disturbances. Consequently, the

operation of the frequency synthesizer becomes sensitive to the external environment as well. This is the last thing that designers want to see.

Some measures could be taken to resolve these drawbacks. The large tuning sensitivity of the VCO could be reduced by employing the switched tuning technique discussed in chapter 3. But the CMOS switch would also induce great losses, leading to phase noise degradation. Besides, the control of the switched-capacitor array requires an automatic calibration circuit. It is a complicated digital circuit, which generates the control code of the switches to achieve the coarse frequency tuning. As for the phase noise performance, the out-band phase noise contribution could be suppressed by using a high frequency reference signal. As a result, the total division ratio of the frequency synthesizer scales down, which implies a smaller noise addition to the out-band noise. In this case, a large loop bandwidth could be designed. The output phase noise then depends upon the out-band phase noise contribution. As we can see in Ref. [111] and [112], 350 MHz and 1 GHz reference signals are used respectively. These two are successful examples which achieve a good phase noise, but at the same time have a large loop bandwidth. But practically, how to generate the high frequency reference signal with low phase noise is still a challenge, since no crystal oscillator could provide such a high frequency reference signal.

In my opinion, stable operation, insensitivity to external environment and low phase noise are the most critical targets for the design of mm-wave LO generation, which designers should be concerned about. In the meantime, aiming at these three targets, LO generation from the fundamental VCO is apparently not a wise choice. The better solution might be to create the desired mm-wave LO signal from a stable, low-noise and frequency-programmable low frequency LO signal. Three different approaches to boost LO frequency have been introduced before. Each one has drawbacks. More effort is required to resolve these disadvantages.

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