Low Power CMOS RF-Transceiver Circuits for K-Band Wireless Localization Systems

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Zusammenfassung

Die rasche Entwicklung der drahtlosen Sensornetzwerke weckt das Interesse an kostengünstigen, drahtlosen Lokalisierungssystemen mit niedriger Leistungsaufnahme. Für die Umsetzung solcher Systeme sind in CMOS-Prozessen hergestellte K-Band Radar-Transceiver eine leistungseffiziente und kostengünstige Wahl. Die Umsetzung der K-Band-Schaltungen in Silizium ist mit vielen Herausforderungen, wie z.B. parasitären elektromagnetischen Effekten und ungenauen Modelle verbunden. Der Schaltungsentwurf für solche Systeme stellt dadurch eine echte Herausforderung dar, da Leistungsaufnahme und Chipfläche in den integrierten Transceivern gleichzeitig minimiert werden müssen.

In dieser Dissertation werden Entwicklung, Simulation und Messung von leistungseffizienten K-Band Transceiver-Schaltungen in einem 130 nm CMOS-Prozess vorgestellt. Zunächst werden Systembetrachtungen durchgeführt, auf deren Basis ein Direct-Conversion-Transceiver für das Frontend des FMCW-Radars ausgewählt wird. Anschließend werden der CMOS-Prozess und die Modellierung der Bauelemente ausführlich besprochen. Mehrere kritische Probleme werden analysiert, z.B. Dämpfungsmechanismen in Silizium-Substraten, elektromagnetische Effekte von passiven Bauelementen und die Zuverlässigkeit und Genauigkeit der Transistormodelle. Darauf basierend werden passive und aktive Schaltungen wie Baluns, Schalter und Mischer mit unterschiedlichen Topologien vorgestellt, verglichen und diskutiert. Die optimierten Designs mit dem primären Ziel eines geringen Stromverbrauchs werden für die weitere Integration ausgewählt. Schließlich wurden die Schaltungen in zwei integrierte Empfänger-Frontends und einen 4-Kanal-Transceiver integriert. Diese integrieren Systeme wurden in Rahmen des BMBF-Projektes „LOWILO“ entworfen, prozessiert und charakterisiert. Simulations- und Mess-Ergebnisse werden kritisch miteinander vergleichen und bewertet.

Abstract

The rapid development of wireless sensor networks brings the demand for low-power low-cost wireless localization systems. For the implementation of these localization systems, K-Band radar transceivers fabricated in CMOS process technologies are a power- and cost-efficient choice. The realization of K-Band circuits in silicon faces many challenges such as parasitic electro-magnetic effects and inaccurate models. The designs become even more difficult as the power consumption and chip area need to be minimized in the integrated transceiver.

In this dissertation, the design, simulation and measurement of low-power K-Band transceiver circuits using a 130 nm CMOS process are presented. Firstly, the system considerations of the transceiver are analysed; a direct conversion transceiver is chosen for the frequency-modulated continuous-wave radar front-end. Then the CMOS process and the component modeling are discussed in detail. Several critical problems are analysed, such as loss mechanisms in silicon substrates, electromagnetic effects of passive components, and model accuracy of the transistors. The designs of baluns, switches and mixers of different topologies are presented, compared and discussed. The optimized designs with focus on low power consumption are then chosen for the further integration. Finally, the developed circuits were implemented in two integrated receiver front-ends and a 4-channel transceiver. These integrated systems were designed, fabricated and characterized in the frame of the BMBF-project “LOWILO”. Finally, simulations and measurements are carefully verified and compared with each other.

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List of Symbols

The following table describes the symbols used throughout the thesis. The unit which applicable and the page on which each one is defined or first used is also provided. Some symbols which are not frequently used are not listed here.

Symbol	Meaning	Unit	Page
B,BW	bandwidth of a signal	Hz	14
T	period of a signal	s	14
Δt	round-trip-time of a radar signal	s	14
Δf	frequency difference	Hz	14
v	relative speed of a target	m/s	14
c	speed of light	m/s	15
P_r	received power of a signal	dBm	17
P_t	transmitted power of a signal	dBm	17
G	gain of a signal	dB	17
σ	radar cross section of a target	m^2	17
and λ	wavelength of a signal	m	17
α	absorption factor of air		17
I_D	drain current of a MOSFET	mA	33
V_{ds}	drain-to-source voltage of a MOSFET	V	33
V_{gs}	gate-to-source voltage of a MOSFET	V	33
V_{th}	threshold voltage of a MOSFET	V	33
μ_0	charge-carrier effective mobility	$m^2/(V \cdot s)$	34
C_{ox}	gate oxide capacitance per unit area of a MOSFET	F/m^2	34
W	transistor width of a MOSFET	μm	34

Symbol	Meaning	Unit	Page
L	transistor length of a MOSFET	μm	34
G_m	transconductance of a MOSFET	1/Ω	35
g_{ds}	output conductance of a MOSFET	1/Ω	35
R_L	load resistance of a MOSFET	Ω	35
R_{out}	output resistance of a MOSFET	Ω	35
ω	angular velocity of a wave	rad/s	38
S_{11}	input port voltage reflection coefficient	dB	39
S_{12}	reverse voltage gain	dB	39
S_{21}	forward voltage gain	dB	39
S_{22}	output port voltage reflection coefficient.	dB	39
ΔA	amplitude imbalance of a balun	dB	64
$\Delta\Phi$	phase imbalance of a balun	degree	64

List of Abbreviations

The following table describes the abbreviations and acronyms used throughout the thesis. The page on which each one is defined or first used is also provided.

Abbreviation	Meaning	Page
ADC	analog-to-digital converter	9
ADS	Advanced Design System (EDA software)	44
AOA	angel of arrival	10
ASITIC	Analysis and Simulation of Spiral Inductors and Transformers for ICs (EDA software)	5
BA	buffer amplifier	152
BB	baseband	21
BiCMOS	bipolar complementary metal–oxide–semiconductor	31
BPF	bandpass filter	20
BSIM	Berkeley Short-channel IGFET Model (transistor model)	44
CG	conversion gain	88
CMOS	complementary metal–oxide–semiconductor	1
CS	common source	59
CST	Computer Simulation Technology (EDA software)	57
CW	continuous wave	13
DC	direct current	3
DRC	design rule check	90
DSB	double sideband	102
EDA	electronic design automation	42

Abbreviation	Meaning	Page
EM	electro-magnetic	5
FET	field effect transistor	118
FFT	fast Fourier transform	18
FMCW	frequency-modulated continuous-wave	5
FSK	frequency-shift-keying	21
GaAs	gallium arsenide	31
GPS	Global Positioning System (satellite navigation system)	11
GSG	ground-signal-ground	57
GSGSG	ground-signal-ground-signal-ground	57
GSSG	ground-signal-signal-ground	57
HBT	heterojunction bipolar transistor	31
HD1	fundamental tone	49
HFSS	high frequency structural simulator (EDA tool)	56
HiSIM	Hiroshima-University STARC IGFET Model (transistor model)	42
IC	integrated circuit	1
IF	intermediate frequency	3
IFA	intermediate frequency amplifier	153
IGFET	insulated-gate field-effect transistor	33
IIP2	input second-order intercept point	22
IIP3	input third-order intercept point	44
IL	insertion loss	64
IM2	second-order intermodulation product	89
IM3	third-order intermodulation product	49

Abbreviation	Meaning	Page
IP1dB	input 1-dB compression point	88
ISM	Industrial Scientific and Medical	4
I/O	input/output	29
I-V	current-voltage	34
LNA	low noise amplifier	3
LO	local oscillator	12
Loc	localization	13
LoWiLo	Low Power Wireless Sensor Network with Localization	4
LVS	layout versus schematic	90
L-C	inductor-capacitor	67
MCU	microcontroller	13
MIM	metal-insulator-metal	29
MIMO	multi-input-multi-output	118
MISFET	metal–insulator–semiconductor field-effect transistor	33
MMIC	monolithic microwave integrated circuit	32
MOSFET	metal–oxide–semiconductor field-effect transistor	1
MU	measurement unit	10
NF	noise figure	54
NMOS	n-channel MOSFET	5
OIP3	output third-order intercept point	51
PA	power amplifier	3
PDK	process design kit	41
PIN	positive-intrinsic-negative	118

Abbreviation	Meaning	Page
PLL	phase-locked loop	3
PMOS	p-channel MOSFET	5
PQF	polyphase quadrature filter	106
PSK	phase-shift-keying	21
PVT	process-voltage-temperature	156
P1dB	1-dB compression point	18
Q-Factor	Quality-Factor	32
RF	radio frequency	3
RFIC	radio frequency integrated circuit	58
RL	return loss	78
RLCK	resistors, inductors, capacitors and mutual inductors	57
RSS	received signal strength	10
RTOF	roundtrip-time-of-flight	10
RX	receiver	4
R-C	resistor-capacitor	100
SC	single channel	114
SiGe	silicon germanium	1
SNR	signal-to-noise ratio	18
SPDT	single pole, double throw	119
SPST	single pole, single throw	119
TDOA	time-difference-of-arrival	10
TOA	time-of-arrival	10
TRX	transceiver	13

Abbreviation	Meaning	Page
TW	triple well	123
TX	transmitter	4
T/R	transmit/receive	6
VCO	voltage-controlled oscillator	3
VGA	variable gain amplifier	12
WLAN	wireless local area network	28
1P4T	single pole, four throw	147

Chapter 1
Introduction

The rapid and continuous progresses of silicon technologies have been evidenced for the last 4 decades. Defined by Moore's Law, the number of transistors that can be placed on a certain area of integrated circuit doubles approximately every 18 months. Although the transistor channel length sees the 10 nm limit while the quantum tunnel effect becomes significant at this dimension, various alternatives provide further possibilities to break through the limit [1]. Recently, Intel started their new factory to scale down the transistor size to 14 nm at year 2014 [2], which could be considered as a further attempt to continue Moore's Law in the next 5~10 years.

The silicon technologies have brought, and are continuously bringing, enormous changes to everyday life of human being. They keep on changing almost all the aspects of human life, including living, production, financing, telecommunication, transportation, medical care, entertainment, education and so on. Before the economic meltdown in 2008, the overall market size of microelectronics exceeds 350 billion US dollar [3]. In the microelectronics industry, nearly 99% of the transistors are MOSFETs which are mainly produced in CMOS technologies.

Due to the rapid progress of the CMOS technologies and their low cost for mass production, various different integrated circuit systems traditionally realized in other technologies are continuously shifting to CMOS. For example, the 77 GHz automotive radar [4], which is previously realized in III-V or SiGe processes, is also developed by Toshiba in 65 nm CMOS technology recently [5].

Among various integrated circuits, the wireless sensor ICs has experienced tremendous growth recently [6]. In year 2010 the shipment of wireless sensor ICs has shown a growth of more than 300%. Wireless sensor nodes are embedded devices which integrate sensor, control, computation and communication capabilities together with limited cost and power consumption; while wireless sensor networks are self-organized wireless networks composed

by large amounts of wireless sensor nodes which detect, analysis and process the required information from a certain area and provide the information to the users.

The wireless sensor network could be implemented in various areas and is considered as one of the most promising technologies in this century. In environmental protection, it can be implemented to gather large amounts of original data to monitor environment and climate change. It could also be used to predict natural catastrophe such as flash floods and forest fires. In agriculture, wireless sensor networks can be implemented to monitor irrigation conditions, earth and air changes, pest, and fertilize situations, the conditions of domestic animals and so on. In industry, wireless sensor nodes can be implemented in highly automated factories for precise control of the manufacture machines, as well as to in high-risk environments to detect the dangerous or poisonous materials. In infrastructure, it can be used to detect the situations of high-buildings, bridges, dams and other buildings and enable people to monitor these situations. In home automation, different devices could be connected by the wireless sensor networks; therefore they could automatically cooperate with each other to provide convenience and comfort to the inhabitants. In medical, wireless sensor network can detect the physiological data of the patients, monitor the health conditions of older people, manage drugs, perform remote medical treatments, and so on.

One important feature of wireless sensor network is local positioning. With the accurate position information of the wireless sensor node, the functionality of wireless sensor networks can be further improved. For example, in industry automation, the position of transporting vehicles or robotic arms should be very accurate; therefore accurate positioning of these devices is crucial to the device performances. For outdoor navigation, the local positioning can provide much more accurate positioning than common navigation systems; which can be used in logistics or for blind people guidance, where accurate positioning is required. For smart home applications, the position of mobile devices could also be quite interesting, especially as they become smaller and smaller day by day. In health care, the localization techniques can be used to regularly monitor the health conditions of patients and to provide in-time first-aid in cases of sudden attacks of diseases.

Among the different techniques to realize the local positioning, using radar technology to measure the distance of the device and certain reference objects is the most popular one. Compared with the other localization techniques, the accuracy of the radar technology depends on the operating frequency. As operating frequency becomes higher, the radar based wireless localization becomes more and more accurate. Therefore, the radar based localization

techniques are ideal for the wireless sensor networks which require high accuracy, such as in industry automation.

The commercial radar is an established technology and is used widely in automotive industry and ship-building industry. However, the commercial radars on market are too bulky, power-hungry and expensive to be directly used in wireless sensor nodes. Therefore, highly-integrated low-cost low-power radar frontends is the proper choice to realize wireless localization in wireless sensor networks. However, people must overcome several major challenges before the implementation of such radar frontends in reality. One of the major challenges in wireless sensor nodes with local positioning is to reduce the power consumption of the radio frequency (RF) blocks. As the power consumption of the wireless sensor node is very critical, additional power consumption should be avoided. The RF power amplifier is usually the most power hungry block in a wireless system. According to the wireless standard, the output power of a wireless system has a specified value (normally higher than 10 dBm); therefore the RF power amplifier usually consumes much DC power. The other active blocks in the RF transceiver, including VCO, PLL, LNA, buffer amplifiers and mixers, are all power-consuming blocks.

To optimize the power consumption of a wireless system, a system level optimization of a RF transceiver is required. For the receiver part, various figures of merits should be optimized and various trade-offs between performance and power consumption should be considered. For example, for the receiver these are the most critical performances: linearity, gain and noise figure. Gain and noise figure defines the sensitivity of the receiver and linearity defines the maximum input power. For the transmitter the output power and linearity are two of the most important figure of merits. And for the PLL the important figures of merits include phase noise, loop bandwidth and spurious sidebands. Other important aspects for the system design include the process and temperature reliability and the overall chip area.

The optimization of the system-level power consumption needs to consider the trade-off between different figures of merits. Take RF receiver as an example. Gain, power consumption and linearity have a certain trade-off. To realize a high gain and high linearity receiver, the power consumption has to be considerably high. Generally, in order to reduce the power consumption, either linearity or gain performance has to be reduced.

To further reduce the overall system power consumption, decent understanding of the independent circuits is required. The circuit blocks can be separated into two categories: the power consuming blocks such as VCO, LNA, PA and IF amplifier; the blocks consumes very

low power such as TX/RX switches, baluns, polyphase quadrature filters and passive mixers. For the power consuming blocks, the maximum performance and minimum power consumption is required; for the blocks consume low power, the circuit performance should be optimized with minimum insertion loss and other figures of merits. In both cases the characteristics of the active and passive components for the specific technology should be studied.

In conclusion, in order to minimize the power consumption of wireless RF systems, a complete understanding of low power design is required in the component level, circuit block level, sub-system level (receiver, transmitter, PLL, etc) and system level (e.g. RF-Mixed-Signal System-On-Chip system). The power consumption optimization for wireless RF IC circuits is a major topic of this thesis.

Another major challenge for wireless sensor nodes with wireless localization is to reduce the cost introduced by the localization feature. As large amounts of wireless sensor nodes are needed for most applications, the cost for each node must be minimized. To reduce the cost, a standard CMOS process is chosen as the standard CMOS process is most suitable for large-volume production. Besides, the cost of a certain system can be minimized by a systematic plan and careful layout. Simple but realistic system architecture could contribute to reduce the power consumption as well as the cost.

The third major challenge is minimization of the wireless localization systems. As the wireless sensor nodes should be easy to be placed everywhere, the wireless localization system should only occupy a very small space. Therefore fully-integrated front-end is the proper choice for the localization systems. The advanced package technologies should also be considered as they also contribute to the system size.

This dissertation focuses on the design of low power RF ICs for wireless localization in standard CMOS processes. Under the project scheme of LoWiLo, the circuits described in this dissertation are intended to be implemented in wireless sensor network systems with localization at 24 GHz. The design, simulation and measurement details of three types of important circuit blocks, mixers, baluns and switches will be described. Various levels of considerations are discussed, including the passive and active component models, the circuit block topology/optimization and the integrated receiver/transceiver sub-systems.

The circuits in this dissertation perform at K-Band, specifically the 24 GHz unlicensed Industrial Scientific and Medical (ISM) band. The accurate frequency band of the 24 GHz ISM band is from 24 GHz to 24.25 GHz. The ISM frequency bands are originally reserved for

the use of radio frequency in the applications of industrial, scientific and medical purposes. However, nowadays, these ISM bands are of growing interest in short range, low power communication systems. Especially, for the 24 GHz ISM band, it is primarily used for radar and satellite communications, including the automotive radar systems. The LoWiLo project intended to integrate a low-cost low-power version of the traditional automotive radar system into the next-generation short-range communication system, which gives the low power communication system the possibility of wireless localization.

The 24 GHz circuits are traditionally realized in III-V technologies or SiGe technologies, although a few researches about 24 GHz CMOS circuits is published [7]-[11], the work in this field is relatively sparse. For the realization of standard CMOS circuits at 24 GHz, two important factors should be considered: Firstly, the relatively small cut-off frequency of the transistors limits the circuit performance. For NMOS transistors the cut-off frequency is around 90 GHz and for PMOS transistors the cut-off frequency is close to 30 GHz. Some circuit topologies become improper at 24 GHz, as the cut-off frequency of PMOS transistors are too low. For example, the inverter-type amplifier, which is quite popular for low power RF applications, is not suitable in this system. Secondly, the Silicon substrate loss of the passive component is different from lower frequencies. Using the EM simulator ASITIC [12], we found out that the eddy currents in the silicon substrate becomes a dominant effect in the passive component loss. It seriously affects the quality factor of an inductor at 24 GHz.

The purpose of the proposed system is to enable wireless localization in the wireless sensor networks. The wireless localization is realized by frequency-modulated-continuous-wave (FMCW) radar. The FMCW radar uses a frequency modulated ramp signal. By analyzing the frequency difference between the received signal and the transmitted signal, the distance and the relative velocity between the radar and the object could be calculated. The FMCW radar transceiver system is similar to other frequency modulated systems, where the frequency modulation is realized in PLLs.

The dissertation is organized as follows:

Chapter 1 is the introduction.

In Chapter 2 the project LoWiLo is described and the fundamental considerations for the RF transceiver system are presented. The project “Low Power Wireless Sensor Network with Localization”, which focuses on enabling wireless localization for wireless sensor network, is discussed with details. Then the FMCW radar technology targeting for wireless localization is

presented and the system specifications of the radar transceiver are analyzed. Different topologies of receiver and transceivers are presented in the last parts while the advantages and disadvantages are compared.

Chapter 3 presents the implement CMOS process, including the metal layers, different active and passive components, cut-off frequencies and so on.

Chapter 4 describes the model and design related to the components. Firstly the MOSFET models, including the lumped element models and compact models, are discussed, analyzed and compared in details. Then selection of different passive components, such as resistors, inductors, capacitors, transmission lines and pads, are presented. The EM simulation methods are compared, and the importance of edge-mesh is demonstrated. Finally the designs of different balun topologies at 24 GHz are described in detail.

Chapter 5 presents the designed passive mixers and their integration with baluns and polyphase filters. The mixers are single balanced passive mixers with complementary switch transistors. Firstly the basics of the RF mixer are presented, and then the selection of the proper topology is discussed. The design of the mixer core and the integration of the mixer with baluns and polyphase filters are presented and analyzed in the following sections. The measured results are compared with state-of-the art results in the last part of the chapter.

In Chapter 6 the design of T/R switches is presented, including the theoretical analysis, circuit realization and characterization of two types of CMOS T/R switches based on the conventional NMOS and the floating bulk NMOS transistors. An improved biasing circuit for floating bulk is implemented. A cascade method to improve the isolation of the T/R switches is proposed. The measured results are compared with the state-of-the-art realizations.

Chapter 7 describes the integrated receiver front-ends. Two K-band low-IF receivers, a single channel receiver and a quadrature receiver, are designed and fabricated in a 130 nm CMOS process. It is demonstrated that, with the proposed polyphase filter, the quadrature receiver is able to achieve similar performance as the single channel receiver in various aspects while maintaining the advantages of quadrature scheme. The measured performances compare the state-of-the-art 130 nm CMOS realizations in this band.

Chapter 8 describes the integrated low power transceiver. The transceiver has one transmission path and four receiving paths. The implemented circuit blocks are described in detail. With careful power management and integration, the designed transceiver has excellent performance and ultra-low-power consumption both at transmission mode and at receiving mode.

The last chapter concludes this dissertation and prospects the future technological possibilities related with this work.

Chapter 2
System Considerations

2.1 Introduction

For a successful system-level design, a decent understanding of system fundamentals is required. Based on the system requirements and the technology specifications, the architecture of the system could be selected and the circuit performance of independent circuit blocks could be specified. In this chapter the fundamentals of the implemented system will be discussed, and basic system level calculation and the proper topologies for the system will be presented.

The chapter is organized as below. Firstly, the LoWiLo Project (Low Power Wireless Sensor Network with Localization) is presented. The basics of wireless sensor network and wireless localization are discussed. Secondly, the basics of FMCW radar system and some preliminary system level calculations are presented. The system specification of the radar front-end is presented. Finally, different topologies of receivers and transceivers are presented, while the advantages and disadvantages of these topologies are analyzed.

2.2 Low Power Wireless Sensor Network with Localization

2.2.1 Wireless Sensor Network

A wireless sensor network consists of distributed sensors to monitor environmental or physical conditions, such as temperature, sound, vibration, pressure, motion or pollutants. The collected data are sent to a main station through a self-organized wireless network. The advanced version of wireless sensor network includes bi-directional data communication,

which allows the main station to control the activity of the sensors. The wireless sensor networks have been used in many military, industrial and consumer applications nowadays [13], [14].

The wireless sensor network is composed of sensor nodes where each node is connected to other sensors. The sensor node, which is called “mote” sometimes, performs some processing, gathers sensor information, and communicates with other sensor nodes. A typical block diagram of a wireless sensor node is depicted in Fig. 2.1. It includes a microcontroller, an RF transceiver, sensors, external memory and power supply. The environmental or physical data are collected by the sensors and encoded by the ADC converter. The microcontroller is used to process the data from the sensors, control the ADC, encode and decode the signal for transmit and reception. The transceiver communicates with other nodes by transferring the signals. The whole circuit is controlled by power supply and the sensor data is saved to memory for further application.

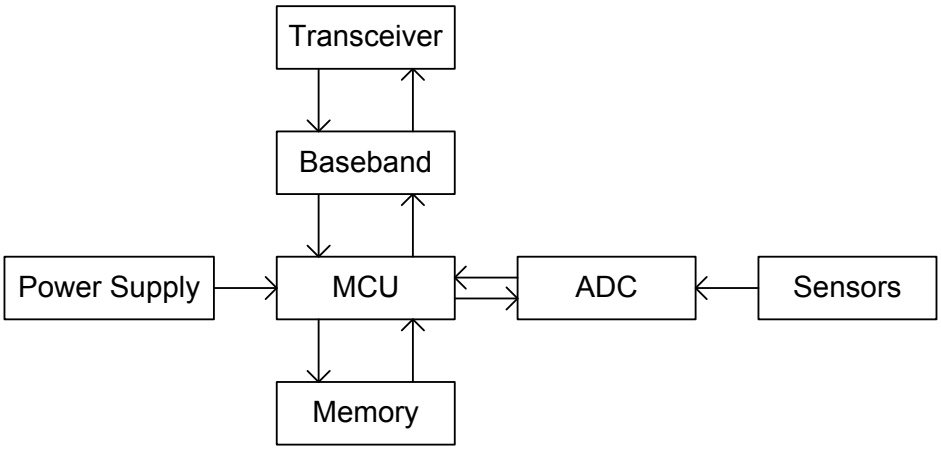


Fig. 2.1 Block diagram of a wireless sensor node

Nowadays high performance sensor nodes with long range communication capability and ultra low power consumption are commercially available. An example is the Waspmote platform produced by Libelium [15]. This sensor node consumes only 0.7 µA current in hibernation mode, together with a high RX sensitivity and TX power it can communicate with each other in a very long range: 7 km for 2.4 GHz, 24 km for 900 MHz and 40 km for 868 MHz.

For indoor and short-range applications, wireless sensor networks operate at higher frequencies are of interest. As higher frequencies is less crowded, the transceiver of the wireless sensor nodes requires less components to operate properly which results in smaller chip area and potentially less power consumption. Besides, the antenna and passive components used at higher frequencies are much smaller than these at lower frequencies, which reduce the size of the wireless sensor nodes as well.

The wireless sensor networks used the license-free communication bands such as 173, 433, 868, and 915 MHz; 2.4 GHz and 5.8 GHz. The standards utilized by wireless sensor networks varies, include ZigBee, Z-Wave, ANT, 6LoWPAN, DASH7, ONE-NET, WirelessHART, BlueTooth Low Energy and so on [16].

2.2.2 Wireless localization

Local positioning is considered as one of the most promising features in the next generation of wireless systems [17]. The great success of wireless systems can be explained by the mobility they enable. However, mobility brings uncertainty, while the only efficient method to overcome the uncertainty problem is local positioning. Local positioning is mostly demanded in systems where uncertainty should be avoided, such as industrial manufacturing, network organization and many other applications. They could also be implemented in self-organizing sensor networks, ubiquitous computing, location sensitive billing, context dependent information services, tracking and guiding and numerous other applications.

Several measurement methods are implemented in wireless local positioning systems, including angle of arrival (AOA), received signal strength (RSS), time-of-arrival (TOA), roundtrip-time-of-flight (RTOF) and time-difference-of-arrival (TDOA) [17].The TDOA is the most popular method as it just needs to synchronize the measuring units.

The operation principle of the TDOA is depicted in Fig. 2.2. The propagation time difference of a signal from a measurement unit (MU) to two different references is measured. The time difference defines a surface in the three dimensional space. By analyzing several measured time differences, the accurate position of the MU could be acquired.

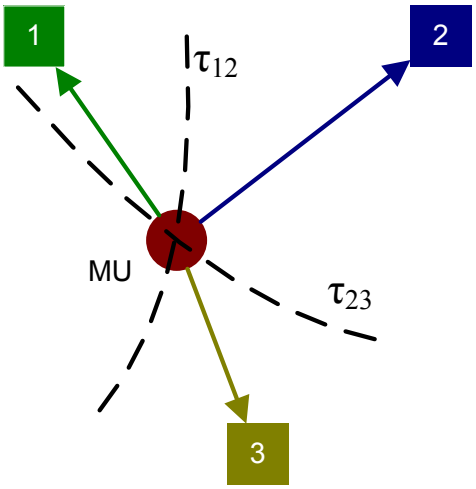


Fig. 2.2 Measurement principle of TDOA

Depending on the required accuracy, the proper technology should be selected for local-positioning systems. For tracking, routing and guiding applications, the demanding accuracy is larger than 1 meter. Existing technologies such as GPS or cell-phone positioning can be implemented. However, for automation or control applications, where the demanding accuracy is much less than one meter, the local positioning technologies mentioned above (such as TDOA) are proper choices. For wireless sensor networks, the TDOA technology and other local positioning technology are the first choice.

2.2.3 Low Power Wireless Sensor Network with Localization (LoWiLo)

The overall objective of the LoWiLo project is the implementation and testing of a miniaturized wireless sensor network with localization functions at 24 GHz. The node size should be smaller than 1 cm^3.In this project, various critical issues regarding the wireless sensor network are studied, which includes advance localization, miniaturization, low power components and transmission reliability.

In this project, the following aspects are of crucial importance. One is the radar localization at 24 GHz: In contrast to the usual procedures, the radar front-end is specially designed for low energy wireless sensor systems. The implementation of the 24 GHz ISM band avoids the crowded ISM bands at lower frequencies. The high bandwidth offers new possibilities in radar techniques for localization with improved spatial resolution.

Secondly, the design of energy-efficient circuit technology for millimeter wave front-end components is also a critical aspect, especially for the CMOS oscillator. As the instantaneous frequency of a CMOS oscillator is usually unstable, the stabilization of the oscillator frequency would be a big challenge.

The other important aspects include energy-efficient signal processing in the baseband, system miniaturization base on stacked sub-functional units and antenna front end circuits, and the sensor node performance optimization through a customized design and so on.

The miniaturized wireless sensor nodes with an extraordinary location function could be used in various important potential applications, such as in the areas of logistics, manufacturing, security, surveillance, robotics, automotive engineering, aeronautics, telecommunications and so on. The first applications would be in home automation and industrial networks.

The system block diagram of the sensor node is shown in Fig. 2.3. There are four important sub-systems in this circuit: antenna and package, RF transceiver, baseband signal processing, and microcontroller, while I am involved in the design of RF transceiver. A 24 GHz VCO is designed to generate the LO signal. A divider is connected to the VCO to generate the 3 GHz signal need by the PLL. In the TX mode the LO signal is sent through a TX/RX switch and amplified by the PA, then it is sent through another TX/RX switch and to the band-pass filter and finally to the antenna. In RX mode the received signal is amplified by the LNA and mixed with the LO signal in the mixer. The generated IF signal is amplified by the IF VGA and converted to digital signal through the ADC.

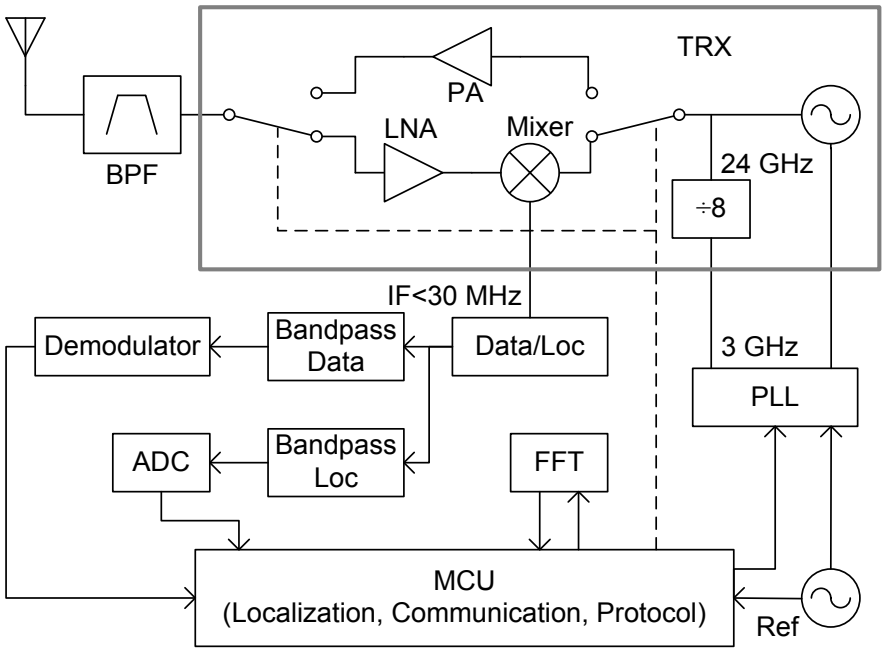
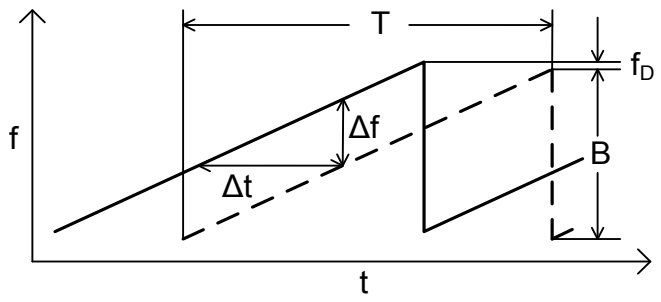


Fig. 2.3 LoWiLo system structure

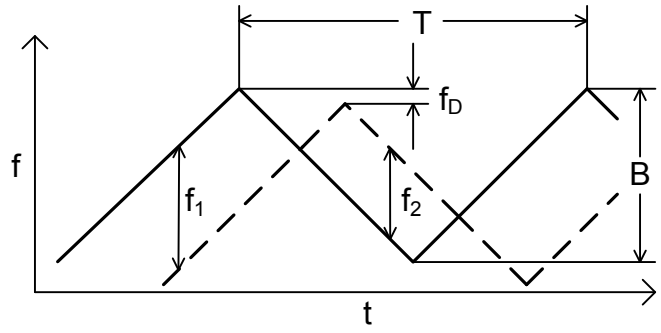
2.3 Radar System Basics

2.3.1 Frequency-Modulated Continuous Wave (FMCW)

The continuous wave (CW) radar, which uses the continuous microwave with constant frequency and amplitude, is able to measure the speed of the object according to the Doppler Effect. However, it is difficult for the continuous-wave radar to measure the distance, as it needs a very accurate timing system to convert the round-trip-time into range. Therefore the frequency modulated continuous wave (FMCW) is proposed. The microwave signal is frequency modulated around a fixed reference. It could be used to detect the distance of the object as well as the speed [18], [19].



(a)



(b)

Fig. 2.4 FMCW system principles

The operation principles of FMCW systems are shown in Fig. 2.4. The solid line is the transmitted signal and the dashed line is the received signal. In Fig. 2.4 (a), the sawtooth type frequency waveform has a bandwidth of B and a period of T. When the transmitted signal is mixed with the received signal, a frequency component Δf is available on the output spectrum. The round-trip-time Δt can be expressed as in case that Δt is less than T,

$$\Delta t = \frac{T}{B}\Delta f \tag{2.1}$$

The peak frequency difference f_D between the transmitted signal and received signal defines the Doppler effect of the object. Suggesting that the received signal has a smaller peak frequency than the transmitted signal, which means that the object is leaving the radar, the relative speed of the target v could be calculated as

$$v = \frac{f_D}{2f} c \tag{2.2}$$

Where f is the average frequency of the transmitted signal and c is the speed of light.

For the angular detection, either multiple antennas or multiple receiver channels are required. By calculating the phase difference between the received signals, the relative angular position of the object could be calculated.

The secondary radar technology is used for calculated the distance between two radar transceivers. FMCW radar is also implemented in the secondary radars. For the secondary radar [20], the calculation of position and speed is similar to the above analysis; however, the time delay of the transceiver nodes is considered. The accurate position could be acquired by processing the signal of multiple nodes, therefore the angular resolution is not required.

Fig. 2.4(b) illustrates another operation principle of the FMCW radar. Instead of the sawtooth frequency waveform, this radar used a triangular frequency waveform. This type of operation avoids the frequency chirp on the sharp edges of the sawtooth waveform, therefore it is more reliable and has less noise. Similarly, the round-trip-time Δt and the relative speed v can be expressed as

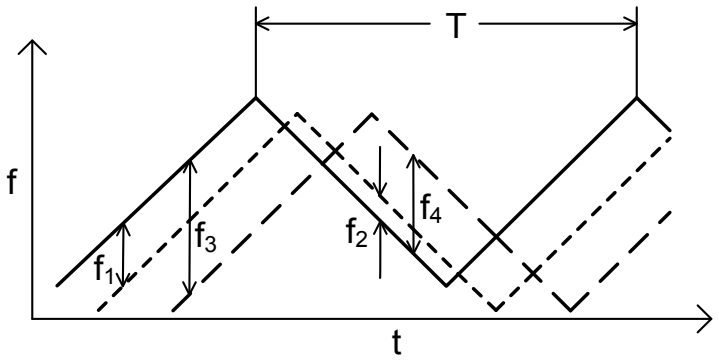
$$\Delta t = \frac{T}{2B}(f_1 + f_2) \tag{2.3}$$

$$v = \frac{f_1 - f_2}{2f} c \tag{2.4}$$

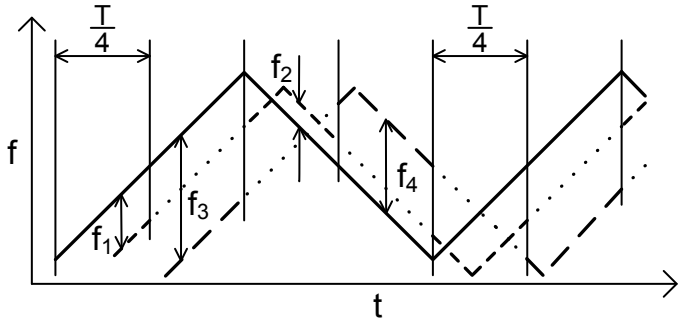
Where f_1 and f_2 are two frequency components of the received signal and represent the received frequency components at different half-periods. From Formula (2.4) it can be seen that the velocity calculation is more precise, as f_1 and f_2 are easy to acquire in the measurement process.

The multi-channel or multi-antenna FMCW radar are implemented also for secondary radar applications. For example, the mechanical arms, which introduced multiple degrees of freedom in the space, are widely used in industry automation systems. The accurate positioning of the joints of the mechanical arms requires multiple channels in a TDOA system.

Fig. 2.5(a) demonstrates the operation principle of multi-channel FMCW radar. Two receive channels operate at the same time. For one channel the received signals are at the frequency f_1 and f_2, for the other channel the frequency of the received signals are f_3 and f_4. From these frequency components the round-trip-time and the relative speed of both receivers could be calculated. Therefore the accurate space position of the complex system could be acquired.



(a)



(b)

Fig. 2.5 Multi-channel FMCW system principles

The receiving-channel cross-talk of the radar system shown in Fig. 2.5(a) might be a crucial problem. In order to solve this problem, a power-saving principle, shown in Fig. 2.6(b) is proposed, as the period T is divided to 2*n time sections. In the different time sections the different channels are switched between on and off. As different channels are switched on and

off in different times, which is similar to time division multiplexing, the channel cross-talk problem could be solved.

2.3.2 Radar System Consideration

The received power of a radar antenna is given by

$$P_r = \frac{P_t G_t G_r \sigma \lambda^2}{(4\pi)^2 R_t^2 R_r^2} e^{-\alpha(R_t+R_r)} L_p \tag{2.5}$$

Where P_t is the transmitted power, G_t is the gain of the transmission antenna, G_r is the gain of the receiving antenna, σ is the radar cross section of the target, and λ is the wavelength of the radio. R_t and R_r are the distance between the transmitter and the object and the distance between the object and the receiver, respectively. α is the absorption factor of air, and L_P is the polarization loss.

For the secondary radar, as it can be considered as the transmission between one antenna and another antenna, the Friis Transmission Formula could be applied

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi R)^2} e^{-\alpha R} L_P \tag{2.6}$$

Where R is the distance between transmit and receive antenna.

From (2.5) it can be seen that the received signal of the radar is reversely proportional to the fourth power of the range, which means the signal declines very fast. On the contrary, the received signal of the secondary radar is reversely proportional to the square of the range, which means the signal declines relatively slowly.

For the low power radar transmitter, considering that the power amplifier cannot draw too much power, the output power of the transmitter is usually 0~6 dBm. The typical antenna gain of the transmitting and receiving signal is several dB, typical 3 dB. Considering that at 24 GHz the absorption of air is not high, the received power could be easily calculated from the distance between the transmitter and receiver:

$$P_r(dBm) \approx P_t(dBm) - 20\log_{10}(\frac{R}{1mm})(dB) \tag{2.7}$$

Therefore, the received power is 6 dBm when the distance is 1 mm. If the distance increases by 10 times, the received power reduces by 20 dB. For a distance of 100 m, the received signal is -94 dBm.

The thermal noise for a FMCW signal can be expressed as

$$P_N(dBm) \approx -174(dBm) + 10\log_{10}(BW_{FFT})(dB) \tag{2.8}$$

Where BW_{FFT} is the bandwidth of the FFT process.

In radar systems, a detectable signal needs a minimum SNR of 16 dB. Suggesting that the bandwidth of the FFT process is 16 kHz, the minimum input power of the received signal should be

$$P_{r\min} \approx -174 + 10\log_{10}(BW_{FFT}) + SNR_{\min} + NF_R(dBm) \tag{2.9}$$

Therefore

$$P_{r\min} \approx -116 + NF_R(dBm) \tag{2.10}$$

Suggesting that the receiver chain has a noise figure of 10 dB, the maximum detecting range is 400 m.

The minimum detecting range depends on the linearity of the receiver. For a FMCW receiver normally the input P1dB is -40~-30 dBm, which limits the minimum detecting range to 0.1 m.

For the standard radar, the detecting range is calculated differently. For a middle-size automotive, σ is approximately 30 m^2. Therefore, the received power can be written as

$$P_r(dBm) \approx 6(dBm) - 40\log_{10}(\frac{R}{0.074m}) \tag{2.11}$$

Taking (2.10) into (2.11), the maximum detecting range is 46 m. The minimum detecting range is approximately 1 m.

By using multi-channel receiver, the SNR of a radar system could be improved. As mentioned in [21], the SNR of a four channel receiver is 4 times higher than a one-channel receiver. This result in 1.4 times longer detection range for standard radar and 2 times longer detection range for a secondary radar.

From the discussion above, it can also be seen that the gain of the antenna is critical for the radar performance. If high gain antennas are implemented, the detecting range of the radar can be further improved. Similarly the overall noise figure of the receiver chain should be minimized, which is also very critical to the radar performance.

2.4 System Specifications

Based on the discussions above, the system specifications of a low power 24 GHz secondary radar transceiver with a detection range from 0.1 m to 100 m can be presented：

Table 2-1 Low Power Secondary Radar Transceiver Specifications

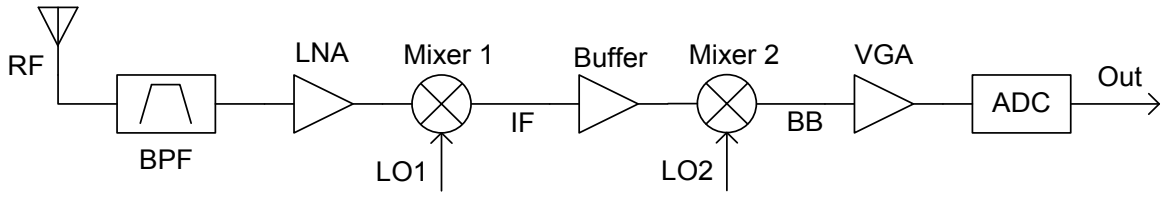
RF Frequency	24.001 GHz ～ 24.03 GHz
LO Frequency	24 GHz
TX Output Power	0 dBm
TX Output P1dB	7 dBm
RX Gain	>30 dB
RX Noise	<10 dB
RX Input P1dB	>-35 dBm
LO Phase Noise	-90 dBc/Hz @ 1 MHz
Power Consumption	TX mode: <100 mW RX mode: <100 mW
LO-RF Isolation	>30 dB
TX-RX Isolation	>60 dB
Out of band rejection	>50 dB

2.5 Front-End Architecture

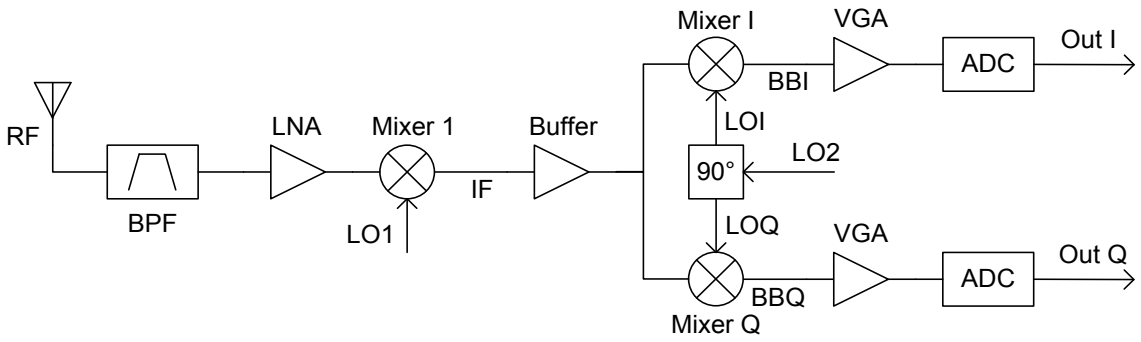
Unlike communication transceivers operate at RF frequencies, the radar transceiver at 24 GHz has several special characteristics. Firstly, at 24 GHz the performances of active and passive components are not comparable with these at lower frequencies; therefore, how to maximize the component performance and reduce the signal loss in and between the components become serious issues. Secondly, at 24 GHz, the mutual interaction and cross inference between different components are much more influential than lower frequencies. Thirdly, the modulation scheme of the radar transceiver is quite different from communication transceivers, therefore the system architecture is also different.

The receiver converts the received RF signal to a usable form, usually a digital signal. The most classical architecture for radio receivers are the super-heterodyne receiver [22]. The super-heterodyne receiver converts the received signal to IF signal through frequency mixing, The IF signal is easier to be processed than the RF signal, and it is processed by other components and converted to a digital-form.

A typical super-heterodyne receiver for millimeter-wave applications is shown in Fig. 2.6(a). The received signal is filtered by a band-pass filter to get the RF signal at the required band, then it is amplified by an LNA and mixed with a LO signal LO1 in the mixer. The converted IF signal is usually at a lower frequency. Then the IF signal is amplified by a buffer amplifier and mixed with another LO signal LO2 in the second mixer. The converted signal is identical to, or very close to the carrier frequency of the baseband signal. Then it is amplified by a VGA and then converted to digital signal through an ADC.



(a)



(b)

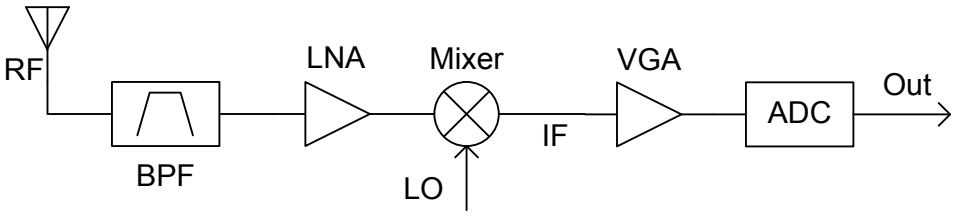
Fig. 2.6 Heterodyne receiver architectures
(a) non-quadrature receiver; (b) quadrature receiver

A more common realization of the receiver is based on the quadrature architectures. Quadrature receivers have many advantages upon the non-quadrature receivers. Firstly, it provides possibility for image rejection. Therefore the frequency of the channel of the received signal will not be mixed with the signals from other channels. It also reduces the overall noise of the receiver. Secondly, quadrature receivers are frequently used in Phase Shift Keying (PSK) or Frequency Shift Keying (FSK) modulation schemes because they are easy to demodulate these signals. Fig. 2.6(b) shows the schematic of an IQ-heterodyne receiver. The RF signal is filtered by the band-pass filter, amplified by the LNA, mixed with LO1 through a mixer and an IF signal is generated. The IF signal is then divided into I-mixer and Q-mixer. In the IQ mixers the IF signal is mixed with the 90 degree phase shifted LO2 signal. Then the output BB signal is also 90 degree phase shifted. The output BB signal is then amplified by the VGA and converted to digital signal through an ADC.

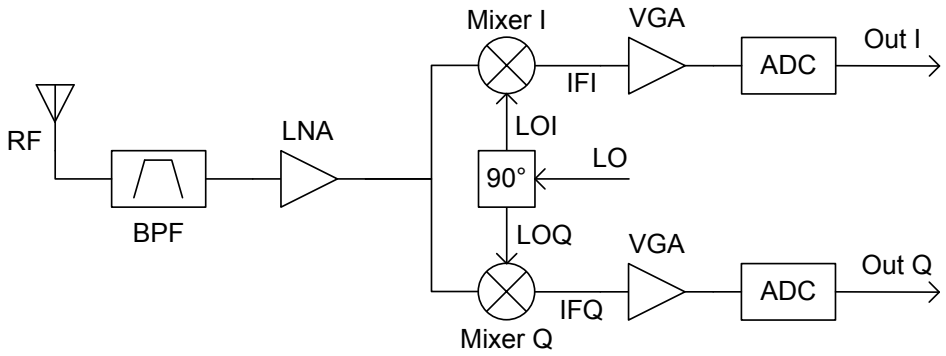
The heterodyne structure is frequently used due to the following reasons. Firstly, the image rejection could be easily realized therefore the frequency channel crosstalk could be minimized. For RF signals which work at high frequency, the quadrature generation can be very difficult and not reliable. Secondly, as the RF frequency is different from the LO frequency, the heterodyne receiver avoid to amplify the oscillator leakage signal. Thirdly, the oscillator phase noise does not have a huge influence on the system performance, otherwise it might directly add to the flicker noise of the baseband signal.

The disadvantages of heterodyne structure are also obvious. The heterodyne receiver requires more circuit building blocks. A complex frequency plan makes the PLL design complicated. It results in more power consumption as well as more chip area requirement.

To overcome the disadvantages of the heterodyne receiver, the homodyne receiver is implemented as an energy/chip-area efficient choice. It is becoming popular these years. Sometimes it is also called direct conversion receiver as it direct convert the RF signal to the IF signal. Compared to the heterodyne receiver, the homodyne receiver has only one LO frequency. Thus, the number of building blocks as well as the power consumption is minimized. The design of the PLL is also simplified as there is only one LO frequency. However, the design of mixer in a homodyne receiver is relatively difficult. Various problems such as flicker noise, DC offset and IIP2 raises when IF is very small. Chapter 5 discussed the detailed design consideration of mixers in homodyne receivers. Homodyne receiver has two categories, low-IF and zero-IF receiver. The low-IF receiver has a low IF frequency but the IF band does not reach zero while the zero-IF receiver reaches zero frequency.



(a)



(b)

Fig. 2.7 Homodyne receiver architectures
(a) non-quadrature receiver; (b) quadrature receiver

Fig. 2.7 shows the architectures of homodyne receivers. Shown in Fig. 2.7(a) is a non-quadrature receiver. The RF signal is received by the antenna and filtered by the band-pass filter, then amplified by the LNA and mixed with the LO signal directly in the mixer. The generated low-IF or zero-IF signal is amplified by the VGA and converted to digital signal by the ADC. Fig. 2.7(b) shows a quadrature homodyne receiver. The difference is that the RF signal amplified by the LNA is mixed with the I-Q LO signal and generated I-Q IF signals. The generation of quadrature LO signal is difficult at higher frequencies. Considering this, the design of quadrature homodyne receivers becomes difficult at higher frequencies. However, the quadrature receiver is easy to measured input signal magnitude and phase at the same time.

For low power wireless localization receivers designed in this thesis, the low-IF homodyne receivers are chosen for the reasons described below:

Firstly, the power consumption and chip area could be minimized as LO signal is only required at a single frequency. Only LO generation circuit is required and the receiver chain is simpler than heterodyne receivers.

Secondly, the signal cross-talk and LO leakage in homodyne receivers can be reduced by careful circuit design. Therefore the heterodyne receiver architecture is not required.

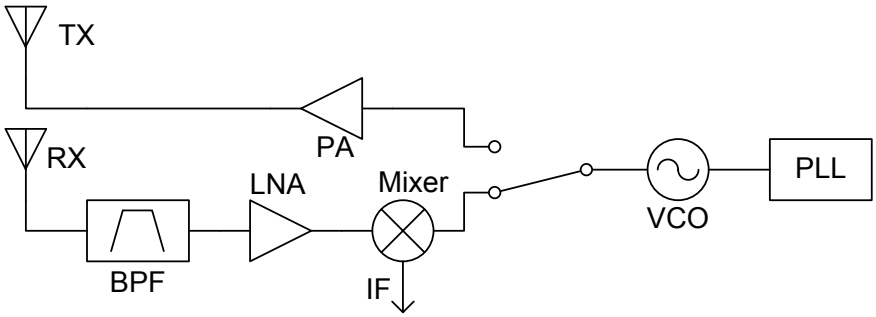
Thirdly, the low-IF receivers do not have the problems such as DC offset or large flicker noise for zero-IF receivers.

Usually, in frequency modulated transmitters, the signal is modulated through the PLL. Various PLL modulation methods, including open loop and close loop modulation methods, are discussed in details in [23]. In FMCW systems, like in other frequency modulated systems, the ramp-signal is generated inside the PLL. For the transmission, the ramp signal is direct amplified by the PA and send to the antenna. For the receiver, the received signal is mixed with the ramp signal in the mixer, where a low-frequency IF signal is generated. The low-frequency signal could be amplified properly through a variable gain amplifier and send to FFT to analyze it at frequency domain.

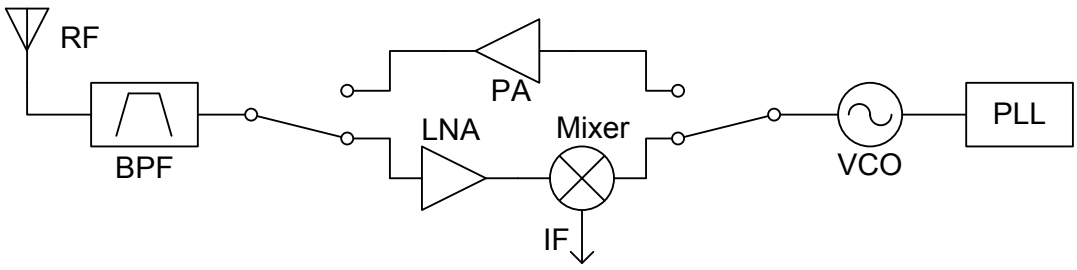
Fig. 2.8 (a) shows the block diagram of a dual-antenna FMCW transceiver. A switch is added between the VCO and the mixer/PA to minimize the LO loss and to improve the TX/RX isolation. The switch can be replaced by a power divider or LO buffers. If a

Wilkinson divider is implemented, a part of the receiving signal will be lost. Considering that at higher frequencies the loss is also higher (at 24 GHz normally 2 dB), the Wilkinson divider simply brings too much loss to the system, therefore it is not recommended. The LO buffers are able to compensate the insertion loss but consumes too much power, therefore they are also not recommended in a low-power system. The switch provides a low-loss and power-efficient solution.

In the receiving mode, the TX is switched off and the RX is switched on. The received signal is filtered by the bandpass filter, amplified by the LNA and mixed with the VCO signal and generate the IF signal. In the transmitting mode, the TX is switched on and the RX is switched off, the FMCW signal is directed amplified by the PA and transmitted to the TX antenna. A state-of-the-art 24 GHz FMCW CMOS transceiver based on this configuration can be found in [24].



(a)



(b)

Fig. 2.8 FMCW transceiver architectures
(a) dual-antenna transceiver; (b) single-antenna transceiver

Fig. 2.8(b) shows a single-antenna topology of the FMCW transceiver. An additional TX/RX switch is inserted between the antenna and the PA/LNA. By turning this switch on and off, the transceiver could be switched between ON and OFF mode. In this case, the insertion loss and the isolation of the switch have a big impact on the transceiver performance. As the insertion loss degrades the noise figure of the receiver and the output power of the TX, the switch reduced the link budget of the transceiver by 2 times of its insertion loss in dB. The leakage of the RX signal to the TX channel is not a big problem, but the leakage of the TX to the RX signal surely will reduce the sensitivity of the receiver. As TX signal is much higher than the RX signal, the sensitivity degradation might have a big impact. Therefore the switch should be carefully designed to minimize the insertion loss and maximize the isolation. Since previously MOSFETs are considered as high-loss and low cut-off frequency devices, they are not recommended as TX/RX switches. However, recently there is a trend to design high-performance low-loss switching circuits in CMOS technologies. Chapter 6 will be focus on the design of high performance CMOS switches.

In the LOWILO project the single antenna topology is chosen over the dual-antenna topology as it is more integrated. Besides, as for secondary radars the transmission and reception do not happen at the same time, hence the requirement of TX/RX isolation is not high which makes the single antenna topology a realistic choice.

The single channel FMCW transceiver has some drawbacks in the application. Therefore sometimes multi-channel transceiver is implemented. For example, in local positioning, the position of the device should be in the middle of several reference nodes. In cases that the device is far from the reference nodes, the space resolution of the device could become very poor. In order to overcome this problem, the angle of arrival (AOA) method is often used in these applications. The AOA method uses multiple antennas which has a fixed space between adjacent ones. As the angle of the input signal varies, the antennas are able to detect the phase difference. By solve the phase differences between the signals, the direction of the reference could be computed. Multi-channel receiver is especially suitable for the AOA method.

In some other applications, multi-channel receiver is required for local positioning as the device is a large device with many degrees of freedom. For example, in the intelligent factory,

such as in fork-lifts, cranes or robotic arms, two or more channel receivers are required as a single-channel receiver cannot provide sufficient positioning information.

Multi-channel receiver has another advantage as it can improve the SNR of the receiver. Therefore the space resolution/angle resolution can also be improved. The details are well discussed in [21]. The reliability of a multi-channel receiver is also higher than a single channel receiver. In case one of the channels is broken due to electrical or mechanical reasons, the performance of other channels is not influenced.

Fig. 2.9 shows the architecture of a dual-channel transceiver chip. The transmitting and receiving part is quite similar to the single-channel transceiver. The only difference is that two receiving channels are used instead of one channel. This implementation might also introduce several problems, such as cross-talk between the channels, LO degradation and LO mismatch, which should be considered in the designing. In Chapter 8 a four-channel fully-integrated transceiver will be presented, which is a further implementation of this topology.

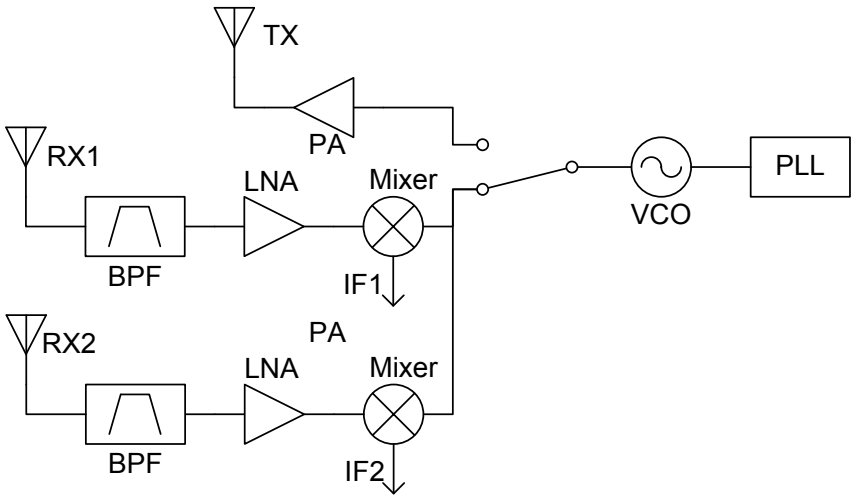


Fig. 2.9 Dual-channel FMCW transceiver chip architecture

The bandpass filters used in this process is off-chip surface-acoustic-wave (SAW) filters, as they could provide the required out of band rejection of 50 dB which is very difficult to realize at 24 GHz on chip.

2.6 Conclusion

Various topics have been discussed in this chapter. A brief overview of wireless sensor network technology and wireless localization technology is given in the beginning, then the content and goal of the project “LoWiLo” is presented. The basics of FMCW radar is discussed, then a comprehensive comparison between FMCW radar and FMCW secondary radar is given and the numerical analysis of the link budget is presented. After that, a discussion regarding different system topologies of transceivers and receivers are presented and several examples are given to demonstrate these topologies in FMCW radar systems. From this chapter, the system considerations of the thesis are presented and an overall view of the complete work is demonstrated.

Chapter 3
Process Technology

The CMOS process used for the transceiver design is IBM 8RF-DM 0.13 μm CMOS process [25]. This process targets the low-cost high performance wireless applications such as Bluetooth, WLAN, cellular handsets and GPS. Eight metal stacks are provided, as shown in Fig. 3.1. Three thin copper layers in the bottom, M1, M2 and M3, provide bottom metal grounding, as well as transistors and varactors gate biasing connections. Two thick copper layers in the middle, MQ and MG, are suitable for the IF transmissions. Three thick RF-top metals, LY(Al), E1(Cu) and MA(Al), are suitable for high-Q inductors and low loss transmission lines.

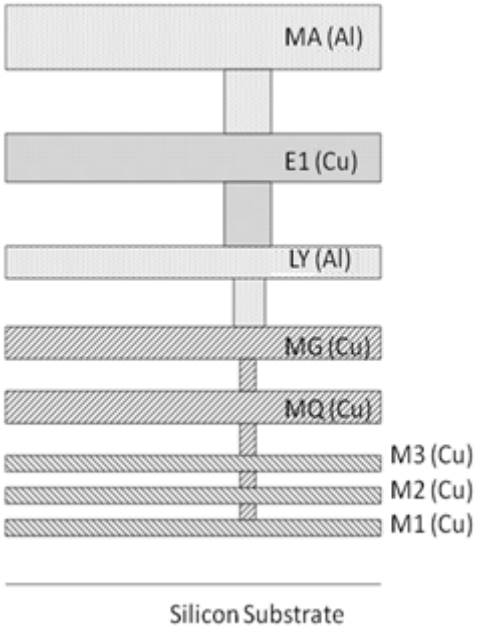


Fig. 3.1 Metal stack configuration of IBM 8RF-DM

Different kinds of MOSFET transistors are available in this technology. The designer can chose the proper kind for different purposes. The transistors which do not require additional masks are thin oxide surface channel NMOS and PMOS transistors. These transistors have the highest cut-off frequency in the process. For NMOS transistors the maximum cutoff frequency is around 90 GHz, while for PMOS transistors the maximum cutoff frequency is around 30 GHz. Therefore they are very suitable for RF circuits. Another type of RF transistors is thin oxide surface channel low power NMOS and PMOS transistors. These transistors have relative higher threshold and consume less power than the standard MOSFETs. The cut-off frequency of these is similar to the standard ones. Therefore the low power MOSFETs are more suitable for low-power RF circuits.

All thin oxide NMOS have the option to implement a triple N-well to isolate the substrate of NMOS from the P-substrate. The triple N-well has several advantages when implemented in RF/analog circuits. On one hand, it reduces the leakage of signal to substrate; therefore the signal loss on the transistor substrate is reduced. On the other hand, it isolates the transistor from substrate noise; therefore unwanted noise in the signal path is limited. Because of the above reasons, triple N-well transistors are ideal for the RF/analog circuits which are sensitive to substrate coupling such as VCO or switches. For PMOS the N-well is already existed, therefore triple-well is not needed.

Another kind of thin oxide surface channel MOSFET is low-threshold MOSFET. The threshold voltage of these MOSFET is much lower compared with the standard MOSFET. It can be used in special biasing circuits or other specified analog circuits. Thin oxide zero-threshold NFET is also available; for analog application it can be used in some certain blocks such as wake-up circuits.

In this process, there are several types of thick oxide surface channel MOSFET. Unlike the thin oxide MOSFETs which operates at 1.2 V supply voltage, the thick oxide MOSFETs need 2.5 V or 3.3 V to operate. There are thick oxide NFET and PFET for native 2.5 V operations which target for I/O and analog applications. There are also 3.3 V thick oxide NFET and PFET for 3.3 V I/O or analog circuits.

High performance capacitors are implemented between MA layer and E1 layer. They are single Nitride MIM capacitors and dual Nitride MIM capacitors. The capacitance density of the dual MIM capacitor is two time of that of the single MIM capacitor. These capacitors have

high quality factor and high accuracy at high frequencies. They could be used as RF-coupling capacitors or feedback capacitors. On the contrary, the MOM capacitors, which utilize the coupling of metal lines between M1, M2 and M3 layer, have lower quality factor and lower accuracy, therefore it is more suitable for insensitive applications such as ground capacitors.

Several kinds of resistors are available and cover a wide range of resistances for different applications. These are N-well resistor, N+ diffusion resistor, P+ polysilicon resistor, metal resistors and other resistors using certain masks. The designer can choice the proper ones with acceptable accuracy and chip area consumption.

The inductors provided by the design kit are mainly on the top metal layers (MA and E1). As these metals are far from the substrate, the quality factor of these inductors could be maximized. Self-designed inductors can also be used in this process. As the inductors for 24 GHz transceiver are usually much smaller than these provided by the design kit, self-designed inductors are implemented massively in this work.

Other passive components provided by the design kits are inductive lines, transmission lines and bondpads. An inductive line is a single top metal (MA) lines with meshed substrate. It could be used as a small inductor. For certain situations, such as the source degeneration, where the inductance are too small to be realized by an inductor coil, the inductive lines should be implemented. Single or coupled shielded transmission lines are used as the interconnect lines. They could be on any metal layer except M1. Both ground and side-shield are introduced to reduce the coupling of the transmission line and other components. In this project most RF interconnects are placed on top metal to ensure the best transmission performance. Different types and sizes of bondpads are also available in this process. Special RF pads are used for the input and output of the RF signal.

Forward biased diodes are supported, as well as the bipolar junction transistors. For analog band-gap designs the bipolar junction transistors are required. Schottky barrier diodes are also provided optionally, which could be used in some special applications such as wake up circuits.

Thin oxide MOS varactor can be used in VCOs to change the tank capacitance continuously. Compared with the varactors based on standard MOSFETs, the thin oxide MOS varactors have much larger voltage tuning range. Thin oxide MOS varactors and hyperabrupt varactors are other alternatives of varactors.

Electronic fuses are also supported by the process. The electronic fuses are mainly for digitally trimming the analog circuits to overcome the problems induced by the process variation.

As various types of components are supported by the process, the designer is able to choose the most proper one from these components. For example, for the amplifying transistors in the 24 GHz RF amplifiers, the NMOSs are chosen as their cut-off frequency (90 GHz) is much larger than the PMOS transistors (30 GHz). The cut-off frequency of PMOS transistors is too close to 24 GHz to provide sufficient gain. The detailed discussions regarding active and passive components are presented in the next chapter.

The wafer size for this process is 8 inches and the die thickness is 250 μm. The substrate resistance is 1~2 Ω-cm, which is a major drawback of the CMOS technology compared to other high frequency technologies such as the SiGe BiCMOS and GaAs HBT technology. The substrate resistance becomes more and more influential as operation frequency increases [26]. At 24 GHz, not only the MOSFETs are influenced by the distributed substrate resistance, but also the passive components are affected by the substrate coupling and eddy currents in the substrate. Therefore, lots of efforts have been done to minimize the impact of substrate coupling during the circuit design.

Chapter 4
Component Modelling and Design

4.1 Introduction

MMIC designs in standard CMOS are difficult due to the high-loss of silicon substrates. As the frequency becomes higher, the design becomes even more difficult. High operation frequencies, such as 24 GHz, are closer to cut-off frequency of the process (for 0.13 μm CMOS process the cut-off frequency of NMOS transistors is 90 GHz), which limits the transistor gain. Besides, the substrate loss also becomes larger as frequency increases, which results in low Q-Factor (Quality Factor) of the passive components.

As the power consumption of the designed circuits is required to be minimized, more problems should be considered. For example, to minimize the drain-source current the transistor size should be minimized, while in that case the MOSFET model becomes inaccurate.

To fully analyzing these problems and giving proper solutions to them, the process and the component modeling which related to the circuit design will be decently discussed in this chapter, including the CMOS processes, active and passive component models and the complete design procedure.

This chapter is organized as below. In section 4.2 the MOSFETs implemented in this work is presented. The equivalent circuit models and compact models of these MOSFETs are introduced. The advantages and disadvantages of different compact models are compared. Section 4.3 presents the passive structures used in this work. The influences of skin effect on passive structures are analyzed, especially at high frequency. In section 4.4 the design of baluns and transformers is presented. Different balun structures are compared and the design procedures and considerations are analyzed in detail. Section 4.5 concludes this chapter.

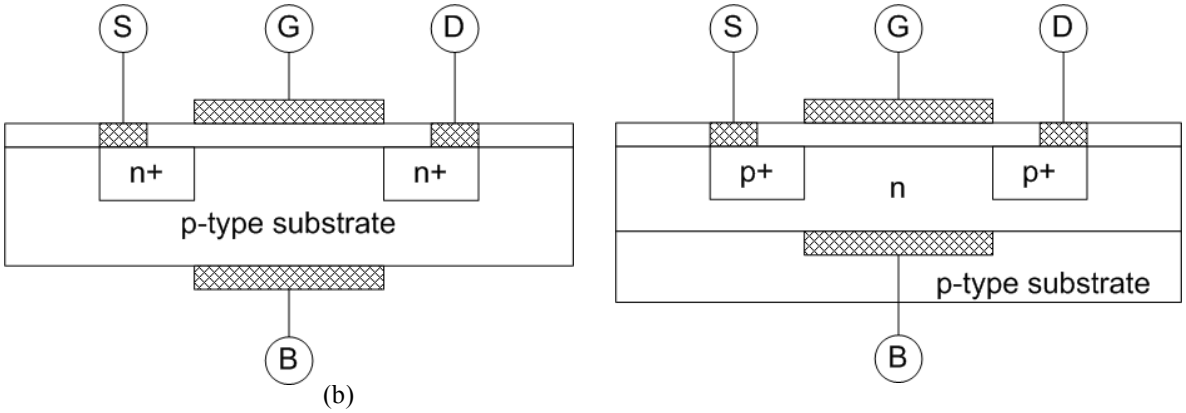


Fig. 4.1 Cross section of (a) NMOS (b) PMOS

4.2 MOSFET Models

4.2.1 MOSFET Basics

MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is the basic active component used in CMOS technologies for amplifying and switching signals. It also called IGFET (Insulated-Gate Field-Effect Transistor) or MISFET (Metal–Insulator–Semiconductor Field-Effect Transistor) sometimes, although the definitions are slightly different. Cross section views of NMOS and PMOS are shown in Fig. 4.1. In IBM 8RF technology, as well as many other CMOS technologies, the gate material is a layer of polysilicon rather than metal.

The MOSFET operation principles are well presented in many books [27]-[29]. In short, an inversion layer, which is called a channel, is formed by proper gate biasing V_{gs}. The drain current I_D depends on the gate biasing V_{gs} and drain biasing V_{ds}. Based on the V_{gs} and V_{ds} there are three operation modes. Take NMOS transistors as an example.

The cutoff mode, is the situation when $V_{gs}<V_{th}$ (V_{th} is the threshold voltage). The current I_D decreases exponentially with the decrease of V_{gs}. Although small leakage current exists, I_D is very small compared with the other modes.

$$I_D \approx 0 \tag{4.1}$$

The linear region (ohmic triode mode), is the situation when $V_{gs}>V_{th}$, and $V_{ds}<V_{gs}-V_{th}$. Here the transistor works as a resistor. I_D increases linearly with V_{gs} and V_{th}.

$$I_D = \mu_0 C_{ox} \frac{W}{L}\left((V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^{\ 2}}{2}\right) \tag{4.2}$$

Here μ_0 is the charge-carrier effective mobility, C_{ox} is the gate oxide capacitance per unit area, while W and L are the transistor width and length, respectively.

The saturation mode is the situation when $V_{gs}>V_{th}$, and $V_{ds}>V_{gs}-V_{th}$. Here the channel is fully created and I_D is majorly depended by V_{gs}.

$$I_D = \frac{\mu_0 C_{ox}}{2}\frac{W}{L}(V_{gs} - V_{th})^2(1 + \mathrm{k}V_{ds}) \tag{4.3}$$

Here k is the channel length modulation parameter.

The I-V curve of a NMOS transistor in the IBM 8RF technology is shown in Fig. 4.2. The transistor length is 130 nm. The total transistor width is 30 μm. The number of finger is 10. This transistor is a typical transistor used in the 24 GHz CMOS transceiver.

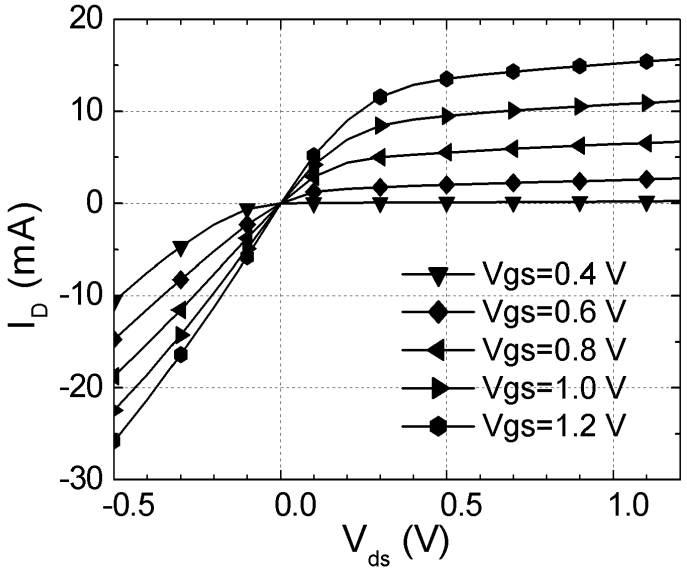


Fig. 4.2 I-V curve of a NMOS transistor

This figure clearly shows that V_{th} of the transistor is around 0.5 V. For the $V_{gs}>V_{th}$ situations, the saturation region is the region where $V_{ds}-V_{gs}>V_{th}$, and the linear region is where $V_{ds}-V_{gs}<V_{th}$. The linear region extends to the $V_{ds}<0$ case, where drain and source swapped, and $|V_{gs}|$ is always larger than $|V_{ds}|$. Although $V_{ds}<0$ case does not exist for the transistor DC solutions, it helps to explain the RF performance of the transistor when $V\approx 0$.

The MOSFET transconductance G_m and output conductance G_d are defined as

$$G_m = \frac{\partial I_D}{\partial V_{gs}} \tag{4.4}$$

$$G_d = \frac{\partial I_D}{\partial V_{ds}} \tag{4.5}$$

In the circuits, the MOSFETs have two basic functions: amplifying and switching. When a MOSFET amplifies, it works in the saturation region. In the saturation region, from Formula 4.3, G_m and G_d can be expressed as

$$G_m = \frac{2I_D}{V_{gs} - V_{th}} \tag{4.6}$$

$$G_d = \mathrm{k} I_D \tag{4.7}$$

Considering R_L as the load of the transistor, the load impedance is the shunt of R_L and R_{out}, here R_{out} is the reverse of g_{ds}. For a low frequency input signal V_{in}, the output signal V_{out} can be calculated as

$$\frac{V_{out}}{V_{in}} = G_m (R_L \| R_{OUT}) \tag{4.8}$$

If the value of V_{out}/V_{in}es higher than 1, the transistor has a voltage gain. If $R_{out}>>R_L$, the voltage gain is approximately the product of g_m and R_L.

When a MOSFET switches, V_{gs} varies and the MOSFET is switched between cutoff and linear region. The transconductance of the MOSFET changes between 0 and a specific value.

4.2.2 Equivalent Circuit Models

Small signal equivalent circuit MOSFET models are essential to understand the physics of the transistors. The well known lumped-element model is shown in Fig. 4.3(a). Besides of the transconductance G_m and output conductance G_{ds}, it consists of the source, drain and gate resistances, and three coupling capacitances between source, drain and gate. These model parameters are functions of frequency. As frequency changes the parameters might vary a lot.

In [30], three new parameters were introduced and the model is shown in Fig. 4.3 (b). The newly introduced parameters are the channel charging resistance r_i, the transconductance delay τ and the gate resistance $R_{g,e}$ and $R_{g,i}$. The channel charging resistance accounts for the channel charge cannot instantaneously response to changes of the gate-source voltage. The transconductance delay accounts for that the transconductance cannot instantaneously response to changes of the gate-source voltage. The gate resistance is split into an external part $R_{g,i}$ and an intrinsic part $R_{g,e}$. The external part comprises the contact resistance to the gate material as well as any resistance prior to entering the intrinsic portion of the gate.

The component parameter of the lumped-element models could be extracted to further understanding the MOSFET performance. Fig. 4.3(c) illustrates the lumped element model used for parameter extraction [31]. It incorporates a substrates network to characterize the substrate effect at high frequency and a transcapacitance to ensure that the small signal model maintains charge conservation. C_m here equals to C_{dg}-C_{gd}. The parameter extraction includes two steps. Firstly, the terminal resistances are extracted. Setting V_{gs} to 1.2 V and V_{ds} to 0 V, Port1 at G, Port2 at D and the source grounded, R_s, R_d, R_g, C_{gs} and C_{gd} could be extracted from the Z-parameters.

$$R_s = \mathrm{Re}(Z_{12}) \tag{4.9}$$

$$R_g = \mathrm{Re}(Z_{11} - Z_{12}) \tag{4.10}$$

$$R_d = \mathrm{Re}(Z_{22} - Z_{12}) \tag{4.11}$$

$$C_{gs} = C_{gd} = \mathrm{Im}(Z_{12}) \tag{4.12}$$

Secondly, the intrinsic parasitic components for a given biasing point could be extracted. The extracted gate resistance is de-embedded from Z-parameters. The source and drain

resistance are neglected since the poles due to the source and drain resistance are at a higher frequency than the transit frequency. By performing Y-parameter analysis, the intrinsic parameters of the MOSFET could be extracted as:

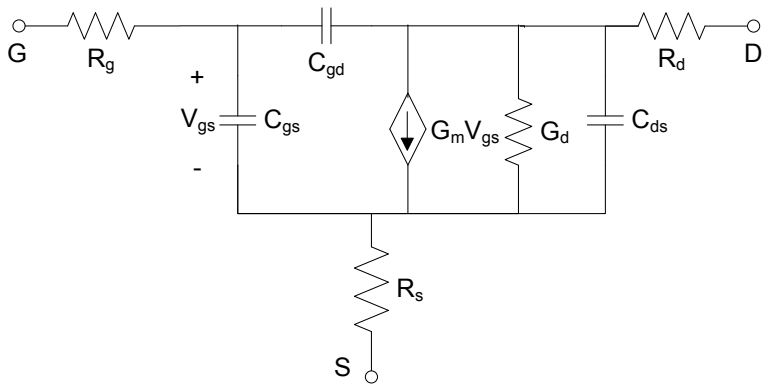
$$G_m = \mathrm{Re}(Y_{21})\big|_{\omega=0} \tag{4.13}$$

$$G_d = \mathrm{Re}(Y_{22})\big|_{\omega=0} \tag{4.14}$$

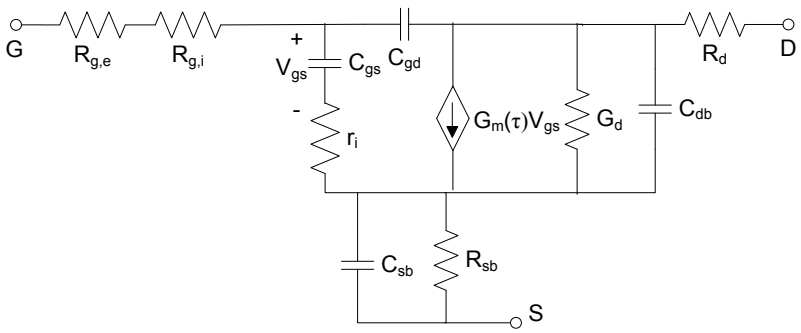
$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \tag{4.15}$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})}{\omega} \tag{4.16}$$

$$C_{dg} = -\frac{\mathrm{Im}(Y_{21})}{\omega} \tag{4.17}$$



(a)



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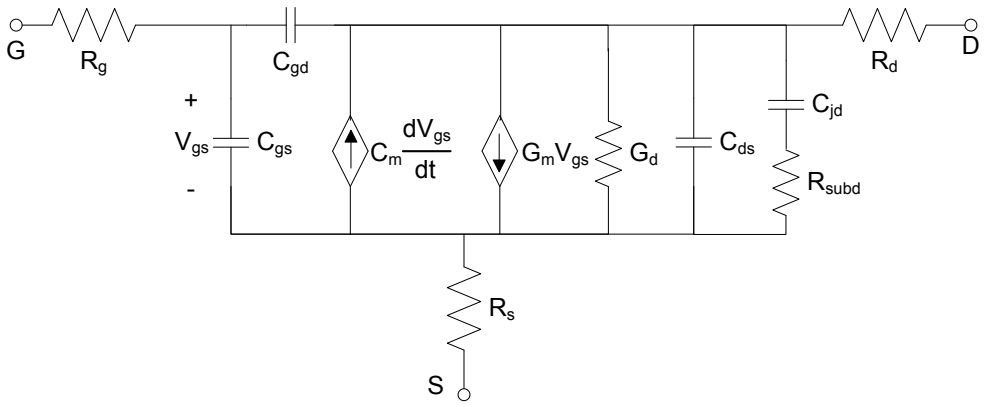


(c)

Fig. 4.3 Schematics of the MOSFET lumped-element models (a) Conventional small-signal lumped-element model of a MOSFET; (b) Small-signal lumped-element model of a MOSFET proposed by T. Manku; (c) The lumped element model for parameter extraction

The substrate parameter R_{subd} and C_{jd} could be extracted from Y_{sub}.

$$Y_{sub} = Y_{22} - g_{ds} - j\omega C_{sd} - j\omega C_{gd} \tag{4.18}$$

By plotting $\omega^2/\mathrm{Re}(Y_{sub})$ against ω^2, the substrate resistance R_{subd} can be obtained from the slope:

$$\frac{\omega^2}{\mathrm{Re}(Y_{sub})} = \omega^2 R_{subd} + \frac{1}{R_{subd} C_{jd}^{\ 2}} \tag{4.19}$$

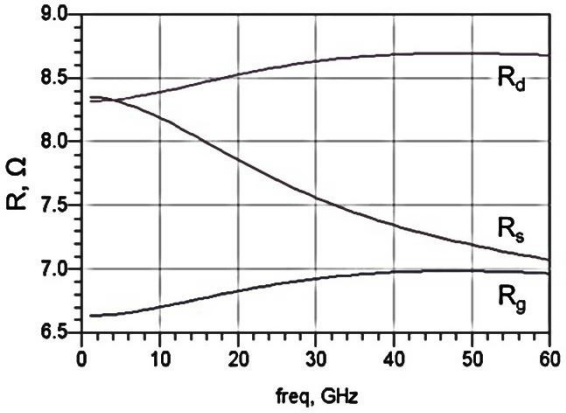
The drain junction capacitance C_{jd} is expressed by:

$$C_{jd} = \left(\frac{\omega^2 R_{subd}}{\mathrm{Re}(Y_{sub})} - \omega^2 R_{subd}^{\ 2}\right)^{-1/2} \tag{4.20}$$

A typical NMOS transistor is taken as an example to perform the parameter extraction. The transistor is with 10*3 μm width and 130 nm length. The drain-source biasing is 1.2 V and the gate-source-biasing is 0.6 V. The extracted terminal resistances are shown in Fig. 4.4(a). G_m and G_{ds} are shown in Fig. 4.4 (b). It should be noticed that G_m and G_{ds} at 0 GHz is defined by (4.13) and (4.14), which are 21.36m and 1.132m, respectively. The extracted capacitances are

shown in Fig. 4.4 (c) and (d). The $\omega^2/\mathrm{Re}(Y_{sub})$ against ω^2 plot is shown in Fig. 4.4 (e), from this figure the substrate resistance R_{subd} is calculated as 514 Ω. Fig. 4.4(f) shows the extracted C_{jd} of the MOSFET.

From the extracted parameters the lumped-element model of the transistor is shown in Fig. 4.5. Here V_{gs}=0.6V and V_{ds}=1.2 V. All the extracted parameters are calculated as frequency at 24 GHz. Based on the extracted lumped-element model and the BSIM4 model supported by the foundry a comparison of S-parameter is presented in Fig. 4.6. It can be seen that there are small variations for S_{11} and S_{22}. For S_{21} and S_{12}, the amplitude differences between the models are less than 1 dB and the phase differences are less than 10 degree up to 60 GHz.



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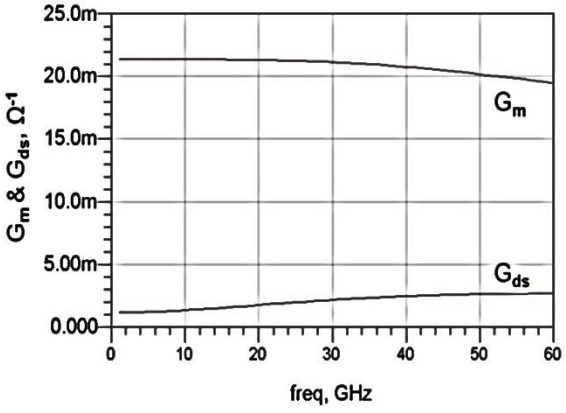

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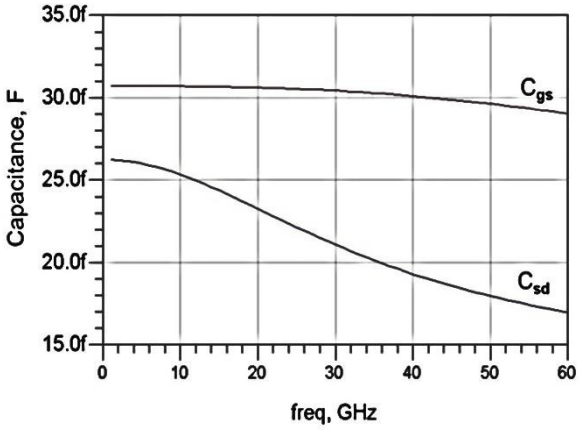

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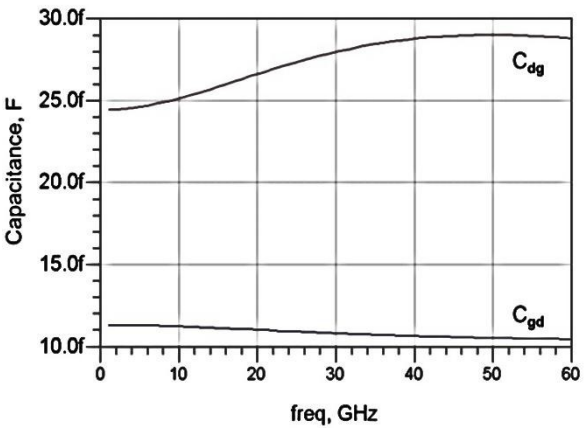

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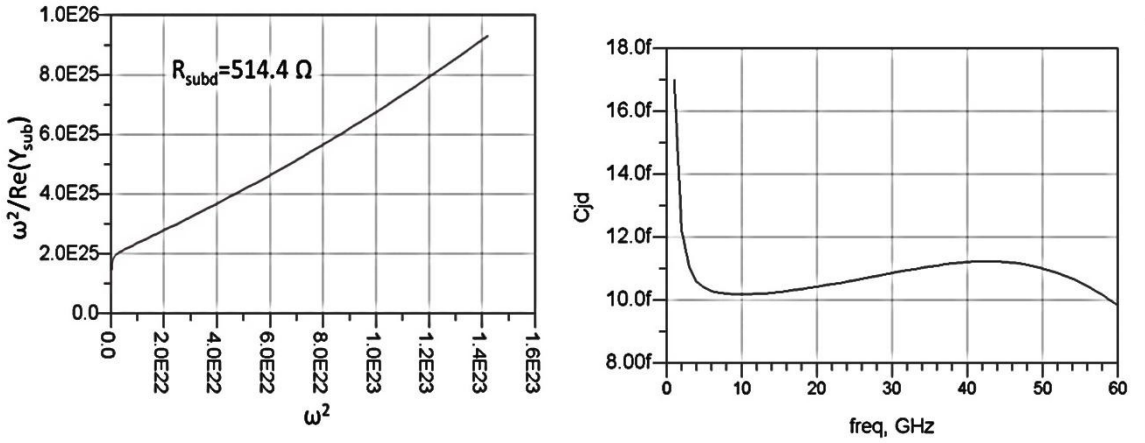


(e) (f)

Fig. 4.4 Extracted lumped-element model parameters of the selected NMOS transistor

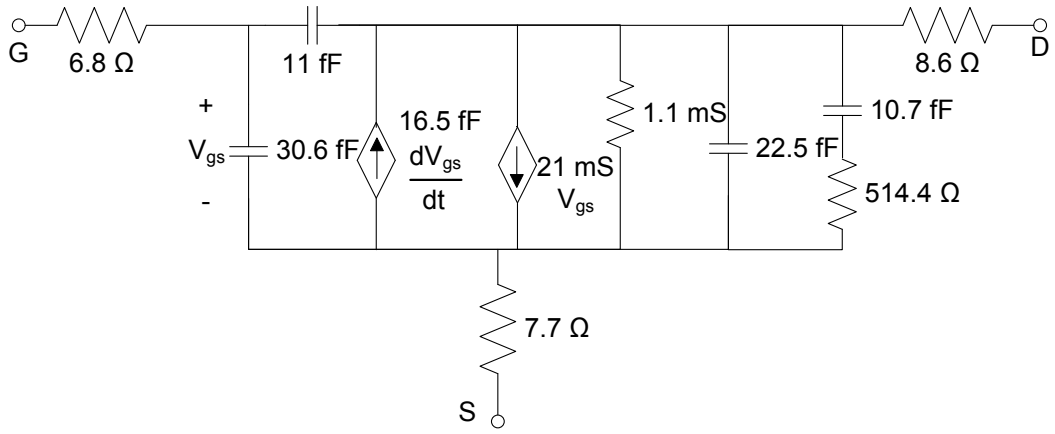


Fig. 4.5 Lumped-element model of the selected NMOS transistor with V_{gs}=0.6V and V_{ds}=1.2 V

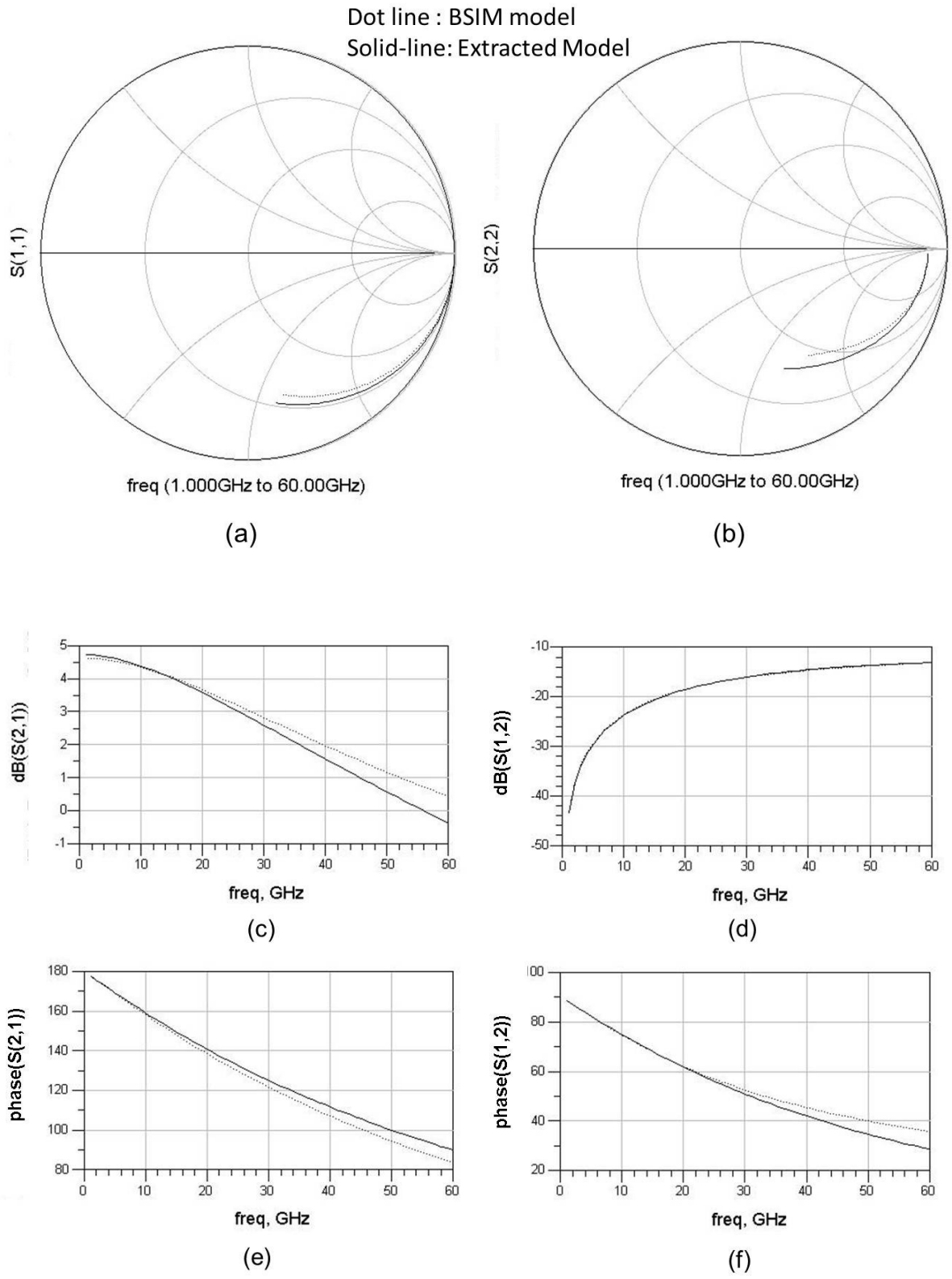


Fig. 4.6 S-parameter comparisons of the extracted lumped-element model and the BSIM model provided by the PDK. Dark line: Extracted model; Light line: BSIM model

In conclusion, the equivalent circuit models are able to model the microwave characteristics of MOSFET accurately with specific V_{gs} and V_{ds}. From the equivalent circuit models, the key intrinsic and external parameters of the MOSFET could be extracted, result in a better understanding of the MOSFET component.

4.2.3 Compact Models

Compact MOSFET models play an important role in contemporary CMOS technologies. For a successful CMOS design, it is essential to select a proper MOSFET model that characterizes the transistor performance accurately. As the devices become smaller and the desire frequencies go higher, the compact modeling, the accuracy of the models and their compatibility with EDA tools become important issues.

Among the various available MOSFET models, the BSIM models [32], PSP model [33],[34] and HiSIM models [35] are selected by the Compact Model Council [36] as standard models for electronic designs. In this section the three kinds of models will be discussed.

A. BSIM MODELS

BSIM model refers to Berkeley Short-channel IGFET Model. For standard MOSFETs, there are two types of BSIM models: BSIM3 and BSIM4.They are developed by the Device Research Group of the Department of Electrical Engineering and Computer Science, University of California, Berkeley and copyrighted by the University of California. BSIM models are used by most companies such as Intel, IBM, TI, TSMC, Samsung, Infineon, and so on [32].

The BSIM models are designed to accurately modeling the MOSFET behavior in deep sub-micron regions. As the devices scale down, many other MOSFET models implemented by the circuit simulators became inaccurate. The BSIM models are designed as an accurate and computationally effect MOS transistor model. Both the strong-inversion and weak-inversion components of the drain current expression are included in BSIM3. In BSIM4 the gate leakage current is also considered. The advantages of the BSIM models include a solid understanding of device physics, simple model formulation, easy to be expanded and

automated model parameter extraction [37]. The BSIM models are the most popular MOSFET models until now.

B. PSP MODEL

The PSP model has been developed by NXP Research (formerly part of Philips Research) and Arizona State University (formerly at Pennsylvania State University). Based on merging the best features of two surface-potential-based models, SP (developed at Pennsylvania State University) and MM11 (developed by Philips Research), it is the first surface-potential-based compact MOSFET model selected by the Compact Model Council.

Compared with the threshold-voltage based models, such as BSIM models, the surface-potential-based models could provide the physics-based modeling of all regions of operation and do not require additional approximations beyond those inherent in the charge-sheet models [38],[39].

Although PSP model is not widely implemented as the BSIM models, it is suggest that it is much accurate for higher-order than the BSIM model when the drain-source voltage is near zero, especially for the linear analysis.

C. HiSIM MODELS

HiSIM model refers to Hiroshima-university STARC IGFET Model. It is another type of surface-potential-model, which solves the surface potentials with an efficient physically correct iteration procedure, thus avoiding additional approximations which are required in the PSP model. It is also demonstrated that excellent model accuracy for higher-order phenomena is achieved by the HiSIM2 model [40].

D. MODEL COMPARISON

Recently a lot of researches have been carried on to compare these models. However, these comparisons might mean differently for foundries and for designers. For foundries, the accuracy of the compact modeling is of primary importance. TI has performed an evaluation

on PSP and HiSIM models and compared them with the existing BSIM4 model [41]. In this report, they concluded that neither model is ready to be a comprehensive BSIM4 model replacement. For example, both PSP and HiSIM do not have enough sub-threshold model scalability. Based on the evaluation TI prefers PSP over HiSIM for these reasons: firstly, PSP aligned more accuracy to long channel G_d; secondly, although both model have negative G_m problem, but PSP's G_m and its derivatives were better behaved; thirdly, they experienced fewer bugs/code issues with PSP.

For designers, although the model accuracy is an important consideration, other aspects, such as the simulation time, EDA software compatibility and foundry support should also be considered. A comparison between BSIM4 and PSP models will be described in the next session. Due to our experience, Spectre and ADS provide better support for BSIM4 model, rather than the PSP model. Since the BSIM4 formulation is much simple, the simulation time of BSIM4 model is also much less than the PSP model.

A comprehensive comparison of these models could be seen in Table 4-1. A detailed comparison between BSIM4 and PSP models based on measurement results are presented in the next section.

4.2.4 Comparison between BSIM4 and PSP models

Several studies have been implemented in comparing the BSIM4 model and the PSP model. In [42], the IP3 properties of the BSIM4 model and the PSP model are compared and briefly analyzed. In [43], various aspects of the PSP model are analyzed from Gummel symmetry to noise modeling, and some of the results are compared with the BSIM4 model. In this section, various parameters, such as DC performance, S-parameters, and IIP3 of the BSIM4 model and the PSP models are studied using the device models provided by the foundry. On-wafer measurements are carried out and the results are compared with the simulate results.

This section is organized as follows. In part A the MOSFET DC characteristics will be studied. The small signal properties of the MOSFET will be investigated in part B. In part C, the linearity performance of MOSFET will be analyzed based on BSIM4 and PSP models.

A. DC ANALYSIS

Two on-chip MOSFET transistor test structures with different widths and number of fingers are designed and fabricated using IBM 0.18 μm SiGe BiCMOS technology. The test transistor dimensions are 180 nm*3 μm*10 (MOSFET M1) and 180 nm*9 μm*20 (MOSFET M2). MOSFET M1 has a typical dimension of transistors in CMOS LNAs or down-convert ion mixers, and MOSFET M2 is typical for CMOS power amplifiers.

The chip micrograph of the transistor test structure is shown in Fig. 4.7. Short transmission lines are implemented to connect the pads and the transistor. The transistor gate is connected to "In" pad, while the transistor drain is connected to "Out" pad. In the measurements, Bias-Tees have been used in the input and output.

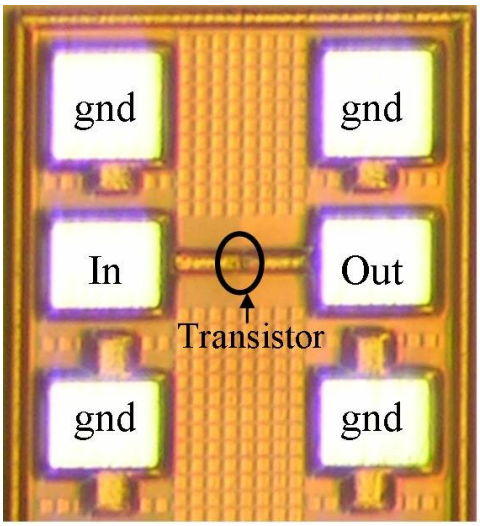


Fig. 4.7 Chip micrograph of a transistor test structure

The pads, transmission lines and metal via connections are fully EM simulated until 60 GHz using ADS Momentum. The PSP and BSIM4 models provided by the foundry are utilized and EM co-simulated.

In the DC analysis, while sweeping the bias voltage on the gate and drain of the transistor, the drain to source current is simulated and measured. Transconductance G_m, output conductance G_d, and its first order derivative G_{d2} are derived from the I-V curves. MOSFET G_m and G_d are critical parameters in CMOS RF circuit designs as they contribute to gain,

noise figure and linearity. They are calculated using the following formulae: $G_m = dI_{ds}/dV_{gs}$, $G_{d2} = dI_{ds}/dV_{ds}$.

The measured transconductance is derived from the I-V measurement results using the formula

$$G_m(V_{gs}) = \frac{I_D(V_{gs} + \Delta V_{gs}/2) - I_D(V_{gs} - \Delta V_{gs}/2)}{\Delta V_{gs}} \tag{4.21}$$

The simulated and measured G_m of M1 is shown in Fig. 4.8. Here V_{ds} is 1.2 V. From Fig. 4.8, it can be seen that the linear portion of the transconductance curve is between 0.5 V and 0.9 V. The calculated G_m value for the BSIM model has a higher slope in this region with respect to V_{gs} in comparison to the PSP.

As the PSP model is surface potential based, the body bias will reverse bias the junction diodes in the linear region. Hence, the transconductance is not explicit. When the G_m value saturates, the PSP model shows accuracy.

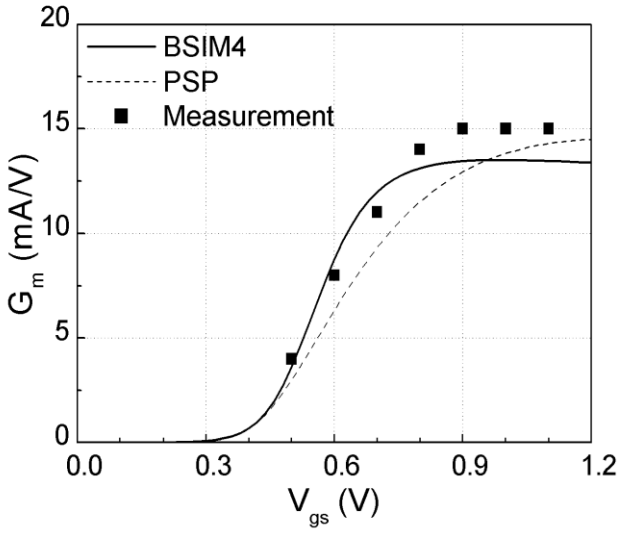


Fig. 4.8 Measured and simulated transconductance of M1

Table 4-1 Comparison of Compact MOSFET Models

	BSIM4	PSP	HiSIM
Scalability	Good	Not Good	Not Good
DC	Good	Good^{o}	Good^{o}
Small Signal	Good	Good^{o}	Good^{o}
Large Signal	Not Good	Good	Good
Noise	Not Good	N/A*	N/A*
Simulation Time	Short	Long	N/A**
Software Compatibility	Good	Not Good	N/A**
Support Foundries	Most Foundries	Several Foundries	Unknown

^{o} DC and small signal are not good at sub-threshold region, besides, for HiSIM model G_d is not accurate for long channel transistors.

*The noise characteristics of PSP and HiSIM model are not yet verified by us. The PDK we are currently using does not support HiSIM model, while for the PSP model the noise simulation has some software compatibility problem.

** The PDK we are currently using does not support HiSIM model. However, according to the TI evaluation, the PSP model has less bugs/code problems than HiSIM model, which hints that HiSIM model might have some software compatibility problem.

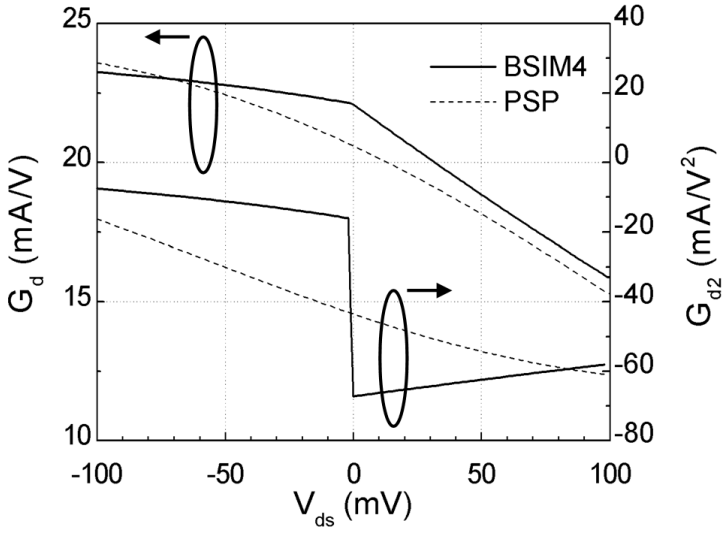


Fig. 4.9 Simulated G_d and G_{d2} of M1 when V_{ds} is close to zero

Fig. 4.9 shows the output conductance G_d of M1 and its first order derivative G_{d2} when V_{ds} is close to zero and V_{gs} equals to 1 V. From Fig. 4.9, it is shown that G_{d2} of the BSIM4 model is discontinuous when V_{ds} = 0 V, while G_{d2} of the PSP model is continuous at the same bias point. This is because that when V_{ds} = 0 V, only the first derivative is available in BSIM4 model while in PSP model the derivatives are up to 5th order [31].

The discontinuous of G_{d2} in BSIM4 model might bring a potential flaw in the MOSFET linearity calculations (IIP2 and IIP3). This is because both of these parameters are related to G_{d2} and G_{d3}. This is quite significant in some circuits, such as passive mixers or switches.

B. SMALL SIGNAL ANALYSIS

The small signal S-parameters of the test transistors are measured using HP 8510C Vector Network Analyzer. The load and source impedances are 50 Ω. The measured and simulated S-parameters are shown in Fig. 4.10. The presented measurement results are up to 40 GHz while the simulations are up to 60 GHz.

Fig. 4.10(a) shows the S-parameters of M1 when I_{ds} = 0.75 mA and V_{ds} = 1.2 V. Here V_{gs} of the PSP model is 0.623 V, while V_{gs} in the measurement and the BSIM model is 0.6 V. As

seen in the figure, S_{21}, the small signal gain of M1, shows the maximum variation. The gain of M1 is higher in the BSIM4 model than in the PSP model, while the measurement agrees with the BSIM4 model.

The intrinsic voltage gain of the transistor is given by G_m/G_d. Hence, the power gain is proportional to the square of G_m. As shown in Fig. 4.8, when the transistor works for V_{gs} around 0.6 V, G_m of the BSIM4 model is more accurate than G_m of the PSP model. This is responsible for the variation in the gain values.

However, the difference in the gain values between the measurement and simulation does not exist for high overdrive voltages (V_{gs}-V_{th}). This can be seen in Fig. 4.10(b), where the S-parameters of M1 for I_{ds} = 3 mA and V_{ds} = 1.2 V are presented. The results are obtained by setting the gate-source voltage to 0.86 V for the PSP model, and 0.8 V for the measurement and the BSIM model. In both of the above cases it can be seen that S_{11}, S_{12} and S_{22} have good agreements with the measurement results for the two models.

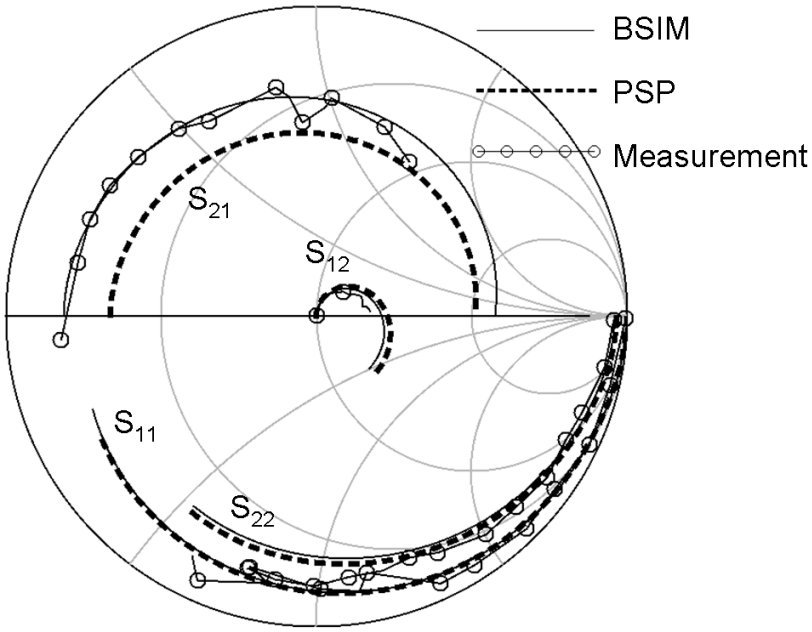
From the analysis above, it can be concluded that BSIM4 model shows reliable results for various bias points, particularly for gate voltages slightly above the threshold voltage. Such operating points are quite common for low power applications and for circuits like LNAs.

C. LARGE SIGNAL ANALYSIS

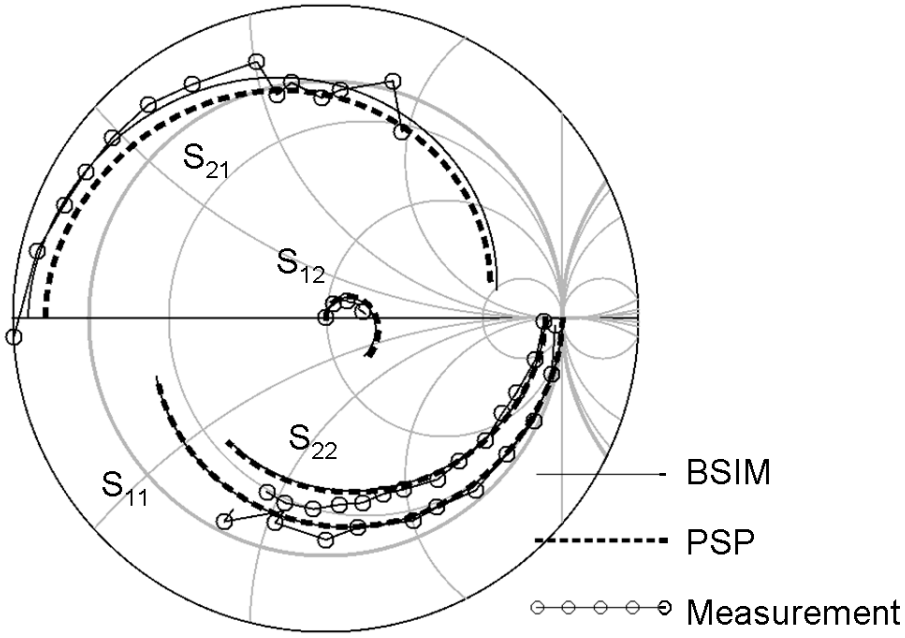
For large signal analysis, two tone tests have been performed utilizing Agilent E4438C Signal Generator and Agilent E4440A Spectrum Analyzer. 5 GHz operation frequency and 1 MHz two tone spacing have been chosen for the characterization. The measurements are carried out with 50 Ω conditions. From the fundamental tone HD1 and the third order intermodulation product IM3, the output IP3 can be calculated as follows [44]

$$OIP3(dBm) = 1.5 \times HD1(dBm) - 0.5 \times IM3(dBm) \tag{4.22}$$

Fig. 4.11 shows the measured and simulated HD1, IM3 and output IP3 of M2 for the bias point of V_{gs} = 0.8 V, and V_{ds} = 1.2 V.



(a)



(b)

Fig. 4.10 Measured and simulated S-Parameters of M1 (a) V_{gs} = 0.8 V, V_{ds} = 1.2 V; (b) I_{ds} = 3 mA, V_{ds} =1.2 V. In both figures f_{simu} = 0.1-60 GHz. $f_{measure}$ = 0.1-40 GHz

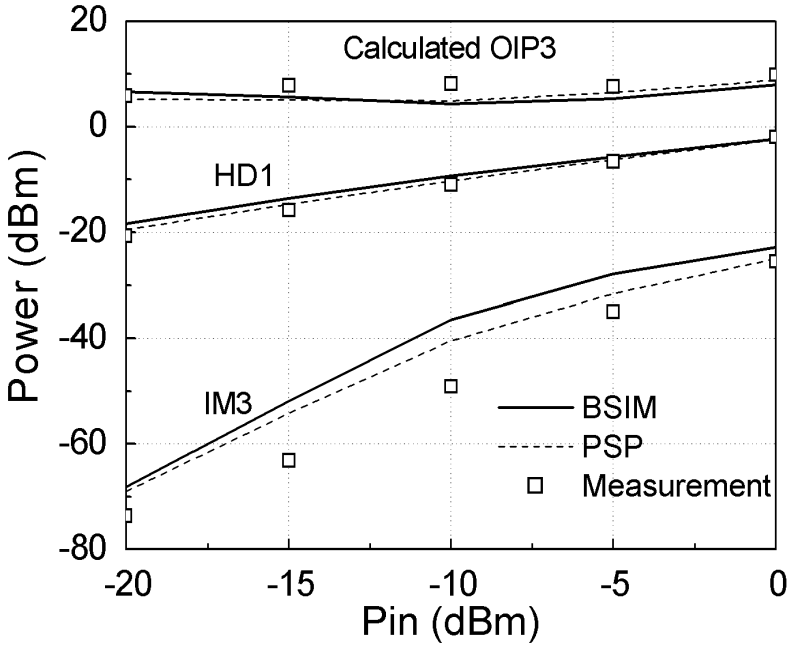


Fig. 4.11 Measured and simulated OIP3 of M2 when V_{ds}=1.2 V

From Fig. 4.11, it can be seen that the simulated HD1 of PSP and BSIM4 model fits each other and closed to the measured values. However, the IM3 values of the PSP model is close to the measurement compare to the BSIM case.

Some previous works have already demonstrated that the PSP model can simulate the circuit performance more precisely when V_{ds} = 0 V [42],[45]. Similar analysis has been performed in this work and the results are presented in Fig. 4.12. Shown in this figure are HD1, IM3 and OIP3 of transistor M2 for V_{ds} = 0 V. The results presented here are different from [42],[45] owing to the chosen common-source structure. Nevertheless, it can be seen that when the input power is less than -20 dBm, the BSIM4 model tends to have an under-estimated IP3 value. When the input power is larger than -20 dBm, both the models provide good estimation.

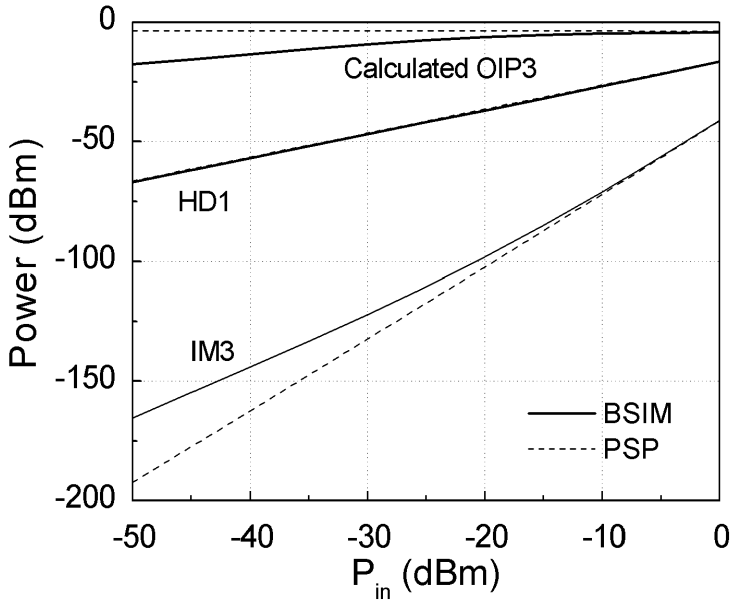


Fig. 4.12 Simulated OIP3 of M2 when V_{ds}=0 V

According to [46], the third order intermodulation currents can be expressed by

$$i_{IM3trans} = \frac{3}{4} G_{m3} v_{gs}^{\ 3} \frac{G_{load}(G_d + G_{load})^2}{G_m^{\ 3}} \tag{4.23}$$

$$i_{IM3output} = \frac{3}{4} G_{d3} v_{ds}^{\ 3} \frac{G_{load}}{G_d + G_{load}} \tag{4.24}$$

Here v_{gs} and v_{ds} are the voltage swings at the transistor gate and drain. G_{load} is the load conductance. $i_{IM3trans}$ and $i_{IM3output}$ are the third order intermodulation current related to the transconductance and the output conductance. It is verified in [46] that when the load resistance is small (less than one hundred Ω), the transconductance is the major source of the nonlinearity; and when the load resistance is large, the nonlinearity of output conductance dominates. In our case, due to a load impedance of 50 Ω, the dominate source of nonlinearity is G_m, and IP3 is determined by (4.23). From (4.23), it can be seen that the third order intermodulation current is proportional to G_{m3}. As G_{m3} of the BSIM4 model is larger than the PSP model, the BSIM4 model shows a poor linearity performance.

In Fig. 4.12, where V_{ds} = 0 V, G_m and G_{m3} are equal to zero. Therefore, IP3 is determined by (4.24) and the third order intermodulation current is proportional to G_{d3}. As analyzed in Part A, G_{d3} of the BSIM4 model is not continuous when V_{ds} = 0 V. Hence, for low input power levels, the BSIM4 model cannot give an accurate result as the PSP model.

D. SUMMARY

In conclusion, BSIM4 and PSP compact MOSFET models are compared with each other. DC, small signal and large signal analysis have been performed on both models and compared with the measurement results. It can be concluded that for low overdrive voltages, the BSIM4 model shows accurate small-signal performance and hence becomes a favorable choice for LNAs, mixers and other low power circuits. However, when the drain source voltage is close to zero, such as passive mixers or switches, the PSP model is more reliable for correct linearity estimation.

4.2.5 Low-power Considerations

The target of this work is designing low power CMOS transceivers. To minimize the power consumption, the selected transistor size should be minimized and the transistor gate should be biased at a relatively low voltage. As the transistor size is small and the biasing voltage is low, special considerations have to be taken, especially when the circuits operate at high frequencies as 24 GHz.

As transistor width is close to the technology limit, the transistor model became highly inaccurate. The technology limitation of transistor width for RF NMOS is 480 nm. However, the model becomes inaccurate when the transistor width is below 2 µm. According to the simulation and measurement, a 2 µm*10*130 nm NMOS transistor has a large frequency shift for S_{11}. The measured S_{11} is less capacitive than the S_{11} provided by the model, which hints that the operate frequency of the NMOS transistor is higher than that predicted by the model. At 24 GHz, according to our experience this frequency shift is about 1 GHz~2 GHz. As frequency goes higher, the frequency shift becomes even larger. Therefore, before the circuit design, test circuits should be designed and the transistor should be characterized accurately to avoid the unwanted frequency shift.

For NMOS transistors, it is recommended that the current density should be 150~200 μA/μm to ensure optimized circuit performance [47]; however, in low power circuits the current density might be less than 50 μA/μm. For example, in a typical cascade LNA, the transistor gate is usually biased at 0.6 V, and the current density is less than 50 μA/μm. In this case, both the transistor gain and NF should be characterized accurately, to make sure that the transistor performance does not degrade too much in the low power condition.

4.3 Passive Component Models

4.3.1 Passive Component Selection

The passive components in IBM 8RF CMOS technology include resistors, capacitors, inductors, transmission lines, transmission line based structures and so on. Each passive component has several different types to be selected from. The selection of proper passive components includes tradeoffs between process variation, performance and occupied chip area. In this section, the selection of different types of passive components is discussed.

A. Resistors

Three types of resistors are commonly used in CMOS technologies, N+ diffusion resistors, (P+) polysilicon resistors and N-well resistors. Since the resistors are very small compared to the other passive components such as inductors and capacitors, the major design aspects that should be considered for resistors are the process variation of the resistors and the frequency response.

In order to minimize the mismatch of the resistors, the resistor width is chosen around 1 μm, which is 5 times larger than the minimum width. The N+ diffusion resistors are selected for resistances less than 1 kΩ and the P+ polysilicon resistors are chosen for resistances larger than 1 kΩ.

The frequency response for resistors should also be considered in the circuit design. A resistor could be considered as a shunt resistor/capacitor pair. As frequency increases, the

resistance R_{in} decreases and the coupling capacitance is relatively stable. For low resistances, R_{in} have relatively large bandwidth. However, R_{in} at 24 GHz are around half of R_{in} at DC. Although C_{in} is more stable, according to the measurement there is a "cut-off frequency" where the capacitance became negative, which is usually higher than 60 GHz. In the design of high frequency circuits such as 60 GHz, these aspects should be evaluated, especially the resistor model accuracy at high frequencies should be analyzed.

B. Capacitors

Various capacitors are available in this CMOS technology: the MOS transistor could be used as capacitors; the thin metal layers could be interlaced as capacitors, MIM (Metal-Insulator-Metal) capacitor is also an option. Among these choices, the MIM capacitors are selected for the high-frequency circuits due to the high Q-factor performance.

From the model provided by the foundry, the Q-factor of a typical MIM capacitor (~10*10 μm) at 24 GHz is 10~20, which is much less than the Q-factor at low frequencies. However, the Q-factor of MOS-based capacitors and metal-interlaced capacitors are only 2~5 at 24 GHz. Therefore, the MIM capacitor is the only proper choice for high frequency. However, when MIM capacitors are implemented in the RF circuits, the resistive effects of these capacitors should be considered.

The area-efficiency of the MIM capacitors is also acceptable. The area capacitance of the MIM capacitors is around 2 $fF/\mu m^2$. To realize a reliable RF ground, the capacitance between the power supply and the DC ground should be larger than 10 pF, therefore a 50 μm*100 μm capacitor is required. Other capacitors used in the circuits are usually smaller than this size.

C. Spiral Inductors

Two RF metal layers are available for the spiral inductors in this technology, the top metal MA and the second metal E1. The third metal LY is also an RF metal layer, but it is close to the silicon substrate (~5 μm, which is one third of the second metal) and it is relatively thin (~0.5 μm). Hence the Q-factor of the spiral inductor on the third metal layer is too low. The spiral inductor could be built on a single RF metal layer, or both MA and E1 layers as a

parallel inductor. By simulation, the Q-factor of the parallel inductor which used both MA and E1 layers is 3~5 higher than the single layer inductor. However, the parallel inductor is hard to layout and modeling because of the squared vias between the two metals. Therefore, in our designs the MA metal based inductors are used.

According to the simulation, the peak Q-factor frequency of a 1 turn spiral inductor with 100 μm outer dimension and 5 μm width is around 20 GHz. In order to maximize the Q-factor of the inductors at 24 GHz, a lot of inductors are simulated and an inductor library is build. The inductor sizes vary from 70 μm to 120 μm, the number of turns varies from one turn, one and a half turn to two turns. The Q-factor of the inductors are 10~20 at 24 GHz, while the inductance varies from 100 pH to 500 pH.

Patterned ground plane is implemented to reduce the eddy currents on the Silicon substrate evoked by the RF signal. These eddy currents increase the loss and bring down the Q-factor of the inductor. The designed comb-like patterned ground plane incorporates strips with 0.8 μm width and ~3 μm distance. A 5 μm width underpass connects the patterned plane to the ground.

D. Transmission Lines

Microwave transmission lines include coplanar waveguide, microstrip, slotline, stripline and so on. In our design the side-shielded single wire transmission lines (or grounded coplanar waveguide) are used. This type of transmission line has metal-shielding at the bottom metal as well as the sides of the transmission line.

Since the loss of the silicon substrate is difficult to model using the EM solvers as Momentum or HFSS, the bottom ground metal plane is introduced to isolate the transmitted signal from the substrate. The ground metals on the sides of the transmission line are introduced to isolate the signal from adjacent components.

To simplify the design process, 50 Ω transmission lines are implemented. The designed transmission lines are on top layer (MA) with bottom ground metal on third layer (LY), with metal width of 6 μm and the distance to the side-shielding of 6 μm. The transmission lines are mainly used as interconnections between different components.

E. Bends and T-Junctions

Bends and T-Junctions are used in the circuits as interconnection. Since the EM models of these structures are more complicated and they introduce more insertion loss, in the circuit designs they are usually avoided if possible. To be easily integrated with the transmission lines, the bends and T-junctions are also on MA layer with bottom ground metal on LY layer. They are also side-shielded and with the same size as the transmission lines.

F. Pads

The bondpads in this technology have several types. Among them the one with the minimum coupling capacitance ground layer is selected. The implemented BFMOAT ground layer is a highly resistive layer to block P-Well and N-Well implants.

The size, pitch and placement of the pads are designed according to the measurement requirements. For DC signals, 5 parallel pads of 100/150 μm pitch are most frequently used. The DC pad sizes varies from 75 μm*100 μm to 100 μm*125 μm. For RF, LO and IF signals, ground-signal-ground pads (GSG), ground-signal-signal-ground (GSSG) pads or ground-signal-ground-signal-ground (GSGSG) pads are used. The pitches of the signal pads are mostly 100 μm, while some of them are 150 μm. The size of the signal pads varies from 75 μm*75 μm to 75 μm*100 μm.

4.3.2 EM Simulation

EM simulation tools are selected over the parasitic extraction tools for their accuracy in the circuit modeling. The Cadence parasitic extraction tool QRC is also a decent choice, which is capable of extracting the parasitic resistances, inductances, capacitances and mutual inductances (RLCK).

Various tools provide a lot of choices to perform the EM simulation. These include the “mainstream” 2D & 3D EM simulators such as HFSS, ADS Momentum, CST and Sonnet, of which the most popular are HFSS and ADS Momentum. In this section HFSS and ADS Momentum will be discussed based on their characteristics and the field of application. Since

nowadays the computer hardware and EM simulation software are improving very rapidly, the comparison of their performance is not very interesting.

HFSS is a 3-D full-wave electromagnetic field software produced by Ansoft which can be used in circuit, high frequency, signal integrity and electromechanical simulations. The simulation technology bases on the finite-element method. Since HFSS provides full-3D simulation, it is a decent choice for the 3-D structures, components and circuits. For the complex integrated RF components build on multiple RF metal layers, HFSS is also a proper choice.

ADS Momentum is a 3-D planar electromagnetic simulator from Agilent EEsof EDA which also bases on the finite-element method. This software is designed for EM simulation of the planar structures, components and circuits. For RFIC/MMIC circuits which build on one or two RF metal layers, ADS Momentum is a proper choice. In our designs, ADS Momentum is usually used, since the RFIC circuits we designed are planar-based structure built on two to three RF metal layers.

Normally full-chip EM simulations are performed to get the accurate EM characteristics of the designed chip. The EM simulation usually takes a lot of simulation time to complete. Besides, the simulation time is approximately proportional to the square of the circuit complexity. Therefore, the size and complexity of the simulated structure should not be too large to avoid the simulation time penalty. To simply the simulation, the inductors are simulated separately and the other passive structures on the chip are fully-simulated.

4.3.3 Skin Effect and Edge Mesh

With increasing frequency of operation, the circuits are getting more and more sensitive to the parasitic effects of on-chip passive elements. As a result, the precise modeling of these components becomes a crucial issue for a successful implementation.

At high frequencies, the inductors and interconnects are hard to model due to the skin effect and the proximity effect. Skin effect refers to the tendency for high-frequency currents to flow on the surface of a conductor, while proximity effect is the tendency for current to be constrained in small regions due to the magnetic coupling between the adjacent conductors. While the proximity effect can be suppressed by guard ring structures [48], the skin effect can

only be simulated and considered by proper meshing method [49]. Although, in [49], the skin-effect model is analyzed up to 3 GHz, there are very few works reporting the importance of the influence of skin effect in high frequency CMOS designs. With a tradeoff between simulation time and accuracy, Electro Magnetic (EM) models can be improved by increasing mesh density and meshing method. This tradeoff is crucial to the time of the design flow, especially at higher frequencies. Hence, it is meaningful to analyze the importance of skin effect and edge mesh of the passive elements at high frequencies and to understand its importance in a circuit level.

In this section, we analyze the skin effect of on-chip passive structures like transmission-lines and inductors in 0~40 GHz range using different meshing strategies. In order to verify the significance of skin effect and selecting a proper meshing methodology, a 24 GHz common source (CS) CMOS low noise amplifier (LNA) is also designed and measured. The results are compared with the simulated results under various conditions.

In this example we use ADS Momentum as the EM simulation tool. Momentum is a 2.5D electromagnetic simulator based on a numerical discrete technique called the method of moments [50]. This method divides each metal plane into a grid-like pattern of triangles and rectangles, which is called mesh. Each triangle and rectangle is called a cell. Then the Maxwell's equations of the circuit can be solved based on the numerical computation of the cells. The skin effects are normally incorporated by the EM simulation tools using edge meshing. Edge mesh is a technique of adding relatively dense mesh along the edge of objects. The default width of the edge mesh is equal to the skin depth, while the skin depth is inversely proportional to the square root of the frequency. Hence, when the frequency goes higher, the skin effect becomes more influential. In multi-layer designs, EM simulations with edge mesh cost more time than the ones without edge mesh and hence normally not suggested by the vendors. However in this work it will be shown that at K-band operating frequencies the skin effect is so influential that EM simulations without edge mesh cause serious problems and provide solid discrepancies with the measured results.

On-chip microstrip lines are widely used as interconnects and matching components in RF integrated circuits. Fig. 4.13 shows the simulated EM field distribution on a section of the microstrip line. The results presented correspond to an operating frequency of 24 GHz. The color of a particular area shows the current density of that area. From the microstrip line we

can see that most of the RF current flows through the side of the line. In the middle of the microstrip line, relatively there is a very low current distribution due to skin effect.

For these microstrip lines, the skin depth at 24 GHz is 0.51 μm. It means at 24 GHz, most of the current is flowing within the 0.51 μm from the edge of the microstrip line. As a result, in the EM simulations these edge areas should be meshed as independent areas in order to properly simulate the skin effect.

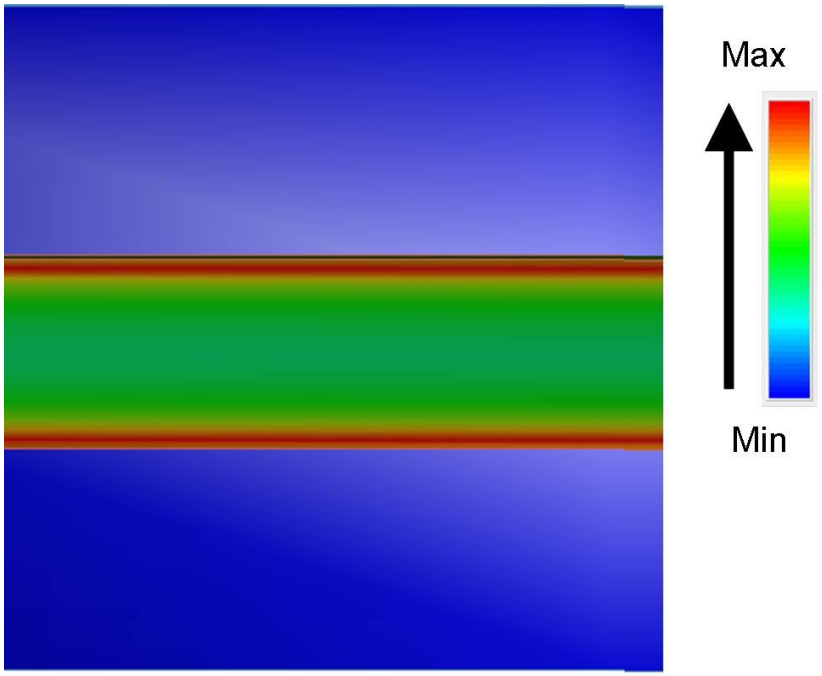


Fig. 4.13 EM current distribution of a 10 μm width microstrip line

In order to investigate the influence of skin effect in high frequency circuits, a 24 GHz two-stage CS LNA is designed and fabricated using IBM 7WL 0.18 μm BiCMOS technology. CS structure is the popular topology in this frequency band because it has lower noise than the cascode structure. But the matching network design of CS LNAs is more critical than cascode LNAs due to their poor input/output isolation. Thus, the passive elements should be modeled very carefully for all the possible EM effects. Fig. 4.14 shows the schematic of the LNA. As shown in Fig. 4.14, two CS cascade transistors have been used. The input matching network uses two spiral inductors with patterned ground shielding. The inter-stage matching and the output matching use shielded-transmission lines and MIM capacitors. The LNA input and

output are matched to 50 Ω. Both transistors have 10 fingers; each finger has a width of 3 μm. A 15 Ω resistor is used in the output matching for stability reasons. The whole chip occupies an area of 0.63 mm^2, and the size of the active region is 0.32 mm^2. The chip micrograph is shown in Fig. 4.15.

The circuit is simulated in ADS Momentum with and without edge mesh using the methodology mentioned in [52]. Although the simulation time is a function of various factors like chip size, complexity etc., in our case, simulations with edge mesh cost about 4 times more computing time than the ones without edge meshing. The transistor gate bias is set at 1 V, and the DC bias at 1.8 V for a bias current of 12.4 mA. As shown in Fig. 4.16, the results of the simulations without the additional edge meshing differ significantly to the measured results compared to the normal simulations. At 24 GHz, simulations without edge mesh showed 8.5 dB power gain, while the one with edge mesh showed a power gain of about 4.5 dB which is very close to the measured 4.8 dB. The significant difference in the gain values are principally contributed by the lack of EM effect consideration of the shielded spirals and lines in the input matching network.

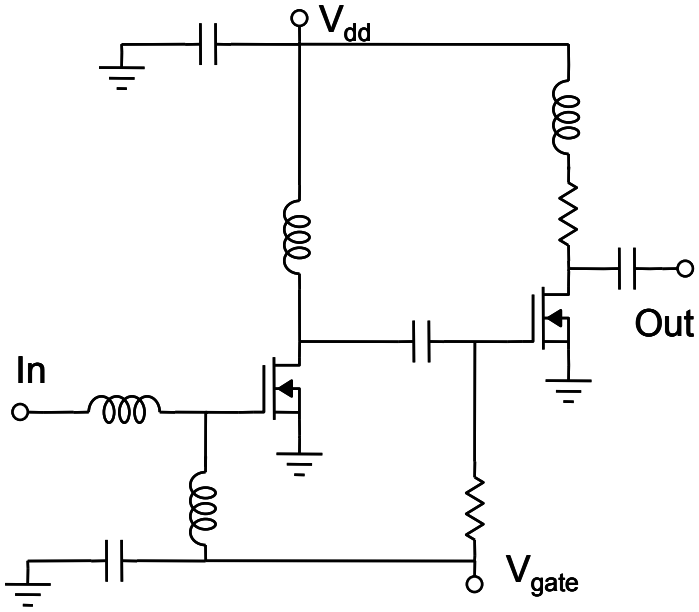


Fig. 4.14 Schematic of the LNA

In this 24 GHz LNA, it can be seen that the gain degradation by 4 dB is correctly estimated when the skin effect of the all the on-chip passive elements is considered through edge meshing. At lower frequencies, the skin effect is not that influential and hence almost no

variations have been observed. It can be concluded that at K-band or higher frequencies, it is quite important to consider such EM effects using advanced meshing to correctly estimate the performance of the circuit. Hence, edge mesh is vital for a successful implementation, especially for the designs at these frequencies using spiral inductors with patterned ground planes. It is also quite important to consider that the percentage of variations in the results of high frequency designs due to such edge mesh considerations is also a very strong function of the design topology and its reliability.

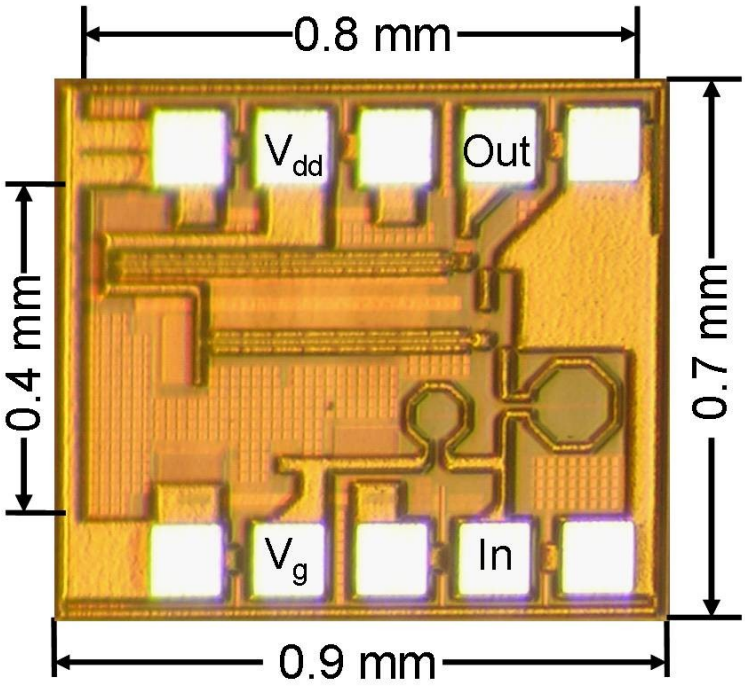


Fig. 4.15 Chip micrograph of the LNA

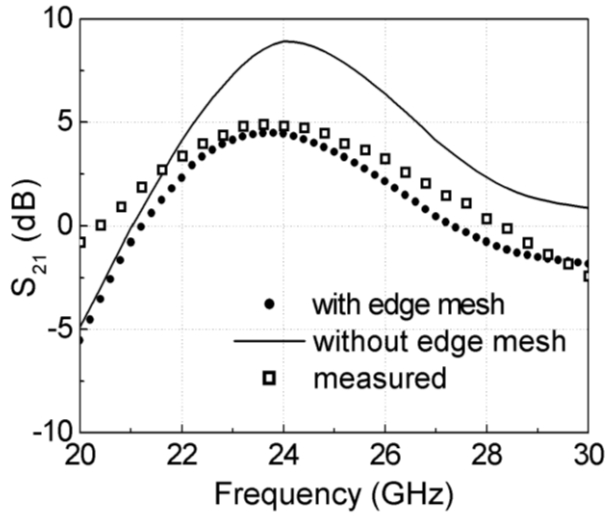


Fig. 4.16 Simulated and measured S_{21} of the LNA

In conclusion, the significance of including the EM effects especially pertaining to skin depth considerations of on-chip passive structures in K-band designs is investigated. To understand the overall importance of these individual discrepancies, a K-band CMOS LNA is designed and realized in the same process utilizing the presented passive structures. A very close estimation of the simulated results with skin effect considerations through edge meshing compared to the conventional method confirmed its importance in K-band circuit realizations. With this it is possible to have a reliable design environment leading to successful and state-of-the-art implementations particularly at K band frequencies and above [53].

4.4 Balun Design

4.4.1 RF Integrated Baluns

The balun is an electrical component which converts balanced signals to unbalanced signal, or the reverse. In RF/Microwave integrated circuits, they are one of the most important components. The balun are implemented in many circuits such as balanced mixers [67]-[69], frequency dividers [70],[71],and differential amplifiers [72],[73].

In hybrid circuits passive baluns are commonly used [74]-[77], while in RFIC and MMIC designs both active baluns and passive baluns are widely implemented. For ICs work below

4 GHz, since the passive baluns are too bulky to realize on chip, usually active baluns are implemented [78]-[80]. For ICs work above 4 GHz, compared with active baluns [81],[82], passive baluns are more intensively studied, such as lumped-element baluns [83], transformer baluns [85],[86] and Marchand-type baluns [87]-[91].

Since there are a lot of choices for baluns operating at higher frequencies, the selection of the proper balun topology for integration becomes complex. This chapter focuses on the design and integration of K-band CMOS baluns, while different topologies are analyzed and compared with each other. The design processes of an active balun, a lumped-element balun and transformer baluns are presented. Various figures of merit are compared, such as insertion loss, phase imbalance, amplitude imbalance, bandwidth, and chip area. Based on the analysis, the case-dependent optimum topology for specific applications is discussed.

The balun integration is also a popular topic. Usually the load impedance of the balun is not at 50 Ω, such as for mixer integration where the balun load is capacitive [67]-[69]. Therefore, re-design of the balun is required. In this chapter an impedance tuning approach is proposed to simplify the integration process. The insertion loss (IL), amplitude imbalance (ΔA) and phase imbalance ($\Delta\Phi$) of the baluns are simulated while the load impedance is tuned at a particular frequency and the performance contours are plotted on the smith chart. Based on the results the proper balun topology could be chosen, while the re-design and integration process could be simplified.

4.4.2 Active and Passive Baluns

A. Active Balun

Among the various topologies of active baluns [74]-[78], the most widely used topology is the differential amplifier topology. As shown in Fig. 4.17(a), a conventional differential amplifier can be used as an active balun. The RF input is the gate of M1, while the gate of M2 is connected to the RF ground. The common source transistor M1 produces 180 degree phase shift and the common gate transistor M2 does not produce any phase shift. This topology suffers from several problems when frequency goes higher. Firstly, the 180 degree phase shift of M1 and 0 degree phase shift of M2 becomes inaccurate. Secondly, M1 and M2 cannot produce the same gain. When the current density is equal, the common source transistor has

much higher gain than common gate transistor. Therefore, the active balun suffers from both phase imbalance and amplitude imbalance.

In order to overcome these problems, the active balun is re-designed and the schematic is shown in Fig. 4.17(b). A cross coupled transistor pair is added between the transistor drains and balun outputs. Varactor pairs are inserted between the gate and source of the cross coupled transistors to control the power split ratio. By tuning the varactor capacitance, the coupling between the two branches can be variable. Therefore, the RF power can be re-distributed between the two branches, and the power imbalance is tunable. The RF distribution is carefully considered to keep the amplifier stable. In order to tune the phase imbalance, a varactor pair is shunted with the series capacitor used in the output matching network of one branch. The shunt varactors capacitance is much less than the series MIM capacitor to maintain low insertion loss and to keep the Q-factor of the shunted capacitors similar to the MIM capacitor. By tuning the varactor capacitance, the phase imbalance of SDC is also tunable in a certain range.

(a) (b)

Fig. 4.17 Schematics of (a) a conventional active balun; (b) the proposed active balun AB-1

The current source transistor M3 is designed 8*12.5 μm transistor width, 1 μm transistor length. The transistor length is very large compared with the other transistors since the voltage drop between the drain and source should be minimized to around 0.1 V. The voltage headroom for the cascade pairs is optimized at 1.1 V for maximum gain.

The transistor size is optimized for gain, NF and matching. For M1 and M2, the finger width is 4 μm, which has the optimized gain and NF. The number of fingers is set to 16 to make a good tradeoff between model reliability and power consumption. For M4 and M5, the transistor size is 16*6.25 μm. Larger transistor size simplifies the output matching. Besides, although the cross coupled transistors does not have significant influence on NF, they still need some gain for optimum power distribution. The M4 and M5 transistor size are enough to provide sufficient gain.

Each varactor is realized by two series varactors with control voltage on the gate between them. The varactor model has low Q-factor of around 3~6 at 24 GHz. C1 and C2 decide the power splitting ratio between the two branches. Since the gain of the common gate transistor M2 is smaller than that of M1, C1 is set larger than C2 to compensate the gain mismatch. The varactor C3 is not directly employed in the output matching circuit, but shunted with a MIM capacitor to increase the Q-factor. The capacitance of the MIM capacitor is 0.3 pF, which is much larger than C3.The Q-factor of the shunted capacitor pair is close to the MIM capacitor.

Fig. 4.18 shows the simulated amplitude and phase imbalance versus C1 and C3 capacitance. The simulation frequency is 24 GHz. C2 is set at 0.3 pF. C3 is 0.06 pF when sweeping C1, while C1 is 0.1 PF when sweeping C3. The Q-factor of the varactors varies as biasing voltage changes; here it is set to 5. It can be see that C3 has large influence on phase imbalance and small influence on amplitude imbalance. On the contrary, C1 has large influence on amplitude imbalance and small influence on phase imbalance. By changing the biasing voltage of the varactors, both amplitude imbalance and phase imbalance can be tuned to minimize the influence of the process mismatch.

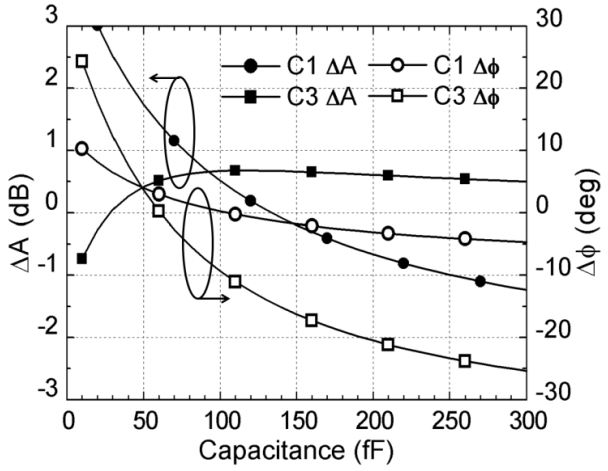


Fig. 4.18 Amplitude and phase imbalance versus C1 and C3 capacitance

B. Lumped Element Balun

The lattice-type L-C balun topology, which is shown in Fig. 4.19, consists of two capacitors and inductors. When the inductor and capacitor values are carefully chosen, the circuit produces ±90 degree phase shift for both branches which results in balanced outputs.

The inductance and capacitance are set to L=Zc/ω and C=1/(Zc•ω), where ω is the angular velocity of the design frequency and Zc is the geometric mean of the source and load impedance. The inductance is 0.35 nH and the capacitance is set to 0.1 pF.

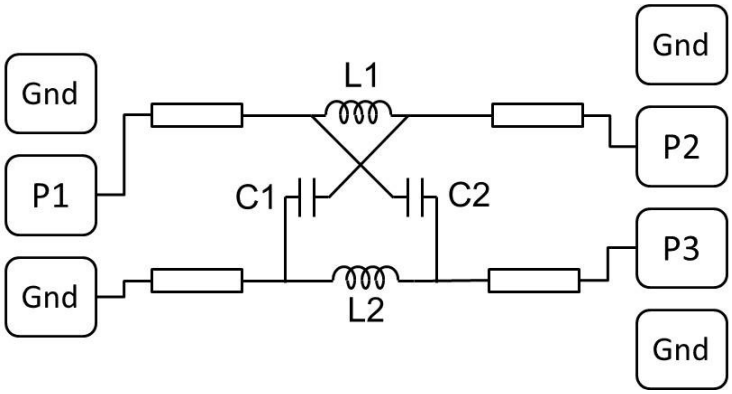


Fig. 4.19 Circuit configuration of lattice-type L-C balun LC-1

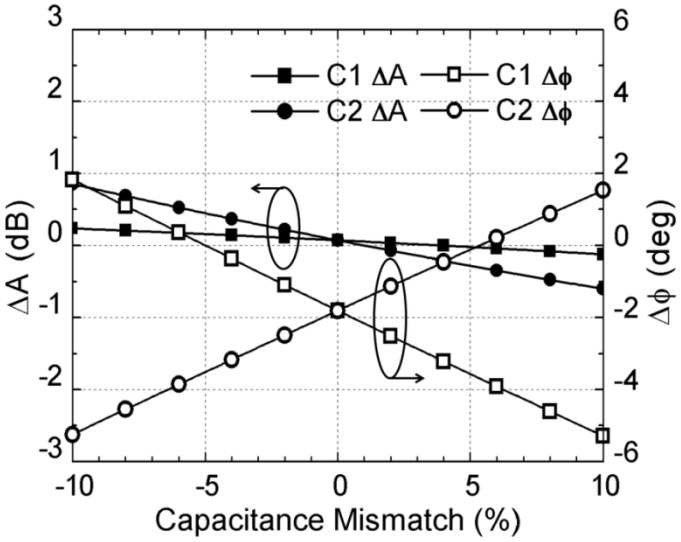


Fig. 4.20 Amplitude and phase imbalance versus C1 and C2 capacitance mismatch

In K-band, the component parasitics are crucial to the circuit performances, therefore, they should be considered from the beginning of the layout design. The inductors and interconnects are carefully designed and EM modeled. Patterned grounded inductors are selected to minimize the substrate coupling. The inductor Q factor is maximized at 24 GHz. High Q-factor ensures low insertion loss. The inductance is 0.35 pH. In order to maximize the Q-factor, parallel inductors are selected, which use both RF metal layers as spiral metals. The inductor outer dimension is 120 μm. The metal width is minimized to 5 μm. The coupled side-shielded transmission lines are chosen as interconnects. The transmission line width is 6 μm and the distance between transmission line and side-shield metal is also 6 μm. The characteristic impedance of the transmission line is 50 Ω. The inductors and interconnects are EM simulated up to 40 GHz using ADS Momentum.

The capacitors type and dimensions are chosen to ensure the phase and amplitude balance. Varactor and MIM-capacitor are two candidates for the capacitors used in this balun. Although the varactors bring some flexibility to this circuit, the varactor Q-factor is only 3~6 at 24 GHz while the Q-factor for MIM capacitors are more than 10 at the same frequency. In order to minimize the insertion loss, the MIM-capacitors are chosen. However, due to process inaccuracy, the MIM-capacitors exhibit maximum 10% capacitance mismatch. Fig. 4.20 shows the simulated phase and amplitude imbalance versus the capacitance mismatch. The frequency is 24 GHz. It can be seen that even if the MIM capacitors varies up to ±10%, the amplitude difference is less than ±1 dB, and the phase difference is less than ±6 degree.

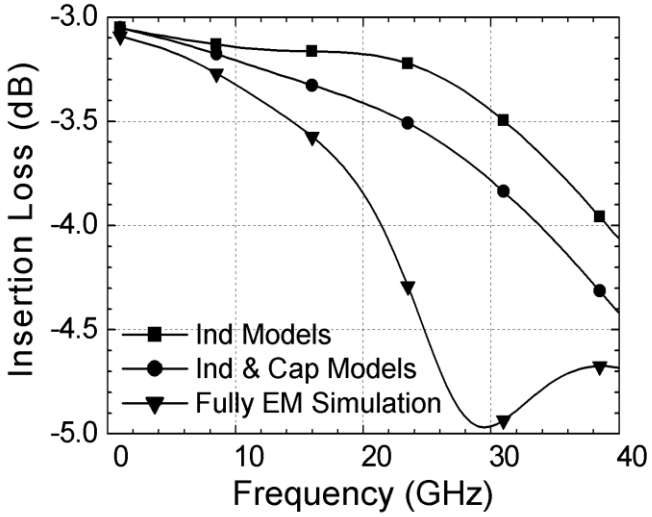


Fig. 4.21 Insertion loss versus frequency considering various parasitic effects

The circuit layout are carefully designed to ensure high symmetry and low insertion loss. The two inductors are placed symmetrically in the layout. These two branches are placed as far as possible to minimize the unwanted coupling. Metal grounds are added all over the chip to minimize the substrate coupling. Then the balun, including the pads but without the capacitors, is fully EM simulated. Fig. 4.21 shows the simulated insertion loss with inductor models and ideal capacitors, with inductor and capacitor models, and with fully EM simulation. The contribution of the insertion loss by inductor, capacitors and passive interconnects can be de-embedded from this figure. At 24 GHz, insertion loss induced by inductors is 0.2 dB, by capacitor is 0.3 dB, and by other passive structures and interconnects is 0.9 dB.

The major problem for L-C baluns is that the phase and amplitude are balanced only in a narrow frequency bandwidth. Special circuit topologies could be implemented to compensate the phase and amplitude imbalance, such as in [83], two filters are integrated with the lumped-element balun to compensate the amplitude and phase errors.

C. Transformer Balun

Transformer baluns utilize transformers to convert single-ended signal to differential. Compared with other topologies, they have high Q-factor, large bandwidth and highly-integrated. The insertion loss of a transformer balun is not only depended by the Q-factor of the windings, but also the coupling factor K between the two windings. In order to minimize the insertion loss, the K-factor and Q-factor should be maximized.

In [85], a comprehensive review of electrical performance of passive transformers fabricated in silicon IC technology is presented, where stacked transformers are compared with planar transformers. However, since the CMOS process and the operation frequency are specified, the two topologies should be compared again in a simulation level. The utilized process has two RF thick metal layers on the top. The stacked transformer use both RF layers and the planar transformer use the bottom one which allows smaller metal-to-metal distance. A stacked transformer and a planar transformer, both with one turn for each winding, metal width of 5 μm and outer dimension of 100 μm, are designed and simulated in ASITIC [12]. The simulated coupling(K-) factor is 0.5 for the stacked transformer and 0.6 for the planar transformer at 24 GHz. The difference of K-factor is due to the process restrictions on the

spacing of the metal windings; the minimum distance between the two windings of the stacked balun is 4 μm, while for the planar balun is only 2 μm. Because the planar transformer balun has larger K-factor than the stacked transformer balun under constant Q-factor of the windings in both the cases, it can be mentioned that the planar balun has smaller IL. EM simulation using ADS Momentum shows that the planar balun has 0.15 dB higher gain than the stacked balun at 24 GHz.

From the analysis above, a rule of thumb to choose between stacked transformer and planar transformer can be proposed: if the distance between the top metal layers is less than the minimum allowed distance between two metal strips on the same layer, the stacked transformer balun is usually a better choice, and vice versa. However, it can only be considered as a general suggestion as other parameters also have influence on the transformer performance, such as the distance to substrate, the metal thickness, material of the metal and so on.

After comparison, the planar transformer baluns are chosen as they have less insertion loss. Then the metal layer on which the planar balun implemented is decided. E1 layer is a copper layer with 3 μm thickness and 10.7 μm distance to the substrate, while the minimum allowed distance between E1 metal strips is 2 μm. MA layer is a aluminum layer with 4 μm thickness and 17.7 μm distance to the substrate, while the minimum allowed distance between MA metal strips is 5 μm. Despite the MA layer is higher and thicker than E1 layer, the minimum allowed distance between E1 metal strips is much less. By simulation, the E1 layer is selected as the simulated coupling factor of a designed transformer is higher and the insertion loss is less than that of a transformer on MA layer. In order to design the planar transformer baluns, the outer dimension and number of turns should be optimized. The outer dimension of the windings should be as small as possible to reduce the chip area. However, as the outer dimension becomes smaller, the inductance of the winding becomes lower and the peak-Q frequency is higher. Similarly, the number of turns should be as high as possible to reduce the chip area. However, as the number of turns increases, the Q-factor drops drastically as well as the peak-Q frequency. To keep reasonable Q-factor at 24 GHz, the number of turns should be less than 2 and the outer dimension should be larger than 100 μm. To ensure the optimum transformer performance, the peak Q frequency of the windings should be at K-Band. Fig. 4.22 shows the peak Q frequency of the inductors versus the outer dimension and number of turns. The inductors are rectangular planar inductors with 5 μm metal width. If the inductor

outer dimension is between 100 μm and 120 μm, and the number of turns is between 1 and 2, the peak frequency is near K-Band. The number of turns in the primary winding is selected as 2, while in the secondary winding is 1.5. The reason for choose the number of turns is for layout considerations. The outer dimension of the balun is 100 μm. The simulated Q-factor is around 15 for these windings.

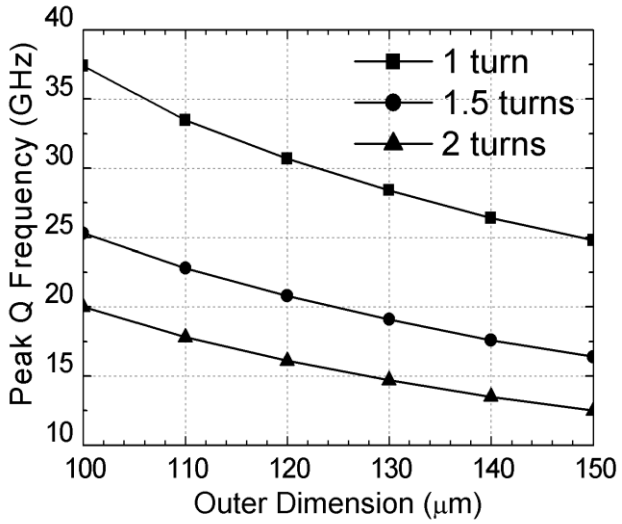


Fig. 4.22 Inductor peak Q frequency versus the outer dimension and number of turns

The layout of the two transformer baluns TF-1 and TF-2 is shown in Fig. 4.23 and Fig. 4.24. The layouts of these two baluns are performed differently to integrate with different circuits. The patterned bottom metal acts as ground shielding. The implementation of patterned ground avoids the eddy current loss in the substrate and ensures high Q-factor of the windings. The input port P1 is matched to 50 Ω at 24 GHz by adding a 0.1 pF series capacitor. The balun outer dimension is slightly modified to tune the winding inductance and improve the input matching. The output ports are not connected with capacitors since by simulation a series capacitor increases the IL. The return loss of P2 and P3 are -5 dB with 50 Ω load impedance at 24 GHz.

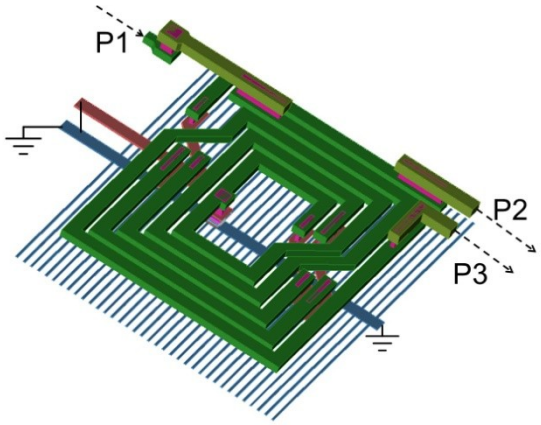


Fig. 4.23 Layout of the transformer baluns TF-1

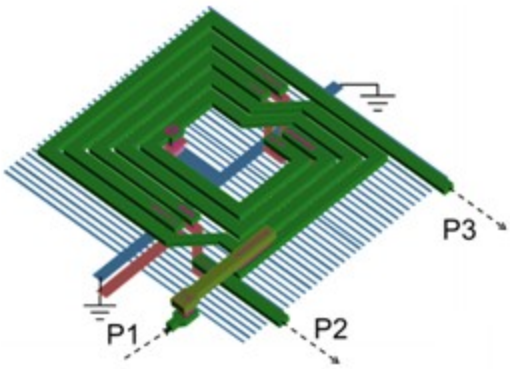


Fig. 4.24 Layout of the transformer baluns TF-2

The transformer topology ensures the phase balance [85], but the amplitude balance is still a problem. To solve this problem, the position of the center-tap on the secondary winding is moved along the winding. By moving the center-tap position, the coupling of the primary winding with one branch of the secondary winding increases, while the coupling with the other branch decreases and hence the amplitude imbalance could be compensated. It should be notice that the phase imbalance also slightly alters.

Further modifications could be implemented to enhance the balancing, such as in [86], the balun incorporates eight-layer metal layers in coil windings at a particular layout exhibits minimal amplitude and phase imbalance. But in our applications these approaches are not practical because of the frequency requirement and the limited number of RF layers.

D. Topology Comparison

To choose a proper balun topology for a specific application, various aspects have to be considered. The primary consideration is the trade-off between insertion loss and the balanced bandwidth. It is possible for active baluns to achieve both low insertion loss and broad bandwidth since the amplifier stages provide gain. For example, in [82] with the gain compensation technique the active balun achieved an ultra broad-band of 2-40 GHz. The trade-off becomes important for passive baluns. For lumped-element balun, high-Q components result in low insertion loss and small bandwidth, while low-Q components result in large bandwidth and high insertion loss. Transformer baluns usually have a board bandwidth but the insertion loss is also high, since the coupling-factor between the two windings is limited by the process. Marchand baluns could achieve both low insertion loss and broadband such as in [87], where board-side stacked topology is implemented.

Minimized chip size is an important performance of ICs. Active baluns usually incorporate several inductors to match the input and output which consume a relatively large chip area. The transmission-line based baluns are usually bulky, since the length of transmission line is large for ICs. For lumped element baluns, the chip size also relatively large when multiple inductors are required. The transformer baluns are smaller, since the size of a transformer is similar to an inductor.

Another important measure is that the balun should be able to easily integrate with other circuits. If a matching network is required between the balun and other circuits, not only the chip size is larger, but also the insertion loss becomes higher. In Section 5.3 the balun integration will be discussed and compared. The transformer balun is the easiest to integrate. The lumped-element balun is also easy to integrate and re-design. The integration is difficult for the active balun.

Some other aspects should also be considered. The active balun not only consumes power, but also have a limited linearity, hence it is not the best choice for high-power applications. The advantage of the active balun is that the output is tunable in a small range. Therefore the circuit is less dependent on component model accuracy.

Table 4-2 Comparison of the Three Balun Topologies at K-Band

	Active Balun	Lumped-element Balun	Transformer Balun
IL	With Gain	Low	Medium
Bandwidth	Wide	Narrow	Wide
Chip Size	Large	Large	Small
Design	Normal	Easy	Normal
Integration Difficulty	Normal	Normal	Easy
Other	Tunablity, Linearity, DC consumption		

Table 4-2 compares the performances of the three balun topologies. The advantages and disadvantages of all topologies are illustrated in this table. The active balun is good for their gain and wide bandwidth, but suffers from chip size and linearity. The lumped-element balun is good for their low loss and easy to design, the disadvantage is their narrow bandwidth. Although the lumped-element balun might be improved to overcome the narrow bandwidth, the chip size also becomes larger since more inductors will be implemented. The transformer baluns is the best choice for most cases for the wide bandwidth, small chip size and simplicity to integration.

4.4.3 Balun Integration

The baluns are usually designed with all port matched to 50 Ω. When integrated with other circuits, such as power amplifiers or mixers, the problem of matching occurs since mostly the load impedance is not 50 Ω. Two approaches could be implemented to solve this problem, either a matching network has to be designed between the balun and load, or the balun has to be re-designed to match the load circuit. Since the matching network introduces insertion loss and consumes chip area, the balun re-design is the better choice. However, the balun re-design usually costs a lot of effort. To simplify the re-design process, an impedance tuning method is

proposed below. While the impedance tuning method is frequently used in power amplifiers to optimum the performance, it can also be used in balun integrations to choose the proper topology and simplify the re-design.

The load reflection coefficient is swept (for both real and imaginary parts), with reference impedance 50 Ω for the designed passive baluns. The design frequency is 24 GHz and the source impedance is 50 Ω. The IL, ΔA and ΔΦ are calculated and the contours are plotted in smith charts shown in Fig. 4.25. The solid line circle is the -3 dB gain (3 dB from maximum gain value) circle. The shadowed area is the impedance range where the baluns have less than 1 dB ΔA and less than 5 degree ΔΦ. The transformer balun TF-1 are better choice for integration since its performance is more robust to impedance variation.

When the balun is integrated with a common source transistor circuit, normally the loads of the balun are the gates of transistors and the load impedance is capacitive. As a test case for integrate, the transformer baluns are simulated with RF NMOS transistors. The width of RF NMOS transistor is swept from 10 μm to 100 μm and the corresponding load impedance variations are depicted in Fig. 4.25(b). The length of the NMOS is 130 nm and the number of fingers is 10. Since the transformer balun TF-1 does not provide enough phase balancing for these impedances, by reducing the balun outer dimension and moving the center tap of the secondary winding, the matching and the amplitude/phase balance performance of the balun are optimized. The layout of the modified balun TF-3 is shown in Fig. 4.26(a). The simulated results from the load impedance tuning of the modified balun are shown in Fig. 4.26(b), the +5 degree ΔΦ curve is not shown since it is outside the smith chart. From Fig. 4.26(b), it can be mentioned that the modified balun TF-3 can provide better phase and amplitude balancing for the transistors of different sizes and hence quite suitable for integration in various circuits.

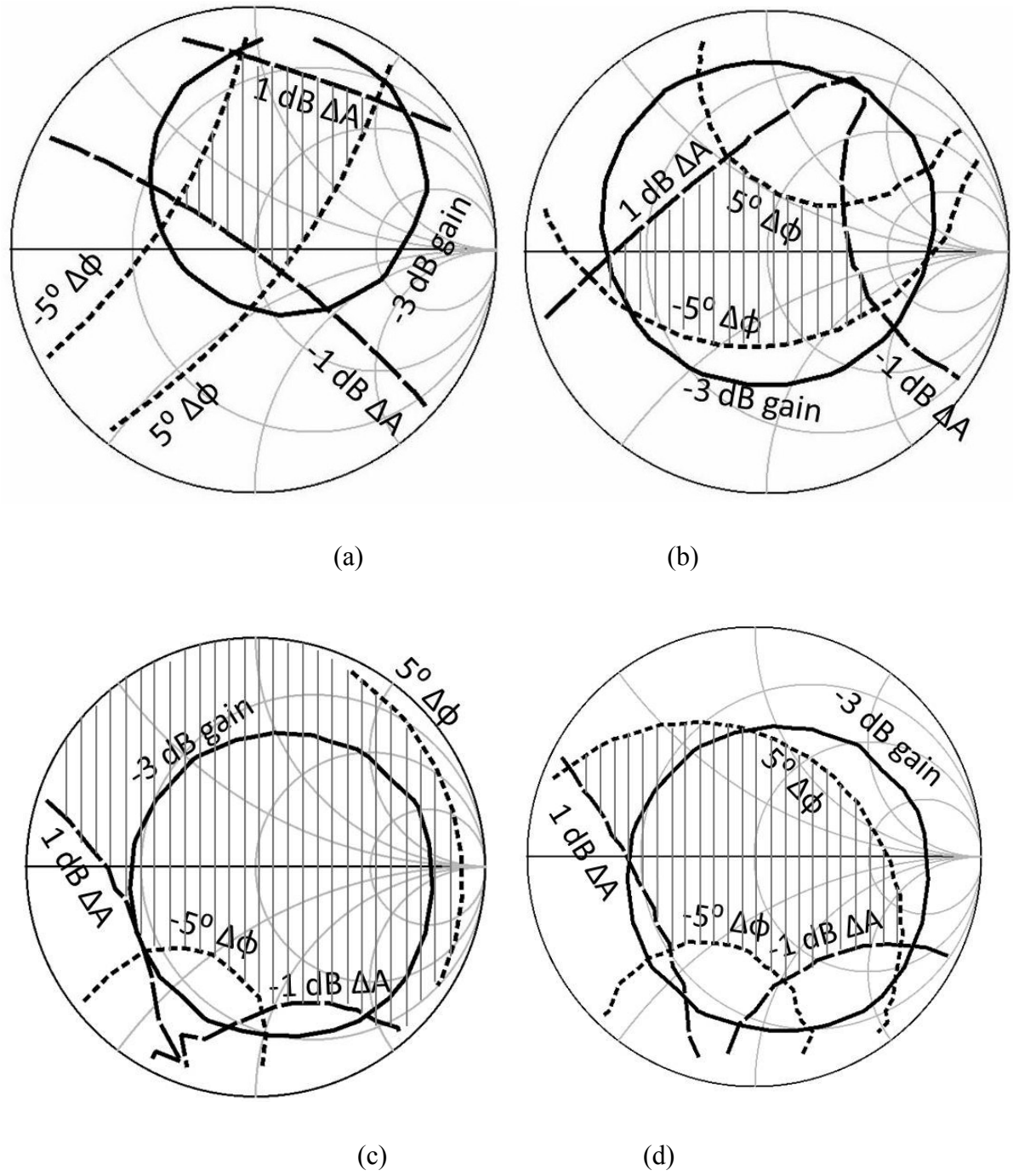
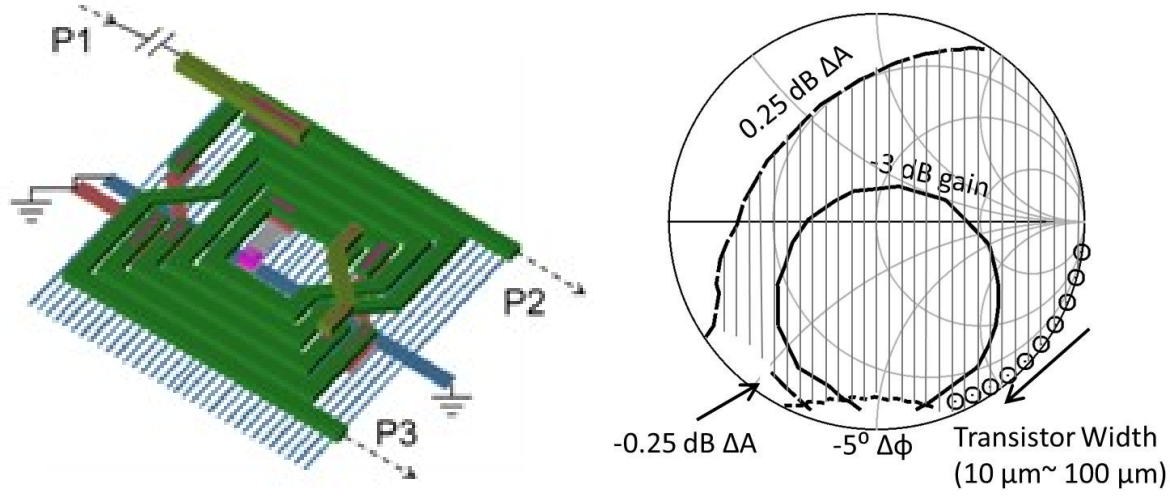


Fig. 4.25 Impedance tuning simulation of the -3 dB gain compression circle, ±1 dB amplitude imbalance and ±5 degree phase imbalance in smith chart for: (a) active balun AB-1; (b) L-C balun LC-1; (c) transformer balun TF-1; (d) transformer balun TF-2

The modified balun is integrated with an 8:1 static divider as presented in [92] and a miller divider as presented in [93].



(a) (b)

Fig. 4.26 (a) Layout of the transformer balun TF-3; (b) impedance tuning simulation for TF-3 in smith chart

Table 4-3 summaries the electrical and geometry parameters of the designed transformer baluns. All three transformer baluns are on E1 layer, with 5 μm metal width, 3 μm metal height and 2 μm distance between different windings. The number of turns P1,P2 and P3 are considered as the number of turns of the primary or secondary winding connected to the port P1, P2 and P3, respectively. For layout reasons the winding connected to P2 and P3 are not exactly symmetrical, but the electro-magnetic simulations show they are well balanced. The input and output impedance indicates that TF-1 and TF-2 can be used with 50 Ω source and load impedance, while TF-3 can only be used with 50 Ω source impedance and capacitive load impedance. The electrical signal goes through TF-1 and TF-3 straightly, while it bends for 90° degree when crossing TF-2.

Table 4-3 Summary of Transformer Balun Parameters

	TF-1	TF-2	TF-3
Metal Layer	E1 (Cu)	E1 (Cu)	E1 (Cu)
Size	110 μm*90 μm	100 μm*90 μm	100 μm*90 μm
Metal Width	5 μm	5 μm	5 μm
Winding Distance	2 μm	2 μm	2 μm
Metal Height	3 μm	3 μm	3 μm
Number of Turns P1	1.875	1.875	1.875
Number of Turns P2	1.375	1.25	1.25
Number of Turns P3	1.675	1.5	1.5
Input Matched To Source	50 Ω	50 Ω	50 Ω
Output Matched To Load	50 Ω	50 Ω	1 MΩ‖100 fF
Input/Output Signal Path	Straight	Bend	Straight

4.4.4 Simulation and Measurement

The baluns are designed and fabricated in 130 nm CMOS process. The chip micrographs and the chip area of the core parts are shown in Fig. 4.27.

The measurement setup utilized a calibrated vector network analyzer. For each balun, the S-parameters of both branches are measured independently whiles the other port is 50 Ω terminated. Then the measured result is compared with the simulated result. The IL (S_{21}) and RL (Return Loss, S_{11}) results of the baluns, together with ΔA and ΔΦ are shown in Fig. 4.28. S_{31} is not depicted here since it equals to S_{21} corrected with ΔA and ΔΦ. It can be seen that the measured results match the simulation well, except for the ΔA and ΔΦ of the L-C balun. As mentioned before, this discrepancy is due to the sensitiveness of the L-C balun to the load

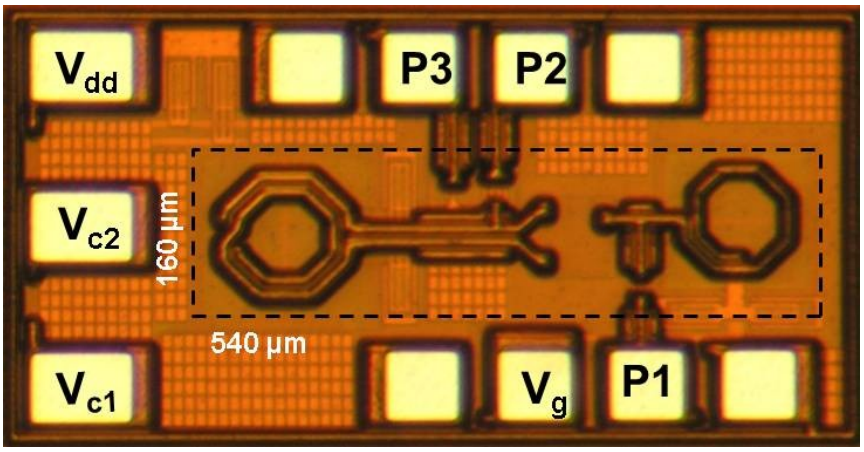
impedance variation. A slight variation of the load impedance changes the balancing of the L-C balun.

The active balun AB1 achieves a 5 GHz bandwidth from 21 to 26 GHz with ±1 dB ΔA and ±10 degree ΔΦ and an IL of 5 dB. The transformer balun TF-1 achieves a 10 GHz bandwidth from 18 to 28 GHz with ±1 dB ΔA and ±10 degree ΔΦ and an IL of 6~8 dB. The L-C balun LC-1 achieves an IL of less than 6 dB and a 2 GHz bandwidth of from 24 to 26 GHz with ±1 dB ΔA and ±10 degree ΔΦ. It should be noticed that all the IL simulated and measured here included the pad and interconnection loss. If the baluns are integrated with other circuits, the IL will be 1~2 dB lower.

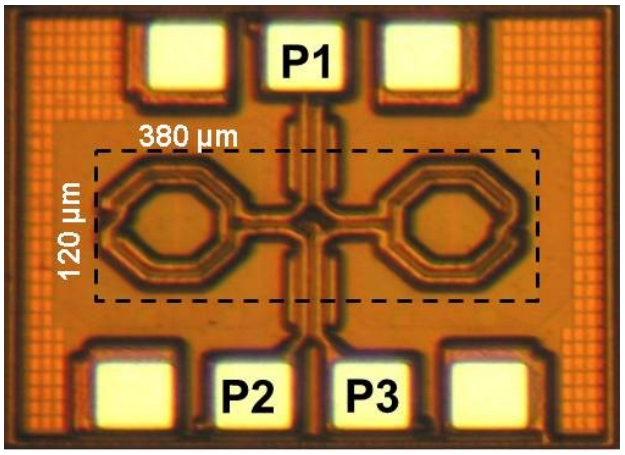
The comparison between this work and several other recently published integrated baluns is shown in Table 4-4. The designed active balun has the smallest power consumption, together with moderate chip size, bandwidth and insertion loss. The designed transformer balun has the smallest chip size, broadband and small IL when compared with other works.

Table 4-4 Summary of Balun Performances

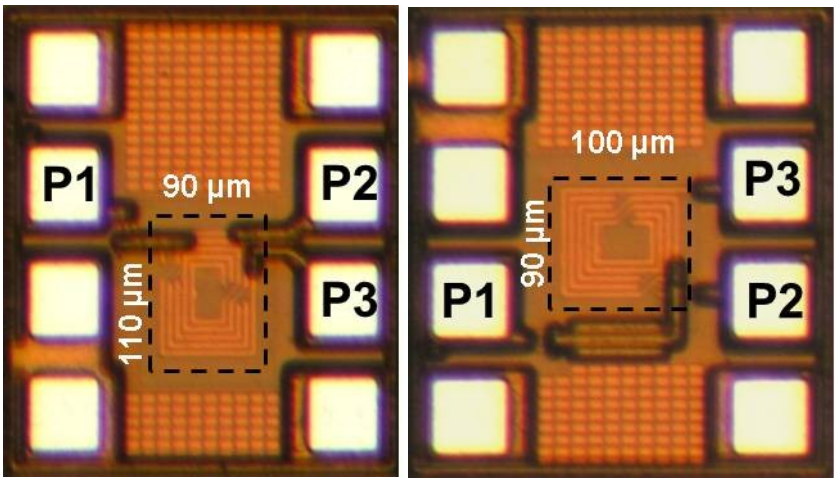
	CMOS Process	Freq (GHz)	IL (dB)	ΔA (dB)/ ΔΦ (degree)	Chip Area (mm^2)
[89]	180 nm	15-40	-9	2/10	0.06
[94]	180 nm	19-32	-7	1/5	0.073
AB-1	130 nm	21-26	-5	1/10	0.086
LC-1	130 nm	24-26	-6	1/10	0.053
TF-1	130 nm	18-28	-8	1/10	0.01
TF-2	130 nm	20-28	-8	1/10	0.01



(a)



(b)



(c) (d)

Fig. 4.27 Chip micrograph of (a) active balun AB-1; (b) lumped-element balun LC-1; (c) transformer balun TF-1; (d) transformer balun TF-2

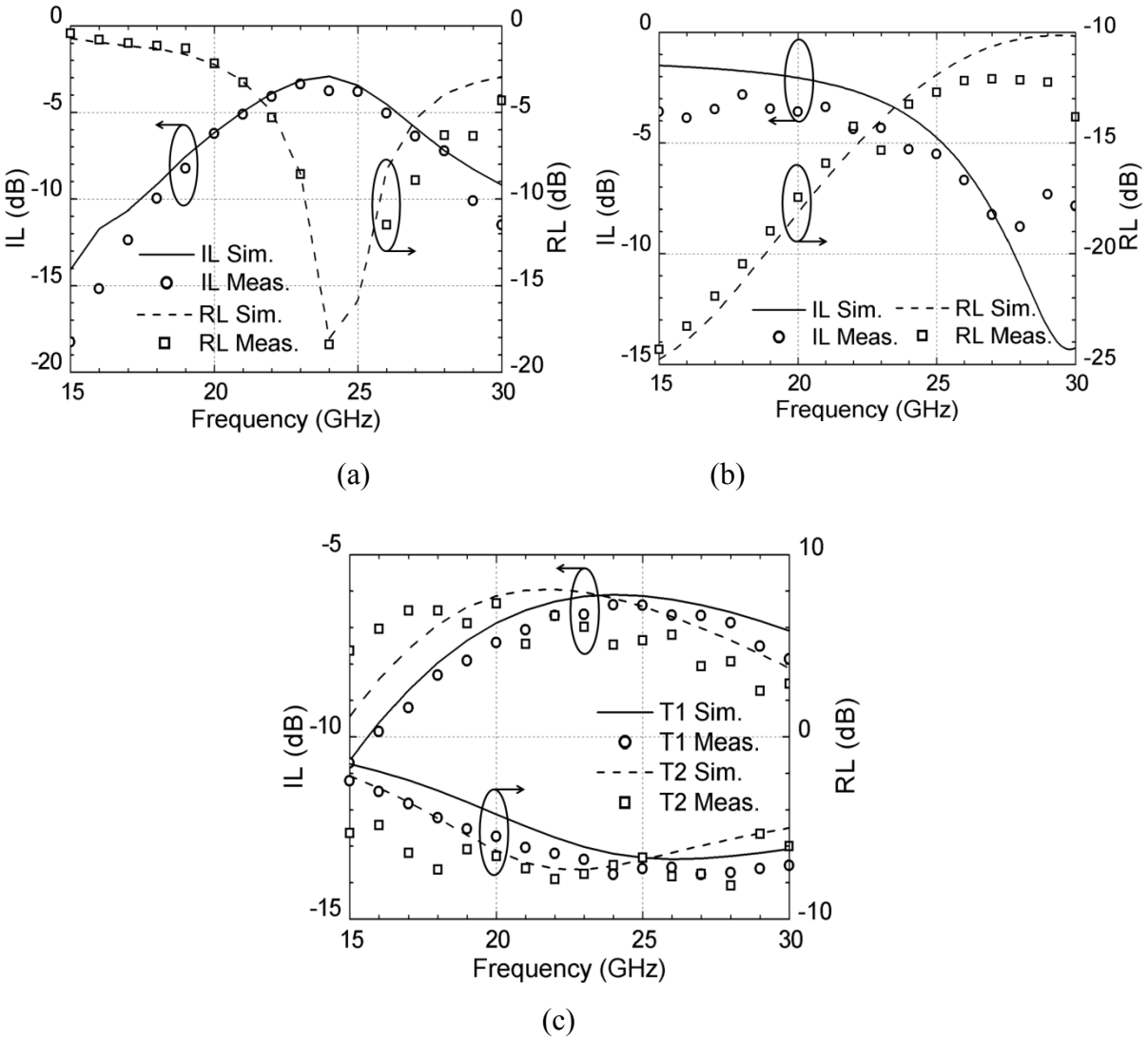


Fig. 4.28 Simulated and measured insertion loss and return loss of the: (a) active balun AB-1; (b) lumped-element balun LC-1; (c) transformer balun TF-1 and TF-2

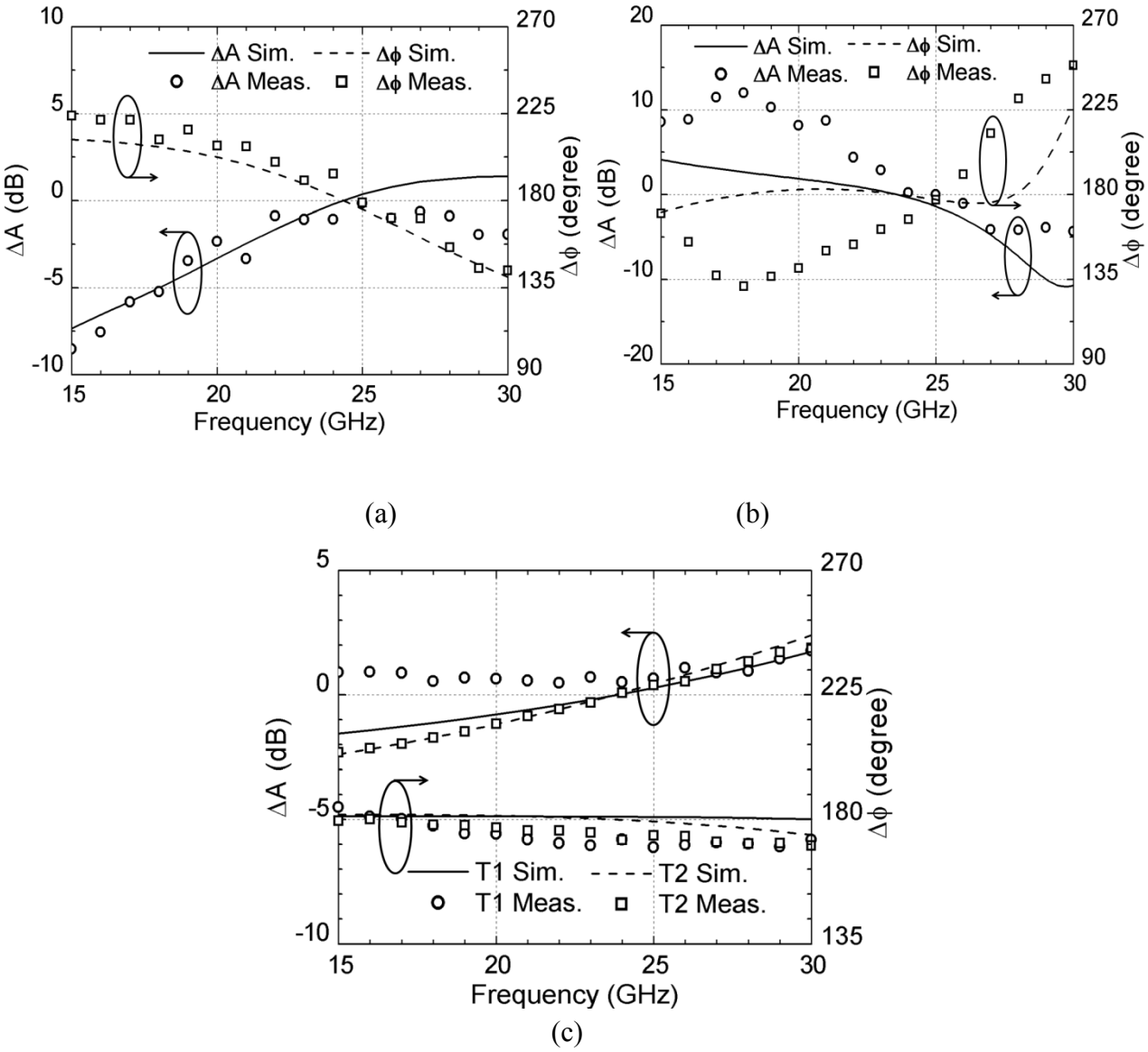


Fig. 4.29 Simulated and measured amplitude and phase imbalance of the: (a) active balun AB-1; (b) lumped-element balun LC-1; (c) transformer balun TF-1 and TF-2

4.5 Conclusion

In this chapter the process and component considerations of low power 24 GHz transceiver circuits are presented. With throughout understanding of the CMOS process, reliable model of the passive and active structures, and an efficient circuit design flow, the prerequisites of successful MMIC designs are satisfied. Three balun topologies, active balun, lumped element balun and transformer balun are compared for CMOS K-Band applications. It is found that the

active balun is a suitable choice for high gain situations, while the transformer balun is the right choice when the balun needs to be broadband and miniature. The methods to minimize the chip size of integrated baluns are discussed, while an impedance tuning method is introduced to characterize the balun performance and to simplify the integration. Based on the presented design methods, several baluns are implemented in a 130 nm CMOS process. The designed baluns are comparable with state-of-the-art realizations in K-Band.

In the following chapters, the design details of different circuits will be discussed, such as mixers, switches, receivers and transceivers. In these circuits the design considerations discussed in this chapter are implemented. Based on the solid understanding of MMIC designs in CMOS technology, the realized circuits achieved very good results compared with the other recent works in similar technologies.

Chapter 5
Mixer Design

5.1 Mixer Basics

In RF circuits, the frequency mixer is an electronic component which creates signals at new frequencies from two signals applied to it. Given two input signals at frequencies f_1 and f_2, a mixer produces a signal at the frequency of their sum f_1+f_2 (up-conversion mixer), their difference f_1-f_2 (down-conversion mixer) or $m*f_1 \pm n*f_2$ (sub-harmonic mixer).

A schematic symbol for a down-conversion mixer is show in Fig. 5.1. It is a three port component which includes the radio frequency (RF) port, the local oscillator port (LO) port, and the intermediate frequency (IF) port. In down-conversion receiver, the RF signal is the high frequency signal amplified by the LNA. The LO signal is from the local oscillator, and it is a large signal which used to turn the switching transistors of the mixer on and off. The IF signal is the low frequency signal which generated by RF and LO in the mixer.

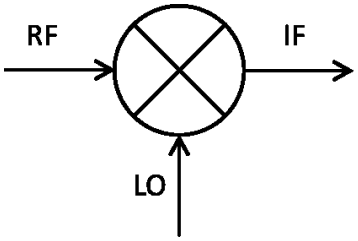


Fig. 5.1 Schematic symbol for a down-conversion mixer

Conventional mixers use diodes as switching devices. The switching diodes are usually Schottky diodes, since their cut-off frequency is much higher than normal diodes [55]. As many CMOS technologies support Schottky diodes, diode mixer could also be implemented in these technologies. The schematic of a double balanced diode mixer is shown in Fig. 5.2 [56]. The right pair and the left pair of diodes are turned on and off periodically by the LO

signal. Since the LO inputs of the diodes are considered as virtual ground of the RF signal, the RF inputs are alternatively connected to the ground. Therefore the in-phase and anti-phase RF signals are alternatively routed to the IF output as controlled by LO. The output IF signal is the RF signal multiplied by the LO squared wave.

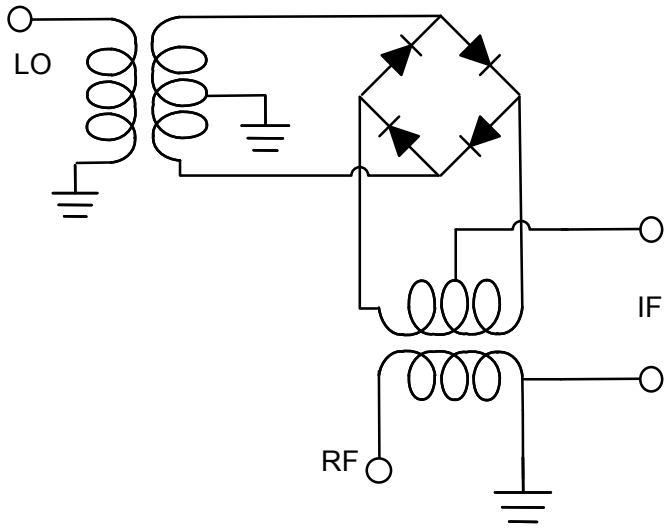


Fig. 5.2 Schematic of double balanced diode mixer

Compared with the diode mixer, the transistor based mixers are more popular in CMOS technologies these days. As shown in Fig. 5.3(a), a switch could be used as a mixer [22]. As the LO signal is a squared-wave signal which turns the switch on and off, the RF and LO signal are mixed together at the IF port. Since a transistor could be used as a switch, it could also be used in a mixer as a switching transistor. The schematic is shown in Fig. 5.3(b). Most CMOS mixers are more complicated than this topology, but the principle is similar as presented here.

The design specifications of a mixer include the operating frequency range, conversion gain, DC power consumption, LO power level, RF and LO matching, thermal noise, flicker noise corner frequency, LO-RF, RF-LO, LO-IF and RF-IF isolation, input 1dB compression point (P_{1dB}), input third-order intercept point (IIP3), input second-order intercept point (IIP2) and chip area requirement. Depending on the system requirement, the importance of the specifications varies.

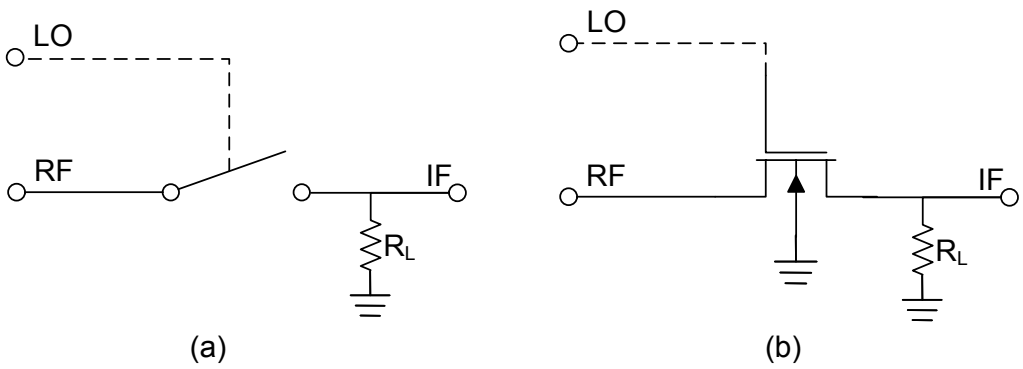


Fig. 5.3 (a) Simple switch as a mixer; (b)NMOS transistor as a mixer

These design specifications are described below.

Conversion Gain

The voltage conversion gain is defined as the ratio of the IF rms voltage to the RF rms voltage, while the power conversion gain is defined as the ratio of IF power delivered to the load to the available RF power from the source [57]. If the source, load and input impedances are same (50 Ω), the voltage conversion gain equals to the power conversion gain.

For low-IF/zero-IF receivers, voltage conversion gain is more important than power conversion gain since the load of the mixer is usually the input of analog circuit blocks such as VGA where the voltage is considered rather than power. Therefore, the load of the mixer is typically not 50 Ω, but several hundred to several thousand Ω to maximize the voltage conversion gain.

DC Power Consumption

Passive mixers do not consume any DC power, while the active mixers need DC biasing to amplify the RF signal through the transconductance stage. Since the transconductance stage works like a common-source amplifier, the DC power consumption is also similar to the common-source amplifier.

LO power level

A high LO voltage swing is required at the gate of the switching-transistor to sufficiently switch it between ON and OFF. However, to generate a high LO power, buffer amplifiers are required to be integrated with the balun, therefore the overall system DC consumption is increased.

By biasing the transistor gate, the requirement of LO power level could be reduced. For passive mixers the switching transistor gate is slightly biased below the threshold voltage, while in this case the mixer could be switched most efficiently.

Thermal Noise

According to Friis Formula for noise [58], the noise factor of a receiver (including cascaded LNA and mixer) could be expressed as:

$$F_{\mathrm{Receiver}} = F_{LNA} + \frac{F_{Mixer} - 1}{G_{LNA}} \tag{5.1}$$

Where F_{LNA} and F_{Mixer} are the noise factor of the LNA and mixer, respectively. G_{LNA} is the gain of LNA. If noise figure of the mixer is lower than the gain of LNA, the total noise figure of the receiver depends on the noise of the LNA.

The thermal noise of the mixer is not particularly important if it is integrated with a high gain LNA. For some applications such as high linear receivers, where LNA is not required, the thermal noise plays an important role and should be optimized.

For passive mixers, the thermal noise is approximately the same as the power insertion loss. To optimize it, the circuit should be designed with minimum power insertion loss. For active mixers, by dividing the mixer into the transconductance stage and switching stage, noise factor of the mixer could be expressed as

$$F_{Mixer} = F_{Trans} + \frac{F_{Switch} - 1}{G_{Trans}} \tag{5.2}$$

where F_{Trans} and F_{Switch} are noise factor of the transconductance stage and switching stage, G_{Trans} is the gain of the transconductance stage. It could be concluded that the thermal noise of an active mixer is decided by the transconductance noise if the gain of the transconductance stage is relatively high.

The noise figure (NF) is defined as the noise factor (F) expressed in decibels (dB).

Flicker Noise

Flicker noise, also called 1/f noise, is critical for low-IF and zero-IF mixers, since the down-converted spectrum extends to very low frequency. The flicker noise corner frequency is defined as the frequency point where the flicker noise equals to the thermal noise. If the frequency is lower than the corner frequency, the flicker noise is the dominant noise. If the frequency is higher than the corner frequency, the thermal noise is the dominant noise. Passive

mixers typically have several hundred kilohertz of flicker noise corner frequency, as no DC current flows through the switching transistors. Active mixers have higher flicker noise corner frequency due to the DC current, sometime approaching several GHz. Considering that active mixers introduces gain which reduce the flicker noise, they could also be interesting choices for low-IF applications.

Port-to-Port Isolation

The isolation between each two ports of a mixer is critical. Since LO is a large and dominant signal, the LO leakage should be firstly prevented. The LO leakage to the RF port goes to the LNA and even to the antenna, which interfere with the received signal or other receivers. The LO existence at the IF output desensitizes the following stage as it is still not negligible even after low-pass filtering. The RF-LO feed through brings RF signal to the local oscillator, which might defect the LO performance. The RF-IF leakage causes even-order distortion problems in homodyne receivers.

To improve the isolation between the ports, single balanced or double balanced topology could be implemented. Low-pass filters could also be used to filter the IF signal and improve the RF-IF and LO-IF isolation.

IIP3 and IP1dB

IIP3 (Input third order interception point) is obtained graphically by plotting the output power of the original signal and the third order intermodulation product (IM3) versus the input power both on logarithmic scales. The intersection point of the extension of these curves is the third order interception point. It models the nonlinearity of a device by measure the third-order non-linear term.

IP1dB (Input 1-dB compression point) is defined as the input power level when the device gain is compressed by 1-dB from the small signal situation. Theoretically IP1dB is 9.6 dB smaller than IIP3.

There is a tradeoff between IIP3 and CG as the linearity of the output IF signal is relatively stable. The OIP3 (Output third order interception point) is the sum of IIP3 and CG in decibel. Another tradeoff is between IIP3 and LO power level. High LO swings ensure the mixer linearity.

IIP2

IIP2 (Input second order interception point) is similar to IIP3, while IM3 is replaced by the second order intermodulation product (IM2). It is critical for low-IF circuits as an IM2 frequency is close to zero. It is the most complicated parameter in the mixer. The IIP2 exists mainly due to various effects such as intrinsic switch-pair nonlinearity, self mixing, LO to RF leakage, load resistance mismatch and LO duty cycle mismatch.

To optimize IIP2, highly symmetrical layout, minimum device and process mismatch, balanced LO and RF signal are required.

5.2 Circuit Design Flow

An accurate and efficient circuit design flow is the key requirement of a successful RFIC design. The topic becomes more important as circuits work at higher frequencies, as transistors become inaccurate and electromagnetic simulation becomes slow.

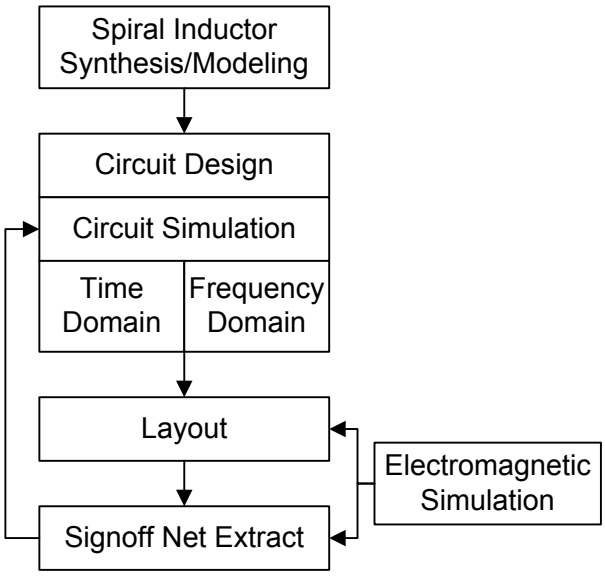


Fig. 5.4 The RFIC circuit design flow proposed by Cadence

Cadence has proposed a design flow which composed a part of the “standard” RFIC design methodology [54]. The design flow is shown in Fig. 5.4. Firstly, the spiral inductors should be synthesized and simulated. Based on the spiral inductor models and other component models

the circuit schematic could be designed and simulated both in time domain and in frequency domain. After the schematic design, the layout design could be performed. Then the layout should be modified to pass the checks such as LVS and DRC to make the circuit sign-off. Electromagnetic simulations are performed during the layout process to verify the circuit. If there are still some problems according to the simulation, the circuits should be re-designed and re-simulated again.

This design flow is practical for RF frequency designs. However, if frequency goes higher as millimeter wave, the layout parasitic influence becomes larger and larger, which results in that the electromagnetic simulation mandatory across the whole design process. This design flow separates the electromagnetic simulation with the circuit simulation. Whenever the circuit is modified, EM simulation is required to be performed once again. As fully EM simulation costs a lot of time, the whole design process becomes inefficient.

To maximize the efficiency of MMIC design, a novel circuit design flow is adopted, as shown in Fig. 5.5.

The first step of the circuit design is to build a complete component model library, including all the passive components and active components. Although some active components such as transistors have reliable models, some other active component such as varactors usually do not have precise models. Hence it would be better to have the measurement results of the active component test structures to verify their models. Besides, the passive components mentioned in Section 3.4.1 should also be modeled properly. The model libraries could be used in all circuits designed in the same technology, therefore it is built in the very beginning.

Before design a certain circuit, the circuit specifications should be clear, such as the key performance requirements of the circuit, the maximum power consumption, the chip integration requirement, the input and output DC voltage and the load and source impedance. From the circuit specifications, the proper circuit topology could be selected.

The next step is the schematic design of the circuit. The circuit might need to be modified in later design steps so the schematic design might have to be changed for several times. Then the layout of the circuit core part (usually the port connections of the transistors and the ground metal plane close to the transistors) is performed and EM modeled. The circuit core together with the transistors is simulated with other components in the schematic to examine

its influence. If the circuit core brings too much performance degradation, the parasitics can be analyzed and the core part can be re-designed.

Based on the circuit core layouts, the layout of the circuit is performed. As RF path could be divided into several sections of EM models and components, the simulation based on components and EM models could be performed. For most circuits the accuracy of this simulation is similar to the fully EM simulation. The component variables could be modified based on the simulation results.

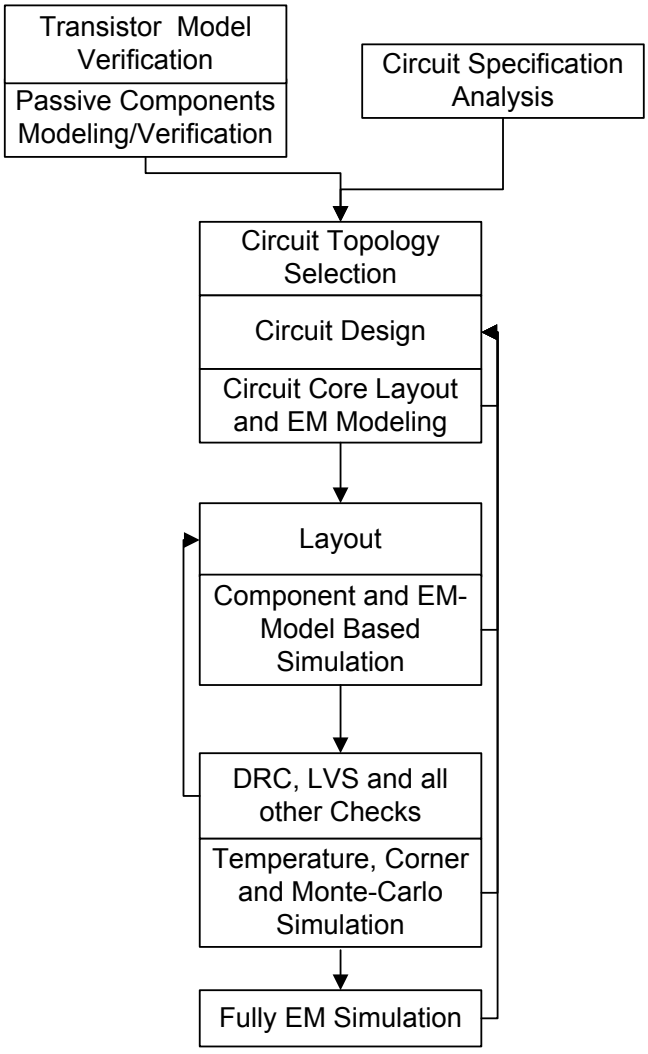


Fig. 5.5 The adopted circuit design flow

As the component variables are optimized, the DRC, LVS and other checks should be performed to clear the errors in the circuits. Various further simulations, such as temperature simulation, corner simulation and Monte-Carlo simulation can be performed to further verify the circuit. If serious problems happened in the simulations, the circuit should be redesigned.

The final step is the fully EM simulation. The simulation is to verify the pervious simulations finally. If the previous simulations have been carefully performed, the fully EM simulation just need to be done for a single time. This is also the major advantage of the proposed design flow, as this method minimized the time required by EM modeling and simulation.

5.3 Mixer Topology Selection and Specifications

CMOS mixer topologies could be classified into two categories: passive mixers and active mixers. A simple cascode-type active mixer [57] is shown in Fig. 5.6. The RF signal is amplified by the transconductance-transistor M1, then mixed with the LO signal in the switching-transistor M2 and generate the IF signal. Compared with the simple passive mixer in Fig. 5.3(b), the mixer implements the transconductance-transistor M1 at the RF input to boost the conversion gain.

To improve the isolation of the mixers, usually single-balanced or double-balanced topology is used to introduce differential RF and/or LO input. As differential signals exists at RF and/or LO input, the leakage could be cancelled at other ports.

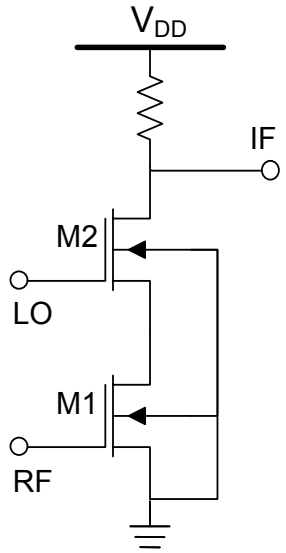
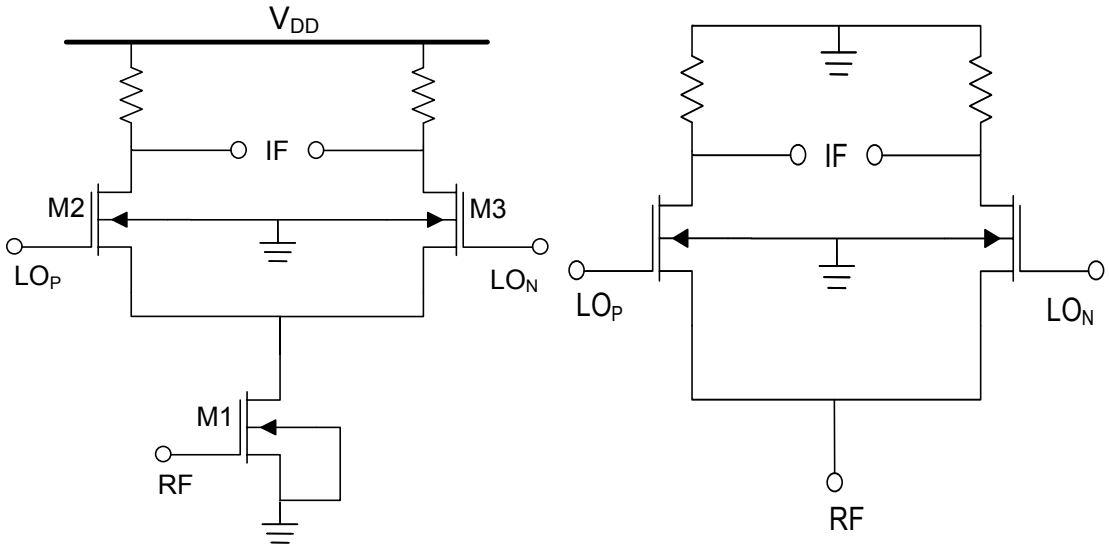


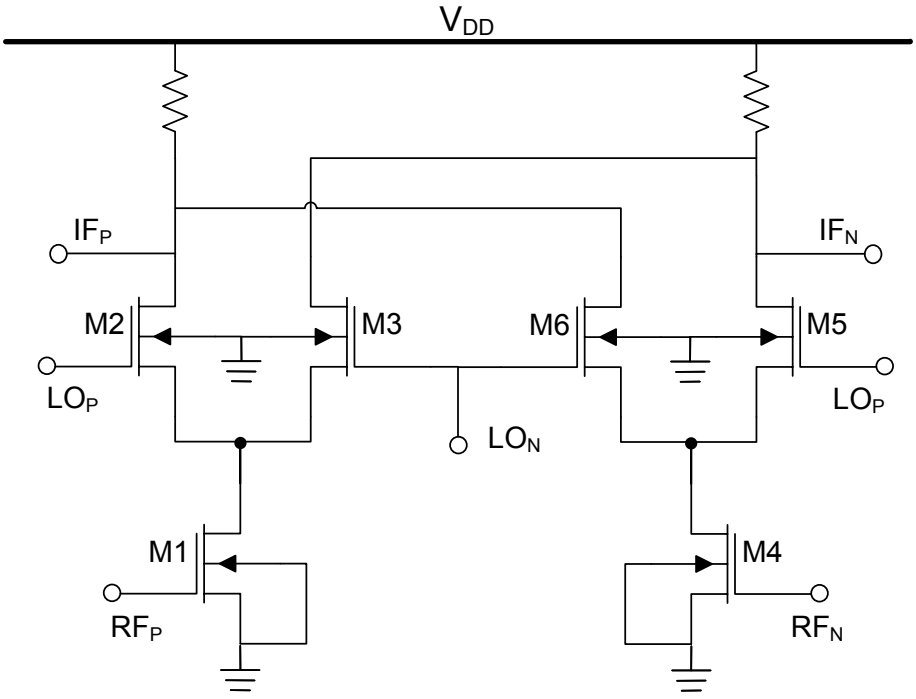
Fig. 5.6 Schematic of a cascode-type CMOS mixer

Schematic of single-balanced active mixer and passive mixer are shown in Fig. 5.7. Both circuits implement a pair of transistors as the differential LO input, the LO signals which leaks to RF cancel each other at the source of the transistors. As the IF outputs of the mixer are also differential, they can be easily integrated with the following analog circuits such as VGAs.

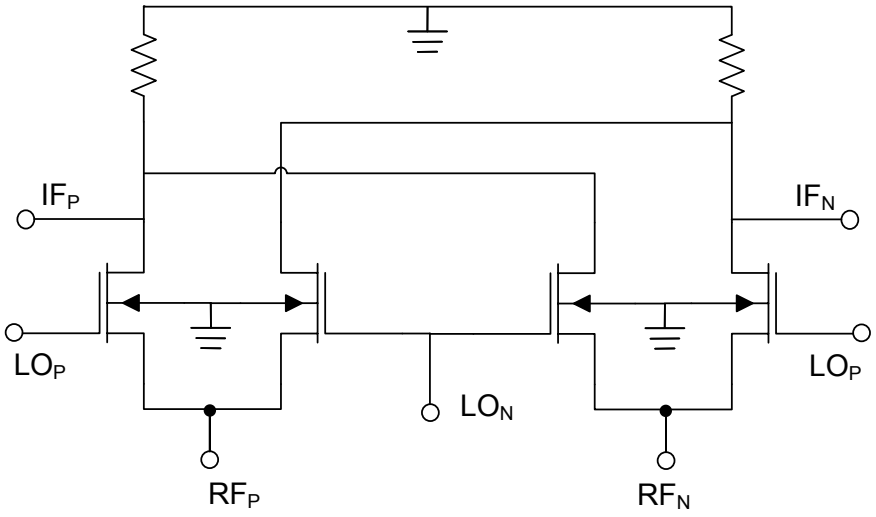


(a) (b)

Fig. 5.7 Schematic of single-balanced CMOS mixers (a) active mixer; (b) passive mixer



(a)



(b)

Fig. 5.8 Schematic of double-balanced CMOS mixers (a) active mixer; (b) passive mixer

Schematic of double-balanced CMOS mixer, which is called the Gilbert-cell mixer, are shown in Fig. 5.8. Both RF and LO implemented differential signals. The port-to-port isolation is ensured inherently since both differential signals cancelled each other at other ports. Two transconductance transistors are implemented to boost the conversion gain in the active mixer.

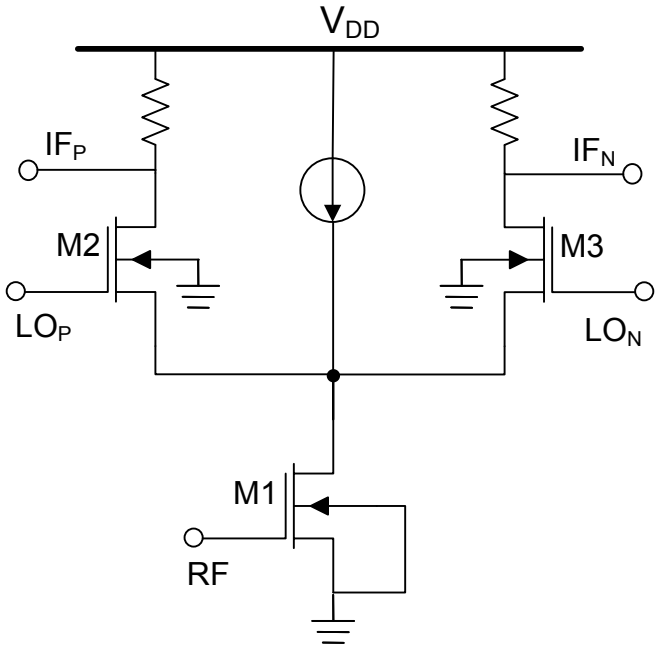


Fig. 5.9 Schematic of the current bleeding mixer

Various methods have been proposed to improve the performance of mixers, such as current bleeding [59], current reusing [60] and folded topology [61]. Here we just take current bleeding mixer as an example. The current distribution in the active mixer shown in Fig. 5.7 is not optimized, as the transconductance transistor require a relatively large DC current to provide sufficient gain, while the switching transistors do not need a large current. The current bleeding technique is introduced to optimize the current distribution. As shown in Fig. 5.9, by adding a current source parallel with the switching transistor, the DC current in both the transconductance transistor and the switching transistor could be optimized.

A low-IF mixer with minimum power consumption and minimum LO power level is required for the radar system. To realize the mixer, the topologies discussed above are compared according to their performances.

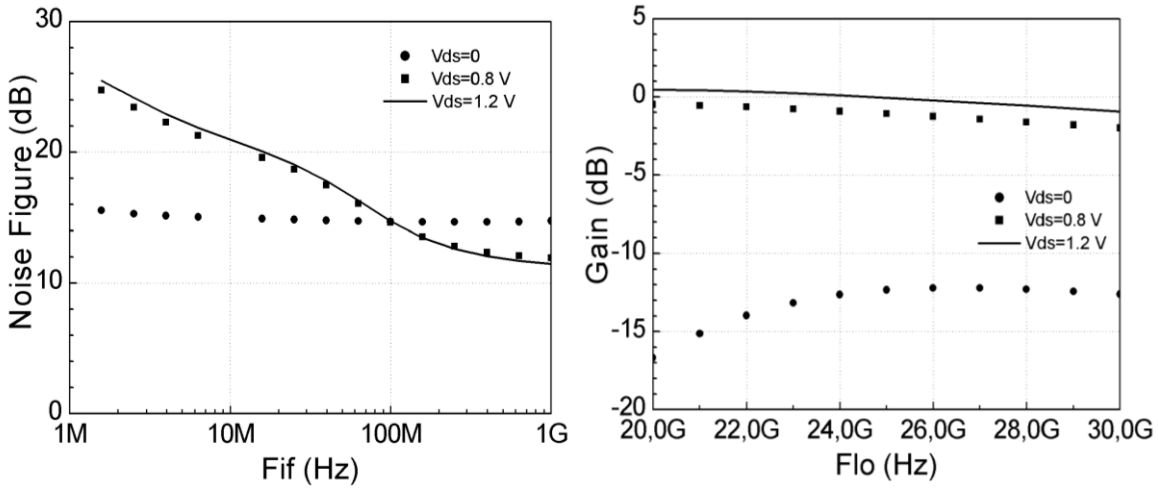
Firstly, the active mixers are compared with passive mixers. Active mixers usually have better conversion gain and less LO power level when compared with passive mixers; while passive mixers have no power consumption, less flicker noise and better linearity. Since the target system is a low IF system which needs to minimize the flicker noise corner frequency, the passive mixer topology is selected. In order to reduce the LO power level, gates of the switch

transistors are biased. The transistor models used for the passive mixers are PSP models, which is accurate when drain-source biasing is near 0.

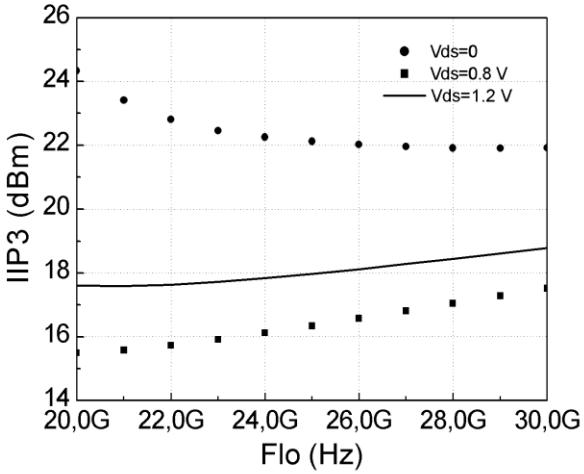
Drain-to-source voltage could be applied to resistive mixers, in that case the mixer works as a combination of passive mixer and common gate amplifier.

Fig. 5.10 shows the gain, flicker noise and IIP3 comparison of the resistive mixer with and without drain to source voltage. The drain to source voltage is 0 V, 0.8 V, 1.0 V. From this figure one can see that the mixer with drain to source biasing has 10 dB larger gain. However, the linearity is also 10 dB worse. Moreover, the flicker noise is 5-10 dB worse in the frequency range of 1-10 MHz. The resistive mixer with drain to source biasing also consumes a DC power of more than 5 mW. Considering the gain, the flicker noise, the power consumption and the linearity, finally the passive mixer structure is chosen.

Secondly, the single balance mixer is compared with double balanced mixer topology in this specific application. Single balanced mixers have larger conversion gain but worse isolation when compared with double balanced mixers. However, the double balanced mixer requires a good balun at the RF input which brings complication to the circuit design and increase the power consumption. A single balanced mixer is designed in the first several tape-outs and special techniques are implemented to reduce the isolation. Double balanced mixer with fully integrated baluns is also designed and will be discussed later.



(a) (b)



(c)

Fig. 5.10 Gain, flicker noise and IIP3 comparison of resistive mixers with and without drain to source biasing.

Thirdly, complementary switches are used in the single balanced passive mixer to improve gain and IIP2 performance. Schematic of a passive mixer with complementary switches is shown in Fig. 5.11. The insertion loss when the switch is ON (V_{gs}=1.2 V for NMOS, V_{dg}= 1.2 V for PMOS) and the isolation when the switch is OFF (V_{gs}=0 V for NMOS, V_{gd}=0 V for PMOS) are compared in Fig. 5.12. The transistor size of PMOS is 2*10 μm and for NMOS is 1*10μm.From the figure it can be seen that PMOS transistors have 2-3 dB more loss than NMOS transistors.

The gain of the complementary switch mixer and normal switch mixer are compared in Fig. 5.13(a) based on schematic simulation, while the IIP2 of the mixers are compared in Fig. 5.13(b). The reason that the complementary mixers have better IIP2 performance is presented in [59]. As described below, complementary switches can also improve the conversion loss and reduce the LO power requirement. The switch time variant conductance g(t) of a single NMOS switch transistor can be expressed by [62]:

$$g(t) = \begin{cases} \mu_n C_{ox} \dfrac{W}{L} [V_{LO} \sin(\omega_{LO} t) - V_k]_{switch=on} \\ 0 \Big|_{switch=off} \end{cases} \tag{5.3}$$

Where μ_n is the charge carrier effective mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are transistor width and length, V_{LO} and ω_{LO} are the LO magnitude and angular speed, and V_k is the model parameter.

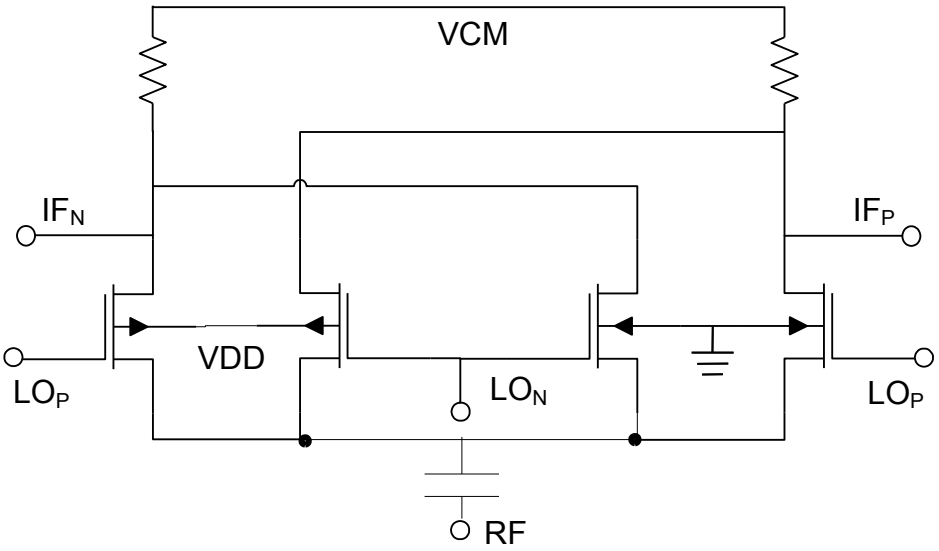


Fig. 5.11 Schematic of a passive mixer with complementary switches

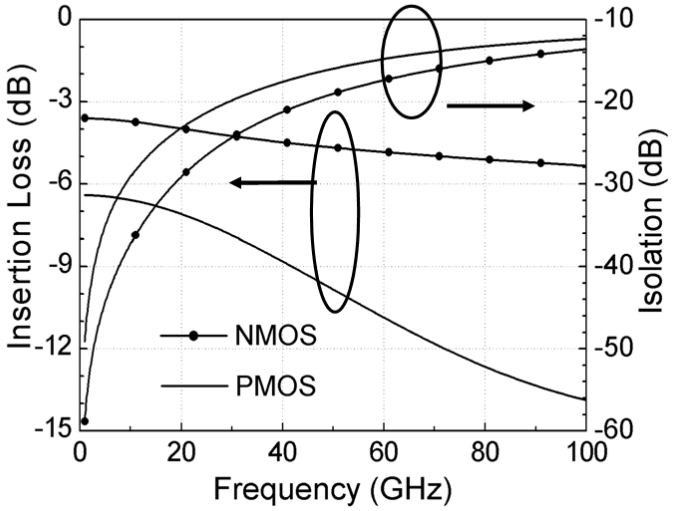
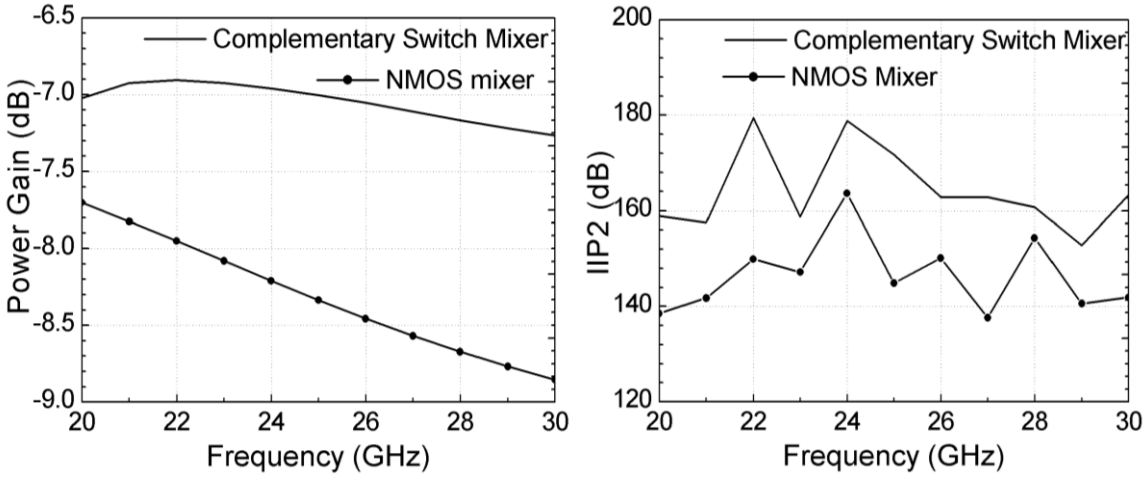


Fig. 5.12 Insertion loss and isolation of NMOS/PMOS transistors



(a) (b)

Fig. 5.13 Comparison of complementary switch mixer and NMOS mixer: (a) power gain; (b) IIP2

In a half period, M1 and M4 are switched on, while M2 and M3 are switched off. Therefore, the total time variant conductance is the sum of NMOS and PMOS time variant conductance:

$$g_C(t) = g_n \sin(\omega_n t) - g_p \sin(\omega_p t) + g_k \tag{5.4}$$

Here g_n and g_p are absolute values of the conductance for NMOS and PMOS, respectively. ω_n and ω_p are the angular velocity of the LO signal for NMOS and PMOS. g_k is a model parameter. When the LO power driving the NMOS and PMOS is 180 degree phase shifted, the time variant conductance is added together. Therefore the mixer works at maximum efficiency.

From (4.4) one can see that maximum $g_c(t)$ of complementary switches is approximately two times of g(t), while both of them is proportional with V_{LO}. Hence, when the desired gain is fixed, the LO voltage requirement of complementary switches mixer is approximately half of the NMOS mixer. Consequently, when the LO power is fixed, the gain of complementary switches mixer is larger than the NMOS mixer.

Based on the selected topology and considering the system requirements, the specifications of the 24 GHz passive mixers are listed below:

Table 5-1 Passive Mixer Specifications

RF Frequency	24.001-24.03 GHz
LO Frequency	24 Ghz
IF Frequency	1-30 MHz
Conversion Gain	-10 dB
LO Power	0 dBm
Input P1dB	-5 dBm
IIP3	5 dBm
IIP2	20 dBm
LO-RF Isolation	30 dB
RF-LO Isolation	30 dB
Thermal Noise	20 dB
Flicker Noise Corner	1 MHz

5.4 Design of Mixers

5.4.1 Single Balanced Mixer

A K-band direct conversion passive mixer MIX-1 is designed in a standard 130 nm CMOS technology. Single balanced topology is selected Due to the large frequency difference between the RF/LO and IF frequency, an R-C filter is introduced to filter the RF and LO leakage to the IF port. Therefore, high port-to-port isolation is ensured. Simulated results show higher than 60 dB isolation for all port pairs.

It has to be mentioned that the transistor model used in the simulation are PSP models [43]. Compared with the conventional BSIM4 model, the PSP models are more accurate for passive transistors, especially for large signal simulation [63].

In order to optimize the conversion gain (CG) and noise figure, the design parameters of the switch transistors should be optimized. These include transistor size, transistor bias point, load impedance and LO power. Voltage conversion gain is used here, because the analog circuits at the IF output deal with voltages.

Fig. 5.14 shows the conversion gain of the complementary switch mixer versus the NMOS transistor width and NMOS gate biasing. The LO frequency is 24 GHz and the IF frequency is 10 MHz. The PMOS finger width is fixed to two times of NMOS finger width, and V_{dg} of PMOS is set as the same as V_{gs} of NMOS. A moderate LO power (0 dBm) and large load impedance (10 KΩ) are chosen for the simulation. It can be seen that the smaller the transistor width, the better the mixer gain. The NMOS transistor width is set to 10*1 μm to minimize the insertion loss. The selected V_{gs} of NMOS is 0.4 V and V_{dg} of PMOS is 0.3 V.

Fig. 5.15 shows the conversion gain and double side band noise figure versus the load impedance and LO power. Voltage CG increases with load impedance, and the optimized load impedance for minimized noise figure is around 1 KΩ. This is because the thermal noise of the passive mixers is approximately equal to the power conversion loss rather than voltage conversion loss. Considering the tradeoff between CG and noise figure, a load impedance of 2 KΩ is chosen.

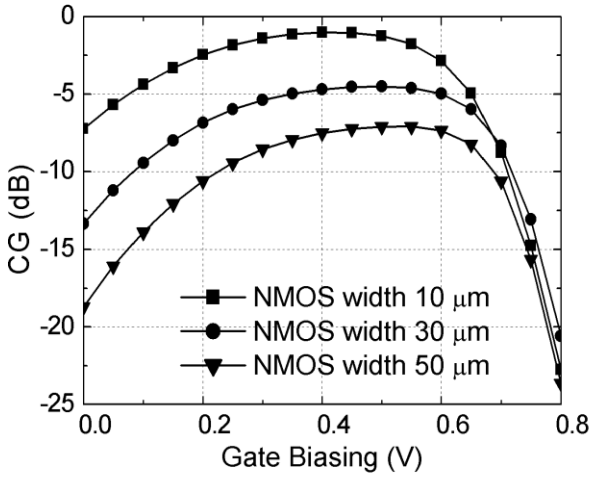


Fig. 5.14 Conversion gain versus NMOS transistor width and gate biasing

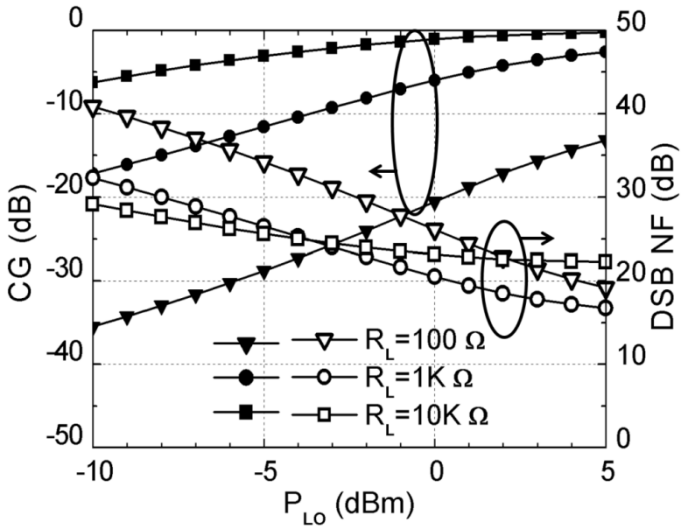


Fig. 5.15 CG and double side band noise figure (DSB NF) versus load impedance and LO power. Solid - CG, hollow – DSB NF

Fig. 5.16 shows the schematic of the designed single balanced mixer MIX-1. The RF input is matched to 50 Ω using an LC matching network. A pair of IF buffers are designed in order to match the IF output impedance to 50 Ω for measurement. In the future, these buffers will be removed and the IF will be directly connected to the VGA. The IF buffers consume 7 mW power from a 1.2 V power supply. However, they introduce approximately 7 dB voltage insertion loss at 10 MHz. Fig. 5.17 shows the layout of MIX-I. The chip size is 0.8 mm*0.6 mm. The layout of the mixer core is very carefully designed to maintain high port-to-port isolation and symmetry. High symmetry ensures high IIP2 and low noise.

MIX-1 is used for integration in other circuits. It is a building block for the next two mixers in this chapter, as well as the receivers in Chapter 7.

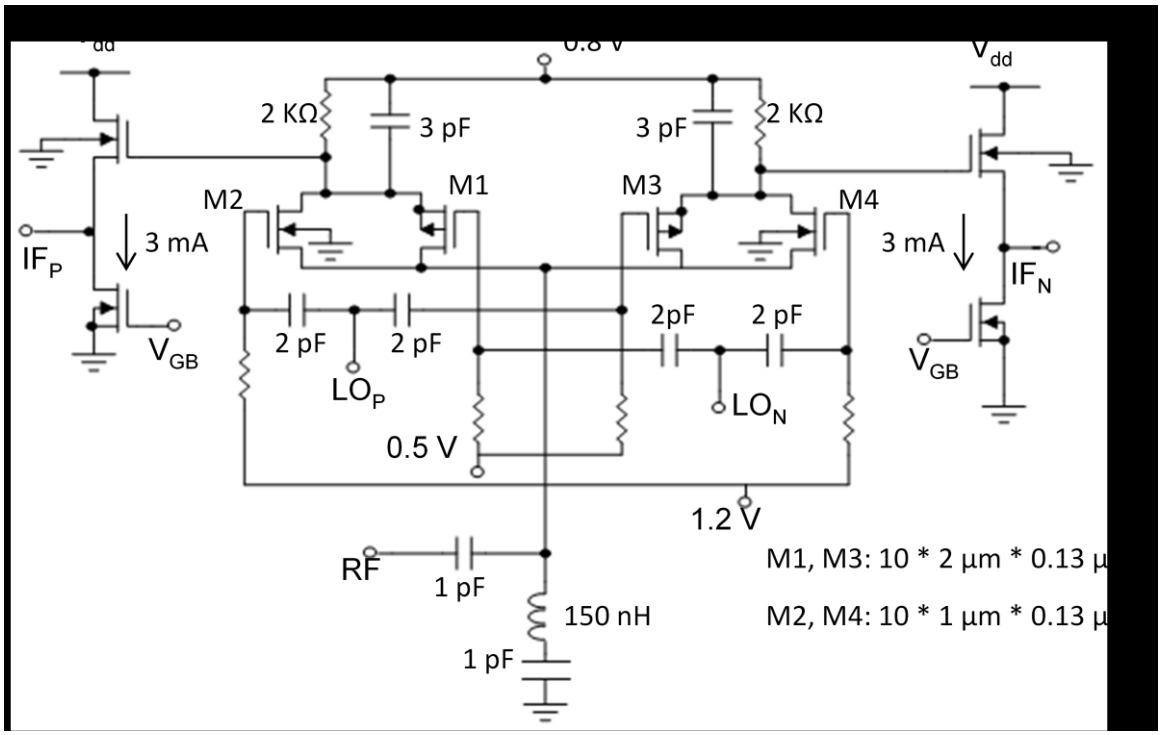


Fig. 5.16 Schematic of the single balanced mixer MIX-1

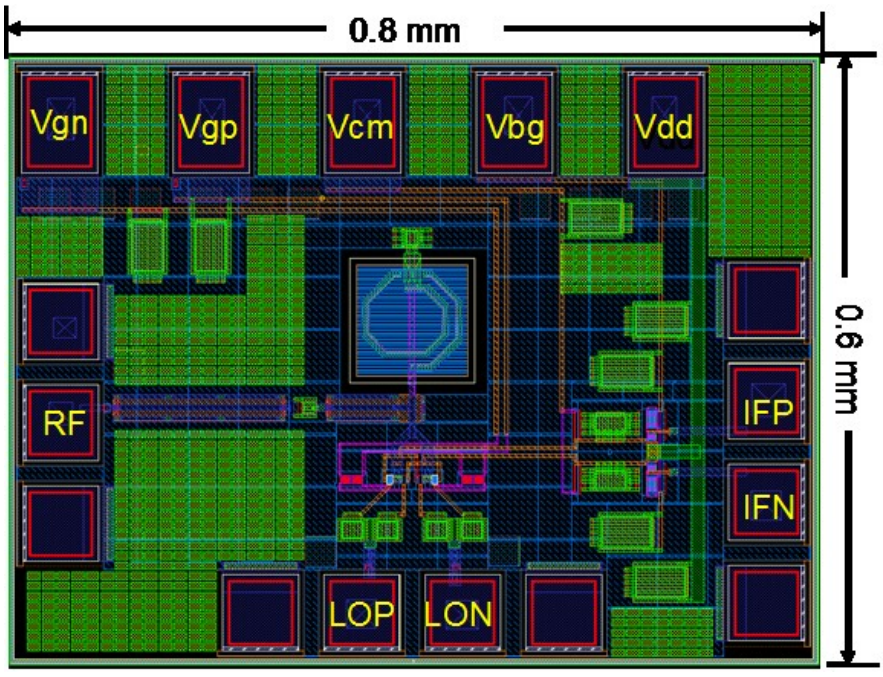


Fig. 5.17 Layout of the single balanced mixer MIX-1

5.4.2 Single Balanced Mixer Integrated with Balun

The LO input diagram for a switching transistor of a passive mixer is shown in Fig. 5.18. Here the switching transistor gate is used as the LO input. The source impedance R_S is typically 50 Ω. The load impedance is capacitive since here the load is the gate of the switching transistor. If the LO input power and source/load impedances are fixed, the LO swing is determined by the matching network. To boost the LO voltage swing, either the LO matching network should be improved, or the load capacitance should be decreased.

Fig. 4.15 shows Z_{LO} magnitude and the extracted C_{LO} of a 130 nm NMOS transistor based on the model provided by the foundry. The transistor width is swept from 10 µm to 100 µm and the gate biasing voltage varies from 0 V to 0.8 V. The simulation frequency is 24 GHz while the number of fingers is 10. Fig. 4.15 depicts that for 10 µm transistor, the LO load capacitance is around 10 fF. As the load capacitance is minimized, the LO voltage swing could be improved.

A passive transformer balun TF-3 which has good matching along both the source and load is designed to integrate with the mixer. The details of the designed balun can be found in Chapter 4.

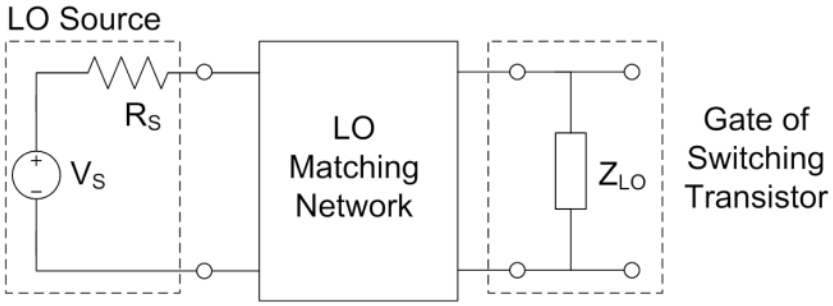


Fig. 5.18 LO input of a switching transistor in a passive mixer

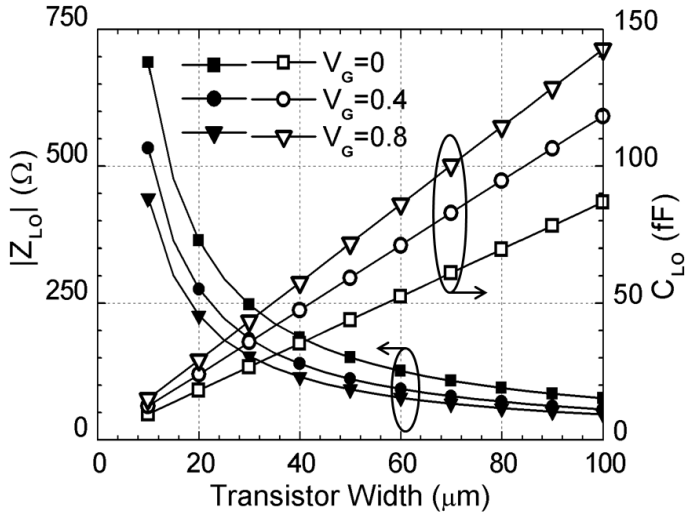


Fig. 5.19 Magnitude of Z_{LO} and the extracted C_{LO} of a NMOS switching transistor vs. transistor width and gate biasing

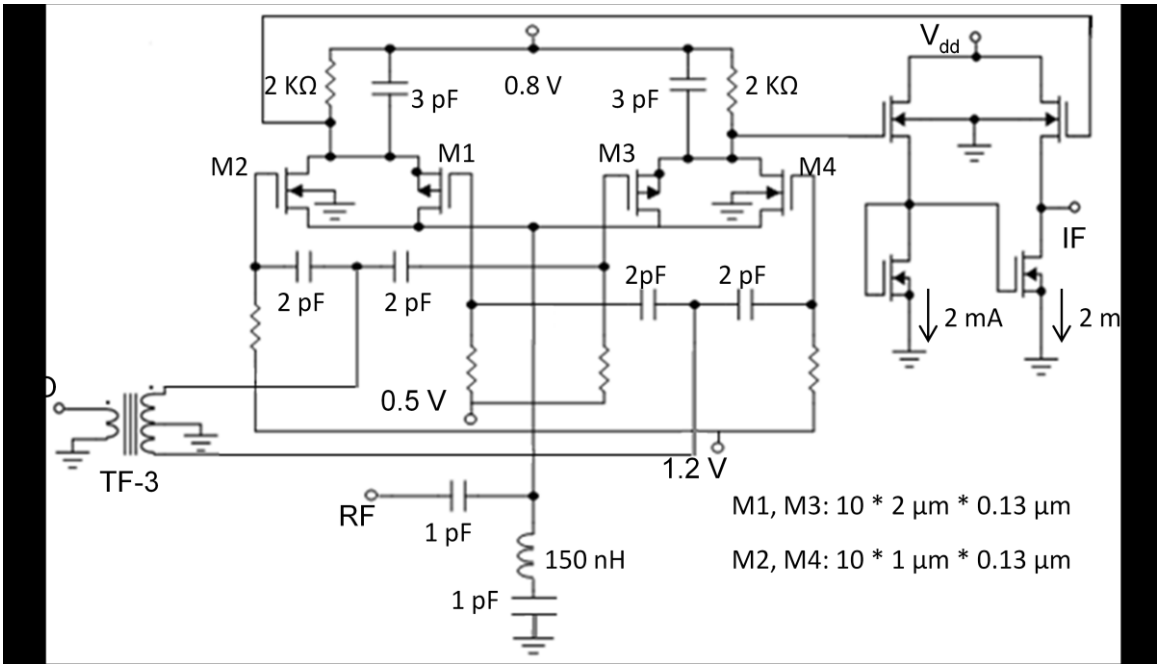


Fig. 5.20 Schematic of the mixer integrated with balun MIX-2

Fig. 5.20 shows the schematic of the mixer integrated with TF-3 balun. To simplify the measurement a differential-to-single-ended IF source follower is designed to match the IF output to 50 Ω. Due to this balun, the voltage conversion gain is decreased by 3.5 dB. The source follower consumes 5 mW DC power and is not required in the fully integrated system. The mixer core is fully EM-modeled using ADS Momentum and the impedance at the LO

ports of the mixer core is 5.7- j*63 Ω at 24 GHz, which is mainly capacitive. The layout of the balun is shown in Fig. 5.21. The chip size of the mixer is 0.8 mm*0.6 mm.

MIX-2 is later implemented in the four channel transceiver in Chapter 8.

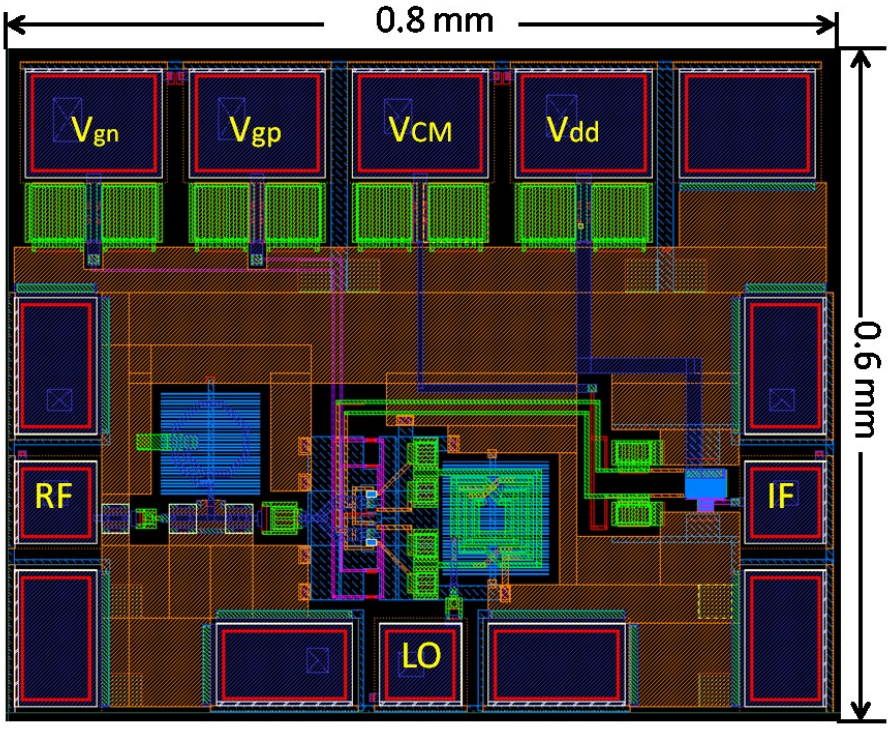


Fig. 5.21 Layout of the mixer integrated with balun MIX-2

5.4.3 Quadrature Mixer Integrated with PQF

For quadrature receivers, both I-mixer and Q-mixer is required. As discussed in Chapter 2, the LO signal need to be divided into I-signal and Q-signal. The polyphase quadrature filter (PQF) should be integrated to divide the differential LO signal to I-Q signals.

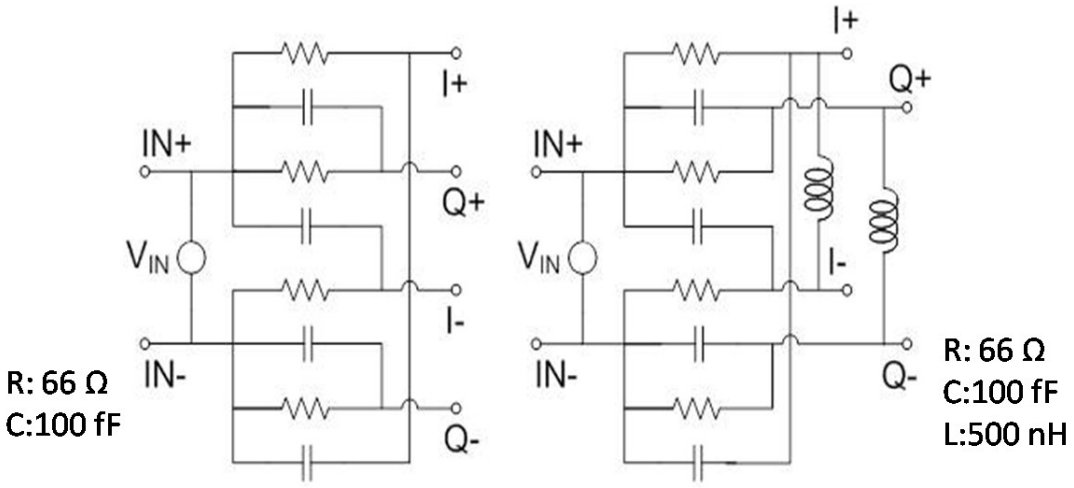
The schematic of a conventional R-C PQF is shown in Fig. 5.22 (a). It utilized the simple concept of R-C filters. The relationship between R,C and ω is given as [84]

$$R \times C \times \omega = 1 \tag{5.5}$$

At 24 GHz, the capacitance C is set as a realistic value of 100 fF, the resistance is then calculated as 66 Ω. Both R and C values can be realized on chip with relatively high accuracy.

A PQF QF-1 is designed to integrate with the quadrature mixer and the schematic is shown in Fig. 5.22 (b). Compared with the traditional PQF, this design utilizes a pair of shunt inductors between the balanced outputs. These inductors are implemented to resonant at a

particular frequency with the capacitances of the PQF and its capacitive loads. With the resonance network the LO voltage swing could be improved. Since the inductors contribute to all the branches equally, the amplitude and phase balancing are not affected. Fig. 5.23 shows the simulated LO swing versus different switching transistor widths and resonant inductor values. The simulation frequency is 24 GHz. As depicted in Fig. 5.23, if the transistor width is between 10 μm and 100 μm, the resonant inductance could be tuned between 400 pH and 600 pH to boost the LO swing. As the transistor size increases, the inductor becomes more and more influential to the LO swing. For transistor size in the range of 100 μm, the LO peak amplitude increases by 5.5 dB from 90 mV to 170 mV.



(a) (b)

Fig. 5.22 (a) Schematic of the conventional PQF; (b) Schematic of PQF QF-1 implemented in MIX-3

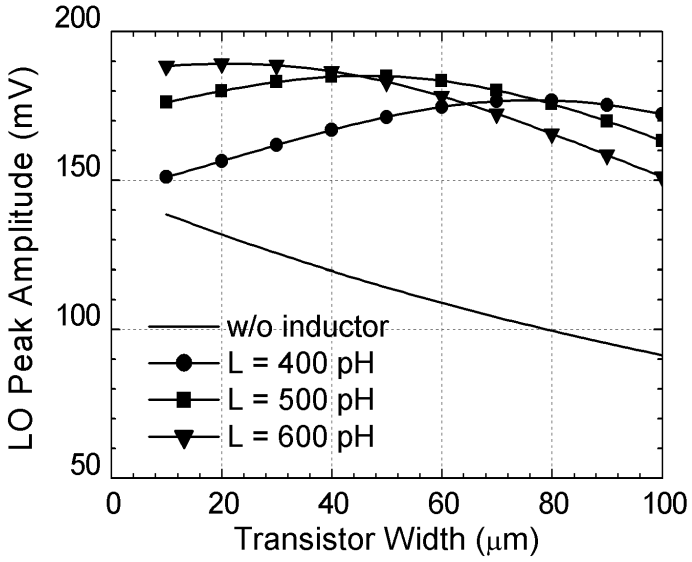
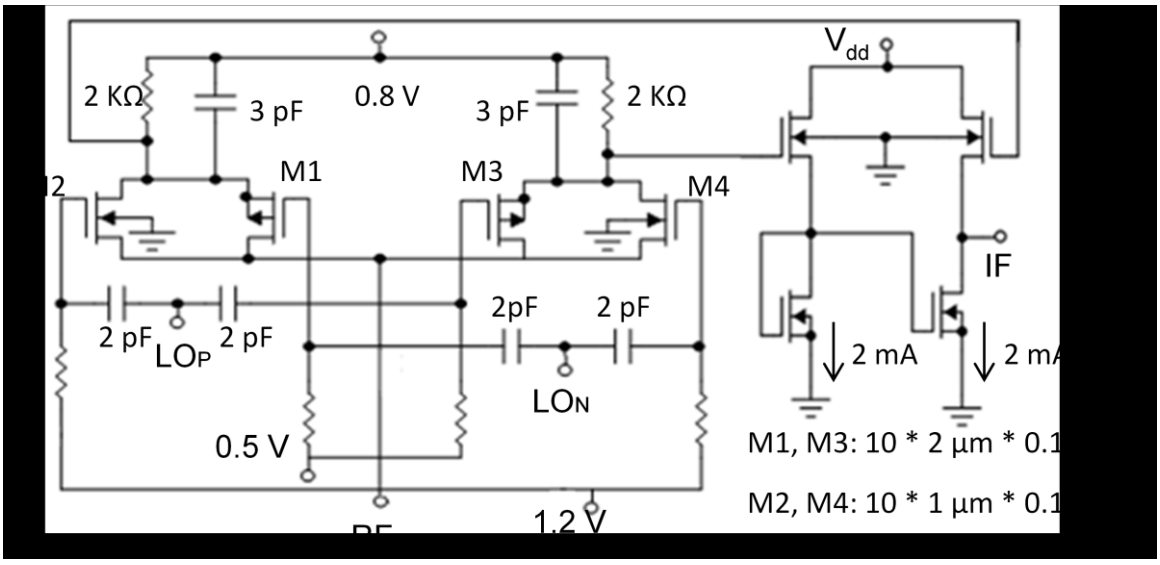
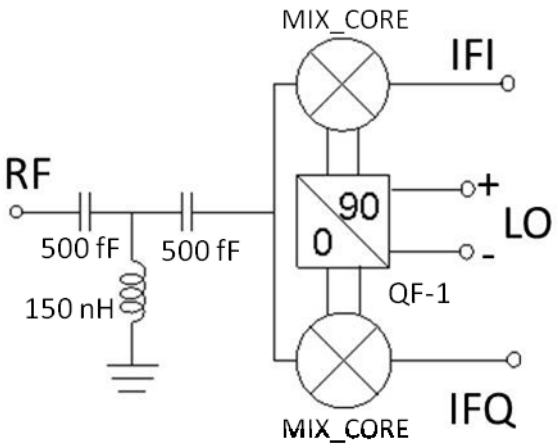


Fig. 5.23 LO peak amplitude of PQF versus transistor width and values of the resonant inductors

The mixer core shown in Fig. 5.24(a) is a single balanced passive mixer with complementary switches. The implementation of the mixer core and the source follower is similar to MIX-2, while the input matching network and LO balun is removed.



(a)



(b)

Fig. 5.24 (a) Schematic of MIX-3 core part MIX_CORE; (b) Schematic of the quadrature mixer MIX-3

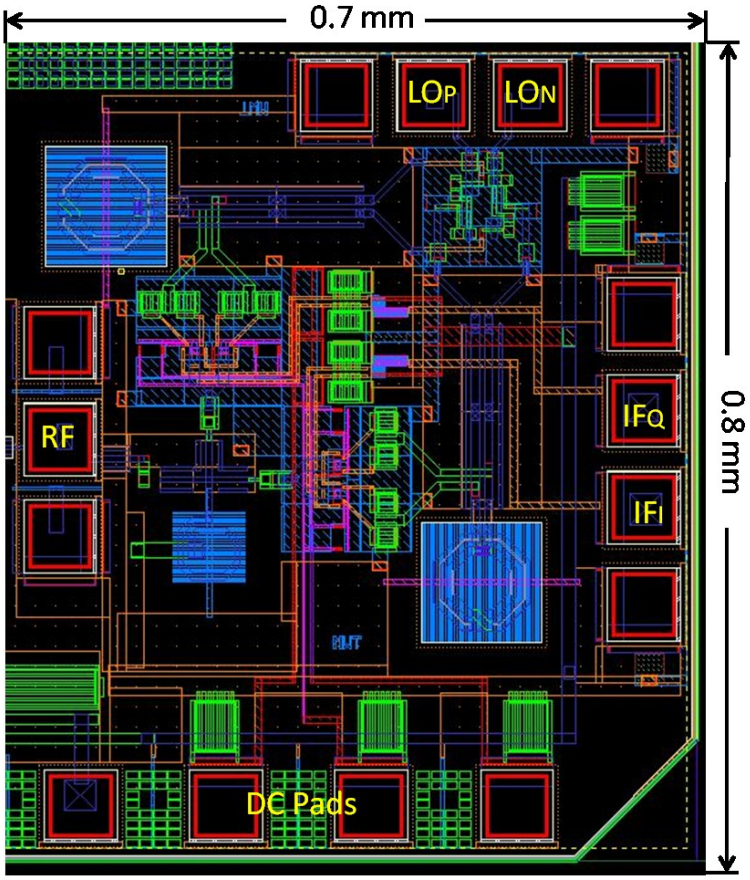


Fig. 5.25 Layout of the quadrature mixer MIX-3

The schematic of the quadrature mixer is shown in Fig. 5.24(b) the mixer core of I and Q channels are integrated with the PQF and an input matching network. The balanced LO input is converted to quadrature LO through the PQF. The RF input is matched to 50 Ω through a T-network..

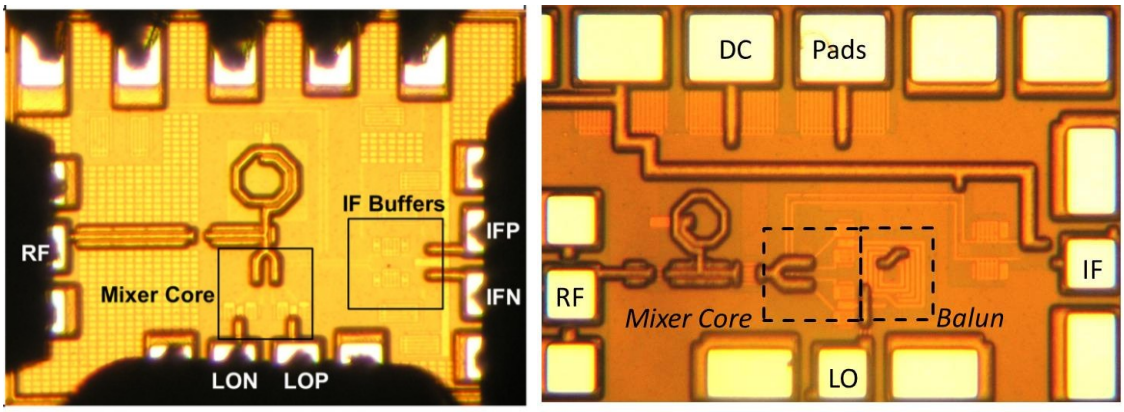
Layout of MIX-3 is shown in Fig. 5.25. MIX-3 consumes a chip area of 0.7 mm*0.8 mm.

MIX-3 is later implemented in the quadrature receiver which described in Chapter 7.

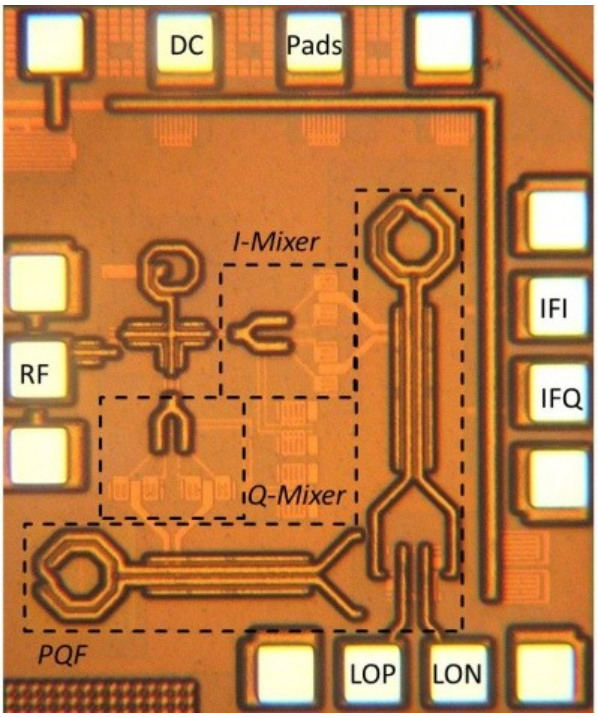
5.5 Simulation and Measurement

Based on the discussions above, three passive mixers with different integrated components in 130 nm CMOS technology are designed, simulated, fabricated and measured. These includes (1) a simple single balanced passive mixer with complement switches (MIX-1); (2) a single balanced passive mixer integrated with balun (MIX-2); (3) an IQ mixer integrated with quadrature polyphase filter (MIX-3).

The chip micrographs of these mixers are shown in Fig. 5.26. RF, LO and IF pads have 100 μm pitch. The DC pads have 150 μm pitch.



(a) (b)



(c)

Fig. 5.26 Chip micrograph of the single balanced passive MIX-1;(b) Chip micrograph of the single channel MIX-2; (c) Chip micrograph of the quadrature MIX-3

The chip is measured via on-wafer-probing with ground-signal-ground (GSG) probe for RF port and ground-signal-signal-ground (GSSG) probes for LO and IF port. Due to measurement complexities all the measurements have been performed using single ended LO. Firstly the small signal S-parameter of the RF port is measured using HP 8510C Vector Network Analyzer. For large signal measurements the RF port and one LO port are connect to signal generators, the IF output is combined using an external 180 degree hybrid and then connected to a spectrum analyzer. The measurement is carried out in a 50 Ω environment; therefore the measured voltage CG is equal to the power CG.

The measured and simulated S_{11}, CG and NF versus the RF frequency are presented in Fig. 5.27. The IF frequency is fixed to 10 MHz, while the RF and LO frequencies are swept. LO power is fixed at 0 dBm, while RF power is -25 dBm. The measured CG is -12~-10 dB for the input frequencies between 21~26 GHz. The measured NF is around 20 dB in this frequency range. There is a frequency shift of 2 GHz between the measured and simulated S_{11}. This is because of two possible reasons. Firstly, as the transistor size scales down, the transistor model becomes more and more inaccurate. The inaccurate transistor model results

in a frequency shift of 1~2 GHz. Secondly, as the transistor external connections are optimized to minimize the transistor gate parasitics, the optimum input matching shifts to a higher frequency.

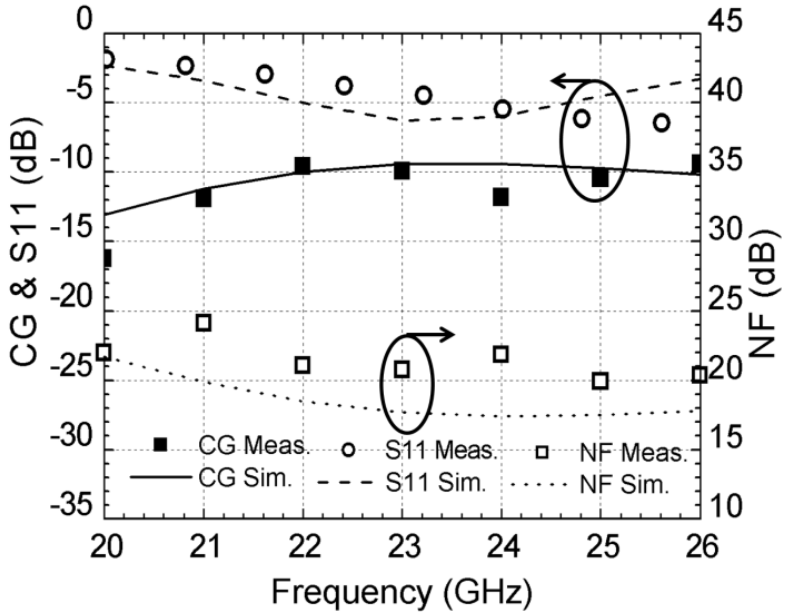


Fig. 5.27 Measured and simulated S_{11} and CG versus RF frequency of MIX-1

The CG and NF versus the LO power is shown in Fig. 5.28. The RF frequency is 24.5 GHz and the LO frequency is 24.51 GHz. RF power is -25 dBm. If LO power is below -5 dBm, CG increases and NF decreases linearly with LO power. The CG and NF become steady when the LO power is larger than 0 dBm.

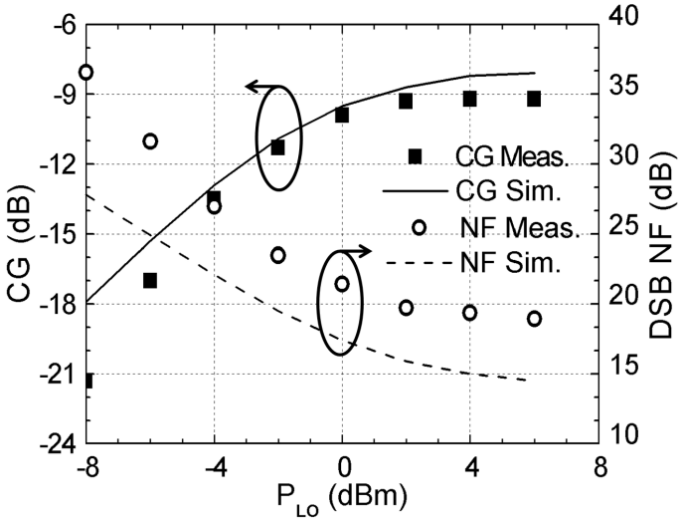


Fig. 5.28 Measured and simulated CG and NF versus LO power (P_{LO}) of MIX-1

The measured CG versus the RF power is depicted in Fig. 5.29. The RF and LO frequency are 24.5 GHz and 24.51 GHz, respectively. The LO power is 0 dBm. The RF power is swept from -25 dBm to 0 dBm. From this figure, an input 1dB compression point of -3 dBm can be visualized. The measured LO-IF and LO-RF isolation exceeds 25 dB in the frequency band of 21~26 GHz.

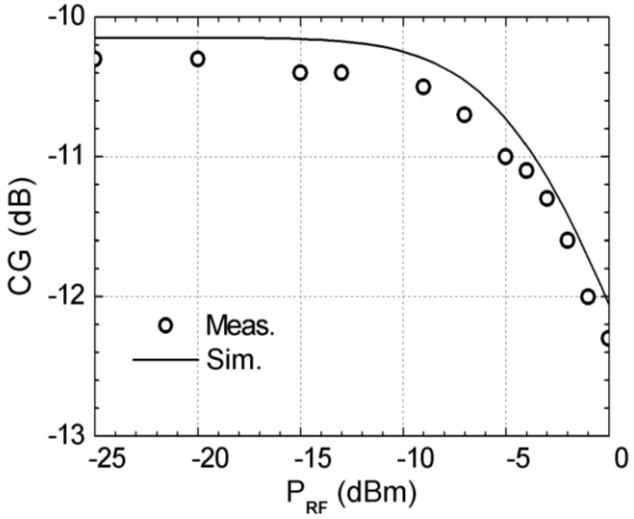


Fig. 5.29 Measured and simulated CG versus input RF power (P_{rf}) of MIX-1

Since both RF source and IF load have 50 Ω impedance, the power CG is approximately equal to the voltage CG. Therefore, after de-embedding the 7 dB insertion loss of the IF source follower, the actually voltage CG of the mixer is 7 dB higher, which is between -5 dB and -2 dB in the 21~26 GHz frequency range.

The single balanced mixer is re-designed to integrate with the balun and quadrature polyphase filter. The input-matching and output buffers are re-designed accordingly. The simulation and measurement results of the single channel MIX-2 and the quadrature MIX-3 are discussed below.

The small signal S-parameters of the RF and LO ports is characterized through HP 8510C Vector Network Analyzer. The measured RF and LO return loss are better than 8 dB at 24 GHz for MIX-2 and MIX-3.

.To measure the large signal performance, the RF and LO ports are connect to signal generators and the IF outputs are connected to a spectrum analyzer. The measurement is carried out in a 50 Ω environment; therefore the measured voltage CG is equal to the power CG.

The conversion gain and noise figure versus the RF frequency for the mixers are shown in Fig. 5.30. The LO power is 0 dBm and the IF frequency is 10 MHz. The non-IQ mixer have a minimum loss of 6 dB and the lowest NF of 12 dB at 23 GHz, while the quadrature mixer shows a minimum loss of 10 dB and the lowest NF of 19 dB at 26 GHz.

Fig. 5.31 shows the conversion gain and NF versus LO power. Both mixers are measured at 24 GHz LO frequency and 24.01 GHz RF frequency. The performance of both mixers remain unaffected if the LO power is larger than 0 dBm.

Fig. 5.32 depicts the LO-IF and LO-RF isolation of the mixers. The isolation exceeds 30 dB for both mixers. The phase and amplitude imbalance of the IQ-mixer are measured through a dual-channel oscilloscope. The phase imbalance is less than 10 degree and the amplitude imbalance is less than 0.5 dB.

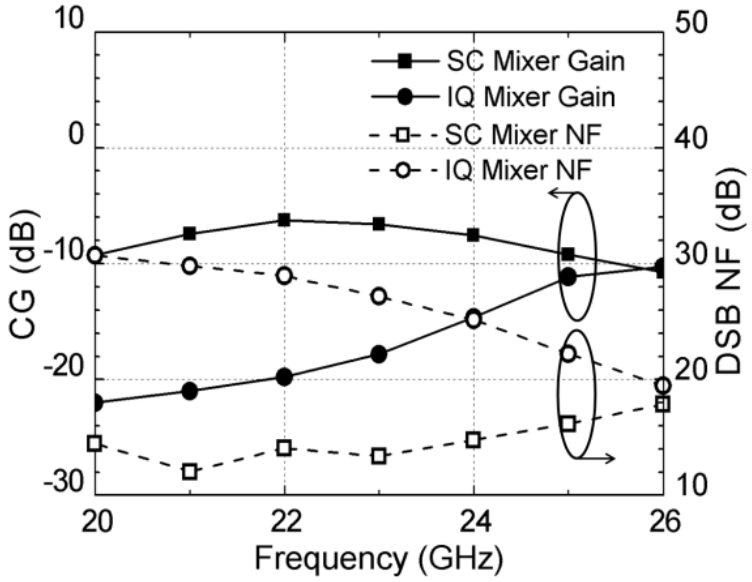


Fig. 5.30 Conversion gain and NF versus RF frequency for single channel mixer (SC Mixer, MIX-2) and IQ mixer (MIX-3)

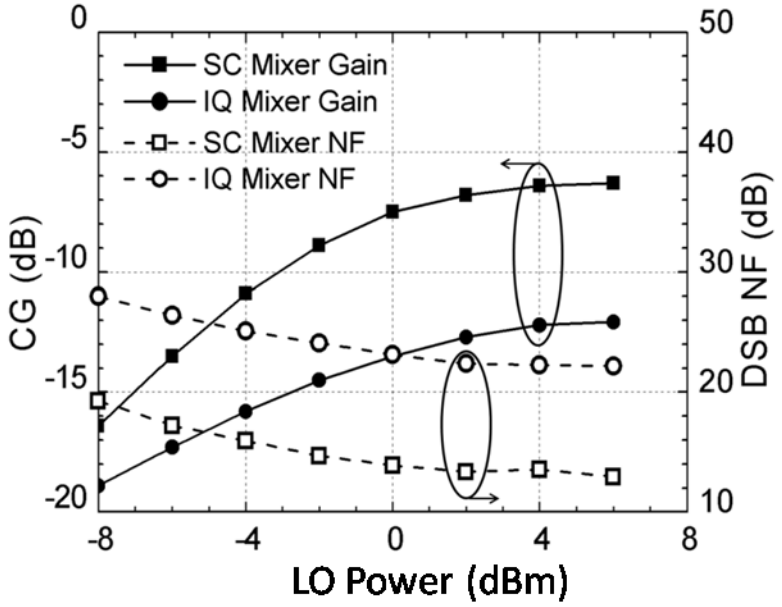


Fig. 5.31 Conversion gain and NF versus LO Power for SC Mixer (MIX-2) and IQ mixer (MIX-3)

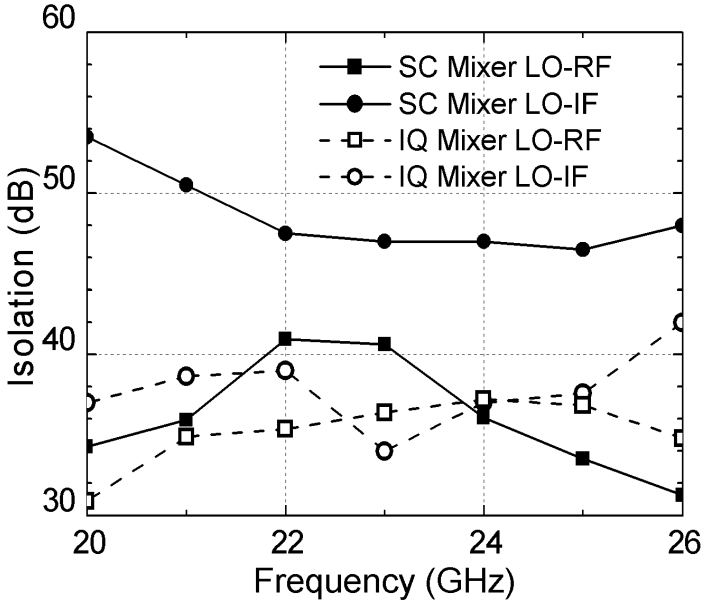


Fig. 5.32 LO-RF and LO-IF versus RF frequency for SC Mixer (MIX-2) and IQ mixer (MIX-3)

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5.6 Summary

A summary of the designed mixers and recent published CMOS passive mixers is shown in Table 5-1. The LO power requirement is much lower than the other realizations, as the mixer design and integration process is targeted to minimize the LO power requirement. The conversion loss, frequency bandwidth, input 1dB compression point and chip size are also comparable with other realizations.

All three mixers achieve the pre-defined specifications. Except for the quadrature mixer MIX-3, the conversion loss is higher than 10 dB due to the high loss of the PQF. By introduce higher LO power or higher LNA gain, the additional conversion loss could be compensated.

It needs to be mentioned that the measurements is based on single-chip circuits. If the mixers are integrated into the receivers and transceivers, the port-to-port isolation could become worse due to the couplings between different ports. In layout, the position and interconnect of the mixer should be carefully planned.

Table 5-2 Summary of Recent Published CMOS Passive Mixers

Reference	Technology	Approach	Conversion Loss (dB)	LO Power/ LO Voltage Swing	Freq (GHz)	Input P1dB (dBm)	Chip Size (mm^2)
[8]	130 nm CMOS	Sub-harmonic	6	1.8 V	24	-3	0.59
[64]	90 nm CMOS	Sub-harmonic	8~11	9.7 dBm	9~31	-3	1
[65]	130 nm CMOS	Sub-harmonic	11~12	4~8 dBm	18~26	4~10	0.4
[66]	130 nm CMOS	Single-ended	9~12	6 dBm	0.5~25	4.7	0.23
MIX-1	130 nm CMOS	Complementary Switch	9~12	0 dBm	21~26	-3	0.48
MIX-2	130 nm CMOS	Single Channel	6~9	0dBm	20~25	-3	0.48
MIX-3	130 nm CMOS	Quadrature	10~13	0dBm	24~26	-3	0.56

Chapter 6
Switch Design

6.1 RF CMOS Switches

Solid state switches are implemented widely in microwave-related applications. Most commercially available switches are PIN diode switches, while a lot of researches are also carried on PIN diode switches in recent years [95]-[98]. Practically PIN diode switches have less loss than the FET switches. Therefore they are widely used in discrete components. However, in MMICs FET switches are more favorable than PIN diodes, since few foundries support PIN diodes in their processes.

In recent years CMOS switches have been widely implemented by RFIC designers [99]-[105]. The switches are used in various applications, such as transceiver antennas, multi-standard communication modules and multi-input-multi-output (MIMO) systems. The most popular topology of T/R switch is the series/shunt architecture [99],[100]. Both TX and RX paths utilize a series transistor and a shunt transistor. When the transceiver is in transmission mode, M1 and M4 are on, M2 and M3 are off, then the TX path is turned on. The receiving mode is vice versa. The series/shunt switch is relatively easy to design, and inherently broad band. Optimum performance of the switch IL, isolation and bandwidth is possible after considering both schematic and layout design issues.

Compared with the traditional III-V semiconductor-based transistors or diodes, CMOS transistor-based switches suffer from high insertion loss (IL) and low isolation, especially for high frequencies. Special techniques have been implemented to solve these problems, such as floating bulk [99],[101],[103]-[105], negative bulk biasing [100] and on-chip L-C matching network [102],[103].

The work in [99] presents the design considerations of ultra-wideband CMOS T/R switches. Different issues, such as floating bulk (body floating) are discussed. The designed switch exhibits less than 2 dB IL and higher than 21 dB isolation up to 20 GHz. The measured P1dB is more than 30 dBm.

In [100], the floating bulk technique was introduced to reduce the effects of the parasitics, leading to enhanced linearity and power handling for the switch. This design exploits patterned-ground-shield on-chip inductors together with MOSFET's parasitic capacitances to synthesize artificial transmission lines, which result in low insertion loss over a wide bandwidth. The switch has lower than 2.5 dB IL and higher than 25 dB isolation until 20 GHz, with P1dB of 26.2 dBm.

In [101], the floating bulk (or body floating) is improved using two different methods. Firstly, the transistor layout with asymmetric drain-source region is proposed to minimize the drain-source feed-through; secondly, the floating bulk condition is switched ON and OFF to optimize the isolation. In the first design the switch achieved up to 2 dB IL and lower than 15 dB isolation until 28GHz; in the second design the switch achieved up to 2.6 dB IL and low than 21 dB isolation until 28 GHz. The linearity is 26.5 dBm and 25.5 dBm, respectively.

The work of [102] compared different single-pole single-throw (SPST) and single-pole double-throw(SPDT) designs based on series and shunt switches on low and high resistance networks. It is found that the series switch and the shunt switch with a high substrate resistance have lower IL than standard designs. Parallel resonant networks are added to the switches to optimize the performance at 35 GHz. The series SPDT switch with a high substrate resistance network shows excellent performance with 2.2 dB insertion loss and 32 dB isolation at 35 GHz. The input P1dB is 23 dBm at this frequency.

[103] introduced an asymmetrical T/R switch topology to achieve high linearity and good isolation. L-C tuned resonant networks are designed to optimize the switch at 24 GHz. The switch has 3.4 dB IL and 22dB isolation at 24 GHz. The P1dB is 28.7 dBm at this frequency.

In [104] and [105], the bulk floating technique was introduced in switches working at 900 MHz to 5.8 GHz. The switches achieved very good performance at these frequency bands.

Based on described above, we can conclude that, among the performance boosting methods, the floating bulk is of primary interest. In this chapter, the design issues of ultra wide-band T/R switches working from DC to K-band will be presented. From transistor based equivalent circuit to circuit realization, the floating bulk switch is compared with the regular switches based on standard RF NMOS transistors. An improved biasing circuit for floating bulk switches will be introduced in this chapter. Various critical aspects such as improved biasing, RF effects of passive interconnections are also discussed.

6.2 Design Considerations and Specifications

The detailed design flow of an ultra-wide-band RF T/R switch is described below.

Firstly, transistor gate length, the number of fingers and the control voltage should be fixed according to the technology limit. The gate length is set to 130 nm to maximize the operation frequency. The number of fingers is set to 10 for a trade-off between transistor model reliability and the transistor parasitics. The control voltage is switched between 0 and 1.2 V.

Secondly, the shunt and series transistor width should be optimized. Fig. 6.1 illustrates the IL and isolation of a single transistor as a function of the transistor width. Two-port S-parameter simulations are carried based on the single transistor models. For the series transistor, the ports are connected to the transistor source and drain, respectively. For the shunt transistor, both ports are connected to the drain while the source is connected to the ground. S_{21} is taken as IL and isolation as the gate voltage switches between 0 and 1.2 V. PSP transistor model is used for simulation since it more suitable when the drain to source biasing is near 0 [63]. The simulation frequency is 24 GHz.

One can see that when the transistor width is between 5 μm and 100 μm, the IL of a series transistor is above 2.5 dB. For a shunt transistor, the IL is less than 0.1 dB. Therefore, the IL of the T/R switch is mainly contributed by the series transistor. The size of the series transistor is selected as 10*3 μm. The optimized IL is 2.5 dB. In order to optimize the isolation, the shunt transistor width should be optimized. As shunt transistor width becomes larger, the isolation becomes larger, but IL also becomes worse. To make a trade-off between IL and isolation, the shunt transistor width of 10*3 μm is selected.

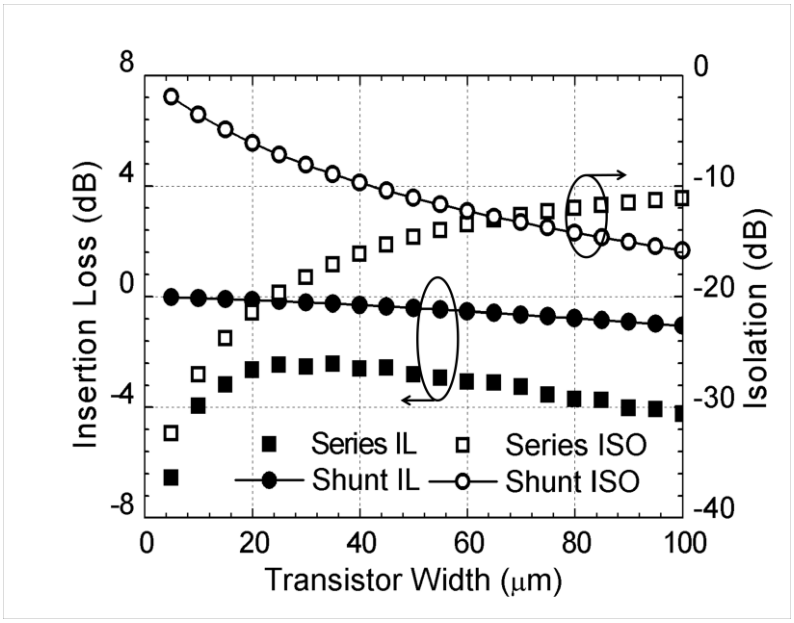


Fig. 6.1 Insertion loss and isolation of single series and shunt transistors versus the transistor width

Finally, the passive components/interconnections should be selected and the layout should be optimized. IL is affected by the interconnection, and the isolation is also deteriorated by the coupling between the passive structures. In the design, in order to minimize the IL, RF signal lines are kept straight with side-shielding, while bends and T-junctions are avoided. In order to maximize the isolation, the transmission lines of TX and RX are placed as far as possible. The block diagram of a conventional T/R switch is shown in Fig. 6.2.

The transmission lines used in the switch are 50 Ω side-shielded transmission lines on the top metal, with 6 μm width and 6 μm distance to the side shielding. The distance between the two branches is 45 μm. Considering the metal grounding and transmission line side-shielding, the coupling between the two branches is minimized. The size of the pads is 75 μm*75 μm. The passive structures are EM simulated and modeled using ADS Momentum [52],[107].

Ideal transistors are introduced to characterize the influence of passive interconnections. An ideal transistor is seen as a perfect transistor with 0 dB IL and infinite isolation. In the ON mode the transistor performs as a shorted circuit; while in the OFF mode the transistor performs as an open circuit. Fig. 6.3 shows the isolation of a T/R switch with ideal transistors based on EM simulated results. It can be see that at 24 GHz, the passive structures introduce

0.6 dB IL, and the isolation is as high as -23 dB. The IL is introduces by the loss of the transmission lines and pads, while the isolation is mainly affected by the coupling between the TX and RX channels as well as the coupling between the substrate and the passive components.

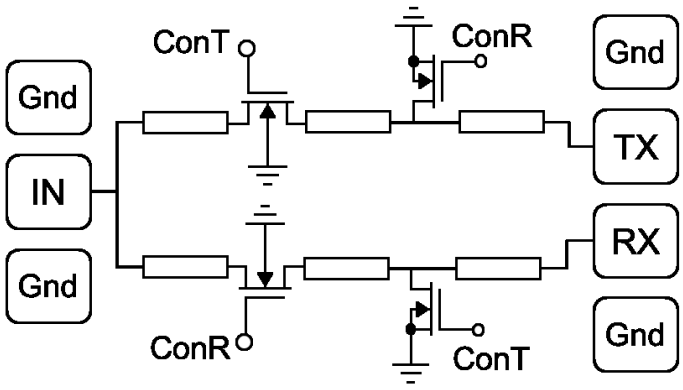


Fig. 6.2 Block diagram of a conventional T/R switch

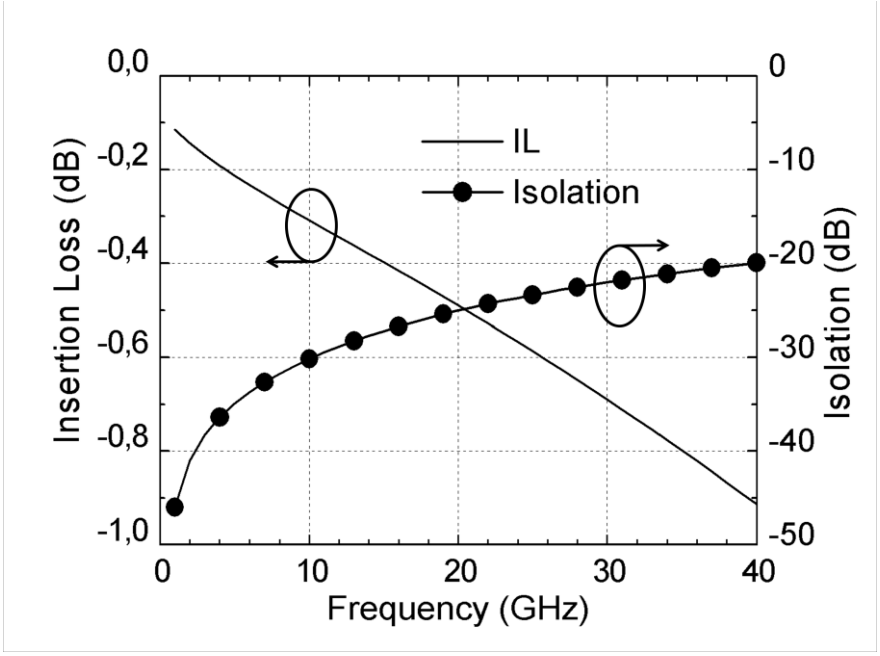


Fig. 6.3 Insertion loss and isolation of a T/R switch with ideal transistors

Based on the analysis above and considering the insertion loss and isolation of real transistors, the reasonable performance specifications of a T/R switch at 24 GHz are listed below:

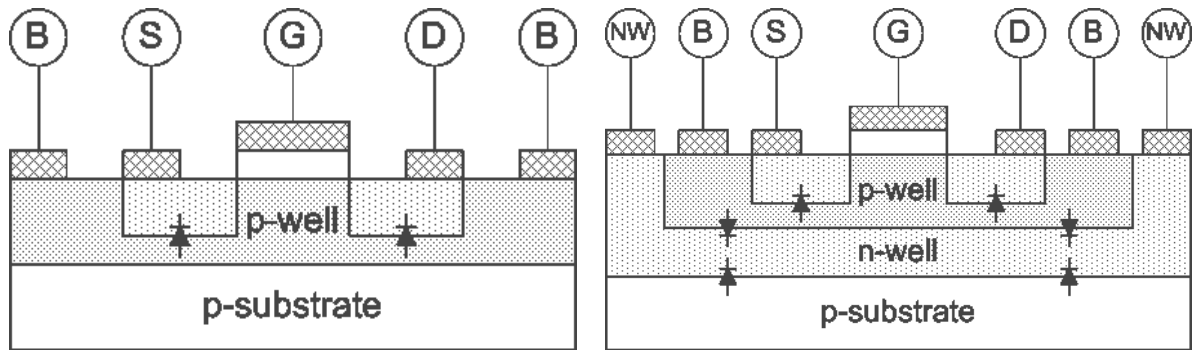
Table 6-1 T/R Switch Specifications

Operating Frequency	24 GHz
Insertion loss	3 dB
Isolation	20 dB
Input P1dB	10 dBm
Chip Size	0.01 mm^2

6.3 Floating Bulk Switch

The floating bulk is realized by the triple well (TW) transistors. Fig. 6.4 shows cross sectional views of a regular NMOS transistor and a TW NMOS transistor.

The regular NMOS suffers from the direct coupling between the source/drain and the substrate since the P-well is directly connected to the substrate. The TW NMOS introduce a deep N-well layer between the P-well and the substrate to provide sufficient isolation. Both the deep N-well and the P-well are biased through a large resistance to ensure reversed biasing of the junctions between the wells.



(a) (b)

Fig. 6.4 Cross sectional view of (a) a regular NMOS; (b) a TW NMOS

Equivalent circuit models for the regular NMOS and the TW NMOS are shown in Fig. 6.5(a), (b). For the regular NMOS, the source/drain n+ diffusion region is directly coupled with the substrate through a P-N junction. The source-drain capacitance C_{sd} and the substrate coupling capacitances C_s and C_d form a pi network.

To simplify the equivalent circuit of the TW NMOS, Y-Δ transformation is applied to transfer it to a pi network as shown in Fig. 6.5(c). The capacitances in Fig. 6.5(c) can be calculated as in equations (6.1) to (6.3)

$$C_{sd}' = C_{sd} + C_{sp}C_{dp}/(C_{sp} + C_{dp} + C_p) \tag{6.1}$$

$$C_s' = C_pC_{dp}/(C_{sp} + C_{dp} + C_p) \tag{6.2}$$

$$C_d' = C_pC_{sp}/(C_{sp} + C_{dp} + C_p) \tag{6.3}$$

Where C_p is defined as the series of C_{pn} and C_n. Therefore, the Y-parameter matrix of the equivalent circuit shown in Fig. 6.5(c) can be expressed as

$$Y_{SD} = \begin{bmatrix} g_{ds} + j\omega(C_{sd}' + C_s') & -g_{ds} - j\omega C_{sd}' \\ -g_{ds} - j\omega C_{sd}' & g_{ds} + j\omega(C_{sd}' + C_d') \end{bmatrix} \tag{6.4}$$

Converting the Y-parameter to S-parameters, the S_{21} amplitude of a single series TW NMOS is calculated as

$$|S_{21}|_{dB} = -20\log_{10}\left|1 + j\omega\frac{C_s' + C_d'}{2}Z_0 + \frac{1}{2(g_{ds} + j\omega C_{sd}')Z_0} + k\right| \tag{6.5}$$

Here Z_0 is the source and load impedance and k represent the higher order terms. IL and isolation equals to the amplitude of S_{21} with the transistors biased at different gate voltages. Therefore, the absolute value of IL and isolation increases with increasing C_s', C_d' and decreasing C_{sd}'.

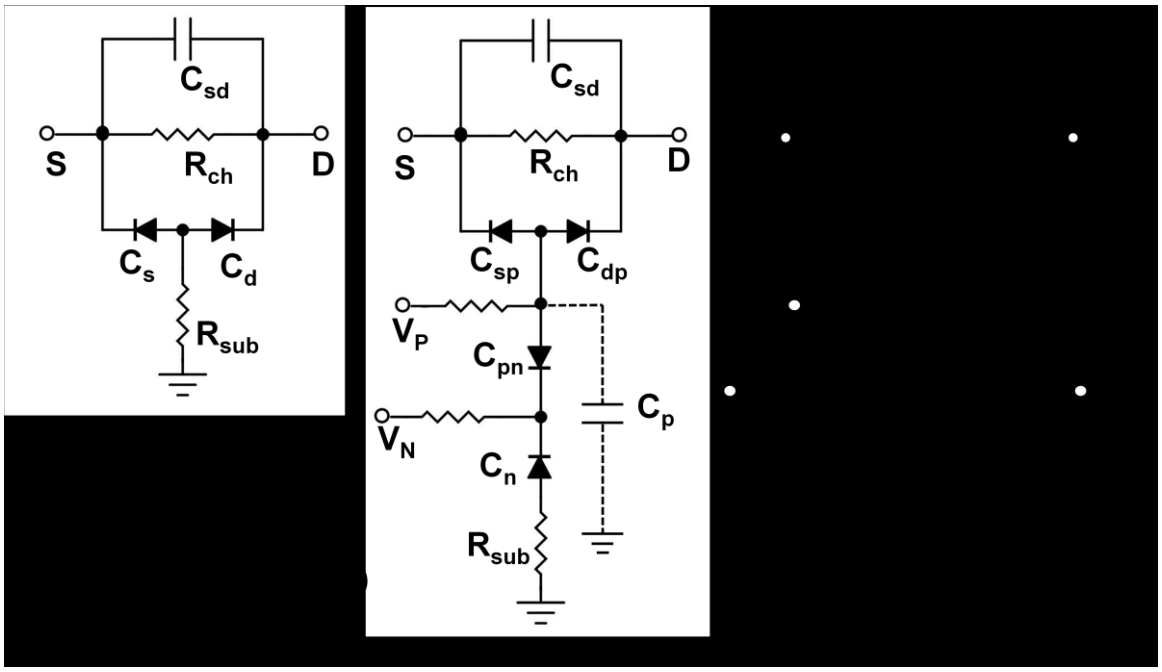


Fig. 6.5 (a) Circuit model of regular NMOS; (b) circuit model of TW NMOS; (c) equivalent Pi network of TW NMOS; (d) improved biasing circuit of TW NMOS.

As the junction reverse biased voltage becomes larger, the junction capacitance decreases. Taking this consideration into (5), several conclusions can be made. In the ON mode, in order to optimize the IL, the substrate coupling should be minimized; therefore the reversed biasing voltage of the P-N junctions should be as large as possible. In the OFF mode, to optimize the isolation, the substrate coupling should be maximized; hence the reversed biasing voltage should be as small as possible.

In Fig. 6.6, IL and isolation of a single series TW NMOS versus different V_N and V_P are depicted. The transistor has a width of 10*3 μm. The simulation results verify the above analysis. As shown in Fig. 6.6, when V_N is 1.2 V and V_P is 0.8 V, the transistor has minimum IL. When V_N and V_P are both 0 V, the transistor has optimum isolation.

The shunt TW NMOS has a different situation. Since the source is connected to the ground, the impedance of the shunt TW can be expressed as

$$Z_{SHUNT} = \frac{1}{g_{ds}} \left\| \frac{1}{j\omega C_{sd}'} \right\| \frac{1}{jwC_d'} \tag{6.6}$$

(6.6)

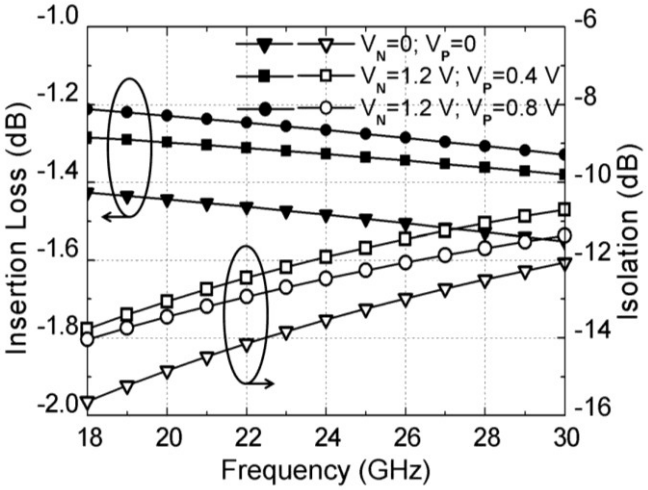


Fig. 6.6 Insertion loss and isolation of a series TW NMOS versus N-well and P-well biasing

Transform the Z-parameter to S-parameter, the S_{21} amplitude of a single shunt TW NMOS is calculated as

$$\left|S_{21}\right|_{dB} = -20\log_{10}\left|1+\frac{Z_0(g_{ds}+j\omega(C_{sd}{}'+C_d{}'))}{2}\right| \tag{6.7}$$

Since C_d' is the only parameter in (7) which strongly depends on the substrate coupling, S_{21} of the shunt TW NMOS is weakly related to the substrate coupling capacitance compared with S_{21} of the series TW NMOS. Considering that IL is very small for shunt transistors, it can be concluded that the floating bulk technique does not have much influence on the performance of the shunt TW NMOS transistors.

Table 6-2 demonstrates the estimated influence on IL by series transistor, shunt transistor and passive interconnections based on simulation. The simulation frequency is 24 GHz. The contributions of the series, shunt transistor, passive interconnections are compared here. The mismatch value presented here is the IL introduced by the source and drain impedance mismatch.

From Table 6-2, it can be concluded that the major difference between the floating bulk and regular switch is the series transistor. The series transistor provides 73% IL of the regular switch and 57% percent of the floating bulk switch. The passive structure also contributed a lot to the overall IL. Hence better performance is possible by further layout optimization. The shunt transistors do not contribute to the IL in both cases.

Table 6-2 Estimated Influence On IL Based On Simulation

	Regular Switch		Floating Bulk	
	IL(-dB)	%	IL(-dB)	%
Series	2.5	73%	1.3	57%
Shunt	0.1	3%	0.1	4%
Passive	0.6	18%	0.6	26%
Mismatch	0.2	6%	0.3	13%

6.4 Schematics and layouts

6.4.1 T/R Switch with Regular NMOS

The schematic of the T/R switch with regular NMOS (SW-1) is shown in Fig. 6.7. The transistors all have 10*3 μm width and 0.13 μm length, as discussed in section 2. The layout of the switch is shown in Fig. 6.8. It consumes a chip area of 0.4 mm*0.6 mm, while the core part only consumes 0.1 mm*0.1 mm. SW-1 is implemented in the four channel transceiver.

Fig. 6.7 Schematic of a series-shunt T/R switch with regular NMOS (SW-1) and TW NMOS (SW-2)

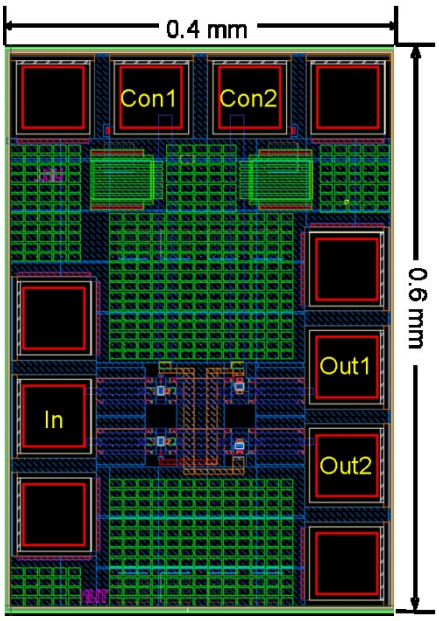


Fig. 6.8 Layout of the series-shunt T/R switch with regular NMOS (SW-1)

6.4.2 T/R Switch with TW NMOS

The schematic of the T/R switch with TW NMOS (SW-2) is the same as SW-1, the only difference is that the transistors used in SW-2 are triple well transistors introduced in Fig. 6.5 (d). Layout of SW-2 is similar with SW-2 and it is shown in Fig. 6.9.

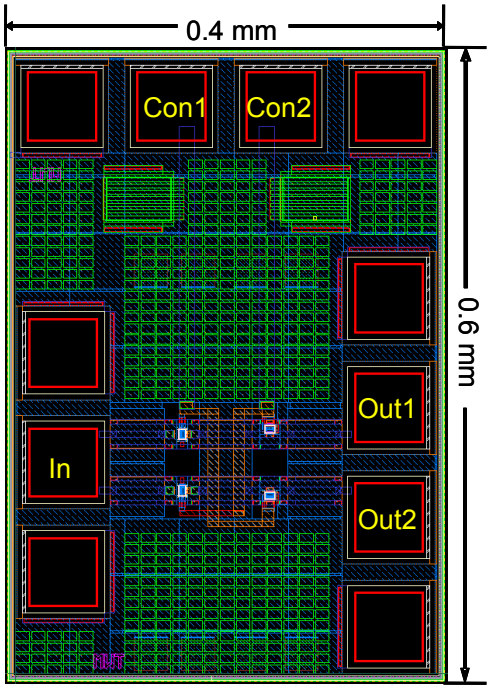


Fig. 6.9 Layout of the series-shunt T/R switch with TW NMOS (SW-2)

6.4.3 High Isolation Asymmetric Switch

In some applications, such as transceiver circuits, high TX-RX isolation is required to avoid the transmitted TX signal leakage into the RX channel. The TX leakage is crucial, since the RX channel will not be able to differentiate the TX leakage and the received signal, which might cause a lot of problems. In our application, 90-100 dB isolation is required for one branch of the switch. Therefore, a novel asymmetric cascaded topology is proposed for high isolation switches.

As shown in Fig. 6.10, the designed asymmetric switch SW-3 is quite similar to SW-1. The difference between SW-3 and SW-1 is that, three stages of series-shunted pair are cascaded together for one branch. This results in an improvement of isolation as well as an increase of insertion loss. Fig. 6.11 shows the layout of SW-3. The chip area of SW-3 is 0.4 mm*0.8 mm, while the core part is only 0.2 mm*0.1 mm.

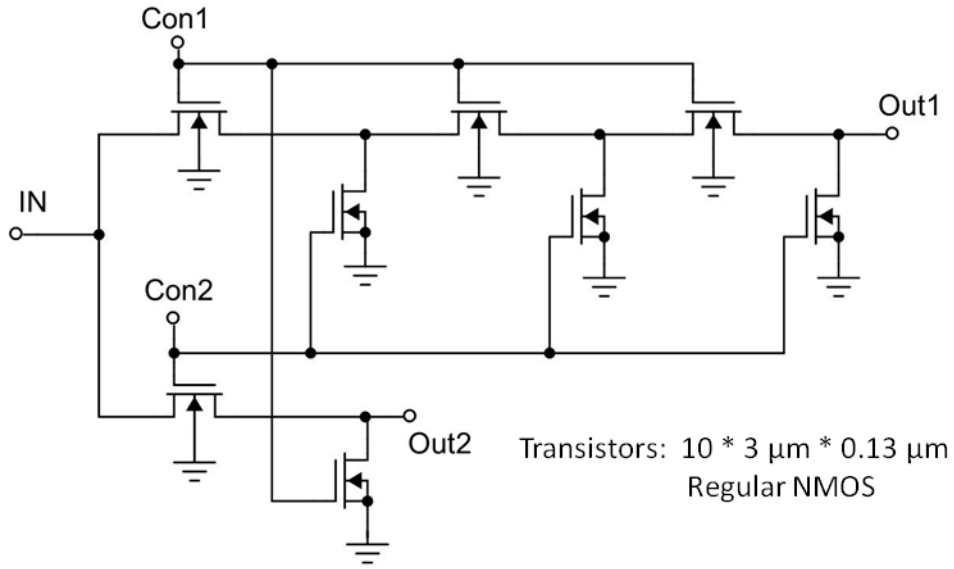


Fig. 6.10 Schematic of the asymmetric switch SW-3

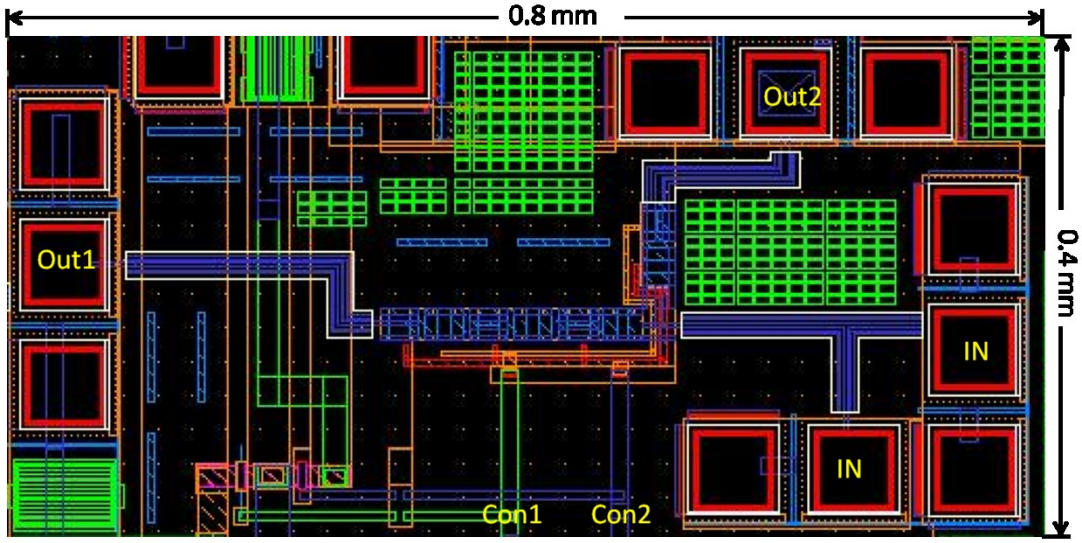


Fig. 6.11 Layout of the asymmetric switch SW-3

The insertion loss and isolation of a switch with N-cascade series-shunt pair at channel 1 and one cascade series-shunt pair at channel 2 could be estimated as

$$IL_1(dB) = N \times IL_2(dB) \tag{6.8}$$

$$Iso_1(dB) = N \times Iso_2(dB) \tag{6.9}$$

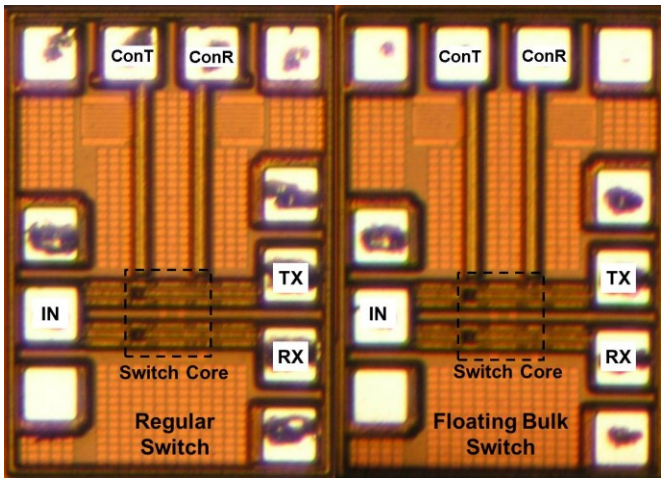
Here IL_2 and Iso_2 are similar to the IL and isolation in the symmetric switch.

According to Table 6-2, the IL of channel 2 is less than 3.6 dB and the isolation is higher than 28 dB until 30 GHz. Therefore the IL and isolation of channel 1 is less than 10.8 dB and higher than 84 dB until 30 GHz, respectively.

The two branches are placed at opposite directions to minimize the coupling between them. The high isolation switch is not fabricated and measured independently, but is integrated in a transceiver frontend [106]. The switch works properly in the transceiver.

6.5 Simulation and Measurement

Two T/R witches, SW-1 and SW-2, are designed and fabricated in IBM 8RF 130 nm CMOS process separately. One is a regular NMOS switch; the other is a TW NMOS switch with floating bulk. Fig. 6.12 illustrates the micrograph of the chips. The input-ports are on the right sides of the chips, while the TX and RX on the left side. The control voltages are depicted on the top of the chips. The switching speed is not measured; however, the layout is carefully performed to ensure that up to 1 GHz signal could be transmitted over the voltage control ports.



(a) (b)

Fig. 6.12 Chip micrograph of the (a) SW-1 and (b) SW-2

Small signal measurements are carried using a calibrated vector network analyzer. Fig. 6.13(a) shows the measured and simulated IL of the switches. Fig. 6.13(b) shows the measured and simulated isolation of the switches. The IL and isolation is measured with one supply voltage biased at 1.2 V and the other biased at 0 V. The IL of the regular NMOS switch is below 3.6 dB, and the isolation is above 28 dB until 30 GHz. The IL of the regular NMOS switch is below 2.8 dB, and the isolation is above 20 dB. The floating bulk switch has around 1 dB less IL than the regular switch in 15~30 GHz band, and the isolation of the floating bulk switch is 10 dB worth than the regular switch. The measured results have a good agreement with the analysis described in the Section 6.3.

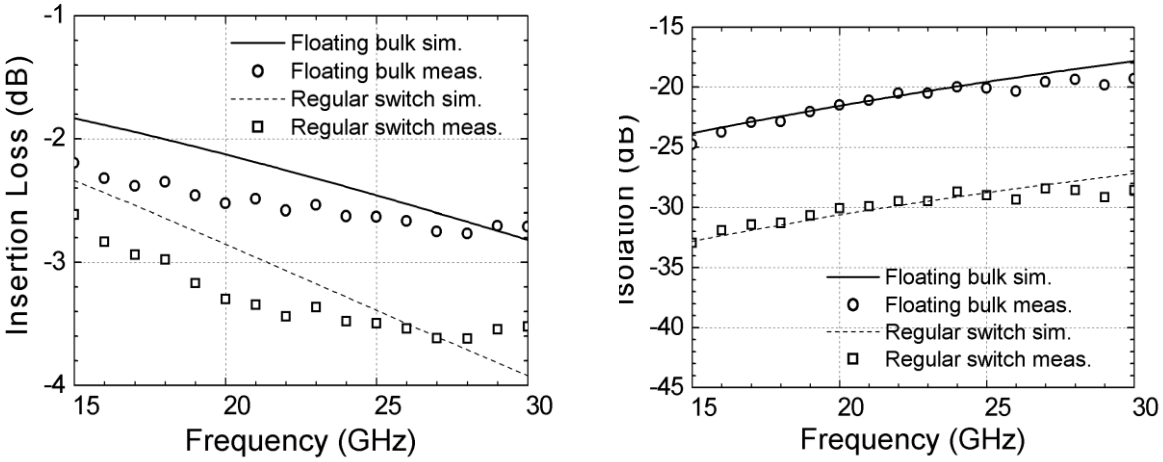


Fig. 6.13 (a) Measured and simulated IL of SW-1 and SW-2; (b) measured and simulated isolation of SW-1 and SW-2

The 1dB gain compression point is measured using a signal generator and a spectrum analyzer. The simulated and measured IL versus the input power is shown in Fig. 6.14. The frequency is 24 GHz. The P1dB for the regular switch is 14 dBm and for the floating bulk switch is 18 dBm. Higher linearity is achievable by increasing the number of fingers of the transistors while fixing the finger width and length.

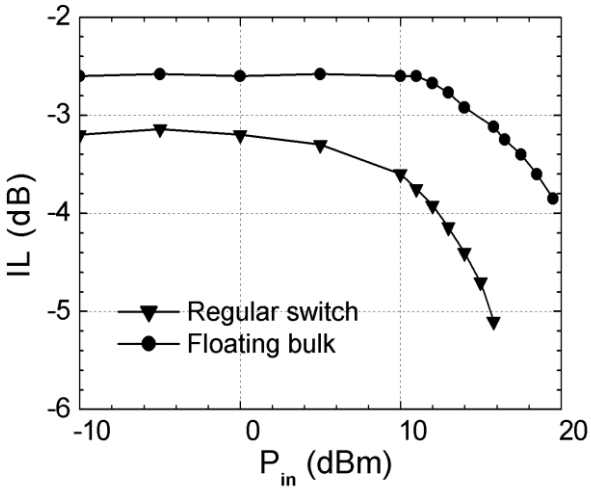


Fig. 6.14 Measured IL versus input power (SW-1 and SW-2)

Table 6-3 Summary of Recent Published CMOS T/R Switches

Reference	Technology	Approach	Freq (GHz)	IL (-dB)	Isolation (-dB)	Chip Size (mm^2)
[96]	180 nm CMOS	Ultra Wide-band	0~20	<2.5	>25	0.06
[97]	130 nm CMOS	Asymmetric D/S	0~28	<2	>15	0.015
[98]	130 nm CMOS	High R-sub Series	35	2.2	32	0.06
[99]	90 nm CMOS	Asymmetric, TW	24	3.4	22	0.018
SW-1	130 nm CMOS	Regular NMOS	0~30	<3.6	>28	0.01
SW-2	130 nm CMOS	Floating Bulk	0~30	<2.8	>19	0.01

The results are summarized and compared with the state-of-the-art passive switches in this frequency band as shown in Table 6-3. Compared with the other state-of-the-art switches, this work has achieved good trade-off between IL and isolation with a very small chip size in a wideband from 0 to 30 GHz.

From the measurement results above, we could see that the performance of the switches matches the specifications mentioned in Section 3. Besides, these broadband switches could be used for circuits of any other RF frequencies below 30 GHz.

6.6 Summary

The design of CMOS switches has been focused on the solution of two major problems. The first problem is to optimize the tradeoff between IL and isolation, and the second problem to improve the linearity of the switch. Since we are deal with a low power system, the linearity problem is not intensively studied in this work. However, we have verified that the utilization of floating bulk transistor could improve the linearity of the switch. Further enhancement of the linearity could be increase the transistor size. However, as the transistor size increases, the parasitic capacitor also increases. Therefore, inductive components could be introduced to resonant with the parasitic capacitor and maintain the IL, while this will result in the reduction of bandwidth.

The tradeoff between IL and isolation is always a problem. Since IL and isolation are the absolute values of S_{21} at different control voltages, the improvement of one performance will weaken the other performance. The floating bulk transistors are used in the designed to enhance the switch performance. Compared to the regular switches, floating bulk switches provides lower IL and higher linearity, but suffers from poor isolation. The performance of the floating bulk switch is boosted by the improved biasing circuit. With careful layout optimization, the floating bulk CMOS switch is a good candidate for ultra-wideband TX/RX realizations. The designed switches presented in the chapter achieved good IL, isolation together with wide band.

Layout and port configuration have significant influences on the switch isolation. The coupling between the ports and the branching across the air or the substrate could significantly influence the switch performance. Several techniques could be introduced to

remove these effects, such as performing the layout carefully to put the branches as far as possible, using ground metal layer to minimize the substrate coupling, adding substrate contacts between the branches to introduce an RF ground to the substrate, and so on.

The cascaded switch describe in the chapter give us another choice to re-adjust the trade-off between IL and isolation. By simply cascade several series-shunt pairs, the isolation could be improved with the sacrifice of IL. By using this technique carefully, the switch could be modified to be implemented in various applications with different system requirements.

It needs to be mentioned that the measurements is based on single-chip circuits. If the switches are integrated into the receivers and transceivers, the isolation could become worse due to the couplings between different ports. In layout, the position and interconnect of the switch should be carefully planned.

Chapter 7
Receiver Design

7.1 Introduction

In modern sub-micron millimeter wave transceivers [7], [8], [11], [108]-[111], low-IF and zero-IF receiver topologies are attractive choices particularly for higher frequency CMOS transceivers [8], [11], [111]. Owing to their simple topologies involving less number of the IF components, these types of receivers achieve relatively a smaller chip area with low power consumption. However in such receiver implementations several critical aspects like the low frequency noise, DC-offset, image rejection need to be considered [112]. In this chapter a simple single channel and a quadrature low-IF receiver have been designed and realized. The receivers are targeted for the 24 GHz low power, low-IF FMCW radar system.

The rest of the chapter is divided into four sections. In section 2 the receiver architectures are illustrated and compared. Section 3 describes the designed circuit blocks: mainly the LNA. In section 4 the measured performance of the receivers are presented and here a table comparing the achieved receiver performance with the published 130 nm CMOS receivers will also be presented. Section 5 concludes the chapter.

The mixers, PQF and buffers are designed by me and the LNA is designed by Viswanathan Subramanian [110]. The integration, characterization and measurement are performed by me.

7.2 Receiver Architectures and Specifications

The block diagram of the single channel receiver front-end is shown in Fig. 7.1(a). After low noise amplification by the LNA the received RF signal from the antenna is directly down converted to the IF signal through the mixer. Several critical aspects for this architecture

include: Low frequency noise of the MOS devices decrease the overall signal to noise ratio at low-IF. Also since these receiver types do not consider any image rejection further degradation in the quality of the received signal remain non-removable.

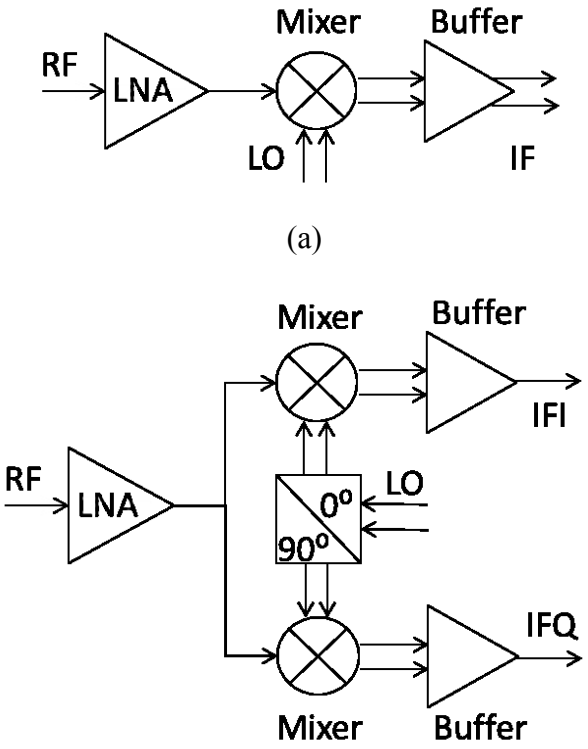


Fig. 7.1 (a) Block diagram of the low-IF single channel receiver RX-1; (b) Block diagram of the low-IF quadrature receiver RX-2

Such issues can be resolved by various techniques such as an optimized mixer design and a modified receiver topology. Fig. 7.1(b) shows the block diagram of one such modified receiver which is based on quadrature architecture. The differential LO signals are converted into a quadrature signal through a quadrature wave generator, and then mixed with the RF signal in the I-mixer and Q-mixer. The quadrature IF output is amplified through IF buffers. By employing a 90° hybrid in the IF output or through IF signal processing, the image rejection could be realized. However, compared with the single channel receiver, the quadrature counter-part is more complicated in high frequency designs. This is particularly due to the quadrature wave generation which becomes more difficult at higher frequencies.

Based on the circuit requirements and performance of the sub-circuits, the specifications of the receivers are shown in the table below

Table 7-1 Receiver Specifications

RF Frequency	24.001-24.03 GHz
LO Frequency	24 Ghz
IF Frequency	1-30 MHz
Gain	15 dB
DC Power	20 mW
LO Power	0 dBm
Input P1dB	-30 dBm
IIP3	-20 dBm
IIP2	0 dBm
LO-RF Isolation	30 dB
RF-LO Isolation	10 dB
Thermal Noise	7 dB
Flicker Noise Corner	1 MHz

7.3 Design Details

The mixer and buffer implemented in RX-1 is MIX-1. The mixers, buffers and PQF implemented in RX-2 is integrated into MIX-3. The design details of these circuits are discussed in Chapter 5.

The schematic of the LNA is shown in Fig. 7.2. In order to achieve high gain and high isolation, the LNA is based on the cascode topology. While the second and third LNA stages

do not utilize any source inductors, additional source inductor has been utilized in the first stage to achieve a wide-band input matching.

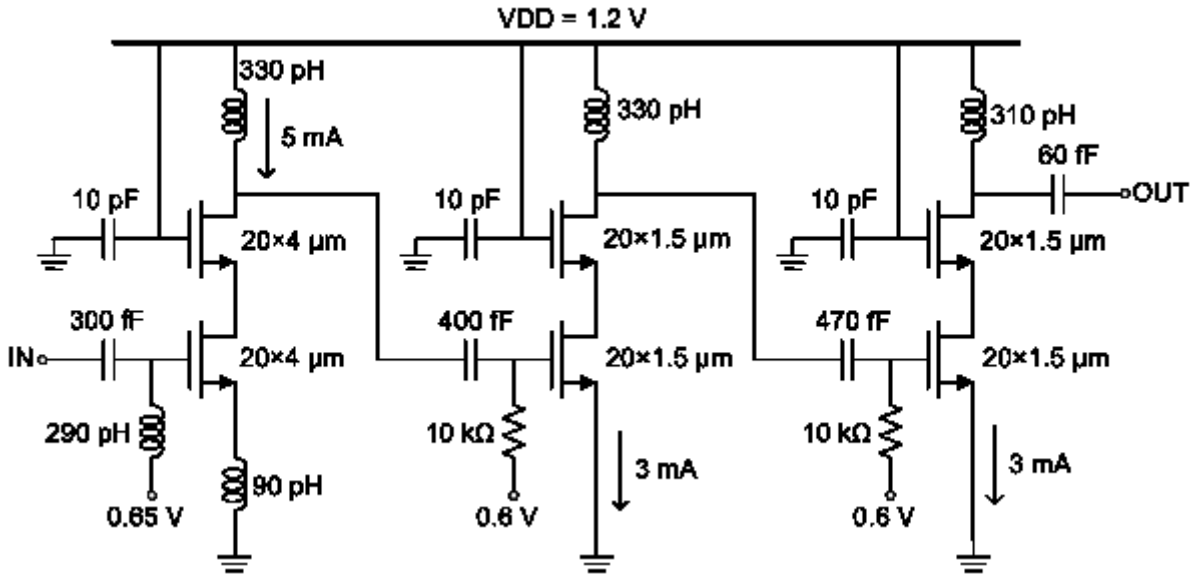
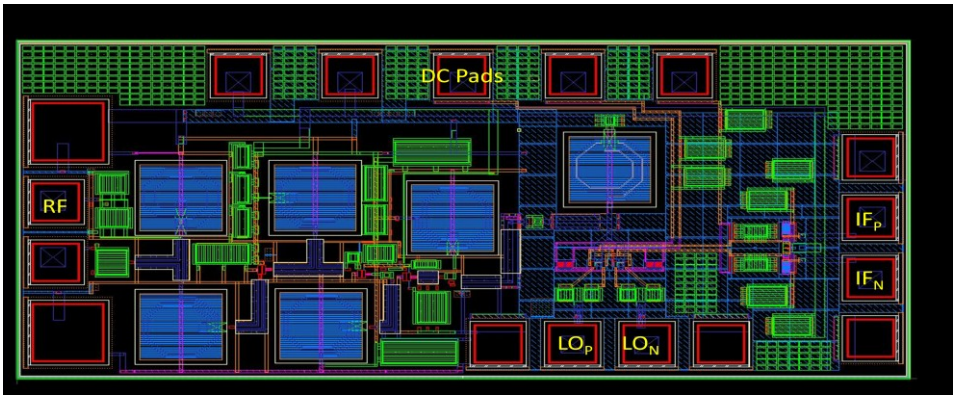


Fig. 7.2 Schematics of the LNA (LNA-1)

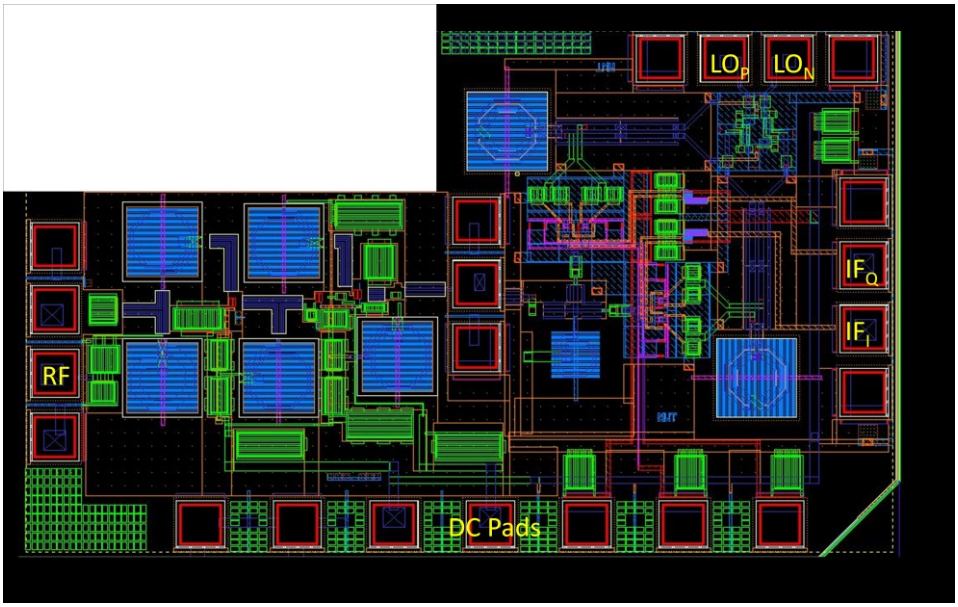
Starting from the transistor size optimization until the final circuit integration a very systematic design procedure has been followed. The LNA design has been carried out in multiple-steps, where taking the advantage of a higher isolation of the cascode stage, initially the stages are designed and optimized separately. In the final step an overall optimization is carried out after complete integration. The 90 pH inductor shown in the schematic has been utilized to simplify the LNA's input matching and facilitate simultaneous noise and gain matching. A 290 pH shunt inductor and the 300 fF input coupling capacitor forms a part of input matching network. The 290 pH inductor also functions as the DC feed for the 0.65 V gate voltage there by decoupling the input RF from the DC voltage source. It will be shown through the careful consideration of the input parasitic elements and transistor sizing, such topologies of the input matching network can result in a wide band input matching performance. The 330 nH and 310 nH inductors along with capacitors 400 fF, 470 fF and 60 fF and the parasitic elements at the output nodes form inter-stage and output matching networks of the amplifier. The 10 pF capacitors shown in the figure is the RF decoupling capacitors which are introduced to minimize the effect of the DC voltage source and the parasitic line inductance onto the RF signals. All the utilized on-chip spiral inductors are

specially designed with a patterned ground shielding based on bottom most metal layer M1. The realized inductors achieve a total size less than 75 µm * 75 µm with quality factor values better than 10 at 24 GHz in all cases. This altogether resulted in a high performance circuit with a high integration.

The mixers and LNA are integrated together as shown in Fig. 7.1. The layout of RX-1 and RX-2 are shown in Fig. 7.3. The single channel receiver RX-1 consumes a chip area of 1.2 mm*0.6 mm, while the quadrature receiver RX-2 consumes a chip area of 1.2 mm*0.8 mm.



(a)



(b)

Fig. 7.3 (a) Layout of the single channel receiver RX-1; (b) Layout of the quadrature receiver RX-2

7.4 Measurements and Discussion

LNA-1 is separately fabricated and characterized through a spectrum analyzer with an external mixer. The gain and NF is measured after de-embedded the interconnection loss and the mixer conversion loss. Fig. 7.4 shows the simulated and measured results of the gain and noise figure of the LNA as a function of the frequency. At 24 GHz, a 50 Ω noise figure (NF) value of 5 dB and small signal power gain of 21 dB have been measured. The LNA consumes 13 mW from 1.2 V power supply. The applied systematic design and development techniques [52] led to a good agreement between the measured and simulated LNA performance resulting in a noise and gain optimum at the targeted 24 GHz design frequency. Due to a wideband input matching of the LNA, a gain variation of less than 3 dB from 22.5 GHz to 26 GHz and an average noise figure value of around 5.3 dB have been achieved.

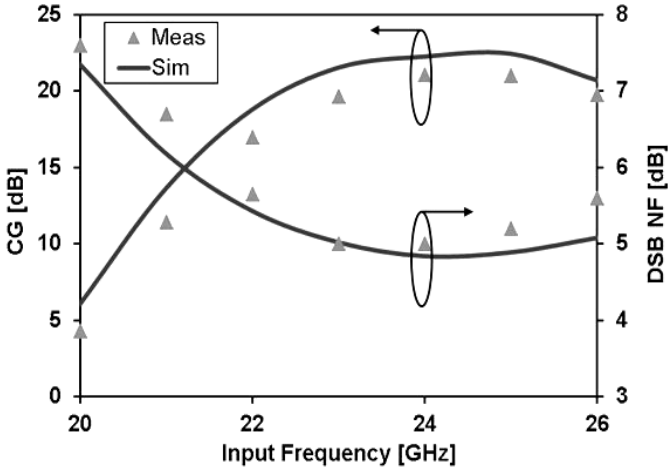


Fig. 7.4 Measured gain and NF of LNA-1 versus input frequency

According to the block diagrams shown in Fig. 7.1 and the circuit blocks, two receivers are designed and fabricated in 130 nm CMOS process. The chip micrographs are shown in Fig. 7.5. Both receivers are measured on-wafer with 1.2 V power supply. The DC power consumption (without the source followers) is only 13 mW for both receivers. Together with the source follower, RX-1 consumes 18 mW power and RX-2 consumes 20 mW power with 1.2 V power supply.

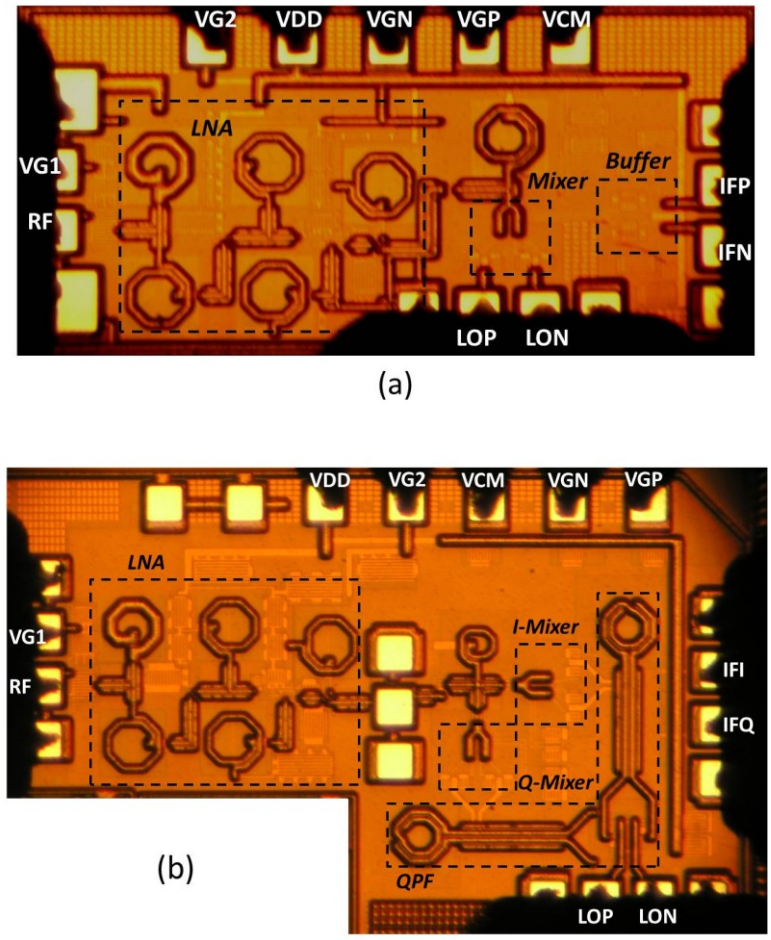


Fig. 7.5 (a) Chip micrograph of the single channel receiver RX-1; (b) Chip micrograph of the quadrature receiver RX-2

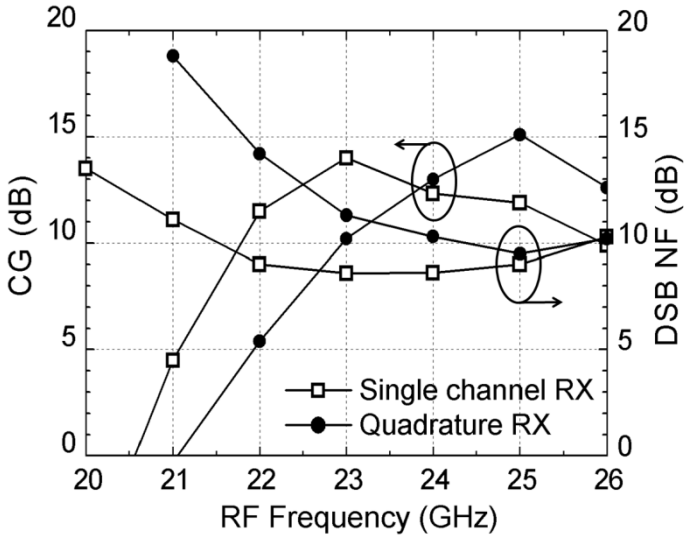


Fig. 7.6 The measured gain and NF of RX-1 and RX-2 versus RF frequency

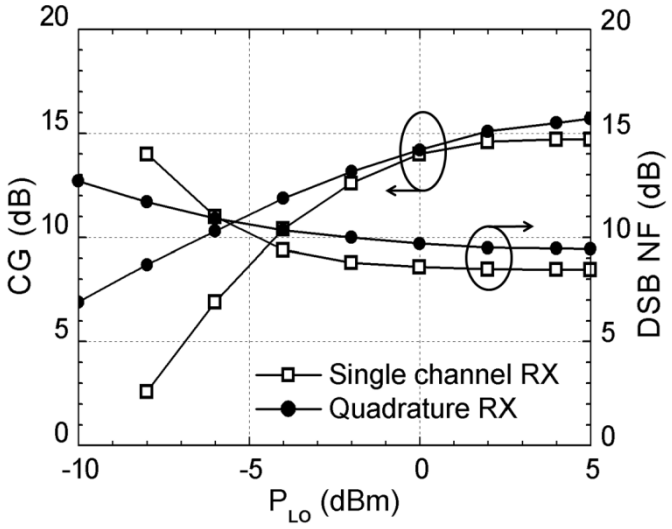


Fig. 7.7 The measured gain and NF of RX-1 and RX-2 versus LO power

The gain and noise figure versus the input RF frequency for the receivers are shown in Fig. 7.6. The IF frequency is 10 MHz and the LO power is 0 dBm. The single channel receiver shows a maximum gain of 14 dB and the lowest NF of 8.5 dB at 23 GHz, while the quadrature receiver have a maximum gain of 15 dB and the lowest NF of 9.5 dB at 25 GHz.

Fig. 7.7 shows the measured gain and NF versus LO power. The single channel receiver is measured at 23 GHz, while the quadrature receiver is measured at 25 GHz. The performance of both the receivers remain unaffected when the LO power is larger than 0 dBm.

Fig. 7.8 depicts the LO-RF and LO-IF isolation of the receivers. The isolation exceeds 25 dB for both receivers. The quadrature receiver has 10 dB higher isolation, since the deployment of QPF introduces power insertion loss, the LO power coupling is also attenuated by the QPF.

Both I-channel and Q-channel of the quadrature receiver are connected to the oscilloscope while the phase and amplitude imbalance are measured. The measured IQ phase imbalance is less than 10 degree while the IQ amplitude imbalance is less than 0.5 dB.

Both the receivers exhibited input matching values greater than 10 dB in their respective operating frequency bands: 22 - 24 GHz for the single channel and 24 – 26 GHz for the quadrature receiver.

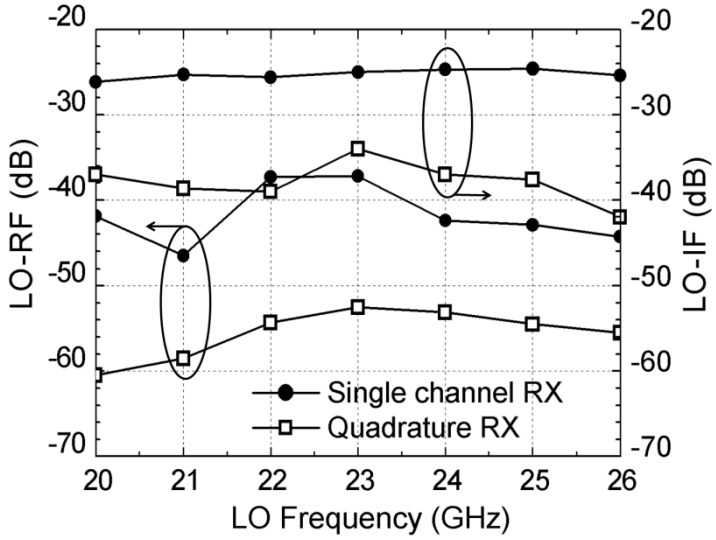


Fig. 7.8 Measured LO-RF and LO-IF isolation of RX-1 and RX-2

Table 7-2 summarizes the measured receiver performance and compares with the state-of-the-art realizations integrating similar circuit blocks in 130 nm CMOS process. From the results and comparison it can be mentioned that the realized receiver circuits achieved sufficient RF gain at a relative low LO power with a low DC power consumption. Lower LO power requirement is particularly very important since it simplifies the VCO design and also minimizes the overall DC power consumption of the transceiver. Additional gain improvement of the receivers are achievable by replacing the IF buffers with IF amplifiers at the output.

Both receivers achieve the specifications of the receivers except noise figure. The noise figure of RX-1 and RX-2 is 1.5 dB to 2.5 dB higher than the specified noise of 7 dB. This is due to the lack of good quality LO signals. If the transformer baluns are integrated with the mixer, such as in [110] or in the transceiver of Chapter 9, the noise figure of the receivers can be further reduced.

7.5 Conclusion

Two low IF K-band receivers in 130 nm CMOS are designed, fabricated, characterized and compared in this work. Through proposed quadrature polyphase filter at the mixer's LO input of the quadrature receiver, comparable performance for both the single channel and the quadrature receivers have been achieved. A comparison of the receiver performance with similar K-band realizations revealed the lower DC power consumption of the receivers achieving their optimum at lower LO signal power.

Table 7-2 K-Band Low Power CMOS Receivers

Reference	[8]	[11]	Single channel Receiver	Quadrature Receiver
CMOS Process	130 nm	130 nm	130 nm	130 nm
Integration	LNA, mixer, buffer	LNA, mixer	LNA, mixer, buffer	LNA,QPF, mixer, buffer
Freq (GHz)	24	24	23	25
Gain (dB)	3.2	2	14	15
NF (dB)	10	7.5	8.5	9.5
P_{LO} (dBm)	N/A	6	0	0
P1dB (dBm)	-12.7	-13.4	-27	-29
P_{dc} (mW)	27.2	18.3	18	20
Chip Size (mm^2)	0.59	0.37	0.63	0.84

Chapter 8
Transceiver Design

8.1 Introduction

In previous chapters, the principles of FMCW radar transceivers have been discussed. The process and components of the technology have been investigated and various building blocks have been demonstrated. Based on these results, an integrated transceiver will be presented in this chapter. This transceiver integrates all the RF components of a 24 GHz transceiver, including LNA, PA, mixer, VCO, IF amplifier, buffer amplifier, switch and frequency divider. It has four transmission channels and a receiving channel. Three operation modes, transmission mode, switch-channel receiving mode and multi-mode receiving mode are available for this transceiver. The highly integrated transceiver has achieved good performance with low power consumption.

Integrated FMCW radar transceivers and receivers at 24 GHz and higher frequencies are widely studied recently [5]-[11], [109], [113]-[118]. A fully integrated transceiver, which integrates all RF and microwave components, has a great advantage in terms of system integrity, RF signal crosstalk and transmission loss as well as the overall power consumption. As the operation frequency becomes higher, the advantage of fully integrated RF transceiver becomes more prominent. Traditionally, III-V processes as well as SiGe technologies are implemented for the transceivers operating at these frequencies [113]-[116]. However, in the recent years, CMOS technologies are also widely used because of the rapid downscale of CMOS processes and the low cost of mass production [5]-[11].

In this work, a 24 GHz low-power FMCW secondary radar transceiver targeted for wireless localization [17]-[20] is designed, fabricated and measured. The secondary radar, which enables the accurate measurement of the distance between two sensor nodes, is chosen to be used in wireless localization for their low power performance. The 130 nm CMOS

process has a cut-off frequency of 90 GHz which is suitable for radar system to operate at 24 GHz.

The transceiver includes an LO generator, a transmitter and four receiver front-ends. The receiver front-ends have two operation modes. They could operate synchronously, or they could be switched on and off one by one as a power saving mode, similar to the switch-antenna receivers in [21]. It does not require a 1P4T RF switch at the receiver input; hence the receiver noise is much lower than the switch-antenna receivers. The transceiver is highly integrated and consumes very low power, while keeps the maximum detection range and radar space resolution as high as possible.

The rest of the chapter is organized as follows. Section 8.2 discusses the system considerations of the transceiver. In section 8.3 the implemented transceiver architecture will be presented. Section 8.4 discusses the design of different building blocks. Section 8.5 discusses the integration considerations of the full transceiver chip. Section 8.6 shows the simulation and measurement results. Section 8.7 concludes the chapter.

The divider in the transceiver is designed by Ran Shu [92], the LNA is designed by Viswanathan Subramanian [110], and the other circuits are designed by me. The system level integration are performed by me.

8.2 System Considerations

For the proposed radar system, the maximum/minimum detection range, range resolution and power consumption are the most critical performances. From the system considerations in Chapter 2, If the transmitter has an output power of 6 dBm, the LO has a phase noise of -115 dBc/Hz at 30 MHz and noise figure of the receiver chain is less than 10 dBm, it is possible to realize a multi-channel secondary radar system with detection range of around 200 m and range resolution of 3 cm.

To minimize the power consumption of the transceiver, a comprehensive understanding from the transistor level to system level is required.

The VCO design used the current reusing PMOS/NMOS topology to minimize the power consumption. For amplifiers, the cascode topology is adopted. The cascode amplifiers have

high gain and provide better stability. The first stage of the LNA is optimized for noise figure, while the other two stages are optimized for low power consumption. Several buffer amplifiers are used for LO signal generation. The number of buffer amplifiers should be minimized as they consume a lot of power. By simulation, a single stage buffer amplifier can produce 6 dB gain at 24 GHz while a two stage buffer amplifier can produce 15 dB gain. The two stage buffer amplifier could produce more gain as the inter-stage matching is simplified. To ensure the amplifier to perform across different process, voltage and temperature variations, a biasing current of 2 mA is required. By implementing the complementary switch passive mixer and high impedance loading, the LO power requirement for the passive mixer is minimized; therefore the power consumption of buffer amplifiers are minimized. To improve the isolation between different channels, single transistor switches are implemented which introduce a very low signal loss around 1 dB. In the system level, different channels are switched off when they are not operating. All these considerations results in an optimized power consumption performance.

The specifications of the transceiver are already listed in Table 2-1.

8.3 Transceiver Architecture

Fig. 8.1 shows the block diagram of the designed 4-channel switchable FMCW transceiver. It includes 4 switchable receiving channels, one transmitter, VCO, buffers, a divide by 8 divider and switch and bias control circuits. The operation principle of the FMCW radar has been demonstrated in Chapter 2 and it is not discussed here.

The VCO is modulated by an external control signal and generates the FMCW signal at 24 GHz. The output signals of the VCO are amplified by two VCO buffers. One signal is converted to differential signal by a balun, and then divided by 8 through a frequency divider. The 3 GHz output signal is send to the external PLL. The other VCO buffer output is send to the power division circuit and sent to the receiver front-ends and transmitters.

The transmitter is composed by a buffer amplifier and a power amplifier. In transmission mode, the VCO signal is firstly amplified by the buffer amplifier, and then amplified by the PA. A receiver is composed by a LNA, an IF amplifier, a mixer and a transformer balun. Through the switching and biasing control, two receiving modes are available. The switch

channel receiving mode switches the receivers on and off one by one, while in the multi channel receiving mode, all the receiver channels are turned on at the same time. The received RF signal is amplified by the LNA, then mixed with the LO signal in the mixer to generate the IF signal. The IF signal is then amplified by the IF amplifier. The LO signal is amplified by the buffer amplifier and converted to differential to drive the mixer.

The biasing circuit of the TX channel and RX channels are switchable and controlled by a bias control circuit. The LO input of these channels are also controlled by RF switches to avoid the loss of LO signal.

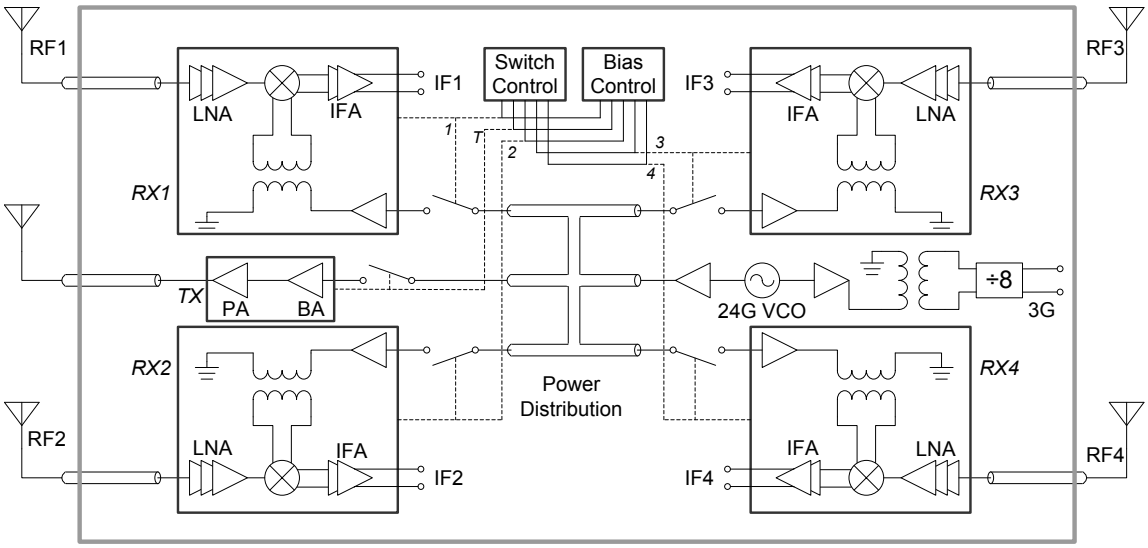


Fig. 8.1 Four channel transceiver block-diagram

8.4 Circuit Blocks

The LNA implemented in the four channel transceiver is LNA-1. The mixers integrated with balun implemented in the receivers are MIXER-2, although the IF amplifiers have been re-designed. In this section the design of other circuits implemented in this transceiver is presented.

8.4.1 Voltage Controlled Oscillator (VCO)

Fig. 8.2 shows the simplified schematic of the designed VCO. PMOS/NMOS cross coupled topology is implemented. As the biasing current is reused to generate the negative resistance in the VCO core, the current consumption could be reduced. The VCO operates both in the transmission mode and receiving mode, therefore the biasing circuit is not designed. The NMOS transistors have widths of 20*2 μm, while the PMOS transistors have widths of 20*4.25 μm. A one-turn 150 pH inductor is designed with patterned ground shielding for the resonance tank. NMOS varactors with minimum length are used as the tuning varactor. Short varactor length reduced the varactor contribution to the phase noise. The control voltage Vc is connected to the center of the symmetrically connected varactors.

Two cascode VCO buffers are implemented to amplify the VCO output and to isolate the VCO core from the loading circuits. Compared with the widely used common-drain buffers, the cascode topology provides much better isolation and better gain. The isolation is very important as at 24 GHz the components are very sensitive, especially for the VCO core. The impedance of the loading circuits varies as the transceiver switches between transmitting mode and receiving mode. Hence, if the isolation is not optimized, the VCO output frequency would be pulled by the load impedances. The cascode topology provides approximately 30 dB isolation by simulation. The transconductance transistors are set to 20*2 μm, while the cascode transistors are set to 20*6 μm. The LO output are matched to 50 Ω using an L-C matching network.

The VCO layout is carefully performed to reduce the parasitic components. The VCO core is minimized, and the VCO buffer input is placed very close to the VCO core. The VCO core and the buffers are electromagnetically modeled to get the accurate circuit performance. By simulation it consumes 11 mW power with 1.2 V biasing voltage. It operates at 24 GHz with 10% of tuning range. The phase noise is 90 dBc/Hz at 1 MHz. The output power at the buffer output is -5 dBm.

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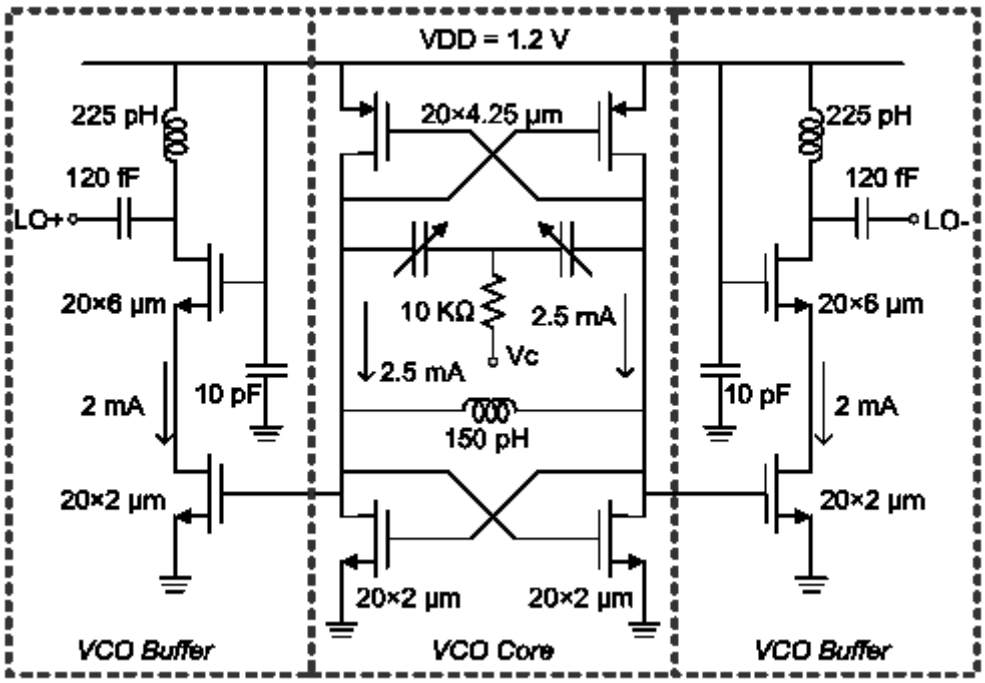

Fig. 8.2 VCO schematic

8.4.2 Power Amplifier (PA)

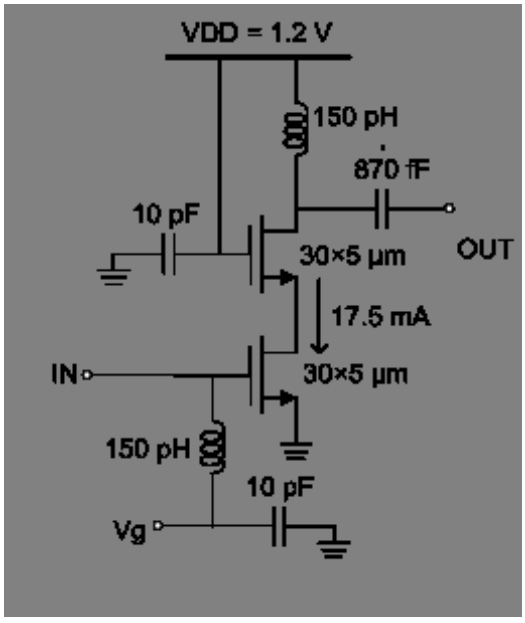

Fig. 8.3 PA schematic

Fig. 8.3 shows the schematic of the designed class AB power amplifier. The required output power is 6 dBm. Low PA output power has two advantages; firstly, the designed PA does not need to consume much power, therefore the power consumption could be minimized. Secondly, PA leakage to the VCO is limited and VCO performance will not be influenced by the PA.

The implemented PA has a cascode topology for higher gain and isolation. The transistor sizes are 30*5 μm. The current flowing through the PA is 17.5 mA by simulation. The current density is 120 μA/μm; this current density allows the PA to operate with maximum efficiency. A 150 pH inductor is used to match the input. 50 Ω Output matching is realized by an 870fF series capacitor and a 150pH shunt inductor.

8.4.3 Buffer Amplifier (BA)

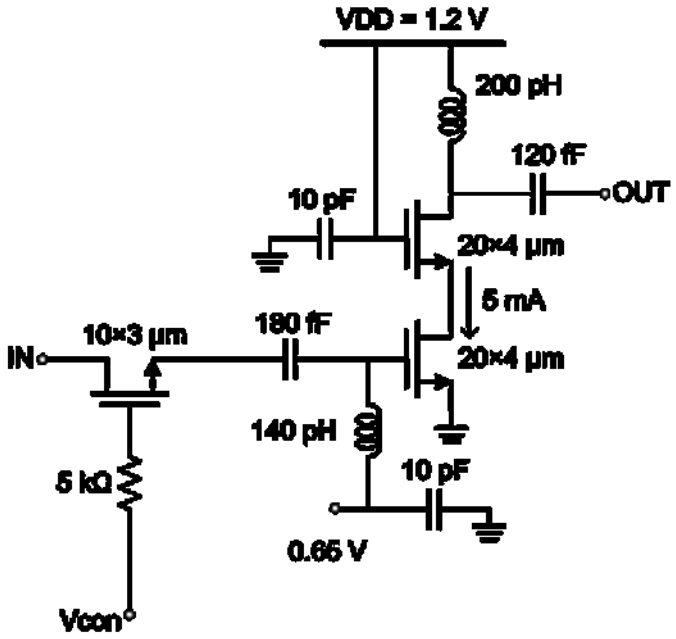

Fig. 8.4 BA schematic

Shown in Fig. 8.4, buffer amplifiers are implemented in the LO signal path to amplify the signal and block it if required. As the transceiver is switched between different transmit and receive modes, a RF transistor is implemented as a switch to improve the LO signal transmission to the operating receivers or transmitter. The buffer amplifier can compensate

the signal loss in the interconnections and the switch, it amplifies the LO signals to a certain level which drive the PA or mixers.

The switch is realized using a 10*3 μm series NMOS transistor. By simulation it provides 15 dB isolation and has 1.1 dB insertion loss at 24 GHz. A 5 kΩ resistor is connected at the transistor gate to block the RF signal.

The buffer amplifier is similar to the first stage of the LNA. 20*4 μm transistors are used. The input matching is realized by a 180 fF capacitor and a 140 pH inductor. The output matching is realized by a 120 fF capacitor and a 200 pH inductor. 10 pF blocking capacitors are used to provide the capacitance between the RF ground and DC ground.

8.4.4 IF Amplifier (IFA)

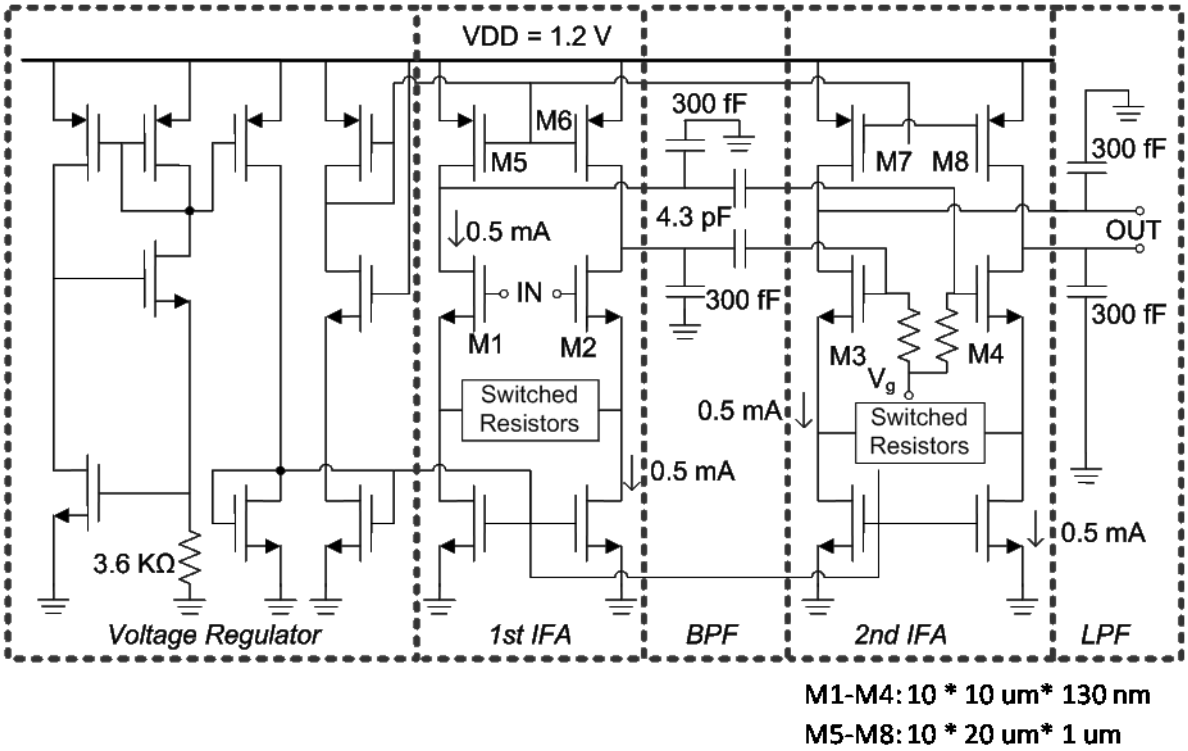

Fig. 8.5 IFA schematic

Fig. 8.5 shows the schematic of the IF amplifier. It is a two stage differential common source amplifier. Two 4.3 pF capacitors are used to decouple the DC of the two amplifiers.

Together with two 300 fF shunt capacitors, a bandpass filter between 1 MHz to 30 MHz is formed. Switched resistors are implemented to control the gain of the amplifiers. The output of the second amplifier is also connected with two 300 fF shunt capacitors to filt the high frequency signals.

The amplifier source transistors are biased by a voltage regulator. Replica biasing circuit is used to accurately bias the circuit. The transconductance transistor of the first stage amplifier is biased from the mixer common mode voltage. The second stage is biased by an external biasing Vg.

By simulation, the IF amplifier provides 0 to 40 dB voltage gain with 3dB bandwidth between 500 kHz to 30 MHz. The amplifier consumes 2.5 mW DC power with 1.2 V DC voltage. The input P1dB is -15 dBm if the IF amplifier gain is set to 0 dB.

8.5 Integration Considerations

The bias circuits of most circuits are designed switchable for power management considerations. The biasing of the TX block and 4 RX blocks are controllable in different operation modes. In transmission mode, the TX is switched on and the RXs are switched off. The power consumption is 55 mW by simulation. In switch channel receiving mode, one RX channel is switched on and the others are switched off. The power consumption is 48 mW by simulation. In multi-channel receiving mode, all four RX channels are switched on and the TX channel is switched off. The power consumption is 124 mW, respectively. Large low-voltage transistors are used in the biasing circuits to reduce the voltage drop from the DC biasing to the biasing of the circuit blocks.

The major considerations in the circuit integration are highly compact, low loss and low channel crosstalk. The layout of the 4-channel transceiver is shown in Fig. 8.6. The four receivers, the transmitter, VCO and divider are integrated into a small chip area of 2.2 mm*1.7 mm.

50 Ω transmission lines are used for interconnection. Side-shielded microstrip topology is chosen for minimizing the leakage of the RF signal to substrate and to adjacent components. The transmission lines are set as short as possible to reduce the signal loss. Bends and

T-Junctions are avoided as they introduce much loss at 24 GHz. The most sensitive circuit is the power division circuits which divides the LO signal into the buffer amplifiers. The length of the transmission lines which connects the RX and VCO are set identical to avoid the phase/magnitude mismatch. The distances between different branches of the power division circuit are set as 100 μm to avoid the crosstalk.

Various inductors are utilized in the circuit. They are very crucial for the amplifiers as without them, the 130 nm transistors are not able to provide sufficient gain at 24 GHz. The external dimensions of the inductors are around 100 μm. The distance between different inductors are large than 100 μm. Critical circuit blocks, such as amplifier transistor cores are also placed as far as possible from the inductors. The distance between the inductor and the interconnections are also minimized.

Large MIM blocking capacitors are implemented to connect the RF ground and DC ground. The DC signals close to the DC pads are also AC coupled with ground to remove the influence from the external DC biasing.

To further suppress the coupling between different channels, guard rings are placed on the edge of different circuit blocks. These guard rings include the metal lines and vias from top metal to bottom metal and to substrate. These guard rings provide sufficient isolation between different channels.

The 4 RX channels are placed symmetrical to avoid the performance mismatch. The RF inputs are GSG pads with 100 μm pitch distance. The TX output is also GSG pads with 100 μm pitch distance. These pads could be connected with external filters through bond-wires to build a 2*2 receive antenna array and a transmit antenna. The DC biasing are DC pads with 150 μm pitch distance and the IF pads are GSSG pads with 100 μm pitch distance. From these pad designs on chip measurement could be easily carried out.

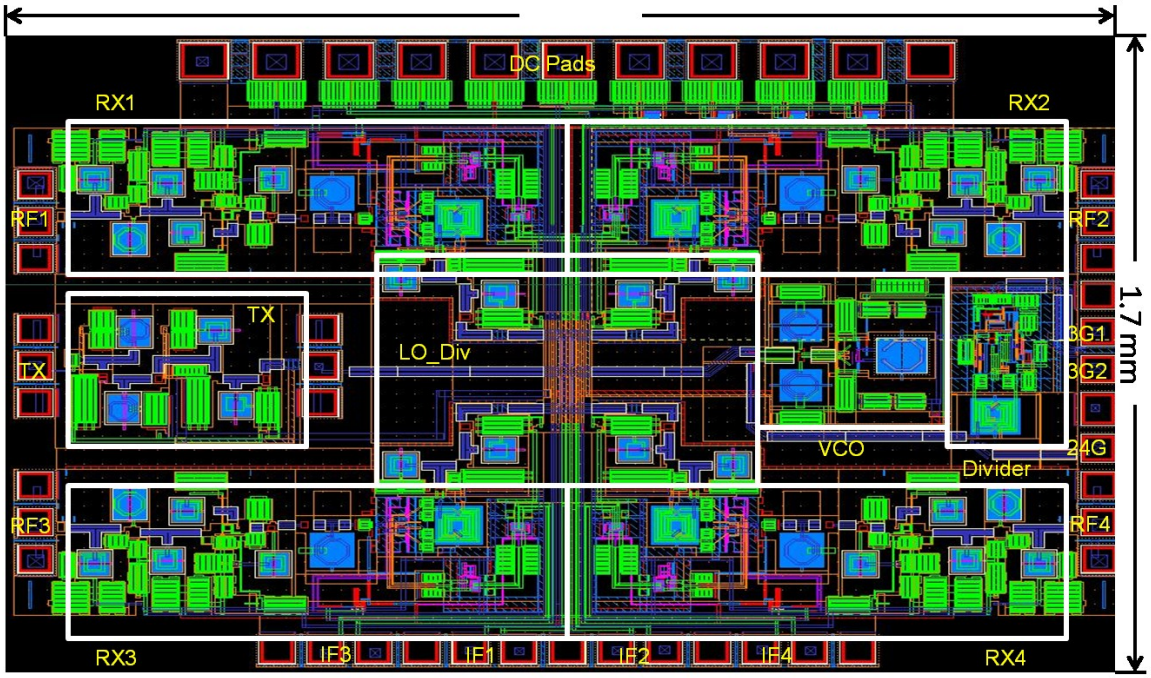

Fig. 8.6 Layout of the 4-channel transceiver

8.6 Simulations and Measurements

Before the fabrication of the complete transceiver, the VCO is designed and characterized independently as it is sensitive with PVT variation and parasitic components. The successful realization of VCO would lead to the successful of the whole transceiver. The spectrum and phase noise of the VCO is characterized through the spectrum analyzer. The measured VCO has an output power of -5.85 dBm with an operation frequency at 24.03 GHz. The tuning voltage is at 0.4 V. When the tuning voltage is changed between 0 V and 1.2 V, the output frequency varies by 1.0 GHz. The phase noise of the VCO is -90 dBc/Hz at 1 MHz. After the characterization, the varactors banks are slightly modified. The phase noise performance is improved and the tuning range is broadened as well.

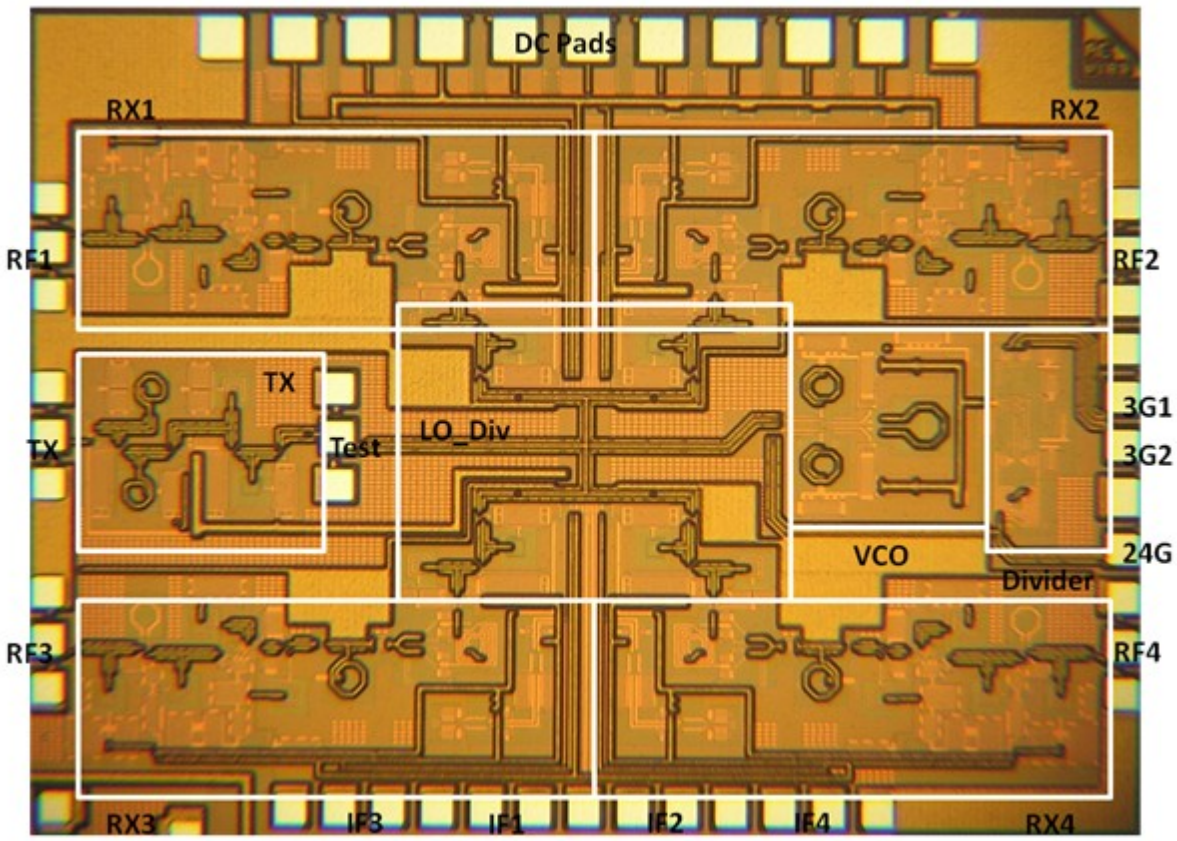

Fig. 8.7 Chip micrograph of the 4-channel transceiver

Fig. 8.7 shows the chip micrograph of the designed transceiver. The integrated transceiver is characterized in 3 different modes: transmission mode, switch-channel receiving mode and multi-channel receiving mode. In the transmission mode, only the transmitter is turned on. The simulated and measured transmitter power and frequency is shown in Fig. 8.8. As the coarse tuning voltage switches from 0 V to 1.5 V, the output power ranges from 4 dBm to 5.5 dBm, which is relatively constant. The frequency tuning range is from 23.5 GHz to 25.4 GHz. If the tuning voltage is from 0.4 V to 1 V, the Kvco is linear and the frequency ranges from 24 GHz to 25.2 GHz. The power consumption is 75 mW with 1.5 V V_{dd}. The transmitter could efficiently cover the 24 GHz operation band.

Fig. 8.9 shows the receiver gain versus RF power in different modes. The RF frequency is 24 GHz and IF is at 50 MHz. In the switch-channel receiving mode, the receiving channels are switched on and off one by one. The gain is 31 dB, input P1dB is -33 dBm and NF is 6 dB by measurement. The power consumption is 65 mW with 1.5 V biasing voltage. In multi-channel receiving mode, the transmitter is turned off and all four receiver channels are

turned on at the same time. The measurements show a gain of 21 dB, input P1dB of -37 dBm and NF of 9 dB. The power consumption is 133 mW with 1.5 V biasing voltage.

The transceiver performance is concluded in Table 8-1. The designed multi-mode transceiver frontend has achieved very low power consumption and very high integration with state-of-the-art performance.

The transceiver achieves the specifications in Table 2-1. Therefore it would be suitable in wireless localization systems. It is worth to mention that a wireless localization system utilizing another transceiver based on the circuit blocks described in this chapter have been developed and shows good localization accuracy. [106]

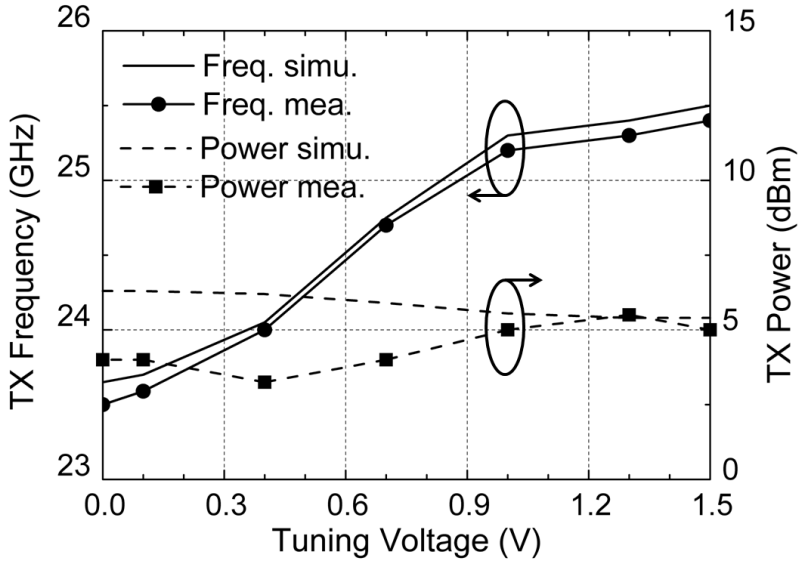

Fig. 8.8 TX output power and frequency versus tuning voltage

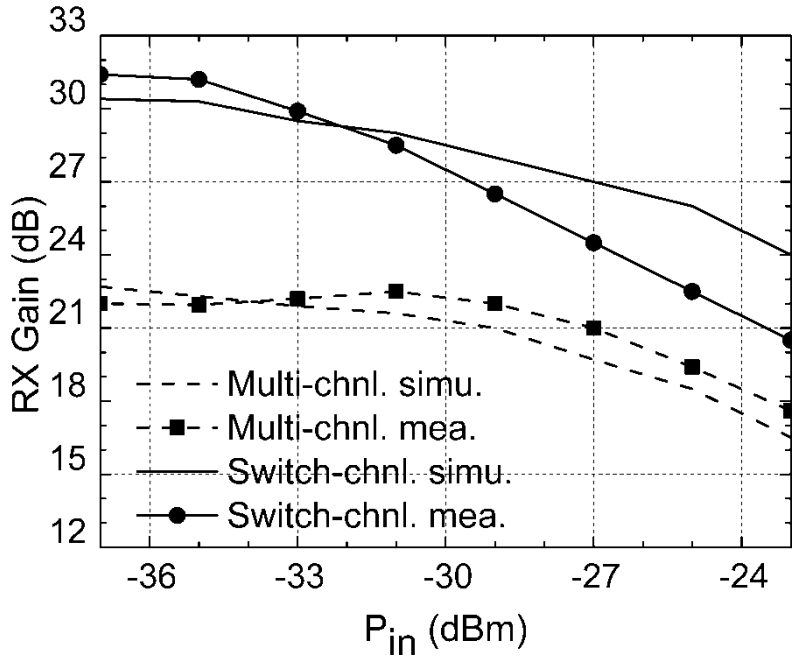

Fig. 8.9 RX gain versus RF input power in different modes

8.7 Conclusion

Based on the previous work, a multi-mode 24 GHz transceiver is designed, integrated and fabricated. The transceiver frontend has four receiver channels and 1 transmit channel. Focusing on low-power-consumption and small chip area, the transceiver integrated four receiver channels and a transmitter channel in 2.2 mm*1.7 mm chip area. The designs of different building blocks, including LNA, mixer, VCO, PA, BA and IFA, are discussed and presented. The integration technique and considerations is discussed. Then the LNA and VCO are fabricated and measured as a single chip. The measurement results match the simulation results. The simulation of the final chip is shown in the last part of the chapter. The designed transceiver frontend achieves low power consumption and high integration with good gain and noise figure performance. It is demonstrated to be a proper choice to be integrated into the 24 GHz FMCW radar systems.

Table 8-1 Transceiver Performance Comparison

Ref.	Process	Intergration	DC Power (mW)	Chip Area (mm^2)	RX Gain (dB)	RX NF (dB)	RX P1dB (dBm)	Phase Noise (dBc/Hz)	TX Pout (dBm)
[9]	0.18 µm CMOS	RX+VCO+ FD	108	2.1	28.4	6	-23.2	-110	-5
[10]	65 nm CMOS	RX+VCO+ FD	78	2.1	31.5	6.7	-24	-110	N/A
[24]	0.13 µm CMOS	RX+VCO+ FD	88	0.8	12	5.5	-16.2	-101	-3
[116]	0.18 µm BiCMOS	TX+RX+P LL	510	7.4	35	4.5	-33.2	-114	14.5
[117]	0.13 µm CMOS	4TX+4RX +PLL	TX mode: 980 RX mode: 520	5.1	32	6	N/A	-97	12.9
[119]	0.18 µm BiCMOS	TX+2RX+ PLL+Digit al	275	NA	18	10	-15	-82	7
This Work	0.13 µm CMOS	TX+4RX+ VCO+FD	TX mode : 75 RX mode : 65	3.7	31	6	-33	-90	4

- Phase noises are measured at 1 MHz.

Chapter 9
Summary and Conclusion

In this thesis, low power CMOS circuit blocks for 24 GHz FMCW radar transceivers are presented. Various issues regarding the design methodology, from the high frequency active and passive component models to transceiver system topologies are discussed and examined. Three types of different circuit blocks, K-Band low-loss passive mixer, K-Band baluns and ultra-broadband switches, are designed, fabricated and characterized.

System level consideration for the FMCW radar transceivers are discussed in this thesis. The basics of wireless sensor networks, wireless localization and FMCW radar are presented firstly. Then the system requirements of the FMCW radar and secondary FMCW radar are analyzed. Different topologies for the receivers and transceivers are shown and compared with each other in this application. Homodyne receiver and single-antenna transceiver are chosen for the final integration.

CMOS circuit design at 24 GHz requires decent understanding of the passive and active components. After reviewing the CMOS process and the MOSFET transistor characteristics, the lumped element models, the compact models, and their implementations in the circuit design are studied. BSIM model shows accuracy for power-consuming transistors, while PSP model is more suitable for the cases that the drain-source voltage equals to 0. Based on EM simulations and on-wafer measurements, various passive components are investigated. It is found that skin effects and substrate eddy currents play crucial rules for CMOS circuits at 24GHz. An accurate and efficient circuit design methodology is established from these studies. Three types of on-chip baluns, active balun, L-C balun and transformer balun, are designed, fabricated and measured. It is found that the active balun is a suitable choice when the balun requires a high gain, while the transformer balun is the right choice when the balun needs to be broadband and miniature. An impedance-tuning method is introduced to simplify the balun integration with other circuits.

K-Band direct conversion passive mixers are designed in a standard 130 nm CMOS technology. The designed mixers achieve low insertion loss and low LO power requirement while maintaining high linearity and good isolation. Reliable integration techniques with polyphase filters and baluns are developed. Double balanced mixers are compared with single balanced mixer in details, while the single balanced mixer shown comparable isolation and high gain for direct conversion receivers.

Regular and floating-bulk TX/RX switches are designed, fabricated and measured. Compared to the regular switches, floating bulk switches provides lower IL and higher linearity, but suffers from poor isolation. The performance of the floating bulk switch is boosted by the improved biasing circuit. The designed switches achieved lower IL, higher isolation together with wide band in a relative small chip area.

Two K-band low-IF receivers, a single channel receiver and a quadrature receiver, are designed and fabricated in a 130 nm CMOS process. It is demonstrated that, with the proposed polyphase filter, the quadrature receiver is able to achieve similar performance as the single channel receiver in various aspects while maintaining the advantages of quadrature scheme. The measured performances compare the state-of-the-art 130 nm CMOS realizations in this band.

An integrated low power transceiver is designed based on the above works. The transceiver has one transmission path and four receiving paths. The implemented circuit blocks are described in detail. With careful power management and integration, the designed transceiver has excellent performance and ultra-low-power consumption both at transmission mode and at receiving mode.

The precise localization techniques in wireless sensor networks are very attractive for various industry and commercial applications. As the wireless sensor networks start to expand recently, the low-cost low-power CMOS localization chip-sets will become interesting to be implemented in these systems. The further work would be prototype design for the localization system utilizing the integrated circuits described in this thesis, while the first applications would be home automation and industrial networks.

List of Publications

[1] **T. Zhang**, A. Hamidian, R. Shu, and G. Boeck, "24 GHz low-power switch-channel CMOS transceiver for wireless localization", accepted by *International Journal of Microwave and Wireless Technologies*.

[2] **T. Zhang**, and V. Subramanian, "Design and integration of compact K-band baluns using impedance tuning approach", Progress In Electromagnetics Research C, vol. 27, pp. 1-13, 2012.

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