Interface investigations of passivating oxides and functional materials on crystalline silicon

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Abstract

The unique property of AlO_x, that it exhibits negative fixed charges, is very attractive for back-side passivated p-type silicon solar cells as well as for high efficiency solar cells featuring highly doped (p^+) regions. However, for a successful integration of AlO_x and AlO_x/SiN_x based systems in different types of high efficiency solar cells, a thorough understanding of the passivation properties and the origin of the negative charge of these materials is necessary.

Theoretical studies suggest that another promising approach to increase silicon-based solar cell efficiency, is to embed plasmonic metal nanoparticles (NPs) in a passivating, anti-reflective oxide for light trapping enhancement. However, not only the optical, but also optoelectronic effects of the metal NPs need to be considered.

In the present study interfaces of passivating oxides and functional materials on crystalline silicon (c-Si) as well as their electrical, optical and optoelectronic properties are investigated. A variety of material systems, including PECVD-deposited AlO_x-single layers and AlO_x/SiN_x stacks on p-type c-Si wafer, as well as TiO_2 in situ doped by Au NPs (TiO_2:AuNPs) deposited by spin coating on c-Si, are subject to these investigations.

For this purpose a high frequency capacitance voltage (C-V) method is refined, enabling a reliable determination of the spectroscopically resolved interface defect state densities over the entire c-Si band gap as well as of the oxide charge densities. C-V investigations in conjunction with lifetime measurements allow a detailed evaluation of the passivation properties in particular of the AlO_x-single layers and AlO_x/SiN_x stacks on c-Si.

In the first part of this work, AlO_x/SiN_x stacks on c-Si are investigated in the as deposited state, after an annealing step and after a firing step. The effects of different c-Si surface wet-chemical treatments, in particular of a wet-chemical oxidation, on the passivation properties are are studied as well as the stability and origin of the negative charge. The investigations of c-Si/(wet-chemical)$SiO_x/AlO_x/SiN_x$ stacks demonstrate that the implemented wet-chemical SiO_x interlayer affects both, the chemical as well as the field-effect passivation. The defect state density is considerably reduced. However, additional traps, most probably in the vicinity of the (wet-chemical)SiO_x/AlO_x interface, are introduced as well, leading to inhomogeneities and instabilities of the negative charge. It is found that the annealing process leads to the formation of negative fixed charges with a stable charge density. The firing process leads to negative charging of traps. In the latter case, however, the initial charge density is unstable and is reduced upon moderate biasing due to electron detrapping. Both thermal treatments lead to an enhancement of the field-effect passivation. The initial high negative charge can be reversibly reduced and inverted by a negative constant voltage stress (V_{stress}). This is caused by electron detrapping and positive charging of traps in the AlO_x/SiN_x stacks.

It is concluded that in addition to the fixed negative charges, trapping of negative charges

near the interface is a crucial mechanism contributing to the field-effect passivation. It is also found that a large V_{stress} leads to a voltage stress induced generation of additional intrinsic Si dangling and strained bond defects at the c-Si/SiO$_x$ interface. Both V_{stress} induced effects are possibly linked to so called potential induced degradation (PID) effects, which have a detrimental influence on photovoltaic module performance.

In the second part of this work, photoconductivity and optical measurements demonstrate that an introduction of 40-50 nm diameter Au NPs into the antireflective TiO$_2$ layer (TiO$_2$:AuNPs) deteriorates the antireflection properties. This is observed as a decrease of the external quantum efficiency of photogeneration of charge carriers. In addition, a decrease of the internal quantum efficiency due to a deterioration of the chemical passivation is found. C-V measurements indicate that this is due to additional defect states at the TiO$_2$:AuNPs/Si interface, caused by Au NPs in contact with the underlying c-Si, enhancing photogenerated charge carrier recombination. It is concluded that TiO$_2$:AuNPs layers with larger (>100 nm) Au NPs could potentially be applied on the passivated rear, but not on the front side of Si solar cells.

Zusammenfassung

Die einzigartige Eigenschaft von AlO_x, dass es negative Festladungen aufweist, ist für die Rückseiten-passivierte p-Typ Silizium-Solarzellen als auch für hocheffiziente Solarzellen mit hochdotierten (p^+)-Regionen sehr attraktiv. Für eine erfolgreiche Integration von AlO_x und AlO_x/SiN_x- basierten Systemen in verschiedenen Arten von hocheffizienten Solarzellen ist jedoch ein gründliches Verständnis der Passivierungseigenschaften und des Ursprung der negativen Ladung dieser Materialien erforderlich.

Theoretische Studien schlagen den Einsatz von plasmonischen Metall-Nanopartikel (NP) in einem passivierenden, anti-reflektierenden Oxid vor, um durch erhöhten Lichteinfang die Effizienz von Silizium-basierten Solarzellen zu verbessern. Doch nicht nur die optischen, sondern auch optoelektronischen Effekte der Metall NPs sind zu berücksichtigen.

In der vorliegenden Arbeit werden die Grenzflächen passivierender Oxide und funktioneller Materialien auf kristallines Silizium (c-Si) untersucht. Das Hauptaugenmerk liegt auf ihren Einfluss auf die elektrischen, optischen und optoelektronischen Eigenschaften des c-Si/Oxid Systems. Eine Vielzahl von Materialsystemen, einschließlich PECVD-abgeschiedene AlO_x -Einzelschichten und AlO_x/SiN_x Stapelschichten auf p-Typ c-Si Wafer, sowie TiO_2 mit eingebetteten Gold-Nanopartikeln (TiO_2:AuNP) durch Spin-Coating auf c-Si deponiert, unterliegen diesen Untersuchungen.

Als Grundpfeiler für diese Untersuchungen wurde im Rahmen der Arbeit eine Hochfrequenz Kapazität-Spannungs- (C-V) Methode weiterentwickelt, die eine zuverlässige Bestimmung der spektroskopisch aufgelösten Grenzflächendefekt-Zustandsdichten über die gesamte c-Si Bandlücke sowie der Oxid-Ladungsdichten ermöglicht. C-V Untersuchungen in Verbindung mit Lebensdauermessungen erlauben eine detaillierte Auswertung der Passivierungseigenschaften der AlO_x-Einzelschichten und AlO_x/SiN_x Stapelschichten auf c-Si. Diese Proben werden in abgeschiedenem Zustand, nach einem Temperschritt und nach einem Feuerschritt untersucht. Der Einfluss von verschiedenen nasschemischen Vorbehandlungen der c-Si-Oberfläche, insbesondere der einer nasschemischen Oxidation, auf die Passivierungseigenschaften sowie der Ursprung und die Stabilität der negativen Ladung werden untersucht.

Im ersten Teil der Arbeit zeigen Untersuchungen des $c-Si/SiO_x/AlO_x/SiN_x$ Schichtstapels, dass eine nasschemisch erzeugte SiO_x-Zwischenschicht sowohl die chemische als auch die Feldeffekt-Passivierung beeinflusst. Die Defektzustandsdichte an der Si/SiO_x Grenzfläche ist erheblich reduziert. Es werden jedoch zusätzliche Zustände vermutlich nahe der SiO_x/AlO_x Grenzfläche generiert, die zu Inhomogenitäten und Instabilitäten der negativen Ladung führen. Es wird festgestellt, dass das Tempern zur Aktivierung der negativen Festladungen führt, wobei der Feuerschritt zur negativen Beladung der Zustände führt. Beide Wärmebehandlungen führen zu einer Verbesserung der Feldeffekt-Passivierung. Weiter wird gezeigt,

dass die anfänglich hohe negative Ladung durch eine negative konstante Stressspannung (V_{stress}) reversibel reduziert und invertiert werden kann. Dies wird verursacht durch die Freisetzung der gefangenen Elektronen und durch die positive Aufladung der Zustände in der AlO_x/SiN_x Stapelschicht. Es wird gefolgert, dass zusätzlich zu den festen negativen Ladungen, das Einfangen von negativen Ladungen in der Nähe der Grenzfläche entscheidend zur Feldeffekt-Passivierung beiträgt. Es stellt sich heraus, dass eine große Stressspannung zu einer spannungsinduzierten Generation von zusätzlichen intrinsischen Si-Defektzuständen an der c-Si/SiO_x Grenzfläche führt. Beide Spannungsstress-induzierte Effekte könnten möglicherweise mit sogenannten Potential-induzierten Degradations- (PID) Effekten zusammenhängen, die einen nachteiligen Einfluss auf die Leistung von Photovoltaik-Modulen haben.

Im zweiten Teil dieser Arbeit zeigen Photoleitfähigkeits- und optische Messungen, dass die Einbettung von 40-50 nm großen Gold-Nanopartikeln in die Antireflex-TiO_2-Schicht (TiO_2:AuNPs) die Antireflexeigenschaften verschlechtert. Dies führt zu einer Verringerung der externen Quanteneffizienz. Zusätzlich wird eine Verringerung der internen Quanteneffizienz aufgrund einer Verschlechterung der chemischen Passivierung beobachtet. C-V-Messungen zeigen, dass dies an der Erhöhten Rekombination durch zusätzliche Defektzustände an der TiO_2:AuNPs/Si-Grenzfläche liegt, die durch den Kontakt von Gold-Nanopartikel mit dem darunter liegenden c-Si entstehen. Daraus wird gefolgert, dass die TiO_2:AuNP-Schichten mit größeren Au NP (> 100 nm) eher auf die Rückseite, aber nicht auf die Vorderseite der Si-Solarzellen, aufgebracht werden sollten.

Contents

1 Introduction

1.1 General introduction

The rapidly increasing man-made climate changes as well as the increasing global energy demand accompanied by the diminishing stock of fossil fuels have underlined the urgency for mankind to find alternative energy sources. Photovoltaics (PV) offers such an alternative as a renewable energy source. Since the 1950s silicon (Si) has been the most widely used material for the realization of photovoltaic systems and modules because of its easy availability and environmental friendliness. At the moment, about 85 % of the solar cells currently produced are based on crystalline silicon (c-Si) wafers. The energy conversion efficiencies of these industrially manufactured cells are typically $\eta = 16$ % – 18 %, whereas laboratory-type Si solar cells hold the record of $\eta = 25.0$ % [Zha99, Gre09, Gre13]. The latter is already fairly close to the theoretical maximum of $\eta = 29$ % [Tie84, Gre84, Ker03], which is given by the Shockley-Queisser-Limit [Sho61]. The efficiency of solar cells is significantly reduced by electronic recombination losses at the wafer surfaces [Din12b]. This primarily leads to a suboptimal open-circuit voltage. Through surface passivation a reduction in surface recombination can be achieved. However, at present, many of the low-cost industrial solar cells have no efficient passivation schemes implemented, which explains a significant part of the power conversion efficiency gap between industrial and high-efficiency laboratory solar cells. So far, a variety of materials and material stacks have been investigated for surface passivation purposes of the cell's front and rear side [Abe00]. Many aspects need to be taken into consideration regarding the suitability of a passivation scheme. These are the doping type and resistivity of the Si, thermal-, UV-, and long-term stability, the optical properties (i.e., parasitic absorption, refractive index), and the processing requirements (e.g., surface cleaning, available synthesis methods). Traditionally, thermally grown SiO_2 has been used as an effective passivation scheme in high-efficiency laboratory cells, including the record passivated emitter rear locally diffused (PERL) cell [Zha99, Gre09]. Nowadays, most laboratory and industrial c-Si solar cell schemes use SiN_x synthesized by PECVD. SiN_x serves as an antireflective coating (ARC) and also as passivation layer. Another widely investigated passivation material is hydrogenated amorphous Si (a-Si:H). The combination of intrinsic and doped a-Si:H nanolayers (< 10 nm) has been successfully applied in commercial heterojunction Si solar cells [Tsu09, Min11, dN11, Bae11].

1.2 Aluminum oxide for passivation in Si solar cells

In recent years, Aluminum oxide (Al_2O_3 or AlO_x) has emerged as an alternative passivation material [Din12b]. First reports on the passivation properties of AlO_x go back to 1989 by Hezel and Jaeger [Hez89], though initially demonstrating a low quality of passivation. After recent advancements in deposition techniques, in particular atomic layer deposition (ALD), [Hoe06, Ago06] AlO_x was reintroduced. A high level of passivation was achieved, as good as obtained by thermally grown SiO_2[Hoe06, Hoe08a]. Unlike other investigated materials, this high level of passivation of AlO_x was assigned to the field-effect passivation induced by negative fixed charges [Hoe08a], which is a unique property of this material. This distinguishing property of AlO_x made it highly interesting as a passivation material because it offered a new opportunity for the PV industry: Due to inversion layer shunting, SiN_x was not a suitable candidate as a passivation layer for the p-type Si cell rear side. Therefore, AlO_x became a promising candidate to improve the rear side of conventional screen-printed p-type Si solar cells by replacing the Al-back surface field (Al-BSF) [Din12b]. The latter leads to lower surface recombination losses, better internal reflection, and reduced wafer bow for thin wafers. A passivated rear side is essential for reaching higher efficiencies and the use of thinner Si wafers. Thus, the focus shifted to AlO_x-single layers and AlO_x/SiN_x stacks as a solution for the p-type Si rear side. In addition, for n-type Si solar cells a suitable passivation solution of the p^+ emitter was required. The negative charges of AlO_x are an ideal match for the passivation of such emitters. To date, the application of AlO_x on p^+ emitters and on the p-type Si rear has resulted in enhanced solar cell efficiencies up to 23.9% [Ben08, Glu10]. In addition to ALD, other deposition techniques, such as atmospheric pressure chemical vapor deposition [Bla12], reactive sputtering [Zha13] and plasma-enhanced chemical vapor deposition (PECVD) [SC09, Laa12], have already demonstrated to produce AlO_x with excellent passivation properties. The PECVD process is a serious contender for the deposition of AlO_x in the photovoltaic industry due to its compatibility with already available inline processes and high throughput. Of particular interest for Si solar cell applications are thin passivating AlO_x films covered by amorphous SiN_x capping layers synthesized by PECVD. Among other benefits, this capping layer leads to an improved chemical stability. Such AlO_x/SiN_x passivation stacks have been applied at the rear and front side of Si solar cells [Gat11, SC10] reaching efficiencies above 20% [Sch12].

However, to insure further development and a successful integration of PECVD-deposited AlO_x and AlO_x/SiN_x based systems in different types of high efficiency solar cells, a thorough understanding of the physical, structural and electronic properties of this material is necessary. A major issue is related to the formation of an interfacial SiO_x- layer that is usually observed during deposition of AlO_x on Si independently of the deposition method [Cho02, Gus00]. The quality of this interfacial layer strongly impacts the Si/AlO_x interface passivation properties [Din11b, Nau12, Laa12]. Thus, an understanding and control of the formation of the interface and its electrical activity upon interaction with external

processes such as thermal steps, illumination or biasing is one concern. A second major issue is related to the origin of the negative charge in this material. The knowledge of this origin could open the way to better control of the material properties in view of tuning the passivation mechanism, particularly to beneficially adapt the field-effect based on the negative charge to different high efficiency solar cell concepts.

1.3 Gold nanoparticles integrated in oxide for plasmonic effects

Light trapping enhancement by plasmonic-active metal antiparticles (NPs) is believed to be a promising approach to increase silicon-based solar cell efficiency. In recent years, extensive studies have been undertaken to investigate the use of metallic nanostructures, which support localized surface plasmons, for achieving enhanced light absorption in Si-based solar cells (see [Atw10] and references therein). Among such metal nanostructures, gold (Au) and silver (Ag) NPs are the most interesting materials. This is based on theoretical calculations which suggest that improved light trapping in silicon covered with metal NPs is due to the preferential light scattering by the NPs into silicon. This property of metal NPs deposited on the front surface of Si-based solar cells is often termed the "plasmonic effect" of metal NPs resulting in an increase of light absorption in the underlying Si material. Given that the light trapping effect originates from interference it is logical that a comparison with Si solar cells covered by a standard antireflective coatings (ARC) as a reference sample should be obligatory. Thus, an evaluation of "plasmonic effects" introduced by metal NPs and the understanding of the optical and the optoelectronic effects due to the integration of such metal NPs into an ARC or a passivating layer on Si is of particular interest.

1.4 Outline

This thesis is organized as follows: Chapter 2 reviews the two passivation mechanisms: The chemical passivation properties of the Si/oxide interface will be discussed regarding recombination active interface defects. The field-effect passivation mechanism will be discussed in conjunction with AlO_x-single layers and AlO_x/SiN_x stacks. Chapter 3 is devoted to the sample preparation and the description of the used basic characterization tools. Chapter 4 has two main objectives: (i) Describing the development of the high-frequency capacitance voltage method for the analysis of chemical and field-effect passivation of metal-insulator-semiconductor (MIS) structures and (ii) identification and analysis of physical mechanisms that may distort the evaluation. In Chapter 5, plasma-enhanced chemical vapor deposited AlO_x-single layers and AlO_x/SiN_x stacks on c-Si are the subject of a detailed investigation regarding their passivation properties. Several process parameters will be varied, and the modified c-Si/AlO_x interfaces as well as the modified negative charges will be characterized by the methods described in chapter 3 and 4. Chapter 6 studies the optical as well as optoelectrical effects of Au NPs integrated into a titanium

oxide ARC on c-Si. Chapter 7 summarizes the main experimental results obtained in the previous chapters.

2 Fundamentals

The efficiency of crystalline Si solar cells is significantly affected by electronic recombination losses at the wafer surfaces, primarily through a suboptimal open-circuit voltage. A reduction in surface recombination is called surface passivation, which is discerned into two components: the chemical and the field-effect passivation. In this chapter these two passivation mechanisms will be discussed in conjunction to the passivation contributing properties of the materials investigated in this work.

2.1 Silicon surface passivation mechanisms

For a discussion of the Si surface passivation mechanisms [Din12b] it is insightful to consider the rate of surface recombination (U_s, in cm^{-2}s^{-1}) based on the Shockley-Read-Hall (SRH) formalism [Sho52, Hal52]. U_s can be expressed as a function of the interface defect density (N_{it}, in cm^{-2}) and the hole and electron densities at the semiconductor surface (p_s and n_s, respectively):

$$U_s = \frac{\left(n_s p_s - n_i^2\right) v_{th} N_{it}}{\frac{n_s + n_1}{\sigma_p} + \frac{p_s + p_1}{\sigma_n}}, \tag{2.1}$$

in which v_{th} represents the thermal velocity of the electrons, n_1 and p_1 statistical factors, n_i the intrinsic carrier concentration, and $\sigma_{p/n}$ the hole and electron capture cross sections. The driving force in surface recombination processes is the term $\left(n_s p_s - n_i^2\right)$, which describes the deviation of the system from thermal equilibrium under illumination. U_s can be decreased by a reduction in N_{it} or D_{it} (in eV^{-1}cm^{-2})[Gir88], which is referred to as chemical passivation. In a recombination event both electrons and holes are involved. It is worth noting that the highest recombination rate is achieved when $p_s/n_s \approx \sigma_n/\sigma_p$ [Abe93]. Consequently, another way to reduce the recombination is by a significant reduction in the density of one type of charge carrier at the surface by an electric field. This is called field-effect passivation [Abe93, Glu99].

Fig. 2.1 demonstrates the the effect of a fixed negative interface charge $Q_f = 2 \times 10^{12}$ cm^{-2} (in units of the elementary charge) on the simulated electron and hole density near the surface for p-type and n-type Si. The surface charge gives rise to band bending (Fig. 2.1(c)). For p-type Si, the increased majority carrier density leads to accumulation conditions (Fig. 2.1(a), whereas the n-type Si surface is inverted (Fig. 2.1(b)). In both cases, a decrease in recombination can be expected as n_s is strongly reduced. However, for the inversion
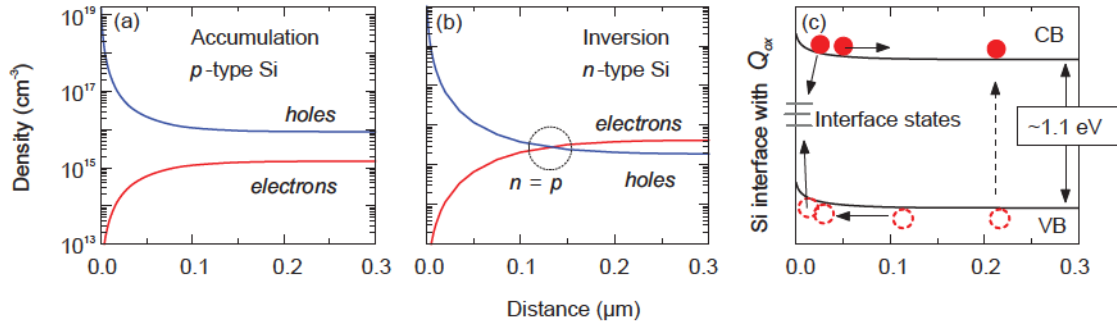
Figure 2.1: Electron and hole density below the Si surface for (a) p-type and (b) n-type Si
under influence of a negative fixed surface charge of $Q_f = 2 \times 10^{12}$ cm^{-2}; (c)
band bending under influence of Q_f. Data was simulated by using PC1D for
2 Ωcm wafers under illumination in [Din12b].

conditions, the electron and hole density become equal a distance away from the interface.
This phenomenon can be expected to enhance recombination in the subsurface when bulk
defects are present.

A measure that reflects the level of surface passivation is the surface recombination velocity S
(in cm/s):

$$S \equiv \frac{U_s}{\delta n}, \tag{2.2}$$

with δn representing the injection level. It is possible to deduce an effective surface
recombination velocity (S_{eff}) from the effective lifetime (τ_{eff}) of the minority carriers in
the Si substrate. The effective lifetime is measured in this work by the quasi-steady-state
photoconductance (QSSPC) decay technique [Sin96] and is controlled by bulk- and surface
recombination processes [Spr92, Nag99],

$$\frac{1}{\tau_{eff}} = \left(\frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{rad}} \right)_{bulk} + \frac{1}{\tau_{surf}}. \tag{2.3}$$

It illustrates that both intrinsic (Auger and radiative recombination) and extrinsic recom-
bination processes determine bulk recombination. Extrinsic recombination via bulk defects
is also known as SRH recombination. Impurities, such as Fe [Col08], lattice faults, and
dangling bonds at grain boundaries (multicrystalline Si) can all represent bulk defect states.
For a symmetrically passivated wafer with sufficiently low S_{eff} values, τ_{eff} can be expressed
as

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{W}, \tag{2.4}$$

with W the wafer thickness.

Since τ_{bulk} is generally not known, an upper level of S_{eff} can be calculated by assuming

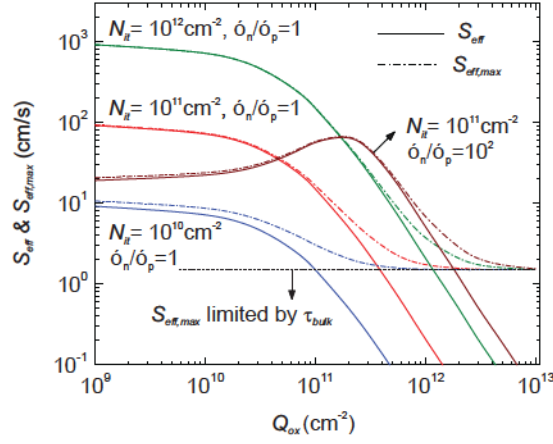Figure 2.2: Simulated S_{eff} and $S_{eff,max}$ values for a variation of Q_f and N_{it}. Note that the relation σ_n/σ_p affects the scaling between S_{eff} and N_{it} (vertical axis) and not the qualitative picture. The simulation is an approximation to illustrate general trends and was calculated using PC1D in [Din12b]. The parameters used were $\sigma_n = \sigma_p = 10^{-16}$ cm^{-2} for $\sigma_n/\sigma_p = 1$; $\sigma_n = 10^{-15}$ cm^{-2} and $\sigma_p = 10^{-17}$ cm^{-2} for $\sigma_n/\sigma_p = 10^2$. Other values included a bulk resistivity of 22 Ωcm p-type Si (doping of 7.2 x 10^{15} cm^{-3}), an injection level of $\delta n = 5 \times 10^{14} cm^{-3}$ and $\tau_{bulk} = 10$ ms.

that recombination only occurs at the wafer surfaces (i.e., $\tau_{bulk} \to \infty$),

$$S_{eff,max} = S_{eff} < \frac{W}{2\tau_{eff}}. \tag{2.5}$$

For bulk lifetimes > 1 ms and for injection levels for which Auger recombination is not dominant, $S_{eff,max}$ is a good approximation for the actual value of S_{eff}.

Fig. 2.2 illustrates the influence of the chemical and field-effect passivation on the surface recombination velocity by simulations [Din12b]. S_{eff} is observed to decrease linearly with a reduction in N_{it}. In addition, it is observed that the reduction in S_{eff} by field-effect passivation is especially prominent for Q_f values $> 10^{11}$ cm^{-2}. The simulations show that for moderately doped Si a twofold increase in Q_f produces a fourfold decrease in S_{eff} (i.e., $S_{eff} \sim 1/Q_f^2$, for sufficiently high Q_f values) [Hoe08a]. It also shows that the trend between S_{eff} and Q_f changes significantly when the value of σ_n/σ_p is increased from 1 to 10^2. In the latter case, a maximum appears in S_{eff} at $Q_f = 2$ x 10^{11} cm^{-2}, which coincides with the condition for maximum recombination ($p_s/n_s = \sigma_n/\sigma_p = 10^2$). In addition, higher Q_f values > 4 x 10^{11} cm^{-2} appear to be required to activate the field-effect passivation. It is worth noting that, for the case of AlO$_x$, a value of $\sigma_n/\sigma_p \gg 1$ is probably more realistic than $\sigma_n/\sigma_p = 1$. As will be discussed later, the c-Si/AlO$_x$ interface is essentially Si/SiO$_x$-like [Ste02a, Ste02b]. The value of $\sigma_n/\sigma_p \sim 10^2$ reported for thermally grown SiO$_2$ interfaces may therefore be a better assumption for the Si/AlO$_x$ interface [Glu99, Abe92].

2.2 Oxidic surface passivation materials

The semiconductor/insulator interface (S/I-interface) constitutes the basic building block of numerous applications such as micro- and nanoelectronic devices [Ger05], thin film transistors [Che12, Kim09], Metal-oxide semiconductor field effect transistors (MOSFETs) [Xua07], high energy radiation and particle detectors [Gar13], Micro-Electro-Mechanical Systems (MEMS) capacitive switches [Li09] and many other integrated circuits (IC) as well as advanced high efficiency solar cell architectures [Din12b]. For many decades, silicon (Si) and its oxide (SiO_2) have been the semiconductor and the gate dielectric of choice of the microelectronic industry, respectively. Accordingly, the Si/SiO_2-interface has been the cornerstone of all metal-oxide-semiconductor (MOS) based electronic devices and ICs. In conventional MOS technology, thermally grown SiO_2 has met key requirements such as a high-quality Si/SiO_2 interface with low interface state densities below 10^{10} cm^{-2}eV^{-1} along with highly insulating properties. Owning to the downscaling of ICs, MOSFET channel lengths have to decrease to the submicrometer range, dictating concomitant decrease of the oxide thickness to the sub-nanometer range. This trend gives rise to high leakage currents, because of increasing tunneling processes across the oxide, which induce off-state leakage currents and consequently a lossy standby mode by power dissipation. In this regard, it was necessary to introduce insulating materials with higher dielectric constant (high-k dielectrics) compared to SiO_2 as alternative [Wil01, Joh06]. High-k dielectrics offer many advantages such as low defect densities at interfaces with semiconductors providing good channel transport for electrons and holes. Amorphous aluminum oxide (AlO$_x$ or Al_2O_3) is currently being investigated as a promising high permittivity (high-k) material for the above mentioned application and in particular as an excellent passivation material for high-efficiency crystalline silicon solar cells [Din12b].

2.2.1 Defect model for the Si/SiO$_x$-interface

The formation on an ultrathin SiO$_x$ interlayer plays a crucial role when applying oxidic passivation materials, such as SiO$_2$ [Nic82, Hel94, Sze07], Al$_2$O$_3$ [Kim03, Hoe08a, Din12b] and TiO$_2$ [Cam99, McC04], on c-Si . Therefore, this section presents the current model for defects at the Si/SiO$_x$-interface based on the most recent experimental and theoretical investigations. The Si/SiO$_2$-interface and its electrically active defects have been subject to extensive studies (see [Len05] and references therein). Beginning with electron paramagnetic resonance (EPR) studies by Nishi, et al. [Nis72], different models for the defect state distributions at the Si/SiO$_2$-interface were developed [Ger86, Fli95], mainly based on results obtained from EPR and capacitance voltage investigations (among others).

The dominant electrically active defects at the Si/SiO$_2$ interface have been identified as several varieties of centers (P$_b$, P$_{b0}$, and P$_{b1}$). Fig. 2.3(a) shows that all centers consist of an unpaired electron on a Si backbonded to three other Si atoms at the Si/SiO$_2$ interface. It has been established that each center has two levels in the silicon band gap [Len05, Cam02], as depicted in Fig. 2.3(b). The essentially identical (111) Si/SiO$_2$ P$_b$ centers and (100) Si/SiO$_2$ P$_{b0}$ centers each have two levels separated by about 0.7 eV and more or less symmetrically distributed in the silicon band gap [Ger86, Poi84]. The (100) Si/SiO$_2$ P$_{b1}$ variant has two levels separated by just a few tenths of an electron volt, with the density of states is skewed toward the lower part of the silicon band gap [Cam02]. First-principles calculations revealed that the energetic positions of the P$_{b0}$, and P$_{b1}$ centers in the lower part of the c-Si band gap are approximately 0.29 eV apart [Kat06], in accordance with
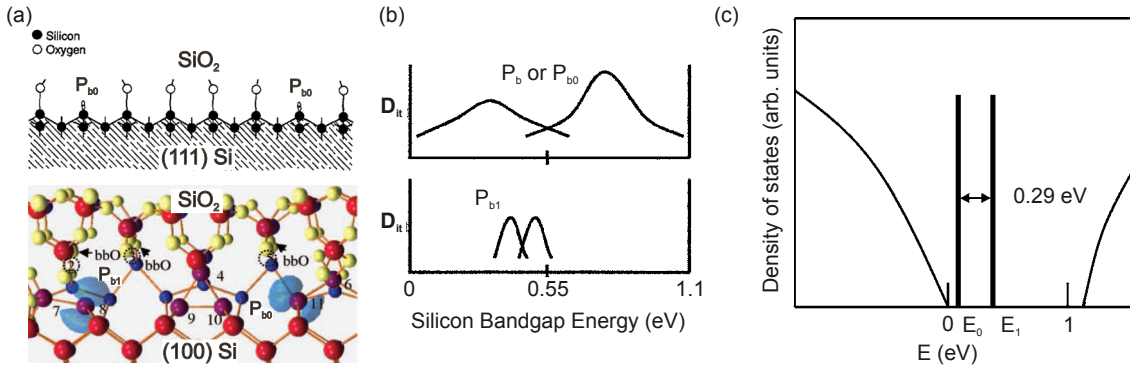
Figure 2.3: (a) Structure of P$_b$ centers on c-Si wafers of (111) and of P$_{b0}$ and P$_{b1}$ centers on c-Si wafers of (100) orientations. In the lower graphic yellow balls represent O atoms. Red and blue balls represent Si atoms. Blue isosurfaces represent dangling bonds at P$_{b1}$ and P$_{b0}$ centers. Graphics are taken from [Hel94] and [Kat06]. (b) Schematic representation of the density of states of the P$_b$ or P$_{b0}$ and P$_{b1}$ defects as a function of band-gap energy. The sketches provide only a crude semiquantitative representation. Graphic is taken from [Cam02]. (b) Schematic densities of states in the vicinity of the Si band gap. Gap states corresponding to P$_{b0}$ and P$_{b1}$ centers are denoted by E$_0$ and E$_1$. Graphic is taken from [Kat06].
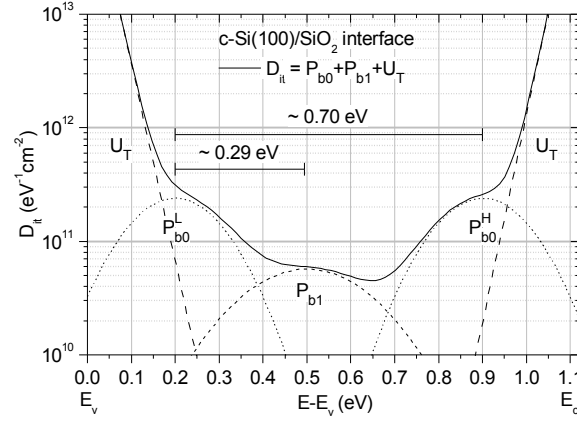
Figure 2.4: Density of defect state density (D_{it}) at the (100) c-Si/SiO$_2$ interface as a function of band-gap energy. Gaussian distributions represent P$_{b0}$ and P$_{b1}$ -like defects. Their energetic positions are in accordance with experimental and theoretical observations from [Cam02, Len05, Kat06, O'S01] (among others). Strained bond defects at the Si band edges are denoted as U$_T$ and described by exponential functions [Fli95].

experimental observations [Cam02].

Fig. 2.4 summarizes the experimental and theoretical observations of the electrically active defects at the Si/SiO$_2$ interface. The two levels of the P$_{b0}$ center are Gaussians denoted as P$_{b0}$^{L} at the lower part and P$_{b0}$^{H} at the higher part of the c-Si band gap. The two levels of the P$_{b1}$ center are represented by one Gaussian, since they are energetically almost indistinguishable. These centers are believed to be the main contributors to the interface defects state density (D_{it}). However, it is worth noting that other types of defects, that are not EPR-active or their densities are below the EPR detection limit ($\sim 10^{12}$ cm^{-2} spin density), may also contribute to D_{it} [Ger86, Fli95]. In fact, very recent studies based on the highly sensitive (10^{11} cm^{-2} spin density) spin-dependent-recombination (SDR) based EPR technique have indicated new types of defects at the Si/SiO$_2$ interface [Mat12, Ots13]. This demonstrates that a complete understanding of the defect states at the Si/SiO$_2$ interface has clearly not been achieved, yet, and that it is still intensely debated. Therefore, in this work the defect distributions in the D_{it}-spectra are described as P$_{b0}$- and P$_{b1}$-like, assuming they indeed are the main contributors as most studies suggest.

2.2.2 AlO$_x$-single layers and AlO$_x$/SiN$_x$ stacks on c-Si

The high level of passivation of AlO$_x$ is related to the combination of excellent chemical surface passivation, lowering the interface defect density (D_{it}), and field-effect passivation by negative oxide-trapped charges (Q_{ox}) located near the semiconductor-oxide interface. The latter is of particular interest for the passivation of p-type Si [Din12b]. AlO$_x$ produced by atomic layer deposition (ALD) [Hoe06] and by plasma enhanced chemical vapor deposition (PECVD) [SC09] have already demonstrated excellent passivation properties. A silicon oxide (SiO$_x$) interlayer formed at the Si/AlO$_x$ interface plays a critical role in the saturation of dangling bonds as well as the formation of the negative charge [Hoe08a, Kim03]. Hence, a wide range of methods to produce and control this SiO$_x$ interlayer have been investigated including ALD [Din10], PECVD [Din11c], thermal [Mac11, Din12a] and wet-chemical [Laa12] oxidation. With increasing SiO$_x$ thickness the chemical passivation improves (i.e. decrease of D_{it}) [Mac11], however, at the cost of the field effect passivation [Din11a, Mac11] due to a reduction of the negative Q_{ox} (or Q_f) at the SiO$_x$/AlO$_x$ interface. Therefore, low-cost ultrathin wet-chemical SiO$_x$-interlayers placed between PECVD-AlO$_x$/SiN$_x$-stacks and the Si wafer have demonstrated an improvement of the chemical passivation of the Si surface [Laa12] while maintaining the field effect passivation. However, for a better control of the latter a clearer understanding of the origin of the negative charges needs to be established [Din12b, Hoe08a]. Through simulations it has been recognized that (ionized) point defects are the origin of the charged traps [Ste05, Rob05, Liu10, Web11, Cho13]. Fig. 2.5(a) illustrates the transition levels induced by native point defects and dangling bonds (DB) in amorphous Al$_2$O$_3$that were calculated by Cho et al. [Cho13]. Traps related to Al vacancies (V$_{Al}$) and oxygen interstitials (O$_i$) are deep acceptors [Cho13] and can be charged negatively [Mat03]. Whereas the Al interstitial (Al$_i$) is a deep donor. The O vacancies (V$_O$) can act as donor or acceptor depending on the position of the Fermi level [Cho13]. It can be responsible for electron hopping and trapping, though not likely for the negative charge [Liu10]. The negatively charged tetrahedral AlO$_4$ which is dominant near the SiO$_x$/AlO$_x$ interface [Kim03] may also be a candidate. The fixed negative charge is consistent with a model for the local atomic bonding of noncrystalline Al$_2$O$_3$ that has two different bonding environments for the Al atoms [Joh01]: (a) a tetrahedrally coordinated Al site that has a net negative charge, and (b) and octahedrally coordinated site in which the Al has a charge of 3+. The negatively charged Al atoms can bond directly to the O atoms of the SiO$_2$ interfacial and this is the arrangement that is responsible for the negative fixed charge.

However, recent experimental works on atomic layer deposited (ALD) AlO$_x$ on c-Si demonstrated that charging of traps near the SiO$_x$/AlO$_x$-interface may play an important role in the formation of the negative charge. Defect states at the SiO$_x$/AlO$_x$ interface were charged negatively either by photon-induced charge injection [Gie08] or by constant voltage stress (V$_{stress}$)-induced charge trapping [Gon13b, Suh13, Raf13] from the Si. However, the charging mechanisms at the SiO$_x$/AlO$_x$ interface and in particular in the AlO$_x$ bulk
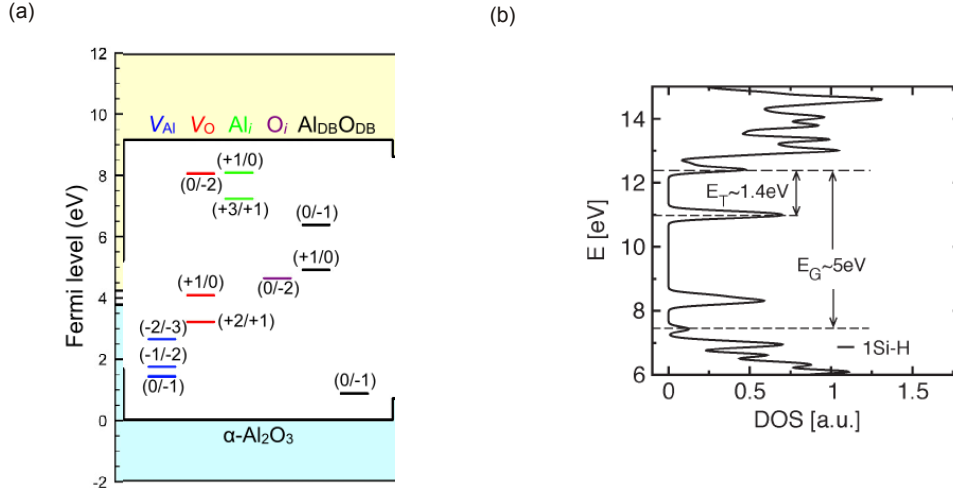
Figure 2.5: (a) The position of thermodynamic transition levels for native point defects and dangling bonds (DB) in α-Al$_2$O$_3$ is shown. The point defects consist of Al and O vacancies (V$_{Al}$ and V$_O$) as well as interstitials (Al$_i$ and O$_i$). The charge state of the acceptor and/or donor levels in the unoccupied and occupied state is indicated in brackets. Graphic is taken from [Cho13]. (b) Total calculated density of stated (DOS) of Si$_3$N$_4$ with one 1Si-H defect. From the curve, it is possible to extract the energy width of the bandgap (E$_G$) and the energy depth of the trapped electron with respect to the bottom of the conduction band (E$_T$). Approximately 1 eV above the top of the valence band, it is possible to note also the presence of deep states. Graphic is taken from [Via11a].

are still not yet clearly understood and more detailed experimental analysis is necessary [Din12b].

Of particular interest for Si solar cell applications are thin passivating AlO$_x$ films covered by amorphous SiN$_x$ (or a-SiN$_x$:H) capping layers synthesized by PECVD. Such passivation stacks have been applied at the rear and front side of Si solar cells [Gat11, SC10] reaching efficiencies >20% [Sch12]. Capping the passivating AlO$_x$ with SiN$_x$ offers several advantages in comparison to uncapped single AlO$_x$ layers for Si solar cell processing:

- The thermal budget during SiN$_x$ deposition (350–450 °C) can activate the surface passivation induced by AlO$_x$ [Din09].

- The application of a SiN$_x$ capping layer can extend the process window for solar cells in terms of AlO$_x$ film thickness and firing temperature [Sch09, Ric11]. Richter et al. have reported that five ALD cycles of Al$_2$O$_3$ in combination with a SiN$_x$ capping layer already results in good passivation properties for p^+-emitters [Ric11, Hoe07].

- AlO$_x$/SiN$_x$ stacks at the rear side of screen-printed solar cells lead to improved chemical stability. It has been observed that the application of metal pastes directly on AlO$_x$ can disintegrate the AlO$_x$ material during firing [Din12b]. N-rich SiN$_x$ layers appear to be robust and to remain chemically stable. These capping films can

therefore protect the AlO_x films from damage caused e.g. by metal paste.

- When ultrathin AlO_x films are considered at the rear side, an SiN_x capping layer can be useful to increase the physical thickness to improve the rear reflection properties of the solar cell [Din12b].

The stacks exhibit a negative fixed charge density [Mac11, Ric11]. This is consistent with the expectation that the positive fixed charge density in SiN_x films applied on Si is related to the Si/SiN_x interface. When the SiN_x is used as capping layer on AlO_x, the positive charges in SiN_x may be absent or much lower in density when compared to SiN_x applied directly on Si.

In addition, defect levels located in the SiN_x [War92, Rob94, Via11b, Via11a] also play an important role in the investigation of the charge mechanisms of AlO_x/SiN_x stacks. Fig. 2.5(b) demonstrates by way of example calculated states in the Si_3N_4 band gap originating from 1Si-H dangling bond defects [Via11a]. Si dangling bonds also introduce defect states located inside the SiN_x band gap at similar energetic positions as the 1Si-H dangling bond depending on its charge state. The density of these defect states as well as the energetic position of the Fermi level dictate whether these states account for charge trapping and/or transport [Via11b]. In fact, through charge injection the traps can be charged positively or negatively and, thus, influence the field-effect passivation of the underlying c-Si [Web09].

The consideration of these defect states located in the AlO_x and in the SiN_x is crucial for the analysis of charging mechanisms and for the evaluation of the field-effect passivation properties of AlO_x-single layers and AlO_x/SiN_x stacks deposited on c-Si.

3 Experimental techniques

3.1 Sample preparation

3.1.1 Plasma-enhanced chemical vapor deposition of AlO_x-single layers and AlO_x/SiN_xstacks on Si

The Si wafer preconditioning, the deposition of AlO_x and SiN_x as well as the thermal post-deposition treatments were performed by CiS Erfurt and Roth & Rau AG in collaboration with HZB. The wafers used were in all cases both sides polished p-type float-zone (FZ) silicon wafers ([100], Boron doped, 1-5 Ωcm) with a thickness of 280 µm. To investigate the impact of interfacial oxides and surface preparation on the passivation quality of AlO_x/SiN_x, different surface terminations consisting of either thin oxides or a hydrogen terminated surfaces were prepared. Details on the wet chemical surface treatments are displayed in Table 3.1. The surface treatment was followed by the deposition of AlO_x (25 nm) and SiN_x (100 nm) using an inline Plasma-enhanced chemical vapor deposition (PECVD) reactor MAiA of Roth & Rau AG. To produce amorphous AlO_x films, a mixture of trimethylaluminum and nitrous oxide was used. The amorphous SiN_x forms a 100 nm thick antireflection coating as used in the front side of silicon solar cells.

To investigate the activation and thermal stability of the passivation, the samples were subjected either to an annealing step at 425°C in air (15 min) or to an industrial firing process (wafer temperature 860 °C, ~ 3 s) in air.

For minority charge lifetime measurements symmetrical SiN_x/AlO_x/c-Si/AlO_x/SiN_x-structures (Fig. 3.1(a)) were fabricated through surface preconditioning and deposition on both sides of the Si wafer. For C-V measurements, first, round Al contacts pads (thickness:

Tab. 3.1: Wet chemical processes applied to silicon wafer surfaces prior to AlO_x-single or AlO_x/SiN_x-stack deposition. The process step labeled Hot-Diw80:HCl leads to wet chemical oxide (SiO_x) growth of 1.0 - 1.5 nm thickness. It was applied after either just HF or RCA+HF. SC1 and SC2 are standard cleaning processes consisting of NH_4OH/H_2O_2/H_2O (75°C) and HCl/ H_2O_2/H_2O (75°C), respectively.

Process	label	Process mixture
Radio corporation of America	RCA	SC1 + HF + SC2 + HF
Hydrofluoric acid dip	HF-Last	HF(2%)/H_2O (60 s, 25 °C)
Hot deionized water and HCl	Hot-DiW80:HCl	Hot-DiW/HCl (1:1000): 80°C
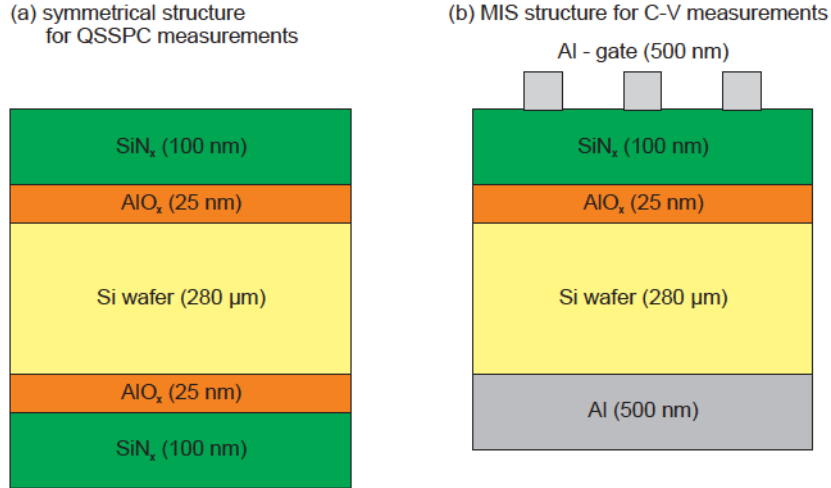
Figure 3.1: (a) Symmetrical sample structure scheme for minority charge carrier lifetime measurements via QSSPC. (b) Metal-Insulator-Semiconductor (MIS) structure scheme for HF C-V measurements. Samples of structure (b) were fabricated from (a) through removal of AlO_x/SiN_x-stack from one side and Al contact deposition.

500 nm, diameter: ~0.65 mm) were deposited on the AlO_x/SiN_x-stack on one side of the wafer through thermal Al evaporation (wafer temperature < 90°C) to form the gate contacts. Then, the AlO_x/SiN_x-stack on the other side was removed through mechanical polishing. The resulting bare Si surface was then fully covered by Al (500 nm) to form an ohmic back contact. Hence, a MIS-structure is formed as depicted in Fig. 3.1(b).
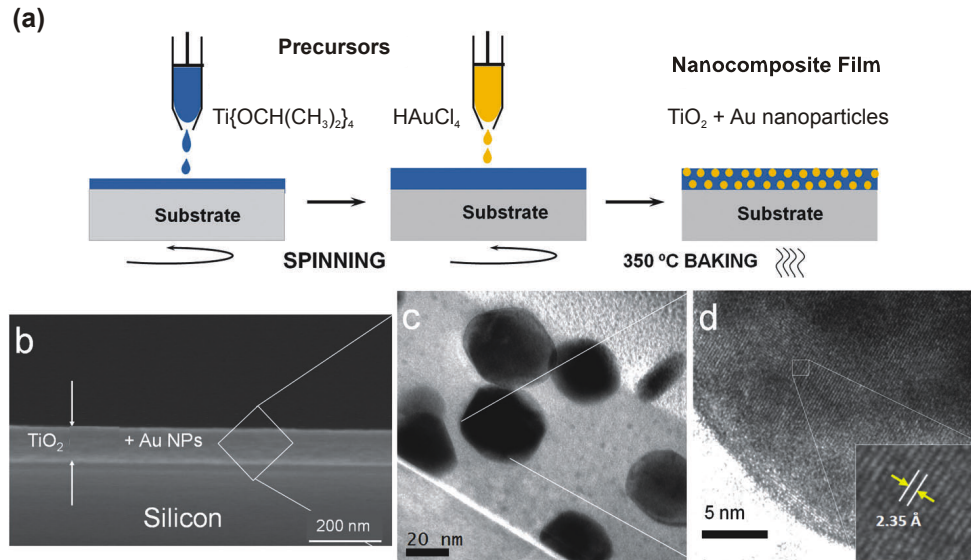
Figure 3.2: (a) The three-step process of TiO$_2$ matrix preparation and in situ synthesis of AuNPs: spin coating of the precursors solutions followed by thermal annealing at 350 °C for 5 minutes to form the AuNPs and eliminate solvents. (b) Scanning electron micrograph (SEM) of the composite, showing the transverse view. (c) Low-magnification TEM image of a cross section of the thin film. (d) HRTEM image of a single gold NP inside the composite; gold (111) atomic planes are visible. Figures were taken from [Ped11].

3.1.2   TiO$_2$ with embedded Au nanoparticles

The sample preparations were performed by UVEG Valencia. TiO$_2$-layers with embedded Au nanoparticles (TiO$_2$:AuNP) were deposited on one side of a pre-cleaned Si wafer by spin-coating (see Ref. [Ped11] for more details). The wafers used were one side polished n-type FZ Si wafers ([111], Phosphor doped, >5000 Ωcm) with a thickness of 380 µm. As depicted in Fig. 3.2(a), an ethanolic solution of the TiO$_2$ precursor and Pluronic P123 is spin coated onto the polished side of the Si wafer or a glass substrate. Subsequently, a solution of HAuCl$_4$ (0.01 – 0.25 M in ethanol) was deposited dropwise onto the surface and the sample was spun again. Finally, the resulting film is baked at 350 °C for 5 min. This leads to the formation of a thin dielectric layer containing AuNPs, which are homogeneously distributed and uniform in size with average diameters ranging in a 40-50 nm interval (see Fig. 3.2(b-d)). Since the TiO$_2$ layer has a thickness of 70-90 nm, it exhibits its first interference minimum near 750 nm which is typical for regular antireflection coatings (ARC). AuNPs embedded into the TiO$_2$ layer modify the optical properties of the latter so that one can observe wavelength-dependent changes of the hybrid layer reflection spectrum as compared to that of the bare TiO$_2$ film of the same thickness. For the etching treatment of TiO$_2$:AuNP thin films, a 0.2‰ solution of HF (Fluka, 40%) in water was heated in a bain-marie at 40 °C. The Si samples with TiO$_2$:AuNP thin films were immersed into the HF

solution under constant agitation for 1 min, and were then washed with deionized water. For photoconductance measurements, the unpolished side of the Si wafer was metalized with 500 nm thick Al stripes with a distance of 250 µm (see Fig. 3.3).

3.2 Sample characterization

3.2.1 Optical properties: UV-VIS spectroscopy

The optical measurements were performed with commercial spectrometers (Perkin Elmer Lambda 19 DM and 1050) with integrating spheres. The absorption A(hν) was calculated from the reflection R(hν) and transmission T(hν) data by using the conservation rule A(hν) + R(hν) + T(hν) = 1. The optical haze was obtained by measuring the diffused and total transmission and calculating their ratio.

3.2.2 Minority charge carrier lifetime measurements

The effective minority charge carrier lifetime in Si with symmetric AlO_x/c-Si/AlO_x and SiN_x/AlO_x/c-Si/AlO_x/SiN_x structures was quantified by employing photoconductance decay measurements with a WCT-100 Sinton-Lifetime-Tester [Sin96]. The sample is placed near the coil of an oscillator circuit and excess charge carriers are generated by a short and intense light pulse provided by a photo flash equipped with an IR filter. Infrared light is chosen for excitation in order to yield a homogeneous generation rate. By the additional charge carrier density in the 10^{16} cm^{-3} range the conductance of the sample is changing which is detected as a detuning of the oscillator circuit due to eddy currents in the sample. The method is fast enough to obtain the temporal development of the conductance after the initial flash. The conductance is directly proportional to the excess carrier density by $\sigma = e(\mu_e + \mu_h)\Delta nW$, therefore the effective lifetime can easily be calculated by employing $\tau_{eff,meas}(t) = \Delta n(t)/\delta_t \Delta n(t)$. Thus, a data set of $\tau_{eff,meas}(t)$ is obtained from the decay of the excess conductance.
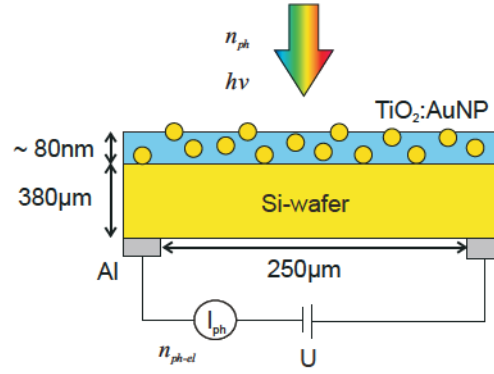
Figure 3.3: Experimental scheme for photoconductivity measurements.

3.2.3 Photoconductance measurements

In order to obtain information on the influence of the TiO_2:AuNP layer on the efficiency of photogeneration of charge carriers in an underlying Si substrate, spectrally resolved photoconductivity measurements were carried out. Fig. 3.3 shows the experimental scheme that was used for photoconductivity measurements. The photoconductivity of a Si wafer is based on the optical absorption and the transport of the photo-generated charge carriers towards the contacts of an absorbing Si material at an applied bias. A Xenon high pressure lamp (200 W) and a halogen light bulb (250 W) in combination with a grating monochromator provided a monochromatic photon flux density $\Phi_{ph}(h\nu) \leq 10^{12}$ photons/cm^2/s, measured by calibrated Si photodiodes, for the spectral range 300 nm - 1050 nm. Upon illumination of a Si wafer (thickness d = 380µm), the photon flux density $\Phi_{ph}(h\nu)$ leads to the generation of free charge carriers. Using a Keithley 6430 Sub-FemtoAmp SourceMeter very sensitive measurements down to a noise level of about $I = 5.10^{-16}$ A were possible and the photocurrent I_{ph} was measured as the difference between the current in the dark and under illumination. In order to maintain a constant charge carrier lifetime over the whole spectrum the photoconductivity measurements were performed in constant photocurrent mode (CPM) [Van81]. To obtain a constant photocurrent the light intensity of the tungsten-halogen light bulb was varied using neutral-grey filters and the lamp current was adjusted according to the set point of the constant photocurrent. The low current measurements were performed under vacuum conditions.

From the measured photocurrent the number of photo-generated electrons $n_{ph\text{-}el}$ can be calculated while the photon flux Φ_{ph} provides the number of incoming photons n_{ph} per area and time at the given photon energy hν. Thus the external and internal quantum efficiency are obtained which refer to the incoming photons as

$$EQE(h\nu) = \frac{n_{ph-el}}{n_{ph}} = \frac{U}{l^2} \cdot \mu \cdot \tau \cdot (1 - R(h\nu)) \cdot (1 - \exp(-\alpha(h\nu) \cdot d)) \qquad (3.1)$$

and

$$IQE(h\nu) = \frac{EQE(h\nu)}{1 - R\left(h\nu\right)} = \frac{U}{l^2} \cdot \mu \cdot \tau \cdot \left(1 - \exp\left(-\alpha\left(h\nu\right) \cdot d\right)\right) \tag{3.2}$$

where *U* is the applied voltage, *l* the contact distance, *μ* the mobility and *α(hν)* the absorption coefficient. Critical quantities to be considered are the reflectance *R(hν)* and the charge carrier lifetime τ. Both quantities are influenced by the TiO_2:AuNP-layer on top of the Si wafer. On the one hand it acts as an ARC, on the other hand it affects the passivation of the Si surface (i.e. of the Si/TiO_2:AuNP interface) and therefore the charge carrier lifetime τ in the Si.

4 Development of the high frequency capacitance voltage method

4.1 Introduction

This chapter gives an overview of the main physical and mathematical aspects regarding the development of the high frequency (1 MHz) capacitance voltage (C-V) and capacitance time (C-t) method for metal-insulator-semiconductor (MIS) capacitors [Nic82, Sze07]. The detailed mathematical derivations and algorithms for data acquisition used for this C-V method can be found in [Fue77, Hen11]. In the work of [Hen11], which was supervised in the framework of this thesis, the C-V method and in particular the data acquisition and analysis algorithms originally developed in [Fue77], were adapted into a new LabVIEW-based measurement and analysis software. This adaptation allowed a further development and modification of the analysis and evaluation algorithms. This enabled a reliable analysis of new material systems, such as AlO_x-single layers and AlO_x/SiN_x stacks on c-Si, which are not as stable and insulating as thermal SiO_2 on c-Si. In order to demonstrate the capabilities of the developed C-V method, firstly, three symmetrical samples consisting of 100 nm thermally grown SiO_2 on double side polished n-type Si wafer (FZ, [100], phosphorus doped, 1-5 Ωcm) were prepared. The SiO_2 thickness of two of these samples was reduced to 49 nm and 12 nm by HF-etching. The thicknesses were verified via spectral ellipsometry. The three symmetrical structures underwent a forming gas anneal and the minority charge carrier lifetime was measured via QSSPC. Afterwards, the SiO_2 on one side was removed by HF-etching followed by Al contacts deposition via thermal evaporation to form MIS structures for C-V measurements. With these c-Si/SiO_2 structures the effects of leakage currents are investigated. The results regarding field-effect and chemical passivation are then compared to the minority charge carrier lifetime measurements. Secondly, using a c-Si/AlO_x/SiN_x structure, the effects induced by charge trapping and charge instabilities are investigated through C-t transient and C-V hysteresis analysis.

4.2 Determination of the Si/SiO₂ interface defect state density and oxide charge density

An ideal MIS capacitor is defined as follows [Nic82, Sze07]: (1) The only charges that can exist in the structure under any biasing conditions are those in the semiconductor and those, with an equal but opposite sign, on the metal surface adjacent to the insulator, i.e., there are no interface traps ($Q_{it} = 0$) nor any kind of oxide charge ($Q_{ox} = 0$). (2) There is no carrier transport through the insulator under direct current (dc) biasing conditions, i.e. the resistivity of the insulator is infinite. When an ideal MIS capacitor is biased with positive or negative gate voltages, basically four cases can exist at the semiconductor surface. In Fig. 4.1 these four cases are illustrated for a thermally grown SiO₂ on n-type c-Si. For the discussion of the ideal MIS capacitor, Q_{it} and Q_{ox} have to be disregarded. When a positive voltage ($V > 0$) is applied to the metal gate, the conduction-band edge E_c bends downwards near the interface and is closer to the Fermi level E_F. For an ideal MIS capacitor, no current flows in the structure, which means that E_F remains flat in the semiconductor. Since the carrier density depends exponentially on the energy difference (E_F - E_c), this band bending causes an accumulation of majority charge carriers (here electrons) near the semiconductor surface. This is the accumulation case as depicted in Fig. 4.1(a). When the positive voltage is reduced, the bands bend upward, and at V = 0 the flat band (FB) condition is achieved (Fig. 4.1(b)), where the band bending is 0. At a low negative voltage ($V < 0$) the density of majority charge carriers is reduced at the interface, as compared to the c-Si bulk (Fig. 4.1(c)). This is the depletion case. When a larger negative voltage is applied, the bands bend upward even more. At a certain negative voltage, which is referred to as the mid gap (MG) voltage, the intrinsic level E_i and the Fermi level E_F overlap at the surface. Once the MG voltage is surpassed ($V \ll 0$) , i.e. E_i crosses over E_F, the number of minority charge carriers (here holes) at the surface becomes larger than that of the majority carriers (Fig. 4.1(d)). Thus, the surface is inverted and this is the inversion case. Similar results can be obtained for p-type c-Si when the polarity of the voltage is changed [Nic82, Sze07].

The resulting total MIS capacitance C (in F/cm²) of the biased structure for high-frequency (1 MHz) C-V measurements [Nic82] is expressed as

$$C = \frac{C_{ox}C_{sc}}{C_{ox} + C_{sc}}. \tag{4.1}$$

Here, C_{ox} is the oxide (or insulator) capacitance, which is constant for a given oxide thickness d_{ox}. C_{sc} describes the space charge capacitance of the Si, which depends on the gate voltage (i.e. band bending) for a given doping concentration N_A. The theoretical 1 MHz C-V curve of an ideal MIS structure consisting of Al contacts covering 100 nm SiO₂ on n-type c-Si ($N_A = 1.3 \times 10^{15}$ cm⁻³) is plotted in Fig. 4.2(a).

However, in a practical, non-ideal MIS capacitor, such as thermally oxidized n-type c-Si,
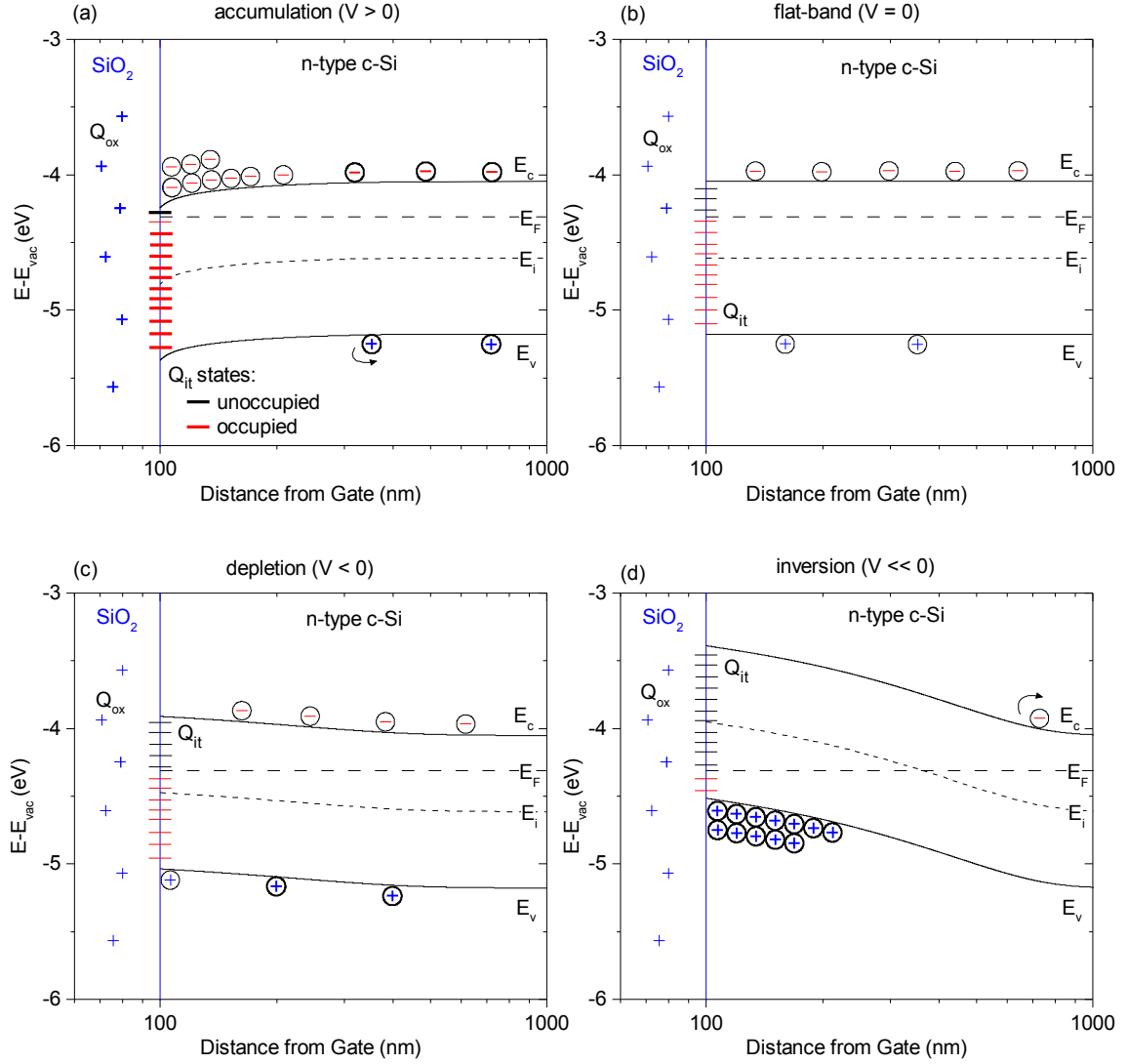
Figure 4.1: Energy-band diagrams for MIS capacitors, here SiO₂ on n-type c-Si, under different bias, for the conditions of: (a) accumulation, (b) flat band, (c) depletion, and (d) inversion. Interface trap charge Q_{it} and oxide charges Q_{ox} are indicated referring to a non-ideal MIS structure. Note the logarithmic scale of the abscissa.

interface traps Q_{it} (in C/cm^2) as well as oxide charges Q_{ox} (in C/cm^2) do exist that will affect the ideal MOS characteristics. Interface defect states located at the c-Si/SiO₂ interface and energetically within the c-Si forbidden band gap (see Fig.4.1(a)) have an amphoteric character. They can exchange charges with the c-Si in a short time, which means that by sweeping the gate voltage they can become occupied depending on the location of E_F at the interface. Interface defect states energetically located in the upper part of the c-Si band gap are considered to be acceptor-like (i.e. neutral when empty, negatively charged when filled) and those located in the lower part are considered donor-like (neutral when filled, positively charged when empty). The consequence of this amphoteric
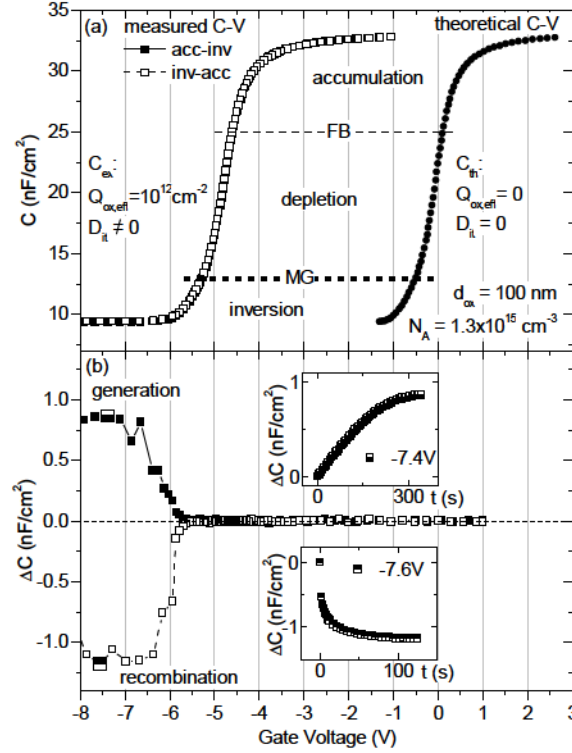
Figure 4.2: (a) Theoretical and experimental high-frequency (1 MHz) capacitance voltage (C-V) curves of MIS structures consisting of an Al-gate on 100 nm SiO$_2$ on n-type c-Si. C-V measurements were performed in relaxation mode from accumulation to inversion (acc-inv) and vice versa (inv-acc). (b) Corresponding relaxation capacitance ΔC over gate voltage. In inversion region relaxation due to minority charge carrier generation (for acc-inv) and recombination (for inv-acc) are indicated. The inserted transients ΔC-t indicate completed relaxation processes at the given gate voltages.

behavior is that the measured C-V curve becomes stretched out along the voltage axis, decreasing its slope relative to the ideal, theoretical C-V curve. This effect can be seen in Fig. 4.2(a). Oxide charges, other than those of the interface traps, can include the fixed oxide charge Q_f, the mobile ionic charge Q_m, and the oxide trapped charge Q_{ot}. Their sum results in a total oxide charge $Q_{ox} = Q_f + Q_m + Q_{ot}$ as shown in Fig. 4.1. In general, unlike interface-trapped charges, these oxide charges are independent of bias, so they cause a parallel shift in the gate-bias direction. In the case of positive oxide charges for SiO$_2$, this results in a shift of the C-V curve towards larger negative gate voltages, as measured in Fig. 4.2.

Consequently, the evaluation of interface defect states and oxide charge is based on the analysis of the measured C-V curve in comparison with the theoretical one of the corresponding ideal MIS capacitor [Ter62, Gro65, Sah69, Kat74]. On the one hand, the voltage conservation rules dictate that for an ideal MIS structure the overall theoretical

voltage is

$$U_{th} = \Phi_s + \Phi_{MS,i} - \frac{Q_{sc}}{C_{ox}}, \tag{4.2}$$

with Q_{sc} describing the space charge in the semiconductor, Φ_s the surface potential, and $\Phi_{M,Si}$ the work function difference between the gate metal and the intrinsic semiconductor. For Al and intrinsic Si $\Phi_{M,Si} = $ -0.22 V [Wer74]. On the other hand, for a practical MIS structure with oxide and interface charges the overall voltage is

$$U = \Phi_s + \Phi_{MS,i} - \frac{Q_{sc} + Q_{ox,eff} + Q_{it}}{C_{ox}}, \tag{4.3}$$

with $Q_{ox,eff}$ as the effective oxide charge. From these, the interface traps charge can be derived and expressed as

$$Q_{it} = -C_{ox}(U - U_{th}) - Q_{ox,eff}. \tag{4.4}$$

Q_{it} is related to the interface defect state density D_{it} (in cm^{-2}eV^{-1}) [Nic82] through

$$D_{it} = -\frac{1}{q_{el}} \frac{dQ_{it}}{d\Phi_s}, \tag{4.5}$$

where q_{el} is the charge of an electron. Combining Eq. 4.4 and 4.5 [Fue77] results in the final expression

$$D_{it} = \frac{C_{ox}}{q_{el}} \left[\left(\frac{C_{ox}}{C_{ox} + C_{sc}} \right)^2 \frac{dC_{sc}}{d\Phi_s} \left(\frac{dC}{dU} \right)^{-1} - \left(1 + \frac{C_{sc,lf}}{C_{ox}} \right) \right]. \tag{4.6}$$

Here, C_{sc} and $C_{sc,lf}$ are the semiconductor space charge capacitances for high and low frequencies, respectively. These are calculated for a known C_{ox} and N_A [Nic82], which are extracted from the experimental C-V curve by iteratively matching the slopes of the theoretical C-V curve to the experimental one in the accumulation and strong inversion regions, respectively [Hen11]. The term dC/dU is the experimentally accessible slope of the measured C-V curve which is stretched out due to charging of the interface defect states. It is obtained through a fitting algorithm using a second-degree polynomial [Hen11]. The value of D_{it} can be positioned correctly within the Si band gap using the known values of the surface potential, which is obtained from the calculated band banding [Hen11]

From the C-V measurements one can also obtain the effective oxide charge density (in cm^{-2}) at mid gap (MG), through

$$N_{ox,eff} = \frac{Q_{ox,eff}}{q_{el}} = \frac{C_{ox}}{q_{el}} (U_{MG,th} - U_{MG,ex}). \tag{4.7}$$

The parameters $U_{MG,th}$ and $U_{MG,ex}$ represent the mid gap voltages of the theoretical and experimental C-V curves, respectively. Unlike for flat band (FB), for a bias leading to $E_F = $ MG at the interface, charge contributions by acceptor- and donor-like interface defect states above and below the MG energy level of the Si band gap, respectively, are minimized.

Assuming $Q_{it} = 0$ at MG, the mathematical expression of $Q_{ox,eff}$ is defined [Goe73, Sno65] as

$$Q_{ox,eff} = \frac{1}{d_{ox}} \int_0^{d_{ox}} x \cdot \rho(x) dx \,. \tag{4.8}$$

Here, $\rho(x)dx$ is the element of the oxide space charge and x is its distance from the gate. This expression differs from the one for the total fixed oxide charge

$$Q_{ox} = \int_0^{d_{ox}} \rho(x) dx \,. \tag{4.9}$$

The definition in Eq. 4.8 indicates that $Q_{ox,eff}$ depends on the location x of the charge $\rho(x)$. One can differentiate between three cases: (1) For $x \to 0$, i.e. ρ is located towards the oxide/gate interface, then $Q_{ox,eff} \to 0$. (2) If ρ is uniformly distributed in the oxide, then $Q_{ox,eff} = 0.5\ Q_{ox}$. (3) For $x \to d_{ox}$, i.e. ρ is located near the semiconductor/oxide interface, then $Q_{ox,eff} \to Q_{ox}$. On the one hand, these cases imply that changes of ρ near the gate have less effect on $Q_{ox,eff}$ than changes of ρ near the semiconductor. On the other hand they imply, that changing the location of ρ, e.g. through redistribution of charges in the oxide, also changes $Q_{ox,eff}$, whereas Q_{ox} is not affected. These properties of $Q_{ox,eff}$ enable the evaluation of charge dynamics in the oxide (or dielectric) through hysteresis analysis which is discussed in section 4.5. In general, the fixed charge Q_{ox} (often also denoted as Q_f) is associated with the field-effect passivation of different materials on c-Si. However, in the case of SiO$_2$, SiN$_x$, and AlO$_x$ it is routinely reported [Nic82, Din12b] that the origin of their fixed charge is located near the c-Si interface. Therefore, $Q_{ox,eff}$ measured via C-V is generally accepted as an approximation for Q_{ox} and also agrees with charge densities obtained from corona charge experiments of these materials [Din12b]. In future reference, in order to concur with most literature, the effective oxide (or insulator) charge density will be referred to as $Q_{ox,eff}$ in units of the elementary charge per cm^2.

In Fig. 4.2(a) the high frequency C-V curve is measured in relaxation mode. This means the applied gate voltage is kept constant while the C-t trace is measured. Once the capacitance remains at a constant value within a defined time interval (here 10 s) the C-t trace is stopped and the average C-value within this last time interval is recorded for the C-V curve [Hen11]. This is then repeated for all gate voltages of the C-V measurement. In this manner, true equilibrium capacitances of the MIS system are obtained. For high frequency C-V measurements this relaxation is crucial since deviating capacitances may lead to errors in the determination of D_{it} [Kat74]. On the one hand, capacitance relaxations are observed in the inversion region due to the generation or recombination of minority charge carriers (depending on measurement direction) after each voltage step. These relaxations indicate whether true inversion capacitances are reached or if leakage currents are present preventing the formation of an inversion layer. On the other hand, slow charging of traps in the insulator or near the semiconductor interface, both affecting $Q_{ox,eff}$, also leads to
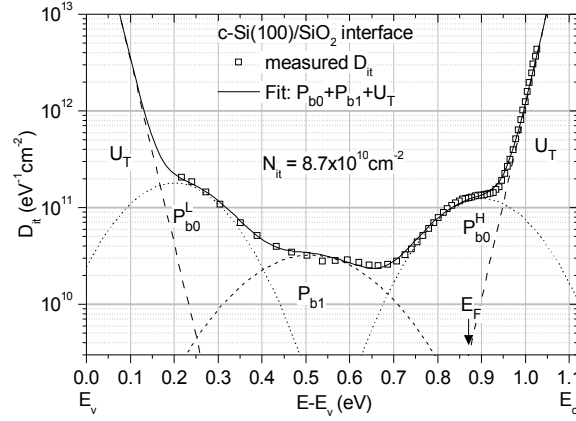
Figure 4.3: Defect state density (D_{it}) at the c-Si(100)/SiO$_2$ interface over c-Si band gap energy relative to the valence band edge E$_v$. The D_{it}-spectrum was fitted by the sum of Gaussian distributions for P$_{b0}$- and P$_{b1}$-like defects and exponential functions for strained bond defects ΔU$_T$. The donor- and acceptor-like states of the P$_{b0}$ defect are energetically separated in the lower (P$_{b0}^L$) and higher (P$_{b0}^H$) part of the Si band gap. For the P$_{b1}$ defect they are energetically close and represented by one Gaussian. The total defect density N_{it} integrated over the entire Si band gap through the fitting process is indicated.

a relaxation of capacitance. This relaxation is most pronounced in the depletion region of the C-V curve due to the larger slope. Here, changes of $Q_{ox,eff}$ distort the slope of the C-V curve and therefore also the calculated D_{it}. These effects will be discussed in more detail in section 4.6. However, this effect is not observed in the case of the thermal 100 nm SiO$_2$ as can be seen in the relaxation capacitance ΔC over gate voltage in Fig. 4.2(b). This is due to the stable charge of the thermal SiO$_2$, containing only positive fixed charges of $Q_{ox,eff} = 10^{12}$ cm^{-2}. Here, only in the inversion region the typical positive and negative relaxations implying the generation and recombination of minority charge carriers, respectively, are observed. The inserted transients ΔC-t indicate completed relaxation processes at the given gate voltages. Hence, true inversion capacitances are obtained.

An analysis of the C-V curves in Fig. 4.2(a) using Eq. 4.6 results in the D_{it}-spectrum depicted in 4.3. The c-Si/SiO$_2$ interface defect state density over nearly the entire c-Si band gap is obtained. Near MG (0.56 eV) a D_{it} of about 3×10^{10}cm^{-2}eV^{-1} is revealed, indicating an efficient chemical passivation typical for thermal SiO$_2$ [Ree88]. In fact, the D_{it}-spectrum can be fitted by Gaussian distributions with energetic positions as those reported for P$_{b0}$ and P$_{b1}$ defects (see section 2.2.1) as well as by exponential functions for strained bond defects U$_T$ [Fli95] at the c-Si/SiO$_2$ interface.

The fitting functions and parameters are presented in Tab. 4.1. The area of each Gaussian represents the density N_t of the corresponding defect type. Note that here the P$_{b0}$-like defect consists of donor states (P$_{b0}^L$) in the lower part of the c-Si band gap and acceptor states (P$_{b0}^H$) in the higher part, as described in section 2.2.1. Their energetic positions are in agreement with those reported in [Ger86, O'S01, Cam02, Len05]. Whereas the Gaussian

Si defect	type	function	E_t(eV) or $E_{v,c}$(eV)	w(eV) or $\beta_{v,c}$(eV^{-1})	N_t(cm^{-2}) or $N_{v,c}$ (cm^{-2})
dangling bond	P$_{b0}$^{L}	$\frac{N_t}{w\sqrt{\frac{\pi}{2}}}e^{-2\frac{(E_t-E)^2}{w^2}}$	0.20	0.20	4.5×10^{10}
	P$_{b0}$^{H}		0.51	0.26	1.1×10^{10}
	P$_{b1}$		0.20	0.20	3.1×10^{10}
strained bond	U$_T$	$N_{v,c}e^{-\beta_{v,c}|E_{v,c}-E|}$	0 , 1.12	44 , 46	2.8×10^{14}

Tab. 4.1: Fitting functions and parameters of Si defect types. For dangling bond defects E_t describes the central energetic position, w the width and N_t the area of the Gaussian distribution. Strained bond defects are described by exponential functions [Fli95] where $E_{v,c}$ describes the energetic position, $\beta_{v,c}$ an experimental value according to [Fli95] and $N_{v,c}$ the states for valence and conduction band.

distribution for the P$_{b1}$-like defect already includes the acceptor and donor states which are energetically very close to one another in the c-Si band gap [Cam02]. Its energetic position agrees with the one calculated in relation to the P$_{b0}$-like defect [Kat06]. Through summation of the individual areas (N_t) one can obtain the total defect density N_{it} over the entire Si band gap, in this case $N_{it} = 8.7\times10^{10}$ cm^{-2}.

In summary, the C-V method presented here allows the analysis of the parameters $Q_{ox,eff}$ and N_{it}, which are crucial for the evaluation of the field-effect and chemical passivation, respectively. The investigated c-Si/SiO$_2$ structure represents a MIS system which fulfills the two main requirements for a reliable analysis of the passivation properties via C-V: It is insulating, and has only fixed stable charges. The former is reflected in the relaxation behavior in the inversion region showing completed C-t transients, the latter in the accumulation and depletion region showing no relaxations. This ideal behavior enables a reliable determination of the D_{it} spectrum and of N_{it}. Therefore, it serves as a reference for the evaluation of other sample structures.

4.3 Effects of leakage currents

In this section the effects of leakage currents on the analysis of the C-V method are studied. Their identification and consideration is of crucial for the evaluation of $Q_{ox,eff}$ and N_{it} because leakage currents influence the formation of accumulation and inversion regions in MIS systems and therefore the accumulation and inversion capacitances [Yan99]. For this purpose, the thermal SiO_2 on n-type c-Si with different thicknesses $d_{ox} = 100$ nm, 49 nm and 12 nm are investigated.
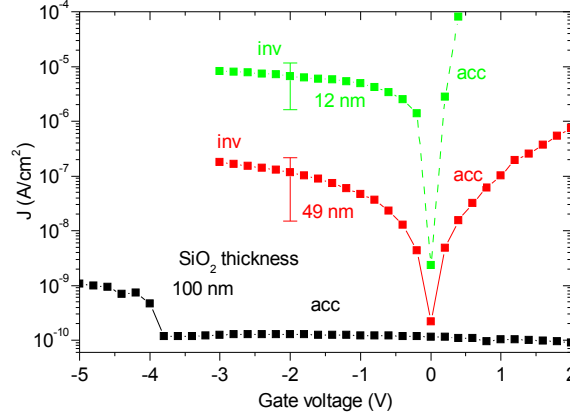
Figure 4.4: Current density - voltage measurement of MIS structures consisting of c-Si/SiO_2/Al with different oxide thicknesses $d_{ox} = 100$ nm, 49 nm and 12 nm. Accumulation (acc) and inversion (inv) regions are indicated for each structure. The error bars represent fluctuations of the current density when measured at different gate contact dots on the sample.

Figure 4.4 shows the current density - voltage (J-V) characteristics of these c-Si/SiO_2/Al capacitors with different SiO_2 thicknesses. The J-V measurements were conducted using a Keithley 6430 Sub-FemtoAmp Source-Meter allowing very sensitive measurements down to a noise level of about $I = 5 \times 10^{-16}$ A. With decreasing oxide thickness the current density clearly increases. In general, for any dielectric film, the current transport behavior is normally controlled by one or two conduction mechanisms. Amongst others, the Fowler-Nordheim tunneling, Poole-Frenkel hopping, and trap-assisted tunneling are the main conduction mechanisms in MIS structures [Yan04, Sze07]. The strong thickness dependence of the current density observed for the MIS capacitors investigated here suggests that (trap-assisted) tunneling is the main contributor to the charge transport.

The effect of these leakage currents on the C/C_{ox}-V curves, which were measured in relaxation mode, as well as the corresponding relaxation ΔC-V can be seen in Fig. 4.5(a) and (b), respectively. For reference, the C/C_{ox}-V and ΔC-V curves of the 100 nm SiO_2 are also plotted. These are unaffected by leakage currents as evidenced by the negligible current densities in Fig 4.4. In the case of the 49 nm SiO_2, in the inversion region up to a negative gate voltage of -3.5 V, true inversion capacitances are obtained. This is verified by the relaxation reaching constant capacitances due to the generation/recombination of minority
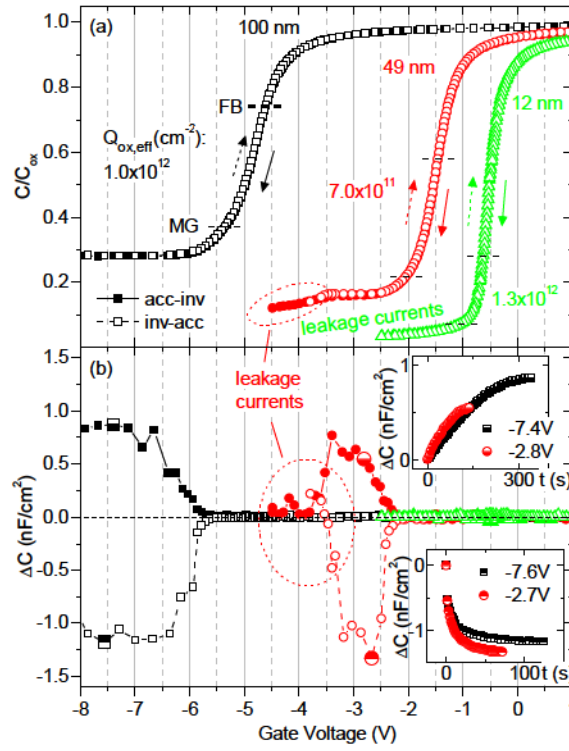
Figure 4.5: (a) High-frequency (1 MHz) normalized capacitance voltage (C/C$_{ox}$-V) curves in relaxation mode of MIS structures consisting of c-Si/SiO$_2$/Al with different oxide thicknesses d_{ox} = 100 nm, 49 nm and 12 nm. C-V measurements were performed in relaxation mode from accumulation to inversion (acc-inv) and vice versa (inv-acc). (b) Corresponding relaxation capacitance ΔC over gate voltage. Relaxations in the inversion region indicate if effects due to leakage currents need to be considered for the evaluation of the theoretical C-V curve. The inserted transients ΔC-t indicate completed relaxation processes at the given gate voltages. $Q_{ox,eff}$ is indicated upon correction of theoretical curves for 49 nm and 12 nm SiO$_2$.

charge carriers, as can be seen in the inserted ΔC-t transients at the corresponding gate voltages. At negative gate voltages larger than -3.5 V, leakage current densities $> 10^{-7}$ A/cm^2 start affecting the C/C$_{ox}$-V as well as the ΔC-V curve. In the C/C$_{ox}$-V curve the effect is reflected as a drop of capacitance indicating the formation of a deep depletion region. In the ΔC-V curve it is reflected in the decrease and disappearing of the relaxation capacitance which can be explained as follows: As the negative gate voltage is increased, the tunneling rate of the tunneling charge carriers increases as well. At a certain point (here $\sim$ -3.5 V) the tunneling rate exceeds the generation/recombination rate of minority charge carriers. The latter is thus suppressed, preventing the formation of an inversion region. This is then reflected as an absence of relaxation ΔC. In the case of the 12 nm SiO$_2$ the leakage current density exceeds 10^{-7} A/cm^2 by two orders of magnitude already in the inversion region. Consequently, no relaxations whatsoever are observed. In accumulation the effects due to leakage currents are minimal due to the relatively high

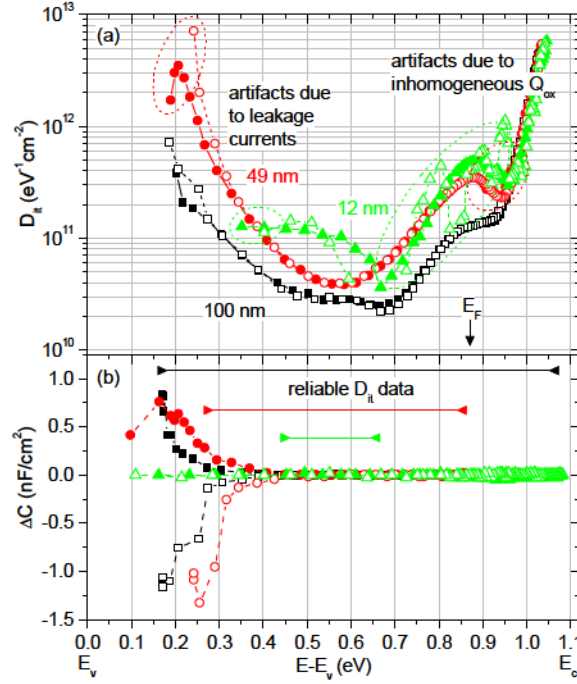Figure 4.6: (a) Defect state density (D_{it}) spectra of c-Si/SiO$_2$ interfaces with 100 nm, 49 nm and 12 nm SiO$_2$. Dashed circles mark D_{it}-data that is distorted either by leakage currents or inhomogeneities of charge density Q_{ox}. (b) Relaxation capacitance (ΔC) spectra. Energetic regions of reliable D_{it}-data are indicated.

majority charge carrier generation rate, which is apparently higher than the tunneling rate for the applied accumulation voltages. Due to the distorted inversion capacitances of both samples, 49 nm and 12 nm SiO$_2$, the iterative matching of the theoretical C-V curve for the evaluation of $Q_{ox,eff}$ and D_{it} would calculate a distorted N_A. Therefore, a correction of the theoretical C-V curve is required. In the case of the 49 nm SiO$_2$, the distorted C-values (for > 3.5 V) are taken out of the evaluation, resulting in $N_A = 1.2 \times 10^{15}$ cm^{-3}, similar to N_A obtained for the c-Si/SiO$_2$(100 nm) structure. In the case of the 12 nm SiO$_2$, the same N_A is used as input for the calculation of the theoretical curve. This results in $Q_{ox,eff} = 7 \times 10^{11}$ cm^{-2} for the 49 nm SiO$_2$, and $Q_{ox,eff} = 1.2 \times 10^{12}$ cm^{-2} for the 12 nm SiO$_2$.

The D_{it}-spectra resulting from these corrections and the corresponding ΔC-spectra are depicted in Fig. 4.6(a) and (b), respectively. The reference spectrum of the 100 nm SiO$_2$, which required no correction, is also plotted. The D_{it}-data below MG (i.e. inversion region) of the 49 nm and 12 nm SiO$_2$ that are affected by leakage currents is marked by dashed circles. At the Fermi level E$_F$ other artifacts arise. A clear peak is evident which does not reflect the true interface defect density but is rather an artifact due to an inhomogeneity of $Q_{ox,eff}$ [McN74, McN75]. In this case these inhomogeneities may be caused by the HF-etching creating locally fluctuating fixed charge densities, or by the leakage currents that influence the formation of the accumulation region and thus the slope of the C-V curve. In either case, these parts of the D_{it}-spectra are considered as not reliable and therefore are also marked by dashed circles. Based on these observations the energetic range of the

corresponding reliable D_{it}-data is marked in Fig. 4.6(b). An increase of D_{it} near MG is evident with decreasing oxide thickness. This may be a result of the HF-etching causing a degradation of the chemical passivation of the thermal oxide.

4.4 Comparison with effective lifetime measurements

In this section $Q_{ox,eff}$ and D_{it} of the c-Si/SiO$_2$ structures (100 nm, 49 nm and 12 nm SiO$_2$) obtained by C-V are qualitatively compared with the effective minority charge carrier lifetimes τ_{eff} measured via QSSPC. The lifetime measurements were performed on these same symmetrical samples prior to MIS-preparation for C-V measurements.
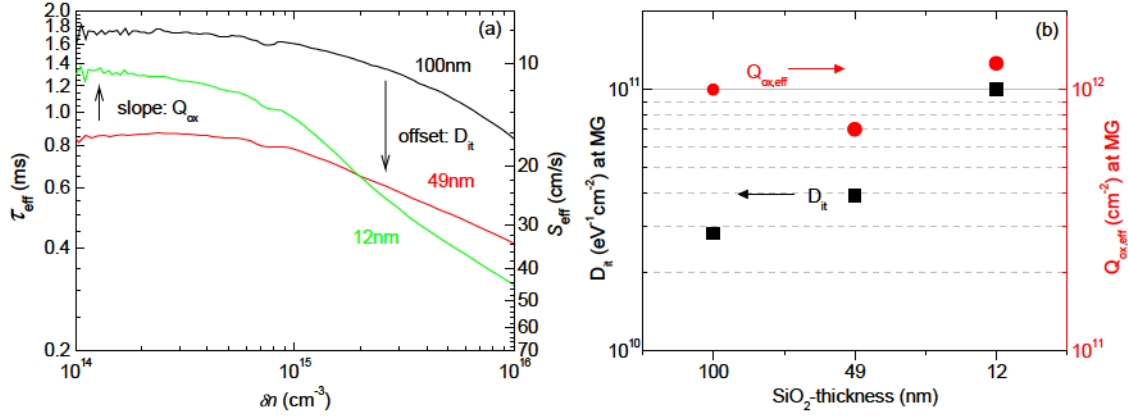

Figure 4.7: (a) Injection dependent effective minority charge carrier lifetimes τ_{eff} and surface recombination velocities S_{eff} of symmetric SiO$_2$/c-Si/SiO$_2$ structures obtained through QSSPC for comparison with (b) D_{it} and $Q_{ox,eff}$ of identical c-Si/SiO$_2$/Al MIS structures obtained through C-V measurements. Different SiO$_2$ thicknesses are indicated.

The measured τ_{eff} as a function of the injection level (δn) is depicted in Fig. 4.7(a). An upper bound of the effective surface recombination velocity (S_{eff}) at the injection level $\delta n = 10^{15} \, cm^{-3}$ is calculated assuming an infinite bulk lifetime: $S_{eff} = W/2 \cdot \tau_{eff}$, where W denotes the wafer thickness. In Fig. 4.7(b) $Q_{ox,eff}$ and D_{it} are depicted. Firstly, comparing the 100 nm with the 49 nm SiO$_2$ reveals a decrease of τ_{eff} , i.e. an increase of S_{eff}, at all injection levels. This deterioration of passivation correlates with the increase of D_{it} over the entire Si band gap as well as the decrease of $Q_{ox,eff}$. Secondly, comparing the 49 nm with the 12 nm SiO$_2$ reveals a deterioration of lifetime in the high injection region ($\delta n > 2 \cdot 10^{15} \, cm^{-3}$) and an improvement in the low injection region ($\delta n < 2 \cdot 10^{15} \, cm^{-3}$). This behavior also correlates qualitatively with $Q_{ox,eff}$ and D_{it}. On the one hand, in the high injection region the photo-generated excess charge carriers can compensate the fixed oxide charges responsible for the field-effect passivation [Lee11]. Thus, the chemical passivation dominates which leads to the reduced τ_{eff} due to the higher D_{it}. On the other hand, in the low injection region the field effect passivation dominates, which results in an enhancement of τ_{eff} due to the higher $Q_{ox,eff}$ of the 12 nm SiO$_2$. These qualitative correlations of τ_{eff} with $Q_{ox,eff}$ and D_{it} clarify the validity and reliability of the results obtained through C-V measurements regarding field-effect and chemical passivation.

4.5 Effects of charge trapping and charge redistribution in oxides

This section discusses the charge mechanisms that cause instabilities of $Q_{ox,eff}$ affecting the C-V curve and what information about the physical properties of the oxide (or insulator) can be obtained from their analysis. As already mentioned: (1) Changes of $Q_{ox,eff}$ lead to a parallel shift of the C-V curve along the voltage axis. (2) $Q_{ox,eff}$ is affected not only by changes of the total amount of charge Q_{ox} in the oxide, but also by redistribution of charges inside the oxide, if Q_{ox} is constant and electronic currents are negligible [Sno65].
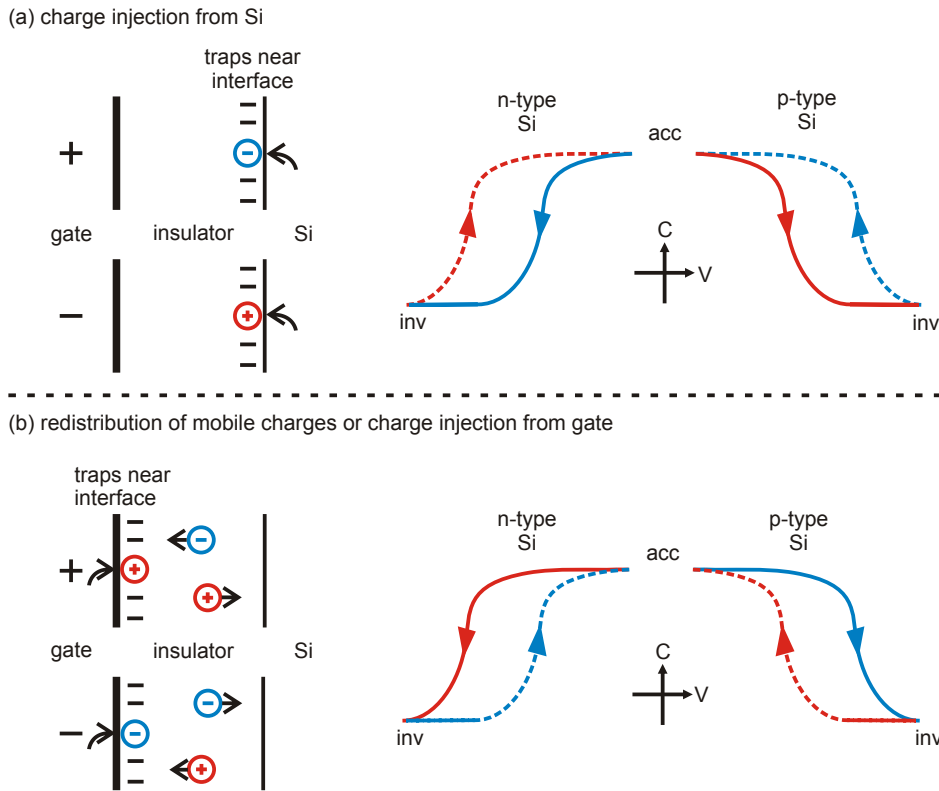
Figure 4.8: Charge mechanisms responsible for C-V hysteresis formation of a MIS capacitor due to (a) charge injection from the Si and (b) redistribution of charges or charge injection from the gate. The hysteresis formation occurs if $Q_{ox,eff}$ is affected when the C-V measurement is conducted in both directions, from accumulation (acc) to inversion (inv) and vice versa.

Fig. 4.8 illustrates different charge mechanism that influence $Q_{ox,eff}$ of an insulator on n-type or p-type c-Si. The thermal SiO_2 on n-type c-Si investigated in the previous sections revealed a stable $Q_{ox,eff}$ due to fixed positive charges. This is not the case for AlO_x-single layers and AlO_x/SiN_x stacks that were deposited on p-type c-Si and are investigated in the next chapter. Therefore, the following discussion about different charge mechanisms is focused on an insulator on p-type c-Si. The first charge mechanism is injection of charges from the c-Si into traps located near the Si/insulator interface, as depicted in Fig. 4.8(a). For instance, when two C-V curves are measured in both directions, i.e. from accumulation

to inversion (acc-inv) and from inversion to accumulation (inv-acc), charge injection leads to a counter-clockwise hysteresis formation for p-type c-Si. If the C-V measurement is started in accumulation, i.e. at a negative gate voltage for p-type c-Si, majority charge carriers (holes) are injected into trap levels located near the interface. This increases the positive component of $Q_{ox,eff}$ of the insulator. Therefore, the C-V curve is shifted towards negative voltages. When starting in inversion, i.e. at a positive gate voltage for p-type c-Si, minority charge carriers (electrons) are injected. Hence, the negative component of $Q_{ox,eff}$ increases and the C-V curve is shifted towards positive voltages. The resulting counter-clockwise orientation of the hysteresis for p-type c-Si is unambiguous for charge trapping near the c-Si/insulator interface [Sch06]. The effects for n-type are similar to the effects for p-type c-Si, but with inverted polarities.

As depicted in Fig. 4.8(b) an inversion of hysteresis orientation can occur when other charge mechanisms dominate, leading to a clockwise hysteresis formation p-type c-Si. When starting in accumulation (negative gate voltage), electrons can be injected from the gate into traps and/or negative mobile charges drift/tunnel towards the c-Si/insulator interface. This increases the negative component of $Q_{ox,eff}$. Therefore, the C-V curve is shifted towards positive voltages. When starting in inversion (positive gate voltage), holes can be injected from the gate into traps and/or positive charges drift/tunnel towards the c-Si/insulator interface. This increases the positive component of $Q_{ox,eff}$. Therefore, the C-V curve is shifted towards negative voltages. The resulting clockwise orientation of the hysteresis for p-type c-Si can therefore be attributed to gate injection and/or redistribution of charges. It is worth noting, however, that according to Eq. 4.8 trap charging near the insulator/gate interface has relatively little effect on $Q_{ox,eff}$. The effect becomes even less or negligible the closer the traps are located to the gate. Whereas charging mechanisms closer to the Si/insulator interface have a larger effect on $Q_{ox,eff}$.

Hysteresis formation due to redistribution of mobile charges can be attributed either to ion transport inside the dielectric, which occurs mainly at elevated temperatures (150 °C - 200 °C) [Sno65, Mit93, Sta06], or due to trap-assisted charge transport in the bulk, if electronic currents through the entire MIS structures are negligible [Sno65, Yan04]. If no C-V hysteresis is formed, this indicates the following: either no traps but only fixed charges are present, as it is the case for the investigated 100 nm thermal SiO_2. Or the trap density in the entire bulk dielectric material is high enough to cause leakage currents rather than charge trapping.

Which of these effects dominates and reveals itself in C-V hysteresis formation depends on the properties of the dielectric material, such as the trap density near/at the interfaces and in the bulk, if present. Therefore, through C-V hysteresis analysis the charging dynamics related to traps in dielectric materials can be studied.

4.6 Effects of slow charge trapping and detrapping

In this section the influence of (slow) trap charging mechanisms on the determination of D_{it} will be discussed. The investigated thermal SiO_2 reference did not reveal any traps. Therefore, for this purpose, an excerpt of the investigated AlO_x/SiN_x stacks on p-type c-Si presented in the next chapter, will be used as an example. In contrast to the thermal SiO_2 reference, these dielectric structures indeed exhibit trap densities that affect the C-V measurements. The following discussion focuses on the qualitative and quantitative effects of instabilities of $Q_{ox,eff}$ on the D_{it} analysis.
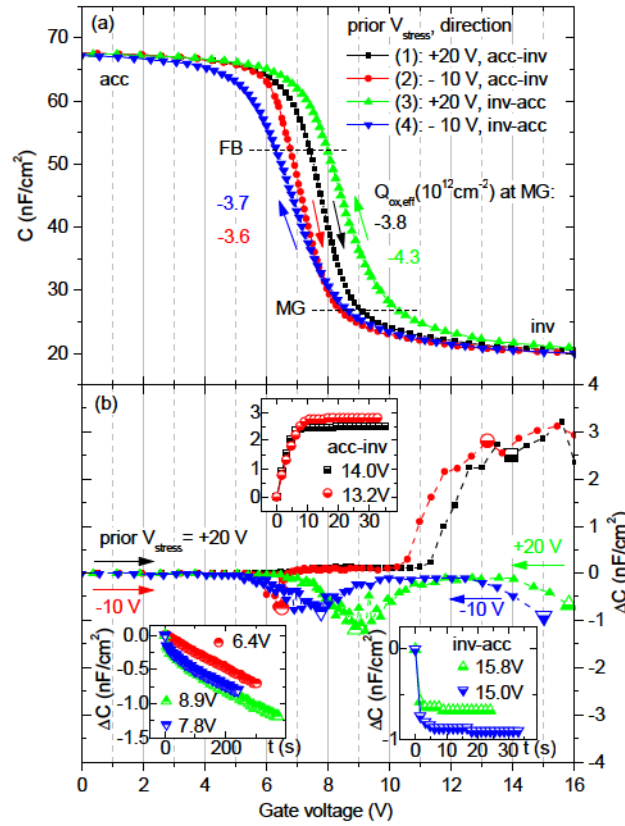
Figure 4.9: (a) High-frequency (1 MHz) capacitance voltage (C-V) curves obtained in relaxation mode of a MIS structure consisting of c-Si/AlO_x/SiN_x/Al upon a constant voltage stress V_{stress} applied for 500 s. (b) Corresponding relaxation capacitance ΔC vs. gate voltage. V_{stress} and C-V measurement direction (acc-inv or inv-acc) were varied (cases 1-4) in order to find parameters for charge stabilization and to study the charge dynamics. Charge trapping causes the parallel shift of C-V curve along the gate voltage axis indicating different $Q_{ox,eff}$. Charge stability is obtained through case (1): V_{stress}= +20 V (500 s) followed by a C-V measurement from accumulation to inversion.

In Fig. 4.9(a) high frequency C-V measurements in relaxation mode of a p-type c-Si/AlO_x/SiN_x structure are depicted. The corresponding relaxation capacitance ΔC-V is shown in Fig. 4.9(b). The resulting D_{it}-spectra are depicted in Fig. 4.10(a) and the
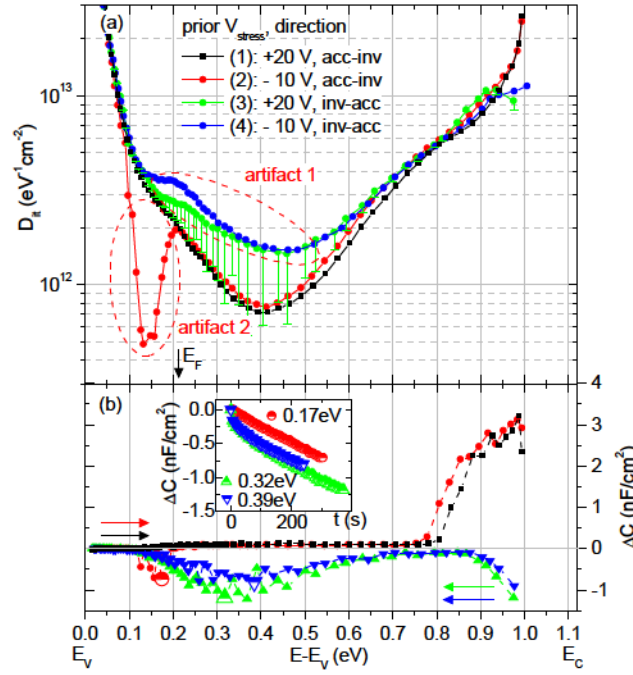
Figure 4.10: (a) Defect state density (D_{it}) spectra obtained from C-V on a c-Si/AlO$_x$/SiN$_x$ structure upon variation of prior V$_{stress}$ and C-V measurement direction. (b) Relaxation capacitance (ΔC) spectra. Artifacts in D_{it}-spectra resulting from instabilities of charges are marked. Estimated deviations of D_{it} due to these instabilities are indicated by error bars for case (3). Only case (1) with stable charges shows no artifacts which results in reliable D_{it}-data over the entire c-Si band gap.

corresponding ΔC-spectra can be found in Fig. 4.10(b). All measurements were performed on the same gate contact pad. In order to enhance the effect of charge trapping, a constant voltage stress (V$_{stress}$) of -10 V (strong accumulation), or +20 V (strong inversion), was applied for 500 s prior to the C-V measurements. During this time period, as described in Fig. 4.8(a), positive or negative charge injection from the c-Si occurred, respectively. Following each V$_{stress}$ a C-V measurement was performed, either in acc-inv or inv-acc direction (indicated by arrows in Fig. 4.9), resulting in four combination of V$_{stress}$ and measurement direction: (1) +20 V, acc-inv; (2) -10 V, acc-inv; (3) +20 V, inv-acc; (4) -10 V, inv-acc. In Fig. 4.10(b) all four cases indicate completed relaxation processes in the inversion region, as can be seen in the exemplary inserted ΔC-t traces at the given inversion gate voltages. Thus, no leakage currents need to be considered. Comparing cases (2) and (3) reveals the negative and positive charge trapping effect due to V$_{stress}$ = -10 V and +20 V, respectively, resulting in the shift of the C-V curves with a counter-clockwise hysteresis (Fig. 4.9(a)). In Fig. 4.10(b), (3) and (4) demonstrate considerable negative incomplete relaxations indicating discharges, as seen in the inserted ΔC-t traces at the gate voltages 8.9 V and 7.8 V. These discharges occur in the entire depletion and partially in the accumulation region, thus increasing the slope of the C-V curve. This leads to distorted

D_{it}-values between mid gap (MG) and the Fermi level (E_F) in the corresponding spectra in Fig. 4.10(a). These distorted D_{it}-values are marked and labeled as artifact 1. Therefore, in both cases (3) and (4), measuring from inversion to accumulation does not result in reliable D_{it}-spectra, independent of the prior V_{stress}. In case (2), no considerable relaxations occur in the depletion region, but rather in the accumulation region near flat band (FB) (Fig. 4.9(b)). The inserted ΔC-t trace at 6.4 V shows that the relaxation is negative. Since this C-V curve was measured from accumulation to inversion, this negative relaxation leads to an increase of the slope of the C-V curve in this gate voltage region. Therefore, the corresponding D_{it}-values energetically located below E_F are distorted, resulting in lower values which are marked as artifact 2. Finally, in case (1), no considerable relaxations are observed neither in accumulation nor in depletion, but only in inversion due to the generation of minority charge carriers. This relaxation behavior is nearly identical to the one of the thermal SiO_2 reference. Thus, it complies with the two main requirements for a reliable analysis of the passivation properties via C-V: It is insulating and $Q_{ox,eff}$ is in a stable charge state.

This evident correlation of relaxations ΔC and D_{it} allows one to make a correction of the distorted D_{it}-values caused by the instabilities of $Q_{ox,eff}$. For this purpose, cases (1) and (3) are considered, since both C-V curves were measured upon V_{stress} = +20 V, but in different directions. From direct comparison of their differences in relaxations $\Delta(\Delta C)$ and defect density ΔD_{it} it is estimated that

$$\Delta(\Delta C(E)) = 1 \ nF \ \widehat{=} \ \Delta D_{it}(E) = 0.9 \times 10^{12} \, eV^{-1} cm^{-2}.$$

A correction of the D_{it}-data of (3) through this estimation results in an approximation of the D_{it}-spectrum of (1), as visualized by the error bars in Fig. 4.10(b). In fact, this estimation was confirmed by similar V_{stress} and C-V experiments with other c-Si/AlO$_x$/SiN$_x$ structures. Therefore, it enables to give an error estimate, indicating a lower bound of the true D_{it}-spectra of structures that exhibit instabilities of $Q_{ox,eff}$ due to charge trapping. A more reliable characterization of the passivation properties is thus achieved.

4.7 Conclusions

In this chapter the main physical and mathematical aspects regarding the development of the high frequency (1 MHz) C-V method for MIS structures were presented. Using an insulating, c-Si/SiO$_2$ structure with stable oxide charge as a reference MIS system, the effects of leakage currents were studied. Through an analysis of the capacitance time (C-t) relaxation, the affected regions of the C-V curve and, thus, the corresponding distorted interface defect state density (D_{it}) can be identified. This allows the designation of reliable D_{it}-data reflecting the chemical passivation quality. Through these corrections, the results obtained through C-V measurements regarding field-effect and chemical passivation correlated qualitatively with results obtained from lifetime measurements. In addition, charge trapping phenomena in a c-Si/AlO$_x$/SiN$_x$ structure leading to charge instabilities were investigated through V$_{stress}$ biasing prior to C-V measurement in relaxation mode. Parameters for V$_{stress}$ and C-V measurements were found for the stabilization of charges. These results are crucial for a reliable determination of the charge density and the interface defect state density. They constitute the basis for the evaluation of the field-effect and chemical passivation properties of AlO$_x$-single layers, AlO$_x$/SiN$_x$ stacks and TiO$_2$:AuNP layers on c-Si in the next chapters.

5 PECVD-deposited AlO$_x$-single layers and AlO$_x$/SiN$_x$-stacks on c-Si

5.1 Introduction

For a successful integration of AlO$_x$ and AlO$_x$/SiN$_x$ based systems in different types of high efficiency solar cells, a thorough understanding of the passivation properties and the origin of the negative charge of these materials is necessary. The purpose of this chapter is to discern chemical and field-effect passivation properties and understand how the properties and the negative charge can be manipulated through different c-Si surface wet-chemical treatments and different thermal processes. Promising initial results reported in [Laa12] in the framework of this thesis and the very limited number of publications concerning detailed C-V analysis for these structures motivated the further development of the high frequency C-V method that would allow more detailed and reliable evaluations of Q_{ox} and D_{it} in the framework of this thesis.

The growth of all-PECVD-deposited single AlO$_x$ layers and AlO$_x$/SiN$_x$ stacks on p-type c-Si with differently preconditioned surfaces was performed at CiS Erfurt in collaboration with HZB and Roth&Rau AG. The layers and structures studied here underwent several prior optimization steps in regard to their thickness and post-deposition treatments. In addition, the effects of a wide range of wet-chemical c-Si surface treatments on the passivation quality were studied [Laa12]. See Tab. 5.1 for an excerpt of these treatments. The evaluation of their passivation properties were based primarily on minority charge carrier lifetime measurements via quasi steady state photoconductance (QSSPC), supported by surface photo voltage (SPV), capacitance voltage (C-V), and Fourier transform infrared

Process	label	Process mixture
Radio corporation of America	RCA	SC1 + HF + SC2 + HF
Hydrofluoric acid dip	HF-Last	HF(2%)/H$_2$O (60 s, 25 °C)
Hot deionized water and HCl	Hot-DiW80:HCl	Hot-DiW/HCl (1:1000): 80°C

Tab. 5.1: Wet chemical processes applied to silicon wafer surfaces prior to AlO$_x$-single or AlO$_x$/SiN$_x$-stack deposition. The process step labeled Hot-Diw80:HCl leads to wet chemical oxide (SiO$_x$) growth of 1.0 - 1.5 nm thickness. It was applied after either just HF or RCA+HF. SC1 and SC2 are standard cleaning processes consisting of NH$_4$OH/H$_2$O$_2$/H$_2$O (75°C) and HCl/ H$_2$O$_2$/H$_2$O (75°C), respectively.
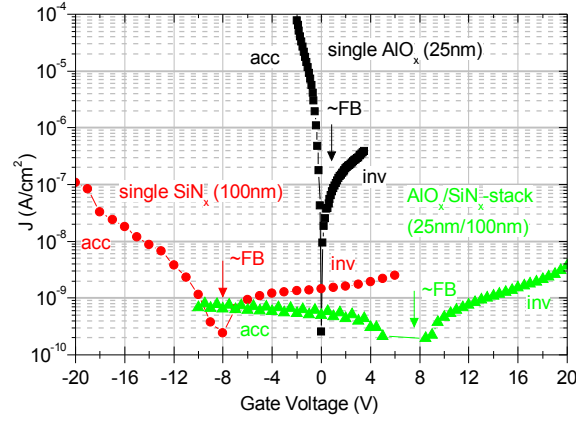
Figure 5.1: Current density - voltage measurement of MIS structures consisting of c-Si/AlO$_x$(25 nm)/Al, c-Si/SiN$_x$(100 nm)/Al and c-Si/AlO$_x$(25 nm)/SiN$_x$(100 nm)/Al. Accumulation (acc) and inversion (inv) regions as well as approximate flat band (FB) regions are indicated for each structure.

spectroscopy (FTIR) measurements [Laa12]. The C-V measurements were performed in the framework of this thesis. It was demonstrated that improved interface properties in terms of a low interface defect state density $D_{it}(E)$ can be obtained already immediately after surface preconditioning which results in a H-terminated surface (e.g., by means of RCA-cleaning and HF-etching) or an interface with an ultrathin oxide of high quality. The latter is obtained by a mixture of hot (80 °C) deionized water (DiW) with a small amount of hydrochloridric acid (HCl), referred to as Hot-DiW80:HCl. These process steps were monitored by the SPV technique. It was demonstrated via FTIR that after deposition of single AlO$_x$ layers an improvement of the interface is obtained in terms of an increase of the Si-O-Si bond density upon thermal steps. The second contribution is assigned to the formation of a negative charge observed via C-V measurements. Its origin could be identified to be partly due to the increase of the density of negatively charged AlO$_4$ tetrahedra at the SiO$_x$/AlO$_x$ interface upon thermal steps, as confirmed by FTIR. It was thus demonstrated that wet-chemical oxides compatible with low manufacturing costs can be used to improve the passivation quality of PECVD deposited AlO$_x$/SiN$_x$ stacks.

These preceding experiments proved the high frequency (1 MHz) C-V method (see chapter 4) to be a powerful tool for the evaluation of the field-effect (i.e. Q_{ox}) and chemical passivation (i.e. D_{it}) in regard to c-Si surface and thermal treatments. However, as a new material system, the AlO$_x$-single layers and AlO$_x$/SiN$_x$ stacks on c-Si revealed new challenges in regard to obtaining reliable C-V data. In contrast to thermal SiO$_2$(100 nm), which is insulating and stable in regard to its charge (see chapter 4.2), the AlO$_x$-single layers (25 nm) exhibited leakage current densities, as depicted in Fig. 5.1, which were large enough to influence the capacitance measurement in accumulation and inversion. The AlO$_x$/SiN$_x$ stacks exhibited leakage current densities lower by several orders of magnitude, allowing more reliable C-V measurements. For the SiN$_x$ layer (100 nm), Fig. 5.1 demonstrates negligible current densities indicating an insulating character. In addition, the AlO$_x$-

single layers and in particular the AlO_x/SiN_x stacks exhibited temporal as well as voltage dependent instabilities in their effective charge $Q_{ox,eff}$, hence, influencing and distorting the measured D_{it} (see section 4.6). Therefore, only an excerpt of the first C-V measurements that were considered reliable was presented in Ref. [Laa12].

The following studies aim at a better understanding of the passivation properties of the single AlO_x layers and in particular of the AlO_x/SiN_x stacks on p-type c-Si, as observed in the lifetime measurements. To achieve this, lifetime measurements via QSSPC are compared with results regarding $Q_{ox,eff}$ and D_{it} obtained through high frequency (1 MHz) C-V combined with capacitance time (C-t) measurements. A detailed analysis of charging mechanisms was performed including trapping-detrapping phenomena in the AlO_x/SiN_x-system and of the c-Si/AlO_x interface defect generation which have great impact on the field-effect and chemical passivation, respectively. It is worth noting that in regard to the AlO_x/SiN_x stacks all results presented in the following sections were obtained from measurements on gate contact dots where the underlying SiN_x revealed highly insulating properties preventing (or minimizing) charge injection from the gate into the AlO_x. The purpose of this was to create conditions more likely to play a role when integrating the stack into a solar cell structure, where charge injection from the c-Si is much more likely to occur than from a source on the capping SiN_x. However, a build-up of an electrical potential across the structure may indeed occur and can affect the performance of the solar cell. This effect is related to the "potential-induced degradation" (PID) [Bau12, Hac11, Pin10], which is currently of highest interest in the photovoltaic community. In order to investigate the effects of large potentials on the passivation properties, but also to examine trapping and detrapping phenomena in the AlO_x/SiN_x stacks, constant gate voltage stresses (V_{stress}) were applied within a V_{stress}-range where the SiN_x kept its insulating property. Through V_{stress}-dependent C-V hysteresis formation and C-t transient analysis the dominant charge contributions due to trapping in the AlO_x/SiN_x-system can be distinguished. In addition, the defect state density at the c-Si/AlO_x interface over the entire c-Si band gap is monitored as well as the effect of a wet-chemically introduced SiO_x interlayer. In addition, the effects of a large V_{stress} on the chemical passivation in regard to intrinsic Si dangling bond defects are investigated. These studies are of interest for understanding the interface properties and charge trapping mechanisms of c-Si/(SiO_x)/AlO_x/SiN_x structures. The investigations related to voltage stress induced degradation are also of interest in regard to the implementation of such PECVD-AlO_x/SiN_x passivation stacks in c-Si solar cells or other devices where degradation of passivation will influence their performance.

5.2   Lifetime measurements of c-Si passivated by AlO$_x$-single layers and AlO$_x$/SiN$_x$ stacks

For the purpose of more detailed and reliable evaluations of Q$_{ox}$ and D$_{it}$ in the framework of this thesis, two new sets of samples were prepared: One consisting of AlO$_x$-single layers and one of AlO$_x$/SiN$_x$ stacks deposited on different wet-chemically pretreated c-Si surfaces.
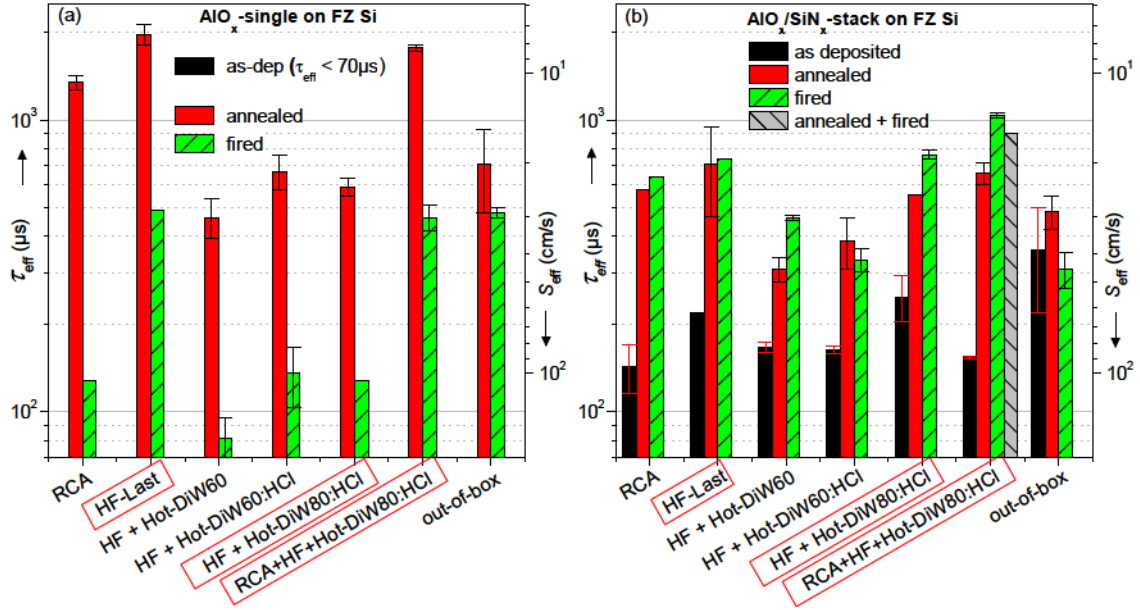
Figure 5.2: Influence of different wet chemical surface treatments (Tab. 5.1) on the passivation quality (in terms of τ_{eff} and S_{eff} at $\delta n = 10^{15}\, cm^{-3}$) of silicon surfaces covered by PECVD-deposited AlO$_x$-single layers (a) and AlO$_x$/SiN$_x$ stacks (b) in the as deposited, annealed and fired state. One sample was subjected to annealing and firing (gray). Samples selected for C-V measurements are marked by a red box. These measurements were performed at CiS Erfurt and verified at HZB.

As a first step to evaluate the passivation quality, effective minority charge lifetime (τ_{eff}) measurements were performed via QSSPC in CiS Erfurt. From the measured τ_{eff} as a function of the injection level (δn), an upper bound of the effective surface recombination velocity (S_{eff}) at the injection level $\delta n = 10^{15}\, cm^{-3}$ is quantified assuming an infinite bulk lifetime: $S_{eff} = W/2 \cdot \tau_{eff}$, where W denotes the wafer thickness. The measured τ_{eff} and the corresponding S_{eff} at an excess charge carrier concentration $\delta n = 10^{15}\, cm^{-3}$ for p-type c-Si passivated by AlO$_x$-single layers and by AlO$_x$/SiN$_x$ stacks are depicted in Fig. 5.2(a) and (b), respectively. In Fig. 5.2(a), c-Si covered by as deposited AlO$_x$-single layers reveal relatively low lifetimes of $\tau_{eff} < 70$ µs for all c-Si surface treatments. This low passivation quality is typical for as deposited AlO$_x$ layers where the field-effect and chemical passivation are not yet activated [Din10]. Upon an industrial firing process (860 °C, ~3 s in air) the passivation improves, i.e. τ_{eff} increases. Yet, τ_{eff} remains below ~500 µs. This demonstrates

that the firing process does not fully activate the AlO$_x$ surface passivation [Din09]. A high passivation quality (i.e. highest τ_{eff}, lowest S_{eff}) is obtained after annealing (425 °C, 15 min in air) the samples, in particular for the AlO$_x$-single layers on a c-Si surface treated with RCA, HF-Last or RCA+HF+HotDiw80:HCl (see. Tab. 5.1).

The activation of the field effect and the chemical passivation upon annealing has been thoroughly investigated in the literature [Din12b, Ben09, Ben10, Bor11, Din09, Din10, Iri11, Kat07]: Post-deposition annealing increases the negative Q_{ox} and lowers D_{it} of the c-Si/(SiO$_x$) /AlO$_x$ system resulting in a significant improvement of the level of surface passivation. The formation of an ultrathin interfacial SiO$_x$ film between the c-Si and the AlO$_x$ plays a key role in both, the origin of the negative Q_{ox} and the interface defect state density D_{it}. A negative Q_{ox} in combination with a sufficiently low interface defect density is routinely reported for annealed AlO$_x$ films deposited on c-Si [Joh01, Hoe08a, Hoe08b], irrespective of the deposition technique.

In any case, the prior wet-chemical treatment of the c-Si surface clearly has a considerable impact on the resulting passivation quality of the annealed samples. Hence, for a more detailed analysis, the annealed samples consisting of AlO$_x$-single layers on c-Si surfaces treated with HF-Last, with HF+Hot-DiW80:HCl and with RCA+HF+Hot-DiW80:HCl were selected together with their AlO$_x$/SiN$_x$ stack counterparts. Their effective minority charge carrier lifetime τ_{eff} as a function of the excess charge carrier concentration δn of these selected samples are depicted in Fig. 5.3(a) and (b), respectively. These lifetime measurements were performed at HZB.

These structures will be subject to a detailed study via C-V in respect of their passivation properties in this chapter. The selection is based on the following observations in the lifetime measurements:

HF-Last:

>A slightly higher passivation quality was obtained for AlO$_x$-single layers and AlO$_x$/SiN$_x$ stacks deposited on H-terminated c-Si than on RCA-cleaned Si. Therefore, these samples were chosen as reference structures.

HF+Hot-DiW80:HCl:

>The purpose of studying these samples is to evaluate the effect of the wet-chemical SiO$_x$ interlayer on the passivation properties through comparison with the reference (HF-Last) sample.

RCA+HF+Hot-DiW80:HCl:

>Applying the RCA-cleaning prior to the HF+Hot-DiW80:HCl treatment results in the highest lifetimes τ_{eff}. Consequently, these samples were chosen in order to investigate the effect of the RCA-cleaning through comparison with HF+Hot-DiW80:HCl.
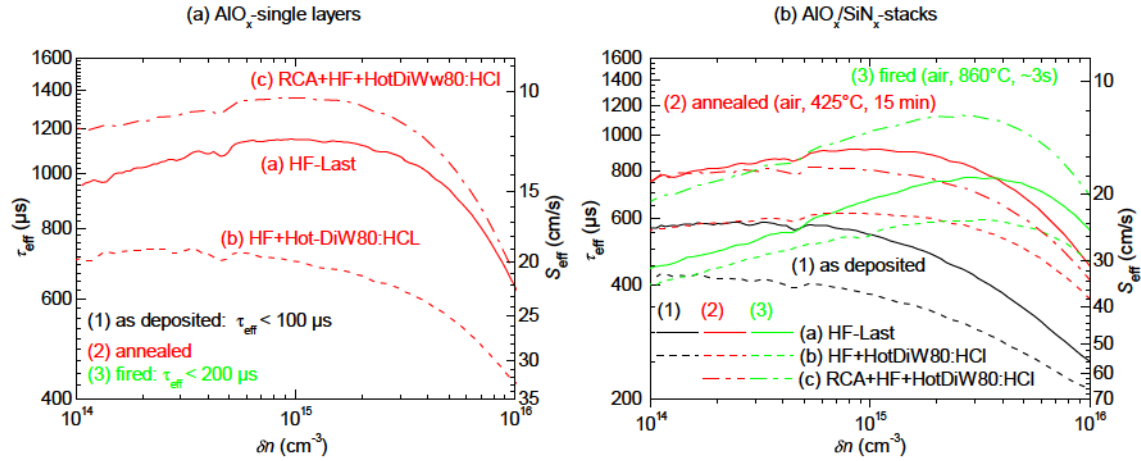
Figure 5.3: Injection dependent minority charge carrier lifetimes of p-type c-Si with different surface treatments and passivated by PECVD-AlO$_x$-single layers (a) and -AlO$_x$/SiN$_x$ stacks (b). Different thermal treatments where applied: as deposited, annealed and fired.

It should be noted that when comparing the lifetime measurements at HZB (Fig. 5.3) with those at CiS Erfurt (Fig. 5.2), a reduction of τ_{eff} (at $\delta n = 10^{15}\,cm^{-2}$) is evident for the annealed and fired AlO$_x$-single layers. The passivation properties of the AlO$_x$-single layers thus seem to have degraded over time (1 - 2 months). However, τ_{eff} of the c-Si passivated by AlO$_x$/SiN$_x$ stacks remained rather stable, possibly due to the protective SiN$_x$ capping layer.

The second set of samples, consisting of c-Si passivated by AlO$_x$ capped with SiN$_x$, reveals several different passivation properties concerning the effect of the thermal treatments (Fig. 5.3(b)), in comparison to the AlO$_x$-single layers:

(i) c-Si covered by as deposited AlO$_x$/SiN$_x$ stacks already exhibits moderate passivation properties with τ_{eff} = 400 - 600 µs. This is due to the thermal budget during SiN$_x$ deposition (350 - 450 °C) that activates the surface passivation induced by AlO$_x$ [Din09].

(ii) Annealing further improves passivation quality leading to τ_{eff} = 600 - 800 µs.

(iii) In contrast to c-Si passivated by AlO$_x$-single layers, direct firing of the c-Si passivated by the AlO$_x$/SiN$_x$-stack astonishingly leads to passivation properties of similar or even higher quality as annealed ones, depending on the c-Si surface treatment.

Introducing a wet-chemical SiO$_x$ interlayer after an HF treatment (HF+Hot-DiW80:HCl), seems to lower the passivation quality in comparison to HF treatment only, regardless of the thermal treatment. This effect can be observed for the c-Si passivated with AlO$_x$-single layers as well as AlO$_x$/SiN$_x$ stacks (Fig. 5.3). However, performing an RCA cleaning prior to HF+Hot-DiW80:HCl and a subsequent firing leads to the highest passivation quality.

5.3 Annealed AlO$_x$-single layers on c-Si: Effects of c-Si surface preconditioning

The passivation properties of annealed AlO$_x$-single layers on different c-Si surfaces were first investigated by τ_{eff} measurements via QSSPC (Fig. 5.3(a)). In this section, for a more detailed analysis, C-V investigations of $Q_{ox,eff}$ and D_{it} are presented, which are a measure for the field-effect and chemical passivation, respectively. As described in section 4.2, $Q_{ox,eff}$ and D_{it} are obtained through a comparison of the experimental C-V curve with the corresponding theoretical one (for $Q_{ox,eff} = 0$ and $D_{it} = 0$). The theoretical C-V curve (C_{th}) is a function of the oxide capacitance (C_{ox}) and the effective wafer doping concentration (N_A), which normally are obtained through iterative matching of the slope of the theoretical C-V curve to the experimental one in the accumulation (C_{acc}) and inversion (C_{inv}) capacitance regions. Consequently, if the experimental C_{acc} and C_{inv} are distorted, in particular due to leakage currents, the resulting theoretical curve is falsified. And indeed, the AlO$_x$-single layers (25 nm) reveal high enough leakage current densities which cause such distortions (Fig. 5.1). For the theoretical curve in this case, the input parameter $C_{ox} = \epsilon_{AlOx}\epsilon_0/d_{ox} = 318.7\,nF/cm^2$ is thus calculated using the AlO$_x$ thickness of $d_{ox} = 25$ nm, the vacuum permittivity $\epsilon_0 = 8.8542 \times 10^{-14}\,F/cm$ and the dielectric constant of AlO$_x$ $\epsilon_{AlOx} = 9$ in accordance with Ref. [Wil01]. A doping concentration of $N_A = 4,6 \times 10^{15}\,cm^{-3}$ is assumed, which is obtained from C-V measurements of c-Si/AlO$_x$/SiN$_x$ stacks (shown later) where a true inversion capacitance is reached due to negligible leakage currents. This value agrees very well with the given wafer resistivity of 1-5 Ωcm.

Fig. 5.4(a) illustrates the resulting calculated theoretical C-V curve (C_{th}) as well as the measured experimental C-V curves of the AlO$_x$-single layers on different c-Si surfaces. The C-V curves were measured in both directions: from accumulation to inversion (acc-inv, closed symbols) and vice versa (inv-acc, open symbols), including relaxation analysis. The latter means that at each applied gate voltage the C-t trace was monitored until a constant C-value was measured during a time interval of 15 s. Fig. 5.4(b) depicts the relaxation (or change) ΔC of the capacitance for each C-t trace over the gate voltage. It significantly differs from the relaxation behavior observed for insulating, stable thermal SiO$_2$ (see section 4.2, Fig. 4.2) which serves as a reference. By comparing both behaviors, the effects of the leakage currents as well as of $Q_{ox,eff}$ instabilities on the measured capacitance can be identified and evaluated:

1. For instance, in Fig. 5.4(a) the accumulation capacitance (C$_{acc}$) is below the theoretical $C_{ox} = 318.7$ nF/cm^2 when compared to the calculated theoretical C-V curve (C$_{th}$). This is due to the fact that leakage currents with high tunneling rates prevent the formation of an accumulation region in the c-Si which is reflected in C$_{acc}$ [Yan99, Yan04].

2. Fig. 5.4(b) shows, between flat band (FB) and weak accumulation, that positive
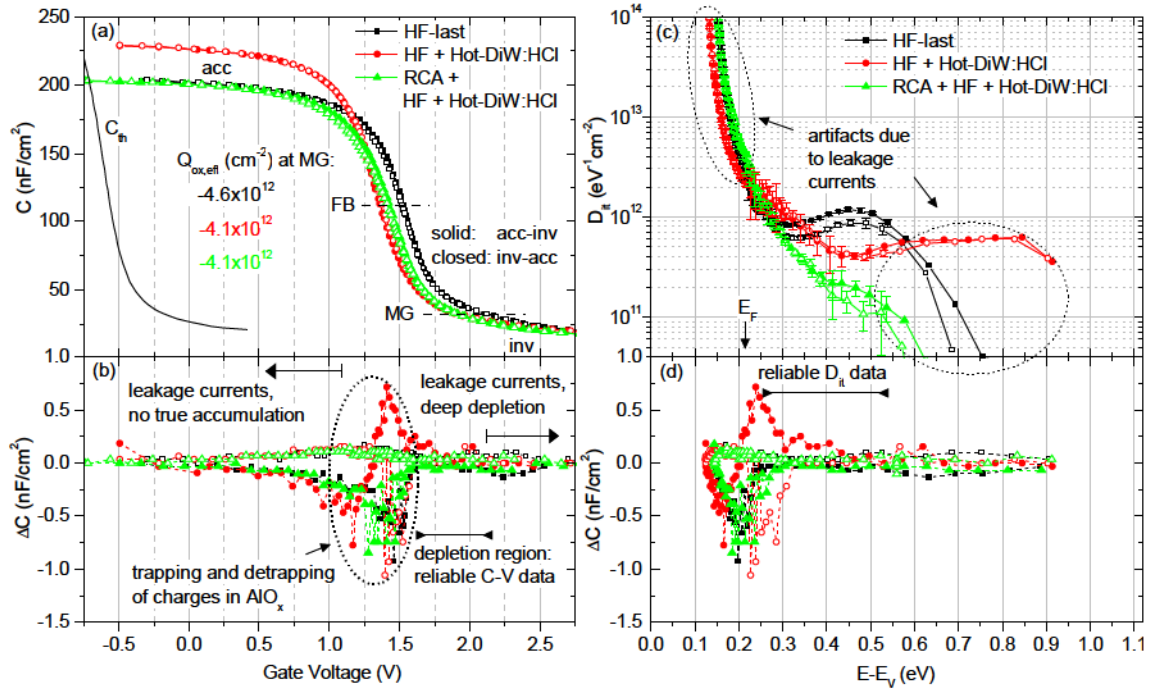
Figure 5.4: (a) High-frequency (1 MHz) capacitance voltage curves of c-Si/AlO_x/Al MOS-structures with different c-Si surface preconditioning measured in relaxation mode. Corresponding corrected theoretical curve (C_{th}) as well as flat band (FB) and mid gap (MG) voltages are depicted. (b) Relaxation of capacitance ΔC vs. gate voltage. Effects of leakage currents and trapping are analyzed. (c) Corresponding calculated c-Si/AlO_x interface defect state density (D_{it}) spectra in relation to the c-Si valence band energy (E_v). Artifacts due to leakage currents are indicated. (d) Relaxation of capacitance ΔC over c-Si band gap energy. Energetic region of reliable D_{it} data is indicated.

and/or negative relaxations ΔC arise depending on the measurement direction, and also on the c-Si surface preparation. These relaxations may be attributed to trapping/detrapping of charges and/or charge redistribution in the AlO_x. Due to a nearly absent and not distinctly identifiable hysteresis formation in the C-V curves as well as possible effects due to the leakage currents, theses relaxations can at this point not be clearly assigned to specific physical effects. However, they reveal slight instabilities in $Q_{ox,eff}$ and therefore will need to be considered in the analysis of D_{it}.

3. The effects of leakage currents on the capacitance in the inversion region are discussed in section 4.3. The absence of relaxations in the inversion region shown in Fig. 5.4(b) reveals that no true inversion capacitance is obtained for the C-V curves in Fig. 5.4(a) due to the leakage currents. The latter prevent the accumulation of minority charge carriers and, hence, the formation of an inversion layer. Consequently, the system goes into a deep depletion state instead.

4. In the depletion region between flat band (FB) and mid gap (MG), where the local

electric field near the c-Si/AlO$_x$ interface is minimal, the effects due to leakage currents are minimal as well. This is reflected in the relaxation analysis in Fig. 5.4(b), where in the depletion region almost no relaxations are observed, similar to the thermal SiO$_2$ reference.

Accordingly, the effects mentioned above leave a window in the C-V curves in the depletion region, which in conjunction with the corrected theoretical curve may result in a reliable analysis of $Q_{ox,eff}$ and D_{it}. For the evaluation of $Q_{ox,eff}$ the leakage currents can be of advantage: The negligible hysteresis formation for all samples reveals that the contribution of charge trapping and detrapping in the AlO$_x$ bulk or near the c-Si/AlO$_x$ interface is also negligible and therefore has a negligible effect on $Q_{ox,eff}$. The leakage currents prevent the stable trapping of charges. Therefore, it can be concluded, that the shift of the FB and MG towards positive voltages is attributed mainly to fixed charges which dominate in the contribution to $Q_{ox,eff}$. The attained fixed oxide charges $Q_{ox,eff}$ at MG for the AlO$_x$-single layers are illustrated in Fig. 5.4(a). AlO$_x$ deposited on HF-last c-Si surface reveals the highest negative fixed charge density with $Q_{ox,eff} = -4.6 \times 10^{12}\,cm^{-2}$. In comparison, AlO$_x$ deposited on a c-Si surface treated with HF+Hot-DiW80:HCl and RCA+HF+Hot-DiW80:HCl both reveal lower negative charge densities of $Q_{ox,eff} = -4.1 \times 10^{12}\,cm^{-2}$. These lower fixed charge densities are most likely due to the interfacial wet-chemical SiO$_x$, which slightly reduces the negative $Q_{ox,eff}$ by small positive charges [?].

Fig. 5.4(c) illustrates the interface defect state density (D_{it}) in the c-Si band gap obtained by comparing the experimental C-V curves to the calculated theoretical one in 5.4(a). The corresponding relaxations ΔC are plotted in Fig. 5.4(d). They serve as an orientation for localizing the effects on D_{it} explained by leakage current and for an estimation of the error ΔD_{it}. The D_{it}-values which are distorted due to the leakage currents are marked by black circles: One at the valence band tail, due to the distorted C$_{acc}$, the other in the upper part above MG in the c-Si band gap, due to the distorted C$_{inv}$. The D_{it}-values located between the Fermi-level (E_F) and MG reflect the slope of the C-V values in the depletion region. Therefore, they can be considered as reliable. Here, the effect of the c-Si surface treatment on D_{it} prior to the AlO$_x$ deposition is clearly visible: The HF-Last c-Si/AlO$_x$ interface reveals the highest defect density of $\sim 1 \times 10^{12}\,eV^{-1}cm^{-2}$ just below MG at E - E_v= 0.5 eV, before it gets distorted because of leakage currents. Applying the HF+Hot-DiW80:HCl treatment reduces D_{it} by a factor of 2 down to $\sim 5 \times 10^{11}\,eV^{-1}cm^{-2}$. The lower D_{it} value can be attributed to the better chemical passivation by the wet-chemical SiO$_x$ interlayer and it correlates with D_{it} measurements via SPV of the treated surface before AlO$_x$ deposition [Laa12]. Performing an RCA-cleaning prior to HF+Hot-DiW80:HCl reduces the defect density even further, down to $\sim 2 \times 10^{11}\,eV^{-1}cm^{-2}$, albeit with an increasing relative error. The reduction of defect states is most probably due to the removal of organic and metallic contaminants from the surface prior to the HF treatment and wet-chemical oxidation. This trend was also observed via the SPV measurements in Ref. [Laa12], therefore it can be concluded that the performed correction of the theoretical C-V curve indeed leads to a
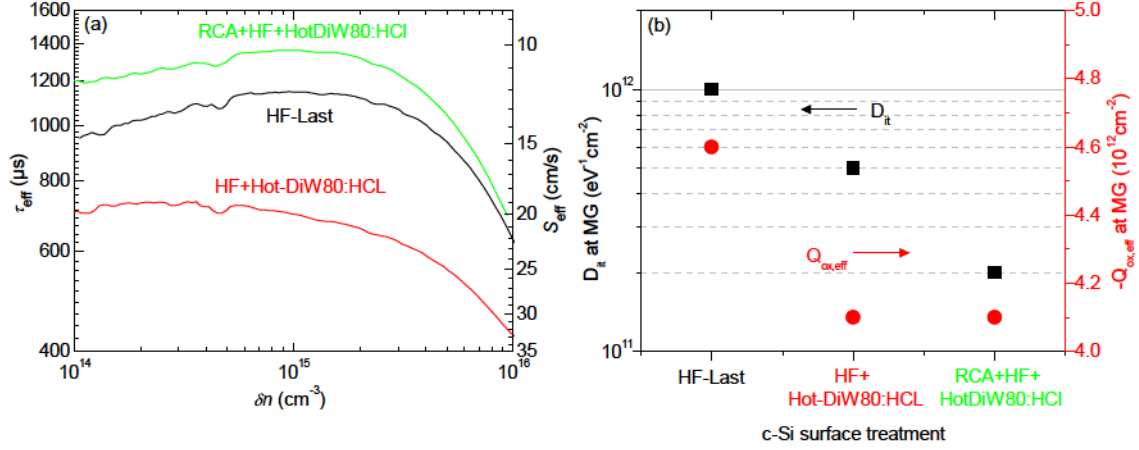
Figure 5.5: Effects of c-Si surface preconditioning on passivation properties of annealed AlO$_x$-single layers: (a) Injection dependent effective minority charge carrier lifetimes τ_{eff} and surface recombination velocities S_{eff} obtained through QSSPC for comparison with (b) D_{it} and $Q_{ox,eff}$ obtained through C-V measurements.

reliable interface evaluation of D_{it} between FB and MG .

Fig. 5.5 compares τ_{eff} and S_{eff} obtained through QSSPC (a) with D_{it} and $Q_{ox,eff}$ obtained through C-V measurements (b). In Fig. 5.5(a) it can be observed that introducing a wet-chemical SiO$_x$ interlayer reduces the passivation quality of the annealed AlO$_x$ on a HF treated c-Si surface: τ_{eff} at $\delta n = 10^{15}\,cm^{-3}$ for HF-last decreases from 1150 µs to 700 µs for HF+Hot-DiW80:HCl, thus, S_{eff} increases from 12 cm/s to 20 cm/s. Similar observations were presented in Ref. [Bor11]. However, this effect seems to contradict the results obtained through C-V (Fig. 5.5(a)), where the wet-chemical SiO$_x$ interlayer leads to a reduction of D_{it} by a factor of 2, but also to a slight reduction of $Q_{ox,eff}$. For the given wafer doping concentration, simulations reveal that $S_{eff} \sim 1/Q_{ox}^2$ for $Q_{ox} > 10^{11}$ cm^{-2} [Hoe08a, Din12b], while S_{eff} is observed to decrease linearly with a reduction in N_{it} (i.e. also in D_{it}) according to Eq. 2.5. Nevertheless, it is unlikely that this rather small reduction of $Q_{ox,eff}$ (by ~10 %) would have greater effect on the reduction (increase) of τ_{eff} (of S_{eff}) than the reduction of D_{it} (by ~50 %). Therefore, for a more consistent comparison between the two methods, other effects, which cannot be detected by the C-V method but do affect τ_{eff} have to be taken into consideration. These are: variations of τ_{bulk} (e.g. due to c-Si bulk contamination) or more probable local inhomogeneities of D_{it} and Q_{ox}. Additionally, Q_{ox} may be influenced by trapping/detrapping of charge carriers in defect states in the AlO$_x$ bulk. This may occur either by photon-induced charge injection [Gie08], which in principle may come about during a QSSPC measurement, or by potential (voltage) -induced charge trapping [Gon13b, Suh13] from the c-Si. The effect of charge trapping was not clearly observed in these C-V measurements due to the high leakage currents in the AlO$_x$. This means that charges injected from the c-Si (or gate) into the AlO$_x$ dominantly traveled through trap-assisted transport to the gate (or Si). However, the C-t relaxations are most likely related to this effect which will play a crucial role in

the following sections were the AlO$_x$ is capped by an insulating SiN$_x$ layer. In regard to the RCA+HF+Hot-DiW80:HCl treatment a more consistent correlation between τ_{eff} (or S_{eff}) in Fig. 5.5(a) and D_{it} and $Q_{ox,eff}$ in Fig. 5.5(b) can be observed: The best passivation quality in this set of AlO$_x$-single layers on c-Si is achieved through a reduction of the interface defect state density down to $D_{it} \sim 2 \times 10^{11}\,\mathrm{eV}^{-1}cm^{-2}$ near MG, by combining RCA-cleaning with a wet-chemical SiO$_x$ interlayer, and the field-effect passivation induced by the negative $Q_{ox,eff} = -4.1 \times 10^{12}\,cm^{-2}$, activated by post-annealing.

In summary, the AlO$_x$ single layers deposited on differently treated c-Si surfaces provide a high quality passivation upon annealing. This is the case in particular when the c-Si surface was RCA-cleaned, HF-treated and wet-chemically oxidized (Hot-DiW80:HCl) prior to AlO$_x$ deposition. The latter lead to $\tau_{eff} = 1.3\,\mathrm{ms}$ and $S_{eff} = 10.1\,\mathrm{cm/s}$ at $\delta n = 10^{15}\,cm^{-3}$. The C-V analysis in this work revealed a high negative fixed charge ($Q_{ox,eff} = -4.1 \times 10^{12}\,cm^{-2}$) combined with a low interface defect state density ($D_{it} \sim 2 \times 10^{11}\,\mathrm{eV}^{-1}cm^{-2}$ near MG) to be the origin of the enhanced field-effect and the chemical passivation, respectively. This identification was possible because of a systematically corrected analysis of the influence of leakage currents, allowing to distinguish reliable from falsified C-V data. In fact, it can be concluded that these corrections, which were developed in the framework of this thesis, specifically helped to identify the contribution of the fixed negative charges, since the leakage currents minimize the contribution owing to charge trapping. This is an important observation in view of the evaluation of $Q_{ox,eff}$ of the AlO$_x$/SiN$_x$ stacks in the following sections, because here the interplay between fixed charges and charge trapping will play a crucial role.

5.4 As deposited AlO$_x$/SiN$_x$ stacks on H-Last c-Si: Effects of annealing

In this section the passivation properties of AlO$_x$/SiN$_x$ stacks deposited on HF-Last c-Si are investigated in the as deposited state and compared to the state after annealing (air, 425°C, 15 min).
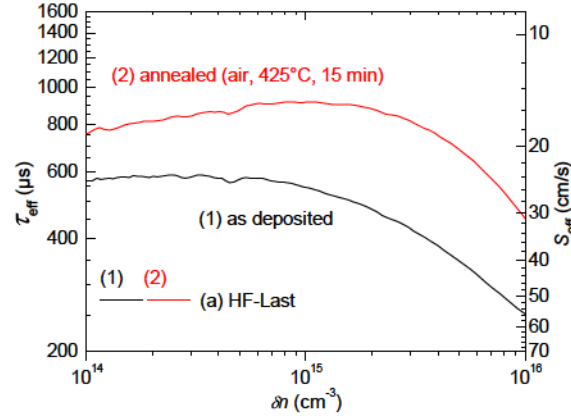
Figure 5.6: Effects of annealing on injection (δn) dependent effective minority charge carrier lifetimes τ_{eff} and surface recombination velocities S_{eff}. HF-Last c-Si passivated by PECVD-AlO$_x$/SiN$_x$ stacks in as deposited state are compared to the annealed state.

Fig. 5.6 demonstrates that in the as deposited state the AlO$_x$/SiN$_x$ stack already exhibits a moderate passivation quality due to a partial activation by the thermal budget during SiN$_x$ deposition. The passivation quality is then enhanced upon annealing, leading to a higher minority charge carrier lifetime (see discussion in section 5.1). The aim of this work is to better understand the origin of this partial activation (as deposited) and of the enhancement (annealed) of passivation quality due to D_{it} and Q_{ox} investigated by means of C-V measurements. All measurements were performed at the same gate contact dot for each sample.

At first, consecutive C-V curves in sweep mode were measured of the as deposited and annealed samples in order to get a first idea of their charge stability, as depicted in Fig. 5.7. The C-V sweeps were measured in both directions: first from accumulation to inversion (acc-inv, solid lines), then from inversion to accumulation (inv-acc, dashed lines). The purpose of this is to obtain information on the trapping and detrapping phenomena through hysteresis analysis as described in section 4.5. The consecutive C-V sweeps, each in both directions, are numbered in the order they were performed (1 to 11). The start- and end-voltages for each sweep were kept constant, unless a shift of the C-V curve along the voltage axis was evident. Fig. 5.7(a) and (b) show a selection of these sweeps, Fig. 5.7(c) and (d) show the obtained charge density $Q_{ox,eff}$ of all consecutive sweeps, for the as deposited and the annealed sample, respectively. The initial sweeps (#1 to #4) of the as
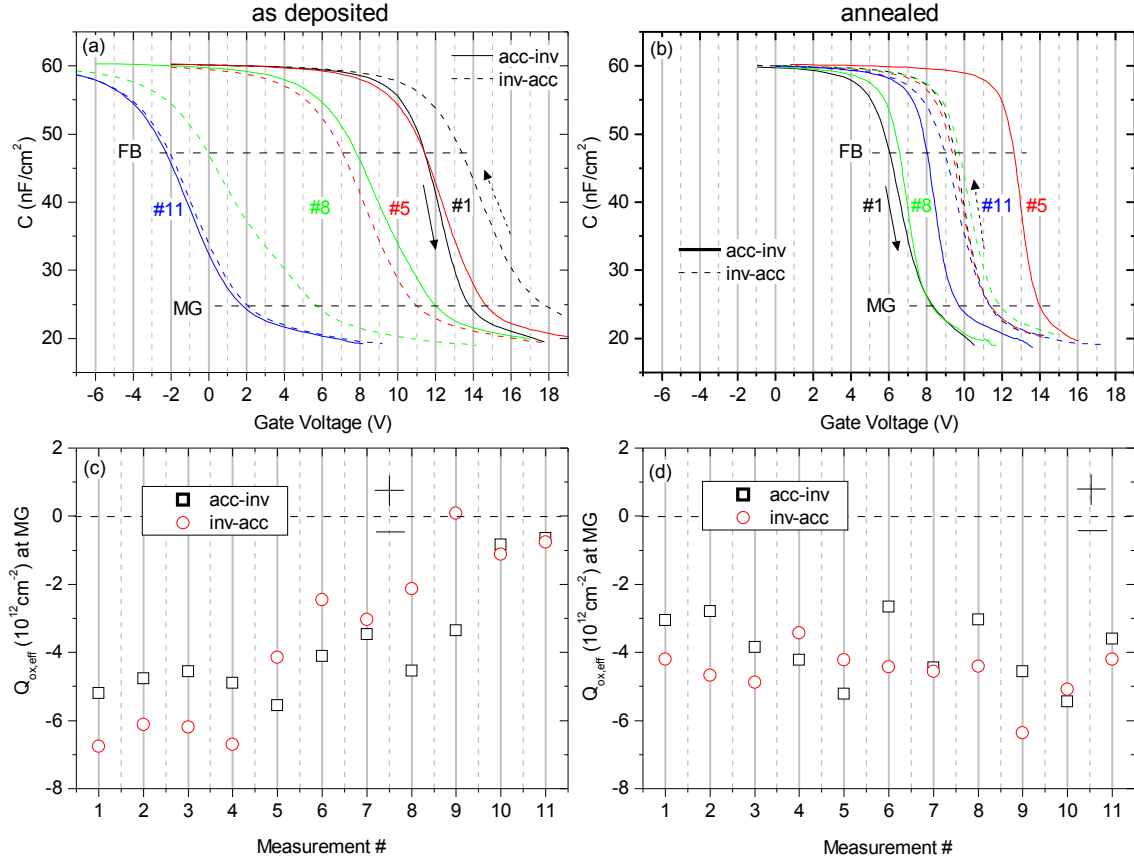
Figure 5.7: Consecutively measured high-frequency (1 MHz) C-V sweeps and the corresponding $Q_{ox,eff}$ at mid gap (MG) of as deposited (a+c) and annealed samples (b+d). Arrows indicate the sweep direction (acc-inv or inv-acc). The stability of $Q_{ox,eff}$ is investigated.

deposited sample reveal a hysteresis formation typical for the trapping and detrapping of charges in AlO_x defects states near the c-Si/AlO_x interface (see section 4.5). Note that the hysteresis forms around a value of $Q_{ox,eff} = -(6 \pm 1) \times 10^{12}\, cm^{-2}$, thus, larger than the fixed charge density of $Q_{ox,eff} = -4.5 \times 10^{12}\, cm^{-2}$ obtained from the annealed AlO_x-single layer deposited also on HF-Last c-Si (section 5.3). Yet, sweeps 5 to 11 reveal a continuous shift of the C-V curves, along with a decrease of negative $Q_{ox,eff}$ down to a stable value of $-7 \times 10^{11}\, cm^{-2}$ including a diminishing hysteresis. Thus, the initially high $Q_{ox,eff}$ is not stable and decreases by almost one order of magnitude upon relatively low applied gate voltages during C-V sweeps. This indicates that a detrapping of negative charges is induced by the moderate applied voltages during the C-V sweeps. Fixed negative charges with a cosiderably lower density remain.

In contrast, the annealed sample reveals a more stable negative charge density with an average value of $Q_{ox,eff} = -4.2 \times 10^{12}\, cm^{-2}$ which is in very good agreement with the fixed charge density of the annealed AlO_x-single layer. This is consistent with the expectation that the positive charges associated with SiN_x, used here as capping layer on AlO_x, may be
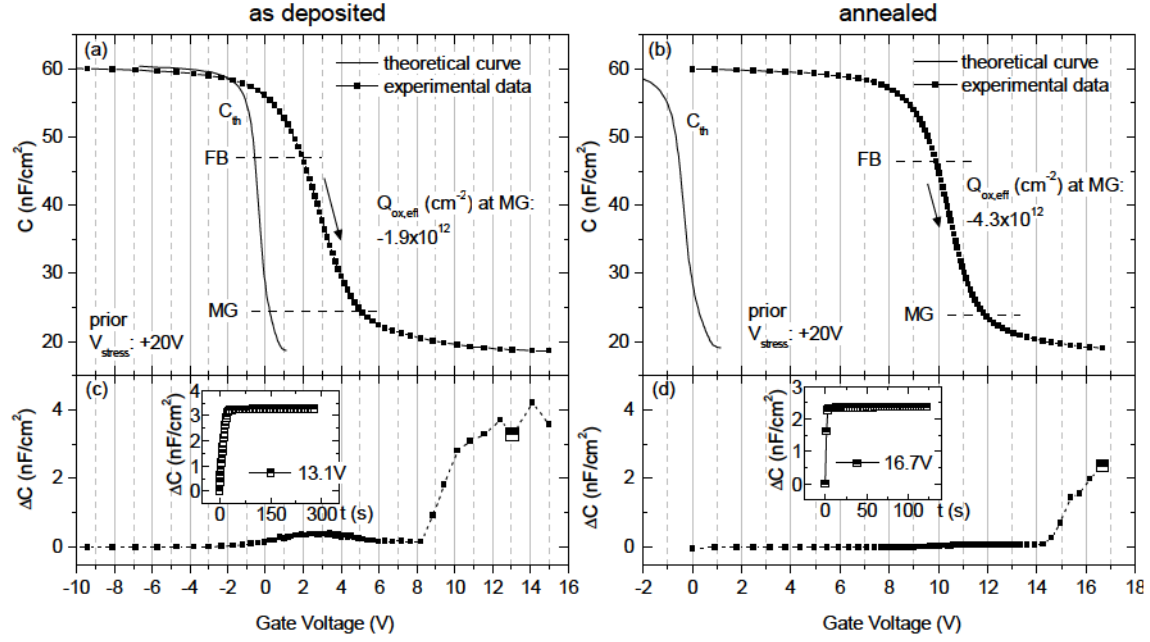
Figure 5.8: High-frequency C-V measurements in relaxation mode and the corresponding relaxation capacitance ΔC over gate voltage of as deposited (a+c) and annealed samples (b+d). C-V curves were measured following a V$_\text{stress}$ of +20 V (500 s) for charge stabilization. Insets illustrate exemplary C-t traces at the indicated gate voltage.

absent or much lower in density compared to SiN$_\text{x}$ applied directly on Si. In the annealed case hysteresis formation does not have a dominant orientation. Conversely, the hysteresis with an amplitude of $\pm 1 \times 10^{12}\,cm^{-2}$ reveals that in addition to the fixed charges, charge trapping/detrapping phenomena and/or charge redistribution in the AlO$_\text{x}$ clearly lead to fluctuations of $Q_{ox,eff}$ and therefore most probably also of the field-effect passivation.

The second experiment aims at the determination of the defect state density D_{it} at the c-Si/AlO$_\text{x}$ interface which is a measure for the chemical passivation. To achieve this, C-V measurements need to be performed in combination with relaxation analysis. This makes it possible to evaluate the reliability of the experimental C-V data and to obtain the correct parameters (C_{ox} and N_A) for the theoretical C-V curve (see section 4.2). The charge instabilities, however, posed a challenge in this regard. Nevertheless, systematic investigations with an applied V$_\text{stress}$ prior to the C-V measurement in relaxation mode revealed that these instabilities can be minimized by applying a prior V$_\text{stress}$ of +20 V for 500 s and then measuring from accumulation to inversion (see section 4.6). The resulting C-V curves with the corresponding relaxations ΔC obtained from the C-t traces for the as deposited and annealed samples are depicted in Fig. 5.8. On the one hand, the charge state of the as deposited sample in Fig. 5.8(a) during the measurement reveals a $Q_{ox,eff} = -1.9 \times 10^{12}\,cm^{-2}$, which is slightly higher than the state after the consecutive C-V sweeps. This indicates that the V$_\text{stress}$ apparently slightly recharged the AlO$_\text{x}$/SiN$_\text{x}$ stack negatively. This even occurs during the C-V measurement itself and can be seen
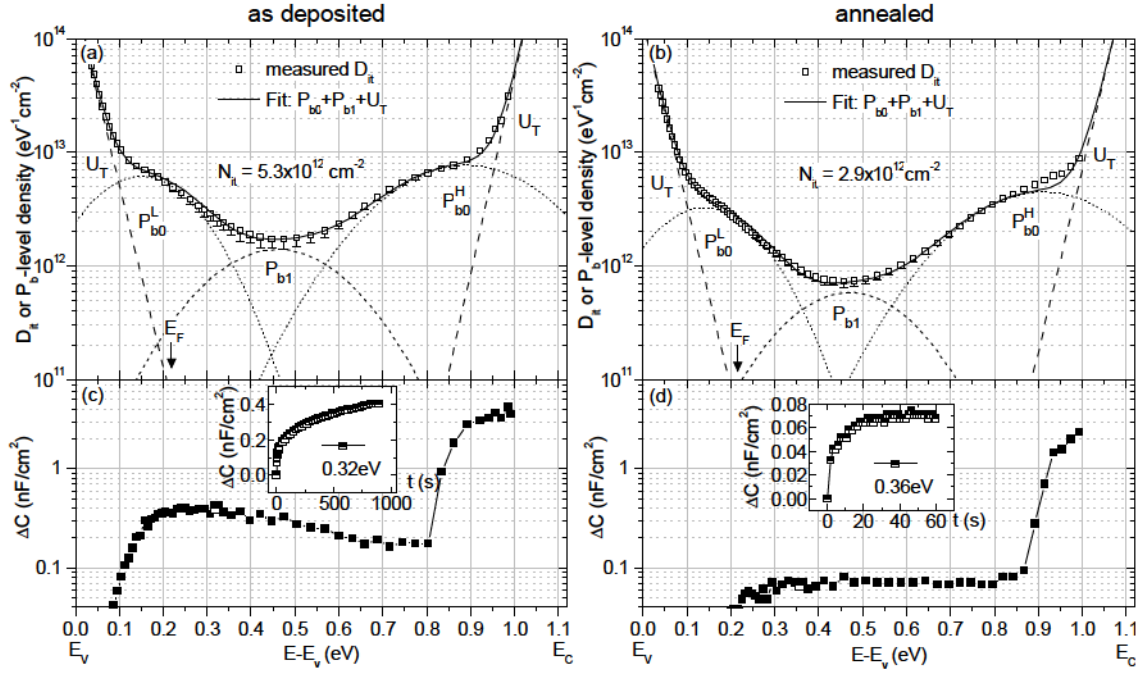
Figure 5.9: Defect state density (D_{it}) at the c-Si/(SiO$_x$)/AlO$_x$ interface over c-Si band gap of an as deposited (a) and annealed (b) sample with corresponding relaxation ΔC-spectra (c,d). D_{it}-spectra were fitted by the sum of Gaussian distributions for P$_{b0}$- and P$_{b1}$-like defects and exponential functions for strained bond defects ΔU$_T$. The donator- and acceptor-like states of the P$_{b0}$-defect are energetically separated into P$_{b0}$^{L} and P$_{b0}$^{H}. For the P$_{b1}$ they are energetically close and represented by one Gaussian. The error bars represent a correction of D_{it} taking into consideration the influence of ΔC.

around the FB voltage in the C-V graph (Fig. 5.8(c)). On the other hand, the annealed sample charge state remains at $Q_{ox,eff} = -4.3 \times 10^{12}\,cm^{-2}$ (Fig. 5.8(b)). For both samples, as can be seen in the relaxation data (Fig. 5.8(c) and (d)), true inversion capacitance is reached. This is indicated by the exemplary C-t trace insets (as deposited: at 13.1 V, annealed: at 16.7 V), where the capacitance reaches a constant value due to the formation of an inversion region. Hence, no correction of the parameters for the theoretical C-V curve (C$_{th}$) needs to be considered for the calculation of D_{it}.

The resulting D_{it}-spectra for both samples are depicted in Fig. 5.9. The corresponding relaxation data ΔC is plotted on a logarithmic scale in order to evaluate its effect on D_{it}. The positive ΔC values (see inserts at 0.32 eV and 0.36 eV) indicate a slight negative charging of the AlO$_x$/SiN$_x$ stack. Since the measurements were performed from accumulation to inversion the positive ΔC leads to a stretching of the C-V curve. This results in an increase of its slope resulting in slightly higher D_{it} values. Therefore, the error bars ΔD_{it} calculated from ΔC only point towards lower D_{it} values, as can be seen in Fig. 5.9(a) for the as deposited sample. For the annealed sample the relaxations are negligible (Fig. 5.9(d)) and half an order of magnitude smaller than for the as deposited sample. This reflects the

stability of the annealed sample regarding its charge which results in a negligible error of D_{it}(Fig. 5.9(b)).

The D_{it} spectra of both samples can be fitted by Gaussian distributions with energetic positions as those reported for P$_{b0}$ and P$_{b1}$ defects at the c-Si/SiO$_2$ interface (see sections 2.2.1 and 4.2). This indicates the presence of a SiO$_x$-like interlayer forming a c-Si/(SiO$_x$)/AlO$_x$ interface for the as deposited, but particularly for the annealed sample. The formation of an SiO$_2$ interlayer upon thermal treatments is commonly reported in the literature [Din12b, Hoe06]. The area of each Gaussian represents N_{it} of the corresponding defect type. Note that the P$_{b0}$-like defect consists of donor states (P$_{b0}$^{L}) in the lower part of the c-Si band gap and acceptor states (P$_{b0}$^{H}) in the higher part, as described in section 2.2.1, whereas the Gaussian distribution for the P$_{b1}$-like defect already includes the acceptor and donor states which are energetically very close in the c-Si band gap. The annealing process clearly leads to a considerable reduction of the interface defect state density. For the as deposited sample a defect density integrated over the c-Si band gap (P$_{b0}$ +P$_{b1}$) of $N_{it} = 5.3 \times 10^{12} \, cm^{-2}$ is calculated. Upon annealing it is reduced down to $N_{it} = 2.9 \times 10^{12} \, cm^{-2}$, by a factor of 1.8. In Fig. 5.6 a reduction of S_{eff} by factor of 1.7 (at $\delta n = 10^{15} \, cm^{-3}$) upon annealing can be observed. Therefore, since $S_{eff} \sim N_{it}$, it can be concluded that this significant reduction of interface defect states is the main contributor to the enhanced passivation quality, i.e. the increase of τ_{eff} shown in Fig. 5.6.

5.5 AlO_x/SiN_x stacks on H-Last Si: Effects of constant voltage stress

In this section the origin of the instabilities of $Q_{ox,eff}$ of the as deposited sample are investigated, which upon consecutive C-V sweeps was reduced from a relatively high negative charge density of $Q_{ox,eff} = -6 \cdot 10^{12} \, cm^{-2}$ down to $Q_{ox,eff} = -7 \cdot 10^{11} \, cm^{-2}$ (Fig. 5.7). For this purpose, constant gate voltage stress (V_{stress}) in conjunction with C-V measurements were performed. In this context, both the stability of the annealed sample as well as the origin of the hysteresis formation have been studied.
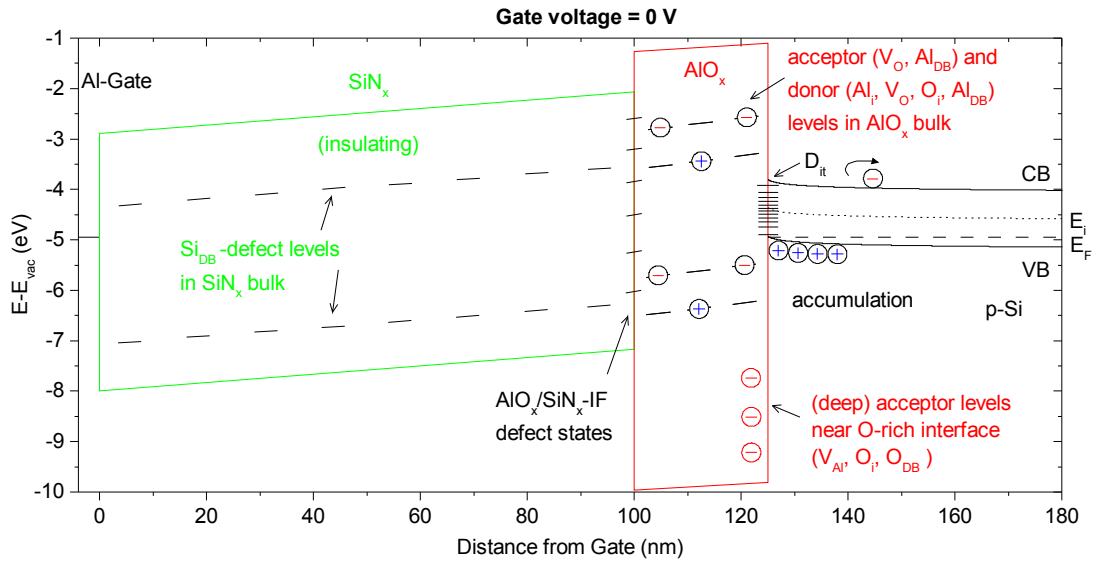
Figure 5.10: Band diagram of the c-Si/AlO_x(25 nm)/SiN_x(100 nm)/Al-system at a gate voltage of 0 V and with a negative fixed charge density of $Q_{ox} = -4 \times 10^{12} cm^{-2}$ located at the c-Si/AlO_x interface. Defect levels in the AlO_x-bulk [Cho13], the SiN_x-bulk [Via11a] and at the interfaces are indicated . The band structure for the given voltage was calculated using the *Band Diagram Program* [Sou06].

For this purpose, it is insightful to discuss the band structure and the defect states of the c-Si/AlO_x(25 nm)/SiN_x(100 nm)/Al-system. Thus, the band structure was simulated using the *Band Diagram Program* [Sou06] and is depicted in Fig. 5.10. This diagram represents the c-Si/AlO_x/SiN_x-structure at a gate voltage of 0 V and with a negative fixed charge density of $Q_{ox} = -4 \times 10^{12} \, cm^{-2}$ located at the c-Si/AlO_x interface. Consequently, the system is in the accumulation state. In the AlO_x bulk, near the c-Si valence (VB) and conduction band (CB), the acceptor and and donor levels related to the aluminum and oxygen interstitials (Al_i, O_i), aluminum dangling bonds (Al_DB) and oxygen vacancies (V_O) are depicted in an arbitrary charge state. These levels are responsible for charge trapping and trap-assisted charge transport via tunneling in the AlO_x. The latter is responsible for the leakage currents observed for AlO_x-single layers. Near the AlO_x VB and close to the O-rich c-Si/(SiO_x)/AlO_x interface the deep acceptor levels associated with

aluminum vacancies (V_{Al}), oxygen interstitials (O_i) and oxygen dangling bonds (O_{DB}) are located. These deep acceptor levels are the origin of the fixed negative charge in AlO$_x$. All these assigned states and their roles are based on theoretical and experimental studies as described in section 2.2.2. This is also the case for the defect levels due to Si dangling bonds (Si_{DB}) in the SiN$_x$ bulk, which in all the measurements presented here acts mainly as an insulator preventing charge injection from the gate into the AlO$_x$. In addition, the interface defect levels are indicated at the c-Si/(SiO$_x$)/AlO$_x$ interface (as D_{it}) and at the AlO$_x$/SiN$_x$ interface.

The V_{stress} experiments were conducted as follows: first a V_{stress} was applied for a time period of 500 s while the C-t trace was monitored. After a relaxation process a constant capacitance was reached, which means that charging or discharging processes were completed. Therefore, the result of V_{stress} is to bring the AlO$_x$/SiN$_x$ insulator system into a defined initial charge state. In addition to fixed negative charges, the main contributors to this charge state $Q_{ox,eff}$ are charged traps near the c-Si/AlO$_x$ interface, in the AlO$_x$ bulk, near the AlO$_x$/SiN$_x$interface and near the SiN$_x$/Al-gate interface. Note that traps inside the SiN$_x$ bulk are not taken into consideration due to the insulating characteristics which suggest that no charge transport takes place through the SiN$_x$. The application of V_{stress} was followed by a C-V sweep measured first from accumulation to inversion. Then, the same V_{stress} was applied again and followed by a C-V sweep measured from inversion to accumulation. These C-V sweeps reveal the charge state generated by the prior V_{stress}. In case of hysteresis formation one can also identify which of the following charge dynamics is dominant at the corresponding charge state (see section 4.5):

- **Counter-clockwise hysteresis:** Charge injection from the c-Si substrate leading to trapping/detrapping of charges near the c-Si/AlO$_x$ interface, in the AlO$_x$ bulk and/or the AlO$_x$/SiN$_x$interface. For p-type c-Si this results into a counter-clockwise hysteresis formation.

- **Clockwise hysteresis:** Results from charge injection from the Al-gate into the SiN$_x$, charging states near the SiN$_x$/Al-gate interface and/or charge redistribution in the AlO$_x$/SiN$_x$ stack due to trap-assisted charge transport.
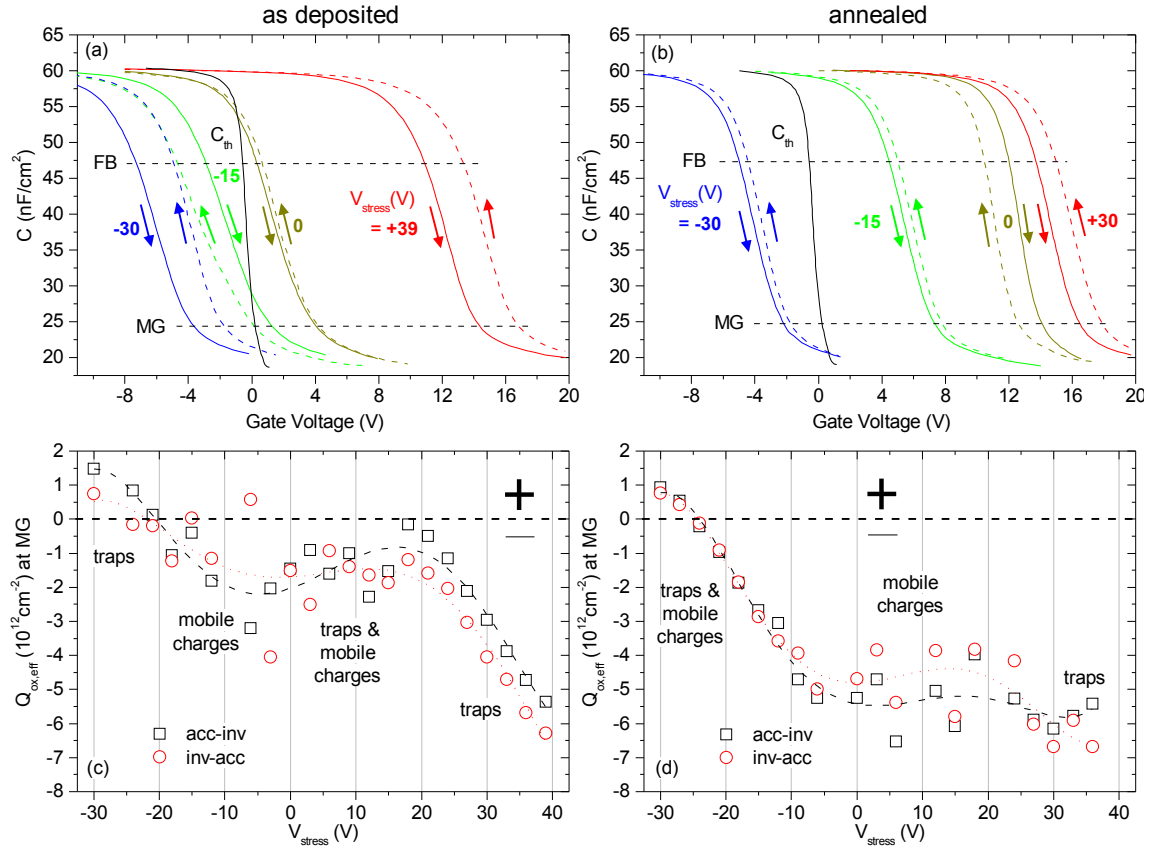
Figure 5.11: High-frequency C-V curves obtained after prior V$_{stress}$ and the corresponding $Q_{ox,eff}$ at mid gap (MG) of as deposited (a+c) and annealed samples (b+d). Arrows indicate the sweep direction (acc-inv or inv-acc) and C_{th} is the theoretical ideal C-V curve. A counter-clockwise hysteresis indicates charge trapping near the c-Si/AlO$_x$ interface through charge injection from the c-Si and is referred to as traps. A clockwise hysteresis indicates charge injection at SiN$_x$/Al gate interface and/or charge redistribution in the AlO$_x$ (and SiN$_x$) bulk, which is referred to as mobile charges.

Fig. 5.11(a) and 5.11(b) show C-V sweep measurements in both directions (acc-inv and inv-acc), each conducted upon prior V$_{stress}$ for the as deposited and the annealed sample, respectively. From these and a larger selection of C-V sweeps $Q_{ox,eff}$ was calculated and is depicted vs. V$_{stress}$ in Fig. 5.11(c) and 5.11(d). Here, the values of $Q_{ox,eff}$ indicate hysteresis formation as observed in the figures above. Initially, for V$_{stress}$ = 0 V, the as deposited sample shows a lower negative $Q_{ox,eff}$ than the annealed sample, as seen already in the previous experiments. As prior negative V$_{stress}$ is applied, the C-V curve (Fig. 5.11(a)) shifts towards negative gate voltages as negative $Q_{ox,eff}$ is reduced (Fig. 5.11(c)). First, hysteresis formation due to mobile charges in the AlO$_x$ or traps at the SiN$_x$/Al interface are revealed. At larger negative V$_{stress}$ hysteresis formation due to traps near the c-Si/AlO$_x$ interface becomes dominant. At V$_{stress}$ = - 30 V these traps are charged positively, thus, the C-V curve (Fig. 5.11a) is shifted to the negative gate voltage range as

Figure 5.12: Band diagram of the c-Si/AlO$_x$(25 nm)/SiN$_x$(100 nm)/Al-system at a gate voltage (stress) of - 15 V and with a negative fixed charge density of $Q_{ox} = -4 \cdot 10^{12} cm^{-2}$ located at the c-Si/AlO$_x$ interface. The left image depicts possible negative charge trapping near the SiN$_x$/Al-gate interface. The right image depicts positive charge trapping in the AlO$_x$ or near the AlO$_x$/SiN$_x$ interface due to charge injection from the c-Si which is in the strong accumulation state. Electron injection from the Al-gate into the AlO$_x$ is negligible due to the insulating character of the SiN$_x$.

$Q_{ox,eff}$ is now positive (Fig. 5.11b).

This effect can be explained by the processes depicted in Fig. 5.12. Here, the band structure of the c-Si/AlO$_x$/SiN$_x$-system is illustrated at a constant gate voltage of V$_{stress}$ = -15 V. The system is in strong accumulation. Therefore, electrons are injected from the AlO$_x$/SiN$_x$-stack into the Si, and/or positive charges (holes) are injected from the c-Si into AlO$_x$/SiN$_x$-stack. The positive charges are trapped and/or transported by the defect levels primarily in the AlO$_x$ and may even reach traps in the SiN$_x$. However, the insulating character of the SiN$_x$ prevents these charges to get to the Al-gate. From the gate negative charges may be injected into the SiN$_x$, but they are prevented to get to the AlO$_x$. The main contributor to $Q_{ox,eff}$ is thus the positive charge trapping in the AlO$_x$ and probably to some extent also in the SiN$_x$ at or near the AlO$_x$/SiN$_x$ interface. This assumption is supported by the formation of the hysteresis which is unambiguously attributed to charge trapping near the c-Si/AlO$_x$ interface through charge injection. The trapped positive charges even exceed the negative fixed charges at higher negative V$_{stress}$ initially leading to a reduction of the negative $Q_{ox,eff}$ and then to a switch of polarity.

As shown in Fig. 5.11(c), applying a positive V$_{stress}$ > 20 V leads to an increase of the initially low negative $Q_{ox,eff}$ of the as deposited AlO$_x$/SiN$_x$ stack. At V$_{stress}$ = 39 V $Q_{ox,eff}$ reaches similar negative values as the stable $Q_{ox,eff}$ of the annealed sample at V$_{stress}$ = 0 V (Fig. 5.11d). Fig. 5.13 depicts the band structure of the c-Si/AlO$_x$/SiN$_x$-system at a
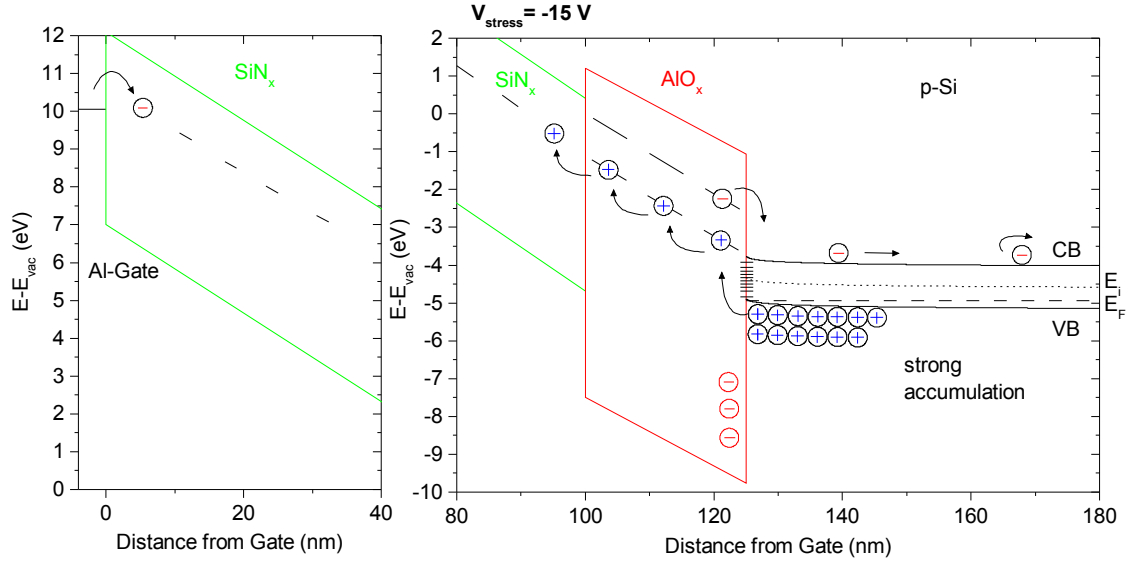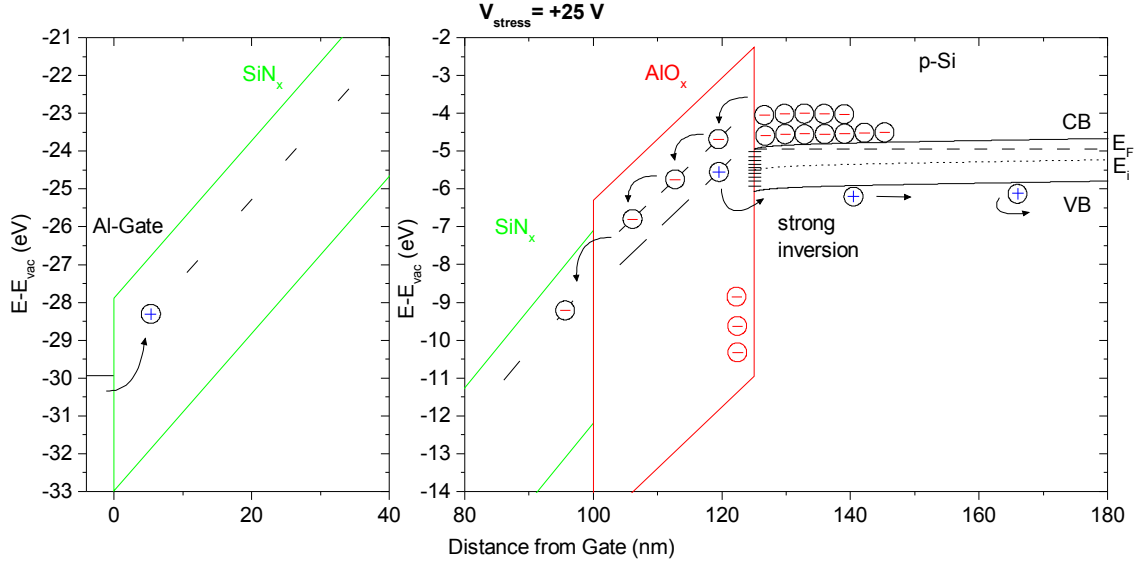
Figure 5.13: Band diagram of the c-Si/AlO$_x$(25 nm)/SiN$_x$(100 nm)/Al-system at a gate voltage (stress) of +15 V and with a negative fixed charge density of $Q_{ox} = -4 \times 10^{12} cm^{-2}$ located at the c-Si/AlO$_x$ interface. The left image depicts positive charge trapping near the SiN$_x$/Al-gate interface. The right image depicts negative charge trapping in the AlO$_x$ or near the AlO$_x$/SiN$_x$ interface due to electron injection from the c-Si which is in the strong inversion state. Positive charge injection from the Al-gate into the AlO$_x$ is negligible due to the insulating character of the SiN$_x$.

constant gate voltage of V$_{stress}$ = + 25 V. In this case, the system is in strong inversion. Hence, electrons are injected from the c-Si into the AlO$_x$/SiN$_x$ stack, increasing the negative charge density. The hysteresis formation at V$_{stress}$ > 20 V in Fig. 5.11(c) clearly indicates the charge trapping near the c-Si/AlO$_x$ interface.

Repeating the V$_{stress}$ experiments revealed that this trapping of positive and negative charges in the AlO$_x$/SiN$_x$ stack is a reversible process. Consequently, for the as deposited sample it can be concluded, that the initially high $Q_{ox,eff}$ measured in Fig. 5.7(a) was due to initially negatively charged traps, that were discharged upon C-V sweeps. This means that the thermal budget during the SiN$_x$ deposition may have partially activated the AlO$_x$ field-effect passivation by charging traps near the c-Si/AlO$_x$ interface negatively. However, this is not a stable state and, therefore, the annealing process is mandatory in order to fully activate the field-effect passivation.

As can be seen in Fig. 5.11 (b) and (d) for the annealed sample, as the positive V$_{stress}$ is increased up to +24 V, the initially already high $Q_{ox,eff}$ remains stable with an average value of $Q_{ox,eff} = -(4.7 \pm 1.0) \cdot 10^{12} \, cm^{-2}$. A counter-clockwise hysteresis becomes evident which can be attributed to either charge trapping near the SiN$_x$/Al interface through charge injection from the Al gate or to mobile charge redistribution in the AlO$_x$/SiN$_x$ stack. It is more likely that the latter effect, in particular charge redistribution in the AlO$_x$, is the main cause for this hysteresis orientation, for the following reasons: Firstly,

this effect takes place closer to the c-Si/AlO$_\text{x}$ interface and therefore has a greater influence on $Q_{ox,eff}$ (see section 4.5), i.e. it is more likely to be measurable. Secondly, due to the high trap density in the AlO$_\text{x}$ bulk (causing the leakage currents), charges may be redistributed more easily through trap-assisted transport. For V$_\text{stress}$ > 27 V the negative $Q_{ox,eff}$ increases to about $Q_{ox,eff} = -6 \times 10^{12}\,cm^{-2}$ and hysteresis formation switches polarity. This indicates that at this large positive V$_\text{stress}$, negative trap charging through charge injection from the c-Si becomes dominant and leads to an increase of the negative $Q_{ox,eff}$. These observations agree very well with the previous conclusion that the high negative $Q_{ox,eff} = -(4.7 \pm 1.0) \cdot 10^{12}\,cm^{-2}$ of the annealed sample originates from fixed charges and not from negatively charged traps like for the as deposited sample. Applying a negative V$_\text{stress}$ to the annealed sample though (Fig. 5.11), leads to a decrease of negative $Q_{ox,eff}$. Similar to the as deposited sample, for a larger negative V$_\text{stress}$> -24 V, $Q_{ox,eff}$ also becomes positive. This is most probably due to the same reason, i.e. injection of positive charges into the AlO$_\text{x}$/SiN$_\text{x}$ stack. The rather small hysteresis formation in this case indicates that either these positively charged traps are located further away from the c-Si/AlO$_\text{x}$ interface, meaning in the AlO$_\text{x}$ bulk and/or in near the AlO$_\text{x}$/SiN$_\text{x}$ interface, or that less traps remain to be charged and discharged.

Consequently, for the annealed sample it can be concluded that although the stable negative fixed charges initially dominate with their contribution to $Q_{ox,eff}$, traps located in the AlO$_\text{x}$ bulk or near the AlO$_\text{x}$/SiN$_\text{x}$ interface can be charged positively upon a negative V$_\text{stress}$. These positively charged traps can overcompensate the negative fixed charges, hence, lead to a net positive charge which would most probably deteriorate the quality of the field-effect passivation.

Figure 5.14: High-frequency (1 MHz) C-V measurements in relaxation mode and the corresponding relaxation capacitance ΔC over gate voltage of as deposited (a+c) and annealed samples (b+d). C-V curves were measured following a V_{stress} of + 20 V (500 s) for charge stabilization. Insets illustrate exemplary C-t traces at the indicated gate voltage. C-V measurements were performed before (initial state) and after negative and positive V_{stress} experiments.

The next experiment aimed at studying the effect of V_{stress} on the chemical passivation properties, thus, D_{it} of the as deposited and annealed c-Si/AlO$_x$/SiN$_x$ structures. For this purpose, following the negative and positive V_{stress} experiments depicted in Fig. 5.11, C-V measurements in relaxation mode were conducted in the same way as in the previous section where the initial D_{it}-spectra were obtained: first a relatively low V_{stress} of + 20 V was applied in order to create a stable charge state. This was followed by the C-V measurement from accumulation to inversion in relaxation mode. The results are visualized in Fig. 5.14. For the as deposited sample (Fig. 5.14(a)) the C-V curves in relaxation mode after the negative V_{stress} (red symbols) and after positive V_{stress} (green symbols) are compared to the one before the V_{stress} experiments (black symbols), i.e. to the initial state of the sample. In Fig. 5.14(c) the corresponding relaxations ΔC are depicted. Apart from the shift along the voltage axis due to shifts of $Q_{ox,eff}$, the relaxations reveal no change in their characteristics. This observation is crucial for the analysis of $Q_{ox,eff}$ and D_{it} since it demonstrates that the voltage stress experiments caused no change in the charge dynamics and no deterioration of the insulating property of the SiN$_x$. The inset shows that still true inversion capacitances are obtained and, therefore, no leakage current needs to be accounted for. This is also the case for the annealed sample. Nevertheless, the charge state in regard to $Q_{ox,eff}$ is affected by the V_{stress} experiments: For the as deposited sample it most probably can be attributed to a "memory effect", where part of the states in the AlO$_x$/SiN$_x$ stack charged during
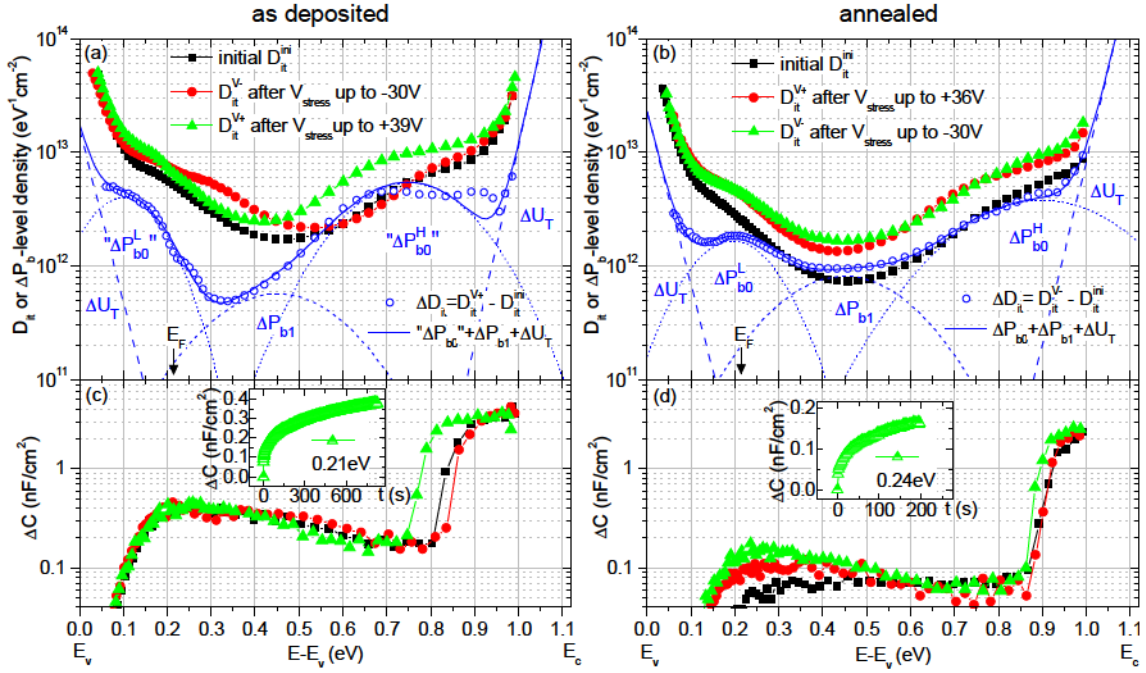
Figure 5.15: Defect state density (D_{it}) at the c-Si/(SiO$_x$)/AlO$_x$ interface over the c-Si band gap of as deposited (a) and annealed (b) sample with corresponding relaxation ΔC-spectra (c,d). D_{it}-spectra were obtained before (initial state) and after negative and positive V_{stress} experiments. The generated defect state ΔD_{it}-spectra were fitted by the sum of Gaussian distributions for generated ΔP_{b0}- and ΔP_{b1}-like defects and exponential functions for strained bond defects ΔU_T.

the negative and positive V_{stress} experiments remain charged positively and negatively, respectively, during the C-V measurement in spite of the prior $V_{stress} = +20$ V. In the case of the annealed sample there is a gradual decrease of $Q_{ox,eff}$ upon the V_{stress} experiments. This may indicate that additional defects in the AlO$_x$ bulk (or even SiN$_x$) were generated reducing the negative $Q_{ox,eff}$ through positive charge trapping.

A large negative or positive V_{stress} has a considerable effect on the c-Si/AlO$_x$ interface defect state density of the as deposited as well as the annealed sample as depicted in Fig. 5.15(a) and (b), respectively. The difference of the D_{it}-spectra before and after the V_{stress} experiments was calculated (blue, open symbols) and fitted by the sum (blue, solid line) of Gaussian distributions representing P$_{b0}$- and P$_{b1}$-defects and of exponential functions for stained bond (U$_T$) defects at the c-Si band edges. This sum indicates additionally generated defects states. Underneath the D_{it}-spectra the corresponding relaxations ΔC over the c-Si band gap energy E-E_v are shown (Fig. 5.15(c) and (d)).

In the case of the as deposited sample, the relaxation ΔC characteristics $\Delta C(E)$ do not change upon V_{stress}. However, the D_{it}-spectra are affected quantitatively as well as qualitatively: After the negative V_{stress} experiments an increase of D_{it} below mid gap (MG), i.e. below E-$E_v = 0.56$ eV, can be observed. Yet, following the positive V_{stress} experiments,
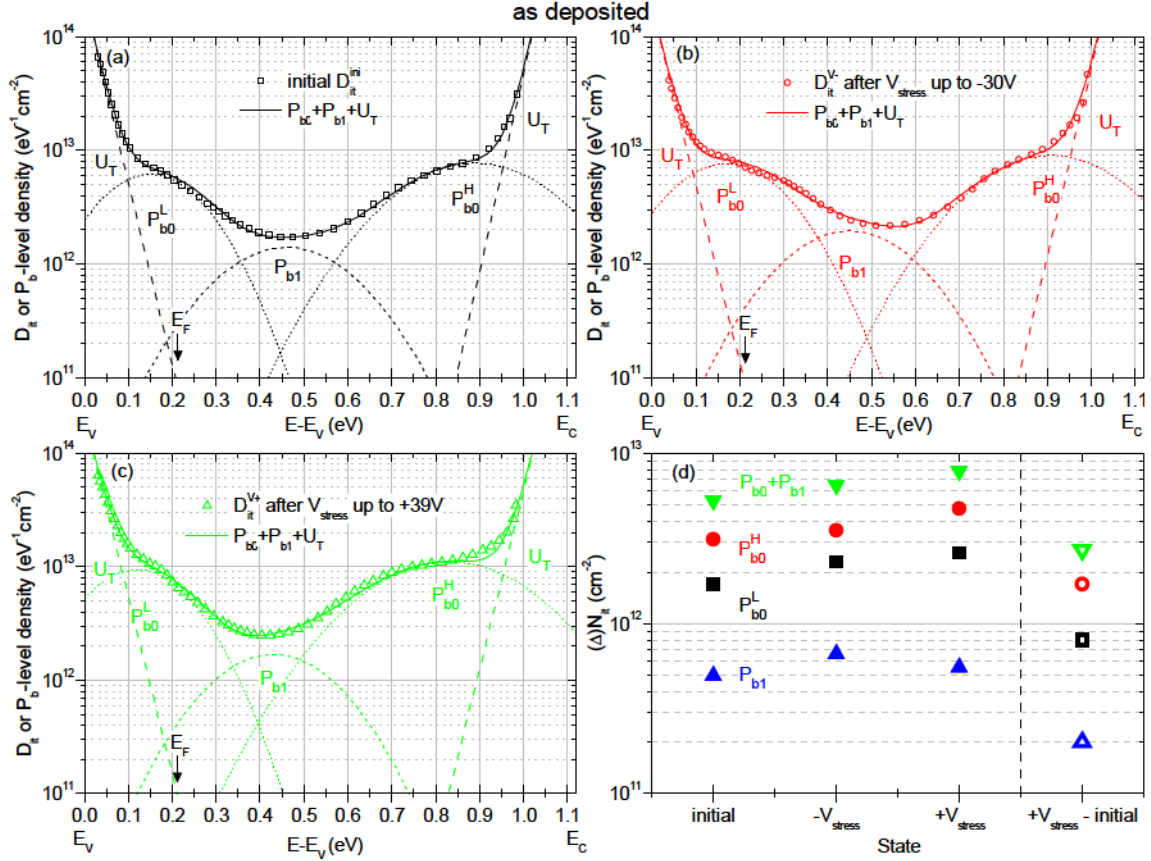
Figure 5.16: Effects of V$_{stress}$ experiments: (a-c) D_{it}-spectra of as deposited AlO$_x$/SiN$_x$ stack on HF-Last c-Si obtained before (initial state) and after negative and positive V$_{stress}$ experiments. D_{it}-spectra were fitted individually by the sum of Gaussian distributions for P$_{b0}$- and P$_{b1}$-like defects and exponential functions for strained bond defects ΔU_T. (d) Defect density N_{it} for obtained from area of corresponding Gaussians of P$_{b0}$- and P$_{b1}$-like defects as well as for generated ones (ΔN_{it}) upon V$_{stress}$ experiments.

D_{it} decreases again below MG and increases above MG. This effect is rather surprising as it cannot originate from errors due to leakage currents or trapping/detrapping of charges as seen for the AlO$_x$-single layers on c-Si (see section 5.3).

For a more detailed analysis of this effect, the D_{it}-spectra were fitted individually by Gaussians of the different defect types. The results are shown in Fig. 5.16 for the initial state (a), which was discussed in the previous section, for the state after negative V$_{stress}$ (b) and for the state after positive V$_{stress}$ (c). Fig. 5.16(d) depicts N_{it} (i.e. area of Gaussians) of the individual defects types P$_{b0}$(black and red closed symbols), P$_{b1}$(blue closed symbols), and their sum P$_{b0}$+P$_{b1}$ (green closed symbols) as well as the generated ones (corresponding open symbols) for the different states. Here, the negative V$_{stress}$ experiments apparently led to an increase of N_{it} for all defect types. The subsequent positive V$_{stress}$ experiments increased the P$_{b0}$-type defects but decreased the P$_{b1}$-types. In principle this may indicate a change of the chemical structure, since the difference between P$_{b0}$ and P$_{b1}$ defects lies in
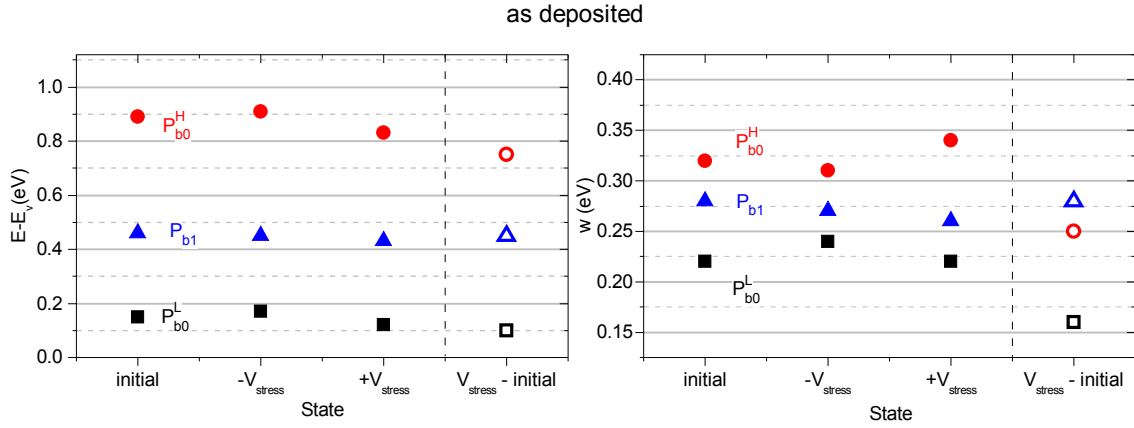
Figure 5.17: Effects of V$_{stress}$ experiments: Energetic position in c-Si band gap (*E-E$_v$*, left graph) and width (w, right graph) of Gaussians for P$_{b0}$- and P$_{b1}$-like defects used for fitting of experimental *D$_{it}$*-spectra of as deposited sample in Fig 5.16. Based on the consistency of the parameters the validity of quantitative and qualitative changes of the *D$_{it}$*-spectra upon V$_{stress}$ experiments can be deduced.

the orientation of their corresponding intrinsic Si dangling bond. However, taking a look at the other parameters of the Gaussians, that is their energetic position (*E-E$_v$*) in the c-Si band gap and their width (w) as depicted in Fig. 5.17, points at a different source for this effect.

As seen in Fig. 5.17, in order to fit the *D$_{it}$*-spectra after the negative V$_{stress}$ experiments the energetic position (left graph) and in particular the width (right graph) of the Gaussians of each defect type had to be adjusted. This is also the case for the *D$_{it}$*-spectra after the positive V$_{stress}$ experiments as well as for the generated ones (state: V$_{stress}$- initial), which all differ from the energetic position and the width of the Gaussians in the initial state. It is unlikely that these modifications may originate from a change of the chemical structure. Therefore, it can be assumed that the qualitative changes of the *D$_{it}$*-spectra upon V$_{stress}$ have a different cause. The more likely cause is a spatial inhomogeneity of *Q$_{ox,eff}$* in the AlO$_x$/SiN$_x$ stack underneath the Al gate contact dot. This assumption is supported by the previous observations in regard to *Q$_{ox,eff}$* of the as deposited AlO$_x$/SiN$_x$stack. This includes the strong impact of trap charging in the AlO$_x$ or near the AlO$_x$/SiN$_x$ interface on *Q$_{ox,eff}$* as well as the "memory-effect" indicating partially stable trapped charges. Consequently, the V$_{stress}$ experiments may have induced locally differently charged traps in the AlO$_x$/SiN$_x$ stack causing a spatial inhomogeneity of *Q$_{ox,eff}$*. This inhomogeneity is known to result in artifacts in the slope of the C-V curve [McN74, McN75] which basically represents the superposition of several parallel connected C-V curves, each with a different *Q$_{ox,eff}$*. These artifacts in the slope are projected into the *D$_{it}$*-spectrum, which distort the true defect state densities. Nevertheless, an increase of *N$_{it}$* as well as strained bonds U$_T$ over the entire c-Si band gap are evident. Thus, a large V$_{stress}$ leads to a degradation of the
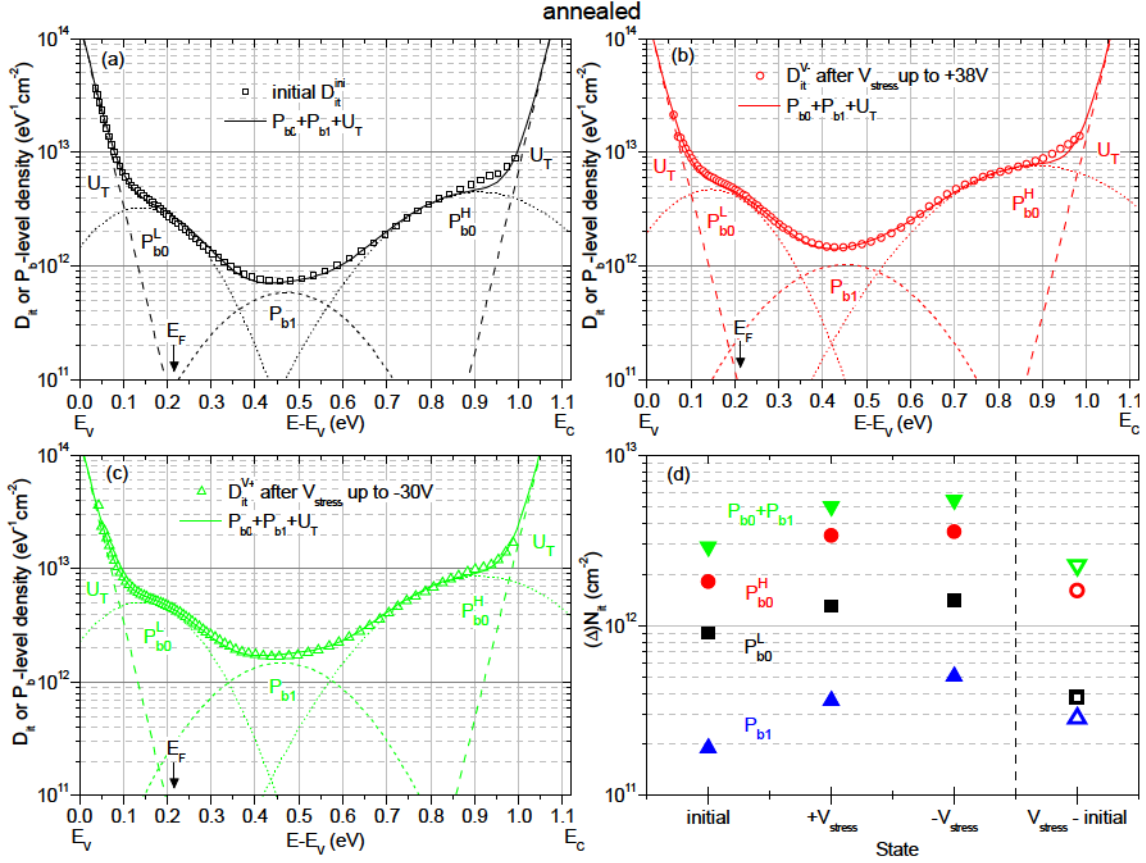
Figure 5.18: Effects of V$_{stress}$ experiments: (a-c) D_{it}-spectra of annealed AlO$_x$/SiN$_x$ stack on HF-Last c-Si obtained before (initial state) and after negative and positive V$_{stress}$ experiments. D_{it}-spectra were fitted individually by the sum of Gaussian distributions for P$_{b0}$- and P$_{b1}$-like defects and exponential functions for strained bond defects ΔU$_T$. (d) Defect density N_{it} for obtained from area of corresponding Gaussians of P$_{b0}$- and P$_{b1}$-like defects as well as for generated ones (ΔN_{it}) upon V$_{stress}$ experiments.

chemical passivation through the generation of additional Si dangling bond defects that act as recombination centers.

In the case of the annealed sample (Fig. 5.15(b)), ΔD_{it} increases nearly uniformly over the entire spectrum. A considerable increase occurs upon the positive V$_{stress}$ experiments, which is followed by a minor increase only after the subsequent negative V$_{stress}$ experiments. In addition, the capacitance relaxation ΔC spectrum shows an increase as well. This supports the previous assumption that, indeed, the V$_{stress}$ experiments also affect the charging characteristics of the annealed AlO$_x$/SiN$_x$ stack, probably by the generation of additional defects in the stack itself. The spectra of the generated defect states ΔD_{it} (blue symbols) can be fitted by Gaussian distributions with energetic positions and widths of Gaussians representing the P$_{b0}$ and P$_{b1}$ defects of a Si/SiO$_2$ interface. This, again, confirms the presence of a SiO$_x$-interlayer at the c-Si/AlO$_x$ interface. Additionally, it demonstrates a more consistent defect generation for the annealed sample than for the as deposited one.
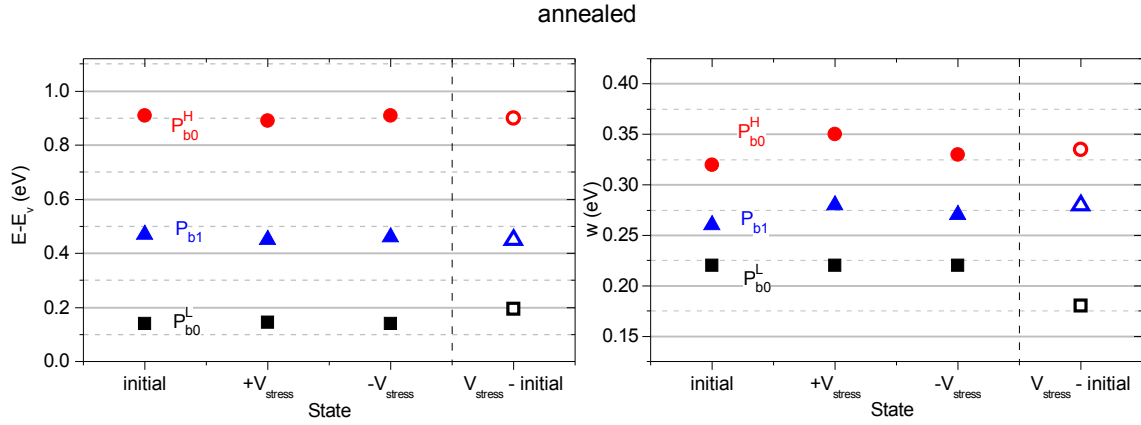
Figure 5.19: Effects of V$_{stress}$ experiments: Energetic position in c-Si band gap (E-E$_v$, left graph) and width (w, right graph) of Gaussians for P$_{b0}$- and P$_{b1}$-like defects used for fitting of experimental D_{it}-spectra of annealed sample in Fig 5.19. Based on the consistency of the parameters the validity of quantitative and qualitative changes of the D_{it}-spectra upon V$_{stress}$ experiments can be deduced.

This observation is supported by the results obtained from the individually fitted D_{it}-spectra in Fig. 5.18(a)-(c) and the correspondent fitting parameters of the Gaussians in Fig. 5.19. The energetic positions as well as the width of the Gaussians are very consistent revealing negligible deviations. This consistency can be attributed to the stability of $Q_{ox,eff}$ which originates mainly from fixed negative charges. Consequently, for the annealed sample a clear generation of P$_{b0}$- and P$_{b1}$-type defects is observed upon a large V$_{stress}$. This leads to a degradation of the chemical passivation at the c-Si/(SiO$_x$)/AlO$_x$ interface. The generation of P$_{b0}$- and P$_{b1}$-type defects (i.e. Si dangling bonds) can be attributed to a dissociation of the atomic bonds, e.g. Si-H or Si-O bonds [Hou02, Ush05, Sta06].

5.6   Annealed AlO$_x$/SiN$_x$ stacks on c-Si: Effects of wet-chemical SiO$_x$ interlayer

The effects of a wet-chemical SiO$_x$ interlayer located between the c-Si and the AlO$_x$ on the passivation properties is investigated. For this purpose, a sample consisting of an AlO$_x$/SiN$_x$ stack deposited on a c-Si surface treated with HF and wet-chemical oxidation (HF+Hot-DiW80:HCl) is compared to one with the same stack deposited on a HF-Last c-Si surface as reference. The latter sample was already investigated in the previous section and demonstrated stable fixed negative charges and a well passivated c-Si/(SiO$_x$)/AlO$_x$ interface. The SiO$_x$ interlayer in this case is possibly formed at elevated temperatures like the thermal budged during SiN$_x$ deposition and/or annealing. Therefore the focus in this section will be on the analysis and interpretation of new effects caused by the wet-chemical SiO$_x$ interlayer on the passivation properties after annealing (air, 425 °C, 15 min).
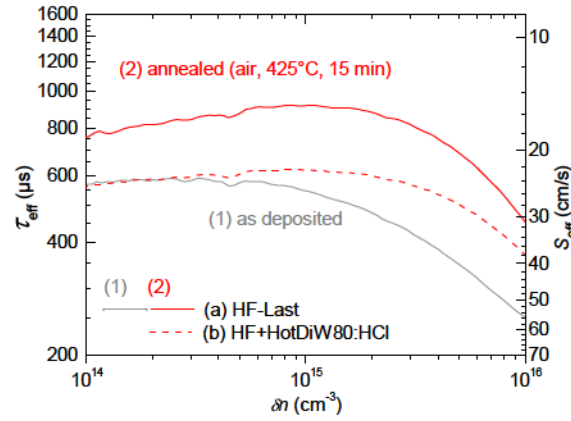

Figure 5.20: Effects of wet-chemical SiO$_x$ interlayer on injection dependent effective minority charge carrier lifetimes τ_{eff} and surface recombination velocities S_{eff}. Highlighted are the HF-Last c-Si (a, red solid line) and HF+Hot-DiW80:HCl c-Si (b, red dashed line) passivated by PECVD-AlO$_x$/SiN$_x$ stacks in the annealed state (2).

Fig. 5.20 demonstrates that the sample with the wet-chemical SiO$_x$ interlayer (HF+Hot-DiW80:HCl) exhibits a lower minority charge carrier lifetime τ_{eff} (higher S_{eff}) than the one with the HF-Last treated c-Si surface. This effect was also observed for the AlO$_x$-single layers (see section 5.3) and is rather surprising, because previous investigations via SPV revealed a better chemical passivation property, i.e. D_{it}, of the wet-chemically oxidized c-Si surface [Laa12]. Therefore, now the goal is to better understand the origin of this reduction of passivation quality by examining the properties of the HF+Hot-DiW80:HCl sample concerning D_{it} and $Q_{ox,eff}$ by means of C-V measurements. These investigations are of interest also for understanding the previous investigations of the annealed AlO$_x$-single layer on c-Si surface treated with HF+Hot-DiW80:HCl as well, where a lower τ_{eff} was observed in comparison to the HF-Last sample (see section 5.3), although the wet-chemical oxidation had led to a decrease of D_{it}.
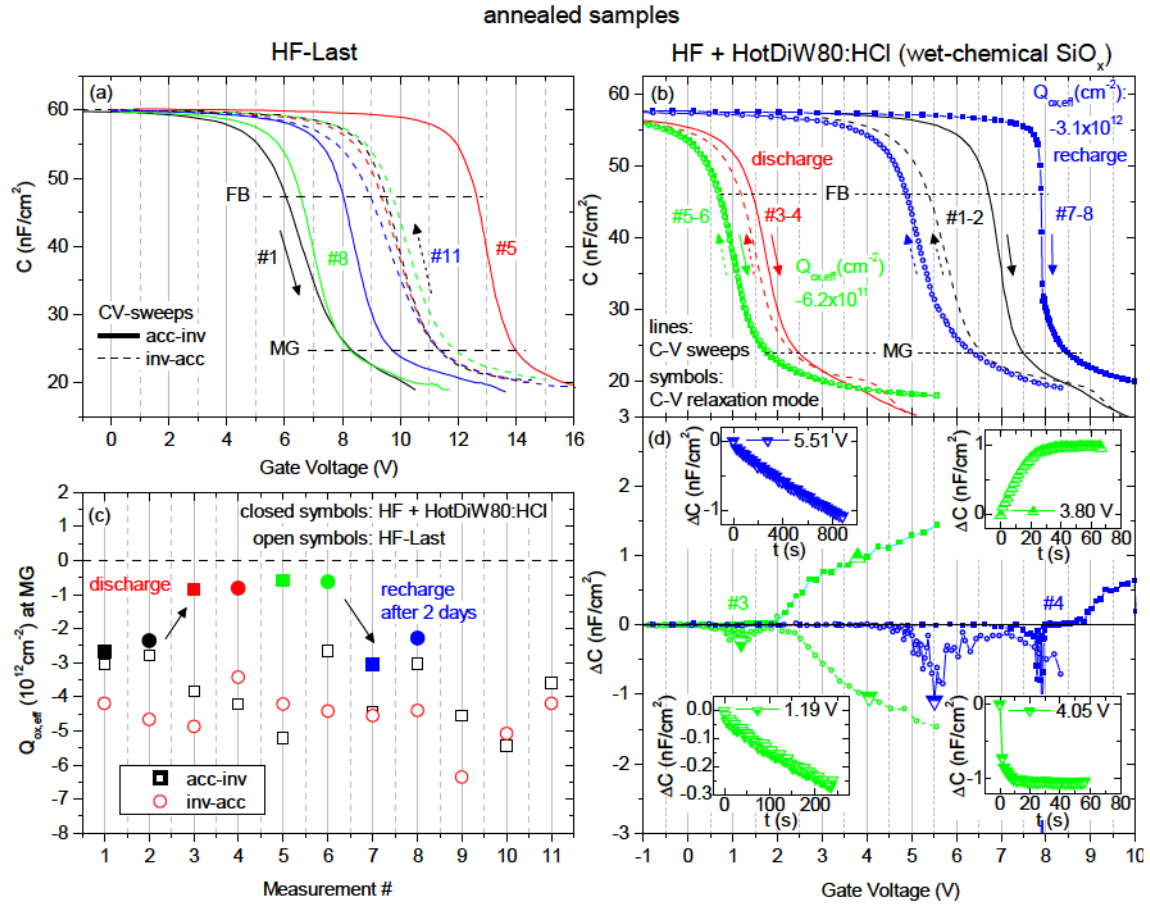
Figure 5.21: High-frequency (1 MHz) capacitance voltage (C-V) curves measured consecutively on MIS structures consisting of (a) HF-Last and (b) HF+Hot-DiW80:HCl c-Si passivated by annealed AlO_x/SiN_x stacks. In (b) C-V measurements were performed in sweep mode (lines, 1-4) and relaxation mode (symbols, 5-6) consecutively, and in relaxation mode 2 days later (symbols, 7-8). (c) Corresponding $Q_{ox,eff}$ at MG obtained from consecutive C-V curves of both samples. (d) Relaxation of capacitance ΔC from (b) vs. gate voltage and selected ΔC-t relaxations (inserts) for selected voltages (single large triangles).

The first C-V experiment aims at the evaluation of the stability of the annealed samples in regard to $Q_{ox,eff}$. The consecutive C-V sweeps of the reference sample (HF-Last) and the corresponding $Q_{ox,eff}$ values (open symbols) are depicted in Fig. 5.21(a) and (c). For comparison, in Fig. 5.21(b) the high frequency C-V curves of the $Si/SiO_x/AlO_x/SiN_x$ structure (HF+Hot-DiW80:HCl) are shown. They reside in the positive bias range indicating that $Q_{ox,eff}$ is negative as expected. The C-V measurements were performed consecutively as numbered on the same metal contact pad of the sample. The measurement direction was alternated starting from accumulation to inversion and vice versa. C-V curves 1-4 (lines) were measured in sweep mode whereas 5-8 (symbols) were measured in relaxation mode. The $Q_{ox,eff}$ values obtained from these C-V curves are also plotted in Fig. 5.21(c) (closed, color-coded symbols) for direct comparison with the reference (HF-Last). In Fig. 5.21(d)

the corresponding relaxation ΔC of capacitance of curves 5-8 is plotted. Positive ΔC-values represent an increase, negative values a decrease of capacitance over time, as depicted by the inserted ΔC-t graphs for selected gate voltages. In Fig. 5.21(b) for curves 1-5, a continuous shift of the C-V curves towards lower voltages, i.e. a continuous reduction of the negative effective charge density $Q_{ox,eff}$, is observed as measurements are simply repeated. Curves 5 and 6, which were measured in relaxation mode, show a negligible hysteresis, suggesting that the MIS structure has reached a nearly stable state where mainly fixed charges and/or stable trapped charges contribute to $Q_{ox,eff}$. The apparently stable effective negative charge density in this case of $Q_{ox,eff} = -6.2 \times 10^{11}\,cm^{-2}$, however, is almost one order of magnitude lower than the negative fixed charge density observed for AlO$_x$-single layer on HF+Hot-DiW80:HCl treated c-Si surface ($Q_{ox,eff} = -4.1 \times 10^{12}\,cm^{-2}$) as well as of the reference AlO$_x$/SiN$_x$ stack on HF-Last c-Si ($Q_{ox,eff} = -4.2 \times 10^{12}\,cm^{-2}$).

In the inversion region a positive (curve 5) and a negative (curve 6) relaxation of capacitance is observed (see representative inserts at 3.80 V and 4.05 V) which can be attributed to the generation and recombination of minority charge carriers, respectively. Hence, a true inversion capacitance is measured and no leakage currents need to be accounted for. The latter observation is crucial as it suggests that only charge injection/ejection from the c-Si and charges in the AlO$_x$/SiN$_x$ can be responsible for the shift of $Q_{ox,eff}$. C-V curve 6 reveals in the depletion region an ongoing decrease of C (see insert for gate voltage 1.19 V). These incomplete relaxations can be attributed to an ongoing decrease of negative charges during the measurement. Two days later, a repetition of the C-V measurement (curve 7, acc - inv) in relaxation mode reveals that $Q_{ox,eff}$ has increased again to $Q_{ox,eff} = -3.1 \times 10^{12}\,cm^{-2}$, i.e. above its initial value. During these two days the sample remained in the dark and contacted, but with the voltage source turned off. However, a gradual decrease of the capacitance in the depletion region (Fig. 5.21(d)) again indicates a decrease of $Q_{ox,eff}$ during the measurement. Measuring in inverse direction (C-V curve 8) reveals a further decrease of $Q_{ox,eff}$. Hence, the reduction of the negative charge seems to be a reversible process. It is worth noting that this behavior was not observed on all investigated gate contact dots that demonstrated insulating characteristics. On another dot of the same sample (HF+Hot-DiW80:HCl) more stable properties where observed. This indicates inhomogeneities of $Q_{ox,eff}$. The following C-V experiments were all performed on this more stable contact pad.

For reference, the V$_{stress}$ experiments of the HF-Last sample are depicted in Fig. 5.22(a) and (c). Fig. 5.22(b) and (d) illustrates representative C-V sweeps and the corresponding $Q_{ox,eff}$ measured upon a constant voltage stress V$_{stress}$ for 400 s on a second metal contact pad of the HF+Hot-DiW80:HCl sample. The C-V sweeps were conducted in both measurement directions (acc-inv and inv-acc) each with a prior V$_{stress}$. The theoretical C-V curve (C$_{th}$) of the corresponding ideal MIS structure (i.e. $D_{it} = 0$ and $Q_{ox,eff} = 0$) is plotted. Starting at V$_{stress}$= 0 V the C-V curves reveal a $Q_{ox,eff} = -4.5 \times 10^{12}\,cm^{-2}$ (see Fig. 5.22(d)), with a negligible hysteresis and therefore in good agreement with the previously demonstrated
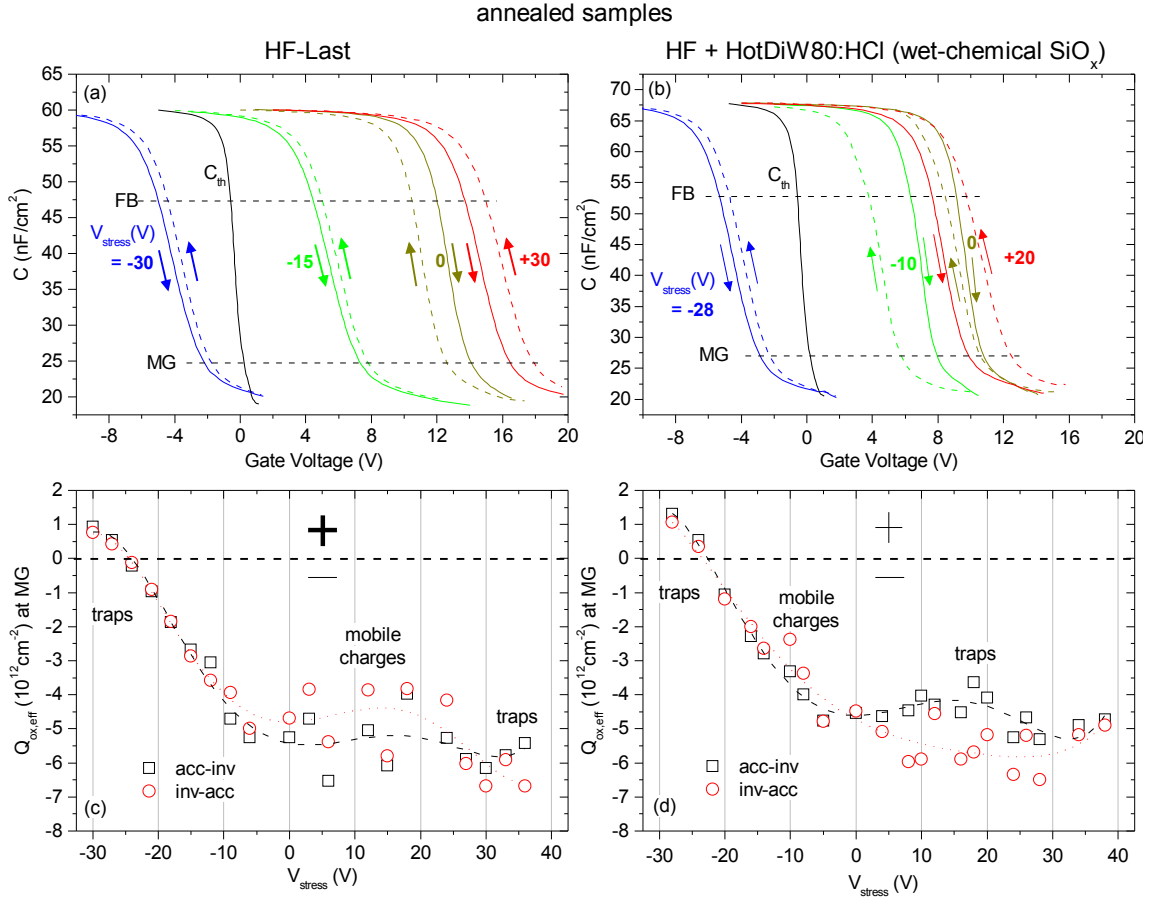
Figure 5.22: High-frequency (1 MHz) C-V curves swept after a prior V$_{stress}$ and the corresponding $Q_{ox,eff}$ at mid gap (MG) of MIS structures consisting of (a) HF-Last and (b) HF+Hot-DiW80:HCl c-Si passivated by annealed AlO$_x$/SiN$_x$ stacks. Arrows indicate the sweep direction (acc-inv or inv-acc) and C$_{th}$ is the referential ideal theoretical C-V curve. (c) and (d) show corresponding $Q_{ox,eff}$ of C-V sweeps of both samples. A counter-clockwise hysteresis indicates charge trapping near the c-Si/(SiO$_x$)/AlO$_x$ interface through charge injection from the c-Si and is referred to as traps. A clockwise hysteresis indicates a charge redistribution in the AlO$_x$ (and SiN$_x$) bulk, which is referred to as mobile charges.

negative fixed charge densities. The small clockwise hysteresis indicates dominant mobile charges in the AlO$_x$/SiN$_x$ stack which also distort the slope of these two C-V curves. Increasing the negative V$_{stress}$ shifts the C-V curves' positive FB and MG voltage values towards lower positive values (for V$_{stress}$ = - 10 V and - 20 V) and then even to negative values (for V$_{stress}$ = - 28 V). The clockwise hysteresis due to charge injection from the Al-gate or to mobile charges becomes larger for V$_{stress}$ = - 10 V. However, for V$_{stress}$ = - 20 V, and - 28 V it changes its orientation to counter-clockwise, indicating dominant charging of traps near the SiO$_x$/AlO$_x$ interface. Applying a positive V$_{stress}$ = + 20 V does not considerably change the FB and MG voltages in comparison to V$_{stress}$ = 0 V, however, it reveals a relatively large counter-clockwise hysteresis for charged traps. In

Fig. 5.22(d) $Q_{ox,eff}$ is calculated at the mid gap (MG) voltage for a larger selection of C-V sweeps including the ones in Fig. 5.22(b). Here, the hysteresis orientation is reflected in the values of $Q_{ox,eff}$ for the different measurement directions (acc-inv and inv-acc). Increasing negative V$_\mathrm{stress}$ leads to two effects: 1. a continuous reduction of negative $Q_{ox,eff}$ due to a positive charging of traps (or electron detrapping) near the interface. 2. up to V$_\mathrm{stress}$ = - 16 V the $Q_{ox,eff}$ values for the two measurement directions reflect a hysteresis formed due to traps charging at the SiN$_\mathrm{x}$/Al-gate interface or mobile charges in particular in the AlO$_\mathrm{x}$-bulk. As for the HF-Last sample, it is more likely that the latter effect, in particular charge redistribution in the AlO$_\mathrm{x}$, is the main cause for this clockwise hysteresis orientation for the following reasons: Firstly, this effect takes place closer to the c-Si/AlO$_\mathrm{x}$ interface and therefore has a greater influence on $Q_{ox,eff}$ (see section 4.5). Secondly, due to the high trap density in the AlO$_\mathrm{x}$ bulk (causing the leakage currents), charges may be redistributed more easily through trap-assisted transport. Hence, it can be assumed that for low negative V$_\mathrm{stress}$ electrons inside the AlO$_\mathrm{x}$ drift near the c-Si/SiO$_\mathrm{x}$/AlO$_\mathrm{x}$ interface and therefore affect hysteresis formation more efficiently. However, this is an assumption that requires additional investigations (e.g. quantitative calculations). Therefore, the possibility that charge trapping at the SiN$_\mathrm{x}$/Al-gate interface may influence this hysteresis should not yet be completely disregarded.

Increasing negative V$_\mathrm{stress}$ > - 16 V further decreases the negative $Q_{ox,eff}$ until even its polarity changes and $Q_{ox,eff}$ becomes positive, similar to the HF-Last sample. A hysteresis due to trap charging appears, supporting the hypothesis that the change of polarity of $Q_{ox,eff}$ is due to positive charging of traps (or electron detrapping) for negative V$_\mathrm{stress}$.

Subsequently applying a positive V$_\mathrm{stress}$ > 0 V leads to an average effective oxide charge density of $Q_{ox,eff} = -(5.0 \pm 1.5) \times 10^{12}\,cm^{-2}$, which remains constant. Here, in contrast to the HF-Last sample, all hysteresis orientations can clearly be attributed to the charging of traps through charge injection from the Si. In principle, these charged traps could be located near the c-Si/SiO$_\mathrm{x}$/AlO$_\mathrm{x}$ interface, in the AlO$_\mathrm{x}$ bulk, or near the AlO$_\mathrm{x}$/SiN$_\mathrm{x}$ interface. For positive V$_\mathrm{stress}$ > 30 V the hysteresis diminishes, indicating a more fixed charge-like character. This fixed charge-like character may be an indication that defects/traps deeper inside the AlO$_\mathrm{x}$ bulk or near the AlO$_\mathrm{x}$/SiN$_\mathrm{x}$ interface are being charged negatively. However, the fact that both annealed samples exhibit hysteresis formation with opposite orientations at positive V$_\mathrm{stress}$, indicates that the wet-chemical oxidation introduces more traps, which must then be located at or near the wet-chemical SiO$_\mathrm{x}$/AlO$_\mathrm{x}$ interface. In fact, their close proximity to the c-Si makes them more susceptible to charge injection from the Si. Therefore, these additional traps may be responsible for the instabilities of $Q_{ox,eff}$ at some locations on the HF+Hot-DiW80:HCl sample.

In regard to the chemical passivation, previous SPV-investigations showed that the c-Si surface defect density is reduced upon a wet-chemical oxidation forming a ~1.5 nm thick SiO$_\mathrm{x}$ layer [Laa12]. The following C-V experiments aim at investigating the effect of the HF+Hot-DiW80:HCl treatment on the chemical passivation of the AlO$_\mathrm{x}$/SiN$_\mathrm{x}$ stack. The
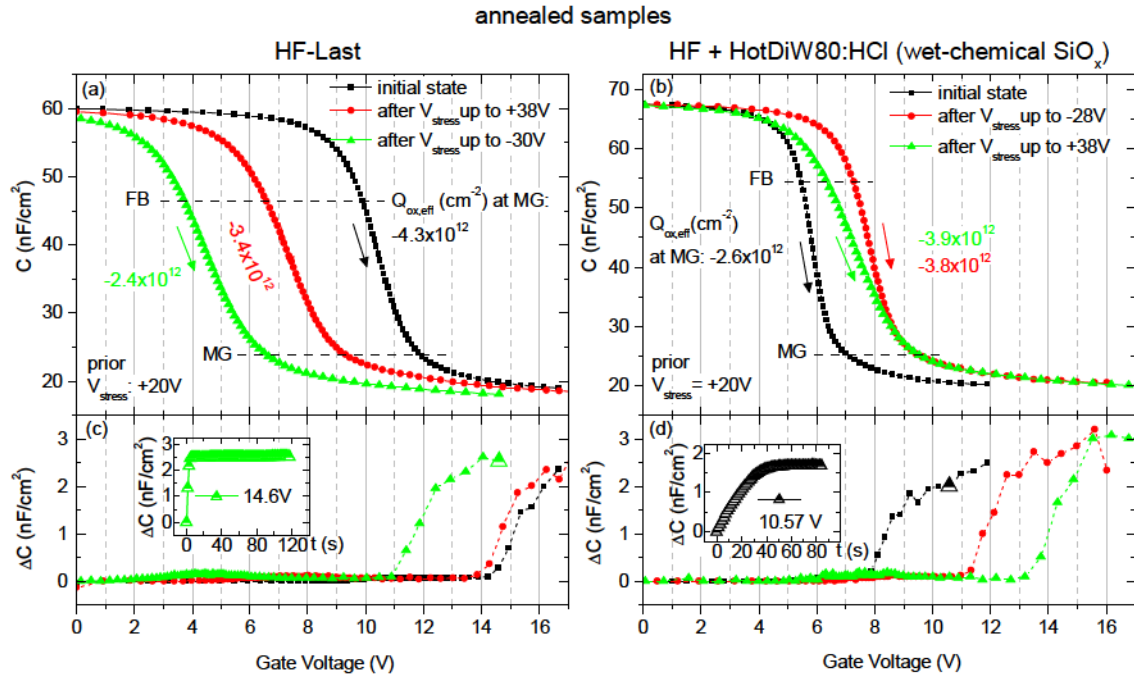
Figure 5.23: High-frequency (1 MHz) C-V measurements in relaxation mode and the corresponding relaxation capacitance ΔC over gate voltage of MIS structures consisting of (a+c) HF-Last and (b+d) HF+Hot-DiW80:HCl c-Si passivated by annealed AlO$_x$/SiN$_x$ stacks. C-V curves were measured following a V$_{stress}$ of + 20 V (> 400 s) for charge stabilization. Inserts illustrate exemplary ΔC-t traces at the indicated gate voltage. C-V measurements were performed before (initial state) and after negative and positive V$_{stress}$ experiments.

V$_{stress}$ experiments showed that the charge state of the SiO$_x$/AlO$_x$/SiN$_x$ stack can be manipulated. Hence, by applying a relatively low V$_{stress}$ of + 20 V for > 400 s until a constant inversion capacitance (C$_{inv}$) is reached a stable equilibrium state in the MIS structure can be created: negative mobile charges drift away from the interface and traps near the c-Si/SiO$_x$/AlO$_x$ interface are charged negatively. In this state high frequency C-V measurement in relaxation mode were performed from accumulation to inversion as depicted in Fig. 5.23(b) with their corresponding ΔC relaxation analysis (d). For reference, the results of the HF-Last sample are depicted in Fig. 5.23(b) and (d). These measurements were conducted before (initial state), after the negative and then after the positive V$_{stress}$ investigations. Up to the MG voltage the relaxation analysis shows negligible temporal changes of ΔC, hence the MIS structure is in a stable equilibrium state during the measurement. Beyond the MG voltage the typical relaxations due to the generation of minority charge carriers are observed (see insert in Fig. 5.23(d) at 10.57 V). In contrast to the HF-Last sample, the HF+Hot-DiW80:HCl sample exhibits a slight increase of $Q_{ox,eff}$ upon the V$_{stress}$ experiments.

The obtained D_{it}-spectra are depicted in Fig. 5.24. Due to the low relaxations in depletion and due to the obtained true C$_{inv}$ the D_{it}-spectra can be considered as reliable, reflecting the
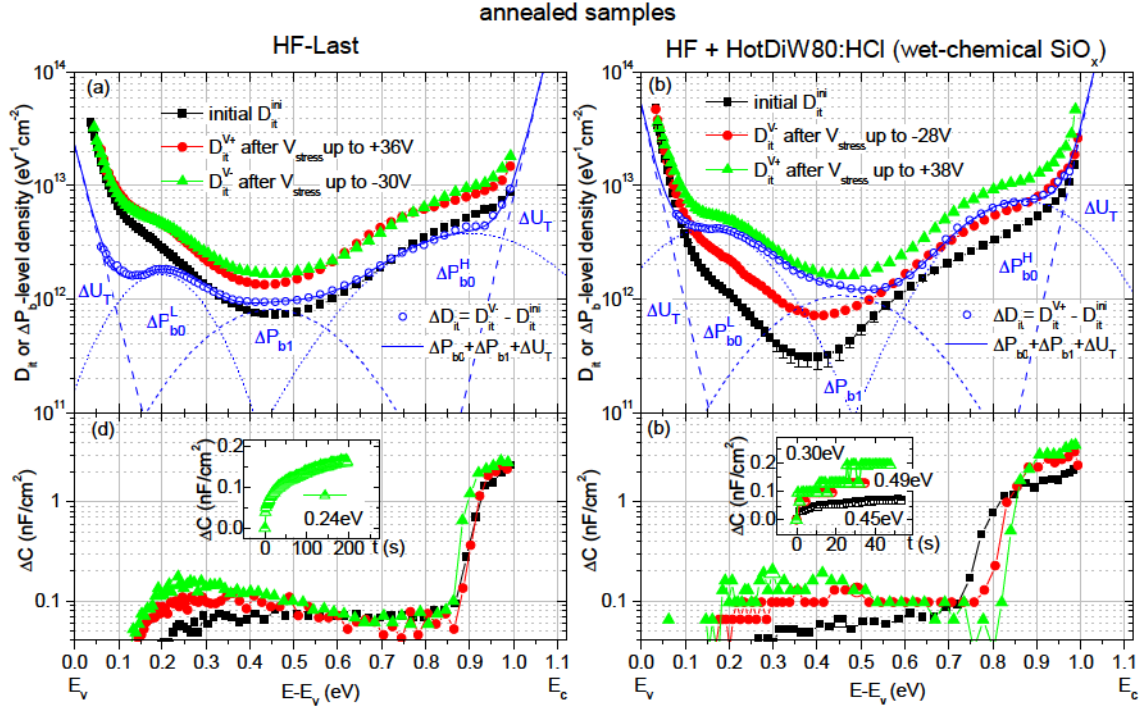
Figure 5.24: Defect state density (D_{it}) at the c-Si/(SiO$_x$)/AlO$_x$ interface over the c-Si band gap of MIS structures consisting of (a) HF-Last and (b) HF+Hot-DiW80:HCl c-Si passivated by annealed AlO$_x$/SiN$_x$ stacks. (c) and (d) show corresponding relaxation ΔC-spectra. D_{it}-spectra were obtained before (initial state) and after negative and positive V$_{stress}$ experiments. The generated defect state ΔD_{it}-spectra were fitted by the sum of Gaussian distributions for generated ΔP_{b0}- and ΔP_{b1}-like defects and exponential functions for strained bond defects ΔU_T.

defect state density at the Si/wet-chemical SiO$_x$ interface. Comparing the two initial D_{it}-spectra reveals that the sample with the wet-chemical SiO$_x$ interlayer exhibits a considerably lower interface defect state density, in particular in the lower part of the spectrum. This is in agreement with the results obtained via SPV [Laa12]. Upon the negative V$_{stress}$ experiments up to - 28 V, D_{it} increases over the whole spectrum. A further increase is observed after the subsequent positive V$_{stress}$ investigations up to + 38 V. To analyze this overall increase the difference is calculated and fitted by three Gaussian distributions. As for the reference sample, their energetic positions are in good agreement with those reported for P$_{b0}$ and P$_{b1}$ defects at the c-Si/SiO$_x$ interface. The increase of the band tails U$_T$ was fitted with exponential functions. This indicates that the large V$_{stress}$ apparently breaks and strains atomic bonds at the c-Si/SiO$_x$ interface, creating additional intrinsic P$_{b0}$ and P$_{b1}$-like dangling bond defects as well as strained bond defects U$_T$. This leads to a voltage stress induced degradation of the chemical passivation.

For a more detailed analysis of this degradation, the D_{it}-spectra in the initial state, after negative and after positive V$_{stress}$ experiments were fitted individually by Gaussians of
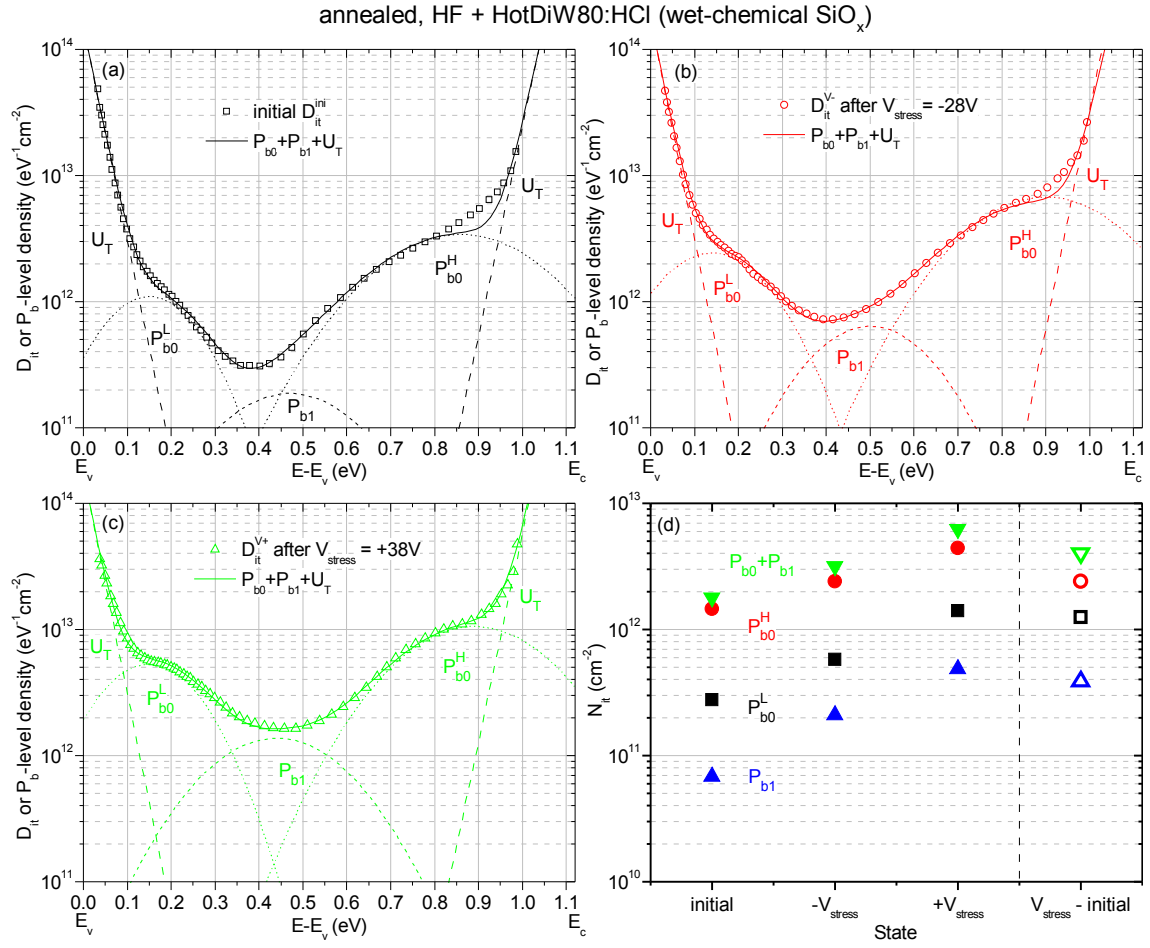
Figure 5.25: (a-c) D_{it}-spectra of annealed AlO$_x$/SiN$_x$ stack on wet-chemically oxidized (HF+Hot-DiW80:HCl) c-Si obtained before (initial state) and after negative and positive V$_{stress}$ experiments. D_{it}-spectra were fitted individually by the sum of Gaussian distributions for P$_{b0}$- and P$_{b1}$-like defects and exponential functions for strained bond defects ΔU$_T$. (d) Defect density N_{it} obtained from the area of the corresponding Gaussians of P$_{b0}$- and P$_{b1}$-like defects as well as for generated ones (ΔN_{it}) upon V$_{stress}$ experiments.

the different defect types. The results are shown in Fig. 5.25(a), (b) and (c), respectively. Fig. 5.16(d) depicts N_{it} (i.e. area of Gaussians) of the individual defects types P$_{b0}$(black and red closed symbols), P$_{b1}$(blue closed symbols), and their sum P$_{b0}$+P$_{b1}$(green closed symbols) as well as the generated ones (corresponding open symbols) for the different states. The fitting parameters, energetic position (E-E_v) and width (w) of the Gaussians, are shown in Fig. 5.26. The energetic positions of all Gaussians are nearly identical for all states. Minor adjustments had to be done in regard to their width. Only the widths of the P$_{b0}$-Gaussians of the ΔD_{it}-spectrum underwent larger corrections, most probably due to its larger absolute error.

Nevertheless, the consistent fitting results support the reliability of the fitted spectra and their interpretation. Hence, one can make a reliable quantitative comparison of N_{it}:
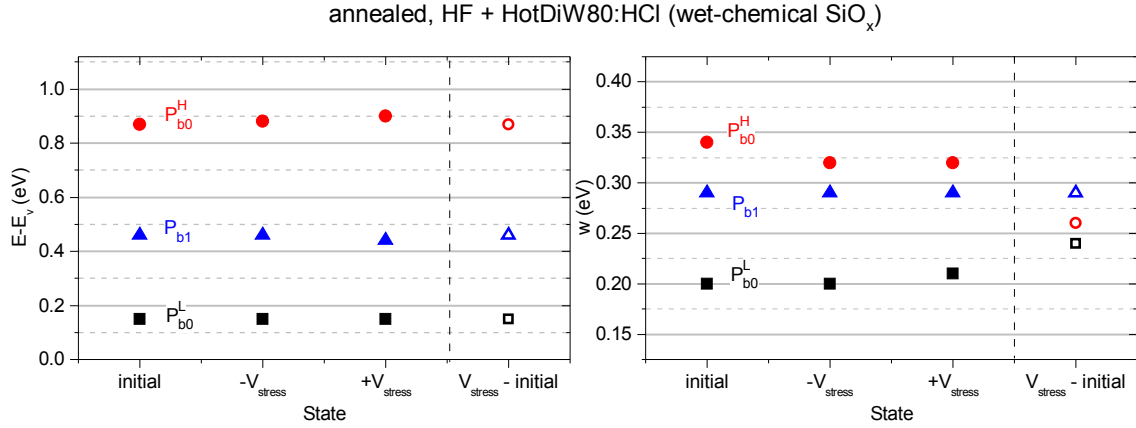
Figure 5.26: Energetic position in c-Si band gap (E-E_v, left graph) and width (w, right graph) of Gaussians for P$_{b0}$- and P$_{b1}$-like defects used for fitting of experimental D_{it}-spectra of annealed sample in Fig 5.16.

The integration of a wet-chemical SiO$_x$-interlayer reduces the integrated interface defect density in the initial state from $N_{it} = 2.9 \times 10^{12}\,cm^{-2}$ (HF-Last) to $N_{it} = 1.8 \times 10^{12}\,cm^{-2}$ (HF+Hot-DiW80:HCl). This reduction, however, does not correlate with the decrement of lifetime, i.e. increase of S_{eff} (Fig. 5.20). Therefore, the instabilities and inhomogeneities in regard to $Q_{ox,eff}$ that arise from the additional traps at the wet-chemical SiO$_x$/AlO$_x$ interface most probably influence the field-effect passivation.

Assuming that $S_{eff} \sim N_{it}/Q_{ox}^2$ [Din12b], the following assessment can be done: In Fig. 5.20 an increase of S_{eff} by a factor of ~1.5 (at $\delta n = 10^{15}\,cm^{-2}$) is observed upon integration of the wet-chemical SiO$_x$ interlayer. This increase of S_{eff} in conjunction with a decrease of N_{it} by a factor of ~1.5 (see discussion above), is achieved if Q_{ox} decreases by a factor of ~1.5. Due to charge injection and trapping from the c-Si, $Q_{ox,eff}$ of the SiO$_x$/AlO$_x$/SiN$_x$ stack deviates on some locations of the sample almost within one order of magnitude (Fig. 5.21(b)). Therefore, a decrease of the average Q_{ox} by a factor of ~1.5 due to inhomogeneities is a reasonable explanation.

5.7 As deposited wet-chemical $SiO_x/AlO_x/SiN_x$ stacks: Effects of firing

In this section the effects of firing (air, 860 °C, ~3 s) with reference to an as deposited AlO_x/SiN_x stack on HF+Hot-DiW80:HCl treated c-Si are investigated. It is worth noting that in the case of these samples only a few gate contact dots could be found with an insulating AlO_x/SiN_x stack. Those few dots fulfilled the conditions for a reliable characterization via C-V measurements. However, they were found not to be stable towards the previously investigated range of V_{stress}. Inhomogeneities of the initial $Q_{ox,eff}$, possibly due to traps at the wet-chemical SiO_x/AlO_x interface, were observed for these samples and most gate contacts dots that were initially insulating revealed leakage currents upon V_{stress} in the course of the investigations. It should be noted that these instabilities do not reflect the passivation quality but rather its applicability for reliable C-V measurements.
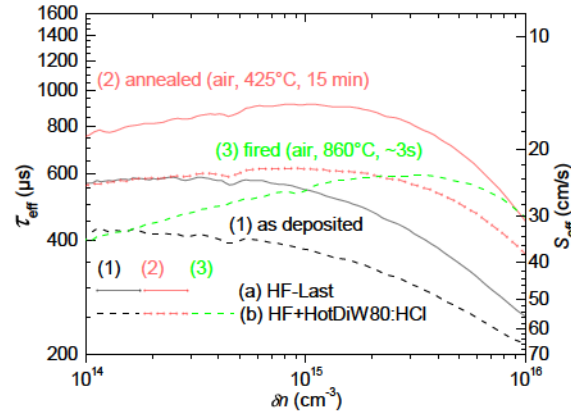

Figure 5.27: Injection dependent effective minority charge carrier lifetimes τ_{eff} and surface recombination velocities S_{eff}. Highlighted are the HF+Hot-DiW80:HCl c-Si passivated by PECVD-AlO_x/SiN_x stacks in the as deposited state (black, dashed line) and after direct firing (green, dashed line).

In Fig. 5.27 the as deposited (black, dashed line) and fired (green, dashed line) AlO_x/SiN_x stack on HF+Hot-DiW80:HCl treated c-Si are shown. First, comparing the as deposited HF+Hot-DiW80:HCl sample with the HF-last one (black, solid line) reveals a reduction of lifetime τ_{eff}, same as for the annealed samples (red lines). The firing leads to an increase of lifetime τ_{eff} (decrease of S_{eff}) particularly in the high injection region.

Fig. 5.28(a) and (c) depict the initial C-V sweeps and the corresponding $Q_{ox,eff}$ of the as deposited sample. All C-V sweeps reveal a stable state with minor hysteresis formation for trap charging found in the negative gate voltage region. This results in a positive $Q_{ox,eff} \sim 6 \times 10^{11}\, cm^{-2}$, indicating that the activation of the negative charges due to the thermal budget during SiN_x deposition did not take place. However, another second contact dot on the same sample indeed revealed a negative charge density $Q_{ox,eff} \sim -1.8 \times 10^{12}\, cm^{-2}$ (see semitransparent triangles in Fig. 5.28(c)). This implies
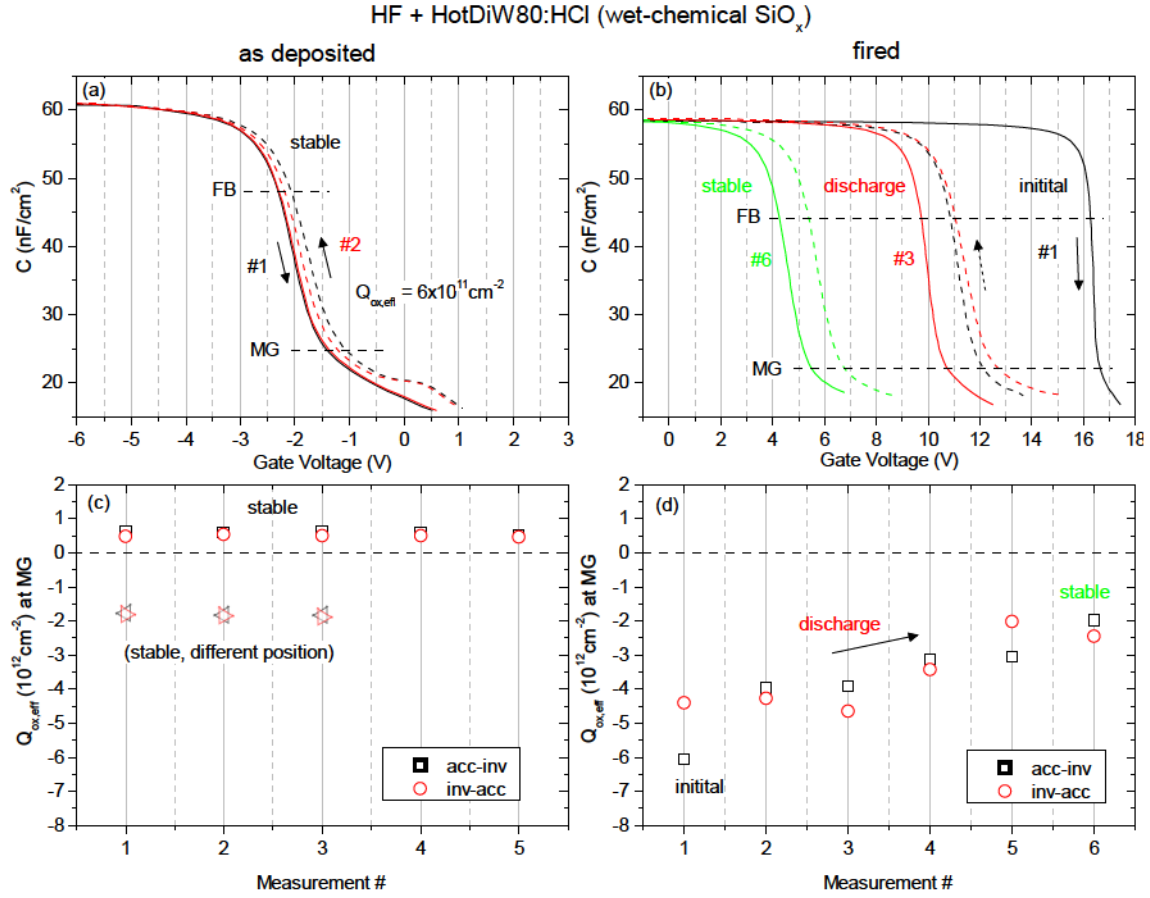
Figure 5.28: Consecutively measured high-frequency (1 MHz) C-V sweeps and the corresponding $Q_{ox,eff}$ at mid gap (MG) of as deposited (a+c) and fired samples (b+d) AlO_x/SiN_x stack on HF+Hot-DiW80:HCl c-Si. Arrows indicate the sweep direction (acc-inv or inv-acc). The stability of $Q_{ox,eff}$ is investigated. In (c) $Q_{ox,eff}$ obtained at a different location of the as deposited sample is indicated (semi-transparent triangles) demonstrating inhomogeneity of sample.

again an inhomogeneity in regard to $Q_{ox,eff}$. The measurements on this first dot, however, sustained most of the following V_{stress} measurements and thus serve for a rather qualitative than a quantitative evaluation of the as deposited sample with SiO_x interlayer. It is representative for locations on the sample that probably lead to this inhomogeneity of $Q_{ox,eff}$ and thus of the passivation quality. The fired sample (5.28(b) and (d)) reveals at its first CV-sweep a relatively high $Q_{ox,eff} = -6 \times 10^{12}\,cm^{-2}$. However, this initial relatively high $Q_{ox,eff}$ is reduced continuously during consecutive C-V sweeps and reaches a stable state at $Q_{ox,eff} = -2 \times 10^{12}\,cm^{-2}$. This indicates a detrapping of negative charges, similar to the as deposited HF-last sample that resulted in considerably lower $Q_{ox,eff}$.

In fact, the implied inhomogeneities of passivation quality of both, the as deposited as well as the fired sample, were verified through spatially resolved minority charge lifetime measurements performed via the µ-photoconductance decay (µ-PCD) method. These new lifetime samples were prepared under same process conditions as the ones investigated here
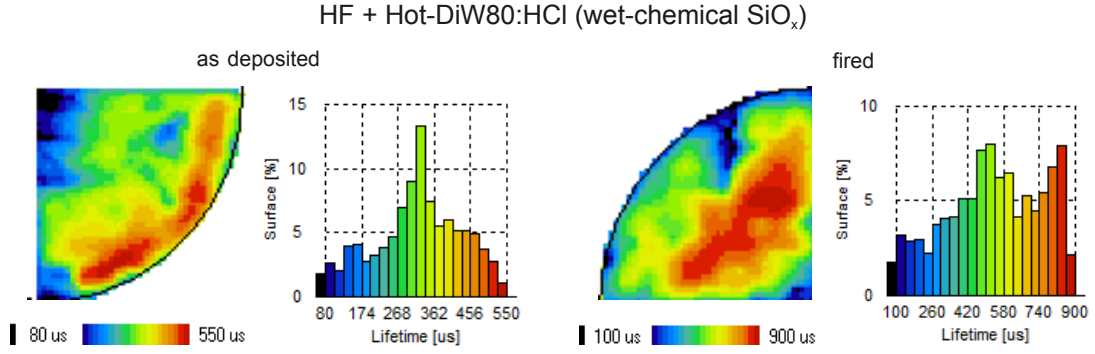
Figure 5.29: Spatial distribution of minority charge carrier lifetime of the HF+Hot-DiW80:HCl c-Si passivated by PECVD-AlO$_x$/SiN$_x$ stacks in the as deposited state and after firing. Lifetime was measured via μ-PCD.

via C-V. The lifetime-maps are depicted in Fig. 5.29. Here, the fired sample demonstrates an increased average lifetime compared to the as deposited one. This is in agreement with the injection dependent QSSPC measurements in Fig 5.27. However, the spatial distribution of the lifetime indicates that the firing process activated the passivation mainly at the center of the sample. As the C-V measurements suggest, at these locations traps were charged negatively enhancing the field-effect passivation.

As can be seen in Fig. 5.30(a) and (c) for the as deposited sample, applying a positive V$_{stress}$ leads first to a change of polarity and then to an increase of negative $Q_{ox,eff}$ of the SiO$_x$/AlO$_x$/SiN$_x$ stack. The counter-clockwise hysteresis reveals that this negative $Q_{ox,eff}$ arises from negative charge injection from the c-Si into traps in the SiO$_x$/AlO$_x$/SiN$_x$ stack. In the case of the fired sample (Fig. 5.30(b) and (d)), the initially negative $Q_{ox,eff}$ is inverted by a negative V$_{stress}$, whereas a positive V$_{stress}$ enhances the negative charge density up to $Q_{ox,eff} \sim -6 \times 10^{12} \, cm^{-2}$ for V$_{stress}$ = + 39 V, apparently reaching an upper limit. Unambiguous counter-clockwise hysteresis formation reveals trap charging to be the cause for the negative charge of the fired sample as well. At this point, however, V$_{stress}$ exceeded the breakdown voltage and caused leakage currents. Hence, reliable C-V investigation could not be continued for this gate contact dot, since leakage currents for these structures led to a drop of the accumulation capacitance and to a loss of control over $Q_{ox,eff}$ through V$_{stress}$.

In its initial state, the as deposited sample did not require a prior V$_{stress}$ (usually + 20 V) in order to obtain a stable charge state for a reliable C-V measurement in relaxation mode. The relaxation mode is required for the determination of the initial D_{it}. The resulting C-V curve from accumulation to inversion and the corresponding relaxation capacitance ΔC are depicted in Fig. 5.31(a) and (c), respectively. ΔC-V reveals minor negative charging in the depletion region, whereas in the inversion region a true inversion capacitance is obtained due to the complete generation of minority charge carriers, as can be seen in the inserted ΔC-t graphs. In the initial state, $Q_{ox,eff} = 6.5 \times 10^{11} \, cm^{-2}$ is identical
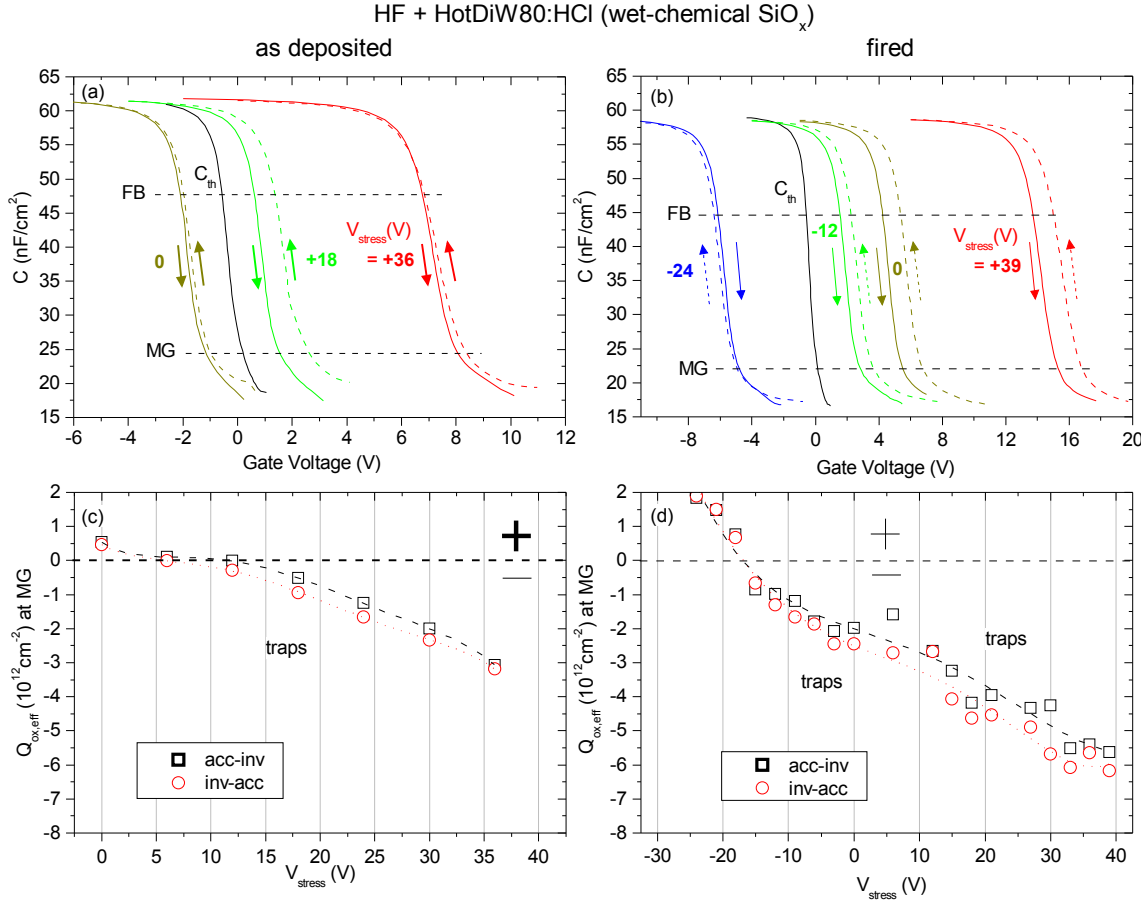
Figure 5.30: High-frequency (1 MHz) C-V curves swept after a prior V$_{stress}$ and the corresponding $Q_{ox,eff}$ at mid gap (MG) of MIS structures consisting of (a) as deposited and (b) fired AlO$_x$/SiN$_x$ stacks on wet-chemically oxidized (HF+Hot-DiW80:HCl) c-Si. Arrows indicate the sweep direction (acc-inv or inv-acc) and C$_{th}$ is the referential ideal theoretical C-V curve. (c) and (d) show corresponding $Q_{ox,eff}$ of C-V sweeps of both samples. A counter-clockwise hysteresis indicates charge trapping near the c-Si/(SiO$_x$)/AlO$_x$ interface through charge injection from the c-Si and is referred to as traps.

to the positive charge of the initial C-V sweeps (Fig. 5.28(c)). However, following the positive V$_{stress}$ experiments the charging properties change, resulting in a stable state at $Q_{ox,eff} = -1.9 \times 10^{12}\, cm^{-2}$, similar to $Q_{ox,eff}$ measured at other contact dots. This demonstrates that the negative charges injected upon the positive V$_{stress}$ experiments are in a stable trapped state in the SiO$_x$/AlO$_x$/SiN$_x$ stack. This stable $Q_{ox,eff}$ of the as deposited sample is the same as the stable $Q_{ox,eff}$ of the fired sample which was obtained due to discharge/detrapping of negative charges upon consecutive C-V sweeps (Fig. 5.28(d)).

Prior to C-V measurement in relaxation mode of the fired sample, a relatively low V$_{stress}$ = + 18 V was applied. The resulting C-V curves in the initial state and after V$_{stress}$ experiments with the corresponding relaxations ΔC are depicted in Fig. 5.31(b) and (d). In the initial case, slight relaxations in accumulation near flat band (FB) reveal
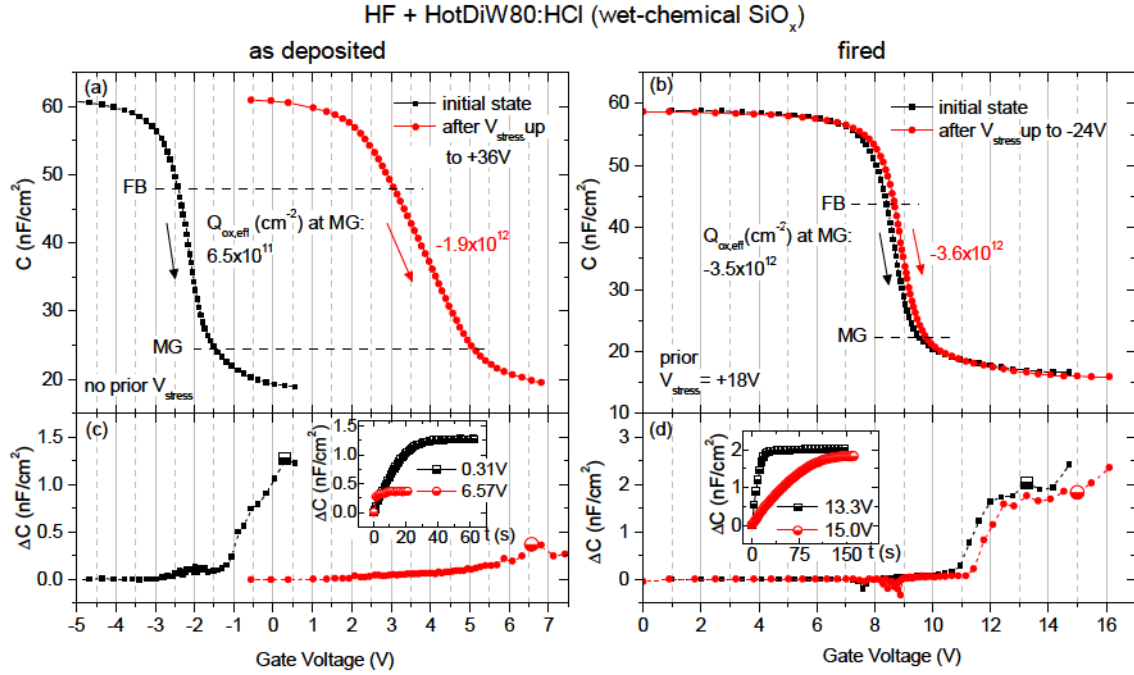
Figure 5.31: High-frequency (1 MHz) C-V measurements in relaxation mode and the corresponding relaxation capacitance ΔC over gate voltage of MIS structures consisting of (a+c) HF-Last and (b+d) HF+Hot-DiW80:HCl c-Si passivated by annealed AlO_x/SiN_x stacks. Inserts illustrate exemplary ΔC-t traces at the indicated gate voltage. C-V measurements were performed before (initial state) and after negative and positive V_{stress} experiments.

detrapping of negative charges. This discharge ceases quickly and becomes negligible in the depletion region, indicating that with $Q_{ox,eff} = -3.5 \times 10^{12}\,cm^{-2}$ a stable state is reached, very similar to $Q_{ox,eff}$ for $V_{stress} = +18$ V (Fig. 5.30(d)). Hence, the charge state obtained indeed is stable and reproducible through V_{stress}. The C-V measurement in relaxation mode (also with a prior $V_{stress} = +18$ V) which results in $Q_{ox,eff} = -3.6 \times 10^{12}\,cm^{-2}$ as well after the negative V_{stress} experiments confirm this assumption. However, this is in contrast to the initial unstable charge measured by the first C-V sweep (Fig. 5.28). Therefore, it can be concluded that upon firing traps near the c-Si/SiO_x/AlO_x interface are negatively charged and therefore more susceptible to detrapping into the c-Si, whereas upon V_{stress}, traps deeper inside the $SiO_x/AlO_x/SiN_x$ stack become negatively charged attaining a more stable state.

The D_{it}-spectra of both the as deposited and the fired sample are depicted in Fig. 5.32 together with the corresponding ΔC-spectra. The initial D_{it} of the as deposited sample is clearly lower than of the fired one, and also lower than of all other investigated samples, over the entire c-Si band gap. This is the case even when taking the higher relative error due to the discharges into consideration. The estimated $N_{it} \sim 7.5 \times 10^{11}\,cm^{-2}$ reflects the low interface defect state density obtained through the wet-chemical oxide [Laa12, Ang04]. Following the positive V_{stress} experiments a considerable increase of D_{it} is evident in
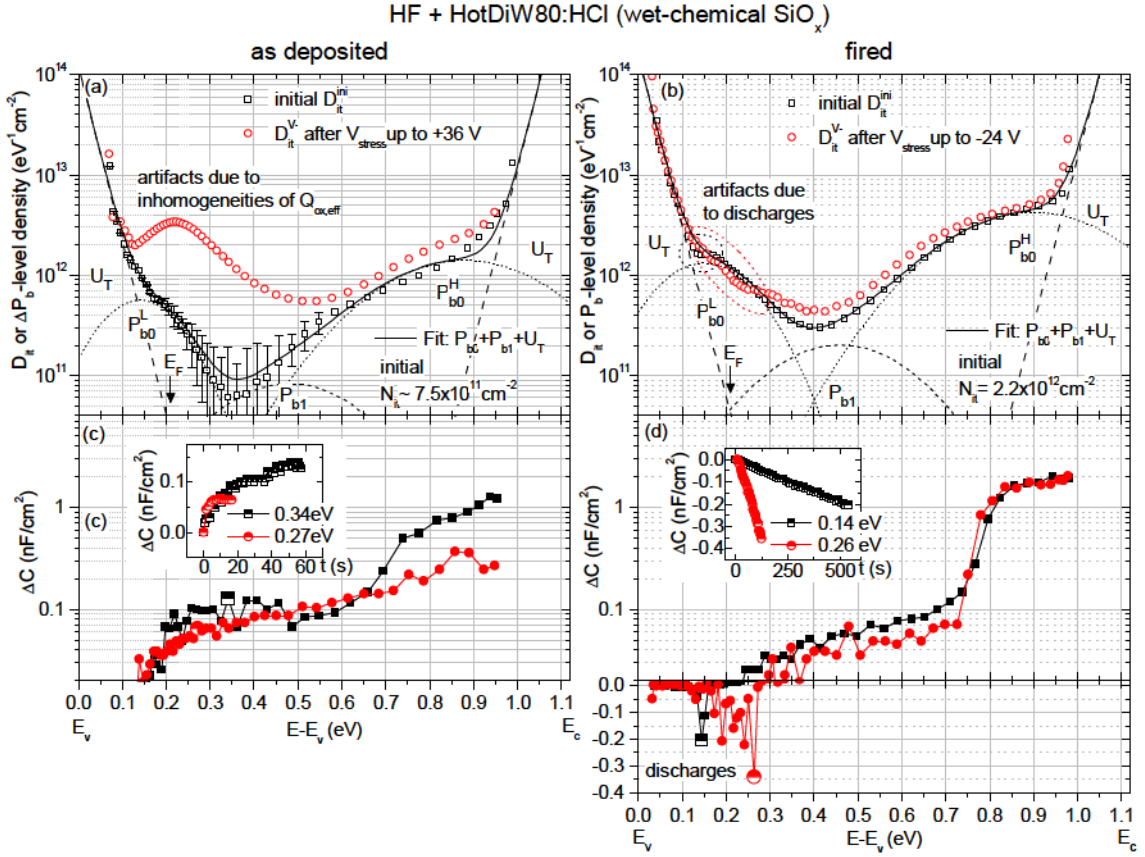
Figure 5.32: Defect state density (D_{it}) at the c-Si/SiO$_x$/AlO$_x$ interface over the c-Si band gap of as deposited (a) and annealed (b) sample with corresponding relaxation ΔC-spectra (c,d). D_{it}-spectra were obtained before (initial state) and after negative and positive V$_{stress}$ experiments. The D_{it}-spectra were fitted by the sum of Gaussian distributions for P$_{b0}$- and P$_{b1}$-like defects and exponential functions for strained bond defects U$_T$.

particular in the lower part of the Si band gap. The spectrum of the generated defects ΔD_{it} can be fitted by the sum of Gaussians representing additional P$_{b0}$- and P$_{b1}$-like defects. However, one needs to consider that the corresponding measured C-V curve is in a state at which $Q_{ox,eff}$ is defined by charged traps. Therefore, it is most likely that inhomogeneities in $Q_{ox,eff}$ have an influence on the D_{it} spectrum. This may be the case for the D_{it}-peak located at 0.21 eV near the Fermi-level E$_f$, since this peak is similar to the one for the thermal SiO$_2$ of 15 nm thickness in Fig. 4.6, also near E$_f$ and originates from inhomogeneities in $Q_{ox,eff}$.

In the case of the fired sample, negative relaxations (see inserts) near E$_f$ in Fig. 5.32(d) lead to slight distortions in the D_{it}-spectra in Fig. 5.32(b) near the conduction band edge. However, the main part of the spectra can be considered reliable since the error due to the slight positive relaxations from 0.3 eV up to 0.7 eV is negligible for the corresponding D_{it}-values. The increase of initial D_{it} in comparison to the as deposited sample can be attributed to the dissociation of hydrogen upon thermal treatment. The resulting

$N_{it} = 2.2 \times 10^{12}\,cm^{-2}$ is similar to the one of the annealed sample which also incorporated a wet-chemical SiO$_x$ interlayer (Fig. 5.25(d), $N_{it} = 1.8 \times 10^{12}\,cm^{-2}$). Upon negative V$_{stress}$ experiments on the fired sample, only a minor degradation of the chemical passivation is observed. This is associated to the lower maximum V$_{stress}$ = -24 V (usually -28 V) applied in this case, which was sufficient to considerably charge the SiO$_x$/AlO$_x$/SiN$_x$ stack positively (see Fig. 5.30(d)), however, not to induce an extensive generation of defects.

Based on these observations the enhancement of τ_{eff} , i.e. the reduction of S_{eff}, upon firing can be explained qualitatively as follows: the firing process leads to a negative charging of the traps in the SiO$_x$/AlO$_x$/SiN$_x$ stack, most likely near the SiO$_x$/AlO$_x$ interface. This initial charged state of $Q_{ox,eff} = -6 \times 10^{12}\,cm^{-2}$ leads to an enhancement of the field-effect passivation, which in this case has greater influence on the lifetime than the degradation of chemical passivation. Its initial charge state, however is not stable, and is reduced upon relative low potentials causing a detrapping and discharge of the initial charge state. The resulting lower charge state of $Q_{ox,eff} = -2 \times 10^{12}\,cm^{-2}$ can be either attributed to fixed charges, e.g. more stable charged traps activated during the firing process. The latter assumption is supported by the measurements of the as deposited sample, where a similar stable $Q_{ox,eff} = -1.9 \times 10^{12}\,cm^{-2}$ is obtained upon charging initially positive states negatively by applying a positive V$_{stress}$.

5.8 Fired SiO$_x$/AlO$_x$/SiN$_x$ stacks: Effects of RCA cleaning

In this section the effects of RCA cleaning on the passivation quality upon firing of the SiO$_x$/AlO$_x$/SiN$_x$ stack are investigated. The RCA cleaning was performed prior to the HF-treatment, followed by a wet-chemical oxidation (Hot-DiW80:HCl), the AlO$_x$/SiN$_x$ stack deposition and the firing step. The sample which underwent the additional RCA cleaning is compared to the one without RCA cleaning as reference. The latter was subject to C-V investigations in the previous section.
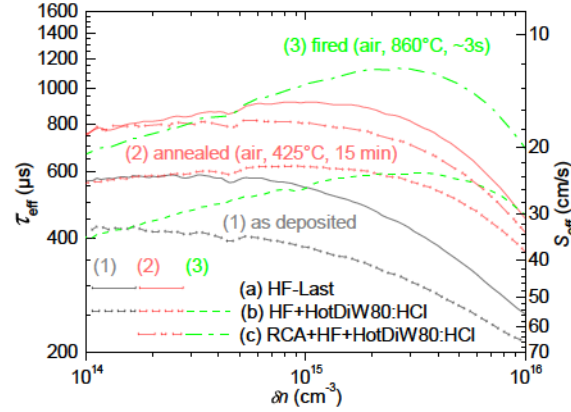

Figure 5.33: Injection dependent effective minority charge carrier lifetimes τ_{eff} and surface recombination velocities S_{eff}. The samples without (green, dashed line) and with RCA-cleaning (green, dot-dashed line) of the Si surface, both followed by HF-treatment, wet-chemical oxidation (Hot-DiW80:HCl), deposition of AlO$_x$/SiN$_x$ stacks and direct firing are shown.

As can be seen in Fig. 5.33 (and also in Fig. 5.2(b)) this treatment with prior RCA-cleaning, combined with HF and wet-chemical oxidation (HF+Hot-DiW80:HCl) and a firing step, led to the highest passivation quality in regard to τ_{eff} and S_{eff} of all investigated (SiO$_x$)/AlO$_x$/SiN$_x$ stacks. It surpasses the passivation quality of the annealed HF-last sample which revealed higher lifetimes than its counterpart with RCA+HF+Hot-DiW80:HCl. Therefore, investigating the fired samples is of particular interest also for solar cell application since these lifetime measurements suggest that the annealing process may not be necessary. In fact, to avoid the annealing step would reduce processing costs; the firing step is a standard process during contact formation in industrial high efficiency Si solar cell production.

The studies in this section aim at investigating whether this significant increase of lifetime can be attributed to an enhanced field-effect ($Q_{ox,eff}$), an enhanced chemical (D_{it}) passivation by the SiO$_x$/AlO$_x$/SiN$_x$ stack or whether other effects need to be considered.

Firstly, the stability of the field-effect passivation regarding $Q_{ox,eff}$ is investigated. In Fig. 5.34(a,c) and (b,d) the initial C-V sweeps and the corresponding $Q_{ox,eff}$ are depicted representing the sample without (just HF) and for the one with prior RCA (RCA+HF) cleaning, respectively. As can be seen from the consecutively measured C-V sweeps, no
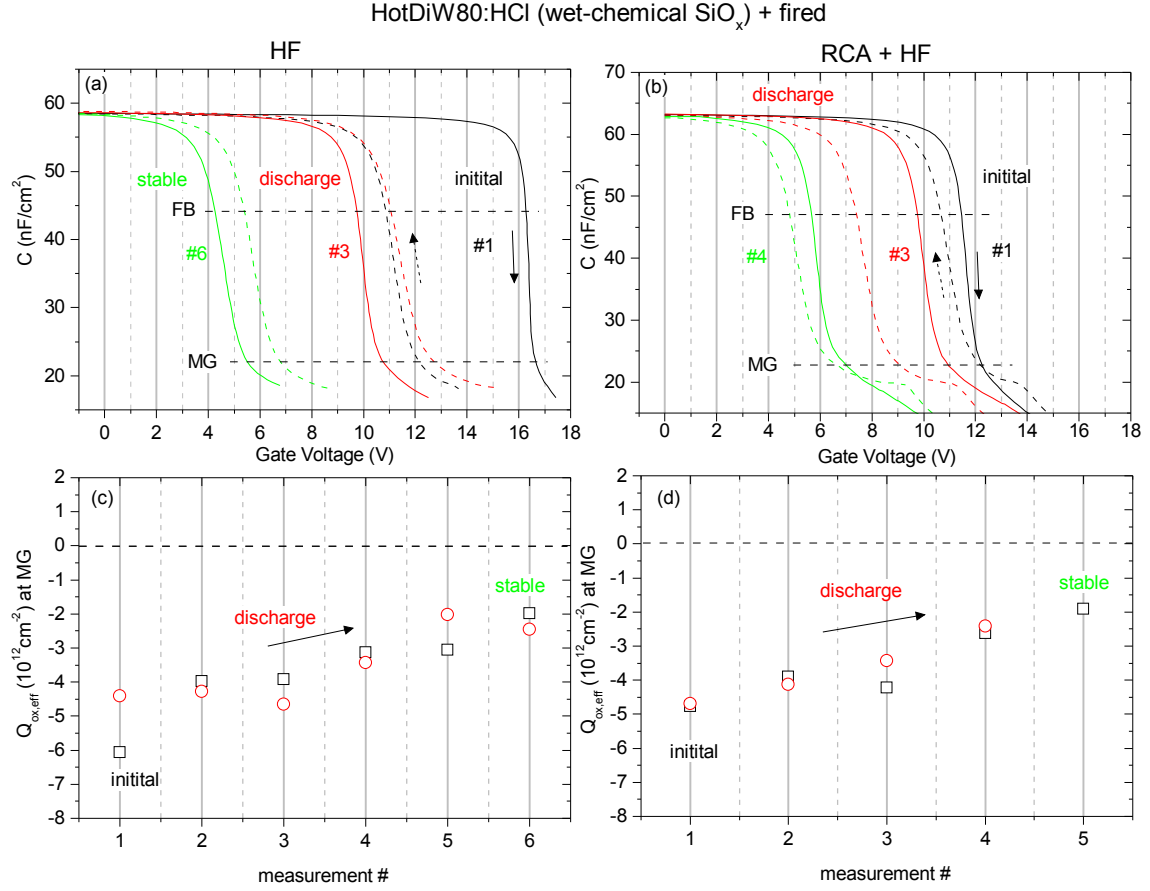
Figure 5.34: Consecutively measured high-frequency (1 MHz) C-V sweeps and the corresponding $Q_{ox,eff}$ at mid gap (MG) of fired $SiO_x/AlO_x/SiN_x$ stacks on HF-treated Si surface without (a,c) and with (b,d) prior RCA cleaning. Arrows indicate the sweep direction (acc-inv or inv-acc). The sweeps reveal no considerable difference regarding the stability of $Q_{ox,eff}$.

qualitative difference in the charging behavior of both samples is observed: both start at similarly high initial negative $Q_{ox,eff}$ which is reduced upon consecutive measurements. Both samples reach a stable state at $Q_{ox,eff} \sim -2 \times 10^{12}\,cm^{-2}$. This discharge can be attributed to electron detrapping, or hole injection from the Si into the $SiO_x/AlO_x/SiN_x$ stack, until only the more stable charged traps remain. In fact, the reproducibility of this discharge with the RCA cleaned sample supports the conclusion that firing leads to a negative charging of traps near the SiO_x/AlO_x interface. Apart from a slight deviation of this initial charge state, there is no considerable effect of the RCA cleaning on the initial value and stability of $Q_{ox,eff}$. Therefore, the higher lifetime measured in Fig. 5.33 does not originate from an enhanced field-effect passivation.

In order to evaluate the chemical passivation properties, C-V curves of both samples were measured in relaxation mode. The results are depicted in Fig. 5.35. In the case of the RCA cleaned sample, the C-V curve revealed highest stability, i.e. shortest relaxations, when a prior V_{stress} = -15 V was applied. This negative V_{stress} caused a further detrapping of
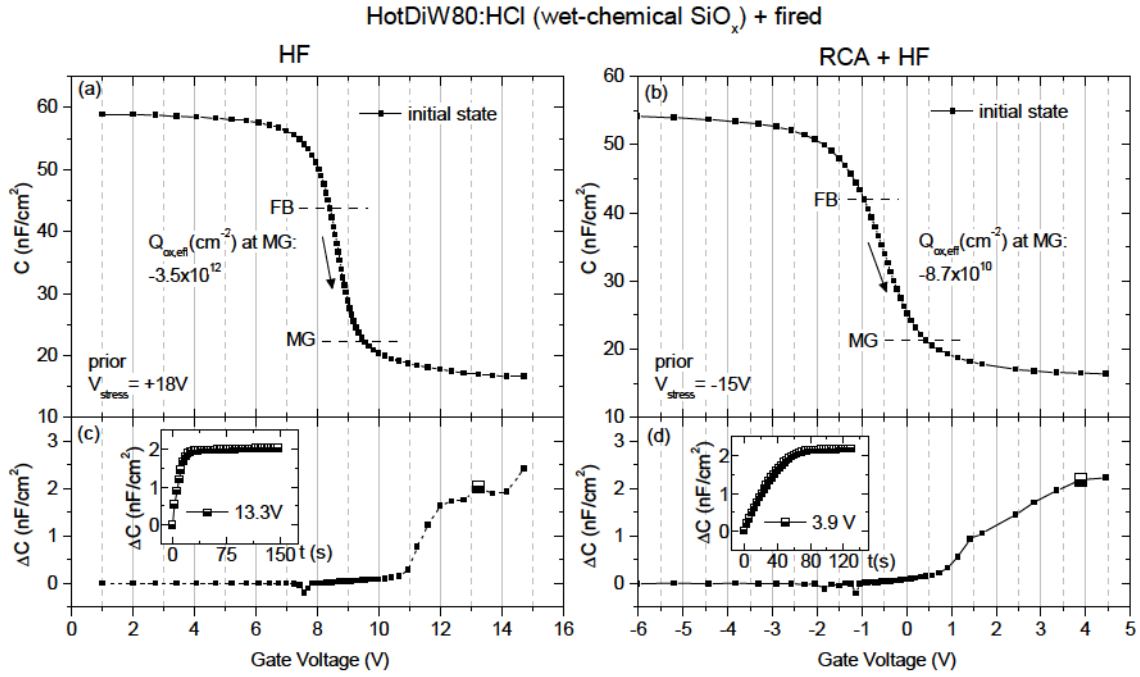
Figure 5.35: High-frequency (1 MHz) C-V measurements in relaxation mode and the corresponding relaxation capacitance ΔC over gate voltage of MIS structures consisting of fired $SiO_x/AlO_x/SiN_x$ stacks on HF-treated Si surface without (a,c) and with (b,d) prior RCA cleaning. C-V curves were measured following a V_{stress} of + 18 V (> 400 s) or - 15 V (400 s) for charge stabilization. Inserts illustrate exemplary ΔC-t traces at the indicated gate voltage.

negative charges leading to a low but stable $Q_{ox,eff} = -8.7 \times 10^{10}\,cm^{-2}$, similar to $Q_{ox,eff}$ of the reference sample after applying the same V_{stress} (see Fig. 5.30(d)). Therefore, this is not considered an effect of the RCA cleaning, but rather of the charge state, which is influenced by V_{stress}.

Despite the different $Q_{ox,eff}$, both samples reveal nearly identical ΔC-V curves:

1. In the accumulation region near FB negative relaxations can be observed indicating that in this state the sample is tending towards lower negative charges. This can be attributed to detrapping of electrons or injection of holes (majority charge carriers) from the Si into traps in the $SiO_x/AlO_x/SiN_x$ stack and, thus, reducing the negative charge density.

2. In the depletion region slightly positive relaxations are observed, hence, in this region the charging tends towards slightly higher negative $Q_{ox,eff}$. This is possibly due to electron trapping in the $SiO_x/AlO_x/SiN_x$ stack.

3. In the inversion region positive relaxations reveal the generation of minority charge carriers. As can be seen in the ΔC-t insets, these relaxations lead to a constant inversion capacitance indicating the formation of a true inversion layer due to a completed generation of minority charge carriers.
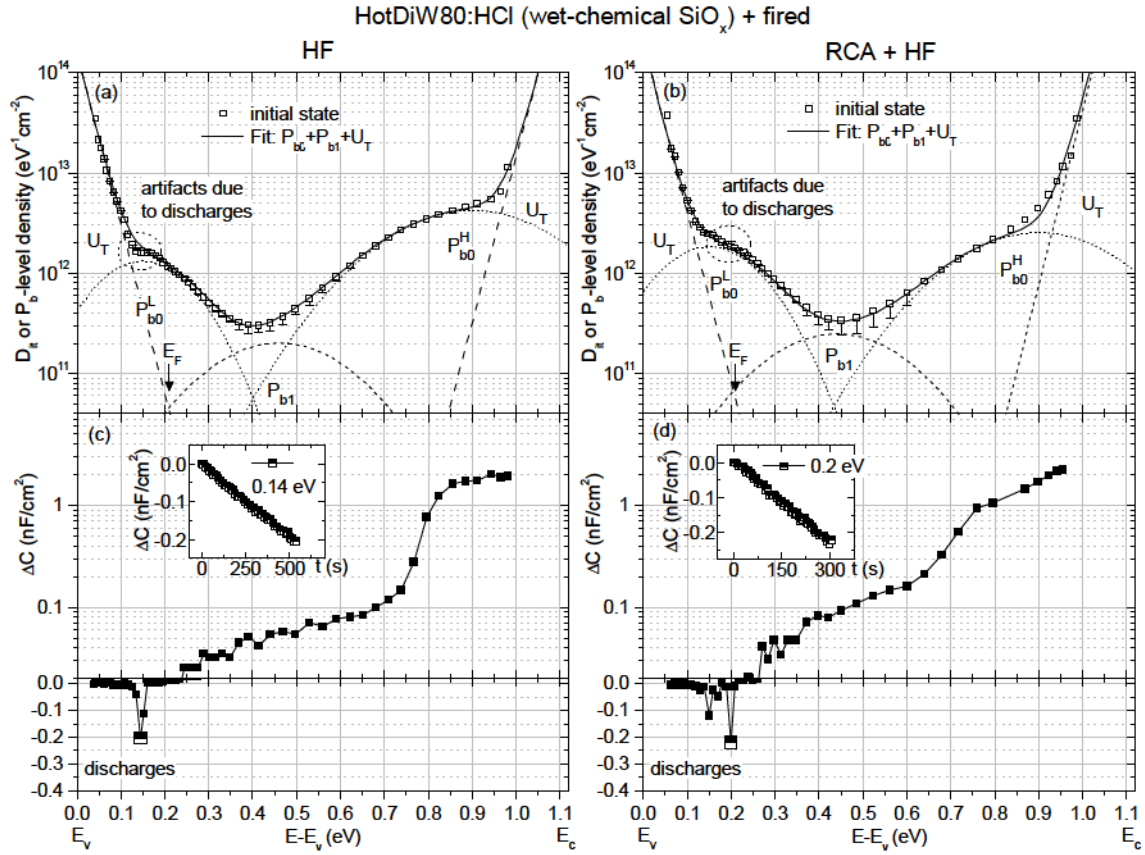
Figure 5.36: Initial defect state density (D_{it}) at the c-Si/SiO_x/AlO_x interface over the c-Si band gap of fired SiO_x/AlO_x/SiN_x stacks on HF-treated Si surface without (a) and with (b) prior RCA cleaning. The corresponding relaxation ΔC-spectra (c,d) are shown. The D_{it}-spectra are fitted by the sum of Gaussian distributions for P_{b0}- and P_{b1}-like defects and exponential functions for strained bond defects U_T.

Taking into consideration the observed relaxations, the C-V curves can be analyzed reliably to determine D_{it}.

The resulting D_{it}-spectra of both samples are depicted in Fig. 5.36. The semi-logarithmic plots of the ΔC-spectra reveals slightly larger positive relaxations between E_F and MG for the RCA cleaned sample. Consequently, the estimated error in the corresponding D_{it}-spectrum is slightly larger. Above MG the rather large positive relaxations are due to the generation of minority charge carriers rather than charging effects in the SiO_x/AlO_x/SiN_x stack. Therefore, they are not considered for error estimation. The relatively large negative relaxations ΔC-t near E_F, depicted in the inserts, lead to slight distortions (artifacts) in the corresponding parts in the D_{it}-spectra of both samples. Regarding the chemical passivation, there seems to be a difference in the D_{it}-spectra. For a better evaluation of the difference, the experimental D_{it}-data was fitted by the sum of three Gaussians representing P_{b0}- and P_{b1}-like defects and exponential functions U_T for the band tails.
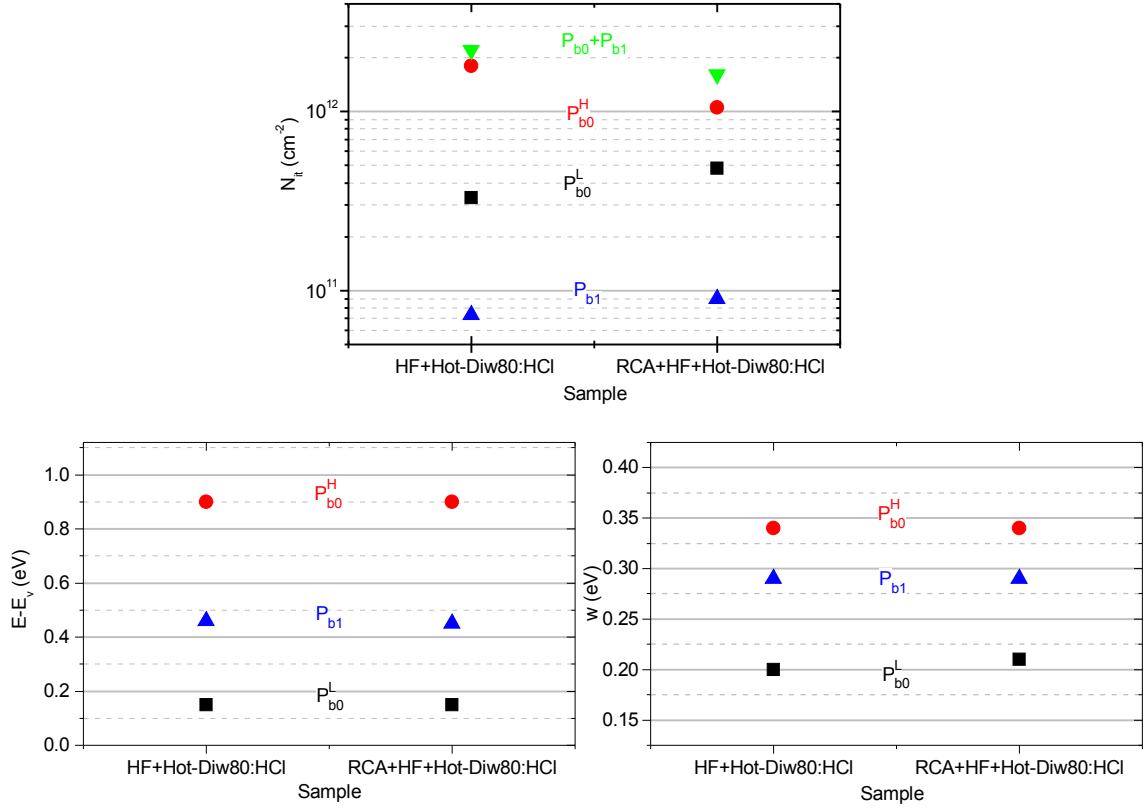
Figure 5.37: Interface defect density (N_{it}, upper graph), energetic position in c-Si band gap (E-E_v, left graph) and width (w, right graph) of Gaussians for P$_{b0}$- and P$_{b1}$-like defects used for fitting of experimental D_{it}-spectra of fired samples in Fig 5.36.

The fitting parameters, i.e. the area (N_{it}), energetic position (E-E_v) and width (w) of the Gaussians, are depicted in Fig. 5.37. For both samples, nearly identical energetic positions (E-E_v) and widths (w) of the Gaussians were obtained allowing a consistent evaluation of the defect density N_{it} given by the area of the corresponding defects types. The RCA cleaning leads to a slight increase of P$_{b1}$-like and P$_{b0}$^{L}-like, however, to a decrease of the P$_{b0}$^{H}-like defects. The latter dominates, leading to an overall reduction of the integrated N_{it}= P$_{b1}$+ P$_{b0}$ from $2.2 \times 10^{12}\,cm^{-2}$ to $1.6 \times 10^{12}\,cm^{-2}$. The asymmetric changes regarding the P$_{b0}$^{L}- and P$_{b0}$^{H}-like Gaussians suggests that other defect types may play a role. These defect types may be related to impurities introduced e.g. through iron (Fe) contamination [Laa13]. Fe impurities introduce additional defect levels predominantly in the upper part of the Si band gap [Sze07]. A removal of such metallic and organic impurities upon RCA cleaning may be related to the observed reduction of P$_{b0}$^{H}-like defects.

Assuming that $S_{eff} \sim N_{it}/Q_{ox}^2$ [Din12b], with $Q_{ox,eff}$ = constant, the reduction of integrated N_{it} by a factor of ~1.4 upon RCA cleaning cannot entirely account for the reduction of S_{eff} (or increase of τ_{eff}) by a factor of ~1.9, as observed in Fig. 5.33. Therefore, in this case it is most likely that τ_{bulk} is affected by the firing. Recent investigations performed by Laades

et al. [Laa13] demonstrated that the firing process lasting only for a few seconds is able to cause Fe surface residuals to migrate into the bulk, thereby causing a degradation of τ_{bulk}. Therefore, it can be concluded that the enhancement of minority charge carrier lifetime upon RCA cleaning combined with HF and wet-chemical oxidation, is attributed to an improvement of the chemical passivation as well as to an enhancement of τ_{bulk} through removal of metallic and organic impurities from the Si surface.

5.9 Summary

The objective of this part of the thesis was to examine the passivation properties of all-PECVD deposited AlO_x-single layers and in particular of AlO_x/SiN_x stacks on p-type c-Si. Both fundamental aspects, field-effect and chemical passivation, have been explored regarding their origin as well as stability. Effective minority charge carrier lifetime (τ_{eff}) measurements via QSSPC and corresponding effective surface recombination velocities S_{eff} were compared with results regarding effective oxide charge density $Q_{ox,eff}$ and interface defect state density D_{it}. The latter was obtained through high frequency (1 MHz) capacitance voltage (C-V) combined with capacitance time (C-t) measurements. The influence of different wet-chemical c-Si surface treatments, such as HF only, HF + wet-chemical oxidation (SiO_x) and RCA + HF + wet-chemical oxidation (SiO_x) on the passivation performance were studied. The samples were investigated in the as deposited state as well as after thermal treatments, such as annealing and firing. An analysis of charging mechanisms was performed including trapping-detrapping phenomena in the $(SiO_x)/AlO_x/SiN_x$-system through voltage stress (V_{stress}) experiments combined with C-V. The $c-Si/(SiO_x)/AlO_x$ interface defect states were spectroscopically analyzed as well as its V_{stress} induced degradation. In this section, the main results achieved in this work are summarized. Table 5.2 gives an overview of the results obtained through QSSPC and C-V.

Annealed AlO_x-single layers on c-Si: Effects of c-Si surface preconditioning

Injection dependent lifetime measurements demonstrated that AlO_x single layers deposited on differently treated c-Si surfaces provide a high quality passivation upon annealing. The highest passivation quality was obtained for the c-Si surface which was RCA-cleaned, HF-treated and wet-chemically oxidized prior to AlO_x deposition and annealing. This treatment resulted in $\tau_{eff} = 1.3\,\text{ms}$ and $S_{eff} = 10.1\,\text{cm/s}$ at an excess charge carrier concentration $\delta n = 10^{15}\,cm^{-3}$. The C-V analysis identified a negative fixed charge density $Q_{ox,eff} = -4.1 \times 10^{12}\,cm^{-2}$ combined with an interface defect state density $D_{it} \sim 2 \times 10^{11}\,eV^{-1}cm^{-2}$ near MG as the origin of the field-effect and the chemical passivation, respectively. Similar values were reported in [Bla13]. The fixed charge density was used as a reference for the analysis of AlO_x/SiN_x stacks regarding $Q_{ox,eff}$.

As deposited AlO_x/SiN_x stacks on c-Si: Effects of annealing and voltage stress

As deposited AlO_x/SiN_x stacks on H-Last c-Si already exhibited a moderate passivation quality in lifetime measurements ($\tau_{eff} = 545\,\mu s$). The C-V investigations demonstrated that this samples exhibited the highest interface defect density ($N_{it} = 5.3 \times 10^{12}\,cm^{-2}$) among all investigated samples. Therefore, the moderate passivation quality is attributed to the measured initial $Q_{ox,eff} = -5.5 \times 10^{12}\,cm^{-2}$, exceeding the reference fixed charge density

c-Si surface	state	τ_{eff} (µs)	S_{eff} (cm/s)	initial $Q_{ox,eff}$ (10^{12} cm^{-2})	stable $Q_{ox,eff}$ (10^{12} cm^{-2})	N_{it} (10^{12} cm^{-2})
HF-Last	as dep.	545	26	-5.5±1.0	-0.7...-1.9	5.3
	anneal.	918	15	-4.5±1.5	-4.5±1.5	2.9
HF+ Hot-Diw80:HCl	as dep.	380	37	+0.6...-2.0	-1.9	0.8
	anneal.	618	23	-3.1...-4.0	-0.6...-4.0	1.8
	fired	545	26	-5.0±1.0	-2.0	2.2
RCA+HF+ Hot-Diw80:HCl	fired	1020	13	-5.0±0.5	-1.9	1.6

Tab. 5.2: Summary of results obtained from QSSPC and C-V measurements of all-PECVD AlO$_x$/SiN$_x$ stacks on p-type c-Si with different surface treatments and states for different thermal treatments. τ_{eff} and S_{eff} were obtained at an excess charge carrier density $\delta n = 10^{15}$ cm^{-3}. The initial $Q_{ox,eff}$ refers to the charge state given by the first measured C-V curve. The stable $Q_{ox,eff}$ refers to the charge state reached after several consecutive C-V measurements with minimal or absent changes in $Q_{ox,eff}$. N_{it} is the defect state density integrated over the entire Si band gap indicating the quality of chemical passivation. For reference, the negative fixed charge densities of annealed AlO$_x$ single layers are $Q_{ox,eff} = -4.6 \times 10^{12}\,cm^{-2}$ for HF-Last and in $Q_{ox,eff} = -4.1 \times 10^{12}\,cm^{-2}$ for (RCA)+HF+Hot-Diw80:HCl treated c-Si surfaces.

($Q_{ox,eff} = -4.6 \times 10^{12}\,cm^{-2}$) of the AlO$_x$-single layer upon annealing. This relatively high $Q_{ox,eff}$ was activated probably by the thermal budget during SiN$_x$ deposition. It was found, however, that this charge state is unstable. It is significantly reduced upon consecutive C-V sweeps at moderate voltages. Therefore, these initial relatively high charge densities most likely originated from negatively charged traps, which were discharged through electron injection into the c-Si upon biasing.

Furthermore, C-V measurements revealed that annealing leads to the formation of stable fixed charges of $Q_{ox,eff} = -4.5 \times 10^{12}\,cm^{-2}$, similar to the reference fixed charge density. It was also found that the interface defect density was significantly reduced down to $N_{it} = 2.9 \times 10^{12}\,cm^{-2}$. In this case, the latter reduction is the main contributor to the enhancement of τ_{eff} ($\tau_{eff} = 918\,µs$) in comparison to the as deposited sample. A fitting procedure of the D_{it}-spectra revealed P$_{b0}$- and P$_{b1}$-like defects, indicating the formation of an ultrathin SiO$_x$ interlayer, which is responsible for the lower N_{it}[Hoe06, Kus03, Din12b].

In addition to the fixed negative charges, charging of traps in the AlO$_x$/SiN$_x$ stack through charge injection from the c-Si by a positive or negative V$_{\text{stress}}$ led to either an enhancement or inversion of negative $Q_{ox,eff}$, respectively. Large V$_{\text{stress}}$ generated additional P$_{b0}$- and P$_{b1}$-like as well as strained bond defects, thus, causing a degradation of the chemical passivation. This V$_{\text{stress}}$ induced degradation of both, $Q_{ox,eff}$ as well as D_{it}, may play an important role for the integration of such AlO$_x$/SiN$_x$ stacks into Si solar cells, where a potential induced degradation (PID) is crucial for their performance.

Annealed AlO$_\text{x}$/SiN$_\text{x}$ stacks on c-Si: Effects of wet-chemical SiO$_\text{x}$ interlayer

The wet-chemical oxidation of the Si surface prior to the AlO$_\text{x}$/SiN$_\text{x}$ stack deposition which was followed by annealing resulted in a considerable decrease of the interface defect ($N_{it} = 1.8 \times 10^{12}\,cm^{-2}$) as compared to the one without wet-chemical SiO$_\text{x}$ interlayer ($N_{it} = 2.9 \times 10^{12}\,cm^{-2}$). However, through this wet-chemical oxidation, instabilities and inhomogeneities of the charge density ($Q_{ox,eff} = -(3.1...4.0 \times 10^{12}\,cm^{-2})$) were introduced as well, which originate most probably from the additional traps/states at or near the wet-chemical SiO$_\text{x}$/AlO$_\text{x}$ interface. Charge trapping at these additional states deteriorated the effect of the fixed negative charges on $Q_{ox,eff}$ (reference: $Q_{ox,eff} = -4.1 \times 10^{12}\,cm^{-2}$) resulting in a deterioration of field-effect passivation quality. This deterioration exceeds the gain in chemical passivation quality through the wet-chemical SiO$_\text{x}$ layer resulting in a lower minority charge carrier lifetime ($\tau_{eff} = 618\,\text{µs}$). The latter is explained by the greater influence of Q_{ox} on the surface recombination velocity than N_{it} at the given charge densities *[Din12b, Hoe08a]*.

As deposited wet-chemical-SiO$_\text{x}$/AlO$_\text{x}$/SiN$_\text{x}$ stacks on c-Si: Effects of firing

In the as deposited state the sample with the wet-chemical SiO$_\text{x}$ interlayer demonstrated the lowest interface defect state density ($N_{it} = 0.8 \times 10^{12}\,cm^{-2}$) of all investigated samples. However, instabilities and inhomogeneities of $Q_{ox,eff}$ were found also for these stacks, ranging from relatively low positive ($Q_{ox,eff} \sim +0.6 \times 10^{12}\,cm^{-2}$) to relatively low negative charge densities ($Q_{ox,eff} \sim -2 \times 10^{12}\,cm^{-2}$) at different location on the sample. Therefore, despite the low N_{it}, this sample demonstrated the lowest effective minority charge carrier lifetime ($\tau_{eff} = 380\,\text{µs}$). However, upon firing, the lifetime considerably increased ($\tau_{eff} = 545\,\text{µs}$). This was attributed to an enhancement of field-effect passivation quality due to a high charge density ($Q_{ox,eff} \sim -5 \times 10^{12}\,cm^{-2}$), despite an increase of the defect state density ($N_{it} = 2.2 \times 10^{12}\,cm^{-2}$). The latter can be attributed to the dissociation of hydrogen upon thermal treatment. It is concluded that firing leads to the activation of negatively charged traps, considerably enhancing $Q_{ox,eff}$ and therefore also the measured lifetime. However, this initially high $Q_{ox,eff}$ is unstable and is reduced down to a similar stable density as of as deposited samples upon moderately applied voltages during C-V sweeps. This is due to electron detrapping and injection from the wet-chemical-SiO$_\text{x}$/AlO$_\text{x}$/SiN$_\text{x}$ stack into the c-Si.

Fired wet-chemical-SiO$_\text{x}$/AlO$_\text{x}$/SiN$_\text{x}$ stacks on c-Si: Effects of prior RCA cleaning

The highest lifetime in the sample series of this work of $\tau_{eff} = 1.20\,\text{ms}$ was obtained upon firing of AlO$_\text{x}$/SiN$_\text{x}$ stacks deposited on RCA-cleaned, HF-treated and wet-chemically oxidized c-Si. C-V investigations revealed that the trapping/detrapping properties regarding

the instability of the initially high $Q_{ox,eff}$ are unaffected by an RCA cleaning. Rather, the enhancement of τ_{eff} is dictated by an improvement of chemical passivation as well as τ_{bulk}. The effect on the chemical passivation was observed as a decrease of the interface defect state density ($N_{it} = 1.6 \times 10^{12}\,cm^{-2}$). The removal of Fe as well as other metallic and organic impurities from the Si surface by the RCA cleaning also prevents their migration into the c-Si bulk and, therefore, a deterioration of τ_{bulk} upon firing *[Laa13]*.

6 Integration of metal nanoparticles into a passivating dielectric

6.1 Introduction

During the past years, extensive studies have been undertaken to investigate the use of metallic nanostructures, which support localized surface plasmons, for achieving enhanced light absorption in Si-based solar cells (see, for example, the review [Atw10] and references therein). Among such metal nanostructures, Au and Ag nanoparticles (NPs) deposited on front or rear sides of Si solar cells are the most interesting materials from both theoretical [Cat08a, Cat08b, Bec11, Sae09, Hae08, Aki09, Cen10] and experimental [Pil07, Bec09, Nak08, Pry10, Sch05, Mat08, Sun08, Fer09, Fer10] points of view. Mainly, this is due to their optical properties related to the confined collective electron oscillations induced by the incident radiation in the NPs; the oscillations are called localized surface plasmon resonance (LSPR). The parameters of the LSPR such as maximum wavelength and extinction coefficient as well as the linewidth are highly dependent on the NP size [Alv97, Hae05], shape [Hae05], dielectric functions of the environment [Nov07], interaction between particles [Su03], and substrate effect [Nog07, Roy89]. In particular, it is generally concluded in most of the existing literature that the deposition of metal nanoparticles on the front surface of silicon solar cells increases the trapping of incident light in Si and, therefore, increases solar cell efficiency. The theoretical calculations suggest that improved light trapping in silicon covered with metal nanoparticles is due to the preferred light scattering by the NPs into a material with a higher dielectric constant, that is, into silicon. This property of metal NPs deposited on the front surface of Si-based solar cells is often termed the "plasmonic effect" of metal NPs resulting in an increase of light absorption in the underlying Si material. However, a careful analysis of publications in the field of plasmonic metal NP applications in solar cells shows that the data and conclusions of practically all studies in this area can hardly be applied to real solar cells which are typically already optimized in terms of light trapping by antireflection coating and/or surface texturing. Indeed, the increase of light trapping in Si absorbers due to metal NP deposition was observed only when compared with solar cells before NP deposition, which had a bare Si surface free of any coatings. Therefore, the questions arise whether metal NP deposition on the front side of Si solar cells can result in more effective light trapping in Si than standard antireflective coatings (ARC), and whether such investigations have

been carried out earlier. In order to better understand the "plasmonic effects" in solar cells, the mechanisms which are responsible for the light trapping increase in the silicon substrate after deposition of noble metal nanoparticles need to be considered. Following the theoretical considerations carried out in the near-field approximation (FDTD method) these mechanisms include [Atw10]: (1) the forward light scattering into the silicon as a material with higher refractive index, (2) light trapping (path length increase due to angular scattering), and (3) the local field enhancement around metal NPs due to excitation of plasmons. The most efficient mechanisms of light absorption enhancement in Si substrates by modification of the cell's front surface with metal NPs are forward scattering and light trapping. As is well known from the literature, small NPs present stronger absorption than scattering efficiencies, and vice versa for large ones. Light trapping is suggested to be especially important in the case of thin film silicon solar cells, although the number of experimental works for such thin film structures is still very limited. Very often the mechanism of forward light scattering is implicitly considered as a real physical mechanism, which is peculiar for metal NPs. It seems, however, that this point of view is a result of some misunderstanding that arises because of the terminological differences between two approaches: (i) the near-field interaction of the electromagnetic field with an individual metal NP and its dielectric environment (usually this is discussed using FDTD numerical modeling – see, for example, Ref. [Bec11] for more details), and (ii) a standard far-field description of the experimentally observed interaction of incident light with a surface: reflectance, transmittance, and absorbance. Such a comparison of the two approaches has been recently carried out in the literature [Por11, Diu11]. It was shown in [Por11] that the repeated sequence of the "forward" light scattering by an individual metal NP to the silicon surface and the light reflection from the back side of the NP creates a constructive interference, which is finally responsible for the enhanced transmission of light through the top layer into silicon. Hence, the metal-NP layer acts as a special antireflective coating (ARC) enhancing the light transmission into silicon; the enhancement is observed relative to bare (uncoated) Si. The interference origin of the action of the metal NP layer deposited on top of a Si substrate is confirmed by modeling in which the NP coating is substituted by a homogeneous film with an effective dielectric constant given by the Maxwell-Garnett formula [Lan84]: the modeling clearly indicates that the first maximum in the film transmission spectrum observed at the long-wavelength side of the plasmonic resonance is the first interference maximum in light transmission through the film. A numerical comparison of relative efficiencies of the three different mechanisms of light trapping enhancement mentioned above was recently carried out in Ref. [Diu11]. It was shown that front-surface plasmonic structures with metal NPs enhance the absorption efficiency of underlying silicon mainly by the effective broad-band scattering into the silicon (interference, or ARC effect), while the contribution of the trapping mechanism (path length enhancement) is relatively small, and the plasmonic local field enhancement contribution is negligible. Therefore, in terms of the far-field approach, the metal NP layer deposited on silicon surfaces of a solar cell is, in fact, a partially absorbing (within the LSPR band)

antireflective coating. Given that the light trapping effect of metal NPs deposited on Si originates from interference is logical that a comparison with Si solar cells covered by a standard ARC as a reference sample should be obligatory for evaluating "plasmonic effects" introduced by metal NPs. Initially, this research study was encouraged by the very limited amount of existing publications, in which the characteristics of metal-NPs covered solar cells are compared with those of identical solar cells with standard ARC. A study of literature showed only one publication in which such a comparison of optical effects [Spi11] and one in which such a comparison of optoelectronic effects was done [ED12]. The present work compares the optical and photovoltaic (photoconductivity) properties of silicon substrates coated by (i) a thin (70-90 nm) layer of TiO_2 doped with in situ grown AuNPs ("plasmonic" TiO_2:AuNP layer), or (ii) a bare TiO_2 layer only (the reference TiO_2 layer). The method of formation of such thin TiO_2:AuNP layers has recently been developed [Ped11] by collaboration partners of HZB from UVEG Valencia in the framework of the project NanoPV (FP7-NMP3-SL-2011-246331). At the present stage this method makes it possible to grow AuNPs with diameters up to 40-50 nm. This relatively small AuNP size, however, is not sufficient to provide preferential scattering of incident light rather than parasitic absorption. Within this approach the light scattering contribution will be higher for diameters larger than 50 nm and dominate above 100 nm in plasmonic layers [Ped13]. Thus, the aims of the following study are: (i) to test the proposed silicon photoconductivity measurement scheme (see chapter 3.2.3) to estimate the contribution of the plasmonic layer to the photoconductivity of the underlying silicon substrate, and (ii) to clarify general (optical and electrical) consequences of metal nanoparticle introduction into a standard ARC layer deposited directly on the Si substrate. Based on the research findings the study will conclude whether certain advantages for future design and implementation of such functional coatings into Si solar cells can be expected.
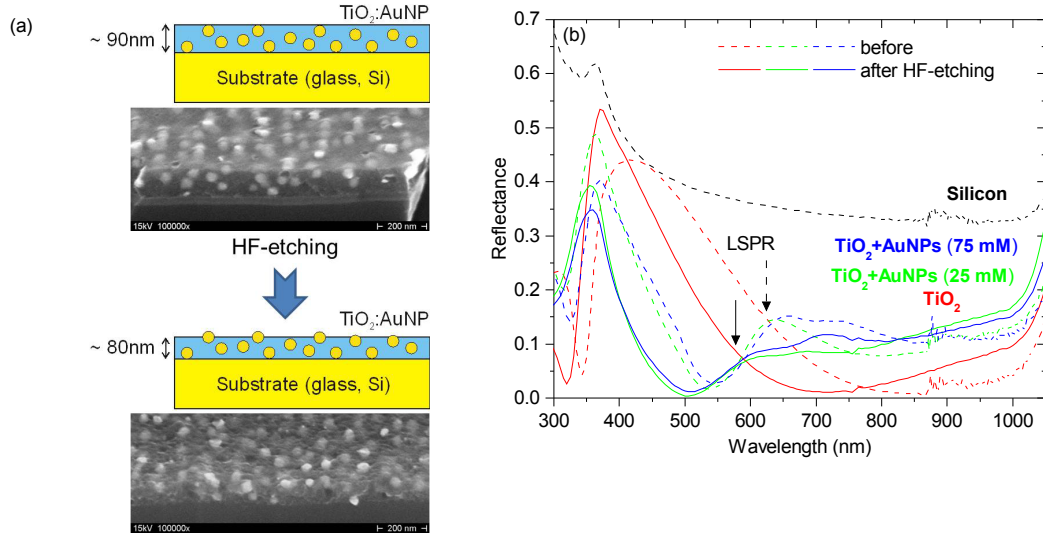
Figure 6.1: (a) Cross-sectional sample structure schemes and SEM images (30° tilted) of TiO$_2$:AuNP (75 mM) on Si before and after HF etching process. After HF-etching an increase of surface roughness is evident. (b) Reflectivity spectra of Si substrates coated by different TiO$_2$-based layers: bare TiO$_2$ (red), TiO$_2$ with AuNPs with 25mM (green) and 75mM (blue) initial Au salt concentrations without (dashed lines) and with (solid lines) additional HF etching. The black dashed line corresponds to the reflection of the bare Si reference substrate. The arrows indicate the spectral positions of the LSPR for each layer determined from the corresponding absorption spectra in Fig. 6.2.

6.2 Optical characterization

As mentioned in the introduction to this chapter, only a comparison with a standard ARC allows one to deduce whether the deposition of a metal-NP based plasmonic layer improves the optical and optoelectronic parameters of a solar cell. The method of plasmonic layer preparation by in situ growth of AuNPs in TiO$_2$ matrix, which has recently been developed by UVEG Valencia [Ped11], is well suited for the purpose of this comparison because the elimination of AuNP precursors from the layer synthesis procedure makes it possible to produce a bare TiO$_2$ layer [Ped11], which represents a standard ARC. Fig. 6.1(a) shows the schemes and SEM images of the TiO$_2$:AuNP (75 mM) layers on Si (or glass) substrate before and after an HF-etch process. It is desirable that embedding AuNPs into the TiO$_2$ layers shall bring about changes in the optical properties that would increase light transmittance through the plasmonic layer to silicon and, therefore, effectively increase light absorption in the silicon substrate. A first evaluation can be obtained through optical measurements of these layers deposited on Si or glass substrates.

Fig. 6.1(b) shows the reflectance spectra of the bare Si substrate (black line), the Si substrate coated by a TiO$_2$ layer (red lines), and coated by TiO$_2$:AuNP films prepared at different initial HAuCl$_4$ concentrations (25 mM: green, 75 mM: blue) that resulted in different AuNP concentrations (filling factors) [Ped11] before (dashed lines) and after the

HF-treatment (solid lines). Before the HF-etching, a TiO_2 layer of 80 nm thickness serves as a standard ARC providing the reflectance minimum at the long wavelength side of Si photosensitivity (around 850 nm in this case). The presence of AuNPs inside the TiO_2 layer leads to a considerable decrease of reflectivity in the $400 - 650$ nm region and some increase in the $650 - 1050$ nm region. The dip of the reflectance with a minimum near 530-550 nm arises due to the interplay between the localized surface plasmon resonance (LSPR) effect and light interference in the TiO_2 thin film [Ped11] and is blue-shifted relative to the LSPR position, which can be directly determined by the absorption measurements (see Fig. 6.2(a)). The reflectance spectra of the identical samples subjected to additional HF treatment are represented by solid lines of the corresponding colors. The distinct noise levels at wavelengths >860 nm originate from different used IR-detectors. The treatment of the plasmonic layer surface by diluted HF solution leads AuNPs close to the outer surface to protrude out of the TiO_2 layer, being only partially immersed in it (Fig. 6.1(a)). This effect was shown to considerably decrease the Si surface reflectivity [Ped11]. Here both, optical and photoconductivity, properties of the HF-treated TiO_2:AuNP/Si system are investigated to clarify whether the treatment can improve optoelectronic properties of solar cells. As one can see in Fig. 6.1(b), HF etching of a bare TiO_2 layer is accompanied by a blue shift of the reflectance curve which is due to the decreased layer thickness. Further blue shift of the reflectivity minimum is observed when the HF treatment is applied to TiO_2 layers containing AuNPs. Again, the reflectance in the red part of the spectrum is higher than in the case of the bare TiO_2 layer. It is worth noting that, contrary to the bare TiO_2 layer, which is transparent in the whole visible spectrum and introduces only light redistribution between reflected and transmitted parts due to the interference effect, AuNP-doped thin layers will always absorb light in the AuNP LSPR band. The absorption may be relatively weak if the NP size is as high as about 100 nm and more. However, in our case the average diameter of AuNPs grown inside TiO_2 layer is rather small (about 50 nm).

In order to investigate the AuNP LSPR band, direct absorption measurements were carried out for TiO_2:AuNP/glass systems to confirm the origin of the dip in the reflectance spectra (Fig. 6.2(a)). All four AuNP-containing layers exhibit an absorption band around 600 nm. The band is clearly due to the LSPR of the AuNPs (see calculations in Ref. [Ped11]). It can be observed that, after etching of the TiO_2:AuNP layer, the absorption decreases by about 20% at the LSPR maximum and the maximum shifts to the short wavelength side. The latter is caused by a decrease of the effective refractive index of the AuNPs' environment because, after TiO_2 matrix etching, a considerable part of AuNPs protrude from the TiO_2 matrix, a high refractive index material, and is surrounded by air, i.e. a low refractive index medium.

The LSPR is characterized not only by light absorption, but also by scattering. The latter can, in principle, contribute to the formation of the dip in the reflectance spectrum around 500-550 nm (Fig. 6.1(b)). Measuring the haze spectra of the plasmonic layers clarified the
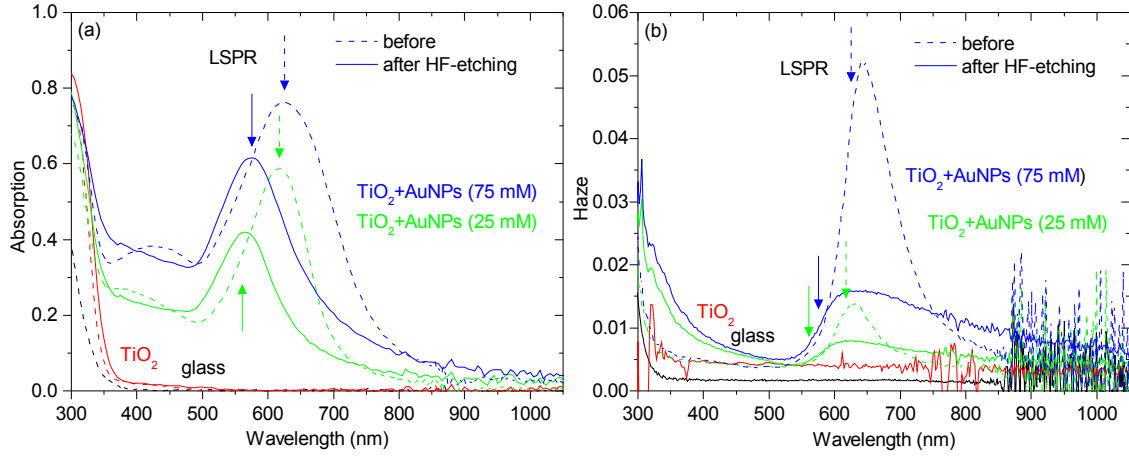
Figure 6.2: Absorption (a) and haze (b) spectra of glass substrates coated with different layers: bare glass (black), glass/bare TiO_2 (red), glass/TiO_2 with AuNPs with 25 mM (green) and 75 mM (blue) initial Au salt concentrations without (dashed lines) and with (solid lines) HF-etching. The arrows indicate the spectral positions of the LSPR for each layer.

role of the LSPR-induced light scattering (Fig. 6.2(b)). The maximum haze value, which is as small as about 5 % (or 0.05) in the LSPR band maximum, was observed for the doped TiO_2 layer with highest AuNP concentration. For all other layers with AuNPs the haze value was even smaller, between 0.5 and 1.5 %. This implies that the haze contribution to the dip in the reflectance spectra in the vicinity of the LSPR band (500-550 nm) is negligible. From these observations it follows that although the deposition of TiO_2:AuNP layer on Si substrate appreciably decreases surface specular reflectance as compared to a bare Si substrate, AuNPs embedding inside the antireflective TiO_2 layer significantly deteriorates antireflective properties of the latter. The deterioration manifests as (1) the reflection increase in the 650-1000 nm region which is, most likely, a result of changes of the interference conditions because of a modification of the layer's effective refractive index, and (2) an appearance of parasitic (plasmonic) light absorption by AuNPs in the 400-600 nm region. The photoconductivity measurements, which are described in the next section, make it possible to determine the external and internal quantum efficiency of photogeneration of charges in the Si substrate as a function of the incident light wavelength.
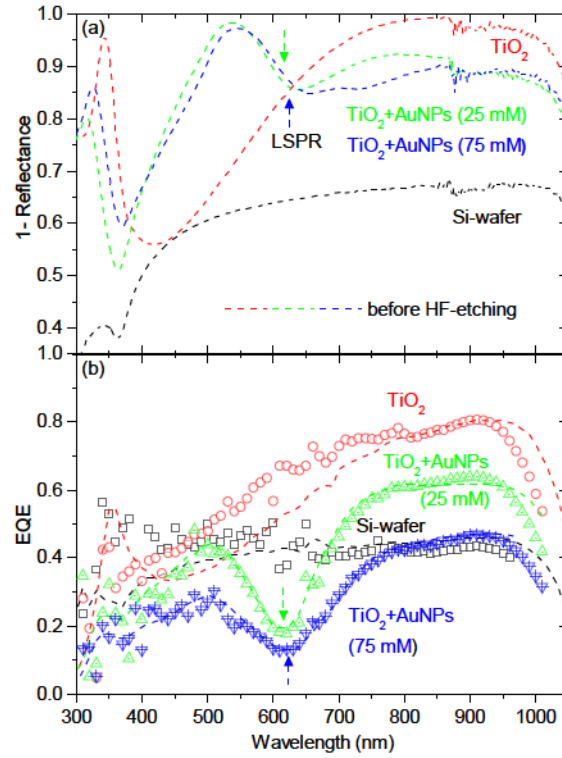
Figure 6.3: 1 - Reflectance (a) and EQE (b) spectra of Si wafers coated with different layers: bare Si (black), Si/bare TiO$_2$ (red), Si/TiO$_2$ with Au NPs with 25 mM (green) and 75 mM (blue) initial Au salt concentrations (open symbols: raw data of first sample set with ohmic contacts but low SNR; dashed lines: data of second sample set with non-ohmic contacts but high SNR, adapted to data of first set). The arrows indicate the spectral positions of the LSPR for each layer.

6.3 Photoconductivity and electrical characterization

To obtain information on the influence of the TiO$_2$:AuNP layer on the efficiency of photogeneration of charge carriers in an underlying Si substrate, spectrally resolved photoconductivity measurements were carried out. Through a comparison of external quantum efficiencies (EQE) (Fig. 6.3(b)) with the optical absorption spectra A(hν) = 1 − R(hν) (Fig. 6.3(a)) it is possible to evaluate, at least qualitatively, whether the effect of the metal NP deposition is determined by the optical properties (interference and absorption) of the TiO$_2$:AuNP/Si system or if there are any additional factors related to (1) the forward light scattering into the silicon or (2) light trapping due to angular scattering. Two sets of Si wafers were used for the preparation of photoconductivity samples. The Si wafers of the first set with a specific resistivity of ~5000 Ωcm produced ohmic contacts. Thus, quantitative comparisons in-between samples of this set were possible. However, the ohmic contacts resulted in a low signal to noise ratio (SNR) in the photocurrent measurements due to still relative high dark currents. Therefore, wafers of higher resistivity (>5000 Ωcm) were chosen for a second set of samples, resulting in dark currents that were two orders

of magnitude lower and a high SNR of the measured photocurrents. However, no ohmic contacts could be formed on these substrates. Thus, the photocurrent values obtained from this second sample set were adapted to the ones of the first set by a correction factor. The resulting EQE for both sets with identically prepared TiO_2:AuNP films (bare Si wafer, Si/bare TiO_2, Si/TiO_2:AuNPs with two different Au salt initial concentrations of 25 mM and 75 mM) are depicted in Fig.6.3(b) (raw data of the first set: open symbols; adapted data of the second set: dashed lines). For comparison with optical properties, the (1-R) spectrum is plotted in Fig. 6.3(a).

The antireflective effect of the bare TiO_2 layer (red symbols/lines) causes a significant increase in photocurrent in the Si wafer over the entire spectrum. As a result of the TiO_2 layer deposition, the shape of the EQE spectrum becomes similar to that of the 1–R spectrum. This similarity confirms the mainly optical (interference) origin of the observed EQE increase. The incorporation of AuNPs into the antireflective TiO_2 matrix leads to a decrease of the EQE values over the main part of the spectrum. The decrease can be separated into two different effects: (a) loss in photocurrent in the Si wafer around the LSPR wavelengths (the LSPR maxima are indicated by arrows), and (b) an overall decrease of photocurrent (especially at the wavelengths higher than 600 nm) with increasing Au NP concentration. The effect (a) is evidently due to the light absorption by the AuNPs themselves. The absorbed photons do not produce electron-hole pairs but, on the contrary, the electromagnetic field of the photons creates currents on the metal NPs surface which finally result in thermal losses. It is worth noting that, in principle, light absorption by AuNPs embedded into TiO_2 matrix can increase the photocurrent in the underlying Si substrate by the mechanism of the electron ejection into the matrix by quantum tunneling. This mechanism was recently observed for AuNP-doped TiO_2 layers for which the photoconductivity markedly increased when AuNPs were photoexcited in the LSPR band [Mub11]. The fact that in our case only a decrease of the photocurrent under excitation in the LSPR band evidences that the above mentioned effect of direct charge injection is negligible. As for effect (b), in case of the TiO_2:AuNP (25 mM) layer, the origin of this is most likely the result of the (1-R) decrease due to the interference effects (the decrease is well visible in Fig. 6.3(a)). However, in case of the TiO_2:AuNP (75 mM) layer the observed overall decrease of EQE values does not correlate with the behavior of the corresponding (1-R) spectrum. This discrepancy will be addressed later in this section.

Since optical measurements demonstrated that etching of the TiO_2 matrix of the TiO_2:AuNP layers results in some decrease and spectral redistribution of the TiO_2:AuNP/Si reflectance (Fig. 6.1 and Ref. [Ped11]), photoconductivity experiments (see Fig. 6.4) to determine how the HF treatment influences the photocurrent in the Si wafer were carried out. The experiments reveal that, firstly, the HF treatment leads to the spectral blue shift of the LSPR bands (indicated by arrows), similarly to what can be observed in the optical absorption spectrum (Fig. 6.2(a)). Secondly, an increase of the photocurrent over the whole spectrum is observed in comparison with the untreated samples. However, this
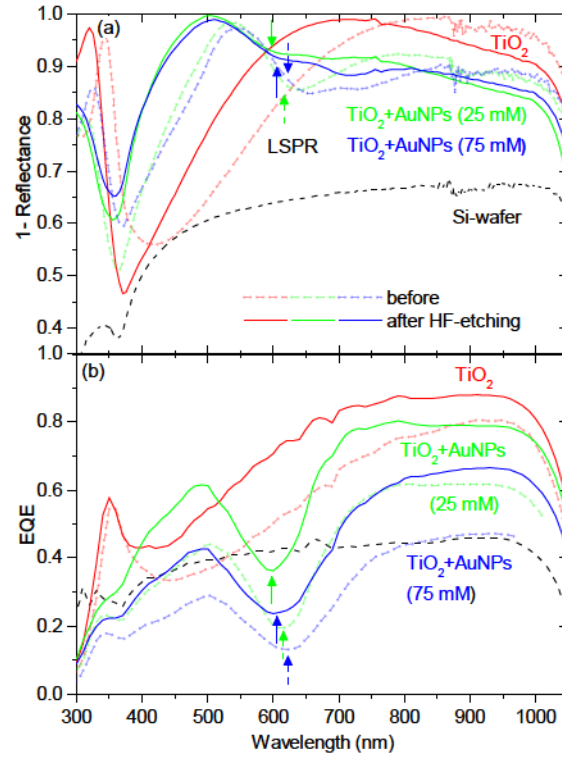
Figure 6.4: 1 - Reflectance (a) and EQE (b) spectra of TiO_2:AuNP layers on Si with different Au concentrations: bare TiO_2 (red), TiO_2 with Au NP with 25 mM (green) and 75 mM (blue) initial Au salt concentrations without (dashed line) and with additional HF etching (solid line). The arrows indicate the spectral positions of the LSPR bands.

relatively large increase does not correlate with the change of optical absorption depicted in Fig. 6.4(a) and, moreover, can be observed not only for AuNPs-containing layers, but also for bare TiO_2 layers. This discrepancy suggests that the HF treatment has an influence both on the optical as well as on the electrical properties of the Si wafer. In accordance with Eq. 3.1 an increase of minority charge carrier lifetime (passivation) can be a reason for higher EQE. Therefore, since the HF-treatment leads to a higher porosity of the TiO_2(:AuNP) layer [Ped13], the HF solution may have reached the Si/TiO_2 interface and improved the passivation. Since the entire sample is immersed into the HF-solution during this treatment, it is also possible that the surface defect density at the wafer backside has been decreased by Hydrogen passivation of Si dangling bonds [Ang98]. Thus, the effective lifetime and hence the measured EQE in the Si wafer becomes higher after such an HF treatment.

Moreover, the internal quantum efficiency (IQE) using Eq. 3.2 was calculated in order to achieve a quantified analysis of the two above mentioned loss mechanisms, (a) parasitic plasmonic absorption by AuNPs at the LSPR range, and (b) quantum efficiency loss over the whole spectrum, in particular when increasing the Au salt concentration from 25 mM to 75 mM. The results of the calculations are displayed in Fig. 6.5. At a wavelength of 950nm,
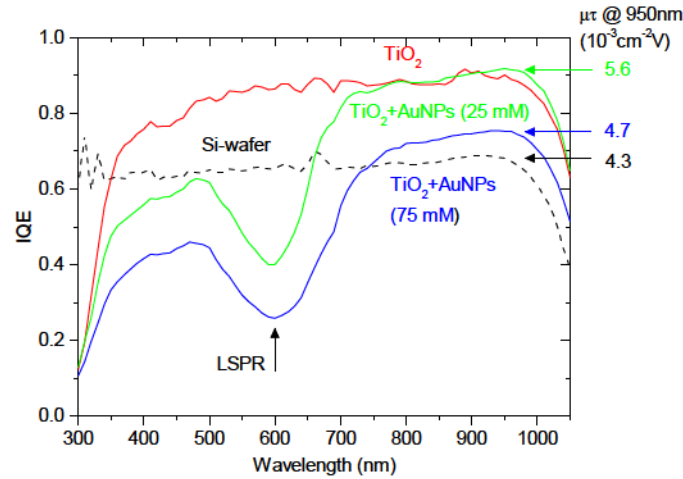
Figure 6.5: IQE spectra of TiO$_2$:AuNP layers on Si with different Au concentrations: bare TiO$_2$ (red), TiO$_2$ with Au NP with 25 mM (green) and 75 mM (blue) initial Au salt concentrations with additional HF etching. The arrows indicate the spectral positions of the LSPR bands maxima. The $\mu\tau$-product is calculated at 950nm.

where the losses based on mechanism (a) are negligible (see Fig. 6.2(a)), the $\mu\tau$-product is calculated (Eq. 3.2). Since the samples originate from the same Si wafer, it can be assumed that their mobilities μ are rather similar, if not identical. Thus, the different $\mu\tau$-product values must arise mainly from different Si surface passivation properties influencing the lifetime τ. On the one hand, all samples coated with a TiO$_2$(:AuNP) layer lead to higher $\mu\tau$-products and therewith appear to result in a better passivation of the Si surface in comparison to the bare Si-wafer. However, increasing the Au salt concentration reduces the $\mu\tau$-product. Direct lifetime measurements by the Quasi Steady State Photoconductance (QSSPC) and µPhotoconductance Decay (µPCD) method revealed lifetimes in the range of a few µs (not shown here), thus below these methods' sensitivity in temporal resolution.

This reduction of the $\mu\tau$-product causing the discrepancy of photoconductivity with optical data, which was mentioned earlier in the analysis of Fig. 6.3, can be explained by a direct influence of AuNPs on the photocurrent (or quantum efficiency). Indeed, the photocurrent depends on the charge carrier lifetime τ, which is determined by the passivation quality of the interface between the Si surface and the TiO$_2$:AuNP-layer. As can be deduced from Eq. 3.1 and 3.2, the measured EQE and IQE have a linear dependance on the lifetime of the photo-generated carriers. Fig. 6.6(a) shows the SEM image (30° tilted) of the Si/TiO$_2$:AuNP (75 mM) interface cross-section. As indicated by the dashed circles some AuNPs are in direct contact with the Si surface. This will result in enhanced charge carrier recombination.

In order to quantify the influence of such AuNPs on the passivation of the Si wafer surface the passivation properties were studied by high frequency (1 MHz) C-V measurements. This method allows the determination of the density of interface defect states (D$_{it}$) in the
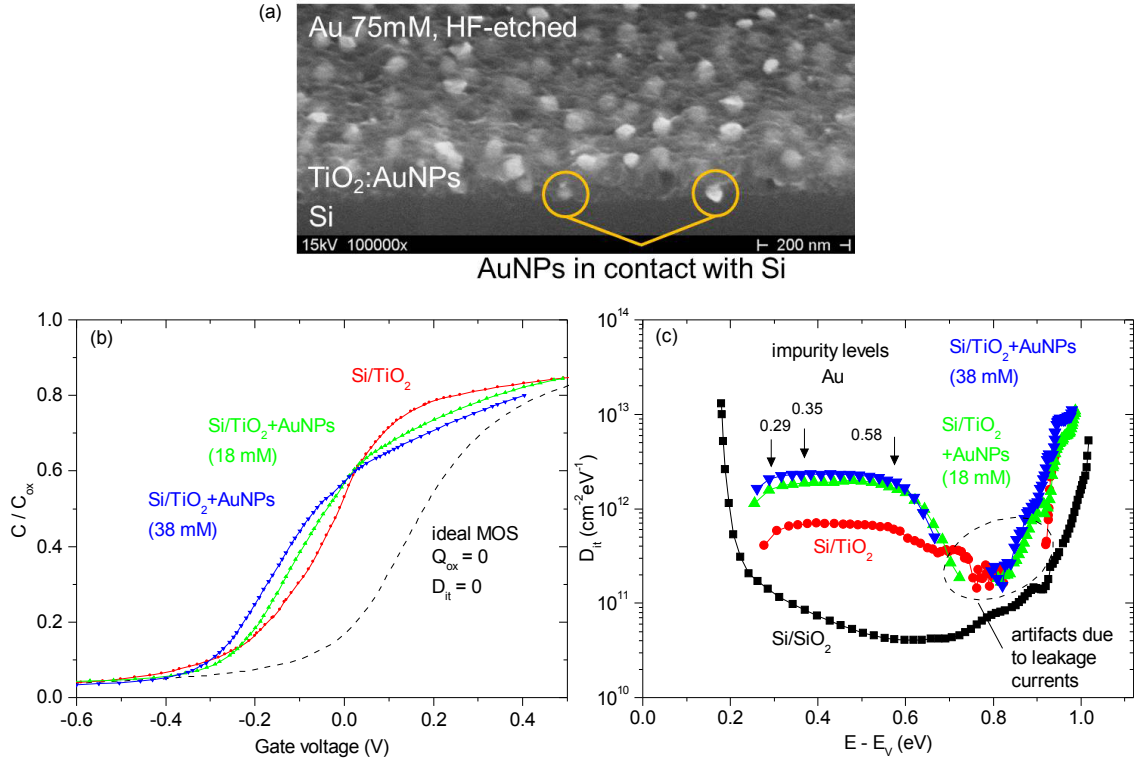
Figure 6.6: (a) SEM image (30° tilted) of TiO$_2$:AuNP (75mM) on Si. AuNPs in contact with Si are marked by dashed circles. (b) Normalized Capacitance-Voltage (CV) curves of n-Si/TiO$_2$:AuNP interfaces with different AuNP concentrations: bare TiO$_2$ (red), 18 mM (green), 38 mM (blue) with the corresponding theoretical CV-curve of an ideal MOS structure (dashed). (c) Corresponding interface state density (D$_{it}$) distribution in the Si band gap obtained from CV vs. energy relative to the valence band edge E$_v$. As a reference curve, D$_{it}$ of a well passivated Si/SiO$_2$ interface (black) is shown.

Si band gap which act as recombination centers for photo-generated charge carriers [Ter62] (see section **??**). Fig. 6.6(b) illustrates the C-V curves for different AuNP concentrations. For this experiment lower Au concentrations (18 mM and 38 mM) were chosen to minimize possible leakage currents through the TiO$_2$:AuNP layer, which could compromise the analysis of the C-V curve. The effect of positive fixed oxide charges Q$_{ox}$ in the TiO$_2$ manifests in the shift of the C-V curve towards negative voltage values. The presence of additional interface defect states by incorporation of AuNPs is clearly visible in the slope of the C-V curve: due to the rechargeable interface defect states, Q$_{it}$, the C-V curve is stretched along the voltage axis. By comparison of the experimental slopes with the theoretical C-V curve of an ideal MOS structure (Q$_{ox}$ = 0, D$_{it}$= 0) the D$_{it}$ within Si band gap was calculated according to Eq. 4.6. In Fig. 6.6(c) the D$_{it}$ values are plotted over the energy relative to the valence band energy E$_v$. The D$_{it}$ values of a Si wafer well passivated by thermal SiO$_2$ are depicted as a reference. They show a typical u-shaped distribution with a low density of dangling bond defects at mid gap and increasing defect density
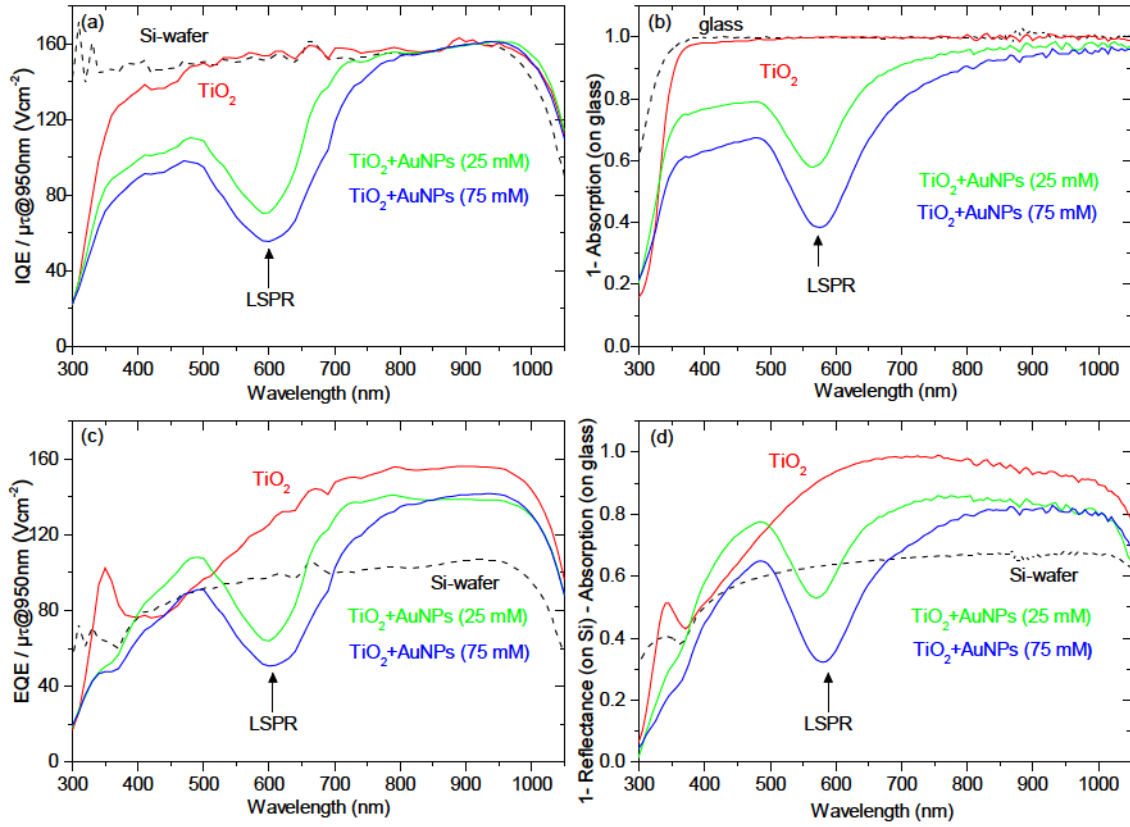
Figure 6.7: Upper panel: Comparison between (a) IQE/$\mu\tau$ spectra of HF-etched TiO$_2$(:AuNP) layers on Si and (b) 1 - Absorption of HF-etched TiO$_2$(:AuNP) layers on glass (i.e. parasitic absorption) with different Au concentrations. Lower panel: Comparison between (c) EQE/$\mu\tau$ spectra of TiO$_2$(:AuNP) layers on Si and (d) 1 - Reflectance (on Si) - Absorption (on glass) .

towards the band edges due to band tail states [Fue96]. The Si/TiO$_2$ interface reveals D$_{it}$ values over one order of magnitude higher around mid gap. Incorporating AuNPs increases D$_{it}$ even further, especially in the energy region where the Au impurity levels in Si are expected [Sze68]. An increase of D$_{it}$ on the Si surface reduces the effective minority charge carrier lifetime in the Si wafer. Therefore, the increased D$_{it}$ values shown in Fig. 6.6(c) are consistent with the decrease of quantum efficiency for higher AuNP concentrations as observed in the $\mu\tau$(@950nm)-product of the photoconductivity measurements (Fig. 6.5).

A possibility to avoid interface recombination losses due to AuNPs in contact with the Si surface is to place a passivating interlayer between the TiO$_2$:AuNP-layer and the Si wafer. This approach was also followed within the framework of this thesis with 30 nm thick thermal SiO$_2$ interlayers. However, the photoconductance results (not shown here) revealed that the chemical deposition method of the TiO$_2$:AuNP-layers lead to a considerable degradation of the initially well passivated Si/SiO$_2$ interface, hence to photocurrents too low for reliable systematic investigations.

Having quantitatively identified the two main loss mechanisms, (a) parasitic plasmonic

absorption by AuNPs at the LSPR range and (b) interface passivation degradation (lower $\mu\tau$-product) due to Au incorporation, the following calculations are conducted for a more consistent comparison of photoconductivity and optical data. To this end, the EQE and IQE data were normalized to their corresponding $\mu\tau$-product (@950nm) (from Fig. 6.5) in order to eliminate the effect of loss mechanism (b). In an ideal case, where no losses due to parasitic optical losses are present (in this case a bare Si wafer), the ratio IQE/$\mu\tau$ should be constant over the entire spectrum for $E > E_g$. Indeed, this is (nearly) the case for the Si-wafer in Fig. 6.7(a). However, with decreasing wavelength IQE/$\mu\tau$(@950nm) shows a slight decrease. This slight decrease can also be observed for the Si coated with bare TiO_2 until losses due to parasitic absorption by the TiO_2-layer dominate at wavelengths < 400 nm. It most probably originates from the depth-dependance of $\mu\tau(d)$ in the Si wafer which has not been considered, yet: light of higher energy (i.e. smaller wavelength) is absorbed closer to the Si surface or TiO_2(:AuNP)/Si interface and therefore closer to the recombination-active interface defects. Therefore, the photogenerated carriers exhibit a smaller lifetime as those generated deeper in the Si bulk through low-energy light absorption. IQE/$\mu\tau$ (Fig. 6.7(a)) is compared with 1 - Absorption of the TiO_2:AuNP layers on glass (Fig. 6.7(b)), which represents mainly the transmitted light through the layer. Comparing Fig. 6.7(a) and (b) now reveals a more consistent correlations between optoelectrical and optical data: absorption by AuNPs leaves a "fingerprint" in the IQE. In addition, the substrate effect is observable as a slight red shift of the LSPR of the layers on the Si substrate in comparison to those on glass [Roy89]. These effects also manifest themselves in the EQE/$\mu\tau$(@950nm) data (Fig. 6.7(c)), as can be observed when compared with 1 - Reflectance (on Si) - Absorption (on glass) (Fig. 6.7(d)). The latter represents the light absorption in the Si-wafer taking into account the parasitic absorption of the TiO_2(:AuNP) layers measured on glass. Regarding all mentioned loss mechanisms, these estimations present a consistent correlation between optical and photoconductance data. Consequently, in future experiments, optical measurements may permit a reliable estimation whether a gain in (external and internal) quantum efficiency can be obtained through photoconductivity measurements.
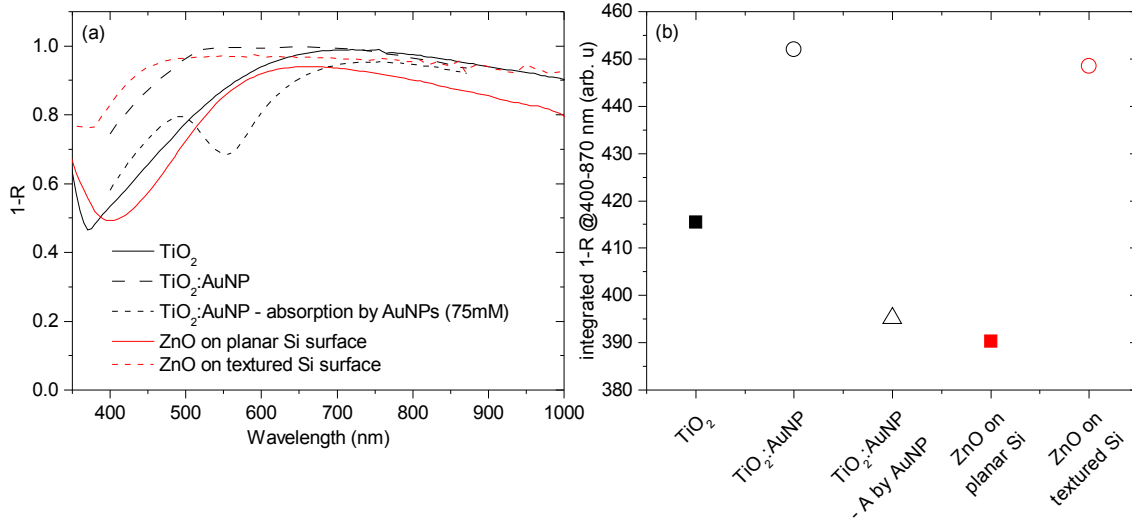
Figure 6.8: (a) Comparison of 1-R between optimized HF-etched TiO$_2$(:AuNP) layers on Si and standard ZnO ARC on planar and textured Si. Parasitic absorption by AuNPs in TiO$_2$:AuNP layer is taken into consideration (short dashed black line) (b) 1-R integrated in the spectral range from 400-870 nm of samples in (a). Optical data of TiO$_2$:AuNP taken from Ref. [Ped13].

6.4 Supplementary experiments

UVEG Valencia conducted an optimization of the HF-treatment procedure by variation of the immersion time of the TiO$_2$:AuNP (75 mM) layers in the HF solution (see Ref. [Ped13]) This optimization leads to further improvement of the anti-reflective effect through a reduction of the parasitic LSPR-absorption by the AuNPs. The TiO$_2$:AuNP layer's optimized anti-reflective effect, taking into account the corresponding parasitic absorption, is depicted in Fig. 6.8(a) (black dashed line) and compared with bare TiO$_2$ as well as HZB-standard ZnO on planar and textured Si. Indeed, when compared to the optical properties before optimization (Fig. 6.7(d)) a considerable reduction of losses due to parasitic plasmonic absorption was achieved. However, as depicted in Fig. 6.8(b), the TiO$_2$ ARC with incorporated AuNPs still exhibits a lower integrated 1 - R than the reference TiO$_2$ without AuNPs. Hence, based on the identified effects and losses presented in the previous section (Fig. 6.7) no gain in EQE through photoconductivity is to be expected even after optimization of the HF treatment. A slight improvement compared to ZnO on a planar surface is observed, but this is due to the favorable optical properties of the TiO$_2$ and not due to the incorporation of the AuNPs. It should be noted, that in comparison to ZnO on textured Si, a higher overall absorption (1-R) by the entire TiO$_2$:AuNP/Si structure can be achieved. In theory, an improved Si absorption could be obtained if parasitic plasmonic absorption could either be completely avoided or if highly effective electron injection from plasmons in the AuNPs into the TiO$_2$-matrix [Mub11] and into the Si by quantum tunneling could be realized. However, experimentally such a realization is highly unlikely due to the loss mechanisms identified in this work, as these by far exceed

any theoretical gain.

6.5 Summary

TiO$_2$:AuNPs/Si plasmonic structures have been thoroughly investigated by means of optical reflection, absorption and haze as well as by photoconductivity (EQE & IQE) measurements to evaluate the use of TiO$_2$:AuNPs plasmonic films in solar cells for light trapping enhancement. After comparing the two systems' (Si substrates coated by TiO$_2$:AuNP or bare TiO$_2$ layers) optical and photoconductivity properties, it can be concluded that the metal NPs-containing layers act as light-absorbing (within the LSPR band) antireflective coatings. The contribution of light scattering is negligible due to the small size of the metal NPs. Furthermore, the randomly dispersed metal NPs inside the TiO$_2$-layer that are in contact with the Si surface generate additional recombination active defect states in the Si band gap which lead to a degradation of passivation and hence photoconductivity. An increase of defect states at the Si/TiO$_2$(:AuNP) interface due to AuNP incorporation was confirmed by HF-CV measurements.

Integration of metal nanoparticles into a passivating dielectric

7 Summary and outlook

In this work different oxidic material systems were subject to investigations of their passivating and optical properties. Advanced measurement methods were developed and refined to enhance the reliability of the results obtained from the analysis of the materials.

Development of experimental methods

The first method was the development of the high frequency capacitance voltage (C-V) method for MIS structures. Here, a c-Si/SiO$_2$ structure with different thermal SiO$_2$ thicknesses (100 nm, 49 nm and 12 nm) was utilized as a reference MIS system. Through systematic investigations of the effects of leakage current as well as of slow charge trapping phenomena, an modification of the analysis procedure was developed. This enabled the reliable determination of the interface defect density over the entire c-Si band gap and the insulator charge density. Thus, a reliable evaluation of the chemical and field-effect passivation became possible. The results obtained from C-V investigations correlated with lifetime measurements. In addition, through prior voltage stress (V$_{stress}$) biasing followed by C-V measurements, trapping and detrapping mechanisms were investigated in AlO$_x$/SiN$_x$ stacks. Through the latter, parameters for the stabilization of charges were found. This set the basis for the reliable evaluation of the field-effect and chemical passivation properties of AlO$_x$-single layers, AlO$_x$/SiN$_x$ stacks and TiO$_2$:AuNP layers on c-Si.

The C-V method developed in this work proved to be a suitable tool in particular for the investigation of the c-Si/dielectric interface defect state density over the entire Si band gap. Insulating MIS-structures are best suited for a reliable investigation. Even though the AlO$_x$ demonstrated rather high leakage currents as a single layer, by capping it with insulating SiN$_x$ a MIS-system was formed exhibiting negligible leakage currents. A prior V$_{stress}$ could bring initially unstable charge in the AlO$_x$/SiN$_x$ stack into a stable state, enabling a determination of D_{it} over the entire c-Si band gap. This finding opens the way to the application of the C-V method on a wider range of materials which normally exhibit leakage currents. Of particular interest would be the investigation of the a-Si:H/c-Si heterojunction interface. By capping the a-Si:H with SiN$_x$ a MIS-structure could be formed and possibly enable the determination of D_{it}. Other interesting material systems and interfaces for C-V investigation are c-Si/AlN, a material system for which applications in photovoltaics have emerged recently [Kru13], as well as poly-Si/SiO$_x$. The latter plays an important role in the passivation of thin-film poly-Si solar cells [Sch13].

The second measurement method was the proposed silicon photoconductivity measurement scheme. It proved to be very well suited to investigate the contribution of a plasmonic TiO$_2$:AuNP-layer to the photoconductivity of the underlying silicon substrate. This method is based on a relatively simple contact scheme and is compatible with materials on Si that require process temperatures >200 °C. Therefore, it enables the evaluation or serves for preliminary assessments of new materials on Si that are not yet compatible with e.g. the processes of the more complex and optimized a-Si:H/c-Si or a-Si:H/poly-Si solar cell structures. On the one hand, the measured EQE allows the identification of optical gains and losses that correlate with optical data. On the other hand, the analysis of the IQE reveals electrical gains or losses due to effects of the layer on the Si surface passivation. These effects are in agreement with results obtained from C-V measurements.

Electronic interface properties of c-Si/AlO$_x$ and c-Si/AlO$_x$/SiN$_x$ systems

In the main part of this work, the passivation properties of AlO$_x$-single layers and AlO$_x$/SiN$_x$ stacks on p-type c-Si were studied. The effects of different wet-chemical treatments of the c-Si surface as well as of thermal treatments (annealing and firing) were subject of these investigations. The wet-chemical c-Si surface treatments consisted of different combinations of RCA-cleaning, HF-etching and wet-chemical oxidation. Regarding the origin of the negative charge, these studies in this work demonstrate that the annealing process leads to the activation of negative fixed charges. The resulting fixed charge densities of $Q_{ox,eff} = -4.6 \times 10^{12} \, cm^{-2}$ agree with values reported for ALD- and PECVD-deposited AlO$_x$ in the range of $Q_f = -(2 - 13) \times 10^{12} \, cm^{-2}$ after annealing at moderate temperatures [Hoe08b, Din11a, Miy10, Din12b]. It was found that the implementation of a wet-chemical SiO$_x$ interlayer as well as the thermal treatments results in a tradeoff between chemical and field-effect passivation. In general, the wet-chemically oxidized interfaces exhibited a considerably reduced interface defect state density (D_{it}) when compared with the reference samples without wet-chemical SiO$_x$ interlayer, in particular in the as deposited state. After thermal treatments, D_{it} increased; however, it remained below the values of the reference sample. Through wet-chemical oxidation, additional traps were introduced as well, which are most likely located in the vicinity of the SiO$_x$/AlO$_x$ interface. These additional traps cause inhomogeneities and instabilities of the negative charge, particularly in the as deposited and fired wet-chemical-SiO$_x$/AlO$_x$/SiN$_x$ stacks. Nevertheless, the fired stacks demonstrated the highest minority charge carrier lifetime (> 1 ms) among the investigated samples in this work. C-V measurements demonstrated that this is in part due to the reduced D_{it}, but is mainly attributed to a relatively high, initial charge density of $Q_{ox,eff} \sim -6 \times 10^{12} \, cm^{-2}$. This initial charge density is higher than the fixed charge density of the annealed samples. An enhancement of lifetime upon firing has been reported for CVD-AlO$_x$-single layers and was attributed to fixed negative charges [Bla13].

The C-V studies in this thesis demonstrated that in contrast to the annealed samples, the initially high negative charge density of the fired sample was not stable. Upon moderate

biasing the charge was considerably reduced down to a stable $Q_{ox,eff} \sim -1 \times 10^{12}\,cm^{-2}$. This reduction is caused by electron detrapping in the AlO_x/SiN_x stack and emission into the c-Si. It is concluded that, while annealing generates fixed negative charges, the firing process leads to negative charging of traps, which contribute to the field-effect passivation. For solar cell application, a stable field-effect passivation performance is essential. Therefore, though initially displaying a high passivation quality, the fired wet-chemical-$SiO_x/AlO_x/SiN_x$ stacks would be unsuitable for implementation in high-efficiency c-Si solar cells: One can expect that upon illumination or through a potential build-up the initially negatively charged traps contributing to the field-effect passivation may discharge through detrapping into the c-Si and lead to a degradation of passivation. Thus, the generation of stable fixed negative charges makes the annealing process indispensable. It is concluded that in addition to the fixed negative charges, trapping of negative charges near the interface is a crucial mechanism contributing to the field-effect passivation. As demonstrated in several works [Laa12], a subsequent firing process of the annealed wet-chem.-$SiO_x/AlO_x/SiN_x$ stack does not deteriorate the passivation quality, making it suitable for solar cell processing. Other works come to a similar conclusion [Din09, Din12b]. However, the AlO_x/SiN_x stack investigated there did not include a wet-chemical SiO_x interlayer. The initial high negative charge can be reversibly reduced and inverted by a negative constant voltage stress (V_{stress}). This is caused by electron detrapping and positive charging of traps in the AlO_x/SiN_x stacks through charge injection from the c-Si.

It was found that a V_{stress} not only allows to control the charge state of the passivation stacks, but also can lead to a voltage stress induced degradation of the chemical passivation. Additional intrinsic Si dangling and strained bond defects can be generated at the c-Si/SiO_x interface. Similar observations have recently been reported for AlO_x-single layers [Gon13b, Gon13a, Raf13]. These results are of interest not only for understanding the charge trapping mechanisms and interface properties of c-Si/SiO_x/AlO_x but also in regard to the implementation of such PECVD-AlO_x/SiN_x passivation stacks in c-Si solar cells, as voltage stress induced degradation of passivation will influence the performance of the solar cell. Both V_{stress} induced effects are possibly linked to so called potential induced degradation (PID) effects, which have a detrimental influence on photovoltaic module performance.

Further optimization processes should focus on minimizing the instabilities and inhomogeneities of the charge density while maintaining the good chemical passivation at the c-Si/SiO_x interface. To benefit from the enhanced chemical passivation obtained by the wet-chemical SiO_x interlayer,it is crucial to reduce the trap density at the (wet-chemical) SiO_x/AlO_x interface responsible for charge instabilities. This may be achieved e.g. by further optimization of the wet-chemical oxidization process and/or of the thermal treatments.

Optical properties and electronic interface properties of the TiO$_2$:AuNPs/Si system

TiO$_2$:AuNPs/Si plasmonic structures have been thoroughly investigated by means of optical reflection, absorption and haze as well as by photoconductivity (EQE & IQE) measurements to evaluate the use of TiO$_2$:AuNPs plasmonic films in solar cells for light trapping enhancement. After comparing the two systems' (Si substrates coated by TiO$_2$:AuNP or bare TiO$_2$ layers) optical and photoconductivity properties, it can be concluded that the metal NPs-containing layers act as light-absorbing - within the localized surface plasmon resonance (LSPR) band - antireflective coatings. The contribution of light scattering is negligible due to the small size of the metal NPs. Furthermore, those of the randomly dispersed metal NPs inside the TiO$_2$-layer that are in contact with the Si surface generate additional recombination active defect states in the Si band gap which lead to a degradation of passivation and hence photoconductivity. An increase of defect states at the Si/TiO$_2$(:AuNP) interface due to AuNP incorporation was confirmed by HF-CV measurements. The use of bigger (> 100 nm) AuNPs could decrease the absorption losses, but this will hardly result in an antireflection efficiency (increase of light absorbance in the underlying Si) of the hybrid TiO$_2$:AuNPs film, exceeding that of the metal-free TiO$_2$ ARC. Indeed, a recent attempt to improve the antireflection efficiency of an optimized Si$_3$N$_4$ film by lithographic deposition of 150 nm Ag nanoparticles resulted in minor optical improvements only [Spi11]. Finally, it can be concluded that the integration of our AuNPs containing hybrid films at the rear side (rather than at the front side) of Si solar cells would definitely circumvent the parasitic absorption in the 500 - 800 nm LSPR range and might thus be preferable for practical applications. Similar conclusions have been made recently in the literature on the basis of experiments with metal NPs deposited on Si [ED12, Tan12]. To prevent additional recombination losses of photogenerated charge carriers due to metal NPs in contact with the silicon substrate, a passivating interlayer should be integrated into the rear side of the solar cell. Based on the results obtained in this work, it was concluded in the framework of the project nanoPV to shift the focus of the work onto bigger (> 100 nm) AgNPs newly developed by UVEG Valencia for implementation into the rear side of thin-film Si solar cells from HZB.

Further investigations of trapping and interface defect properties

Regarding the application of AlO$_x$/SiN$_x$ passivation stacks in photovoltaics, the goal is to reduce charge instabilities in order to achieve stable, large negative charge densities for more efficient field-effect passivation. Therefore, a deeper understanding of the trapping/detrapping kinetics observed in the studies of this thesis as well as the effect of the thermal treatments is necessary.

The high-frequency (1 MHz) C-V method in conjunction with C-t transient measurements developed in the framework of this thesis enabled, amongst others, the identification of

traps in the AlO_x/SiN_x stacks as well as the study of their influence on the passivation properties. However, the C-V method can in principle give more information on the fundamental properties of such traps. Such a C-V method that gives a deeper insight in the trapping phenomena is the measurement of constant capacitance voltage transients (CCVTs) in MOS structures under low electric fields [Sal13]. The CCVT method is based on tracking the evolution of the required gate voltage to keep the capacitance constant, e.g. at mid gap. It provides information about the trapping/detrapping kinetics under low electric fields. In contrast to the V_{stress} experiments, where large electric fields are applied, this technique allows the sensing of deep traps without risking the generation of new traps inside the dielectric. In a recent study of thin ALD Al_2O_3 layers with this method and supported by physical modeling, Salomone *et al.* [Sal13] found two different types of traps. One is responsible for the instabilities observed in C-V measurements, the other has characteristic trapping times three orders of magnitude longer. The energy levels of the studied traps were determined at 2.2 and 2.6 eV below the Al_2O_3 conduction band. Such CCVT investigations of the all-PECVD AlO_x/SiN_x stacks would be of fundamental interest.

To learn more about the chemical passivation properties of the AlO_x/SiN_x passivation stacks, a more fundamental study of the interface defect states is necessary. Of particular interest are those interface defects which were generated due to a large applied bias. The C-V method in this thesis enabled a reliable spectroscopic evaluation of the defects states over the entire Si band gap, a feature rarely found in the literature, in particular for the c-Si/(SiO$_x$)/AlO$_x$ interface. This allowed to fit the D_{it}- as well as ΔD_{it}-spectra with Gaussian distributions for P_{b0}- and P_{b1}-like defects, based on the current defect model of the c-Si(100)/SiO$_2$ interface. A verification of the nature of these defects states, in particular of the generated ones, could be performed via electron paramagnetic resonance (EPR) [Can02, Ste02a, Ste02b, Len05] or electrically detected magnetic resonance (EDMR) [Boe03, Len05] measurements. Previous studies already confirmed the c-Si/AlO$_x$ interface to be c-Si/SiO$_x$-like [Din12b]. However, so far, no EPR or EDMR studies have been performed so far on V_{stress} generated defects at the c-Si/(SiO$_x$)/AlO$_x$ interface. Therefore, an investigation of these generated defects in conjunction with V_{stress}-based C-V experiments could give an answer to the question whether they are indeed P_{b0}- and P_{b1}-like defects or possibly of a different nature.

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A Publications

Publications in the framework of this thesis

- <u>J. A. Töfflinger</u>, A. Laades, L. Korte, C. Leendertz, L. M. Montañez, U. Stürzebecher, H.-P. Sperlich, B. Rech. *PECVD-AlO$_x$/SiN$_x$ passivation stacks on wet-chemically oxidized silicon: Constant voltage stress investigations of charge dynamics and interface defect states.* Solar Energy Materials & Solar Cells, (2014), in press, DOI: 10.1016/j.solmat.2014.09.024.

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- <u>J. A. Töfflinger</u>, E. Pedrueza, V. Chirvony, C. Leendertz, R. García-Calzada, R. Abargues, O. Gref, M. Roczen, L. Korte, J. P. Martínez-Pastor, B. Rech. *Photoconductivity and optical properties of silicon coated by thin TiO$_2$ film in situ doped by Au nanoparticles.* Physica Status Solidi A 210 (2013), p. 687-694.

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Other publications involving the author

- C. Leendertz, V. S. Chirvony, R. García-Calzada, L. Görög, <u>J. A. Töfflinger</u>, L. Korte, S. Agouram, J. P. Martínez-Pastor, N. Petermann, H. Wiggers and A. G. Ulyashin. *Towards solar cell emitters based on colloidal Si nanocrystals.* Physica Status Solidi A, (2014), in press, DOI: 10.1002/pssa.201431264.

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properties of Si/SiO₂ nanostructures grown by decomposition of substoichiometric SiOₓNᵧ layers for photovoltaic applications. Physica Status Solidi / A 210 (2013), p. 676-691

- M. Roczen, M. Schade, E. Malguth, G: Callsen, T. Barthel, O. Gref, <u>J. A. Töfflinger</u>, A. Schöpke, M. Schmidt, H. S. Leipner, F. Ruske, M. R. Phillips, A. Hoffmann, L. Korte, B. Rech. *Structural investigations of silicon nanostructures grown by self-organized island formation for photovoltaic applications.* Appl. Phys. A, 108 (2012), p. 719-726.

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- <u>J. A. Töfflinger</u>, A. Laades, C. Leendertz, L. M. Montañez, L. Korte, U. Stürzebecher, H.-P. Sperlich, B. Rech. *PECVD-AlOₓ/SiNₓ passivation stacks on silicon: Constant voltage stress investigations of charge dynamics and interface defect states.* E-MRS Spring Meeting, 2014 in Lille, France, talk.

- <u>J. A. Töfflinger</u>, A. Laades, C. Leendertz, L. M. Montañez, L. Korte, U. Stürzebecher, H.-P. Sperlich, B. Rech. *PECVD-AlOₓ/SiNₓ passivation stacks on silicon: Effective charge dynamics and interface defect state spectroscopy.* SiliconPV 2014 in 's-Hertogenbosch, Netherlands, talk.

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- <u>J. A. Töfflinger</u>, M. Roczen, M. Schade, O. Gref, A. Schöpke, E. Malguth, L. Korte, H. Leipner and B. Rech. *Si/SiO₂ nanostructures grown by dewetting of ultrathin amorphous Si-layers for photovoltaic applications.* DPG Frühjahrstagung 2012 in Berlin, talk.

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