

CIGSE SUPERSTRATE SOLAR CELLS: GROWTH AND CHARACTERIZATION OF CIGSE THIN FILMS ON TRANSPARENT CONDUCTIVE OXIDES

vorgelegt von
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zur Erlangung des akademischen Grades

Doktor der Naturwissenschaften
-Dr.-rer.-nat-

genehmigte Dissertation

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Tag der wissenschaftlichen Aussprache 13. Oktober 2015

Berlin 2016

Abstract

The prospects and the limitations of Cu(In,Ga)Se₂ (CIGSe) solar cells in superstrate configuration were studied in this work. The, compared to the standard substrate configuration, inverted device structure, sets new requirements for the materials used in the device. CdS cannot be used as the buffer layer between the CIGSe absorber and the ZnO window layer due to its low thermal stability. The direct deposition of CIGSe onto ZnO is known to induce the formation of a GaO_x layer at the CIGSe/ZnO interface, but its influence on the device was yet unclear. The correlation between the interface and device properties of CIGSe/ZnO devices is the core part of this work.

Interface analysis show that the GaO_x layer exhibits large impurities of Cu, which are known to induce acceptor states in oxides. Also In was found as an impurity and is shown to reduce the interface band gap, increasing the interface recombination. The amount of Cu and In within the GaO_x layer depend critically on the CIGSe deposition process and best efficiencies were achieved for a process type leading to the lowest Cu and In concentrations. A device model, based on numerical methods, was set up and can explain several aspects of the superstrate device's behaviour. The performance limiting effect was found to be indeed deep acceptor states within the GaO_x and not a conduction band spike as was speculated earlier. Analysis of the amorphous GaO_x show that the electron affinity is similar to CIGSe due to oxygen deficiency.

This understanding leads to new concepts to overcome the efficiency limitations. In this work the use of doped amorphous oxide diffusion barriers is tested. Ga₂O₃ deposited at low temperatures and without intentional doping is shown to perform best. Nevertheless the devices still suffer from acceptor states, in this case at the CIGSe/GaO_x interface.

The efficiency of the CIGSe/ZnO devices could be substantially increased to above 10% by doping the CIGSe layer with Na. This was shown to be a sensitive process step, as Na, tends to accumulate within the GaO_x layer, and, similar to Cu, induces acceptor states within it. The device degradation and the previously reported effect of forward-biasing is assumed to originate from electro-migration of Na within the *p/n*-junction. A low-rate post-deposition of NaF could reduce the Na concentration at the interface and leads to a stable device efficiency of up to 11%.

Zn diffusion from the ZnO into the CIGSe absorber is shown to lower the *p*-type doping and the electron lifetime within the CIGSe. Device simulations however indicate, that this does not limit the device efficiency substantially and that Na reduces the negative effect of the Zn contamination.

Further it is shown, that the Au back contact can be substituted by MoO_x/Ag without sacrificing the device efficiency. Simulations suggest that the high reflectivity and high scattering of this type of back contact leads to a possible reduction of the CIGSe layer thickness down to 600 nm, while maintaining the same efficiency as a substrate device with a 1000 nm thick CIGSe layer. Another advantage of the superstrate configuration was shown to be the defect annealing within the ZnO during the CIGSe deposition. This increases the electron mobility and the overall sub-band gap transparency.

Band gap engineering by Ga and S is shown to be well implementable, making the superstrate configuration very attractive provided that a Cu tolerant buffer layer can be found in the future.

Zusammenfassung

Die vorliegende Arbeit untersucht die Chancen und die Limitierungen von Cu(In,Ga)Se₂ (CIGSe) Solarzellen in Superstratkonfiguration. Diese im Vergleich zur gewöhnlichen Substratkonfiguration invertierte Schichtstruktur, stellt neue Anforderungen an die Materialeigenschaften ihrer Schichtkomponenten. Dies führt unter anderem zur Untauglichkeit der generell verwendeten CdS-Pufferschicht, aufgrund deren geringen thermischen Stabilität. Bei der direkten Abscheidung von CIGSe auf ZnO ist bekannt, dass sich eine dünne GaO_x-Schicht an der Grenzfläche bildet. Der Einfluss dieser Schicht war bisher ungeklärt, weshalb die Grenzflächenbildung und deren Einfluss auf die Solarzelleneigenschaften hier eingehend untersucht wurde.

Ein numerisches Bauteilmodell wurde aufgestellt, welches die Solarzelleneigenschaften bei unterschiedlichen Grenzflächeneigenschaften konsistent erklären kann. Mit der Hilfe dieses Modells wird gezeigt, dass der typischerweise niedrige Wirkungsgrad durch tiefe Akzeptorzustände im GaO_x verursacht wird und nicht, wie bislang angenommen, durch eine zu niedrige Elektroneffinität des GaO_xs. Es konnte bestätigt werden, dass amorphes Ga₂O₃ eine Elektronenaffinität ähnlich zu der von CIGSe besitzt. Direkt an der Grenzfläche durchgeführte Photoelektronenspektroskopiemessungen zeigen, dass die GaO_x-Schicht sowohl mit Cu als auch mit In verunreinigt ist. Die Cu-Verunreinigung wird als Ursache für die Akzeptorzustände vermutet, während die In-Verunreinigung die Aktivierungsenergie der Rekombination an der CIGSe/GaO_x Grenzfläche vermindert. Aus Tiefenprofilen der Elemente geht hervor, dass die Konzentration von In und Cu in der GaO_x-Schicht stark von dem verwendeten CIGSe-Abscheidungsprozess abhängen. Die Schicht mit der geringsten In- und Cu-Verunreinigung führt zu dem höchsten Wirkungsgrad, welcher jedoch weiterhin durch die Cu induzierten Akzeptorzustände im GaO_x limitiert ist. Die Zn-Diffusion aus dem ZnO in den CIGSe-Absorber hat sich als schädlich aber nicht limitierend herausgestellt.

Diese Erkenntnisse führten zu neuen Ansätzen zur Effizienzsteigerung. In dieser Arbeit wurden dotierte amorphe Oxidschichten geprüft, um die Cu-Diffusion zu reduzieren und die Akzeptorzustände zu kompensieren. Amorphes Ga₂O₃ hat zu den besten Ergebnissen geführt. Die Limitierung durch Akzeptorzustände, in diesem Fall an der CIGSe/Ga₂O₃ Grenzfläche, bleibt jedoch bestehen.

Der Wirkungsgrad in den CIGSe/ZnO-Solarzellen konnte durch eine kontrollierte Na-Dotierung wesentlich erhöht werden. Dabei hat sich herausgestellt, dass Na, ähnlich wie auch Cu, Akzeptorzustände an der Grenzfläche verursacht. Diese führen darüber hinaus zu einer Degradation der Solarzelle, angetrieben durch die Migration von Na im elektrischen Feld des *p/n*-Übergangs. Eine NaF-Nachbehandlung mit geringer Diffusionsrate ermöglichte eine Dotierung der CIGSe-Schicht ohne eine wesentliche Erhöhung der Na Konzentration an der Grenzfläche zu verursachen. Auf diese Weise konnte ein zeitlich stabiler Wirkungsgrad von 11.0% erreicht werden.

Des Weiteren wird gezeigt, dass es möglich ist, MoO_x/Ag als Rückkontaktmaterialien zu verwenden. Simulationen deuten darauf hin, dass die hohe Reflektivität des Rückkontaktes eine Reduzierung der CIGSe Schichtdicke von 1000 nm auf 600 nm erlaubt. Die CIGSe-Abscheidung führt zudem zu einem Ausheizen von Defekten im ZnO. Dies erhöht die Elektronenbeweglichkeit im ZnO und dessen Transparenz unterhalb der Bandlücke. Eine Aufweitung der Bandlücke an den Grenzflächen durch Ga und S Gradienten wurde als praktisch anwendbar aufgezeigt, was die Anwendung der Superstratkonfiguration als Ganzes attraktiv macht, vorausgesetzt eine Cu tolerante Pufferschicht wird verfügbar.

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Symbols and Abbreviations

$\Delta E_{C/V,BC}$	CBM/VBM gradient within CIGSe at the back contact	I_P	Ionization potential
$\Delta E_{C/V,S}$	CBM/VBM gradient within CIGSe at the hetero-junction	χ	Electron affinity
$\Delta E_{C,IF}$	CBM offset at the hetero-junction	$S_{n,h}$	interface recombination velocity for electrons and holes
E_F	Fermi level	E_g	Band gap
N_A	Acceptor state density	R_S	Series resistance
E_B	Binding energy	R_P	Parallel resistance
α	Absorption coefficient	ϕ	Work function
L_n	Electron diffusion length	N_D	Donor state density
l	Diode quality factor	$E_{F,n}$	Electron quasi Fermi level
J_{SC}	Short circuit current density	$E_{F,h}$	Hole quasi Fermi level
J_0	Saturation current density	d_{SCR}	Space charge region width
V_{OC}	Open circuit voltage	SP	Stoichiometry Point
FF	fill factor	XRD	X-ray Diffraction
η	Power Conversion Efficiency	CIGSe	Cu(In,Ga)Se ₂
VBM	Valence Band Maximum	DOS	Density Of States
CBM	Conduction Band Minimum	SCR	Space Charge Region
LLS	laser light scattering	CIGSe	CuInSe ₂
ILR	Infrared Light Reflectometry	CGSe	CuGaSe ₂
WLR	White light Reflectometry	PDT	Post Deposition Treatment
PVD	Physical Vapour Deposition	PLD	Pulsed Laser Deposition
GDOES	Glow Discharge Optical Emission Spectroscopy	XPS	X-ray Photoelectron Spectroscopy
TCO	Transparent Conductive Oxide	EBIC	Electron Beam Induced Current
SCAPS	Solar cell Capacitance Simulator	TEM	Transmission Electron Microscopy
EQE	External Quantum Efficiency		

Introduction

The highest reported efficiency of CIGSe solar cells is currently at 21.7% for devices in substrate configuration and is expected to further increase in the future [1]. But despite the highest efficiency of all thin film materials, it is not CIGSe, but CdTe which is leading the thin film solar cell market. CdTe has lower production costs [2] partially due to the easily up-scalable deposition process of CdTe and partially due to its superstrate device structure. But what are the advantages of the superstrate configuration? To answer this, Fig.0.1a shows the breakdown of the production costs for a framed CIGSe module in substrate configuration. The costs are dominated by the material costs and by the depreciation, the latter depending strongly on the processing time per module [3]. A breakdown of the total CO₂ footprint in Fig.0.1b shows that the two glass sheets and the electricity used during the high temperature CIGSe deposition dominate the CO₂ emission. Thus both factors, costs and CO₂ emission, can be strongly reduced by eliminating one glass sheet and by reducing the processing time and the material usage. This is where the superstrate configuration has its benefits. The thickness of the TCO layer can be reduced in the superstrate configuration as it allows improving the electro-optical properties due to the deposition on a flat substrate and a subsequent annealing. The back contact can be designed for high light reflection, allowing the use of thinner CIGSe absorber layers. Materials like Ag, Cu or Al would also allow a reduction of the thickness of the back contact layer. Another advantage is that the encapsulate can be opaque, which allows the elimination of one glass sheet and with it a quarter of the total material costs of a module [4].

The drawback of the superstrate configuration is that the highest reported efficiency for devices in superstrate configuration is a non-certified and unstable efficiency of 12.8%, which was reported in 2001 [5]. This is due to the difficulty to achieve a defined *p/n*-junction at the high CIGSe deposition temperature. Chemical reactions between the CIGSe and the buffer layer was shown to deteriorate the *p/n*-junction which leads to lower efficiencies compared to the substrate-type device. For superstrate devices without buffer layers the TCO window reacts with the CIGSe absorber, forming a GaO_x interfacial oxide layer at the CIGSe/TCO interface [6]. However, the influence of this oxide layer on the electric device properties is poorly studied and not yet understood. Also the influence of the CIGSe deposition conditions onto the formation of this interfacial oxide layer was not yet investigated. Sodium, which is key to achieve highly efficient CIGSe devices in

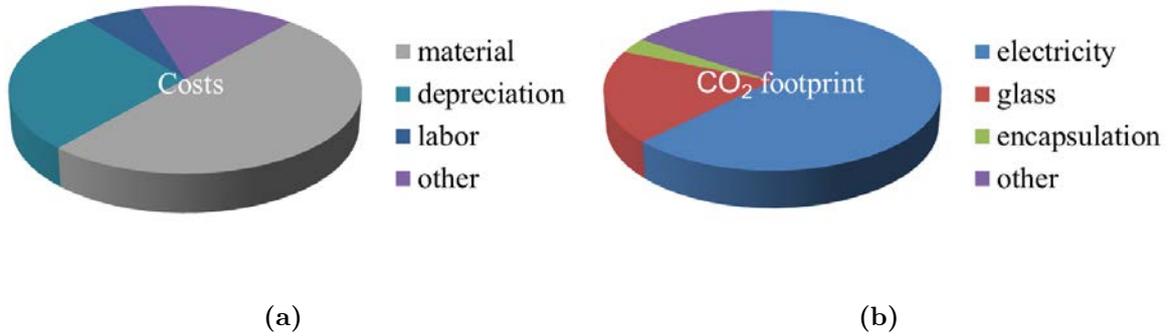


Figure 0.1: Break down of **a)** the costs involved for the production of a CIGSe module [3] and **b)** the CO₂ footprint of the production of an unframed CIGSe module [7].

general, was shown to lead to meta-stabilities in superstrate devices, whereas the deeper relationship still remain in the dark [5].

The aim of this work is to develop an understanding for the correlation of the interface chemistry at the CIGSe/TCO interface, the efficiency limitations and the degradation mechanisms of superstrate solar cells. Pathways to overcome these limitations and increase the efficiency will be discussed and partially tested. Proof for the above mentioned advantages of the superstrate configuration will be given as well.

This thesis is organized in the following way. After introducing the basics (Ch. 1-3), the most suitable TCO for CIGSe superstrate will be evaluated (Ch. 4), which will be studied in depth (Ch. 5-6), followed by the device simulations (Ch. 7), from which new strategies for efficiency improvement will be derived (Ch. 8).

Chapter 1: An introduction to the basics of a CIGSe solar cell and to its main active materials. Literature review for the state of the art of CIGSe superstrate cells is reported. Thermo-dynamical calculations are presented for possible interface reactions between a TCO and CIGSe.

Chapter 2: Introduction to the experimental details of the fabrication and the characterization of CIGSe devices as used in the course of this thesis. The basic knowledge required to understand the characterization methods is given as well.

Chapter 3: Introduction to the numerical device simulations. Exemplary simulations show the effects of defects at the interface between CIGSe and a TCO.

Chapter 4: Evaluation of different standard TCOs.

Chapter 5: Analysis of the CIGSe/ZnO interface chemistry and its influence on the electronic properties of the solar cell in superstrate and in substrate configuration.

Chapter 6: The effect of Cu deficiency on the back contact is studied. Degradation mechanisms occurring at the interfaces to the TCO and the back contact are analysed.

Chapter 7: Device simulations of the $J-V$ and $C-V$ curves of the studied superstrate solar cell. Together with the results from Chapter 5 and 6 the efficiency limitations are identified or confirmed. The device properties are correlated to the device properties of the solar cells in substrate configuration.

Chapter 8: Discussion of different strategies for efficiency improvement. Application of new buffer materials deposited by combinatorial material exploration.

Additional information:

- Detailed opto-electronic and XPS analysis of amorphous GaO_x .
- Influence of sulphur gradient on the reduction of interface recombination.
- Experimental and theoretical proof of potential optical advantages of the superstrate configuration. ZnO annealing and etching as well as highly reflective back contacts are studied.
- Influence of the ZnO substrate on the morphology of the CIGSe morphology.
- Information about CIGSe tandem solar cells.

Chapter 1

CIGSe solar cell basics

1.1 Cu(In,Ga)Se₂ Solar Cells

This first section will introduce the working principle of a solar cell, the energy band alignment at the CIGSe/Oxide interface, the superstrate configuration and the state of knowledge about it, the material basics and the thermodynamics at the CIGSe/Oxide interface. More in depth information about general solar cells can be found in [8] and on CIGSe solar cells in [9].

1.1.1 Physics of a Solar Cell

A solar cell is a device that converts the energy of light directly into electrical energy by the photovoltaic effect [10]. During this process, an electron within a semi-conductor becomes energetically excited by the absorption of a photon. For photon energies above the semi-conductor band gap, the electron becomes excited from the valence band into the conduction band and becomes spatially separated from the positively charged hole by diffusion. Electron and hole selective contacts to the semi-conductor lead to the permanent separation of the electrons and the holes, creating a potential difference between these contacts which can be used to drive an electric current.

The electron selective contact in a CIGSe solar cells is realized by a p/n -junction and the hole contact by a metal with a similar work function as CIGSe. A p/n -junction develops at the interface between the p -type CIGSe material, which has a high density of mobile holes, and a n -type material, like ZnO, which has a high density of mobile electrons. Once both materials are brought into contact, the free electrons from the n -type material diffuse into the CIGSe and recombine with the free holes in the CIGSe, leading to a negatively charged region in the CIGSe and a positively charged region in the n -type material, together this forms the so-called space charge region (SCR). Fig. 1.1 illustrates this situation. Due to the charge separation an electric field is generated, which limits the diffusion of the electrons and holes leading to an equilibrium between drift and diffusion. It should be noted at this point, that this field can also cause electro-migration of highly mobile ions, like Cu⁺ or Na⁺, which will become important later in this work.

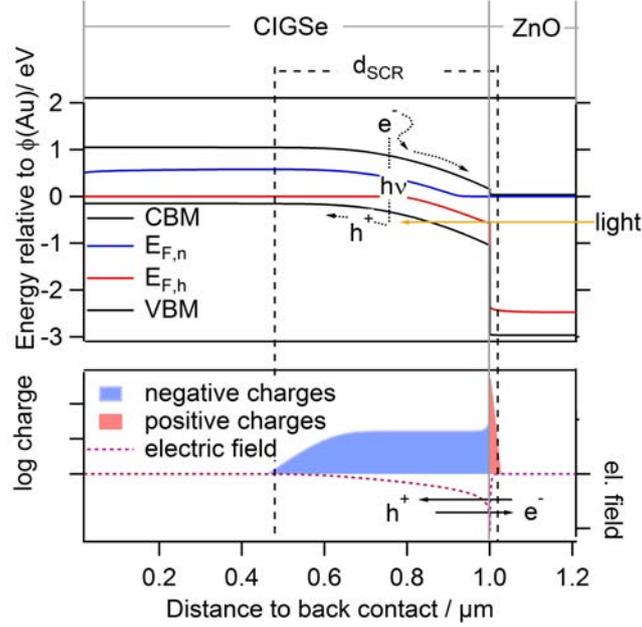


Figure 1.1: Top: Band diagram of a CIGSe/ZnO solar cell calculated with SCAPS (top). The CIGSe layer is 1 μm thick and the ZnO layer 200 nm. The conduction band minimum (CBM) and the valence band maximum (VBM) is shown together with the electron and hole quasi Fermi levels, $E_{F,n}$ and $E_{F,h}$. The space charge region of the p/n -junction under 100 mWcm^{-2} illumination is marked with the dashed line. The charge separation at the hetero-junction lead to an electric field (bottom). The local gradient of the quasi Fermi level, determine the flow of the photo-generated charge carriers. Bottom: The charge distribution within the SCR and the resulting electric field, which drives the electron into the n -type material.

The equilibrium between drift and diffusion of the charge carriers is equivalent to a flat Fermi level throughout the device, which tells that the chemical potential of the electrons is the same everywhere within the device. During illumination electron-hole pairs are created and the Fermi distribution becomes different for electrons and holes. This requires the introduction of the quasi-Fermi level for electrons, $E_{F,n}$ and the quasi-Fermi level for holes, $E_{F,h}$ [11], as shown in Fig. 1.1. During illumination, the quasi-Fermi levels are not flat within the CIGSe, thus electrons can lower their potential energy by moving to the minimum of the electron quasi-Fermi level, which is located in the n -type material.

In case that the p -type material and the n -type material are different from each other, the junction is called hetero-junction. Different electron affinities, $\chi_{n/p}$, and/or different band gaps, $E_{g,n/p}$, of these two materials lead to band offsets at the CBM or the VBM respectively. This is shown in Fig. 1.2 for the example of CIGSe and ZnO. The electron affinity is defined as the difference between the vacuum energy level and the CBM. If $\chi_p < \chi_n$ is valid, the offsets can be approximated by the following equations (Anderson's law [12]), shown here for the example of CIGSe and ZnO:

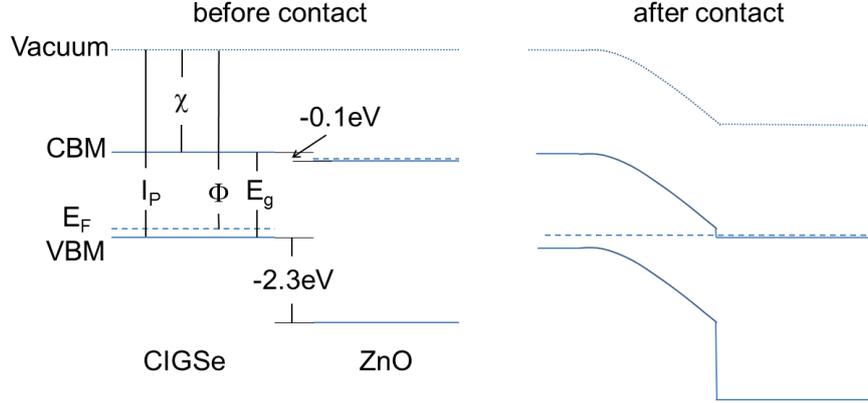


Figure 1.2: Band diagram of CIGSe and ZnO before and after contact. Shown are the vacuum levels, the conduction band minima (CBM), the valence band maxima (VBM), the work function (Φ), the electron affinity (χ), the ionization potential (I_P), the band gap (E_g) and the CBM and VBM offsets between CIGSe and ZnO.

$$\Delta E_{C,IF} = \chi_p - \chi_n = \chi_{CIGSe} - \chi_{ZnO} = 4.5\text{eV} - 4.6\text{eV} = -0.1\text{eV}, \quad (1.1)$$

$$\begin{aligned} \Delta E_{V,IF} &= (\chi_p + E_{g,p}) - (\chi_n + E_{g,n}) = (\chi_{CIGSe} + E_{g,CIGSe}) - (\chi_{ZnO} + E_{g,ZnO}) \quad (1.2) \\ &= (4.5\text{eV} + 1.2\text{eV}) - (4.6\text{eV} + 3.4\text{eV}) = -2.3\text{eV}. \end{aligned}$$

Especially the conduction band offset $\Delta E_{C,IF}$ has a strong influence on the recombination losses in CIGSe solar cells as will be discussed in Sec. 3.1 and Sec. 3.2.

Loss mechanisms during the conversion from light to electrical energy are thermal relaxation of the excited electron, as illustrated in Fig. 1.1, entropy generation, optical losses as well as radiative and non-radiative recombination. The non-radiative recombination losses are described in Sec. 3. The conversion efficiency is extracted from the plot of the photo-generated current density over the photo-voltage, the so-called $J - V$ curve, which is explained in Sec. 2.4.1.

1.1.2 The superstrate configuration

This work studies CIGSe solar cells in the superstrate configuration. In this configuration, the light passes through the substrate, which is commonly glass, onto which the active layers are deposited. Thus, during normal operation the substrate is above the active layers and the configuration is therefore called superstrate. This is shown in Fig. 1.3 together with the standard substrate configuration.

Within the substrate configuration the CIGSe is deposited onto the hole collecting material, which is usually Mo. The p/n -junction is formed by the deposition of the n -type materials CdS and i-ZnO. CdS is called the buffer layer between CIGSe and ZnO, as it reduces the interface recombination velocity at the hetero-interface to CIGSe due to

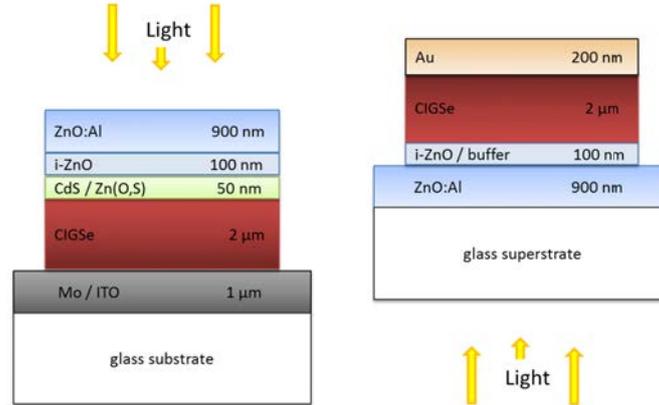


Figure 1.3: Substrate (left) and superstrate (right) configuration of CIGSe solar cell devices (not to scale). In the example for the substrate device, the window layer material is ZnO:Al/i-ZnO, the buffer layer CdS or Zn(O,S), the back contact Mo or if optical transparency is required ITO. In the example for the superstrate device, the window layer material is ZnO:Al, the buffer layer i-ZnO and the back contact Au.

a better lattice match [13], better conduction band alignment [14] and a better chemical compatibility [15] to CIGSe compared to ZnO. Between the window layer ZnO:Al and the buffer layer CdS, a thin highly resistive layer of i-ZnO is used to reduce the impact of shunts on the device performance [16].

In the superstrate configuration the CIGSe layer is deposited onto the electron collecting window layer, which is ZnO:Al. In between the window layer and the CIGSe the i-ZnO is inserted similar as in the substrate configuration. However, the buffer layer is dismissed, since CdS as the buffer layer material is not suitable due to its low thermal stability (see Tab.1.2). The back contact is deposited onto the CIGSe absorber which is typically Au. Mo is not used as the successful application requires the formation of an interfacial MoSe_x layer at the interface to CIGSe, but this forms only at high temperatures. In addition, for optimum performance, the CIGSe deposition process should be altered in order to invert the Ga gradient, which can be used to increase the charge carrier collection efficiency.

From the technological point of view, the superstrate configuration leads to the following advantages and disadvantages:

1. Increased quality of the transparent conductive oxide (TCO), since the TCO can be deposited on a flat substrate and deposited at whatever temperature is optimal for the specific TCO. In case that ZnO:Al is used, annealing in nitrogen was shown to strongly increase the transparency and conductivity [17] (see Sec. 10.3.1 for more details). Further, in [18] it was shown that the conductivity of ZnO:Al drops if deposited on rough substrates like CIGSe surfaces. The rough surface leads to an accelerated ZnO degradation [18].
2. The p/n -junction undergoes the high temperature CIGSe deposition step. This leads

to unwanted inter-diffusion (as Zn diffusion) and possible phase transformations (as GaO_x formation [6]). See Sec. 5.1 for more details.

3. The back contact can be designed to achieve low back contact recombination in combination with high light reflectivity and strong light scattering. This would allow the use of thinner CIGSe layers, which helps to lower the high material costs, especially for indium. See Sec. 10.3.2 for more details.
4. Device encapsulation from the back side can be opaque and flexible, which may lower the costs compared to a second glass sheet as used for substrate devices. The disadvantage is, that the supporting substrate has to be transparent, which makes it difficult to use flexible substrates like metal foils.

In addition, to achieve all chalcopyrite 4-terminal tandem devices, it is necessary to prepare the wide-gap chalcopyrite in superstrate configuration. This will be discussed in Sec. 10.5.

1.1.3 Literature review

The first efficient chalcopyrite superstrate devices were reported in 1994 by Nakada et al. [19] and by Negami et al. [20], both with CdS as the buffer layer. The CdS was observed to diffuse into the CIGSe absorber at deposition temperatures of 450 °C and above, which limited the device efficiency to 8.1 %. Dismissing the CdS buffer and the use of Ga containing CIGSe, lead to an increase in device efficiency above 10 %, reported in [5] and [21].

In both reports, the CIGSe was deposited at 550 °C on top of an i-ZnO layer. The formation of a thin layer of GaO_x between the i-ZnO and the CIGSe was observed [6], as well as meta stabilities when applying a voltage bias or light bias [21] [5].

The highest efficiency reported so far, 12.8 %, was achieved in 2001 by Nakada et al. by applying a forward bias to the finished device, which enhanced the efficiency from 2 % to 12.8 % [5]. The Cu/(In+Ga) ratio was 0.44, which corresponds to the ordered vacancy phase Cu(In,Ga)₃Se₅. Higher Cu contents lead to shunting of the device. 30 mg of Na₂S was deposited during the CIGSe deposition, leading to a Na concentration of approximately 2 at.% within the CIGSe. In the experiments conducted for this thesis, it was not possible to reproduce these results with similar experimental conditions.

The second report on superstrate devices with efficiencies above 10 % is from Haug et al. [21] in 2002. An efficiency of 11.2 % for slightly Cu poor absorbers without any external sodium supply. Extensive light soaking was required to increase the efficiency from 5 % temporarily to above 11 %. The light soaking was observed to increase the charge carrier density in the device [22].

Another interesting approach was reported by Minemoto et al. [23], who exchanged the i-ZnO layer with ZnMgO which was shown to reduce the interface recombination. The ZnMgO was deposited by RF co-sputtering without intentional heating. By depositing the CIGSe absorber at a low temperature of 450 °C they achieved 9.0 % efficiency. Kaigawa et

Table 1.1: Overview of the published results on CIGSe superstrate solar cells. All reports use i-ZnO buffer layers if not noted else wise.

Author	PCE	Speciality	Stability
[5] Nakada	12.8 %	ODC absorber, Na ₂ S, forward bias	unstable
[21] Haug	11.2 %	light soaking	unstable
[26] this work	11.0 %	low-rate NaF PDT	stable
[23] Minemoto	9.0 %	ZnMgO buffer	-
[19] Nakada	8.1 %	CdS buffer	-
[20] Negami	6.7 %	CdS buffer	-
[27] Shafarman	4.0 %	ZnSe buffer	-
[28] Kaigawa	3.8 %	Cu(In,Ga)S ₂	-
[29] Balboul	3.5 %	CuGaSe ₂	-
[30] Ikeda	2.9 %	In ₂ (S,Se) ₃ buffer	-
[31] Nguyen	2.1 %	spray pyrolysis CIGSe -	-

al. prepared wide gap Cu(In,Ga)S₂ onto ZnO substrates and achieved 3.8 % by a two stage process. Balboul et al. also processed wide gap CuGaSe₂ and reached 3.5 %. Shafarman and co-workers currently work on superstrate CIGSe devices and have reported efficiencies up to 5.1 % for i-ZnO buffer layers and 4.0 % for ZnSe buffer layers. Recently Ohm et al. tried to grow CIGSe on ZnO nanorods, but due to strong interface recombination losses the efficiency could not be increased above 2 % [24].

Back-wall superstrate devices, which have a transparent back contact and are illuminated through this transparent back contact have been realized by Shafarman et al. with an efficiency of 8.3 % [25]. The efficiency in this case was limited by the back contact recombination. This approach is in this thesis not further pursued.

In summary, the best results have been obtained with i-ZnO/CIGSe junctions. However, intensive light- or voltage- soaking were required to achieve efficiencies above 10 %. In both cases the formation of GaO_x were observed, which were assumed to induce a CBM spike. However, only few studies on CIGSe superstrate devices were done and the influence of the GaO_x layer, of sodium supply and of the biasing/ageing is not yet understood.

1.2 Thermodynamics of the interface reaction

The difficulty of designing a defined *p/n*-junction is the difficulty to understand and to control the thermodynamics at the interface between the *p*-type and the *n*-type material. Thermodynamic processes like diffusion or chemical reactions at this interface can determine the electronic properties of the whole device, as it will be seen in the case of CIGSe grown on ZnO in Sec. 5.1. The physics involved in these processes will be introduced in this chapter. The tools which are available to control these processes are temperature, time and chemical composition.

1.2.1 Gibbs free energy

The “driving force” of all thermodynamic processes is the minimization of the Gibbs free energy of a given isolated system. Therefore a reaction from one state of a system to another state is favourable if $\Delta G < 0$. The change of the Gibbs free energy, ΔG , is defined as follows:

$$\Delta G = \Delta H - T\Delta S, \quad (1.3)$$

with T the temperature, ΔS the change of entropy and ΔH the change of enthalpy during the potentially occurring reaction. Thus, ΔG becomes negative if ΔH decreases or ΔS increases. The entropy is defined as the amount of energetically equivalent arrangements of a given system. An increase of entropy therefore increases the disorder within the system. Diffusion along a defined interface will lead to an increase in entropy, due to an increase of disorder. The enthalpy is defined as $H = U + pV$, with U the internal energy, p the pressure and V the volume of the system. At constant pressure a change in enthalpy is therefore equivalent to a change in volume or heat of the system. A chemical reaction is mostly driven by a reduction of the enthalpy of the system, for example an increase of inter-atomic binding energy. With ΔS and ΔH defined as:

$$\Delta H = H(\text{products}) - H(\text{reactants}) \quad (1.4)$$

$$\Delta S = S(\text{products}) - S(\text{reactants}), \quad (1.5)$$

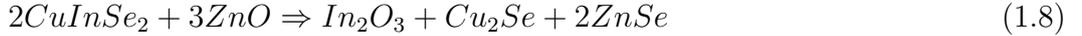
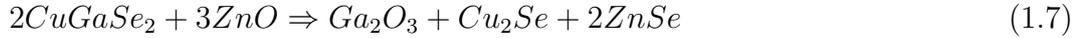
with $S(\text{products})$ and $H(\text{products})$ being the entropy and enthalpy of all products, $S(\text{reactants})$ and $H(\text{reactants})$ of all reactants. Since the enthalpy is a potential energy and cannot be measured, it is set to 0 for single elements at the standard state of 293 K and 1 atm. The so-called “enthalpy of formation” ΔH of a compound system, like CuInSe_2 , is then referred to the standard enthalpy of the constituting materials, Cu, In and Se. It follows for a phase transformation $\Delta H = \Delta H(\text{phase1}) - \Delta H(\text{phase2})$ and $\Delta S = \Delta S(\text{phase1}) - \Delta S(\text{phase2})$.

A reaction can spontaneously occur if $\Delta H < T\Delta S$ is fulfilled. Thus, at higher temperatures, the equilibrium between disorder and locally defined stable phases is pushed towards disorder. To perform the exact calculations for a given system at temperatures different from 293 K it is necessary to know the temperature dependence ΔH and ΔS , which depend on the heat capacity at constant pressure $C_p (= \Delta H / \Delta T = a + bT + c/T^2 + \Delta T^2)$ of the compound. Further, starting from a certain concentration of different elements present locally within a small volume a large amount of different phases have to be considered which can possibly occur. Commercial programs like ChemSage [35] are able to calculate the phase equilibriums at any given temperature from a given molar concentration of starting materials or compounds. The advantage of these programs is the large database of enthalpies, entropies and heat capacities for a large selection of different compounds. Results of the calculations for the interface of ZnO with $\text{Cu}(\text{In,Ga})\text{Se}_2$ or the binary compounds Ga_2Se_3 , In_2Se_3 and Cu_2Se at 1 bar and 900 K are shown below. It should be noted however, that no temperature dependence of these reactions could be observed and

Table 1.2: Standard enthalpies of formation and standard entropies of different compounds at 293 K and in solid state, taken from [32], [33] and [34]. The values for Cu(In,Ga)Se₂ are interpolations of the CuInSe₂ and CuGaSe₂ values.

Compound	$\Delta H / \text{kJ mol}^{-1}$	$S / \text{J K}^{-1}\text{mol}^{-1}$
CuInSe ₂	-262	158.0
CuGaSe ₂	-313	147.0
Cu(In,Ga)Se ₂	-273	160.0
ZnO	-350	43.6
Ga ₂ O ₃	-1089	84.9
In ₂ O ₃	-926	104.1
SnO ₂	-581	52.3
Ga ₂ Se ₃	-408.8	179.9
In ₂ Se ₃	-309	163.6
Cu ₂ Se	-65	129.7
ZnSe	-170	77.6
CuGaO ₂	-637	83.2
Cu ₂ O	-198	93
MoO ₃	-745	77.8
CdS	-177	

calculations for 300 K lead to the same results.



The higher enthalpy of formation of Ga₂O₃ and In₂O₃ compared to ZnO leads to a complete cation exchange of the oxide and the selenide. If In and Ga are present simultaneously, then oxygen binds preferably the gallium atoms. It has to be kept in mind, that these calculations only indicate preferable reaction mechanism. The change in free energy for the reaction of ZnO with In₂Se₃ is -528 kJ/mol which is very close to the change in free energy for the reaction with Ga₂Se₃, which is -581 kJ/mol.

Also other TCOs like SnO₂ and In₂O₃ are all predicted to selenize, once they are in contact with Ga₂Se₃:



Even though the change in the free energy is only -53 kJ/mol for the reaction of Ga₂Se₃ with In₂O₃, it has been observed experimentally [36].

Only Cu₂Se is predicted not to react with ZnO. At elevated temperature however, the entropy becomes more important and diffusion of Cu into the ZnO is expected to occur. Also, it has to be kept in mind, that these calculations do not take the reaction kinetics into account, which potentially limits the cation exchange between the materials at low temperatures. Thus even though the reactions are proposed to occur at room temperature it is likely that they are limited by slow diffusion processes, which will be introduced in the next section.

1.2.2 Diffusion

As described above, inter-diffusion between the elements of two adjacent layers, is driven by an increase in entropy and a reduction of the free energy of the system. The change of the concentration N of a certain element at the position x over the time t depends on the concentration gradient of that element at that point [37]. In the one dimensional case and a spatially constant diffusion constant D , this can be written as

$$\frac{\partial N}{\partial t} = D \frac{\partial^2 N}{\partial x^2}. \quad (1.15)$$

The diffusion constant describes the thermally activated hopping process of the elements or ions through a given crystal lattice. It can be described as follows:

$$D(T) = D_0 \exp(-E_A/kT), \quad (1.16)$$

with D_0 being the diffusion constant at infinite temperature and E_A the activation energy of the hopping mechanism. The hopping may occur between interstitial, vacancy or occupied lattice sites. For example, in [38] the diffusion constant for Zn in polycrystalline CIGSe and single crystal CIGSe was measured to be D_0 1.3e-12 cm²s⁻¹ with E_A 1.24 eV. A second, slower, diffusion mechanism was also identified. It was speculated that the faster diffusion mechanism is via Zn_i states and the slower one via Zn_{Cu}.

The shape of the diffusion profile depends on the boundary conditions at the material interfaces, on whether the material supply is limited or not. In the case of sodium doping, the supply is limited if a thin layer of NaF is deposited on the CIGSe layer prior to the annealing and it is unlimited if the NaF is deposited continuously with a low rate during annealing. In the case of an unlimited supply the diffusion profile has the form of an complementary error function:

$$N(x, t) = N_0 \operatorname{erf} \left(\frac{x}{2\sqrt{D(T)t}} \right), \quad (1.17)$$

with N_0 being the constant dopant concentration at the surface. In the case of limited supply, the surface concentration is described by the initial concentration $N_{0,i}$ and $N_0(t) =$

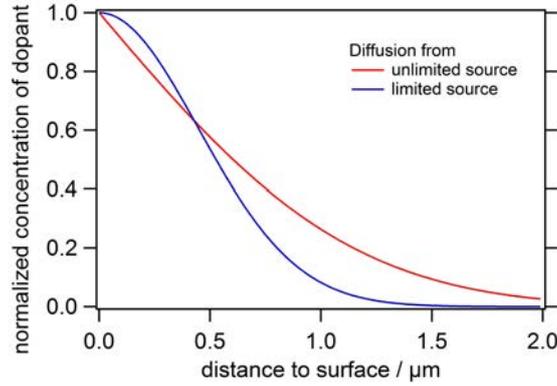


Figure 1.4: Normalized diffusion profile of a dopant diffusing into a material with a single diffusion constant

$-N_{0,i}/(2\sqrt{D(T)t\pi})$. In this case the profile decays exponentially with the square of the distance from the surface:

$$N(x, t) = N_0(t) \exp\left(-\frac{x^2}{4D(T)t}\right). \quad (1.18)$$

The resulting diffusion profiles depend strongly on the temperature and the time the system is held at this temperature. Fig. 1.4 compares the diffusion profiles for unlimited and for limited supply, both calculated with equal time, temperature and diffusion constants.

1.3 Material Characteristics

The materials which will be studied most within this thesis are CIGSe, ZnO and amorphous GaO_x . However, very little literature exists on amorphous GaO_x , why its electro-optical properties are studied in Sec. 10.1.

1.3.1 Cu(In,Ga)Se₂ (CIGSe)

CIGSe is one of the most successful absorber materials for thin film photovoltaic applications due to its high absorption coefficient, low density of deep defects and the possibility to engineer the band gap. This section will give a short overview of the crystal structure and the electronic structure.

CIGSe structure

The semi-conductor Cu(In,Ga)Se_2 belongs to the I-III-VI compounds and crystallizes in the chalcopyrite structure. The chalcopyrite is a superstructure of the ZnSe sphalerite structure with ordered substitution of Zn with Cu, In and Ga. The lattice has a body centred tetragonal order in which each Cu, In or Ga cation is tetrahedrally coordinated to

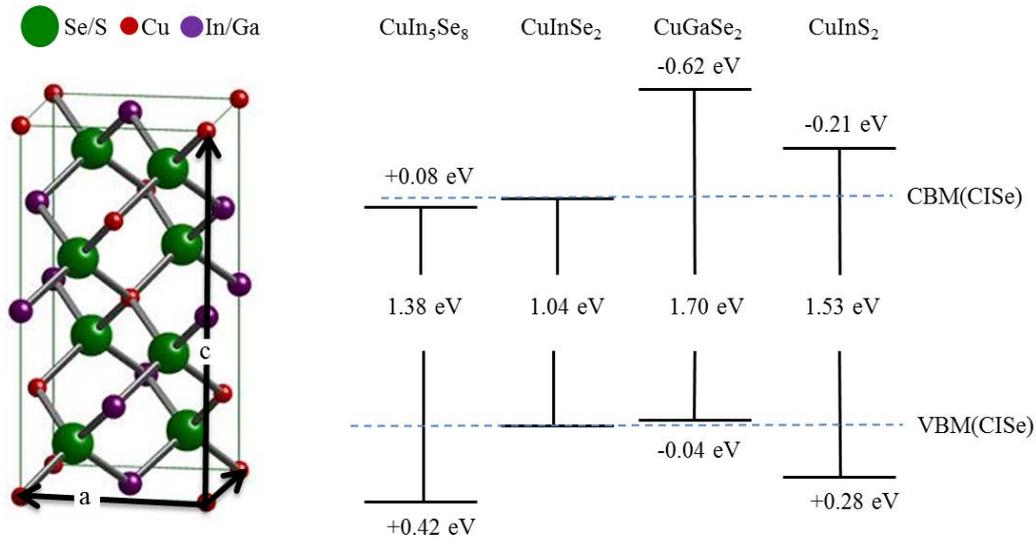


Figure 1.5: Tetragonal chalcopyrite structure of $\text{Cu}(\text{In,Ga})(\text{Se,S})_2$ shown together with the lattice parameters a (5.75 Å) and c (11.5 Å) for $\text{Ga}/(\text{Ga}+\text{In})=0.23$ and $\text{Se}/(\text{Se}+\text{S})=1$ (left). Image taken from [39]. Band gap values and relative position of the CBM and VBM for the different chalcopyrite compounds compared to the CMB and VBM of CuInSe_2 (second from left). Values taken from [40].

four Se anions and each Se anion is tetrahedrally coordinated to two Cu and two In/Ga atoms. The different bonding strength of the weak covalent Se-Cu bond compared to the partially ionic bond of Se-In or Se-Ga leads to a tetragonal distortion [41]. For the $\text{Ga}/(\text{Ga}+\text{In})$ ratio of 0.23 the distortion is compensated and the lattice parameter c equals twice the lattice parameter a . It was shown that poly-crystalline $\text{Cu}(\text{In,Ga})\text{Se}_2$ with this ratio, deposited via co-evaporation, exhibit a larger average grain size compared to other $\text{Ga}/(\text{Ga}+\text{In})$ ratios [42].

The band structure of $\text{Cu}(\text{In,Ga})\text{Se}_2$ is derived by density-functional (DFT) theory [43]. The valence band emerges from a hybridization of the Se $4p$ orbitals and the Cu $3d$ orbitals. A Cu deficiency therefore leads to a lowering of the valence band maximum [40]. Fig. 1.5 shows the lowered VBM of the ordered vacancy compound CuIn_5Se_8 compared to the CuInSe_2 compound. The conduction band is mainly derived from In $5s$ / Ga $4s$ and Se $4p$ orbitals. A change in the Ga/In ratio leads to a change in the position of the conduction band minimum (CBM) [44]. Fig. 1.5 shows the difference in the CBM of the CuGaSe_2 and the CuInSe_2 compound. Since Se p orbitals contribute to the valence and conduction band, the substitution of Se with S influences the position of the conduction and valence band [45], as shown in Fig. 1.5.

Defects in CIGSe

The relevant intrinsic defects within CuInSe_2 are listed in Tab. 1.3. The shallow defects in CuInSe_2 are the acceptor V_{Cu} and the donor In_{Cu} , which have low formation energies

Table 1.3: Properties of the native defects and defects which are possibly induced due to the diffusion of elements from ZnO into the CIGSe. The description "shallow" refers to defects energetically close to one of the bands and contribute to the conductivity, "deep" refers to localized states which act as recombination centers.

Origin	Defect	Type	Position in the band gap	Ref.
intrinsic	V_{Cu}	acceptor	shallow	[46]
	V_{In}	acceptor	deep	[46]
	Cu_{In}	acceptor	deep	[46]
	V_{Se}	donor	deep	[46]
	In_{Cu}	donor	shallow	[46]
	Cu_i	donor	deep	[46]
	$(V_{Se}-V_{Cu})^*$	amphoteric	shallow	[46]
from ZnO	O_{Se}	acceptor	deep	[47]
	Zn_{In}	acceptor	shallow	[15]
	Zn_{Cu}	donor	shallow	[15]
Alkali treatment	Na_{In}	acceptor	deep	[46]
	Na_{Cu}	neutral		[46]
	Na_i	donor		[46]

for Cu poor compositions, whereas the defects related to Cu rich compositions like Cu_{In} or Cu_i are deep defects which will degrade the electronic quality of the crystal. Within Cu poor crystals it is energetically favourable when two V_{Cu}^- acceptors and one In_{Cu}^{2+} donor form neutral defect pairs. This can lead to neutral chalcopyrite crystals even for strong off-stoichiometric conditions. Small deviations from the 2:1 defect ratio determine whether the crystal becomes p -type or n -type. Due to the very low formation energy of the acceptor V_{Cu} the deviation is generally directed towards p -type. Cu-poor $CuInSe_2$ can turn n -type by extrinsic doping as long as the Ga concentration is relatively low. For high Ga concentrations the formation energy of V_{Cu} becomes negative once the Fermi level increases to mid-gap, this increases the V_{Cu} concentration and compensates the n -type doping. Selen vacancies, V_{Se} are predicted to form amphoteric defect pairs with V_{Cu} , changing from donor to acceptor depending on the Fermi level position. This is often assumed to be the origin of the observed metastabilities in CIGSe [48].

Extrinsic defects can lead to a n -type conductivity in CIGSe with low Ga content [15], which could be beneficial at the CIGSe interface to the buffer material. Cd_{Cu} induced by a CdS buffer layer is a shallow donor in $CuInSe_2$, which qualifies CdS as a buffer layer in substrate devices. Zn_{Cu} is known to be a shallow donor as well, which qualifies Zn containing buffer layers as alternatives to CdS. However, Zn_{Cu} is not as shallow as Cd_{Cu} . In $CuInSe_2$, Zn_{Cu} is predicted to be 60 meV below the conduction band and for

CuGaSe₂ 110 meV [15], which could introduce recombination centres in the chalcopyrite. Zn_{In} is predicted to be a shallow acceptor lying within the valence band for CuInSe₂ and 70 meV above the valence band in CuGaSe₂. Assuming a similar trend as calculated for Cd [15], the formation energy for Zn_{Cu} is supposed to be smaller than for Zn_{In} under *p*-type condition. This predicts a preferential occupation of Cu sites resulting in an increase of donor states due to the presence of Zn. However, experimental observation on the closely related CuInS₂ system do not confirm these predictions. Neutron powder diffraction experiments showed a preferred occupation of In sites by Zn [49]. Enzenhofer et al. [50] reported a preferred occupation of In sites in the bulk of CuInS₂ and a preferred occupation of Cu sites at the Cu-poor surface. Similar results were obtained in [51]. Secondary ZnSe phases are unlikely to form, as Schorr et al. [49] found that a phase separation occurs only for molar concentrations above 8% of ZnSe in CuInSe₂.

Selen vacancies can be occupied by oxygen atoms, transforming the donor states into deep O_{Se} acceptors. Interestingly, CuInSe_{1-x}O_x was shown not to be stable and would decompose into CuInSe₂, In₂O₃ and Cu₂O [47]. Thus it is unclear whether oxygen acts as an acceptor or if it leads to the precipitation of binary phases.

Sodium is known to increase the *p*-type doping in CIGSe, if present at low concentrations [52]. It will preferably occupy Cu sites and Na_{Cu} is electrically inactive. However, Na_{InCu} neutralizes a double donor state, whereas Na_{VCu} neutralizes a single acceptor. Na_{VCu} has a higher formation energy as Na_{InCu}, which leads to the preferred occupation of In_{Cu} states by Na. This is believed to be the origin of the increased *p*-type doping density induced by sodium [47]. Photoluminescence measurements confirmed that the enhanced *p*-type doping originates from the annihilation of donor states and not from the formation of new acceptor states [53].

1.3.2 ZnO

ZnO is one of the most common TCOs used in photovoltaic devices, due to its wide band gap, high conductivity and relatively low material costs. In CIGSe devices, ZnO doped with Al or with Ga is usually used as the window layer and in superstrate devices intrinsic ZnO sometimes form the *p/n*-junction with CIGSe [54]. In this section the crystal structure, the band structure, the intrinsic and the extrinsic defects of ZnO will be summarized.

Structure

ZnO layers deposited on glass substrates crystallizes in the hexagonal wurtzite structure [55]. The structure is shown in Fig. 1.6 together with the lattice parameters *a* and *c*. The structure is composed of two inter-penetrating hexagonal-close-packed sub lattices for each type of atom, which are displaced to each other by one atom along the *c*-axis. Sputtered ZnO layers are polycrystalline and preferably grow in the [001] direction, which is along the *c*-axis.

The energy band structure resulting from DFT calculations for wurtzite ZnO is shown

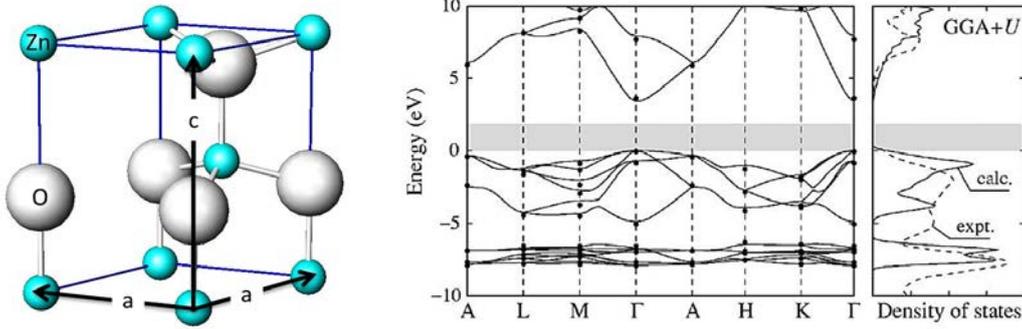


Figure 1.6: Unit cell of ZnO in the hexagonal wurtzite structure shown together with the lattice constants a (3.25 Å) and c (5.207 Å)(left) [60]. Corresponding band structure obtained from DFT calculations, corrected to the experimental band gap, whereas the grey stripe indicate the calculated band gap (right) [56].

on the right hand of Fig. 1.6. The direct band gap of 3.44 eV was corrected to the experimental value [56]. The valence band is derived from O 2*p* and Zn 4*s* orbitals. The conduction band is almost solely derived from Zn *s* orbitals [56]. Thus, alloying ZnO with MgO to (Zn,Mg)O influences the position of the valence band maximum and the conduction band minimum [57]. Alloying ZnO with ZnS to Zn(O_{1-x},S_x) shifts only the valence band maximum for low sulphur concentrations, $x < 0.3$. The conduction band is shifted as well for larger concentrations of sulphur [58]. The density of states (DOS) for the conduction and valence bands are shown in Fig. 1.6 as well. The low DOS at the CBM can cause an increase of the optical band gap, in case the ZnO becomes strongly *n*-type doped as described by the Burstein-Moss effect [59].

Defects

The energetic position of the native defects in ZnO were calculated by Janotti et al [61]. It was shown, that they do not contribute to the *n*-type conductivity of ZnO. The oxygen vacancies V_O are deep donors and can only compensate *p*-type doping, but cannot lead to *n*-type conductivity. The Zn interstitial Zn_i is a shallow donor, but has a high formation energy under *n*-type conditions, which limits the density of Zn_i defects. The same holds for Zinc antisites. Zinc vacancy V_{Zn} on the other side have low formation energies under *n*-type conditions. They are deep acceptors and partially compensate the *n*-type doping. The out-diffusion of Zn during the CIGSe deposition onto the ZnO would increase the V_{Zn} density and could be a potential source of *p*-type doping.

Oxygen interstitials and anti-sites can also act as acceptors but they have very high formation energies and are assumed to have no significant impact.

When growing CIGSe onto ZnO at temperatures between 400°C and 600°C, interdiffusion between these materials is likely to occur. Table 1.4 lists the possible generated defects by this process. The diffusion of Ga and In into ZnO increases the *n*-type conduc-

Table 1.4: Properties of the native defects and defects which are possibly induced due to the diffusion of elements from NaF doped CIGSe into the ZnO. The description "shallow" refers to defects energetically close to one of the bands and contribute to the conductivity, "deep" refers to localized states which act as recombination centers.

Origin	Defect	Type	Position in the band gap	Ref.
intrinsic	V_{Zn}	acceptor	deep	[61]
	V_O	donor	deep	[61]
	Zn_i	donor	shallow	[62]
CIGSe deposition	Cu_{Zn}	acceptor	deep	[63]
	Ga_{Zn}	donor	shallow	[64]
	In_{Zn}	donor	shallow	[64]
	Se_O	donor	deep	[65]
Alkali treatment	Na_{Zn}	acceptor	deep	[66]
	K_{Zn}	acceptor	deep	[66]
	Na_i	donor	shallow	[66]
	K_i	donor	deep	[66]
	F_O	donor	shallow	[62]

tivity, since they are common doping elements for ZnO by introducing the shallow donor states Ga_{Zn} and In_{Zn} [64]. Se is the least mobile atom within CIGSe, which makes the diffusion of Se into the ZnO unlikely. Se_O is assumed to be a deep donor [65] and should have no significant influence on the ZnO properties for low concentration.

The diffusion of Cu into ZnO is more critical since Cu is incorporated preferably on the Zn sites which leads to Cu_{Zn} acceptor states [63]. *P*-type conductivity was not yet achieved by Cu doping, since the Cu_{Zn} is too deep. Still, rectifying ZnO homo-junctions were claimed by doping ZnO with 3 at.% of Cu [67]. A problem of *p*-type doping ZnO is the compensating nature of the native V_O deep donor, whose formation energy drops and concentration rises with increasing *p*-type doping.

The diffusion of Na and K from the glass substrate or from the CIGSe absorber lead to amphoteric defects within the ZnO. For low concentrations they are predicted to form deep acceptor states due to the occupation of Zn sites, Na_{Zn} or K_{Zn} . However, once the Fermi level moves towards mid-gap, the formation energy of the Na_i and K_i becomes reduced and the Na_i and K_i donor states compensate the *p*-type doping [66].

Chapter 2

Experimental: Deposition and Characterisation

2.1 CIGSe growth

The CIGSe layers studied in this work were deposited by co-evaporation of Cu-In-Ga-Se, as this method allows a good controllability of the Ga-gradient and keeps the selenization of the underlying substrate to a minimum compared to selenization processes of metallic precursors. This section will shortly introduce the physical vapour deposition (PVD) system, the process control and the deposition process it self.

PVD Chamber

The evaporation of Cu-In-Ga-Se was done within a vacuum system, similar to a Molecular Beam Epitaxy (MBE) system, the so-called PVD-B chamber at the HZB, which is shown in Fig. 2.1. The deposition was performed at a background pressure of $1e-7$ mbar. The evaporation sources were effusion cells with pyrolytic boron nitride (PBN) crucibles for Cu, In, NaF and a vitreous carbon crucible for Ga. The source-substrate distance is 530 mm leading to a inhomogeneity of $\pm 3\%$ in the deposited layer thickness across a $200 \times 200 \text{ mm}^2$ deposition area. Selenium is supplied via a Valved Selenium Cracker Source (VSCS) which optionally provides thermally cracked selenium molecules (not yet used) and allows fast regulation of the Se flux. The substrate is heated by a resistive wire heater with a PBN ceramic diffuser. A maximum substrate size of $200 \times 200 \text{ mm}^2$ can be coated and heated uniformly. A cooling shroud fed with water is used to cool the inside walls of the PVD to limit re-evaporation of previously condensed material.

Process control

A **pyrometer** is used to measure the substrate surface temperature. It measures the thermal radiation at a fixed wavelength. The radiation intensity increases with the temperature to the power of four and linearly with the material emissivity. The latter re-

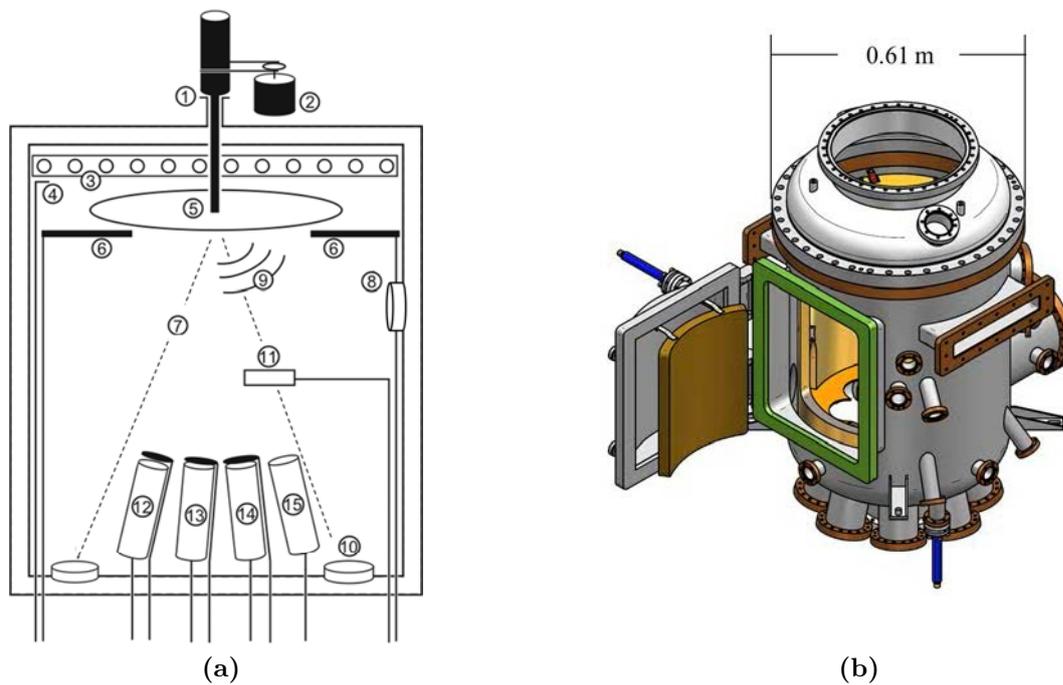


Figure 2.1: **a)** Schematic sketch of the PVD. 1. Manipulator; 2. Motor for substrate rotation; 3. Substrate heater; 4. Thermo-element; 5. Rotating substrate holder; 6. Substrate shutter; 7. ILR and LLS; 8. LLS detector; 9. IR detected by Pyrometer; 10. ILR detector; 11. Quartz crystal balance; 12.-14. Cu, In, Ga effusion cells; 15. Valved Se Cracker Source **b)** technical drawing of the PVD-B from Createc, showing the cooling shroud (yellow) within the PVD [68].

quires a calibration of the measured temperature, which can be the softening point of glass for example. **Laser light scattering (LLS)** is a common technique to control the co-evaporation process of CIGSe [69] [70] [71]. For this technique, chopped laser light, which is scattered from the growing film, is recorded by a Lock-In amplifier. The signal intensity is influenced by the film thickness, due to interference effects, by the film roughness, due to scattering, and by the refractive index of the growing film. Thus, changes in one of these parameters can be detected by LLS. The stoichiometry points (SP1 and SP2) are detected by the change of the refractive index induced by the segregation of a CuSe_x phase on top of the Cu-rich CIGSe surface. A He-Ne laser with a wavelength of 633 nm is used. Thus, the interference effect disappears the moment the band gap is low enough to absorb the laser light. **Infrared Laser Reflectometry (ILR)** records specular reflected monochromatic infrared light with $\lambda=1040$ nm. As the refractive index of the growing material is approximately known, the number of the interference maxima and minima are a measure for the film thickness during the deposition. **White Light Reflection (WLR)** is a relatively new process control which was first reported by [72] to get an exact value for the film thickness. Within this work the technique has been refined to allow exact band gap, roughness and defect absorption of the growing film. Within WLR the specular reflected white light is recorded with two diode arrays to cover the wavelength range from 400 nm to 1600 nm. The reflection spectrum depends on the thickness, roughness, band gap, Urbach energy and refractive index. As the refractive index can be reasonable approximated from literature values it is possible to extract all these parameters instantly. The technique is not yet applied to the CIGSe growth for superstrate solar cells.

CIGSe thin film deposition

The deposition process for the CIGSe absorbers followed a similar routine as the well-known 3-stage process [73], but is slightly modified to achieve a Ga profile, which is inverted compared to the standard process to account for the superstrate structure. The key of the 3-stage process is that the CIGSe layer is grown Cu-poor while it passes through a Cu-rich regime only close to the end of the deposition process. The Cu-rich regime induces a re-crystallization [74], which leads to reduced film stress [75] and crystallographic disorder [76]. Further, the Ga profile can be well controlled by this process. The modified 3-stage process used in this work will be shortly explained in the following. During all the three stages the Se deposition rate is kept constant at around 15 Å/s.

- 1st stage: Deposition of a layered $\text{Ga}_2\text{Se}_3/\text{In}_2\text{Se}_3/\text{Ga}_2\text{Se}_3/\text{In}_2\text{Se}_3$ stack at 300 °C substrate temperature. The thickness ratio of the Ga_2Se_3 layers to the In_2Se_3 determines the minimum Ga/(Ga+In) ratio and therefore the minimum band gap of the CIGSe device, as shown in Fig. 2.3. The layer stack has also been varied during this work as will be discussed later.
- 2nd stage: Co-evaporation of Cu-Ga-Se. The temperature is increased with 40 K/min to typically 525 °C in stage 2A. During this stage, the increased tem-

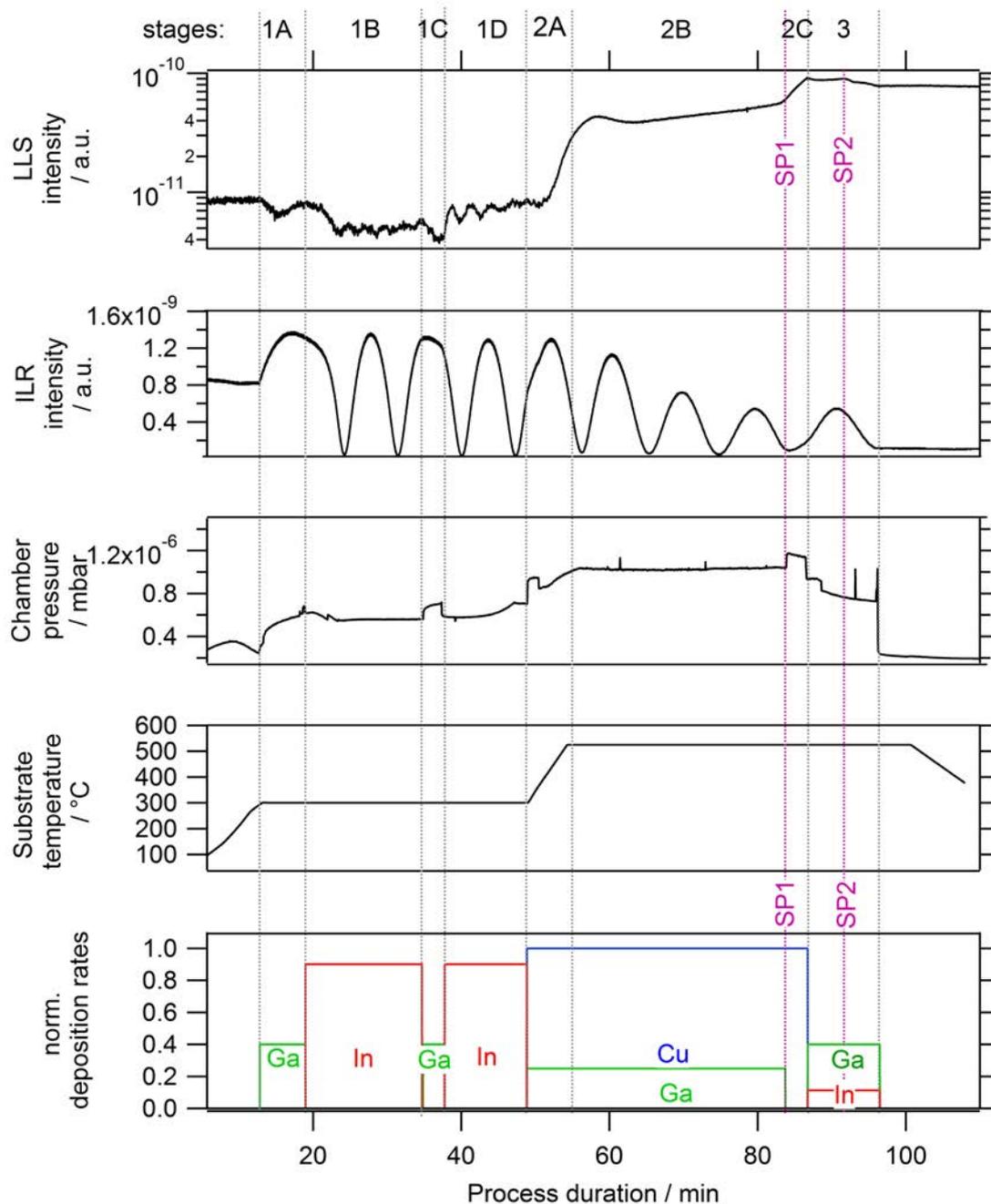


Figure 2.2: Modified 3-stage process for a superstrate-type CIGSe deposition. The deposition rates are chosen to lead to an inverted Ga profile compared to the standard 3-stage process. The Se evaporation rate was constant throughout the process at 15 \AA/s , which corresponds to a Se/In rate ratio of around 3. The LLS and ILR signals are used to control the deposition process. The increase of the LLS signal in stage 2 indicates the first point of stoichiometry, SP1, and the decrease the second point SP2.

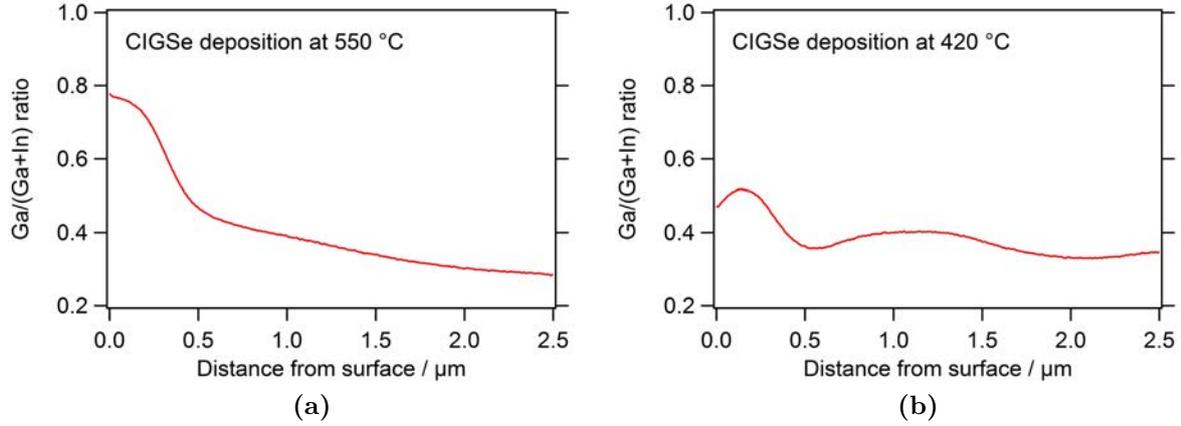


Figure 2.3: GDOES depth profile of Ga/(Ga+In) ratio resulting from the modified 3-stage process at **a)** 550 °C and **b)** 420 °C substrate temperature. The Ga/(Ga+In) gradient is determined by the Ga rates and the deposition temperature. During deposition of the 420 °C layer, the Ga rate was set too low in the 3rd stage, leading to a weak Ga gradient close to the surface.

perature leads to an equalization of the Ga/(Ga+In) ratio of the pre-deposited stack from the 1st stage. The evaporated Cu diffuses into this stack leading to the formation of $\text{Cu}(\text{In,Ga})_5\text{Se}_8$ phase, followed by the $\text{Cu}(\text{In,Ga})_3\text{Se}_5$ phase and then the $\text{Cu}(\text{In,Ga})\text{Se}_2$ phase in stage 2B and 2C. The Ga/(Ga+In) ratio of the growing CIGSe layer increases with time due to the co-evaporation of Ga (GDOES depth profile shown in Fig. 2.3). Once the stoichiometry point is reached a CuSe_x phase starts to form on the CIGSe surface. CuSe_x has a higher refractive index compared to CIGSe and leads to an increase of the LLS signal once it segregates on the CIGSe surface. This is used for the detection and defines the end of stage 2B. In stage 2C only Cu-Se is evaporated until the CIGSe/ CuSe_x stack reaches a Cu/(Ga+In) ratio of around 1.1.

- 3rd stage: Co-evaporation of Ga-In-Se, with a Ga/In rate ratio of 4. The temperature is kept constant at the temperature of the 2nd stage. The CuSe_x phase is transformed to CIGSe and the second point of stoichiometry is marked by a decrease of the LLS signal. The Ga-In-Se evaporation is continued until a Cu/(Ga+In) of 0.85 is achieved.

At the end of the 3rd stage, the Se evaporation rate is reduced from 15 \AA/s to 1 \AA/s and the substrate is kept at the deposition temperature for 5 minutes, before the substrate is cooled down with 20 K/min . At a substrate temperature of 250 °C the Se source is fully closed.

NaF Post-Deposition Treatment (NaF PDT)

The sodium supply for the CIGSe layers were controlled by the deposition of the compound material NaF onto the finished CIGSe layer. This was done by thermal evaporation

within the same PVD chamber used for the CIGSe deposition. However, in between both depositions, the samples were brought in contact with ambient air for several seconds. If not stated differently, the NaF PDT was performed as following: 10 nm of NaF were deposited at a rate of 3 Å/s at substrate temperature of 300 °C. The substrate temperature was then hold for 10 minutes prior cooling down to room temperature within the vacuum chamber. The term "low-rate NaF PDT" refers in this thesis to the deposition process during which NaF is deposited constantly for 10 minutes at a reduced deposition rate of 10 Å/min. This is supposed to lead to a different diffusion profile within the CIGSe layer (see Sec. 1.2.2). Generally the NaF PDT was not followed by any washing steps.

Ga profile

The resulting Ga profile from the above described deposition process at 525 °C and without sodium supply is shown in Fig. 2.3a. The CIGSe bulk is characterised by a shallow Ga gradient which supports the electron collection. The bulk gradient is mainly determined by the Ga rates in stage 1 and 2. The CIGSe close to the surface is characterised by a steep Ga gradient, mainly determined by the Ga rate in stage 3. Since the surface layer forms the back contact, the Ga gradient helps to reduce the back contact recombination losses by reducing the electron density at the back contact.

The profile strongly depends on the deposition temperature. For temperatures below 500 °C, the layered structure from the 1st stage becomes visible in the Ga profile, as seen in Fig. 2.3b. This has the benefit, that the Ga content at the hetero-junction is increased compared to the CIGSe bulk. The disadvantage is the notch in the Ga profile at 0.5 µm film depth. It appears, that during the Cu-rich phase preferably In diffuses to the surface and reacts with the CuSe_x phase, leading to the observed notch.

2.2 TCO growth

The ZnO layers used during this work were deposited by dynamical radio frequency (RF) magnetron sputtering, while most of the new buffer layers were deposited with combinatorial pulsed laser deposition (PLD). Here, both deposition techniques are shortly introduced.

Sputter deposition

Sputtering is a physical vapour deposition in which the target material ejects atoms due to bombardment with accelerated Ar ions [77]. The Ar ions are confined within a magnetic and electric field of a magnetron close to the target. To avoid charging of the target, as often observed in insulating targets, an alternating electric field at the radio frequency can be used. In dynamic sputtering the substrate moves back and forth below the fixed target. The ejected target atoms condensate on the substrate and form a thin film. On the way to the substrate, the atoms undergo scattering with Ar gas (which is above 1e-3 mbar) and with background impurities (below 1-6e mbar). The total pressure

Table 2.1: Process parameter of the ZnO:Al and i-ZnO sputter deposition.

Parameter	ZnO:Al	i-ZnO
Sputter system	VISS 300 S	VISS 300 S
Target dopant concentration	1 wt% Al ₂ O ₃	-
Base pressure	< 4e-7 mbar	< 4e-7 mbar
Ar pressure	1.5 μ bar	8 μ bar
Ar/O ₂ gas flow	0	1
Sputter power (target size 0.075 m ²)	2.5 kW	1.5 kW
Substrate temperature	180°C	without heating
Substrate velocity	0.25 m/min	1.1 m/min
Runs (dynamic mode)	18	28

and the sputtering power control the energy of the particles reaching the substrate and both have a strong influence on the film growth. Further, the film growth depends on the substrate temperature. The process parameters used for the ZnO layers used in this work, if not mentioned otherwise, are shown in Tab.2.1. Prior to the ZnO deposition, the glass substrates were cleaned and optionally a 185 nm thick SiO_x diffusion barrier to avoid sodium diffusion was sputtered onto the glass.

Combi-PLD deposition

Combinatorial pulsed laser deposition (PLD) was used to fabricate TCO layers with compositional gradients from a wide range of different materials. PLD uses laser ablation [78] to create a plasma from a defined solid state target. This has the advantage, that the chamber does not heat up during deposition and cross contamination from previous depositions is less severe than in other deposition methods. A schematic drawing of the PLD system is shown in Fig.2.4. Material from up to six different targets can be deposited onto a single substrate. Whereby the deposition of the different materials is done sequentially, by switching the targets while the position of the laser beam is fixed. No simultaneous depositions are possible. The target position is off-center to the substrate center, leading to thickness gradient on the static substrate. Turning the substrate in between the deposition steps, allows to create a material concentration gradient. The laser ablating is induced by a pulsed KrF laser (248 nm), with an energy density of 300 mJ, a repetition rate of 10 Hz and a distance of 10 cm between the material source and the sample substrate.

One deposition step consists of maximum 50 laser pulses, which ablate material from one target, like Ga₂O₃, while the substrate is kept at a fixed position. For 50 pulses, the deposited material thickness varies from around 1 nm to 0.25 nm, depending on the position on the 5 cm x 5 cm large substrate. In the next deposition step material from a different target can be deposited onto a different position on the substrate. The sequentially deposited layers are supposed to inter-diffuse vertically, while horizontally, almost any arbitrary material gradient can be achieved. The procedure is repeated until the

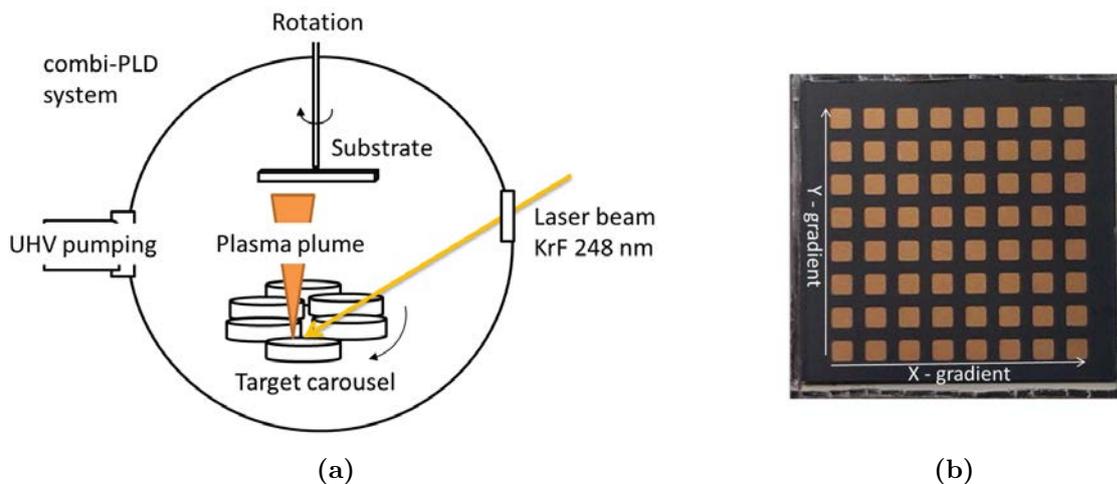


Figure 2.4: **a)** Schematic drawing of the Pulsed Laser Deposition (PLD) system. The target carousel can switch between six targets. The laser ablated material hits the sample off-center, leading to a film thickness gradient. Turning the sample when switching the target creates material gradient. **b)** A 5x5 cm glass/GZO/InGaO_x/CIGSe/Au sample with a X-gradient (thickness) and a Y-gradient (Ga content). The Au pixels define the active area of the solar cell, leading 64 solar cells each with a slightly different buffer layers.

desired film thickness is reached.

2.3 Metallization and device layout

After the TCO and the CIGSe deposition, the back contacts were deposited onto the CIGSe. As a standard back contact material Au is used. Au was thermally evaporated within an electron beam evaporator. A strong electric field combined with a magnetic field is used to accelerate and steer the electron beam, which is ejected from a tungsten filament by thermionic emission, onto the Au target, which heats up and evaporates. The Au vapour condensates onto the substrate leading to the formation of a thin Au film. A shadow mask in front of the substrate was used to create defined back contacts in different sizes, as shown in Fig. 2.5. The pressure during the evaporation was typically 2e-6 mbar. The distance between the Au target and the rotating substrate was 20 cm, leading to a slight heating of the substrate to approximately 60°C during the process duration of around 8 minutes. The layer thickness was 100 nm.

The metallization of the PLD samples was performed with a different shadow mask to allow the analysis of the graded materials. 64 Au pixels, each 3x3 mm in size, were deposited onto a 50x50 mm substrate, as shown in Fig. 2.4b.

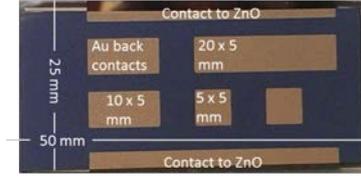


Figure 2.5: Layout of the Au back contacts on a 50 x 25 mm large substrate. Generally five solar cells were defined by the Au back contacts with three different sizes. The substrate edges were free of CIGSe and the two Au bars were in direct contact to ZnO.

2.4 Device Characterization

To understand the electronic processes which determine the performance of the solar cell, it is necessary to study the recombination and the charging processes occurring at different applied voltages. This can be done by measuring $J - V$ and $C - V$ curves and describing them analytically or numerically based on physical models. Further clarification regarding the recombination losses can be gained from the quantum efficiency measurement (QE), which measures the photo-current wavelength dependent, and from the electron beam induced current (EBIC) measurement, which locally resolves the current generation. In this section these four techniques will be introduced.

2.4.1 $J - V$ measurements

The $J - V$ curve displays the current density J versus the applied voltage V of a device under test in the dark or under illumination. For a standard rectifying p/n -junction, fabricated from homogeneous semi-conductors, the characteristics of the $J - V$ curve can be described by the one-diode model following the equation [11]:

$$J = J_0 \left(\exp \left(\frac{q(V - JR_s(V))}{lkT} \right) - 1 \right) + \frac{V - JR_s(V)}{R_p} - J_{photo}\eta_J(V), \quad (2.1)$$

with the following parameters:

1. The voltage dependent series resistance $R_s(V)$, describing the ohmic losses but also barriers for current extraction. Can be therefore different in the dark and under illumination. Shown in Fig. 2.6.
2. The parallel resistance R_p , describing the parasitic current pathways. Has to be measured in the dark. Shown in Fig. 2.6.
3. The ideality factor l , describes the pathway of the recombination current. $l = 1$ for recombination at the interface or outside the space charge region. $l = 2$ for recombination in the space charge region.
4. The reverse saturation current J_0 , describing the recombination losses.

5. The photo-current $J_{photo}\eta_J(V)$, where J_{photo} describes the maximum extractable photo-current and $\eta_J(V)$ describes the voltage dependent efficiency for the extraction of photo generated electron-hole pairs [9].

This equation can be solved analytically if the photo-current is not voltage dependent. However, this is not the case for the solar cells studied in this work. This leads to ideality factors above 2, which has no physical meaning within the simple diode model. Therefore, the $J - V$ curves shown in this work, will be analysed numerically as described in Sec. 3. Still, it will be referred to the standard characteristics of a $J - V$ curve of a solar cell, like fill factor FF, open circuit voltage V_{OC} , short circuit current J_{SC} and finally the power conversion efficiency η (PCE). These values are defined in Fig. 2.6. Further, analytical expressions are useful to express qualitatively evaluable trends. A good example is the open circuit voltage, which, under negligence of the shunt conductance, can be described by [9]:

$$V_{OC} = \frac{kT}{q} \ln \left(\frac{(N_{A,CIGSe} + \Delta n)\Delta n}{n_i^2} \right), \quad (2.2)$$

where $N_{A,CIGSe}$ is the p -type doping concentration of CIGSe, Δn is the excess charge carrier density due to the illumination, n_i is the intrinsic charge carrier density. This expression shows, that the V_{OC} depends on the doping concentration and the excess electron density within the CIGSe, which is defined by the illumination intensity and the electron lifetime. The value for the band gap defines the intrinsic charge carrier density. V_{OC} can also be expressed in the following way [9]:

$$V_{OC} = \frac{E_g}{q} - \frac{kT}{q} \ln \left(\frac{J_{photo}\eta_J(V_{OC})}{j_0 \exp(-E_a/lkT)} \right), \quad (2.3)$$

The V_{OC} loss relative to E_g/q is mainly determined by the activation energy E_a for recombination. E_a can be lowered by defect states within the band gap or by a conduction band cliff at the interface (see Sec. 3.1).

Experimental conditions: The $J - V$ curves presented within this thesis were measured at 25 °C, controlled by water cooling, with a Keithley 238 source measure unit. The optional illumination from a halogen lamp was set to a light intensity of 100 mW/cm² and the spectrum was modified to fit the AM1.5G spectrum. The solar simulator class was B. The intensity calibration was performed with a calibrated Si solar cell. The uncertainty of the absolute light intensity is estimated to be ±5%. Additionally the uncertainty of the active area is around ±5%, leading to a total error of ±7%. The voltage sweep was performed from positive to negative voltages at a speed of 250 mV/s. No light-soaking prior to the measurements was performed.

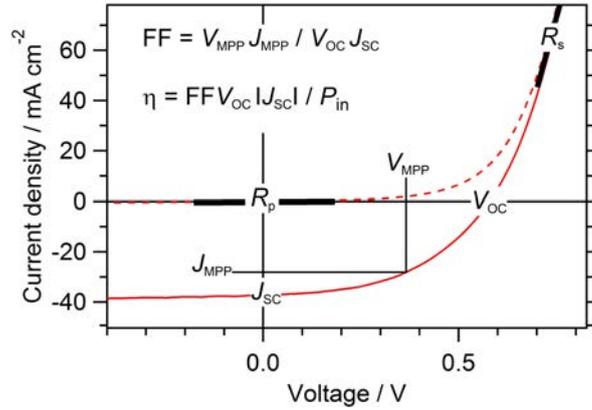


Figure 2.6: Dark (dashed line) and illuminated $J - V$ curve of a CIGSe superstrate solar cell. The resistances R_p and R_s are measured on the dark $J - V$ curve around the voltage range marked with the thick lines. The V_{OC} , the J_{SC} , the J_{MPP} and the V_{MPP} are taken from the illuminated $J - V$ curve. The fill factor FF and the power conversion efficiency η are calculated as shown in the graph.

2.4.2 $C - V$ measurements

The capacitance is a measure for the charge stored within the device, studying the voltage and frequency dependence of the capacitance can therefore give information about the spatial and energetic distribution of localized charges such as defect levels within a semiconductor. The capacitance can be derived from the phase shift of an applied alternative voltage bias and the current induced by it. The current response is determined by the complex conductivity of the device, which is called the admittance Y [79].

$$Y(\omega) = G(\omega) + i\omega C(\omega), \quad (2.4)$$

with $G(\omega)$ being the conductivity and $C(\omega)$ the capacitance, both in principle dependent on the frequency ω of the applied voltage. If no charging or discharging occurs, the admittance equals the conductivity and the phase shift becomes zero. If only charging and discharging occurs, the admittance equals the capacitance and the phase shift becomes 90° . By measuring the amplitude and phase shift of the current it is possible to calculate the capacitance, which is defined as following:

$$C(\omega) = A \frac{dQ}{dV}, \quad (2.5)$$

where dQ is the additional charge stored in the device by a small change of the voltage dV . A is the area of the device.

Space charge capacitance

When applying a small AC voltage (20 mV) oscillating around 0V to a perfect p/n -junction, the conductivity $G(\omega)$ is zero due to the absence of shunts and the capacitance

originates from charging and discharging shallow defect states with free charge carriers at the edges of the space charge region. The capacitance can be then described similar to a parallel plate capacitor with an inserted dielectric [79].

$$C = \frac{\epsilon\epsilon_0 A}{d_{\text{SCR}}}, \quad (2.6)$$

where ϵ_0 is the vacuum permittivity, ϵ the dielectric constant of the charge depleted semi-conductor and d_{SCR} the width of the space charge region. This formula only holds for homo-junctions or for $n+/p-$ or $n/p+$ -hetero-junctions, where the space charge region width within one side of the junction can be neglected. The space charge width for such a junction can be described by the following equation [79]:

$$d_{\text{SCR}} = \sqrt{\frac{2\epsilon\epsilon_0(V_{\text{bi}} - V)}{eN_{\text{CV}}}}, \quad (2.7)$$

where e is the elementary charge, V_{bi} the built-in voltage (defined by the difference of the Fermi levels in the p and n material), V the applied DC voltage and N_{CV} the shallow defect density at the edge of the space charge region. For homogeneously doped semi-conductors it is possible to derive N_{CV} by combining Eq. 2.5 and Eq. 2.6. For non-homogeneous semi-conductors like CIGSe the doping profile has to be measured, which is shown in the next Section.

Profiling

In non-homogeneously doped semi-conductors, the change of the space charge region dd_{SCR} due to a small voltage bias dV depends on the local doping density $N_{\text{CV}}(x)$ at the edge of the space charge region d_{SCR} . With the assumption that only shallow defects contribute to the capacitance, an equation for dd_{SCR} can be derived by extending Eq. 2.7 with $dd_{\text{SCR}}/d_{\text{SCR}}$ and integrating over d_{SCR} [80]:

$$dd_{\text{SCR}} = \frac{\epsilon\epsilon_0 dV}{ed_{\text{SCR}}N_{\text{CV}}(d_{\text{SCR}})}. \quad (2.8)$$

A change in dd_{SCR} leads to a change of the capacitance as defined in Eq. 2.5:

$$\frac{dC}{dV} = -\frac{A\epsilon\epsilon_0}{d_{\text{SCR}}^2} \frac{dd_{\text{SCR}}}{dV}. \quad (2.9)$$

Inserting Eq. 2.8 into Eq. 2.9 leads to the equation for the position dependent shallow defect density $N_{\text{CV}}(x)$:

$$N_{\text{CV}}(d_{\text{SCR}}) = \frac{-C^3}{e\epsilon\epsilon_0 A^2 dC/dV}. \quad (2.10)$$

By choosing small changes of the applied voltage dV , in a way that dC is linear to dV , the expression dC/dV can be exchanged with $\Delta C/\Delta V$, which is more practical in application.

It has to be kept in mind, that these equations are only valid for semi-conductors without deep defects, which is not necessarily the case for CIGSe. In the next section the influence of deep defects will be discussed.

Deep defect capacitance

The capacitance C_d of a homogeneously distributed deep defect whose charging and discharging is fast enough to follow the change of the applied voltage is described by the following equation [81]:

$$C_d = \frac{e^2}{kT} N_d f(E_d)(1 - f(E_d)), \quad (2.11)$$

where N_d is the defect density, $f(E_d)$ the Fermi function at the energy level of the defect, k the Boltzmann constant and T the temperature. Thus, the capacitance is highest, when $f(E_d)=0.5$, which is the case when the Fermi level crosses the defect level. Thus the position of the defect charging and discharging process does not occur at the edge of the space charge region, but somewhere within the space charge region. Eq. 2.10 is no longer valid, because of two effects. First, the deep defects increase the capacitance compared to the capacitance defined in Eq. 2.5. Secondly, they reduce d_{SCR} if they are charged, i.e. if $f(E_d) > 0$. It is, however, possible to freeze out the influence of deep defects to the capacitance, since the average charging and discharging time depends on the temperature and on how deep the defect lies within the band gap. The cut-off frequency ω_0 defines the transition when the defect charging cannot follow the change of the applied AC voltage any more. It is given for a defect, which interacts with the valence band by [81]:

$$\omega_0 = 2c_p N_V e^{E_a/kT}, \quad (2.12)$$

with c_p being the capture coefficient, N_V the density of states of the valence band and E_a the activation energy, which is the difference of the defect level and the valence band. Thus for high activation energies or for low temperatures, defect charging can eventually not follow the change of the applied voltage and does not contribute any more to the capacitance. The study of the frequency dependence of the defect capacitance is called admittance spectroscopy.

Influence of series resistance

The influence of the solar cell series resistance R_s and parallel resistance $1/G$ on the measured capacitance C_m has to be kept in mind. The real space charge capacitance differs from the measured capacitance as follows [82]:

$$C_m = \frac{C}{(1 + R_s G)^2 + \omega^2 C^2 R_s^2}. \quad (2.13)$$

For high R_s or high $G = 1/R_p$ values the measured capacitance is lower than the real capacitance. Therefore these two conditions $R_s \ll R_p$ and $R_s \ll 1/\omega^2 C^2$ should always be met. For $R_p=1000 \Omega$, $R_s=1 \Omega$, $C=500 \text{ nF}$, which are common values for the solar cells studied in this thesis, the measured capacitance is $C_m=0.1 C$ at $f=1 \text{ MHz}$ and $C_m=0.99 C$ at $f=1 \text{ kHz}$. Therefore, all measurements shown in this work were done at $f=1 \text{ kHz}$.

Experimental conditions: The $C - V$ curves presented within this thesis were measured at room temperature, with an Agilent 4284A precision LCR meter. The solar cells were contacted with metal probes, whose influence was corrected for prior to each measurement. The devices were relaxed in the dark for 5 minutes before each measurement.

2.4.3 External Quantum Efficiency (EQE)

The external quantum efficiency (EQE) is a measure for the efficiency of the conversion of incoming photons to extracted charge carriers in a solar cell. Thus, from the EQE it is possible to calculate the short circuit current by a convolution of the EQE with the solar spectrum. However, the short circuit current of the solar cells studied in this work exhibit a "pathologic" dependence on the incoming light intensity and therefore leads to different values for the short circuit current in EQE and $J - V$. The more interesting application of the EQE measurement in this case is the possibility to approximate the collection length for the minority carriers, L_n , from the EQE spectrum [83]. The following equation describes the external quantum efficiency [8]:

$$Q_{\text{ext}}(\lambda) = \frac{hc j_{\text{photo}}(\lambda)}{e\lambda E(\lambda)}, \quad (2.14)$$

where hc/λ describes the energy of the photon with the wavelength λ , e the elementary electric charge, $j_{\text{photo}}(\lambda)$ the photo-current at the photon wavelength λ and $E(\lambda)$ the energy of the incoming photons at the wavelengths λ . The photo-current can be described by $j_{\text{photo}}(\lambda) = (qL_n G_0)/(1 + \alpha L_n)$ [84], with G_0 being the generation rate at the surface and α the absorption coefficient. From this it follows:

$$Q_{\text{ext}}(\lambda) = \frac{hc}{e\lambda} \frac{1}{E(\lambda)} \frac{qL_n G_0(\lambda)}{1 + \alpha(\lambda)L_n}. \quad (2.15)$$

By lumping together all constants in the equation, the equation becomes:

$$\frac{\lambda}{Q_{\text{ext}}(\lambda)} = (\alpha(\lambda)^{-1} + L_n) \cdot \text{const.}, \quad (2.16)$$

from which the collection length can be graphically obtained by plotting λ/Q_{ext} over α^{-1} . Interpolation of λ/Q_{ext} to zero gives L_n .

Experimental conditions: The EQE spectra were recorded at room temperature. The light was provided by a halogen lamp whose wavelength band width was narrowed by a Czerny–Turner monochromator to 10 nm. The short circuit current was amplified by a Stanford Research 560 amplifier and recorded with the lock-in technique (SR830). A calibrated Si and GaAs solar cell was measured prior to the device under test to quantify the external quantum efficiency.

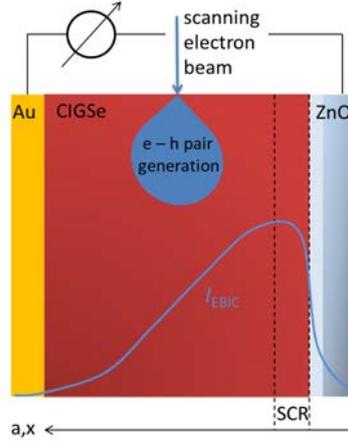


Figure 2.7: Schematic of an EBIC experiment on a cross section of a CIGSe superstrate solar cell. The resulting current profile is shown schematically as well. The collection efficiency within the space charge region, which is marked with dashed lines, is set to unity.

2.4.4 Electron-Beam-Induced Current (EBIC)

Another technique to study the electron-hole pair extraction within a solar cell is the Electron-Beam-Induced Current (EBIC) measurement. The basic principle of this technique is shown in Fig. 2.7. The electron beam generated from a scanning electron microscope, is used to create electron hole pairs within the solar cell. The electron beam is then scanned along the cross section of the solar cell, which is at short circuit condition, while the generated current is recorded and plotted over the lateral location a of the electron beam. From this a photo-current profile I_{EBIC} , as shown in Fig. 2.7, is obtained which can be further analysed. The obtained current profile is a convolution of the charge carrier collection function $f_c(x)$ of the solar cell and the lateral generation function $g(x)$ of the electron beam [85]:

$$I_{\text{EBIC}}(a) = \int_0^{\infty} g(x, a) f_c(x) dx. \quad (2.17)$$

The generation function g is described in [86] as follows:

$$g(x) = \frac{A}{R_G} \beta(|a - x|), \quad (2.18)$$

where $A = (E_b I_b (1 - \Lambda)) / (e E_{eh})$ stands for the generation rate, depending on the electron beam energy E_b , the beam current I_b , the electron-hole pair generation E_{eh} and the back scatter coefficient Λ . $R_G(\rho, E_b)$ stands for the Gruen penetration depth depending on the material density ρ and E_b . The collection function f_c can be obtained by solving the differential equation $f_c(x) = L_n^2 \Delta f_c(x)$, with the boundary conditions $f_c(x_{\text{SCR}}) = 1$ and

$f_c(x_C) = \exp(-(S_C/D_e)x)$ [87], which leads to:

$$f_c(x)dx = \frac{\frac{1}{L_n} \cosh\left(\frac{x-x_c}{L_n}\right) - \frac{S_c}{D_e} \sinh\left(\frac{x-x_c}{L_n}\right)}{\frac{S_c}{D_e} \sinh\left(\frac{x_c-x_{\text{SCR}}}{L_n}\right) + \frac{1}{L_n} \cosh\left(\frac{x_c-x_{\text{SCR}}}{L_n}\right)}, \quad (2.19)$$

where x_{SCR} is the position of the space charge region edge within the CIGSe, x_c the position of the CIGSe-Au back contact, S_c the back contact recombination velocity of electrons, and L_n the electron diffusion length.

Experimental conditions: The EBIC signal was recorded within a Gemini LEO 1530 Scanning Electron Microscope. To access the cross-section of the device, the device under test was broken at a predefined place of fracture, immediately before the measurement. No polishing of the cross-section was performed. The contact wires were fixed onto the sample with silver paint. The current was amplified by an SR560. At an extractor voltage at 10 kV and an extractor current of 260 μm , a probe current of 63 pA was measured at no high current mode. The detected current was amplified and returned to the image processing unit of the SEM.

Care has to be taken not to reach the high in-injection level, which occurs when the density of injected electrons exceeds the doping density of CIGSe, as this leads to a charge accumulation and a distortion of the built-in potential and subsequent of the EBIC profile [88].

2.5 Material Characterization

Material characterization allows the correlation of the electrical properties with the structural and chemical properties of a sample. This can be used to determine the origin of device limitations and to optimize the fabrication routine accordingly. In this section the following techniques will be introduced: X-ray Photoelectron Spectroscopy (XPS), X-ray Diffraction (XRD) and Glow Discharge-Optical Emission Spectroscopy (GDOES).

2.5.1 X-ray Photoelectron Spectroscopy (XPS)

The chemical reaction between the TCO and the CIGSe layer is studied by cleaving the sample at the respective interface with subsequent XPS surface analysis of both sides. XPS can provide information about the elemental composition at the surfaces and Auger analysis can additionally reveal the chemical state of the detected atoms at the interface. This section will give a brief overview of the XPS technique and the sample preparation. Further in depth information can be found in [89].

Basic principle

The electron binding energy, E_B , in core levels depend on the specific element, the electron orbital and the chemical environment of the probed atom. Therefore, it is possible to

identify the type and the state of an atom by measuring the binding energy of these electrons. To do this the core electrons are excited by X-ray photons of a known energy $h\nu$, which is sufficient to eject the electrons from the atom. Excess energy provides kinetic energy for the electron, E_{kin} , which can be measured with an electron detector. Using the following equation one can infer E_B from E_{kin} [90]:

$$E_{\text{kin}} = E_{h\nu} - E_B - \Phi_{\text{spec}}, \quad (2.20)$$

with Φ_{spec} being the work function of the spectrometer. A sketch of this process is shown in Fig. 2.8a. An example of a XPS spectrum is shown in Fig. 2.8d, where the detected electron intensity is plotted over their binding energy. Peaks correspond either to core levels of a specific element or from Auger processes (sketched in Fig. 2.8c). The energy of the Auger electrons depend on the energy difference between the core hole and the energy level of the electron that fills this core hole. Note that this Auger process has a much higher cross section than the radiative process, shown in Fig. 2.8b. However, the ejected electrons, both photo-excited or Auger, experience strong scattering within the probed material. This limits the information depth to a few nano meters, depending on the kinetic energy of the electrons.

The radiative recombination process shown in Fig. 2.8b is exploited in techniques like X-ray fluorescence spectroscopy (XRF) to identify elements in the material bulk. XRF is used in this thesis to calibrate the GDOES measurements (see Sec. 2.5.3)

Quantification

Each isolated peak in the XPS spectrum shown in Fig. 2.8d corresponds to one type of atom. The intensity, which is the integral of the peak, is proportional to the amount of atoms present within the sample, thus it is possible to quantitatively analyse the XPS measurement. However, the error of such a quantification can become quite large due to the fact that other factors have influence on the peak intensity. In general the peak intensity I_{AX} of an electron ejected from an energy level X within an Atom A can be described as follows:

$$I_{\text{AX}} = \sigma_{\text{AX}}(h\nu, Z, X) \cdot D(E_{\text{AX}}) \cdot L_{\text{AX}}(\gamma) \cdot J_0 \cdot C_A \cdot \lambda_{\text{M}}(E_{\text{AX}}) \cos\theta \cdot T(x, y, \gamma, \theta, E_{\text{AX}}), \quad (2.21)$$

where $\sigma_{\text{AX}}(h\nu, Z, X)$ is the cross section for the photo-ionization process, which depends on the photon energy $h\nu$, the element Z and the electron orbital X. $D(E_{\text{AX}})$ is the detection efficiency of the detector, which depends on the electron energy. $L_{\text{AX}}(\gamma)$ is the asymmetry factor of the electron emission, which depends on the angle of the excitation to the electron orbital X. J_0 is the intensity of the X-ray source and C_A is the density of the atom A in the sample. $\lambda_{\text{M}}(E_{\text{AX}}) \cos\theta$ is the average free path length of the electron, which depends on the electron energy and the excitation angle θ . $T(x, y, \gamma, \theta, E_{\text{AX}})$ is the transmission function, which mainly depends on the kinetic energy of the free electron. All these values can be measured or calculated, which allows the determination of C_A from the intensity

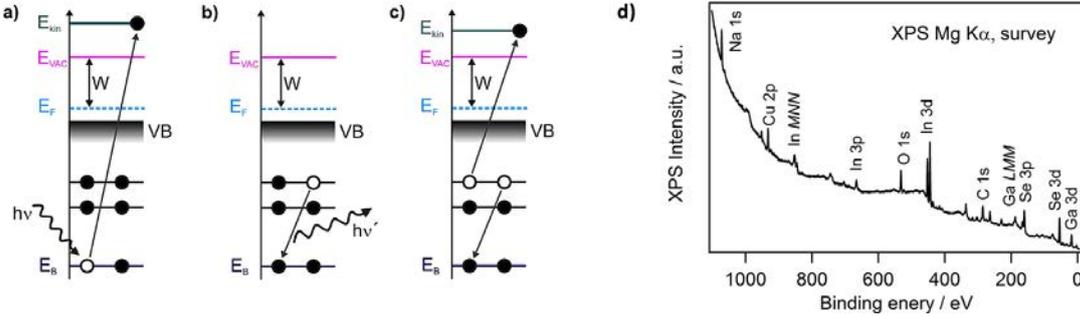


Figure 2.8: Schematic representation of the processes occurring during a) photo-ionisation b) recombination and emission of a photon and c) recombination and emission of an Auger electron [92]. d) XPS survey scan taken from a CIGSe absorber.

I_{AX} . However, all the correction factors in Eq. 2.20 come along with an uncertainty. First, the sample itself is the origin of the uncertainty, that is due to inhomogeneities of the atom density, both in depth and along the surface. Further, uncontrolled contamination from air on the sample surface can be expected. Second, the properties of the measurement setup is not always perfectly known. And thirdly, the calculation for the asymmetry factor, the photo-ionization cross section and the free path length are subject to errors. This leads to a minimum error of 52 % [91]. The error can be further minimized if peaks of similar kinetic energy are compared, since most of the correction factors mainly depend on the kinetic energy. In this work an average error of 60 % is assumed for all quantitative XPS values.

Sample preparation and experimental conditions

To enable the XPS analysis of the TCO/CIGSe interface in superstrate solar cells, it is necessary to cleave the sample at this interface. It was found that this can be achieved by thermal shock. To do this, a few mm thick aluminium plate is glued with silver epoxy onto the CIGSe surface. Care has to be taken, that the epoxy does not spread to the sample edges, since this will hinder the cleaving. After drying the epoxy, the resulting glass/TCO/CIGSe/Ag/Al stack is inserted into a beaker filled with liquid nitrogen. Due to the rapid cool down and the different thermal expansion coefficient of these layers, stress builds up and the sample cleaves at the weakest point, which is the TCO/CIGSe interface. However, this only works if an interfacial oxide layer like GaO_x forms at the interface, otherwise the stack cleaves at the Ag/Al interface.

The beaker, still filled with liquid nitrogen, is then loaded into a glove box and only inside a nitrogen filled glove box, the cleaved sample is removed from the liquid nitrogen. It is assumed, that despite the nitrogen atmosphere, a 1 nm thick C_2H_4 layer accumulated on the sample surface. Both sides are then fixed with graphite tape onto the XPS sample holder and loaded into the XPS system.

The XPS measurements were performed in the CISSY tool, which is a XPS system

connected to a glove box and a sputter deposition chamber. The X-ray tube uses a magnesium and an aluminium anode, which have characteristic emission lines at 1253,6 eV and 1486,6 eV respectively. The angle between the incoming X-rays and the entrance slit of the spectrometer is $54,7^\circ$. More detailed information on the system specification can be found in [93].

The resulting measurement data was analysed by using the multi-peak fitting routine of the analysis software IGOR [94]. First, the background is subtracted with a linear function, then the peaks are fitted with Voigt functions. For quantitative analysis the results were corrected according to the ionization cross section and mean free path of the electron lines as well as the electron analyzer characteristics (as described by Eq. 2.21) and possible surface contamination (1 nm thick C_2H_4).

Care is to be taken since the relative error of the at.% values is at least 50%. Since we only compare similar samples the error is systematic in character since it mainly originates from uncertainties of the mean free path length of the x-rays, the ionisation cross section and the transmission function. Therefore it is still possible to interpret trends between the samples.

2.5.2 X-ray Diffraction (XRD)

In this work X-ray diffraction (XRD) is used to identify crystalline phases and preferred orientation of poly-crystalline thin films.

The periodicity within a crystal can be measured by the positive interference of X-rays scattered at different, parallel planes of electron densities. The condition for such a positive interference is given by Braggs law [95]:

$$n\lambda = 2d \sin \theta, \quad (2.22)$$

where λ is the X-ray wavelength, θ the Bragg angle, d the distance between the parallel planes and n is called interference order. If λ and θ are known, it is possible to calculate d/n . Commonly θ is varied during the XRD measurement, which allows to scan for different lattice spacings present in the studied crystal. The angle is generally varied by a goniometer, whereby only planes perpendicular to the substrate normal lead to interference peaks. In poly-crystalline films this allows to determine the preferred crystal orientation by comparing the peak intensities within the obtained pattern to a powder pattern. When performing energy dispersive XRD (ED-XRD), the Bragg angle θ is fixed, but the detected wavelengths λ is varied [96]. Commonly polychromatic photons from synchrotron radiation is used as the X-Ray source.

The XRD peak width is limited by the effects from the X-ray source, the detector area, and any deficiency in the focus, but for small crystalline domain sizes it is often limited by the domain size. If this is the case, the domain size can be calculated from β , which is the FWHM value (in radians) of the peak after subtracting the instrumental line broadening,

with the Scherrer formula [97]:

$$D = \frac{0.9 * \lambda}{\beta \cos(\theta)}. \quad (2.23)$$

Experimental conditions: In this work the X-rays were generated at a Cu anode, whose Cu-K_α X-ray radiation has a characteristic wavelength λ of 1.5418 Å. The used Diffractometer was a PANalytical XPert MPD with a PIXcel linear detector, set up in the Bragg-Brentano configuration to record the XRD patterns. The Cu anode was supplied with 40 kV and a current of 30 mA. A description of the experimental ED-XRD details can be found in [98].

2.5.3 Glow Discharge-Optical Emission Spectroscopy (GDOES)

Depth profiles of the elemental composition of CIGSe/TCO thin film stacks are very useful to identify phase transitions at the interface as well as analysing the Ga depth profile within the CIGSe layer. There are several techniques available to study the elemental depth profiles: Energy-Dispersive X-ray spectroscopy in a Transmission or Scanning Electron Microscope (SEM/TEM-EDX), Time-Of-Flight Secondary Ion-Mass Spectrometry (TOF-SIMS), X-ray Photoelectron Spectroscopy (XPS) in combination with sputtering or, as described here, Glow Discharge-Optical Emission Spectroscopy (GDOES). In this work GDOES is used due to its better sensitivity compared to SEM-EDX or XPS and the fact, that it is more convenient in application compared to TOF-SIMS or TEM-EDX.

The basic principle

The principle of GDOES is to sputter material from the sample's surface and to identify the material by their characteristic optical emission, induced by the electronic excitation within the sputtering plasma.

The experimental setup is separated into the optical detector and the glow discharge source for the sputtering process [99]. The idea is to sustain an Ar discharge current between anode and cathode, in which the sample acts as the cathode. The resulting Ar plasma close to the sample sputters material from the sample surface and this material gets ionized and excited within the Ar plasma. The form of the resulting sputter crater determines the depth resolution and has to be carefully optimized for each material by varying the plasma conditions (pressure, voltage and current in pulsed mode). The optical emission of the sputtered material is focused onto a concave grating and the monochromatic light is then detected by a CCD array. The analysed spectral range lies between 110 and 800 nm, sufficient for most elements including light elements as carbon, but not oxygen.

Calibration

To correlate the measured intensities $I_{i,k}$ of the optical emissions to the chemical composition of the film it is necessary to calibrate the measurement. This is shown in detail in [99] and shortly summarized here. The calibration is done by analysing a film with a known chemical composition and thickness, which must be similar to the sample under test. This allows determining a constant emission yield $R_{i,k}$ and the sputtering rate q_j for a certain element i within the sample j at the wavelength k . Both values depend on the plasma conditions, detection setup and material composition of the sample. Therefore the calibration has to be done prior to every measurement. The concentration of the element within the sample is described by:

$$c_i = \frac{I_{i,k}}{q_j R_{i,k}} \quad (2.24)$$

To calculate the depth of the sputter crater it is necessary to know the mass density ρ of the film, which can be approximated by a sum of the pure element densities ρ_i and from this the depth d of the sputter crater is determined:

$$d = \sum_m m \frac{q_j \Delta t}{\rho A} \quad (2.25)$$

, with m being the numbers of optical emission spectra recorded during the glow discharge and A the area of the sputter crater.

Example

An example of a CIGSe depth profile measured with GDOES is shown in Fig. 2.9a. The uncalibrated optical emission signals at certain wavelengths, characteristic to a specific element, are shown in Fig. 2.9a. From Fig. 2.9a it is obvious, that the emission yields vary strongly between the elements, as Na is for example only a trace element, but its optical emission signal is as high as for Cu. For the calibration a reference cell with constant Ga content is used, whose composition and thickness was determined from X-Ray Fluorescence (XRF) analysis. Trace elements like Na and C are not considered during the calibration. Oxygen is not considered as its concentration is negligible and because the signal for oxygen at 130 nm is too noisy and is not shown here. The calibrated results are shown in Fig. 2.9b. The surface appears to be covered by a few nm thick Se layer, which is an artefact due to the unstable sputter conditions during the first seconds of the measurement. After stabilization of the experimental conditions, the Se and the Cu concentration profiles are flat throughout the film. The In and Ga profiles add up to a constant (In+Ga) profile and the Cu/(In+Ga) ratio is 0.9 throughout the film. At the interface to the molybdenum layer the emission signals of the CIGSe elements decrease approximately exponential. The exact form depends on the crater formation and the surface roughness of the CIGSe and the Molybdenum film. In [99] it is mentioned that the sputter rate for Cu is slower compared to that of In and Ga, thus leading to columns

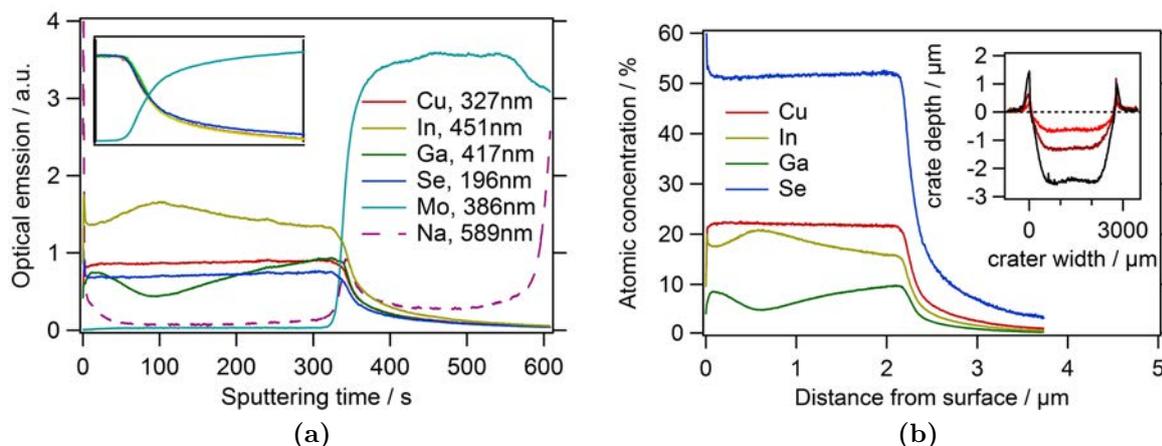


Figure 2.9: **a)** Uncalibrated optical emission profiles of different elements measured at their characteristic wavelength. Inlet: Normalized profiles in order to compare the decay of the different profiles at the interface to Mo. **b)** Atomic percentage profiles of the CIGSE elements and Mo, calibrated with a reference cell. Inlet: Typical sputter crater at different sputter time steps measured with a profilometer.

of pure copper within the sputter crater. To check whether this is the case for the sputter conditions used in this work, the signals of all CIGSe elements are normalized to the copper signal close to the interface. If the sputter rate of Cu would differ from the other elements, the decay of the Cu signal at the interface to Mo should also differ from the decay of the other signals. As seen in the inlet of 2.9a this is not the case. Since all elements decay similar to each other, it can be concluded, that the sputter rates of all elements are similar to each other.

Experimental conditions: The spectrometer used in this work is the GDA 650 from Spectrumba with 2.5-mm anode diameter and argon as a discharge gas (3.5 hPa process pressure, voltage 500 V). Due to the low sample conductivity pulsed RF plasma mode was used with a frequency of 350 Hz and a low duty cycle. The resulting crater is shown in the inlet of Fig. 2.9b.

Chapter 3

Numerical Simulation

CIGSe thin film solar cells are difficult to describe with analytical models due to their non-ideal characteristics caused by charged interface defects, deep bulk defects, non-ohmic back contacts and band discontinuities. Therefore numerical simulations can be the better choice to reproduce or to evaluate the experimental results [100]. These numerical models calculate the charge distribution and the drift/diffusion current based on the Poisson equation and continuity equation for electron and holes. The most known commercial program is Sentaurus TCAD [101], which is able to simulate the electrical performance of three dimensional device structures and is also suitable for testing advanced optical concepts. Other freeware programs like AFORS-HET [102], ASA [103], PC1D [104] and SCAPS [105] exist, which are able to simulate one dimensional structures. In this work SCAPS was used to do the numerical simulations, since it is capable to compute AC signals for the simulation of capacitance spectroscopy [106] and is designed to handle graded semiconductors [107] with large band discontinuities, which is necessary for CIGSe devices. This chapter will give an introduction to the mathematical framework of the numerical simulation programs.

Basic equations

The basic equations used in the numerical simulation are the Poisson equation and the continuity equations. The Poisson equation describes the local electrostatic potential $\Phi(\vec{x}, t)$ within the solar cell and for the one dimensional approximation of a solar cell reads as follows [108]:

$$\frac{\delta^2 \Phi(x, t)}{\delta x^2} = - \frac{q[n(x, t) - p(x, t)]}{\epsilon_0 \epsilon_r}, \quad (3.1)$$

where x stands for the position within the solar cell, t for the time, q for the elementary charge, ϵ for the dielectric constant and $n(x)$, $p(x)$ for the electron and hole densities respectively, including trapped charges within defects. Charged defects change the local electrostatic potential and may improve or hinder the extraction of charge carriers. The

Table 3.1: Baseline parameter used in this work for the numerical simulations, if not stated otherwise. Charge carrier lifetimes and interface recombination velocities varied for most simulations and are not given here. The recombination velocity at the back contact was always set to $1e+7$ cm/s. Data taken from [100].

Symbol	Property	Unit	CIGSe	ZnO
E_g	band gap	eV	1.18	3.3
χ	electron affinity	eV	4.5	4.6
N_C	CB effective density of states	cm^{-3}	$2.2e+18$	$3.7e+18$
N_V	VB effective density of states	cm^{-3}	$1.8e+19$	$1.1e+19$
ν_{thn}	electron thermal velocity	cm/s	$1e+7$	$1e+7$
ν_{thh}	hole thermal velocity	cm/s	$1e+7$	$1e+7$
μ_n	electron mobility	cm^2/Vs	$1e+2$	$1e+2$
μ_h	hole mobility	cm^2/Vs	$2.5e+1$	$2.5e+1$
ϵ_r	relative permittivity (at 1kHz)		13.6	9
R^{rad}	Radiative recombination coefficient	cm^3/s	$1e-10$	$1e-10$
A	absorption coefficient prefactor	$1/(cm\sqrt{eV})$	from file	from file

continuity equations are [108]:

$$\frac{\delta n(x, t)}{\delta t} = U_n(x, t) + \frac{1}{q} \frac{\delta J_n(x, t)}{\delta x}, \quad (3.2)$$

$$\frac{\delta p(x, t)}{\delta t} = U_p(x, t) + \frac{1}{q} \frac{\delta J_p(x, t)}{\delta x}, \quad (3.3)$$

where $J_{n,p}$ is the electron/hole current density and $U_{n,p}$ is the net generation rate of electrons and holes, which is the difference between generation of free carriers and recombination of free carriers. These equations ensure the conservation of energy. The drift and diffusion currents can be calculated from the respective charge carrier densities and potentials as follows [108]:

$$J_n = -qn\mu_n \frac{\delta \phi}{\delta x} + qD_n \frac{\delta n}{\delta x}, \quad (3.4)$$

$$J_p = -qp\mu_p \frac{\delta \phi}{\delta x} + qD_p \frac{\delta p}{\delta x}, \quad (3.5)$$

where $\mu_{n,h}$ stands for the charge carrier mobilities and $D_{n,h}$ for the diffusion constants of electrons and holes. At the boundaries of the device model, i.e. the metal contacts, the potential values and the charge carriers densities are fixed. For a discrete position x within the device, three non linear equations have to be solved, the poisson equation and the two continuity equations. Since the 1 dimensional device structure is discretized into N points, $3N$ equations have to be solved to get a solution for the full device. This is usually done by starting with a first guess of the potential and the charge carrier densities, then the potential is calculated from the poisson equation and corrected, followed by the calculation of the charge carrier density from the continuity equations.

The whole procedure is repeated until convergence is achieved. The current can then be calculated from the final potential and charge carrier distribution within the device.

Recombination in a p -type absorber via a single defect level is described by the Shockley-Read-Hall recombination rate R^{SRH} [109].

$$R^{\text{SRH}} = \frac{(np - p_i^2)}{\tau_p \left(n + N_c \exp\left(\frac{E_T - E_c}{k_B T_L}\right) \right) + \tau_n \left(p + N_v \exp\left(\frac{E_V - E_T}{k_B T_L}\right) \right)}, \quad (3.6)$$

with p_i being the intrinsic hole density, $\tau_{n,p}$ the electron and hole lifetime, N_V and N_C are the effective densities of states of the valence and conduction band, E_T the energy level of the defect, E_C the energy at the conduction band minimum (CBM) and E_V at the valence band maximum (VBM). The exponential terms become large, and with it the recombination rate low, when E_T lies close to E_C or E_V , as this is the case for shallow defects. It can further be shown [110], that for equal τ_n and τ_p , R^{SRH} reaches a maximum once $n = p$ is fulfilled. In a p/n -junction this is fulfilled within the space charge region, with the exact position depending on the doping densities and the voltage bias. Further, low charge carrier lifetimes, τ_n or τ_p , increase the recombination rate. An estimate of the single level electron lifetime τ_n can be calculated by [100]:

$$\tau_n = \frac{1}{\sigma_n \nu_{th,n} N_{\text{def}}}, \quad (3.7)$$

where N_{def} is the defect density and σ_n the effective cross-section of the defect for electrons. The cross-section of ionized donor states is larger for electrons than for holes due to the coulomb attraction. A simple approximation of the cross-section for a Coulomb-attractive defect center is $\sigma_n = q^4 / (16\pi\epsilon_r^2 k_B^2 T^2)$ [111]. For single ionized donor states, it is in the range of $10\text{e-}12$ - $10\text{e-}13$ cm^2 for electrons and for holes $10\text{e-}15$ - $10\text{e-}16$ cm^2 . Further recombination pathways like radiative and Auger recombination are also implemented into SCAPS but both effects only have a negligible effect on the total recombination current in the CIGSe devices studied here.

Interface recombination is handled in a very similar way to bulk recombination, by the Pauwels-Vanhoutte theory [112], which is an extension of the Shockley-Read-Hall theory. The difference is that the interface defect states can interact with the charge carriers from both materials. Eq. 3.6, describing the SRH recombination rate, has to be extended to describe the interaction between the defect state and two conduction band and two valence bands. For example, due to the conduction band offset at the CIGSe/ZnO interface, the interface defect interacts mainly with the holes from the VBM of CIGSe and with the electrons from the CBM of ZnO. Further, the recombination rate becomes a recombination velocity, since the defect density N_{def} in Eq. 3.7 has the unit cm^{-2} at the interface instead of cm^{-3} in the bulk.

Due to the different band gaps and electron affinities of the materials in hetero-junction solar cells, charge carriers may have to overcome energetic barriers at interfaces. The

charge carrier transport over a barrier Φ_B is calculated with the formula for thermionic emission [113]. The equation for the thermionic emission current of electrons, $J_{\text{TE,n}}$, reads:

$$J_{\text{TE,n}} = q\nu_{\text{th}}N_c \exp\left(\frac{\Phi_B}{k_B T_L}\right) \left[\exp\left(\frac{qV}{k_B T_L}\right) - 1 \right], \quad (3.8)$$

where T_L is the lattice temperature and V the applied voltage bias. In addition, band to band tunnelling, intra band tunnelling, tunnelling to interface defects and tunnelling to contacts are all implemented into SCAPS, details can be found in [114].

The baseline parameters used for the SCAPS simulations in this thesis are shown in Tab. 3.1.

3.1 Controlling interface recombination in CIGSe devices

Lattice mismatch and elemental diffusion at a hetero-interface can lead to high interface defect densities in hetero-junction solar cells. This may disqualify certain materials for the application as a buffer layer in CIGSe devices. This section will present the impact of interface recombination in CIGSe solar cells and how it can be reduced by device design.

As shown in Eq. 3.6, the bulk recombination rate at a single defect level depends on the distance of the defect level E_T to the CBM and the VBM. The higher the band gap of the material the smaller the recombination rate at the defect, due to the reduced density of free electrons and holes. The same holds for recombination at defects at the hetero-interface, only that the band gap at the hetero-interface depends on the energetic position of VBM and CBM of both materials. These depend on the electron affinity and the band gap of the materials as described in Eq. 1.1. Thus, the buffer layer should have a lower electron affinity but a higher band gap compared to CIGSe, in order not to reduce the interface band gap. In the special case that i-ZnO is in direct contact to CIGSe, the conduction band offset was shown to be slightly negative, which is called a "cliff" like conduction band offset. The "cliff" like offset lowers the interface band gap and increases the band-to-band recombination as well as the recombination via defect levels at the interface. An example of a cliff like interface with a neutral mid-gap defect level ($\sigma_n = \sigma_h = 1\text{e-}13 \text{ cm}^2$) is given in Fig. 3.1a by the solid lines. In the following the parameters of the buffer layer are varied to analyse the influence on the interface recombination losses. Since the open circuit voltage, V_{OC} (see Sec. 2.3), is the parameter which is most sensitive to recombination losses (as long as no Fermi-level pinning is present) it will be used as a measure for the recombination losses.

The simulated V_{OC} for varying $\Delta E_{\text{C,IF}} = \chi_{\text{CIGSe}} - \chi_{\text{buffer}}$ is shown in Fig. 3.1b. In case, that only band-to-band recombination occurs at the interface the CB offset can become as small as -0.2 eV without experiencing any loss in V_{OC} . For well passivated interfaces, with a interface recombination velocity of $S_{\text{IF}} = 1\text{e}+3 \text{ cm/s}$, already small negative offsets lead

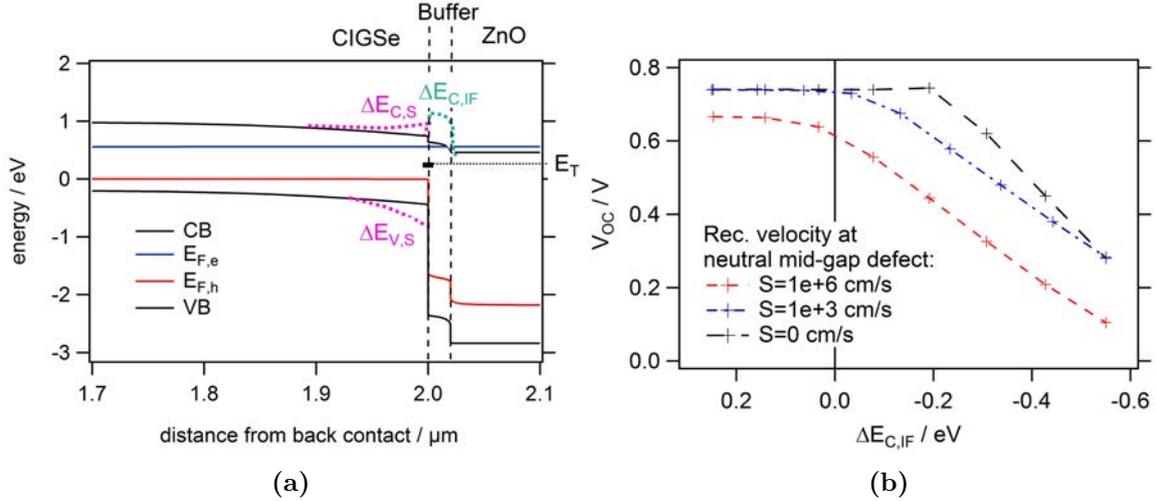


Figure 3.1: **a)** Band diagram of a CIGSe/buffer/ZnO solar cell at V_{OC} condition. $\Delta E_{C,S}$ stands for the CBM gradient of the CIGSe close to the surface/interface, $\Delta E_{V,S}$ for the VBM gradient of the CIGSe close to the surface/interface, $\Delta E_{C,IF}$ for the CBM offset at the CIGSe/buffer interface. **b)** V_{OC} depending on $\Delta E_{C,IF}$. No CBM or VBM gradient set within the CIGSe, $\Delta E_{C,S} = \Delta E_{V,S} = 0$. The doping level of the buffer is set 10x the value of the CIGSe layer.

to a V_{OC} loss. In case of high interface recombination velocities, with $S_{IF} = 1e+6$ cm/s, a positive $\Delta E_{C,IF}$, also called a conduction band "spike", of at least +0.1 eV is required, but the V_{OC} is still reduced compared to the passivated interface.

To further reduce interface recombination losses it is required to increase the band gap of CIGSe close to the hetero-junction. Fig. 3.2a shows the effect of increasing the CBM of the CIGSe at the interface relative to the bulk value, which is called $\Delta E_{C,S}$ in this work. For the specific device model used for these calculations, it is possible to increase the conduction band by up to 300 meV without introducing any loss in the short circuit current J_{SC} or the fill factor FF (not shown), while the V_{OC} steadily increases due to the reduced density of free electrons available for recombination at the interface. Still, the effect is rather limited due to the unchanged density of holes within the CIGSe at the interface. This requires a lowering of the CIGSe VBM.

The influence of lowering the VBM of the CIGSe at the interface compared to the bulk value, $\Delta E_{V,S}$, is also shown in Fig. 3.2a. For a $\Delta E_{V,S}$ of 150 meV present only at the first 10 nm from the interface is already sufficient to suppress most of the interface recombination losses. This can be achieved by anion substitution from selenium to sulphur, or by a reduction of the Cu content on the surface (see Sec. 1.3.1). The width of the modified CIGSe layer should be limited to the width of the space charge region and should not be larger than 200 nm, otherwise it may create a barrier for the electron extraction, since the p -type doping density is not reduced at the same time.

Another issue is the buffer doping density. Hetero-junctions from n -type and p -type materials with similar doping densities, have equal electron and hole densities at the

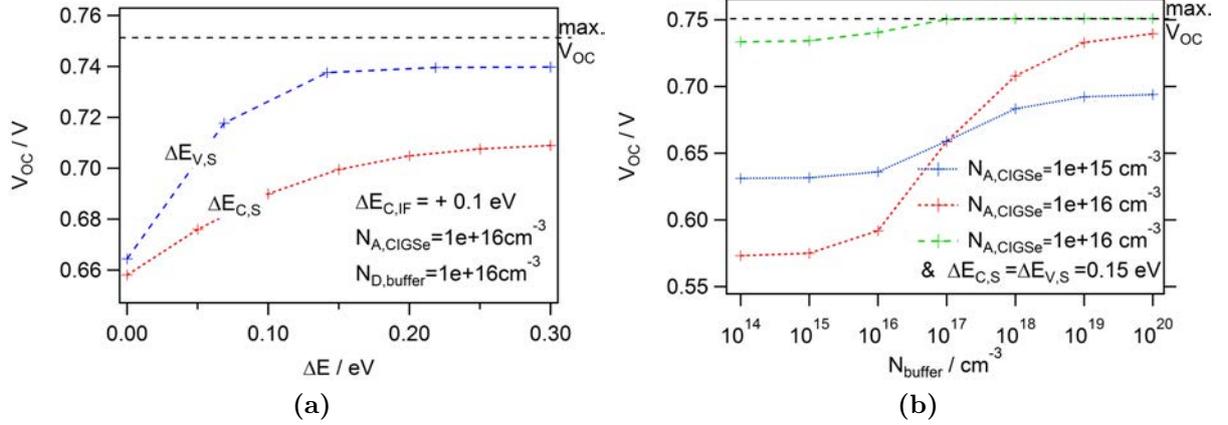


Figure 3.2: a) V_{OC} depending on the energy difference of the CBM and the VBM within the bulk and the interface of the CIGSe (see Fig. 3.1a). The electron affinity of the buffer is set 100 meV smaller than the electron affinity of the CIGSe bulk, $\Delta E_{C,IF} = 100$ meV. S_{IF} was set to $1e+6$ cm/s. b) V_{OC} depending on the doping level of the 50 nm thick buffer layer, with $\Delta E_{C,IF} = 100$ meV. $\Delta E_{C,S} = \Delta E_{V,S} = 0$ was set for the red and the blue profile. $\Delta E_{C,S} = \Delta E_{V,S} = 150$ meV was set for the green profile. Interface recombination velocity was set to $S_{IF} = 1e+6$ cm/s.

interface, which according to Eq. 3.6 results in high recombination losses. To reduce the hole concentration at the interface the type of majority charge carrier has to be inverted in the CIGSe layer close to the hetero-interface, this is called an inverted junction. This can be achieved by a high n -type doping density of the buffer layer. To reduce the interface recombination it is therefore crucial that the doping density of the n -type buffer is larger than the p -type doping of the CIGSe. The simulation results in Fig. 3.2b show how V_{OC} is influenced by the doping density of a 50 nm thick n -type buffer layer in the case of a high interface recombination velocity ($1e+6$ cm/s) and no CIGSe band gap gradient close to the hetero-interface. It shows, that the buffer doping should be at least $1e+18 \text{ cm}^{-3}$.

The most trivial but at the same time most difficult way to reduce the interface recombination losses is to reduce the amount of defect states. But even in the presence of high defect densities the interface recombination losses can be almost completely quenched, if the CIGSe interface band gap is increased by 300 meV and if the buffer doping density is increased to above $1e+17 \text{ cm}^{-3}$. The top profile in Fig. 3.2b shows this.

In summary, by engineering the material properties of the buffer layer and the CIGSe at the hetero-interface it is possible to achieve high efficiencies even in the presence of highly defective hetero-interfaces. This qualifies non-lattice matched materials as buffer layers as long as their electron affinity is smaller compared to the bulk CIGSe and their n -type doping density is higher compared the p -type doping density of CIGSe. However, if the interface defects are acceptor type, they trap electrons and have a strong impact on the band alignment, eventually leading to an electron extraction barrier. This will be shown in the next section.

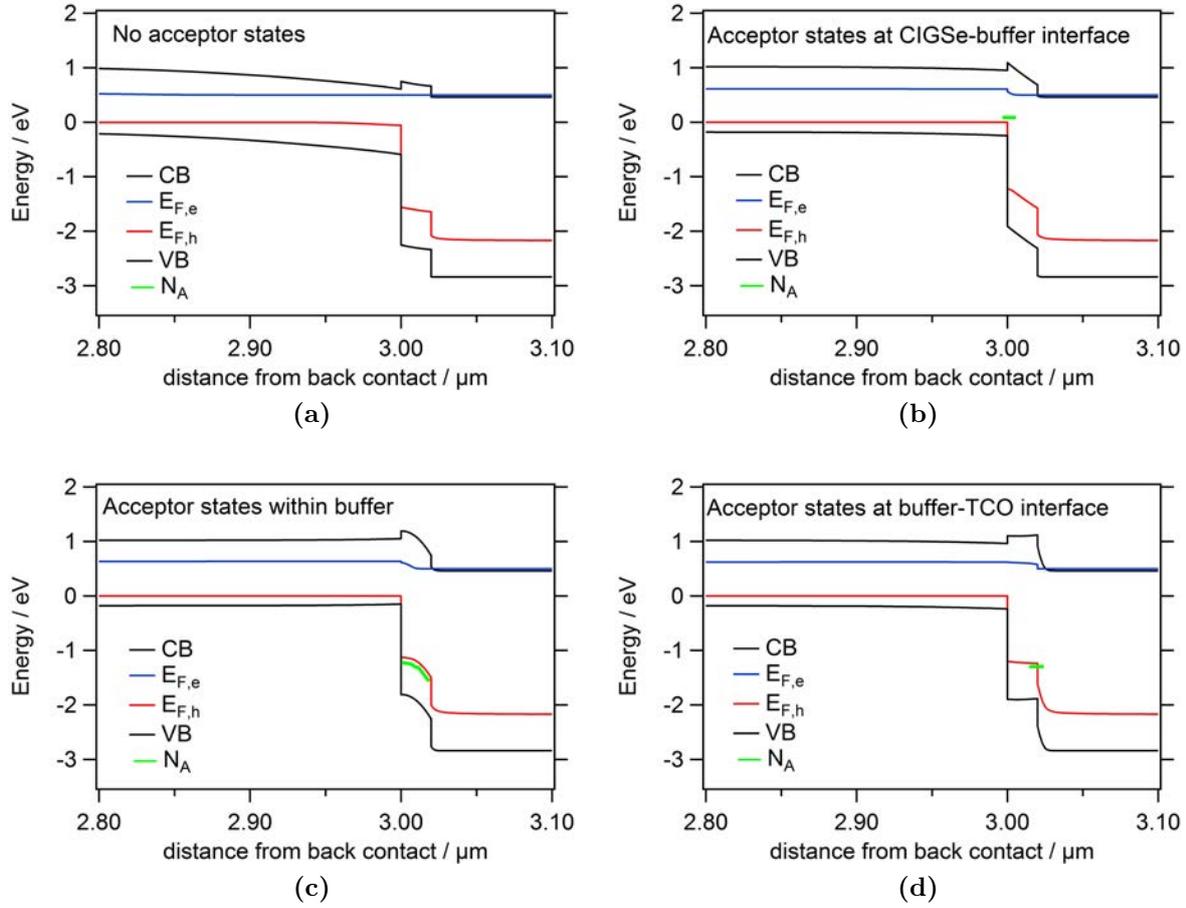


Figure 3.3: Energy band diagrams at the hetero-interface region of a CIGSe/buffer/ZnO solar cell, the voltage bias was set to +500 mV. The influence on the band alignment of acceptor states N_A at different energetic and spatial positions (green line) is shown in the graphs b), c) and d).

3.2 Acceptor states at the hetero-interface

As shown earlier the quality of the CIGSe/buffer interface determines interface recombination losses, but also the bulk recombination can be influenced by the interface quality. An electron barrier at the hetero-interface induced by a conduction band spike or due to acceptor states at the interface lead to a slower electron extraction and hence a possible higher bulk recombination loss. In this section both of these factors are studied exemplary on a bulk limited CIGSe device model. The results presented here will become important for the discussion of the device properties in Sec. 5.2 and Sec. 8.3. It should be noted that interfacial donor defects cannot induce electron barriers in CIGSe devices and are therefore not considered in this section.

Within the applied model, the electron diffusion length is set to a relatively low value of 500 nm. No band gap gradings are set and the electron affinity of the buffer χ_{buffer} was

chosen to be the same as of the CIGSe layer (in Fig. 3.3 a CBM spike is shown only to visualize the interface to the buffer layer). The cross section of the acceptor states were chosen to be small in order to limit recombination induced by them.

The influence of the spatial position of the acceptor states on the energy band diagram is shown in Fig. 3.3. The diagram shows the situation at a forward bias of +500 mV, close to the V_{OC} . χ_{buffer} is chosen to induce a small spike for better illustration of the effects, for the simulations shown in Fig. 3.4 it was set to the CIGSe value.

For the situation that no acceptor states are present at the interface the space charge region expands into the CIGSe absorber and the inversion at the interface is strongly pronounced as seen in Fig. 3.3a. The presence of a high density of interfacial acceptor states removes the inversion within the CIGSe layer completely, independent of whether the states are located at one of the buffer interfaces or in the buffer bulk, Fig. 3.3b-d. This can have several effects. As shown earlier, the interface recombination losses will increase, but also the electron collection will be reduced due to the missing space charge region within the CIGSe. If the acceptor density is sufficiently high, the electron quasi-Fermi level drops down towards the acceptor level. This leads to an increase of the CBM at the position where the acceptor states are located and therefore to an electron barrier. Such a barrier can reduce the extraction efficiency and increase the bulk and interface recombination. In the following it will be shown how acceptor states at three different locations effect the device performance.

Acceptor states at the interface between CIGSe and the buffer layer can lead to a pinning of the Fermi level (in the dark) at the interface. The consequence of this is, that the width of the space charge region within the CIGSe does not vary with the applied voltage bias and is determined by the energetic position of the acceptor state. Fig. 3.3b shows an exemplary band diagram at a voltage bias of +500 mV for an acceptor state present 300 meV above the CIGSe VBM. It is seen that d_{SCR} within the CIGSe becomes almost zero. Interface states energetically located higher than 300 meV above the CIGSe VBM would increase d_{SCR} , whereas states closer to the valence band would further reduce d_{SCR} and possibly introduce a barrier. Fig. 3.4a shows the effect on the current collection. Due to the reduced space charge region width the photo-current becomes smaller. The open circuit voltage increases since the electron density within the CIGSe is strongly reduced. A kink in the $J - V$ curve can develop if a conduction band spike is present or if the acceptor state is closer to the CIGSe valence band. The density of the defect states have a strong influence on the measured capacitance as can be seen in Fig. 3.4b. A characteristic of the Fermi level pinning is the flat profile of the capacitance profile.

A high concentration of acceptor states located within the buffer layer, lifts up the conduction band relative to the electron quasi-Fermi level within the buffer. An electron barrier develops with a similar energetic height for both, the electron extraction (photo-current) and the electron injection (diode current) into the CIGSe. Thus, the $J - V$ curve in Fig. 3.4c exhibits a characteristic s-shape around the V_{OC} . At higher voltage biases, the series resistance does not increase. The $C - V$ curve in Fig. 3.4d shows a strong increase of the capacitance at forward bias, since at this condition the space charge region is confined

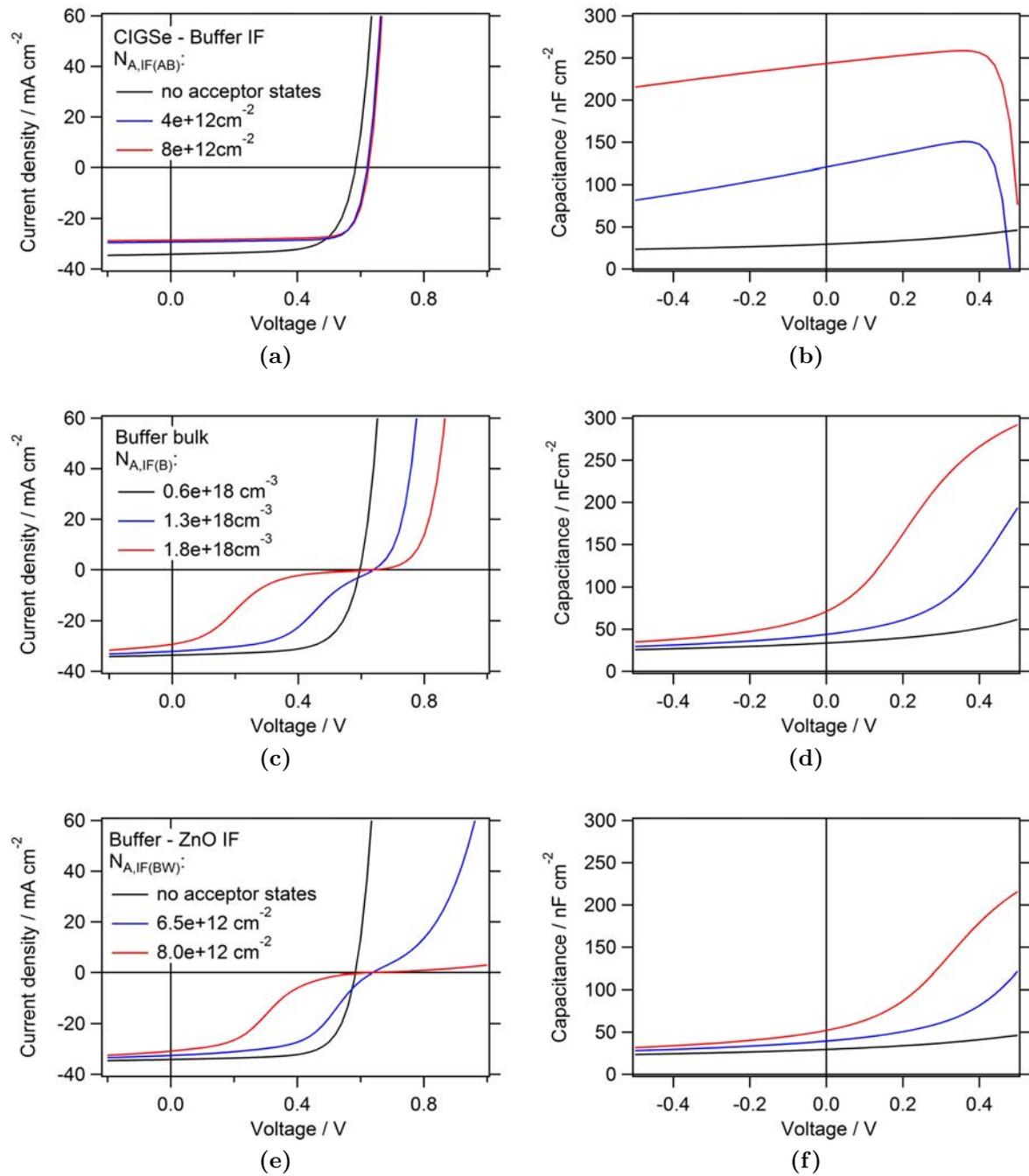


Figure 3.4: Simulated $J - V$ and $C - V$ (1 kHz) curves at 293 K for different positions and densities of acceptor states at the hetero-interface of a CIGSe/buffer/ZnO solar cell. The electron affinity of the buffer and of CIGSe were set to the same value. **a)-b)** Acceptor states between CIGSe and buffer. **c)-d)** Acceptor states within buffer. **e)-f)** Acceptor states between buffer and ZnO. Interface recombination velocity was set to zero.

to the buffer layer and the space charge capacitance increases with $1/d_{\text{SCR}}$, see Eq. 2.6.

In case a high density of acceptor states is located at the interface between the buffer layer and the TCO, the space charge region at forward bias is limited to the TCO. This induces an electron barrier for electron extraction and injection, with the difference to the previous case, that the barrier for electron injection is higher than for extraction. This leads to a disturbed s-shape of the $J - V$ curve as shown in Fig. 3.4e. The onset of the current injection is pushed to higher voltages compared to the situation when the acceptor states are located in the buffer layer. The capacitance is slightly smaller but both situations lead to similar capacitance profiles.

Another cause for an electron barrier at the hetero-interface between CIGSe and the buffer layer is a large conduction band spike, e.g. when χ_{buffer} is 500 mV smaller compared to χ_{CIGSe} . The effect on the $J - V$ curve of such a barrier is shown in Fig. 3.5a. The effect is similar to an increases series resistance, as the barrier height is comparable for electron extraction as for injection. The barrier has no influence on the V_{OC} since the Fermi level is less influenced by the conduction band alignment. Further it only has a negligible influence on the measured capacitance (Fig. 3.5b).

In the presence of a high density of acceptor states within the buffer layer, it was shown above that a barrier can be present already for $\chi_{\text{buffer}} = \chi_{\text{CIGSe}}$. As shown in Fig. 3.6a this barrier increases strongly for a slightly reduced χ_{buffer} . On the other hand, the barrier can be reduced by increasing χ_{buffer} above χ_{CIGSe} . Thus, in the case of high acceptor densities at the interface, a slight cliff may be beneficial for the device performance.

In case of a high acceptor density within the buffer layer and a high interface recombination velocity at the CIGSe-buffer interface, the negative effect of a conduction band cliff sets in, as described in the previous section. The V_{OC} decreases linear with the decrease of χ_{buffer} (Fig. 3.6b).

In summary, the shape of the $J - V$ and $C - V$ curves are good indicators for the existence and the location of interfacial acceptor states. It allows to differentiate between interfacial electron extraction barriers induced by a spike in the CBM or by charged acceptor states. This will become important during the study of the CIGSe superstrate solar cells in the next Chapter.

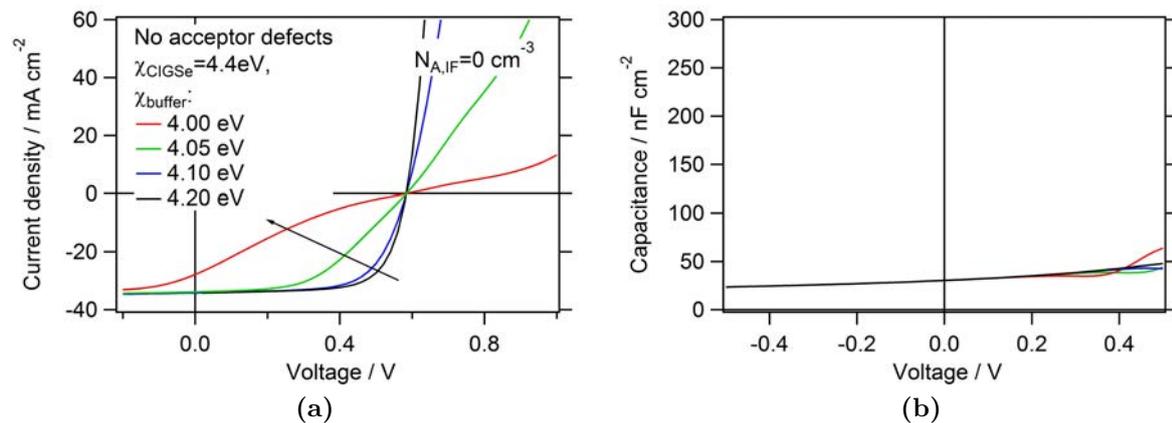


Figure 3.5: Simulated $J - V$ and $C - V$ (1 kHz) curves at 293 K. Variation of the buffer electron affinity in the absence of interfacial acceptor states.

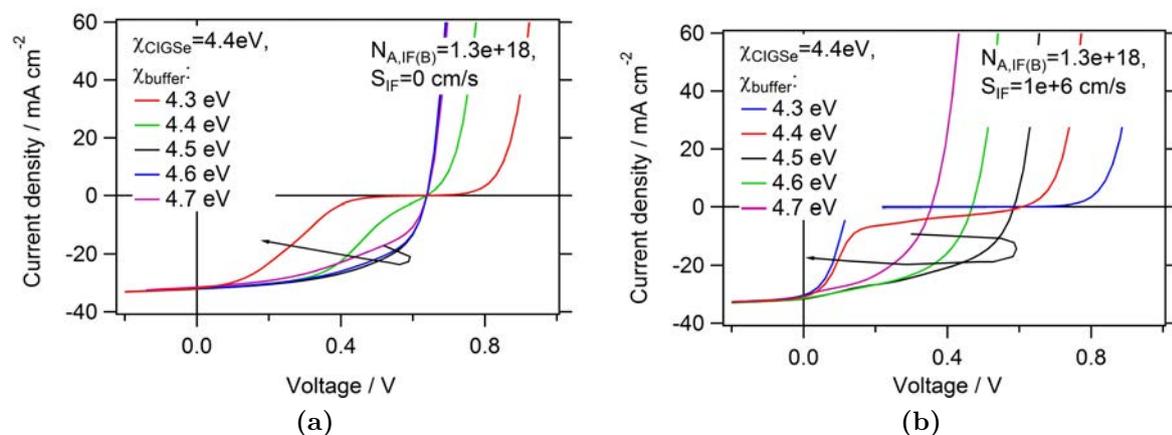


Figure 3.6: Simulated $J - V$ curves at 293 K. Variation of the buffer electron affinity in the presence of interfacial acceptor states and **a)** low interface recombination velocity or **b)** high interface recombination velocity.

Chapter 4

TCO evaluation

The basic requirements on a TCO used as the window layer in a CIGSe superstrate device is first of all good optical transparency between 1.2 eV (CIGSe band gap) and 3 eV of photon energy combined with a low sheet resistance, $<10 \Omega/\square$. Further, if the TCO is forming the p/n -junction with CIGSe, the TCO electron affinity is important to reduce the interface recombination losses (Sec. 3.1). However, it is difficult to predict which TCO will be best suited, since little is known about the formation of the inter-facial phases (Sec. 1.2) and their influence on the device performance [115]. Therefore this chapter will compare the performance of different TCOs in CIGSe superstrate devices. In depth interface analysis will be done for the most promising TCO in the subsequent chapter.

4.1 FTO, ITO and ZnO

The three most commonly used TCOs in photovoltaics are $\text{In}_2\text{O}_3:\text{Sn}$ (ITO), $\text{SnO}_2:\text{F}$ (FTO) and $\text{ZnO}:\text{Al}$ (AZO). This section will compare their performance as the window layer in CIGSe superstrate solar cells without buffer layer. The AZO was capped with a 100 nm thick layer of $i\text{-ZnO}$, which therefore forms the interface with the CIGSe. All TCOs were deposited on alkali containing glass substrates. The sheet resistance of the three TCOs, measured before and after the CIGSe deposition, are listed in Tab. 4.1, together with the V_{OC} and the η of the resulting solar cells.

Fig. 4.1a shows the $J - V$ curve for the three TCOs upon which a CIGSe layer was deposited at 560°C via the modified three stage process as described in Sec. 2.1. The most striking difference between the device performances is the difference in V_{OC} . The V_{OC} of the ZnO device is 400 mV, the V_{OC} of the ITO device 120 mV and the V_{OC} of the FTO device is 0 mV. The FTO device is not shunted though, as a rectifying behaviour at negative voltage biases can be observed. The ITO device shows the largest short circuit current, $28 \text{ mA}/\text{cm}^2$ and the lowest series resistance, $1.7 \Omega\text{cm}^2$, compared to the ZnO device with $23 \text{ mA}/\text{cm}^2$ and $3.3 \Omega\text{cm}^2$. Still, η of the ZnO device is the highest with 2.4%, followed by the ITO device with 1%. The sheet resistance of the TCOs after the process were almost unchanged as shown in Tab. 4.1. Even for CIGSe depositions at lower temperatures the highest device efficiencies were achieved by using ZnO as the window

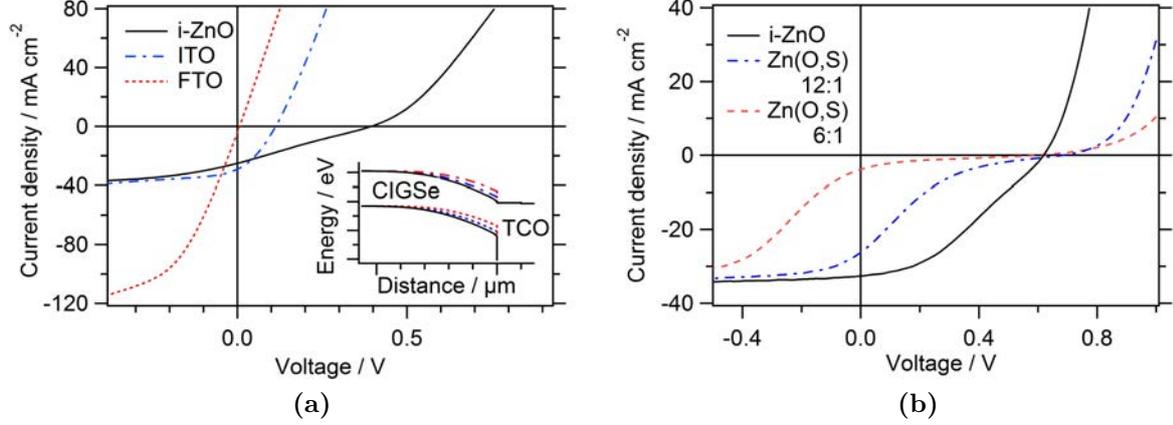


Figure 4.1: **a)** $J - V$ curves of Au/CIGSe/TCO superstrate devices with $\text{In}_2\text{O}_3:\text{Sn}$ (ITO), $\text{SnO}_2:\text{F}$ (FTO) and $\text{i-ZnO}/\text{ZnO}:\text{Al}$ (ZnO) as the TCOs. CIGSe deposited at 560°C . Inset: CBM and VBM levels of the different CIGSe/TCO stack. **b)** $J - V$ curves of Au/CIGSe/ $\text{Zn}(\text{O},\text{S})/\text{ZnO}:\text{Al}$ devices with varying sulphur content in the $\text{Zn}(\text{O},\text{S})$ layer. CIGSe deposited at 520°C .

layer (not shown here).

Discussion The significant difference in the V_{OC} of the devices with the different TCOs is likely to originate from the different interface formation of each TCO with the CIGSe layer. In [116] the formation of Ga_2O_3 was observed for CIGSe growth at 550°C on ZnO and on In_2O_3 , but not for SnO_2 . This may be a reason for the increased V_{OC} of ITO and ZnO . Further, in [117] the electron affinities χ of these oxides are compared, where χ for ZnO is listed as 4.5eV , very similar to the one of CIGSe, 4.7eV for ITO and 4.9eV for FTO. Thus, a conduction band cliff forms at the CIGSe interface to ITO and FTO. This is shown schematically in the SCAPS band diagram of Fig. 4.1a. According to Fig. 3.1 in Sec. 3.1 a cliff like conduction band alignment leads to a strongly reduced V_{OC} in the presence of interface defects. For high interface recombination velocities, the drop in V_{OC} was shown to be equivalent to $\Delta E_{\text{C,IF}}/q$ at the TCO/CIGSe interface. For FTO the difference in V_{OC} compared ZnO is 400mV , which is exactly the difference in their electron affinity. For ITO the difference in V_{OC} is 280mV compared to 200meV difference of their electron affinity. Thus, despite the different chemical interface formation the V_{OC}

Table 4.1: Comparison of the standard TCOs and their performance in CIGSe superstrate devices. Note that χ_{ZnO} of 4.6eV is used for the device simulations in this work.

TCO	$R_{\text{sq,before}} [\Omega/\square]$	$R_{\text{sq,after}} [\Omega/\square]$	$\chi [\text{eV}]$	$V_{\text{OC}} [\text{mV}]$	$\eta [\%]$
FTO	8	9	4.9	0	0
ITO	6	6	4.7	120	1
$\text{i-ZnO}/\text{ZnO}:\text{Al}$	6	6	4.5	400	2.4

correlates well with the electron affinities of the TCOs, as expected in case of a high interface recombination velocity (as shown in Fig. 3.1).

The higher series resistance of the ZnO device compared to the other two devices is seen in Tab. 4.1 does not originate from the degradation of the ZnO conductivity. The formation of Ga₂O₃, as observed in the literature, may lead to the increased series resistance.

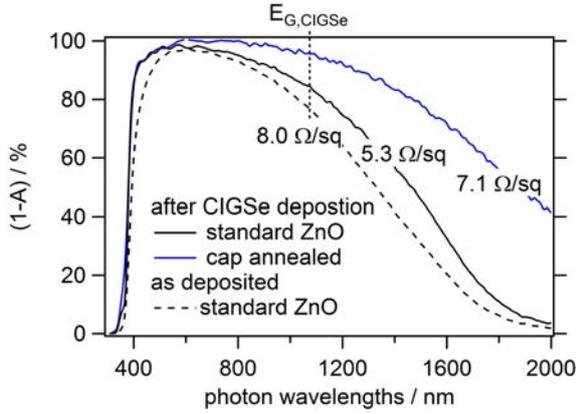
Despite the poor efficiencies of all the devices with different TCOs, ZnO seems to be the TCO with the highest potential for superstrate devices as it reproducibly lead to the highest open circuit voltages and power conversion efficiencies. In Sec. 5 the interface formation between ZnO and CIGSe with varying Ga content will be studied in order to understand and optimize the system.

4.2 Zn(O,S)

In CIGSe substrate solar cells typically Zn(O,S) is used to replace the CdS buffer layer with an oxide material. The advantage of Zn(O,S) over ZnO is the reduced electron affinity, turning the conduction band cliff into a conduction band spike and reducing the interface recombination. Good results for substrate devices were obtained for different deposition methods, like sputtering [118], chemical bath deposition [119] and ALD [120]. In superstrate configuration it hasn't been tested so far. Here, Zn(O,S) with different O/S ratios was deposited via ALD onto i-ZnO/ZnO:Al substrates and used as the buffer layer for superstrate CIGSe solar cells. Experimental details of the Zn(O,S) deposition can be found in [121]. The Zn(O,S) layer was deposited by an alternating sequence of ZnO and ZnS layers. The O/S ratio corresponds to the number of ZnO layers deposited before one ZnS layer was deposited. The ratio 12:1 corresponds to a S/(S+O) in the layer of approximately 0.16 and 6:1 to approximately 0.3. According to [122], this leads approximately to an electron affinity reduction of 150 meV for the 12:1 ratio and 300 meV for the 6:1 ratio. The CIGSe absorber was deposited at 520 °C via the modified three stage process.

The resulting $J - V$ curves are shown in Fig. 4.1b. The $J - V$ curves of the i-ZnO device exhibit a relatively poor fill factor but high open circuit voltage of 610 mV and a short circuit current of 32 mA/cm². The devices with Zn(O,S) exhibit a strong s-shape character. The 12:1 Zn(O,S) layer shifts the photo-current decay and the injection current onset by around 250 mV. The 6:1 Zn(O,S) layer shifts the photo-current decay by around 600 mV.

Discussion According to Sec. 3.2 the s-shape character of the Zn(O,S) devices originate from a strong electron barrier at the hetero-interface. This is surprising, because the electron affinity of the Zn(O,S) devices are approximately 4.45 eV and 4.3 eV, far below 4.1 eV which would be required to lead to such $J - V$ curves (compare with Fig. 3.6a). But in Fig. 3.6c it was shown, that such a s-shape profile can occur for lower electron affinities, if a high density of acceptor states is present at the interface. In such a case,



std. ZnO	R_{sq}	n_e	μ_n
	Ω/sq	cm^{-3}	$cm^2(Vs)^{-1}$
as-dep.	8.0	$4e+20$	45
annealed	5.3	$3.7e+20$	60

(a)

(b)

Figure 4.2: a) Transmission curves, corrected for the reflectance, of standard as-deposited ZnO:Al and of ZnO:Al annealed during the CIGSe deposition process at 525°C. The corrected transmission of the cap annealed ZnO:Al is shown for comparison. b) Sheet resistance of the standard ZnO samples measured with a four point probe. Free charge carrier density and electron mobility extracted from T and R spectra using a fitting procedure based on a Drude approach [123]. It should be noted that the improved properties are only observed on sodium free glass substrates.

it is beneficial to have a slight conduction band cliff at the hetero-interface, which is the case for i-ZnO.

4.3 ZnO annealing

With ZnO being the best performing TCO, it is interesting to study the effect of annealing. It is known that the opto-electronic properties of ZnO can be improved by annealing the ZnO under conditions prohibiting oxygen loss or chemi-sorption of oxygen. A very successful method was found to be annealing in nitrogen while capping the ZnO with SiO_x [17]. The application of such ZnO is attractive for CIGSe superstrate solar cells, as the optical losses can be strongly reduced. A similar effect is observed in this work simply due to the high-temperature CIGSe deposition onto the ZnO as shown in Fig. 4.2. The CIGSe/ZnO stack was cleaved after the process, which allowed to measure the sheet resistance and the optical transmission. It can be seen that both properties improve due to the annealing which occurred during CIGSe deposition. The average light absorption between 400 nm and 1100 nm is reduced from 10.7 % to 6.5 % which yields a photo-current increase of 1.5 mA/cm². At the same time does the sheet resistance decrease from 8 Ω/sq to 5.3 Ω/sq, which allows a thickness reduction of the ZnO:Al layer by 30 %.

It should be noted, that this is only observable when the sodium diffusion from the glass is blocked. A more detailed study of the ZnO annealing can be found in the appendix in Sec. 10.3.1. It is shown, that the increased mobility can be measured via the Hall technique and via the free carrier absorption. This proves that the improved properties

are induced by a bulk and not a grain boundary effect. It is assumed that the density of bulk defects, induced by the dopants, are reduced.

4.4 Summary: TCO evaluation

1. **Evaluation:** Different oxides, with different electron affinities, were tested as the window layer within the buffer-free superstrate solar cells. The highest efficiency was achieved by using a i-ZnO/ZnO:Al double layer. The oxides with higher electron affinity than ZnO lead to low V_{OC} values due to high interface recombination. The oxides with lower electron affinity lead to a strong electron barrier at the hetero-interface, presumably due to the combination of a high acceptor defect density and an increased electron affinity. Thus, even though ZnO leads to a slight conduction band cliff (50-100 meV) it leads reproducibly to the highest power conversion efficiencies. Therefore the chemical and electronic properties of the CIGSe/ZnO interface will be studied in the following sections.
2. **ZnO annealing:** The CIGSe deposition onto the ZnO layer was shown to improve the electron mobility and the transparency of the ZnO, provided that no sodium diffuses from the glass into the ZnO.

Chapter 5

ZnO/CIGSe device and interface analysis

The p/n -heterojunction is the most important and the most sensitive part of a CIGSe solar cell and in the superstrate configuration it is at the same time the least controllable interface. As it was shown in Sec. 1.2, phase formations and diffusion processes are expected to occur at the interface between CIGSe and ZnO. Conduction band misalignment and lattice mismatch possibly lead to high interface recombination losses as shown in Sec. 3.1. Therefore the first section studies the interface formation in detail. The next section will correlate the solar cell performance to the different chemical compositions at the interface and find the optimum process condition. Finally, a comparison with ZnO/CIGSe devices in substrate configuration will be given to find a general conclusion for the ZnO/CIGSe interface. In the following the expression CIGSe/ZnO will be used as an abbreviation for ZnO:Al/i-ZnO/CIGSe.

5.1 Interface formation

This section studies the chemical interface formation of different chalcopyrites with ZnO. First the experimental results will be described from Sec. 5.1.1 to Sec. 5.1.5, while the discussion of all results takes place in Sec. 5.1.6.

5.1.1 CGSe/ZnO interface formation

A CGSe thin film was deposited via the 3-stage-process (see Sec. 2.1) on top of the i-ZnO/AZO double layer coated with a 10 nm NaF precursor. The deposition temperature was 330 °C in the first stage and 520 °C in the second and third stage. To study the interface reaction between the CGSe and the ZnO layer, an SEM image and a GDOES depth profile were recorded from the CGSe/ZnO sample (Fig. 5.1 and 5.2a).

The SEM image shows poly-crystalline growth of the CGSe layer on top of the ZnO, with no correlation of their morphology. No inter-facial layer from the reaction of CGSe with ZnO layer can be immediately identified. The GDOES elemental depth profile in

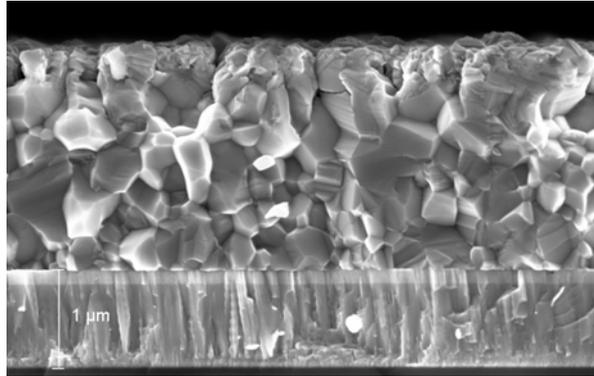


Figure 5.1: SEM image (InLens detector) of CGSe grown on ZnO at 520°C. The top 100 nm of the ZnO stack appears brighter in the SEM picture, when recorded with the InLens detector, due to the lower doping density of the i-ZnO compared to the darker appearing AZO.

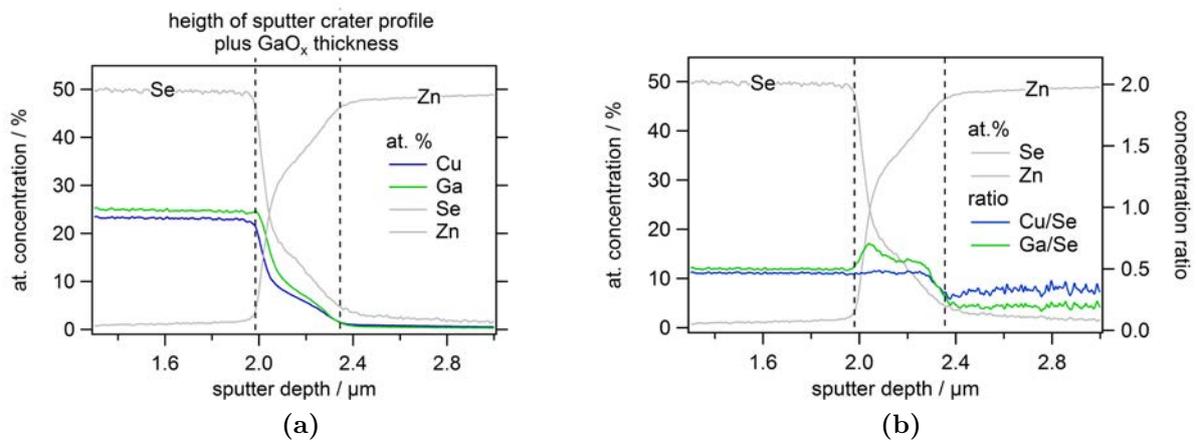


Figure 5.2: a) GDOES elemental depth profiles of the CGSe/ZnO stack. The dashed lines mark the approximate height of the sputter crater profile, which leads to the misleading appearance of an intermixed interface. It is around 370 nm. b) Depth profile of the Ga/Se and Cu/Se ratios from the same sample. The increased Ga/Se ratio at the interface indicate that Ga is partially bound to O instead of Se.

Fig. 5.2a shows the hetero-interface region. The edges of the hetero-interface are marked with two dashed lines. The distance between the hetero-interface edges is defined by the depth/homogeneity of the sputter crater profile (see inlet of Fig. 2.9b), the surface roughness and the thickness of a potential interfacial layer. At the hetero-interface the Cu, Ga and Se signal decrease similar to the elemental profiles shown in Sec. 2.5.3 and as expected from a typical sputtering crater profile. The GDOES setup is not able to detect oxygen in order to identify interfacial oxide layers, however, the profile of the Ga/Se ratio, shown in Fig. 5.2b, is expected to rise once the Ga is partially bound to O instead of Se. And indeed, within the interface region, the Ga/Se ratio increases. This increase could also originate from the formation of a Ga_2Se_3 phase, but this should lead to a simultaneous change of the Cu/Se ratio, which cannot be observed. Therefore the Ga atoms at the ZnO interface have to be bound partially to oxygen instead of selenium, forming an GaO_x rich layer. This is in accordance with the thermo-dynamical considerations in Section 1.2. Further, the constant Cu/Se ratio within the interfacial region, indicates that the Cu atoms around the interface are bound within the CGSe matrix. This shows, that the composition close to the interface is not Cu depleted compared to the bulk, and that no formation of CuO_x occurs at the interface.

In summary, only a thin layer rich in GaO_x forms at the interface, which can be identified from the increased Ga/Se GDOES signal ratio within the interfacial region, but cannot be identified in the SEM picture.

5.1.2 CISE/ZnO interface formation

Similar to the CGSe/ZnO sample, CISE was deposited on top of the i-ZnO/AZO double layer coated with a 10 nm NaF precursor at a substrate temperature of 550 °C. An SEM image of the stack is shown in Fig. 5.3. The CISE layer grows poly-crystalline on top of the ZnO, with no morphologic correlation to the ZnO layer. At the interface to the ZnO a thin layer of around 30 nm thickness can be seen. The GDOES elementary depth profile of the region around the CISE/ZnO interface is shown in Fig. 5.4a. The interface region is marked with two dashed lines. At the interface, a strong increase of the In signal (in Fig. 5.4a and of the In/Se signal (in Fig. 5.4b) can be observed. Similar to the CGSe/ZnO case the formation of In_2Se_3 at the interface can be excluded, since the Cu/Se ratio does not decrease simultaneously. Thus, the In atoms close to the ZnO interface have to be partially bound to oxygen instead of selenium, forming an InO_x rich layer. Again, this is in accordance to the thermo-dynamical considerations. The constant ratio of Cu/Se before it drops into the noise level indicates that the Cu atoms close to the interface are bound within the CISE matrix and that no formation of CuO_x occurs at the interface.

Compared to the CGSe/ZnO system, the interfacial oxide layer in the CISE/ZnO system is thicker and can be seen in the SEM image and from the higher In/Se ratio compared to the Ga/Se ratio in the GDOES depth profiles. In addition, the elemental GDOES depth profiles differ in shape at the hetero-interface. At the CGSe/ZnO interface (Fig. 5.2a) the Se and Cu signal decrease sharply followed by a longer tail, as expected for sharp interfaces (compare with Sec. 2.5.3). In the CISE/ZnO system the profiles do not show this

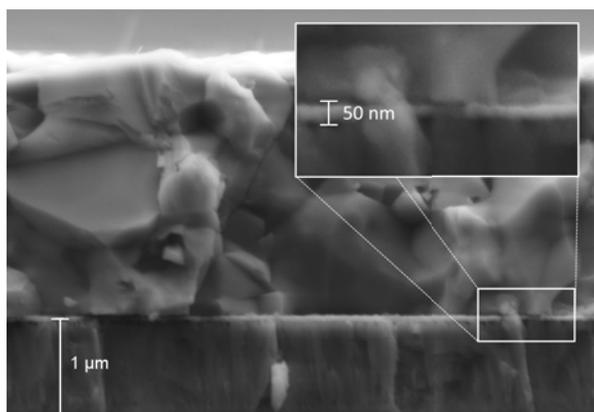


Figure 5.3: SEM image (SE detector) of CIGSe grown on ZnO at 520°C. The magnified area shows the InO_x layer at the CIGSe/ZnO interface.

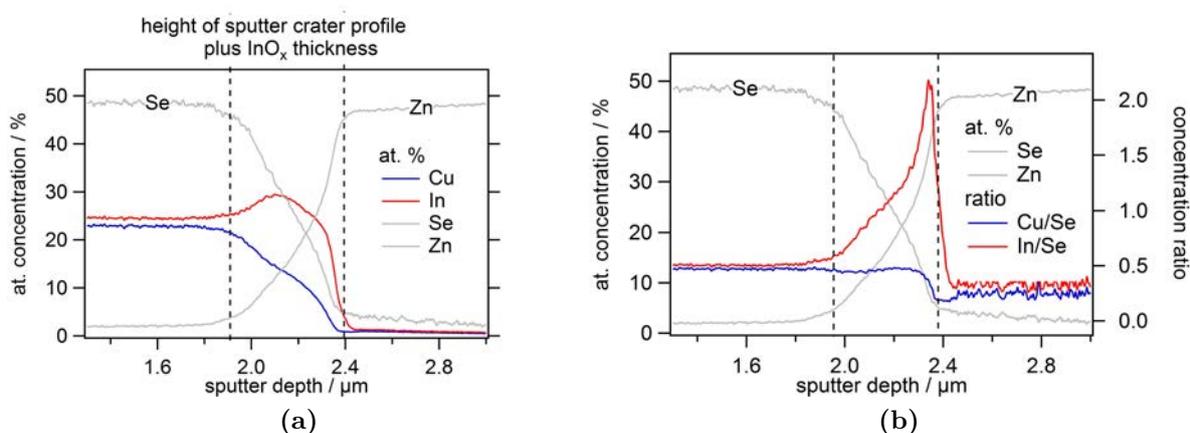


Figure 5.4: a) GDOES elemental depth profiles of the CIGSe/ZnO stack. The dashed lines mark the approximate height of the sputter crater profile plus the InO_x thickness, which is around 470 nm. b) Depth profile of the In/Se and Cu/Se ratios from the same sample. The increased In/Se ratio indicates the InO_x layer at the interface.

sharp signal change at the interface. Surface roughness and the sputter conditions were similar for the CIGSe and CGSe samples and cannot explain this effect. This indicates, that the interfacial InO_x layer is not a sharp interface but that it is heavily intermixed with Se, Cu and Zn. Furthermore, the In/Se profile increases over the interfacial region until it reaches the maximum value at the ZnO side, showing that the reaction front is at the interface to ZnO, as expected from the thermo-dynamical calculations.

In the following this interfacial oxide layer will be named InO_x for simplicity.

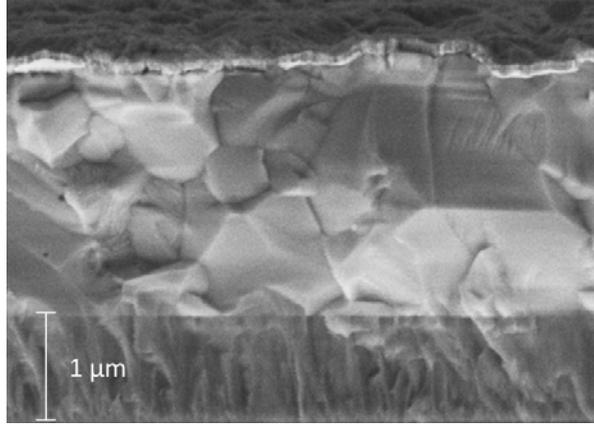


Figure 5.5: SEM image (SE detector) of CIGSe grown on ZnO at 525 °C, with Au on top as the back contact.

5.1.3 CIGSe/ZnO interface formation

In CIGSe/ZnO stacks the question arises whether the formation of InO_x or GaO_x dominates, or whether an $(\text{In}_y, \text{Ga}_{1-y})\text{O}_x$ alloy forms. Fig. 5.5 shows an SEM image of a sample fabricated with a modified three stage process at $T = 525^\circ\text{C}$ without sodium addition, as described in Sec. 2.1. The CIGSe layer grows poly-crystalline with no morphologic correlation to the ZnO layer. No inter-facial layer can be directly identified. To study the interface formation between CIGSe and ZnO TEM images were taken and XPS spectra of cleaved samples were recorded.

TEM analysis Fig. 5.6a shows a HR-TEM image of the hetero-junction region. In the region between the CIGSe and the ZnO an approximately 6 nm thick layer can be identified. Fig. 5.6b shows an interface image taken at a different, thinner sample area. The interfacial layer is marked in red within this image. The layer thickness varies between 4 and 6 nm, thus around $\pm 20\%$. To identify the crystalline structure of the interfacial layer a fourier transform (FFT) of this image was calculated at the interface, the ZnO and the CIGSe area. The FFT images of the ZnO and the CIGSe areas show distinct peaks originating from the periodicity of the lattice planes, with $d_{\text{ZnO}}=0.27$ nm and $d_{\text{CIGSe}}=0.32$ nm. The FFT of the interface layer does not show any peaks characteristic for a crystalline structure, which leads to the conclusion that the layer has an amorphous structure. The chemical composition of the interface layer is obtained by a TEM-EDX line scan over the interface at a thicker part of the TEM sample. The EDX profile is shown in Fig. 5.7a. Clearly visible from this measurement is that the amorphous layer consists of a segregation of Ga. No segregation of In or Cu is visible. The O profile is shifted 4 nm from the Zn profile towards the CIGSe layer, indicating that the Ga is bound to oxygen within a few nanometer thick layer. The FWHM of the Ga EDX signal peak is 22 nm, which is broader than the width of the actual interfacial layer, since it is the projection of a rough interface.

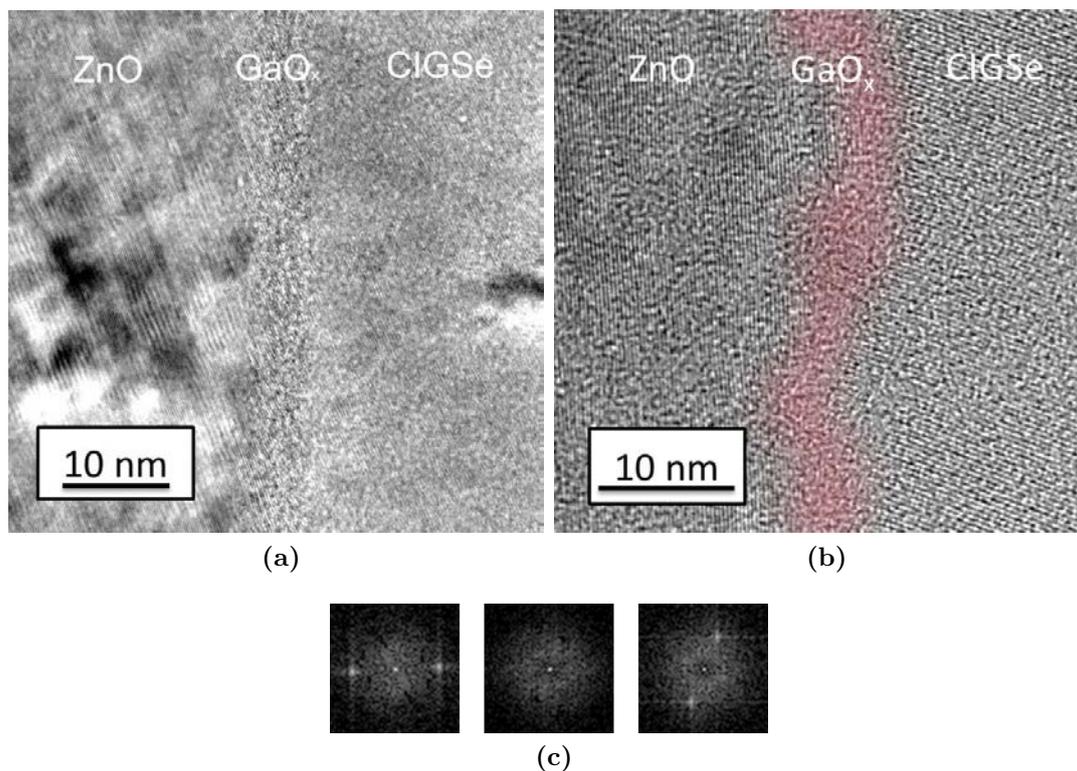


Figure 5.6: **a)** HR-TEM image of the CIGSe/ZnO interface. The CIGSe is grown at 525°C without additional NaF supply. **b)** HR-TEM image of the same CIGSe/ZnO interface recorded at a thinner sample area used for EDX analysis. The interface layer between CIGSe and ZnO is coloured in red. **c)** From left to right: FFT of the ZnO area, peak corresponding to 2.7 Å (spacing of the (002) lattice planes). FFT of the interface area, no peaks visible. FFT of the CIGSe area, peak corresponding to 3.5 Å (spacing of the (112) lattice planes). The same amount of pixels were used for all three FFTs.

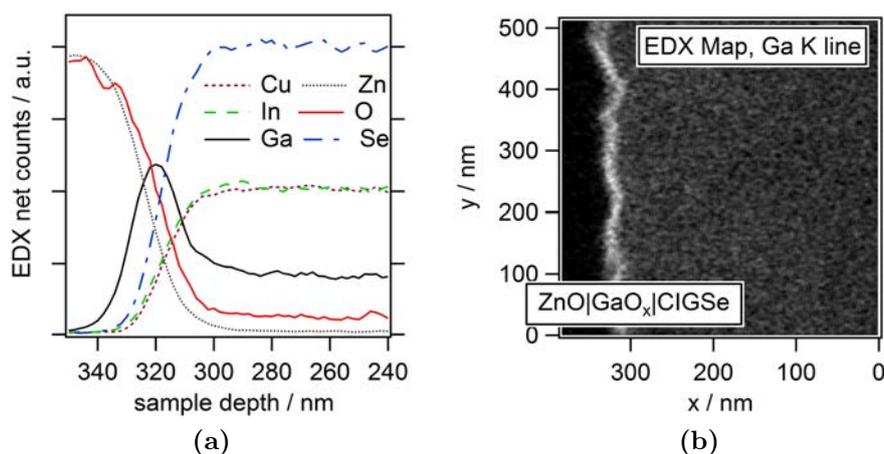


Figure 5.7: **a)** TEM-EDX line profile showing the elemental depth profiles at the CIGSe/ZnO interface **b)** TEM-EDX map of the same interface region. The GaO_x layer is clearly visible due to the increased Ga K line signal at the GaO_x layer.

A two-dimensional EDX map of the Ga Signal from the same interface region is also shown in Fig. 5.7b. The Ga-rich layer observed in the one-dimensional plot can be observed along the hetero-interface. It covers the whole interface relatively homogeneous, with a variation of the FWHM of the Ga EDX signal peak of around $\pm 20\%$ along the interface, similar to the variation of the GaO_x thickness observed in Fig. 5.6b.

XPS analysis Further insight into the elemental composition of the interfacial layer was obtained by quantitative XPS measurements. To analyse the interface, the sample was cleaved by thermal shock at the interface between CIGSe and ZnO, as described in Sec. 2.5.2. The layer remaining on the glass substrate was the ZnO layer and the layer attached to the silver epoxy the CIGSe layer. As seen in Tab. 5.1 the surface of the ZnO layer contains all elements of ZnO and CIGSe. The quantitative analysis (details in Sec. 2.5.2) shows that it mainly consists of Ga, O and Se with impurities of Cu, In and Zn in the range of a few atomic percent. No sodium was detected at the interface. The information depth of the Ga and Zn XPS signal is around 2 nm. Assuming that the GaO_x layer is free of holes, the Zn signal does not originate from the ZnO underneath the interfacial layer. The concentration of Zn within the interfacial layer may increase closer to the ZnO layer though. The information depth varies for the different elements between 1.6 nm and 6.1 nm and the error of the quantitative results are around 60%, thus the chemical composition can only be approximated to $(\text{In}_y, \text{Ga}_{1-y})(\text{O}_z, \text{Se}_{1-z})_x \cdot \text{Zn}, \text{Cu}$, with y and z close to 1. In the following the interfacial layer will be named GaO_x whenever the In concentration is below 5 at.%, else it will be named $(\text{In}_y, \text{Ga}_{1-y})\text{O}_x$ or InO_x for $y=1$.

The surface of the CIGSe layer consists mainly of Cu poor CIGSe with around 1 at.% Zn and O contamination. The low Cu-content cannot be confirmed by the TEM-EDX depth profile in Fig. 5.7a.

Table 5.1: Quantitative results from XPS measurements shown in atomic % of all elements within a sample. The sample was cleaved at the CIGSe/ZnO interface. Care is to be taken since the relative error of the atomic concentrations is between 50% and 60%.

	inf. depth in ZnO nm	ZnO surface at.%	inf. depth in CIGSe nm	CIGSe surface at.%
Cu	2.4	3	3.1	13
In	4.6	5	5.8	25
Ga	1.6	44	2.1	6
Se	6.1	17	7.8	54
O	4.2	32	4.1	1
Zn	2.0	1	2.6	1
Na	4.2	0	2.3	0

Temperature dependence

In this section, the temperature dependence of the interfacial oxide formation is studied with the help of GDOES depth profiling. All samples were grown similar to the sample used for the TEM/XPS analysis and without external sodium supply. Figs. 5.8a-c show the ratios of the cations to selenium for various CIGSe deposition temperatures, each together with the Zn signal as a reference.

Interestingly, for the sample deposited at 420 °C, all cations, Cu, In and Ga, show a slight increase of their ratio to Se at the interface. Following the arguments given in the previous section, this originates from an anion substitution from selenium to oxygen within a thin layer at the interface. In this case the interfacial layer consists of all elements in similar concentration, forming a $\text{Cu}(\text{In}_y, \text{Ga}_{1-y})(\text{O}_z, \text{Se}_{1-z})_x$ layer.

At the deposition temperature of 520 °C it is known from the TEM and XPS measurements in the previous section, that a 6 nm thick GaO_x layer forms with impurities from Cu, In, Zn and Se. The GDOES signal ratios in Fig. 5.8b show indeed that mainly the Ga/Se ratio increases at the interface to ZnO, whereas The Cu/Se and the In/Se ratios show only minor deviations.

If the temperature is further increased to 550 °C (Fig. 5.8c), the Ga/Se ratio at the hetero-interface also increases further compared to the deposition at 520 °C. Indicating the growth of a thicker GaO_x layer at higher deposition temperatures. Interestingly though, at this temperature, the Cu/Se ratio at the hetero-interface increases noticeably as well, indicating detectable Cu diffusion into the GaO_x layer at such elevated temperatures.

The Ga/Se ratios for the three different profiles are shown together in Fig. 5.8d. The signal peak intensities of the ratios were calculated by fitting the signal peaks with Voigt functions using the horizontal dashed line in Fig. 5.8d as the baseline. The peak area of the Ga/Se ratio of the 420 °C sample is 25 %, and the intensity of the 550 °C sample 150 % of the peak intensity of the 520 °C sample. In the previous section, the GaO_x thickness for a 520 °C sample was shown to be approximately 6 nm, leading to an estimated GaO_x thickness of 9 nm for the 550 °C sample. The interfacial oxide layer of the 420 °C sample, consists of all elements and is therefore estimated to be around 3 nm thick.

5.1.4 Influence of Na

Since Na is an essential doping element for CIGSe it is important to study the influence of Na on the inter-facial phase formation between ZnO and the different CIGSe with varying Ga content.

NaF Precursor One way to supply sodium is by depositing a NaF precursor on the substrate prior to the CIGSe deposition. Here, 10 nm of NaF were deposited at 300 °C on top of the ZnO layer. In the literature it is known, that if present during the growth process, sodium slows down the Ga diffusion [124] and changes the preferential crystalline orientation of the CIGSe layer [47]. This work however, concentrates on the impact on the interface reaction in the CIGSe/ZnO and CGSe/ZnO system.

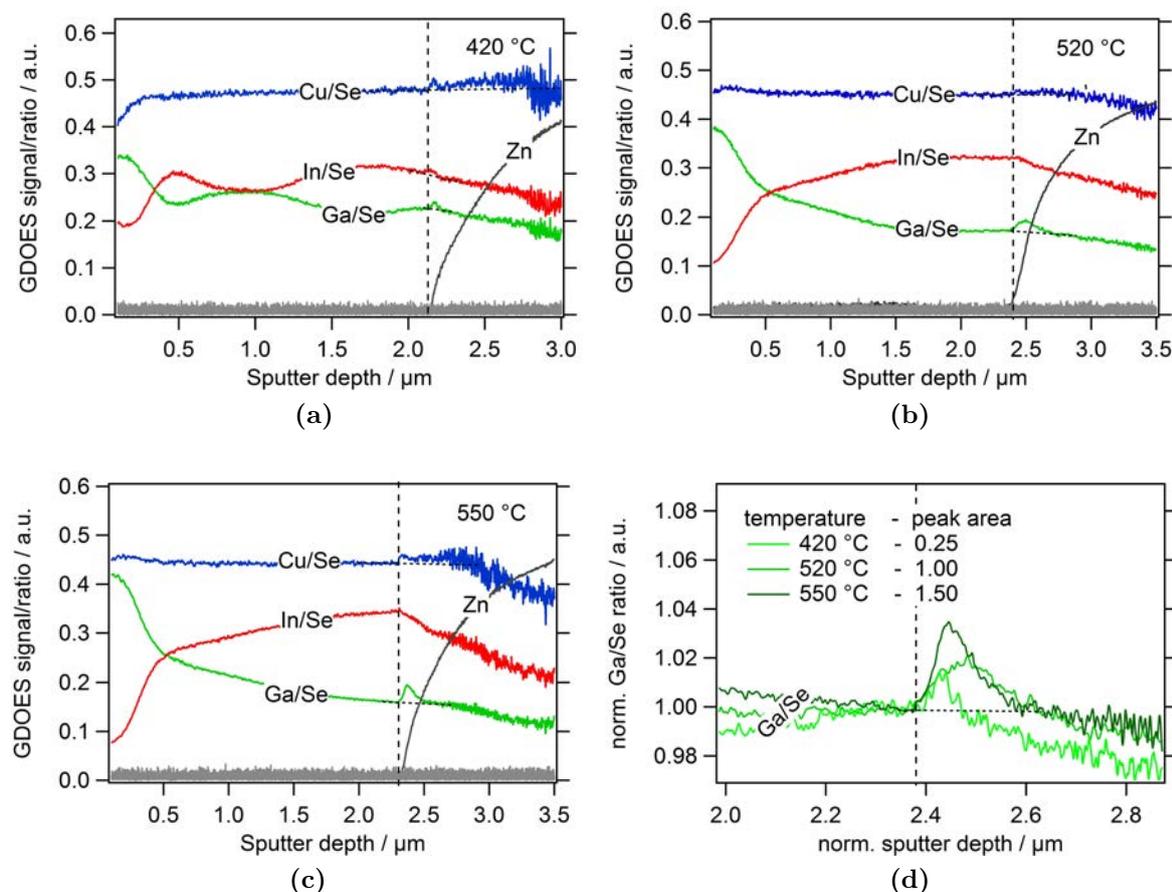


Figure 5.8: a) - c) Calibrated ratios of the cations to Se for different deposition temperature as stated in the graphs. The Zn profile is shown as a reference, the dashed lines indicate the interface with ZnO. d) Ga/Se ratios for the different temperatures, normalized to the same Ga/Se value just before the ZnO interface. The dashed horizontal lines are used as the baselines for the peak area calculations.

Figs. 5.9 and 5.10 show the GDOES elemental depth profiles of the resulting CGSe/ZnO and ClSe/ZnO stacks deposited with the NaF precursor layers in-between. The depth profiles of the elements Cu, In, Ga, Se, Zn, Na and Au are shown. Au is not present in the film and indicates the noise level. The GDOES signal intensities are not transformed into at.% since there is no calibration standard for sodium, which is required for this procedure. The interface region is marked with two dashed lines.

The shape of the sodium profile within the chalcopyrite is similar for both ClSe and CGSe. It shows a local maximum at the depth, approximately where the chalcopyrite surface was Cu-rich during growth (compare with Sec. 1.3.1). Most of the sodium remains at the hetero-interface though, where the shape of the profile shows two overlapping peaks (well resolved in the ClSe/ZnO stack in Fig. 5.9).

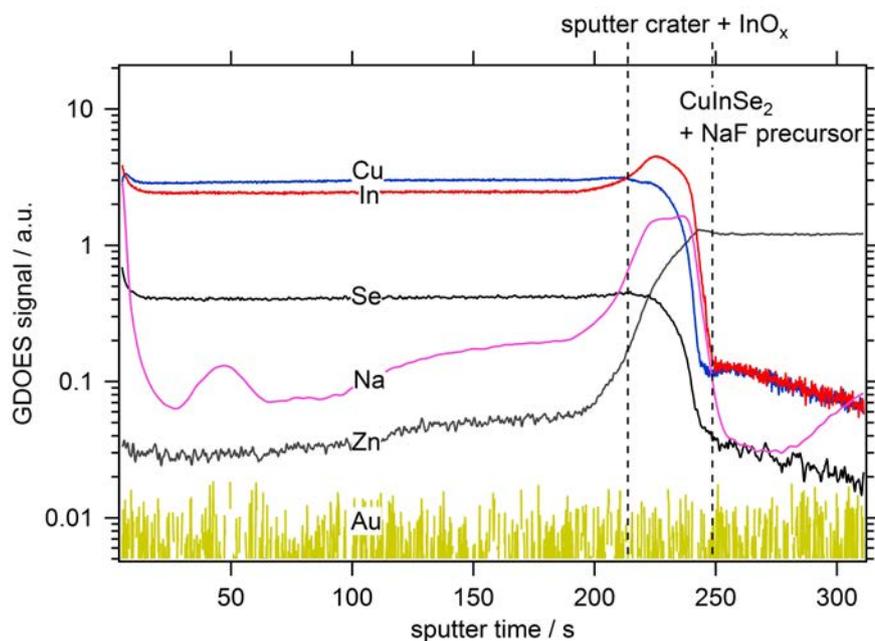


Figure 5.9: Uncalibrated GDOES depth profile of a $\text{CuInSe}_2/\text{ZnO}$ stack, fabricated with a NaF precursor.

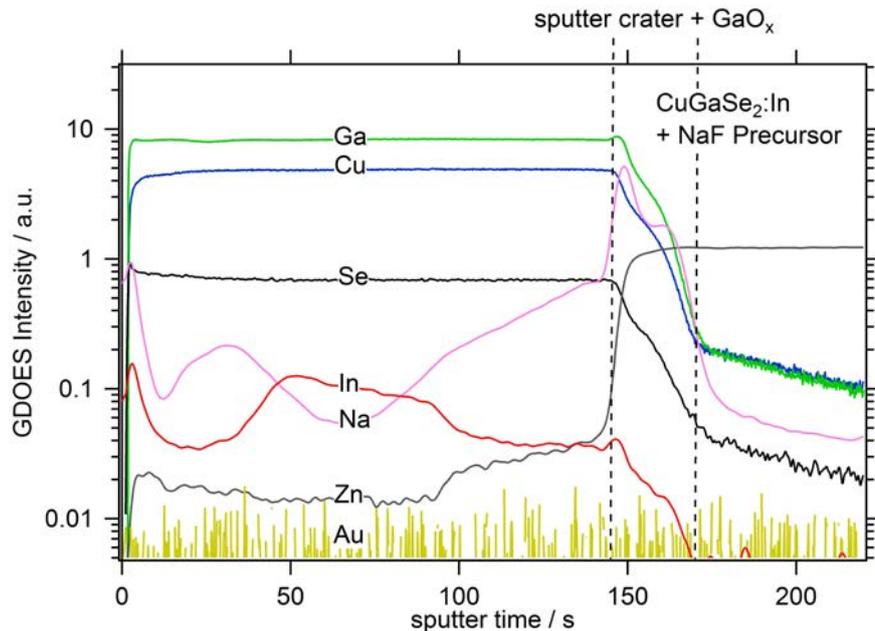


Figure 5.10: Uncalibrated GDOES depth profile of a $\text{CuGaSe}_2/\text{ZnO}$ stack, fabricated with a NaF precursor. Indium is present as an impurity from the deposition chamber.

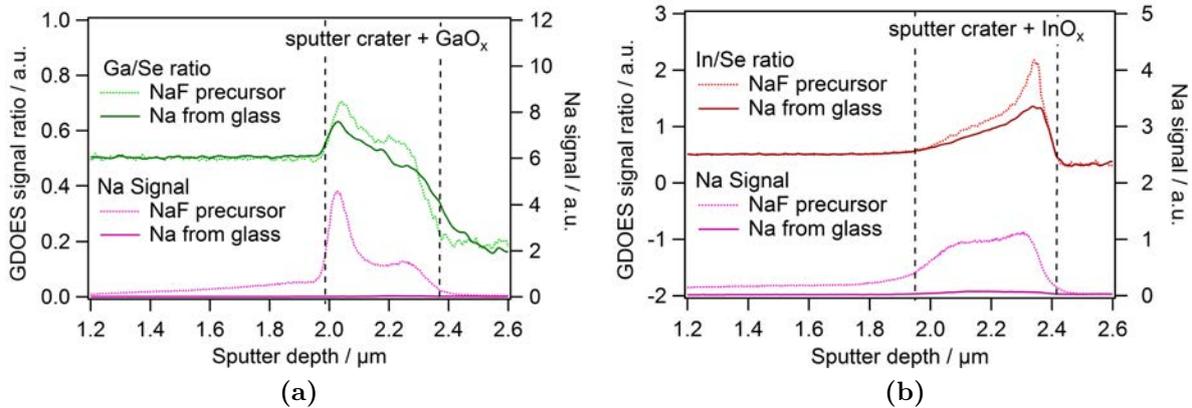


Figure 5.11: a) Depth profile of the Ga/Se ratio and the Na signal of CGSe on ZnO with and without NaF precursor. The increase in the Ga/Se signal at the interface relative to the bulk indicates the presence of GaO_x . Sodium catalyses the oxide formation. The dashed lines mark the interface region. b) Depth profile of the In/Se ratio of CIGSe on ZnO with and without NaF precursor.

Fig. 5.11 shows the sodium profiles together with the ratios of In/Se and Ga/Se of the two stacks. The ratios at the ZnO interface are increased for both stacks with NaF precursor. The increased ratio at the interface compared to the bulk can be explained by the increased binding of In and Ga with O instead of Se at the interface (see Sec. 5.1.2). A higher concentration of sodium at the interface clearly leads to a more pronounced formation of InO_x in CIGSe samples and GaO_x in CGSe samples.

Further, the shape of the sodium profile resembles the shape of the Ga/Se and the In/Se ratio, respectively. This indicates, that the sodium accumulates in the bulk of the GaO_x or InO_x layers and not on their interfaces to CIGSe and ZnO.

NaF post deposition treatment (PDT) The NaF precursor strongly enhanced the interface reaction between CIGSe and ZnO and appears not to be suitable for the fabrication of a superstrate solar cell with a very defined p/n -junction. An alternative for controlled sodium incorporation to the NaF precursor is the NaF post deposition treatment (PDT), which can be done at a temperature lower than the CIGSe deposition temperature. This paragraph studies the influence of a NaF PDT on CIGSe/ZnO stacks only, not separated for CIGSe and CGSe as it has been done for the NaF precursor.

10 nm of NaF were deposited after the CIGSe deposition by thermal evaporation onto the CIGSe surface. The substrate temperature after the NaF deposition was kept constant for 10 minutes before cooling down to room temperature. Fig. 5.12a shows the diffusion profile of sodium within the CIGSe absorber for different PDT substrate temperatures.

For the PDT temperature of 100°C it seems that no sodium diffuses into the absorber, but remains on the CIGSe surface. The low concentration of sodium found in the bulk and at the hetero-interface is most likely due to the sodium diffused from the glass substrate.

For the PDT temperature of 250 °C, the sodium is still mostly on the CIGSe surface, but the concentration is increased in the CIGSe bulk with the highest concentration found at the hetero-interface. The PDT at 400 °C leads to the highest sodium concentration within the CIGSe bulk and especially at the hetero-interface. The interface concentration is increased considerably compared to the interface concentration obtained by the PDT at 250 °C.

The Ga/Se ratio profiles of these samples are shown in 5.12b. The Ga/Se ratio of all samples slightly increases at the hetero-interface indicating the GaO_x formation. No change in the Ga/Se ratios can be observed for the samples with the different PDT temperatures. This indicates, that the Na PDT does not lead to an increased oxidation at the interface as it does for the NaF precursors. But similar as for the NaF precursor, Na accumulates within the interfacial oxide layer as seen from the Na peak position in the depth profile.

To get a more detailed view of the interfacial chemical composition before and after the Na PDT done at 300 °C, XPS measurements on cleaved samples were performed. As described in Sec.2.5.2, the samples were cleaved in an inert atmosphere at the CIGSe/ZnO interface. The sodium concentration is measured to be 6% on the ZnO side and 4% on the CIGSe side. These values are most likely not the real sodium concentrations within the layers, since sodium is prone to diffuse to the surface after cleaving the sample. Further, the oxygen concentrations are increased for the ZnO and the CIGSe surface compared to the sample without Na. This could be due to adsorption of oxygen on the CIGSe surface during the cleaving process from the oxygen solved within the liquid nitrogen. Whether or not the Ga is really more heavily oxidized due to the increased Na concentration or if the oxygen is simply bound to Na on the surface (i.e. to NaOH) can be verified by the analysis of the Ga *LMM* auger peak. The Ga *LMM* auger peak is reported in the literature to be around 1060.5 eV for Ga atoms bound to selenium and around 1057.5 eV if bound to oxygen [125]. Fig. 5.13 shows the normalized Ga *LMM* Auger peaks of the ZnO and CIGSe surfaces before and after the NaF PDT. The ZnO surface shows exactly the same auger peak profile for the surface with and without sodium. The CIGSe surface does not show any indication for oxidized Ga. Thus the increased oxygen concentration for the sodium containing surfaces are not relevant and originate from a thin layer of possibly NaOH. No further oxidation of the GaO_x occurs due to the PDT.

In summary, it is shown, that the sodium supply via NaF precursors leads to a strong increase of the oxidation of the CIGSe layer at the interface to ZnO. The sodium remains preferentially within this interfacial oxide layer. Sodium supply via PDT was effective for temperatures above 100 °C, when sodium diffuses into the CIGSe bulk and also accumulates within the interfacial oxide layer. This concentration at the interface increases strongly for temperatures above 250 °C. Despite the presence of sodium no further oxidation or growth of the GaO_x layer could be observed during the NaF PDT at temperatures of 300 °C.

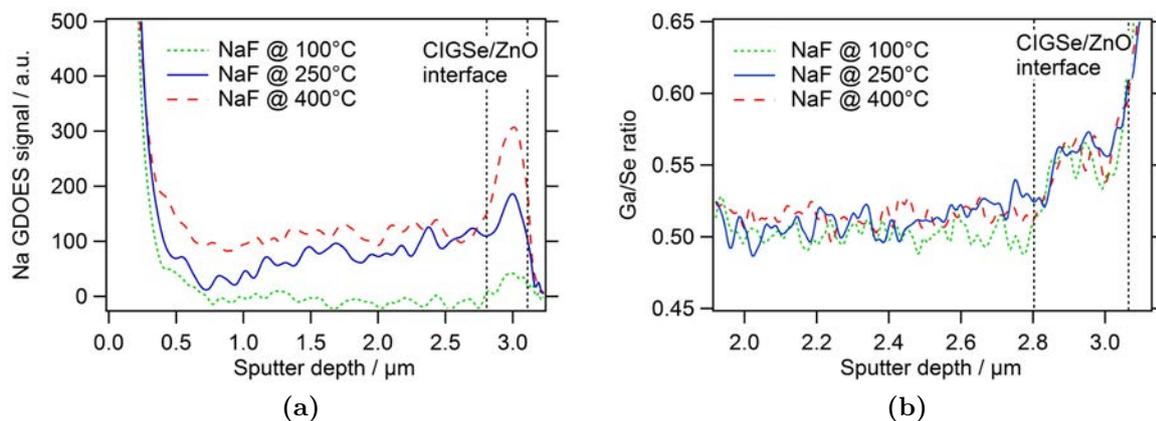


Figure 5.12: GDOES depth profiles of **a)** Na and **b)** Ga/Se ratio from samples with NaF post-depositions performed at different temperatures. The amount of sodium at the interface depends critically on the temperature.

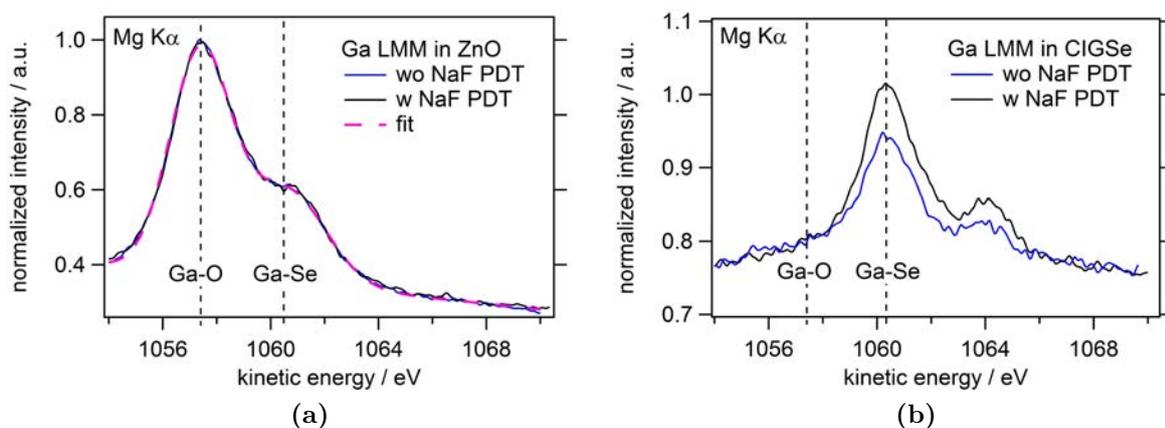
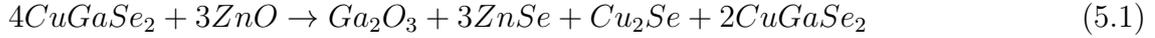


Figure 5.13: Normalized Ga *LMM* auger peaks from XPS measurements of the cleaved CIGSe/ZnO samples, with and without NaF PDT. **a)** ZnO side. Both spectra are fitted with two Gaussian functions and a linear background level. **b)** CIGSe side.

5.1.5 Diffusion of Zn

During the formation of the oxide layer in-between the chalcopyrite and the ZnO layer the following reaction occurs for the case of CGSe/ZnO (see Sec. 1.2):



The resulting ZnSe and Cu₂Se may remain as secondary phases at the interface or alloy with the chalcopyrite bulk. Zn diffusion profiles within CIGSe and CGSe deposited at 520°C, with and without NaF, are shown in Fig. 5.14. The average Zn concentration within the absorber correlates very well with the intensity of the interface reaction of the different chalcopyrites. From the SEM image in Fig. 5.3 it is known that CIGSe with a NaF precursor forms an approximately 30 nm thick interfacial InO_x layer, from which an average Zn concentration of around 2 at.% can be calculated within the CIGSe layer (calculation details are given below). This fits well to the GDOES intensity of Zn, which is between 1.2-2.5% within the CIGSe layer. This confirms that most of the ZnSe diffuses into the absorber layer. If sodium is not present during the absorber growth, the interface reaction is less pronounced and the Zn signal is around 1% in the CIGSe layer. The same trend can be observed for CGSe with a generally lower Zn concentration due to the lower interface reaction in the CGSe/ZnO system.

In the CIGSe/ZnO system, the interface reaction is even less pronounced and the Zn concentration cannot be approximated from the GDOES profiles, since the Zn signal does not rise above the noise level. But from the TEM image (Fig. 5.6) the GaO_x thickness is known to be around 6 nm. Taking the weight and molar density of ZnO (5.61 g/cm³ and 81,4 g/mol [126]) and Ga₂O₃ (6.44 g/cm³ and 187,4 g/mol [127]) into account, one can calculate the amount of oxygen atoms per cm³ to be 4.13e+22 and 6.19e+22, respectively. Thus, for a certain amount of oxygen atoms, their required volume decreases if they change their binding partners from Zn to Ga. Around 9 nm of ZnO must be dissipated during the formation of the 6 nm Ga₂O₃. Assuming, that all the Zn atoms, which are then bound to Se diffuse into the CIGSe absorber (5.77 g/cm³ and 336,29 g/mol for Ga/(Ga+In)=0.3 [128]) and distribute uniformly in this layer, the Zn concentration would be around 0.3 at.% within the 2.8 μm thick CIGSe layer. The effect of the Zn concentration on the electrical device properties are studied in Sec. 5.2.3.

The diffusion constant of Zn in CIGSe (without NaF precursor) can be approximated by fitting Eq. 1.18 to the Zn profile close to the ZnO in Fig. 5.14 to $D_{Zn,CIGSe} \approx 1e-12 \text{ cm}^2/s$, similar to the $1.3e-12 \text{ cm}^2/s$ reported for Zn diffusion via Cu-sites in the literature [129]. It should be noted, that the Zn distribution is not completely independent of the native chalcopyrite defect distribution, mainly V_{Cu} and In_{Cu} or Ga_{Cu} [46]. This is especially pronounced in the Zn profile of the CGSe samples, since the Zn signal increases towards the CGSe surface, away from the source, the interface to ZnO. Interestingly, the Zn concentration within the CGSe/NaF sample has a sudden increase at a sputter depth of 1.3 μm. It should be noted, that in these nominally pure CGSe samples, In was observed as an impurity, shown in Fig. 5.10. Further it can be seen, that the Zn profile correlates with the Na profile and anti-correlates with the In profile.

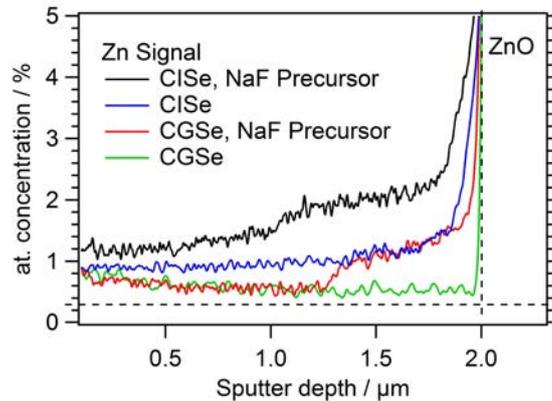


Figure 5.14: GDOES depth profiles of the Zn signal in different chalcopyrites deposited at 520°C on ZnO. Calibrated with the XRF data, which gives approximate values for the Zn concentration in the bulk. The Zn concentration in the bulk is strongly enhanced if sodium is present during the chalcopyrite growth. In the CIGSe/ZnO stacks the Zn signal in the bulk is within the noise level. The estimated value of 0.3% is marked with the dashed line.

5.1.6 Discussion

The results of Sec. 5.1 are discussed in this section.

- **CIGSe vs. CGSe:** CIGSe deposited at 520°C on top of ZnO leads to the formation of a 30 nm thick InO_x layer. In CGSe/ZnO stacks, an approximately 10 nm thick GaO_x layer formed under the same experimental conditions. The reason for the difference in the oxide thickness may originate from a higher reaction rate of CIGSe with ZnO, but this is unlikely, since the two layers are separated the moment the first closed layer of the interfacial oxide layer has formed. Thus the diffusion rates of In/Ga and O through the interfacial oxide layer must determine the growth rate of the layer. Since GaO_x has a smaller lattice parameter than InO_x [130], the diffusion constant of O is supposed to be smaller, which could explain the difference of the interfacial oxide layer thickness for the CIGSe/ZnO and the CGSe/ZnO stack.
- **Temperature dependence:** The chemical composition of the interfacial oxide layer was shown to depend on the CIGSe deposition temperature. At 420°C the interfacial oxide layer consists of all elements in similar concentration, with a thickness of approximately 3 nm. At 520°C mainly GaO_x forms at the interface and the formation of CuO_x is suppressed. However, the GaO_x layer has impurities of In and Cu between 3-5 at.%, as known from XPS measurements. The layer thickness was determined to be around 6 nm from HR-TEM images.

Interestingly, the thermodynamic calculations in Sec. 1.2 did not predict the formation of CuO_x at any temperature, since the enthalpy of formation is lower than for ZnO. Thus at 420°C the system is limited by the reaction kinetics, possibly limited due to the relatively low ionic mobility at 420°C and has therefore not reached its energetic minimum. It appears that the oxidation process occurs during the high

temperature deposition step in stage 2, when Cu, In and Ga are present at the interface to ZnO. At the interface an anion exchange of Se and O leads to the oxidation of Cu, In and Ga.

When the temperature is raised, the Ga ions gain sufficient mobility, which lowers the kinetic limitation and the Cu-O and the In-O bonds are replaced with the energetically favoured Ga-O bonds. After the formation of the first GaO_x monolayers, the growth should be limited by the diffusion rates of the different elements through this initial layer. The ionic size of In³⁺ is 0.81 Å and 0.77 Å for Cu¹⁺, both larger than to 0.62 Å for Ga³⁺ [131]. This indicates a lower diffusivity of In and Cu ions compared to Ga ions through the GaO_x layer, which also explains the low concentration of Cu and In within the 6 nm thick GaO_x layer.

For a temperature as high as 550 °C, an increased concentration of Cu was again found to be bound to oxygen at the interface. Most likely this is due to the increased diffusion of Cu into the GaO_x, which was still low at 520 °C. The higher diffusivity of Cu compared to In is due to the smaller ionic radius and the weaker covalent bond of Cu-Se compared to the In-Se bond within CIGSe [41].

- **Impurities within GaO_x:** XPS interface analysis showed that the GaO_x layer has large impurities of In, Zn, Cu and Se in the range of some at.% points. XPS results suggest that the layer is anion poor. The influence of these impurities on the electronic properties will be studied in the next chapter.
- **Influence of Na:** It was shown that NaF precursors lead to an increased oxidation of Ga or In and that the Na preferably accumulates within the interfacial oxide layer. No further oxidation at the interface was observed for the samples post treated with NaF, during which the sample is heated to 300 °C for only 10 minutes. Still, it was found, that Na increasingly accumulates within the interfacial oxide layer, with increasing temperature during the post treatment.

Thus it can be concluded, that the presence of sodium acts catalytic on the oxidation process. But the oxidation process is negligible at low temperatures applied for a short time, as for the NaF PDT. The catalytic effect is unlikely to be induced by an increased diffusion rate of Ga and O, since sodium is known to reduce the mobility of Ga [124]. It is more likely to be induced by a reduction of the Zn-O bonding strength at the interface between ZnO and the interfacial oxide layer. This could be triggered by the strong ionicity of the Na-O bond, which reduces the ionicity and with it the bonding strength of a neighbouring the Zn-O bond, similar as argued in [132] for surface reactions.

Thus, depending on the time and the temperature, the presence of sodium within the GaO_x could lead to an increase of the net density of acceptor states in two ways, first by reducing the amount of V_O donor states within the GaO_x, secondly by introducing acceptor states due to Na_{Ga} states.

- **Zn diffusion:** It was shown that Zn, which is set free from the ZnO layer during the interface reaction, diffuses into the chalcopyrite bulk and that the concentration of Zn depends on the thickness of the interfacial oxide layer. Due to the enhanced formation of an interfacial oxide layer in the ZnO/CISe system, the Zn concentration within CISe devices was estimated to be up to 2 at.% points. Within CGSe layers a lower Zn concentration between 0.5 at.% and 1 at.% was found. The interfacial oxide layer in the studied CIGSe devices was only 6 nm, from which an average Zn concentration of 0.3 at.% was calculated.

The resulting Zn depth profile within the chalcopyrite bulk was shown not to be distributed as expected from a single diffusion process as shown in Fig. 1.4. Rather it is found, that the Zn distribution correlates with the Na distribution, especially clearly observable in the CGSe layer. Na is iso-electronic to Cu, and Cu sites are commonly believed to be the preferred occupation sites for Na in the literature (see Sec. 1.3.1). Due to the strong off-stoichiometry of the CGSe layer, with a Cu/(In+Ga) ratio of approximately 0.9, it can be assumed that the Cu vacancies are not saturated by Na, Zn or In impurities. Thus, the observed correlation with Na implies that Zn, in the region where it follows the shape of the Na profile, preferably sits on V_{Cu} sites. The observed anti-correlation of the Zn profile with the In impurity profile in the CGSe layers supports this assumption. Further away from the ZnO interface, where the Zn concentration is lower, no correlation to the In and Na profiles is found any more and it may be, that Zn is equally distributed between the native defects. Thus, this analysis indicates a preferable V_{Cu} site occupation of Zn atoms at high Zn concentrations. Zn can be both donor and acceptor in CIGSe (see Sec. 1.3.1), depending on whether it sits on a Ga/In site or a Cu site. The impact of the Zn impurities on the device is studied in Sec. 5.2.3.

In summary, all samples studied in this section showed an inter-facial oxide layer, which developed during the high temperature process step in stage 2 and 3. The composition was shown to depend on the chemical composition of the chalcopyrite at the interface, the chalcopyrite deposition temperature and the NaF treatment. These three dependencies can be used to engineer the interface. The next section will study the influence of the different interfacial oxide layers on the device performance.

5.2 Device Properties

In this section the information obtained on the structural and chemical properties of the ZnO/CIGSe interface will be correlated with the electrical properties of ZnO/CIGSe/Au devices. First, the experimental results will be presented, which will then be discussed jointly at the end of this chapter.

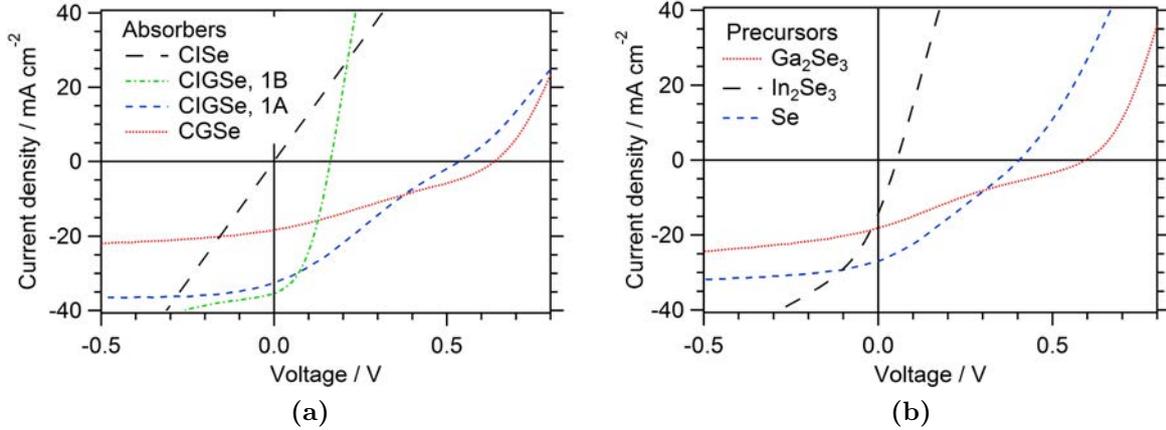


Figure 5.15: **a)** $J - V$ curve of devices with CISe, CIGSe and CGSe deposited on ZnO. The deposition process of the CIGSe, 1B started with stage 1B (In-Se) instead of 1A (Ga-Se). **b)** $J - V$ curve of devices with the same CIGSe absorbers, but different 50 nm thick annealed precursor layers.

5.2.1 Interface composition

The elemental composition of the interfacial oxide was shown in the Sec. 5.1 to be dependent on the Ga content of the CIGSe layer deposited on top of the ZnO. Thick layers of InO_x were formed for CISe whereas thinner GaO_x layers were formed for CIGSe and CGSe. Fig. 5.15a shows the $J - V$ curves of devices with CISe, CGSe or CIGSe absorber deposited on ZnO at 525 °C.

The CISe devices were observed to be generally shunted. Lock-in thermography measurement showed, that no local shunts were present and thus it can be concluded that the InO_x interfacial layer forms an ohmic contact between ZnO and CISe. Hot-point probe was performed on the bare absorber, which showed that the CISe layer remains p -type even with a few at.% contamination of Zn.

Devices made from CGSe do show a rectifying behaviour, but a relative low V_{OC} of 640 mV, compared to CGSe devices in substrate configuration whose V_{OC} is around 900 mV. The $J - V$ -curve shows a kink in the fourth quadrant, indicating some kind of barrier for the charge carriers.

A similar kink can be observed for the CIGSe devices, when the deposition process has started with stage 1A, which is Ga-Se. The V_{OC} drops significantly if the deposition process starts with stage 1B, which is In-Se. This results in an In rich chemical composition around the interface to ZnO, possibly leading to the formation of $(\text{In,Ga})\text{O}_x$ instead of GaO_x .

To prove that the difference in the rectifying behaviour is due to the interfacial oxide layer and not due to the different Ga content in the chalcopyrite bulk layers, thin buffer layers were deposited prior to the absorber deposition. To analyse the chemical com-

position of the buffer layers with XPS, first 10 nm thick In_2Se_3 and Ga_2Se_3 layers were deposited onto ZnO substrates and annealed in vacuum at the CIGSe process temperature of 520 °C. The XPS measurements on these samples showed the presence of $(\text{In,Ga})\text{O}_x$ for the In_2Se_3 precursor and GaO_x for the Ga_2Se_3 precursor. $(\text{In,Ga})\text{O}_x$ instead of pure InO_x must have formed due to Ga contaminations from the deposition chamber. Knowing the interface reaction to occur for these very thin buffer layers, now 50 nm of In_2Se_3 , Ga_2Se_3 and Se were deposited onto fresh ZnO substrates and annealed at the CIGSe process temperature of 520 °C. On top of these buffer layers, CIGSe was deposited, resulting in a nominally identical bulk chemical composition but different interfacial chemical composition. The CIGSe process was standard as described in Sec. 2.1. The results are shown in Fig. 5.15b. The Se precursor slightly reduces the V_{OC} and the J_{SC} compared to the standard device in Fig. 5.15a. The device with the In_2Se_3 precursor, which was shown to be transformed to $(\text{In,Ga})\text{O}_x$, was not shunted, as the pure CIGSe samples without any Ga content. But it showed a low parallel resistance and V_{OC} of only 55 mV. The sample with the pre annealed Ga_2Se_3 precursor was shown to form pure GaO_x at the interface. This leads to an increased V_{OC} but a decreased J_{SC} compared to the CIGSe sample without precursor and very similar to the $J - V$ curve of the CGSe sample. Clearly indicating that the chemical composition at the interface is the determining factor for the shape of the $J - V$ curve.

5.2.2 Deposition temperature

Fig. 5.16a shows the $J - V$ curves of samples with absorber layers deposited at different temperatures. For temperatures below 500 °C a low open circuit voltage in combination with a high short circuit current is usually observed. The open circuit voltage increases for samples made at 525 °C, while the maximum photo-current remains the same. If the deposition temperature is further increased, the voltage does not increase further but the fill factor and the maximum photo-current decreases. For the sample fabricated at 560 °C the light and the dark $J - V$ curve cross over in the first quadrant. The optimum CIGSe deposition temperature was found to be around 525 °C.

The corresponding $C - V$ curves are shown in Fig. 5.16b. All samples show a strong increase of the capacitance when positively biased. Standard substrate devices generally have capacitances below 50 nF/cm² at positive bias, while the capacitance of superstrate devices go up to 600 nF/cm². It should be noted, that the dashed lines in Fig. 5.16b indicate that in this bias range the capacitance of the space charge could not be measured correctly due to the high DC current present at positive voltages for the 475 °C sample, and due to the degradation of the back contact (see Sec. 6.2), which leads to a second diode in opposite direction, for the 560 °C sample. It should be noted, that the capacitance at negative voltage bias is increased for the 560 °C sample compared to the other two. The plot of the charge carrier density over the width of the space charge region, derived with Eq. 2.10 and shown in the inset of Fig. 5.16b, shows a constant value in the absorber bulk for all three samples. It is around 6×10^{14} cm³ for the samples made at 475 °C and 525 °C and slightly lower at around 4×10^{14} cm³ for the 560 °C sample.

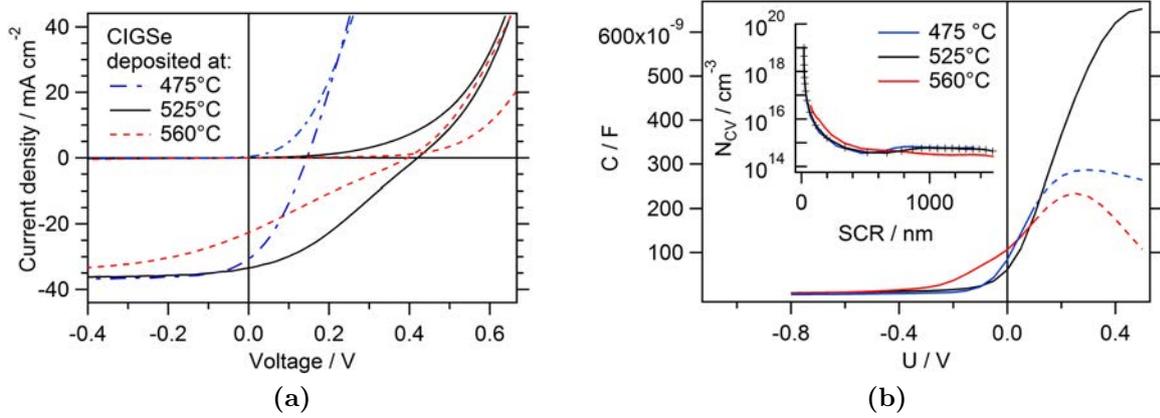


Figure 5.16: a) dark and illuminated $J - V$ curves of devices fabricated at different temperatures. b) $C - V$ curve of the same devices recorded at 293 K and 1 kHz. The dashed lines indicate that the capacitance does not correspond to the space charge region due to secondary effects.

For the rest of this work, devices fabricated at the optimum temperature of 525 °C are studied, if not mentioned other wise.

Charge carrier diffusion length To understand the distorted shape of the $J - V$ curve in Fig. 5.16, it is useful to study the voltage and depth dependent charge carrier collection within the device. EQE, EBIC and $C - V$ are used in this work to study the charge carrier collection. Fig. 5.17a shows the EBIC image of the 525 °C device, recorded at short circuit condition. The EBIC image shows the local current generation along a cross section, randomly broken from a finished device. There is a slight dependence on the grain structure, but a clear trend can be observed towards lower currents for increasing distances from the CIGSe/ZnO interface. Fig. 5.17b shows a representative profile over a single absorber grain. By fitting the Eq. 2.19 to the profile, it is possible to extract the electron diffusion length within CIGSe, L_n , and the space charge region width, x_{SCR} (see 2.4.4). The result for x_{SCR} between 0 - 200 nm, whereas 0 nm lead to the best fit. The result for L_n within the CIGSe is between 800 nm and 900 nm, with the best fit for 880 nm. As a comparison to the EBIC results, the effective collection length, which is x_{SCR} plus L_n , can be extracted from the slope of the EQE spectra by Eq. 2.16. The wavelengths range between 550 - 800 nm was used, since this is the range less influenced by the shape of the ZnO absorption spectrum. Fig. 5.18 shows the EQE spectra for three different bias voltages. The effective collection length extracted from the EQE spectrum recorded at short circuit condition is 1000 nm. With $x_{SCR} = 220$ nm as derived with Eq. 2.7 from the $C - V$ measurement, the diffusion length L_n becomes 780 nm. At a voltage bias of -250 mV, the EQE increases in the near infrared region and the calculated diffusion length remains at around 800 nm and x_{SCR} increases to 800 nm according to the $C - V$ results. For the positive voltage bias, the diffusion lengths is calculated to 200 nm and the x_{SCR}

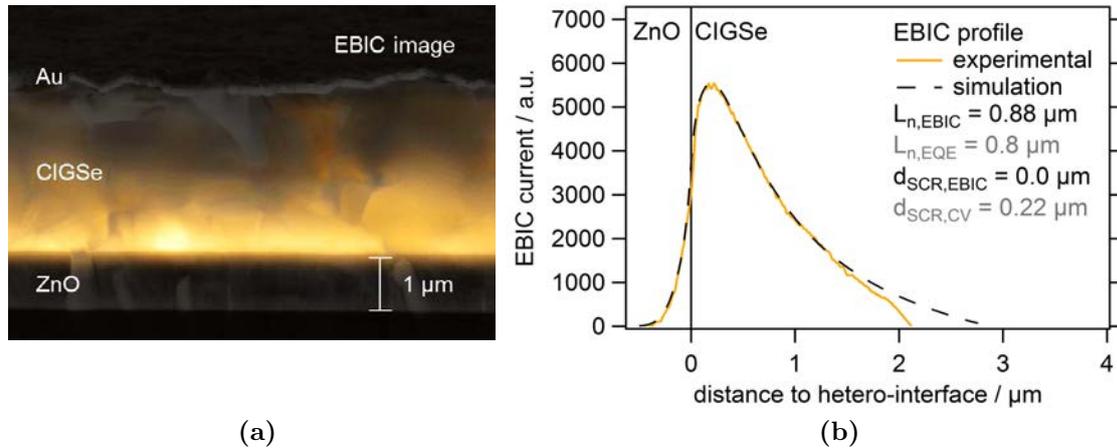


Figure 5.17: **a)** Electron Beam Induced Current (EBIC) image of the 525 °C device, recorded from a cross-section, and superimposed with the SEM image. A probe current of 63 pA was measured at no high current mode (Gemini column, extractor voltage at 10 kV, extractor at 260 μm). **b)** Extracted line profile together with a fit of Eq. 2.19 performed with EBIC-view.

25 nm. Further, the whole EQE spectrum is lowered to smaller values even in the short wavelength region, indicating a barrier present at forward bias.

5.2.3 Diffusion of Zn

During the reaction of CIGSe with ZnO, not only GaO_x is formed but also free Zn atoms, which diffuse into the absorber as shown in Fig. 5.14. It was estimated that the Zn concentration in the best superstrate devices with a 6 nm thick GaO_x layer is around 0.3 at.%. As it is discussed in Sec. 1.3.1, this can lead to an increase in acceptor states or donor states depending on whether the Zn atoms preferably sit on Cu or In/Ga sites. The effect

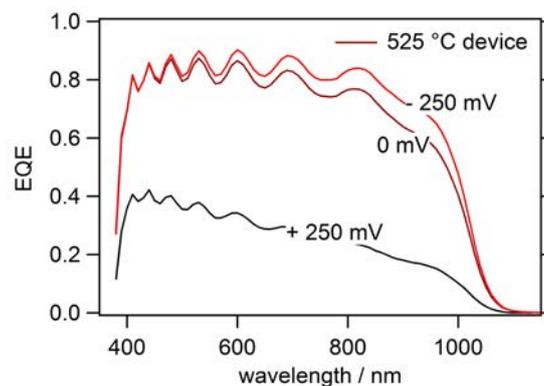


Figure 5.18: EQE spectra of the 525 °C device at different voltage biases. The electron diffusion length within the CIGSe is calculated to be around 800 nm.

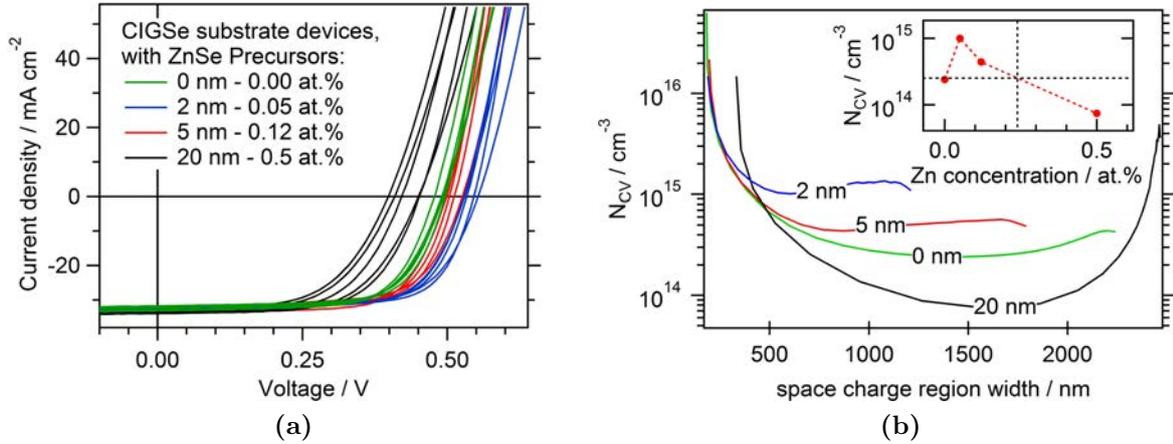


Figure 5.19: **a)** IV curves of solar cells fabricated in substrate configuration ZnO/CdS/CIGSe/ZnSe/Mo with different thickness values of ZnSe layers added as precursor onto the Mo back contact for controlled Zn contamination. 2 nm ZnSe correspond to 0.05 at.% in the CIGSe bulk. The Zn doping of the CIGSe layer has strong influence on the V_{OC} . **b)** Corresponding $C - V$ curves, recorded at 1 kHz and 293 K. The Zn doping of the CIGSe layer increases the CIGSe doping level for low concentrations and decreases it for high Zn concentrations. The inset shows the relation between charge carrier density and Zn concentration.

of Zn on CIGSe is now studied in substrate devices to enable the exact control of the Zn content. To do this ZnSe buffer layers were deposited on Molybdenum substrates and on top of that the CIGSe absorber, followed by CdS and ZnO. The CIGSe was deposited by a three stage process at 520 °C, designed to lead to a flat Ga profile with $Ga/(In+Ga)=0.27$ and $Cu/(In+Ga)=0.87$. 2, 5 and 20 nm thick ZnSe layers were deposited by thermal evaporation at 300 °C. Due to the similar mass density and average atomic mass of ZnSe and CIGSe 20 nm of ZnSe can be calculated to correspond to 0.5 at.% of Zn within the 2 μ m thick CIGSe layer. The 2 nm and 5 nm layers correspond to 0.05 at.% and 0.12 at.%.

The $J - V$ measurements of the Zn doped devices are shown in Fig. 5.19a. The main influence of the Zn doping can be observed on the open circuit voltage. The V_{OC} is highest for the samples with low Zn concentration of 0.05 at.%, around 520 mV, whereas the V_{OC} values of the devices without Zn are lower at around 500 mV. The cells with a high Zn concentration of 0.5 at.% show the lowest V_{OC} , around 425 mV. Corresponding to this, the effective charge carrier density, derived from $C - V$ measurements, follows the same trend, as shown in Fig. 5.19b. The sample with 0.05 at.% has a high doping density of $1e+15$ cm⁻³ compared to $1e+14$ cm⁻³ for the sample with 0.5 at.% Zn. To analyse whether the Zn doping has an effect only on the charge carrier density or also on the charge carrier lifetime, the V_{OC} of representative samples is plotted in Fig. 5.20b over a logarithmic scale of the charge carrier density. For a constant charge carrier lifetime of the different samples, the measurements points should fall on a single line, since the V_{OC} is proportional to the exponential of the charge carrier density (see Eq. 2.2). The

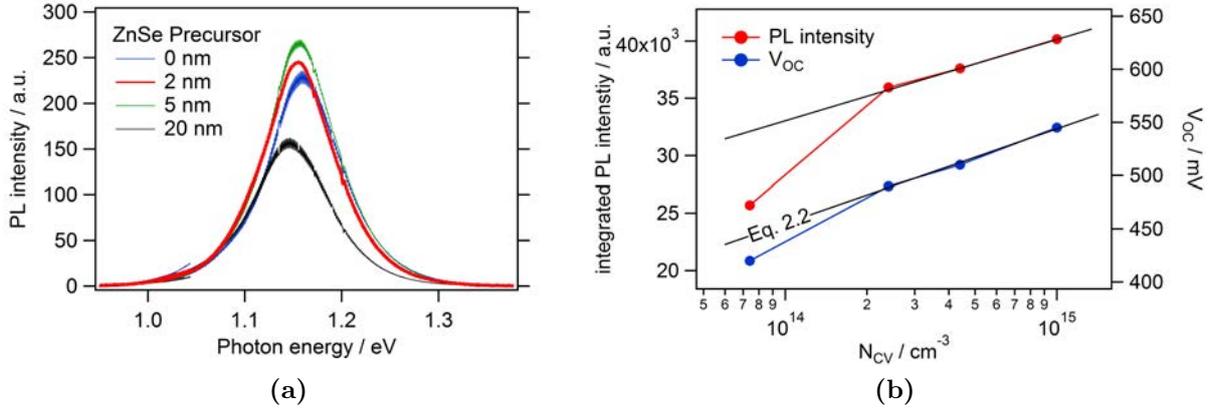


Figure 5.20: **a)** Photo-luminescence spectra of CIGSe/ZnSe/Mo stacks with different ZnSe thickness values **b)** Comparison of the V_{OC} and the PL intensity with the doping density taken from Fig. 5.19. The sample with high Zn concentration deviates from the $V_{OC}/I_{PL} \propto \ln(N_{CV})$ line (black), obtained from Eq. 2.2 for a constant electron lifetime, due to increased non-radiative recombination.

three samples with 0, 0.05 and 0.12 at.% Zn lie indeed on a single line. The sample with 0.5 at.% Zn (20 nm ZnSe) does deviate though. This could originate from a lower bulk lifetime of this sample or from increased interface recombination.

In order to eliminate the influence of the interface recombination at the CdS interface, the recombination in bare absorbers was studied by photo-luminescence (PL) spectroscopy. The resulting PL spectra of the bare absorbers are shown in Fig. 5.20a. The PL intensity is, similar to the V_{OC} , proportional to the charge carrier density and can also be lowered by non-radiative recombination in the bulk or at the interface. The integrated intensity of these peaks is plotted in Fig. 5.20b. The same trend as for the V_{OC} can be observed for the PL intensity. The sample with 0.5 at.% Zn shows stronger non-radiative recombination loss.

It should be further noted, that very similar results were obtained with CIGSe absorbers on ZnS buffer layers of different thickness, confirming that Zn leads to detrimental deep donor states if present in high concentrations. For the absorber studied here ($Ga/(In+Ga)=0.27$ and $Cu/(In+Ga)=0.87$) the threshold concentration was found to be approximately 0.25 at.% of Zn.

5.2.4 Influence of alkalis

Alkali treatments are usually performed on CIGSe absorbers to enhance the p -type doping density. Sodium and Potassium are the most common choices of the alkali metals. Often they are supplied via out-diffusion from alkali containing glass substrates through the Mo layer. Since, in contrary to the Mo back contacts, ZnO layers are good diffusion barriers for alkalis, the alkali dopants have to be supplied externally prior to the absorber

deposition by a precursor or after the CIGSe deposition by a post deposition treatment (PDT). In order to suppress the formation of NaOH and KOH, the fluoride compounds of the alkali metals, NaF and KF, are used. No negative influence of the fluorine atoms on the CIGSe absorber has been shown so far [133].

Sodium Fluoride Treatment (NaF) Fig. 5.21a shows the $J-V$ curves of superstrate devices with different NaF treatments. During the post deposition treatments, 10 nm of NaF were deposited on the CIGSe surface at a given temperature and annealed for 10 minutes at the same temperature. For the NaF precursor, 10 nm of NaF were deposited onto the ZnO prior to the CIGSe deposition. The absorber was deposited via a modified three-stage process starting with the co-evaporation of Ga-Se, as described in Sec. 1.3.1.

The NaF PDT at 100 °C leads to a $J-V$ curve that is similar to the $J-V$ curve of an untreated device (see Fig. 5.16) but with a decreased series resistance (details in Sec. 6.1). The J_{SC} is 32 mA/cm², the V_{OC} 620 mV and the FF 28% leading to an overall η of 5.5%. If the temperature during the NaF PDT is increased to 300 °C, η increases to 10.1%, due to an increase in J_{SC} to 37 mA/cm², V_{OC} to 680 mV, and FF to 40%. The FF drops if the NaF PDT is performed at temperatures higher than 300 °C. At 400 °C the FF drops to 20%, while the V_{OC} remains 680 mV and the J_{SC} drops to 25 mA/cm². The device with NaF deposited as a precursor prior to the CIGSe deposition has a low J_{SC} of 5 mA/cm² in combination with a high V_{OC} of 740 mV and the injection current is pushed towards higher voltages. This indicates a strong electrical barrier in the device.

Fig. 5.21b shows the corresponding $C-V$ curves of the post-treated devices. The NaF PDT at 100 °C leads to no change in the $C-V$ curve compared to the untreated device shown in Fig. 5.16b. If the capacitance is interpreted as a space charge capacitance, then the high capacitance at positive bias translates with Eq. 2.7 into a 20 nm thick space charge region. The free charge carrier density can be calculated with Eq. 2.10 to be $6e+14$ cm⁻³ in the CIGSe bulk. The NaF PDT at 300 °C leads to $C-V$ curves with high capacitances for the whole studied voltage range. Leading to a SCR width of 10 nm at 0.5 V and 30 nm at -0.5 V. The NaF PDT at 400 °C further increases the capacitance, lowering the SCR width even further.

Beside the deposition temperature, the diffusion velocity of sodium into the absorber may be important. In order to slow down the diffusion of sodium during the annealing time a 10 nm thick Mo layer was deposited prior to the NaF PDT on the absorber surface. This leads to a different sodium depth profile compared to the same NaF PDT performed without Mo layer, shown in Fig. 5.22. The sodium concentration within the CIGSe bulk reaches a similar value for both samples, but close to the CIGSe/ZnO interface and especially at the interface, the concentration is considerably smaller for the sample with the Mo layer on the CIGSe surface.

The $J-V$ and $C-V$ curves of these two devices are compared to the untreated device in Fig. 5.23a and b. Compared to the untreated device both show high J_{SC} values of 37 mA/cm². However, the V_{OC} of the Mo diffusion barrier device is lowered from 670 mV to 570 mV. Nevertheless η is increased to 10.8% due to an increase of the FF from 40%

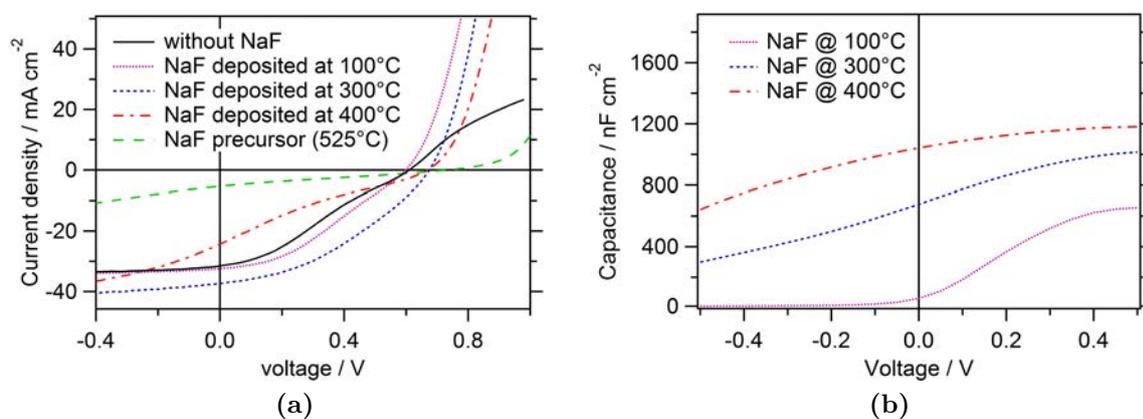


Figure 5.21: a) $J - V$ curves of devices with CIGSe deposited at 525 °C and with NaF PDT at performed at different temperatures b) $C - V$ curves of the same devices recorded at 293 K and 1 kHz.

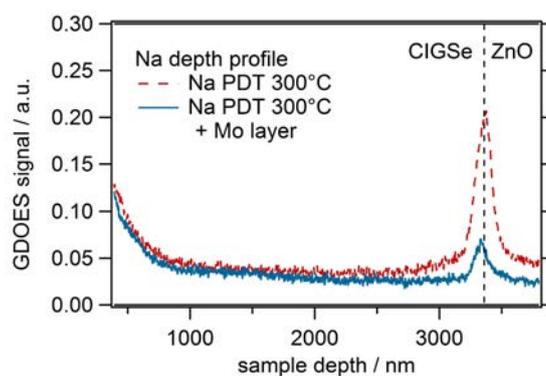


Figure 5.22: GDOES depth profile of Na in CIGSe/ZnO stacks, with and without the deposition of a 10 nm thick Mo diffusion barrier prior to the NaF PDT.

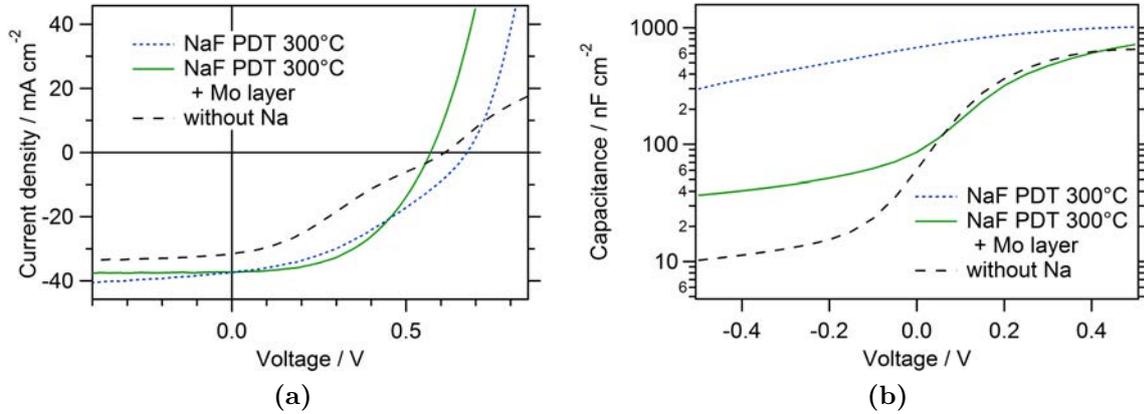


Figure 5.23: a) $J - V$ curves of devices with CIGSe deposited at 525°C and with NaF PDT at performed at different temperatures b) $C - V$ curves of the same devices recorded at 293K and 1kHz .

to 51%. Employing Eq. 2.10 the charge carrier density can be calculated from the $C - V$ curves in Fig. 5.23b. The Na PDT increased the charge carrier density in the CIGSe bulk of the device with the Mo layer from $5\text{e}+14\text{ cm}^{-3}$ to $9\text{e}+15\text{ cm}^{-3}$, and for the device without Mo layer to $5\text{e}+16\text{ cm}^{-3}$.

In forward voltage bias, the capacitance of the Mo layer device is unchanged compared to the sample without sodium. This indicates that the strong increase as observed for the NaF treated sample without the Mo layer is most likely due to the presence of sodium at the interface between CIGSe and ZnO.

Potassium Fluoride Post Deposition Treatment (KF PDT) The effect of potassium in superstrate devices is shown in Fig. 5.24. All samples were from the same deposition run performed at 525°C . The post deposition treatment was performed at nominally 300°C . The deposition of potassium fluoride was performed at a high deposition rate of several nm/s and lead to a slight kink in the fourth quadrant of the $J - V$ curve. Very similar to the $J - V$ curve of the sample with the NaF PDT in Fig. 5.21. Not shown here, but KF provided as a precursor leads to an even more pronounced kink within the $J - V$ curve. This indicates, that potassium, similar to sodium, induces an electron barrier at the hetero-interface.

The pure NaF treatment performed in this sample variation was done with a very low NaF deposition rate of $1\text{ nm}/\text{min}$ for 10 minutes. This leads to a $J - V$ curve similar to the one in Fig. 5.21 where the sodium diffusion rate was lowered by the additional Mo layer.

The third sample became the same NaF PDT for only 5 minutes, followed by a KF PDT with $1\text{ nm}/\text{min}$ also for 5 minutes. Compared to the pure NaF treatment, the combined NaF and KF treatment leads to an increase of the V_{OC} from 525mV to 580mV . η of this device was 11.0%, one of the highest measured efficiencies obtained

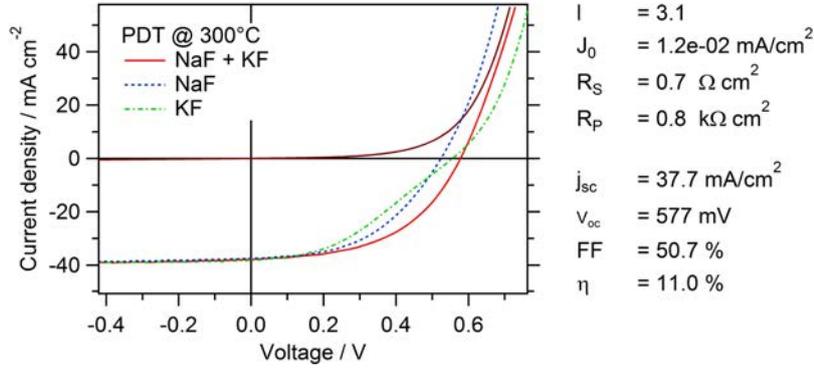


Figure 5.24: $J - V$ curves of devices with absorbers from the same deposition run performed at 525 °C, but with different PDTs performed at 300 °C. The device with the NaF PDT followed by the KF PDT reached the highest efficiency of 11%. The $J - V$ characteristics were obtained from a one-diode model fit of the illuminated and dark curve (I , J_0 , R_s , R_p). The minimum band gap was 1.15 eV (GDOES) and the $\text{Cu}/(\text{In}+\text{Ga}) = 0.89$.

in this work, indicating further potential of improvements by fine tuning the alkali post deposition.

In summary, as shown before, low-rate deposition of sodium leads to an improved fill factor above 50 %. The combination of NaF and KF treatment was shown to improve the V_{OC} similar as observed in substrate devices.

5.2.5 Discussion

V_{OC} and the chemical interface composition

In Sec. 5.2.1 it was shown, that the V_{OC} of the superstrate device depends critically on the chemical composition of the CIGSe absorber directly at the interface to the ZnO. Pure CIGSe absorbers were completely shunted due to the non-rectifying contact between the InO_x layer, which formed at the interface to ZnO. Pure CGSe layers and CIGSe layers with an annealed Ga_2Se_3 precursor, were shown to have the highest V_{OC} values, but low J_{SC} values. In CIGSe devices, the V_{OC} was shown to be dependent on how much In was present in the GaO_x layer, which depend on whether or not the deposition process was started with In-Se or whether or not a In_2Se_3 precursor was used.

As it will be shown later (in Fig. 8.4), the band gap of amorphous InGaO_x varies by 1 eV depending on the In content, being the lowest for pure InO_x . According to the common anion rule, which was found to be a good approximation for most oxide semiconductors [134], the valence band maximum is similar for all oxides but the conduction band varies with varying cation species. Thus, the CBM of InO_x is expected to be around 1 eV lower than the CBM of GaO_x . As discussed already in Sec. 4 this should lead to a conduction band cliff at the interface for InO_x , and a conduction band spike for GaO_x . How this difference can influence the V_{OC} in a standard device was shown in Fig. 3.1. For highly

defective interfaces, the V_{OC} drops almost linearly with the height of the conduction band cliff, which lowers the activation energy for the interface recombination. Therefore it can be assumed that larger concentrations of In within the interfacial oxide layer limit the V_{OC} due to a high interface recombination velocity and a cliff like conduction band alignment.

A Cu poor surface, as often observed in substrate devices, could reduce the interface recombination losses as discussed in Sec. 3.1. The XPS measurement presented in Sec. 5.1 indicate such a Cu-poor surface, but the error of the quantitative determination is large and TEM-EDX as well as GDOES measurements could not confirm this. In the following no Cu poor surface is assumed for the superstrate devices.

In summary, In contaminations within the GaO_x layer reduce the V_{OC} due to an increasingly cliff like conduction band offset.

FF and the Cu impurities within the GaO_x

All superstrate samples studied in this Section, showed a strong capacitance increase together with a decrease of the extracted photo-current at forward biases, leading to a low FF and a low η . This behaviour was found in Sec. 3.2 to be characteristic for devices with a high acceptor density around the buffer layer. In this model the capacitance is interpreted as a pure SCR capacitance. The capacitances measured at forward bias would translate into a d_{SCR} of just 10-20 nm. With 5-10 nm of the SCR within the p -type region. This is approximately the thickness of the GaO_x layer, seen in the TEM images in Fig. 5.6. Such a short space charge region would limit the collection efficiency of the photo-current and could explain the observed low fill factors of the $J - V$ curves. However, such a small space charge region would require a high density of acceptor states at the hetero-junction.

These acceptor states may originate from O_{Se} within CIGSe, induced by an oxidation of the CIGSe at the interface to ZnO or to the interfacial GaO_x layer. The O_{Se} acceptor state is reported to be 120-140 meV above the VBM of CIGSe [?]. Thermodynamic calculations predict that the oxide binaries will segregate during the oxidation process [47], limiting the O_{Se} acceptor states to the interface between CIGSe and the oxide.

Another origin of interfacial acceptor states can be found from the XPS measurements presented in Sec. 5.1.3. They show that the interfacial oxide layer consists of GaO_x with large amounts of impurities of all other elements. Se and In are iso-electronic to O and Ga respectively, and the defects Se_O and In_{Ga} are charge neutral. They only lower the band gap of the GaO_x layer [135] [136] [137], which was shown in Sec. 3.2 to have negligible influence on the capacitance. However, Cu impurities are known to lead to acceptor states within TCOs, as shown in Sec. 1.3.2. No literature exists on the doping effect of Cu_{Ga} states within Ga_2O_3 , but it is known that at high concentrations of Cu, the p -type TCO $CuGaO_2$ forms [138], in which the valence band is composed of the Cu 3d orbitals and shifted by around 1 eV compared to Ga_2O_3 . Also Zn is believed to form shallow Zn_{Ga} acceptor states within Ga_2O_3 [139], but for the amorphous $GaZnO$ an increasing n -type doping was observed for low Zn concentrations compared to the pure Ga_2O_3 [140], with

the Zn 4s orbitals forming the extended conduction band [141]. Therefore, it is not clear whether or not Zn leads to acceptor states within amorphous GaO_x . Experiments shown in Sec. 8.3 indicate that Zn does not lead to *p*-type doping.

The XPS results further indicate, that the GaO_x is oxygen poor which would induce cation interstitials like Ga_i or anion vacancies like V_O , both leading to deep donor states [142]. The maximum charge carrier concentration reported previously for O-poor Ga_2O_3 is 10^{18} cm^{-3} [143], which could be compensated by the large amount of impurities from Cu .

In summary, Cu_{Ga} or O_{Se} are assumed to lead to acceptor states in the bulk at the interface to GaO_x , which in turn lowers the fill factor and limits the device efficiency.

V_{OC} , FF and the deposition temperature

Besides the chemical composition of the interfacial layer, the deposition temperature of the CIGSe absorber was shown to have a strong influence on the V_{OC} as well as on the FF. In Sec. 5.2.2 it was shown that absorbers deposited at 475°C lead to low V_{OC} values below 200 mV and absorbers deposited at 560°C lead to low fill factors.

The change of the interfacial composition with the deposition temperature was shown in Fig. 5.1.3. For a deposition temperature as low as 420°C , it was found that an approximately 2-3 nm thick interfacial oxide layer forms, with equal contribution of Cu, In and Ga on the cation sites. Taking the arguments of the discussions above into account, this material combination should lead to a *p*-type oxide, due to the Cu content, with an electron affinity higher than that of CIGSe, due to the In content. This resembles the situation illustrated in Fig. 3.6e for $\chi > 4.5 \text{ eV}$. In this model the low V_{OC} is induced by the increased interface recombination due to the combination of high acceptor density and high electron affinity of the buffer layer. Further, this situation could lead to an increased tunnel current from the ZnO conduction band to the CIGSe valence band, if the buffer layer is sufficiently thin.

Once the temperature is increased to around 520°C , the GDOES and the XPS measurements showed, that the contribution from Cu and In to the interfacial oxide layer is strongly reduced and mainly GaO_x is present at the interface. The low concentration of In possibly leads to a reduced conduction band cliff at the hetero-interface, which leads to a reduced interface recombination and an increased V_{OC} . The Cu impurities induce a high density of acceptor states in the interfacial oxide layer leading to the observed low FF.

At temperatures above the optimum deposition temperature, at 560°C , the GaO_x thickness increases further to approximately 9-10 nm. This is expected, as the Ga diffusion through the GaO_x layer is enhanced at higher temperature, which was argued to be the limitation of the interface reaction. The increased temperature also increases the diffusion of the other elements and since Cu is the most mobile specie, an enhanced diffusion of Cu into the GaO_x is expected and is indeed observed for these high temperatures. Cu is supposed to induce acceptor states in the oxide. And according to the

simulations shown in Fig. 3.4c an increase of the acceptor density leads to an increased electron barrier and an increased capacitance, resulting in a kink in the fourth quadrant of the $J - V$ curve. The increased kink together with the increased capacitance was indeed observed experimentally.

In summary, it is proposed that In reduces the activation energy for the interface recombination and Cu induces acceptor states within the interfacial oxide layer. The concentration of In and Cu within the GaO_x layer is the lowest at an optimum deposition temperature of around 520°C , leading to the highest device efficiencies.

Zn doping

As discussed in Sec. 1.3.1, Zn is amphoteric as it can act as a donor or acceptor depending on which lattice site it occupies. Zn_{In} leads to acceptor states, whereas Zn_{Cu} leads to donor states. Due to the overall Cu-poor composition of the CIGSe absorbers it is likely that in this case Zn prefers the Zn_{Cu} states and thus reduces the p -type doping of the CIGSe layer. This is in accordance with the observation in Sec. 5.1.5, which showed that the Zn depth profile in CIGSe correlates with the Na depth profile, whenever the Zn concentration is high. The controlled doping experiments in Sec. 5.2.3 show indeed, that for a high Zn concentration of 0.5 at.% the measured p -type doping is reduced when compared to the Zn-free device. For low concentrations, below approximately 0.25 at.%, the measured p -type doping in the CIGSe bulk was observed to increase. Thus, in the CIGSe studied here, the Zn atoms appear to preferably occupy the In/Ga sites for low concentrations.

Further it was found from the $J - V$ and PL measurements that the electron lifetime, and thus the recombination losses, are unchanged for Zn concentrations below 0.25 at.% compared to undoped devices. But the recombination losses were increased for the sample with 0.5 at.% Zn concentration. Since both measurements are sensitive to bulk and interface recombination, both recombination channels could be increased due to the high Zn contamination. But, as it was shown in Sec. 3, that the interface recombination generally decreases when the bulk doping density decreases compared to that of the buffer layer. Further, the increased recombination loss was observed for two totally different interfaces. Thus it is more likely that bulk recombination has increased. Simulations with SCAPS show that a donor level has to be located 200 - 300 meV below the CBM in order to increase the recombination loss and lead to a V_{OC} reduction of the observed 20 mV without reducing the J_{SC} . Thus it can be concluded, that Zn_{Cu} states are effective recombination centres and that Zn preferably occupies the V_{Cu} states at concentrations above approximately 0.25 at.%. Zn_{In} is a shallow acceptor which does not act as a recombination centre and is dominant for Zn concentration below approximately 0.25 at.%.

In Sec. 5.1.5, the Zn concentration for the sample prepared at 525°C was approximated to be 0.3 at.%. This is slightly above the critical threshold concentration for Zn atoms (see inset of Fig. 5.19b). Thus it seems that the amount of Zn present due to the formation of a 6 nm thick GaO_x layer, could have a small negative influence on the charge carrier density and charge carrier lifetime. It should have a more noticeable negative

influence on the samples deposited at higher temperatures than 525 °C, which have thicker GaO_x layers and therefore higher Zn concentration within the absorber. This could explain the lower charge carrier density and the lower V_{OC} of the sample deposited at 560 °C.

In summary, Zn doping is only detrimental for the device when present at concentrations above 0.25 %. The Zn concentration for the optimum deposition temperature is estimated to be only slightly above this value, and should therefore define no major limitation for the state-of-the-art device efficiency.

Alkali treatment

As in substrate devices, it is found that Na and K doping increases the device efficiency, in this case from around 5-6 % absolute to 10-11 %. The difference to substrate devices is, that the alkali treatment increases the V_{OC} and the J_{SC} , as shown in Fig. 5.21a. An increase of the V_{OC} is the expected result of a NaF treatment due to the increased p -type doping generally observed due to the reduction of In_{Cu} states by Na. The increase of J_{SC} is more unusual. This could originate from a Fermi-level pinning as illustrated in the simulations shown in Fig. 3.4a. But the measured capacitance is not increased at negative biases, which excludes such an option. Further, back contact recombination may play a role, but the strong Ga gradient present in the films should not allow any back contact recombination. Thus SRH bulk recombination is the most likely option. A cause of an increased bulk recombination rate are the Zn_{Cu} donor states within the CIGSe. Further, Na is known to preferably occupy Cu sites and the discussion of Fig. 5.10 revealed that Na and Zn share similar sites for high concentrations of Zn as in the samples studied here. Thus, the presence of Na could reduce the amount of Zn_{Cu} states, similar as it is argued for the In_{Cu} states in the literature (Sec. 1.3.1). This would increase the p -type doping and reduce the bulk recombination rate.

The effect of the NaF post-deposition is found to be highly dependent on the Na deposition rate and temperature. A temperature of 300 °C is required to achieve sufficient Na diffusion into the CIGSe. At higher temperatures the fill factor and short circuit current become strongly reduced. In the previous Section it was shown, that Na tends to accumulate at the hetero-interface the more the higher the PDT temperature is set. Here the increasing Na content is correlated with an increasing capacitance. And an increasing capacitance with a decreasing charge extraction was shown in Sec. 3.2 to originate from an increase in acceptor states at the hetero-junction. The Na profile follows the shape of the Ga/Se ratio, which indicates, that Na accumulates within the interfacial GaO_x layer and not at the interface between CIGSe and GaO_x. Thus it appears that Na introduces acceptor states within the GaO_x layer.

In Sec. 1.3.2 it was already mentioned that Na_{Zn} leads to acceptor states within the ZnO. No literature data is available for Ga₂O₃, but Na, like Cu, does introduce acceptor states to most n -type oxides. Therefore it is likely that the high concentration of sodium at the interface leads to a high concentration of acceptor states, which would narrow

the space charge region to ZnO and lead to the observed increase in the capacitance in Fig. 5.21b.

It was found, that the concentration of Na at the hetero-interface can be reduced by depositing a thin layer of Mo prior to the NaF PDT. The Mo layer is supposed to reduce the diffusion rate of Na into the CIGSe, which leads to the beneficial depth profile, with a low Na concentration at the hetero-interface while remaining a high Na concentration in the bulk (Fig. 5.22 with Fig. 5.23). This leads indeed to the best fill factor. Reducing the NaF rate to 1 nm/min was shown to have a very similar effect.

Thus it can be concluded from the correlation of the depth profiles, the $C - V$ curves and the $J - V$ curves, that sodium leads to acceptor states within the GaO_x layer, which lifts up the conduction band at the interface and therefore introduces an electron barrier and lowers the extraction of the photo-current.

Potassium was tested as an alternative for sodium. Potassium leads to very good PCEs in substrate devices, where it is supposed, that the potassium atoms sit on Cu sites and are replaced by Cd atoms during the CdS deposition [144]. This leads to a n -type doping of the surface and a reduced interface recombination. This mechanism is unlikely to occur in superstrate devices though, since the deposition sequence is switched, first Zn diffuses into the CIGSe and then K is introduced. And indeed, the use of potassium as a precursor or supplied with a PDT, both lead to similar results as the use of sodium only. A kink developed in the fourth quadrant, strongly pronounced for the precursor and less pronounced for the PDT. However, the combination of a 5 minute NaF PDT followed by a 5 minute KF PDT lead to a PCE of 11%, compared to 9% for the pure NaF treatment from the same deposition run. A speculative explanation could be, that K atoms replace Cu atoms close to the hetero-interface, which increase the band gap and reduce the interface recombination as observed in substrate devices [145]. In other deposition runs an efficiency of 11% were also achieved for pure NaF treatments. Thus, the KF treatment appears to be beneficial, but this is not yet sufficiently reproduced and secured.

In summary, The NaF and KF PDT lead to a strong increase in efficiency due an increased bulk p -type doping and a reduced bulk recombination rate. Both effects presumably originate from the reduction of Zn_{Cu} and In_{Cu} states by Na_{Cu} or K_{Cu} . On the other hand, the efficiency can be reduced by the alkalis if their concentration at the hetero-interface is too high. They are argued to induce Na_{Ga} or K_{Ga} acceptor states within the GaO_x which leads to an electron barrier and a reduced fill factor.

5.3 Comparison with buffer free ZnO/CIGSe substrate devices

To get the full picture of the ZnO/CIGSe interface, this section studies substrate devices without CdS buffer layer. Several publications exist on ZnO/CIGSe/Mo devices with

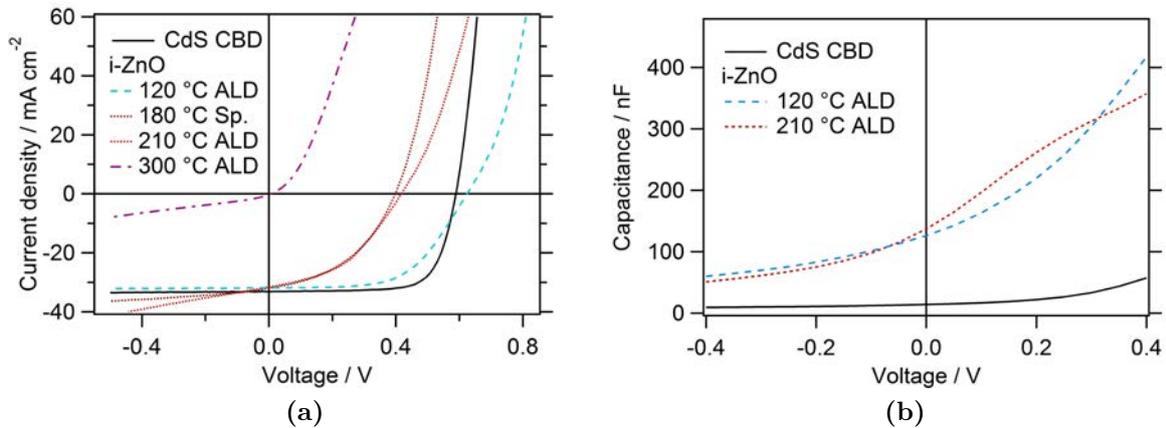


Figure 5.25: a) $J - V$ curves and b) $C - V$ curve of substrate devices with CdS or i-ZnO buffer. The i-ZnO was deposited via ALD at different deposition temperatures.

reported efficiencies around 12 % [146] [147]. The influence of the substrate temperature during the i-ZnO deposition onto the CIGSe is studied here. The i-ZnO is deposited via ALD and sputtering, the AZO window layer has been sputtered identically for all devices.

Fig. 5.25a shows the $J - V$ curves of substrate devices with i-ZnO buffer layers and one CdS reference device under illumination. The CIGSe absorber were deposited with a standard three-stage process at 560 °C and a resulting Cu/(Ga+In) ratio of 0.85 and Ga/(Ga+In) ratio of 0.3. The CdS reference device exhibits the highest PCE of 14.2 %. The ALD deposited i-ZnO at 120 °C leads to the second most efficient device, but the FF is considerably lower compared to the CdS device. If the deposition temperature is increased to 210 °C, the V_{OC} starts decreasing from 590 mV to 410 mV. The same result, with only slightly lower V_{OC} , was obtained from an i-ZnO layer sputtered at 180 °C. If the deposition temperature of the ALD i-ZnO is further increased to 300 °C, the V_{OC} and PCE is reduced to zero, indicating very high interface recombination currents. The corresponding $C - V$ curves are shown in Fig. 5.25b for the two devices deposited at 120 °C and 210 °C. The CdS free devices show a strongly increased capacitance at all applied voltage biases compared to the CdS device.

Discussion The data presented here shows that both deposition methods, ALD and sputtering, lead to very similar device characteristics, whereas the deposition temperature has an unexpected drastic influence. The low FF together with the increased capacitance compared to the CdS device indicate that interfacial acceptor states are again responsible for the lower FF, similar as it was found for the superstrate devices (Sec. 5.2.5). It was however, not possible to find a device model which fits both the $J - V$ and $C - V$ curves sufficiently well. This is likely to be caused by the rough p/n -heterojunction in substrate devices compared to superstrate devices, which reduces the straight forward correlation of the $C - V$ and the $J - V$ curves and cannot be represented by a one dimensional device model any more.

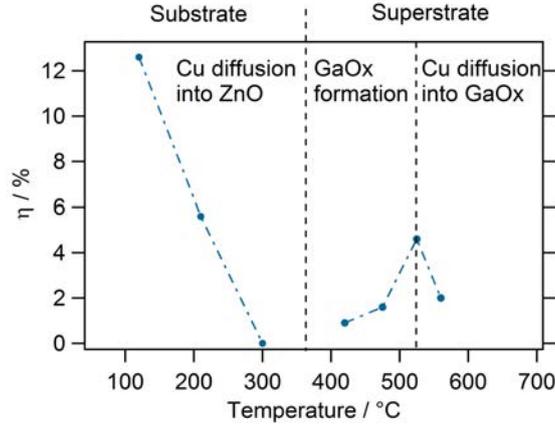


Figure 5.26: PCE and V_{OC} for ZnO/CIGSe devices in substrate and superstrate configuration displayed versus the maximum temperature exposure of the ZnO/CIGSe interface during fabrication. For substrate devices this is the ZnO deposition temperature, for superstrate devices the CIGSe deposition temperature. The formation of GaO_x in superstrate devices is assumed to lead to the increase of PCE and V_{OC} until it starts limiting the current at 560 °C.

Regarding the nature of the acceptor states, it is argued in [148], that the acceptor states are induced by the $V_{Se}-V_{Cu}$ defect complex [48] within the CIGSe. This is unlikely, since it can't explain the temperature dependence. It could however be assumed that the acceptor states are induced by copper and sodium diffusion into the ZnO layer or by O_{Se} states at the CIGSe/ZnO interface. It should be noted that the very same trend was observed in Cu_2O/ZnO devices [149], which supports the assumption of Cu being responsible for the acceptor states within ZnO. This interpretation would lead to a conclusive model for the CIGSe/ZnO interface, in which the quality of the p/n junction mainly depends on the temperature load that it experiences during fabrication.

The dependence of the power conversion efficiency on the temperature exposure of the ZnO/CIGSe interface is shown in Fig. 5.26 for both configurations, substrate and superstrate. η and V_{OC} appear to be correlated with the deposition temperature. It seems a plausible assumption, that the acceptor type defect density from diffusion of copper and sodium, increases with increasing temperature. The resulting increased interface defect density reduces η and V_{OC} due to interface recombination, until, at a certain temperature, a thin layer of GaO_x forms at the interface. The GaO_x layer reduces the electron density at the interface which reduces the interface recombination, leading again to an increase of η for increasing temperature. At a certain temperature the Cu diffusion into the GaO_x occurs, which again increases the acceptor density at the interface and decreases the electron collection and with it also η .

In summary, it is proposed that the diffusion of Cu and/or Na into ZnO or GaO_x is a general problem independent of the device configuration. The acceptor states induced by Cu/Na reduce electron collection and increase interface recombination.

5.4 Summary: ZnO/CIGSe interface

1. **GaO_x formation:** At the interface between CIGSe and ZnO a thin layer of an $(\text{In}_y, \text{Ga}_{1-y})(\text{O}_z, \text{Se}_{1-z})_x$ alloy forms with strong Cu and Zn contaminations. The best efficiencies were reached for low In and Cu concentrations. The Ga rich alloys were named GaO_x for simplicity. The In and Cu content was shown to depend on the CIGSe deposition process. For low In content the process should start with Ga-Se evaporation and the deposition temperature should be above 500 °C. For low Cu content the deposition temperature should be below 550 °C. The optimum temperature was found to be 525 °C.
2. **Influence of sodium:** Under certain conditions, Na was shown to be able to considerably increase the device efficiency. In case it is present during CIGSe growth it catalyses the GaO_x formation. If supplied by a post-deposition it tends to accumulate at the CIGSe/GaO_x interface without further catalysing the GaO_x formation. However, when present in high concentration at the hetero-interface it induces an electron barrier and leads to the reversible degradation of the device. Very low-rate NaF post-deposition or diffusion through a thin Mo layer was shown to reduce the Na concentration at the interface while keeping the concentration high within the bulk.
3. **Influence of Zn diffusion:** Zn contamination was found to be proportional to the thickness of the interfacial oxide layer. A systematic doping study suggests that for low concentrations below 0.25 % the acceptor state $\text{Zn}_{\text{In/Ga}}$ is dominant, whereas for higher concentrations the Zn_{Cu} donor state is dominant. GDOES depth profiles supports this assumption. The $\text{Zn}_{\text{In/Ga}}$ acceptor state appears to be shallow, whereas the Zn_{Cu} donor state leads to a reduction of the charge carrier lifetime. In the superstrate device fabricated at the optimum temperature the Zn concentration was estimated to be 0.3 %. This is likely to reduce the device efficiency, especially at CIGSe deposition temperature above 525 °C. The electron diffusion length was measured to be around 800 nm.

Chapter 6

Back contact and degradation

The back contact is the second critical interface in CIGSe devices. In superstrate devices Au is generally used as the back contact material, which was shown to form an ohmic contact to CIGSe. But so far no reports exist on the influence of potentially Cu poor interfaces or on the degradation of the Au/CIGSe interface. Further no highly reflective and cheap alternative back contact has been reported to date. This chapter will study these objects as well as the degradation of the p/n -junction, which will be linked to the electro-migration of sodium and copper in the electric field of the p/n -junction.

6.1 The back contact

The quality of the back contact depends on the difference of the metal and the CIGSe work function. In substrate devices the formation of MoSe_x at the interface between Molybdenum and CIGSe establishes an ohmic contact to CIGSe [150]. In superstrate devices the back contact is deposited at room temperature on top of the CIGSe layer. The formation of MoSe_x does not occur and as an alternative to molybdenum, gold is generally used as the back contact, which has one of the highest work functions (5.3 eV) of all metals. Still a Cu-poor back surface of the CIGSe could increase the CIGSe work function leading to a non-ohmic contact.

Cu-poor CIGSe surface The CIGSe growth process, in which only Ga-Se is deposited during the last stage, may induce a Cu-poor back surface. This would lower the VBM and increase the work function at the interface to Au (see Sec.1.3.1). To pronounce this effect, the last stage of the growth process, during which no copper is offered, was extended. Instead of 200 nm as in the standard process, 400 nm of Ga-Se are deposited at the end of the process.

Fig.6.1 shows the $J - V$ curves of a device with a normal third stage and with an extended third stage, both without external sodium supply. The $J - V$ curve of the standard device shows an increased series resistance starting at 800 mV. This occurs if the back contact is not perfectly ohmic due to different work functions of the metal and

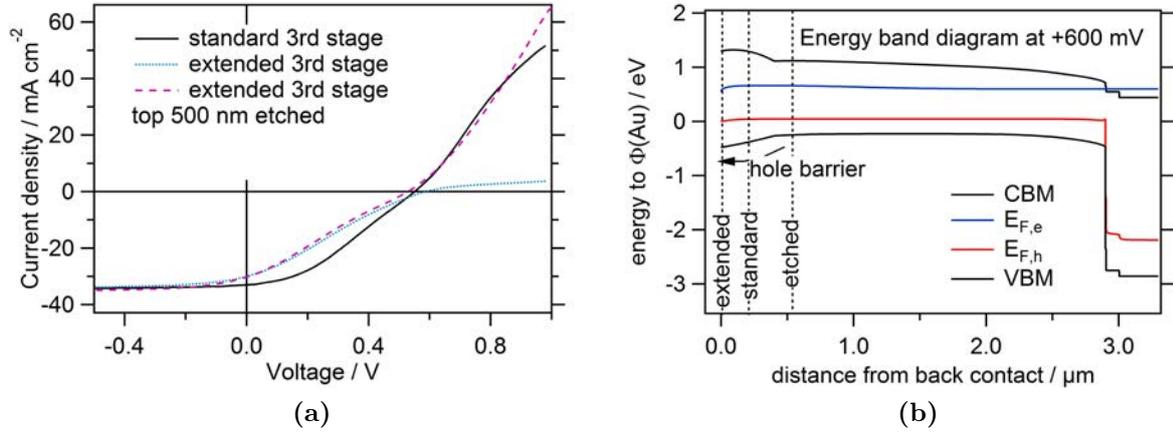


Figure 6.1: a) $J - V$ curves of ZnO/CIGSe/Au stacks with a standard 3rd stage, an extended 3rd stage and an etched surface. The CIGSe is deposited at 525 °C. b) Corresponding schematic energy band diagram at a forward bias of 600 mV. The Ga-rich back surface becomes increasingly Cu-poor the thicker it gets, increasing the hole barrier. The dashed bars indicate the different back surfaces of the three samples studied here.

the CIGSe. The resulting space charge region results in a slight barrier for the hole extraction which increases the series resistance, a so-called roll-over.

The $J - V$ curves of the device with the extended third stage shows a reduced fill factor and a stronger roll-over starting from V_{OC} . The strong roll-over observed for this device can be explained by an increased hole barrier at the back contact due to the Cu-poor back surface. To prove this, the top 500 nm from the surface was etched by using bromine-methanol, to remove the Cu-poor surface completely. The $J - V$ curve of the etched sample is also shown in Fig. 6.1. The fill factor remains unchanged, therefore this should be a bulk or ZnO/CIGSe interface effect. However, the roll-over disappears completely.

This proves that if the surface becomes Cu-poor, its work function increases, and a roll-over at forward bias develops. If the Cu-poor surface is etched, the back contact with Au becomes ohmic. The slight roll-over often observed for the standard superstrate devices therefore indicate a slight Cu deficiency at the back surface.

To measure the barrier between Au and CIGSe a test structure glass/Mo/CIGSe/Au was fabricated with the CIGSe deposited by the standard modified three-stage process at 525 °C. As shown in the previous paragraph the surface of the CIGSe absorber is slightly Cu-poor, which is the origin of the hole barrier. As it can be seen in Fig. 6.2a the $J - V$ curve shows a roll-over in forward bias and in reverse bias. To quantify the barrier heights the $J - V$ curve was simulated with SCAPS (Fig. 6.2 a). From $C - V$ measurements this was calculated to be $1e+15 \text{ cm}^{-3}$ and therefore the work function within the CIGSe is 5.4 eV. The barrier between Mo and CIGSe, which is the difference in their work function, is calculated to be 140 meV. From this the work function of MoSe_x is determined to be 5.26 eV. The barrier at the CIGSe/Au interface is 160 meV. Assuming a maximum work

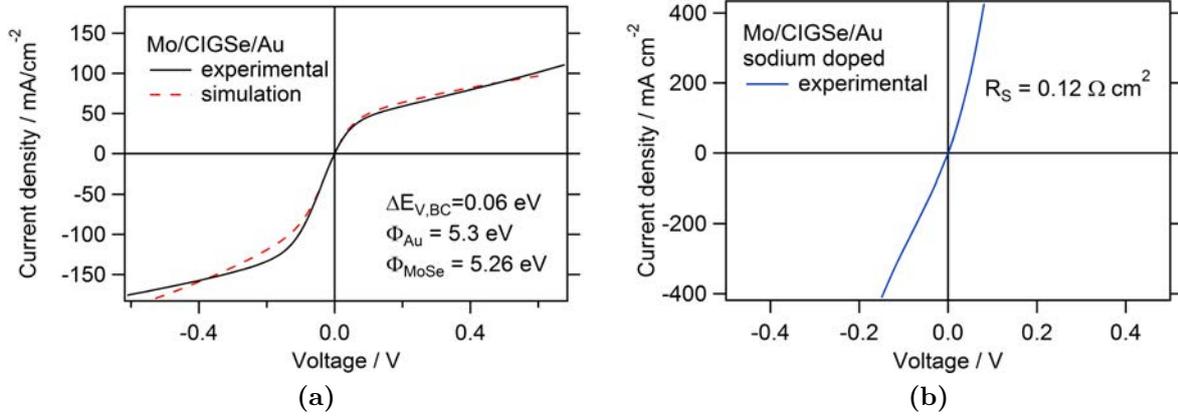


Figure 6.2: a) $J - V$ curves of Mo/CIGSe/Au stack. The CIGSe is deposited at 525°C on top of the Mo layer. The Au is deposited at around 50°C . The dotted red line shows the simulation result from which the work functions of MoSe_x and the lowering of the VBM at the back surface, $E_{V,BC}$, are derived. The work function of Au is assumed to be 5.3 eV b) Mo/CIGSe/Au stack with CIGSe doped with sodium.

function of 5.3 eV for Au, the lowering of the CIGSe VBM at the interface to Au has to be at least 60 meV .

Once sodium is supplied to the CIGSe absorber via PDT the p -type doping increases, which increases the thermionic emission over the barrier at the contacts, leading to an ohmic contact between CIGSe with MoSe_x and Au, despite the Cu-poor surface. The $J - V$ curve is shown in Fig. 6.2b. The series resistance derived from this $J - V$ curve is $0.12\ \Omega/\text{cm}^2$.

6.2 Degradation

Most CIGSe devices are known to increase their performance on a short time scale due to light soaking effects [151], which is assumed to change the hole population of the defects [22], but also degrade on a long time scale due to back contact or TCO degradation [152]. The stability of CIGSe superstrate devices has not been studied so far. In this section the degradation of the p/n junction and of the Au back contact are studied. It is shown, that the back contact degradation can be hindered by storage in an inert atmosphere, whereas the degradation of the p/n junction is independent of the atmosphere during storage.

Degradation of the back contact

Degradation of the back contact can be a problem in the superstrate configuration, since the back contact is in contact with humidity and oxygen from air, which may lead to oxidation. Further, the metal may diffuse into the CIGSe absorber. Fig. 6.3 shows the degradation of the series resistance R_s with and without external sodium supply. Without

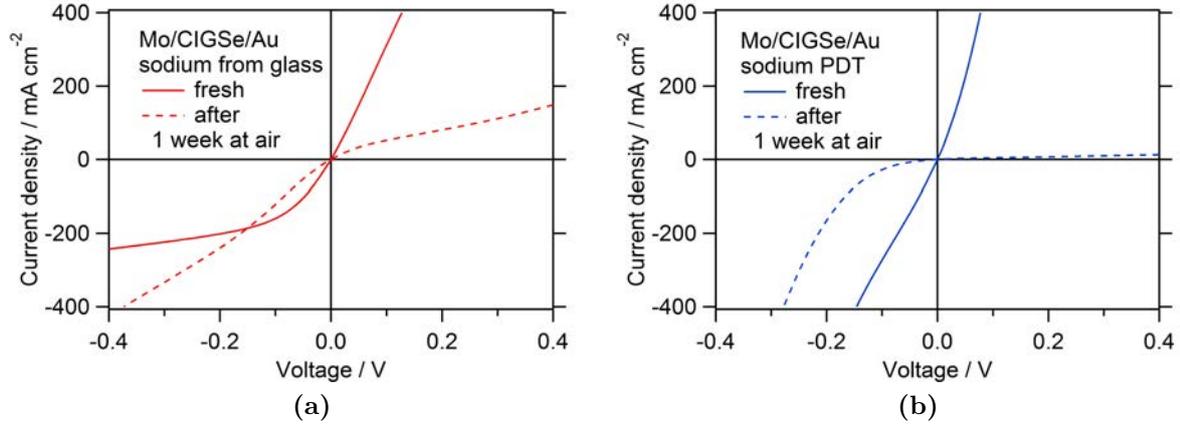


Figure 6.3: a) Dark $J - V$ curves of a Mo/CIGSe/Au stack. The CIGSe is deposited at 525 °C on top of the Mo layer. The dotted red line shows the $J - V$ curve of the same device after 1 week storage in air. b) same as a), but the CIGSe absorber has received a standard NaF PDT (see Sec. 2.1).

external sodium supply and freshly prepared devices the contact to Au is ohmic, which is seen from the linear slope of the $J - V$ curve at forward bias. This was previously shown to be the case as long as the surface is not Cu poor. After storage in air for one week, a roll-over in forward bias developed, which tells that the contact to Au has degraded. In case sodium is present, the contacts to Au and Mo are both ohmic for the fresh device, after 1 week of storage the contact to Au degraded as well. However, the sodium doped device shows a much stronger increase of the R_s up to a value of 36 Ωcm^2 compared to 3 Ωcm^2 for the non-doped device. This shows that sodium catalyses the degradation process.

GDOES measurements were done to reveal if the origin of degradation is due to an increasingly Cu-poor back surface, possibly induced by electro-migration of Cu. Fig. 6.4a shows the Cu/(In+Ga) and the Ga/Se ratio of three samples which received the absorber simultaneously in the same CIGSe deposition run. They were stored in nitrogen until the NaF PDT was performed. The time between the absorber deposition and the NaF PDT was different for each samples. After the NaF PDT 100 nm of Au was deposited and they were stored in air. The GDOES measurements of all three samples were done at the same day. The time between the GDOES measurement and the NaF treatment was 2 days, 3 days and 2 months.

The Cu/(In+Ga) ratio shows that the surface is indeed copper depleted for all three samples, but it is independent on the date of the NaF PDT and is therefore not the cause of degradation. The Ga/Se ratio however increases with increasing time difference between the PDT and the measurement. As shown in Sec. 5.1, the increased Ga/Se ratio is a sign for the formation of GaO_x at the Au/CIGSe interface. Only the sample which received the NaF treatment two days before the measurement did not show any sign of GaO_x formation. GaO_x has a large band gap of 4.8 eV and is therefore assumed to block

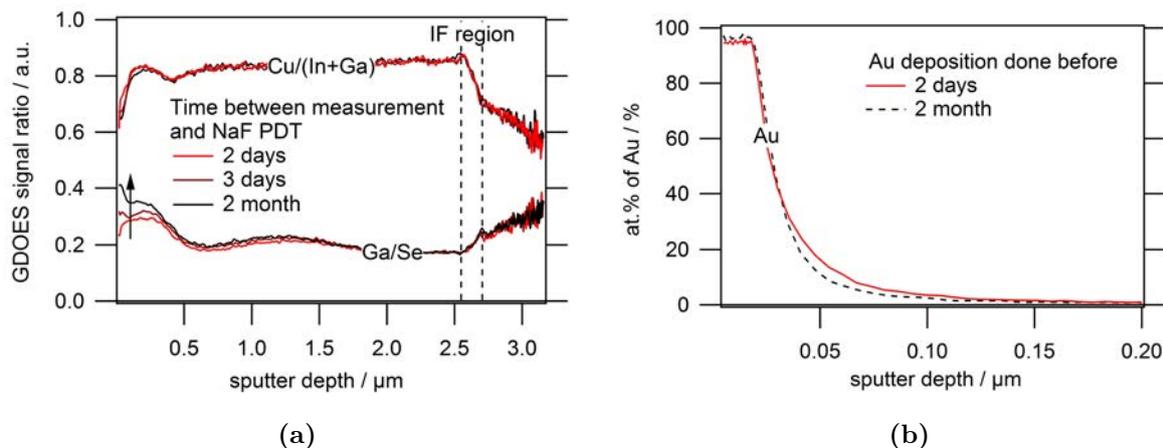


Figure 6.4: **a)** Ratios of the GDOES signals for a CIGSe layer deposited at 525°C . The time between the NaF PDT and the GDOES measurement was varied. **b)** Depth profile of the Au concentration. The tail is due to the sputter crater and not due to Au diffusion.

holes very efficiently. The results in Sec. 5.1 showed that sodium acts as a catalyzer for the oxidation of Ga at high temperatures. At high oxygen, gallium and sodium concentrations, this seems to occur even at room temperature.

The Au depth profile is shown in Fig. 6.4b. The shape of the profile does not originate from diffusion but from the sputter crater and surface roughness (see Sec. 2.5.3). No increased Au concentration within the CIGSe layer can be observed two month after the Au deposition compared to two days after the Au deposition.

Thus, the cause of the degradation of the series resistance can be found in the formation of GaO_x at the interface between CIGSe and Au. A high concentration of sodium at the interface catalysis the oxide formation. The deposition of a thicker layer of a metal, which sticks better to CIGSe than Au, may reduce the degradation of the back contact.

Degradation of the p/n junction

If sodium is supplied via PDT at temperatures around 300°C or above, an additional degradation pathway to the degradation of the back contact can be observed even if the device is stored in an inert atmosphere. Fig. 6.5a shows the $J - V$ curve of a sodium doped device after 3 days of storage in an inert atmosphere, without illumination and at open circuit condition. During this time the $J - V$ curve did not develop a roll-over, as observed for the back contact degradation, but a kink in the fourth quadrant. Further it can be observed, that the capacitance increases at all applied voltages.

The degradation process was found to be reversible, by applying a positive voltage to the device. Fig. 6.5a shows the $J - V$ and the $C - V$ curves of two solar cells from the same substrate, but one was stored at open circuit condition and one at forward bias of $+1\text{V}$, both in air. The biased solar cell developed no kink. However, the short circuit

Table 6.1: Quantitative results from XPS measurements shown in atomic % of all elements within a cleaved CIGSe/ZnO sample, post-treated with NaF, fresh and degraded. The samples were cleaved at the CIGSe/ZnO interface. Care is to be taken since the relative error of the atomic concentrations is between 50% and 60%. Still, the trends between the samples are qualitatively correct. The high concentration of Na and O are due to NaOH formation at the surface.

	ZnO side fresh	ZnO side degraded	CIGSe side fresh	CIGSe side degraded
Cu	1	1	13	11
In	2	2	24	26
Ga	27	30	12	10
Se	8	7	42	36
O	56	53	4	11
Zn	1	1	0	0
Na	6	5	4	11

current decreased, compared to the fresh device. Interestingly, the capacitance increases proportional to the loss in photo-current at each voltage. Once this cell is stored at open circuit condition for a few hours, the kink does develop as well. This indicates that the degradation process is triggered by the electric field at the p/n junction of the device (Fig. 1.1 shows the electric field).

XPS measurement were done on identically prepared fresh and degraded samples, cleaved at the CIGSe/ZnO interface. The results are shown in Tab. 6.1. The chemical composition of the CIGSe surface and the ZnO surface hardly changes during degradation. But the concentration of sodium and oxygen actually changes. During degradation over time, the sodium concentration within the GaO_x slightly decreased whereas it increased considerably in the CIGSe surface. The oxygen concentration follows the trend on both surfaces. It was shown earlier in Sec. 5.1.4, that the concentration of oxygen at the surface depends on the concentration of sodium due to the formation of NaOH. But nevertheless, the change in the sodium concentration indicates, that the sodium likely diffuses during degradation.

To see whether the applied voltage can have an influence on the Na distribution, GDOES measurements were performed before and after the application of +1 V forward bias to the device. The results are shown in Fig. 6.6a. Indeed the Na profile changed due to the applied voltage, which proves that electro-migration of Na within CIGSe is possible. The change is only visible at the back contact, where the concentration of Na is high.

The Na migrates deeper into the absorber during the application of the positive bias, which creates an electric field at the back contact as seen in Fig. 6.6b. This observed sodium migration at the back contact is assumed to have no impact on the device, as the exact doping profile at the back contact is not important for the device performance. But it shows that sodium in principle does migrate within the CIGSe in the presence of an

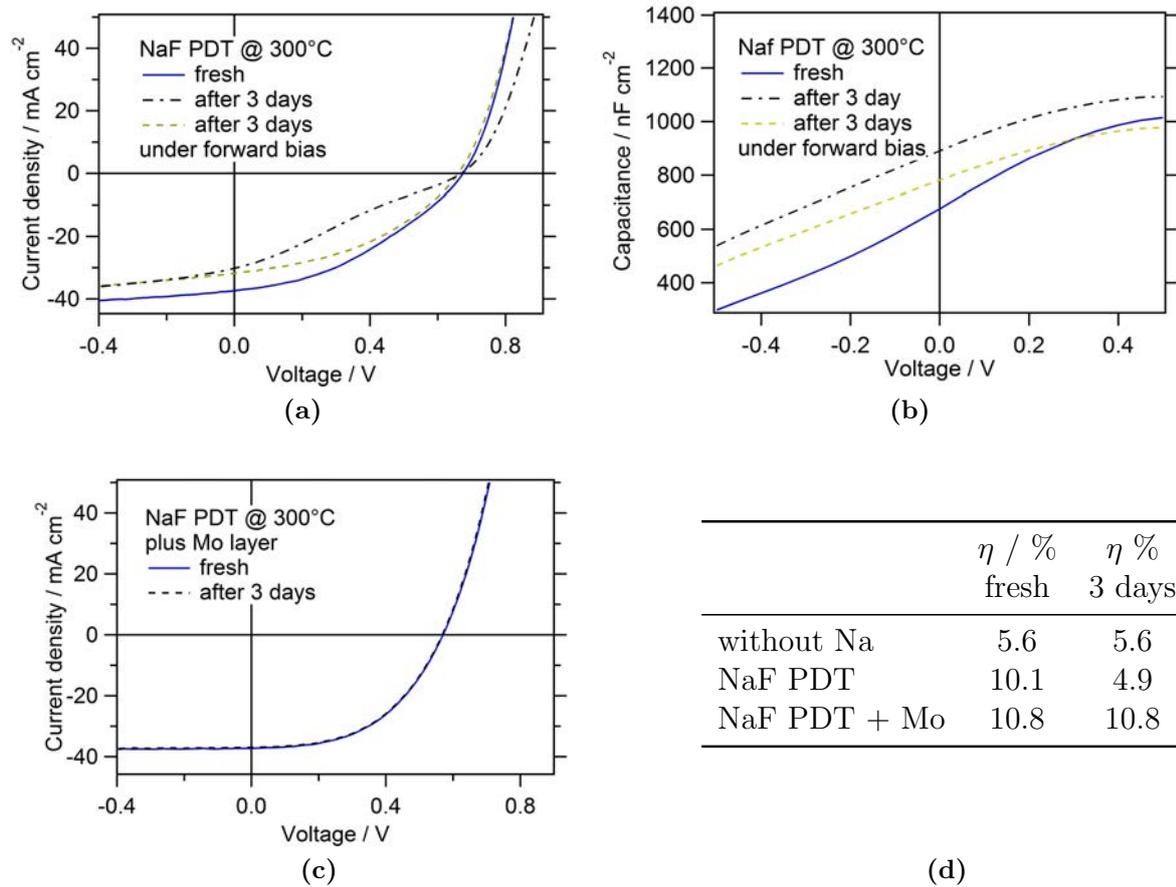


Figure 6.5: **a)** Effect of degradation and forward bias on the $J - V$ curves of a sample with a NaF post-deposition treatment at 300°C. The photo-current decreases over time independent of the storage condition, whereas the kink does not show up if the sample is stored under a forward bias voltage of +1 V. **b)** $C - V$ curves of the same devices recorded at 293 K and 1 kHz. **c)** $J - V$ curves of a sample with a NaF post-deposition treatment at 300°C and a Mo diffusion barrier, freshly prepared and after three days. **d)** Table of the device efficiencies when freshly prepared and when stored for 3 days in the dark, without voltage bias and in nitrogen atmosphere.

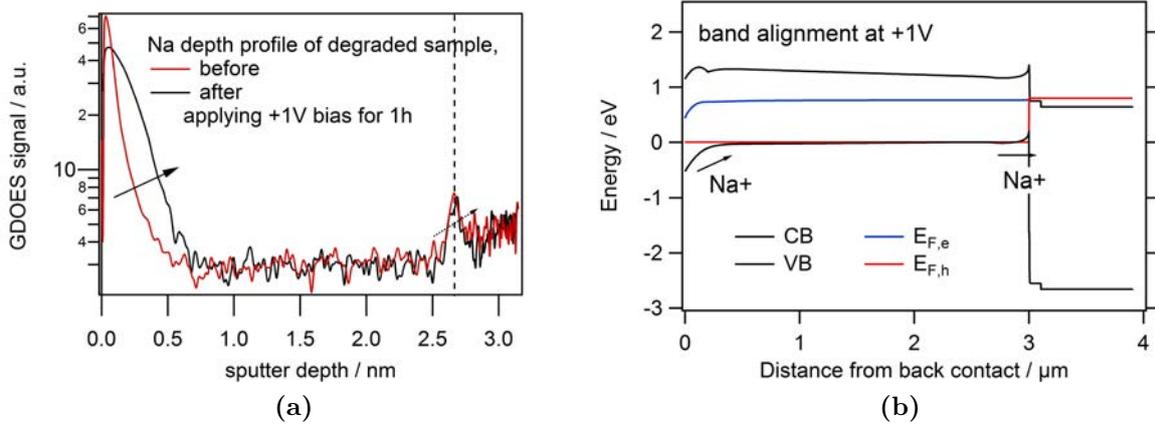


Figure 6.6: **a)** To prove the sodium electro-migration: Depth profile of sodium within the same sample before and after applying +1 V. The sample was fabricated by the standard superstrate CIGSe process with a NaF PDT. The back contact material was gold, which induces Schottky junction under forward bias. The electric field within this junction leads to the migration of sodium into the absorber. The degradation of the device probably occurs due to the sodium migration at the p/n -junction at 0 V. **b)** band diagram of a standard Au/CIGSe/ i -ZnO/Al:ZnO stack, without interface acceptor states, at +1 V bias.

electric field. At the p/n -junction the concentration is too low to detect small changes in the concentration by GDOES, but the band diagram in Fig. 6.6b shows that at +1 V the Na^+ ions should be pushed into the GaO_x .

In summary, Na present at the CIGSe/ZnO interface induces over time an increasing barrier for electron extraction. During the degradation a diffusion of Na from the GaO_x to the CIGSe was observed from XPS measurements. The degradation process was partly reversible by applying an electric field. GDOES depth profiles could prove that Na migrates within an electric field inside the CIGSe. Under operating conditions the photo-voltage works against the degradation mechanism. It should be noted that a change in the GaO_x layer thickness could not be detected.

Discussion It was shown that degradation of superstrate devices occur under two conditions, first, if stored in an oxygen containing atmosphere and second, if the device contains sodium. Regarding the first point, in the presence of oxygen, a thin layer of GaO_x forms between the Au contact and the CIGSe absorber. This is likely to be caused by cracks in the thin Au back contact, which allow oxygen to diffuse to the Au/CIGSe interface. The presence of sodium was shown to accelerate this process.

If sodium is also present at the interface between ZnO and CIGSe, the p/n -junction appears to degrade over time if stored unbiased and in the dark. It was shown that the charge extraction efficiency was lowered during this process, most likely due to the formation of an electron barrier at the interface.

In Sec. 5.2, it was argued, that the experimentally observed kink in the $J - V$ curve of

superstrate devices is due to Na_{Ga} states within the GaO_x layer. Thus it seems logically, that the increasing kink during the degradation process is induced by sodium migration to the interface, which increases the acceptor density within the GaO_x layer.

However, this migration seems to be induced by the electric field of the p/n -junction, as it does not occur at an applied voltage of +1 V which cancels the electric field of the p/n -junction. And the electric field of the p/n -junction would push the Na^+ ions, just like holes, into the CIGSe away from the GaO_x layer. That raises the question, why does the kink increase if the source of the kink, which is believed to be Na, diffuses out of the narrow p/n -junction, which means out of the GaO_x layer.

This could only occur, if the Na_{Ga} states are transformed into V_{Ga} states within the GaO_x layer. This would increase the valency of the acceptor state from -2 to -3, thus increasing the negative charge within the GaO_x and with-it the electron barrier.

No literature values for the mobility of Na^+ ions directly in amorphous GaO_x exists, but for the $\text{Na}_2\text{O}-6\text{Ga}_2\text{O}_3$ system. It shows very high mobilities of Na, comparable with those of liquids [153]. Assuming again, that the p/n -junction is limited to the GaO_x , the electric field in the dark without voltage bias is about 6 MV/cm within the sodium doped GaO_x , which is close to the estimated breakdown field of 8 MV/cm [154] for Ga_2O_3 , and strong enough to cause electro-migration of sodium or even copper ions. The migration of Cu^+ within CIGSe due to an electric field was also observed in [155].

Applying a positive bias to the device was shown to hinder the degradation, or even reverse the degradation. This can be explained by the reduction of the electric field at the p/n -junction which stops or reverses the sodium migration.

However, the positive bias could not hinder the decrease of the short circuit current over time together with the capacitance increase measured around zero voltage and at negative biases. As shown in Sec. 3.2 and as it will be confirmed in the following Sec. 7.1 this can be explained by a $p+$ layer within the CIGSe at the interface to GaO_x . Thus it is likely that sodium from the CIGSe bulk diffuses to the interface and forms a $p+$ layer at the CIGSe interface to GaO_x .

To avoid the Na induced degradation mechanism it is therefore important to keep the Na concentration at the interface as small as possible. Devices which were shown to have little Na at the GaO_x interface, as the ones with a Mo diffusion barrier deposited prior to the NaF PDT (Sec. 5.2.4), did not degrade over time. Also, the low-rate deposition of NaF lead to low Na concentration at the interface and therefore stable and efficient devices. An example is shown in Fig. 6.5c.

Damp-heat tests of encapsulated devices have not been performed so far, which has to be done in the future.

6.3 Summary: Back contact and degradation

1. **Back contact:** A Cu-poor back surface was found to be present in most devices, which was shown to induce a hole barrier at the back contact, leading to a roll-over

in the $J - V$ curve. Na doping decreases the barrier at the back contact.

Alternative back contact metals were found to be only Pt. The insertion of MoO_{3-x} allowed the use of Ag, which is highly reflective and more cost effective than Au or Pt. Device simulations indicate the potential of a CIGSe thickness reduction by 40% due to the high reflectivity of Ag in comparison to Mo.

2. **Degradation of the back contact:** GaO_x formation at the CIGSe/Au interface was observed after prolonged storage in air. Cracks in the thin Au back contact may allow oxygen to diffuse to the Au/CIGSe interface. The GaO_x layer introduces a hole barrier due to the large band gap, which results in a strong roll-over of the $J - V$ curve. The presence of sodium at the CIGSe/Au interface was found to accelerate this process.
3. **Meta-stability/Degradation of the p/n -junction:** A reversible degradation mechanism was found to reduce the fill factor of the $J - V$ curves. Based on XPS and GDOES measurements, this is assumed to be induced by sodium migration out of the GaO_x layer. The Na migration is triggered by the strong electric field of the p/n -junction which is confined to the GaO_x layer. Na_{Ga} states are transformed into V_{Ga} states, which have a valency of -3, thus increasing the negative charge within the GaO_x and with-it the electron barrier. This effect could explain the observed dependence of the device performance on the light and voltage bias soaking previously observed on superstrate devices in the literature [22] [5].

A non-reversible degradation is the reduction of the short-circuit current, which is also assumed to originate from Na migration, but from the CIGSe bulk to the CIGSe interface region. Creating an additional $p+$ layer at the interface. Both effects only appear for high concentrations of Na at the interface. Low-rate NaF PDT reduces the sodium concentration at the hetero-interface leading to stable devices.

Chapter 7

Device Modelling

This chapter sets up a 1-D device model to describe the properties of the different superstrate devices observed so far. A device model for a substrate device fabricated under comparable conditions will be used as a comparison at the end of this chapter. Based on these models strategies to overcome the limitations will be discussed in Chapt. 8.

7.1 Device model for superstrate solar cells

To verify the speculations of the previous sections and to find solutions for the existing limitations of the superstrate solar cell, a device model has to be found which can explain the effects of the temperature dependence, Na doping and the ageing effects. This section will set up a model for the non-degraded, non NaF treated device fabricated at 525 °C. This model will then be used to find the relevant parameters, which can describe the effects of Na and ageing.

Table 7.1: Source of the simulation parameters used to simulate the $J - V$ curve of the standard device fabricated at 525 °C without external Na supply.

measured		from literature		from model	
$\Delta E_{V,BC}$	0.06 eV	χ_{CIGSe}	4.5 eV	χ_{GaO_x}	4.55 eV
$N_{A,\text{CIGSe}}$	$5e+14 \text{ cm}^{-3}$	χ_{ZnO}	4.6 eV	$N_{D,i-\text{ZnO}}$	$1.58e+19 \text{ cm}^{-3}$
$L_{n,\text{CIGSe}}$	800 nm	$N_{D,\text{ZnO:Al}}$	$1e+20 \text{ cm}^{-3}$	N_{A,GaO_x}	$1.27e+19 \text{ cm}^{-3}$
E_g profile	Fig. 2.3	$\mu_{n,\text{CIGSe}}$	$10 \text{ cm}^2/\text{Vs}$	$N_{A,\text{CIGSeIF}}$	$5e+14 \text{ cm}^{-3}$
d_{GaO_x}	6 nm	$\mu_{h,\text{CIGSe}}$	$2.5 \text{ cm}^2/\text{Vs}$	$N_{A,\text{GaO}_x/\text{ZnO}}$	0 cm^{-2}
R_S	$0.7 \Omega \text{ cm}^{-2}$	α_{CIGSe}	[100]	$S_{n,h,\text{CIGSe}}$	$1.0e+6 \text{ cm/s}$
R_P	$1 \text{ k}\Omega \text{ cm}^{-2}$	DOS_{CB}	$2.2e+18 \text{ cm}^{-3}$		
		DOS_{VB}	$1.8e+19 \text{ cm}^{-3}$		
		ϕ_{Au}	5.3 eV		

Standard device

Tab. 7.1 lists the important parameters used for the SCAPS device model for the standard device, a non-degraded, non NaF treated device fabricated at 525 °C. Many parameters are known from measurements or from the literature. The unknown parameters are listed in the column "from model".

A precise quantitative solution can however not be expected, since the simulation does not take 2 dimensional effects and grain boundaries into account. Even though the 2 dimensional variations are strongly reduced for superstrate devices compared to substrate devices, where the roughness of the p/n -junction is determined by the CIGSe surface roughness, the thickness variation of the GaO_x layer does also introduce a certain error. Further, small errors in the literature or the experimental values will induce errors to the fitting parameters. However, such a 1-D model based on many literature values is still a valid estimation to the reality, if it is possible to find a parameter set, which reproduce general trends observed in the $J - V$ curves and in the $C - V$ curves.

To find this parameter set, it is a good strategy to first fit the $C - V$ profile with only the relevant fitting parameters. These are the free charge carrier densities in the GaO_x and ZnO layers plus deep acceptors in the bulk and at the interfaces of the n -type materials GaO_x and ZnO and deep donors in the p -type material CIGSe. Once approximate values are obtained from the $C - V$ curve fitting, they are fixed for the $J - V$ curve fitting. For the $J - V$ curve only the interface recombination velocity, $S_{n,h\text{CIGSe}}$, and the electron affinity of the GaO_x layers are left as the free fitting parameters. The bulk and interface defects within CIGSe are set as neutral in the model. The CIGSe layer is separated into three layers within the model, one fixed bulk layer with $N_{A,\text{CIGSe}}$ and two interface layers, which can differ from the bulk properties due to Cu deficiency and/or increased sodium content (will be stated when applied).

Modelling $C - V$ data To derive the charge distribution within the sample deposited at the optimum temperature of 525 °C without external Na supply, the $C - V$ curve is fitted as described above. Fig. 7.1a shows the $C - V$ curve with the typical strong capacitance increase under forward bias. Simulations assuming any kind of bulk defect in the CIGSe, distributed homogeneously or close to the hetero-interface, could not reproduce any qualitatively similar $C - V$ curves. However, it is possible to simulate the $C - V$ curve almost perfectly, by assuming an acceptor state density of around $1\text{e}+19 \text{ cm}^{-3}$ within the GaO_x and setting the shallow donor state concentration to a similar value within the i -ZnO. This leads to the simulated $C - V$ curve shown in Fig. 7.1a. It should be noted, that acceptor states at the interface between GaO_x and ZnO, with a density of around $6\text{e}+12 \text{ cm}^{-2}$, can lead to a similar shape of the experimental $C - V$ curve. Whereas acceptor states at the CIGSe/ GaO_x interface, like O_{Se} , could not reproduce the $C - V$ profile. A combination of defects at the CIGSe/ GaO_x interface and the GaO_x bulk could however qualitatively reproduce the profile. Thus, it can be concluded that the high capacitance at forward bias originates from acceptor states dominantly located within the GaO_x layer or at the GaO_x/ZnO interface. For the simulation results, the energetic position of the

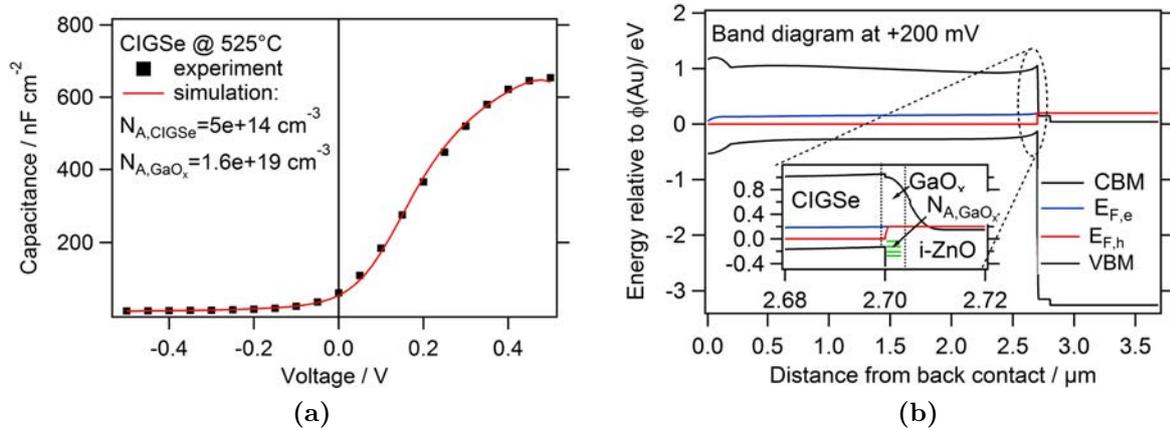


Figure 7.1: a) Experimental and simulated $C - V$ curves, recorded at 293 K and 1 kHz, from a standard superstrate device fabricated at 525 °C without external Na supply. The simulation with the best fit assumes a high acceptor state density N_{A,GaO_x} within the GaO_x layer. b) Energy band diagram at a positive voltage bias of 200 mV resulting from the fit parameters listed in Figure a). The inset shows a magnification of the p/n -junction, where the 6 nm thick and charge depleted GaO_x layer is marked by the two dashed lines.

acceptor states has to be at least 900 meV below the CBM of GaO_x to be below the quasi-Fermi level for electrons, which ensures permanent occupation. In this model the acceptor level is arbitrarily set to 1.2 eV below the CBM of GaO_x , as shown in Fig. 7.1b.

In this model, the electrons from the ZnO occupy the acceptor states within the GaO_x . If the density of acceptor states is similar to the shallow donor concentration in ZnO, the SCR of the p/n -junction will be limited to the GaO_x and the i-ZnO. If the acceptor density is lower, the SCR can reach into the CIGSe. However, if the density is higher, the Fermi level within the GaO_x will be pushed towards the acceptor level, resulting in a lift of the CBM, which could induce an electron barrier. Both situations are shown in Fig. 7.2b and in Fig. 7.1b for equal densities and +200 mV. If the acceptor density is equal or larger compared to the donor density the SCR extends into the CIGSe only at negative voltage biases. This is the reason for the low capacitance observed only at reverse bias together with the efficient charge extraction as observed experimentally from the EQE spectra. At forward bias, the capacitance increases, the SCR is limited to the GaO_x and the charge extraction is reduced.

It should be kept in mind, that the simulation is one dimensional and that e.g. spatial variations of the GaO_x thickness and GaO_x doping inhomogeneities on the nm-scale are not taken into account. The TEM-EDX mapping image of the GaO_x layer in Fig. 5.7b in Sec. 5.1.3 shows, that the local thickness varies between 5 - 10 nm. Similar variations in the doping density can be assumed. Thus, the fitting value for the acceptor density presented here is an average value, and it has to be assumed, that this value varies locally.

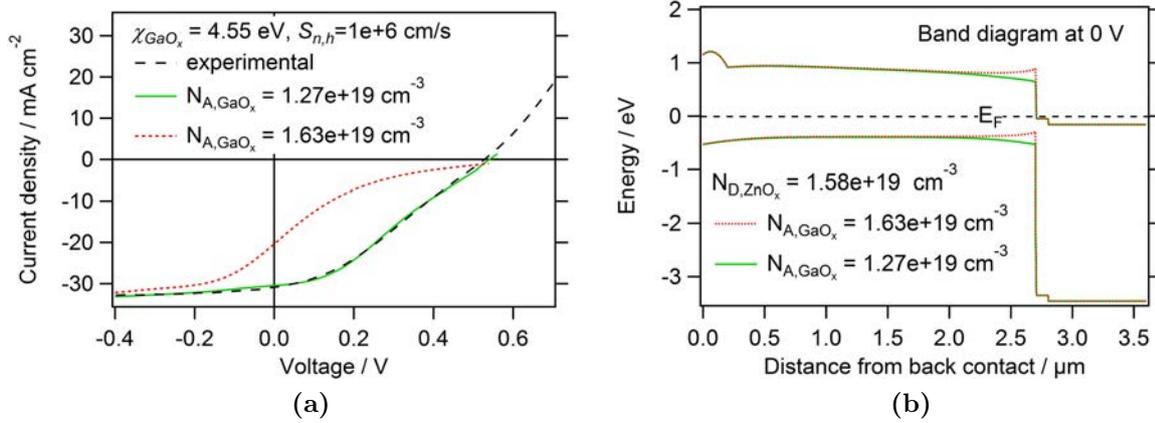


Figure 7.2: **a)** The dashed red line is the simulated $J - V$ curve with the parameters obtained from the fit to the $C - V$ curve shown in Fig. 7.1. The interface barrier is overestimated, likely due to local variations in the GaO_x properties. The green solid line shows the simulation result for a reduced acceptor density, which reproduces the experimental curve well (black coarsely dashed line). **b)** Energy band diagrams resulting from the two different acceptor densities used for the simulation in Figure a).

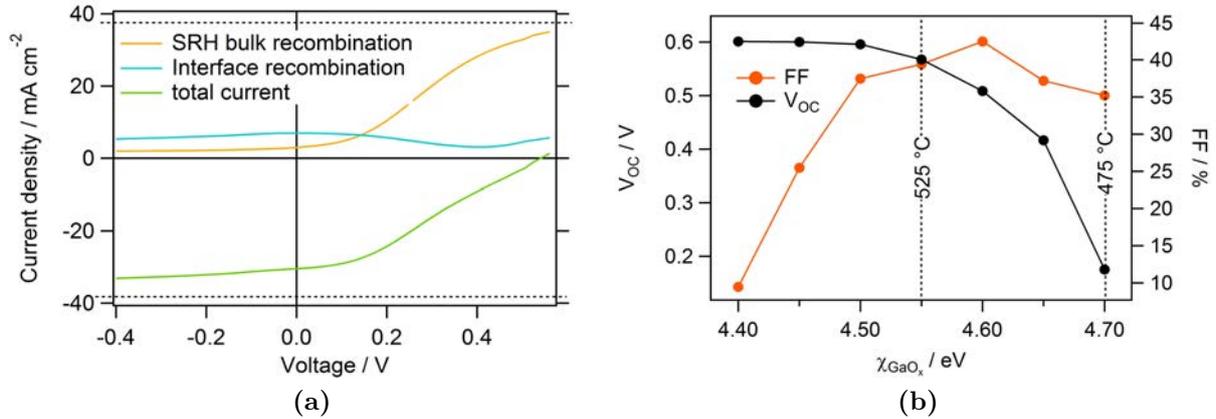


Figure 7.3: **a)** The same simulated $J - V$ curve as shown in Fig. 7.2a, together with the interface recombination current ($S = 1 \times 10^6 \text{ cm/s}$) and bulk recombination current ($L_n = 0.8 \mu\text{m}$). The dashed bars indicate the maximum photo-current. **b)** V_{OC} and FF in dependence of χ_{GaO_x} . The model predicts $\chi_{\text{CIGSe}} = 4.55 \text{ eV}$ for the CIGSe deposition temperature of 525°C . At a lower deposition temperature, the χ_{GaO_x} is reduced due to the In content within the GaO_x , leading to lower V_{OC} values.

Modelling $J - V$ data To simulate the $J - V$ curve only two unknowns are left, since the charge distribution and thus the doping profile was obtained from the $C - V$ fit. As argued above and shown in Tab. 7.1 the electron affinity of GaO_x (χ_{GaO_x}) and the interface recombination velocity ($S_{n,h}$) are still free fit parameters. The resulting best fit to the experimental $J - V$ curve is shown as the red dashed line in Fig. 7.2a. Independent of the choice of the two free fit parameters, the electron transport barrier at the GaO_x is simply too high to achieve a good fit to the experimental data. But, as stated in the previous paragraph, the GaO_x acceptor density and therefore the barrier height is likely to vary locally. Such a variation would create preferable electron transport pathways, similar to point-contacts on the nm scale. If the GaO_x acceptor density is lowered from $1.63\text{e}+19 \text{ cm}^{-3}$ to $1.27\text{e}+19 \text{ cm}^{-3}$ to take this effect into account, the barrier over the GaO_x is reduced as shown in Fig. 7.2b. Together with $\chi_{\text{GaO}_x}=4.55 \text{ eV}$ and $S_{n,h}=1\text{e}+6 \text{ cm/s}$ for the free fit parameter, a very good fit to the experimental $J - V$ curve is possible, as shown in Fig. 7.2a. However this requires a reduction of $N_{\text{A,GaO}_x}$ by 20 % for the illuminated $J - V$ curve and 30 % for the dark $J - V$ curve (not shown). The recombination currents for the simulated $J - V$ curve are shown in Fig. 7.3a, separated into interface and bulk recombination. The simulated curves are only shown until $J = 0$ because SCAPS were running into problems for the non-ohmic back contacts under injection condition where $J > 0$.

According to these simulation results, the open circuit voltage and the fill factor are mainly defined by the bulk recombination rate, which is strongly enhanced under forward bias due to the extraction barrier induced by the non-depleted acceptor states in the GaO_x . The voltage dependent profile of the bulk recombination therefore correlates well with the corresponding capacitance profile. The voltage dependent collection length obtained from the EQE spectra support this result. The short circuit current is reduced due to bulk and interface recombination. The interface recombination remains about constant for all voltages, due to the low electron density within the GaO_x layer.

Impact of the electron affinity The electron affinity for the GaO_x , χ_{GaO_x} , was determined to be 4.55 eV, leading to a small cliff at the CIGSe/ GaO_x interface. However, lower CIGSe deposition temperatures increase the In content and with-it χ_{GaO_x} . Fig. 7.3b shows the effect of different electron affinities on V_{OC} and the fill factor.

If χ_{GaO_x} is increased the CBM cliff increases, which increases the electron density at the interface and therefore the interface recombination current. The limiting factor for the interface recombination in this case is the hole density within the CIGSe at the interface. The hole density increases with increasing positive voltage and therefore the recombination current increases under forward voltage bias as seen in Fig. 7.3b. Thus, for a cliff type interface between CIGSe and the interfacial oxide layer, the V_{OC} limiting factor is the interface recombination. Thus, this model can explain the observed significant drop in V_{OC} for GaO_x layers with increased electron affinity due to increased In content, like the samples deposited at low temperatures.

Table 7.2: Values derived from the C–V curve simulations: acceptor and donor state densities within the GaO_x, the CIGSe close to the interface, the CIGSe bulk and ZnO at the interface. Values derived from the J–V curve simulations: Diffusion length within the CIGSe, $L_{n,\text{CIGSe}}$, and interface recombination velocity at the CIGSe/GaO_x interface, S_{IF} . It should be noted, that the values for N_A GaO_x were reduced by 10-20% for the illuminated J–V curve simulations.

sample	N_A GaO _x bulk cm ⁻³	N_A CIGSe at interface cm ⁻³	N_A CIGSe bulk cm ⁻³	N_D i-ZnO _x bulk cm ⁻³	L_n μm	S_{IF} cm/s
No Na	1.6e+19	5.0e+14	5.0e+14	2e+19	0.8	1.0e+6
Na @ 300 °C+ Mo	1.6e+19	9.0e+15	9.0e+15	2e+19	1.6	3.5e+6
Na @ 300 °C	2.3e+19	1.0e+18	5.0e+16	1e+20	1.6	4e+5
- Stored at 0 V	2.8e+19	2.0e+18	5.0e+16	1e+20	1.6	4e+5
- Stored at +1 V	2.3e+19	2.0e+18	5.0e+16	1e+20	1.6	4e+5
Na @ 400 °C	3.7e+19	1.1e+18	5.0e+16	1e+20	1.6	4e+5

In case of conduction band spike at the interface (when $\chi_{\text{GaO}_x} < 4.5$ eV) photo-generated electrons from the CIGSe accumulate at the interface and lead to an enhanced recombination rate at flat band condition around 0 V. At forward bias the accumulation is lowered due to the lifted conduction band at the interface. This explains the lowered photo-current observed for devices with an annealed Ga₂Se₃ precursor (see Fig. 5.15b) or which were deposited at higher temperatures, as the GaO_x layer in these devices have a decreased electron affinity due to the decreases In content.

Influence of sodium

The device model with the parameters listed in Tab. 7.2 is now used to simulate the C–V curves of the sodium containing devices.

All experimental C–V curves for different sodium treatments can be well reproduced by adjusting the acceptor densities within the GaO_x and the CIGSe, as seen in Fig. 7.4a and Fig. 7.4c. The adjusted parameters are summarized in Tab. 7.2. In all cases the NaF PDT increases the charge carrier density in the CIGSe bulk considerably. Whereas the CIGSe charge carrier density at the interface and the acceptor density within the GaO_x is only increased for the samples without Mo diffusion barrier. And this increase is more pronounced for the NaF PDT at 400 °C compared to the PDT at 300 °C. The trend of the acceptor densities is similar to the experimentally observed trend of the sodium concentration at the interface as seen in Fig. 5.12a and 5.22. This shows that the sodium concentration is directly related to the acceptor density at the hetero-interface. Further, the device model leads to an increased i-ZnO doping for the samples with an increased sodium concentration at the interface. This could be due to the catalytic effect of sodium, which creates more oxygen vacancies within the ZnO close to the hetero-interface or due to Na interstitials within the ZnO.

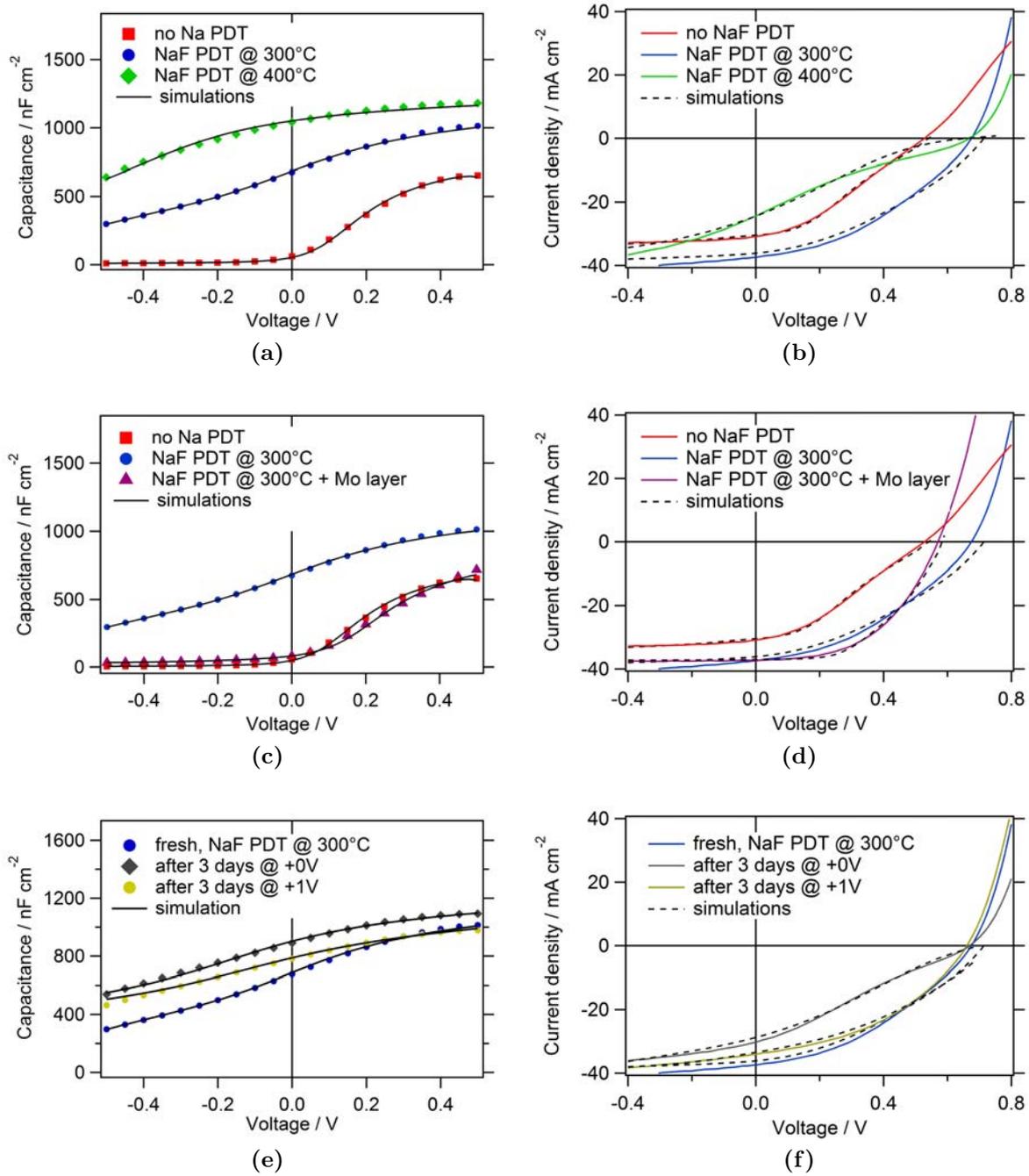


Figure 7.4: Simulated and experimental $C - V$ and $J - V$ curves of CIGSe/ZnO devices fabricated at 525 °C. The $C - V$ simulations are based on the model of deep acceptor defects within the GaO_x layer. For the $J - V$ simulations the results of the $C - V$ fits were used, free fit parameters were the diffusion length and the interface recombination velocity. **a)** and **b)** show the results for different NaF PDT temperatures. **c)** and **d)** show the results for the Mo diffusion barrier. **e)** and **f)** show the curves of the degraded samples.

The simulated $J - V$ curves for the sodium treated devices are shown in Fig. 7.4b and Fig. 7.4d. The results of the $C - V$ simulations were used for the doping and defect distribution within the device. Due to the above discussed effect of the two-dimensional variation of the GaO_x thickness and doping density, the value were again lowered by around 10-20% to achieve a better fit to the experimental $J - V$ curves. Further, the charge carrier density in the interface near CIGSe layer was set to the same value as in the bulk to enable fitting of the $J - V$ curves. The diffusion length and the interface recombination velocity were free fitting parameters, whereas the GaO_x electron affinity was fixed at 4.55 eV. The fit results for these two parameters are shown in Tab. 7.2. According to the fit results, the CIGSe layers, which contains sodium in the bulk, show an increased electron diffusion length of 1.6 μm . Plus, the two samples, which have a high concentration of sodium at the interface, show a reduced interface recombination velocity. Leading to the conclusion, that within this model, sodium reduces the recombination rate within the bulk as well as at the interface.

Degradation

The influence of the degradation under a voltage bias of +1 V on the $C - V$ curve is shown in Fig. 7.4e. It can be well reproduced with the model for the NaF treated device if the charge carrier density is increased within the CIGSe in the direct vicinity of the hetero-interface with GaO_x . The exact values are given in Tab. 7.2. This creates an additional p+ layer within the CIGSe, which leads to an additional electron barrier, constant for all the voltages applied in the experimental range, explaining the reduced short circuit current. The simulated $J - V$ curve with the input data from the $C - V$ fit gives a very good fit to the experimental $J - V$ curve, the degradation has no influence on the electron diffusion length, GaO_x electron affinity or interface recombination velocity.

The influence of the degradation without any voltage bias on the $C - V$ curve is also shown in Fig. 7.4e. To reproduce this curve an additional parameter needs to be adjusted. The acceptor density within the GaO_x has to be increased from $2.3\text{e}+19 \text{ cm}^{-3}$ to $2.8\text{e}+19 \text{ cm}^{-3}$. This creates a stronger voltage dependent barrier for electron extraction and leads to the additional decrease of the fill factor. Thus, in both cases the applied model for the $C - V$ data allows very good predictions for the $J - V$ data, without any additional parameter variation.

The reversible degradation process is the change of the acceptor density within the GaO_x and the non-reversible part is the due to the development of a p+ layer within the CIGSe close to the hetero-interface. Both processes presumably due to Na^+ migration (see Sec. 6.2).

7.2 Device model for substrate solar cells

To compare the properties of the superstrate device with them of a standard substrate device this section sets up a model for a substrate device with CdS as the buffer layer,

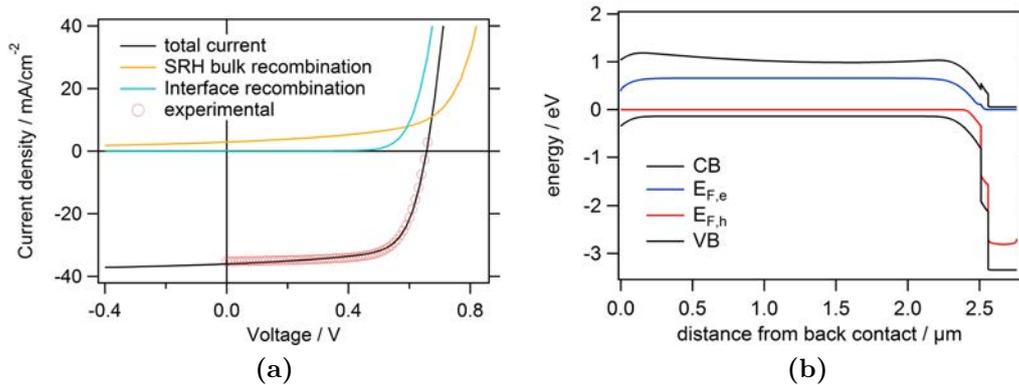


Figure 7.5: a) Experimental and simulated $J - V$ curve of a substrate type device under illumination, shown together with the bulk and interface recombination currents from the simulation (diffusion length $1.9 \mu\text{m}$, IF rec. Vel. $2\text{e}+4 \text{ cm/s}$, mid-gap acceptor). b) Corresponding band diagram at 0 V voltage bias.

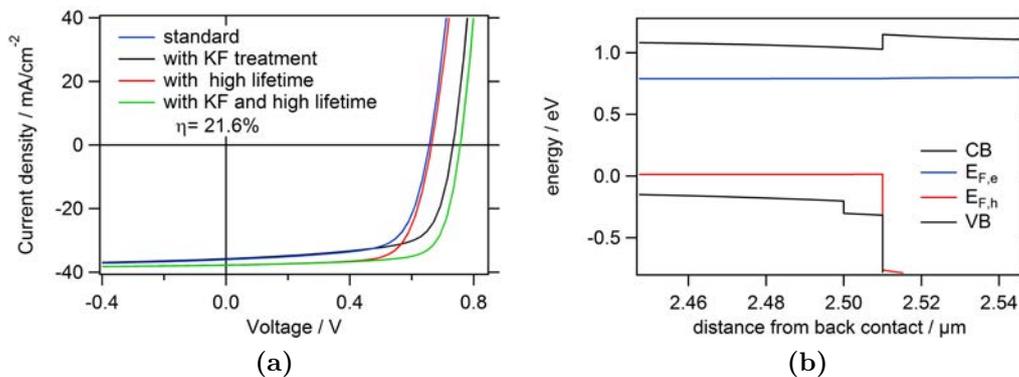


Figure 7.6: a) Simulated $J - V$ curve from Fig. 7.5 with lowered VBM at the CIGSe surface due Cu depletion, with increased electron lifetime of the CIGSe and with both effects combined. b) Corresponding band diagram at 0 V voltage bias shows the lowered VBM due to Cu depletion, potentially induced by the KF treatment.

but otherwise fabricated by identical tools and an equivalent deposition process. The experimental and simulated $J - V$ curve of a typical in house fabricated device is shown in Fig. 7.5a. The charge carrier density of the CIGSe was obtained from $C - V$ measurements performed at room temperature and 1 kHz . The band gap profile was measured with GDOES. The properties for CdS, ZnO and Molybdenum were chosen as shown in Tab. 3.1 and in [100]. The recombination rate is described with two parameters, a neutral bulk defect and an acceptor type interface defect. Both defects were set as free fitting parameters. From this an electron diffusion length of $1.9 \mu\text{m}$ (corresponds to a lifetime of 27 ns) and an interface recombination velocity of $2\text{e}+4 \text{ cm/s}$ is obtained. Fig. 7.5a also shows the recombination currents in the bulk and at the interface. This shows that within this device model, the J_{SC} is limited by the bulk recombination and the V_{OC} is limited

Table 7.3: Comparison of the solar cell characteristics of a substrate and a superstrate device.

Property	unit	Substrate	Superstrate
$N_{A,CIGSe}$	cm^{-3}	1e+16	9e+15
L_n	μm	1.9	1.6
S_{IF}	cm/s	2.0e+4	3.5e+6
R_s	Ωcm^{-2}	0.4	0.7
R_p	$\text{k}\Omega\text{cm}^{-2}$	1.1	1.0
$x_{SCR@500\text{mV}}$	nm	230	10
η	%	16.3	10.6

by the interface recombination. The efficiency of this device is 16%. From time resolved PL measurements charge carrier lifetimes between 10 and 100 ns are generally obtained. If the lifetime within this device model is adjusted to 100 ns (corresponds to 3.6 μm) a PCE of 18% can be achieved, which is indeed often achieved experimentally. Therefore it seems likely that the absorber bulk defects are the origin of the observed variations in the device performance of in-house substrate devices.

To further increase η and V_{OC} it is necessary to reduce the interface recombination, which can be done by changing the buffer chemistry, or by engineering the absorber surface prior to the buffer deposition. The latter is done for the current record efficiency devices by an additional KF treatment. The KF PDT depletes the surface from copper [144] resulting in a lowered VBM at the interface [43]. This can be modelled by changing the properties of the first 10 nm of the absorber within the device model. The results are shown in Fig. 7.6 together with the resulting band alignment at the interface.

7.3 Superstrate vs. Substrate

This section compares a standard substrate device with a superstrate device. The Na supply for the substrate device was from the soda lime glass and for the superstrate device from a low-rate NaF PDT, which was shown to lead to record efficiencies of up to 11%. Both absorber had a minimum band gap of approximately 1.15 eV. The experimental $J - V$ curves together with the corresponding energy band diagrams (at 500 mV) are shown in Fig. 7.7. The solar cell characteristics are compared in Tab. 7.3.

The solar cell characteristics in Tab. 7.3 show, that despite the Zn contamination in the superstrate device, both devices are quite comparable in terms of CIGSe doping, $N_{A,CIGSe}$, and electron diffusion length, L_n . This is another indication, that the concentration of the harmful Zn_{Cu} states is reduced in the presence of Na. Further, the series and parallel resistances, R_s and R_p , of both cells are comparable, with a lower series resistance of the substrate device due to the metal grid on top of the TCO.

The difference in the efficiency, can be found in the interface recombination velocity, S_{IF} , and the width of the space charge region, x_{SCR} , at forward bias. The small x_{SCR} for the superstrate cells is due to the high acceptor density at the GaO_x interfacial layer. This

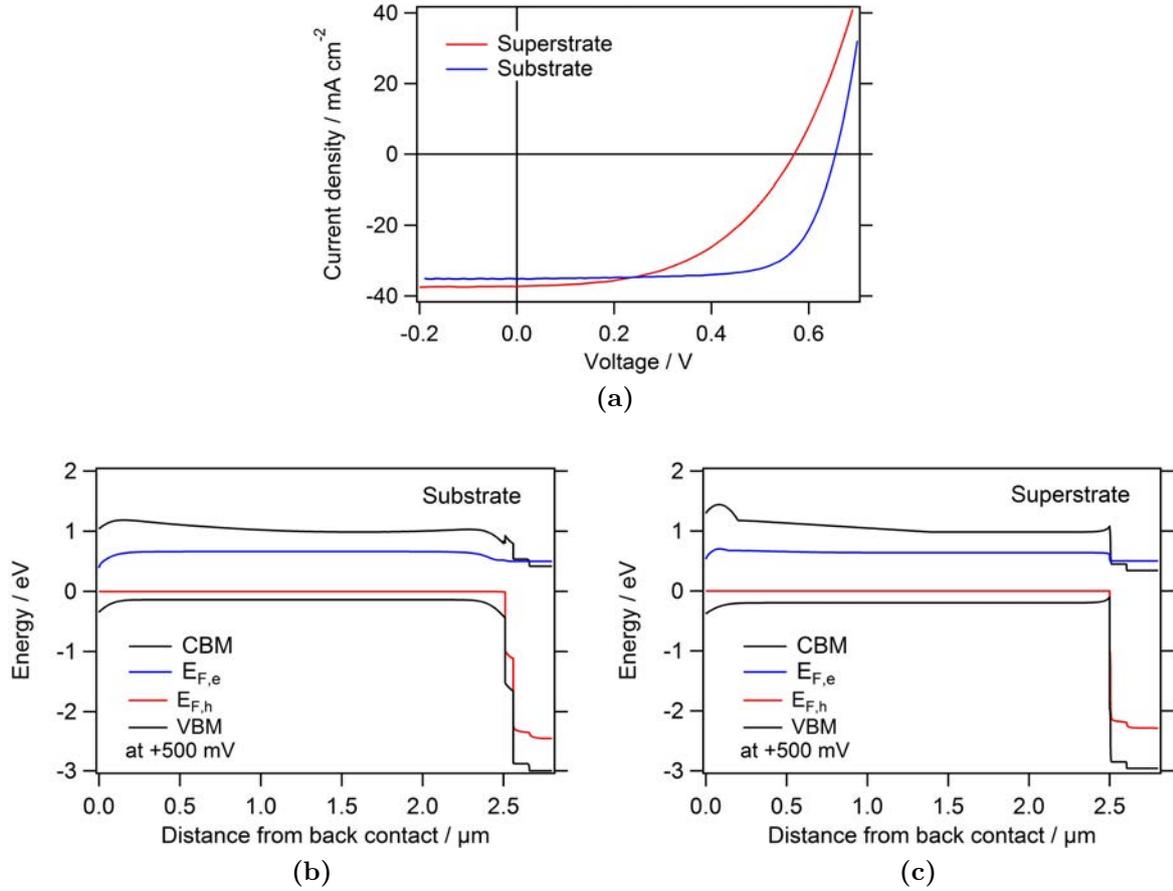


Figure 7.7: a) $J - V$ curve of a substrate and a superstrate solar cell. b-c) Energy band diagram of the two devices at 500 mV voltage bias, obtained from the device modelling in Sec. 7.2 and in Sec. 7.1.

prevents the type inversion observed for the substrate device in Fig. 7.7b. In combination with the high interface recombination velocity this leads to a lower V_{OC} for the superstrate device. Further the charged acceptor states in the GaO_x lower the fill factor due to a reduced x_{SCR} .

7.4 Summary: Device modelling

A device model was found which can reproduce the experimental $C - V$ and $J - V$ curves of ZnO/CIGSe/Au superstrate devices for different Na treatments and different ageing conditions. The results were compared to the device model for a standard substrate device. In the following a summary of the simulation results is given:

1. **Acceptor states at the hetero-interface:** The observed low $J - V$ curve fill factor of superstrate devices was successfully correlated to interfacial acceptor

states. The model confirms the assumption of deep acceptor states (like Cu_{Ga}) within the GaO_x layer and/or at the GaO_x/ZnO interface. Acceptor states at the $\text{CIGSe}/\text{GaO}_x$ interface (like O_{Se}) may be present but could not describe the $C - V$ profile sufficiently well.

2. **Influence of Na:** The influence of Na was correlated with an increase of the charge carrier density in the CIGSe bulk, together with an increase of the density of deep acceptor states at the hetero-junction. The optimum NaF PDT temperature is therefore determined by the optimum balance between these two effects. Further, Na reduces the recombination rate in the CIGSe bulk and at the hetero-interface within this model.
3. **CB alignment:** The device model predicts a conduction band cliff of 50 meV between CIGSe and the interfacial GaO_x layer. Still, the presence of the GaO_x layer reduces the interface recombination, since it lowers the electron density at the hetero-interface. However, the cliff increases with increasing In content within the interfacial oxide layer, which was shown to decrease the V_{OC} due to a high interface recombination velocity. Potential buffer layers leading to a CBM spike are predicted to further increase the electron barrier and with it reducing the fill factor.
4. **Origin of degradation:** The simulation of the $C - V$ data revealed that the reversible part of the degradation (meta-stability) is due to an increase of the acceptor density within the GaO_x layer. The non-reversible part is due to an increase of the acceptor density within the CIGSe at the interface. This is in accordance with the model presented in Sec. 6.2, that the reversible part is due to Na migration in the p/n -junction and the non-reversible part is due to Na migration outside of the p/n -junction.
5. **Comparison to substrate devices:** The comparison suggests, that the electron diffusion length in NaF treated superstrate absorber is not strongly reduced due to the Zn contamination. But the high interface recombination velocity in combination with the high acceptor density at the hetero-interface reduces the FF and the V_{OC} of the superstrate device compared to the substrate device.

Chapter 8

Strategies for efficiency improvement

In the course of this thesis, the CIGSe/ZnO system has been optimized to a power conversion efficiency of up to 11 %, mainly by experimental optimization of the CIGSe deposition routine and the sodium supply. Here, the device model which was set up in the previous chapter, will be used to evaluate which of the device parameters inhibits the highest potential for further efficiency improvement. A proposition to change this parameter will be followed up experimentally by applying new oxide buffer layers.

8.1 Parameter evaluation

The first obvious parameter to examine within the model is the **minority carrier diffusion length**. The diffusion length in the cells studied here are eventually limited by the Zn contamination, even though Na doping seems to lower this effect. Further, the diffusion length could be improved by reducing the background impurity level during the CIGSe fabrication. However, the simulations show, that an increase of the electron diffusion length from 1.6 μm to 3.2 μm leads to an efficiency increase of only 0.5 %, from 11.0 % to 11.5 %.

Another way to increase the efficiency is to reduce the **interface recombination** losses. Within the model, this can be achieved most efficiently, by lowering the VBM by 100 meV within the 10 nm of the CIGSe next to the hetero-interface (compare with Sec. 3.1). An increase of η to 13.3 % is predicted by the model. As shown in Fig. 1.5b this can be achieved by reducing the Cu concentration at the hetero-interface. Substrate devices exhibit the advantage of a Cu-poor surface induced by a surface reconstruction [156] or induced by post treatments [144]. In superstrate devices it is difficult to engineer a Cu poor interface due to the high mobility of Cu within CIGSe. However, optimisation of a KF PDT may enable a Cu depletion at the hetero-interface in the future. It may also be possible to exploit the high mobility and deplete the interface from Cu by electro-migration [157] at negative biases. However, the cells studied here showed improvement during positive biasing, due to the electro-migration of sodium. Another option to reduce the VBM is the exchange of Se atoms locally with S atoms. In Fig. 8.1 and in more detail

Table 8.1: Pathway to 20% efficiency, by optimizing certain parameters within the device model.

Steps	Varied parameter	from	to	efficiency
0	none	-	-	11.0
1	el. diff. length, $L_{L,n}$	1.6 μm	3.2 μm	11.5
2	VBM offset, $\Delta E_{V,S}$	0 eV	0.1 eV	13.3
3	Acceptor density N_{A,GaO_x}	1.2e+19 cm^{-3}	2e+18 cm^{-3}	15.5
4	n -type doping, N_{D,GaO_x}	1e+17 cm^{-3}	2e+19 cm^{-3}	17.1
1, 2 combined				15.2
2, 4 combined				18.4
1, 4 combined				19.3
1, 2, 3 combined				19.3
1, 2, 4 combined				20.2
1, 2, 3, 4 combined				20.3

in Sec. 10.2 it is shown, that it is indeed possible to confine the sulphur atoms close to the hetero-interface by the deposition of an In_2S_3 precursor prior to the CIGSe deposition. However, the increased sulphur content also causes an increased CBM of the chalcopyrite, which, in the presence of interfacial acceptor states, further increases the electron barrier and therefore lowers the device efficiency.

The combined effect of an increased diffusion length and a reduced VBM (by Cu depletion) at the hetero-interface would lead to a PCE of 15.2%.

The simulations presented in Chapter 7 point out though, that the main limitation of the superstrate solar cell devices originates from the high density of **acceptor type defects** within the interfacial oxide layer. Reducing the acceptor defect density by one order of magnitude, to 1.2e+18 cm^{-3} , leads to a simulated efficiency of 15.5%. However, this would require a reduced diffusion of Cu and Na into the GaO_x layer. An alternative would be to enhance the **n -type doping** of the interfacial oxide layer to 2e+19 cm^{-3} , which would increase the efficiency of 17.1%.

An overview of the different efficiency improvements due to the different optimization processes and their combinations are listed in Tab. 8.1. It should be noted, that in case a buffer layer is found which can suppress the effect of the interfacial acceptor states (step 4 in Tab. 8.1), it will be easy to reduce the interface recombination (step 2) by applying a sulphur gradient, leading to an efficiency of 18.4%. Combined with an increased diffusion length (3.2 μm) an efficiency of 20.2% could be achieved, despite the high density of acceptor defects within the buffer layer.

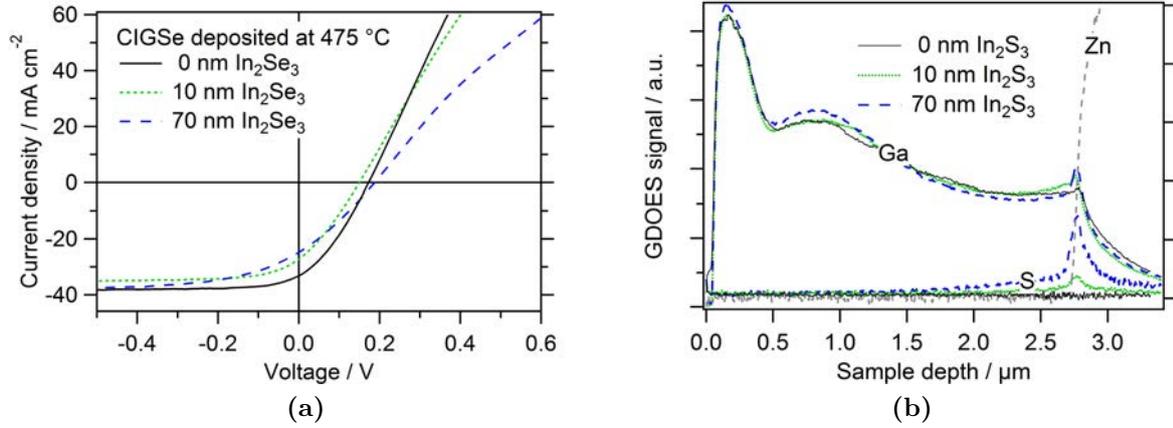


Figure 8.1: a) $J - V$ curve of devices with differently thick In_2Se_3 precursors and a CIGSe layer deposited by the modified 3-stage process at 475 °C. b) The corresponding GDOES depth profile shows the confined S gradient and that Ga prefers to accumulate at the S-rich regions. A solution to overcome this problem is presented in Sec. 10.2.

8.2 Definition of the ideal buffer layer

Thus, to achieve efficiencies above 20 %, a new material has to be found, which remains its n -type character even in the presence of copper and sodium. Further it also has to block the diffusion into the ZnO layer underneath. The additional criteria are high band gap, suitable electron affinity and chemical resistance against the formation of GaO_x during the deposition of CIGSe.

Criteria for an ideal buffer layer material in a superstrate CIGSe device:

1. n -type despite Cu and Na doping at the interface,
2. $N_D > 1 \times 10^{18} \text{ cm}^{-3}$,
3. Electron affinity, χ , between 4.25 eV and 4.50 eV,
4. Band gap above 3 eV,
5. Amorphous, or better lattice matched to CIGSe ,
6. High formation enthalpy, non-reactive with CIGSe and ZnO at 560 °C,
7. Diffusion barrier for Cu and Na.

Finding such a thermally stable and wide band gap material, in which Cu and Na do not introduce acceptor states is difficult. They require a formation enthalpy larger than the formation enthalpy of Ga_2O_3 . Otherwise Cu-contaminated Ga_2O_3 will form at the interface to CIGSe, which was shown to limit the device efficiency. Further, an amorphous

structure is generally preferred, since poly-crystalline layers allow Cu diffusion along the grain boundaries. Thus, all oxides which crystallize above 400 °C, which is the minimum CIGSe deposition temperature, are unlikely to perform well. To perform as a better diffusion barrier than amorphous Ga₂O₃, the ionic radii of the cations should be smaller compared to Ga³⁺, like Si²⁺ or Al³⁺. However, materials like amorphous SiO_x or AlO_x have too large conduction band offsets to CIGSe [134]. 3 nm thick SiO_x layers have been tested and didn't allow current transport. AlO_x has an even smaller electron affinity. The same for MnO.

However, a possible candidate for a material which is highly stable and a good diffusion barrier, would be amorphous Ga₂O₃ itself. It was shown in this work that GaO_x forms intrinsically at the CIGSe/TCO interface and that Cu and Na do introduce acceptor states within it. But it is not clear, which defect density will be induced by Cu and Na if Ga₂O₃ is deposited purposefully prior to a CIGSe deposition at low temperatures. It may be possible to compensate the acceptor states by intentional *n*-type doping of the Ga₂O₃ with Sn or Si [158] on the cation site or Cl and F [142] on the anion site. Charge carrier densities as high as 1e+19 cm⁻³ for Si [159] and 1.44e+19 cm⁻³ for Sn [160] as a dopant have been reported for crystalline β-Ga₂O₃. This would be sufficient to compensate the acceptor states induced by Cu and Na. The electron affinity of crystalline β-Ga₂O₃ is reported to be 4 eV [143], which would require alloying Ga₂O₃ with oxides of lower electron affinity, like In₂O₃ or SnO₂. Unfortunately, no reports on the electron affinity or on the doping of amorphous Ga₂O₃ exists. Therefore this will be studied in depth in Sec. 10.1. However, recently amorphous Ga₂O₃ was successfully applied as a buffer layer to CIGSe [?] and Cu₂O [161] solar cells in substrate configuration and in CdTe solar cells in superstrate configuration [162].

The question remains, whether or not the purposefully deposited Ga₂O₃ layer will have the suitable electron affinity and whether the Cu diffusion remains a problem. The following sections will try to answer these questions.

8.3 Combinatorial material exploration

By knowing the desired properties of the optimum buffer layer material in CIGSe superstrate devices, it would be ideal to predict the perfect material by quantum mechanical computations [163]. However, the time frame of this work did not allow this approach. An alternative option is to start with a good guess for a suitable material, like Ga₂O₃, and tweak its properties to these desired by alloying with other materials. In Sec. 8 amorphous Ga₂O₃ was identified as a base material, which will be alloyed with other elements whose conduction band is made of *s* orbitals, like Zn, Sn or In. The spherical symmetry of these orbitals is beneficial, as it makes the delocalized electronic transport less sensitive to structural disorder compared to *p* or *d* orbitals [164].

A very useful strategy to do this sufficiently fast is to produce graded samples, which allow fast screening of the fabricated alloys. This can be achieved with combinatorial pulsed laser deposition (PLD, see Sec. 2.2), in which the co-deposition of different materi-

als, from spatially separated sources, allows to create very defined compositional gradients onto the substrate.

Experiment

Based on the considerations given in the beginning of this section, the base material was chosen to be Ga_2O_3 , which is alloyed with TiO_2 , ZnO , SnO_2 , In_2O_3 and ZnSnO_3 to change the electron affinity and charge carrier density. The alloys were deposited on a 5 cm x 5 cm large alkali-free glass substrate covered with GZO. Generally the layers were deposited with two gradients, the overall layer thickness in X -direction and the Ga_2O_3 content in Y -direction. The deposition temperature was set to 100 °C to achieve amorphous layers, and set to 500 °C to achieve crystalline films. The oxygen partial pressure was set to 1.3e-5 mbar for the depositions at 500 °C and increased to 6.5e-3 mbar for the depositions at 100 °C to ensure the formation of transparent films. The doping with Sn and Ti is aiming to increase the charge carrier density and compensate potential acceptor states induced by Cu and Na during the subsequent CIGSe deposition. Additional materials with suitable electron affinities for CIGSe, like ZnMgO:Ga , SrTiO_3 and $\text{TiO}_2\text{:Nb}$, were prepared by PLD on GZO substrates. All films were prepared together with the group "Process Technology and Advanced Concepts" at the National Renewable Energy Laboratory (NREL).

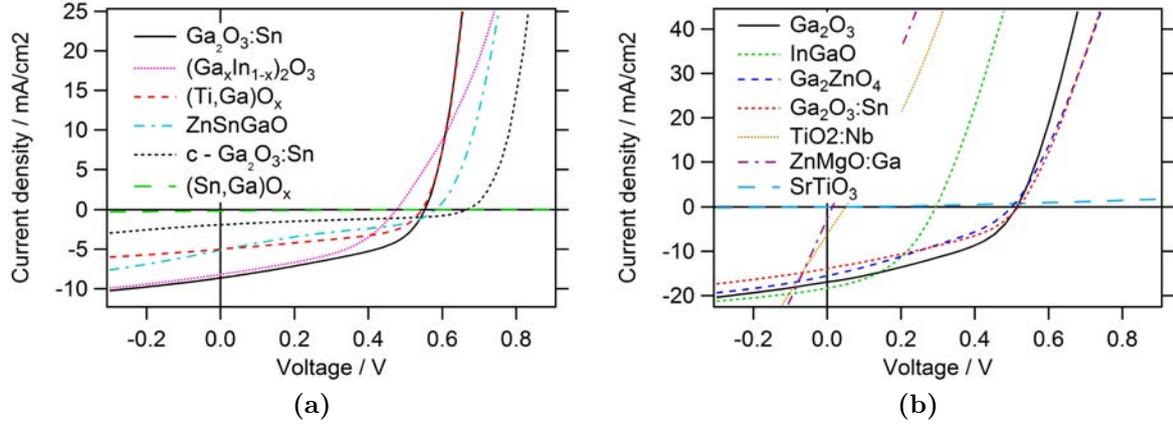
The CIGSe layer were deposited by M. Contreas at NREL. The deposition process was a different three-stage process from the one explained in Sec. 2.1, due to different PVD system specifications. In the first stage evaporation of In-Ga-Se was set with a constant rate, followed by a Cu-In-Ga-Se at a constant rate, followed by In-Ga-Se in the 3rd stage. The temperature was set to 450 °C. An SEM image of the absorber can be seen in Fig. 10.8. The process was not optimized and lead to poor absorber quality.

The back contacts were realized by thermal evaporation of 64 Au pixels (3x3 mm) distributed over the 5x5 cm CIGSe coated substrate. This allowed a mapping of the electrical properties of the graded compositions.

Results

The performance results of the solar cells with the different oxides as the buffer layer are shown in the table in Fig. 8.2. It should be noted, that only the best performing solar cell of the 64 solar cells on each sample is shown. The results originate from two CIGSe depositions, which lead to different absorber qualities, resulting in different values for the J_{SC} but identical V_{OC} values (due to Fermi-level pinning at the interface, will be discussed later). For both deposition runs, 10 nm thick amorphous Ga_2O_3 deposited at 100 °C, leads to highest efficiencies. The following paragraph will shortly describe the performance results of the different alloys.

Similar as in the work of Nakada et al. [5] the pure i-ZnO leads to non-rectifying devices for the Cu/(In+Ga) ratio of about 0.85 used in this experiment. This was observed reproducibly on 128 solar cells on two substrates and not only for i-ZnO, but also for



Material	Gradient	max. V_{OC}	max. PCE
ZnMgO:Ga	Ga, Mg	0	0
i-ZnO	d	0	0
ZnO:Ga	-	0	0
SrTiO ₃	d	0	0
TiO ₂ :Nb	Nb, d	60	0.06
(Zn, Ga)O _x	Ga, d	0	0
(Sn, Ga)O _x	Ga, d	500	0.02
(Zn, Sn, Ga)O _x (am)	Zn, Sn	580	0.6*
(Ti, Ga)O _x	Ga, d	500	0.9*
(Zn, Sn, Ga)O _x (cr)	Zn, Sn	450	1.2*
(In, Ga)O _x :Sn	Ga, d	420	2.5
Ga ₂ ZnO ₄	Ga, d	500	2.6
Ga ₂ O ₃ (am)	d	500	3.5
Ga ₂ O ₃ :Sn (am)	Sn, d	500	2.9
Ga ₂ O ₃ :Ti (am)	Ti, d	580	1.6
Ga ₂ O ₃ (cr)	d	660	0.4*

(c)

Figure 8.2: $J - V$ curves of the best result of the 64 solar cells on each sample with a new buffer layer. CIGSe absorbers from **a)** the first CIGSe deposition run **b)** the second CIGSe deposition run. **c)** Overview of the $J - V$ curve parameters. The first group are Ga₂O₃-free layers, the second group are Ga₂O₃ alloy layers, the last group are pure Ga₂O₃ layers.

* The efficiency values marked by the star are around two times lower compared to the others, due to a qualitatively worse CIGSe layer. However, the V_{OC} values are comparable.

ZnMgO:Ga, ZnO:Ga and (Zn,Ga)O_x. Thus, it is unlikely, that shunting causes the non-rectifying behaviour. A possible explanation could be a tunnelling contact between these oxide layers and the CIGSe. Based on the device model described in Sec. 7.1, this requires a high electron density in the TCO and high acceptor density at the TCO/CIGSe interface.

The samples with buffer layers based on Ga₂O₃ rich alloys do show a rectifying behaviour, and exhibit a V_{OC} larger than zero. Ga₂O₃ is known to reduce the charge carrier density and reduce the electron affinity within alloys, which makes a tunnelling contact to CIGSe more unlikely. The highest V_{OC} is achieved by the crystalline Ga₂O₃ layer, which suffers from a poor J_{SC} though. The crystalline Ga₂O₃ and also the crystalline ZnSnGaO_x films lead to poor adhesion of the CIGSe layer onto the substrate.

Alloying Ga₂O₃ with Ti leads to $J - V$ curves similar to those with pure Ga₂O₃, but exhibit a slightly lower short circuit current. The same occurs when doping Ga₂O₃ with Ti in the concentration range below 1 at.%. The optical measurements, showed that alloying with Ti at 200°C does not effect the band gap value, despite the fact, that the band gap for pure TiO₂ is 3.2 eV. Pure TiO₂ samples lead to non-rectifying $J - V$ curves. Alloying Ga₂O₃ with Zn leads to non-rectifying devices. Interestingly this is not the case for the buffer layer deposited from a single Ga₂ZnO₄ target, which leads to very similar $J - V$ curves as the pure Ga₂O₃ layers, again with a slightly lower J_{SC} . Alloying Ga₂O₃ with Sn leads to a strong electron barrier not allowing any current transport within the studied voltage range. Doping with Sn, in the concentration range below 1 at.% leads to a reduction of the photo-current. Alloying Ga₂O₃ with Sn and Zn also reduced the photo-current and for higher Ga concentration (above 50 at.%) a strong electron barrier develops. Similar behaviour was observed for the amorphous and crystalline ZnSnGaO_x layers. Alloying Ga₂O₃ with In leads to a reduction of the V_{OC} while the J_{SC} remains the same as for the pure Ga₂O₃. The details are shown in Fig. 8.4d.

In summary, amorphous and undoped Ga₂O₃ was found to perform best as a buffer layer compared to the other oxides testes in this experiment. Doping and alloying Ga₂O₃ with Ti or Sn lead to lower J_{SC} values. Alloying with In leads to lower V_{OC} values. All materials not based on Ga₂O₃ lead to non-rectifying devices.

The positive result is, that the efficiency of 3.5% was achieved without sodium addition and without optimisation of the CIGSe deposition process. The next section will therefore analyse the properties of the Ga₂O₃ layer and the corresponding solar cells to understand the limitations.

8.4 Amorphous Ga₂O₃ buffer

To understand the limitations of the ZnO/a-Ga₂O₃/CIGSe device presented in the previous section it is necessary to study electronic properties of the amorphous Ga₂O₃. This will be done in detail in Sec. 10.1 and some of the obtained results are shown here. Fig. 8.3 shows the charge carrier density, N_{D,GaO_x} , and the electron affinity, χ_{GaO_x} , of a-Ga₂O₃ in dependence of the a-Ga₂O₃ deposition temperature. The charge carrier density was

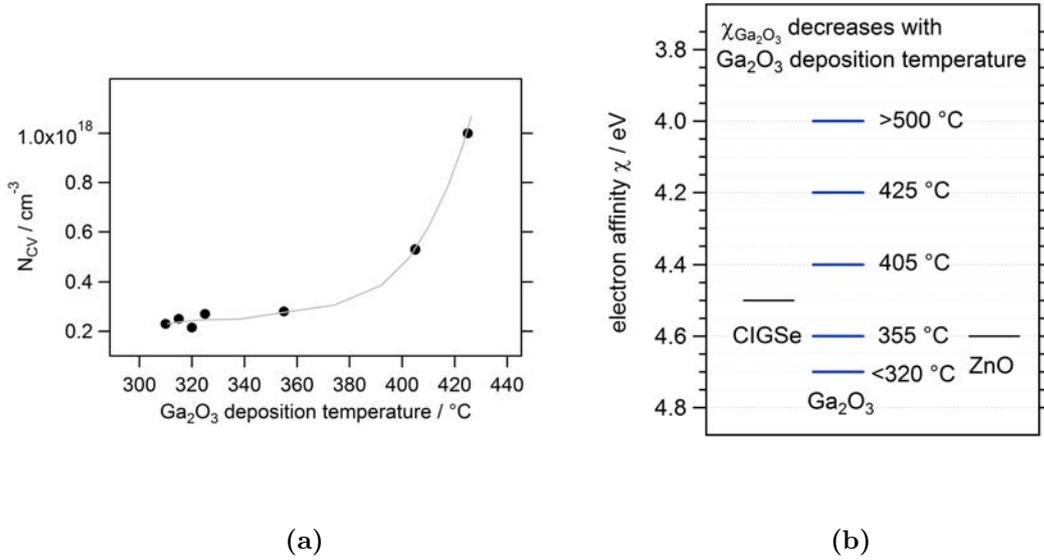


Figure 8.3: **a)** Charge carrier density within the Ga_2O_3 layers, measured with $C-V$ technique at 1 kHz and 298 K, **b)** Comparison of the electron affinities of CIGSe and ZnO (both taken from literature) with the assumed electron affinities of the different Ga_2O_3 layers. Based on the literature value for the crystalline phase (4 eV) and the assumption that the decreasing optical band gap with decreasing deposition temperature is due to an increasing electron affinity (see Sec. 10.1). The error of determining χ is estimated to be ± 100 meV. Best conduction band alignment is achieved at a Ga_2O_3 deposition temperature between 355 and 405 $^\circ\text{C}$.

measured by $C - V$ at 1 kHz, therefore it has to be interpreted as the maximum charge carrier density, since at this frequency deeper defects can contribute to the capacitance which do not contribute to the free carrier density.

For deposition temperatures below 320 $^\circ\text{C}$ both properties, charge carrier density and electron affinity, are independent of the deposition temperature, with $N_{D,\text{GaO}_x} = 2 \times 10^{17} \text{ cm}^{-3}$ and $\chi_{\text{GaO}_x} = 4.7 \text{ eV}$. Interestingly both properties change once the deposition temperature becomes larger than 320 $^\circ\text{C}$, N_{D,GaO_x} increases and χ_{GaO_x} decreases (Fig. 8.3). As will be discussed in depth in Sec. 10.1, this is attributed to an oxygen vacancy defect band present in the low temperature deposited Ga_2O_3 films. At 405 $^\circ\text{C}$ the values are $N_{D,\text{GaO}_x} = 5 \times 10^{17} \text{ cm}^{-3}$ and $\chi_{\text{GaO}_x} = 4.4 \text{ eV}$. This comes close to the optimum properties for a buffer layer in CIGSe superstrate devices.

Fig. 8.4a show the effect of the Ga_2O_3 deposition temperature on the device performance. The device with the Ga_2O_3 layer deposited at a temperatures of 360 $^\circ\text{C}$ exhibits an increased series resistance and a strongly reduced photo-current compared to the devices with Ga_2O_3 layer deposited at lower temperatures. This indicates a barrier at the hetero-interface, likely induced by the reduced $\chi_{\text{Ga}_2\text{O}_3}$. However, according to the results shown in Fig. 8.3b $\chi_{\text{Ga}_2\text{O}_3}$ should not differ more than 300 meV from χ_{CIGSe} , which would be required to induce an electron barrier. The reason for the electron barrier induced by a

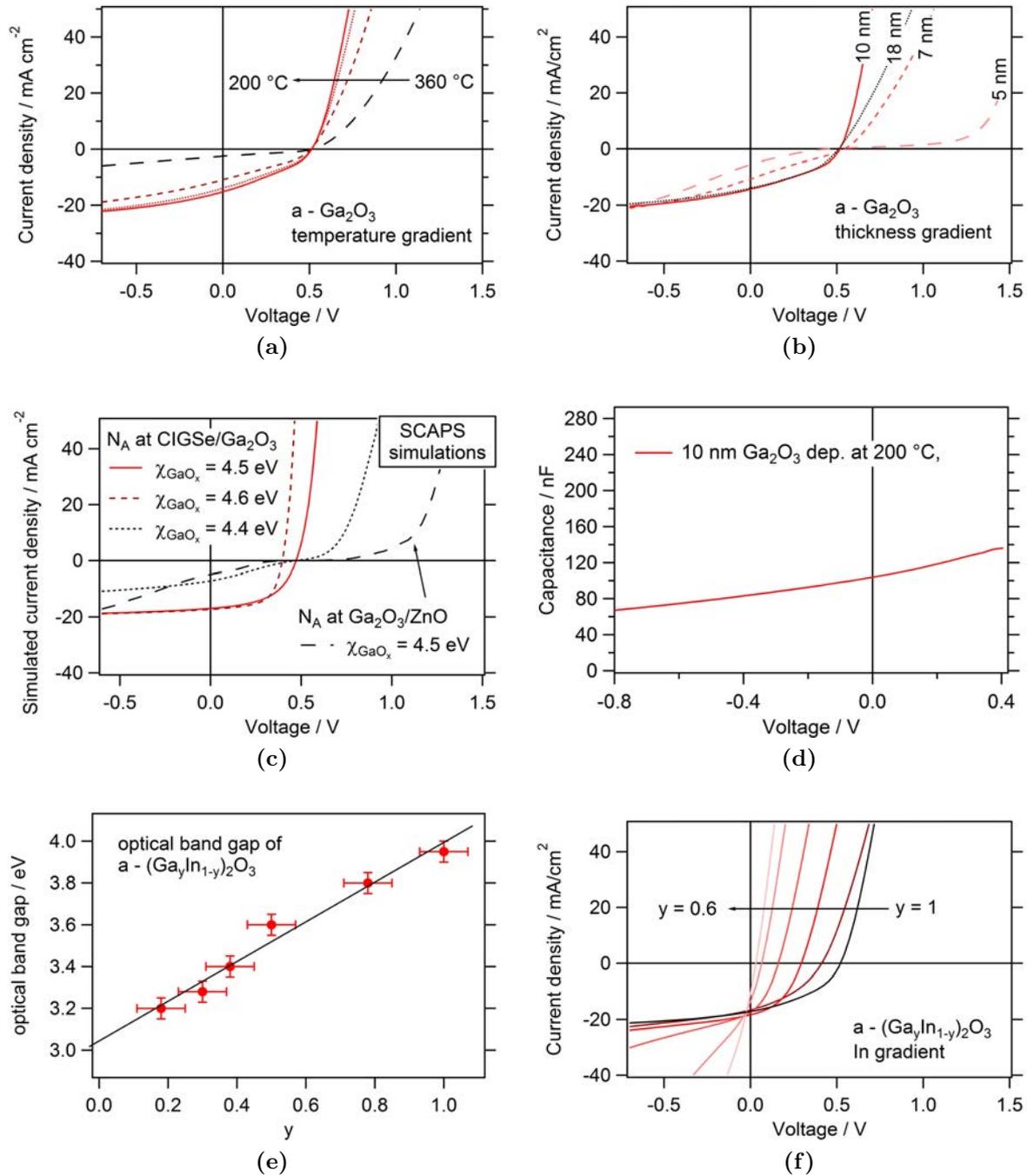


Figure 8.4: **a)** $J-V$ curves of CIGSe superstrate devices with $\text{a-Ga}_2\text{O}_3$ buffer layers deposited at varying temperatures and 1.3×10^{-3} mbar O_2 partial pressure. **b)** $J-V$ curves for different thickness but constant temperature of 200°C . **c)** Simulated $J-V$ curves for different $\chi_{\text{Ga}_2\text{O}_3}$ and different position of the acceptor states with the density N_A . **d)** Experimental $C-V$ curve. **e)** Optical band gap of $\text{a-(Ga}_y\text{In}_{1-y})_2\text{O}_3$ buffer layers with varying y value deposited at 100°C and 1.3×10^{-3} mbar O_2 partial pressure. **f)** $J-V$ curves of CIGSe devices with $\text{a-(Ga}_y\text{In}_{1-y})_2\text{O}_3$ buffer layers and varying y value.

small change of $\chi_{\text{Ga}_2\text{O}_3}$ requires a high density of charged acceptor states at the interface, similar as already observed for the CIGSe/ZnO system. The $C - V$ profile is a flat curve at a high capacitance value of around 100 nF for all applied voltages (shown in Fig. 8.4d). This is typical for Fermi level pinning at the CIGSe/TCO interface as shown in Fig. 3.3b. A fit to the experimental $J - V$ curves indeed requires a high acceptor density at the CIGSe/Ga₂O₃ interface. The simulation results are shown in Fig. 8.4c. Slight changes of $\chi_{\text{Ga}_2\text{O}_3}$ can well reproduce the experimentally observed variations, when assuming a high acceptor density at the CIGSe/Ga₂O₃ interface ($N_A=7e+12 \text{ cm}^{-2}$, 0.35 eV above $\text{VBM}_{\text{CIGSe}}$, $\sigma_{n,h}=1e-15 \text{ cm}^2$).

Another interesting observation is the dependence on the layer thickness. Fig. 8.4b shows the $J - V$ curves of the Ga₂O₃ layer with varying thickness values. The 10 nm thick layer leads to the best results, thicker layer increase the series resistance due to the low conductivity of the Ga₂O₃ layer. Surprisingly, layers thinner than 10 nm lead to a strong electron barrier, which becomes noticeable from the s-shaped $J - V$ curves. Also the $C - V$ curves (not shown) show a strong increase of the capacitance at forward bias, which indicate that the s-shape is due to acceptor states at the Ga₂O₃ interface. The asymmetry of s-shape can indeed be simulated by the model of acceptor states at the buffer/TCO interface discussed in Sec. 3.2 and shown in Fig. 3.3d and Fig. 3.4f. The simulation results in Fig. 8.4c are based on acceptor states at the Ga₂O₃/ZnO interface, with $N_A=3e+12 \text{ cm}^{-2}$, 1 eV below CBM_{ZnO} , $\sigma_{n,h}=1e-19 \text{ cm}^2$.

To fully control $\chi_{\text{Ga}_2\text{O}_3}$ it is interesting to alloy Ga₂O₃ with In₂O₃. Fig. 8.4d shows that the band gap of the amorphous (In,Ga)₂O₃ decreases almost linearly from 4 eV to 3 eV with increasing In content. According to the anion rule, the VBM remains constant for similar oxides independent of the cations, thus the electron affinity can be increased by 1 eV due to alloying Ga₂O₃ with In₂O₃. This is confirmed by the reduction of the V_{OC} with increasing In content (Fig. 8.4e), which tells increased interface recombination due to an increased CBM cliff.

8.5 Summary of and Outlook for improvement strategies

The parameter evaluation of the superstrate devices studied in this thesis shows that the research priority should be on novel buffer layers, which reduce the acceptor defect density at the hetero-interface. This section tested new oxide buffer layers, which were chosen by considerations based on their electron affinity and chemical stability. A summary of the obtained results is given here:

1. **Combinatorial material exploration:** Different oxide materials, many of them based on Ga₂O₃ alloys, were tested as the buffer layer in CIGSe devices. Amorphous Ga₂O₃ led to the best device performance. Doping and alloying attempts did not improve the performance. This indicates, that additional mid-gap states are introduced by the dopants, resulting in an increased interface recombination veloc-

ity. New experiments at elevated temperatures could help to improve the doping efficiency.

2. **Amorphous Ga₂O₃:** It was shown that the electron affinity and the charge carrier density of amorphous Ga₂O₃ can be adjusted in the range of 700 meV by the deposition temperature and by alloying with In₂O₃. In principle this allows a material design, which comes close to the criteria for an optimal buffer layer.
3. **Acceptor states:** Despite the well suited properties of amorphous Ga₂O₃, device simulations suggest, that the devices utilizing amorphous Ga₂O₃ as the buffer layer, suffer from acceptor type defects positioned mainly at the CIGSe/Ga₂O₃ interface. For a Ga₂O₃ layer thickness below 10 nm, the device model suggests acceptor states at the Ga₂O₃/ZnO interface. This would indicate the Cu diffusion to the ZnO interface for thin Ga₂O₃ layers.
4. **Sulphur gradient:** It was shown, that an In₂S₃ precursor can be used to introduce a sharp sulphur gradient at the hetero-interface. However, as long as the acceptor density at the hetero-interface is not compensated, an additional band gap increases the electron barrier at the hetero-interface further. Nevertheless, such a well defined sulphur gradient may allow highly efficient devices once a suitable new buffer layer is found.

Outlook: Two options are suggested to overcome the limitations by future research work. First, compensating the acceptor states by increasing the *n*-type doping of the amorphous Ga₂O₃ to above $1e+19\text{ cm}^{-3}$, or secondly, to find a material which is tolerant to Cu and a Cu diffusion barrier at the same time.

The first option is to sufficiently increase the *n*-type doping in amorphous Ga₂O₃. One way to do this is to increase the deposition temperature to 425 °C, as it was shown in Fig. 8.3a. At this temperature the layer is still amorphous but the *n*-type doping is increased. At the same time this decreases the electron affinity to around 4.2 eV, which can be shifted back to 4.5 eV by alloying Ga₂O₃ with In₂O₃ to (In_{0.3}Ga_{0.7})₂O₃. The higher In content in combination with the increased deposition temperature leads to a better dopability of the oxide. Instead of using Sn as the dopant, Si should lead to more shallow donor states which would allow more efficient *n*-type doping [159]. Thus amorphous (In_{0.5}Ga_{0.5})₂O₃:Si deposited at 425 °C has the potential to reach charge carrier densities of $2e+19\text{ cm}^{-3}$ and is proposed as a buffer layer material for new experiments.

However, a general problem of oxides is, that the valence band is formed by O *2p* orbitals, which are energetically close to the Cu *3d* orbitals, leading to a hybridization of the O *2p* and the Cu *3d* orbitals to binding and non-binding states. The binding states lie deep within the band gap, where they form a band structure as in the *p*-type CuGaO₂, or, if Cu is present as an impurity, they induce a compensation of the *n*-type doping. Thus it may be necessary to switch from oxides to nitrides. Within integrated circuits the use of nitrides as TiN, TaN or TiZrN as a Cu diffusion barrier is standard [165]. TiN, TaN and GaN have suitable work functions [166] and can become *n*-type doped by

nitrogen vacancies. In case of GaN, the formation of GaO_x was reported to occur only at temperature above 540°C [167]. Thus, this could be a successful future research direction.

In summary, the outlook of superstrate CIGSe devices depends on whether or not a suitable buffer layer can be found. However, if this is possible, the ability to produce very thin CIGSe absorber with a steep S and Ga gradient at the front and back interface respectively, should lead to highly efficient devices. The following design of the future CIGSe solar cell in superstrate configuration is proposed:

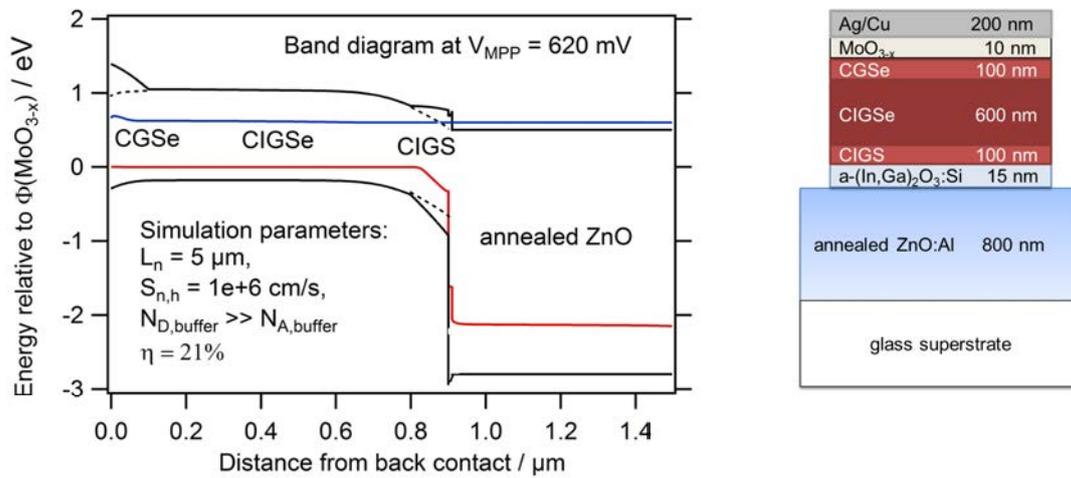


Figure 8.5: Energy band diagram and schematic illustration of the proposed ideal superstrate solar cell. A Ga gradient at the back contact reduces back contact recombination, S gradient at the front reduces interface recombination. A thin CIGSe absorption layer reduces the In consumption. The buffer layer is adjusted by the In/Ga ratio to the optimal CBM alignment. Annealed ZnO and $\text{MoO}_{3-x}/\text{Cu}$ or $\text{MoO}_{3-x}/\text{Ag}$ back contact lead to low electrical and optical losses. The simulated PCE is 21% for an assumed electron diffusion length of $5 \mu\text{m}$, compensated interfacial acceptor states and a high interface recombination velocity of $1\text{e}+6 \text{ cm/s}$.

Chapter 9

Summary and Conclusion

The growth of CIGSe absorbers onto TCOs is studied to achieve efficient CIGSe solar cells in the superstrate configuration. It is desired to reveal the factors which are limiting the device efficiency till date. In this work interface analysis by XPS and GDOES measurements, combined with device analysis by numerical simulations were used to establish this correlation for CIGSe layers co-evaporated onto ZnO layers. The results indicate that a general limiting factor of the superstrate devices is the Cu diffusion into the oxide materials.

Thermodynamic calculations predict the formation of Ga_2O_3 at the CIGSe/ZnO interface during the deposition of CIGSe onto ZnO or any other suitable oxides. Further, during the high temperature deposition process, Cu is shown to diffuse from the CIGSe layer into the oxide layer. From literature, it is known that Cu impurities induce acceptor states within ZnO and most other oxide materials. In this work, general device simulations have shown that these states if present at the hetero-junction, reduce the current collection efficiency and that the devices are very sensitive on the electron affinity of the oxide facing the CIGSe.

For the detailed interface analysis, ZnO was chosen as the oxide since it led to the best performing devices owing to its slightly larger electron affinity compared to CIGSe. The analysis shows that the composition of the interfacial layer between ZnO and CIGSe depends critically on the CIGSe deposition process. At low deposition temperatures, a 3 nm thin $(\text{Cu,In,Ga})(\text{O,Se})_x$ alloy forms. The Cu content induces acceptor state, the In content increases the electron affinity which reduces the V_{OC} . The In and Cu content can be reduced by increasing the deposition temperature, leading to a 6 nm thick GaO_x layer, which increases the V_{OC} and the device efficiency. However, the current collection is still limited by an extraction barrier for electrons caused by Cu induced acceptor states. At temperatures above 525°C , the Cu diffusion into the GaO_x increases, further reducing the current collection efficiency.

The formation of the interfacial oxide layer causes Zn diffusion into the CIGSe absorber. It is shown that the effect of the Zn contamination is detrimental for a concentration above 0.25 %, which is the case for devices fabricated at 525°C . The electron diffusion length

within the Zn contaminated devices is measured to be smaller compared to substrate devices. However, Na doping counteracts the negative effect of Zn contamination and increases the diffusion length to a value comparable to those in substrate devices.

Na was also found to catalyse the GaO_x formation if supplied as a precursor to the CIGSe growth. If it is supplied by a post-deposition it accumulates at the CIGSe/ GaO_x interface, without further catalysing the GaO_x formation. However, it induces additional acceptor states, which further reduce the current collection efficiency if present at high densities. The presence of Na at the hetero-junction further induces a reversible degradation of the device, which reduces the fill factor of the $J - V$ curves. Based on XPS and GDOES measurements, this is assumed to originate from Na migration out of the GaO_x layer. The Na migration is triggered by the strong electric field of the p/n -junction which is confined to the GaO_x layer. This could explain the need for voltage/light soaking of the previously reported superstrate devices.

Low-rate NaF post-deposition or diffusion through a thin Mo layer reduce the Na concentration at the interface while keeping the concentration in the bulk sufficiently high. This leads to stable efficiencies of up to 11 %, observed for the first time without the need of light or voltage biasing. Efficiencies above 10 % were also achieved by employing a $\text{MoO}_{3-x}/\text{Ag}$ back contact, which allows the substitution of the expensive Au contact. The back contact was shown to be slightly non-ohmic due to the Cu-poor back surface in superstrate devices. However, the presence of Na reduces its detrimental effect.

A 1-D model of the full device allowed a comparison of the solar cell parameters with a standard substrate device. The highest potential for efficiency improvement was found to be the reduction of the interfacial acceptor density, followed by a reduction of the interface recombination velocity.

To find a new suitable oxide buffer layer, which can solve these issues, a combinatorial material deposition approach was used to alloy Ga_2O_3 with other oxides to find the material with the optimum electron affinity, doping density and chemical stability. The best results were obtained with amorphous Ga_2O_3 as the buffer layer material, whose electron affinity was found to be comparable to the one of CIGSe. However, interfacial acceptor states were found to be present at the interface between CIGSe and GaO_x and the n -type doping density of the Ga_2O_3 layer was not sufficient to compensate these.

To overcome this problem, future research should focus on new buffer layers, as for example the development of an amorphous Ga_2O_3 layers with doping densities above $1 \times 10^{19} \text{ cm}^{-3}$. First experiments presented in this thesis indicate that this can be achieved by increasing the Ga_2O_3 deposition temperature, alloying it with In_2O_3 and doping it with Si. Alternatively, the material system for the buffer layer should switch from oxides to nitrides, as Cu may be less detrimental within nitrides.

Once a suitable new buffer layer is found, the application of a well defined sulphur gradient, as shown in this work, should reduce the interface recombination to achieve highly efficient devices. The speculated cost benefits of the superstrate configuration were shown to be realistic, as the ZnO annealing will allow 30 % thinner ZnO:Al layers while increasing the photo-current by 1.5 mA/cm^2 and the highly reflective back contact

will allow a CIGSe thickness reduction of 40 %. These factors could lead to a considerable reduction of material costs, electricity costs and process time of CIGSe modules.

Chapter 10

Additional Information

In this Chapter a more in depth study of the amorphous Ga_2O_3 , the sulphur gradient, the ZnO annealing, the MoO_{3-x} back contact and the CIGSe thickness reduction will be given. Beyond this, light scattering from etched ZnO layers and the CIGSe growth on ZnO will be addressed. Finally the paper on white light reflectometry (WLR) is shown.

10.1 Amorphous Ga_2O_3 characterization

Amorphous Ga_2O_3 lead to the highest device efficiency of the buffer layers tested within the combinatorial material exploration. This is especially remarkable, since the electron affinity for crystalline Ga_2O_3 is given in the literature to be around 4 eV [?], which is not suitable for CIGSe devices. Thus, in this section, the energy levels of the conduction and valence bands are approximated via a combination of transmission/reflection (T/R) spectroscopy, XPS and $J - V$ measurements. The oxygen content in the sample was measured by XPS. Further, Au/ Ga_2O_3 /GZO Schottky devices were fabricated to measure the charge carrier density and the Schottky barrier height between Au and Ga_2O_3 . The Ga_2O_3 layers were deposited by PLD on substrates which exhibited a temperature gradient. The oxygen partial pressure was set to $2\text{e-}5$ mbar for the samples with a temperature gradient from 425°C until 300°C and to $1.3\text{e-}3$ mbar for the samples with a temperature gradient from 160°C until 100°C . Thickness of the deposited layers were 10 nm on GZO substrates for the XPS measurements, 200 nm thick layers on GZO substrates for the Schottky devices and 200 nm thick layers on Quartz substrates for the T/R measurements.

Results

Band diagram Fig. 10.1a shows the square of the absorption coefficient of Ga_2O_3 layers, obtained from the T/R measurements. For direct band gaps, the value of the band gap E_g can be extracted from a linear extrapolation of α^2 to zero [168]. It is found, that the band gap correlates strongly with the substrate temperature, at 425°C the band gap is 4.5 eV and at 320°C around 4 eV. For temperature below 320°C the band gap remains at

4 eV, for temperatures above 450 °C, the Ga₂O₃ crystallizes and the band gap becomes 4.7 eV, which is the literature value for crystalline Ga₂O₃ [169].

Fig. 10.1c shows the valence band XPS spectrum for a sample deposited at 425 °C and a sample deposited at 100 °C. The onset, at the binding energy of around 4 eV, originates from electrons energetically located at the VBM. Thus, the binding energy at the onset gives the distance between the valence band maximum and the Fermi level E_F . For the 425 °C sample this difference is 4.5 eV and for the 100 °C sample it is 4.15 eV. These values are very similar to the optical band gap of 4.5 eV and 4.0 eV, respectively, which tells, within the uncertainty of the measurement, that the E_F is located close to the CBM. The GaO_x must therefore have a high degree of n-type doping.

This is indeed confirmed by the charge carrier density extracted from $C - V$ measurements at 1 kHz and shown in Fig. 10.2a. For substrate temperatures around 300 °C and below, the measured charge carrier density within the Ga₂O₃ is around $3 \times 10^{17} \text{ cm}^{-3}$. It increases with increasing temperature until $1 \times 10^{18} \text{ cm}^{-3}$ at 425 °C. The difference between the Fermi level and the CBM can be calculated from the measured charge carrier density, which is 20 meV for $1 \times 10^{18} \text{ cm}^{-3}$ and 50 meV for $3 \times 10^{17} \text{ cm}^{-3}$.

The small discrepancy observed between the optical band gap and the XPS data for VBM- E_F can be explained by the surface sensitivity from the XPS measurement compared to the T/R measurement. XPS probes only the first few nanometres and the band gap at the surface is likely to differ from the band gap in the bulk. The general trend of the VBM- E_F value is however the same as for E_g , as can be seen in Fig. 10.1d. Both values start increasing at substrate temperatures above 320 °C.

If the band gap change is due to a change of the electron affinity, which is the energetic distance of the CBM to the vacuum level, the work function will change accordingly, which is the difference between the Fermi level and the vacuum level, and with-it the Schottky barrier between Ga₂O₃ and Au will change. And indeed, for Ga₂O₃ layers deposited at an increased temperature the $J - V$ curves of the Au Schottky devices in Fig. 10.1b show a strong shift of the injection current to larger voltages, which has to be due to an increased Schottky barrier. Thus it can be concluded that the change in the band gap is due to a change of the electron affinity.

The highest reported charge carrier density for the crystalline β -Ga₂O₃ is also $1 \times 10^{18} \text{ cm}^{-3}$. To check whether the observed change in the free carrier density is correlated to the oxygen vacancies, XPS measurements were performed and the ratio of the Ga 2p and the O 1s peak intensities are plotted against the deposition temperature in Fig. 10.2a. Two plateaus can be observed, one at lower oxygen concentration for the lower temperatures and one at higher oxygen concentration for the higher temperatures. The transition temperature is 320 °C, which is also the temperature where the band gap, Fermi level and charge carrier density start to rise. Fig. 10.2b correlates band gap and the charge carrier density with the oxygen to gallium ratio. It can be approximately described with an exponential function.

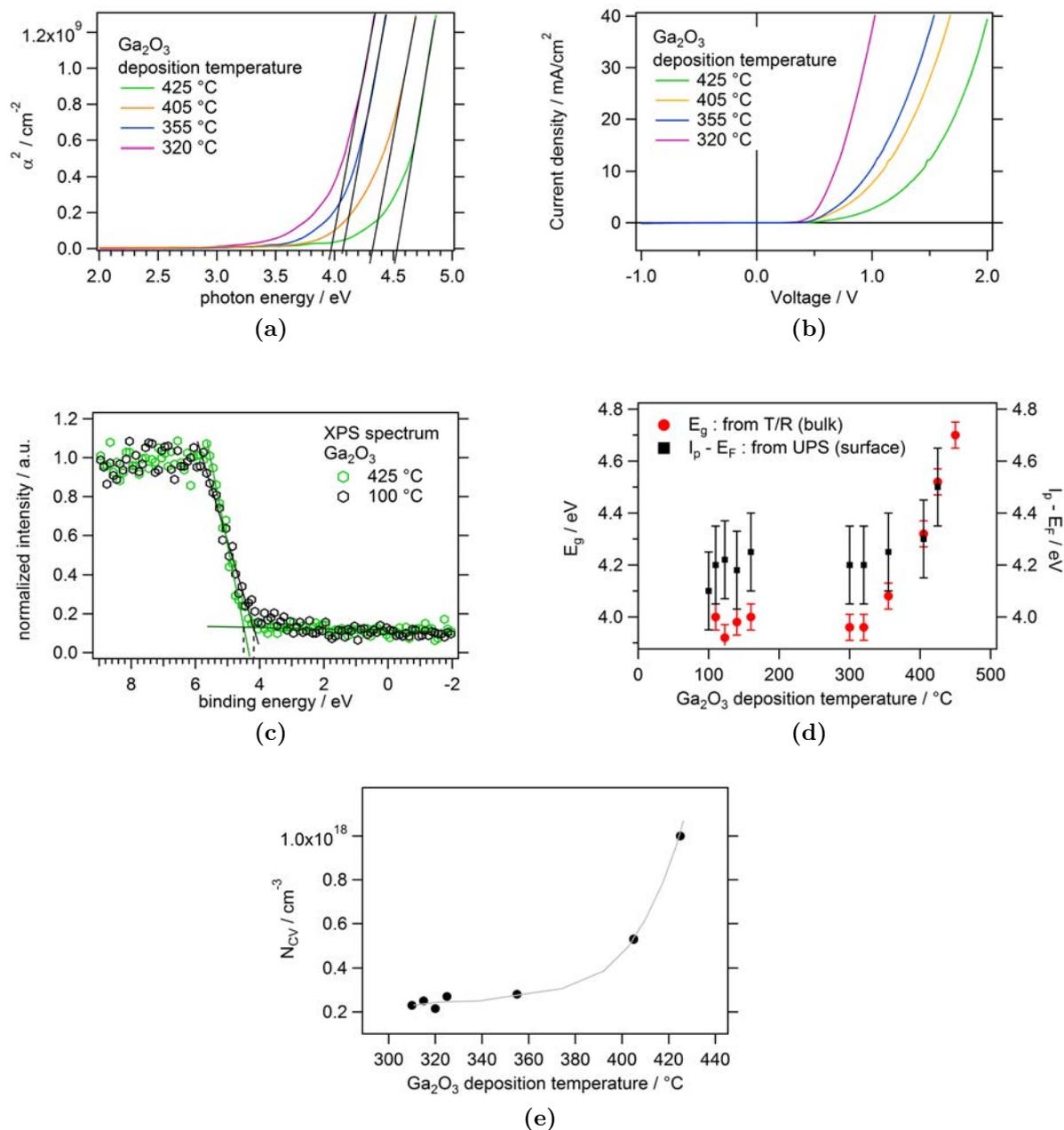


Figure 10.1: **a)** Square of the absorption coefficient of Ga_2O_3 layers deposited at different temperatures. The linear extrapolation until $\alpha^2=0$ gives the optical band gap, E_g . **b)** $J - V$ curves of $\text{Au}/\text{Ga}_2\text{O}_3$ Schottky devices, with the Ga_2O_3 layers deposited at different temperatures **c)** XPS spectra of two Ga_2O_3 layers. The VBM onset ($I_p - E_F$) varies with different deposition temperatures. **d)** $I_p - E_F$ and E_g plotted over the deposition temperature. Both follow the same trend, showing that mainly the conduction increases with increasing deposition temperature. **e)** Charge carrier density within the Ga_2O_3 layers measured with $C - V$ technique at 1 kHz and 298 K.

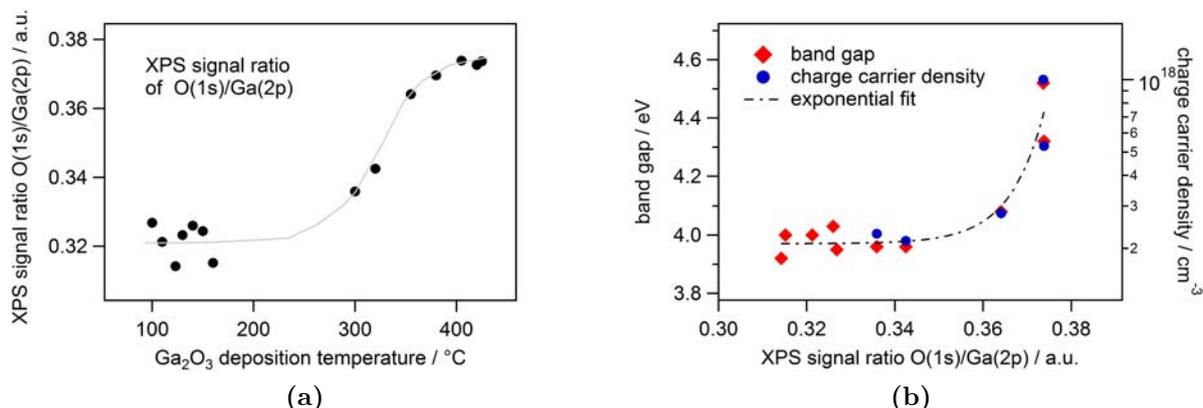


Figure 10.2: **a)** Relative oxygen concentration between the samples given by the ratio of the XPS intensities of Ga 2p and O 1s peaks. **b)** Correlation of the O to Ga ration with the band gap and the charge carrier density.

Sn doping To compensate the potentially present acceptor states created by the Cu and Na diffusion during the CIGSe deposition it may be necessary to further *n*-type dope the Ga₂O₃. The best reported results with a charge carrier density of $1.44 \times 10^{19} \text{ cm}^{-3}$ have been achieved by doping with Sn [160]. No reports exist so far on doping amorphous Ga₂O₃. Fig. 10.3 shows the measured charge carrier density, extracted from *C* – *V* measurements at 1 kHz, plotted over the Sn concentration. The measurements were performed on a sample deposited at 100 °C with a Sn Gradient varying from 0.2 % until 0.9 %. The Sn concentration was estimated from the ratio of the SnO₂ to Ga₂O₃ ablation pulses, weighted with the deposition thickness per pulse for SnO₂ and Ga₂O₃. The measured charge carrier density increases almost linear with increasing Sn concentration from $2 \times 10^{17} \text{ cm}^{-3}$ as measured for undoped Ga₂O₃ until $1 \times 10^{18} \text{ cm}^{-3}$ at a Sn concentration of 0.6 %. For Sn concentrations above 0.6 % the charge carrier density drops again, possibly due to the formation of SnO₂ phases.

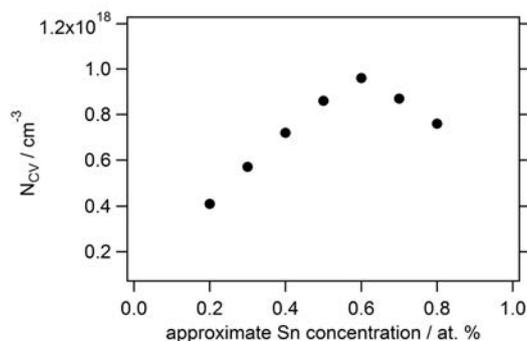


Figure 10.3: Charge carrier density within the Ga₂O₃ layers measured with *C* – *V* technique at 1 kHz and 298 K.

Discussion

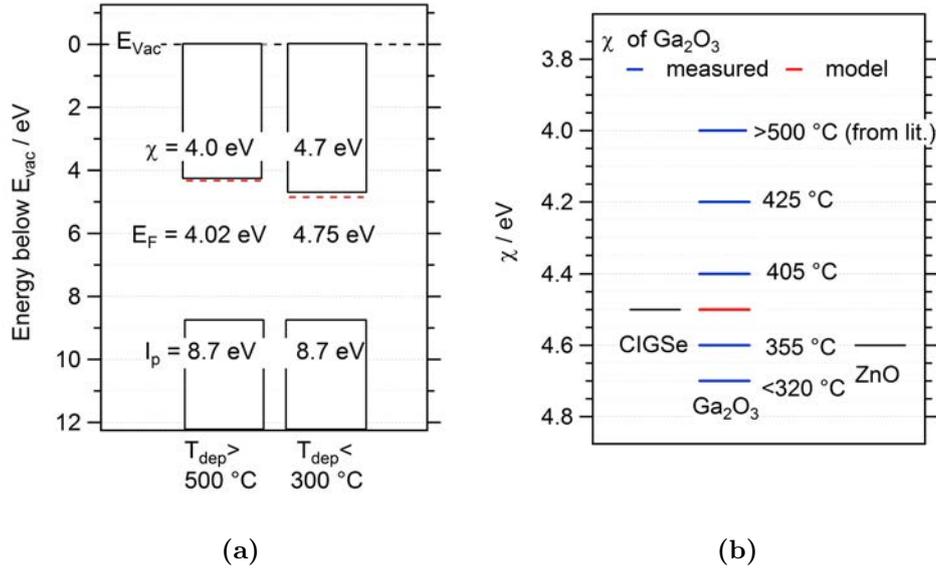


Figure 10.4: **a)** Energy band diagram for Ga_2O_3 layers deposited at substrate temperatures of 450°C and 100°C . Values for I_{p} , E_{g} and E_{F} were obtained from XPS, T/R and $C - V$ measurements, respectively. The error of determining χ is estimated to be ± 100 meV. **b)** Comparison of the electron affinities of CIGSe and ZnO with the electron affinities of the different Ga_2O_3 layers. Best conduction band alignment is achieved at a Ga_2O_3 deposition temperature around 400°C .

From the optical measurements it is clear that the band gap increases with increasing deposition temperature and the Schottky devices have shown that this shift is due to a decreased electron affinity. The increase of the electron affinity with increasing deposition temperature goes along with an increase of the charge carrier density. Both properties are correlated with the oxygen to gallium ratio, shown in Fig.10.2b. It appears, that the band gap and the charge carrier density increases exponentially with the oxygen to gallium ratio until a certain ratio for the crystalline films. It is likely, that this ratio equals the point of stoichiometry, which is $\text{O}/\text{Ga}=1.5$. From this it would follow, that the band gap drops exponentially with the oxygen deficiency until it reaches a plateau for $\text{O}/\text{Ga}=1.42$. Thus 3% oxygen deficiency would be sufficient to reduce the band gap to 4 eV. This could be induced by a oxygen vacancy defect band. Theoretical calculations have estimated the V_{O} donor state to be around 1 eV below the conduction band [142]. Thus, it is likely that a defect band created by V_{O} donor states decreases the band gap by 700 meV compared to the stoichiometric crystalline film. Similar as it was reported for MoO_3 non-stoichiometric films [170].

From literature it is known, that the electron affinity of crystalline Ga_2O_3 lies at around 4 eV with the same optical band gap as observed in this study [?]. As it was found here, Ga_2O_3 layers deposited at lower temperatures exhibit smaller band gaps together with

smaller Schottky barriers to Au. From this correlation, it has to be assumed, that the band gap reduction is due to an increase of the electron affinity. The band diagram for the crystalline layer (from literature) and for the low temperature deposited amorphous layer is shown in Fig. 10.4a. This band diagram is valid under the assumption, that the band gap reduction is solely due to an electron affinity reduction. Fig. 10.4b shows the electron affinities for different temperatures in comparison to the literature value for CIGSe and ZnO.

The shift of the optical band gap of oxygen poor amorphous films were observed once before in [171], although from 5 eV to 4.8 eV. The films were deposited by electron-beam evaporation. In crystalline films, substoichiometry was also identified as the origin for strong sub-band gap absorption leading to opaque films [160]. This was argued to be due to the formation of Ga₂O phases. The presence of Ga₂O was identified by a shift of the O 1s XPS peak together with a strong sub-band gap absorption, leading to opaque films. Increasing the temperature to above 800 °C was argued to lead to the evaporation of the Ga₂O phase, since it has a low melting point of Ga₂O of 650 °C. If the oxygen partial pressure is set to values below 1 mbar at low temperatures around 100 °C, opaque films were observed as well.

Further, the charge carrier density derived from the C-V analysis showed an increase towards stoichiometry. Simulations with SCAPS show that donor defects below 700 meV do not contribute to the measured capacitance. Thus, the increase of the charge carrier density must originate from a different source. Conductivity in Ga₂O₃ is commonly explained by background impurities like hydrogen or silicon [142]. Doping the oxygen poor and amorphous Ga₂O₃ with Sn lead to an increase in a maximum increase of the free charge carrier density up to 1e+18 cm⁻³ for a Sn concentration of around 0.6 at.%. This is the same value as obtained for the stoichiometric undoped films prepared at higher deposition temperatures. It cannot be excluded, that Sn was present as a background impurity for the undoped films. However, the strong correlation of the charge carrier density, the band gap and the oxygen concentration indicate a certain mechanism, independent of the extrinsic dopants, responsible for these changes. Further studies need to be performed to fully understand this process.

Anyhow, the change of the electron affinity with the deposition temperature is important for the application in solar cells, since the difference of the electron affinities at hetero-interface should be small to allow current transport, while keeping the interface recombination low. Fig. 10.4b compares the electron affinities of CIGSe and ZnO with them of the different Ga₂O₃ layers. The deposition temperature should be set around 400 °C to achieve optimum band alignment with CIGSe. These results show that amorphous Ga₂O₃ does not necessarily induces a charge transport barrier due to a CBM spike at the interface to CIGSe devices. How the electron affinity will be influenced by the CIGSe deposition is not know, however, the best fit to the experimental $J - V$ curves in Sec. 8.4 is achieved for $\chi_{\text{Ga}_2\text{O}_3} = 4.5 \text{ eV}$ for the low temperature deposited ($T < 320 \text{ °C}$) Ga₂O₃. It is marked in Fig. 10.4b as a red bar. The value fits very well to the results obtained here for the pure Ga₂O₃ layers deposited by PLD.

The properties of the GaO_x forming during the CIGSe deposition on ZnO are difficult to compare to the results given here, since the formation occurs completely different from the formation during a PLD deposition. Also the In impurities reduce the electron affinity. The device model used for the $J - V$ curve fitting in Sec. 7, lead to a value of 4.55 eV for the electron affinity.

10.2 Sulphur gradient

This section will explore the possibility of reducing the interface recombination by a local sulphur enrichment at the hetero-interface.

It was previously shown that low temperature CIGSe depositions lead to samples that are limited by interface recombination. As discussed in Sec. 3.1 one strategy to reduce the interface recombination losses is by increasing the band gap of the CIGSe at the hetero-interface, e.g. by sulphurization. The effect of the sulphurization on the energy band diagram is shown in Fig. 1.5b, the CBM is increased while the VBM is reduced. However, the device modelling in Sec. 7 indicated that in the current state-of-the-art superstrate solar cells the application of a sulphur enrichment at the hetero-interface cannot lead to an increased efficiency since the reduced CBM will not be sufficiently compensated by the band bending of the space charge region, leading to an increased electron barrier and increased bulk recombination. Thus, the successful application of a $\text{Cu}(\text{In,Ga})(\text{S,Se})$ layer at the hetero-interface requires an inverted CIGSSe at the p/n -junction, requiring new effective n -type buffer layers. Still, in order to analyse the potential of superstrate devices, it is important to know whether or not it is possible to create a local sulphur gradient at the hetero-interface.

Here, it is tested if an In_2S_3 precursor layer, deposited onto the $i\text{-ZnO}/\text{ZnO}:\text{Al}$ substrate prior to the CIGSe deposition, can achieve a sharp sulphur gradient. The In_2S_3 is deposited at 200 °C by thermal evaporation from an In_2S_3 powder. The layer thickness were 10 nm and 70 nm. The CIGSe absorber is deposited at 475 °C by the modified three stage process as described in Sec. 2.1. The resulting $J - V$ curves are shown in Fig. 10.5a.

As expected from the device model, the In_2S_3 buffer layer lead to an increased electron barrier, reducing the short circuit current and the series resistance, if the sulphur remains at the interface. Both effects are more pronounced for the thicker In_2S_3 precursor. However, this indicates that the sulphur atoms remain localized at the interface. Fig. 10.5b shows the GDOES depth profile. Two effects can be observed indeed. First, sulphur atoms diffuse only slightly into the CIGSe absorber, leading to a very effective sulphur gradient directly at the hetero-junction. Second, Ga accumulates at the sulphur rich areas. While the first effect is the desired effect, the second could lead to situation, where the CBM is increased too much due to the increases presence of S and Ga at the hetero-interface.

Too reduce this effect, a new CIGSe deposition approach is tested. Followed by the optional 50 nm of In_2S_3 precursor deposition, 900 nm of In_2Se_3 are deposited. Onto this

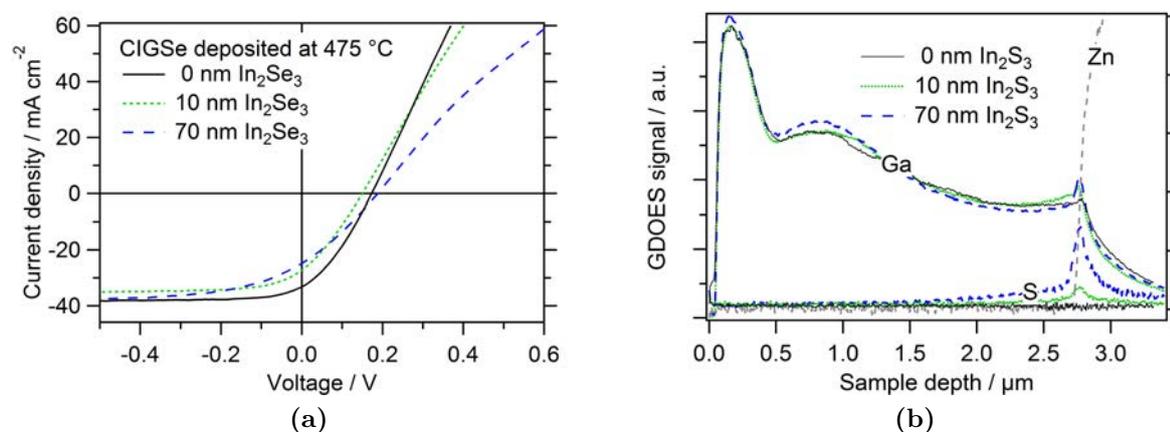


Figure 10.5: **a)** $J - V$ curve of devices with differently thick In_2S_3 precursors and a CIGSe layer deposited by the modified 3-stage process at 475 °C. **b)** The corresponding GDOES depth profile.

stack, Cu-Ga-Se is deposited at 420 °C. Due to the different diffusion constants of Cu and Ga, this leads to a depth profile as shown in Fig. 10.6b. While Cu is homogeneously distributed throughout the absorber, the Ga concentration at the hetero-interface is reduced to almost zero. By increasing the deposition temperature the Ga concentration could be increased as desired. The low temperature deposition leads to a low power conversion efficiency of 0.7% for the sample without the In_2S_3 precursor and 1.1% for the sample with the precursor. In this case, the sulphur gradient still induces an electron barrier, but also reduces the recombination losses, which leads to a higher V_{OC} . The generally poor performance is due to the missing GaO_x interfacial oxide layer.

Discussion It is expected that a sulphur gradient at the hetero-interface will reduce the interface recombination for well behaving devices with a inverted CIGSe layer close to the hetero-interface. New buffer layer will hopefully allow this in the future. As expected from the device model for the state-of-the-art superstrate solar cell, an enhanced sulphur concentration at the interface leads to an increased electron barrier and a decreased device efficiency. But, nevertheless, it was shown that it is possible to design a local sulphur gradient at the hetero-interface by applying a In_2S_3 precursor. The strong Ga accumulation due to the sulphur was reduced by a new deposition routine which allows good control over the Ga concentration at the sulphur rich interface. This is important, since the accumulation of S and Ga at the hetero-junction will induce an electron barrier.

10.3 Light management

As discussed in the first chapter, the big advantage of the superstrate structure is the advantageous light management due to the possibility to engineer the back contact, im-

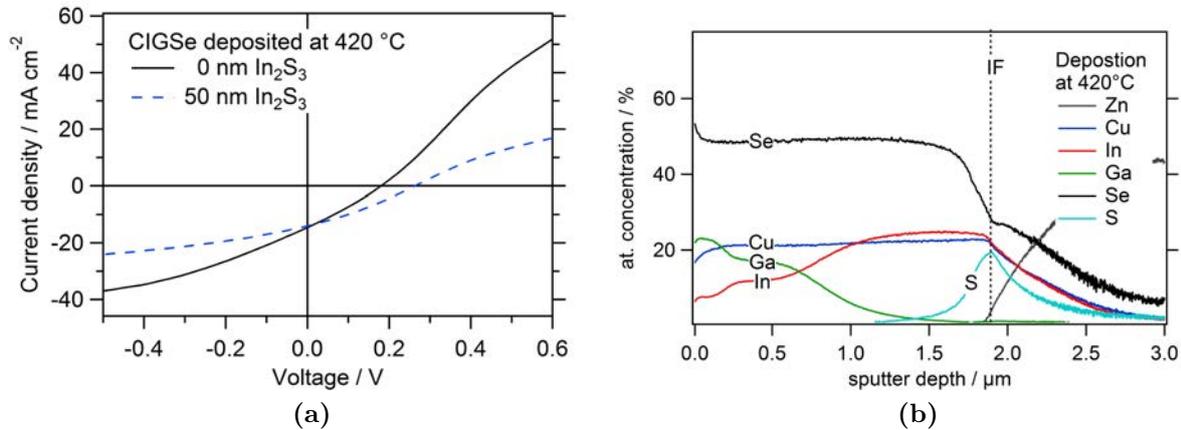


Figure 10.6: a) $J - V$ curve of devices with and without an In_2S_3 precursors and a CIGSe layer deposited by In-Se followed by Cu-Ga-Se at 420°C . b) The corresponding GDOES depth profile.

plement light scattering by ZnO etching and improving the ZnO transparency by annealing prior to the absorber deposition. This Chapter studies these three issues.

10.3.1 ZnO annealing

Annealing is supposed to improve the electrical and optical properties of ZnO. The best results reported in the literature so far, were achieved by capping the film with a-Si or SiO_x during annealing in a nitrogen atmosphere [17]. The question for the application in CIGSe superstrate devices is, whether vacuum annealing is sufficient and what happens to the ZnO during the deposition of CIGSe at high temperatures without any capping layer. To give an answer to this, first, the effect of vacuum annealing is studied, then the influence of the CIGSe deposition and then the applicability of the cap annealed ZnO.

Vacuum annealed ZnO

To evaluate the effect of vacuum annealing, as deposited ZnO:Ga layers were annealed at 250°C and at 500°C for 10 minutes in ultra high vacuum. The ZnO films were RF sputtered at 50°C from a Ga:ZnO target with 2 at.% Ga. The film thickness was 1200 nm. The mobility and free charge carrier density was measured by the Hall technique and also extracted from the optical transmission and reflection data, by fitting the spectra with an empirical model based on a Drude approach. The fitting procedure was developed from Pflug et al. within the RigVM environment [123]. The electrical and optical properties of the as-deposited and the annealed films are shown in Tab. 10.1.

Results The conductivity increases due to the annealing and with increasing annealing temperature the conductivity increases further. The results of the Hall measurements and the optical measurements show that the mobility increases together with the conductivity

whereas the free charge carrier density slightly drops. The optical analysis also shows a slightly decreasing density of free charge carriers with increasing annealing temperature.

Similar results were obtained by annealing in an oxygen atmosphere of $1.3\text{e-}4$ mbar. Only at an oxygen pressure of $1.7\text{e-}3$ mbar the conductivity decreased due to a strong reduction in free carrier density.

In addition to the observed increase in mobility a strong increase in the transparency of the ZnO in the region between the band gap absorption and the free carrier absorption can be observed. The optical band gap increases from 3.51 to 3.57 during the annealing. The average transparency in the range of 400-1000 nm is increased from 77% to 87%. For a typical band gap for CIGSe of 1.2 eV, the gain in photo-current is calculated to be 4 mA/cm^2 due to the increased transparency after the annealing.

The XRD pattern of the two films are shown in Fig. 10.8a. No change of the structural properties can be identified from the XRD pattern, which only shows the (002) peak. The (002) growth direction is preferentially orientated perpendicular to the glass substrate, as can be seen in the SEM image in Fig. 10.8b. Using the formula of Scherrer (Eq. 2.23 [97]), the domain size D can be calculated to 22 nm. Whereas an average grain diameter of around 60 nm can be estimated from the SEM picture in Fig. 10.8b.

Discussion The beneficial effect of vacuum annealing on ZnO was observed earlier in the literature. It was argued that the origin of the increased conductivity is due to an increase in charge carrier density from an increased oxygen vacancies density [172] or due to the activation of the Ga dopants [173]. The annealing effect described in both works did not come along with a reduced absorption, only a blue shift of the absorption edge due to the Burstein-Moss effect. This can be ruled out in the here presented case, since the charge carrier density does not increase during annealing.

An increase of mobility and transparency was observed by Yu et al. [174]. They argued, on the basis of temperature dependent Hall-effect measurements, that the mobility in as-deposited film is limited by grain boundary scattering, whereas the mobility in vacuum annealed sample was limited by thermal lattice vibration scattering. They observed an

Table 10.1: Electrical and optical properties of $1.2\text{ }\mu\text{m}$ thick Ga:ZnO samples prepared via RF sputtering on sodium free glass (Eagle 2000). The transparency is given for the ZnO/air interface and not corrected for the reflectivity. It is given for the wavelength range of 400-1000 nm. The charge carrier density and the mobility is also calculated from the T and R spectra with the drude model.

property	R_{sq}	G	T	n_e	μ_n	n_e	μ_n
unit	Ω	S/cm	%	cm^{-3}	$cm^2(Vs)^{-1}$	cm^{-3}	$cm^2(Vs)^{-1}$
method	4 point	v-d-Pauw	T/R	Hall	from Hall	T/R	T/R
as deposited	5.7	1590	77	$6.25\text{e}+20$	15.9	$5\text{e}+20$	16.7
250 °C anneal	3.9	2322	84	$5.56\text{e}+20$	26.1		
500 °C anneal	3.3	2746	87	$5.96\text{e}+20$	28.8	$4\text{e}+20$	21.5

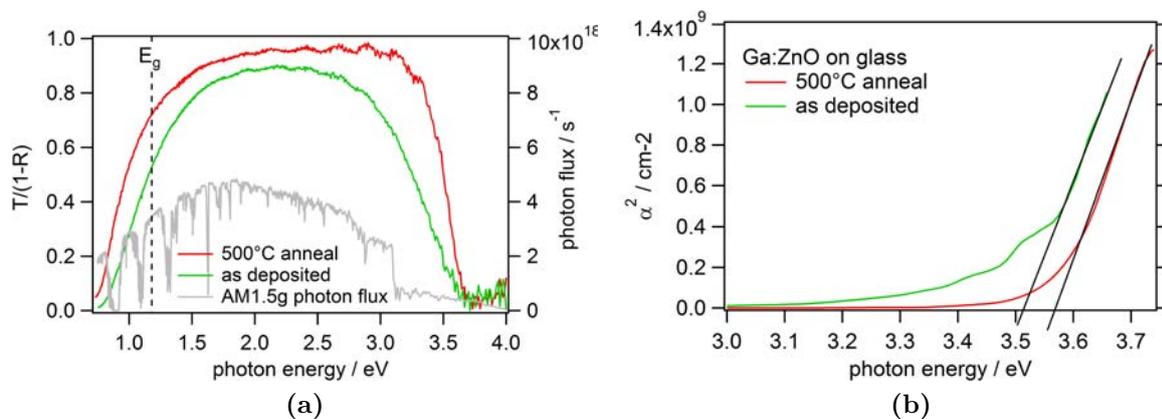


Figure 10.7: **a)** Transmittance corrected for the reflection, $T/(1-R)$, of the as deposited and the annealed ZnO layers on glass. The AM1.5g photon flux spectrum is shown as well. The typical band gap of CIGSe is marked by a dashed line. The gain in transparency leads to a gain in photocurrent of 4 mA/cm^2 **b)** Square of the absorption coefficient spectrum of the as deposited and the annealed ZnO layer. The optical band gaps are approximated to be 3.51 eV and 3.57 eV by a linear extrapolation until $\alpha^2 = 0$.

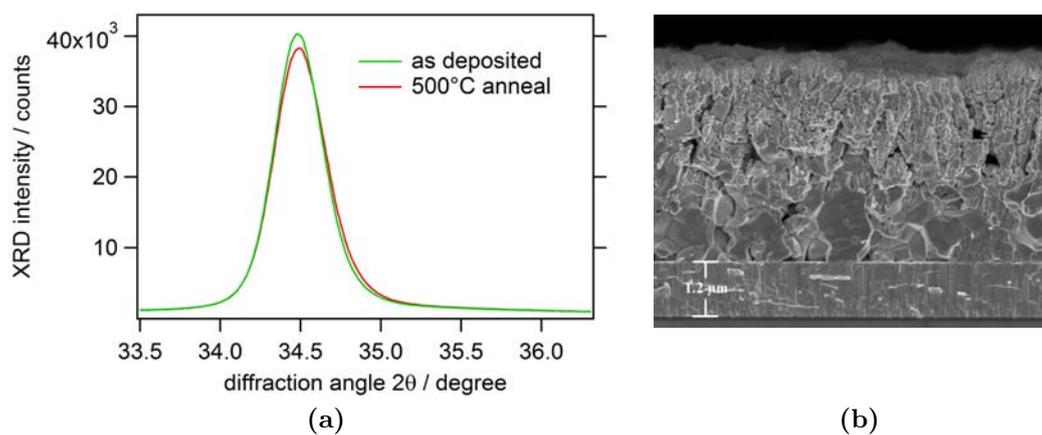


Figure 10.8: **a)** XRD pattern of the as deposited and the annealed ZnO layers on glass. Only the (002) peak is visible within the recorded angle range of $2\theta = 20 - 50^\circ$. No change of the pattern occurs due to the annealing. **b)** SEM image of the annealed ZnO covered with CIGSe.

increase in the dominant (002) XRD peak due to the annealing. An increase of the domain size is not observed in the here presented work, thus grain boundary scattering may not be the origin of the here presented annealing effect. Even though the amount of charged defects at the grain boundaries may change during the annealing, which could improve the current transport along the grains. Other reports like [175] [176] observed all of the effects also observed in this work, but did not give any explanation for the observations. Ruske et al. observed an increased mobility and reduced sub-band gap absorption during the annealing of capped ZnO layers inside a nitrogen atmosphere [17]. They showed that the sub-band gap absorption can be described with Urbach tails, which becomes reduced during the annealing [177]. It is assumed, that this is due to the reduction of structural disorder, partially caused by the dopant atoms.

In the layers studied here, the increased conductivity after the annealing is solely due to a higher mobility of the free charge carriers. This explains the reduced absorption in the infrared region, since the improved charge carrier mobility narrows the plasma absorption band. The annealing effect also comes along with a reduction of the light absorption close to the band gap and in the visible light range. This may be due to a reduction of the absorption from defect states. The fact, that the mobility increase was measured by Hall and by the optical technique further indicate, that the origin is a bulk effect, as the reduction of structural disorder as argued by Schönau et al.

In summary, the work presented here, an increased mobility in combination with reduced sub-band gap absorption is observed after the vacuum annealing. It is likely that the origin is the reduction of structural disorder induced by the Ga and Al dopants. The structural disorder could induce a strong tailing of the valence band, which leads to an increased sub band gap absorption and due to the scattering at the charged defects to an reduced mobility for the as-deposited films. The annealing leads to a better structural order which reduces these two effects.

ZnO annealing during CIGSe growth

The CIGSe deposition onto the ZnO layer has a similar annealing effect as the above described vacuum annealing. The sub band gap absorption of the ZnO decreases and the mobility increases, as shown in Fig. 10.9. The mobility increase at a constant charge carrier density was derived from a fitting procedure based on the Drude approach, and is therefore induced by a bulk and not grain boundary effect. Similar as for the vacuum annealing this is likely to be induced by a reduction of structural disorder. The average light absorption between 400 nm and 1100 nm is reduced from 10.7 % to 6.5 % which yields a photo-current increase of 1.5 mA/cm².

However, if sodium can diffuse into the ZnO during the CIGSe growth, the positive effect of the annealing cannot be observed. Fig. 10.12 shows the transmission and the photo-luminescence before and after the CIGSe deposition. Both sub-band gap absorption and photo-luminescence increase during the CIGSe deposition. This may be induced by sodium diffusion from the glass into the ZnO, forming the optical active defect Na_{Zn} [178] [179].

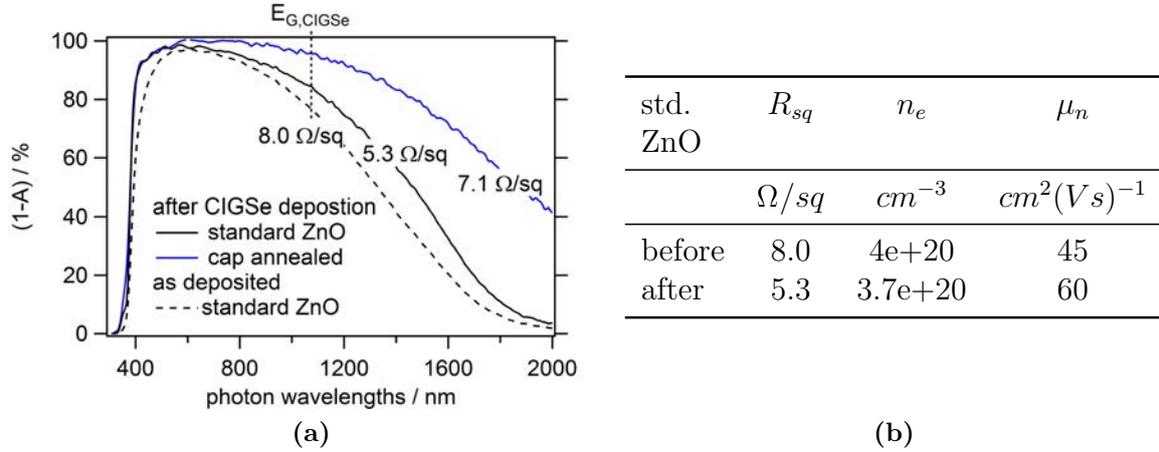


Figure 10.9: **a)** Transmission curves, corrected for the reflectance, of standard ZnO on sodium free substrate before and after the CIGSe deposition process at 525 °C. The corrected transmission is also shown for the cap annealed ZnO for comparison. **b)** Free charge carrier density and electron mobility of the standard ZnO samples extracted from T and R spectra using a fitting procedure based on a Drude approach, developed from Pflug et al. [123]

Non-vacuum annealed ZnO

Annealing outside of the vacuum usually leads to a degraded charge carrier density. However, in [17] it is reported, that the annealing step can be performed in a nitrogen atmosphere, if a thin capping layer of a-Si or SiO_x is deposited onto the ZnO:Al prior to the annealing in order to prevent the oxygen chemisorption. Following to the annealing step the capping layer is etched from the ZnO surface, resulting in ZnO:Al layers with high mobilities of up to 67 cm^2/Vs . This procedure is already successfully exploited in a-Si:H/ μc -Si:H solar cells [180], which improved the efficiency by an absolute gain of 0.7%. In this section it is studied, whether or not such cap annealed ZnO layers are suitable for CIGSe superstrate devices.

The $J - V$ curve of the best performing cap annealed ZnO layers in CIGSe superstrate devices fabricated at the standard temperature of 525 °C is shown in Fig. 10.10a. Compared to the standard as deposited ZnO, the V_{OC} is reduced by 150 mV. It is important to note that the cap annealed ZnO is deposited on sodium free Corning Eagle XG glass, whereas the standard ZnO is deposited on sodium containing soda lime glass. This leads to an accumulation of sodium at the hetero-interface as it is seen in the GDOES depth profiles shown in Fig. 10.11. Further, the Ga/Se ratio in Fig. 10.11 reveals, that at the interface between the CIGSe and the cap annealed sodium free ZnO less GaO_x forms compared to the standard ZnO. In Sec. 5.1.4 it was shown, that the sodium catalyses the GaO_x formation, which in turn was shown in Sec. 5.3 to reduce the interface recombination. This explains the reduced V_{OC} , which is solely due to the absence of sodium in the glass substrate.

The photo-current at negative voltage bias is increased by 4 mA/cm^2 compared to the standard ZnO with sodium. As it is seen in Fig. 10.12a, this is due to the higher

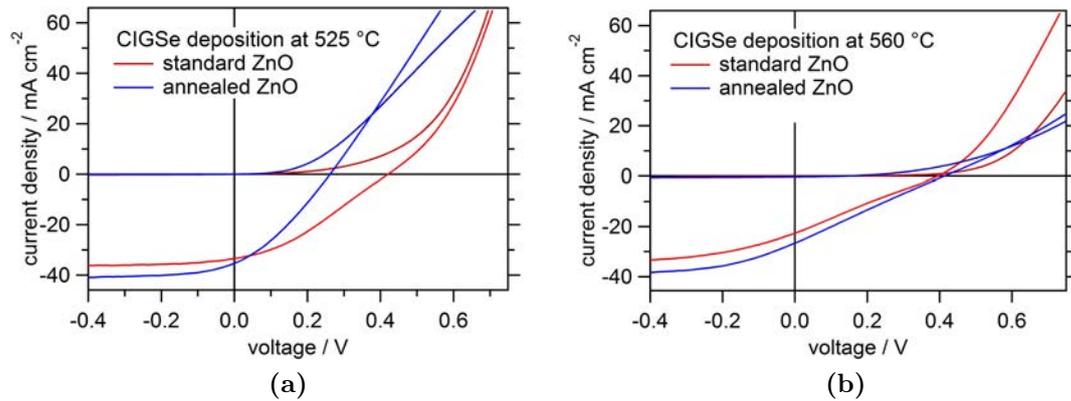


Figure 10.10: $J - V$ curves of CIGSe/ZnO devices with standard and annealed ZnO and a) CIGSe layer deposited at 525 °C b) CIGSe layer deposited at 560 °C.

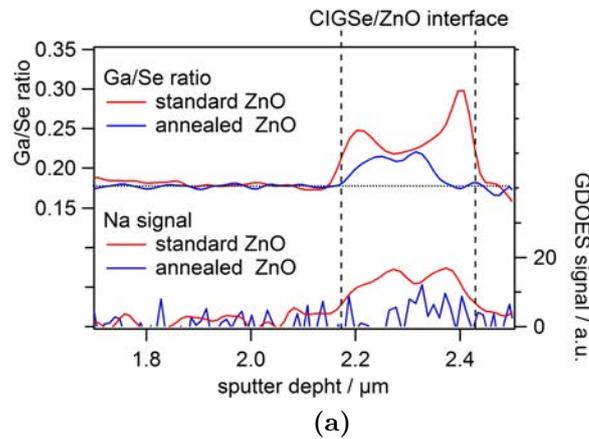


Figure 10.11: GDOES depth profile of the Ga/Se ratio and the uncalibrated sodium signal. The Ga/Se ratio increases at the interface, indicating the formation of GaO_x . The presence of sodium catalyses the interfacial oxide formation.

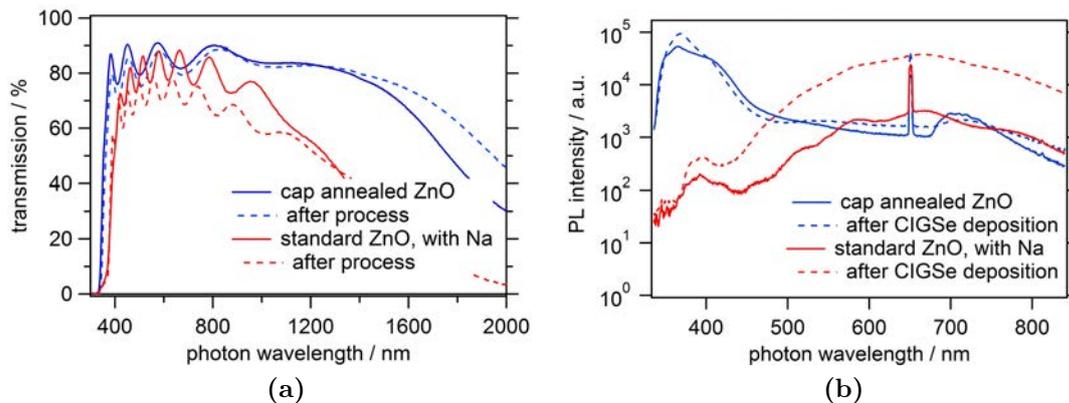


Figure 10.12: a) Transmission curves and b) PL spectra of standard and annealed ZnO before and after the CIGSe deposition process at 525 °C. The peak at 650 nm originates from the second harmonic

transparency of the cap annealed substrate. The lower sub-band gap absorption of the cap annealed ZnO layer is likely to be due to reduced defect absorption as discussed in the previous chapter for vacuum annealed ZnO. To check this, the PL spectrum of both ZnO layers were recorded and displayed in Fig.10.12b. The cap annealed ZnO has a pronounced band to band PL peak with minor defect induced PL intensity in the sub-band gap region. The PL spectrum of the standard ZnO shows a strong contribution of the defect PL peaks in the sub-band gap region with only little band to band radiative recombination. Thus it is likely that the lower sub-band gap absorptivity of the cap annealed film originate from a reduced defect concentration. As discussed in the previous chapter, this is believed to originate from structural disorder possibly induced by the dopants.

By cleaving the sample with the technique described in Sec.2.5.2 it was possible to measure the change in transmission and PL spectra due to the deposition of a CIGSe layer at 525°C. The results are shown in Fig.10.12a and b. The cap annealed ZnO shows an increased band to band PL signal, which indicates further improved structural order due to the high temperature CIGSe deposition. The infrared absorption is slightly reduced, indicating, that the charge carrier density become reduced during the CIGSe deposition, similar as for the vacuum annealed sample in the previous section. The sub-band gap absorption and sub-band gap PL intensity is slightly increased after the CIGSe deposition, which shows that the CIGSe deposition has a negative influence on the ZnO layer. However, the average light absorption between 400 nm and 1100 nm is still reduced from 6.5 % to 2.1 % which yields a photo-current increase of 1.6 mA/cm² compared to the sodium free ZnO annealed during the CIGSe deposition.

Summary

ZnO annealing in vacuum was shown to increase the electron mobility and decrease the defect absorption in ZnO layers. The increase in mobility was shown not to originate from structural changes or reduced grain boundary scattering, but from the reduced defect concentrations in the ZnO bulk. The same effect is on observed due to the CIGSe deposition onto as-deposited ZnO layers. However, the best ZnO properties were obtained from the cap annealed ZnO, even though the CIGSe deposition slightly deteriorates these. The vacuum annealing has the advantage, that it does not require any additional processing step, as the ZnO gets annealed during the CIGSe deposition. If sodium diffused from the glass into the ZnO layer, the annealing effect was not beneficial, but the defect absorption actually increased.

10.3.2 Highly reflective back contact

A major advantage of the superstrate configuration is the possibility to design the back contact in order to increase the reflectivity and decrease the recombination losses. This allows reducing the absorber thickness, which would increase the production speed and reduce the material costs. Possibly, it could even increase the efficiency, due to

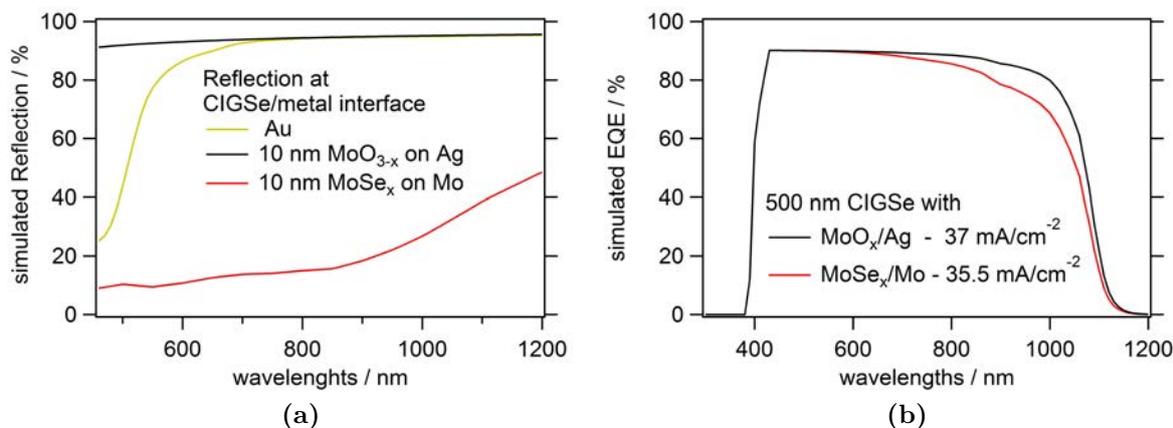


Figure 10.13: a) Calculated reflection at the interface between CIGSe and MoSe_x/Mo, MoO_{3-x}/Ag and Au. b) Simulated EQE spectra for a 500 nm thick CIGSe device with different back contacts and without recombination in the CIGSe bulk. A gain in short circuit current of 1.5 mA/cm⁻² can be achieved due to the highly reflective MoO_{3-x}/Ag back contact.

better charge carrier collection if high doping levels limit the SCR width within the CIGSe.

CIGSe devices in the substrate configuration utilize molybdenum as the back contact material, since it has the tendency to form a thin layer of MoSe_x during the CIGSe deposition, which is beneficial for the back contact quality [150]. The disadvantage of the Mo/MoSe stack is the very low reflectivity.

The calculated light reflectivity at the interface between CIGSe and the MoSe_x/Mo stack is shown in Fig. 10.13. The *n* and *k* values for CIGSe were taken from [181] and for the metals from [182]. The Reflectivity is between 20 and 40%, which leads to a reduced EQE in the infrared region for thin absorber layers, as shown in Fig. 10.13b. The reduced EQE translates into a short circuit current loss of 1.5 mA/cm⁻² for a 500 nm thin CIGSe layer, compared to a device with a highly reflective contact like Au. The high material costs of Au makes it no option for industrial application though. As shown in Fig. 10.14 alternative metals to Au are only Pt and Ni, with Pt being as expensive as Au and Ni being less reflective. Other highly reflective metals, like Al, Ag and Cu are not well suitable due to their high low work function of 4.2, 4.5 and 4.7, respectively. Copper has the further disadvantage of high diffusivity, which leads to shunted devices. Aluminium oxidises very quickly, leading to a highly resistive contact. Leaving silver as the best option. Devices fabricated with Ag back contacts were tested, but they suffered from a strong Schottky contact which suppressed any photovoltaic activity.

Hole transport layers, like PEDOT:PSS or MoO_{3-x}, typically used in organic solar cells were also tested and surprisingly, MoO_{3-x} in combination with Au lead to the best devices. In organic solar cells MoO_{3-x} is a standard material for hole extraction [183]. It is highly resistive, but 5-10 nm layer thickness were shown to be sufficient to achieve ohmic contacts with ITO (WF 4.7 eV) [184] [183] and also Ag (WF 4.5 eV) [185]. The

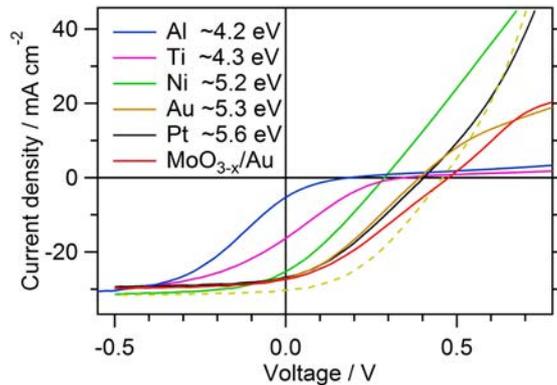


Figure 10.14: $J - V$ curves of ZnO/CIGSe stacks with different metals as the back contact, without sodium doping. The dashed line is for a ZnO/CIGSe/Au device doped with sodium.

calculated reflectivity for the MoO_{3-x}/Ag stack is also shown in Fig. 10.13a.

So far, only the MoO_{3-x}/ITO stack was tested for semi-transparent CIGSe devices [184]. But the MoO_{3-x} reacted with CIGSe to GaO_x during the deposition of CIGSe on top of it. The MoO_{3-x}/Ag stack has not yet been used for CIGSe solar cells. Here it is tested for application as a highly reflective back contact in CIGSe superstrate devices. The MoO_{3-x} was thermally evaporated from a MoO₃ powder source onto two CIGSe coated ZnO substrates at room temperature. One CIGSe layer was NaF post treated directly after the CIGSe deposition. Reference cells were fabricated with Au back contacts, directly after the CIGSe deposition, whereas, prior to the MoO_{3-x}/Ag deposition, both CIGSe layers were stored for 3 months in vacuum with several short vacuum breaks in between. No further treatments were performed to remove potential oxidation of the surface on the CIGSe layer.

The $J - V$ curves of devices with Au and MoO_{3-x}/Ag as the back contact are shown in Fig. 10.15a. The devices are slightly Cu-poor at the back contact interface, which leads to a high ohmic contact above 4 Ωcm² for the devices fabricated without sodium. The series resistance is slightly higher for the device with MoO_{3-x}/Ag, probably induced by the high resistive MoO_{3-x} layer [186]. To increase the back contact quality it was shown in Sec. 6.1, that it is necessary to dope the CIGSe surface with sodium. However, it was not possible to perform the NaF PDT after the MoO_{3-x} deposition, as it was done with the 10 nm Mo layer described in Sec. 5.2.4, since the sodium did not diffuse through the MoO_{3-x} layer, even at 300°C. Fig. 10.15b shows the $J - V$ curve of the sample with the NaF PDT performed prior to the MoO_{3-x} deposition. Again, the MoO_{3-x} layer increases the series resistance by 0.5 Ωcm² compared to the Au reference device. The MoO_{3-x}/Ag contact does not reduce the shunt resistance or the short circuit current. The variations in the FF and the V_{OC} are relatively small and likely to originate from typical sample quality fluctuations and not from the MoO_{3-x}/Ag contact.

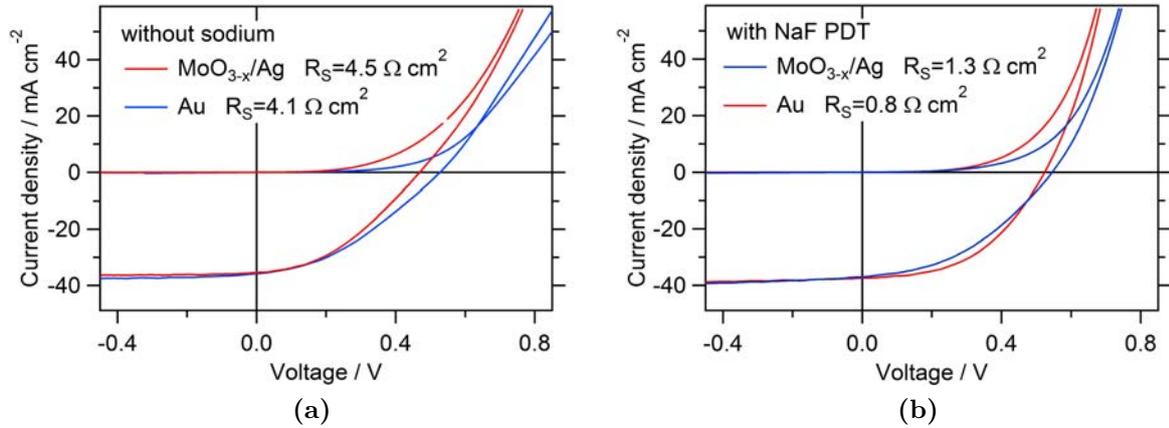


Figure 10.15: Experimental $J - V$ curves of superstrate CIGSe solar cells with Au and MoO_{3-x}/Ag as the back contact, **a)** without any sodium present **b)** with NaF PDT at 300°C for both samples.

10.3.3 Ultra thin absorbers

Fig. 10.16a displays the simulation results of the PCE for different values of the absorber thickness. The device simulation was set-up with a Ga gradient towards the back contact, the gradient increases over 100 nm CIGSe the conduction band minimum by 250 meV. Further, no conduction band spike or cliff at the hetero-junction is set and the bulk electron diffusion length is set to 2.3 μm . The charge carrier density is $1\text{e}+16 \text{ cm}^{-3}$. The Schottky barrier at the back contact was set to 200 meV with a high recombination velocity of $1\text{e}+7 \text{ cm/s}$ for electrons and holes. The back contact reflectivity was set to 95 %. The corresponding energy band diagram is shown in Fig. 10.16b. The absorption coefficient for the different band gaps were taken from [187]. For 2.8 μm thick CIGSe layers this setup results into a PCE of 18.6 %, limited by bulk and interface recombination. The CIGSe thickness given in Fig. 10.16a refers to the CIGSe layer with no conduction band gradient. The 100 nm thick graded layer, has to be added to the total thickness. It is not varied during the thickness variation, since a too sharp increase of the Ga content could lead to an increased defect density [188]. The diffusion length was set to 500 nm in this layer, to account for the defects created by the Ga gradient. The contribution to the absorption of this layer is low due to the increased band gap compared to the bulk.

The simulation results for the above described setup, show, that the PCE decreases with decreasing CIGSe thickness. For thickness values between 500 nm and 2 μm this is due to the increasing recombination losses at the back contact, despite the 250 meV electron barrier at the back contact induced by the Ga Gradient. For thickness values below 500 nm the PCE decreases sharply due to the poor light absorption yield. If the back contact is perfectly passivated, which can be partially achieved with AlO_x as reported in [189], the recombination velocity for electrons is zero. This enhances the PCE considerably for all thickness values below 3 μm .

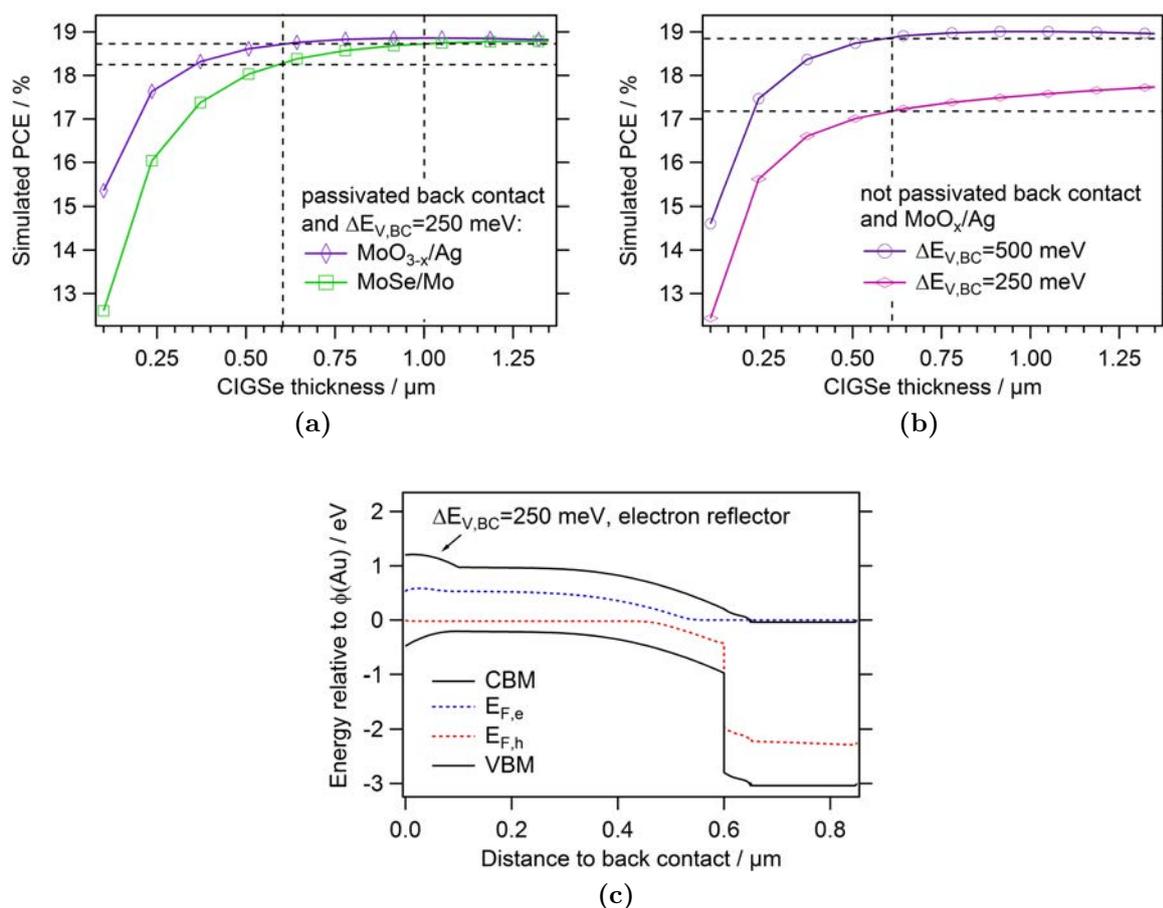


Figure 10.16: **a)** Dependence of the power conversion efficiency on the CIGSe layer thickness. The recombination at the back contact is set to zero. Incomplete absorption and back contact recombination leads to a reduced PCE for thin layers. **b)** Thickness dependence of the efficiency for devices with a $\text{MoO}_{3-x}/\text{Ag}$ back contact and differently strong Ga gradients at the back surface. **c)** Energy band diagram, which shows the Ga gradient at the back contact, which reduces the back contact recombination and increases the electron collection.

The maximum efficiency of 18.9% for the $\text{MoO}_{3-x}/\text{Ag}$ device, in the absence of back contact recombination, is reached for the total CIGSe thickness of 1 μm . For thinner layers, the light absorption is incomplete and for thicker layers the bulk recombination is increased due to the small SCR at a charge carrier density of $1\text{e}+16\text{ cm}^{-3}$. For the MoSe_x/Mo stack in substrate devices the maximum PCE is lowered to 18.8% and shifted to 1.4 μm due to the reduced back contact reflectivity. At a total CIGSe thickness of 600 nm the PCE is reduced to only 18.6% for the superstrate device and 18.0% for the substrate device. For layers thinner than 500 nm, the PCE drops sharply. To reach an efficiency of 18.6%, the thickness of the CIGSe layer has to be increases to 1.0 μm .

It is questionable whether the back contact can be fully passivated in a real device. But the back contact recombination can be also reduced by increasing the conduction band gradient $\Delta E_{V,BC}$ at the back contact from 250 meV to 500 meV. It even increases the PCE further due to the improved electron collection from the back. Such a steep Ga gradient is difficult to realize in substrate devices due to the inter-diffusion of In and Ga during the deposition. In superstrate devices though it was shown in Sec. 2.1 that it can be realized. This increases the maximum PCE to 19.0% for a total thickness of 1 μm and for 600 nm to 18.75%.

The PCE could be increased even further due to the removal of the implemented Schottky contact (not shown here), which improves the V_{OC} value.

Experimentally, superstrate devices with thin and thick absorbers are difficult to compare due to the different interface formation. The chemical composition at the interface during the growth differs as well as the duration of the growth process. This leads to different charge carrier collection efficiencies and different V_{OC} values. Fig. 10.17a shows the $J-V$ curve of a standard device with a 2.8 μm thick CIGSe layer and the same device with a 0.75 μm thick CIGSe layer. The photo current at negative voltages drops by 1.5 mA/cm^2 in the thinner device, which is exactly the expected value from the simulation. The V_{OC} and the FF are difficult to compare though, since the interface properties are not directly comparable. The FF of the thin device is slightly better, which compensates the loss in V_{OC} . Still, the PCE for both devices are the same, as expected from the simulation.

Light scattering

Another option, to reduce the CIGSe thickness, is to increase the light pathway within the absorber by light scattering. This can happen at the front or at the back contact. The back contact has a given roughness due to the CIGSe surface roughness. This is typically around 60 nm (RMS) for the co-evaporated layers prepared during this work. The amount of diffuse scattering at the back contact can be calculated with the help of the simple scalar scattering theory [190] [191] as follows:

$$R_{diffuse} = R_{tot} \cdot \exp\left(-\left[\frac{2\pi\sigma_{rms}2n_{CIGSe}(\lambda)\cos(\theta)}{\lambda}\right]^2\right), \quad (10.1)$$

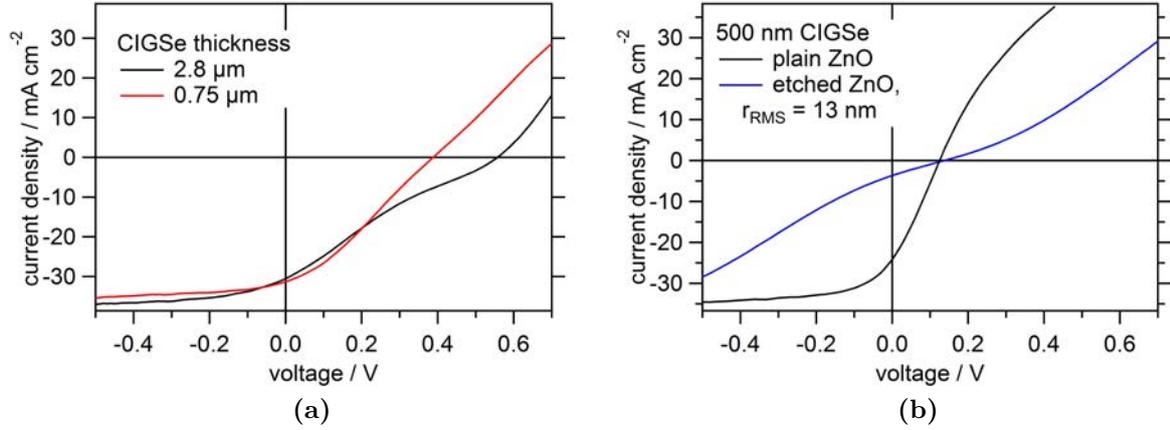


Figure 10.17: $J - V$ curve of superstrate devices with CIGSe layers fabricated at 520 °C and with a) different thickness b) plain and untreated ZnO as well as HCl etched ZnO.

with σ_{rms} describing the RMS surface roughness, $n_{CIGSe}(\lambda)$ the wavelength dependent refractive index of CIGSe, θ the incoming angle to the surface normal. Equation 10.1 is only valid if diffraction effects dominate the light reflection, which is the case for surfaces whose facets are smaller or comparable to the wavelengths of the reflected light. For typical CIGSe layers this is given for light in the visible and infrared region. The percentage of diffuse reflected light at the back contact is given in Fig. 10.19a. For the typical roughness of 60 nm the diffuse reflected light is 90 % in the infrared region. Assuming a \cos^2 angle distribution of the reflected light, the average optical path of photons with $\lambda = 1200$ nm would increase by 30 % for one way through the absorber. The minimum thickness of 500 nm could be further reduced to 440 nm in order to achieve 19.1 % with the in the previous section described model. The MoSe_x/Mo reference would lead to a PCE of 18.3 %. To reach 19.1 % a thickness of 710 nm would be required.

In substrate devices the CIGSe surface roughness leads to light scattering at the front contact. The equation to describe the diffuse transmission is similar to Eq. 10.1, but the refractive index in the numerator of the exponential is exchanged by half of the difference of the refractive index of ZnO and CIGSe:

$$T_{diffuse} = T_{tot} \cdot \exp\left(-\left[\frac{2\pi\sigma_{rms}(n_{CIGSe}(\lambda) - n_{ZnO}(\lambda))\cos(\theta)}{\lambda}\right]^2\right) \quad (10.2)$$

Fig. 10.19b shows the percentage of diffuse transmittance of the total transmittance for different values of the surface roughness. For the typical CIGSe roughness of 60 nm the diffuse transmittance is 6 % and 94 % of the infrared light is transmitted specular. Thus, the average optical pathway increases only 2 % for one way through the absorber, which does not reduce the minimum absorber thickness noticeably.

The fraction of diffuse transmittance through the ZnO can be controlled in superstrate devices by controlling the ZnO roughness prior to the CIGSe deposition. This is a standard

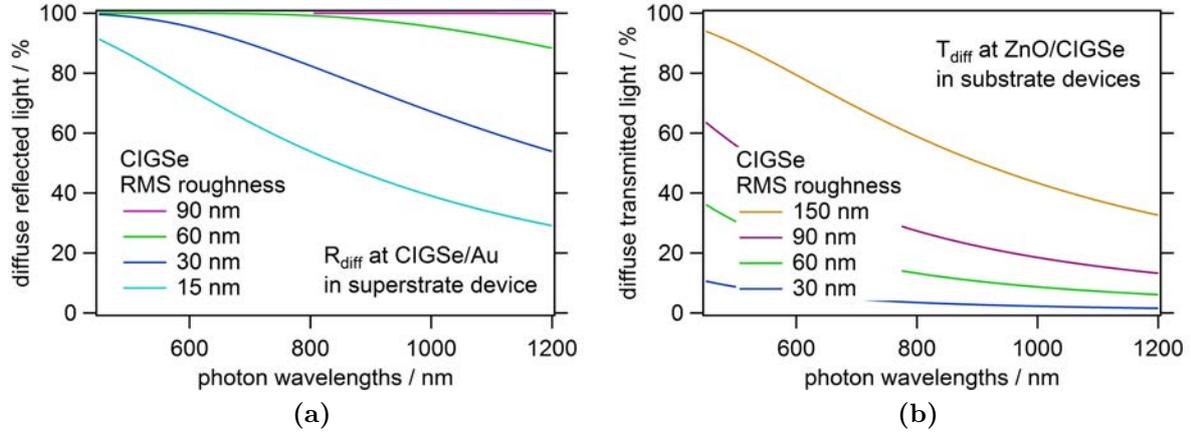


Figure 10.18: **a)** Percentage of diffuse reflected light from the total reflected light at the CIGSe/Au interface in superstrate devices. **b)** Percentage of diffuse transmitted light from the total transmitted light at the ZnO/CIGSe interface in substrate devices.

procedure in amorphous silicon solar cells and usually achieved by HCl etching [192]. Achieving strong scattering for long wavelength photons with energies close to the band gap of CIGSe devices is more difficult, due to the lower band gap and the lower refractive index. To describe the scattering from a HCL etched ZnO it was found in [193] that the exponent within the exponential function of Eq. 10.2 has to be changed from 2 to 3, to account for the different roughness profile of the etched ZnO compared to the natural CIGSe surface profile. This leads to the following formula:

$$T_{diffuse} = T_{tot} \cdot \exp\left(-\left[\frac{4\pi\sigma_{rms}(n_{CIGSe}(\lambda) - n_{ZnO}(\lambda))\cos(\theta)}{\lambda}\right]^3\right) \quad (10.3)$$

With this equation the measured diffuse transmittance of a HCL etched ZnO substrate can be fitted to obtain the RMS roughness. Fig. 10.18a shows the measured and the calculated diffuse transmission spectra, which are in very good agreement. The HCl etching was performed for 60s in a 1 wt.% HCl solution, as done in [194]. A RMS roughness of 46 nm is obtained from the fit. The calculated diffuse transmittance at the ZnO/CIGSe interface in the infrared only increases by 0.2%. Fig. 10.18b shows the dependence of the diffuse transmittance at the CIGSe/ZnO interface. In order to get sufficient scattering to reduce the layer thickness, the ZnO RMS roughness has to be above 100 nm for CIGSe superstrate devices. This high roughness is likely to lead to shunting of the only 450 nm thick CIGSe layer. Further it will increase the series resistance. The sheet resistance of the 1 μm thick test sample had a roughness of 46 nm and the sheet resistance increased from 6 Ω/\square to 13 Ω/\square due to the etching. This requires thicker ZnO layers, which in turn increase the absorption losses within the ZnO and with it the PCE of the device independent of the CIGSe thickness. The positive effect of the increased light scattering is therefore exceeded by the negative effects from the increased series resistance or light

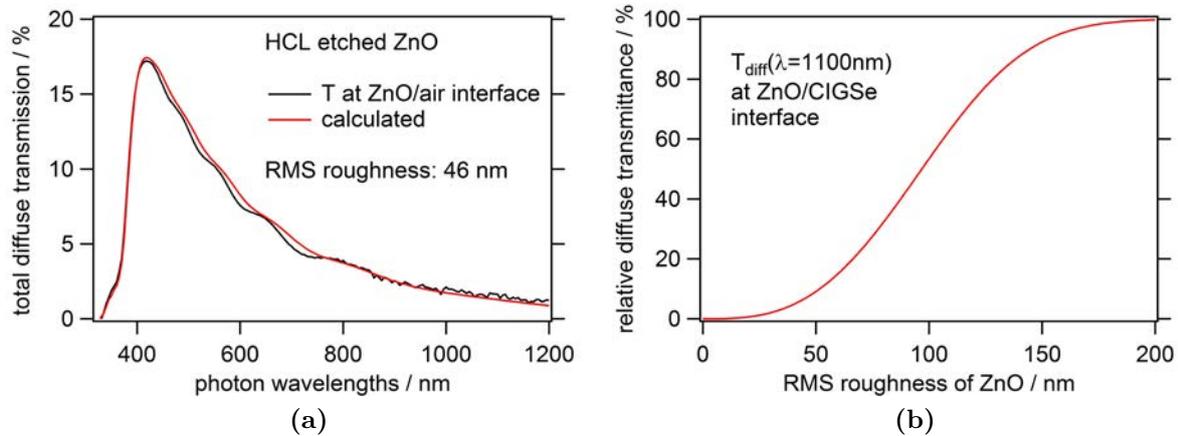


Figure 10.19: a) The total diffuse transmitted light at the HCl etched ZnO interface with air, fitted the function defined in Eq. 10.3. b) Percentage of the light which is diffuse transmitted at the HCl etched ZnO interface with CIGSe.

absorption.

Experimentally, the $J - V$ curves of superstrate devices with etched ZnO layers, show very low fill factors and PCEs. Fig. 10.17b shows one example. Most likely this is caused by a combination of increased series resistance and increased interface recombination, due to the increased surface area. The parallel resistance, obtained from the dark $J - V$ curve, is however not reduced due to the 46 nm RMS roughness of the ZnO layer.

10.3.4 Summary

ZnO annealing was shown to enable a photo-current increase of up to 3 mA/cm^2 for cap annealed ZnO and 1.5 mA/cm^2 for ZnO annealed during the CIGSe deposition, compared to a as-deposited ZnO layer. At the same time it reduces the sheet resistance by 30%. Both effects were linked to the reduced structural disorder in the annealed films.

It was shown that $\text{MoO}_{3-x}/\text{Ag}$ back contacts can replace the Au contact in CIGSe superstrate solar cells. Due to the high reflectivity of this contact it is possible to reduce the total CIGSe thickness to $1 \mu\text{m}$ while even increasing the efficiency compared to thicker devices. The increased efficiency is due to better charge carrier collection. Substrate devices were shown to experience lower efficiencies already below $1.4 \mu\text{m}$ due to the poor back contact reflection.

It was estimated that the total thickness of superstrate devices can be reduced to 540 nm in superstrate configuration while remaining the efficiency at 18.75% compared to 17.8% in the substrate configuration. This is not only due to the improved light reflection at the back contact, but also due to the enhanced light scattering naturally occurring in superstrate devices. Increasing the light scattering further due to etching the ZnO prior to the CIGSe deposition was not successful, due to increased interface recombination losses. It is questionable whether TCO roughening is principally beneficial in CIGSe solar cells,

since efficient scattering requires a TCO RMS roughness around 100 nm due the low band gap and refractive index of CIGSe.

10.4 CIGSe growth

To study the effect of an amorphous substrate on the CIGSe growth, this section will compare a CIGSe layer grown on a crystalline ZnO layer and on an amorphous Ga₂O₃ layer. The difference of the ZnO and the CIGSe crystal structure and their lattice constants is supposed to introduce crystallographic defects at the interface, as dangling bonds for example, but may also induce increased stress within the CIGSe film or influence the texture and the micro-structure. The ZnO surface is dominated by the (002) plane, whose inter-atomic distance is 3.24 Å. The inter-atomic distance in the dominant (112) plane in CIGSe is between 2.4 and 2.6 Å. Thus, no epitaxial growth of CIGSe onto such textured ZnO is expected. As shown in the previous sections, no transfer of texture and micro-structure of the ZnO to the CIGSe layer was observed for the deposition temperature of 520°C. However, at this temperature the formation of an amorphous interfacial layer was observed. The amorphous layer forms during the high-temperature deposition stage. Here, the CIGSe was deposited at a lower temperature, to reduce the formation of this amorphous interfacial layer.

Experimental: The CIGSe was deposited by the modified 3-stage process at a temperature of 470°C. The buffer layer was chosen to be a crystalline i-ZnO layer and a 20 nm thick amorphous Ga₂O₃ layer. The i-ZnO/ZnO:Al stack was deposited on soda lime glass with a SiO_x alkali barrier, the Ga₂O₃/ZnO:Ga stack was deposited on alkali free glass. SEM images were taken and XRD patterns (in Bragg-Brentano geometry) recorded

Results: The SEM images of the resulting CIGSe layers are shown in Fig. 10.20a and b. The obvious difference is that the CIGSe layer grown on the i-ZnO exhibits smaller grains compared to the CIGSe layer grown on the amorphous Ga₂O₃ layer. Further, it appears that the structure of the ZnO grain boundaries are transferred to the grain boundary structure of the first 100 nm CIGSe layer. This cannot be observed for the layer grown on the Ga₂O₃, which exhibits larger grains, with the same size close to the substrate as in the bulk. The XRD pattern of both samples are shown in Fig. 10.20c, which shows a different texture for both samples. The CIGSe deposited on i-ZnO has a stronger (112) orientation compared to the CIGSe deposited on the amorphous layer. The same was observed for CIGSe layers deposited at 450°C.

Discussion: The CIGSe layers compared in this study show a different average grain size and a different texture even though they were deposited in the same deposition run. One reason could be the different glass and ZnO used as the substrate, which can lead to different stress within the CIGSe film. One way to reduce the stress would be to increase the grain growth [195], which could explain the different average grain sizes. But this cannot explain the correlation of the micro-structure between the CIGSe layer, close to the ZnO interface, and the ZnO layer. This indicates a structural correlation between the ZnO and the CIGSe, which is lost once an amorphous interfacial layer develops. CIGSe layers deposited at higher temperatures exhibit a more pronounced amorphous interfacial

layer and do not show such a correlation of the micro-structure.

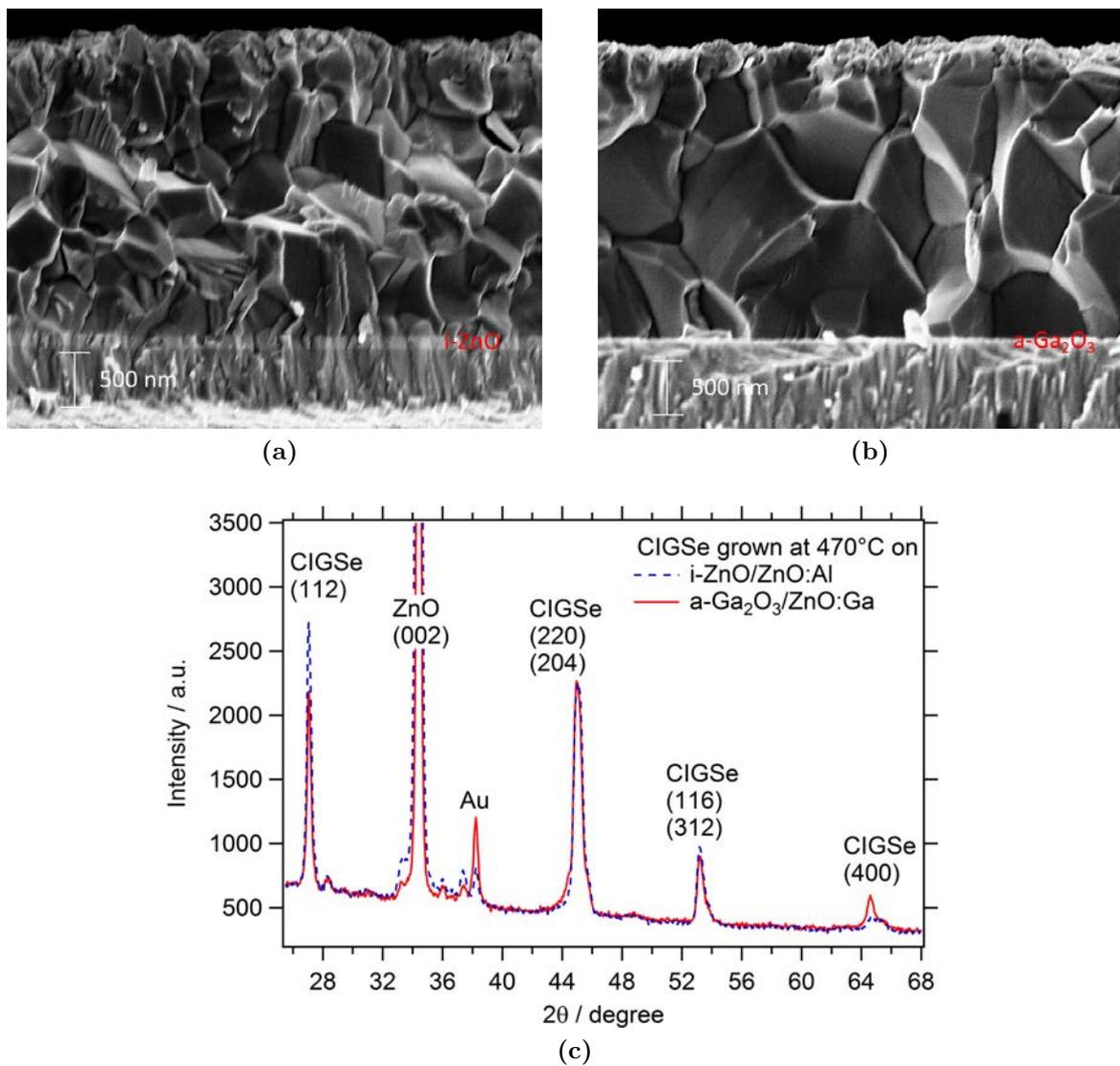


Figure 10.20: SEM image of a $\text{Cu}(\text{In}_{0.7}\text{Ga}_{0.3})\text{Se}_2$ layer grown at 470°C on top of a a) $\text{i-ZnO}/\text{AZO}$ and b) $\text{a-Ga}_2\text{O}_3/\text{GZO}$ substrate. c) XRD pattern of both samples.

10.5 Tandem configuration

To achieve all chalcopyrite 4-terminal tandem devices, it is necessary to prepare the wide-gap chalcopyrite in superstrate configuration. Therefore, this section gives a short overview on the different tandem configuration and their material requirements.

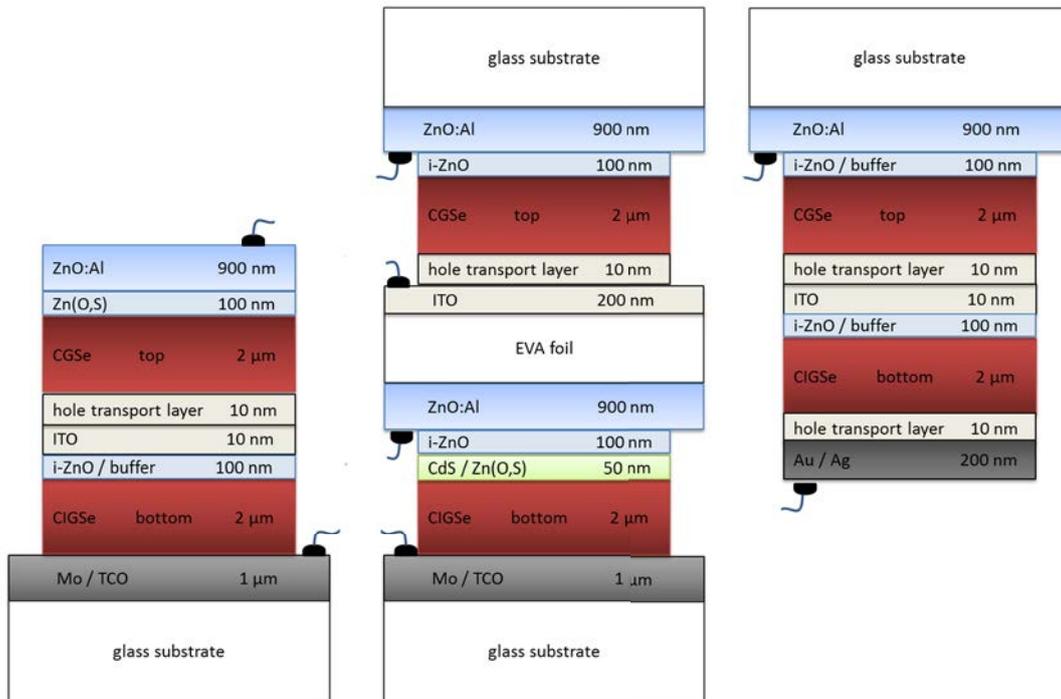


Figure 10.21: Monolithic (two-terminal) tandem device in substrate configuration (left) and in superstrate configuration (right), both electrically connected by a tunnel-junction (hole transport layer with ITO). Mechanically stacked (four-terminal) tandem device (center) mechanically connected with EVA foil (not to scale).

A mechanically stacked tandem device, as shown in the center image of Fig. 10.21, requires a wide band gap semi-transparent superstrate device together with a narrow band gap substrate device. The semi-transparent back contacts can be realized by using ITO as the back contact [36]. These two devices are laminated together and contacted separately, therefore they are also called 4-terminal device. For a narrow band gap of 1.16 eV for CIGSe, the wide gap material for the superstrate device should be between 1.7 eV and 2.0 eV to reach maximum theoretical efficiencies above 38% [196]. Thus, a combination of CIGSe and CGSe ($E_g = 1.70$ eV) would be suitable.

An alternative tandem design is the monolithic, or 2-terminal, connection of the narrow and wide band gap device. The distribution of optimum band gaps are narrower in this case, due to the requirement of current matching in monolithic tandem devices. The optimum combination would be 1.10 eV for the CIGSe bottom cell in combination with a 1.70 eV for the CGSe top cell. When choosing the substrate configuration, as shown

in the left image of Fig. 10.21, a wide gap CGSe solar cell has to be grown on top of a narrow gap CIGSe bottom solar cell. This does not require the use of a superstrate device, but the CIGSe bottom solar cell has to withstand a high temperature step during the deposition of the top cell. The CdS/CIGSe interface was shown to be stable only until 300 °C [197], thus the CdS has to be exchanged with a thermally stable buffer layer just as in superstrate devices. The monolithic tandem in superstrate configuration is shown in the right image of Fig. 10.21. In this case the narrow gap bottom cell has to be grown on top of the wide gap top cell.

In summary, independent of the choice for the tandem design, whether monolithic or mechanically stacked, a thermally stable buffer layer has to be found in order to realize an all chalcopyrite tandem solar cell with CGSe as the wide gap material. However, the maximum efficiency for CGSe is so far limited to 11.2% [198] and the highest wide gap chalcopyrite superstrate device is reported to be only 3.8% [28]. Further, parasitic light absorption in CGSe devices were shown to be high [199]. This makes an all chalcopyrite tandem unlikely at the moment and other wide gap materials like perovskites are more favourable. Common PbI₂ based perovskite solar cells were shown to be stable until 140 °C [200].

List of Publications

First-authorship

- M. D. Heinemann, V. Efimova, R. Klenk, B. Hoepfner, M. Wollgarten, T. Unold, H.-W. Schock and C. A. Kaufmann, "Cu(In,Ga)Se₂ Superstrate Solar Cells: Prospects and Limitations", *Progress in Photovoltaics: Research and Applications* (2014), published online.
- M. D. Heinemann, D. Greiner, T. Unold, R. Klenk, H. Schock, R. Schlatmann and C.A. Kaufmann, "The Importance of Sodium Control in CIGSe Superstrate Solar Cells", *IEEE Journal of Photovoltaics* 5, 2015, Issue 1, 378-381
- M.D. Heinemann, F. Ruske, D. Greiner, AR Jeong, M. Rusu, B. Rech, R. Schlatmann and C.A. Kaufmann, "Light management in Cu(In,Ga)Se₂ superstrate solar cells", *Solar Energy Materials and Solar Cells* (submitted).
- M.D. Heinemann, J. Berry, G. Teeter, T. Unold and D. Ginley, "Oxygen deficiency and Sn doping of amorphous Ga₂O₃", *Applied Physics Letters* (accepted).
- M. D. Heinemann, R. Mainz, H. Rodriguez-Alvarez, D. Greiner, C.A. Kaufmann and T. Unold, "In-situ Analysis of Cu(In,Ga)Se₂ Absorber Growth: Band Gap Energy, Defect Absorption, Growth Rate and Roughness", *Advanced Energy Materials* (submission in progress).

Co-authorship:

- C. Kaufmann, D. Greiner, H. Rodriguez-Alvarez, A. Weber, M.D.Heinemann, J. Lauche, M. Klaus, C. Genzel, H. W. Schock and R. Mainz, "Co-evaporation of Cu(In, Ga)Se₂ at low temperatures: An In-Situ x-ray growth analysis" *IEEE 39th PVSC proceedings*, 2013, 3058 - 3061
- W. Ohm, W. Riedel, Ü. Askünger, M. D. Heinemann, C. A. Kaufmann, J. L. Garcia, V. Izquierdo, X. Fontane, T. Goislard, M. C. Lux-Steiner, "An Overview of Technological Aspects of Cu(In,Ga)Se₂ Solar Cell Architectures Incorporating ZnO Nanorod Arrays" *physica status solidi (a)* 212 (2015), Nr. 1, 76-87.
- J. K. Larsen, S.-Y. Li, J. J. Scragg, Y. Ren, C. Högglund, M.D. Heinemann, S. Kretzschmar, T. Unold, C. Platzer-Björkman, "Interference effects in photoluminescence spectra of CZTS and CIGS thin films", *Journal of Applied Physics*, 118, 2015.

- S. C. Siah, R. E. Brandt, L. T. Schelhas, K. Lim, J. D. Perkins, R. Jaramillo, M. D. Heinemann, D. Chua, J. Wright, C. U. Segre, R. G. Gordon, M. F. Toney, T. Buonassisi, "Dopant activation in Sn-doped Ga₂O₃ investigated by synchrotron-based X-ray absorption spectroscopy" *Applied Physics Letters*, not yet published.
- R. Mainz, H. Rodriguez-Alvarez, M. Klaus, D. Thomas, J. Lauche, A. Weber, M. D. Heinemann, S. Brunken, D. Greiner, C. A. Kaufmann, T. Unold, H.-W. Schock, and C. Genzel, "Sudden Stress Relaxation in CuInSe₂ Films during Cu-Se Deposition Revealed by Real-time X-ray Analysis" *Physical Review B* 92, 2015, 155310 1-8.
- R. Mainz, H. Rodriguez-Alvarez, D. Greiner, M. D. Heinemann, H. Stange, M. Klaus, C. Genzel, H.-W. Schock, C. A. Kaufmann, "Formation of Cu(In,Ga)Se₂ thin-film solar cell absorbers by multi-stage co-evaporation studied by real-time X-ray analysis" *manuscript in process*

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Acknowledgement

First of all I would like to thank my wife Anna, who supported me throughout the course of this PhD with her cheerfulness :)

I want to thank Christian Kaufmann, Thomas Unold and Hans-Werner Schock, who made it possible for me to work in their groups and learn from their experience and knowledge. Especially I would like to thank Christian, who was a great supervisor throughout the three years. Special thanks also to Bernd Rech and Thomas Unold for making it possible for me to join NREL for six months. At NREL I would like to thank David Ginley, Joe Berry and Miguel Contreas for the support during this time. In addition I want to thank Susan Schorr, Michael Powalla and Bernd Rech for reviewing this thesis.

At HZB I want to thank:

- Jakob Lauche and Dieter Greiner for keeping the PVD up and running,
- Britta Höpfner and Jan Alsmeier for the great help with the XPS measurements,
- Daniel Abou-Ras and Norbert Schäfer for facilitating the SEM,
- Lars Steinkopf, Jo Klaer, Jan Schniebs and Karsten Prietzel for all the help inside the lab,
- Roland Mainz for facilitating the in-situ EDXRD measurements,
- Anja Scheu and Dieter Greiner for optimizing and running the GDOES measurements,
- Markus Wollgarten for doing the TEM images,
- Reiner Klenk and Susanna Harndt for the discussions and providing the In_2S_3 evaporator,
- Carola Kirch and Michael Kirsch for the ZnO depositions,
- Justus Just for providing the EBIC fitting software,
- Alexander Redinger for preparing ZnS and ZnSe layers,
- Rutger Schlatmann, Sebastian Schmidt, Stephan Brunken and Dieter Greiner for proof reading,
- Sergej Levenco for all the entertaining discussions on optics and capacitances,
- Joachim Liebich for the LabView support,
- Dieter Greiner for performing the Drude model fits to the optical data,
- Sebastian Fichter for introducing me to the program ChemSage,
- Steffen Kretzschmar for the support in the optical lab.

Also I want to thank the whole former team of the E-IT institute for the very pleasant three years inside and outside the HZB.

Last but not least special thanks to my friends, especially Jan, Tobi and Thorsten, as well as my family, especially my parents, my sister and my grandparents, to remind me of the life outside of the PhD while keeping me motivated at the same time.