V-Band Low Noise Amplifier and Mixer Design using 90 nm CMOS Technology

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No, non ti ho dimenticato. Grazie...

Abstract

This thesis is the result of more than three years research work at TU-Berlin. Several radio frequency integrated circuits have been designed in a commercial CMOS technology, the TSMC 90 nm, and measured on-wafer within the project WiONet. The author of this work has been focused on the design of the receiver part of a V-band high data-rate millimetre-wave transceiver and particularly on two important building blocks such as low-noise amplifier and down-conversion mixer.

At first, the specifications of the receiver and its sub-blocks have been extracted applying to the planned transceiver system the requirements obtained by the IEEE 802.15.3c standard. Afterwards, a deep study of the passive and active components provided by the technology and a careful characterization of the structures to be used have been carried out in order to get familiar with the technology and optimize its use. The noise behaviour of several amplifier and mixer topologies has been deeply studied, leading to the design and the characterization of several CMOS circuits. Finally, a four stage fully differential common source low noise amplifier and a fully differential Gilbert cell with resonating current bleeding network have been chosen for being part of the WiONet system. Both circuits showed state of the art performance in terms of gain, linearity, noise and power consumption. Furthermore, they fulfil the system requirements within the whole V-band.

Zusammenfassung

Diese Dissertation ist das Ergebnis von mehr als drei Jahren Forschung an der TU Berlin. Mehrere integrierte Hochfrequenz-Schaltungen wurden innerhalb des Projekts WiONet in einer kommerziellen CMOS Technologie, TSMC 90 nm, entwickelt und gemessen. Ziel des Projektes war die Entwicklung eines V-Band Transceivers im Millimiterwellenbereich für künftige Anwendungen mit sehr hohen Datenübertratungsraten. Der Autor dieser Arbeit hat sich auf den Entwurf des Receivers, insbesondere auf die zwei wichtigen Elemente, rauscharmer Verstärker und Abwärtsmischer, konzentriert.

Die Spezifikationen des Receivers und dessen Untereinheiten wurden aus den geplanten Transceiver-Anforderungen entnommen, basierend auf dem IEEE 802.153c Standard. Anschließend wurden die von der Technologie bereitgestellten passiven und aktiven Komponenten gründlich untersucht und eine gewissenhafte Charakterisierung der genutzten Strukturen durchgeführt, um mit der Technologie vertraut zu werden und ihren Nutzen zu optimieren. Das Rauschverhalten mehrerer Verstärker- und Mischer-Architekturen, welche zu dem Design und der Charakterisierung verschiedener CMOS-Schaltungen führte, wurde analysiert. Schlussendlich wurde ein vier-stufiger volldifferenzieller, rauscharmer Verstärker in Source-Schaltung, sowie eine volldifferenzielle Gilbert Zelle mit resonantem current bleeding Netzwerk als Teil des WiONet Systems gewählt. Beide Schaltkreise entsprechen bezüglich Verstärkung, Linearität, Rauschen und Leistungsaufnahme dem Stand der Technik. Außerdem genügen sie den Systemanforderungen im kompletten V-Band.

Abbreviations

TRx	Transceiver
IQ	In-phase and quadrature
LNA	Low noise amplifier
CMOS	Complementary metal-oxide-semiconductor
OOK	On-off keying
IF	Intermediate frequency
DC	Direct current
PLL	Phased locked loop
LO	Local oscillator
FTTH	Fast fibre to the home
FITH	Fast fibre in the home
RF	Radio frequency
IEEE	Institute of Electrical and Electronics Engineers
FSPL	Free space loss
PHY	Physical layer
MAC	Media access control
UM	Usage model
SC	Single carrier
HSI	High speed interface
AV	Audio visual
OFDM	Orthogonal frequency division multiplexing
CMS	Common mode signalling
BPSK	Binary phase shift keying
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
DAMI	dual alternate mark inversion
Tx	Transmitter
Rx	Receiver
BER	Bit error rate
PAPR	Peak to average power ratio
F	Noise factor

ABBREVIATIONS

NF	Noise figure
SNR	Signal to noise ratio
IC	Integrated circuit
BB	Baseband
DCM	Down conversion mixer
DEM	Demodulator
MOD	Modulator
UCM	Up conversion mixer
PA	Power amplifier
SFD	Static frequency divider
TSMC	Taiwan Semiconductor Manufacturing Company
f_t	Transition frequency
f_{max}	Maximum oscillation frequency
UTM	Ultra thick metal
GCTL	Grounded coplanar transmission line
DUT	Device under test
GSG	Ground-signal-ground
MOS	Metal-oxide-semiconductor
BSIM	Berkeley Short-channel IGFET Model
MSG	Maximum stable gain
EM	Electro-magnetic
SCTL	Shielded coplanar transmission line
MIM	Metal-insulator-metal
CBM	Capacitor bottom metal
CTM	Capacitor top metal
VCO	Voltage controlled oscillator
MAG	Maximum available gain
IP1dB	Input power at the 1 dB compression point
MOSFET	Metal-oxide-semiconductor field-effect transistor
P1dB	1 dB compression point
CMRR	Common mode rejection ratio
P_{DC}	Direct power
BW	Bandwidth
FOM	Figure of merit
SSB	Single side band
DSB	Double side band

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Introduction

Wireless communications are changing the world. Nowadays, an always growing amount of data is being exchanged without physical connections. The overcrowding of the ether, especially at low frequency bands, and the need of gigabit per second (Gbit/s) data exchange, requested by the wireless internet advent, justify the great effort produced by researchers in the field of high frequency wireless systems. This should all be supported by reliable and mass production-competitive technologies. Within this context finds place the WiONet project, where a broadband internet signal carried outdoor through optic fibres has to be broadcast indoor in a wireless fashion.

The task of the Berlin University of Technology team is the development of a wireless transceiver (TRx) to be used for in-room communication and able to process broadband signals. The requested functionalities can be achieved exploiting the portion of the V-band at around 60 GHz, particularly appropriate for short-range high-data-rate communication, and using a 90 nm complementary metal oxide semiconductor (CMOS) technology, a widely used and market-competitive silicon technology.

As it will be shown, a super-heterodyne architecture with in-phase and quadrature-of-phase (IQ) outputs has been chosen. This thesis is focused on the development of the 60 GHz receiver, consisting of a low noise amplifier (LNA) and a 60 GHz to 20 GHz down-conversion mixer. All the design steps, from the design and the characterization of active devices and passive structures until the development and the optimization of the two requested circuits, will be presented and in details discussed. Simulations and measurements results will be reported and compared, and any open issues will be mentioned and left for future works.

Many scientific publications can be found in this field. A great variety of technical papers present very impressive results concerning the design of 90 nm CMOS 60 GHz transceivers as well as stand-alone circuits. A deep literature study is always a good

starting point, fundamental to understand what are the most used (which means, in many cases, most suitable) solutions and the state-of-the-art performance one has to refer to. In [1] and [2] simple on-off keying (OOK) receivers are presented, which are not able to handle more complex and bandwidth efficient modulation schemes. Some more interesting results are presented in [3], where within only 0.29 mm^2 an LNA, a mixer and an intermediate frequency (IF) buffer are integrated, giving 16 dB gain and 7 dB noise figure for a DC power consumption of 60 mW. A receiver chip including the frequency synthesizer is presented in [4], achieving a conversion gain of 22 dB and a noise figure of 8.4 dB along with 144 mW power consumption, all in a chip of about 3 mm^2. A similar work, but smaller and less power-hungry, is presented in [5]. Here, an LNA, a phased-locked-loop (PLL) and two mixers for a double frequency conversion are integrated within only 1 mm^2, amplifying the input of 15 dB with 9 dB noise figure and consuming only 96 mW. The newest publication is a sub-harmonic receiver including an on-chip Yagi antenna [6]. In an overall area of 3 mm^2 the signal is received by the antenna and processed by the receiver. The whole receiving system, with an external local oscillator (LO) signal, shows a conversion gain of 16.2 dB and a noise figure of 13.5 dB, consuming 31 mW.

Keeping in mind the WiONet specifications and taking a cue from the existing literature, several solutions have been investigated, giving eventually birth to the circuits which will be presented in this thesis.

Chapter 1

Background: WiONet Project

WiONet, acronym standing for Wireless Optical Network, is a project founded by the German Ministry of Education and Research, Bundesministerium für Bildung und Forschung (BMBF). It aims the combination of optic and wireless data networks. In the last years, the bandwidth demand has tripled every year, pushed by new technologies as broadband internet or 3D television. The telecommunications operators answered to this need investing a lot on the optical transmission of digital signals via optic fibres, capable to reach very high data rates up to some Gbit per second. Another aspect of modern systems is the portability. Devices as mobile phones and laptops must have a wireless connection as fast as the optic one to avoid any slowdown of the data exchange. The WiONet project addresses both the mentioned aspects, the optic connection of the single house, so called Fast fibre To The Home (FTTH), and inside the house, known as Fast fibre In The Home (FITH), and the wireless connection inside the rooms. The idea behind the WiONet project is made clearer in Figure 1.1. The target speed is fixed at some Gbit per second for the optic wired network as well as for the wireless network.

The system is developed by a consortium of German private companies and universities, each of them taking care of one single area. The component which the Berlin University of Technology group is focused on is the one reported as RF switch in Figure 1.1, which is a fully integrated radio-frequency transceiver allowing all the wireless devices to be connected to the network. Since the market competitiveness of the system is one of the main tasks of the project, a very cheap CMOS technology has been chosen for the transceiver realization.

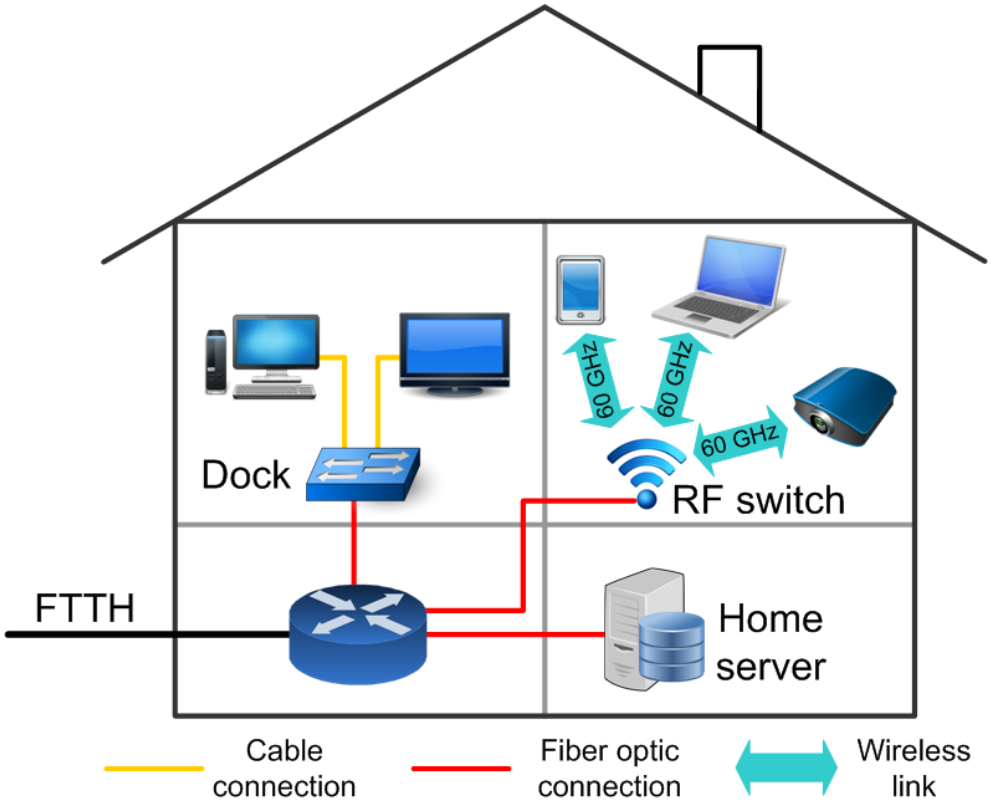


Figure 1.1: WiONet structure.

1.1 The 60 GHz band and the IEEE 802.15.3c standard

The speed of a wireless connection can be increased by using different methods. One of them is increasing the spectral efficiency. This can be achieved by high order modulation schemes [7], at the cost of additional transmit power, or using multiple antennas [8], paid with complexity and processing power. An easier and cheaper way is to increase the bandwidth. The existence of a very wide band at around 60 GHz, very suitable frequency band for high data-rate short-range communication [9], gives an unique opportunity in this regard since it is unlicensed in most of the countries, as visible in the diagram of Figure 1.2. Unfortunately, the free space loss at 60 GHz is much higher than in other wireless bandwidth like the ones at 2 GHz and 5 GHz, as states the Friis transmission equation [10]. In fact, the free space path loss (FSPL) increases quadratically with the frequency as shown in (1.1), where d is the distance between

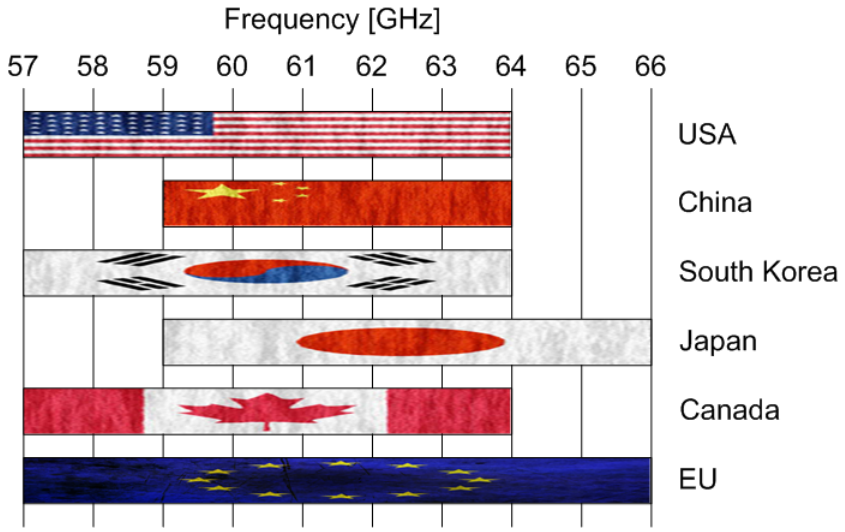


Figure 1.2: Allocated 60 GHz bandwidth in different countries.

transmitter and receiver, c the speed of light in vacuum and f the signal frequency.

$$FSPL = \left(\frac{4\pi df}{c}\right)^2 \tag{1.1}$$

On top of that, the specific attenuation characteristic of the 60 GHz band due to atmospheric oxygen of more than 10 dB/km worsens the situation. All this makes this band unusable for long range communications, restricting its usage to short distance applications.

Looking on the bright side, the huge attenuation isolates very well the communication from unwanted listeners. Considering an in-room communication, a common concrete wall would attenuate a 60 GHz signal of more than 30 dB, making the single room a well defined cell. Furthermore, to achieve acceptable transmit distance, 60 GHz antennas are designed usually with a very narrow associated beam [11], which improves the link interference immunity. This all makes such a communication highly secure. To intercept a 60 GHz transmission, it would be easier to dig into the wall and get the signal from the optic fibres than to find a way to install a wireless receiver without being detected.

The IEEE standard 802.15.3c defines the use of a physical layer (PHY) operating in the millimetre wave band along with the necessary media access control (MAC) layer

changes to support this PHY [12]. It includes five different usage models (UM) [13]:

- UM1: Uncompressed video streaming, high definition video signals.
- UM2: Uncompressed multi-video streaming, multiple video signals supplied by a single transmitter.
- UM3: Office desktop, communication between computer and peripherals.
- UM4: Conference ad hoc, many inter-communicating computers.
- UM5: Kiosk file downloading, an electronic kiosk enables upload and download by hand-held devices.

Due to the conflicting requirements of the different UMs, three new PHY modes have been developed:

- SC: Single carrier mode.
- HSI: High-speed interface mode.
- AV: Audio/visual mode.

The main difference between the PHY modes is the modulation technique, being single carrier for the SC mode and orthogonal frequency division multiplexing (OFDM) for HSI and AV modes. Other differences are the UMs within they are used and the required data rate, as summarized in Table 1.1. All the PHY modes use the same characteristic packet, consisting of a preamble, an header and a payload. An additional PHY mode designed to mitigate interference among other modes is the common mode signalling (CMS). It is used for low data rate transmission of command frames, using a single carrier $\pi/2$ binary phase shift keying (BPSK) modulation.

All the channels within the 60 GHz band must support the data rates required by the defined usage models. The IEEE 802.15.3c standard defines four different channels, each of them 2.16 GHz wide, divided in such a way that at least two of them are included into the allocated bandwidth all over the world. In order to minimize interference with other bands, a lower guard band 240 MHz wide and an upper guard band 120 MHz wide are also considered. The IEEE 802.15.3c channelization schema is reported in Figure 1.3. Defining the four channels this way, the second and the third

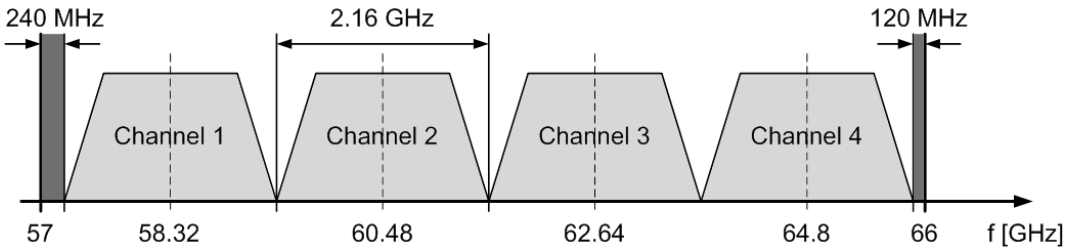


Figure 1.3: IEEE 802.15.3c Channelization.

channel are included in all the allocated bandwidth in the different countries, as it can be understood comparing Figure 1.2 and Figure 1.3.

1.2 System specifications

A system thought to work within a certain standard should be able to satisfy the specifications given by its most stringent scenario. The IEEE 802.15.3c standard includes multiple operating modes, as explained by Table 1.1. The highest data rate, more than 5 Gbit/s, is achieved using an OFDM 64 quadrature amplitude modulation (64-QAM) within the HSI PHY mode: this will be taken as target for the WiONet system, the starting point where the needed specifications can be extrapolated from. An high level view of the WiONet transceiver system is shown in Figure 1.4. For the calculations of the receiver specifications, some assumptions on the performance of transmitter, an-

Table 1.1: IEEE 802.15.3c PHY modes

	SC	**HSI**	**AV**
UMs	UM3, UM5	UM3, UM4	UM1, UM2
Modulations	OOK, $\pi/2$ BPSK, QPSK, $\pi/2$ 8-PSK, $\pi/2$ 16-QAM, DAMI	QPSK, 16-QAM, 64-QAM	QPSK, 16-QAM
Data rates	0.3 Mb/s–5.28 Gb/s	1.54 Gb/s–5.78 Gb/s	0.98 Gb/s–3.8 Gb/s

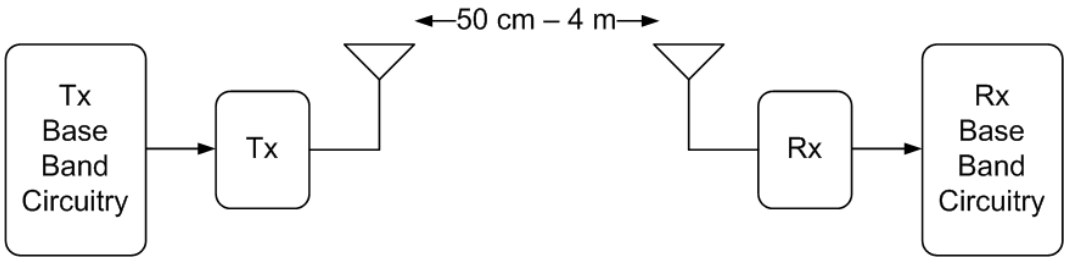


Figure 1.4: High level view of the WiONet transceiver

tenna and package have also to be done, as well as a communication distance range has to be defined. In Table 1.2 are reported system requirements, in terms of bit error rate (BER) and peak to average power ratio (PAPR), and assumed system performance, considering typical values for wire-bonding packaging technology and conventional Vivaldi antennas (or, instead, an array of 4 patch antennas). The listed information are enough to define the specifications of the receiver in terms of noise and maximum input power.

The noise factor (F), or equivalently its value in decibels, the noise figure (NF), determines the noise performance of a network. It measures how a signal, in particular its signal to noise ratio (SNR), is degraded by a circuit. Given a certain network, its

Table 1.2: HSI 64-QAM requirements and assumed system performance

System requirements	
PAPR	10 dB
BER	$< 10^{-7}$
Distance	50 cm–4 m
Assumed system performance	
Max. PA output power $P_{out,max}$	12 dBm
Tx/Rx Package losses	1.5 dB
Tx/Rx Antenna gain	14 dBi

noise figure is mathematically defined as the difference between input SNR and output SNR, both given in decibel, as reported in (1.2).

$$NF = SNR_{IN,dB} - SNR_{OUT,dB} \tag{1.2}$$

Knowing both $SNR_{OUT,dB}$ and $SNR_{IN,dB}$, the noise figure required by the target system can be calculated.

The $SNR_{OUT,dB}$ can be easily extracted considering the equation which links the desired BER and the SNR required by an OFDM M-QAM modulation [14], reported in (1.3).

$$BER_{M-QAM} = \frac{\sqrt{M}-1}{\sqrt{M}\log_2\sqrt{M}} erfc\left(\sqrt{\frac{3}{2}\frac{\log_2 M}{M-1}SNR}\right) \tag{1.3}$$

In (1.3), $erfc$ is the complementary error function, defined as in (1.4).

$$erfc(x) = \frac{2}{\sqrt{\pi}}\int_x^\infty e^{-t^2}\,\mathrm{d}t \tag{1.4}$$

In the case of a 64-QAM modulation, M is equal to 64. Substituting BER $< 10^{-7}$as required by the system, the corresponding SNR can be easily calculated, obtaining the value in (1.5).

$$SNR_{OUT,dB} > 19.6\,\mathrm{dB} \tag{1.5}$$

On the other side, the value of the required $SNR_{IN,dB}$ can be extracted by using the Friis transmission equation [10] together with the expression of the thermal noise formulated by Johnson and Nyquist [15]. In particular, the power received by the receiver P_r is given in terms of antenna gains (G_r and G_t), transmitted power P_t, distance R and wavelength λ by (1.6),

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi R}\right) \tag{1.6}$$

while the associated noise depends by the temperature T and by the frequency channel width Δf as stated in (1.7) where k_B is the Boltzmann constant.

$$N = k_B T \Delta f \tag{1.7}$$

Considering the values reported in Table 1.2 at the maximum distance $R = 4\,\mathrm{m}$, at the

centre frequency of 61.5 GHz and at the room temperature, the SNR in input can be calculated dividing P_r by N. It has to be noticed that packaging losses and average transmitted power ($P_{out,max}$- PAPR) must be considered within the Friis transmission formula. The obtained value for the input SNR, in decibels, is reported in (1.8).

$$SNR_{IN,dB} = 27.4\,\text{dB} \tag{1.8}$$

Joining the results obtained in (1.5) and (1.8) as in (1.2), it comes out that the required receiver noise figure has an upper limit fixed as in (1.9).

$$NF_{Rx} < 7.8\,\text{dB} \tag{1.9}$$

In order to completely define the receiver specifications, the maximum input power has to be fixed. In fact, the receiver must be able to operate with an acceptable linearity, that is without appreciable distortion, with the strongest possible input signal. Using once again the Friis transmission formula (1.6), this time at the minimum distance of 50 cm and with the maximum transmitted power $P_{out,max}$, the maximum received power can be extracted. The result of such calculation is reported in (1.10).

$$P_{in,max} = -25.2\,\text{dBm} \tag{1.10}$$

The results reported in (1.9) and (1.10) define the main specifications for a receiver which should fulfil the IEEE 802.15.3c standard requirements. Other specifications as power consumption and area occupation are not fixed. Anyway, the aim for any good IC design is to develop small and low power components.

The defined specifications refer to the entire receiver, comprehensive of circuits such as demodulator and further amplification stages. In order to extract the specifications which are of interest for LNA and Mixer designs, a deeper look at the targeted system has to be given.

1.3 System overview

For satisfying the discussed requirements, a concept for a 60 GHz transceiver has to be developed. The chosen system is a fully differential super-heterodyne transceiver,

with a double frequency conversion, the first from the radio frequency (RF) to the intermediate frequency (IF), the second from the IF to the baseband frequency (BB). A block diagram of the transceiver is given in Figure 1.5, where its operation principle can be easily understood. The signal is received by the Rx antenna, amplified maintaining low the noise by the LNA and down converted to the IF by the down conversion mixer (DCM). The IQ demodulator (IQ DEM) converts down the received signal once again, creating two BB signals, one in phase (I) and another in quadrature of phase (Q). In the transmitter chain, the process is performed backwards. The BB IQ signal is up converted two times, the first by the IQ modulator (IQ MOD) and the second by the up conversion mixer (UCM), amplified maximizing the output power by the power amplifier (PA) and transmitted by the Tx antenna. The reference frequency is generated by a phase locked loop (PLL) operating at around 40 GHz and spread by a local oscillator (LO) distribution network, consisting of some amplifiers and power dividers.

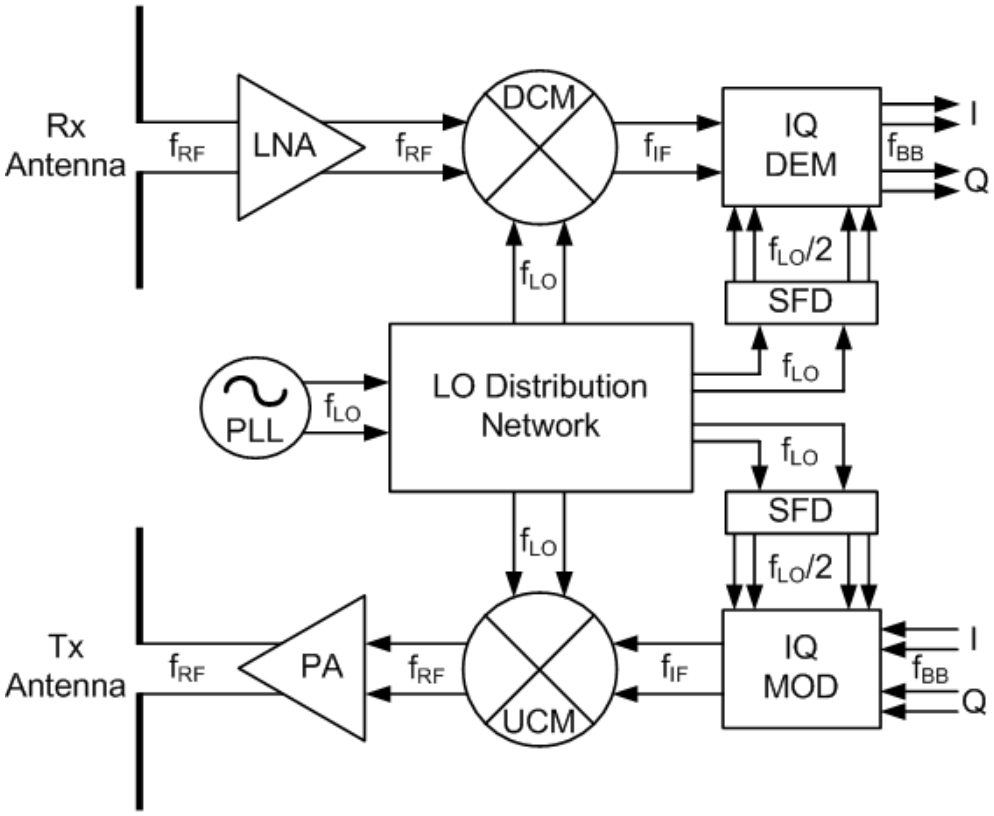


Figure 1.5: Transceiver block diagram.

The static frequency divider (SFD) halves the LO frequency, generating an IQ signal at half the LO frequency and giving it both to the demodulator and to the modulator.

Compared to homodyne systems, based on a single frequency conversion, this concept presents many advantages. Beyond the very well known benefits of any superheterodyne architecture [16], such as the absence of DC offset and self-mixing issues, the presented architecture implies the design of a 40 GHz PLL, which is rather simpler than the design of a 60 GHz one. Furthermore, the huge spacing between RF and LO frequencies facilitates the image rejection at around RF. However, the most important peculiarity of the chosen architecture is the reuse of the same LO signal for both first and second frequency conversions, avoiding an additional PLL at the cost of a static frequency divider, which is much easier to design, less power hungry and less area demanding. This contributes to drastically alleviate the major drawbacks of superheterodyne transceivers, that are complexity, power consumption and integrability.

The choice of a fully differential system is mainly endorsed by a practical reason. At very high frequencies, the ground distribution is a very challenging topic. The inductive impedance offered by a ground network grows with the frequency, becoming sometimes not acceptable. A differential circuit is immune to this issue, since a virtual ground is always created when a differential signal travels. For example, an inductive ground can drop the gain of a single-ended common source amplifier behaving as source degeneration, while in a differential pair this problem is overcome by the virtual ground between the sources of the transistors, created by the opposite polarity of the two signals adding at that node. This concept is visually explained in Figure 1.6.

Most of the blocks have been designed, manufactured and measured by the TU-Berlin MWT group, and some of them published, as PLL circuits [17, 18], power amplifiers [19–21], baseband circuitry [22], LO distribution amplifiers [23, 24], up converter [25], demodulator [26], frequency divider [27, 28] and antennas [29]. A functional on-off keying (OOK) transmitter has also been published [30].

1.4 Receiver specifications extraction

This work is focused on the design of the first two components of the receiver chain depicted in Figure 1.5, namely the LNA and the first down-conversion mixer. Once the transceiver architecture has been fixed, the performance required to the considered

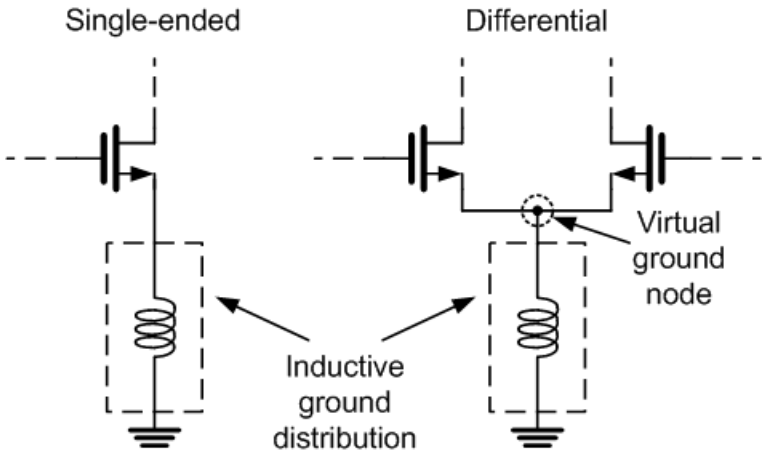


Figure 1.6: Ground distribution in single-ended and differential amplifiers.

circuits can be deduced from the receiver specifications extracted within the previous section. In order to calculate the specifications of the RF to IF receiver, the Friis formula for noise [31], reported in (1.11) for cascaded noise factors, can be used.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots \tag{1.11}$$

In (1.11) G_i is the linear gain of the i-th stage and F_i its noise factor, while F_{total} stands for the noise factor of the cascaded stages. Applying the Friis noise formula in the receiver case, if between mixer and IQ demodulator there is no impedance mismatching the expression in (1.12) can be obtained.

$$F_{Rx} = F_{RFtoIFRx} + \frac{F_{IQDEM} - 1}{G_{RFtoIFRx}} \tag{1.12}$$

Being F_{Rx} fixed by the system specifications to be smaller than 7.8 dB and assuming a reasonable value for the demodulator noise figure F_{IQDEM}, let us say 10 dB (easily achievable by using a simple IF buffer at the demodulator input), a $G_{RFtoIFRx}$ of 10 dB and a $NF_{RFtoIFRx}$ of 7 dB satisfy the system requirements. Regarding the maximum input power, the value previously found and reported in (1.10) is still valid for the considered circuital block. A summary of the receiver specifications is given in Table 1.3.

The extracted receiver specifications reported in Table 1.3 are the starting point for

Table 1.3: Receiver specifications

Gain	10 dB
Noise figure	7 dB
Maximum input power	-25.2 dBm
RF frequency range	57.24 – 65.88 GHz
IF frequency range	18.36 – 22.68 GHz
LO frequency range	38.88 – 43.2 GHz

the designs within this work. The extraction of the specifications of LNA and mixer is now straightforward. An overall gain of 10 dB can be achieved amplifying of 15 dB through the LNA and limiting the losses of the down converter to 5 dB. Applying once again the noise Friis formula under the condition that at interface between LNA and down converter there is no impedance mismatching, it can be found that an LNA with a noise figure of 6.6 dB followed by a down converter with a noise figure of 12 dB satisfies the noise receiver specifications. In terms of maximum input power, the one of the LNA is already fixed at -25.2 dBm by the receiver specifications. Considering a maximum LNA gain of 22 dB in the band of interest, the maximum power at the down converter input results to be -3.2 dBm. The just calculated LNA and mixer specifications are summarized in Table 1.4 and Table 1.5 respectively. It has to be remarked that the performance presented here as specifications have to be taken as worst case performance. In fact, both LNA and down converter behaviours, as for any microwave circuit, will be strongly frequency dependent. This means that they have to fulfil the extracted specifications also in the frequency points where their operation is not optimal.

Before proceeding with the planned designs, a brief look at the used CMOS technology is given within the next chapter.

Table 1.4: LNA specifications

Gain	15 dB
Noise figure	6.6 dB
Maximum input power	-25.2 dBm
RF frequency range	57.24 – 65.88 GHz

Table 1.5: Down converter specifications

Conversion Gain	-5 dB
Noise figure	12 dB
Maximum input power	-3.2 dBm
RF frequency range	57.24 – 65.88 GHz
IF frequency range	18.36 – 22.68 GHz
LO frequency range	38.88 – 43.2 GHz

Chapter 2

TSMC 90 nm CMOS Technology

In the last years, the development of semiconductor technologies, driven mainly by digital circuits, has encountered an exponential acceleration. The need of pushing down the fabrication costs led to a growing interest in the downscaling of the chip size and in the integration of different circuits into a single chip.

CMOS transistors are up to now the undisputed leaders of the digital world. Their strong switching capability and their relatively cheap fabrication process made this technology the worldwide most used one. The request of miniaturization caused a continuous size shrinking to the deep-sub-micron region. In fact, many foundries are nowadays able to manufacture transistors whose channel length is only some tens of nanometres. These technological developments made the integration of digital and analogue circuits on the same chip realistic. The introduction of ultra-thick low-losses metal layers gives also the possibility of designing inductors and transmission lines with an acceptable quality factor, making the integration of high frequency components also possible. Anyway, many drawbacks have to be taken into account, as the poor performance of the CMOS RF transistors compared with other technologies, worsened in the deep sub-micron region by short channel effects, and the relatively low silicon substrate resistivity: the design of CMOS RF circuits, especially at high frequencies, is still a very challenging research topic.

The Taiwan Semiconductor Manufacturing Company (TSMC) is offering access to a low-power 9-layers 90 nm CMOS technology called CMN90LP. Widely used for commercial digital circuits, this technology provides also RF transistors with very high transition (f_t) and maximum oscillation (f_{max}) frequencies, and an ultra-thick metal

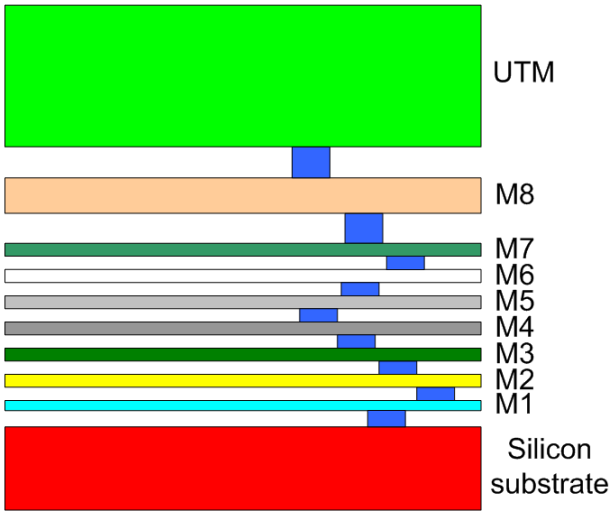


Figure 2.1: CMN90LP Cross-section.

layer, the uppermost, to be used for inductive components. The supply voltage is nominally 1.2 V. Thanks to its capabilities, the CMN90LP technology has been chosen for the manufacture of all the circuits designed within the WiONet project. The cross-section of the used technology is shown in Figure 2.1. The uppermost layer, called Ultra-Thick-Metal (UTM), is used for inductive components, while the thinner metal layers are used for interconnections. All the metal layers are made by copper.

2.1 Pads and feeding structures

An additional aluminium layer is provided by the foundry to be used exclusively as signal pad. Since pads are needed in all the designs to connect the on-chip circuits to the external world, either through probes or through wire bonds, a good modelling of such structures is required for successful measurements. The designed pads are 82 µm long and 47 µm wide, with 100 µm pitch between two consecutive pads. In the present technology, stringent design rules do not allow to place other structures in the neighbourhood of the pads. To overcame this issue, a 50 µm long grounded coplanar transmission line (GCTL) with a characteristic impedance of 50 Ω is used to feed the devices under test (DUT), tapered at one side to alleviate transition effects between the large pad and the tiny line. A sample layout of the pad plus the described feeding

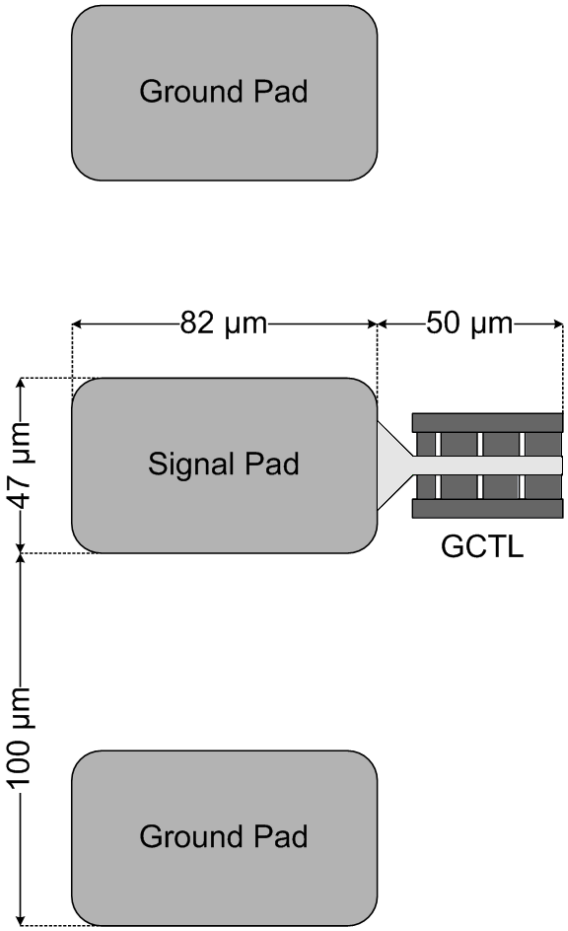


Figure 2.2: GSG pads and GCTL feeding structure.

structure in a ground-signal-ground (GSG) configuration is given in Figure 2.2.

In order to characterize the considered structure, a 100 µm long GCTL has been interspersed between two of them, one as input and one as output, and the whole structure manufactured. As described in [32], the scattering parameters of the designed pad structures can be extracted solving some matrix equations by means of numerical solvers. The so found scattering parameters can then be used in simulation to represent the pads effects.

The extraction technique has been then validated. The considered ground-signal-ground pad structure has been manufactured both in short and open configuration. The comparison between extracted and measured results is shown in Figure 2.3. The closeness of the curves in Figure 2.3 proves the accuracy of the used extraction technique.

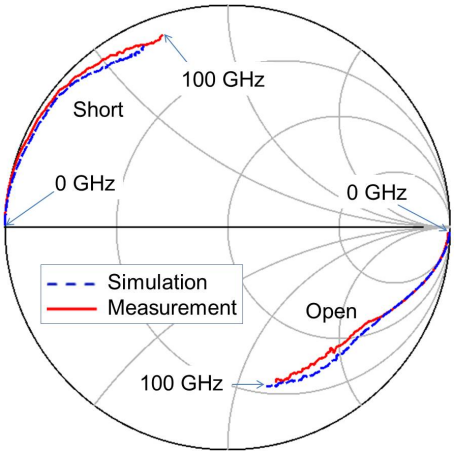


Figure 2.3: Simulated and measured return losses of the considered structure under open and short conditions.

In all the following designs, the extracted scattering parameters have been used in simulation for taking into account input and output pads.

2.2 MOS transistors

The technology provides RF multi-finger triple-well MOS transistors, whose cross-section looks like the one in Figure 2.4. All the terminals are brought out on the third metal layer (M3). The triple-well characteristic provides, besides a better isolation, the possibility to bias substrate, nMOS bulk and pMOS bulk separately.

The used model is based on a standard MOS model developed by the Berkeley

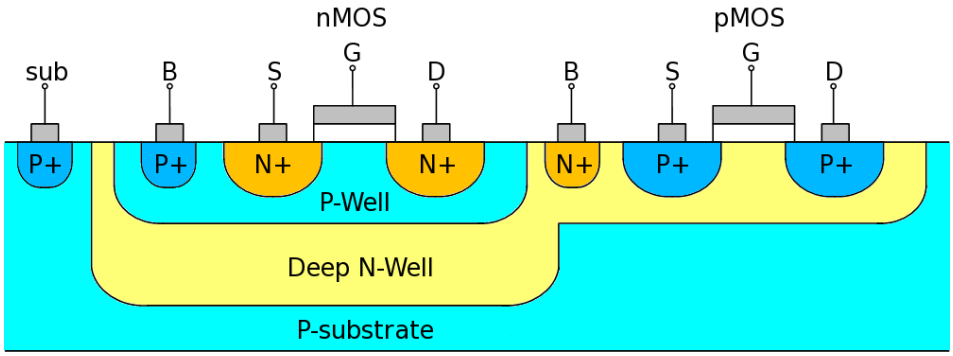


Figure 2.4: Triple-well MOS Cross-section.

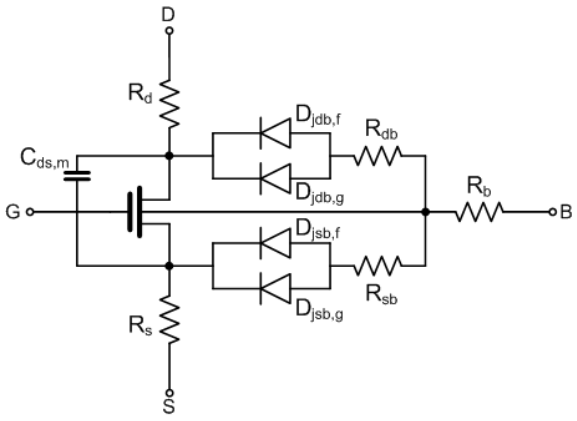
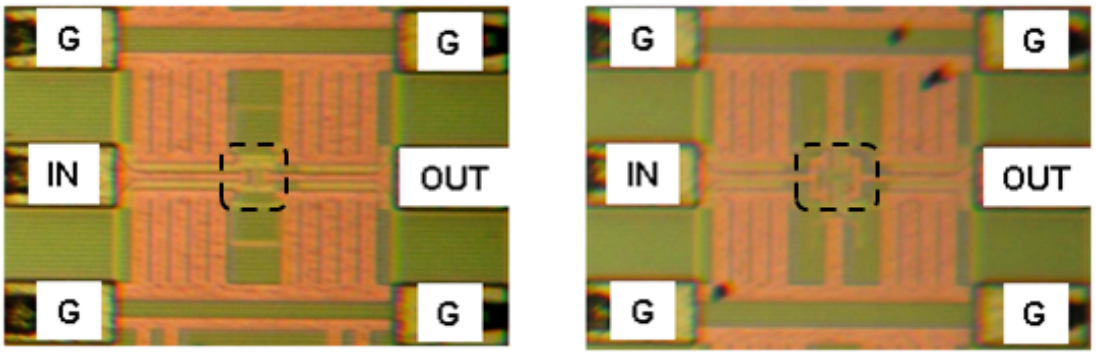


Figure 2.5: CMN90LP MOS equivalent model.

university, the BSIM model. To be more precise, the considered model is a BSIM4-based model with some additional parasitics given by the connections. An equivalent model is shown in Figure 2.5, where a BSIM4 core is surrounded by the extrinsic parasitics typical of the considered technology. The parasitics added to the BSIM4 core in Figure 2.5 take into account the substrate resistivity (R_{sb}, R_{db}, R_b), the effect of metallic connections at the terminals (R_s, R_d, $C_{ds,m}$) and the parasitic drain-bulk and source-bulk junctions ($D_{jdb,f}$ and $D_{jsb,f}$ model area and field-edge sidewall effects, while $D_{jdb,g}$ and $D_{jsb,g}$ model gate-edge sidewall effects). The BSIM4 MOS core takes into account all the main features of short channel devices, as reported in the BSIM manual [33].

The transistor model is guaranteed by the foundry up to 30 GHz. In order to test the functionality of the model and its deviation from the real device at higher frequencies, some test transistors have been printed out and measured [34]. In particular, two transistors having gate width of 25 µm and 80 µm respectively have been characterized at various bias points up to 110 GHz. Their chip micrographs are shown in Figure 2.6. Figure 2.7 shows the 3D view of the transistors access network. Gate and drain terminals are connected through a via stack to the lines carrying output and input signals, while source and bulk are connected to the closest possible ground, represented in this case by the grounded walls of the coplanar input and output lines.

Figure 2.8 shows the comparison between measured and simulated insertion losses of the two structures at the fixed gate bias of 800 mV. Simulated and measured in-



(a) (b)

Figure 2.6: Chip micrograph of the structures containing (a) the 25 µm and (b) the 80 µm MOS transistors. The transistors are highlighted.

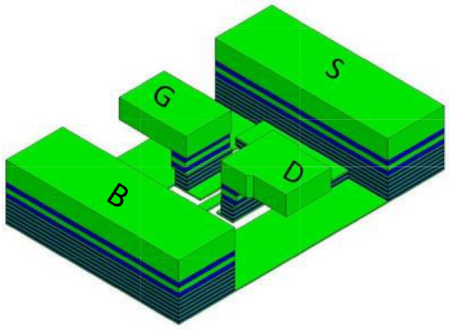
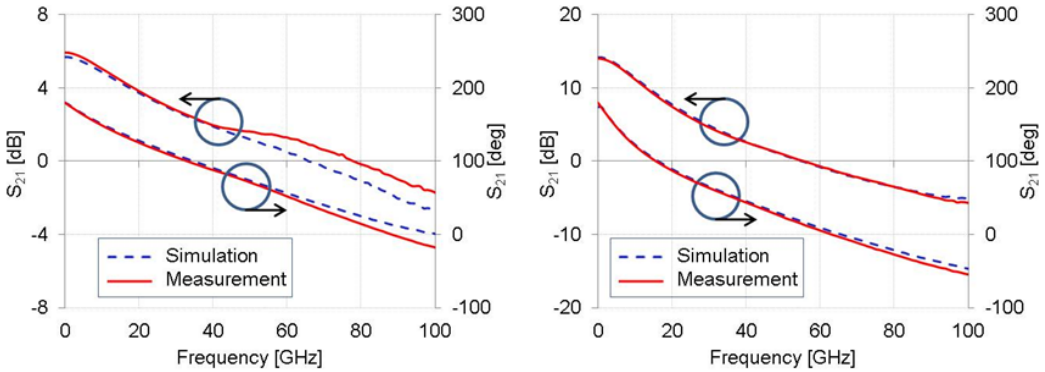
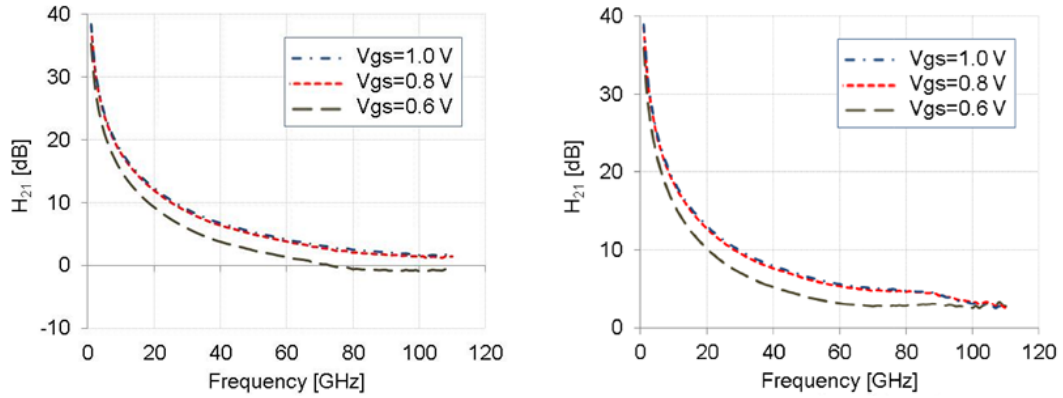


Figure 2.7: 3D view of the transistor access network.



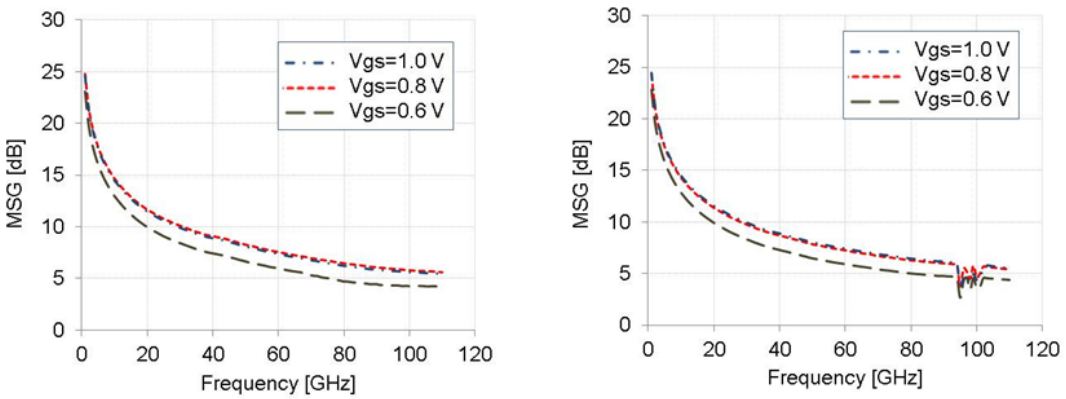
(a) (b)

Figure 2.8: Insertion loss (S_{21}) of the structures containing (a) the 25 µm and (b) the 80 µm MOS transistors.



(a) (b)

Figure 2.9: Current gain (H_{21}) (a) of the 25 µm and (b) the 80 µm MOS transistors (extracted from s-parameters measurements).



(a) (b)

Figure 2.10: Maximum stable gain (MSG) (a) of the 25 µm and (b) the 80 µm MOS transistors (extracted from s-parameters measurements).

sertion losses agree very well each other, except a little discrepancy for the 25 µm transistor above 40 GHz. After an accurate de-embedding of the feeding structures, the performance of the transistor core can be extrapolated. The f_t of the two transistors can be seen looking at the current gains plotted in Figure 2.9, while their f_{max} can be extracted from the maximum stable gain plots of Figure 2.10.

From these plots, it can be seen how both f_t and f_{max} are placed for the two MOS above 110 GHz in saturation region (that is for gate voltages greater than 600 mV). At around 60 GHz, which is here the frequency of interest, a single transistor could

guarantee a maximum stable gain between 5 dB and 8 dB, as visible in Figure 2.10.

2.3 Inductive components

In every RF integrated circuit, most of the chip area is occupied by inductors and transmission lines. Very often, the quality of their performance is the key of the success of an high frequency design. Therefore, inductive elements with very high self-resonance frequency and acceptable quality factor are needed.

TSMC includes into its library some inductors already laid out and modelled. Unfortunately, they are quite big and their self resonance frequency is most of the times not enough for our purposes. That is why the inductive elements to be used in all the circuits of the present designs have been self designed and characterized through EM simulations and on-wafer measurements.

2.3.1 Inductors

The most area-saving option to design integrated inductive components is offered by spiral inductors. But at very high frequencies, the inter-spiral capacitance becomes high, dangerously lowering their self-resonance frequency. Anyway, single-turn inductors do not suffer from this problem, and are good candidates to be used at 60 GHz. Two different test inductors providing inductances of about 150 pH and 250 pH have been designed, EM simulated and measured [35]. They are single-turn inductors, designed on the UTM metal layer to minimize the losses and with the addition of an electromagnetic shield on M1, which decouples the inductor from the substrate increasing both its quality factor and its self-resonance frequency [36]. Their chip micrograph is shown in Figure 2.11, while simulations and measurements of their inductance and their quality factor are given in Figure 2.12.
After deembedding the pads, inductance and quality factor have been calculated using Y and Z parameters with the well known formulas here reported in (2.1) and (2.2).

$$L = \frac{Im\{Y_{21}\}}{2\pi f(Im\{Y_{21}\}^2 + Re\{Y_{21}\}^2)} \tag{2.1}$$

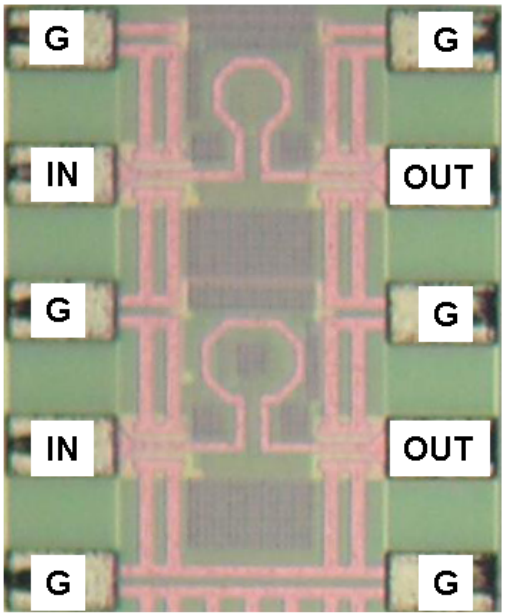


Figure 2.11: Inductors chip micrograph.

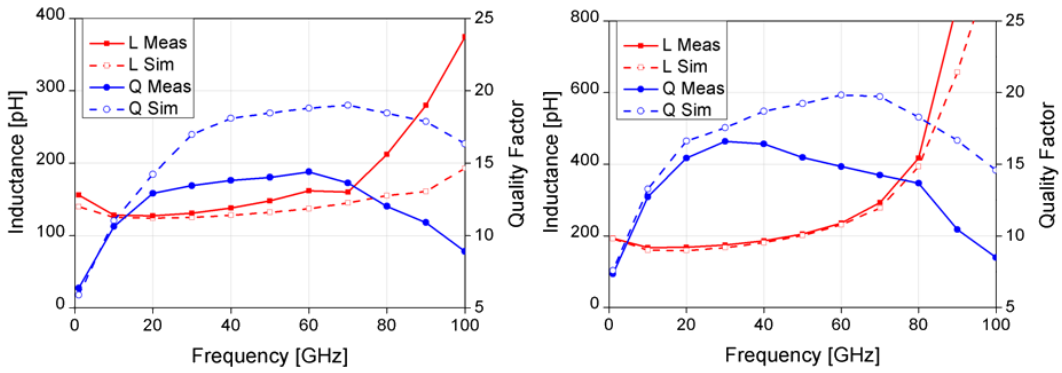


Figure 2.12: Inductance and quality factor of (a) the 150 pH inductor and (b) the 250 pH inductor.

$$Q = -\frac{Im\{Y_{11}\}}{Re\{Y_{11}\}} \tag{2.2}$$

The plots in Figure 2.12 show how the measured quality factors are smaller than the simulated ones, especially after 20 GHz. This is mostly due to the dummy fillers required from the technology. In fact, the current flowing on the lines couples to the

dummy fillers causing eddy currents which enlarge the losses of the structure [37]. Furthermore, their impact is hardly predictable since they cannot be included effectively into EM simulations. This is the main reason why this kind of inductors have not been used for 60 GHz designs, but only at lower frequencies where the dummy fillers impact is less prominent.

2.3.2 Transmission lines

In order to avoid the use of fillers, giving a better reliability to the simulations, the use of coplanar transmission lines has been taken into account [38]. The cross-section of a coplanar transmission line is the one depicted in Figure 2.13, where W is the line width and S the spacing between line and side walls. The use of grounded side walls, besides providing an electro-magnetic isolation to the lines, increases the metal density in the proximity of the signal line removing the need of dummy fillers in critical zones. On top of that, the absence of any inter-spiral capacitance allows to have a very high self-resonance frequency. The isolation from the substrate is given by a shield on M1. On the shape of this shield is based the distinction between two different types of transmission lines: Grounded Coplanar Transmission Lines (GCTL) and Shielded Coplanar Transmission Lines (SCTL) [39].

2.3.2.1 Grounded Coplanar Transmission Lines

Grounded Coplanar Transmission Lines (GCTL) have a shield consisting of wide M1 blocks. The three dimensional (3D) and the bottom views of a GCTL are shown in Figure 2.14, where W_1 is the width of the M1 shield block and S_1 the spacing between two consecutive blocks. TSMC technology density rules limit the M1 blocks to

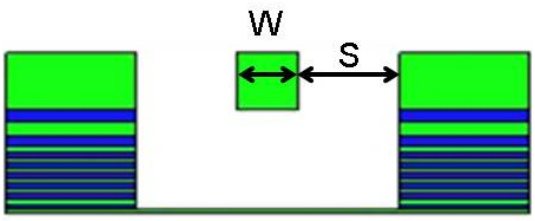
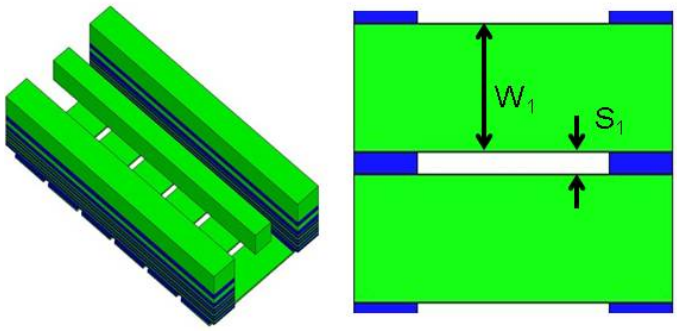


Figure 2.13: Coplanar transmission line cross-section.



(a) (b)

Figure 2.14: GCTL (a) 3D view and (b) bottom view.

have W_1 of 9 μm and S_1 of 1.5 μm. This kind of transmission line offers a rather low characteristic impedance, due to the high capacitance between line and shield, and a not optimal quality factor, due to the lossy eddy currents induced on the conductive shield. These effects can be seen from Figure 2.15, where the EM simulated characteristic impedance (Z_c) and line losses are depicted for a GCTL with various values of line width W and line to wall spacing S.

In order to validate the simulations, a GCTL 100 μm long, 5 μm wide and with a spacing of 7.5 μm has been manufactured and measured up to 100 GHz. The measured inductance, after pads de-embedding, is shown in Figure 2.16, where it is also compared with the EM simulated one. The curves of Figure 2.16 show a higher inductance value at low frequencies, behavior strictly connected to the skin effect. In fact, the in-

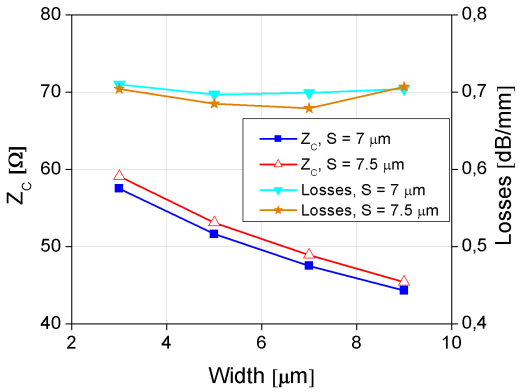


Figure 2.15: Simulated GCTL characteristic impedance and losses at 60 GHz.

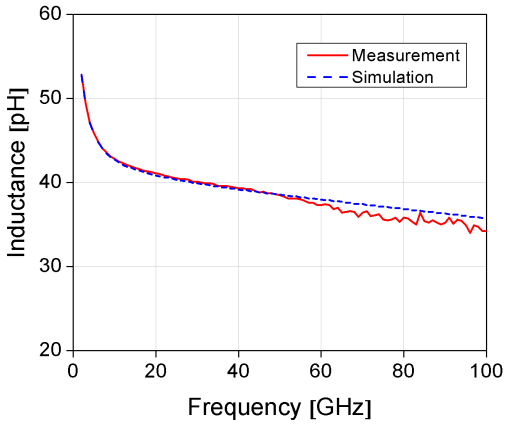


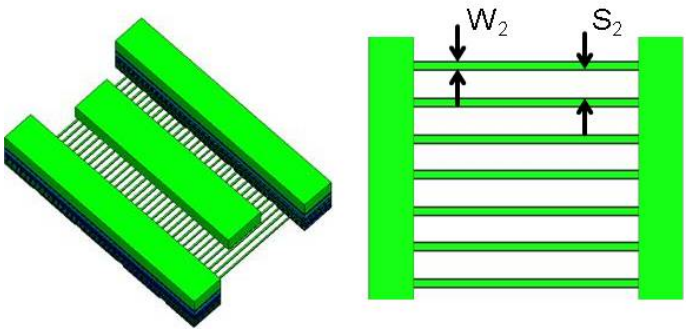
Figure 2.16: Inductance of a GCTL with L = 100 µm, W = 5 µm and S = 7.5 µm.

ductance of a wire can be divided into external and internal inductance, the first being constant in frequency and the second directly proportional to the skin depth. At high frequencies, the skin depth becomes very low, making the total inductance approximately equal to the external term, therefore lower then its low frequency value which includes both inductance components [40].

The low characteristic impedance of the GCTL makes it appropriate to be used as 50 Ω line, but not as inductor. In particular, a GCTL with 5 µm width W and 7.5 µm spacing S will be used as connection where the impedance is required to remain 50 Ω and no impedance transformation is needed, as in the already discussed feeding structures.

2.3.2.2 Shielded Coplanar Transmission Lines

A shield made of very tiny M1 stripes, as the one depicted in Figure 2.17, is a good way to reduce the line to shield capacitance and to cut the eddy currents coupled to the shield. TSMC technology density rules fix the size of the M1 stripes, which have W_2 of 0.3 µm and S_2 of 1 µm. Such a shield can therefore at the same time increase the characteristic impedance of the line and lower its losses. EM simulations confirm this feeling, as can be understood looking at the simulated results of Figure 2.18 which shows characteristic impedance (Z_c) and line losses of a SCTL with various values of line width W and line to wall spacing S.



(a) (b)

Figure 2.17: SCTL (a) 3D view and (b) bottom view.

A 100 µm SCTL having W of 8 µm and S of 9.5 µm has been also manufactured in order to confirm the simulated results. Figure 2.19, where simulated and measured inductances are compared, shows the accuracy of the simulation process, except some calibration problems beyond 70 GHz. Thanks to its high characteristic impedance and low losses, SCTLs will be used as inductors in the matching networks to be designed.

SCTLs will be very extensively used, and successful designs cannot be performed without an optimization and a deep characterization of this kind of structures. Given the inherently low SCTL losses, the other characteristic that has to be maximized is the inductance per unit length. Indeed, highly inductive structures allow to reduce consistently the lines length, and in general the area occupation of the circuits to be designed. In order to enlarge the inductivity, the line width has to be reduced as much

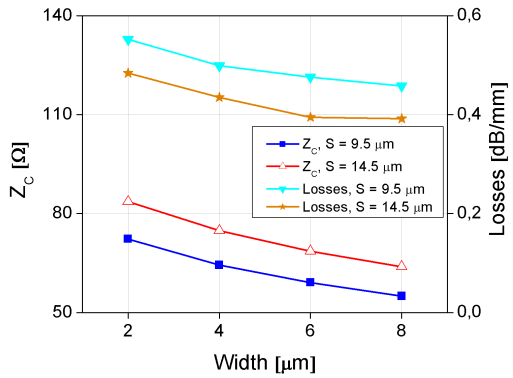


Figure 2.18: Simulated SCTL characteristic impedance and losses at 60 GHz.

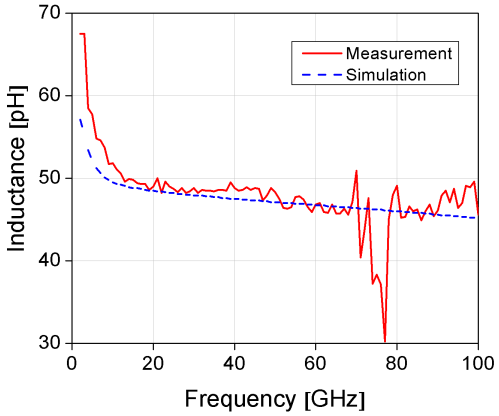


Figure 2.19: Inductance of a SCTL with L = 100 µm, W = 8 µm and S = 9.5 µm.

as possible while the ground walls have to be brought as far as possible from the line. Therefore, a width of 3 µm, 1 µm larger than the technology limit, and a spacing of 12 µm, the biggest spacing which guarantees to fulfil the density technology rules, have been chosen.

In order to avoid a large amount of EM simulations and speed up the design process, a simple lumped elements model has been developed for the optimized SCTL [41]. To make it scalable in length, a model of a 10 µm long SCTL has been developed, consisting of a series resistor, a series inductor and a shunt capacitor as visible in Figure 2.20. SCTLs with length multiple than 10 µm will be a cascade of a corresponding number of 10 µm blocks. In Figure 2.20, the inductor L is the inductance of the line, the capacitor C is a sum of the capacitance to the grounded side walls and the capacitance to the M1 shield, while the resistor R represents the ohmic losses of the structure, which after a certain frequency are dominated by the skin effect and can be

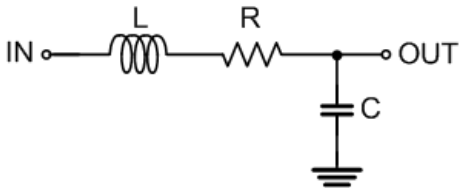
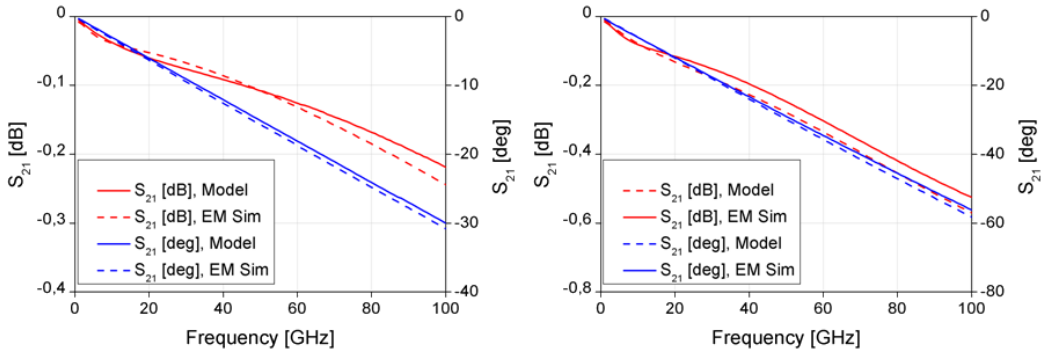


Figure 2.20: Lumped model of 10 µm of the optimized SCTL. The values of the components are L = 5.8 pH, R = 0.8 Ω and C = 1.06 fF.



(a) (b)

Figure 2.21: Model fitting of (a) 100 µm and (b) 200 µm optimized SCTLs. Both lines have W = 3 µm and S = 12 µm.

considered constant in frequency, but at lower frequencies are frequency dependent. The values of C, L and R have been fit until the scattering parameters of the lumped model have met the EM simulated ones. The result of such a fitting is shown in Figure 2.21, where lumped model and EM simulations are compared in terms of magnitude in decibels and phase of the insertion loss S_{21} for two different line lengths (100 µm and 200 µm).

2.4 MIM capacitors

Various kinds of capacitors are provided by TSMC. Among them, Metal-Insulator-Metal (MIM) capacitors are capable to guarantee very high self-resonance frequency together with low losses. The addition of a metal shield improves the isolation between capacitor and substrate. The cross section of the used MIM capacitors is given in Figure 2.22. The MIM capacitor is sandwiched between M8 and M7. The two plates, called Capacitor-Bottom-Metal (CBM) and Capacitor-Top-Metal (CTM), are separated by a very thin dielectric and connected through vias to M8, where both the terminals of the capacitor are located. M5 and M6 together constitute the shield. Also capacitors have been manufactured and measured to test their functionality at high frequencies [32]. In particular, a 470 fF capacitor, that is a square capacitor with an area of 225 μm^2, has been considered for this test, and its chip micrograph is shown in Figure 2.23. The measured return loss of such a capacitor is compared with the simulated

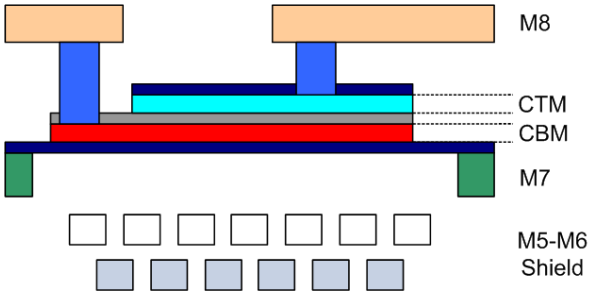


Figure 2.22: Shielded MIM cross-section.

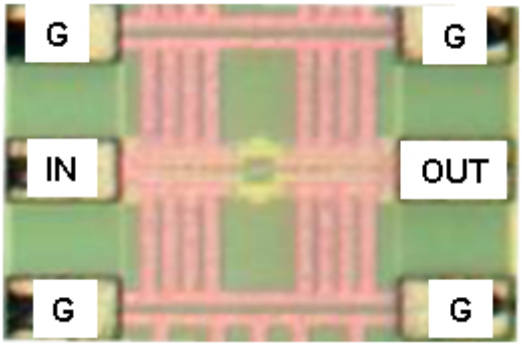


Figure 2.23: Chip micrograph of the considered MIM capacitor.

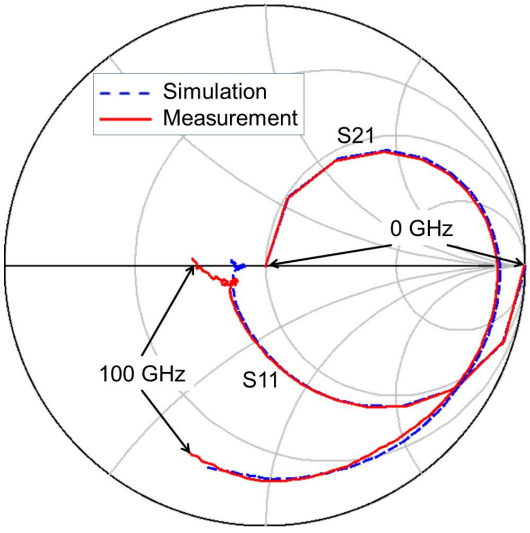


Figure 2.24: Simulated and measured return loss of the considered MIM capacitor.

one up to 100 GHz in Figure 2.24. The closeness of the two curves shows once again the goodness of the extraction technique up to 100 GHz.

2.5 Resistors

The used resistors have to provide high resistance in a very small area. The used ones are polysilicon resistors, consisting simply of a polysilicon strip with the two terminals carried out on M1. Usually, resistors are used in RF designs only to improve isolation on DC paths or for power amplifiers stabilization networks, therefore the accuracy of the model is not required to be very high. This is the reason why their behaviour and the validity of their model have not been further investigated.

2.6 Varactors

Variable capacitors are needed for VCO design, therefore they will not be used by the circuits described within this thesis. Their characterisation is anyway important for the PLL included into the WiONet system and is here discussed for completeness.

The TSMC technology makes available CMOS varactors, which are, at a first sight, MOS transistors where source and drain are connected together. Their equivalent capacitance, that is mostly the junction capacitance between the source-drain terminal and the gate terminal, can be adjusted varying the gate voltage.

The CMOS varactors model given by the foundry has been tested considering variable tank circuits designed using such devices [42]. In particular, two tanks, the first using a 16 fingers varactor and resonating at around 50 GHz and the second using a 13 fingers varactor and resonating at around 60 GHz, have been simulated, manufactured and measured. The chip micrograph of one of them is visible in Figure 2.25. Both tanks use the same inductor, which has already been measured [35], and the same feeding structures [32], already discussed. The varactor admittance matrix $[Y_{var}]$ has been then extracted as in (2.3), where $[Y_{tank}]$ is the admittance matrix of the whole tank and $[Y_{ind}]$ the one of the inductor stand-alone.

$$[Y_{var}] = [Y_{tank}] - [Y_{ind}] \tag{2.3}$$

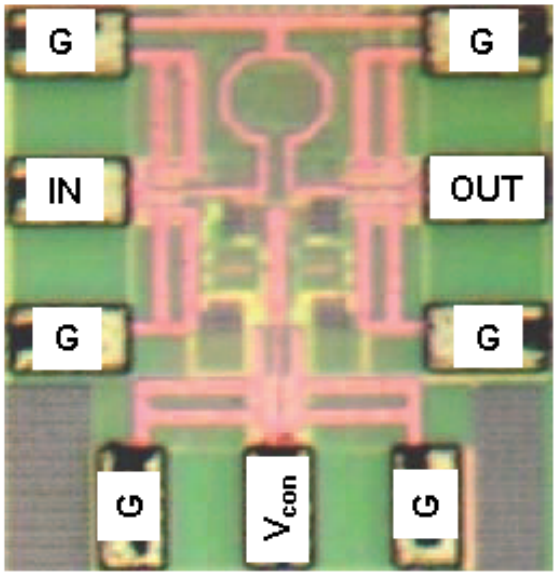


Figure 2.25: Tank micrograph.

Simulations have been performed using the measured inductor, the feeding structures scattering parameters and the varactor extracted as in (2.3), and in a second time they have been compared with the measurements of the complete tank structure. Both simulations and measurements are carried out within a single port environment, where the resonance is described by a peak in the real part of the parallel impedance parameter Z_{11}. This comparison is shown in Figure 2.26 for the 50 GHz tank and in Figure 2.27 for the 60 GHz one for various values of the control voltage V_{con}. In both circuits, a tuning range larger than 30 GHz has been achieved. The similarities between simulations and measurements underline the validity of the extraction technique.

All the components needed for the designs to be done are verified. Both active and passive elements show an acceptable behaviour at the frequency of interest. The closeness between measurements and simulations show that the simulation process is reliable and can be further used for the development of all the circuits to be designed. The results presented in this section are a precious background for the designs of all the circuits of the WiONet system, and in particular of the LNA and the down converter whose design process, simulations and measurements will be presented within the next two chapters.

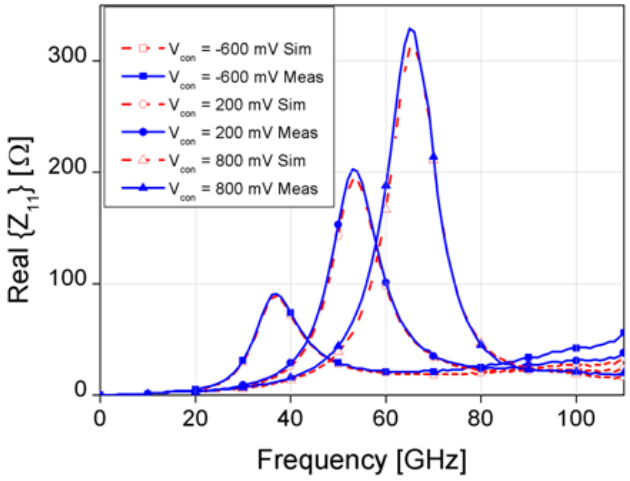


Figure 2.26: Real part of the parallel impedance Z_{11} of the 50 GHz (16 fingers varactor and 250 pH inductor) tank.

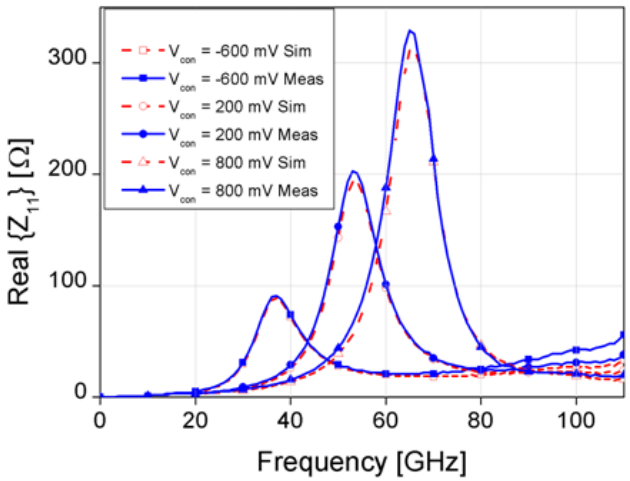


Figure 2.27: Real part of the parallel impedance Z_{11} of the 60 GHz (13 fingers varactor and 250 pH inductor) tank.

Chapter 3

Low Noise Amplifier Design

As already stated in Chapter 1, this thesis is focused on the design of the first part of the WiONet receiver chain, consisting of a 60 GHz LNA and a 60 GHz to 20 GHz down converter. The first circuit in this chain, coming straight after the antenna, is the LNA. Its main role is to amplify the signal adding as low noise as possible, ensuring anyhow a good linearity and maintaining low both the power consumption and the area occupation.

The minimum noise figure of a transistor is a technological parameter, and it can be achieved theoretically transforming the source impedance, that is usually 50 Ω, to a certain input optimum impedance $Z_{in,opt}$. Anyway, most of the times the $Z_{in,opt}$ does not correspond to an acceptable power gain and a trade-off between the two performance is needed.

In the following sections, after an introduction about noise sources in CMOS circuits, the research process which led to the design chosen for being part of the WiONet system will be presented.

3.1 Noise in CMOS devices

In MOS devices, the noise has many different natures. Table 3.1 lists the main noise sources [43], along with some comments on their most important dependencies. Table 3.1 shows how the shot component has usually a very light influence in CMOS device, where the gate DC current is ideally zero and in reality only given by negligible leakage, while flicker and popcorn noise can be neglected at very high frequency.

Table 3.1: MOSFET noise sources

Noise type	**Main dependencies**
Thermal	Temperature ($\propto T$)
Shot	Gate DC current ($\propto I_G$)
Flicker	Frequency ($\propto 1/f$)
Popcorn	Frequency ($\propto 1/f^2$)

Many models have been developed for describing the noise sources peculiar of CMOS devices [44]. One of the most used, which can be found in [45], includes a drain noise current [46] and a gate noise current [47], and it is reported in Figure 3.1. At very high frequency, that is without flicker noise contribution, the two noise currents $\overline{i_{nd}}$ and $\overline{i_{ng}}$ can be written by mean of their power spectral densities as in (3.1),

$$\begin{aligned} \overline{i_{nd}^2} &= 4kT\gamma g_{d0}\Delta f \\ \overline{i_{ng}^2} &= 4kT\delta\frac{|Y_{gs}|^2}{5g_{d0}}\Delta f \end{aligned} \tag{3.1}$$

where g_{d0} is the drain-source conductance at zero drain-source voltage and Δf the noise bandwidth. The two noise coefficients γ and δ are called drain and gate noise coefficients respectively, and their values are 2/3 and 4/3 for long channel devices. The gate induced thermal noise grows as the frequency increases, since the gate-source

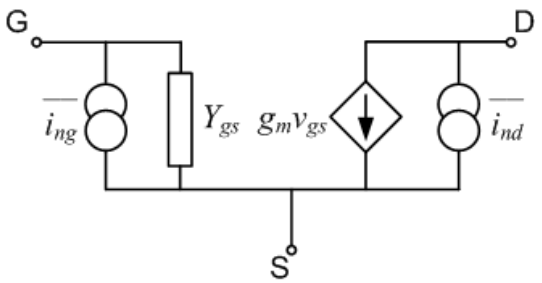


Figure 3.1: MOS noise model.

admittance Y_{gs} is directly proportional to the operating frequency. These two sources are also partially correlated through a correlation factor c defined as in (3.2), which has a value of j0.395 for long channel devices.

$$c = \frac{\overline{i_{ng} i_{nd}}^*}{\sqrt{\overline{i_{ng}^2} \times \overline{i_{nd}^2}}} \tag{3.2}$$

Anyway, an exact quantitative analysis is quite difficult, since an exact estimation in short channel regime of the coefficients introduced in (3.1) and (3.2) is not available at the authors knowledge. Only trends on their values are available:

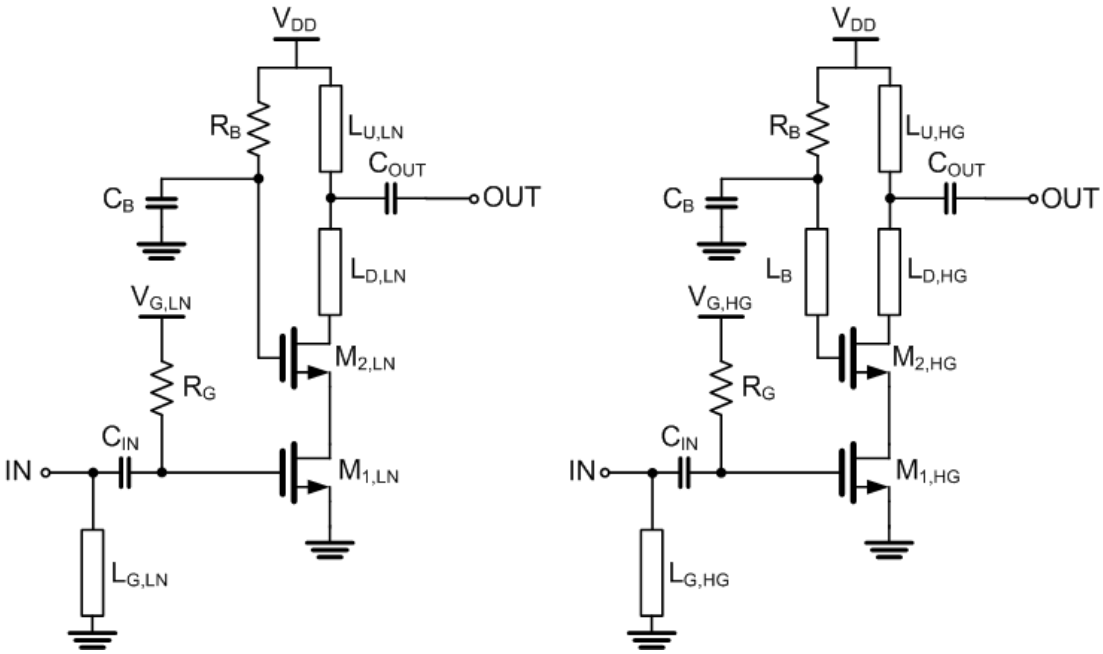
- γ has been proved to be bigger than 2/3 in short channel regime [48].
- δ could be roughly assumed twice as big as γ [43].
- The noise sources of the MOS noise model have been demonstrated to lose gradually their correlation with the device miniaturization [49]. As a consequence, $|c|$ becomes close to 0.1 for short channel devices.
- g_{d0}, equal to g_m for long channel devices, becomes smaller than g_m as the channel size shrinks [43].

In spite of everything, the model in Figure 3.1 is still a simple and effective way to understand and outline the noise sources inside an RF MOS device.

3.2 Single ended cascode LNAs

The cascode topology is one of the most widely utilized in the LNA design. With respect to the common source topology, it provides a better isolation between the output and the input ports, which improves its stability and eases the matching network design, and provides a better bandwidth due to the reduction of the Miller capacitance. On the other hand, it has worse large-signal linearity due to the lower available output voltage swing [50]. The issue regarding its noise figure will be addressed later within this chapter.

To get start with LNA design, two single-stage single-ended 60 GHz LNAs based on the cascode topology have been designed, manufactured and measured [51]. They



(a) (b)

Figure 3.2: Schematic of the (a) low-noise and (b) high gain cascode LNAs.

are designed for two different purposes. While the first one has been optimized to achieve a low noise figure, the second has the goal to have a gain as high as possible. Both amplifiers are intended to be cascaded in a multi-stages LNA configuration, the low noise one as early stage and the high gain one as subsequent stage. The schematics of the two designed stages are shown in Figure 3.2.

As these amplifiers are designed for two different purposes, some differences exist between them. These differences lay mainly in the size of the transistors and the matching networks. Also, the presence of the inductive element L_B on the gate of the common gate transistor of the high gain stage $M_{2,HG}$ resonates out, around the desired frequency, the capacitance between the two transistors, resulting in a peaking of the power gain [52]. On the other hand, the insertion of this inductance makes the amplifier less stable. L_B has to be designed keeping a reasonable amplifiers stability margin. C_{OUT} and C_{IN} are used for blocking the DC signal, in other words as DC-block capacitors, while C_B represents the capacitances used as RF ground. The resistors R_G and R_B allow the correct biasing of the amplifiers.

A crucial design step is the transistors sizing. From the simulation results reported

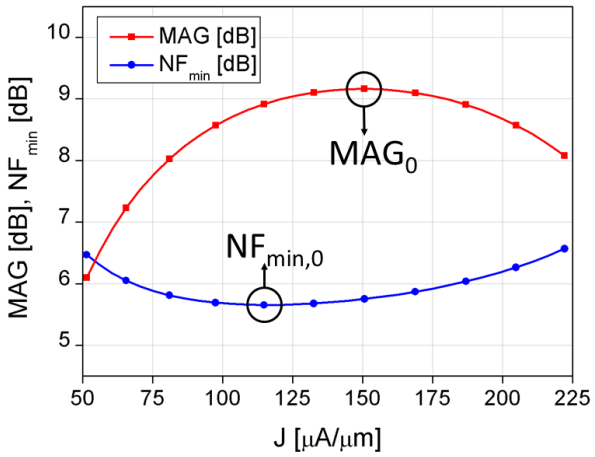


Figure 3.3: Cascode sizing: choice of the bias current density for maximum MAG and minimum NF_{min}.

in Figure 3.3 it can be seen how a current density of 150 μA/μm maximizes the maximum available gain (MAG) while a current density of 120 μA/μm minimizes the minimum noise figure (NF_{min}), in agreement with the results reported in literature [53]. Based on these results, the current density has been fixed and the transistor size swept in simulation. The choice of the size is based on a trade-off between gain, noise figure, output and input impedance (optimum noise input impedance in the case of the low noise stage). The selection process is better explained by the plots in Figure 3.4 and in Figure 3.5, where maximum available gain, minimum noise figure and impedances are plotted for different transistor sizes at the constant current densities previously found. The used technology is a multi-finger technology, so that the degrees of freedom in the choice of the transistor size are two, the finger width and the number of fingers. Anyway, transistors with a lot of fingers would be very long implying a big step when a line has to be connected to their terminals. This is the main reason why transistors with no more then 20 fingers have been chosen. As the theory says [54], a large number of fingers has a beneficial effect on the noise, since it reduces the gate resistance. In fact, the low noise stage uses transistors with more fingers then the high gain stage. The presented optimization process brought to the selection of the transistors listed in Table 3.2.

After the sizing of the active devices, a noise matching has been performed for the noise-optimized amplifier, a classic conjugate matching for the gain-optimized one.

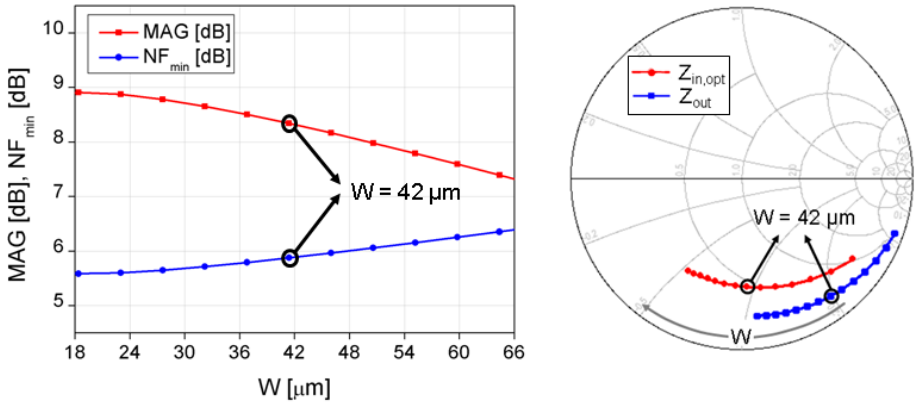


Figure 3.4: Cascode sizing: choice of the transistor size of the low noise stage (fixing the current density to J = 120 µA/µm).

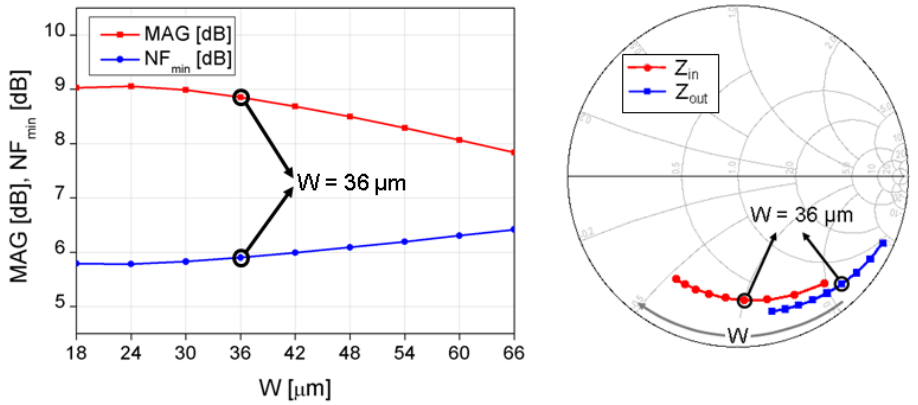


Figure 3.5: Cascode sizing: choice of the transistor size of the high gain stage (fixing the current density to J = 150 µA/µm).

The used inductive components are the SCTL previously introduced, having a width of 3 µm and a spacing of 12 µm. In Table 3.2 the dimensions of the passive components used in the matching networks of both amplifiers are listed as well. It has to be noticed how some T-junctions are inserted in the design for layout purposes. Even if they are not reported in the schematics of Figure 3.2, they have a very important impact on the performance of the amplifier and have to be considered during the simulation process. A trained eye can notice their presence in the chip micrographs of Figure 3.6, where the manufactured layouts of the two amplifiers are reported.

Large-signal, small-signal and noise measurements have been performed on-wafer.

Table 3.2: Cascode LNAs components size

Component	Size
C_{IN}, C_{OUT}	300 fF
C_B	1 pF
$M_{1,LN}$, $M_{2,LN}$	$18 \times 2.3\,\mu m$
$M_{1,HG}$, $M_{2,HG}$	$12 \times 3\,\mu m$
R_G	5.3 kΩ
R_B	1 kΩ
$L_{G,LN}$	130 µm
$L_{D,LN}$	220 µm
$L_{U,LN}$	80 µm
$L_{G,HG}$	120 µm
$L_{D,HG}$	260 µm
$L_{U,HG}$	70 µm
$L_{B,HG}$	40 µm

The noise figure has been measured utilizing the Y-factor method [55]. All the measurements have been carried out at the room temperature and under a supply voltage V_{DD} of 1.2 V. Figure 3.7 and Figure 3.8 present the simulated and measured performance of the low noise stage, while Figure 3.9 and Figure 3.10 refer to the high gain stage.

Despite a slight frequency shift, which can be mainly due to the limited accuracy of the transistors high frequency model, good performance have been achieved. All over the bandwidth, input and output return losses are more then 10 dB and both the stages present quite flat small-signal gain and noise figure. Among them, the high gain stage has a little lower 1 dB bandwidth due to the gain peaking effect given by the inductor L_B. The measured performance are summarized in Table 3.3.

After designing the single stages, they have been cascaded to achieve more gain

Table 3.3: Cascode LNAs performance

	Low noise stage	**High gain stage**
Centre frequency	62 GHz	62 GHz
Small signal gain	5.6 dB	7.1 dB
Noise figure	7.5 dB	8.5 dB
IP1dB	-11 dBm	-13 dB
1 dB bandwidth	8 GHz	6 GHz
Input-output isolation	>22 dB	>22 dB
Power consumption	7 mW	7 mW
Chip size	0.35 mm^2	0.35 mm^2

in a three stage cascode LNA. In particular, a low noise stage has been used as input stage, while two high gain stages have been used as second and third stage. In this way, the noise figure is maintained low by the first stage, and the gain enhanced by the subsequent ones.

The so built amplifier has been then simulated, laid out and manufactured. Figure 3.11 shows its chip micrograph. In Figure 3.11 can be noticed how some SCTLs

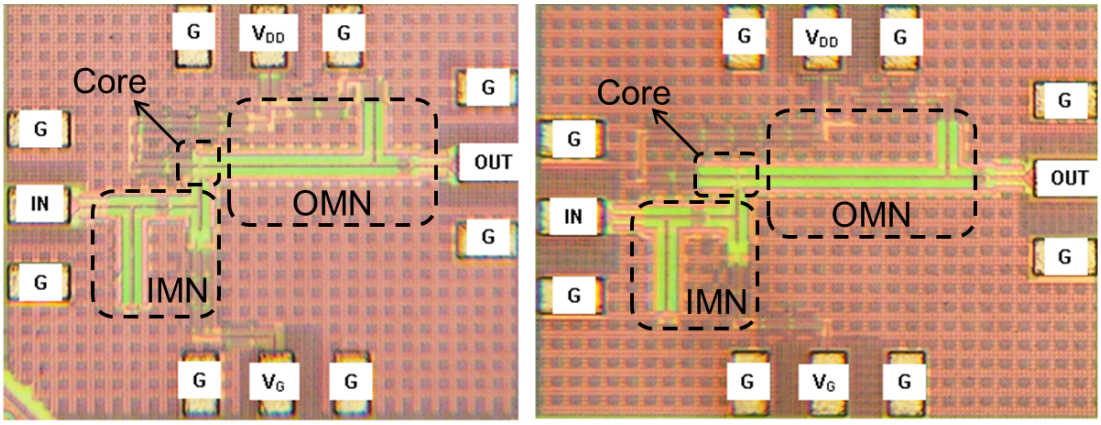
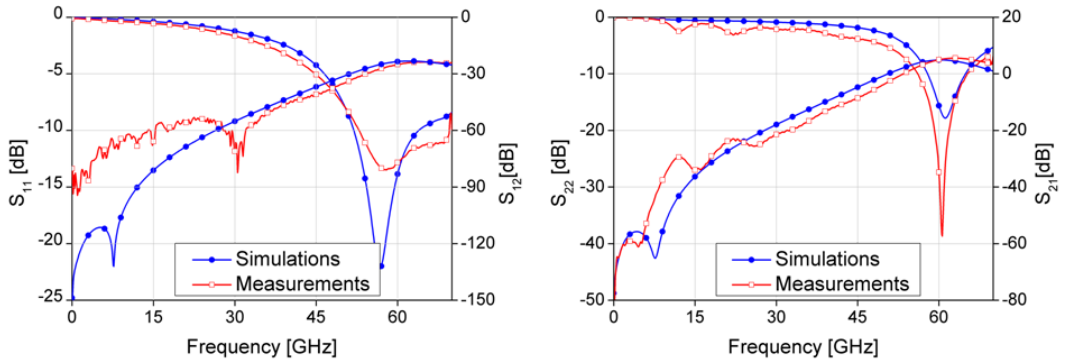
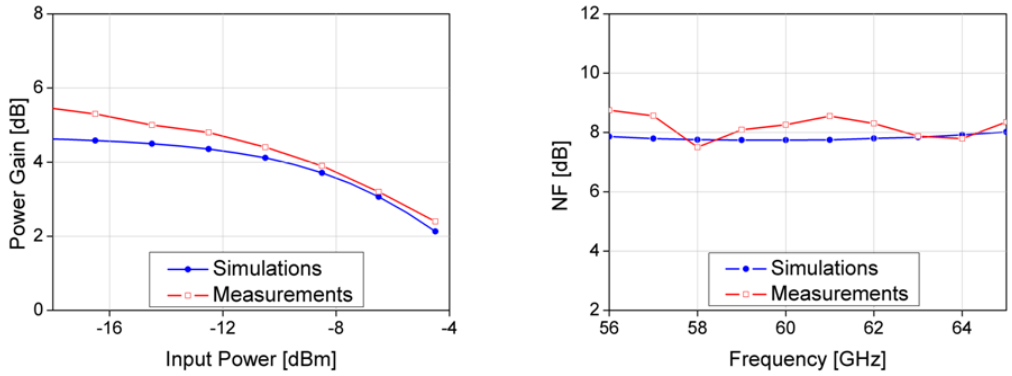


Figure 3.6: Micrograph of the (a) low noise and (b) high gain cascode LNAs. The chip size is in both cases 0.35 mm^2.



(a) (b)

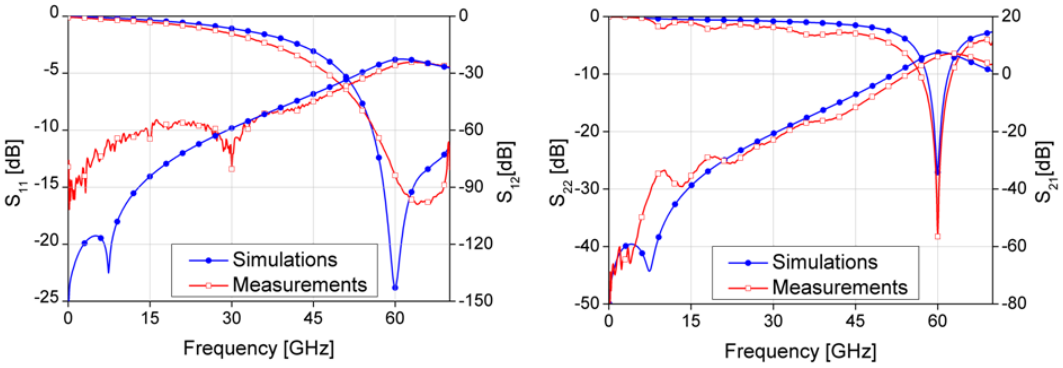
Figure 3.7: Low noise stage, simulations vs. measurements: (a) S_{11} and S_{12}, (b) S_{22} and S_{21}. The supply voltage is V_{DD} = 1.2 V and the drain current I_D = 5.5 mA.



(a) (b)

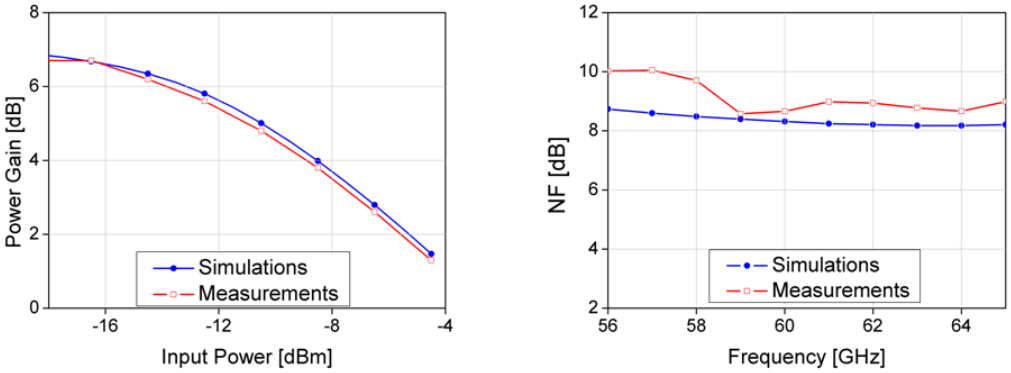
Figure 3.8: Low noise stage, simulations vs. measurements: (a) large signal power gain at 60 GHz and (b) noise figure. The supply voltage is V_{DD} = 1.2 V and the drain current I_D = 5.5 mA.

have been bended for area saving. Small signal, large signal and noise measurements have then been performed on wafer. In Figure 3.12 and Figure 3.13 its performance in terms of scattering parameters, large signal gain and noise figure are reported, and they are finally summarized in Table 3.4. The frequency shift already reported for the single stage amplifiers is now heavier, due to the presence of multiple stages giving each some shift. Being the gain peak frequency 66 GHz, the upper limit of the 1 dB bandwidth, starting at 64 GHz, can not be defined since the measurements have been performed up to 67 GHz. As expected, more than 20 dB gain have been achieved along



(a) (b)

Figure 3.9: High gain stage, simulations vs. measurements: (a) S_{11} and S_{12}, (b) S_{22} and S_{21}. The supply voltage is V_{DD} = 1.2 V and the drain current I_D = 5.7 mA.



(a) (b)

Figure 3.10: High gain stage, simulations vs. measurements: (a) large signal power gain at 60 GHz and (b) noise figure. The supply voltage is V_{DD} = 1.2 V and the drain current I_D = 5.7 mA.

with an average noise figure of 9 dB. Due to the poor output swing offered by the cascode topology, the 1 dB compression point does not satisfy the system requirements. However, the main problem is the noise figure. It is clear that the required noise figure of 6.6 dB can not be easily reached by using cascode amplifiers. The literature does not give any better hope, as the published cascode amplifiers present also high noise figures [56, 57]. A topology which guarantees higher output swing and, above all, lower noise figure is therefore needed.

Table 3.4: Three stages cascode LNA performance

Centre frequency	66 GHz
Small signal gain	20.6 dB
Noise figure	9 dB
IP1dB	-29 dBm
1 dB bandwidth	>3 GHz
Input-output isolation	>50 dB
Power consumption	21 mW
Chip size	0.78 mm^2

3.3 LNA topologies noise analysis

The common source topology is a good candidate for obtaining the desired noise figure reduction. In fact, the finite impedance to ground in the node between the two

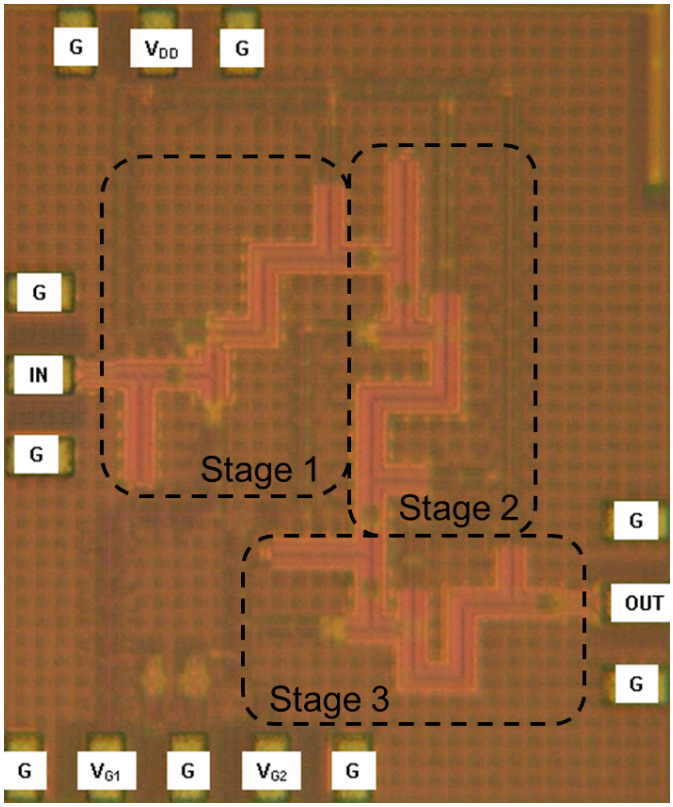
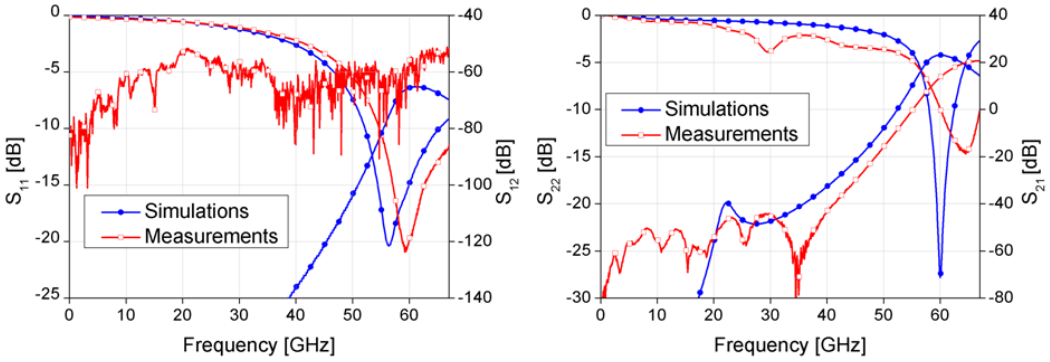
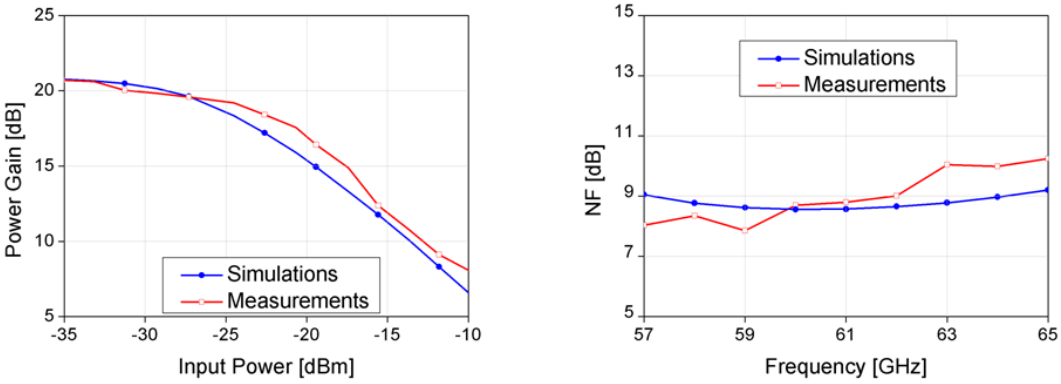


Figure 3.11: Three stages cascode LNA micrograph. The chip size is 0.78 mm^2.



(a) (b)

Figure 3.12: Three stages cascode LNA, simulations vs. measurements: (a) S_{11} and S_{12}, (b) S_{22} and S_{21}. The supply voltage is V_{DD} = 1.2 V, while the drain current is I_{D1} = 5.5 mA for the first stage and $I_{D2,3}$ = 5.7 mA for the subsequent ones.



(a) (b)

Figure 3.13: Three stages cascode LNA, simulations vs. measurements: (a) large signal power gain at 60 GHz and (b) noise figure. The supply voltage is V_{DD} = 1.2 V, while the drain current is I_{D1} = 5.5 mA for the first stage and $I_{D2,3}$ = 5.7 mA for the subsequent ones.

transistors of a cascode stage introduces a mismatching, which becomes perceptible at high frequencies, making its noise figure worse than the one of a simple common source stage [58]. In this section, an analytical study of the noise in the two different topologies is reported [59].

Considering a common source topology, the noise factor can be obtained as in [60], reporting the noise sources in input. The input referred noise model is depicted in Figure 3.14. The value of the input noise sources is reported in (3.3), where α, defined

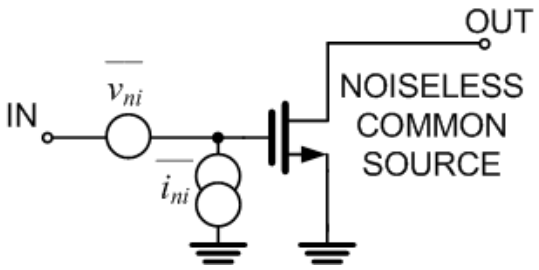


Figure 3.14: Common source input referred noise sources.

as in (3.4), is unity in long channel devices.

$$\begin{aligned} \overline{v_{ni}^2} &= 4kT\gamma\frac{1}{\alpha g_m}\Delta f \\ \overline{i_{ni}^2} &= 4kT|Y_{gs}|^2\left(\delta\frac{1}{5g_{d0}}+\gamma\frac{1}{\alpha g_m}\right)\Delta f \end{aligned} \tag{3.3}$$

$$\alpha = \frac{g_m}{g_{d0}} \tag{3.4}$$

After building the input referred noise model, calculating the noise factor is straightforward. A well known expression, shown in (3.5), is based on the noise parameters R_n, G_c, B_c and G_u, reported in (3.6), where G_s and B_s are respectively conductance and susceptance of the input source.

$$F = 1+\frac{G_u+[(G_c+G_s)^2+(B_c+B_s)^2]R_n}{G_s} \tag{3.5}$$

$$\begin{aligned} G_c &\simeq 0 \\ G_u &= \delta\frac{|Y_{gs}|^2}{5g_{d0}}(1-|c|^2) \\ R_n &= \frac{\gamma}{\alpha g_m} \\ B_c &= |Y_{gs}|\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \end{aligned} \tag{3.6}$$

The same quantities can be calculated for a cascode amplifier, which is made by cascading a common source stage and a common gate stage. Since the noise factor of the common source stage has already been calculated, in order to compute the noise

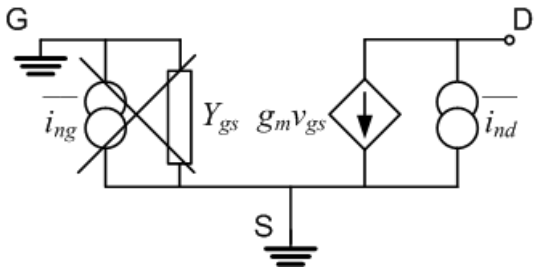


Figure 3.15: Common gate noise sources with shorted input.

factor of the cascode amplifier the noise of the common gate stage has to be studied.

Starting from the MOSFET noise model of Figure 3.1, in order to report the noise contributors in input two steps have to be followed [61]: shorting the input, an equivalent input noise voltage source can be determined; opening it, an equivalent input noise current can be calculated. In the case when the input is shorted, the model becomes as shown in 3.15. The gate-source voltage becomes zero and the gate current source i_{ng} is cancelled, so that the only contributor is the drain noise current source i_{nd}, leading to the expression of the equivalent input noise voltage source shown in (3.7).

$$\overline{v_{ni}^2} = 4kT\gamma\frac{1}{\alpha g_m}\Delta f \tag{3.7}$$

In the case when the input is opened, visible in Figure 3.16, neglecting for simplicity the gate noise current generator i_{ng}, the common gate stage can be seen as a current buffer with input impedance Y_{gs}. This behaviour can be modelled by a noiseless common gate with an input impedance equal to Y_{gs}. Bringing together the results, the equivalent noise model of the common gate amplifier depicted in Figure 3.17 is

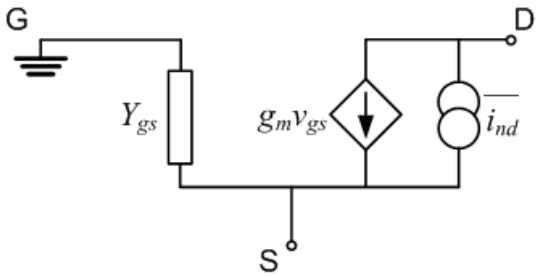


Figure 3.16: Common gate noise sources with open input.

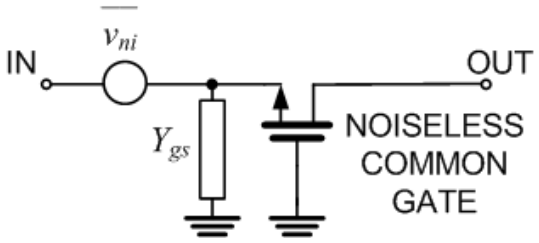


Figure 3.17: Common gate input referred noise sources.

obtained.

Once the input referred noise sources of the common gate amplifier are defined, the input referred noise sources of a cascode stage can be obtained simply cascading one common source and one common gate and referring all the noise sources at the input of the cascaded stages. For simplicity, the two transistors are considered to be the same. For clearness, the equivalent impedance at the node between common source and common gate is now called Y_x, which includes all the impedances at that point. After cascading the two stages as in Figure 3.18, the noise voltage source v_{nicg} can be reported in input dividing it by the common source power gain, leading to the model in 3.19 where the two input referred noise sources have the expressions given in (3.8).

$$\begin{aligned}\overline{v_{niC}^2} &= 4kT\gamma\frac{1}{\alpha g_m}\left(1+\frac{|Y_x|^2}{g_m^2}\right)\Delta f \\ \overline{i_{niC}^2} &= 4kT|Y_{gs}|^2\left(\delta\frac{1}{5g_{d0}}+\gamma\frac{1}{\alpha g_m}\right)\Delta f\end{aligned} \tag{3.8}$$

From the input referred noise model of a cascode stage, its noise parameters and

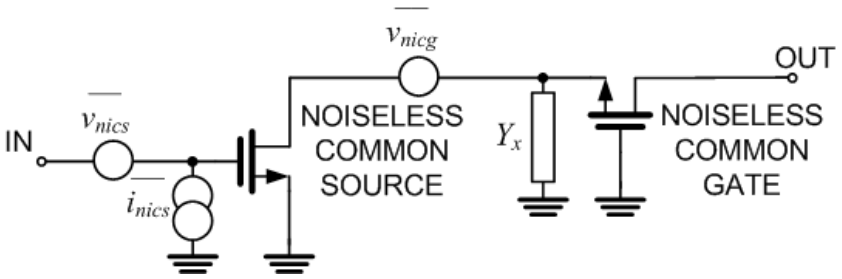


Figure 3.18: Cascaded stages in a cascode topology.

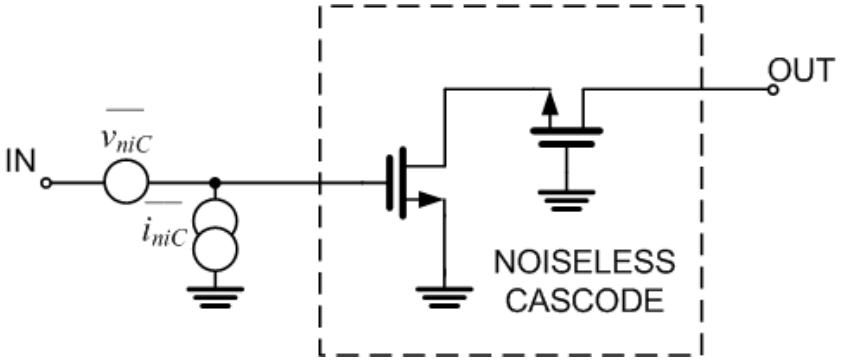


Figure 3.19: Cascode input referred noise sources.

hence its noise factor can be obtained. The term added by the common gate stage is completely uncorrelated, since it comes solely from the drain noise current of this stage. This means that the noise parameters of the cascode will be the same as the ones calculated for the common source and reported in (3.6), except an additional one which depends on the common-gate dependent part of the input noise voltage source, absent in the common source case. This term can be extracted as in (3.9), where v_{nicg} is the term coming from the common gate transistor.

$$\overline{v_{niuC}^2} = \overline{v_{nicg}^2} = 4kT\gamma\frac{1}{\alpha g_m}\frac{|Y_x|^2}{g_m^2}\Delta f \tag{3.9}$$

A new noise parameter R_u taking into account this term can be defined as in (3.10).

$$R_u = \frac{\overline{v_{niuC}^2}}{4kT\Delta f} \tag{3.10}$$

Substituting the value of v_{nicg} in (3.9) and bringing this result in (3.10), the expression of R_u reported in (3.11) is obtained.

$$R_u = \gamma\frac{|Y_x|^2}{\alpha g_m^3} \tag{3.11}$$

The noise factor of the cascode topology can be then easily calculated as in (3.12).

$$F = 1 + \frac{G_u + [(G_c+G_s)^2 + (B_c+B_s)^2]R_n + (G_s^2+B_s^2)R_u}{G_s} \tag{3.12}$$

Minimizing (3.12) with respect to G_s and B_s, an optimum value of the source impedance $Y_s = G_s + jB_s$ which minimizes the noise factor can be found, and it is shown in (3.13).

$$\begin{aligned} G_{s,opt} &= \sqrt{\frac{(G_u + R_n G_c^2)(R_n + R_u) + R_n R_u B_c^2}{(R_n + R_u)^2}} \\ B_{s,opt} &= -\frac{B_c R_n}{R_n + R_u} \end{aligned} \tag{3.13}$$

From (3.5) and (3.12) can be noticed that the only difference between the noise factor of the common source stage and the cascode stage is the term including the newly defined noise parameter R_u. Their comparison leads to the relation in (3.14), where F_{CAS} and F_{CS} are the noise factors of the cascode and the common source respectively.

$$F_{CAS} = F_{CS} + \frac{(G_s^2 + B_s^2)R_u}{G_s} \tag{3.14}$$

Since the term depending on R_u in (3.14) is an always positive function, it is demonstrated how a cascode stage has always a higher noise factor than a common source stage, and consequently a higher noise figure.

It has been seen how the term R_u represents the additional noise introduced by the common gate stage. Its expression (3.11) shows its dependency on the technological parameters. As expected, a higher transconductance g_m and a smaller middle node admittance Y_x will contribute to make the cascode noise performance closer to the common source ones. A quantitative analysis is not easy due to the already discussed lack of exact estimation in short channel regime of the noise coefficients. An estimation of R_u can be anyway done considering reasonable values of all the parameters [59], and it is presented at the end of the next paragraph.

3.4 Two stages LNA

The main result obtained in the last section says that a common source amplifier can be used instead of a cascode amplifier in order to obtain better noise performance. Following these results, a common source topology is taken into consideration for further reducing the LNA noise figure. In order to do that, the low noise cascode stage described in the last section has been used as second stage of a two stages amplifier,

preceded by a common source stage. The schematic of the two stages LNA so obtained is depicted in Figure 3.20.

Additional solutions are also used. In order to avoid the use of decoupling MIM capacitors, which are very sensitive to process tolerances and pretty lossy, the output of the first stage has been biased together with the gate voltage of the second stage V_G. This reduces the available voltage swing at the output of the first stage, but does not affect much the small signal performance, despite a small reduction of the small signal gain due to the channel length modulation. The inter-matching between the two stages consists only of L_M, which performs a conjugate matching at the first stage output and a noise matching at the second stage input. The transistor size is chosen considering Figure 3.21 and Figure 3.22, which show the simulation results of a common source transistor stand-alone. The size of active and passive components finally selected for the present design are reported in Table 3.5, while its chip micrograph is presented in Figure 3.23.

Once again, the chosen size allows to have an acceptable gain and a good noise figure along with a reliable layout. The used SCTLs look like the ones used for the previous designs. As mentioned, MIM capacitors are only used for decoupling DC-wise input and output and as RF grounds, but not within matching networks. The input is matched for minimum noise, that is at the optimum noise input impedance. The layout shows how the SCTLs within the cascode stage are now bended for reducing

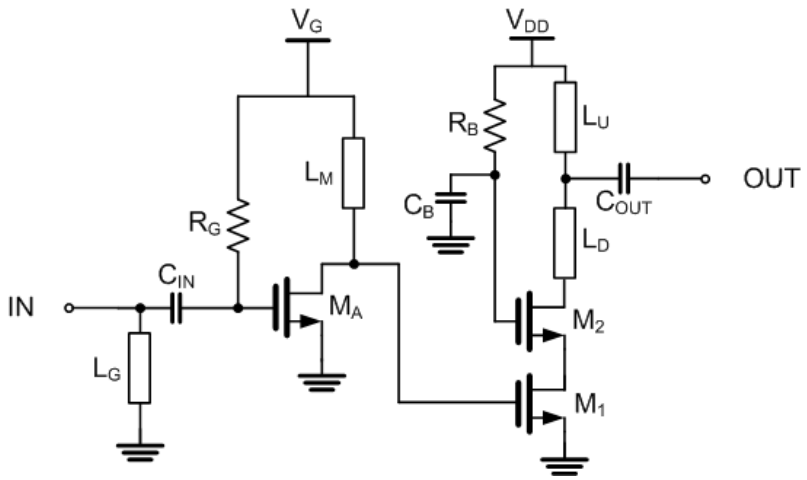


Figure 3.20: Schematic of the two stages LNA.

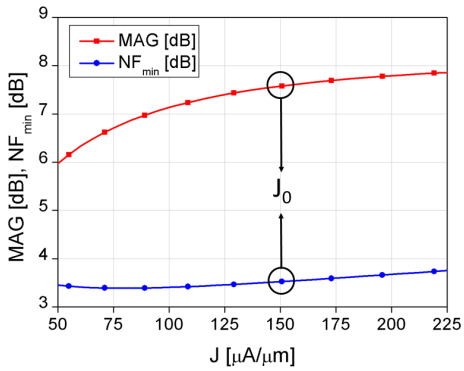


Figure 3.21: Common source sizing: choice of the bias current density.

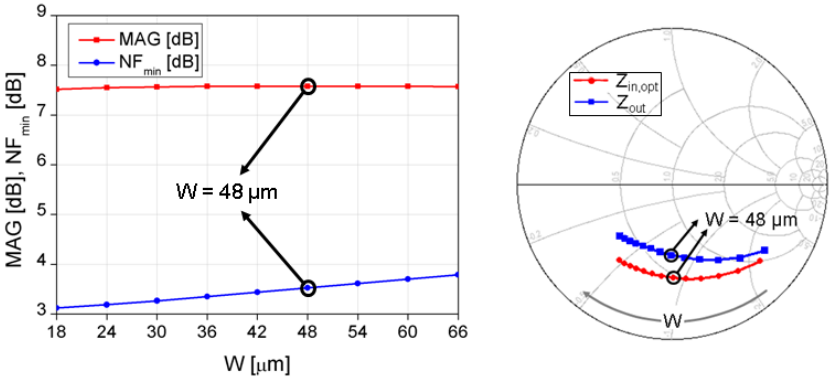


Figure 3.22: Common source sizing: choice of the transistor size (fixing the current density to J = 150 µA/µm).

the area occupation. In fact, while the single low noise stage presented in the last section occupies 0.35 mm^2, the two stages amplifier sits in only 0.36 mm^2.

The small signal measurement results are shown in Figure 3.24, while large signal and noise performance are presented in Figure 3.25. In both cases, measurements and simulations are compared, showing each other a good agreement.

The LNA performance are summarized in Table 3.6. It can be seen how, by using a common source stage at the input, the overall noise figure is reduced as predicted by the simple calculations of the last section. This improvement consists of around 0.5 dB in average. Obviously, the gain and the input-output isolation are improved by the use of two stages instead of one, even if the power consumption is not much higher thanks to the low bias voltage at the intermediate point. The 1 dB bandwidth starts at 59 GHz,

Table 3.5: Two stages LNA components size

Component	Size
C_{IN}, C_{OUT}	300 fF
C_B	1 pF
M_1, M_2	$18 \times 2.3\,\mu m$
M_A	$16 \times 3\,\mu m$
R_G	5.3 kΩ
R_B	1 kΩ
L_G	140 µm
L_M	110 µm
L_D	220 µm
L_U	80 µm

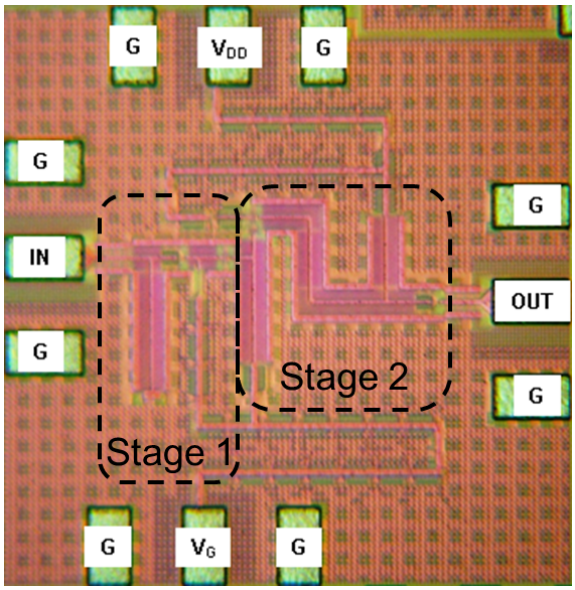
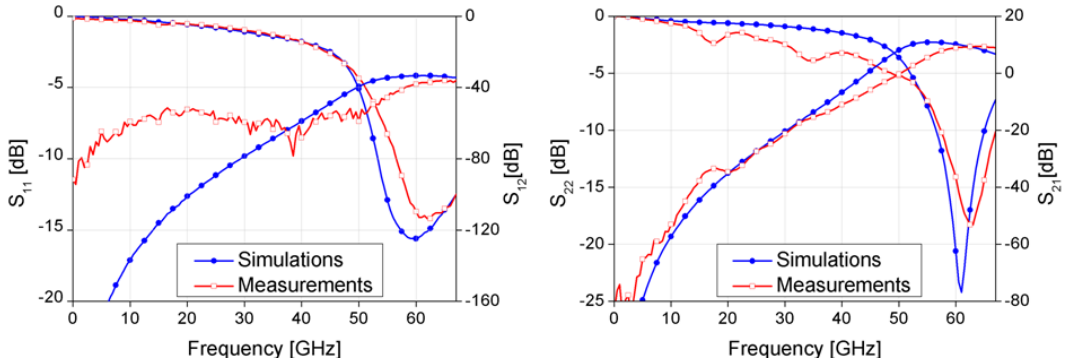
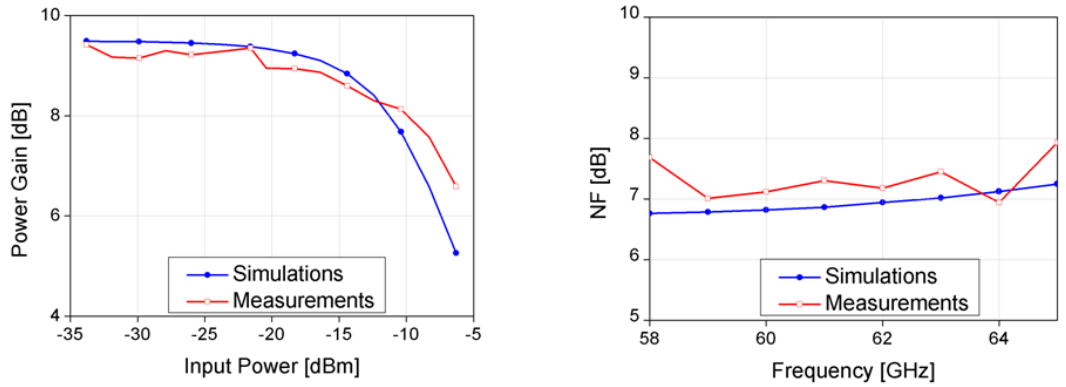


Figure 3.23: Two stages LNA micrograph. The chip size is 0.36 mm^2.



(a) (b)

Figure 3.24: Two stages LNA, simulations vs. measurements: (a) S_{11} and S_{12}, (b) S_{22} and S_{21}. The common source stage has a supply voltage of $V_G = 0.7\,V$ and a drain current $I_{D1} = 7\,mA$, while the cascode stage has a supply voltage of $V_{DD} = 1.2\,V$ and a drain current $I_{D2} = 5.5\,mA$.



(a) (b)

Figure 3.25: Two stages LNA, simulations vs. measurements: (a) large signal power gain at 60 GHz and (b) noise figure. The common source stage has a supply voltage of $V_G = 0.7\,V$ and a drain current $I_{D1} = 7\,mA$, while the cascode stage has a supply voltage of $V_{DD} = 1.2\,V$ and a drain current $I_{D2} = 5.5\,mA$.

but its upper limit is above 67 GHz which is the highest measured frequency. The input P1dB lies at -13 dBm, as can be expected considering the measured IP1dB of the low noise cascode stage and adding some gain given by the common source stage.

The noise calculations showed in the last paragraph have been applied to the design just presented, the two stages LNA, and to the low noise cascode LNA previously

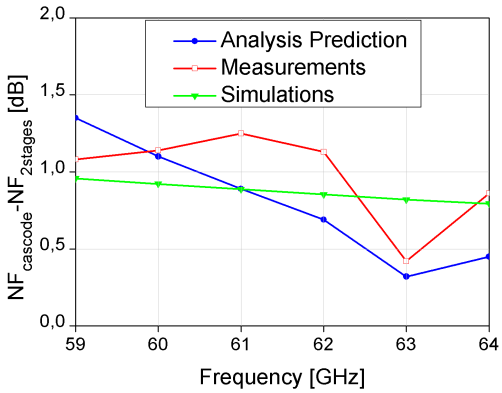


Figure 3.26: Difference between the NF of the two LNAs: calculation, simulation and measurements.

discussed. In particular, the noise parameter R_u has been calculated as in 3.11 and its impact on the noise figure of the cascode stage has been derived as in 3.12. The values of g_m, g_{d0} and the impedances at the various points have been calculated through simulation, while the value of γ has been set at 1.7. Extracting the pads where needed, the noise figure of the cascode stage and the two stages LNA have been derived, and their difference compared at different frequencies with the simulated and the measured ones. The difference between the noise figures of the two LNAs is reported in Fig. 3.26, where in blue are presented the calculated values, in green the simulations and in red the measured results.

It can be seen how the presented calculations lead to a quite exact prediction, validating the presented analysis. The difference between the two curves has to be most probably referred both to the gate induced noise current of the common gate stage, neglected for simplicity during the computations, and to the not exact value of the noise parameter γ.

The picture is now clearer. In order to satisfy the system requirements, a common source topology has to be used due to the need for low noise figure. Furthermore, it has been seen how a single common source stage can give between 4 dB and 5 dB gain, meaning that for obtaining the targeted 15 dB gain four stages have to be used. The last observation is that the targeted WiONet system is fully differential, so that the LNA to be designed should be differential as well. All these considerations are the base for the

Table 3.6: Two stages LNA performance

Centre frequency	64 GHz
Small signal gain	9.4 dB
Noise figure	7 dB
IP1dB	-13 dBm
1 dB bandwidth	>8 GHz
Input-output isolation	>36 dB
Power consumption	11 mW
Chip size	0.36 mm^2

following design steps.

3.5 Fully differential LNA

The conclusions drawn at the end of the previous section led to the design of a fully differential four stages common source amplifier [62], whose schematic view is reported in Figure 3.27.

Beyond the pros given by the virtual ground as discussed in Chapter 1, a noteworthy advantage of differential structures with respect to single ended ones is the common mode rejection, having differential circuits the possibility to partially reject the common mode signal at their inputs. The common mode rejection is here performed by the SCTLs L_{M1}, L_{M2}, L_{M3} and L_{M4}, designed having low DC losses in order to avoid any voltage drop on them.

Regarding the transistor sizing, Figure 3.22 shows how a common source transistor smaller than the one previously used can guarantee a lower noise figure, maintaining an acceptable power gain. This is the main reason why, in order to further push down the amplifier noise figure, a transistor with a total width of 36 μm has been chosen as core of all the four stages. The bias point has been kept at the optimum current density discussed in the previous sections. Anyway, a common source amplifier is, unlike a cascode one, not always unconditionally stable. The Rollett stability factor [63] is a widely used dimensionless small signal parameter giving indications on amplifiers

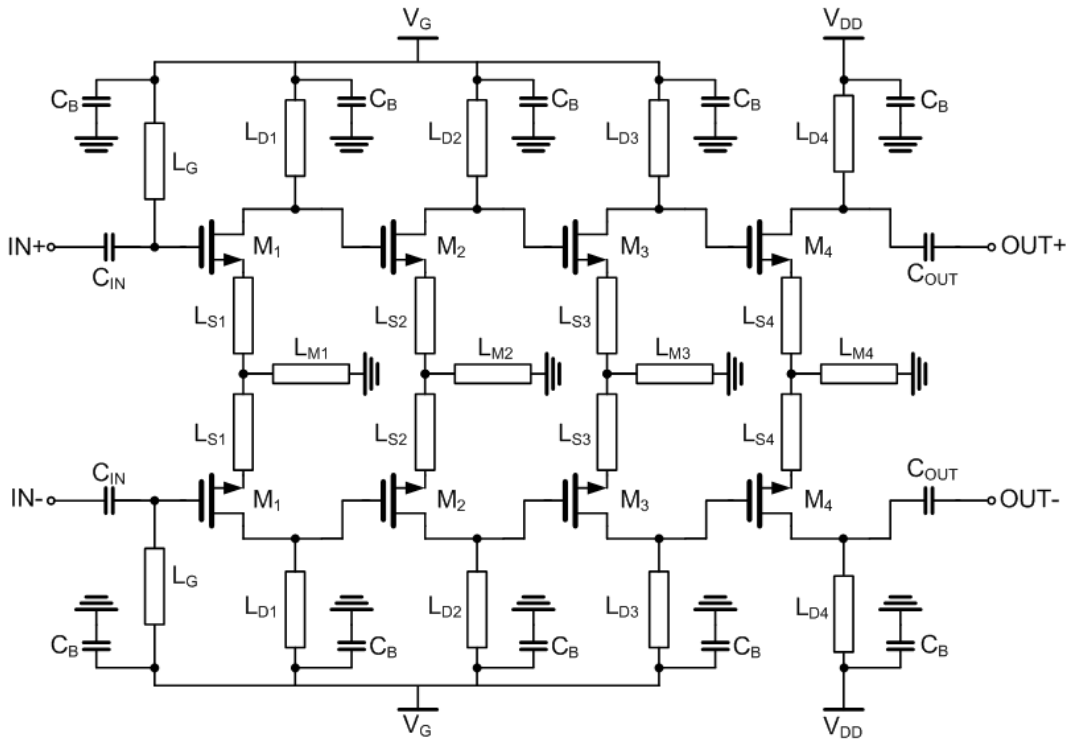


Figure 3.27: Schematic of the fully differential LNA.

stability. It has been seen how this stability factor becomes smaller as the total channel width goes down [64]. In other words, if the usage of a smaller and less noisy transistor is wished, the amplifier can become unstable. Having the CMOS devices intrinsically low gain, low frequency stability is not a major issue in designs like the ones here presented. Unstabilities can arise at the operating frequency, especially in multistage designs, where the amplified signal can couple back to the previous stages making the whole circuit oscillating. In order to keep a reasonable stability margin, in the present design a degeneration source inductance has been used in every stage. The value of the degeneration inductor has been chosen looking at the simulation results here presented in Figure 3.28 and making a trade-off between stability and gain. Since the single stage gain is very low, only small degeneration inductors can be used, which cause negligible variations of noise figure and input impedance, in the order of few tenth of decibel. The selected inductor should offer about 17 pH, which corresponds to a SCTL 30 μm long.

Matching networks are built using once again SCTLs. The input noise matching

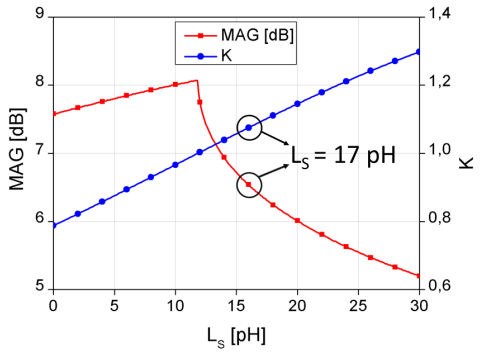


Figure 3.28: Fully differential LNA: degeneration inductance effect at 60 GHz.

is performed by L_G, while the SCTLs L_{D1}, L_{D2}, L_{D3} and L_{D4} are employed to match the stages each other and the output to 50 Ω. A good RF ground is obtained connecting big capacitors C_B to ground after the matching inductors. The input and output capacitors C_{IN} and C_{OUT} are used to decouple DC-wise the circuit for measurement purposes. The drains of the three first stages are biased together with the gates of the subsequent stages at V_G in order to reduce the power consumption and simplify the DC distribution, while the drain bias of the last stage is kept at V_{DD} to enhance the output swing and consequently the P1dB. The size of the employed components are summarized in Table 3.7, while the chip micrograph of the amplifier is shown in Figure 3.29. The optimization of the layout allowed to achieve a chip size of only 0.38 mm^2 pads included.

Large signal, small signal, and noise measurements have been performed on wafer. The scattering parameters have been directly measured with a fully differential vector network analyser. Large signal and noise measurements must be performed using probes with integrated balun to create a differential signal from a single generator in input and to combine the outputs. The noise figure has been then extracted following the extraction technique suggested in [65].

Figure 3.30 presents the comparisons between simulated and measured small signal power gain and noise figure. The slight frequency shift between simulated and measured differential S_{21}, already encountered in the previous designs, can be mainly due to the limited model accuracy. The measured small signal differential gain is almost flat in the band of interest, and achieves a peak gain of 21.3 dB at a central frequency

Table 3.7: Fully differential LNA components size

Component	Size
C_{IN}, C_{OUT}	300 fF
C_B	1 pF
M_1, M_2, M_3, M_4	$12 \times 3\,\mu m$
L_G	180 µm
L_{S1}, L_{S2}, L_{S3}, L_{S4}	30 µm
L_{M1}, L_{M4}	130 µm
L_{M2}, L_{M3}	50 µm
L_{D1}, L_{D2}	110 µm
L_{D3}	120 µm
L_{D4}	210 µm

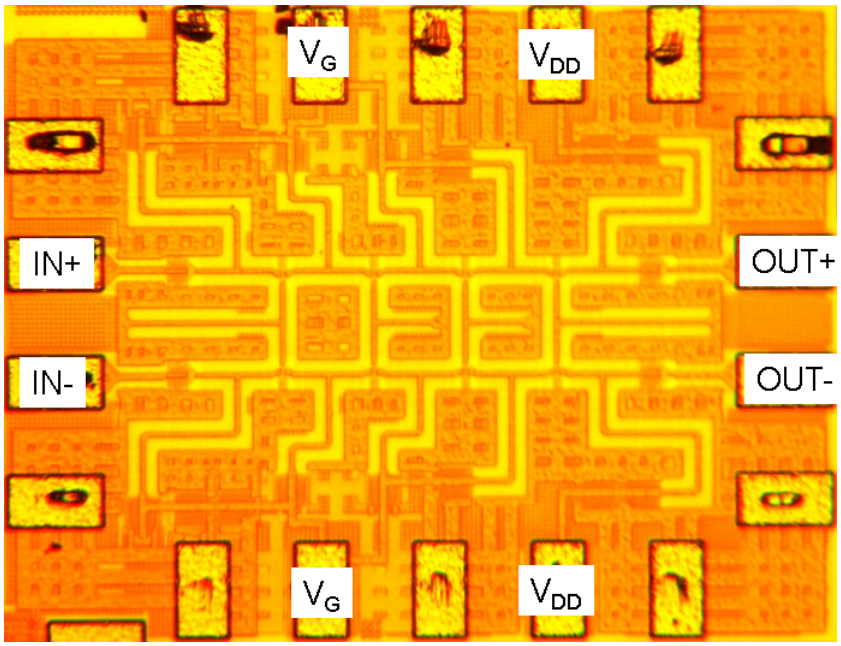


Figure 3.29: Fully differential LNA micrograph. The chip size is 0.38 mm^2.

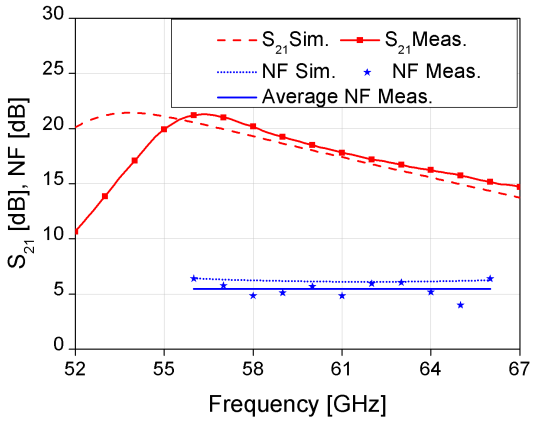


Figure 3.30: Fully differential LNA, simulations vs. measurements: small signal power gain and noise figure. The supply voltage is $V_G = 0.7\,V$ for the first three stages and $V_{DD} = 1.2\,V$ for the last one, while the drain current is for all the stages $I_D = 4.7\,mA$.

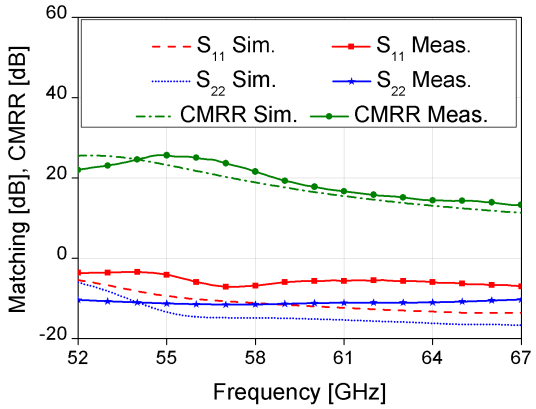


Figure 3.31: Fully differential LNA, simulations vs. measurements: input return loss, output return loss and CMRR. The supply voltage is $V_G = 0.7\,V$ for the first three stages and $V_{DD} = 1.2\,V$ for the last one, while the drain current is for all the stages $I_D = 4.7\,mA$.

of 57 GHz and a 3 dB bandwidth between 54.4 GHz and 60.4 GHz. The measured differential noise figure takes values around an average value of 5.4 dB between 56 GHz and 66 GHz. Figure 3.31 shows the matching performance, in terms of S_{11} and S_{22}, and the common mode rejection ratio (CMRR) of the circuit, defined as the ratio between differential and common mode gain. Wideband matching is achieved along with a CMRR higher than 17 dB within the 3 dB bandwidth of the amplifier. Large signal

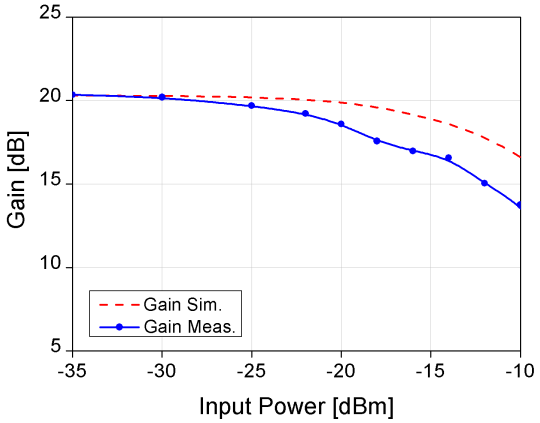


Figure 3.32: Fully differential LNA, simulations vs. measurements: large signal power gain at 57 GHz. The supply voltage is V_G = 0.7 V for the first three stages and V_{DD} = 1.2 V for the last one, while the drain current is for all the stages I_D = 4.7 mA.

measurements are performed to obtain the 1 dB gain compression point (P1dB). Figure 3.32 presents these measurement results at 57 GHz, performed keeping the same bias condition as the small signal measurement. From this plot it can be seen that the compression comes slightly earlier in measurements, due probably to some output bias issue during the measurement process. The input P1dB occurs when -22 dBm are given to the input of the amplifier, which means an output P1dB of -1.7 dBm. The total power consumption is 30 mW, since 28 mA from 700 mV and 10 mA from 1.2 V are drawn. Table 3.8 shows the comparison between the measured performance of the presented design and the other recently published 60 GHz 90 nm CMOS LNAs [66–71].

A very well known LNA figure of merit [72], here reported in (3.15), is calculated for all the considered amplifiers and shown in Table 3.8. It has to be noticed that in this calculation a factor n is added for a fairer comparison, taking into account that differential topologies have double power consumption. In fact, n is equal to 1 for single-ended circuits and to 2 for differential ones. In (3.15) G, F, and P_{DC} stand for linear gain, noise factor, and power consumption, respectively.

$$FOM = \frac{G}{(F-1)(P_{DC}/n)} \tag{3.15}$$

Table 3.8 shows how this design is in line with the state of the art in LNA design.

Table 3.8: Comparison between this work and published 90 nm CMOS LNAs

Reference	[66]	[67]	[68]	[69]	[70]	[71]	**This work**
Topology	CS	CS	CS	diff. Cas.	CS	CS	**diff. CS**
No. Stages	3	3	3	3	3	3	**4**
f_0 [GHz]	58	57	59.5	63	60	57.3	**57**
Gain [dB]	15	18.6	10.9	16.2	23	12.5	**21.3**
*NF** [dB]	5	6.5	6	7.8†	5	6	**5.4**
IP1dB [dBm]	-18	-15	-17	N.A.	-19.5	-16	**-22**
BW_{3dB} [GHz]	56–61	54–63	58–63	59–66	57–65	55–61	**54.4–60.4**
Supply [V]	1.3	1.2	1	1.2	1.3	1	**1.2**
P_{DC} [mW]	4	29	5.5	45	16	44	**30**
CMRR [dB]	–	–	–	>10	–	–	**>17**
Area [mm^2]	0.14	0.70	0.39	N.A.	0.06‡	0.36	**0.38**
FOM [mW^{-1}]	3.66	0.72	0.75	0.37	5.77	1.36	**3.64**

* Average values over the measured frequency points
† Extrapolation from receiver measurements
‡ Without pads

The designed LNA satisfies the system requirements. The desired gain, noise figure and input maximum power given in Table 1.4 are reached, and even enhanced, within the whole RF frequency range, as visible in Figure 3.30 and Figure 3.32. Anyway, the designed LNA can be included into the WiONet system only if the subsequent down converter do not significantly worsen the signal quality. This is the goal pointed within the next chapter.

Chapter 4

Down Converter Design

The second circuit block that is addressed in this thesis is the 60 GHz to 20 GHz down converter. Its function is to convert the signal amplified in a low noise fashion by the LNA down to the intermediate frequency f_{IF}. The conversion process should be performed without deteriorating the signal quality, that means preserving an acceptable signal to noise ratio and introducing as less nonlinearities as possible.

In a receiver, the noise introduced by the circuits following the LNA has less influence on the overall signal to noise ratio, as stated by the previously mentioned Friis noise formula [31]. Anyway, the noise introduced by the down converter can become relevant when the LNA gain is relatively low or the noise figure of the mixer assumes large values. These conditions are the ones faced in very high frequency CMOS designs, where only low gain and noisy devices are available. Such considerations make clear how the design of high frequency CMOS down converters having sufficient gain and noise performance is still a very tough job.

In the next sections, after a brief introduction on mixers fundamentals and on the peculiarities of CMOS mixers, the research process which led to the design of the down converter chosen for being part of the WiONet system will be presented.

4.1 Mixers fundamentals

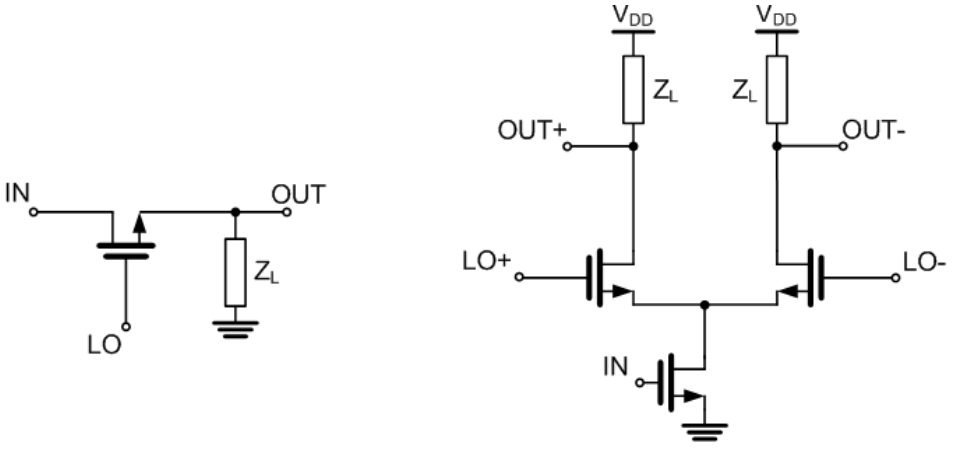
The frequency translation operation of a mixer is based on the multiplication of two signals at its inputs, giving as output a signal at a frequency which is a combination of the two input frequencies [73]. In a down conversion mixer, the input signals are the

RF signal at f_{RF}, coming from the LNA and carrying the information, and the local oscillator signal at f_{LO}, which acts as reference frequency. The output signal is at the frequency f_{IF}, defined as in (4.1).

$$f_{IF} = f_{RF} - f_{LO} \tag{4.1}$$

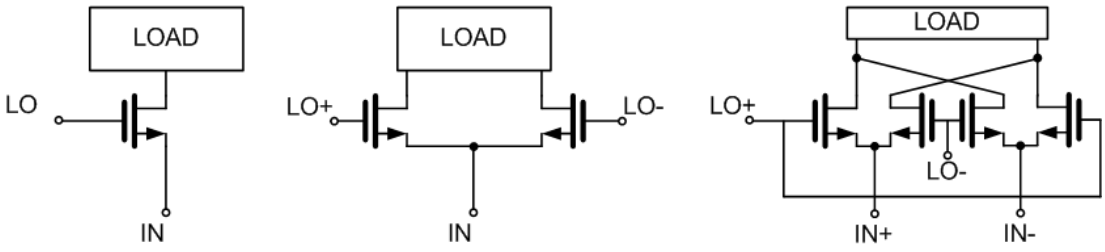
Circuits implementing a frequency translation have to be nonlinear. In fact, mixers are mainly made by switching transistors which get in input the RF signal and whose transitions between ON and OFF states are regulated by the LO signal. If a mixer uses an amplifying device to increase the strength of the product signal, then it is called "active", otherwise it is called "passive". A passive mixer has usually high linearity and speed, but shows always negative conversion gain [74]. On the other hand, an active mixer can achieve large gain values, reducing in a receiver the noise contributions of the subsequent stages [75]. In Figure 4.1, a simple passive mixer (a) and an active mixer (b) are depicted.

Mixers are also classified considering the way they accommodate their inputs. A balanced mixer gets the LO signal differentially. It can be double balanced, when the input port is also differential, or single balanced, when it accommodates single-ended input signals. Figure 4.2 explains more clearly the just presented concept. With respect to a single balanced topology, a double balanced one shows a higher LO rejection, since



(a) (b)

Figure 4.1: Examples of (a) passive and (b) active mixers.



(a) (b) (c)

Figure 4.2: Examples of (a) unbalanced, (b) single balanced and (c) double balanced mixers.

it performs a LO signal cancellation at the output nodes [50].

The definition of the performance of a mixer is not always straightforward and it is often source of confusion. In the case of high frequency mixers it is convenient to define the conversion gain in terms of power, that is output power delivered to the load divided by the input power available at the source, since they are always measured in a $50\,\Omega$ environment.

The mixer noise behaviour is usually quantified using two different noise figure definitions. Defining the image frequency f_{IM} as in (4.2), namely as that frequency at a distance f_{IF} from f_{LO}, it can be easily demonstrated how in a frequency conversion all the components present at around the image frequency will be translated into the IF frequency together with the RF signal.

$$f_{IM} = f_{LO} - f_{IF} \tag{4.2}$$

When the image frequency lies outside the RF band, then f_{IM} contains only noise, and the single sideband noise figure NF_{SSB} is defined. When the image frequency is inside the RF bandwidth, then f_{IM} contains not only noise, but also part of the modulated signal: in this case the noise figure to be considered is the double sideband noise figure NF_{DSB} [76]. From the above definitions, if the mixer gain at the image frequency is equal to the mixer gain at the signal frequency, then the relation in (4.3) comes automatically.

$$NF_{SSB} = NF_{DSB} + 3\,dB \tag{4.3}$$

4.2 CMOS mixers

The CMOS technology is one of the most used for designing integrated mixers. The biggest difference between CMOS and bipolar mixers is the reaction of the switching transistors to the LO signal in balanced structures [50]. In particular, considering a sinusoidal LO signal, more realistic than a squared LO in high frequency applications, the switching transistors of structures similar to the ones in Figure 4.2 (b) and Figure 4.2 (c) do not switch ideally. There exists a certain time slot where both are conducting, giving to the output the input signal as common mode, whose duration affects the mixer conversion gain. The longer are both switches ON, the lower is the mixer conversion gain and consequently the higher its noise figure is. This issue is typically more noticeable in CMOS mixers. In fact, MOS devices usually need a larger LO drive to switch fully with respect to the bipolar counterpart, being the drain current quadratically dependent from the gate-source voltage (or linearly in short-channel regime), while the collector current depends exponentially from the base-emitter voltage. This means that for a fixed LO swing the switches of a balanced mixer are both ON longer in the case they are MOS transistors than in the one they are bipolar.

Better switching can be achieved using large switching transistors, but this solution increases the parasitic capacitance between their sources, named C_m in Figure 4.3. If C_m increases, the impedance between the node M and ground decreases and a large amount of input signal is dissipated to ground instead of going towards the output. Another remedy is the reduction of the drain current of the switches, but doing so their transconductance is also reduced and the impedance seen looking into their sources,

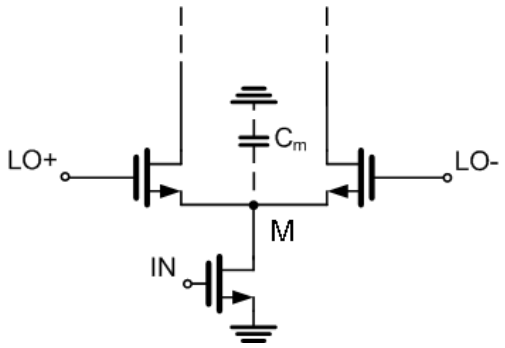


Figure 4.3: Parasitic capacitance between the sources of a balanced mixer.

equal to the inverse of their transconductance, grows. This means that the input signal approaching that node prefers once again to go to the ground through C_m instead of going towards the output through the switches, decreasing the conversion gain. From the previous discussion, it can be seen how lowering the time window where both the switches of a CMOS mixer are ON is not an easy task and it has to face a lot of trade-offs.

The noise analysis of CMOS mixers is not straightforward, being it only possible using numerical computations through simulators. Looking at the problem from a qualitative point of view, and considering an active single balanced mixer, its noise can be divided into two main sources. One is the noise introduced by the input transistor, the other the one given by the switches. The noise given by the input transistor corresponds to the noise injected by a common source stage, which can be divided into drain current noise and gate noise as already seen in Chapter 3.

A more complicated analysis is needed for the study of the noise added by the switching part. For simplicity, let us consider the noise coming from the LO path negligible, reasonable assumption since balanced structures show a good immunity to this noise component. If the two switches were instantaneously switching and noiseless, the input noise would have been brought directly to the output. Anyway, the reality is far away from this situation. As already stated, the LO signal is in most cases sinusoidal, slowing down the switching operation of the quad transistors. On top of that, noiseless transistors have unfortunately not yet been invented. If one wants to study the noise behaviour of a balanced mixer considering the mentioned non-idealities, a systematic approach consists in dividing the overall operation of the switching cell into two time intervals. An explanatory picture is given in Figure 4.4, where the MOS noise model of Figure 3.1 has been considered. The first time slot occurs when just one of the switches is ON and the other is OFF, as shown in Figure 4.4(a). In this time window the noise created by the input stage follows the dashed arrow of Figure 4.4(a), being brought to the output with the addition of the switch noise, similarly to the cascode case treated in Chapter 3 (for an accurate analysis, the frequency translation should be also taken into account in this case). The second time slot comes when both the transistors are ON, as in Figure 4.4(b). Within this time window, they inject to the output their own noise, given once again by the combination of gate and drain current noise contributors. In particular, the gate noise is amplified and the drain current noise

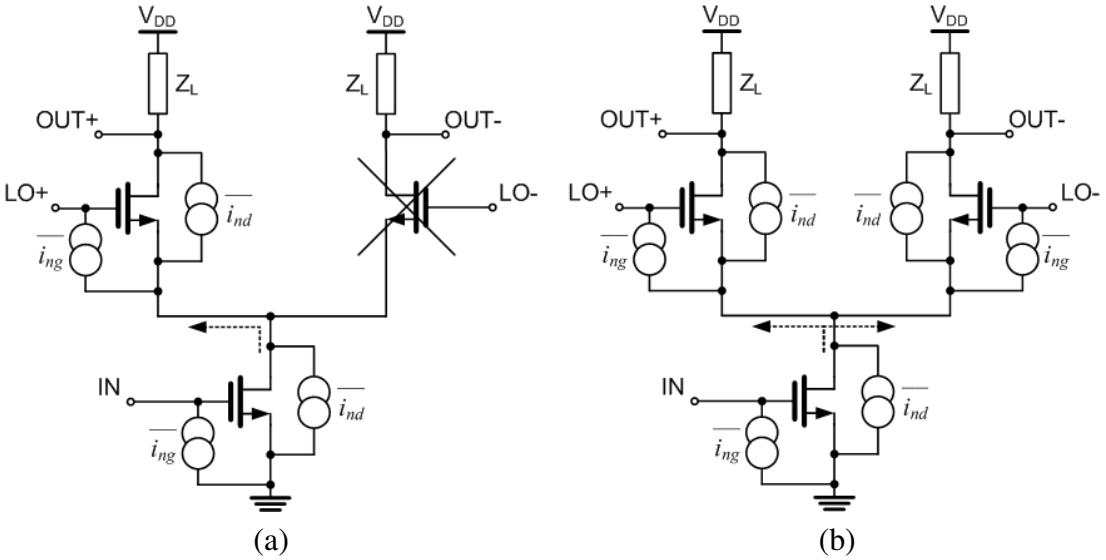


Figure 4.4: Mixer noise with (a) one switch ON and the other OFF and (b) both switches ON.

directly injected. Thanks to the topological symmetry, the noise coming from the input is in this case negligible since a differential output would see it as totally correlated (improperly said, as common mode noise). In fact, it comes from the equal division of the input noise, as shown by the dashed arrows of Figure 4.4(b).

From the above analysis, it is clear how the reduction of the mixer noise passes through the minimization of the noise introduced by the input stage as well as through the lowering of the switching stage injected noise. The input stage is nothing more than a common source transistor, whose noise figure can be reduced as explained in Chapter 3 by proper choice of its size and input noise matching. The switching stage can become less noisy, given a fixed LO swing, reducing both gate and drain noise sources of the switches and making their switching action more abrupt. Looking at the formulas presented in (3.1), the noise sources can be minimized using small transistors, in such a way that the gate-source admittance Y_{gs} is minimized. Anyway, seeing the switching transistors in ON stage as being in a common gate configuration, the impedance seen looking into their source becomes high if their size shrinks, being it proportional to the gate width [77]. This means that if the quad is made by small transistors, the input signal prefers the way to ground through the capacitance C_m instead of the way towards the output through the switches, lowering the conversion gain and

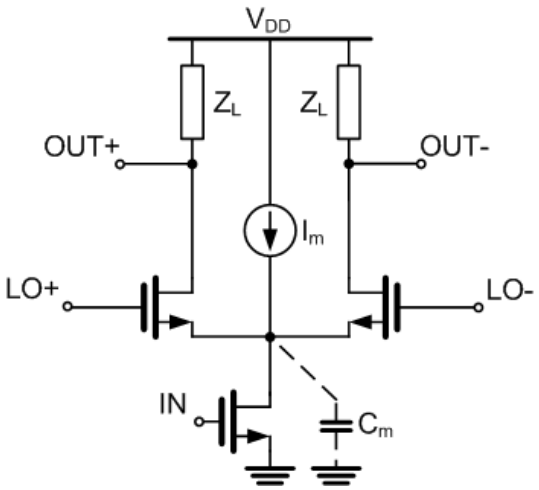


Figure 4.5: Current bleeding mixer.

consequently the noise figure. A more abrupt switching can be reached lowering the DC bias current through the switches. In other words, a faster commutation can be achieved when the RF signal is the most significant current given to the switches. This remedy can be adopted by decoupling the input stage DC current from the one in the switching stage.

A widely used solution is called current bleeding [78], where a current source furnishes the DC current to the input stage reducing the DC current carried by the switches. An example of current bleeding mixer is reported in Figure 4.5. This configuration suffers heavily from the presence of the parasitic capacitance C_m, which is the equivalent capacitance at the middle node already showed in Figure 4.3. Being the DC current through the switches very small, this results in a drastic reduction of their transconductance, and therefore in a further increase of their input impedance. This leads to a higher signal loss through C_m. Furthermore, the current source I_m is usually a MOS transistor, which not only gives its noise contribution to the circuit but also concurs with its parasitics in making C_m growing.

The above analysis cleared how the design of a low noise mixer is not an easy task. It has been seen how in addition to a low noise input stage, a low noise switching stage has to be realized. In order to do that, the switching operation should be made more abrupt and the middle capacitance C_m should be minimized. A design which addresses at the same time these two issues, namely the improvement of the switching operation

together with the minimization of the parasitic capacitance C_m, is presented within the next section.

4.3 Double balanced resonating current bleeding mixer

The frequency plan of the WiONet system is reported in Table 4.1. The targeted mixer is a down converter required to translate the received data from the band at around 60 GHz to the one at around 20 GHz. Being the whole WiONet system differential, including the LO distribution network, the mixer has to be also fully differential, with differential input, output and LO ports. Considered the very low gain offered by CMOS components at very high frequencies, the use of an active topology is desirable in the present design. These are the main reasons justifying the selection of a double balanced Gilbert cell [79] as topology for the considered mixer.

Looking at the frequency plan, it is clear how no image rejection is needed, being in this case the image at around 20 GHz very well filtered out by the bandpass nature of the circuit. Another consequence of the great distance between RF frequency and image frequency is that the single sideband noise figure and the double sideband noise figure are in this case equal, being the conversion gain at the image frequency extremely low. The LO signal is as well filtered out, in this case by the output matching network, but this filtering action is usually not enough. The LO rejection peculiar of double balanced structures improves the IF-LO isolation until the desired level.

As remarked within the previous section, a solution which speeds up the switching operation of the quad and cancels the effect of the capacitance C_m is needed if one

Table 4.1: WiONet frequency plan

	Channel 1	**Channel 2**	**Channel 3**	**Channel 4**
f_{RF} [GHz]	57.24–59.40	59.40–61.56	61.56–63.72	63.72–65.88
f_{LO} [GHz]	38.88	40.32	41.76	43.20
f_{IF} [GHz]	18.36–20.52	19.08–21.24	19.80–21.96	20.52–22.68

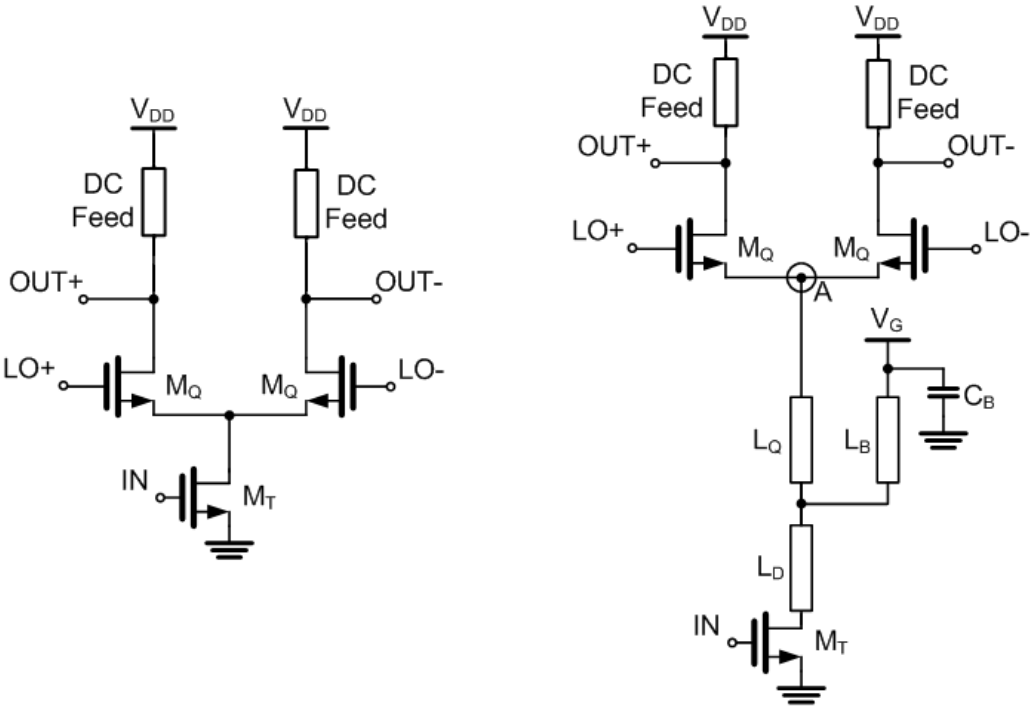


Figure 4.6: Half Gilbert cell: (a) conventional topology and (b) with resonating current bleeding network.

wants to design a low noise down converter. A resonating current bleeding network suits these requirements [80]. Figure 4.6 shows the differences between the conventional active mixer and the one with resonating current bleeding network. For simplicity, in Figure 4.6 only half circuit is depicted.

The current bleeding network performs two different tasks. At first, it decouples DC-wise the input stage from the switching one, giving the possibility to bias the node A to an optimum DC voltage. The optimum bias voltage is chosen in such a way that the quad does not carry any DC current, which is supplied to the input stage through the current bleeding network. This makes the M_Q transistors switching faster, since they have to switch only the signal current [80]. The benefits given by this additional degree of freedom are cleared in Figure 4.7, where conversion gain and noise figure of a double balanced switching quad are shown with respect to the bias voltage V_G. These simulations have been made keeping RF, LO and IF ports matched and the LO power constant. At the optimum V_G of 800 mV, an improvement of 2 dB conversion gain and

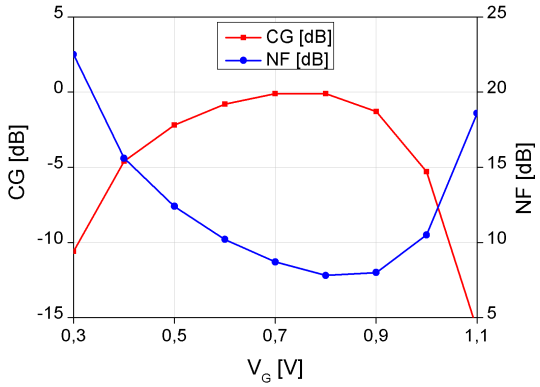


Figure 4.7: Resonating current bleeding network bias voltage impact.

5 dB noise figure can be appreciated with respect to the conventional double balanced cell, which corresponds to a V_G of approximately 500 mV in Figure 4.7. Furthermore, the current bleeding network resonates out the parasitic capacitance C_m at the node A, giving a certain degree of impedance matching at that point. The analysis just carried out justifies the choice of inserting into the chosen double balanced Gilbert cell a resonating current bleeding network.

In order to measure the down converter in a stand-alone fashion, the LO signal has to be given as single-ended. This is the reason why an on-chip balun has to be designed and inserted into the LO path. Figure 4.8 shows the full schematic of the designed down converter [81]. The mixer can be divided into four main parts, namely the switching quad, the input differential pair, the passive networks (input matching, output matching and current bleeding) and the LO balun. Each of them requires an accurate optimization in order to maximize the performance of the entire down converter.

4.3.1 Switching quad design

In order to optimize the quad performance, the sizes of its transistors, named M_Q in Figure 4.8, have to be chosen as well as their bias point. A high frequency integrated design must also take into account all the layout issues that can be encountered. Such issues are very relevant when complex structures as the Gilbert cell have to be laid out. The routing of signals at three different frequencies, each of them carried around

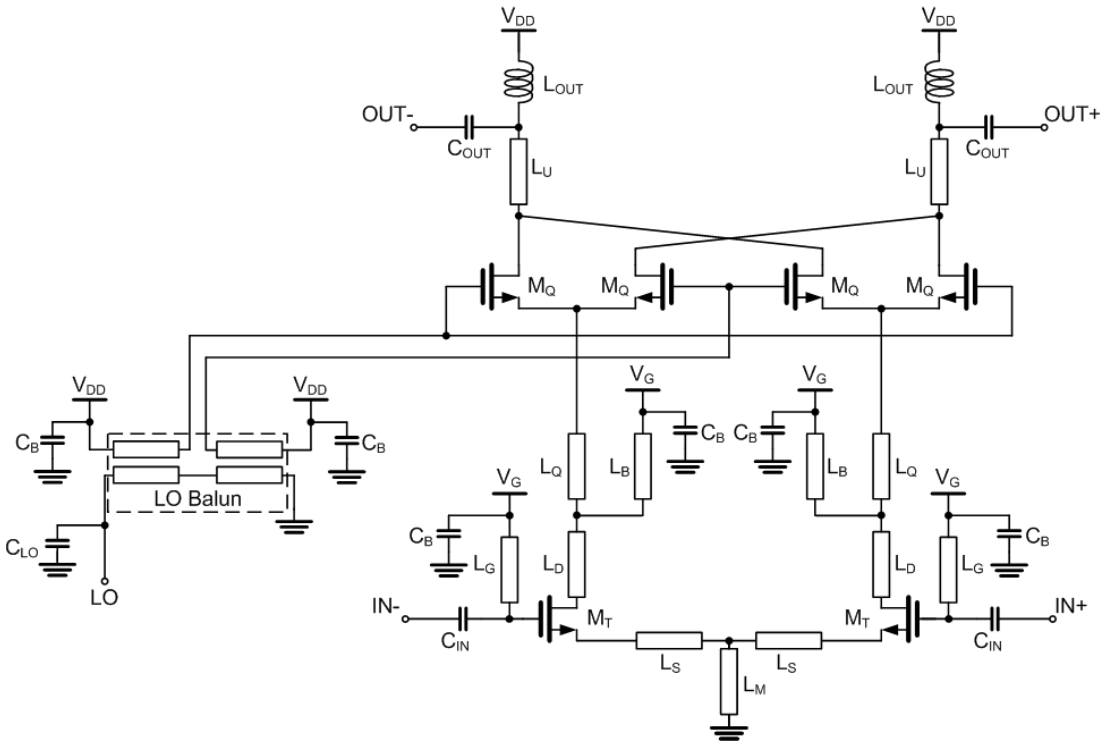


Figure 4.8: Schematic of the down converter.

in a differential fashion, is not an easy task to solve. In the present design, undesired couplings are avoided by using metal shields where lines carrying signals at different frequencies are close to each other. Some cross overs are anyway unavoidable: the cross talking is limited letting cross each other only differential lines carrying signals at the same frequency. The layout is kept as symmetric as possible, and tapers have been used to avoid impedance jumps. The whole switching core has then been EM simulated.

Regarding the optimization of the M_Q transistors, Figure 4.9 shows simulated conversion gain and noise figure of the switching quad for various M_Q sizes, obtained keeping matched all the ports and with LO power and V_G fixed from time to time at their optimum values. From Figure 4.9 is clear how the optimum total gate width is around 50 μm. Considering that transistors with a large number of fingers have a wide layout and would introduce, as already mentioned in Chapter 3, an unacceptable impedance step in their connections, the chosen M_Q transistors have gate width of 5 μm and 10 fingers.

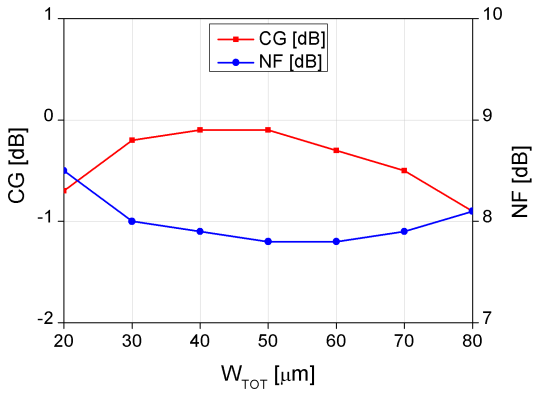


Figure 4.9: Switching quad optimization. All the ports are kept matched, while LO power and V_G are fixed from time to time to their optimum value.

4.3.2 Input differential pair design

The input differential pair is designed with the aim of making a trade-off between gain and noise figure. Two very small inductors, called L_S in Figure 4.8, are introduced as source degeneration for stability reasons, while L_M performs a certain common mode rejection. The transistors M_T are sized with a total gate width of 36 µm, 12 fingers each 3 µm wide, since this size has been found giving a good compromise between noise figure and gain [62] and has been already used in the design of the fully differential LNA presented in Chapter 3. The gate bias voltage is adjusted to be the same as the current bleeding network DC voltage, in order to reduce the number of DC pads and ease the layout.

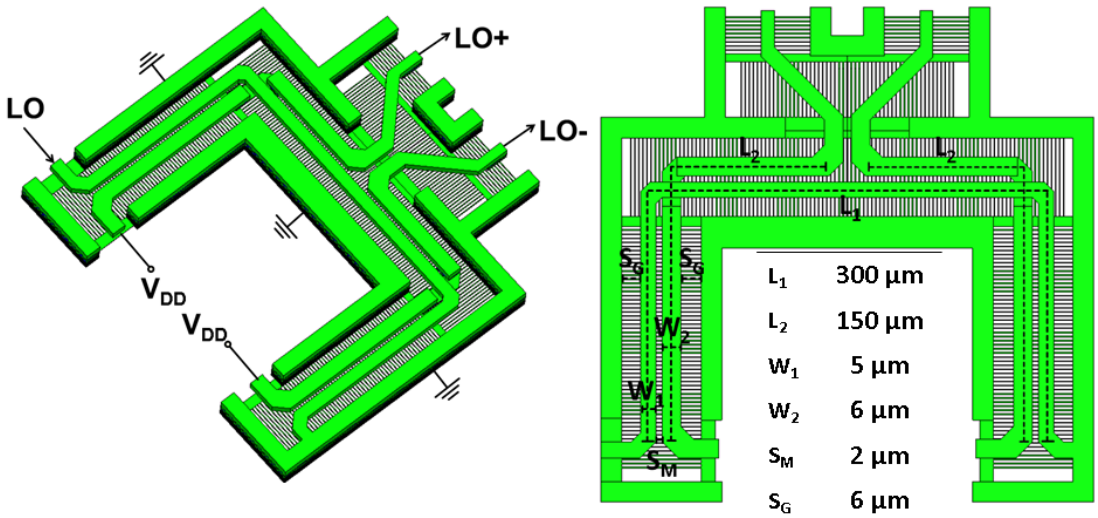
4.3.3 Passive networks design

Most of the inductive elements in the design are SCTLs. Spiral inductors are used for the output matching network instead (L_U in Figure 4.8) in order to save chip area, since their self resonance frequency is far enough from the frequency of the output signals. The input matching network is designed to match the optimum noise input impedance to the differential 100 Ω, while the output matching is performed in order to match for maximum conversion gain in a large signal fashion. The resonating current bleeding network matches the output of the differential pair to the input of the switching quad, in order to cancel the impedance mismatch between these stages, resonating out the

parasitic capacitance C_m. The DC decoupling capacitors C_{IN} and C_{OUT} have been inserted for measurement purposes, but they have to be taken into account during the matching networks design as well as the pad structures. The capacitors C_B represent a bank of 1 pF capacitors in parallel, used as RF-ground. Their number depends from time to time on the free area available in the layout.

4.3.4 LO balun design

An LO balun is inserted to obtain a differential signal from a single LO input. Due to the narrow band characteristic of lumped element based baluns, a transformer based topology is chosen [82]. In order to fulfil the density rules of the technology without inserting any dummy metal filler, which would introduce uncontrollable parasitic effects especially at very high frequencies, edge-side coupled SCTLs are employed. Their width, length, mutual distance and spacing to the side ground walls are optimized in order to reach minimum losses and high balancing between the two outputs. Figure 4.10 shows in (a) the 3D view and in (b) the top view and the dimensions of the designed balun. An input shunt capacitor, named C_{LO} in Figure 4.8, is inserted to improve the input matching of the balun. Its simulated effect is shown in Fig. 4.11, where the input impedance of the balun at 40 GHz is plotted on the Smith chart varying



(a) (b)

Figure 4.10: LO balun: (a) 3D view and (b) top view.

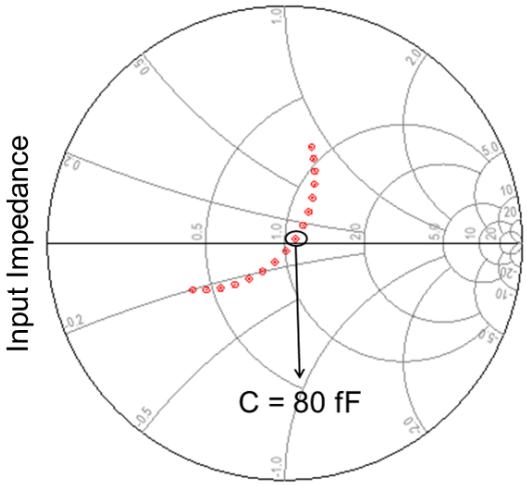
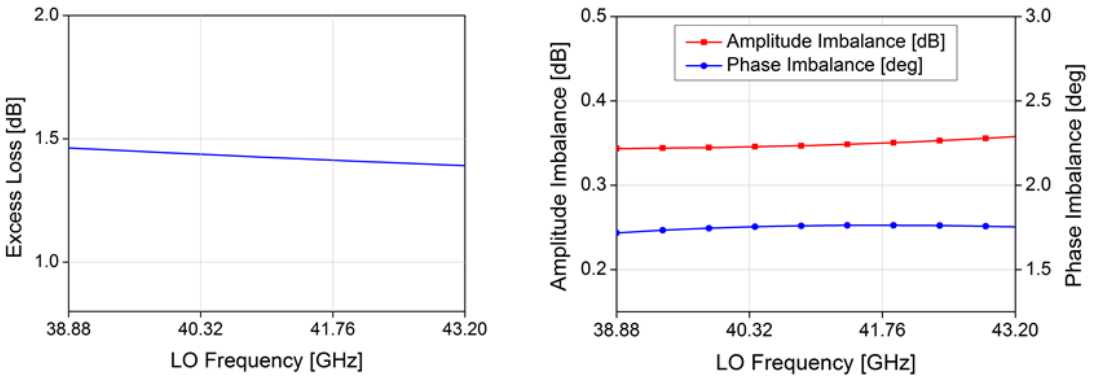


Figure 4.11: Simulated effect of the capacitor C_{LO} on the input impedance of the LO balun at 40 GHz.

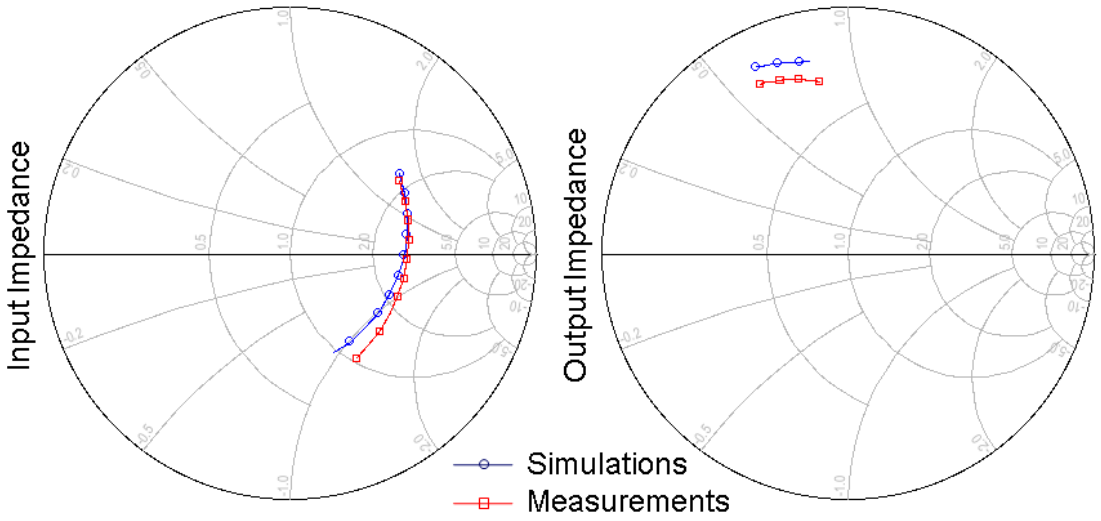
the value of this capacitor. In Fig. 4.11 is visible that a C_{LO} of 80 fF matches very well the input of the balun to 50 Ω.

The simulated performance of the designed LO balun are reported in Figure 4.12 in terms of excess loss, amplitude and phase imbalance. In simulation, along the four LO frequencies the balun loses 1.4 dB and its two outputs present a difference of 0.35 dB in amplitude and 1.75 º in phase. The LO balun is measured stand-alone for validating its design. For measurements purposes, one of the outputs is terminated on-chip to 50 Ω,



(a) (b)

Figure 4.12: LO balun simulated performance along the LO frequencies: (a) excess loss, (b) amplitude and phase imbalance.



(a) (b)

Figure 4.13: LO balun, simulations vs. measurements: (a) input and (b) output impedances.

while the other is brought out via pad as well as the input. The design includes the matching capacitance C_{LO}. Figure 4.13 shows the comparison between simulations and measurements in terms of input and output impedances at the LO frequency range. The closeness between simulated and measured results confirms the goodness of the design process.

4.3.5 Mixer measurements

After the design of all the constituting parts, they have been put together and the complete down converter has been manufactured. Its chip micrograph is reported in Figure 4.14. The sizes of the used components are summarized in Table 4.2.

The down converter has then been measured on wafer at the room temperature. Figure 4.15 shows the input return loss, while Figure 4.16 the conversion gain and the noise figure at the four IEEE 802.15.3c standard channels. The linearity measurements at the central frequency of the second channel, that means with a f_{RF} of 60.48 GHz and a f_{LO} of 40.32 GHz, are shown in Figure 4.17. All the measurements are carried out with a LO power of 2 dBm.

Table 4.2: Down converter components size

Component	Size
C_{IN}	300 fF
C_{OUT}	135 fF
C_{LO}	90 fF
C_B	1 pF
M_T	$12 \times 3\,\mu m$
M_Q	$10 \times 5\,\mu m$
L_G, L_D	150 µm
L_S	30 µm (W = 11 µm)
L_M	180 µm
L_B	290 µm
L_U	80 µm
L_Q	140 µm
L_{OUT}	2.5 turns, spacing 2 µm, radius 20 µm

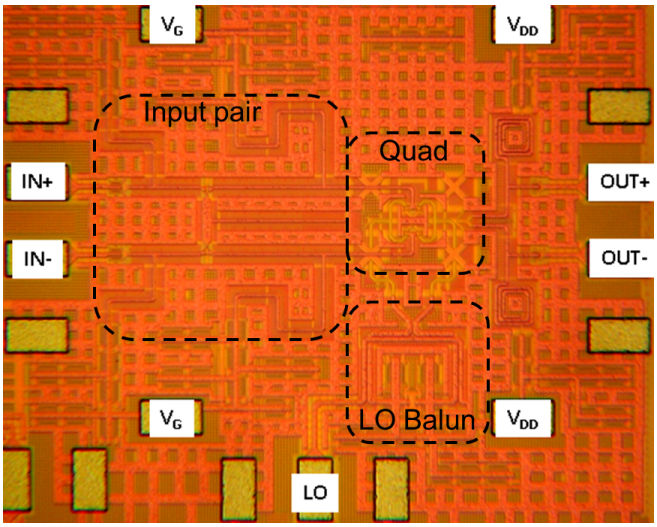


Figure 4.14: Down converter micrograph. The chip size is 0.54 mm^2.

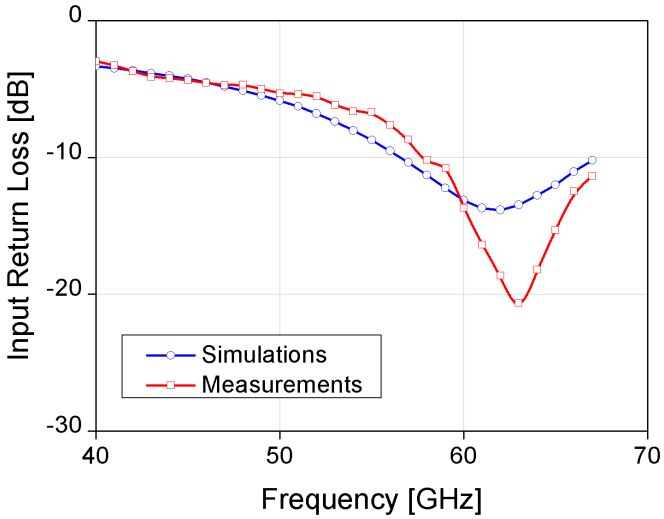


Figure 4.15: Down converter input return loss. The DC voltages are V_{DD} = 1.2 V and V_G = 0.8 V.

A measured conversion gain between -5 dB and 0 dB and a noise figure of around 11 dB are achieved within all the channels, consuming only 11.6 mW. The occupied chip area is 0.54 mm^2 pads included. Thanks to the layout symmetry, an IF to LO

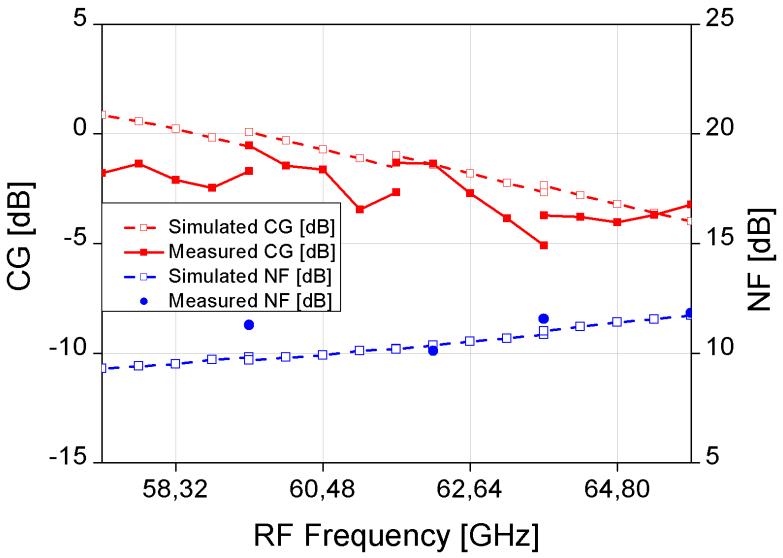


Figure 4.16: Down converter conversion gain and noise figure along the IEEE 802.15.3c channels. The DC voltages are V_{DD} = 1.2 V and V_G = 0.8 V.

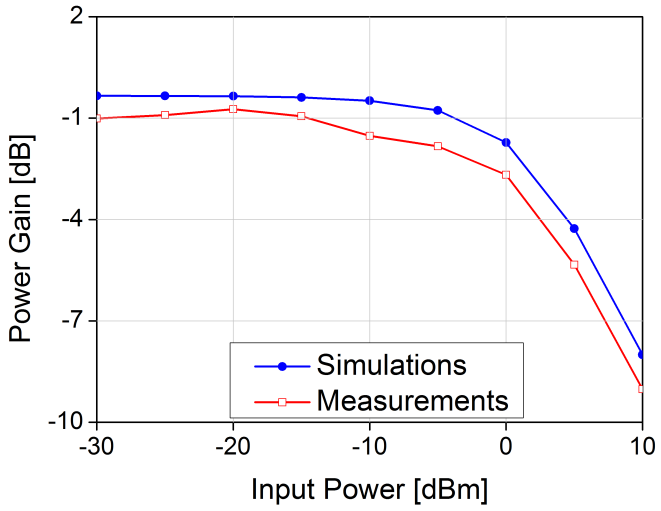


Figure 4.17: Down converter large signal power gain with f_{RF} of 60.48 GHz and f_{LO} of 40.32 GHz. The DC voltages are V_{DD} = 1.2 V and V_G = 0.8 V.

isolation greater than 40 dB is measured all over the channels, together with an LO-RF isolation of more than 70 dB. The measured IP1dB is of about -1 dBm.

Table 4.3: Performance comparison between this work and recently published 90 nm CMOS down converters

Reference	[83]	[84]	[85]	[86]	**This work**
IF frequency [GHz]	4	1	0.1	0.1	**20**
Conversion Gain [dB]	-1.2	12	15.5	0	**-2.5**
NF [dB]	N.A.	13.25	12.8	12	**11**
IP1dB [dBm]	-0.5	-23	-25	-10.5	**-1**
P_{LO} [GHz]	1.5	-13	-5	-2	**2**
Supply [V]	1.2	1.2	1.8	1.2	**1.2**
P_{DC} [mW]	30	8.8	17	7.2	**11.6**
Area [mm^2]	0.49	0.24	0.44*	0.22	**0.54**
Output Buffer	YES	YES	YES	YES	**NO**

* Without pads

Table 4.3 reports the comparison between this work and the state of the art V-band 90 nm CMOS mixers [83–86]. The resonating current bleeding approach allows achieving an outstanding noise figure, along with an acceptable conversion gain and a good IP1dB. The other performance are in line with the state of the art. The achieved conversion gain is lower then the others here reported due to the higher IF frequency, namely 20 GHz, and to the absence of any output buffer.

The obtained performance fulfil the system requirements presented in Table 1.5, and can be used together with the LNA presented in Chapter 3 within the receiver chain of the WiONet system.

Chapter 5

Conclusion and future work

This work describes the design of a low noise amplifier and a down conversion mixer thought to be used within a super-heterodyne V-band transceiver system for short-range high data-rate communication using a commercial 90 nm CMOS technology.

After the extraction of the circuit specification, active and passive components to be used in the designs have been systematically characterised in order to validate their model and ensure the functionality of the electro-magnetic simulation process.

The design of the low noise amplifier has been performed through different steps. At the beginning, a cascode topology has been employed in the development of two different single-ended single stage amplifiers, one optimized for low noise performance and the other for high gain, which have been integrated in a three-stages LNA. Being the noise performance of such amplifier not enough for satisfying the system specifications, after an analytical study of the noise behaviour of different LNA topologies, validated by the measurements of a two-stage LNA, a common source based fully differential four stages amplifier has been designed, which improved the noise figure to a satisfying value. More in details, the designed LNA offers 21.3 dB peak gain and 5.4 dB average noise figure, along with -22 dBm IP1dB. It consumes only 30 mW and occupies a silicon area of 0.38 mm^2. The LNA satisfies the required specifications being its gain greater than 15 dB over the whole band of interest, its noise figure lower than the required 6.6 dB and its compression point enough to process the maximum input power without significant distortion.

The down conversion mixer has been designed based on some gain and noise considerations. An active topology has been chosen because of its relatively low losses,

while a double balanced structure has been exploited to reject the large LO signal. A resonating current bleeding network has been introduced in order to both reduce the current commutated by the switching transistors and resonate out the parasitic capacitance at the interface between input and switching section. Then, all the single parts of the down converter have been carefully optimized in order to minimize both the introduced noise and the conversion losses. The down converter shows an average conversion gain of -2.5 dB and an average noise figure of 11 dB, together with a -1 dBm IP1dB. Its power consumption is 11.6 mW, while the occupied silicon area is 0.54 mm^2. As well as the designed LNA, this down converter fulfil the system specifications, since its conversion losses are smaller than 5 dB, its noise figure constantly less than 12 dB and its IP1dB such that the maximum input power can be easily handled.

The specifications and the achieved performance are here summarized in Table 5.1, where can be easily seen how the designed circuits are appropriate for their use within the WiONet transceiver system. In both cases, the comparison with the state of the art shows that the designed circuits are between the most successful implementations in 90 nm CMOS technology.

The measured circuits are stand-alone designs. Even if a simple connection of the two circuits will still meet the system requirements, their integration into a receiver can bring further benefits. At first, the lossy signal pads can be removed, since in an integrated version they will be needed only at the input of the LNA. On top of that, the output matching network of the LNA and the input matching network of the down

Table 5.1: Requested specifications and achieved performance

		Specifications	**Performance**
LNA	**Gain**	15 dB	$>$ 15 dB, peak 21.2 dB
	Noise figure	6.6 dB	$<$ 6.4 dB, average 5.4 dB
	Maximum input power	-25.2 dBm	-22 dBm (IP1dB)
Mixer	**Conversion Gain**	-5 dB	$>$ -5 dB, average -2.5 dB
	Noise figure	12 dB	$<$ 12 dB, average 11 dB
	Maximum input power	-3.2 dBm	-1 dBm (IP1dB)

converter can be removed and replaced by a more efficient inter-matching network. Finally, being the LO distribution network of the WiONet system fully differential, the LO balun used for the single to differential conversion at the mixer LO port can be replaced by a simpler and less lossy differential matching network. However, the presented circuits are an excellent starting point for the design of a high performance CMOS V-band receiver.

Appendix A

Measurement setup

In this appendix, the measurement method used for evaluating the circuits of the present work will be introduced. A brief explanation will be given within the first paragraphs on s-parameters and power measurements. The second part will be focused on noise measurements, starting with a general overview and focusing afterwards on the methodology adopted for the noise evaluation of amplifiers and down-converters.

A.1 S-Parameters measurements

Measuring s-parameters in the 60 GHz band is nowadays straightforward. In fact, modern 67 GHz Vector Network Analyzers (VNA) allow to measure s-parameters directly both in single-ended and differential mode. For the s-parameters measurements shown in this thesis, a ZVA67 from Rohde&Schwarz has been employed[1]. The measurement setup is here reported in Fig. A.1.

V-band 50 Ω cables and Cascade on-wafer probes[2] have been calibrated out performing a through-open-short-match (TOSM) calibration [87] using an on-wafer calibration setup from Cascade[3].

As previously mentioned, the ZVA allows both single-ended and differential measurements, having four different ports which can be set at different configurations. In

[1] http://www.rohde-schwarz.com
[2] http://www.cascademicrotech.com/products/probes/rf-microwave/z-probe
[3] http://www.cascademicrotech.com/products/calibration-tools

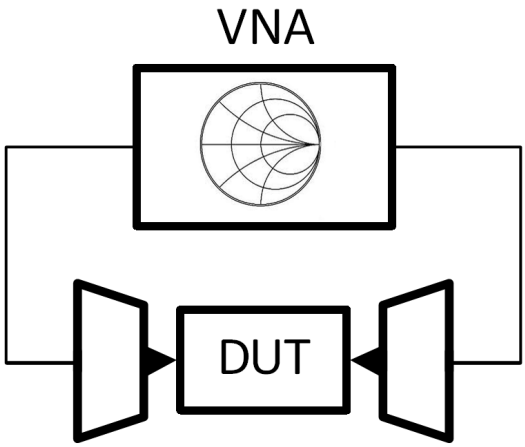


Figure A.1: S-parameters measurements setup.

Fig. A.1, the ports of the network analyzer, the cables and the probes have to be considered as single in the case of a single-ended device under test and as differential in the case of differential s-parameters measurements.

A.2 Power measurements

A spectrum analyzer is not the best tool to be used for measuring power. Anyway, when the power to be measured is not too high, it can be still employed with acceptable precision. In order to confirm the results, the spectrum analyzer can be calibrated for comparison with a more accurate power meter. This is what has been done when power measurements had to be performed. The used spectrum anaylzer is a Rohde&Schwarz FSU67[1], while the input signal has been given to the circuit through the signal generator Agilent 83650B with an additional V-band extension. The measurement setup is here reported in Fig.A.2. In this case, what is important to know are the losses of the output network from the reference plane B to the spectrum analyzer. At first, a through measurement has been performed in order to have information on the total losses. Measuring directly the input power until the reference plane A and adding the losses of input probe and calibration through line as reported in their datasheet, the losses of the output network can be easily calculated. It has to be noticed, that neither

[1] `http://www.rohde-schwarz.de`

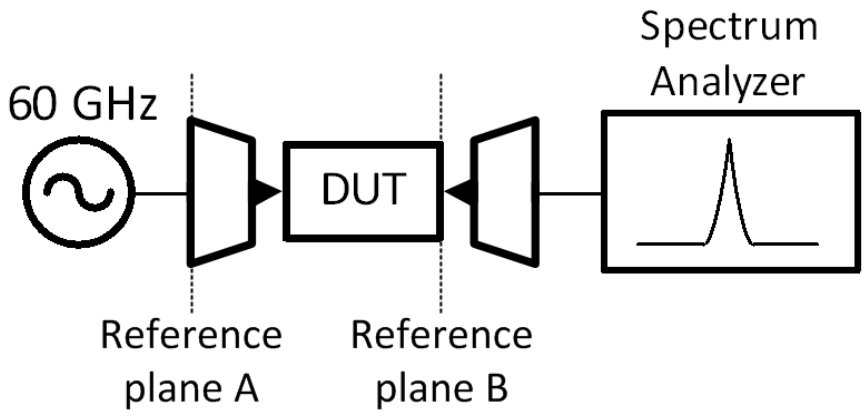


Figure A.2: Power measurements setup.

the signal generator nor the spectrum analyzer are able to deal with differential signals. Differential circuits are measured by making use both in input and in output of RF probes with integrated balun, made available from Cascade[1].

A.3 Noise measurements

Measuring noise of a circuit is often a very sensitive process and a lot of care has to be taken in order to account for all the possible sources of error. Particularly error prone are electronic systems with very low noise figure, whose noise measurements can be affected by all the environmental noises. Fortunatelly, the circuits measured in this work can not be defined as very low noise circuits, being their noise figure always higher than 5 dB. In the present case, the biggest issue to be overcome is the low gain presented by some circuits. In fact, when the gain is under a certain threshold the measurement device can reach its sensitivity limit. In these cases, the use of a low noise and high gain post amplifier will make the measurement process possible. A schematic view of the setup used for noise measurements is reported in Fig. A.3.

The method used for measuring the noise performance of the circuits presented in this thesis is the Y-factor method, very widely used in the microwave world [88]. The instruments used for this kind of measurements, their settings and the basics of the Y-factor method itself will be introduced in the next sections.

[1] https://www.cmicro.com/products/probes/rf-microwave/infinity-probe

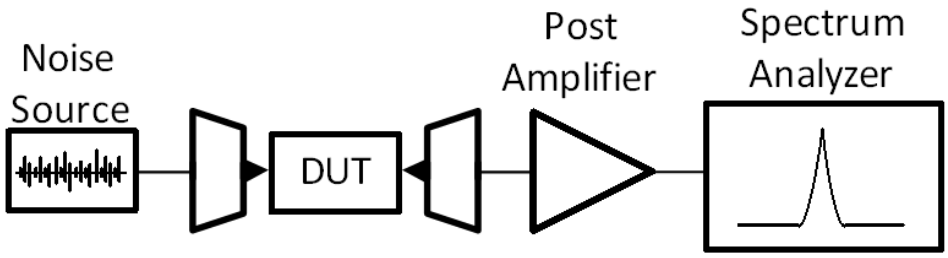


Figure A.3: Noise measurements setup.

A.3.1 Noise source

The Y-factor method requires the use of a calibrated noise source. A noise source is nothing else than a diode whose operating region can be switched by an external DC voltage. Usually, the external voltage switches the diode between cut-off and break-down region, in such a way that it gives no output when it is OFF and a noise power when it is ON. These two states are called “cold” the first one and “hot” the second. A noise source can be represented by a quantity called Excess Noise Ratio (ENR), defined as in (1) and often reported in decibel.

$$ENR = \frac{T_{s,ON} - T_{s,OFF}}{T_0} \tag{1}$$

In (1) $T_{s,ON}$ and $T_{s,OFF}$ are the noise temperatures of the noise source at the ON and at the OFF states respectively, while T_0 is the reference temperature, usually set at 290 °K. Calibrated noise sources are usually referred to T_0, meaning that $T_{s,OFF}$ is equal to T_0. Keeping the temperature of the noise source at T_0 during the measurements through an air conditioner, no temperature correction is needed. The used noise source is a V-band Noisecom NC5215 with waveguide output and ENR of around 17 dB[1]. Some components have been added at its output. They are a waveguide to coaxial transition, to insert it into a fully coaxial measurement system, and an output isolator, to improve its output matching. These additional components slightly modify the noise source characteristics, so that its ENR has been recalibrated after their insertion. The used noise source can be controlled switching the external DC voltage between 0 V and 28 V.

[1] `http://www.noisecom.com/products/calibrated-sources`

A.3.2 Post amplifiers

As already stated, a post amplifier helps in measuring the noise figure of low gain devices. In fact, during the "cold" measurements, that is with noise source OFF, the risk is that the power coming out from the device under test is below the noise floor of the measurement instrument. A post amplifier between device under test and spectrum analyzer works to avoid this risk. For amplifiers noise measurements, a V-band MITEQ post amplifier with 4.5 dB noise figure at around 60 GHz has been used[1]. For down converter noise measurements, being the DUT lossy, in output is required a very high gain block. That is the reason why an amplifier chain with a total noise figure of 6.5 dB at around 20 GHz has been employed.

A.3.3 Spectrum analyzer settings

The settings of the spectrum analyzer play a very important role as well. As stated in [88], its resolution bandwidth should be much narrower than the bandwidth of the device under test because of two different reasons. The first reason is to push down the instrument noise floor, while the second one is to avoid that the measured noise takes into account components out of the considered bandwidth. Being noise a time-variant quantity, the averaging facility of the spectrum analyzer is heavily exploited. Each measurement is here the result of about hundred averaging cycles. Last but not least, for a good accuracy of the measurement process it is fundamental to keep the same spectrum analyzer settings both during calibration and measurement.

A.3.4 The Y-factor method

The Y-factor method is the most used method to measure noise figure of electronic systems. It consists of the calculation of the Y-factor, defined as the ratio between two noise powers, N_{ON} measured at the "hot" state, that is with the noise source ON, and N_{OFF} measured at the "cold" state, that is with the noise source OFF. Its definition is in (2) reported [55].

$$Y = \frac{N_{ON}}{N_{OFF}} \tag{2}$$

[1] `http://www.miteq.com`

The Y-factor together with the ENR of the noise source can be used to find the noise factor of the system as in (3).

$$F = \frac{ENR}{Y-1} \tag{3}$$

This formula allows to calculate the system noise factor after a set of two measurements, one at the "hot" state and one at the "cold" one. The noise factor of the device under test can be easily calculated afterwards. The effect of input connections, such as cables and probes, can be easily removed since they are passive elements and add an amount of decibels to the noise figure equal to their losses. The effect of the output connections and of the post amplifier has to be deembedded applying the Friis noise formula [31], assuming as known the gain of the device under test.

A.3.5 LNA noise measurements

The setup employed for amplifier noise measurements is similar to the one shown in Fig. A.3. This is reported in a more detailed way in Fig. A.4.

The noise source is switched ON and OFF via a DC supply. A post amplifier is employed for improving the sensitivity of the system. In the case of differential amplifiers, as in [62], the input and output balun probes have to be deembedded. Such a deembedding is performed as presented in [65]. This procedure allows to extract the noise factor of the device under test in a configuration like the one shown in Fig. A.5. Knowing the single-ended losses L_1 and L_2 of the baluns, the gain G of the device

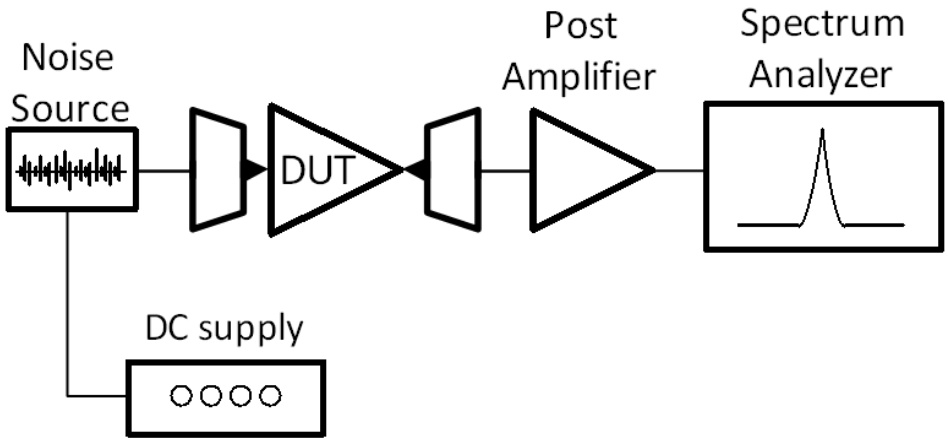


Figure A.4: LNA noise measurements setup.

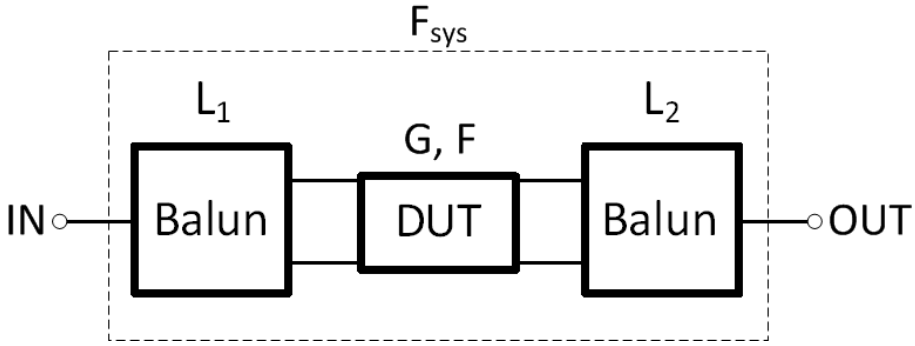


Figure A.5: Differential noise measurements: balun probes deembedding.

under test and the measured noise factor F_{sys} of the system in Fig. A.5, the wanted noise factor can be extracted through the equation reported in (4), which takes into account the noise correlation as well.

$$F = \frac{2F_{sys}}{L_1} - \frac{L_2 - 2}{2L_1} - \frac{2}{G} \tag{4}$$

Basing on the measurement setup of Fig. A.4, the procedure followed for LNA noise measurements can be summarized as follows:

- Calibration:
  - Measurement of the input losses given by the input cable.
  - Measurement of the noise figure of the second stage network, including cables and post amplifier.
- Measurement of the noise figure of the entire system through the Y-factor method.
- Noise figure extraction:
  - Deembedding of the second stage network effect through the Friis noise formula.
  - Removal of the input losses.
  - Deembedding of the probes effect using the losses reported into their datasheets.

A.3.6 Down converter noise measurements

The measurement setup built in order to measure the noise figure of the down converter is in details shown in Fig. A.6. Being the mixer to be measured fully differential [81], the input signal needs to be converted from a single ended one using balun probes, as done in the case of the differential LNA. In output, one of the two signals is connected to the spectrum analyzer, being the other closed to 50 Ω. The measurements have been in all cases repeated swapping the output connections. The LO signal, made differential by an integrated balun, is supplied by an Agilent 83650L signal generator. The software option FS-K30 [89] embedded into the Rohde&Schwarz FSU67 spectrum analyzer is used in this case. This facility requires to enter only the frequencies to be considered and the ENR of the noise source. Before the measurement process itself starts, the noise source has to be automatically calibrated connecting it directly to the spectrum analyzer. After the connection of the system as in Fig. A.6, the measured noise figure will be plotted on the screen of the spectrum analyzer. Anyway, this option has been used to measure the overall noise figure of the system, being cables, probes and post amplifier later deembedded as done for the LNA noise measurements. It has

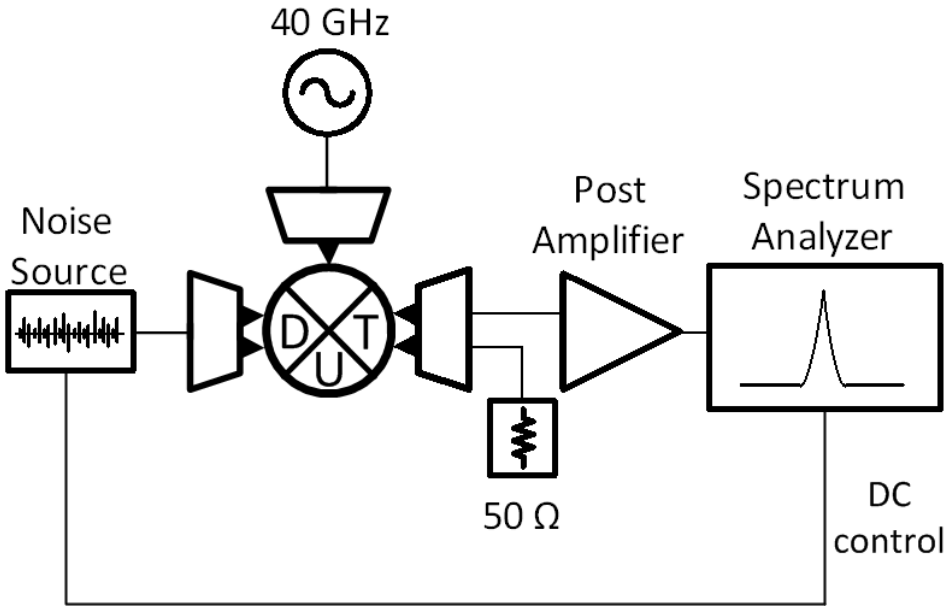


Figure A.6: Down converter noise measurements setup.

to be noticed that, as visible in Fig. A.6, the switching of the noise source is now controlled directly by the spectrum analyzer.

Basing on the measurement setup of Fig. A.6, the procedure followed for down converter noise measurements can be summarized as follows:

- Calibration:
  - Measurement of the input losses given by the input cable.
  - Measurement of the noise figure of the second stage network, including cables and post amplifier.
  - Calibration of the noise source.
- Measurement of the noise figure of the entire system through the FS-K30 software option.
- Noise figure extraction:
  - Deembedding of the second stage network effect through the Friis noise formula.
  - Removal of the input losses.
  - Deembedding of the probes effect using the losses reported into their datasheets.

APPENDIX A

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