Liquid Phase Crystallized Silicon on Sinusoidal Textured Glass Substrates

– Silicon Material Quality and Absorption Enhancement –

vorgelegt von
M. Sc.
Grit Köppel
geb. in Dachau

von der Fakultät IV - Elektrotechnik und Informatik
der Technischen Universität Berlin
zur Erlangung des akademischen Grades

Doktorin der Ingenieurwissenschaften
– Dr. Ing. –

genehmigte Dissertation

Promotionsausschuss:

Vorsitzender:	Prof. Dr. Bernd Szyszka
Gutachter:	Prof. Dr. Bernd Rech
Gutachterin:	Prof. Dr. Christiane Becker
Gutachter:	Prof. Dr. Janez Krč
Gutachter:	RNDr. Antonín Fejfar, CSc.

Tag der wissenschaftlichen Aussprache: 22. März 2017

Berlin 2017

So viel Bemühungen man sich auch zu diesem Zweck gegeben;
so bleibt doch die völlige Befriedigung
dieser Forderungen nur ein frommer Wunsch
und gar manches künftigen Zeiten vorbehalten.

Johann Wolfgang von Goethe
in „Naturwissenschaftliche Schriften. Optik und Farbenlehre, Physik“

Contents

1 Introduction

In the German tale "*The Schildburghers*" the citizens of the fictive city Schilda were known for their wisdom and had been hired to work as counselors for kings and nobles all around the world. To protect the city from depopulation and doom, one day the Schildburghers decide to take action in order to become well-known for their fatuity instead. One of these bizarre acts had been to build a new town hall without windows and any sources of light. In order to avoid holding council meetings in the dark, the citizens work hard outside to catch the sunlight in buckets, bags and pots, and – though unsuccessfully – try to carry the light inside [1].
The Schildburghers storyline and the thesis presented have a common narrative: finding an efficient way to trap sunlight. However, instead of bringing the light into a town hall, this thesis aims to enhance the amount of light in liquid phase crystallized silicon thin-film solar cells on glass substrates.

Last year's (2015) silicon photovoltaic market share of wafer based technologies amounted to about 93 % of the total annual production [2]. This number includes mono- and multi-crystalline modules, wafers as well as cells. The record lab cell efficiency is 26.3 % using mono-crystalline silicon [3] and 21.3 % using multi-crystalline silicon [4]. In recent years, these solar cells have been developed to operate close to their physical boundaries. A further reduction of costs per Watt peak can no longer trust on an efficiency enhancement only. It requires lower manufacturing costs as well, which in turn calls for lower material consumption. There are several approaches to realize this: first, the utilization of thinner wafers [5, 6], second, manufacturing by kerfless technologies [7, 8], and third, thin-film solar cells [9, 10]. The latter approach was used in this thesis.

By definition, thin-film solar cells have a thickness of less than 50 µm. Hence, they need to be deposited onto a suitable substrate in order to enhance its mechanical robustness and to avoid fracturing of the thin film. The making of such a device faces a number manufacturing and cell design challenges. In particular, a sufficient carrier-collection is required notwithstanding the lesser cell thickness. Thus, measures for efficient light trapping to harvest the available solar cell spectrum in thin absorber

layers are paramount. The major challenge remains to address these challenges with low-cost methods for solar cell fabrication and design.
In 2015 the remaining market share of 7 % accounted for thin-film technologies [11]. This comparatively low market share is conditioned by the lower efficiencies of silicon thin-films compared to wafer based cells. In case of silicon thin-film solar cells, a record efficiency of 10.5 % has been achieved with an absorber layer thickness of less than 2 µm [12]. Therefore, the advantage of thin-film solar cells is not based on a high efficiency but on its promising low cost production. The cost advantages of thin-film silicon are likely to be realized if the support for the thin film is provided by a low-cost substrate. A promising approach comprises crystalline silicon thin-film solar cells on glass, unifying the advantages of thin-film technology, namely the material reduction, suitability for large-scale applications and high throughput, with the high material quality and the abundance of silicon. Glass substrates have demonstrated their suitability as low-cost substrates for depositing silicon thin-films [13]. Indeed, the silicon thin-film record cell mentioned before was prepared on a glass substrate [12].

The technology of directly growing and crystallizing 10 µm thin silicon absorber layers on glass substrates became of particular interest when Liquid Phase Crystallization (LPC) [14, 15] replaced Solid Phase Crystallization (SPC) [16] techniques [13]–[15]. During LPC the sample is scanned with a line shaped electron or laser beam locally heating the silicon absorber layer above its melting temperature. The silicon film solidifies from the melt and recrystallizes into grains that are up to a few centimeters in length and several millimeters in width [17, 18].
Thinning the silicon layer from typical wafer thicknesses of around 200 µm to about 10 µm in a thin-film device causes a reduction of absorption. This especially accounts for light with wavelengths in the near-infrared range being only weakly absorbed in an optical path length of less than 10 µm. Moreover, due to its indirect band gap silicon exhibits a small absorption coefficient in this spectral range. Insufficient optical absorption is a major factor limiting the device current of silicon thin-film solar cells. Thinned absorber layers demand for the implementation of an efficient light trapping scheme. A suitable light trapping scheme can increase the optical path length within the absorber layer based on a larger number of internal reflections enhancing the probability of light to be absorbed.
Light trapping textures at different interfaces for thin-film solar cell devices have been in the focus of various experimental and numerical studies. The shape and geometry of the light scattering structure vary widely depending on the underlying cell design. Current research includes random [19–22] and periodic structures, like photonic crystals [23–29] and plasmonic scatterers [5, 30–32] or even a combination

of both [33–35], as well as structures produced by etching in various shapes like wires [36], hole arrays [37] or pyramids [38]. If the absorber layer is grown on top of the light trapping texture, not disturbing the material quality of the absorber layer has also to be safeguarded [20, 39–41].

In current cell designs of liquid phase crystallized silicon thin-film solar cells light trapping schemes are only applied at the air-glass interface as an anti-reflection foil geometrically scattering incident light into the device [42], a pyramidal texture at the rear side of the absorber layer as well as a white back-reflector for long wavelength light. This design enables efficiencies of up to 12.1 % (in-house) [43]. It does not address reflection losses at the planar glass-silicon interface. Thus, the optical potential is not fully exploited. According to an analytical loss analysis conducted by Frijnts et al. [43], reflection losses amount to a short-circuit current density loss of $3.4\,\mathrm{mA\,cm^{-2}}$ and were identified as a major loss mechanism in present device design. To further increase photo-generated current densities effective measures for light management are needed at the glass-silicon interface of LPC silicon thin-film solar cells whilst maintaining the electronic silicon material quality.

A suitable method for fabricating nano-structures on glass substrates for texturing the glass-silicon interface in LPC silicon thin-film solar cells is Nanoimprint Lithography (NIL) [44, 45] in combination with high-temperature stable sol-gels [46–49]. NIL is a technology widely used in industry not only for photovoltaic, but also, e.g. for sensor fabrication [50–52], and has already proven to meet the manufacturing and cost requirements for industrial applications [53, 54]. The high-temperature stability of the sol-gels is a crucial point since the textured substrates have to withstand the high energy input during the LPC process. Such sol-gels have been developed by the companies SCHOTT [55] and Philips [56]. If a textured substrate is used during LPC, the substrate texture can be maintained at the rear side of the absorber layer enabling the fabrication of double-sided textured absorber layers with the same light management texture at both interfaces, the front and the rear side of the absorber layer [57].
In previous work, a statistically etched ZnO:Al texture with a typicall feature size of 1 µm and an aspect ratio of 0.05 as well as a periodic U-shaped texture with a pitch of 2 µm an aspect ratio of 0.5 were implemented [58]. The statistically etched low aspect ratio texture maintained the electronic silicon material quality with respect to a planar reference cell but did not significantly enhance light incoupling into the cell. The U-shaped high aspect ratio texture enhanced the optical properties of the cells but disturbed the silicon material quality resulting in reduced quantum efficiencies [59]. Nevertheless, these structures serve as benchmarks for optical enhancement

and the silicon material quality for LPC thin-films on textured glass-substrates.

The aim of this thesis is to identify a light trapping scheme for LPC silicon thin-film solar cells providing anti-reflective properties in the wavelength range of interest and to demonstrate its suitability for maintaining the silicon material quality. Since the silicon material quality is mainly determined by the crystallization step, the interplay between a substrate texture and the liquid phase crystallization process is analyzed. Nanoimprinted high-temperature stable front surface textures using hexagonal sinusoidal nanotextures are studied for application in state-of-the-art liquid phase crystallized silicon thin-film solar cells. The findings may be used to develop improved cell designs and to gain substantial insights on the liquid phase crystallization process on textured glass substrates.

This thesis is structured as follows:

Chapter 2 provides a brief review of fundamental knowledge for understanding the physical background of the experiments conducted. The review of silicon as a semiconductor material comprises electronic and optical loss mechanisms, light trapping and silicon solar cell device characteristics.

Chapter 3 introduces the experimental methods applied. This chapter covers relevant methods needed for substrate, absorber layer and solar cell preparation as well as for structural, optical and electronic characterization.

Chapter 4 identifies a suitable substrate texture unifying anti-reflective properties at the front interface of the silicon absorber layer with distinguished electronic material quality. Previous work on texturing the glass-interface by nanoimprint lithography is presented. To gain fundamental understanding of the interplay between textured substrates and the liquid phase crystallization process, a one dimensional model texture is examined revealing suitable substrate texture geometries. Based on these results two hexagonal textures, the steep pillar texture and the smooth sinusoidal texture, are developed. These textures are tested regarding their influence on the optical and electronic properties as well as on the silicon material quality of LPC silicon thin-films revealing that the sinusoidal substrate texture is the most promising approach.

Chapter 5 addresses the influence of the sinusoidal substrate geometry on the optical properties of state-of-the-art LPC silicon thin-films. Additionally, the thicknesses of every layer of the solar cell stack are varied in order to maximize absorption

in the silicon layer. Furthermore, the influence of combining the sinusoidal glass-silicon texture with additional light management measures at other interfaces on the optical properties of the silicon absorber layer is studied.

Chapter 6 discusses the influence of the sinusoidal substrate texture on the electronic properties of LPC silicon thin-film solar cells. Electronic properties of a solar cell featuring a sinusoidal substrate texture are analyzed with regard to planar and textured reference cells.

Chapter 7 compares the sinusoidal substrate texture at the glass-silicon interface to alternative approaches. Differently sized random textures are studied in contrast to the sinusoidal substrate texture. The optical potential of the sinusoidal substrate texture is compared to an optically rough but morphologically flat light scattering texture. Finally, a short discussion of the different light management concepts in this thesis is provided.

Chapter 8 summarizes this thesis and introduces suggestions for future research.

2 Theoretical Background

This chapter provides a brief review of basic knowledge for understanding the physical background of the experiments conducted. In the first section crucial fundamentals of silicon as an absorber layer and its interaction with incident light are presented. In two subchapters optical loss mechanisms and essential principles of light trapping are introduced. The second section provides a summary of the electronic properties of silicon and its most common structural defects with subchapters on electronic loss mechanisms and important solar cell device characteristics.

Silicon is an indirect semiconductor and with its band gap of around 1.12 eV at room temperature, which approximately corresponds to a wavelength of about 1100 nm, it is well suited for converting sunlight into electric current [60, 61]. Silicon crystallizes in a face-centered cubic (fcc) diamond structure, where the $\langle 111 \rangle$ plane corresponds to the closed-packed plane. Neighboring atoms are covalently bonded forming sp^3 hybrid orbitals, which are tetrahedrally arranged. A picture of the unit cell is depicted in figure 2.4.

2.1 Optical Properties of Silicon

Conditioned by its indirect band gap silicon can absorb incident light with an energy of less than 3.4 eV or a wavelength longer than 365 nm, respectively, only in a two-step process involving phonons in addition to photons in order to account for energy and momentum conservation [60–63]. Considering electrons in the valence band and in the conduction band with the same k value as well as the occupation probabilities of the states in both bands, the absorption coefficient $\alpha(h\nu)$ of an indirect semiconductor can be derived by summing over all possible inter-band transitions between states [61, 62, 64]:

$$\alpha(h\nu) = \alpha_a(h\nu) + \alpha_e(h\nu), \tag{2.1}$$

where

$$\alpha_a\left(h\nu\right) = \frac{c(h\nu - E_{bandgap} + E_{phonon})^2}{\exp(E_{phonon}/kT) - 1}$$

describes absorption events if a phonon is absorbed (index a) and

$$\alpha_e\left(h\nu\right) = \frac{c(h\nu - E_{bandgap} - E_{phonon})^2}{1 - \exp(-E_{phonon}/kT)}$$

describes absorption events if a phonon is emitted (index e). The parameter c is a material specific constant of typically $10^5\,\mathrm{cm}^{-1}$ to $10^6\,\mathrm{cm}^{-1}$. Optical absorptance $A(\lambda)$ in a semiconductor layer of thickness d is then given by

$$A(\lambda) = 1 - \exp(-\alpha(\lambda) \cdot d) \tag{2.2}$$

Thus, the absorption coefficient $\alpha(\lambda)$ is the quantitative description of the probability for a given wavelength λ to be absorbed within the semiconductor layer. The inverse of the absorption coefficient $\alpha(\lambda)^{-1}$ determines the penetration depth or absorption depth of incident photons of wavelength λ. The absorption coefficient $\alpha(\lambda)$ (equation 2.1) of silicon as well as the penetration depth $\alpha(\lambda)^{-1}$ of light into silicon are depicted in figure 2.1 (a) and optical absorptance (equation 2.2) in the context of the spectral AM1.5g irradiance spectrum [65] for absorber layer thicknesses of 1 µm and 10 µm are depicted in figure 2.1 (b).

The absorption coefficient, or more precisely the absorption depth, can be used to determine the minimum absorber layer thickness required to absorb usable sunlight. For silicon this corresponds to a minimum absorber layer thickness of several hundred µm in order to absorb the entire usable spectrum up to the band gap energy [60, 62, 63, 67]. The photon flux of incident light at depth z in the absorber layer can be calculated according to Lambert-Beer's law by:

$$\Phi(z, \lambda) = \Phi(0, \lambda) \cdot \exp\left(-\alpha(\lambda) \cdot z\right)$$

under the assumption that light enters the semiconductor at position $z = 0$. Accordingly, the generation rate of electron-hole pairs as a function of position within the silicon layer is given by

$$G(z, \lambda) = \int_\lambda \left(1 - R(\lambda)\right) \cdot \Phi(z, \lambda) \cdot \alpha(\lambda) \cdot \exp\left(-\alpha(\lambda) \cdot z\right) d\lambda \tag{2.3}$$

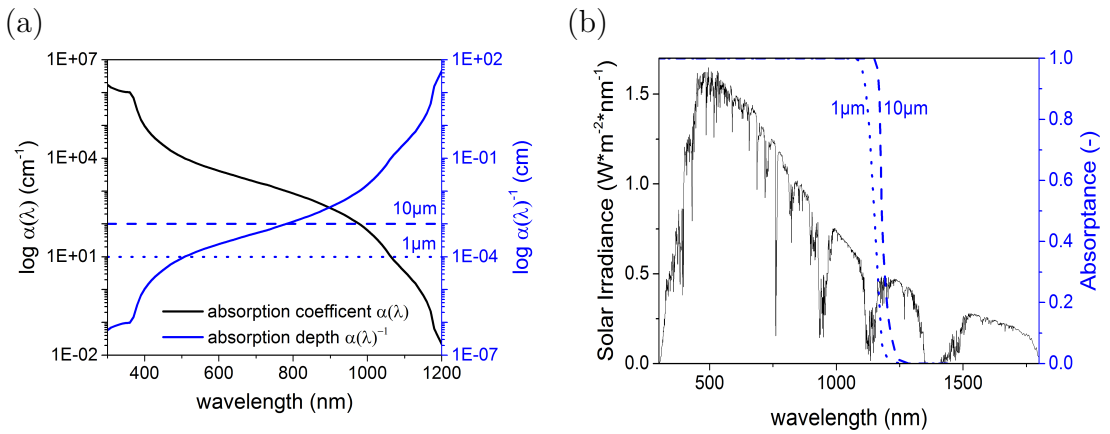


Figure 2.1: (a) Absorption coefficient $\alpha(\lambda)$ (equation 2.1) of crystalline silicon (black) and penetration depth $\alpha(\lambda)^{-1}$ of light into crystalline silicon (blue) in the wavelengths range of interest of 300 nm to 1200 nm at 300 K. The data plotted was taken from [66]. (b) Solar AM1.5g irradiance spectrum (data taken from [65]) and optical absorptance as a function of incident wavelengths depicted for a wavelength range of 300 nm and 1800 nm. Calculated values (equation 2.2) for absorber layer thicknesses of $d = 1\,\mu m$ (dotted) and $d = 10\,\mu m$ (dashed) are added in both graphs.

where $R(\lambda)$ describes the amount of incident light being reflected before entering the silicon absorber layer.

Since the absorption coefficient strongly declines with increasing wavelengths, the majority of carriers are photogenerated within less than a micron of the illuminated surface [60, 63] as it is highlighted by dotted lines in figure 2.1 (a) and (b).

2.1.1 Optical Loss Mechanisms

The propagation properties of light in a medium, e.g. a semiconductor absorber layer, are described by the refractive index

$$n(\lambda) = n'(\lambda) + ik(\lambda)$$

of the respective medium, where

$$k(\lambda) = \frac{\alpha(\lambda) \cdot \lambda}{4\pi}$$

is the extinction coefficient characterizing the degree of attenuation if the electromagnetic wave propagates through the medium. When encountering an interface between two different media the refractive index changes abruptly. This can cause

a fraction of light being reflected back into the initial medium 1 instead of being refracted and proceeding propagation into the second medium [62, 68, 69].

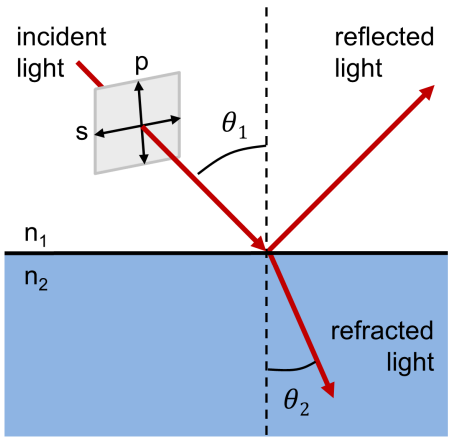


Figure 2.2: Sketch of incident light approaching an interface between two distinct media with refractive indices n_1 and n_2 under an incidence angle Θ_1 being reflected into medium 1 or refracted into medium 2 with an angle of refraction Θ_2 (depicted for $n_1 < n_2$, e.g. if light is refracted at an air-glass interface). S- and p-polarization of the incident light are indicated.

The angle of refraction in medium 2, Θ_2, is determined by the refractive indices of the different media and the angle of incidence Θ_1 according to Snell's law:

$$n_1 \sin \Theta_1 = n_2 \sin \Theta_2$$

For incident angles, Θ_1, larger than a critical angle $\Theta_{critical}$ total internal reflection into medium 1 occurs, which means that no light is transmitted into medium 2. This critical angle can be determined using Snell's law to be

$$\Theta_{critical} = \arcsin\left(\frac{n_2 \sin \Theta_2}{n_1}\right) = \arcsin\left(n \sin \Theta_2\right), \tag{2.4}$$

where for simplicity the ratio between the refractive indices has been simplified to $n = n_2/n_1$, which is sometimes referred to as relative refractive index of the interface between medium 1 and 2.

If light travels from an optically thicker medium into an optically thinner medium ($n_1 > n_2$), as it is the case for light travelling in a glass substrate encountering a glass-air interface, total internal reflection occurs as soon as the angle of refraction, Θ_2, reaches an angle of at least 90°.

The fraction of light being reflected back into medium 1 at the interface depends in addition to the incident angle Θ_1 and the relative refractive index of the interface n on the polarization of the incident light, which means the orientation of the electric field with respect to the incident plane as it is indicated in figure 2.2 by black arrows. The parallel (p) and perpendicular (s) polarized fractions of reflected light are described by Fresnel's equations in combination with Snell's law and trigonometric identities:

$$R_p\left(\Theta_1\right) = \left(\frac{\tan\left(\Theta_1 - \Theta_2\right)}{\tan\left(\Theta_1 + \Theta_2\right)}\right)^2 = \left(\frac{n^2\cos\Theta_1 - \sqrt{n^2 - \sin^2\Theta_1}}{n^2\cos\Theta_1 + \sqrt{n^2 - \sin^2\Theta_1}}\right)^2$$

for parallel (p) polarization and

$$R_s\left(\Theta_1\right) = \left(\frac{\sin\left(\Theta_1 - \Theta_2\right)}{\sin\left(\Theta_1 + \Theta_2\right)}\right)^2 = \left(\frac{\cos\Theta_1 - \sqrt{n^2 - \sin^2\Theta_1}}{\cos\Theta_1 + \sqrt{n^2 - \sin^2\Theta_1}}\right)^2$$

for perpendicular (s) polarization, respectively. In unpolarized light both polarizations contribute equally. In case of unpolarized light, as it is the case for spectral irradiance on a solar cell, the total angular reflectance is given by the average of the two polarizations:

$$R\left(\Theta_1\right) = \frac{1}{2}\left[R_p\left(\Theta_1\right) + R_s\left(\Theta_1\right)\right]. \tag{2.5}$$

Under oblique incidence p- and s-polarized fractions of light are reflected in different proportions resulting in partial polarization of the reflected and transmitted light fractions. At normal incidence $R_p\left(\Theta_1 = 0\right) = R_s(0) = R(0)$ holds and the equations for angular reflectance reduce to [61, 69, 70]:

$$R(0) = \left(\frac{n-1}{n+1}\right)^2 = \left|\frac{n_2 - n_1}{n_2 + n_1}\right|^2. \tag{2.6}$$

In a real solar cell device, reflection can occur at various interfaces before reaching the absorber layer. In the solar cell design used in this thesis (chapter 3.1) light enters the solar cell through a glass substrate (with a refractive index of $n_2 \approx 1.52$ [71]) from air ($n_1 = 1$). About 4 % of the incident light is lost by reflection at the air-glass interface. Reflection losses at the air-glass interface are illustrated by case i in figure 2.3. Additional reflection losses of incident light occur at the interlayer system consisting of sputtered silicon oxide, a textured sol-gel layer and another SiO_x

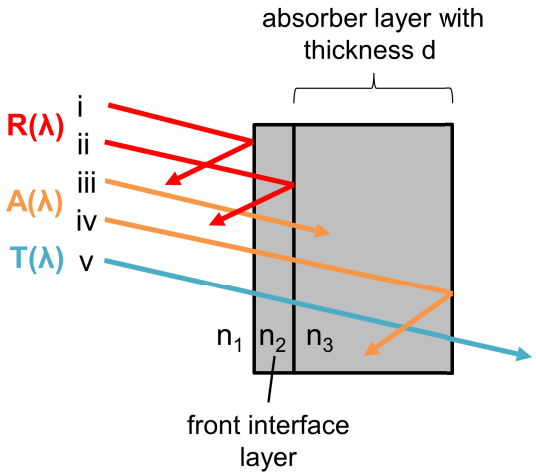


Figure 2.3: Schematic of an optical device with finite thickness d and front interface layer with refractive indices n_3 and n_2, respectively. Light encountering an optical device from a medium with refractive index n_1 can (i) be reflected at the air-front interface, (ii) be reflected at the front-absorber layer interface, (iii) be absorbed in the absorber layer, (iv) be reflected at the rear side of the absorber layer and subsequently be absorbed, or (v) be transmitted.

layer or a SiN_x / SiO_x layer stack prior to the silicon absorber layer. In figure 2.3 these cases are summarized by case ii. A numerical study about reflection at this interlayer system can be found in [72]. These reflected parts of incident light are summarized as reflectance $R(\lambda)$ and constitute the reflection loss. Hence, only the fraction $1 - R(\lambda)$ of incident light is able to reach the absorber layer and contribute to current generation (equation 2.3).

Another optical loss mechanism is non-absorption of photons with sub-band gap energies. These photons are transmitted at the rear side of the absorber layer and are summarized as transmittance $T(\lambda)$. In thin-film solar cells non-absorption of incident photons is one of the major loss mechanisms [43, 67]. In summary, light encountering an optical device can (i) be reflected at the air-front interface, (ii) be reflected at the front-absorber layer interface, (iii) be absorbed in the absorber layer, (iv) be reflected at the rear side of the absorber layer and subsequently be absorbed, or (v) be transmitted. These cases are schematically illustrated in figure 2.3.

In short, light interacting with a semiconductor absorber layer can either be absorbed $A(\lambda)$ in the active layer or it is lost due to reflection $R(\lambda)$ or transmission $T(\lambda)$. This relationship is often described by

$$A(\lambda) = 1 - R(\lambda) - T(\lambda) \tag{2.7}$$

and is visualized in figure 3.4 (b) in the next chapter.

Assuming that every photon absorbed contributes to current generation in the absorber layer a maximum achievable short-circuit current density ($j_{sc,max}$) can be calculated:

$$j_{sc,max} = q \int_{280nm}^{1100nm} \frac{S(\lambda)}{h\nu} A(\lambda) d\lambda \tag{2.8}$$

with q the elementary charge, $h\nu$ the photon energy, $S(\lambda)$ the spectral intensity under AM1.5g and $A(\lambda)$ the absorption.

In a real solar cell device the actual achievable short-circuit current density (j_{sc}, equation 3.2) is lower because of electronic losses (chapter 2.2.1) [67]. Maximum achievable short-circuit current densities are a common figure of merit for comparing absorptance of different samples because they allow for a comparison independent of the solar cell processing technology and the cell area. The $j_{sc,max}$ serves as an upper limit for short-circuit current densities reachable in a respective solar cell device.

2.1.2 Light Trapping

In order to minimize optical losses (chapter 2.1.1) and enhance the path length (figure 2.1) of incident light within the silicon absorber layer without increasing the absorber layer thickness, various light trapping schemes at different interfaces are available. Besides, the different penetration depths of different wavelengths demand for individual light trapping geometries at each interface [29, 73–77]. A simplified optical device is sketched in figure 2.3. In the following it is assumed that light incidences from air ($n_1 = 1$) onto a crystalline silicon absorber layer ($n_3 = 3.4$) without front interface layer. Thus, optical losses can occur by reflection losses at the front (in figure 2.3 illustrated by red arrows, since no front interface layer is present case ii equals to case i) and by transmission losses at the rear side of the optical device (in figure 2.3 illustrated by a blue arrow, case v).

First, reflection losses at the front interface are addressed in order to enhance absorptance of light with wavelengths shorter than the penetration depth (case iii in figure 2.3). In principal, there are three approaches to reduce front reflection. Most light trapping methods combine at least two of these concepts [60, 67, 78, 79]:

- First, an optically thick layer with a refractive index lower than that of silicon can be applied to the front surface making use of a **graded index effect** [80, 81]. In the simplified optical device shown in figure 2.3 this corresponds to introducing the depicted front interface layer with $n_1 < n_2 < n_3$. An example for an optically thick layer are glass substrates with a refractive index of $n_2 \approx 1.52$ reducing reflection at the air-glass interface according to equation 2.6 to about 4 % (case i in figure 2.3) plus 15 % reflection loss at the glass-silicon interface (case ii in figure 2.3) in comparison to 35 % reflection loss for a direct air-silicon interface.

- Second, **single or multi-layer anti-reflection coatings** [78, 82–85] with an optical thickness corresponding to $\lambda/4$ can be applied allowing for total internal reflection at one particular wavelength. In this thesis, an interlayer stack containing 70 nm SiN_x ($n_{sinx} \approx 2.0$) is applied between the glass substrate and the silicon absorber layer, which is, among other properties, a state-of-the-art anti-reflection coating for LPC silicon thin-film solar cells on glass [86–88].

- Last, **surface and interface textures** can be used minimizing reflection losses at the air-glass and glass-silicon interface. In figure 2.3 the latter corresponds to roughening the interface between the front interface layer with n_2 and the absorber layer with n_3 in order to reduce case ii reflection losses. Rough surfaces can either be statistically or periodically textured. A perfect statistical texture is called Lambertian reflective [22, 89, 90]. Such textures cause a perfect randomization of the light path inside the absorber layer with an isotropic energy distribution. Two examples for statistically textured front interfaces are etched ZnO:Al layers [22, 59, 91–93] and black silicon [94]. Similar absorption enhancements can be achieved by periodic textured surfaces with a feature size larger than the wavelength of incident light. Such textures are called geometric reflective [80, 95]. For a narrow wavelength range it has been demonstrated that geometric light trapping structures can outperform random light trapping structures at certain angles of incidence. Nonetheless, so far no broad band enhancement under isotropic illumination could be demonstrated [73, 79, 96–98].

Since short-wavelengths light is absorbed during its first pass through the cell, a high back reflectance at the rear side of the absorber layer is only required for light with wavelengths longer than the penetration depth (case iv in figure 2.3) in order to avoid transmission losses (case v in figure 2.3). A well-designed light trapping scheme allows for a large number of reflections within the cell raising the probability

for absorption of long wavelengths light despite the limited absorber layer thickness and the declining absorption coefficient of silicon [figure 2.1 (a)]. Two possibilities to avoid transmission and to enhance reflection at the rear-side of a silicon thin-film absorber layer in order to rise the probability for absorption are:

- The **rear side** of silicon can be **textured** with pyramids produced by anisotropic wet chemical etching in an etching solution containing KOH [43, 99]. The amount of silicon being removed correlates with the crystal orientation at the surface, e.g. surface atoms of less dense packed {100}-planes are preferentially etched compared to surface atoms of the closed-packed {111}-planes resulting in etch pyramids characteristic for the underlying crystal orientation. Figure 2.4 displays a (a) silicon unit cell with these two lattice planes highlighted, (b) KOH etched rear side of a planar 15 µm thick LPC silicon absorber layer as well as (c) etch results achieved on different grain orientations.

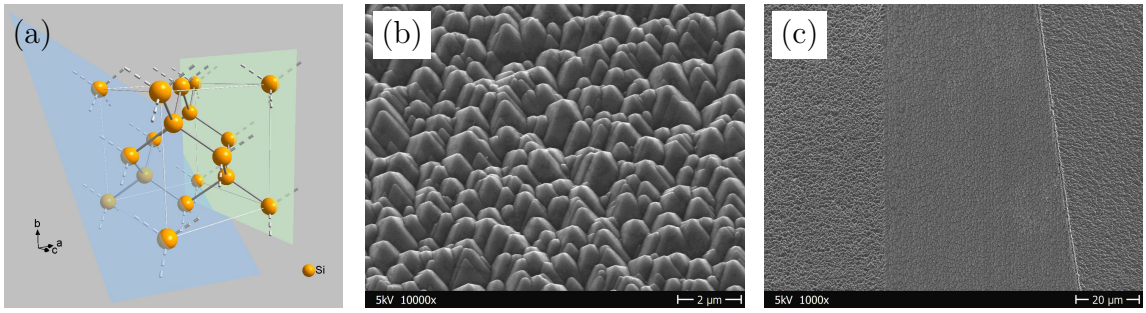


Figure 2.4: (a) Unit cell of crystalline silicon with highlighted {100}-plane (green) and closed-packed {111}-plane (blue). Connecting bonds between atoms are drawn in gray and broken off bonds are dashed. Atoms at the edges of the unit cell are connected with white lines for clarity. This picture was created using the software package diamond version 3 [100] with data taken from [101]. (b) SEM top view image tilted by 30° of KOH etched rear side of a 15 µm thick LPC silicon absorber layer. (c) SEM image depicting etch results achieved on different grain orientations.

  Typical feature sizes of KOH etched pyramids in LPC silicon are in the range of micrometers in width and depth, which are well suited for scattering long-wavelength light reaching the rear side of the silicon absorber layer without being absorbed in the first path. An alternative to etch pyramids are diffraction gratings [77, 102–104].

- Alternatively, or additionally, **flat or textured dielectric and metallic reflectors** [104, 105] can be applied to the rear side of the absorber layer. However, metal and dielectric reflectors suffer from metallic absorption losses at each reflection enhancing the optical loss by parasitic absorption. This optical loss enhancement becomes more severe with increasing metal area, e.g.

by texturing, a decreasing absorber layer thickness or an increasing number of passes [104]. Typical dielectric reflectors are white paints [106, 107] or silver layers [30, 108, 109].

The upper achievable or **theoretical limit** for optical path length enhancement at a certain wavelength in a semiconductor layer with thickness d was derived by Yablonovitch et al. to be $\boldsymbol{4n^2d}$ assuming no reflection losses at the front side, no transmission losses at the rear side and a Lambertian scatterer as front side texture of a weak-absorbing semiconductor [29, 110, 111]. One possibility to surpass the $4n^2d$ benchmark, which is commonly referred to as Yablonovitch limit, is to use texture feature sizes smaller than or in the range of the wavelength of incident light such that the wave nature of light becomes vital. To fulfill this requirement in case of a periodic texture, the texture period needs to be smaller than the incident wavelength. In this case incident light is rather diffracted than scattered and can couple into modes of different diffraction order within the absorber layer [25, 79, 112]. Typical examples are moth eye structures [113] and photonic crystals [27, 98, 114]. The periodic nano-textures applied in this thesis at the glass-silicon interface belong to this category as well.

In terms of maximum achievable short-circuit current density ($j_{sc,max}$) for a silicon absorber layer with a thickness of 10 µm 28.3 mA cm^{-2} can be reached with a planar stack without light trapping scheme. Applying a perfect Lambertian light trapping scheme can enhance the maximum photogenerated current density to 39.7 mA cm^{-2} and with an optimum geometrical light trapping up to 41.0 mA cm^{-2} can be reached for the same absorber layer thickness [67]. The upper limit for absorption enhancement with feature sizes in the range of the wavelengths of incident light depends on many factors like the absorber layer thickness and the texture geometry. In case of a thick absorber layer there is a continuum of modes available to which incident light can couple. If, in addition, the structure period is larger than the incident wavelength, the maximum light path enhancement approaches the Yablonovitch limit. In case of a thin absorber layer only guided modes with discrete states are accessible and with a structure period of slightly smaller than the wavelength the maximum light path enhancement can exceed the Yablonovitch limit at normal incidence by a factor of π for a square lattice and by a factor of $2\pi/\sqrt{3}$ for a triangular lattice, respectively. The corresponding calculation of the maximum light path enhancement under consideration of the electromagnetic light properties using a rigorous electromagnetic leaky mode formalism can be found in literature [98].

In summary, in order to reduce optical losses to a minimum and tap the full efficiency potential of crystalline silicon thin-film solar cells: first, front surface reflection has

to be reduced, ideally to zero, second, back surface reflection has to be enhanced, ideally to unity, and, third, an efficient light trapping scheme has to be implemented at the front of the absorber layer increasing the path length of incident light in the cell.

The samples featured in this thesis address these challenges by combining parts or even all approaches introduced. First, front reflection is minimized by applying a glass substrate, a SiN_x anti-reflection coating and a substrate-silicon interface texture (chapters 5.1 and 5.2). Moreover, the 4 % air-glass reflection can be further minimized by attaching an anti-reflective layer [21, 42, 80] at this interface (chapter 5.3). Second, to enhance reflection at the rear side pyramidal textures and white paint pack reflectors are tested in addition to the double-sided textured absorber layers (chapter 5.3). Third, the development of an efficient light trapping texture with feature sizes in the wavelength range of incident light allowing for an increased incoupling of light into the absorber layer whilst maintaining the silicon material quality is the objective of this thesis.

2.2 Electronic Properties of Silicon

In a real silicon crystal various defects and combinations of defects can be present [68, 70, 115–119]:

- **0-dimensional** defects are disturbances of the crystal symmetry at atomic size and often called point defects. One distinguishes between intrinsic point defects, which can be formed by vacancies or self-interstitials, and extrinsic point defects, which can be formed by impurity atoms on lattice or interstitial sites. At elevated temperatures point defects become mobile and play a crucial role for enabling solid state diffusion, e.g. of dopant atoms into the bulk material.

- **1-dimensional** defects are usually called dislocations or line defects. Dislocations can occur in various forms like loops or screws. The extension of a dislocation is quantified by its Burgers vector b, describing the disturbance of the crystal lattice containing the dislocation in comparison to a perfect crystal lattice. For energetic reasons b often corresponds to the shortest translation vector of the lattice, which corresponds to $a/2\,\{110\}$ in fcc lattices like silicon.

- **2-dimensional** defects disturb the crystal symmetry over a randomly curved area occurring as stacking faults or grain boundaries. Stacking faults can be

caused by vacancy or interstitial agglomerations (partial dislocation or Frenkel dislocation) or by intrinsic stacking faults (Shockley dislocations) and are characterized by Burgers vectors b, which do not correspond to a translational vector of the lattice. Defects caused by lattice mismatches between neighboring grains are called grain boundaries. In dependency on the energetic disturbance compared to a perfect crystal lattice, grain boundaries are characterized by Σ-values. $\Sigma - 3$ boundaries are the energetic most favorable grain boundaries in fcc lattices, because the tetrahedral bonding between neighboring atoms is preserved. $\Sigma - 3$ grain boundaries, which often occur as twin boundaries, are the most frequently encountered grain boundaries in silicon.

- **3-dimensional** defects include precipitates, which are usually formed by impurity atoms, and agglomerates of vacancies forming voids. In fcc lattices special 3-dimensional defects like stacking fault tetrahedra can occur.

In poly-crystalline silicon, like LPC silicon, intra-grain defects, like twin boundaries, stacking faults, point defects and dislocations leaving unsaturated or dangling bonds, and grain boundary defects with a high number of dangling bonds and segregation of point defects are the most important defect types [118, 120, 121].

In addition to these structural properties, defects have an impact on the electronic properties by introducing energy states in the band structure. This effect can be used for doping the semiconductor layer by introducing suitable foreign atoms to the crystal lattice. At elevated temperatures these foreign atoms can become ionized and additional allowed localized energy levels are introduced close to the valence band maximum or conduction band minimum, respectively, and the relative concentration of electrons in the conduction band and holes in the valence band can be influenced resulting in an increased effective density of states.

By illumination or current injection generating excess electron-hole pairs, a semiconductor can be forced out of its thermal equilibrium, forming a stationary equilibrium, with raised carrier concentrations of electrons (n) and holes (p)

$$n = n_0 + \Delta n = N_C \exp\left(-\frac{1}{k_B T}\left(E_C - E_{F,n}\right)\right)$$
$$p = p_0 + \Delta p = N_V \exp\left(+\frac{1}{k_B T}\left(E_V - E_{F,p}\right)\right),$$

where the index 0 denotes the thermal equilibrium carrier concentration and Δ denotes the generated excess carriers. N_C and N_V denote the effective density of

states and E_C and E_V the band edge energies of the conduction band (C) and valence (V) band, respectively. E_F is the quasi-Fermi energy of electrons (n) and holes (p) [61].

2.2.1 Electronic Loss Mechanisms

After terminating the source generating excess carriers, excess electrons and holes tend to restore their equilibrium concentrations by recombining and, thereby, eliminating an electron-hole-pair, with a recombination rate U of

$$U\left(\Delta n\right) = -\frac{\delta \Delta n}{\delta t}. \tag{2.9}$$

Recombination processes can be severely enhanced if allowed energy states in the band gap are present acting as recombination centers as it is, most importantly, caused by unsaturated silicon bonds and impurity atoms in silicon solar cells. In contrast to the shallow energy levels of dopant atoms, energy levels of impurity atoms are located further within the band gap. In addition to recombination via intra-band gap trap states, recombination can occur as radiative and Auger recombination. In the following these types of recombination are described (If not stated otherwise, the given equations refer to n-type semiconductors.) [61, 63, 67, 119, 122, 123]:

- Recombination via a single level trap or **Shockley-Read-Hall (SRH) recombination** takes place via a defect state located at energy E_{trap} within the band gap. The position of the trap energy within the band gap depends on the impurity atom or crystallographic defect type and can be influenced by specific growth or processing conditions. Trap energy levels close to the band edges are less harmful than trap energy levels close to the middle of the band gap, because electrons and holes on trap levels close to the band edges experience a high probability to be re-emitted to the conduction or valence band, respectively. SRH recombination, especially via dangling bonds [121] is the dominant recombination process in indirect semiconductors like silicon. Calculations of Steffens *et al.* [120] identified recombination via intra-grain dislocations as dominant recombination process in LPC silicon limiting the open-circuit voltage (equation 2.14).
- **Band-to-band recombination** is a radiative recombination process, in which the energy of the recombining electron-hole pair is transferred to a photon, which is emitted with an energy similar to the band gap energy, and, in case

of an indirect semiconductor like silicon, to a phonon. This process corresponds to the inverse of the carrier generation process based on optical absorption and can be analyzed as photoluminescence. Compared to a direct semiconductor this radiation process is rather unlikely in indirect semiconductors like silicon because of the necessity of a phonon contribution. Radiative recombination is an intrinsic or fundamental recombination process and, hence, unavoidable. The radiative recombination rate can be minimized via photon recycling, i.e. by re-absorption of an emitted photon.

- In an **Auger recombination** process the excess energy is given to another carrier instead of to an emitted photon, as it is the case for radiative recombination. This carrier subsequently relaxes thermally transferring the extra energy and momentum to phonons. Like radiative recombination Auger recombination is an unavoidable intrinsic recombination process. Due to its quadratic dependency on the carrier concentration Auger recombination is a crucial recombination process especially under high-injection conditions as well as in highly doped semiconductors with doping concentrations between about $10^{17}\,\mathrm{cm}^{-3}$ and $10^{18}\,\mathrm{cm}^{-3}$, which is higher than the typical doping concentration in LPC silicon solar cells [124].

These recombination processes occur in parallel. Despite it is unlikely, more than one trap can be involved in a single SRH recombination event. The total recombination rate in a semiconductor is given by

$$U_{total} = \left[\sum_{SRH,i} U_{SRH,i}\right] + U_{rad} + U_{Auger}.$$

Accordingly, the carrier lifetime (τ) in the semiconductor bulk, which is defined as

$$\tau_{bulk} = \frac{\Delta n}{U_{total}} \tag{2.10}$$

can be calculated:

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}}.$$

At the front and rear surface of the absorber layer as well as at grain boundaries or more general at interfaces between two dissimilar materials, a high concentration of defects occurs because of the abrupt termination of the crystal lattice. The net recombination rate at grain boundaries and at surfaces is calculated according to the SRH recombination. Due to the high number of trap states often forming a

continuum of states within the band gap, the net surface recombination rate is calculated by integrating over all energy states between the valence and conduction band. The net surface recombination rate, U_s, can be used to calculate the surface recombination velocity via

$$S(n,p) = \frac{U_s(n_s, p_s)}{\Delta n_s}, \tag{2.11}$$

where Δn_s is the excess carrier concentration at the surface. The carrier lifetime for an absorber layer with a thickness d is then given by an effective (index *eff*) carrier lifetime:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{S_{front} + S_{rear}}{d} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_s}$$

[61, 63, 119, 122, 125].

While the bulk recombination rates are calculated for a unit volume, the surface recombination rate is calculated per unit area [63]. Following as consequence, if a textured substrate is used, surface recombination is expected to increase conditioned by the increased surface area compared to a respective planar reference.

Recombination via unsaturated silicon bonds can be minimized in the bulk by hydrogen passivation [60, 126] forming a Si-H bond and at the surface by growing an oxide forming a Si-O bond, respectively. Both passivation mechanisms shift the electronic defect states out of the bandgap by forming bonding and anti-bonding states in the valence and conduction band (chemical passivation) [67]. Another possibility to reduce the surface recombination velocity is to reduce one carrier type in order to retard recombination (field effect passivation) as it can be achieved using silicon oxide [127] and silicon nitride [128] passivation layers. Silicon nitride provides passivation by reducing the interface state density in combination with a large concentration of positive surface charges due to the formation of nitrogen vacancy centers, which repel holes from the surface [67]. In the solar cell design used in this thesis the silicon front surface is terminated by a silicon oxide interlayer followed by a silicon nitride interlayer. Under standard conditions the excess carrier concentration in silicon solar cells is in the range of $1 \times 10^{12}\,\mathrm{cm}^{-3}$ to $5 \times 10^{14}\,\mathrm{cm}^{-3}$. In this excess carrier concentration regime the silicon oxide-silicon surface recombination velocity in n-type silicon is about one order of magnitude lower than in p-type silicon [129]. Therefore, only n-type silicon absorber layers have been investigated in the scope of this thesis.

2.2.2 Solar Cell Characteristics

As for any electronic device the operation principle of a solar cell can be described by an equivalent circuit diagram. The equivalent circuit of a solar cell is a diode. In case of an ideal solar cell the corresponding jV curve is only determined by the diffusion current. The material properties of the diode are described by the saturation current j_0 [61, 63, 119, 130, 131]:

$$j_0 = \frac{qD_n n_0}{L_n} + \frac{qD_p p_0}{L_p},$$

where D is the diffusion coefficient and $L = \sqrt{D \cdot \tau}$ the diffusion length of electrons n and holes p, respectively, and n_0 and p_0 are the minority carrier concentration in thermal equilibrium.

If the solar cell is illuminated, a current source is added to the equivalent circuit in parallel to the diode, where the photo current j_{ph} is generated. In this case the relationship between current density and voltage is given by:

$$j_{light,ideal}(U) = j_0 \left[\exp\left(\frac{qU}{kT}\right) - 1\right] - j_{ph}. \tag{2.12}$$

While an ideal solar cell can be fully described by an equivalent circuit consisting of these parameters, the performance of a real solar cell is affected by recombination losses, which are added to the equivalent circuit as short-circuits or shunts. Losses at the metal contacts, at the metal-semiconductor interface, at interfaces of different semiconductor layers and within the semiconductor are depicted as a series resistance R_s. Losses due to short-circuits, defects or grain boundaries as well as doping inhomogeneities, which bypass the p-n junction, are considered as parallel or shunt resistance R_p. For a real solar cell the relationship between current density and voltage is given by:

$$j_{light}(U) = j_0 \left[\exp\left(\frac{q\left(U - j_{light}R_s\right)}{fkT}\right) - 1\right] + \frac{U - j_{light}R_s}{R_p} - j_{ph} \tag{2.13}$$

The equivalent circuit of this so called one diode model is depicted in figure 2.5.

These equations describing the relationship between the current density and the voltage are implicit equations and can only be numerically solved resulting in a current density–voltage (jV) curve being characteristic for the solar cell.

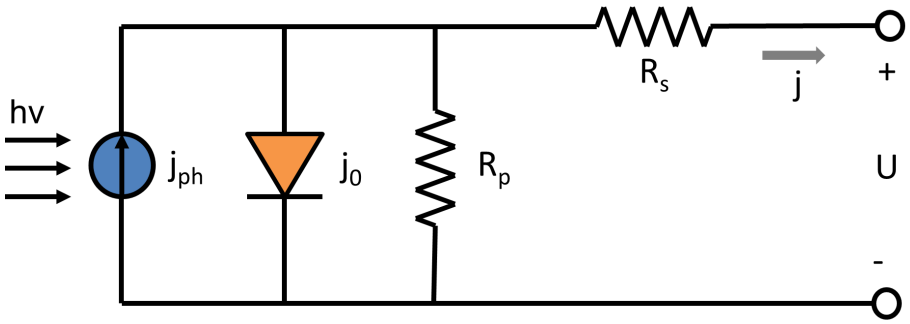


Figure 2.5: Equivalent circuit of a non-ideal solar cell in the one diode model. j_{ph} symbolizes the photocurrent generated by incident light ($h\nu$). The diode is characterized by the saturation current (j_0). Both contribute to the total current flow (j). Shunt (R_s) and parallel (R_p) resistances are added to the equivalent circuit at appropriate positions. In between the contacts, denoted with + and -, the circuit voltage (U) can be extracted.

A typical jV curve and power (P)-voltage curve of a silicon thin-film solar cell are depicted in figure 2.6.

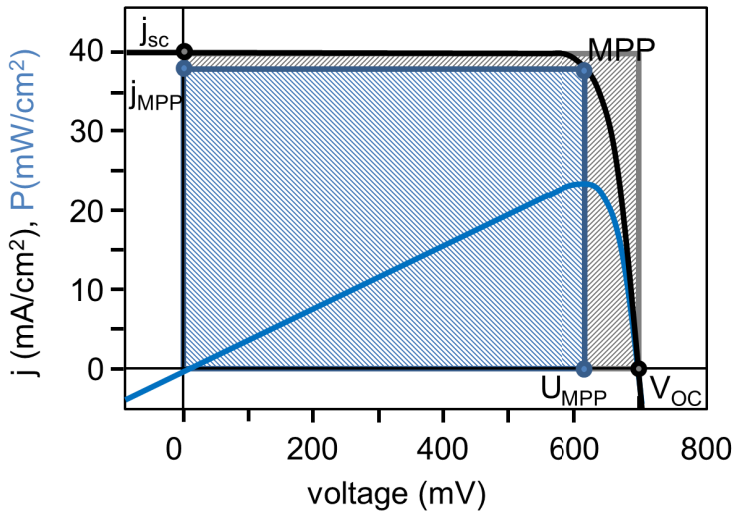


Figure 2.6: jV-curve (black) and $P-V$-curve (blue) of a silicon solar cell. The maximum power point (MPP), the current (j_{MPP}) and voltage (U_{MPP}) at the MPP, the short-circuit current density (j_{sc}) and the open-circuit voltage (V_{oc}) are denoted. The area determined by $j_{MPP} \cdot U_{MPP}$ is highlighted in blue while the area determined by $j_{sc} \cdot V_{oc}$ is shaded in grey.

The jV curve of a solar cell under illumination can be used to determine or calculate all crucial solar cell parameters. These parameters are [61, 63, 119, 130, 131]:

- The **open-circuit voltage (V_{oc})** is the voltage at the solar cell contacts if no current is flowing in the solar cell ($j(U = V_{oc}) = 0$). From equation 2.12 for an ideal solar cell:

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{j_{ph}}{j_0} + 1\right) \tag{2.14}$$

  is obtained for the open-circuit voltage. Furthermore, the V_{oc} is determined by the splitting of the Fermi levels at both contacts, which in turn is limited by the splitting of the quasi-Fermi levels in the absorber layer. The latter is called implied V_{oc} (V_{oc}^{imp}):

$$V_{oc}^{imp} = \frac{1}{q}\Delta E_F = \frac{k_B T}{q} \ln\left(\frac{(n_0 + \Delta n)\,(p_0 + \Delta p)}{n_i^2}\right). \tag{2.15}$$

- The **short-circuit current density (j_{sc})** describes the current produced by the solar cell in case there is not voltage applied ($U(j = j_{sc}) = 0$). Ideally the short-circuit current density is equal to the light generated current density $j_{sc} = j_{ph}$. For a real solar cell under short-circuit conditions $R_p \gg R_s$ holds and an expression for the short-circuit current density can be derived from equation 2.13:

$$j_{sc}(U = 0) = j_0 \exp\left[\left(\frac{q j_{sc} R_s}{f k_B T} - 1\right)\right] - j_{ph}. \tag{2.16}$$

- The **fill factor (FF)** is a measure for the deviation from an ideal solar cell. An ideal solar cell would result in a rectangular jV curve with an area of $j_{sc} \cdot V_{oc}$. In figure 2.6 this area is shaded in gray To characterize a real solar cell the current and voltage at the maximum power point (MPP) have been chosen. In figure 2.6 this area is shaded in blue. The fill factor can then be derived by the ratio of the real to the ideal area:

$$FF = \frac{j_{MPP} \cdot U_{MPP}}{j_{sc} \cdot V_{oc}} \tag{2.17}$$

- The **efficiency** η states how much of the power density provided by incident radiation P_{in} (at standard test conditions $P_{in} = 100\,\mathrm{mW\,cm^{-3}}, T = 25\,^{\circ}\mathrm{C}$, AM1.5g spectrum) the solar cell can at maximum convert into a usable power density P_{MPP}:

$$\eta = \frac{P_{MPP}}{P_{in}} = \frac{j_{MPP} \cdot U_{MPP}}{P_{in}} = \frac{j_{sc} \cdot V_{oc} \cdot FF}{P_{in}} \tag{2.18}$$

The main impact of parallel resistance (illustrated as R_p in figure 2.5), which is mainly determined by crystallographic defects in the absorber layer, is to reduce the open-circuit voltage (equation 2.14). Furthermore, the open-circuit voltage depends on the excess carrier lifetime (equation 2.15). The latter is directly related to recombination processes in the bulk and at surfaces as well as to the minority carrier lifetime (equations 2.9, 2.10 and 2.11). For these reasons, the open-circuit voltage of a solar cell is not only a vital cell parameter but can also be used to qualitatively characterize the material quality of the measured cell.
The solar cell devices measured in this thesis exhibit a high series resistance (illustrated as R_s in figure 2.5) of typically 200 Ω to 2000 Ω [17]. This is owed to the fast and simplified production process of the contacting scheme (chapter 3.1). A high series resistance mainly reduces the fill factor (equation 2.17). Besides, excessively high values can also negatively affect the short-circuit current density (equation 2.16). Nonetheless, the contacting scheme applied allows for determination of the vital solar cell parameters open-circuit voltage and short-circuit current density (chapter 3.2). Based on these two parameters, a jV-curve and, hence, a solar cell efficiency (equation 2.18) can be calculated. The difference between measured and calculated jV-curves is highlighted in figure 2.7.

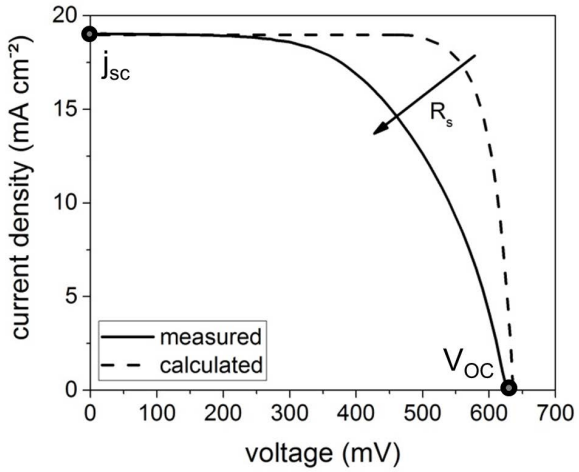


Figure 2.7: jV-characteristic of an 8 µm thick planar LPC silicon thin-film solar cell highlighting the differences between measured (solid) and calculated (dashed) jV-curves. The influence of the cell's series resistance (R_s) is indicated.

Since these calculations are not affected by the cells series resistance, the jV-curve, the determined fill factor as well as the calculated efficiency are idealized and serve as an upper achievable limit.

3 Methods and Characterization

This chapter introduces relevant methods for sample preparation (subchapter 3.1) and sample characterization (subchapter 3.2). The preparation methods include textured substrates, silicon absorber layers and solar cell devices. The characterization methods comprise morphological, optical, electrical as well as material quality analysis techniques.

3.1 Sample Preparation

Substrate Preparation

0.7 mm and 1.1 mm thick 5 cm x 5 cm Corning Eagle XG^{TM} glasses were used as glass substrates. All substrates were coated with a 250 nm SiO_x layer acting as diffusion barrier against substrate impurities. For nano-structuring the glass substrates were spin-coated with a high temperature stable, UV-curable sol-gel resist. Sol-gels based on silicon alcoxides providing high-temperature stability were applied, which have been developed and produced by SCHOTT, Mainz, Germany [55] and PHILIPS, Eindhoven, Netherlands [56]. A technology suitable for transferring nano-textures to glass substrates is Nanoimprint Lithography (NIL) [44, 45, 107, 132, 133], which is applied in various fields in industry and science, like electronics, photonics or photovoltaics [23, 47, 53, 134–141]. Moreover, UV based nanoimprint lithography (UV-NIL) in combination with a high-temperature stable sol-gel resists has proven its suitability for implementing periodic nano-textures in liquid phase crystallized (LPC) silicon devices [46, 57, 59]. The main advantage of NIL technologies is that a once produced master structure can be transferred to a large number of substrates. The costs of producing the master structure have to be expended only once. Master structures newly introduced into the LPC process are a hexagonal 750 nm pitched pillar structure as well as hexagonal 500 nm and 750 nm pitched sinusoidal structures. In case of the pillar structure the master structure was produced by electron beam lithography [52]. The master structures of the sinusoidal nano-textures were

fabricated at Fraunhofer ISE, Freiburg, Germany by interference lithography [142]. The master structure is transferred onto the sol-gel coated glass substrates with the aid of a polydimethylsiloxan (PDMS) mold [143]. The applied UV-NIL process is schematically depicted in figure 3.1.

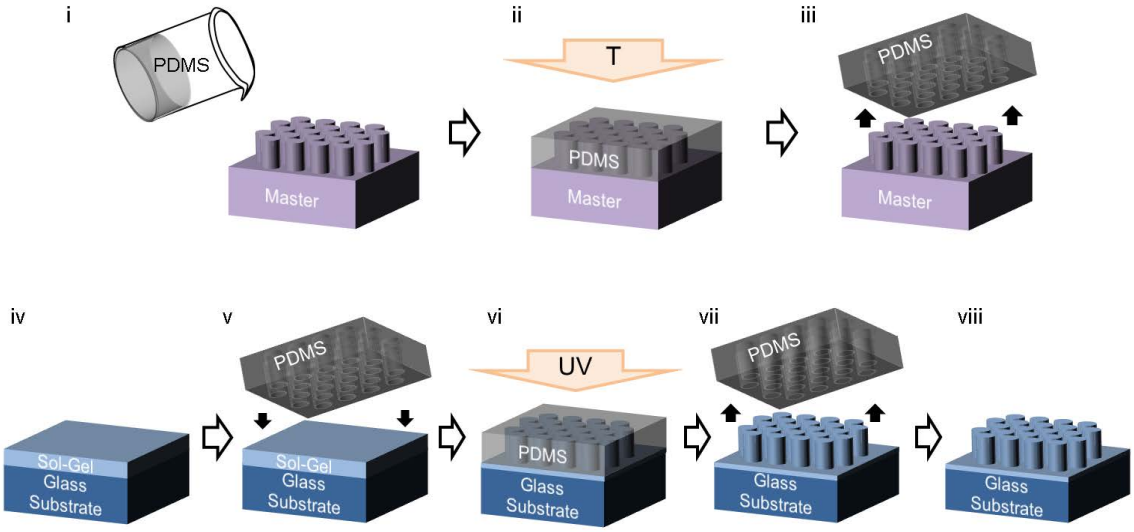


Figure 3.1: Schematic of the UV-NIL process. In the first row (step i-iii) stamp fabrication and in the second row (step iv-viii) nano-texturing of glass substrates is depicted using a hexagonal pillar structure as example.

To produce a PDMS mold containing the negative of the master structure, commercially available liquid PDMS precursor material has been mixed with a suitable catalyst in a ratio of 9 : 1. The PDMS mixture has been degassed, poured over the master structure (step i) and thermally (T) hardened for 20 min at 70 °C (step ii). After removal of the solidified mold (step iii) the master is ready for reuse. The sol-gel has been spin-coated onto the glass substrate in a two-step process consisting of spin coating for 10 s at 1000 rpm to form a layer of sol-gel adhering to the glass substrate and for 30 s at 500 rpm forming the sol-gel bulk layer (step iv). The molds were rolled onto the sol-gel layers (step v). Due to capillary forces the sol-gel fills the mold structure. Subsequently, the sol-gel layers were UV-cured (UV) for 5 min and solidified into a structure determined by the PDMS mold (step vi). The two-step spin coating procedure results in a total sol-gel thickness of around 600 nm, in which up to 400 nm can be textured, typically, leaving a residual planar sol-gel layer of 200 nm thickness between the glass substrate and the sol-gel texture. After mold removal (step vii) a textured glass substrate is obtained (step viii). In order to remove organic solvents the glass substrate with the textured sol-gel layer underwent

a post-bake procedure of 8 min at 100 °C followed by a hard-bake procedure of 1 h at 600 °C. The hard-baking step reassures the removal of all organic ingredients and, hence, the high-temperature stability required for the LPC process featuring temperatures of over 1000 °C. During this temperature treatment the sol-gel densifies and, following as a consequence, shrinks. In case of the sol-gels used a shrinkage factors of about 30 % (Philips) and 40 % (SCHOTT) compared to the initial structure size after UV-curing were determined. This shrinkage factor in combination with different contact pressures when applying the PDMS mold to the spin-coated sol-gel resist enabled an easy procedure to tailor the feature size of the imprinted structures.

In case of the planar references all steps after depositing the 250 nm thick SiO_x diffusion barrier are omitted. The nano-textures produced in this thesis are compared to a high aspect ratio 2 µm pitched square lattice structure [58], to random textures with different feature sizes [144] and to a smooth 3-dimensional anti-reflective texture [145]. Descriptions of the respective production processes can be found in the references.

Absorber Preparation

The textured substrates as well as planar reference substrates were coated either with a SiO_x interlayer or a SiN_x / SiO_x interlayer stack (chapter 2.2.1 and References [129, 146, 147]). The silicon absorber layers were deposited by electron beam evaporation with a deposition rate of around 600 nm min^{-1} at a heater temperature of 600 °C resulting in a nano-crystalline silicon precursor layer of the desired thickness. Due to self-shadowing the deposited silicon grows more porous at substrate texture angles steeper than 30° than on planar substrate texture parts, as indicated by increased oxygen incooperation [148]. For doping a thin layer system consisting of 80 nm n-doped hydrogenated amorphous silicon and 10 nm intrinsic hydrogenated amorphous silicon were deposited on top of the nano-crystalline silicon precursor layers onto samples intended for electronic characterization. After silicon deposition the samples were capped with a 200 nm thick SiO_x layer [149]. In order to prevent cracking of the glass substrates and reduce thermal stress in the layers, the samples are preheated to 700 °C prior to crystallization. The silicon precursor layers are crystallized by scanning a line-shaped continuous-wave infrared laser emitting at 808 nm in air atmosphere over the samples with a scanning velocity of 3 mm s^{-1} [14, 88, 150]. During this liquid phase crystallization (LPC) process the electron beam deposited silicon precursor material is molten and recrystallizes into

a poly-crystalline silicon absorber layer with grain sizes of up to a few centimeters in length and a few millimeters in width [17, 18]. The SiO_x capping layer enhances wetting during crystallization. In case a textured substrate is used it allows to preserve the substrate texture at the top of the silicon absorber layer after liquid phase crystallization resulting in a double-sided textured silicon absorber layer [57]. After crystallization the samples undergo a rapid thermal heat treatment for 1 min at 950 °C in order to reduce stress and avoid cracks in the glass substrate caused by the rapid heat input during crystallization. By means of the described procedure, absorber layers with thicknesses between 5 µm and 30 µm were fabricated. If the absorber layers have been doped for further solar cell processing, these absorber layers exhibited a doping density between $5 \times 10^{16}\,\mathrm{cm}^{-3}$ and $1 \times 10^{17}\,\mathrm{cm}^{-3}$. At this stage the samples were ready for examination of the silicon absorber layer material quality as well as for optical characterization. These analysis techniques do not require a contacting scheme. A corresponding schematic of the sample stack is depicted in figure 3.2 (a).

Solar Cell Device Processing

To enable a characterization of the electronic properties the absorber layers have to be processed to solar cells featuring an electronic contacting scheme. In this thesis, a modified version of the lithography free and thereby fast to process contacting scheme developed by Haschke *et al.* [17], there denoted by "test structure", was applied. For this purpose the prepared absorber layers were exposed to a hydrogen plasma treatment at a pressure of 1 mbar for 30 min at 600 °C in order to passivate dangling bonds in the silicon bulk and at the buried SiO_x terminated substrate-silicon interface [126, 149, 151]. Subsequently, possible plasma induced damages at the silicon surface were removed by a wet chemical silicon etch solution consisting of HF, HNO_3 and H_3PO_4 for 60 s. The latter step thins the silicon absorber by about 500 nm compared to silicon thickness deposited by electron beam evaporation. The samples were cleaned with a standard RCA cleaning solution before depositing a p-type emitter consisting of 5 nm a-Si:H(i) and 10 nm of a-Si:H(p). An 80 nm thin ITO layer served as emitter contact. The emitter area was protected by round kapton dots with a diameter of 8 mm while processing the absorber layer contact. In order to reach the absorber layer for contacting, the ITO layer is removed by wet etching in 20 % HCl for 10 s. Subsequently, the emitter layer is removed using the silicon etch for 20 s. As absorber layer contact 30 nm Ti and 1000 nm Al are evaporated. Before characterization the kapton dots protecting the emitter area had to be removed.

Figure 3.2 (b) depicts a schematic of the described solar cell device. This device structure represents the solar cells being used for electronic characterization and electronic material quality analysis in this thesis. A corresponding photograph of a sinusoidal textured LPC solar cell device is depicted as well. Under certain angles of incident light the samples shimmer colorful due to the light scattering effect of the periodic nano-textures.

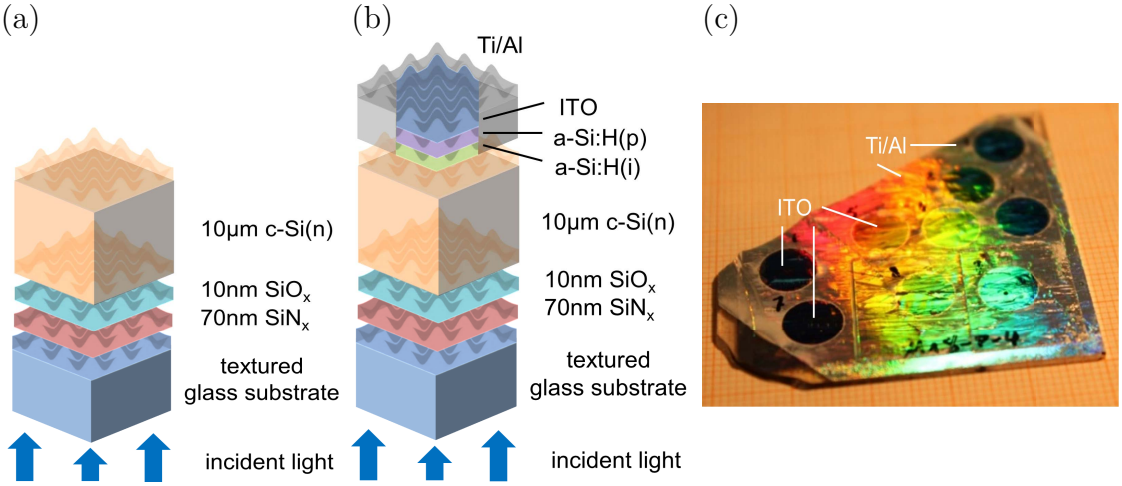


Figure 3.2: Schematics of (a) a LPC-Si absorber layer used for optical characterization and LPC silicon bulk material quality analysis as well as (b) a solar cell device structure used for electronic characterization and electronic material quality analysis. (c) Photograph of a sinusoidal textured LPC solar cell device as prepared for this thesis. The Ti/Al contacting the absorber layer and the ITO contacting the emitter layer, respectively have been partially denoted.

3.2 Sample Characterization

Surface Imaging

Atomic force microscopy (**AFM**) measurements were conducted for surface imaging at nanometer scale using a Park Systems XE-70 AFM equipped with high aspect ratio tips. A cantilever is scanned over the sample surface, adjusting its height according to its interactions with the sample surface. The alternating height of the cantilever is monitored and transferred into a topography image of the surface [70, 152]. As the interactions with the sample surface are based on long-range attractive (Van-der-Waals and capillary forces) and short-range repulsive (Pauli exclusion and Coulomb forces) interactions, conductivity of the sample surface is no prerequisite. Thus, AFM is a suitable method to determine the surface morphology of nanoimprint textured glass substrates. An example of an AFM image of a hexagonal sinusoidal

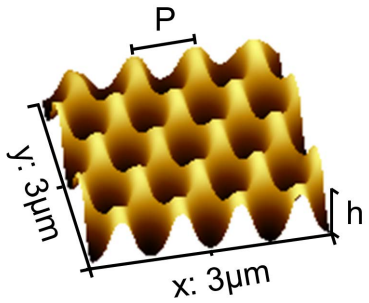


Figure 3.3: AFM image of a 750 nm pitched sinusoidal substrate texture, where the pitch (P) and height (h), which determine the aspect ratio (h/P), have been denoted.

textured glass substrate is depicted in figure 3.3. AFM topography images were used to extract pitches (P) and heights (h) in order to determine the aspect ratio (h/P) of the nanoimprinted textures on glass substrates. In the depicted case the structure's pitch is $P = 750\,\text{nm}$ and the height is $h = 150\,\text{nm}$ resulting in an aspect ratio of $h/P = 0.2$. Due to inhomogeneities in the manually conducted imprint process as well as AFM measurement errors, the AFM measurement inhomogeneity is assumed to be 20 nm.

Scanning Electron Microscopes (**SEM**) image surfaces of thin films by scanning the sample surface with a focused electron beam in high-vacuum. SEM top-view images have been measured with a HITACHI S-4100 SEM, in which the electron beam is generated by a cold field emission gun and accelerated up to 5 kV to 30 kV towards the sample surface in high-vacuum. For imaging the sample holder has been tilted to normal incidence or by 30° with respect to the incident electron beam. By elastic and inelastic scattering of the incident electron beam at surface near atoms secondary electrons are released and together with backscattered electrons they can be detected by means of a suitable detector. The amount of released secondary electrons depends on various parameters, e.g. the incidence angle of the electron beam and is a suitable parameter to be translated into an image contrast [153–155]. In order to enable a focusing of the electron beam on the sample surface, conductivity of the sample surface is a prerequisite for this measurement type. Therefore, SEM is a suitable method to determine the surface morphology of thin LPC silicon absorber layers.

By detecting the diffracted electrons instead of the forward scattered electrons local information about the crystallographic orientation and symmetry can be obtained. This method is known as Electron BackScatter Diffraction (**EBSD**). In this thesis an EBSD tool and analysis software OIM DATA ANALYSIS [156] provided by the company EDAX/TSL was used. For recording the EBSD lines the sample were tilted

by 70° and an SEM acceleration voltage was set to 25 kV. Areas of 800 µm x 800 µm were mapped with a step size of 2 µm. The results are pictured as 2D topography maps of the sample surfaces revealing the local grain orientation and grain size. For imaging the different crystallographic orientations are translated into different colors.

Optical UV/Vis/NIR Spectroscopy

Optical analysis was conducted using a Perkin Elmer UV/Vis/NIR LAMBDA 1050 spectrometer in a wavelength range of 300 nm up to 1200 nm with a 5 nm step size. The incident light spectrum is modeled using a deuterium lamp for wavelengths shorter than 320 nm and a tungsten lamp for longer wavelengths and is monochromatized. The samples are placed in the middle of an integrating sphere with the aid of a rotatable middle-position-holder enabling measurements under various angles of incidence. Incident light entering the integrating sphere is either absorbed in the sample under investigation, reflected back and scattered out of the device or transmitted at the rear side of the sample. For every incident wavelength the amount of light being reflected and transmitted and, hence, not absorbed (1-absorptance) is detected in the integrating sphere with a diameter of 15 cm [157–159]. The direct measurement of the entire amount of light not being absorbed (1-absorptance) allows for a straightforward calculation of the absorptance. Measuring inside the integrating sphere minimizes losses due to light being scattered out of device before entering the integrating sphere. The latter is of particular importance if textured substrates are analyzed. For reflectance measurements a black sheet is attached to the rear side of the samples absorbing the transmitted part of the light. The amount of light leaving the sample is reflected inside the integrating sphere as long as it reaches the detector area, which is mounted at the bottom of the integrating sphere. As detectors a high sensitive photomultiplier as well as an InGaAs detector are used. The detector change takes place at a wavelength of 820 nm. For shorter wavelength the monochromator slit size determining the resolution is set to 2 nm, for longer wavelength the slit size is adjusted between 2 nm and 20 nm to ensure a constant light intensity entering the integrating sphere. Insufficient adjustment of the light intensity can cause discontinuities in the measured spectra at the detector change. In order to account for possible fluctuations of the emitted light intensity the light beam is split into a reference beam being directly detected and a probe beam being detected after interacting with the sample under investigation. During measurement the samples are tilted by 8° with respect to the incident light beam avoiding a di-

rect escape of the specular reflectance out of the integrating sphere via the opening for incident light. Besides this opening, the integrating sphere is equipped with an opening for the reference beam to enter the detector area, an opening for reflectance measurements outside the integrating sphere as well as diffuse transmission measurements at the opposite side of the opening for incidence light and an opening for measuring haze in reflectance. For measurements conducted in the scope of this thesis the latter two openings were closed. Scattering out of the integrating sphere through any of these openings, imperfections of the integrating sphere, e.g. at the transition between the integrating sphere and the closing material, and parasitic absorption in any components of the integrating sphere are possible sources for measurement errors amounting to up to 4 % in total [160–162]. The measurement setup used as well as a typical example spectrum of a 10 µm thin LPC silicon absorber layer on a planar glass substrate coated with a SiO_x (250 nm) / SiN_x (70 nm) / SiO_x (10 nm) interlayer stack are schematically depicted in figure 3.4.

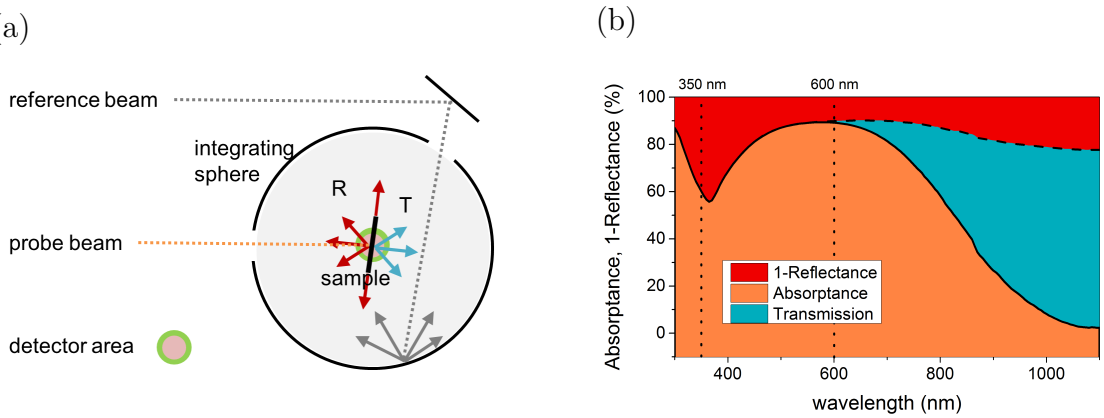


Figure 3.4: (a) Schematic of the UV/Vis/NIR measurement setup. (b) Optical spectrum of a 10 µm thin LPC silicon thin film absorber on a planar glass substrate coated with a SiO_x (250 nm) / SiN_x (70 nm) / SiO_x (10 nm) interlayer stack. The area of interest concerning the anti-reflective properties, starting from 350 nm to 600 nm, is enclosed by dotted lines.

Figure 3.4 (b) depicts a typical optical spectrum for a state-of-the-art planar absorber layer system as it is used as references in this thesis. As explained in chapter 2.1.1, incident light interacts with the sample under investigation either by being absorbed (A, orange), by being reflected (R, plotted as 1-R, red) back and scattered out of the device or by being transmitted (T, cyan) at the rear side of the sample (equation 2.7). For wavelengths shorter than the penetration depth reflection at the front interfaces is the only optical loss mechanism present in the device and the absorptance curve and the 1-reflectance curve coincide. For longer wavelengths incident light reaches the rear side of the silicon absorber layer and can partially escape

by being transmitted out of the device. Concerning the anti-reflective properties, optical analysis is restricted to a wavelength range of 350 nm to 600 nm, an area enclosed by dotted lines in figure 3.4,(b). Within this wavelength range measurement results of the absorber layers are not superimposed by parasitic absorption in other layers like the glass substrate or by back-scattering and transmission losses at the rear side of the device. Hence, light incoupling properties at the front side are separated from light trapping effects at the back side of the absorber layer.

The structures investigated in this thesis aim to enhance absorption (orange area) by reducing reflection losses (red area). For this purpose different light management methods with focus on reducing reflection losses at the substrate-silicon interface are applied to LPC silicon thin-film devices as described in chapter 2.1.2. Average reflectance values and the corresponding standard deviation have been calculated for a wavelength range of 350 nm to 600 nm, the substantial wavelength range for anti-reflective properties at the glass-silicon interface.

The maximum achievable short-current density can be calculated from the measured absorption curve (equation 2.8 in chapter 2.1.1) under the assumption that every photon absorbed contributes to current generation in the absorber layer:

$$j_{sc,max} = q \int_{280nm}^{1100nm} \frac{S(\lambda)}{h\nu} A(\lambda) d\lambda \tag{3.1}$$

with q the elementary charge, $h\nu$ the photon energy, $S(\lambda)$ the spectral intensity under AM1.5g and $A(\lambda)$ the absorption.

Quantum Efficiency

Solar cells are commonly characterized by determining their quantum efficiency. For external quantum efficiency measurements a custom-made setup was used, containing a probing beam size of 3 mm x 2 mm and LED-based bias-light imitating the AMG1.5g spectrum. The solar cell under investigation is illuminated by monochromatic light and for every wavelength the generated current is measured. The ratio, the number of generated carriers per incident photon, constitutes the External Quantum Efficiency (**EQE**) of a solar cell. In an ideal solar cell every incident photon would be converted to electric current and EQE curve would correspond to unity up to a wavelength corresponding to the band gap of silicon of around 1100 nm. For longer wavelengths the EQE would equal to zero. A real solar cell device suffers from various losses reducing the collection and conversion probability of incident photons

and the EQE. Depending on the penetration depth of the incident wavelength different loss mechanisms are dominant. Short wavelengths light being absorbed near the substrate-glass interface is mainly limited by front surface recombination, while long wavelengths are limited by rear surface recombination and transmission losses caused by a limited absorption depth and a declining absorption coefficient of silicon (figure 2.1). Reflection losses, parasitic absorption and low diffusion lengths reduce the quantum efficiency over the entire wavelength range. From EQE measurements the total number of carriers created, known as the short-circuit current density (j_{sc}, equation 2.16), of a cell can be extracted by determining the area under the EQE curve via:

$$j_{sc} = q \int_{300nm}^{1100nm} \Theta(\lambda) \cdot EQE(\lambda) d\lambda, \tag{3.2}$$

where q is the elementary charge of an electron, $\Theta(\lambda)$ the incident photon flux and $EQE(\lambda)$ the measured external quantum efficiency at wavelength λ.

If not considering all incident photons but the part of incident photons actually absorbed in the absorber layer, the Internal Quantum Efficiency (**IQE** = $EQE \,/\, A$) of a cell is obtained. Parasitic absorption in the substrate texture stack does not influence the measurements because of the low energy carried in the solar spectrum for wavelengths shorter than 350 nm [figure 2.1 (b)]. Due to optical loss mechanisms the amount of photons being absorbed in the absorber layer is typically smaller than the amount of incident photons. The IQE curve typically exceeds the EQE curve and the difference between EQE and IQE curve can be used to distinguish between electronic and optical losses in the cell. In summary, the external quantum efficiency is a suitable method to measure how efficiently the solar cell under investigation generates current at a given wavelength of incident light considering optical and electronic loss mechanisms, while the internal quantum efficiency is a measure for the absorber layer material quality considering electronic loss mechanisms only [60, 67, 119, 163].

Suns-V_{oc} measurements

Suns-V_{oc} is a suitable method to measure the open-circuit voltage of the solar cell devices in this thesis which were equipped with a simple and fast-to-process contacting scheme (chapter 3.1). Measurements were carried out at room temperature in superstrate configuration using a Suns-V_{oc} unit of a WCT-100 photo-conductance lifetime tool by Sinton Instruments. Suns-V_{oc} devices measure the open-circuit voltage of the solar cells as a function of the light intensity. For illumination with various intensities, typically starting from 0.1 suns up to a few suns, a flash lamp with slow decay is used. The intensity decay of the flash lamp is decisively lower than the minority carrier lifetime of the device under investigation. This ensures a quasi-stationary equilibrium during every measurement. In contrast to conventional jV-measurements, in Suns-V_{oc} measurements the illumination intensity is time-dependent monitored via a separate photodiode rather than using the short-circuit current density of the investigated cell. The combination of the two latter aspects allows for an easy and quick determination of a cell's open-circuit voltage (equation 2.14) as well as for high throughput [164–166]. As the voltage is measured under open-circuit conditions, there is no current flow. Therefore, the cell's series resistance does not influence the measurement (chapter 2.2.2). Thus, no sophisticated contacting scheme is needed. Using the short-circuit current density, which can be determined by external quantum efficiency measurements (equation 3.2), as input parameter and assuming that the generated current density is a linear function of the illumination intensity, an idealized jV-curve can be calculated [167, 168]. From this curve an idealized fill factor (equation 2.17) and an idealized efficiency (equation 2.18) can be extracted, as described in chapter 2.2.2. The fill-factor determined from Suns-V_{oc} measurements is also referred to as "pseudo fill factor" (**pFF**).

Light Beam Induced Current Analysis

In a Light Beam Induced Current (**LBIC**) measurement the area of a solar cell is scanned with a laser beam generating a local current flow, which is measured in order to determine a topography map of the short-circuit current density over the cell area. LBIC measurements can be used to image the local electronic material quality of a solar cell revealing for every measurement point its contribution to the current generation of the solar cell [169–172]. Typically, areas with a high contribution are depicted in bright colors while areas, which suffer from recombination losses and contribute less to current generation, are depicted in dark colors. Areas with high

current contribution are often found within a grain while areas with low current contribution are commonly found at grain boundaries or in grains with high defect density. LBIC measurements serve as a nondestructive method for defect imaging. To reveal the local electronic material quality a LBIC setup equipped with a 532 nm laser with a full width half maximum spot size of 26 µm and a halogen lamp based bias light was used as described in [43].

Secco wet etching

Wet chemical etching is a suitable method to uncover defects in crystalline silicon films since it offers the examination of large areas with a high selectivity. In general, a typical wet etching process consists of three parts. First, the etchant diffuses to the surface to be etched. Second, the etchant binds to the material being removed via a chemical reaction altering the original material. Third, the formed etch products detach and diffuse away from the reacted surface in order to allow the next etchant to reach the surface. At places containing defects the silicon crystal lattice is disturbed and bonds are weakened. Such places are more easily attacked by an oxidation agent forming silicon oxide, which can subsequently be removed using hydrofluoric acid. This mechanism provides the selectivity to preferentially etch defect-rich material. In a Secco based defect etch [173] an aqueous solution of CrO_3 is used as oxidizer. A Secco etching solution consists of HF, $K_2Cr_2O_7$ and H_2O in a ratio of HF:$H_2O = 2{:}1$ with 44 g $K_2Cr_2O_7$ dissolved in 1 l H_2O. Chromium atoms bind to the hydrogen-terminated silicon surface via an oxygen atom forming an Si-O-Cr-Cr(O_2)-O-Cr(O_2)-OH complex. The redox-reaction oxidizing silicon takes place as a second step. The high Cr-O bond strength as well as the high standard oxidation potential of Cr to Cr^{6+} allow for etch rates in the range of a few µm per minute. Beyond this, the chemistry involved when using chromium-based etching solutions is not fully understood yet [174–176]. In contrast to other silicon wet etches Secco etching provides the advantage of etching defects on all silicon surfaces independent of the crystal orientation [176]. This is of particular importance if poly-crystalline material, like LPC silicon, is used. To examine the material quality of silicon films grown and liquid phase crystallized on nano-textured glass substrates wet chemical Secco defect etching for 3 s to 4 s has been performed in order to uncover line and point defects at the silicon surface.

Raman Spectroscopy

The silicon bulk crystallinity was examined by Raman spectroscopy in a back-scattering geometry using a micro-spectroscopic Raman setup of InVia REFLEX, Renishaw, with an excitation laser of 785 nm. All spectra were measured with a 5x objective resulting in a laser spot diameter of approximately 10 µm. The Raman effect is based on inelastic scattering of incident monochromatic light in crystals or molecules. By measuring the energetic difference between incident light and scattered light corresponding to a characteristic energy shift of phonons being emitted (Stokes-scattering) or absorbed (Anti-Stokes-scattering) information about the structural properties and bonding conditions can be obtained. For crystalline silicon the characteristic optical phonon band is located at around 520 cm^{-1}. The full-width half maximum of this phonon band is related to the crystallinity of the sample. From shifts of the optical phonons band from the standard position information about stress can be deduced [177–179]. This measurement method has already been successfully applied to characterize light trapping structures in µc-Si:H thin-film solar cells [180, 181].

Optical simulations

In order to simulate the optical properties of the layer stacks under investigation a rigorous solver of the time-harmonic Maxwell's equations featuring a Finite Element Method (FEM) software package developed by JCMwave [182, 183] was used. By 3D FEM simulations optical reflection losses originating from backscattering at the textured glass substrate-silicon interface of sinusoidal textures with a pitch of 500 nm or 750 nm and aspect ratios varied between 0 (planar case) and 0.5 were analyzed. Differences between the simulated result and the result obtained experimentally might originate from imperfections of the experimental structure like inhomogeneities of the nanoimprint over the substrate or deviations of the experimental texture from a perfect sinusoidal shape. Simulating the amount of light being reflected back towards the silicon absorber, a repetitive reflection and subsequent escape of the device is not considered. These factors lead to an idealization of simulated device for the benefit of simulation cost.

4 Identifying a Suitable Glass-Silicon Texture

Current cell designs for 10 µm thick liquid phase crystallized (LPC) silicon thin-film solar cells on glass address optical losses by texturing the sun-facing air-glass interface as well as the silicon absorber backside. The optical absorption potential is not fully tapped mainly due to losses at the planar glass-silicon interface. According to calculations of Frijnts *et al.* these direct reflection losses translate into a short-circuit current density loss of at least $3.4\,\mathrm{mA\,cm^{-2}}$ [43]. Effective measures for light management are needed at the glass-silicon interface to further increase photo-generated current densities in LPC-Si thin-film solar cells.
This chapter enfolds a detailed study identifying suitable nano-textures for the glass-silicon interface to increase incoupling of light whilst at least maintaining the electronic material quality of the silicon absorber layer. For this purpose the interplay between a simplified one-dimensional model texture and the liquid phase crystallization process is studied. Subsequently, two-dimensional structures with different hexagonal texture geometries are developed. The resulting devices are evaluated regarding their ability to reduce reflection losses and their influence on the silicon absorber layer material quality. The structures developed are put into context with previous work on texturing the glass-silicon interface as well as state-of-the-art planar references.

4.1 Previous Work on Texturing the Glass-Silicon Interface

Nanoimprint lithography [44, 107, 132] in combination with high-temperature stable sol-gels [55, 56] has demonstrated its suitability for texturing the glass-silicon interface in LPC silicon solar cells [46]. In previous work, texturing of the glass substrates was realized by utilizing a statistically etched crater-like texture with an

aspect ratio of around 0.05 as well as a periodic U-shaped square lattice (SL) texture with an aspect ratio of 0.5. The statistically etched low-aspect ratio texture allowed for maintaining the electronic silicon material quality but did not significantly enhance light incoupling into the cell. On the other hand, the high aspect ratio SL texture enhanced the optical properties of the cells but disturbed the silicon material quality causing a decline in quantum efficiencies [57, 59]. The high aspect ratio structure determined an upper limit regarding the silicon material for textures at the glass-silicon interface in LPC solar cells.

As a second reference system, representing the optimum electronic material quality case, a planar device stack has been chosen. The planar reference stacks were produced following the current LPC silicon thin-film solar cells on glass design featuring a substrate-to-silicon interlayer system consisting of a 70 nm to 80 nm thick SiN_x layer providing anti-reflective properties followed by a 10 nm to 20 nm thick SiO_x interlayer for passivation (chapters 2.1.2 and 2.2.1) and a 10 µm thick n-doped silicon absorber layer with a doping density of roughly $5 \times 10^{16}\,\mathrm{cm}^{-3}$ [17, 86, 146, 184]. The latter two devices types, the nanoimprinted high aspect ratio square lattice structure and the planar device, determine the cornerstones of this thesis and are depicted in figure 4.1.

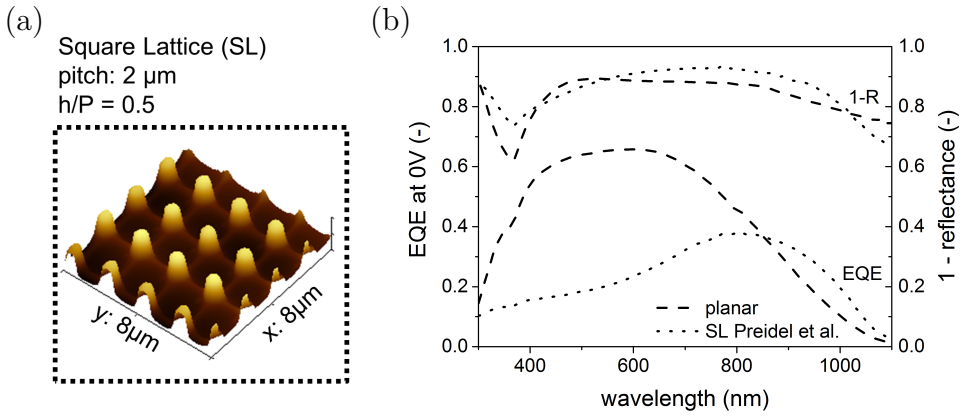


Figure 4.1: Characteristics of a U-shaped square lattice (SL) structure of Preidel *et al.* [58] (dotted) as well as a state-of-the-art planar reference device (dashed). (a) Atomic force microscope (AFM) image of a SL structure. The corresponding pitch and aspect ratio (height/pitch) of the SL structure are given in the figure. (b) External quantum efficiency (EQE) and reflectance measurements (R, plotted as 1-R) of a SL textured device (dotted) and a planar reference device (dashed).

Figure 4.1 (a) depicts an AFM image of the high aspect ratio square lattice (SL) structure of Preidel [58]. Its pitch (P) of 2 µm and height (h) of 1 µm resulting in an aspect ratio (h/P) of 0.5 are stated. The structure features smooth valleys between the structure tips. Determined by its high aspect ratio, the structure flanks are steep. The optical properties are shown in figure 4.1 (b) (plotted as 1-Reflectance,

dotted). Since the structure's pitch of 2 µm is large with respect to the wavelength of incident light, the anti-reflective effect in the short wavelength range is small compared to a state-of-the-art planar reference layer (dashed). On the contrary, for wavelengths longer than 600 nm a reduction of reflection is found, which might be caused by a light scattering effect into higher angles at the glass-silicon texture as well as back scattering at the rear side of the double-sided textured silicon absorber layer. The electronic properties, here represented by external quantum efficiency measurements (EQE), of a U-shaped high aspect ratio square lattice texture are severely disturbed compared to the planar reference. Only for wavelengths longer than 850 nm the enhanced optical properties lead to an enhancement in photocurrent generation and the EQE of the square lattice exceeds the planar reference. As cause of the decline in electronic properties, dislocation lines, which originate at the steep structure flanks and proceed through the silicon absorber layer until the silicon surface, were identified by TEM investigations [59].

In summary, compared to a high-quality state-of-the-art planar reference the square lattice structure enhances light incoupling for wavelength longer than 600 nm and, following as a consequence, enhances the electronic properties for wavelength longer than 850 nm. For shorter wavelengths the electronic properties decline. This could be attributed to a disturbance of the silicon absorber layer material quality caused by the steep texture flanks of the high aspect ratio square lattice structure [59]. Based on these results of Preidel [58, 59] the structures of this thesis were designed as it follows.

4.2 Interplay Between One-Dimensional Line Gratings and the Liquid Phase Crystallization Process

To explore the interplay between a substrate texture and the liquid phase crystallization process from a more basic point of view one-dimensional line gratings with a pitch (P) of 690 nm and a height (h) of 140 nm resulting in an aspect ratio (h/P) of 0.2 have been chosen as simplified substrate geometry. The texture pitch was selected as compromise between optical simulations for 10 µm thick LPC silicon absorber layers revealing optimized anti-reflective properties for a hexagonal substrate texture of 500 nm to 600 nm [185, 186] and literature values revealing a higher silicon material quality for larger pitches [39]. An aspect ratio of around 0.25 was chosen

as compromise between the two model textures of Preidel [58] described in the last sub-chapter. A schematic sample stack and an AFM scan of the substrate textured with a one-dimensional line grating are depicted in figure 4.2.

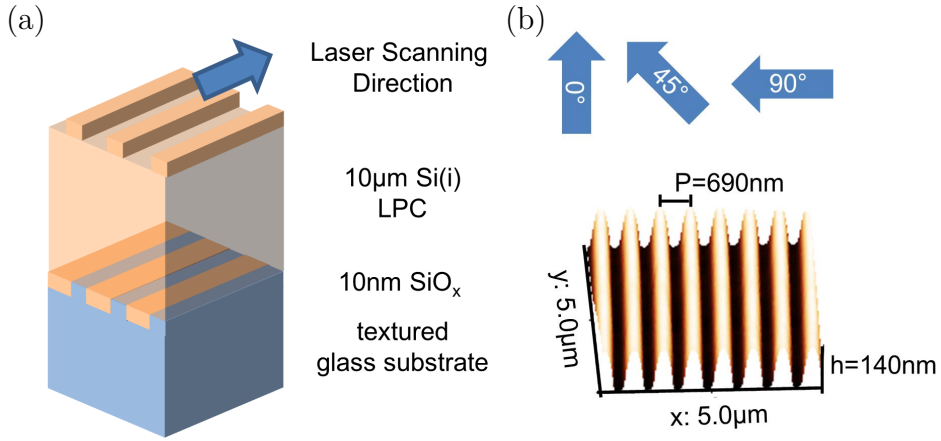


Figure 4.2: (a) Schematic sample stack designed according to the sinusoidal sample stack with a one-dimensional line grating as substrate texture. The laser scanning direction during liquid phase crystallization is indicated by a blue arrow. (b) AFM scan of the line grating substrate texture. The height (h) and pitch (P) are denoted. As indicated by blue arrows above the AFM scan during this study the laser crystallization direction determining the crystal growth direction is altered by 0°, 45° and 90° with respect to the line grating direction.

In order to investigate whether the substrate texture affects the liquid phase crystallization process and the resulting silicon material quality the laser is scanned in grating direction (0°), in a 45° angle and perpendicular to the grating direction (90°). The resulting silicon material quality is analyzed in the following.

4.2.1 Grain Size Analysis

A defect rich silicon grain growth bears many disturbances in the silicon layer. Defect sides can act as crystallization centers starting grain growth when recrystallizing from the melt during the liquid phase crystallization process. Silicon grown on a steep-valley substrate texture should appear finer grained, i.e. smaller and a larger number of grains. To make grain boundaries visible, the samples were etched for two minutes in a silicon etching solution for two minutes (chapter 3.2). In order to allow for quantification, grains per unit area are counted. Due to the anisotropic silicon growth with preferential growth in scanning direction of the crystallization laser an area of 0.5 cm in length and 1 cm in width has been chosen as unit area for all depicted pictures. The number of grains per unit area of 10 µm thick LPC silicon

absorber layers crystallized in different angles with respect to the grating direction (as schematically shown in figure 4.2) is analyzed in figure 4.3.

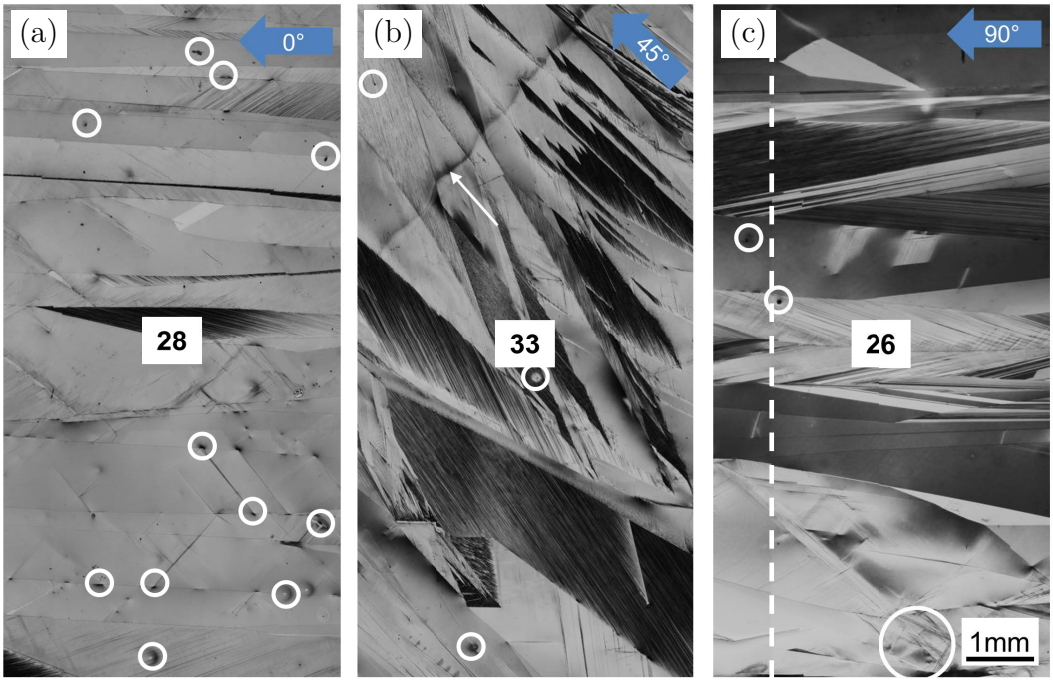


Figure 4.3: Light microscope images of 10 µm thick absorber layers grown and crystallized on one-dimensional line gratings. The crystallization direction with respect to the grating direction was alternated by (a) 0°, (b) 45°, and (c) 90° as indicated by blue arrows as insets. The numbers in the middle of each image correspond to the number of grains counted depicted per unit area of 0.5 cm x 1 cm. Some defects are highlighted by white circles. The dashed line indicates a stitching line of the microscope.

On an area of 0.5 cm x 1 cm 28 grains are found if the absorber layer is crystallized in grating direction, as displayed in figure 4.3 (a). 33 grains are found if the absorber layer is crystallized in a 45° angle with respect to the grating direction, which is shown in figure 4.3 (b). 26 grains per unit area are found if the silicon absorber layer is crystallized perpendicular to the grating direction. The latter is depicted in figure 4.3 (c). While the image excerpts for the 0° and 90° sample have been chosen according to the corresponding crystallization directions, the area for the 45° sample has not been tilted, in order to demonstrate that the silicon crystal growth direction in laser scanning direction is not disturbed by the substrate texture. This missing tilting in crystal growth direction explains the slightly higher number of grains on the absorber layer crystallized in a 45° angle. Indeed, if the area on the 45° sample is adjusted according to its crystallization direction a number of 30 grains are counted (not depicted in figure 4.3). By applying the silicon etch solution not only grain boundaries but also point defects on the silicon absorber layer can be made visible. Some of these point defects have been highlighted by white circles in

figure 4.3. Comparing the absorber layers with different crystallization directions, most point defects are found on the absorber layer crystallized in line grating direction. Figure 4.3 (b), displaying the sample crystallized in a 45° angle, features a dislocation line running perpendicular to the grain growth, which is highlighted by a white arrow. Overall, according to grain size analysis by wet-chemical etching the highest material quality is achieved if the absorber layer is crystallized perpendicular to the one-dimensional grating direction. Compared to this sample, the sample crystallized in grating direction features a similar number of grains per unit area but a higher number of defects while the sample crystallized in a 45° angle with respect to the grating direction features a similar number of defects but a higher number of grains per unit area, which appear less uniform. The respective experiments on planar absorber layers are depicted in the appendix (figure A.1) demonstrating that the material quality of absorber layers crystallized on textured glass substrates corresponds to the material quality obtained on planar substrates.

In order to allow for a more quantitative analysis, EBSD mapping on an area of 800 µm x 800 µm with a step size of 2 µm has been conducted. In addition to the grain size, EBSD maps reveal the crystal orientation. The EBSD maps of 10 µm thick silicon absorber layers are depicted in figure 4.4. The corresponding crystallization directions with respect to the line grating direction are indicated by an arrow as insets.

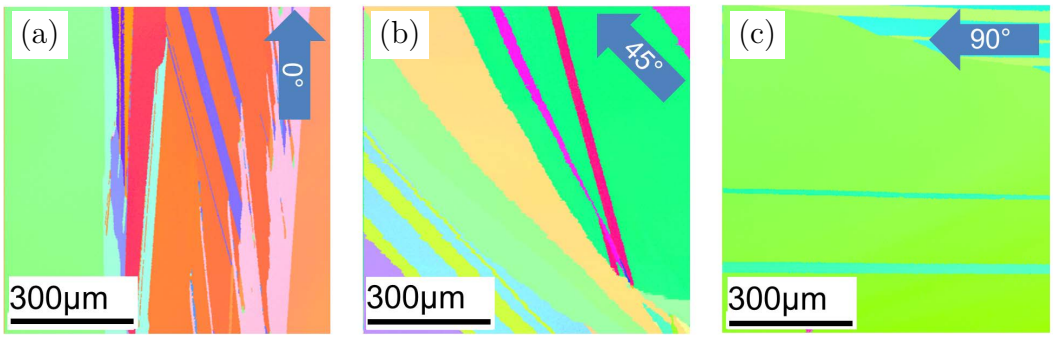


Figure 4.4: EBSD images of 10 µm thick silicon absorber layers on 1D line gratings crystallized (a) in grating direction (0°), (b) with an angle of 45° with respect to the grating direction, and (c) perpendicular to the grating direction (90°). The crystallization direction is indicated by an arrow in the corresponding pictures.

Figure 4.4 compares EBSD maps of 10 µm thick silicon absorber layers on line grating textured substrates being crystallized (a) in grating direction, (b) in a 45° angle with respect to crystallization direction, and (c) perpendicular to the grating direction. The crystallization and crystal growth direction is reflected in all three images. The first two absorber layers feature large and small grained areas with a variety

of crystallographic orientations. The least grains and, moreover, only two different crystal orientations are found for the sample where the silicon was grown perpendicular to the grating direction. According to the EBSD measurements presented here the highest silicon material quality is achieved if the laser beam is scanned perpendicular to the grating direction. A possible explanation might be that if the line-shaped laser beam is scanned in an 0° or 45° angle over an absorber layer deposited on a one-dimensional line grating, this laser beam interacts with many lines of the grating along the beam line at the same time. This might alternate the otherwise uniform shape of the laser beam, in term, alternating the energy input into the film. An uneven energy distribution in the silicon layer might be a cause for a more defective grain growth and might explain the occurrence of the large number of crystals and crystal orientation on these two absorber layers. On the contrary, if the laser beam is scanned perpendicular to the line grating, the laser beam is scanned either over a flat ground part or over a flat grating without alternations along the beam line. This might avoid disturbances of the beam and lead to a more uniform energy input and film growth.

4.2.2 Defect Density Analysis

To reveal defects in the silicon bulk, the silicon absorber layers were etched for 3 s with a wet-chemical Secco etch. In order to account for the large uniform grain size resulting from the LPC process, SEM images were taken at three spots throughout the absorber layer. These three spots are depicted in figure 4.5 for every crystallization direction (according to figure 4.2).

On the absorber layer crystallized in grating direction depicted in figure 4.5 (a) no defects are found within the three areas investigated by SEM imaging. On the absorber layers crystallized in 45° or 90° angles with respect to the line grating direction, which are depicted in figure 4.5 (b) and (c), respectively, two out of the three investigated areas exhibit line defects. In both cases these line defects occur in crystallization direction. On the absorber layer crystallized with 45° angle 8 and 10 line defects are found. The absorber layer crystallized perpendicular to the grating direction exhibits 15 and 12 line defects. Therefore, based on Secco etching the best material quality is found if the absorber layer is crystallized in grating direction. The respective experiments on planar absorber layers are depicted in the appendix (figure A.2) highlighting that the material quality of absorber layers crystallized on textured glass substrates equates to the material quality achieved on planar absorber layers.

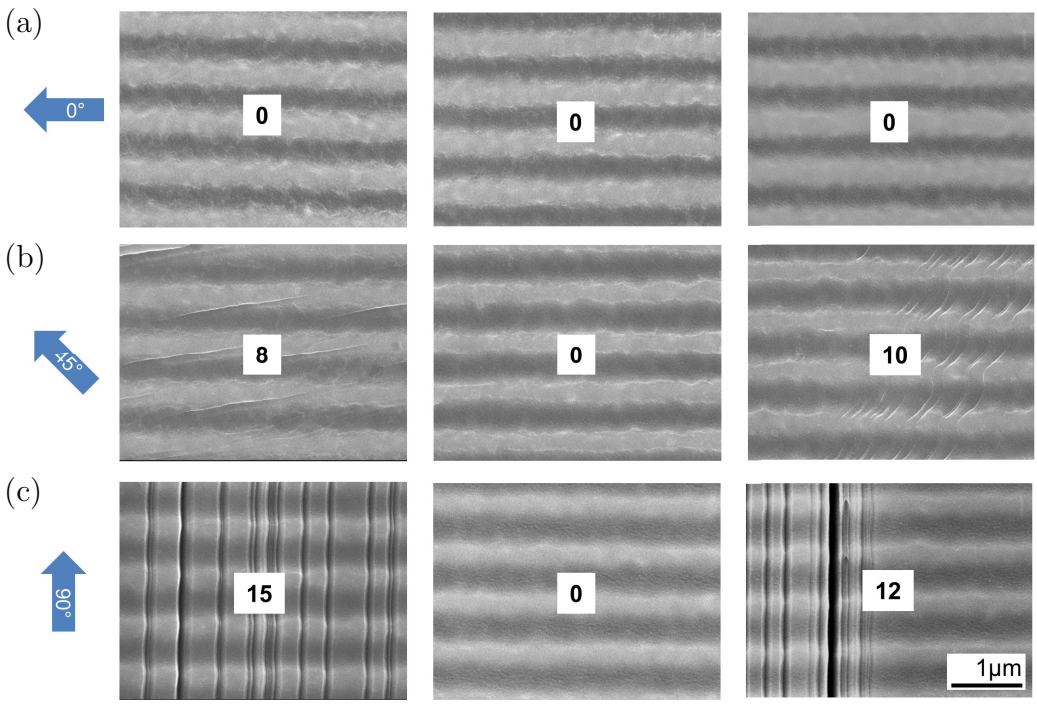


Figure 4.5: SEM images of 10 µm thick LPC silicon absorber layers grown on substrates textured with one-dimensional line gratings crystallized (a) in grating direction (0°), (b) in a 45° angle with respect to the grating direction and (c) perpendicular (90°) to the grating direction. The crystallization directions are indicated by blue arrows. The numbers in the middle of every image refer to the number of defects counted in this image.

In summary, a similar silicon material quality is achieved regardless of the crystallization direction. In case of the absorber layer crystallized in grating direction, this high material quality is mainly demonstrated by exhibiting no line defects uncovered by Secco defect etching over three randomly chosen areas on the absorber layer. In case of the absorber layer being crystallized perpendicular to the grating direction the high material quality was especially highlighted by the large uniform areas revealed by EBSD imaging. Taking into account all analysis techniques applied, a silicon material quality comparable to planar references was achieved concerning the structural properties, grain size and defects in the silicon bulk. Thus, a substrate texture pitch of around 700 nm and an aspect ratio of about 0.2 have proven their suitability as substrate texture geometries in LPC crystallized absorber layers and are recommended for further experiments.

4.3 Pillar and Sinusoidal Shaped Glass-Silicon Textures

The substrate texture geometries revealed in the last subchapter have been chosen for the first newly developed structure for textured LPC silicon solar cells, namely a hexagonal pillar structure ("Pillar") with a 750 nm pitch and an aspect ratio of 0.2. The structure flanks were chosen to be steep because these are known to reduce reflection losses more efficiently than smooth texture flanks [67, 187]. In previous work this structure has demonstrated enhanced incoupling of light on a broad wavelength range [188]. An atomic force image of the pillar shaped structure is depicted in figure 4.6 (a).

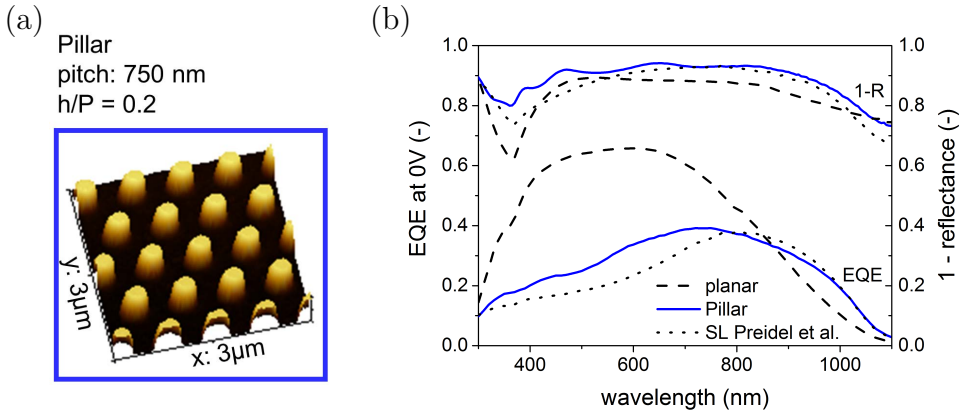


Figure 4.6: Characteristics of the pillar shaped texture (Pillar, blue): (a) pitch, aspect ratio (h/P) and AFM image and (b) external quantum efficiency (EQE) and 1-Reflectance data of a Pillar patterned device compared to a high aspect ratio square lattice (SL) texture of Preidel *et al.* [59] (black, dotted) as well as a planar reference (black, dashed).

Comparing the optical properties of the pillar structure (in figure 4.6 (b) plotted as 1-Reflectance, blue) to the square lattice (SL) structure, the light scattering effect in the long wavelength range could be preserved despite the smaller texture feature sizes exhibiting less light scattering potential from a geometrical optics point of view. The pillar structure offers an enhanced incoupling of light into the silicon absorber layer over a broad wavelength range, which is attributed to its smaller pitch [188]. Using the pillar shaped substrate texture instead of the square lattice texture reflection losses are reduced in the wavelength range below 600 nm, now exceeding the planar reference (black, dashed) over the entire wavelength range. Mean reflectance averaged over the wavelength range between 350 nm and 600 nm amounts to 17.1 % ± 8.8 % for the planar device, 16.0 % ± 5.3 % for the square lattice device and 11.0 % ± 3.7 % for the pillar patterned device. In the wavelength range of interest this corresponds to a reduction of reflection losses of 6 % (absolute) if

using a pillar patterned sample instead of a planar device. The electronic material quality is still declined and only little improvement is found compared to the high aspect ratio square lattice device.

In summary, changing the high aspect ratio square lattice structure to a pillar structure with smaller feature sizes increases the optical properties but maintains the disturbed electronic material quality. Nevertheless, the pillar structure with an aspect ratio of 0.2 can serve as guideline for enhanced optical properties.

Concluding from the experiment presented above steep texture flanks, even with moderate aspect ratio fo 0.2, have to be avoided in order to combine enhanced optical properties with a high electronic material quality. A sinusoidal type structure ("Sine") with same pitch and aspect ratio as the pillar structure but smooth instead of for the electronic material quality detrimental steep texture flanks has been chosen [figure 4.7 (a)] as second model texture. In addition, optical simulations revealed that sinusoidal nano-structures exhibit excellent anti-reflective properties for 10 µm thick silicon absorber layers with a broad optimum at pitches around 500 nm to 600 nm [185, 189]. A pitch width of 750 nm was chosen as a compromise based on these numerical simulations and preliminary LPC experiments showing a better silicon material quality at larger pitches. Besides, a fixed pitch of 750 nm and aspect ratio of 0.2 allow for a comparison between the sinusoidal and pillar structure as independent of the structure geometry as possible.

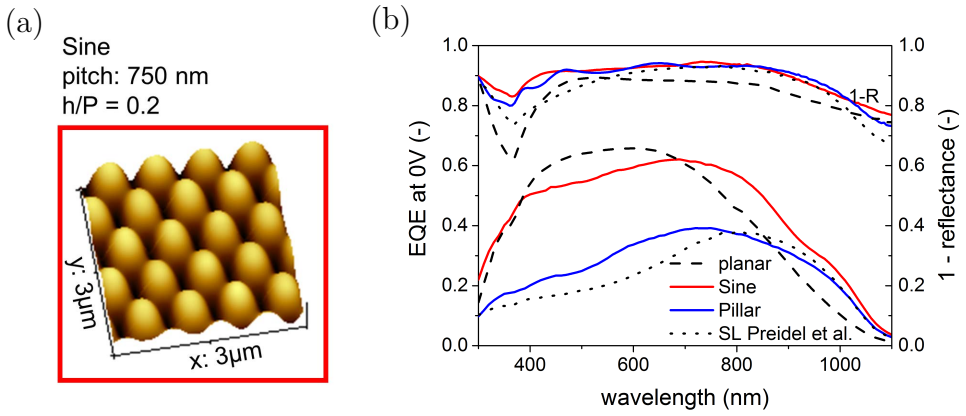


Figure 4.7: Characteristics of the sinusoidal shaped texture (Sine, red): (a) AFM image with pitch and aspect ratio given, and (b) external quantum efficiency (EQE) as well as reflectance data (plotted as 1-reflectance) compared to an optimized state-of-the-art planar reference (black, dashed), a high aspect ratio reference of Preidel [58] (black, dotted) and a pillar patterned device (blue).

Just as the pillar textured devices (blue), sinusoidal textured devices (red) exhibit an anti-reflective effect over the entire wavelength range compared to a planar reference, as shown in figure 4.7 (b). By smoothing the texture flanks from a pillar to

a sinusoidal structure the enhanced optical properties were not only preserved but even slightly enhanced. In the wavelength range of 350 nm to 600 nm mean reflection of the sinusoidal texture equals 9.5 % ± 3.1 %, a reduction of 7.6 % (absolute) compared to the planar reference device with a state-of-the-art anti-reflective layer stack. For wavelengths longer than 750 nm the incident light starts to reach the rear of the 10 µm silicon absorber layer and light is partially reflected back into the absorber layer. This process is especially enhanced if the backside of the absorber layer is textured as it is the case for double-sided textured devices. For all devices the absolute difference between optical and electrical measurements is caused by recombination losses in the electronic device [67]. Despite the superior optical properties, the external quantum efficiency of the sinusoidal texture, depicted in figure 4.7 (b), cannot outperform the planar reference cell (black, dashed) over the entire wavelength range. For wavelengths smaller than 400 nm the sinusoidal textured device performs better than the planar reference due to the anti-reflective effect of the sinusoidal texture. The light trapping effect of the double-sided textured rear side causes again an enhanced performance of the sinusoidal textured device for wavelengths above 700 nm. In the wavelength range between 400 nm and 700 nm the external quantum efficiency of the sinusoidal device is reduced compared to the planar reference. Nevertheless, compared to the pillar and square lattice (SL) textured references the electronic properties of the sinusoidal textured device are remarkably enhanced. This might again be attributed to the superior bulk material quality of silicon being grown and crystallized on the sinusoidal grating. These results underline that compared to a pillar patterned device and the high aspect ratio square lattice device the smooth sinusoidal shape is favorable for high quality silicon absorber layers.

4.4 LPC Silicon Material Quality on Textured Substrates

In order to explain the impact of the different substrate texture types on the silicon absorber layer material quality influencing the external quantum efficiency measurements, the corresponding internal quantum efficiencies are calculated as described in chapter 3.2 and depicted in figure 4.8.

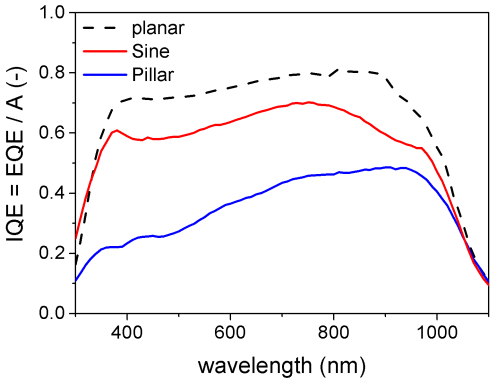


Figure 4.8: Internal quantum efficiencies (IQE) of a sinusoidal textured solar cell (red), a pillar textured solar cell (blue), and a planar reference solar cell (black, dashed) calculated from measured external quantum efficiencies (EQE, figure 4.7) and absorptance (A=1-R-T).

The internal quantum efficiency (IQE) of a solar cell reveals the amount of actually absorbed photons that contribute to current generation. In the planar reference cell (back, dashed) up to 80 % of the absorbed photons generate an electron-hole pair in the visible region of light. The sinusoidal textured device (red) exhibits a similar IQE for wavelengths shorter than 380 nm. For longer wavelengths the IQE of the sinusoidal textured device follows the curve obtained for the planar reference with a reduced offset of around 0.1. This decline might be attributed to an increased surface recombination velocity caused by the increased surface area of the textured substrate or an increased defect density arising at the textured front interface. For wavelengths longer than 500 nm the IQE slightly increases up to values of 70 % indicating that the declined material quality might not only be a bulk but especially a surface near problem. The pillar textured device (blue) exhibits a strongly reduced IQE over the entire wavelength range. In case of the pillar structure a maximum internal quantum efficiency of only 50 % is reached. Compared to the sinusoidal textured device, the IQE of the pillar texture is diminished over the entire wavelength range. This result highlights the beneficial effect of the smoothed sinusoidal texture flanks on the material quality compared to steep texture flanks, as featured for the pillar texture.

In addition to the calculation of the IQE curves, wet-chemical Secco defect etching of silicon absorber layers and LBIC measurements on solar cells prepared on correspondingly textured substrates were conducted. The results are summarized in figure 4.9.

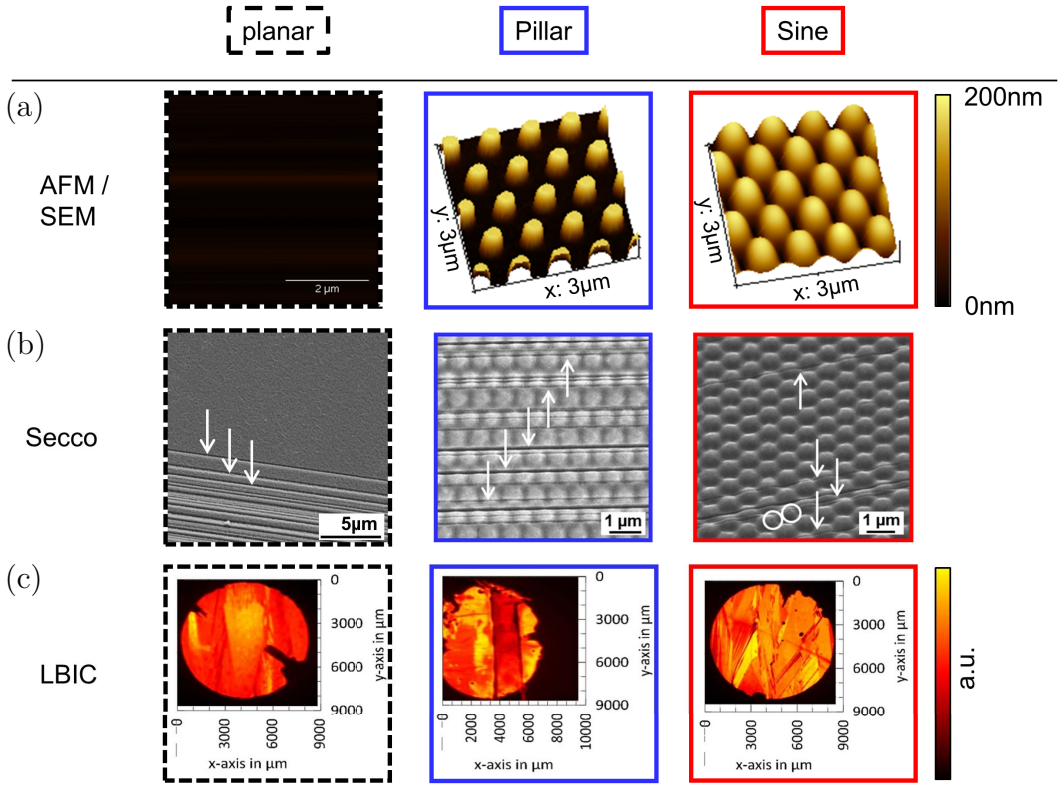


Figure 4.9: Examination of the LPC silicon absorber layer material quality on the different substrate texture types planar (dashed), pillar (blue) and sinusoidal ("Sine", red). (a) For easier identification AFM images of the textured substrates are depicted. (b) SEM images of 10 µm thick LPC silicon absorber layers on the respective substrate types after 4 s of wet-chemical Secco defect etching. (c) LBIC measurements of LPC silicon thin-film solar cell devices prepared on the respective substrate types. The respective EQE curves are depicted in figure 4.7.

Secco defect etching uncovers that a planar absorber layer (dashed) exhibits both, large areas without etch defects as well as areas with a high number of defects [figure. 4.9 (b)]. The large areas of uniform high-quality material are not only reflected by the EQE measurement (figure 4.1) but also demonstrated by LBIC topography imaging [figure 4.9 (c)], where large bright areas correspond to a high local photocurrent while few dark areas correspond to a low local photocurrent. The strips approaching from both sides into the cell area correspond to shadowed areas caused by insufficient coverage prior to emitter etching and contact deposition.

For a silicon absorber layer grown and liquid phase crystallized on a 750 nm pitched pillar structure with an aspect ratio of 0.2 (blue) a substantial number of line defects originating from grain boundaries is found by Secco defect etching [figure 4.9 (b)]. One possible reason for the large amount of defects arising from steep structure flanks

might be voids in the silicon known to grow increasingly porous on texture flanks steeper than 30° [148]. Such voids might be the starting point for the high amount of dislocations in the silicon absorber layer arising at steep texture flanks [59]. Another reason might be voids in the silicon caused by self-shadowing effects during the silicon growth resulting from silicon growing simultaneously on the bottom of the substrate as well as on top of the texture features shadowing the texture flanks underneath [46]. Note that on the pillar texture areas like depicted for the planar case can be found and vice versa. Owned to the large crystal dimensions achieved by the liquid phase crystallization process only a small excerpt of the absorber layers can be imaged here. The excerpts depicted in figure 4.9 (b) have been chosen to be representative for the entire sample and are intended to provide qualitative impressions rather than to give a quantitative analysis. LBIC topography imaging [figure 4.9 (c)] reveals a large area with disturbed photocurrent generation corresponding to darker areas in the topography image. This area of disturbed material quality is bordered by line defects, probably grain boundaries, running along the entire cell area. These results explain the low electronic material quality of pillar textured solar cell devices revealed by EQE measurements (figure 4.6).

In case of the sinusoidal nano-structure (red) with an aspect ratio of 0.2 large areas without Secco etched defect lines or point defects can be found as depicted in figure 4.9 (b). The occurrence of some line defects and rare occurrence of point defects prove that defect etching has been successful. The pillar (blue) and sinusoidal (red) structures feature the same pitch and aspect ratio and differ only by the slope of the texture flanks. The reason for the strongly differing amount of extended defects in LPC silicon layers on sinusoidal and pillar textured glasses might be a large number of dislocations that have been shown to occur on steep textures [59] as they are featured in the pillar grating but not in the sinusoidal shaped texture. An LBIC topography image, corresponding to the EQE measurement (figure 4.7), is depicted in figure 4.9 (c) containing a high number of bright areas with a high contribution to photocurrent. Compared to a planar reference (dashed) the cell area appears finer grained. Apart from being smaller grained, the silicon morphology is comparable to state-of-the art planar references. In conclusion, because only a small decline in electronic bulk material quality compared to the planar reference was found during LBIC topography imaging and Secco defect etching, most of the decline in external and internal quantum efficiency might be ascribed to enhanced surface recombination caused by the enlarged surface of the patterned substrate.

4.5 Influence of the Sinusoidal Texture Geometry on the Silicon Material Quality

In order to examine the influence of the sinusoidal texture geometry on the silicon material quality in detail, silicon absorber layers have been prepared on a sinusoidal textured substrates with varied texture geometries: a sinusoidal texture with steep bottom and wide top angle, a sinusoidal texture with inverted opening angles, a wide bottom angle and a sharp top angle, and a planar reference. Sharp bottom angles are known to disturb the silicon material quality by causing a defective silicon growth [41]. Likewise, high aspect ratios [59] and smaller pitches [39] have demonstrated to be detrimental for the silicon material quality.
In the following, the silicon material quality on different sinusoidal texture geometries is analyzed. For simplicity, the samples featured in this study are illustrated in figure 4.10.

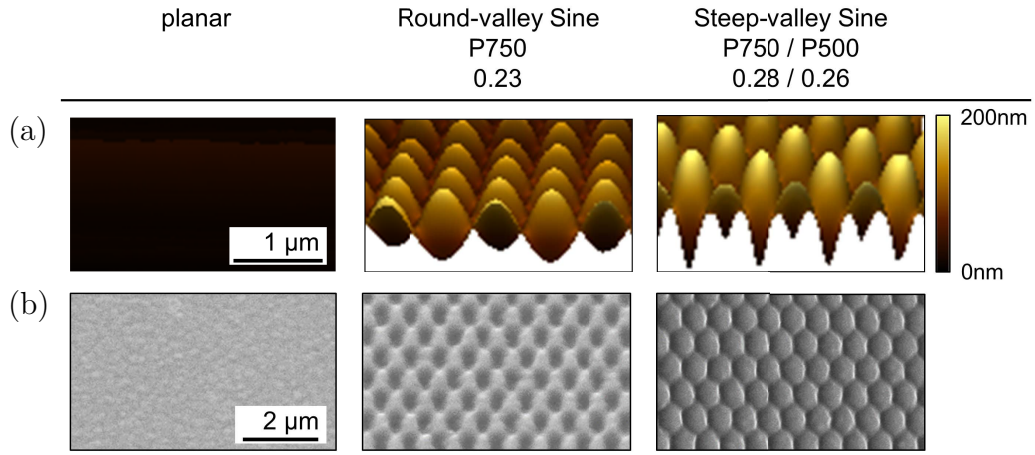


Figure 4.10: (a) AFM scans of the planar reference and sinusoidal substrate textures focusing on the opening angles. (b) SEM images of the rear side of the 10 µm thick silicon absorber layers. In case of the textured substrates the substrate texture is preserved, again illustrating the inverted opening angles and texture shapes. In addition to the sample descriptions, the substrate pitch (P) and aspect ratio (h/P) are given. In case of the steep-valley sinusoidal substrate geometry the substrate pitch of 750 nm is depicted, since both steep-valley textures differ by the substrate pitch only.

Due to the hexagonal periodicity of the sinusoidal gratings the silicon material quality on two-dimensional substrate textures is not influenced by the crystallization direction with respect to the substrate geometry but only by the texture geometry itself. In order to make the different sinusoidal substrate geometries as distinguishable as possible and, hence, differences most likely to be observable, the sinusoidal texture with the sharp bottom angle was designed to feature a high aspect ratio

of 0.28 and is in the following referred to as "Steep-valley Sine". Accordingly, the sinusoidal texture with wide bottom angle was chosen to feature a smoother aspect ratio of 0.23 and is in the following referred to as "Round-valley Sine". In order to intensify the detrimental influences of the sharp bottom angle, an additional sample with reduced pitch to 500 nm with an aspect ratio of 0.26 was prepared, which is in the following referred to as 500 nm pitched Steep-valley Sine.

4.5.1 Grain Size Analysis

In order to analyze if the different substrate textures influence the crystal growth during liquid phase crystallization, 10 µm thick LPC silicon absorber layers were prepared on the different sinusoidal substrate geometries as well as on a planar reference (according to figure 4.10). The corresponding light microscope images after grain boundary etching are given in figure 4.11 and the number of grains per unit area of 0.5 cm x 1 cm are given.

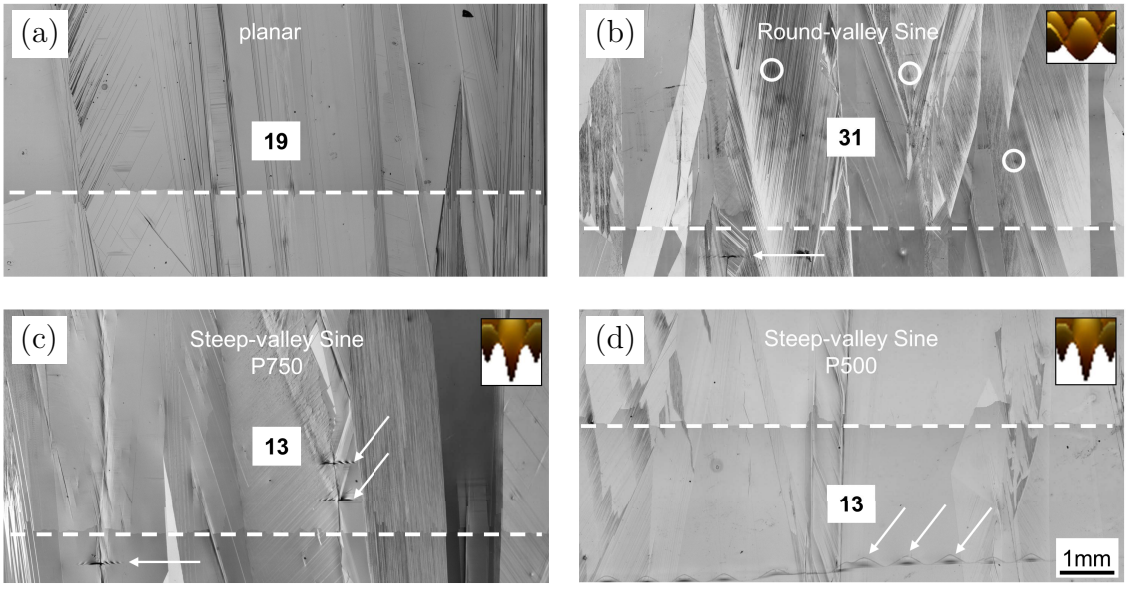


Figure 4.11: Light microscope images of 10 µm thick LPC absorber layers on (a) a planar substrate (b) a Round-valley Sine with 750 nm pitch, (c) a Steep-valley Sine with 750 nm pitch, and (d) a Steep-valley Sine with 500 nm pitch. For simplicity, AFM images of the corresponding substrate texture are depicted as insets. The dotted lines mark lines caused by stitching when taking the light microscope image and shall prevent confusion with a grain boundary. The numbers given in the middle of the pictures refer to the number of grains counted per depicted unit area of 0.5 cm x 1 cm. Circles mark some of the dark circular defects in (b) and arrows in (c) and (d) highlight line defects.

In figure 4.11 the grain growth is analyzed by counting grains per unit area. For (a) the planar absorber layer this amounts to 19 grains, for (b) the Round-valley Sine with 750 nm pitch to 31 grains, for (c) the Steep-valley Sine with a 750 nm pitch to 13 grains, and (d) the Steep-valley Sine with 500 nm pitch to 12 grains per unit area. On both steep-valley substrates a grain growth comparable to the planar reference is achieved. Nonetheless, there are dislocation lines arising at grain boundaries (in figure 4.11 (b) and (d) highlighted by arrows), which probably are caused by stress release during the LPC process. The occurrence of such dislocation lines at grain boundaries hint at a too high heat input during the LPC process. Similar dislocation lines occurred on planar absorber layers prior to optimizing the LPC process suggesting that those dislocation lines on textured substrate can be avoided by adjusting the LPC process to slightly lower energies. On the contrary, the round-valley sinusoidal texture is the only substrate texture for which a disturbed silicon growth is observed. On the same unit area, twice as much grains accompanied by a reduced grain size are found than for the planar reference or the inverse sinusoidal textures suggesting that there are twice as much defects in the silicon layer grown on the round-valley sinusoidal textured substrate. On the other hand, from literature it is known that a wide opening angle as well as a reduced texture height have beneficial effects on the silicon material quality [39–41]. Therefore, it is likely that these defects arise from a processing issue rather than be caused by the substrate texture. One possible issue might be insufficient cleaning of the glass substrate, which would also explain the dark spots in figure 4.11 (b), some of them have been highlighted by circles. Nevertheless, these results demonstrate that a grain sizes and grain growth comparable to the planar reference are possible despite using a 500 nm and 750 nm pitched sinusoidal textured substrate with aspect ratios of up to 0.28 during silicon growth and crystallization.

For a more quantitative analysis of the crystal growth EBSD measurements have been conducted on the planar reference as well as on the Steep-valley and the Round-valley Sine with same pitch of 750 nm. The respective results are depicted in figure 4.12.

Figure 4.12 displays EBSD images of randomly chosen 800 µm x 800 µm areas on 10 µm thick silicon absorber layers crystallized on (a) a planar reference, (b) a round-valley sinusoidal structure, and (c) a steep-valley sinusoidal texture. In agreement with the grain size analysis by light microscopy (figure 4.11), a similar grain structure is found for the planar and the steep-valley sinusoidal texture. Both absorber layers feature only two grains extending uniform in both, width and length, with the only difference that in case of the planar substrate the grain orientation changes smoothly

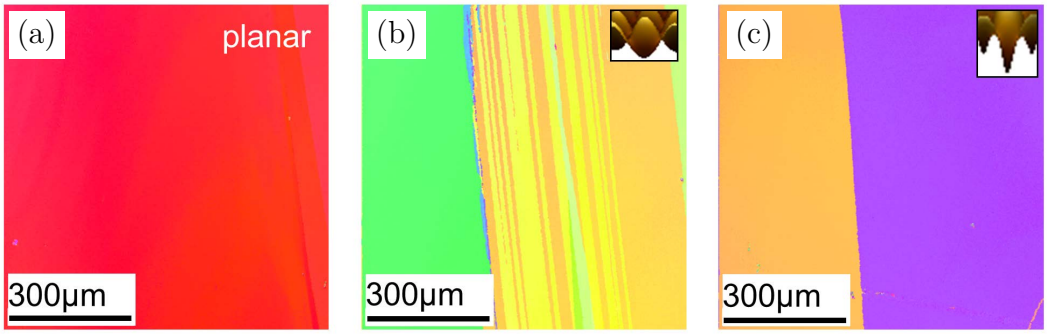


Figure 4.12: EBSD images of 10 µm thick silicon absorber layers on (a) a planar reference, (b) a round-valley sinusoidal structure, and (c) a 750 nm pitched steep-valley sinusoidal texture. AFM images of the corresponding substrate types are added as insets.

while there is an abrupt grain boundary in case of the steep-valley substrate. As in the last picture, a disturbed material quality is found for the round-valley substrate texture. The corresponding EBSD image reveals a fine grained area (alternating stripes of yellow and orange) next to a larger grain (displayed in green). Because of the contradiction to theory this behavior is attributed to a processing issue rather than a detrimental effect of the round-valley substrate texture as discussed before. Compared to the grain size measurements the areas analyzable with EBSD are rather small and can only give a hint on the material quality rather than providing a full quantitative description of the absorber layers.

4.5.2 Defect Density Analysis

To reveal defects in the silicon bulk, the silicon absorber layers were etched for 3 s with a wet-chemical Secco etch and SEM images were taken at three randomly chosen spots throughout the absorber layers in order to account for the large uniform grain size of the liquid phase crystallized silicon. For every substrate type introduced in figure 4.10 these three spots are depicted in figure 4.13.

On (a) the planar substrate, (c) the steep-valley sinusoidal substrate with a pitch of 750 nm, and (d) the 500 nm pitched steep-valley sinusoidal textured substrate two areas without or with only one defect line are observed. Only one out of the three areas observed per substrate features a high number of about 40 defect lines. A similar area of fine grained grain boundaries was observed on the round-valley sinusoidal structure during EBSD imaging. Taking into account the results obtained by the different analysis techniques applied, this suggests that high- and low-quality areas can be found on all absorber layers regardless of whether or not a textured

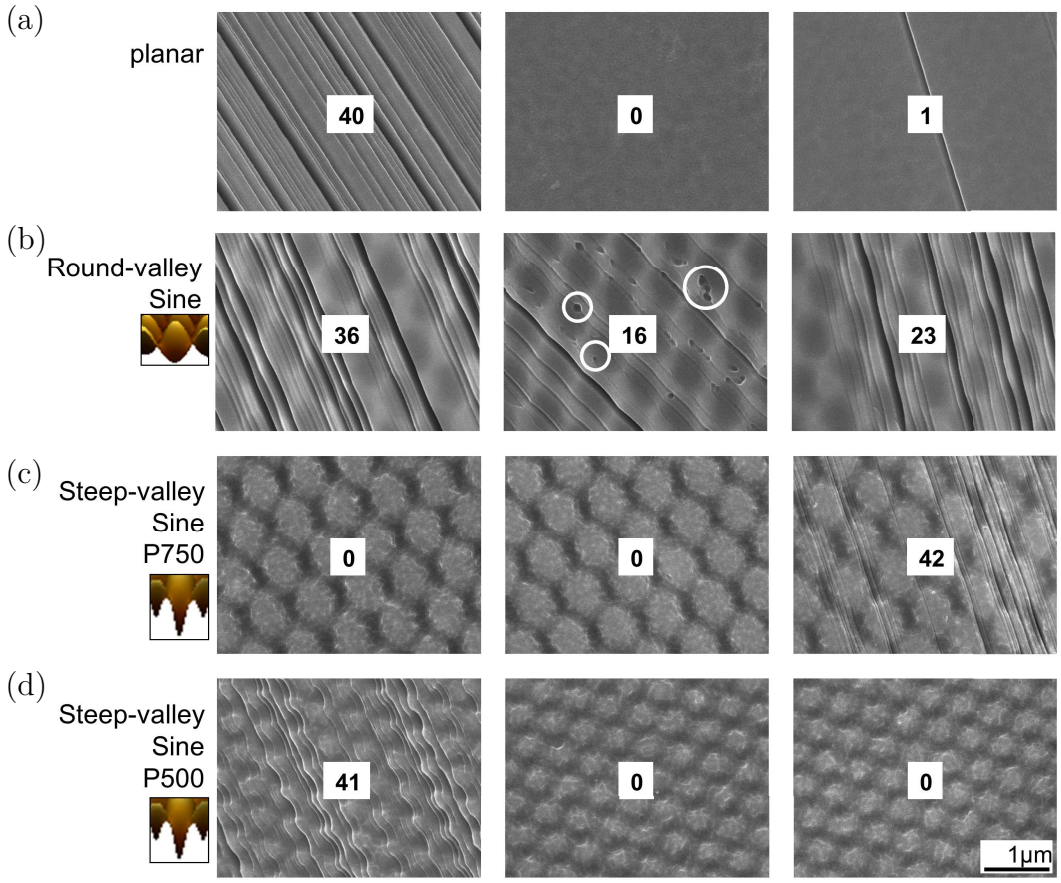


Figure 4.13: SEM images of 10 µm thick absorber layers after 3 s of wet-chemical Secco defect etching on (a) a planar substrate, (b) a round-valley sinusoidal textured substrate, (c) a steep-valley sinusoidal textured substrate with 750 nm pitch, and (d) a steep-valley sinusoidal textured substrate with 500 nm pitch. In addition to the sample names, AFM images of the corresponding substrate textures are depicted. The numbers in the pictures correspond to the number of defect lines present in the picture.

substrate is used. Overall, a high silicon material quality in terms of structural properties (grain size, defects in the silicon bulk) is achieved on the steep-valley sinusoidal textured substrates with rare occurrence of defect rich areas as it is similarly observed for the planar reference. Only for the silicon layer on the round-valley sinusoidal structure defect lines are observed in all three areas ranging from 16 to 36 defect lines suggesting that such defect lines occur throughout the entire silicon absorber layer. As only sample the round-valley sinusoidal features point defects, which area highlighted by circles in figure 4.13 (b). The result obtained by Secco etching are consistent with the results obtained by grain size and EBSD analysis revealing a high silicon material quality comparable to the planar reference on both steep-valley sinusoidal textures but a disturbed material quality on the round-valley structure.

By means of Raman spectroscopy further insight in silicon bulk material shall be gained. For all substrate types the peak height, related to the scattering ability of the structures, the peak position, related to stress inside the silicon layer, and the peak width, related to the crystallinity are examined in figure 4.14.

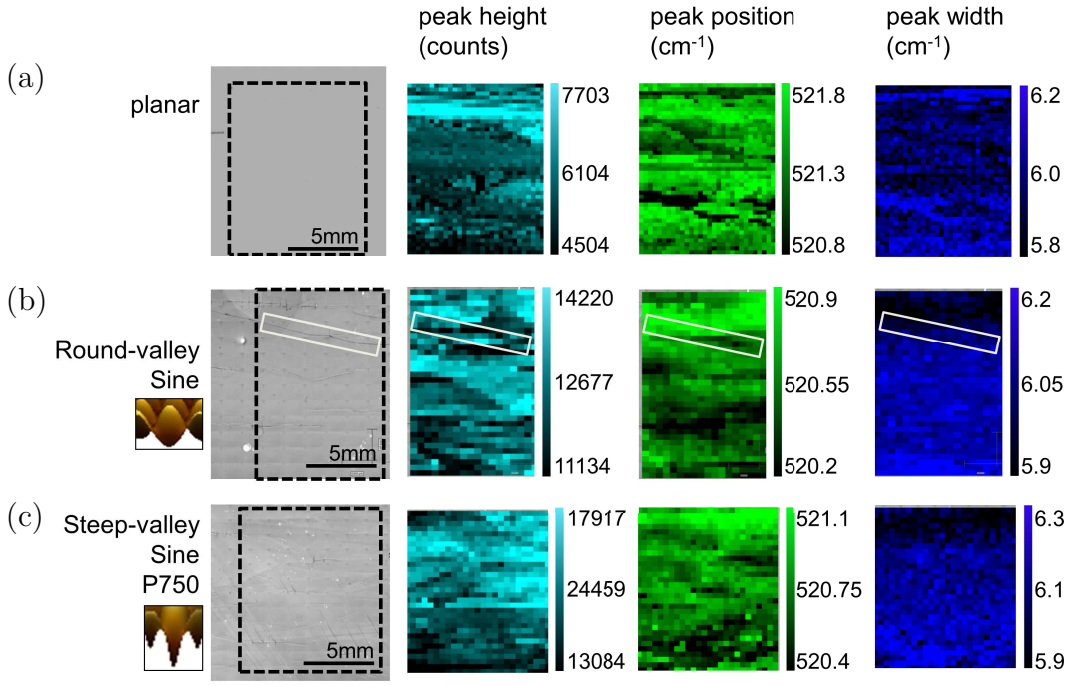


Figure 4.14: Light microscope images of (a) a planar sample, (b) a round-valley sinusoidal textured sample, and (c) a steep-valley sinusoidal textured sample with 750 nm pitch (P750). The areas scanned by Raman are marked by dashed rectangles. The resulting Raman peak height (cyan), peak position (green), and peak width (blue) are given. In (b) a grain boundary is highlighted by a white rectangle, which is also depicted in the corresponding Raman scans.

Considering the peak height (cyan), which corresponds to the measured intensity, the intensity of the textured substrates is up to one order of magnitude higher than of the planar substrate, which is depicted in figure 4.14 (a). This is attributed to the scattering ability of the textures. The laser wavelength of 735 nm and the texture period of 750 nm are similar and allow for interference enhancing the detected intensity. Among the textured samples the peak intensity is slightly higher for the steep-valley sinusoidal texture depicted in figure 4.14 (c), which is likely to be caused by the higher aspect ratio of 0.28 compared to the round-valley substrate texture with an aspect ratio of 0.23, which is depicted in figure 4.14 (b). In terms of peak position (green) all structures show only little variance regardless if the Raman scan is conducted on a single grain, as it is the case for the planar sample as well as the steep-valley sinusoidal textured sample, or over a grain boundary, which is highlighted by a white box in figure 4.14 (b). One reason that no changes are seen

if scanning over a grain boundary could be that the localized impinging laser spot, which is scanned over the sample, is diffracted at the hexagonal sinusoidal double-side texture, losing its local information. The detected signal corresponds to an average value of the area interfering with the refracted beam. Likewise, the peak width (blue) varies too little for changes to be observed throughout the samples. Moreover, not only no changes within one sample but also between the different samples are visible. Comparing the mean values for peak position and peak width, which are given additionally in the middle of the corresponding scale bars, these values differ by less than $1\,\mathrm{cm}^{-1}$ and by up to $0.1\,\mathrm{cm}^{-1}$, respectively. Thus, variations on one sample as well as between different samples lie within the measurement error of Raman spectroscopy. This suggests either that there is no difference in the silicon bulk quality regardless of which substrate type has been used or that the Raman analysis conducted is not sensitive enough to detect the defects in high-quality LPC silicon.

Before drawing the general conclusion that the same material quality as on a planar substrate can be achieved on sinusoidal textured substrates up to an aspect ratio of 0.28 for 750 nm pitches and 0.26 for 500 nm pitches, respectively, a more sensitive method, for which the signal is not disturbed by the substrate texture, should confirm these results. One possibility are TEM images investigating the stress in the absorber layer region close to the textured substrate-silicon interface as it was applied to identify dislocation lines arising of the steep texture flanks of the square lattice texture with an aspect ratio of 0.5 causing the material quality to decline [59].

In summary, the analysis of the LPC silicon material quality on textured substrates was conducted by means of grain size analysis, EBSD, Secco defect etching, and Raman characterization. None of the methods applied was able to identify statistically relevant structural differences neither between textured and planar absorber layers nor between different texture geometries. From literature the beneficial effect of smooth texture flanks and detrimental effect of steep texture angles on the silicon material quality are known in other silicon thin-film solar cell types. A similar effect could not be confirmed for LPC silicon. Hint for a declined material quality was solely found for the wide-angled (round-valley) sinusoidal texture with comparable low aspect ratio, which was attributed to a processing issue rather than an effect of the substrate texture. Nonetheless, a detrimental effect of steep texture flanks was demonstrated in case of the pillar shaped structure (chapter 4.3). Based on IQE analysis (figure 4.8) a higher material quality of the planar absorber layers compared to textured devices was demonstrated. Either the methods applied char-

acterizing the LPC silicon material quality are not sensitive enough, as discussed before, or LPC silicon recrystallizing from its melt is not influenced by the shape of the substrate texture. In this case, the detrimental effect demonstrated by IQE analysis can be ascribed to enhanced surface recombination on textured substrates. The latter could be addressed by a systematic interlayer thickness study or changing the interlayer deposition method to PECVD methods possibly enabling closed interlayers despite being deposited on texture flanks. This could enable the desirable enhanced passivation properties. However, whether a surface enhancement of around 6 % [figure 7.1 (b)] is pronounced enough to attribute the declined IQE to a pure enhancement of the surface recombination velocity is unclear. For clarification electrical simulations would be desirable. Overall, in future work the result of a comparable material quality of planar and textured LPC silicon absorber layers should be confirmed by methods sensitive enough for LPC silicon. Suitable methods could be TEM investigations [59] or an adapted QSSPC method [190].

4.6 Conclusion

Based on the results of previous work [58, 185, 186] and literature [39–41] a one-dimensional line grating with a pitch of 690 nm and an aspect ratio of 0.2 was developed as model texture to investigate the interplay between substrate textures and the liquid phase crystallization (LPC) process of 10 µm thick silicon absorber layers. The resulting silicon absorber layer material quality was analyzed in dependency on the crystallization and crystal growth direction with respect to the line grating direction for three different angles (0°, 45° and 90°) finding that the crystal growth direction in laser scanning direction was preserved despite the differently orientated substrate textures. A similar material quality reflected by large uniform silicon grains alternated with areas exhibiting a high grain boundary density was obtained regardless of the scanning direction. This corresponds to the material quality realized on a planar absorber layer and proofs the suitability of a substrate texture pitch of around 700 nm with an aspect ratio of 0.2 for texturing in LPC silicon thin-film solar cells. The expertise gained was used to identify suitable crystallization parameters for more sophisticated two-dimensional substrate textures.
A 750 nm pitched hexagonal pillar substrate textures with an aspect ratio of 0.2 was developed and analyzed regarding its suitability for implementation into LPC silicon thin film solar cells on glass. In comparison to the square lattice structure developed by Preidel [58], the pillar structure offered vital optical anti-reflective properties. The pillar structure exhibited an impaired electronic material quality

caused by the steep texture flanks as also shown for the square lattice structure [59]. Thus, in case of a 750 nm pitched hexagonal pillar structure no suitability for LPC silicon thin-film solar cells was found despite enhanced optical properties.
Subsequently, a structure with similar feature sizes as the pillar shaped texture but smooth texture flanks, the sinusoidal texture, was developed. The sinusoidal substrate texture preserved the optical anti-reflective properties of the pillar structure despite the smoothed texture flanks. The external quantum efficiency of the sinusoidal textured device could be enhanced compared to pillar and square lattice textured devices and compared to a state-of-the-art planar reference device with exception of a wavelength range between 400 nm and 700 nm.
For all substrate texture types the behavior of the EQE curves could be correlated to the amount of defects present in the silicon absorber layer being grown and crystallized on the respective substrate textures. IQE analysis revealed a declined internal quantum efficiency of the sinusoidal textured device compared to the planar reference, especially for wavelengths shorter than 500 nm, which are absorbed close to the textured front interface. For longer wavelengths the IQE of the sinusoidal textured device increases. In addition, by Secco and LBIC analysis a comparable defect density was found on sinusoidal and planar devices. The combination of both implied that the decline of the EQE curve for the wavelength range discussed is rather an interface than a bulk property. If this is the case, the decline in IQE and EQE of the sinusoidal textured device can be attributed to an increased surface recombination velocity at the textured and, hence, surface enhanced front interface. This conclusion was supported by a detailed silicon material quality analysis on different sinusoidal textured substrates. Based on the methods applied, no detrimental influence of 750 nm or 500 nm pitched sinusoidal substrate textures compared to a planar reference device could be identified.
Therefore, the sinusoidal substrate texture was chosen for further experiments as most promising approach unifying enhanced optical properties with the required silicon material quality.

5 Optical Properties of Sinusoidal Nano-Textures

Sinusoidal substrate textures have proved suitable for implementation into LPC silicon thin-film solar cells. They provide vital anti-reflective properties and the required silicon material quality. In the scope of this chapter the full optical potential of sinusoidal textured absorber layers shall be exploited. Every layer constituting the optical stack is systematically varied and the relevant optical properties are analyzed. A schematic sample stack is depicted in every paragraph highlighting the varied part by a horizontal arrow.

In subchapter 5.1 the influence of the sinusoidal substrate texture geometry, namely of the pitch (P) and the height (h), on the absorption behavior of 10 µm thick LPC silicon layers is demonstrated. The comparison of experimentally and numerically obtained results was subject of a previous publication [191].

Subchapter 5.2 highlights the influence of the SiN_x / SiO_x interlayer stack and the silicon absorber layer thickness on the optical properties of LPC absorber layers being grown and crystallized on sinusoidal textured substrates with a fixed pitch of 750 nm and an aspect ratio of 0.2–0.25. This part of the chapter is based on a previous publication referenced as [192].

In subchapter 5.3 the sinusoidal substrate-silicon interface texture is combined with additional light management approaches at the air-glass interface and silicon rear side in order to address remaining reflection and transmission losses. Parts of these results are published in [193]. The application of the sinusoidal texture to the air-glass interface of planar LPC devices was analyzed as part of a previous publication [194].

5.1 Influence of the Sinusoidal Substrate Feature Sizes

In order to examine the influence of the sinusoidal texture pitch, samples with a fixed aspect ratio of around 0.24 and varied pitches (P) of 500 nm ("Sine P500") and 750 nm ("Sine P750") are compared to a state-of-the-art planar reference. For both pitches samples with and without additional anti-reflexive SiN_x layer were prepared. The samples solely coated with a SiO_x interlayer illustrated the pure influence of the substrate's pitch on the optical properties without the influence of an additional anti-reflective coating. The samples with SiN_x / SiO_x interlayer stack represent absorber layers intended for implementation in LPC solar cell devices. The optical properties of all devices are analyzed in figure 5.1.

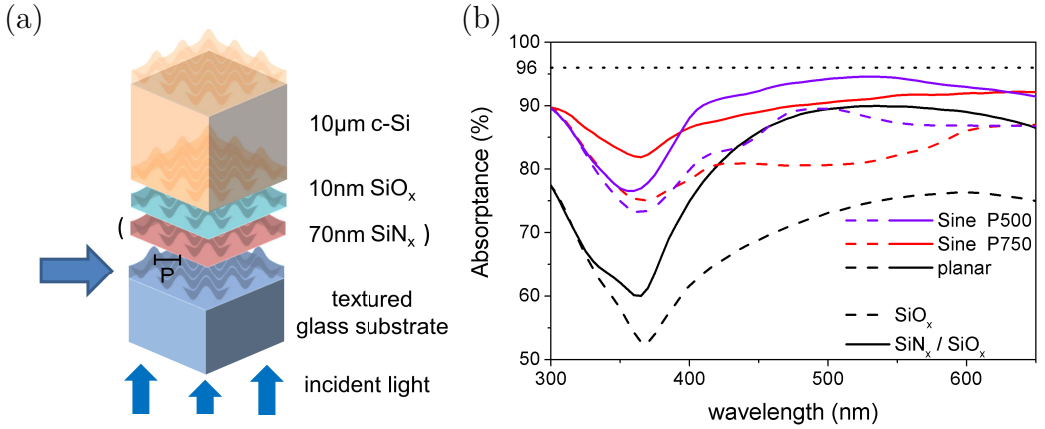


Figure 5.1: (a) Schematic of the sample stacks under investigation. The varied part, the pitch (P) of the textured glass substrate, is highlighted by a horizontal arrow. (b) Absorptance of a planar state-of-the-art reference (black), sinusoidal nano-textures with 500 nm pitch (Sine P500, purple) as well as with 750 nm pitch (Sine P750, red), respectively. Samples with SiO_x interlayer are plotted in dashed lines, while samples with a SiN_x / SiO_x interlayer (IL) stack are plotted in solid lines. At 96 % a dotted line is added as guideline to mark the 4 % reflection loss of incident light at the air-glass interface.

Comparing the samples without additional anti-reflective SiN_x layer (dashed lines) it is found that both textured samples, Sine P500 (purple) and Sine P750 (red), enhance light absorption compared to the planar reference (black). Best anti-reflective properties corresponding to the highest absorption enhancement (chapter 3.2), are found for the 500 nm pitched sinusoidal structure. Despite absolute differences becoming smaller, this trend is preserved when adding an additional anti-reflective SiN_x layer to the sample stack (solid lines). The Sine P500 sample without SiN_x layer (purple, dashed) performs as good as a planar reference (black, solid) featuring an optimized SiN_x anti-reflective layer. Adding a SiN_x layer to a 500 nm pitched sinu-

soidal textured sample stack (purple, solid) enables absorption close to 96 % (dotted line) over a broad wavelength range. Since 4 % of the incident light are directly lost at the air-glass interface, this 96 % serve as an upper achievable boundary neglecting any other loss mechanism in the device. For wavelengths longer than about 640 nm the larger 750 nm pitched sinusoidal sample starts to outperform the smaller 500 nm pitched sample. In this part of the spectrum absorption enhancement originating from the front interface texture is superimposed by light being partially scattered back into the device at the rear side texture. Since only light with wavelengths longer than the penetration depth can reach the rear side of the silicon absorber layer, it is expected from geometrical optics that light scattering at the rear side is more pronounced for the lager pitch with higher and broader structure features.

In order to allow for a more quantitative analysis, mean absorptance values are calculated for the wavelength range of interest and summarized in table 5.1.

Table 5.1: Optical properties of the samples depicted in figure 5.1. For each sample the aspect ratio, the interlayer stack and mean absorptance in the wavelength range from 350 nm to 600 nm are listed.

Sample and Pitch	Aspect Ratio	Interlayer	Mean Absorptance 350 nm – 600 nm (%)
planar	–	SiO_x	68.7
planar	–	SiN_x / SiO_x	82.6
Sine P500	0.23	SiO_x	84.5
Sine P500	0.24	SiN_x / SiO_x	90.5
Sine P750	0.23	SiO_x	80.7
Sine P750	0.24	SiN_x / SiO_x	88.8

For samples featuring solely a SiO_x interlayer texturing the silicon absorber layer with a 500 nm pitch sinusoidal texture with an aspect-ratio of 0.23 increases mean absorption by 15.8 % (absolute) with respect to the respective planar reference device and by 3.8 % (absolute) with respect to a sample with same aspect-ratio but 750 nm pitch. When adding 70 nm SiN_x anti-reflection coating to the planar reference, as it is commonly featured in state-of-the-art planar devices [86], absorptance is enhanced by 13.9 % to a mean absorptance of 82.6 % in the wavelength range of interest. Indeed, the 500 nm pitched sinusoidal texture without additional anti-reflective coating exceeds the planar reference featuring a SiN_x layer by 1.9 % (absolute). Texturing the absorber layer enhances absorption more effectively than using a state-of-the-art anti-reflective coating in a planar device. Since sinusoidal textured glass substrates already provide anti-reflective properties, the effect of adding a SiN_x coating to textured devices is less pronounced than in the planar case. Nevertheless, the 750 nm

pitched device gains 8.1 % (absolute) and the 500 nm pitched device gains 6 % (absolute) resulting in the highest mean absorptance achieved of 90.5 %. Comparing the samples featuring an anti-reflective SiN_x coating the 750 nm pitched sample enhances mean absorptance by 6.2 % (absolute), while the 500 nm pitched sample enhances mean absorptance by 7.9 % (absolute) compared to the planar reference. The superior anti-reflective properties of the 500 nm pitched sample were predicted by simulations of Lockau *et al.* [185] and Jäger *et al.* [72] revealing an optimum range of pitches between 500 nm and 600 nm for anti-reflection properties in LPC-Si thin-film solar cells on glass substrates at the glass-silicon interface.

In order to investigate the impact of the structure height (h) on the optical properties of 10 µm thick LPC silicon absorber layers, sinusoidal textured substrates with 500 nm and 750 nm pitch (P) and systematically varied aspect ratios (h/P) between 0.05 and 0.28 were prepared. To study solely the effect of the texture height without superposition of other anti-reflective measures, this paragraph only features samples without SiN_x anti-reflection coating. The resulting devices are analyzed by means of optical spectroscopy in figure 5.2 and compared to theoretical results obtained by optical simulations (figure 5.3) using a 3D time-harmonic finite-element Maxwell solver [191] in figure 5.4.

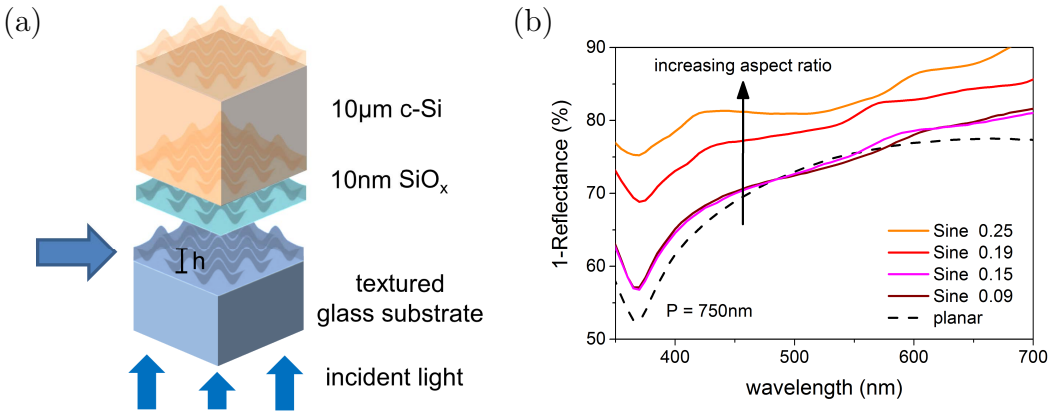


Figure 5.2: (a) Schematic of the sample stacks under investigation. The varied part, the height (h) of the textured glass substrate, is highlighted by a horizontal arrow. (b) Absorptance, measured as 1-reflectance, of sinusoidally textured 10 µm thick LPC silicon absorber layers with varying aspect ratios (numbers are given in the figure according to the colors) in comparison to a planar reference (black, dashed).

Figure 5.2 (b) reveals a trend of decreasing reflection losses with increasing aspect ratios. The anti-reflective effect and, hence, absorption enhancement rises slowly up to an aspect ratio of 0.15 (brown and magenta). For higher aspect ratios (red and orange) the trend of increase in absorption with increasing aspect ratio is more

pronounced. This result suggests that increased aspect ratios are beneficial for increasing the optical properties of LPC silicon absorber layers.

These results played a vital role in adapting an optical 3D FEM simulation algorithm [72] for usage to gain insight into experimental results. Agreement between simulation data and experimental data was achieved when considering not only reflection at the textured glass substrate-silicon interface but also reflection at the glass-air interface [191].

In order to explain the trend of decreasing reflection loss with increasing aspect ratio such numerical calculations are used to simulate reflection at the sinusoidal textured substrate-silicon interface. Schematics in figure 5.3 (a) and (b) illustrate the conducted simulations. The respective result is depicted in figure 5.3 (c).

In figure 5.3 (a) the object of the simulations, the fraction of incident light being reflected at the textured glass-silicon interface, is indicated by a red arrow. The result of the optical simulations, which are in detail described in Jäger *et al.* [191], is schematically depicted in figure 5.3 (b) for a wavelength of around 400 nm. While in the calculations up to five diffraction orders are considered, the graphs only include diffraction orders up to the 3$^{\text{rd}}$ order for clarity reasons. After reflection at the glass-silicon interface all simulated diffraction orders are present in the glass substrate. The angles, in which the reflected light propagates in the glass substrate towards the glass-air interface increase with increasing diffraction order (please refer to eq. 11 in reference [72]). At the glass-air interface, determined by the critical angle (black, dashed line) of around 41° (equation 2.4), the different diffraction orders are either refracted out of the device (ii), as it is the case for the 0$^{\mathbf{th}}$ (blue) and 1$^{\mathbf{st}}$ (green) diffraction order, or reflected back towards the silicon absorber layer (iii), as it is the case for the 2$^{\text{nd}}$ (red) and 3$^{\text{rd}}$ (third) diffraction order. Therefore, the amount of light in the 0$^{\text{th}}$ (orange) and 1$^{\text{st}}$ (green) diffraction orders add to the reflection losses of the device, while the 2$^{\text{nd}}$ (red) and 3$^{\text{rd}}$ (third) diffraction orders constitute to the amount of light being absorbed.

Figure 5.3 (c) depicts the numerically determined energy distribution in different diffraction angles in dependence on the aspect ratio of a 750 nm pitched sinusoidally textured sample. Below an aspect ratio of 0.1 all energy is carried in the 0$^{\text{th}}$ (blue) and 1$^{\text{st}}$ (green) diffraction orders. With increasing aspect ratio the energy distribution in the different diffraction orders shifts towards higher diffraction orders. At the glass-air interface the amount of light lost by scattering out of the device being present in the 0$^{\text{th}}$ (blue) and 1$^{\text{st}}$ (green) diffraction order is reduced with increasing aspect ratio. Likewise, the amount of light in the 2$^{\text{nd}}$ (red) and 3$^{\text{rd}}$ (orange)

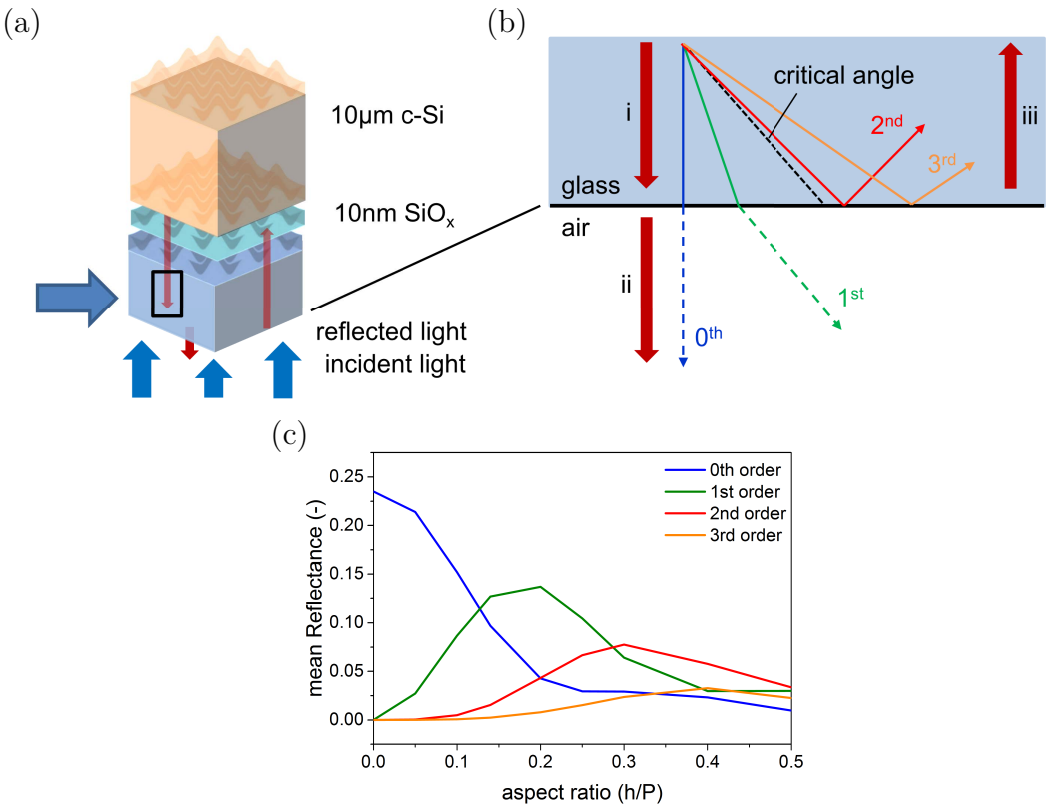


Figure 5.3: (a) Schematic of the sample stack. The object of the simulations, the fraction of incident light being reflected at the textured glass-silicon interface, is indicated by red arrows and highlighted by a horizontal arrow. (b) Schematic of the different diffraction angles ($0^{\mathbf{th}}$ to $3^{\mathbf{rd}}$ order are depicted) of light encountering the glass-air interface under different angles for a wavelength of around 400 nm. The reflected diffraction orders encountering the glass-silicon interface (i) are, determined by the critical angle (black, dashed line), either scattered out of the device (ii) or reflected back towards the silicon absorber layer (iii). Light propagating in the glass substrate is depicted with solid lines while light propagating in air is depicted in dashed lines. (c) Numerically determined energy distribution into different diffraction angles in dependence on the aspect ratio of a 750 nm pitched sinusoidal textured sample.

diffraction order, which is reflected back into the device towards the silicon absorber layer, is enhanced. Following as a consequence, reflection losses are reduced with increasing aspect ratio. For high aspect ratios the amount of light being still present in the 0^{th} and 1^{st} diffraction order stabilizes around 4 % in total. These 4 % add to the total reflection loss of the device, unavoidable in a device design featuring a glass substrate and a 750 nm (or 500 nm [191]) pitched sinusoidal textured glass-silicon interface.

An extended study of the influence of the influence of the aspect ratio on the optical properties of 750 nm and 500 nm pitched sinusoidal textured absorber layers in comparison to results obtained by simulations is presented in figure 5.4.

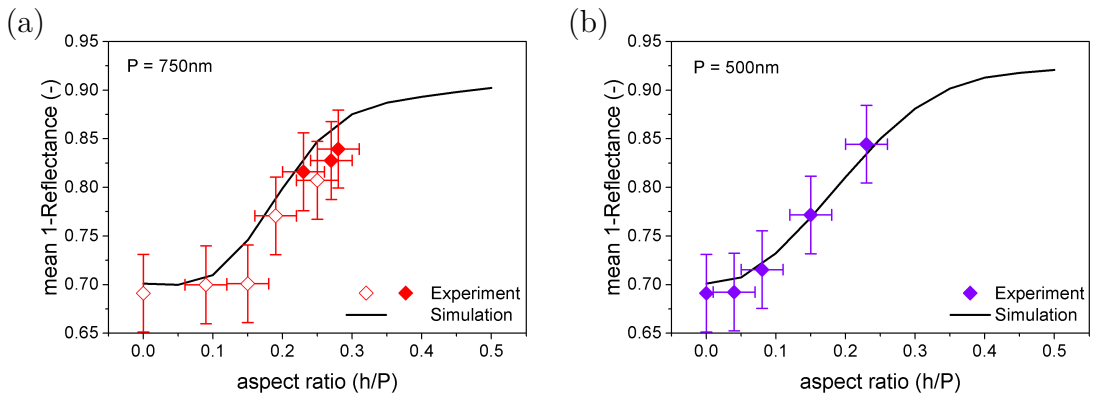


Figure 5.4: Mean absorptance values, measured as 1-reflectance and averaged over a wavelength range of 350 nm to 600 nm, obtained by experiment compared to simulations for sinusoidal textured absorber layers with a pitch of (a) 750 nm and (b) 500 nm. Data points obtained from figure 5.2 (b) are represented by open symbols while additional data points are represented by filled symbols.

For both pitches the values obtained by experiment closely follow the simulated curves in figure 5.4 (a + b). In figure 5.4 (a) only the value obtained by the sample with a pitch of 750 nm and an aspect ratio of 0.15 [magenta in figure 5.2 (b)] seems to be slightly lower than predicted by the simulation. This deviation can probably be attributed to inaccuracies in the production process of this sample, e.g. in the height determining step by AFM or thickness inhomogeneities in the imprint or interlayer stack. In figure 5.4 (b) and table 5.1 the trend of increasing absorptance with increasing aspect ratio is reproduced for a second pitch of 500 nm. In agreement with figure 5.1 (b) slightly higher absorptance values are found for 500 nm pitched sinusoidal textured samples than for 750 nm pitched sinusoidal textured samples. In general, the agreement between simulation and experimental results not only validates the experimental results but also allows drawing conclusion from the reflectance measurements to the structures' feature height via the simulation. Since the match of experimental and simulated results was demonstrated here, simulations can be used for explanation and prediction of experimental results. Aspect ratios higher than 0.3 were not obtained by experiment due to shrinkage of the sol-gel layer (chapter 3.1). The simulations allow for predicting the further development of the experimental curve even beyond the experimentally reachable values. From the simulation data it can be stated that absorption further increases with increasing aspect ratio. For aspect ratios larger 0.4 the slope of the absorption curves starts to decline. In total, an S-shaped curve is obtained for the absorptance behavior in dependence on the aspect ratio. It is unclear, however, if a further increase in aspect ratio beyond 0.3 would lead to a declined electronic material quality as it was observed for the 2 µm pitched square lattice sample of Preidel *et al.* featuring

an aspect ratio of 0.5 [59]. For both pitches observed, the highest possibly achievable absorptance values stagnate at around 92 %. The remaining 8 % reflection loss constitute of the 4 % remaining reflection loss revealed in figure 5.3 (c) as well as of the 4 % reflection directly lost when light impinges on the air-glass interface for the first time (equation 2.6).

In summary, these results explain the shape of the experimentally obtained absorptance behavior in dependence on the aspect ratio of the sinusoidal 750 nm pitched substrates depicted in figure 5.2 (b). For aspect ratios below 0.1 almost all energy is featured in the lower 0^{th} and 1^{st} diffraction orders encountering the glass-interface under an angle which allows the light to escape the device. For aspect ratios exceeding 0.1 the amount of energy being diffracted into higher orders, which are reflected back into the device at the glass-air interface, steadily increases. For higher aspect ratios absorption in the silicon absorber layer increases with increasing aspect ratio. For aspect ratios larger than 0.4 the absorption increment declines and stabilizes at around 92 % for an aspect ratio of 0.5, with 4 % reflection loss at the air-glass interface and 4 % remaining reflection loss at the textured glass-silicon interface. With an experimentally obtained absorptance of 90.5 % the optical potential of silicon absorber layers on sinusoidal textured glass substrate is almost fully exploited if a 500 nm pitch is used. Nevertheless, further analysis is restricted to 750 nm pitched sinusoidal structures because these have proven to be better suited for integration into LPC-Si solar cells (chapter 6).

5.2 Influence of Interlayers and Silicon Absorber Layer Thicknesses

The optical properties of a layer stack are influenced by every layer forming the optical stack. The 70 nm SiN_x, 10 nm SiO_x interlayers as well as the 10 µm silicon absorber layer deposited subsequently to texturing the substrate are varied systematically by keeping two layer thicknesses fixed and varying one layer thickness in order to optimize the optical properties of the sample stack.

For wavelengths shorter than 450 nm figure 5.5 (b) reveals decreasing reflection losses with decreasing SiN_x interlayer thickness. The lowest reflection losses are found for the thinnest barrier (50 nm, dark blue) and the highest reflection losses are found for the thickest barrier (80 nm, orange). For longer wavelengths this trend inverts and the highest reflection losses are found for the thinnest barrier while for all other

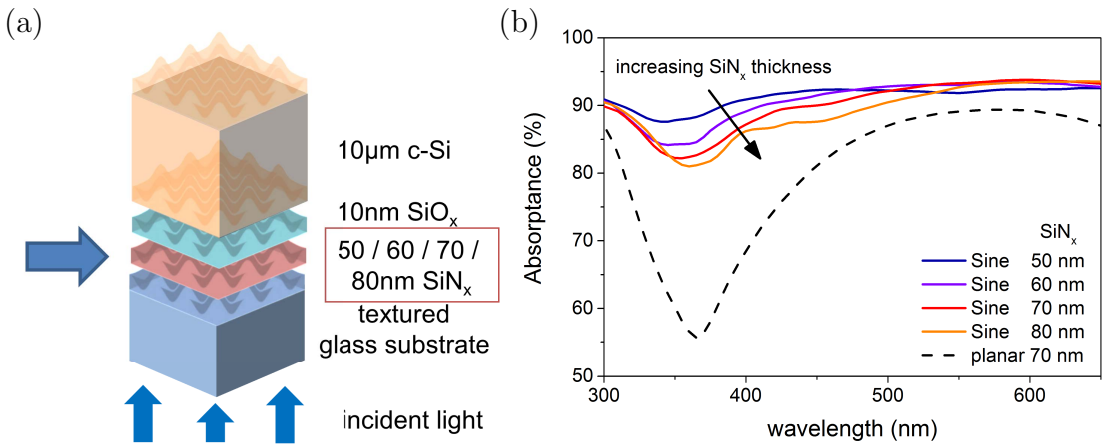


Figure 5.5: (a) Schematic of the sample stacks under investigation. The varied part, the SiN_x layer, is highlighted by a horizontal arrow. (b) Absorptance of sinusoidally textured 10 µm thin c-Si absorber layers with varying SiN_x interlayer thicknesses (numbers are given in the figure according to the colors) in comparison to a planar reference (black).

barrier thicknesses no pronounced differences can be distinguished. If comparing the 60 nm and 70 nm interlayer thicknesses, the 70 nm barrier (red) features slightly higher reflection losses than the 60 nm barrier (purple) for wavelengths shorter than 500 nm. For longer wavelengths the reflection losses of the thinner barrier are slightly higher, such that, if the entire wavelengths range is considered, no clear difference between these two SiN_x barrier thicknesses can be identified. Both medium interlayer thicknesses (60 nm and 70 nm) are equally suited for absorption enhancement in LPC-Si solar cell devices.

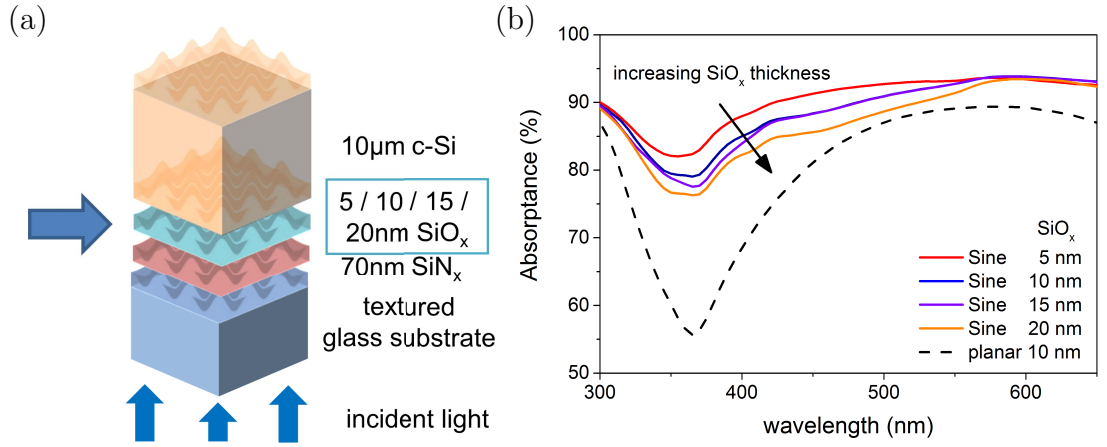


Figure 5.6: (a) Schematic of the sample stacks under investigation. The varied part, the SiO_x layer, is highlighted by a horizontal arrow. (b) Absorptance of sinusoidally textured 10 µm thin c-Si absorber layers with varying SiO_x interlayer thicknesses (numbers are given in the figure according to the colors) in comparison to a planar reference (black).

For the SiO_x layer thickness variation, which is depicted in figure 5.6 (b), differences regarding the optical absorption behavior are only found for wavelengths shorter than 550 nm. In this spectral range reflection losses increase with increasing SiO_x thickness. For implementation into LPC silicon thin-film solar cells the thinnest SiO_x barrier (5 nm, red) is favorable. The study was not extended to lower SiO_x thicknesses because these are known to degrade the electronic properties of a solar cell [20]. If using a textured substrate a too thin barrier bears the risk of not being closed and, hence, of insufficient passivation.

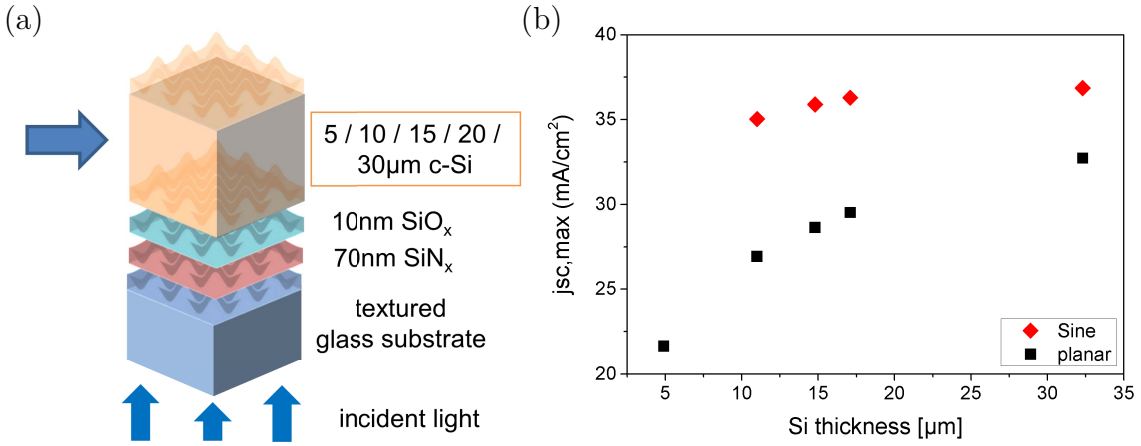


Figure 5.7: (a) Schematic of the sample stacks under investigation. The varied part, the Si absorber layer, is highlighted by a horizontal arrow. (b) Maximum achievable short circuit current density ($j_{sc,max}$) calculated from absorptance spectra for a wavelength range from 280 nm to 1100 nm of sinusoidally textured c-Si absorber layers (diamond, red) as a function of varying silicon absorber layer thicknesses in comparison to planar references (square, black).

Figure 5.7 (b) depicts the absorption behavior of different silicon absorber layer thicknesses on sinusoidal textured substrates (diamond, red) and corresponding planar reference substrates (square, black). In order to allow for a comprised comparison the maximum achievable short-circuit current density ($j_{sc,max}$) was calculated based on the measured absorption data according to equation 3.1. At 5 µm silicon thickness the data point of the sinusoidal texture is missing because this sample suffered from delamination during crystallization. At all remaining silicon thicknesses an absorption enhancement is found compared to the respective planar reference if a sinusoidal textured substrate is used. At a silicon thickness of 15 µm the sinusoidal texture rises the maximum achievable short-circuit current density of the planar reference of 28.6 mA cm^{-2} by 7.3 mA cm^{-2} to 35.9 mA cm^{-2}. A doubling of the absorber layer thickness to 30 µm yields an $j_{sc,max}$ increase of 4 mA cm^{-2} for the planar sample and of 1.5 mA cm^{-2} for the textured sample. Independent of the substrate

type used, absorption increases with increasing silicon absorber layer thickness due to the rising absorption depth [figure 2.1 (a)] allowing for an increased electron-hole pair generation in the NIR range of the spectrum. A larger amount of long wavelength light is absorbed during the first path, before it reaches the rear side of the absorber layer reducing the light trapping advantage of the sinusoidal rear side texture compared to a planar rear side. In addition, with increasing amount of silicon deposited on top of the textured substrate the rear side texture of the double-sided textured absorber layer flattens causing a reduced scattering ability. Nevertheless, when choosing an appropriate silicon thickness, absorption enhancement has to be balanced with processing time and cost considerations. An absorber layer thickness of 15 µm is a reasonable compromise between enhancing absorption and a low material consumption. Silicon absorber layer thicknesses of around 15 µm have already demonstrated their compatibility with the LPC process as well as their suitability for integration into LPC silicon thin-film solar cells [21].

In summary, based on the results presented in this chapter, optimized optical properties of textured and planar LPC silicon absorber layers were found using interlayer thicknesses of SiN_x 60 nm to 70 nm / SiO_x 5 nm and an absorber layer thickness of 15 µm. From an optical point of view these layer thicknesses are recommended for future LPC silicon solar cell designs irrespective of whether or not a textured substrate is used.

5.3 Addressing Remaining Optical Losses with Additional Measures for Light Management

To further enhance light incoupling into the device, texturing of the glass-silicon interface can be combined with additional measures for light management. This additional light management approaches are intended to minimize remaining reflection losses at the front and remaining transmission losses at the rear side of double-sided textured LPC silicon absorber layers on 750 nm pitched sinusoidal textured glass substrates. Different wavelengths demand for differently sized light scattering structures. At the front side of the silicon absorber layer small pitches are needed to scatter the short wavelengths and reduce reflection losses of incident light. Only the longer wavelengths manage to travel to the rear side of the absorber layer without being absorbed. At the rear side of the silicon absorber layer large pitches are needed to scatter the long wavelengths (chapter 2.1.2). Common examples, also used in planar LPC silicon thin film devices [43, 124, 195, 196], are applying

pyramidal rear side textures, back reflectors, and texturing the light-facing air-glass interface. The concept of separately optimized light scattering structures at different interfaces has successfully been applied to other silicon thin film solar cell types [29, 74, 75, 197, 198].

For LPC-Si silicon thin film solar cells a pyramidal rear side texture was developed contributing to a cell efficiency of 12.1 % [43] featuring a planar substrate-silicon interface. A suitable front silicon texture is developed within this thesis, the sinusoidal nano-texture. The optical potential of the combined approach, a sinusoidal front and a pyramidal rear texture, is depicted in figure 5.8.

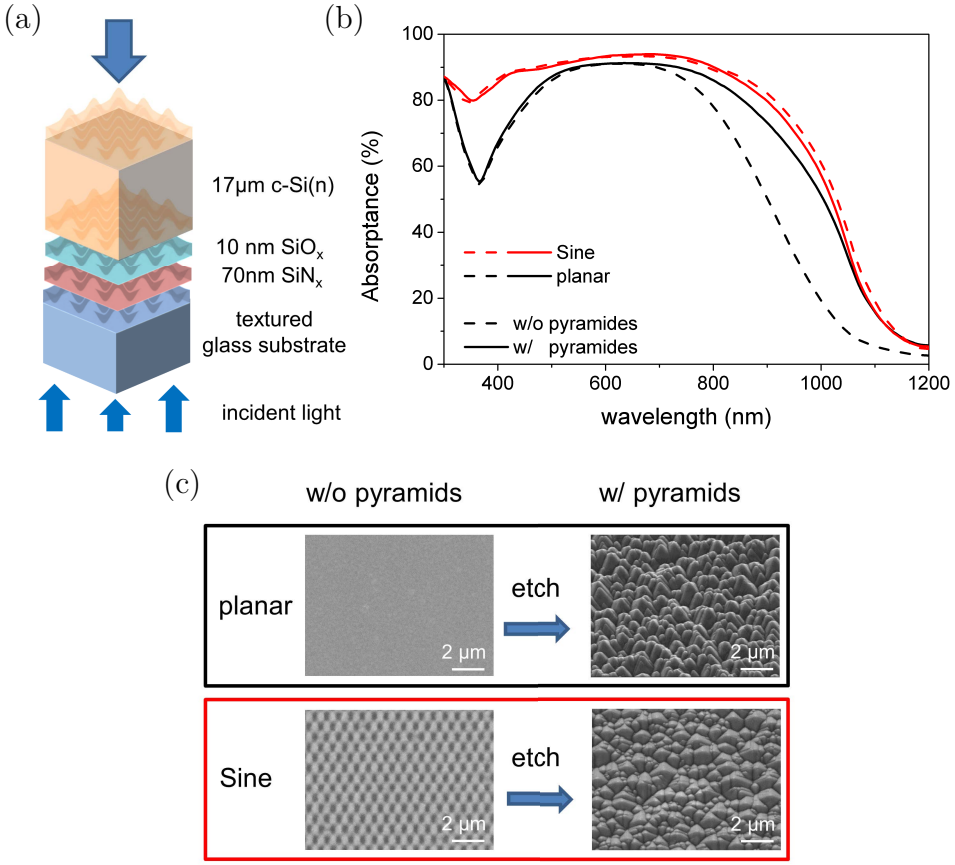


Figure 5.8: (a) Schematic of the sample stacks under investigation. The varied part, the silicon rear side texture, is highlighted by a vertical arrow. (b) Absorptance spectra of 17 µm c-Si absorber layers with (solid lines) and without (dashed lines) pyramidal rear side texture for a sinusoidal textured layer (red, aspect ratio $h/P = 0.19$) in comparison to a planar reference (black). (c) Respective SEM images of the rear side of the silicon absorber layer before and after KOH etching.

The absorptance spectrum of a sinusoidal double-sided textured silicon absorber layer (red, dashed) exceeds the spectrum of the planar reference (black, dashed) over the entire wavelength range. In terms of maximum achievable short-circuit current density an enhancement of 6.5 mA cm^{-2} from 29.5 mA cm^{-2} in the planar

case to 36.0 mA cm^{-2} in the sinusoidal double-sided textured case is obtained. This absorption enhancement in the double-sided sinusoidal textured device is based on an increased incoupling of light due to an anti-reflective effect at the front side (chapter 5.1) as well as a light scattering effect at the rear side. An increased light path through the silicon absorber layer results enabling enhanced photo-generation of electron-hole pairs.

Applying a pyramidal rear-side texture (solid lines) to both, the double-sided textured silicon absorber layer as well as the planar layer stack, no change of the spectra in the short wavelength range is found because only the longer wavelengths can reach the altered back side of the absorber layer. In the long wavelength regime the difference between the front sinusoidal – rear pyramidal textured sample (red) and the front planar – rear pyramidal textured sample (black) is diminished compared to devices without additional pyramidal texture. Nevertheless, with a sinusoidal front side texture an absorption enhancement corresponding to an enhancement of 2.0 mA cm^{-2} from 33.4 mA cm^{-2} in the planar case to 35.4 mA cm^{-2} in the sinusoidal textured case is achieved. If comparing devices with same front interface, applying a pyramidal rear-side texture to a planar 17 µm thick LPC silicon absorber layer enhances the maximum achievable short-circuit current density by 3.9 mA cm^{-2}. Applying a pyramidal rear-side texture to a sinusoidal double-sided textured 17 µm thick LPC silicon absorber layer decreases the maximum achievable short-circuit current density by 0.5 mA cm^{-2}.

By SEM imaging, depicted in figure 5.8 (c), no difference in the rear side pyramids between the planar sample (black) and the formerly double-sided sinusoidal textured sample (red) is found. This confirms that a sinusoidal rear side texture with a pitch of 750 nm and an aspect ratio below 0.25 does not disturb the pyramidal etching process. Insufficient etching can be excluded as cause for the diminished absorption enhancement in the long wavelength range for the sinusoidal textured device. Another reason might be the material removed from the silicon absorber rear side during the etching process. While in the planar case the gain in absorptance caused by the rear side texture is pronounced enough to compensate for the loss of absorber layer material, in the sinusoidal textured case this material loss outweighs the optical benefits. Furthermore, in case of the sinusoidal textured device incident light is already scattered at the textured front side of the silicon absorber layer which alternates the light path within the absorber layer compared to a planar front interface. The scattered light might approach the steep pyramidal rear side texture flanks at angles favorable for scattering the light outside the absorber layer instead of reflecting it back into the device (compare reference [80]).

In summary, applying pyramidal rear side textures to planar and sinusoidal textured devices with a silicon absorber layer thickness of 17 µm leads to $j_{sc,max}$ values of 33.4 mA cm^{-2} and 35.4 mA cm^{-2}, respectively. While the pyramidal texture is well suited to enhance absorption in a planar device, it decreases the optical performance of a double-sided sinusoidal textured device. The decline of absorption if a sinusoidal front side texture is combined with a pyramidal rear side texture highlights that in the scope of future work deeper understanding of the optical light path inside textured absorber layers has to be gained on a wave optic point of view. This will be key prerequisite for developing a rear side texture complementary to a sinusoidal front side texture. Before then, the rear side texturing step is expendable in case of double-sided sinusoidal textured LPC-Si solar cells.

Considering the samples without pyramidal rear side texture absorptance is still present for wavelengths larger than the band gap of silicon at around 1100 nm. At 1200 nm absorptance amounts to about 5 % (absolute) for the sinusoidal texture, while absorptance of the planar reference reduces to about 2.5 %. The latter might be attributed to imperfections of the integrating sphere like opening slits for detectors and for incident light. Nevertheless, despite the high material quality of the planar reference, defect absorption might be another reason for absorptance of wavelengths longer than the band gap [199]. Following as a consequence, the higher absorption at 1200 nm of the sinusoidal textured sample might be a hint for a slightly lower material quality than the planar reference and is attributed to defect absorption. After pyramidal rear side texturing, absorptance at 1200 nm remains at about 5 % for both sample types. In case of the planar reference this increase could be explained by additional defects being introduced due to the texturing process. In case of the sinusoidal sample no additional increase in absorptance at 1200 nm after pyramidal rear side texturing is found, which contradicts the hypothesis developed for the planar sample. Nonetheless, it is possible that in case of the sinusoidal textured sample defect absorption takes place mainly in the bulk material. In this case, defect absorption at the rear side would only have minor impact on the absorptance spectra, whereas in case of the planar sample defect absorption at defects introduced by the rear side texture plays a vital role. For clarification high resolution material quality analysis techniques like electron-spin-resonance spectroscopy [121] would be needed. In case of LPC silicon absorber layers defect densities have shown to be close to the detection limit [58, 120] of 1×10^{15} cm^{-3} [120, 200]. So far, the cause of absorptance of wavelengths longer than 1100 nm remains unclear and is attributed to defect absorption with unknown defect nature.

Another common approach to enhance absorption in solar cells is the usage of back reflectors. The influence of a white paint back reflector on the absorption behavior of a sinusoidal textured absorber in comparison to a planar reference is depicted in figure 5.9.

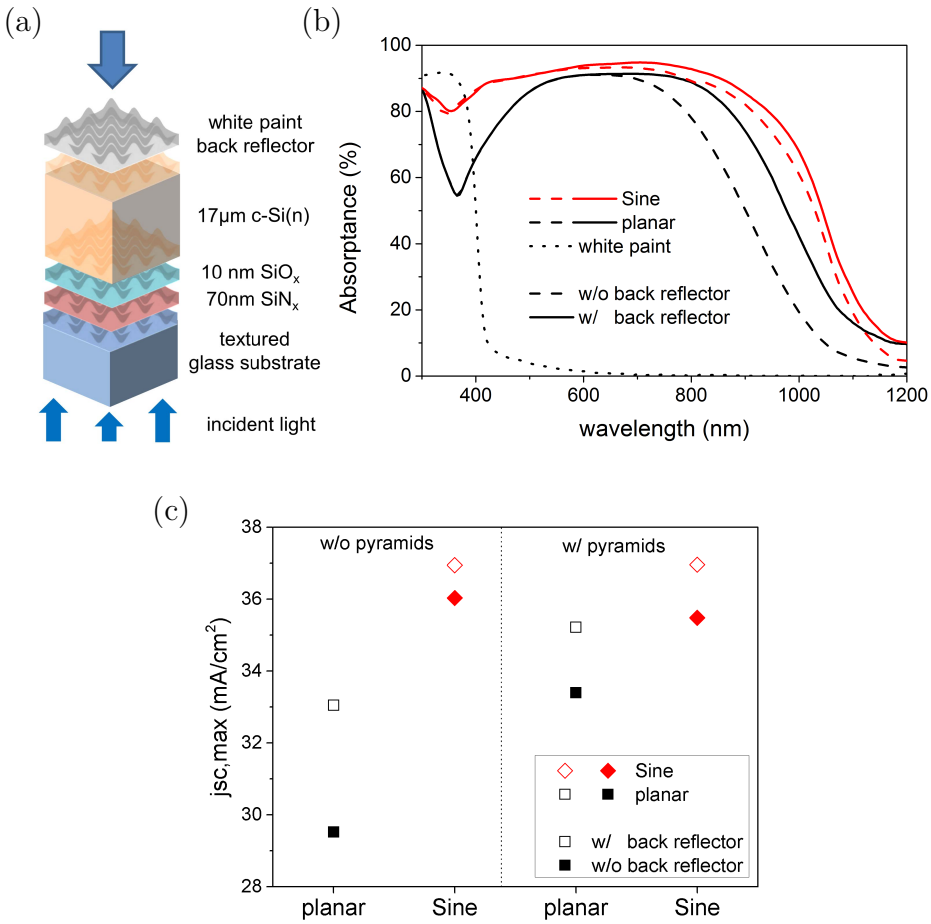


Figure 5.9: (a) Schematic of the sample stacks under investigation. The varied part, the white paint back reflector, is highlighted by a vertical arrow. (b) Absorptance spectra of 17 µm c-Si absorber layers with (solid lines) and without (dashed lines) white paint back reflector at the rear side of a sinusoidal textured layer (red, aspect ratio $h/P = 0.19$) in comparison to a planar reference (black). Absorptance in the white paint is added using a dotted line. (c) Maximum achievable short-circuit current densities ($j_{sc,max}$) of figure 5.8 (b) and figure 5.9 (b) summarizing the absorptance data obtained with and without pyramidal rear texture in combination with (empty symbols) and without (filled symbols) white paint back reflector. For clarity a dotted line separates absorber layers without pyramidal rear side texture (left) and absorber layers with pyramidal rear side texture (right).

Like adding a pyramidal texture, adding a white paint acting as a back reflector does only affect the absorption spectra for wavelengths long enough to reach the rear side of the silicon absorber layer. Applying a back reflector (solid lines) enhances absorption of both sample types, the double-sided sinusoidal textured sample (red) as

well as the planar reference sample (black), compared to not using a back reflector (dashed lines). Back reflectors prolong the light path inside the silicon absorber layer by reflecting light reaching the rear side into the device. As indicated by the dotted line parasitic absorption in the white paint is close to zero for wavelengths longer than 600 nm. For shorter wavelengths the parasitic absorption in the white paint does not influence the measurement result since the light incidences through the glass side and is absorbed in the silicon absorber layer before reaching the rear side of the silicon where the white paint is applied. The gain in absorptance can fully be attributed to enhanced reflection at the rear side of the device.
Since the sinusoidal textured sample already features a rear side texture, enhancement found for the this sample is smaller than the enhancement found for the planar reference. As also made visible in figure 5.9 (c), this absorption enhancement amounts to 3.6 mA cm^{-2} in the planar case (black), from 29.5 mA cm^{-2} (filled symbol) to 33.1 mA cm^{-2} (empty symbol), and to 0.9 mA cm^{-2} in the sinusoidal textured case (red), from 36.0 mA cm^{-2} to 36.9 mA cm^{-2}. A value 3.8 mA cm^{-2} higher than the one obtained on the planar reference.
For wavelengths longer than the band gap of silicon at around 1100 nm parasitic absorption is increased to about 10 % (absolute) independent of the substrate type if a white paint back reflector is used. Parasitic absorption in the white paint used as back reflector (dotted line) can be excluded in this wavelength range. In case of the pyramidal rear side textures absorptance at wavelength higher than the band gap has been attributed to defect absorption in the silicon bulk as well as at the rear side introduced during the KOH etching process. Adding a white paint to the rear side of the silicon absorber layers should not introduce defects in the silicon layer. Nevertheless, in this study absorptance at 1200 nm increases for both texture types after adding the white paint back reflector. Long wavelengths light being reflected at the white painted rear side of the absorber layer undergoes at least a second path through the absorber layer. This might enhance effect of defect absorption inside the absorber layer bulk. Absorptance in both texture types amounts to the same value of around 10 %. The cause of the parasitic absorption at wavelengths loner than 1100 nm remains unknown and is attributed to defect absorption with unknown defect nature as in case of the pyramidal rear side texture.

Figure 5.9 (c) also features the $j_{sc,max}$ of the pyramidal textured samples plotted in figure 5.8 (b) as an additional data set to the right of the data set already described. In addition, the result of combining both, the pyramidal texture with a white paint back reflector, is presented. It is found that adding a white paint back reflector in any case leads to a gain in absorptance. For the planar sample the greatest absorption enhancement is found for the combination of a pyramidal rear texture

with a white paint back reflector leading to a maximum achievable short circuit current density of 35.2 mA cm^{-2}, a gain of 1.8 mA cm^{-2} compared to the sole use of a pyramid texture [figure 5.8 (b)] and a gain of 2.1 mA cm^{-2} compared to the sole use of a white paint back reflector [figure 5.9 (b)], respectively. In case of the sinusoidal texture no difference is found whether or not a pyramidal texture has been applied prior to adding a white paint back reflector (open symbols), corresponding to a $j_{sc,max}$ of 36.9 mA cm^{-2} without and 37.0 mA cm^{-2} with pyramidal texture, a difference within the measurement error. The small decline in absorption between a double sided sinusoidal texture and an added pyramidal texture [figure 5.8 (b)] is compensated by the usage of a white paint back reflector. These results demonstrate that using a double-sided sinusoidal textured substrate instead of a planar substrate enhances absorption as much as applying a pyramidal rear texture in combination with a white paint back reflector to the planar device. Considering the best results achieved an absorption enhancement corresponding to 1.8 mA cm^{-2} is possible using a double-sided sinusoidal textured absorber layer instead of a planar device with optimized rear side light trapping system - a pyramidal texture in combination with a white paint reflector.

In summary, in any case examined the sinusoidal textured device exceeded the corresponding planar reference. Hence, sinusoidal front side textures have demonstrated their suitability for providing anti-reflective properties at the glass-silicon interface as well as light scattering properties at the rear side of the absorber layer. The latter can be enhanced if a white paint back reflector is used enabling maximum achievable short-circuit current densities of 37.0 mA cm^{-2} in 17 µm thick sinusoidal textured LPC silicon absorber layers.

Due to the successful demonstration of providing anti-reflective properties at the glass-silicon interface, as a next step, sinusoidal nano-textures are tested regarding their ability to reduce reflection losses at the air-glass interface. At this point of the thesis, the air-glass interface is the last remaining interface in the underlying device design without applied light management scheme. To reduce reflection losses at the air-glass interface as well as to enhance the light path inside the device, anti-reflective layers can be attached to this interface. In order to rule out possible differences and fluctuations in the production process and to isolate the effect of the attached structures on the optical properties, these anti-reflective layers were modularly attached by means of an index matching liquid to a planar reference. A detailed description of this experiment can be found in a preliminary study [194] revealing an increasing anti-reflective effect with increasing texture feature geometry as it is expected from geometrical optics. The highest reflection loss reduction

has been found for a textured light trapping foil (DSM Advanced Surfaces) [42], which is commonly used to enhance light incoupling in planar LPC solar cell devices [43, 124, 195]. In figure 5.10 the planar reference with modularly attached 750 nm pitched sinusoidal glass texture with an aspect ratio of 0.27 and the respective device without anti-reflective (AR) layer taken from [194] are complemented by a 500 nm pitched sinusoidal substrate texture with similar aspect ratio and by a textured light trapping foil (DSM Advanced Surfaces, [42]). In all cases isopropanol was used as index matching (IM) liquid.

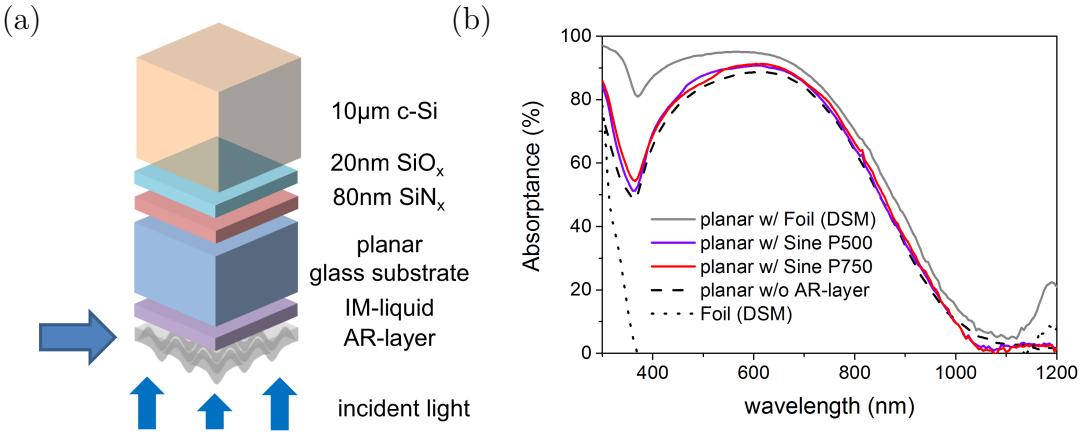


Figure 5.10: (a) Schematic of the sample stacks under investigation. The varied part, the by an index matching (IM) liquid modularly attached anti-reflective (AR) layer, is highlighted by a horizontal arrow. (b) Absorptance spectra of 10 µm planar c-Si absorber layers with (solid lines) modularly attached 500 nm pitched (purple, aspect ratio $h/P = 0.25$) and 750 nm pitched (red, aspect ratio $h/P = 0.27$) sinusoidal textured glass substrates as well as textured light trapping foil (DSM Advanced Surfaces) [42] (gray) as anti-reflective (AR) layers at the air-glass interface in comparison to the same planar device without anti-reflective layer (dashed). Absorptance in the textured light trapping foil (DSM) is added as dotted line.

Independent of the pitch almost no anti-reflective effect is found for sinusoidal textured glasses with pitches of 500 nm (purple) and 750 nm (red) and aspect ratios of around 0.25 if modularly attached at the air-glass interface of a planar device (dashed) instead of being implemented at the glass-silicon interface (chapter 5.1). On the contrary, if a textured light trapping foil (DSM) (gray) developed for usage at this interface is attached to the air-glass interface of a planar absorber layer an absorption enhancement over the entire wavelength range is found. By attaching the scattering foil the maximum achievable short-circuit current density of the planar absorber layer of 26.8 mA cm^{-2} is enhanced by 3.0 mA cm^{-2} to 29.8 mA cm^{-2} [194]. For wavelengths shorter than 400 nm parasitic absorption takes place in the light scattering foil. Since incident light has to pass through the foil this amount of incident light is lost for current generation if implemented into a solar cell device.

However, due to the low amount of energy carried in this wavelength range [figure 2.1 (b)] the loss expressed in terms of maximum achievable short-circuit current density amounts to $0.13\,\mathrm{mA\,cm^{-2}}$. For wavelengths larger than the band gap the scattering foil exhibits parasitic absorption (dotted line) explaining the gain in absorptance for wavelengths longer than 1100 nm. An advantage of the nanoimprinted sinusoidal structures is that these can be directly attached to the glass substrate of the device and can directly be integrated into the solar cell design. On the contrary, the scattering foil (DSM) can only be modularly attached by means of an index matching layer. If not perfectly adapted to the surrounding materials, the latter can be a cause for enhanced reflection losses of incident light. If the modularly attached foil remains effective and stable under various lab and outdoor conditions is unclear. For this reason, currently the anti-reflective foil (DSM) applied is not recommended for implementation into future cell designs but serves as guideline and example for an anti-reflective light management scheme applied to the air-glass interface. Nonetheless, these results as well as the results obtained in a preliminary study [194] demonstrate that an anti-reflective effect can be achieved if nanoimprinted textures are implemented at the air-glass interface of LPC solar cell devices. For direct integration at the air-glass interface a structure with larger texture feature dimensions than the sinusoidal textures in this thesis designed for implementation at the glass-silicon interface would be desired. The beneficial effect of separately optimized textures for different interfaces is also known from literature [29, 74, 75, 197, 198].

So far, best anti-reflective properties at the air-glass interface were found for the textured light trapping foil (reference [194]) and best anti-reflective properties at the glass-silicon interface were found for the sinusoidal substrate texture (this thesis). In figure 5.11 both approaches are combined.

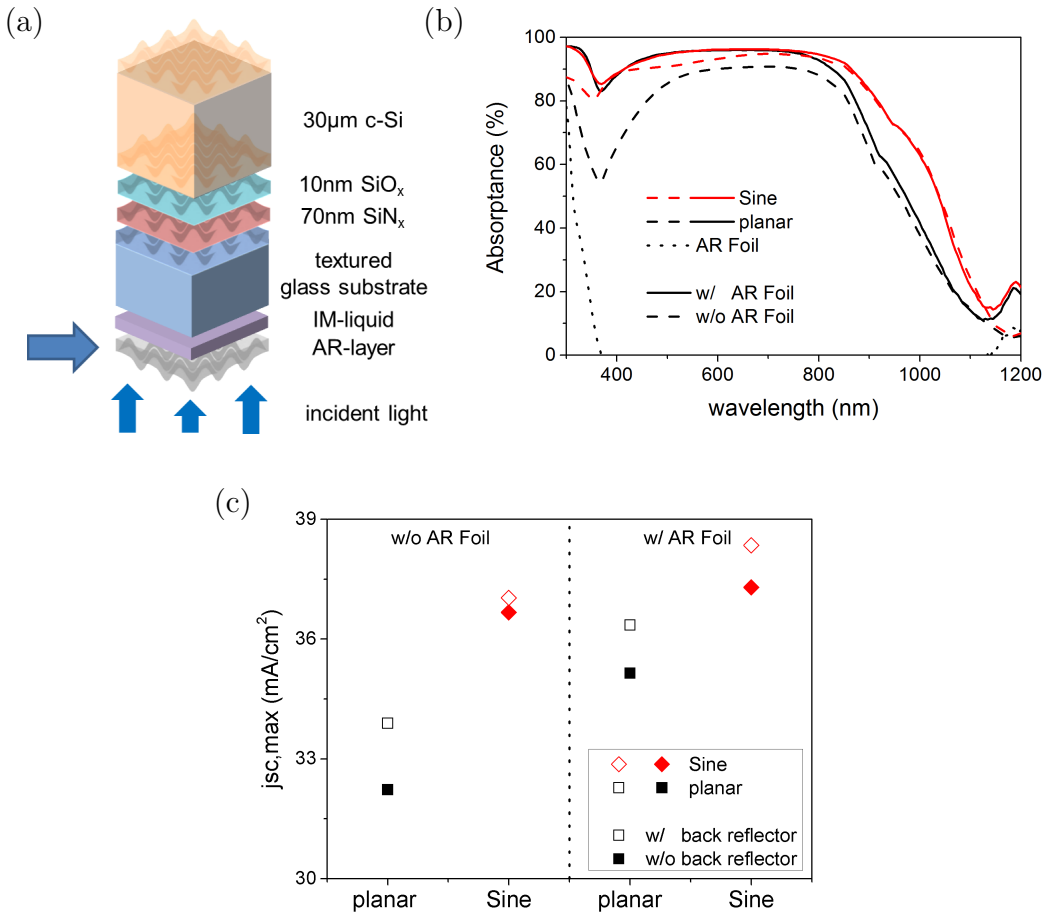


Figure 5.11: (a) Schematic of the sample stacks under investigation. The varied part, the textured light trapping foil (DSM Advanced Surfaces [42]) as anti-reflective (AR) layer modularly attached with an index matching (IM) liquid, is highlighted by a horizontal arrow. (b) Absorptance spectra of 30 µm thick c-Si absorber layers with (solid lines) and without (dashed lines) anti-reflective (AR) foil at the air-glass interface of a sinusoidal textured device (red, aspect ratio $h/P = 0.19$) in comparison to a planar reference (black). Absorptance in the textured light trapping foil (DSM) is added as dotted line. (c) Maximum achievable short-circuit current densities ($j_{sc,max}$) of figure 5.11 (b) summarizing the absorptance data obtained with and without anti-reflective foil in combination with (empty symbols) and without (filled symbols) white paint back reflector. For clarity a dotted line separates absorber layers without anti-reflective foil (left) and absorber layers with anti-reflective foil (right).

For 30 µm thick LPC silicon absorber layers without anti-reflective (AR) foil (dashed lines) the implementation of a sinusoidal substrate texture leads to an increase in mean absorptance in the wavelength range of 350 nm to 600 nm from 78.0 % in the planar case (black) to 89.7 % in the sinusoidal textured case (red). If a textured light trapping foil (DSM) is attached at the air-glass interface (solid lines) mean absorptance increases to 92.4 % in the planar case and 92.6 % in the sinusoidal textured case. If a scattering foil is attached to the air-glass interface reflection losses are reduced to a remaining reflection loss of around 7.5 % regardless whether a 750 nm pitched glass-silicon texture is used or a planar interface. While the scattering foil mainly affects the short wavelength range (dashed lines compared to solid lines), the sinusoidal substrate texture enhances absorption over the entire wavelength range (red lines compared to black lines). Comparing both device types with attached scattering foil the short-circuit current densities calculated for a wavelength range of 280 nm to 1100 nm according to equation 3.1, 35.2 mA cm^{-2} are achieved with a planar absorber layer and 37.3 mA cm^{-2} are achieved with a 750 nm pitched sinusoidal textured absorber layer. Since below 600 nm both devices perform about equal, this increase is solely attributed to the scattering ability of the sinusoidal substrate texture for longer wavelengths. Enhanced absorption for wavelengths longer than 1100 nm is attributed to parasitic absorption in the attached light scattering foil (DSM) (dotted line in figure 5.11)
These values are depicted in figure 5.11 (c). In addition, a combined approach of the best light trapping schemes identified so far, the white paint reflector (figure 5.9) and the textured light trapping foil (this figure), are presented. The maximum achievable short-circuit current densities ($j_{sc,max}$) were calculated from measured absorptance spectra according to equation 3.1. Plane planar and sinusoidal devices with a silicon absorber layer thickness of 30 µm achieve maximum achievable short-circuit current densities of 32.2 mA cm^{-2} and 36.7 mA cm^{-2}, respectively. Adding the textured light trapping foil increases the $j_{sc,max}$ values by 3.0 mA cm^{-2} in the planar case and 0.6 mA cm^{-2} in the sinusoidal textured case. Likewise, adding a white paint back reflector increases the $j_{sc,max}$ values by 1.7 mA cm^{-2} in the planar case and 0.3 mA cm^{-2} in the sinusoidal textured case. Combining both approaches leads to maximum achievable short-circuit current densities of 36.4 mA cm^{-2} in case of the planar device and 38.4 mA cm^{-2} in case of the sinusoidal textured device. Compared to the plane devices this corresponds to a gain of 4.2 mA cm^{-2} for the planar device and 1.7 mA cm^{-2} in case of the sinusoidal textured device.

In summary, despite that the anti-reflective effect of the sinusoidal substrate texture vanishes if a textured light trapping foil (DSM Advanced Surfaces) [42] is attached to the air-glass interface the implementation of a sinusoidal substrate texture is

still beneficial for enhancing absorption over the entire wavelength range. This absorption enhancement is translated into a maximum achievable short-circuit current density enhancement of 2.1 mA cm^{-2} if in combination to the scattering foil at the air-glass interface a sinusoidal substrate texture is used at the glass-silicon interface of a 30 µm thick LPC silicon absorber layer. Even if the textured light trapping foil at the air-glass interface is complemented by a white paint rear side texture, the sinusoidal textured device outperforms the planar device by 2.0 mA cm^{-2}. Since the technological feasibility of the light scattering foil (DSM) applied to the air-glass interface is unclear, future light trapping schemes could combine nanoimprinted textures with suitable feature sizes of planar anti-reflection coatings with sinusoidal textured glass-silicon interfaces.

Figure 5.12 summarizes the gain in $j_{sc,max}$ if a sinusoidal glass-silicon texture instead of a planar interface is applied in addition to the light management schemes named. This gain ranges between 7.3 mA cm^{-2} (figure 5.7) if no additional light management schemes are applied and 1.8 mA cm^{-2} if a combination of a pyramidal rear side texture and a white paint reflector is applied (figure 5.9). To allow for a comparison independent of the silicon absorber layer thickness, the numbers given in the picture correspond to the absolute difference in maximum achievable short-circuit current density ($\Delta j_{sc,max} = j_{sc,max}(\text{Sine}) - j_{sc,max}(\text{planar})$) in mA cm^{-2}.

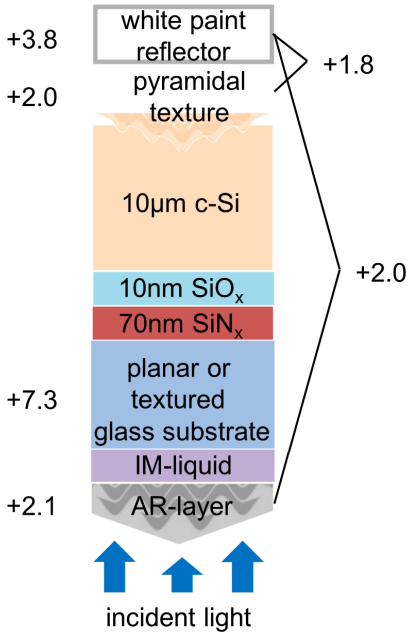


Figure 5.12: Schematic of the sample stacks with different light trapping schemes applied. The numbers given correspond to the gain in in maximum achievable short-circuit current density ($\Delta j_{sc,max} = j_{sc,max}(\text{Sine}) - j_{sc,max}(\text{planar})$) in mA cm^{-2} if a sinusoidal glass-silicon texture is applied in addition to the light management schemes named.

5.4 Conclusion

In order to explore the optical potential of hexagonal sinusoidal nano-textures for LPC silicon absorber layers, the influence of the sinusoidal substrate geometry and of the thicknesses of the different components of the layer stack on the optical properties have been analyzed. The 500 nm pitched sinusoidal substrate texture outperformed the respective 750 nm pitched sample for wavelengths longer than 400 nm. In this crucial wavelength range the 500 nm pitched sinusoidal sample with an aspect ratio of 0.24 was found to perform close to the 96 % absorption limit determined by 4 % reflection loss of incident light at the air-glass interface.
When alternating the substrate texture's aspect ratio between 0 (planar case) and 0.5, absorptance was found to grow with increasing aspect ratio for both pitches. By means of 3D FEM simulations the S-shape behavior of the absorption enhancement could be correlated to the amount of energy being carried in different refraction orders of the fraction of light being reflected back at the textured substrate-silicon interface. With higher aspect ratios reflection losses decrease because more energy is carried in higher refraction orders, which encounter the glass-air interface under angles large enough for total internal reflection. This fraction of light experiences a second chance of being absorbed in the absorber layer. Lower diffraction orders leave the device at the glass-air interface and contribute to the reflection loss.
Varying the thicknesses of the subsequently deposited SiN_x and SiO_x interlayers as well as of the silicon absorber layer an optimized layer stack composed of 60 nm or 70 nm SiN_x / 5 nm SiO_x / 15 µm LPC-Si was identified.
Optical losses in planar LPC devices are often minimized by using a pyramidal rear side texture to scatter long wavelengths at the silicon rear side and a white paint back reflector at the rear side of the device to enhance the light path inside the device. This can also be pursued by modularly attaching an anti-reflective textured light trapping foil (DSM Advanced Surfaces) [42] at the air-glass interface to reduce reflection losses of incident light [43, 124, 195, 196]. In order to explore the full optical potential of sinusoidal textured absorber layer, these measures have successively been applied to 750 nm double-sided sinusoidal textured LPC silicon absorber layers with an aspect ratio of about 0.2. The pyramidal rear texture was found to decrease and the white paint was found to increase absorptance in 17 µm thick LPC silicon absorber layers with sinusoidal front side texture. Implementing a sinusoidal substrate-silicon texture instead of a planar interface lead to a gain in maximum achievable short-circuit current density regardless of what kind of light trapping scheme was applied. This gain varied between 7.3 mA cm^{-2} if no additional light trapping scheme was implemented and 1.8 mA cm^{-2} if a pyramidal rear side

texture with white paint reflector was added. Combining the best methods enhancing absorptance revealed in this thesis, namely an anti-reflective foil (DSM) at the air-glass interface, a silicon absorber layer thickness of 30 µm and a white paint reflector at the rear side, enabled maximum achievable short-circuit current densities of 36.4 mA cm^{-2} in case of the planar device and 38.4 mA cm^{-2} in case of the sinusoidal textured device, respectively. Even if an optimized light trapping scheme is applied to the air-glass and silicon-air interface, texturing the remaining glass-silicon interface with a 750 nm sinusoidal texture enhances the maximum achievable short-circuit current density by 2.0 mA cm^{-2}. Therefore, the sinusoidal substrate texture has demonstrated its great potential for optical enhancement in future LPC silicon thin-film solar cell devices, especially if combined with a white paint reflector. For a silicon absorber layer thickness of 15 µm this device design enabled a maximum achievable short-circuit current density of 37.0 mA cm^{-2}.

6 Electronic Properties of Sinusoidal Nano-Textures

Having demonstrated a suitable material quality and an optical performance exceeding the planar reference device, in this chapter the sinusoidal substrate texture is analyzed regarding its optoelectronic performance in LPC silicon thin-film solar cells. Solar cell devices were prepared as outlined in the experimental part (chapter 3.2). In device design used absorber and emitter contacts are placed on the rear side of the cell in order to avoid optical losses caused by shadowing. Light incidences through the glass-side of the device (superstrate configuration). The sinusoidal nano-textures are implemented at the glass-silicon interface to reduce reflection losses and to enhance the light path inside the silicon layer.
The optoelectronic characterization of sinusoidal textured LPC solar cells is conducted with regard to the influence of the sinusoidal substrate geometry (subchapter 6.1) and in comparison to planar and textured references (subchapter 6.2). Parts of the results presented in this chapter were previously published [192].

6.1 Influence of the Texture Geometry on the Electronic Material Quality

From former experiments of Preidel [58] a U-shaped square lattice structure with a pitch of 2 µm and aspect ratio of 0.5 is known to disturb the electronic material quality (chapter 4.1). The impact of a 500 nm and 750 nm pitched sinusoidal textured glass substrates on the silicon material quality was examined in chapter 4.3. A silicon quality comparable to planar references was revealed demonstrating the suitability of sinusoidal nano-textures for implementation into LPC thin-film solar cells.
Here, the influence of the substrate's pitch of sinusoidal nano-textures on the electronic material quality of 10 µm thick LPC silicon thin-film solar cells is studied.

The respective external quantum efficiency spectra as well as the corresponding open-circuit voltages are given in figure 6.1.

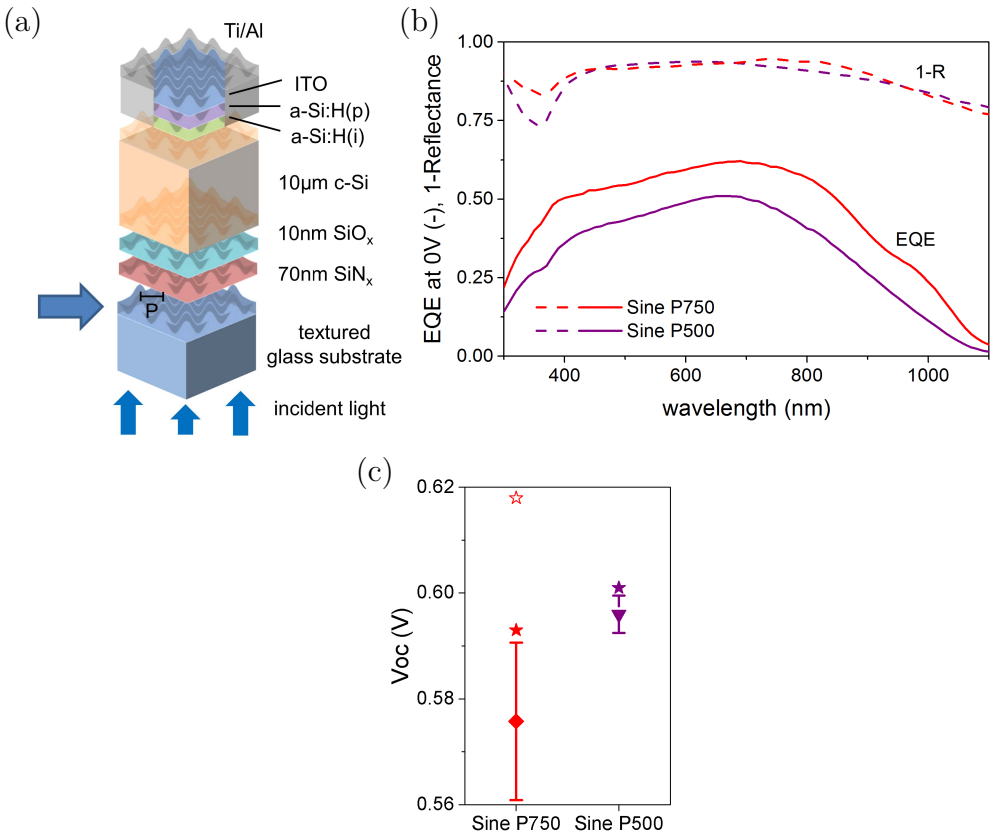


Figure 6.1: (a) Schematic of the solar cell device. The varied part, the pitch (P) of the textured glass substrate, is highlighted by a horizontal arrow. (b) External quantum efficiency (EQE, solid lines) and 1-Reflectance (1-R, dashed lines) of sinusoidal textured devices with 750 nm pitch (red) and 500 nm pitch (purple), respectively. (c) Corresponding open-circuit voltages averaged over the best five cells on each substrate in the respective color code. Peak values are denoted by stars. For the 750 nm pitched sinusoidal structure the best value was obtained on another 750 nm pitched sample of the same batch and is, therefore, marked with an empty symbol.

The superior anti-reflective properties of the 500 nm pitched absorber layers compared to 750 nm pitched absorber layers revealed in chapter 5.1 are preserved if implemented into solar cell devices (1-Reflectance, dashed lines). The external quantum efficiency curve of the sinusoidal 750 nm pitched sample (red) was already depicted and discussed in chapter 4.3. Compared to the 750 nm pitched sample, the EQE curve of the 500 nm pitched sample (purple) [figure 6.1 (b)] is about 0.1 (absolute) lower over the entire wavelength range. This translates into a short-circuit

current density loss of 5.2 mA cm^{-2} from 20.9 mA cm^{-2} for the 750 nm pitched device to 15.7 mA cm^{-2} for the 500 nm pitched device. Despite having demonstrated a comparable silicon material quality in chapter 4.5, this might indicate a reduced silicon material quality on a 500 nm pitched substrate compared to a 750 nm pitched substrate with same aspect ratio of 0.2. Possible reasons are a higher defect density in the bulk (chapter 2.2) or a enhanced surface recombination velocity (equation 2.11). Both could arise from an increased number of texture features per unit area on the smaller pitched substrate. This might intensify the detrimental effect of a textured substrate on the silicon material quality. Hence, for the electronic material quality a larger pitch is favorable.
In terms of open-circuit voltage (V_{oc}), depicted in figure 6.1 (c), slightly higher values are achieved on the smaller 500 nm pitch. On the 750 nm pitched sample an average V_{oc} of 576 mV $\pm$ 2 mV with a peak value of 593 mV is obtained, while on the 500 nm pitched sample an average V_{oc} of 596 mV $\pm$ 1 mV with a peak value of 601 mV is obtained. However, on another 750 nm pitched substrate processed in the same batch as the samples shown a peak V_{oc} value of 618 mV (but lower EQE as the curve shown) was achieved (empty symbol). This demonstrates that independent of the substrate pitch open-circuit voltages above 600 mV can be obtained on sinusoidal textured substrates. The differences in open-circuit voltages on the different 750 nm pitched substrates are in the range of possible fluctuations within one batch. A possible cause for the deviating values could be differences in the thicknesses of the SiN_x / SiO_x interlayer stack caused by different positions of the sample on the sample holder and, hence, different distances to the sputtering target. This SiO_x thickness difference could explain the difference of about 20 mV in V_{oc} [86].

Since the 750 nm pitched substrate has demonstrated a greater potential for high conversion efficiencies, it represents the best compromise between optical absorption enhancement and at least maintaining the electronic material quality of a planar reference so far. Therefore, this pitch was chosen for further detailed investigation.

The geometry of a periodically textured substrate is not only determined by the pitch but also by the height. Thus, the impact of the structure's height on the electronic material quality is analyzed. In addition, for a fixed aspect ratio of 0.2 the influence of the SiN_x / SiO_x interlayer thicknesses is studied. The SiN_x interlayer mainly affects the optical properties and, hence, only indirectly the electronic material quality by an increased or decreased incoupling of light. The SiO_x interlayer is known to influence the electronic properties directly as it was demonstrated for the open-circuit voltage by Amkreutz *et. al.* [86]. In case of the SiO_x layer a thickness of around 5 nm is most beneficial for the electronic properties of a LPC-Si solar cell.

Higher SiO_x interlayer thicknesses as well as no SiO_x layer disturb the electronic material quality.

Based on the results obtained earlier in this chapter as well as in chapter 4.3 a pitch of 750 nm with varied aspect ratios of 0.2 and 0.3 is chosen to examine the influence of the texture height. However, in contrast to formerly shown sinusoidal textures, the sinusoidal textured solar cells in this study do not feature surface enhancement corrected interlayers. Therefore, their interlayer thicknesses are reduced to nominally 60 nm SiN_x / 8 nm SiO_x, while the silicon absorber layer thickness is increased to about 12 µm. The reduced interlayer thicknesses correspond to a combination of optimized optical properties, as found in chapter 5.2, with optimized electronic properties, as known from literature [86]. On the contrary, the formerly shown 750 nm pitched sinusoidal sample with an aspect ratio of 0.2 features surface enhancement corrected interlayer thicknesses of nominally 70 nm SiN_x / 10 nm SiO_x according to the state-of-the-art interlayer thicknesses for planar devices and a silicon absorber layer thickness of 10 µm [86–88]. To examine the influence of the interlayer thicknesses, the surface enhancement corrected sample analyzed in the preceding experiment (red) is depicted again in this study. For all samples the electronic material quality is studied in terms of external quantum efficiency and open-circuit voltage measurements. The corresponding results are depicted in figure 6.2.

Figure 6.2 (b) depicts external quantum efficiencies (EQE) as well as reflectance data (1-R) and (c) open-circuit voltages of 750 nm pitched sinusoidal textured solar cell devices with varied aspect ratios of 0.2 (red) and 0.3 (orange). Samples without surface enhancement corrected interlayers are displayed with (b) dashed lines and (c) open symbols while the sample exhibiting surface enhancement corrected interlayers is displayed with (b) a solid line and (c) a filled symbol. For wavelengths shorter than 600 nm the samples featuring an optimized interlayer stack (chapter 5.2) exceed the sample with state-of-the-art 70 nm SiN_x / 10 nm SiO_x interlayer stack (solid line). For longer wavelengths the optical properties are not comparable since the samples feature different silicon absorber layer thicknesses. In agreement with figure 5.2 (b), the sample with higher aspect ratio exceeds the lower aspect ratio sample regarding their anti-reflective properties. Concerning the samples without surface corrected interlayer thicknesses the greater external quantum efficiency is found of the higher structure with an aspect ratio of 0.3. Hence, for sinusoidal 750 nm pitched substrate textures the maximum height allowing for a high silicon absorber material quality might not been reached yet. The corresponding short-circuit current densities calculated from external quantum efficiency measurements amount to 15.4 mA cm^{-2} for

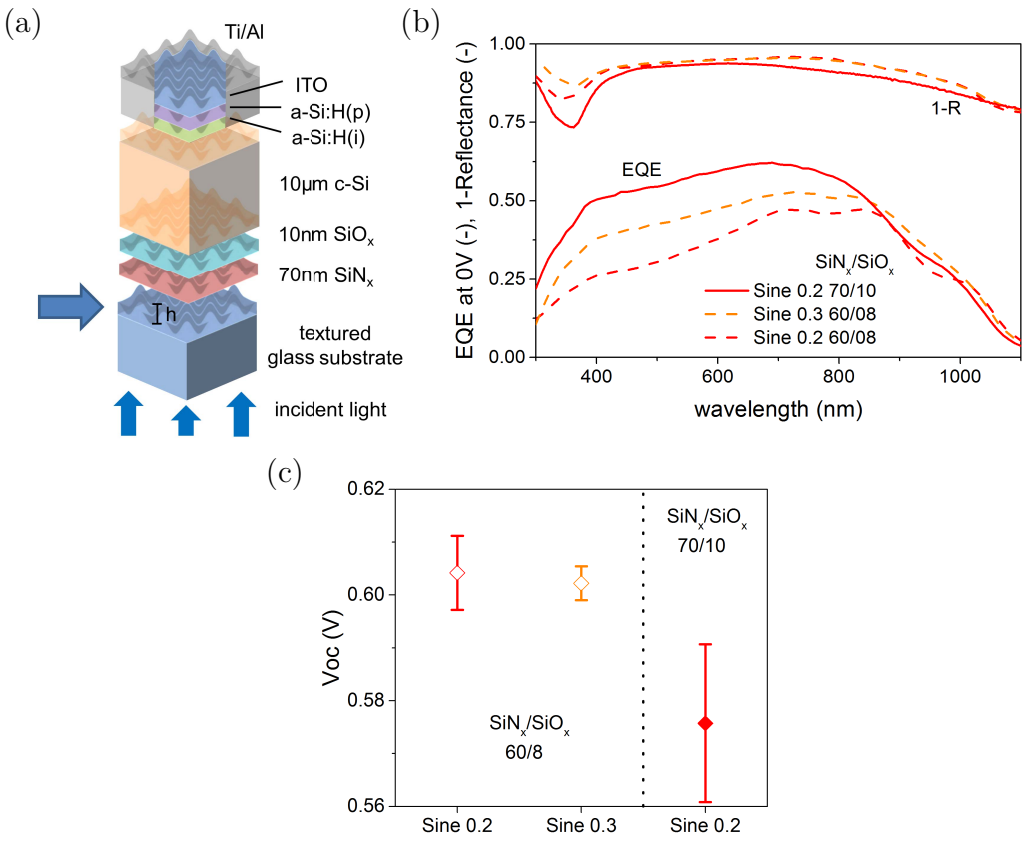


Figure 6.2: (a) Schematic of the solar cell device. The varied part, the height (h) of the textured glass substrate, is highlighted by a horizontal arrow. (b) External quantum efficiency of sinusoidal 750 nm pitched devices with varied aspect ratio of 0.2 (red) and 0.3 (orange). (c) Corresponding open-circuit voltages averaged over the best five cells on each substrate. Samples without surface enhancement corrected interlayer thicknesses of 60 nm SiN_x / 8 nm SiO_x are displayed with (b) dashed lines and (c) open symbols while the sample exhibiting corrected interlayer thicknesses of 70 nm SiN_x / 10 nm SiO_x is displayed with (b) a solid line and (c) a filled symbol. For clarity, samples with and without corrected interlayer thicknesses are separated by a dotted line in figure 6.2 (c).

an aspect ratio of 0.2 and 16.0 mA cm^{-2} for an aspect ratio of 0.3, respectively. For both aspect ratios of 0.2 and 0.3 open-circuit voltages above 600 mV are reached. However, short-circuit current densities above 20.0 mA cm^{-2} are only reached if the SiN_x and SiO_x interlayer thicknesses were corrected for the enhanced surface texture to nominally 70 nm SiN_x / 10 nm SiO_x according to the optimized planar state-of-the-art reference. Comparing samples with same aspect ratio of 0.2 (red) without (dashed line) and with corrected interlayer thicknesses (solid line) the short-circuit current density increases by 6 mA cm^{-2} if surface enhancement corrected interlayers are used. This gain in short-circuit current density can possibly be attributed to a better interface passivation due to the higher interlayers thicknesses. Mean V_{oc}-values are, however, about 30 mV lower. As mentioned before, this lower open-circuit

voltage values might be explained by the different SiO_x passivation layer thickness [86]. Since there should not be different material qualities when using substrates with similar texture feature sizes, another explanation for differing open-circuit voltages observed for samples produced in different batches might be differences in doping densities caused by fluctuations in the solar cell preparation process. The results of this subchapter highlight the importance of valuable passivation by interlayers for an efficient solar cell performance.

6.2 Electronic Properties in Comparison to Textured and Planar References

Despite not featuring the highest possible aspect ratio the sample with surface enhancement corrected SiN_x and SiO_x interlayers exhibits the highest external quantum efficiency of the structures investigated so far. Therefore, this structure is chosen for further comparison with other nanoimprinted glass-silicon textures regarding their electronic material quality. The structures for comparison, a state-of-the-art planar reference, a 750 nm pitched hexagonal pillar structure with an aspect ratio of 0.2 featuring the same interlayer thicknesses as the sinusoidal textured sample and a U-shaped square lattice ("SL") structure [58] with an aspect ratio of 0.5 have already been introduced in chapter 4.1. There, the respective EQE are shown and discussed regarding their silicon material quality. Here, the electronic properties of all structure types are compared.

Figure 6.3 depicts averaged cell characteristics. The structures are compared regarding their (a) external quantum efficiency, (b) short-circuit current densities (j_{sc}, equation 3.2) calculated from EQE measurements averaged over the best three cells, their measured (c) open-circuit voltages (equation 2.14) and (d) their calculated fill factor (FF, equation 2.17), both averaged over the best five cells. The applied contacting scheme does not allow measuring the FF directly due to the high series resistance caused by the simple contacting scheme (chapter 2.2.2). Therefore, the FF is calculated from Suns-V_{oc} measurements assuming zero series resistance. It serves as an upper achievable boundary and is denoted by "pseudo FF". The respective peak values are denoted by stars.

Figure 6.3 compares the averaged cell characteristics of sinusoidal (diamond, red), pillar (circle, blue) and SL (open square, black) textured solar cell devices to a planar (filled square, black) reference cell. For an easier identification the EQE

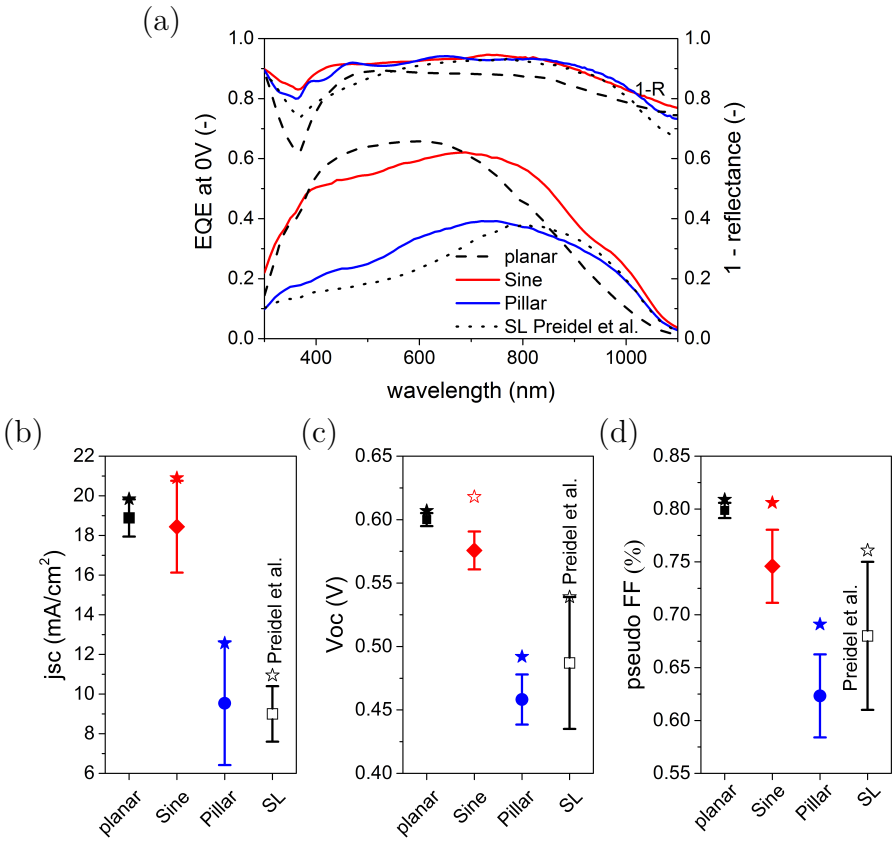


Figure 6.3: (a) External quantum efficiency (EQE) and 1-Reflectance data replotted from figure 4.7 (b). Averaged cell characteristics (b) short-circuit current densities (j_{sc}) calculated from EQE, (c) measured open-circuit voltage (V_{oc}) and (d) pseudo fill factor (pseudo FF) calculated from Suns-V_{oc} on a planar (filled square, black), a sinusoidal (diamond, red), a pillar shaped (circle, blue) structured and square lattice (SL) of Preidel [58] (open square, black) textured substrate. Peak values are denoted by stars.

curves belonging to the peak j_{sc} values are depicted in figure 6.3 (a), despite being already discussed in chapter 4.1. As one of the results there, a declined material quality for the both sharp edged structure types, the pillar and the SL structure, was revealed. Moreover, for all cell parameters analyzed the pillar and square lattice structures exhibit lower values than the planar reference. This decline can probably be attributed to the disturbed silicon material quality if grown and crystallized on steep textured substrates (chapter 4). In contrast, the sinusoidal patterned cells (diamond, red) demonstrate cell characteristics comparable to the planar reference cell, whereby mean j_{sc}-values are slightly higher and mean V_{oc}-values and calculated pseudo fill factors are slightly lower than the planar reference. It is noteworthy that measurement results of different cells on the same substrate differ more for the textured cells than for the planar cells indicating that the material quality is less uniform on patterned substrates. A possible reason for the varying material quality

on the patterned substrates could be inhomogeneities in the nanoimprint pattern itself caused by the manual imprinting process. The respective solar cell parameters are summarized in table 6.1.

While averaged solar cell performance is still slightly lower on sinusoidal tex-

Table 6.1: Averaged cell characteristics, short-circuit current density (j_{sc}), open-circuit voltage (V_{oc}) and calculated pseudo fill factor (pseudo FF), and respective peak values.

	j_{sc} ($\mathrm{mA\,cm^{-2}}$)	Best j_{sc} ($\mathrm{mA\,cm^{-2}}$)	V_{oc} (mV)	Best V_{oc} (mV)	pseudo FF (%)	Best pseudo FF (%)
Planar	18.9 ± 0.9	19.8	600 ± 5	607	79.9 ± 0.7	80.9
Sine	18.4 ± 2.3	20.9	576 ± 15	618	74.6 ± 3.5	80.6
Pillar	9.54 ± 3.1	12.6	458 ± 20	492	62.3 ± 3.9	69.1
SL [58]	9.0 ± 1.4	11.0	487 ± 52	539	68.0 ± 7.0	76.1

tured substrates, peak values, in figure 6.3 denoted by stars, are equal to the values achieved on the planar substrate, as it is the case for pseudo FF, or even outperform the planar values, as it is the case for j_{sc} with $20.9\,\mathrm{mA\,cm^{-2}}$ by 5.3 % (relative) and for V_{oc} with 618 mV by 1.8 % (relative). The latter was obtained on another substrate of the same batch and, therefore, is marked with an empty symbol in figure 6.3 (c). Hence, cells on hexagonal sinusoidal nano-textured substrates have the ability to outperform planar cells if the material quality can be increased further and, recalling the results of chapter 4, increasing passivation in order to reduce surface recombination losses at the textured glass-silicon interface. So far, no optimization of the passivation properties of the SiN_x / SiO_x interlayer stack enhancing the electronic material quality was performed. Indeed, it is likely, that a compromise has to be found between optimized optical properties demanding for thinner interlayers (chapter 5) and thicknesses ensuring that the interlayers are closed even at the steep texture flanks providing the necessary passivation properties. One solution might be a change to an interlayer deposition method better suited for conformal layer growth on textures than the PVD processed used here. Nevertheless, the successful integration of sinusoidal patterned substrates into the solar cell devices proves the suitability for current LPC silicon thin-film solar cells on glass substrates as well as demonstrates their potential for future improvements in cell design.

One limitation of the external quantum efficiency spectra found in both subchapters was the interlayer thicknesses, particularly the SiO_x interlayer thickness, acting as passivation layer. So far, those restrictions inhibit transferring the optimized optical results into enhanced electronic properties when using sinusoidal textured substrate textures for LPC silicon thin film solar cells. Hence, future work on textured substrates for LPC-Si thin-film solar cells should address an optimization of these interlayers' thicknesses. A change of the interlayer deposition method to PECVD techniques allowing for diffusion along the substrate surface during deposition [201] should be included in the scope of further experiments regarding textured substrates for LPC-Si thin-film solar cells. This might allow for closed SiO_x interlayers at thinner and for the electronic properties more beneficial thicknesses.

Based on the results obtained optically (chapter 5) and electronically (this chapter) an efficiency potential for sinusoidal textured solar cell devices can be calculated. To explore the full electrical potential an idealized device is assumed lacking any electronic loss mechanism. This affects mainly two solar cell characteristics: the short-circuit current density and the fill factor. In case of the short-circuit current density (j_{sc}, equation 2.16) it is assumed that no defects are active reducing the optically obtained maximum achievable short-circuit current density compared to the electronically obtained short-circuit current density ($j_{sc,max} = j_{sc}$). For the fill factor (FF, equation 2.17) an ideal contacting scheme without shunt resistances ($R_s = 0$, compare figure 2.5) is assumed. In this case the idealized pseudo fill factor directly corresponds to the fill factor of the solar cell ($pFF = FF$). The measurement of the open-circuit voltage (V_{oc}, equation 2.14) is not effected by shunt resistances of the contacting scheme and can be taken as measured by Suns-V_{oc} (chapter 3.2).

For a sinusoidal textured absorber layer with a 750 nm pitch, a SiN_x (70 nm) / SiO_x (10 nm) interlayer stack and a silicon thickness of around 10 µm a $j_{sc,max}$ of 34.9 mA cm^{-2} was achieved [figure 5.1 (b)]. With an open-circuit voltage of 618 mV and fill factor of 80.6 % (table 6.1) this amounts to an idealized efficiency (η, equation 2.18) of

$$\eta_{ideal}(10\,\mu m) = 34.9\,mA\,cm^{-2} \cdot 618\,mV \cdot 80.6\,\% \cdot \frac{1}{100\,mW\,cm^{-2}} = 17.5\,\%.$$

These values were measured without any additional light management scheme neither at the air-glass nor at the absorber layer rear side. By applying a light scattering foil and a white paint reflector at the respective interfaces and increasing the absorber layer thickness to 30 µm, maximum-achievable short-circuit current density of

38.4 mA cm^{-2} was achieved (figure 5.11). Even higher maximum-achievable short-circuit current densities are likely to be realized if a 500 nm pitched substrate is used instead of a 750 nm pitched substrate (figure 5.1). Moreover, open-circuit voltages of 650 mV could already be demonstrated for LPC silicon thin-film solar cells on planar (references [17, 43, 195]) and textured (chapter 7.1, published in [202]) glass substrates. Assuming that these best values achieved so far can be unified and realized in a sinusoidal texture LPC silicon thin-film solar cell device would increase the efficiency potential to

$$\eta_{ideal}(\text{best}) = 38.4\,\text{mA}\,\text{cm}^{-2} \cdot 650\,\text{mV} \cdot 80.6\,\% \cdot \frac{1}{100\,\text{mW}\,\text{cm}^{-2}} = 20.1\,\%.$$

The calculated efficiency potential is close to the current efficiency record of multi-crystalline silicon wafer solar cells of 21.3 %. This wafer cell exhibits a short-circuit current density of 39.8 mA cm^{-2}, an open-circuit voltage of 668 mV and a fill factor of 80.0 % [203]. Except for the fill factor, these values are only slightly higher than the values obtained with LPC silicon on textured glass substrates. This comparison of idealized cell characteristics of sinusoidal textured LPC silicon solar cells to the multi-crystalline silicon wafer record solar cell highlights the technological potential of silicon thin-film solar cells on textured glass substrates.

6.3 Conclusion

Nanoimprinted, high-temperature stable hexagonal 750 nm pitched sinusoidal and pillar shaped substrate textures have successfully been integrated into 10 µm thick state-of-the-art LPC silicon thin-film solar cells. In this chapter, the influence of the sinusoidal substrate texture geometry on the electronic properties of solar cell devices was studied. Despite the superior optical properties (chapter 5) a reduction of the substrate's pitch from 750 nm to 500 nm was found to decrease the electronic properties. When increasing the substrate's aspect ratio form 0.2 to 0.3 an enhancement of the external quantum efficiency with increasing aspect ratio was found. However, all devices suffered from a reduced electronic material quality compared to the planar reference devices. A material quality comparable to the planar references was only achieved if the thicknesses of the SiN_x / SiO_x interlayer stack were increased beyond the values of the planar references although greater interlayer thicknesses are known to be unfavorable for the optical (chapter 5) and electronic (please refer to reference [86]) properties. This suggests that the applied interlayer thicknesses adapted from state-of-the-art planar reference devices are not closed on textured

substrates. Hence, further research on suitable interlayers on textured substrates in LPC devices is required. Furthermore, a change of the deposition method from PVD to PECVD might be beneficial for growing dense interlayers on textured substrates. Nevertheless, on all sinusoidal pitch sizes and aspect ratios V_{oc} over 600 mV have been achieved demonstrating the high electronic material quality of LPC silicon being grown and crystallized on sinusoidal substrate textures. Despite remaining optimization challenges regarding the textured substrate to silicon interface these results underline the suitability of the sinusoidal texture for LPC silicon devices.
The best solar cell results achieved on a sinusoidal substrate texture so far were compared to alternative nanoimprinted substrates textures, the pillar and the square lattice texture, as well as a planar state-of-the-art reference. The sinusoidal substrate texture outperformed the pillar and square lattice texture allowing for solar cell parameters being comparable to the values achieved on the planar reference. With a silicon absorber layer thickness of less than 9 µm and a doping density of around $5 \times 10^{16}\,\mathrm{cm}^{-3}$ a short-circuit current density of $20.9\,\mathrm{mA\,cm}^{-2}$, an open-circuit voltage of 618 mV and a pseudo fill factor of 80.6 % have been achieved on a 750 nm pitched sinusoidal substrate texture with an aspect ratio of 0.2, thus paving the road for future experiments. Based on these results and optical values obtained in chapter 4 an efficiency potential of 20.1 % under idealized assumptions for 750 nm pitched sinusoidal textured LPC silicon thin-film solar cells.
Further studies could involve sinusoidal substrate textures with higher aspect ratio and optimized interlayer thicknesses. The latter is vital to reduce surface recombination losses in order transfer the optical achievements into an electrical cell performance enhancement over the entire wavelength range. Peak values of sinusoidal patterned devices already outperform their planar references in terms of V_{oc} and j_{sc}. In combination with the high material quality demonstrated in chapter 4 and the optical potential exploited in chapter 5, these electronic values highlight that sinusoidal patterned substrates are promising candidates for future LPC silicon thin-film solar cells cell designs.

7 Comparison of the Sinusoidal Texture to Alternative Substrate Textures

In this chapter alternative approaches to texture the glass-silicon interface in LPC-Si thin film solar cell devices are introduced. In subchapter 7.1 the sinusoidal texture is compared to random glass texture with different feature sizes. These random textures were developed and produced at the University of Delft for enhanced light incoupling in 3 µm thin µc-Si:H thin film solar cells [144, 144, 204], enabling a cell efficiency above 10 % [144]. In the scope of this thesis, the suitability of these random textured glasses for the usage in 10 µm thick LPC-Si thin film solar cells is examined. This part of the chapter was subject of an earlier publication cited as [202]. In subchapter 7.2 the sinusoidal texture is compared to an optically rough but morphologically flat glass-silicon interface texture. This "SMART" texture was designed partially on the basis of the results of this thesis and is developed in parallel by Eisenhauer *et al.* [145].

7.1 Comparison to Random Textures

At the University of Delft random glass substrate textures are produced by depositing sacrificial layers onto the glass substrates and subsequent wet-chemical etching. Depending on the sacrificial layer type differently sized crater-like etch features can be fabricated. A morphology with typical average lateral feature size of 15 µm is achieved with an ITO induced process ("IIT"). A typical average lateral feature size of 2 µm is accomplished using ZnO:Al as sacrificial layer ("ZIT") [204]. In addition, both textures can be superimposed to produce a modulated surface texture ("MST") [144]. Details on the LPC silicon absorber layer and solar cell production process on random textured glass substrates can be found in [202]. In addition to SEM images of the surfaces of 10 µm silicon being grown and crystallized on each of these random

textured substrates, the substrate feature sizes of the sinusoidal texture and a MST texture, as representative for a random texture, are compared in figure 7.1.

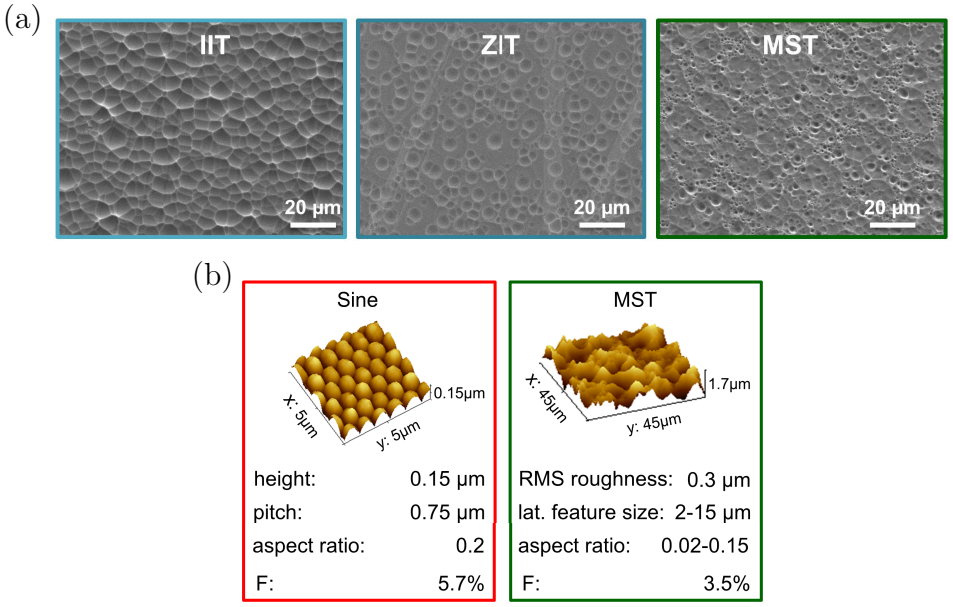


Figure 7.1: (a) SEM top view images tilted by 30° of silicon on IIT (cyan), ZIT (dark cyan) and MST (green) textured glass substrates exhibiting differently lateral feature sizes. (b) AFM images on the silicon oxide passivation layer coated surface of a 750 nm pitched hexagonal sinusoidal structure (red) and a random MST textured glass substrate (green). Note the different scales in both images. Typical values for the height and pitch or, respectively, for the root-mean-square (RMS) roughness and lateral feature size as well as the resulting aspect ratio and the surface enhancement factor (F) are given of each structure.

Figure 7.1 (a) shows SEM images of 10 µm thick silicon absorber layers being grown and crystallized on randomly textured glass substrates with differently sized etch features achieved when using different sacrificial layers for wet-chemical etching. On an IIT texture (cyan) large etch craters in the range of tens of µm are obtained while on a ZIT texture (dark cyan) smaller etch craters in the range of µm are formed. A modulated surface texture (green) is created if combining both textures with both feature sizes in the range of µm. The latter has exemplarily been chosen for a detailed comparison to the hexagonal sinusoidal textured substrate in terms of substrate geometry parameters in figure 7.1 (b). Hexagonal sinusoidal textures (red) with a pitch (P) of 750 nm typically exhibit a range of feature heights (h) between 150 nm and 200 nm resulting in aspect ratios (h/P) varying between 0.2 and 0.25 for different sinusoidal textured substrates. With a typical root-mean-square (RMS) roughness around 300 µm the structure feature sizes of a typical MST texture (green) are up to around 1.5 µm higher than for a sinusoidal texture. Considering typical lateral feature sizes ranging between 2 µm and 15 µm an aspect ratio range

(RMS roughness / lateral feature size) between 0.02 and 0.15 is obtained for the MST texture, up to one order of magnitude lower than on the sinusoidal texture. Despite higher absolute numbers, the texture flanks are smoother on the MST texture than on the sinusoidal texture. This results in surface enhancement factors (F) of 3.5 % in the case of the depicted MST texture example compared to a surface enhancement factor of 5.7 % in case of the depicted sinusoidal texture example.

The optical properties of 10 µm thick LPC silicon absorber layers crystallized on all three random texture types are compared to a sinusoidal texture as well as a planar reference in terms of anti-reflective properties and maximum achievable short-circuit current density in dependence on the silicon absorber layer thickness in figure 7.2

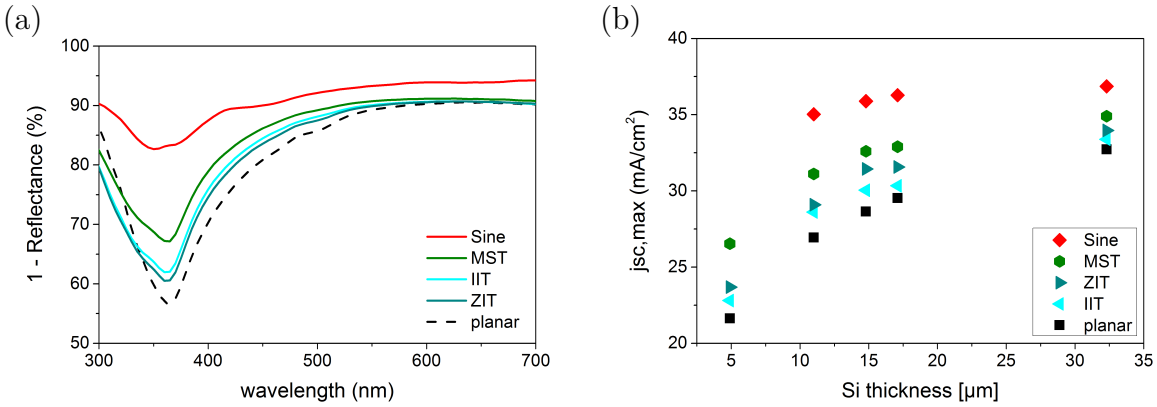


Figure 7.2: (a) Reflectance data (R, plotted as 1-R) of 11 µm thick silicon absorber layers on a planar reference (black, dashed), different random textures with large features (IIT, cyan), small features (ZIT, dark cyan) and a combination of both (MST, green) as well as a hexagonal sinusoidal texture (Sine, red). (b) Corresponding maximum achievable short-circuit current densities $j_{sc,max}$ in the respective color code calculated from absorptance measurements according to equation 3.1 in dependence on the silicon absorber layer thickness.

Figure 7.2 (a) studies the optical properties of both texture types regarding their ability to provide anti-reflective properties in state-of-the-art 10 µm thick LPC silicon absorber layers including a SiN_x (70 nm) / SiO_x (10 nm) interlayer stack. All textures provide additional anti-reflective properties (solid lines) over the entire wavelength range in comparison to a planar reference (black, dashed line) with optimized interlayer stack. Analyzing the different random textures with large features (IIT, cyan), small features (ZIT, dark cyan) and with both feature sizes combined (MST, green), the largest reflection reduction and absorption enhancement is found for the combined MST texture while no difference between the both textures with a single feature size range is found. The hexagonal sinusoidal textured device (red) outperforms the random textures in terms of reflection loss reduction. In the wavelength range of 350 nm to 600 nm average reflection losses of the planar reference of 20.2 %

are reduced by 2.9 % (absolute) when using an IIT texture, by 2.2 % (absolute) using the ZIT texture, by 4.8 % (absolute) in case of the MST texture and 10.4 % (absolute) by texturing the silicon absorber layer with a hexagonal 750 nm pitched sinusoidal texture, respectively. Within the random textures the best result is obtained for the MST texture featuring combined texture feature sizes. This combination of different feature sizes implies a combination of different scattering mechanisms optimized for multiple wavelengths enables absorption enhancement over a broad wavelength range [144]. For further comparison the maximum achievable short-circuit current densities have been calculated from absorptance spectra over the entire wavelength range of 280 nm to 1100 nm (equation 3.1) for every structure. The corresponding results are added to the thickness dependent absorption plot for the sinusoidal texture [figure 5.7 (c)] and plotted in figure 7.2 (b) in dependence on the silicon absorber layer thickness varied between 5 µm and 30 µm. For all silicon thicknesses the absorption enhancement is more pronounced if a sinusoidal texture (red) is applied than if a random texture is used. Within the random textures the same trend as found for the anti-reflective properties is followed achieving the highest absorption enhancement for the combined MST texture. The smaller sized ZIT texture achieves slightly higher $j_{sc,max}$ values than the larger sized IIT texture. Taking into account the silicon absorber layer thickness of around 11 µm, an average lateral feature size of 15 µm might be too large to enable an effective light path enhancement inside the absorber layer.

In summary, to enhance light incoupling into LPC silicon absorber layers by providing anti-reflective properties the feature sizes and shape of the sinusoidal texture is better suited than the random textures featured in this study. Nevertheless, among the random textures best results were obtained on the combined MST texture, which was selected for further experiments. As a compromise between absorption enhancement and material consumption reduction a silicon thickness of 15 µm has been selected for further experiments (chapter 5.2). With this silicon thickness the maximum achievable short-circuit current density of the planar reference of 28.6 mA cm^{-2} is enhanced by 4.0 mA cm^{-2} if a random MST texture is used and by 7.3 mA cm^{-2} if a hexagonal 750 nm pitched sinusoidal texture is applied.

In order to estimate the full optical potential of the random texture compared to the sinusoidal texture as well as a state-of-the-art planar reference the angular dependence of the absorption on the incident light is analyzed. The optical behavior under different angles of incident light plays a crucial role for application in a solar cell device. Based on the results of chapter 5.3, the 15 µm thick absorber layers were additionally provided with a pyramidal rear side texture and a white paint reflector in order to minimize transmission losses at the rear side while the random MST and periodic sinusoidal texture provide anti-reflective properties at the front side of the silicon absorber layer. The respective results are depicted in figure 7.3.

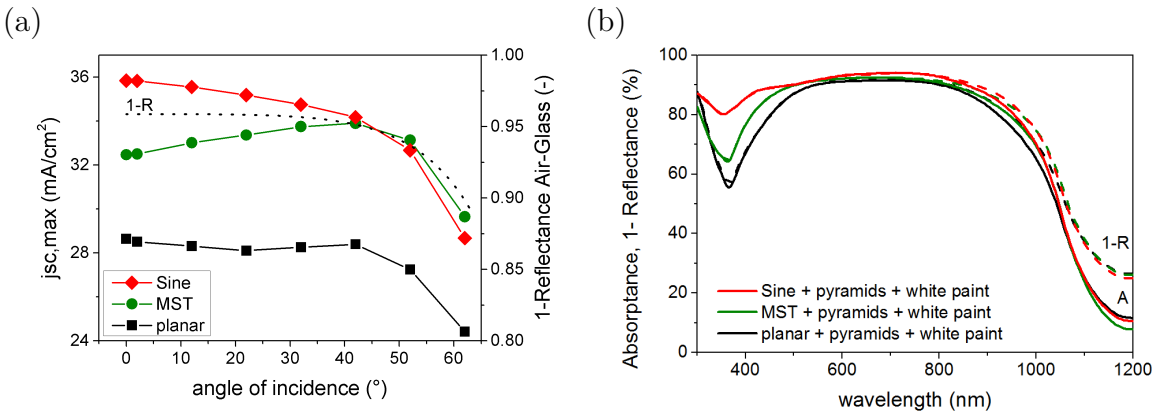


Figure 7.3: Comparison of 15 µm thick absorber layers deposited on a sinusoidal (diamond, red) texture, on a MST texture (circle, green) and on a planar substrate (square, black). (a) Maximum achievable short-circuit current density calculated from measured absorptance data under different angles of incidence. The data points were connected with lines as guide for the eyes. Reflection losses (plotted as 1-R) of incident light at the air-glass interface were calculated according to equation 2.5 and added as dotted line. (b) Absorptance (A, solid lines) and reflectance (R, dashed lines, plotted as 1-R) of the absorber layer featuring a pyramidal texture and a white paint back reflector at the rear side.

For comparison of the absorption behavior under different angles of incidence maximum achievable short-circuit current densities ($j_{sc,max}$) were calculated according to equation 3.1 based on the measured absorption spectra for every angle of incidence. The result is illustrated in figure 7.3 (a). Using a textured absorber layer is beneficial for absorption over the entire range of incidences angle compared to a planar reference absorber. In contrast to the sinusoidal textured absorber layer (red, diamond), slowly declining with increasing angle of incidence, absorption in the MST textured layer (green , circle) slightly increases. The decline for the sinusoidal texture can be attributed to small differences in refractive index between glass substrate, sol-gel and interlayers as demonstrated by calculations of Jäger *et al.* [72]. Absorptance of the planar reference (black) stays approximately constant until an incident angle

of around 50° is reached. For higher angles absorptance of all three structure types starts to decline due to increasing reflection losses at the air-glass interface (dotted line, calculated according to equation 2.5). For such shallow incident angles the MST texture outperforms the sinusoidal texture. Hence, absorption is more stable, especially for high angles of incidence, when using a wet-etched random MST texture with feature sizes in the µm-range than a nanoimprinted 750 nm pitched sinusoidal texture. However, for incident angles smaller than 40° the sinusoidal texture is more beneficial for absorption enhancement than the MST texture.

In figure 7.3 (b) the optical properties of sinusoidal textured (red), MST textured (green) and planar 15 µm thick LPC silicon absorber layers with rear side pyramidal texture and white paint reflectors are compared. For wavelengths shorter than 600 nm both texture types reduce average reflection losses (reflectance data, dashed lines) from 20.4 % for the planar case (black) down to 15.7 % for the MST sample (green) and 11.5 % for the sinusoidal sample (red), respectively. Because no additional anti-reflection layer at the air-glass interface and for every device anti-reflective SiN_x interlayers with the same thickness were used, this reduction of reflection losses can fully be attributed to the anti-reflective effect of the substrate textures. The reduction of reflection losses as well as light scattering at the textured front and rear side of the absorber layers are translated into an absorption enhancement over the entire wavelength range (solid lines), which is more pronounced for the sinusoidal texture than for the MST texture. The corresponding maximum achievable short-circuit current density enhancements amount to 32.2 mA cm^{-2} for the planar device, 34.5 mA cm^{-2} for the MST textured device and 37.0 mA cm^{-2} for the sinusoidal textured device. As discussed in chapter 5.3, absorptance of wavelengths larger than the band gap of silicon at around 1100 nm is attributed to defect absorption in the silicon layer. Since the maximum achievable short-circuit current density is calculated for a wavelength range of 280 nm to 1100 nm, this does not influence the calculation of $j_{sc,max}$ values.

In order to estimate the electronic performance of the MST texture compared to the sinusoidal texture and the planar reference, a MST textured sample corresponding to the sample set discussed in chapter 4.3 was prepared exhibiting a state-of-the-art layer stack of 70 nm SiN_x / 10 nm SiO_x and 10 µm thick silicon absorber. The result is plotted in figure 7.4 (a). In order to allow for a direct comparison as well as to enhance the solar cell performance on textured glass substrates, solar cell devices were prepared on a sinusoidal textured, a MST textured and a planar reference substrate using the optimized layer stack based on the results of chapter 5.2 of 70 nm SiN_x, 5 nm SiO_x and 15 µm silicon absorber layer thickness. The sinusoidal

textured cell is missing in the data set after optimization because this substrate suffered from delamination during liquid phase crystallization. Therefore, only the results of the opto-electronic analysis of the MST texture and the planar reference device are summarized in figure 7.4 (b).

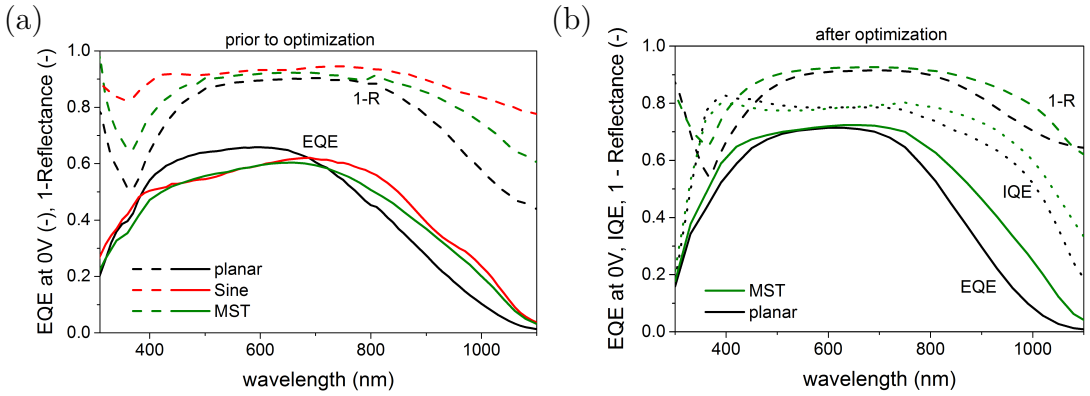


Figure 7.4: (a) 1-Reflectance (1-R, dashed lines) and external quantum efficiency (EQE, solid lines) prior to optimization of the sinusoidal textured device (red) and the planar textured device (black), as depicted in figure 4.7 (b), where the data of a MST textured device (green) has been added for comparison. (b) Opto-electrical properties, reflectance (dashed lines, plotted as 1-R), internal quantum efficiencies (IQE = EQE / A, dotted lines) and external quantum efficiencies (EQE, solid lines) of a planar reference cell (black) and a MST textured cell (green) using an optimized layer stack as revealed in chapter 5.2.

Comparing both texture types, the sinusoidal (red) and the MST (green) texture, the solar cell performance of the MST textured device is lower in the short and long wavelength range. In an intermediate wavelength range of around 450 nm to 600 nm both texture types perform about equal. This indicates that the thickness of the interlayer stack has to be adapted to the substrate texture instead of solely being transferred from the optimized planar case in order to provide sufficient passivation. The MST texture is only able to outperform the planar reference for wavelengths longer than 750 nm due to the scattering effect of the double-sided textured absorber layer. The anti-reflective properties of the textured absorber layers (figure 7.2) were preserved if implemented into solar cell devices and were discussed in the scope of figure 7.2. Absolute numbers are not compared because the MST texture was produced in a different batch than the sinusoidal texture and the planar reference, but from a qualitative point of view, the sinusoidal textured device exhibits a greater potential than the MST texture to exceed the planar cell performance. This result is in correspondence with the result found for the optical properties depicted in figure 7.2.

In figure 7.4 (b) the external quantum efficiencies (solid lines) of a planar reference (black) and a MST textured device (blue) featuring optimized layer stacks based

on the results of chapter 5.2 are compared. The MST textured device outperforms or is equal to the planar reference over the entire wavelength range enabling a short-circuit current density (j_{sc}) enhancement from 21.8 mA cm^{-2} in the planar case to 24.8 mA cm^{-2} in the MST textured case. Considering the optical properties (dashed lines) or both device types this short-circuit current enhancement can be attributed to the optical absorption enhancement resulting from the anti-reflective properties of the MST texture. In order to enable a comparison of the electronic material qualities obtained on both device types, the differences between the maximum achievable short-circuit current density ($j_{sc,max}$, equation 3.1) obtained from optical measurements and the electronically achieved short-circuit current densities (j_{sc}, equation 3.2) were calculated to a loss of 6.8 mA cm^{-2} for the planar device and 7.8 mA cm^{-2} for the MST textured device. This difference is attributed to electronic losses in the absorber layer (chapter 2.2.1) and related to the material quality of the same. The result indicates that the material quality of the MST textured silicon absorber layer is only slightly lower than the material quality of the planar absorber layer. This conclusion is assisted by comparing the internal quantum efficiencies (IQE, dotted lines) being comparable or slightly lower for wavelengths shorter than 700 nm before light trapping of the double-sided textured absorber layer enables a higher current generation for long wavelengths light.
In fact, comparing the open-circuit voltages and pseudo fill factors averaged over the best five cells on an planar and a MST textured substrate, values of (643 ± 6) mV and (78.8 ± 0.8) %, respectively, are obtained on the planar reference while average values of (630 ± 4) mV and (75.8 ± 0.9) % are accomplished on the MST texture. As in case of the sinusoidal substrate texture (chapter 6.2) the lower V_{oc}-values on the textured substrate might be explained by insufficient passivation provided by a too thin or not closed SiO_x layer [86]. This aspect is of particular importance, since nominally only 5 nm SiO_x were deposited on both, the planar as well as textured substrate featuring an increased surface area and probably partially steep texture flanks. Furthermore, the standard deviation of the averaged values can be qualitatively correlated to the uniformity of the material quality again indicating that material quality on the MST texture is comparable to the material quality obtained on a planar reference despite the silicon has been grown and crystallized on a textured substrate.

The result obtained on the MST texture proves that with a suitable surface passivation LPC silicon thin-film devices fabricated on textured glass substrates can outperform planar devices not only optically but also electrically. This highlights the suitability of the approach to texture the glass-silicon interface enabling enhanced short-circuit current densities in future LPC silicon thin-film solar cell devices.

7.2 Comparison to a Smooth Three-Dimensional Light Scattering Nano-Texture

An alternative approach to a sinusoidal substrate texture, which corresponds to a pillar texture with smoothed textured flanks, is to fill the voids of a 750 nm pitched hexagonal pillar texture with a suited optically transparent material in order to obtain an optically rough but morphologically flat substrate texture. This approach is called "smooth anti-reflective three-dimensional" (SMART) texture and developed in parallel to this thesis [145] based on the results of the pillar textured substrate exhibiting desirable optical properties but due to its steep texture flanks diminished electronic properties (chapter 4). In a SMART textured substrate the SiO_x sol-gel pillars are filled with TiO_x enabling an anti-reflective effect arising from a graded index effect of the materials used [145]. In figure 7.5 all texture types, the periodic sinusoidal and SMART textures, the random MST texture and the planar reference are compared regarding their optical properties in LPC-Si absorber layers.

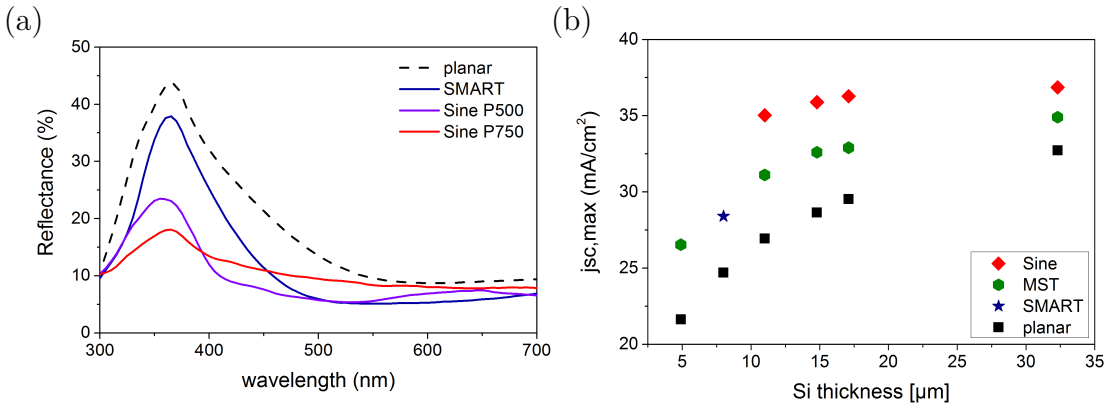


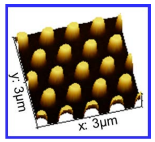
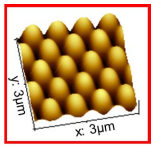
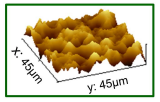
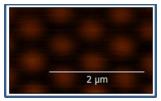
Figure 7.5: Comparison of optical properties of LPC silicon on a SMART textured substrate [145] (dark blue, star) to a state-of-the-art planar reference (black, dashed, square), MST textured (green, hexagon) as well as 750 nm pitched (red, diamond) and 500 nm pitched (purple) sinusoidal textured absorber layers in terms of (a) reflectance and (b) maximum achievable-short circuit current density calculated from absorptance spectra for a wavelength range of 280 nm to 1100 nm.

The reflectance spectrum of a SMART textured absorber layer (dark blue) is compared to 500 nm (purple) and 750 nm (red) pitched sinusoidal textured absorber layers in figure 7.5 (a). The reflectance of a planar reference has been added (back, dashed) for guidance. Mean reflectance in the wavelength range of 350 nm to 600 nm amounts to 20.7 % for the planar device, 14.0 % for the SMART, 11.2 % for the 750 nm pitched sinusoidal and 9.5 % for the 500 nm pitched sinusoidal textured device, respectively. As any other substrate textured investigated in this thesis the

SMART texture reduces reflection losses compared to the planar reference device. Compared to the 750 nm pitched sinusoidal sample the SMART texture performs worse in terms of reducing reflection losses for wavelengths shorter than 450 nm and better for longer wavelengths while the 500 nm pitched sinusoidal sample outperforms the SMART texture with exception of a small decline in a wavelength range of 550 nm up to 700 nm. For longer wavelengths the reflectance spectra are no longer comparable since the samples were prepared in different batches featuring different silicon absorber layer thicknesses and, hence, penetration depths (figure 2.1).

To obtain an impression on how the SMART texture performs in the context of the other texture types presented in this thesis, the maximum-achievable short-circuit current density of the SMART texture is added to the comparison in figure 5.7 (b). The planar reference of the SMART texture fits well in the trend of the planar references presented in figure 7.5 (b) assuring the validity of the comparison of the SMART structure in this context. The 8 µm thick SMART textured silicon absorber layer (blue, star) achieves a maximum achievable short-circuit current density of 28.4 mA cm^{-2}. This value fits in the trend of the MST texture and, thus, is assumed to be lower than a sinusoidal texture with the same silicon thickness. However, while the double-sided textured sinusoidal texture has already almost fully exploited its optical potential (chapter 5), the SMART texture offers potential for improvement if texturing its so far planar silicon absorber layer rear side. In case of the planar reference using a KOH pyramidal rear side texture gained 4.2 mA cm^{-2} (chapter 5.3). Assuming the same gain for the SMART texture, a combination of a SMART front side texture with a pyramidal rear side texture has the potential to achieve optical properties comparable to double-sided textured sinusoidal textures. However, the SMART texture exhibits the additional advantage of a planar substrate-silicon interface promising an enhanced silicon material quality (chapter 4.4) and electronic properties (chapter 6.2). In a first study, this planar substrate-silicon interface allowed the SMART texture to exceed the planar reference in terms of external quantum efficiency for wavelengths longer than 400 nm. This corresponds to an increase of j_{sc} by 13 % (relative) despite of suffering from parasitic absorption in the TiO_x layer in the wavelength range below 400 nm [145]. Overall, the minor optical properties of the SMART texture compared to sinusoidal substrate textures are overcome by its advantageous planar substrate-silicon interface allowing for easier passivation and solar cell processing. Therefore, the SMART concept is a suitable candidate to overcome the processing challenges of the 750 nm pitched texture.

As a last point, a summarized list of key points on the different substrate-silicon textures analyzed in the scope of this thesis is presented:

Structure	Properties	Key Remarks
Pillar 	+ good optical properties - decreased electronic material quality	• not suited for implementation into LPC solar cells • served as new optical benchmark
Sine 	+ superior optical properties + enhanced material quality compared to Pillar + adjustable feature sizes (optics ↔ electrics) - material quality lower than on planar reference	• 500 nm Sine offers best anti-reflective properties of all structures • interface passivation remains a challenge
MST 	+ material quality alike planar reference + electronic properties exceeded planar reference - minor optical properties compared to Sine	• due to minor optical potential not expected to remarkably enhance j_{sc} in future cell designs
SMART 	+ optical properties alike Pillar and 750 nm Sine + smooth substrate-silicon interface - requires complementary light management	• most promising approach to unify enhanced optical and electrical properties • expected to rise j_{sc} in future cell designs

7.3 Conclusion

The sinusoidal substrate texture was compared to alternative approaches for texturing the substrate-silicon interface. For this purpose random textured glass substrates with differently sized etch features fabricated at the University of Delft, were implemented into LPC silicon devices as part of this thesis. All textures enhanced absorption compared to the planar reference. Among the random textures the highest absorption enhancement was found for the random texture with combined feature sizes, the modulated surface texture. However, none of the random textures was able to outperform the absorption enhancement of the sinusoidal substrate texture for silicon absorber layer thicknesses varied between 5 µm and 30 µm. The random modulated surface texture offered a higher angular stability than the hexagonal sinusoidal substrate texture although outperforming absorption of the sinusoidal textured absorber layer was only possible for angles larger than 40°. If provided with pyramidal rear side textures and white paint back reflectors (chapter 5.3), 15 µm thick LPC silicon absorber layers achieved a maximum achievable short-circuit current densities of 32.2 mA cm^{-2} in case of a planar substrate-silicon interface, 34.5 mA cm^{-2} in case of a modulated surface textured substrate-silicon interface and 37.0 mA cm^{-2} in case of a hexagonal 750 nm pitched sinusoidal textured substrate-silicon interface, respectively. Preliminary tests revealed that the sinusoidal surface texture provides not only better optical but also slightly better electronic properties. Both texture types suffered from interface problems compared to the planar reference. Applying the optical optimizations found in chapter 5.2, the modulated surface texture was able to outperform the planar reference in terms of external quantum efficiency over the entire wavelength range rising the short-circuit current density by 3 mA cm^{-2}. Average open-circuit voltages of 630 mV were obtained for MST textured cells and of 643 mV for planar cells, respectively. These results as well as a comparison of the corresponding internal quantum efficiencies indicate that the high material quality of LPC silicon on planar substrates can be transferred to wet-etched MST textured substrates. As the relevant sinusoidal device was destroyed during processing, the modulated substrate texture was in-house the first substrate texture, which was able to achieve a better external quantum efficiency than the corresponding planar reference device. Based on the results achieved for the modulated surface texture the conversion efficiency potential of the sinusoidal texture was estimated to be 13.8 % due to the higher optical and similar electronic potential. In comparison to the SMART concept, which is developed in-house in parallel to this thesis, the sinusoidal texture provides the higher absorption enhancement. However, as long as the remaining challenges with regard to the interface passivation of the sinu-

soidal textured substrates will not be overcome, the SMART concept featuring a flat substrate-silicon interface offers an interesting alternative for enhancing the cell performance of current LPC silicon thin-film devices.

8 Summary and Outlook

Nanoimprinted high-temperature stable hexagonal sinusoidal front surface textures were implemented into state-of-the-art liquid phase crystallized silicon thin-film solar cells on glass. Suitable substrate texture geometries were identified, based on a one-dimensional model texture and a variation of smooth and steep texture flanks. At the same time, substantial insights into the liquid phase crystallization process on textured glass substrates were found. Sinusoidal nano-textured glass substrates enable anti-reflective and light trapping properties while maintaining the silicon material quality. Double-sided sinusoidal textured absorber layers constitute a promising approach to minimize optical losses, one of the major shortcomings in current liquid phase crystallized (LPC) thin-film solar cell designs.

The analyzed structures were developed based on previous work on texturing the glass-silicon interface by nanoimprint lithography of Preidel [58]. The work of Preidel revealed that a suitable substrate texture for LPC silicon thin-film solar cells has to be a compromise between a statistically etched crater-like texture with an aspect ratio of 0.05 favorable for desirable electronic properties and a steep square lattice structure with an aspect ratio of 0.5 favorable for enhanced optical properties. First, the interplay between a one-dimensional substrate texture and the liquid phase crystallization process was analyzed. The expertise gained allowed to identify a texture period of around 700 nm with an aspect ratio of 0.2 as suitable substrate texture geometries. These benchmarks ensured a silicon material quality comparable to planar references. Identifying a suitable substrate texture was complemented by a comparative analysis of two 750 nm pitched hexagonal substrate textures with an aspect ratio of 0.2, the steep pillar and the smooth sinusoidal textures.

The steep pillar texture offered vital optical anti-reflective properties but due to the steep texture flanks exhibited a diminished silicon material quality. Considering simulations of Lockau *et al.* [185], the sinusoidal substrate texture was developed, matching the pillar structure except for the smoothed texture flanks. The sinusoidal substrate texture preserved the optical gain of the pillar texture while enabling a silicon material quality only slightly lower than on a planar references. Especially, the

absorber layer region near to the textured substrate-silicon interface was affected. The decline was attributed to an enhanced surface recombination velocity at the textured substrate-silicon interface. This conclusion was supported upon analyzing the material quality of the LPC silicon bulk. According to the methods applied, a comparable silicon material quality was achieved on 750 nm or 500 nm pitched sinusoidal substrate textures and a planar reference approving the compatibility of these textures for LPC silicon absorber layers. Hence, with the hexagonal sinusoidal nanotexture a suitable substrate texture was identified, unifying anti-reflective properties with the desirable electronic material quality.

Next, the influence of the sinusoidal substrate geometry on the optical properties of 10 µm thick LPC silicon absorber layers was explored. A 500 nm pitched sinusoidal substrate texture has proven to be even more beneficial for minimizing reflection losses at the substrate-silicon interface than a 750 nm pitched sinusoidal texture. For both pitches the anti-reflective properties grew with increasing aspect ratio, which was varied between 0 (planar case) and 0.3. The physical background could be explained by optical 3D FEM simulations. The electronic properties of the 750 nm pitched device outperformed the 500 nm pitched device. Subsequently, the sinusoidal substrate pitch was set to 750 nm and the aspect ratio was set to 0.2–0.25, compromising between optical enhancement and the required silicon material quality.

To explore the full optical potential of sinusoidal textured devices, the sinusoidal substrate-silicon texture was combined with additional light trapping measures at other interfaces. In contrast to the planar case, only a slight beneficial impact or even a detrimental effect of these additional light management methods was found. Highest absorption values were obtained when combining the best approaches enhancing absorptance revealed, namely an anti-reflection foil at the air-glass interface, a silicon absorber layer thickness of 30 µm and a white paint reflector at the rear side. This combined light trapping scheme enabled maximum achievable short-circuit current densities of 36.4 mA cm^{-2} in case of the planar device and 38.4 mA cm^{-2} in case of the sinusoidal textured device, respectively. Hence, even if optimized light trapping methods are applied to the air-glass and silicon-air interface, texturing the remaining glass-silicon interface with a 750 nm sinusoidal texture enhances the maximum achievable short-circuit current density by 2.0 mA cm^{-2}.

The influence of sinusoidal substrate textures on the electronic properties of LPC silicon thin-film solar cells was analyzed in comparison to planar and textured cells. The 750 nm pitched sinusoidal textured device offered a higher external quantum efficiency than the 500 nm pitched device. Moreover, no detrimental effect of an

increased texture height investigated for aspect ratios ranging from 0.2 to 0.3 was found. This suggested that the aspect ratio of the sinusoidal substrate texture can be increased up to 0.3 without disturbing the silicon material quality. This might also be beneficial from an optical point of view. The highest quantum efficiency was found for a device with an aspect ratio of 0.2 with interlayer thicknesses enhanced according to the surface enhancement of the substrate texture. This indicates that interlayer thicknesses adapted from the planar reference cell do not provide sufficient passivation on textured substrates. Regardless of the sinusoidal pitch size and texture heights, open-circuit voltages above 600 mV display a high electronic material quality of LPC silicon on sinusoidal substrate textures. With an silicon absorber layer thickness of less than 9 µm and a doping density of around $5 \times 10^{16}\,\mathrm{cm}^{-3}$, a short-circuit current density of $20.9\,\mathrm{mA\,cm}^{-2}$, an open-circuit voltage of 618 mV, and a pseudo fill factor of 80.6 % were achieved on a 750nm pitched sinusoidal substrate texture with an aspect ratio of 0.2. These values are alike those achieved on the planar reference, thus highlighting the suitability of the sinusoidal texture for LPC silicon devices.

Finally, using sinusoidal textured substrate textures was compared to two alternative approaches, differently sized random textures and an optically rough but morphologically flat anti-reflective texture. Among the random textures, most pronounced absorption enhancement compared to a planar reference device was found for a random texture combining different texture feature sizes, the modulated surface texture. If provided with pyramidal rear side textures and white paint reflectors, 15 µm thick LPC silicon absorber layers achieved maximum achievable short-circuit current densities of $32.2\,\mathrm{mA\,cm}^{-2}$ in case of a planar substrate-silicon interface, $34.5\,\mathrm{mA\,cm}^{-2}$ in case of a modulated surface textured interface and $37.0\,\mathrm{mA\,cm}^{-2}$ in case of a hexagonal 750 nm pitched sinusoidal textured substrate-silicon interface, respectively. Applying optimized interlayer and absorber layer thicknesses, the random modulated surface texture was able to outperform the planar reference in terms of external quantum efficiency over the entire wavelength range, rising the short-circuit current density by $3\,\mathrm{mA\,cm}^{-2}$. This result, the corresponding internal quantum efficiency, and an average open-circuit voltage of 630 mV indicate that the high material quality of LPC silicon on planar substrates was reproduced on wet-etched random modulated surface textured substrates. Another alternative to sinusoidal front textures is the implementation of an optically rough but morphologically flat three-dimensional anti-reflective texture. This texture provided similar anti-reflective properties as a 750 nm pitched sinusoidal texture but offers the additional advantage of a flat substrate-silicon interface and the potential of an increased silicon absorber layer material quality compared to a textured device.

Overall, sinusoidal substrate textures have proven to be effective "buckets" to carry light into LPC silicon thin-film solar cells. Based on this thesis' results, an efficiency potential of 20.1 % was calculated. A comparison to the current multi-crystalline wafer record cell with an efficiency of 21.3 % highlighted the substantial technological potential of LPC silicon on (sinusoidal) textured glass substrates. Despite not having reached this goal yet, the approach of implementing sinusoidal nano-textures at the glass-silicon interfaces is an important step forward.

The 750 nm pitched sinusoidal substrate texture developed in this thesis provided crucial insight into the implementation of textured glass substrates in LPC solar cells and the interplay between optical properties, electrical properties and the absorber layer material quality. With the aim of the 750 nm pitched sinusoidal substrate texture, the ability of textured substrates minimizing optical losses at the glass-silicon interface, the major loss mechanism of current LPC silicon thin-film solar cell designs, was demonstrated. To further enhance the silicon material quality on textured glass substrate, future work might address the usage of analysis techniques sensitive enough to characterize LPC silicon, which are not influenced by interfering with the substrate texture. An interlayer system providing reliable passivation for textured substrates should be developed. For combining different light trapping methods at various interfaces, it is crucial to better understand the light path inside the absorber layer from a waveguide perspective, such that the front and rear side textures can be adapted to one another.

For future LPC cell designs two approaches in the scope of this thesis have demonstrated a greater potential for enhancing the solar cell performance. If the cell design shall be optimized regarding its optical performance, a 500 nm pitched sinusoidal substrate texture provides the required properties. In this case the development of a suitable interlayer providing sufficient passivation is of particular importance. If the cell design shall be optimized regarding its electrical performance, a smooth anti-reflective three-dimensional texture provides a similar optical potential as the 750 nm pitched sinusoidal texture but features the advantage of a flat substrate-silicon interface. Due to the flat absorber layer rear side, the latter approach requires the development of complementary light trapping methods at other interfaces in order to exploit the full optical potential.

List of Figures

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Chapter 6

Chapter 7

Chapter A

List of Tables

Bibliography

[1] E. Kästner. *"Die Schildbürger"*. Dressler, 2006.

[2] DMA Photovoltaic Equipment. "International Technology Roadmap for Photovoltaics (ITRPV) Results 2015 including maturity report ". `http://www.itrpv.net/Reports/Downloads/2016/`, 2016. accessed 21-11-2106.

[3] New Energy and Industrial Technology Development Organization (NEDO) Kaneka Corporatio. "World's Highest Conversion Efficiency of 26.33 % Achieved in a Crystalline Silicon Solar Cell – A World First in a Practical Cell Size". `http://www.kaneka.co.jp/kaneka-e/images/topics/1473811995/1473811995{_}101.pdf`, September 2016. Accessed: 14-Sep-2016.

[4] Trina Solar. "Trina Solar Announces New Efficiency Record of 21.25 % Efficiency for Multi-crystalline Silicon Solar Cell ". `http://www.trinasolar.com/us/about-us/newinfo{_}978.html`, 2015. Accessed: 14-Sep-2016.

[5] Y. Zhang, N. Stokes, B. Jia, S. Fan, and M. Gu. "Towards ultra-thin plasmonic silicon wafer solar cells with minimized efficiency loss". *Sci. Rep.*, 4:4939, 2014.

[6] K. Masuko, M. Shigematsu, T. Hashiguchi, D. Fujishima, M. Kai, N. Yoshimura, T. Yamaguchi, Y. Ichihashi, T. Mishima, N. Matsubara, T. Yamanishi, T. Takahama, M. Taguchi, E. Maruyama, and S. Okamoto. "Achievement of More Than 25 % Conversion Efficiency With Crystalline Silicon Heterojunction Solar Cell". *IEEE J. Photovoltaics*, 4(6):1433–1435, 2014.

[7] J. H. Petermann, D. Zielke, J. Schmidt, F. Haase, E. G. Rojas, and R. Brendel. "19 %-efficient and 43µm-thick crystalline Si solar cell from layer transfer using porous silicon". *Prog. Photovoltaics Res. Appl.*, 20(1):1–5, 2012.

[8] H. Sivaramakrishnan Radhakrishnan, R. Martini, V. Depauw, K. Van Nieuwenhuysen, T. Bearda, I. Gordon, J. Szlufcik, and J. Poortmans. "Kerfless layer-transfer of thin epitaxial silicon foils using novel multiple layer porous silicon stacks with near 100% detachment yield and large minority carrier diffusion lengths". *Sol. Energy Mater. Sol. Cells*, 135:113–123, 2015.

[9] I. Gordon, F. Dross, V. Depauw, A. Masolin, Y. Qiu, J. Vaes, D. Van Gestel, and J. Poortmans. "Three novel ways of making thin-film crystalline-silicon layers on glass for solar cell applications". *Sol. Energy Mater. Sol. Cells*, 95:S2–S7, 2011.

[10] G. Conibeer, M. A. Green, R. Corkish, Y. Cho, E.-C. Cho, C.-W. Jiang, T. Fangsuwannarak, E. Pink, Y. Huang, T. Puzzer, T. Trupke, B. Richards, A. Shalav, and K.-l. Lin. "Silicon nanostructures for third generation photovoltaic solar cells". *Thin Solid Films*, 511-512:654–662, 2006.

[11] Fraunhofer ISE. "Photovoltaics Report". `https://www.ise.fraunhofer.de/de/downloads/pdf-files/aktuelles/photovoltaics-report-in-englischer-sprache.pdf`, updated: 20 October 2016. Accessed: 15-Nov-2016.

[12] M. Keevers, T. Young, U. Schubert, and Green M. A. "10 % efficient CSG minimodules". In *22nd European Photovoltaic Solar Energy Conference*, Milan, 2007.

[13] M. A. Green, P. A. Basore, N. Chang, D. Clugston, R. Egan, R. Evans, D. Hogg, S. Jarnason, M. Keevers, P. Lasswell, J. O´Sullivan, U. Schubert, A. Turner, S. R. Wenham, and T. Young. "Crystalline silicon on glass (CSG) thin-film solar cell modules". *Sol. Energy*, 44:857–863, 2004.

[14] D. Amkreutz, J. Müller, M. Schmidt, T. Hänel, and T. F. Schulze. "Electron-beam crystallized large grained silicon solar cell on glass substrate". *Prog. Photovoltaics Res. Appl.*, 19:937–945, 2011.

[15] J. Dore, D. Ong, S. Varlamov, R. Egan, and M. Green. "Progress in Laser-Crystallised Thin-Film Polycrystalline Silicon Solar Cells". *IEEE J. Photovoltaics*, 4(1):33–39, 2014.

[16] T. Matsuyama, N. Terada, T. Baba, T. Sawada, S. Tsuge, K. Wakisaka, and S. Tsuda. "High-quality polycrystalline silicon thin film prepared by a solid phase crystallization method". *J. Non-Cryst Solids*, 198–200:940–944, 1996.

[17] J. Haschke, D. Amkreutz, L. Korte, F. Ruske, and B. Rech. "Towards wafer quality crystalline silicon thin-film solar cells on glass". *Sol. Energy Mater. Sol. Cells*, 128:190–197, 2014.

[18] S. Kühnapfel, N.H. Nickel, S. Gall, M. Klaus, C. Genzel, B. Rech, and D. Amkreutz. "Preferential {100} grain orientation in 10 micrometer-thick laser crystallized multicrystalline silicon on glass". *Thin Solid Films*, 576:68–74, 2015.

[19] C. Battaglia, J. Escarre, K. Söderström, M. Charrie‘re, M. Despeisse, F.-J. Haug, and C. Ballif. "Nanomoulding of transparent zinc oxide electrodes for efficient light trapping in solar cells". *Nat. Photonics*, 5:535–538, 2011.

[20] K. Söderström, G. Bugnon, F.-J. Haug, S. Nicolay, and C. Ballif. "Experimental study of flat light-scattering substrates in thin-film silicon solar cells". *Sol. Energy Mater. Sol. Cells*, 101:193–199, 2012.

[21] M. Z. Pakhuruddin, J. Huang, J. Dore, and S. Varlamov. "Light Absorption Enhancement in Laser-Crystallized Silicon Thin Films on Textured Glass". *IEEE J. Photovoltaics*, 6(1):159–165, 2016.

[22] S. Fahr, T. Kirchartz, C. Rockstuhl, and F. Lederer. "Approaching the Lambertian Limit in Randomly Textured Thin-Film Solar Cells". *Optics Express*, 19:A865–A874, 2011.

[23] C. Trompoukis, I. Abdo, R. Cariou, I. Cosme, O. Deparis W. Chen, A. Dmitriev, E. Drouard, M. Foldyna, E. G.-Caurel, I. Gordon, B. Heidari, A. Herman, L. Lalouat, K.-D. Lee, J. Liu, K. Lodewijks, F. Mandorlo, I. Massiot, A. Mayer, V. Mijkovic, J. Muller, R. Orobtchouk, G. Poulain, P. Prod'Homme, P. R. I. Cabarrocas, C. Seassal, J. Poortmans, R. Mertens, O. El Daif, and V. Depauw. "Photonic nanostructures for advanced light trapping in thin crystalline silicon solar cells". *Phys. status solidi*, 212(1):140–155, 2015.

[24] P. Bermel, C. Luo, L. Zeng, L. C. Kimerling, and J. D. Joannopoulos. "Improving thin-film crystalline silicon solar cell efficiencies with photonic crystals". *Opt. Express*, 15(25):16986–17000, 2007.

[25] A. Polman and H. A. Atwater. "Photonic design principles for ultrahigh-efficiency photovoltaics". *Nat. Mater.*, 11(3):174–177, 2012.

[26] D. Zhou and R. Biswas. "Photonic crystal enhanced light-trapping in thin film solar cells". *J. Appl. Phys.*, 103(9):93102, 2008.

[27] S. B. Mallick, M. Agrawal, and P. Peumans. "Optimal light trapping in ultrathin photonic crystal crystalline silicon solar cells". *Opt. Express*, 18(6):5691–5706, 2010.

[28] B. Lin, Q. Hua, S.-F. Leung, X. Duan, and Z. Fan. "Efficient Light Absorption with Integrated Nanopillar/Nanowell Arrays for Three-Dimensional Thin-Film Photovoltaic Applications". *ACS Nano*, 7(3):2725–2732, 2013.

[29] K. X. Wang, Z. Yu, V. Liu, Y. Cui, and S. Fan. "Absorption Enhancement in Ultrathin Crystalline Silicon Solar Cells with Antireflection and Light-Trapping Nanocone Gratings". *Nano Lett.*, 12(3):1616–1619, 2012.

[30] H. Tan, R. Santbergen, A. H. M. Smets, and M. Zeman. "Plasmonic Light Trapping in Thin-film Silicon Solar Cells with Improved Self-Assembled Silver Nanoparticles". *Nano Lett.*, 12(0):4070, 2012.

[31] P. Spinelli, V. E. Ferry, J. van de Groep, M. van Lare, M. A. Verschuuren, R. E. I. Schropp, H. A. Atwater, and A. Polman. "Plasmonic light trapping in thin-film Si solar cells". *J. Opt.*, 14(2, SI):11pp, 2012.

[32] V. E. Ferry, M. A. Verschuuren, H. B. T. Li, E. Verhagen, R. J. Walters, R. E. I. Schropp, H. A. Atwater, and A. Polman. "Plasmonic Light Trapping For Thin Film a-Si:H Solar Cells". In *35th IEEE Photovolt. Spec. Conf.*, IEEE Photovoltaic Specialists Conference, pages 760–765. IEEE, 2010.

[33] J. Bhattacharya, N. Chakravarty, S. Pattnaik, W. D. Slafer, and R. Biswas. "A photonic-plasmonic structure for enhancing light absorption in thin film solar cells". *Appl. Phys. Lett.*, 99:131114, 2011.

[34] P. R. Pudasaini and A. A. Ayon. "Modeling the front side plasmonics effect in nanotextured silicon surface for thin film solar cells application". *Microsyst. Technol.*, 19(6):871–877, 2013.

[35] J. Y. Kwon, D. H. Lee, M. Chitambar, S. Maldonado, A. Tuteja, and A. Boukai. "High Efficiency Thin Upgraded Metallurgical-Grade Silicon Solar Cells on Flexible Substrates". *Nano Lett.*, 12(10):5143–5147, 2012.

[36] M. D. Kelzenberg, S. W. Boettcher, J. A. Petykiewicz, T. B. Turner-Evans, M. C. Putnam, E. L. Warren, J. M. Spurgeon, R. M. Briggs, N. S. Lewis, and H. A. Atwater. "Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications". *Nat. Mater.*, 9:239–244, 2010.

[37] K.-Q. Peng, X. Wang, L. Li, X.-L. Wu, and S.-T. Lee. "High-Performance Silicon Nanohole Solar Cells". *J. Am. Chem. Soc.,*, 132:6872+, 2010.

[38] C. Haase and H. Stiebig. "Thin-film silicon solar cells with efficient periodic light trapping texture". *Appl. Phys. Lett.*, 91(6):061116, 2007.

[39] H. Sai, K. Saito, N. Hozuki, and M. Kondo. "Relationship between the cell thickness and the optimum period of textured back reflectors in thin-film microcrystalline silicon solar cells". *Appl. Phys. Lett.*, 102(5):53505–53509, 2013.

[40] M. Python, E. Vallat-Sauvain, J. Bailat, D. Domine, L. Fesquet, A. Shah, and C. Ballif. "Relation between substrate surface morphology and microcrystalline silicon solar cell performance". *J. Non. Cryst. Solids*, 354(19-25):2258–2262, 2008.

[41] H. Cui, P. R. Campbell, and M. A. Green. "Compatibility of glass textures with E-beam evaporated polycrystalline silicon thin-film solar cells". *Appl. Phys. A*, 111(3):935–942, 2012.

[42] C. Ulbrich, A. Gerber, K. Hermans, A. Lambertz, and U. Rau. "Analysis of short circuit current gains by an anti-reflective textured cover on silicon thin film solar cells". *Prog. Photovoltaics Res. Appl.*, 21:1672–1681, 2013.

[43] T. Frijnts, S. Kühnapfel, S. Ring, Onno Gabriel, S. Calnan, J. Haschke, B. Stannowski, B. Rech, and R. Schlatmann. "Analysis of photo-current potentials and losses in thin film crystalline silicon solar cells". *Sol. Energy Mater. Sol. Cells*, 143:457–466, 2015.

[44] L. J. Guo. "Nanoimprint lithography: methods and material requirements". *Adv. Mater.*, 19:495–513, 2007.

[45] S. Y. Chou, P. R. Krauss, and P. J. Renstrom. "Nanoimprint lithography". *J. Vac. Sci. Technol. B*, 14(6):4129–4133, 1996.

[46] C. Becker, V. Preidel, T. Sontheimer, C. Klimm, E. Rudigier-Voigt, M. Bockmeyer, and B. Rech. "Direct growth of periodic silicon nanostructures on imprinted glass for photovoltaic and photonic applications". *Phys. Status Solidi C*, 9(10-11):2079–2082, 2012.

[47] C. Battaglia, J. Escarré, K. Söderström, L. Erni, L. Ding, G. Bugnon, A. Billet, M. Boccard, L. Barraud, S. de Wolf, F.-J Haug, M. Despeisse, and C. Ballif. "Nanoimprint Lithography for High-Efficiency Thin-Film Silicon Solar Cells". *Nano Lett.*, 11:661–665, 2011.

[48] C. Trompoukis, A. Herman, O. El Daif, V. Depauw, D. Van Gestel, K. Van Nieuwenhuysen, I. Gordon, O. Deparis, and J. Poortmans. "Enhanced absorption in thin crystalline silicon films for solar cells by nanoimprint lithography". In *Proc. SPIE*, volume 8438, page 84380R, 2012.

[49] W. Soppe, M. Döenkämper, J.-B. Notta, P. Pex, W. Schipper, and R. Wilde. "Nanoimprint lithography of textures for light trapping in thin film silicon solar cells". *Phys. Status Solidi A*, 210(4):707–710, 2013.

[50] M. Khorasaninejad, N. Abedzadeh, J. Walia, S. Patchett, and S. S. Saini. "Color Matrix Refractive Index Sensors Using Coupled Vertical Silicon Nanowire Arrays". *Nano Lett.*, 12(8):4228–4234, 2012.

[51] J. Zhu, Y. Bai, L. Zhang, Z. Song, H. Liu, J. Zhou, T. Lin, and Q. H. Liu. "Large-Scale Uniform Silver Nanocave Array for Visible Light Refractive Index Sensing Using Soft UV Nanoimprint". *IEEE Photonics J.*, 8(4):1–7, 2016.

[52] T. Senn, J. Bischoff, N. Nüsse, M. Schoengen, and B. Löchel. "Fabrication of photonic crystals for applications in the visible range by Nanoimprint Lithography". *Photonics Nanostructures - Fundam. Appl.*, 9(3):248–254, 2011.

[53] N. Kooy, K. Mohamed, L. Pin, and O. Guan. "A review of roll-to-roll nanoimprint lithography". *Nanoscale Res. Lett.*, 9(1):320, 2014.

[54] S. H. Ahn and L. J. Guo. "Large-Area Roll-to-Roll and Roll-to-Plate Nanoimprint Lithography: A Step toward High-Throughput Application of Continuous Nanoimprinting". *ACS Nano*, 3(8):2304–2310, 2007.

[55] F. Back, M. Bockmeyer, E. Rudigier-Voigt, and P. Löbmann. "Periodic nanostructures imprinted on high-temperature stable sol-gel films by ultraviolet-based nanoimprint lithography for photovoltaic and photonic applications". *Thin Solid Films*, 562:274–281, 2014.

[56] M. Verschuuren and H. van Sprang. "3D Photonic Crystal Structures By Sol-Gel Imprint Lithography". *MRS Spring Meet.*, 1002(12):105–1002, 2007.

[57] C. Becker, V. Preidel, D. Amkreutz, J. Haschke, and B. Rech. "Double-side textured liquid phase crystallized silicon thin-film solar cells on imprinted glass". *Sol. Energy Mater. Sol. Cells*, 135:2–7, 2015.

[58] V. Preidel. *"Kristalline Silizium-Dünnschichten auf nanoimprintstrukturiertem Glas"*. PhD thesis, TU Berlin, 2014.

[59] V. Preidel, D. Amkreutz, J. Haschke, M. Wollgarten, B. Rech, and C. Becker. "Balance of optical, structural, and electrical properties of textured liquid phase crystallized Si solar cells". *J. Appl. Phys.*, 117(22):225306, 2015.

[60] H.-G. Wagemann and H. Eschrich. *"Photovoltaik"*. Vieweg+Teubner, 2nd edition, 2010.

[61] M. A. Green. *"Solar Cells - Operating Principles, Technology and System Application"*. University of NSW, 1992.

[62] P. Y. Yu and M. Cardona. *"Fundamentals of Semiconductors"*. Graduate Texts in Physics. Springer Berlin Heidelberg, 2010.

[63] A. Luque and S. Hegedus, editors. *"Handbook of Photovoltaic Science and Engineering"*. John Wiley & Sons, Ltd, 2nd edition, 2003.

[64] J. I. Pankove. *"Optical Processes in Semiconductors"*. Dover Publications, 1971.

[65] National Renewable Energy Laboratory (NREL). "Reference Solar Spectral Irradiance: ASTM G-173". `http://rredc.nrel.gov/solar/spectra/am1.5/astmg173/astmg173.html`, 2016. Accessed: 19-Oct-2016.

[66] M. A. Green and M. Keevers. "Optical properties of intrinsic silicon at 300 K". *Prog. Photovoltaics*, 3(3):189–192, 1995.

[67] R. Brendel. *"Thin-Film Crystalline Silicon Solar Cells: Physics and Technology"*. John Wiley & Sons, 2003.

[68] D. Meschede. *"Gerthsen Physik"*. Springer Berlin Heidelberg, 2015.

[69] W. Demtröder. *"Experimentalphysik 3"*. Springer Berlin Heidelberg, 2010.

[70] C. Kittel. *"Introduction to Solid State Physics"*. John Wiley & Sons, 8th edition, 2005.

[71] Corning Incorporated. "CORNING EAGLE XG® Slim Glass". `https://www.corning.com/media/worldwide/cdt/documents/EAGLEXG{%}C2{%}AESlimGlass.pdf`, 2013.

[72] K. Jäger, C. Barth, M. Hammerschmidt, S. Herrmann, S. Burger, F. Schmidt, and C. Becker. "Simulations of sinusoidal nanotextures for coupling light into c-Si thin-film solar cells". *Opt. Express*, 24(6):A569, 2016.

[73] C. Ulbrich, S. Fahr, J. Üpping, M. Peters, T. Kirchartz, C. Rockstuhl, R.f Wehrspohn, A. Gombert, F. Lederer, and U. Rau. "Directional selectivity and ultra-light-trapping in solar cells". *Phys. Status Solidi Appl. Mater. Sci.*, 205(12):2831–2843, 2008.

[74] V. Jovanov, U. Planchoke, P. Magnus, H. Stiebig, and D. Knipp. "Influence of back contact morphology on light trapping and plasmonic effects in microcrystalline silicon single junction and micromorph tandem solar cells". *Sol. Energy Mater. Sol. Cells*, 110:49–57, 2013.

[75] W.-C. Hsu, J. K. Tong, M. S. Branham, Y. Huang, S. Yerci, S. V. Boriskina, and G. Chen. "Mismatched front and back gratings for optimum light trapping in ultra-thin crystalline silicon solar cells". *Opt. Commun.*, 377:52–58, 2016.

[76] M. Boccard, P. Cuony, C. Battaglia, S. Haenni, S. Nicolay, L. Ding, M. Benkhaira, G. Bugnon, A. Billet, M. Charriere, K. Soederstroem, J. Escarre, F. Sculati-Meillaud, M. Despeisse, and C. Ballif. "Nanometer- and Micrometer-Scale Texturing for High-Efficiency Micromorph Thin-Film Silicon Solar Cells". *IEEE J. Photovoltaics*, 2(2):83–87, 2012.

[77] X. Meng, E. Drouard, G. Gomard, R. Peretti, A. Fave, and C. Seassal. "Combined front and back diffraction gratings for broad band light trapping in thin film solar cell". *Opt. Express*, 20(S5):A560, 2012.

[78] J. Zhao and M. A. Green. "Optimized antireflection coatings for high-efficiency silicon solar cells". *IEEE Trans. Electron Devices*, 38(8):1925–1934, 1991.

[79] R. B. Wehrspohn, U. Rau, and A. Gombert, editors. *"Photon Management in Solar Cells"*. Wiley-VCH, 2015.

[80] J. Escarre, K. Soederstroem, M. Despeisse, S. Nicolay, C. Battaglia, G. Bugnon, L. Ding, F. Meillaud, F.-J. Haug, and C. Ballif. "Geometric light trapping for high efficiency thin film silicon solar cells". *Sol. Energy Mater. Sol. Cells*, 98:185–190, 2012.

[81] A. Lin, Y.-K. Zhong, and S.-M. Fu. "Comparison of nano-structured solar cell anti-reflection coating based on graded-index or mode coupling approach". *Photonics Nanostructures - Fundam. Appl.*, 12(5):493–500, 2014.

[82] C. Ballif, J. Dicker, D. Borchert, and T. Hofmann. "Solar glass with industrial porous SiO_2 antireflection coating: Measurements of photovoltaic module properties improvement and modelling of yearly energy yield gain". *Sol. Energy Mater. Sol. Cells*, 82(3):331–344, 2004.

[83] S. Chattopadhyay, Y. F. Huang, Y. J. Jen, A. Ganguly, K. H. Chen, and L. C. Chen. "Anti-reflecting and photonic nanostructures". *Mater. Sci. Eng. R Reports*, 69(1-3):1–35, 2010.

[84] D. G. Chen. "Anti-reflection (AR) coatings made by sol-gel processes: A review". *Sol. Energy Mater. Sol. Cells*, 68(3-4):313–336, 2001.

[85] K. Katagiri, S.-I. Yamazaki, K. Inumaru, and K. Koumoto. "Anti-reflective coatings prepared via layer-by-layer assembly of mesoporous silica nanoparticles and polyelectrolytes". *Polym. J.*, 47(2):190–194, 2015.

[86] D. Amkreutz, W. D. Barker, S. Kuhnapfel, P. Sonntag, O. Gabriel, S. Gall, U. Bloeck, J. Schmidt, J. Haschke, and B. Rech. "Liquid-Phase Crystallized Silicon Solar Cells on Glass: Increasing the Open-Circuit Voltage by Optimized Interlayers for n- and p-Type Absorbers". *IEEE J. Photovoltaics*, 5(6):1757–1761, 2015.

[87] J. Haschke, D. Amkreutz, T. Frijnts, S. Kühnapfel, T. Hänel, and B. Rech. "Influence of Barrier and Doping Type on the Open-Circuit Voltage of Liquid Phase-Crystallized Silicon Thin-Film Solar Cells on Glass". *IEEE J. Photovoltaics*, 5:1001–1005, 2015.

[88] J. Dore, R. Evans, U. Schubert, B. D. Eggleston, D. Ong, K. Kim, J. Huang, O. Kunz, M. Keevers, R. Egan, S. Varlamov, and M. A. Green. "Thin-film polycrystalline silicon solar cells formed by diode laser crystallisation". *Prog. Photovoltaics Res. Appl.*, 21(6):1377–1383, 2013.

[89] M. A. Green. "Lambertian light trapping in textured solar cells and light-emitting diodes: analytical solutions". *Prog. Photovoltaics Res. Appl.*, 10(4):235–241, 2002.

[90] C. Battaglia, M. Boccard, F.-J. Haug, and C. Ballif. "Light trapping in solar cells: When does a Lambertian scatterer scatter Lambertianly?". *J. Appl. Phys.*, 112(9):094504, 2012.

[91] J. Müller, B. Rech, J. Springer, and M. Vanecek. "TCO and light trapping in silicon thin film solar cells". *Sol. Energy*, 77(6):917–930, 2004.

[92] C. Battaglia, K. Söderström, J. Escarré, F.-J. Haug, D. Dominé, P. Cuony, M. Boccard, G. Bugnon, C. Denizot, M. Despeisse, A. Feltrin, and C. Ballif. "Efficient light management scheme for thin film silicon solar cells via transparent random nanostructures fabricated by nanoimprinting". *Appl. Phys. Lett.*, 96:213504, 2010.

[93] T. Minami, T. Miyata, R. Uozaki, H. Sai, and T. Koida. "Textured surface structures formed using new techniques on transparent conducting Al-doped zinc oxide films prepared by magnetron sputtering". *Thin Solid Films*, 614:56–61, 2016.

[94] X. Liu, P. R. Coxon, M. Peters, B. Hoex, J. M. Cole, and D. J. Fray. "Black silicon: fabrication methods, properties and solar energy applications". *Energy Environ. Sci.*, 7(10):3223–3263, 2014.

[95] C. Trompoukis, O. El Daif, V. Depauw, I. Gordon, and J Poortmans. "Photonic assisted light trapping integrated in ultrathin crystalline silicon solar cells by nanoimprint lithography". *Appl. Phys. Lett.*, 101(10):103901, 2012.

[96] C. Battaglia, C.-M. Hsu, K. Söderström, J. Escarré, F. J. Haug, M. Charriére, M. Boccard, M. Despeisse, D. T. L. Alexander, M. Cantoni, Y. Cui, and C. Ballif. "Light trapping in solar cells: Can periodic beat random?". *ACS Nano*, 6(3):2790–2797, 2012.

[97] P. Campbell and M. A. Green. "The Limiting Efficiency of Silicon Solar Cells under Concentrated Sunlight". *IEEE Trans. Electron Devices*, 33(2):234–239, 1986.

[98] Z. Yu, A. Raman, and S. Fan. "Fundamental limit of nanophotonic light trapping in solar cells". In *Proc. Natl. Acad. Sci. USA*, volume 107, pages 17491–17496, 2010.

[99] Y. Wang, R. Luo, J. Ma, and S.-Q. Man. "Fabrication of the pyramidal microstructure on silicon substrate using KOH solution". *5th International Conference on Advanced Engineering Materials and Technology*, 5:302–307, 2015.

[100] Crystal Impact GbR. "Diamond Crystal and Molecular Structure Visualization". `http://www.crystalimpact.com/diamond/`, 2016.

[101] A. M. C. S. Database. "Silicon". `http://rruff.geo.arizona.edu/AMS/minerals/Silicon`, 2015. Accessed: 19-Oct-2016.

[102] D. Madzharov, R. Dewan, and D. Knipp. "Influence of front and back grating on light trapping in microcrystalline thin-film silicon solar cells". *Opt. Express*, 19(S2):A95, 2011.

[103] T. K. Chong, J. Wilson, S. Mokkapati, and K. R. Catchpole. "Optimal wavelength scale diffraction gratings for light trapping in solar cells". *J. Opt.*, 14:024012, 2012.

[104] B. Bläsi, H. Hauser, C. Walk, B. Michl, A. Guttowski, Benick H. Mellor A., M. Peters, S. Jüchter, C. Wellens, V. Kübler, M. Hermle, and A. J. Wolf.

"Photon Management Structures for Solar Cells". *Proc. SPIE*, 8428:8438Q–1 – 8438Q–12, 2012.

[105] M. van Lare, F. Lenzmann, and A. Polman. "Dielectric back scattering patterns for light trapping in thin-film Si solar cells". *Opt. Express*, 21(18):20738, 2013.

[106] S. Varlamov, Z. Ouyang, X. Zhao, and D. S. Jung. "Surface Plasmon Enhanced Light-Trapping in polycrystalline Silicon Thin-Film Solar". In *Proc. photonics Glob. Conf. Sydney, Aust.*, 2010.

[107] J. Escarre, C. Battaglia, K. Soederstroem, C. Pahud, R. Biron, O. Cubero, F.-J. Haug, and C. Ballif. "UV imprinting for thin film solar cell application". *J. Opt.*, 14(2):024009 (8pp), 2012.

[108] F J. Haug, A. Naqavi, and C. Ballif. "Diffraction and absorption enhancement from textured back reflectors of thin film solar cells". *Appl. Phys. Lett.*, 112(2):24516–24517, 2012.

[109] Z. Ouyang, S. Pillai, F. Beck, O. Kunz, S. Varlamov, K. Catchpole, P. Campbell, and M. Green. "Effective light trapping in polycrystalline silicon thin-film solar cells by means of rear localized surface plasmons". *Appl. Phys. Lett.*, 96:261109, 2010.

[110] E. Yablonovitch. "Statistical ray optics". *J. Opt. Soc. Am.*, 72(7):899, 1982.

[111] T. Tiedje, E. Yablonovitch, G.D. Cody, and B.G. Brooks. "Limiting efficiency of silicon solar cells". *IEEE Trans. Electron Devices*, 31(5):711–716, 1984.

[112] S. Mokkapati and K. R. Catchpole. "Nanophotonic light trapping in solar cells". *J. Appl. Phys.*, 112(101101):101101 (19pp), 2012.

[113] Stuart A. Boden and Darren M. Bagnall. "Optimization of moth-eye antireflection schemes for silicon solar cells". *Prog. Photovoltaics Res. Appl.*, 18(3):195–203, 2010.

[114] D. M. Callahan, J. N. Munday, and H. A. Atwater. "Solar Cell Light Trapping beyond the Ray Optic Limit". *Nano Lett.*, 12(1):214–218, 2012.

[115] W. Hayes and A. M. Stoneham. *"Defects and defect processes in nonmetallic solids"*. John Wiley & Sons Inc, 1. edition, 1985.

[116] J. P. Hirth and J. Lothe. *"Theory of Dislocations"*. Krieger Publishing Company, 1991.

[117] D. Hull and D.J. Bacon. *"Introduction to Dislocations"*. Butterworth-Heinemann, 2011.

[118] H. Föll. "Defects in Crystals". `http://www.tf.uni-kiel.de/matwis/amat/def{_}en/index.html`, 2016.

[119] S.M. Sze and Kwok K. Ng. *"Physics of Semiconductor Devices"*, volume 10 of *Environmental Science and Engineering*. John Wiley & Sons, Inc., Hoboken, NJ, USA, 2006.

[120] S. Steffens, C. Becker, D. Amkreutz, A. Klossek, M. Kittler, Y. Y. Chen, A. Schnegg, M. Klingsporn, D. Abou-Ras, K. Lips, and B. Rech. "Impact of dislocations and dangling bond defects on the electrical performance of crystalline silicon thin films". *Appl. Phys. Lett.*, 105(2):0–5, 2014.

[121] N. M. Johnson. "Deuterium passivation of grain-boundary dangling bonds in silicon thin films". *Appl. Phys. Lett.*, 40(10):882, 1982.

[122] R. F. Pierret. *"Advanced Semiconductor Fundamentals"*. Pearson, 2nd edition, 2002.

[123] A. Goetzberger, B. Voss, and J. Knobloch. *"Sonnenenergie: Photovoltaik"*. Teubner, 2nd edition, 1997.

[124] D. Amkreutz, J. Haschke, S. Kuhnapfel, P. Sonntag, and B. Rech. "Silicon Thin-Film Solar Cells on Glass With Open-Circuit Voltages Above 620 mV Formed by Liquid-Phase Crystallization". *IEEE J. Photovoltaics*, 4(6):1496–1501, 2014.

[125] A. B. Sproul. "Dimensionless solution of the equation describing the effect of surface recombination on carrier decay in semiconductors". *J. Appl. Phys.*, 76(5):2851, 1994.

[126] B. Gorka, B. Rau, P. Dogan, C. Becker, F. Ruske, S. Gall, and B. Rech. "Influence of hydrogen plasma on the defect passivation of polycrystalline Si thin film solar cells". *Plasma Process. Polym.*, 6:36–40, 2009.

[127] S. W. Glunz, D. Biro, S. Rein, and W. Warta. "Field-effect passivation of the SiO_2 Si interface". *J. Appl. Phys.*, 86(1):683, 1999.

[128] J. R. Elmiger and M. Kunst. "Investigation of charge carrier injection in silicon nitride/silicon junctions". *Appl. Phys. Lett.*, 69(4):517, 1996.

[129] S. W. Glunz, A. B. Sproul, W. Warta, and W. Wettling. "Injection-level-dependent recombination velocities at the Si-SiO2 interface for various dopant concentrations". *J. Appl. Phys.*, 75(3):1611, 1994.

[130] T. Markvart and L. Castañer. "Principles of Solar Cell Operation". In *Pract. Handb. Photovoltaics*, pages 7–31. Elsevier, 2012.

[131] L. Fraas and L. Partain, editors. *"Solar Cells and their Applications"*. John Wiley & Sons, 2010.

[132] E. A. Costner, M. W. Lin, W.-L. Jen, and C. G. Willson. "Nanoimprint Lithography Materials Development for Semiconductor Device Fabrication". *Annu. Rev. Mater. Res.*, 39:155–180, 2009.

[133] C. Peroz, V. Chauveau, E. Barthel, and E. Sondergard. "Nanoimprint Lithography on Silica Sol-Gels: A Simple Route to Sequential Patterning". *Adv. Mater.*, 21(5):555+, 2009.

[134] F. Schlachter, J. Barnett, U. Plachetka, C. Nowak, M. Messerschmidt, M. Thesen, and H. Kurz. "UV-NIL based nanostructuring of aluminum using a novel organic imprint resist demonstrated for 100 nm half-pitch wire grid polarizer". *Microelectron. Eng.*, 155:118–121, 2016.

[135] C. Pina-Hernandez, V. Lacatena, G. Calafiore, S. Dhuey, K. Kravtsov, A. Goltsov, D. Olynick, V. Yankov, S. Cabrini, and C. Peroz. "A route for fabricating printable photonic devices with sub-10 nm resolution". *Nanotechnology*, 24(6):065301, 2013.

[136] Q. Jiao, Z. Chen, Y. Feng, S. Li, S. Jiang, J. Li, Y. Chen, T. Yu, X. Kang, B. Shen, and G. Zhang. "The effects of nanocavity and photonic crystal in InGaN/GaN nanorod LED arrays". *Nanoscale Res. Lett.*, 11(1):340, 2016.

[137] L. Jacot-Descombes, V. J. Cadarso, A. Schleunitz, S. Grützner, J. J. Klein, J. Brugger, H. Schift, and G. Grützner. "Organic-inorganic-hybrid-polymer microlens arrays with tailored optical characteristics and multi-focal properties". *Opt. Express*, 23(19):25365, 2015.

[138] A. Mellor, H. Hauser, C. Wellens, J. Benick, J. Eisenlohr, M. Peters, A. Guttowski, I. Tobías, A. Martí, A. Luque, and B. Bläsi. "Nanoimprinted diffraction gratings for crystalline silicon solar cells: implementation, characterization and simulation". *Opt. Express*, 21(S2):A295, 2013.

[139] U. W. Paetzold, W. Qiu, F. Finger, J. Poortmans, and D. Cheyns. "Nanophotonic front electrodes for perovskite solar cells". *Appl. Phys. Lett.*, 106(17):173101, 2015.

[140] K. Wilken, U. W. Paetzold, M. Meier, N. Prager, M. Fahland, F. Finger, and V. Smirnov. "Nanoimprint texturing of transparent flexible substrates for improved light management in thin-film solar cells". *Phys. status solidi - Rapid Res. Lett.*, 9(4):215–219, 2015.

[141] E. Rudigier-Voigt, M. Bockmeyer, V. Hagemann, and S. Bauer. "Sol-gel based structuring of the front electrode in Si-based thin film PV device". In *Proc. 24th Eur. Photovolt. Conf. 2009, Hamburg, Ger.*, pages 2884–2886, 2009.

[142] A. J. Wolf, H. Hauser, V. Kübler, C. Walk, O. Höhn, and B. Bläsi. "Origination of nano- and microstructures on large areas by interference lithography". *Microelectron. Eng.*, 98:293–296, 2012.

[143] C. Huelsen, J. Probst, and B. Loechel. "Replication of sub-100 nm structures using h- and s-PDMS composite stamps". *Microsyst. Technol.*, 20:2001–2004, 2014.

[144] Gu. Yang, R.A.C.M.M. van Swaaij, H. Tan, O. Isabella, and M. Zeman. "Modulated surface textured glass as substrate for high efficiency microcrystalline silicon solar cells". *Sol. Energy Mater. Sol. Cells*, 133:156–162, 2015.

[145] D. Eisenhauer, G. Köppel, K. Jäger, D. Chen, O. Shargaieva, P. Sonntag, D. Amkreutz, B. Rech, and C. Becker. "Smooth anti-reflective three-dimensional textures for liquid-phase crystallized silicon thin-film solar cells on glass". *Sci. Rep.*, 2017. accepted.

[146] J. Dore, R. Evans, B. Eggleston, S. Varlamov, and M. A. Green. "Intermediate Layers for Thin-Film and Polycrystalline Silicon and Solar Cells and on Glass and Formed by Diode Laser Crystallization". In *MRS Proc.*, volume 1426, pages 63–68, 2012.

[147] I. Höger, M. Himmerlich, A. Gawlik, U. Brückner, S. Krischok, and G. Andrä. "Influence of intermediate layers on the surface condition of laser crystallized silicon thin films and solar cell performance". *J. Appl. Phys.*, 119(4):045306, 2016.

[148] T. Merkel, J .and Sontheimer, B. Rech, and C. Becker. "Directional growth and crystallization of silicon thin films prepared by electron-beam evaporation on oblique and textured surfaces". *J. Cryst. Growth*, 367:126–130, 2012.

[149] D. Amkreutz, J. Haschke, T. Häring, F. Ruske, and B. Rech. "Conversion efficiency and process stability improvement of electron beam crystallized thin film silicon solar cells on glass". *Sol. Energy Mater. Sol. Cells*, 123:13–16, 2014.

[150] J. Haschke, D. Amkreutz, and B. Rech. "Liquid phase crystallized silicon on glass: Technology, material quality and back contacted heterojunction solar cells". *Jpn. J. Appl. Phys.*, 55(4S):04EA04, 2016.

[151] M. Mews, T. F. Schulze, N. Mingirulli, and L. Korte. "Hydrogen plasma treatments for passivation of amorphous-crystalline silicon-heterojunctions on surfaces promoting epitaxy". *Appl. Phys. Lett.*, 102(12):122106, 2013.

[152] P. Eaton and P. West. *"Atomic Force Microscopy"*. Oxford University Press, 2010.

[153] L. Reimer. *"Scanning Electron Microscopy: Physics of Image Formation and Microanalysis"*. Springer, 2nd edition, 1998.

[154] R.F. Egerton. *"Physical Principles of Electron Microscopy: An Introduction to TEM, SEM, and AEM"*, volume 1. Springer US, 2005.

[155] H. Haferkorn, editor. *"Optik: Physikalisch-technische Grundlagen und Anwendungen"*. John Wiley & Sons, 4th edition, 2002.

[156] EDAX. "Orientation Imaging Microscopy (OIM) Analysis". `http://www.edax.com/Products/EBSD/OIM-Data-Analysis-Microstructure-Analysis.aspx`.

[157] M. W. Finkel. "Integrating sphere theory". *Opt. Commun.*, 2(1):25–28, 1970.

[158] A. Roos. "Use of an integrating sphere in solar energy research". *Sol. Energy Mater. Sol. Cells*, 30(1):77–94, 1993.

[159] L. Hanssen. "Integrating-sphere system and method for absolute measurement of transmittance, reflectance, and absorptance of specular samples". *Appl. Opt.*, 40(19):3196, 2001.

[160] F. J. J. Clarke and J. A. Compton. "Correction methods for integrating-sphere measurement of hemispherical reflectance". *Color Res. Appl.*, 11(4):253–262, 1986.

[161] A. V. Prokhorov, S. N. Mekhontsev, and L. M. Hanssen. "Analytical evaluation and correction of port loss error in integrating sphere reflectometers". In Leonard M. Hanssen, editor, *Proceedings of SPIE*, page 69, 2003.

[162] A. M. Nilsson, A. Jonsson, J. C. Jonsson, and A. Roos. "Method for more accurate transmittance measurements of low-angle scattering samples using an integrating sphere with an entry port beam diffuser". *Appl. Opt.*, 50(7):999, 2011.

[163] PVeducation.org. "Quantum Efficiency". `http://www.pveducation.org/pvcdrom/solar-cell-operation/quantum-efficiency`, 2016.

[164] M. Wolf and H. Rauschenbach. "Series resistance effects measurements". *Adv. Energy Convers.*, 3(2):455–479, 1963.

[165] R. A. Sinton, A. Cuevas, and M. Stuckings. "Quasi-steady-state photoconductance, a new method for solar cell material and device characterization". *Conf. Rec. Twenty Fifth IEEE Photovolt. Spec. Conf.*, 25:457–460, 1996.

[166] R.A. Sinton and A. Cuevas. "A quasi-steady-state open-circuit voltage method for solar cell characterization". *16th European Photovoltaic Solar Energy Conference*, 16(May):1–4, 2000.

[167] M. J. Kerr and A. Cuevas. "Generalized analysis of the illumination intensity vs. open-circuit voltage of solar cells". *Sol. Energy*, 76(1-3):263–267, 2004.

[168] S. Bowden, V. Yelundur, and A. Rohatgi. "Implied-Voc and Suns-Voc measurements in multicrystalline solar cells". In *25th Photovolt. Spec. IEEE Conf.*, pages 371–374. IEEE, 2002.

[169] S. Martinuzzi and M. Stemmer. "Mapping of defects and their recombination strenght by a light-beam-induced current in silicon wafers". *Mater. Sci. Eng. B*, 24(1-3):152–158, 1994.

[170] N. M. Thantsha, E. Q. B. Macabebe, F. J. Vorster, and E. E. van Dyk. "Optoelectronic analysis of silicon solar cells by LBIC investigations and current-voltage characterization". *Phys. B Condens. Matter*, 404(22):4445–4448, 2009.

[171] M. Rinio, H. J. Moller, and M. Werner. "LBIC investigations of the lifetime degradation by extended defects in multicrystalline solar silicon". *Solid State Phenomena*, 63–64(4):115–122, 1999.

[172] G. Micard, G. Hahn, and B. Terheiden. "Injection in light beam induced current systems : An analytical model". *Phys. Status Solidi*, 11(5):1–11, 2016.

[173] F. Secco d' Aragona. "Dislocation Etch for (100) Planes in Silicon". *J. Electrochem. Soc.*, 119(7):948, 1972.

[174] A. Abbadie, J.-M. Hartmann, and F. Brunier. "A Review of Different and Promising Defect Etching Techniques: from Si to Ge". In *ECS Trans.*, volume 10, pages 3–19. ECS, 2007.

[175] G. Kissinger and S. Pizzini. *"Silicon, Germanium, and Their Alloys: Growth, Defects, Impurities, and Nanocrystals"*. CRC Press, 2015.

[176] M. Fathi. "Delineation of crystalline extended defects on multicrystalline silicon wafers". *Int. J. Photoenergy*, 2007:4, 2007.

[177] Z. Iqbal and S. Veprek. "Raman scattering from hydrogenated microcrystalline and amorphous silicon". *J. Phys. C Solid State Phys.*, 15:377–392, 1982.

[178] W. Qiu and Y.-L. Kang. "Mechanical behavior study of microdevice and nanomaterials by Raman spectroscopy: a review". *Chinese Sci. Bull.*, 59(23):2811–2824, 2014.

[179] G. Gouadec and P. Colomban. "Raman Spectroscopy of nanomaterials: How spectra relate to disorder, particle size and mechanical properties". *Prog. Cryst. Growth Charact. Mater.*, 53(1):1–56, 2007.

[180] M. Ledinský, E. Moulin, G. Bugnon, K. Ganzerová, A. Vetushka, F. Meillaud, A. Fejfar, and C. Ballif. "Light trapping in thin-film solar cells measured by Raman spectroscopy". *Appl. Phys. Lett.*, 105(11):111106, 2014.

[181] C. Droz, E. Vallat-Sauvain, J. Bailat, L. Feitknecht, J. Meier, and A. Shah. "Relationship between Raman crystallinity and open-circuit voltage in microcrystalline silicon solar cells". *Sol. Energy Mater. Sol. Cells*, 81(1):61–71, 2004.

[182] J. Pomplun, S. Burger, L. Zschiedrich, and F. Schmidt. "Adaptive finite element method for simulation of optical nano structures". *Phys. status solidi*, 244(10):3419–3434, 2007.

[183] M. Hammerschmidt, D. Lockau, S. Burger, F. Schmidt, C. Schwanke, S. Kirner, S. Calnan, B. Stannowski, and B. Rech. "FEM-based optical modeling of silicon thin-film tandem solar cells with randomly textured interfaces in 3D". *Proc. SPIE*, 8620:86201H–1 – 86201H–9, 2013.

[184] S. Kühnapfel, J. Huang, A. Teal, H. Kampwerth, D. Amkreutz, S. Gall, and S. Varlamov. "Lifetime analysis of laser crystallized silicon films on glass". *J. Appl. Phys.*, 118(5):055304, 2015.

[185] D. Lockau, M. Hammerschmidt, J. Haschke, M. Blome, F. Ruske, F. Schmidt, and B. Rech. "A comparison of scattering and non-scattering anti-reflection designs for back contacted polycrystalline thin film silicon solar cells in superstrate configuration". *Proc. SPIE*, 9140:914006, 2014.

[186] K. Jäger, G. Köppel, C. Barth, M. Hammerschmidt, S. Herrmann, S. Burger, F. Schmidt, and C. Becker. "Sinusoidal gratings for optimized light management in c-Si thin-film solar cells". In *Proc. SPIE*, volume 9898, 2016.

[187] H. Nussbaumer, G. Willeke, and E. Bucher. "Optical behavior of textured silicon". *J. Appl. Phys.*, 75(4):2202, 1994.

[188] C. Becker, P. Wyss, D. Eisenhauer, J. Probst, V. Preidel, M. Hammerschmidt, and S. Burger. "5x5 cm^2 silicon photonic crystal slabs on glass and plastic foil exhibiting broadband absorption and high-intensity near-fields". *Sci. Rep.*, 4:5886, 2014.

[189] K. Jäger, C. Barth, M. Hammerschmidt, S. Herrmann, S. Burger, F. Schmidt, and C. Becker. "Sinusoidal Nanotextures for Coupling Light into c-Si Thin-Film Solar Cells". In *Light. Energy Environement 2015*, page PTu4B.3, Washington, D.C., 2015. OSA.

[190] M. Vetter, A. Gawlik, J. Plentz, and G. Andrä. "Carrier Lifetime in Liquid-phase Crystallized Silicon on Glass". *Energy Procedia*, 92:248–254, 2016.

[191] K. Jäger, M. Hammerschmidt, G. Köppel, S. Burger, and C. Becker. "On Accurate Simulations of Thin-Film Solar Cells With a Thick Glass Superstrate". In *Light, Energy and the Environment*, page PM3B.5. Optical Society of America, OSA Technical Digest (online), 2016.

[192] G. Köppel, B. Rech, and C. Becker. "Sinusoidal nanotextures for light management in silicon thin-film solar cells". *Nanoscale*, 8(16):8722–8728, 2016.

[193] B. Rech G. Köppel, D. Eisenhauer and Ch. Becker. "Combining tailor-made textures for light in-coupling and light trapping in liquid phase crystallized silicon thin-film solar cells". *Opt. Express*, 25(12):A467–A472, 2017.

[194] G. Köppel, V. Preidel, S. Mangold, E. Rudigier-Voigt, M. Hývl, A. Fejfar, B. Rech, and C. Becker. "Nanoimprint-textured Glass Superstrates for Light Trapping in Crystalline Silicon thin-film Solar Cells". *Energy Procedia*, 84:118–126, 2015.

[195] O. Gabriel, T. Frijnts, N. Preissler, D. Amkreutz, S. Calnan, S. Ring, B. Stannowski, B. Rech, and R. Schlatmann. "Crystalline silicon on glass-interface passivation and absorber material quality". *Prog. Photovoltaics Res. Appl.*, 20(1), 2015.

[196] P. Sonntag, J. Haschke, S. Kühnapfel, T. Frijnts, D. Amkreutz, and B. Rech. "Interdigitated back-contact heterojunction solar cell concept for liquid phase crystallized thin-film silicon on glass". *Prog. Photovoltaics Res. Appl.*, 20(1):716–724, 2015.

[197] M. Peters, M. Rüdiger, H. Hauser, M. Hermle, and B. Bläsi. "Diffractive gratings for crystalline silicon solar cells-optimum parameters and loss mechanisms". *Prog. Photovoltaics Res. Appl.*, 20(7):862–873, 2012.

[198] M. Boccard, C. Battaglia, S. Hänni, K. Söderström, J. Escarré, S. Nicolay, F. Meillaud, M. Despeisse, and C. Ballif. "Multiscale Transparent Electrode Architecture for Efficient Light Management and Carrier Collection in Solar Cells". *Nano Lett.*, 12(3):1344–1348, 2012.

[199] W. B. Jackson. "Density of gap states of silicon grain boundaries determined by optical absorption". *Appl. Phys. Lett.*, 43(2):195, 1983.

[200] S. Varlamov, J. Dore, R. Evans, D. Ong, B. Eggleston, O. Kunz, U. Schubert, T. Young, J. Huang, T. Soderstrom, K. Omaki, K. Kim, A. Teal, M. Jung, J. Yun, Z.M. Pakhuruddin, R. Egan, and M.A. Green. "Polycrystalline silicon on glass thin-film solar cells: A transition from solid-phase to liquid-phase crystallised silicon". *Sol. Energy Mater. Sol. Cells*, 119:246–255, 2013.

[201] T. Kuwahara, H. Ito, K. Kawaguchi, Y. Higuchi, N. Ozawa, and M. Kubo. "The reason why thin-film silicon grows layer by layer in plasma-enhanced chemical vapor deposition". *Sci. Rep.*, 5:9052, 2015.

[202] G. Köppel, D. Amkreutz, P. Sonntag, G. Yang, R. van Swaaij, O. Isabella, M. Zeman, B. Rech, and C. Becker. "Periodic and Random Substrate Textures for Liquid-Phase Crystallized Silicon Thin-Film Solar Cells". *IEEE J. Photovoltaics*, 7(1):85–90, 2016.

[203] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop. "Solar cell efficiency tables (version 48)". *Prog. Photovoltaics*, 25:905–913, 2016.

[204] G. Yang, R. van Swaaij, and O. Isabella. "A method for texturing a glass surface", 2015. WO Patent App. PCT/NL2014/050,895.

Appendices

A Supplementary Results

Interplay between crystallization direction and planar absorber layers

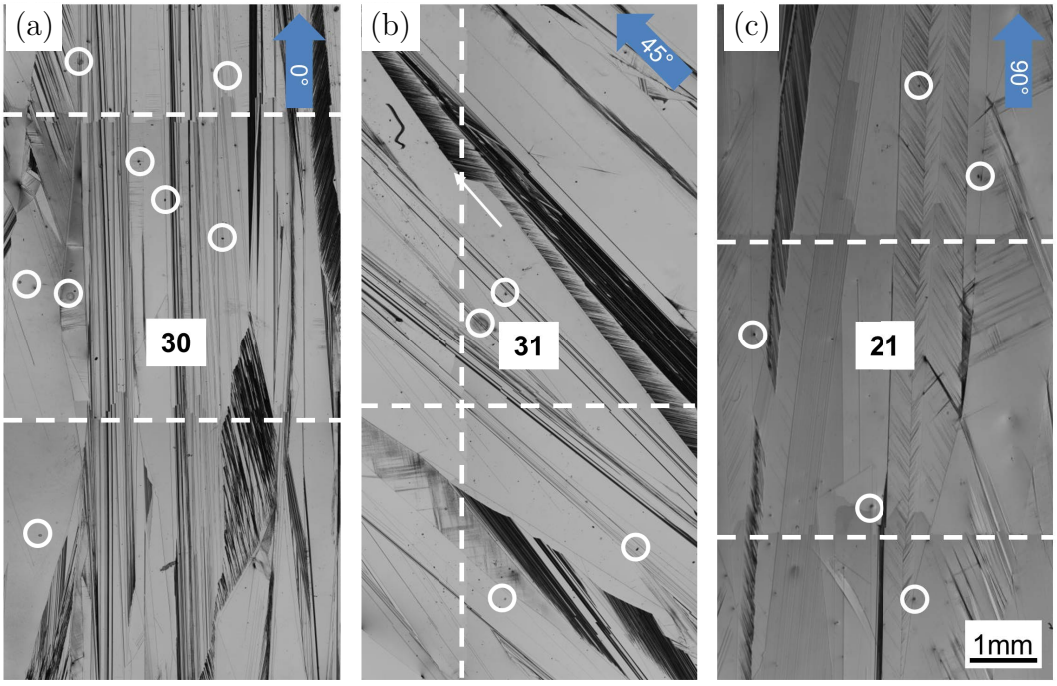


Figure A.1: Light microscope images of 10 µm thick absorber layers grown and crystallized on planar absorber layers. According to the experiment conducted on the one-dimensional line gratings, the crystallization direction was alternated by (a) 0°, (b) 45°, and (c) 90° as indicated by blue arrows as insets. The numbers in the middle of each image correspond to the number of grains counted depicted per unit area of 0.5 cm x 1 cm. Some defects are highlighted by white circles. The dashed line indicates a stitching line of the microscope.

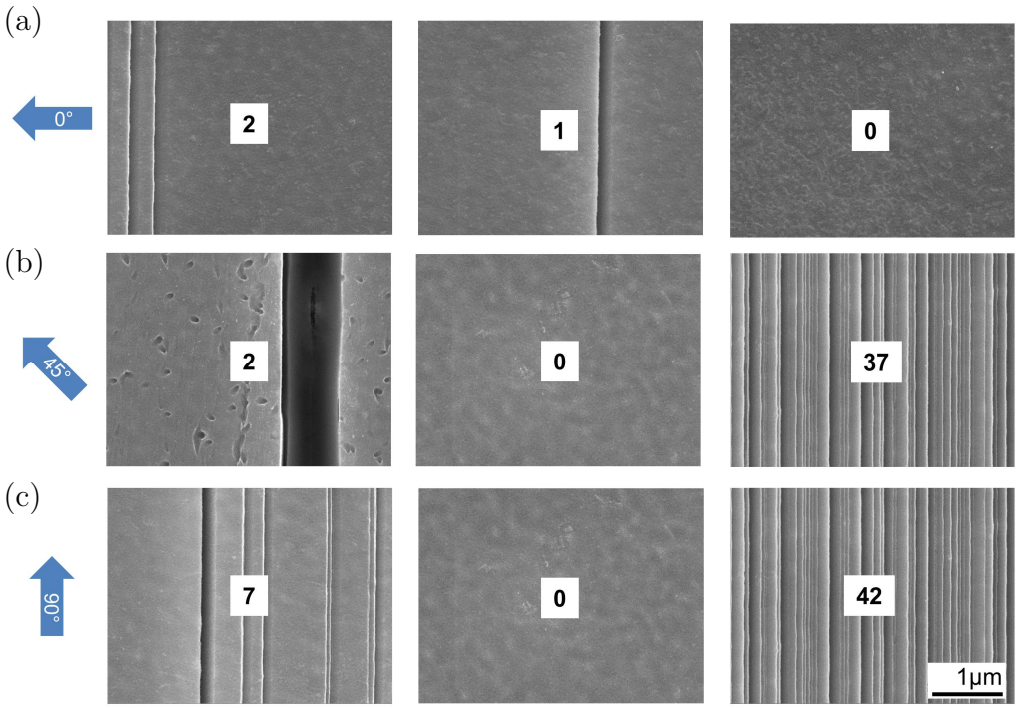


Figure A.2: SEM images of 10 µm thick LPC silicon absorber layers grown on planar substrates and crystallized in an angle of (a) 0°, (b) 45°, and (c) 90°. The crystallization directions are indicated by blue arrows. The numbers in the middle of every image refer to the number of defects counted in this image.

B Scientific Contributions

Patent Application

- Deutsches Patentamt 10 2016 107 877.8, "Lichtdurchlässiger Träger für einen halbleitenden Dünnschichtaufbau sowie Verfahren zur Herstellung und Anwendung des lichtdurchlässigen Trägers", angemeldet: 28.04.2016, Helmholtz-Zentrum Berlin für Materialien und Energie, Erfinder: David Eisenhauer, **Grit Köppel**, Christiane Becker, Bernd Rech

Peer-Reviewed Publications

- **Grit Köppel**, Veit Preidel, Stephanie Mangold, Eveline Rudigier-Voigt, Matej Hývl, Antonin Fejfar, Bernd Rech, and Christiane Becker. "Nanoimprint-textured Glass Superstrates for Light Trapping in Crystalline Silicon thin-film Solar Cells". Energy Procedia, 84:118-126, 2015.

- **Grit Köppel**, Bernd Rech, and Christiane Becker. "Sinusoidal nanotextures for light management in silicon thin-film solar cells". Nanoscale, 8(16):8722-8728, 2016.

- **Grit Köppel**, Daniel Amkreutz, Paul Sonntag, Guangtao Yang, Rene van Swaaij, Olindo Isabella, Miro Zeman, Bernd Rech, and Christiane Becker. "Periodic and random substrate textures for liquid-phase crystallized silicon thin-film solar cells". IEEE Journal of Photovoltaics, pages 1–6, 2016.

- David Eisenhauer, **Grit Köppel**, Klaus Jäger, Duote Chen, Oleksandra Shargaieva, Bernd Rech, and Christiane Becker. "Smooth anti-reflective threedimensional textures for liquid-phase crystallized silicon thin-film solar cells on glass". submitted to Progress in Photovoltaics: Research and Applications (pre-print available online under: https://arxiv.org/abs/1609.06997), 2016.

- David Eisenhauer, Klaus Jäger, **Grit Köppel**, Bernd Rech, and Christiane Becker. "Optical properties of smooth anti-reflective three-dimensional textures for silicon thin-film solar cells". Energy procedia, accepted, 2016.

Conference Contributions

- **Grit Köppel**, Veit Preidel, Stephanie Mangold, Eveline Rudigier-Voigt, Matej Hývl, Antonin Fejfar, Bernd Rech, and Christiane Becker. "Nanoimprint-textured glass superstrates for light trapping in crystalline silicon thin-film solar cells". In EMRS 2015 Spring meeting, Lille, France, May 2015. European Materials Research Society.

- **Grit Köppel**, Daniel Amkreutz, Paul Sonntag, Guangtao Yang, René van Swaaij, Olindo Isabella, Miro Zeman, Bernd Rech, and Christiane Becker. "Facing the challenge of liquid phase crystallizing silicon on textured glass substrates". In Proc. 43rd IEEE Photovoltaic Spec. Conf., Portland, OR, USA, June 2016. Photovoltaic Specialist Conference (PVSC), 2016 IEEE 43rd. to be published.

- Klaus Jäger, **Grit Köppel**, Carlo Barth, Martin Hammerschmidt, Sven Herrmann, Sven Burger, Frank Schmidt, and Christiane Becker. "Sinusoidal gratings for optimized light management in c-si thin-film solar cells". In Proc. SPIE, volume 9898, 2016.

- David Eisenhauer, **Grit Köppel**, Bernd Rech, and Christiane Becker. "Angle resolved reflectivity analysis of textured substrates for liquid-phase crystallized silicon thin-film solar cells". In Light, Energy and the Environment, page JW4A.35. Optical Society of America, OSA Technical Digest (online), 10.1364/FTS.2016.JW4A.35, 2016.

- David Eisenhauer, **Grit Köppel**, Klaus Jäger, Bernd Rech, and Christiane Becker. "Imprinted Nanostructures for Light Management in Crystalline Silicon Thin-Film Solar Cells on Glass". In Light, Energy and the Environment, page PM2B.5. Optical Society of America, OSA Technical Digest (online), 10.1364/PV.2016.PM2B.5, 2016.

- Klaus Jäger, Martin Hammerschmidt, **Grit Köppel**, Sven Burger, and Christiane Becker. "On accurate simulations of thin-film solar cells with a thick glass superstrate". In Light, Energy and the Environment, PM3B.5 OSA Technical Digest (online), 10.1364/PV.2016.PM3B.5, 2016.

C Acknowledgement

Many individuals have made either direct or indirect contributions to this work and for that I am extremely grateful.
Foremost I would like to thank Prof. Dr. Bernd Rech and Prof. Dr. Christiane Becker who gave me the opportunity to work at HZB, supported me in all aspects and agreed to review my thesis. I would also like to thank Prof. Dr. Janez Krč and RNDr. Antonín Fejfar, CSc., for their precious time and efforts evaluating this thesis.
Deepest gratitude is owed to Prof. Dr. Christiane Becker and all members of her young investigator group. Dr. Klaus Jäger is acknowledged for developing and conducting optical simulations. Special thanks go to David Eisenhauer, Martin Krüger and Sebastian Roder who have been cheerful roommates, helpful co-workers and have become good friends. Thank you all for keeping me on track through the highs and lows.
I am indebted to Dr. Veit Preidel. Upon his legacy and fruitful discussions much of this work is built. I hope this thesis will be worthy to share a shelf with his. Likewise, I am grateful for the support and patience of Philippe Wyss who introduced me to relevant technologies at HZB.
My gratitude goes to Antonín Fejfar and his group at the Academy of Sciences of the Czech Republic for the warm welcome and allowing me to be part of their group for three weeks. This was made possible by a scientific exchange program between the groups of Prof. Dr. Christiane Becker and RNDr. Antonín Fejfar, CSc., who funded this experience. The Raman measurements included in this thesis were conducted with the help of Kristina Ganzerova and Martin Ledinský. During my time in Prague, Kristina Ganzerova, Matěj Hývl, and Peter Pikna have all helped me with words, deeds and continuing friendship.
I would like to thank Stephanie Mangold and Dr. Eveline Rudigier-Voigt for giving me the opportunity to work at SCHOTT AG for two days. They made me feel welcome and provided valuable insights into working with nanoimprint lithography.
Dr. Daniel Amkreutz, Dr. Olindo Isabella and Dr. R.A.C.M.M. van Swaaij I would like to thank for allowing me to participate in their collaboration on implementing

randomly textured glass substrates into LPC silicon thin-film solar cells. All of them provided valuable support and helped with suggestions and discussions.
This work is built onto a foundation of hard working scientists, technicians and staff from HZB, EE-IS, PVcomB, Bessy, the Academy of Sciences of the Czech Republic and TU Berlin who keep everything running. For that I am extremely grateful. Marion Krusche, Martin Krüger, Holger Rhein, Conrad Erhard, Daniel Amkreutz, Paul Sonntag, Carola Klimm, Martin Muske, Mona Wittig, Charlene Last, Kerstin Jacob, Thomas Lußky, Andreas von Kozierowski, Tobias Hänel, and Karolina Mack deserve special thanks.
My thanks also go to Marion Krusche for being "Die gute Fee am HZB", her support far exceeding her work-duties and making impossible things possible.
Prof. Dr. Christian Pettenkofer is acknowledged for thinking outside the box and enlightening my introduction.
I also like to thank the "Lunch-Gang" for their help, honesty and friendship. They are just a few of the many friends in many places who have helped me over the last few years to sometimes focus on my work and to sometimes forget it. I thank everyone for their role in keeping me balanced.
My family and friends I let know in person how grateful I am for the continuing loving support and tireless patience.
I apologize for everyone I might have missed out. Without your tremendous help this work would not have been possible.

D Declaration

Hiermit versichere ich, dass ich diese Arbeit selbstständig verfasst und keine anderen als die angegebenen Hilfsmittel und Quellen benutzt habe.

Berlin, 28.11.2016 Grit Köppel