Thermo-Mechanical Reliability of Flip-Chip Assemblies with Heat-Spreaders

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Thermo-Mechanical Reliability of Flip-Chip Assemblies with Heat-Spreaders

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Summary

The concept in flip-chip technology, to cool a chip by attaching its electrically inactive reverse side to the heat-spreading cover of e.g. a controller-housing, represents a very promising solution to thermal management problems encountered in automotive applications. However, its technological realization imposes new mechanical constraints on the flip-chip assembly which have an influence on its thermo-mechanical reliability.

Whereas the unconstrained flip-chip assembly without reverse side cooling has been in the focus of reliability studies for a long time, the loading induced by additional mechanical constraints caused by the attachment of the heat-spreader and hence its impact on solder bump reliability are still largely unknown. To qualify the typical load situation and to quantify the lifetime as a function of appropriate variables is therefore a fundamental prerequisite for a reliable design and its optimization by virtual prototyping. Consequently, there is a need for a comprehensive study to provide adequate design rules.

This thesis comprises analysis, assessment and prediction of solder bump reliability for flip-chip assemblies on organic board. These assemblies are subjected to various influential mechanical constraints under periodic thermal load in simulation and subsequent experiment.

A flexible, modular and parametric finite element model was developed to handle the required variations as to geometry, material and loads. The required material parameters were measured and made available to the software. Then the model was calibrated and optimized with respect to accuracy and speed. This allows a computational analysis of the reliability of eutectic tin-lead solder bumps, where the accumulated creep strain within the bump was evaluated as an appropriate failure criterion. For experimental verification especially designed test-assemblies underwent thermal cycling and were regularly checked for solder bump failure.

Experiment and simulation are in good agreement when compared within the framework of the Coffin-Manson low cycle fatigue damage approach. So for the first time a correlation could be established between lifetime and cooling for flip-chip assemblies.

It was found that flip-chip reverse side cooling represents a thermo-mechanically reliable option for modern high performance thermal management. However, an attached heat-spreader results in general in a lower reliability compared to the mechanically unconstrained flip-chip assembly.

The following variables could be shown to be representative and sufficient for the universal loading description of the assembly and to determine its reliability. Based on the resulting distinct ranking of the individual configurations the influence of the variables can be obtained:

The thickness of the board (a) has the strongest influence on lifetime, where thick boards do reduce reliability. This is particularly critical in combination with a fixation (b) of the board on the heat-spreader for reasons of thermal mismatch. Next, a displacement of the board (c) reduces lifetime proportionally to its value. Negative values of displacement, which cause a convex curvature of the chip, can also be realized and do even induce a small increase in reliability. As far as the thermal interface material (d) is concerned, gap-fillers yield slightly better results than adhesives. With adhesives a low stress bond at all

temperatures guarantees a higher reliability. The value of a compressive force (e) needed to displace the board does not have an effect.

Although the individual configurations differ, depending on applied loads and interface material, largely in chip deformation at low temperatures, this does not influences reliability to a large extent. Chip and bump are found to accommodate to the applied loads after a transient response phase. The critical situation for solder bump reliability is a continuing, enforced or constrained deformation of the chip at high temperatures which differs from the deformation behaviour of the mechanically unconstrained chip.

A novel set of design guidelines obtained from this study now allows technological realization of flip-chip assemblies with reverse side cooling featuring maximum solder joint reliability. Moreover, the presented analytical and numerical framework permits its future simulative prediction. The applied methodology can easily be extended to further configurations and transferred to related problems in microelectronic packaging facilitating their solution.

Zusammenfassung

Die Entwärmung von Flip-Chip Aufbauten über ihre elektrisch inaktive Rückseite ist ein sehr vielversprechendes Konzept für Chips mit höherer Verlustleistung. Dabei kann der Chip thermisch an das Gehäuse angekoppelt werden, wobei dieses gleichzeitig als Kühlkörper fungiert. Dies ist besonders interessant für Anwendungen im Kraftfahrzeugbereich (z.B. bei Steuergeräten). Durch die technische Realisierung dieses Konzeptes ist der Chip jedoch neuartigen mechanischen Belastungen unterworfen, welche seine thermomechanische Zuverlässigkeit beeinflussen.

Flip-Chip Aufbauten ohne spezielle Entwärmungsmaßnahmen sind schon seit längerer Zeit Gegenstand von Zuverlässigkeitsuntersuchungen. Für den immer wichtiger werdenden Fall der Rückseitenentwärmung hingegen ist der Belastungszustand des Chips, hervorgerufen durch die Befestigung des Kühlkörpers, ebenso wie dessen Auswirkungen auf die Zuverlässigkeit der Lotverbindungen (Bumps) noch immer größtenteils unbekannt. Eine Beschreibung der typischen Belastungssituation und die quantitative Ermittlung der Lebensdauer als Funktion geeigneter Variablen ist jedoch die Grundvoraussetzung für ein zuverlässiges Design und dessen Optimierung mittels simulativer Methoden. Deshalb erscheint eine umfassende Untersuchung zur Aufstellung von Designrichtlinien dringend notwendig.

Die vorliegende Arbeit umfaßt Analyse, Ermittlung und Vorhersage der Zuverlässigkeit von Lotverbindungen für Flip-Chip Aufbauten auf organischem Substrat unter verschieden mechanischen Randbedingungen und thermischer Wechselbelastung in Simulation und Experiment.

Um die erforderlichen Variationen bezüglich Geometrie, Material und Belastungsmodi einfach handhaben zu können, wurde ein flexibles, modular und parametrisch aufgebautes Finite Elemente Modell entwickelt. Die eingesetzten Materialien wurden charakterisiert und die gemessenen Daten implementiert. Danach konnten das Modell kalibriert und bezüglich Genauigkeit und Schnelligkeit in der Simulation optimiert werden.

Dies ermöglichte eine schnelle und genaue rechnergestützte Zuverlässigkeitsanalyse der eutektischen Zinn-Blei Lotverbingungen. Dabei ließen sich die akkumulierten Kriechdehungen im Lotbump als Schadenskriterium bewerten. Zur experimentellen Verifizierung wurden entsprechende Testvehikel entwickelt, Temperaturwechselbelastung unterworfen und in regelmäßigen Abständen auf Lotversagen getestet.

Experiment und Simulation konnten innerhalb des Coffin-Manson Ansatzes (Low Cycle Fatigue) miteinander korreliert werden und zeigten gute Übereinstimmung. Auf diese Weise ließ sich zum erstem Mal der Zusammenhang von Lebensdauer und Rckseitenentwärmung für Flip-Chip Aufbauten ermitteln.

Die getesteten Konfigurationen ergaben, daß die Rückseitenentwärmung von Flip-Chips ein zuverlässiges Konzept bezüglich der Thermomechanik darstellt. Trotzdem wird generell die Anbringung einer Wärmesenke, im Vergleich zu einem unbelasteten Flip-Chip Aufbau, zu einer geringeren Zuverlässigkeit führen.

Es konnte gezeigt werden, daß die folgenden Variablen hinreichend den Belastungszustand des Aufbaus charakterisieren und deutliche Auswirkungen auf die Zuverlässigkeit haben.

Aufgrund der sich ergebenden, deutlich abgestuften Rangfolge der einzelnen Konfigurationen läßt sich der Einfluss der einzelnen Variablen angeben: Den stärksten Einfluss auf die Lebensdauer hat die *Dicke der Leiterplatte*, wobei dicke Substate die Zuverlässigkeit reduzieren. Dies ist besonders kritisch in Kombination mit einer *Fixierung* der Leiterplatte auf dem Kühlkörper aufgrund der Differenz in den thermischen Ausdehnungskoeffizienten. Eine größere *Leiterplattenverschiebung* bewirkt eine stärkere Reduzierung der Lebensdauer. Auch negative Verschiebungen, welche eine konvexe Chipkrümmung verursachen, können realisiert werden, was sich auf die Zuverlässigkeit sogar günstig auswirkt. Bei der Wahl des *Wärmeleitmediums* schneiden die Folien geringfügig besser ab als die Kleber. Für Wärmeleitkleber ist eine spannungsarme Verbindung bei jeder Temperatur Voraussetzung für eine höhere Zuverlässigkeit. Die Größe einer *kompressiven Kraft*, zuständig für die Durchbiegung der Leiterplatte, zeigte hingegen keinen Einfluss.

Obwohl sich die einzelnen Konfigurationen bei tiefen Temperaturen je nach Belastung und Wärmeleitmedium stark im Deformationsverhalten des Chips unterscheiden, hat dies keinen großen Einfluss auf die Zuverlässigkeit. Chip und Bumps passen sich nach einer Übergangsphase den neuen Belastungen an. Der kritische Bereich für die Lebensdauer sind eine andauernde, erzwungene oder eingeschränkte Bewegungsfähigkeit des Chips bei hohen Temperaturen im Vergleich zum unbelasteten Chip.

Die aus dieser Arbeit resultieren Designregeln erlauben nun die technische Realisierung von Flip-Chip Aufbauten mit Rückseitenentwärmung bei maximierter Bump-Zuverlässigkeit. Die vorgestellte analytische und simulative Methodik kann leicht auf weitere Konfigurationen ausgedehnt oder auch auf verwandte Probleme im Packaging-Bereich angewandt werden, um deren Lösung zu vereinfachen.

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Chapter 1

Introduction

There is plenty of room at the bottom¹. Richard P. Feynman

And there still is. Indeed, the trend in electronic industry towards higher integration densities along with structural downsizing is unbroken. As unbroken as the visionary impact of Moore's law which predicts that the number of transistors per chip soars by a hundredfold roughly every decade [3,4]. And again there is much reason for a continuation of this trend [5] since the requirements of the next generation of products have always spun off new technologies and been a challenge for future research. Together with a high circuit density these requirements are nearly olympic: faster, smaller, lighter and above all, less expensive than today [6]. At the same time power and power density will also go up demanding effective heat dissipation and high performance thermal management even at elevated temperatures. This is for example the case in automotive applications, where electronic devices are to conquer the space close to the engine.

In this respect the packaging concept of flip-chip on organic board has been the focus of renewed interest over the last couple of years which seems to meet most of the described demands [7]: Due to its high pin count and the possibility for area-array layout renders it eligible for microprocessors or ASICs with smallest dimensions. Shortest possible signal paths reduce inductance and enhance signal processing. A big advantage is the compatibility with in-line SMT production equipment and the inexpensiveness of the organic substrate and the other materials in application. Then, the electrically inactive reverse side of the chip offers a unique opportunity: It may be used for most effective heat dissipation and represents therefore a promising basis for thermal management of flip-chip assemblies. As there is no insulating encapsulant that blocks the heat path a very direct thermal contact can be established if only a thermally conductive interface material is sandwiched between chip and heat-spreader. This is how flip-chip reverse side cooling came into being, an interesting concept which is gradually emerging as recent papers show [8–11]. Therefore this work is concerned with it.

¹This was the title of this famous talk [1] which he gave in 1957 on the potential of increasing the integration density in microelectronics by going down to the atomic scale. Remarkably, he made an allusion to the two years earlier published and celebrated novel 'Room at the top' by John Braine [2]. In this piece of literature the protagonist is invited to join the upper class of society by the words: 'There is plenty of room at the top.' As usual, Feynman presents himself visionary yet not quite modest.

However, as the above trends persist, thermo-mechanical reliability of microelectronic components – its analysis, assessment and prediction – becomes an issue of increasing importance [12,13]: Thermally induced deformations and stresses constitute the major contribution to an elevated failure rate and finite service life of modern integrated circuits as they cause damage to solder interconnects as well as materials and interfaces [13–19].

Flip-chip technology on organic boards has been made possible by the introduction of an underfill which translates the thermal shear strains into an overall bending of the assembly thus reducing greatly the deformation of the bumps which represent the critical point of the flip-chip assembly [20]. Still at some point during its service life the flip-chip assembly will eventually fail. In this respect solder bump fatigue cracking represents the main failure mode if no delamination at various decisive interfaces (e.g. chip-underfill) occurs, a different failure mode which considerably accelerates bump cracking by eliminating the beneficial effect of the underfill. The occurrence of failure, however, depends crucially on the combination of mechanical and adhesive properties of the employed materials as well as the environmental conditions the component is subjected to. These conditions manifest themselves in thermal and mechanical loads. In this respect also the flipped chip with attached heat-spreader will be liable to solder fatigue cracking or delamination as a function of material properties and loading.

For normal, mechanically unconstrained flip-chip assemblies is concerned, its reliability has been the object of longstanding research work (e.g. [13,21–33]). As far as the flip-chip assembly with attached heat-spreader is concerned, this experience and information is lacking: Some authors have addressed the excellent thermal performance of this concept [8] or emphasized the need for reliability assessment [9,10]. Others have carried out preliminary design studies by Finite Element simulations in conjunction with sporadic tests [11]. However, its thermo-mechanical reliability as a function of characteristic (but currently still unspecified) design variables is, although urgently needed, still largely unknown.

To remedy this, the comprehensive study presented in this work is necessary.

The ability to analyze, assess and predict – then possibly minimize the consequences of thermal stress is of obvious practical interest: The time to market as well as the cost for development are crucial ingredients for the competitiveness in industry and so it is of invaluable advantage to know the reliability of a product already at the design stage.

This need for lifetime assessment has sparked off much activity on the field of microelectronic packaging and stimulated a rapid and ever increasing application of advanced thermal and mechanical simulation methods and tools for the theoretical and practical treatment of thermo-mechanical reliability [34]. As for solder joint reliability assessment, Finite Element simulations coupled with thermal cycling tests of test-specimens have been used to analyze their average lifetime in order to make statements of general validity and to extrapolate the results to new designs and material combinations [35]. Thereby one draws upon the principle of inelastic phenomena causing the joints or bumps to accumulate damage before they finally crack. A (mostly) scalar, monotonically increasing failure variable is calculated and correlated to the mean of cycles to failure recorded in the experiment.

Some authors have used the amount of plastic deformation accumulated within one thermal cycle as failure criterion [36,37]. Others have simulated the creep strain [22,26,38,39] or dissipated energy [23] within the framework of thermally induced low cycle fatigue and

used a Coffin-Manson type of approach [40,41]. All do calibrate the bump as the reliability sensitive locus of the assembly to function as a 'reliability sensor' for given thermal loads and a specific solder material. This allows an analysis of influence and comparison of different load and material combinations with respect to solder joint reliability and permits subsequent lifetime prediction [26, 42, 43]. Alternatively some papers also suggest an approach based on fracture mechanical means [44–46]. Such a method, although in principle more universal, was not considered as crack analysis in solder materials requires not only sophisticated computational methods to allow for the physically correct evaluation of creep crack growth under periodic loading [47,48], but also experimental investigations concerning the temperature- and rate-dependent fracture toughness, both of which are beyond the scope of this work.

Under the given service conditions (high homologous temperatures) all inelastic deformation is essentially creep deformation. Creep induced damage represents the main failure mechanism of the bump in this regime which makes the creep strain-based approach especially suitable. Therefore it is preferred over the others and used in this work to describe low cycle fatigue of eutectic tin-lead solder bumps. Hereby the highly nonlinear and temperature-dependent response of the material is accurately taken into account.

With the introduction of reverse side cooling the flip-chip assembly is exposed to mechanical loads and boundary conditions [49] which do influence its lifetime. It is therefore the objective of this work to analyze, assess and predict the thermo-mechanical reliability of flip-chip on organic board as a function of the mechanical loads, which are induced by the attachment of a heat-spreader, under periodic thermal loading.

Different thermal interface materials (sandwiched for efficient heat transfer between chip and heat-spreader) may significantly alter the state of bending counteracting the beneficial effect of the underfill [11]. What geometrical and mechanical properties can therefore be derived for the best thermal interface material? What consequences do the fixations, deformations and forces the assembly is subjected to bring along for solder bump reliability? What part does the board's thickness and inner structure play in the assembly? Which are other influential factors determining the lifetime of a flip-chip assembly with heat-spreaders and what are resulting design rules to optimize this package concept with respect to thermo-mechanical reliability?

These are some of the interesting questions which are to be answered by this work. To do this, we draw upon a universal, parametric and modular concept of finite element model generation to handle the large required parameter variations. Thereby the model is automatically created by a combination of standard modules (e.g. the chip or the bump) according to previously specified parameters. In parallel performed thermal cycling tests are used to verify the simulatively obtained results for eutectic tin-lead solder bumps.

As flip-chip reverse side cooling represents a new concept, we start with a brief survey concerning the boundary conditions brought along with its technical realization.

Chapter 2

Flip-Chip Assemblies under Thermal and Mechanical Load: Motivation & Conception

As the technical realization of flip-chip reverse side cooling entails a new state of loading, a qualitative overview is given concerning the loads and boundary conditions the chip is subjected to and how it responds to them on a macroscopic level (chip) and how this might affect solder joint reliability (microscopic level).

2.1 Thermal Management of Flip-Chip Assemblies for Higher Power Applications

As the trend in the electronic industry to draw towards a higher packaging density is unbroken and the interest in higher power applications persists one faces the problem of ever increasing power dissipation in electronic circuits.

In the automotive sector this situation is aggravated by a decrease in headroom up to the maximally allowed junction temperature ($T_{max} = 125 \, ^{o}C$): Here demands of environmental temperatures as high as $T_{env} = 85 \, ^{o}C$ have to be met since electronic devices are to conquer the space close to the engine. So the question of high-performance thermal management of flip-chips that allows such a small temperature delta arises.

For an illustration of the requirements¹ of the thermal management for flip-chip assemblies let us take an average power dissipation of $P_T = 10~W$ which is the interesting order of magnitude for a power transistor module, an ambient temperature of $T_{env} = 85~^{o}C$ and a maximum temperature of $T_{max} = 125~^{o}C$.

This results in a temperature delta of $\Delta T = 40~K$ which can be used for heat transfer. This imposes that the system features a heat path with a total thermal resistance of

$$R_T = \frac{\Delta T}{P_T} \tag{2.1}$$

¹Specifications by Robert Bosch GmbH, Germany.

which has to be lower than $R_T = 4 K/W$. This condition will be the knock-out criterion for eligibility.

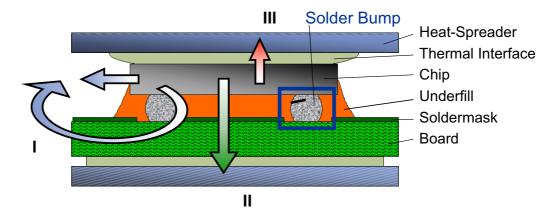


Figure 2.1. The three ways of cooling a flipped chip. The arrows are to indicate the heat path. From top to bottom the layers represent heat-spreader (casing), thermal interface (e.g. adhesive), chip, underfill, soldermask, board, (adhesive and casing again). These different ways of cooling entail new boundary conditions which may affect the reliability of solder bumps (blue frame). A beginning fatigue crack causing bump failure is indicated.

Some methods of cooling a flip-chip assembly are presented in the following. Their respective heat paths are illustrated in figure 2.1 and their thermal performance compiled in table 2.1. The values are taken from a computationally verified experimental study [50] carried out on a $20 \ mm^2$ chip.

• Cooling by Natural Convection:

This is the situation where no heat-spreader is attached in any way to the chip. This is the easiest way of cooling. The heat is spread by convection and radiation (smaller part in this temperature-range). Referring to the thermal resistance evaluated in table 2.1 below this way is by far not sufficient to rise up to our needs for larger power dissipation. It may be used for powers up to $P_T = 0.5 W$ under the given conditions. The reason for this is the low thermal conductivity of the organic substrate and underfill (lower by at least one order of magnitude with respect to thermal interface materials).

A reduction in thermal resistance may be achieved by enlarging the surface of the copper fan-out which can then act as a heat spreader, since the solder bumps function as heat conducting element in this extended heat path. Still R_T stays above of what is needed quite apart from the fact that this measure requires valuable space.

However, the thermal performance of methods relying on natural convection inside the housing is limited, as no direct thermal contact to the housing is provided. A heat-spreader inside the housing is not of much use unless there is some additional ventilation or fan.

• Cooling Through the Board:

This is the time-honoured way of cooling a flip-chip for situations where higher power is needed. Here, thermal vias are used to transfer the heat through the board to the heat-spreader, i.e. the housing, on which the board has to be glued to establish thermal contact. But as can be seen again from table 2.1 it still does not fulfill our expectations. The thermal resistance of the heat path is still too large even if the thermal connection to the heat spreader is improved by thermal vias within the board [50]. This is due to the low thermal conductivity of the intermediate layers (particularly the organic board) and the limited number of (thermal) bumps especially for smaller chips.

• Cooling via the Reverse Side:

In this case the – electrically inactive – reverse side of the flip-chip is used for heat transfer to a heat spreader which should for thermal and practical reasons be a part of the housing of the device. Silicon has a comparatively large thermal conductivity $\lambda_T = 149 \, W/mK$ which assures low thermal resistance by the die itself. In order to assure perfect thermal contact an interface material (gap filler or adhesive) is put between the chip and the heat spreader.

Flip Chip Cooling Possibilities

Method and Heat Path	#	$R_T [K/W]$
$\overline{FC} \to Convection \to Housing$	I	> 70
FC Front Side \rightarrow Board + Thermal Vias \rightarrow Housing	II	> 10
FC Reverse Side \rightarrow Thermal Interface \rightarrow Housing	III	< 4

Table 2.1. Thermal performance of the three presented methods for cooling a flip-chip assembly. These values are obtained by experimental test using a chip of area $A_{chip} = 20 \text{ mm}^2$ and were verified computationally [50].

Of these three methods only the last one – flip-chip reverse side cooling – is eligible for high power applications due to its outstandingly low thermal resistance. Ways have to be found to facilitate an attachment of the reverse side of the flip-chip to an heat spreader assuring optimum permanent thermal contact, but also maximum thermo-mechanical reliability. The thermal performance of the methods presented in the following has very recently been evaluated by [8] and was found to be exceptional. Thermo-mechanical reliability will be in the focal point of this work.

2.1.1 Maximum Thermal Performance: Flip-Chip Reverse Side Cooling

Working on what has been stated in the last paragraph, we want to look on the flip-chip reverse side cooling (FC&RSC) in more detail. The principle behind is again depicted in

figure 2.2. In order to realise the required low thermal resistance technologically one has to look for the shortest heat path and combine good thermal contact at the surfaces with thermal interface materials which display a high thermal conductivity. So we go back to equation 2.1 and rewrite it for insertion of material properties (refer to A.2):

$$R_T = \frac{\Delta T}{P_T} = \frac{1}{\lambda_T} \frac{b}{A_T} \quad , \tag{2.2}$$

where b is the thickness of the thermal interface layer, λ_T its thermal conductivity and A_T the effective or thermally active surface. The latter has been introduced to point out that there might be 'hot spots' on the chip (areas which mainly dissipate heat, e.g. a power transistor) and would thus reduce the active surface. Therefore in general $A_T < A_{chip}$ should be assumed², at least this point should be considered when it comes to making the layout for a specific cooling set-up. (For the following considerations we have set $A_T = \frac{1}{5}A_{chip}$, which corresponds to the assumptions in [50].)

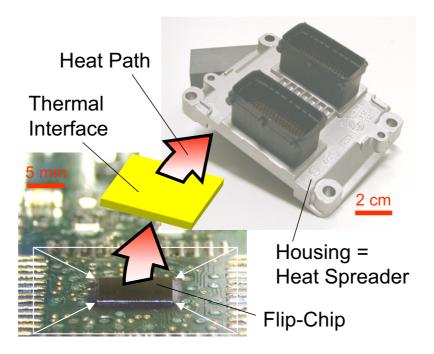


Figure 2.2. Principle of flip-chip reverse side cooling: The heat path is symbolized by arrows as it starts at the flip-chip via a thermal interface medium (gap filler or adhesive) before it is spread by the housing itself which serves as a heat-sink. The pads around the chip (white square) demonstrate the area reduction due to flip-chip mounted devices with respect to electrically equivalent but encapsulated components (e.g. QFP).

Taking into account our upper limit of $R_T = 4 \text{ K/W}$ (the housing itself is assumed to be an ideal heat spreader), one may realize reverse side cooling using interface materials which are commercially available. Thereby, the maximum thickness of the gap is obviously

²It has indeed been shown by thermal simulation [50] that one may severely underestimate the thermal resistance in such a case. Still the latter depends greatly on λ_T which, when chosen large enough, will in return result in a more uniform temperature distribution over the chip.

dependent on the thermal conductivity of the material. Some representative examples are given in table 2.2. These are also the materials we carry out our studies on in this work. Therefore, a code letter for future reference is introduced already at this point.

Other criteria for the eligibility³ of the materials were on one hand applicability and compatibility with production line assembly processes, availability on the market and possibly an already existing long-term experience with the material. On the other hand they should be representative examples of their group of materials in order to yield results which may be extrapolated to similar materials. For a computational treatment they must be characterisable in their physical properties for Finite Element implementation.

Thermal Properties of Interface Materials

Thermal Interface Material	Code	$\lambda_T [W/mK]$	Gap $b [\mu m]$
Epoxy-Silicone Adhesive with Silver Flakes	Ε	4.0	320
Silicone Adhesive with Aluminium Oxide Particles	S	0.9	72
Carbon Foil	\mathbf{C}	$7.0 \bot 140.0$	560
Gap filler, Silicone with Boron Nitride Particles	\mathbf{F}	5.0	400

Table 2.2. Examples of typical high performance materials eligible for cooling a flip-chip assembly. The values are taken from the respective data sheets. $A_T = 20 \text{ mm}^2$ is used for evaluating the maximum gap for the thermal interface layer. The code letter is introduced for easy reference throughout this work. The carbon foil displays an anisotropy in the thermal conductivity.

The given materials do meet all these prerequisites. They are commercially available interface materials and were tested in their thermal performance for flip-chip reverse side cooling by [8]. They feature the following properties and can be divided into:

• Gap fillers

Gap fillers (flexible mats or foils) which are usually made of elastomeric binder (e.g. silicone moulding resin) in compound with a ceramic filler. Generally the matrix material is reinforced by some sort of fibre-tissue. Filler particles employed are aluminium oxide as well as boron nitride for their high thermal conductivity $\lambda_T = 1...5 \ W/mK$ (data sheets). Various thicknesses are available, usually in multiples of 250 μm .

An other material apt for this purpose is carbon foil which displays a very high thermal (orthotropic) conductivity (see table 2.2). This material has a wax coating to assure perfect gap closure and thermal contact.

The pros and cons of gap fillers are the fact that no additional curing process is needed. But on the other hand they require special handling and are not inexpensive.

The thermal conductivity is in general a function of the applied pressure on the medium. Hereby, a minimum pressure for reliable thermal contact is usually specified

³Specifications by Robert Bosch GmbH, Germany.

by the manufacturer and lies around $p_N = 0.1 MPa$ for high performance materials. This pressure is needed to make the material conform to surface irregularities eliminating air gaps.

• Thermal adhesives

Thermal adhesives are based on silicone, epoxy or co-polymeric matrix material and use besides the above mentioned filler materials also silver flakes as good thermal conductor. Thermal conductivities are comparable to those reached by gap fillers.

Their advantage is easy application by dispensing. The disadvantage is an additional curing process which may interfere with the remaining assembly of the device. The surfaces may need an extra (chemical) treatment to promote adhesion. An applied pressure is not needed as the adhesive fills potential cavities during dispensing.

2.1.2 New Boundary Conditions Through Reverse Side Cooling

Flip-chip reverse side cooling is the only promising way for high power applications, relying on standard SMT processes. Yet it brings along new, system-inherent boundary conditions.

For reasons of reliable heat dissipation (thermal reliability) it is essential that the maximum gap width once determined is never exceeded despite all other tolerances there might be. This fundamental requirement entails the consequence, that the gap is to be kept close and its width to be held constant. This can only be ensured by applying a pressure to the thermal interface.

On imagining the situation in a electronic device one is faced with material imperfections and manufacturing tolerances which are, although specified, to be compensated for. As a rough guide to the magnitude in question serves the following contemplation: Typical tolerances to be taken into account are due to the die itself ($\pm 10~\mu m$), the contact (or bump) height ($\pm 20~\mu m$) and the housing ($\pm 200~\mu m$), yielding in sum an overall tolerance of ($\pm 230~\mu m$) to make up for.

We want to tackle this problem by bending the board from below by applying a pressure on a point just below the chip to obtain a displacement which moves the chip so close to the housing that the specification for the gap is met. This situation is depicted in figure 2.3.

For the case of a gap filler (non-adhesive) this means that this pressure has to ensure permanent closure of the gap during operation, at the same time keeping up the minimum force needed to compress the interface material.

This force, in conjunction with geometric boundary conditions such as a local fixation of the board or a neighbouring component of great stiffness, will subject the flip-chip assembly to deformation and thus induce an alteration in the state of stress and strain as a function of temperature.

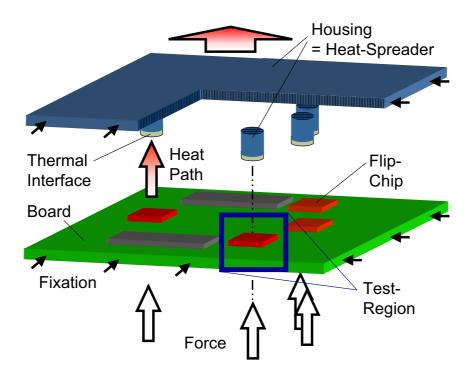


Figure 2.3. Schematic of flip-chip reverse side cooling ('exploded' view). Each flip-chip is pressed against the housing from below the board (black arrows). Thermal contact of the chips' reverse side (see red arrows for heat path) can be established to parts of the housing which are shaped to reach down to the site of the chip and are tipped with a thermally conductive interface material. The board is fixed at its edges.

2.2 Thermo-Mechanical Reliability Issues of Flip-Chip Reverse Side Cooling

It is expected that these mechanical loads applied to the flip-chip assembly to facilitate reverse side cooling do have an influence on its thermo-mechanical reliability with respect to solder bump failure.

For this reason it will be the task of this work to examine the reliability of the chip under these novel boundary conditions.

As an approach we want to shed some light on the characteristic qualitative behaviour of the flip-chip assembly which gives rise to interesting guiding questions and consequences which will have to be taken into account in the course of this work.

2.2.1 Model Assumptions and Qualitative Considerations

As seen from figure 2.3 we deal with a very complex set-up indeed. But for reasons of universality of the conclusions we seek concerning flip-chip reliability it is not advisable to put the whole of such a device to a test, quite apart from the fact that it is beyond

our means to carry out a corresponding finite element simulation with today's computers. So we want to see what constraints are active at the local site of the flip-chip (blue frame in the quoted figure labelled 'test-region'), extract the characteristic variables suitable to describe its behaviour and to condense this situation into a model where the boundary conditions or loads can be applied and controlled.

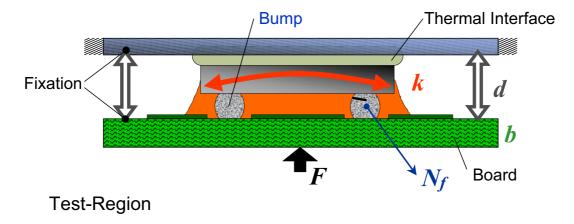


Figure 2.4. Schematic of test-region for reliability study as stated in figure 2.3. From there typical loads and boundary conditions must be extracted and controllably applied to the chip. Depicted is the force F and the displacement d (with fixation) which may cause, in conjunction with the properties of the thermal interface and the board thickness b, a change in the deflection k of the constrained chip and hence influence the reliability N_f (cycles to failure) of the solder bump.

A set-up well-suited for this purpose is sketched in figure 2.4. An adjustable displacement d allows to mimic the gap caused by the manufacturing tolerances and a force F bridges it by bending the assembly. A rigid or sliding joint (fixation) between plate and board (at the point of the arrows) can also be considered to mimic the boundary conditions of the real casing.

The chip, although attached or pressed to an adhesive or gap filler, may alter its state of bending together with the curvature of the whole assembly. A suitable parameter to describe this response is a curvature or deflection k of the silicon die. This macroscopic response may in return have an influence on solder bump reliability which is given by N_f , the (mean) number of cycles to failure.

2.2.2 Potential Influence on Thermo-Mechanical Reliability

The whole of flip-chip technology on organic board relies on the function of the underfill, which stiffens the assembly to a degree where it is able to translates the thermally induced shear strains in the underfill and soldermask into an overall bending of the assembly. These strains are caused by the mismatch in the CTEs of chip and board as a function of temperature. Chip and board are the materials which govern this behaviour. So already at room temperature the chip is in a state of thermally-induced curvature.

It has been shown [20,51] that flip-chip on organic board is not viable without underfill. For instance, this problem of severe global mismatch does not arise for ceramic substrates which have a CTE similar to silicon.

So the state of bending is beneficial for the flip-chip assembly and its degree of bending, its curvature, seems to have a correlation to the lifetime of the bumps as this has repercussions on the strains the bump will have to comply to [52]. To illustrate this: If no underfill is used the assembly does not bend under thermal load and the shear strains thus induced do cause the bumps to fail during a few thermal cycles [53].

Since the ability to curve seems the assembly's decisive macroscopic behaviour the question arises if and to what degree bump reliability may be influenced if this curvature is altered or constrained by mechanical loads, i.e. an externally applied force. The initial, thermally induced curvature may be superposed by a mechanical one. In addition to this, the boundary conditions or fixation may change this response.

Moreover, different kinds of thermal interface materials represent different kinds of constraint to the chip and may entail various types and degrees of bending as a function of temperature.

We may ask further if the reliability may even be enhanced by a particular type of bending. If the intrinsic concave bending of the flip-chip assembly is vital for its thermo-mechanical reliability, a further (mechanical) drive promoting this tendency could prolong bump lifetime. Or what is the effect of convex bending which counteracts the intrinsic mode of bending but could also be a viable technological variant?

For a coupled numerical and experimental approach as we envisage it here the following topics have to be covered:

- The materials of interest for this assembly have to be characterized concerning their material properties and made available for Finite Element (FE) input.
- An appropriate failure criterion is to be implemented.
- A FE model is to be created and calibrated to design, simulate and optimize a testspecimen for numerical evaluation of solder bump reliability.
- The test-specimen has to be constructed and built to undergo a thermal cycling test for experimental verification of solder bump reliability.

These are key issues for this work. They will be treated quantitatively in the next chapters.

Chapter 3

Material's Characterization, Constitutive Theories, Failure Mechanisms and Lifetime Prediction

In this chapter we determine the mechanical properties of the materials that make up the flip-chip assembly with reverse side cooling (see table 3.1) for subsequent Finite Element implementation. These materials belong to different groups (polymers, alloys, metals, compound materials) and display, apart form linear elastic material behaviour also non-linearities and a high temperature- and rate-dependence (elasto-plasticity, viscoelasticity and viscoplasticity).

We begin with eutectic tin-lead solder and describe its mechanical behaviour and failure mechanism based on the assumptions of low cycle fatigue (due to large, periodic inelastic deformation, here: induced by thermal mismatch) at high homologous temperatures. In this regime creep represents the main failure mechanism of the bump and is evaluated as failure criterion used for lifetime prediction. As the solder bump constitutes the reliability-sensitive part of the flip-chip assembly, the correct representation by a viscoplastic law is of crucial importance: Here we draw upon data from literature [26,43] of strong experimental support. The respective constitutive equations are discussed and numerically implemented. Finally, the theoretical framework of lifetime prediction within the Coffin-Manson approach is motivated and demonstrated.

The second class of important materials comprises polymers. Underfill, thermal adhesives, organic board do fall among this rubric. They are characterised with respect to their viscoelastic properties and the recorded data is subsequently implemented via the respective constitutive laws. Various measurement techniques are employed to accurately characterise these materials in the time and temperature domain. These comprise dynamic mechanical analysis (DMA), thermo-mechanical analysis (TMA), rheometric measurements, tension and relaxation testing [54].

For the (elastic) characterization of the gap-fillers one has to resort to another experimental method. Fortunately, material data was provided by the manufacturer, the elastic modulus could be measured in compression.

As far as elasto-plastic material data of metals is concerned we did rely on values taken from literature on the subject [55].

For the solder and polymers used here it is shown how the material data is made available for the numerical simulations. In the course of this process the material laws or constitutive equations were implemented as user-programmable features as *Fortran* subroutines and linked to the respective simulation tool. This procedure was necessary since the required material laws were not available as standard function. The employed algorithms fit the experimental data very well in Ansys and Abaqus, which were the FE-tools¹ in use. For standard material routines we refer to the respective theory manuals for details [56], [57].

To assure readability of this chapter we proceed as follows: Measured data is given as *Ansys* input format. This tabular form and nomenclature is explained the first time it appears for a specific group of materials. Eutectic solder, underfill and gap-filler data is given at the end of the respective section, whereas all remaining measured data can be found in the appendix B as also listed in table 3.1.

Table	Ωf	Emn	lowed	NIst	oriale
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Material	Behaviour	Constitutive Law	Application	Section
Eutectic SnPb Solder	vp	Secondary Creep	Bump	3.1
Filled Epoxy Resin	ve	Temperature-time shift	Underfill	3.2
Fibre-Epoxy Resin	ve	Temperature-time shift	Board	B.2
Epoxy Resin	ve	Temperature-time shift	Soldermask	B.3
Epoxy-Silicone	ve	Temperature-time shift	Adhesive	B.4
Steel	el-pl	BISO	Fixations	B.6
Copper	el-pl	BISO	Traces	B.6
Aluminium	el-pl	BISO	Plate	B.6
Nickel	el-pl	BISO	UBM	B.6
Silicon	el	Linear	Chip	B.6
Silicone	el	Linear	Adhesive	B.5
Carbon	el	Linear	Gap filler	3.3
Flex-Foil	el	Linear	Gap filler	3.3

Table 3.1. The abbreviations stand for: el-elastic, pl-plastic, vp-viscoplastic, ve-viscoelastic, BISO-bilinear isotropic hardening. The last column references the section where the material data (specified for Ansys input) can be found.

The testing conditions of thermal cycling comprise a temperature interval of $T \in [-40; 125]$ °C, but simulation requires the knowledge of material behaviour up to the highest temperature encountered in the assembly process, which is the curing temperature $T'_c = 160$ °C of underfill and thermal adhesive. Therefore the materials had to be characterised within a temperature range of $T \in [-40; 160]$ °C.

¹Ansys, Release 5.7 and Abaqus, Release 5.8.

3.1 Viscoplastic Creep and Failure of Eutectic Tin-Lead Solder

Viscoplasticity means, that a material starts to flow from a certain stress level on and deforms irreversibly over time as a function of stress and temperature. The material is also said to creep for a constant stress experiment. Viscoplasticity is a relevant factor only at high homologous temperatures, i.e. for T > 1/2 T_m , where T_m is the melting temperature on an absolute temperature scale. As eutectic tin-lead solder melts at $T_m = 456$ K, it is justified to assume creep as governing mechanism for the deformation behaviour even at the bottom end of our temperature interval of interest (T > 233 K).

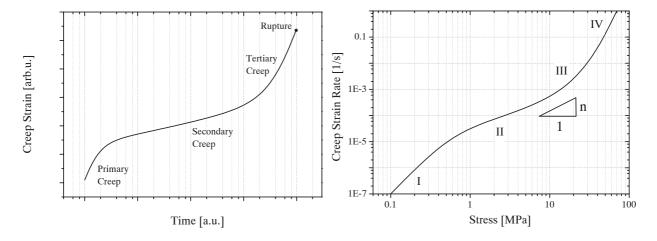


Figure 3.1. Left: Creep types typical for alloys at high homologous temperatures. Right: The stress dependence of the steady-state creep rate for eutectic tin-lead solder can be divided into four regions [43]. The slope of the graph corresponds to the stress exponent n.

A typical creep curve as depicted in figure 3.1 shows the essential features. Three regimes of the creep process may be distinguished [58]:

- Primary creep: Under constant load the material undergoes first a transient phase of creep. It is a dominant part for low homologous temperatures.
- Secondary or steady-state creep: The creep strain rate and microstructure is constant over time in this regime.
- Tertiary creep: This regime precedes fatal failure of the material due to rupture.

For small strains we can assume an additive decomposition of strain:

$$\varepsilon_{ij}(t) = \varepsilon_{ij}^{el}(t) + \varepsilon_{ij}^{pl}(t) + \varepsilon_{ij}^{cr}(t) + \varepsilon_{ij}^{T}(t)\delta_{ij}, \tag{3.1}$$

where the total strain tensor is composed of an elastic, a (rate-independent) plastic, a creep contribution and the thermal strain. The Kronecker-delta reflects the fact that

thermal strains have no shear components. Under the given environmental (and hence testing) conditions the elastic² and time-independent plastic part may be neglected³: This is justified due to slowly varying loading or drive (as given for low cycle fatigue and service conditions on the automotive sector [15]). For the same reason we can assume that we only deal with steady-state creep for eutectic solder under the envisaged testing conditions. Primary – or transient – creep may be neglected and the high stress regime is not touched either. It may be assumed that the deformations are, to a good approximation, completely converted into steady-state creep strain [60]. As can be inferred from figure 3.1 (right) no yield criterion exists as in conventional plasticity, the material starts to creep as soon as there is a minor force.

3.1.1 Material Behaviour and Constitutive Equations

The steady state creep regime which is reached when the material has passed through a phase of transient creep is characterised by a constant creep rate:

$$\dot{\varepsilon}_{ij}(t) = \text{const. or } d_t^2 \varepsilon_{ij}(t) = 0.$$
 (3.2)

The steady-state creep rate $\dot{\varepsilon}_{ij}(t)$ is a strong and highly nonlinear function of stress and temperature and displays furthermore a dependence on microstructure χ , i.e. phase size [44,60]. It is, to a first order approximation, assumed not to depend on time [15,43]. This involves necessarily a dynamic stability in $\dot{\varepsilon}$ and χ . Therefore one may write:

$$\dot{\varepsilon}_{ij} = \dot{\varepsilon}_{ij}(\sigma_{ij}, T, \chi), \tag{3.3}$$

where σ_{ij} and χ denote the stress-tensor and the microstructure respectively. In general, the microstructure will be itself a function of the load-history and the creep rate, i.e. there is an interdependence which would eventually entail a self-consistent relationship for evaluation.

$$\chi = \chi(\dot{\varepsilon}_{ij}, \varepsilon_{ij}, \sigma_{ij}, T, \chi_0), \tag{3.4}$$

Since we do not intend to evaluate the creep strain self-consistently, we merely assume that the effect of χ can be sufficiently described by the phase size d which is then introduced as a structural parameter characteristic for a specific microstructure. This will have to manifest itself in the respective constitutive equations which have to consider phenomenology and physical mechanisms.

Steady state creep can be divided into four different creep phases as a function of stress which are determined each by a different creep mechanism as seen in figure 3.1 to the right after [43]. All of these mechanisms are assumed to be diffusion controlled due to high homologous temperatures. Therefore the shear creep strain rate $\dot{\varepsilon}_{xy}$ can be expressed by a Weertman-Dorn's type of equation as a function of shear stress σ_{xy} :

$$\dot{\varepsilon}_{xy} \sim \frac{GbD}{kT} \left(\frac{\sigma_{xy}}{G}\right)^n \left(\frac{b}{d}\right)^p,$$
(3.5)

²still for FE-input the Elastic modulus need to be measured. This is accomplished with a high-frequency method or by determining the sound-velocity in the material according to $c_s \sim \sqrt{E}$ [59].

³It may be argue that the decomposition into plastic and creep strain is artificial anyway. All plastic deformation is essentially time-dependent, but this dependence is a strong function of temperature which overcomes the activation energy of rate-dependent mechanisms [43].

where G is the shear modulus, b the absolute value of the Burger's vector describing the magnitude of the dislocation orthogonal to a slip-plane and $D = D_0 e^{-Q/kT}$ is the temperature-dependent diffusion coefficient for the creep mechanism in question, Q the activation energy for the respective thermally activated diffusion process or mechanism that is rate-controlling, k is Boltzmann's constant. Further, n denotes the stress exponent and p the grain size exponent, d – originally the grain size – is here to be understood as interphase spacing according to [43].

These four regions can then be distinguished by different mechanisms, which means stress exponents, activation energies and microstructural parameters. Hereby the first (I) and second (II) are based on grain boundary sliding (superplastic deformation at the phase boundaries) whereas the third (III) features matrix power-law creep (plastic deformation within the phases) and region (IV) is characterised by a breakdown of the power-law and could be based on mechanisms like obstacle-controlled glide.

It has been proposed [61], that for eutectic tin-lead solder the creep strain can be described by two, separately but additively acting mechanisms in the stress domain of interest in electronic packaging for automotive applications:

$$\dot{\varepsilon} = \dot{\varepsilon}_{II} + \dot{\varepsilon}_{III}. \tag{3.6}$$

Hereby region (II) is dominated by grain boundary sliding and features a dependence on microstructure (here characterised by the interphase spacing d), whereas region (III) proves independent of d. The following constitutive equation is thus formulated, which is based on strong experimental support by thermo-mechanically driven shear tests carried out on eutectic solder bumps [43]. It was verified e.g. in tension tests on bulk specimens [26] and for flip-chip bumps [42] using micro-deformation analysis by gray-scale correlation [24,62,63] in combination with FE-analysis. So it can be assured that the measured creep strain in a bump can indeed be accurately described by this equation. In uniaxial form

$$\dot{\bar{\varepsilon}} = \frac{1}{\sqrt{3}} \frac{A_{II}}{T} \frac{1}{d^p} \left(\frac{\bar{\sigma}}{\sqrt{3}}\right)^{n_{II}} \exp\left\{-\frac{Q_{II}}{kT}\right\} + \frac{1}{\sqrt{3}} \frac{A_{III}}{T} \left(\frac{\bar{\sigma}}{\sqrt{3}}\right)^{n_{III}} \exp\left\{-\frac{Q_{III}}{kT}\right\}. \tag{3.7}$$

The constants assume the following values after [43] and are compiled in table 3.2.

It should be noted that this equation was originally derived from a fit to experimental data recorded in shear. For conversion to applicability to tensile (uniaxial) data shear stress and shear strain have to be replaced by the corresponding equivalent entities $\bar{\sigma}$ and $\bar{\varepsilon}$. This is a straightforward calculation⁵ and produces

$$\bar{\varepsilon} = \frac{2}{\sqrt{3}} \varepsilon_{xy}$$
 and $\bar{\sigma} = \sqrt{3} \sigma_{xy}$. (3.8)

In figure 3.2 the simulated creep strain rate is plotted versus the stress in equivalent entities. Obvious is the extreme nonlinear temperature and stress dependence over many orders of magnitude. For a correlation to the measured data see [26].

What enters here is the influence of the phase size which should only influence grain boundary sliding. It was found [43] that when the average phase size in the solder bump

 $^{^4}MicroDAC^{TM}$

⁵Use equations 3.13 and 3.11 taking $\nu = 0.5$

was considered the postulated relationship (3.5) could indeed be verified although d does not represent a mechanistically correct grain size, but is surely a measure – as long as it is meaningfully measurable – of solder coarsening. Coarsening in solder alloys occurs during thermal and mechanical processes towards an energetically more favourable state of minimised overall surface of the phases [64], since as-cast solder is not in a state of equilibrium. A coarser microstructure favours deformation due to matrix creep rather than through grain boundary sliding. So as coarsening proceeds, matrix creep will become more and more dominating. As a result of this, the creep rate goes down for given values of stress and temperature, the solder hardens.

Parameters for Creep Law

Parameter	Meaning	Value
$\overline{A_{II}}$	Fit constant	$1.39 \cdot 10^{-6}$
A_{III}	Fit constant	$2.38\cdot 10^3$
n_{II}	Stress exponent Grain Boundary Sliding	1.96
$n_{I\!I\!I}$	Stress exponent Matrix Creep	7.10
Q_{II}	Activation Energy Grain Boundary Sliding	0.50~eV
Q_{III}	Activation Energy Matrix Creep	0.84~eV
k	Boltzmann's constant	$8.61 \ 10^{-5} \ eV/K$
d	Phase size	$2.4~\mu m$
p	Phase size exponent	1.8

Table 3.2. The corresponding elastic properties are given in section 3.1.2 as Ansys input file.

As has already been mentioned, the microstructure is itself a function of temperature and creep strain (rate) in a self-consistent relationship. Therefore the grain size of a stable and periodic cycle depends on the cycle itself, that is T(t) being ramped up and down and held constant in between. The coarser initial phase size of $d=2.4~\mu m$ was achieved for a cycle close to the one used in this work. Therefore this value of phase size will be chosen as stable value for the phase size. This value is larger than for 'as cast' solder $d\approx 1\mu m$ [60], but microstructure is extremely sensitive to cooling and solidification conditions [44] quite apart from the fact that it is not homogeneous [60], off-eutectic [65] close to intermetallics due to depletion, different from bump to bump [64] and difficult to measure as coarsening goes on. So discrepancies concerning measurement results [38, 66] might be due to the strong dependence of creep on the microstructure [15].

Due to these difficulties d is usually taken constant and characteristic for a steady-state creep phase. Then equations (cf. $\dot{\varepsilon}(d) \leftrightarrow d(\dot{\varepsilon})$) 3.3 and 3.4 need not be solved self-consistently. Still, work in this direction is being done but not at a stage where it would furnish conclusive results ([67] take into account a gradual change in creep mechanism $(II) \rightarrow (III)$ with the numbers of cycles).

When the constitutive equation is implemented in an FE-tool and a tension test is simulated for a consistency check, typical stress-strain curves are obtained as in figure 3.3. This type of more familiar graphical representation shows that the creep law is indeed correctly

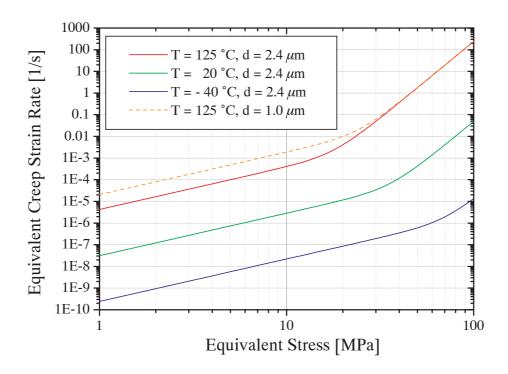


Figure 3.2. Constitutive behaviour of eutectic tin-lead solder according to equation 3.7, [43]. A smaller phase size (dashed line) favours region (II) creep (grain boundary sliding) at low stresses. The result would be a higher creep rate.

implemented as the values of stress are reproduced in accordance with those of figure 3.2 for a given value of T and $\dot{\varepsilon}^{cr}$.

Sometimes constitutive equations for solder are proposed which use a hyperbolic sine dependence on stress for the creep strain rate [68,69] according to:

$$\dot{\bar{\varepsilon}} \sim \frac{1}{T} \left(\sinh\left(\frac{\bar{\sigma}}{c}\right) \right)^n \exp\left(-\frac{Q}{kT}\right).$$
 (3.9)

A law of this type does hence not reflect the physical effect of grain boundary sliding in the sense of a constitutive equation⁶ (as n is not a stress exponent in the actual sense of the term) and may therefore underestimate this contribution for small (thus effective or averaged) phase sizes. It is not considered any further in this work for this reason.

In general lifetime prediction is extremely sensitive to correct representation of the material's response by a creep law. In this respect especially the determination of the correct stress exponent is very demanding [70], whereas there is less argument about activation energies of the corresponding diffusion processes.

3.1.2 Numerical Implementation of Creep

For both FE-tools (Ansys and Abaqus) the use of the presented creep law signified a non-standard use and required an extra compilation, linking and testing procedure of a Fortran

⁶Based on the constitution of a material and the physical processes which determine its response.

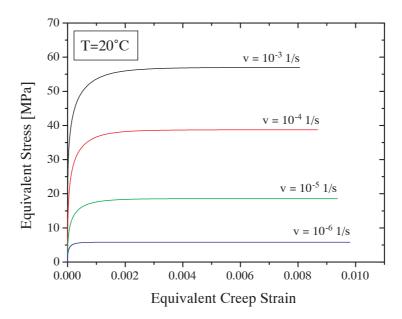


Figure 3.3. Test: Familiar stress-strain curves for eutectic tin-lead solder as calculated by an Ansys-implemented Fortran subroutine for a solder-bar in tension, i.e. $\bar{\varepsilon} = \varepsilon_{zz}$ and $v \equiv \dot{\varepsilon}_{zz}^{tot}$.

subroutine. It is instructive to see how creep is treated numerically:

Numerical implementation of the constitutive equation given in the last section follows an incremental flow rule scheme [56,57]. Therefore, the equations need to be transformed for equivalent entities first. This enables a simple description of a complex 3D stress state, not just the well-defined (shear-) stress and strain set up in the experiment. Here, the von Mises equivalent stress (and strain) is used: It is well suited for the description of plastic deformation as it characterises the deviation from the hydrostatic state which does involve hardly any plasticity. As it is evaluated based on the second invariant of the deviatoric part of the respective tensor it does not depend on the coordinate system. The directional dependence of the creep strain is subsequently added as the material is assumed to flow into the direction of the strongest gradient.

The equivalent stress is defined by (see e.g. [58,71]):

$$\bar{\sigma} = \left(\frac{3}{2}s_{ij}s_{ij}\right)^{\frac{1}{2}}$$

$$= \frac{1}{\sqrt{2}}\left((\sigma_{xx} - \sigma_{yy})^2 + (\sigma_{yy} - \sigma_{zz})^2 + (\sigma_{xx} - \sigma_{zz})^2 + 6(\sigma_{xy}^2 + \sigma_{yz}^2 + \sigma_{xz}^2)\right)^{\frac{1}{2}},$$
(3.10)

where the inner product extends over s_{ij} , the stress deviator given by

$$s_{ij} = \sigma_{ij} - \frac{1}{3}\sigma_{kk}\delta_{ij},\tag{3.11}$$

where the Kroneker-delta and Einstein's convention (A.1) has been used.

Analogously an equivalent strain can be defined:

$$\bar{\varepsilon} = \frac{3}{2} \frac{1}{1+\nu} \left(\frac{2}{3} e_{ij} e_{ij} \right)^{\frac{1}{2}}$$

$$= \frac{\sqrt{2}}{2(1+\nu)} \left((\varepsilon_{xx} - \varepsilon_{yy})^2 + (\varepsilon_{yy} - \varepsilon_{zz})^2 + (\varepsilon_{xx} - \varepsilon_{zz})^2 + 6(\varepsilon_{xy}^2 + \varepsilon_{yz}^2 + \varepsilon_{xz}^2) \right)^{\frac{1}{2}}.$$

$$(3.12)$$

Here again e_{ij} is the strain-deviator calculated in the same vein as in equation 3.11, only that ε_{ij} takes the place of σ_{ij} . The mean volumetric strain is hereby $e_m = \frac{1}{3}\varepsilon_{kk}$. ν is Poisson's ratio, which for creep strain evaluation is usually set equal to $\nu = 0.5$ as creep is assumed to be volume-preserving, i.e. incompressible [58].

A Fortran subroutine calculates now the equivalent creep strain increment (time step)

$$\Delta \bar{\varepsilon}_k^{cr} = \int_{t_k}^{t_{k+1}} dt \, \dot{\varepsilon}^{cr} = \dot{\varepsilon}^{cr}(\bar{\sigma}, T, \chi) \Delta t_k \tag{3.13}$$

and its derivative with respect to stress (for extrapolation for the next time step) for every integration point according to a implicit time-integration scheme (unconditionally stable backward Euler method). (This routine is essentially the same in *Ansys* or *Abaqus* and contains the formulae in their formulation for equivalent entities.)

As already mentioned, the directional material flow follows the gradient n_{ij} of the von Mises stress potential $q(\sigma_{ij}) = \bar{\sigma}$ (can be thought of as a surface in 3D stress space):

$$\Delta \varepsilon_{ij}^{cr} = \Delta \bar{\varepsilon}^{cr} n_{ij} \quad \text{where} \quad n_{ij} = \frac{\partial q}{\partial \sigma_{ij}} = \frac{3}{2} \frac{1}{q} s_{ij}$$
 (3.14)

So for the creep strain increment in three dimensions we obtain:

$$\Delta \varepsilon_{ij}^{cr} = \frac{3}{2} \frac{\Delta \bar{\varepsilon}^{cr}}{\bar{\sigma}} s_{ij} \tag{3.15}$$

The stress state is in return defined by Hooke's law based on the fact that only elastic strains give rise to stress at time t_{k+1} :

$$\sigma_{ij}|_{t_{k+1}} = D_{ijmn} \left(\varepsilon_{mn}|_{t_{k+1}} - \varepsilon_{mn}^T \delta_{mn}|_{t_{k+1}} - \varepsilon_{mn}^{cr}|_{t_k} - \Delta \varepsilon_{mn}^{cr}|_{t_k} \right), \tag{3.16}$$

where D_{ijmn} is the elasticity tensor and use has been made of equation 3.1.

Finally the sum over the individual increments yields the total accumulated creep strain:

$$\bar{\varepsilon}^{cr} = \sum_{k} \Delta \bar{\varepsilon}_{k}^{cr} \tag{3.17}$$

This summation is carried out already within the subroutine. *Ansys* leaves so-called state-variables for the user to specify. The accumulated equivalent creep strain is as an always positive quantity put out by either a state variable. *Abaqus* has this feature already implemented.

This routine was compiled for both *Abaqus* and *Ansys* and produced identical results for various test cases, only dependent on the used time stepping scheme i.e. creep limit control (cf. section 4.2). The creep laws were tested for a beam under constant load in tension and in shear and for a flip-chip bump (results are depicted in the appendix section C.1.1). The Ansys input data file comprising elastic and inelastic properties is given below.

How this creep strain can be used for lifetime evaluation is the subject of the next sections.

3.1.3 Ansys Data File for 63Sn37Pb Solder

In the input file given below first the elastic properties are given in tabular form as a function of temperature where intermediate values are interpolated linearly.

In the second half of the code file the creep routine usercreep.F⁷ [72] is addressed and the parameters defining the creep law as given in table 3.2 are transferred to the subroutine. A state variable sums up the creep strain increments and makes them available to the program's post-processor either by etable,svar,4 or by etable,nl,psv. Summing up the output equivalent creep strain by etable,epcr,eqv is not recommended unless the values are written to a file after every substep, which may produce quite a bit of data. The methods are only equivalent for monotonic loading, which is not the case for thermal cycling. Here, the second method would underestimate the creep strain.

```
!-- Eutectic Solder: isotropic, viscoplastic,
!-- Elastic Properties:
MPTEMP,
                    1,
                         210,
                                 398,
                                        423
                                            ! Temperature
            mat_pb, 1,
MPDATA, EX,
                       36000,
                               21000,
                                      19000
                                            ! E-modulus
                         .36,
                                 .36,
MPDATA, NUXY, mat_pb, 1,
                                        .36
                                            ! Poisson's Ratio
MPDATA, ALPX, mat_pb, 1, .24e-4, .24e-4, .24e-4
                                            ! CTE
! -- Calls user-defined subroutine "usercreep.F" for Creep Strain evaluation
TB, CREEP, mat_pb,,,100,
TBDATA, 1, 1.39e-6,
                     1.96, 7.6626e-11, 48157.0, 2.38e3
TBDATA, 6,
             7.1, 81239.0,
!-- Accumulation of Creep Strain
TB, STATE, mat_pb,,5
!-----
```

3.1.4 Lifetime Prediction and Failure Mechanisms for Eutectic Tin-Lead Solder

In order to correlate bump failure determined during a thermally induced low cycle fatigue experiment with a computationally accessible damage criterion one needs a theory which describes this correlation. Based on such a relationship the bump is 'calibrated' as a reliability-sensitive device (in this case the solder bump acts like a reliability-sensor) under given boundary conditions. Once this is done this relationship can be used to extrapolate to other tin-lead solder interconnect assemblies, i.e. to predict lifetime for a specific set-up by simulation.

In order to establish this correlation one draws upon the hypothesis, that damage and its evolution can be described via state variables which are measurable as well as describable by a constitutive model, i.e. by numerical simulation of this state [15,73]. As usual the argumentation follows the scheme of system, drive and response on various levels. Correlation must ideally be given at each stage, and the better a single link in this chain is,

⁷Ansys commands are given in typewriter style.

the better the final result will be. This scheme is depicted in figure 3.4, illustrating this one-to-one correspondence of simulation (bottom left) and experiment (top right).

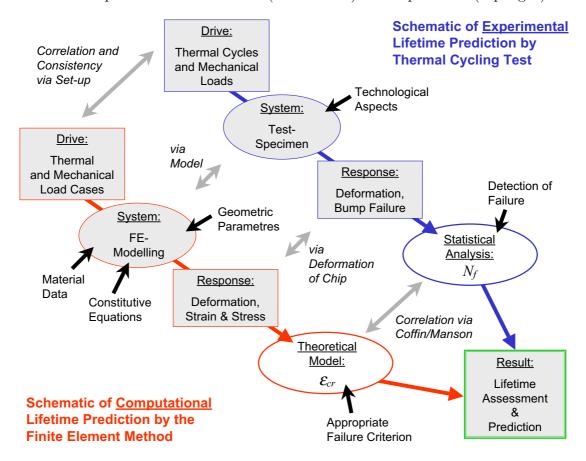


Figure 3.4. Schematic representation of the correlation between simulation steps and their respective experimental counterparts in the framework of the Coffin-Manson approach. From top left to bottom right the argumentation proceeds and makes use of correlations (italics, grey arrows) to allow for consistency checks at each stage. Procedures are depicted as ovals, quantities in rectangles. This figure can also be thought of as a roadmap through the crucial points of this work.

The system we contemplate is a flip-chip assembly with an attached heat spreader, more abstractly spoken a multi-layered assembly with small embedded solder interconnections. This assembly is liable to solder fatigue cracking which proves fatal for the electrical function of the device. If it occurs, it has to be modelled via an appropriate failure criterion or parameter which should ideally reflect the physics of the damage mechanism as a function of a set of state variables [74]. For low cycle fatigue (large periodic inelastic deformation) of eutectic solder this will involve evaluating the stress and strain states as a function of applied thermal and mechanical loads.

A word has to be said about possible delamination at various interfaces [12] of the assembly. If delamination occurs e.g. at the chip-underfill interface, it may severely accelerate bump failure as it eliminates the beneficial effect of chip bending by the underfill. In any case a chip has to be checked for delamination (by ultrasound microscopy) and its effect to

be accounted for in the model. A fracture mechanics approach to interface delamination has not been attempted, as it necessitates sophisticated computational effort [47, 48] to describe stress field singularities at crack-tips or edges of dissimilar materials [75] and a comprehensive experimental treatment [76] beyond the scope of this work.

Stress and strain state can be appropriately evaluated by nonlinear and rate-dependent finite element simulation based on constitutive material laws and corresponding data after input of the respective geometry of the system to be modelled [25,77]. This *correlation* has been established in the last section where the employed materials were characterised and their behaviour implemented into FE-tools. The appropriate numerical *correlation* is established FE-modelling.

The external drive the system is subjected to is the next crucial ingredient. For obvious reasons one wants the drive to represent the typical load conditions the device is exposed to in its service life. A standardized thermal cycle [19] is used to this end where the environmental conditions (e.g. automotive sector with temperatures $T \in [-40; 125]$ °C) are thought to be controllably and representatively applied in an accelerated manner. This allows to compare different assemblies to one another and make statements of reliability based on specified testing conditions. To establish correlation for the drive input loads, their effect has to be measured and properly mirrored by the simulation (section 5.1).

The response of the system to the imposed drive is subsequently recorded. This involves an analysis of the strain and stress states within the bump for the simulation and a statistical analysis of bump failure on the experimental side. Various theoretical approaches exist to describe the correlation between the two [73]. For low cycle fatigue phenomena one draws upon the irreversible inelastic (creep-) deformation which is a measure for damage: Alternate deformation induced by periodic thermal loading causes the solder to creep and to accumulate creep strain which leads first to the built-up of cavities on a microscale, then to the initiation and coalescence of microcracks until the bump ultimately fails by propagation of a macrocrack.

Thereby the approach works on the principle that the amount of accumulated inelastic strain per converged periodic⁸ cycle is correlated to the statistical mean of a distribution which can adequately describe bump failure. For this case the Weibull-distribution is best suited and the mean is calculated for the cycles to failure. A correlation can be established by the well-known Coffin-Manson relationship which will be explained in the next section. This relationship which involves free coefficients to be determined as a result of a best fit procedure may then be used for extrapolation as indicated above. Therefore it will be the aim to 'calibrate' our solder bump – or reliability sensor – by determining these Coffin-Manson coefficients.

On the way it is advisable to countercheck the correlation on different levels, i.e. to check for consistency between simulation and experiment by more easily accessible i.e. measurable quantities. For example the macroscopic behaviour (see again figure 3.4) of the assembly represents a well-suited starting-point. Deformations (e.g. curvature of the chip) as a function of mechanical load and, if possible, of temperature can be recorded and simulated and provide a quantitative statement about the quality of the correlation [24] at this stage.

⁸The system will usually go through an initial transient phase until the response becomes stably periodic.

Below we want to deal in detail with the correlation between measured bump failure and computational inelastic strain in solder fatigue. This works on the principle that the solder bump is the crucial point of the total assembly and that there is no delamination which could override solder fatigue as governing failure mechanism.

3.1.5 Thermally Induced low Cycle Solder Fatigue: Reliability Concept According to Coffin-Manson

The Coffin-Manson relation [40, 41] states that the mean cycles to failure $\bar{N}_f = N_{50\%}$, i.e. the point at which 50 % of the parts subject to cyclic loading have failed is correlated to a failure parameter evaluated for one cycle ψ by a simple relationship

$$\bar{N}_f = c_1 \psi^{c_2},$$
 (3.18)

where c_1 and c_2 are constants which depend on the material and the characteristics of the cyclic load [73,78]. In low cycle fatigue, i.e. conditions of high periodic stress and strain, creep represents nearly all of the inelastic deformation at high homologous temperatures [15,22,64]. Under these conditions eutectic solder failures are due to accumulated creep-induced damage. Creep is the dominant failure mechanism [17,43,68]. Therefore creep strain [26, 38, 39, 43], (or sometimes also the inelastic, dissipated energy⁹ [23] which is equal to the area of the hysteresis loop) is taken as failure parameter. Elastic strains are also negligible in this regime as deformations occur slowly under given test-conditons. So $\bar{\varepsilon}^{cr} \gg \bar{\varepsilon}^{el}$ is a good assumption and so damage done by elastic strain is also negligible in this regime. So the accumulated (equivalent) creep strain per cycle $\psi \equiv \bar{\varepsilon}^{cr}$ is used in the Coffin-Manson relaionship, which is written now as

$$\bar{N}_f = c_1(\bar{\varepsilon}^{cr})^{c_2}. (3.19)$$

Empirically it was found that $c_2 \in [-2; -3]$ for many ductile materials [78] for isothermal low cycle fatigue. This relation is taken to hold also for thermally induced low cycle fatigue and for eutectic solder bumps values of $c_2 \in [-1.0; -2.1]$ are found [11, 22, 23, 38, 39, 80, 81] under cyclic thermal load. c_1 is assumed to depend on a variety of material and cycle parameters [23] showing that a correlation between isothermal and thermal or different thermal data is still an unresolved question. For this reason it may be argued to compare only results on a relative scale (for the same type of cyclic load and taking also geometric features of the bump into consideration) where c_1 drops out as a parameter. In addition comparability hinges critically on the correct detection of experimental failure, a correct statistical analysis and correct computation and reading of the failure criterion.

For eutectic solder bumps under thermally induced cyclic strains creep has been shown to be the governing damage mechanism. In the course of its fatigue life it accumulates creep strain in localized, band-like structured zones [15] as a result of an inhomogeneous

⁹For Coffin-Manson plots the strain produces a higher sensitivity due to a functional dependence $\bar{\varepsilon} \sim W^{\frac{1}{2}}$ and is therefore preferred. Also conflicting, non-monotonic results have been obtained which render the use of W questionable [79]. Still it would have been interesting to consider W for comparison, but this requires further customizing of a subroutine for the specific creep law in use as this currently represents a non-standard use of Ansys.

stress distribution over the bump [42]. These bands act as weakened zones [80] due to an agglomeration of dislocations which grow by stress-assisted diffusion [73] before microcrack-nucleation starts. So cracks are assumed to start at a local maximum of strain [24] and follow a path or band of high local creep strain which has to be taken as its representative value responsible for the volume damage [38].

It has been discussed [67] if or to what extent the microstructure of eutectic solder influences its fatigue life as it is well known that it depends e.g. on solidification conditions and its loading history (annealing, cycling). As already mentioned, creep and its mechanisms depends also on this microstructure which evolves during cycling and causes consequently a drift in make-up of the mechanisms. As the solder coarsens its creep rate hinging on grain-boundary sliding decreases and the overall steady-state creep rate may also. Still it is undecided if this may be beneficial or harmful for the fatigue life of the joint [44]. There are indications though [43] that the initial preparation of solder (e.g. by reflow, cooling, storage) does not have a great effect on its reliability.

As has been pointed [77] out equation 3.19 is based upon a stable creep cycle (closed hysteresis loop) which displays a constant microstructure (secondary creep) and surely represents a linear extrapolation: So to a first approximation linear accumulation of damage is assumed, i.e. $\bar{\varepsilon}^{cr} \neq f(N)$ or for the total failure creep strain $\bar{\varepsilon}_f^{cr} \sim N$. Hereby the damage processes are assumed to start from the point where the stable state is reached as shown in [43]. It is on the other hand impossible to simulate 1000 cycles or more and actively incorporate feedback via the phase size into FE-simulations for a flip-chip or a package of related complexity for reasons of numerical stability (due to nonlinearities) and time.

The Coffin-Manson relationship can be made plausible despite of its empirical origin (see e.g. [74]) by an approach based on the thermodynamics of irreversible processes without taking into account a detailed reference to the complexity of microstructural effects. Here the basis forms the introduction of a damage variable ϕ which is sometimes also called a load-drop parameter (cf. [36] or [43]):

$$\phi = \frac{A_{\phi}}{A_0} = \begin{cases} 0 & \text{(no failure)} \\ 1 & \text{(total failure)} \end{cases} , \tag{3.20}$$

which describes the ratio of damaged area A_{ϕ} with respect to the area A_0 prior to damage. The idea behind this is that at regions where the material is damaged (cavity) it cannot sustain any load any more. This results in a higher effective stress $\tilde{\sigma}$, with

$$\tilde{\sigma} = \frac{\sigma}{1 - \phi} \ge \sigma. \tag{3.21}$$

(In the following paragraph we want to assume that stresses and strains are given in equivalent entities and leave out the bar over the symbol.) It is postulated that the respective state-governing equations and kinetic damage evolution laws can be obtained by differentiation of the thermodynamic potential F (free energy) with respect to the corresponding associated variables.

$$F = F(T, \varepsilon, \phi)$$
 from which e.g. $Y = \rho \frac{dF}{d\phi}$ (3.22)

the strain energy density release rate Y can be derived. Analogously a dissipation potential D with

$$D = D(Y, T, \phi)$$
 from which by $\dot{\phi} = \frac{dD}{dY}\dot{\lambda}$ (3.23)

the evolution of damage with time $\dot{\phi}$ can be obtained where the material's dissipative constitutive behaviour has to be incorporated via the viscoplastic multiplier $\dot{\lambda}$ [74], which for creep entails a strain-damage coupling.

Without going into further detail a general evolution equation for creep damage can be derived [74] which looks like

$$\dot{\phi} = \frac{Y}{S} \dot{\varepsilon}^{cr} = \frac{\sigma^2}{2ES(1-\phi)^2} \dot{\varepsilon}^{cr}.$$
 (3.24)

where the *damage* rate is now proportional to the *creep* rate $\dot{\varepsilon}^{cr}$. S can be interpreted as damage resistance strength and E is as usual the elastic modulus. All quantities will depend on temperature and macroscopic (no structural) material properties.

This equation would now have to be solved (in general numerically) taking into account the interdependence of creep strain rate and damage, i.e. effective stress $\tilde{\sigma}$. To renounce a self-consistent evaluation we make the following assumptions for an extrapolation:

- The damage is constant over the period of one cycle.
- The stable hysteresis loop is approximated by a rectangle symmetric to the origin and can therefore be described by a constant stress and (creep-) strain amplitude $\Delta \sigma/2$ and $\Delta \varepsilon^{cr}/2$.
- The cyclic stress-strain relationship is given by a Ramberg-Osgood type of equation

$$\Delta \varepsilon^{cr} = \left(\frac{\Delta \sigma}{c(1-\phi)}\right)^{\frac{1}{m}},\tag{3.25}$$

where m is the cyclic fatigue ductility exponent [73] and c a constant; both are material specific.

We can thus evaluate the damage per cycle (of duration $t = \tau$):

$$\frac{d\phi}{dN} = \int_{Cucle} dt \ \dot{\phi} = 2 \frac{(\Delta \sigma/2)^2}{2ES(1-\phi)^2} \int_0^{\frac{\tau}{2}} dt \ \dot{\varepsilon}^{cr} = \frac{c^2}{4ES} (\Delta \varepsilon^{cr})^{(1+2m)}, \tag{3.26}$$

and making use of equation 3.20 for failure

$$\phi_f = \int_0^{\bar{N}_f} dN \, \frac{d\phi}{dN} = 1 \tag{3.27}$$

and assume linear aging we obtain an expression

$$\bar{N}_f = \frac{4ES}{c} \left(\frac{1}{2}\right)^{-(1+2m)} (\varepsilon^{cr})^{-(1+2m)},$$
 (3.28)

where we have set $\varepsilon^{cr} = 2\Delta\varepsilon^{cr}$. This equation takes the form of a Coffin-Manson relationship, where the fatigue ductility exponent $c_2 = -(1+2m)$ should be of the order of 2. Indeed the cyclic hardening exponent m is found to lie within $m \in [0.05; 0.2]$, for higher temperatures also $m \in [0.05; 1]$ ([70]). Derivations stating a larger influence of m like e.g. $c'_2 = -(1+5m)$ are also found in literature [73].

For thermal low cycle fatigue the above argument would imply a temperature dependence of all parameters. The integration over one cycle would require a rigorous treatment of the *T*-dependence. Although a hysteresis loop for a thermal cycle as measured and simulated [43,69,81] could still to first order be approximated by a rectangle, the procedure would become handwaving for the cyclic hardening exponent.

For a simple triangular temperature profile, however, this integration can be carried out: Let us assume a purely displacement-driven assembly so that to a good approximation all thermal strain is converted into creep strain for a slow enough temperature variation. Then we may write:

$$\varepsilon^{cr}(t) \sim \varepsilon^{T}(t) = \Delta \alpha (T(t) - T(0)) \sim T(t) \sim t,$$
 (3.29)

where we assume a linear time-temperature dependance as in a triangular profile with $\Delta T = T(\tau/2) - T(0)$. Using again equation 3.26 to evaluate the damage per cycle we have to properly integrate over one cycle, this time making use of the creep law 3.7 in a simplified form, written for the effective stress (taking equivalent entities):

$$\tilde{\sigma}(t) \sim T(t)^{\frac{1}{m}} \dot{\varepsilon}(t)^{\frac{1}{m}} e^{\frac{Q}{mkT(t)}}, \tag{3.30}$$

where m is this time an average stress exponent, which for our creep law is $m \in [2; 3]$ in the considered stress interval (see figure 3.2).

So we calculate with respect to equation 3.26:

$$\frac{d\phi}{dN} = \int_{Cycle} dt \ \dot{\phi} = 2 \int_0^{\frac{\tau}{2}} dt \ \frac{\sigma^2(t)}{2ES(1-\phi)^2} \dot{\varepsilon}(t) \sim \int_{\varepsilon(T(0))}^{\varepsilon(T(\tau/2))} d\varepsilon \ \varepsilon^{\frac{2}{m}} e^{\frac{2Q}{mk\varepsilon}}, \tag{3.31}$$

where we have made use of $t \sim T \sim \varepsilon$ and $\dot{\varepsilon} = const.$ Using a series expansion of the exponential function we can easily show that the leading terms of the sum give a dependance on according to

$$\frac{d\phi}{dN} \sim \varepsilon^{\frac{2}{m}+1} + \varepsilon^{\frac{2}{m}} \left(\frac{2Q}{mk\varepsilon}\right) + \varepsilon^{\frac{2}{m}-1} \frac{1}{2} \left(\frac{2Q}{mk\varepsilon}\right)^2 + \cdots$$
 (3.32)

With the first term governing the functional dependance, we apply equation 3.27 and we obtain now a Coffin-Manson type of equation as:

$$\bar{N}_f \sim (\varepsilon^{cr})^{1+2/m},$$
 (3.33)

where with $m \in [2;3]$ we obtain a Coffin-Manson exponent $c_2 = 1 + 2/m \approx 2$. In this respect the stress exponent influences the Coffin-Manson exponent. This explains also an other tendency: Lead-free tin-based solders in general display a larger stress exponent (see e.g. [42, 82]), which should result in a smaller Coffin-Manson exponent. This is indeed

the case as stated in [83]. Still, this contemplation only serves to make a statement of plausibility. As the conditions for our case are much more complicated, the integration has to be carried out numerically by the finite element tool.

An other interesting topic is a deviation from linear aging and how it would alter the above contemplations. If we take a weak power law dependence with $n \approx 3$ as suggested by e.g. [67] like

$$\frac{d\bar{\varepsilon}^{cr}}{dN} \sim N^{\frac{1}{n}},\tag{3.34}$$

an evaluation similar to equation 3.27 would yield

$$\bar{N}_f \sim (\bar{\varepsilon}^{cr})^{\frac{n}{n+1}c_2}$$
 (3.35)

which reduces the value of the fatigue ductility exponent. This hereby considered slight increase in creep induced damage per cycle could e.g. be caused by solder coarsening and hence reduce bump lifetime. So an experimentally found exponent with $|c_2| < 2$ could indicate a deviation from linear ageing due to microstructural changes with lifetime reducing effect as in [67]. In this work, however, we assume linear aging implied in the Coffin-Manson exponent.

3.2 Linear Viscoelasticity for Thermosetting Polymers

In our assembly we have many materials for which a linear viscoelastic behaviour can be assumed as they fall among the class of thermosetting polymers. The importance of the consideration of rate-dependence for FE-modelling of electronic packages has already been stressed [75,84] or [85]. The significant change in the properties of the material as a function of temperature and time needs therefore consideration.

A viscoelastic material has a deformation that consists of both an instantaneously recoverable part and a time-dependent, mechanically (not thermodynamically) recoverable part (retarded elasticity). This means, that although the system can reestablish its initial state of deformation, it has nevertheless dissipated energy which manifests itself in a hysteresis loop in a stress-strain diagram. Viscoelasticity combines the characteristics of an elastic body which obeys to Hooke's law

$$\sigma = E\varepsilon^{el} \tag{3.36}$$

and a perfect viscous fluid which features

$$\sigma = \eta \dot{\varepsilon}^{vs}. \tag{3.37}$$

Here E and η are the elastic and viscous modulus respectively.

Further, these class of materials feature a glass transition temperature T_g below which the material is in a stiffer, 'glassy' state and above which is behaves rubber-like. This change in the material's behaviour influences the elastic modulus, its rate-dependence and the CTE. Around T_g the change of the properties is strongest. Therefore this point manifests itself in DMA, TMA and relaxation testing [86, 87]. Shrinking of the polymers was not considered as the manufacturers state a negligible cure dependance in this respect.

In the following we will give a brief outline of the theory of viscoelasticity, employed models and the resulting constitutive equations. Measurement techniques are presented and exemplified for a filled epoxy resin which serves as underfill. Finally the process of implementing the data is explained.

3.2.1 Material Behaviour and Constitutive Equations

A simple model to describe viscoelastic relaxation is the Maxwell model (cf. figure 3.5 to the left). It consists of a spring symbolising the elastic part and a dashpot is meant to embody viscosity connected in series. When a constant strain is applied to the model, then the stress relaxes exponentially to zero.

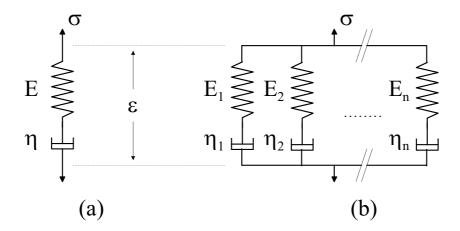


Figure 3.5. Maxwell-element (a) for viscoelasticity-model composed of a spring (linear elastic) and a dashpot (viscous). Generalized Maxwell-model (b) is made up of n Maxwell-elements connected in parallel.

Following this description, one can formulate the differential equation using $\varepsilon(t) = \varepsilon^{el}(t) + \varepsilon^{vs}(t)$, $\dot{\varepsilon}(t) = \dot{\varepsilon}^{el}(t) + \dot{\varepsilon}^{vs}(t)$ and defining $\lambda = E/\eta$:

$$\dot{\varepsilon}(t) = \left(\frac{1}{E} d_t \cdot + \frac{1}{\eta}\right) \sigma(t) \qquad \Leftrightarrow \qquad E\dot{\varepsilon}(t) = (d_t \cdot + \lambda) \sigma(t), \tag{3.38}$$

where d_t is a differential operator with respect to time.

This differential equation is knowingly solved by a decaying exponential function. This can be made clear by applying the Laplace-transform $\mathcal{L}(f(t)) = \tilde{f}(s)$ and $\mathcal{L}(d_t f(t)) = s\tilde{f}(s) - f(0^+)$ [58] and incorporating the boundary condition that the strain has been applied as $\varepsilon(t) = \varepsilon \theta(t)$ to 3.38 (see e.g. [88]):

$$Es\tilde{\varepsilon}(s) = (s+\lambda)\tilde{\sigma}(s) \qquad \Leftrightarrow \qquad \tilde{\sigma}(s) = \frac{E}{s+\lambda}s\tilde{\varepsilon}(s).$$
 (3.39)

It has been made use of Hooke's law again in the shape of $E\varepsilon(0^+) = \sigma(0^+)$. This reduces the differential equation to a normal algebraic equation. Taking the inverse transform \mathcal{L}^{-1}

now we obtain an expression for $\sigma(t)$ in the form of a convolution integral:

$$\sigma(t) = \mathcal{L}^{-1}\left(\frac{E}{s+\lambda}\right) \otimes \mathcal{L}^{-1}\left(s\tilde{\varepsilon}(s)\right) = \int_0^t dt' \ R(t-t')d_{t'}\varepsilon(t'),\tag{3.40}$$

where

$$R(t) = \mathcal{L}^{-1}\left(\frac{E}{s+\lambda}\right) = Ee^{-\lambda t}$$
(3.41)

has been used. R(t) is the relaxation function.

Now the general solution function can be written:

$$\sigma(t) = \int_0^t dt' \ Ee^{-\lambda(t-t')} d_{t'} \varepsilon(t'). \tag{3.42}$$

If we now want to obtain the solution for a special case, e.g. the displacement step-loaded Maxwell-element at time $t=t_0$ this specifies the drive function $\varepsilon(t)=\varepsilon\theta(t-t_0)$ (with $\theta(t)$ being the Theta or Heaviside-Function) and consequently the derivative with respect to time $\dot{\varepsilon}(t)=\varepsilon\delta(t-t_0)$ yields the Dirac-distribution.

Insertion into equation 3.42 does reduce to

$$\sigma(t) = \varepsilon E e^{-\lambda(t - t_0)} \tag{3.43}$$

as expected. This behaviour is depicted in the graphs of figure 3.6. The individual strain distribution can be easily calculated from equations 3.43 and 3.36 and 3.37.

This model, however, does not fully describe viscoelastic behaviour. To describe strain recovery and convergence (for a creep test) one needs to expand the Maxwell-model (MM) by putting several of them in parallel. This arrangement, to be seen in figure 3.5 to the right, is also referred to as the generalized Maxwell-model (GMM).

The mathematical description of the GMM is analogous to the Maxwell-model and will result in a Prony-series. We start with

$$\sigma(t) = \sum_{i=1}^{n} \sigma_i(t)$$
 and $\varepsilon(t) = \varepsilon_i(t)$ (3.44)

where the stresses σ_i of the individual Maxwell-elements add up to give the total stress. We use the differential equation for each MM (equation 3.38) and take the sum over the stresses:

$$\sigma(t) = \sum_{i=1}^{n} \sigma_i(t) = \sum_{i=1}^{n} \frac{E_i}{\lambda_i + d_t} \dot{\varepsilon}(t). \tag{3.45}$$

Again we make a Laplace transform and due to its being linear the sum remains to give an algebraic equation

$$\tilde{\sigma}(s) = \sum_{i=1}^{n} \tilde{\sigma}_{i}(s) = \sum_{i=1}^{n} \frac{E_{i}}{\lambda_{i} + s} s\tilde{\varepsilon}(s). \tag{3.46}$$

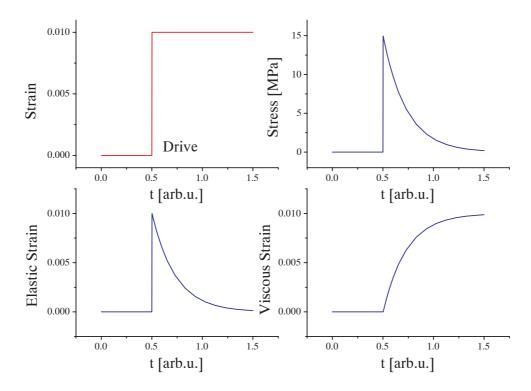


Figure 3.6. The axial relaxation response for a step strain loaded Maxwell-model. In this example, the springs have moduli of 1000 and 500 MPa respectively, the time-constant of the dashpot has been taken to be $\tau_1 = 0.5$ a.u.

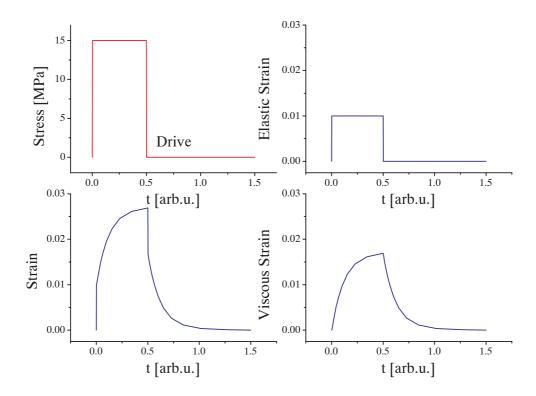


Figure 3.7. The axial creep response behaviour for a generalized Maxwell-model. $\tau_1 = 0.2$ a.u. Note the strain recovery and finite strain upon constant stress.

Taking the inverse Laplace transform making use of the distributivity of the convolution it allows

$$\sigma(t) = \int_0^t dt' \ R(t - t') d_{t'} \varepsilon(t') \qquad \text{where again} \qquad R(t) = \sum_{i=1}^n E_i e^{-\lambda t} s \tilde{\varepsilon}(s). \tag{3.47}$$

Taking again the case of a step load as in equation 3.43 we obtain the solution in the shape of what is called a Prony-series.

$$\sigma(t)/\varepsilon = E(t) = \sum_{i=1}^{n} E_i e^{-\lambda_i t}.$$
 (3.48)

This function is a linear combination of non-orthogonal functions (as long as λ remains a real number) apt to describe monotonously exponential decaying asymptotic behaviour. Here, λ_i are the inverse relaxation times τ_i and E_i the Prony-coefficients for the respective relaxation process or Maxwell-element.

This, slightly more complex model describes linear viscoelasticity in a better way. The model includes the extreme cases of missing out a spring or a dashpot. This can then account for a finite asymptotic elastic modulus E_{∞} and strain recovery, both of which are features often encountered with polymers. This behaviour is depicted in figure 3.7. For a real polymer the individual Prony-coefficients E_i , λ_i can be thought of as being characteristic of internal relaxation processes.

For the sake of completeness it is mentioned, that also other models exist to describe viscoelastic behaviour (Kalvin-Voigt-Model, Standard-Model, etc., see e.g. [58]). They use springs and dashpots in other combinations but can be shown to be equivalent to the GMM in their generalised formulation.

Equations of the type of 3.45 are also called a hereditary integral equation. The integral therein describes the stress-history of the system by integrating over all past strain input $d\varepsilon(t)$ at time t=t'. The bilocal function R(t-t') in the time domain communicates all time-dependent behaviour to the current or observation time t. The relaxation function embodies the material system, whereas the remaining functions the external drive applied to the system to obtain the response which is in this case the stress.

It shall be mentioned that the material is thought not to depend on absolute time. No aging is taken into account, only rate dependent behaviour on a relative time scale with respect to to the observation time. Otherwise one would need $R(t - t') \to R(t, t')$.

In case of a creep experiment it is more practical to deal with the creep compliancy function J:

$$\varepsilon(t) = \int_0^t dt' J(t - t') d_{t'} \sigma(t') \quad \text{where} \quad \int_0^t dt' J(t - t') d_t R(t') = 1 \quad (3.49)$$

is the one to one relationship between the relaxation function and the compliance.

The above equation is also a manifestation of Boltzmann's superposition principle which states that a material is viscoelastic if when two stresses are applied a two different times the strain response at any time subsequent to either of the previous is the same as though any of the stresses were acting separately.

For a real, three-dimensional linear viscoelastic isotropic body one has to consider the full tensorial formulation for a multi-axial state of stress and strain [58,89]:

$$\sigma_{ij}(t) = \int_0^t dt' \ 2G(t - t')\dot{e}_{ij}(t') + \int_0^t dt' \ 3K(t - t')\dot{e}_m(t')\delta_{ij},\tag{3.50}$$

where a tensor decomposition analogous to equation 3.11 for the strain tensor has been used. The strain deviator interacts with the shear modulus G(t) and the volumetric strain with the bulk modulus K(t). Special attention has to be paid to the time-dependence, which imposes [89–91]:

$$G(t) = \mathcal{L}^{-1} \left(\frac{\mathcal{L}E(t)}{2(1 + \mathcal{L}\dot{\nu}(t))} \right)$$
 (3.51)

$$K(t) = \mathcal{L}^{-1}\left(\frac{\mathcal{L}E(t)}{3(1 - 2\mathcal{L}\dot{\nu}(t))}\right), \tag{3.52}$$

where the expected familiar correspondence

$$G = \frac{E}{2(1+\nu)} {(3.53)}$$

$$K = \frac{E}{3(1 - 2\nu)} \tag{3.54}$$

holds for the time independent case or the initial elasticity-dominated instantaneous response or the asymptotic case where no rate dependence is active any more i.e. the cases where $G(t_0) = G_0$ and $G(t_\infty) = G_\infty$. The same is true for K. The derivation of these equation is given in the appendix A.3.

3.2.2 Experimental Results of Relaxation Tests: Exemplified for an Underfill (Silica-filled Epoxy-Resin)

Now we want to measure the viscoelastic behaviour of a polymer which can be assumed to have a linear viscoelastic response. Two methods of testing are usually used for this purpose. The first is a relaxation test where a constant strain (within the elastic limit) is applied at a time $t = t_0$ within a certain time (specified is t = 1 s) and the material is left to relax over the period of one hour. This test seems well suited for materials which are shapable as dog's bone specimens (see figure 3.8) to fit into a tension testing machine. Further, this test is expected to yield suitable results since the data is obtained on a time scale of one hour which is of interest for a thermal cycling test, which usually use ramp and hold times of several minutes.

This procedure worked well for the harder thermosetting polymers as the underfill, soldermask and the organic board but the softer elastomers could not be clamped by the tension testing machine. But these elastomers (silicone-based) were successfully tested by frequency-driven measurement techniques as there are DMA and rheometre. There, the viscoelastic properties can be converted from the frequency into the time-domain and be made comparable to the relaxation data (as is shown in the next section).

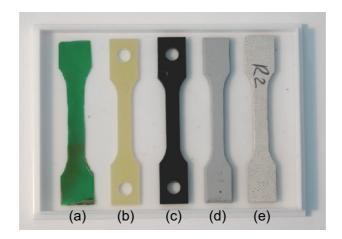


Figure 3.8. 'Dog's-bone' specimens as they are used for the viscoelastic relaxation test. All depicted materials were characterised: (a) Soldermask, (b) Organic Board, (c) Underfill, (d) Silicone Adhesive and (e) Epoxy-Silicone Adhesive. For dimensions see figure B.1.

The first method is exemplified for the case of a silica filled epoxy resin. These materials are of special interest in electronic packaging [17], especially as underfills are concerned which require matched properties to the employed solder [20]. The filler allows to manipulate the mechanical properties of polymers. To increase the elastic modulus or reduce the CTE for instance, one may add micro-particles of a different material, e.g. silica (SiO_2) . However, the material will still display a viscoelastic response due to the polymer matrix.

The measurement presented here were conducted at different temperatures on a universal testing machine (type Zwick 1446). The typical outcome is presented in figure 3.9.

As pronounced temperature dependance, a softening of the material is discernible around the glass-transition temperature $T_g = 125$ °C. This behaviour is typical for epoxy-resins. E(t) does not relax to zero though but to the asymptotic value E_{∞} .

This measured data is now to be made available to the FE-tool. For the incremental evaluation of viscoelastic stress and strain it is computationally advantageous to have an analytical and continuous function for the material data. The time-honoured way to do this is by introducing a temperature dependent pseudo time $t' = \xi(t)$, a relationship which is defined by a shift-function a(T,t). It encompasses the whole temperature and time scale [89,92].

$$t' = \xi(t) = \int_0^t d\tau \ a(T(\tau))$$
 (3.55)

which reduces to

$$t' = \xi(t) = a(T)t \tag{3.56}$$

for the simple case of a non explicitly time-dependent temperature ($\partial_{\tau}T = 0$) as we want to assume. This shift function is characteristic for the respective polymer and is a manifestation of what is called thermo-rheologically simple. This states the following: There is a defined correlation between the material's behaviour at high temperature on a short

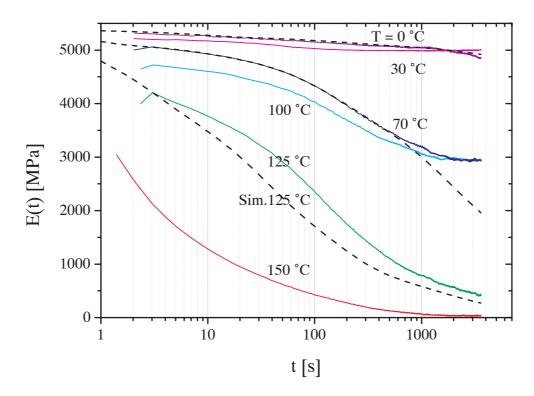


Figure 3.9. Measured relaxation data E(t) of underfill. Simulated data is printed in dashed lines for verification.

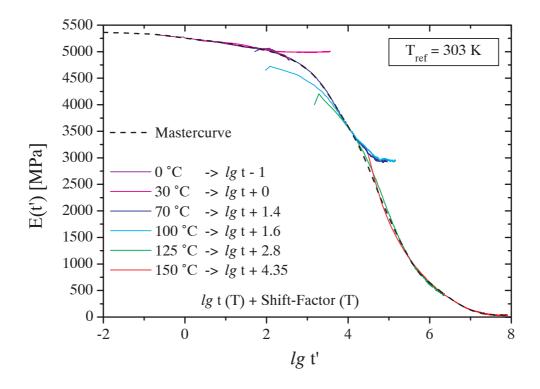


Figure 3.10. Temperature-time shifted data for construction of mastercurve (dashed line). The individual shift factors are given for each temperature. t refers to the (T-dependent) time shifted by a factor with respect to the time at T_{ref} measured on a logarithmic scale.

time scale and low temperatures at a larger time scale. The respective relaxation or creep processes occur faster for high temperatures but are of the same nature, i.e. T affects only the relaxation times hence allowing a temperature-time superposition principle.

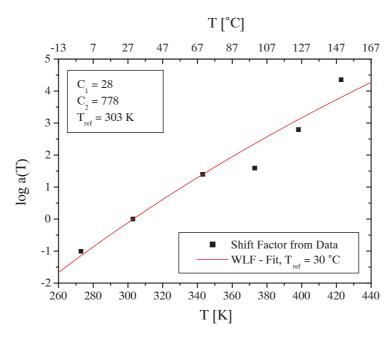


Figure 3.11. WLF shift function.

Based on this assumption a so-called master curve can be constructed. This is done by shifting the curves of figure 3.9 on the logarithmic time scale by the shift factor $\lg a(T)$ until it produces a continuous function with the next lower temperature curve.

It is easy to see that on a logarithmic scale 3.56 defines a shift factor:

$$\lg t' = \lg t + \lg a(T) \tag{3.57}$$

The result of this process is demonstrated in figure 3.10. The respective values for the shift function are plotted versus temperature in figure 3.11 and fitted to the so-called WLF-function¹⁰ (William, Landell, Ferry) by two coefficients $c_{1,2}$.

$$\lg a(T) = \frac{c_1(T - T_{ref})}{c_2 + (T - T_{ref})}$$
(3.58)

Hereby the mastercurve is defined for the reference temperature T_{ref} . The last step is the approximation of the mastercurve by a Prony-series expansion as presented in the last section. This is possible since the mastercurve is always a monotonously decaying function with exponential asymptotic behaviour. The fit is carried out for the pseudo-time $t'(T_{ref})$. It has been proved suitable to use one Prony element for each order of magnitude of time $\tau_i = 1/\lambda_i$, although this obviously does not reflect any specific material relaxation

 $^{^{10}}$ According to theory this function is strictly valid only around T_g . Practical experience has proved though that it can also be applied to the whole temperature scale. Also other fit-functions are found in literature [89].

mechanism any more. But here we are only looking for a fit-function. This underfill consequently exhibits a viscoelastic relaxation on a pseudo-time scale of up to ten orders of magnitude.

As we only measure the relaxation of the stress this has to be translated into a time-dependent modulus according to equations 3.50 and 3.52. In this respect we have fitted E(t') by the modified Prony-series

$$E(t') = \sum_{i=1}^{m} E_i e^{-\frac{t'}{\tau_i}} + E_{\infty}, \tag{3.59}$$

where we have missed out one dashpot $\tau_n = \infty$ and retain as asymptotic E-modulus E_{∞} . Consequently we get

$$G(t') = \sum_{i=1}^{m} G_i e^{-\frac{t'}{\tau_i}} + G_{\infty}$$
 (3.60)

$$K(t') = \sum_{i=1}^{m} K_i e^{-\frac{t'}{\tau_i}} + K_{\infty}.$$
 (3.61)

Note that the respective relaxation times need not necessarily be the same for shear and bulk modulus.

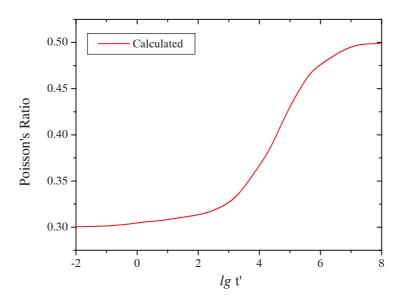


Figure 3.12. Calculated behaviour of Poisson's ratio. For high temperatures or very long relaxation times the material becomes incompressible. This has to be so since E relaxes and K stays constant (see equation 3.54).

To a good approximation [84] we assume that the bulk modulus is not a function of time, i.e. that there is no volumetric relaxation but only a purely elastic response. So we set $K(t) = K_0 = K_{\infty}$. It follows with 3.54 that near T_g , where E assumes small values the material approaches the incompressible limit, i.e. Poisson's ratio assumes the value $\nu \leq 0.5$

which is experimentally observable. This is indeed confirmed by evaluation of equation 3.52 based on the measured values E(t') (see 3.12). Depending on which quantities are required by the FE-code (usually E(t), $\nu(t)$ or G(t), K(t)) a conversion according to equations 3.52 and 3.52 can (numerically¹¹) be made.

Once the data has been implemented into the program the relaxation test by which the data was obtained was simulated for a check. The result is depicted as solid black lines in the respective diagrams (see e.g. for the underfill in figure 3.9).

The deviation from the measured curves is due to the shift-function which governs now the time-temperature relationship. As can be seen from figure 3.11, the temperatures for which the shifted points lie off the curve a computational deviation will appear. Still this inaccuracy is small bearing in mind that the manually effectuated shift process gives rise to deviations as well as a temperature drift during measurement. It should hereby not be forgotten that we do interpolate ten orders of magnitude¹² on a time scale!

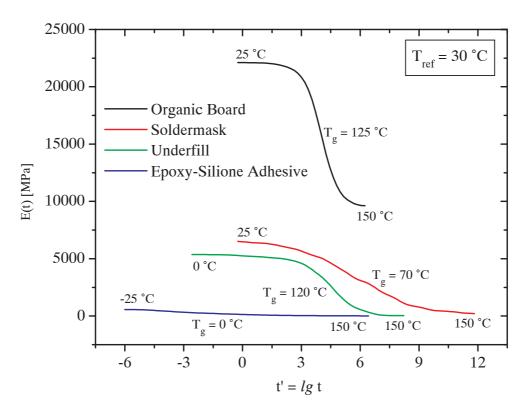


Figure 3.13. Mastercurves of all viscoelastic materials determined in this work by relaxation testing. Highlighted is the glass transition region and the extremal temperatures for which the material was characterised. $T_{ref} = 30$ °C for all materials.

Further measurements comprised TMA for determination of the CTE. The result data can be found in the respective data input files given at the end of this chapter or in

 $^{^{11}{\}rm This}$ conversion can easily made by expert systems featuring a Laplace-transformation like Mathematica, Maple or Matlab.

¹²This is 300 years vs 1 second.

the appendix for the remaining materials (see also table 3.1). For a brief overview the mastercurves of all viscoelastic materials treated in this work by relaxation testing are given in figure 3.13. Note the differences in relaxation behaviour concerning extension and position of the glass-transition region.

3.2.3 Comparison to Frequency Method

As has already been mentioned it is also possible to determine rate-dependent material properties by a measurement technique based on a frequency controlled drive as there are DMA or rheometry. In our case this has been necessary for the softer, silicone-based materials which did not produce meaningful results in relaxation (cf. appendix B.5).

Frequency-based techniques have the great advantage that the measurements can be carried out within minutes rather than days as is the case for the relaxation tests but for reasons of discrepancies between the methods [91] one has so far opted for the relaxation test results for FE-input. This relaxation test is considered to provide the correct material description, as it evaluates material viscosity over one hour, which is the same order of magnitude on a time scale as for the thermal cycle test itself.

Still the frequency-based method gives a qualitative impression how the rate-dependence changes with temperature (i.e. how pronounced it is at all) and where e.g. the glass-transition temperature is. For this reason the method came into use for each material used in this work as preliminary examination.

The frequency based method hinges on the fact that if a viscoelastic material is subjected to an enforced oscillation, the complex modulus $\underline{E}(\omega) = E'(\omega) + iE''(\omega)$ of the material is frequency-dependent. We apply a the drive, where as usual t' is the pseudo-time

$$\varepsilon(t') = \varepsilon e^{i\omega t'} \tag{3.62}$$

to the viscoelastic material that is characterised by

$$R(t') = \sum_{k} E_k e^{-\frac{t'}{\tau_k}}$$
 (3.63)

and take the constitutive equation 3.47 to evaluate the stress response of the system:

$$\sigma(t') = \int_0^t dt \sum_k E_k e^{-\frac{t'-t}{\tau_k}} \varepsilon(i\omega) e^{i\omega t}.$$
 (3.64)

Straightforward integration yields finally

$$\sigma(t') = \sum_{k} \left(E_k \frac{\omega^2 \tau_k^2}{1 + \omega^2 \tau_k^2} + i E_k \frac{\omega \tau_k}{1 + \omega^2 \tau_k^2} \right) \left(\varepsilon e^{i\omega t'} - \varepsilon e^{-\frac{t'}{\tau_k}} \right), \tag{3.65}$$

where the left brackets signify the complex, frequency-dependent modulus. With the first term on the right we retrieve the oscillation whereas the second term is just a decaying exponential representing a tune-in behaviour and can therefore be neglected for our purposes. Consequently for large t

$$\sigma(t') = \varepsilon e^{i\omega t'} (E'(\omega) + iE''(\omega)) = |\underline{E}(\omega)| e^{i\omega t + i\varphi} \qquad \text{where} \qquad \varphi = \arctan \frac{E''(\omega)}{E'(\omega)} \quad (3.66)$$

with

$$E'(\omega) = \sum_{k} E_k \frac{\omega^2 \tau_k^2}{1 + \omega^2 \tau_k^2} \quad \text{and} \quad E''(\omega) = \sum_{k} E_k \frac{\omega \tau_k}{1 + \omega^2 \tau_k^2}. \tag{3.67}$$

The interesting thing now is that if $E'(\omega)$ is measured by DMA or rheometry then the above equation can be used to fit a mastercurve on a frequency-scale. The mastercurve is constructed analogously to the one on the time-scale by a frequency shift function $a_{\omega}(T)$. The Prony times and coefficients remain the same. So we compare

$$E(t') = \sum_{k=1}^{m} E_i e^{-\frac{t'}{\tau_k}} + E_{\infty}$$
 (3.68)

$$E(f') = \sum_{i=k}^{m} E_i \frac{(2\pi f' \tau_k)^2}{1 + (2\pi f' \tau_k)^2} + E_{\infty}.$$
 (3.69)

where $f' = \frac{\omega}{2\pi} a_f(T)$ and $t' = t a_t(T)$ with $\lg a_f = -\lg a_t$. For the frequency domain E_{∞} is assumed for the static limit f = 0.

The storage modulus $E'(\omega)$ of the underfill of the last section was now measured with a rheometre. The result is to be seen in figure 3.14.

The corresponding frequency-shifted curves is depicted in figure 3.15. For comparison to relaxation data the mastercurve of figure 3.10 is also depicted. It has been transformed according to $E(t') \to G(t') \to G(t')$, $T_{ref} = 30 \, ^{o}C \to T_{ref} = 100 \, ^{o}C$ and $\lg a_f = -\lg a_t$ by the above equations.

One notices that the rate-dependence extends over a larger time or frequency interval for the frequency method. For obvious reasons this fact must manifest itself also in the shift-function in figure 3.16. Worrying is the frequency interval which comprises sixteen orders of magnitude in frequency (and time) compared to eight for the relaxation test. Apparently the theoretical equivalence of relaxation processes measured at frequencies (around $f \leq 10~Hz \leftrightarrow t \geq 0.1s$) and relaxation times of $t \approx 1000~s$, i.e. over four orders of magnitude seems less obvious in praxi. For lower frequencies the accordance of the curves is therefore better, although the measurement inaccuracies are higher in this domain. However, one should not forget that manual shifting of the curves introduces some degree of subjectiveness.

So assuming correct measurement and time-temperature shifting the outcome seems to depend on the time scale used for the measurement. Preference should therefore be given to the relaxation test data when simulation a thermal cycle experiment. Relaxation processes are then measured on the same time scale as used for lifetime evaluation.

Still, glass-transition zone and extremal values are comparable to the ones obtained by the relaxation test. Assuming correct measurement, the frequency based result data should still be viable for the simulation of short-term behaviour, let alone for a qualitative check for viscoelasticity of a new material in general.

It may be furthermore speculated if the assumptions of thermo-rheological simplicity and viscoelasticity do not become (at best) vague for an extrapolation on a scale where the bottom end is marked by the big bang itself. Still extrapolations of this kind are found

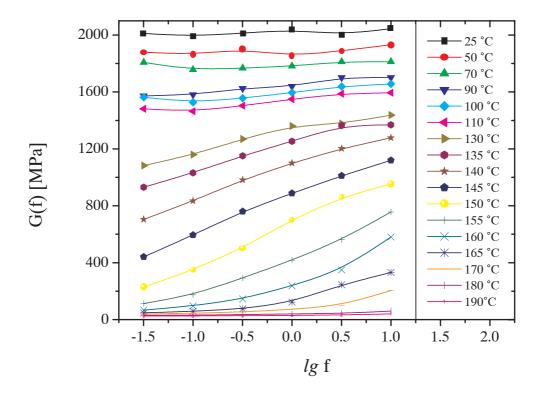


Figure 3.14. Measured rheometer data of underfill.

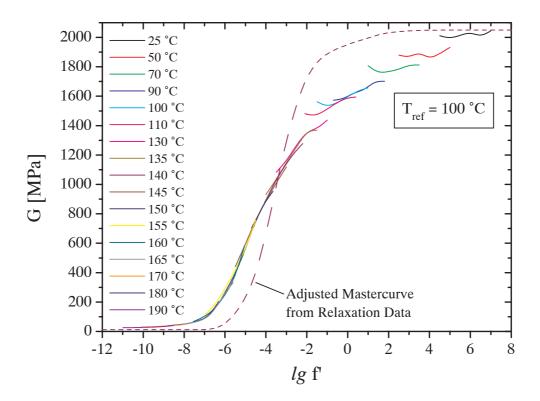


Figure 3.15. Temperature-frequency shifted data. Note the deviation from relaxation data.

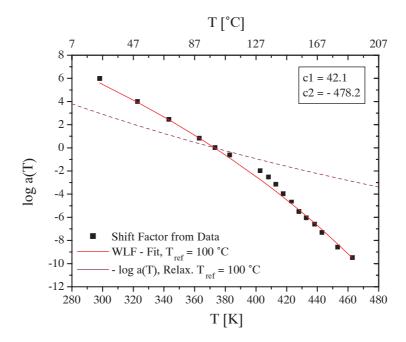


Figure 3.16. WLF shift function for the above mastercurve. Again a pronounced deviation from relaxation data is found.

in literature (10^{16} s, [93]) (Palaeozoic) and nicer (10^{50} s, [31])(!) and are used for lifetime predictions.

At any rate: Further experimental investigation and data is needed for comparison of the two methods for a – if possible – general verdict.

3.2.4 Numerical Implementation of Viscoelasticity

The calculation of the viscoelastic strain increment is again performed by a subroutine. This subroutine does all the logic starting from calculating the thermal strain increment as well as shifting the time according to the WLF-function and the summation of the Prony-series of both shear and bulk modulus. At the end of the increment the full tensor is again assembled as for the viscoplastic case.

To this end a Fortran subroutine which already exists (UsrViscEl.F) and is foreseen as Ansys user-programmable feature is customized to our needs. Newly implemented was the WLF-shift function and a different concept for temperature-dependent CTE-input. Therefore the input variables on the tb, evisc-command given in the Ansys theory manual [57] have been modified since the number of overall variables is limited. The new relationship becomes clear from the example input-file given in the next section.

The routine demands a normalised shear g(t) and bulk k(t) Prony-series. Therefore first the above indicated conversion of E(t) to G(t) and K(t) has to be made. The relaxation times may be input as they are, but the Prony coefficients need a normalisation according

to:

$$g(t) = \sum_{i=1}^{m} g_i e^{-\frac{\xi(t)}{\tau_i}},$$
(3.70)

$$g_i = \frac{G_i}{G_0 - G_\infty}$$
 with $\sum_{i=1}^m g_i = 1,$ (3.71)

k(t) is treated accordingly if needed. The routine allows input of ten Maxwell-elements which is just about sufficient to describe the polymers of interest in this work.

3.2.5 Ansys Data File for Underfill

After definition of a viscoelastic material by tb,evisc,# the subroutine is called through the input tbda,5,20. The remaining input is the WLF-coefficients of equation 3.58, then the CTEs which need to be specified in ascending order of temperature where $T_1 < T_{min}, \cdots, T_5 > T_{max}$ must be fulfilled. The CTE is then linearly interpolated. It follows the asymptotic values for the shear and bulk modulus and the Prony coefficients and times for the shear modulus. Further details can be found in the Ansys-manuals.

```
!-----
!--viscoelastic constants input for usrve5x.f
!--for underfill ------
tb,evisc,mat_uf
                 ! initialize
tbda, 1, 28.56
                 ! wlf c1
tbda, 2, 778.84
                 ! wlf c2
tbda, 4, 303
                 ! wlf tref
tbda, 5, 20
                 ! function key, must be 20
!--temperature and cte input-----
!- follows 5 temp in ascending order covering t-range of simulation
tbda, 26, 210, 273, 393, 413, 440
!- follows 5 corresponding cte values
tbda, 36, 44.4e-6, 44.4e-6, 133.0e-6, 133.0e-6
!--prony setup------
tbda, 46, 2071.15
                 ! G0
tbda, 47, 11.6768
                 ! Ginf
tbda, 48, 4487.5
                ! K0
tbda, 49, 4487.5
                ! Kinf
tbda, 50, 10
                 ! # g
! -- prony coeff shear-----
tbda, 51, 0.0043080, 0.0257507, 0.0277004, 0.0318087, 0.1885794
tbda, 56, 0.3006677, 0.2617653, 0.0582660, 0.0657374, 0.0354158
! -- prony times shear-----
tbda, 61, 0.0158398, 0.6288024, 12.542844, 198.67980, 3082.6693
tbda, 66, 30321.403, 171099.06, 883451.51, 3.13087e6, 9.94582e6
!-- end of underfill viscoelastic data input-----
! an effective nu = 0.3 has been used for data conversion
```

3.3 Characterisation of Thermally Conductive Gap Fillers (Foils)

Another type of materials used as thermal interface need to be characterised (see figure 3.17 below). The materials used have been described in detail in section 2.1.1. But it was difficult to determine their material properties with one of the previously described methods due to the crumbly, plasticine-like make-up of the silicone-based foil (see figure 3.17 (a) below) and the paper-like nature of the carbon-foil (b). Fortunately the manufacturer did provide material data as far as CTE and material composition was concerned. No viscoelasticity was assumed for either material, since the data-sheet for the carbon foil stated it and silicone in bulk shape (as cured adhesive) did not display significant rate-dependence (see appendix B.5).

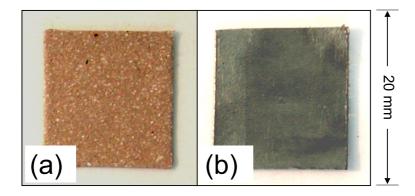


Figure 3.17. Examples of some comercially available gap-fillers. Of the five ones tested only the flexible foil (a) and the carbon foil (b) were characterized and came into use in the experiment.

Since neither of the foils could be fixed without damage by a tension testing machine, the elastic modulus had to be measured by a different technique. The modulus could be measured in compression, as both foils are comparatively compliant to deform already under small forces (see figure 3.18).

A force was applied on a die of specified size $(10 \times 10 \ mm^2)$ which compressed the foil. Through a hole in the foil and the stator plate opposite the die the displacement of the die and hence the thickness of the foil could be measured very accurately by means of a LVDT (Linear Variable Displacement Transducer). An apparatus similar to the one depicted in figure 4.9 later in this work was used for this procedure.

From this data which is graphed in figure 3.18 the elastic modulus can easily be calculated. As the graphs are curved, a linear approximation in the region closest to the envisaged work point were used and the elastic modulus was obtained by the slope of the straight line. The force $F_N = 10 N$ is the normal force needed to assure thermal contact specified by the manufacturer. This value is slightly above the lower limit.

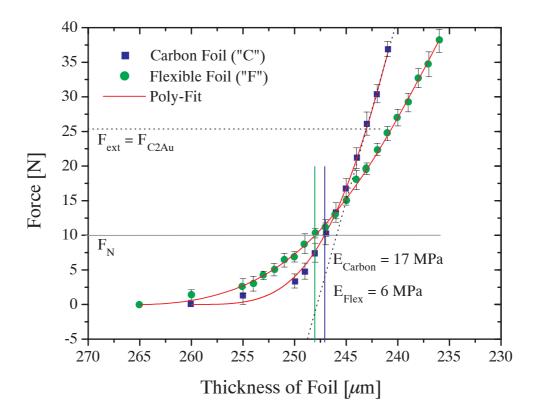


Figure 3.18. Characteristic curves of carbon foil (code 'C') and flexible foil (code 'F'). The elastic modulus has been determined by taking the gradient in the work point determined by $F_{ext} = F_{C2Au}$ (see table 5.2 and figure 5.1) of the curves measured in compression.

3.3.1 Ansys Data Files for Gap-Fillers

The data for CTE were not measured but provided by the manufacturer. As for Poisson's ratio the value for the carbon foil was provided, whereas for the silicone (a usual value) of $\nu \approx 0.4$ was assumed.

The measured E-modulus for the flexible, silicone-based gap filler produced similar values as the silicone based adhesive in section B.5. This underpins the quality of the measurement.

Chapter 4

Finite Element Modelling, Consistency Check and Experimental Design

The objective of this chapter is to show the creation of the finite element model which is to mirror the flip-chip assembly with attached heat spreader. For reasons of universality the model is devised in a parametric (scalable) form which furthermore allows to combine modular entities and merge them into a large FE-model. This model is optimized to strike a balance between speed and accuracy and is checked for numerical stability and convergence as to the evaluation of the creep strains which do serve as failure criterion. Some special features like contact mode simulation are highlighted and commented on. As the FE-model is parametric, it can easily be adjusted to any real test assembly at a later stage.

Then the model is checked for consistency with experimental tests by comparing the macroscopic behaviour of the flip-chip on board under externally applied loads. Quantities like displacement of the board and deflection of the die are accessible to measurement. A special apparatus was built for that purpose. Thereby it is clarified which influences will act upon a chip in such a configuration and how these constraints of different kind and magnitude are best applied and varied within a range of technological or practical interest and physical limit.

The organic board was found to display viscoelastic and orthotropic behaviour, material properties which can currently not be treated simultaneously by the FE-tools in use. Viscoelasticity was eventually given preference over orthotropism, after accordance between experimental tests and simulation was obtained by the introduction of a calibration factor for the set of material data.

The considerations made in the previous sections are to manifest themselves in the construction of a test-specimen which is to furnish the experimental correlation to computational lifetime prediction.

So in the remainder of this chapter the layout of the daisy-chained chip and board is given to explain how bump failure is to be detected. Finally, the assembly process of the test-specimen is explained and the problem of voids in solder bumps after reflow is addressed. Technological difficulties which were surmounted are pointed out.

4.1 Universal FE-Modelling: The Modular-Parametric Approach

As has been motivated we need to construct a finite element model which has to meet demands of flexibility concerning size, material and load configuration.

The main geometric features as the size and shape of the individual components, their position, their connectivity (merged or sliding contact) ought to be variable. The same is true for the mesh-related properties of each part of the model as mesh-density, mesh type and application of constraints. The incorporation of modules created by other CAD-Tools¹ could become necessary. The inclusion of required constitutive equations has already been explained in the last chapter.

This are prerequisites for a comprehensive model-parameter study of the intended range and scope allowing comparability of the results and an automatic model generation.

Another important point is computational efficiency. This implies that the model be as simple as possible, yet accurate. The question of how much detail is necessary for stable results concerning our objective, the evaluation of the failure criterion in the solder bump, needs answering. In order to determine for example the lowest uncritical (result-invariant that is) mesh-density one has to be able to study the effect of this parameter. One does not want the result to depend on numerical issues, on the other hand there is little point in wasting computer resources. It has turned out that this FE-related parameter optimization helped much reduce the complexity and hence the number of nodes in the model.

This so-called *modular-parametric* approach to solve this problem is presented below. As a tool the commercial code *Ansys* has been used. It is believed that with this approach it is generally possible to facilitate accelerated model generation and verification for a large class of electronic components (or microsystems [94]) due to its universality.

4.1.1 Philosophy of Parametric Modelling in *Ansys*: Combination and Meshing of Standard Modules

In order to handle the different configurations assuring at the same time an economic and smart management of elements the parametric approach looks as follows:

All relevant size and shape information is supplied to the program (Ansys, Release 5.7) via a ASCII file. Here all parameters are identified and mesh definitions given. In a similar vein material data is read into the program which has been customized beforehand to provide the required material routines by compiling and linking the respective Fortran subroutines [72].

The geometry is set up according to a modular system, i.e. each geometric FE-entity (for example a bump or a chip) is modelled separately and saved to disk. At a later stage it can be read into the model again at the location where it is needed. This procedure has the great advantage that one deals with each part at a time and one may create a library

¹The shape of the bump can also be crated by e.g. Surface-Evolver, (a program which calculates the shape according to the surface-tension of the material) and be incorporated.

of e.g. bumps (see figure 4.1). This is especially practical if these modular subparts require particular devotion as in this study the make-up of the bumps. So meshing operations can be tested for the individual modules first before they are integral part of a complex model.

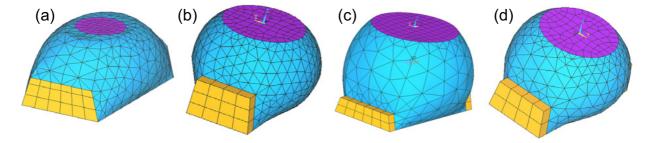


Figure 4.1. Some bump shapes to be found in flip-chip technology. The one labelled (a) is the focus of this work (for dimensions refer to figure 4.28), the others represent time-honoured shapes. This picture illustrates also the capacity of parametric bump-modelling by alteration of only a few size-parameters with subsequent automatic generation of bump-geometry.

It has been acknowledged (see e.g. [45]) that meshing a flip-chip assembly is challenging in terms of economic management of elements and may require some tricks. This is mainly due to the fact that very small, volume-like regions of interest with non-trivial topology (here: the bumps) are to be combined with large, area-like regions which require less attention and are usually of simple topology (the die). This raises the question of which type of element is expedient for the individual parts taking into account the need for automatic mesh generation. This latter boundary conditions entails that the model be continuous and accurate enough for the operations to work flawlessly.

To assure this all submodules were of simple shape (e.g. brick-shape) within which the non-trivial topological structure is embedded. At the location within the larger entity the submodules are to be incorporated into a hole of the same size has to be cut out (by Boolean operations) to create space for the module to fit in neatly. For automatic meshing the model is 'glued' together² at the boundaries to form one single continuous model.

As a rule brick-shaped (HEX) elements are better suited and more economic than tetrahedrons (TET-elements) for layered structures of simple topology, whereas TETs should be used for volume-like structures and have the advantage that volumes of any topology can be meshed. A continuous mesh transition can be facilitated by pyramid (PYR) elements when HEX and TETs have already been crated. For largest flexibility and automatic mesh generation one proceeds as depicted in figure 4.2: The bump geometry is modelled (a) and clad into a module or box of standard dimensions (b). The second standard module is represented by the assembly's layers (c) in which the bump is to be incorporated. At any desired position in the xy-plane one or more bumps can be inserted (arrows). Therefore a volume of the size of the module has to be cut from the layers at the specified future location of the bump (d). The standard bump module is inserted (e) and merged with the remaining model (f) to form a continuous model. Then the layered structures of simple

 $^{^{2}}Ansys$ VGLUE command.

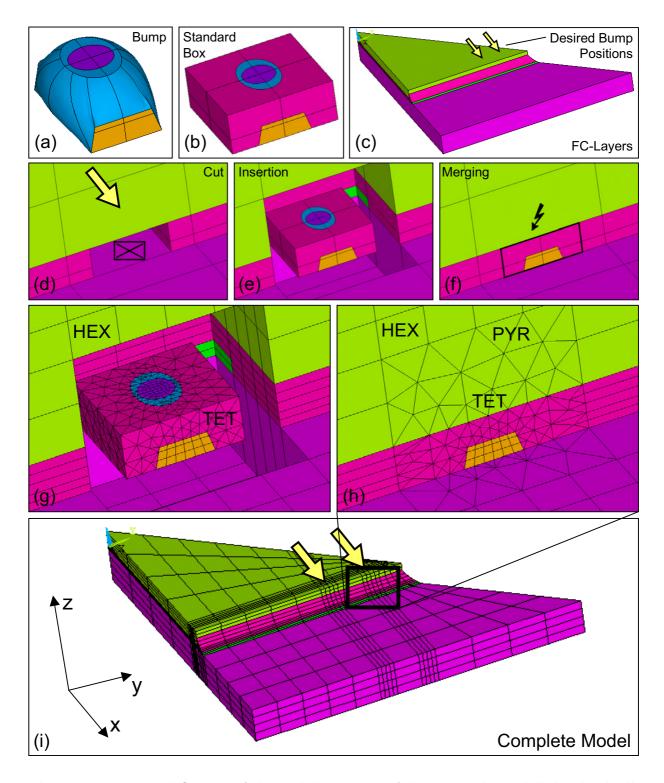


Figure 4.2. Exemplification of the modular system: A bump may be modelled individually (a), clad into a brick-shaped box of standardized (modular) dimensions and saved to disk (b). At the desired positions (shown for the case of two bumps (arrows)) of the modelled flip-chip assembly layers (c) a standard box is cut out (d), the bump is inserted (e) and topologically merged (f) with the model. The bump module is meshed after the main parts only (g) and remaining space is automatically filled with elements (h) to accurately integrate it to form the complete model (i).

topology are HEX-meshed first, followed by the non-trivial topological volumes of bump and box. Here a TET-mesh is used where appropriate (g). Now a concentric box enclosing the submodule from all sides is automatically filled with TETs (h). PYRs are formed at the interface to the HEX-meshed layered structures. This can also be seen in figure 4.3 bottom left.

This procedure has another great advantage: The submodule is integral part of the model and not just 'sewed' into it (cf. [10,39]) by additional constraint equations³, which is liable to convergence problems due to an often ill-conditioned matrix.

4.1.2 Model for Flip-Chip with Attached Heat-Spreader: Loads, Constraints and Special Features

A FE-model for an unconstrained flip-chip on board may, within the described concept, look like the one in figure 4.2. But for the FE-representation of a flip-chip assembly with reverse side cooling one needs to add the thermal interface material and incorporate mechanical boundary conditions (e.g. a fixation) and loads (e.g. a force and displacement) as they are to be applied to the chip as in figure 2.2. This model is depicted in figure 4.3, where the colors signify the different materials as explained in table 4.1.

Element	Specifications	for	individual	Materials
		101	mairiada	TITATO

Item	Code	Colour	Material	Law	Element-Type	Feature
Plate	pl	lt. blue	Aluminium	el	S186	
Board	bd	magenta	Fibre-Epoxy	ve	V89	
Chip	ch	lt. green	Silicon	el	S186/187, T174	Target
Interface	ad	turquoise	diverse	el, ve	S186, V89, C173	Contact
Underfill	uf	red	Epoxy, filled	ve	V89	
Soldermask	sm	green	Epoxy	ve	V89	
Bump	bp	blue	eut. SnPb	vp	S187, C173	Contact
Footprint	fp	yellow	Copper	pl	S186	
UBM	um	violet	Nickel	pl	S186	
Screw	sc	dk. blue	Steel	pl	S186	
Spacer	sp	dk. blue	Steel	pl	S186	Birth/Death

Table 4.1. The materials in their FE-representation: The colour code refers to all FE-figures in this work as does the abbreviation for all formulae. For the material property item we assign el – elastic, vp – visco-plastic, ve – visco-elastic and pl - plastic. The element types which support these material laws are given in Ansys-nomenclature (see [57]) and are quadratic elements in their HEX or TET form.

The model in figure 4.3 exhibits octant symmetry. Via symmetry boundary conditions, which constrain all displacements orthogonal to the edges, the whole assembly is (numerically) complemented to a full square.

³e.g. by CEINTF command

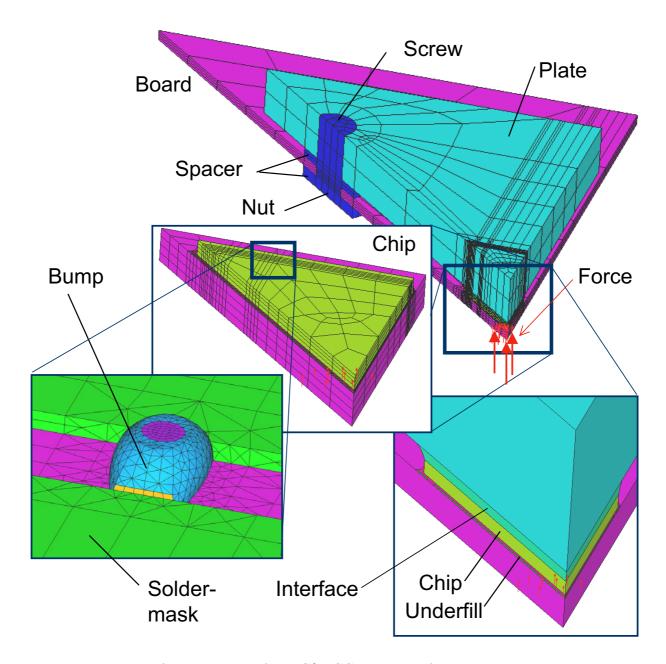


Figure 4.3. The full FE-Model for FC&RSC, regions of equal material have the same colours. Due to octant symmetry of the assembly only one eighth needs to be modelled. The details inside the zoomed-out boxes show (from right to left): The interface region layers, the meshed chip and a bump. Note again the mesh-transition from TET to HEX via PYR-elements around the bump, which is thus incorporated as a modular entity into the chip without difficulty. The red arrows symbolize the force acting upon the chip from below.

A cylindrically shaped meshed region is intended to serve as area for the application of the external force. Hereby, the force acts as a pressure (red arrows), which is advantageous since by this means the force acts like a load homogeneously distributed over the specified area. In order to hold the model fixed in three dimensional space the nodes of the area just opposite the force application area on top of the plate is fixed in the out-of-plane direction.

In simulating the different configurations one has to take into account the assembly process and with it the correct order of the application of the individual loads which precede thermal cycling. So it is e.g. necessary to leave the contact between spacer and nut undefined as long as this joint does not exist, i.e. as long as the nut is not tightened. This requires an element 'birth and death'-capacity.

In praxi this means that underfill and adhesive are cured before a spacer of given thickness is inserted into the gap between plate and board. Only then the pressure is applied and the nut tightened, i.e. the contact defined and the elements of all regions have to be active and merged at the nodes – 'alive' as it is called in *Ansys*. This capability of the elements allows to build the model in its most comprehensive shape right from the beginning, but to deactivate elements which are not needed at certain load steps. In the same vein they can be brought back to life when it is their turn.

The kind of thermal interface material poses an other constraint to come into effect. An adhesive, as long as the interface area is intact (i.e. no cracks or delamination), may doubtlessly be modelled as two merged regions and a continuous mesh. In the event of a gap filler though this is not the case. For this situation the chip-foil interface is layouted as a contact-target joint. Sliding contact with no friction is used here which is certainly a good approximation: The chip does not move laterally, only in z-direction. In this case it is the main task of the interface to allow a gap between the two regions⁴. This approach can also be used to include the phenomenon of delamination (e.g. at the bump) into the model if needed.

A word should be said to dimensional reduction of an FE-model, as proposed by some authors [33], could not be considered for our purposes. The bumps are at positions where they can only be taken into account by an octant model. Further, as shown by e.g. [95], only 3D models can reproduce the true states of stress and strain to the degree of required sensitivity.

4.1.3 Averaging Region for Creep Strain

For accumulating the failure criterion it is necessary to average the creep strain over a certain volume in the bump as the value of one single node or a path would not give a representative result due to local variations of the creep strain. In a 3D-model one has to take into account a the 3D distribution of the strain fields: An averaging region should include the highly strained part in which failure does occur i.e. the elements below the pad.

Due to the fact that TET-elements do not fill a volume in a regular and reproducible pattern as HEX-elements would do, a volume adjustable in size and location inside the solder just

⁴This is also depicted in figure 5.36 where the simulation shows a evolving gap between chip at thermal interface at low temperatures.

below the pad has been created. This allows averaging over exactly the same volume for each bump irrespective of the shape of the elements and hence furnish comparable results. This feature is depicted in figure 4.4. The averaging itself is done by using Ansys element table operations⁵.

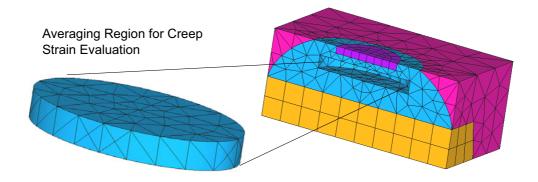


Figure 4.4. The (adjustable) averaging region for the creep strain.

Important is the location of the averaging region. As a guideline it should be at one element's distance from a material interface [75]. This avoids influences of numerical artifacts like interpolations or singularities which exist at material boundaries and do not reflect correct values [10,38]. It can be shown that very close to a sharp edge (as would be found at the UBM-Solder interface) the creep strain depends on the creep limit (see next section). The averaging volume depicted fulfills these criteria and is located close to the pad where the cracks develop and the creep strains reach a local maximum in a band-shaped structure.

4.2 Guidelines for FE-Model Optimization: The Influence of Critical Parameters

As been mentioned before the final results should not depend on *FE-related parameters*. These shall be understood as all parameters which are of purely numerical nature (e.g. mesh-density) and do not alter the geometric appearance of the model. There will usually be a limit value of the respective parameter where the solution converges, i.e. where the calculated creep strains do not depend on the value of the parameter any more. This value has to be determined for each so-called 'critical' parameter. A list of those is given in the first half of table 4.2.

There are other - model-related parameters which represent the extent of geometric detail down to which the solution is convergent. Desirable is a model which can renounce a lot of detail requiring in detail only the region of interest as is in our case the solder bump for the correct evaluation of creep strain. They are listed in the second half of table 4.2.

 $^{^5} Ansys$ ETABLE-Command

In order to determine the influence of the individual parameters the parametric model described above has been altered accordingly. As load case a full thermal cycle (as further carried out in section 5.1) is used for the comprehensive FE-model (figure 4.3) to yield results apt for quantitative comparison. For some parameter studies other (less complex) models have been used (see appendix C). They underwent a ramped thermal load (160 $^{o}C \rightarrow 25$ ^{o}C within 5 min.), which is the first load step for all configurations as it simulates the curing of the underfill.

In the following the individual points are illuminated, where some of them may be taken as guidelines for FE-modelling of flip-chip devices evaluating creep strain in solder bumps. But some parameters may depend on the employed materials. Still the presented approach may provide some guidance, as these parameters will have to be checked in any case to calibrate the model.

Parameter (FE-related) Influence Guideline Description 1 Simulation Tool N Abagus to Ansys? Y 2 Element Type (Solder) HEX to TET? Use TET Y 3 Stable Solution? Mesh-Density ∠ Lower Limit 4 Creep Rate (Law) Force - driven? Y Stable Solution? Y 5 Creep Limit Control ≯ Upper Limit Parameter (Model-related) Description Influence Guideline 6 Copper traces Necessary? Ν Leave out 7 External Force Model or BC? Ν Use BC for F8 Ν Bump Neighbourhood # of Bumps? One Bump o.k.

Influence of FE-Parameters on Creep Strain & Guidelines

Table 4.2. The label 'No Effect' signifies a deviation of less that one percent. For details refer to the text. The results are given graphically in figure 4.7

Necessary?

Creep Strain?

DNP?

N

Y

Y

Leave out

Use Outer Bump

Large Pad & Gap

1. Influence of Simulation Tool:

Passivation Layer

Bump Position

Bump Shape

9

10

In the course of the model generation constitutive laws for secondary creep and viscoelasticity had been implemented in *Abaqus* and had to be transferred to *Ansys*. For an equivalence check a three-dimensional chip model which simulated one bump in a 'slice' (see appendix C.1.4) was created which incorporates all characteristic features to check our simulations with. Both tools produced identical results (see appendix C.1.1). *Ansys* was finally chosen due to better parametric modelling capabilities.

2. Influence of Element Type:

For its non-trivial topology the bump can only be meshed automatically with TETelements. The creep strains of the bump may show a sensitivity towards element shape and density. This must be excluded since creep strain serves as failure criterion. To check this a model was created analogous to the one described in point (1) save the fact that there is a second bump which is this time meshed with TET-elements (see appendix C.1.2).

The result is that a TET-mesh produces identical results at the expense of more elements⁶. A HEX-mesh, however, would be the more economic solution. Differences are to be seen at the edges which shows a numerical difference (same creep limit). Fortunately these zones are not averaged over when evaluating creep strain. So TET-elements were finally chosen.

3. Influence of Mesh-Density:

In order to determine the influence of the bump mesh-density on the creep strain the bump was meshed as described in figure 4.5 (left). (The individual meshes are depicted in appendix C.1.3.)

It is seen that from a lower limit density the result converges towards a stable value for equivalent creep strain. This density has been used (> 1000 Elements/Bump-Volume).

The influence of the mesh density of the main model (chip and board) was checked, too. No significant effect on either creep strain ($\Delta \bar{\varepsilon} < 0.0001$) or deflection of the chip ($\Delta k < 1\%$) was detected. A mesh as is printed in figure 4.3 has been found suitable.

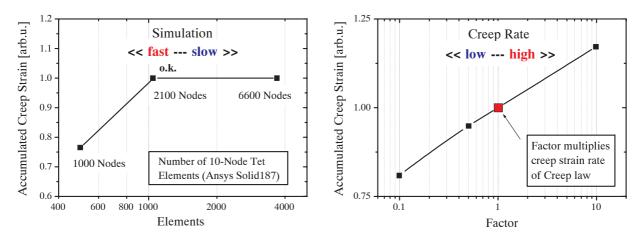


Figure 4.5. Left: Influence of the bump mesh-density on equivalent creep strain $\bar{\varepsilon}^{cr}(t,T)$. The number of nodes and elements refer to solder material only. The creep strain is normalized to the value for the stable limit. The arrows show the conflicting tendencies. Right: Influence of creep-rate on creep strain. The factor multiplies the creep-rate given in equation 3.7.

4. Influence of Creep Rate:

An other issue is the creep rate. Although there are many indications that the flip-chip assembly is mainly displacement-driven (i.e. the bump itself does not contribute to the stiffness but has to comply with the applied drive [70]). This could mean that the creep rate or law is not as important since the solder has to comply to the imposed deformation.

 $^{^6}$ This corresponds to a factor four in elements and a factor two in nodes. Here, TET-elements have 10 nodes, whereas HEX do have 20.

The results in figure 4.5 (right) show that this is not so. The tested variations of creep rate display a pronounced deviation from the originally resulting accumulated creep strain in magnitude and structure. This may be on account of a local interaction between the solder and its surrounding materials like underfill and soldermask as a result of the elastic energy still stored in the assembly, since the global curvature is not affected. Obviously this behaviour will also depend on the solder material which the creep law is characteristic of.

5. Influence of Creep Limit Control (Creep Criterion):

Ansys allows to specify a creep criterion c_{lmt} which controls the maximum creep strain c_{max} per iteration and per integration point. It is defined as upper limit for the creep ratio

$$c_{lmt} \ge c_{max} := \max \frac{\Delta \bar{\varepsilon}^{cr}}{\bar{\varepsilon}^{tm}} \bigg|_{t=t_n}$$
 (Ansys), (4.1)

where $\Delta \bar{\varepsilon}^{cr}$ is the equivalent creep strain increment at time $t = t_n$ and $\bar{\varepsilon}^{tm}$ is the equivalent strain of a modified total strain tensor:

$$\varepsilon_{ij}^{tm}\big|_{t=t_n} = \varepsilon_{ij}^{tot}\big|_{t=t_n} - \varepsilon_{ij}^{th}\big|_{t=t_n} - \varepsilon_{ij}^{cr}\big|_{t=t_{n-1}}.$$
(4.2)

As usual equivalent quantities are labelled with a bar. This criterion is different from the one used by $Abaqus^7$ which reads

$$c_{max} := \max \left\{ \Delta \bar{\varepsilon}^{cr} |_{t=t_n} - \Delta \bar{\varepsilon}^{cr} |_{t=t_{n-1}} \right\}$$
 (Abaqus), (4.3)

where in either case

$$\Delta \bar{\varepsilon}_n = \int_{t_{n-1}}^{t_n} dt \ \dot{\bar{\varepsilon}}_{(t)}. \tag{4.4}$$

There is no obvious relationship between these two criteria which made the investigation that follows necessary. Simulations have been run for different values of the creep-criterion⁸ where implicit time-integration was employed. This is shown in the graph of figure 4.6.

If no creep limit is specified, the creep ratio may take on any value which results in a overestimation of creep strain despite the implicit time integration scheme which always assures a numerically stable solution (backward Euler algorithm). As a creep limit is given, the creep strain converges to a stable value. As a consequence the number of substeps increases – for small values of c_{lmt} anti-proportionally since the limit is reached in each substep. It is instructive to see that this influence is stronger for the elements at corners than in the centre (averaging region). From the graph an uncritical value of $c_{lmt} = 10$ can be assumed.

6. Influence of Copper Traces:

It would have made the model much more complicated to model the wiring on the board. It has been found sufficient just to model the footprint below the solder, the creep strains

⁷ Abagus-command cetol=0.0005

⁸ Ansys-command cutcontrol, crplimit, value, implicit

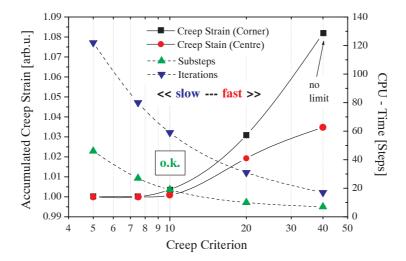


Figure 4.6. Influence of creep limit control on failure criterion accumulated equivalent creep strain. The rightmost value is extrapolated since no creep limit was specified for that case.

do not depend on the size of the fan-out ('slice'-model). This largely reduces model complexity.

The whole of the copper on the board may still influence the overall stiffness of the board. Measurements⁹ have shown no difference between a board with fan-out and one which had the fan-out removed. This is due to the fact that we deal with only very few tracks on our PCB¹⁰ (printed circuit board). An effective board thickness and E-modulus do account for this.

7. Influence of Application Mode of External Force:

The external force should be applied to the model as FE-load on a specified surface (see figure 4.3). In an experiment, however, this would require a stator to hold a spring etc. So in this respect it is worthwhile checking if the omission of such a stator in the FE-model has any influence on the result. No influence was found and so further simplification of the model was possible (cf. figure C.6).

8. Influence of Bump Neighbourhood (Number of Bumps in the Model):

Obviously it would greatly reduce CPU-time to have only a small number of bumps to model, since they represent the most element-consuming part. For this reason it had to be checked if it is immaterial for the result if only a small number e.g. two (separated) bumps are modelled or if the creep strain is affected by an adjacent bump. Therefore a chip was modelled with two adjacent bumps at the corner (see section C.1.6) and the remaining part of the soldermask 'channel' was filled with a large barrel-shaped bump.

The comparison with the chip with two separated bumps produced no difference. This

⁹As those described in section 4.3.1.

¹⁰Depicted in figure 4.25.

tendency is also stated in [10,39]. Therefore it was concluded that it is sufficient to model only two bumps at arbitrary positions. Apparently the stiffness of the assembly is large enough to override any effect of the bumps. This may be different for an other material combination though.

9. Influence of Passivation Layer (Polyimide):

The active chip surface is protected by a passivation (polyimide) layer of 5 μm thickness. It was therefore checked if any change in the result would occur if it was missed out.

For this simulation the UBM was taken as thick as the passivation layer (5 μm instead of 8 μm) which makes the solder gap between pad and footprint $\approx 6\%$ larger. This causes the creep strains to decrease as seen in the corresponding bar in figure 4.7. A slightly greater value has been chosen to make up for the larger solder gap accordingly in that it can be assumed that there is no significant difference and that this polyimide layer can be omitted for our purposes. This furthermore illustrates the large influence of the solder gap width on creep strain. The model can be seen in the appendix C.1.7.

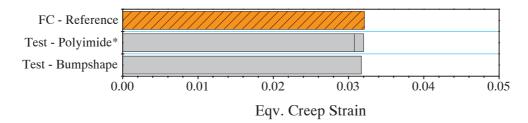


Figure 4.7. The influence of the model-parameters depicted. * The slightly smaller value is due to a slightly higher bump (see test). The strain has been adjusted accordingly. The abbreviations in brackets refer to table 5.2.

10. Influence of Bump Position and Distance to Neutral Point (DNP):

In some papers [96] the DNP is given as a parameter characteristic for flip-chip reliability. It states that usually the outermost bump experiences the largest creep strain and consequently fails first, a fact which is not necessarily true for a force-driven package like a CSP [97].

Here it could be verified that the outermost bump did indeed produce the largest strains (as will also be shown later in the results chapter). This means that it is sufficient to simulate bumps close to the corner at maximum distance to the neutral point.

11. Influence of bump shape:

One critical (set of) parameter(s) in the design process is surely the shape of the bump. This comprises not only absolute size, proportion and pitch but also pad diameter, footprint height, contact to soldermask etc. This topic is addressed in many papers and represents undoubtedly a point of interest [98,99].

The simulation tool presented above is able to model bumps of most shapes of interest in flip-chip technology. Some of them are presented in figure 4.1 (a-d). Obviously

combinatorially-many variations are thinkable and a parametric study focusing on bump shape is therefore beyond the scope of this work. Furthermore, experimental verification and analysis, which should always accompany a numerical assessment, are only carried out for the one set (a).

However, to show the influence of the bump shape on the numerical failure criterion a comparison between bump (a) and bump (b) has been made. They both exhibit the same gap $(47 \,\mu m)$ but differ in extension and pad diameter. Bump (b) yields slightly lower creep strain as depicted in figure 4.7, which is accredited to the larger pad. The lateral extension of the bump seems not relevant. Now our FE-model highlights all features necessary to evaluate flip-chip reverse side cooling under thermal and mechanical load. As it has been set up in parametric we can adjust it to any required geometric dimensions. This will be of interest in the next section.

4.3 Characteristic Behaviour under Thermal and Mechanical Loads in Experiment and Simulation

From the last section a FE-tool is now available that functions reliably and the results of which do not depend on FE-related parameters. We which details are necessary to obtain numerically correct results and can run our simulations in the shortest possible time. Furthermore we have recorded the material data and implemented the corresponding constitutive laws. The model is ready for a consistency check with some measured quantity.

The macroscopic response of the chip such as its curvature and displacement as a function of the applied loads is well suited for this check. Values of curvature (measured as deflection) and displacement can be obtained by simulation and are at the same time quantities which are accessible by measurement.

So in a next step we determine experimentally the characteristic behaviour of the flip-chip on board assembly for various relevant loading situations. A special apparatus was designed for that purpose which allows to measure displacement and deflection with a fixation as in the finite element model. The influence of the adhesive was also examined.

The resulting agreement of simulation and experiment on the macroscopic level are a prerequisite for the accurate evaluation of creep strain, an outcome which is more difficult to verify experimentally [63]. It also gives us an idea of a range of interesting or critical values for experimental adjustment: Interesting in the sense of getting a *significant* response,—critical in the sense of upper limits e.g. for die crack.

4.3.1 Response of Flip-Chip and Organic Board to external Load: Displacement and Deflection

First, the dependence of displacement and deflection (a measure for the curvature) on the external force is measured. To this end a small apparatus was built which permits controlled application of a force and simultaneous measurement of the displacement of the board with the chip mounted on it. This device is depicted schematically in figure 4.8 and

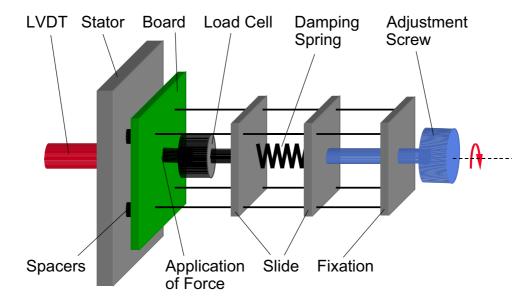


Figure 4.8. Schematic of apparatus used to determine force - displacement relationship.

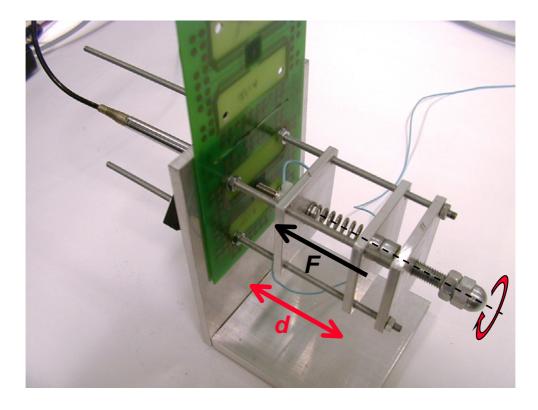


Figure 4.9. Photograph of the apparatus. On the left the LVDT can be seen.

physically in figure 4.9. To the very right a screw allows to compress a spring which is sandwiched between two plates which are guided by slides. In collinear arrangement the tension of the spring is transferred through a load cell to the rear side of the board. (The spring is only used to enable fine-tuning of the force.) The tip of the load cell is shaped to make a defined contact zone. The board is supported symmetrically at four points which form a square in the middle of which the chip is mounted. The distance from board to stator is adjusted with precision spacers. Now the force can be adjusted by turning the screw. As a result the board with the chip on it is pressed to the left, in z-direction. This is called the displacement d of the board. In some sense we are about to conduct a five-point bending test, the arrangement being reminiscent of the number five on the face of a die in a game of dice.

The displacement is measured by a linear variable displacement transducer (LVDT) which is also depicted on the photograph¹¹. This very accurate gauge¹² (accuracy $<\pm 1~\mu m$) touches with a needle the surface of the chip, where the tiny force used to keep up the contact is negligible. As a display only a commercially multi-meter was needed. The same applied for the load cell¹³ (accuracy $\pm 0.5~N$).

The result of this is seen in figure 4.10. The measurement was carried out for organic boards of thicknesses of $0.8 \ mm$ and $1.2 \ mm$. One notices, that the force-displacement relationship is completely linear at room temperature according to

$$d = pF + d_0, (4.5)$$

where p is the compliance of the respective board (thickness) and F the external force, d_0 represents the zero offset. The scatter around the origin reflects mainly the fact that the boards are warped over an area of $41 \times 41 \ mm^2$ (position of fixation screws) after reflow and underfilling, i.e. after two thermal processes above T_g . The compliance p is not affected hereby, as the measured values show hardly any scatter for it. Especially the thin board reveals a great deal of – in some cases even initial – unevenness. In such a case this warpage was gently corrected by bending the board until it was even again. Still a final warpage remains which is responsible for the – therefore intrinsic – deviation of $\delta d_0 = \pm 15 \ \mu m$ (thin board). This is not bad at all if one considers that we deal with a low-cost material.

Unfortunately these measurements could not be carried out at other temperatures due to specification limits of the (expensive) gauges. Due to the viscoelastic material properties of the organic board (cf. section B.2) the curves are expected show some relaxation at temperatures close to the glass transition temperature T_g as the material displays a rate dependence.

Then the curvature is measured as the difference in displacement in z-direction (orthogonal to the chip plane) of two points: the centre of the quadratic die and the corner (as e.g. depicted in figure 4.18). This quantity shall henceforth be referred to as the *deflection* k of the die, whereas the curvature $\kappa = 1/r$ is defined as the inverse radius (of curvature) at the centre of the die.

 $^{^{11}}$ This apparatus was also used to produce the curves in figure 3.18 by which the foils could be characterized.

 $^{^{12}\}mathrm{Type}$: Amos AWM-47-1.5 with amplifier Amos AE-2

 $^{^{13}}$ Type: Amos ALM-170

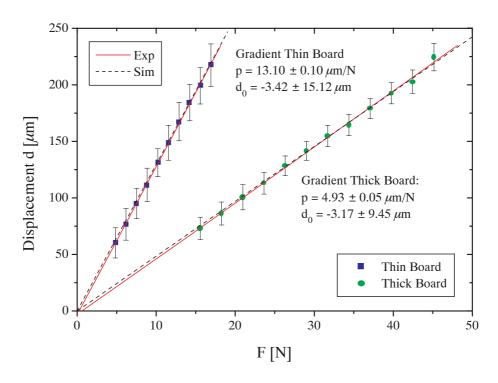


Figure 4.10. Experimental result for characteristic force F versus displacement $d = pF + d_0$ curve for thick and thin board. Warpage of the board causes an intrinsic inaccuracy of $\delta d_0 = \pm 15 \ \mu m$ for the thin and $\delta d_0 = \pm 10 \ \mu m$ for the thick board respectively.

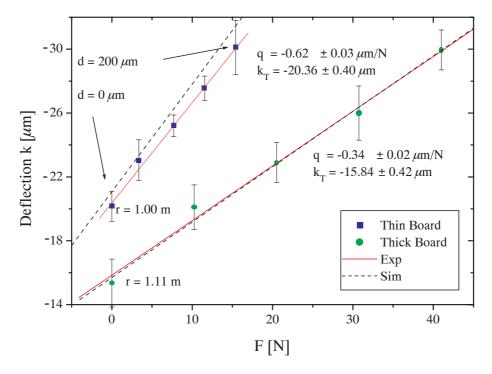


Figure 4.11. Characteristic curve force versus deflection $k = k_T + k_F$ with $k_F = qF$. The dotted curves represent the simulated result.

The deflection is a very accessible quantity and to a very good approximation proportional to the curvature for all values of force and temperature of interest in this work (see figure B.6 in the appendix).

$$k \sim \kappa = \frac{1}{r}.\tag{4.6}$$

The measurement¹⁴ of the deflection was performed using the same apparatus as depicted above only with the change that instead of the LVDT a curvature gauge was placed to scan the chip.

The best results¹⁵ were obtained using a profilometer¹⁶ which made scans of the chip across its diagonal with a position-sensitive precision probe. Its sub-micron resolution yielded smooth curves and allowed fast recording of data. The results are depicted in figure 4.11.

Again we find a linear relationship between force and deflection according to

$$k = k_T + k_F = k_T + qF,$$
 (4.7)

where as expected the chip exhibits an initial curvature k_T due to the thermal mismatch between chip and board. As the force F increases the deflection increases by a mechanically induced contribution $k_F = qF$, where q is the function gradient for the respective board thickness. The underfill stiffens the assembly to a degree that it communicates this mismatch. For the thick board the curvature is smaller since there is more board to resist bending.

Some words have to be said about the fixation of the board. The following type of fixation was found to come closest to the technological realization of flip-chip reverse side cooling and was therefore finally used to measure the characteristic curves: First a given value of force was adjusted, then the nuts were tightened. This assures that these fixations are stress free and serve only to hold the board parallel to the plate at the location of the screws. This turns out to be the most stable configuration and comes closest to the assembly process in a electronic device. Apart from that this has the immeasurable advantage that the nut joints – which are normally a non-trivial FE-issue – can be simulated as merged regions and no contact mode is necessary. (For alternatives see the comment in section 4.4.2 at the end of this chapter.)

Then, the dependence of the curvature of the chip on temperature is measured. The deflection as a function of T is measured by speckle interferometry [100]. The speckle pattern for the deformed chip is depicted in figure 4.12. One had to resort to this less accurate means since the described precise methods would not work in higher temperature environment as LVDT and load cell are not specified for it. So these measurements could only be carried out for the unconstrained flip chip, i.e. for $k = k_T(T)$.

The values for the deflection at the corner of the die were measured at various temperatures for various chips again for both board thicknesses and depicted in graph 4.13. Again the

 $^{^{14}}$ The results are based on measurements carried out on a number of samples > 20 and includes averaging over both diagonals. The difference does not exceed a value of $1 \mu m$.

¹⁵The values are in accordance with results gained by a laser scanner, but this method proved too time-consuming and had a lower resolution.

¹⁶Type: Perthometer PCV 350 with 59 cm cantilever

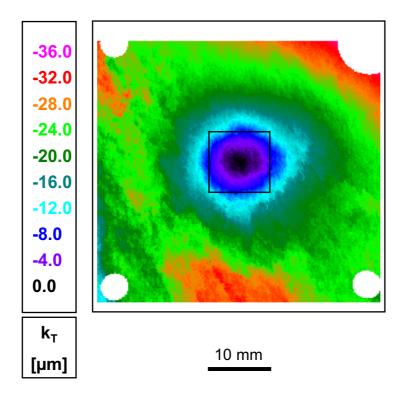


Figure 4.12. Flip-chip on board as examined by speckle interferometry. Depicted is the deflection $k_T(T)$, i.e. the displacement u_z measured from the centre of the die at room temperature for the thick board. Note also the intrinsic warpage of the board $\delta d < \pm 10..15 \ \mu m$.

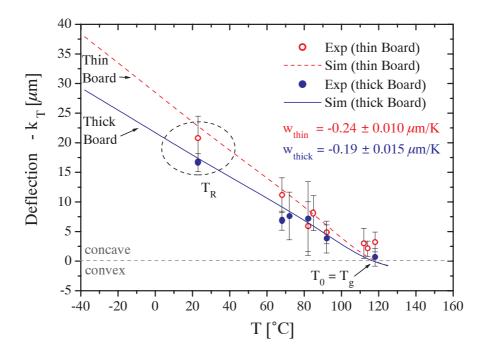


Figure 4.13. The deflection $k_T(T) = w(T_g - T)$ for $T < T_g$ (w being the function gradient) as a function of temperature measured by speckle interferometry. The highlighted region refers to room temperature. At these points the corresponding values on the lines represent the precision measurements which the simulations are also based on.

simulated result is depicted. The temperature dependence is reproduced consistently by the simulation and is linear. We complete the last formular by writing:

$$k = k_T + k_F = w(T_q - T) + qF,$$
 for $T < T_q$, (4.8)

where w is the function gradient (board thickness-dependent). Significant is the fact that close to the glass transition temperature T_g of the board the curvature changes sign although the stress-free state is reached at $T_c = 160$ °C only. This is due to the fact that above its T_g the board's CTE drops to a very small value (around $\alpha_{T>T_g} \approx 1 \ ppm/K$, cf. data set for organic board in the appendix B.2.2). This anomaly together with a decreasing stiffness above T_g causes the flip-chip assembly to essentially display hardly any curvature. A tendency which has also been observed in [18].

Obviously, displacement and deflection are interconnected here, but it is important to remember that eventually the curvature (deflection) of the chip is the desired local quantity and that the displacement is dependant on the specific set-up of the device, housing, component etc., or as is the case here, the apparatus depicted above in figure 4.9 and only a means to produce a state of bending.

Still as the displacement is a tangible quantity it will be always stated despite its being only an auxiliary variable and therefore not universal but only significant for this work. It can now be written down for this test-setup:

$$d = d(F, b, P_{bd}(T, t), fix), (4.9)$$

$$k = k(d(F), b, P_{bd}(T, t), fix),$$
(4.10)

where the quantities in brackets signify force F, board thickness b, temperature- and rate-dependent material properties $P_{bd}(T,t)$ (e.g. viscoelasticity of board) and the type of fixation.

Here the results obtained by simulation have already been shown in the graphs for verification. The next section deals with this accordance between simulation and experiment.

4.3.2 Verification: Displacement and Deflection

In simulating the macroscopic response of the flipped chip on board according to the experimental set-up depicted in figure 4.8 the main model (figure 4.3) was employed. So in this case we are not interested in any creep strain for the moment but only in the global behaviour so no bumps were included in the model. This has no effect on either deflection or displacement as already mentioned.

In a first load step the curing of the underfill was taken into account by cooling down from the curing temperature $T_C = 160$ °C to room temperature $T_R = 25$ °C. This results in a thermal deflection k_T of the chip due to the thermal mismatch of chip and board.

In a second load step the boundary conditions which hold the board parallel to the xy-plane where the spacers touch the board (fixed u_z -displacements) are activated. The respective nodes are thus allowed to move freely in the directions orthogonal to it, thereby mirroring the experimentally prescribed situation. The external force is then applied, too. As a

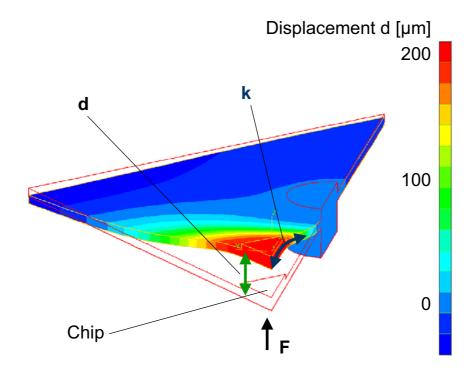
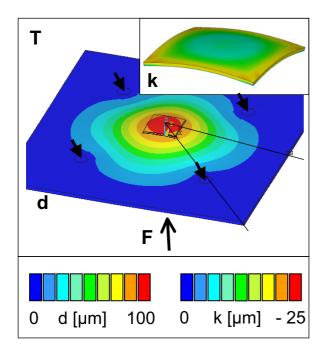


Figure 4.14. Visualisation of displacement (d) of the board and deflection (k) of the chip as a function of the externally applied force (F). No adhesive is present for this case. The scale refers to the displacements d in z direction. This model was used to verify the experimental results stated in figures 4.10 and 4.11 by dashed lines.

result, chip and board experience a displacement d in out of plane direction. In addition to that, the chip reacts again by bending and produces the second, mechanical contribution to the deflection k_F . This behaviour is illustrated in figure 4.14.

When not only an octant but the whole device is modelled the perfectly spherical displacement field around the chip is clearly visible (cf. figure 4.15 to the left). The effect of the non-circular fixation by four screws is thus neutralized by the stiffness of the board. This indicates that our set-up may indeed be used to make statements of more general validity as the kind of fixation seems not important. Even if a non-symmetrical fixation is used the state of bending is to a good approximation spherical (cf. figure 4.15, right) as can be inferred by the insets which show the deflection k of the die under combined thermal and mechanical load (the force is applied directly below the die). For obvious reasons we do not want to have our lifetime evaluation depend on any special position or fixation: So both figures feature similar kinds of local bending at the site of the chip although globally their fixation is completely different.

It can therefore be concluded that it is sufficient to study a symmetrical set-up and we may concentrate on interesting parameters like materials, mechanical loads and constraints. Further it allows easy, reproducible and controllable application of boundary conditions and loads and represents an invaluable advantage for FE-simulations as only one octant needs to be considered.



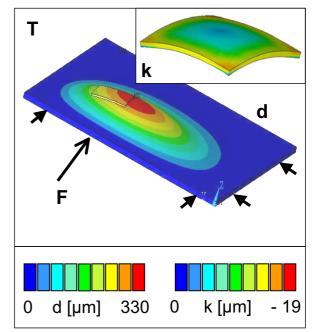


Figure 4.15. Left: Symmetric set-up suitable to study effect of 'five-point bending': At four points (arrows) the board is fixed, at the centre point the force is applied). The displacement field close to the chip is perfectly spherical. Right: Arbitrary set-up of a flip-chip on board with a force F applied from below. Despite its eccentric position the chip still bends spherically as seen from the deflection k.

4.3.3 Calibration of Organic Board Data: Viscoelastic-Isotropic vs Elastic-Orthotropic

In comparing the experimental results discussed in the last section with the simulative prediction for displacement and deflection, a discrepancy was found which has to be attributed to the numerical representation of the organic board.

One reason for this is that in carrying out simulations one is forced to make a choice as to rate-dependence (elastic-viscoelastic) and symmetry (iso-orthotropic): Ansys supports only isotropic viscoelasticity or orthotropic elasticity. The material, however, exhibits both features and both ought to be simulated: viscoelastic relaxation as a function of time and temperature was found and is depicted in section B.2. Possible viscoelastic behaviour of compound materials consisting of a fibre-reinforced epoxy resin have already been pointed out in [101]. Then the material is orthotropic which is obvious from its layered structure.

So the question is: Which behaviour is more important for the description of the board, orthotropism or viscoelasticity, and which material parameter is responsible for the deviation? Then: How can agreement between experiment and simulation be obtained? To answer these questions the following parameter study was made. Thereby first the influence of the material parameters on the result is clarified before a physically justified calibration is made to reach agreement (by introduction of a calibration factor). Some quantities had to be remeasured with greater accuracy as they have a stronger influence on the result

than previously assumed.

In the following the decisive steps are presented and the results given in table 4.3 and figure 4.16. A complete protocol of the study can be found in the appendix B.2.4.

Cornerstones of the calibration process:

To countercheck the experimentally obtained data (quoted in lines $(1a,b)^{17}$ of table 4.3) the measured viscoelastic set of data was used to carry out the simulation (lines (2a,b)). A distinct discrepancy was found. The board appeared to be too stiff; The applied loads did not yield a high enough displacement of the board.

Board Data: Elastic versus Visco-elastic

Cnfg	#	b	Law	β	\overline{F}	k_T	k_F	d	Comment
Units		[mm]			[N]	[mm]	$[\mu m]$	$[\mu m]$	
Exp	1a	0.78	?	-	7.7	20.3	4.6	100	k_F and d linear in F
	1b	1.15	?	-	20.3	15.8	6.9	100	k and d linear in F
Sim	2a	0.82	ve-iso	1.0	7.7	20.5	4.3	70.3	measured ve-data:
	2b	1.18	ve-iso	1.0	20.3	14.9	5.4	70	d too small
	3a	0.82	ve-iso	0.7	7.7	21.1	5.2	99.9	best solution:
	3b	1.18	ve-iso	0.7	20.3	15.7	7.05	98.5	closest set visco
	4a	0.82	el-ort	1.0	7.7	20.6	4.5	85	derived el-data:
	4b	1.18	el-ort	1.0	20.3	15.2	5.9	83	d too small
	5a	0.82	el-ort	0.85	7.7	20.8	5.1	99	no effect on k_T
	5b	1.18	el-ort	0.85	20.3	15.5	7.0	97.5	but closest set elastic
	6a	0.82	el-iso	0.85	7.7	20.6	4.9	90.7	isotropic and elastic
	7a	0.73	ve-iso	1.0	7.7	22.3	5.3	97	b_{eff} for 0.8 mm
	7b	1.045	ve-iso	1.0	20.3	16.7	7.0	97	b_{eff} for 1.2 mm
	7c	1.38	ve-iso	1.0	43.8	12.7	8.4	100	b_{eff} for 1.6 mm

Table 4.3. Cornerstones of calibration process; The discussion is in full given in appendix B as well as the elastic-orthotropic and visco-elastic-isotropic material data used. As usual b is the board thickness, β is a calibration factor for the elastic modulus of the board. Applied loads are: $T = 160 \rightarrow 25$ °C within t = 300 s. The abbreviations signify: ve-viscoelastic, el-elastic, ort-orthotropic, iso-isotropic.

It was then tried to adjust the material data of the board in that as good as possible an agreement of experiment and simulation could be established. As criterion the values of the two board thicknesses have to coincide in the tree variables k_T , k_F and d as a function of F.

¹⁷These values are taken from figure 4.10. As in the experiment, simulations were carried out for the thin (a) and the thick (b) board.

A calibration factor $\beta < 1$ introduced to 'soften' the board by multiplying the elastic modulus of the board. Thereby an effective E-modulus (tensor) is given by

$$\boldsymbol{E}_{eff} = \beta \boldsymbol{E}_0. \tag{4.11}$$

This measure did not affect k_T but only d (lines (3a,b)). The change in the modulus is not the crucial variable to dominate the deflection of the chip. Also a viscoelastic change in time does not enter significantly. k_T is mainly influenced by T_g and $\alpha_{T < T_g}(T)$ as shown in the appendix.

Still an effective modulus does affect the displacement of the board. Taking $\beta_{ve} = 0.7$ (rows (3a,b)) produces the best fit to all considered quantities when compared to the experiment (again lines (1a,b)). It is important to point out that also the thickness b of the board influences d and k. This quantity has to be measured carefully.

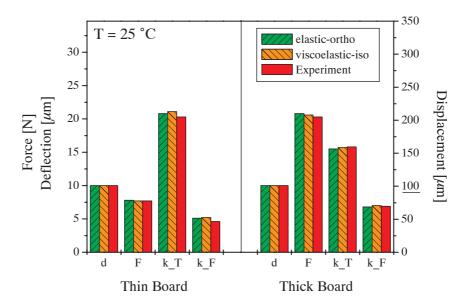


Figure 4.16. Visualisation of the main statement of table 4.3: Both viscoelastic-isotropic and elastic-orthotropic material data achieve good agreement with the experiment in all measured quantities. Here, as driving quantity is the displacement is given, not the force. Both sets of data are calibrated to optimum fit by their respective factor β given in the table.

Then for comparison to the viscoelastic-isotropic board, an elastic-orthotropic set of data is needed. This represents the time-honoured way of simulating an organic board. This set was obtained from the measured viscoelastic data by simulation: A pull-test (as it would have been performed for the measurement of the elastic modulus in tension) was modelled and computed by simulation. For this purpose the pull-test was performed on this 'virtual' dog's bone specimen for various temperatures with a speed of $v = 0.1 \, mm/s$. The thereby obtained values for the elastic modulus $E_{x,y}$ lay close to the initial modulus of the viscoelastic data. The remaining orthotropism parameters shear modulus and Poisson's ratio (G_{ij}, ν_{ij}) are now tensorial quantities and came in through a calibration factor derived from an already existing orthotropic data set [102] and subsequent adjustment.

The simulations were carried out with this set, assuming $\beta_{el} = 1$ as an initial value (rows (4a,b)). Again this yielded too large values for d and was corrected by taking $\beta_{el} = 0.85$ (rows (5a,b)).

So a very good accordance as to the displacement and both types of deflection can be established with either set of data when a calibration factor β is used. This fact is illustrated once more in figure 4.16. There the values are calculated for a given displacement $d = 100 \ \mu m$ which makes it easier to analyze the values for k_F which should only be compared at equal values of d.

Row (6a) shows the influence of the material's symmetry: The board was simulated elastic-isotropically. A deviation of 10 % is the result, the inclusion of orthotropism softens the board for this set-up. This is a consequence of a more complicated load situation due to the fixation and the presence of the chip which deviates from a state of pure bending for which no deviation is expected.

Influence of Organic Board Material Parameters

Increase in Parameter	Symbol	Influence	Response
E-Modulus	E_{ii}, G_{ij}	++	d
		_	k_T
		+	k_F
Board Thickness	b	++	d
Glass-Transition Temperature	T_g	++	k_T
		0	d
CTE (in-plane) below T_g	$\alpha_{\parallel,T < T_g}$	++	k_T
		0	d
CTE (in-plane) above T_g	$\alpha_{\parallel,T>T_g}$	++	k_T
		0	d
CTE (out-of-plane)	$\alpha_{\perp,T>T_g}$	0	d, k_T
Poisson's Ratio (in-plane)	$ u_{ij}$	_	d
		0	k_T
Cooling Time	t_{cool}	+	k_T
		0	d, k_F

Table 4.4. Qualitative effect of an increase in a material parameter on the macroscopic response. Legend: ++: strong increase; +: weak increase; 0: no influence; -: weak reduction; --: strong reduction.

Now the aim is reached and the simulation describes accurately the experimentally obtained data for the global quantities. Also the dependence on temperature is accurately reproduced by both sets of data as counterchecked by speckle interferometry in figure 4.13.

Eventually the viscoelastic set of data was given preference for carrying out the simulations although is seems not to be responsible for the accurate description of bending of the chip. It may still have an influence on the remaining assembly and stress relaxation may become important at other points and over the period over one or more complete cycles,

where temperatures close to T_g are encountered over a significant span of time. In view of (6a) the influence of the material's symmetry can – at this point – be assumed to be compensated by a calibration factor, whereas this is not possible for rate-dependence. The graphs in figures 4.10, 4.11 and 4.13 have been calculated with this set of data. Finally the qualitative influence of the material parameters varied in the study on the response quantities is summarized in table 4.4.

The system is now ready for the evaluation of creep strain!

Several comments need to be made:

First of all, an organic board represents an multi-layered, orthotropic, inhomogeneous low-cost material. It consists of a fibre-reinforced epoxy matrix, where the fibres mainly fill the middle layer of the board and the epoxy makes up the surface. The fibre tissue extents only in the xy-plane, therefore it is undoubtedly orthotropic. Fibre and matrix are not interwoven regularly, and they do not interchange on a microscopic scale but are of the order of magnitude of e.g. a bump or a pad, therefore the material is inhomogeneous. The board is neither perfectly plane nor is its thickness constant over our region of interest.

In other words, a material model for an organic board is bound to make assumptions and simplify. So an introduction of calibration factors seems justifiable.

To determine orthotropic data of a quasi two-dimensional material is difficult, let alone for a visco-elastic case. Many parameters – such as Poisson's ratio – have to be extrapolated from the bulk material or taken from literature. Then material parameters do vary. Especially the glass transition temperature T_g and the CTE α may diverge a good deal¹⁸ from the values measured for this special material employed in this work and do have a relevant influence on the results as shown in table B.1. This variety is also reflected in literature (see e.g. [68] or [29]).

Further, it has been mentioned that not all material models are available in FE-tools. Viscoelasticity in *Ansys* allows only isotropic symmetry. In the adjustment process calibration factors were introduced in order to establish accordance. This indicates further that it is not trivial to model these composite material.

But the calibration factor $\beta < 1$ can be physically motivated: The set-up of the flip-chip on board involves a different kind of loading of the board than the one its material data was measured with. Dog's bone specimens were loaded in tension and left to relax in the in-plane direction only. The stiff fibres determine most of the elastic modulus before relaxation starts which means that material inhomogeneity and orthotropism are not 'seen' in this measurement. In our set-up which resembles a 'five-point bending' experiment (for its being reminiscient of the number 'five' on the face of a die in a game) the board is loaded in bending and also in shear (at the spacers). Hereby the zone of loading is shifted from the central layer (fibres) to the outer layers (epoxy-resin). This thesis is supported by a three-point bending experiment of a dog's bone specimen (no shear(!)). The measured elastic modulus dropped¹⁹ by a factor $\beta \approx 0.83$ which would justify the elastic-orthotropic calibration factor. So this can account for a smaller stiffness but entails that our material

¹⁸Own investigations have shown $T_g \in [115 \, {}^{o}C, 135 \, {}^{o}C]$ and $\alpha_{T < T_g} \in [11.5, 13.5]$ and $\alpha_{T > T_g} \in [0.0, 4.5]$ for material provided by different manufacturers.

¹⁹Tension: $E_{x,y} = 23 \ GPa$; Three-point bending: $E_{x,y} = 19 \ GPa$

data is to a certain degree load-case dependent and that for a universal material model a more elaborate, composite description has to be found.

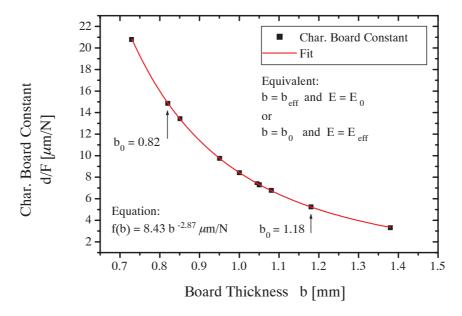


Figure 4.17. Simulated values for the board constant d/F as a function of board thicknes. The graph is valid for the board data and experimental set-up of this work.

But both data sets need a calibration factor. A 10% increase in stiffness due to the incapacity to simulate the material's orthotropism would nearly account for the viscoelastic $\beta_{ve} = 0.7$. Still there remains a general measurement inaccuracy in determining the modulus. The correlation between the viscoelastic and elastic data as was described earlier depends on the correct numerical representation of the simulated pull-test in the time domain, a discrepancy which could make up for the remaining difference in the calibration factor.

As far as the thickness of the board plays a role, the copper fan-out (see layout of the circuit board in figure 4.25), is not considered on board level due to its fineness. It is thought condensed in the overall thickness of the board and elastic modulus.

The measured board thickness (as stated in lines (1a,b)) does not include the soldermask layer on either side of the board. Since the board is not uniformly covered with soldermask, an averaged value was added to yield a working thickness of $b_u = 0.82 \ mm$ for the thin board and $b_x = 1.18 \ mm$ for the thick one. Here, the nominal value provided by the manufacturer $(0.8 \ mm)$ and $1.2 \ mm$ respectively were not accurate enough.

It ought to be mentioned that instead of introducing an effective elastic modulus as in equation 4.11 one might have introduced an effective board thickness like:

$$b_{eff} = \gamma b_0. \tag{4.12}$$

This equivalence as to the board is illustrated in figure 4.17. The diagram is either valid for $E = E_0$ and $b = b_{eff}$ with $\gamma = 0.878^{20}$ or $E = E_{eff}$ and $b = b_0$ with $\beta = 0.7$.

 $^{^{20}}$ cf. figure B.5

The equivalence prevails as long as there is no chip mounted and only the pure board is considered. As seen from lines (7a,b) the effective modulus produces better results concerning the thermal deflection and therefore E_{eff} is finally given preference.

4.3.4 Critical Displacement and Risk of Die Crack

In determining the save parameter range for our experiments it is necessary to rule out the risk of die crack and therefore to determine the maximally allowed values for the applied loads. To this end the displacement was further increased until the die finally cracked. The maximally attainable curvature was recorded experimentally by gradually increasing the force in edging towards the critical point and recording the curvature at each step until the die did crack.

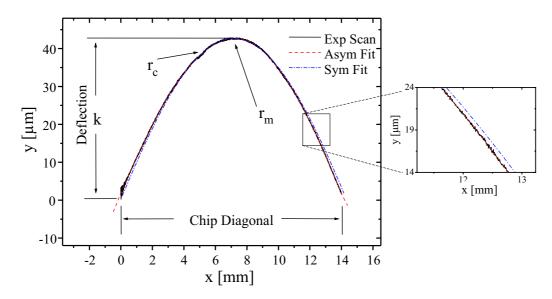


Figure 4.18. Illustration of Deflection k: Profile as scanned along the diagonal of the chip and fitted by a polynomial. At the peak the radius of curvature assumes the theoretical minimum r_m , but due to non-ideal conditions (asymmetry), this chip has an eccentric minimum radius r_c . It is assumed that this radius is the critical one for die fracture.

The radius of curvature has been evaluated by fitting the experimental (see figure 4.18) data to a polynomial function of sixth order comprising only even powers (to get the theoretical minimum radius r_m in the middle of the die) and by taking the inverse of the second derivative. This obviously assumes, as the simulation always does, that the die bends symmetrically and that the point of greatest stress is in the exact centre of the die. This is not always true, but a polynomial of the above kind can make up for this deviation if it is not too large. For with a large asymmetry this method would predict a larger radius than there really is thus underestimating the risk of fracture.

Therefore the measured data were fitted to a ninth degree polynomial with all powers allowed. This curve produces a very close fit (cf. the inset in figure 4.18) which is then not necessarily centred about the middle of the die. The eccentric minimum radius r_c thus

obtained by the asymmetric fit is always slightly smaller or similar to the one obtained by the symmetric fit $r_c \leq r_m$ but has to be taken as the correct critical value for fracture, whereas r_m is evaluated and correlated to the simulation. This asymmetry may be due to an eccentric force application or inhomogeneities within the assembly (the effect is, although smaller, also visible if no force is applied).

This precision deflection measurement could only be performed at room temperature, but since the curvature is also a strong function of T it is important to know the highest stress in the die which should coincide with the smallest radius of curvature. This situation is aggravated as the temperature decreases. Diverse values for the radius were recorded at T_R and extrapolated via simulation to the lowest temperature of interest (T = -40 °C) for our cycle tests. The result is given by the graphs in figure 4.19.

Here the (inverse) radius is printed versus the deflection and displacement for room temperature T_R and T = -35 °C which is close the minimum temperature for the thermal cycle test. For each board thickness the radius has been measured for various values of force at T_R (red symbols and lines). Averaged values for the critical radius r_c just before die crack (red stars) and the corresponding symmetric radius r_m (red square below) are marked. Then r_c defines a borderline for each board thickness, i.e. the minimum radius found under a given load in the experiment. Beyond this line die crack is likely to occur.

Then these values are simulated and the extrapolation to low temperature is made. For T_R the simulated values (green lines) slightly underestimate the curvature and thus the risk of die crack. This should be due to a systematic feature of the simulation concerning e.g. material data: We see that as expected, deflection and inverse radius increase with decreasing T (blue lines). The relationship between k and 1/r is linear which means that for an unconstrained die (no adhesive, see next section) either variable is fit to describe its behaviour. Mechanical and thermal load do contribute to r to equal parts and in the same fashion (see figure B.6 in the appendix where this is depicted for a larger range of values). Still the proportionality is not exact, as (we quote from this reference):

$$r(k) = c_1 \frac{1}{k} + r_{\infty} > c_1 \frac{1}{k}, \tag{4.13}$$

where $c_1 = -2.08 \ 10^{-4} \ m^2$ and $r_{\infty} = 0.055 \ m$. The deflection is reproduced correctly as it was used to calibrate the simulation, whereas for the radius there remains a slight overestimation by r_{∞} .

The results are correlated to the displacements in figure 4.20 and we obtain an upper limit of $d_c \approx 300~\mu m$ which is what we were looking for. This is thought to be a good value despite the slight underestimation of curvature by the simulation: The measurement of the crackpoint is a very delicate procedure and depends on how careful the force is increased. In the test-specimen during thermal cycling the adjusted curvature increases further due to the slowly varying thermal load and unlike in the test without sudden effects. This means that the die could tolerate even a smaller radius, $r_c = 0.46~m$ given in the graph would then have to be considered too large and therefore conservative enough to make up for the computational overestimation of r_m .

Under the given boundary conditions a save upper displacement should not exceed a value of $d \approx 200 \ \mu m$.

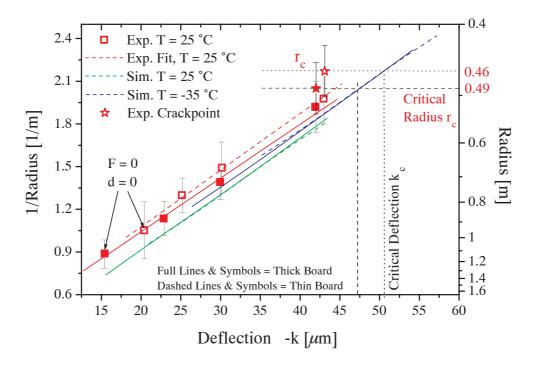


Figure 4.19. The radius of curvature $r_m(k,T)$ at the centre of the die measured along its diagonal versus the deflection k: The experimental values are recorded at room temperature, the computational ones are based on the simulations presented in the last section. Uncritical values of r are below the dotted line. r_m and r_c are defined in figure 4.18.

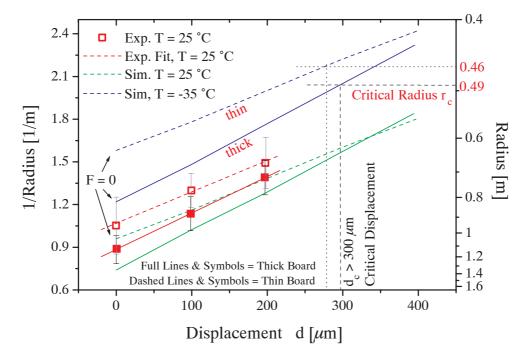
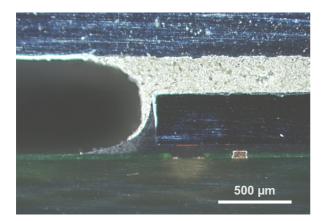


Figure 4.20. Radius r(d,T) versus displacement d. A critical displacement can be derived as $d_c > 300 \ \mu m$.

Response of Flip-Chip with Adhesive: 4.3.5Inhibited Curvature

An other important topic in FC&RSC is the reverse side attachment of the die by a thermal adhesive. Thereby it is expected that the movability of the die is further constrained in comparison to the 'free' case which should have repercussions on its curvature and later on its reliability.

In order to measure the curvature of an attached chip the method described in the last section cannot come into effect. One had to resort to another, unfortunately much less accurate means. The chip was glued to an aluminum plate where the thickness of the adhesive was adjusted by precision spacers between the board and the plate. Then it was cut in half parallel to the edge²¹. A line cut along the diagonal did break the chip at the corner. These specimens were subsequently polished and can be seen in figure 4.21.



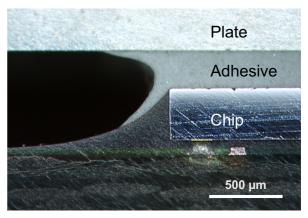


Figure 4.21. Left: Set-up for measuring the curvature: Cross section through the chip attached by a (medium-hard) epoxy-silicone based thermal adhesive ('E'). From top to bottom the different layers are: Aluminium plate, adhesive, silicon die, underfill, solder mask, organic board. The coarse structure of the adhesive is due to silver flakes. Right: Cross section with (very soft) silicone based thermal adhesive 'S'.

The deflection (as defined above or in figure 4.18) of the die was determined by repeatedly measuring the thickness of the adhesive (the distance from chip-top to plate-bottom) with a special microscope at three points (left edge, centre, right edge of the die). From this information it is easy to calculate the curvature of the chip. A mean value of three measurements was taken and the whole procedure carried out on at least 5 chips for each type of adhesive and board thickness. We optimized this method in order to come down to an error of within $\pm 3 \mu m$ which was the best result for this not very accessible value. (A laser scan over precision bolts which reached down through the plate to touch the chip surface [103] did show the effect of curvature but the results were not reproducible due to preparation effects.) Great care had to be taken not to cause the die to crack or splint since all attempts to clad the specimen into any kind of mold-mass leaving the adhesive

²¹This has to be taken into account when comparing it to the results of the last section!

intact and thus rendering it machineable failed. In the end it turned out best to do all steps manually. By the same method the thickness of the adhesive layer could be checked. The adjusted value of $h_{ad} = 265 \pm 20 \mu m$ was retrieved with a large deviation reflecting the known warpage of the board mentioned in section 4.3.1.

On analyzing the behaviour of the attached chip (cf. figure 4.22) one can distinctly discern the effect of the harder epoxy-silicone based adhesive which inhibits the curvature of the die significantly. Thus, it neutralizes to a certain extent the stiffening effect of the underfill which tries itself to curve the chip. The correlation of $k \sim 1/r$ (equation 4.6) may surely be lost at this point, but there is no possibility to measure r now.

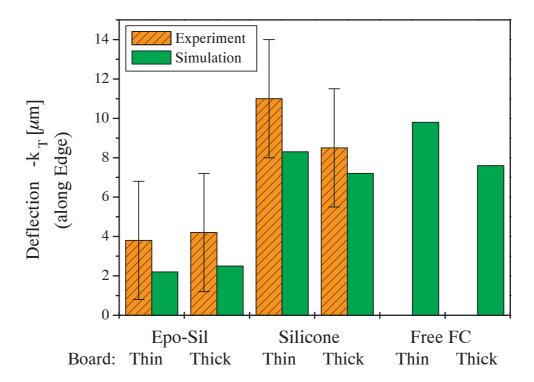


Figure 4.22. Juxtaposition of simulation and experiment for the deflection k_T at $T_R = 25$ °C. For comparison the corresponding value for the unconstrained flip-chip assembly is also given (rightmost column). Curing conditions of the adhesive were $t_c = 15$ min at $T_c = 160$ °C, the size of the chip used was $10 \times 10 \times 0.375$ mm. It should be noted that for technological reasons these values of k_T are measured along the edge, not the diagonal as in the previous section.

For the pure silicone adhesive there is hardly any effect as can be inferred from the nearly equal values for the free chip²² depicted in the right column. The standard deviation of $\pm 3~\mu m$ is mainly due to blurred edges at the aluminium-adhesive and adhesive-silicon interfaces. An other contribution to this could derive from the deviations in the thickness of the adhesive due to already mentioned intrinsic warpage of the board.

²²The curvature along the polished edge of the free chip could not be measured meaningfully by any of the presented techniques. Here the simulated value (approximately half of the curvature along the diagonal) is given.

The simulated value of the curvature along the edge is slightly smaller than half the value along the diagonal. The error bars show the standard deviation of the measurements according to which the simulation has been calibrated. The curvature along the cut for the unconstrained (pure) chip was not measured.

In analogy to equations 4.10 the dependence on variables can now be complemented by the properties $P_{ad}(T,t)$ and gap width h_{ad} of an adhesive material:

$$k = k(d(F), b_{bd}, P_{bd}(T, t), h_{ad}, P_{ad}(T, t), fix).$$
(4.14)

To model what had been done in the test required a quarter-model of the flip-chip assembly with adhesive and plate (the model can be seen in the appendix C.9): In a first load step the assembly was cooled down from curing temperature. At this point we still deal with a full chip and consequently the symmetry boundary conditions are set to complement the quarter model to a full one. This can be seen in figure 4.23 (a): The chip bends as expected, but much less compared to the unconstrained chip (no adhesive). The result is identical – as it must be – to a simulation with octant symmetry. Now the system is left to relax for a twenty-four hours – just as was done in the experiment.

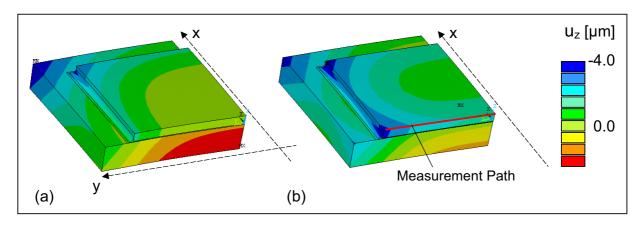


Figure 4.23. The displacements u_z in the simulation of the quarter model after cooling down from T_c (a) and after cutting in half and having the system relax (b). The adhesive and plate are not depicted to permit view on the chip surface. Symmetry boundary conditions are indicated by dashed lines and the path for measuring the deflection of the chip is printed as a red line.

In a third load step the assembly is 'cut in half' (as is to be seen in figure 4.21) by removing the symmetry boundary conditions along the y-direction (see figure). The assembly is left to relax for a load step lasting one week and the result can be seen in (b): The chip takes on a different state of bending, its centre moves to the centre point of the remaining – now rectangular – chip. This means that the adhesive complies with the much stiffer rest of the assembly. The deflection is now recorded along the printed path (red line in figure 4.23) as was done in the measurements. From the bars in figure 4.22 it can be inferred that the simulation can reproduce the measured values to a fair degree of accuracy. The simulation underestimates the deflection thus overestimating the stiffness of the assembly. There may be several reasons for that: First it could be a systematic measurement error

since all values measured with this method are slightly higher than the ones measured with the profilometer (cf. figure 4.22). For the silicone adhesive in any case a value smaller than for the free chip is expected.

For the case of the epoxy-silicone adhesive there might be other explanations. Any crack at the interface caused in the separation process or any tiny bubble in it would have the effect of an increase in k. Another reason for the discrepancy might be found in a particularity of the material. In chapter 3 we have worked on the principle that our polymeric materials behave thermorheologically simple, i.e. that their short-time behaviour at high temperature is correlated to their long time behaviour at low temperatures. A small deviation from this assumption may cause an underestimation of the viscoelastic relaxation at low T.

Now the correlation between experiment and simulation has been established on a macroscopic level, it remains to tackle the experimental evaluation of solder bump reliability for the flip-chip assembly with reverse side cooling.

4.4 Experimental Design and Procedure: The Test-Specimen

This part is concerned with the experimental verification of solder bump reliability. Its objective is to furnish a statistical statement about the average lifetime of a flip-chip assembly as a function of the mechanical loads prescribed. Therefore specially prepared test-specimens have to undergo thermal cycling under specified conditions in a thermal cycling chamber.

To this end a test-specimen was designed which allows reproducible and precise adjustment of loads in the range of interest. This specimen permits a statistical analysis of bump failure accomplished by computer-controlled high precision measurements of the electrical resistance of selected bumps as a function of the number of thermal cycles.

In the construction and preparation of the test-specimens we draw upon the experience gained in the previous chapters. On top of this, some other guidelines or boundary conditions were considered for the design:

- Comparability: All test-specimens have identical dimensions.
- Reproducibility, identical process parameters: For each test-group i.e. parameter configuration the samples should be in the same state, in the ideal case they should be identical. This imposes that all processes to which the samples are subjected during their assembly should in return produce reproducible states. Therefore high precision and low tolerances were assured by qualified standard flip-chip processes wherever possible.
- Series-conditions: Production steps are carried out under series conditions with professional equipment. For future impact on the market integrability into existing processes is important. Further it helps keep tolerances down.

- Realistic and economic design: The design which most realistically models the envisaged application should be tested and the materials most likely employable for this technology should come into use.
- FE-compatibility: The specimen complies to the FE-model's specifications.
- Low complexity and standardized parts.

All these requirements are met for the test-specimen which is presented in the following.

4.4.1 Electrical Layout of Chip and Board: Circuitry for the Detection of Bump Failure

In order to yield information about bump failure the electrical resistance of the bumps must be measurable. The chip in use provided two kinds of possibilities for this:

- Single-bump measurements at selected bumps (#2 and #6 as seen from each corner). This feature permits position-sensitive and four-point currentless (therefore very accurate) determination of the electrical resistance of a single bump (see 4.24). This possibility exists for sixteen bumps, where 8 × 2 are located at statistically equivalent positions due to the octant symmetry of the chip.
- So-called 'Daisy-chain' measurements. Hereby the resistance of all bumps plus the wiring on the chip and board as depicted below is measured. This kind of measurement considers all electrically connected bumps save the ones involved in the four-point wiring. It is therefore not position-sensitive but serves as an indicator for overall bump-failure. It is much less accurate since it is not wired as a currentless measurement and the resistance is not purely due to the solder.

The individual connections for the single-bump (SB) as well as the daisy-chain (DC) measurements respectively are linked to pads on the circumference of the board as shown in figure 4.25. They can be connected via a needle-pin adaptor to a computer-controlled Ohm-meter.

The region to the left and the right of the chip are not covered by solder-mask on either side in order to attach the fixation directly to the board.

To reduce the warpage of the board after reflow the identical layout is again found on the rear side. This measure had indeed the desired effect as did show the comparison to the boards used for the set-up and had the circuits on one side only.

A slit decouples the two specimens per test-board mechanically. The twin-layout facilitates handling of the specimens when it comes to place and measure them.

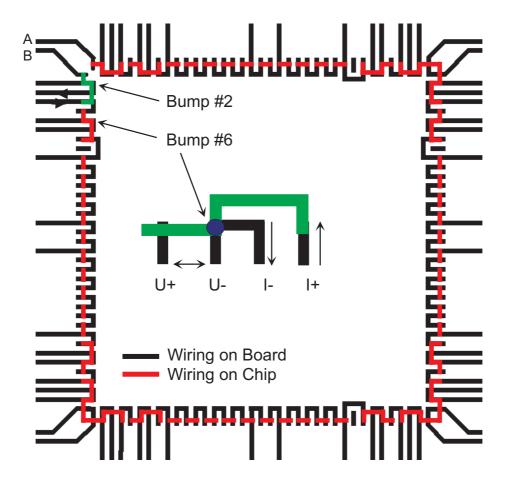


Figure 4.24. 'Daisy-chain'-circuit on chip (red) and board (black). It is connected via the pads labelled (A,B). In addition, currentless four-point-resistance measurements can be performed at 8×2 geometrically equivalent positions (arrows) due to octant symmetry. One four-point circuit is highlighted (green) and magnified (centre).

4.4.2 Design and Assembly of the Test-Specimen

The test-specimen essentially comprises the features of the apparatus used for the set-up experiments (cf. section 4.3.1) only in less universal but standardised and most compact form. The outcome is to be seen in figures 4.26 (as built) and 4.27 (schematic, 'exploded' view). The dimensions used are compiled in table 4.5 for the specimen and in figure 4.28 for the bump.

Flip-Chip Processes and Quality Checks

The qualified standard processes 23 employed under series conditions 24 were accompanied

²³We will not go into any detail for any of these processes. Here we refer to the standard textbooks on flip-chip technology [4,51].

²⁴Most steps were carried out in the *Robert Bosch* production site in *Ansbach/Germany* or in the laboratories in *Waiblingen* and *Schwieberdingen (Germany)*

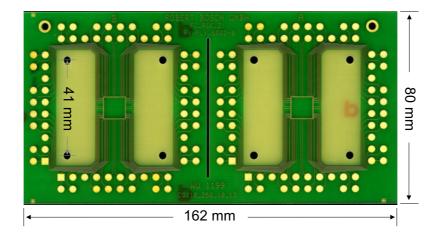


Figure 4.25. The circuit board for the test-specimen. The circuits on two chips may be contacted via pads.

by frequent quality checks²⁵ as to UBM (bump shear strength), bump hight, underfill airenclosures etc. All samples which did not pass one of the checks were sorted out and not considered any further (less than 1 %).

A non-standard process became necessary due to the occurrence of voids (next section) in the bumps on board level: The voids were extracted under vacuum.

Reproducible Application and Curing of the Adhesive

The chips have to be glued to the plate before any of the other boundary conditions or loads are applied. This corresponds to the series-conditions where the last step would be the closure of the housing under pressure and hence the application of external loads. The chip must then already adhere to the heat-spreader. Moreover, any load applied to the chip at curing temperature could do irreversible damage to the bumps and alter our required identical initial state preparation²⁶.

The following procedure furnished the best and most reproducible results for the adhesive-filled gap width $b_{gap} = h_{ad} = 265 \pm 20 \ \mu m^{27}$:

• The adhesive is dispensed in x-shape onto the chip. Then the board is put chip-down onto the plate where the spacers at the four holes adjust the specified gap width b_{gap} for the adhesive according to:

$$b_{gap} = b_{sp} - (b_{sm} + b_{uf} + b_{ch}), (4.15)$$

 $^{^{25} \}mathrm{This}$ test-programm was absolved according to the quality standards specifications of the Robert Bosch GmbH / Germany

²⁶The underfill cannot stiffen the assembly as required at $T_C >> T_g$ with the consequence that the bump is strained.

 $^{^{27}}$ The scatter is due to the warpage of the board and one of the reasons why the gap width was increased to hold the error down to less that 10 %. See also section 4.3.1 or 4.3.5

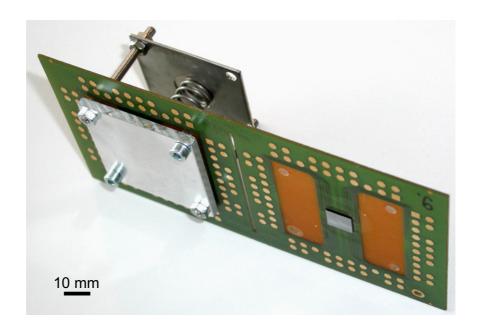


Figure 4.26. The test-specimen as it was built 220 times. One aluminium plate is demounted to permit view on the chip. Despite the plate the sample still fits in the needle-pin adaptor in figure 5.17.

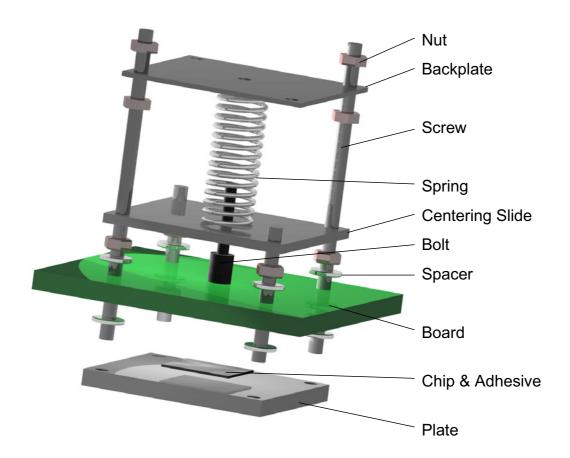


Figure 4.27. 'Exploded view' of the test-specimen and its individual components.

Item	Dimensions
Plate	$50 \times 50 \times 4 \ mm$
Nuts	M4
Spacers	$M4, 8 \ mm \ \phi \times b$
Screws	$M4 \times 50 \ mm$
Bolt	$6~mm~\phi$
Screw Positions	$41 \times 41 \ mm$
Board	$82 \times 82 \ mm \times b$
Chip	$10 \times 10 \times 0.375 \ mm$
Pitch	$250~\mu m$
Footprint	$230 \times 125 \ (btm), 100 \ (top) \times 45 \ \mu m$
Bump (Height)	$100 \ \mu m$, see also figure 4.28
Underfill (Thickness)	$65~\mu m$
Soldermask (Thickness)	$35~\mu m$
Thermal Interface (Thickness)	$265~\mu m$
Back-plate	$50 \times 50 \times 1.5 \ mm$

Table 4.5. Constant dimensions common to all test-specimens. b signifies a variable thickness (parameter) of the respective item, ϕ a diameter.

where the thicknesses of soldermask, underfill and chip are subtracted from the spacers' thickness b_{sp} . The amount of adhesive material is just enough to fill the whole gap without bubbles up to the edge of the chip and forms a fillet as depicted in figures 4.21. The exact quantity is important, since an encapsulation is to be prevented as it could severely crack down on the lifetime of the chip as pointed out in [11].

- Four small screws are inserted and gently tightened to keep the chip in position as the adhesive is cured.
- Either of the two adhesives is cured for fifteen minutes at the cure temperature of the underfill $T_C = 160$ °C. (Both adhesives are specified for this process.) This has the following advantage: The flip-chip assembly reaches again its stress-free state it had when the underfill was cured. This puts us in the comfortable situation that we deal with a defined state at this temperature to start from in our computational lifetime prediction. Shrinkage of underfill and adhesive is negligible according to the manufacturer's specifications.
- The assemblies are left to cool down to room temperature and the screws and spacers are removed.

Application of Loads and Boundary Conditions

In the next step the individual groups had to be configured i.e. their set of parameters adjusted.

For the non-adhesive groups there is no problem and the test-specimen can be assembled as pictured in figure 4.27:

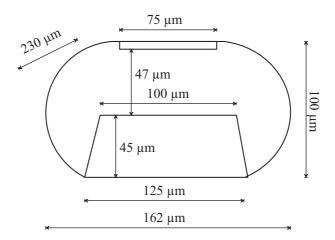


Figure 4.28. Dimensions of the bump as seen along the PCB track. The skew arrow indicates the length.

• The gap filler (sticky side) is attached to the plate and the four screws are put into their holes and fixed. In the order depicted, the spacers which specify the displacement d of the respective group are put in their position. The total thickness of the spacers b_{tot} now measures:

$$b_{tot} = b_{sp} + d, (4.16)$$

where b_{sp} is the thickness of the spacers from equation 4.15 to which the displacement which represents the load is to be added.

Then board, spacers again (here they serve only as washers), nuts and plates are added. The nuts on board and steel plate are not tightened yet.

- The steel plate labelled 'centering slide' serves to hold a bolt (well defined contact surface where it touches the board, identical for all samples) centered at the position of the chip. It is only held by the force of the spring and is not fixed anywhere. Is other function is to cage the spring. A force of $F \approx 50 N$ is not to be trifled with.
- Now the force is applied. To increase precision and reduce assembly time, small-scale production equipment driven by a pneumatic cylinder was designed (see figure 4.29 (right)): A very important feature represented the in-situ measurement of the applied force for each sample.
- As the cylinder compresses the spring with the correct force, the nuts at the backplate are fixed. The force can not change any more now.
- As a last step the nuts at the board are tightened. The board is now in the intended position: parallel to the plate at the four points as in our set-up experiments (section 4.3.1). So no in-plane forces which could cause the board to slide are active as would have been the case if the board was fixed before the application of the force.





Figure 4.29. To the left: All test-specimens (440 chips in 24 configurations) just before they go to the thermal cycling chamber. They are taken out and checked for bump failure in periodic intervals.

To the right: Small-scale 'production' equipment: Pressure application device for assembly process. An air pressure cylinder allows precise compression of the spring as the resulting force is adjusted and measured by a load cell (cable).

(Other washers with grip did not perform as well but put some inclination on the board.)

For the adhesive groups the procedure is a bit more complicated but follows in principle the same steps. Here it is important that the spacers are inserted before the screws are added (it does not function otherwise). Then the rest of the sample is put together, the force applied and then all nuts tightened, the ones on the board last.

Automatized Recording of Bump Failure

through measurement of electrical bump resistance was used. At specified intervals all specimens were taken out of the cycling chamber to be checked for their bump resistance. An in-situ measurement (permanent electrical check for bump failure) was beyond every means due to the immense number of contacts (see 4.29). To this end each sample was put into a needle-pin adaptor (see figure 5.17) and a program²⁸ was run which performed all necessary steps.

²⁸The program was written in *HP-VEE*.

4.4.3 Extraction of Voids under Vacuum

Voids were found in the bumps after reflow on board level as is to be seen from the pictures in figure 4.30. As can be seen also from X-ray photographs in figure 4.31 (a), the voids do emerge in a wide range of size from $b=5..50~\mu m$ and are distributed over the bump neither deterministically (always at the same position) nor randomly (small bubbles all over the bump, sponge-like): Voids tend to gather around and below the pad where they stay pinned after they float upwards during reflow. There they reduce the effective cross section which may also reduce their compliance to withstand fatigue cracking and therefore the lifetime of the bump. Above all it is the task of the bump to resist fracture rather than exhibit a large load carrying capability [15]. Voids are classified to be harmful depending on their size and location [12], [104]. They were reported to cause major concern if they are situated close to the connecting surfaces like pad or land [105]. On the other hand it has been reported [106] that voids may have the ability to stop already propagating cracks thus prolonging the lifetime of bumps.

In any case: Irrespective of whether voids do prolong or reduce the reliability of a bump the configuration in which they occur here disturbs the preparation for statistical equivalence of the bumps and the whole assembly: The bumps are not in a well-defined initial state identical for all bumps and so it is unlikely that the average lifetime for bumps with voids will only differ from a scaling factor from an impeccable configuration. This could cause a blurring of the statistical mean value for the cycles to failure. Moreover there is no *typical* void-configuration which could be modelled and simulated.

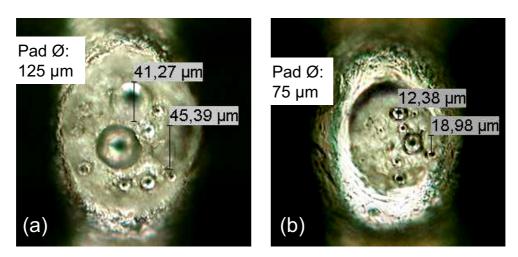


Figure 4.30. Voids just below the pad as they appear after reflow on board level. The chip and UBM have been removed to permit view on the solder bump. On the right the 'shoulder' is to be seen which is typical of this bump shape due to the small pad diameter.

For this reason the voids had to be eliminated.

A succinct parameter study was conducted in order to try to eliminate this phenomenon. Varied parameters were: The reflow profile (temperature and time above liquidus), the flux (tackiness, activity, volume), solder paste (manufacturer), the type of passivation on

chip and the UBM (different companies) [107]. Here it is important to point out that the aluminium trays the chips were reflowed on had no influence on the creation of voids.

It turned out that none of the parameters varied in this study could account for the prolific occurrence of voids and that it was beyond the scope of this thesis to optimize this process which would constitute a time- and resource-demanding technological development. A decision was therefore made to eliminate the voids by a vacuum process.

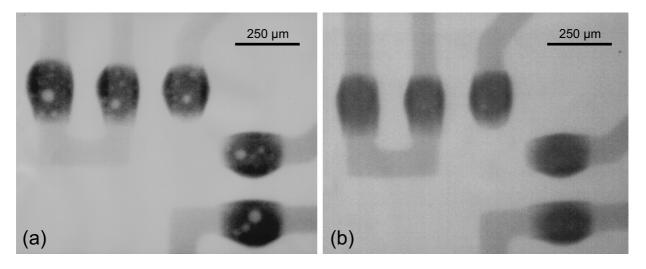


Figure 4.31. X-ray pictures of the same group of bumps before (a) and after vacuum treatment (b).

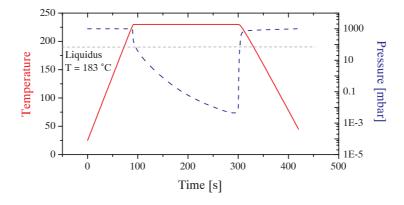


Figure 4.32. Process parameters of vacuum treatment on a hot plate used for obtaining the above depicted void reduction. The curves depict only a qualitative behaviour, but extremal values are to scale.

This vacuum process²⁹ was carried through on a hot-plate according to the scheme depicted in figure 4.32 for four chips at a time. This process step was optimized according to the following guidelines:

First, obviously, it should eliminate the voids to a satisfactory degree. Then the treatment itself should be as short as possible using as low a vacuum as possible not to cause any

²⁹Employed was a computer controlled hot-plate with vacuum-pump, a special design by SRO-Systems.

harm to the organic board. The result is depicted in the X-ray photographs in figure 4.31 to the right: The size and number of voids was greatly reduced by the vacuum process.

Now the preparations for the simulative and experimental study are all done. A numerically optimized and calibrated parametric FE-tool is set up to accurately evaluate the creep stain in the solder bumps and thus make a predictive statement about reliability. For the experimental part a test-specimen has been designed which is able to verify the numerical results in a thermal cycling test. The results of either of the two and their correlation will be the subject of the next (and concluding) chapter.

Chapter 5

Results and Discussion— Simulation vs Experiment

In this chapter the results of the finite element simulations are stated and interpreted for the individual load configurations. Therefore a ranking is drawn up according to the varied input quantities. Then the FE-results are compared to the statistical outcome of the experiment for verification.

Within the framework of the Coffin-Manson approach a correlation is established which enables lifetime assessment and extrapolation to other, not explicitly tested but interesting parameter and load configurations for the flip-chip assembly with attached heat-spreader.

Some configurations could not be analysed with respect to bump reliability as die crack did occur. A fracture criterion was applied to explain and predict this phenomenon.

At the end of this chapter we draw some conclusions, summarize the functional dependence of solder bump reliability on the varied parameters, give design guidelines and an outlook.

5.1 The individual Configurations and Applied Loads

The test-specimens are now to undergo the thermal cycling test. The available chips were divided up in 24 configurations, most of which containing 20 samples, a number which is considered sufficient for a Weibull-based analysis of solder bump failure. The chips were distributed according to the following philosophy and list of priority:

- All samples should undergo the same thermal cycling test, i.e. they should all be thermally equivalent. No variation according to the thermal loads is to be tested.
- The mechanical loads should be applied in a way which allows a variation of the value in the required range as well as a cross check to see the effect of force and displacement independently.
- Both a thick and a thin organic board are to be tested.
- Of the thermal interface materials the two gap fillers and two adhesives of different physical properties (soft, hard) are to be employed.

• Some configurations should be tested without loads to serve as reference to an unconstrained flip-chip assembly. For the same reason a group featuring only an attachment by an adhesive without further loads should be tested.

As there was a limited number of chips, the testing-scheme drawn up exhibits several preferences. So not the full program for the whole matrix was conducted. Some parameter variations have to be limited to one type of interface-material. The choice which was taken is explained in the next section.

5.1.1 Mechanical Loads and Characteristic Curves

All necessary information is now given to develop a distinct picture of what loads are present in a housing in reality. Each board thickness gives rise to a set of characteristic curves by which one may determine – as for a transistor – the characteristic parameters for the work point.

Classification of Load Configurations

#	Item	Code	Meaning
1	Letter:	K	Pure flip-chip (no attachment)
	Kind of reverse side attachment	${f L}$	FC with voids (no attachment)
	(thermal interface material)	\mathbf{F}	Flex foil
		\mathbf{C}	Carbon foil
		\mathbf{S}	Silicone adhesive
		E	Epoxy-silicone adhesive
2	Number:	0	No displacement
	Displacement	1	$d = 100 \ \mu m$
		2	$d = 200 \ \mu m$
3	Letter:	G	Gap closure
	Force	A	Work point
		В	Overload
		M	by negative Displacement
		_	Zero Force
4	Letter:	u	Thin board
	Board thickness	X	Thick board

Table 5.1. These abbreviations or encodings are used to specify the loads and materials of the individual configurations. See also table 5.2.

These characteristic curves are depicted in figure 5.1 and are to be read as follows: From section 4.3.4 it is known that the critical limit for the displacement is $d_c = 300 \ \mu m$. Beyond this value die crack is likely to occur. For this reason let us specify $d_2 = d_G = 200 \ \mu m$ as maximum gap width, encoded by the number '2' (for 200). To bridge this gap the board has to be pressed from below by the external force $F = F_G$ (x-axis) and follows a linear relationship up to the point where the chip touches the thermal adhesive. This linear

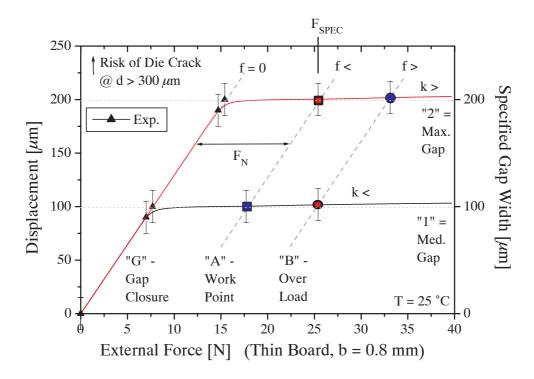


Figure 5.1. Force vs Displacement: Characteristic curves for thin board.

behaviour and the error-bars have been derived in figure 4.10. At this point the chip exerts no pressure (internal force) f = 0 N on the interface material yet.

Now the extra normal force F_N is applied to compress the interface material for optimum thermal contact. F_N is specified by the manufacturer. Throughout this work $F_N=10~N$ has been taken, a value which is for both gap fillers above the specified minimum force. This force cannot displace the board any further, therefore the curve flattens out parallel to the x-axis. The compression of the interface material is negligible compared to the accuracy the gap-width can be specified ($\delta d \approx \pm 15~\mu m$ from figure 4.10). This applies for the adhesives in any case, but also for the gap-fillers (figure 3.18). This point is called the work point 'A' for the given displacement at room temperature. It is furthermore characterised by a curvature k and an internal force $f = F_N$. Its external force is thus

Example:
$$F = F_{2Au} = F_G + F_N = \frac{1}{p_b} \Big|_{b='u'} d_G|_{G=2} + F_N,$$
 (5.1)

where p_b is the thickness-dependent board compliance defined in section 4.3.1 and b = `u' stands for the thin board. The same scheme is true for a medium-sized gap of width $d_G = d_1 = 100 \ \mu m$. This curve is depicted below the first one and is characterised by a smaller deflection k.

Let us assume that a chip has to be specified to function for a work point $F_{spec} = F_{2Au}$, then the situation may arise where the tolerance of the housing causes the gap to be smaller and the work point gets shifted down to lie on the lower curve. This represents an 'overload' situation denoted by 'B'. The internal force f is increased, since there is less force needed to displace the board. It assumes the value of $f_{1Bu} = f_{2Au} + 1/c_b \Delta d_G$, where Δd_G is the

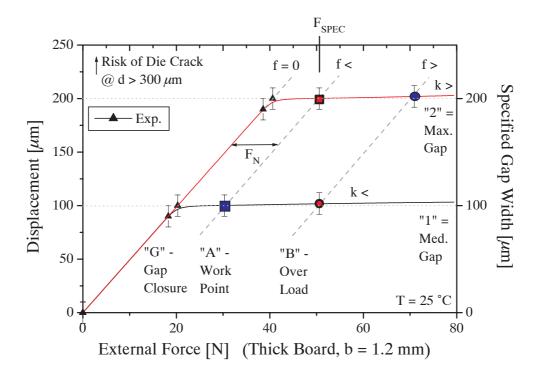


Figure 5.2. Force vs Displacement: Characteristic curves for thick board.

difference in gap width, which is chosen half the maximum gap width in expectation for a good resolution. This situation has to be managed by the chip also in reality. Therefore it is incorporated in the test-program.

These are the two points of practical interest for the design of a real housing situation. But we need to cross-check if it is the smaller displacement or the higher effective force on the chip that now affects bump life if it does at all. To this end the points F_{1Au} and F_{2Bu} , which represent the lowest and highest loads respectively, are also checked for. The same is true for the thick board and is depicted in the second diagram, figure 5.2.

Following this philosophy a test plan was drawn up which is depicted in table 5.2. For better visualization the main categories which the test-configurations can be divided into are illustrated in figure 5.3. So the line-up of the groups presents itself (table 5.2):

• K0u, K0x

The unconstrained chips 'K' are tested for both boards to serve as reference group. For thermal equivalence to the other samples they need to be connected thermally to the aluminium plate via their reverse side. This is accomplished by a very soft gap filler which merely touches the flip chip and does therefore *not* represent a mechanical load. This situation is depicted in figure 5.3 (a).

\bullet L0x

The group 'L' consists of chips which did not undergo the vacuum process. Therefore their bumps do still contain voids (figures 4.31 and 5.3 (a)).

Group and Material	Code	d	F	b	Type
Units		$[\mu m]$	[N]	[mm]	cf. Fig. 5.3
Flip Chip, no BC	K0u	0	-	0.8	(a)
	K0x	0	_	1.2	(a)
FC with Voids, no BC	L0x	0	_	1.2	(a)
FC, Flexible Foil	F1Au*	(200); 100	17.7	0.8	(c)
	F1Bu*	(225); 100	25.4	0.8	(c)
	F2Au	200	25.4	0.8	(c)
	F2Bu	200	33.1	0.8	(c)
	F1Ax	100	30.3	1.2	(c)
	F1Bx	100	50.6	1.2	(c)
	F2Ax	200	50.6	1.2	(c)
FC, Carbon Foil	C1Bu	100	25.4	0.8	(c)
	C2Au	200	25.4	0.8	(c)
FC, Silicone, no BC	S0x	0	-	1.2	(b)
FC, Epoxy-Silicone, no BC	E0x	0	-	1.2	(b)
FC, Epoxy-Silicone	E1Au	100	17.7	0.8	(c)
	E2Au	200	25.4	0.8	(c)
	E1Ax	100	30.3	1.2	(c)
	E2Ax	200	50.6	1.2	(c)
FC, Epoxy-Silicone, neg. Displ	E2Mu	-200	15.4	0.8	(d)
FC, Flexible Foil, neg. Displ	$F2Mx^*$	(-100); -200	20.3	1.2	(d)
FC, Silicone	S1Au	100	17.7	0.8	(c)
	S2Au	200	25.4	0.8	(c)
	S1Ax	100	30.3	1.2	(c)
	S2Ax	200	50.6	1.2	(c)

Test-Configurations and Applied Loads

Table 5.2. Overview over the individual configurations. The code refers also to the values for the applied loads (see table 5.1). The groups marked with an asterisk feature different loads (given in brackets) as originally specified due to a reduction of foil-thickness during thermal cycling. For Configurations with negative displacement ('M') the force is not externally applied by a spring but by the bending of the board itself.

• F1Au, etc.

The flexible foil 'F' seems a promising solution for thermal management. Therefore it undergoes (nearly) the full program depicted in figures 5.1 for both board thicknesses. Unfortunately die crack occurred in most configurations due to an unforeseen reduction of the foil-thickness. The remaining groups (asterisk) are still incorporated in the analysis. Above this situation is depicted in (c).

• C1Bu, C2Au

The carbon foil is only tested for the points of practical interest. The off-line values

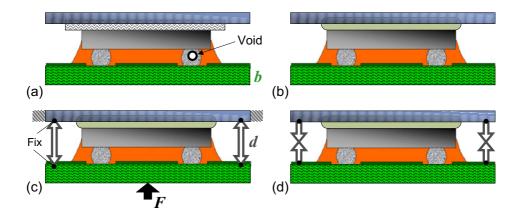


Figure 5.3. The main test categories depicted schematically (cf. table 5.2 and explanations below). Displacements d are depicted as black arrows which denote concave (c) or convex (d) bending of the board. An external force is symbolised by a bold black arrow.

C1Au and C2Bu are not tested for lack of chips. The cross-check is expected from another configuration. Again this situation is the one depicted in (c).

• S0x, E0x

The adhesives 'S' and 'E' are put to a test without any mechanical loads save their reverse side attachment (see figure 5.3(b)). In the first place they are incorporated as a less complex configuration for comparison to the computational results. Although these groups do not reflect the boundary conditions for flip-chip reverse side cooling in a casing (cf. figure 2.4), they still mimic the situation of a small, chip-sized heat-spreader attached to the chip.

• E1Au, etc.

The Epoxy-Silicone 'E' groups are tested for the two work points only (for lack of chips). The remaining two configurations can be evaluated by simulation if needed. This configuration is represented by (c).

• E1Mu, F2Mx

This principle is depicted in figure 5.3(d) and tested to see if a curvature which counteracts the tendency of the concave thermal bilayer¹ bending of the flip-chip on board. These groups have no external force applied but the chips are only pressed against the adhesive or foil with the reaction force of the board caused by a negative displacement of the board. At room temperature this compressive internal force is readily evaluated as $F_{2Mu,x} = f_{2Mu,x} = 1/c_b \ d_G > F_N$, which is, as it has to be, always greater than the normal force F_N needed for sufficient thermal contact.

• S1Au, etc.

The same as for the E1Au groups, only with Silicone adhesive 'S'.

¹Chip and board determine the sense of curvature due to their difference in the CTE.

5.1.2 Thermal Loads

The test-specimens finally undergo air-to-air thermal cycling in a two-chamber system. As a check we have recorded the temperature over the duration one (stable) cycle, since due to the large thermal mass represented by the aluminium plates it is expected that the given temperature profile of the chamber does not coincide with the one measured at the test-vehicle.

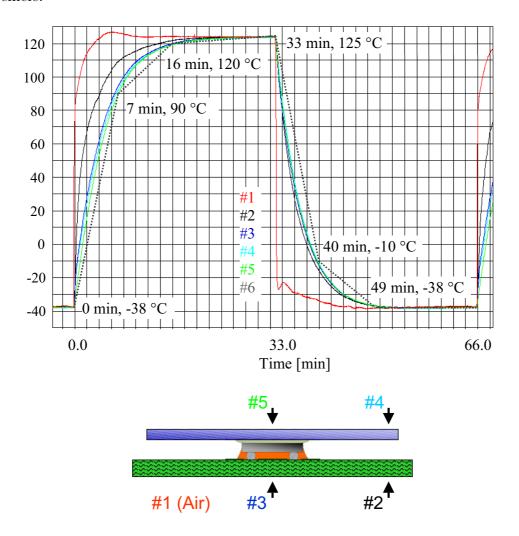


Figure 5.4. Temperature as recorded during thermal cycling at different positions on the test-specimen. The chamber was fully loaded during the measurements. Below: Position of the temperature sensors.

This is depicted in figure 5.4, where the individual graphs correspond to different locations of the temperature sensors on a representatively positioned test-specimen. First one notices indeed the retardation with respect to the chamber temperature (#1). But then it is important to see that there seems to be hardly any temperature gradient within the assembly since plate (#4,5) and chip (#3) show nearly the same profile, whereas the board (#2) follows with some distance the chamber air due to its small heat capacity and low

thermal conductivity. It is therefore a good assumption to assume a homogeneously distributed temperature across the chip where the creep law for the solder bumps displays a very sensitive temperature and rate dependence.

This outcome necessitates indeed the attachment of a heat-spreader also to the normal flip-chip test groups $K\theta u, x$ as they would otherwise 'see' cycle (#2) instead of (#3) as all other samples do.

The dotted, linearised temperature versus time function is taken to serve as thermal load input for the simulation.

5.2 Results of Computational Analysis

The simulation starts at the stress-free point which is assumed to be identical to the curing-temperature of underfill and adhesive respectively (see also [31,32]). Here, $T_{cure} = T_{ref} = 160$ °C. At this point all 'layers' are assumed to be parallel to one another, even after a second heat-up to this temperature for the curing of the adhesive this initial condition is assumed to be reestablished since T_{ref} is well above T_g of both underfill and soldermask. The results obtained by speckle interferometry in section 4.3.1 underpin this assumption. According to information provided by the manufacturers shrinkage of the adhesives is negligible.

For these reasons it is enough to simulate both of these curing processes simultaneously as the multi-layered assembly is cooled down to room temperature. This is depicted in figure 5.5 (first load step LS1).

In a second load step LS2 the mechanical loads are applied. This corresponds to simulating the assembly of the test-specimen. The model is then left to relax and to accommodate to the loads for some time before the actual thermal load cycle begins in the third load step (arrow).

This preparation is important to model the correct initial state of the different configurations and follows the steps conducted in the experiment as explained in the last chapter.

In this respect figure 5.5 represents the drive and response functions of the physical system we are about to observe. The graphs describe the loaded group C1Bu, i.e. an assembly using a carbon foil, medium loads and a thin board. The creep strains are recorded from the point where the thermal cycle starts since our model considers no singular (initial) events but only the creep strain accumulated over one cycle as required by the Coffin-Manson approach. As expected, the bumps exhibit the largest rise in creep strain during changes in temperature at high temperatures where large thermal strains and can cause maximum creep deformation of the solder due to a high creep rate. The outer bump (# 2^2 in figure 5.6) accumulates more strain induced damage than the inner one (#6). So for a flip-chip assembly under these mechanical loads bump creep strain increases with the bump's distance from the neutral point (DNP). This may indicate a dependence on chip size, too.

²The selection of bump #2 and #6 was imposed by the electrical chip layout (figure 4.24).

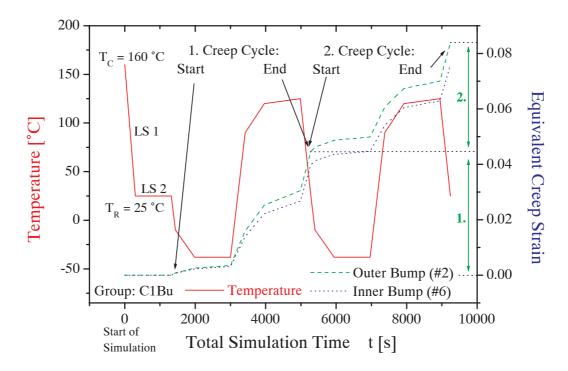


Figure 5.5. Drive and response: Temperature cycles as measured (cf. figure 5.4) and simulated as sequence of load cases. The resulting creep strain accumulates monotonically right from the beginning (t=0) and is recorded for each bump over a sequence of cycles.

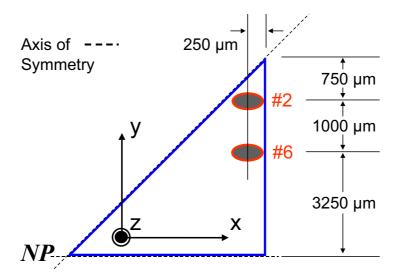


Figure 5.6. Schematic of flip-chip model with bump-location and orientation (not to scale). The bumps are numbered starting from the outermost bump, i.e. bump #2 is the second bump from the corner (cf. figure 4.24). The lower left corner represents the neutral point (NP). Due to the specific symmetry it suffices to model only one octant.

Remarkable in figure 5.5 is the fact that the creep strain per cycle seems to show a convergence behaviour as it changes (in this case decreases) for the second cycle. Apparently the flip-chip assembly accommodates to the external loads after the first cycle and $\bar{\varepsilon}^{cr}$ becomes stable. This will also be explained below in the course of the next sections.

5.2.1 Ranking of Configurations

The results of the simulations of the configurations tested in the cycle experiment are depicted in figure 5.7 for the first cycle and in figure 5.8 for the second cycle. The ranking is determined by the equivalent creep strain averaged over both bumps.

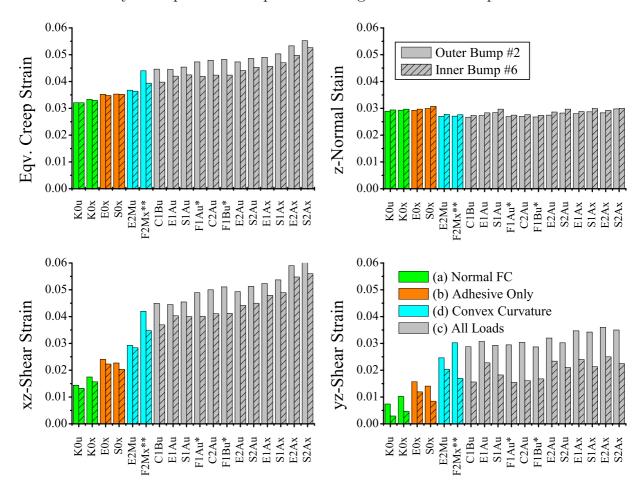


Figure 5.7. Ranking of configurations for the first simulated cycle sorted by equivalent creep strain ε^{cr} . Depicted are also the accumulated normal ε_{zz} and shear components ε_{xz} and ε_{yz} of the creep strain tensor ε^{cr}_{ij} for outer and inner bump. The numerical values are also given in table D.1. During the first cycle the system goes through a phase of transient response before convergence is reached in the second cycle. The asterisk refers to table 5.2, the colours/letters (a-d) to the categories of figure 5.3.

In the diagram the dominant strain tensor components are depicted individually for inner (#6) and outer bump (#2). For reference see again the schematic of the chip in figure 5.6.

The first observation is that there is a distinct difference as to the individual configurations, i.e. there is a ranking and a dependence on the mechanical loads which cause an increase in equivalent creep strain in all configurations. Hereby the values range from $\bar{\varepsilon} > 0.03$ for the best configuration up to $\bar{\varepsilon} < 0.06$ for the worst. This is nearly an increase by a factor two for the first cycle! Apparently mechanical loads do have a significant and harmful influence on lifetime, a tendency already indicated by [11] who considered chips attached to a heat-spreader by an adhesive (comparable to the groups $E\theta x$ or $S\theta x$) without fixation.

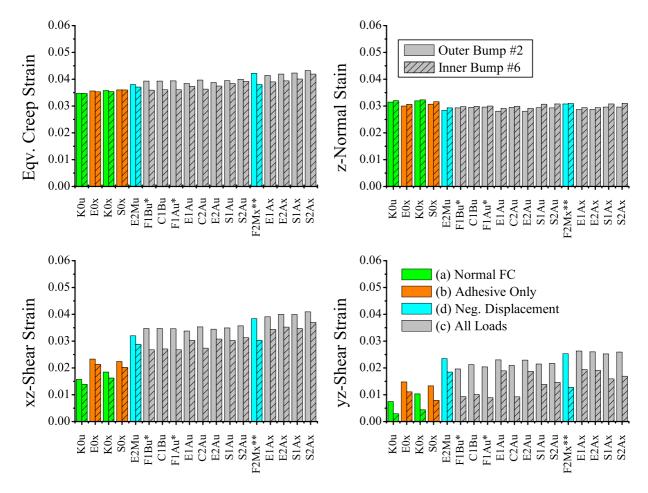


Figure 5.8. Ranking after the second (stabilized) simulated cycle.

On simulation of a second cycle the system relaxes and there is a creep strain redistribution to the effect of a smaller equivalent creep strain for all constrained chips. The order of the ranking changes, too, i.e. the degree of relaxation depends upon the constraints. From figure 5.8 we find:

- The most reliable configurations are the unconstrained flip-chip assemblies $K\theta u, x$ together with the adhesive groups without displacement $E\theta x$ and $S\theta x$, followed by groups featuring displacement and fixation.
- For the groups without displacement and fixation on a thick board: The siliconeepoxy adhesive group $E\theta x$ shows a slightly better reliability than the corresponding

unconstrained chip K0x. This is a quite unexpected result. The silicone adhesive S0x, however, comes last for the considered configurations.

- A displacement (with simultaneous fixation) considerably increases bump creep strain and hence reduces reliability.
- For the same interface material the larger displacement produces the lower reliability.
- Board thickness is a dominant factor. Thin boards prolong lifetime throughout all configurations.
- Groups using a gap-filler (foil) prove slightly more reliable than those with an adhesive. The epoxy-silicone adhesive yields slightly better results than the silicone-based one. A distinction between the gap-fillers is hardly possible.
- A convex curvature of the chip (E2Mu) seems to produce slightly better results (cf. E2Au). This, however, is changed when a thick board is used (cf. F2Mx).
- The influence of a force cannot be judged at this point yet. We will come back to do this later in this work.

The influence of the individual parameters is extracted and again depicted in figure 5.9.

The dominance of the board thickness and fixation after the transient response of the first cycle indicates that eventually flip-chip reliability is again mainly governed by the mismatch between chip and board. Additional mechanical loads like a displacement or the type of interface material do exert a smaller influence, but their effect is amplified by a fixation or a thicker board.

The increase in creep strain of the constrained groups with respect to the normal flip chip is largely due to an increase in shear strain ε_{xz} and ε_{yz} . The latter component assumes smaller strain due to a more favourable position (less close to the chip edge as seen in figure 5.6) of the bump within the chip. The same argument applies to the always smaller shear strains of the inner bump, an effect which is stronger for groups with mechanical loads and most pronounced for the foil groups, then the silicone groups and least for the epoxy-silicone groups. This tendency is correlated to the movability of the die during cycling which is constrained most for the epoxy-silicone adhesive as depicted in figure 5.14. The normal component ε_{zz}^{cr} shows the inverse behaviour. The inner bump yields slightly higher values. This illustrates that the die does not deform exactly parallel to the board but that its centre has a higher out-of-plane amplitude than the corners. Still the differences are only minute. As far as the equivalent creep strain is concerned though, $\bar{\varepsilon}_{\#2}^{cr} \geq \bar{\varepsilon}_{\#6}^{cr}$ from figures 5.7 and 5.8).

Further, the ε_{zz} component hardly shows any dependence on the applied loads and is mainly caused by the comparatively large thermal mismatch between bump and underfill $(\alpha_{UF}(T < T_g)) = 44 \ ppm/K)$ and solder $(\alpha_{SnPb}) = 24 \ ppm/K)$. For the unconstrained chip $K\partial u, x$ this contribution is the dominant part, a tendency which has already been pointed out by [24]. As the soldermask with an even higher CTE of $\alpha_{SM}(T < T_g) = 72 \ ppm/K$ fills one third of the gap between chip and board this tendency is even aggravated [30]. In

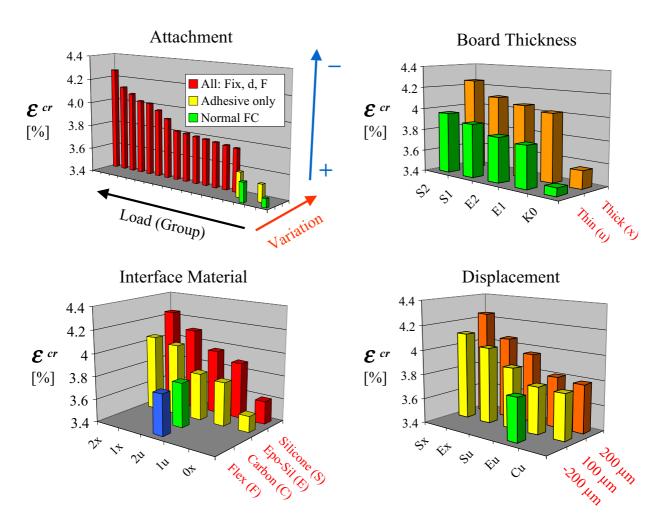


Figure 5.9. Ranking according to individual parameters. Creep strain is averaged over both bumps.

figure 5.10 the effect of underfill-solder mismatch is illustrated for the assembly used in this work and a matched system for comparison.

In figures 5.11 and 5.12 the evolution of the creep strain components over the period of the first and second cycle is again depicted for two representative groups, the unconstrained chip $K\theta u$ and a carbon-foil configuration with medium loads C1Bu. For the sake of clarity the strain is zeroed after the first cycle.

Here we see that the application of external loads does indeed manifest itself in a large increase of the shear strain components with respect to to the unconstrained case $K\theta u$.

This is true for all loaded groups (figure 5.7): Shear stain becomes the ranking-governing tensor component for all groups with displacement and fixation. For the unconstrained flip-chip assembly on the contrary the normal strain represents the governing part for the equivalent creep strain. This tendency prevails also for the second cycle (figure 5.8).

But from the first to the second cycle a convergence or relaxation behaviour is observable resulting in a redistribution of creep strain as follows: First, all creep strain components

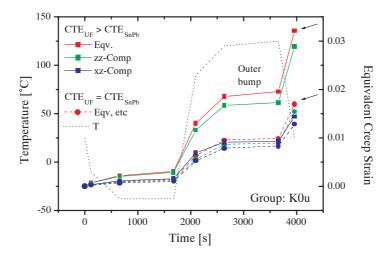


Figure 5.10. Effect of the underfill CTE on creep strain. A thermally matched solder-underfill system largely reduces (normal) creep strain thus improving reliability.

display an increase at low temperatures (cf. figures 5.11 and 5.12) irrespective of the group. Second, at high temperatures the normal component ε_{zz}^{cr} still rises for all groups, and largest values of this component are obtained for the unconstrained chip (cf. figure 5.8). All loaded groups, however, feature lower values of normal creep strain. Third, groups with a displacement $d \neq 0$ display shear strain components which relax to lower values (see again figure 5.12). For groups with no displacement, however, there is no such relaxation as the graphs in figure 5.11 show. This is also true for groups which only feature a reverse side attachment by an adhesive like $E\theta x$ or $S\theta x$.

This redistribution of strain might be due to the viscoelastic properties of the underfill and soldermask as it appears in any group irrespective of loads and board-properties (elastic/viscoelastic). It is furthermore in accordance with the respective stress components plotted in figure 5.13. Higher stress goes along with less creep as the solder displays more elastic behaviour at this point at low T and does not transform the stress into inelastic deformation. The slight increase of creep strain at low temperatures for the second cycle might be due to local plastic deformation of the pad. Interestingly the stress does not go to zero not even at high temperatures. The movements have not come to rest in the package. Due to the mismatch in CTE with the underfill, the bump is always under compression during the cycle.

Still the unexpectedly good result of the epoxy-silicone adhesive group without loads E0x needs explaining: All loads and constraints *increase* the shear components of bump creep strain, but slightly *reduce* the normal component with respect to the values for the unconstrained chip K0x (see figure 5.8). Due to the underfill-solder mismatch, this normal component is extraordinarily high ($\varepsilon_{zz}^{cr} \approx 0.03$) and dominates in this case the equivalent creep strain on which the ranking is based. So although the constrained group E0x features larger shear strain and should therefore be less reliable, this is compensated by a larger normal component for the free group K0x. Interestingly, the constrained group can so outdo the free chip K0x with respect to reliability.

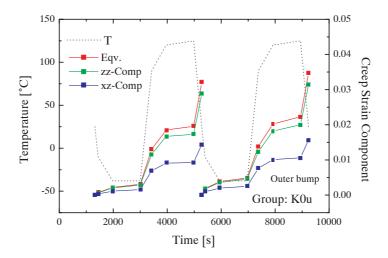


Figure 5.11. Creep strain components' evolution for unconstrained chip K0u, bump #2.

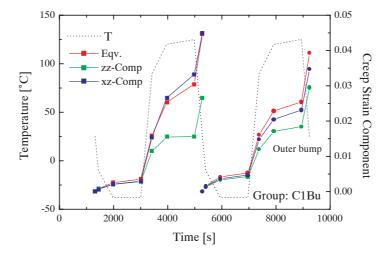


Figure 5.12. Creep strain components' evolution for loaded chip C1Bu, bump #2.

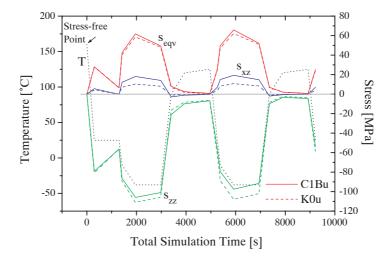


Figure 5.13. Corresponding evolution of stress, bump #2.

This result for E0x, however, cannot be generalized, as for a (normally used and technically relevant) matched solder-underfill system the shear strain part would dominate and the ranking would favour the unconstrained chip K0x as expected.

5.2.2 Correlation of Curvature and Creep Strain

The curvature (measured as deflection k) has been used as tangible and accessible quantity for the global or macroscopic behaviour of the flip-chip assembly to determine its current state under mechanical and thermal loading. Its measurement did serve for fine-adjustment of the simulations. For this reason it is again used in the following to examine if there is a correlation between the curvature itself and the creep strain. The next two pages show the simulated movement of the chip diagonal over the first two cycles. Each curve (figure 5.14) corresponds to a certain T(t), where the full cycle is divided into seven load cases, i.e. we deal with eight curves. The corresponding accumulated creep strain averaged over both bumps per load step is given by the graphs in the lower right diagram. Chosen were five groups, the unconstrained chip $K\theta u$ and the groups having the same displacement of $|d| = 200 \ \mu m$ and the same board thickness and external force (save E2Mu – due to convex bending), but feature different thermal interface materials. A red arrow marks beginning and end of the cycle. All graphs do have the same scale.

First of all the qualitative difference is remarkable. Different materials constrain the movement of the chip to a different extent. The 'free' chip $K\partial u$ (a) moves as predicted since it has been the object of study and calibration in the preceding chapters. As expected, the harder epoxy-silicone adhesive allows hardly any movement, whereas softer adhesive or gap-filler do. The directional tendency to curve is prescribed by the sign of the displacement: For the group with negative displacement (b) the curvature results in a convex state of bending at nearly all temperatures, whereas for the group with positive displacement the chip bends concavely (d). Here it is evident that the curvature is not proportional to k any more as was supposed for the chip without adhesive (cf. section 4.3.5 or figure B.6). For the carbon foil group (c) the mechanical load causes a large increase in curvature with respect to to (a). The silicone adhesive (e) displays an interesting reaction: At high temperatures the chip hardly 'feels' the adhesive due to its very low E-modulus. This changes at low T since the silicone adhesive exhibits a rise in E and develops considerable strain due to a very high CTE ($\alpha = 175 \ ppm/K$) during cooling down. This flattens the chip. This extra movement the chip has to undergo each cycle reduces its reliability with respect to groups with similar loads as can be seen for the interval in which the temperature is ramped up (f). This effect is even larger in combination with a thick board.

As can be seen in all graphs save (a) the chip does not return to its initial state. This 'open' loop is indicated by red arrows and is typical for all groups with a non-zero displacement $d \neq 0$. Only the movement of the unconstrained chip $K\theta u$ (a) and $E\theta x$ in figure 5.31 (e), both of which do not feature a displacement, has converged after the first cycle (green arrow).

Therefore a second cycle is simulated and its results presented in figure 5.15. After the second cycle the movements of the chip diagonal do indeed form closed loops and become periodic as is to be seen again from the green arrows. This is also true for the creep

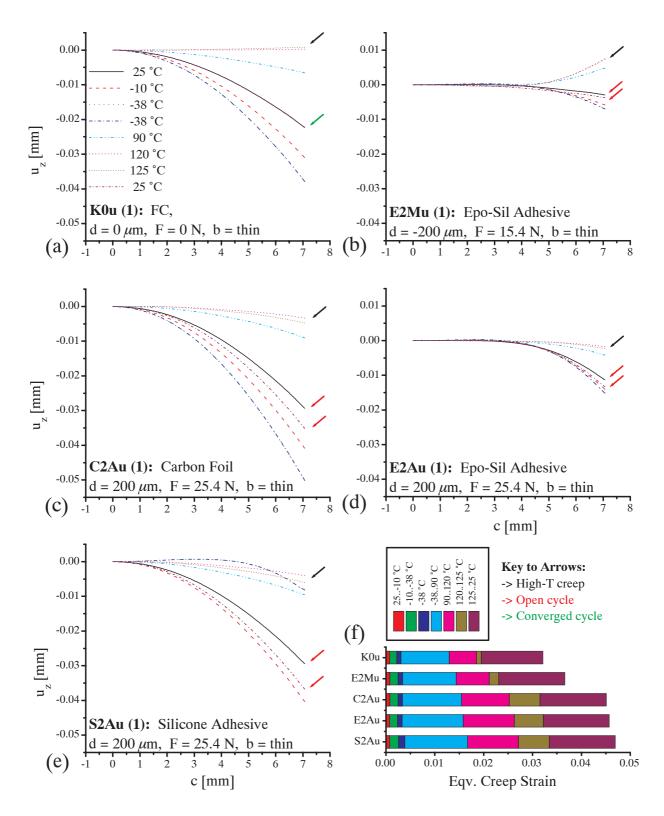


Figure 5.14. Movement of chip diagonal over the period of first simulated cycle. The corresponding equivalent creep strains (averaged over both bumps) per load step are added up in (f). Note the large effect of loads (b) and interface medium (c-e) with respect to (a). A red arrow indicates beginning and end of an 'open' cycle, a green arrow a converged cycle. Black arrows denote the critical creep phase at higher T.

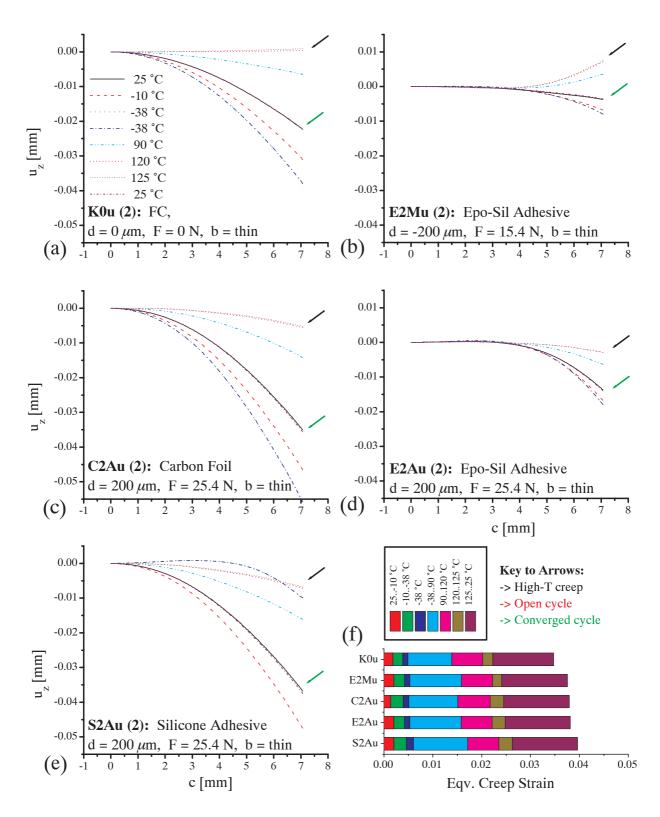


Figure 5.15. The same configurations but for the second simulated cycle. Again green arrows indicate closed loops now and hence a stabilized, converged system for all groups.

strains which assume lower values for the constrained groups. This is an important result: The system has relaxed and accommodated to the given loads, although the characteristic differences due to the interface material are still prominent.

However, these differences in deflection amplitude seem not to influence the creep strain of the solder to an expected extent. Apparently, the low-T phase of the cycle, where there is most difference in the curvature of the contemplated groups, is of no relevance for the creep strain. Creep needs high temperatures to be activated. This phase is crucial for the accumulation of creep and hence damage.

At high temperatures the chip essentially assumes a state of lower curvature and differences due to the different interface materials are not as pronounced as at low T. Therefore the identically loaded groups (c-e) do display similar creep strains, small differences are may depend on the way the interface material constrains the curvature of the die. Thereby the sign of the curvature seems not to play an important role (b).

This leads to the following observation: Large creep strains are caused by a continuing movement of the die (black arrows in first cycle) or remaining (constrained) curvature at high temperatures which differs from the unconstrained case (a), i.e. the unconstrained chip which yields the highest reliability. Here only chip and board determine the curvature of the chip.

Every external influence seems to increase creep strain. Thereby also the sense of bending (concave or convex) seems to be of no importance. This is not intuitive at first glance, but due to the viscoelastic properties of underfill and soldermask which allow a relaxation and consequent convergence of the cycle at high temperatures $T \approx T_g$ the chip and with it the bump may deform until they assume a new equilibrium position (green arrows) about which they oscillate driven by the thermal cycle T(t). The bump's creep strains develop eventually only through a relative, thermally induced deformation. This is evident also from a mathematical point of view: The strain depends only on the derivative of the deformation, not on the deformation itself. In order to assume this new equilibrium though, the bump has to undergo this transient period of larger creep of the first cycle.

5.2.3 Structural Distribution of Creep Strain inside Bump-Volume and Consequences for Averaging

This large increase in shear strain for the mechanically loaded groups manifests itself also in the structural distribution over the bump volume. This phenomenon is shown in figure 5.16. For a mechanically unconstrained chip $K\theta u$ a well-known structure (a) [25] evolves. This structural distribution of strain, shaped like an X, develops as the chip bends down at low temperatures and up again at high temperatures, each time giving rise to one 'leg' of the X. This particular structure is obviously characteristic for a situation where the normal strain dominates over the shear strains.

However, this structural feature is lost when mechanical loads are applied to the chip and shear strain wins over normal strain. Again we use group C1Bu (carbon foil, medium loads, thin board) for comparison. A rather layered structure develops (b). As the creep strains per cycle become stable, the equivalent creep strain assumes lower values and a

more X-like band structure reappears (c) due to the earlier mentioned redistribution of strain (see also figure 5.12).

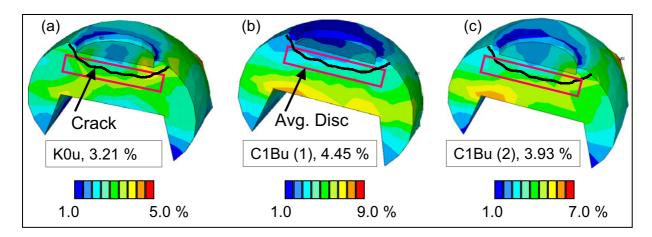


Figure 5.16. (a): Typical X-shaped structure after one thermal cycle for a bump within an unconstrained chip K0u. (b): Flip-chip bump with reverse side attachment exemplified for C1Bu: The X-band structure is overlaid by a layered structure due to an increase in the out-of plane shear components. Creep strains are averaged over a disc-shaped region (red box, cf. figure 4.4) where fatigue cracking occurs. (c): Stabilized creep strains of second cycle.

When it comes to evaluating the creep stain, the need for averaging over a certain volume has already been stressed (see section 4.1.3). In order to capture the points of maximum creep strain and its local variations in the region where the crack develops (red frame), the averaging region has to extend over the diameter of the pad at a certain thickness. At the same time numerical artifacts at corners have to be excluded. The best shape to accomplish this is an oval disc as depicted in figure 4.4. Its dimensions have been obtained in order to yield the maximum value for the case of the unconstrained flip-chip figure 5.16(a). The creep-strain distribution in the volume is still found to be reasonably homogeneous.

For comparability of the results, the averaging region has been chosen identical in all configurations as also in all cases the bump cracks below the pad. This has been confirmed by experimental investigation (see e.g. figure 5.24). So the red framed region constitutes the zone of the damage path across the bump.

5.3 Results of Experimental Analysis

Now the results predicted by the simulation are now to be verified by the experiment. The analysis of the experiment consists mainly in detecting bump failure as a function of the numbers of cycles. This is done by electrical resistance measurement and verified by cross-sectioning of the respective bumps by metallographic means. The recorded values are shown to obey a Weibull-distribution and the individual groups do show a ranking as a function to the applied loads. Analysis techniques like ultrasound microscopy and

metallographic sectioning again were employed to check for delamination and local defects, voids or microstructure coarsening.

5.3.1 General Inspection of Specimens After Thermal Cycling

A general inspection after each stop during thermal cycling was carried out. This meant disassembling the test-specimens to look for delamination of the adhesives, die crack, tightened nuts and overall integrity of the samples. At each stage of cycling (every $\Delta N = 250$ cycles) one sample per group was held back to perform this check.

Here it was found that nearly all flexible foil groups 'F' had a large number of dies cracked due to a unforseen reduction in the thickness of this thermal interface material. As a consequence the critical displacement load was exceeded which caused too large a curvature of the chip and then die crack. This could be confirmed by FE-simulations making use of the surface stress as fracture criterion. Only three groups remained with enough samples to yield statistically meaningful results to be included in the analysis. They are henceforth marked with an asterisk. Die crack was not observed in any other group.

All adhesive groups were impeccable in that no delamination of the adhesive at either interface, plate or chip, was found. This was detected by optical inspection under tensile load and finally by twisting off the die from the plate where the silicone adhesive still stuck to either surface and the epoxy-silicone left a homogeneous mark on the aluminium plate.

The remains of the adhesive were removed and the chips underwent a ultrasound examination to look for delamination. Here only minor, very localized delamination at the solder-passivation interface was found. As for the nuts which are to secure a tight joint between the board and the plate no decrease in strength was noticed.

5.3.2 Determination of Bump Failure: Correlation Single Bump and Daisy Chain Resistance and Verification by Metallographic Means

A computer-controlled resistance measurement was carried out on all chips at regular intervals. Therefore the test-specimen is inserted into a needle-pin adaptor (see figure 5.17) which conducts single bump and daisy-chain measurements, each of which featuring advantages and disadvantages as described in section 4.4.1.

A program (MS-Excel Macro) automatically measures the resistance of sixteen single bumps and the daisy chain. Failure is detected according to a certain threshold value scheme which is explained in table 5.3. This reflects a consistent relationship between the two measurement types and is underpinned by metallographic sectioning confirming the through-crack in the bumps.

In order to carry through a correct statistical analysis for the failure behaviour of the bumps a maximum of information is needed from both kinds of measurements. However, there is some difficulty in determining the exact point of failure for the daisy-chain as it represents an overlay of the failure of many bumps connected in series. Therefore it is first of all



Figure 5.17. Computer-controlled measurement of bump resistance. To the left the multimeter and the relay box for switching between the individual bumps can be seen. Inset: Needle-pin adaptor. The plate fits in neatly between the needles.

important to establish a correlation. This is done in a self-consistent way as outlined below.

Single Bump Failure

The evolution of the resistance is illustrated graphically in figures 5.18 and 5.21 for the single bump and the daisy-chain respectively. Here arrows mark the points of failure and the evolution of the resistance at failure is illustrated. The single bump resistance rises gradually by ∂R_{SB} per ΔN , an effect which is attributed to gradual ageing: Growing intermetallics, accumulating crystal defects and coalescence of microcracks caused by low cycle fatigue (cf. section 3.1.4 and [108]) may contribute to a slight increase in electrical resistance through reduction of the current carrying volume in the sense of equation 3.20. Only a 'catastrophic' event can be counted as failure where the resistance rises sharply by nearly one order of magnitude. Hereby the failure sometimes announces itself by an earlier rise is resistance which proves not fatal yet. It usually stays below around $R_l \approx 20 \ m\Omega$ then. An open circuit seldom exceeds an upper value of $R_u = 1 \Omega$ at failure (as to be seen in figure 5.18) at room temperature due to the bump being under compression. Still, the best way to detect a fatal damage unambiguously is by making use of the increase with respect to to the last measured value (see table 5.3). This criterion traps the fatal event best. The subsequent number of cycles is then taken as number of cycles to failure. This is in agreement with the analyses presented in [37] or [109] which use an absolute value of $R > 100 \ m\Omega$ as failure criterion for SB failure. In our case, however, bumps could be shown to have failed already at absolute values above $R_c \approx 25 \ m\Omega$.

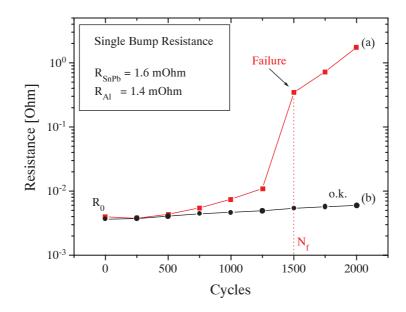


Figure 5.18. Single bump resistance vs cycles: Bump failure (a) at $N_f = N_{SB}^i$ cycles is unequivocally detectable by a sharp rise in electrical resistance which signalizes a 'catastrophic' event (arrow). Usually this is preceded by a steeper slope of the curve than for an intact bump (b). This rise in resistance can be experimentally correlated to crack propagation. The inset shows the composition of the resistance: solder vs Aluminium (leads).

Correlation Between Single-Bump and Daisy-Chain Measurements

	o i			
Item	Single Bump Measurements (SB)	Daisy Chain Measurements (DC)		
Number of Bumps $n_{SB} = 8 \times 2$ at statistically equiv-		$n_{DC} = 112$ out of 148 (save SB)		
	alent positions	bumps contacted in series		
Resolution	Very good due to measurement	Smeared out due to overlay of		
	of single bump. Therefore locally	failure of many bumps. Not lo-		
	sensitive.	cally sensitive but evaluates inte-		
		gral value over chip.		
Sensitivity	Ratio $\frac{R_{SnPb}}{R_{tot}} = 0.53$	Ratio $\frac{R_{SnPb}}{R_{tot}} = 0.083$		
Accuracy	Very good due to four-point cur-	Blurred. Error $\delta_{R_{DC}} < 100 \ m\Omega$		
	rentless resistance measurement.	due to two point resistance mea-		
	Error $\delta_{R_{SB}}$ < 1 $\mu\Omega$ (Resolution	surement affected by drift in relay		
	of Gauge)	contact resistance.		
Normal value	$\partial R_{SB} \approx 0.5 \ m\Omega$ \rightarrow	$\partial R_{DC} \approx n_{DC} \partial R_{SB} + \delta_{R_{DC}}$		
Threshold value	$\partial R_{SB} > 5 \ \partial' R_{SB}$ \rightarrow	$\partial R_{DC} > 5 \ \partial' R_{DC}$		
or	$\partial R_{SB} > \partial R_{SB}^C = 25 \ m\Omega; \qquad \rightarrow$	$\partial R_{DC} > n_{DC} \partial' R_{SB} + \delta_{R_{DC}} +$		
		$+\frac{n_{DC}}{n_{SB}}\partial R_{SB}^{C} = 375 \ m\Omega$		

Table 5.3. The single bump results are used to establish a correlation to the daisy-chain values. We define: $\Delta N = 250$ (Cycles); The increase in resistance per ΔN ; $\partial R = R_N - R_{N-\Delta N}$; $\partial' R = R_{N-\Delta N} - R_{N-2\Delta N}$.

This fact can be confirmed by intersections through the bump as depicted in figure 5.19. Bumps (a) shows no cracks whereas (c) and (d) show a clear crack accompanied by many micro- and mesocracks across the entire cross-section of the bump. Bump (b) is just becoming critical and its crack is already half the way through.

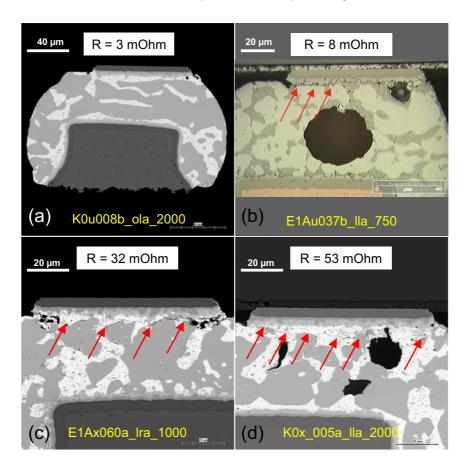


Figure 5.19. Different bumps from various test-groups and their resistance. The bump is specified by the notation: GROUP/CHIP/POSITION/CYCLE. Magnification is 500× and 1000× respectively. Red arrows indicate cracks.

Another test supports this threshold value R_c : The samples were measured, heated up to T=125 °C, measured again, and remeasured an other time at room temperature. The resistance went up and returned to exactly the same value if the bump was intact. A cracked bump did not so once it exceeded this value of $R_c \approx 25 \ m\Omega$. Interestingly pure mechanical unloading of the chips (disassembly of the test-specimen) did not show this effect. This is due to the fact that at room temperature the solder bump is always under compression (see figure 5.13).

The dependence of the resistance on the cracked area is simulated and sketched in figure 5.20. For a single bump of height H and initial cross-section A_0 (= area of the pad) the overall resistance is composed of a solder R_{SnPb} and a non-solder fraction R_{Rest} which are calculated to account each for nearly half of the total resistance. Based on the assumption that a crack zone of area A_{ϕ} and height h reduces the effective current carrying solder

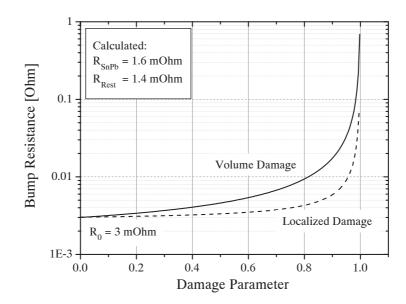


Figure 5.20. Calculated single-bump resistance as a function of crack zone extension given by a damage parameter $\phi = A_{\phi}/A_0$. The upper curve assumes a large damage zone of extension h equal to the solder gap width $H = 47 \,\mu\text{m}$ (cf. figure 4.28) whereas the lower represents a local cracking (h=0.1 H) of the solder bump below the pad.

volume of the bump the resistance rises as a function of the extension ϕ (or damage parameter as in equation 3.20) of this zone according to:

$$R(\phi) = \varrho_{SnPb} \left(\frac{h}{A_0(1-\phi)} + \frac{H-h}{A_0} \right) + R_{Rest}, \tag{5.2}$$

where the specific resistance for eutectic solder was taken to be $\varrho_{SnPb} = 16 \ \mu\Omega \ cm$ [65] at room temperature.

As one can derive from the curves, however rough a guideline they may seem, a soaring resistance means in any case a severe damage in the bump. As can be seen from the intersections the cracks are multiple and microscopic encompassing an extended damage process zone around them before they finally merge to cause fatal rupture. This is in accordance with the damage hypotheses of thermally induced low cycle fatigue in ductile materials where a weakened, coarsened zone precedes fatal failure [64] as presented earlier in this work. There may be, however, other metallurgical changes contributing to the increase in resistance prior to fatal failure of the bump by fracture. Multiple cracks, oxidation at crack faces, point contacts or grain boundary effects can add to the effective decrease in area and increase in electrical path length.

Daisy-Chain Failure

When considering a typical daisy-chain response like those graphs in figure 5.21 the difficulty in determining the point of failure becomes obvious: Bump failure produces much less an effect in the overall resistance. In this respect graphs (b) and (d) do present no problem since they clearly testify a 'catastrophic' event. But many chains produce curves like (a) and (c). This is due to the low sensitivity (i.e. solder resistance to overall resistance ratio) and the considerable measurement inaccuracy caused by the two-point measurements which are unfortunately affected by the non-constant contact resistance of needle to pin and also the relays in the switching box. This is responsible for an intrinsic error of $\delta_{R_{DC}} = \pm 50..100 \ m\Omega$.

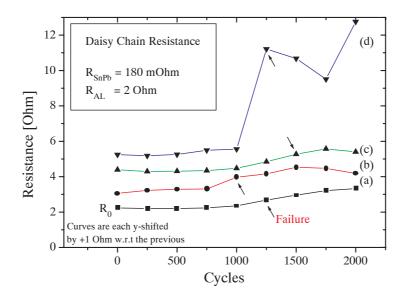


Figure 5.21. Some representative examples (chip a-d) for daisy-chain measurement results: The number of cycles to failure (arrow, $N_f = N_{DC}^i$) is more difficult to detect but consistent with the experiment and correlated to single bump results.

Therefore the insights gained with the single-bump measurements are now used to develop a threshold criterion for the daisy-chain that is consistent with experimentally verified bump cracking. This is in principle a straightforward extrapolation from the single bump criticality criterion to a larger number of bumps connected in series as is described in table 5.3. It was made use of the fact that a critical state must account for the gradual increase and – as experience from the single bump measurements shows – on average one bump in sixteen goes up by ∂R_{SB}^{C} which means failure of one bump. The error $\delta_{R_{DC}}$ has to be added.

The criterion given in the table is in good agreement with experimental results. Sectioning showed unequivocal fatal damage to at least one bump in every case. The value N_{DC}^{i} thus obtained for the daisy-chain is usually smaller than the number of cycles to first single-bump failure per chip N_{SB}^{i} (cf. figure 5.18) by a number N_{c}^{i} (cf. figure 5.21) for each chip where i is a chip-index. This result seems reasonable, since with a much larger number of bump involved the daisy chain is more likely to display bump failure.

Determination of Chip-Failure

A chip has failed when the first bump has failed. The corresponding number of mean cycles to failure \bar{N}_f for this particular event has to be found. A bar on top of the symbol signifies a mean value $\bar{N}_f = N_{50 \%}$.

A purely daisy-chain based evaluation can be ruled out for various reasons: First, the daisy-chain usually fails for all chips of a group within two or three subsequent measuring intervals ΔN . Two points do not produce a Weibull-fit and three produce a very vague result with a large scatter. It did not give rise to a meaningful and well-resolved ranking when put up. Second, the daisy-chain value \bar{N}_{DC} provides no local information which makes it difficult to correlate it to the computational strains of a specific bump which depend very much on bump position (distance to neutral point).

The next possibility to rigorously evaluate \bar{N}_f would be to determine \bar{N}_{SB} based on all single bumps per group $n = n_{SB} \times n_{ch}$ and evaluate the probability for the above event \bar{N}_f for the number of bumps in the daisy chain n_{DC} (n_{ch} is the number of chips in the group) according to

$$\bar{N}_f = \bar{N}_{SB} \left(\frac{1}{n_{DC}}\right)^{\frac{1}{\beta}} \tag{5.3}$$

This is derived in the appendix A.4. The method, however mathematically correct it may be, has several practical shortcomings. First, the number of single-bump failures is small³ which requires far-reaching extrapolation to $N_{50\%}$ which produces a large uncertainty and is not recommended [110]. This is further aggravated as it is difficult to fit the single bump failure data to a straight line (cf. figure D.1 in the appendix). Then, our contemplation requires that necessarily all bumps display equal ageing behaviour which is of course not true: Bumps closer to the corner fail earlier. This manifests itself in a lower effective number of bumps $n_{eff} \approx 30 \ll n_{DC} = 112$ which has to be introduced to bring \bar{N}_f to a meaningful value of the order of $\bar{N}_f = 1000$ which is at any rate postulated by the daisy-chain values for the normal flip-chip group $K\theta u^4$. Further, n_{eff} may vary from group to group and so this again is no tenable approach and furnishes only a tendency but no conclusive result.

Taking this into account the following approach is finally adopted: The first single-bump failure per chip is counted as chip failure. For chips where no single-bump failure occurred a group-averaged value for single-bump failure \tilde{N}_{SB} based on the corresponding daisy-chain \tilde{N}_{DC} value of the chip in question was calculated:

$$\tilde{N}_{SB} = \tilde{N}_{DC} + \tilde{N}_c, \tag{5.4}$$

where a mean shift $\tilde{N}_c > 0$ is evaluated for each group according to:

$$\tilde{N}_c = \frac{1}{n_f} \sum_{i}^{n_f} N_{SB}^i - N_{DC}^i, \tag{5.5}$$

where the tilde signify averaged quantities over all samples n_f in the group which have a single bump failure and i is an index. This self-consistent evaluation of \tilde{N}_c per group takes into account that the failure behaviour of the bumps differs from group to group and its values are printed in table D.1.

³The group $K\theta x$ shows the greatest percentage of single bump failures with $n_f/n < 20$ %. The average is $n_f/n \approx 10$ %.

 $^{{}^4}K0u$ happens to produce unambiguous daisy-chain failure. For comparison: $\bar{N}_{SB}=4806\pm900,$ $\bar{N}_{DC}=1020\pm200.$

This has great advantages: All chips of the group do contribute to the statistics and we obtain a well defined mean. The percentage of failure is defined for many values of N (usually 5 up to 10) which allows a good Weibull-fit. The statistical evaluation is carried out for bumps at specified locations which enables a direct reference to the corresponding bump in the FE-model. This method proved successful also in that it produced the best Weibull fit as can be seen in figure 5.22.

5.3.3 Ranking of Configurations: Statistical Analysis and Weibull-Distribution

We assume the fatigue data to be Weibull-distributed. Therefore we take the data obtained for bump failures as percentage of first single bump failure per chip of the total number of chips in the group. Here we do not distinguish between inner and outer bump, since the slight domination of the outer bump was not deemed significant enough. This value was then plotted versus the corresponding number of cycles to failure according to the Weibull-Distribution as reviewed in section A.4

$$F(N) = 1 - e^{-(\lambda N)^{\beta}} \tag{5.6}$$

where $\lambda^{-1} = N_{63\%}$ is the characteristic number of cycles to failure and β is the Weibull-exponent and function gradient in the (y-axis double-logarithmic, x-axis logarithmic) diagram. Therefore Weibull-distributed data appears as a straight line in the diagram [110, 111].

This can be seen in figure 5.22 where the plot is depicted for some representative groups. The characteristic lifetime $N_{63\%}$ can be read from the graph.

This is done for all experimental groups. The mean value of cycles to failure $\bar{N}_f = N_{50\%}$ needed for the Coffin-Manson relationship is then calculated by (see appendix A.4).

$$\bar{N}_f = N_{50\%} = N_{63\%} \Gamma_{(1-1/\beta)},$$
(5.7)

where Γ is the Gamma-Function.

When \bar{N}_f is plotted for all groups the ranking to be seen in figure 5.23 is obtained. The results are also summarized in tabular form in section D.2 in the appendix.

Also the experiment shows a dependence on the mechanical loads. Although the ranking is not as clearly resolved as for the simulative results, the outcome is for the most part consistent with the computational results quoted in section 5.2:

- Thin boards seem more reliable than thick boards, although with increasing loads this tendency becomes blurred.
- All mechanical loads and constraints reduce reliability.
- Foils seem better than adhesives. Thereby epoxy-silicone seems better than pure Silicone adhesive.

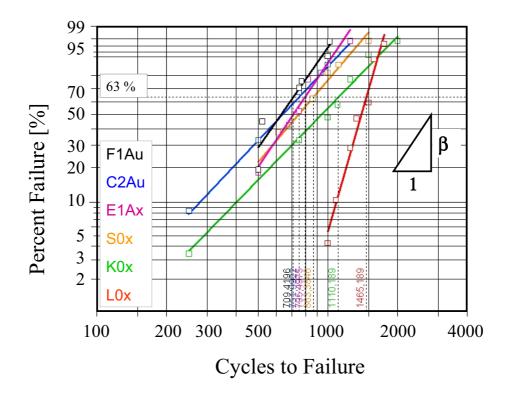


Figure 5.22. Weibull-plot for some representative groups. Highlighted is the characteristic lifetime at 63 % failure. The fit to a straight line indicates one single failure mechanism. Note the steeper slope (of gradient β) for the group containing voids (L0x).

- There is no significant dependence on the sign of the displacement (convex or concave bending).
- There is no significant dependence on the *value* of the displacement.
- There is no significant dependence on the force.
- A vacuum process has a negative influence on reliability or voids do have a positive effect (compare L0x (voids) to K0x (extracted voids)).
- There is no significant dependence on a second curing process.

The simulation resolves an effect concerning the displacement, whereas this result is blurred in the experiment. And unfortunately, many cross-relationships – especially those concerning displacement and force – were lost due to the die crack in most flexible foil groups . So in this respect one has to rely on the computational result.

This low resolution is a consequence of the remarkably early overall failure of the configurations. All values of \bar{N}_f do lie within one order of magnitude. This may be due to the following points:

• The solder gap between pad and land is very small $b = 47 \mu m$. So the bump experiences more creep strain which strongly depends on b.

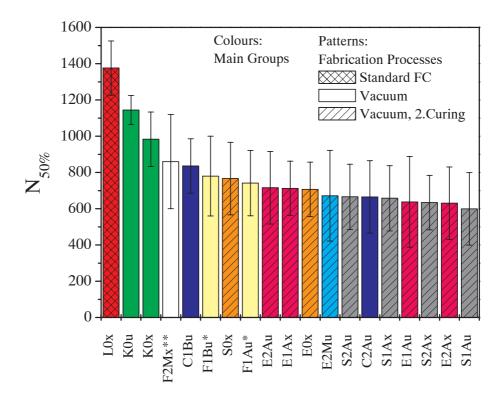


Figure 5.23. Experimental ranking of configurations. *Due to a shrinkage of the foil (see later in section 5.4.5) these two 'F'-groups actually support a higher displacement load than specified. **This displacement load is actually lower than specified.

- There is a prolonged creep phase due to the heat capacity of the attached heat spreader during thermal cycling.
- The underfill-solder mismatch ($\alpha_{Uf} \approx 2\alpha_{PbSn}$) for this specific underfill cf. figure 5.10 is quite large. This induces additional normal creep strain in the bump which reduces reliability.
- A potential initial damage (e.g. pre-crack) caused by non-standard processes during assembly as there were the extraction of voids under vacuum (or a second curing process).
- Last but not least the geometric features of the bump, a small pad and the resulting 'shoulder' could be a reason for faster fatigue cracking along the pad or earlier crack initiation around this shoulder.

This might also be an explanation for the unexpectedly low reliability of the adhesive groups without mechanical load $S\theta x$ and $E\theta x$ for which a value close to the unconstrained chip $K\theta x$ was predicted by simulation.

The best group is undoubtedly the unconstrained assemblies L0x, K0u, K0x. As expected, the thin board (-u) produces higher reliability than the thick board within a group [52]. Still, L0x, K0x should produce identical results. Let us therefore have another look on the preparation of the samples, which differ in two points:

Not all chips have seen the same fabrication processes during the assembly. A potential dependence may exist and therefore this difference is encoded in the patterns of figure 5.23. L0x has undergone the standard flip-chip processes and incorporates voids (cross-hatched). All other groups have seen a vacuum treatment described in section 4.4.3 and are depicted without hatching. The singly hatched groups are all adhesive groups which have therefore seen a second curing process.

There is also an indication that L0x displays an ageing behaviour different from the others since its Weibull-exponent $\beta_{L0x} = 7.55$ (see table D.1 in the appendix) is about twice the ones of the remaining groups. If this is caused due to the presence of voids or due to an absence of a vacuum treatment is impossible to say since there exists no cross-check. Values for $\beta \in [2;4]$ have also been reported in [23] to by characteristic for thermal low cycle fatigue of eutectic tin-lead solder. Values in this range signify on average a quadratic failure rate $\lambda(N) \sim N^2$. For all groups though the values lie to a very good approximation on a straight line from which it can be concluded that there is only one single failure mechanism (a second would cause a kink in the curve).

For this reason a second curing process is not likely to have caused any harm. The respective groups are not conspicuous among the others in figure 5.23 and their failure-rates lie among the others. It remains to verify if the vacuum treatment did induce any initial damage. In order to explain this deviation one has to look on some intersections of the bump.

5.3.4 Solder Bump Failure and Effects of Vacuum Treatment

In figure 5.24 bumps representative of their configuration have been chosen for comparison.

With respect to the 'as cast' solder bump (a) a second curing e.g. for the adhesive coarsens the solder (c). This is a phenomenon [43,64] typically observed at high temperatures. Here, $T_c = 160$ °C. It does, however, not induce any damage. Clearly visible on the contrary is the initial damage caused by the vacuum treatment (b). Although this process does eliminate large voids as seen in figure 4.31, it leaves behind gaps or cavities around the pad at the preferred location of the voids before their extraction under vacuum. Although the temperature is well above liquidus, the void does apparently not vanish with a wettable surface which would allow the solder to close the gap. These gaps are seen in nearly all bumps for all groups which underwent the vacuum process.

This can be seen in (d) where the void seems to be trapped in being sucked away by the vacuum. All groups which have undergone this process do show these gaps. It could well be that the comparability in terms of an identical initial preparation is hence reduced. Unfortunately this initial damage was not detected until the whole experiment was carried through. In this respect it produced exactly the effect it was meant to eliminate.

The bump finally cracks below the pad (f). This is so for all groups and no dependence of the loads on this behaviour is detectable. Interphase and intraphase cracking is observable in most cases. Fatigue cracking evolves gradually and due to merging of many microcracks which leave behind a 'crumbly' structure of a certain bandwidth. The gaps which are left behind by the vacuum process seem to be involved in the cracking process and as they reduce the effective cross-section it may be that they promote failure rather than

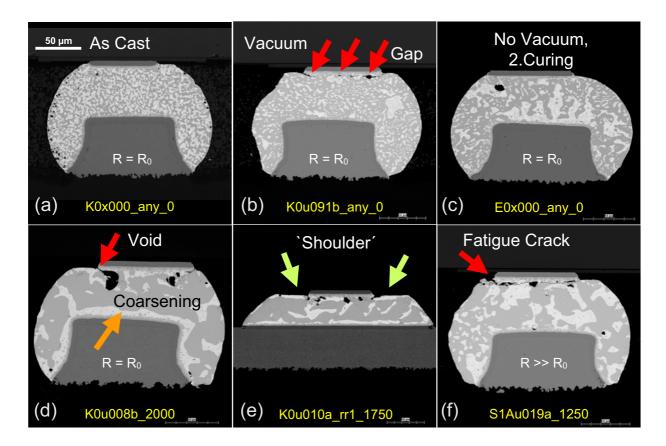


Figure 5.24. Solder as cast (a). Zero cycles: Initial damage due to extraction of voids. This process leaves behind gaps (b). A second curing process (no vacuum) only coarsens the solder (c). 2000 cycles: Remaining voids. Note the channel and the extreme coarsening (d). Side view of bump. A 'shoulder' forms at the passivation (e). 1250 Cycles: Fatigue cracking (f).

reduce it. Their cross-section area passes as already cracked path length. This has already been mentioned [105]. Big round voids which are far off the crack zone near the pad (as depicted in figure 5.19 (b)) seem not to have any influence on bump cracking. This may be the reason for the group L0x having higher lifetime despite the presence of voids.

It may therefore be concluded that the vacuum process did cause some damage to the bumps which caused them to fail earlier, although they did still fail by low cycle fatigue cracking as can be inferred from the failure-rate common to all groups. As the problem occurred in all groups – and as far as could be told from sectioning in nearly every bump – it may be assumed that on average the bumps act as if they had an even smaller pad than they actually have. This is consistent with the strong dependence on pad size found in literature (see e.g. [98,99]).

Further, a huge amount of phase coarsening is seen at large numbers of cycles (d,e). This is attributed to the very small gap width of the solder $b \approx 47 \ \mu m$ and the prolonged high temperature creep phase due to the large heat capacity of the aluminium plate as depicted in figure 5.4. This tendency is confirmed by the high values of creep strain throughout all groups $\bar{\varepsilon}^{cr} > 0.03$.

5.3.5 Check for Delamination

It is well known that the interfaces of multi-layered assemblies are liable to delamination. Thereby cracks start near common points of bi- or tri-material interfaces due to high stresses which are characteristic at these point under thermal loading [112,113]. For elastic theory this feature exhibits stress singularities which represent numerical artifacts since real materials will yield at a certain stress [76]. Still high (peel-) stresses will act in these zones and are likely to cause crack initiation. Several critical points have been detected [28] as far as flip-chip assemblies are concerned and they will have to be checked for delamination since this will considerably accelerate bump fracture or may even become the dominant failure mechanism over solder fatigue [18,33]. This means that we would deal with a second failure mechanism that cannot be treated conclusively along with the Coffin-Manson relationship for solder but requires additional fracture mechanical means. Critical points are the chippassivation-underfill and solder-underfill interfaces. The damage likely to be caused by delamination depends on its location and its extension.

In order to check for delamination ultrasound microscopy was employed. The result is to be seen in figure 5.25.

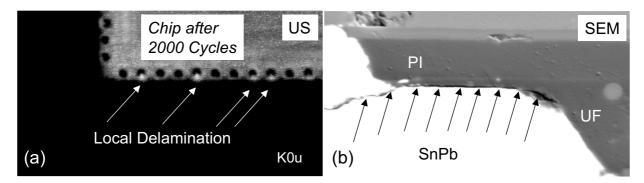


Figure 5.25. Ultrasound (US) pictures and verification by scanning electron microscopy (SEM). The white patches in the ultrasounds reveal local delamination, which occurs at the solder-passivation (SnPb-PI) interface. Due to its particular shape, the bump forms a 'shoulder' at this point. For the US-pictures an 230 MHz transducer was used.

Delaminated layers form a material discontinuity which causes a sudden change in the elastic modulus at this point of the assembly which reflects the ultrasound waves and is depicted as bright region on the sonographs. Bright spots can only be seen close to the pads at a few odd bumps and after about N=500 cycles (group-dependent). A new chip does not show any spots.

Metallographic examination revealed local delamination at the 'shoulder' which the solder bump forms at its top surface with the passivation (polyimide) layer. Obviously this combination displays no strong adhesion. The underfill-polyimide interface however seems impeccable. There was no delamination found in any group. It was known beforehand that this material combination had outstanding adhesive properties. On the other hand no indicative correlation between an early failure of a bump and the appearance of the white spot could be established.

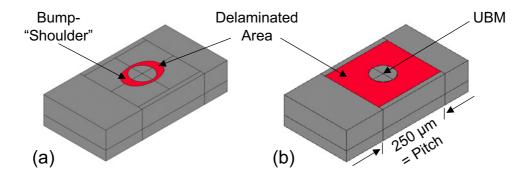


Figure 5.26. The delaminated area on the FE-model for small delamination at the 'shoulder' caused at the interface solder-chip (a) and for larger delamination of the size of one square pitch (b). The bump itself is surrounded by underfill and soldermask (grey) and located just below the UBM.

After this finding it has still to be made sure that this kind of very localized delamination does not interfere with the simulation. First, a delamination which only affects the solder interface to the polyimide (chip) as intended to mimic the above detected failure. The delaminated area is depicted in figure 5.26 (a).

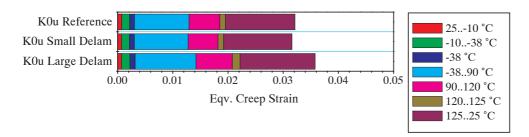


Figure 5.27. Influence of delamination on creep strain as predicted by simulation. Simulated is the first cycle for the unconstrained chip K0u. For details about the simulation refer to the appendix, section C.2.

For this case no negative influence on the solder was detected, on the contrary, a slight reduction of creep strain was noticed (see figure 5.27, K0u, small delamination). So this result agrees with the experimental observation. The corresponding FE-model is depicted in figure C.10 in the appendix.

In order to see if this tendency pertains, i.e. if a certain delamination could even be beneficial, a second, larger delamination between the underfill- and polyimide layer was simulated (see again appendix figure C.12). Hereby the ablated area was of square shape centred about the pad and measured one pitch (250 μ m) as shown in figure 5.26 (b). Here a small rise in creep strain could be detected in the centre of the bump, whereas on the outer rim of the bump there was a pronounced increase in creep strain. So larger delamination may indeed be harmful.

The delamination was simulated using a contact-target pair with sliding contact mode.

A model which considered delamination on other interesting surfaces between solder and underfill or underfill and chip was not attempted yet.

In any case we may be sure that we mainly deal with pure solder fatigue failure and are allowed to use the Coffin-Manson relationship which is based on this assumption.

5.4 Comparison of Experimental and Computational Results

Now the interpretation of the results in comparison between simulative prediction and experimental verification follows. This is done via the Coffin-Manson approach.

It is shown that the experiments agree well with the simulatively predicted results within 25 % accuracy. The Coffin-Manson coefficients are determined, some peculiarities commented on and extrapolations to some other interesting configurations are made.

As die crack did occur in some flexible foil groups a stress-based fracture criterion is evaluated and correlated to experiment and simulation.

Finally we draw some conclusions and venture an outlook to future activities.

5.4.1 Coffin-Manson Plot

The experimentally obtained results of figure 5.23 are now plotted as mean cycles to failure versus the simulated accumulated equivalent creep strain given in figures 5.7 (first cycle) and 5.8 (second cycle) respectively. (The values are explicitly given in the appendix in table D.1.) For each configuration the corresponding simulated strain was averaged over both bumps (#2 and #6 in figure 5.6). As there was no detectable difference in the experimental value of cycles to failure between the two bumps no separate analysis was made.

So the Coffin-Manson plot for the first simulated cycle can be seen below in figure 5.28.

For the indicated groups (see symbols in legend of figures) a best fit to the Coffin-Manson relationship

$$\bar{N}_f = c_1(\bar{\varepsilon}^{cr})^{c_2} \tag{5.8}$$

in order to determine the coefficient c_1 , c_2 was undertaken to calibrate the bump as a 'reliability sensor'. Thereby the void containing group $L\theta x$ has never been incorporated in the fit since it displays a different failure behaviour (different failure rate) due to a different treatment and existing voids. Also its value for the creep strain seems vague because voids were not considered by the simulation. For reasons of completeness its value for the creep strain $\bar{\varepsilon}_{L0x}^{cr} = \bar{\varepsilon}_{K0x}^{cr}$ was set equal to the corresponding group with extracted voids $K\theta x$. But it is for this reason not considered any further in this contemplation and the mark in the graph has been put in brackets.

The tendency, larger creep strain – lower reliability, is met. Two curves have been calculated to fit the data. The green, dotted curve features a specified exponent of $c_2 = 2$ which is the value most often reported (cf. section 3.1.5) in theory. It is here stated for

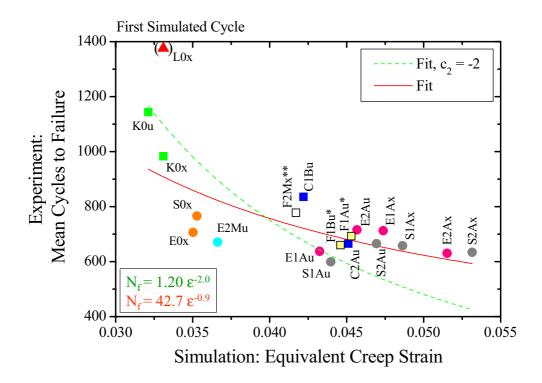


Figure 5.28. Coffin-Manson plot for first simulated cycle. The system features too low a Coffin-Manson exponent. The colour scheme resumes the one from figure 5.23. The shape of the symbols indicate identical process steps. The graphs of the CM-fit do not include L0x.

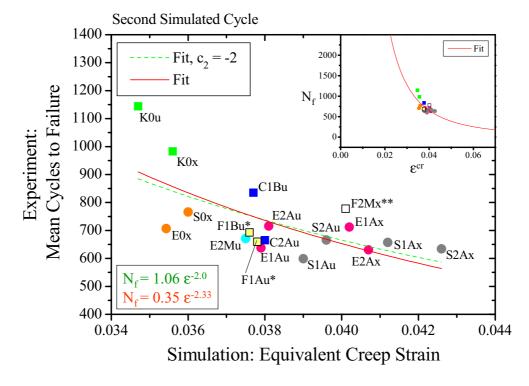


Figure 5.29. Coffin-Manson plot for second simulated cycle. The zoomed graph (inset) includes the origin. The dashed curve represents the fit with expected exponent $c_2 = 2$.

comparison. As can be seen the red curve, which includes all save L0x, is still far from this value. It exhibits a very low value for the Coffin-Manson exponent. But this is just an other manifestation of the transient response of the simulation during the first cycle as has been mentioned already and for the second cycle the curves do very nearly obey the theoretical prediction of $c_2 = 2$.

Several things are remarkable though: The groups E0x and S0x were expected to display better reliability since they did not see any further mechanical loading apart from being attached by an adhesive. Also the simulation does predict a high reliability. E2Mu was expected to show a low lifetime but the simulation of a first cycle does not reflect this yet. Also the 'gap' on the x-axis between the mechanically loaded and the unloaded groups to the left and the right of E2Mu need an explanation which could indicate a dependance on the make-up of the test-specimen, namely the thermal misfit between board and plate communicated by the fixation whenever a non-zero displacement is specified.

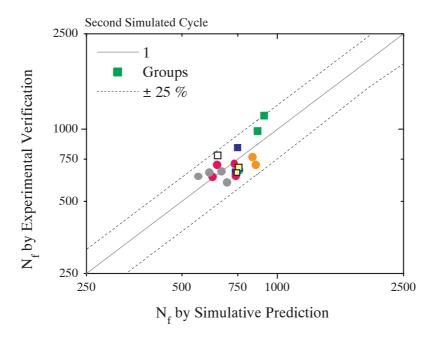


Figure 5.30. Correlation of lifetime prediction model with test data.

Many of these queries are resolved when analyzing the Coffin-Manson plot for the second cycle in figure 5.29 as it shows a much more consistent picture. The accommodation process of the chips to the loads already described earlier in section 5.2 shifts the equivalent creep strain (x-axis) of the loaded groups towards smaller values and the unconstrained chip $K\theta u, x$ experiences a slight shift to the right. The resulting fit reproduces a value of $c_2 = 2.33$, which is still close to $c_2 = 2$ (see section 3.1.4).

The discrepancy to the red curve is accredited to the seemingly low resolution of the experiment. An other explanation is that the simulated creep strain should actually be higher due to the pre-cracked bumps. As this would affect the loaded groups more strongly, the curve would be flatter, i.e. the exponent smaller. But as can be inferred from figure 5.30, the actual inaccuracy between simulative prediction and test still is around 25 %,

which is of the order of values found in literature (see e.g. [39], also 25 %). In this respect the encountered deviations are within the normally expected range.

Due to the high values of creep stain, which are mainly caused by the underfill-solder mismatch (normal creep strain component), all configurations are located within a region of the Coffin-Manson curve where its slope is rather gradual as can be seen from the inset in figure 5.29: For smaller values of creep strain one expects a much larger split up between the individual configurations and a much greater effect of the individual load variations in the experiment. The influence of the external loads in the simulation, a pronounced increase in the shear components of the bump creep strain, is additionally attenuated by the extraordinarily large normal component.

As a result one can state that the experiments do confirm the simulative predictions. The ranking given in section 5.2.1 can therefore be taken to correctly serve as calibration scale for the solder bump creep strain.

Still there remain some points to discuss. For instance the 'gap' of values which was originally between the loaded and unconstrained groups has been greatly reduced in the second cycle. This 'gap' can indeed be shown to be due to the fixation of the board to the plate and therefore a characteristic particularity of this very test-specimen. This can be seen when again we have a look at the curvature over the period of one cycle in the next section.

5.4.2 Effect of Fixation and Influence of Displacement

The first graphs of figure 5.31 (a) show a chip on a thin board with medium load attached by an epoxy-silicone adhesive (E1Au). At high temperatures the chip goes slightly convex. If the CTE of the aluminium plate (normally $\alpha_{al} = 23.5 \ ppm/K$) is set equal to the CTE of the board $(\alpha_{bd}(T < T_q)) = 11.5 \ ppm/K)$ for a test, then the result looks as in (b), the chip would not bend convexly, i.e. it is not stretched out by thermally induced stress in (a). The same result as in (b) is obtained if the fixation is loose (c), i.e. there is a displacement which holds the board parallel to the plate but allows sliding – a configuration which is easy to simulate but very difficult to adjust experimentally for reasons given in the last chapter. The two groups display also similar creep strains (f) which are both much lower than for the tested group (a). For a thicker board and corresponding loads (d) the force induced by the thermal mismatch is not as strong to flatten out the chip as in (a) and the for this case stiffer board maintains a concave state of bending. One has to consider that near T_g of the underfill the internal stiffness of the chip is greatly reduced. So the less compliant thick board causes the bump to creep more. As the large creep strains for this configuration show, a fixation has to be considered harmful although the chip accommodates to it in the following cycles.

The effect of the presence of the fixation is so large that it overshadows the influence of the actual value of the displacement, a tendency which is only apparent in the convergence limit of the second cycle. This is predicted by simulation in figure 5.32, where this is exemplified for the silicone adhesive groups which feature two different displacements ($d_1 = 100 \ \mu m$ and $d_2 = 200 \ \mu m$) once with fixation and once without (loose). Although there is a tendency that larger displacements (this results in a larger curvature) reduce lifetime, this cannot

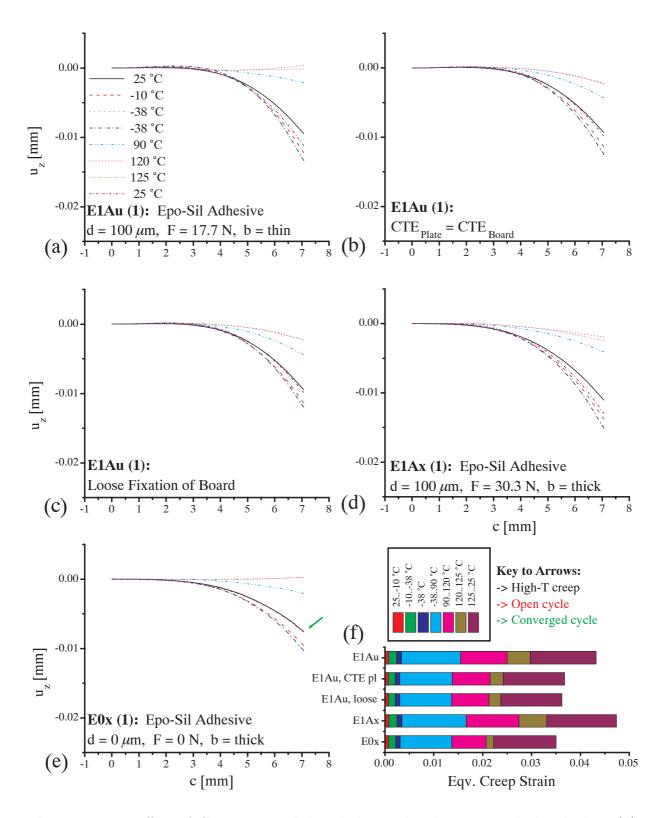


Figure 5.31. Effect of CTE mismatch board-plate: The chip is stretched at high T (a). This does not occur if board and plate are CTE-matched (b). A loosely fixed board (c) has the same effect. A stiffer thick board (d) displays stronger curvature even at high T. Groups with d=0 show convergence already for first cycle (e). Shown is the first cycle. Groups (b) and (c) represent a simulative extrapolation.

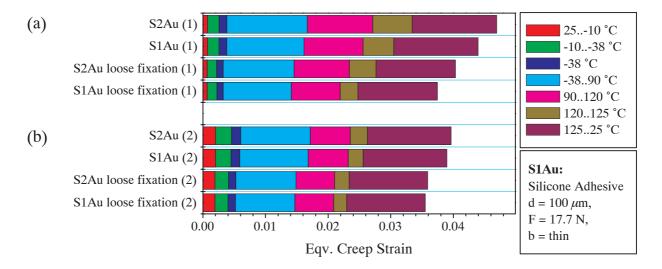


Figure 5.32. Influence of fixation of the board with respect to the value of the displacement exemplified for the silicone adhesive group. A 'loose' attachment has not been realized experimentally and so this diagram represents a simulative extrapolation. Depicted are first (1) and second (2) cycle.

be resolved by the experiment. In any case this means that a fixation is not recommended unless the heat-spreader is thermally matched to the board as in figure 5.31 (b).

Apparently the flip-chip assembly likes best a movement which is dominated by the thermomechanical coupling of underfill and soldermask only. The more constrained the chip is and the larger the elongation from equilibrium are, the larger the relaxation will be, resulting in a transient phase of higher creep strain. As seen in figure 5.31 (e) for the adhesive without mechanical loads the chip behaves as if it were unconstrained for high temperatures. This is also obvious from the fact that it has already converged after the first cycle.

5.4.3 Effect of Board-Viscoelasticity and Orthotropism

In section 4.3.3 it was found that *both* sets of data, the viscoelastic-isotropic and elastic-orthotropic could adequately describe the measured macroscopic behaviour under thermal and mechanical loads when a calibration factor was introduced. (The problem of the correct choice arose due to the fact that *Ansys* does currently not support orthotropic viscoelasticity.) So the global effect of orthotropism seemed to be included and so the viscoelastic set of data was used for all simulations to additionally consider rate-dependent behaviour which could have an effect if the whole test-assembly is simulated.

At the end a simulation was run using the elastic-orthotropic data and the results are seen in figure 5.33. For the curvature there is, as expected, hardly any difference for low temperatures (compare (a) and (c)). At high T the elastic board shows greater stiffness and more creep strain which is also in accordance with the expectations. But both elastic and viscoelastic board show a convergence behaviour concerning curvature (nearly identical) and creep strain which corroborates the thesis of underfill and soldermask being responsible

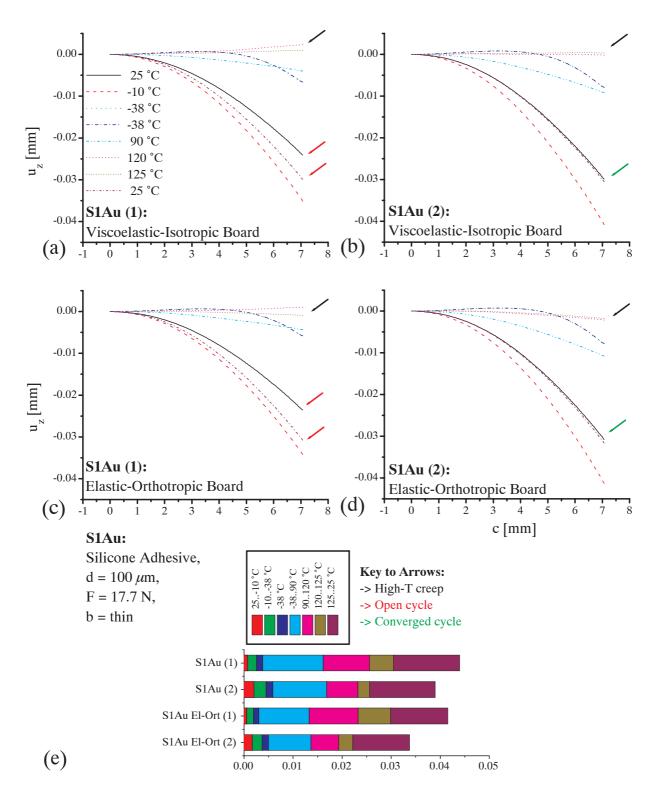


Figure 5.33. Effect of fixed viscoelastic-isotropic board (a,b) compared to fixed elastic-orthotropic (c,d) exemplified for a silicone-attached chip S1Au. Note that the board properties do not influence the macroscopic behaviour of the chip but the creep strain.

for the stabilization of the cycle. But the converged second cycle produces much lower creep for the elastic board (d) compared to (b). This must be a local effect. But it is to the largest part not due to the rate dependence:

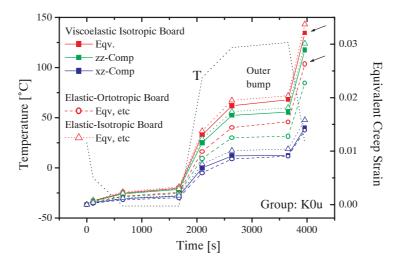


Figure 5.34. The reduced $\bar{\varepsilon}^{cr}$ (arrows) for the elastic board is a local effect of symmetry (orthotropism with respect to isotropy), not of rate-dependence.

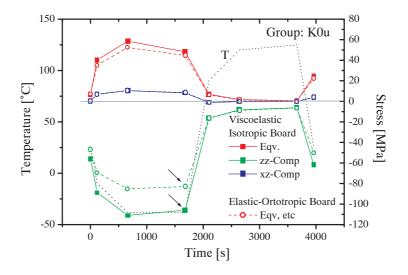


Figure 5.35. The orthotropic board produces less stress in the bump at low T due to a smaller E_z modulus which would induce creep strain ε_{zz} at high T.

As shown in figure 5.34 for the unconstrained chip K0u it is seen that the elastic board influences only the normal strain component. This is a local effect of symmetry, not of rate-dependence. The orthotropic elastic modulus E_z is only one third compared to the isotropic case. Therefore it induces less stress at low T in the bumps as seen in figure 5.35 which in return leads to lower drive for creep strain ε_{zz}^{cr} as the temperature is ramped up. Board orthotropism, i.e. a low E_z , is therefore beneficial for the lifetime of a bump. A similar effect has been quoted in [62], where a local variation of the board-modulus was

assumed to be due to the underlying glass-fibres.

So viscoelasticity is the smaller effect as can be seen when a third variant is introduced: An isotropic-elastic board. It produces only slightly larger values as the isotropic viscoelastic one, a deviation that can only be attributed to rate-dependence.

So orthotropism has greater influence on creep strain than board- viscoelasticity. This may be due to the fact that it maintains still half of its stiffness above T_g because of the fibre reinforcement. But since the variation in E_z is the only difference board-orthotropism should only influence ε_{zz}^{cr} for all groups in an identical way and our ranking still valid.

Still there is a need for a orthotropic viscoelasticity subroutine in FE-tools to represent an organic board adequately.

5.4.4 Check for Thermal Contact in Gap-Filler Groups

A remarkable result was obtained for the foil groups. As the curvature of the chip reaches the largest values for these groups at low temperatures, it is interesting to ask if the contact to the thermal adhesive is still established.

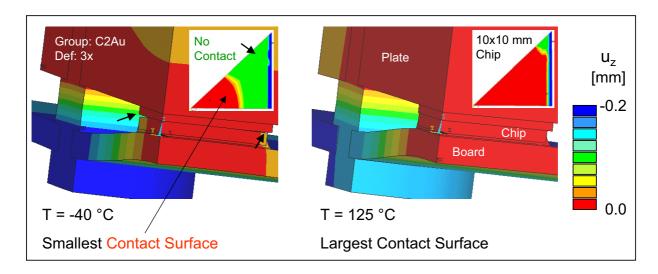


Figure 5.36. Carbon-foil groups (here C2Au): Effective chip-foil contact at extreme temperatures. The inset shows contact areas shaded red. (Magnification: 3×).

As can be seen in figure 5.36 to the left, the effective surface is indeed reduced at low T due to extreme bending. As the temperature rises, the chip touches the thermal interface medium with its entire surface (to the right). This effect depends on the chip size and has to be considered for large chips in that cooling is assured. But as the chip dissipates heat, the assembly will relax and become flat again. For this reason it will still be able to accomplish its task of heat transfer. For a softer gap filler the effect is less severe though. An experimental proof of the thermal performance of these materials and the applicability for flip-chip reverse side cooling has been carried out in parallel and been published in [8].

5.4.5 Die Crack in Flexible Foil Groups

In disassembling the samples as part of the routine test during thermal cycling die crack in the flexible foil groups was found. This could be correlated to the resistance's increase of the daisy chain which went to infinity whenever a die was cracked. Unfortunately infinite resistance is not sufficient but only a necessary criterion for die crack in that all flexible foil samples had to be disassembled to check for a good die and hence for statistical viability. A dependence of the percentage of dies cracked per group on the applied external loads could be found as depicted in figure 5.37.

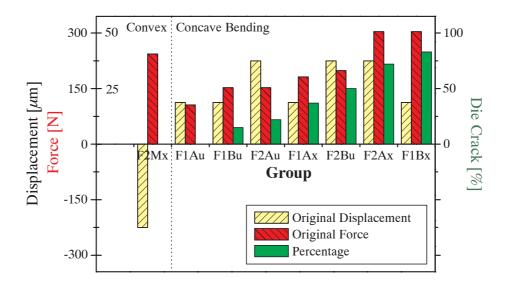


Figure 5.37. Percentage of dies cracked per group. This value is a function of the originally applied mechanical loads d and F. A negative displacement result in a small convex curvature and shows consequently no die crack.

For groups with a positive displacement (enlarged concave curvature of the die), the probability for die crack increases with the applied force. The group with a negative displacement (slightly convex curvature) was not affected. So die crack could have been caused by an unforseen exceeding of the critical deflection of the die as specified in section 4.3.4. Typical cracks are depicted in figure 5.38.

This kind of failure could only be observed with the flexible foil groups since this gap filler did exhibit a non-recoverable deformation which nearly halved its initial thickness under a constant compressive load induced by the external force. This was not known beforehand or noticed during the material's characterisation in section 3.3, as it obviously takes a higher temperature and some time for this effect to occur.

So during thermal cycling the foil shrunk from its initial thickness $h \approx 250 \pm 10 \ \mu m$ to about half its value i.e. in this case to a final thickness of $h' \approx 100 \cdots 150 \ \mu m$ depending on the group. This reduction in thickness could be measured by the device in figure 4.9 but it was also confirmed by a pronounced decrease in thermal resistance as observed by [8]. This decrease could be unambiguously correlated to this reduction, the effect of which is

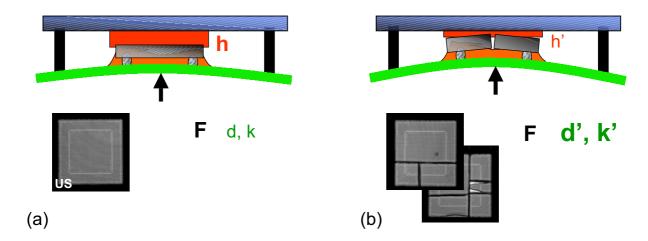


Figure 5.38. Die crack in flexible foil ('F') groups during thermal cycling due to a thinning of the foil down to half its initial thickness. The broken dies (US-pictures) show typical cracks.

depicted in figure 5.38. As the foil shrinks, the displacement of the die and with it its curvature is increased since the force remains constant.

Revised Configurations and Applied Loads for Flexible Foil Groups

Group and Material	Code	d	ď'	F	b	Type
Units		$[\mu m]$	$[\mu m]$	[N]	[mm]	cf. Fig. 5.3
FC, Flexible Foil	F1Au*	100	200	17.7	0.8	(c)
	F1Bu*	100	225	25.4	0.8	(c)
FC, Flexible Foil, neg. Displ	$F2Mx^{**}$	-200	-100	-20.3	1.2	(d)

Table 5.4. Table in analogy to table 5.2: Due to a reduction in foil-thickness the adjusted displacements d of table 5.2 are no longer valid. The results obtained by simulation and experiment have to be accredited to these new values d'.

As can be told from the daisy-chain resistance the die crack occurred already within the first 250 cycles. This means that for most of the thermal cycles the *surviving* chips have seen a much greater $(F1Au, F1Bu)^5$ or a much smaller load (F2Mx) than originally specified. This is given in table 5.4. The chips did operate off their adjusted work-points (figures 5.1) and cannot be directly compared to the other groups for cross-checks. However, simulations were rerun for the new load cases given by the shrunk foil and plotted in the Coffin-Manson diagram among the others and are marked with an asterisk.

⁵As can be seen from figure 5.37 these groups still contain enough chips for a statistical analysis.

⁶See table 5.2.

5.4.6 Failure Criterion for Die Crack

It is interesting to see why the die cracked in the sense of a fracture criterion. Based on the considerations of section 4.3.4 the range of the variables has been extended by simulation in figure 5.39.

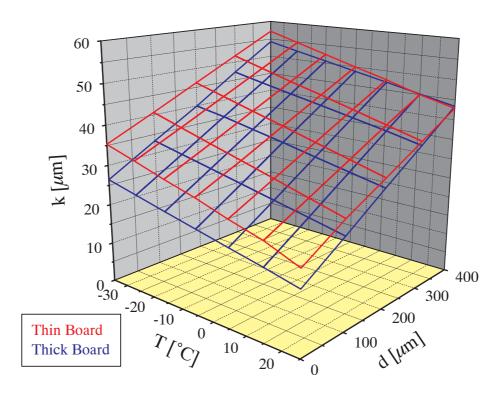


Figure 5.39. The curvature k as a function of T and d for both board thicknesses.

It was concluded that a critical situation could arise for $d > d_c \approx 300 \ \mu m$ or equivalent, $k > k_c \approx 47 \ \mu m$ at low temperatures where the critical curvature or deflection⁷ of the thin board is slightly higher. If we add an (average) displacement h - h' caused by foil thinning to the specified displacement d then we get values $d' = d + (h - h') \ge d_c$ very close and beyond the critical displacement d_c .

If the corresponding values of maximum top surface stress are calculated for the silicon die and incorporated into the above scheme then we can set up a stress criticality criterion. This is depicted in figure 5.40. Obviously the critical stress should be the same for each configuration and not depend on any geometric feature but only on the silicon and the way it was processed (polished, diced).

One obtains, that although the temperature contributes largely to the deflection, it hardly influences the stress. The stress is in return a strong function of the displacement and therefore the mechanically induced curvature. For equal states of overall curvature the thick board induces more surface stress which means that the deflection is not an independent

⁷We recall that for this set-up and within the specified loading regime the curvature κ is proportional to the deflection k to a very good approximation: $\kappa = 1/r \sim k$, see also figure B.6.

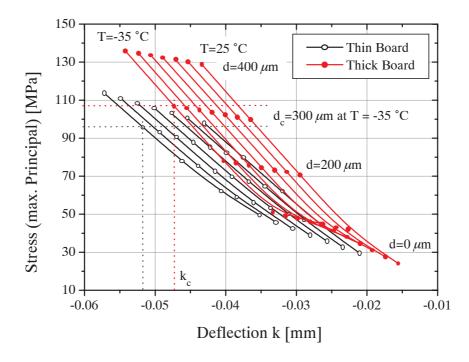


Figure 5.40. Maximum principal top-surface stress in silicon die as a function of curvature k. Highlighted (dots) are the corresponding displacements which lie on the equally spaced isothermal curves. FLTR: $T = \{-35; -25; -15; -5; 5; 15; 25\}$ °C. Dotted lines signify the d_c and k_c from section 4.3.4. The discrepancy concerning σ_c for thin and thick board could be due to the measurement inaccuracy of k_c in the first place.

parameter for die-crack but dependent on b_{bd} , the board thickness. For a given value of stress the thin board can tolerate higher displacement and deflection. This is confirmed very well in figure 5.40. Unfortunately the values for d' have not been measured for each group but only at random over all groups⁸. Hence the mean value of $h' = 125 \pm 25 \ \mu m$.

Drawing upon the critical deflection k_c and displacement d_c determined both experimentally and computationally in section 4.3.4 we can set an upper threshold limit for the stress to be $\sigma_c \approx 100\,MPa$. This value seems low, but as already stated the simulation slightly underestimates the deflection. This could explain this low value. But it should be kept in mind that the considerations given in this section do serve more as a qualitative illustration. For a quantitative analysis more experimental data is needed and the problem of die crack needs a fracture mechanical approach for rigorous treatment. A resulting fracture parameter is still expected to be proportional to σ due to the fact that silicon can be treated linear elastically⁹. Die crack was not expected after all and not the focus of this work.

⁸The idea for this correlation was born later.

⁹K-concept in fracture mechanics, see e.g. [114]

5.4.7 Extrapolation by Simulation: Variation of some Interesting Parameters

Some simulations were run to investigate the influence of some geometric and material parameters. Results were only obtained for the first cycle but from the experience gained we can assume that the ranking is preserved. In this respect the following outcome represents a tendency only. In figure 5.41 (a) the thickness of the adhesive layer is varied. Its original thickness was $h_{ad}=260~\mu m$. The simulations were carried out for the epoxy-silicone adhesive and hence for a viscoelastic material:

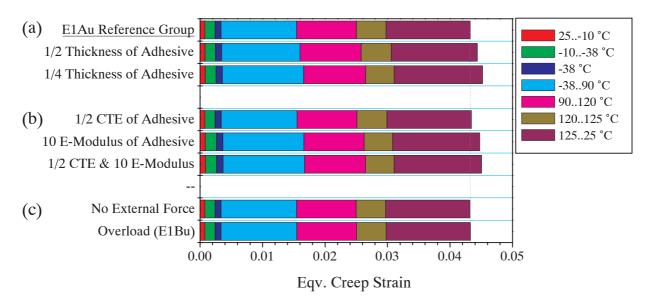


Figure 5.41. Simulative extrapolation concerning the adhesive layer. Varied is its CTE and E-Modulus with respect to the first configuration (reference group).

• Variation of Adhesive Thickness

For a smaller gap with which is more advantageous for cooling purposes there is a rise in creep strain an so one expects a lower reliability (a).

• Variation of Adhesive CTE and E-Modulus

The CTE of the adhesive seems not to be very influential, whereas its elastic modulus does. A softer material should produce more reliable results (b).

• Variation of External Force

The magnitude of an external force itself has no influence on the creep strain at all (c). This is true only for adhesive groups or as long as the chip touches the thermal interface medium. The force only bends the board, but it is much too small to influence the stress in chip and bumps directly and to cause additional strain. A maximum force of F = 50 N only results in a negligibly small stress of $\sigma_{zz} = -0.5 MPa$ for a die with an area of $10 \times 10 mm^2$ as is used here. A

quick estimation by Hooke's law yields, based on the high-T Young's modulus of the underfill, a total strain delta of $\Delta \varepsilon^{tot} \approx 0.0002$ which is negligible.

Unfortunately the groups meant to prove this relationship experimentally were lost due to die crack. Configurations with force A and B for equal displacement were only set for the flexible foil groups (see table 5.2). But this result still holds when comparing F1Bu and F1Au in figure 5.23: Due to the foil thinning described in the last section both have been subjected to loads different from those originally specified. But still the displacements are nearly comparable as to be seen in table 5.4 and the force of F1Bu larger than the one applied to F1Au. The experimentally obtained reliability is similar.

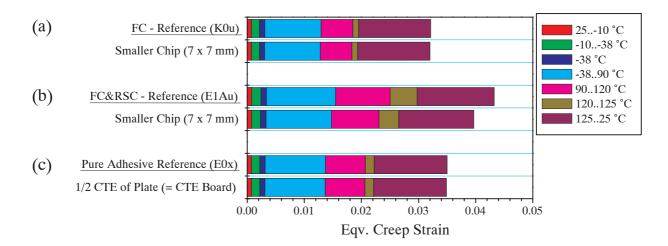


Figure 5.42. Variation of other parameters of interest. Notable is the effect of chip size. The respective reference group is underlined for each comparison.

• Variation of Chip Size

Figure 5.42 shows the effect of some geometric alterations. For the unconstrained chip $K\theta u$ the creep strain does not depend on die size¹⁰ (a), whereas for a mechanically constrained chip E1Au this relationship is lost. A smaller chip will show longer life than a big one under mechanical load (b) as the shear-strains, which depend on bump position, will be smaller (see e.g. figure 5.8).

• Variation of Further Parameters

Further results show (figure 5.42): There is no dependence on the CTE of the plate (c) on reliability as long as there is no fixation (as for $E\theta x$). The simulation (c) was motivated by a paper [10] in which the contrary was stated.

¹⁰A related observation has been mentioned by [27].

5.5 Conclusions, Design Guidelines and Outlook

In this thesis we have numerically evaluated and experimentally verified the thermomechanical reliability of flip-chip assemblies on organic boards under mechanical and thermal loads¹¹ induced by the attachment of a heat-spreader and thermal cycling. Boundary conditions for this study were set by the automotive industry and the application for a real (e.g. controller-) housing. Reliability was examined as function of thermal interface material, displacement (with fixation) of the board, external force and board thickness. These are characteristic variables which describe the load situation for flip-chip reverse side cooling. Experiment and simulation could be consistently and to a good accuracy correlated by the Coffin-Manson relationship, where bump creep strain was evaluated as failure criterion. So for the first time it is possible to correlate reliability and flip-chip cooling.

- It was found that reverse side cooling in flip-chip technology is a reliable option for high-power thermal management. Each tested configuration reached more than $\bar{N}_f = 600$ cycles under the given boundary conditions but for a thermally mismatched assembly. This can still be largely improved by an optimized, thermally matched set-up as already stated and summarized by the guidelines given below. The Coffin-Manson coefficients could be determined to be $c_1 = 0.36$ and $c_2 = -2.33$ which is close to values found in literature.
- Low cycle solder fatigue was found to be the only failure mechanism, therefore the Coffin-Manson approach is justified a posteriori. Delamination did not occur on a large scale. Locally confined ablation did only concern the solder-passivation interface and was shown to be uncritical for solder bump fatigue and therefore negligible.
- It was found that the reverse side attachment of a flip-chip assembly generally reduces lifetime. A prolongation by means of a special fixation or state of bending is not possible, therefore the mechanically unconstrained chip yields the best results.
- From a computational point of view mechanical loading leads mainly to an increase in shear strain, whereas normal strain is mainly influenced by the thermal mismatch of the solder-underfill/soldermask system. Shear strain depends on the kind and amount of constraint on the free movability of the chip as a function of temperature. These constraints, however, depends on board thickness (largest effect), fixation (large effect), displacement and interface material (pronounced effect) as can be concluded from the ranking of configurations with respect to lifetime. The sign of curvature has hardly got any influence on lifetime. A convexly bent chip yields a slightly higher reliability than its concave counterpart. A force has no effect on reliability.
- The flip-chip assembly can be conceived as a system which undergoes periodic, thermally driven deformation. Under the test conditions of thermal cycling the assembly accommodates to the applied load after a convergence period of transient response.

¹¹The *thermal* performance and viability of this concept has recently been studied and proved in [8] using the same set-up, loads and thermal interface materials.

The movement of the chip diagonal (centre to corner) under periodic thermal load stabilizes around a new equilibrium position determined by the applied mechanical loads. The bump creep strain shows corresponding convergence behaviour.

• A modular parametric FE-model was developed, optimized and experimentally verified for this study. A novel concept consisting in the combination of standard modules allows a very flexible, accurate and accelerated model generation and subsequent evaluation of creep strain within the bump. Corresponding guidelines are given. This approach may also be extended to related packages wherever repetitive parts can be modelled as standard module as e.g. any solder joint.

Design Guidelines

A distinct ranking can be drawn up according to the tested variables based on the computational value for better resolution. The results and consequent design guidelines (DG:) are once more compiled in table 5.5.

- The most reliable configurations are the unconstrained chips K0u,x together with the adhesive groups without displacement E0x and S0x (a chip-sized heat-spreader glued to the chip), followed by groups featuring displacement and fixation. DG: It is not possible to increase reliability by reverse side attachment.
- A flip-chip assembly which is attached by an epoxy-silicone adhesive only shows slightly higher reliability than the unconstrained one. It was shown that this is an exception and only the case for a thermally mismatched solder-underfill system. For this reason this result cannot be generalized, as normally the technically relevant matched system is preferred which guarantees smaller bump creep strain and hence a longer lifetime. The silicone adhesive group S0x, however, comes last for the considered configurations. DG: If a small (chip-sized) heat-spreader is sufficient, a very reliable configuration can be realized by gluing it to the chip.
- Thick boards largely reduce lifetime. DG: As this is the strongest effect boards should be as thin as possible. Tested values were $b \in [0.8; 1.2] \ mm$.
- A fixation of the board considerably increases bump creep strain and hence reduces reliability. *DG*: The board should not be fixed unless global mismatch board-plate can be eliminated. A sliding fixation solves the problem.
- Larger displacements produce lower reliability. *DG*: Displacement should be minimized, but compared to fixation and board thickness its value has only a small effect. So if no fixation is used, a comparatively large displacement can be realized.
- A convex curvature of the chip seems to produce slightly better results than a concave one (which is the normal state of bending for an unconstrained chip). *DG*: A chip may also be bent convexly, allowing negative values of displacement if needed.

- Groups using a gap-filler prove slightly more reliable than those with an adhesive. The epoxy-silicone adhesive yields slightly better results than the silicone-based one. A distinction between the gap-fillers is hardly possible. DG: Gap-fillers are to be given preference. If an adhesive is employed, it should have a low E-modulus ($E < 500 \, MPa$) and low CTE ($\alpha < 100 \, ppm/K$) for all T to maintain a low stress bond and prevent a stretching out of the die at low T as encountered for the silicon adhesive which features a CTE of $\alpha \approx 200 \, ppm/K$ and increasing E at low T.
- A force has no detectable influence on reliability. *DG*: A design need not consider the magnitude of a force.
- In the temperature and time domain used for testing this assembly board-viscoelasticity is not as important an effect as board-orthotropism for the simulation. There is, however, a reduction of normal bump strain which is due to a lower out-of-plane E-modulus for an orthotropic formulation. DG: Therefore a board should be highly orthotropic for high reliability, $E_z < 6 \, GPa$. Still, the board should be implemented as orthotropic and viscoelastic material to capture both characteristic properties. This, however, requires a new element capability for the respective FE-tool in use.
- For a mechanically loaded flip-chip assembly its reliability is not independent from chip size any more. The chip should be kept small, as under identical loads a chip with $A = 7 \times 7 \, mm^2$ did show lower creep strains than the $A = 10 \times 10 \, mm^2$ chip.
- A fracture criterion for die crack based on the maximally allowed surface stress could be evaluated to $\sigma_c = 100 \, MPa$. This corresponds to a (board thickness-dependent) critical deflection $k_c = 52 \, \mu m$ and $k_c = 44 \, \mu m$ for thin and thick board respectively. In the experiment this condition was met if a maximum displacement of $d_c \approx 300 \, \mu m$ was not exceeded.

The early overall failure is in accordance with the large simulated creep strains, which are mainly due the high normal strains induced by the solder/underfill mismatch. As can be seen from the inset in figure 5.30, reliability and the difference between the groups would be much larger for lower values of strain. The effect of the mechanical loads (shear strain) would also be better resolved in that case. Then values above $\bar{N}_f > 1500$ can be reached for most loaded groups¹² in contrast to the experimentally obtained value of $\bar{N}_f > 600$. This can be realized by following the guidelines given below.

- The solder gap is very small $(h = 47 \ \mu m)$. So the bump creep more. DG: Creep strain depends strongly on h, so the gap should be maximized.
- There is a prolonged creep phase due to the heat capacity of the attached heat spreader during thermal cycling. This may be responsible for the large amount of solder coarsening.

 $^{^{12} \}rm Based$ on the values of a matched under fill-solder system taken from figure 5.10 and extrapolated with the inset of figure 5.30

- The very large underfill-solder mismatch ($\alpha_{UF} \approx 2\alpha_{SnPb}$) induces additional normal strain in the bump which reduces reliability. DG: The underfill (and if possible also the soldermask) must be thermally matched to the solder. Use $\alpha_{UF} > 24 \, ppm/K$ and $\alpha_{SM} < 70 \, ppm/K$.
- The extraction of voids (non-standard process) under vacuum caused initial damage (gaps, pre-cracks) and blurs the statistical outcome. *DG*: Flip-chip processes should be optimized *not* to produce any voids.
- The pad diameter is small $\phi = 75 \,\mu m$ there is less solder to crack. The lateral extension of the bump is of no influence. DG: Bumps with larger pads respond favourably in terms of reliability.

Compilation of Results and Design Guidelines

Variable		Effect on Reliability	Design Guidelines
	р	ositive (+), neutral (0), negative (-)	(Values as tested)
Displacement	_	Proportional to value	$d \in [-200; 200] \mu m$
Fixation		If $\alpha_{Board}(T) \neq \alpha_{Plate}(T)$	Sliding, matched or none
Force	0	Within checked range	$F \in [17; 50] N$
Adhesive	+	Low E for all T	E < 500 MPa
	+	Low $\alpha(T)$ for all T	$\alpha < 100 ppm/K$
	0	Large gap	$b \in [65; 260] \mu m$
Gap Filler	+	Slightly better than adhesives	by $< 10 \%$
Curvature	_	If constrained at high T	Use low stress bond
(Response)	0	At low T	
	+	If convex	d < 0 is possible
Processes	0	Curing of adhesives	$T_{cure} = 160 {}^{o}C$
	_	Extraction of voids by vacuum	To be avoided
Delamination	0	Localized around pad	Width $a < 20 \mu m^2$
	_	If of size of pitch around bump	$A = 250 \times 250 \mu\text{m}^2$
Board	+	Thin	$b \in [0.8; 1.2] mm$
Board	+	Low E_z	$E_z < 6 GPa$
Underfill	_	If $\alpha_{UF}(T) \neq \alpha_{SnPb}(T)$	$\alpha_{UF} > 24 ppm/K$
Soldermask	_	If $\alpha_{SM}(T) \gg \alpha_{UF}(T)$	$\alpha_{SM} < 70 ppm/K$
Heat Spreader	0	$\alpha(T)$ (if no fixation)	
Chip	+	If small size	$A \in [7 \times 7; 10 \times 10] mm^2$
	0	Size if die is unconstrained	
Bumps	+	If small pad; If large gap width	$\phi > 75 \mu m; b > 47 \mu m$
	0	Lateral extension	$a \in [160; 230] \mu m$
	_	Voids	$\phi < 10 \mu m^{\dagger}$
Surface stress	0	If below value for die fracture	$\sigma < \sigma_c = 100 MPa$

Table 5.5. The individual factors and their impact on Flip-Chip reliability according to this study. Recommendations are given based on the checked range of values. For remaining details refer to the text. † Below this value no voids could be detected, ϕ is a diameter.

Optimum Configuration

Working on the given design guidelines the configuration optimized for reliability looks as follows. Based on the a multi-chip module as depicted in figure 2.3 one obtains:

- A flexible foil is used as thermal interface material as this produces the most reliable results and allows for lateral movement of the die (i.e. a thermo-mechanical decoupling) if more than one chip is on the board. Otherwise other chips may have the negative effect of a fixation.
- \bullet As there a manufacturing tolerances G, a force per chip of

$$F \ge F_G + F_N = \frac{1}{p_b} d_G + F_N,$$
 (5.9)

which displaces the board by d_G to bridge the hence existing gap should be applied (cf. equation 5.1). The force may exceed the calculated value as this does not affect reliability. A displacement reduces lifetime only slightly in this configuration. Should convex bending of the die occur, this is of no further concern.

- The board is thermo-mechanically decoupled from the housing (i.e. the heat-spreader, e.g. aluminium) to eliminate the thermal mismatch. For this purpose a sliding fixation is used to hold the board in place.
- The flip-chip assembly is mounted on a thin board $(b = 0.8 \, mm)$ and its underfill is thermally matched to the void-free eutectic solder bumps. The CTE of the soldermask is lower than $\alpha_{SM} < 70 \, ppm/K$.

For the situation where only a chip-sized heat-spreader is needed (in a casing where there is enforced convection) the following reliable solution is possible as a 'spin-off' of this study:

- A low stress bond is established between the chip's reverse side and the heat-spreader by a thermal adhesive with low CTE $\alpha(T) < 100 \, ppm/K$ and low stiffness $E < 500 \, MPa$ for all temperatures.
- The thickness of the adhesive is set by thermal boundary conditions, but if a highly conductive material is used a larger gap can be realized which increases reliability.
- A curing process $t = 900 \, s$, $T = 160 \, {}^{o}C$ does not reduce the reliability of the assembly.

Outlook

• Extreme solder coarsening was observed during cycling. It was speculated if this was due to a prolonged ramping time which theoretically allows more creep. A cross-check should be made with chips subjected to a different thermal cycle to see if this phenomenon persists.

• For future experimental analysis of bump failure use a chip which is devised for fourpoint measurements for a maximum number of bumps (not just eight bumps) for more data. Desirable is further a daisy-chain which allows multiple access to measure its resistance for a smaller group of bumps (for example around the corner) for failure localization. This measurement should be conducted in four-point arrangement, too.

Appendix A

Annotations on Theory

Here we give an overview over the definitions, mathematical conventions and most important abbreviations which are used in this work.

An other section will provide a brief summary about the Weibull distribution and how it is applied to fatigue phenomena.

A.1 Conventions and Notation

A.1.1 Units

If not specified otherwise, this consistent system of units is used [57].

Units

Quantity	Unit
Length	mm (Millimetres)
Force	$N ext{ (Newtons)}$
E-Modulus, Stress, Pressure	MPa (Megapascals)
Time	$s ext{ (Seconds)}$
Mass	$t ext{ (Tons)}$
Temperature	$K \text{ or } {}^{o}C$

Table A.1.

Helpful is: 1 psi = 6890 Pa.

A.1.2 Mathematical Representation

Throughout the thesis stress is normally symbolised by the tensor σ_{ij} and strain by ε_{ij} (mathematical notation). Engineering notation $\{\sigma_i, \tau_{ij}\}$ is hereby translated into $\{\sigma_{ii}, \sigma_{ij}\}$ and $\{\varepsilon_i, 1/2\gamma_{ij}\}$ into $\{\varepsilon_{ii}, \varepsilon_{ij}\}$.

Mathematical Notation

Quantity	Symbol
Scalar	a
Vector	\boldsymbol{a},a_i
Tensor	$m{\hat{a}},a_{ij}$
Equivalent Entity	$ar{a}$
Derivative with respect to t	d_t,∂_t

Table A.2.

Einstein's sum convention is used. Hereby the sum extends over doubly appearing indices.

$$b_i = \sum_j \alpha_{ij} a_j = \alpha_{ij} a_j. \tag{A.1}$$

Ansys commands are printed in typewriter style.

A.1.3 Abbreviations

Table of Abbreviations

Abbreviation	Meaning
CSP	Chip Size Package
CTE	Coefficient of Thermal Expansion
DC	Daisy Chain
DMA	Dynamic Mechanical Analyis
DNP	Distance to Neutral Point
FC	Flip-Chip
FC&RSC	Flip-Chip and Reverse Side Cooling
FE	Finite Element(s)
PCB	Printed Circuit Board
QFP	Quad Flat Package
SB	Single Bump
SEM	Scanning Electron Microscopy
TMA	Thermo Mechanical Analysis
UBM	Under Bump Metalisation
US	Ultrasound

Table A.3. A compilation for quick reference.

For material abbreviations see table 4.1.

For group encoding see table 5.1.

A.2 Heat Transfer

The heat energy flow per unit time P_T transferred though any area A to a conductive medium can be evaluated as (see e.g. [115]):

$$P_T = \frac{dQ_T}{dt} = \int_{\mathcal{A}} \boldsymbol{j} \, \boldsymbol{dA}, \tag{A.2}$$

where j is the heat current density

$$j(r) = -\hat{\lambda}_T(r) \nabla_r T(r). \tag{A.3}$$

In its most general form the thermal conductivity λ is a tensor. If the current density is homogeneous and passes through the area orthogonally, the equations reduce to

$$|P_T| = jA = \lambda \frac{\Delta T}{\Delta b} A. \tag{A.4}$$

As the temperature rises heat can be transferred also by radiation. The fraction of energy per unit time and area dissipated by the whole frequency spectrum ν of electromagnetic waves is according to the *Stefan-Boltzmann law* for black body radiation [59] proportional to T^4 :

$$\frac{P_T}{A} = \int_{\nu} d\nu \ p(\nu) = c(T^4 - T_0^4), \tag{A.5}$$

where $c = 5.6 \times 10^{-8} \frac{W}{m^2 K^4}$, $p(\nu)$ the spectral power density and T_0 the ambient temperature.

A.3 Time Dependence of Viscoelastic Moduli

We will briefly outline the derivation of equation 3.52. Point of departure is the hereditary integral form of the stress-strain relationship for isotropic viscoelastic materials:

$$\sigma_{ij}(t) = \int_0^t dt' \ 2G(t - t')\dot{e}_{ij}(t') + 3K(t - t')\dot{e}_m(t')\delta_{ij},\tag{A.6}$$

We consider a relaxation test. An oblong bar is strained in x-direction: $\varepsilon_{xx}(t) = \varepsilon_{xx}\theta(t-t_0)$. This entails $\varepsilon_{yy}(t) = \varepsilon_{zz}(t)$ and no shear strains. For the stresses only $\sigma_{xx} \neq 0$. We can write:

$$\sigma_{xx}(t) = \int_0^t dt' \, \frac{4}{3} G(t - t') \left(\dot{\varepsilon}_{xx}(t') - \dot{\varepsilon}_{yy}(t') \right) + K(t - t') \left(\dot{\varepsilon}_{xx}(t') + 2\dot{\varepsilon}_{yy}(t') \right). \tag{A.7}$$

Then we exploit

$$\sigma_{yy}(t) = \int_0^t dt' \ 2G(t - t') \left(\dot{\varepsilon}_{yy}(t') - \dot{\varepsilon}_{xx}(t') \right) + 3K(t - t') \left(\dot{\varepsilon}_{xx}(t') + 2\dot{\varepsilon}_{yy}(t') \right) = 0. \quad (A.8)$$

If we insert this into the previous equation we may eliminate e.g. K(t) and obtain:

$$\sigma_{xx}(t) = \int_0^t dt' \, 2G(t - t')(\dot{\varepsilon}_{xx}(t') - \dot{\varepsilon}_{yy}(t')) \quad \text{and} \quad (A.9)$$

$$\sigma_{xx}(t) = \int_0^t dt' \, 3K(t - t')(\dot{\varepsilon}_{xx}(t') + 2\dot{\varepsilon}_{yy}(t')). \tag{A.10}$$

Rewriting the first equation using $\dot{\varepsilon}_{yy}(t) = -\dot{\nu}(t)\varepsilon_{xx}(t) - \nu(t)\dot{\varepsilon}_{xx}(t)$ like

$$\sigma_{xx}(t) = \int_0^t dt' \ 2G(t - t')(1 - \nu(t'))\dot{\varepsilon}_{xx}(t') + \int_0^t dt' \ 2G(t - t')\dot{\nu}(t')\varepsilon_{xx}(t') \tag{A.11}$$

yields after insertion of the initial conditions $\varepsilon_{xx}(t) = \varepsilon_{xx}\theta(t)$ and $\dot{\varepsilon}_{xx}(t) = \varepsilon_{xx}\delta(t)$, i.e. assuming the strain to be applied at zero time

$$\frac{\sigma_{xx}(t)}{\varepsilon_{xx}} = E(t) = 2G(t)(1 - \nu_0) + \int_0^t dt' \ 2G(t - t')\dot{\nu}(t'). \tag{A.12}$$

We take the Laplace transform of the above equation taking into account $\mathcal{L}(f(t)) = \tilde{f}(s)$ and $\mathcal{L}(d_t f(t)) = s\tilde{f}(s) - f(0^+)$ and the convolution theorem

$$\tilde{E}(s) = 2\tilde{G}(s)(1+\nu_0) + 2\tilde{G}(s)s\tilde{\nu}(s) - 2\tilde{G}(s)\nu_0.$$
 (A.13)

Applying the same procedure to the second equation in A.10 and simplifying yields

$$\tilde{G}(s) = \frac{\tilde{E}(s)}{2(1+s\tilde{\nu}(s))} \tag{A.14}$$

$$\tilde{K}(s) = \frac{\tilde{E}(s)}{3(1 - 2s\tilde{\nu}(s))}.$$
(A.15)

which is equivalent to equation 3.52 as was to be proved.

A.4 Weibull-Distribution

The Weibull distribution is often encountered in the description of lifetime phenomena as for example solder fatigue [68, 110, 111]. It can reflect decreasing, constant and increasing failure rate $\lambda(t)$, i.e. the percentage occurrence of failure as a function of increasing random variable t. This behaviour manifests itself in the well-known 'bathtub'-shaped curve depicted in figure A.1.

The Weibull distribution is a two-parameter function (λ, β) and can be defined by its probability density function:

$$f(t) = \lambda \beta (\lambda t)^{\beta - 1} e^{-(\lambda t)^{\beta}}.$$
 (A.16)

Then the Weibull cumulative distribution function describes the probability \bar{p} that an event that item i will have failed under given service conditions after a time τ_i has elapsed:

$$\bar{p}(\tau_i < t) = F(t) = \int_0^t dt' f(t') = 1 - e^{-(\lambda t)^{\beta}}.$$
 (A.17)

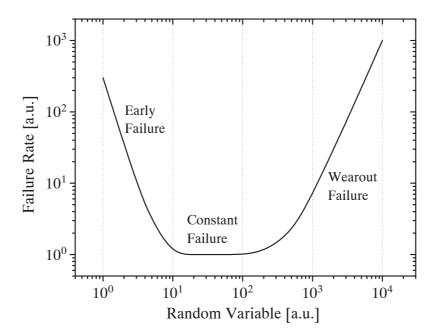


Figure A.1. Typical 'bath-tub'-shaped failure rate of Weibull distribution.

Then the reliability function R(t) describes the probability p for the inverse event, that the item performs flawlessly until $t = \tau_i$:

$$p(\tau_i < t) = R(t) = 1 - F(t) = e^{\int_0^t dt' \, \lambda(t)}$$
 as $\int_0^\infty dt' \, f(t') = 1$. (A.18)

This means for the failure rate $\lambda(t)$ according to the definition:

$$\lambda(t) = -\frac{d_t R(t)}{R(t)} = \lambda \beta(\lambda t)^{\beta - 1}, \tag{A.19}$$

where always $\lambda = 1/t_c$ and t_c is the characteristic lifetime where 63 % of the items have failed (d_t) is the derivative with respect to t).

The mean time to failure of the distribution is calculated to

$$\bar{t} = \int_0^\infty dt' \, t' f(t') = t_c \Gamma(1 + 1/\beta),$$
 (A.20)

i.e. the time after which 50 % of the items have failed. Here, Γ is the Gamma-function [116]. Working on the principle that no defects are detectable at t=0, the distribution can describe, depending on the Weibull exponent β , different cases (cf. figure A.1).

• β < 1: Early failures (or infant mortality¹) due to randomly distributed weaknesses in the material due to process or quality related problems, not deterministic. Failure occurs during burn-in or initial tests. $\lambda(t)$ tends to infinity as the random variable approaches zero.

Samples belonging to this group are be sorted out for lifetime evaluation.

¹This curve also reflects a human death table.

- $\beta = 1$: Constant failure rate: In this region no aging or wearout occurs. distribution essentially resembles a exponential distribution.
- $\beta > 1$: Increasing failure rate: Degradation processes (aging and wearout) occur, damage accumulates. These region is typical for solder fatigue. For $\beta = 2$ this failure rate is linearly increasing (cf. A.19), for values even larger the distribution becomes a normal distribution.

In a logarithmic representation² as e.g. in figure 5.22 F(t) appears as a straight line and β represents the function gradient of this Weibull plot according to:

$$\ln\left(\ln\left(\frac{1}{1-F(t)}\right)\right) = \beta\ln(t) + \beta\ln(\lambda). \tag{A.21}$$

For the numerical evaluation the experimental F(t) is linearly fitted (by a least squares algorithm) to this line to yield t_c and β .

For the analysis of the failure mode solder fatigue we contemplate the failure mechanism of creep crack growth which causes electrical failure or breakdown of the component (flip-chip assembly).

Important for the evaluation of the lifetime of a flip-chip assembly is the failure of the first bump. This is a system without redundancy, i.e. all items (bumps) must work to assure function of the system. The used daisy-chain is a series-structure and theoretically signalises the event of failure of the one first bump. We have to consider: If

$$p(t < \tau_i) = R(t) = e^{-(\lambda_i t)^{\beta_i}}$$
(A.22)

is the reliability of one bump, then – given that all bumps are identical $(\lambda_i = \lambda, \beta_i = \beta)$ – the reliability of n bumps is:

$$R_{tot}(t) = \bigcap_{i=1}^{n} p_i(t < \tau_i) = \prod_{i=1}^{n} R_i(t) = \prod_{i=1}^{n} e^{-(\lambda_i t)_i^{\beta}}$$

$$= e^{-n(\lambda t)^{\beta}} = e^{-(\lambda n^{1/\beta} t)^{\beta}} = e^{-(\lambda_{tot} t)^{\beta}},$$
(A.23)

$$= e^{-n(\lambda t)^{\beta}} = e^{-(\lambda n^{1/\beta} t)^{\beta}} = e^{-(\lambda_{tot} t)^{\beta}}, \tag{A.24}$$

where now a higher failure rate for the system $\lambda_{tot} = \lambda n^{1/\beta}$ could be derived. Obviously this results in a lower overall reliability. In this vein the characteristic lifetime t_c^{tot} can be evaluated to:

$$t_c^{tot} = t_c n^{-\frac{1}{\beta}}. (A.25)$$

For calculation of the mean equation A.20 is used.

²X-axis logarithmic, y-axis double logarithmic.

Appendix B

Annotations on Materials

Here we give the results of the characterisation of the remaining materials including the data files for Ansys-input.

B.1 Dimensions of Dog's-bone Specimen

The dog's bone specimens as they are depicted in figure 3.8 were shaped according to the below depicted dimensions. Thickness is 2 mm.

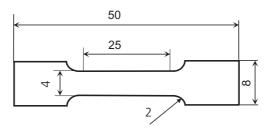


Figure B.1. Dimensions of test-specimen # 53504 in [mm].

B.2 Organic Board

B.2.1 Measured Viscoelastic Material Data

The measured data for the organic board was recorded on a Zwick 1446 universal testing machine. The last measured curve (T = 150 °C) shows a different relaxation behaviour. This might be due to measurement inaccuracies as this value does not fit into the WLF regime (figure B.4). It could be attributed to more than one relaxation processes (deviation from pure exponential decay) occurring at this temperature.

A typical feature of organic boards, i.e. glass fibre reinforced epoxy compounds, is a severe reduction of the CTE above T_g . This is caused by the dominance of the (relaxed) glass fibres which exhibit CTEs close to $\alpha \approx 2 \ ppm/K$ or even lower.

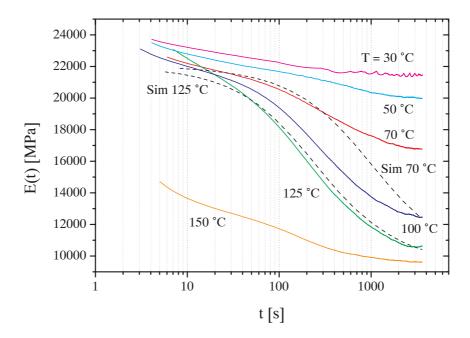


Figure B.2. Measured relaxation data of organic board. Simulated data is printed in dashed lines.

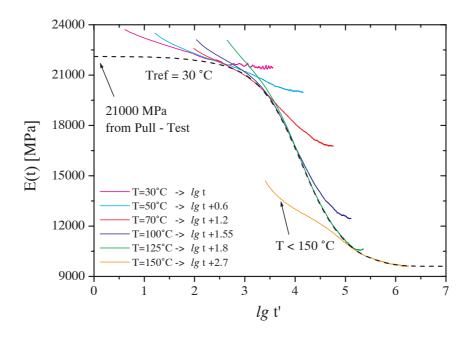


Figure B.3. Temperature-time shifted data for construction of mastercurve (dashed line).

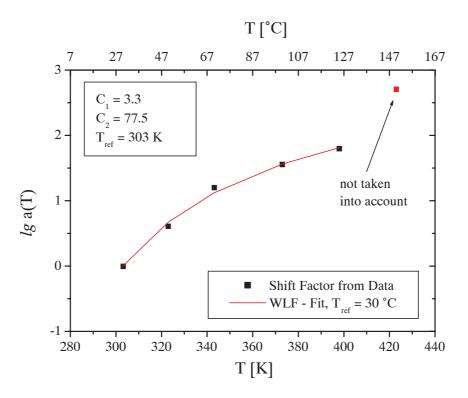


Figure B.4. WLF shift function for organic board.

B.2.2 Ansys Data File for Viscoelastic-Isotropic Board

```
! Organic Board
!--viscoelastic constants input for usrve5x.f
1-----
tb,evisc,mat_fr
                ! initialize
tbda, 1, 3.28
                ! wlf c1
tbda, 2, 77.44
                ! wlf c2
tbda, 4, 303
                ! wlf tref
tbda, 5, 20
                ! function key, must be 20
!--temperature and cte input------
!- follows 5 temp in ascending order covering t-range of simulation
tbda, 26, 210, 273, 388, 408, 440
!- follows 5 corresponding cte values
tbda, 36, 11.5e-6, 11.5e-6, 1.2e-6, 1.2e-6
!--prony setup-----
!-- these next four coeff are modified by x 0.7 to account for orthotropy
tbda, 46, 6729.12 ! 9613.04
                           ! G0
tbda, 47, 2495.40 ! 3564.87
                            ! Ginf
tbda, 48, 7370.02 ! 10528.6
                           ! K0
tbda, 49, 7370.02 ! 10528.6
                            ! Kinf
tbda, 50, 7
                           ! # g
! -- prony coeff shear---------
tbda, 51, 0.0187527001065796
tbda, 52, 0.009571006487340366
tbda, 53, 0.15913976237286734
tbda, 54, 0.4571182689898273
tbda, 55, 0.2610001403657228
tbda, 56, 0.05423469041781277
tbda, 57, 0.04018343125984965
! -- prony times shear-----
tbda, 61, 99.72507728233133
tbda, 62, 998.6102310320236
tbda, 63, 4366.5765878401835
tbda, 64, 11722.110300122671
tbda, 65, 47951.251043004006
tbda, 66, 197666.3873758236
tbda, 67, 497700.88540016394
!-- end of viscoelastic data input-----
!-- Comment: Viscoelastic Input has assumed an effective nu = 0.15, since
!-- the material, although orthotropic, can only be simulated isotropically.
I-----
```

B.2.3 Ansys Data File for Elastic-Orthotropic Board

```
! Organic Board, orthotropic, elastic, temp-dep.
                                   ! T-Table in Kelvins
mptemp,1, 220, 268, 308, 348, 368
mptemp,6, 388, 398, 408, 443
mpdata, ex, mat_fr, 1, 17850, 17850, 17850, 17850, 17850
mpdata, ex, mat_fr, 6, 17000, 16000, 15725, 15725
mpdata, ey, mat_fr, 1, 17850, 17850, 17850, 17850, 17850
mpdata,ey,mat_fr,6, 17000, 16000, 15725, 15725
mpdata,ez,mat_fr,1, 7055, 7055, 7055, 7055,
mpdata,ez,mat_fr,6, 5695, 5000, 4420,
                                     4420
mpdata,gxy,mat_fr,1, 6630, 6630, 6630, 6630
mpdata,gxy,mat_fr,6, 6290, 6000, 5822, 5822
mpdata,gxz,mat_fr,1, 2250, 2250, 2250, 2250, 2250
mpdata,gxz,mat_fr,6, 2122, 2100, 2040, 2040
mpdata,gyz,mat_fr,1, 2250, 2250, 2250, 2250, 2250
mpdata,gyz,mat_fr,6, 2122, 2100, 2040, 2040
mpdata,prxy,mat_fr,1, 0.15, 0.15, 0.15, 0.15, 0.15
mpdata,prxy,mat_fr,6, 0.15, 0.15, 0.15, 0.15
mpdata,prxz,mat_fr,1, 0.35, 0.35, 0.35, 0.35, 0.35
mpdata,prxz,mat_fr,6, 0.35, 0.35, 0.35, 0.35
mpdata,pryz,mat_fr,1, 0.35, 0.35, 0.35, 0.35, 0.35
mpdata,pryz,mat_fr,6, 0.35, 0.35, 0.35, 0.35
mpdata,alpx,mat_fr,1, 9.80e-6, 9.30e-6, 8.60e-6, 7.20e-6, 5.95e-6
mpdata,alpx,mat_fr,6, 3.48e-6, 2.27e-6, 1.20e-6,
                                                1.20e-6
mpdata,alpy,mat_fr,1, 9.80e-6, 9.30e-6, 8.60e-6,
                                               7.20e-6,
mpdata,alpy,mat_fr,6, 3.48e-6, 2.27e-6, 1.20e-6,
                                                1.20e-6
mpdata,alpz,mat_fr,1, 61.0e-6, 68.3e-6, 78.6e-6,
                                                90.2e-6, 106.0e-6
mpdata,alpz,mat_fr,6, 135.0e-6, 140.0e-6, 142.0e-6, 142.0e-6
!--- use secant gradient for CTE Definition T= 433 K
```

The data is temperature-dependent. It is important to note that Ansys wants the CTE to be inserted as secant value $\bar{\alpha}(T)$, not as tangent value $\alpha(T)$. Therefore the given tangent values (which are needed for the viscoelastic routine) are transformed into secant values. This can be effectuated by:

$$\bar{\alpha}(T) = \frac{1}{T - T_{ref}} \int_{T}^{T_{ref}} dT \ \alpha(T) \quad . \tag{B.1}$$

There is a trick which applies to polymers to circumvent this tedious procedure: For increasing $\alpha(T)$ the corresponding values of $\bar{\alpha}(T)$ may be automatically calculated by inserting the $\alpha(T)$ values together with the command mpamod,mat,Tg, where T_g is the glass transition temperature. Unfortunately this does not work here for alpx due to a decreasing $\alpha(T)$. $T_{ref} = 160~^{o}C$ as stress-free point.

B.2.4 Calibration of Viscoelastic Board Data (Full Account)

The main steps and results of the calibration process of the organic board data has been explained in section 4.3.3. Here we give the steps of this process in full and in chronological order.

It will be shown that the simulation can reproduce the experimental values for either viscoelastic-isotropic and elastic-orthotropic material behaviour if an effective modulus is introduced. This can be ascribed to the material's inhomogeneity and layered structure. Viscoelastic behaviour does seem not to govern the *bending* of the assembly in the examined temperature and time domain. In the discussion we refer to table B.1; The columns from left to right are:

Variables: Thickness of the board; Temperature drop after cooling down from curing temperature; Material law (elastic-orthotropic/viscoelastic-isotropic); Cooling time; Poisson's ratio (in plane, out of plane); Glass transition temperature; Coefficient of thermal expansion (in plane, out of plane) below T_g ; CTE above T_g ; Factor for effective stiffness; Applied external force aimed for $d = 100 \ \mu m$;

Observables: Thermal deflection of chip; Mechanical deflection of chip; z-displacement of board.

For reasons of clarity the variations of the individual variables are grouped together. Now it is the task to vary the variables in that the observables for thin and thick board show maximum accordance under the given boundary conditions. Hereby every computationally obtained result is to be compared to rows (1a,b) from the experiment.

• Row (2a):

First of all the elastic-orthotropic set was used. This had been the time-honoured way to simulate an organic board and accounts for the fact that the board is clearly not isotropic. It is obvious that k_T is largely overestimated. Apart from that, the board is too stiff. The values of k_F should only be compared at the experimental value $d = 100 \ \mu m$.

• Row (2b):

It was checked if the poisson's ratio could have any influence since these values were only determined by the method of the 'educated guess': As we have to deal with pure fibre-epoxy (hardly any copper) the in-plane value is dominated by the glass fibres (0.15) whereas the out-of-plane value should be epoxy-like (0.35). An exchange of the values produces the expected result, a board which is less stiff (less in-plane contraction).

• Row (3a):

It was checked if this discrepancy could be remedied by the assumption of a viscoelastic board, i.e. if this overestimation of k_T is due to any not considered stress relaxation effects which were clearly measured and were described in the last section. Still, the value of the deflection is hardly influenced by this alteration. Here, (too large) values from literature for the CTE have been assumed. As Ansys only supports isotropic viscoelasticity the in-plane value of ν was chosen.

• Row (3b,c):

A scaling factor β is introduced which results in an effective E-modulus according to equation 4.11 which affects only d but not k_T . The thick board is evaluated, too.

• Row (4a,b,c,d)

shows the strong dependence of k_T on T_g and the CTE for both thicknesses. Better values are reached when smaller values for either quantity are used. This tendency is indeed experimentally confirmed (TMA). At the same time the thickness of the board is remeasured and found to differ from the manufacturer's value.

• Row (5a,b,c,d,e)

shows the influence of board thickness. To the measured value for pure fibre-epoxy (rows (1a,b)) a thickness for the solder mask averaged over the area of the board is added (20 μm for either side of the board). This levels out the difference between the thick and the thin board. Now the newly measured values for T_g and CTE are used, too. (5b,e) represent the closest sets.

• Row (6a,b,c)

show the small influence of the cooling time. This states that the decrease in the E-modulus of the board in this time domain is not a very crucial factor for bending. But also a smaller, time independent E-modulus (E_{eff}) has no influence on the deflection k_T .

• Row (7a,b)

checks if a further reduction of Poisson's ratio has any influence.

• Row (8a,b)

proves the linear relationship between k_F , d and F.

• Row (9a,b,c,d,e,f):

These simulations check for the influence of β on the optimized sets. The factor only influences d linearly and k_T not at all. The dependence of k_F on β is not linear in F though as can be seen from row (9f). Row (9e) uses a different factor also for comparison to the elastic material data set in the next lines.

• Row (10a,b,c,d):

Back to the elastic-orthotropic data. Optimized values for CTE and T_g and b are used to recheck to accordance with the experiment. A factor $\beta_{el}=0.85$ can be calculated for best agreement with the experimental data and comes very close also to the viscoelastic simulations. This fact is depicted in figure 4.16 where the best sets of either material behaviour are compared.

• Row (11a):

Influence of degree of orthotropism. In (11a) elastic-isotropic material data was used. The orthotropic case is (10a). The anisotropy accounts for a reduction of approximately 10% of the stiffness of the board.

• Row (12a,b,c):

Introduction of an effective board thickness according to equation 4.12 instead of an

effective modulus. This is possible for a pure board and has been checked against the experiment for three board thicknesses (see figure B.5). But for a flip-chip on board the effective E-modulus produces better results as to k_T so this version was preferred in the end.

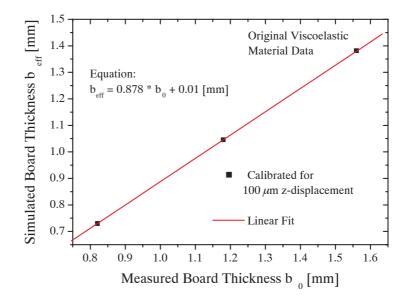


Figure B.5. Measured versus simulated data using an effective board thickness instead of an effective E-modulus.

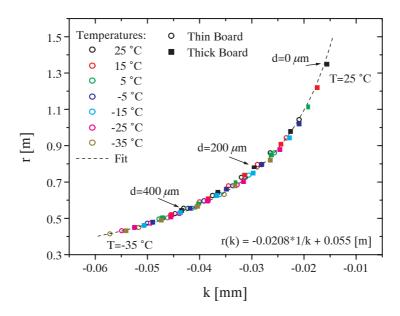


Figure B.6. The radius of curvature as a function of the deflection k. The values comprise different temperature and board thickness and displacement. To a very good approximation the inverse proportionality is confirmed and independent from the applied loads within the given range.

Board Data: Elastic vs Visco-elastic (Full Version)

_																							_															
Comment	(chronological)	measured data:	k and d linear in F	d, k_F -good, k_T -bad	Effect of Poisson's ratio	try ve: k_T still too large	try factor β	same for thick board	all values still too large	vary T_g , α	$ ext{vary} \; t_{cool}$		newly measured $lpha$	newly measured thickness b	$\operatorname{vary} b$	$\operatorname{vary} b$	$\operatorname{vary} b$	$\text{vary } t_{cool}$	has only small effect		$\text{vary } \nu$		show linearity for d, k_F		best set visco	β has no effect on k_T	best set visco	β has no effect on k_T	compare to elastic	β has no effect on k_T	adjusted set elastic	adjusted set elastic	β has no effect on k_T	best sets elastic	isotropic and elastic - stiffer	b_{eff} for 0.8 mm board	b_{eff} for 1.2 mm board	b_{eff} for 1.6 mm board
p	$[\mu m]$	100	100	81.5	91.8	73.4	90	83.5	106	106	94	94	105.8	6.66	94	90	98.5	94	94	94	96	94	94	187	98.5	70	6.66	70.3	83	70	85	83	66	97.5	7.06	26	97	100
k_F	$[\mu m]$	4.6	6.9	4.5	5	4.7	5.5	6.3	6.3	5.7	6.9	6.7	5.8	5.2	8.9	6.5	7.05	6.7	6.7	6.7	6.95	6.7	6.9	13.7	7.05	5.4	5.2	4.3	4.8	3.9	4.5	5.9	5.1	7	4.9	5.3	7	8.4
k_T	[mm]	20.3	15.8	27.2	27.2	27.8	28.3	20.1	25.3	23.5	18.1	16.6	21.5	21.1	15.51	15.3	15.7	16.45	16.17	16.02	16.28	16.4	16.6	16.6	15.7	14.9	21.1	20.5	20.9	21.1	20.6	15.2	20.6	15.5	20.4	22.3	16.7	12.7
F	[N]	7.7	20.3	7.7	7.7	7.7	7.7	20.3	7.7	7.7	20.3	20.3	7.7	7.7	20.3	20.3	20.3	20.3	20.3	20.3	20.3	20.3	20.3	40.6	20.3	20.3	7.7	7.7	7.7	5.4	7.7	20.3	7.7	20.3	7.7	7.7	20.3	43.8
β		1	ı	1	1	1	8.0	8.0	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	1	0.7	1	0.83	0.7	П	1	0.85	0.85	0.85	1	Н	1
$\alpha,T>T_g$	[ppm/K]	1.2; 140	1.2; 140	4.5; 140		4.5			1.5				1.2					1.2				1	1.5		1.2						1.2; 140				1.2	1.2		
$\alpha_{xy,xz,T< T_g}$	[ppm/K]	11.5; 42.0	11.5; 42.0	13.0; 42.0		13			12.2				11.5					12				12	12.2		11.5						11.5; 42.0				11.5	11.5		
T_g	[oC]	115-135	115-135	125		125			134	125	134	125	125					125			125		125		125						125				125	125		
$\nu_{xy,xz}$		<i>ii</i>	22	0.35, 0.15	0.15, 0.35	0.15			0.15				0.15					0.15			0.05	0.15	0.15		0.15						0.15, 0.35				0.15	0.15		
t_{cool}	[s]	300	300	300		1000			300		1000		300					300	009	1000	300		1000		300						300				300	300		
Law		<i>ii</i>	55	el-ortho		ve-iso			ve-iso				ve-iso					ve-iso			ve-iso		ve-iso		ve-iso						el-ortho				el-iso	ve-iso		
T	$[\ ^{o}C]$	160-25	160-25	160-20		160-20			160-25				160-25					160-25			160-25		160-25		160-25						160-25				160-25	160-25		
q	[mm]	0.78	1.15	8.0	0.8	8.0	8.0	1.2	8.0	8.0	1.2	1.2	8.0	0.82	1.2	1.22	1.18	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.18	1.18	0.82	0.82	0.82	0.82	0.82	1.18	0.82	1.18	0.82	0.73	1.045	1.38
#		1a	11b	2a	2b	3a	3b	3c	4a	4b	4c	4d	5a	5b	5c	2d	5e	6a	q9	99	7a	7b	8a	q8	9a(5e)	96	9c(5b)	p6	9e	96	10a	10b	10c	10d	11a	12a	12b	12c
	Units	Exp		Sim																																		

Table B.1. Detailed and chronological account of adjustment process of board data.

B.3 Soldermask

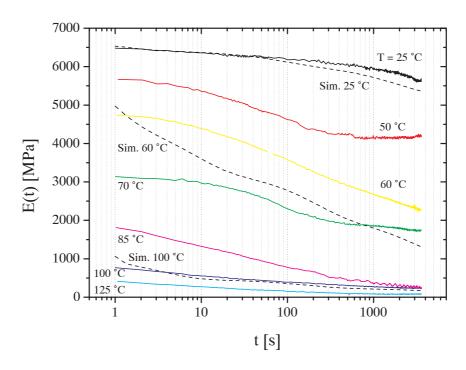


Figure B.7. Measured relaxation data of soldermask adhesive.

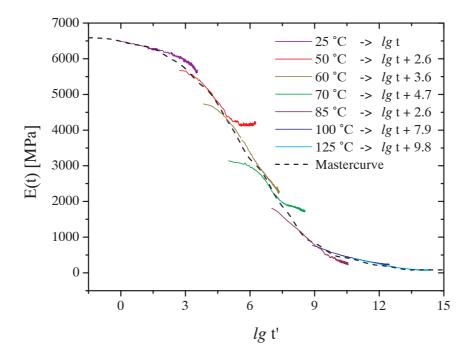


Figure B.8. Temperature-time shifted data to construct mastercurve.

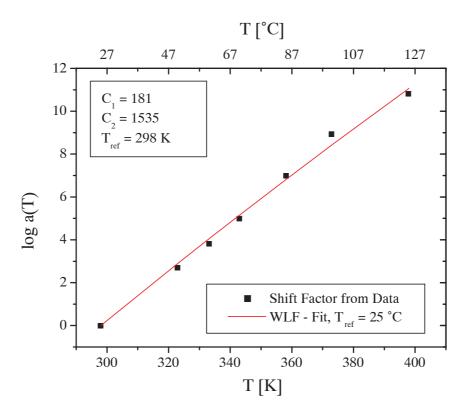


Figure B.9. WLF shift function.

The soldermask (epoxy resin) data as it was measured on a dynamic testing machine (MTS). Special clamps were used to fix the $b=100~\mu m$ thin foil. The dog's-bone specimens were cut from a sheet after etching away the copper foil it was dispensed on.

B.3. SOLDERMASK 163

B.3.1 Ansys Data File for Soldermask

```
! Soldermask: isotropic, viscoelastic, userdefined subroutine "UsrViscEl.F"
!--viscoelastic constants input for usrve5x.f
I-----
tb,evisc,mat_sm
                  ! initialize
tbda, 1, 181.0
                 ! wlf c1
tbda, 2, 1532.99
                 ! wlf c2
tbda, 4, 293
                 ! wlf tref
tbda, 5, 20
                 ! function key, must be 20
!--temperature and cte input-----
!- follows 5 temp in ascending order covering t-range of simulation
tbda, 26, 210, 273, 373, 393, 440
!- follows 5 corresponding cte values
tbda, 36, 72.9e-6, 72.9e-6, 72.9e-6, 156.4e-6, 156.4e-6
!--prony setup-----
tbda, 46, 2441.48
                    ! G0
tbda, 47, 27.3674
                    ! Ginf
tbda, 48, 7324.44
                    ! KO
tbda, 49, 7324.44
                    ! Kinf
tbda, 50, 10
                    ! # g
! -- prony coeff shear-----
tbda, 51, 0.030597294502196178
tbda, 52, 0.059023078725877635
tbda, 53, 0.10943680056118402
tbda, 54, 0.1409904718964544
tbda, 55, 0.1947144430454931
tbda, 56, 0.17721652033962254
tbda, 57, 0.16325100147644703
tbda, 58, 0.07187638056888405
tbda, 59, 0.032087381624738086
tbda, 60, 0.02080662725910286
! -- prony times shear------
tbda, 61, 1.255117014313305
tbda, 62, 78.96810063161455
tbda, 63, 1567.5991535818268
tbda, 64, 31173.843173684763
tbda, 65, 309922.3379767589
tbda, 66, 7.796365875725074e6
tbda, 67, 1.2370433351844682e8
tbda, 68, 3.137656715427452e9
tbda, 69, 1.5793444828408884e11
tbda, 70, 6.295199578594803e12
!-- end of soldermask viscoelastic data input-----
! An effective nu = 0.3 has been used for conversion of data
!-----
```

B.4 Epoxy-Silicone Adhesive

The data was measured on a Zwick 1446 universal testing machine in combination with a temperature chamber. The deviation from the expected behaviour at low temperatures is due to problems with the cooling chamber. Therefore the corresponding value was taken from the DMA measurements which in this domain does produce very good accordance with the tension testing and the rate-dependence was assumed to follow the behaviour predicted by the WLF-function.

A peculiarity was found when doing the TMA and DMA measurements: The relatively low T_g results form the two-component chemically cross-linked co-polymeric (epoxy and silicone) system. Around T_g the CTE produces a plateau, and the $\tan \delta = E''/E'$ assumes one single maximum. This is accredited to this fact, too.

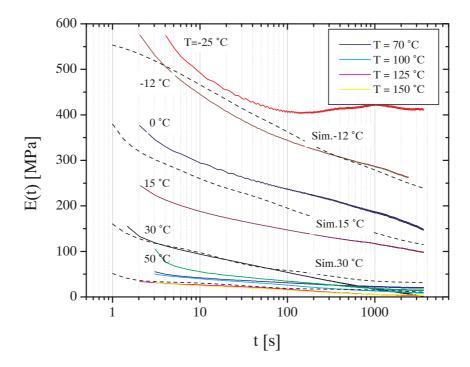


Figure B.10. Measured relaxation data of epoxy-silicone adhesive.

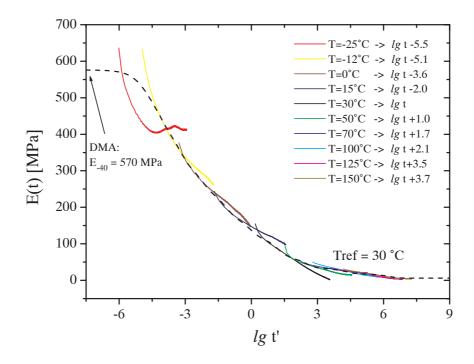


Figure B.11. Temperature-time shifted data to construct mastercurve.

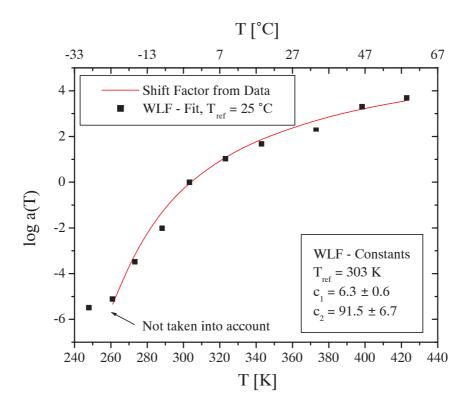


Figure B.12. WLF shift function.

B.4.1 Ansys Data File for Epoxy-Silicone Adhesive

```
!--viscoelastic constants input for usrve5x.f
!--for epoxy-silicone adhesive ------
tb,evisc,mat_ad     ! initialize
tbda, 1, 6.3
                  ! wlf c1
tbda, 2, 91.5
                 ! wlf c2
tbda, 4, 303
                 ! wlf tref
tbda, 5, 20
                  ! function key, must be 20
!--temperature and cte input-----
!- follows 5 temp in ascending order covering T-range of simulation
tbda, 26, 210, 313, 333, 353, 440
!- follows 5 corresponding cte values
tbda, 36, 90.6e-6, 90.6e-6, 1.0e-6, 102.4e-6, 102.4e-6
!--prony setup-----
tbda, 46, 221.583
                 ! GO
tbda, 47, 2.00278
                 ! Ginf
tbda, 48, 480.0
                 ! KO
tbda, 49, 480.0
                 ! Kinf
tbda, 50, 10
! -- prony coeff shear-----
tbda, 51, 0.10106419116302987
tbda, 52, 0.17329189629833477
tbda, 53, 0.19144061293761264
tbda, 54, 0.13406066700026065
tbda, 55, 0.12109937658888058
tbda, 56, 0.09447770345769652
tbda, 57, 0.09043346806500113
tbda, 58, 0.051227981346581866
tbda, 59, 0.024583576834513676
tbda, 60, 0.018320526308088367
! -- prony times shear-----
tbda, 61, 0.000012422246332449864
tbda, 62, 0.00006163258024196875
tbda, 63, 0.0004880138871352868
tbda, 64, 0.0049171171648512094
tbda, 65, 0.06199857340784209
tbda, 66, 0.7833585011853264
tbda, 67, 15.636604334249645
tbda, 68, 313.7946421922904
tbda, 69, 19878.423293103053
tbda, 70, 1.98971242703975e6
!-- end of adhesive viscoelastic data input-----
!-- used effective nu = 0.3 for conversion of data.
!-- note the low Tg and the peculiar CTE which displays a dip at 60C
!-----
```

B.5 Silicone Adhesive

The first data for this elastomer was recorded on a Zwick 1446 universal testing machine. The measured data does not respresent a qualitatively meaningful result. Only the order of magnitude of the E-modulus could be determined, the influence of temperature cannot be resolved. This is due to the fact that the very soft silicone was very difficult to clamp in the first place, thus giving rise to artifacts. Then the sensitivity limit of the load cell was obviously reached.

To make up for these shortcomings the frequency method was employed and the measurements were repeated (for high temperatures only due to lack of a cooling system) on a rheometre. The much better results can be seen in figure B.14.

Still the relaxation was not thought significant enough to arouse the need for a viscoelastic modelling of the material. As DMA measurements below T = -40 °C do show a pronounced frequency (time) dependence. But this temperature range is not important for our experiment or simulation. No CTE variation was measured either in this range since the material already works above its (typically very low) T_q for silicone.

Still the comparison of these two results clearly indicate that for very soft materials the rheometre has the edge over the relaxation test.

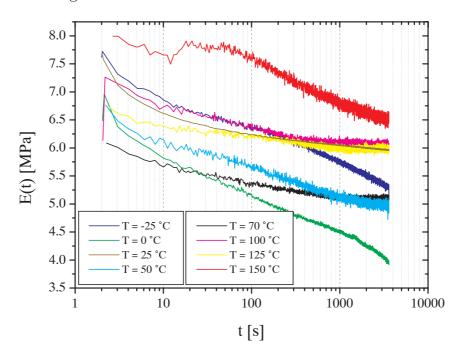


Figure B.13. Measured relaxation data of silicone adhesive. There is neither any significant relaxation nor a meaningful temperature dependence in the covered T-interval.

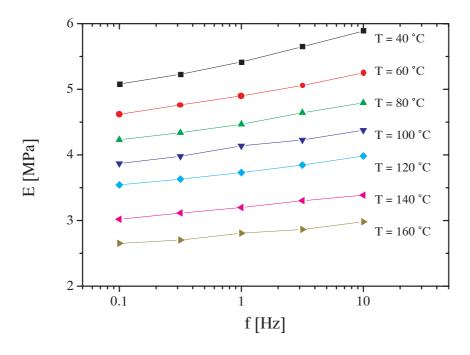


Figure B.14. Data recorded with a rheometre. This method is much better suited for soft materials.

B.5.1 Ansys Data File for Silicone Adhesive

Linear-Elastic and Elastic-Plastic: B.6 Material Data for Si, CrNi-Steel, Cu, Al, Ni

Here the employed material data for the remaining materials is given. The respective data was taken from standard literature (see e.g. [55] or [115]).

For the description of elasto-plastic materials one needs the yield stress and the tangent modulus in the plastic regime.

```
Silicon
! ------
mp, ex, mat_si, 168000 ! Elastic Isotropic Modulus
mp, nuxy, mat_si, 0.3
                      ! Poisson's Ratio
mp, alpx, mat_si, 2.8e-6 ! CTE
Steel (X5CrNi18 10)
mp, reft, mat_st, 298 ! Define: Stress-free State at Room-T mp, ex, mat_st, 220000 ! Elastic Isotropic Modulus mp, prxy, mat_st, 0.28 ! Poisson's Ratio mp, alpx, mat_st, 11.0e-6 ! CTE
mp, ex, mat_cu, 97000 ! Elastic Isotropic Modulus
mp, nuxy, mat_cu, 0.35 ! Poisson's Ratio
mp, alpx, mat_cu, 16.5e-6 ! CTE
tb, biso, mat_cu, 1 ! Isotropic Plastic Hardening tbdata, 1, 180, 6685 ! Yield Stress, Tangent Modulus
!-----
Aluminium
mp, ex, mat_al, 72000 ! Elastic Isotropic Modulus
mp, nuxy, mat_al, 0.32 ! Poisson's Ratio
mp, alpx, mat_al, 23.5e-6 ! CTE
the bire mat_al
                 ! Isotropic Plastic Hardening
! Yield Stress, Tangent Modulus
tb, biso, mat_al, 1
tbdata, 1, 180, 7000
```

Nickel

```
mptemp, 1, 233, 293, 373, 463 ! T(Kelvins) mpdata, ex, mat_ni, 1, 233000, 227500, 221300, 214400 ! E-Moduli mpdata, nuxy, mat_ni, 1, 0.3, 0.3, 0.32, 0.38 ! PR
mpdata, alpx, mat_ni, 1, 12.5e-6, 12.5e-6, 12.5e-6, 12.5e-6 ! CTE
                                                    ! Pl. Hard.
     biso, mat_ni, 1
tbdata, 1, 420, 20280
                                                    ! Y.S., T.M.
!-----
```

Appendix C

Annotations on FE-Simulation and Test-Specimen

C.1 FE-Models

C.1.1 Abaqus-Ansys Comparison

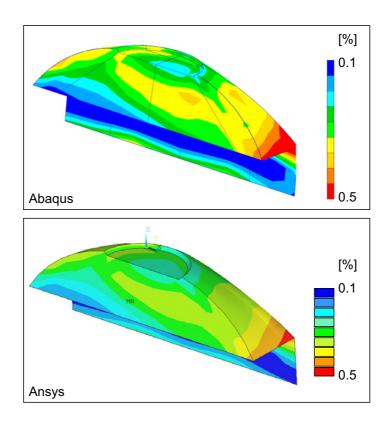


Figure C.1. Equivalent creep strain in Ansys and Abaqus. Note the qualitative and quantitative accordance of the result. (Unfortunately the scale uses different colours.) A 'slice'-model (see figure C.5) was used for comparison.

C.1. FE-MODELS

C.1.2 HEX-TET Model

TETs as well as HEX elements may be used to describe creep of solder materials. Here also a creep limit of $c_{lmt} = 10$ was specified.

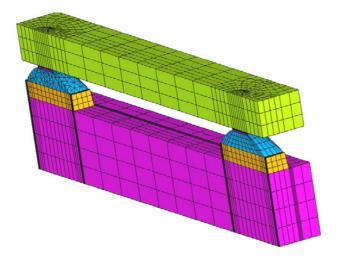


Figure C.2. The model created to compare a HEX mesh to a TET mesh. Underfill and soldermask are not depicted.

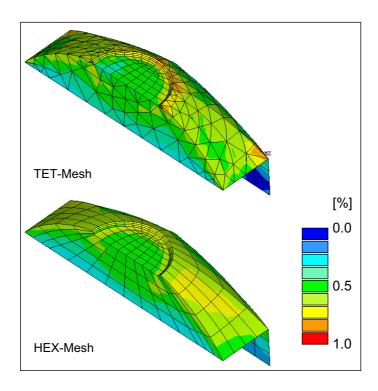


Figure C.3. Comparison of the results. Depicted is the equivalent creep strain for a sufficiently dense mesh.

C.1.3

These are the nine combinations that were tested for solution stability concerning the creep strain as described in section 4.2. The best compromise between speed and accuracy was found for the bump and the chip respectively depicted in the middle. The pictures correspond to the mesh-densities referred to in figure 4.5

Variation of the Mesh Density Parameter

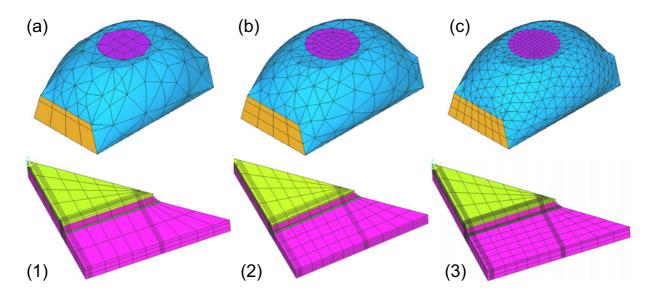


Figure C.4. Different mesh densities which were tested for numerically stable results.

C.1.4 Slice Model

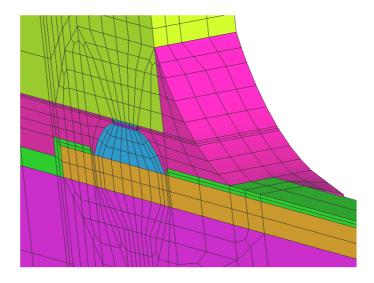


Figure C.5. FE-'slice' model for quick determination of critical parameters.

C.1. FE-MODELS

C.1.5 Stator Model

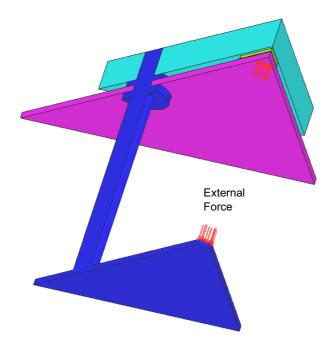


Figure C.6. Full model with stator (screw and backplate). The simulation indicates that the omission of the stator in the model does not affect the results. The elements are not depicted for the sake of clarity.

C.1.6 Solder Barrel Model

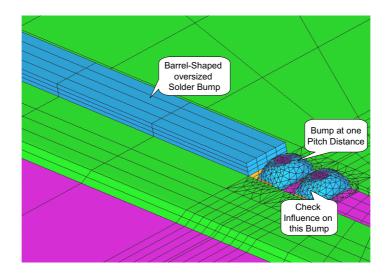


Figure C.7. Model crated to clarify the influence of a neighbouring solder bump and the omission of all but two of them. A giant solder bump (barrel) was therefore inserted.

C.1.7 Polyimide Model

The polyimide was modelled elastically by data determined through DMA measurements.

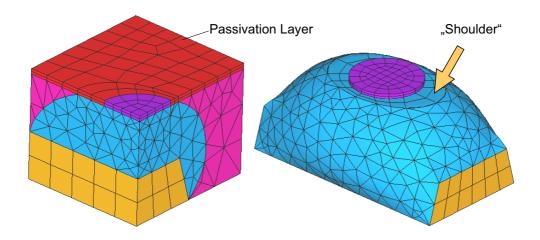


Figure C.8. FE-model adjusted to assess the influence of the presence of a passivation layer (polyimide) between chip and underfill. The bump exhibits a non-embedded UBM now, which still does not alter the result. Three element layers have been used for the polyimide.

C.1.8 Quarter Model for Verification of Curvature with Adhesive

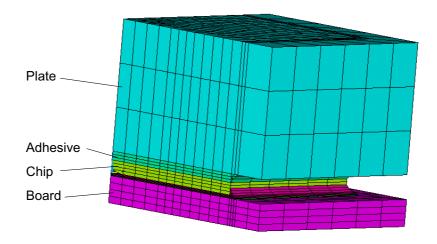


Figure C.9. FE-model to simulate the curvature of the chip measured along the edge after the chip is cut in half. This requires quarter-symmetry.

C.2 Delamination and Contact-Mode Simulation

Ansys provides the capability of contact mode simulation. This means that areas which are not adhesively bonded may come into contact and lose contact again in the course of a simulation. This situation arises when delamination occurs. No friction was assumed in the simulations due to lack of the respective parameter. Still this should be a good approximation since the very slowly varying internal forces which act at the boundary are strong enough to overcome any kind of fixation.

C.2.1 Small Local Delamination at Solder-Chip Interface (Feature of this special Bump-Shape)

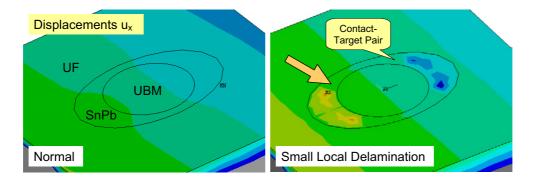


Figure C.10. Delamination at the solder-chip interface. The effect of delamination is visualized by the displacements diverging from the ones in the region around.

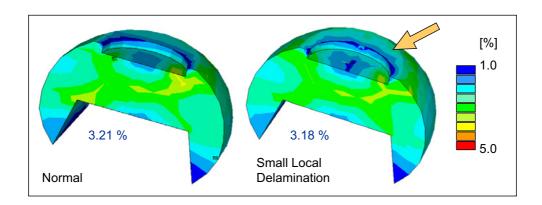


Figure C.11. The equivalent creep strain after one thermal cycle: The small local delamination has no effect on the creep strain.

As depicted in figure 5.25 this is the kind and extent of delamination which occurs at the 'shoulders' (cf. figure 5.24 (e)). The simulation shows no influence, rather there seems to be a small improvement. This means that we do not have to be concerned about a second failure mechanism apart form solder fatigue in this work.

C.2.2 Large Local Delamination at Underfill-Chip Interface

But this tendency is not a trend. Larger delamination (as does *not* occur in our model) does cause harm to the bump. Distinctly a local increase in creep strain is discernable.

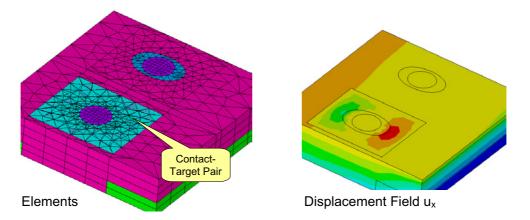


Figure C.12. Delamination at underfill-chip interface. Highlighted are the contact and target elements. Again the effect of delamination is visualized through the displacement fields. The ablation region measures one square pitch.

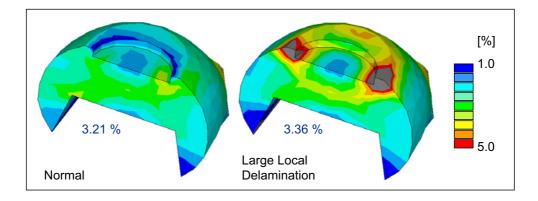


Figure C.13. The equivalent creep strain after one thermal cycle: A delamination around the pad of this size significantly increases creep strain. The maximum strains follow the damage path. Peak value is $\bar{\varepsilon}^{cr} = 6.7 \%$.

C.3 Annotations on Test-Specimen

C.3.1 Comments on Technological Constraints and Design Alternatives

For a discussion of alternative methods or materials there has been no space yet. This section is meant to briefly outline why a specific choice was made and why it was given preference over at first glance seemingly more obvious alternatives.

Type of Fixation of the Board

Many ways of attaching the board to the plate were considered involving an initial fixation, fixation with special bolts or no fixation at all. All of them had severe shortcomings either because of an incompatibility with the production steps (and hence the modelling of an technologically irrelevant method) or because the type of fixation did not establish an reproducible state but caused additional warpage of the board. The 'free' board, i.e. no fixation at all (the board merely hinges on the spacers) was ruled out due to two concerns: First, the test-specimen loses all its intrinsic stability. This may cause damage to chip and interfaces when it is put into the needle-pin adaptor for resistance measurement. Second, the spacers assume their nominal thickness only under pressure. Therefore the fixation of the board sandwiched between precision spacers and given permanence through tightening of the nuts in the last assembly step represented in every respect – apart form the other advantages already mentioned in section 4.4.2 or 4.3.1 – also the best technological solution.

Use of Aluminium as Material for the Heat-Spreader

Aluminium serves better here, since adhesives do form a strong joint to prevent delamination. Then a housing/heatsink will very likely be made of aluminium in the end. This outweighs the advantage of steel which there are: CTE close to the one of the board, higher stiffness which means a thinner plate and less thermal mass for the cycling chamber.

Use of an Aluminium Tray During Reflow

One of the problems encountered was the warpage of the boards, especially the thin ones. The initial warpage could easily be corrected by gently bending the board until it was even again. However, the warpage developing during reflow could not be remedied. But for automatic underfill dispensing also an even board is needed.

So two measures were successfully employed: First, the circuit layout and soldermask were printed on either side of the board. This helped reduce distortions due to different thermal expansion. Second, warpage could nearly be eliminated (down to $\delta d < \pm 15~\mu m$ over an area of $41 \times 41~mm^2$) when the board was laid on a thin aluminium tray during reflow. This had no influence on void formation, as the profile was designed for this purpose.

Use of Washer-like Spacers for Gap-Adjustment

Commercially available silicone spacers (tiny spheres) which are mixed into the adhesive before curing were first considered. But here again it is not clear how to simulate some randomly distributed spheres of unknown (very difficult to measure) material behaviour neither would the manufacturers provide any material data. It was therefore opted for the approach explained above.

Use of a Spring for Force Application

The spring has the advantage that its stiffness is no function of temperature in the range required here. It allows a reliable and easily adjustable way of applying a force. This renders it particularly suitable for FE-representation as a pure surface load. The spring itself need not be modelled at all. For the use in a real casing the force might be applied by another means.

Reason for Value of Gap-Width

There are two reasons: First, due to the intrinsic warpage of the board any displacement can only be adjusted to an accuracy of $\delta_d = \pm 15..20~\mu m$ (Refer to section 4.3.1 and 4.3.5). Therefore the gap was chosen to be made as wide as possible to minimize the percentage of deviation from the adjusted value. Extrapolations to smaller gap widths are made by simulation.

Second, the spacers¹ are only available in a few discrete thicknesses but have to exactly match the thicknesses b_{sp} of equation 4.15 and b_{tot} and 4.16. For reasons of comparability the gap should be identical for adhesive and foil groups, and most gap-fillers are available in thicknesses in multiples of $b_{gap} \approx 10 \ mil \approx 250 \ \mu m$. Therefore this lowest gap-width was chosen which could fortunately also be formed with a suitable combination of spacers.

¹DIN-988

Appendix D

Annotations on Results

D.1 Failure Analysis According to Single-Bump Measurements

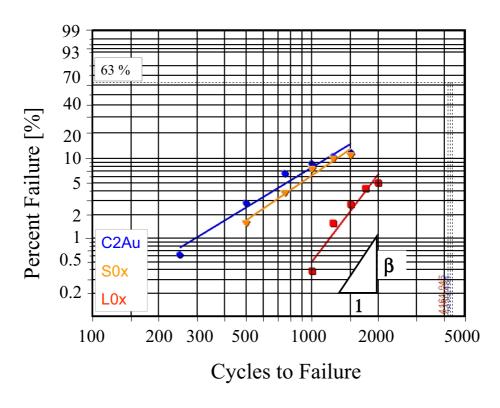


Figure D.1. Weibull plot according to all single bump failures per group for three representative groups (cf. figure 5.22). Note the difficulty in fitting the data by a straight line and the consequently vague extrapolation to $\bar{N}_{50\%}$, let alone $\bar{N}_{63\%}$. Not enough single bump failures are detectable for a meaningful analysis. A more adequate method was chosen as explained in section 5.3.2.

D.2 Tabulated Results of Simulation and Experiment

Group	n_{ch}	n_{SB}	$N_{63\%}$	$N_{50\%}$	$ ilde{N}_c$	β	CI	$\bar{\varepsilon}_1^{cr}$ [%]	$\bar{arepsilon}_2^{cr}$ [%]
K0u	20	13	1266	1144	115	3.78	80	3.21	3.47
K0x	20	18	1110	983	100	2.22	150	3.32	3.56
L0x	16	6	1465	1376	330	7.55	150	3.32	3.56
E0x	20	16	793	707	360	2.85	150	3.50	3.54
S0x	20	14	863	766	360	2.07	200	3.53	3.60
E2Mu	16	14	757	671	310	2.34	250	3.66	3.75
E1Au	16	9	720	638	330	2.14	250	4.32	3.78
E2Au	20	17	806	716	235	2.57	200	4.57	3.81
E1Ax	20	15	795	712	320	3.22	150	4.74	4.02
E2Ax	20	16	712	631	125	2.09	200	5.15	4.06
S1Au	20	17	675	599	260	2.56	200	4.40	3.89
S2Au	20	15	747	666	200	2.86	180	4.69	3.96
S1Ax	20	16	739	658	200	2.74	180	4.86	4.11
S2Ax	20	15	711	634	210	2.90	150	5.35	4.25
C1Bu	20	15	922	835	350	3.98	150	4.22	3.77
C2Au	20	15	751	665	180	2.28	200	4.51	3.79
F2Mx**	8	3	860	778	410	3.90	250	4.20	4.01
F1Au*	20	12	741	660	270	2.85	180	4.45	3.77
F1Bu*	17	11	780	693	180	2.65	220	4.53	3.76

Table D.1. Groups are sorted by kind of reverse side attachment.

Columns:

 n_{ch} - Number of chips per group;

 n_{SB} - Number of chips with a single bump failure;

 $N_{63\%}$ - Characteristic lifetime;

 $N_{50\%}$ - Mean cycles to failure;

 N_c - Correction number for daisy chain value;

 β - Weibull exponent;

CI - Confidence intervall (goodness of fit);

 $\bar{\varepsilon}_{i}^{cr}$ - Equivalent creep stain for i^{th} cycle.

The creep strain is averaged over both bumps as no significant difference was found in the experiment. For $L\theta x$ the same value as for $K\theta x$ is used since voids could not be simulated consistently. Groups with an asterisk do have other loads as originally specified (cf. table 5.4).

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