Temperature-Stable, Energy-Efficient, and High Bit-Rate 980 nm VCSELs

vorgelegt vom
Master of Science Physik
Hui Li
geb. in Rizhao

von der Fakultät II - Mathematik und Naturwissenschaften
der Technischen Universität Berlin
zur Erlangung des akademischen Grades
Doktor der Naturwissenschaften
Dr. rer. nat.

genehmigte Dissertation

Promotionsausschuss:
Vorsitzender: Prof. Dr. Michael Lehmann
Berichter/Gutachter: Prof. Dr. Dieter Bimberg
Berichter/Gutachter: Prof. Dr. Gadi Eisenstein
Berichter/Gutachter: Prof. Dr. James A. Lott

Tag der wissenschaftlichen Aussprache: 30. Juli 2015

Berlin 2015
D 83

Abstract

For over 30 years, vertical-cavity surface-emitting lasers (VCSELs) have been the subject of intensive worldwide research, due to their many applications in optical data communications, optical and spectroscopic sensing, printing, and displays. Most notably VCSELs are the key enabling technology for short-reach optical interconnects (OIs) across multimode fiber in modern data centers and petaflop-scale to exaflop-scale supercomputers. VCSELs have replaced edge-emitting laser diodes as the preferred light sources for short-reach OIs due to their significant advantages, including high bit-rates, low energy consumption, high beam quality, low manufacturing cost, and more. Optical communications provide the only reliable means of transferring large volumes of data at the ultra-high bit-rates needed in data centers. Considering cost, long-term system sustainability, and reliability, future OIs must be suited for operation without extra cooling, implying the VCSELs must be capable of operating perpetually and reliably at elevated temperatures (e.g. at 85 °C). Temperature stability can also contribute to the low energy consumption of OIs, because high bit-rate operation at constant current and voltage driving parameters provides the opportunity to dispose of cooling systems and to use simpler driver circuits. In addition to temperature insensitivity one also seeks to concurrently improve the energy efficiency and to increase bandwidth via an increased single-channel bit rate to reduce the total life cycle cost of a given VCSEL-based OI system. Future exaflop-scale supercomputers will require billions of OIs and are predicted to require high bit-rate interconnects operating at 25 Gb/s per channel or beyond. This leads to the firm requirement for future OI systems of increased bit rate and lower energy dissipation.

This work experimentally demonstrates that 980 nm VCSELs can achieve high bit-rate, temperature-stable, and energy-efficient operation concurrently with one epitaxial wafer design for the first time. It is shown that this is a result of high-speed device fabrication and careful wafer design, including the active region design, the quantum well gain-to-etalon wavelength offset design, the distributed Bragg reflector design, and a careful thermal design. Systematic experimental temperature-dependent and oxide-aperture diameter-dependent characterization are presented, including static measurements, small-signal analysis, and data transmission experiments. It is also demonstrated that VCSELs with oxide-aperture diameters between ~3 and ~4 μm are most suitable to achieve energy-efficient, temperature-stable, and high bit-rate operation at the same time. Error-free data transmissions at 38 Gb/s at 25, 45, 65 and 85 °C are achieved without any change of working point and

modulation condition by using VCSELs with oxide-aperture diameters smaller than 5 μm. Moreover, error-free data transmission at a bit rate of 42 Gb/s at room temperature is achieved, as is 38 Gb/s at 85 °C by using small oxide-aperture VCSELs. These maximum achievable data transmission bit rates match very well with the prediction from small-signal analysis. Record low energy dissipation of 139 and 177 fJ/bit for 35 and 38 Gb/s error-free data transmission at 85 °C are achieved by using ~3 μm oxide-aperture diameter VCSELs. These VCSELs are the most energy efficient VCSELs operating at 85 °C at any wavelength to date. At room temperature, only 145, 147, and 217 fJ/bit of dissipated heat energy per transferred bit are needed for 35, 38, and 42 Gb/s error-free data transmission by using a ~3 μm oxide-aperture diameter VCSEL, which are all record low heat energy dissipation for 980 nm VCSELs. A temperature-dependent and oxide-aperture diameter-dependent impedance analysis are performed to better understand the data bit rate limitations and to understand what improvements should and can be made for the next generation 980 nm VCSEL device design. Relative intensity noise (RIN) values are also given, which are low enough to satisfy the application requirements of the 32 GFC Fibre Channel standard. During the course of this dissertation, small oxide-aperture diameter (smaller than 5 μm) 980 nm VCSELs are demonstrated to be especially well suited for use in short-reach optical interconnects in high performance computers, and in board-to-board and chip-to-chip integrated photonics systems.

Table of Contents

Chapter 1
Introduction

1.1 A Brief History of VCSELs

The basic concept of a "surface-emitting injection laser" [1] that later evolved into what is now call the vertical-cavity surface-emitting laser (VCSEL), as shown in Fig. 1-1, was proposed in 1977 by Haruhisa Soda and Kenichi Iga at the Tokyo Institute of Technology [2]. The modern VCSEL structure that grew from this original idea contains a top distributed Bragg reflector (DBR) mirror, a bottom DBR mirror, and an optical cavity active region. Prof. Iga was awarded the 2013 Franklin Institute Award, the Bower Award and Prize specifically for the conception and development of the vertical-cavity surface-emitting laser and its multiple applications in optoelectronics [3]. In 1979, Prof. Iga's group demonstrated the first surface-emitting injection laser that lased under pulsed operation at 77 K [1]. This predecessor to the modern VCSEL was based on InP/GaInAsP materials, had a relatively long ~90 μm vertical optical cavity, and used thin semitransparent gold and tin layers as the top mirror and gold and zinc layers as the bottom mirror. The idea of making an all-semiconductor AlGaAs DBR via epitaxial growth by MBE originated from a paper by Jan P. van der Ziel and M. Ilegems from AT&T Bell laboratories in 1975 [4]. This pioneering work on semiconductor DBRs was followed by a similar work on 20 repeating pairs of GaAs/$Al_xGa_{1-x}As$ "multilayer reflectors" (or MLRs) grown by molecular beam epitaxy (MBE) by Matsuo Ogura *et al.* at the Electrotechnical Laboratory in Japan in 1983 [5]. In 1984 Ogura *et al.* reported an MBE-grown "surface emitting laser diode" or SLED that used 20 top periods and 30 bottom periods of Si-doped (n-doped) $Al_{0.3}Ga_{0.7}As$/GaAs DBR layers surrounding a half-lambda-thick GaAs "phase shifter layer" and zinc diffusion to form a lateral p-n junction in every GaAs layer in the DBRs [6]. The SLED emitted with pulsed excitation at about 840 nm from about 54 to 150 K. Dr. Ogura moved to the University of California

Berkeley and with his new colleagues in 1987 demonstrated a similar vertical-cavity laser diode grown by metal-organic chemical vapor deposition (MOCVD) that consisted of 20 top pairs and 60 bottom pairs of undoped $Al_{0.3}Ga_{0.7}As$/GaAs DBRs surrounding a half-lambda-thick GaAs "phase shifter layer" (about 118 nm-thick) that in fact served as an optical cavity [7]. The device structure was etched forming a rectangular pillar and then surrounded by n-type and p-type $Al_{0.4}Ga_{0.6}As$ cladding re-growth layers that were grown by liquid-phase epitaxy. In 1989, Fumio Koyama *et al.* at the Tokyo Institute of Technology reported the room temperature operation of quantum well (QW) VCSELs emitting at 894 nm [8]. The bulk GaAs optical cavity length was ~5.5 μm-thick and included a 2.5 μm-thick GaAs active layer that was surrounded by GaAs/AlGaAs layers. The vertical cavity laser diode wafer was grown by a two-step MOCVD process. The optical cavity was surrounded by SiO_2/TiO_2 dielectric DBRs on the top and bottom. The lowest threshold current achieved was 30 mA at 20 °C, and the highest achieved output power was 1.6 mW [8]. Also in 1989 Dr. Yong H. Lee (now a Prof. at Korea Advanced Institute of Science and Technology) working at AT&T Bell Laboratories with colleagues from Bellcore including Dr. Jack L. Jewell and Dr. Axel Scherer reported a ~983 nm QW VCSEL [9]. This was the first modern VCSEL with all-semiconductor DBRs as reported by Dr. Ogura but with a QW active region – a critical advance for the future success of VCSELs. The VCSEL operated continuous wave (CW) at room temperature with electrical injection. A single $In_{0.2}Ga_{0.8}As$ QW with a thickness of 10 nm was used in the active region, and the threshold current was 1.5 mA [9]. Subsequently the performance of VCSELs improved rapidly during the 1990's due in large part to the development of the molecular beam epitaxy and MOCVD semiconductor growth techniques, which make the growth of DBRs with high power reflectance possible (e.g. with $R > 0.99$) by precisely controlling the epitaxial layers thicknesses and material compositions, but also the spatial doping profiles. The golden age of VCSEL development included many pioneering contributions by research groups at the Technische Universität Berlin, the University of California Santa Barbara (UCSB), the University of Texas Austin, the University of Ulm, the Tokyo Institute of Technology, the University of New Mexico, Sandia National Laboratories, Chalmers University of Technology, the University of California Berkeley, the Ferdinand Braun Institut, and many others. The introduction of selective wet oxidation technology [10, 11] by the use of a thin oxide aperture layer buried inside an epitaxial structure in 1994 greatly improved the VCSEL performance, and made it easier to achieve room temperature CW operation with wall-plug efficiencies of 50 % or higher. The first commercial VCSELs came on the market in the middle 1990s [12, 13]. In 1990, Prof. Larry Coldren's group at UCSB achieved room temperature CW lasing operation of a 979 nm VCSEL with

a single $In_{0.2}Ga_{0.8}As$ QW, with a threshold current of only 0.7 mA [14]. In 1993, the first near room temperature (14 °C) CW operation of a 1.3 μm GaInAsP/InP VCSEL was report by Prof. K. Iga's group [15]. A buried heterostructure and MgO/Si heat sink mirror were used. The 1.3 μm VCSEL's threshold current was reduced to 22 mA. In 1993, the first AlGaInP visible light VCSELs (620 – 680 nm) operating pulsed and CW room temperature were demonstrated by James A. Lott at Sandia National Laboratories in Albuquerque, New Mexico [16–18]. Follow up work in 1995 using selective wet oxide technology to confine current and the optical modes led to red VCSELs with low threshold currents (0.66 mA) and low threshold voltages (150 mV above the photon bandgap energy of about 1.9 V at 650 nm) [19]. The first 1.54 μm VCSELs operating at room temperature were realized by the groups of Prof. Evelyn Hu and Prof. John Bowers at UCSB in 1995 [20].

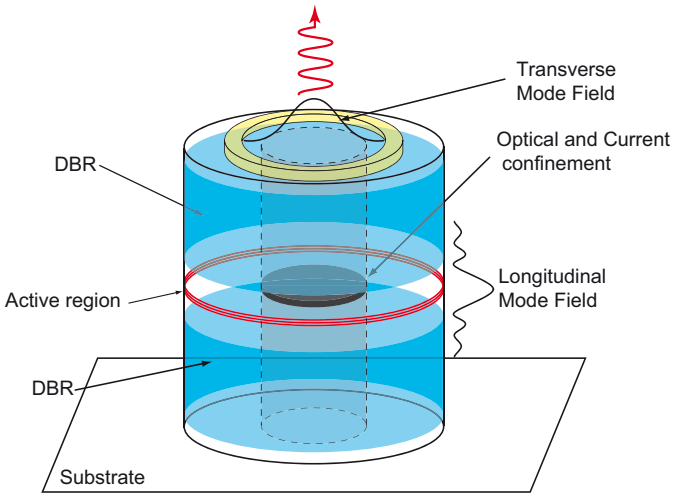

Fig. 1-1. Model of a VCSEL as described by Prof. K. Iga in [2]. The structure contains a top DBR, a bottom DBR, and an active region within an optical cavity. The QWs that comprise the gain media are placed at the center of the optical cavity formed between the two DBR mirrors. Oxidized or proton-implanted regions provide the lateral confinement for both the current and the optical mode. Carriers are injected through the metal contacts at the top and bottom of the structure and light is emitted from the top mirror. The beam profile is governed primarily by the diameter of optical and current confinement.

1.2 VCSELs for Short-Reach Optical Communication

The exponential growth in computer performance and Internet traffic has prompted the great interest in optics technologies to replace conventional electronics in data communication links. Optical interconnects (OIs) have been widely used for data centers and supercomputers, due to their advantages of higher bandwidth, lower energy consumption, and a smaller physical footprint and volume as compared to

conventional copper-based electrical interconnects [21]. One of the main challenges in data centers is to satisfy the increased bandwidth capacity while keeping a moderate level of required energy consumption, module cost, complexity, and physical space. The VCSEL-based short-reach (SR) optical links for data communication have been used since their commercial introduction by Honeywell Inc. in 1996 [12, 13]. These VCSELs have found important applications in data communications as the light-sources for optical interconnects. The demand for OIs in data centers and supercomputers is estimated to reach a market revenue of $520 million by 2019 [22]. VCSELs have become a main laser source for short-range high-speed optical links, and VCSEL light sources are a key component for the development of other OI systems including on-chip photonics. The GaAs-based VCSEL technology is presently extensively utilized in short-reach optical communication links. 850 nm VCSELs are now in volume production and are used for 10 to 28 Gb/s, multimode fiber transceivers for the ANSI Fibre Channel and Gigabit Ethernet IEEE 802.3 standards [13]. Future optical interconnects such as those envisioned in large scale integration (LSI) chips, optical circuit boards and backplanes, and multiple-core fiber systems as in supercomputers and personal computers (PCs) will continue the great demand for high performance VCSELs for the next several decades [23].

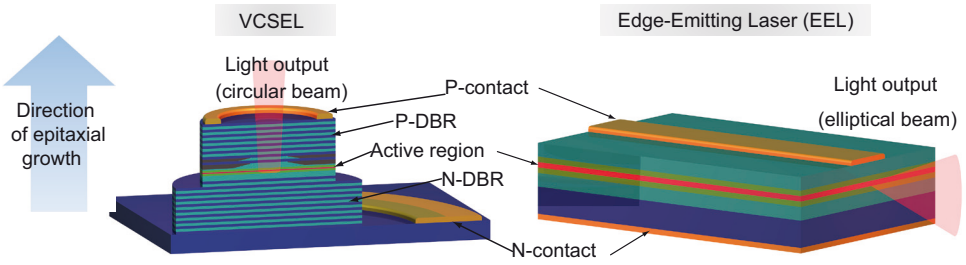

Fig. 1-2. Comparison between a VCSEL and an edge-emitting laser (EEL). The VCSEL has a circular output light beam of low divergence, and the beam direction is perpendicular to the epitaxial layers. The edge-emitting laser has an elliptical output light beam, and the beam direction is parallel with the epitaxial layers.

Table 1-1. Comparison of typical parameters between EELs and VCSELs as in [2]

Parameter	EEL	VCSEL
Active layer thickness (d)	10 nm – 0.1 μm	8 nm – 0.5 μm
Active Volume (V)	60 μm^3	0.07 μm^3
Cavity Length (L)	300 μm	≈ 1 μm
Reflectivity (R_m)	0.3 (uncoated)	0.99 – 0.999
Relaxation frequency (f_R)	< 5 GHz	> 10 GHz

1.2.1 Advantages of VCSELs

Different compared to conventional edge-emitting lasers (EELs), the VCSEL's vertical cavity is formed by the surfaces of epitaxial layers and light output is taken from one of the DBR mirror surfaces. The comparison of an EEL and a VCSEL [24] is shown in Fig. 1-2. For the VCSEL, the active layer is sandwiched between two DBRs. The light oscillates perpendicular to the epitaxial layers and exits the top or bottom mirror stack in a circular, low-diverging beam. Edge-emitters are made up of cleaved bars diced from the wafers. The two cleaved facets act as mirrors. The light oscillates along the epitaxial layers and exits through the coated cleaved facets in a high-diverging elliptical beam. Selected parameters for typical directly modulated EELs and VCSELs for data communication are given in Table 1-1 for comparison.

Table 1-2. Advantages of VCSELs compared to EELs and communication LEDs [26]

VCSELs vs. EELs	VCSELs vs. LEDs
Low threshold current	High modulation bandwidth
High efficiency at low power	Focused output beam
Slowly divergent circular beam	Narrow spectrum
Wafer-level testing, low cost	Small operating current
Simplified mounting and packaging	High output power
Two-dimensional arrays	High power conversion efficiency

Compared to conventional EELs and light-emitting diodes (LEDs) for data communications across optical fiber [25], VCSELs have many advantages as listed in Table 1-2 [26]. To satisfy the requirements for optical interconnect applications, VCSELs offer superior characteristics including [26]: 1) low threshold currents and correspondingly small driving currents to produce optical output powers in the milliwatt range, thus minimizing energy consumption and making the design of an electronic driver circuit easier; 2) excellent modulation behavior for data rates approaching 64 Gb/s [27]; 3) high power conversion efficiencies; 4) circular beam profiles with small divergence angles; 5) a wide ambient temperature range that enables uncooled operation; 6) the straightforward formation of homogeneous laser arrays that is the key to compact space division multiplexed data transmission; 7) on wafer-level device testing, yielding an enormous cost reduction; 8) the use of mounting and packaging technology that is well known from light-emitting diode production; and 9) very high reliability with projected lifetimes on the order of ten million hours at room temperature.

1.2.2 High Bit-Rate VCSELs

Future supercomputers capable of operating at tens to 100s of exaflops will require billions of optical interconnects and are predicted to require high bandwidth optical interconnects operating at single-channel bit rates of at least 25 Gb/s before 2020 [28, 29]. Google Inc. stated in 2011 that 40 Gb/s would be the desired bandwidth for their new generation datacenters [30]. Recently, 16 Gb/s Fibre Channel has begun to replace the 8 Gb/s Fibre Channel lasers, and the next major speed milestone is deployment at 25 Gb/s for the new Ethernet standard and at 28 Gb/s for the Fibre Channel standard [12]. Many industrial companies, universities, research centers, and institutes have focused their activity on the development of high bit-rate VCSELs for data communication across standard 850 nm multimode optical fiber, and significant progress has been made due to these intensive research efforts. In the following an overview of the state-of-the-art high bit-rate GaAs-based VCSEL results is presented, including the wavelengths of 850, 980, and 1100 nm.

The wavelength 850 nm is the standard for local area network (LAN) and Fibre Channel serial links. Unstrained GaAs QWs with AlGaAs barrier layers are commonly used for the active region of 850 nm VCSELs. The highest data rate achieved with GaAs QWs is 30 Gb/s at a bias current of 8 mA using 6 µm oxide-aperture diameter devices [36]. By adding indium to the GaAs active layers, compressive strain is introduced to increase the differential QW gain [37]. 32 Gb/s error-free data transmission (defined as a bit error ratio (BER) $< 1 \times 10^{-12}$) was achieved in 2009 [38]. The same year, our group at the Technische Universität Berlin reported the first 39 Gb/s error-free transmission and open eye diagram at 40 Gb/s [39]. Prof. Anders Larsson's group at Chamlers achieved 40 Gb/s error-free data transmission in 2011 [40]. In 2013, 57 Gb/s was achieved by reducing the optical cavity thickness to $\lambda/2$ to increase the photon density at the QWs and by optimizing the cavity photon lifetime [32]. By using similar 850 nm VCSELs with a bandwidth of ~26 GHz packaged in a module with a SiGe-based driver integrated circuit that incorporates feed forward equalization (FFE) and a custom-built highly sensitive and fast photoreceiver, error-free operation at 64 Gb/s was demonstrated [27].

The 980 nm high-speed VCSELs typically employ strained InGaAs/GaAs QWs. Compared with 850 nm VCSELs, 980 nm VCSELs typically have deeper QWs that suppress the escape of non-equilibrium carriers and thus have improved temperature stability. The operating voltage of 980 nm VCSELs is lower due to smaller energy bandgaps, which is important for the low voltage complementary metal oxide semiconductor (CMOS) drivers. In addition, the 980 nm VCSELs may be bottom-emitting structures due to the transparency of the GaAs substrate at 980 nm. But the

absorption loss is higher at 980 nm because the free carrier absorption coefficient of the AlGaAs material increases with the wavelength. In 2007, error-free data transmission at 35 Gb/s was achieved [41] using a 3 μm diameter VCSEL with a bias current of 4.4 mA. This VCSEL employed a tapered oxide aperture, multiple deep oxide layers, and a spatially modulated doping profile in the DBRs to lower the capacitance and the resistance, leading to a larger than 20 GHz maximum −3 dB modulation bandwidth. Our group achieved 44 Gb/s error-free operation at 25 °C in 2011 [42, 43] , and 42 Gb/s error-free operation with a 1.5λ-thick optical cavity active region [34]. Our most recent generation of 0.5λ-thick optical cavity 980 nm VCSELs achieve a −3 dB modulation bandwidth of 23.9 GHz and demonstrate error-free operation at 50 Gb/s at 25 °C [33].

For VCSELs emitting at 1100 nm their energy bandgaps are even smaller thus their operating voltages are lower than for the 980 nm VCSELs. However, the 1100 nm VCSELs typically have higher free carrier losses as compared to VCSELs emitting at shorter wavelengths. The NEC System Device Research Laboratory demonstrated 1100 nm oxide-confined VCSELs operating at bit rates of up to 25 Gb/s at 25 °C in 2006 [44], and up to 30 Gb/s [36] and 40 Gb/s [37] both in 2007 by using a buried tunnel junction [45].

Table 1-3. Selected state-of-the-art optical data transmission parameters of VCSELs at room temperature

Affiliation	UIUC [31]	CHT [32]	TUB [33]	TUB [34]	NEC [35]
Wavelength (nm)	850	850	980	980	1100
Bit Rate (Gb/s)	40	57	50	42	40
Oxide-Aper. Dia. (μm)	4	~8	4.5 − 5	~4	6
Current Density ($kA \cdot cm^{-2}$)	51.7	25.86	~50.3	43.77	17.68
Year of Publication	2014	2013	2014	2014	2007

1.2.3 High Operating Temperature VCSELs

Optical communications provide a reliable means of transferring the large volumes of data at the ultra-high bit-rates needed in data centers. Using VCSELs for data communication requires operation in an environmental temperature of up to 85 °C or higher, making reliable operation at high temperature an essential element for the development of optical components. Considering cost, energy consumption, and long-term system sustainability and reliability, optical interconnects ideally must

be able to operate without cooling at up to 85 °C or higher temperatures with low sensitivity to temperature variations. The stable performance of VCSELs against temperature variation is an important criterion of a high performance light source in optical interconnect applications.

Table 1-4. Selected state-of-the-art optical data transmission performance of VCSELs at high temperatures

Affiliation	NEC [46]	TUB [47]	TUB [48]	TUB [50]	TUB [33]
Wavelength (nm)	1100	980	980	980	980
Temperature (°C)	100	85	120	85	85
Bit Rate (Gb/s)	25	25	25	38	46
Year of Publication	2010	2010	2012	2014	2014

In 2001, data transmission at 12.5 Gb/s was measured at temperatures up to 100 °C using an 850 nm VCSEL [51]. In 2007, 20 Gb/s eye diagrams at 70 °C was reported by Agilent [52]. In 2008, our group reported 20 Gb/s error-free operation between 0 and 120 °C without any adjustment of the driving conditions using 980 nm VCSELs [53]. In 2010, the NEC System Device Research Laboratories reported 25 Gb/s error-free operation at 100 °C [46]. These device show extremely long lifetime of about 10000 hours MTTF (mean time to failure) under an ambient temperature of 150 °C and a current density of about 19 kA/cm^2. Also in 2010, our group reported error-free data transmission at 980 nm at 25 Gb/s at temperature of 25 and 85 °C without any change of working point and modulation condition [47]. In 2012, our group achieved 40, 38, 25 and 12.5 Gb/s at temperatures as high as 75, 85, 120 and 155 °C, respectively, with short 0.5λ-thick optical cavity 980 nm VCSELs [48, 54]. The Chalmers University of Technology group reported the first 40 Gb/s 850 nm VCSELs operating at up to 85 °C in 2013 [49]. The results were achieved at a modulation bandwidth of 27 GHz at 25 °C and at 21 GHz at 85 °C. In this dissertation, error-free data transmission at 38 Gb/s at 25, 45, 65 and 85 °C without any change of working point and modulation condition are achieved by using 1.5λ-thick optical cavity 980 nm VCSELs. Our new generation short 0.5λ-thick cavity 980 nm VCSELs can achieve 46 Gb/s error-free data transmission at 85 °C with a record high −3 dB modulation bandwidth of 23 GHz [33].

1.2.4 Energy-Efficient VCSELs

VCSELs will continue to be a key part of the optical interconnects market at 28 Gb/s and beyond [12]. Another key technology now under development in optical communications is Silicon Photonics. For VCSELs and multimode fiber to continue to compete favorably with Silicon Photonics, it is important to continue to focus on lower energy consumption, low cost multimode optical interconnections, and low cost packaging. The energy consumption of VCSELs is typically 2 to 10 times lower than Silicon Photonics when the total energy consumption of the entire transmitter chain is included [12]. A complete energy consumption accounting calculated by Finisar reveals the "value proposition" for using VCSELs in the data center for short reach applications [12]. The very rapid growth of global Internet traffic over the past two decades and the perpetually increasing demand for raw computational power has led to an exponential increase of energy consumption in data centers and supercomputers [55]. The efforts for "green photonics" set rigorous demands on achieving the smallest possible energy consumption. It is thus vitally important to optimize the performance and energy efficiency of high-speed VCSELs for use in optical interconnects and as the low-cost and integrated light sources for Silicon Photonics and on-chip OI systems. According to estimates and predictions based on the International Technology Roadmap for Semiconductors, laser diodes for optical interconnects must operate with a maximum energy dissipation of ~100 femtojoules (fJ) per bit by circa 2015 [56].

To compare the energy efficiency of different VCSEL designs, the electrical energy-to-data ratio (EDR) and the dissipated heat-to-bit rate ratio (HBR) are defined as [57]:

$$EDR = \frac{P_{el}}{BR} \quad \text{(fJ/bit)} \tag{1.1a}$$

$$HBR = \frac{P_{diss}}{BR} = \frac{P_{el} - P_{opt}}{BR} \quad \text{(fJ/bit)} \tag{1.1b}$$

where $P_{el} = I \cdot V$ is the input CW electrical power, I is the bias current, V is the operating voltage of the VCSEL, $P_{diss} = I \cdot V - P_{opt}$ is the dissipated power, P_{opt} is the optical output power, and BR is the bit rate. Table 1-5 summarizes the state-of-the-art high-speed 850 nm and 980 nm VCSELs performance. For 850 nm VCSELs, the best reported energy efficiency is 108 fJ/bit at room temperature for 40 Gb/s error-free data transmission [58]. For high temperature operation, 477 fJ/bit is needed for 40 Gb/s error-free data transmission using 850 nm VCSEL [49]. For 980 nm VCSELs, the best previously published power dissipation is 233 fJ/bit for 35 Gb/s error-free

operation at 25 °C [54]. In this dissertation record low 139 fJ/bit [34] and 177 fJ/bit [50] for 35 and 38 Gb/s error-free data transmission at 85 °C with a ~3 µm oxide-aperture diameter VCSEL are reported. To date, these VCSELs are still the most energy efficient VCSELs operating at 85 °C at any wavelength. At room temperature, only 145, 147, and 217 fJ/bit of dissipated energy are needed for 35, 38 and 42 Gb/s error-free data transmission with a ~3 µm oxide aperture diameter VCSEL [59], which are record low energy dissipations for 980 nm VCSELs.

Table 1-5. Selected state-of-the-art optical data transmission with 850 nm and 980 nm VCSELs

Affiliation	UIUC [31]	TUB [54]	TUB [59]	CHT [49]	TUB [50]	TUB [34]
Wavelength (nm)	850	980	980	850	980	980
Temperature (°C)	20	25	25	85	85	85
Bit Rate (Gb/s)	40	35	35	40	38	35
EDR (fJ/bit)[1]	~435	287	178	~578	230	168
HBR (fJ/bit)[2]	~395	233	145	~477	177	139
Aperture dia. (µm)	4	4	~3	7	~4	~3
Current Density ($kAcm^{-2}$)	51.7	32	38.2	25	28.6	38.2

[1]EDR: electrical energy-to-bit rate ratio. [2]HBR: heat-to-bit rate ratio.

1.3 More Applications of VCSELs

VCSELs are used in many different consumer products including in laser printers, computer mice, as sources for optical sensors, and more as depicted in Fig. 1-3 [23, 60]. One mass application of VCSELs besides optical interconnects is their use in optical mice and sensing. VCSELs offer a better performance than LEDs as illumination sources for sensing applications [61]. The market of lasers for computer mice and optical finger navigation devices, like smartphones exceeds the data communication laser market in numbers and is the second largest laser market. VCSELs are ideal illumination source for optical mice [61], because the emission profiles of the VCSEL is circular and maybe designed for a small divergence and fixed polarization, which reduces the requirements on the optics in the illumination path and allows a simple system. Additionally, VCSELs offer very low threshold currents and low energy consumption, which is especially important for battery powered devices. Single-mode VCSEL arrays are used as a light source for laser printing systems [62 – 64]. The world's first VCSEL-based electrophotographic printer was launched utilizing a 780 nm single-mode 8×4 VCSEL array. This printer features 2400 dots per inch (dpi)

resolution, which is still the highest level in the industry [65]. The laser wavelength was chosen to be 780 nm where the organic photoconductor materials have a maximum sensitivity. Each VCSEL must emit a Gaussian beam profile and operate in a single transverse mode [66]. Also, each VCSEL must emit sufficient output power to produce a latent image at the photoconductor [62]. The concept of VCSELs has also been expanded into the nanophotonics and photonic crystals fields. The ultra parallel and ultrahigh-speed photonics based upon sophisticated VCSELs including MEMS and integrated optics will begin a new era of VCSEL research [23].

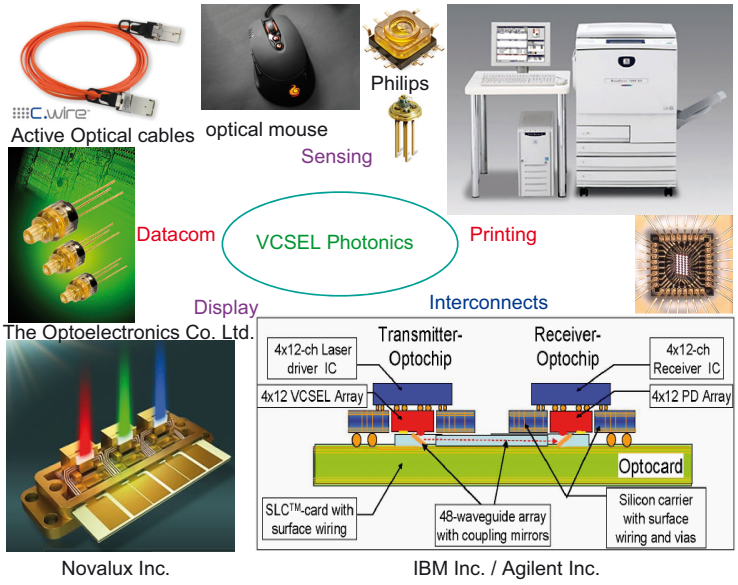

Fig. 1-3. Example application areas of VCSELs [23, 60].

1.4 Dissertation Overview

This dissertation consists of eight chapters. The first chapter is an overview of the VCSEL concept, history, and applications, especially the application for short-reach optical communication, including the requirements and the state-of-the-art of VCSELs. The second chapter includes the necessary theoretical background and design considerations, including active region design, DBR design, and suitable QW gain-to-etalon wavelength offset design, and careful thermal design. The third chapter elucidates the device structure studied in this dissertation in detail, and the simulated optical, electrical, and gain properties. In addition, the fabrication techniques, main measurements, and evaluation methods are presented. The fourth chapter presents a detailed temperature-dependent and oxide-aperture diameter-dependent impedance analysis. The impedance study provides a better understanding

of the data bit rate limitations and helps us to understand what improvements should and can be made for the next generation 980 nm VCSEL device design. In the fifth chapter, noise characteristics are investigated. These VCSELs can satisfy the requirements of bandwidth and relative intensity noise (RIN) of the 32 GFC Fibre Channel standard. In the sixth chapter, highly temperature-stable VCSELs are experimentally demonstrated. Systematic experimental characterization of 980 nm VCSELs are presented, including static measurements, small-signal analysis, and data transmission experiments. In the seventh chapter, 980 nm VCSELs that can simultaneously achieve temperature-stable, energy-efficient, and high bit-rate operation are experimentally demonstrated for the first time. From the experimental results, 980 nm VCSELs with ~3 to ~4 μm oxide-aperture diameter have small threshold currents, large mode spacing, and large *D*-factors at room temperature and at high temperatures. These results lead to low energy dissipation, and to temperature-stable and high bit-rate operation. Finally, in chapter eight, the main results are summarized and an outlook on future work based on the results of this dissertation is given.

Chapter 2

Design and Modeling of 980 nm VCSELs

A 980 nm quantum well (QW) VCSEL consists of an optical cavity active region surrounded by a top DBR and a bottom DBR, all epitaxially grown upon a GaAs substrate. A proper VCSEL epitaxial design is critical for the production of high performance devices for both commercial applications and for research. A theoretical design study of VCSEL structures is necessary to establish a first understanding of the design trade-offs, the expected device performance, and to set the goals of the research work. The active region simulation can provide an estimate of the required QW material composition and thickness, plus an understanding of the effective layer-by-layer QW spatial strain, the overall strain of the composite QW and barrier system, the theoretical differential gain, and the emission wavelength for a given set of materials. Via an $Al_xGa_{1-x}As/Al_yGa_{1-y}As$ DBR modeling and simulation analysis, the number of DBR periods required for a given top and bottom DBR power reflectance can be determined, and also the impact of various compositional DBR hetero-interfacial grading and doping schemes on DBR resistance and free carrier absorption losses can be studied. One or more $Al_xGa_{1-x}O_y$ aperture layers of various thicknesses and various AlAs mole fractions x may furthermore be added to reduce mesa capacitance and thus increase the parasitic cutoff frequency. Many other attributes of the VCSEL may be investigated theoretically prior to planning a series of experiments with device structures grown by an epitaxial growth technique including the trade-offs between the –3 dB modulation bandwidth, the photon lifetime, and the QW gain-to-etalon wavelength offset.

In this Chapter, important aspects of 980 nm VCSEL designs are presented via a theoretical framework. In Section 2.1 the basic theoretical background is reviewed, including static VCSEL equations relating cavity gain versus losses, and the theoretical dynamic properties of VCSELs as modeled by the standard laser diode rate equations. Section 2.2 presents a numerical study of strained InGaAs QW active regions. Next in Section 2.3 important aspects of DBR design are examined,

including optical calculations of the power reflectance of multilayer semiconductor DBRs, and the electrical properties of the same structure via a description of heterostructure energy band offsets, DBR heterointerface grading, and DBR doping schemes. In Section 2.4 the impact of QW gain-to-etalon wavelength offset are investigated, as it relates to the temperature performance of 980 nm VCSELs. Finally, in Section 2.5 the theoretical concepts useful for a study of the thermal performance of 980 nm VCSELs are presented.

2.1 Theoretical Background

2.1.1 Static VCSEL Properties

The lasing threshold is the lowest excitation level at which a laser's output is dominated by stimulated emission. If the gain is high enough to compensate the optical losses due to the mirrors, absorption, and scattering, the transparency condition is reached, and the laser will emit coherent light through the output mirror. The lasing condition of a one-dimensional (1D) Fabry-Pérot cavity with cavity length of L (cm) and for simplicity considering only propagating plane waves parallel to the flat opposing mirrors can be expressed as:

$$R_1 R_2 \exp[(g - \alpha_i)2L] = 1 \tag{2.1}$$

where R_1 and R_2 (both unitless and ranging from 0.0 to 1.0) are the mirror power reflectance, g (cm^{-1}) is the gain and is taken as acting uniformly over the entire cavity length L, and α_i (cm^{-1}) is the internal loss. The optical loss is typically nearly constant especially close to the lasing threshold. The threshold gain g_{th} (cm^{-1}) condition can be rearranged under this assumption as:

$$g_{th} = \alpha_i + \frac{1}{L}\ln\left(\frac{1}{\sqrt{R_1 R_2}}\right) \quad (cm^{-1}) \tag{2.2}$$

The 1D VCSEL cavity can be treated as an effective Fabry-Pérot resonator by using an effective resonator length L_{eff}, which is composed of the cavity length L_c plus the effective penetration depths of the resonant optical field intensity into the top and the bottom DBRs, given by $l_{eff,t}$ and $l_{eff,b}$, respectively. The penetration depth into a DBR is derived from a simplified model of the given DBR mirror. A DBR is replaced by a thickness of optical cavity material (l_{eff}) with an effective (average) refractive

index <n> for the multiple-layer DBR that accounts for the linear phase-shift of the optical field intensity that travels over the distance l_{eff} in the given DBR and a fixed discrete mirror with a power reflectance equal to the power reflectance of the actual DBR at the resonance wavelength [67, 68]. The threshold condition for the VCSEL cavity can then be expressed as:

$$\Gamma g_{th} = \alpha_i + \alpha_m = \alpha_i - \frac{1}{2L_{eff}} \ln\left(R_t R_b\right) \tag{2.3}$$

where $$L_{eff} = L + l_{eff,t} + l_{eff,b} \text{ and } l_{eff} \approx \frac{\lambda_{Bragg}}{4\Delta n_{Bragg}} \tag{2.4}$$

where R_{t} and R_{b} are top- and bottom-mirror power reflectance, λ_{Bragg} is the center wavelength of the Bragg-mirror, and Δn_{Bragg} is the refractive index contrast. For a VCSEL cavity, the cavity gain region does not extend over the full cavity length L_{eff} but is enclosed by larger bandgap layers to form typically a double-heterostructure. In Equation (2.3) the confinement factor Γ (unitless) is introduced to obtain the average gain in the cavity. The terms Γ_{x} and Γ_{y} are the traditional lateral confinement factors (along the x- and y-axis directions), which are self-aligned by the VCSEL's aperture and therefore can be assumed to be unity [67]. The terms can be combined as a product term $\Gamma_{\text{x}} \cdot \Gamma_{\text{y}} = \Gamma_{\text{xy}} \approx 1.0$. A final term Γ_{z} is the longitudinal (along the z-axis for a VCSEL) confinement factor.

$$\Gamma = \Gamma_{xy}\Gamma_z \approx \Gamma_z \equiv \frac{\int_{L_{act}} \left|E(\text{z})\right|^2 dz}{\int_{L_{eff}} \left|E(\text{z})\right|^2 dz} \tag{2.5}$$

where L_{act} is the total thickness of the active layers (i.e. the QWs), and $|E(z)|^2$ is the electrical filed intensity. Once the laser reaches lasing threshold, the carrier density N and gain g may be assumed to be fixed to their threshold values N_{th} and g_{th} [69]. Under this approximation the threshold current density J_{th} (A cm^{-2}) and the threshold current I_{th} (A) can be expressed as [26]:

$$J_{th} = \frac{qd_{act}}{\eta_i \tau} N_{th} \text{ and } I_{th} = A_a J_{th} \tag{2.6}$$

where q (1.602×10^{-19} C) is the electronic charge, τ (ps) is the carrier lifetime, η_{i} (unitless) is the injection efficiency, and A_{a} (cm^2) is the active area. Above the threshold current, the optical output power P (mW) from the mirrors increases linearly with driving current I [69]:

$$P = \eta_d \frac{h\nu}{q}(I - I_{th}) \tag{2.7}$$

where η_d (unitless) is the differential quantum efficiency, which can be obtained from a measurement of the slope of the output power-current (PI) characteristic. The η_d defined as the number of photons out per electron [69], contains the current injection efficiency η_i and the photonic quantum efficiency η_p. The term η_p is the fraction of the generated coherent light that is available for top (or bottom) emission, which determined by the ratio of τ_p (s) and $\tau_{p,m}$ (s):

$$\eta_d = \eta_i \eta_p = \eta_i \frac{\tau_p}{\tau_{p,m}} \approx \eta_i \frac{\alpha_m^T}{\alpha_i + \alpha_m^T + \alpha_m^B} = \eta_i \frac{-\frac{1}{L_{eff}} \ln(\sqrt{R_t})}{\alpha_i - \frac{1}{L_{eff}} \ln(\sqrt{R_t R_b})} \tag{2.8}$$

where τ_p is the photon lifetime which is related to the internal cavity loss rate $\alpha_{i(rate)}$ (s^{-1}), and $\tau_{p,m}$ is the photon lifetime which is related to the coupling mirror loss rate $\alpha_{m(rate)}$ (s^{-1}) (in this example the top (*T*) DBR mirror is used as the coupling mirror), as expressed [26]:

$$\tau_p \approx \frac{1}{\alpha_{i(rate)} + \alpha_{m(rate)}^T + \alpha_{m(rate)}^B} \text{ (s) and } \tau_{p,m} \approx \frac{1}{\alpha_{m(rate)}^T} \text{ (s)} \tag{2.9}$$

Equation (2.9) is for top-emitting VCSELs. For bottom-emitting VCSELs, $\alpha_{m(rate)}$ for the top mirror should be replaced by the bottom (*B*) mirror loss rate. Note that $\alpha_{(rate)} = \langle v_g \rangle \cdot \alpha$, thus relating a power loss rate to a power loss per distance. The wall plug efficiency is defined as the ratio of coherent light output power and electrical input power, and can be expressed as:

$$\eta_{WPE} = \frac{P}{I \cdot V} \text{ (unitless)} \tag{2.10}$$

2.1.2 Dynamic VCSEL Properties

Rate equations are used to analyze the intrinsic dynamic behavior of semiconductor lasers. The single mode equations that describe the supply and the loss of the carriers and photons within the active region [69] are:

$$\frac{dN}{dt} = \frac{\eta_i I}{qV_a} - \frac{N}{\tau} - v_g g N_p \tag{2.11a}$$

$$\frac{dN_p}{dt} = \Gamma v_g g N_p + \Gamma \beta_{sp} R_{sp} - \frac{N_p}{\tau_p} \tag{2.11b}$$

where N (cm^{-3}) is the carrier density, N_p (cm^{-3}) is the photon density, η_i is the injection efficiency or internal quantum efficiency, I (mA) is the injection current, q is the electronic charge, V_a (cm^3) is the active region volume, τ (s) is the carrier lifetime, v_g is the group velocity of the lasing mode, g is the gain, Γ is the optical confinement factor, β_{sp} is the spontaneous emission factor, R_{sp} is the spontaneous recombination rate, and τ_p is the photon lifetime. Equation (2.11a) is for the carrier density in the active region, and (2.11b) is for the photon density of the lasing mode in the cavity. Interestingly the single mode rate equations can be used to describe and understand the intrinsic dynamic modulation behavior of multimode VCSELs, because the dynamic behavior of index-guided multimode VCSELs with highly overlapping transverse intensity fields have approximately uniform transverse carrier and photon densities and thus exhibit a single relaxation resonance frequency very similar to a single mode VCSELs [70–72]. The small-signal response can be obtained by superimposing a small sinusoidal modulating current on the bias current. The modulation transfer function $H_i(\omega)$ is defined as [69, 73]:

$$H_i(\omega) \equiv \frac{\omega_R^2}{\omega_R^2 - \omega^2 + j\omega\gamma} \tag{2.12}$$

where $\omega_R = 2\pi f_R$ is the relaxation resonance angular frequency, and γ (s^{-1}) is the damping factor. This transfer function is in the form of a second-order low pass filter with a damped resonance peak [69, 73]. The relaxation resonance frequency is the natural oscillation frequency between the carriers and photons in the laser cavity and can be approximately expressed as [69]:

$$f_R = \frac{\omega_R}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{\eta_i \Gamma v_g}{q.V_a} \cdot \frac{(\partial g / \partial N)}{\chi}(I - I_{th})} \tag{2.13}$$

where $\partial g/\partial N$ (cm^2) is the differential gain, I_{th} (mA) is the threshold current, and χ (unitless) is the transport factor. The D-factor [74] characterizes the dependence of the relaxation resonance frequency on the driving current, and can be expressed as:

$$D = \frac{f_R}{\sqrt{(I - I_{th})}} = \frac{1}{2\pi}\sqrt{\frac{\eta_i \Gamma v_g}{q \cdot V_a} \cdot \frac{(\partial g / \partial N)}{\chi}} \quad \text{(GHz/(mA}^{1/2}\text{))} \tag{2.14}$$

The modulation current efficiency factor (*MCEF*) is another commonly used figure-of-merit to evaluate and compare the overall high-speed performance of one or more VCSELs, as given in equation (2.15) [75].

$$MCEF = \frac{f_{-3dB}}{\sqrt{(I - I_{th})}} \tag{2.15}$$

where $f_{-3\mathrm{dB}}$ is the –3 dB bandwidth of the modulation response, which is defined as the frequency when:

$$\left|H(f_{-3dB})\right|^2 / \left|H(0)\right|^2 = 1/2 \tag{2.16}$$

The damping represents the rate of energy loss in the cavity, which effectively reduces the strength of the resonance peak. The damping γ (s^{-1}) increases linearly with the square of f_r. The proportionality is the *K*-factor

$$\gamma = K \cdot f_R^2 + \gamma_0\,,\ K = 4\pi^2\left(\tau_p + \frac{\varepsilon \cdot \chi}{v_g\left(\partial g / \partial N\right)}\right)\ (s^{-1}) \tag{2.17}$$

The bandwidth of a VCSEL is also determined by the extrinsic electrical parasitic response besides the intrinsic laser response. The effects of parasitic equivalent circuit elements can be approximated by a single-pole low-pass filter function with a cut-off frequency f_P. Then the overall small signal modulation response of a laser diode may be approximated by a three-pole transfer function, by introducing the additional effects due to the parasitic elements into the intrinsic laser transfer function.

$$H(f) = H_i(f) \cdot H_{par}(f) = \frac{f_R^2}{f_R^2 - f^2 + j \cdot f \cdot \left(\frac{\gamma}{2\pi}\right)} \cdot \frac{1}{1 + j \cdot \left(\frac{f}{f_P}\right)} \tag{2.18}$$

According to equation (2.18) the small signal modulation response and thus the high speed physical properties of a laser diode can be described using three parameters: the relaxation resonance frequency f_R, the damping factor γ, and the parasitic cut-off frequency f_P. Accordingly, there are three physical limits that restrict speed performance of VCSELs: thermal limits, damping limits, and parasitic limits. The general approach toward increasing the speed of a laser diode is to increase f_R by increasing the differential gain and by reducing the active region volume. The reduction of mode volume can be accomplished by reducing the oxide-aperture diameter or by reducing the penetration depth of the optical field into the VCSEL mirrors. Based on these methods to overcome the limitation of the f_R, several optimization considerations of high-speed VCSELs are as follows:

1. reduction of electrical parasitics by minimizing the resistance and capacitance;
2. optimization of the active layer to provide a high differential gain;
3. improvement of thermal conductivity and a reduction of heat generation;
4. improvement of the optical confinement; and
5. optimization of the photon lifetime (i.e. the trade-off between the relaxation resonance frequency and the damping).

2.2 Active Region Design

High bit-rate and temperature-stable VCSELs are required for short-reach (up to about 300 m) optical data transmission. As discussed in section 2.1.2, a larger differential gain for the QWs in the active region generally leads to a higher modulation bandwidth. In addition, an increase of the relaxation resonance frequency can be obtained with a larger differential gain, which in turn enables a higher –3 dB modulation bandwidth to be reached. In this section, a detailed numerical study is presented for selecting QW and barrier layer designs that can satisfy the requirements for the active regions of 980 nm VCSELs.

Table 2-1. Parameter values of selected binary semiconductors GaAs, InAs, and GaP at room temperature [78]

Parameter	GaAs	InAs	GaP
Lattice constant a_0 (Å)	5.65325	6.0583	5.4505
Elastic stiffness constant C_{11} (10^{11}dyn cm^{-2})	11.879	8.329	14.05
Elastic stiffness constant C_{12} (10^{11}dyn cm$^{-2)}$	5.376	4.526	6.203
Luttinger parameter γ_1 (unitless)	6.98	20.0	4.05
Luttinger parameter γ_2 (unitless)	2.06	8.5	0.49
Luttinger parameter γ_3 (unitless)	2.93	9.2	1.25
Hydrostatic deformation potential a (eV)	–8.33	–6.08	–9.9
Shear deformation potential b (eV)	–2.0	–1.8	–1.6

2.2.1 Critical Layer Thickness

For the epitaxial growth of lattice mismatch material, the theoretical maximum thickness for an epitaxial layer should be below a certain critical layer thickness in order for this layer not to experience misfit dislocations. The dislocations form at the interface between the strained layer and the lattice-matched layer or layers (the lattice-matched layer or layers are taken to be infinitely thick). The critical layer thickness h_c (Å) can be calculated for a zinc-blende III-V semiconductor by using the standard Matthews-Blakeslee mechanical equilibrium model as [76]

$$h_c = \frac{a_{epi}}{\kappa\sqrt{2}\pi f}\frac{1-0.25\nu}{1+\nu}\left(\ln\frac{h_c\sqrt{2}}{a_{epi}}+1\right) \tag{2.19}$$

where a_{epi} is the natural relaxed (unstrained) lattice constant of the epitaxial layer, a_{sub} is the lattice constant of the substrate layer. $f = (a_{epi} - a_{sub}) / a_{epi}$ is the misfit strain, and v (unitless) is the Poisson ratio, defined as $v = C_{12} / (C_{11} + C_{12})$, where C_{11} and C_{12} are the elastic stiffness constants. The term κ is a constant with the value of 1, 2, and 4 for a superlattice structure, a single QW surrounded on both sides by infinitely-thick lattice-matched layers, and a single strained layer on an infinitely-thick substrate, respectively [76]. Linear interpolation [77] from the binary material endpoints are used to obtain the basic parameters for ternary compound semiconductor materials. In Table 2-1, useful parameters of relevant binary semiconductors are shown [78].

2.2.2 Compressively-strained InGaAs QWs

Compressively-strained InGaAs QWs are commonly used for the active region of 980 nm VCSELs, and GaAs and GaAsP are two candidate barrier materials. The compressive strain of InGaAs for different indium compositions and the tensile strain of GaAsP grown on GaAs with different phosphorus compositions are show in Fig. 2-1(a), which shows the strain increase with the increase of the compositions of indium and phosphorus. The critical layer thickness h_c for a single pseudomorphic $In_xGa_{1-x}As$ QW surrounded on both sides by infinitely-thick GaAs barrier layers, is calculated with the mechanical equilibrium model [76] in Equation (2.26). The result is shown in Fig. 2-1(b). These values should not be exceeded in order to prevent the formation of misfit dislocations. Multiple (usually five QWs) compressively-strained InGaAs layers surrounded by GaAs barrier layers or tensile-strained GaAsP layers are usually used for 980 nm VCSEL active regions, and thus the resultant critical thickness of the QW and barrier layers in the active region is more complicated than for a single strained epitaxial layer on an infinite substrate.

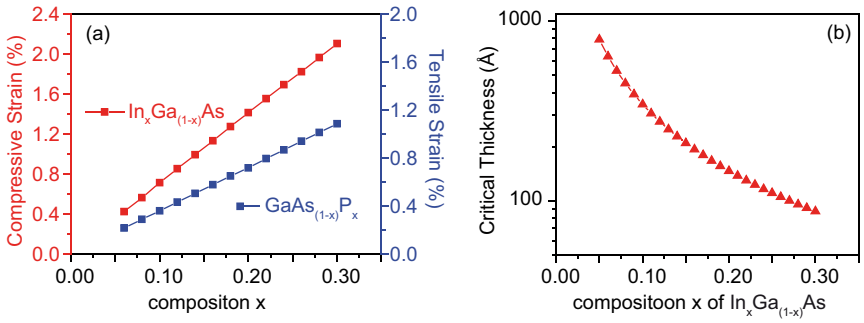

Fig. 2-1. (a) Compressive-strain change with the indium-arsenide composition x of $In_xGa_{1-x}As$ layer and tensile strain change with phosphorus composition x of $GaAs_{1-x}P_x$ layer, both realtive to the lattice constant of GaAs, and (b) calculated critical layer thickness h_c change with indium composition x by using κ = 2 in equation (2.26) according to the mechanical equilibrium model.

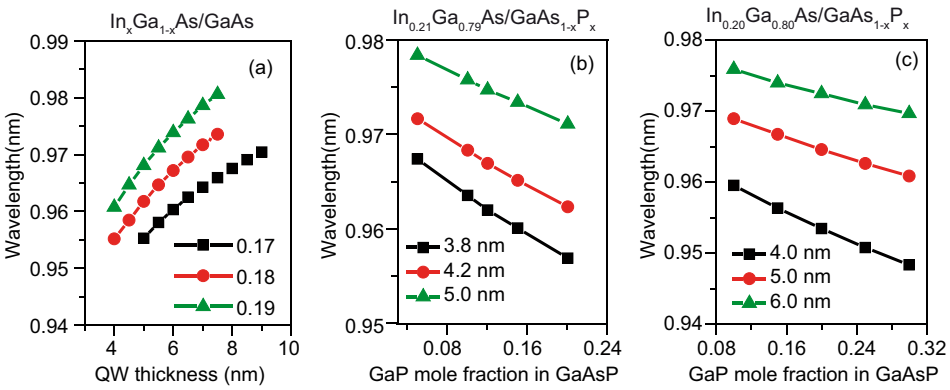

Fig. 2-2. Peak emission wavelengths versus the QW thickness for (a) $In_{0.17}Ga_{0.83}As/GaAs$, $In_{0.18}Ga_{0.82}As/GaAs$, and $In_{0.19}Ga_{0.81}As/GaAs$ QW/barrier materials, and the peak emission wavelengths as a function of the GaP content for (b) $In_{0.21}Ga_{0.79}As/GaAs_{(1-x)}P_x$ and (c) $In_{0.20}Ga_{0.80}As/GaAs_{1-x}P_x$ QW/barrier materials.

The calculated emission wavelength (i.e. the energy transition between the n = 1 electron level and the n = 1 heavy-hole level) as a function of QW thickness for $In_{0.17}Ga_{0.83}As$, $In_{0.18}Ga_{0.82}As$, and $In_{0.19}Ga_{0.81}As$ single QWs surrounded on both sides by GaAs barrier layers (for modeling purposes taken to be infinitely-thick) are shown in Fig. 2-2(a). The emission wavelength increases toward longer wavelengths with increasing QW thickness. The emission wavelengths are 955 and 970 nm for 5 and 9 nm-thick $In_{0.17}Ga_{0.83}As/GaAs$ QWs, respectively. For QWs with the same thickness, the expected peak emission wavelength increases with increasing indium content, which is because the energy bandgap decreases with increasing indium content. For a 6 nm-thick QW, the emission wavelengths are 960, 967 and 974 nm for $In_{0.17}Ga_{0.83}As$, $In_{0.18}Ga_{0.82}As$, $In_{0.19}Ga_{0.81}As$ QWs, respectively. This means the thickness of QWs should be decreased to maintain a certain constant emission wavelength when increasing the indium composition x in the $In_xGa_{1-x}As$ QWs. For strain compensation of the $In_xGa_{1-x}As$ QW by using tensively strained $GaAs_{1-x}P_x$ barrier layers, different phosphorus content x of the $GaAs_{1-x}P_x$ barrier layers are considered in the calculations to determine the influence on the emission wavelengths. Calculated results for $In_{0.21}Ga_{0.79}As/GaAs_{1-x}P_x$ and $In_{0.20}Ga_{0.80}As/GaAs_{1-x}P_x$ QW/barrier systems are shown in Fig. 2-2(b) and 2-2(c). For a fixed indium content and thickness in the QWs, the emission wavelength shifts to shorter wavelengths with an increase of the phosphorus content x. When the tensively strained $GaAs_{1-x}P_x$ barrier layers are fixed in composition and taken to be infinitely thick, the emission wavelength increases with an increase of the thickness of InGaAs QWs. The final emission wavelength of a QW and barrier layers depends on the net results of three impact factors, which are the indium content, the thickness of the QW, and the particular barrier material (i.e. the resultant conduction and valence band offsets, effective masses, QW-barrier

interface sharpness, etc.). Additionally, the use of coupled multiple strained QWs and barriers further complicates the calculation of emission wavelength, net gain, overall average strain of the QW/barrier active region, and more.

2.2.2.1 The Influence of Strain on QWs

As already mentioned, the indium concentration of compressively strained InGaAs QWs surrounded by GaAs barrier layer can be varied to reach certain emission wavelengths. A more detailed study of the effects of compressive strain on the gain properties of InGaAs QWs are conducted to determine the change of the gain peak wavelength, and transparency carrier density as a function of strain. Five $In_xGa_{1-x}As$ QWs are investigate here, including $In_{0.17}Ga_{0.83}As$, $In_{0.18}Ga_{0.82}$ As, $In_{0.19}Ga_{0.81}As$, $In_{0.20}Ga_{0.80}As$, and $In_{0.21}Ga_{0.79}As$, each surrounded by infinitely-thick GaAs barrier layers. These compressively-strained QWs lattice-matched to GaAs have corresponding compressive strains of 1.20, 1.27, 1.34, 1.41 and 1.48 %, respectively. The QWs used in the following study have the same 6 nm thickness and same GaAs barrier layers. The band alignment diagrams of the $In_xGa_{1-x}As$/GaAs QWs are calculated using the model-solid theory [79, 80]. This theory may be used to predict reliable values for the experimentally observed energy band lineups in a wide variety of test cases and can be used to explore which combinations and configurations of strained and unstrained epitaxial materials layers will lead to the desired electronic properties for an active QW gain region as used in a semiconductor laser diode. The principal feature of the model-solid theory consists of assuming the alignment of band structure on an absolute energy scale. This puts all calculated energies on an absolute energy scale, and allows us to derive the energy band lineups by simply subtracting values for individual semiconductors. For the real-space energy band diagrams plotted in Fig. 2-3, the $In_{0.21}GaAs$/GaAs QW/barrier system has the largest conduction and valence band offsets, which is beneficial for hole and electron confinement [81]. Note that in Fig. 2-3 there are separate band offsets for the heavy-holes

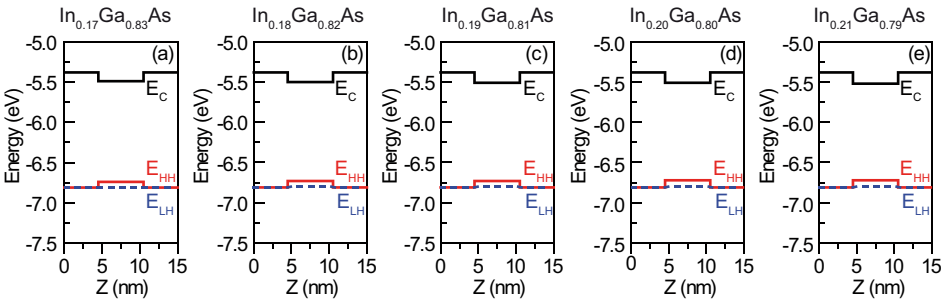

Fig. 2-3. Real-space charge neutral energy-band diagrams showing the conduction and valence bands for (a) $In_{0.17}Ga_{0.83}As$/GaAs; (b) $In_{0.18}Ga_{0.82}As$/GaAs; (c) $In_{0.19}Ga_{0.81}As$/GaAs; (d) $In_{0.20}Ga_{0.80}As$/GaAs; and (e) $In_{0.21}Ga_{0.79}As$/GaAs QWs.

(solid lines) and the light holes (dashed lines). The valence subbands are calculated using the k•p theory [82, 83]. An advanced three-dimensional simulator Crosslight (PICS3D) [84] is used for the calculations in this work, which self-consistently combines quantum well band structure calculations by using the k•p theory, radiative and nonradiative carrier recombination, carrier drift and diffusion, and optical mode computation. Based on the k•p theory, the valence subbands, optical gain spectra, transparency carrier densities, and maximum differential gain for the InGaAs QW with different compressive strains are calculated. The valence subbands for the $In_xGa_{1-x}As/GaAs$ QWs are shown in Fig. 2-4. The QWs with higher strain (increasing indium) have a larger energy separation between the first heavy hole HH1 and first light hole LH1 subband at the Γ point (Wave Vector = 0). This leaves more carriers for the C1-HH1 (conduction band n = 1 quantized electron energy level to heavy-hole n = 1 quantized energy level) transitions to improve the material gain, as shown in Fig. 2-5(a).

The gain spectra are calculated at a fixed carrier density of 3×10^{18} cm^{-3} for transverse-electric (TE) polarization at 300 K. The gain peak shifts to longer wavelengths as the strain in the QW increases (thus as the amount of indium increases). Fig. 2-5(b)

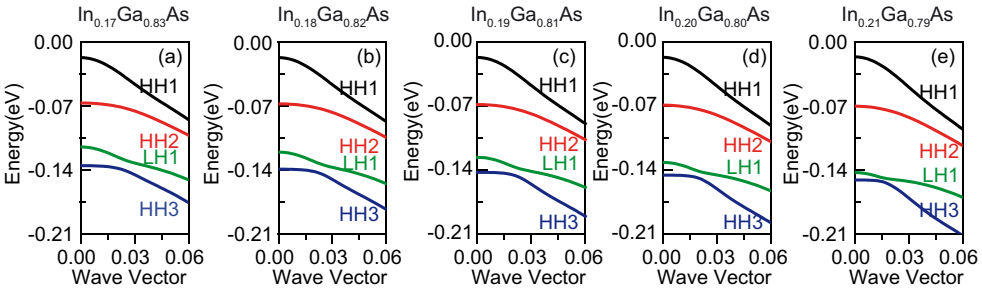

Fig. 2-4. K-space dispersion of the valence heavy-hole and light-hole subbands for (a) $In_{0.17}Ga_{0.83}As/GaAs$; (b) $In_{0.18}Ga_{0.82}As/GaAs$; (c) $In_{0.19}Ga_{0.81}As/GaAs$; (d) $In_{0.20}Ga_{0.80}As/GaAs$; and (e) $In_{0.21}Ga_{0.79}As/GaAs$ QWs with the hole subband energies versus the in-plane (transverse) wave vector k_t normalized by $2\pi/a_0$ ($Å^{-1}$), where $a_0 = 5.6533$ Å is the lattice constant.

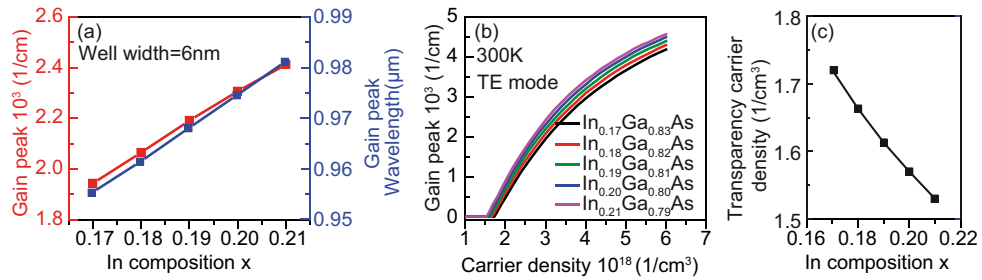

Fig. 2-5. (a) Gain peak and gain peak wavelength change with indium composition, (b) peak gain as a function of carrier density, and (c) transparency carrier density versus the indium composition for $In_{0.17}Ga_{0.83}As/GaAs$, $In_{0.18}Ga_{0.82}As/GaAs$, $In_{0.19}Ga_{0.81}As/GaAs$, $In_{0.20}Ga_{0.80}As/GaAs$, and $In_{0.21}Ga_{0.79}As/GaAs$ QWs, all at room temperature.

shows the calculated peak material gain as a function of carrier density for the single $In_xGa_{1-x}As$/GaAs QW/barrier structures at 300 K. The QWs with a larger strain have smaller transparency carrier density due to the higher valence band curvature (as in the E versus k diagrams in Fig. 2-4), which leads to a smaller joint densities of states, making it easier to achieve a population inversion. The gain characteristics of $In_xGa_{1-x}As$ QWs can be improved by adding a certain compressive strain (emission wavelength and critical thickness should be considered). Higher compressively strained $In_xGa_{1-x}As$ QWs have a higher material gain and lower transparency carrier concentration.

2.2.2.2 The Influence of QW Thickness

The QW thickness is another important factor that influences the peak emission wavelength and gain properties. The QW thickness needed to maintain good electron and hole wave-function overlap is from 2 to 10 nm. In addition, the QW thickness cannot exceed the critical layer thickness limit h_c to avoid misfit dislocations. Fig. 2-6(a) shows the gain peak and the gain peak wavelength as a function of the thickness of $In_{0.19}Ga_{0.81}As$ QWs that are surrounded by GaAs barrier layers at a fixed carrier density of 3×10^{18} cm^{-3} for TE polarization at 300 K. The emission wavelength shifts to a longer wavelength with increasing the QW thickness. Also, the material gain increases rapidly when QW thickness increases from 4 to 6 nm, and achieves a maximum value at a QW thickness of 6.5 nm, then the emission wavelength decreases with further increases of the QW thickness. When the QW thickness is thin (less than ~6.5 nm), the L energy band valley will also fill with electrons, which reduces the number of available carriers that can fill the Γ energy band valley. As the Γ band valley has the larger impact on QW material gain, the reduced number of available carriers for Γ energy band valley filling leads to a lower material gain of the thinner $In_{0.19}Ga_{0.81}As$ QWs. In contrast when the QW thickness further increases (i.e. ~6.5 nm and thicker), the injected carrier confinement in the eakens

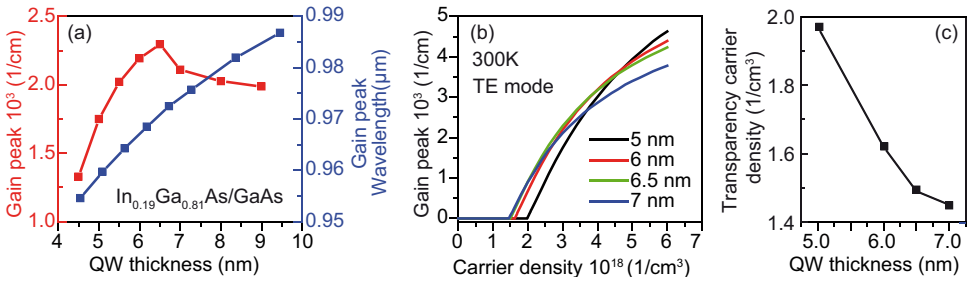

Fig. 2-6. (a) Gain peak and gain peak emission wavelengths versus QW thickness, (b) peak gain as a function of carrier density, and (c) transparency carrier density change with QW thickness for $In_{0.19}Ga_{0.81}As$/GaAs QWs.

and this leads to a decrease of material gain. Fig. 2-6(b) shows the peak material gain of the TE mode as a function of carrier density for QW structures at 300 K. The thicker QW has a smaller transparency carrier density. An $In_{0.19}Ga_{0.81}As$/GaAs QW with a thickness of 6.5 nm has a large material gain and a small transparency carrier density. For QWs with a fixed strain, an optimized QW thickness can be chosen to achieve a high material gain and a low transparency carrier density.

2.2.2.3 Comparison of InGaAs QW designs for 980 nm VCSELs

Based on the analysis in the previous sections, the following QW structures are chosen to analyze as candidates for the active region of 980 nm VCSELs, as listed in Table 2-2. The indium concentration varies from 17 to 19 % for these InGaAs QWs with GaAs barrier layers. The thicknesses of the QWs are chosen to set the gain peak wavelength close to 965 nm. The resultant QW thicknesses do not exceed the critical layer thickness limit.

Table 2-2 The QW structures chosen to analyze and compare

QW material	Barrier material	QW thickness (nm)	Barrier thickness (nm)
$In_{0.17}Ga_{0.83}As$	GaAs	7.0	3.5
$In_{0.18}Ga_{0.82}As$	GaAs	5.6	4.7
$In_{0.19}Ga_{0.81}As$	GaAs	4.5	5.6

The gain spectra of the candidate QWs at a fixed carrier density of 3×10^{18} cm^{-3} for TE polarization at 25 and 85 °C are plotted in Fig. 2-7. The $In_{0.17}Ga_{0.81}As$ QW (7.0 nm-thick) has a higher material gain than the other two structures at both 25 and 85 °C. This result is the combination of the effects of strain and QW thickness. The effect of QW thickness is overwhelmed by the effect of strain. With increasing indium content from 0.17 to 0.19, the material gain increases as the strain increases, but in order to keep the same emission wavelength, the QW thickness is decreased from 7.0 to 4.5 nm, leading to a decrease in material gain. Also, the QW peak gain wavelengths shift into longer wavelength for all three studied QW structures, and the peak material gain decreases when temperature increases from 25 to 85 °C. Thus, both strain and layer thickness of the QWs are very important for high gain QWs, and both influences should be considered. The $In_{0.177}Ga_{0.823}As$/GaAs QWs are used for the active region of one of our 980 nm VCSEL designs [43, 54] , and achieved reasonable performance both at room temperature and at high temperature.

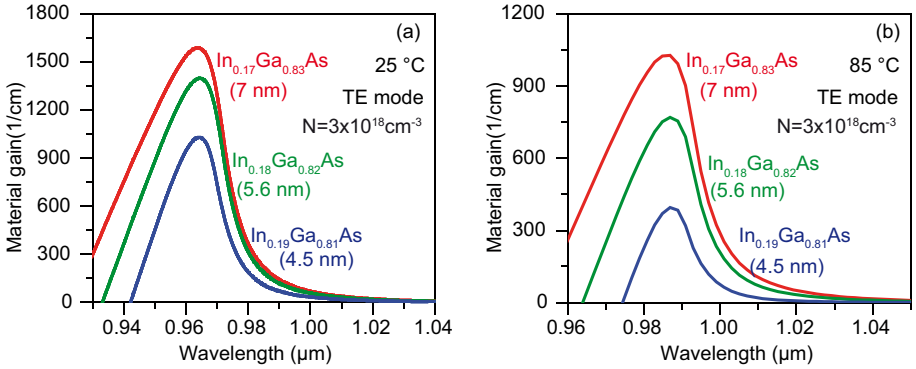

Fig. 2-7. Calculated material gain spectra for $In_{0.17}Ga_{0.83}As$/GaAs (7 nm-thick QW), $In_{0.18}Ga_{0.82}As$/GaAs (5.6 nm-thick), and $In_{0.19}Ga_{0.81}As$/GaAs (4.5 nm-thick) QWs at a fixed injected carrier density of 3×10^{18} cm^{-3} for TE polarization at (a) 25 °C and (b) 85 °C.

2.2.3 Strain-Compensated InGaAs/GaAsP QWs

GaAs barrier layers [85, 86] are commonly used to surround the compressively strained InGaAs QWs for the active region of GaAs-based 980 nm VCSELs. GaAsP is another candidate barrier material [33, 47], where the GaAsP layers are in tensile strain and serve to partially counter the compressive QW strain. In order to show the difference, $GaAs_{0.88}P_{0.12}$ barrier layers with 0.43 % tensile strain and no-strain GaAs barrier layers are chosen to surround the $In_{0.21}Ga_{0.79}As$ QWs. The QW thickness is chosen to be 4.2 nm, the barrier thickness is 6 nm, and thus the combined single $GaAs_{0.88}P_{0.12}$/$In_{0.21}Ga_{0.79}As$/$GaAs_{0.88}P_{0.12}$ QW structure lattice-matched to GaAs is below the critical layer thickness limit. The band alignment of $In_{0.21}Ga_{0.79}As$/$GaAs_{0.88}P_{0.12}$ and $In_{0.21}Ga_{0.79}As$/GaAs QWs are calculated using the model-solid theory [79], and the results are shown in Fig. 2-8. The use of GaAsP barrier layers results in a better band alignment of the strain-compensated QWs compared to standard $In_{0.21}Ga_{0.79}As$/GaAs QWs. For $In_{0.21}Ga_{0.79}As$/GaAs the conduction band offset is 0.15 eV. The conduction band offset of $In_{0.21}Ga_{0.79}As$/$GaAs_{0.12}P_{0.88}$ QWs is 0.18 eV, 20 % larger than the $In_{0.21}Ga_{0.79}As$/GaAs QWs. An increased conduction band offset and valence band offset is beneficial for the electron and hole confinement [81] and also can reduce the thermal escape of carriers [88]. VCSELs with strain compensated $In_{0.21}Ga_{0.79}As$/$GaAs_{0.88}P_{0.12}$ QWs will have less temperature sensitivity, enabling the VCSELs to have a better performance at high temperature, which has been proven by experimental comparison [89]. The valence subbands are calculated using the k•p theory [82, 83]. The results are shown in Fig. 2-8(c) and 2-8(d). One can see that $In_{0.21}Ga_{0.79}As$/$GaAs_{0.88}P_{0.12}$ QWs have a larger energy separation at the Γ point than the standard $In_{0.21}Ga_{0.79}As$/GaAs QWs, between the first heavy hole HH1 and the first light hole LH1 subband. Also the in-plane effective mass of the holes become lighter

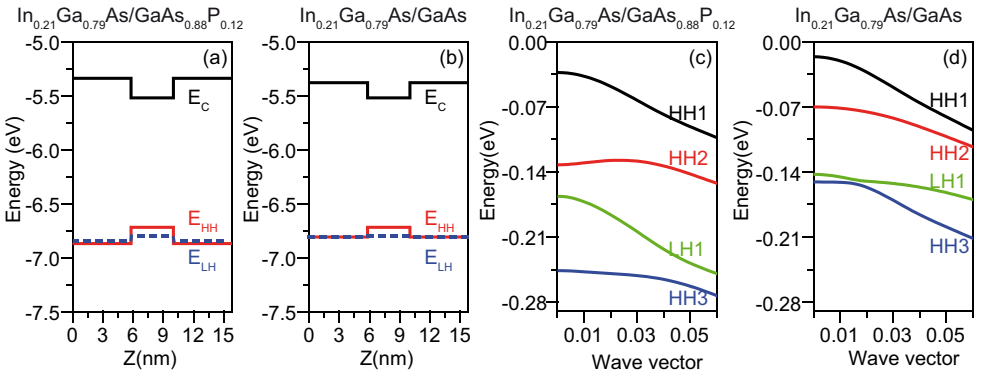

Fig. 2-8. Real-space energy-band diagram showing the conduction and valence bands of an $In_{0.21}Ga_{0.79}As$ (4.2 nm-thick) QW with $GaAs_{0.88}P_{0.12}$ barrier layers (a) and GaAs barrier layers (b). *k*-space dispersion of the valence heavy-hole and light-hole subbands for $In_{0.21}Ga_{0.79}As$ QWs surrounded by $GaAs_{0.88}P_{0.12}$ barriers (c) and GaAs barriers (d) with the hole subband energies versus the in-plane wave vector normalized by $2\pi/a_0$ ($Å^{-1}$), where a_0 = 5.6533 Å is the lattice constant of GaAs at 25 °C.

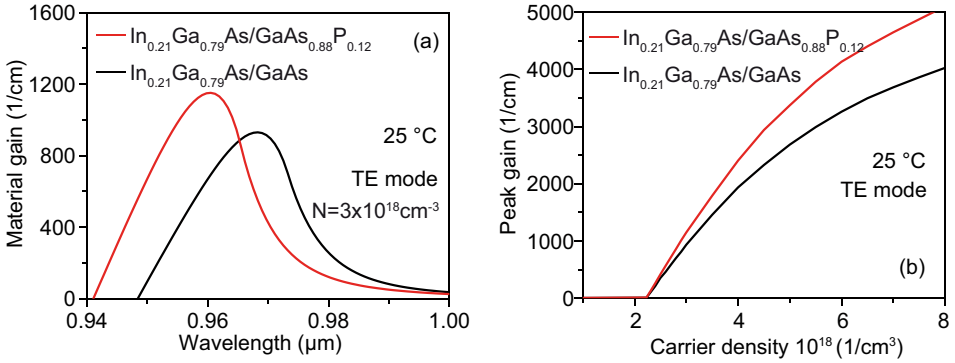

Fig. 2-9. Calculated material gain spectra (a) and peak material gain as a function of carrier density (b) for $In_{0.21}Ga_{0.79}As/GaAs$ and strain-compensated $In_{0.21}Ga_{0.79}As/GaAs_{0.88}P_{0.12}$ QWs at a fixed injected carrier density of 3×10^{18} cm^{-3} for TE polarization at 25 °C, both QWs have the thickness of 4.2 nm.

[90]. The carrier filling is mainly related to the in-plane (perpendicular to the growth direction) effective mass of the holes, and thus the density of states in the valence and conduction bands are more closely matched, the population inversion is earlier achieved at lower injection carrier density, resulting in a higher differential gain and lower transparency carrier density [91, 92].

The optical gain spectra calculated at a fixed carrier density of 3×10^{18} cm^{-3} for TE polarizations at 300 K are shown in Fig. 2-9(a). Partially strain-compensated $In_{0.21}Ga_{0.79}As/GaAs_{0.88}P_{0.12}$ QWs have higher material gain than normal $In_{0.21}Ga_{0.79}As/GaAs$ QWs. The peak material gain as a function of carrier density at 300 K are shown in Fig. 2-9(b). The partially strain-compensated $In_{0.21}Ga_{0.79}As/GaAs_{0.88}P_{0.12}$ QW has a slightly smaller transparency carrier density, which is beneficial for low threshold current, and has a higher material gain and differential gain (larger increase of slope of the gain versus the carrier density). As discussed in section 2.1.2,

larger differential gain is very important for high bit-rate performance, not only essential for higher –3 dB modulation bandwidth, but also indicates the ability to achieve high modulation bandwidth at low bias current.

2.2.4 Summary

The peak gain wavelength is determined by the composition of the QW material, barrier material, and QW thickness. An optimized QW design for the active region of 980 nm VCSELs should have large band offsets, high material gain, low transparency carrier density, and high differential gain, which will result in a large relaxation resonance frequency, and ultimately a large –3 dB modulation bandwidth.

2.3 DBR Design

DBR mirrors composed of $Al_xGa_{1-x}As/Al_yGa_{1-y}As$ are commonly used for GaAs-based VCSELs. VCSELs have a limited round-trip gain due to their short cavity and therefore rely on highly reflective mirrors, where the power reflectance usually is 0.99 (99 %) or higher for the output coupling mirror and 99.9 % or higher for the other high-reflector mirror. The DBR mirrors consists of a stack of quarter-wavelength layers with alternating high- and low- refractive index to reach a very high power reflectance above 99 %. At 980 nm with AlGaAs/GaAs DBR layers more than 20 DBR periods are generally needed to achieve a power reflectance higher than 99 %. There will be more than 40 total DBR periods in the top and bottom DBRs, which is the main part of the entire VCSEL epitaxial wafer structure that also contains the largest number of hetero-interfaces of the VCSEL structure. Therefore, a proper and careful electrical design of the DBR mirrors is very important. Since the thicknesses of the DBR layers are defined by the lasing wavelength, the main goal of the electrical simulations is to improve the conductivity of the mirrors, mainly by reducing potential barriers at the interfaces, which arise from the different material compositions and thus different energy band gaps of the corresponding materials used in the DBR mirrors. Increasing the doping level can reduce the electrical resistances, but will generally increase free carrier absorption losses, which means the doping level needs to be chosen to carefully balance the trade-off of resistance and loss simultaneously. The DBR mirrors for 980 nm VCSELs are used as an example to show the effect of grading the DBR interface layers and the effect of various doping levels on the DBR's electrical and optical properties.

2.3.1 Electrical Design of DBR Mirrors

A lot work has been done before seeking to optimize the interfaces inside a DBR mirror. Different schemes were investigated [93], for example composition linear grading, step grading [94], biparabolic grading [95], uniparabolic grading [95], modulation doping [96], or delta-doping (δ-doping) at the interfaces to lower the resistance of the DBR. Linear compositional grading layers are used in this work to improve the mirror conductivity because these can be easily grown by standard MOCVD techniques. Additionally, no significant differences are found between the previously listed grading schemes. The thicknesses of linear compositional grading layers are important, and the exact sequence and spatial density of dopants within the DBRs is found to be indeed important as well.

2.3.1.1 The Influence of Grading Layer Thickness

The Al-composition for $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$ DBR mirrors without and with 10, 16, and 20 nm linear compositional grading is shown in Fig. 2-10(a). Only one and a half periods of the DBR are shown for more clarity. As electron mobility is approximately 20 times higher than hole mobility, the main source of serial resistance is the p-DBR layers, and it is thus important to lower the resistance of the p-DBR layers. The energy band diagrams are calculated using Nextnano software [97] in this work. The energy band diagram results for a p-doping level of 2×10^{18} for $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$ DBR mirrors without and with 20 nm-thick compositional linear grading is showed in Fig. 2-10(b) and 2-10(c), in which energies of different minima and maxima in the conduction and the valence bands are shown. The energy band gap of $Al_xGa_{1-x}As$ is direct for aluminum-arsenide compositions x from 0 up to ~0.41 − 0.45 (the lowest energy occurs at the Γ-point), while for higher compositions (x > 0.45), AlGaAs becomes an indirect semiconductor with the X-valley minima

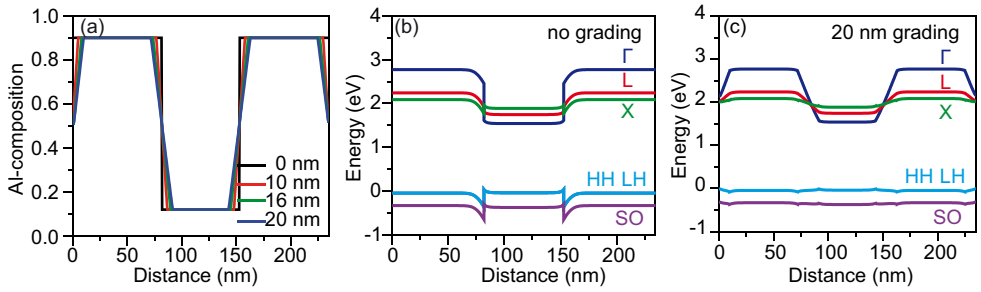

Fig. 2-10. Aluminum composition (x) for $Al_{0.12}Ga_{0.9}As/Al_{0.9}Ga_{0.1}As$ DBR mirrors with 0, 10, 16, 20 nm linear grading layer (a), and band diagram including Γ, X and L conduction bands and heavy-hole HH, light-hole LH and split-off SO valence bands of p-doping level of 2×10^{18} for the $Al_{0.12}Ga_{0.9}As/Al_{0.9}Ga_{0.1}As$ DBR without (b) and with 20 nm (c) grading layers.

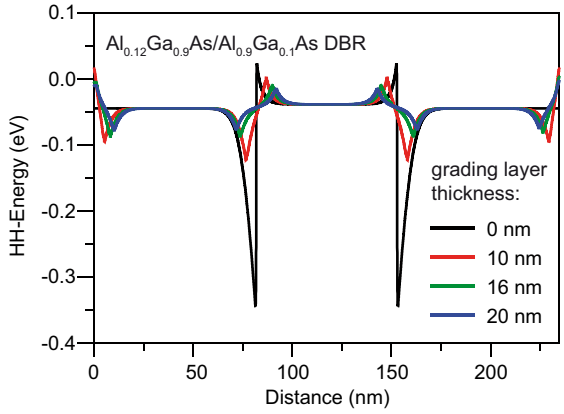

Fig.2-11. Heavy-hole HH valence band diagram of p-doping level of 2×10^{18} for the $Al_{0.12}Ga_{0.9}As/Al_{0.9}Ga_{0.1}As$ DBR without and with 10, 16 and 20 nm grading layers.

having the lowest energy in the conduction band. In Fig. 2-10(b), the potential barriers between two different aluminum composition materials ($Al_{0.12}Ga_{0.88}As$ and $Al_{0.90}Ga_{0.10}As$) for holes in the valence band is considerably large for DBRs without grading layers. This downward peak barrier adds to the difficulty to move holes, which makes this barrier the main source of series resistance for the p-DBR. In addition, these barriers in the p-DBR increase the voltage drop of the VCSELs. By using a 20 nm-thick compositional linear grading layer, this barrier is reduced obviously, which means a huge improvement of conductivity and smaller resistance.

In order to see the improvement in conductivity of a DBR with different thickness grading layers, a zoomed-in view of the heavy-hole band minimum is shown in Fig. 2-11. The height of the potential barrier for holes reaches ~0.4 eV with an ungraded DBR, and decreases into ~0.1 eV for the DBR with 20 nm-thick graded layers, which means the potential barriers can be effectively suppressed by adding a grading layer at every hetero-interface in the DBR. Moreover, the height of the potential barrier has a large decrease of ~0.27 eV by adding 10 nm grading layers, but a slower decrease with a further increase of the thickness of the grading layers. When the grading layer thickness is larger than 16 nm, the decrease of the potential barrier becomes very small, which means extra-thick grading layers will not noticeably further improve the hole conductivity, but will degrade the optical properties of the DBR. The compositional linear grading layers used for AlGaAs DBR mirrors with thickness between 16 to 20 nm are thus suitable for low resistance 980 nm VCSELs.

2.3.1.2 The Influence of Doing Level

Increased doping levels is another method to increase the conductivity of DBRs. The energy of the heavy-hole band minimum for $Al_{0.12}Ga_{0.9}As/Al_{0.9}Ga_{0.1}As$ DBR with 20 nm linear compositional grading layers is shown in Fig. 2-12, including the cases of different p-type doping levels of 5×10^{17}, 1×10^{18}, 2×10^{18}, and 3×10^{18} cm^{-3}. By

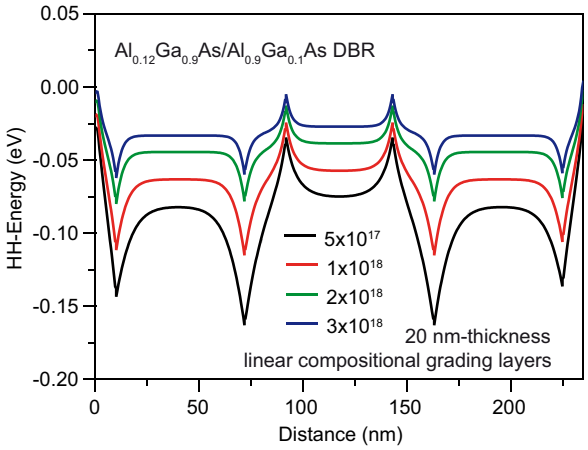

Fig. 2-12. Heavy-hole valence band diagram of p-doping level of 5×10^{17}, 1×10^{18}, 2×10^{18}, and 3×10^{18} for the $Al_{0.12}Ga_{0.9}As/Al_{0.9}Ga_{0.1}As$ DBR with 20 nm linear compositional grading layers.

increasing the p-doping level from 5×10^{17} to 2×10^{18} cm^{-3}, the interface improves drastically. The height of the potential barriers for holes decreases significantly, and a further increase to 3×10^{18} cm^{-3} results in smaller improvement, but at the same time higher doping levels increase free carrier absorption losses.

Figure 2-12 shows that increased doping levels can reduce the downward peak barriers and lower the electrical resistance, but potentially introduce more carrier absorption loss. Modulation doping profiles can be used to simultaneously achieve low resistance and low loss. The p-doped DBR for the VCSELs structure used in this work is chosen as an example to show the effect of a modulation doping profile. Two different doping levels are used in the VCSEL structure. For the first 5 DBR pairs near the active region where the electric filed intensity is high relatively low doping levels are used to avoid strong optical losses, which is 2×10^{18} cm^{-3} for the high refractive index layers, low refractive index layers, and grading layers. Higher doping levels are used for the next 19 DBR mirror pairs where the electric filed intensity is lower. The doping level is 3×10^{18} cm^{-3} for the high refractive index layers and the low refractive index layers, and 4×10^{18} and 5×10^{18} cm^{-3} for the two graded layers in each period, as show in Fig. 2-13(a). Fig. 2-13(b) shows that the hole concentration has two peaks, one is in the node of the optical standing cavity wave, which won't add to the optical absorption loss, as they are located at the intensity nulls. However, the other peak is in the position of the grading layer when the aluminum-arsenide composition x increases from 0.12 into 0.9. This high hole concentration will add optical absorption loss. A lower doping level for this grading layer (from low aluminum-arsenide composition x increasing to high composition x) in the future design should be used to further lower the optical loss.

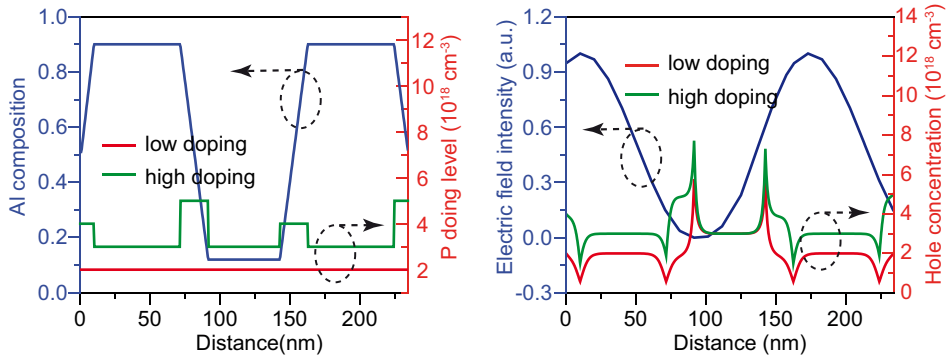

Fig. 2-13. Aluminum-composition and doping level (a) for first 6 pair low-doped and 19 pair high-doped p-type $Al_{0.12}Ga_{0.9}As/Al_{0.9}Ga_{0.1}As$ DBR with 20 nm grading layers, and corresponding normalized electric field intensity and free hole concentration (b).

2.3.2 Optical Design of the DBR Mirrors

The optical properties of multilayer dielectric structures can be calculated using the 2 × 2 transfer matrix method [69, 80]. Crosslight software [84] is used for the calculations in this work. Increasing the number of DBR pairs and the refractive index contrast between the high refractive index and low refractive index materials increases the mirror power reflectance. For the 980 nm VCSEL structure used in this work, $Al_{0.12}Ga_{0.9}As/Al_{0.9}Ga_{0.1}As$ layers with a refractive index difference $\Delta n = 0.4391$ at 980 nm are used for both top- and bottom-DBR mirrors. The high refractive index layer is $Al_{0.12}Ga_{0.9}As$, with a real refractive index at 980 nm of n = 3.4433 and a quarter-layer thickness of 71 nm. The low refractive layer is $Al_{0.9}Ga_{0.1}As$, with a refractive index at 980 nm of n = 3.0042 and a quarter-layer thickness of 81.5 nm. The power reflectance for the top- and bottom-DBRs is calculated using the transfer matrix method [69]. Fig. 2-14(a) shows the calculated power reflectance of the top 24 period DBR including two $Al_{0.98}Ga_{0.02}As$ layers placed within two of the low-index layers for the wet oxidation, using transfer matrix method. The power reflectance at 980 nm is R = 0.9975 for 24 DBR pairs with 20 nm-thick DBR grading layers. For comparison, the power reflectance for a 24 period DBR without the grading layers is also shown, which is R = 0.9978, a little higher than for the DBR with the 20 nm-thick grading layers. In addition, the stop-band width is slightly decreased. The grading layers thus have a small impact on the optical property. Fig. 2-14(b) shows the power reflectance for the 37.5 period bottom DBR, where the power reflectance at 980 nm is R = 0.9998 for the 37.5 period DBR with 20 nm-thick grading layers. For comparison, R = 0.9999 for the DBR without the grading layers. The stop-band width is also slightly decreased when grading layers are used.

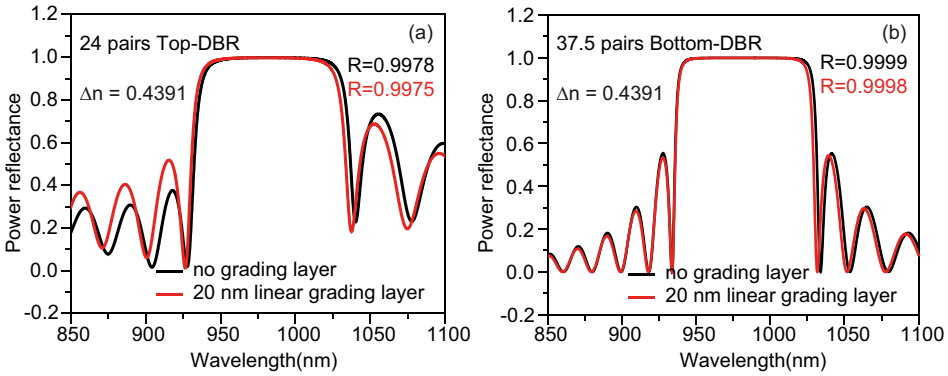

Fig. 2-14. Power reflectance as a function of the wavelength of the 24 pair $Al_{0.12}Ga_{0.9}As/Al_{0.9}Ga_{0.1}As$ top-DBR without and with 20 nm grading layers including two $Al_{0.98}Ga_{0.02}As$ layers for the wet oxidation (a). Power reflectance as a function of the wavelength of the 37.5 pair $Al_{0.12}Ga_{0.9}As/Al_{0.9}Ga_{0.1}As$ bottom-DBR without and with 20 nm grading layers (b).

2.4 QW Gain-to-Etalon Wavelength Offset Design

In this section, the reason why a –15 nm QW gain-to-etalon wavelength offset is particularly suitable for temperature-stable VCSELs is briefly explained. The effects of the gain-to-etalon wavelength offset on both the static and high-speed modulation properties of VCSELs are discussed. The research goal is to achieve high bit-rate operation from 25 to 85 °C and highly temperature stable operation across a large temperature range simultaneously.

2.4.1 The Effect on Static Properties

The three-dimensional cavity resonant modes determine the emission wavelengths of VCSELs. Due to the typically short horizontal planar cavity with perpendicular, z-direction optical thickness of an integer multiple of λ/2 the VCSEL's free-spectral range is typically larger than the spectral width of the QW gain, thus only one longitudinal resonant cavity etalon mode overlaps with the gain. As is well known a room temperature offset between the QW's gain peak wavelength and the cavity etalon wavelength can be introduced in VCSELs such that these wavelengths align at elevated operating temperatures [98]. The result may be a relatively flat threshold current versus temperature behavior across a broad range of temperatures and a highly temperature insensitive output power-current (L-I) characteristic from threshold up to several mA of forward bias. Fig. 2-15(a) shows the calculated material gain based on the k•p theory [82] for the $In_{0.21}Ga_{0.79}As$ QWs with $GaAs_{0.88}P_{0.12}$ barrier layers at a fixed carrier density of 3×10^{18} cm^{-3} for TE polarization at temperatures

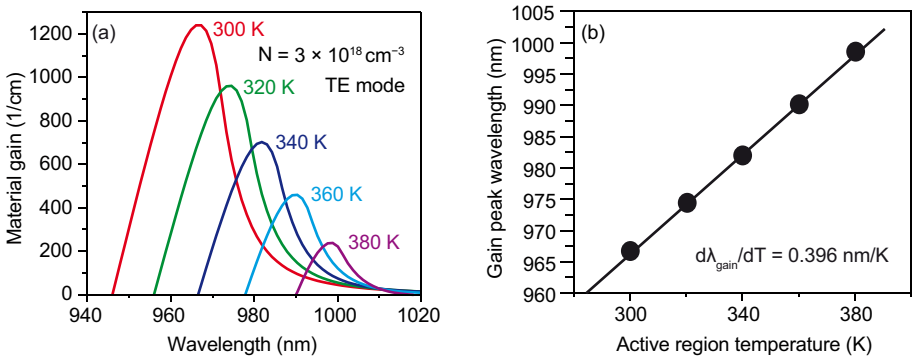

Fig. 2-15. Calculated material gain spectra (a) at different temperatures for a fixed injected carrier density of 3×10^{18} cm^{-3}, and peak gain wavelength (b) versus temperature for a single $In_{0.21}Ga_{0.79}As$ QW (4.2 nm-thick) surrounded by $GaAs_{0.88}P_{0.12}$ barrier layers.

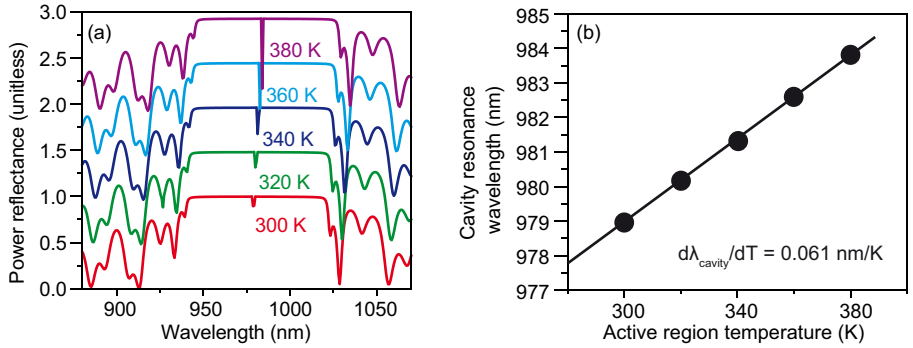

Fig. 2-16. Calculated power reflectance at normal incidence for the full 980 nm VCSEL epitaxial structure at different temperatures (a) and the resultant cavity longitudinal resonance (etalon dip) wavelength (b) versus the active region temperature.

from 300 to 380 K. The QW gain peak wavelengths change with active region temperature as shown in Fig. 2-15(b), with a calculated gain shift rate of 0.396 nm/K. Fig. 2-16(a) shows the calculated power reflectance of a 980 nm VCSEL as a function of increasing temperature. The corresponding extracted cavity resonance wavelength shift with temperature is depicted in Fig. 2-16(b), with the shift rate of 0.061 nm/K.

The cavity resonance wavelength shifts to longer wavelengths as the temperature increases, as does the QW peak gain, but at a smaller rate of 0.061 nm/K compared to 0.396 nm/K for the QW gain peak. Given these rates of wavelength-shift versus temperature one can choose a gain-to-etalon wavelength offset at room temperature so the offset is equal to zero at a certain elevated temperature to facilitate highly temperature stable or possibly temperature insensitive operation within a limited operating range. The peak QW gain wavelength change of the $In_{0.21}Ga_{0.79}As/GaAs_{0.88}P_{0.12}$ QW system and the 1D fundamental longitudinal etalon resonance wavelength change for three different VCSEL cavities with a gain-to-etalon wavelength offset at 300 K of 0, –15, and –25 nm is shown in Fig. 2-17. The intersection between the

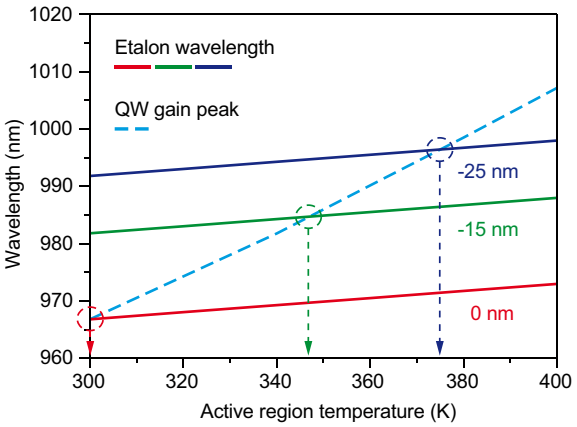

Fig. 2-17. Stimulated peak gain wavelength of a single $In_{0.21}Ga_{0.79}As/GaAs_{0.88}P_{0.12}$ QW/barrier active region and the etalon resonance wavelength of 980 nm VCSELs versus temperature for gain-to-etalon wavelength offsets fixed at 300 K at 0, –15, and –25 nm relative to the peak QW gain.

QW gain peak and the cavity resonance occurs at a specific temperature, which is 300, 347, and 376 K for 0, –15 and –25 nm offset, respectively. This temperature corresponds to the threshold, i.e. the best static working point for efficient operation.

2.4.2 The Effect on High Bit-Rate Modulation Properties

The QW gain-to-etalon wavelength offset not only has an important influence on the static performance, but also a large impact on the high-speed modulation properties [99], as the change of the differential QW gain upon a temperature increase is noticeably reduced. This effect can be predicted based on temperature dependent calculations of the differential gain. The differential gain versus wavelength at the threshold-gain-point for different temperatures is calculated by: 1) determining the threshold gain of the VCSELs at a given temperature accounting for mirror losses and absorption; 2) using the same approach as in Fig. 2-15(a) to determine the parameters for the specific required QW gain; and 3) calculating the differential gain at this threshold-gain-point. The threshold gain is calculated to be here 472 cm^{-1} at 300 K. As expected, the calculations show that the differential gain peak moves to longer wavelengths with elevated temperatures and at the same time, the maximum gain decreases slowly, as shown in Fig. 2-18(a). An active region with high differential gain is desired for high bit-rate VCSELs. A higher differential gain leads to a larger *D*-factor and thus a faster increase of relaxation resonance frequency with current. This enables the VCSEL to reach a larger modulation bandwidth before it is limited by damping or thermal effects [69]. In order to illustrate the importance of the change in differential gain with temperature to the temperature stability of the devices, the results for gain-to-etalon wavelength offsets of 0, –15, and –25 nm are depicted in Fig. 2-18(b). For this calculation, the 1D cavity etalon resonance wavelength values from Fig. 2-16 were used. The highest differential gain is obtained when the

gain-to-etalon wavelength offsets is 0 nm and the active region temperature is 300 K, and the differential gain decreases rapidly with increasing temperature. The active region temperature T_{active} increases fast with increasing operating bias current, and can be estimated for the linear LI region using $T_{active} = T_{ambient} + R_{th} \cdot (I \cdot V - P_{out})$ [100], where R_{th} is the thermal resistance, I and V are bias current and voltage, and P_{out} is the optical output power. By taking the ~4.0 μm oxide-aperture diameter 980 nm VCSEL measured in Chapter 6 as an example, using an ambient temperature of 25 °C, a bias current and voltage of 5.4 mA and 2.59 V, respectively, an optical output power of 1.78 mW, and a measured thermal resistance of 4.68 K/mW, the active region temperature is estimated to be 82.1 °C (355.25 K), which is 57.1 °C higher than the ambient temperature. The temperature of the active region is always higher than the ambient temperature, thus a large differential gain at elevated temperatures is clearly important for a temperature robust VCSEL. The –15 nm gain-to-etalon wavelength offset design has a smoother change of the differential gain across the temperature range of 25 − 85 °C compared to offsets of 0 nm and –25 nm. The –15 nm offset also results in higher differential gain at temperatures above ~350 K as compared to a VCSEL with a 0 nm gain-to-etalon wavelength offset. This is clearly beneficial for operation at high bit-rate at high temperatures for temperature stability. Also, this larger differential gain results in a larger D-factor, which is an important factor for VCSELs to reach a certain bandwidth at a low bias current, to enable a low operating energy consumption. A larger offset, for example –25 nm, results in a lower differential gain at 300 – 340 K. In addition, the differential gain at from ~360 – 385 K is less than what is possible with a –15 nm offset.

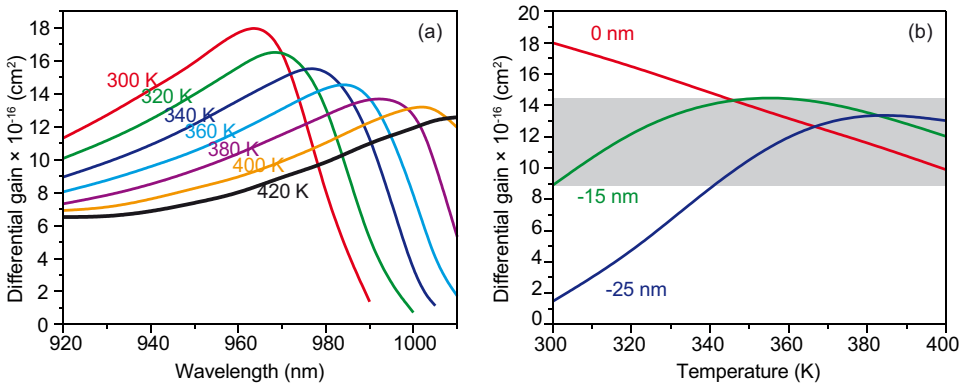

Fig. 2-18. Calculated differential gain spectra for our QW active region designed for a room temperature gain peak of 965 nm. The curves are shown for active-region temperatures ranging from 300 to 420 K (a), and differential gain versus temperature for 300 K gain-to-etalon wavelength offsets of 0, –15, and –25 nm.

2.4.3 Summary

The temperature dependence of the QW differential gain for several 980 nm active region designs are numerically investigated. The influence (both on static performance and on high bit-rate modulation performance) of QW gain-to-cavity etalon wavelength offset for 980 nm VCSEL is theoretical analyzed. By introducing a −15 nm QW gain-to-cavity etalon wavelength offset, the temperature-stability, the maximum bit rate at high temperature (~85 °C), and the energy efficiency of VCSELs can be simultaneously improved. VCSELs designs with –15 nm gain-to-etalon wavelength offset are shown to be well suited for temperature-stable static and high-speed modulation operation.

2.5 Thermal Design

The temperature sensitivity of VCSELs is related to their structure and thermal conductivity of the constituent materials. The use of high thermal conductivity materials for DBR mirrors is helpful to achieve high thermal performance VCSELs. Therefore, the optimization of the parameters that influence the thermal performance is of great importance in designing high temperature performance VCSELs.

2.5.1 Theoretical Background

Heat transport in semiconductor lasers can be simulated by numerically solving the heat conduction equation using the finite-element method (FEM). The mathematical equation for heat transfer by conduction is the heat equation:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot \left(-k \nabla T\right) = Q \tag{2.20}$$

where T (K) is the temperature, Q (W/m^3) is a heat source, ρ (kg/m^3) is the material density, C_p (J/kg·K) is the heat capacity and k (W/m·K) is the thermal conductivity of the medium. If the thermal conductivity is isotropic, the equation (2.20) becomes:

$$\rho C_p \frac{\partial T}{\partial t} - k \nabla^2 T = Q \tag{2.21}$$

Owing to the very large-scale difference in the vertical and radial directions, the effective thermal conductivity of active region layers and DBR layers is different in the two directions. For active region layers, the equivalent thermal conductivity of the multilayer in the lateral (k_L) and the vertical (k_v) directions are determined from the following two expressions [101]:

$$k_L = \frac{\sum_{n=1}^{N} d_n k_n}{\sum_{n=1}^{N} d_n}, \; k_v = \frac{\sum_{n=1}^{N} d_n}{\sum_{n=1}^{N} d_n / \kappa_n} \tag{2.22}$$

where d_n and k_n represent the thickness and the thermal conductivity of the n_{th} layer, N is the number of layers. The effective thermal conductivity for a DBR can be expressed as [102]:

$$k_L = \frac{d_1 k_1 + d_2 k_2}{d_1 + d_2}, \; k_v = \frac{d_1 + d_2}{d_1 / k_1 + d_2 / k_2} \tag{2.23}$$

Table 2-3. Material parameters at 300K [102, 105, 106]

Material	[1]C_p	[2]ρ	[3]k	[4]Thickness
GaAs (P-contact layer)	327	5.32	44	20
$Al_{0.12}GaAs$/ $Al_{0.9}GaAs$ (Top DBR)	378.2	4.48	k_L = 22.27 k_v = 21.07	71/81.5 (22.5 pairs)
Al_xO_y	850	3.96	0.7	30
$Al_{0.98}Ga_{0.02}As$ (Selective oxidation)	448	3.79	58.43	30
$Al_{0.9}GaAs$/ $Al_{0.12}Ga_{0.88}As$ (Top DBR)	378.2	4.48	k_L = 22.27 k_v = 21.54	52.3/71
Al_xO_y	850	3.96	0.7	30
$Al_{0.98}Ga_{0.02}As$ (Selective oxidation)	448	3.79	58.43	30
$Al_{0.9}GaAs$/ $Al_{0.625}GaAs$/ $Al_{0.35}Ga_{0.65}As$ (Cladding layer)	400.25	4.08	k_L = 19.7 k_v = 17.237	75.5/70/20
$In_{0.21}Ga_{0.79}As$/ $GaAs_{0.88}P_{0.12}$ (QWs)	328.12	5.26	k_L = 14.44 k_v = 10.78	6/(4.2/6) (5 QWs)
$Al_{0.35}Ga_{0.65}As$/ $Al_{0.625}GaAs$/ $Al_{0.9}GaAs$ (Cladding layers)	400.25	4.08	k_L = 19.7 k_v = 17.237	20/70/104.6
$Al_{0.12}GaAs$/ $Al_{0.9}GaAs$ (Bottom DBR)	378.2	4.48	k_L = 22.27 k_v = 21.54	71/81.5 (37.5 pairs)
GaAs/AlAs (Bottom DBR)	382.9	4.44	k_L = 63.27 k_v = 58.66	69.2/83.1 (37.5 pairs)
GaAs (Subtract)	327	5.32	44	2000

[1]C_p is in unit of J/kg·K; [2]ρ is in unit of 10^3 kg/m^3; [3]k is in unit of W/m·K; [4]thickness is in unit of nm.

2.5.2 Thermal Simulation

The thermal behavior of semiconductor lasers is very complex, since many parameters are functions of temperature. To simplify the calculation the variations of the threshold current, differential quantum efficiency, thermal conductivities, and resistivity with temperature is neglected in the following simulations. Since VCSELs are symmetric with respect to the z-axis in the cylindrical coordinate system with three curvilinear coordinates (r, φ, z), a two-dimensional FEM simulation in the r and z directions for an arbitrary azimuth angle φ are used to simplify the problem. The cross section of our simulated VCSEL is shown in Fig. 2-19. As shown in equation (2.21), three parameters are important, which are density ρ (kg/m^3), heat capacity C_p (J/kg·K), and thermal conductivity k (W/m·K). These three parameters need to be defined for each material for the heat transfer simulation. Table 2-3 lists the parameter values used in following simulations.

The heat sources in VCSELs are more complicated than those in edge-emitting lasers, where the non-radiative recombination of charge carriers in the active region is the dominating heat source. Important heat sources of VCSELs are non-radiative recombination and reabsorption of spontaneous emission in the active region and Joule heating. The heat flux distribution in the device is related to the voltage drop across the active region and DBRs [103]. The voltage drop across the active region is 1.2653 V for 980 nm VCSEL (calculated through the average bandgap energy). The voltage drop across the DBRs is caused by interface barriers, which increase the

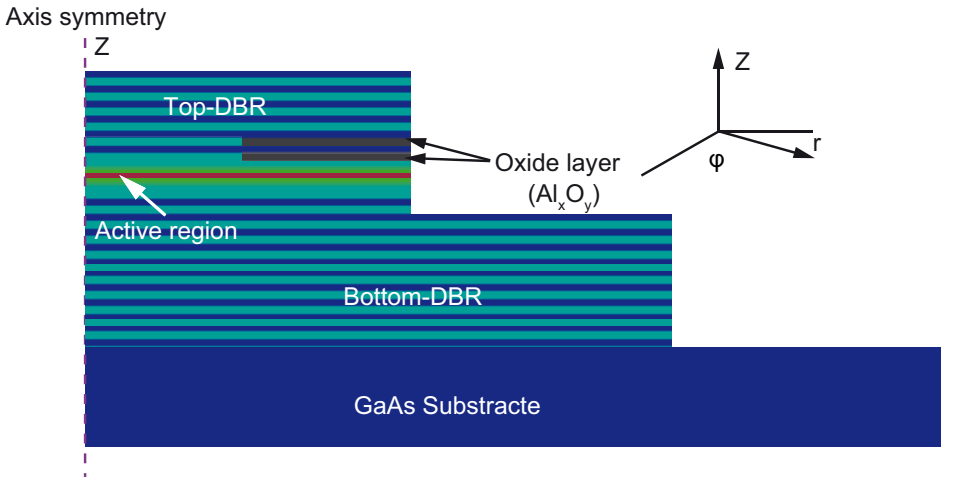

Fig. 2-19. Two-dimensional GaAs-based top emitting 980 nm VCSEL structure employing a rotational structural symmetry along the z-axis used in the simulation.

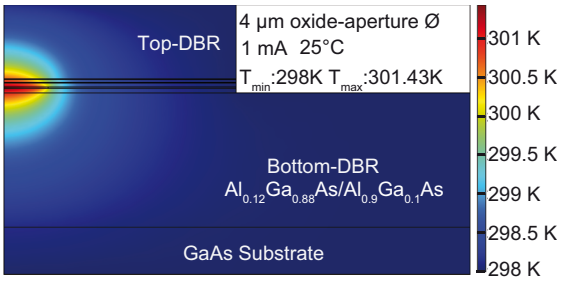

Fig. 2-20. Simulated temperature distributions $T(r,z)$ in a 4 µm oxide-aperture diameter 980 nm VCSEL at CW current of 1 mA with T_{min} = 298 K (dark blue) and T_{max} = 301.37 K (dark red).

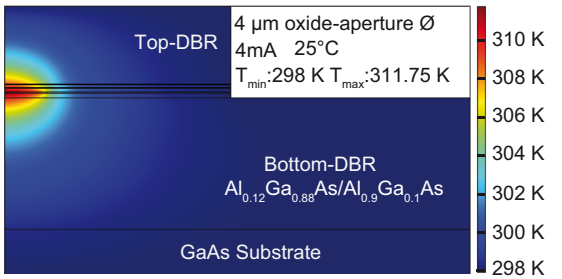

Fig. 2-21. Simulated temperature distributions $T(r,z)$ in a 4 µm oxide-aperture diameter 980 nm VCSEL at CW current of 4 mA with T_{min} = 298 K (dark blue) and T_{max} = 311.75 K (dark red).

resistance and threshold voltage [104]. The heat transfer problem is solved by defining an initial value of constant temperature T_0 for all domains and as the temperature boundary condition for keeping all outer sides of the device at T_0 at any time.

2.5.2.1 Active region temperature vs. current

Contour plots of the temperature distribution in a cross sectional plane (r-z plane) of the 4 µm oxide-aperture diameter 980 nm VCSEL are given in Fig. 2-20. The continuous wave (CW) injection current is 1 mA, the voltage is 1.93 V, and the output power is 0.29 mW. So the total heat flux in the VCSEL is 1.64 mW. Based on the voltage drop across the active region and DBRs, the active region heat source is calculated to be 1.5×10^{15} W/m^3. So 1 mA CW injection current leads to a temperature rise of 3.437 K in the active region. The contour plots of the temperature distribution at higher injection current of 4 mA is shown in Fig. 2-21, which leads to a higher temperature rise of 13.75 K in the active region.

2.5.2.2 Thermal resistance vs. oxide-aperture diameter

From this thermal simulation, the thermal resistance R_{th} (K/mW) of the device can easily be obtained by using $R_{th} = \Delta T / \Delta P_{diss}$. The same heat flux of 4 mW across the active region for different oxide-aperture diameter VCSELs is applied to study the influence of oxide-aperture diameter on the thermal performance, which corresponds to active region heat sources of 2.23×10^{16}, 9.95×10^{15}, 5.59×10^{15}, 3.5×10^{15}, 2.48×10^{15}, and 1.82×10^{15} W/m^3 for VCSELs with oxide-aperture diameter of 2, 3, 4, 5, 6, and 7 µm, respectively. The contour plots of the temperature distribution for

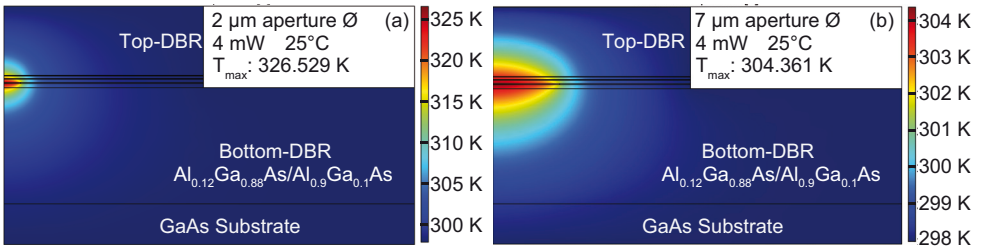

Fig. 2-22. Simulated temperature distributions T(r,z) at the heat flux of 4 mW across the active region for 2 μm (a) and 7 μm (b) oxide-aperture diameter 980 nm VCSELs with T_{min} = 298 K and T_{max} = 326.529 K for the 2 μm oxide-aperture diameter VCSEL (a), and T_{max} = 304.361 K for the 7 μm oxide-aperture diameter VCSEL (b).

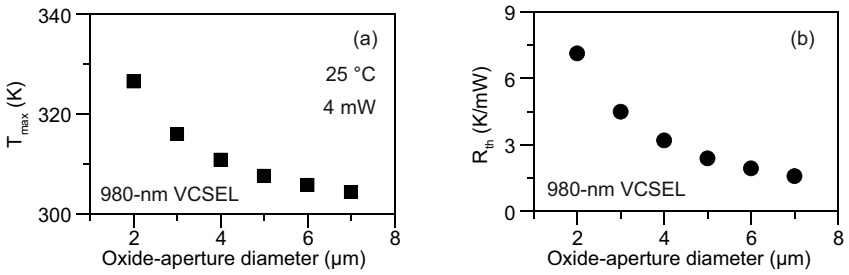

Fig. 2-23. Simulated maximum active region temperature (a) at the same heat flux of 4 mW across the active region, and the thermal resistance (b) for VCSELs with oxide-aperture diameter of 2, 3, 4, 5, 6, and 7 μm, respectively.

2 and 7 μm oxide-aperture diameter 980 nm VCSELs are shown in Fig. 2-22, with the maximum active region temperature of 326.529 and 304.361 K, respectively. This translates into a thermal resistance of 7.13 and 1.59 K/mW, respectively.

The same thermal simulations are performed for VCSELs with oxide-aperture diameter of 3, 4, 5, 6 μm by applying the same heat flux of 4 mW across the active region. The maximum active region temperatures are 315.985, 310.81, 307.566, and 305.771 K for 3, 4, 5, and 6 μm oxide-aperture diameter VCSELs, respectively, as shown in Fig. 2-23(a). The thermal resistance is calculated to be 4.49, 3.2, 2.39, and 1.94 K/mW for 3, 4, 5, 6 μm oxide-aperture diameter VCSELs, respectively, as show in Fig. 2-23(b). As expected, small oxide-aperture VCSELs have higher active region temperature under a given heat flux due to the smaller volume of the heat source. This higher active region temperature increase for a given heat flux leads to a higher thermal resistance for the small oxide-aperture VCSELs.

2.5.2.3 Active region temperature vs. bottom-DBR material

Ternary alloys have lower thermal conductivity compared with binary material, due to the strong scattering of phonons caused by the random distribution of alloy atoms. To study how much improvement of the thermal performance of VCSELs is possible when a binary GaAs/AlAs bottom DBR is used compared to a $Al_{0.12}Ga_{0.88}As$/

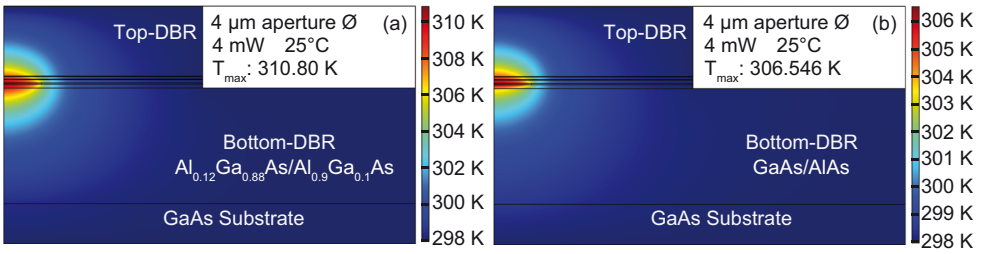

Fig. 2-24. Simulated temperature distributions at the heat flux of 4 mW across the active region for 4 μm oxide-aperture diameter VCSELs with T_{max} = 310.80 K with $Al_{0.12}Ga_{0.88}As/Al_{0.9}Ga_{0.1}As$ bottom DBR (a), and T_{max} = 306.546 K with GaAs/AlAs bottom DBR (b). The two $Al_{0.98}Ga_{0.02}As$ oxide layers are 30 nm-thick.

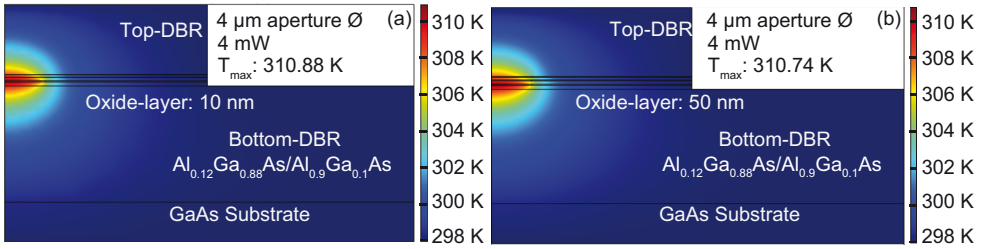

Fig. 2-25. Simulated temperature distributions at the heat flux of 4 mW across the active region for 4 μm oxide-aperture diameter VCSELs with T_{max} = 310.88 K with 10 nm-thick double oxide layers (a), and T_{max} = 310.74 K with 50 nm-thick double oxide layers (b).

$Al_{0.9}Ga_{0.1}As$ DBR, the temperature distributions for 4 μm oxide-aperture diameter 980 nm VCSELs with two different DBRs are calculate at the same heat flux of 4 mW across the active region at room temperature. The contour plots are shown in Fig. 2-24. The maximum active region temperatures are 310.80 and 306.456 K for the $Al_{0.12}GaAs/Al_{0.9}GaAs$ DBR and for the GaAs/AlAs DBR. The binary bottom DBR can reduce the active region temperature by 4.3 K when the heat flux is 4 mW, which means the thermal resistance can be reduced by 1.05 K/mW when binary GaAs/AlAs mirrors replace $Al_{0.12}Ga_{0.88}As/Al_{0.9}Ga_{0.1}As$ mirrors in 4 μm oxide-aperture diameter 980 nm VCSELs.

2.5.2.4 Active region temperature vs. oxide-layer thickness

Oxide-layer thickness can influence the static and high bit-rate modulation performance of VCSELs, because the index-step, parasitic capacitance, and electrical path vary with oxide-layer thickness. The temperature distributions for 4 μm oxide-aperture diameter 980 nm VCSELs with different oxide-layer thicknesses are calculated at the same heat flux of 4 mW across the active region at room temperature, in order to see if the oxide-layer thickness change will influence the active region temperature or not. The contour plots for 4 μm oxide-aperture diameter VCSELs with 10 nm-thick and 50 nm double oxide layers are shown in Fig. 2-25(a) and 2-25(b). The contour plots for 30 nm-thick oxide layer VCSELs is already shown in Fig. 2-24(a).

The maximum active region temperatures are 310.88, 310.80, and 310.74 K for 10, 30, 50 nm-thick oxide-layers VCSELs, respectively. The active region temperature only increases 0.14 K when the oxide layer thickness is decreased form 50 to 10 nm when the heat flux is 4 mW.

2.5.3 Summary

Thermal simulations are performed on 980 nm VCSEL structures. The temperature distribution of the active region is studied, and the thermal resistance is obtained by thermal simulation for different oxide-aperture diameter VCSELs. Also, the thermal performance improvement by the use of binary bottom DBRs is numerically demonstrated. The increase of active region temperature decreases the differential gain of the QWs. With an improved thermal performance design combined with a room temperature QW gain-to-etalon wavelength offset design, a given 980 nm VCSEL's high-speed and temperature-stable static and high-speed modulation performance can be greatly improved.

Chapter 3

Fabrication and Measurements

The fabrication of devices is as important as the wafer epitaxial design and wafer growth to achieve high performance devices. In this Chapter, the main processing techniques and measurement techniques are presented. In Section 3.1 the detailed information of the epitaxial structure used in this work is given, and the simulated mode and gain characteristics of this structure are given. Section 3.2 briefly describes the main processing techniques used for 980 nm VCSELs fabrication, and the main equipment used for these fabrication steps are briefly introduced with the process results. Next Section 3.3 presents the VCSEL characterization methods, including static and high bit-rate modulation measurements. Also the evaluation methods are briefly shown with several measurement results.

3.1 The 980 nm VCSEL Structure

The epitaxial structure designed for high-speed, temperature-stable, and energy-efficient operation at an emission wavelength of 980 nm, is grown by MOCVD on GaAs-substrates by IQE plc (Cardiff, UK), a well-known commercial epitaxy foundry. The active region contains five ~4.2 nm-thick $In_{0.21}Ga_{0.79}As$ QWs with ~6 nm-thick $GaAs_{0.88}P_{0.12}$ barrier layers. An approximately room temperature –15 nm QW gain-to-etalon wavelength offset is introduced. A QW calibration wafer is grown just before the growth of the full 980 nm VCSEL structure. The photoluminescence (PL) of this calibration wafer is measured at room temperature and the result is a 2D PL map of the wafer surface. The QW gain-to-etalon wavelength offset is determined from this PL map, and a 2D power reflectance map that is produced after the growth of the full VCSEL structure. The QWs together with the strain compensating layers are surrounded by two 20 nm-thick $Al_{0.35}Ga_{0.65}As$ barrier layers to improve carrier localization in the active region. The optical thickness of the cavity is $3\lambda/2$. In addition,

a 70 nm-thick linear grading from the $Al_{0.35}Ga_{0.65}As$ barrier to the first $Al_{0.90}Ga_{0.10}As$ low-index layers is implemented for fast carrier transport and capture times. A 24-period p-doped top distributed Bragg reflector (DBR) and a 37.5-period n-doped bottom DBR are employed. Both DBRs are composed of alternating $Al_xGa_{1-x}As$ layers with the AlAs mole fractions of x = 0.12 and x = 0.90 for the high and low refractive index layers, respectively. The $Al_xGa_{1-x}As$ regions between the low and high index layers are linearly graded over a distance of 20 nm. The doping through the DBRs is spatially varied to minimize the VCSEL's series resistance but at the same time to minimize any free-carrier absorption. In order to reduce electrical parasitics, two 30 nm-thick (as grown before selective oxidation) oxide aperture layers are formed in the first two low-index (p)DBR layers adjacent to the optical cavity by selective wet thermal oxidation of the aluminum-rich (p)$Al_{0.98}Ga_{0.02}As$ layers using a proprietary TU Berlin-designed and built oxidation furnace.

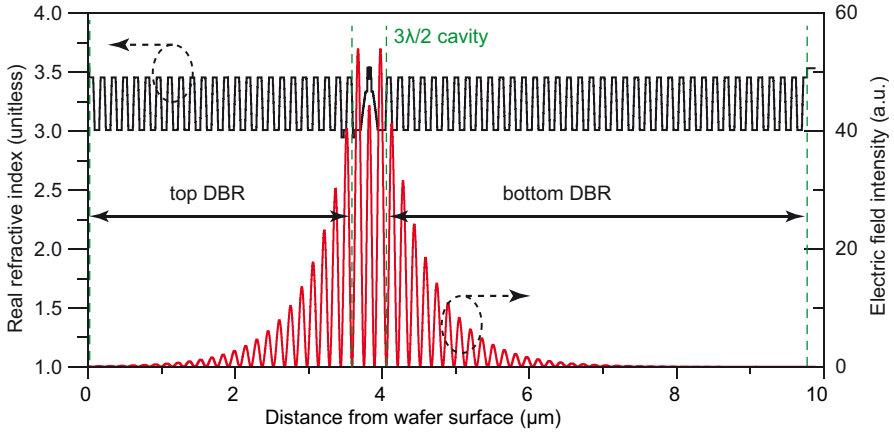

Fig. 3-1. 1D refractive index profile and electric field intensity versus distance from the top epitaxial surface of the 980 nm VCSEL epitaxial structure.

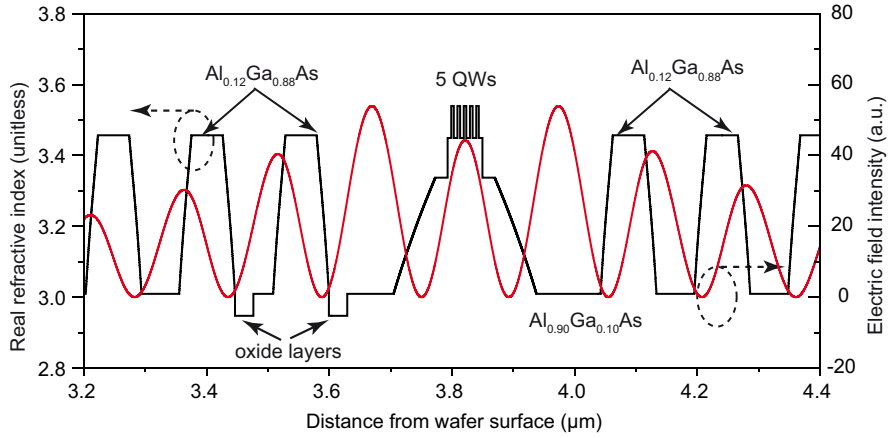

Fig. 3-2. Zoomed-in view of the refractive index profile and electric field intensity versus distance from the top epitaxial surface of the 980 nm VCSEL epitaxial structure.

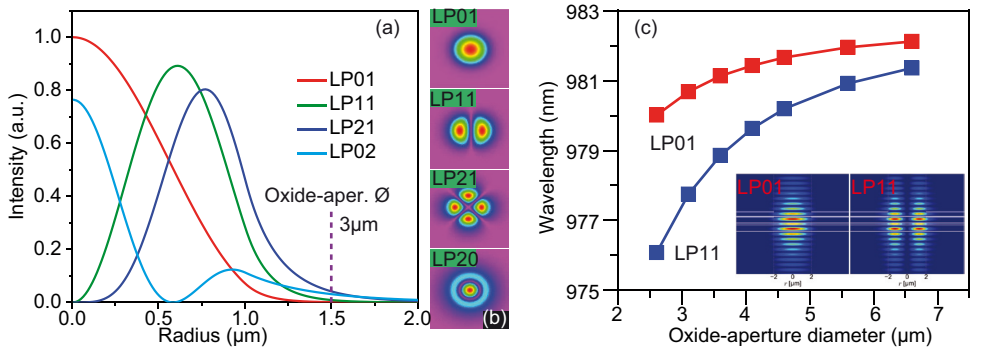

Fig. 3-3. The four lowest transverse mode profiles in the radial direction for a 3 μm oxide-aperture diameter 980 nm VCSEL (a), and intensity distributions for the four lowest LP*mn* modes of a cylindrical step-index waveguide in the transverse plane (b). Calculated cold cavity emission wavelengths of the LP01 and LP11 modes of 980 nm VCSELs as a function of oxide-aperture diameter (c), and calculated 2D plots of the optical field intensity of the LP01 mode and LP11 mode [107] for a 980 nm VCSEL with an oxide-aperture diameter of 4 μm.

3.1.1 Mode Characterization

The cavity resonant modes determine the emission wavelengths of the VCSELs. Optical field confinement in the longitudinal direction is accomplished by the highly reflective DBRs positioned below and above the active region. Due to the short cavity, a VCSEL's free-spectral range is larger than the spectral-width of the QW gain and thus only one longitudinal resonant cavity etalon mode may lase. The refractive index profile and electric-field intensity distribution of a 980 nm VCSEL epitaxial structure is shown in Fig. 3-1. A zoomed-in view is shown in Fig. 3-2.

Although in a typical VCSEL only one longitudinal resonant mode can lase, several transverse modes can be supported due to the large lateral dimensions. Transverse modes of circular-shaped VCSELs can be approximated by linearly polarized (LP*lp*) modes. The indices l and p are the azimuthal and radial transverse-mode numbers, respectively. In cylindrical coordinates, the electric field amplitude of an LP*mn* mode can be expressed as:

$$E_{mn}(r,\Phi,z) \propto e^{jm\Phi} e^{-j\beta_{mn} z} J_m(u_{mn} r), \; r < a \text{ (core)} \tag{3.1a}$$

$$E_{mn}(r,\Phi,z) \propto e^{jm\Phi} e^{-j\beta_{mn} z} K_m(v_{mn} r), \; r > a \text{ (cladding)} \tag{3.1b}$$

where r, Φ, and z are the cylindrical coordinates, β_{mn} is the propagation constant, J_m and K_m are mth order first kind and second kind Bessel function. The parameters u_{mn} and v_{mn} are given in equation (3.2), where k_0 is the propagation constant in vacuum. The propagation constants can be obtained by applying the boundary conditions as expressed in equation (3.3).

$$u_{mn}^2 = k_0^2 {n_{eff1}}^2 - \beta^2 \text{ and } \nu_{mn}^2 = \beta^2 - k_0^2 {n_{eff2}}^2 \tag{3.2}$$

$$u \cdot J_{m-1}(ua)/J_m(ua) = -v \cdot K_{m-1}(va)/K_m(va) \tag{3.3}$$

The mode intensities, which are proportional to the square of the electric field amplitudes, of the first four lowest order LPmn modes are shown in Fig. 3-3(a). The spatial intensity distributions are different for different transverse modes, which means the threshold of the higher order modes can be increased by introducing a spatially varying loss, in order to achieve single mode operation [108]. Calculated LP01 and the LP11 mode wavelength results as a function of oxide-aperture diameter [107] are shown in Fig. 3-3(c). The VCSEL resonant wavelength blue-shifts as the oxide-aperture diameter decreases [109]. For 980 nm VCSELs if the oxide-aperture diameter is ~10 μm or larger the resonant wavelength is nearly constant [107]. The wavelengths and 2D field intensities of the LP01 and LP11 modes are calculated using 2D simulation model and plotted in Fig. 3-3(c) [107].

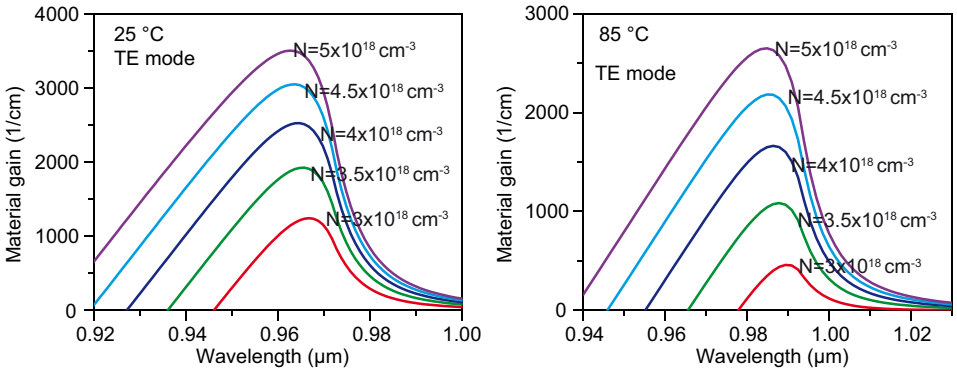

Fig. 3-4. Calculated gain spectra for $In_{0.21}Ga_{0.79}As/GaAs_{0.88}P_{0.12}$ QWs/barries used for the active region of the 980 nm VCSELs at an injected carrier density of 3×10^{18} to 5×10^{18} cm^{-3} for TE polarization at (a) 25 °C, and (b) 85 °C.

3.1.2 QW Active Region

Fig. 3-4 shows the calculated optical gain spectra of $In_{0.21}Ga_{0.79}As/GaAs_{0.88}P_{0.12}$ QWs at carrier densities of 3, 3.5, 4, 4.5, and 5 × 10^{18} cm^{-3} for TE polarization at 25 and 85 °C. The room temperature gain peak wavelength is close to 965 nm at 25 °C, as an –15 nm QW gain-to-etalon wavelength offset is introduced to improve temperature stability. This gain peak wavelength shifts to the longer wavelength of ~990 nm when the temperature is increased to 85 °C. The peak material gain decreases with increasing active region temperature.

3.1.3 Photon Lifetime Adjustment

Adjustment of the photon lifetime by changing the mirror power reflectance, thus changing the penetration depth of the optical field energy into the mirrors, is another way to increase the modulation bandwidth of VCSELs [110]. The VCSEL's photon lifetime τ_p (in s) is related to cavity loss, and can be expressed as:

$$\tau_p \approx \frac{1}{\alpha_{i(\text{rate})} + \alpha^T_{m(\text{rate})} + \alpha^B_{m(\text{rate})}} \text{ (s)} \tag{3.4}$$

where $\alpha_{i(\text{rate})}$ (s^{-1}) is the internal cavity loss rate, and $\alpha_{m(\text{rate})}$ (s^{-1}) is the top (T) or bottom (B) DBR mirror loss rate. The loss rate can be calculated using power loss per unit distance according to $\alpha_{(\text{rate})} = \langle v_g \rangle \cdot \alpha$, where $\langle v_g \rangle$ (cm s^{-1}) is the average photon group velocity in the VCSEL. The mirror loss is

$$\alpha_m = \alpha^T_m + \alpha^B_m = -\frac{1}{2L_{eff}} \ln(R_t R_b) \text{ (cm}^{-1}\text{)} \tag{3.5}$$

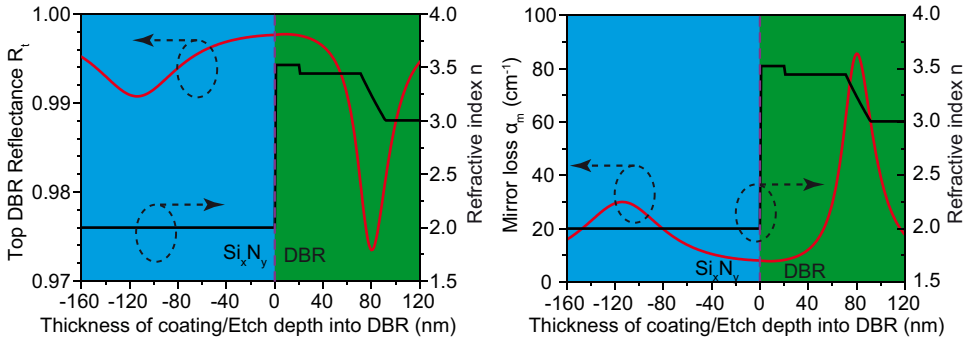

Fig. 3-5. Calculated top DBR power reflectance (a) and mirror loss (b) as function of Si_xN_y thickness and etch depth into the top DBR calculated for the 980 nm VCSEL structure. The refractive index is also shown.

where α_m, α_m^T, and α_m^B are the total mirror loss, the top-DBR mirror loss, and the bottom-DBR mirror loss. R_b is the bottom-DBR power reflectance as seen from the optical cavity looking down toward the substrate, which is 0.9998 for the DBR with 37.5 mirror pairs and with 20 nm-thick grading layers. R_t is the top-DBR power reflectance as seen from the optical cavity looking up toward air. R_t can be changed by etching away part of the top-most DBR layer or by coating the VCSEL with a thin layer, for example, Si_xN_y. The change of R_t versus the coating thickness of added Si_xN_y and versus the etch depth of the top-most GaAs layer in the top DBR are show in Fig. 3-5(a). The mirror loss change can be calculated using equation (3.5), and the results are shown in Fig. 3-5(b). The effective internal loss is calculated to be 9.1 cm^{-1} by using free carrier absorption loss coefficients, which are assumed to be 11.5 and 5 cm^{-1} at 980 nm for holes and electrons, respectively [73]. The photon lifetime can be calculated with equation (3.4), and the results are shown in Fig. 3-6. The output power can be increased by decreasing the photon lifetime at a cost of slightly increasing the threshold current. As the photon lifetime decreases the –3 dB modulation bandwidths of VCSELs are generally expected to increase [111].

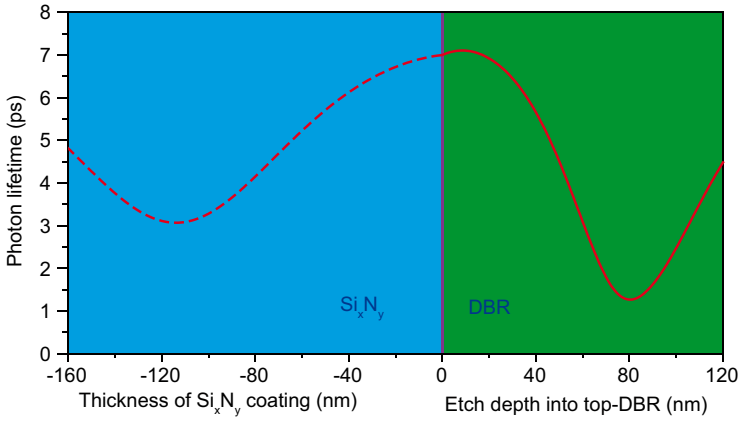

Fig. 3-6. Photon lifetime as function of Si_xN_y thickness (dashed line) and etch depth into the top DBR (solid line) calculated for the 980 nm VCSEL structure.

3.2 VCSEL Fabrication

In this section, the main processing techniques used in this work for the fabrication of 980 nm VCSELs is briefly described, including lithography, metal contact deposition, mesa etching, selective wet thermal oxidation, annealing, BCB planarization, and pad metallization. Also, the main equipment used for these fabrication steps, such as the photoresist spinner, UV contact mask aligner, e-beam deposition system,

thermal evaporation system, ICP-RIE etching machine, RIE etching machine, and the oxidation furnace are shortly introduced by showing example processing results from this work.

3.2.1 Process Techniques

3.2.1.1 Lithography

Lithography is used to transfer small feature size patterns onto the wafer. Standard UV contact photolithography can be used for feature sizes down to approximately 1 μm, and is used in this work due to its simplicity. Electron-beam lithography can be used for smaller patterns with sub-10 nm resolution [112], but takes longer time and costs more. The standard UV photolithography process starts with spinning a photoresist onto the wafer piece at a few thousand revolutions per minute (rpm) to form a thin film where the viscosity of the resist and the spin speed determine the thickness of the resulting film. The photoresist is then baked on a hotplate. Then the sample is exposed to UV radiation through a patterned mask. For positive photoresist, the exposed areas are removed using a developer solution, leaving a pattern on the sample, as shown in Fig. 3-7(b), while for negative photoresist, the unexposed resist areas are removed, as shown in Fig. 3-7(a) and 3-7(c). The mask pattern is thus transferred onto the sample. The patterned resist can then be used to protect parts of the surface during etching or metal deposition.

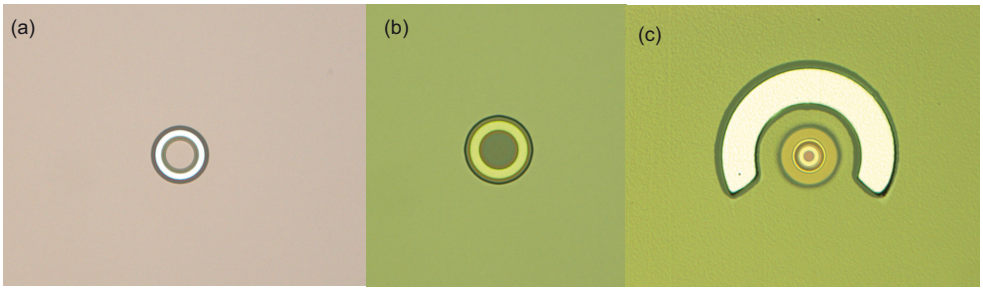

Fig. 3-7. Microscope images of a VCSEL structure at various stages of processing after the development of the photoresist (a negative photoresist) for the top p-metal contact (a); after development of the photoresist (a positive photoresist) for the mesa one etch (b); and after the development of the photoresist (a negative photoresist) for the bottom n-metal contact (c).

3.2.1.2 Metal Contact Deposition

Lift-off processes are used for metal contacts, which proceed as follows: 1) a contact pattern is defined in a spun-on photoresist using standard contact UV photolithography; 2) the metal layers are deposited over the entire patterned wafer using a series

of thermal evaporations or electron-beam evaporations; 3) the wafer is placed in a solvent (N-Methyl-2-pyrrolidinone (NMP) (Microposit Stripper 1165) [113]) where the patterned photoresist is dissolved, lifting off the metal that lies on the photoresist, but leaving the metal that lies directly on the semiconductor. What is left is a metal pattern on the surface of the wafer where no photoresist was present during the metal deposition. The Ni/Ge/Au metal layers are used for n-contacts, deposited by a Vecco thermal evaporation system. A quartz crystal monitor controls the thickness. The Ti/Pt/Au and Cr/Pt/Au metal layers are used for p-contacts and pad contacts, deposited by an electron-beam evaporation system. In an electron-beam evaporation system, an electron beam is generated by thermionic emission and accelerated and directed onto a source of metal that lies in a crucible where the kinetic energy of the electrons is converted to thermal energy, thus heating the metal and causing metal atoms to evaporate and form a thin metal film on the wafer. A noticeable advantage of electron-beam evaporation over thermal evaporation is the possibility to add a larger amount of energy into the source material. This yields a higher density film with an increased adhesion to the wafer. The deposition system utilizes a quartz

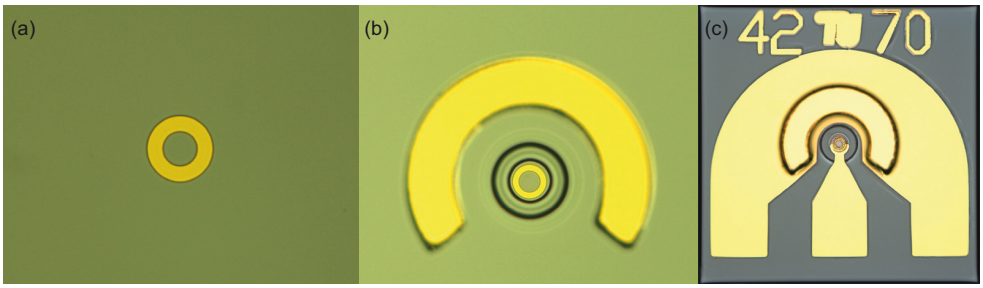

Fig. 3-8. Microscope images of a VCSEL structure after the top-metal contact lift-off step (a); after the bottom-metal contact lift-off step (b); and after the ground-signal-ground pad lift-off step (c).

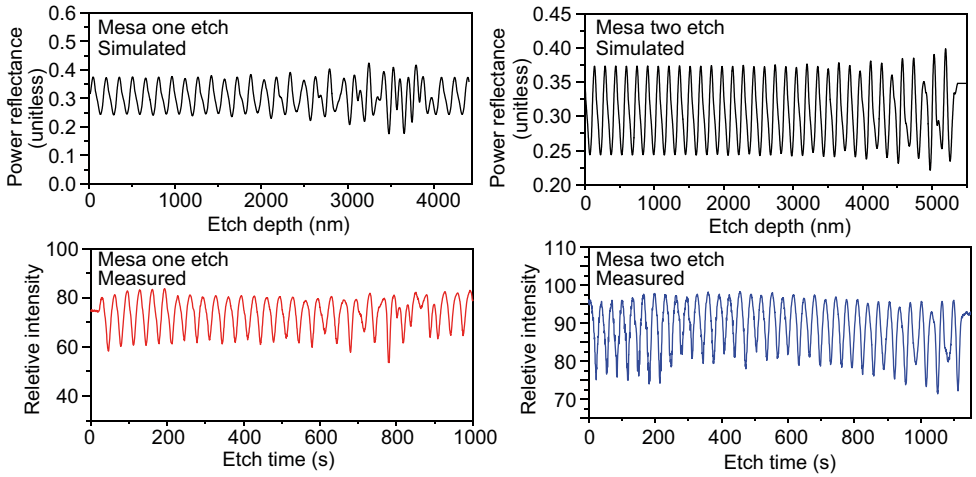

Fig. 3-9. Simulated power reflectance and measured relative intensity monitor profiles at a wavelength of 632.5 nm for the mesa one and the mesa two etching.

crystal monitor to accurately display the thickness and deposition rate of the metal deposition process. A shutter is used to block the evaporated metal from hitting the wafer until everything is ready for the deposition. Microscope images of a VCSEL structure after various metal lift-off processing steps including after lift-off of the top-metal contact, the bottom-metal contact, and the ground-signal-ground pads are shown in Fig. 3-8.

3.2.1.3 Etching

Etching is an important micro-fabrication technique to remove material using a patterned mask for protection. Two different types of etching technology can be used, wet or dry etching techniques [114]. Wet etching is inexpensive, typically causes no damage to the wafer, and may be highly selective. Dry etching techniques, using an energetic ion beam or a plasma, is currently used in semiconductor fabrication due to its unique ability over wet etching to remove material anisotropically to create high aspect ratio structures. Inductively coupled plasma reactive ion etching (ICP-RIE) is a more advanced reactive ion etching technique that uses two independent RF sources. One RF source is coupled inductively to a low-pressure gas mixture creating a high-density plasma, and another RF source is applied to a lower electrode to produce a substrate bias to extract and accelerate the reactive species from the plasma to the sample being etched. Separate RF generators for the plasma and the

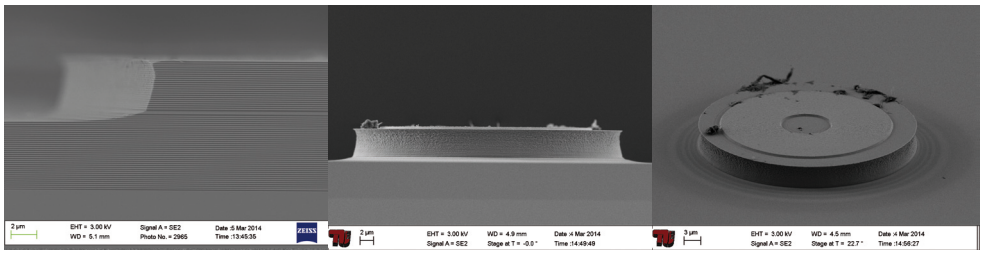

Fig. 3-10. SEM images of a 980 nm VCSEL wafer after the mesa one etch.

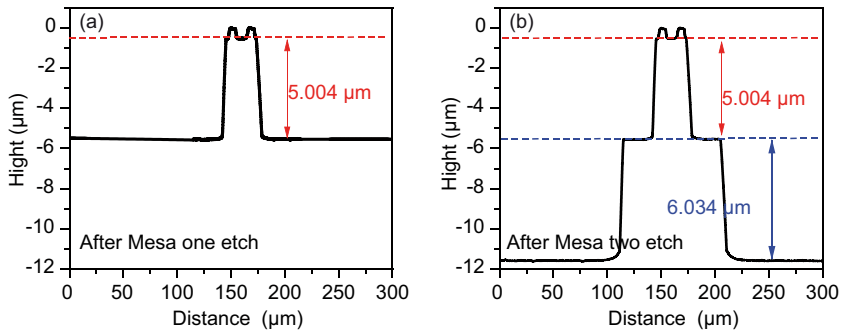

Fig. 3-11. Profile measurement results of a 980 nm VCSEL after the first mesa etch and after the second mesa etch.

lower electrode allow independent control of ion density and energy. To monitor the etch depth in situ, a 632.5 nm He-Ne laser is directed onto the wafer and the reflected power is recorded, all during the etching process. The simulated and measured etch monitor profiles for a mesa one etch and a mesa two etch for 980 nm VCSELs are shown in Fig. 3-9. As the DBRs are multi-layer structures, the signal monitored by the laser interferometer has periodic reflected intensity oscillations as a function of etch depth. The etch depth at a given instant during the etching process can be determined by the reflected oscillatory profile, so a precise control of the etching depth can be achieved. Scanning electron microscope (SEM) images of VCSELs after a mesa one etch are shown in Fig. 3-10. The profilometer measurement results after a mesa one etch and a mesa two etch are shown in Fig. 3-11. These measurements indicate that the heights of the first mesa and the second mesa are 5 and 6 µm, respectively.

3.2.1.4 Selective Wet Oxidation

The oxide apertures for current and transverse optical mode confinement are defined by the selective wet oxidation of two aluminum-rich $Al_{0.98}Ga_{0.02}As$ layers with our home-built oxidation furnace, where the sample is exposed to a purified water steam atmosphere at a temperature of 420 °C. The schematic diagram of our oxidation furnace is shown in Fig. 3-12. Inert nitrogen is used as a carrier gas to transport water steam into the furnace. The furnace heater is kept at a constant temperature and the flow of nitrogen and water steam as well as the chamber pressure are regulated to achieve a stable and reproducible process. The oxidation rate of $Al_xGa_{1-x}As$ is very sensitive to the aluminum composition. Precise control of the stop time for a desired oxide-aperture diameter is very important. The oxidation rate is first determined by running a calibration test using the same VCSEL epitaxial structure. The SEM image of the side view of a cleaved 980 nm VCSEL wafer is shown in Fig. 3-13(a), where two oxide apertures can be clearly seen as partially darkened layers. The

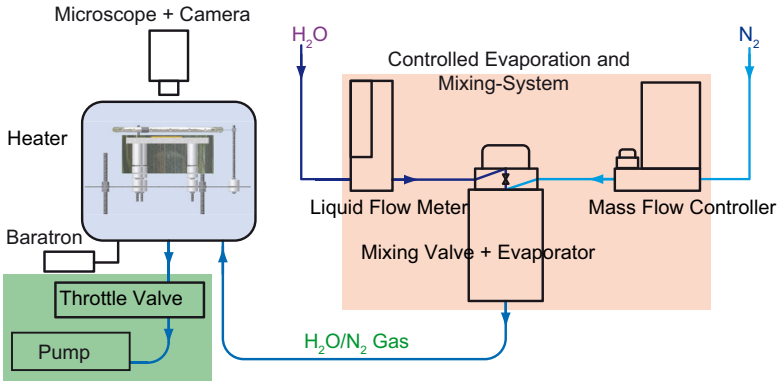

Fig. 3-12. Schematic diagram of the oxidation furnace.

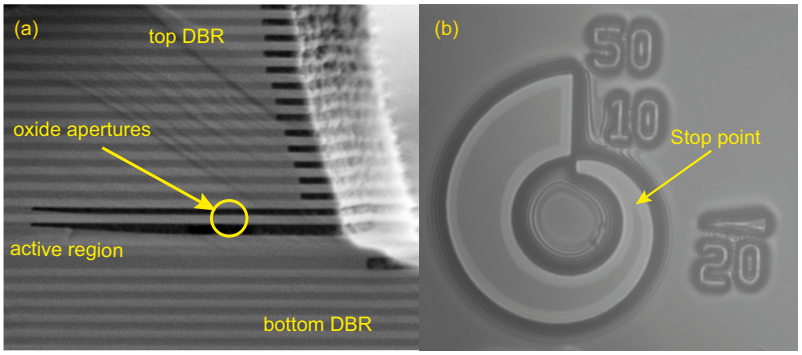

Fig. 3-13. A SEM image of the side view of a cleaved 980 nm VCSEL wafer test oxidation piece after oxidation (a) and a microscope image of one of the structures used to monitor the oxidation depth (b).

oxidation rate can be determined by measuring the depth of these oxide layers for the given oxidation time. The approximate oxidation time needed for the desired oxide-aperture diameters on the subsequent VCSEL wafer piece to be fully processed can be calculated using the oxidation rate. During the wet oxidation procedure, an in-situ monitoring system, consisting of a silicon CCD camera and a microscope with an appropriate illumination wavelength of 850 nm to produce a high contrast between oxidized and unoxidized $Al_xGa_{1-x}As$ material is used to control the size of the oxide apertures. Fig. 3-13(b) shows one of the structures that are used to monitor the oxidation depth, illustrating the contrast difference between oxidized and unoxidized AlGaAs attainable with the monitoring system.

3.2.1.5 RTA Annealing

Low resistance ohmic contacts are required for low threshold, high-speed VCSELs. The ohmic contact is the contact of a metal and a semiconductor, which neither the metal or the semiconductor generate significant additional resistance or significantly change the equilibrium carrier concentration in the semiconductor. Ohmic contacts have a significant impact on the resistance of the VCSELs, and further affect the usable operating lifetime and reliability of the devices. Low resistance ohmic contacts can help to reduce the threshold current, improve the efficiency, and prolong the lifetime of the VCSELs. A SSI Solaris 150 Rapid Thermal Processing System [115] is used for the metal contact annealing. Using the optimized rapid thermal anneal (RTA) conditions in N_2 with an annealing temperature of 380 °C and an annealing time duration of 60 s, good ohmic contacts are obtained for the processed VCSELs. Fig. 3-14 (a) shows the voltage-current (VI) characteristics of one VCSEL before and after the RTA annealing step, which shows a clear improvement, as the resistance decreases after the annealing step.

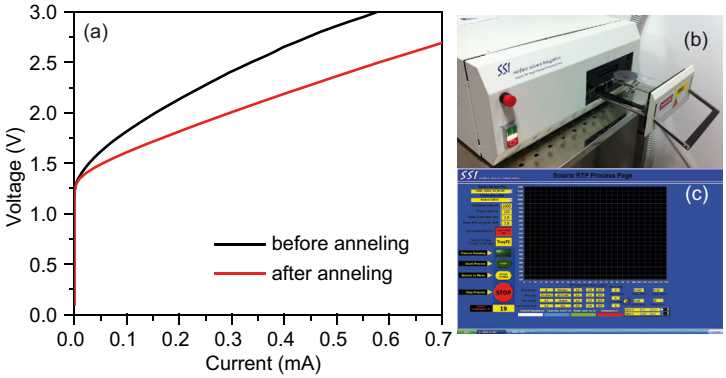

Fig. 3-14. The voltage-current (VI) characteristics (a) before and after annealing for a 980 nm VCSEL, and the layout (b) of the SSI Solaris 150 Rapid Thermal Processing System, also the screen (c) showing the run process menu [117].

3.2.2 High-Speed VCSEL Processing

The processing is started by cleaving the as-grown 3-inch diameter wafer into four equal pieces and using one-quarter wafer for the following steps (Fig. 3-15(a)). Top p-contact metal (Ti/Pt/Au) rings are deposited by e-beam evaporation (Fig. 3-15(b)). The first circular mesas with diameters from 18 to 31 μm are defined by photolithography and etched using ICP-RIE with Cl_2/BCl_3, and the etch depth is monitored by an in-situ laser interferometer (Fig. 3-15(c)). Different oxide-aperture diameters are obtained after the selective wet thermal oxidation due to the different mesa diameters. The oxide depth is monitored using the in-situ microscope and an 850 nm illumination source (Fig. 3-15(d)). Next the second mesa etch is performed. The mesa two etch proceeds into the bottom (n+)GaAs contact layer after oxidation using the same recipe as for the first mesa etch (Fig. 3-15(e)). Double mesas are used to improve heat dissipation. The bottom Ni/Ge/Au n-contacts with the shape of a three-quarter ring are deposited by thermal evaporation and annealed for 60 s at 380 °C in an N_2 atmosphere (Fig. 3-15(f)). Thick dry-etched bisbenzo-cyclobutene (BCB) is used for producing a relatively flat dielectric layer to reduce the parasitic capacitance and provide a clean surface for the radio frequency (RF) coplanar contact pads. The BCB is photosensitive enabling the opening of the BCB that covers the n-contact and first mesa by using UV photolithography. Since the UV photolithography typically does not fully open and remove all of the thick BCB, RIE etching was used to remove the remaining BCB above the first mesa and above the bottom metal contact with CF_4/O_2 (Fig. 3-15(g)). The coplanar ohmic Cr/Pt/Au contact pads for on-wafer radio frequency probing are evaporated by electron-beam deposition to achieve a good step coverage into the n-contact trench in the shape of a high-speed ground-signal-ground

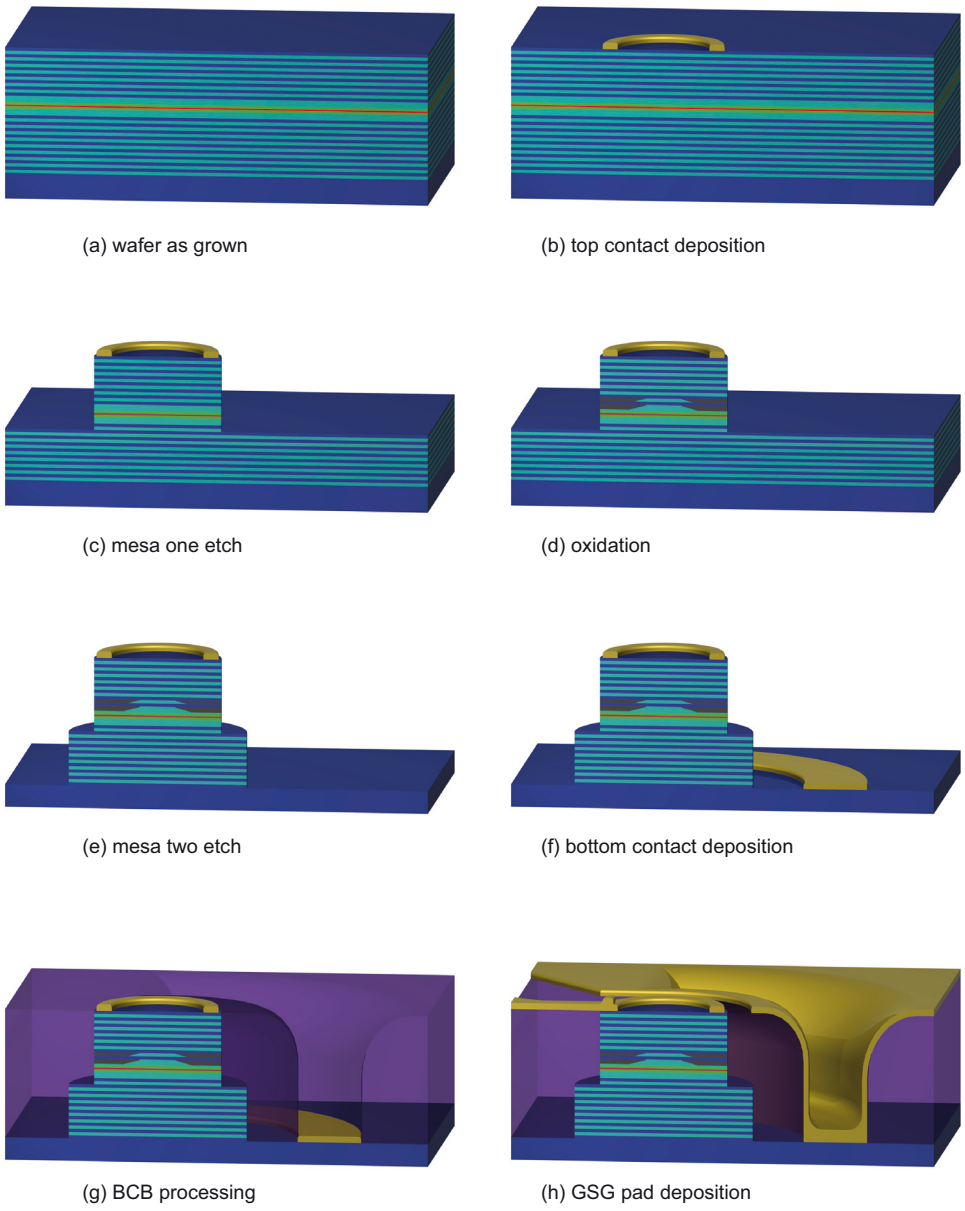

Fig. 3-15. The 980 nm VCSEL processing scheme showing the primary individual steps: (a) the wafer as grown; (b) top contact deposition; (c) mesa one etch; (d) wet oxidation; (e) mesa two etch; (f) bottom contact deposition and annealing; (g) BCB processing; and (h) GSG contact pad deposition.

(GSG) configuration, Fig. 3-15(h). The device pitch and contact sizes are designed to facilitate fast automatic continuous wave on-wafer characterization. Additional processing details may be found in Appendix A.

3.3 VCSEL Measurements

A detailed analysis of the static and high frequency characteristics are performed for the 980 nm VCSELs, including measurements of the static light output power-current-voltage (LIV), emission spectra, small-signal frequency response, and high bit rate data transmission measurements. This section present how these measurements are performed and the evaluation methods, and several results are given as examples. A more detailed analysis can be found in Chapters 6 and 7.

3.3.1 LIV Measurements

Static characteristics give the basic information of a VCSEL's performance. The static LIV characteristics are measured and evaluated using our home-built automated wafer mapping system. For LIV measurements, VCSELs are driven by the digital source meter Keithley 2400-LV [117] and the output light is collected by a calibrated integrating sphere. The photocurrent from the integrating sphere is measured by a second digital source meter. A LabVIEW program controls both source meters. The temperature is controlled by a vacuum thermochuck Temptronic TP03010 [118]. Fig. 3-16(a) shows one example set of LIV measurement results for a ~7.0 μm oxide-aperture diameter 980 nm VCSEL as a function of the heat-sink temperature from 25 to 95 °C. The range of currents is chosen to be larger than the rollover current. Several important parameters can be extracted from the LIV curves, including threshold current I_{th}, threshold electrical power P_{th}, rollover current $I_{rollover}$, maximum output power P_{max}, maximum differential quantum efficiency DQE_{max}, and maximum wallplug efficiency WPE_{max}, as shown in Fig. 3-16(b) − (g).

3.3.2 Spectral Measurements

To measure the emission spectra, the VCSELs are driven by the digital source meter (Keithley 2400-LV) and the output light is coupled into a multimode fiber with a 62.5 μm core diameter connected to an optical spectrum analyzer HP 70951B. The

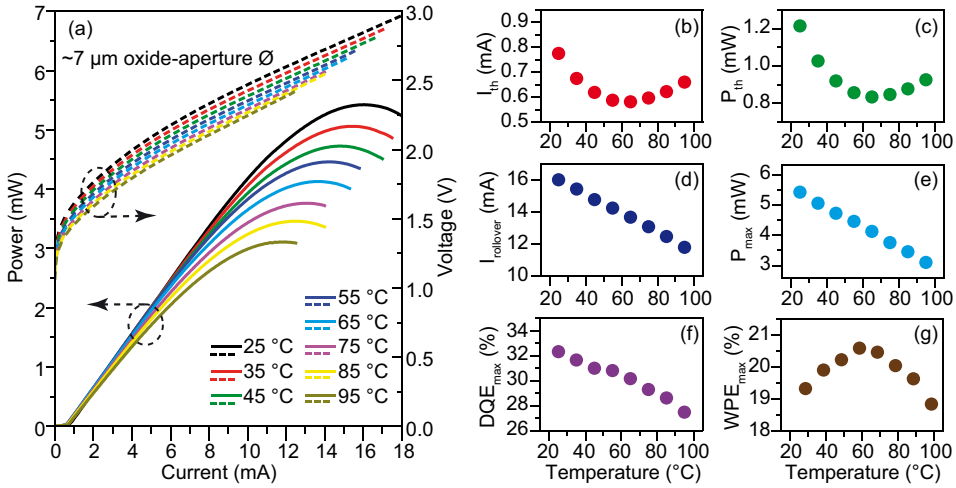

Fig. 3-16. Static L-I-V characteristics (a) at 25 to 95 °C for a ~7 μm oxide-aperture diameter 980 nm VCSEL, and the basic parameters versus temperature including: (b) threshold current I_{th}; (c) threshold electrical power P_{th}; (d) rollover current $I_{rollover}$; (e) maximum output power P_{max}; (f) maximum differential quantum efficiency DQE_{max}; and (g) maximum wallplug efficiency WPE_{max}.

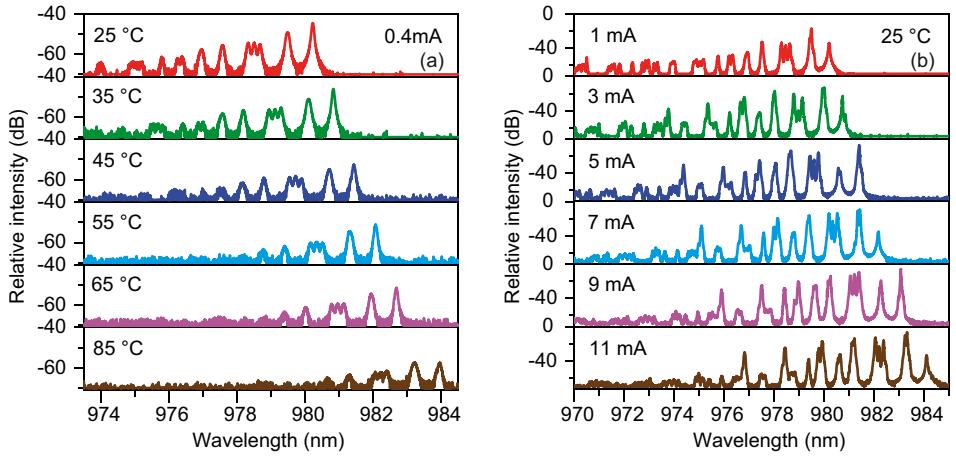

Fig. 3-17. Measured emission spectra at different heat-sink temperatures (a) at 0.4 mA and at different bias current (b) at 25 °C for a ~7 μm oxide-aperture diameter 980 nm VCSEL.

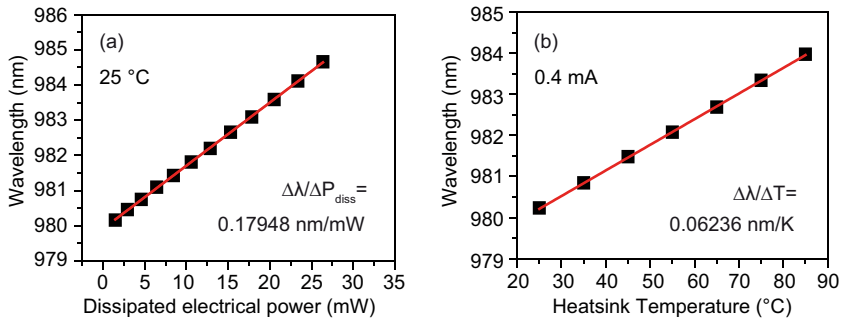

Fig. 3-18. Measured emission wavelength (fundamental LP01 mode) as a function of dissipated electrical power (a) and measured peak emission wavelength (fundamental LP01 mode) as a function of heat-sink temperature (b) for the ~7 μm oxide-aperture diameter 980 nm VCSEL.

temperature is controlled by the vacuum thermochuck (Temptronic TP03010B). Fig. 3-17(a) shows the measured continuous wave (CW) emission spectra for a ~7 µm oxide-aperture diameter VCSEL at a fixed forward bias current of 0.4 mA as a function of heat-sink temperature from 25 to 85 °C. The measured CW emission spectra from the same VCSEL at 25 °C as a function bias current from 1 to 11 mA are shown in Fig. 3-17(b). The cavity etalon resonance wavelength shift rate versus the dissipated power $\Delta\lambda/\Delta P_{diss}$ ($P_{diss} = I \cdot V - P_{opt}$ is the dissipated power, P_{opt} is the optical output power) and versus the heat-sink temperature $\Delta\lambda/\Delta T$ can be obtained from the spectral results, which are 0.17948 nm/mW and 0.06236 nm/K, respectively, as shown in Fig. 3-18(a) and 3-18(b). In addition, the thermal resistance can be calculated by using $R_{th} = (\Delta\lambda/\Delta P_{diss}) / (\Delta\lambda/\Delta T)$ [100], which is 2.878 K/mW for the ~7 µm oxide-aperture diameter VCSEL.

3.3.3 Small-Signal Measurements

Small-signal modulation response (S21) and reflection (S11) measurements can be measured at the same time. The operating currents are determined by a digital source meter (Keithley 2400-LV), which is connected via an HP 8722C Network Analyzer

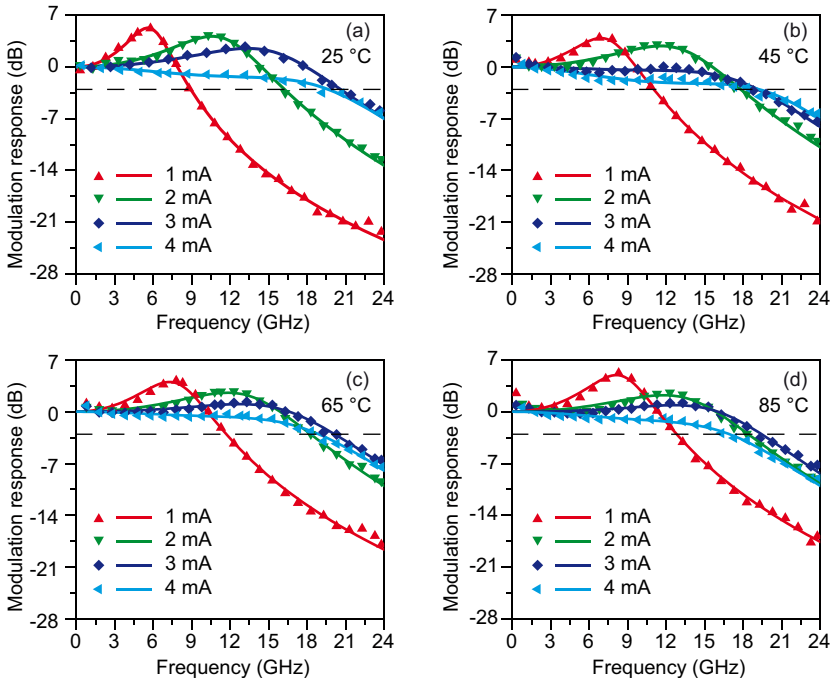

Fig. 3-19. Magnitude of the small-signal modulation response S21 for different applied bias currents and the corresponding fits by using a transfer function at 25 °C (a), 45 °C (b), 65 °C (c), and 85 °C (d) for a ~2.5 µm oxide-aperture diameter 980 nm VCSEL.

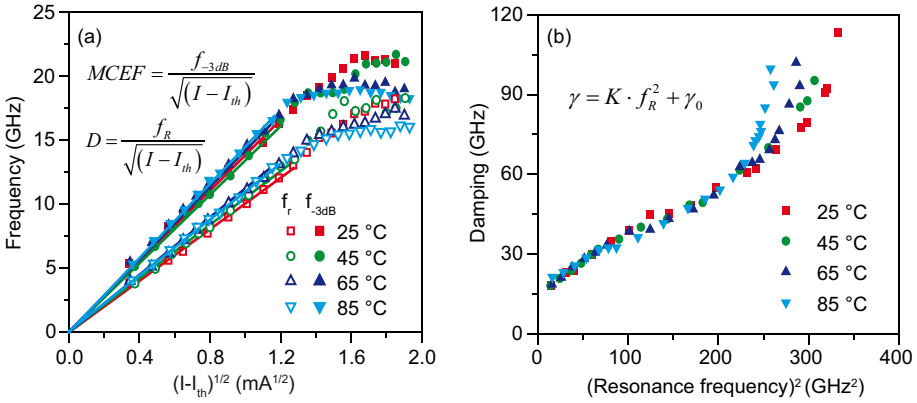

Fig. 3-20. –3 dB bandwidth and relaxation resonance frequency versus the square root of bias current minus threshold current (a) and damping rate versus squared relaxation resonance frequency (b) at 25, 45, 65 and 85 °C for the ~2.5 µm oxide-aperture diameter VCSEL.

to the VCSEL under test. The constant signal from the source meter is overlapped with a small harmonic signal from the network analyzer and delivered to the device under test. The output optical signals from the VCSELs are coupled into a multi-mode optical fiber and guided to a calibrated photodetector (New Focus 1434-50-M [119, 120] with a bandwidth of 25 GHz), which is connected to the second port of the network analyzer. After measurement, the response of the detector is subtracted to eliminate its influence on the measured response. A small-signal electrical equivalent circuit model [121, 122] is used for the S11 reflection measurements data fitting, in order to obtain the parasitic cut-off frequencies. With these pre-determined parasitic cut-off frequencies, the S21 modulation responses are fitted using a transfer function to extract the relaxation resonance frequency f_r and the damping factor γ [69].

The measured S21 curves with corresponding fits for different currents at 25, 45, 65 and 85 °C for a ~2.5 µm oxide-aperture diameter 980 nm VCSEL are shown in Fig. 3-19. The extracted –3 dB bandwidth and relaxation resonance frequency versus the square root of bias current minus threshold current and damping rate versus the squared relaxation resonance frequency are shown in Fig. 3-20. The *MCEF* can be obtained from the slope of the linear dependence of the –3 dB bandwidth versus the square root of the quantity bias current minus the threshold current. The *D*-factor can be obtained from the linear fit of the relaxation resonance frequency versus the square root of the quantity bias current minus threshold current. The *K*-factor can be obtained from the relationship of damping and the square of the relaxation resonance frequency.

3.3.4 Data Transmission Measurements

For data transmission measurements, VCSELs are driven by a combined signal consisting of a constant bias signal and an amplified bit pattern. A digital source meter is used for the constant bias signal, and the pseudorandom bit patterns are generated by a 12100B bit pattern generator from SHF Communication Technologies AG (Berlin, Germany) followed by an 8 dB amplifier and a 3 dB electrical attenuator to compensate for the losses of the electrical wires. After amplification, the signal is superimposed onto the DC biased VCSEL using a 65-GHz SHF bias-tee and a 67 GHz-rated coplanar GSG probe. Simple fiber-to-VCSEL butt-coupling is used to couple the light into a 5 m long OM2 multi-mode optical fiber. A variable optical attenuator is used in front of the photoreceiver for both the determination of the bit error ratio (BER) and for measurements of the eye diagrams. Eye diagrams and bit error ratio measurements are studied using a 70 GHz Agilent sampling oscilloscope 86100C and a SHF 11100B error analyzer. An u^2t Photonics AG photoreceiver with an integrated limiting transimpedance amplifier is used for recording the optical eye diagrams and for measuring the BERs. The bandwidth of this photoreceiver is ~28 GHz. A standard non-return to zero (NRZ) modulation scheme with a 2^7-1 bit word-length in a pseudorandom binary sequence (PRBS) is used for all transmission measurements. Fig. 3-21 shows eye diagrams for a ~7 µm oxide-aperture diameter

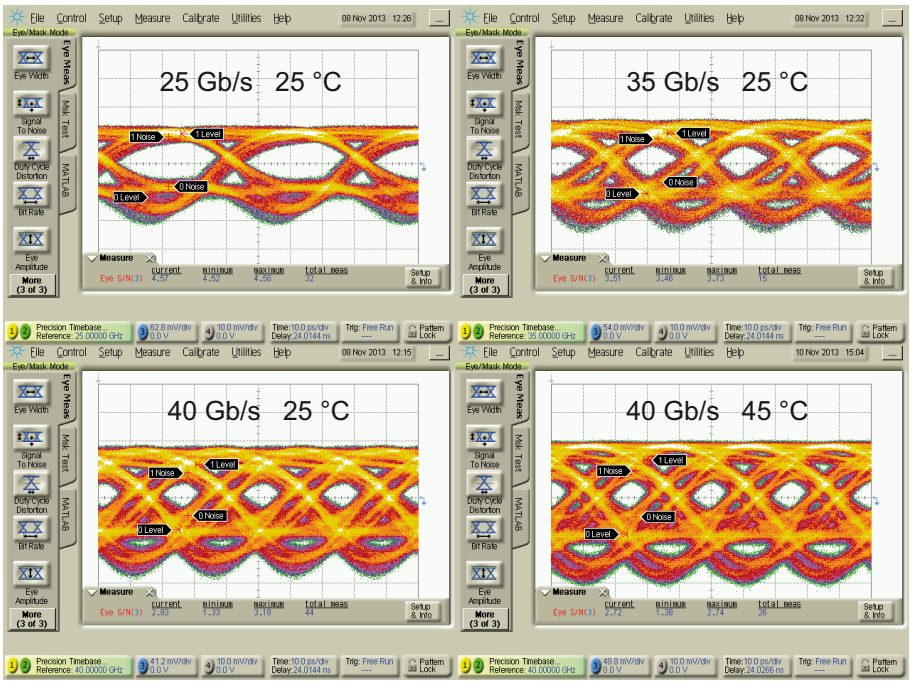

Fig. 3-21. Eye diagram for a ~7 µm oxide-aperture diameter VCSEL operating at 25 and 35 Gb/s at 25 °C, and 40 Gb/s at 25 °C and at 45 °C.

980 nm VCSEL operating at 25, 35, and 40 Gb/s at 25 °C, and at 40 Gb/s at 45 °C. In Fig. 3-21 it can be seen that clear open eyes can be obtain at 40 Gb/s at 25 and 45 °C for the ~7 μm oxide-aperture diameter 980 nm VCSELs. BER test results for 20, 30, 36 and 40 Gb/s error-free data transmission are shown in Fig. 3-22, which shows error-free data transmission at 40 Gb/s at room temperature can be achieved using a ~7 μm oxide-aperture diameter 980 nm VCSEL.

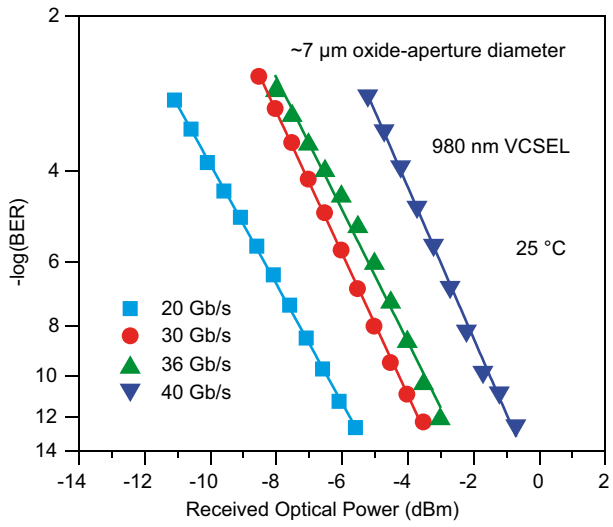

Fig. 3-22. Bit error ratio (BER) versus received optical power for a ~7 μm oxide-aperture diameter 980 nm VCSEL operating at 24, 30, 36 and 40 Gb/s at 25 °C.

Chapter 4

Impedance Characteristics

In this Chapter, the temperature dependence of the impedance characteristics is studied for high bit-rate, highly temperature-stable 980 nm oxide-aperture VCSELs. A small-signal equivalent circuit model is fitted to measured small-signal reflection S11 parameters across a large range of operating bias currents, temperatures, and oxide-aperture diameters to extract the circuit elements and parasitic cutoff frequency for each particular operating condition. The parasitic cutoff frequencies of small oxide-aperture diameter VCSELs is highly temperature-insensitive from room temperature up to 85 °C, and does not limit the VCSELs' maximum data transmission rate. Finally, the dependence of the impedance characteristics and modulation bandwidth on the oxide-aperture diameter is analyzed at 25 and 85 °C. The results show that the larger capacitance is the main reason larger oxide-aperture diameter VCSELs, compared to smaller aperture VCSELs, have a lower parasitic cutoff frequency. The results are useful for the device-, circuit-, and microsystem- level modeling of VCSELs, optical interconnect subassemblies, and hybrid integrated photonics systems that employ VCSELs. The results are also useful for analyzing the performance of state-of-the-art visible and infrared (~600 − 1600 nm) VCSELs to further understand the device design and performance trade-offs and to improve the performance of future device iterations.

4.1 Motivation and Applications

The VCSEL is a cost-effective, energy-efficient, and reliable light source for short-reach optical interconnects in datacenters and supercomputers [123–125]. Vast arrays of VCSELs are envisioned for use in photonic integrated circuits for chip-to-chip and on-chip optical computer communications, where the intrinsic temperatures of the VCSELs placed close to silicon processor cores, memories, and input-output

circuits may soar. The continuous operating temperature may be 85 °C or higher in future commercial optical interconnect applications, and furthermore the VCSELs may be operated in and out of an idle-mode, sleep-mode, or at various bias currents to optimize the energy efficiency of the system. Given the desire to reduce operating costs and energy consumption by not cooling the system components the VCSELs must thus perform well over a large range of temperatures from near zero to 85 °C. There are three primary factors that can limit the intrinsic modulation bandwidth of VCSELs including: 1) thermal effects; 2) over damping; and 3) extrinsic parasitic elements [69]. Several groups have investigated the thermal effects [69, 86, 126] and damping limitations [111] of VCSELs, and therefore in this work a detailed systematic study and analysis of the third critical factor, the influences of parasitic elements on the modulation bandwidth is performed, seeking techniques to optimize the epitaxial design, the device structure and geometry, and thus the high frequency performance. In particular parasitic elements at room temperature and at high temperatures and with variations of oxide-aperture diameter are analyzed in detail for high-speed, highly temperature-stable 980 nm VCSELs. Thus, the key factors that limit the performance for different oxide-aperture diameter VCSELs versus temperature are analyzed to determine how to minimize the impact of these elements on the high bit-rate modulation performance of VCSELs.

4.1.1 Equivalent Circuit Model for VCSELs

In order to better understand how the extrinsic electrical properties of VCSELs affect their modulation bandwidth, the reflection coefficient S11 and the S21 scattering parameter are measured and analyzed for a large range of currents, oxide-aperture diameters, and heat-sink temperatures. Through small-signal equivalent-circuit modeling [121, 127–129] where the reflection coefficient S11 data are fitted to an equivalent circuit model to obtain the circuit capacitances and resistances. The parasitic cutoff frequency f_p can then be determined. With this pre-determined value of parasitic cutoff frequency f_p, and using the measured S21 data, the resonance relaxation frequency f_r and the intrinsic damping coefficient γ can then be determined. Furthermore, with this modeling information the parasitic influence can be de-embedded [121] to obtain the estimated intrinsic frequency response of VCSELs. This also can determine intrinsic parameters including the gain slope coefficient, photon lifetime, and spontaneous emission recombination lifetime [130]. The result is a more detailed understanding of the devices and insight on how to improve the performance of subsequent device iterations.

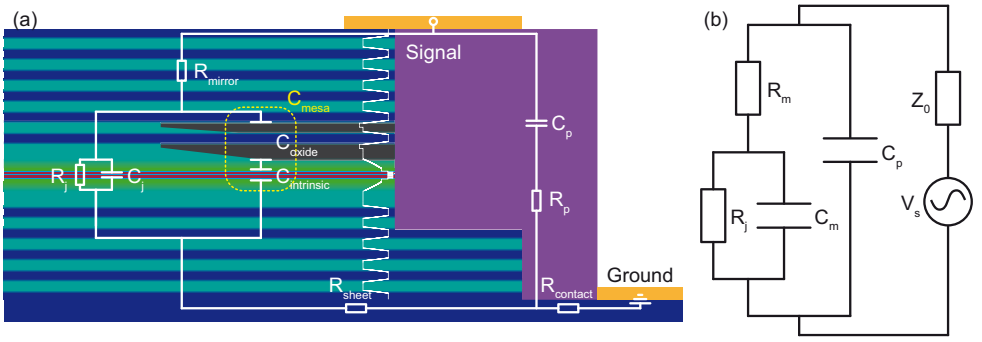

Fig. 4-1. Cross-sectional schematic of the VCSEL structure including electrical parasitic capacitances and resistances (a), and a simplified electrical equivalent-circuit model (b).

Fig. 4-1(a) shows a cross-sectional schematic view of the VCSEL structure including the electrical parasitic capacitance and resistance elements. C_p and R_p represent the contact pad capacitance and resistance between the p-contact and n-contact. The term R_p and all inductive elements are neglected as these elements are determined to be negligible in S-parameter fittings and may be replaced by zero impedance wires. The circuit element R_{mirror} is the combined series mirror resistance of the p-DBR and the n-DBR, the circuit element R_{sheet} is the sheet resistance in the n-contact layer, and the circuit element $R_{contact}$ is the combined p-contact and n-contact resistances. These resistances are grouped together into R_m (where $R_m = R_{mirror} + R_{sheet} + R_{contact}$) as shown in Fig. 4-1(b). R_j represents the junction resistance. The mesa capacitance C_{mesa} consists of the oxide-aperture capacitance C_{oxide} in series with the intrinsic region layers capacitance $C_{intrinsic}$. Thus the mesa capacitance can be expressed as $C_{mesa} = (C_{oxide}^{-1} + C_{intrinsic}^{-1})^{-1}$. The circuit element C_j is the capacitance of the junction region. This term combine with the mesa capacitance into $C_m = C_{mesa} + C_j$. The final resulting simplified electrical small-signal equivalent circuit model for VCSELs after combining several of the original electrical elements is shown in Fig. 4-1(b), along with a microwave voltage source V_s and the characteristic source output impedance of the measuring equipment Z_0, which is 50 Ω.

The load impedance [128, 131] of the electrical equivalent circuit in Fig. 4.1(b) is:

$$Z(f) = \left(\frac{1}{Z_1} + \frac{1}{Z_2}\right)^{-1} \tag{4.1}$$

where $$Z_1 = R_m + \left(\frac{1}{R_j} + i2\pi f C_m\right)^{-1}, \text{ and } Z_2 = \left(i2\pi f C_p\right)^{-1} \tag{4.2}$$

The complex reflection 2-port S-parameter S11 can be expressed with the impedances as:

$$S_{11}(f) = \frac{Z(f) - Z_0}{Z(f) + Z_0} \tag{4.3}$$

where Z_0 is the characteristic source output impedance of the measuring equipment (50 Ω). Therefore, the equivalent impedance of the VCSEL can be determined from the measured reflection coefficient S11 using:

$$Z(f) = Z_0 \frac{1 + S_{11}(f)}{1 - S_{11}(f)} \tag{4.4}$$

The transfer function due to the electrical parasitic effects [127] is:

$$H_{\text{par}}(f) = i(f)/V_{\text{s}} \tag{4.5}$$

where $i(f)$ is the current through R_{j}, and V_{s} is the source voltage. The parasitic cutoff frequency f_{p} is defined as the frequency where:

$$\frac{|H_{par}(f)^2|}{|H_{par}(0)^2|} = 1/2 \tag{4.6}$$

4.1.2 Measurement of Impedance

The impedance is obtained by measuring the real part and the imaginary part of the complex impedance vector using a reflection coefficient measurement S11 with an HP 8722C Network Analyzer. The S21 scattering parameter data are measured at the same time by the same measurement setup. For the S11 reflection measurement, a pre-measurement system calibration is very important, as both the magnitude and phase information are needed. So the entire measurement setup is calibrated to the radio frequency (RF) probe tip to avoid any electrical delay, otherwise the RF probe will add an extra frequency-dependent phase shift to the measured data. A full two-port calibration procedure is used. This calibration uses the short, open, and broadband load standards on a calibration substrate. Due to system drift, the calibration must be performed immediately before the S11 measurement to ensure the accuracy of the results. The values of the equivalent-circuit elements for the simplified model (given in Fig. 4-1(b)) are determined by fitting the simulated results to the measured scattering parameters. Fig. 4-2 shows one fitting example for a ~2.5 μm oxide-aperture diameter 980 nm VCSEL with a forward bias current of 2 mA at room temperature. The fit shows very good agreement with the measured data, and this helps to verify the validity of the equivalent-circuit model. The same measurements and evaluations are completed for many different oxide-aperture diameter VCSELs at different bias currents, and at different operating temperatures.

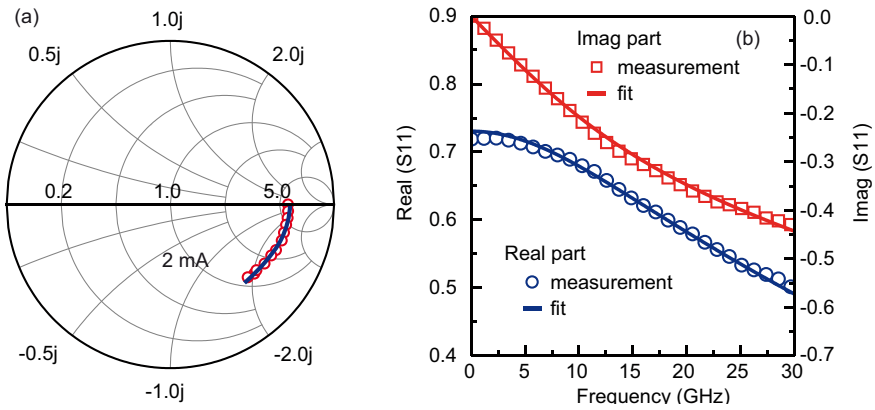

Fig. 4-2. Measured S11 values for a ~2.5 µm oxide-aperture diameter 980 nm VCSEL operating at 2 mA at 25 °C plotted on a Smith Chart over a frequency range from 50 MHz to 30 GHz (a), and the real and the imaginary parts of S11 versus frequency (b). The curve fits using the simplified equivalent circuit model are shown as solid lines, whereas the measured data are shown as the open symbols.

4.2 Experimental Results

4.2.1 Impedance vs. Temperature

The 980 nm VCSELs in this work show highly temperature-stable large-signal modulation performance and high bit-rates, and energy efficient data transmission at high temperatures, as detailed discussed in Chapter 6. To show how the small-signal reflection response changes with increasing temperature, complex S11 values are measured for a ~4 µm oxide-aperture diameter VCSEL operating at forward bias currents ranging between 1 to 8 mA at room temperature and at 85 °C. The S11 data are then plotted on a Smith Chart over a frequency range from 50 MHz to 30 GHz as shown in Fig. 4-3. The curve fits using the equivalent circuit model from Fig. 4-1(b) are also shown. The measured real and imaginary parts of S11 and the corresponding curve fits are shown in Fig. 4-4 on linear-linear plots. The curve fits of the real and the imaginary parts of S11 match very well to the measured data.

The small-signal reflection coefficient S11 and the scattering parameter S21 are measured for a small oxide-aperture diameter 980 nm VCSEL over a wide range of currents at 25, 45, 65, and 85 °C to further understand the influence of parasitic device parameters at different temperatures. First the electrical reflection S11 data are fitted to the equivalent circuit model [129]. The values of the equivalent-circuit elements can be obtained through this fitting and the parasitic cutoff frequency can be determined through the parasitic response. The capacitance values extracted at 25, 45, 65, and 85 °C are plotted in Fig. 4-5(a). The C_m values (the combination of

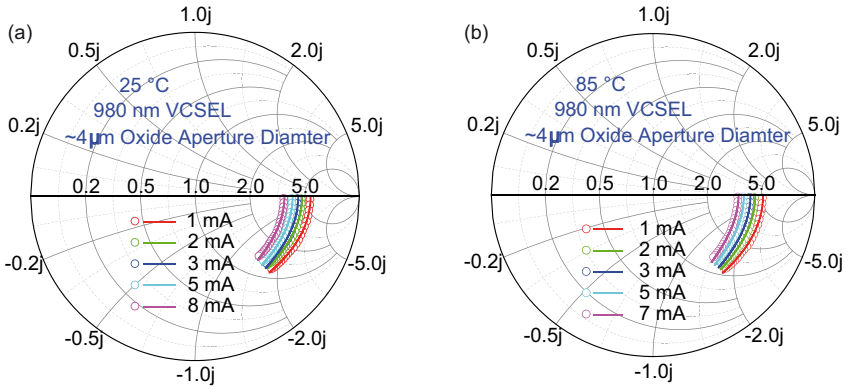

Fig. 4-3. Measured complex S11 values for a ~4 μm oxide-aperture diameter 980 nm VCSEL operating at different currents at 25 °C (a) and at 85 °C (b) plotted on a Smith Chart over a frequency range from 50 MHz to 30 GHz. The curve fits using the equivalent circuit model are shown as solid lines, whereas the measured data are shown as the open symbols.

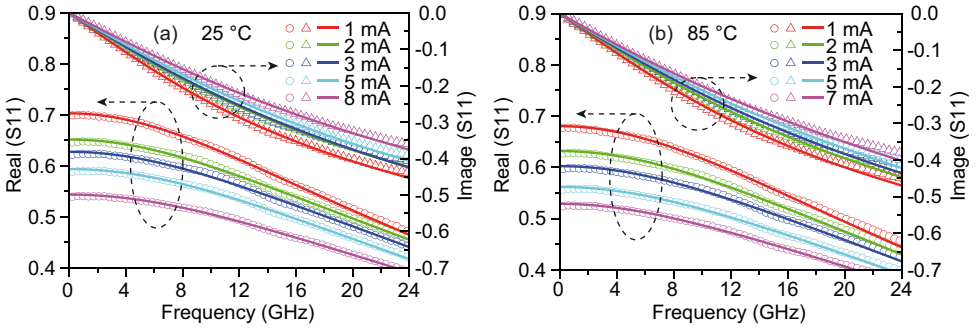

Fig. 4-4. Measured real (circles) and the imaginary (triangles) parts of S11 for a ~4 μm diameter oxide aperture 980 nm VCSEL operating at different currents at 25 °C (a) and at 85 °C (b). The curve fits using the equivalent circuit model are shown as solid lines, whereas the measured data are shown as the open symbols.

capacitance of the intrinsic region layer and the mesa capacitance) are shown as solid symbols, and the contact pad capacitances C_p are shown as hollow symbols. The C_m increase with increasing current at all temperatures. In addition, the values of C_m at low currents are higher at room temperature compared to their values at high temperatures. The resistance values extracted at 25, 45, 65, and 85 °C are shown in Fig. 4-5(b). The junction resistances R_j are shown as solid symbols, and the R_m data (combination of series mirror resistance, sheet resistance, and contact resistances) are shown as hollow symbols. The R_j decrease fast with increasing current at all temperatures. The R_m values also decrease with increasing current, but this reduction is relatively small. The R_m values are higher at room temperature compared to their values at high temperatures. The VCSEL's mirror resistance is higher than desired, with R_m greater than 150 Ω at room temperature, although this is not unusual for such

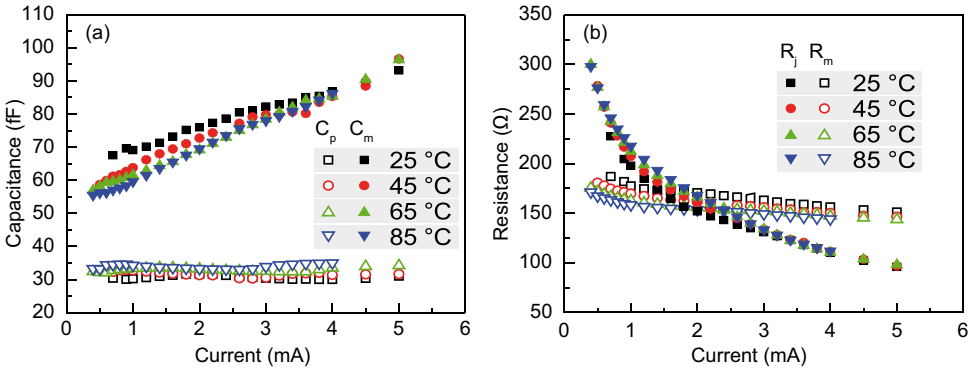

Fig. 4-5. Extracted values of the equivalent-circuit elements as a function of current for a ~2.5 µm oxide-aperture diameter 980 nm VCSEL at 25, 45, 65, and 85 °C. (a) The C_m (combination of the capacitance of the intrinsic region layer and the mesa capacitance) are shown as solid symbols, and the C_p (the contact pad capacitance between the p- and n-contacts) are shown as unfilled symbols. (b) The R_j (junction resistance) are shown as solid symbols, and the R_m (combination of the series mirror resistance of the p-DBR and n-DBR, the sheet resistance in the n-contact layer, and the p- and n-contact resistances) are shown as unfilled symbols.

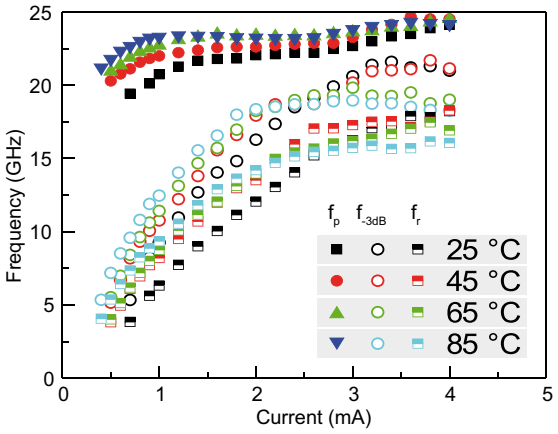

Fig. 4-6. Extracted small-signal modulation response and reflection measurements including the parasitic cut-off frequency f_p (solid symbols), the –3 dB frequency f_{-3dB} (hollow symbols), and the relaxation resonance frequency f_r (half-solid symbols) as a function of current for a ~2.5 µm oxide-aperture diameter 980 nm VCSEL at 25, 45, 65, and 85 °C.

small oxide-aperture diameter (~2.5 µm) VCSELs. This leaves room to improve the DBRs to lower the series resistance in future designs via perhaps improved grading and doping schemes.

The transfer function, which is described in [69], is used to fit the measured modulation response. The response of the photoreceiver is subtracted to eliminate its influence on the measured data. The relaxation resonance frequency f_r and the damping factor γ are extracted using the standard single-mode emission rate equation model for semiconductor diode lasers [69]. The –3 dB modulation bandwidth f_{-3dB} is also extracted from the transfer function fits of the modulation response. The parasitic cutoff frequency f_p is reasonably temperature insensitive, as seen in Fig. 4-6. There is only a small increase in f_p with an increase of bias current. By comparing the f_{-3dB} and f_p values at a given current and temperature, f_p is higher than f_{-3dB} from 25 to 85 °C (Fig. 4-6) across the entire measured current range. Thus parasitics are not limiting the high frequency performance of the small oxide-aperture 980 nm

VCSELs. In fact, the f_p increases when moving from 25 to 85 °C, and this benefits the VCSELs' temperature stable high bit-rate performance. The given extracted values of f_r, f_p, and f_{-3dB} show that the high bit-rate performance of the small oxide-oxide aperture VCSELs are limited by thermal effects, and partially by over damping.

4.2.2 Impedance vs. Oxide-Aperture Diameter

The maximum achievable bit rate and minimum possible energy dissipation per bit for error-free data transmission are both strongly dependent on the oxide-aperture diameter of the VCSEL, which will be discussed in further detail in Chapter 7. The VCSELs with oxide-aperture diameters of ~3 to 5 µm are most suitable for energy-efficient and high-speed operation at high temperatures. It is interesting to determine how the parasitic cutoff frequency and the values of the small-signal

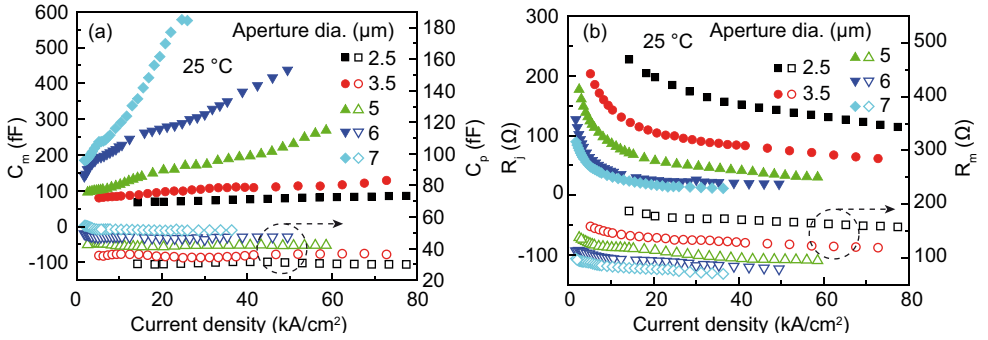

Fig. 4-7. Extracted values of the equivalent-circuit elements as functions of current density for ~2.5, 3.5, 5, 6, and 7 µm 980 nm oxide-aperture diameter VCSELs at 25 °C; (a) the C_m are shown as filled symbols, and the C_p are shown as unfilled symbols; (b) the R_j are shown as filled symbols, and the R_m are shown as solid symbols.

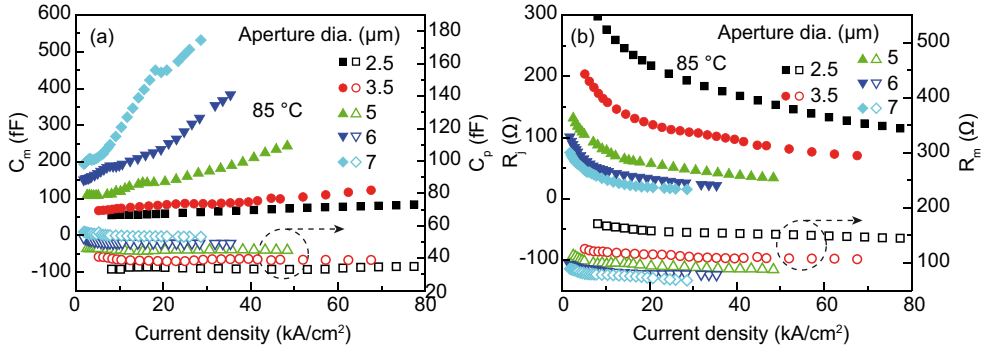

Fig. 4-8. Extracted values of the equivalent-circuit elements as functions of current density for ~2.5, 3.5, 5, 6, and 7 µm 980 nm oxide-aperture diameter VCSELs at 85 °C; (a) the C_m are shown as filled symbols, and the C_p as unfilled symbols; (b) the R_j are shown as filled symbols, and the R_m are shown as solid symbols.

equivalent-circuit elements change with the VCSEL's oxide-aperture diameter. Thus oxide-aperture diameter-dependent small-signal measurements are performed. The extracted capacitance results of ~2.5, 3.5, 5, 6, and 7 µm oxide-aperture diameter VCSELs at 25 °C are shown in Fig. 4-7(a). The C_m increases with increasing current density for all VCSELs. In addition, the value of C_m is larger for large oxide-aperture diameter VCSELs, which have larger mesa diameters compared to small oxide-aperture VCSELs. For the entire current density range, small oxide-aperture diameter VCSELs have a smaller C_m at the same current density. The values of C_p have a negligible change with increasing current density. The extracted capacitance results at 85 °C are shown in Fig. 4-8(a), which shows a similar change as at 25 °C, only with different values. The value of C_m is lower at 85 °C than at 25 °C for the entire current range investigated here, which is the same as observed for the ~2.5 µm oxide-apertures diameter VCSEL as shown in 4-5(a). The resistance results (as shown in Fig. 4-7(b)) for ~2.5, 3.5, 5, 6, and 7 µm oxide-apertures diameter VCSELs at 25 °C show that small oxide-aperture diameter VCSELs have larger R_j and R_m than the large oxide-aperture diameter VCSELs at the same current density as is expected due to current crowding. The VCSEL resistances at 85 °C follow the same general trend as the resistances at 25 °C, as shown in Fig. 4-8(d). The junction resistance R_j is higher at 85 °C than at 25 °C for the entire current range investigated here. This is also the same as what has been observed before for the ~2.5 µm oxide-apertures diameter VCSEL as shown in 4-5(b). The opposite change trends of the capacitance and the resistance offset each other, which leads to a highly temperature-stable parasitic cutoff frequency for the different oxide-aperture VCSELs.

Thus, as expected larger oxide-aperture diameter VCSELs have a higher capacitance and a lower resistance compared to smaller VCSELs, and at the same current density, the capacitance C_m increases faster with growing oxide-aperture diameter.

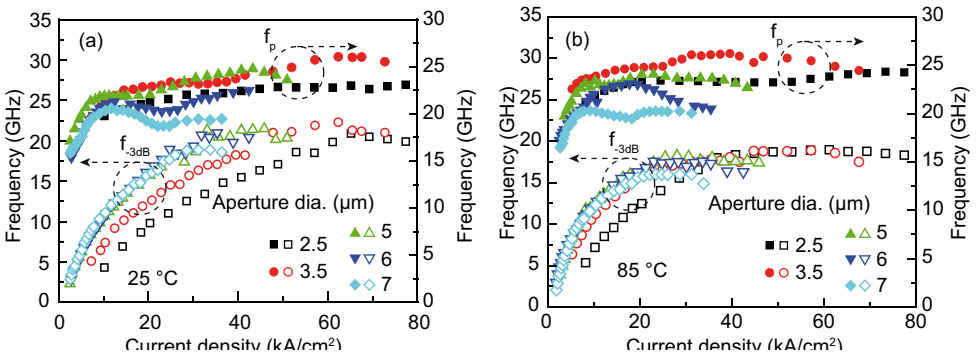

Fig. 4-9. Parasitic cut-off frequency f_p extracted from small-signal modulation response and reflection measurements at increasing bias current density for ~2.5, 3.5, 5, 6, and 7 µm oxide aperture diameter 980 nm VCSELs at 25 °C (a) and at 85 °C (b).

This is in contrast to the resistance R_j and its slower decrease with increasing oxide-aperture diameters. The net result is a near-stable f_p with increasing current density. Fig. 4-9 shows the extracted parasitic cutoff frequency at room temperature and at high temperature. The ~3.5 μm oxide-aperture diameter 980 nm VCSEL has the highest parasitic cutoff frequency both at room temperature and at high temperature. With further increases of the oxide-aperture diameter, the parasitic cutoff frequency starts to decrease. Large oxide-aperture diameter VCSELs have a noticeably lower parasitic cutoff frequency. This is because the resistances decrease slowly while the capacitance rapidly increases as the device area increases. This high capacitance and its faster change with increasing bias current is the main reason for a reduced parasitic cutoff frequency. Thus, the capacitance can be further decreased to improve the parasitic cutoff frequency, by for example reducing the mesa area, by adding additional deep oxide layers without increasing mirror resistance, or perhaps by using an added proton implantation.

4.3 Summary

The temperature-dependent and oxide-aperture diameter-dependent impedance characteristics are investigated for high-speed, highly temperature-stable 980 nm VCSELs. The values of the small-signal equivalent-circuit elements (capacitances and resistances) over a large range of currents at different temperatures are compared. The analysis shows that small oxide-aperture diameter VCSELs are not limited by parasitics at temperatures from 25 to 85 °C. The study of oxide aperture-dependent impedance also shows that the larger capacitance of larger oxide-aperture VCSELs limits the VCSELs' parasitic cutoff frequency. This work provides a better understanding of the direct current modulation rate limitation of VCSELs at different temperatures, and gives insight on how to maximize 980 nm VCSELs' high frequency performance.

Chapter 5

980 nm VCSEL Noise Characteristics

Semiconductor laser relative intensity noise (RIN) is the major source of data communication system noise. RIN characterizes the relative amplitude of optical power fluctuation around the average optical power level, which is often associated with transmission of optical data, as it limits the maximum available signal-to-noise ratio (S/N) of the laser during signal modulation. In high-speed digital systems, RIN can limit the bit-error ratio and the system performance under certain conditions. This makes the RIN value an important parameter for characterizing optical communication systems.

5.1 Semiconductor Laser RIN

Relative intensity noise in a laser diode is caused by random carrier and photon recombination and generation events, producing instantaneous time variations in the carrier and photon densities. The intensity noise mainly comes from the laser diode mode competition, as well as the optical interference between the coherent laser modes and the spontaneous light emission. A laser with low RIN is essential in the pursuit of high fidelity optical transmission. According to [132], the RIN needs to be below −128 dB/Hz for reliable 28 Gb/s optical data transmission. As RIN changes with bias current and with the oxide-aperture diameter of VCSELs, it is useful to know the RIN value at the bias conditions for high bit-rate and energy efficient operation.

The variation in photon density causes a variation in output power. The intensity noise (optical power fluctuations) is quantified using the relative intensity noise, which is the power noise normalized to the average power level. Optical power is

detected with a fast photodetector, and thus the optical power fluctuations are transformed into electrical power fluctuations, which are measured with an electrical spectrum analyzer (ESA). RIN can be expressed through the electrical values:

$$RIN = \frac{N_{total}}{P_{avg,elec}} = \frac{N_{laser} + N_{th} + N_{PD,shot}}{P_{avg,elec}} \text{ (dB/Hz)} \tag{5.1}$$

where N_{total} (dBm/Hz) is the overall noise and $P_{\text{avg,elec}}$ is the average electrical power. The overall noise N_{total} has three noise components: the VCSEL noise N_{laser}, the thermal noise N_{th}, and shot noise $N_{\text{PD,shot}}$. The total amplified system noise power spectrum N_{total} is measure by the ESA with the laser diode on. By turning off the laser and keeping the operation of the photodetector and amplifiers, the signal analyzer measures only the thermal noise power spectrum $N_{\text{th}}(f)$. N_{total} and N_{th} are weighted using the power spectral density per unit bandwidth with the unit of dBm/Hz, which can be calculated from noise power (dBm) and the resolution bandwidth (RBW) of the ESA using 1 dBm/Hz = 1 dBm − 10 log(BW). $G(f)$ (dB) is the frequency-depended amplifier power gain. Shot noise $N_{\text{PD,shot}} = 2qI_{\text{ph}}R_{\text{L}}$ is the shot noise power of the photodetector under the average input laser power P_0, I_{ph} is the photocurrent out of the photodetector, R_{L} is the load resistance of the amplifier input port. $N_{\text{PD,shot}}$ appears at the photodetector and rises proportionally to the detected optical power. The average electrical power $P_{\text{avg,elec}} = I_{\text{ph}}{}^2 R_{\text{L}}$. After subtracting the system thermal noise and the photodetector shot noise, the intrinsic laser RIN can be extracted as:

$$RIN\big|_{laser}(f) = \frac{\left[N_{total}(f) - N_{th}(f)\right]/G(f) - N_{PD,shot}}{P_{avg,elec}} \tag{5.2}$$

RIN corresponding to shot noise can be calculated as:

$$RIN\,|_{PD,shot} = \frac{N_{PD,shot}}{P_{avg,elec}} = \frac{2qI_{ph}R_l}{I_{ph}^2 R_L} = \frac{2q}{I_{ph}} \tag{5.3}$$

From a small-signal analysis of the rate equations for a single-mode laser diode, the transfer function describing the RIN spectrum attains the following frequency dependence [69, 133]:

$$RIN(f) = \frac{Af^2 + B}{\left(f_r^2 - f^2\right)^2 + \left(\gamma/2\pi\right)^2 f^2} \tag{5.4}$$

which shows that RIN peaks at the relaxation resonance frequency, and A and B are given in Ref. [133].

5.1.1 Laser Diode RIN Measurement

The laser diode RIN is characterized with the measurement setup in Fig. 5-1. The VCSEL under test is biased at constant DC currents, and the output light is directly coupled into a 5 m-length lensed multimode fiber. The optical fiber is connected to a high speed New Focus 25 GHz photodetector 1434-50, and the signal is amplified by two cascaded amplifiers SHF 100AP and SHF 804EA with a gain of 19 and 20 dB to produce enough amplification to raise the signal above the noise floor of our spectrum analyzer. The frequency-dependent total amplifier power gain $G(f)$ of the two cascaded amplifiers is measured using a Network Analyzer. This factor $G(f)$ is subtracted from the noise measured by the ESA to compensate for the gain and the frequency response of the amplifiers. The New Focus photodetector has a build in bias monitor to measure the average photocurrent during the measurements. The average DC photocurrent can be calculated using a gain factor of 1 mV/μA to determine the average optical power. To measure one RIN value at a specific diode current, the first measurement is performed with the VCSEL turned on to determine the amplified overall noise N_{total} by using a Hewlett-Packard (HP) 8562A Spectrum Analyzer. Then a second measurement is performed with the VCSEL turned off, while leaving unchanged the photodetector and amplifiers, to determine the thermal noise N_{th}. The thermal noise does not depend on the optical power, which can be simply subtracted from the total noise. The resolution bandwidth of the ESA should be set low enough for the highest possible measurement precision with still enough sensitivity. The measurement precision is set at 30 kHz for the following measurements. The VCSEL RIN can be extracted by fitting to the theoretical small signal model using equation (5.4) as described in [69, 133].

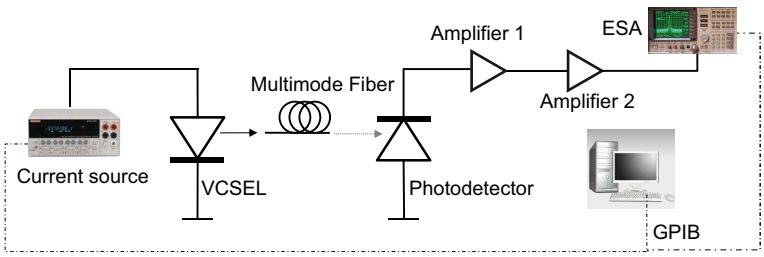

Fig. 5-1. Schematic view of the RIN measurement setup for 980 nm VCSELs

5.1.2 RIN Specification Trend for the Fibre Channel Standard

VCSELs have attractive features that have made these laser diodes the most popular transmitter choice in short-range optical communication links. The Fibre Channel standard is one of the most important standards in short-range communications across optical fiber [132]. A summary of the Fibre Channel standards that have been ratified to date is shown in Tab. 5-1 [132, 134, 135]. Obviously, the criteria specified for RIN has become more and stricter as the bit rate increases. It is interesting to investigate whether VCSELs can satisfy the requirements of the relative intensity noise performance. In addition, the knowledge learned from RIN data can be used to better construct next generation designs to improve the performance of these VCSELs for specific low-noise applications

Tab. 5-1. RIN specifications in the different Fibre Channel standards to date [133, 135, 136], [137, 138]*

Standard	Line Rate (GBaud)	VCSEL RIN (dB/Hz)	Market Availability (Year)
1 GFC	1.0625	−116	1997
2 GFC	2.125	−117	2001
4 GFC	4.25	−118	2005
8 GFC	8.5	−128	2008
16 GFC	14.025	−128	2011
32 GFC	28.5	−131*	2014

5.2 980 nm RIN Characteristics

Laser diode RIN depends on many device performance and measurement test condition parameters, the most important are test frequency, laser diode output power, the operating temperature, modulation frequency, modulation signal time delay, the magnitude of any optical feedback, the side-mode-suppression ratio of the emission spectra, and the relaxation oscillation frequency.

5.2.1 980 nm RIN versus Bias Current

Fig. 5-2 (a) shows the measured RIN spectra for different bias currents above the threshold current at room temperature for a ~3 µm oxide-aperture diameter 980 nm VCSEL as well as the calculated shot noise level for the highest bias current. The threshold current is 0.33 mA. Fitted theoretical curves using equation (5.4) are included for four of the curves. The behavior is as expected [69], with maximum noise intensity at the relaxation oscillation frequency, an increasing relaxation frequency with bias current, and a decrease in the RIN with an increase in bias current. This is because the predominant source of RIN is usually spontaneous emission. Hence, RIN reaches a maximum just above threshold when the spontaneous emission is typically at a maximum, and then the RIN decreases with increasing bias current, when the noise power does not increase too much while the optical power increases fast at high currents. These high-frequency RIN spectra contain well-defined peaks and reach the maximum RIN value at the relaxation oscillation frequency. The RIN decreases with increasing bias current, reaching a theoretical minimum level of −152 dB/Hz at a bias current of 3 mA. From the measured photocurrent of 0.55 mA, the shot noise level can be calculated into −152.3 dB/Hz, which is nearly the same as the measured minimum level. At this bias point (3 mA), the measurements are already very close to the measurement system noise. Fig. 5-2(b) shows the maximum RIN value at different currents. The maximum RIN value at measured bias current decreases with increasing current. In order to indicate the achievable speed, the –3 dB bandwidth obtained from S21 measurements at different currents are also shown. For the applied bias current of 3 mA, the –3 dB bandwidths reaches a high value of 19.85 GHz where the RIN is as low as –141 dB/Hz, which is lower than the requirement for the 32 GFC standard [136, 137]. The shot noise limit can be reached by further increasing the forward bias current. The RIN data shows that 980 nm

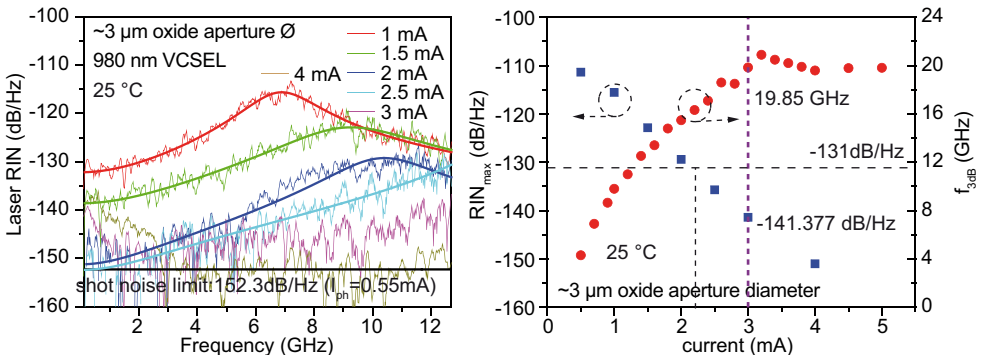

Fig. 5-2. RIN spectra (a) for different bias conditions at room temperature for a ~3 µm oxide-aperture diameter 980 nm VCSEL, and (b) the maximum value of RIN and the –3 dB bandwidth at the maximum RIN versus the bias current.

VCSELs can be operated at high bit-rates with low noise. VCSELs may be operated at the lowest currents where still error-free data transmission is observed to improve energy efficiency. Fig. 5-2 shows that low current usually means a high RIN value, so it is necessary to know whether the RIN is low enough at low currents to also achieve energy efficiency operation. Chapter 7 shows that error-free data transmission at 35, 38, and 42 Gb/s with low power dissipation of 145, 147, and 217 fJ/bit are achieved using the same VCSEL employed here. The bias currents are 2.7, 2.9, 4.1 mA, respectively. According to [132], the requirement of RIN for the 32 GFC Standard is below −131 dB/Hz. Fig. 5-2(b) shows that this RIN requirement can be met with a current larger than 2.2 mA. The current for record energy efficient 35, 38, and 42 Gb/s error-free data transmission are all larger than 2.2 mA, which means RIN is lower than the requirement for the 32 GFC Standard. So this VCSEL can be operated at high bit-rates with low energy dissipation and with low noise.

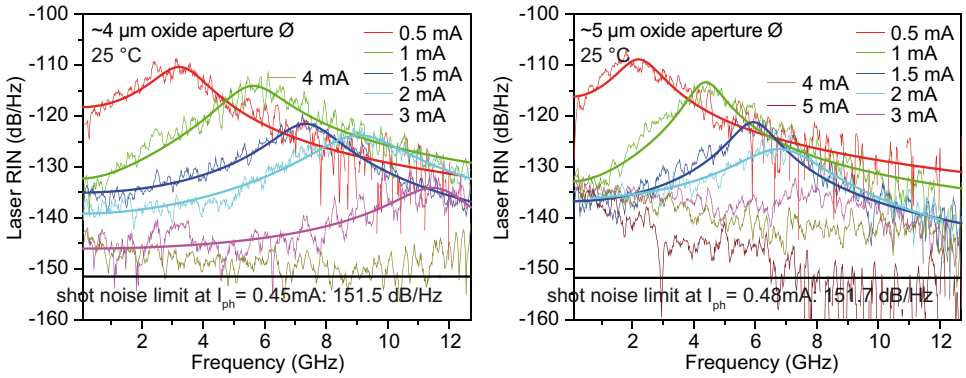

Fig. 5-3. RIN spectra for different bias conditions at room temperature for ~4 µm (a) and ~5 µm (b) oxide-aperture diameter 980 nm VCSELs.

5.2.2 980 nm RIN versus the Oxide-Aperture Diameter

The same measurements and evaluation as in Fig. 5-2(a) are performed for different oxide-aperture diameter 980 nm VCSELs. Fig. 5-3 and Fig. 5-4 show the RIN spectra for different bias currents above threshold at room temperature for ~4 to ~7 µm oxide-aperture diameter 980 nm VCSELs as well as the calculated shot noise level for the highest bias current and the theoretical fitting of the RIN data (the smooth lines). The results are similar to the RIN behavior of the ~3 µm oxide-aperture diameter VCSEL. However, there is one difference at the high bias current. For the small oxide-aperture diameter (~3 µm) VCSEL, the noise saturates at the shot noise floor, but the noise of the large oxide-aperture diameter (~6 and 7 µm) VCSELs is higher due to mode competition. Due to much larger photocurrent, the shot noise level is also lower for larger oxide-aperture diameter VCSELs. Also, larger oxide-aperture

diameter VCSELs are faster (small percentage of rollover current) to achieve low RIN compared to small ones despite higher order mode competition, as shown in Fig. 5-5, where maximum RIN values and the output power versus current are shown. For the same low RIN value of −141 dB/Hz, the bias current needs to be larger than 3 and 6.1 mA for ~3 and 7 µm oxide-aperture diameter VCSELs, respectively. The rollover currents are 6 and 16 mA for ~3 and 7 µm oxide-aperture diameter VCSELs. The bias current needs to be larger than 49 % of the rollover current to have a low RIN of −141 dB/Hz with ~3 µm oxide-aperture diameter VCSELs, but only 37.6 % of the rollover current to have a low RIN of −141 dB/Hz by using ~7 µm oxide-aperture diameter VCSELs. So larger oxide-aperture diameter VCSELs are faster to reach a low RIN value, leading to a lower RIN for high-bit rate operation.

The maximum value of laser diode RIN is at the relaxation resonance frequency. Fig. 5-6 shows these maximum RIN values versus bias current for VCSELs with ~3, 4, 5, 6 and 7 µm oxide-aperture diameters. It is clear that for a given constant current larger oxide-aperture diameters VCSELs have higher RIN values than smaller aperture ones. This is because the photon density is higher for smaller oxide-aperture diameter VCSELs due to the smaller optical mode volume. The relaxation resonance frequency and the damping both increase with an increase in photon density, which

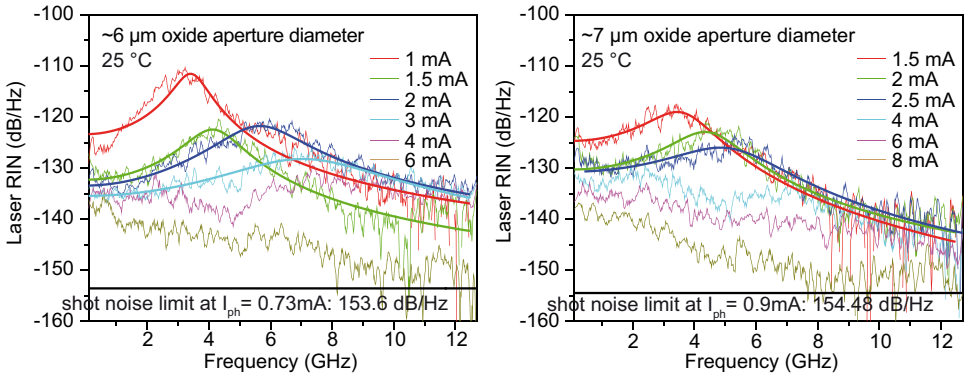

Fig. 5-4. RIN spectra for different bias conditions at room temperature for ~6 µm (a) and ~7 µm (b) oxide-aperture diameter 980 nm VCSELs.

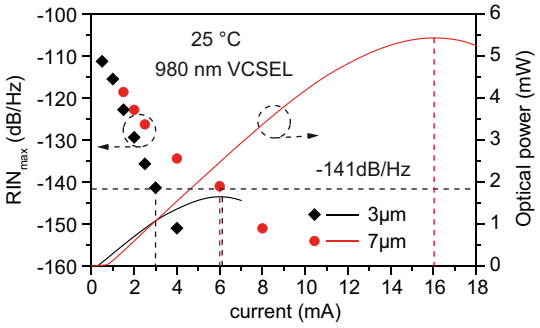

Fig. 5-5. Maximum RIN value and the output power versus current for ~3 and ~7 µm oxide-aperture diameter 980 nm VCSELs.

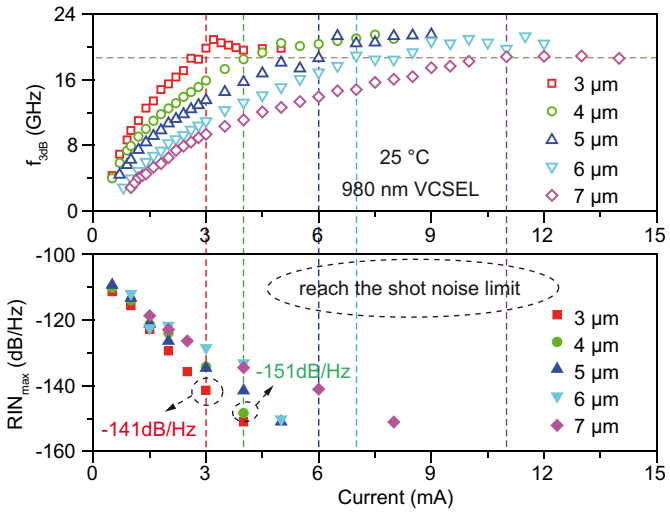

Fig. 5-6. Comparison of maximum RIN value for 980 nm VCSELs with different oxide-aperture diameters operated at room temperature, and the −3 dB bandwidth versus bias current. The −3 dB bandwidth is extracted from the S21 measurements and may be used to estimate the maximum achievable non-return-to-zero error-free bit rate.

leads to lower RIN values for smaller oxide-aperture diameter VCSELs. At the same time, smaller oxide-aperture diameter VCSELs need smaller currents to achieve the same bandwidth, as show in Fig. 5-6. Small currents lead to a high RIN value. To achieve a high –3 dB bandwidth of 18.9 GHz, the RIN is only –141 and –151 dB/Hz for ~3 and ~4 μm oxide-aperture diameter VCSELs, and reaches the shot noise limit for larger VCSELs. So small oxide-aperture diameter VCSELs not only benefit from a higher –3 dB bandwidth and lower energy dissipation, but they also have sufficiently low noise, that enables the use of these VCSELs in future high-speed and low noise optical links with low energy consumption.

5.3 Summary

The relative intensity noise is investigated for high-speed and energy-efficient 980 nm VCSELs. Measurements are performed at different bias currents at room temperature for different oxide-aperture diameter VCSELs. The VCSELs can satisfy the requirements of bandwidth and RIN for the 32 GFC Fibre Channel standard. Larger oxide-aperture diameter VCSELs have higher RIN values than smaller oxide-aperture diameter VCSELs when biased at the same current. To achieve a certain high bandwidth, small oxide-aperture diameter VCSELs can be used for high-speed and energy-efficient data transmission with sufficiently low noise, thus enabling the use of small oxide-confined 980 nm VCSELs in future high bit-rate and low noise optical links with low energy consumption.

Chapter 6

Temperature-Stable 980 nm VCSELs

Vertical-cavity surface-emitting lasers are cost-effective, energy-efficient, and reliable light sources for optical interconnects in datacenters and supercomputers [124, 125, 138]. Highly temperature-stable operation against the temperature variation is a highly desired attribute for high-speed lasers for optical interconnects, because the operating temperature can reach 85 °C or higher in datacenters and supercomputers. These optical interconnects should operate without extra cooling to reduce the cost. This requires that VCSELs are capable of operating over a large temperature range with relatively stable and energy-efficient performance. The experimental results of temperature-stable 980 nm VCSELs will be presented in this Chapter. In Section 6.1 the temperature-dependent static characteristics are shown, including output power, threshold current, wallplug efficiency, and emission spectra. The temperature-dependent small signal modulation analysis is in Section 6.2. Highly temperature-stable data-transmission results are presented in Section 6.3.

6.1 Temperature-Dependent Static Analysis

Introducing a certain gain-to-etalon wavelength offset into the cavity design can improve the static performance of VCSELs at high temperatures. The calculation results of the static performance for different gain-to-etalon wavelength offset designs have been presented in Chapter 2. In this section, the experimental static results of 980 nm VCSELs with a –15 nm quantum well gain-to-etalon wavelength offset will be presented. These VCSELs are demonstrated to be particularly well suited for temperature-stable operation from 25 to 85 °C.

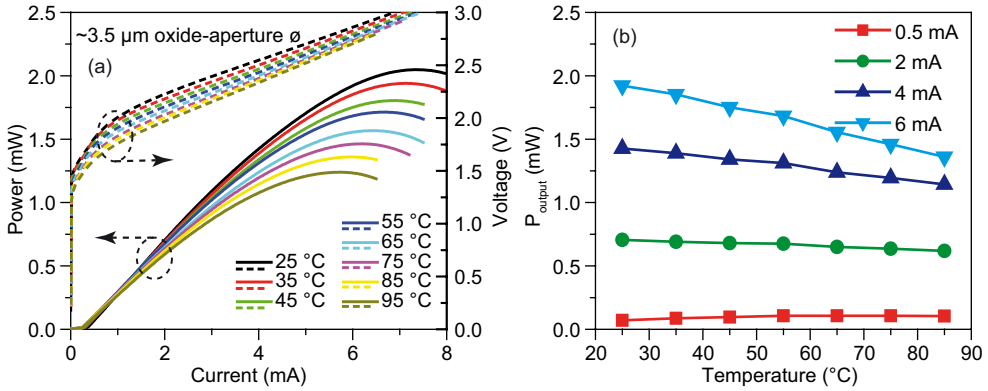

Fig. 6-1. Static L-I-V characteristics at 25 to 95 °C (a) of a ~3.5 µm oxide-aperture diameter 980 nm VCSEL, and the output power versus temperature at different bias currents (b).

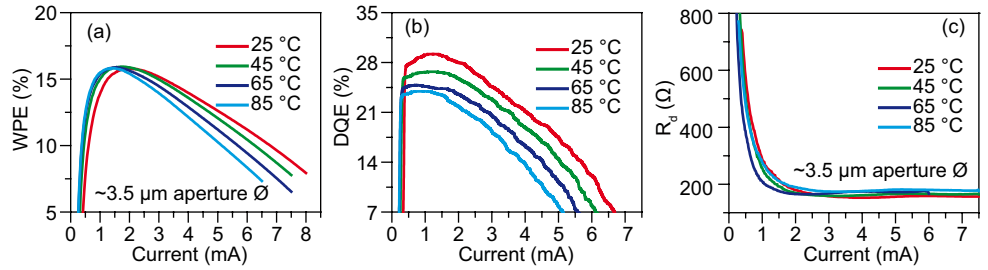

Fig. 6-2. Wall plug efficiency (*WPE*) (a), differential quantum efficiency (*DQE*) (b), and differential resistance (R_d) (c) versus current at 25, 45, 65, and 85 °C for the ~3.5 µm oxide-aperture diameter 980 nm VCSEL.

6.1.1 Temperature-Dependent LIV Results

LIV results between 25 and 95 °C for ~3.5 µm oxide-aperture diameter 980 nm VCSEL are shown in Fig. 6-1(a). The approximate oxide-aperture diameters can be determined with the model described in [139] by measuring the emission spectra. The device has very temperature-stable output power, which is nearly constant for the temperature range from 25 to 95 °C for bias current smaller than 2 mA, as shown in Fig. 6-1(b). The differential quantum efficiency *DQE*, wall plug efficiency *WPE*, and differential resistance R_d change with current. Fig. 6-2 shows the *WPE,DQE*, and R_d versus current at 25, 45, 65, and 85 °C for the ~3.5 µm oxide-aperture diameter 980 nm VCSEL. The *WPE* reaches the maximum value with a current increase then decreases with a further increase of current. This change trend with current is the same for room temperature and high temperature operation. The *WPE* is very temperature-stable, and the maximum values are very close at 25 to 85 °C. The current for maximum *WPE* is smaller at 85 °C than at room temperature. The maximum differential quantum efficiency *DQE* is lower at the high temperature than at room

temperature, and needs a slightly higher current to reach the maximum value at 25 °C. The differential resistance is quite stable with temperature, and only slightly decreases at lower temperature.

Figure 6-3 shows the static parameters extracted from the LIV curves of the ~3.5 µm oxide-aperture diameter 980 nm VCSEL. At 25 °C the threshold current I_{th} is 0.388 mA, and decreases to a minimum value of 0.259 mA at 75 °C, then increases slightly to 0.271 mA at 85 °C, with a relative change of –30 % when the temperature increases from 25 to 85 °C. The measured threshold current reaches a minimum value at around 75 °C, which matches with the QW gain-to-etalon offset design to improve the temperature stability. The threshold voltage U_{th} approximately linearly decreases with temperature and the change is very small, thus the threshold electrical power P_{th} ($P_{th} = I_{th} \times V_{th}$) has a similar change as the threshold current. The maximum output power P_{max} and the rollover current $I_{rollover}$ also approximately linearly decrease with increasing temperature. The maximum optical output power is 2.05 mW at room temperature with a rollover current of 7.36 mA, and reduces

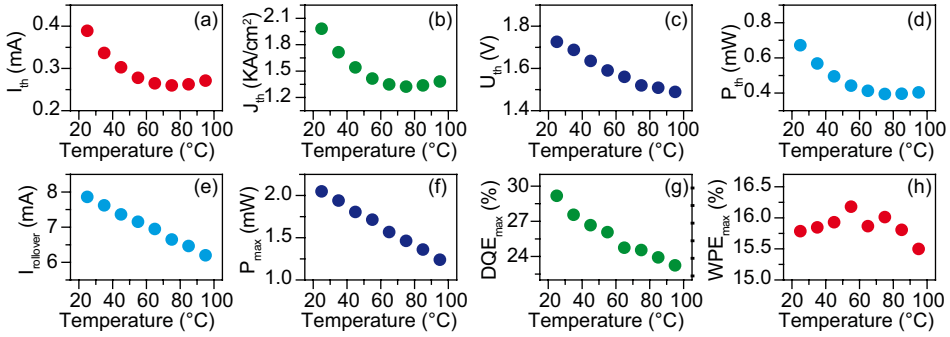

Fig. 6-3. Extracted parameters of the ~3.5 µm oxide-aperture diameter 980 nm VCSEL versus temperature: (a) threshold current I_{th}; (b) threshold current density J_{th}; (c) threshold voltage U_{th}; (d) threshold electrical power P_{th}; (e) rollover current $I_{rollover}$; (f) maximum output power P_{max}; (g) maximum differential quantum efficiency DQE_{max}; and (h) maximum wallplug efficiency WPE_{max}.

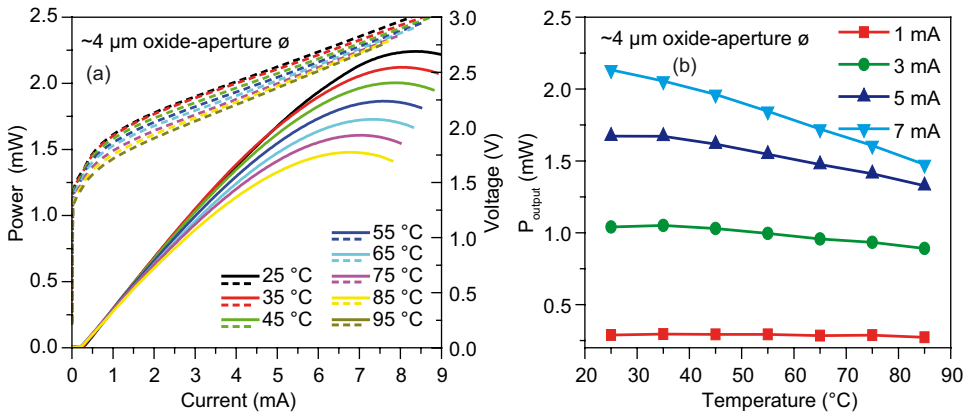

Fig. 6-4. Static LIV characteristics at 25 to 95 °C (a) of a ~4 µm oxide-aperture diameter 980 nm VCSEL, and the output power versus temperature at different bias currents (b).

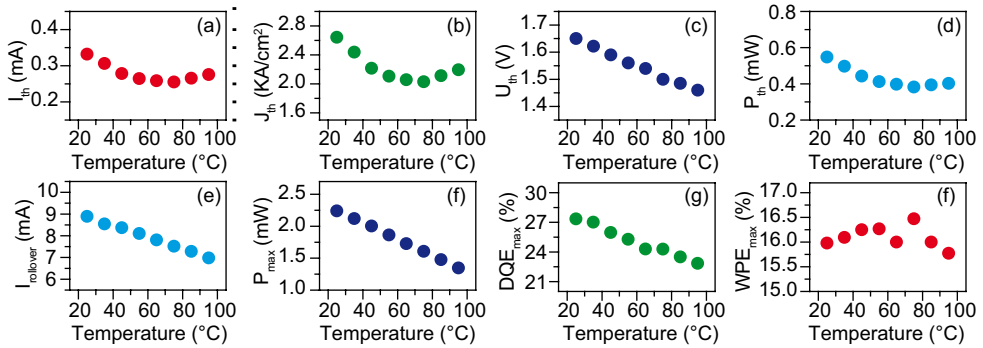

Fig. 6-5. Parameters of the ~4 µm oxide-aperture diameter 980 nm VCSEL versus temperature: (a) threshold current I_{th}; (b) threshold current density J_{th}; (c) threshold voltage U_{th}; (d) threshold electrical power P_{th}; (e) rollover current $I_{rollover}$; (f) maximum output power P_{max}; (g) maximum differential quantum efficiency DQE_{max}; and (h) maximum wallplug efficiency WPE_{max}.

to 1.36 mW with a rollover current of 5.96 mA at 85 °C. The maximum differential quantum efficiency decreases with the temperature increases. The maximum *WPE* is quite stable, and slightly increases with the temperature up to 55 °C, then slowly decreases as the operating temperature further increases.

Fig. 6-4 shows the LIV results for a slightly larger VCSEL with ~4.0 µm oxide-aperture diameter between 25 and 95 °C. The LIV curves are similar to the LIV curves for the ~3.5 µm oxide-aperture diameter VCSEL. The output power is higher due to the larger oxide-aperture diameter. The extracted parameters also show a similar change trend, only with different values. The threshold current I_{th} and threshold electrical power P_{th} decrease with increasing temperature reaching a minimum and then increase in a parabolic shape as shown in Figs. 6-5(a) and 6-5(d). The measured threshold current reaches a minimum value at around 75 °C. At 25 °C the threshold current is 0.33 mA, and decreases to a minimum value of 0.25 mA at 75 °C, then increases slightly to 0.26 mA at 85 °C, with a relatively small change of only −24 % when the temperature increases from 25 to 85 °C.

6.1.2 Spectral Characteristics

Emission spectra are measured to determine the thermal resistance of the 980 nm VCSELs, and to determine the approximate oxide-aperture diameter as mentioned in section 3.3.2. Figure 6-6(a) shows the measured CW emission spectra for the 980 nm VCSEL with an oxide aperture diameter of ~2.5 µm at a fixed forward bias current of 0.4 mA as a function of heat-sink temperature from 25 to 85 °C. Figure 6-6(b) shows the measured CW emission spectra from the same VCSEL at

25 °C as a function bias current from 1 to 6 mA. From the fundamental mode LP01, the cavity etalon resonance wavelength shift rate versus the dissipated power $\Delta\lambda/\Delta P_{diss}$ ($P_{diss} = I \cdot V - P_{opt}$ is the dissipated power, P_{opt} is the optical output power) and the cavity etalon resonance wavelength shift rate versus the heat-sink temperature $\Delta\lambda/\Delta T$ can be obtained, which are 0.367 nm/mW and 0.064 nm/K, respectively, as shown in Fig. 6-7. The thermal resistance R_{th} [100] is then determined to be 5.73 K/mW for the ~2.5 µm oxide-aperture diameter VCSEL. The larger $\Delta\lambda/\Delta P_{diss}$ value of 0.367 nm/mW is the reason of high thermal resistance for the small oxide-aperture diameter VCSEL. Figure 6-8(a) shows the emission intensity of the fundamental mode LP01 and the first higher-order mode LP11 as a function of the bias current for the ~2.5 µm oxide-aperture diameter VCSEL at 25, 35, 45, 65, and 85 °C. The intensity of the fundamental mode is nearly temperature independent, but the intensity of the first higher-order mode decreases with increasing the temperature. The side-mode-suppression-ratios (SMSRs) obtained from the values in Fig. 6-8(a) are shown in Fig. 6-8(b). The SMSR slightly increases as the temperature increases. At 85 °C the SMSR is ~40 dB across the entire current range.

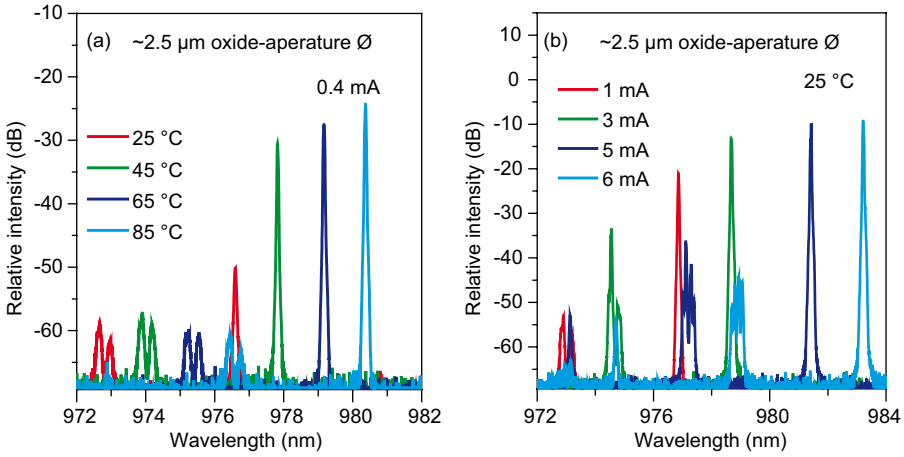

Fig. 6-6. Measured emission spectra (a) at 0.4 mA and at different bias currents (b) at 25 °C for the ~2.5 µm oxide-aperture diameter 980 nm VCSEL.

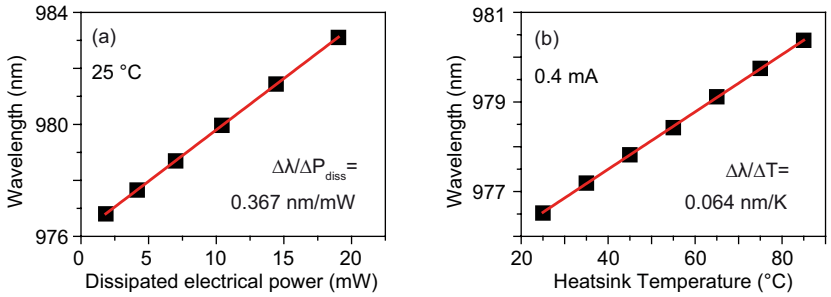

Fig. 6-7. Measured wavelength of the LP01 mode as a function of the dissipated electrical power (a), and as a function of the heat-sink temperature (b) for the ~2.5 µm oxide-aperture diameter 980 nm VCSEL.

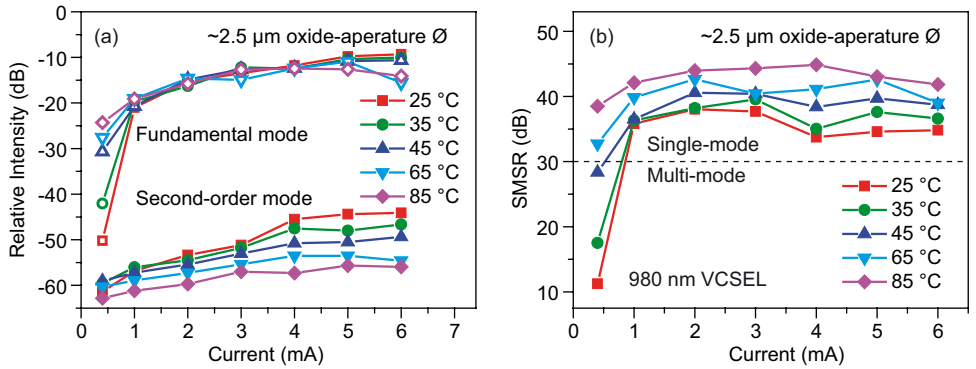

Fig. 6-8. Emission intensities for the fundamental (LP01) and first higher-order (LP11) modes as a function of the bias current (a), and the side-mode-suppression-ratio (SMSR) versus the bias current (b) for the ~2.5 µm oxide-aperture diameter VCSEL at 25, 35, 45, 65, and 85 °C.

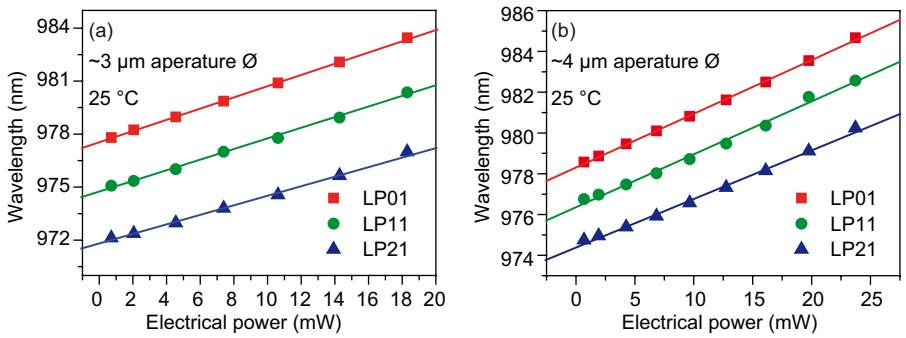

Fig. 6-9. Measured emission wavelengths of the LP01, LP11, and LP21 modes against applied electrical power at 25 °C for ~3 µm (a) and ~4 µm (b) oxide-aperture diameters 980 nm VCSELs. The cold cavity wavelengths are determined by extrapolating the measured results to 0 mW.

The measured LP01, LP11, and LP21 peak wavelengths as a function of the forward bias electrical power P_{el} $(I \cdot V)$ are plotted in Fig. 6-9 for ~3 and ~4 µm oxide-aperture diameter VCSELs. The wavelengths of the modes toward zero electrical power (no heating) are extrapolated by fitting the data with a straight line, and the resultant wavelengths at zero electrical power are called the "cold cavity modes". The measured cold cavity optical emission wavelengths for the LP01, LP11, and LP21 modes as a function of oxide-aperture diameter from ~2.5 to 7.0 µm for the 980 nm VCSELs are shown in Fig. 6-10(a). The VCSEL resonant wavelength shifts to the shorter wavelength as the oxide-aperture diameter decreases. As the oxide-aperture diameter increases beyond about 10 µm the peak wavelengths of the LP01, LP11, and LP21 modes reach a constant value. In Fig. 6-10(b) the mode spacing between the fundamental mode LP01 and the first higher-order mode LP11 is shown as a function of the oxide-aperture diameter. The small oxide-aperture diameter VCSELs have a larger mode spacing, which is beneficial for a low single-mode emission threshold current [139].

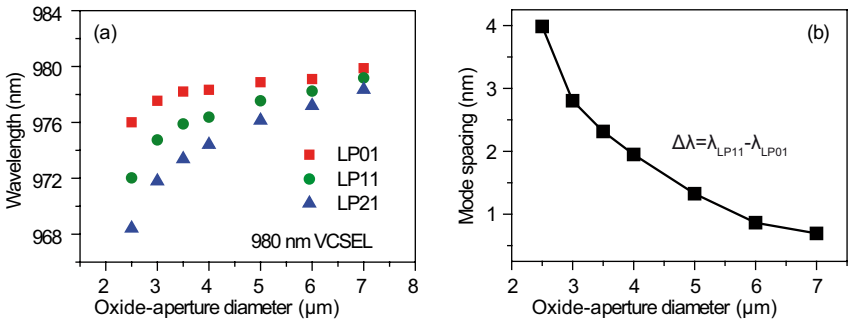

Fig. 6-10. Measured cold cavity emission wavelengths [107] (a) for the LP01, LP11, and LP21 modes; and (b) measured mode spacing between the fundamental mode LP01 and second order mode LP11 as a function oxide-aperture diameter for 980 nm VCSELs.

6.2 Small-Signal Modulation Analysis

To understand how temperature affects the high bit-rate modulation performance of VCSELs, the temperature-dependent small-signal analysis is performed. In Fig. 6-11, the measured small-signal modulation response curves with corresponding fittings are shown for different currents at 25, 45, 65, and 85 °C for the ~4 μm oxide-aperture diameter VCSEL. All the fittings match very well with the measurement data. The −3 dB bandwidth is an important parameter to determine the high-speed capability of VCSELs, since it is generally directly related to the maximum achievable bit rate. The −3 dB bandwidth increases with increasing the current, and eventually saturates and decreases. The −3 dB bandwidth decreases typically due to thermal limitations. The change of −3 dB bandwidth with the current at high temperatures is the same as at room temperature, and high values of $f_{-3\mathrm{dB}}$ can be achieved over a large range of temperatures. 4 and 5.4 mA are taken as typical currents to show the influence of the temperature on the high-speed modulation performance. The measured small-signal modulation response curves with the corresponding fittings at the bias currents of 4 and 5.4 mA at 25, 45, 65, and 85 °C for the ~4 μm oxide-aperture diameter VCSEL are shown in Fig. 6-12. The modulation response is very temperature-stable. For the bias current of 4 mA, the modulation response stays nearly the same when the temperature increases from room temperature to high temperatures. For the 5.4 mA bias current, the −3 dB bandwidth is 20.5, 20.7, 19.6, and 18.3 GHz at temperatures of 25, 45, 65, and 85 °C, respectively, with a small change of only 2.2 GHz when the temperature increases from 25 to 85 °C.

Fig. 6-13(a) plots the −3 dB bandwidth versus the bias current for temperatures of 25, 45, 65, and 85 °C for the ~4 μm oxide-aperture diameter 980 nm VCSEL. The plot shows that the VCSELs can achieved higher bandwidths at 85 °C compared to 25 °C for currents smaller than 3 mA. The $f_{-3\mathrm{dB}}$ is higher at 25 °C than at higher

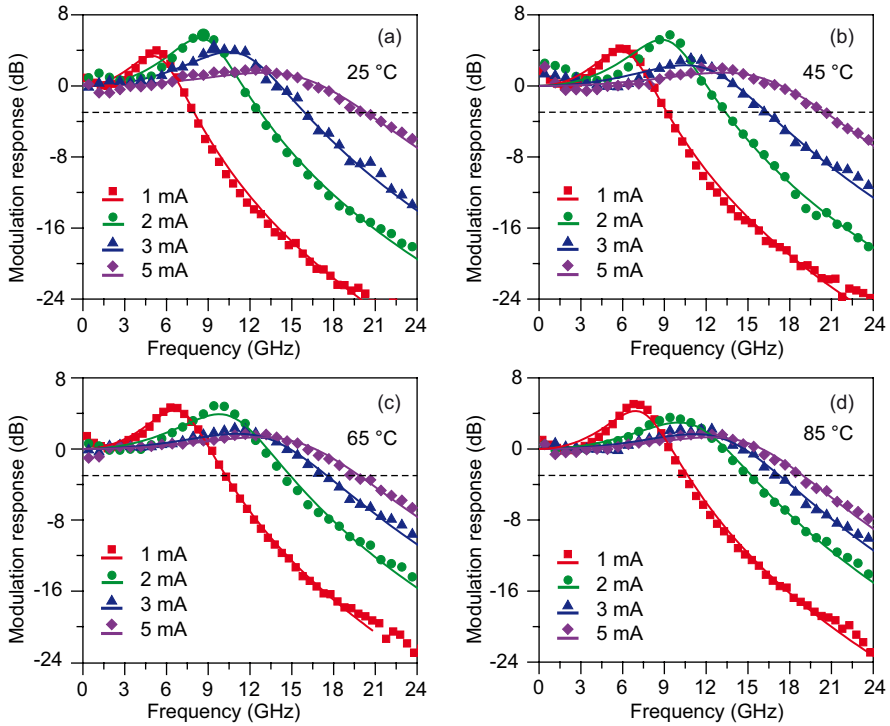

Fig. 6-11. Magnitude of the small signal modulation response S21 for bias currents of 1, 2, 3, 5 mA and corresponding fittings at 25 °C (a), 45 °C (b), 65 °C (c), and 85 °C (b) for the ~4 μm oxide-aperture diameter VCSEL.

temperatures for currents above ~4 mA, where thermal effects introduced by Joule heating lead to a reduced f_{-3dB} at a given current. The f_{-3dB} is nearly constant at ~18 GHz at 85 °C for currents larger than 3.7 mA, and larger than 18 GHz at lower temperatures. A nearly temperature-independent high bit-rate over a large current range is possible. For example, 38 Gb/s error-free transmission is achieved at currents above 3.7 mA without a change in the bias current or in the voltage modulation conditions from 25 to 85 °C. The extracted relaxation resonance frequency f_r shows a similar change trend versus the temperature as f_{-3dB}, as shown in Fig. 6-13(b), in which a reverse point at 4.5 mA, where f_r at 25 °C starts to exceed the value at 85 °C, can be seen clearly. For large bias current (> 5 mA), the f_r is higher at room temperature than at higher temperatures. This is different with low current, but still reasonable. The differential gain increases with increasing active region temperature until it reach a maximum value at around 360 K (~87 °C) then starts to decrease with further temperature increases due to the –15 nm QW gain-to-etalon wavelength offset design. The active region temperature depends on the ambient temperature, and increases with the bias current. At an ambient temperature of 25 °C, a bias current of 5 mA leads to an active region temperature of 82.1 °C (355.25 K), close to the maximum differential gain value. For a higher ambient temperature of 85 °C the same bias current results in a much higher active region temperature of 142.1 °C

(415.25 K), leading to a lower differential gain compared to the value at 25 °C. Therefore, at large bias currents higher relaxation resonance frequencies can be reached at room temperature than at higher temperatures.

For applications in optical data communications, it is of much interest to obtain high modulation bandwidths at small operating currents to reduce the energy consumption. The *D*-factor describes how fast the relaxation resonance frequency f_r increases with increasing bias current above the threshold current. A large *D*-factor implies the VCSEL can reach a large f_r at low bias currents. The *D*-factor can be obtained from the linear dependence of the relaxation resonance frequency versus the square root of current above threshold at low currents, where the increase of the active region temperature due to the self-heating is small. The modulation current efficiency factor *MCEF* specifies the increase of f_{-3dB}, which can be obtained by the linear dependence of f_{-3dB} on the square root of current above threshold at low currents. The extracted relaxation resonance frequencies f_r versus the square root of the bias current minus the threshold current and the corresponding linear fittings for the

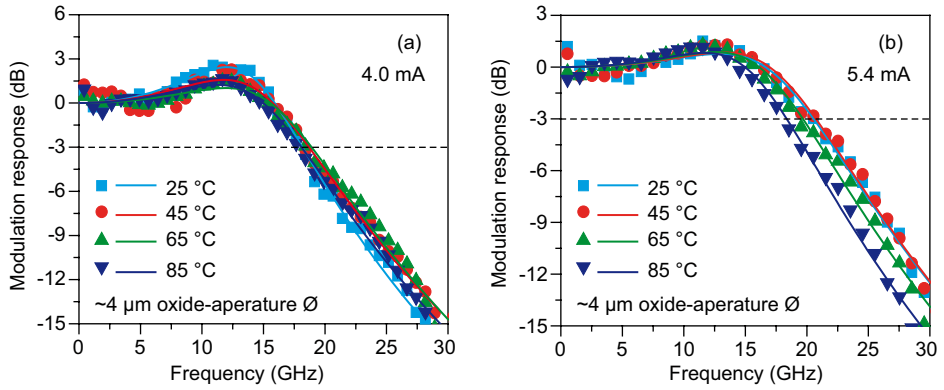

Fig. 6-12. Magnitude of the small signal modulation response S21 and corresponding fittings at bias currents of 4 mA (a) and 5.4 mA (b) at 25, 45, 65, and 85 °C for the ~4 µm oxide-aperture diameter VCSEL.

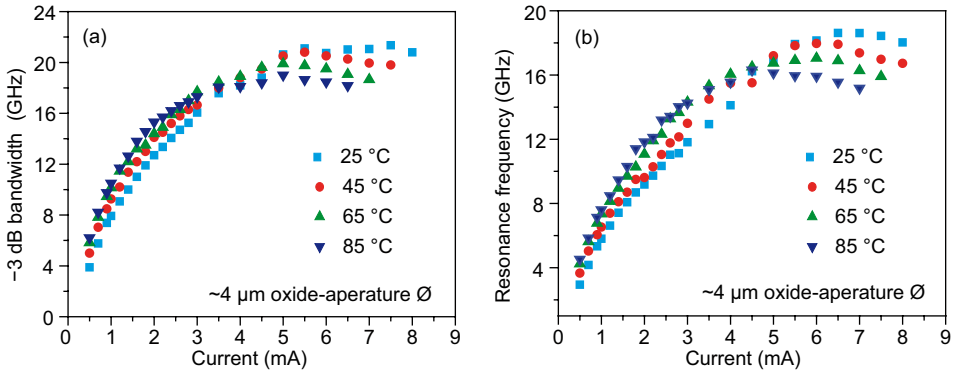

Fig. 6-13. f_{-3dB} (a) and f_r (b) extracted from small-signal modulation response measurements at different bias currents for the ~4 µm oxide-aperture diameter 980 nm VCSEL at 25, 45, 65 and 85 °C.

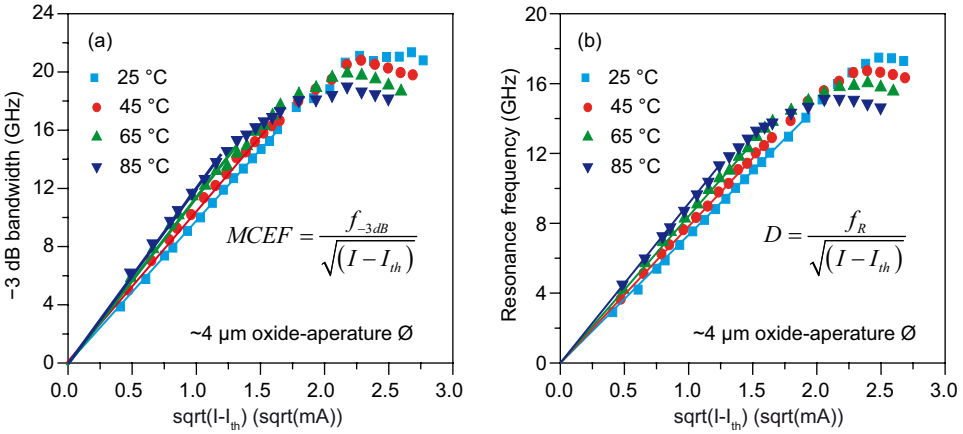

Fig. 6-14. –3 dB bandwidth (a) and relaxation resonance frequency (b) versus the square root of the bias current minus the threshold current for the ~4 μm oxide-aperture diameter VCSEL at 25, 45, 65 and 85 °C.

980 nm VCSELs are shown in Fig. 6-14(b). These curves are different from what is typically observed, since the *D*-factor is larger at 85 °C compared to the value at 25 °C. High-speed and energy-efficient operation from room temperature to 85 °C can be achieved due to the stable and large *D*-factor. The extracted f_{-3dB} versus the square root of the bias current minus threshold current and the corresponding linear fittings are shown in Fig. 6-14(a), showing the *MCEF* data is similar to the *D*-factor data, but with higher values.

6.3 Highly Temperature-Stable VCSELs

The data transmission measurements are carried out at various bit rates and heat-sink temperatures. To demonstrate the VCSELs are highly temperature-stable, data transmission tests are performed at a fixed bit rate, bias, and modulation conditions. Figure 6-15(a) shows that the error-free data transmissions at 35 Gb/s at 25 up to 85 °C are achieved at the same bias and modulation conditions by using a ~3 μm oxide-aperture diameter VCSEL. The CW bias currents used for these measurements are all 2.7 mA, and the modulation conditions with a peak-to-peak amplitude of 470 mV are used over the entire measured temperature range. With a little increase of bias current to 2.9 mA, 38 Gb/s error-free data transmissions at 25 up to 85 °C at the same bias and modulation conditions are realized using the same VCSEL, as shown in Fig. 6-15(b).

In Fig. 6-16, 38 Gb/s error-free data transmission at 25 up to 85 °C are shown by using a slightly larger oxide-aperture diameter (~3.5 μm) VCSEL without any changes in bias and modulation conditions. The CW bias current is 3.5 mA, which is

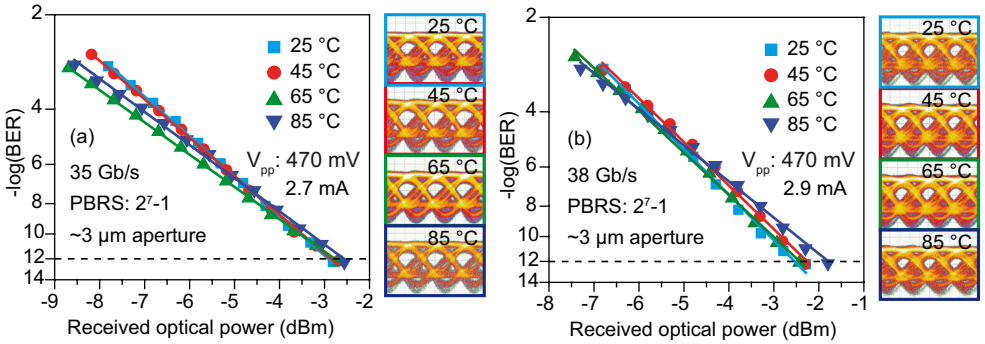

Fig. 6-15. Bit error ratio versus received optical power for a ~3 µm oxide-aperture diameter 980 nm VCSEL operating at 35 Gb/s (a) and 38 Gb/s (b) at 25, 45, 65 and 85 °C, respectively, and eye diagrams at the corresponding temperatures and modulation conditions.

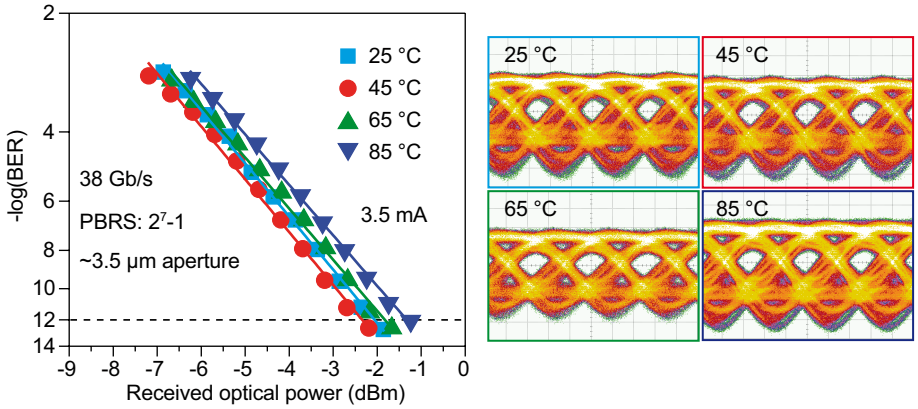

Fig. 6-16. Bit error ratio versus received optical power for an ~3.5 µm oxide-aperture diameter 980 nm VCSEL operating at 38 Gb/s at 25, 45, 65 and 85 °C, respectively, and eye diagrams at the corresponding temperatures and modulation conditions.

a little higher than the bias current used for the same bit-rate operation of the smaller oxide-aperture diameter (~3 µm) VCSEL, and the modulation conditions with a peak-to-peak amplitude of 470 mV are used over the entire temperature range. For a ~4 µm oxide-aperture diameter VCSEL, the error-free operation at 35 Gb/s at 25, 45, 65, and 85 °C are shown in Fig. 6-17(a). The bias current used for these four measurements is 3.2 mA. Also the error-free operation at 38 Gb/s at 25, 45, 65, and 85 °C by using a bias current of 5.4 mA and a modulation condition with a peak-to-peak amplitude of 380 mV, are shown in Fig. 6-17(b). It is found that up to the temperature of 65 °C no penalty of received optical power occurs. Figures 6-15, 6-16 and 6-17 show that very temperature-stable data transmission can be achieved by using small oxide-aperture VCSELs (with oxide-aperture diameters of 3 − 4 µm). Even smaller oxide VCSELs, for example ~2.5 µm oxide-aperture diameter VCSELs, are also not beneficial for temperature-stable data transmission tests due to their small optical output power, large differential resistance, and large thermal resistance (high active region temperature).

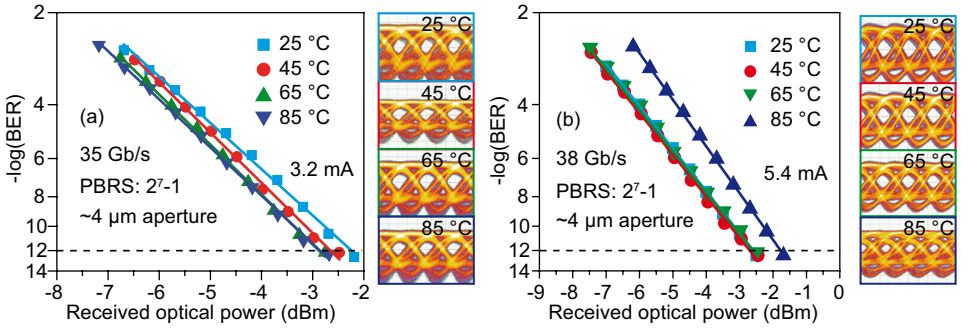

Fig. 6-17. Bit error ratio versus received optical power for a ~4 µm oxide-aperture diameter 980 nm VCSEL at 35 Gb/s (a) and 38 Gb/s (b) at 25, 45, 65 and 85 °C, respectively, and eye diagrams at the corresponding temperatures and modulation conditions.

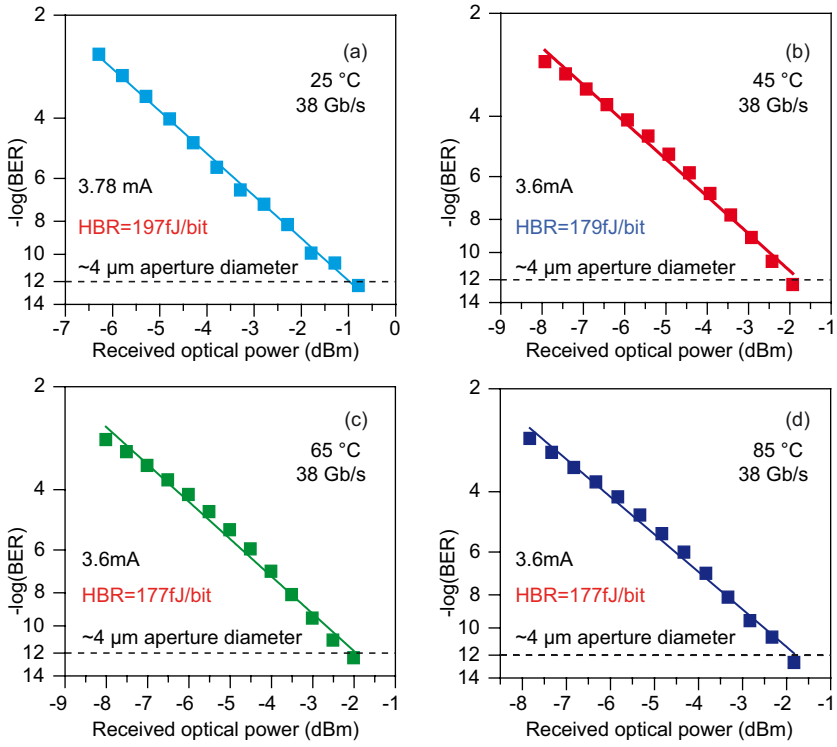

Fig. 6-18. BER versus received optical power for the ~4 µm oxide-aperture diameter 980 nm VCSEL operating at 38 Gb/s at the bias currents that yield the maximum energy efficiency at 25 °C (a), 45 °C (b), 65 °C (c), and 85 °C (d).

Figure 6-18 shows the BER versus received optical power for a ~4 µm oxide-aperture diameter VCSEL operating at 38 Gb/s at the bias currents yielding the maximum energy-efficiency at different temperatures. The corresponding eye diagrams are shown in Fig. 6-19(a). The error-free operation at 38 Gb/s is achieved with low HBR values of 197, 179, 177, and 177 fJ/bit at 25, 45, 65, and 85 °C, respectively. The corresponding EDR values are 231, 211, 207, and 203 fJ/bit, respectively. The CW bias current used at 25 °C for the BER measurements is 3.78 mA (at a corresponding voltage of 2.33 V), and the CW bias current is 3.6 mA for the BER measurements at

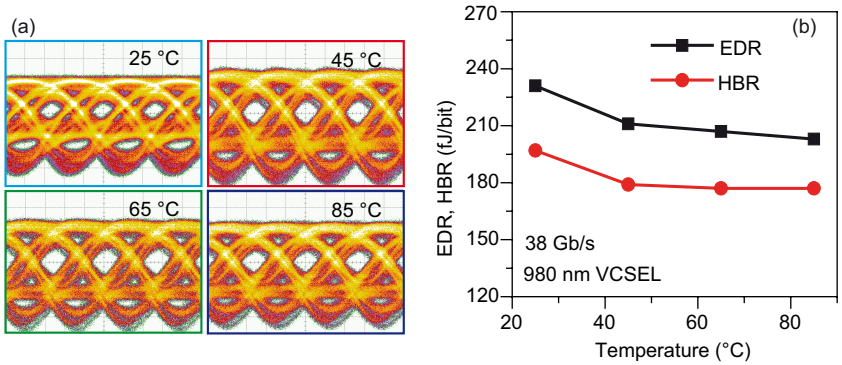

Fig. 6-19. Eye diagrams for the ~4 µm oxide-aperture diameter 980 nm VCSEL operating at 38 Gb/s at the bias currents yielding the maximum energy-efficiency at 25, 45, 65, and 85 °C (a), and the minimum electrical energy-to-data ratio EDR and heat-to-bit rate ratio HBR change with temperature (b).

45, 65, and 85 °C with voltages of 2.23, 2.19 and 2.14 V, respectively. Both the HBR and EDR values are highly temperature-stable, as show in Fig. 6-19(b). Besides these highly temperature-stable static properties and high-speed modulation properties, the modulation bandwidth, data transmission bit rate, and energy dissipation also show high temperature stability, which are all beneficial for the use of these VCSELs in optical interconnect applications.

6.4 Summary

In this Chapter the experimental results of the highly temperature-stable 980 nm VCSELs are presented. Systematic characterizations including static measurements, small-signal analysis, and data transmission experiments are carried out. The error-free data transmissions at bit rates of 38 Gb/s at 25, 45, 65, and 85 °C are demonstrated without any change of the operating point or the modulation conditions. The VCSELs demonstrate very temperature-insensitive static and dynamic characteristics. The superior results are attributed to the employment of InGaAs QWs and GaAsP barrier layers, and the −15 nm gain-to-etalon wavelength offset.

Chapter 7

Energy-Efficient High Bit-Rate VCSELs

The increasing demand for optical communication can only be met by the realization of ever more energy-efficient emitters with increased bandwidth and thus higher information capacity via faster modulation capabilities. Exascale supercomputers will require billions of optical interconnects and are predicted to require high-speed interconnects operating at least at 25 Gb/s before 2020 [28, 140], thus the VCSELs within the optical interconnect (OI) systems and links must operate at high bit-rates with a low energy consumption. A maximum energy dissipation of ~100 fJ/bit is predicted for VCSELs used for OIs by circa 2015 [56]. The experimental results of energy efficient high bit-rate 980 nm VCSELs will be presented in this Chapter. Section 7.1 shows the oxide-aperture diameter-dependent static characteristics. The oxide-aperture diameter-dependent small-signal modulation analysis at room temperature and high temperature will be presented in Section 7.2 and 7.3. The energy efficient high bit-rate results at room temperature and at high temperature are presented in this Chapter as well.

7.1 Static Characteristics

In this section, detailed static results at 25 and 85 °C for VCSELs with oxide-aperture diameters ranging from ~2.5 to 7 µm are given. The continuous wave (CW) figures-of-merit are extracted and the change of these parameters with changing oxide-aperture diameter is discussed. It is demonstrated that the –15 nm quantum well gain-to-etalon wavelength offset allows the VCSELs to operate well at room temperature and also at high temperatures up to 85 °C.

7.1.1 Static LIV Characteristics

Static LIV measurement results at room temperature (25 °C) and at high temperature (85 °C) for the 980 nm VCSELs with oxide-aperture diameters ranging from ~2.5 to 7 µm are shown in Fig. 7-1. The LIV curves are similar at room temperature and high temperature. The significant difference is that the output power at 85 °C is lower. The threshold currents and rollover currents are also changed with changing temperature. The extracted parameters at room temperature for VCSELs with oxide-aperture diameter ranging from ~2.5 to ~7 µm are shown in Fig. 7-2. The threshold current I_{th} increases with increasing oxide-aperture diameter, and is 0.38, 0.33, 0.33, 0.40, 0.54, and 0.77 mA for ~2.5, 3, 4, 5, 6, and 7 µm oxide-aperture diameter VCSELs, respectively. The smallest I_{th} of 0.33 mA is achieved with oxide-aperture diameters of ~3 and 4 µm. The smaller (< 3 µm) oxide-aperture diameter VCSELs have higher I_{th} at 25 °C due to several opposing interacting parameters including modal gain, cavity losses, gain-to-etalon wavelength offset, and other factors. As the oxide-aperture

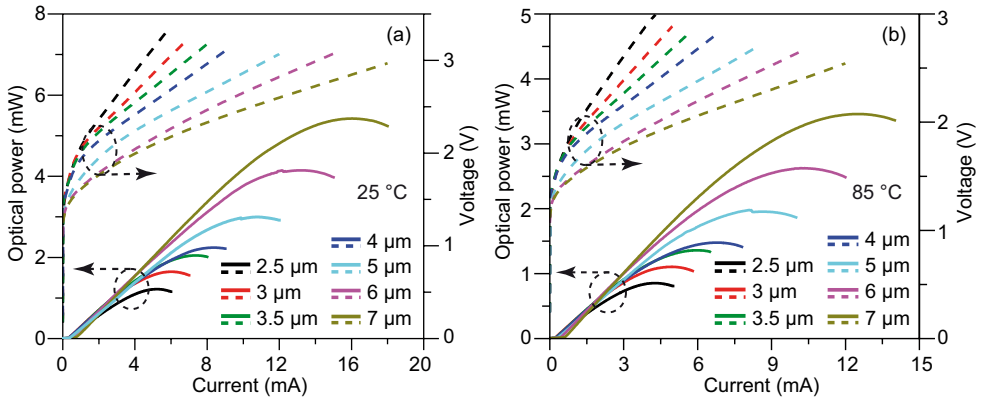

Fig. 7-1. Measured CW L-I-V characteristics for the 980 nm VCSELs with oxide-aperture diameters ranging from ~2.5 to ~7 µm at 25 °C (a) and 85 °C (b).

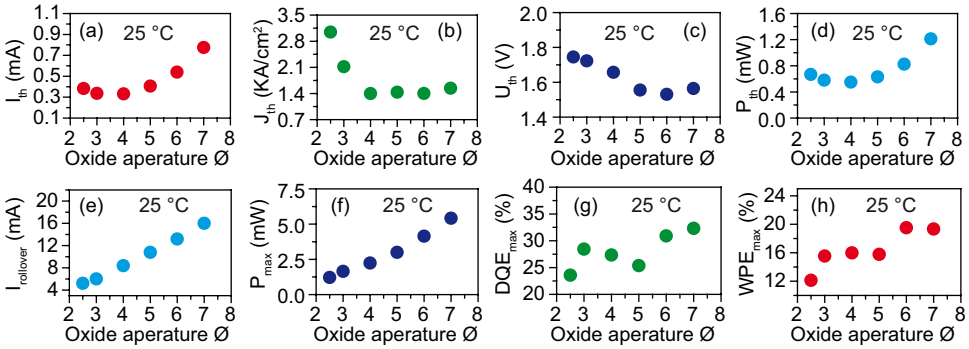

Fig. 7-2. Threshold current I_{th} (a), threshold current density J_{th} (b), threshold voltage U_{th} (c), threshold electrical power P_{th} (d), rollover current $I_{rollover}$ (e), maximum output power P_{max} (f), maximum differential quantum efficiency DQE_{max} (g), and maximum wall-plug efficiency WPE_{max} (h) versus oxide aperture diameter for ~2.5 to ~7 µm 980 nm VCSELs at 25 °C.

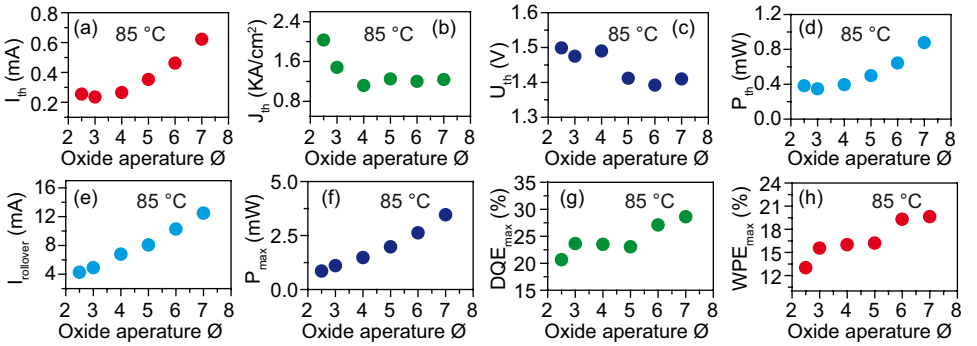

Fig. 7-3. I_{th} (a), J_{th} (b), U_{th} (c), P_{th} (d), $I_{rollover}$ (e), P_{max} (f), DQE_{max} (g), and WPE_{max} (h) versus oxide aperture diameter for ~2.5 to 7 µm 980 nm VCSELs at 85 °C.

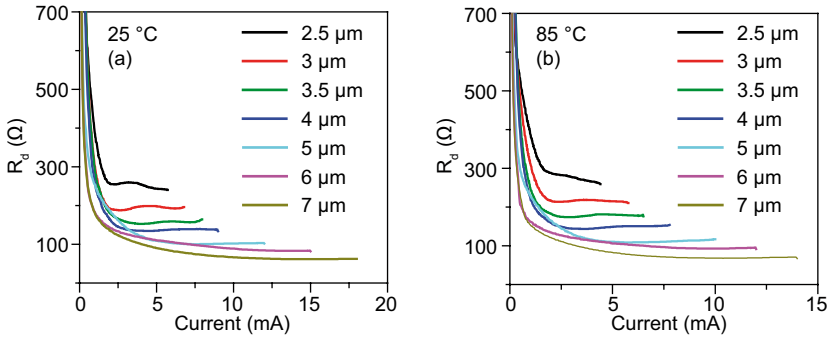

Fig. 7-4. Differential resistance (R_d) versus current for the 980 nm VCSELs with oxide-aperture diameters ranging from ~2.5 to ~7 µm at 25 °C (a) and 85 °C (b).

diameters increase beyond ~4 µm there is a noticeable increase in the threshold current as a function of the oxide-aperture diameter, because the lasing area of the VCSEL is increasing with the aperture diameter and a larger current is required to achieve the lasing threshold, even as the scattering and other optical losses become less significant. For VCSELs with small oxide-aperture diameters (from ~2.5 to 4 µm), the quite stable low threshold current I_{th} is beneficial for the energy efficient operation. The threshold electrical power P_{th} has the similar change with I_{th}. The rollover current and maximum output power nearly linearly increase with increasing oxide-aperture diameter. The maximum optical output power is 1.22 mW for the ~2.5 µm oxide-aperture diameter VCSEL with a rollover current of 5.21 mA, and increases to 5.42 mW with a rollover at 16.01 mA for the ~7 µm oxide-aperture diameter VCSEL. The maximum differential quantum efficiency DQE_{max} is 23.58 % for the ~2.5 µm oxide-aperture diameter VCSEL, and increase to 28.45 % for the ~3 µm oxide-aperture diameter VCSEL. The DQE_{max} reaches a value of 32.32 % at the oxide-aperture diameter of ~7 µm. The maximum WPE_{max} has a similar trend as the differential quantum efficiency. The WPE_{max} is 12.13 % for the ~2.5 µm oxide-aperture diameter VCSEL, and increases to 15.53 % for the ~3 µm oxide-aperture diameter VCSEL. The WPE_{max} remains about constant for apertures from ~3 to

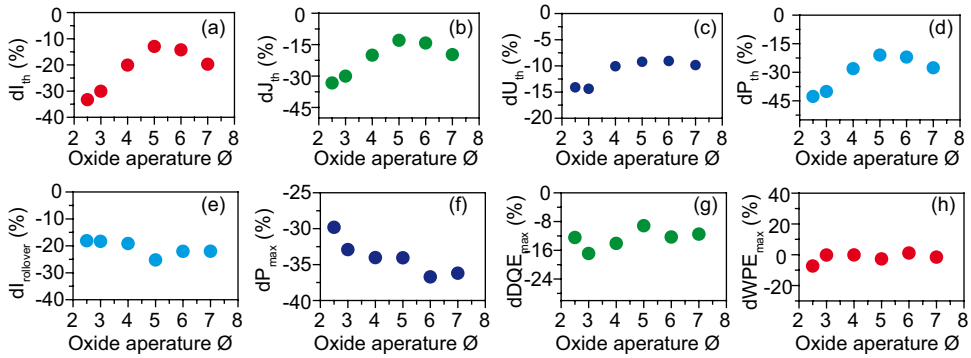

Fig. 7-5. Relative change of I_{th} (dI_{th}) (a), relative change of J_{th} (dJ_{th}) (b), relative change of U_{th} (dU_{th}) (c), relative change of P_{th} (dP_{th}) (d), relative change of P_{max} (dP_{max}) (f), relative change of $I_{rollover}$ ($dI_{rollover}$) (e), relative change of WPE_{max} ($dWPE_{max}$) (h), and relative change of DQE_{max} ($dDQE_{max}$) (g) with a temperature increase from 25 to 85 °C for VCSELs with oxide-aperture diameters ranging from ~2.5 to ~7 µm.

~5 µm, then increases to 19.33 % for the ~7 µm VCSEL. Thus the small aperture VCSELs (~2.5 to 5 µm) have small I_{th}, and small P_{th}, which are both beneficial for the energy efficient operation. However, the output power of the small aperture VCSELs is small, resulting in small WPE_{max} and DQE_{max} values. For larger oxide-aperture diameter VCSELs (larger than ~5 µm), the WPE_{max} and DQE_{max} are larger, but also have large I_{th} and P_{th} values, which will increase the energy consumption.

The extracted parameters at 85 °C for VCSELs with oxide-aperture diameters ranging from ~2.5 to 7 µm are shown in Fig. 7-3. The I_{th} increase with increasing the oxide aperture, which is 0.25, 0.23, 0.26, 0.35, 0.46, and 0.62 mA for the ~2.5, 3, 4, 5, 6, and 7 µm oxide-aperture diameter VCSELs, respectively. I_{th} is lower than at 25 °C for all devices of a given size. The changing of I_{th} and P_{th} with the aperture diameter corresponds to the behavior at room temperature. These two parameters are nearly constant for the small oxide-aperture diameters (~2.5 to 4 µm) but increase for the larger oxide-aperture diameter VCSELs. The $I_{rollover}$ and P_{max} increase linearly as the oxide-aperture diameter increases. The P_{max} is 0.85 mW for the ~2.5 µm oxide-aperture diameter VCSEL with $I_{rollover}$ of 4.2 mA, and increases to 3.45 mW at 12.4 mA for the ~7 µm oxide-aperture diameter VCSEL, respectively. The DQE_{max} is 20.6 % for the ~2.5 µm aperture VCSEL, and increases to 23.6 % for the ~3 µm aperture VCSEL. The DQE_{max} remains quite stable until ~5 µm when it increases to 28.6 % at ~7 µm. The WPE_{max} and DQE_{max} behave similarly. As at 25 °C, the small oxide-aperture diameter VCSELs (~3 to 5 µm) have small I_{th} and P_{th} values quite high WPE_{max} and DQE_{max} values. The smallest VCSELs (~2.5 µm) have small I_{th} and P_{th}, but the P_{opt} is very small, as are the WPE_{max} and the DQE_{max}, which limit the VCSELs' high-speed operation at 85 °C. From a static analysis, it is found that VCSELs with oxide-aperture diameters between ~3 and ~4 µm are best suited for energy-efficient and high bit-rate operation at 85 °C. Differential resistance (R_d) versus current for

the VCSELs with oxide-aperture diameter from ~2.5 to 7 µm at 25 and 85 °C are shown in Fig. 7-4. Small oxide-aperture diameter VCSELs have larger differential resistance R_d, which is not favorable for matching the input impedance of the VCSEL to the 50 Ω impedance of a standard radio frequency transmission line. The differential resistance R_d decreases with increasing oxide-aperture diameter.

The relative change of I_{th} (dI_{th} = ((I_{th} (85 °C) − I_{th} (25 °C)) / I_{th} (25 °C)) · 100 %) for ~3, 4, 5, 6, and 7 µm oxide-aperture diameter VCSELs is shown in Fig. 7-5(a). The P_{th} (Fig. 7-5(d)) follows the trend of I_{th}. The I_{th} and P_{th} are temperature-stable for all VCSELs, due to around –15 nm QWs gain-to-etalon wavelength offset at room temperature [141]. For VCSELs with a smaller gain-etalon wavelength offset [142], the P_{th} increase with increasing temperature and the relative change is as high as 30 % to 60 % for VCSELs with oxide-aperture diameter from ~2.5 to 7 µm. The VCSELs with smaller oxide-aperture diameters generally have the smallest relative change with a temperature increase. For the structure in this work, the P_{th} decreases with a temperature increase with a relative change of only between –42 % to –27 %. In this case, the ~5 µm oxide-aperture diameter VCSEL has the smallest relative change.

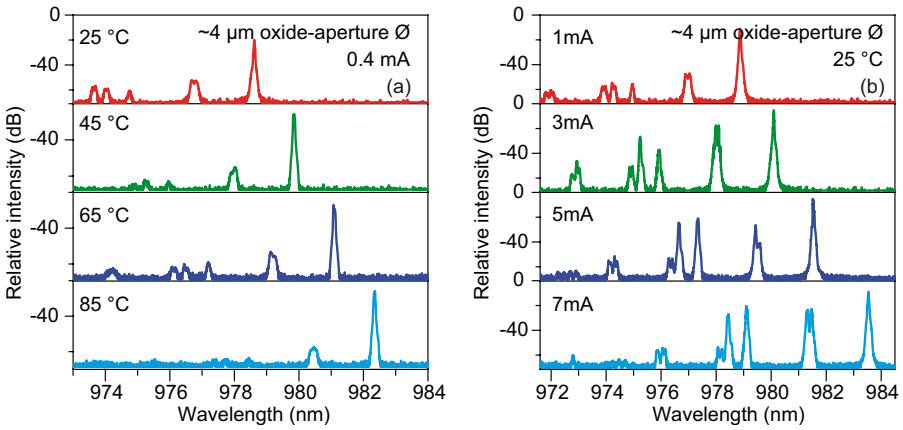

Fig. 7-6. Measured emission spectra (a) at 0.4 mA at different heat-sink temperatures and (b) at 25 °C at different bias currents for the ~4 µm oxide-aperture diameter 980 nm VCSEL.

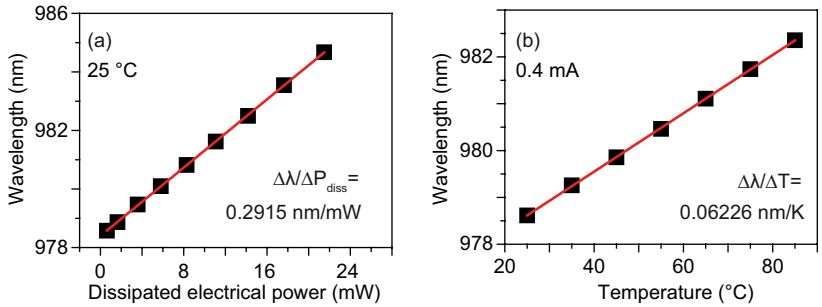

Fig. 7-7. Measured emission wavelength (fundamental mode) versus (a) dissipated electrical power and (b) heat-sink temperature for the ~4 µm oxide-aperture diameter 980 nm VCSEL.

7.1.2 Spectral Characteristics

Measurements of emission spectra are carried out for the ~4 µm oxide-aperture diameter VCSEL at different bias currents and different temperatures. The measured CW emission spectra at a fixed forward bias current of 0.4 mA as a function of heat-sink temperature from 25 to 85 °C are shown in Fig. 7-6(a), and the measured CW emission spectra at 25 °C as a function bias current from 1 to 7 mA are shown in Fig. 7-6(b). The cavity etalon resonance wavelength shift rate versus the dissipated power $\Delta\lambda/\Delta P_{diss}$, and versus heat-sink temperature $\Delta\lambda/\Delta T$ are 0.292 nm/mW and 0.062 nm/K, respectively, giving a thermal resistance $R_{th} = \Delta T/\Delta P_{diss}$ [100] of 4.68 K/mW for the ~4 µm oxide-aperture diameter VCSEL.

Optical spectral measurements following the same evaluation procedure are performed for different oxide-aperture diameter VCSELs. The cavity resonance wavelengths change with the dissipated power for VCSELs with oxide-aperture diameter ranging from ~2.5 to ~7 µm are shown in Fig. 7-8(a). The cavity resonance wavelengths shift faster for small oxide-aperture diameter VCSELs than larger ones, as shown in Fig. 7-9(a). The cavity resonance wavelength changes with heat sink

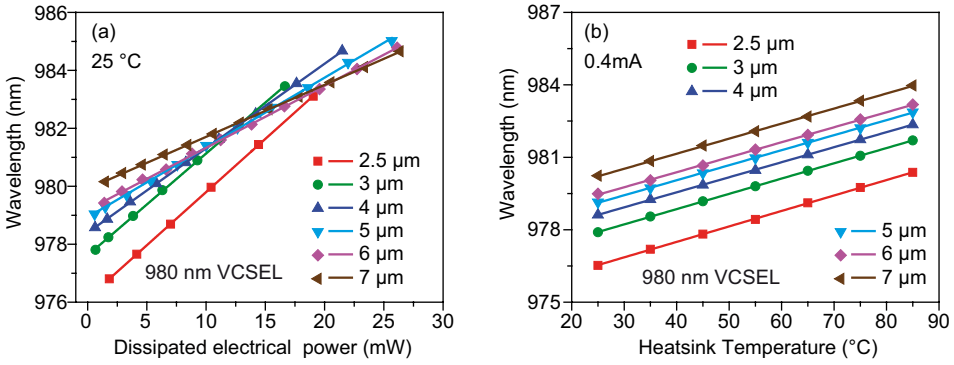

Fig. 7-8. Measured emission wavelength as a function of the dissipated power and (b) measured emission wavelength as a function of heat-sink temperature for 980 nm VCSELs.

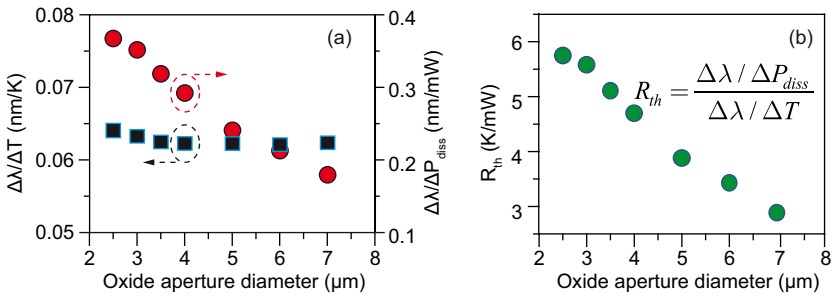

Fig. 7-9. Measured shift rate of cavity resonance wavelength with dissipated electrical power and with heat sink temperature (a), and the calculated thermal resistance (b) for 980 nm VCSELs.

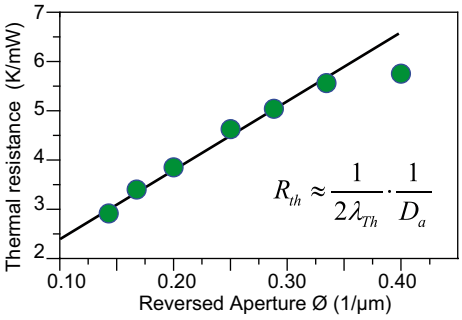

Fig. 7-10. Measured thermal resistance as a function of inverse oxide-aperture diameter ($1/D_a$) for 980 nm VCSELs.

temperature are shown in Fig. 7-8(b). The lines are nearly parallel, which means the cavity resonance wavelength shift rates with heat sink temperature are nearly independent of oxide-aperture diameter. The thermal resistances are calculated by using the data in Fig. 7-9(a), and the results are shown in Fig. 7-9(b). The smaller oxide-aperture diameter VCSELs have a large thermal resistance compared with larger VCSELs, which matches well with the thermal model [26, 143] and the simulation results shown in Chapter 2.

The heat flow inside the VCSEL can be approximated as a disk heat source on an isotropic, semi-infinite substrate. This model gives a simple relation for the thermal resistance [26, 143], by assuming the heat flow from a circular area with diameter D_a (equal to the oxide-aperture diameter) into a half-space filled with medium of thermal conductivity λ_{Th} (in W/cm·K):

$$R_{th} \approx \frac{1}{2\lambda_{Th}} \cdot \frac{1}{D_a} \text{ (K/mW)} \tag{7.1}$$

Figure 7-10 is a plot of the thermal resistance as a function of inverse oxide-aperture diameter using the measured data in Fig. 7-9(b). Using the data in Fig. 7-10 and Equation (7.1) the thermal conductivity λ_{Th} can be obtained from the slope of the linear fitting of the data, which is ~0.41 W/cm·K. This value is comparable to the published values of other groups [73, 144]. Various methods have been tried to increase the thermal conductivity. Thermal conductivity can be increased from 0.41 to 0.53 W/cm·K by using 2 μm of Cu-plating on the VCSEL [144]. Thermal resistance can be reduced by another factor of 2 by using a Au-plated heat spreading layer [145]. Oxide-free lithographic VCSELs have also been that thermal resistance can be further reduced [146].

The active region temperature T_{active} change with increasing operating bias current can be estimated for the linear LI region using $T_{active} = T_{ambient} + R_{th} \times (I \times V - P_{out})$ [100], as shown in Fig. 7-11. The active region temperature is much higher than $T_{ambient}$, and small oxide-aperture diameter VCSELs suffer higher T_{active} for the same bias current compared with larger VCSELs due to their larger thermal resistance R_{th}.

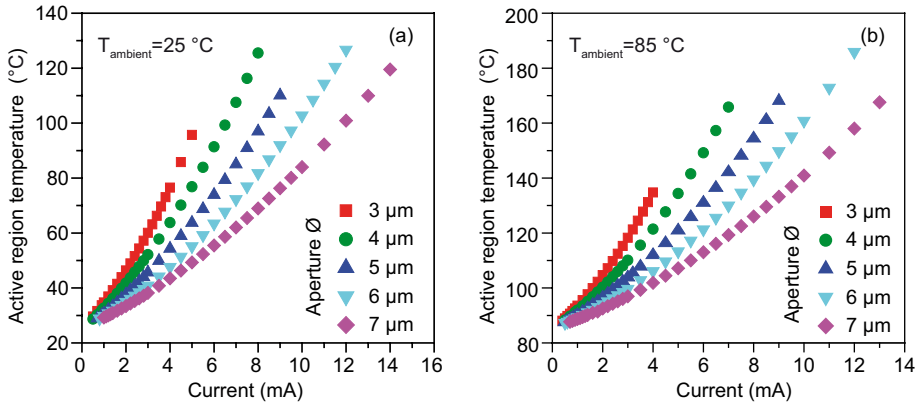

Fig. 7-11. Active region temperature T_{active} change with bias current for 980 nm VCSELs with oxide-aperture diameters ranging from ~3 to 7 µm at ambient temperatures of 25 °C (a) and 85 °C (b).

7.2 Room Temperature Energy Efficiency

In this section, detailed small-signal analyses for different oxide-aperture diameter VCSELs at room temperature are performed to obtain the –3 dB bandwidths f_{-3dB}, which indicate the achievable bit rate information, and the *D*-factor and *MCEF*, which indicate the ability of the VCSEL to obtain high modulation bandwidths at small operating currents (as required for energy efficiency). Then the data transmission results at room temperature are shown, including the maximum achievable error-free bit rates and the minimum dissipated energy.

7.2.1 Small-Signal Analysis at Room Temperature

The –3 dB modulation bandwidth f_{-3dB} versus the bias current for VCSELs with oxide-aperture diameters from ~3 to 7 µm are shown in Fig. 7-12(a). The maximum f_{-3dB} at room temperature is 20.9, 21.4, 21.5, 21.3, and 18.9 GHz for ~3, 4, 5, 6, and 7 µm oxide-aperture diameter VCSELs, respectively. The maximum f_{-3dB} reaches similar values of 21 GHz for VCSELs with oxide-aperture diameters from ~3 to 6 µm, and starts to decrease with further increases of the oxide-aperture diameter. At the same bias current, the f_{-3dB} is higher for the smaller oxide-aperture diameter VCSELs compared to larger VCSELs. In addition, the smaller oxide-aperture diameter VCSELs need a smaller current to achieve a certain f_{-3dB}. The f_{-3dB} versus the consumed electrical power P_{el} for VCSELs with oxide-aperture diameters of from ~3 to ~7 µm are shown in Fig. 7-12(b), showing the influence of oxide-aperture diameter on the potential energy consumption of the data transmission. The change of f_{-3dB} with P_{el} is similar to the change with current due to a nearly linear dependence of

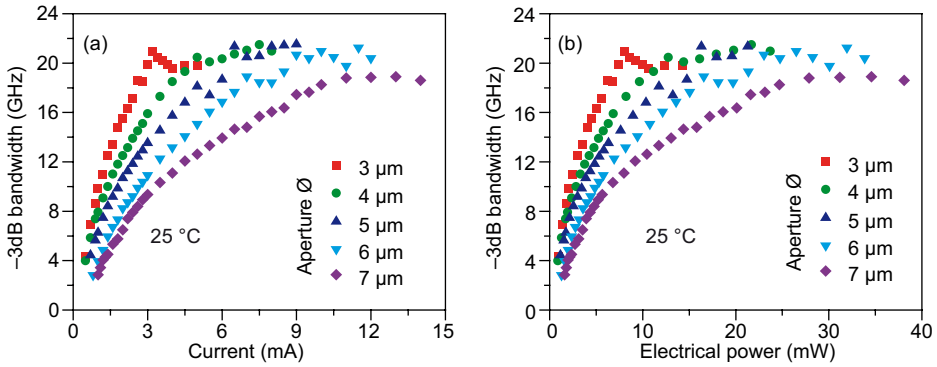

Fig. 7-12. –3 dB modulation bandwidth f_{-3dB} versus current (a) and versus electrical power (b) at 25 °C for 980 nm VCSELs with oxide-aperture diameters ranging from ~3 to 7 µm.

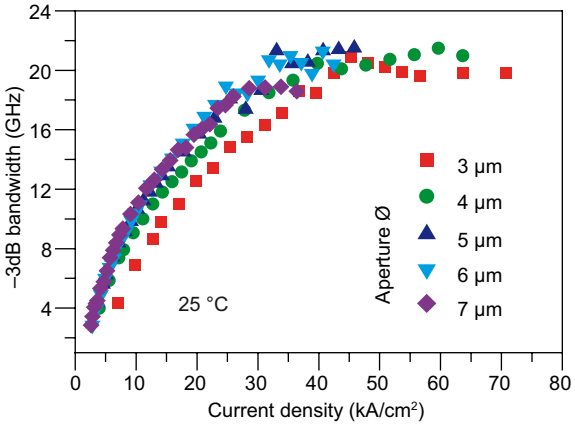

Fig. 7-13. –3 dB modulation bandwidth versus current density at 25 °C for 980 nm VCSELs with oxide-aperture diameters ranging from ~3 to 7 µm.

the bias voltage with current. The f_{-3dB} increase with increasing P_{el} until reaching a saturation point (the maximum f_{-3dB}), and a further increase of P_{el} does not lead to an increase of f_{-3dB}. To achieve a certain f_{-3dB}, smaller oxide-aperture diameter VCSELs need a lower P_{el} compared to larger VCSELs.

Fig. 7-13 shows the f_{-3dB} versus the current density. It is known that VCSELs biased at higher current densities tend to have a reduced device lifetime [147], while small oxide-aperture diameter VCSELs are generally more reliable [147]. Slightly higher current density is needed for smaller VCSELs to reach the same f_{-3dB} compared to larger VCSELs. The lifetime of VCSELs should be nearly aperture-independent because the smaller oxide-aperture diameter VCSELs are more capable of handling larger current densities. Overall, smaller oxide-aperture diameter VCSELs need smaller current, smaller electrical power, and slightly larger current density than larger VCSELs to achieve the same bandwidth.

A larger *D*-factor and a correspondingly larger *MCEF* mean a faster increase of f_r and f_{-3dB} with the current. These factors indicate the ability of the VCSEL to obtain high modulation bandwidths at small operating currents. The extracted f_{-3dB} at room temperature versus the square root of bias current minus the threshold current and

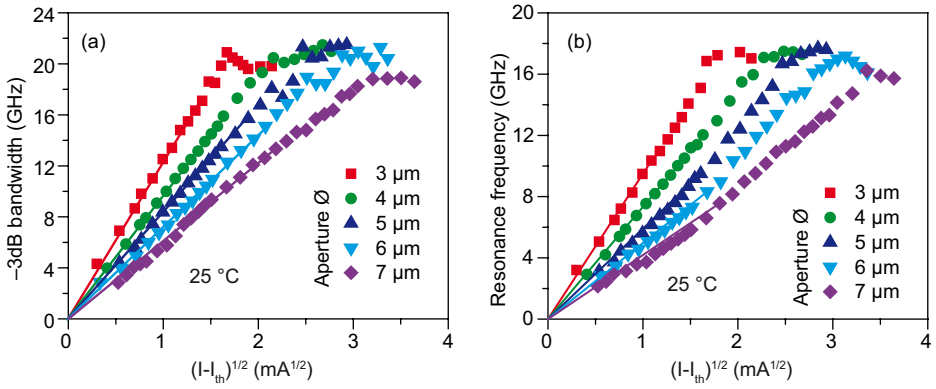

Fig. 7-14. –3 dB modulation bandwidth (a) and relaxation resonance frequency (b) versus the square root of bias current minus the threshold current at 25 °C for 980 nm VCSELs with oxide-aperture diameters ranging from ~3 to 7 µm.

the corresponding linear fittings for VCSELs with oxide-aperture diameters ranging from ~3 to ~7 µm are shown in Fig. 7-14(a), in which the *MCEF* decreases with increasing oxide-aperture diameter. The extracted f_r versus the quantify the square root of bias current minus the threshold current and the corresponding linear fittings are shown in Fig. 7-14(b). From the slope, it is found that smaller oxide-aperture diameter VCSELs have larger *D*-factors, and a faster increase of the resonance relaxation frequency with current. The *D*-factor is 9.1, 7.3, 5.9, 4.8, 3.9 GHz/(mA$^{1/2}$) for ~3, 4, 5, 6, and 7 µm oxide-aperture diameter VCSELs, respectively. Thus, at room temperature smaller oxide-aperture diameter VCSELs should achieve higher energy efficiency due to their higher *MCEFs* and *D*-factors compared to larger VCSELs.

7.2.2 High Bit-Rate Data Transmission

The small-signal measurement results show that the VCSELs can achieve high bit-rate error-free transmission at room temperature, and the maximum achievable transmission bit-rate should be different for different oxide-aperture diameter VCSELs. The results of bit error ratio (BER) measurements for maximum achievable transmission bit-rates at room temperature and the corresponding eye diagrams are shown in Fig. 7-15. Error-free data transmission is achieved at 42 Gb/s for VCSELs with oxide-aperture diameters smaller than 7 µm, and at 40 Gb/s for the ~7 µm oxide-aperture diameter VCSEL, using a standard non-return-to-zero (NRZ) modulation scheme with a pseudorandom binary sequence (PRBS) of word-length of 2^7–1 bits. This result matches well the small-signal results, where a similar maximum

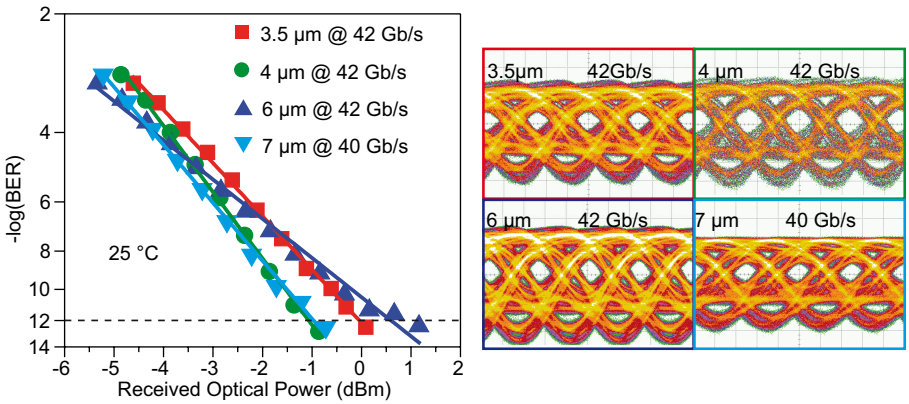

Fig. 7-15. Bit error ratio versus received optical power for a ~3.5, 4, 6, and 7 µm oxide-aperture diameter 980 nm VCSELs at 42 and 40 Gb/s at 25 °C, respectively, across 5 m of MMF with a PRBS word length of 2^7–1 and a NRZ modulation scheme, and eye diagrams at the corresponding points of error-free data transmission.

f_{-3dB} can be reached for VCSELs with oxide-aperture diameters smaller than ~7 µm, and smaller maximum f_{-3dB} can be reached for the ~7 µm oxide-aperture diameter VCSEL.

7.2.3 Energy-Efficient Data Transmission

The dissipated heat-to-bit rate ratio (HBR) is commonly used to compare the energy dissipation of different VCSEL designs for applications in energy-efficient optical interconnects. The devices are measured at operation currents that require the minimum energy per bit, which means the VCSELs operate at the lowest currents where still error-free data transmission is observed. Error-free data transmission at 35, 38, and 42 Gb/s with low energy dissipations of 145, 147, and 217 fJ/bit are achieved using the ~3 µm oxide-aperture diameter VCSEL, as shown in Fig. 7-16, with the corresponding eye diagrams. Each of these are the record energy efficiency result at the measured bit rate for 980 nm VCSELs [54, 86, 148, 149]. The same measurements are performed for slightly larger oxide-aperture diameter VCSELs. Error-free 35, 38, and 42 Gb/s data transmission with low heat dissipations of 161, 181, 228 fJ/bit are achieved by using the ~3.5 µm oxide-aperture diameter VCSEL, and 175, 197, and 296 fJ/bit are needed for a ~4 µm oxide-aperture diameter VCSEL. These entire three small oxide-aperture diameter (~3 to 4 µm) VCSELs can achieve high-speed data transmission with a low energy dissipation.

The small-signal analysis and BER measurement results show the energy dissipation change with the oxide-aperture diameter. To show this influence numerically, error-free data transmission at certain bit rates are performed using ~3, 3.5, and 4 µm

oxide-aperture diameter VCSELs. In Fig. 7-18(a), 35 Gb/s error-free data transmission at room temperature is shown. The CW bias current for the BER measurements is 2.7, 3.0, and 3.3 mA for ~3, 3.5, and 4 µm oxide-aperture diameter VCSELs, with the voltage of 2.31, 2.30, and 2.18 V, respectively. The ~3 µm oxide-aperture diameter VCSEL needs a lower bias current and electrical power, which matches with the conclusion obtained from our small-signal analysis. Low HBR values of only 145, 161, and 175 fJ/bit are required for 35 Gb/s error-free data transmission at 25 °C using VCSELs with oxide aperture diameters of ~3, 3.5, and 4 µm. The corresponding EDR values are 178, 197, and 206 fJ/bit, respectively, as shown in Fig. 7-18(b). Higher HBR and EDR values are needed for larger oxide-aperture diameter VCSELs compared with smaller VCSELs. The same data transmission experiments are performed at higher bit rates of 38 and 42 Gb/s using ~3, 3.5, and 4 µm oxide-aperture diameter VCSELs. The BER results are shown in Fig. 7-19. For 38 Gb/s error-free data transmission, the CW bias current for ~3, 3.5, and 4 µm oxide-aperture diameter VCSELs is 2.9, 3.5, and 3.78 mA with the voltage of 2.35, 2.38, and 2.32 V, respectively. Heat

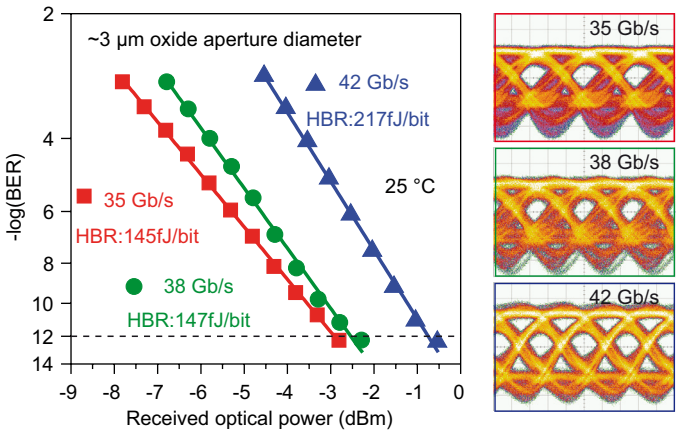

Fig. 7-16. Bit error ratio (BER) versus received optical power for the ~3 µm oxide-aperture diameter 980 nm VCSEL operating at 35, 38 and 42 Gb/s at 25 °C, respectively, and the corresponding eye diagrams.

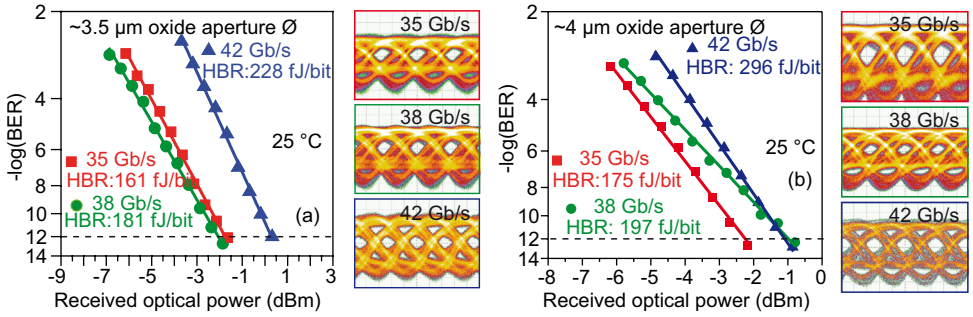

Fig. 7-17. Bit error ratio (BER) versus received optical power for ~3.5 µm (a) and ~4 µm (b) oxide-aperture diameters 980 nm VCSELs operating at 35, 38, and 42 Gb/s at 25 °C, respectively, and the corresponding eye diagrams.

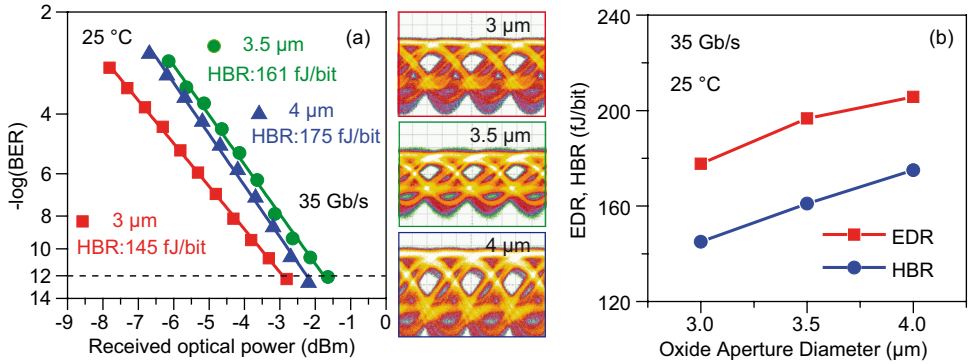

Fig. 7-18. Bit error ratio (BER) versus received optical power (a) in a back-to-back configuration for ~3, 3.5, and 4 µm oxide-aperture diameter 980 nm VCSELs at 35 Gb/s at 25 °C, and the corresponding eye diagrams. Plotted EDR and HBR values versus the oxide-aperture diameter (b).

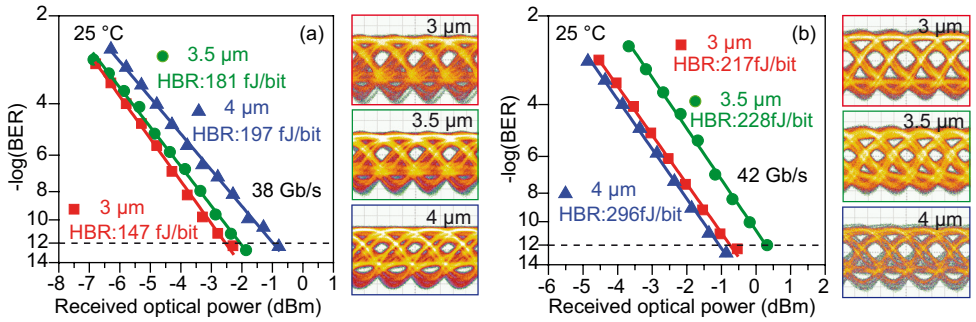

Fig. 7-19. Bit error ratio (BER) versus received optical power in a back-to-back configuration for ~3, ~3.5, and ~4 µm 980 nm VCSELs at 25 °C at 38 Gb/s (a), and at 42 Gb/s (b), and the corresponding eye diagrams at the point of error-free operation.

dissipation HBR of 147, 181, and 197 fJ/bit are required for 38 Gb/s error-free data transmission, and the corresponding EDR values are 180, 220, and 231 fJ/bit, respectively. For 42 Gb/s error-free data transmission, the CW bias current for ~3, ~3.5, and ~4 µm oxide-aperture diameter VCSELs is 4.1, 4.4, and 5.5 mA, respectively, with HBR values of 217, 228, and 296 fJ/bit, respectively. For all the bit rates investigated here, VCSELs with small oxide-apertures between ~3 to ~4 µm achieve error-free data transmission with a low energy dissipation. Furthermore, the ~3 µm oxide-aperture diameter VCSEL requires a lower bias current, lower electrical power, lower HBR, and lower EDR to achieve the same error-free data transmission as for the ~3.5 and ~4 µm oxide-aperture diameter VCSELs. This proves that small oxide-aperture diameter VCSELs are more energy-efficient than larger oxide-aperture diameter VCSELs. This behavior has also previously been observed for 850 nm VCSELs. In [142, 150], it is been demonstrated that VCSELs with small oxide-aperture diameters of from ~3 to ~4 µm are more energy-efficient than VCSELs with larger oxide-aperture diameters of 5 µm or larger when operating at room temperature. But the different part is that 850 nm VCSELs with larger oxide-aperture diameter (5 µm)

achieve larger maximum f_{-3dB} values as compared to VCSELs with smaller-oxide aperture diameter (3 μm) [142]. However, the structure used in this work shows that the 3 and 5 μm oxide-aperture diameter VCSELs achieve the same maximum f_{-3dB} at room temperature. At 85 °C, larger oxide-aperture diameter (5 μm) VCSEL achieve smaller maximum f_{-3dB} values as compared to VCSELs with smaller oxide-aperture diameters (3 μm), which is the opposite with the 850 nm VCSELs results showed in [142]. The modulation response of optimized oxide-aperture diameters for high maximum f_{-3dB} can be different for different structure designs. Due to different damping and parasitic level, the small oxide-aperture (3 μm) VCSELs can reach the same, smaller, or larger maximum f_{-3dB}. However, due to a larger D-factor, small oxide-aperture diameter VCSELs usually show better energy efficiency.

7.3 High Temperature Energy Efficiency

It is very important to achieve high energy efficiency and high bit-rate operation at high temperatures due to the high operation temperature in commercial applications. This section focuses on high temperature operation (85 °C) of high bit-rate 980 nm VCSELs. The VCSEL epitaxial structure is designed to have improved temperature stability by introducing an around –15 nm gain-to-etalon wavelength offset [98, 141]. With this offset, the VCSELs display much improved static and dynamic performance (including the maximum bit rate at the high temperature of ~85 °C, and the energy efficiency of VCSELs) at the high temperatures of 85 °C simultaneously compared to VCSELs with a smaller gain-to-etalon wavelength offset.

7.3.1 Small-Signal Analysis at High Temperature

The same small-signal measurements and evaluation presented in section 7.2.1 are performed at temperatures of 45, 65, and 85 °C. The f_{-3dB} results versus the bias current at 45 °C are shown in Fig. 7-20(b), showing a comparable behavior as at 25 °C. The difference is that the maximum f_{-3dB} only stays at high values for VCSELs with oxide-aperture diameters of between ~3 to ~5 μm, and starts to decrease for ~6 μm and larger oxide-aperture diameter VCSELs. At room temperature, the maximum f_{-3dB} stays at high values for VCSELs with oxide-aperture diameters smaller than 7 μm. The maximum –3 dB bandwidth is 21.3, 21.6, 20.6, 19.2, and 17.8 GHz for ~3, 4, 5, 6, and 7 μm oxide-aperture diameter VCSELs at 45 °C, respectively. The extracted relaxation resonance frequencies f_r versus the quantity the square root of

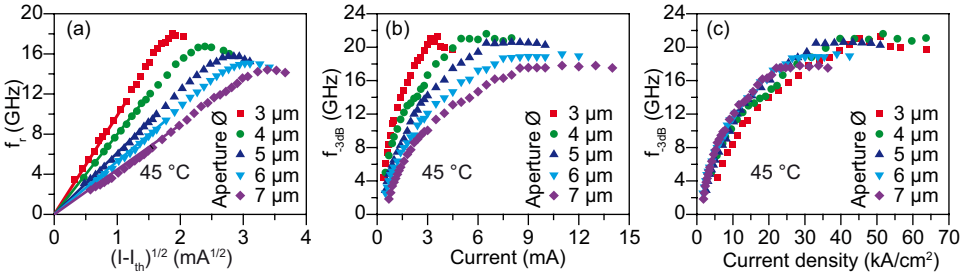

Fig. 7-20. Relaxation resonance frequency f_r (a) at 45 °C versus the square root of the current above the threshold current for 980 nm VCSELs with oxide-aperture diameters ranging from ~3 to 7 µm. The dots show the measurement data and the straight lines indicate the linear fittings used for obtaining the *D*-factors. Also shown is the –3 dB modulation bandwidth f_{-3dB} versus the current (b), and as a function of the current density (c).

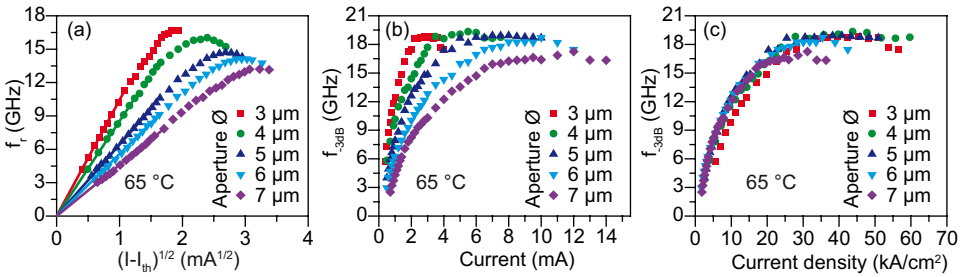

Fig. 7-21. Relaxation resonance frequency f_r (a) at 65 °C versus the square-root of the current above the threshold current for 980 nm VCSELs with oxide aperture diameters ranging from ~3 to 7 µm. The dots show the measurement data and the straight lines indicate the linear fittings used for obtaining the *D*-factors. Also shown is the –3 dB modulation bandwidth f_{-3dB} versus the current (b), and as a function of the current density (c).

the current above the threshold current and the corresponding linear fittings to this data are shown in Fig. 7-20(a). This data also shows a similar trend of variation with current as at 25 °C. The *D*-factor is 9.5, 8.0, 6.1, 5.3, and 4.5 GHz/(mA$^{1/2}$) for ~3, 4, 5, 6, and 7 µm oxide-aperture diameter VCSELs, respectively. The maximum f_r slightly decreases with increasing oxide-aperture diameter at 45 °C, while at room temperature the maximum f_r reach similar values for VCSELs with oxide-aperture diameter ranging from ~3 to ~7 µm. The f_{-3dB} change with the current density is very similar to the result at room temperature as well, as shown in Fig. 7-20(c). The change of f_{-3dB} at 65 °C with the current and current density are similar to the results at 45 °C, where the only difference is a smaller maximum value. The extracted relaxation resonance frequencies f_r versus the square root of the current above the threshold current are shown in Fig. 7-21(a). The *D*-factor is 10.4, 8.5, 6.3, 5.6, and 4.6 GHz/(mA$^{1/2}$) for ~3, 4, 5, 6, and 7 µm oxide-aperture diameter VCSELs, respectively, which are higher than the results at 25 and 45 °C. The maximum f_r value is 16.7, 16.1, 14.7, 14.1, and 13.2 GHz for ~3, 4, 5, 6, and 7 µm oxide-aperture diameter VCSELs, respectively, which decreases with increasing oxide-aperture diameter. This is different from the

result at 25 °C, where the maximum f_r, (i.e. the saturation values of f_r for a given oxide-aperture diameter) for the 3, 4, and 5 μm oxide-aperture diameter VCSELs are almost equal.

Fig. 7-22(a) shows the extracted f_{-3dB} for the VCSELs against current at 85 °C. The small oxide-aperture diameter VCSELs need smaller bias currents to achieve a certain f_{-3dB} compared to the larger oxide-aperture diameter VCSELs. Furthermore, the small oxide-aperture diameter VCSELs can achieve slightly higher maximum f_{-3dB} than large oxide-aperture diameter VCSELs. Thus the small oxide-aperture VCSELs are able to operate at higher bit rates, which will be proved later via data transmission experiments. The –3 dB bandwidth f_{-3dB} versus the electrical power for the VCSELs with oxide-aperture diameters of from ~3 to ~7 μm are shown in Fig. 7-22(b). The f_{-3dB} increase with increasing the electrical power at small values until they reach the saturation, then a further increase in electrical power does not lead to an increase of f_{-3dB}. VCSELs with smaller oxide-aperture diameters achieve larger f_{-3dB} at a given electrical power compared to VCSELs with large apertures. In addition, VCSELs with smaller oxide-aperture diameters need lower electrical power to achieve a given f_{-3dB} compared to larger VCSELs. Fig. 7-22(c) shows the

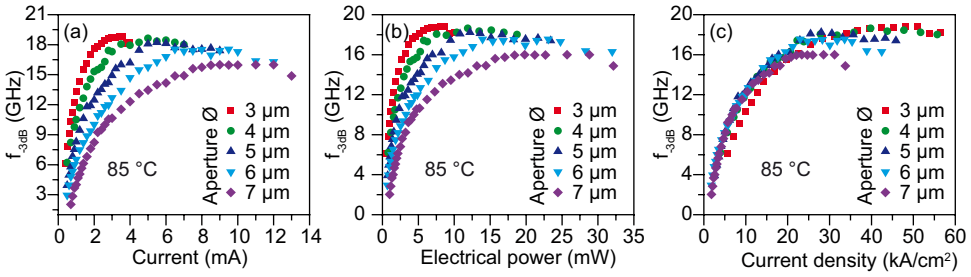

Fig. 7-22. –3 dB modulation bandwidth f_{-3dB} versus current (a), electrical power (b), and current density (c) at 85 °C for 980 nm VCSELs with oxide-aperture diameters ranging from ~3 to 7 μm.

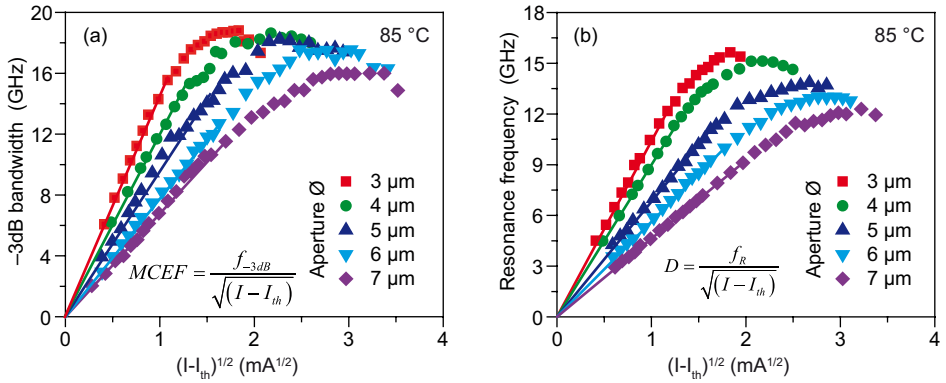

Fig. 7-23. –3 dB bandwidth f_{-3dB} (a) and relaxation resonance frequency f_r (b) at 85 °C versus the square-root of the current above the threshold current for 980 nm VCSELs with oxide-aperture diameters ranging from ~3 to 7 μm. The dots show the measurement data and the straight lines indicate the linear fittings used for obtaining the *MCEF* and *D*-factors.

f_{-3dB} versus the current density at 85 °C. Smaller oxide-aperture diameter VCSELs need lower currents, lower electrical powers, and nearly the same current density to reach the same bandwidth at 85 °C compare with larger VCSELs.

Figure 7-23 shows the f_{-3dB} and the f_r versus the quantity the square root of the current above the threshold current at 85 °C for the VCSELs with oxide-aperture diameters ranging from ~3 to ~7 μm. The *MCEF* and *D*-factor decrease with increasing oxide-aperture diameter, which are 14.97 and 10.7 GHz/(mA)$^{1/2}$ for the ~3 μm oxide-aperture diameter VCSEL and 7.0 and 4.7 GHz/(mA)$^{1/2}$ for the ~7 μm oxide-aperture diameter VCSEL, respectively. The small oxide-aperture diameter VCSELs have larger *MCEF* and *D*-factors and thus a faster increase of f_{-3dB} and f_r with the bias current and larger values of *MCEF* and *D*-factors at a given forward bias current. In combination with the f_{-3dB} evaluation, it should be noted that the small oxide-aperture VCSELs (from ~3 to ~4 μm) have larger *MCEF* and *D*-factors and achieve slightly higher bit rates at the same current compared to the large oxide-aperture VCSELs (larger than 4 μm). This means small oxide-aperture VCSELs (from ~3 to ~4 μm) in this work will be beneficial for the high-speed and energy-efficient operation at high temperatures such as at 85 °C.

Figure 7-24(a) shows the f_{-3dB} as a function of temperature at certain bias currents for a ~3 μm oxide-aperture diameter VCSEL, in order to study the effect of temperature on the f_{-3dB}. For small bias currents, the f_{-3dB} increase with increasing the heat sink temperature, due to an around –15 nm QW gain-to-etalon wavelength offset, which leads to an increased differential gain with increasing the active region temperature. The *D*-factor has the same change trend with the differential gain as for the f_{-3dB}. The differential gain reaches a maximum value at around 87 °C then starts to reduce slowly. The active region temperature can be much higher than the heat-sink temperature. When the current is low, the active region temperature is lower than 87 °C. The differential gain increases with the current until it reaches

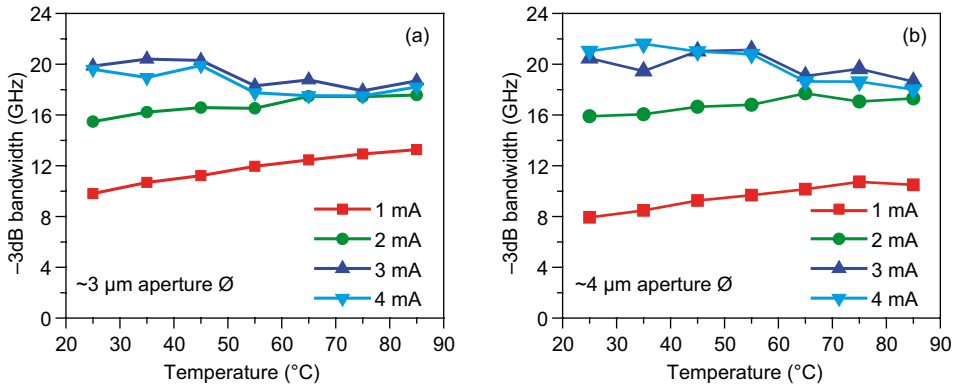

Fig. 7-24. –3 dB modulation bandwidth f_{-3dB} change with temperature at certain currents for ~3 μm (a) and ~4 μm (b) oxide-aperture diameter 980 nm VCSELs.

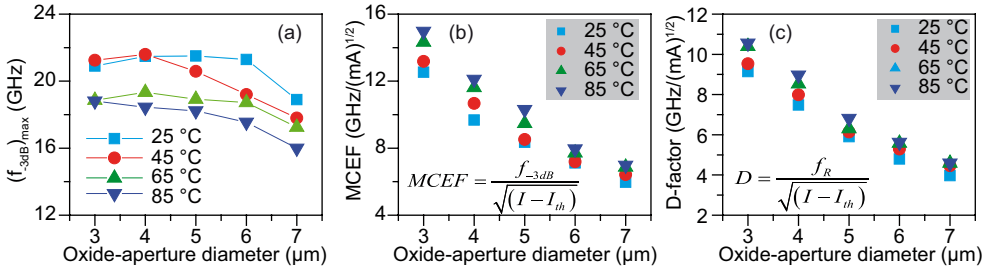

Fig. 7-25. Maximum –3 dB bandwidth f_{-3dB} (a), *MCEF* (b), and *D*-factor (c) versus oxide-aperture diameter at 25, 45, 65, and 85 °C for 980 nm VCSELs with oxide-aperture diameters ranging from ~3 to ~7 μm.

its maximum value. The increasing differential gain leads to a larger f_r, and thus a larger –3 dB bandwidth f_{-3dB} can be reached before reaching thermal limitation. For a large bias current, the f_{-3dB} decreases with increasing the temperature due to the high active region temperature. The f_{-3dB} shows the high temperature-stability over the entire current range. Larger oxide-aperture diameter (~4 μm) VCSELs show a similar change trend as shown in Fig. 7-24(b).

Fig. 7-25(a) shows the maximum f_{-3dB} versus oxide-aperture diameter at 25, 45, 65, and 85 °C. At room temperature, VCSELs with oxide-aperture diameters ranging from ~3 to~6 μm can reach a similar high f_{-3dB}. At a higher temperature of 45 °C, the small oxide-aperture (~3 to ~4 μm) VCSELs can reach a slightly higher f_{-3dB}, and then f_{-3dB} starts to decrease as the aperture diameter increases. For even higher temperatures of 65 and 85 °C, the maximum f_{-3dB} starts to decrease with the ~4 μm oxide-aperture diameter VCSEL. Large aperture VCSELs have smaller maximum bandwidths over all of the temperature range. The results predicted from the modulation theory match the measured results, where the *MCEF* and *D*-factor decrease with increasing oxide-aperture diameter, as shown in Fig. 7-25(b) and 7-25(c).

7.3.2 High Bit-Rate Data Transmission

Due to the optimized active region and mirror design, process flow, and optimized gain-mode offset, the 980 nm VCSELs can achieve high bit-rate also at high temperatures besides at room temperature. The eye diagrams for the ~3.5 μm oxide-aperture diameter VCSEL operated at 20, 30, and 42 Gb/s at room temperature and operated at 35, 36, and 38 Gb/s at 85 °C are shown in Fig. 7-26. At room temperature, clear open eyes can be achieved from 20 to 42 Gb/s. Open eyes at 38 Gb/s with a signal to noise ratio (S/N) of 3.08 is achieved for the temperature of 85 °C. With increasing

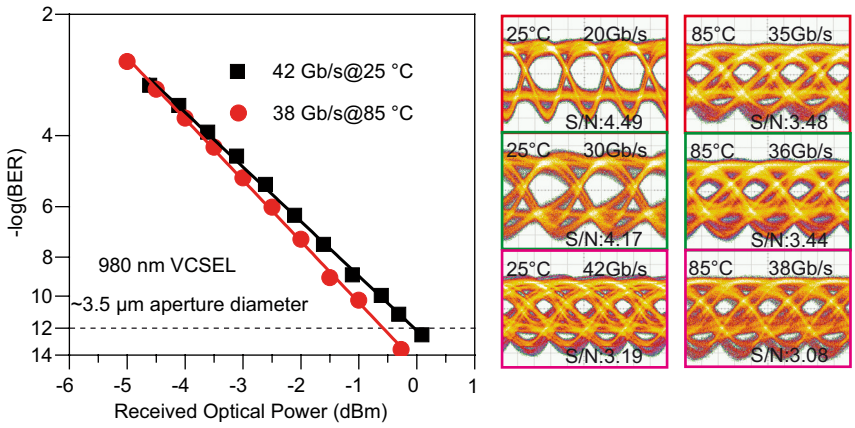

Fig. 7-26. Bit error ratio (BER) versus received optical power operating at 42 and 38 Gb/s at 25 and 85 °C, and eye diagrams at 20, 30, and 42 Gb/s at 25°C, and at 35, 36, and 38 Gb/s at 85 °C for a ~3.5 µm oxide aperture diameter VCSEL.

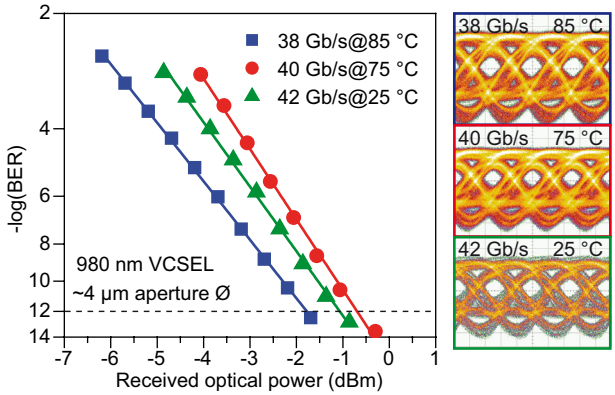

Fig. 7-27. Bit error ratio (BER) versus received optical power for a ~4 µm oxide-aperture diameter 980 nm VCSEL operating at 42, 40, and 38 Gb/s at 25, 75, and 85 °C, respectively, and the corresponding eye diagrams.

bit-rate, the eye openings are getting smaller and the S/N value decreases. The BER measurement results of this maximum achievable transmission bit-rate, which are 42 Gb/s at room temperature and 38 Gb/s at 85 °C, are shown in Fig. 7-26.

The BER results of maximum achievable error-free transmission bit-rate at the maximum temperature for the ~4 µm oxide-aperture diameter VCSEL are shown in Fig. 7-27. Error-free data transmission at 42 Gb/s is achieved at room temperature, while 40 and 38 Gb/s is achieved at 75 and 85 °C, respectively.

Eye diagrams at 24, 32, 38, and 42 Gb/s at 25 °C using the ~6 µm oxide-aperture diameter VCSEL are shown in Fig. 7-28. Clear open eyes can be obtained up to 42 Gb/s (with a signal-to-noise ratio of 3.14). At 45 and 65 °C, clear open eyes at 40 Gb/s are obtained with S/N ratios of 2.78 and 2.86, respectively. At 85 °C, clear open eyes at 31 and 35 Gb/s are achieved. The BER measurement results of these corresponding clear open eyes at room temperature are shown in Fig. 7-29(a). Error-free data transmission at 24, 32, 38, and 42 Gb/s can be achieved at 25 °C using the ~6 µm oxide-aperture diameter VCSEL. As shown in Fig. 7-29(b), error-free data transmission at 31 and 35 Gb/s can be achieved at 85 °C. The maximum achievable

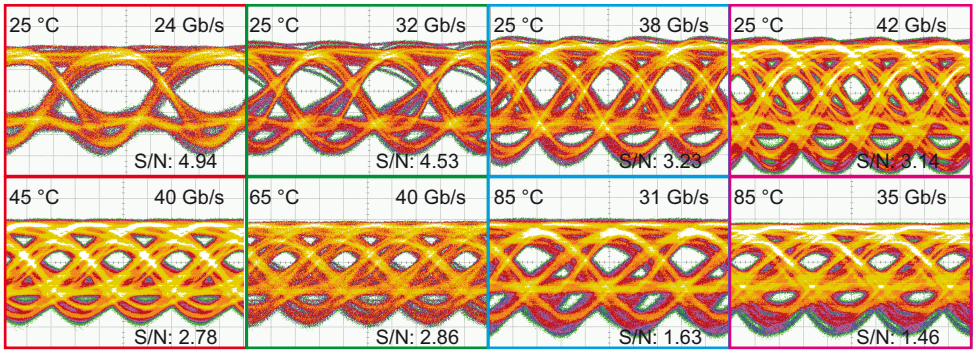

Fig. 7-28. Eye diagrams for the ~6 µm oxide-aperture diameter 980 nm VCSEL operating at 24, 32, 38 and 42 Gb/s at 25 °C, 40 Gb/s at 45 °C, 40 Gb/s at 65 °C, and 31 and 35 Gb/s at 85 °C.

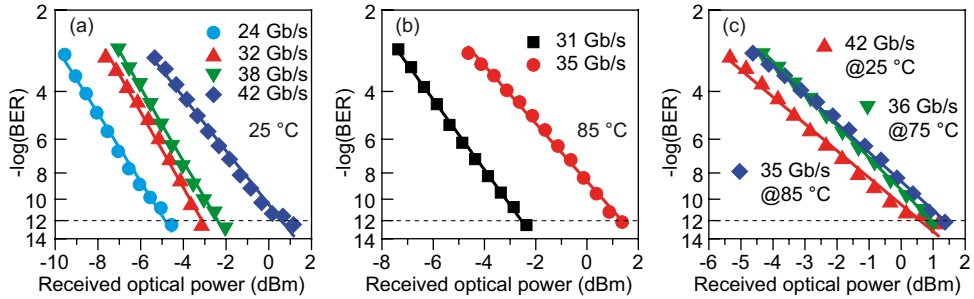

Fig. 7-29. Bit error ratio (BER) versus received optical power for the ~6 µm oxide-aperture diameter 980 nm VCSEL operating at 24, 32, 38 and 42 Gb/s at 25 °C (a), and operating at 31, and 35 Gb/s at 85 °C (b), and at the maximum achievable bit rate at different temperatures (c).

bit rate at the highest preset temperature is 42, 36 and 35 Gb/s at 25, 75, and 85 °C, respectively. For the large oxide-aperture diameter VCSELs (~6 µm), the maximum achievable speed at high temperature (75 and 85 °C) slightly decreases compared to the smaller oxide-aperture diameter (from ~3 to ~4 µm) VCSELs.

Figure 7-30 shows the BER results for the maximum achievable transmission bit rate at 85 °C using the VCSELs with oxide-aperture diameters ranging from ~3 to ~5 µm [34]. 38 Gb/s error-free data transmission for VCSELs smaller than 5 µm is achieved, and only 35 Gb/s can be achieved for ~5 µm oxide-aperture diameter VCSELs, which is 3 Gb/s lower than for the VCSELs with smaller oxide-aperture diameters. These data transmission results match well with the predictions from the small-signal analysis, where the maximum −3 dB bandwidth is predicted to be a stable high value for VCSELs with small oxide-aperture diameters (smaller than 5 µm), and start to decrease for ~5 µm and larger oxide-aperture diameter VCSELs. For the smaller VCSELs (with an oxide-aperture diameter smaller than 5 µm), the maximum achievable bit rate only has a 4 Gb/s (9.5 %) change, decreasing from 42 to 38 Gb/s when the temperature increases from 25 to 85 °C, thus showing highly temperature-stable modulation.

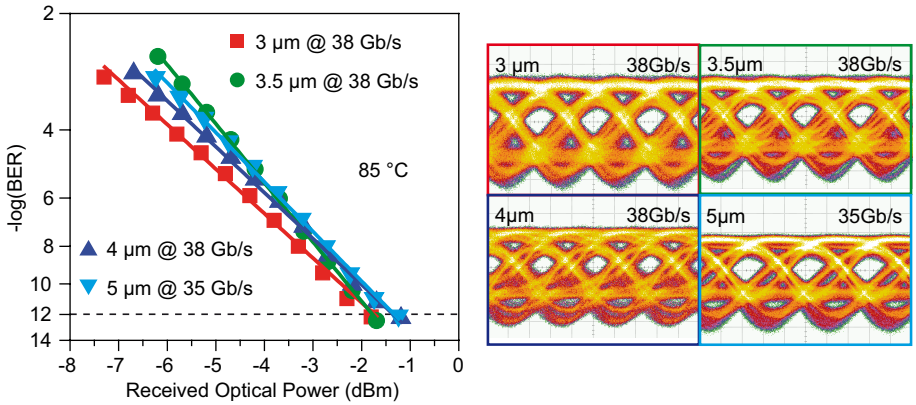

Fig. 7-30. Bit error ratio versus received optical power in a BTB configuration for ~3, 3.5, 4, and 5 µm oxide-aperture diameter 980 nm VCSELs at 38 and 35 Gb/s at 85 °C, respectively, and eye diagrams at the corresponding points of error-free data transmission.

7.3.3 Energy-efficient data transmission

Highly temperature-stable static performance (threshold current, threshold electrical power, differential quantum efficiency, and more) and highly temperature-stable high bit-rate modulation performance (maximum achievable modulation bandwidth, *D*-factor, and *MCEF*) provide the possibility of energy-efficient operation at high temperature as at room temperature. 35 and 38 Gb/s error-free data transmissions at 85 °C are achieved with low energy dissipation of only 139 [34], and 177 fJ/bit with the ~3 µm oxide-aperture diameter VCSEL, as shown in Fig. 7-31. These are the lowest values for VCSELs operating at 85 °C at any wavelength [49, 54] at the corresponding bit-rate. Figure 7-32 shows that the slightly larger VCSELs (~3.5 and 4 µm oxide-aperture diameter) operate at 35 and 38 Gb/s at 85 °C. Also the low power dissipation of only 140 and 177 fJ/bit are needed by using ~3.5 µm oxide-aperture diameter VCSEL for 35 and 38 Gb/s error-free data transmission, respectively, while 159 and 177 fJ/bit are needed by using a ~4 µm oxide-aperture diameter VCSEL. 20 fJ/bit more power dissipation per bit is needed for 35 Gb/s error-free data transmission by increasing the oxide-aperture diameters of the VCSELs from ~3 µm to 4 µm. All of the small VCSELs with an oxide-aperture diameter between ~3 and 4 µm are investigated and can achieve a high bit-rate data transmission with a low energy dissipation at the high temperatures.

Error-free data transmission at certain bit rates at 85 °C are performed using ~3, 3.5, and 4 µm oxide-aperture diameter VCSELs to show how the oxide-aperture diameter impacts the power dissipation. Error-free 35 Gb/s data transmission at 85 °C using ~3, 3.5, and 4 µm oxide-aperture diameter VCSELs are shown in Fig. 7-33(a). The CW bias current for 35 Gb/s error-free data transmission is 2.7, 2.8, and 3.2 mA

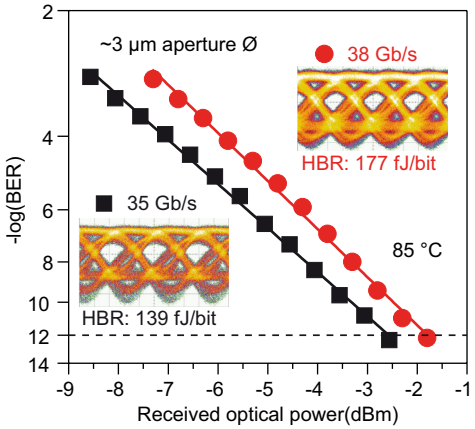

Fig. 7-31. Bit error ratio versus received optical power for 980 nm VCSELs with oxide-aperture diameters of ~3 μm operating at 35 and 38 Gb/s at 85 °C, and eye diagrams at the corresponding bit rates and modulation conditions.

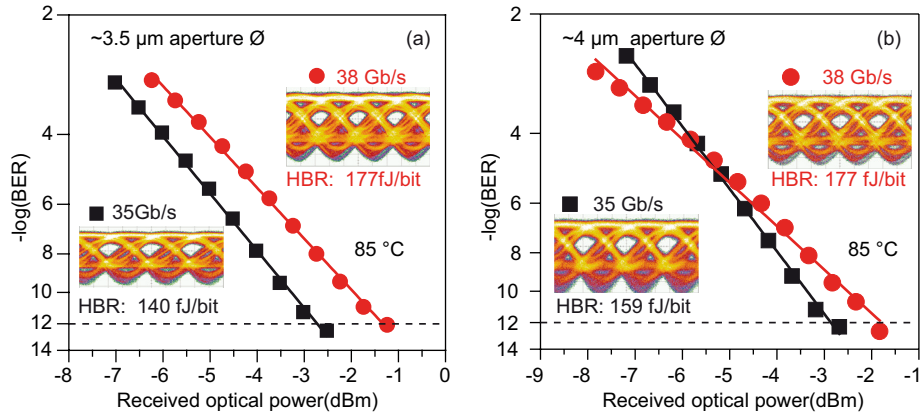

Fig. 7-32. Bit error ratio versus received optical power for 980 nm VCSELs with oxide-aperture diameters of ~3.5 μm and 4.0 μm operating at 35 and 38 Gb/s at 85 °C, and eye diagrams at the corresponding bit rates and modulation conditions.

where a low energy dissipation of only 139, 140, and 159 fJ/bit are needed for ~3, 3.5, and 4 μm oxide-aperture diameter VCSELs, respectively. Smaller oxide-aperture diameter VCSELs need lower operating bias currents and have lower energy dissipation than larger oxide-aperture diameter VCSELs, as is predicted from small signal analysis. The same data transmission experiments are performed at the higher bit rates of 38 Gb/s and the results are shown in Fig. 7-33(b). The CW bias current for 38 Gb/s error-free data transmission is 3.4, 3.5, and 3.6 mA and low energy dissipation of 177, 177, and 177 fJ/bit for ~3, 3.5, and 4 μm oxide-aperture diameter VCSELs, respectively. For 38 Gb/s error-free data transmission, VCSELs with oxide-aperture diameters from ~3 to 4 μm have the same power dissipation. This is because the bias current needs to be slightly larger than the minimum current needed to reach the given bandwidth due to the low output power for the ~3 μm oxide-aperture diameter VCSEL. Small oxide-aperture diameter VCSELs display low bias currents, low electrical power, and low energy dissipation to achieve high bit-rate error-free data

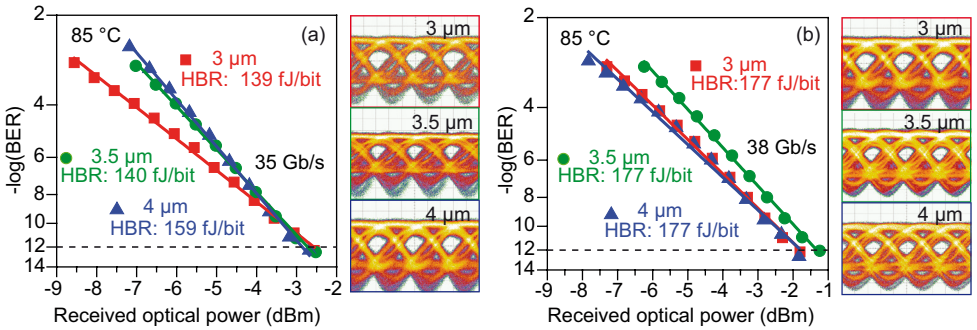

Fig. 7-33. Bit error ratio versus received optical power in a back-to-back configuration for a ~3, ~3.5, and 4 µm 980 nm VCSELs at 35 Gb/s in (a) and at 38 Gb/s in (b), both at 85 °C, and the corresponding eye diagrams at the point of error-free operation.

transmission, which proves the small oxide-aperture diameter (from ~3 to ~4 µm) VCSELs are very energy-efficient, suitable for high bit-rate, energy-efficient optical interconnect applications.

7.4 Summary

For the first time it is experimentally demonstrated that 980 nm VCSELs can achieve temperature-stable, energy-efficient, and high bit-rate operation concurrently. Error-free data transmission at 42 and 38 Gb/s are achieved at 25 and 85 °C, respectively. Record low 139 and 177 fJ/bit for 35 and 38 Gb/s error-free transmission at 85 °C are achieved with a ~3 µm oxide-aperture diameter VCSEL, which are the most energy-efficient VCSELs operating at 85 °C at any wavelength. At room temperature, only 145, 147, and 217 fJ/bit energy dissipation are needed for 35, 38 and 42 Gb/s error-free transmission. These are the record low energy dissipations for any 980 nm VCSELs. These VCSELs also demonstrate very temperature-insensitive static and dynamic properties. 38 Gb/s error-free transmission can be achieved at 25, 45, 65, and 85 °C without any change of the operating point or the modulation conditions using ~3.5 and 4 µm oxide-aperture diameter VCSELs. The 980 nm VCSELs with oxide-aperture diameters from ~3 to 4 µm have a small threshold current, large mode spacing, large *D*-factor, are very energy efficient, are very temperature-stable, and are capable of operating at high bit-rates. Such VCSELs are especially well suited for optical interconnects in high performance computers.

Chapter 8
Conclusions and Outlook

In this Chapter the main contributions and conclusions of this dissertation are summarized along with an outlook for future research in the area of vertical-cavity surface-emitting lasers (VCSELs).

8.1 Conclusions

The work presented in this dissertation is centered around one key problem, how to achieve high bit-rate performance with 980 nm GaAs-based oxide-confined VCSELs at room temperature and at high temperatures while simultaneously operating with minimal energy dissipation. These VCSEL performance attributes are a main requirement for the use of VCSELs as light sources in future short-reach (hundreds of meters across multimode optical fiber) to on-chip (centimeters or shorter distances across waveguides) optical interconnect applications. In order to achieve these requirements concurrently, VCSELs are developed to be capable of high bit-rates at low forward bias currents at room temperature and at high temperatures (up to about 85 °C). This involves the consideration of all aspects of the devices including the epitaxial design, device geometry and device fabrication, and device characterization. This work experimentally demonstrates for the first time that high bit-rate, temperature-stable, and energy-efficient operation can be achieved concurrently. The key contributions and conclusions of this dissertation are:

1. Optimized 4.2 nm-thick compressive-strained $In_{0.21}Ga_{0.79}As$ QWs are used in the active region to improve high bit-rate performance.
2. Tensile strained $GaAs_{0.88}P_{0.12}$ barrier layers which can partially compensate strain are used to improve performance at high temperature.
3. An around –15 nm QW gain-to-etalon wavelength offset is used to improve temperature stability. The influence of the QW gain-to-etalon wavelength offset on the static performance and the high-speed modulation performance is simulated and experimentally studied.

4. Linearly graded, modulation-doped DBRs, multiple-oxide layers, thick BCB under the bond pad, and a double mesa structure with an optimized geometry are used to improve the parasitic cutoff frequency.
5. Photon lifetime is adjusted during the device processing by etching the topmost DBR layer to change the power reflectance as seen by photons propagating up toward the top DBR. This DBR reflectivity tuning increases the output power and increases the −3 dB modulation bandwidth.
6. Temperature-dependent and oxide-aperture diameter-dependent impedance characteristics are investigated. The small oxide-aperture diameter VCSELs are not limited by parasitics at temperatures from 25 to 85 °C. The larger capacitance of larger oxide-aperture VCSELs restricts the VCSELs' parasitic cutoff frequency and limits the −3 dB modulation bandwidth.
7. The relative intensity noise is investigated at different bias currents at room temperature for different oxide-aperture diameter VCSELs. The studied VCSELs can satisfy the requirements of bandwidth and RIN for the 32 GFC Fibre Channel standard.
8. Systematic characterization including temperature-dependent and oxide-aperture diameter-dependent static measurements, small-signal analysis, and data transmission experiments are presented. Important parameters, for example −3 dB modulation bandwidth, *D*-factor, resonance frequency, parasitic cutoff frequency are extracted.
9. Different from what is typically observed, the threshold current, threshold electrical power, *D*-factor, *MCEF,* and –3 dB modulation bandwidth (at low bias current) are larger at 85 °C compared to their values at 25 °C for the 980 nm VCSELs, which results from the QW gain-to-etalon wavelength offset.
10. The maximum −3 dB modulation bandwidth can reach high values of 21 GHz for VCSELs at room temperature with oxide-aperture diameters from 3 to 6 μm, and the bandwidth starts to decrease with further increase of the oxide-aperture diameter at room temperature.
11. The maximum −3 dB modulation bandwidth can reach high values of 19 GHz for VCSELs at 85 °C with oxide-aperture diameters from 3 to 4 μm, and starts to decrease with further increase of the oxide-aperture diameter at room temperature.
12. Both at room temperature and high temperature, the smaller oxide-aperture diameter (3 to 4 μm) VCSELs need a smaller bias current and smaller electrical power to achieve a certain −3 dB modulation bandwidth.

13. The VCSELs demonstrate very temperature insensitive static and dynamic characteristics. Error-free data transmission at a bit rate of 38 Gb/s is achieved at 25, 45, 65, and 85 °C, without any change of the operating point or the modulation conditions.
14. The VCSELs demonstrate that high bit rates can be reached at room temperature and at high temperature. Error-free data transmission at 42 and 38 Gb/s are achieved at 25 and 85 °C, respectively.
15. A record low energy dissipation of 139 and 177 fJ/bit for 35 and 38 Gb/s error-free transmission at 85 °C is achieved with a 3 µm oxide-aperture diameter VCSEL. These VCSELs are the most energy efficient VCSELs operating at 85 °C at any wavelength to date.
16. At room temperature, only 145, 147, and 217 fJ/bit of energy dissipation is needed for 35, 38 and 42 Gb/s error-free transmission. These are record low energy dissipations for 980 nm VCSELs.

To conclude and summarize, 3 to 4 µm oxide-aperture diameter 980 nm VCSELs studied in this work have a small threshold current, large mode spacing, large *D*-factor, are very energy-efficient, are very temperature-stable, and are capable of operating at high bit-rates, compared to larger oxide-aperture diameters. Such VCSELs are especially well suited for optical interconnects in high performance computers.

8.2 Outlook

Based on fabrication and characterization methodologies the work has proven that with one 980 nm VCSEL design it is possible to achieve high bit-rate, temperature-stable, and energy-efficient operation concurrently. Nevertheless, there is still room for further improvement. Following is listed some key points of potential improvements based on the results of this dissertation.

1. Reduce the 1.5λ-thick optical cavity to a 0.5λ-thick optical cavity to further increase the photon density and reduce the mode volume.
2. Change the $Al_{0.12}Ga_{0.9}As/Al_{0.9}Ga_{0.1}As$ bottom DBR to a binary GaAs/AlAs DBR to improve the thermal conductivity and reduce the effective cavity length to improve the thermal performance and high bit-rate modulation performance.
3. Improve the VCSEL's doping profile to further lower the resistance and absorption, by for example lowering the doping levels of the grading layer when the aluminum-arsenide composition increases from a low value to high values to lower free carrier absorption.

4. Use undoped substrates and remove the bottom contact layer beneath the contact GSG pads to further reduce the pad capacitance.
5. Add deep oxide layers in addition to the two oxide-aperture layers to further lower the mesa capacitance.
6. Reduce the size of the top mesa for large oxide-aperture diameter VCSELs to reduce mesa capacitance.
7. Reduce the number of top DBR pairs from 24 pairs to 20 pairs to increase the output power and lower the photon lifetime.
8. Use different QW barrier material besides GaAs and GaAsP, for example, $Al_{0.35}Ga_{0.65}As$ to improve the differential gain.
9. Use QDs as the active region media to improve temperature stability.
10. Use higher strained InGaAs QWs for longer wavelength VCSELs, like 1060 nm VCSEL to improve the differential gain.
11. Use a tunnel junction for longer wavelength (1060 nm) VCSELs to further lower resistance and absorption and increase the modulation bandwidth.

References

[1] H. Soda, K. Iga, C. Kitahara, and Y. Suematsu, "GaInAsP/InP Surface Emitting Injection Lasers", *Japanese Journal of Applied Physics*, vol. 18, no. 12, pp. 2329–2330, 1979.

[2] K. Iga, "Surface-emitting laser-its birth and generation of new optoelectronics field", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 6, no. 6, pp. 1201–1215, Nov. 2000.

[3] K. Iga, "VCSEL-Vertical Cavity Surface Emitting Lasers by their inventor", in *Proc. 6th Ludwig Boltzmann Symposium*, Feb. 2014, pp. 1–1.

[4] J. P. van der Ziel and M. Ilegems, "Multilayer GaAs-$Al_{0.3}Ga_{0.7}As$ dielectric quarter wave stacks grown by molecular beam epitaxy", *Applied Optics*, vol. 14, no. 11, pp. 2627–2630, 1975.

[5] M. Ogura, T. Hata, N. J. Kawai, and T. Yao, "GaAs/$Al_x Ga_{1-x} As$ Multilayer Reflector for Surface Emitting Laser Diode", *Japanese Journal of Applied Physics*, vol. 22, no. 2A, pp. L112–L114, Jan. 1983.

[6] M. Ogura, T. Hata, and T. Yao, "Distributed Feed Back Surface Emitting Laser Diode with Multilayered Heterostructure", *Japanese Journal of Applied Physics*, vol. 23, no. 7A, pp. L512–L514, Jun. 1984.

[7] M. Ogura, W. Hsin, M.-C. Wu, S. Wang, J. R. Whinnery, S. C. Wang, and J. J. Yang, "Surface-emitting laser diode with vertical GaAs/GaAlAs quarter-wavelength multilayers and lateral buried heterostructure", *Applied Physics Letters*, vol. 51, no. 21, pp. 1655–1657, Sep. 1987.

[8] F. Koyama, S. Kinoshita, and K. Iga, "Room-temperature continuous wave lasing characteristics of a GaAs vertical cavity surface-emitting laser", *Applied Physics Letters*, vol. 55, no. 3, pp. 221–222, May 1989.

[9] Y. H. Lee, J. L. Jewell, A. Scherer, S. L. McCall, J. P. Harbison, and L. T. Florez, "Room-temperature continuous-wave vertical-cavity single-quantum-well microlaser diodes", *Electronics Letters*, vol. 25, no. 20, pp. 1377–1378, Sep. 1989.

[10] D. L. Huffaker, D. G. Deppe, K. Kumar, and T. J. Rogers, "Native-oxide defined ring contact for low threshold vertical-cavity lasers", *Applied Physics Letters*, vol. 65, no. 1, pp. 97–99, Jul. 1994.

[11] M. H. MacDougal, P. D. Dapkus, V. Pudikov, Hanmin Zhao, and G.-M. Yang, "Ultralow threshold current vertical-cavity surface-emitting lasers with AlAs oxide-GaAs distributed Bragg reflectors", *IEEE Photonics Technology Letters*, vol. 7, no. 3, pp. 229–231, Mar. 1995.

[12] J. A. Tatum, “The evolution of 850nm VCSELs from 10Gb/s to 25 and 56Gb/s”, in *Proc. Optical Fiber Communications Conference and Exhibition (OFC)*, 2014, pp. 1–3.

[13] M. R. T. Tan, “Commercial applications of vertical cavity surface emitting lasers”, in *Proc. Conference on Lasers and Electro-Optics (CLEO)*, 2000, pp. 201.

[14] R. S. Geels and L. A. Coldren, “Submilliamp threshold vertical-cavity laser diodes”, *Applied Physics Letters*, vol. 57, no. 16, pp. 1605–1607, Oct. 1990.

[15] T. Baba, Y. Yogo, K. Suzuki, F. Koyama, and K. Iga, “Near room temperature continuous wave lasing characteristics of GaInAsP/InP surface emitting laser”, *Electronics Letters*, vol. 29, no. 10, pp. 913–914, May. 1993.

[16] J. A. Lott, “Visible Vertical Cavity Surface Emitting Lasers”, *Dissertation*, the University of New Mexico, Albuquerque, New Mexico, USA, 18 Dec. 1993.

[17] J. A. Lott and R. P. Schneider, Jr, “Electrically injected visible (639-661 nm) vertical cavity surface emitting laser”, *Electronics Letters*, vol. 29, no. 10, pp. 830–832, 1993.

[18] J. A. Lott, R. P. Schneider, J. C. Zolper, and K. J. Malloy, “AlGaInP visible resonant cavity light-emitting diodes”, *IEEE Photonics Technology Letters*, vol. 5, no. 6, pp. 631–633, 1993.

[19] K. D. Choquette, R. P. Schneider, M. H. Crawford, K. M. Geib, and J. J. Figiel, “Continuous wave operation of 640-660 nm selectively oxidised AlGaInP vertical-cavity lasers”, *Electronics Letters*, vol. 31, no. 14, pp. 1145–1146, Jul. 1995.

[20] D. I. Babić, K. Streubel, R. P. Mirin, N. M. Margalit, J. E. Bowers, E. L. Hu, D. E. Mars, L. Yang, and K. W. Carey, “Room-temperature continuous-wave operation of 1.54-um vertical-cavity lasers”, *IEEE Photonics Technology Letters*, vol. 7, no. 11, pp. 1225–1227, Nov. 1995.

[21] E. Towe, R. F. Leheny, and A. Yang, “A historical perspective of the development of the vertical-cavity surface-emitting laser”, *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 6, no. 6, pp. 1458–1464, Nov. 2000.

[22] CIR market Report # CIR-ODCm–V1-0714, *Revenue Opportunities for Optical Interconnects: Market and Technology Froecast-2013 to 2020 VOL II,* Available: http://cir-inc.com/news/cir-report-predicts-that-chip-level-optical-interconnect-market-will-genera

[23] K. Iga, “Vertical-Cavity Surface-Emitting Laser (VCSEL)”, *Proceedings of the IEEE*, vol. 101, no. 10, pp. 2229–2233, Oct. 2013.

[24] *Princeton Optronics,* Available: http://www.princetonoptronics.com/technology/technology.php#2

[25] F. E. Schubert, “Light-Emitting Diodes”, 2nd ed, New York, Cambridge University Press, 2006, pp. 122–161.

[26] R. Michalzik, "VCSEL Fundamentals", *VCSELs Fundamentals, Technology and Applications of Vertical-Cavity Surface-Emiting Lasers,* R. Michalzik Ed, Heidelberg, Springer, 2013, pp. 521–538.

[27] D. Kuchta, A. V. Rylyakov, C. L. Schow, J. Proesel, C. Baks, P. Westbergh, J. S. Gustavsson, and A. Larsson, "64 Gb/s Transmission over 57 m MMF using an NRZ Modulated 850 nm VCSEL", in *Proc. Optical Fiber Communication Conference*, Mar. 2014, pp. Th3C.2.

[28] J. A. Kash, A. F. Benner, F. E. Doany, D. M. Kuchta, B. G. Lee, P. K. Pepeljugoski, L. Schares, C. L. Schow, and M. Taubenblatt, "Optical interconnects in exascale supercomputers", in *Proc. IEEE 23rd Annual Meeting of thePhotonics Society*, Nov. 2010, pp. 483–484.

[29] B. Offrein, "Silicon Photonics packaging requirements", in *Proc. IBM Silicon Photon. Workshop*, 2011, pp. 1–l4.

[30] A. Vahdat, H. Liu, Z. Xiaoxue, and C. Johnson, "The Emerging Optical Data Center", in *Proc. Optical Fiber Communication Conference and National Fiber Optic Engineers Conference (OFC/NFOEC)*, Mar. 2011, pp. 1–3.

[31] F. Tan, M.-K. Wu, M. Liu, M. Feng, and N. Holonyak, "850 nm Oxide-VCSEL with Low Relative Intensity Noise and 40 Gb/s Error Free Data Transmission", *IEEE Photonics Technology Letters*, vol. 26, no. 3, pp. 289–292, Feb. 2014.

[32] P. Westbergh, E. P. Haglund, E. Haglund, R. Safaisini, J. S. Gustavsson, and A. Larsson, "High-speed 850 nm VCSELs operating error free up to 57 Gbit/s", *Electronics Letters*, vol. 49, no. 16, pp. 1021–1023, Aug. 2013.

[33] P. Moser, J. A. Lott, P. Wolf, G. Larisch, H. Li, and D. Bimberg, "Error-free 46 Gb/s operation of oxide-confined 980 nm VCSELs at 85°C", *Electronics Letters*, vol. 50, no. 19, Sep. 2014.

[34] H. Li, P. Wolf, P. Moser, G. Larisch, J. A. Lott, and D. Bimberg, "Energy-Efficient and Temperature-Stable 980 nm VCSELs for 35 Gb/s Error-Free Data Transmission at 85 °C with 139 fJ/bit Dissipated Heat", *IEEE Photonics Technology Letters*, vol. 26, no. 23, pp. 2349–2352, Dec. 2014.

[35] N. Suzuki, A. Takayoshi, H. Hatakeyama, K. Fukatsu, K. Yashiki, K. Tokutome, T. Akagawa, and M. Tsuji, "High speed 1.1-um-range InGaAs-based VCSELs", *IEICE transactions on electronics*, vol. 92, no. 7, pp. 942–950, 2009.

[36] R. H. Johnson and D. M. Kuchta, "30 Gb/s Directly Modulated 850 nm Datacom VCSELs", in *Proc.* May 2008, pp. CPDB2.

[37] S. B. Healy, E. P. O'Reilly, J. S. Gustavsson, P. Westbergh, Å. Haglund, A. Larsson, and A. Joel, "Active Region Design for High-Speed 850 nm VCSELs", *IEEE Journal of Quantum Electronics*, vol. 46, no. 4, pp. 506–512, Apr. 2010.

[38] P. Westbergh, J. S. Gustavsson, Å. Haglund, A. Larsson, F. Hopfer, G. Fiol, D. Bimberg, and A. Joel, "32 Gbit/s multimode fibre transmission using high-speed, low current density 850 nm VCSEL", *Electronics Letters*, vol. 45, no. 7, pp. 366–368, Mar. 2009.

[39] S. A. Blokhin, J. A. Lott, A. Mutig, G. Fiol, N. N. Ledentsov, M. V. Maximov, A. M. Nadtochiy, V. A. Shchukin, and D. Bimberg, "Oxide-confined 850 nm VCSELs operating at bit rates up to 40 Gbit/s", *Electronics Letters*, vol. 45, no. 10, pp. 501–503, May. 2009.

[40] P. Westbergh, J. S. Gustavsson, B. Kögel, Å. Haglund, A. Larsson, A. Mutig, A. Nadtochiy, D. Bimberg, and A. Joel, "40 Gbit/s error-free operation of oxide-confined 850 nm VCSEL", *Electronics Letters*, vol. 46, no. 14, pp. 1014–1016, Jul. 2010.

[41] Y.-C. Chang, C. S. Wang, and L. A. Coldren, "High-efficiency, high-speed VCSELs with 35 Gbit/s error-free operation", *Electronics Letters*, vol. 43, no. 19, pp. 1022–1023, Sep. 2007.

[42] W. Hofmann, P. Moser, P. Wolf, A. Mutig, M. Kroh, and D. Bimberg, "44 Gb/s VCSEL for optical interconnects", in *Proc. Optical Fiber Communication Conference and National Fiber Optic Engineers Conference (OFC/NFOEC)*, 2011, pp. 1–3.

[43] P. Wolf, P. Moser, G. Larisch, W. Hofmann, and D. Bimberg, "High-Speed and Temperature-Stable, Oxide-Confined 980 nm VCSELs for Optical Interconnects", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 19, no. 4, pp. 1701207–171207–7, Jul. 2013.

[44] N. Suzuki, H. Hatakeyama, K. Fukatsu, T. Anan, K. Yashiki, and M. Tsuji, "25-Gbps Operation of 1.1-um-Range InGaAs VCSELs for High-Speed Optical Interconnections", in *Proc. Optical Fiber Communication Conference and National Fiber Optic Engineers Conference*, 2006, pp. OFA4–OFA4–3.

[45] K. Yashiki, N. Suzuki, K. Fukatsu, T. Anan, H. Hatakeyama, and M. Tsuji, "1.1-μm-Range Low-Resistance InGaAs Quantum-Well Vertical-Cavity Surface-Emitting Lasers with a Buried Type-II Tunnel Junction", *Japanese Journal of Applied Physics*, vol. 46, no. 6L, pp. 512–514, May 2007.

[46] H. Hatakeyama, T. Anan, T. Akagawa, K. Fukatsu, N. Suzuki, K. Tokutome, and M. Tsuji, "Highly Reliable High-Speed 1.1 μm-Range VCSELs With InGaAs/GaAsP-MQWs", *IEEE Journal of Quantum Electronics*, vol. 46, no. 6, pp. 890–897, Jun. 2010.

[47] A. Mutig, J. A. Lott, S. A. Blokhin, P. Wolf, P. Moser, W. Hofmann, A. M. Nadtochiy, A. Payusov, and D. Bimberg, "Highly temperature-stable modulation characteristics of multioxide-aperture high-speed 980 nm vertical cavity surface emitting lasers", *Applied Physics Letters*, vol. 97, no. 15, pp. 151101–151101–3, Oct. 2010.

[48] P. Wolf, P. Moser, G. Larisch, M. Kroh, A. Mutig, W. Unrau, W. Hofmann, and D. Bimberg, "High-performance 980 nm VCSELs for 12.5 Gbit/s data transmission at 155 °C and 49 Gbit/s at -14 °C", *Electronics Letters*, vol. 48, no. 7, pp. 389–390, Mar. 2012.

[49] P. Westbergh, R. Safaisini, E. Haglund, J. Gustavsson, A. Larsson, M. Geen, R. Lawrence, and A. Joel, "High-Speed Oxide Confined 850 nm VCSELs Operating Error Free at 40 Gbit/s up to 85 °C", *IEEE Photonics Technology Letters*, vol. 25, no. 8, pp. 768–771, Apr. 2013.

[50] H. Li, P. Wolf, P. Moser, G. Larisch, A. Mutig, J. A. Lott, and D. Bimberg, "Energy-efficient and temperature-stable oxide-confined 980 nm VCSELs operating error-free at 38 Gbit/s at 85°C", *Electronics Letters*, vol. 50, no. 2, pp. 103–105, Jan. 2014.

[51] F. H. Peters and M. H. MacDougal, "High-speed high-temperature operation of vertical-cavity surface-emitting lasers", *IEEE Photonics Technology Letters*, vol. 13, no. 7, pp. 645–647, Jul. 2001.

[52] C.-K. Lin, A. Tandon, K. Djordjev, S. W. Corzine, and M. R. T. Tan, "High-Speed 985 nm Bottom-Emitting VCSEL Arrays for Chip-to-Chip Parallel Optical Interconnects", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 13, no. 5, pp. 1332–1339, Sep. 2007.

[53] A. Mutig, G. Fiol, P. Moser, F. Hopfer, M. Kuntz, V. A. Shchukin, N. N. Ledentsov, D. Bimberg, S. S. Mikhrin, I. L. Krestnikov, D. A. Livshits, and A. R. Kovsh, "120 °C 20 Gbit/s operation of 980 nm single mode VCSEL", in *Proc. IEEE 21st International Semiconductor Laser Conference (ISLC)*, Oct. 2008, pp. 9–10.

[54] P. Moser, P. Wolf, A. Mutig, G. Larisch, W. Unrau, W. Hofmann, and D. Bimberg, "85 °C error-free operation at 38 Gb/s of oxide-confined 980 nm vertical-cavity surface-emitting lasers", *Applied Physics Letters*, vol. 100, no. 8, pp. 081103–081103–3, Feb. 2012.

[55] H. Liu, C. F. Lam, and C. Johnson, "Scaling Optical Interconnects in Datacenter Networks Opportunities and Challenges for WDM", in *Proc. IEEE 18th Annual Symposium on High Performance Interconnects*, 2010, pp. 113–116.

[56] D. A. B. Miller, "Device Requirements for Optical Interconnects to Silicon Chips", *Proceedings of the IEEE*, vol. 97, no. 7, pp. 1166–1185, Jul. 2009.

[57] P. Moser, W. Hofmann, P. Wolf, J. A. Lott, G. Larisch, A. Payusov, N. N. Ledentsov, and D. Bimberg, "81 fJ/bit energy-to-data ratio of 850 nm vertical-cavity surface-emitting lasers for optical interconnects", *Applied Physics Letters*, vol. 98, no. 23, pp. 231106–231106–3, Jun. 2011.

[58] P. Wolf, P. Moser, G. Larisch, H. Li, J. A. Lott, and D. Bimberg, "Energy efficient 40 Gbit/s transmission with 850 nm VCSELs at 108 fJ/bit dissipated heat", *Electronics Letters*, vol. 49, no. 10, pp. 666–667, May. 2013.

[59] H. Li, P. Wolf, P. Moser, G. Larisch, J. A. Lott, and D. Bimberg, "Temperature-Stable, Energy-Efficient and High-Speed Oxide-Confined 980 nm VCSELs for Optical Interconnects", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 21, no. 6, pp. 1700409–1700409–9, Nov./Dec. 2015.

[60] Y. Suematsu and K. Iga, "Semiconductor laser development and its impact", in *Proc. 36th European Conference and Exhibition onptical Communication (ECOC)*, 2010, pp. 1–7.

[61] M. Grabherr, H. Moench, and A. Pruijmboom, "VCSELs for optical mice and sensing", *VCSELs Fundamentals, Technologyand Applications of Vertical-Cavity Surface-Emiting Lasers,* R. Michalzik Ed, Heidelberg, Springer, 2013, pp. 521–538.

[62] N. Ueki and N. Mukoyama, "VCSEL-based Lser Printing System", *VCSELs Fundamentals, Technologyand Applications of Vertical-Cavity Surface-Emiting Lasers,* R. Michalzik Ed, Heidelberg, Springer, 2013, pp. 539–548.

[63] N. Ueki, H. Teyuka, and A. Ota, "Vertical-cavity Surface-emitting Laser Diode (VCSEL)-VCSEL array and its application to the copier", *J. Imaging Soc. Jpn,* vol. 44, no. 3, pp. 149–155, 2005.

[64] N. Mukoyama, H. Otoma, J. Sakurai, N. Ueki, and H. Nakayama, "VCSEL array-based light exposure system for laser printing", in *Proc. SPIE 6908 Vertical-Cavity Surface-Emitting Lasers XII*, 2008, pp. 69080H–69080H–11.

[65] *VCSEL-ROS,* Available: http://www.fujixerox.com/eng/company/technology/vcsel_ros/

[66] H. Otoma, A. Murakami, Y. Kuwata, N. Ueki, N. Mukoyama, T. Kondo, A. Sakamoto, S. Omori, H. Nakayama, and T. Nakamura, "Single-Mode Oxide-Confined VCSEL for Printers and Sensors", in *Proc. Ist Electronics Systemintegration Technology Conference*, 2006, pp. 80–85.

[67] S. W. Corzine, R. S. Geels, J. W. Scott, R.-H. Yan, and L. A. Clodren, "Design of Fabry-Perot surface-emitting lasers with a Periodic Gain Structure", *IEEE Journal of Quantum Electronics*, vol. 25, no. 6, pp. 1513–1523, Jun. 1989.

[68] R. Michalzik and K.J. Ebeling, "Operating Princles of VCSELs", *Vertical-Cavity Surface-Emitting Laser Device,* H. Li and K. Iga Ed, Heidelberg, Springer, 2003, pp. 53–93.

[69] L.A. Coldren and S. W. Corzine, "Diode lasers and photonic integrated circuits", 2nd ed, Ed, New York, Wiley, 1995, pp. 195–245.

[70] P. Westbergh, "High Speed Vertical Cavity Surface Emitting Lasers for Short Reach Communication", *Dissertation*, Chalmers University of Technology, Göteborg, Sweden, Apr. 2011.

[71] Y. Satuby and M. Orenstein, "Mode-coupling effects on the small-signal modulation of multitransverse-mode vertical-cavity semiconductor lasers", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 35, no. 6, pp. 944–954, Jun. 1999.

[72] L.-G. Zei, S. Ebers, J.-R. Kropp, and K. Petermann, "Noise performance of multimode VCSELs", *Journal of Lightwave Technology*, vol. 19, no. 6, pp. 884–892, Jun. 2001.

[73] Y.-C. Chang, "Engineering vertical-cavity surface-emitting lasers for high-speed operation", *Dissertation*, University of California Santa Barbara, USA, Dec. 2008.

[74] D. Tauber, G. Wang, R. S. Geels, J. E. Bowers, and L. A. Coldren, "Large and small signal dynamics of vertical cavity surface emitting lasers", *Applied Physics Letters*, vol. 62, no. 4, pp. 325–327, 1993.

[75] T. R. Chen, B. Zhao, L. Eng, Y. H. Zhuang, J. O'Brien, and A. Yariv, "Very high modulation efficiency of ultralow threshold current single quantum well InGaAs lasers", *Electronics Letters*, vol. 29, no. 17, pp. 1525–1526, Aug. 1993.

[76] J. W. Matthews and A. E. Blakeslee, "Defects in epitaxial multilayers: I. Misfit dislocations", *Journal of Crystal Growth*, vol. 27, no. 0, pp. 118–125, 1974.

[77] S. Adachi, "Properties of Semiconductor Alloys: Group-IV, III-V and II-VI Semiconductors", Great Britain, John Wiley & Sons, 2009, pp. 9–97.

[78] I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, "Band parameters for III–V compound semiconductors and their alloys", *Journal of Applied Physics*, vol. 89, no. 11, pp. 5815–5875, Feb. 2001.

[79] C. G. Van de Walle, "Band lineups and deformation potentials in the model-solid theory", *Physical Review B*, vol. 39, no. 3, pp. 1871–1883, Jan. 1989.

[80] S. L. Chuang, "Physics of optoelectronic devices", 2nd ed, New York, Wiley, 1995, pp. 655–671.

[81] J.-W. Pan and J.-I. Chyi, "Theoretical study of the temperature dependence of 1.3-um AlGaInAs-InP multiple-quantum-well lasers", *IEEE Journal of Quantum Electronics*, vol. 32, no. 12, pp. 2133–2138, Dec. 1996.

[82] T. Fujisawa, T. Sato, M. Mitsuhara, T. Kakitsuka, T. Yamanaka, Y. Kondo, and F. Kano, "Successful Application of the 8-band Theory to Optical Properties of Highly Strained In(Ga)As/InGaAs Quantum Wells With Strong Conduction-Valence Band Coupling", *IEEE Journal of Quantum Electronics*, vol. 45, no. 9, pp. 1183–1191, Sep. 2009.

[83] S. L. Chuang, "Efficient band-structure calculations of strained quantum wells", *Physical Review B*, vol. 43, no. 12, pp. 9649–9661, Apr. 1991.

[84] *Crosslight,* Available: http://crosslight.com/products/pics3d/

[85] A. Mutig and D. Bimberg, "Progress on high-speed 980 nm VCSELs for short-reach optical interconnects", *Advances in Optical Technologies*, vol. 2011, pp. 1–15, Jun. 2011.

[86] Y.-C. Chang and L. A. Coldren, "Efficient, High-Data-Rate, Tapered Oxide-Aperture Vertical-Cavity Surface-Emitting Lasers", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 15, no. 3, pp. 704–715, May. 2009.

[87] R. Safaisini, J. R. Joseph, and K. L. Lear, "Scalable high-CW-power high-speed 980 nm VCSEL arrays", *IEEE Journal of Quantum Electronics*, vol. 46, no. 11, pp. 1590–1596, Nov. 2010.

[88] J. Tignon, O. Heller, P. Roussignol, G. Bastard, C. Piermarrochi, R. Planel, and V. Thierry-Mieg, "Carrier dynamics in shallow GaAs/AlGaAs quantum wells", *Physica E: Low-dimensional Systems and Nanostructures*, vol. 2, no. 1–4, pp. 126–130, 1998.

[89] C. Chen, P. O. Leisher, A. A. Allerman, K. M. Geib, and K. D. Choquette, "Temperature Analysis of Threshold Current in Infrared Vertical-Cavity Surface-Emitting Lasers", *IEEE Journal of Quantum Electronics*, vol. 42, no. 10, pp. 1078–1083, Oct. 2006.

[90] D. Lancefield, A. R. Adams, A. T. Meney, W. Knap, E. Litwin-Staszewska, C. Skierbiszewski, and J. L. Robert, "The light-hole mass in a strained InGaAs/GaAs single quantum well and its pressure dependence", *Journal of Physics and Chemistry of Solids*, vol. 56, no. 3–4, pp. 469–473, Jan. 1995.

[91] Y.-A. Chang, J.-R. Chen, H.-C. Kuo, Y.-K. Kuo, and S.-C. Wang, "Theoretical and experimental analysis on InAlGaAs/AlGaAs active region of 850 nm vertical-cavity surface-emitting lasers", *Journal of Lightwave Technology*, vol. 24, no. 1, pp. 536–543, Jan. 2006.

[92] N. K. Dutta, W. S. Hobson, D. Vakhshoori, H. Han, P. N. Freeman, De Jong, J. F, and J. Lopata, "Strain compensated InGaAs-GaAsP-InGaP laser", *IEEE Photonics Technology Letters*, vol. 8, no. 7, pp. 852–854, Jul. 1996.

[93] W. W. Chow, K. D. Choquette, M. H. Crawford, K. L. Lear, and G. R. Hadley, "Design, fabrication, and performance of infrared and visible vertical-cavity surface-emitting lasers", *IEEE Journal of Quantum Electronics*, vol. 33, no. 10, pp. 1810–1824, Oct. 1997.

[94] K. Tai, L. Yang, Y. H. Wang, J. D. Wynn, and A. Y. Cho, "Drastic reduction of series resistance in doped semiconductor distributed Bragg reflectors for surface-emitting lasers", *Applied Physics Letters*, vol. 56, no. 25, pp. 2496–2498, Apr. 1990.

[95] B. H. Na, Y. M. Song, K. M. Park, K. S. Chang, and Y. T. Lee, "Low resistance uniparabolic graded distributed Bragg reflectors using digital alloy", in *Proc. The Optical Society of Korea Summer Meeting*, 2008, pp. 247–248.

[96] E. F. Schubert, L. W. Tu, G. J. Zydzik, R. F. Kopf, A. Benvenuti, and M. R. Pinto, "Elimination of heterojunction band discontinuities by modulation doping", *Applied Physics Letters*, vol. 60, no. 4, pp. 466–468, Nov. 1992.

[97] *Nextnano,* Available: http://www.nextnano.de/

[98] D. B. Young, J. W. Scott, F. H. Peters, M. G. Peters, M. L. Majewski, B. J. Thibeault, S. W. Corzine, and L. A. Coldren, "Enhanced performance of offset-gain high-barrier vertical-cavity surface-emitting lasers", *IEEE Journal of Quantum Electronics*, vol. 29, no. 6, pp. 2013–2022, Jun. 1993.

[99] E. S. Bjorlin, J. Geske, M. Mehta, J. Piprek, and J. E. Bowers, "Temperature dependence of the relaxation resonance frequency of long-wavelength vertical-cavity lasers", *IEEE Photonics Technology Letters*, vol. 17, no. 5, pp. 944–946, May 2005.

[100] T. Flick, K. H. Becks, J. Dopke, P. Mättig, and P. Tepel, "Measurement of the thermal resistance of VCSEL devices", *Journal of Instrumentation*, vol. 6, pp. 1–5, Jan. 2001.

[101] M. Osiński and W. Nakwaski, "Effective thermal conductivity analysis of 1.55 μm InGaAsP/InP vertical-cavity top-surface-emitting microlasers", *Electronics Letters*, vol. 29, no. 11, pp. 1015–1016, May. 1993.

[102] H. K. Lee, Y. M. Song, Y. T. Lee, and J. S. Yu, "Thermal analysis of asymmetric intracavity-contacted oxide-aperture VCSELs for efficient heat dissipation", *Solid-State Electronics*, vol. 53, no. 10, pp. 1086–1091, Jul. 2009.

[103] C. Webb and J. Julian, "Handbook of Laser Technology and Applications: Laser design and laser systems", *Vertical-cavity surface-emitting lasers,* Ed. CRC Press, 2004, pp. 673–688.

[104] J. Piprek, "Electro-Thermal Analysis of Oxide-Confined Vertical-Cavity Lasers", *physica status solidi (a)*, vol. 188, no. 3, pp. 905–912, 2001.

[105] S. Adachi, "Lattice thermal conductivity of group-IV and III–V semiconductor alloys", *Journal of Applied Physics*, vol. 102, no. 6, pp. 063502–063502–7, Sep. 2007.

[106] W. Nakwaski, "Thermal conductivity of binary, ternary, and quaternary III-V compounds", *Journal of Applied Physics*, vol. 64, no. 1, pp. 159–166, 1988.

[107] H. Li, P. Moser, P. Wolf, G. Larisch, L. Frasunkiewicz, M. Dems, T. Czyszanowski, J. A. Lott, and D. Bimberg, "Energy efficiency, bit rate, and modal properties of 980 nm VCSELs for very-short-reach optical interconnects", *in proc. SPIE 9001 on Vertical-Cavity Surface-Emitting Lasers XVIII*, Feb. 2014, pp. 900110B–90010B–8.

[108] E. Haglund, Å. Haglund, P. Westbergh, J. S. Gustavsson, B. Kögel, and A. Larsson, "25 Gbit/s transmission over 500 m multimode fibre using 850 nm VCSEL with integrated mode filter", *Electronics Letters*, vol. 48, no. 9, pp. 517–519, Apr. 2012.

[109] M. J. Noble, J.-H. Shin, K. D. Choquette, J. A. Lott, and Y.-H. Lee, "Calculation and measurement of resonant-mode blueshifts in oxide-apertured VCSELs", *IEEE Photonics Technology Letters*, vol. 10, no. 4, pp. 475–477, Apr. 1998.

[110] P. Westbergh, J. S. Gustavsson, B. Kögel, Å. Haglund, A. Larsson, and A. Joel, "Speed enhancement of VCSELs by photon lifetime reduction", *Electronics Letters*, vol. 46, no. 13, pp. 938–940, Jun. 2010.

[111] P. Westbergh, J. S. Gustavsson, B. Kögel, Å. Haglund, and A. Larsson, "Impact of Photon Lifetime on High-Speed VCSEL Performance", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 17, no. 6, pp. 1603–1613, Nov. 2011.

[112] *Electron-beam lithography,* Available: http://en.wikipedia.org/wiki/Electron-beam_lithography

[113] M. Ahmad, *N-Methyl-2-pyrrolidone (NMP) (Microposit Stripper 1165),* Available: http://www3.imperial.ac.uk/pls/portallive/docs/1/7276130.PDF

[114] A. P. Nayak, L. V. Jay, and M. S. Islam, *Wet and Dry Etching,* Available: http://web.ece.ucdavis.edu/~anayakpr/Papers/Wet%20and%20Dry%20Etching_submitted.pdf

[115] *Solaris 150 Rapid Thermal Processing System,* Available: http://www.ssintegration.com/rtp.html

[116] *SSI Solaris 150 RTA,* Available: http://nrf.aux.eng.ufl.edu/_files/documents/411.pdf

[117] *Keithley 2400-LV SourceMeter,* Available: http://www.keithley.com/products/dcac/specialtysystems/optoelectronics/?mn=2400-LV

[118] *Temptronic TP03010B ThermoChuck,* Available: http://de.caeonline.com/listing/product/9013096/temptronic-tp03010b-2100-1

[119] *Models 141X, 143X, 144X & 145X Fiber-coupled, ultrahigh-speed photodetector modules User's Manual,* Available: http://assets.newport.com/webDocuments-EN/images/15167.PDF

[120] *New Focus 1434 25-GHz Photodetector,* Available: http://assetrelay.com/shop/optical-heads/1361-new-focus–1434-25-ghz-photodetector.html

[121] A. Bacou, A. Hayat, A. Rissons, V. Iakovlev, A. Syrbu, J. Mollier, and E. Kapon, "VCSEL Intrinsic Response Extraction Using T-Matrix Formalism", *IEEE Photonics Technology Letters*, vol. 21, no. 14, pp. 957–959, Jul. 2009.

[122] Y.-C. Chang and L. A. Coldren, "High-efficiency, high-speed VCSELs for optical interconnects", *Applied Physics A*, vol. 95, no. 4, pp. 1033–1037, Feb. 2009.

[123] D. Collins, N. Li, D. Kuchta, F. Doany, C. Schow, C. J. Helms, and L. Yang, "Development of high-speed VCSELs: 10 Gb/s serial links and beyond", in *Proc. SPIE 6908 Vertical-Cavity Surface-Emitting Lasers XII*, Jan. 2008, pp. 690809–690809–9.

[124] A. F. Benner, M. Ignatowski, J. A. Kash, D. M. Kuchta, and M. B. Ritter, "Exploitation of optical interconnects in future server architectures", *IBM Journal of Research and Development*, vol. 49, no. 4.5, pp. 755–775, Jul. 2005.

[125] E. Kapon and A. Sirbu, "Long-wavelength VCSELs: Power-efficient answer", *Nature Photonics*, vol. 3, no. 1, pp. 27–29, Jan. 2009.

[126] A. Larsson, J. Gustavsson, Å. Haglund, and P. Westbergh, "Advances in VCSELs for communication and sensing", in *Proc. IEEE 22nd InternationalSemiconductor Laser Conference (ISLC)*, 2010, pp. 1–2.

[127] Y. Ou, J. S. Gustavsson, P. Westbergh, Å. Haglund, A. Larsson, and A. Joel, "Impedance Characteristics and Parasitic Speed Limitations of High-Speed 850 nm VCSELs", *IEEE Photonics Technology Letters*, vol. 21, no. 24, pp. 1840–1842, Dec. 2009.

[128] M. J. Miah, A. Al-Samaneh, A. Kern, D. Wahl, P. Debernardi, and R. Michalzik, "Fabrication and Characterization of Low-Threshold Polarization-Stable VCSELs for Cs-Based Miniaturized Atomic Clocks", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 19, no. 4, pp. 1701410–1701410–10, Jul. 2013.

[129] A. N. Al-Omari, I. K. Al-Kofahi, and K. L. Lear, "Fabrication, performance and parasitic parameter extraction of 850 nm high-speed vertical-cavity lasers", *Semiconductor Science and Technology*, vol. 24, no. 9, pp. 095024–095024–8, Aug. 2009.

[130] J. J. Gao, "High Frequency Modeling and Parameter Extraction for Vertical-Cavity Surface Emitting Lasers", *Journal of Lightwave Technology*, vol. 30, no. 11, pp. 1757–1763, Jun. 2012.

[131] E. Barsoukov and J. R. MacDonald, "Fundamental of Impedance spectroscopy", *Impedance spectroscopy: theory, experiment, and applications,* 2nd ed., E. Barsoukov and J. R. Macdonald Ed, New Jersey, John Wiley & Sons, 2005, pp. 1–20.

[132] *Fibre Channel Roadmaps v1.8,* Available: http://fibrechannel.org/fibre-channel-roadmaps.html

[133] M. C. Tatham, I. F. Lealman, C. P. Seltzer, L. D. Westbrook, and D. M. Cooper, "Resonance frequency, damping, and differential gain in 1.5 μm multiple quantum-well lasers", *IEEE Journal of Quantum Electronics*, vol. 28, no. 2, pp. 408–414, Feb. 1992.

[134] R. Johnson, *Experiments in Measuring Laser RIN with an Oscilloscope,* Available: ftp://www.t11.org/t11./pub/fc/msqs-2/11-405v0.pdf

[135] D. Coleman, *Optical Trends in the Data Center,* Available: http://www.bicsi.org/uploadedfiles/bicsi_conferences/canada/2012/presentations/concses_2a.pdf

[136] L. A. Graham, H. Chen, D. Gazula, T. Gray, J. K. Guenter, B. Hawkins, R. Johnson, C. Kocot, A. N. MacInnes, G. D. Landry, and J. A. Tatum, "The next generation of high speed VCSELs at Finisar", in *Proc.* 2012, pp. 827602–827602–10.

[137] J. A. Tatum, *VCSEL Based 32GFC Data links,* Available: http://www.t11.org/ftp/t11/pub/fc/pi-5/10-268v0.pdf

[138] D. Bimberg, "Ultrafast VCSELs for datacom", *IEEE Photonics Journal*, vol. 2, no. 2, pp. 273–275, Apr. 2010.

[139] C. H. Wu, F. Tan, M. K. Wu, M. Feng, and N. Holonyak, "The effect of microcavity laser recombination lifetime on microwave bandwidth and eye-diagram signal integrity", *Journal of Applied Physics*, vol. 109, no. 5, pp. 053112–053112–9, Mar. 2011.

[140] M. A. Taubenblatt, "Optical Interconnects for High-Performance Computing", *Journal of Lightwave Technology*, vol. 30, no. 4, pp. 448–457, Feb. 2012.

[141] H. Li, P. Wolf, P. Moser, G. Larisch, A. Mutig, J. A. Lott, and D. Bimberg, "Impact of the quantum well gain-to-cavity etalon wavelength offset on the high temperature performance of high bit-rate 980 nm VCSELs", *IEEE Journal of Quantum Electronics*, vol. 50, no. 8, pp. 613–621, Aug. 2014.

[142] P. Moser, P. Wolf, G. Larisch, H. Li, J. A. Lott, and D. Bimberg, "Energy-efficient oxide-confined high-speed VCSELs for optical interconnects", in *Proc. SPIE 9001 Vertical-Cavity Surface-Emitting Lasers XVIII*, Feb. 2014, pp. 900103–900103–8.

[143] W. Nakwaski and M. Osiński, "Thermal resistance of top-surface-emitting vertical-cavity semiconductor lasers and monolithic two-dimensional arrays", *Electronics Letters*, vol. 28, no. 6, pp. 572–574, Mar. 1992.

[144] A. N. Al-Omari, G. P. Carey, S. Hallstein, J. P. Watson, G. Dang, and K. L. Lear, "Low thermal resistance high-speed top-emitting 980 nm VCSELs", *IEEE Photonics Technology Letters*, vol. 18, no. 11, pp. 1225–1227, Jun. 2006.

[145] T. Wipiejewski, D. B. Young, M. G. Peters, B. J. Thibeault, and L. A. Coldren, "Improved performance of vertical-cavity surface-emitting laser diodes with Au-plated heat spreading layer", *Electronics Letters*, vol. 31, no. 4, pp. 279–281, Feb. 1995.

[146] G. Zhao and D. G. Deppe, "Thermal performance of oxide-free lithographic VCSELs", in *Proc. Photonics Conference (PHO), 2011 IEEE*, 2011, pp. 915–916.

[147] B. M. Hawkins, R. A. Hawthorne III, J. K. Guenter, J. A. Tatum, and J. R. Biard, "Reliability of various size oxide aperture VCSELs", in *Proc. 52nd Electronic Components and Technology Conference*, 2002, pp. 540–550.

[148] Y.-C. Chang and L. A. Coldren, "Optimization of VCSEL structure for high-speed operation", in *Proc. IEEE 21st International Semiconductor Laser Conference*, Sep. 2008, pp. 159-160.

[149] H. Dalir and F. Koyama, "29 GHz directly modulated 980 nm vertical-cavity surface emitting lasers with bow-tie shape transverse coupled cavity", *Applied Physics Letters*, vol. 103, no. 9, p. 091109, Aug. 2013.

[150] P. Moser, J. A. Lott, P. Wolf, G. Larisch, H. Li, N. N. Ledentsov, and D. Bimberg, "56 fJ dissipated energy per bit of oxide-confined 850 nm VCSELs operating at 25 Gbit/s", *Electronics Letters*, vol. 48, no. 20, pp. 1292–1294, Sep. 2012.

Appendix A

High Bit-Rate VCSEL Process Flow

I. Sample preparation

1. Cleave a VCSEL 76.2 mm-diameter epitaxial wafer into quarters

II. Top-metal deposition

1. Solvent clean: Acetone (5 min @ RT), Isopropanol (5 min @ RT) clean and N_2 dry
2. Dehydration bake: hot plate 120°C, 5 min
3. Spin negative photoresist MaN-1420: 3000 rpm, 30 s, and edge bead removal
4. Post-bake: hot plate 100 °C, 2 min, wait ≥ 10 min
5. Expose: 60 s (6 mW/cm^2), wait ≥ 5 min
6. Develop: MaD 533S, 50 s; Stop water one (20 s), stop water two (30 s), DI rinse and N_2 dry
7. O_2 plasma descum: 150 W, 3 min
8. Dip: HCl (37 %): H_2O = 1 : 4 (15 mL/ 60 mL), 15 s; N_2 dry
9. Deposit metal: E-beam evaporation system
   a. Ti: 20 nm @ 0.5 Å/s
   b. Pt: 50 nm @ 0.5 Å/s
   c. Au: 300 nm @ 1 Å/s
10. Lift-off: N-Methyl-2-pyrrolidinone (NMP) (Microposit Stripper 1165), hot plate 75 °C, 50 min, water to remove NMP, and N_2 dry

III. Mesa one etch

1. Solvent clean: Acetone (5 min @ RT), Isopropanol (5 min @ RT) clean and N_2 dry
2. Dehydration bake: hot plate 120 °C, 5 min
3. Spin HMDS: 2000 rpm, 30 s
4. Bake: hot plate 90 °C, 3 min
5. Spin positive photoresist AZ MIR 701: 1000/ 3000 rpm, 2/ 40 s, and edge bead removal
6. Bake: hot plate 90°C, 2 min, wait ≥ 10 min
7. Expose: 35 s, wait ≥ 5 min

8. Develop: AZ 726 MIF, 40 s; Stop water one (20 s), stop water two (30 s), DI rinse and N_2 dry
9. O_2 plasma descum: 150 W, 3 min
10. Etch: ICP-RIE, sample with oil on AlO_x Chuck, Cl_2 @ 2.5 sccm, BCl_3 @ 12.5 sccm, Reactor Pressure: 0.33 Pa, RF-Generator: 30 W, Source: 500 W, in-situ etch depth control with Nanomess
11. Clean: Acetone/ Isopropanol solvent clean to remove oil
12. Photoresist etch mask removal: NMP, hot plate 75 °C, 50 min, water to remove NMP, and N_2 dry
13. O_2 plasma descum: 600 W, 5 min

IV. Oxidation

1. Calibrate oxidation time with dummy samples
2. Remove native oxide: AZ MIF 726, 5 min, Stop water one (20 s), stop water two (30 S), DI rinse and N_2 dry, immediately to furnace
3. Oxidize: furnace 420 °C, N_2 flow: 0.8 Liter/min, H_2O flow: 0.8 Liter/min, Pressure: 50 mbar, with in-situ control

V Mesa two etch

1. Solvent clean: Acetone (5 min @ RT), Isopropanol (5 min @ RT) clean and N_2 dry
2. Spin positive photoresist AZ 4562: 4000 rpm, 30 s, and edge bead removal, wait 5 min
3. Bake: hot plate 100 °C, 7 min, wait ≥10 min
4. Expose: 150 s, wait ≥ 10 min
5. Develop: AZ 351B: H_2O= (1 : 4), 140 s; Stop water one (10 s), stop water two (5 s), DI rinse and N_2 dry
6. O_2 plasma descum: 150 W, 3 min
7. Etch: ICP-RIE, sample with oil on AlO_x Chuck, Cl_2 @ 2.5 sccm, BCl_3 @ 12.5 sccm, Reactor Pressure: 0.33 Pa, RF-Generator: 30 W, Source: 500 W, in-situ etch depth control with Nanomess
8. Clean: Acetone/ Isopropanol solvent clean to remove oil
9. Photoresist removal: NMP, hot plate 75 °C, 50 min, water to remove NMP, and N_2 dry
10. O_2 plasma descum: 600 W, 5 min

VI. Bottom-metal deposition

1. Solvent clean: Acetone (5 min @ RT), Isopropanol (5 min @ RT) clean and N_2 dry
2. Dehydration bake: hot plate 120 °C, 5 min, wait 1 min
3. Spin negative photoresist MaN-490: 700/ 2500 rpm, 5 /40 s, and edge bead removal
4. Postbake: hot plate 100 °C, 14 min, wait ≥ 20 min
5. Expose: 150 s (6 mW/cm^2), wait ≥ 20 min
6. Develop: MaD 532S, 8 min; Stop water one (20 S), stop water two (20 S), DI rinse and N_2 dry
7. O_2 plasma descum: 150 W, 3 min
8. Dip: HCl (37 %): H_2O = 1 : 4 (15 mL/ 60 mL), 15 s; N_2 dry
9. Deposit metal: Vecco evaporation system
   a. Ni: 20 nm
   b. Au/Ge: 88/12 nm
   c. Au: 300 nm
10. Lift-off: NMP, hot plate 75 °C, 50 min, water to remove NMP, and N_2 dry
11. Annealing: RTA, 380 °C, 60 s

VII. BCB Planarization

1. Warmup BCB at least 1 hour
2. Solvent clean: Acetone (5 min @ RT), Isopropanol (5 min @ RT) clean and N_2 dry
3. Dry: 4000 rpm, 90 s
4. Spin adhesion promotor AP3000: 3000 rpm, 20 s
5. Spin photo BCB 4026–46: 700/ 3000 rpm, 10/ 40 s, edge bead removal, wait 1 min
6. Bake: hot plate 80 °C, 90 s
7. Expose: 50 s (CP mode without UV filter)
8. Develop: DS3000, 35 °C, 10 min
9. Develop: DS3000, RT, 90 s
10. Cure BCB: N_2 flow, 500-600 mbar
11. BCB etch: O_2 @ 13.75 sccm, CF_4 @ 11.25 sccm, Reactor Pressure: 20 Pa, RF-Generator: 50 W

VIII. GSG Pad metal deposition

1. Solvent clean: Acetone (5 min @ RT), Isopropanol (5 min @ RT) clean and N_2 dry
2. Dehydration bake: hot plate 120 °C, 5 min

3. Spin negative photoresist MaN-1440: 3000 rpm, 30 s, and edge bead removal
4. Post-bake: hot plate 90 °C, 5 min, wait ≥ 5 min
5. Expose: 24 s (6 mW/cm^2), wait ≥ 5 min
6. Develop: MaD 533S, 90 s; Stop water one (20 S), stop water two (20 S), DI rinse and N_2 dry
7. O_2 plasma descum: 150 W, 3 min
8. Dip: HCl (37 %): H_2O = 1 : 4 (15 mL/ 60 mL), 15 s; N_2 dry
9. Deposit metal: E-beam evaporation system
   a. Cr: 50 nm @ 0.5 Å/s
   b. Pt: 50 nm @ 0.5 Å/s
   c. Au: 300 nm @ 1 Å/s
10. Lift-off: NMP, hot plate 75 °C, 50 min, water to remove NMP, and N_2 dry

Appendix B

Abbreviations

BCB	bisbenzo-cyclobutene
BER	bit error ratio
BTB	back-to-back
CW	continuous wave
DBR	distributed Bragg reflector
EDR	electrical energy-to-data ratio
EEL	edge-emitting laser
ESA	electrical spectrum analyzer
GSG	ground-signal-ground
HBR	dissipated heat-to-bit rate ratio
ICP-RIE	inductively coupled plasma reactive ion etching
LIV	light output power-current-voltage
MBE	molecular beam epitaxy
MCEF	modulation current efficiency factor
MOCVD	metal-organic chemical vapor deposition
NMP	N-Methyl-2-pyrrolidinone
NRZ	non-return-to-zero
QW	quantum well
OSA	optical spectrum analyzer
PECVD	plasma-enhanced chemical vapor deposition
PRBS	pseudorandom binary sequence
PD	photodetector
RF	radio frequency
RIE	reactive ion etching
RIN	relative intensity noise
RTA	rapid thermal annealing
SEM	scanning electron microscope (or microscopy)
SMF	single mode fiber
SMSR	side-mode-suppression ratio
S/N	signal-to-noise ratio
MMF	multimode fiber
VCSEL	vertical-cavity surface-emitting laser
VNA	vector network analyzer

Appendix C

Symbols

α_i	internal loss (cm^{-1})
R_t	top-mirror power reflectance (unitless)
R_b	bottom-mirror power reflectance (unitless)
L_{eff}	effective resonator length (nm)
L	cavity length (nm)
Γ	optical confinement factor (unitless)
g	gain (cm^{-1})
g_{th}	threshold gain (cm^{-1})
g_0	gain coefficient (cm^{-1})
ε	gain compression factor (unitless)
N	carrier density (cm^{-3})
N_{tr}	transparency carrier density (cm^{-3})
N_p	photon density (cm^{-3})
q	electron charge (C)
τ	carrier lifetime (s)
τ_p	photon lifetime (s)
η_d	differential quantum efficiency (W/A)
η_i	current injection efficiency (unitless)
V	volume of active region (cm^3)
V_p	mode volume (cm^3)
v_g	group velocity of the lasing mode (cm^{-1})
$H(f)$	transfer function (dB)
f_R	relaxation resonance frequency (GHz)
γ	damping factor (s^{-1})
f_{-3dB}	−3 dB modulation bandwidth (GHz)
f_P	parasitic cut-off frequency (GHz)
I	bias current (mA)
I_{th}	threshold current (mA)
J_{th}	threshold current density (Acm^{-2})
V	bias voltage (Volts)
P_{th}	threshold electrical power (mW)
P_{el}	input CW electrical power (mW)
R_{th}	thermal resistance (K/mW)

Acknowledgments

First of all, I would like to express my sincere gratitude to my advisor Prof. Dr. Dieter Bimberg for his continuous support of my PhD study and research, and for his patience, guidance, motivation, enthusiasm, and encouragement along the way. Prof. Bimberg showed me the importance of both optimism and courage to grasp opportunities by taking risks and challenges, and what I learned from Prof. Bimberg is priceless to my future. His guidance helped me throughout the entire duration of my research. I could not have imagined having a better advisor and mentor. I am very grateful to Prof. Dr. Gadi Eisenstein for reviewing my dissertation. Many thanks to Prof. Dr. Michael Lehmann for taking on the chair of the dissertation committee.

I would like to give my warmest thanks to my colleagues, Philip Wolf, Philip Moser, and Gunter Larisch, who patiently guided me off to a smooth start from the very first day. Nothing in this thesis could have been done without their great efforts. I would also like to thank all of my former and current colleagues in Prof. Bimberg's group. I have been honored getting to know you wonderful people.

I am very grateful to Prof. Dr. James A. Lott for all of his patient help, valuable advice, and interesting discussions on physics, philosophy, and life. As one of the world's famous professors and pioneering scientists on the topic of VCSELs, Prof. Lott always likes to help young scientists, and I will forever value his encouragement, his desire for me to always do my best work, his constant assurance that I am able to go well beyond what I though I was capable of, his extensive review of manuscripts, his help with English, and his intense, and highly nontrivial lectures and lessons on VCSELs. I really have learned a lot from Prof. Lott, especially about his professional way of doing things in all aspects.

I would also like to thank all the people of the Center of Nanophotonics, for sharing the equipment, for keeping such a nice laboratory, and for all of the much-appreciated assistance. I give my special thanks to Stefan Bock.

I want to thank all my Chinese friends in Berlin for their continuous help and companionship. I must express my special gratitude to Xingwei An, Nan Zhu, and Ye Zhu for teaching me to cook Chinese food, and for helping me to survive and enjoy my life in Berlin. Many thanks to my neighbors, Quan Liu, Xiaobei Ma, and Juan Liu. We have been like a family all the time.

I give my gratitude to the China Scholarship Council (CSC) for financial support.

Last and foremost, to my family, thank you for always being with me and for supporting me. I love you all.

Berlin, 30 May 2015

Hui Li

List of Publications

[1] **H. Li**, P. Wolf, P. Moser, G. Larisch, J. A. Lott, and D. Bimberg, "Temperature-Stable, Energy-Efficient and High-Speed Oxide-Confined 980 nm VCSELs for Optical Interconnects," *IEEE J. Sel. Top. Quant. Electron.* vol. 21, no. 6, pp. 1700409–1–9, Nov./Dec. 2015.

[2] **H. Li**, P. Wolf, P. Moser, G. Larisch, A. Mutig, J. A. Lott, and D. Bimberg, "Impact of the quantum well gain-to-cavity etalon wavelength offset on the high temperature performance of high bit-rate 980 nm VCSELs," *IEEE J. Quantum Electron.*, vol. 50, no. 8, 613–621, Aug. 2014.

[3] **H. Li**, P. Wolf, P. Moser, G. Larisch, J. A. Lott, and D. Bimberg, "Temperature-Stable 980 nm VCSELs for 35 Gb/s Operation at 85 °C with 139 fJ/bit Dissipated Heat," *IEEE Photon. Technol. Lett.*, vol. 26, no. 23, pp. 2349–2352, Dec. 2014.

[4] **H. Li**, J. A. Lott, P. Wolf, P. Moser, G. Larisch, and D. Bimberg, "Temperature-Dependent Impedance Characteristics of Temperature-Stable High-Speed 980 nm VCSELs," *IEEE Photon. Technol. Lett.*, vol. 26, no. 23, pp. 832–835, Apr. 2015.

[5] **H. Li**, P. Wolf, P. Moser, G. Larisch, A. Mutig, J. A. Lott, and D. Bimberg, "Energy-efficient and temperature-stable oxide-confined 980 nm VCSELs operating error-free at 38 Gbit/s at 85 °C," *Electron. Lett.*, vol. 27, no. 8, pp. 103–105, Jan. 2014.

[6] **Hui Li**, Philip Moser, Philip Wolf, Gunter Larisch, Leszek Frasunkiewicz, Maciej Dems, Tomasz Czyszanowski, James A. Lott, and Dieter Bimberg, "Energy efficiency, bit rate, and modal properties of 980 nm VCSELs for very-short-reach optical interconnects," *in proc. SPIE 9001 on Vertical-Cavity Surface-Emitting Lasers XVIII*, Feb. 2014, pp. 900110B–90010B–8.

[7] **H. Li**, P. Wolf, P. Moser, G. Larisch, J. A. Lott, and D. Bimberg, "Temperature-Stable Energy-Efficient High-Bit-Rate Oxide-Confined 980 nm VCSELs for Optical Interconnects," *in proc. Asia Communications and Photonics Conference (ACP)*, Nov. 2014, pp. ATh1A. 5.

[8] **H. Li**, P. Wolf, P. Moser, G. Larisch, J. A. Lott, and D. Bimberg, "Vertical-cavity surface-emitting lasers for optical interconnects," *SPIE Newsroom Optoelectronics & Communications*, pp. 1–3, Nov. 2014. DOI: 10.1117/2.1201411.005689

[9] D. Bimberg, **H. Li**, P. Moser, P. Wolf, G. Larisch, and J. A. Lott, "VCSELs for computer interconnects," *in proc. IEEE Photonics Conference (IPC)*, Oct. 2014, ME1.2, pp. 89–90.

[10] P. Wolf, **H. Li**, P. Moser, G. Larisch, J. A. Lott, and D. Bimberg, "Extraction and analysis of high-frequency response and impedance of 980 nm VCSELs as a function of temperature and oxide aperture diameter," *in proc. SPIE 9381 on Vertical-Cavity*

Surface-Emitting Lasers XIX, Feb. 2015, pp. 9381-9381-15.

[11] **H. Li**, P. Moser, P. Wolf, G. Larisch, J. A. Lott, and D. Bimberg, "Energy efficient 850 nm VCSELs for Multimode Fiber Based Optical Interconnects," *in proc. International Nano-Optoelectronics Workshop (iNOW)*, Aug. 2013, pp. B60–B61.

[12] P. Wolf, P. Moser, G. Larisch, **H. Li**, J. A. Lott and D. Bimberg, "Energy efficient 40 Gbit/s transmission with 850 nm VCSELs at 108 fJ/bit dissipated heat," *Electron. Lett.*, vol. 49, no. 10, pp. 666−667, May 2013.

[13] P. Moser, J. A. Lott, P. Wolf, G. Larisch, **H. Li**, and D. Bimberg, "85-fJ Dissipated Energy Per Bit at 30 Gb/s Across 500-m Multimode Fiber Using 850 nm VCSELs," *IEEE Photon. Technol. Lett.*, vol. 25, no. 16, p. 1638−1294, Aug. 2013.

[14] P. Moser, J. A. Lott, P. Wolf, G. Larisch, **H. Li**, N. N. Ledentsov, and D. Bimberg, "56 fJ dissipated energy per bit of oxide-confined 850 nm VCSELs operating at 25 Gb/s," *Electron. Lett.*, vol. 48, no. 20, pp. 1292−1294, Sep. 2012.

[15] P. Moser, J. A. Lott, P. Wolf, G. Larisch, **H. Li**, and D. Bimberg, "Error-free 46 Gb/s operation of oxide-confined 980 nm VCSELs at 85 °C," *Electron. Lett.*, vol. 50, no. 19, pp. 1369−1371, Sep. 2014.

[16] Dieter Bimberg, Dejan Arsenijević, Gunter Larisch, **Hui Li**, James A. Lott, Philip Moser, Holger Schmeckebier, Philip Wolf, "Green nanophotonics for future datacom and Ethernet networks," *in proc. SPIE9134 on Semiconductor Lasers and Laser Dynamics VI*, May 2014, pp. 913402–913402.

[17] P. Moser, P. Wolf, G. Larisch, **H. Li**, J. A. Lott, and D. Bimberg, "Energy Efficient 850 nm VCSELs for Error-free 30 Gb/s Operation across 500 m of Multimode Optical Fiber with 85 fJ of Dissipated Energy per Bit," *in proc. IEEE Optical Interconnects Conference 2013*, May 2013, pp. 13–14.

[18] Philip Moser, Gunter Larisch, Philip Wolf, **Hui Li**, James A. Lott, and Dieter Bimberg, "Green photonics for data and computer communication," *in proc. IEEE Photonics Society Summer Topical Meeting Series 2013*, Jul. 2013, pp. 5–6.

[19] Philip Wolf, Philip Moser, Gunter Larisch, **Hui Li**, James A. Lott, and Dieter Bimberg, "119 fJ of Dissipated Energy per Bit for Error-free 40 Gbit/s Transmission Across 50 m of Multimode Optical Fiber Using Energy Efficient 850 nm VCSELs," *in proc. Conference on Lasers and Electro-Optics (CLEO)*, Jun. 2013, pp. CTu3L.

[20] Philip Moser, Philip Wolf, Gunter Larisch, **Hui Li**, James A. Lott, and Dieter Bimberg, "Energy-efficient oxide-confined high-speed VCSELs for optical interconnects," *in proc. SPIE 9001 on Vertical-Cavity Surface-Emitting Lasers XVIII*, Feb. 2014, pp. 9001103–900103.

[21] Philip Wolf, Philip Moser, Gunter Larisch, Werner Hofmann, **Hui Li**, James A. Lott, Chien-Yao Lu, Shun L. Chuang, Dieter Bimberg, "Energy-efficient and temperature-stable high-speed VCSELs for optical interconnects," *in proc. 15th International*

Conference on Transparent Optical Networks (ICTON), Jun. 2013, pp. 1–5.

[22] Dieter Bimberg, Gunter Larisch, Philip Moser, Philip Wolf, **Hui Li**, and James A. Lott, "Energy-efficient, temperature stable, high data rate VCSELs for optical interconnects," *in proc. 16th International Conference on Transparent Optical Networks (ICTON)*, Jul. 2014, pp. 6–10.

[23] Philip Moser, James A. Lott, Philip Wolf, Gunter Larisch, **Hui Li**, Nikolay N. Ledentsov, and Dieter Bimberg, "Impact of the aperture diameter on the energy efficiency of oxide-confined 850 nm high speed VCSELs," *in proc. SPIE 8639 on Vertical-Cavity Surface-Emitting Lasers XVIII*, Mar. 2013, pp. 86390V–86390V.

[24] Philip Moser, James A. Lott, Philip Wolf, Gunter Larisch, **Hui Li**, and Dieter Bimberg, "Temperature-stable oxide-confined 980 nm VCSELs operating error-free at 46 Gb/s and 85°C," *in proc. IEEE International Semiconductor Laser Conference (ISLC)*, Sep. 2014, TA7, pp. 76–77.

[25] Werner Hofmann, Philip Moser, Philip Wolf, Gunter Larisch, **Hui Li**, Wei Li, James A. Lott, Dieter Bimberg, "VCSELs for exascale computing, computer farms, and green photonics," *in proc. SPIE 8552 on Semiconductor Lasers and Applications V*, Nov. 2012, pp. 855205–855205.