Wideband High-Performance Sigma-Delta Modulators for High-Speed Communications

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Eidesstattliche Erklärung

Ich versichere an Eides statt, dass ich die Dissertation selbständig verfasst habe. Die benutzten Hilfsmittel und Quellen sind in der Arbeit vollständig angegeben.

Yin Yi

Zusammenfassung

Heutzutage ist es möglich Millionen von Transistoren auf einem einzigem Chip zu integrieren, wobei Submikron CMOS Technologien angewendet werden. Gleichzeitig hat sich die Geschwindigkeit der digitalen Schaltungen in den GHz-Bereich erhöht. Wegen der permanenten Entwicklung der digitalen CMOS Technologie ist es möglich die anaolge Signalverarbeitung in den digitalen Bereich zu verschieben. Damit vermeidet man den Einsatz der teuren analogen Schaltungen. Dadurch steigen aber die Anforderungen an die A/D-Umsetzer bezüglich Auflösung und Bandbreite. Besonders in modernen Kommunikationssystemen benötigt man A/D-Umsetzer mit mehr als 14-bit Auflösung und 90 dB Spurious-free Dynamische Bereich (SFDR). Die andere, gleichzeitige gewünschte Schlüsseleigenschaft von A/D-Wandlern sind Wandlungsraten von zehn MSample/s bis zu mehreren hundert MSample/s.

Mit der Erhöhung der gewünschten Signal-Wandlungsrate wird das Einschwingverhalten zum Engpaß bei den gegenwärtigen breitbandigen Sigma-Delta Modulatoren mit geschaltete Kapazitäten (SC). In dieser Dissertation, wurde ein systematischer Entwurf von Sigma-Delta Modulatoren mit hoher Bandbreite und hoher Auflösung vorgestellt. Es wurde ein kaskadierte Sigma-Delta-Modulator 5. Ordnung (2-1-1-1) beschrieben, der mittels der BICMOS-Technologie die gewünschten Eigenschaften, auch bezüglich des Einschwingverhaltens, aufweist. Erreicht wird dies durch einen neuartigen Operationsverstärker, der die geforderten guten elektrischen Eigenschaften besitzt. Weiter wird in der Arbeit beschrieben, wie alle für den Modulator notwendigen Grundschaltungen entworfen werden können.

Ein wesentlicher Teil der Arbeit stellt die Entwicklung eines Simulationswerkzeuges dar, mit dessen Hilfe die nichtidealen Effekte in Sigma-Delta-Modulatoren gut simuliert werden können. Diese Werkzeuge dienten der Entwicklung von verbesserten Strukturen. Als Alternaitve hierzu wurde ein kaskadierter Modulator entwickelt, der mit einer reinen CMOS-Technologie implementiert werden kann. In der Literatur kann man lesen, daß kaskadierte Sigma-Delta-Wandler höherer Ordnung zwar immer stabil sind, aber den großen Nachteil aufweisen, daß sie sehr empfindlich auf Nichtidealitäten, wie endliche

Verstärkung, begrenzte Bandbreite und Slewrate und Toleranzen von Kapazitätsverhältnissen sind. In dieser Arbeit wurde ein Konzept für einen breitbandigen hochauflösenden Sigma-Delta-Umsetzer nachdem Mash-Prinzip vorgestellt, das die in der Literatur benannte Nachteile vermeidt. Im Gegenteil mit der neuen Struktur erzielt man eine Verbesserung des Signal-Rausch-Verhältnisses um 10 dB. Gleichzeitig werden die Anforderungen an die Operationsverstärker drastisch verringert. Da in der neuen 3-1-1 Struktur die Wirkungen der Nichtidealitäten entschärft sind. Die vorgeschlagenen Architekturen sind sehr gut geeignet für die Implementierung von hochwertigen A/D-Umsetzer mittels einer reinen CMOS-Technologie.

Abstract

Nowadays, it is possible to integrate millions of transistors in a single chip by using submicron CMOS processes. Simultaneously, the speed of digital circuits has increased up to the gigahertz range. With the ongoing advance of the CMOS digital technology, the trend is that digitizing an analog signal and performing digital signal processing is as early as possible in a signal processing system, to eliminate the requirements of accurate and expensive traditional analog building blocks. However, early signal digitization increases requirements on the analog-to-digital converters (ADCs) regarding resolution and bandwidth. Particularly in the modern communication systems, over 14-bit signal-to-noise ratio and 90-dB spurious-free dynamic-range should be satisfied, in order to avoid that small analog input signals are masked under the distortions by intermodulation products with the interfering signals. The other simultaneously desired key performance of ADCs is the conversion rate from tens of MSample/s to hundreds of MSample/s in the future communication systems to meet the growing needs of the high-capacity and high-speed data transfer.

As the desired signal conversion rate increases, integrator defective settling becomes the main bottleneck in the present wideband Switch-Capacitor (SC) Sigma-Delta modulators. In this thesis, a systematic approach for designing high-speed high-resolution Sigma-Delta modulators is introduced. This approach has been adopted in designing a high-order cascade multi-bit Sigma-Delta modulator in the 0.4 u SiGe-BiCMOS process, which was donated by Freescale Semiconductor, Inc. Therefore, a power efficient implementation has been obtained in a short design cycle. In this design, high-performance analog circuits, such as opamp, bandgap, etc., have been designed in the SiGe-BiCMOS process. It shows that by properly using the BiCMOS process, the conversion rate of the Sigma-Delta modulator integrators can be greatly improved without the degradation of the achievable resolution.

A substantial part of the work is to develop a simulation tool. With its assistance the non-ideal effects and corresponding improved structures can be well simulated in sigma delta modulators. As alternatives, a novel low-disortion cascade and a low-disortion cascade

multi-bit Sigma-Delta modulator with improved noise-transfer-function (NTF) have been proposed in the mainstream CMOS process. Both architectures combine the merits of low-distortion, cascaded Sigma-Delta structure and multi-bit quantization to achieve high dynamic range at low oversampling ratio of 8. A comprehensive analysis of both proposed architectures in comparison with the traditional high-order Sigma-Delta modulator architectures has been performed. It shows that both architectures are fundamentally immue to the finite integrator settling and other circuit non-idealities, such as finite and non-linear DC-gain of opamps, capacitor mismatching, etc. Additionally, the second one exhibits an SNR improvement over 10 dB against theoretical value. These overall outstanding advantages have been validated by behavior simulation. The proposed architectures are potentially suitable for wideband and low-power applications with deep sub-micron CMOS processes.

Contents

List of Abbreviations

ADC	Analog-to-Digital Converter
BiCMOS	Bipolar and Complementary Metal Oxide Semiconductor
CAD	Computer Aided Design
CMFB	Common-Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous-Time
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DR	Dynamic Range
DSP	Digital Signal Processing
DT	Discrete-Time
DWA	Data Weighted Averaging
ENOB	Effective Number Of Bits
ESD	Electrostatic Discharge
FIR	Finite Impulse Response
FOM	Figure of Merit
FS	Full Scale
GB	Gain-Bandwidth Product
HD	Harmonic Distortion
HDTV	High-definition television
IC	Integrated Circuit
IIR	Infinite Impulse Response
ILA	Individual Level Averaging
INL	Integral Non-Linearity
LSB	Least Significant Bit
MASH	Multi-Stage Noise-Shaping
MiM	Metal-insulator-Metal
MSB	Most Significant Bit
NMOS	N-channel MOS
Nyquist-rate	Twice of its highest frequency component

NTF	Noise Transfer Function
OS	Output Swing
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PMOS	P-channel MOS
PSD	Power Spectral Density
RF	Radio Frequency
ROM	Read-Only Memory
S/H	Sample-and-Hold
SC	Switched-Capacitor
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-(Noise+Distortion) Ratio
SoC	System-on-Chip
SR	Slew-Rate
STF	Signal Transfer Function
THD	Total Harmonic Distortion
VDSL	Very high bit-rate digital subscriber line

Chapter 1 Introduction

1.1 Thesis background

1.1.1 Background

According to ITRS roadmap (International Technology Roadmap for Semiconductors), the feature size of the mainstream CMOS process will continue to be scaled down for at least another decade without deceleration, and it will reach 32 nm by the year 2013, which is about one third of the current technology level (90 nm, year 2004). At the same time, transistors become faster, making possible the ever-increasing clock rates in digital circuits.

For analog circuits the evolution of technology is not as beneficial. Thus, there is a trend to move signal processing functions from the analog domain to the digital one, which speeds up the design cycle, brings more flexibility and programmability, and increases the possibility for design reuse. But the real world has the analog nature, and furthermore, the input and output signals of communication systems are inherently analog. Therefore, analog to digital converters and digital to analog converters are always needed to link the real world and the digital signal processing [Li03].

The A/D conversion comprises of two procedures: sampling, which makes the signal discrete in time, and quantization, which makes the signal discrete in amplitude. Accordingly there are two important specifications for an ADC: speed and resolution. The speed represents how fast the discretization can be done; the resolution represents how accurate the discretization in amplitude can be done. Signal to noise ratio (SNR) is often used to characterize the conversion resolution [Raz95].

A band-limited analog signal must be sampled at least twice as far as its highest frequency component (Nyquist-rate) so that the signal can be reconstructed without loss [Sha49]. Many ADCs are designed to sample the signal just a little faster than the Nyquist rate, resulting in the large bandwidth. These ADCs are categorized as the Nyquist-rate ADCs.

Using a standard CMOS process, the conversion bandwidth has been expanded to the range of Giga Hz [Pou02]. The main drawback of Nyquist-rate ADCs is their low resolution, which is limited by the matching of analog components. Another problem is the complex hardware structure and the high power consumption (mainly contributed by the large number of comparators). Using other structures like pipeline or folding can reduce the required number of comparators and power consummation. However, they are still very sensitive to the matching of analog components. Without additional calibration or correction mechanisms, they are difficult for high-resolution applications[Li03].

Sigma-Delta ADCs, which provide a robust and economical solution for high-resolution analog-to-digital conversion, have being developed since the 60's of last century [Ino62]. A Sigma-Delta modulator realizes that the input signals and the corresponding quantization errors pass through the low-pass loop filter and the high-order high-pass filter, respectively. Therefore, at output the signals comprise of the delayed input signals and the quantization errors that are shaped by the high-order high-pass filter. Theoretically, quantization error can be infinitely shifted out from the interesting bandwidth, and the conversion resolution can be arbitrarily increased until the device thermal noise floor physically limits the resolution. Furthermore, a Sigma-Delta ADC does not require accurate analog component matching to achieve the superior resolution, which makes it suitable for standard CMOS processes. In comparison with the Nyquist-rate ADCs, however, Sigma-Delta ADCs have to operate at an oversampling frequency, which results in the main drawback: the narrow conversion bandwidth.

Considering the circuit realization, Sigma-Delta ADCs can be categorized into discrete time structure and continuous-time structure. Using switched-capacitor (SC) circuits, the discrete-time Sigma-Delta ADC offers a good degree of accuracy. But the circuit speed is limited by the defective settling of switched-capacitor integrator. Continuous-time (CT) Sigma-Delta ADCs are more adaptive to low supply voltage. The low power consummation makes the realization of CT ADCs more attractive in future advanced CMOS processes. Input-signal sampling errors, like settling error, charge injection and some other discrete-time problems do not exist in continuous-time circuits. The circuits can operate at a higher speed for a given technology than their switched-capacitor counterpart. Furthermore, Continuous-time (CT) Sigma-Delta ADCs provide implicit anti-

alias filtering, thus reducing the need for explicit anti-alias filtering prior to the modulator. But the drawbacks of continuous-time Sigma-Delta ADCs are serious. A CT Sigma-Delta ADC requires a highly linear resistor or transconductor, which is not well-suited for implementation in modern sub-micro CMOS processes. Additionally, the pole locations of these integrations are set by the RC (or C/Gm) time constants of these devices. The variation of pole locations determined by products of two dissimilar device parameters (rather than as a ration of similar device parameters), is as large as about ±30%. The large mismatch greatly limits the efficacy of multi-stage CT Sigma-Delta ADCs without adding elaborate tuning mechanisms. It is also more sensitive to clock jitter and quantizer metastability, which cause random pulse width modulation in the feedback DAC. Therefore, they, in turn, cause high-frequency quantization noise to fold into the signal bandwidth, which lowers the conversion resolution [Che00] [Ben97]. Since the requirement on ADC resolution in high-integration low-cost wireless receivers is normally higher than applications like traditional wireless receivers, this drawback prevents continuous-time Sigma-Delta ADCs from being a good choice for modern receivers.

Considering conversion signal-band, Sigma-Delta ADCs can be categorized into low-pass ADCs and band-pass ADCs. Band-pass ADCs are especially suitable for converting a narrow-band signal which has a non-zero centre frequency. This character makes band-pass ADCs ideal for IF digitization in wireless communications. Recently many band-pass ADCs [Sal01], [Sch02] adopt the continuous-time structure to achieve a high centre frequency and a large oversampling ratio, where the resolution requirement is moderate.

A complete Sigma-Delta ADC includes a modulator (mostly analog) and a digital decimation filter. The modulator shapes the quantization error and the decimation filter reconstructs the signal in digital form. The focus of this thesis is on the high-speed high-resolution modulator part.

1.1.2 Recent developments

In recent years, Sigma-Delta converters have been frequently applied to high-resolution

low power applications. In order to compare the performance improvement, the figure of merit (FOM) is defined according to the formula:

$$FOM = \frac{2^{ENOB} \times (2 \times signalband)}{power} \qquad 1.1$$

where ENOB is the effective number of bits, calculated according to the peak signal-to-noise-and-distortion-ratio (SNDR):

$$ENOB = (SNDR_{dB} - 1.76)/6.02 \qquad 1.2$$

Fig 1.1 shows the performance increase of Sigma-Delta ADCs in the past 16 years (1988-2004) and in this work, where the chips are chosen that have higher FOM of the year.

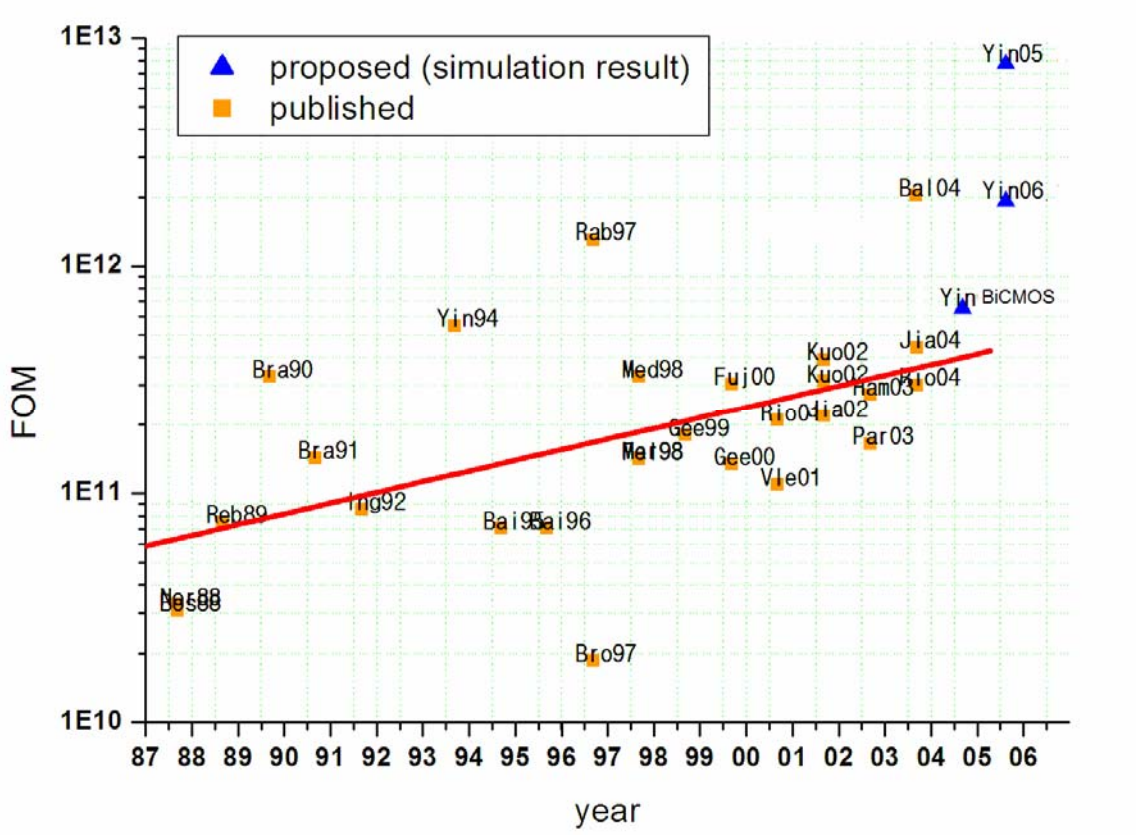


Fig. 1.1 FOM of Sigma-Delta ADC

The increase of conversion bandwidth and the relative decrease of power are two contradictory design targets. In the past 16 years the FOM of Sigma-Delta ADCs has increased by more than 30 times, as illustrated in Fig. 1.1. Note that the achieved conversion resolution has not changed much more, — already in the early 90's there was a

20-bit-resolution converter reported [Yam94]. Therefore, the continuous increase of signal bandwidth and the decrease of power consumption are ever addressed on, in order to boost the FOM. For example, compare the chips of 1989 and 2004; [Reb89] chip has a 13-bit resolution, while the [Bal04] chip has a 14-bit resolution. But the signal band of [Bal04] chip is about 78 times as large as that of [Reb89], and its power consumption is only about 5 times of that of [Reb89] chip.

In recent years, the higher FOM of the published Sigma-Delta ADCs is achieved by compensating the weakened benefits of oversampling (necessarily moderate) in the Sigma-Delta architectures with high-order topologies —either in a single loop [Gee00] [Kou02][Reu02][Bal04][Jia04] or in a multi-stage cascade [Yin94] [Feld98] [Mar98] [Gee99] [Mor00] [Fuj00] [Rio02] [Par03] [Rio04]— which often incorporate multi-bit quantization —either purely [Gee00] [Fuj00] or by means of dual quantization techniques [Bra91b] [Bro97] [Med99a] [Ham04].

1.2 Motivation

1.2.1 Goal of this work

The goal of this work is to study the design feasibility of Sigma-Delta modulators, which should feature 12-14-bit resolution at 20-25Msample/s aimed for AD conversion in high-performance wireline or wireless communication applications, such as very high bit-rate digital subscriber (VDSL), 3G, and even low-cost high-integration, high-flexibility software radio systems. The power consumption is limited to 150 mW--300 mW, in order to obtain higher FOMs.

1.2.2 Problem statement

In analog-to-digital converters (ADCs), the requirements on sampling linearity, conversion rate, resolution, and power consumption are becoming tighter. As mentioned above, generally, in order to achieve a wide bandwidth and a high resolution, the sampling

frequency, the noise-shaping order and the quantizer resolution should be increased separately or together.

The process advance brings a thinner gate oxide and therefore a larger transconductance gm. As a result, the sampling speed (f_s) of a Sigma-Delta ADC is continuously increasing. In early 1990's the typical sampling frequency is tens of Mega-Hertz [Bra90], [Yin94]. Nowadays above hundred-Mega-Hertz switched-capacitor Sigma-Delta ADCs are implemented [Bal04]. Therefore, the bottleneck of speed increase is mainly the defective settling procedure of the integrators, since the large settling error results in non-linearity and the converter output will contain not only the increased noise floor but also the large harmonic distortions [Reb90].

With respect to the high order noise-shaping, the cascade multi-bit Sigma-Delta modulator (MASH) structures by cascading the Sigma-Delta stages of the second or lower order [Fuj00][Rio01][Vel01] are unconditionally stable. However, the circuit non-idealities, due to the mismatch in capacitor ratios and finite open-loop gains of the opamp, both result in an incomplete cancellation of the quantization error of the former stages, which degrade the dynamic range. [Yin94] [Mer99] [Rio01].

An alternative is to use the single-loop high order structures, which have the advantage that they are insensitive to the capacitor mismatch and do not require high-performance analog circuits, but if the order of integrator is larger than 2, the modulator is prone to instability. Therefore, the gain of the noise-transfer-function (NTF) has to be decreased by dividing the Lth-order polynomial D(Z), which results in a lower noise suppression of the base band quantization noise[Bal04][Kuo02]. Another problem associated with high-order single-stage modulators is the high coefficient spread leading to larger area, more power consumption and poorer stability.

1.2.2 Solutions

In order to avoid a significant degradation of the SNR relative to the theoretical limit, the cascade multi-stage Sigma-Delta modulators based on the easily implemented stable first-

or second-order Sigma-Delta modulators are good choose. The key in this typ architecture is to design high-performance analog circuit's building blocks that is difficult to be achieved in the modern CMOS technology.

The evolution of technology has been driven by the microprocessor industry, and hence does not always go in the best direction for the analog. However, the recent rapid growth of the wireless telecommunication device market has caused a boost in the development of advanced mixed signal technologies, such as silicon germanium-based BiCMOS, which is becoming a viable technology for the production of competitively priced and superior performance circuits.

Indeed, Sigma-Delta converters like any other data converters are inherently mixed signal circuits. The emergence of mixed-signal oriented SiGe-BiCMOS process now offers a more direct and effective alternative. The high transconductance of bipolar device for given current and area is higher than MOS transistors, therefore, it can be used to expand the open-loop gain and the unity-gain bandwidth of opamps, and the superior matching properties of bipolar devices make the offsets lower, which improves the common-mode rejection. Bipolar transistors also have considerably lower l/f noise than comparably-sized MOS transistors, which makes it possible to reduce system noise without devoting excessive area to MOS transistors forward in the signal path. In this scenario, this work primitively tried to adequately select, design, and develop high-performance key analog building blocks in BiCMOS for a multi-stage high-order Sigma-Delta modulator to meet our design goal.

The rapid development of modern deep-submicron CMOS processes and the ultimate goal being a single chip solution -- the system on a chip (SoC) -- bring the additional challenges in the data converter design, such as decreasing supply voltage, short channel effects in MOS devices, matching of devices, etc. Therefore, the requirements of sampling linearity, process matching, high DC gain and high gain-bandwidth product opamps in the traditional data converter architectures are becoming more and more difficult to be realized. This encourages me, in parallel, to concentrate on the development of novel high-order multibit Sigma-Delta ADC architectures. The performance requirements of analog circuits

should be significantly relaxed, so that the proposed Sigma-Delta ADC architectures are suitable for realizing high resolution broadband ADCs even as IC technologies advance. In this scenario, a novel low-disortion cascade and a low-disortion cascade multi-bit Sigma-Delta modulator with improved noise-transfer-function (NTF) are proposed in the mainstream CMOS process. Both architectures combine merits of low-distortion, cascaded Sigma-Delta structures and multi-bit quantization to achieve high dynamic range at low oversampling ratio of 8.

1.3 Thesis Organization

The thesis is organized as follows.

Chapter 2 illustrates the principle of Sigma-Delta ADCs. Associated with ideal performances basic topologies of Sigma-Delta modulators are introduced and their pros and cons are discussed.

Chapter 3 is dedicated to an exhaustive analysis of the main non-idealities that affect the performance of Sigma-Delta modulators. System considerations, behavioral models, and closed expressions are obtained for the impact of the different non-idealities, which can be used as estimable guidelines for practical implementation of Sigma-Delta modulators.

Chapter 4 describes the cascade Sigma-Delta modulator implemented in BiCMOS technology. The topology selection, the requirements of each building block and its corresponding design at the transistor level are discussed in detail in this chapter.

Chapter 5 describes the development of two cascade Sigma-Delta modulators. The proposed architectures are elaborated in comparison with the traditional topologies in this chapter.

Chapter 6 summarizes and concludes the thesis.

Chapter 2 Sigma-Delta ADC Overview

2.1 Introduction

This chapter will begin with an introduction to some basic metrics, which are used to evaluate the modulator performance. Then the fundamental topologies of Sigma-Delta modulators are reviewed. Following this basic introduction, tradeoffs among a variety of Sigma-Delta architectures that are suitable for high-speed applications are explored.

2.2 Performance metrics

This section reviews the key metrics, such as dynamic range, Nyquist rate and power dissipation, which are needed by the evaluation of the Sigma-Delta modulator quality [Fel98b].

2.2.1 Peak SNR/SNDR, DR and SFDR

Each component in the system has associated errors. The goal is to keep the total errors below a certain limit. The accuracy of ADCs is usually evaluated by several key parameters, i.e. Peak SNR, SNDR and dynamic range, which are related to specifications and can be defined together.

Signal-to-noise ratio (SNR):

SNR is the ratio in power between the input sine wave $f_{(IN)}$ and the noise of the converter from DC to Nyquist rate. SNR includes all noise sources in the modulator, both thermal and quantization. It is typically expressed in decibels.

$$SNR = 10\log\left(\frac{P_{signal}}{P_{noise}}\right) \qquad 2.2.1$$

Signal-to-noise-distortion ratio (SNDR):

SNDR is similar to SNR, except that it includes the harmonic content.

$$SNDR = 10\log\left(\frac{P_{signal}}{P_{noise} + P_{distortion}}\right) \qquad 2.2.2$$

For small signal levels, distortion is not important. As the signal level increases, distortion degrades the modulator performance, and the SNDR will be less than the SNR.

Dynamic range (DR):

DR is the ratio in power between the maximum input signal level that the modulator can handle and the minimum detectable input signal. Practically, the maximum input signal level is the input level where the SNDR drops 3 dB beyond the peak. For an analog-to-digital converter (ADC), if the signal is too large, it will over-range the ADC input. If it is too small, the signal will get lost in the quantization noise of the converter.

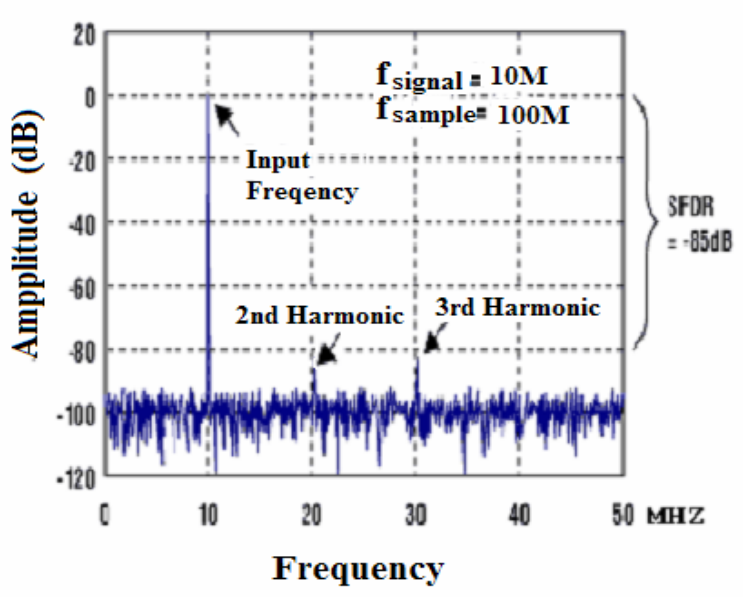


Fig. 2.1 Illustration of SFDR

Spurious-free dynamic range (SFDR):

SFDR is the ratio of the power value of the input sine wave with a frequency f_{IN} for an ADC, to the power value of the peak spur observed in the frequency domain. As illustrated in Fig 2.1, a large spur in the frequency domain may not significantly affect the SNR, but

will significantly affect the SFDR. SFDR is a useful metric in communication applications, where the distortion component can be much larger than the signal of interest due to the intermodulation of unwanted interferential signals. Consequently, the small input signals are masked into the spurs; the dynamic range of the ADC is attenuated.

2.2.2 Nyquist rate

Nyquist rate f_N is the lowest sampling frequency that can be used for analog-to-digital conversion of a signal without resulting in significant aliasing. This frequency is twice the rate of the highest input frequency f_b. Therefore, Nyquist rate specifies the minimum sampling frequency required to avoid aliasing.

2.2.3 Oversampling ratio (OSR)

In contrast to Nyquist-rate ADCs, Sigma-Delta converters use oversampling to decrease the quantization error power within the signal band and increase the accuracy of the A-to-D conversion. The *oversampling ratio* is defined as the ratio between the sampling frequency f_s and the Nyquist rate f_N. Since $f_N = 2f_b$, the oversampling ratio can be expressed as:

$$OSR = \frac{f_S}{f_N} = \frac{f_S}{2f_b} \qquad 2.2.3$$

2.2.4 Power dissipation

When a current flows in a component, that component will consume power and heat up. This process is called power dissipation and is measured in Watts. In a switched-capacitor implementation, there are two fundamental contributors to power dissipation. The first is dynamic power. This is the power required to charge and discharge capacitors in the integrator. The second is the static power dissipated by the active devices within the integrator amplifier.

Dynamic power dissipation:

Dynamic power dissipation is due to periodical charge/discharge of load capacitances. Suppose that the amplifier delivers just the required charge/discharge for the sampling capacitor and introduces no additional noise into the circuit. Then, the integrator power will follow the relationship [Kla96] [Gra01]:

$$P = \alpha V_{DD}{}^2 C_s f_N OSR \qquad 2.2.4$$

where the samplings capacitor is C_s, the system Nyquist rate is f_N and the oversampling ratio is *OSR*. The average change of the voltage on the sampling capacitor is indicated by a nominal variable α.

Static power dissipation:

As the sampling frequency increases in Sigma-Delta modulators to process wideband signals, integrator defective settling due to the slew-rate of the amplifiers becomes the main bottleneck in present SC designs. If the integrator in switched-capacitor circuits is implemented by employing class A single-pole operational amplifiers, the device transconductance (g_m) is proportional to bias current I_{BIAS}, and the integrator input value at the end of the preceding sampling phase is $v_s=V_{in}(nT_s-T_s/2)$, then the active device should be biased at a constant current, which satisfies [Wil94]:

$$I_0 > gm \left| \frac{C_S}{C_I} v_s \right| \qquad 2.2.5$$

so that the amplifier operates linearly settling. Therefore, the evolution of the minimal static power by the amplifier becomes:

$$P_{STAT} = V_{DD} I_{BIAS} = V_{DD} * g_m \left| \frac{C_S}{C_I} v_s \right| \qquad 2.2.6$$

2.3 Basic architecture

2.3.1 Basic principle

The basic idea of Sigma-Delta ADC is that it exchanges resolution in amplitude to resolution in time. In such ADC, the analog signal is modulated into a low resolution code at a frequency much higher than the Nyquist rates, and then the excess quantization noise is removed by the following digital filters [Nor97]. Thus, if OSR is high, the oversampling ADCs are very suitable for CMOS VLSI digital technology, because it does not require high performance analog buildings.

Fig. 2.2 shows the basic block diagram of a Sigma-Delta modulator and its corresponding linear model. The Sigma-Delta modulator consists of a feedforward path formed by a loop filter and a B-bit quantizer, and a negative feedback path around them, using a B-bit D-to-A converter [Ino62]. In the linear model as illustrated in Fig.2.2b, the DAC is assumed to be ideal and the injected quantization error of the quantizer is assumed as an additive white noise approximation.

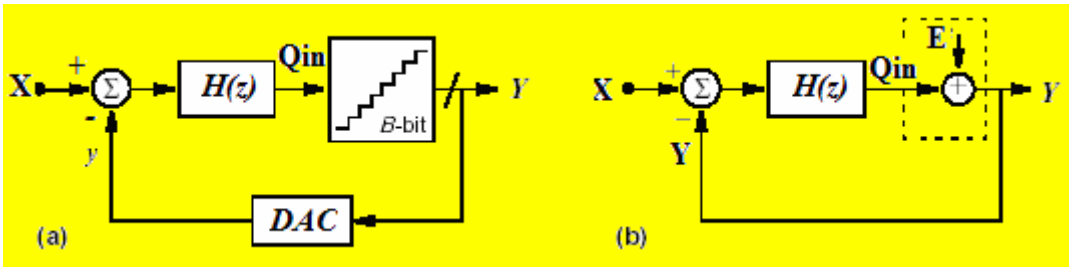


Fig 2.2 Sigma-Delta modulator architecture: (a) Basic block diagram, (b) Corresponding linear model.

In this way, the modulator can be considered as a two-input, one-output linear system. Therefore, a signal transfer function, STF(z), and a noise transfer function, NTF(z), can be derived:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} \qquad 2.3.1$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \qquad 2.3.2$$

In the frequency domain, the output signal is obtained as the combination of the input signal and the noise signal, with each being filtered by the corresponding transfer function:

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \qquad 2.3.3$$

By properly selecting the loop filter, the signal transfer function and the noise transfer function of a theoretical *Lth*-order Sigma-Delta modulator yield in the z-domain:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} = z^{-L} \qquad 2.3.4$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} = \left(1-z^{-1}\right)^{L} \qquad 2.3.5$$

where $H(z)=1/(1-z^{-1})$.

Fig 2.3 plots the frequency responses of NTFs with different orders of *L*. When the loop order is higher than one, the frequency response of NTF presents the characteristic of high-pass filters. The higher the order *L* is, the more quantization error energy is suppressed at low frequencies.

In this way, the output signal for the ideal case can be written as:

$$Y(z) = X(z)z^{-L} + E(z)(1-z^{-L}) \qquad 2.3.6$$

The output signal has only a pure delay in comparison with the real input signal *X(z)*, while the quantization error *E(z)* will be pushed out of the output, as it passes through a *Lth*-order high-pass filter.

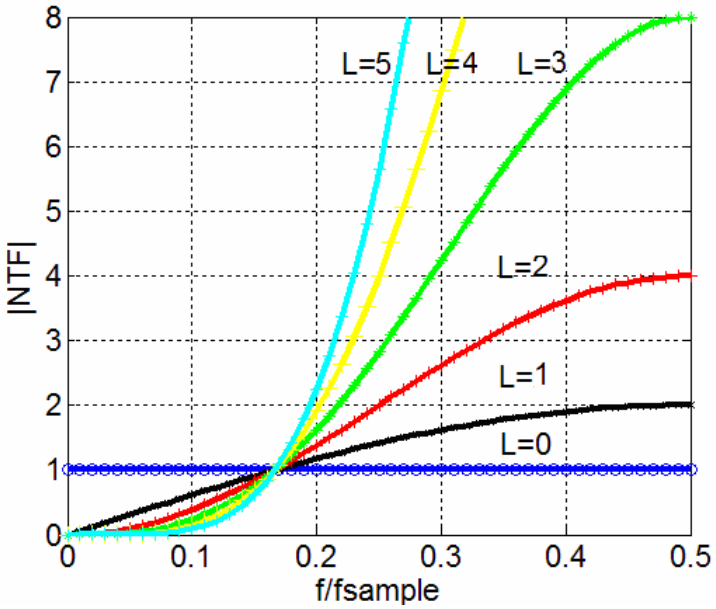


Fig 2.3 Frequency responses of NTFs with different orders of *L*

The quantization error can be viewed as a random process. If assuming that Δ indicates the quantization step, the quantization error is distributed uniformly over the range $\pm\Delta$, and

has a probability density of 1/Δ. [Ben48] [Wid60] [Sri77] [Gra90]. The mean-square value of the quantization error is defined by:

$$\overline{e^2} = \sigma^2(e) = \int_{-\infty}^{+\infty} e^2 \frac{1}{\Delta} de = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} e^2 de = \frac{\Delta^2}{12} \qquad 2.3.7$$

Hence, the in-band power of the filtered quantization error results in

$$P_Q = \int_{-f_b}^{+f_b} \frac{\Delta^2}{12} |NTF(f)|^2 df \approx \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} \qquad 2.3.8$$

Since the maximum input amplitude in the non-overloaded region of the quantizer is A_{FS} and its corresponding power at the ADC output can be approximated to [Pla94]

$$P_{signal} \cong \frac{\left(\frac{A_{FS}}{2}\right)^2}{2} \approx \frac{\left((2^B - 1)\frac{\Delta}{2}\right)^2}{2} = 2^{2B-3}\Delta^2 \qquad 2.3.9$$

Using Equations (2.3.8) and (2.3.9), the dynamic range of an ideal oversampling noise-shaping converter yields

$$DR_Q \approx \frac{3}{2}\frac{(2L+1)}{\pi^{2L}} OSR^{2L+1}(2^B - 1)^2 \qquad 2.3.10$$

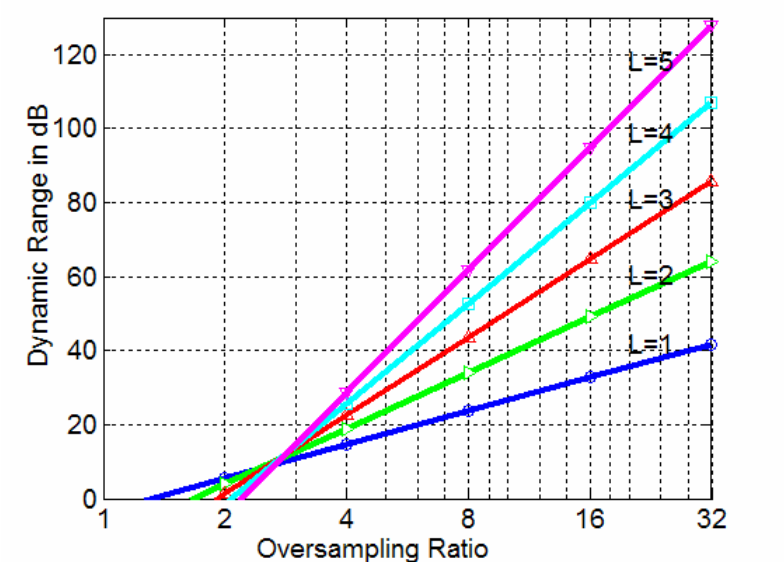


Fig. 2.4 DR versus OSR of a theoretical Sigma-Delta modulator (with all zeros at DC) for different *Lth*-order

The theoretical DR is a power function in combination with the order L, oversampling ratio OSR, and the numbers of the quantizer *B*. Note from the Equation 2.3.10 that an additional

bit in the internal quantizer can roughly obtain a 6-dB improvement of DR. This improvement is independent of the *OSR*, while high-order quantization error shaping is dependent on it. The DR of a theoretical *Lth*-order Sigma-Delta converter increases with OSR in *(L+1/2)* bit/octave. This is shown in Fig. 2.4, where the DR is plotted as a function of the oversampling ratio and the modulator order, in case of a single-bit internal quantizer. Note that for *OSR>4*, the combined action of oversampling and noise-shaping considerably improves performance. It implies that oversampling is the essential condition for a noise shaping. On the other hand, sampling frequency is directly limited by the technology and the slew-rate of opamps, it can not be infinitely increased. Therefore, using multibit quantizer are becoming the common methods to improve the DR, since it has to be designed at a low *OSR* to maximize the signal bandwidth [Yin04].

In order to get a stable modulator, the input of the quantizer must be not saturated. The input of the quantizer as illustrated in Fig. 2.2 can be calculated as in [Nor97]:

$$Q_{in}(z) = STF(z)X(z) + |NTF(z) - 1| E(z) \qquad 2.3.11$$

Therefore, the gain of the |NTF(z)-1| or |NTF(z)| should be small. However, note from Fig 2.3 that the gain of noise transfer functions of the form $(1-z^{-1})^L$ increases rapidly in the high-frequency region. The maximum gain $\|NTF\|_\infty$ is equal to 2^L at $f=f_s/2$, thereby, exhibiting unbounded states, if L>2. Consequenntly, the theoretical increase of performance by using high-order Sigma-Delta modulator at certain OSR is not achievable in practice [Ada97a].

In general, instability appears at the modulator output as a large-amplitude low-frequency oscillation, leading to long strings of alternating +1's and -1's [Ada97a]. High-order quantization error shaping can be achieved by either single-loop through suppression of out-of-band gain or cascading the Sigma-Delta modulators of only 1^{st}- and/or 2^{nd}-order.

2.3.2 High-order single loop

For the Sigma-Delta modulator with one bit internal quantizer to remain stable this gain $\|NTF\|_\infty$ must be adjusted to satisfy that is smaller than 1.5[Lee87b]. Fig. 2.5 shows the scheme of the generic Lee-Sodini Lth-order Sigma-Delta modulator, in which multiple

feedforward and feedback paths are used. Thanks to the large set of analog coefficients, more complex high-pass NTFs can be built as [Lee87a] [Lee87b]:

$$NTF(z) = \frac{(z-1)^L - \sum_{i=1}^{L} B_i (z-1)^{L-i}}{z\left[(z-1)^L - \sum_{i=1}^{L} B_i (z-1)^{L-i}\right] + \sum_{i=0}^{L} A_i (z-1)^{L-i}} \qquad 2.3.12$$

with sufficiently low gain at the high-frequency region.

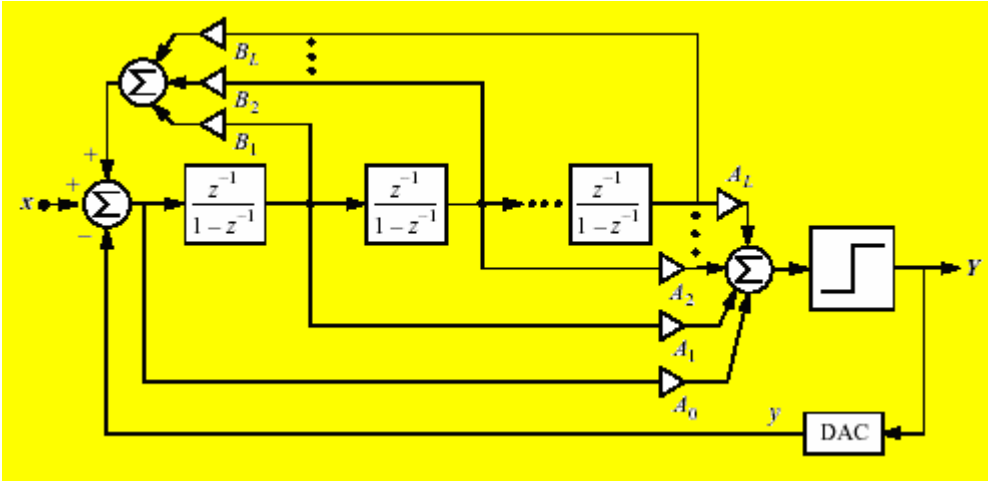


Fig. 2.5 Lee-Sodini Lth-order Sigma-Delta modulator

If the feedback coefficients B_i are set to zero, the following form of the Butterworth IIR filter is obtained

$$NTF(z) = \frac{(z-1)^L}{z\left[(z-1)^L\right] + \sum_{i=0}^{L} A_i (z-1)^{L-i}} = \frac{(z-1)^L}{D(z)} \qquad 2.3.13$$

Where $(z-1)^L$ is the noise-shaping factor, and $D(Z)$ is the Lth-order polynomial. The gain of the *NTF* at high frequencies is decreased by dividing with the Lth-order polynomial $D(Z)$. Since all zeros of this type of modulator are located at position one, the NTF has a good response at the dc level, but not at higher frequencies [Nor96]. NTF rises monotonically in the signal band, so the power spectral density (PSD) at the end of the signal band will practically determine the total in-band error power.

If the feedback coefficients B_i are non-zeros, but small in comparison with A_i, the position of the zeros can be controlled to build the form of the inverse-Chebyshev filter [Lin02]:

$$NTF(z) = \frac{(z-1)^i G(z)}{D(z)} \qquad 2.3.14$$

in which D(Z) is Lth-order polynomial, $(z-1)^i$ is the noise-shaping factor with zeros at DC, G(z) is the function of optimal complex-conjugate pairs of zeros. The imposed G(z) results in a flat band response at low frequency and ripples at the stop band of the signal. Thus, NTF can be improved by placing notches in the signal band for further shaping of the quantization error, while preserving its flat out-of-band gain, and therefore, the modulator stability[Sch93].

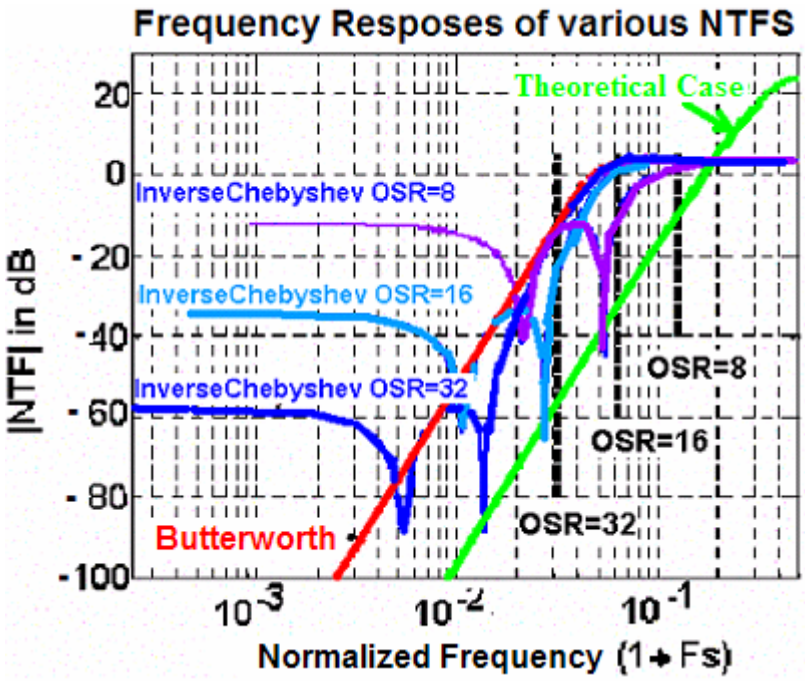


Fig.2.6 The magnitude responses of the 4th-order NTFs of pure FIR, Buterworth and inverse- Chebyshev filter with various OSR.

The *NTF* response of a pure FIR filter and its alternatives for implementing stable 4th-order *NTF*s are shown in Fig.2.6. Note that the X-axis is normalized to the sampling frequency. The *NTF* curve of Butterworth configuration is independent of *OSR*, since its pole-locations do not depend on the *OSR*. The attenuation of the quantization noise is very poor at high frequencies. The zero-locations of the inverse-Chebyshev filter can be optimized with various *OSR*s. Thus, three solid *NTF* curves can be obtained, each with two notches in the signal band. The existence of notches will cause faster decay at its upper edge of the $|NTF(f)|$; this considerably reduces $|NTF(f)|$ at its upper edge, and in turn, the in-band error

power. For each case of *OSR* of 8, 16, 32, P_Q is reduced up to about 13dB by optimally spreading the zeros over the band [Yin04]. However, in comparison with the theoretical *NTF* with all zeros at DC, the in-band noise attenuation of both alternatives is poor, not only at low frequencies but also at high frequencies. The average root-mean-square (RMS) attenuation over the signal band for each |*NTF*| is summarized in Table 2.1.

RMS|NTF| dB / NTF	OSR of 8	OSR of 16	OSR of 32
Butterworth filter configuration	-3dB	-22dB	-46dB
Inverse-Chebyshev filter	-15dB	-35dB	-59dB
Ideal with all zeros at DC	-42dB	-66dB	-90dB

TABLE 2.1 Summary of the average root-mean-square (RMS) attenuations over the signal band for various 4th-order |NTFs|

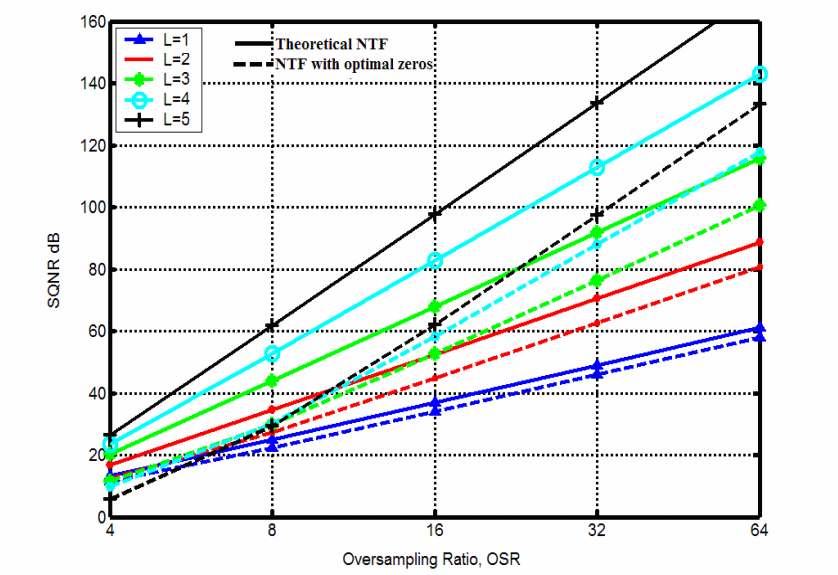


Fig.2.7 Maximum achievable SQNR by Lth -order single-loop Sigma-Delta modulators versus OSR (solid curves: pure NTFs; dashed curves: NTFs designed by inverse-Chebyshev filters with zeros optimally spread over the signal band)

As a result, the maximal achievable *SQNR* of Lth-order single-loop Sigma-Delta modulators designed by inverse-Chebyshev filters is higher than that of Butterworth filter. But the imposed non-zero polynomial *D(Z)* to stabilize the modulator, increases the in-band noise in comparison with the theoretical L^{th}-order one (pure FIR-filter). The maximum achievable *SQNR*s of *L*th-order single-loop Sigma-Delta modulators versus

OSR are illustrated in Fig. 2.7 (solid curves: pure NTFs; dashed curves: NTFs designed by inverse-Chebyshev filters with zeros optimally spread over the signal band). SQNR of the corresponding alternative Sigma-Delta modulator is deteriorated much more than the theoretical values with *NTF* of pure FIR-filter form. Furthermore, it can be detected that increasing the loop-order of Sigma-Delta modulator, which is designed according to inverse-Chebyshev high-pass filter, does not increase *SQNR* at *OSR* lower than 8. Hence, high-orders single-loop structures are unsuitable for high-resolution applications with low *OSR*. [Yin04].

In the last years, many design approaches and architectures have been proposed [Cha90][Che96][Bur98][Lin02][Bal04]. The goal of these approaches and architectures is to improve the stability problem, or/and to determine the values of loop coefficients of a designed modulator with limited coefficient ratios for easy integrated-circuit implementation, while achieving high signal-to-noise ratio (*SNR*) and a wide range of maximum dc input levels. A better set of loop coefficients could be obtained for the same system performance by adding more unknown coefficients than conventional architectures [Lin02]. The modified generic multiple-feedback architecture of an Lth-order modulator is shown in Fig. 2.8. The scaling coefficient c_i in the circuit is to increase the limit of integrator output, while the coefficient b_i is to determine the pole positions and system stability.

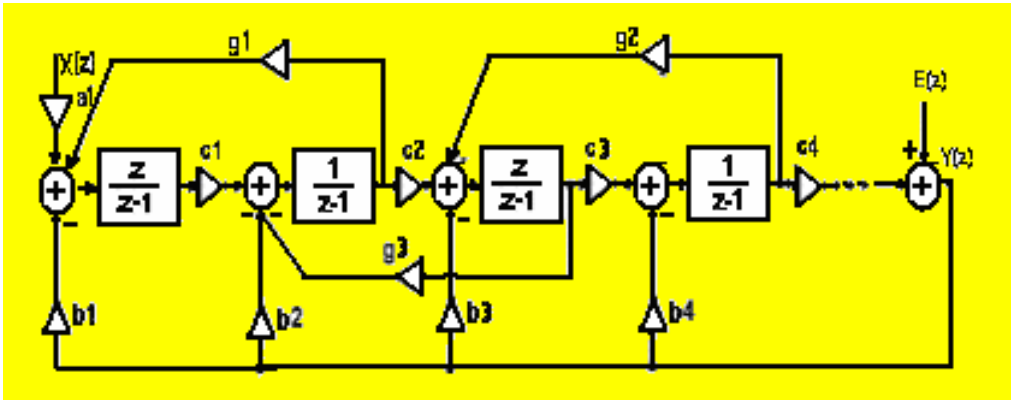


Fig. 2.8 Lin generic multiple-feedback modulator

The coefficient g_i in the circuit generates complex pairs of zeros, and the circuit will thus have the same NTF form as the conventional inverse-Chebyshev filter. If all of the

resonator paths are removed from the circuit, then the modulator becomes a Butterworth filter.

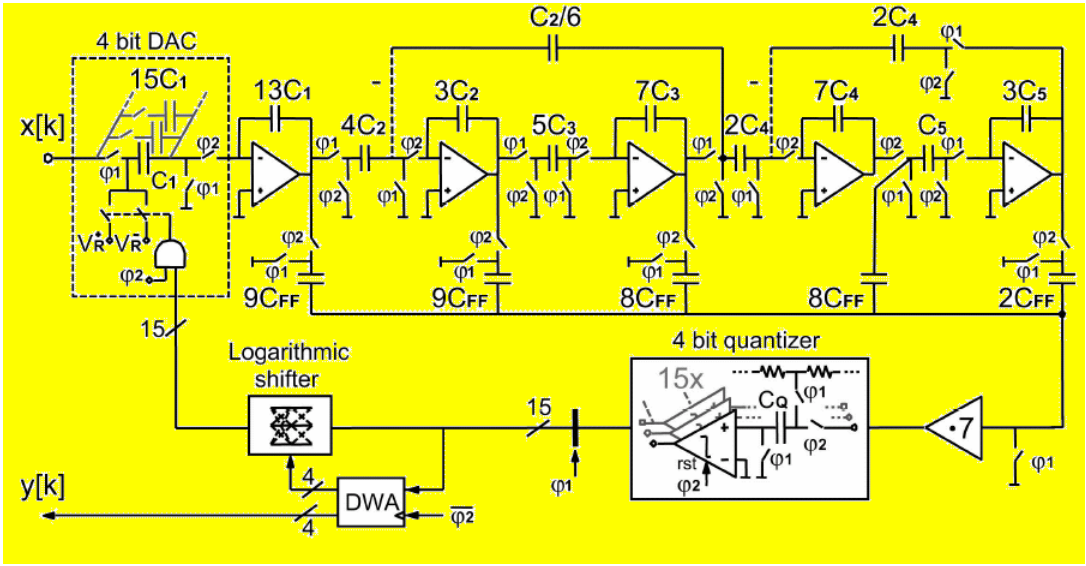


Fig. 2.9 Balmelli 5th-order Sigma-Delta modulator

Better performance has been achieved by Balmelli [Bal04]. The 5th-order architecture is shown in Fig. 2.9 in which all five integrator outputs are fed forward to the quantizer before the global feedback. Local feedback loops are introduced around the last two pairs of integrators to create two pairs of poles in the forward path of the closed-loop signal transfer function. Since the same poles are in the feedback path for the quantizer error, two pair of transmission zeros are created only for the quantization noise transfer function that result in two very deep notchs of the noise spectrum[Bal04]. The loop filter coefficients have been carefully chosen to optimize three aspects of performance. The first is effective highpass shaping of quantization noise. The second is stability and recoverability from overload saturation without forced reset. The third is a low spread of capacitor ratios, so that kT/C noise can be lowered by larger minimum capacitors for each independently scaleable group [Bal04].

2.3.3 Cascade

An alternative scheme to realize high-order noise-shaping is to cascade multiple first and second-order Sigma-Delta A/D modulators. Such architecture is called MASH or cascaded

Sigma-Delta A/D modulator [Mat87] [Lon88] [Cho89] [Reb90]. It is unconditionally stable.

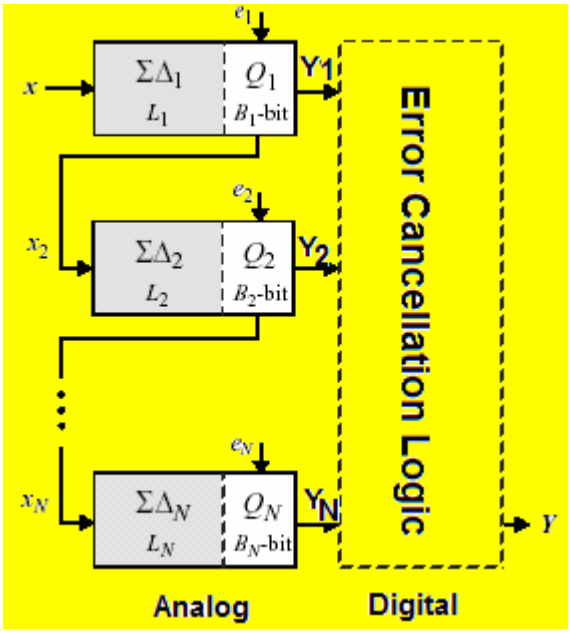


Fig. 2.10 Generic N-stage cascade Sigma-Deltą modulator

Fig. 2.10 shows the generic basic block diagram of a cascaded Sigma-Delta A/D modulator [Med99a]. It consists of several stages of Sigma-Delta modulators, in which each stage re-modulates a signal that contains the quantization error generated in the previous stage. Once the outputs of the stages are properly processed and combined in the digital domain, the quantization errors of all the stages can be canceled out, except for the last one in the cascade. This error at the overall modulator output is shaped by a function of the order equal to the summation of the order of all the stages. Furthermore, since only 1st- and/or 2nd-order Sigma-Delta modulators are cascaded and all feedback loops are local, unconditionally stable high-order shaping can be obtained. The performance of a multistage Sigma-Delta modulator is therefore similar to that of a theoretical high-order loop without instability problems.

In order to illustrate the operation of cascade Sigma-Delta modulators, let us consider the 3rd-order cascade as shown in Fig.2.11, in which a second-order converter is cascaded by a first-order Sigma-Delta. Using linear analysis, the output of the first second-order loop in the z-domain Y_1 (z) can be written as [Rio04b]:

$$Y_1(z) = \frac{g_1 g_2 z^{-2} X(z) + \left(1 - z^{-1}\right)^2 E_1(z)}{1 + (g_2^{'} - 2)z^{-1} + (1 + g_1^{'} g_2 - g_2^{'})z^{-2}} \qquad 2.3.15$$

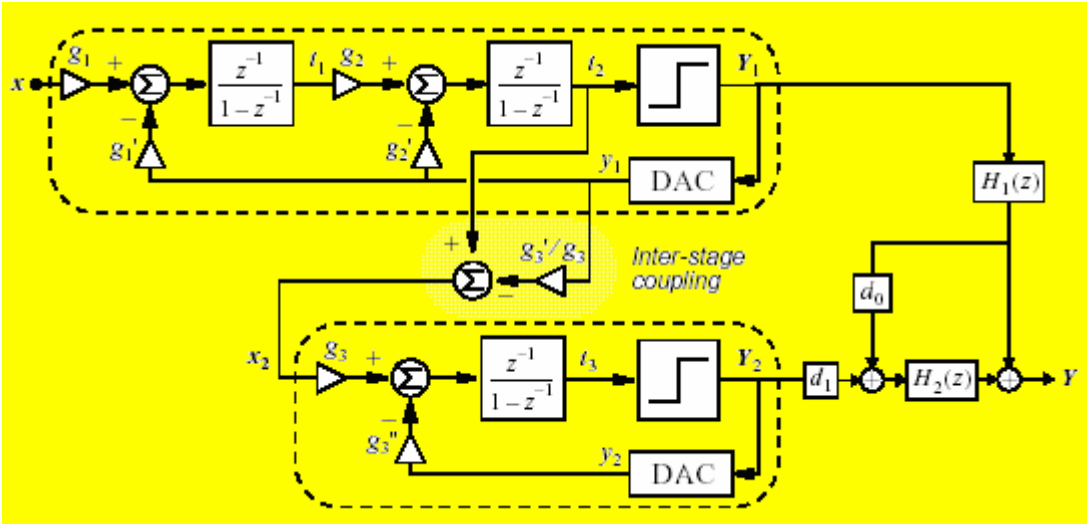


Fig. 2.11 2-1 3rd-order 2-stage cascade Sigma-Deltą modulator

where X(z) and $E_1(z)$ are the input signal and the quantization error of the first quantizer, respectively. In order to obtain the 1st-stage output:

$$Y_1(z) = z^{-2} X(z) + \left(1 - z^{-1}\right)^2 E_1(z) \qquad 2.3.16$$

the following condition must be fulfilled:

$$g_1^{'} = g_1, \; g_1^{'} g_2 = 1 \text{ and } g_2^{'} = 2 g_1^{'} g_2 \qquad 2.3.17$$

The input to the second stage $X_2(z)$ is a linear combination of the input and output signals of the 1st-stage quantizer, given by

$$X_2(z) = I_2(z) - \frac{g_3^{'}}{g_3} Y_1(z) = Y_1(z) - E_1(z) - \frac{g_3^{'}}{g_3} Y_1(z) \qquad 2.3.18$$

Whereas the output of the second first-order loop in the z-domain can be written as:

$$Y_2(z) = \frac{g_3 z^{-1} X_2(z) + \left(1 - z^{-1}\right) E_2(z)}{1 + (g_3^{''} - 1)z^{-1}} = g_3 z^{-1} X_2(z) + \left(1 - z^{-1}\right) E_2(z) \qquad 2.3.19$$

where E2(z) stands for the quantization error of the quantizer in the second stage with $g_3^{''} = 1$. Substituting the former Equations (2.3.16) (2.3.18), Y2 (z) yields [Nor97]

$$Y_2(z) = \frac{g_1}{g_1'}\left(\frac{g_1' g_2 g_3}{g_3''} - \frac{g_3'}{g_3''}\right) z^{-3} X(z) + \left(1 - z^{-1}\right) E_2(z) + \left[\left(\frac{g_1' g_2 g_3}{g_3''} - \frac{g_3'}{g_3''}\right)\left(1 - z^{-1}\right)^2 - \frac{g_1' g_2 g_3}{g_3''}\right] z^{-1} E_1(z) \qquad 2.3.20$$

which involves the input signal, 1st-order shaped quantization error from the second stage, and second-order shaped and unshaped quantization error from the first stage. If the output of the stages is correctly processed in the digital domain with the cancellation logic given by:

$$d_0 = \frac{g_3'}{g_1' g_2 g_3} - 1 \qquad d_1 = \frac{g_3''}{g_1' g_2 g_3} \qquad H_1(z) = z^{-1} \qquad H_2(z) = \left(1 - z^{-1}\right) \qquad 2.3.21$$

the overall output of the 2-1 cascade Sigma-Delta modulator yields

$$Y(z) = \frac{g_1}{g_1'} z^{-3} X(z) + \frac{g_3''}{g_1' g_2 g_3}\left(1 - z^{-1}\right)^3 E_2(z) \qquad 2.3.22$$

Therefore, $Y(z)$ contains only a delayed version of the modulator input and a 3rd-order shaped version of the 2nd-stage quantization error, whereas the quantization error of the 1st-stage is completely cancelled thanks to the cancellation logic. As a result, its performance is similar to that of an ideal Sigma-Delta modulator with a 3rd-order FIR noise transfer function, but unconditionally stable by construction.

The in-band quantization error power of the 2-1 cascade Sigma-Delta modulator is: [Nor97]

$$P_Q \approx d_1^2 \frac{\Delta_2^2}{12} \frac{\pi^6}{7 OSR^7} \qquad 2.3.23$$

where Δ_2 is the quantization step of the 2nd-stage quantizer. Note that the performance would equal to that of an ideal 3rd-order Sigma-Delta modulator if $d_1=1$, but it will be lower if $d_1>1$, because of the amplification of the quantization error by the factor d_1^2. Unfortunately, d_1 equals to $g_3''/g_1' g_2 g_3$, so that reducing d1 involves increasing the integrator weights, which may lead to an excessively large swing of the internal state variables and/or a premature overload of the quantizers. Thus, a trade-off must be established between minimizing the excess of in-band quantization error and maximizing the overload level and peak SNR of the cascade Sigma-Delta modulator [Rio04b].

In general, for a N-stage cascade Sigma-Delta modulator like the one shown in Fig.2.9, a stable Lth-order Sigma-Delta modulator can be built by cascading stages of second order or lower. If the stages outputs are adequately processed in the digital domain, only the modulator input signal *X(z)* and the last-stage quantization error $E_N(z)$ remain in the z-domain modulator output, yielding

$$\begin{aligned} Y(z) &= STF(z) * X(z) + NTF(z) * E_N(z) \\ &= z^{-L} X(z) + d_{2N-3}(1 - z^{-1})^L E_N(z) \end{aligned} \qquad 2.3.24$$

where $L = L_1 + L_2 + \ldots + L_N$ and d_{2N-3} is the *scaling factor* related to the integrator weight that amplifies the last-stage quantization error.

The corresponding in-band quantization error power of a N-stage cascade is then given by [Med99a]

$$P_Q \approx d_{2N-3}^2 \frac{\Delta_N^2}{12} \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} \qquad 2.3.25$$

with Δ_N being the level spacing in the B_N-bit quantizer of the N^{th} stage. Hence, the performance corresponds to that of a theoretical L_{th}-order B_N–bit Sigma-Delta modulator, except for the scalar factor d_{2N-3} that causes a systematic loss of performance. Common values for this amplifying factor are 2 and 4, which lead to a decrease of SNR in 6dB (1bit) and 12dB (2bit), respectively. However, these performance degradations, inherent to multi-stage Sigma-Delta modulators, are considerably lower than the ones shown in Section 2.3.2 for high-order single-loop architectures.

In the last years, many designed approaches and architectures have been proposed for higher loop-order modulator, such as 4^{th}-order cascades: 2-2 Sigma-Delta modulators [Mia98] [Mar98b], 5^{th}-order cascades: the 2-2-1 Sigma-Delta modulator [Vle01] and the 2-1-1-1 Sigma-Delta modulator [Rio00a], as well as the 6^{th}-order 2-2-2 cascade [Ded94] [Fel98]. The focuses on the cascade Sigma-Delata modulator topology are:

- Minimizing the scaling factor that determines the loss of resolution.
- Maximizing the output swing to ensure a high peak SNR.
- Minimizing the required output swing of the integrators, especially in low-voltage implementations.

- Simplifying the set of analog coefficients to be easily implemented as capacitor ratios using unit elements.
- Reducing the total number of unit capacitors to save silicon area.

2.3.4 Comparison

The key issue of designing high-speed Sigma-Delta modulators is to lower the oversampling ratio [Fel98a], and thus maximize the signal bandwidth by a given technology. Since the simultaneously desired performance is the high resolution for the communication systems, the order number of the Sigma-Delta modulator has to be increased, and/or multi-bit quantizer has to be used.

As mentioned in the previous sections, the single-loop high order structures have a low attenuation of in-band quantization noise, and, consequently, low achievable SQNR, since non-zero poles have to be inserted in the NTF to ensure stability. Whereas the high-order cascaded MASH structures are unconditionally stable. The noise-transfer-function (NTF) of this type Sigma-Delta modulators approximates the theorectical NTF of $(1-z^{-1})$. Therefore, cascade Sigma-Delta modulators can achieve much higher resolution than the single-loop one with the same loop-order, OSR and internal quantization, particularly at low OSR.

2.4 Summary

The principles of Sigma-Delta modulators have been studied in the chapter and various alternative modulator topologies have been presented. The achievable performance of different architectures has been addressed by only taking into account the quantization error. In single-loop Sigma-Delta architectures, non-zero poles need to be introduced in NTF to suppress the out-of-band gain, and therefore stabilize the modulator loop. Consequently, the single-loop Sigma-Delta architectures obviously degrade the achievable signal-to-noise ratio (SNR). The cascade multibit Sigma-Delta modulator (MASH) structures greatly relieve the constraint on the stability of high-order loop, so that they offer a good compromise between high accuracy and speed.

Chapter 3 Non-Idealities on Sigma-Delta Modulators

3.1 Introduction

This chapter will investigate circuits' non-idealities in Sigma-Delta A/D converters and present corresponding behavioral models. These effects of circuits' non-idealities on performance of Sigma-Delta A/D will be intuitively illustrated by the simulation of the PSD vs. frequency by means of the constructed behavioral models.

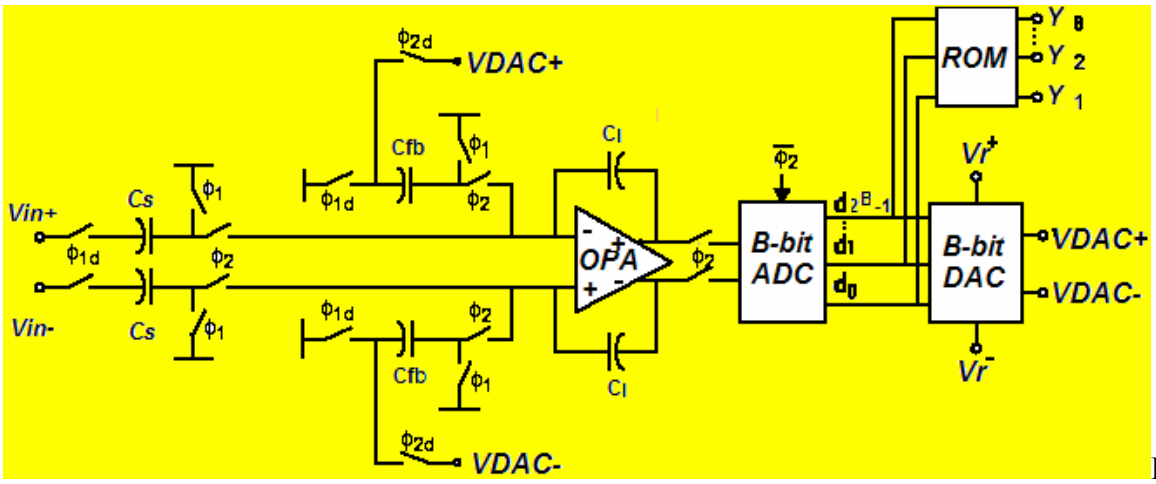


Fig. 3.1. Schematic of an SC first-order Sigma-Delta modulator

The block diagram of a first-order SC Sigma-Delta modulator is shown in Fig. 3.1. The modulator consists of input samplers, an SC integrator, a quantizer and a feedback digital-to-analog converter (DAC). The non-idealities can be categorized in six classes: Sampler related errors, such as sampling jitter; integrator related noises, such as kT/C and opamp noises, integrator related non-idealities, which are caused by finite key parameters of opamps (finite gain, finite bandwidth, slew-rate and saturation voltages); comparator related ones and the DAC non-idealities.

Although non-idealities occur on all topologies (single-loop, cascade, multi-bit), it does not

mean that the impact of these non-idealities is the same for all topologies. The impact differences will also be introduced in this chapter.

3.2 Sampler related errors

3.2.1 Clock jitter

Jitter is mainly caused by thermal noise, phase noise and spurious components in every clock-generation circuitry —i.e., crystal oscillators, PLL-based oscillators, etc. In a SC circuit, clock jitter can be defined as a short-term, non-cumulative variation of the switching instant of a digital clock form from its ideal position in time [Lee01] (see Fig.3.2*a*). It results in a non-uniform sampling time sequence, and produces an error which increases the total error power at the quantizer output.

When a sinusoidal input signal x(t) with amplitude A_x and frequency f_x is sampled at an instant, which is in error by a statistical non-uniform uncertainty Δt, the magnitude of this error, as illustrated in fig. 3.2(b), is given by[Bos88]

$$e(nT_s + \Delta t) = x(nT_s + \Delta t) - x(nT_s) = \Delta t \frac{d}{dt} x(t)\Big|_{nT_s} = 2\pi f_x A_x \cos\left[2\pi f_x nT_s\right]\Delta t \qquad 3.2.1$$

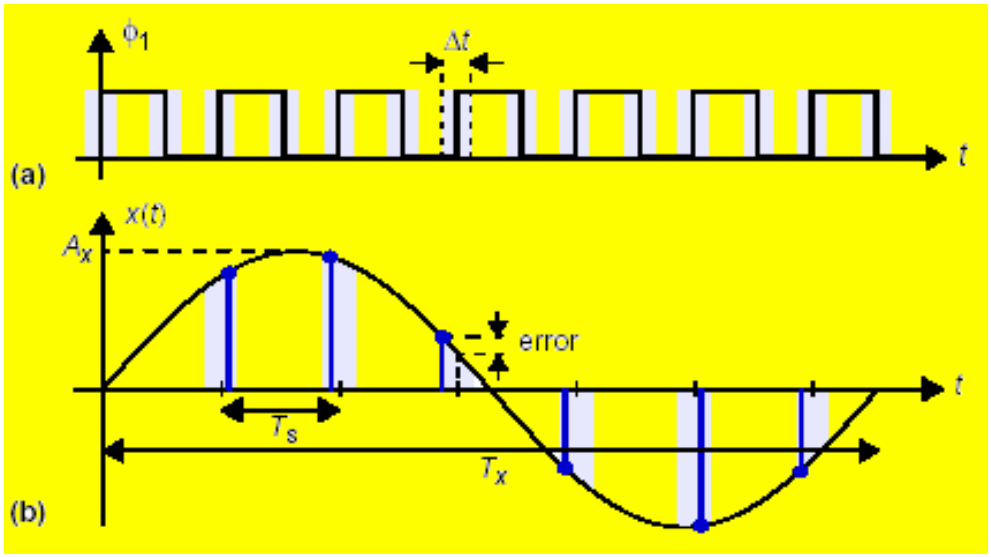


Fig. 3.2 (a) Jitter in a digital clock signal; (b) Effect of clock jitter in the sampling.

This error can be modeled at the behavioral level as shown in Fig. 3.3 [Bri99], where the continuous-time input signal X and the magnitude of this jitter error are firstly summed together in the output, and then the actual sample value is implemented by a zero-order hold block with sampling period T_s. The random noise signal is implemented with a random block, which creates a sequence of random numbers with Gaussian distribution, zero mean, and unity standard deviationσ. Since assuming that the jitter is white noise, the resultant error has an uniform power-spectral density (PSD) from 0 to fs/2, with total power of $(2\pi f_x \sigma A)^2 / 2$. Therefore, the in-band jitter noise power is given by

$$P_J = \int_{-f_b}^{f_b} S_J \, df = \frac{(2\pi f_{in} \sigma A)^2}{2 * OSR} \qquad 3.2.2$$

In this case, high oversampling is helpful in reducing the error [Bos88].

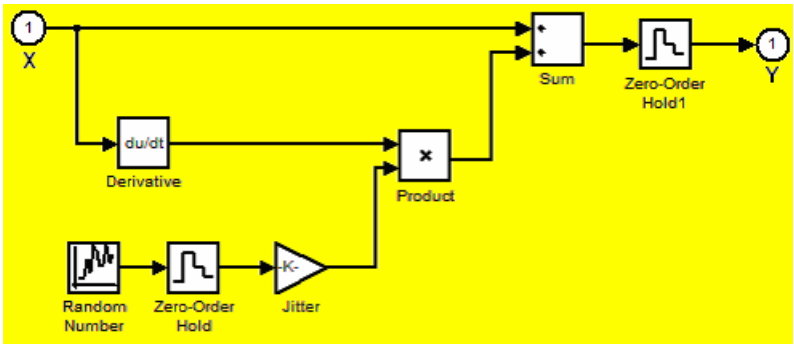


Fig. 3.3. Modeling a random sampling jitter

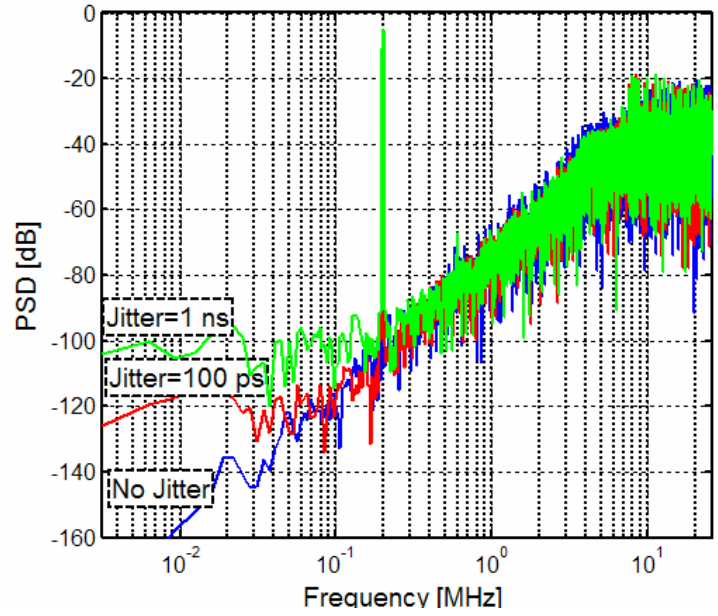


Fig3.4 (a) Effect of jitter error on PSD of second-order modulator (fx=200KHz)

Note that once the analog signal has been sampled, the variation of the clock period has no direct effect on the circuit performance. Consequently, clock jitter is introduced only by sampling the input signal, and the effect of clock jitter on a Sigma-Delta modulator is independent of the structure or the order of the modulator.

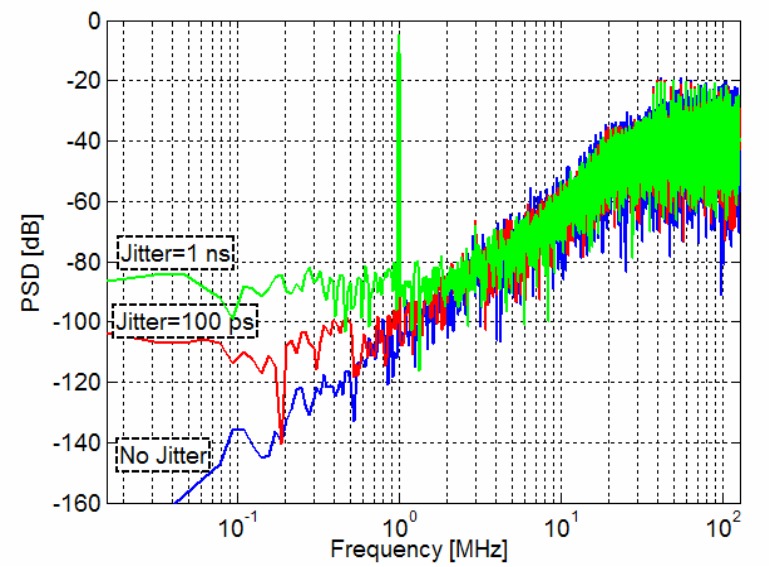


Fig3.4 (b) Effect of jitter error on PSD of second-order modulator (fx=1MHz)

Fig.3.4 (a) (b) show the effects of jitter error on PSD of a second-order Sigma-Delta modulator, where the input frequency is 200 KHz and 1MHz, respectively. The PSDs of the ideal case have a slope of 40dB/decade that indicates a second-order noise shaping of the quantization noise over a wide band of frequency. The jitter error dominates the noise floor at lower in-band frequency, and the noise floor increases as the jitter increases. Comparing with Fig.3.4 (a) and Fig.3.4 (b), it is shown that the jitter error is dependent on the frequency of input signal: the higher the frequency of the input signal, the more error power will be introduced with the same time deviation.

3.3. Integrator related noises

3.3.1 Thermal noise

Thermal noise is generated by the switches in the SC integrators due to the random thermal energy motion of electrons; it is present even at equilibrium. In a switched-capacitor integrator, two switchs are turned on or off at the same instant. Since both switch transistors work in the triode region, the noise has a mean-square value within the bandwidth Δf (in Hz) [Shr05]:

$$\overline{v^2} = 8kTR_{on}\Delta f \qquad 3.3.1$$

Where k is the Boltzman constant, T is the absolute temperature in Kelvin. At room temperature 4kT = 1.66 x 10-20 V-C.

The total power (mean-square value) $_{PN,TOT}$ of the SC-integrator are calculated by evaluating the integral for all frequencies: [Gra01] [Sch05]

$$P_{N,TOT} = \int_0^\infty \frac{\overline{v^2}}{\Delta f} \frac{1}{\left|1 + j2\pi 2R_{on}C_S f\right|^2} df = \int_0^\infty \frac{8kTR_{on}}{1 + \left(4\pi R_{on}C_S f\right)^2} df = \frac{kT}{C_S} \qquad 3.3.2$$

Therefore, in order to effectively reduce the power of the folded-back thermal noise, C_s must be increased. Note that reducing R_{on} is useless for reducing the total noise power [Gra01].

The switched thermal noise voltage e_T appears as an additive noise to the input voltage x(t), which leads to

$$y(t) = \left[x(t) + e_T(t)\right]c = \left[x(t) + \sqrt{\frac{kT}{C_S}}n(t)\right]c = \left[x(t) + \sqrt{\frac{kT}{cC_i}}n(t)\right]c \qquad 3.3.3$$

where n(t) denotes a Gaussian random process with unity standard deviation, and c is the integrator gain and $c=C_s/C_i$. The behavior model of the switched thermal noise is shown in Fig. 3.5. [Bri99].

The KT/C noise at the input integrator is dominating, since the white noise introduced in the subsequent integrators will be noise shaped by high-pass filters. Therefore, Capacitors in the subsequent integrators can be scaled down.

Fig.3.6 shows that KT/C noise of a second-order Sigma-Delta modulator has the same

effect on the PSD as that of a clock jitter. The KT/C noise increases the noise floor at lower in-band frequencies, and the noise floor increases as the sampling capacitor decreases.

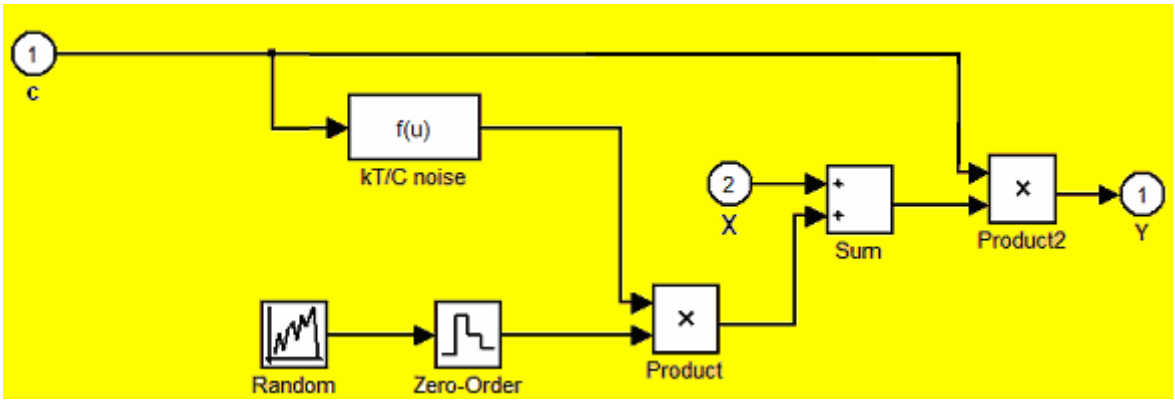


Fig. 3.5. Modeling the thermal noise (kT/C block)

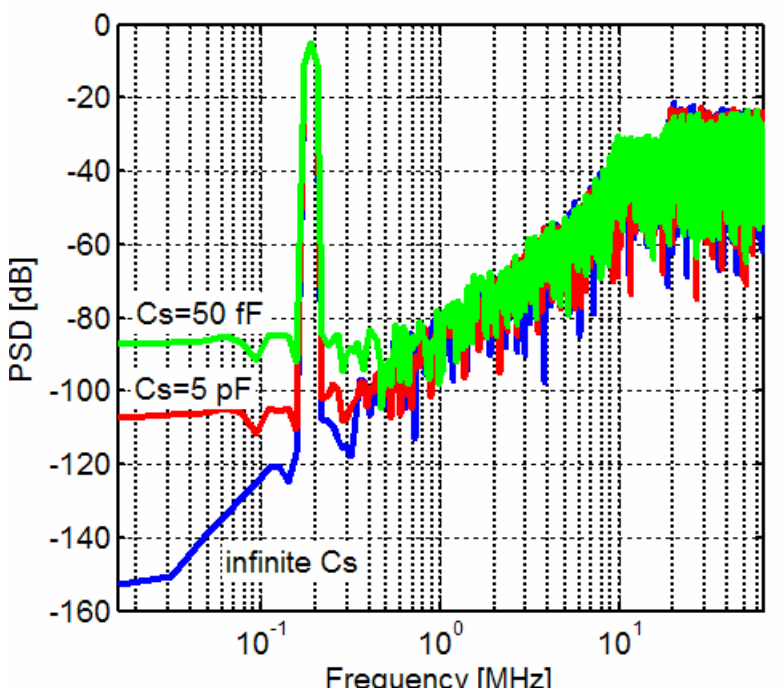


Fig3.6 Effect of KT/C noise on PSD of second-order modulator

3.3.2. Op-Amp noise

The noise voltage source in the opamp generally consists of a thermal (v_s) and a flicker component (v_f). For a MOSFET operating in strong inversion region, the thermal noise can be modeled by a current source in parallel with the channel. The mean-square value of the

input-referred thermal noise within the bandwidth Δf (in Hz) of a MOSFET in saturation is approximately [Gra01] [Sch05]:

$$\overline{v_{op,th}^{\,2}} = \frac{8kT}{3g_m}\Delta f \qquad 3.3.4$$

The flicker (or 1/*f*) noise, which is nearly independent of the bias condition, is approximated by

$$\overline{v_{op,f}^{\,2}} = \frac{k}{C_{ox}WL}\frac{\Delta f}{|f|} \qquad 3.3.5$$

where *k* is a process- and temperature-dependent parameter. Flicker noise dominates at low frequencies and decreases with the increase of frequencies. The frequency at which 1/f noise is equal to the white thermal noise is called corner frequency f_{cr}. Beyond f_{cr}, thermal noise dominates.

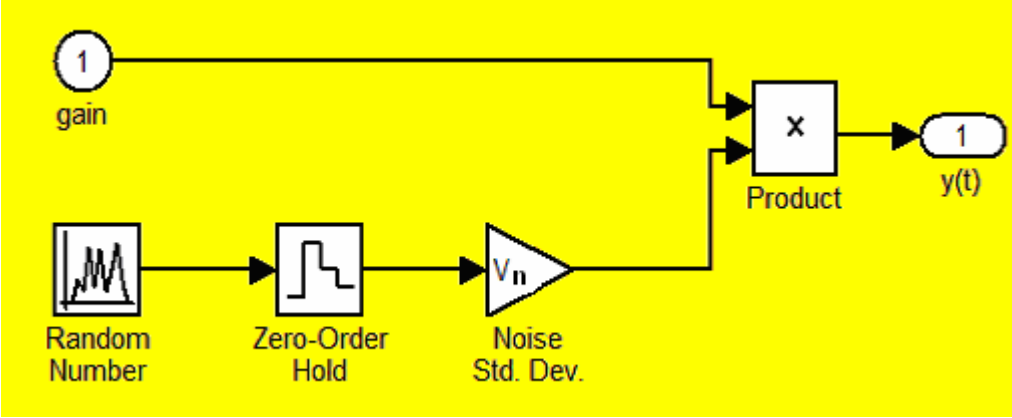


Fig. 3.7 Op-amp noise behavior model

The flicker (1/*f*) noise and wide-band opamp thermal noise are uncorrelated in the same device, so their noise powers can be directly added together. Practically they can be obtained from circuit simulation, calculation and measurement during the integration phase, by adding the noise contributions of all the devices referred to the op-amp input and integrating the resulting value over the whole frequency spectrum [Bri99]. If assuming that the total rms noise voltage referred to the op-amp input is V_n, the behavior model of the effect of the opamp noise on Sigma-Delta modulators can be simplified as Fig. 3.7. Fig.3.8 shows the PSDs of the second-order Sigma-Delta modulator with and without opamp

noise. The opamp noise increases the noise floor at lower in-band frequency, and the noise floor increases as the opamp noise increases.

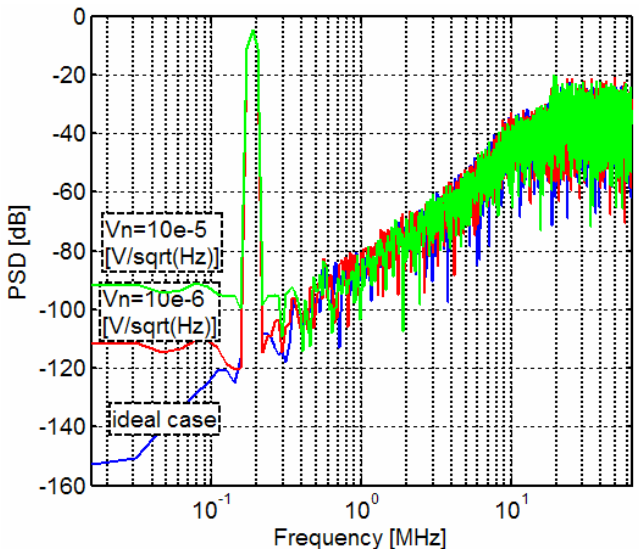


Fig. 3.8 Effect of opamp noises on PSD of second-order modulator

Note the thermal noise of the opamp is considerably lower than that of the switches by comparing Eq. 3.3.1 and Eq. 3.3.4, and the flick noise can be suppressed by using big device with big length (L), width (W) or both.

3.4 Integrator related non-idealities

3.4.1 Integrator leakage

3.4.1.1 Model of integrator leakage

The integrator leakage caused by finite-DC-gain of the opamp in the integrator can be modeled with a variable "alpha". In the SC integrator shown in Fig. 3.1, the parameter α is approximated with [Yin94]:

$$\alpha \cong \frac{A_0 C_I}{A_0 C_I + C_S + C_{fb}} \qquad 3.4.1$$

where A_0 is the finite DC-gain of opamps, C_I, C_S and C_{fb} stand for the integration,

sampling and feedback capacitor. The transfers function of the integrator with leakage becoms

$$H(z) = \frac{z^{-1}}{1 - z^{-1}\alpha} \qquad 3.4.2$$

Therefore, the pole location is shifted. It can be modeled in Simulink as illustrated in Fig. 3.9. [Bri99].

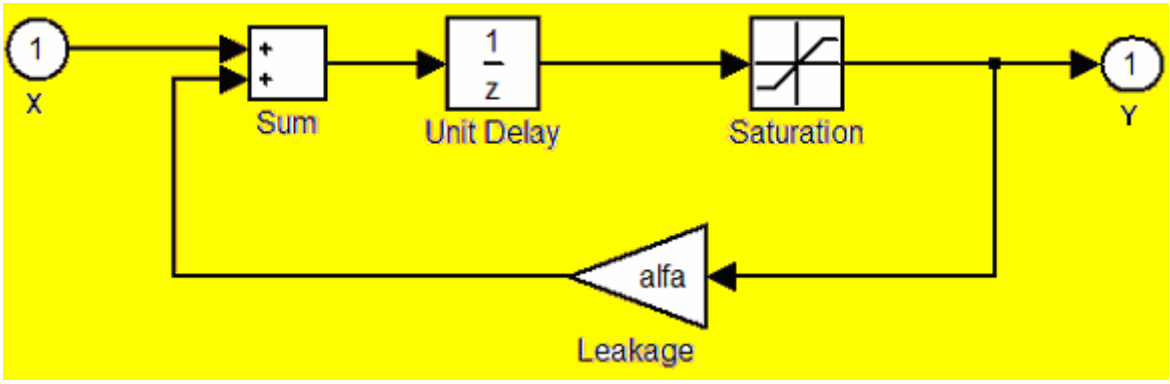


Fig. 3.9 Real integrator model with leakage

The output voltage of a real amplifier is not rail-to-rail but bounded to a voltage smaller than the supply voltage (determined by the drain-source saturation voltages of the output transistors). This effect is easily taken into account at a high level by clipping the output voltage. This can simply be done in SIMULINK using the saturation block inside the loop of the integrator, as shown in Fig. 3.9.

3.4.1.2 Impact on single-loop Sigma-Delta modulators

Considering the integrator leakage, specifically, when α approximates to 1, in a 1st-order loop, the STF and NTF of the modulator are given, respectively:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{\frac{z^{-1}}{1-\alpha z^{-1}}}{1+\frac{z^{-1}}{1-\alpha z^{-1}}} = \frac{z^{-1}}{1+(1-\alpha)z^{-1}} \cong z^{-1} \qquad 3.4.3$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+\frac{z^{-1}}{1-\alpha z^{-1}}} = \frac{1-\alpha z^{-1}}{1+(1-\alpha)z^{-1}} \cong \left(1-z^{-1}\right)+(1-\alpha)z^{-1} \qquad 3.4.4$$

Note from Eq. 3.4.3 that the leakage affects the signal transfer function introducing a gain error that, in general, will be negligible. On the other hand, the leakage (1-α) shifts the zero location away from its ideal position at z=1 (DC) in the noise-shaping function. Note that the first term corresponds to the ideal 1st-order shaping, whereas the leakage adds a second term that is not shaped.

By doing the transformation z→exp(j2πf/fs), the in-band error power at the modulator output under this degradation of the integrator leakage can be calculated as [Rio04b]

$$P_Q = \int_{-f_b}^{+f_b} \frac{\Delta^2}{12} |NTF(f)|^2 \, df \approx \frac{\Delta^2}{12}\left(\frac{\pi^{2L}}{(2L+1)OSR^3} + \frac{(1-\alpha)^2}{OSR} \right) \qquad 3.4.5$$

with f_b being the signal bandwidth, f_s the modulator sampling frequency, OSR= $f_s/(2f_b)$ the oversampling ratio, and Δ the spacing between adjacent levels in the quantizer. Note from Eq. 3.4.5, that the first term is inversely proportional to the corresponding ideal 1st-order shaped quantization error, whereas the second term introduced by the leakage is proportional to $(1-\alpha)^2$ and inversely proportional to OSR. This second term may dominate the in-band error power for low amplifier DC-gains and/or low oversampling ratios.

For a second-order single-loop Sigma-Delta modulator, the noise transfer function can be calculated with: [Rio04b]

$$\begin{aligned} NTF(z) &= \frac{1}{\left(1+\frac{z^{-1}}{1-\alpha_1 z^{-1}}\right)\left(1+\frac{z^{-1}}{1-\alpha_2 z^{-1}}\right)} = \frac{\left(1-\alpha_1 z^{-1}\right)}{1+(1-\alpha_1)z^{-1}} \times \frac{\left(1-\alpha_2 z^{-1}\right)}{1+(1-\alpha_2)z^{-1}} \\ &\cong \left(1-z^{-1}\right)^2 + z^{-1}\left(1-z^{-1}\right)\left((1-\alpha_1)+(1-\alpha_2)\right) + z^{-2}(1-\alpha_1)(1-\alpha_2) \end{aligned} \qquad 3.4.6$$

where $1-\alpha_1$ and $1-\alpha_2$ are integrator leakages at the first and second integrator, respectively. The in-band error power at the second-order modulator can be calculated as

$$P_Q \cong \frac{\Delta^2}{12}\left(\frac{\pi^4}{5OSR^5} + \frac{\left((1-\alpha_1)+(1-\alpha_2)\right)^2 \pi^2}{3OSR^3} + \frac{(1-\alpha_1)^2(1-\alpha_2)^2}{OSR} \right) \qquad 3.4.7$$

Note that the first term in Eq. 3.4.7 corresponds to the ideal second-order shaped quantization error, whereas the leakage-introduced term of $((1-\alpha_1)+(1-\alpha_2))^2$ is first-order shaped and the term of $(1-\alpha_1)^2(1-\alpha_2)^2$ non-shaped.

If same integrators with integrator leakage (1-α) are applied, these expressions can be generalized for an Lth-order single-loop modulator as follows [Rio04b]

$$NTF(z)=\frac{Y(z)}{E(z)}=\frac{1}{1+\left(\frac{z^{-1}}{1-\alpha z^{-1}}\right)^{L}}=\left[\frac{1-\alpha z^{-1}}{1+(1-\alpha)z^{-1}}\right]^{L}\cong\left[\left(1-z^{-1}\right)+(1-\alpha)z^{-1}\right]^{L} \qquad 3.4.8$$

From Eq. 3.4.8, the in-band power can be calculated, which is given by [Rio04b]:

$$P_{Q}=\approx\frac{\Delta^{2}}{12}\left(\frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}+\frac{(1-\alpha)^{2L}}{OSR}+\sum_{m=1}^{L-1}\frac{L(L-1)\ldots(L-m+1)}{m!}\frac{(1-\alpha)^{2(L-m)}\pi^{2m}}{(2m+1)OSR^{(2m+1)}}\right) \qquad 3.4.9$$

Note that in an Lth-order loop, L terms corresponding to shapings of order 0, 1, 2, …, L-1 are added. These extra terms are proportional to decreasing powers of 1-α—i.e., $(1-\alpha)^{2L}$, $(1-\alpha)^{2(L-1)}$, … $(1-\alpha)^{4}$, $(1-\alpha)^{2}$, respectively— so that, for usual values of the oversampling ratio and the amplifier DC-gain, the dominant extra term is that with a shaping of order L-1. [Rio04].

3.4.1.3 Impact on cascade Sigma-Delta modulators

In a MASH or cascaded N-stage architecture, the shift in pole location of the integrator transfer-function results in incomplete cancellation of the quantization noise from the previous stages, so their quantization errors can not be completely canceled by the subsequent digital signal processing. The output of the modulator can be described by the equation below,

$$Y(z)=STF(z)X(z)+NTF_{N}E_{N}(z)+\sum_{i=1}^{N-1}NTF_{i,leakage}(z)E_{i}(z) \qquad 3.4.10$$

Where the $NTF_{i,leakage}$ indicates the integrator leakage term of a Lth-order modulator in the ith stage. For example, from Eq. 3.4.4 and Eq. 3.4.6, it is obtained that the NTF leakage of the first-order and the second-order modulators are $(1-\alpha)z^{-1}$ and $2(1-\alpha)(1-z^{-1})+(1-\alpha)^{2}z^{-2}$, respectively.

3.4.1.4 Comparison

In order to intuitively compare the impact on Sigma-Delta modulators, the model of

the integrator leakage is incorporated in a cascade 2-1-1-1 (4bit) [Rio00a] and a single-loop 5th-order 4bit [Bal04] Sigma-Delta modulator. The oversamping ratio is chosen 8 and 16 for the cascade and the single-loop, respectively. Note that the OSR of the single-loop is chosen as high as double of the cascade, to achieve the comparable SNR, as mentioned in section 2.3.2.

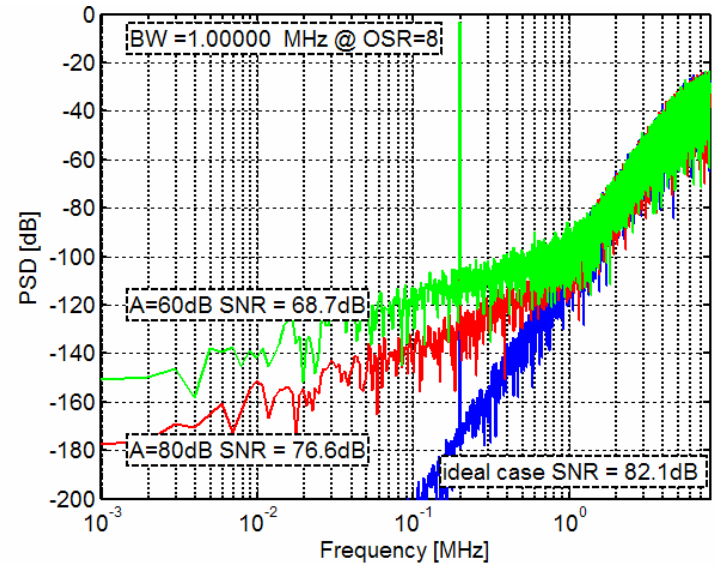


Fig. 3.10. PSD of the cascade 2-1-1-1(4bit) at OSR of 8 for different DC-gain implementations.

Fig.3.10 illustrates the PSD curves of cascade 2-1-1-1 (4bit) Sigma-Delta modulator at OSR of 8 for different opamp DC-gains. Fig.3.11 illustrates the PSD of the 5th-order 4bit single-loop one at OSR of 16 for different DC-gains. Comparing them, it is found that the system noise floor increases due to finite DC-gain, which will significantly attenuate the SNR, but not the SFDR. The added noise part causes that the quantization noise in the previous stages of cascade one can not completely canceled in the digital domain, therefore cascade topologies present a higher sensitivity to the finite DC-gain than single-loop topologies. In the simulation examples, for a 1-bit loss in DR, over 80dB opamp DC-gain is required at OSR of 8 as shown in Fig. 3.10. Whereas the single-loop structure is very immune to the integrator leakage as shown in Fig.3.11, so that the impact due to the finite DC-gain can be neglected. Comparing the impacts on single-loop and cascade topologies, it is obvious that every stage, except for the last stage, contributes to the additional noise power due to integrator leakage. Consequently, cascade topologies are always more

sensitive to leakages than single-loop topologies; and the sensitivity rapidly increases when increasing the order of the modulator, unlike single-loop topologies.

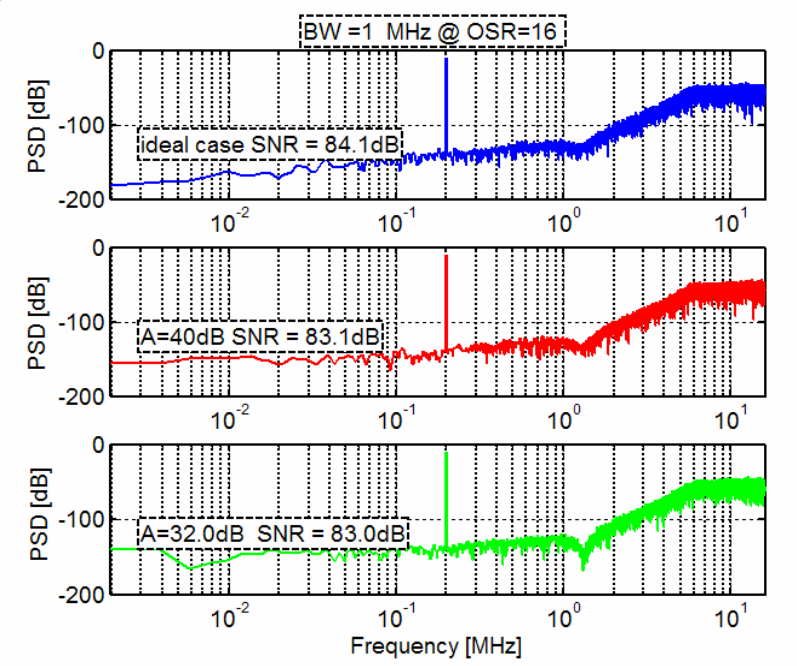


Fig. 3.11 PSD of 5th-order single-loop with 4b quantizer at OSR of 16 for different DC-gain implementations.

3.4.2 Integrator weight variation

3.4.2.1. Model of integrator weight variation

The integrator weights are implemented by means of capacitor ratios in the SC integrator. The variation of process parameters and sizes makes the integrator weights have a small deviation ε from their nominal values. In the worse case, the weight *gi* (m over n unit capacitors) is assumed as three times its relative standard deviation and $\sigma_C=\sigma_{CN}/C_N$, the error parameter ε is approximated with [Rio04b]:

$$\varepsilon \cong \frac{3\sigma_{gi}}{g_i} = 3\sqrt{\frac{1}{m}+\frac{1}{n}}\sigma_C \qquad 3.4.11$$

It indicates that the errors may be further decreased if total number of unit capacitors is increased, to implement the weights of a given integrator.

The behavior model is illustrated in Fig. 3.12., where the integrator weight g and the small deviation are firstly summed together; then the actual value is multiplied by the sampled input signal IN as the input of the integrator. The small deviation is implemented with a random block with Gaussian distribution, mean value of zero, and standard deviation of σ, where the gain -k- is equal to $\sqrt[3]{\frac{1}{m}+\frac{1}{n}}$.

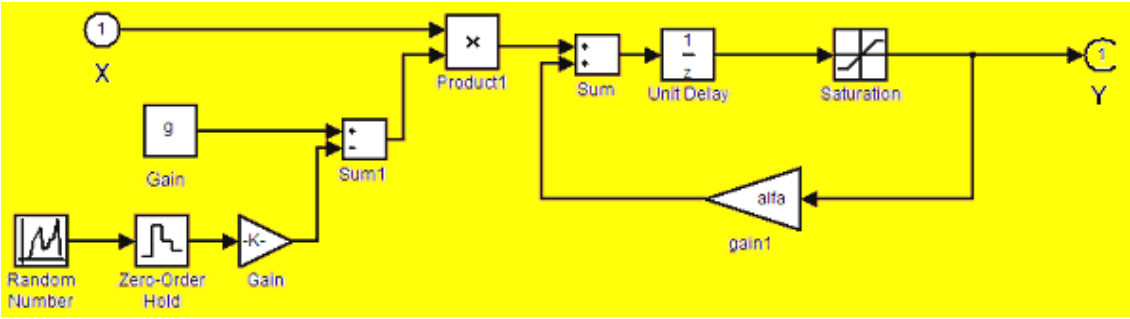


Fig. 3.12 Weight variation model due to capacitor mismatch

3.4.2.2 Impact on single-loop Sigma-Delta modulators

Assuming that the actual integrator weights gi deviate from their nominal values with a small error term εgi, then the actual weights are gi*= gi (1±εgi). In the general case g1=g1' and g2'=2g1'g2, the signal transfer function can be calculated as:

$$STF(z) \cong \left(1 - \left|\varepsilon_{g1'} - \varepsilon_{g1}\right|\right) z^{-2} \qquad 3.4.12$$

the noise transfer function can be calculated:

$$NTF(z) \cong (1 + (\varepsilon_{g2} + \varepsilon_{g1'}))(1 - z^{-1})^2 \qquad 3.4.13$$

where the terms in ε_{gi}^2 have been neglected [Rio04b].

The in-band error power at the second-order modulator under capacitor mismatching can be calculated as [Rio04b]

$$P_Q \approx \frac{\Delta^2}{12}\left(\frac{(1+(\varepsilon_{g2}+\varepsilon_{g1'}))\pi^4}{5 OSR^5}\right) \qquad 3.4.14$$

These aforementioned expressions can be extend to an Lth-order single-loop modulator as follows

$$Y(z) \cong z^{-L} X(z) + (1+\varepsilon_g)(1-z^{-1})^L E(z) \qquad 3.4.15$$

where $\varepsilon_g=\varepsilon_{g1}'+\varepsilon_{g2}+\ldots\ \varepsilon_{gL}$.

$$P_Q \cong \frac{\Delta^2}{12}\frac{(1+\varepsilon_g)^2 \pi^{2L}}{(2L+1)OSR^{2L+1}} \qquad 3.4.16$$

Note that the error power due to capacitor mismatch is shaped by an one-order higher high-pass filter than that due to finite open-loop gain.

3.4.2.3 Impact on Cascade Sigma-Delta modulators

In the same manner, the output of a cascaded Lth-order N-stage modulator can be described by the equation as below: [Rio04b]

$$\begin{aligned} Y(z) = {} & z^{-L} X(z) + \varepsilon_1 z^{-(L-L_1)}\left(1-z^{-1}\right)^{L_1} E_1(z) + \\ & + d_1\varepsilon_2 z^{-(L-L_1-L_2)}(1-z^{-1})^{(L_1+L)} E_2(z) + ... \\ & + d_{2N-3}(1+\varepsilon_N)(1-z^{-1})^L E_N(z) \end{aligned} \qquad 3.4.17$$

Therefore, the output-referred in-band error power can be calculated as the following expression:

$$\begin{aligned} P_Q \approx {} & \frac{\Delta_1^2}{12}\left(\frac{\varepsilon_1^{\,2}\pi^{2L_1}}{(2L_1+1)OSR^{(2L_1+1)}}\right) \\ & + \frac{\Delta_2^2}{12} d_1^2\left(\frac{\varepsilon_2^{\,2}\pi^{2(L_1+L_2)}}{(2(L_1+L_2)+1)OSR^{(2(L_1+L_2)+1)}}\right) + ... + \\ & + \frac{\Delta_2^2}{12} d_{2N-3}^2\left(\frac{\varepsilon_N^{\,2}\pi^{2L}}{(2L_1+1)OSR^{(2L_1+1)}}\right) + ... + \end{aligned} \qquad 3.4.18$$

where Δ_i stands for the level spacing between adjacent levels in the quantizer of the ith stage, L_i indicates the loop-order of the ith stage, and $d_1 \ldots d_{2N-3}$ are the digital coefficients in the direct path from the output of the stages.

3.4.2.4 Comparison

In order to intuitively compare the impact on Sigma-Delta modulators, the model of the integrator weight variation is incorporated in the cascade 2-1-1-1 (4bit) [Rio00a] and the single-loop 5th-order 4bit [Bal04] Sigma-Delta modulator as before. Fig.3.13 illustrates the PSD curves of cascade 2-1-1-1 (4bit) Sigma-Delta modulator at OSR of 8 for different σc of capacitor mismatches. Fig.3.14 illustrates the corresponding PSD of the 5th-order 4-bit single-loop one at OSR of 8. Note that the achievable SNR is considerablely lower than that of the cascade. Comparing Fig. 3.13 and Fig. 3.14, it is found that the system noise floor increases due to capacitor mismatch, which will attenuate the SNR. Increasing modulator order of cascade topologies must add more error power into the modulator output, and therefore, it is impossible to expand the cascade topologies to any order, while preserving a low systematic loss of resolution (only one bit) and a high overload level.

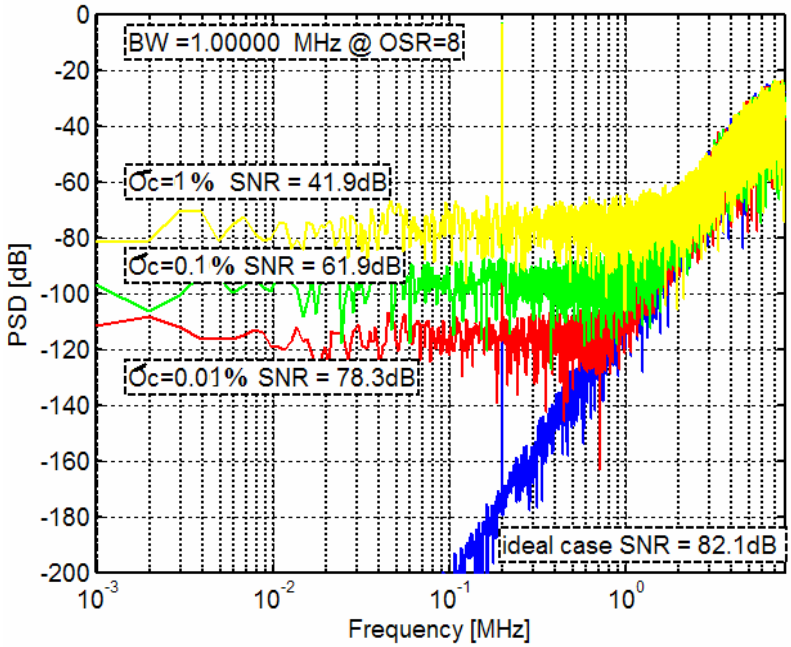


Fig. 3.13 PSD of the cascade 2-1-1-1 (4bit) at OSR of 8 for different capacitor mismatches.

In the simulation examples, for a 0.5-bit loss in DR, σ_c should be smaller than 0.01% at OSR of 8 for cascade one as shown in Fig. 3.13. However, the single-loop structure is very immune to the integrator leakage, and σ_c as large as 1% at OSR of 8 can be tolerated.

Note that the achievable ideal SNR of the single-loop is significantly lower than that of the cascade at the same OSR of 8.

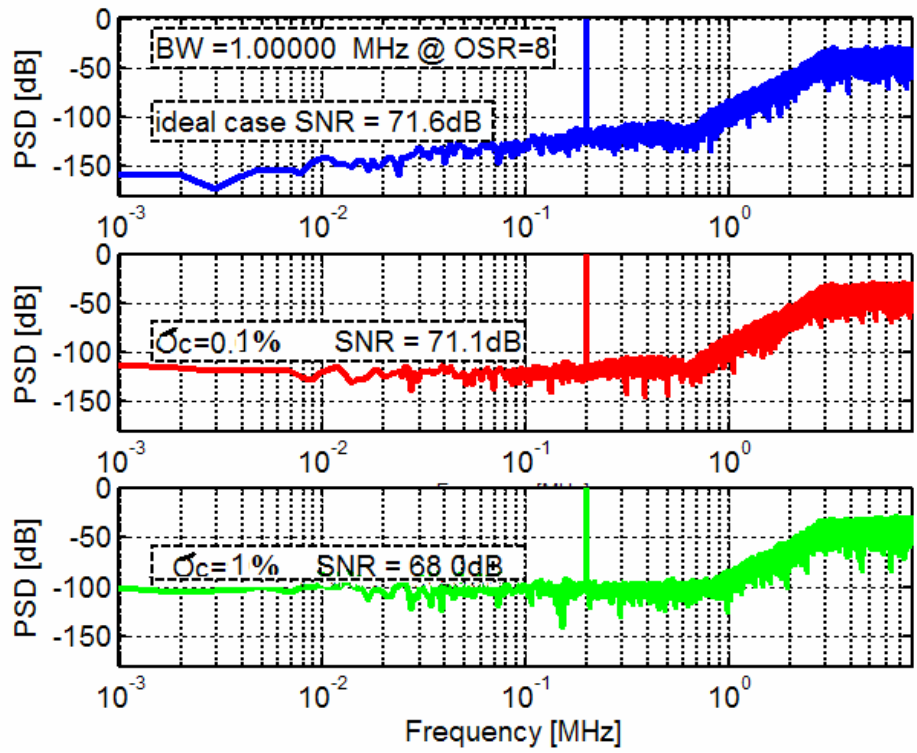


Fig. 3.14 PSD of the single-loop (4bit) at OSR of 8 for different σc of capacitor mismatches.

3.4.3 Integrator settling error

As the clock frequency increases in Sigma-Delta modulators to process wideband signals, integrator defective settling becomes one of the bottlenecks in present SC designs. The output voltage settling error is basically caused by the finite gain-bandwidth product and slew-rate of the amplifiers.

3.4.3.1 Model of finite bandwidth and slew rate

In order to analyze the integration settling behavior, the integrator model as shown in Fig. 3.15 is used. In this model, a single-pole amplifier is modeled by a transconductance *gm*,

which has a non-linear characteristic, with biasing current I_{BIAS}, and C_{GS} and C_L stand for parasitic capacitors associated with the summation node of the integrator input and the capacitive load, which includes the parasitic at the amplifier output node and the one associated to the bottom plate of the integration capacitor C_I, respectively; C_S and C_I stand for the sampling capacitance and the integration capacitance, respectively. In this case, the equivalent closed-loop capacitance at the integrator output depends on the equivalent open-loop capacitance ($C_{cl,ol}$) and the dc feedback factor (*f*) during the integration phase, and it is given by [Gee99]:

$$C_{eq,cl} = \frac{C_{eq,ol}}{f} = C_S + C_{GS} + \frac{(C_S + C_{GS} + C_I)C_L}{C_I} \qquad 3.4.19$$

Therefore, the close-loop time constant τ, GBW and SR are obtained, respectively:

$$\tau = \frac{C_{eq,cl}}{g_m} \qquad 3.4.20$$

$$GBW = \frac{g_m}{2\pi C_{eq,cl}} = \frac{1}{2\pi\tau} \qquad 3.4.21$$

$$SR = \frac{I_{BIAS}}{C_{eq,cl}} \qquad 3.4.22$$

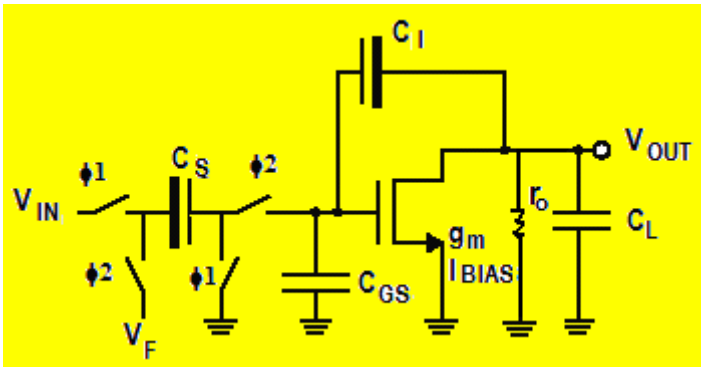


Fig. 3.15 Simplified CMOS integrator schematic

Furthermore, a more useful relationship between the slew rate and the time constant has been derived by using the simple square-law model of the MOS transistors [Gra01]:

$$SR * \tau = \frac{I_{BIAS}}{g_m} = \frac{V_{GS} - V_{th}}{2} = \frac{V_{eff}}{2} \qquad 3.4.23$$

where V_{GS} is the quiescent gate-to-source voltage of the input transistor, V_{th} is its threshold voltage, and V_{eff} is the overdrive voltage. Reforming Eq. 3.4.23 by introducing gain-bandwidth product GBW, a more design-oriented constant is obtained:

$$\frac{SR}{GBW} = \pi V_{eff} \qquad 3.4.24$$

It indicates that both design parameters SR and GBW are directly proportional to I_{BIAS}, and therefore, the ratio is quite constant in a single-pole opamp, which depends directly on the overdrive voltage.

Since slew rate appearing or not depends on the instantaneous amplitude of the input signal, the relationship between slew rate and the level of the input signal will be studied as follows.

In a SC integrator, the input signal consists of the assumed sinusoidal input signal minus the feedback signal. During the *nth* integration interval, the input signal v_s is equal to $V_{in}(nT_s\text{-}T_s/2)\text{-}V_F(nT_s\text{-}T_s/2)$, and the output node is evolved as: [Med94] [Rio00b]

$$\begin{aligned} v_{out}(t) &= v_{out}\left(nT_S - \frac{T_S}{2}\right) + \frac{C_S}{C_I}\left(v_{in}\left(nT_S - T_S\right) - v_F\left(nT_S - \frac{T_S}{2}\right)\right)\left(1 - \exp\left(-\frac{t}{\tau}\right)\right) \\ &= v_{out}\left(nT_S - \frac{T_S}{2}\right) + \frac{C_S}{C_I} v_s\left(1 - \exp\left(-\frac{t}{\tau}\right)\right) \end{aligned} \qquad 3.4.25$$

where $v_{out}(nT_s\text{-}T_s/2)$ is the integrator output value at the end of the preceding sampling phase, and Cs/C_I stands for the feed forward gain of the integrator. The maximum slope value of this curve is:

$$\left.\frac{d}{dt} v_o(t)\right|_{t=0} = \frac{C_S}{C_I}\frac{v_s}{\tau} \qquad 3.4.26$$

Regarding to the settling error, two separated cases have been considered: linear, partial-slew [Rio00a]:

In the case of

$$SR \geq \left|\frac{C_S}{C_I}\frac{v_s}{\tau}\right| \qquad 3.4.27$$

there is no slew-rate limitation, and the integrator output will be linearly settled. Imposing Eq. 3.4.23 in Eq. 3.4.27 and reforming, the linearly-settling condition is obtained:

$$V_{eff} \geq 2\frac{C_S}{C_I}|v_s| \qquad 3.4.28$$

The linear settling error can be approximated as:

$$\varepsilon_{st} \cong \exp\left(-\frac{T_S}{2\tau}\right) = \exp(-\pi GB_{norm}) \qquad 3.4.29$$

In the case of

$$SR < \left|\frac{C_S}{C_I}\frac{v_s}{\tau}\right| \qquad 3.4.30$$

and

$$t_0 = \frac{C_S}{C_I}\frac{|v_s|}{SR} - \tau < \frac{1}{2f_s} \qquad 3.4.31$$

the opamp is first in slewing within t_0, and therefore, the integrator output shows a partially SR limited *nonlinear settling*. Similarly, imposing Eq. 3.4.23 in Eq. 3.4.30 and Eq. 3.4.31, the partially SR limited nonlinear settling condition with $GB_{norm}=GBW/f_s$ is:

$$2\frac{C_S}{C_I}\frac{|v_s|}{1+\pi GB_{norm}} < V_{eff} < 2\frac{C_S}{C_I}|v_S| \qquad 3.4.32$$

The linear settling error can be approximated as:

$$\varepsilon_{st} \cong \exp\left(-\frac{T_S}{2\tau}\right) = \exp(-\pi GB_{norm}) \qquad 3.4.33$$

whereas the nonlinear settling error can be approximately evaluated as:

$$\begin{aligned}\varepsilon_{st} &\cong \frac{SR*\tau}{\frac{C_S}{C_I}v_S} * \exp\left(-T_S/2\tau - 1 + \frac{C_S}{C_I}\frac{|v_s|}{SR\tau}\right)\\ &\cong \frac{V_{eff}}{2\frac{C_S}{C_I}v_s} * \exp\left(-\frac{\pi GBW}{f_S} - 1 + 2\frac{C_S}{C_I}\frac{|v_s|}{V_{eff}}\right)\\ &= \frac{V_{eff}}{2v_{norm}} * \exp\left(-\pi GB_{norm} - 1 + 2\frac{|v_{notm}|}{V_{eff}}\right)\end{aligned} \qquad 3.4.34$$

Fig. 3.16 illustrates the corresponding relationship between the normalized GB and the integrator's relative input level. The output responses of the integrators are assumed to be

settled to a given error of 0.05%, 0.1% and 0.5%, respectively, and V_{eff}=200mV. It is shown that the low input level of the integrator is the key to reduce the required normalized gain-bandwidth GB. Note that most of the existing Sigma-Delta modulators have a great occurrence that the input levels of the integrators are relatively large. Therefore, they operate mostly in the non-linear settling region.

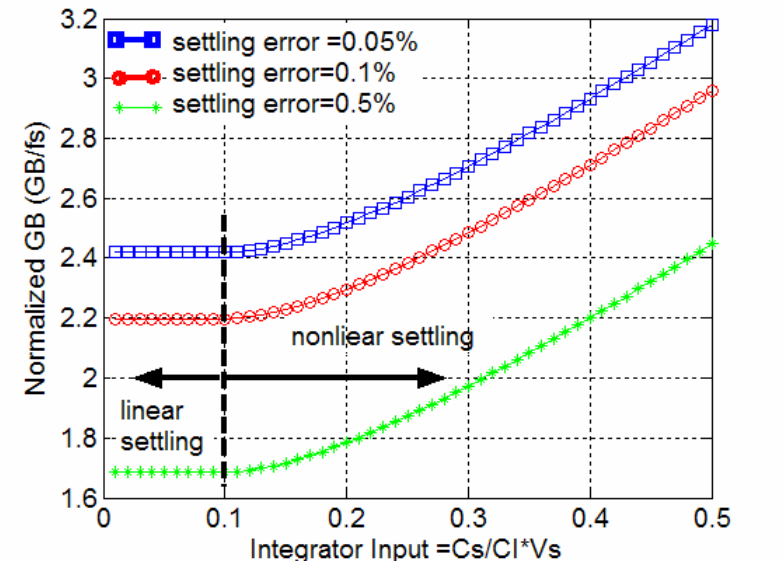


Fig. 3.16 The relationship between the required normalized GB and the relative integrator input level for a given settling error

Consequently, a relatively large opamp gain-bandwidth is required, and harmonics are produced. Additionally, the opamp-normalized gain-bandwidth GB can also be reduced with a certain topology, which is insensitive to the settling error.

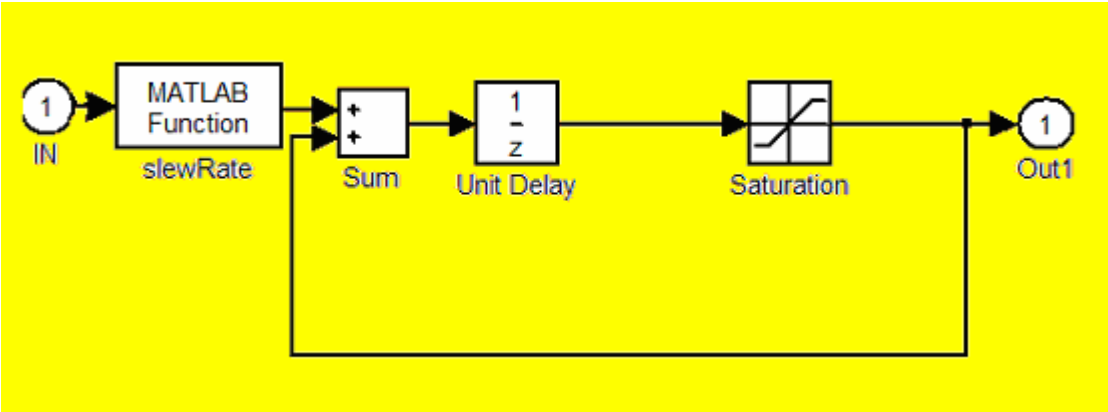


Fig. 3.17 Real integrator with SR model

The integrator output value $v_{out}(nTs)$ can be described in the MATLAB function block as shown in Fig. 3.17. In the case of the linear settling, the incomplete settling causes a degradation of the integrator gain; in the case of the nonlinear settling, the incomplete settling causes a nonlinear gain, since the gain of the integrator is dependent on the input [Med94]. The effect of the integrator response due to settling error on the 2-1-1-1 cascade modulator is illustrated in Fig. 3.18 through behavioral simulation. The most common dynamic of an integrator is slew-rate limited during integration over the clock cycles. The integrator response is not linear and distortion appears at the modulator output spectrum.

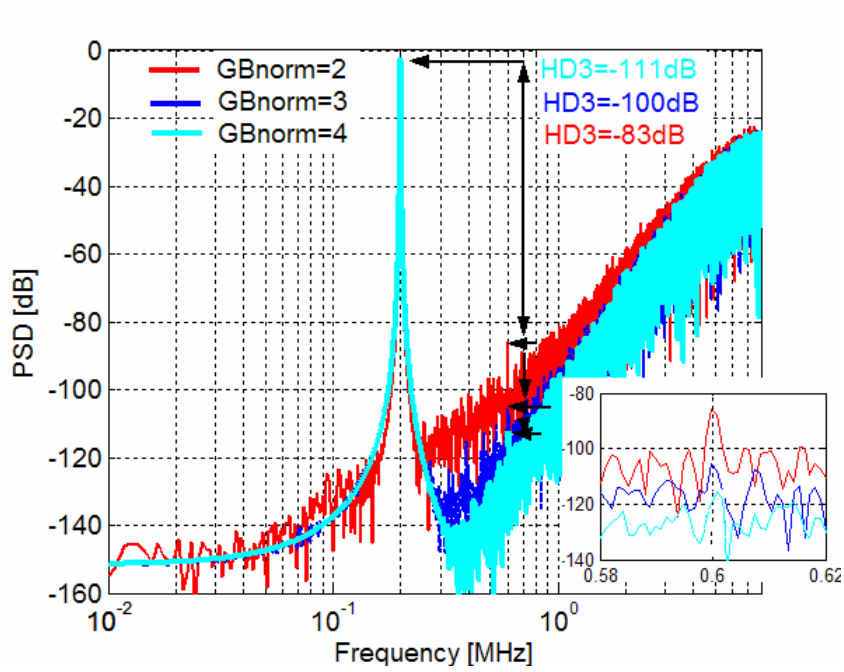


Fig. 3.18 PSD of a 2-1-1-1 modulator considering the settling error due to finite GBW and SR of the integrators (SR=πVeff GBW and V_{eff}= 0.2V)

Note from Fig.3.18 that a 3rd-order harmonic component arises in all the spectra, due to the non-linearity of the settling and the fully-differential implementation of the modulator. The corresponding values for the harmonic distortion are *HD*3 =-83, -100, -111dB, which correspond to GB^{norm} *=2, 3, 4* in the integrators, respectively. Besides this, the 3rd-order harmonic component rapidly decreases when *GBW* increases, showing that full performance can be achieved although the dominant integrator dynamic is partially slew-rate limited.

3.4.3.3 Impact on Sigma-Delta modulators

The required normalized gain-bandwidth GB can be reduced, if input levels of the integrators are low. Fig. 3.17 and Fig. 3.18 show the historgram of the corresponding integrator inputs of the cascade 2-1-1-1 [Rio00a] and the 5th-order single-loop architecture [Bal04], relative to the FS voltage, respectively.

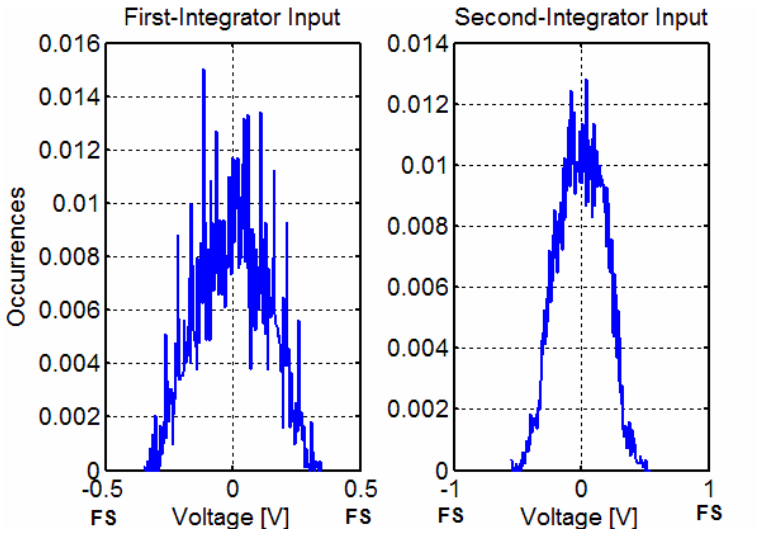


Fig. 3.19 Historgram of the first and second integrator inputs of the cascade 2-1-1-1 relative to the FS voltage

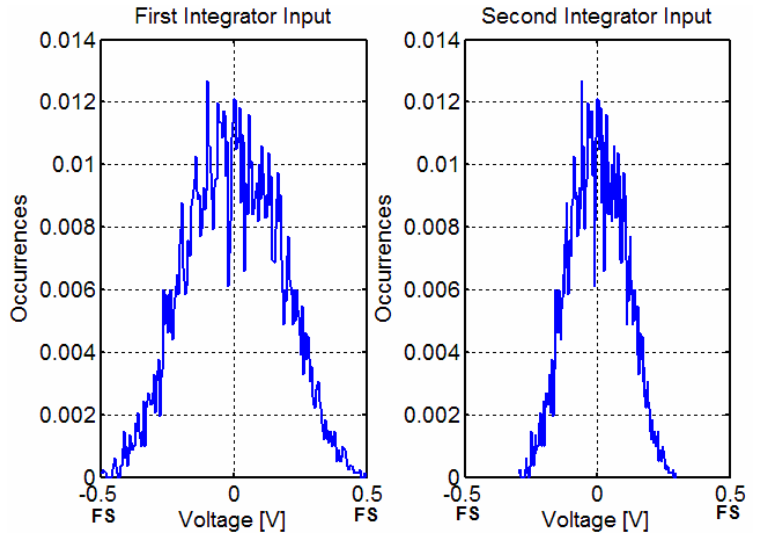
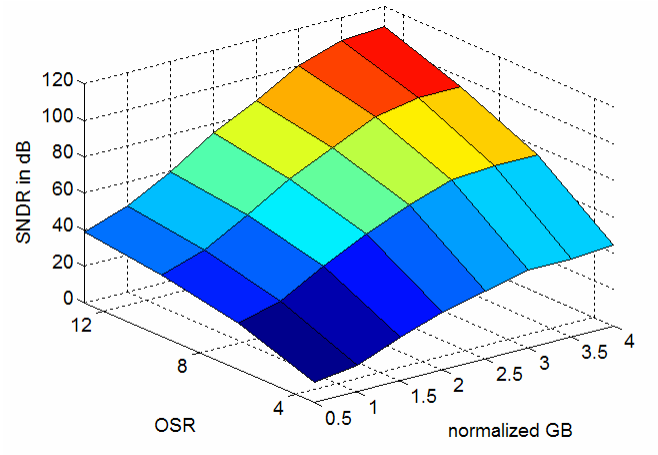
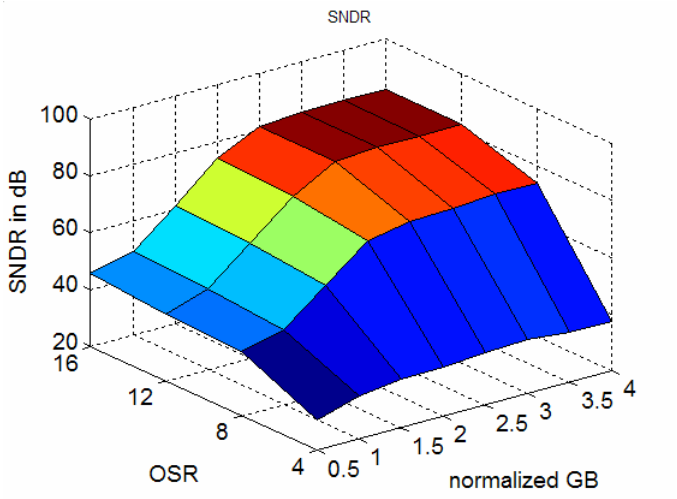


Fig. 3.20 Historgram of respective integrator inputs of the 5th-order single-loop architecture [Bal04] relative to the FS voltage

Obviously, both Sigma-Delta modulators have a great occurrence operating mostly in the non-linear settling region. Fig. 3.21 presents the achieble SNDR vs. the normalized GB and OSR of the 2-1-1-1(4b) cascade [Rio00a] and the 5th-order single-loop [Bal04] Sigma-Delta modulators. In order to avoid the performance degradation due to settling error, the GBW of opamps should be 3 f_S *and* 4 f_S for the 5th-order single-loop and the 2-1-1-1(4b) cascade, respectively.



(a)



(b)

Fig. 3.21 SNDR vs normalized GB and OSR of (a) the 2-1-1-1(4b) cascade [Rio00a], and (b) the 5th-order single-loop Sigma-Delta modulator.

Note that the results of behavioral simulations are obtained by assuming that the slew rate of opamps always follows the relationship of Eq. 3.4.24, where V_{eff}=200 mV. The linear

settling error can be interpreted as a gain error. Therefore, the impact of this error on the Sigma-Delta modulators is similar to that mentioned in Sections 3.4.1 that the cascade topologies are more sensitive to settling errors than single-loop Sigma-Delta modulators. It is also shown that

- if the integrator dynamic along the clock cycles involves full-slew during integration, the performance of the modulator will be completely degraded.
- if the integrator dynamic is in partial-slew, as long as the slew-rate is large enough to offer sufficient time to the linear transient to settle within the desired accuracy, the performance of the modulator will not be degraded.

3.4.4 Non-linearity of amplifier gain

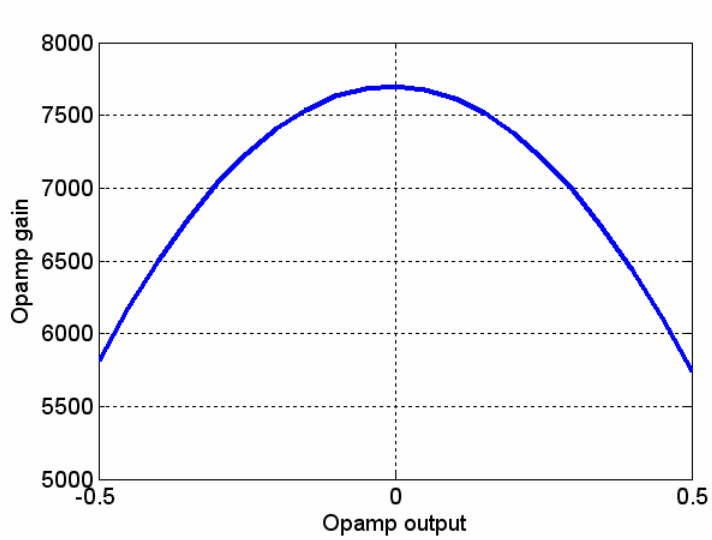


Fig. 3.22 the extracted open-loop gain curve of the gain-boosted amplifier with the maximum value of 7700 in the center of the scale (α= 0.01, and b= 0.5)

Operational amplifiers are utilized to implement SC integrators. In reality, the gain of opamps is not only finite but also nonlinear. The gain nonlinearity depends on the output voltage and can be fitted with a second-order polynomial equation:

$$A(v_0) = A\left(1 + \alpha v_0 + b v_0^{\,2}\right) \qquad 3.4.35$$

where α and b are the linear and quadratic voltage coefficient of the gain. Fig. 3.22 shows the curve of the extracted open-loop gain of the gain-boosted amplifier. The gain presents a

maximum value in the center of the scale and decreases as the output voltage approaches to the end of the saturation region, where its maximal gain is 7700, first-order nonlinearity is 0.01, and second-order nonlinearity is 0.5.

The Fig. 3.23 shows the impact of the non-linear opamps on the second order Sigma-Delta modulator at OSR of 64. The harmonics appear at the output, and have been obviously attenuated at such a high OSR. However, if OSR is low in wideband applications, the contribution of the non-linear opamps to harmonics is sufficiently high.

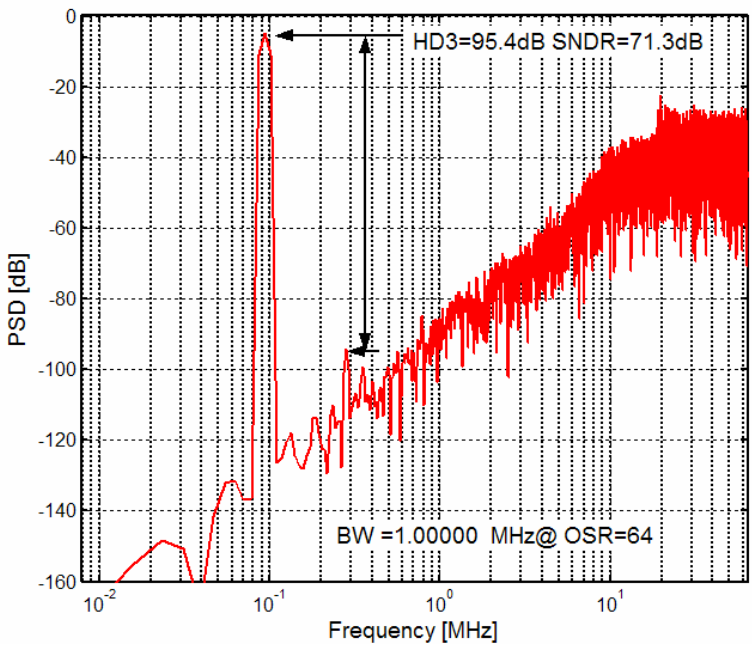


Fig. 3.23 Harmonics due to the non-linear opamps gain of the traditional second order Sigma-Delta modulator at OSR of 64

3.5. Comparator related non-idealities

Ideally, a comparator can be described by:

$$V_{in} < V_{ref} \qquad V_{out} = V_{out-} \tag{3.5.1}$$

$$V_{in} \geq V_{ref} \qquad V_{out} = V_{out+} \tag{3.5.2}$$

Where V_{in} and V_{out} are the input and output voltages of the comparator, V_{ref} is the reference voltage for the comparison and V_{out+} and V_{out-} are the positive and negative values of the output respectively (mostly the digital supply voltages).

Two of the most important specifications for a comparator used in a Sigma-Delta modulator are offset and hysteresis as illustrated in Fig. 3.24. These are discussed next.

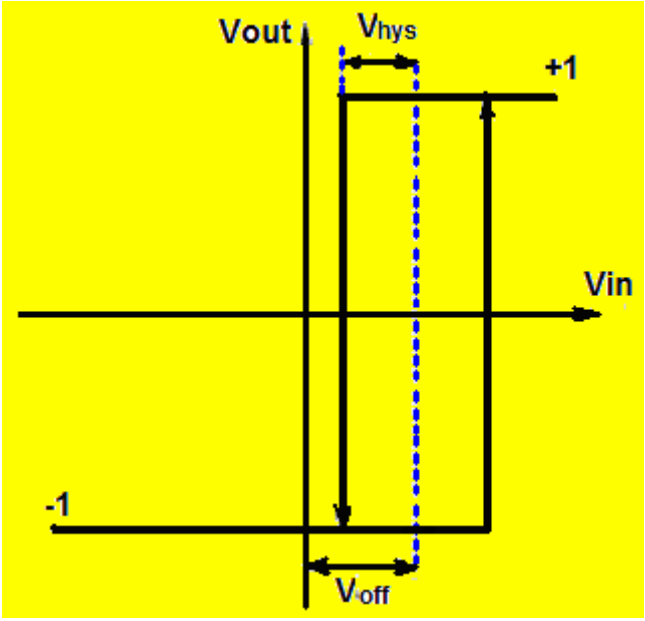


Fig. 3.24 Transfer curve of a comparator with offset and hysteresis

3.5.1. Comparator offset

Since the description of an ideal comparator at a high level is just a comparison between two values, one can easily add the comparator offset to the reference value. This simple alteration suffices to use it at a behavioral level. Equations 3.5.1 and 3.5.2 now become:

$$V_{in} < V_{ref} + V_{off} \qquad V_{out} = V_{out-} \qquad 3.5.3$$

$$V_{in} \geq V_{ref} + V_{off} \qquad V_{out} = V_{out+} \qquad 3.5.4$$

3.5.2. Comparator hysteresis

Instead of comparing the input with one reference voltage one can use two reference

voltages (plus or minus the hysteresis value) depending on the previous output value. This requires a memory function. Again, this is trivial at a behavioral level. Equations (3.5.1) and (3.5.2) now depend on the previous output value (Vout_prev):

CASE 1: $V_{out\_prev}=V_{out-}$

$$V_{in} < V_{ref} + V_{hys} \qquad V_{out} = V_{out-} \qquad 3.5.5$$

$$V_{in} \geq V_{ref} + V_{hys} \qquad V_{out} = V_{out+} \qquad 3.5.6$$

CASE 2: $V_{out\_prev}=V_{out+}$

$$V_{in} < V_{ref} - V_{hys} \qquad V_{out} = V_{out-} \qquad 3.5.7$$

$$V_{in} \geq V_{ref} - V_{hys} \qquad V_{out} = V_{out+} \qquad 3.5.8$$

3.5.3. Comparator offset and hysteresis combined

Finally, combining offset and hysteresis yields the following equations:

$$V_{in} \leq V_{ref} + V_{off} - \mathrm{sgn}(V_{out-prev}) * V_{hys} \qquad V_{out} = V_{out-} \qquad 3.5.9$$

$$V_{in} > V_{ref} + V_{off} - \mathrm{sgn}(V_{out-prev}) * V_{hys} \qquad V_{out} = V_{out+} \qquad 3.5.10$$

Because offsets and hysteresises in the comparator are suppressed by the large low-frequency gain of the integrators, Sigma-delta A/D converters are insensitive to them [Bos88]. Therefore, the simulation of their effect on the Sigma-Delta modulator is neglected. In practice, excessive offsets and hysteresises should be avoided because of the consequent reduction in the effective signal range in the integrators.

3.6. DAC nonlinearity

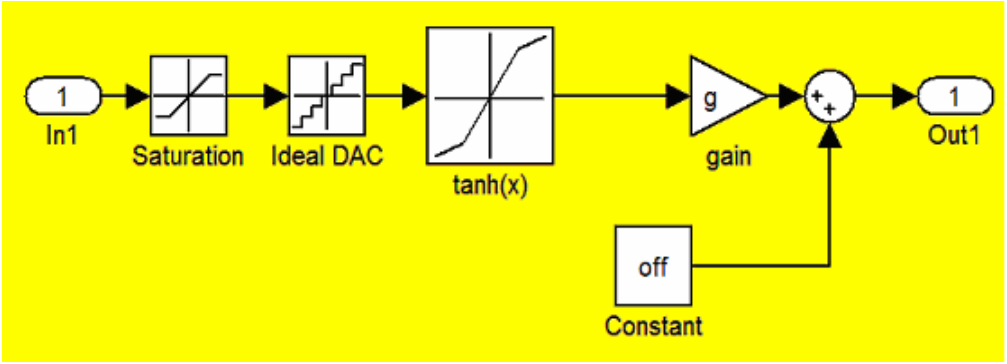


Fig. 3.25. The DAC nonlinearity model in Simulink

Multi-bit Sigma-Delta converters increase the SQNR, which is independent of the OSR. Other advantages of multibit quantization include enhanced modulator stability as well as relaxed slew-rate and settling requirements on the opamps of the loop-filter integrators. The main problem of multi-bit quantization is the linearity of the digital-to-analog converter (DAC) in the feedback path.

The DAC nonlinearity can be modeled in Simulink as illustrated in Fig. 3.25. [Cas03], where an offset *off*, a gain γ, and an integral non-linearity INL are incorporated together with an ideal D/A converter.

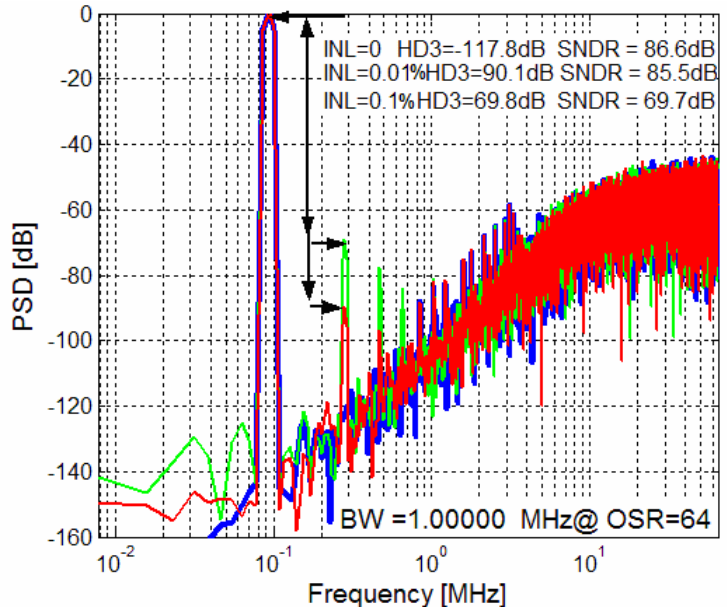


Fig. 3.26 PSD of the second order modulator considering the non-linearity of 4-bit DAC

Since this nonlinearity appears directly at the input of the modulator and, therefore, limits its overall linearity. Fig. 3.26 shows the simulated spectrum of the traditional 4-bit second-order Sigma-Delta modulator at OSR of 64, considering the non-linearity with INL of 0, 0.01% and 0.1%, respectively. The corresponding SNDR is degraded by the non-linearity of the DAC; particularly, the harmonics appear considerately high at the output, if the non-linearity of the DAC is high. If the OSR is decreased for wideband applications, the requirement on the linear DAC is further increased; consequently, designing a sufficiently

high linear DAC can be impossible and some auxiliary linearity techniques, such as laser trimming, digital correction, dynamic element matching, etc., have to be utilized to relieve the problem.

In a cascade Sigma-Delta modulator, if multi-bit quantization is exclusively used in the last stage, the linearity requirements for the multi-bit DAC are relaxed, since DAC error is filtered by high-pass filter and most of its power falls out of the band. The output of an *Lth*-order *N*-stage cascade Sigma-Delta modulator with a multi-bit quantization only in the last stage can be obtained through linear analysis in z-domain, [Med98a]

$$Y(z) = z^{-1}X(z) + d_{2N-3}\left(1-z^{-1}\right)^{L} E_N(z) + d_{2N-3}\left(1-z^{-1}\right)^{L-L_N} E_D(z) \qquad 3.6.1$$

where E_D is the z-transform of the non-linearity error in the last-stage DAC. Such an error presents a shaping of (L-L_N)th-order; i.e., the order of the overall modulator minus that of the last stage. This means that the influence of the DAC non-linearity is attenuated inside the band, and hence some non-linearity can be tolerated without correction/calibration. From Eq. 3.6.1, the in-band error power for each of the cascades considered can be expressed as follows [Rio04b],

$$\begin{aligned}
P_Q\big|_{2-2mb} &\approx d_1^2\left(\sigma_Q^2\frac{\pi^8}{9OSR^9} + \sigma_D^2\frac{\pi^4}{5OSR^5}\right)\\
P_Q\big|_{2-1-1mb} &\approx d_3^2\left(\sigma_Q^2\frac{\pi^8}{9OSR^9} + \sigma_D^2\frac{\pi^6}{7OSR^7}\right)\\
P_Q\big|_{2-1-1-1mb} &\approx d_5^2\left(\sigma_Q^2\frac{\pi^{10}}{11OSR^{11}} + \sigma_D^2\frac{\pi^8}{9OSR^9}\right)\\
P_Q\big|_{2-2-2mb} &\approx d_3^2\left(\sigma_Q^2\frac{\pi^{12}}{13OSR^{13}} + \sigma_D^2\frac{\pi^8}{9OSR^9}\right)
\end{aligned} \qquad 3.6.2$$

where $\sigma_Q^2 = [FS/(2^B-1)]^2/12$ is the power of the last-stage quantization error (FS stands for the quantizer full scale and B for its resolution) and $\sigma_D^2 = [FS*INL/100]^2/2$ represents the DAC-induced error power [Med99a], with INL being the DAC integral non-linearity expressed in percentage of the full scale (%FS). Note that this error power is shaped by 2^{nd}-order high-pass filter (OSR^{-5}) in the 2-2 modulator, whereas it is 3^{rd}-order shaped (OSR^{-7}) in the 2-1-1 modulator, 4^{th}-order it is attenuated by OSR^{-9} in the 2-1-1-1 and the 2-2-2 cascades. The larger immunity of the latter modulators to DAC imperfections makes it possible, to implement a calibration-free multi-bit Sigma-Delta modulator.

3.7 Summary

In this chapter the main error mechanisms caused by different non-idealities of the analog building blocks have been reviewed and discussed, and behavioral models and the degradation of the performance of Sigma-Delta modulators have been presented.

The models and guidelines derived in this chapter will be extensively used during the design phases of the two high-speed Sigma-Delta modulators presented in the following chapters.

Chapter 4 A 2-1-1-1(4b) Cascaded Wideband ∑Δ Modulator in 3.3-V 0.4-μm BICMOS

4.1 Introduction

The very high bit-rate digital subscriber line (VDSL) as a telecommunication standard has been developed to support exceptionally high-bandwidth applications, such as high-definition television (HDTV). The speed and channel adaptability of such an application require that AD Converters are capable of achieving a resolution of 12-14 bit and a conversion rates of more than 20 MS/s.

This chapter will demonstrate the implementation of a 13 bit Sigma-Delta modulator at a sampling rate of 200 MHz with OSR of 10 in a 0.4μm four-metal SiGe-BiCMOS process. Firstly, the selected architecture is described. After that, the chapter will focus on study the requirements and the implementation of the main analog building blocks in the BiCMOS process. Finally the experimental results will be reported.

4.2. Design Methodology

The top-down methodology [Med99b] is used for designing the targeted Sigma-Delta modulator. In this methodology, the specification of the AD converter is predefined, and then designed the ADC step by step in more detail according the design flow, which involving three linked design steps:

- Modulator architecture level
- Analog building block level
- Transistor level

At each level, detailed specifications were refined and translated into design parameters using either equations, behavioral, or electrical models for the evaluation purposes and statistical optimization routines for providing a 'good-enough' solutions. Therefore, the

design parameters were obtained for the each level and served specification on the next level down in the hierarchy.

4.3. Topology selection

In Sigma-Delta A/D converters, the resolution is predominately governed by three factors: the oversampling ratio (OSR), the order of the noise shaping (L) and the internal quantizer resolution (B). The sampling frequency of the Sigma-Delta modulator is ultimately limited by the speed capability of the intended technology. A great deal of effort has been put into using either high-order loop filtering (increasing the order L) or multibit quantization (increasing the resolution of the quantizer B), or both in recent years, to design Sigma-Delta modulators for high-frequency applications with a medium or high resolution — typically 12 bits or more needed for telecom.

As mentioned in Chapter 2, higher-order Sigma-Delta modulators are not always stable. A single-loop structure of an order higher than two can get stable by using a complex loop filter with feedforward and feedback of the internal signals to reduce the out-of-band gain [Sch93] [Ada97a], or by properly choosing the integrator scaling factors for the switched-input and switched-feedback signals [OptE90] [Mar98b]. These feedforward and feedback coefficients are very small. Therefore large capacitors have to be used, which lead to more area, power consumption, and introduce heavy loads to the opamps in the converter, and thus slow down the operational speed. Moreover, as shown in Section 2.3.3, stable high-order single-loop Sigma-Delta modulators suffer from a considerable reduction of the achievable DR in comparison with the corresponding theoretical one with the noise-shaping of a power of $(1 - z^{-1})$. Whereas the cascaded multi-stage Sigma-Delta converters based on the easily implemented stable first- or second-order Sigma-Delta modulators give the possibility to realize an almost-theoretical higher order noise shaping [Med99a][Rio04b]. In a cascaded Sigma-Delta modulator, there is no accumulation of signals at the later stages. The succession of stages tends to randomize and decorrelate the quantization error(s), such that the later stages are more closely approximated by the white noise assumption. The strongly correlated quantization error from the first stage and the error(s) from the later stage(s), except for the last one, are canceled by the digital

cancellation logic. The transfer function of the converter can be simply expressed as the input signal plus the shaped quantization error from the last stage [Sch97]. Behavioral simulations reveal that there is no input signal component above the noise floor in the quantization error(s) of the later stages. The disadvantage of the cascaded modulator structure is that it requires a higher opamp gain and a better capacitor matching in order to ensure proper noise cancellation.

Silicon germanium-based (SiGe) BiCMOS processes have recently become a viable technology for the production of competitively-priced, superior-performance circuits. The high transconductance of a bipolar device for a given current and area is higher than MOS transistors. Therefore, it can be used to expand the open-loop gain and the unity-gain bandwidth of opamps. Superior matching properties of devices (bipolar transistors and capacitors) make the mismatch limitation also partially solvable by using the SiGe-BiCMOS. In this scenario, a cascaded high-order Sigma-delta modulator was primarily designed in the SiGe-BiCMOS, to obtain the desired high-resolution and high-speed.

The use of the cascade high-order modulation may not be enough to obtain a given dynamic range. A direct solution to this problem is to increase the internal quantizer resolution. However, the linearity of the multi-bit DAC in the feedback path of multi-bit compromises that of the overall converter. Correction, calibration, or dynamic element matching techniques can be included in multi-bit Sigma-Delta modulators, either in the digital or in the analog domain, to attenuate its impact, but often at the cost of higher circuit complexity and larger occupation area. This issue can be overcome with a multibit quantizer only at the last stage of the cascade, as mentioned in section 3.6, keeping the others single-bit [Bra91] [Tan93], where the D/A converter nonlinearity error of this last stage is attenuated by a shaping function, provided by the cancellation logic, and filtered out by the digital decimator.

The 5^{th}-order 4-stage 2-1-1-1 cascade [Rio00a] and the 6^{th}-order 3-stage 2-2-2 cascade [Fel98] Sigma-Deltạmodulators are considered as possible candidates. As shown in Section 3.6, the error power of DAC integral non-linearity is attenuated by OSR^{-9} in both aforementioned structures. However, the scalar factor d_{2N-3} in Eq. 3.6.2 required for the

signal scaling to avoid signal premature overload equals the inverse of the product of the inter-stage coupling factors. In general, this results in a value larger than unity, which means an amplification of the last-stage quantization error, and thus generates a systematic loss of resolution in comparison with the theoretical case. With proper selection of the inter-stage couplings, the scaling factor can be reduced to only 2 for the cascade structure shown in [Rio00a], whereas the scalar d equals to 8 for the 2-2-2 cascade modulator [Fel98]. The former implies a 1-bit reduction in DR, whereas the latter leads to an 18-dB (3-bit) reduction.

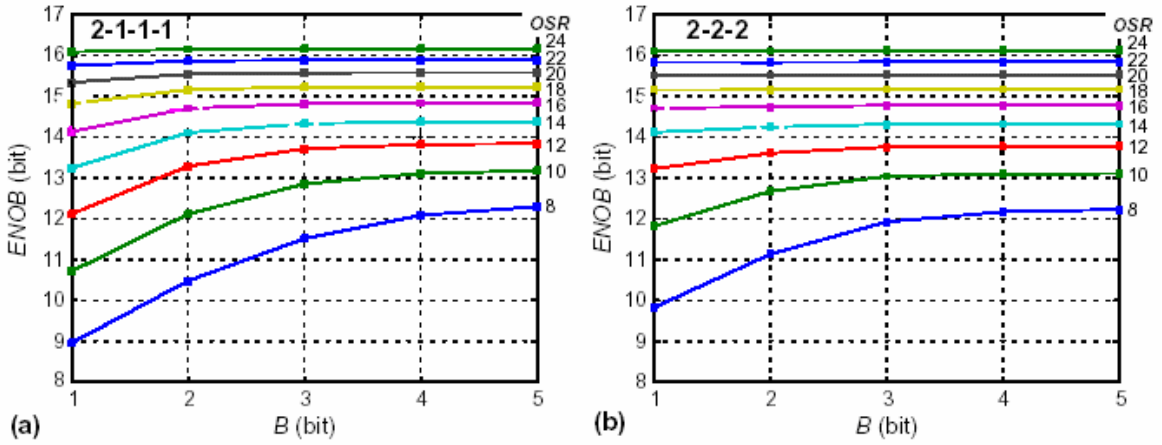


Fig. 4.1 Cascade Sigma-Delta modulators versus the resolution in the last-stage quantizer, (a) 2-1-1-1 Sigma-Delta modulator, (b) 2-2-2 Sigma-Delta modulator, ADC =4000, (C =0.12%, and DAC INL= 0.4%FS)

The other issue of cascade modulators is the sensitivity to noise leakage, which can degrade the benefits of high-order filtering and multi-bit quantization. As shown in Chapter 3, finite amplifier DC-gain and capacitor mismatch mainly contribute to the noise leakage. Hence, the feasibility of the cascades depends on how demanding the requirements for the DC-gain and capacitor matching are. Fig.4.1 shows the effective resolution achieved by the cascade 2-1-1-1[Rio00a] and 2-2-2 [Fel98] Sigma-Delta modulators as a function of the last-stage quantizer resolution and the oversampling ratio, where a reasonable DC-gain of 4000, capacitor mismatch of 0.12%, and a DAC of INL of 0.4% FS have been taken into account [Rio04b]. Note that curves in Fig. 4.1 saturate in the presence of non-idealities, leading to a practical useful limit for the loop order. In other words, the 2-2-2 Sigma-Delta modulator employs one more integrator than the 2-1-1-1, but the benefit from higher noise shaping is masked by its 3-bit systematic loss in dynamic

range and its larger sensitivity to mismatch. Therefore, the best choice was considered to be the 2-1-1-1 Sigma-Delta modulator. The fifth-order cascade 2-1-1-1 architecture working with 4-bit quantization in the last stage can achieve the targeted resolution (13 bits) with only an OSR of 10 and still provides some margin. If the system's sampling frequency is as high as 200 MHz, then, the maximal conversion rates of 20 MS/s can be achieved.

Fig.4.2 shows the block diagram of the selected 2-1-1-1 Sigma-Delta modulator. Table 4.1 shows the reported coefficients for the cascade Sigma-Delta modulator.

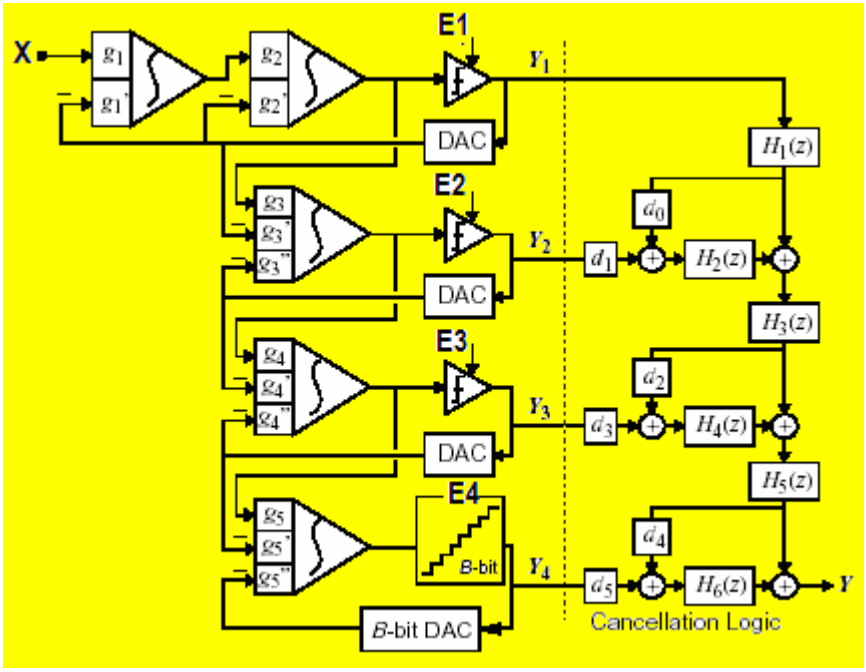


Fig. 4.2 5th-order cascade 2-1-1-1Sigma-Delta modulator

g1	g1'	g2	g2'	g3	g3'	g3"	g4	g4'	g4"	g5	g5'	g5"
0.25	0.25	1	0.5	1	0.5	0.5	1	0.5	0.5	1	0.5	0.5

Table 4.1 Coefficients for the 5th-order 2-1-1-1 cascade Sigma-Delta modulator

Therefore, the scale factor can be chosen:

$$d = \frac{g_5^{"}}{g_1 g_2 g_3 g_4 g_5} = 2 \qquad 4.3.1$$

It indicates a system loss of only 6dB.

4.4. Design technology

The stringent requirements on the analog building blocks represent a significant challenge for a Sigma-Delta ADC. Switched-capacitor circuits are very robust and tolerant to clock jitter compared to continuous time circuits, thus, the integrators are implemented with switched-capacitor circuits. For the opamp in a switched-capacitor (SC) integrator, the requirements for high speed are exactly opposite to those for high gain and low noise. It is difficult to simultaneously achieve high open-loop gain, high speed, and low noise in a CMOS process. The Sigma-Delta modulator described in this thesis has been implemented in the low-cost 0.4-um SiGe-BiCMOS technology. In this section, the main devices and corresponding features in the CDR1 SiGe-BiCMOS technology will be briefly introduced [CDR04].

4.4.1 GCMOS transistors

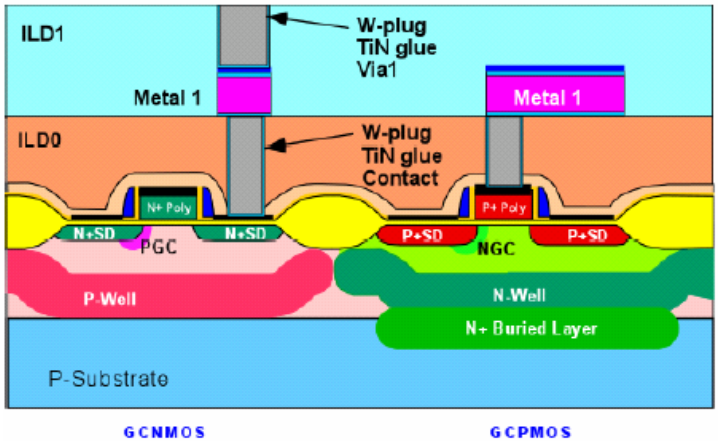


Fig. 4.3 Cross-sectional view of CMOS transistors in BiGCMOS process

The CMOS portion of the BiCMOS technology is based on a graded-channel process. In the GCMOS process flow three types of transistors can be obtained with a single masking step: unilateral, bilateral, and natural. Unilateral devices are graded laterally from the source end of the device. A cross-sectional view of MOS transistors in this technology is shown in Fig. 4.3. The oxide thickness is 50 Å and the CMOS gate is the second layer of polysilicon. CMOS wells are created by chain implants and graded channels are formed by

ion implantation. Each transistor can be isolated in its own well so that a high signal isolation better than -80 dB at 1-GHz can be achieved. The main benefits of the graded-channel process are avoiding short-channel effects and adjusting threshold voltages at the same time. Consequently, this type of device achieves the highest DC and RF performance, which is equivalent to the 0.25µm CMOS technology. Therefore, they can be used for this purpose only when drain-to-source voltage is low, i.e. the device is in the linear region of operation. Bilateral devices are graded from both source and drain regions. The bilateral device is required for switching applications where the source and drain terminals are used interchangeably. Natural devices are formed when no GC mask is applied. These transistors are near-depletion mode devices and are useful for their better matching and 1/f noise characteristics [Oli02].

4.4.2 Enhanced SiGe:C (eHBT) transistors

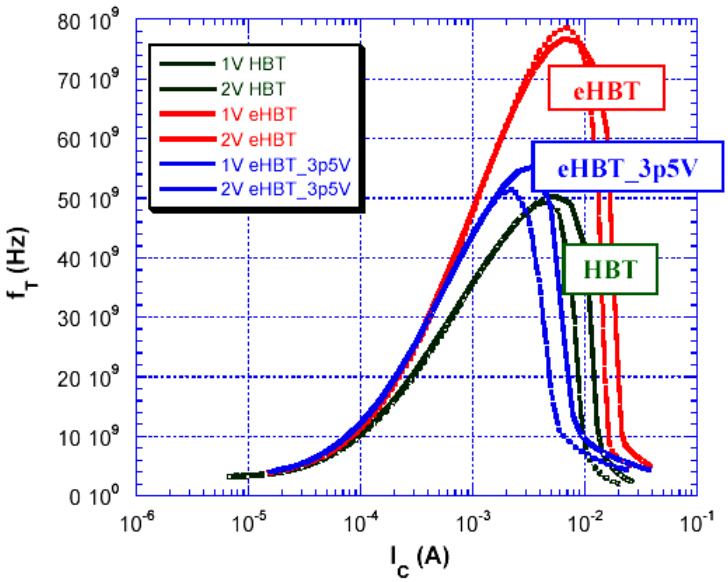


Figure 4.4 Typical f_T vs. I_C comparing the eHBT, eHBT_3p5V, and HBT devices for a 0.3x10µm^2 1 emitter HBT with temperature = 27°C

The enhanced SiGe:C HBT transistors are designed for higher f_T/f_{MAX} (80GHz/ 120GHz), lower noise figure, lower collector resistance and a 2.5V BVCEO. The minimum emitter window size for the eHBT device is scaled to 0.3x0.8µm^2, while the emitter poly enclosure of emitter window is reduced for improved base resistance (and noise figure). Additionally,

a higher breakdown-voltage enhanced HBT device (eHBT_3p5V) is also available. In the eHBT_3p5V device, peak f_T/f_{MAX} performance (56GHz/115GHz) is balanced with lower collector-base capacitance, high Early voltage, along with a low noise figure, low collector resistance, a 3.6V B_{VCEO} and 85V V_A. Layout rules for the eHBT_3p5V device are identical to the eHBT device: the minimum emitter window size is 0.3x0.8µm2, while the emitter poly enclosure of emitter window is also reduced from that of the HBT device. Figure 4.4 shows a comparison of fT for the eHBT, eHBT_3p5V and standard HBT devices for a 0.3x10μm^2 with a 1 emitter layout.

4.4.3 Passives

A complete suite of passive elements are offered in this technology. Brief descriptions are provided below.

4.4.3.1 Capacitors

A 4 fF/um^2 high-density Double-Poly Capacitor (DPC) is available with a Nitride-Oxide (NO) dielectric. The addition of one implant mask provides good-linearity for the high-precision analog applications. A 1.6 fF/um^2 low-parasitic, high-linearity Metal-Insulator-Metal (MIM) capacitor is available and formed by placing a thin nitride layer between the last two metal layers in the process. The MIM capacitor requires one additional lithography masking step.

4.4.3.2 Resistors

Several resistors are available in this technology with sheet resistances from 3.5 ohms/sq to 1.5k ohms/sq for the purpose of RF/IF mixed signal design. Diffused and polysilicon resistors are offered with both positive and negative temperature-coefficients depending on the resistor type. Additionally, the RPSD and RP2PSD resistors, and the PMOS devices have substantially improved matching and 1/f noise performances on the enhanced HBT process.

4.4.3.3 Inductors

Spiral inductors can be constructed using the existing AlCu metal system. These inductors will not have high Q due to the limitations imposed by the CMOS logic MLM module. An alternative thick (4um) AlCu metallization is available for such usage as inductors, transmission-lines and interconnect routing at the 4th metal layer in the CDR1-BiCMOS process. This alternative thick metallization is available in place of an optional thin-AlCu M4 layer. This thick-AlCu M4ALT and the thin-AlCu M4 cannot be used on the same design. In the M4ALT option, a standard, thin, 0.6um AlCu is replaced by a thicker 4um AlCu layer. The via and ILD processing below the thicker M4ALT do not change, but design rules require an increase in minimum M4ALT W, S, and enclosure of the via. However, other via rules remain the same as used for VIA1-VIA2. As a result, a separate VIA3ALT design layer is defined for the usage with the thick-AlCu M4ALT. The standard VIA3 design layer is reserved for the usage with the optional thin-AlCu M4.

4.5. Switched-Capacitor implementation

This section will describe the switched-capacitor implementation of the proposed four-stage fifth-order Sigma-Delta modulator by properly using the BiCMOS technology.

4.5.1. Fully differential implementation

A fully differential implementation is selected to implement the converter. It offers a net increase of 3 dB in the signal-to-noise ratio, compared with the single-ended implementation. Moreover, in this implementation, the noise immunity is higher and the charge/clock feedthrough cancels better. Finally, in a differential implementation, the operational transconductance amplifiers (OTA's) have better settling characteristics, since the differential to single-ended conversion is avoided.

The schematic of the fully differential SC 2-1-1-1 Sigma-Deltạmodulator is shown in Fig. 4.5 [Rio04a]. The first stage of the cascade consists of two SC integrators and a comparator Since there is only a single input branch, the signal gain g_1 and feedback gain g_1' are

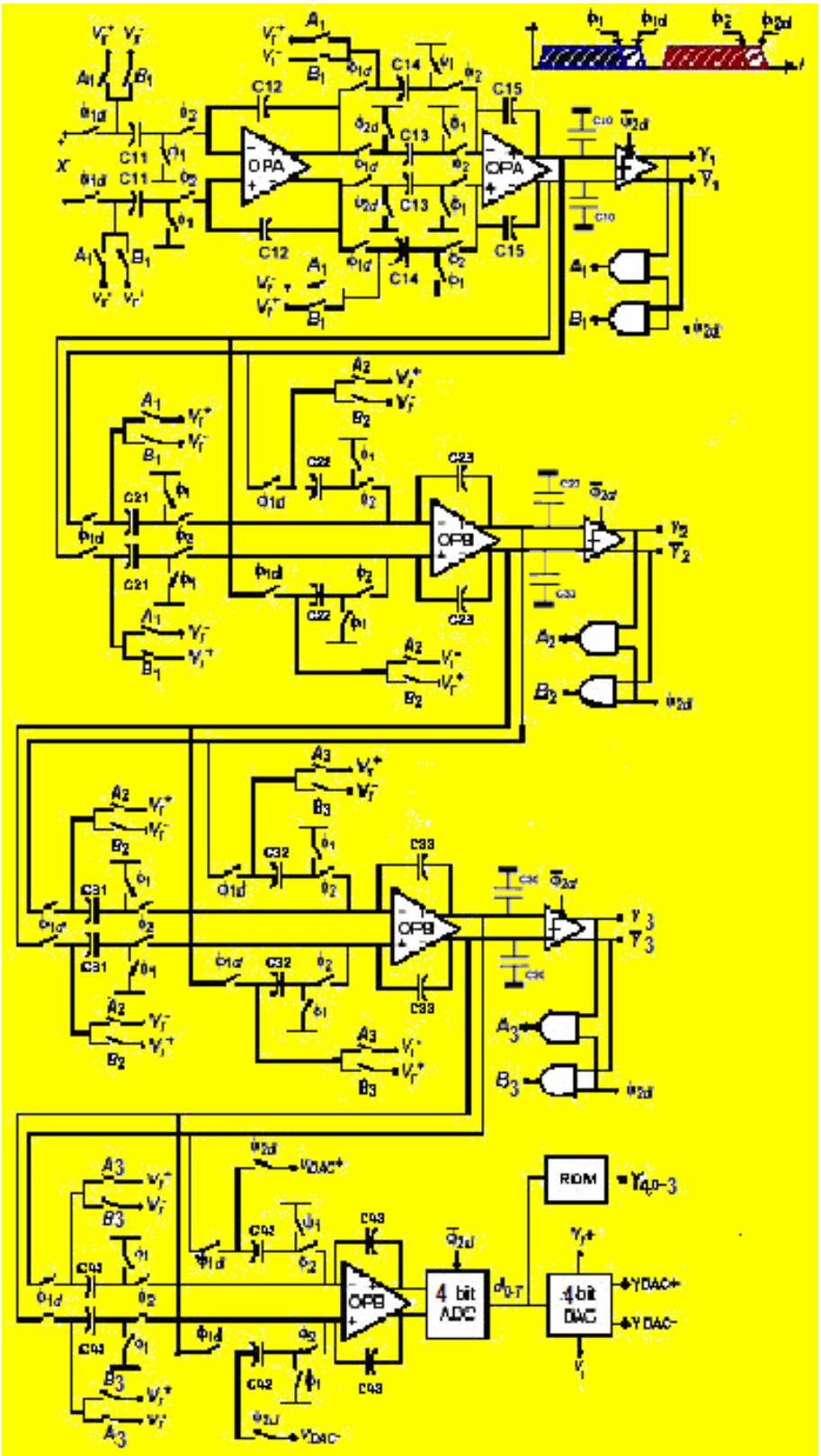


Fig. 4.5 The fully differential SC 2-1-1-1 Sigma-Delta modulator

identical in the front-end integrator and equal to C11/C12. Whereas the second integrator has two input branches, it realizes the different weights: g2=(C13+C14)/C15, g2'=C14/C15. The second stage uses an integrator with also two input branches, where three weights are implemented for this integrator: g3=(C21+C22)/C23, g3'=C21/C23, g3"=C22/C23, which are distributed between the two branches in order to save area . The same applies for the third and fourth integrators. At the back-end of the former stages except the last one the 1-bit comparator with a double reference (Vr, -Vr) is used. The integrator in the last stage drives a 4-bit ADC and the 4^{th} stage loop is closed with a 4-bit DAC. The output code of the ADC is converted into binary code by using a ROM. The analog version of that signal is fed back to the integrator using the sampling capacitors in the integration phase. Due to this capacitor sharing, the number of white noise sources is reduced, and consequently, the capacitor and OTA sizes can be scaled down by a factor of two, reducing the power consumption and die area. Furthermore, due to this sharing, the capacitive feedback factor is increased, reducing the integrators' capacitive load and moving the dominant pole of the closed-loop to a higher frequency. The modulator operation is controlled by two non-overlapping clock phases, $\phi 1$ and $\phi 2$. The integrator input signals are sampled during phase $\phi 1$ and then integrated together with the corresponding feedback signals during phase $\phi 2$. The comparators and the ADC are activated at the end of $\phi 2$ (using $\overline{\phi_2}$ as a strobe) to avoid any possible interference of the integrator's transient response at the beginning of sampling. In order to attenuate the signal-dependent charge injection [Lee85], delayed versions of the two phases are provided ($\phi 1d$ and $\phi 2d$). Note that, to avoid kickback noise, the input for every comparator is sampled on a 125-fF capacitor [Aug98].

4.5.2 Specifications for the building blocks

The second step of the modulator design is to estimate the requirements on the building blocks, such as amplifiers, capacitors, switches, comparators and multi-bit quantizers in the SC implementation. For this task, the non-ideality behavior models of the modulator operation, as mentioned in Chapter 3, have been compiled into the proposed 2-1-1-1 (4bit) Sigma-Delta modulator by using the tool Matlab and Simulink. The performance of the

modulator as a function of each parameter was derived. The results obtained are presented next.

4.5.2.1 Sampling capacitors sizing

The actual capacitor values depend only on KT/C thermal noise considerations. The total input-referred white noise power N_{wn} of the proposed converter, as shown in Fig. 4.5 is given by

$$N_{wn} \approx \frac{KT/C_{11}}{OSR} + \frac{\pi^2}{3}\frac{KT/(C_{13}+C_{14})}{OSR^3} + \frac{\pi^4}{5}\frac{KT/(C_{21}+C_{22})}{OSR^5} + \frac{\pi^6}{7}\frac{KT/(C_{31}+C_{32})}{OSR^7} + \frac{\pi^8}{9}\frac{KT/(C_{41}+C_{42})}{OSR^8} \quad 4.5.1$$

Equation (4.5.1) shows that the main contribution to the converter noise comes from the first integrator. Furthermore, it shows that all integrators can be progressively scaled down, without a negligible increase of the overall converter noise [Fel98] [Aug98]. Note that the sampling capacitors have to been chosen to be bigger, as the OSR is low. In order to simplify the design, the sampling capacitor of the first integrator is chosen considerable big that provides a noise floor low enough for 14-b resolution. In this case, the impact of the KT/C noises from the other SC-integrators can be neglected. This sets the lowest limit for capacitor value C11 as

$$C_{11} > \frac{12KT}{LSB^2 OSR} = \frac{12KT}{\left(V_{FS}^{\ 2}/2^{2N}\right)OSR} \quad 4.5.2$$

	Sampling Capacitors	Integration Capacitors
First stage	C11=2.5 C13=1 C14=1	C12=10 C15=2
Second stage	C21=0.5 C22=0.5	C23=1
Third stage	C31=0.5 C32=0.5	C33=1
Fourth stage	C41=0.5 C42=0.5	C43=0.5

TABLE 4.2 CAPACITOR SIZES

where k is Boltzmann's constant, T is 300 K, N is the number of bits 14 and V_{FS} the full scale voltage 2-volt. The capacitor value required for 14-bit resolution is 2.5 pF. All subsequent capacitors are scaled down due to the decreased noise contribution in the input. Table 4.2 shows the used capacitor values (the smallest unit capacitor is 0.125 pF).

4.5.2.2 Effect of the finite opamp gain

The finite gain of an integrator introduces simultaneously a gain and a pole error in the integrator transfer function. These errors are especially important in the first and second integrators of the first stage, which create noise leakage at low frequencies that is not canceled by the digital noise cancellation network. Therefore, the finite gain of an integrator can significantly degrade the converter performance. Fig. 4.6 shows the simulated SNDR as a function of the opamp gain when the amplitude of input signal is close to overloaded. To ensure that the degradation is smaller than 3 dB, the gain has to be higher than 2000. The final 3 dB can only be recovered at the expense of a large increase in gain. Therefore, to have a very small performance reduction and to provide some margin for other non-ideal effects, the design was made for a significantly higher gain, by resorting to an opamp structure with a gain of at least 80 dB (10000).

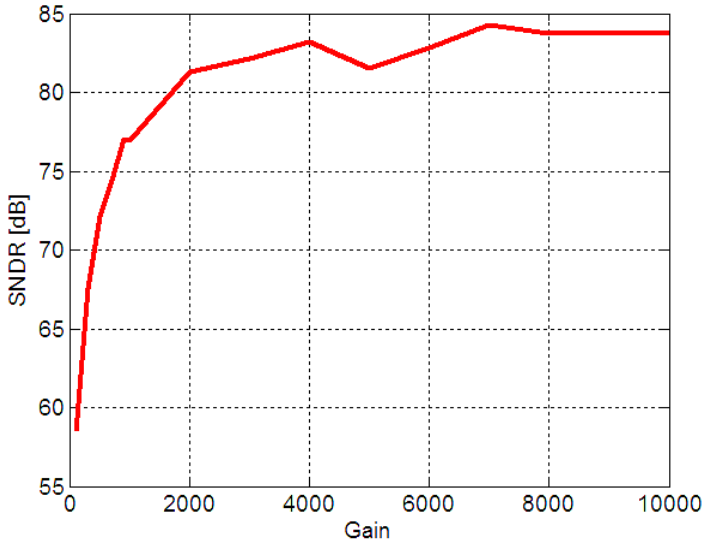


Fig. 4.6. SNDR as function of the opamp gain

4.5.2.3 Effect of the capacitor mismatch

The capacitor mismatch introduces a gain error in the integrator transfer function. It creates the noise leakage that is not canceled by the digital noise cancellation network. Therefore, the capacitor mismatch degrades the converter performance as shown in Fig. 4.7, in which the SNDR is simulated as a function of the capacitor deviation σ_c. In order to avoid the

obvious degradation of the performance (<3dB), the capacitor variation should be smaller than about 0.4%.

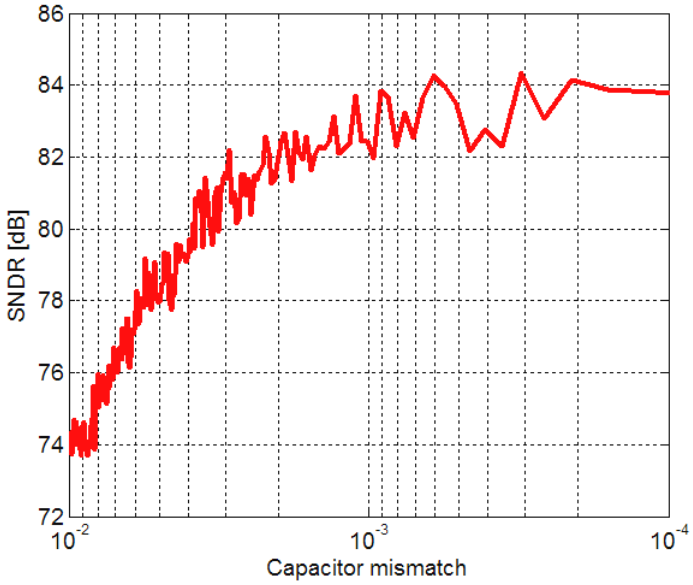


Fig. 4.7. SNDR as function of the capacitor mismatch

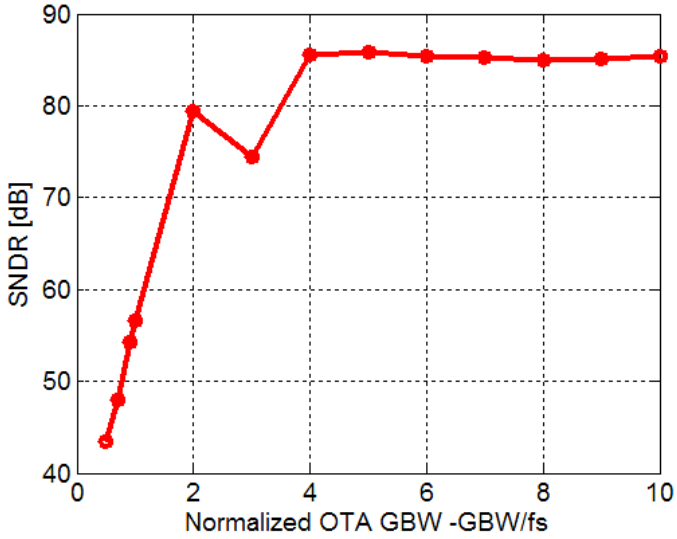


Fig. 4.8. SNDR as function of the opamp GBW

4.5.2.4. Effect of the finite opamp gain-bandwidth-product

The finite gain-bandwidth-product of opamp also introduces a gain and a pole error on the integrator transfer function as described in Chapter 3. Fig. 4.8 presents the behavioral simulation results of the proposed converter as a function of the finite gain-bandwidth-

product. Hence, the closed-loop pole has to be greater than 4 times the sampling frequency, to have a good performance. Considering providing some margin for other effects, the dominant closed loop pole was pushed to a higher frequency of about 850 MHz, for a clock frequency of 200 MHz.

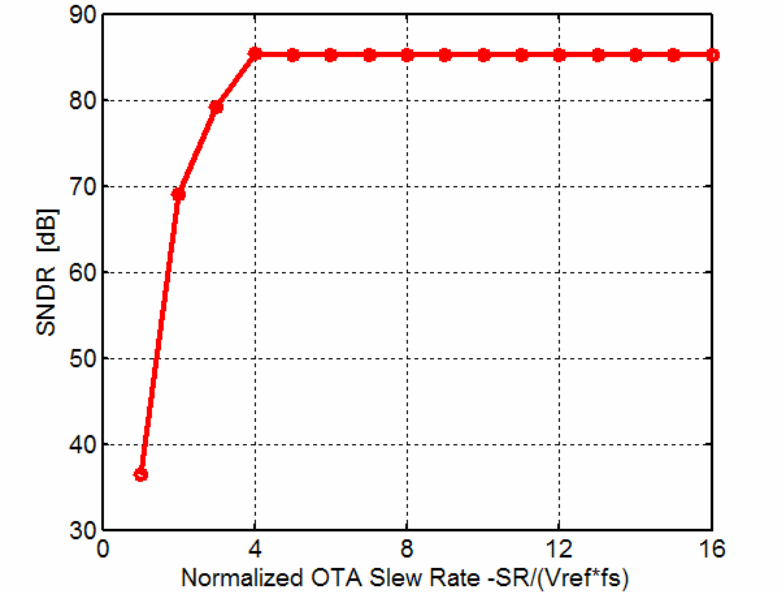


Fig. 4.9. SNR as function of opamp slew-rate.

4.5.2.5. Effect of the finite opamp slew rate

The finite opamp slew rate combined with the finite closed-loop pole can introduce a significant degradation in the overall transfer function of an integrator [San87]. If the switch resistance is assumed to be zero, then at the beginning of the integration phase, there is an instantaneous charge redistribution that immediately feeds forward the sampled voltage, causing the opamp to slew. Fig. 4.9 presents the results of the behavioral simulations of the overall converter as a function of the finite opamp slew rate, for an opamp gain of 80 dB and a closed-loop pole of 900 MHz. Hence the slew-rate should obey

$$SR > 4 f_s V_{ref} \qquad 4.5.2$$

With a 1-V reference, this means that the opamp slew rate should be higher than approximately 800 V/ μs. This slew rate specification is quite large and could imply that an unreasonably large overdrive voltage should be used for the input transistors, if only MOS transistors are used.

4.5.2.6. Effect of the non-linearity of the multi-bit DAC

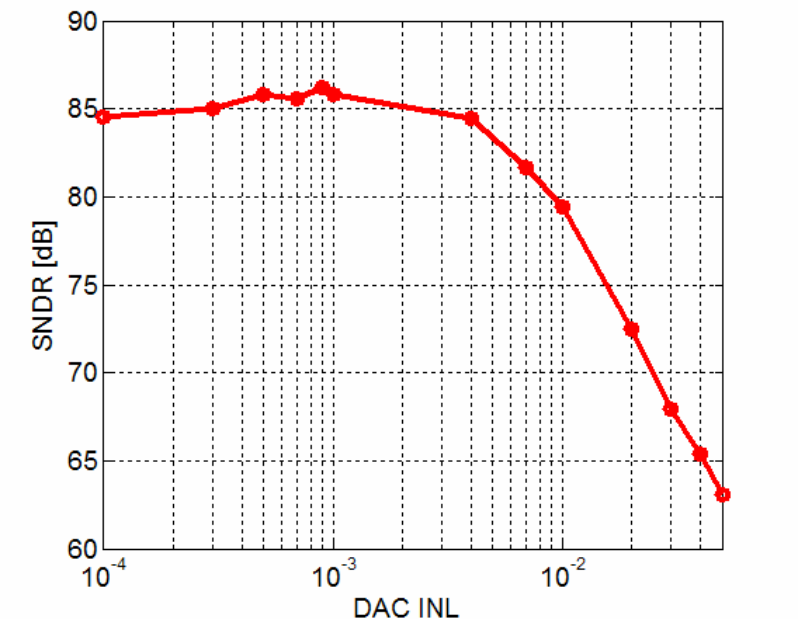


Fig. 4.10. SNR as function of the DAC INL

The proposed 2-1-1-1 cascade modulator has a 4-bit quantizer in the last stage, since it has better immunity to DAC imperfections, Therefore, it makes it possible to exploit a calibration-free multi-bit Sigma-Delta modulator. The DAC-induced error power can be represented with INL being the DAC integral non-linearity expressed in percentage of the full scale (%FS):

$$\sigma_D^2 = [FS*INL]^2 /2 \qquad 4.5.3$$

This error power is 4^{th}-order high-pass shaped (OSR^{-9}) in the 2-1-1-1[Med99a]. Fig. 4.10 shows the simulated SNDR as a function of the DAC INL. To ensure that the degradation is smaller than 3 dB, the INL should be smaller than 0.4%.

4.6. Design of the building blocks

This section will describe the circuit blocks on the experimental prototype chip. Details of the operational amplifier design such as common-mode feedback and biasing will be

discussed. Various auxiliary circuits such as comparator, bandgap, clock generator and output buffer will be described.

4.6.1 Operational amplifiers

The high-speed high-accuracy cascade Sigma-Delta A/D converters demand high open-loop gain opamps in the first stage, in order to suppress the non-linearity error and noise; on the other hand the broad unity-gain frequency are demanded, in order to reach the desired accuracy within settling time. It is difficult to simultaneously achieve both in a CMOS process. Therefore, the operational amplifiers in the first stage of the modulator are designed by using the BiCMOS technology. The rest operational amplifiers, which are used in the sequent stages of the designed cascade Sigma-Delta A/D converter, can be progressively scaled down, since their contributions of the in-band noise leakage from the third, fourth and fifth integrators due to the finite DC-gain are proportional to OSR^{-7}, OSR^{-9} and OSR^{-11} , respectively. Therefore, they are designed by using only PMOS and NMOS transistors. This section describes the design of the two operational amplifiers.

4.6.1.1 BiCMOS operational amplifier

For the opamps in the first stage, due to its good frequency characteristics, as well as its especially enhanced slew-rate, a fully differential folded cascode opamp is selected [Lac94]. The modified BiCMOS opamp is depicted in Fig. 4.11. The MOS pair as the input offers infinite input impedance to the switched capacity and avoids the current leakage even if the transistor switchs off. Large PMOS instead of NMOS input transistors are used to keep the flicker noise low. Due to lower transconductance of MOS transistors, the traditional use of MOS transistors is replaced by the NPN bipolar transistors Q_6 and Q_7 in the main opamp. Therefore, the second poles, occurring at the emitters of Q_6 and Q_7, are shifted to high frequencies due to the large transconductance and small parasitic of the bipolar transistors. As a result, the dominant pole and the unity-gain-bandwidth (UGBW) of the amplifier can be designed higher than the configuration of pure MOS transistors, with the same phase margin. In addition, the high transconductance together with high early voltage of the NPN bipolar transistors (V_A=90V) offers over two orders higher a

magnitude of the output impedance than PMOS transistors, which effectively increase the output impedance of the cascade bipolar NPN and NMOS. Therefore, the gain-boosting stage [Bul90] is only needed for the cascade of the PMOS side to increase the corresponding output impedance, hence simplifying the circuit and resulting in additional power saving.

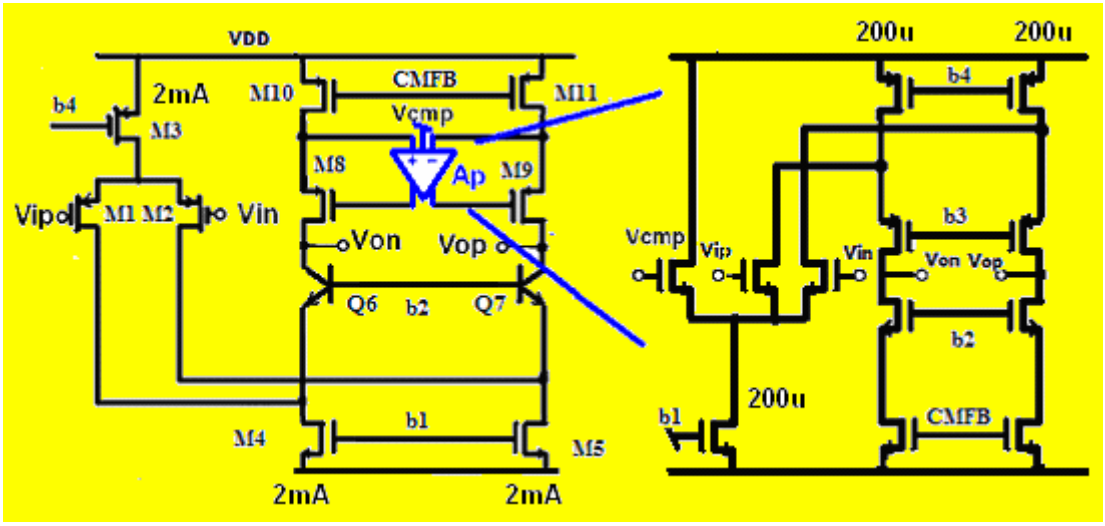


Fig. 4.11. BiCMOS Operational Amplifier

The gain-boosting amplifier is shown in the right half of Fig. 4.11. It is designed in the folded-cascode topology. Compared with a common source amplifier, folded-cascode gain stages provide higher DC gain with a high input swing. The cost for this enhancement, however, is a small increase in power and area. The gain-boosting amplifier operates at 1/10 of the main amplifier's bias current. Neither the frequency nor the settling characteristics are impaired [Fla96]. Thus, the DC gain of the overall operational amplifier is in the order of $(gmro)^4$, boosted above 90 dB.

In a fully-differential amplifier, a common-mode feedback is needed to define the DC voltages at the high impedance output nodes. A dynamic (switched-capacitor) common-mode feedback is selected because it does not dissipate additional power.

Figure 4.12 illustrates the switched-capacitor CMFB circuit [Gra01] adopted for the main gain stage, where Φ1 and Φ2 are non-overlapping phases. The common-mode feedback uses capacitors C_{m1} and C_{m2} to sense the output common-mode voltage. Since the integrator is active on both clock phases, switched capacitors C_{CM1} and C_{CM2} are used to

define the appropriate dc voltage on the sense capacitors. V_{CM0} is the desired output common-mode voltage, and v_{bns_cm} is a bias voltage formed by a diode-connected transistor with a current source to create the proper replica bias current. Minimum size devices are used for the CMOS switches (Ms1-Ms8), and $C_{m1,2}$ and $C_{CM1,2}$ are 20fF and 4fF, respectively.

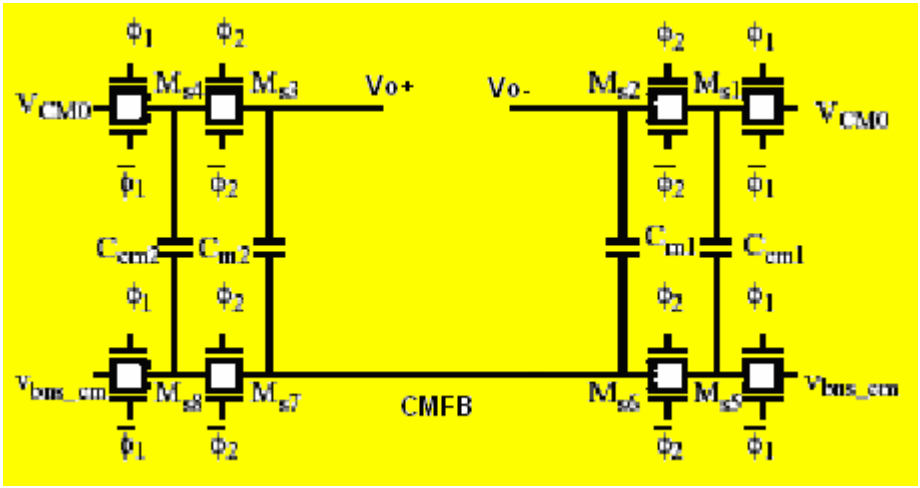


Fig. 4.12. Switched-capacitor CMFB circuit

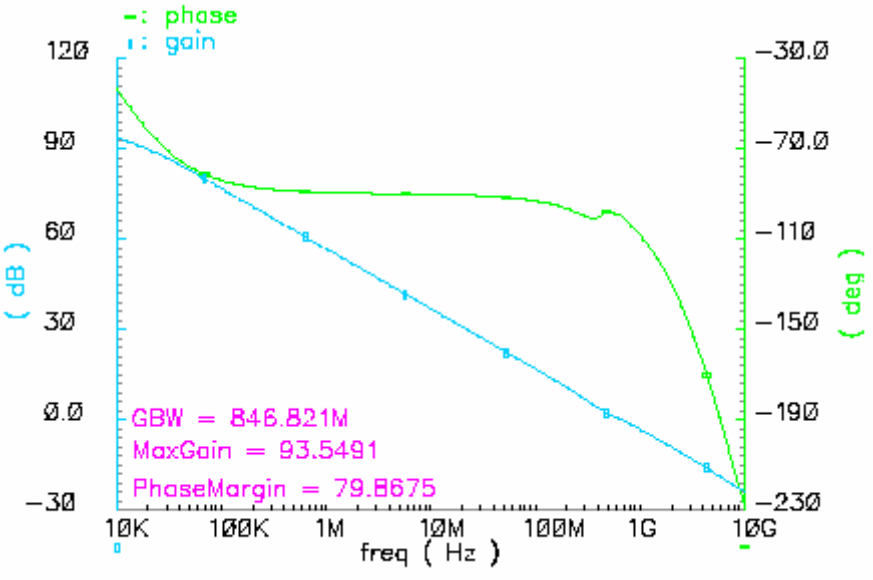


Fig. 4.13. opamp AC characteristics

Simulations show that the CMFB loop has a phase margin of 72°. The nominal output common-mode voltage VCMO is 1.8 V for this implementation.

With a current consumption of 4.4 mA, of which 4 mA are spent in the main amplifer and the rest in the regulating amplifers. The implemented OTA has gm=16 mS, I_{M3}=2 mA, and I_{M10}=1 mA. The extracted equivalent load capacitor is about 3 pF. The slew-rate and the closed-loop unity-gain frequency can be expressed as:

$$SR = \frac{I_{M3} + I_{M10}}{C_L} \approx 1000 \quad V/\mu s \qquad 4.6.1$$

$$f_{cl} = \frac{gm}{2\pi C_L} \approx 850 \quad MHz \qquad 4.6.2$$

Fig. 4.13 illustrates the AC simulation result that GBW is about 846 MHz, maximal DC-gain is about 93.54 dB and phase margin is about 79.86 °.

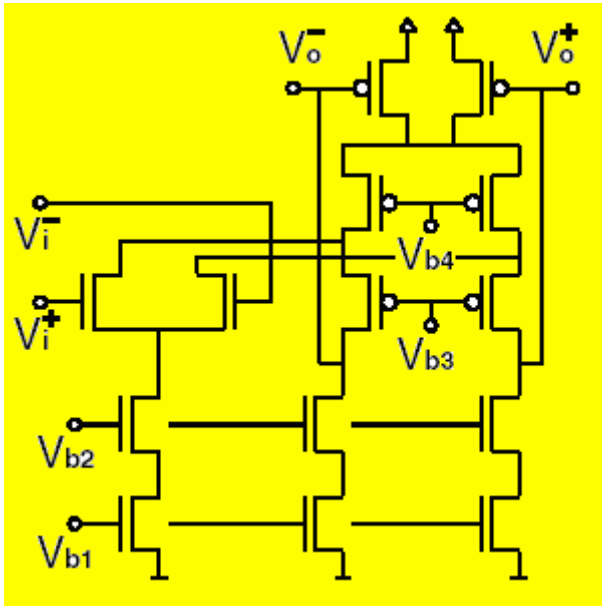


Fig. 4.14 Schematic of the rest opamps.

4.6.1.2. CMOS operational amplifier

As aforementioned that the input-referred noises are decreased by the high-order filters character in the Sigma-Delta modulator. Therefore, the opamps can be scaled down as the sampling capacitors. The relative scaling of the OTA's is 1:1:0.2:0.2:0.2. Therefore, the opamps in the success stages are designed in CMOS.

The fully differential folded cascode opamp is designed as shown in Fig. 4.14. It is biased at one fifth the current of the previous one, without the gain enhancement. The achieved

maximal DC-gain is 60 dB; phase margin 70°; output swing of the opamp is = 4 V (full-differential); and the maximum GBW 800 MHz with a 3.3V supply voltage. The opamp uses a continuous-time common mode feedback, which is advantageous for the transistor sizes used in these designs [Bur98].

4.6.2 Comparators

Comparators are the other most important analog components in Sigma-Delta ADCs. The function of a comparator is to compare the applied input signal voltage with a reference voltage. Then, the signal is further amplified to the digital logic level for subsequent processing.

4.6.2.1 Single-bit comparator

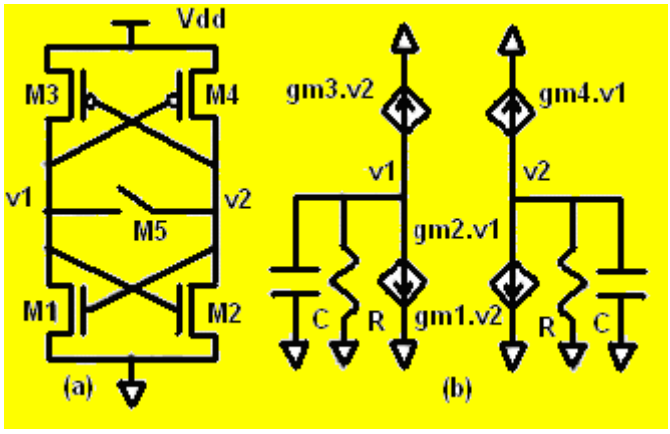


Fig. 4.15 The basic regeneration latch comparator and its corresponding model

In the cascaded 2-1-1-1 Sigma-delta A/D converter, the single-bit quantizers at the end of the first, second and third stages of the modulator demand only a low resolution. Moreover, Sigma-Delta A/D converters are insensitive to comparator offset and hysteresis [Rio04b]. However, the maximum comparison time can be designed at 1.25 ns —a quarter of the worst-case clock period. For this reason, the latched comparator is preferred.

The basic CMOS regenerative latch can be simplified as shown in Fig 4.15a. It consists of a n-channel flip-flop and a p-channel flip-flop in a positive feedback loop. It can be

modeled by its small signal equivalent circuit shown in Fig. 4.15.b [Kla96] [Haj98]. There exist the following functions for v_1 and v_2

$$\frac{d v_1}{dt} + \frac{G_0}{C} v_1 + \frac{G_m}{C} v_2 = 0 \qquad 4.6.3$$

$$\frac{d v_2}{dt} + \frac{G_0}{C} v_2 + \frac{G_m}{C} v_1 = 0 \qquad 4.6.4$$

where C represents the total parasitic capacitance on regenerative nodes, and

$$G_m = g_{m1} + g_{m3} = g_{m2} + g_{m4} \qquad 4.6.5$$

$$G_0 = g_{01} + g_{03} = g_{02} + g_{04} \qquad 4.6.6$$

where $g_{m1}=g_{m2}$ and $g_{m3}=g_{m4}$ represent the transconductance of the NMOS and PMOS devices at the beginning of the operation, respectively; $g_{o1}=g_{o2}$, and $g_{o3}=g_{o4}$ are the output conductances of the NMOS and PMOS devices. This pair of equations can be decoupled, defining the following variables:

$$v_{diff} = v_1 - v_2 \qquad 4.6.7$$

$$V_{cm} = \frac{v_1 + v_2}{2} \qquad 4.6.8$$

During the sensing period, the major interest is the differential voltage which is governed by

$$\frac{dv_{diff}}{dt} + \frac{G_0 - G_m}{C} v_{diff} = 0 \qquad 4.6.9$$

This equation has the following solution

$$v_{diff}(t) = v(0) e^{t/\tau} \qquad 4.6.10$$

where

$$\tau = \frac{C}{G_m - G_0} \cong \frac{C}{g_m} \qquad 4.6.11$$

The time required for the output to reach a minimum acceptable voltage difference, V_{min} is given by $t = \tau . \ln \frac{V_{\min}}{V_{init}}$ [Kla96].

Fig.4.16 shows the architecture employed for the implementation of comparators [Yuk85]. The CMOS latch is composed of a NMOS flip-flop (M3, M4) with a pair of n-channel

transfer gates (M9, M10) for strobing, and a p-channel flip-flop (M5, M6) with a pair of p-channel precharge transistors (M7, M8). Additionally, a differential NMOS pair (M1 and M2) is employed as the input. The opration of the comparator is controlled by the clock: $\overline{Phi2}$. When $\overline{Phi2}$ is low, the comparator is in the reset mode. In this mode, a voltage proportional to the input voltage difference is established between nodes X1 and X2. In the same time, M9 and M10 are opening, which isolate the input and output.The p-channel flip-flop is reset by the two closed precharge transistors M7 and M8, which charge nodes *a* and *b* to the positive power supply voltage. As a result, the outputs of the inverters are forced to the low state and the previous two logic state voltages at output are unchanged by an SR flip-flop, which is depicted in Fig.4.16*b*. When $\overline{Phi2}$ is high, the comparator is in the regeneration mode. In this mode, the n-channel flip-flop, together with the p-channel flip-flop, regenerates the voltage differences at X1 and X2. The voltage difference is soon amplified to a voltage swing nearly equal to the power supply voltages. The following *S-R* latch is driven to full complementary digital outputs. The electrical simulation shows that the comparator is suitable to the high-speed one-bit application.

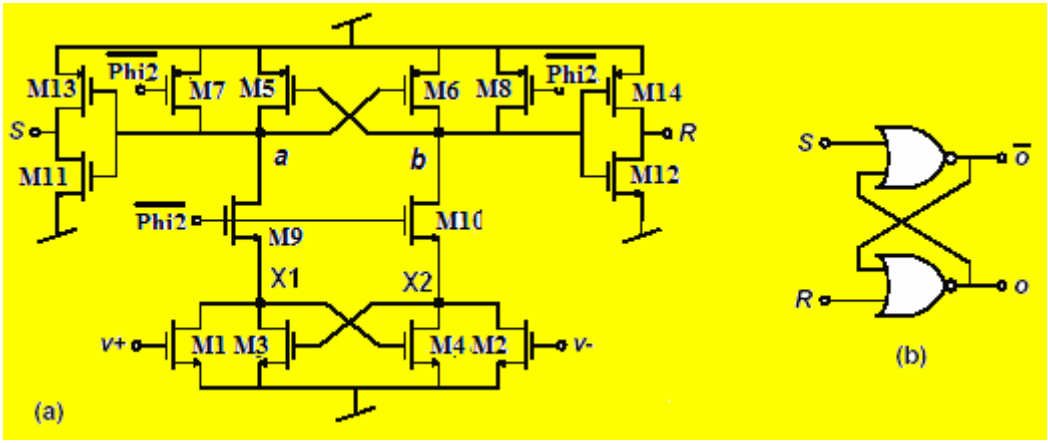


Fig. 4.16 Comparator implementation: (a) Regenerative latch, (b) SR latch.

4.6.2.2. 4-bit comparator

With respect to the 4-bit flash A/D converter in the last-stage, the dynamic comparator based on a regenerative latch with a pre-amplifying stage is applied. Fig.4.17 shows the architecture employed for the implementation of comparators [Yin92]. It includes a PMOS input differential-pair, a CMOS regenerative latch stage, and a SR latch. The CMOS latch

is composed of a n-channel flip-flop (M3, M4) with a pair of n-channel transfer gates (M5, M 6) for strobing, a n-channel switch (M11) for resetting, and a p-channel flip-flop (M8, M9) with a pair of p-channel precharge transistors (M7, M10). The comparator is controlled by two non-overlapping clocks: Phi1 and Phi2.

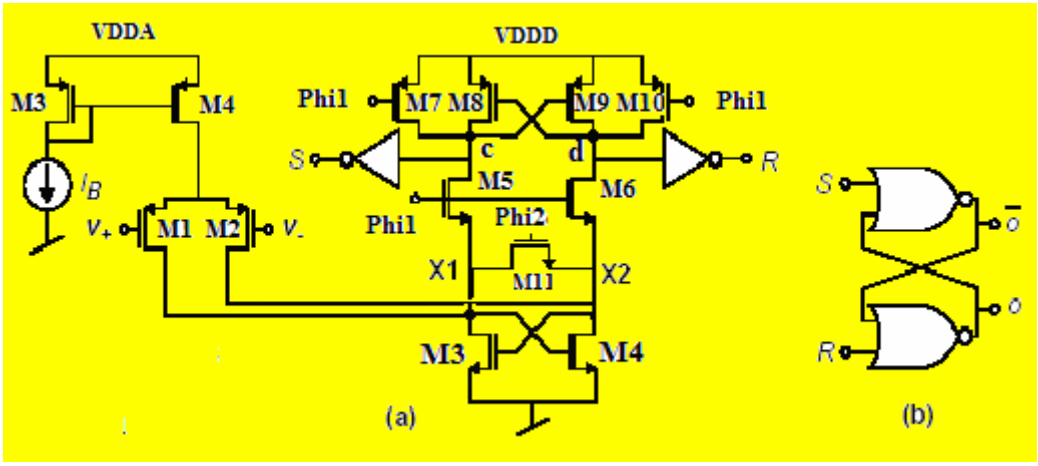


Fig. 4.17 Comparator: (a) Pre-amplifier and regenerative latch, (b) SR latch.

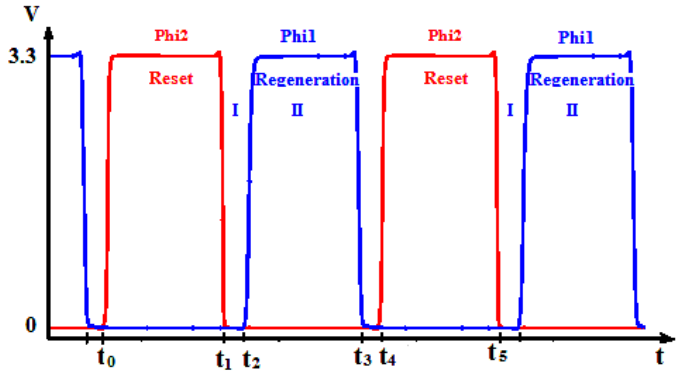


Fig. 4.18. Time relation between Phi1, Phi2

The dynamic operation of this circuit is divided into a reset time interval (t_0-t_1) and a regeneration time interval (t_2-t_3), as shown in Fig. 4.18. When Phi2 is high, the comparator is in the reset mode. Current flows through the closed resetting switch M11, which forces the note voltages at X1 and X2 to be equalized; the n-channel flip-flop is reset. In the meantime, the p-channel one is also reset by the two closed precharge transistors (M7 and M10), which charge nodes *c* and *d* to the positive power supply voltage. As a result, the outputs of the inverters are forced to the low state and the previous two logic state voltages at output are kept unchanged by an SR flip-flop, which is depicted in Fig.4.17*b*. When both

Phi2 and Phi1 are low (t_1-t_2), the M5 and M6 isolate the still precharged p- channel flip-flop and the n-channel flip-flop. At the same time, the PMOS input differential-pair performs the voltage-to-current conversion and a voltage proportional to the input voltage difference is established between nodes X1 and X2. This voltage will act as the initial imbalance for the following regeneration time interval, when the clock Phi2 is low, Phi1 is high. The n-channel flip-flop, together with the p-channel flip-flop, regenerates the voltage differences between nodes *X1* and X2 and between nodes *c* and *d.* The voltage difference between node *c* and node d is soon amplified to a voltage swing nearly equal to the power supply voltages. The following *S-R* latch is driven to full complementary digital output levels at the end of the regenerative mode and remains in the previous state in the reset mode. There is no slew-rate problem in the regenerative period because the p-channel flip-flop is used instead of two class-A current sources.

In this design, the IB is 60uA that is enough for the 200MHz sample application. Monte Carlo and corner analysis have been used to characterize the comparator after full sizing. Table 4.3 summarizes its worst-case performance.

Hysteresis	**120 uV**
Offset	**6.3 mV**
Power consumption	**1 mW**

TABLE 4.3 Worst-case electrical simulation results for the comparator

4.6.3. Band gap

The bandgap voltage reference is often used to create the bias reference voltages in an analog-to-digital converter. Ideally, this block will supply a fixed dc voltage of known amplitude that does not change with temperature.

Figure 4.19 shows the complete schematic diagram of the designed bandgap reference circuit. It consists of the basic bandgap cell, start up circuit, and output buffer. The band gap circuit is based on cancelling the negative temperature dependence of a pn junction (or

base-emitter junction) with positive temperature dependence of a proportional to the absolute temperature (PTAT) [Joh97].

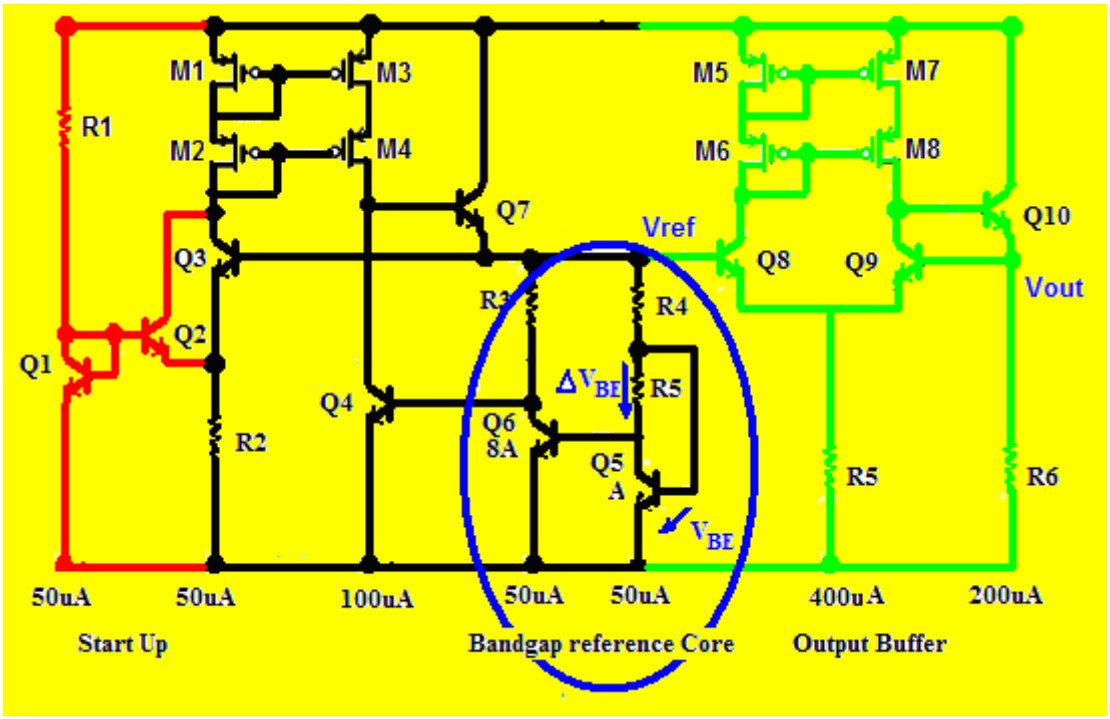


Fig. 4.19 the complete schematic diagram of bandgap reference

The basic bandgap cell consists of Q_5, Q_6, R_3, R_4 and R_5 in the figure. The reference voltage V_{ref} is the sum of the V_{BE} of Q_5 and the temperature -dependent voltage across R_4. The base-emitter voltage (V_{BE}) of a bipolar transistor Q_5 has a negative temperature coefficient. The transistors Q_5 and are biased with different current densities by choosing the emitter area of Q_6 larger than that of Q_5 by a ratio of 8-to-1. Therefore, the difference of the base-emitter voltage Q_5 and Q_6 (ΔV_{BE}) is proportional to the absolute temperature (PTAT).

Since the current in R_5 is equal to the current in R_4, and the voltage across R_4 is given by

$$V_{R4}=\frac{R_4}{R_5}\Delta V_{BE}=\frac{R_4}{R_5}\frac{kT}{q}\ln\left(\frac{J_5}{J_6}\right) \qquad 4.6.12$$

the created reference voltage is given by

$$V_{ref}=V_{BE}+\frac{R_4}{R_5}\frac{kT}{q}\ln\left(\frac{J_5}{J_6}\right) \qquad 4.6.13$$

Now, this reference voltage can be set by adjusting R_4/R_5, to a temperature-independent value.

In order to determine the resistor ratio, the equation is differentiated with regard to the temperature, and it is obtained:

$$\frac{\partial V_{ref}}{\partial T}=\frac{\partial V_{BE}}{\partial T}+\frac{R_4}{R_5}\frac{k}{q}\ln\left(\frac{J_5}{J_6}\right) \qquad 4.6.14$$

For the constant *Ic*, V_{BE} has approximately a -1.31mV /°K temperature dependence at 50°C, as the illustrated point A in Fig. 4.20. Therefore, the resistor ratio R4/R5 is set to about 7, which results in an approximately 1.31mV /°K temperature dependence at 50°C, as the illustrated point B in Fig. 4.20, exactly to compensate the negative temperature coefficient of V_{BE}.

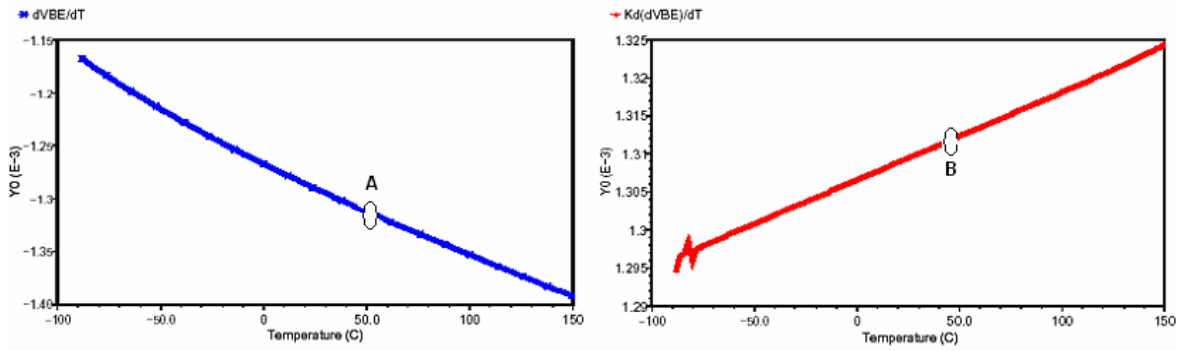
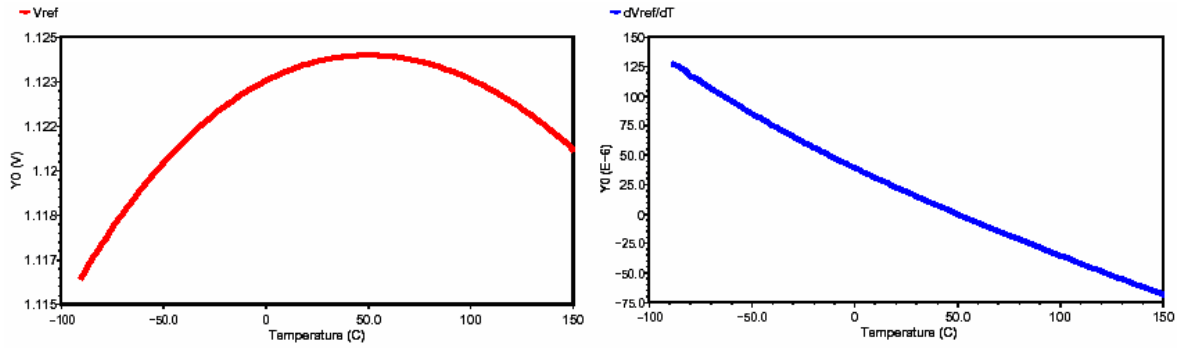


Fig. 4.20 Temperature dependence of V_{BE} and $K\Delta V_{BE}$

The bandgap circuit has two stable operation points: the desired one and the other, where the current is zero. To ensure that the circuit always ends up, even when the base voltage of Q5 and Q6 is zero, a startup circuit is included. There, the resistor R1 is used to produce a current, therefore, the collector-base connected transistor Q1 is always on. A transistor, Q2, is incorporated into the circuit to provide starting. The transistor insures that a minimum current flows into the cascode PMOS pair of M1 and M2, even when the base voltage of Q5 and Q6 is zero. This current is "reflected" by the cascade current mirror M3 and M4 to drive Q7 and turn on the circuit. Once the circuit is on, the collector current of Q7 becomes nearly equal to the current in Q4. Moreover, the emitter current of Q7 is split to provide Q5 and Q6 with equal collector currents.

The voltage provided by the band gap reference is generated by a resistor, and thus it is not suitable for supplying a switched capacitor load without buffering. The generated reference voltage is buffered with the unity gain buffer. The schematic of the buffer is shown on the right side of Figure 4.20. It is an amplifier, which consists of a differential pair (Q8 and Q9), a cascode current mirror load (M5-M8), and an emitter follower (Q6 and R6) connected in unity gain feedback. The current sources are cascoded to increase the output current accuracy.

Fig. 4.21 (a) shows the simulated output voltage of the proposed bandgap circuit as a function of temperature. The output voltage is equal to the target voltage 1.124 V at 50C, and the peak-to-peak variation is 8 mV in the temperature range from -100 °C to 150 °C. The power dissipation of this bandgap circuit is approximately 3 mW from a 3.3-V supply. The temperature dependence of Vref is demonstrated in Fig.4.21 (b). The temperature coefficient of this bandgap voltage reference is less than ±100 ppm/°C.



(a) **(b)**

Fig. 4.21 a)Output voltage versus temperature
b)Temperature dependency of output voltage

4.6.4. Bias

The high-swing cascode bias [Lab87] [Abo99], as shown in Fig. 4.22, is used for the prototype chip. A master biasing current source is created through the band-gap voltage, as mentioned before, incorporating the cascade of diode-connected PMOS devices. The functions of the NMOS side in the circuit are described as following, and the PMOS version is similar.

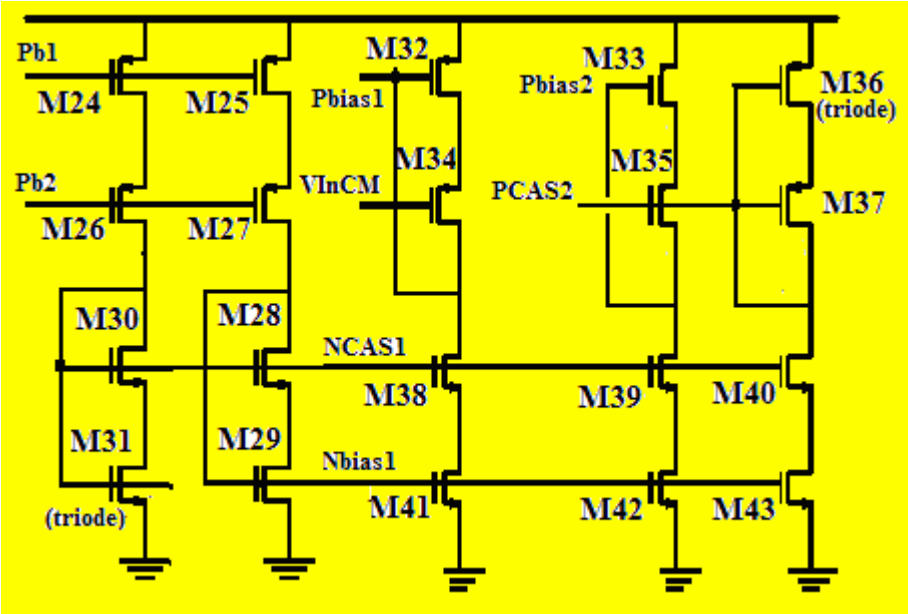


Fig. 4.22 Bias circuit

To bias common-source devices whose drain is connected to the source of a cascode device, such as the NMOS devices M4 and M5 in Fig. 4.22, a configuration such as M29 and M35 is used to generate the gate bias voltage on the PMOS side. M29 is essentially a diode-connected device except that M28 mimics the cascode device so that the drain-to-source voltage of in-circuit device (M4, M5) and the bias device (M29) are approximately equal. This eliminates the first order mismatch due to finite output impedance (Early effect). To bias the cascode devices, Q6 and Q7, a stack of devices driven by a current source was used, such as M30 and M31. This scheme provides a high-swing cascode bias [Lab87] [Lin91]. M31 operates in the triode region, M30 is a diode-connected device operating in the saturation region, and M24 and M26 acts as a current source. M31 is sized to create a V_{ds} that is sufficient to keep Q6 and Q7 in the linear region. M28 and M30 have the same current density as Q6 and Q7, therefore $V_{gs28} = V_{gs30} = V_{be6}$. Furthermore to ensure that all devices are operating in saturation under all conditions, $V_{ds} > V_{dsat} + 200$ mV is required. At the output of the opamp a single-ended swing of 1V was chosen. From these specifications, the $(V_{gs} - V_t)$ values of all PMOS devices were chosen to be 200mV and of all NMOS devices to be 150mV. The current levels in the bias circuits were chosen to be 400 uA.

4.6.5. Switch

An effective way to reduce on-resistance of the switch and to extend its linear range is to employ a voltage higher (in the case of nMOS) than the supply with a charge pump to control the switch transistor gate.

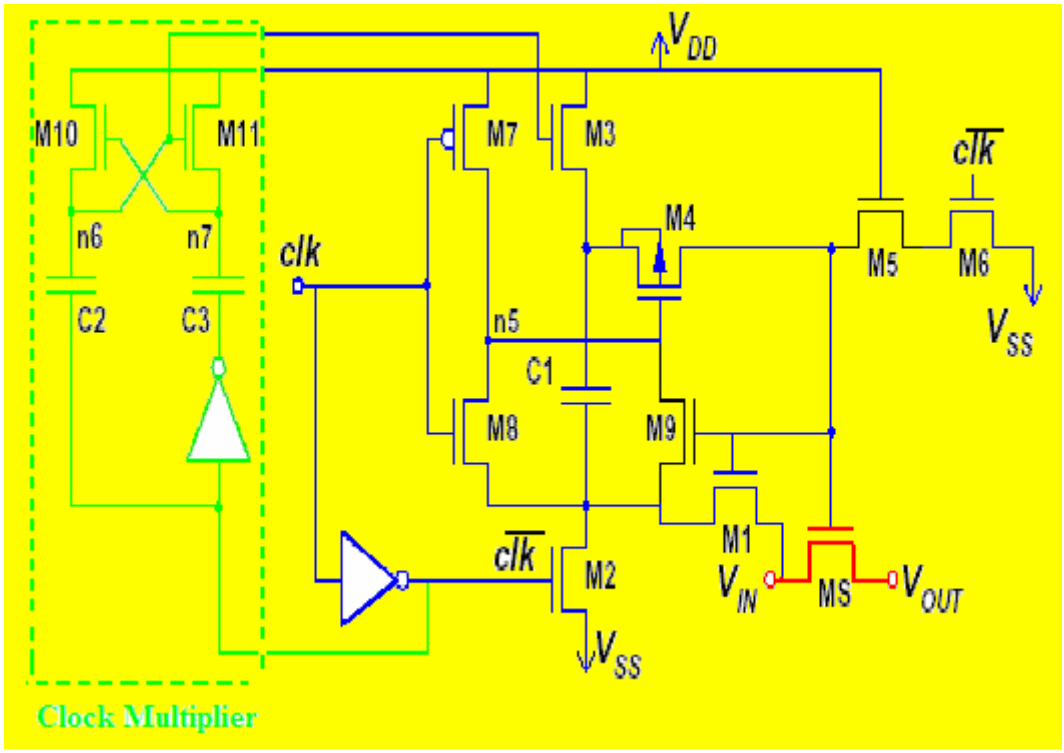


Fig. 4.23 Bootstrapped NMOS switch

The bootstraped single NMOS switch with a local charge pump circuit is shown in Figure 4.23 [Abo99]. It operates on a single phase clock clk that turns the switch MS on and off. When clk is low, $\overline{clk}$ is high, the gate of MS is grounded through the device M5 and M6, and the switch is cutoff. At the same time, the capacitor C1 is charged to V_{DD} by M2 and M3. M4 and M1 isolate the switch from C1 while it is charging. When Phi goes high, M8 pulls down the gate of M4, allowing charge from the battery capacitor C1 to flow onto the gate G. This turns on both M4 and M11. M1 enables the gate G to track the input voltage S shifted by V_{DD}, keeping the gate-source voltage constant independent of the input signal. In figure 4.23, device M5 is simply used to improve the circuit reliability by reducing the V_{ds} and V_{gd} of device M6 when $\overline{clk}$ = 1. Therefore, the channel length of M7 can be

increased to further improve its punchthrough voltage. The device M9 is used to ensure that V_{gs4} does not exceed V_{DD}. M10, M11, C2, and C3 form a clock multiplier that enables M3 to charge C3 during the off phase.

Figure 4.24 shows the output waveforms of the bootstrap switch. The gate voltage of the switch transistor V_g is boosted to $V_{DD}+V_i$, where V_i is the analog input signal and V_{DD} is the supply voltage. Therefore, a fixed difference of V_{DD} is applied for gate-source voltage of the switch during the on-phase of the switch. As a result, this switch has the advantage that the transistor gate-source (or gate-drain) voltage may not exceed the nominal supply voltage. It satisfies the condition of technology reliability and ensures the switch a long lifetime operation. Besides reliability, another advantage of this circuit is that a low on-resistance may be established from drain to source, which is independent of the input signal, since the gate-source voltage is constant. Therefore, a major source of nonlinearity is greatly attenuated.

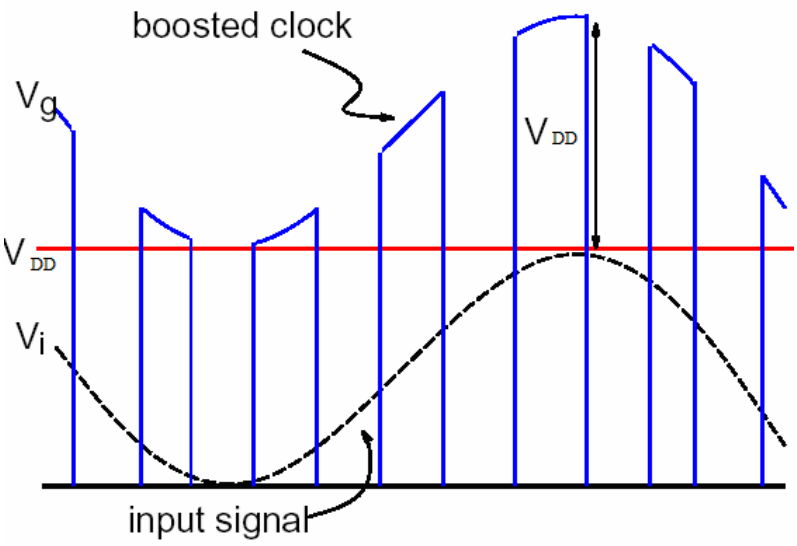


Fig 4.24 Waveform of Bootstrapped NMOS switch

In practice, the gate-source (or gate-drain) voltage is somewhat lower because of parasitic capacitances associated with the switch transistor and the auxiliary switches. Note that the parasitic capacitances may cause some distortion. In order to minimize the attenuation of the gate voltage and distortion, the parasitic capacitances have to be minimized and the bootstrapping capacitor C1 has to be made large.

4.6.6 Clock generator

Switched-capacitor circuits require the generation of two-phase non-overlapping clocks with delayed clocks to reduce the signal-dependent charge injection. The clock generator for producing non-overlapping clock signals can be realized with a simple circuit constructed with logic gates. Such a circuit is shown in Fig. 4.25 [Abo99]. An external 50% duty-cycle reference clock drives the input CLKIN. The falling edge of the input clock passes immediately through the NAND1, whileas the rising edge passes through the NAND2, until the passed clock from the NAND1 through the cascaded delay element feedbacks to the input of the NAND2. The duration of the dependent phases is a function of the propagation delays of the various gates in the clock generator. By adjusting these delays, the designer can allocate the time spent in each of the phases. The resulted non-overlapping signals Phi1 and Phi2 have a non-overlapping time equal to the sum of the delays at the NAND gate and the delay element. The delay element is usually realized with an even-numbered chain of inverters. The NAND3 and NAND4 delay clock signals Phi1d and Phi2d.

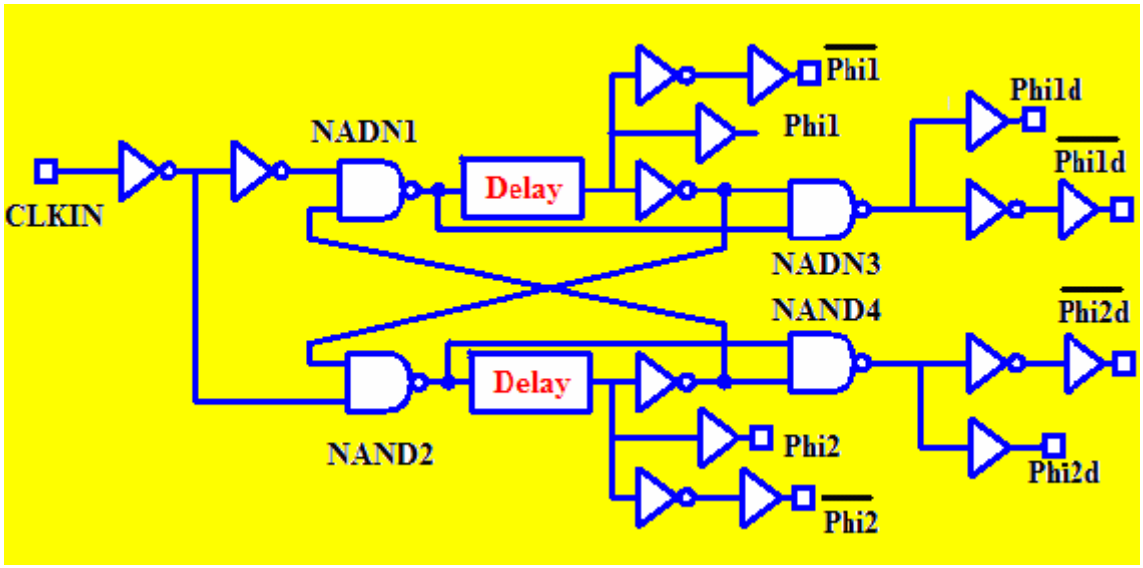


Fig. 4.25 Clock generator

In the prototype, the non-overlapping clock signals and their inverted phases are buffered and routed across the chip for respective applications. Figure 4.26 shows the clock

waveforms.

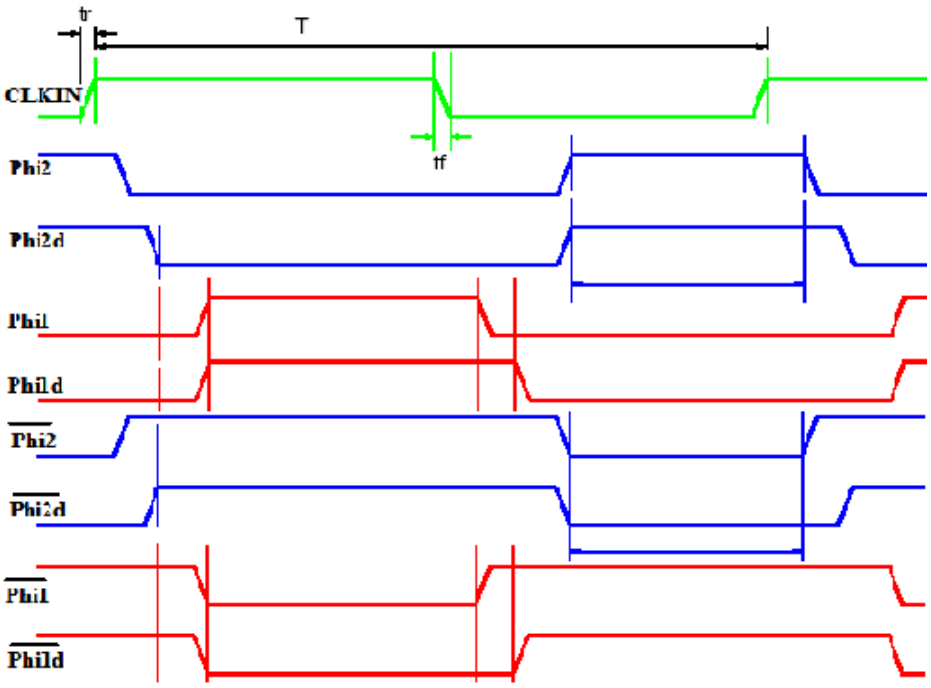


Fig. 4.26 Clock waveforms

The main advantage of this circuit is its simplicity. At least a part of the buffering of output signals can be included in the delay elements, making the circuit quite robust. On the other hand, the input clock is required to be close to 50% duty cycle since the non-overlapping clock signals are generated inherited from the input clock.

4.6.7. 4-bit A/D/A converter

The last-stage quantizer is implemented by means of a A/D/A converter with 4-bit quantization. The SC implementation of the 4-bit A/D/A converter is illustrated in Fig.4.27. A/D converter.

The A/D converter uses a fully-differential flash architecture [Lewis87] [Bran91b] and compares the differential input voltage v_i^+, v_i^-, (5th-integrator output) with reference voltages v_r^+, v_r^-, generated in a resistive-ladder DAC. During ϕ_1 references v_r^+, v_r^-, are stored in the input capacitors, which are then used to compute the difference $(v_i^+ - v_i^-) - (v_r^+ -$

v_r^-) during ϕ_2. At the end of ϕ_2, comparators are activated to solve the sign of that difference. The thermometer output code of the 15 comparators is then translated to a code using AND gates.

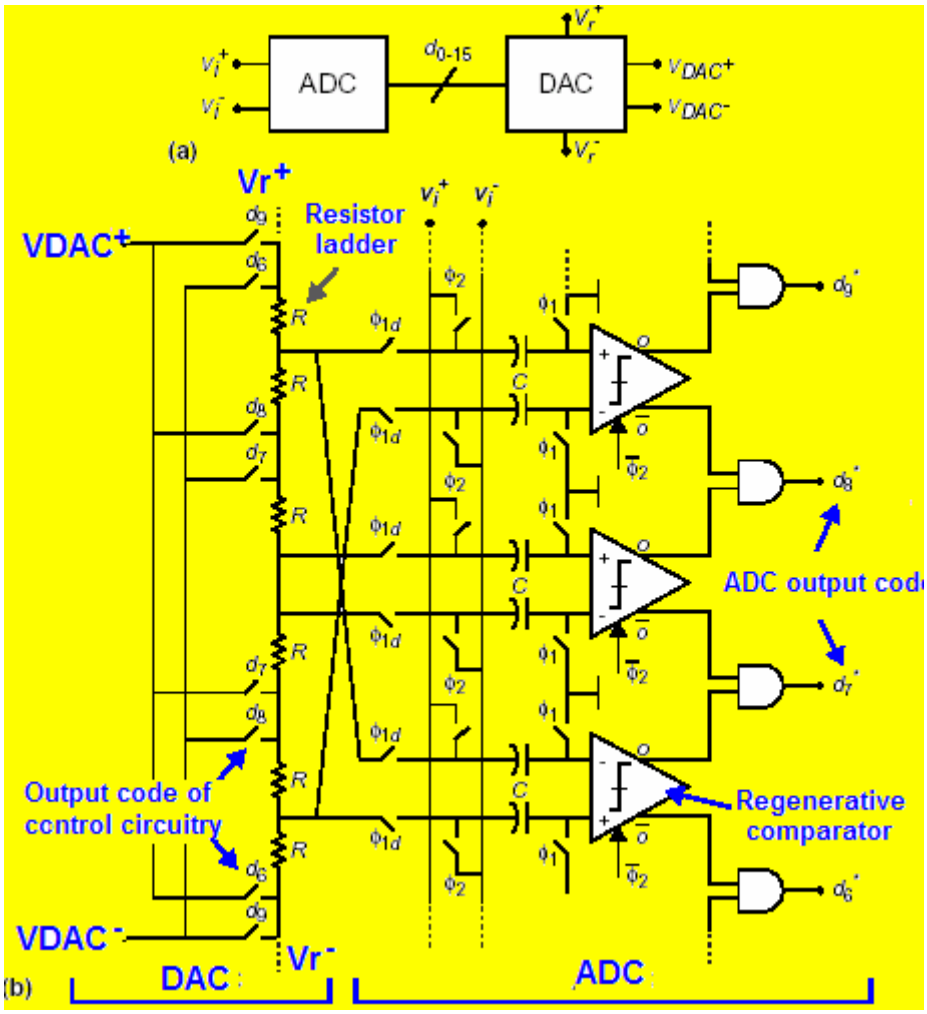


Fig.4.27. 4-bit A/D/A converter: (a) Block diagram, (b) Partial view of the SC implementation.

The D/A converter consists of a simple resistor ladder. The ladder consists of 30 unit resistors of value 50 Ω connected between reference voltages Vr^+ and Vr^-. The resistor ladder provides the reference voltages for the operation of the ADC, and generates the analog output of the overall A/D/A converter, through the selection of the voltages generated in the ladder by the 1-16 output code of the ADC ($d_{0\text{-}15}$) [Rio04a].

4.6.8 Output buffers

Supply and ground noises occur when variable currents are injected into the supply and ground. As is known from digital circuits, state changing can cause big digital noise. Thus, in this design the target is to minimize digital noise-coupling into the substrate as well as through the bond wires by using a constant bias current. The buffer utilized is shown in Figure 4.28; it mainly consists of NMOS switch-pairs (M4-M7) and a differential low gain amplifier. The differential pair (M2 and M3) is controlled by differential digital input by switching constant reference voltages appropriately through NMOS switches. The output of the amplifier drives digital signals on chip to a 400 ohm load resistor, to obtain an 800mV peak-to-peak digital signal. Therefore, a constant current is maintained into the substrate through transistor M1 that is independent of the digital output. The differential signal further provides first-order cancellation of the noise power induced in the bond wires, when the signal comes off chip.

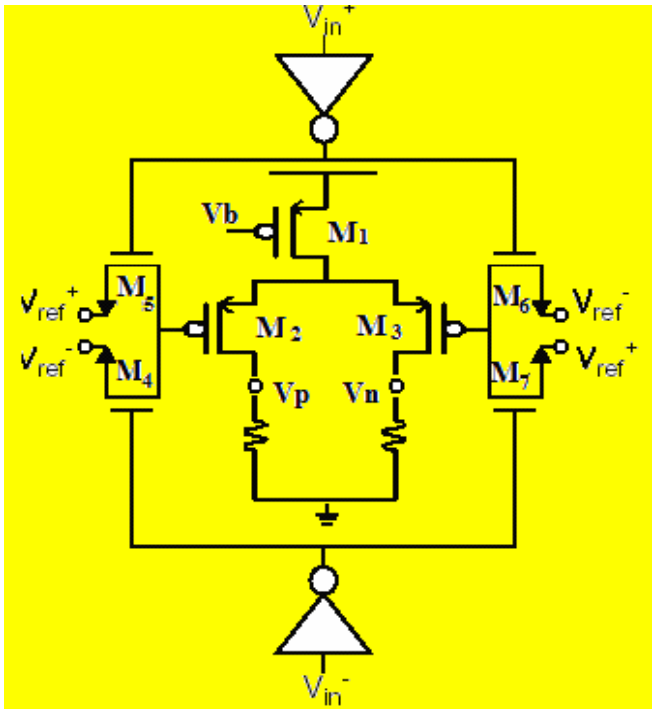


Fig. 4.28 Output buffer

4.7. Layout and prototype

An analog to digital converter prototype was designed, laid out, and fabricated in a 0.4 μ SiGeBiCMOS technology. The analog-to-digital converter regarding the desired high-resolution is highly sensitive to process variations so that it demands much more layout precautions to minimize interference such as crosstalk, mismatching, noise, etc. Therefore, it is necessary to use the complicated and time consuming full-custom layout for this high-precision analog layout. The layout strategy is summarized as follows:

A. Matching layout

Matching layout is important for analog circuits to achieve a high electrical performance. Matching of transistors and routing are also important for digital circuits because of skew in memories. In order to layout matching circuits to avoid mismatching problems, the following rules of matching are complied for layout of a ratio of two devices (i.e., transistors, capacitors or resistors) [Joh97]:

- Prefer to use parallel/series connection with the unit cells rather than varying W or L to take out ΔW and ΔL effects.
- Prefer to place relative devices by using common-centroid or nearly common-centroid layout to take out oxide and doping gradients.
- Prefer to use dummy devices at the ends of the row to improve matching by making the edge effects similar [McN94] [McC81] [Shy84].
- For creating current sources from a nominal current, the override-voltage V_{gs}-V_T should be kept above 200mV for a good matching! Since V_T mismatch has a larger effect at low bias levels.
- For creating current sources from a nominal current, the current should not be too big for a good matching! Since β mismatch dominates at high currents.
- Prefer to make clean and well balanced routing

B. Noise Coupling into Signals

Noise can couple into signals through neighboring wires and substrate, where the performance can be dramatically degraded. In order to avoid the performance degradation, the following rules of matching are complied:

- With full-differential design, it is important to minimize the noise coupling, since any noise that appears on both components of a differential signal as a common-mode signal can be compensated by the common-mode rejection of the subsequent circuits
- Physical separation of noisy signals from sensitive ones reduces the direct capacitive coupling, but does not help with substrate coupling in epi-silicon. Well and diffusion guard rings do not help that much, because they only penetrate the first few microns of the substrate, which is hundreds of microns deep. Shielding is an useful technique. As shown in Fig.4.29, shielding signal with whatever gnd or vdd, can keep the signal away from the noise sources.

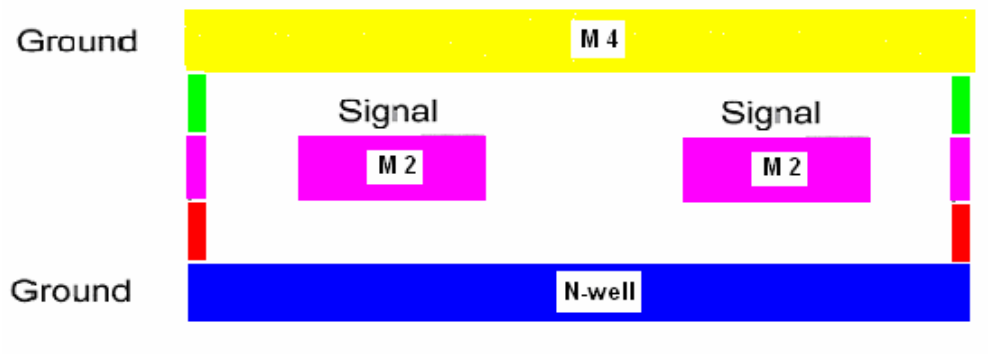


Fig.4.29 illustration of shielding for the signal path

- One helpful trick is to put a floating well under clock busses. The well provides some measure of isolation by placing a series capacitor in the noise path. Since both the well and the substrate are lightly doped, the capacitance per unit area is low. However, the paracsitic capacitance accumulates along the wire being so much well, that the total amount of capacitance is still somewhat large.
- The separation of digital and analog blocks at considerable distance helps to attenuate the switching noise injected to analog devices.

- When a signal crosses one of the differential signals, it is better to make it cross the other one too. Always route differential signals together. Generally, it is desirable to use a high metal layer to carry signals to reduce the noise coupling and to minimize the loading.

C. Noise coupling in biases

Noise can also couple into bias nodes through neighboring wires. An epitaxial substrate can be viewed as a single node connecting all transistors to each other. Therefore, even if there are no wires to carry the noise, the noise can go through the substrate from one end of a chip to the other! In order to avoid the performance degradation, the following rules of matching are complied:

- For bias nodes, prefer to use decoupling capacitors to reduce the amplitude of noise coupling. Note that the decoupling capacitors have to been traded off between the recovery-speed and bounce amplitude. Low decoupling capacitor causes in fast recovery but big bounce; high capacitor causes in a small bounce but slow recovery.
- Separate analog and digital power supplies should be used, to reduce the amount of noise on the power supplies of sensitive circuits. Among them, analog power supply is employed in the analog blocks, digital power supply is used in the modulator digital blocks: clock phase generator, SR latches, 4-bit ROM, digital buffers, etc.
- Also, heavily bypassing the analog and digital supplies with capacitors is useful. Note that if the series resistance of the capacitors is too high, the benefits can be compensated at high frequencies.
- Ringing on the supplies is sure to be disastrous for most designs.

D. ESD protection and considerations

The technology's shallow junctions, thin gate oxides, small feature size and salicided implant regions, makes it highly susceptible to ESD induced damage. Pads with ESD protection are used for signals that are driving transistor gates (clk and amplifier bias

currents etc.); whereas no protections are used for differential input voltage and references of the modulator.The modulator digital outputs and the digital power supply also use pads with no ESD protection. Since no biasing is required for these pads, they have been placed outside the pad ring.

In spite of the limited effectiveness of these common strategies, they have been incorporated in the prototype of the 2(1b)-1-1-1(4b) dual-quantization Sigma-Delta modulator. The die photo of the prototype is shown in Fig. 4.30, which was designed in a 0.4 μm SiGeBiCMOS process provided by Freescale for a 3.3V power supply. The prototype occupies an area of 3.1μm X 3.1 μm (pads included) and has been packaged in a 44-pin ceramic quad flat pack.

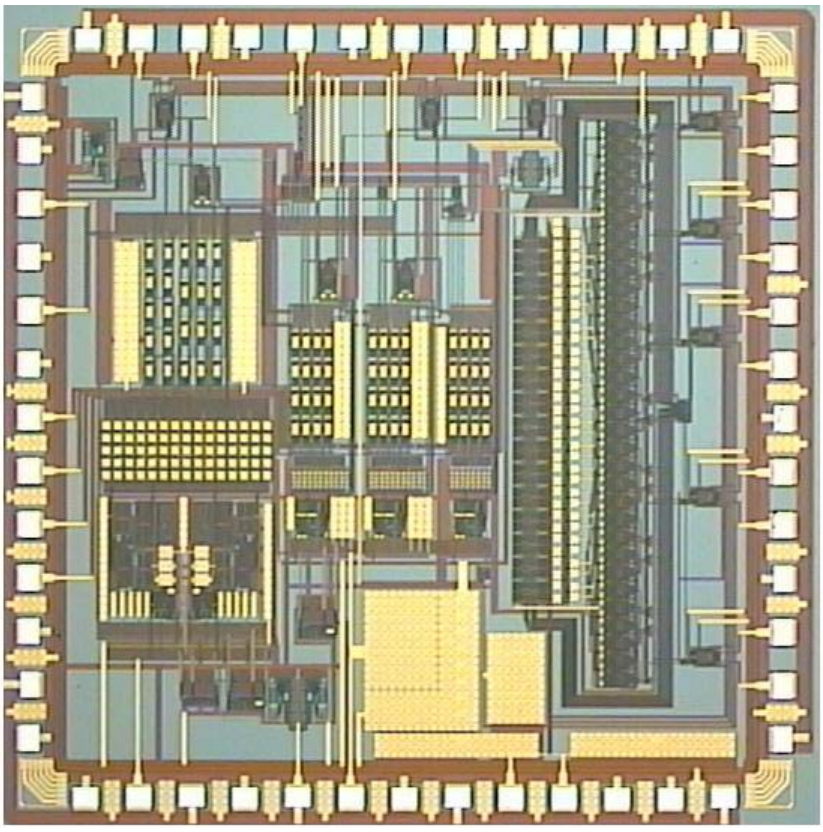


Fig. 4.30 Prototype of the Sigma-Delta modulator

4.8. Experimental simulation results

The software package used for the design is Design Framework-II from Cadence. The circuits are first described and simulated at schematic level, using Analog Artist and Spectre. After confirmation of the required performance, the layout for each block is drawn and compared with the schematic for errors. The digital blocks are described only at the schematic level. The operation is verified with digital simulation tool such as Verilog-XL. The layout for these blocks is then automatically generated by a Place-&-Route tool.

Modulator	Topology	2-1-1-1
	Dual-quantization	1bit/4bit
	Oversampling ratio	10
	Clock frequency	200 MHz
	Supply voltage	3.3 V
	Clock jiter	0.5 ps
Front-End Integrator	Sampling capacitor	2.5 pF
	Unit capacitor	0.125 pF
	Capacitor standard deviation	0.12%
	Bottom paracitic capacitor	20%
Amplifier	Open-loop DC-gain	80 dB
	Gain-bandwidth product (2.5pF)	850 MHz
	Slew-rate (2,5 pF)	800V/uS
	Differental output swing	+-2V
	DC-gain non-linearity	20%
Comparator	Hysteresis	20 mV
	Offset	+-10mV
	Resolution time	1ns
AD/DA	Resolution	4 bit
	DAC INL	0.4%FS

TABLE 4.4. Modulator design specifications

Additionlly, the proposed cascade 2(1b) -1(1b)-1(1b)-1(4b) Sigma-Delta modulator was simulated with Matlab to evaluate its dynamic performance. Main considerations made for the circuit-level modulator specifications are summarized in Table 4.4. Five groups of specifications are enclosed: modulator, front-end integrator, amplifier, comparator, and A/D/A converter. In this procedure, the worst-case performance has been evaluated in the

presence of variations in the process (for instance, changes in device parameters), temperature, and supply.

In the following simulations, a 1.5 MHz sine-wave signal with amplitude of -5dBFS was applied, the sample frequency was 200 MHz for a targeted 10 MHz bandwidth. The output spectra were computed with a 16384 point FFT.

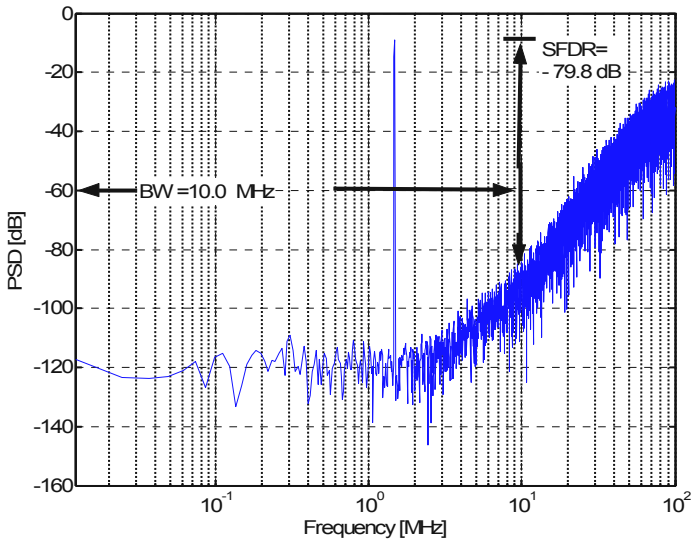


Fig. 4.31 The output spectra of the proposed 2-1-1-1(4b) with circuit non-idealities

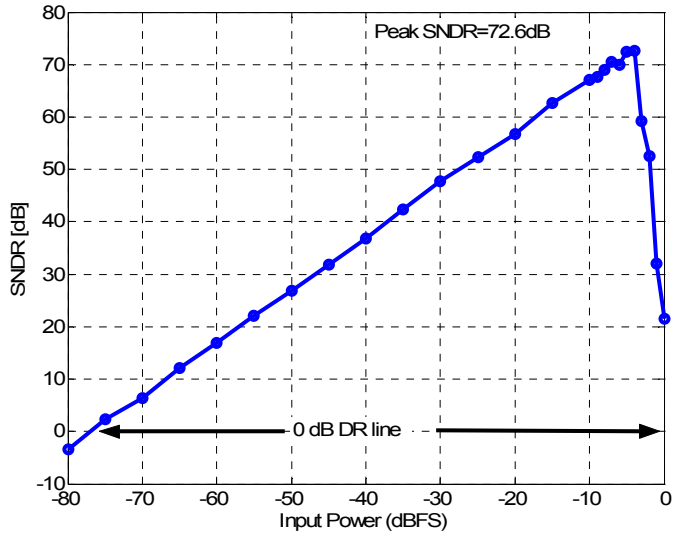


Fig. 4.32 SNDRvs input power obtained through behavioral simulation

The resulting output signal spectrum is shown in Fig. 4.31. The proposed modulator achieves 71.2 dB SNDR, 79.8 dB peak SFDR. Fig.4.32 shows the SNDR vs. the input level obtained through behavioral simulation. According to the behavioral simulation result, the modulator achieves approximately peak SNDR 72.6dB with the input amplitude of -4 dBFS. The respective dynamic range is 78.3dB (13bit).At this speed, the total power dissipation at 200-MHz clock rate is 140 mW from a 3.3 V supply, from which 95.3 mW (70%) are consumed in the analog blocks, 11.2 mW (6%) in the digital section and (24%) in the digital output buffers. The corresponding value of the figures-of-merit defined in Equations (1.1) and (1.2), respectively, approximates to $7*10^{11}$ Hz/W.

4.9 Conclusions and summary

Since the performance targeted for the Sigma-Deltąmodulator here was over 13-bit effective resolution at the clock rate of 200MHz, the oversampling ratio should be as small as possible. It suggested the use of high-order cascade multi-bit Sigma-Deltąmodulator topologies, because the cascade high-order shaping could be obtained without significant loss of performance.

This chapter has presented the design of the prototype chip in a 0.4 um BiCMOS. The analytical expressions for the requirements on the circuit-specifications have been derived. It shows that that the performance of the proposed Sigma-Delta modulator is limited by the two amplifiers in the first stage, where not only high DC gain, but also high gain-bandwidth-product and slew-rate were needed. A folded cascade opamp structure with CMOS and bipolar transistors has been proposed to achieve the desired performance. Also, the using BiCMOS process has met with the requirement of the accurate reference voltage in band gap. The other circuits have been designed in CMOS to save the power consumption. The electrical simulation result shows that the proposed converter achieves a dynamic range is of 78.3dB (13bit) with an oversampling ratio of only 10 at 10 MHz Nyquist output rate. At this speed, the total power dissipation is 140 mW from a 3.3 V. As shown in Fig. 1.1 the overall features of the prototype ADC are clearly better than what can be obtained in cascade Sigma-Delta modulators [Fel98] [Fuj00] [Vle01] [Rio02]

[Rio04a] [Jin04], and compare well with the state of the art, in spite of the slight increase in power dissipation due to the desired high-performance analog circuit blocks in comparison with the high-order single-loop modulator reported in [Bal04].

Chapter 5 High-Performance Wideband Cascade Sigma-Delta Modulators

5.1 Introduction

In the future HD-televisons and communication systems, high dynamic-range and high conversion rate ADCs are endlessly desired to meet with the evolution of the high-performance, low-cost and high-integration systems. We have seen that the proposed BiCMOS integrator has superior settling behavior over regular switched-capacitor integrators. However, it consumes much more power in order to implement the opamps with high DC-gain and high-gain-bandwidth-product in the BiCMOS process. With the repect to lower cost, smaller chip size, and lower power dissipation, the development of high performance ADCs in the mainstream CMOS prosess is expected. However, in the modern low-cost CMOS technology, due to poor analog performances, the implementation of high performance analog building bocks, especially the high DC-gain and high bandwidth opamp is difficult to be achieved. Therefore, the high conversion rate associated with achieving a high resolution by using poor analog perforemance, digital-oriented submicron CMOS process is a critical challenge in the ADC design. In this chapter, two Sigma-delta modulator architectures that potentially facilitate the implementation of high-resolution wideband Sigma-Delta ADCs in digital oriented deep-submicron CMOS technologies will be analyzed and discussed.

5.2 Background

In this section, I will introduce and discuss the low distortion Sigma-Delta modulator architecture with STF=1 [Ste99] [Sil01], the single-stage multibit Sigma-Delta modulator architecture with a high-order finite-impulse-response NTF [Ham04], and several linearization techniques for DACs. These techniques are potentially served for the design of the high-speed high resolution Sigma-Delta modulators in sub-micron CMOS processes.

5.2.1 Low-distortion Sigma-Delta topologies

As described in section 3.4, if the desired signals are processed by integrators based on nonlinear opamps, distortion signals will be introduced at integrator outputs. Although inherent high-pass filtering function of the modulator attenuates these nonlinear effects, but it is not sufficient for wideband signals when OSR is low.

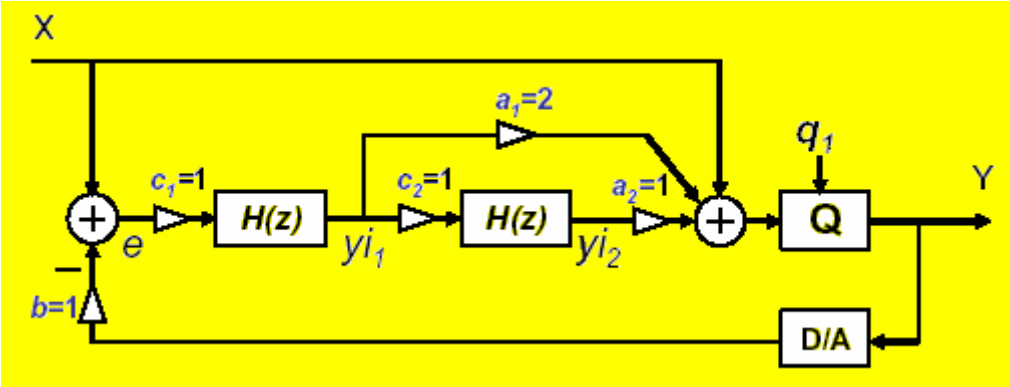


Fig. 5.1 The 2nd-order low-distortion Sigma-Delta modulator

Figure 5.1 shows the low distortion second-order Sigma-Delta modulator topology proposed in [Ste99] [Sil01]. The loop filter H(z) is an integrator, whose transfer function in the z-domain is

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{5.2.1}$$

In this way, it is obtained:

$$\begin{aligned} E(z) &= X(z) - Y(z) \\ Yi_1(z) &= \big(X(z) - Y(z)\big)H(z) \\ Yi_2(z) &= Yi_1(z)H(z) = \big(X(z) - Y(z)\big)H^2(z) \\ Y(z) &= X(z) + 2Yi_1(z) + Yi_2(z) + Q_1(z) \\ &= X(z) + 2\big(X(z) - Y(z)\big)H(z) + \big(X(z) - Y(z)\big)H^2(z) + Q(z) \end{aligned} \tag{5.2.2}$$

Reforming the equation 5.2.2, the modulator output yields

$$\begin{aligned} Y(z) &= X(z)STF(z) + Q(z)NTF \\ &= X(z)\frac{1 + 2H(z) + H^2(z)}{1 + 2H(z) + H^2(z)} + Q(z)\frac{1}{1 + 2H(z) + H^2(z)}. \end{aligned} \tag{5.2.3}$$

Therefore, the signal transfer function is:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{1 + 2H(z) + H^2(z)}{1 + 2H(z) + H^2(z)} = 1 \qquad 5.2.4$$

and the noise transfer function is :

$$NTF(z) = \frac{Y(z)}{Q(z)} = \frac{1}{1 + 2H(z) + H^2(z)} = \frac{1}{1 + 2\dfrac{z^{-1}}{1 - z^{-1}} + \left(\dfrac{z^{-1}}{1 - z^{-1}}\right)^2} = \left(1 - z^{-1}\right)^2 \qquad 5.2.5$$

The noise transfer function is the same as for a conventional Sigma-Delta modulator, but not the signal transfer function, where STF is equal to 1. Since no input signal is processed by the integrators, no input signal harmonics due to the non-linear opamp can be generated for this kind of design [Ben93], [Ste99] [Sil01].

In order to intuitively compare the performance differences between the traditional and the low-distortion second order Sigma-Delta modulator topology, corresponding spectra simulations were made. Figure 5.2 shows the simulated spectra of the conventional topology; Figure 5.3 shows the spectra of the low-distortion topology. To keep the comparison fair, the coefficients in the low-distortion topology were adjusted so that its integrator outputs have voltage swings similar to those of the conventional topology, therefore using similar nonlinear ranges. The opamps with nonlinearity are assumed as in section 3.5. Unlike the conventional topology, the low-distortion topology does not show any input signal components at the integrator outputs, y_{i1} and y_{i2}. It shows only shaped quantization noise. Consequently, the spectra of the integrator outputs y_{i1} y_{i2} and output y contain no harmonics [Sil01].

The fact that no signal is processed by the integrators means that the output swing of the opamps is not limited by the input signal amplitude. Therefore, the maximum input amplitude can now be as large as the output saturation voltage. In contrast, traditional Sigma-Delta modulators whose signal path goes through H(z) are typically designed for a maximum input amplitude between 0.25-0.5 of the output saturation voltage to avoid saturating the opamps [Nor96]. Consequently, the integrator coefficients c_1 and c_2 - implemented as sampling-to-integrating capacitor ratios (C_S/C_I) - can be as large as 1 that is larger than those of a conventional topology. The maximized input amplitude allows minimizing the input sampling capacitor, which is constrained by kT/C noise

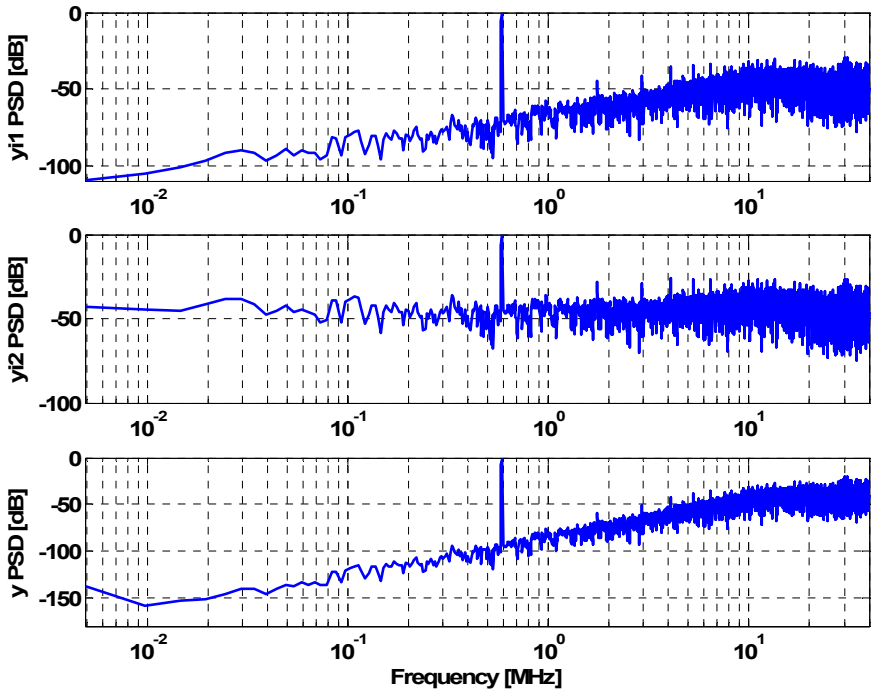


Fig. 5.2 Spectra of the 2nd-order low-distortion Sigma-Delta modulator

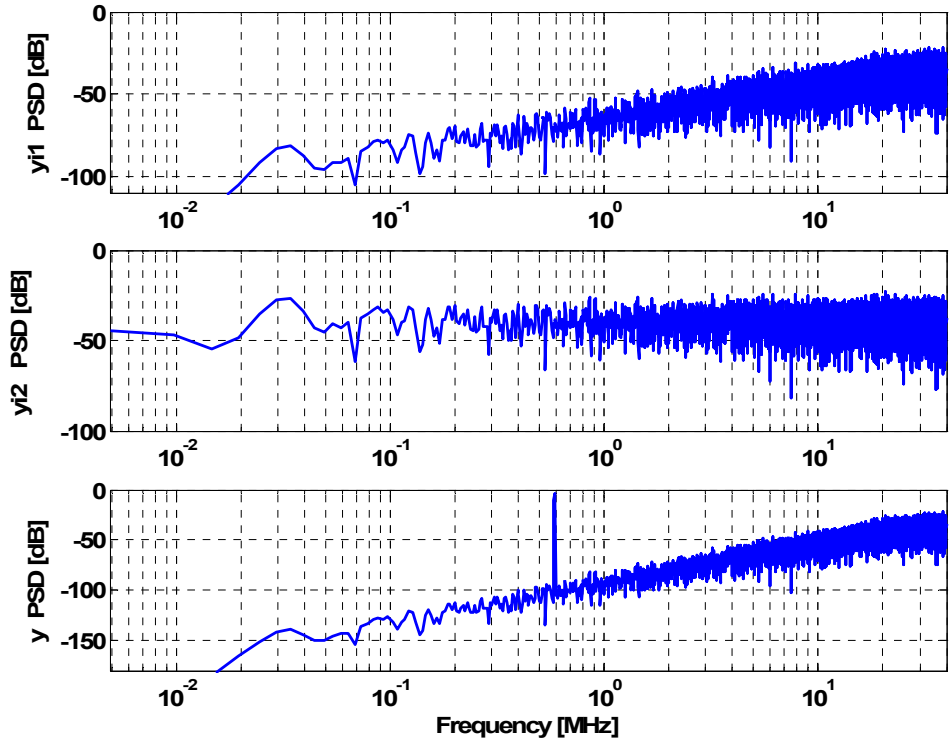


Fig. 5.3 Spectra of the 2nd-order low-distortion Sigma-Delta modulator

considerations in each integrator; and the corresponding integrating capacitor can be as small as the sampling capacitor. Hence, the total capacitive load is low, which is

particularly effective in maximizing integrator bandwidth.

5.2.2 High-order Sigma-Delta topologies with improved FIR NTFs

The theoretical achievable signal-to-quantization noise ratios of Sigma-Delta modulators with pure FIR filter characteristics can be increased by replacing two zeros at dc with one pair of complex-conjugate zeros in the NTF. The corresponding NTF for L≥2 becomes [Ham03]:

$$NTF(z) = (1 - z^{-1})^{L-2}(1 - \delta z^{-1} + z^{-2}) \qquad 5.2.6$$

where $\delta=2\cos(2(f_0/f_s))$, f_0 and fs are the notch frequency and the sampling frequency, respectively. The optimal placement of the notch frequency is at approximately:

$$f_0 = \sqrt{(2L-3)/(2L-1)}\, f_{BW} \qquad 5.2.7$$

This corresponds to a factor of $(L-0.5)^2$ improvement in SQNR compared to the case, in which all zeros of the NTF are at DC. (For example, with $L=4$, $f_0=0.845f_{BW}$ results in an 11-dB SQNR improvement relative to $f_0=0$ [Ham04]. This technique can be realized by using a much simpler circuit implementation as shown in Fig. 5.4, where $\int \equiv 1/(1-z^{-1})$. The feedforward coefficients a_i (i = 3; . . . ; L) needed to realize the FIR NTF in (5.2.6) are given in Table 5.1.

L	a3	a4	a5
3	δ+1		
4	2 and 2z-1	δ+2	
5	5	5	δ+3

TABLE 5.1. FEEDFORWARD COEFFICIENTS a_i (i = 3;...; L) NEEDED TO REALIZE THE LTH-ORDER (L ≥ 3) FIR NTF IN (Eq. 5.2.6) [Ham04].

For $L = 4$, path $a3$ consists of two parallel paths: a non-delaying path with coefficient 2 and a delaying path with coefficient $2z^{-1}$. In order to verify that the generic Sigma-Delta modulator that realizes the improved FIR NTF, an analysis on the third-order Sigma-Delta modulator, whose schematic is shown in Figure 5.5, is performed as follows:

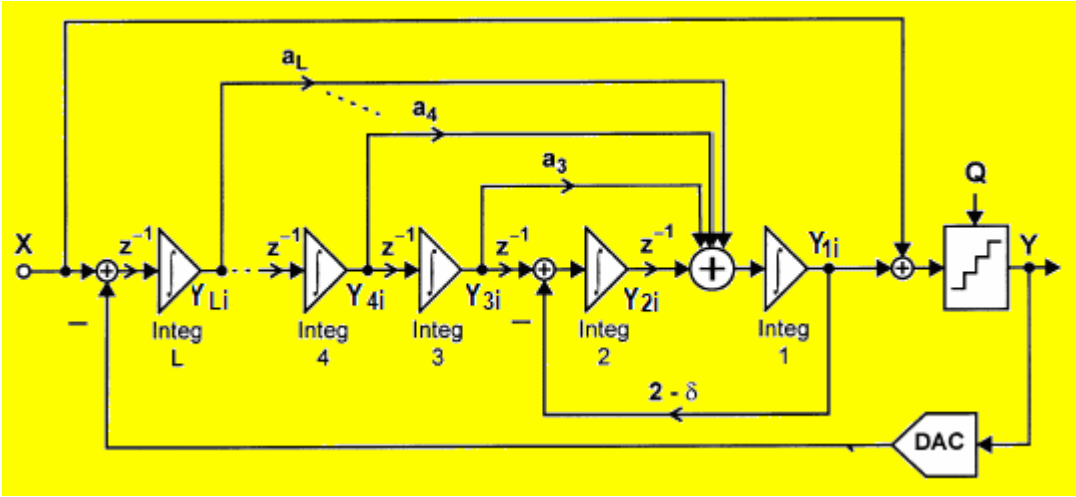


Fig. 5.4. Sigma-Delta modulator of order L (L ≥3) with improved FIR NTF

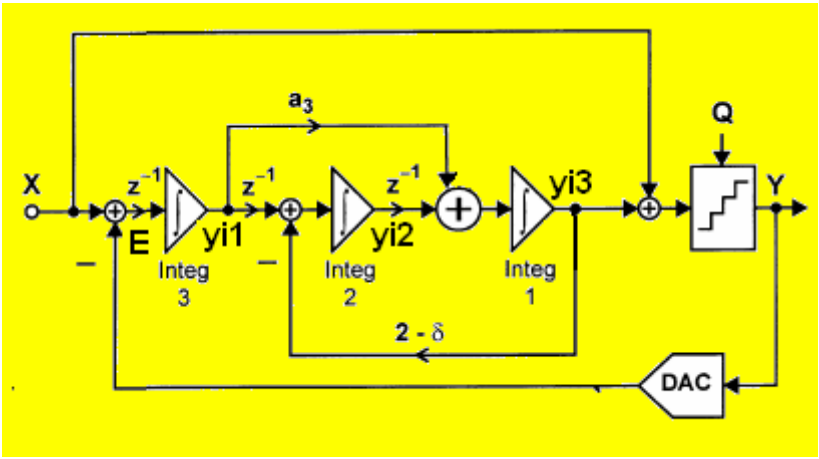


Figure 5.5. The corresponding third-order Sigma-Delta modulator

Firstly, the input of the first integrator is:

$$E(z) = X(z) - Y(z) \qquad 5.2.8$$

the respective outputs of the integrators are:

$$Y_{i1}(z) = \big(X(z) - Y(z)\big)\frac{z^{-1}}{1-z^{-1}} \qquad 5.2.9$$

$$\begin{aligned} Y_{i2}(z) &= \big(Y_{i1}(z)z^{-1} - (2-\delta)Y_{i3}(z)\big)\frac{1}{1-z^{-1}} \\ &= \left(\big(X(z) - Y(z)\big)\frac{z^{-1}}{1-z^{-1}}z^{-1} - (2-\delta)Y_{i3}(z)\right)\frac{1}{1-z^{-1}} \end{aligned} \qquad 5.2.10$$

$$Y_{i3}(z) = \big(Y_{i2}(z)z^{-1} + a_3 Y_{i1}(z)\big)\frac{1}{1-z^{-1}}$$

$$= \left(\left((X(z) - Y(z)) \frac{z^{-1}}{1 - z^{-1}} z^{-1} - (2 - \delta) Y_{i3}(z) \right) \frac{z^{-1}}{1 - z^{-1}} + (\delta + 1)(X(z) - Y(z)) \frac{z^{-1}}{1 - z^{-1}} \right) \frac{1}{1 - z^{-1}}$$

5.2.11

Rreforming the Eq. 5.2.11, it is obtained:

$$Y_{i3}(z) \left(\frac{1 - \delta z^{-1} + z^{-2}}{1 - z^{-1}} \frac{1}{1 - z^{-1}} \right)$$

$$= (X(z) - Y(z)) \left(\frac{z^{-1}}{1 - z^{-1}} \right)^3 + (\delta + 1)(X(z) - Y(z)) \frac{z^{-1}}{1 - z^{-1}} \frac{1}{1 - z^{-1}}$$

$$= (X(z) - Y(z)) \left(\frac{z^{-1}}{1 - z^{-1}} \right)^3 + (\delta + 1)(X(z) - Y(z)) \frac{z^{-1}(1 - z^{-1})}{(1 - z^{-1})^3}$$

$$= (X(z) - Y(z)) \frac{1}{(1 - z^{-1})^3} \left(z^{-3} + (\delta + 1) z^{-1} - (\delta + 1) z^{-2} \right)$$

$$Y_{i3}(z) = (X(z) - Y(z)) \frac{\left(z^{-3} + (\delta + 1) z^{-1} - (\delta + 1) z^{-2} \right)}{(1 - z^{-1})(1 - \delta z^{-1} + z^{-2})} \qquad 5.2.12$$

The output of the modulator is:

$$Y(z) = X(z) + Yi_3(z) + Q_1(z) = X(z) + (X(z) - Y(z)) \frac{\left(z^{-3} + (\delta + 1) z^{-1} - (\delta + 1) z^{-2} \right)}{(1 - z^{-1})(1 - \delta z^{-1} + z^{-2})} + Q(z)$$

$$Y(z) \left(1 + \frac{\left(z^{-3} + (\delta + 1) z^{-1} - (\delta + 1) z^{-2} \right)}{(1 - z^{-1})(1 - \delta z^{-1} + z^{-2})} \right) = X(z) \left(1 + \frac{\left(z^{-3} + (\delta + 1) z^{-1} - (\delta + 1) z^{-2} \right)}{(1 - z^{-1})(1 - \delta z^{-1} + z^{-2})} \right) + Q(z)$$

The modulator output yields

$$Y(z) = X(z) + Q(z) \frac{1}{\left(1 + \frac{\left(z^{-3} + (\delta + 1) z^{-1} - (\delta + 1) z^{-2} \right)}{(1 - z^{-1})(1 - \delta z^{-1} + z^{-2})} \right)}$$

$$= X(z) + Q(z) \frac{(1 - z^{-1})(1 - \delta z^{-1} + z^{-2})}{(1 - z^{-1})(1 - \delta z^{-1} + z^{-2}) + \left(z^{-3} + (\delta + 1) z^{-1} - (\delta + 1) z^{-2} \right)}$$

$$= X(z) + Q(z) \frac{(1 - z^{-1})(1 - \delta z^{-1} + z^{-2})}{1 - \delta z^{-1} + z^{-2} - z^{-1} + \delta z^{-2} - z^{-3} + z^{-3} + (\delta + 1) z^{-1} - (1 + \delta) z^{-2}}$$

$$= X(z) + Q(z)(1 - z^{-1})(1 - \delta z^{-1} + z^{-2})$$

.

5.2.13

since $Y(z) = X(z) STF(z) + Q(z) NTF$

Therefore, the signal transfer function is:

$$STF(z) = \frac{Y(z)}{X(z)} = 1 \qquad 5.2.14$$

and the noise transfer function is :

$$NTF\ (z) = \frac{Y(z)}{Q(z)} = (1 - z^{-1})(1 - \delta z^{-1} + z^{-2}) \qquad 5.2.15$$

Hence, as expected, this structure realizes a Sigm-Delta modulator with an STF=1, at the same time, it realizes a single-stage Sigm-Delta modulator with a high-order finite-impulse-response NTF in Eq. 5.2.6 with L=3.

Figure 5.6 shows the spectrum of the 3rd-order low-distortion topology with the improved NTF. Unlike the conventional topologies, this topology demonstrates higher attenuation of the quantization noise at the in-band high-frequencies due to the deep notch. The SQNR is improved about 6 dB in comparison with the theoretical 3rd-order modulator with all zeros at DC [Ham04]. Indeed, the key advantages of the topology include: higher signal-to-quantization-noise ratios at low OSRs, decreased circuit complexity, improved robustness to modulator coefficient variations, reduced sensitivity to integrator nonlinearities, and reduced power dissipation [Ham04].

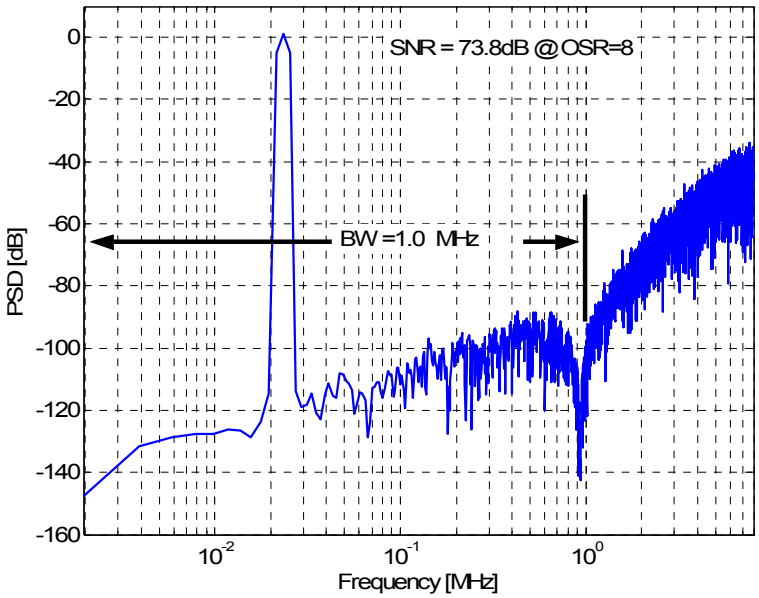


Fig. 5.6 Spectrum of the 3rd-order low-distortion Sigma-Delta modulator with improved NTF

In order to preserve the stability of the Sigma-delta modulator in an actual implementation, it is necessary to ensure that the peak outputs of the integrators are within the boundaries dictated by the opamp saturation voltages (i.e., perform dynamic-range scaling) and the multi-bit quanzizer is not overloaded at any time. With *STF=1*, the out-of-band spectral components are reduced due to the lack of input signal in the integrators of the loop-filter, therefore the stability of the Sigma-Delta modulator is improved. If the quantizer overload

ratio A_{OL} is defined as the ratio between the maximum amplitude of the input sine-wave signal and the quantizer's reference voltage (full-scale range/2), a sufficient condition to guarantee that the quantizer will never be overload, [Ken88] [Ken93], can be stated as

$$A_{OL} \le 1 - \frac{\|ntf\|_1 - 2}{2^B - 1} \qquad 5.2.16$$

where B is the bit number of the quantizer, $\|ntf\|_1$ is the 1-norm of the impulse sequence ntf(n) for the noise transfer function NTF(z) . For the L^{th}-order FIR NTF in Eq. 5.2.6 it exists

$$\|ntf\|_1 \equiv \sum_{n=0}^{\infty} |ntf(n)| = (2+\delta)2^{L-2} \qquad 5.2.17$$

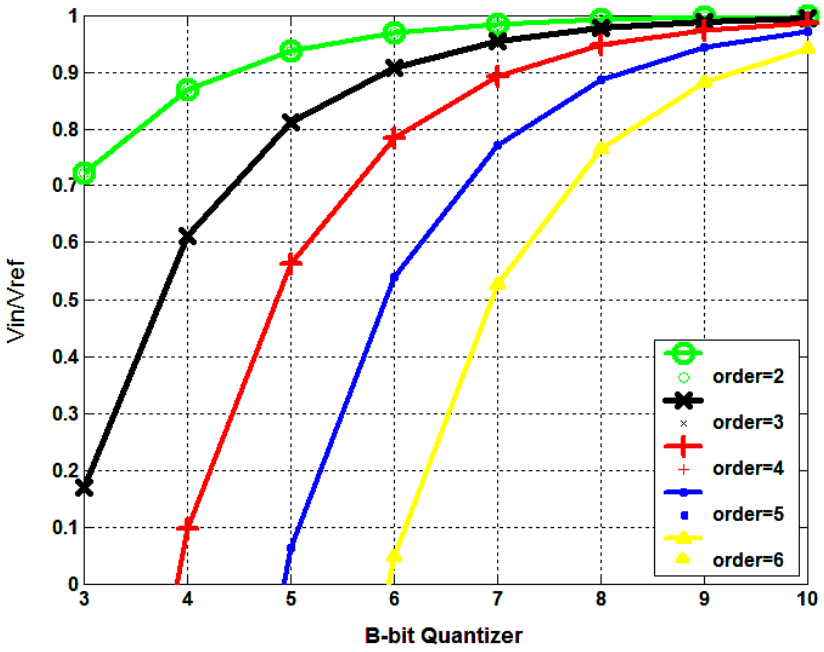


Fig. 5.7. Stable boundary under consideration of the input amplitude and the number of quantization bits for various orders with improved FIR NTF

According to the sufficient stability condition, the stable regions (under each boundary) are illustrated in Fig.5.7 for various *L*th-order ΣΔ modulators, where the maximum amplitude ratio V_{in}/V_{ref} between the input signal V_{in} and the quantizer's reference voltage V_{ref}, and the number of quantization bits were incorporated together with respect to stability. For the order higher than the third, extreme large numbers of the quantization bits are required to achieve reasonable input amplitude in a stable system. For example, a 5th-order this type

Sigma-Delta modulator needs a 6-bit internal quantizer to avoid that the ratio V_{in}/V_{ref} gets too small (<0.5).[Yin04]

5.2.3 Linearization techniques on multibit DAC

The improvement of SQNR by means of increasing the loop-order diminishes significantly as the OSR is reduced. In contrast, the effectiveness of increasing the number of quantization bits is independent of the OSR. Other advantages of multibit quantization include enhanced Sigma-Delta stability as well as relaxed slew-rate and settling requirement on opamps of the loop-filter integrators. However, the linearity of a multi-bit Sigma-Delta is limited by its multi-bit feedback D/A converter (DAC), because errors due to nonidealities in the feedback DAC add directly to the input signal. Therefore, the errors are not shaped by the loop and linearization techniques are required to correct for the mismatch errors in the DAC elements. Rather than using special fabrication processes or laser trimmed components to improve the DAC element matching, two signal-processing strategies have been developed to enhance the linearity of multibit modulators due to DAC element mismatch: 1) calibration/correction using analog [Groed89], [Moo99], digital [Pet00], or mixed-mode [Kis01] schemes and 2) dynamic element matching (DEM) [Sch97], [Welz01]. A combination of DEM and digital correction has also been proposed in [Wan01] and [Wan02].

Background calibration schemes are more expensive to implement in terms of system design complexity, hardware requirement, and power consumption in comparison with DEM techniques. DEM techniques have been proven very useful in improving the linearity of multi-bit D/A converter in Sigma-Delta modulators. It averages out DAC errors dynamically by properly choosing elements in the DAC. Various algorithms have been proposed. The conventional approach is random averaging (RNA) [Carl89], [Fat93], which randomly shuffles the DAC elements sequence and converts DAC error into a white noise. But this approach degrades signal-to-noise ratio (SNR). Individual level averaging [Che95] has firstly been proposed as a way of noise-shaping the noise resulting from distortions due to element mismatch. Data weighted averaging (DWA) [Bai95] and data directed

scrambling [Kwa96], which have the noise shaping characteristics, are very useful and efficient in shaping DAC errors because they take advantage of the oversampling feature which already exists in the modulator.

In high-speed modulators, the complexity of the DEM algorithm becomes a concern because the delay introduced by the DEM selection logic in the feedback loop can limit the maximum achievable clock speed of the modulator. In this aspect, DWA [Bai95] is a highly practical DEM technique to implement, especially when the number of DAC elements is large.

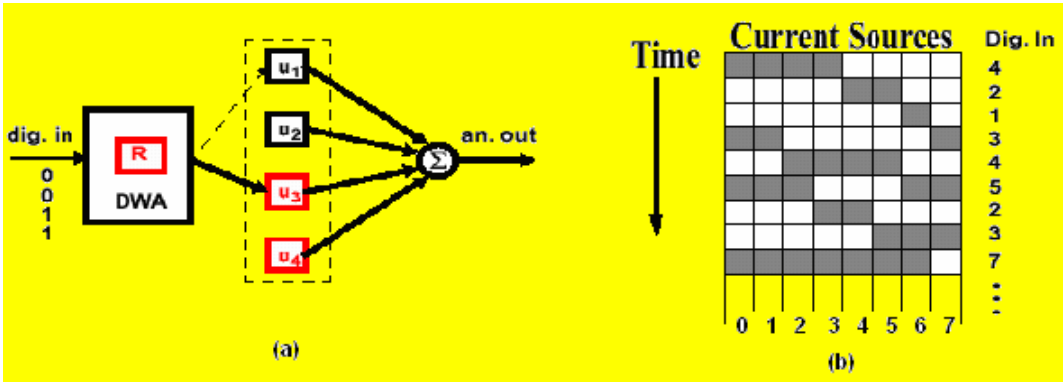


Fig. 5.8. Illustration of the rotational element-selection process of DWA

The basic DWA for a 3-bit DAC is illustrated in Fig. 5.8(a) (b). The block diagram Fig. 5.8 (a) shows the needed hardware: an integrator is used to create pointer R that shows the point of first unused unit element. The code is converted to thermometer code, and a logarithmic shifter is used to move the origin of the thermometer code to the new position. The algorithm cycles through the DAC elements by sequentially selecting the elements based upon the input data. Fig. 5.8 (b) shows the DAC starting at element 0. The initial input of 4 will select elements 0, 1, 2 and 3. The second input 2 will select elements 4 and 5. The next input will beginn with the next available unused element; sequentially select the DAC unit elements from the DAC array. The cycling through the elements ensures that all the elements are used once before an identical single element is repeated, thus summing their errors (deviations from the average current) to zero as quickly as possible.

Through such rotational element-selection process, DWA achieves first-order high-pass

shaping of the DAC mismatch errors [Sch97] [Nys96]. However, when a periodic signal is applied to the DAC, making a complete rotation (with the index pointer returning to its exact starting point) every M/r clock cycles, where M is the DAC-elements, and r is the greatest common divisor of the Y_{DAC} and M. As a result, the DAC mismatch noise will be a periodic sequence of period MT_S/r (where $T_S=1/f_S$), and its power spectrum will take the form of tones at frequencies [Che99] [Ham04]

$$f_{tone} = k\frac{r}{M}f_s \qquad k = 1,2,... \tag{5.2.18}$$

Thus, in general, for an M-element DAC, the lowest tone frequency can be at f_s/M with DWA. If the maximum possible input frequency to the modulator is $f_{BW}=f_s/(2OSR)$, then the constraint that the k^{th} harmonic of the modulator's input signal does not fall back into the signal bandwidth after being modulated by the DWA tone at f_s/M requires that [Che98]

$$\frac{f_s}{M} - kf_{BW} > f_{BW} \Leftrightarrow OSR > \left(\frac{1+k}{2}\right)M \tag{5.2.19}$$

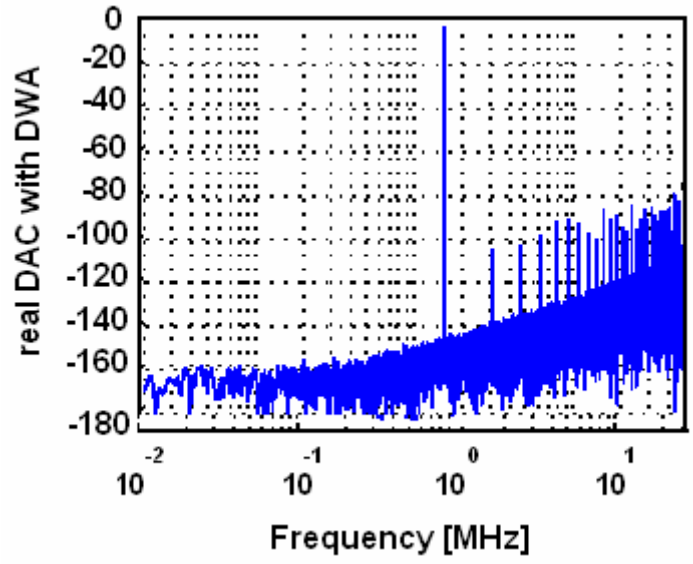


Fig. 5.9. Illustration of the tones behavior of DWA

As shown in Fig. 5.9, on the oneside, DWA technique produces harmonic tones that degrade the SFDR, on the other side, the harmonic distortion has been turned into white noise, part of the noise energy falls inside the passband, and the overall SNR is reduced. The tone problem of DWA can preclude using DWA at a low OSR, especially when the number of DAC elements (quantization bits) is large [Bai95], [Che98].

A number of techniques have been proposed to reduce the tone behavior of DWA, by means of using an extra modification to DWA to break the cyclic nature of the element-selection process. These techniques can be classified into four categories: 1) Dithering [Bai95]; 2) Incremental DWA (IDWA) [Kuo02], [Che99]; 3) DWA with multiple data-directed index pointers, as in Bi-Directional DWA (Bi-DWA) [Fuj00] and Partitioned DWA (P-DWA) [Vle01]; 4) DWA with randomized index pointer, as in Rotated DWA (RDWA) [Mil03], [Rad00], Randomized DWA (RnDWA) [Par03], [Vad00], and Pseudo DWA [Ham04], [Ham02a].

DAC Linearization	Peak SNDR (dB)
Ideal DAC	92.8
No DWA	60.4
DWA [Bai95]	90.9
Pseudo DWA [Ham02a]	89.9
P- DWA [Ham02a]	89.7
Bi-DAW [Fuj00]	85.8
RnDWA [Par03]	83.2
IDWA [Kuo02]	82.0

TABLE 5.2 ACHIEVABLE PEAK SNDR USING VARIOUS DWA SCHEMES IN A THIRD-ORDER SIGMA-DELTA MODULATOR WITH OSR = 16, B = 5 BITS, AND M= 31 ELEMENTS. A RANDOM DAC-ELEMENT MISMATCH OF 0.5% IS ASSUMED. (INPUT SIGNAL: -2 dBFS AT fs/2048)

A summary description of these techniques is presented in [Ham04]. Table 5.2 compares the peak SNDR when using the above techniques for DWA tone reduction.

Fig. 5.10 shows the maximum in-band tone relative to the average tone power [Ham04]. Compared to DWA, using Pseudo DWA,
P-DWA, and RnDWA (with an ideal implementation) achieve reductions of about 15, 16, and 18 dB in the maximum in-band tone, respectively. Note that, in general, the in-band DWA tones cannot completely eliminated by a modified DWA technique, to achieve a smooth DAC noise floor over all input signal levels, unless a perfectly random component is introduced in the DAC element-selection process (for example, in an ideal

implementation of a randomized DWA technique). However, assuming a 0.5% DAC-element mismatch is present in the ADC described above; behavioral simulations show that the largest in-band toner with P-DWA or Pseudo DWA is well below the level of the noise floor of the ADC. Thus, such in-band tone will not be visible in the ADC output spectrum and will not degrade its performance.

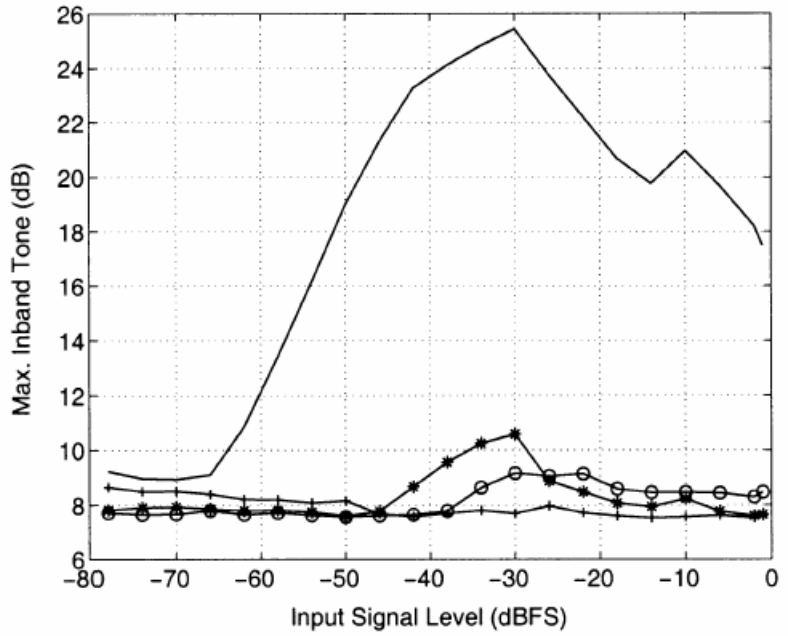


Fig. 5.10. Maximum in-band tone versus input signal levels when using: — DWA ; * Pseudo DWA; o P-DWA; + RnDWA with an ideal implementation [Ham04]

5.3 Proposed wideband Sigma-Delta modulators

5.3.1 Introduction

As desired signal conversion rate increases, integrator defective settling is becoming one of the bottlenecks in the present wideband SC Sigma-Delta modulator designs. The settling error in SC Sigma-Delta modulators is caused by GBW and SR of amplifiers [Med94]

In this section, two Sigma-Delta modulators are introduced. Firstly, a low distortion cascade multibit Sigma-Delta A/D modulator architecture is proposed to achieve better performances at low oversampling ratio. The modulator is based on the theoretical point of

view of the settling error due to finite gain-bandwidth product (GBW) and slew-rate (SR) of opamps in SC Sigma-Delta A/D modulators, as shown in section 3.4.3. The proposed architecture combines the merits of the cascaded Sigma-Delta modulator structure, the low distortion structure, and multibit quantization, and relaxes the GBW requirement of opamps as low as twice of the sampling frequency f_s, much lower than the 3-4-times f_S in other Sigma-Delta modulator implementations [Mar98][Rio00a][Rio00b]. Another advantage of the proposed modulator is that it is insensitive to circuit non-idealities. The second proposal is a low distortion cascade multibit Sigma-Delta A/D modulator architecture with improved NTF, which achieves extra high attenuation of the quantization noises at high frequencies by replacing two zeros at DC with one pair complex-conjugate ones. Therefore, the modulator architecture achieves high SQNR even better than theoretical value. Both proposed architectures significantly relax the circuit requirements; and reduce the power dissipation. As a result, it is very suitable for realizing high resolution broadband ADCs as well as for low-power design as IC technologies advance.

5.3.2 Low distortion cascade architecture

5.3.2.1 Proposed architecture

In section 3.4.3, it has been derived that the ratio between the SR and GBW of the opamps can be approximated to a constant by means of a single-pole opamp. With respect to saving power and maximizing the conversion rate, the most essential issue in the design of ADC's becomes to reduce the normalized GB requirment as much as possible, whereas the resolution of the converter is not deteriorated. It means, when the signal bandwidth is fixed, fs is also fixed, and the reduced requirement on the opamp GBW results in a smaller I_{BIAS}, and thus smaller power consumption; on the other hand, when the opamp GBW is fixed due to technology limitation, a higher fs can be used, resulting in extended signal bandwidth.

Based on the analysis of the settling behavior of SC integrators, a new alternative approach to realize ADC with wideband and wide-dynamic-range is proposed, in which the low-distortion multi-bit Sigma-Delta modulator concept [Sil01] is introduced into cascaded

Sigma-Delta modulators. The proposed generic architecture is shown in Fig.5.11, where g_{N1}, g_{N2}, g_{N3} are the interstage scaling factors in the n^{th} stage. With the consideration of physically achievable output swings, in combination of the behavior simulation and the statistical optimization, it is obtained:

$$g_{i1}=1 \; g_{i2}=1 \; g_{i1}=0.5 \qquad i=2\ldots.N-1$$

$$g_{N1}=1 \; g_{N2}=0.5 \; g_{N3}=1 \qquad 5.3.1$$

H(z) in the blocks denotes the integration function. Ideally, the quantization error from all stages except the last one of the cascade structure can be completely cancelled in the digital domain. Therefore, the output signal can be expressed as the combination of the delayed input signal and the $(N+1)^{th}$-order noise-shaped quantization noise (N is the number of cascaded stages), that is:

$$Y = X * z^{-(N-1)} + E_N (1 - z^{-1})^{N+1} \qquad 5.3.2$$

where E_N indicates the last-stage quantization error. Note that the proposed interstage scaling factors do not degrade the dynamic range as other cascade structures.

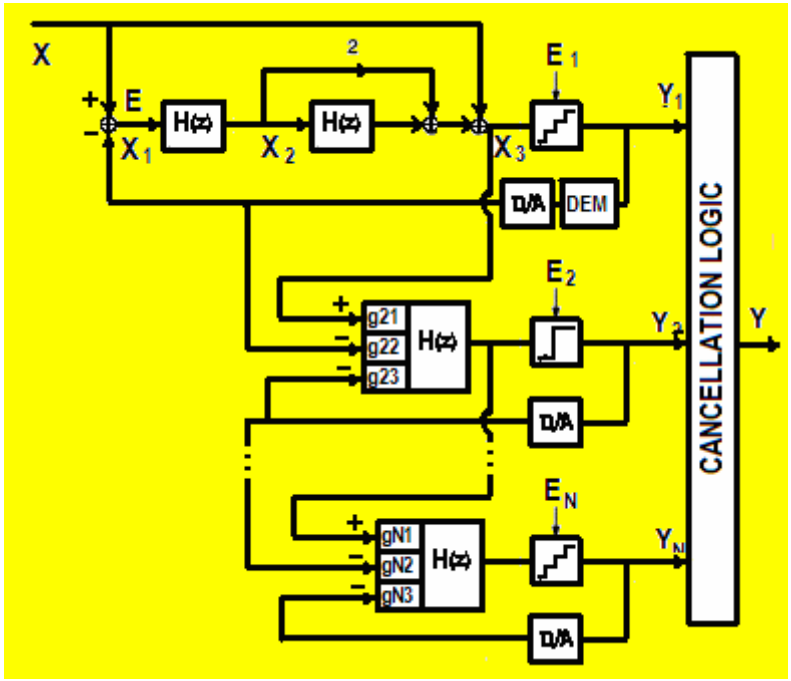


Fig.5.11. The proposed N-stage cascade Sigma-Delta modulator

The key advantage over other high-order cascades is that the individual input level of the integrators is considerably lower, even with high feedforward gain $C_S/C_I=1$ in the two

integrators of first stage, as only low-level quantization noise *E* is introduced in the integrator loops. To illustrate this, Fig. 5.12 shows the histogram of the integrator inputs (*X1* and *X2*) and quantizer input (*X3*) for an input signal with the amplitude of -3 dBFS.

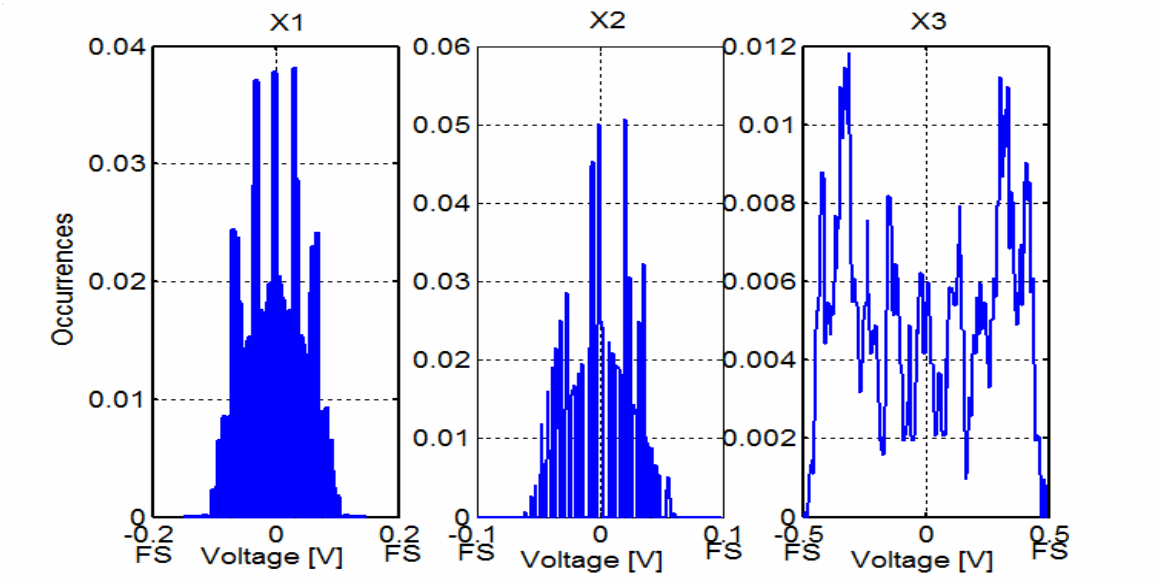
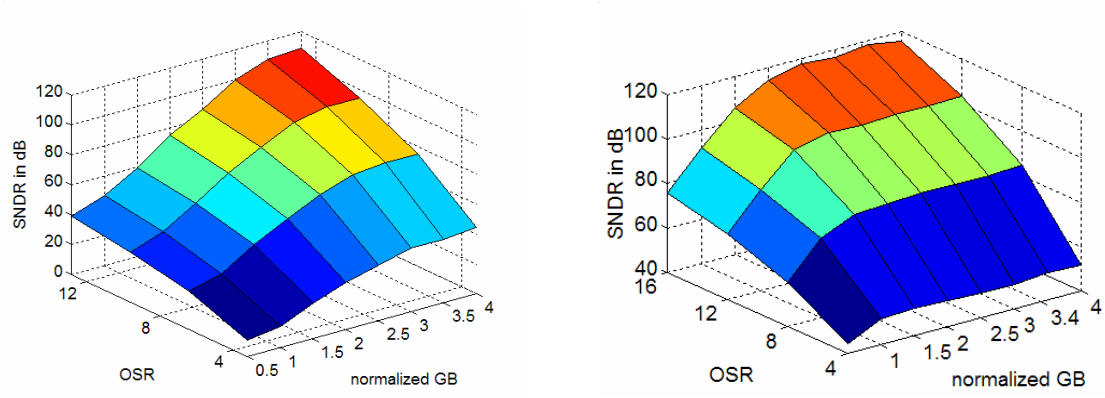


Fig. 5.12 First stage histogram of the integrator inputs and quantizer input relative to the FS voltage.



(a) **(b)**

Fig.5.13 SNDR vs normalized GB and OSR of (a) the 2-1-1-1 cascade [Rio00b], and (b) the proposed one in this paper with N=4.

Fig.5.13 presents the performance improvement with respect to the settling error by comparing the SNDR, signal-to-(noise+distortion) ratio, vs. the normalized GB and OSR of the 2-1-1-1(4b) cascade [Rio00b] with the one described in this paper with *N=4* and 4-bit quantizers in the first and third stage, respectively. The result of behavioral simulation

is obtained by assuming that the slew rate of opamps always follows the relationship of described in Equation 3.4.22, where $V_{eff}=200\ mV$. It is shown that the needed gain-bandwidth-product in Hz of the proposed one is only $2f_s$, whereas that of the traditional 2-1-1-1 cascade is over $4fs$ [Mar98] [Rio00a], in order to avoid the impact of settling error.

Note that there is a systematic loss of 1 bit, or 6 dB SNDR in the traditional cascade architectures due to the smaller amplifying factor in comparison with a theoretical $(N+1)^{th}$-order Sigma-Delta modulator. This loss is avoided in the proposed architecture, since the proposed integrator gains are optimized to obtain the ideal $(N+1)^{th}$-order noise shaping function [Yin06a] [Yin06b].

Returning to the proposed 4-b quantizer in the first stage, note that the quantization noise is low, so that the quantization noise leakage is significantly low. The new modulator architecture dramatically relaxes the requirements of high precision analog stages especially that of opamps with high dc-gain, which is more difficult to obtain as IC technologies advance [Yin05a].

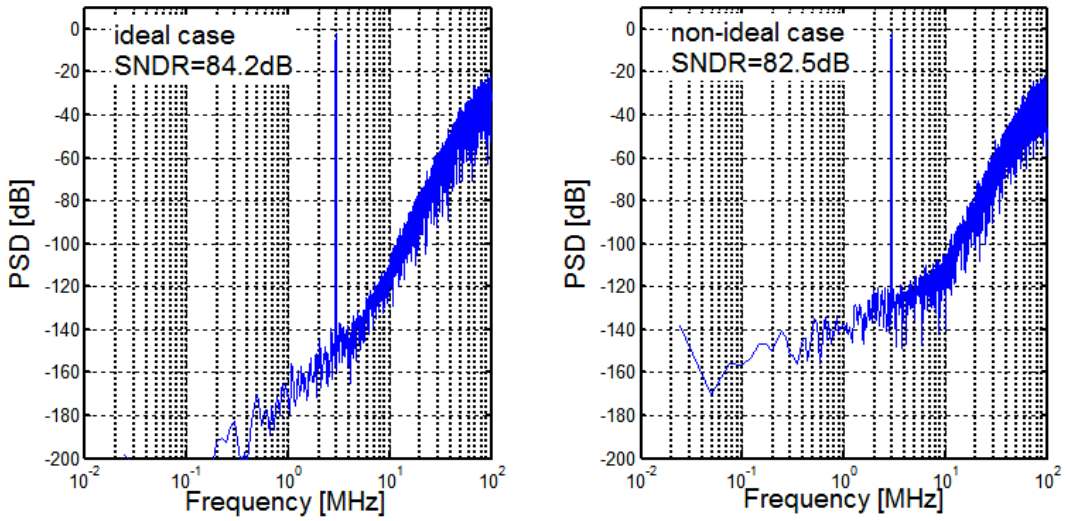
Finally, the proposed architecture is insensitive to the nonlinearity of opamps by inserting the additional feed-forward path from the modulator input directly to the quantizer input in the first stage, where the loop filter processes only shaped quantization noise. Because no input signal is processed by the loop-filter integrators; therefore, no harmonic distortion is generated [Siv01].

5.3.2.2. Simulation results

The proposed architecture has been validated by behavior simulation of a 2(4b)-1-1-1(4b) modulator in MATLAB®. The modulator was designed with a sampling rate of 200 MHz, a fixed OSR of 8, yielding a signal bandwidth of 12.5 MHz. The input is a 3 MHz sine-wave signal with amplitude of -3 dBFS. The 4 bit quantizers are used for the first- and last stage modulators, and the single-bit quantizers are used for other modulators. The scaling loop gains are set as mentioned before. The finite dc gain, non-linearity, unity-gain

frequency of opamps, and capacitor mismatching in the integrators of the first stage are set to 55 dB, 20%, 400 MHz (SR≈260 V/μs) and 0.1%, respectively.

The output spectra of the ideal case and the aforementioned non-ideal case are shown in Fig. 5.14. The achievable SNDR is 84.2 dB and 82.5 dB, respectively.



(a) **(b)**

Fig. 5.14 The output spectra of the proposed 2(4b)-1-1-1(4b) (a) with ideal case, (b) with circuit non-idealities

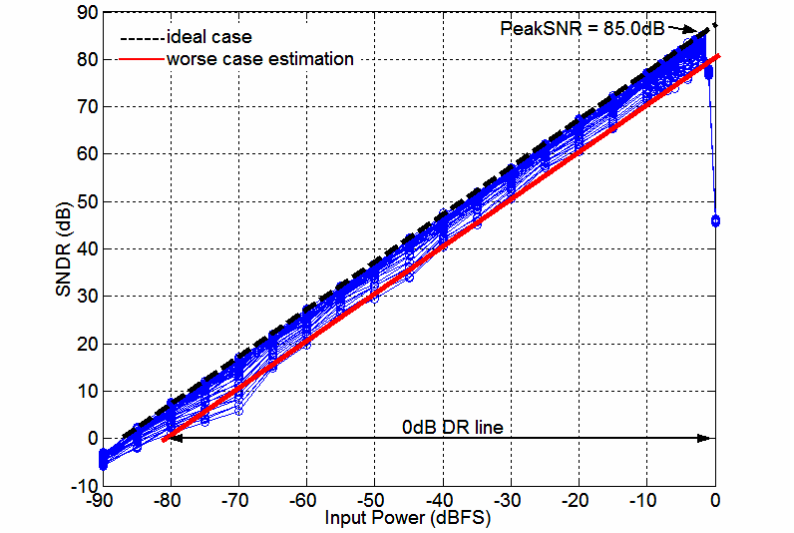


Fig. 5.15 The SNDR against input level in the proposed Sigma-Delta modulator with Monte Carlo analysis.

Fig. 5.15 illustrates the SNDR against the input level for the proposed modulator with Monte Carlo analysis of 30 times, where not only the process variation of capacitors are considered as the worst case σ_C=0.5%, but also the design parameter variation of finite opamp dc gain and GBW frequency are assumed in the worse case as large as 20% deviated from their nominal values, respectively. It is shown that the achievable peak SNDR and DR of the proposed modulator are not sensitive to circuit non-idealities, and even with the assumed large parameter variations the performance degradation is only about 6 dB.

These considerations made for the behavior simulation are summarized in Table 5.4.

Front-end Integrator	Capacitor standard deviation	0.1-0.5%
	Bottom paracitic capacitor	20%
Amplifier	Open-loop DC-gain	55 dB+-20%
	Gain-bandwidth product (2.5pF)	400 MHz+-20%
	Slew-rate (2,5 pF)	260V/uS+-20%
	DC-gain non-linearity	20%

Table 5.4. Non-idealities considerations

Table 5.5 presents the predicted performance summary of the proposed 2(4b)-1-1-1-(4b) Sigma-Delta modulator.

Sampling frequency	200	MHz
Digital output rate (M=8)	25	MS/s
Peak SNDR(ideal case)	85	dB
Peak SNDR(nonideal case)	82.5	dB
Peak SNDR(worse case)	79.2	dB
DR (ideal case)	87.8	dB
DR (worse case)	81.5	dB
Estimated Power Consumption (1.8Vsupply)	120-150	mW

Table 5.5. Performance summary

5.3.3. Cascade multibit Sigma-Delta modulator with improved NTF

5.3.3.1. Proposed architecture

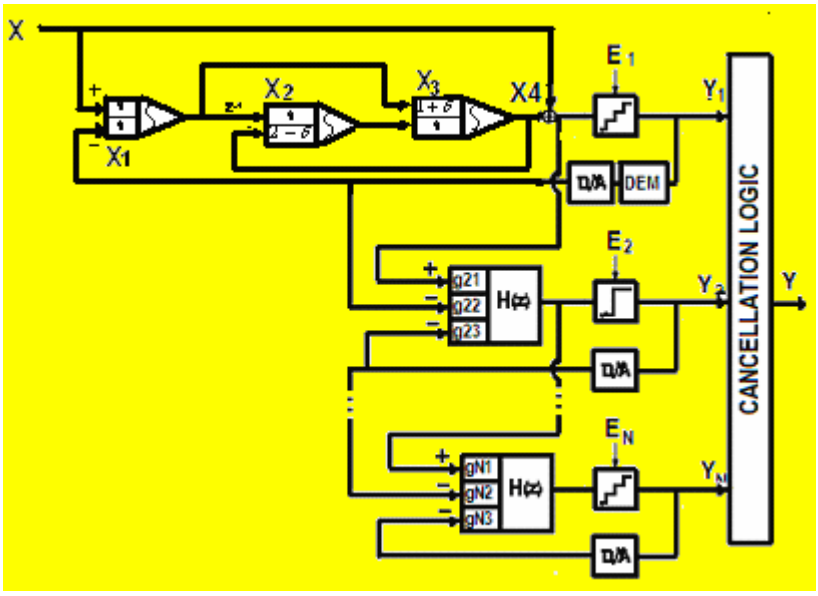


Fig. 5.16 The proposed 5th-order 3-stage cascade 3(5b)-1-1(5b) ΣΔ modulator.

Based on the section 5.2.2, a Sigma-Delta modulator with the 3rd-order finite-impulse-response NTF in the first stage is used to replace the second order modulator of the tranditional cascade Sigma-Delta modulators. Fig. 5.16 illustrates the proposed generic modulator architecture, where the interstage scaling factors are 1 based on the consideration of physically achievable output swings, combined with behavior simulation and statistical optimization. The number of quantization bits of the quantizer in the first stage and the last stage are 5. The quantizer in the first stage serves to ensure the stability as mentioned in section 5.2.2, and the other one in the last stage helps to increase the resolution. ∫ in the blocks denotes the integration function. Ideally, the quantization error in all stages except that in the last one of the cascade structure can be completely cancelled in the digital domain. The noise and signal transfer functions of the proposed ΣΔ modulator can be simply derived from the corresponding functions of the modified 3rd-order and cascade, respectively. Therefore, the output signal can be expressed as the combination of the delayed input signal and the modified $(N+2)^{th}$-order noise-shaped quantization noise (**N** is the number of cascaded stages), that is:

$$Y(z) = X(z) * z^{-(N-1)} + E_N (1 - z^{-1})^N (1 - \delta z^{-1} + z^{-2}) \qquad 5.3.3$$

where $X(z)$ is the Z-transform of the modulator input, E_N indicates the last-stage quantization error. Note that the proposed interstage scaling factors do not degrade the dynamic range as the other cascade structures.

5.3.3.2. Comparison

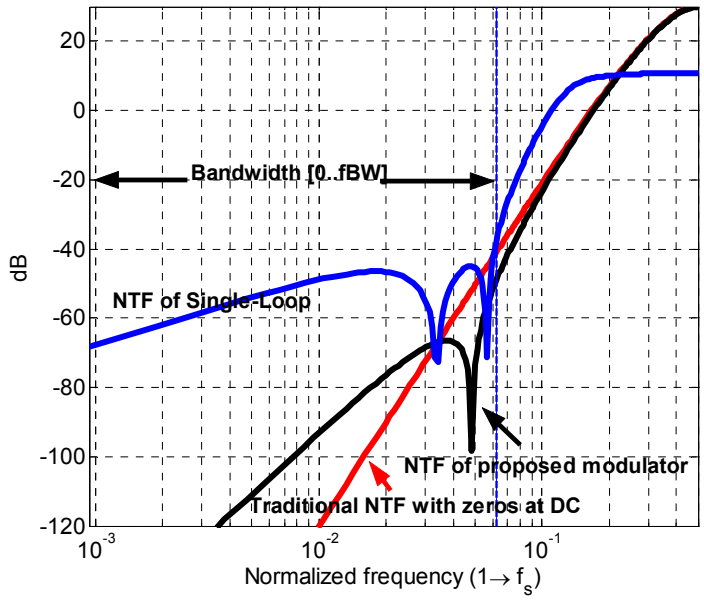


Fig. 5.17. The output spectra and frequency responses of various 5th-order NTF's

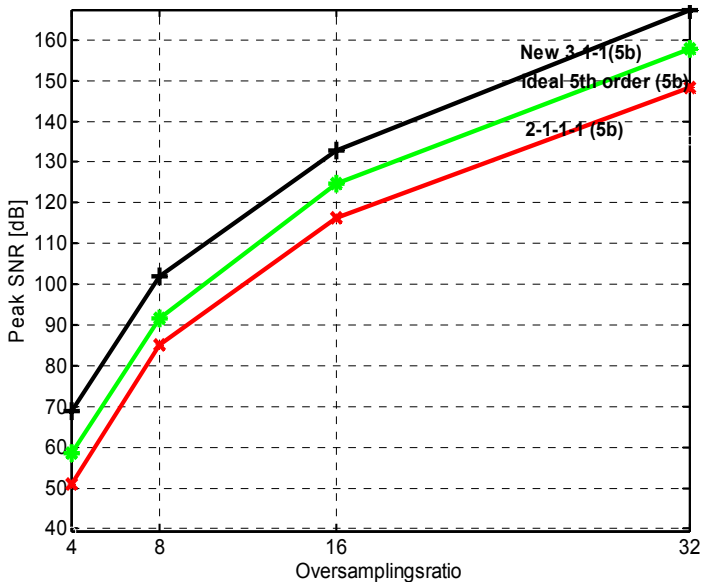


Fig. 5.18. The dynamic range versus oversampling ratio

Fig.5.17 shows the frequency responses of various types of 5th-order NTF, where the aggressive 5th-order NTF with relaxed OBG of 3.5 is applied for the single-loop one. We found that the proposed in-band noise shaping provides the better overall attenuation of quantization noise than single-loop topology, and significantly better attenuation of quantization noise at high-frequencies even than the traditional theoretical Sigma-Delta modulator with all zeros at DC. Furthermore, by assuming that all integrators, comparators, and DACs are ideal, and then the theoretically achievable peak SNR can be compared for the proposed Sigma-Delta modulator, as a function of the oversampling ratio, with the theoretical 5th–order (zeros at DC) and cascade 2-1-1-1 proposed in [Rio00a], respectively,. The results are shown in Fig.5.18. With an oversampling ratio of 8, the proposed topology is the best choice, which achieves the highest peak SNR over 100dB.

Note that the proposed cascade multibit Sigma-Delta modulator realizes the high-order low-distortion multibit Sigma-Delta modulator with improved NTF without the requirement for the quantizer with extreme high numbers of the quantization bits. [Yin04]

5.3.3.3. Analysis of circuit non-linearites

Besides the DAC-induced errors, nevertheless, it must be taken into account in practice that the circuit nonidealities, such as integrator leakage, capacitance mismatching, finite settling-time, etc., can degrade the Sigma-Delta performances. Both the integrator leakage and weight mismatching affect the integrators not exactly to $z^{-1}/(1-z^{-1})$. Since the dominant noise leakage and weight mismatching are added at the first stage, and at the following stages are shaped by higher-order high-pass filters, the noise budget at the first stage are only needed to consider the noise budget at the first stage in order to simplify the analysis.

As mentioned in section 3.4.1, the integrator leakage caused by finite- DC- gain of opamp in the integrator can be modeled with a variable “alpha”, where α is $(A-1)/A$, and A is the finite DC-gain of opamps. The integrator transfer fuction is rewritten:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}\alpha} \qquad 5.3.4$$

Thus, the z-domain output of the first stage in the cascade 3-1-1 multibit Sigma-Delta can be calculated as [Yin05a]

$$Y_1(z) = X(z) + E_1(z)\left(\frac{1-\delta z^{-1}.\alpha + \alpha^2 z^{-2}}{1+\delta z^{-1}(1-\alpha)+z^{-2}(1-\alpha)^2}\right)\left(\frac{1-z^{-1}.\alpha}{1+z^{-1}(1-\alpha)}\right) \qquad 5.3.5$$

where $E_1(z)$ is the first-stage quantization error. Considering $\alpha \cong 1$, Eq. 5.3.5 can be approximated to [Yin05a]

$$\begin{aligned} Y_1(z) &\cong X(z) + E_1(z)\left(1-\delta z^{-1}.\alpha+\alpha^2 z^{-2}\right)\left(1-z^{-1}.\alpha\right) \\ &\cong X(z) + E_1(z)(1-\delta z^{-1}+z^{-2})(1-z^{-1}) \\ &+ E_1(z)\left[(1-\delta z^{-1}+z^{-2})(1-\alpha)z^{-1} + \delta(1-\alpha)z^{-1}(1-z^{-1})^2\right. \\ &+ \left.\left(\delta(1-\alpha)^2 z^{-2}(1-z^{-1})\right) + (\delta-1-\delta\alpha+\alpha^2)\,z^{-2}(1-z^{-1})\right. \\ &+ \left.(\delta-1-\delta\alpha+\alpha^2)\,(1-\alpha)z^{-3}\right] \end{aligned} \qquad 5.3.6$$

Note that the first and second terms together in Eq. 5.3.6 correspond to the ideal output of Sigma-Delta modulator with a modified 3rd–order quantization error shaping; the quantization errors are ideally completely cancelled in the digital domain. Furthermore, the leakage error presented in the additional third term of $(1-\alpha)$ can be suppressed by high-pass filters of $(1-\delta z^{-1}+2)^{-2}$ (i.e. modified 2nd-order) and $(1-z^{-1})^{-2}$ (i.e. 2nd-order), respectively. The leakage of $(1-\alpha)^2$ and $(\delta-1-\delta\alpha+\alpha^2)$ in the third term are the 1st–order noise shaped. Nevertheless, they are neglectable, since $\alpha \cong 1$ and $\delta \cong 2$. Furthermore, the leakage $(\delta-1-\delta\alpha+\alpha^2)(1-\alpha)$ can also be ignored.

As mentioned in section 3.4.2, in SC Sigma-Delta modulators, integrator weights are implemented by means of capacitor ratios. In practice, the variation of the process parameters causes a deviation of the implemented weights from their nominal values. Assuming that the actual integrator weight has a small deviation ε from their nominal value, the practical integration function in z-domain is obtained [Rio04b]:

$$H(z) = \frac{(1+\varepsilon)z^{-1}}{1-z^{-1}} \qquad 5.3.7$$

It can further be derived an additional error ΔY(z) due to the incomplete cancellation of the quantization error[Yin05a]:

$$\Delta Y(z) \cong \varepsilon \times E_1(z)(1-z^{-1})\,(1-\delta z^{-1}+z^{-2}) \qquad 5.3.8$$

where terms in ε_2 are neglected due to $\varepsilon<<1$. The deviation is modified 3rd-order noise shaped.

The increase of the output-referred in-band error power of at cascade 3-1-1 ΣΔ modulator due to leakages and weight mismatching can be estimated as [Yin05a]:

$$P_{in-band} \approx \frac{\Delta_1^2}{12}\left(\frac{\gamma_1(1-\alpha)^2\pi^4}{M^5} + \varepsilon_1^2\frac{\gamma_2\pi^6}{7M^7}\right) \qquad 5.3.9$$

where Δ1 is the level spacing in the N-bit quantizer of the first stage, M is the oversampling ratio. γ_1 and γ_2 are the modified factor corresponding to modified NTF.

The Equation (5.3.9) demonstrates that the noise leakage is modified *2rd*-order shaped, capacitor mismatching error source is modified *3th*-order shaped, one order noise-shaping more than that in the conventional cascade 2-1-1-1mb[Rio00a] or 2-2-1mb[Vle01] ΣΔ ADC. The use of 5-b quantizers in the first stage not only ensures the stability of the 3rd – order modulator, but also directly reduces their quantization noise, and hence further reduces quantization noise leakage. As a result, the new modulator architecture significantly relaxes the requirements of high precision analog blocks, especially the requirement for high performance opamps. These effects will be illustrated by the following simulation results.

5.3.3.4 Simulation results

The proposed low-distortion cascade 3(5b) -1(1b)-1(5b) Sigma-Delta modulator was simulated with Matlab to evaluate the dynamic performance and circuit requirements. In these simulations, a 3 MHz sine-wave signal with the amplitude of -4dBFS was applied; the sample frequency was 200MHz for a targeted 12.5MHz bandwidth. The output spectra were computed using 16384 points FFT.

The spectra of various Sigma-Delta architectures were compared in Fig. 5.19, where only quantization errors were considered. The proposed architecture presents much higher attenuation at the in-band high-frequencies. The SQNR of the proposed Sigma-Delta modulator is 99dB, in contrast to 87.4 dB of the cascade 2-1-1-1(5bit) structure, 76.8 dB of

the single-loop structure, where both structures were slightly modified to the same 5th-order 5-bit quantizer according to [Rio00a] [Rhe00], respectively, to ensure that the performances of these structures were comparable.

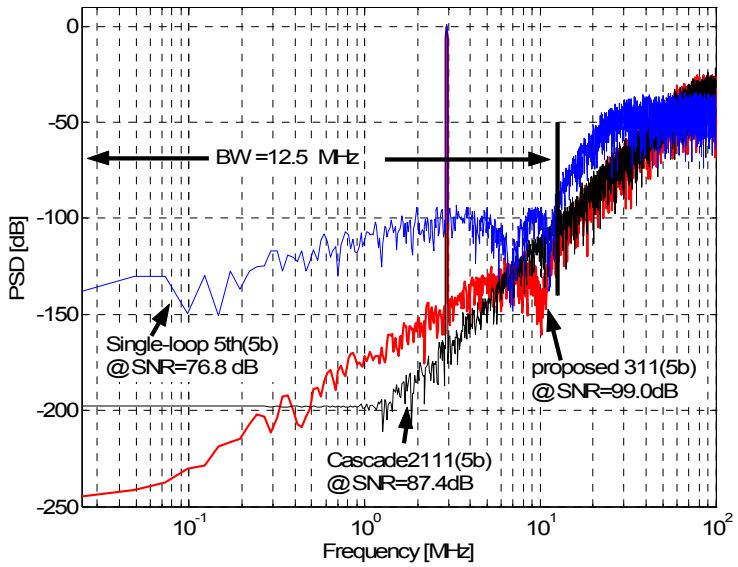


Fig. 5.19. The ideal output spectra of various ΣΔ modulators.

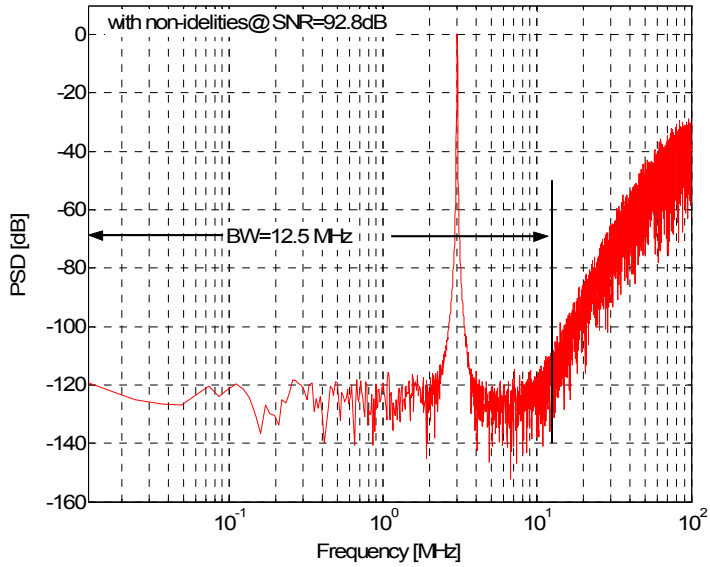


Fig. 5.20. The output spectrum of proposed ΣΔ modulator with non-idealities.

Fig.5.20 presents the output spectrum of the proposed ΣΔ modulator with non-idealities. The thermal noise (KT/C) budget was assumed -96 dBFS (FS=+-2V). Since the noise

leakages are shaped by higher orders, the opamp DC-gain as well as its dynamic requirements are significantly relaxed. The nonlinear opamp gain used to construct the integrator was assumed as 40dB. The opamp gain varied from about half of the maximum dc-gain to the maximum dc-gain according to hyperbolic tangent function. The choices of opamp bandwidth (GBW) and slew-rate were 200MHz and 300V/us, respectively. Taking into account of these circuit imperfections, the proposed modulator achieved a signal-to-(noise+distortion) ratio SNDR of 93.3dB, a spurious-free dynamic range SFDR of 109dB, and produced almost no harmonics of the input signal at the output.

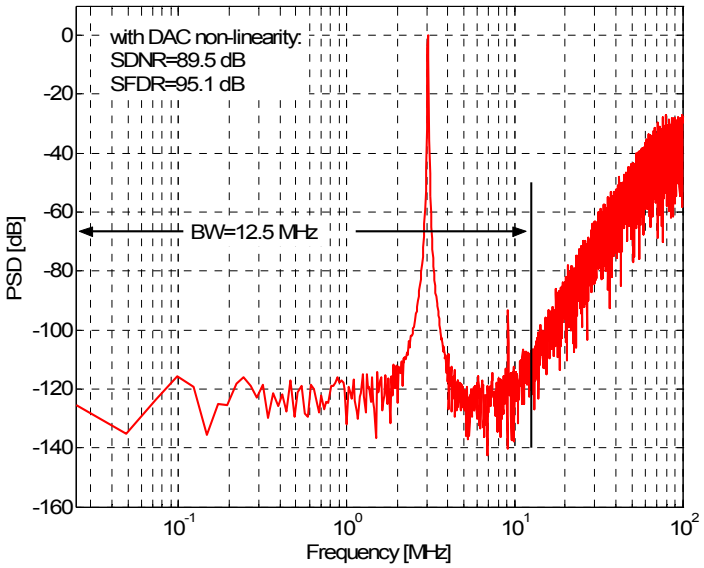


Fig. 5.21. The output spectrum of proposed ΣΔ modulator with 0.05% DAC non-linearity.

The effects of the DAC non-linearity on the proposed topology are shown in Fig.5.21. In this simulation, additional 0.05% DAC non-linearity errors and involving the partitioned DWA [Ham04] model as DEM in the feedback path of the first stage were considered. According to Fig. 5.21, it is shown that the power spectral density of the output presents a raised noise floor and obviously introduced harmonic tones due to non-linearity of DAC. The achievable SNDR is 89.8dB and SFDR 96.3 dB. The maximum SNDR of 91.9dB shown in Fig. 5.22 is obtained for a -2dB input level. It also implies that the modulator has a wide enough stable range.

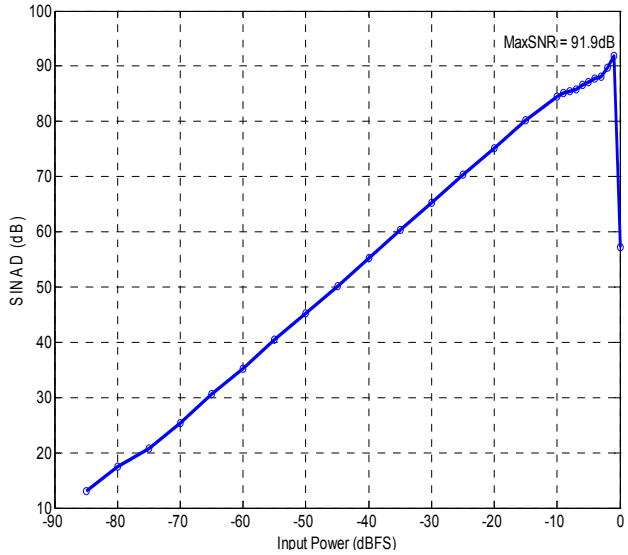


Fig. 5.22. The dynamic range of proposed ΣΔ modulator

These considerations of the worse case made for the behavior simulation are summarized in Table 5.6.

Front-end Integrator	Capacitor standard deviation	0.5%
	Bottom paracitic capacitor	20%
Amplifier	Open-loop DC-gain	40 dB
	Gain-bandwidth product (2.5pF)	300 MHz
	Slew-rate (2,5 pF)	200V/uS
	DC-gain non-linearity	50%

Table 5.6. Non-idealities considerations of the worse case

Table 5.7 presents the predicted performance summary of the proposed 3(5b)-1-1-1-(5b) Sigma-Delta modulator.

Sampling frequency	**200**	**MHz**
Digital output rate (M=8)	**25**	**MS/s**
Peak SNDR(ideal case)	**99**	**dB**
Peak SNDR(worse case)	**91.9**	**dB**
Peak SFDR(worse case)	**96.3**	**dB**

Table 5.7. Performance summary

5.3.4 Comparison of proposed

In order to compare performance differences of both proposed Sigma-Delta modulator architectures, the proposed 3-1-1 Sigma-Delta modulator is slightly modified to 3(5b)-1-1(4b) with the assumed nonidealities as mentioned in section 5.3.2.2. Therefore, the both proposed modulators have the same modulator order, effective quantizer and non-idealities of circuits.

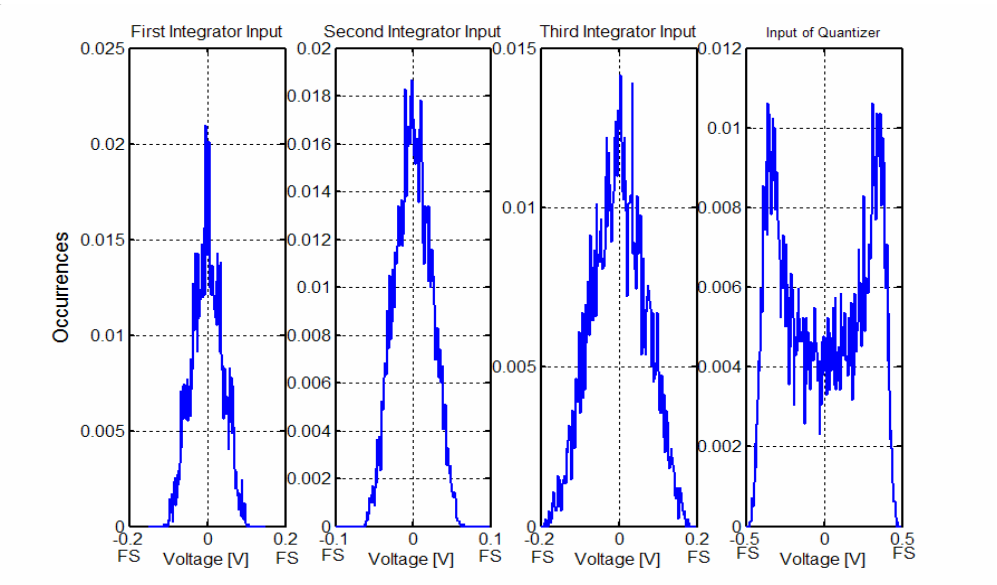


Fig. 5.23 First stage histogram of the integrator inputs and quantizer input relative to the FS voltage.

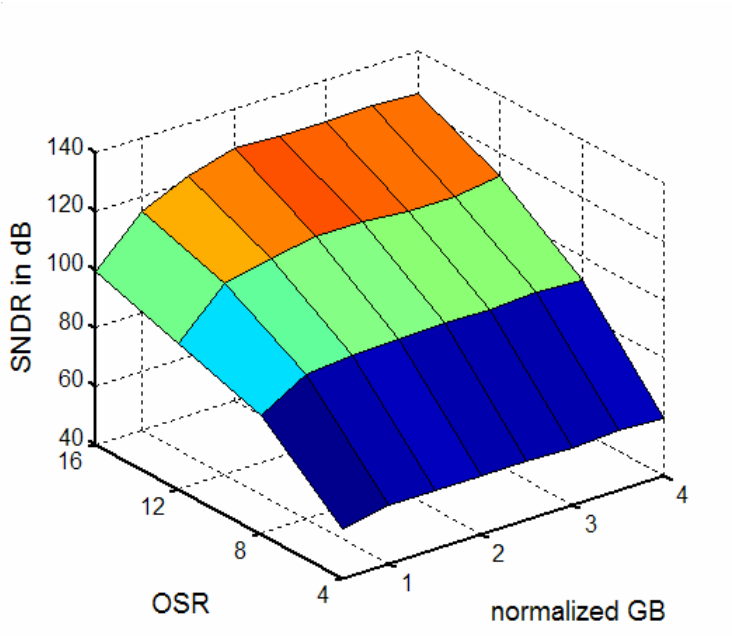


Fig.5.24 SNDR vs normalized GB and OSR of the 3(5b)-1-1(4b) cascade

Fig. 5.23 shows the histogram of the integrator inputs (*X1, X2* and *X3*) and quantizer input (*X4*) of the 3-1-1 modulator (as illustrated in Fig. 5.16) for an input signal with the amplitude of -3 dBFS. The possible amplitudes are considerable low as the proposed 2(4b)-1-1-1(4b) as illustrated in Fig 5.12. Consequently, the demanded gain-bandwidth-product in Hz of opamps in the proposed one is only $2f_s$ as illustrated in Fig 5.24, which is as that of the proposed 2(4b)-1-1-1(4b) cascade illustrated in Fig 5.13(b).

Note that there is a over 10 dB SNDR improvement in the 3-1-1 cascade architectures due to the higher noise suppression at high frequencies [Yin06a] [Yin06b].

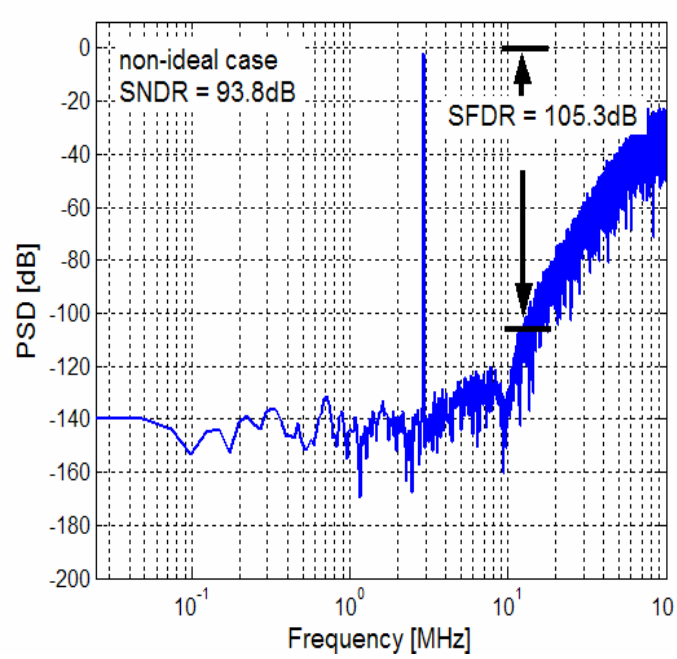


Fig 5.25 The out spectrum of the proposed 3(5b)-1-1(4b) with circuit non-idealities

The output spectrum of the proposed 3-1-1 in case of the aforementioned non-idealities in section 5.3.2.2 is shown in Fig. 5.25. The achievable SNDR is 93.8 dB and SFDR 105.3 dB, respectively.

Fig. 5.26 illustrates the SNDR against the input level for the proposed modulator with Monte Carlo analysis of 30 times, where not only the process variation of capacitors are considered as the worst case σ_C=0.5%, but also the design parameter variation of finite opamp dc gain and GBW frequency are assumed in the worse case as large as 20%

deviated from their nominal values, respectively. It is shown that the achievable peak SNDR and DR of the proposed modulator are not sensitive to circuit non-idealities, and even with the assumed large parameter variations the performance degradation is only about 3 dB, which is insensitiver than the proposed 2(4b)-1-1-1(4b).

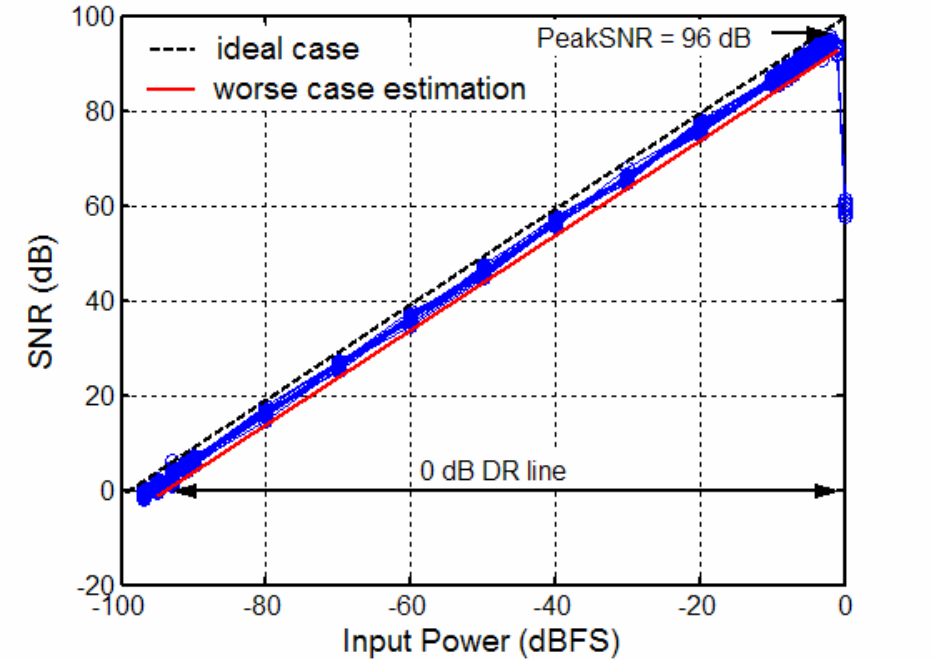


Fig. 5.26 The SNDR against input level in the proposed Sigma-Delta modulator with Monte Carlo analysis.

Clearly, the proposed 3(5b)-1-1(4b) modulator has better performance than the proposed 2(4b)-1-1-1(4b); the slight increased hardware in quantizer and digital circuits is generally the price of the performance improvement.

5.4. Summary

In this chapter, two low-distortion cascade high-order Sigma-Delta modulator architectures have been proposed. The performance of the proposed modulators has been analyzed and compared with other topologies. Simulation results show that the settling behavior is improved; the sensitivity to nonidealites of analog circuits, such as finite bandwidth, DC gain and slew rate, etc. is decreased. Moreover, the low distortion with improved NTF

cascade multibit Sigma-Delta modulator architecture significantly suppresses the in-band noise power, especially at high frequencies, so that the achievable SQNR is even better than theoretical value. Indeed, the proposed architectues are very suitable for high-resolution broadband applications, as well as for low-power design in scaled IC technologies.

Chapter 6 Conclusions and Future Work

6.1 Introduction

This work focused on studying high-speed high-resolution Sigma-Delta modulators for communication systems. In this research area, techniques for relaxing the settling error were the key. There were two general motives of this research: 1) the use of BiCMOS processes in designing high DC-gain and bandwidth opamp to reduce settling errors in Sigma-Delta modulators; 2) the use of developed architectures, which relaxing the requirement on settling behavior of opamps. This chapter will summarize key research contributions and results regarding the motives, and provide some recommendations for future work.

6.2 Key research contributions

This research explored the implementation of high-speed, high-resolution, low-power Sigma-Delta modulators in concert with diverse design techniques. According to the knowledge of the author, key research contributions and results are summarized below:

- Analyzed and simulated impacts of circuit non-idealities in SC Sigma-Delta modulators. Futhermore introduced a systematic method in design of SC Sigma-Delta modulators.

- Demonstrated a wideband Sigma-Delta modulator with BiCMOS process at reasonable power dissipation. An experimental prototype achieved 78.3dB (13bit) of dynamic range and dissipated 140 mW by electrical simulation at 10 MS/s Nyquist rate.

- Designed a new single-stage BiCMOS operational amplifier with one side gain-boosting which has desirable properties for maximizing DC-gain and bandwidth.

- Provided a comprehensive analysis of the settling limitation in high-order Sigma-Delta ADC architectureș.

- Developed a new 2(mb)….1(mb) N-stage low distortion cascade Sigma-Delta architecture at 8X oversampling ratio.

- Developed a new 3(mb)…1(mb) N-stage low distortion cascade Sigma-Delta architecture with improved NTF at 8X oversampling ratio.

6.3. Conclusion

In this dissertation, the resolution and the speed limitation of the existing Sigma-Delta ADC architectures have been discussed. A cascade BiCMOS Sigma-Delta modulator has been presented. In this design, the operational amplifier (opamp) with high dc gain and gain-bandwidth-product has been achieved by using the advanced BiCMOS technology. In order to meet with the main-stream sub-micron CMOS processes two low-distortion cascade Sigma-Delta ADC architectures have been proposed. The 2(4b)-1-1-1(4b) low distortion cascade Sigma-Delta architecture minimizes the signal level at the integrators of the first stage by using a feedforward path from the input directly to the input of the quantizer, therefore, *STF=1*. The advantages of this proposed architecture are relaxed requirement on the opamp gain-bandwidth-product up to $2\,f_s$, which is lower than $3\text{-}4\,f_S$ in other traditional Sigma-Delta modulator implementations, and reduced sensitivitiy to nonidealities of circuits, such as finite dc-gain of opamps and capacitor mismatching. Particularly the non-linearity of the opamps is also reduced. The 3(5b)-1-1-1(4b) low distortion cascade Sigma-Delta architecture achieves the same performance as the 2(4b)-1-1-1(4b) modulator. Additionally, the proposed approach realizes the modified FIR-NTF, by replacing two DC-zeros with a pair complex-conjugat zeros, to suppress the in-band noise floor at high-frequencies. Hence, these architectures are particularly suitable for realizing wide bandwidth ADCs as well as for low-power design as IC technologies advance.

6.4 Recommended future work

Demonstrations of the proposed modulators by using advanced CMOS processes would be a good next step in this area. In addition, the design of low-power programmable decimation filters is another area where further research is demanded. High-linear DAC will be a critical part, which should be further investigated, developed and implemented in the future.

References

[Abi00] A. A. Abidi, G. J. Pottie, and W. J. Kaiser, “Power-conscious design of wireless circuits and systems,” *Proc. IEEE*, vol. 88, pp. 1528–1545, Oct. 2000.

[Abo99] A. Abo, P.R. Gray, .A 1.5V, 10-bit, 14.3-MS/s CMOS pipelined analog-to-digital converter,. *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp.599-606, May. 1999

[Ada87] S.R. Adarlan and J.J. Paulos, “An Analysis of Nonlinear Behaviour in Sigma Delta Modulators”. IEEE Transactions on Circuits and Systems, vol. 34, pp. 593-603, June 1987.

[Ada86] R.W. Adams, “Design and Implementation of an Audio 18-bit Analog-to-Digital Converter Using Oversampling Techniques”. Journal of Audio Engineering Society, vol. 34, pp. 153-166, March 1986.

[Ada90] T. Adachi, A. Ishikawa, A. Barlow, and K. Takasuka, "A 1.4V switched capacitor filter", in proc. IEEE Custom Integrated Circuits Conference, pp.8.2.1-8.2.4, 1990.

[Ada91] R.W. Adams, P.F. Ferguson, A. Ganesan, S. Vincelette, A. Volpe, and R.Libert, “Theory and practical implementation of a fifth-order sigma-delta A/D converter”. Journal of Audio Engineering Society, vol. 39, pp. 515-528, July 1991.

[Ada95] R.W. Adams and T.W. Kwan, “Data-directed scrambler for multi-bit noiseshaping D/A converters”. U.S. Patent 5,404,142, 1995.

[Ada97a] R.W. Adams and R. Schreier, “Stability Theory ΣΔModulators”, Chapter 4 in Delta-Sigma Data Converters: Theory, Design and Simulation (S.R.Norsworthy, R. Schreier, nd G.C. Temes, Editors). IEEE Press, 1997.

[Ada97b] R.W. Adams, “The Design of High-Order Single-Bit ΣΔ ADCs”, Chapter 5 in Delta-Sigma Data Converters: Theory, Design and Simulation (S.R. Norsworthy, R. Schreier, and G.C. Temes, Editors). IEEE Press, 1997

[Agr83] B.P. Agrawal and K. Shenoi, “Design methodology for Sigma-Delta modulators”. IEEE Transactions on Communications. vol. 31, pp. 360-370, March 1983.

[Ahu83] B.K. Ahuja, “An Improved Frequency Compensation Technique for CMOS Operational Amplifiers”. IEEE Journal of Solid-State Circuits, vol. 18, pp. 629-633, December 1983.

[And90] N.Andrew Karanicolas, Kenneth K.O, John Y. Wang, Hae-Seung Lee, Rafael L. Reif, “A High Frequency Full Differential BiCMOS Operational Amplifier” IEEE 1990 CUSTOM INTEGRATED CIRCUITS CONFERENCE 8.3.1-8.3.4

[Ank91] B.Ankele and F. Schrank, “High Precision SPICE Models for the Simulation of Analogue CMOS Circuits”, Proc. of IEEE EUROASIC Conf., Paris 1991.

[Apa02] R. Aparicio and A. Hajimiri, “Capacity Limits and Matching Properties of Integrated Capacitor”. IEEE Journal of Solid-State Circuits, vol. 37, no. 3, pp. 384-393, March 2002.

[Ara99] X. Aragonès, J.L. González, and A. Rubio, Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs. Kluwer Academic Publishers,1999.

[Au97] S. Au and B.H. Leung, “A 1.95-V, 0.34-mW, 12-b Sigma-Delta Modulator Stabilized by Local Feedback Loops”. IEEE Journal of Solid-State Circuits, vol. 32, no. 3, pp. 321-328, March 1997.

[Azi93] P. Aziz, H.V. Sorensen, and J.V.D. Spiegel, “Multiband Sigma-delta Modulation”. Electronics Letters, vol. 29, pp. 760-762, April 1993.

[Bah92] H. Baher and E. Afifi, “Novel fourth-order sigma-delta convertor”. Electronics Letters, vol. 28, pp. 1437-1438, July 1992.

[Baj02] O. Bajdechi and J.H. Huijsing, “A 1.8-Ṿ ΣΔ Modulator Interface for an Electret Microphone With On-Chip Reference”. IEEE Journal of Solid-State Circuits, vol. 37, pp. 279-285, March 2002.

[Bai94] R.T. Baird and T.S. Fiez, “Stability Analysis of High-Order Delta-Sigma Modulation for ADC’s”. IEEE Transactions on Circuits and Systems - II, vol. 41, pp. 59-62, January 1994.

[Bai95] R.T. Baird and T. Fiez, “Linearity Enhancement of Multibit ΣΔ A/D and D/A Converters using Data Weighted Averaging”. IEEE Transactions on Circuits and Systems - II, vol. 42, pp. 753-762, December 1995.

[Bai95b] R. T. Baird, T. S. Fiez, "A 14-bit 500 kHz delta-sigma ADC with 16 times oversampling", in proc. IEEE Custom Integrated Circuits Conference, pp.199-202, 1995.

[Bai96] R.T. Baird and T.S. Fiez, “A Low Oversampling Ratio 14-b 500-kHz ΣΔADC with a Self-Calibrated Multibit DAC”. IEEE Journal of Solid-State Circuits, vol. 31, pp. 312-320, March 1996.

[Bal00] P. Balmelli, Q. Huang, and F. Piazza, “A 50-mW 14-bit 2.5-MS/s ΣΔ modulator in a 0.25 μm digital CMOS technology”. Proc. of the Symposium on VLSI Circuits, pp. 142-143, 2000.

[Bal04] P. Balmelli, and Q. Huang, “A 25MS/s 14b 200mW ΣΔ Modulator in 0.18 μm CMOS,” in ISSCC Dig. Tech.Papers, Feb. 2004, pp. 74–75.

[Baz95a] S. Bazarjani, M. Snelgrove, and T. MacElwee, "A 1 V Switched-Capacitor Sigma-Delta modulator", in proc. IEEE Symposium on Low Power Electronics, pp. 70-71, 1995

[Baz95b] S. Bazarjani, and M. Snelgrove, "Low voltage SC circuit design with low - Vt MOSFETs", in proc. IEEE International Symposium on Circuits and Systems, vol. 2, pp. 1021-24, 1995.

[Ben48] W.R. Bennett. “Spectra of quantized signals”. Bell System Technical Journal, vol. 27, pp. 446-472, July 1948.

[Ben93] P. Benabes, A. Gauthier, and D. Billet, “New wideband sigma-delta convertor,” Electron. Lett., vol. 29, pp. 1575–1577, Aug. 1993.

[Ben97] P. Benabes, A. Gauthier, and D. Billet, “A Methodology for Designing Continous-Time Sigma-Delta Modulators,” Proceeding of the IEEE European Design and Test , pp. 46-50, March 1997.

[Ber99] J. Berrie, “The Defensive Design of Printed-Circuit Boards”. IEEE Spectrum, pp. 76-81, September 1999.

[Bla80] B. Black and D. Hodges, “Time-interleaved A/D conversion”. IEEE Journal of Solid-State Circuits, vol. SC-15, pp. 1022-1029, December 1980.

[Bla02] P.G. Blanken and S.E.J. Menten, “A 10μV-Offset 8kHz Bandwidth 4th-Order Chopped ΣΔ A/D Converter for Battery Management”. Proc. of the IEEE International Solid-State Circuits Conference, vol. 1, pp. 338-339, 2002.

[Bon96a] A. Boni and C. Morandi, “Low-power, low-voltage BiCMOS comparators for -200MH2, 8bit operation”, Proc. of IEEE VLSI Design ‘96 Conference, 1996.

[Bon96b] A. Boni and C. Morandi, “A Current Mirroring BiCMOS Comparator for Low-Voltage, Low-Power Applications”, Proc. of IEEE ESSCIRC’96 Conference, Neuchatel, Switzerland, September 1996.

[Bos88] B.E. Boser and B.A. Wooley, “The Design of Sigma-Delta Modulation Analog-to-Digital Converters”. IEEE Journal of Solid-State Circuits, vol. 23. pp. 1298-1308, December 1988.

[Bra90] B. P. Brandt, D. E. Wingard, and B. A. Wooley, "A 12.8-MHz sigma-delta modulator with 16-bit performance", in proc. Symposium on VLSI Circuits, pp. 27-28, 1990.

[Bra91a] B. Brandt, D.W. Wingard, and B.A. Wooley, “Second-Order Sigma-Delta Modulation for Digital-Audio Signal Acquisition”. IEEE Journal of Solid-State Circuits, vol. 23. pp. 618-627, April 1991.

[Bra91b] B.P. Brandt and B.A. Wooley, “A 50-MHz Multibit Sigma-Delta Modulator for 12-b 2-MHz A/D Conversion”. IEEE Journal of Solid-State Circuits, vol. 26, pp. 1746-1756, December 1991.

[Bra91c] B. Brant, *Oversampled analog-to-digital conversion,* PhD Dissertation ,Stanford University, 1991

[Bra97a] B. Brandt, “High-Speed Cascaded ΣΔ ADCs”, Chapter 7 in Delta-Sigma Data Converters: Theory, Design and Simulation (S.R. Norsworthy, R. Schreier, and G.C. Temes, Editors). IEEE Press, 1997.

[Bra97b] B. Brandt, P.F. Ferguson, and M. Rebeschini, “Analog Circuit Design of ΣΔADCs”, Chapter 11 in Delta-Sigma Data Converters: Theory, Design and Simulation (S.R. Norsworthy, R. Schreier, and G.C. Temes, Editors). IEEE Press, 1997.

[Bre99] L. J. Breems, E. J. van de Zwan, E. C. Dijkmans, and J. H. Huijsing, "A 1.8 mW CMOS Sigma Delta modulator with integrated mixer for A/D conversion of IF signals", in proc. IEEE International Solid-State Circuits Conference, pp. 52-53, 1999.

[Bre00] L. J. Breems, E. J. van der Zwan, and J. H. Huijsing, “A 1.8-mW CMOS ΣΔ modulator with integrated mixer for A/D conversion of IF signals,” *IEEE J. Solid-State Circuits*, vol. 35, pp. 468–475, Apr. 2000.

[Bri99] S. Brigati, F. Francesconi, P. Malcovati, D. Tonietto, A. Baschirotto and F. Maloberti“, Modeling Sigma-Delta Modulator Non-Idealities in SIMULINK”, *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS ‘99)*, 2, Orlando, USA, pp. 384-387, 1999.

[Bri02] S. Brigati, F. Francesconi, P. Malcovati, and F. Maloberti, “A fourth-order single-bit switched-capacitor sigma-delta modulator for distributed sensor applications”. Proc. of the IEEE Instrumentation and Measurement Technology Conference, vol.1, pp. 253-256, 2002.

[Bro74] A. P. Brokaw, “A simple three-terminaf bandgap reference,” *IEEE* J. Solid-State Circuits, vol. SC-9, pp. 288-393, Dec. 1974.

[Bro97] T.L. Brooks, D.H. Robertson, D.F. Kelly, A. Del Muro, and S. W. Harston, “A Cascaded Sigma-Delta Pipeline A/D Converter with 1.25 MHz Signal Bandwidth and 89 dB SNR”. IEEE Journal of Solid-State Circuits, vol. 32, pp. 1896-1906, December 1997.

[Bro02] T. Brooks, “Architecture Considerations for Multi-Bit ΣΔ ADCs”, in Analog Circuit Design — Structured Mixed-Mode Design, Multi-Bit Sigma-Delta Converters, Short Range RF Circuits (M. Steyaert, A.H.M. van Roermund, and J.H. Huijsing, Editors). Kluwer Academic Publishers, 2002.

[Bul90] K. Bult and G.J.G.M. Geelen, “A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain”. IEEE Journal of Solid-State Circuits, vol. 25, pp. 1379-1384, December 1990.

[Bul00] K. Bult, “Analog Design in Deep Sub-Micron CMOS”. Proc. of the IEEE European Solid-State Circuits Conference, pp. 11-17, 2000.

[Bur96] T.V. Burmas, K.C. Dyer, P.J. Hurst, and S.H. Lewis, “A second-order doublesampled delta-sigma modulator using additive-error switching”. IEEE Journal of Solid-State Circuits, vol. 31, pp. 284-293, March 1996.

[Bur98a] T. Burger and Q. Huang, “A 3-V 2.8-mW CMOS ΔΣ modulator for GSM applications,” in Symp. VLSI Circuits Dig. Tech. Papers, June 1998, pp. 90–91.

[Bur98b] T. Burger and Q. Huang, “On the optimum design of regulated cascade operational transconductance amplifiers,” in *Int. Symp. Low Power Electronic Design*, Aug. 1998, pp. 203–208.

[Bur01] T. Burger, and Q. Huang, "A 13.5-mW 185-Msample/s Delta Sigma modulator for UMTS/GSM dual-standard IF reception", IEEE Journal of Solid- State Circuits, vol. 36, pp. 1868-78, Dec. 2001.

[Can81] J.C. Candy and O.J. Benjamin, “The structure of quantization noise from sigma-delta modulation”. IEEE Transactions on Communications. vol. 29, pp. 1316-1323, September 1981.

[Can85] J.C. Candy, “A Use of Double Integration in Sigma-Delta Modulation”. IEEE Transactions on Communications. vol. 33, pp. 249-258, March 1985.

[Can86] J. C. Candy, "Decimation for Sigma Delta modulation", IEEE trans. on communications, ol. COM-34, No. 1, pp. 72-76, 1986.

[Can92] J. Candy and G. Temes, Oversampling Methods for A/D and D/A Conversion. New York: IEEE Press, 1992.

[Can95] J. Candy, .A use of double integration in sigma-delta modulation,. *IEEE Trans.Comm*. vol. COM-33, pp.249-258, Mar. 1995.

[Can97] J.C. Candy, “An Overview of Basic Concepts”, Chapter 1 in Delta-Sigma Data Converters: Theory, Design and Simulation (S.R. Norsworthy, R. Schreier, and G.C. Temes, Editors). IEEE Press, 1997.

[Cao00] J. Cao et al, "A 90 dB SNR, 2.5 MHz output rate ADC using cascaded multibit Delta-Sigma modulation at 8x oversampling ratio", in proc. IEEE International Solid-State Circuits Conference, pp. 338-339, 2000.

[Car88] L.R. Carley and J. Kenney, “A 16-bit 4^{th} order noise-shaping D/A converter”.Proc. of the IEEE Custom Integrated Circuits Conference, pp. 21.7.1-4, 1988.

[Car97] L.R. Carley, R. Schreier, and G.C. Temes, “Delta-Sigma ADCs with Multibit Internal Converters”, Chapter 8 in Delta-Sigma Data Converters: Theory, Design and Simulation (S.R. Norsworthy, R. Schreier, and G.C. Temes, Editors). IEEE Press, 1997.

[Cas01] H.J. Casier, “Requirements for Embedded Data Converters in an ADSL Communication System”. Proc. of the IEEE International Conference on Electronics, Circuits and Systems, vol. I, pp. 489-492, September 2001.

[Cat89] T. Cataltepe, A.R. Kramer, L.E. Larson, G.C. Temes, and R.H. Walden, “Digitally corrected multi-bit ΣΔ data converters”. Proc. of the IEEE International Symposium Circuits and Systems, pp. 647-650, 1989.

[CDR04] CDR1 BiCMOS Design Manual, Motorola, Inc, 2004

[Cha90a] K.C.-H. Chao, S. Nadeem, W.L. Lee, and C. Sodini, “A Higher Order Topology for Interpolative Modulators for Oversampling A/D Converters”. IEEE Transactions on Communications, vol. 37, pp. 309-318, March 1990.

[Cha90b] K. Chao, S. Dadeem, W. Lee and C. Sodini, .A higher order topology for interpolative modulators for oversampling A/D converter., *IEEE Trans. Circuits Systems*, pp.309-318, Mar. 1990

[Cha01] E. Charbon, R. Gharpurey, P. Miliozzi, R.G. Meyer, and A. Sangiovanni-Vincentelli, Substrate Noise: Analysis and Optimization for IC Design. Kluwer Academic Publishers, 2001.

[Che95] F. Chen and B.H. Leung, “A High Resolution Multibit Sigma-Delta Modulator with Individual Level Averaging”. IEEE Journal of Solid-State Circuits, vol. 30, pp. 453-460, April 1995.

[Che96] F. Chen; B. Leung, "A 0.25 mW 13 b passive Sigma Delta modulator for a 10 MHz IF input", in proc. IEEE International Solid-State Circuits Conference,pp. 58-59, 1996.

[Che98] F. Chen and B. Leung, “Some observations on tone behavior in data weighted averaging,” in Proc. IEEE ISCAS, May 1998, pp. 500–503.

[Che99] K.-D. Chen and T.-H. Kuo, “An improved technique for reducing baseband tones in sigma-delta employing data weighted averaging algorithms without adding dither,” IEEE Trans. Circuits Syst. II, vol. 46, pp. 63–68, Jan. 1999.

[Che01] H. Chen, B. Song, and K. Bacrania, "A 14-b 20-MSamples/s CMOS pipelined ADC", IEEE Journal of Solid-State Circuits, vol. 36, pp. 997-1001, June 2001.

[Che02] V. Cheung, H. Luong, and W. Ki, "A 1-V 10.7 MHz switched-opamp bandpass Sigma-Delta modulator using double-sampling finite-gain-

compensation technique", IEEE Journal of Solid-State Circuits, vol. 37, pp. 1215-25, Oct. 2002.

[Chi96] S.-Y. Chin, C.-Y. Wu, .A CMOS ratio-independent and gain-insensitive algorithmic analog-todigital converter,. *IEEE Journal of Solid-State Circuits*, vol.31, no.8, pp.1201-1207, Aug. 1996.

[Chi00] Y. Chiu, **"**Inherently linear capacitor error-averaging techniques for pipelined A/D conversion,. IEEE Transactions on Circuits and Systems II: Analog and Digital *Signal Processing*, vol.47, no.3, pp.229-232, Mar. 2000.

[Chi04] Y. Chiu, C. Tsang, B. Nikolic, P. R. Gray .Least-mean-square adaptive digital background calibration of pipelined A/D converters ,. to be appeared in *IEEE* Transaction on Circuits and Systems(I), Jan. 2004

[Cho89] W. Chou, P. Wong, and R. Gray, "Multi-Stage Sigma-Delta Modulation". IEEE Transaction on Information Theory, vol. 35, pp. 784-796, July 1989.

[Cho95a] T. Cho, Low-Power Low-Voltage Analog-to-Digital Conversion Techniques *Using Pipelined Architectures*, PhD. Dissertation, University of California at Berkeley, 1995.

[Cho95b] T. Cho, P. R. Gray, .A 10 b, 20 Msample/s, 35 mW pipeline A/D converter,. *IEEE Journal of Solid-State Circuits*, vol.30, no.3, pp.166-172, March 1995.

[Cli96] D.W. Cline, P.R. Gray, **"**A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2-μm CMOS,. *IEEE Journal of Solid-State Circuits*, vol.31, no.3, pp.294-303, March 1996

[Cob99] A.L. Coban and P.E. Allen, "A 1.5V 1.0mW Audio Delta Sigma Modulator with 98dB Dynamic Range". Proc. of the IEEE International Solid-State Circuits Conference, pp. 50-51, 1999.

[Col93] W.T. Colleran and A. A. Abidi, "A lO-b, 75-MHz Two-stage Pipelined Bipolar AID converter", JSSC, vol. 28, no. 12, December 1993.

[Cor94] R.F. Cormier Jr., T.L. Sculley, and R.H. Bamberger, "Combining Sub-band Decomposition and Sigma-delta Modulation for Wide-band A/D Conversion". Proc. of the IEEE International Symposium Circuits and Systems, pp. 357-360, 1994.

[Cro83] R.E. Crociere and L.R. Rabiner, Multirate Digital Signal Processing. Prentice-Hall, 1983.

[Cut60] C.C. Cutler, Transmission System Employing Quantization. U.S. Patent No. 2,927,962, 1960.

[Ded94] I. Dedic, “A Sixth-Order Triple-Loop ΣΔ CMOS ADC with 90dB SNR and 100kHz Bandwidth”. Proc. of the IEEE International Solid-State Circuits Conference, pp. 188-189, 1994.

[Des01] M. Dessouky, and A. Kaiser, "Very low-voltage digital-audio Delta-Sigma modulator with 88-dB dynamic range using local switch boothstrapping", IEEE Journal of Solid-State Circuits, vol. 36, pp. 349-355, Mar. 2001.

[Dez03] A. Dezzani, and E. Andre, "A 1.2-V dual-mode WCDMA/GPRS Sigma Delta modulator", in proc. IEEE International Solid-State Circuits Conference, pp. 58-59, 2003.

[Dia92] V.F. Dias, G. Palmisano, P. O’Leary, and F. Maloberti, “Fundamental Limitations of Switched-Capacitor Sigma-Delta Modulators”. IEE Proceedings-G, vol. 139, pp. 27-32, February 1992.

[Dia93] V.F. Dias and V. Liberali, “Cascade Pseudomultibit Noise Shaping Modulators”. IEE Proceedings-G, vol. 140, no. 4, pp. 237-246, August 1993.

[Doe84] J. Doernberg, H. S. Lee, and D.A. Hodges, “Full-Speed Testing of A/D Converters”. IEEE Journal of Solid-State Circuits, vol. 19, no. 6, pp. 820-827, December 1984.

[Dorr03] L. Dorrer, A. Di Giandomenico, and A. Wiesbauer, “A 10-Bit, 4 mW Continuous-Time Sigma-Delta ADC for UMTS in a 0.12 μm CMOS process”. Proc. of the IEEE International Symposium Circuits and Systems, pp. 1057- 1060, 2003.

[Eng99] J.V. Engelen and R. van de Plassche, BandPass Sigma-Delta Modulators: Stability Analysis, Performance and Design Aspects. Kluwer Academic Publishers, 1999.

[Enz96] C.C. Enz and G.C. Temes, “Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization”. Proceedings of the IEEE, vol. 84, no. 11, pp. 1584-1614, November 1996.

[Esh96] A. Eshraghi and T. Fiez, “A Comparison of Three Parallel ΣΔA/D Converters”. Proc. of the IEEE International Symposium Circuits and Systems, pp. 517-520, 1996.

[Esh03] A. Eshraghi and T. Fiez, “A Time-Interleaved Parallel ΣΔ A/D Converter”. IEEE Transactions on Circuits and Systems - II, vol. 50, pp. 118-129, March 2003.

[Fel97] A. R. Feldman, ”High speed, low-power sigma-delta modulator for RF baseband channel application”, Ph.D. Dissertation, University of California Berkeley, 1997

[Fel98a] A.R. Feldman, B.E. Boser, and P.R. Gray, “A 13-Bit, 1.4-MS/s Sigma-Delta Modulator for RF Baseband Channel Applications”. IEEE Journal of Solid-State Circuits, vol. 33, pp. 1462-1469, October 1998.

[Fel98b] A.R. Feldman, “High-Speed, Low-Power Sigma-Delta Modulators for RF Baseband Channel Applications”. Dissertation, University of California, Berkeley, 1998.

[Fel99] M. Felder and J. Ganger, “Analysis of Ground-Bounce Induced Substrate Noise Coupling in a Low Resistive Bulk Epitaxial Process: Design Strategies to Minimize Noise Effects on a Mixed-Signal Chip”. IEEE Transactions on Circuits and Systems - II, vol. 46, pp. 1427-1436, November 1999.

[Fer90] P. F. Ferguson Jr, A. Ganesan, and R. W. Adams, “One bit higher-order sigma-delta A/D converters,” in Proc. IEEE ISCAS, May 1990, pp. 890–893.

[Fis82] J.H. Fischer, “Noise Sources and Calculation Techniques for Switched Capacitor Filters”. IEEE Journal of Solid-State Circuits, vol. 17, no. 4, pp. 742-752, August 1982.

[Fis82] G. Fisher and G. Moschytz, “On the frequency limitations of SC filters,” *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 510–518, Aug. 1984.

[Fla96] D. Flandre, A. Viviani, J. Eggermont, B. Gentine, and P. Jespers, “Design methodology for CMOS gain-boosted folded-cascode OTA with application to SOI technology,” in *Proc. ESSCIRC’96*, 1996, pp. 320–323.

[Fog00] E. Fogleman, I. Galton, W. Huff, and H. Jensen, “A 3.3-V Single-Poly CMOS Audio ADC Delta-Sigma Modulator with 98-dB Peak SINAD and 105-dB Peak SFDR”. IEEE Journal of Solid-State Circuits, vol. 35, pp. 297-307, March 2000.

[Fog01] E. Fogleman, J. Welz, and I. Galton, “An audio ADC Delta-Sigma modulator with 100-dB peak SINAD and 102-dB DR using a second-order mismatchshaping DAC”. IEEE Journal of Solid-State Circuits, vol. 36, pp. 339-348, March 2001.

[Fuj97] I. Fujimori, K. Koyama, D. Trager, F. Tam, and L. Longo, “A 5-V Single-Chip Delta-Sigma Audio A/D Converter with 111 dB Dynamic Range”. IEEE Journal of Solid-State Circuits, vol. 32, pp. 329-336, March 1997.

[Fuj00] I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kosic, J. Cao, and S.-L.Chan, “A 90-dB SNR 2.5-MHz Output-Rate ADC Using Cascaded Multibit Delta-Sigma modulation at 8x Oversampling Ratio”. IEEE Journal of Solid-State Circuits, vol. 35, pp. 1820-1828, December 2000.

[Gag03] R. Gaggl, A. Wiesbauer, G. Fritz, C. Schranz, and P. Pessl, “A 85-dB Dynamic Range Multibit Delta-Sigma ADC for ADSL-CO Applications in 0.18-µm CMOS”. IEEE Journal of Solid-State Circuits, vol. 38, pp. 1105-1114, July 2003.

[Gag04] R. Gaggl, M. Inversi, A. Wiesbauer , “ A Power Optimized 14-Bit SC ΔΣ Modulator for ADSL CO Applications,” in ISSCC Dig. Tech.Papers, Feb. 2004, pp. 82 – 83

[Gal95] I. Galton and H.T. Jensen, “Delta-Sigma Based A/D Conversion Without Oversampling”. IEEE Transactions on Circuits and Systems - II, vol. 42, pp. 773-784, December 1995.

[Gal96] I. Galton and H.T. Jensen, “Oversampling Parallel Delta-Sigma Modulator A/D Conversion”. IEEE Transactions on Circuits and Systems - II, vol. 43, pp. 801-810, December 1996.

[Gau00] G. Cauwenberghs and G. C. Temes, “Adaptive digital correction of analog errors in MASH ADC’s-part I. Off-line and blind on-line calibration,” IEEE Trans. Circuits Syst. II, vol. 47, pp. 621–28, July 2000.

[Gee99] Y. Geerts, A. Marques, M. Steyaert, and W. Sansen, “A 3.3-V, 15-bit, Delta-Sigma ADC with a Signal Bandwidth of 1.1 MHz for ADSL Applications”. IEEE Journal of Solid-State Circuits, vol. 34, pp. 927-936, July 1999.

[Gee00] Y. Geerts, M. Steyaert, and W. Sansen, “A High-Performance Multibit ΣΔ CMOS ADC”. IEEE Journal of Solid-State Circuits, vol. 35, pp. 1829-1840, December 2000.

[Gee02] Y. Geerts, M. Steyaert, and W. Sansen, Design of Multi-Bit Delta-Sigma A/D Converters. Kluwer Academic Publishers, 2002.

[Gei82] R. Geiger and E. Sanchez-Sinencio, “Operational amplifier gainbandwidth product effects on the performance of switched-capacitor networks,” *IEEE Trans. Circuits Syst.*, vol. CAS-29, pp. 96–106, Feb. 1982.

[Ger03] F. Gerfers, M. Ortmanns, and Y. Manoli, “A 1.5-V 12-bit Power-Efficient Continuous-Time Third-Order ΣΔ Modulator”. IEEE Journal of Solid-State Circuits, vol. 38, pp. 1343-1352, August 2003.

[Ger03] A. Gerosa and A. Neviani, “A Very Low-Power 8-bit ΣΔ Converter in a 0.8µm CMOS Technology for the Sensing Chain of a Cardiac Pacemaker, Operating down to 1.8V”. Proc. of the IEEE International Symposium on Circuits and Systems, vol. 5, pp. 49-52, 2003.

[Gob81] C.-A. Gobet and A. Knob, “Noise Analysis of Switched Capacitor Networks”.Proc. of the IEEE International Symposium on Circuits and Systems, pp. 856-859, 1981.

[Gob83] C.-A. Gobet and A. Knob, “Noise Analysis of Switched Capacitor Networks”.IEEE Transactions on Circuits and Systems, vol. CAS-30, no. 1, pp. 37-43, January 1983.

[Gog95] P. van Gog, B. M. J. Kup, and R. van Osch, “A two-channel 16/18b audio AD/DA including filter function with 60/40 mW power consumption at 2.7 V,” in ISSCC Dig. Tech. Papers, Feb. 1995, pp. 208–209.

[Gom00] G.J. Gomez, “A 102-dB Spurious-Free DR ΣΔ ADC Using a Dynamic Dither Scheme”. IEEE Transactions on Circuits and Systems - II, pp. 531-535, June 2000.

[Gom02] G. Gomez and B. Haroun, "A 1.5V 2.4/2.9mW 79/50dB DR ΣΔ Modulator for GSM/WCDMA in a 0.13µm Digital Process". Proc. of the IEEE International Solid-State Circuits Conference, vol. 1, pp. 306-307, 2002.

[Goo95] M. Goodson, B. Zhang, and R. Schreier, "Proving Stability of Delta-Sigma Modulators Using Invariant Sets". Proc. of the IEEE International Symposium on Circuits and Systems, vol. 2, pp. 633-636, 1995.

[Goo96] F. Goodenough, "Analog Techniques of all Varieties Dominate ISSCC". Electronic Design, vol. 44, pp. 96-111, February 1996.

[Gra77] P. R. Gray and R. G. Meyer, Analysis and Design of Analog *Integrated Circuits. New* York: Wiley, 1977

[Gra90] R.M. Gray, "Quantization Noise Spectra". IEEE Transactions on Information Theory, vol. 36, pp. 1220-1244, November 1990.

[Gra97] R.M. Gray, "Quantization Noise in ΣΔ A/D Converters", Chapter 2 in Delta-Sigma Data Converters: Theory, Design and Simulation (S.R. Norsworthy, R. Schreier, and G.C. Temes, Editors). IEEE Press, 1997.

[Gra01] P.R. Gray, P. Hurst, S. Lewis, R. G. Meyer, "Analysis and Design of Analog Integrated Circuits", 4th Edition, January 2001

[Gre86] R. Gregorian and G.C. Temes, Analog MOS Integrated Circuits for Signal Processing. John Wiley & Sons, 1986.

[Gri96] J. Grilo, E. Mac Robbie, R. Halim, and G. Temes, "A 1.8V 94dB Dynamic Range ΣΔ Modulator for Voice Applications". Proc. of the IEEE International Solid-State Circuits Conference, pp. 230-231, 1996.

[Gri02] J. Grilo, I. Galton, K. Wang, and R.G. Montemayor, "A 12-mW ADC Delta-Sigma Modulator With 80 dB of Dynamic Range Integrated in a Single-Chip Bluetooth Transceiver". IEEE Journal of Solid-State Circuits, vol. 37, pp. 271-278, March 2002.

[Gro89] D. W. J. Groeneveld et al., "A self-clibration technique for monolithic high-resoultion D/A converters," IEEE J. Solid-State Circuits, vol. 24, pp. 1517–1522, Dec. 1989.

[Gui01] J. Guilherme, P. Figueredo, P. Azevedo, G. Minderico, A. Leal, J. Vital, and J. Franca, "A Pipeline 15-b 10Msample/s Analog-to-Digital Converter for

ADSL Applications". Proc. of the IEEE International Symposium on Circuits and Systems, vol. 1, pp. 396-399, May 2001.

[Gup02] S.K. Gupta and V. Fong, "A 64-MHz Clock-Rate ΣΔ ADC with 88-dB SNDR and -105-dB IM3 Distortion at a 1.5-MHz Signal Frequency". IEEE Journal of Solid-State Circuits, vol. 37, pp. 1653-1661, December 2002.

[Gus00] M. Gustavsson, J.J. Wikner, and N.N. Tan, CMOS Data Converters for Communications. Kluwer Academic Publishers, 2000.

[Hai83] D. Haigh and B. Singh, "A Switching Scheme for Switched Capacitor Filters which Reduces the Effect of Parasitic Capacitances Associated with Switch Control Terminals". Proc. of the IEEE International Symposium on Circuits and Systems, pp. 586-589, 1983.

[Hai91] A. Hairapetian, G.C. Temes, and Z.X. Zhang, "Multibit sigma-delta modulator with reduced sensitivity to DAC nonlinearity". Electronics Letters, vol. 27, pp. 990-991, May 1991.

[Hai94] A. Hairapetian and G.C. Temes, "A Dual-Quantization Multi-Bit Sigma Delta Analog/Digital Converter". Proc. of the IEEE International Symposium on Circuits and Systems, vol. 5, pp. 437-440, 1994.

[Hai96] A. Hairapetian, "A 81-MHz IF receiver in CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 1996, pp. 56–57.

[Hal92] B. Hallgren, "Design of a Second-Order CMOS Sigma-Delta A/D Converter with 150MHz Clock Rate". Proc. of the European Solid-State Circuits Conference, pp. 103-106, 1992.

[Hal93] B. Hallgren, "Continuous-Time Implementation of Sigma-Delta Converters for High Frequency Operation". Proc. of the European Conference on Circuit Theory and Design, pp. 1601-1606, 1993.

[Ham00] C. Hammerschmied, "CMOS A/D converters using MOSFET-only R-2R ladders," Ph.D. dissertation, ETH, Zurich, Switzerland, 2000.

[Ham02a] A. A. Hamoui and K. Martin, "Linearity enhancement of multibit ΔΣ modulators using pseudo data-weighted averaging," in *Proc. IEEE ISCAS*, May 2002, pp. III 285–288.

[Ham02b] A. A. Hamoui and K. Martin, “Delta-sigma modulator topologies for high-speed high-resolution A/D converters,” in *Proc. IEEE Midwest Symp. Circ. Syst.*, Aug. 2002, pp. I 356–359.

[Ham03] A. A. Hamoui and K. Martin, “A1.8-V 3-MS/s 13-bit ΣΔ A/D converter with pseudo data-weighted-averaging in 0.18-μm digital CMOS,” in Proc. IEEE Custom Integrated Circ. Conf., Sept. 2003, pp. 7-3-1–7-3-4.

[Ham04] A. A. Hamoui, K. Martin, “High-Order Multibit ΔΣ Modulators and Pseudo Data-Weighted-Averaging in Low- Oversampling ΣΔ ADCs for Broad-Band Applications,” *IEEE Trans. Circuits Syst. I*, vol. 51, pp. 72-85, Jan. 2004

[Hay86] T. Hayashi, Y. Inabe, K. Uchimura, and A. Iwata, "A multistage Delta-Sigma modulator without double integration loop", in proc. IEEE International Solid-State Circuits Conference, pp. 182-183, 1986.

[Hog81] E. B. Hogenauer, “An economical class of digital filters for decimation and interpolation,” IEEE Trans. Acoust., Speech Signal Processing, vol. ASSP-29, pp. 155–162, Apr. 1981.

[Hua99] Q. Huang, P. Orsatti, and F. Piazza, “GSM tranceiver front-end circuits in 0.25-μm CMOS,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 292–303, Mar. 1999.

[Ing92] S. Ingalsuo, T. Ritoniemi, T. Karema, and H. Tenhunen, "A 50 MHz Cascaded Sigma-delta A/d Modulator", in proc. IEEE Custom Integrated Circuits Conference, pp. 16.3.1-16.3.4, 1992.

[Ing97] M. Ingels and M.S.J. Steyaert, “Design Strategies and Decoupling Techniques for Reducing the Effects of Electrical Interference in Mixed-Mode IC’s”. IEEE Journal of Solid-State Circuits, vol. 32, pp. 1136-1141, July 1997.

[Ing98] J. M. Ingino, B. A. Wooley, .A continuously calibrated 12-b, 10-MS/s, 3.3-V A/D converter,. *IEEE Journal of Solid-State Circuits*, vol.33, no.12, pp.1920-1931, Dec.1998.

[Ino62] H. Inose, Y. Yasuda, and J. Murakami, “A Telemetering System by Code Modulation − Δ-Σ Modulation”. IRE Transactions on Space Electronics and Telemetry, vol. 8, pp. 204-209, September 1962.

[Int05] INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS 2005 EDITION *EXECUTIVE SUMMARY*

[Jag52] F. de Jagar, "Delta modulation -- a method of PCM transmission using the one unit code", Philips Res. Rep., vol. 7, pp. 442-466, 1952

[Jia02] R. Jiang, and T.S. Fiez, "A 1.8V 14b ΔΣ A/D Converter with 4MSamples/s Conversion". Proc. of the IEEE International Solid-State Circuits Conference, pp.220-221, 2002.

[Jia04] R. Jiang, and Terri S. Fiez, "A 14-bit ΔΣ ADC With 8 OSR and 4-MHz Conversion Bandwidth in a 0.18-μm CMOS Process" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 39, NO. 1, JANUARY 2004 63-74

[Joh97] D.A. Johns and K. Martin, "Analog Integrated Circuit Design" John Wiley&Sons, 1997.

[Joh99] J.E. Johnston, "A 24-bit delta-sigma ADC with an ultra-low noise chopperstabilized programmable gain instrumentation amplifier". Proc. of the International Conference on Advanced A/D and D/A Conversion Techniques and Their Applications, pp. 179-182, 1999.

[Kar90] T. Karema, T. Ritoniemi, and H. Tenhunen, "An oversampled sigma-delta A/D converter circuit using two-stage fourth order modulator". Proc. of the IEEE International Symposium on Circuits and Systems, vol. 4, pp. 3279-3282,1990.

[Kar92] T. Karema, T. Husu, T. Saramaki, and H. Tenhunen, "A filter processor for interpolation and decimation", in proc. IEEE Custom Integrated Circuits Conference, pp. 19.2.1-19.2.4, 1992.

[Kar93] A.N. Karanicolas, H.-S. Lee, K.L. Barcrania, **"**A 15-b 1-Msample/s digitally self-calibrated pipeline ADC,. *IEEE Journal of Solid-State Circuits*, vol.28, no.12, pp.1207-1215, Dec. 1993.

[Kas99] D.B. Kasha, W.L. Lee, and A. Thomsen, "A 16-mW, 120-dB linear switchedcapacitor delta-sigma modulator with dynamic biasing". IEEE Journal of Solid-State Circuits, vol. 34, pp. 921-926, July 1999.

[Ken88] J. G. Kenney and L. R. Carley, "CLANS: A high-level synthesis tool for high resolution data converters," in ICCAD Dig. Tech. Papers, Nov. 1988, pp. 496–499.

[Ken93] J. G. Kenney and L. R. Carley, “Design of multibit noise-shaping data converters,” in Analog Integrated Circuits and Signal Processing. Boston, MA: Kluwer, 1993, pp. 99–112.

[Ker94] D.A. Kerth, D.B. Kasha, T.G. Mellissinos, D.S. Piasecki, and E.J. Swanson, “A 120dB Linear Switched-Capacitor Delta-Sigma Modulator”. Proc. of the IEEE International Solid-State Circuits Conference, pp.196-197, 1994.

[Kes02] M. Keskin, U.-K. Moon, and G.C. Temes, “A 1-V 10-MHz Clock-Rate 13-Bit CMOS ΣΔ Modulator Using Unity-Gain-Reset Opamps”. IEEE Journal of Solid-State Circuits, vol. 37, pp. 817-824, July 2002.

[Kho93] R. Khoini-Poorfard and D.A. Johns, “Time-interleaved oversampling converters”. Electronics Letters, vol. 29, pp. 1673-1674, September 1993.

[Kho97] R. Khoini-Poorfard, L.B. Lim, and D.A. Johns, “Time-interleaved Oversampling A/D Converters: Theory and Practice”. IEEE Transactions on Circuits and Systems - II, vol. 44, pp. 634-645, August 1997.

[Ki 87] W.-H Ki and G. C. Temes, “Offset-compensated switched-capacitor integrators,” in Proc. IEEE ISCAS, May 1990, pp. 2829–2832.

[Kin94] E. King, F. Aram, T. Fiez, and I. Galton, “Parallel Delta-Sigma A/D Conversion”. Proc. of the IEEE Custom Integrated Circuits Conference, pp. 23.3.1-4, 1994.

[Kin98] E.T. King, A. Eshragi, I. Galton, and T.S. Fiez, “A Nyquist-Rate Delta-Sigma A/D Converter”. IEEE Journal of Solid-State Circuits, vol. 33, pp. 45-52, January 1998.

[Kis99] P. Kiss, Adaptive Digital Compensation of Analog Circuit Imperfections for Cascaded Delta-Sigma Analog-to-Digital Converters. Ph.D. Thesis, Politehnica University of Timisoara, 1999.

[Kis00] P. Kiss, J. Silva, A. Wiesbauer, T. Sun, U.-K. Moon, J.T. Stonick, and G.C. Temes, “Adaptive Digital Correction of Analog Errors in MASH ADCs – Part II: Correction Using Test-Signal Injection”. IEEE Transactions on Circuits and Systems - II, vol. 47, pp. 629-638, July 2000.

[Kis01a] P. Kiss, U. Moon, J. Steensgaard, J. T. Stonick, and G. C. Temes, “High-speed ΣΔ ADC with error correction,” Electron. Lett., vol. 37, pp. 76–77, Jan. 2001.

[Kis01b] P. Kiss, U. Moon, J. Steensgaard, J. T. Stonick, and G. C. Temes, "Multibit delta-sigma ADC with mixed-mode DAC error correction,"in Proc. IEEE Int. Symp. Circuits and Systems (ISCAS'2001), Sydney, Australia, May 6–9, 2001, pp. 280–283.

[Kla75] K.B. Klaasen, "Digitally controlled absolute voltage division". IEEE Transactions on Instrumentation and Measurement, vol. 24, no. 3, pp. 106-112, June 1975.

[Kla96] H. Klar, "Integrierte Digitale Schaltungen MOS/BICMOS", 2th Edition, January 1996

[Koz00] M. Kozak and I. Kale, "Novel Topologies for Time-Interleaved Delta-Sigma Modulators". IEEE Transactions on Circuits and Systems - II, vol. 47, pp. 639-654, July 2000.

[Kuj73] K. E. Kujik, "A precision reference voltage source," *IEEE J. Solid-State Circuits,* vol. *SC-8,* pp. 222-226, June 1973.

[Kun88] K.K. Kung, P.K. Ko, C. Hu, and Y.C. Cheng, "Flicker Noise Characteristics of Advanced MOS Technologies". Proc. of the International Electron Device Meeting 1988, Technical Digest, pp. 34-37, December 1988.

[Kuo99] T.-H. Kuo, K.-D. Chen, and J.-R. Chen, "Automatic coefficients design for high-order sigma-delta modulators". IEEE Transactions on Circuits and Systems - II, vol. 46, pp. 6-15, January 1999.

[Kuo02] T.-H. Kuo, K.-D. Chen, and H.-R. Yeng, "A Wideband CMOS Sigma-Delta Modulator With Incremental Data Weighted Averaging". IEEE Journal of Solid-State Circuits, vol. 37, pp. 11-17, January 2002.

[Kwa97] S.-U. Kwak, B.-S. Song, K. Bacrania, **"**A 15-b, 5-Msample/s low-spurious CMOS ADC,. *IEEE Journal of Solid-State Circuits*, vol.32, no.12, pp.1866-1875, Dec. 1997.

[Lab87] C. A. Laber, C. F. Rahim, S. F. Dreyer, G. T. Uehara, P. T. Kwok, P. R. Gray, "Design Considerations for a High-Performance 3-μm CMOS Analog Standard-Cell Library," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 2, pp. 181-9, April 1987.

[Lak94] K. Laker and W. Sansen, Design of Analog Integrated Circuits and *Systems*. New York: McGraw-Hill, 1994.

[Lam01] H. Lampinen and O. Vainio, “Low-voltage fourth-order CMOS sigma-delta modulator implementation”. Electronics Letters, vol. 37, pp. 734-735, June 2001.

[Lar88] L.E. Larson, T. Cataltepe, and G.C. Temes, “Multi-bit oversampled ΣΔ A/D converter with digital error correction”. Electronics Letters, vol. 24, pp. 1051-1052, August 1988.

[Lee84] H.-S. Lee, D.A. Hodges, P.R. Gray, **“**A self-calibrating 15 bit CMOS A/D converter,.*IEEE Journal of Solid-State Circuits*, vol.SC-19, no.6, pp.813-819, Dec. 1984.

[Lee85] K.-L. Lee and R.G. Meyer, “Low-Distortion Switched-Capacitor Filter Design Techniques”. IEEE Journal of Solid-State Circuits, vol. 20, no. 6, pp. 1103-1113, December 1985.

[Lee87a] W.L. Lee, A novel higher order interpolative modulator topology for high resolution oversampling A/D converters. Ph.D. Thesis, Massachusetts Institute of Technology, 1987.

[Lee87b] W.L. Lee and C.G. Sodini, “A Topology for Higher Order Interpolative Coders”. Proc. of the IEEE International Symposium on Circuits and Systems, pp. 459-462, 1987.

[Lee94] H.-S. Lee, **“**A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC,.*IEEE Journal of Solid-State Circuits*, vol.29, no.4, pp.509-515, Apr. 1994.

[Lee01] S. Lee and K. Yang, “Design a Low-Jitter Clock for High-Speed A/D Converters”. Sensors, vol. 18, no. 10, October 2001.

[Lee03] K.-S. Lee and F. Maloberti, “A 1.8V, 1MS/s 85dB SNR 2+2 Mash ΣΔ Modulator with ±0.9V Reference Voltage”. Proc of the Symposium on VLSI Circuits, pp. 71-74, June 2003.

[Lei98] T.F. Lei, J.Y. Cheng, S.Y. Shiau, T.S. Chao, and C.S. Lai, “Characterization of Polysilicon Oxides Thermally Grown and Deposited on the Polished Polysilicon Films”. IEEE Transactions on Electron Devices, vol. 45, pp. 912-917, April 1998.

[Les90] T.C. Leslie and B. Singh, “An Improved Sigma-Delta Modular Architecture”. Proc. of the IEEE International Symposium on Circuits and Systems, pp. 372-375, 1990.

[Leu92] B. Leung and S. Sutarja, “Multibit Sigma-Delta ΔA/D Converter Incorporating a Novel Class of Dynamic Element Matching Techniques”. IEEE Transactions on Circuits and Systems - II, vol. 39, pp. 35-51, January 1992.

[Leu97] K.Y. Leung, E.J. Swanson, K. Leung, S.S. Zhu, “A 5V, 118dB ΣΔ Analog-to-Digital Converter for Wideband Digital Audio”. Proc. of IEEE International Solid-State Circuit Conference, pp. 218-219, 1997.

[Lew87] S.H. Lewis and P.R. Gray, “A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter”. IEEE Journal of Solid-State Circuits, vol. 22, no. 6, pp. 954-961, December 1987.

[Lew92] S.H. Lewis, H.S. Fetterman, G.F. Gross, R. Ramachandran, and T.R. Viswanathan, “A 10-b 20-Msample/s analog-to-digital converter”. IEEE Journal of Solid-State Circuits, vol. 27, no. 3, pp. 351-358, March 1992.

[Li84] P.W. Li, M.J. Chin, P.R. Gray, R. Castello, **“**A ratio-independent algorithmic analog-to-digital conversion technique,. *IEEE Journal of Solid-State Circuits*, vol.SC-19,no.6, pp.828-36, Dec. 1984.

[Li03] Bingxin Li, “Design of Multi-bit Sigma-Delta Modulators for Digital Wireless Communications” ISBN 91-7283-641-5 ISRN KTH/IMIT/LECS/ AVH-03/10—SE, ISSN 1651-4076 TRITA-IMIT-LECS AVH Stockholm, 2003

[Lib00] V. Liberali, R. Rossi, and G. Torelli, “Crosstalk effects in mixed-signal ICs in deep submicron digital CMOS technology”. Microelectronics Journal, vol. 31, pp. 893-904, December 2000.

[Lim90] P.J. Lim and B.A. Wooley, “An 8-bit 200-MHz BiCMOS Comparator”, IEEE JSSC, vol 25, no. 1, February 1990.

[Lin90] Y. M. Lin, Performance Limitations on High-Resolution Video-rate Analog-to-Digital Interfaces, PhD Thesis, University of California, Berkeley, UCB/ERL M90/55, 1990.

[Lin91] Y.-M. Lin, B. Kim, P. R. Gray, .A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3 μm CMOS,. *IEEE Journal of Solid-State Circuits*, vol.26, no.4, pp.628-636, April 1991.

[Lin99] C.-H. Lin, C. Shi, M. Ismail, and M. Gyu, "A 5MHz Nyquist Rate Continuous-Time Sigma-Delta Modulator for Wideband Wireless Communication". Proc. of the IEEE International Symposium on Circuits and Systems, vol. 2, pp. 368-371, 1999.

[Lin00] J.C.H. Lin, TSMC 0.25μm Mixed-Signal 1P5M+ MIM Salicide 2.5V/5.0V Design Guideline. Taiwan Semiconductors Manufacturing Co., LTD, March 2000.

[Lin02] Z. Lin, W. Sheu, "A Generic Multiple-Feedback Architecture and Method for the Design of High-Order Σ–Δ Modulators *IEEE Trans. Circuits Syst. II*, vol. 49, pp. 465-473, Jul. 2002

[Lip92] S.P. Lipshitz, R.A. Wannamaker, and J. Vanderkoy, "Quantization and Dither: A Theoretical Survey". Journal of the Audio Engineering Society, vol. 40, pp. 355-375, May 1992.

[Lon88] L. Longo and M. Copeland, "A 13 bit ISDN-band oversampled ADC using two-stage third-order noise shaping". Proc. of the IEEE Custom Integrated Circuit Conference, pp. 21.2.1-4, 1988.

[Lon93] L. Longo *et al.*, "A cellular analog front end with a 98-dB IF receiver," in *ISSCC Dig. Tech. Papers*, Feb. 1993, pp. 36–37.

[Luh98a] L. Luh, J. Choma Jr., and J. Draper, "A 50-MHz Continuous-Time Switched-Current Sigma-Delta Modulator". Proc. of the IEEE International Symposium on Circuits and Systems, vol. 1, pp. 579-582, 1998.

[Luh98b] L. Luh and J. Choma, "A Continuous-Time Switched-Current Sigma-Delta Modulator with Reduced Loop Delay". Proc. of the 8th Great Lakes Symposium on VLSI, pp. 286-291, 1998.

[Luh00] L. Luh, J. Choma, and J. Draper, "A 400-MHz th-Order Continuous-Time Switched-Current ΣΔ Modulator". Proc. of the European Conference on Solid-State Circuits, pp. 72-75, 2000.

[Mal01] F. Maloberti, Analog Design for CMOS VLSI Systems. Kluwer Academic Publishers, 2001.

[Mal03] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral Modeling of Switched-Capacitor Sigma–Delta Modulators" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: FUNDAMENTAL THEORY AND APPLICATIONS, VOL. 50, pp. 352-364, MARCH 2003

[Mar81] K. Martin and A. Sedra, "Effects of the op amp finite gain and bandwidth on the performance of SC filters," *IEEE Trans. Circuits Syst.*, vol. CAS-28, pp. 822–829, Aug. 1981.

[Mar97] A. Marques, V. Peluso, M. Steyaert, and W. Sansen, "Optimal parameters for cascade ΣΔ modulators," in *Proc. IEEE ISCAS'97*, June 1997, pp. 61–64.

[Mar98a] A.M. Marques, V. Peluso, M.S.J. Steyaert, and W. Sansen, "A 15-b Resolution 2-MHz Nyquist Rate ΣΔ ADC in a 1-µm CMOS Technology". IEEE Journal of Solid-State Circuits, vol. 33, pp. 1065-1075, July 1998.

[Mar98b] A.M. Marques, V. Peluso, M.S.J. Steyaert, and W. Sansen, "Optimal Parameters for ΣΔ Modulator Topologies". IEEE Transactions on Circuits and Systems - II, vol. 45, pp. 1232-1241, September1998.

[Mar02] J. Márkus and G. C. Temes, "An efficient delta-sigma noise-shaping architecture for wideband applications," in Proc. 4th Int. Conf. Advanced A/D and D/A Conversion Techniques and their Applications; 7th Eur. Workshop on ADC Modeling and Testing (ADDA-EWADC 2002), Prague, Czech Republic, June 26–28, 2002, pp. 35–38.

[Mar04] János Márkus, Gabor C. Temes, "An Efficient ΔΣ ADC Architecture for Low Oversampling Ratios"IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 51, NO. 1, pp. 63-71 JANUARY 2004

[Mat87] Y. Matsuya, K. Uchimura, A. Iwata, T. Kobayashi, M. Ishikawa, and T. Yoshitome, "A 16-bit oversampling A-to-D conversion technology using triple-integration noise shaping". IEEE Journal of Solid-State Circuits, vol. 22, pp. 921-929, December 1987.

[Mau00] P.C. Maulik, M.S. Chadha, W.L. Lee, and P.J. Crawley, “A 16-Bit 250-kHz Delta-Sigma Modulator and Decimation Filter”. IEEE Journal of Solid-State Circuits, vol. 35, pp. 458-467, April 2000.

[Med94] F. Medeiro, B. Perz-Verdu, A. Rodriquez-Vazquez, and J.L. Huertas “Modeling OpAmp-Induced Harmonic Distortion for Switched-Capacitor ΣΔ modulator Design,” *IEEE ISCAS1994*, pp. 445–448, Jun. 1994.

[Med95] F. Medeiro, B. Pérez-Verdú, A. Rodríguez-Vázquez, and J.L. Huertas, “A Vertically-Integrated Tool For Automated Design of ΣΔ Modulators”. IEEE Journal of Solid-State Circuits, vol. 30, pp. 762-772, August 1995.

[Med98a] F. Medeiro, B. Pérez-Verdú, J.M. de la Rosa, and A. Rodríguez-Vázquez, “Multi-bit cascade ΣΔ modulator for high-speed A/D conversion with reduced sensitivity to DAC errors”. Electronics Letters, vol. 34, pp. 422-424, March 1998.

[Med98b] F. Medeiro, B. Pérez-Verdú, J.M. de la Rosa, and A. Rodríguez-Vázquez, “Fourth-Order Cascade ΣΔ Modulators: A Comparative Study”. IEEE Transactions on Circuits and Systems - I, vol. 45, pp. 1041-1051, October 1998.

[Med99a] F. Medeiro, B. Perez-Verdú, and A. Rodríguez-Vázquez, “A 13-bit, 2.2-MS/s, 55-mW Multibit Cascade ΣΔ Modulator in CMOS 0.7-µm Single-Poly Technology”. IEEE Journal of Solid-State Circuits, vol. 34, no. 6, pp. 748-760, June 1999.

[Med99b] F. Medeiro, B. Pérez-Verdú, and A. Rodríguez-Vázquez, “Top-Down Design of High-Performance Modulators.” Kluwer Academic Publishers, 1999.

[Mei82] G. C, M. Meijer, P. C. Schmafe, and K. van Zalinge, “A new curvature-corrected bandgap reference,” *IEEE J. Solid-State Circuits,* vol. *SC-17,* p . 1139–1143, Dec. 1982.

[Mia98] G. Miao, H.C. Yang, and T. Pushan, “An Oversampled A/D Converter Using Cascaded Fourth Order Sigma-Delta Modulation and Current Steering Logic”. Proc. of the IEEE International Symposium on Circuits and Systems, vol. 1, pp. 412-415, 1998.

[Mil03] M.R. Miller and C.S.A. Petrie, “A Multibit Sigma-Delta ADC for Multimode Receivers”. IEEE Journal of Solid-State Circuits, vol. 38, no. 3, pp. 475-482, March 2003.

[Min01] J. Ming, S.H. Lewis, **“**An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration,. *IEEE Journal of Solid-State Circuits*, vol.36, no.10, pp.1489-1497, Oct. 2001.

[Moo97] U.-K. Moon, B.-S. Song, **“**Background digital calibration techniques for pipelined ADCs,. IEEE Transactions on Circuits and Systems II: Analog and Digital Signal *Processing*, vol.44, no.2, pp.102-109, Feb. 1997.

[Moo99] U.-K. Moon, J. Silva, J. Steensgaard, and G. C. Temes, “Switched-capacitor DAC with analogue mismatch correction,” Electron. Lett., vol. 35, pp. 1903–1904, Oct. 1999.

[Moo00] U. Moon, J. Silva, J. Steensgaard, and G. C. Temes, “A switched-capacitor DAC with analog mismatch correction,” in Proc. IEEE Int. Symp. Circuits and Systems (ISCAS’2000), Geneva, Switzerland, May 28–31, 2000, pp. 421–424.

[Mor00] J.C. Morizio, M. Hoke, T. Kocak, C. Geddie, C. Hughes, J. Perry, S. Madhavapeddi, M.H. Hood, G. Lynch, H. Kondoh, T. Kumamoto, T. Okuda, H. Noda, M. Ishiwaki, T. Miki, and M. Nakaya, “14-bit 2.2-MS/s Sigma-Delta ADC’s”. IEEE Journal of Solid-State Circuits, vol. 35, pp. 968-976, July 2000.

[Mot93] C.D. Motchenbacher and J.A. Conelly, Low-Noise Electronic System Design.John Wiley & Sons, 1993.

[Mou94] S.M. Moussavi and B.H. Leung, “High-Order Single-Stage Single-Bit Oversampling A/D Converter Stabilized with Local Feedback Loops”. IEEE Transactions on Circuits and Systems - I, vol. 41, pp. 19-25, January 1994.

[Moy03] M. Moyal.; M Groepl.; , H. Werker; G. Mitteregger,; J. Schambacher , “ A 700/900mW/channel CMOS dual analog front-end IC for VDSL with integrated 11.5/14.5dBm line drivers ,” in ISSCC Dig. Tech.Papers, Feb. 2003, pp. 416 - 504

[Nad94] S. Nadeem, C.G. Sodini, and L. Hae-Seung, “16-Channel Oversampled Analog-to-Digital Converter”. IEEE Journal of Solid-State Circuits, vol. 29, pp. 1077-1085, September 1994.

[Nor88] S. R. Norsworthy, and I. G. Post, "A 13-bit 160 kHz sigma-delta A/D converter for ISDN", in proc. IEEE Custom Integrated Circuits Conference, pp. 21.3.1-21.3.4, 1988.

[Nor97] S.R. Norsworthy, R. Schreier, and G.C. Temes (Editors), Delta-Sigma Data Converters: Theory, Design and Simulation. IEEE Press, 1997.

[Nys96a] O. Nys and R. Henderson, “A monolithic 19 bit 800 Hz low-power multibit sigma delta CMOS ADC using data weighted averaging,” Proc. IEEE Eur. Solid-State Circuits Conf., pp. 252–255, Sept. 1996.

[Nys96b] O. J. A. P. Nys and R. K. Henderson, “An analysis of dynamic element matching techniques in sigma-delta modulation,” in Proc. IEEE ISCAS, May 1996, pp. 231–234.

[Nys97] O. Nys and R. Henderson, “A 19-bit Low-Power Multi-Bit Sigma-Delta ADC Based on Data Weighted Averaging”. IEEE Journal of Solid-State Circuits, vol. 32, pp.933-942, July 1997.

[Oli00] O. Oliaei, “Thermal Noise Analysis of Multi-Input SC-Integrators for Sigma-Delta Modulator Design”. Proc. of the IEEE International Symposium on Circuits and Systems, vol. 4, pp. 425-428, 2000.

[Oli02] O. Oliaei, P. Clement, and P. Gorisse, “A 5-mW Sigma-Delta Modulator With 84-dB Dynamic Range for GSM/EDGE”. IEEE Journal of Solid-State Circuits, vol. 37, pp. 2-10, January 2002.

[Ono88] H. Onodera, T. Tateishi, K. Tamaru, .A cyclic A/D converter that does not require ratio-matched components,. *IEEE Journal of Solid-State circuits*, vol.23, no.1, pp.152-158, Feb. 1988.

[Opp99] A.V. Oppenheim, R.W. Shafer, J.R.Buck, *Discrete-time signal processing,* Upper Saddle River, New Jersey, Prentice Hall 1999.

[Opt91] F. Op’t Eynde, G.M. Yin, and W. Sansen, “A CMOS Fourth-order 14b 500ksample/s Sigma-delta ADC Converter”. Proc. of IEEE International Solid-State Circuit Conference, pp. 62-63, 1991.

[Pan00] H. Pan et al, "A 3.3-V 12-b 50-MS/s A/D converter in 0.6um CMOS with over 80-dB SFDR", IEEE Journal of Solid-State Circuits, vol. 35, pp. 1769-80, Dec. 2000.

[Par03] Y.-I. Park et al., “A 16-bit, 5-MHz multi-bit sigma-delta ADC using adaptively randmoized DWA,” in Proc. IEEE Custom Integrated Circ.Conf., Sept. 2003, pp. 7-2-1–7-2-4.

[Pau87] J.J. Paulos, G.T. Brauns, M.B. Steer, and S.H. Ardalan, “Improved signal-tonoise ratio using tri-level delta-sigma modulation”. Proc. of the IEEE International Symposium on Circuits and Systems, pp. 463-466, 1987.

[Pee86] B. Peetz, B.D. Hamilton and J. Kan, “An 8-bit 250 Megasample per Second Analog-to-Digital Converter: Operation Without a Sample and Hold”, JSSC, vol. 21, no. 6, December 1986.

[Pel97] V. Peluso, M. Steyaert, and W. Sansen, “A 1.5-V 100µ-W ¥Ò. Modulator with 12-bit Dynamic Range Using the Switched-Opamp Technique”. IEEE Journal of Solid-State Circuits, vol. 32, pp. 943-952, July 1997.

[Pel98] V. Peluso, P. Vancorenland, A.M. Marques, M.S.J. Steyaert, and W. Sansen, “A 900-mV Low-Power .Ó A/D Converter with 77-dB Dynamic Range”. IEEE Journal of Solid-State Circuits, vol. 33, pp.1887-1897, December 1998.

[Pet00] C. Petrie and M. Miller, “A background calibration technique for multibit delta-sigma modulators,” in Proc. IEEE ISCAS, May 2000, pp. 29–32.

[Phi03] K. Philips, "A 4.4mW 76dB complex Sigma Delta ADC for bluetooth receivers", in proc. IEEE International Solid-State Circuits Conference, pp. 64-65, 2003.

[Pla94] R. van de Plassche, “Integrated Analog-to-Digital and Digital-to-Analog converters”, Kluwer Academic Pub., Netherlands, 1994, pp.178-179.

[Pla03] R. van de Plassche, CMOS integrated analog-to-digital and digital-to-analog *Converter*. 2nd edition, Netherlands, Kluwer Academic Publishers, 2003.

[Pou02] K. Poulton et al, "A 4GSamples/s 8b ADC in 0.35um CMOS", in proc. IEEE International Solid-State Circuits Conference, pp. 166-167, 2002.

[Pre98] L. Lo Presti and A. Akhdar, “Efficient antialiasing decimation filter for ΣΔ converters,” in Proc. th IEEE Int. Conf. Electronics, Circuits, and Systems (ICESC ’98), vol. 1, Lisboa, Portugal, Sept. 7-10, 1998, pp. 367–370.

[Pre00] L. Lo Presti, “Efficient modified-sinc filters for sigma-delta A/D converters,” IEEE Trans. Circuits Syst. II, vol. 47, pp. 1204–1213, Nov. 2000.

[Qin99] W. Qin, B. Hu, and X. Ling, “Sigma-deltaADCwith reduced sample rate ´ multibit quantizer,” IEEE Trans. Circuits Syst. II, vol. 46, pp. 824–828, June 1999.

[Rab97] S. Rabii and B.A. Wooley, “A 1.8V Digital-Audio Sigma-Delta Modulator in 0.8μm CMOS”. IEEE Journal of Solid-State Circuits, vol. 32, pp. 783-796, June 1997.

[Rab98] S. Rabii, .Design of low-voltage low power sigma-delta modulators,. Ph.D. Dissertation, Stanford University, 1998

[Rad00] R. E. Radke, A. Eshraghi, and T. S. Fiez, “A 14-bit current-mode ΣΔ DAC based upon rotated data weighted averaging,” IEEE J. Solid-State Circuits, vol. 35, pp. 1074–1084, Aug. 2000.

[Raz92] B. Razavi, B. A. Wooley, .Design Techique for high speed, high resolution comparators,. *IEEE Journal of Solid-State Circuits*, vol. 27, no. 12, pp.1916-1926, Dec. 1992

[Raz95] B. Razavi, Principles of Data Converter System Design. IEEE Press, 1995.

[Raz00] B. Razavi, Design of Analog CMOS Integrated Circuits. McGraw-Hill, 2000.

[Reb89] M. Rebeschini et al, "A high-resolution CMOS sigma-delta A/D converter with 320 kHz output rate", in proc. International Symposium on Circuits and Systems, pp. 246-249, 1989.

[Reb90] M. Rebeschini, N.R. van Bavel, P. Rakers, R. Greene, J. Caldwell, J.R. Haug, “A 16-b 160 kHz CMOS A/D Converter using Sigma-Delta Modulation”. IEEE Journal of Solid-State Circuits, vol. 25, pp. 431-440, April 1990.

[Reb97] M. Rebeschini, “The Design of Cascaded ΣΔ. ADCs”, Chapter 6 in Delta-Sigma Data Converters: Theory, Design and Simulation (S.R. Norsworthy, R. Schreier, and G.C. Temes, Editors). IEEE Press, 1997.

[Red94] W. Redman-White and A.M. Durham, “Integrated fourth-order ΣΔ Convertor with stable self-tuning continuous-time noise shaper”. IEE

Proceedings -Circuits, Devices and Systems, vol. 141, pp. 145-150, June 1994.

[Reu02] R. Reutemann, P. Balmelli, and Q. Huang, “A 33mW 14b 2.5MSample/s ΣΔA/D converter in 0.25µm digital CMOS”. Proc. of IEEE International Solid-State Circuits Conference, vol. 1, p. 316, 2002.

[Rev03] R. Le Reverend, I. Kale, G. Delight, D. Morling, and S. Morris, “An Ultra-Low Power Double-Sampled A/D MASH ΣΔ Modulator”. Proc. of the IEEE International Symposium on Circuits and Systems, vol. 1, pp. 1001-1004, 2003.

[Rhe00] W. Rhee, A. Ali, and B. Song, “A 1.1GHz CMOS fractional-N frequency synthesizer with a 3b 3rd-order delta-sigma modulator,” IEEE Journal of Solid-State Circuits S, vol. 35, pp. 1453-1460 October 2000

[Rit90] T. Ritoniemi, T. Karema, and H. Tenhunen, "The design of stable high order 1-bit Sigma Delta modulators", in proc. IEEE International Symposium on Circuits and Systems, vol. 4, pp. 3267-70, 1990.

[Rib91a] D.B. Ribner, “A Comparison of Modulator Networks for High-Order Oversampled ΣΔ Analog-to-Digital Converters”. IEEE Transactions on Circuits and Systems, vol. 38, pp. 145-159, February 1991.

[Rib91b] D.B. Ribner, R.D. Baertsch, S.L. Garverick, D.T. McGrath, J.E. Krisciunas, and T. Fuji, “A Third-Order Multistage Sigma-Delta Modulator with Reduced Sensitivity to Nonidealities”. IEEE Journal of Solid-State Circuits, vol. 26, pp.1764-1774, December 1991.

[Rit94] T. Ritoniemi et al, "A stereo audio Sigma-Delta A/D converter", IEEE Journal of Solid-State Circuits, vol. 29, pp. 1514-23, Dec. 1994.

[Rio98] R. del Río, F. Medeiro, B. Pérez-Verdú, and A. Rodríguez-Vázquez, “High-Order Cascade Multi-bit ΣΔ Modulators for High-Speed A/D Conversion”.Proc. of the Design of Circuits and Integrated Systems Conference, pp. 76-81, 1998.

[Rio99] R. del Río, F. Medeiro, J.M. de la Rosa, B. Pérez-Verdú, and A. Rodríguez-Vázquez, “Reliable Analysis of Settling Errors in SC Integrators – Application to High-Speed Low-Power Sigma-Delta Modulators”. Proc. of

the Design of Circuits and Integrated Systems Conference, pp. 727-732, 1999.

[Rio00a] R. del Río, F. Medeiro, B. Pérez-Verdú, and A. Rodríguez-Vázquez, "Highorder cascade multibit ΣΔ modulators for xDSL applications". Proc. of the IEEE International Symposium on Circuits and Systems, vol. 2, pp. 37-40, 2000.

[Rio00b] R. del Río *et al.*, "Reliable analysis of settling errors in SC integrators Application to the design of high-speed ΣΔ Modulators," IEEE ISCAS 2000 pp. IV417 –IV420, May. 2000.

[Rio01a] R. del Río, J.M. de la Rosa, F. Medeiro, B. Pérez-Verdú, and A. Rodríguez-Vázquez, "Top-down Design of a xDSL 14-bit 4-MS/s Sigma-Delta Modulator in Digital CMOS Technology". Proc. of the Design, Automation and Test in Europe Conference, pp. 348-351, 2001.

[Rio01b] R. del Río, J.M. de la Rosa, F. Medeiro, B. Pérez-Verdú, and A. Rodríguez-Vázquez, "High-performance sigma-delta ADC for ADSL applications in 0.35µm CMOS digital technology". Proc. of the IEEE International Conference on Electronics, Circuits and Systems, vol. 1, pp. 501-504, 2001.

[Rio02a] R. del Río, F. Medeiro, J.M. de la Rosa, B. Pérez-Verdú, and A. Rodríguez-Vázquez, "Correction-Free Multi-Bit Sigma-Delta Modulators for ADSL", in Analog Circuit Design — Structured Mixed-Mode Design, Multi-Bit Sigma-Delta Converters, Short Range RF Circuits (M. Steyaert, A.H.M. van Roermund, and J.H. Huijsing, Editors). Kluwer Academic Publishers, 2002.

[Rio04a] R. del Río, J.M. de la Rosa, B. Pérez-Verdú, M. Delgado-Restituto, R. Domínguez-Castro, F. Medeiro, and A. Rodríguez-Vázquez, "Highly Linear 2.5-V CMOS ΣΔ Modulator for ADSL+". IEEE Transactions on Circuits and Systems - I, vol. 51, pp. 47-62, January 2004.

[Rio04b] R. del Río, "Convertidores A/D ΣΔ de Altas Prestaciones en Tecnologías CMOS Submicrométricas ". Dissertation 2004. DE SEVILLA, IMSE-CNM (CSIC) INSTITUTO DE MICROELECTRÓNICA, UNIVERSIDAD D SEVILLA

[Rit77] G.R. Ritchie, High Order Interpolation Analog-to-Digital Converters. Ph.D.Thesis, University of Pennsylvania, 1977.

[Rit90] T. Ritoniemi, T. Karema, and H. Tenhunen, “Design of stable high-order 1-bit sigma–delta modulators,” in Proc. IEEE Int. Symp. Circuits and *Systems*, May 1990, pp. 3267–3270.

[Rit94] T. Ritoniemi, E. Pajarre, S. Ingalsuo, T. Husu, V. Eerola, and T. Saramiki, “A Stereo Audio Sigma-Delta A/D-Converter”. IEEE Journal of Solid-State Circuits, vol. 29, pp. 1514-1523, December 1994.

[Rob88] J. Robert and P. Deval, “A second-order high-resolution incremental A/D converter with offset and charge injection compensation,” IEEE J. Solid-State Circuits, vol. 23, pp. 736–741, June 1988.

[Rob91] A. Robertini, Linear and Nonlinear Distortion in SC Circuits due to Nonideal Amplifiers and Switches. Hartung-Gorre Verlag, 1991.

[Rob92] A. Robertini and W. Guggenb¨uhl, “Errors in SC circuits derived from linearly modeled amplifiers and switches,” *IEEE Trans. Circuits Syst. I*, vol. 39, pp. 93–101, Feb. 1992.

[Rod99] A. Rodríguez-Vázquez, M. Delgado-Restituto, and R. Domínguez-Castro, “Comparator Circuits”, in Wiley Encyclopedia of Electrical and Electronics Engineering (J.G. Webster, Editor). John Wiley & Sons, 1999.

[Rom01] P. Rombouts, W. de Wilde, and L. Weyten, “A 13.5-b 1.2-V Micropower Extended Counting A/D Converter”. IEEE Journal of Solid-State Circuits, vol. 36, pp. 176-183, February 2001.

[Sal01] T. Salo, S. Lindfors, and K. Halonen, "A 80MHz Band-Pass Sigma Delta Modulator for a 100MHz IF-receiver", in proc. European Solid-State Circuits Conference, pp. 528-531, 2001.

[San87] W.M.C. Sansen, H. Qiuting, and K.A.I. Halonen, “Transient Analysis of Charge Transfer in SC Filters - Gain Error and Distortion”. IEEE Journal of Solid-State Circuits, vol. 22, pp. 268-276, April 1987.

[San99] W. Sansen, “Distortion in elementary transistor circuits,” *IEEE Trans.Circuits Syst. II*, vol. 46, pp. 315–325, Mar 1999.

[Sen82] D. Senderowicz, S. F. Dreyer, J. H. Huggins, C. F. Rahim, and C. A. Laber, “A family of differential NMOS analog circuits for a PCM codec filter chip,” *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 1014–1023, Dec. 1982.

[Sar88] T. Saramaki, and H. Tenhunen, "Efficient VLSI-realizable decimators for sigma-delta analog-to-digital converters"", in proc. International Symposium on circuits and systems, vol. 2, pp. 1525-28, 1988.

[Sar90] T. Saramaki, and H. Tenhunen, "Multiplier-free decimator algorithms for superresolution oversampled converters", in proc. International Symposium on circuits and systems, vol. 4, pp. 3275 -78, 1990.

[Sar93] M. Sarhang-Nejad and G.C. Temes, “A High-Resolution ΣΔ ADC with Digital Correction and Relaxed Amplifiers Requirements”. IEEE Journal of Solid-State Circuits, vol. 28, pp. 648-660, June 1993.

[Sau02] J. Sauerbrey, T. Tille, D. Schmitt-Landsiedel, and R. Thewes, “A 0.7-V MOSFET-Only Switched-Opamp ΣΔ Modulator in Standard Digital CMOS Technology”. IEEE Journal of Solid-State Circuits, vol. 37, pp. 1662-1669, December 2002.

[Sau03] J. Sauerbrey, M. Wittig, D. Schmitt-Landsiedel, and R. Thewes, “0.65V Sigma-Delta Modulators”. Proc. of the IEEE International Symposium on Circuits and Systems, vol. 1, pp. 1021-1024, 2003.

[Sch88] R. Schreier, ftp://next242.ece.orst.edu/pub/delsig.tar.Z.

[Sch93] R. Schreier, “An Empirical Study of Higher Order Single Bit Sigma Delta Modulators”. IEEE Transactions on Circuits and Systems - II, vol. 40, pp. 461-466, August 1993.

[Sch94] M.C. Schneider, C. Galup-Montoro, and J.C.M. Bermudez, “Explicit formula for harmonic distortion in SC filters with weakly nonlinear capacitors”. IEE Proceedings - Circuits, Devices and Systems, vol. 141, no. 6, pp. 505-509, December 1994.

[Sch95] R. Schreier and B. Zhang, “Noise-shaped multibit D/A converter employing unit elements”. Electronics Letters, vol. 31, pp. 1712-1713, September 1995.

[Sch97] R. Schreier, “Mismatch-shaping digital-to-analog conversion,” in Proc. 103rd Conv. Audio Eng. Soc., Sept. 1997, Preprint no. 4529, pp. 1–27.

[Sch02] R. Schreier et al, "A 50 mW bandpass Sigma Delta ADC with 333 kHz BW and 90 dB DR", in proc. IEEE International Solid-State Circuits Conference, pp. 216-217, 2002.

[Sch03] R. Schreier. (2003) The Delta-Sigma Toolbox v6.0 (Delsig). [Online]. Available: http://www.mathworks.com/matlabcentral/fileexchange/

[Sch05] R. Schreier, J. Silva, J. Steensgaard, G. C. Temes "Design-Oriented Estimation of Thermal Noise in Switched-Capacitor Circuits" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 52, pp. 2358-2368 , NOVEMBER 2005.

[Sen82] D. Senderowicz et al, .A family of differential NMOS analog circuits for a PCM Codec Filter Chip,. *IEEE Journal of Solid-State Circuits*, vol. Sc-17, no.6, pp.1014- 1023 Dec. 1982

[Sen97] D. Senderowicz, G. Nicollini, S. Pernici, A. Nagari, P. Confalonieri, and C. Dallavalle, "Low-Voltage Double-Sampled ΣΔ Converters". IEEE Journal of Solid-State Circuits, vol. 32, pp. 1907-1919, December 1997.

[Sen98] S. Sen, and B. Leung, "A 150 MHz 13b 12.5 mW IF digitizer", in proc. IEEE Custom Integrated Circuits, pp. 233-236, 1998.

[Sha49] C. E. Shannon, "Communication in the presence of noise", in proc. IRE, pp. 37:10-21, 1949.

[Shi86] C. Shih, P.R. Gray, **"**Reference refreshing cyclic analog-to-digital and digital-to-analog converters,. *IEEE Journal of Solid-State Circuits*, vol.SC-21, no.4, pp.544-554, Aug. 1986.

[Shu95] T.-H. Shu, B.-S. Song, K. Bacrania, **"**A 13-b 10-Msample/s ADC digitally calibrated with oversampling Delta-Sigma converter,. *IEEE Journal of Solid-State Circuits*, vol.30, no.4, pp.443-452, Apr. 1995.

[Sil01] J. Silva, U.-K. Moon, J. Steensgaard, and G. C. Temes, "Wideband low-distortion delta-sigma ADC topology," Electron. Lett., vol. 37, pp. 737–738, Jun. 2001.

[Sil02] J. Silva et al, "Digital techniques for improved Delta Sigma data conversion", in proc. IEEE Custom Integrated Circuits Conference, pp. 183-190, 2002.

[SIM97] *SIMULINK and MATLAB Users Guides*, The MathWorks, Inc., Natick, MA, 1997.

[Sno01] M.F. Snoeij, O. Bajdechi, and J.H. Huijsing, "A 4th-order switched-capacitor sigma-delta A/D converter using a high-ripple Chebyshev loop

filter". Proc. Of the IEEE International Symposium on Circuits and Systems, vol. 1, pp. 615-618, 2001.

[Son88] B.-S. Song, M. F. Tompsett, K. R. Lakshmikumar, .A 12-bit 1-Msample/s capacitor error-averaging pipelined A/D converter,. *IEEE Journal of Solid-State Circuits*, vol.23, no.6, pp.1324-1333, Dec. 1988.

[Son00] S. Sonkusale, J. van der Spiegel, K. Nagaraj, **"**True background calibration technique for pipelined ADC,. *IEE Electronics Letters*, vol.36, no.9, pp.786-788, 27th Apr. 2000.

[Sri77] A.B. Sripad and D.L. Snyder, "A necessary and sufficient condition for quantization errors to be uniform and white". IEEE Trans. Acoust., Speech, Signal Processing, vol. ASSP-25, pp. 442-448, October 1977.

[Ste98] J. Steensgaard, "Nonlinearities in SC delta-sigma A/D converters," Proc. IEEE ICECS, pp. 355–358, May 1998.

[Ste99] J. Steensgaard-Madsen, High-Performance Data Converters, Ph.D. thesis, The Technical University of Denmark, Department of Information Technology, March 8, 1999.

[Sti88] E.F. Stikvoort, "Some remarks on the stability and performance of the noise shaper or Sigma-Delta modulator". IEEE Transactions on Communications. vol. 36, pp. 1157-1162, October 1988.

[Sut88] S. Sutarja, P.R. Gray, **"**A pipelined 13-bit 250-ks/s 5-V analog-to-digital converter,.*IEEE Journal of Solid-State Circuits*, vol.23, no.6, pp.1316-1323, Dec. 1988.

[Tab00] A. Tabatabaei and B. A. Wooley, "A two-path bandpass sigma–delta modulator with extended noise shaping," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1799–1809, Dec. 2000.

[Tao99] H. Tao and J. M. Khoury, "A 400-Ms/s frequency translating bandpass sigma–delta modulator," *IEEE J. Solid-State Circuits*, vol. 34, pp.1741–1752, Dec. 1999.

[Tan93] N. Tan and S. Eriksson, "Fourth-order two-stage delta-sigma modulator using both 1 bit and multibit quantisers". Electronics Letters, vol. 29, pp. 937-938, May 1993.

[Tem80] G. Temes, “Finite gain and bandwidth effects in SC filters,” *IEEE J.Solid-State Circuits*, vol. SC-15, pp. 358–361, June 1980.

[Tha97] C.K. Thanh, S.H. Lewis, and P.J. Hurst, “A second-order double-sampled delta-sigma modulator using individual-level averaging”. IEEE Journal of Solid-State Circuits, vol. 32, pp. 1269-1273, August 1997.

[Tie98] K.-D. Tiepermann, “Understand the basics of WCDMA signal generation,” *Microw. RF*, no. 12, pp. 83–86, Dec. 1998.

[Til01] T. Tille, J. Sauerbrey, and D. Schmitt-Landsiedel, “A 1.8-V MOSFET-Only Sigma-Delta Modulator Using Substrate Biased Depletion-Mode MOS Capacitors in Series Compensation”. IEEE Journal of Solid-State Circuits, vol. 36, pp. 1041-1047, July 2001.

[Tui96] H. Tuinhout, M. Pelgram, R. Penning de Vries, M. Vertregt,.Effects of metal coverage on OSFET matching,. *IEEE IEDM*, 1996

[Uen02] T. Ueno, A. Yasuda, T. Yamaji, and T. Itakura, "A fourth order bandpass Sigma-Delta modulator using second order bandpass noise-shaping dynamic element matching", IEEE Journal of Solid-State Circuits, vol. 37, pp. 809-816, July 2002.

[Vad00] M. Vadipour, “Techniques for preventing tonal behavior of data weighted averaging algorithm in ΣΔ modulators,” IEEE Trans. Circuits Syst. II, vol. 47, pp. 1137–1144, Nov. 2000.

[Vai90] P.P. Vaidyanathan, “Multirate digital filters, filter banks, polyphase networks, and applications: a tutorial”. Proceeding IEEE, vol. 78, January 1990.

[Van00] E. J. van der Zwan, K. Philips, and C. A. A. Bastiansen, “A 10.7-MHz IF-to-baseband ΣΔ A/D conversion system for AM/FM radio receivers,” *IEEE J. Solid-State Circuits*, vol. 35, pp. 1810–1819, Dec. 2000.

[Vel02] R.H.M. van Veldhoven, B.J. Minnis, H.A. Hegt, and A.H.M. van Roermund, “A 3.3-mW ΣΔ Modulator for UMTS in 0.18-µm CMOS With 70-dB Dynamic Range in 2-MHz Bandwidth”. IEEE Journal of Solid-State Circuits, vol. 37, pp. 1645-1652, December 2002.

[Vel03] R. Veldhoven, "A Tri-mode continuous time Sigma Delta modulator with switched-capacitor DAC for a GSM-EDGE/CDMA2000/UMTS receiver",

in proc. IEEE International Solid-State Circuits Conference, pp. 60-61, 2003.

[Vel03] R. Veldhoven, "A Tri-mode continuous time Sigma Delta modulator with switched-capacitor DAC for a GSM-EDGE/CDMA2000/UMTS receiver", in proc. IEEE International Solid-State Circuits Conference, pp. 60-61, 2003.

[Ver93] N. K. Vergehese, D. J. Allstot, and S. Masui, "Rapid simulation of substrate coupling effects in mixed-mode ICs", in proc. IEEE Custom Integrated Circuits conference, pp. 18.3.1-18.3.4, 1993.

[Ver96] N. K. Verghese, D. J. Allstot, and M. A. Wolfe, "Verification techniques for substrate coupling and their application to mixed-signal IC design", IEEE Journal of Solid State Circuits, vol. SC-31, pp. 354-65, Mar. 1996.

[Vle01] K. Vleugels, S. Rabii, and B. Wooley, “A 2.5-V Sigma-Delta Modulator for Broadband Communications Applications”. IEEE Journal of Solid-State Circuits, vol. 36, pp. 1887-1899, December 2001.

[Wal90] R.H. Walden, T. Cataltepe, and G.C. Temes, “Architectures for higher-order multi-bit ΣΔ modulators”. Proc. of the IEEE International Symposium Circuits and Systems, vol. 5, pp. 895-898, 1990.

[Wal02] Mikko Waltari, “CIRCUIT TECHNIQUES FOR LOW-VOLTAGE AND HIGH-SPEED A/D CONVERTERS” Helsinki University of Technology, Electronic Circuit Design Laboratory, Report 33, Espoo 2002

[Wan92] H. Wang, "A geometric view of Sigma-Delta modulations", IEEE Trans. Circuits and Systems II: Analog Digital Signal Processing, vol. 39, pp. 402-405, June 1992.

[Wan97] F. Wang and R. Harjani, “Nonlinear Settling Behavior in Oversampled Converters”. Proc. of the IEEE Custom Integrated Circuits Conference, pp. 23.6.1-4, 1997.

[Wan00] X. Wang, W. Quin, and X. Ling, “Cascaded Parallel Oversampling Sigma-Delta Modulators”. IEEE Transactions on Circuits and Systems - II, vol. 47, pp. 156-161, February 2000.

[Wan01a] X. Wang, P. Kiss, U. Moon, J. Steensgaard, and G. C. Temes, “Digital estimation and correction of DAC errors in multibit ΣΔ ADCS,” Electron. Lett., vol. 37, pp. 414–415, Mar. 2001.

[Wan01b] C.B. Wang, “A 20-bit 25-kHz delta-sigma A/D converter utilizing a frequencyshaped chopper stabilization scheme”. IEEE Journal of Solid-State Circuits, vol. 36, pp. 566-569, March 2001.

[Wan 02] X. Wang, U. Moon, M. Liu, and G. C. Temes, “Digital correlation technique for the estimation and correction of DAC errors in multibit MASH ΣΔ ADCS,” in Proc. IEEE ISCAS, May 2002, pp. IV 691–694.

[Wan03] X. Wang, P.J. Hurst, S. Lewis,.A 12-bit 20MS/s pipelined ADC with nested digital background calibration,. IEEE Proceedings of CICC, Sept 2003

[Welz01] J. Welz, I. Galton, and E. Fogleman, “Simplified logic for first-order and second-order mismatch-shaping digital-to- analog converters,” IEEE Trans. Circuits Syst. II, vol. 48, pp. 1014–1026, Nov. 2001.

[Wid56] B. Widrow, "A study of rough amplitude quantization by means of nyquist sampling theory", IRE transcation on circuit Theory, vol. CT-3, pp. 266-276, 1956

[Wid60] B. Widrow, “Statistical analysis of amplitude-quantized sample-data systems”. Trans. AIEE - Part II: Applications and Industry, vol. 79, pp. 555-568, January 1960.

[Wie96] A. Wiesbauer and G.C. Temes, “Adaptive compensation of analog circuit imperfections for cascaded ΣΔ modulators”. Proc. of the Asilomar Conference on Signals, Systems and Computers, vol. 2, pp. 1073-1077, 1996.

[Wie99] A. Wiesbauer, H. Weinberger, M. Clara, and J. Hauptmann, “A 13.5-bit cost optimized multi-bit delta-sigma ADC for ADSL,” in Proc. Eur. Solid-State Circ. Conf., Sept. 1999, pp. 82–88.

[Wid71] R. J. Widlar, “New developments in IC voltage regulators,” *IEEE* J. Solid-State Circuits, vol. SC-6, pp. 2-7, Feb. 1971.

[Wil91] L.A. Williams III and B.A. Wooley, “Third-Order Cascaded Sigma-Delta Modulators”. IEEE Transactions on Circuits and Systems, vol. 38, pp. 489-498, May 1991.

[Wil93] L. Williams, Modeling and design of high resolution sigma-delta modulators, PhD Dissertation, Stanford University, 1993

[Wil94] L.A. Williams and B.A. Wooley, “A Third-Order Sigma-Delta Modulator with Extended Dynamic Range”. IEEE Journal of Solid-State Circuits, vol. 29, pp. 193-202, March 1994.

[Wu98] J.-T. Wu and K.-L. Chang, “MOS Charge Pumps for Low-Voltage Operation”. IEEE Journal of Solid-State Circuits, vol. 33, no. 4, pp. 592-597, April 1998

[Yam94] K. Yamamura, A. Nogi, and A. Barlow, “A low power 20 bit instrumentation delta-sigma ADC”. Proc. of the IEEE Custom Integrated Circuits Conference, pp. 519-522, 1994.

[Yan03a] Y. Yang, A. Chokhawala, M. Alexander, J. Melanson, D Hester, .A 114dB 68mW chopper-stabilized stereo multi-bit audio A/D converter,. *ISSCC Digest of technical papers,* pp.56-57, Feb. 2003.

[Yan03b] S. Yan and E. Sanchez-Sinencio, “A continuous-time ΣΔ modulator with 88 dB dynamic range and 1.1 MHz signal bandwidth,” in ISSCC Dig. Tech. Papers, Feb. 2003, pp. 62–63.

[Yin90] G. Yin, F. Op’t Eynde, and W. Sansen, “A high-speed CMOS comparator with 8-b resolution,” *IEEE J. Solid-State Circuits*, vol. 27, pp.208–211, Dec. 1990.

[Yin92] G.M. Yin, F. Op’t Eynde, and W. Sansen, “A High-Speed CMOS Comparator with 8-b Resolution”. IEEE Journal of Solid-State Circuits, vol. 27, pp. 208- 211, February 1992.

[Yin93] G. Yin, F. Stubbe, and W. Sansen, “A 16-b 320-kHz CMOS A/D Converter Using Two-Stage Third-Order ΣΔ Noise Shaping”. IEEE Journal of Solid-State Circuits, vol. 28, pp. 640-647, June 1993.

[Yin94] G. Yin and W. Sansen, “A High-Frequency and High-Resolution Fourth-Order ΣΔ A/D Converter in BiCMOS Technology”. IEEE Journal of Solid-State Circuits, vol. 29, pp. 857-865, August 1994.

[Yin04] Y. Yin, H. Klar, P Wennekers, *“A Novel Broadband Cascaded Sigma-Delta Analog-to-Digital Converter”* Proc. The IASTED International Conference on on Circuits, Signals, and Systems (CSS 2004), Nov.-Dec 2004, Clearwater Beach, Florida, USA, (pp.86-91)

[Yin05a] Y. Yin, H. Klar, P. Wennekers, “A CASCADE 3-1-1 MULTIBIT ΣΔ MODULATOR WITH REDUCED SENSITITIES TO NON-IDEALITIES,” *IEEE ISCAS2005*, pp. 3087–3090, May. 2005.

[Yin05b] Y. Yin, H. Klar, P. Wennekers, “A 8X Oversampling Ratio, 14bit, 5-MSamples/s Cascade 3-1Sigma-delta Modulator,” Advances in Radio Science, 3, 277–280, 2005

[Yin06a] Y. Yin, H. Klar, P. Wennekers, “A Wideband Low-Power Cascade ∑Δ Modulator Based on the Considerations of Integrator Settling Behavior,” In Proceedings of the 5th WSEAS Int. Conf. on Instrumentation, Measurement, Circuits and Systems (IMCAS '06), pp. 112-116, April, 2006.

[Yin06b] Y. Yin, H. Klar, “Wideband SC-Sigma-Delta Modulator Topology with Relaxed Requirement on Integrator Settling,” WSEAS TRANSACTIONS ON CIRCUITS AND SYSTEMS, Issue 4 vol. 5, pp. 499-504, 2006

[Yoo98] S.H. Yoon and H.S.M. Rezaul, “A sixth-order CMOS sigma-delta modulator”.Proc. of the IEEE International ASIC Conference, pp. 63-66, 1998.

[Yos84] Y. Yoshii, K. Asano, M. Nakamura and C. Yamada, “An 8 Bit, 100Ms/s Flash ADC”, IEEE JSSC, vol. 19, no. 6, December 1984.

[Yu99] W. Yu, S. Sen, and B.H. Leung, “Distortion Analysis of MOS Track-and-Hold Sampling Mixers Using Time-Varying Volterra Series”. IEEE Transactions on Circuits and Systems - II, vol. 46, pp. 101-113, February 1999.

[Yuk85] A. Yukawa, “A CMOS 8-bit High-Speed Converter IC”. IEEE Journal of Solid-State Circuits, vol. 20, pp. 775-779, June 1985.

[Zho01] J. Zhou, M. Cheng, and L. Forbes, “SPICE Models for Flicker Noise in p-MOSFETs in the Saturation Region”. IEEE Transactions on Computer-Aided Design of Integrated Circuits, vol. 20, pp. 763-767, June 2001.

[Zha91] Z. Zhang, and G. C. Temes, "Multibit oversmapled Sigma-Delta A/D convertor with nonuniform quantisation", Electronics Letters, vol. 27, no. 6, pp. 528-529, 1991.

[Zwa96] E.J. van der Zwan and E.C. Dijkmans, “A 0.2-mW CMOS ΣΔ Modulator for Speech Coding with 80 dB Dynamic Range”. IEEE Journal of Solid-State Circuits, pp. 1873-1880, December 1996.

[Zwa99] E.J. van der Zwan, R.H.M. van Veldhoven, P.A.C.M. Nuijten, E.C. Dijkmans, and S.D. Swift, “A 13mW 500kHz Data Acquisition IC with 4.5 Digit DC and 0.02% Accurate True-RMS Extraction”. Proc. of the IEEE International Solid-State Circuits Conference, pp. 398-399, 1999.