
Electroabsorption Modulated Lasers and Hybridly Integrated Lasers for Communication and Sensing

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Zusammenfassung

Für die Entwicklung photonischer Komponenten bietet die photonische Integration ein immenses Innovationspotential. Mit neuen technologischen Integrationslösungen trägt diese Arbeit dazu bei, dieses Potential auszuschöpfen. Es werden zum einen auf III-V-Halbleiter basierende elektroabsorptionsmodulierte Laser (EMLs) mit monolithisch integrierten optischen Halbleiterverstärkern (engl. semiconductor optical amplifiers - SOAs) weiterentwickelt, zum anderen wird ein Prozess für die hybride Integration von auf III-V basierten photonischen Komponenten mit der auf SiN basierenden photonischen Plattform TriPleX entwickelt.

Die EMLs mit integrierten SOAs werden mit identischem aktivem Schichtpaket realisiert, was eine kostengünstige Fabrikation ermöglicht. Ausgehend von Simulationen und experimentellen Ergebnissen werden relevante Designparameter identifiziert und entsprechende Leistungskompromisse evaluiert. Ein Einzeltransmitter-EML mit integriertem SOA wird vorgestellt, welcher die hohen Anforderungen an Ausgangsleistung und Extinktionsverhältnis von passiven optischen Netzwerken (PONs) erfüllt. Ein EML-Array mit integrierten SOAs wird als kompakte und kostengünstige Lösung für 200-Gbit/s Transmitter demonstriert.

Es wird erstmalig ein generischer Prozess der hybriden Integration vorgestellt, welcher eine Flip-Chip-Montage von auf III-V basierten Komponenten zu SiN TriPleX auf Wafer-Maßstab erlaubt. Der Prozess verwendet mechanische Auflageflächen mit epitaktisch präzisen Dimensionen für eine passive vertikale Justage. Für die horizontale Ausrichtung wird ein neuartiges Justageverfahren vorgestellt. Dabei wird ein reflektiertes optisches Signal für die aktive Justage genutzt, wodurch auf die sonst notwendige elektrische Kontaktierung verzichtet werden kann. Der hybride Integrationsprozess wird für DFB-Laser (engl. distributed feedback laser), DFB-Laser-Arrays, Gain-Chips und EML-Arrays demonstriert.

Abstract

Photonic integration offers great innovation potential for the development of photonic components. This work explores this potential by investigating III-V based electroabsorption modulated lasers (EMLs) with monolithically integrated semiconductor optical amplifiers (SOAs) and by developing a III-V to SiN TriPleX hybrid integration process.

The EMLs with integrated SOAs are realized with a low-cost identical active layer design. Based on simulations and experimental results, critical design parameters are identified and the corresponding performance tradeoffs are evaluated. A single transmitter EML with integrated SOA is presented, which meets the high output power and extinction ratio requirements of passive optical network (PON) applications. An EML array with integrated SOAs is demonstrated as a compact low-cost solution for 200 Gbit/s transmitter.

For the first time, a generic hybrid integration process that is compatible with wafer-scale flip-chip integration of III-V to SiN TriPleX is developed. It comprises mechanical alignment stops with epitaxial precise dimensions for passive vertical alignment. For the horizontal alignment, a novel active alignment method is presented. It utilizes optical backscatter reflectometry, which allows overcoming the electrical contacting limitations of classical active alignment. The flip-chip hybrid integration process is demonstrated for distributed feedback (DFB) lasers, DFB laser arrays, gain chips, and EML arrays.

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1. Introduction

1.1 Motivation

The beginning of the digital revolution in the late 20th century has marked the start of a new historical period known as the information age. The information age is characterized by a momentous technological shift from conventional industrial technology towards information technology with significant economic and social consequences. The foundation of this evolution was the invention of the integrated circuit (IC) [1], [2], which allowed mass production of information processing technology, and the development of the internet, which enabled worldwide information transmission. The integrated circuit and a majority of the photonic components required for digital communication are based on semiconductor material systems. With the widespread use of integrated circuits for complex electronic functionalities in nearly every modern electronic device, a gigantic silicon-based complementary metal-oxide-semiconductor (CMOS) industry has evolved. On a much smaller but technologically highly advanced scale, the III-V semiconductor industry evolved around photonic components required for fiber-optic communication. In contrast to silicon-based material systems, III-V compound semiconductors comprise direct bandgap materials that allow light absorption and emission at the telecommunication wavelengths. The third big column defining the information age next to information processing and information transmission is information acquisition. The key element for information acquisition is sensing, either via human senses or via sensor devices. Modern sensor devices can accurately measure a multitude of different signal types, exceeding by far the human sensing capacity [3]–[5]. For many photonics-based sensing applications, the III-V material system is of particular interest as it allows utilizing mature components from the well-established telecom industry [6]–[9]. Steady demand for higher internet bandwidth and increasing use of sensor devices in all forms of modern technology fuels the need for innovation in the field of III-V based photonic components. On a discrete device level, III-V based photonic components have been developed to a degree at which further functional advancements become very challenging. Current research increasingly focuses on photonic integration, as it offers a sheer endless innovation potential. Two different concepts of photonic integration are under investigation: monolithic integration of components on a common substrate and hybrid integration that combines different material platforms. This thesis investigates selected key objectives of both approaches.

The monolithic integration of photonic components to a photonic integrated circuit (PIC) allows for significant improvements in footprint, packaging complexity, and device performance and novel functionalities [7], [10]. One common example of successful monolithic integration is the electroabsorption modulated laser (EML) as a transmitter chip in optical communication [11]. Compared to the established directly modulated laser (DML), the EML can achieve significantly better modulation performance with a similar footprint and packaging complexity. The biggest challenge for monolithically integrated PICs is to accommodate the individual design requirements of the integrated components on a single wafer. This can be accounted for by using different epitaxial layers on the same wafer (e.g. via regrowth), but this significantly increases fabrication cost and complexity [7], [12]. It has been demonstrated that by carefully balancing tradeoffs in the design, simple PICs such as the EML can achieve excellent performance with an identical epitaxial layer-stack [13]–[16]. This thesis investigates the application of the identical epitaxial layer-stack approach to advanced EML devices that comprise monolithically integrated semiconductor optical amplifiers (SOAs).

Hybrid integration takes the concept of photonic integration one step further by combining different material systems. It allows breaking free of the limitations of a single material system and enables PIC designers to choose the best material system for each integrated component. Hybrid integration of III-V based photonic components to silicon-based CMOS compatible photonic platforms is of particular interest as it promises remarkable cost reduction by leveraging available CMOS fabrication infrastructure [17]. One of the biggest challenges in hybrid integration is finding a scalable and reliable solution for the assembly of different material systems. This thesis addresses this issue by developing a hybrid integration process for flip-chip integration of III-V photonic chips to the CMOS compatible SiN TriPleX platform [18].

1.2 Objectives

The first objective of this thesis is to investigate and further develop EMLs with monolithically integrated SOAs. This is carried out for single EMLs and EML arrays. For single EMLs, the focus lies on achieving high output power at elevated temperatures for semi-cooled operation. For EML arrays, the focus lies on achieving uniform performance over different wavelength channels.

The second objective of this thesis is to develop and evaluate a wafer-scale compatible process for flip-chip hybrid integration of III-V based photonic chips to the SiN based

TriPleX platform. The design will be evaluated via the hybrid integration of III-V based distributed feedback (DFB) lasers and gain chips to SiN TriPleX PICs using different methods for the hybrid assembly process.

The final objective of this thesis is to develop and evaluate a III-V based monolithically integrated EML array for hybrid integration to a SiN TriPleX multiplexer chip. The focus is to implement and assess the novel hybrid integration process for a multi-PIC approach employing active III-V PICs and PICs of modern passive photonic platforms.

1.3 Thesis Organization

After the introduction, the thesis is organized into three main parts corresponding to the three objectives described in the previous section. Section 2 investigates EML devices with integrated SOAs, section 3 focuses on the development of a hybrid integration process, and section 4 explores the development of an EML array for hybrid integration. Sections 2 and 3 are written to be self-contained and can be read independently from each other. Section 4 references to sections 2 and 3. A conclusion and outlook to the thesis are given in section 5.

2. EML with Integrated SOA

This section focuses on EMLs that comprise an identical epitaxial layer-stack design with monolithically integrated SOAs. It investigates the possible benefits and drawbacks of utilizing integrated SOAs for high output EMLs (section 2.2.1 and 2.3.1) and EML arrays (section 2.2.2 and 2.3.2).

2.1 Fundamentals

2.1.1 Electroabsorption Modulated Laser

EMLs are one of the first photonic integrated circuits to be commercially successful on a larger scale [19]. The reason for this is that due to their relatively simple design, their fabrication complexity is similar to that of DMLs, but with superior performance regarding high-speed modulation. In contrast to DMLs, they typically exhibit a lower output power but achieve a higher extinction ratio with lower chirp and higher modulation bandwidths. This makes them the ideal device for low-cost direct detection based high-speed transmitters.

The EMLs described in this work comprise a DFB laser, with $\lambda/4$ phase-shifted index coupled grating, which is monolithically integrated with an electroabsorption modulator (EAM) (cf. Figure 1). The DFB laser is forward biased to generate continuous wave (CW) laser light and the EAM section is reversely biased for modulation of the optical output light via electroabsorption. The facet at the EAM side is coated with an anti-reflection coating to prevent optical feedback into the laser. The facet of the DFB laser is either high-reflection coated to maximize the optical power at the EAM output or it is anti-reflection coated to mitigate optical feedback to the DFB laser and thus achieve higher single-mode yield. To mitigate electrical crosstalk between DFB and EAM, the p-contacts are electrically isolated with an etched separation trench providing a separation resistance R_{sep} of several tens of $k\Omega$. A common ground contact is used for the n-contact. The active layer structure of DFB and EAM consists of a multiple quantum well (MQW) structure. Compared to EAMs with a bulk structure, where the electroabsorption is mainly caused by the Franz-Keldysh effect, the electroabsorption in a MQW structure is dominated by the quantum-confined Stark effect as described in section 2.1.2. InGaAlAs is used as the active material for the MQW structure. Due to the aluminum content, it oxidizes easily and thus requires special fabrication processes to avoid device failure. The more complex fabrication of InGaAlAs compared to e.g. InGaAsP is made up for by its superior optical performance. It allows designing the

MQW layers with a larger conduction band offset and simultaneously a more shallow valence band offset. The large conduction band offset leads to stronger confinement of electrons, which is beneficial for high-temperature operation of the DFB and a larger extinction ratio for the EAM [20], [21]. The shallow valence band offset allows for shorter escape times for the less mobile holes, which leads to smaller chirp and less input power dependence [22]–[24].

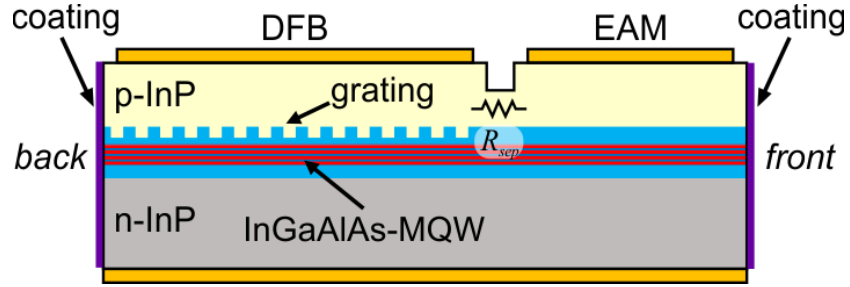


Figure 1: Schematic cross-section parallel to the waveguide direction of an EML. A distributed feedback (DFB) laser is monolithically integrated with an electroabsorption modulator (EAM).

The DFB laser is operated in the gain regime with a forward bias voltage in contrast to the EAM section, which is operated in the absorption regime with a reverse bias voltage (cf. Figure 2). As such, the two sections have different requirements on the epitaxial design for optimum operation. To achieve the lowest threshold and highest output power for the DFB laser, it is preferred to have the maximum gain wavelength at the same position as the operation wavelength (cf. Figure 2 (green)). For the EAM section, typically a longer wavelength with lower absorption at zero bias voltage is preferred to reduce the insertion loss and mitigate carrier pileup effects (cf. Figure 2 (blue)).

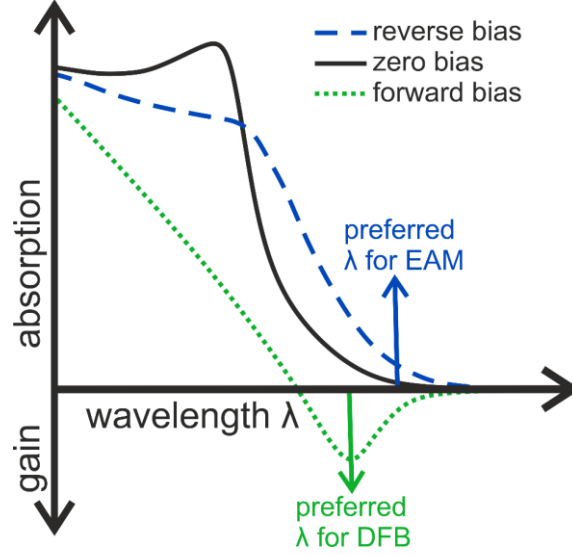


Figure 2: Optical gain and absorption spectra of EML active layers for different biasing conditions.

Light absorption in the EAM is described by the transmission coefficient $T(V)$ with

$$T(V) = e^{-\alpha(V)L}, \quad (1)$$

where L , $\alpha(V)$, and V are the modulator length, the absorption coefficient, and bias voltage over the active layers, respectively. The extinction ratio ER describes the optical output power relation between the “on” and the “off” state of the modulator, expressed here in dB with

$$ER = 10 \log \left(\frac{T(V_{off})}{T(V_{on})} \right) = 10 \log \left(\frac{e^{-\alpha(V_{off})L}}{e^{-\alpha(V_{on})L}} \right) = 4.343 \left(\alpha(V_{on}) - \alpha(V_{off}) \right) L \quad (2)$$

A simple way to increase the extinction ratio is to increase the modulator length L . When doing so, one has to take into account that the mean insertion loss η_{mean} , expressed here in dB with

$$\eta_{mean} = -10 \log \left(\frac{T(V_{on}) + T(V_{off})}{2} \right) = -10 \log \left(\frac{e^{-\alpha(V_{on})L} + e^{-\alpha(V_{off})L}}{2} \right) \quad (3)$$

will also increase and thus decrease the averaged modulated optical output power. Additionally, the modulator capacitance will increase which reduces the modulation bandwidth, so a compromise has to be found when designing the modulator length (cf. section 2.2.1).

As mentioned before, the DFB and EAM sections have very different requirements on the epitaxial layer structure. Great effort has been made in the past on fabricating epitaxial layer structures that can accommodate these different requirements (cf. Figure 3 (a), (b)). The simplest approach is to use an identical layer structure for DFB and EAM. It allows for simple fabrication but the epitaxial design has to compromise between DFB and EAM performance. The identical epitaxial layer approach is typically realized with a single type MQW (cf. Figure 3 (a)) or with a double type MQW (cf. Figure 3 (b)) [14]–[16], [25], [26]. For the twin guide coupling approach (cf. Figure 3 (c)), a double type MQW is grown but the top MQW type is etched away at the EAM section. This allows for different epitaxial structures of the sections but it requires a sophisticated taper to couple the light from the DFB to the EAM waveguide or high optical loss at the transition has to be taken into account. An alternative is to use selective quantum well intermixing (cf. Figure 3 (d)). The absorption spectrum at the EAM section is blue-shifted by a localized interdiffusion between the well and barrier material [27], [28]. Another method of achieving a wavelength shift for one of the sections with a single epitaxy is to use the selective area growth (SAG) technique (cf. Figure 3 (e)) which allows growing different layer thicknesses on the same wafer. That way the bandgap energy of each section can be individually adjusted because it depends directly on the quantum well thickness of the MQW layers [29], [30]. The highest flexibility regarding the MQW design of each section is given by the butt-joint approach (cf. Figure 3 (f)). It consists of etching down the initially grown epitaxy at the DFB or EAM section followed by a regrowth step [19], [21]. It allows fully individual epitaxial layer design of the individual sections but has the highest fabrication complexity. For this work, the identical epitaxial layer design with a single type MQW was chosen (cf. Figure 3 (a)). Due to its simplicity, it offers good reproducibility with a fabrication complexity close to that of a DML. In previous publications, it has been demonstrated that excellent performance can be achieved for EMLs with a well balanced single type MQW design [13]–[16].

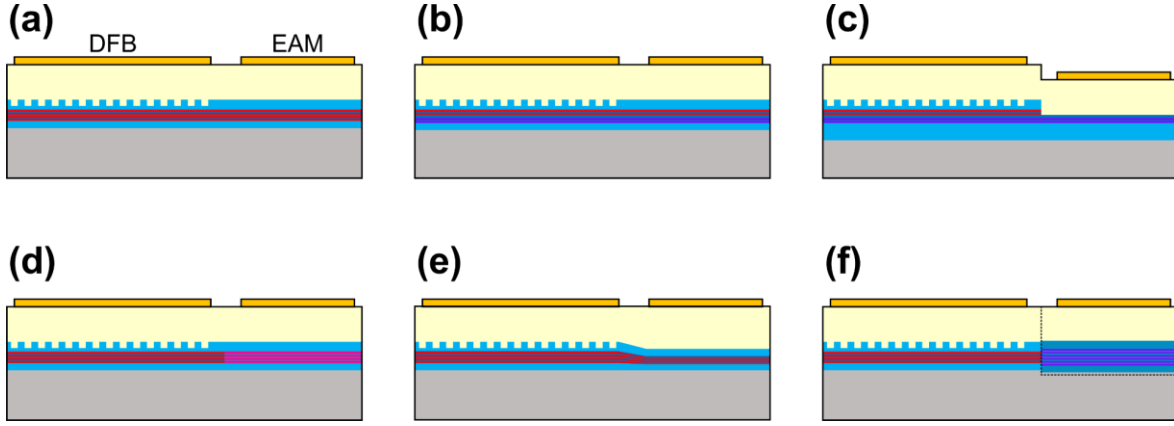


Figure 3: Schematic cross-sections parallel to the waveguide direction for EMLs with different epitaxial designs: Identical epitaxial layer with single type MQW (a) and with double type MQW (b), twin guide coupling (c), selective quantum well intermixing (d), selective area growth (e), butt-joint (f).

2.1.2 Electroabsorption in MQW

The electroabsorption modulators described in this work use an MQW structure as an absorbing layer. The absorption of MQW structures is dominated by the quantum-confined Stark effect (QCSE). From a performance point of view, the biggest difference to the Franz-Keldysh effect, which is prominent in bulk structures, is the higher modulation efficiency of the QCSE for a given modulator length [31]. This allows for more compact and power-efficient devices.

The working principle of the QCSE is illustrated in Figure 4. The electron and hole wave functions are confined in a quantum well layer by two surrounding barrier layers with higher bandgap. The confinement leads to quantized energy levels, called subbands, within the quantum well (E_e and E_h in Figure 4). For an incoming photon to be absorbed, its energy $h\omega$ has to be higher than the energy difference of the subbands $E_e - E_h$, and the probability of absorption depends on the wave functions' overlap integral [32]. When an electrical field is applied to the quantum wells with a reverse bias voltage, the energy bands are tilted and the subbands move closer together resulting in a redshift of the absorption spectra (cf. Figure 2). That way absorption is increased for wavelengths on the longer wavelength side of the absorption spectrum. As an opposing effect, the applied electrical field pulls the electron and hole wave functions in opposing directions (cf. Figure 4), which decreases their overlap integral and thus reduces overall absorption.

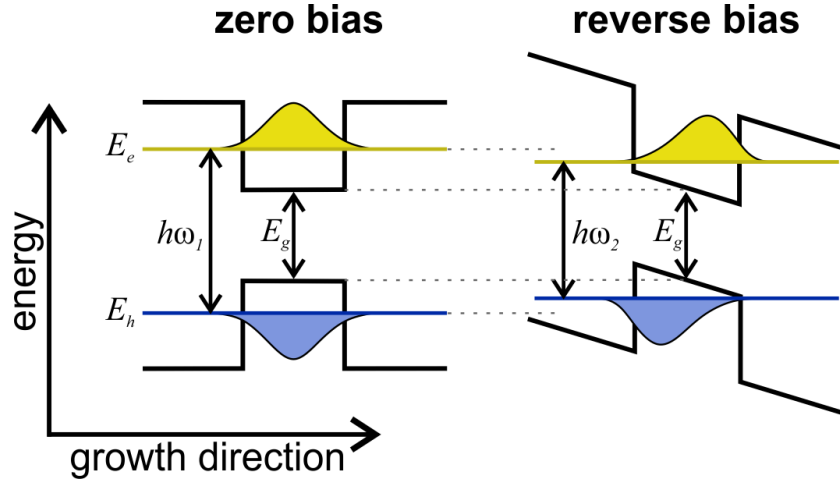


Figure 4: Schematic illustration of the quantum-confined Stark effect in a quantum well. E_e and E_h mark the subbands of the electron and hole wave functions. E_g marks the bandgap energy of the quantum well layer.

Figure 5 (a) shows an example of the reverse bias voltage dependent EAM insertion loss that corresponds to the transmission coefficient (1). At high reverse bias voltages, the wave functions overlap integral is so much reduced that there is a limit to the maximum absorption coefficient that can be achieved via voltage increase. The corresponding dependence of the output power on the reverse bias voltage together with its first derivative is shown in Figure 5 (b). The voltage where the derivative dP/dV is highest is the point where the power voltage dependence is the most linear and where an EAM typically exhibits a symmetrical eye (i.e. 50% crossing). This is the bias voltage at which EAMs are typically operated at and in this work, it is referred to as the operation point voltage. The voltage of the operation point is determined by the detuning of the DFB wavelength to the absorption peak wavelength, where a larger detuning leads to a larger operation point voltage.

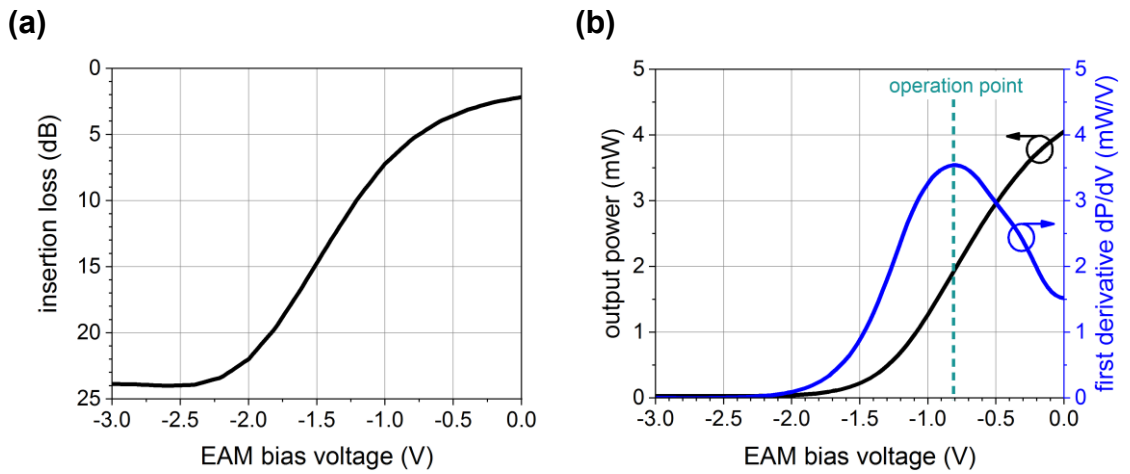


Figure 5: Exemplarily the measured insertion loss (a) and optical output power (b) versus EAM bias voltage. The point of highest slope dP/dV is referred to as operation point in this work.

2.1.3 Equivalent Circuit Model

In the following section, the EML is described with an equivalent circuit model and its corresponding frequency response function is derived. In section 2.1.4 and 2.1.6, the frequency response function is extended to include the effects of optical feedback and SOA saturation. The extended frequency response function will allow for a comprehensive evaluation of the small-signal characteristic of EML with integrated SOA.

The frequency response of an EML can be derived in good approximation with an electrical equivalent circuit model of the EAM section (cf. Figure 6). This is a contrast to DMLs, for which the electro-optical frequency response is strongly influenced by the carrier-photon interaction inside the laser cavity. The equivalent circuit model in Figure 6 is divided into three sections: the electroabsorption modulator, the RF-probe, and the voltage source. The reversely biased active layers of the electroabsorption modulator are described as a capacitor with the capacitance C_{EAM} . When input light is absorbed in the active layers, a voltage V dependent photocurrent I_{pho} is generated. This is approximated in the equivalent circuit model with a photocurrent resistance $R_{pho} = \Delta V / \Delta I_{pho}$ that is connected in parallel to the EAM capacitance C_{EAM} . The EAM ridge is described with a series resistance R_{ser} that connects via a transmission line the EAM contact pad with the capacitance C_{pad} . The transmission line is approximated by an inductance L_{trans} with two capacitors at each side, each with half of the transmission lines capacitance C_{trans} . In this work, all high frequency measurements are performed with an RF-probe with $50\ \Omega$ termination resistance R_{term} to match the $50\ \Omega$ of the source impedance Z_1 . The $50\ \Omega$ termination has a DC blocking capacitor C_{DC} . The RF-probe has a parasitic capacitance C_{probe} and inductance L_{probe} .

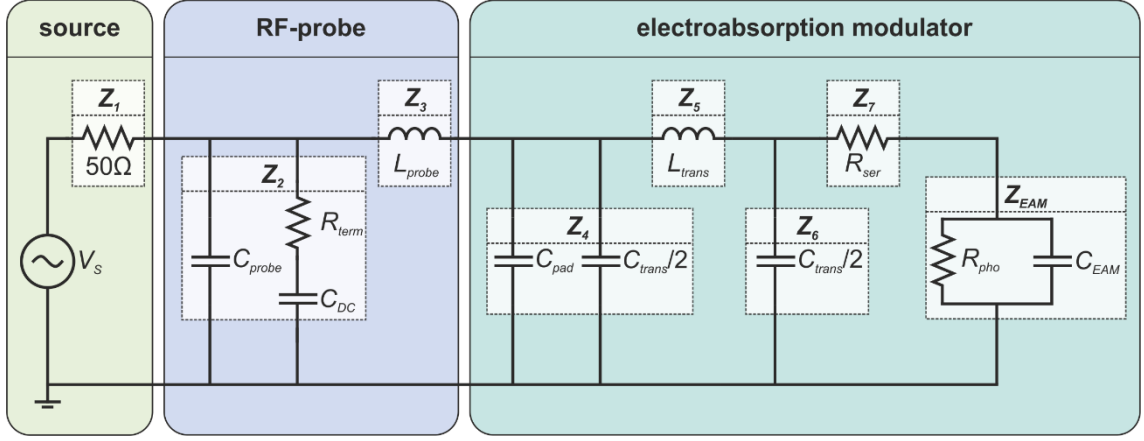


Figure 6: Equivalent circuit model of an EML with input source (left), 50 Ohm terminating RF-probe (middle), and EAM section (right).

From the equivalent circuit model, an analytical frequency response function is derived with an impedance-based formalism [33]. Each passive component in the circuit is expressed by their complex impedance with $Z_R = R$ for resistors, $Z_C = (i\omega C)^{-1}$ for capacitors and $Z_L = i\omega L$ for inductors. By combining the impedances that share the same nodes, the circuit is simplified to a set of eight individual impedances (cf. Figure 6)

$$\begin{aligned}
 Z_1 &= 50 \, \Omega, \\
 Z_2 &= \left(i\omega C_{probe} + \frac{1}{R_{term} + (i\omega C_{DC})^{-1}} \right)^{-1}, \\
 Z_3 &= i\omega L_{probe}, \\
 Z_4 &= \left(i\omega C_{pad} + i\omega \frac{C_{trans}}{2} \right)^{-1}, \\
 Z_5 &= i\omega L_{trans}, \\
 Z_6 &= \left(i\omega \frac{C_{trans}}{2} \right)^{-1}, \\
 Z_7 &= R_{ser}, \\
 Z_{EAM} &= \left(\frac{1}{R_{pho}} + i\omega C_{EAM} \right)^{-1}.
 \end{aligned} \tag{4}$$

Based on the Kirchhoff's circuit laws the following equation system can be derived

$$\begin{aligned}
V_S &= V_1 + V_2 = Z_1 I_1 + Z_2 I_2, \\
V_S &= V_1 + V_3 + V_4 = Z_1 I_1 + Z_3 I_3 + Z_4 I_4, \\
V_S &= V_1 + V_3 + V_5 + V_6 = Z_1 I_1 + Z_3 I_3 + Z_5 I_5 + Z_6 I_6, \\
V_S &= V_1 + V_3 + V_5 + V_7 + V_{EAM} = Z_1 I_1 + Z_3 I_3 + Z_5 I_5 + Z_7 I_7 + V_{EAM}, \\
0 &= -I_1 + I_2 + I_3, \\
0 &= -I_1 + I_2 + I_4 + I_5, \\
0 &= -I_1 + I_2 + I_4 + I_6 + I_7, \\
0 &= -I_1 + I_2 + I_4 + I_6 + V_{EAM} Z_{EAM}^{-1},
\end{aligned} \tag{5}$$

where V_S is the voltage supplied from the source, V_{EAM} is the voltage at the active layers of the EAM and V_i and I_i are the voltage and current at the i -th impedance, respectively. To derive the transfer function that describes how much of the source voltage V_S transfers to the voltage at the EAMs active layers V_{EAM} , we write the equation system in matrix form

$$\vec{b} = \mathbf{A} \vec{x}, \tag{6}$$

with

$$\vec{b} = \begin{pmatrix} V_S \\ V_S \\ V_S \\ V_S \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}, \mathbf{A} = \begin{pmatrix} Z_1 & Z_2 & 0 & 0 & 0 & 0 & 0 & 0 \\ Z_1 & 0 & Z_3 & Z_4 & 0 & 0 & 0 & 0 \\ Z_1 & 0 & Z_3 & 0 & Z_5 & Z_6 & 0 & 0 \\ Z_1 & 0 & Z_3 & 0 & Z_5 & 0 & Z_7 & 1 \\ -1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 1 & 0 & 1 & 1 & 0 \\ -1 & 1 & 0 & 1 & 0 & 1 & 0 & Z_{EAM}^{-1} \end{pmatrix}, \vec{x} = \begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \\ I_7 \\ V_{EAM} \end{pmatrix} \tag{7}$$

and solve for V_{EAM} by using the Cramer's Rule

$$V_{EAM} = \frac{\det(\mathbf{A}_b)}{\det(\mathbf{A})}, \tag{8}$$

where \mathbf{A}_b is the matrix \mathbf{A} with the last column replaced by the vector \vec{b} . The electrical transfer function of the EAM is then given by

$$H_E(\omega) = \frac{V_{EAM}}{V_S}. \tag{9}$$

The relation of the EMLs optical output power with the source voltage can be expressed with the electro-optical transfer function as

$$H_{E/O}(\omega) = H_E H_{MQW}, \quad (10)$$

where H_{MQW} is the transfer function describing the relation between the voltage that is applied to the active MQW layers and the optical output power. With the assumption that the field-induced absorption in the EAM is near-instantaneous, the transfer function H_{MQW} is frequency independent and can be expressed as a constant. The normalized electro-optical frequency response $|S_{21}(\omega)|$ of the EML then writes as

$$|S_{21}(\omega)| = \frac{|H_{E/O}(\omega)|}{|H_{E/O}(0)|} = \frac{|H_{MQW}H_E(\omega)|}{|H_{MQW}H_E(0)|} = \frac{|H_E(\omega)|}{|H_E(0)|}. \quad (11)$$

Thus, the normalized electro-optical frequency response of the EML is identical to the normalized electrical frequency response of the EAM. Figure 7 shows exemplarily the measured electro-optical frequency response of an EML and the corresponding fitting function based on (11).

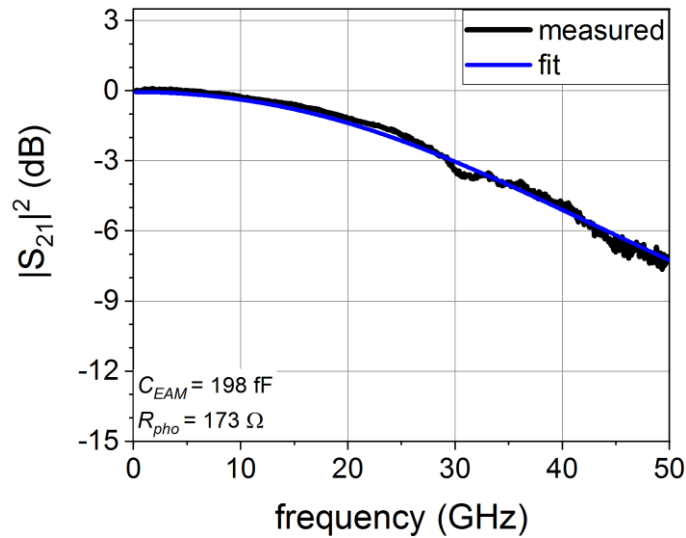


Figure 7: Exemplarily the measured electro-optical frequency response of an EML with fitting function based on (11). Additional fitting parameters are given in Table 4 of Appendix 1.

The reflection coefficient of the EAM is also derived with an impedance-based formalism and writes as [34]

$$|S_{11}(\omega)| = \left| \frac{Z_{DUT} - Z_1}{Z_{DUT} + Z_1} \right|, \quad (12)$$

with Z_{DUT} being the impedance of the device under test including the RF-probe. Z_{DUT} can be expressed as a combination of parallel and serial connections of the impedances in the equivalent circuit model in (4) with

$$Z_{DUT} = (Z_2^{-1} + (Z_3 + (Z_4^{-1} + (Z_5 + (Z_6^{-1} + (Z_7 + Z_{EAM})^{-1})^{-1})^{-1})^{-1})^{-1}). \quad (13)$$

The reflection coefficient $S_{11}(\omega)$ gives a measure of how much electrical power supplied by the source is reflected at the EAM.

2.1.4 Optical Feedback

In section 2.1.3, a frequency response function for the EML was derived with the assumption that the operation of the EAM section does not influence the DFB section. This approximation becomes inaccurate when optical feedback, e.g. from the output facet, is present. The modulation of the EAM section results in a modulation of the optical feedback light that influences the DFB laser which in turn changes the frequency response of the EML. Sun et al. derived in [15] a frequency response function that includes optical feedback for an EML with a simple equivalent circuit model. In this section, the results from [15] will be applied to the frequency response function (11) that was derived in this work.

The light that is reflected at the EMLs output facet travels back to the DFB where it has an amplitude and phase that is dependent on the absorption and propagation constant in the EAM. To simplify the scenario, the EAM can be described as an equivalent reflectivity with variable amplitude and phase at the front of the DFB [15]

$$r_{equivalent} = r_{facet} e^{-(1+i\alpha_{chirp})\alpha L} e^{-2i\beta L}. \quad (14)$$

where r_{facet} , α_{chirp} , α , β , L are the reflectivity at the output facet, the chirp parameter, the absorption coefficient, the propagation constant, and the length of the EAM, respectively. For small-signal modulation, the voltage applied to the active layers can be expressed as the sum of DC and AC components [15]

$$V = V_{DC} + V_{AC}e^{i\omega t}, \quad (15)$$

and the absorption coefficient is written as

$$\alpha = \alpha_{DC} + \alpha_{AC}e^{i\omega t}. \quad (16)$$

If the optical feedback light is modulated at a frequency ω close to the relaxation oscillation frequency ω_R of the DFB, the DFB is excited in resonance, which leads to an oscillation of the output power. For the electro-optical transfer function of the EML, this effect can be expressed by including an additional transfer function related to the optical feedback

$$H_{E/O}^*(\omega) = H_E(H_{MQW} + H_{feedback}). \quad (17)$$

The change of DFB laser output power induced by the optical feedback runs in parallel to the field-induced absorption in the EAM. This is expressed in (17) by the addition of the two transfer functions H_{MQW} and $H_{feedback}$. The feedback related transfer function $H_{feedback}$ can be expressed as [15]

$$H_{feedback}(\omega) = \frac{A_F(i\omega + \gamma)}{\omega_R^2 - \omega^2 + i\omega\gamma}, \quad (18)$$

where A_F is a coefficient describing the strength of the influence of the optical feedback and γ is the damping coefficient of the DFB. As explained in section 2.1.3, H_{MQW} can be expressed as a constant and because the goal is to derive a normalized function, we set $H_{MQW} = 1$ for simplicity. By using (9), (17), and (18), the normalized frequency response of the EML including optical feedback writes as

$$|S_{21}^*(\omega)| = \frac{|H_{E/O}^*(\omega)|}{|H_{E/O}^*(0)|}, \quad (19)$$

with

$$H_{E/O}^*(\omega) = H_E \left(1 + \frac{A_F(i\omega + \gamma)}{\omega_R^2 - \omega^2 + i\omega\gamma} \right). \quad (20)$$

The strength of the influence of optical feedback A_F is related to the amplitude as well as the phase of the light that is coupled back, which can be seen in the following relation [15]

$$A_F \propto r_{facet} e^{-\alpha_{DC}L} \cos(2\beta L + \alpha_{chirp}\alpha_{DC}L). \quad (21)$$

The first two factors relate to the amplitude of the optical feedback. A higher absorption α_{DC} in the EAM will reduce the light that is reflected at r_{facet} . The third factor relates to the phase of the optical feedback. If the feedback light is in-phase to the DFB light (positive A_F), it will enhance the frequency response close to ω_R . If the light is out-of-phase (negative A_F), it will suppress the frequency response close to ω_R . An example of measured frequency response functions with corresponding fitting function (19) is shown in Figure 8. The fitting function agrees well with the measured curves and allows extracting internal EAM parameters like the EAM capacitance C_{EAM} despite the influence of optical feedback. The classical method of evaluating the EAM capacitance from the 3dB bandwidth of the normalized frequency response is often unprecise when optical feedback is present. The reason for this is that the influence of optical feedback can shift the DC-point (0 GHz) level and thus change the 3dB bandwidth of the normalized curve, even if the EAM capacitance is unchanged.

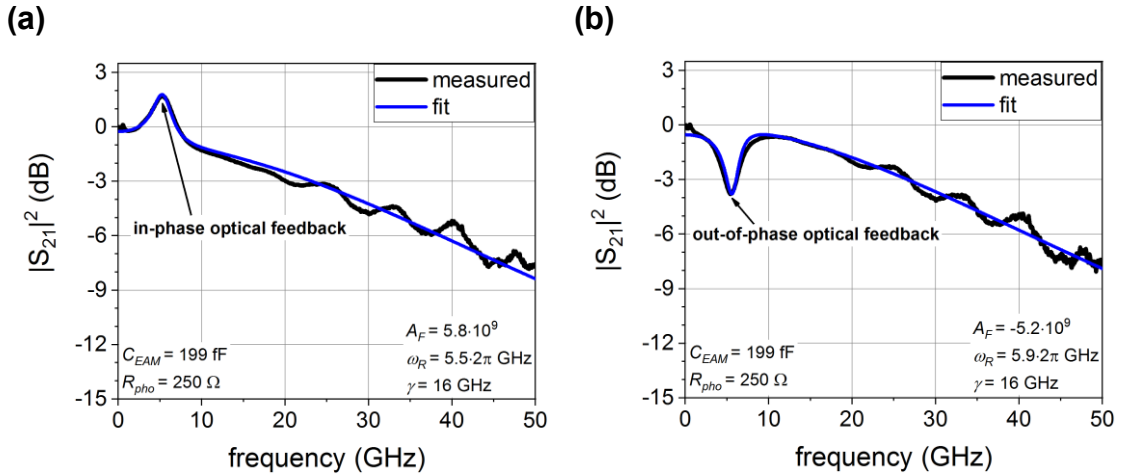


Figure 8: Exemplarily the measured frequency response of an EML with in-phase (a) and out-of-phase (b) optical feedback, each with fitting function based on (19). Additional fitting parameters are given in Table 4 of Appendix 1.

2.1.5 Photogenerated Carriers

When photons are absorbed in the EAM section by excitation of electrons from the valence band to the conduction band, charge carriers are generated in the form of electron-hole pairs. The electrons and holes leave the EAM in opposite directions following the electrical field of the applied bias voltage and thus generate a photocurrent. These photogenerated carriers influence the modulation performance of the EAM due to a corresponding photocurrent resistance and due to a change of EAM capacitance, as will be described in this section.

The photocurrent generated in the EAM can be written as [35]

$$I_{pho}(V) = -I_{pho,0} - \eta_{EAM}P_{in}(1 - T(V)), \quad (22)$$

where $I_{pho,0}$ is the photocurrent at zero bias voltage, η_{EAM} the photodetection responsivity of the EAM and P_{in} the incident optical power. The photocurrent resistance is defined as the differential resistance of the EAM for a specific bias voltage with

$$R_{pho}(V) = \frac{dV}{dI_{pho}}. \quad (23)$$

By using (22) and (23) the photocurrent resistance can be written as

$$R_{pho}(V) = \left(\eta_{EAM}P_{in} \frac{dT}{dV} \right)^{-1}. \quad (24)$$

Figure 9 shows exemplarily the measured photocurrent and the corresponding photocurrent resistance versus the EAM bias voltage for an EML with different DFB currents. The photocurrent curves (cf. Figure 9 (a)) exhibit a point of highest slope dI_{pho}/dV , here around -1 V, which, based on (23), corresponds to the lowest photocurrent resistance (cf. Figure 9 (b)). With increasing DFB current, the incident optical power increases, which, in correspondence to (24), decreases the overall photocurrent resistance (cf. Figure 9 (b)). Because the photocurrent is directly related to the optical output power, the bias voltage with the lowest photocurrent resistance coincides with the operation point voltage (c.f. Figure 5 (b – dashed line)).

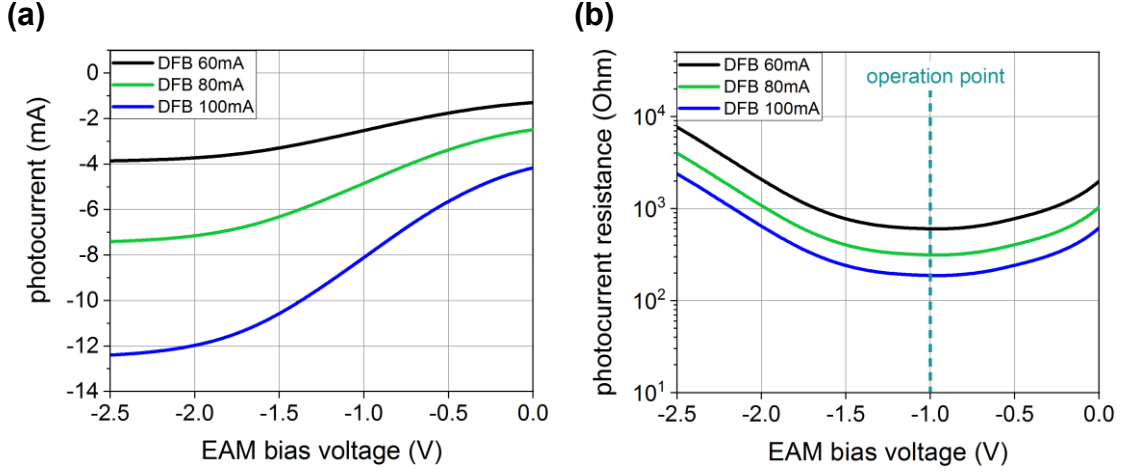


Figure 9 Exemplarily the measured photocurrent (a) and corresponding photocurrent resistance (b) versus EAM bias voltage for an EML with different DFB currents. Photocurrent resistance is calculated with (23).

To evaluate the influence on the EAMs modulation performance, the frequency response S_{21} and the reflection coefficient S_{11} based on (11) and (12) are calculated in Figure 10 for different photocurrent resistances. It can be seen that when the photocurrent resistance gets close to the 50 Ohm termination resistance and thus $R_{pho} \gg R_{term}$ is not valid anymore, the frequency response S_{21} increases. At the same time, the reflection coefficient S_{11} increases for low frequencies. Therefore, a low photocurrent resistance can benefit the high frequency (HF) performance of an EAM but an increased reflection coefficient has to be taken into account. Additionally, a small photocurrent resistance leads to an overall voltage drop at the active layers, which can be calculated with (9). For the parameters of the example shown in Figure 10, the voltage at the active layers drops by 20% for a photocurrent resistance of 150 Ω compared to the case of an infinite photocurrent resistance. So a high photocurrent and a correspondingly low photocurrent resistance reduce the amplitude of the voltage swing at the active layers and accordingly reduce the extinction ratio (2) that is achieved.

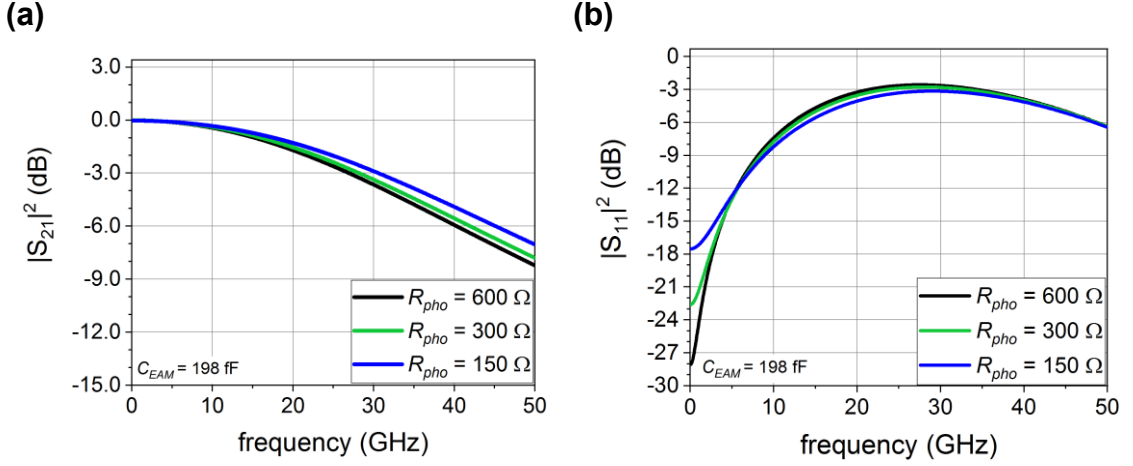


Figure 10 Calculated S21 (a) and S11 (b) curves of an EML based on (11) and (12) for different photocurrent resistances R_{ph0} . Additional function parameters are given in Table 4 of Appendix 1.

In addition to the change of resistance in the equivalent circuit of the EAM, the photogenerated carriers directly influence the capacitance of the EAM. The generated electron-hole pairs increase the electric polarization in the EAMs active layers, which corresponds to a larger effective permittivity and thus increases the capacitance [36]. This effect is particularly strong for low EAM bias voltages and high incident optical powers at which a large number of carriers are generated but cannot leave the active layers effectively due to the low voltage [37]. In the worst case, it can increase the capacitance to a multiple of its original value [38], which significantly reduces the modulation bandwidth and thus limits the maximum incident power and minimum applied bias voltage that can be used for the practicable operation of the EAM section.

2.1.6 Integrated Semiconductor Optical Amplifiers

In section 2.1.5 it was shown that a high incident power at the EAM can decrease the modulation bandwidth and reduce the extinction ratio of the EML. This limits the maximum EML output power that can be achieved by simply increasing the DFB laser's output power. This limitation can be overcome by integrating a semiconductor optical amplifier (SOA) at the output facet of the EML. It allows achieving a large EML output power while keeping the EAM incident power low. An ideal SOA with linear and time-independent amplification would not influence the shape of a modulated input signal other than amplifying it. In reality, SOAs exhibit time-dependent nonlinearity at large optical powers due to saturation. In this section, a frequency response function is derived that includes saturation effects and thus allows the characterization of EMLs with integrated SOAs.

The power and gain of the SOA can be described for the steady-state condition by the following two equations [11]

$$\frac{\partial P}{\partial z} = (g - \alpha_{int})P, \quad (25)$$

$$g = \frac{g_0}{1 + \frac{P}{P_{sat}}}, \quad (26)$$

where P, P_{sat}, g, g_0, z , and α_{int} are the optical power, the saturation power, the saturated modal gain, the unsaturated modal gain, the longitudinal position in the SOA, and the modal loss, respectively. In most practical cases, it can be assumed that $\alpha_{int} \ll g$, so we set $\alpha_{int} = 0$ in the following. From (26) one can see that the saturation power P_{sat} describes the optical power at which the saturated gain g is half of the unsaturated gain g_0 . In the unsaturated case with $P \ll P_{sat}$, equation (26) yields $g = g_0$ and by solving (25) the unsaturated power inside the SOA can be written as

$$P(z) = P(0)e^{g_0 z}. \quad (27)$$

The amplifier gain is defined as

$$G = \frac{P(L)}{P(0)}, \quad (28)$$

where L is the length of the SOA. The unsaturated amplifier gain then yields

$$G_0 = \frac{P(0)e^{g_0 L}}{P(0)} = e^{g_0 L}. \quad (29)$$

When the optical power gets close to the saturation power, the high rate of stimulated emission reduces the carrier density to a degree that the gain is significantly decreased. The saturated amplifier gain can be derived by direct integration of (25) with the boundary conditions $P(z = 0) = P_{in}$, $P(z = L) = P_{out}$ and yields

$$G_{CW} = G_0 e^{-(G_{CW}-1)\frac{P_{in}}{P_{sat}}}. \quad (30)$$

In the case of a modulated input signal, the gain at the beginning of an optical pulse, where the current density is still high, will be close to the unsaturated case G_0 . Towards the end of the optical pulse, where the carrier density has been reduced by stimulated emission, the gain will be close to G_{CW} . The longer the pulse, the closer the gain will be to G_{CW} . This imbalance leads to overshooting and patterning effects for the modulated output signal. To quantify the degree of saturation we define the saturation factor

$$a_{sat} = \frac{G_{CW}}{G_0}. \quad (31)$$

It has been shown by Pham et al. [39] that the SOAs transfer function including saturation effects can be expressed as

$$H_{SOA}(\omega) = a_{sat} G_0 \frac{1 + \frac{i\omega\tau_c}{a_{sat}}}{1 + i\omega\tau_c}, \quad (32)$$

where τ_c is the effective SOA carrier lifetime. For an EML with integrated SOA, the electro-optical transfer function including (9), (18) and (32) can then be written as

$$H_{E/O}^{**}(\omega) = H_E (1 + H_{feedback} H_{SOA}^2) H_{SOA}. \quad (33)$$

The transfer function $H_{feedback}$ is multiplied by the square of H_{SOA} because optical feedback light passes the SOA twice on its way to the DFB. The last H_{SOA} term in (33) represents the influence of the SOA on the modulated light that finally exits at the EML output. The normalized frequency response writes as

$$|S_{21}^{**}| = \frac{|H_{E/O}^{**}(\omega)|}{|H_{E/O}^{**}(0)|}. \quad (34)$$

This function allows the small-signal characterization of EMLs with integrated SOAs that exhibit optical feedback and SOA saturation. Figure 11 gives an example of the effect of SOA saturation on the frequency response of an EML. For saturation factors $a_{sat} < 0$ dB, the nonlinearity of the gain leads to a drop in the frequency response for frequencies lower than the inverse carrier lifetime τ_c . At these frequencies the SOA gain is reduced towards the saturated gain G_{CW} . It should be noted that although the 3dB bandwidth of the normalized

response function increases, saturation is typically unwanted due to the previously mentioned overshooting and patterning effects.

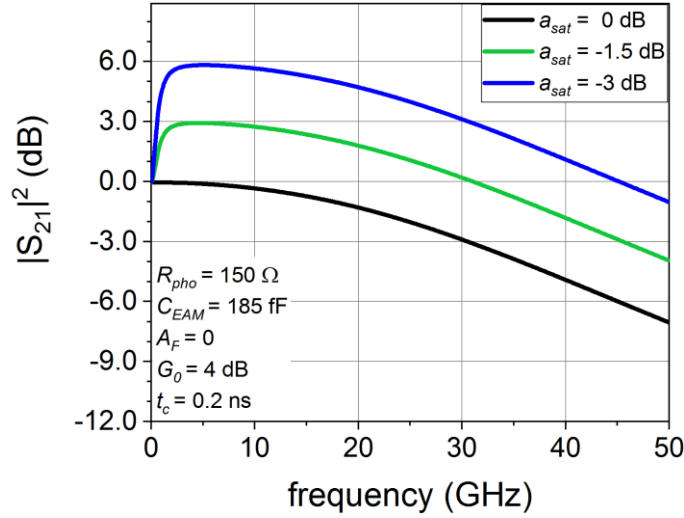


Figure 11 Calculated S21 curves based on (34) for an EML with integrated SOA with different saturation factors a_{sat} . Additional function parameters are given in Table 4 of Appendix 1.

2.2 Design and Simulation

In this section, the structural layout of the EML with integrated SOA devices is described, and critical design parameters are identified. The monolithic integration of SOA structures to EMLs was first introduced in 2003 by NTT [40]. Since then NTT has further developed its design and other groups have started developing similar devices [12], [41]–[43]. For these devices, the SOA integration was carried out with a sophisticated epitaxial design of either selective area growth or butt-joint regrowth (c.f. Figure 3 (e), (f)). In contrast to this, an identical epitaxial layer design with a single type MQW is used in this work (c.f. Figure 3 (a)). The identical epitaxial layer design has the lowest fabrication complexity and thus allows for the low-cost device fabrication.

2.2.1 High Power EML

EMLs with integrated SOA that were fabricated prior to this work were used as the basis of the device design presented here. In this section, the original design is further developed based on experimental results and simulation models. This advanced design is experimentally characterized in section 2.3.1. The experimental characterization of the original design is given in [44].

The primary goal of the high power EML design variant is to boost the maximum optical output power of the EML while simultaneously maintaining a good high-speed modulation performance. Compared to the EML structure described in section 2.1.1, the high power EML has an SOA that is monolithically integrated after the EAM section (cf. Figure 12 & Figure 13). This allows increasing the EMLs output power above the limit where a high incident optical power at the EAM would degrade its modulation performance (c.f. section 2.1.5). The targeted operation temperature is 50 °C, which allows for semi-cooled operation and thus reduces overall power consumption. The targeted operation wavelengths lie in the L-Band around 1577 nm. To maximize the optical output efficiency towards the front facet, the back facet of the 250 μm long DFB laser is high-reflection coated (c.f. Figure 12 & Figure 13). The waveguide at the front facet is anti-reflection coated and tilted by 7°, to mitigate signal degradation from optical feedback (cf. section 2.1.4). As depicted in Figure 13 (left), an identical epitaxial layer design with a single type MQW was chosen for the DFB, EAM, and SOA section. That way, no fabrication complexity is added from SOA integration. Etched separation trenches that provide a separation resistance R_{sep} of several tens of k Ω separate the p-contacts of all three sections. As depicted in Figure 13 (right), all three sections have a ridge waveguide structure. At the EAM section, the waveguide is additionally etched through the MQW to minimize the EAM's capacitance.

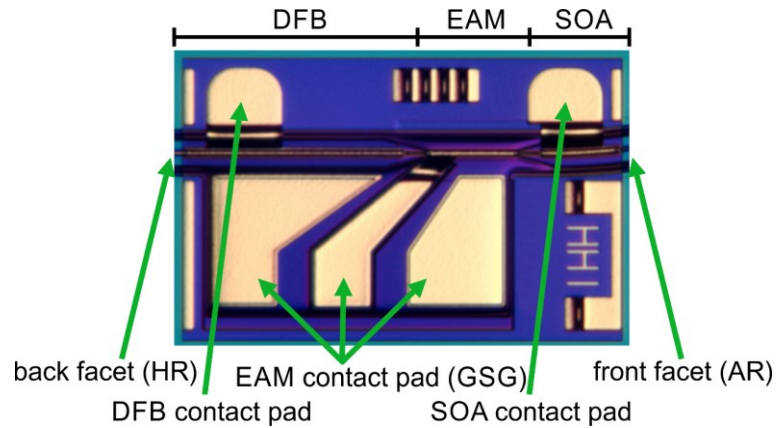


Figure 12: Top view of a fabricated high power EML chip with monolithically integrated DFB, EAM and SOA section. The back facet is high-reflection (HR) coated and the front facet is anti-reflection (AR) coated. A ground-signal-ground (GSG) configuration is used for the EAM contact pad. Chip dimensions are 590 μm x 350 μm .

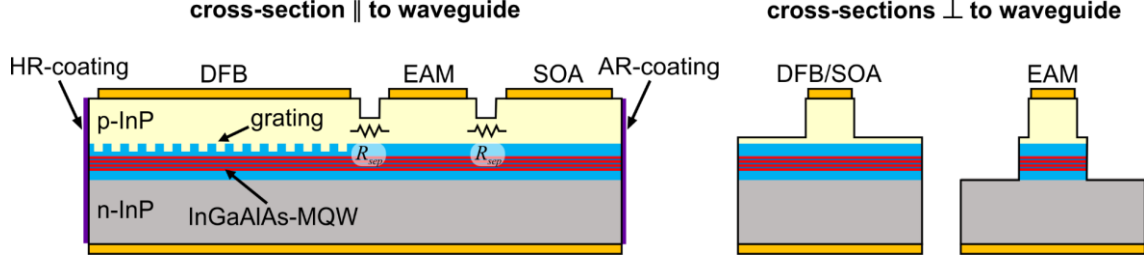


Figure 13: Schematic cross-sections parallel (left) to the waveguide direction and perpendicular (right) to the waveguide direction of the high power EML (cf. Figure 12).

EAM Length

One of the most critical design parameters of an EML is the length of the EAM section. By increasing the length of the EAM, a higher extinction ratio and a lower series resistance can be achieved. By reducing the length of the EAM, its insertion loss and its capacitance are reduced (c.f. section 2.1.1). These tradeoffs have to be carefully considered. In this section, an estimation of the related performance tradeoffs will be given, which can be used as a guideline for EAM design.

The EAM capacitance C_{EAM} , the series resistance R_{ser} and the photocurrent resistance R_{phot} are all EAM length-dependent parameters that determine the EAMs modulation bandwidth as shown in section 2.1.3. The influence of the photocurrent resistance is typically small and thus it is assumed as length-independent in the following. The series resistance is approximated to be inversely proportional to the EAM length with

$$R_{ser} = \frac{R_0}{L}, \quad (35)$$

where R_0 is a constant. The capacitance of the EAM corresponds to that of a parallel plate capacitor with

$$C_{EAM} = \varepsilon \frac{wL}{d} = C_0 L, \quad (36)$$

where ε , d , and w , are the capacitors permittivity, the thickness, and the width. These parameters are summarized here with the constant factor C_0 . Based on experimental results of EMLs designed previous to this work, the parameters R_0 and C_0 are estimated with $R_0 = 1.3 \cdot 10^{-3} \Omega m$ and $C_0 = 1.95 \cdot 10^{-9} F/m$. With the electro-optical frequency response function (11) from the equivalent circuit model the length dependence of the EAMs 3dB

bandwidth is calculated (c.f. Figure 14 (a)). The calculated static extinction ratio and the mean insertion loss are shown in Figure 14 (b). The values for the absorption coefficient are taken from experimental results of EMLs designed previous to this work. Based on the estimations shown in Figure 14 (a) and (b), an EAM length of 100 μm was chosen for the high power EML variant described in this work. The bandwidth is expected to exceed 30 GHz, which makes it well suited for 10 Gbaud and 28 Gbaud operation and even up to 56 Gbaud as shown in section 2.3.1. With a static extinction ratio around -8.5 dB, it offers a good modulation efficiency without having a too high insertion loss that would limit the maximum achievable output power.

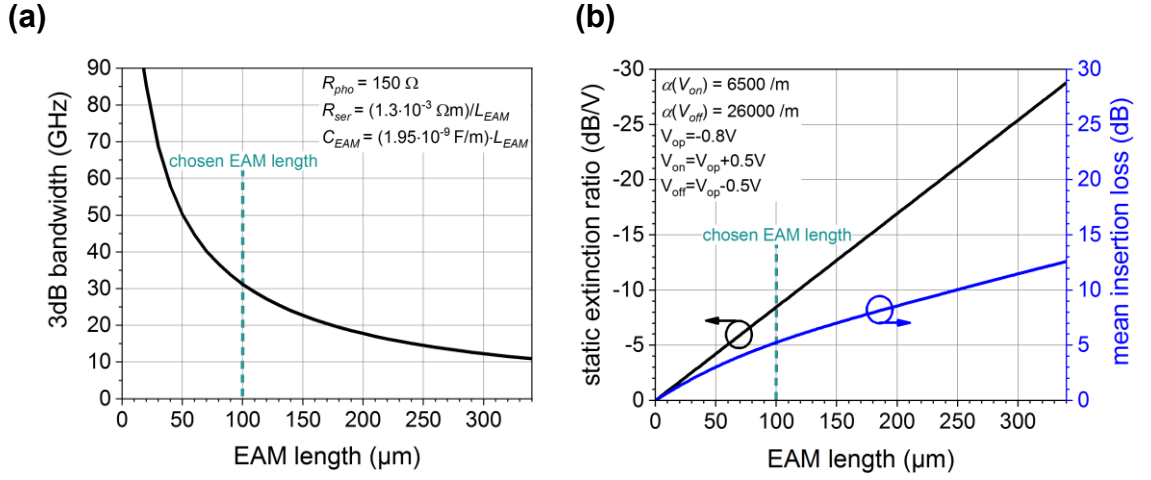


Figure 14: Estimated EAM 3dB bandwidth (a), static extinction ratio (b - black curve) and mean insertion loss (b - blue curve) for different EAM lengths. The 3dB bandwidth is calculated with (11). DC extinction ratio and the mean insertion loss are calculated with (2) and (3), respectively. Additional parameters are given in Table 4 of Appendix 1.

Optical Feedback Reduction

As mentioned in section 2.1.4, EMLs are highly sensitive to optical feedback. Already a small residual reflection of the output facet can lead to serious degradation of the modulated signal [45]. With the integration of an SOA, forward traveling output light is amplified but simultaneously any backward traveling optical feedback light will be amplified as well. This limits the maximum SOA gain that can be practicably used and thus reduces the maximum achievable output power. To minimize residual reflection, the original EML design that was developed previous to this work included anti-reflection coated facets and the output waveguide was tilted by 7°. The original EML design has proven to be sufficient for pure EML devices [14] but for the integration of SOAs, the amount of residual feedback from the facet has shown to degrade the output signal quality. In this work, this limitation is overcome

by implementing a simple change of the output waveguide profile. As shown by Marcuse et al. [46], the additional return loss due to waveguide tilt can be increased by increasing the mode field diameter (MFD) in the plane of the tilt angle. For the ridge waveguide structure used in this work, this can be achieved by increasing the width of the waveguide ridge. The optical mode field profile at the SOA output facet was simulated with the commercial software package RSoft [47] and is shown for the original design with a ridge width of $1.6\ \mu\text{m}$ in Figure 15 (a) and the new design with an increased ridge width of $3.6\ \mu\text{m}$ in Figure 15 (b). The corresponding MFD in the plane of the tilt angle (MFD_x) increases from $1.8\ \mu\text{m}$ to $3.1\ \mu\text{m}$.

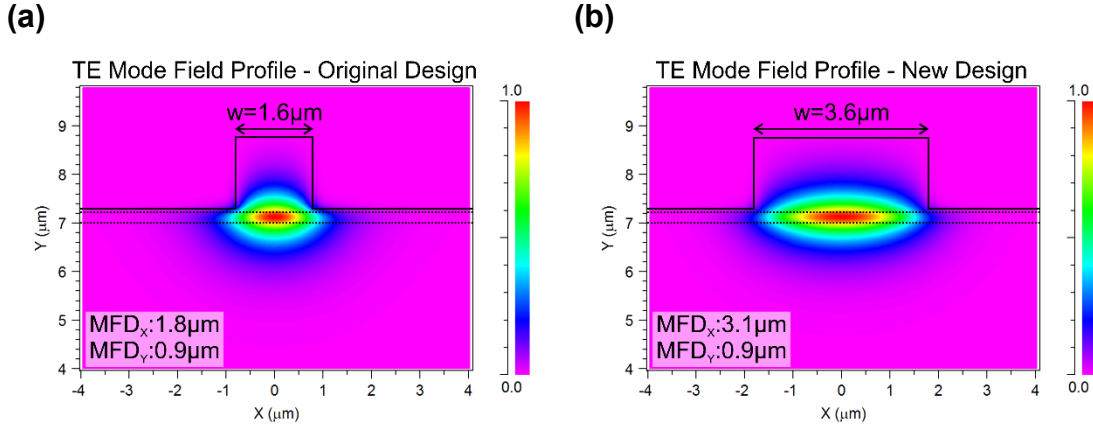


Figure 15: Simulated (RSoft) transversal electrical mode field profile at the SOA output facet for the original design (a) and the new design (b). The semiconductor to air border is indicated with solid lines and the area of the active layers with dotted lines.

Figure 16 shows the simulated additional return loss for the original design (black curve) and the new design (blue curve). The additional return loss is calculated from the overlap integral between the reflected light and the waveguide mode assuming a hundred percent reflective facet. It corresponds to the return loss that is added due to the waveguide tilt in comparison to a zero degree tilted facet. The new design with the wider ridge yields a greater return loss and local minima are visible around 7 and 10.5 degrees (c.f. Figure 16). This can be understood by describing the reflected field as the incident mode field multiplied by a phase factor $e^{i2\theta\beta x}$ where θ , β , and x are the tilt angle, the waveguide propagation constant, and the coordinate perpendicular to the reflected light beam in the plane of the tilt angle [46]. With increasing mode field diameter, the field spans over a larger distance in x , which increases the phase mismatch between the reflected field and the waveguide mode and thus reduces the overlap integral. For large MFDs and tilt angles, a part of the reflected field is shifted by a multiple of two π , which causes the overlap integral to increase again and explains the origin of the local minima in the return loss curves shown in Figure 16. It should be noted for clarity that the curve of the original design (c.f. Figure 16 (black curve)) yields

local minima at angles outside of the plotting range. For the new design, the same tilt angle (7°) as for the original design was used and the width of the ridge was chosen so that the tilt angle overlaps with a local minimum. Based on the simulation, this should give around 50 dB greater return loss compared to the original design. The minima in the return loss curve are very steep and due to fabrication tolerances, it is not realistic to assume that such high values can be reproducibly achieved. For this work, it is conservatively estimated that the additional return loss of the fabricated device is at least 20 dB greater compared to the original design. This is expected to be well sufficient for the high power EML designs targeted SOA gain of 4 dB (c.f. Figure 18 (a)).

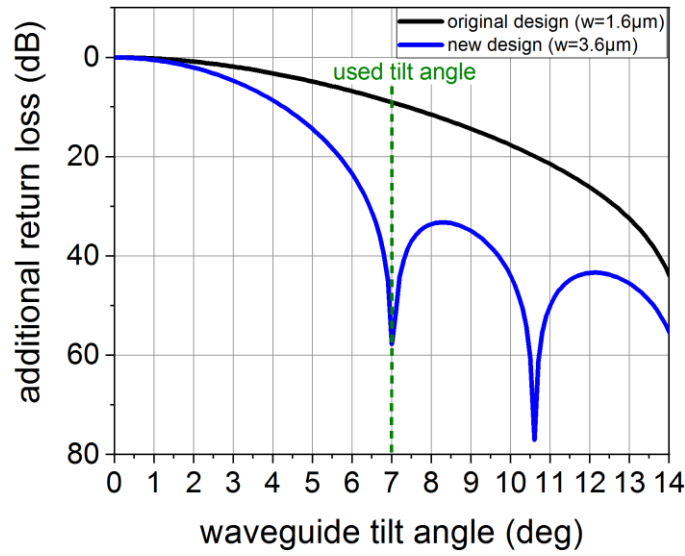


Figure 16: Simulated (RSoft) additional return loss due to waveguide tilt for the original design (black curve) and the new design (blue curve). For both designs, a tilt angle of 7° was used for fabrication.

SOA Length

A critical parameter in SOA design is the SOA length because it directly affects the two parameters that are most relevant for the amplification of modulated signals: the gain and the saturation. If the SOA is too short, it will not supply sufficient gain. If it is too long, gain saturation degrades the quality of the modulated signal. In this section, a transmission-line model of the SOA, using the commercial software VPIphotonics [48], is used to evaluate the gain and saturation tradeoff with SOA length.

The parameters for the VPI transmission-line model are extracted from the experimental results of integrated SOAs that were developed previous to this work. These SOAs are $150\ \mu\text{m}$ long with a ridge width that tapers from $2.5\ \mu\text{m}$ at the start to $1.6\ \mu\text{m}$ at the output

facet. The output power was measured for EMLs with and without integrated SOA at different DFB and SOA currents to evaluate the SOA gain and incident optical power (c.f. Figure 17 (solid lines)). The parameters of the VPI transmission-line model were fitted to match the measured gain versus incident power characteristic (c.f. Figure 17 (connected dots)). It should be noted that, due to the many parameters involved, this simple curve fitting approach is expected to yield only a rough estimation on the real device parameters. The target here is to reproduce the gain and saturation characteristic for the given device structure and then apply small structural variations (SOA length, ridge width), for which the model is expected to be still valid.

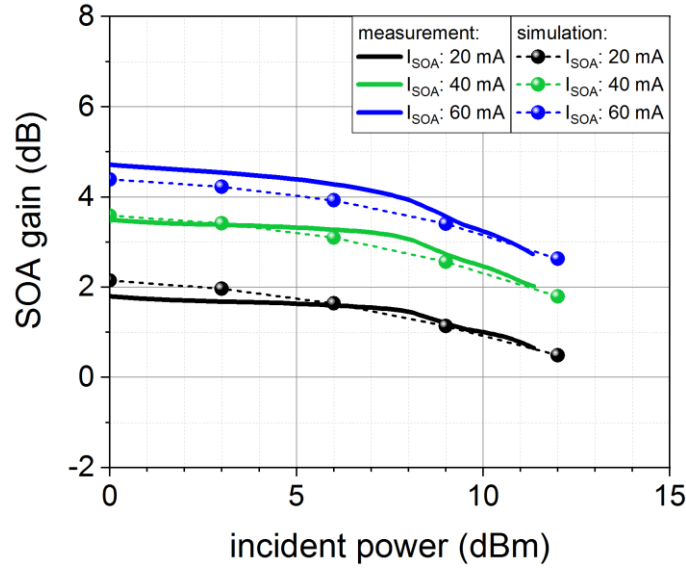


Figure 17: Measurement and simulation (VPI) of SOA gain versus incident optical power for SOA with the original design (L_{SOA} : 150 μm , w_{start} = 2.5 μm , w_{facet} = 1.6 μm). T = 50 $^{\circ}\text{C}$. Additional simulation parameters are given in Table 6 of Appendix 1.

After reproducing the gain characteristics of the old SOA design, the VPI transmission-line model is adapted to the new facet design (c.f. Figure 15) by tapering the ridge width from 2.5 μm at the start of the SOA to 3.6 μm at the output facet. In the following, this new model is evaluated for different SOA lengths for a given incident power and target output power. Based on previous measurement results on EMLs without SOA, the SOA incident power is set to 9 dBm at 0 V EAM bias voltage. The target output power is set to 13 dBm at 0 V EAM bias voltage, which complies with the launch power requirements for passive optical networks (PONs) [49], [50]. Figure 18 (a) shows the simulation results of the SOA gain for different SOA lengths and currents. To reach the target output power of 13 dBm, the SOA length should be at least 200 μm with an electrical current exceeding 80 mA. The maximum SOA length that allows good signal quality is limited by gain saturation, which increases significantly for long SOAs as can be seen in Figure 18 (b).

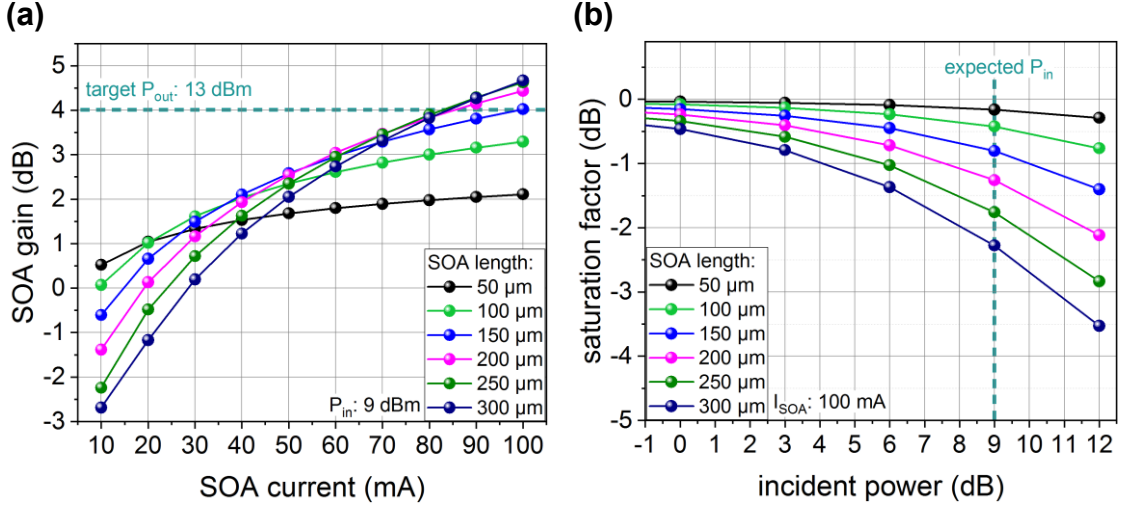


Figure 18: Simulation (VPI) of SOA gain versus SOA current (a) and saturation factor, defined in (31), versus incident optical power (b) for different lengths of SOA with the new design ($w_{start} = 2.5 \mu\text{m}$, $w_{facet} = 3.6 \mu\text{m}$). Additional simulation parameters are given in Table 6 of Appendix 1.

To evaluate the expected degree of signal degradation from saturation, the SOA transmission of a 10 Gbaud non-return-to-zero (NRZ) optical signal is simulated for different SOA lengths (c.f. Figure 19). At 100 μm SOA length, no signal degradation is visible, but the gain is not sufficient to reach the desired output power target. At 200 μm SOA length, slight effects of SOA saturation start to show in the form of increased noise from overshoots at the one-level. At 300 μm SOA length, SOA saturation leads to strong overshoots and significant degradation of the eye diagram. To keep signal degradation from saturation to a minimum while achieving the desired target output power, an SOA length of 200 μm is chosen for the high power EML design in this work.

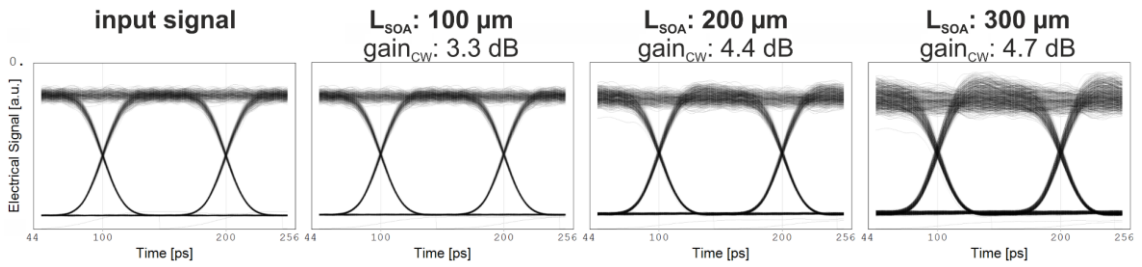


Figure 19: Simulation (VPI) of 10 Gbaud NRZ optical eye diagram after transmission through SOA with the new design ($w_{start} = 2.5 \mu\text{m}$, $w_{facet} = 3.6 \mu\text{m}$) at different SOA lengths. $P_{in_SOA_one-lvl} = 9 \text{ dBm}$, $P_{in_SOA_zero-lvl} = -1 \text{ dBm}$, $I_{SOA} = 100 \text{ mA}$. Additional simulation parameters are given in Table 6 of Appendix 1.

2.2.2 EML Array

The EML array design and fabrication were carried out prior to this work and thus the focus within this thesis lies in its experimental characterization (c.f. section 2.3.2). In the following, the design of the EML array structure is described and the concept behind it is explained.

The primary target of the EML array design is to reduce packaging costs. By integrating several chips into an array, the number of required assembly steps for multichannel transmitter modules is greatly reduced, which simplifies the packaging process and increases packaging yield. The challenge in designing an array is that it is not possible to fully optimize each component individually but rather the array has to be considered as a whole. This is particularly true for devices with an identical epitaxial layer design (c.f. Figure 3 (a)) where all components share the same epitaxy. The focus of the EML array design described in this work lies in achieving equal device performance over the different wavelength channels in the array and further simplifying packaging. The basic design is similar to that of the high power EML described in section 2.2.1. The differences will be described in the following. The EML array comprises four EMLs, each with integrated SOA, that are monolithically integrated to a single array chip (c.f. Figure 20) with an identical epitaxial layer design with a single type MQW (c.f. Figure 3 (a)). The EML array is from a device generation previous to the high power EML described in section 2.2.1, and thus it comprises the old SOA design ($w_{start} = 2.5 \text{ } \mu\text{m}$, $w_{facet} = 1.6 \text{ } \mu\text{m}$). The electrical contacts of the DFBs, EAMs, and SOAs are routed to the backside of the chip to allow for easy wire bonding with short wire bonds when mounted on a carrier for packaging (c.f. Figure 20). In contrast to the high power EML design, the EML array has an anti-reflection coated back facet. This is to ensure a high single-mode yield, which typically cannot be achieved with a reflective facet [51]. High single mode yield is critical for array structures as the yield of the full array corresponds to the yield of the individual EML raised to the power of the number of EMLs in the array. With an anti-reflection coated back facet, roughly half of the optical power generated by the DFB is lost through the backside of the chip, which decreases the power conversion efficiency of the device. The integrated SOA offers the advantage that it allows boosting the output power at the front facet of the chip, which improves the total power conversion efficiency. The target operating temperature of the EML array is 20 °C. At this reduced temperature, the EML array can achieve output power levels that are comparable to the high power EML, which targets 50 °C operation (c.f. section 2.2.1). The EML array comprises four EMLs that operate at four different wavelength channels in the L-Band. The wavelength spacing is 2.5 nm, which covers a wavelength span of 7.5 nm for the full array. Since all EMLs in the array share the same epitaxy, the detuning of the lasing wavelength to the gain and absorption

spectrum of the DFB and EAM section is different for each wavelength channel in the array. For the DFBs, this leads to different threshold currents and output powers, which can be compensated by applying different currents to the SOAs. For the EAMs, the different detunings lead to different extinction ratios and EAM capacitances. Typically, the extinction ratio and the capacitance are decreased with a larger detuning. As shown in Figure 14, these parameters can be adjusted by choosing different EAM lengths. For the EML array described in this work, the EAM length is 80 μm for the two shorter wavelengths (lower detuning) and 100 μm for the two longer wavelengths (larger detuning). This allows achieving a similar performance regarding extinction ratio and bandwidth for the different wavelength channels in the array as will be shown in section 2.3.2. The length of the DFB is 450 μm for all four EMLs, the length of the SOA is 170 μm and 150 μm for the two shorter and the two longer wavelengths, respectively. The total length of the EML array, including separation trenches, is 740 μm and the width is 2560 μm .

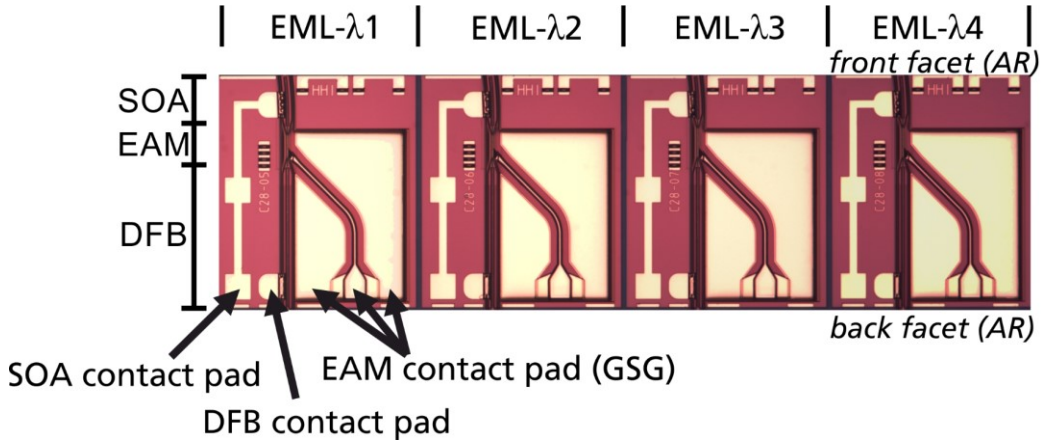


Figure 20: Top view of a fabricated EML array chip with monolithically integrated DFB, EAM, and SOA section. The front and back facets are anti-reflection (AR) coated and the waveguide is tilted by 7° towards the front facet. The DFB and SOA contacts pads and the ground-signal-ground (GSG) contact pads of the EAM are routed to the backside of the chip. Target wavelengths are λ_1 : 1569.25 nm, λ_2 : 1571.75 nm, λ_3 : 1574.25 nm, λ_4 : 1576.75 nm. Chip dimensions are 2560 μm x 740 μm .

2.3 Experimental Characterization

In this section, the experimental characterization of the EML devices described in section 2.2 is carried out. All experiments were performed with devices mounted on temperature-controlled heatsinks. Needle probes were used for electrical contacting of the DFB and SOA sections. An RF-probe with integrated 50 Ω termination resistance was used for the electrical contacting of EAM sections in GSG configuration. For the evaluation of

facet output power, the output light was measured with an integrating sphere. For all other measurements, the output light was coupled to a single-mode fiber with an optical isolator (-30 dB) to mitigate optical feedback from the measurement setup. The single-mode fiber had an anti-reflection coated and lensed fiber tip with a spot size of 3.5 μm .

2.3.1 High Power EML

As described in section 2.2.1, the design target of the high power EML is to realize an EML with high optical output power at semi-cooled operation (50°C). This makes it an ideal candidate for PON applications, which require a high output power together with a high extinction ratio to compensate for the overall high losses of the passive optical network. In the following, the high power EML with the new design described in 2.2.1 is experimentally characterized with regard to its suitability for 10G-PON (XG-PON) [49] and next-generation PON (NG-PON2) [50]. Both standards specify optical transmitters for up to 10 GBd NRZ modulation with a mean optical output power around 9 dBm and a minimum extinction ratio of 8.2 dB. At the end of this section, an experimental outlook for high-speed operation (56 GBd) of the high power EML will be given.

DC Characterization

For EMLs that are operated at the EAMs operation point bias voltage (c.f. Figure 5 (b)), it can be estimated that the mean optical power of a modulated signal is about 3 dB to 4 dB lower than the DC power at 0 V EAM bias. So to achieve the targeted 9 dBm mean optical output power [49], [50], the target for the optical power at 0 V EAM bias is set here to 13 dBm. Figure 21 (a) shows the measured optical ex-facet output power of the high power EML (solid lines) and an EML without SOA (dashed line) at 0 V EAM bias for various DFB and SOA currents. The devices exhibit a threshold current of 27 mA. At 0 mA SOA current, the power of the high power EML is reduced compared to the EML without SOA due to absorption in the SOA. At SOA currents exceeding 20 mA, the SOA amplifies the output power. The target output power of 13 dBm is achieved for 87 mA and 80 mA of DFB and SOA current, respectively. For the corresponding incident power of 9 dBm, Figure 21 (b) shows the SOA gain calculated from the measurements in (a) and the simulation results from the VPI model described in section 2.2.1. The simulation results show good overlap with the measurement, there is only a slight deviation for the highest and the lowest currents.

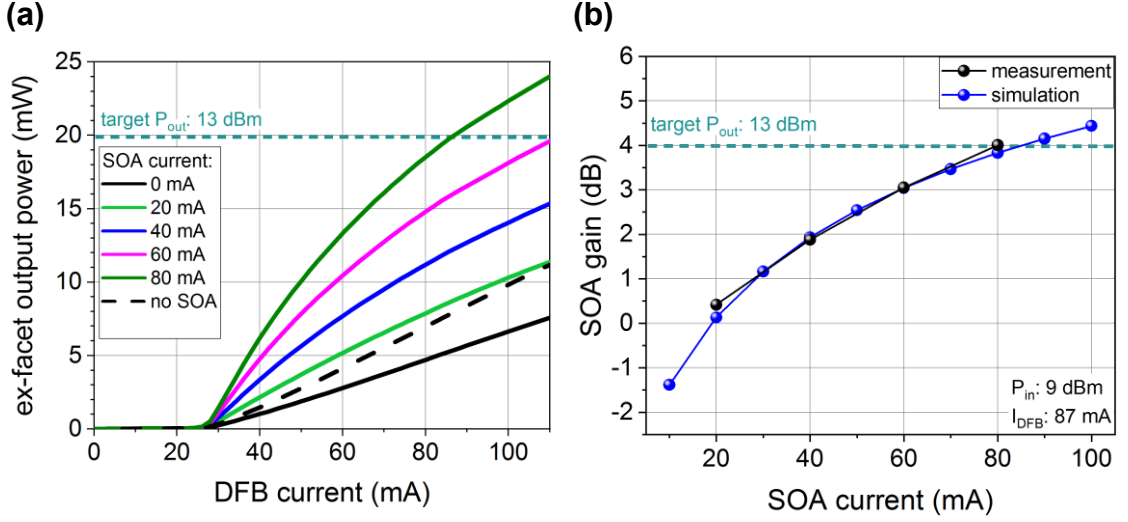


Figure 21: Measured cw ex-facet output power of high power EML and EML without SOA at different DFB and SOA currents (a). Measurement and simulation of SOA gain versus SOA current (b). The measured SOA gain is calculated by comparing the measured output power of the EML with and without SOA in (a). $V_{EAM} = 0V$, $T = 50^\circ C$.

Figure 22 (a) shows the measured ex-facet output power of the high power EML versus EAM bias voltage. The most linear regime, which is defined here as the operation point, is at $-0.85 V$. With increasing SOA current, the output power increases without a significant change of the static extinction ratio curve (c.f. Figure 22 (b)). For SOA currents above 0 mA, the absolute extinction ratio at large EAM bias voltages is slightly reduced, which can be attributed to the amplified spontaneous emission (ASE) of the SOA. The SOA ASE is typically in the order of μW and thus it is only significant at large EAM bias voltages at which the optical power that passes the EAM section is in a comparable order of magnitude. The static extinction ratio for 1 V peak-to-peak voltage swing around the operation point is 9.5 dB for 80 mA SOA current. This is 1 dB higher than the estimated value from the design section 2.2.1.

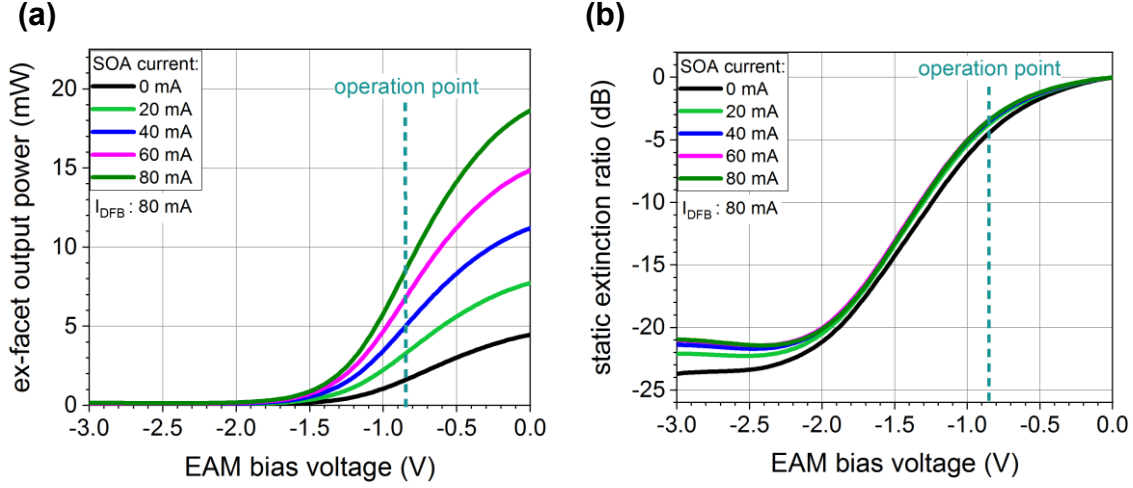


Figure 22: Measured ex-facet output power of high power EML (a) and static extinction ratio (b) versus EAM bias voltage for different SOA currents. $T = 50\text{ }^{\circ}\text{C}$.

Small-Signal Characterization

The small-signal frequency response of EMLs with integrated SOA is determined by the EAMs capacitances, inductances, and resistances as well as optical feedback and SOA saturation. In section 2.1 an analytical frequency response function (34) was derived that allows the extraction of these individual parameters by fitting. When using a fitting function with multiple parameters, it has to be taken into account that a single curve can be fitted by a multitude of different parameter sets. In the following, this ambiguity is mitigated by fixing the majority of the fitting parameters of (34) to values extracted via separate measurements or to values known otherwise (c.f. Table 4 of Appendix 1). Figure 23 (a) shows exemplarily the measured (dashed lines) frequency response of the high power EML together with the fitted curves (solid lines) for three different EAM biases with 0 mA SOA current. With the SOA turned off, no relevant saturation or optical feedback influence is visible and thus the saturation factor a_{sat} and the optical feedback parameter A_F are set to zero. The parameter R_{pho} is extracted from separate photocurrent measurements (c.f. section 2.1.5) and set to the fixed values shown in the inset. Using a Levenberg-Marquardt algorithm with C_{EAM} as only fitting parameter, the function (34) is fitted to the measurement. The fitted curves show good agreement with the measurement. The EAM capacitance C_{EAM} decreases from 293 fF to 205 fF for -0.5 V to -1.3 V. It is interesting to see that despite the capacitance decrease for -0.9 V to -1.3 V the 3 dB bandwidth stays nearly constant around 27 GHz. This can be attributed to the lower photocurrent resistance at -0.9 V, which compensates for the increased capacitance. Figure 23 (b) shows the EAM capacitance C_{EAM} extracted via fitting for different EAM bias voltages and DFB currents. The EAM capacitance exhibits a strong dependence on the DFB current and EAM bias voltage. At large DFB currents and small

EAM biases, the capacitance increases up to more than 350 fF. This effect can be explained by an increased carrier pileup and a reduction of the space charge region at high optical input powers and low bias voltages as described in section 2.1.5. It can be concluded that to achieve a low EAM capacitance, a high EAM bias and a low DFB current are preferable, which has the drawback that it results in low output power. This emphasizes the advantage of integrating an SOA after the EAM section, as it allows increasing the output power without affecting the EAM capacitance.

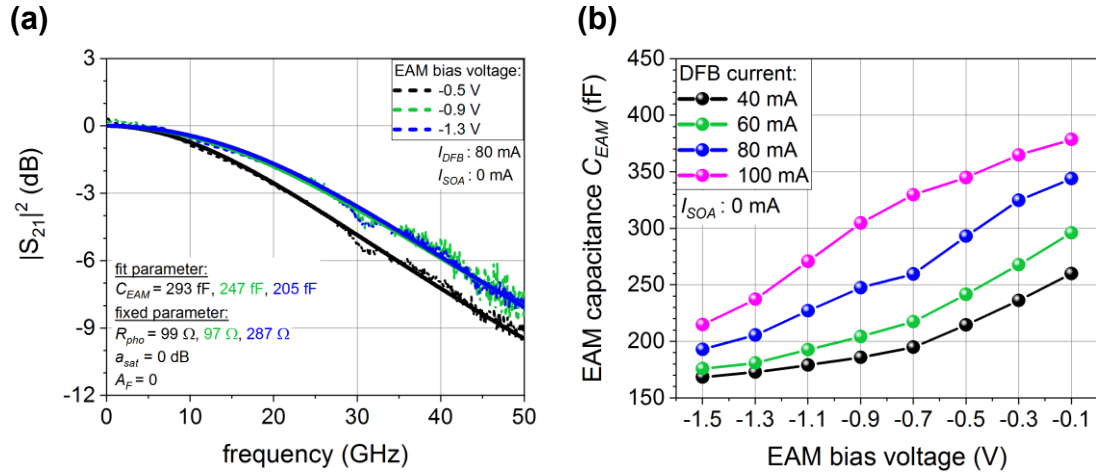


Figure 23: Measured (dashed lines) and fitted (solid lines) frequency response of high power EML for different EAM bias voltages (a). EAM capacitance versus EAM bias voltage for different DFB currents extracted via fitting (b). Function (34) was used as fitting function. Additional fixed parameters are given in Table 4 of Appendix 1. $T = 50$ °C.

Next, the frequency response at different SOA currents is evaluated with fixed values for C_{EAM} (c.f. Figure 23 (b)) and variable values for the optical feedback and saturation parameters. Figure 24 shows exemplarily the measured (dashed lines) and fitted (solid lines) frequency response for different SOA currents at an EAM bias (-0.9 V) close to the operation point (-0.85 V). With increasing SOA current, saturation and a slight influence of optical feedback start to show. The saturation is visible in the form of a drop of the response curve towards low frequencies (<4 GHz). The optical feedback influence can be seen by the resonance around 7 GHz. The effects of saturation and optical feedback are well reproduced by the fitting function. Figure 25 (a) shows the fitting results for the saturation factor a_{sat} at different DFB and SOA currents and -0.9 V EAM bias voltage. Saturation increases with higher DFB current due to the increased optical input power at the SOA. The saturation factor also shows a dependence on the SOA current, which is especially strong for low SOA currents (<60 mA). The saturation factor dependence on the EAM bias voltage for 100 mA SOA current is shown in Figure 25 (b). For large EAM bias values at which the SOA input

power is low the saturation is low. It increases significantly for small EAM bias voltages at which the SOA input power is high. The largest saturation factor is -1.7 dB at 100 mA DFB current. The corresponding SOA input power at that point is estimated to be close to 10 dBm (Figure 21 (a –black dashed line)). The measured saturation factor of -1.7 dB shows good agreement with the saturation factor expected from the simulation ($a_{sat} \sim -1.6$ dB at P_{in} : 10 dBm, L_{SOA} : 200 μ m in Figure 18).

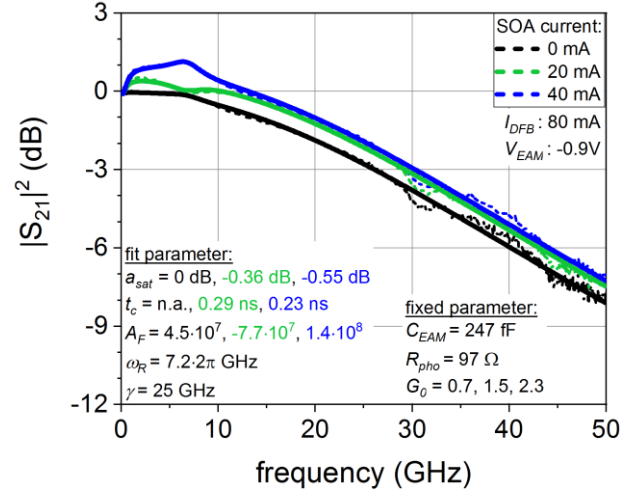


Figure 24: Measured (dashed lines) and fitted (solid lines) frequency response of high power EML for different SOA currents. Function (34) was used as the fitting function. Additional fixed parameters are given in Table 4 of Appendix 1. $T = 50$ °C.

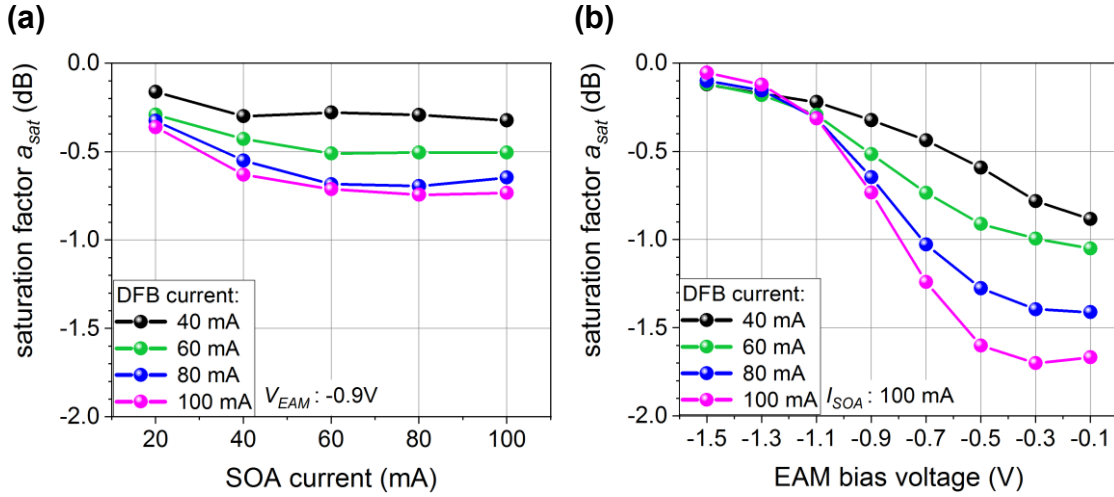


Figure 25: Saturation factor versus SOA current (a) and EAM bias voltage (b) for different DFB currents extracted via fitting. Function (34) was used as the fitting function. Additional fixed parameters are given in Table 4 of Appendix 1. $T = 50$ °C.

Large Signal - 10 GBd NRZ

In this section, the high power EML is evaluated regarding its performance for 10 GBd NRZ modulation, which corresponds to the highest line rate specified in 10G-PON (XG-PON) [49] and next-generation PON (NG-PON2) [50]. The measurements were carried out using the measurement setup shown in Figure 26.

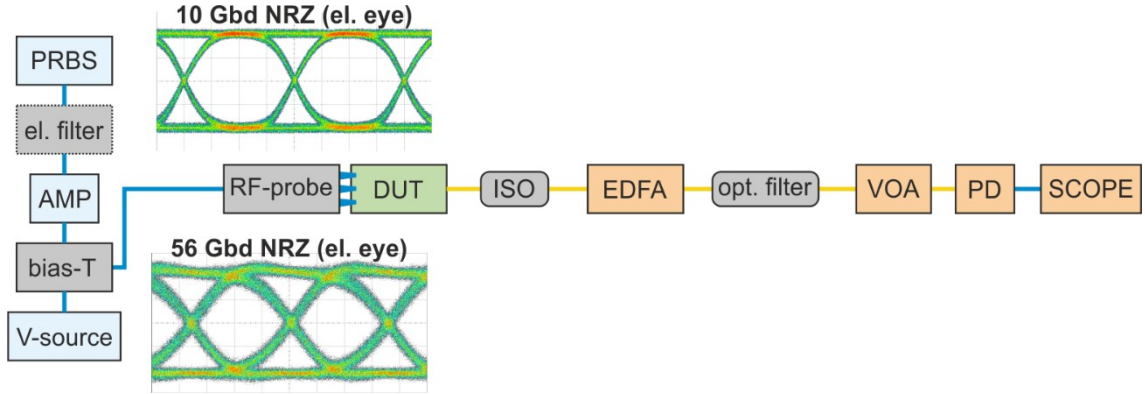


Figure 26: Large signal measurement setup. An NRZ signal is generated at the output of a SHF12103A bit pattern generator (PRBS) and filtered by a 7.46 G electrical filter (el. filter) for the 10 GBd measurements (for 56 GBd the filter is removed). The electrical signal is amplified by an SHF804EA electrical amplifier (AMP) and combined at a SHFBT65T bias tee (bias-T) with the bias of a DC voltage source (V-source). The electrical signal is applied in ground-signal-ground configuration to the EML (DUT) with an RF-probe that comprises a 50 Ohm matching resistor. The optical output of the EML is coupled to a lensed fiber that is connected to an optical isolator (ISO, return loss: 30 dB). The combination of the erbium-doped fiber amplifier (EDFA) and the optical attenuator (VOA) is used to control the input power at the high bandwidth photodiode (PD). An optical filter (opt. filter, band-pass: 3 nm) is used to reduce the contribution of amplified spontaneous emission of the EDFA. The electrical signal of the photodiode was recorded with a Keysight 86118a sampling scope (SCOPE).

The EAM bias voltage was set to -0.85 V, which corresponds to the device's operation point voltage (c.f. Figure 22). The peak-to-peak voltage swing was set to 2 V. Figure 27 (a) shows the mean ex-facet output power of the modulated signal for different DFB and SOA currents. By increasing the SOA current, the mean output power is significantly increased. The targeted output power of 9 dBm is exceeded for 80 mA DFB current and 100 mA SOA current or 80 mA DFB current and 100 mA SOA current. The corresponding dynamic extinction ratio is shown in Figure 27 (b). The extinction ratio is well above the target of 8.2 dB for all currents. The extinction ratio decreases with the DFB current and increases with SOA current. The former can be explained by a smaller photocurrent resistance with higher optical input power at the EAM, which leads to a reduction of the voltage swing at the active layers as described in section 2.1.5. The reason for the increase of the dynamic extinction ratio with SOA current is unclear. A possible explanation would be that electrical

heating from the SOA affects the EAM, but this contradicts with the static extinction ratio curve, which does not show this effect (c.f. Figure 22).

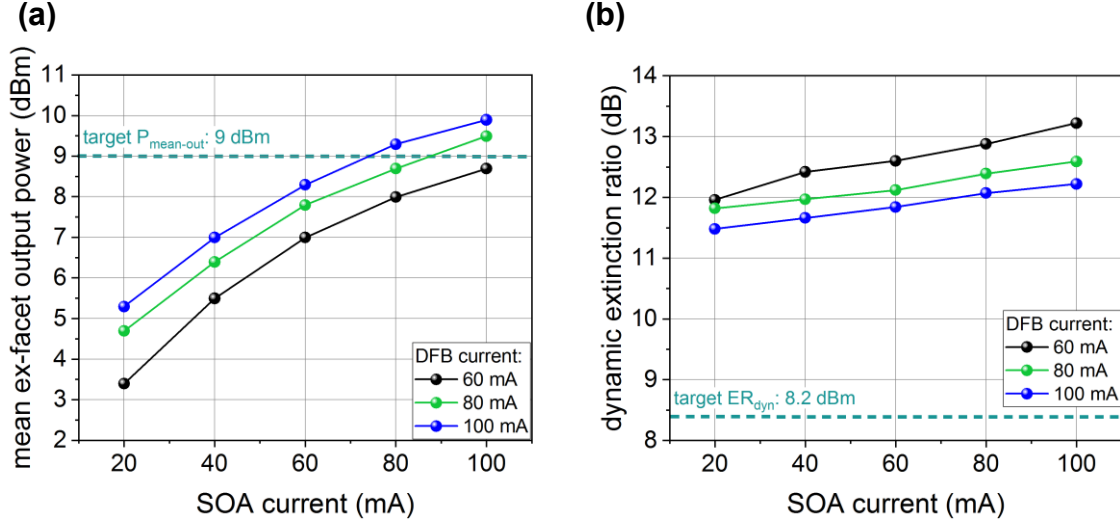


Figure 27: Mean ex-facet output power (a) and dynamic extinction ratio (b) for high power EML operated at 10 GBd NRZ. The target values for PON applications [49], [50] are marked by a dashed line. PRBS $2^{31}-1$, $V_{pp} = 2$ V, $V_{EAM} = -0.85$ V, $T = 50$ °C.

A DFB current of 80 mA and 100 mA SOA current is chosen as preferred operation conditions, as it complies with the targeted specs and shows a lower EAM capacitance, lower saturation, and higher dynamic extinction ratio compared to 100 mA DFB current (c.f. Figure 23, Figure 25, Figure 27). The corresponding measured 10 GBd NRZ eye diagram is shown in Figure 28 for back-to-back and 20 km fiber transmission. The ex-facet output power was 9.5 dB with a dynamic extinction ratio of 12.6 dB. No significant influence of optical feedback or SOA saturation is visible. Good eye quality is achieved in back-to-back configuration and after 20 km of single-mode fiber transmission. Overall, the high power EML proves to be well suited for 10G-PON (XG-PON) [49] and next-generation PON (NG-PON2) [50] applications.

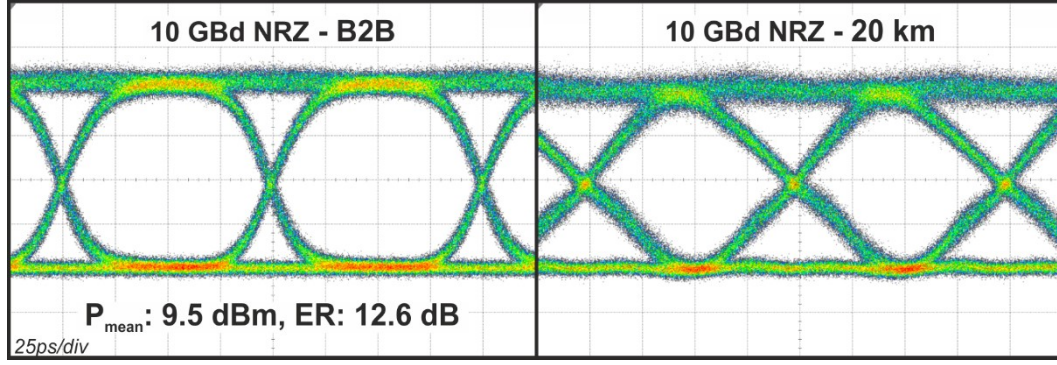


Figure 28: 10 GBd NRZ optical eye diagrams of high power EML for back-to-back (a) and after 20 km single-mode fiber transmission (b). PRBS $2^{31}-1$, $V_{pp} = 2$ V, $V_{EAM} = -0.85$ V, $I_{DFB} = 80$ mA, $I_{SOA} = 100$ mA, $\lambda_{DFB} = 1579$ nm, $T = 50$ °C.

Large Signal – Influence of Optical Feedback

A critical limitation for SOA integration to EMLs is the amplification of optical feedback. To allow for a high SOA gain, optical feedback has to be kept to a minimum. In section 2.2.1, a new facet design was introduced that significantly reduces optical feedback from the output facet (c.f. Figure 16). In the following, a direct comparison of the optical feedback influence on the 10 GBd NRZ eye quality is carried out for the new and old facet design. It should be noted that the effects of optical feedback are particularly strong at 10 GBd, as the baud rate is close to the relaxation oscillation frequency ω_R of the DFB laser (c.f. Figure 24). Figure 29 shows the measured 10 GBd NRZ eye diagram of two high power EML variants that are structurally identical apart from one having the old facet design (left) and the other having the new facet design (right). In back-to-back configuration, only a slight difference in eye quality is visible. The EML with the old design shows some distortion on the one-level and the downwards slope (Figure 29 (top)). After 20 km of fiber transmission, the eyes exhibit a significant difference. The EML with the old design shows huge distortions in the form of overshoots and eye closure that greatly degrade the eye quality (Figure 29 (middle)). The reason for this can be understood when one looks at the corresponding optical spectra under modulation (Figure 29 (bottom)). The new design shows a sharp peak with a width that corresponds to the 10 pm resolution bandwidth of the optical spectrum analyzer. For the old design, the spectrum is significantly widened to a width of 60 pm, which in turn will lead to increased dispersion effects in fiber transmission. The widening of the lasing spectrum and the corresponding distortion of the eye diagram can be attributed to the stronger optical feedback of the old facet design. The simple method of widening the ridge width at the output facet in the new facet design as described in section 2.2.1, proves to be highly beneficial in optical feedback mitigation.

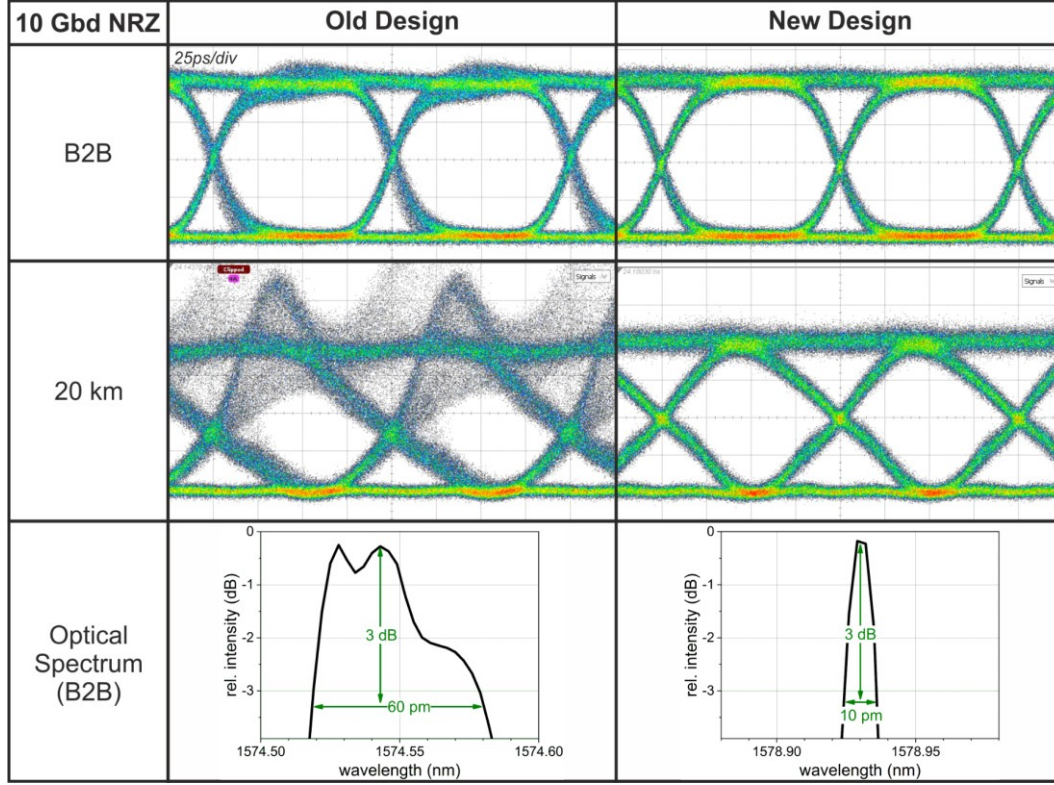


Figure 29: 10 GBd NRZ optical eye diagrams of high power EML with old (left) and new (right) facet design (c.f. Figure 15) for back-to-back (top) and after 20 km single-mode fiber transmission (middle) with the corresponding optical spectra under modulation (bottom). PRBS $2^{31}-1$, $V_{pp} = 2$ V, $V_{EAM} = -0.85$ V, $I_{DFB} = 80$ mA, $I_{SOA} = 80$ mA, $T = 50$ °C.

Large Signal - 56 GBd NRZ

To give an outlook to the potential of the high power EML for higher speed operation, its performance at 56 GBd NRZ modulation is tested. The same measurement setup as shown in Figure 26 was used with the PRBS source set to generate a 56 GBd NRZ signal and the electrical filter removed. The measured eye diagrams for a DFB current of 80 mA with different SOA currents is shown in Figure 30. The same eye quality is maintained for all SOA currents and no negative influence from the SOA is visible. Although the eyes are clear and open, slight eye closure is visible, which can be attributed to bandwidth limitation (c.f. Figure 23). The eye closure leads to a reduced dynamic extinction ratio and lower mean output power compared to the 10 GBd NRZ operation. Still, more than 9 dB extinction ratio and up to 9 dBm mean ex-facet output power are achieved. Overall, the high power EML proves to be a promising candidate for high-speed applications up to 56 GBd. Performance improvement is expected from an increased EAM bandwidth, which could be achieved for example by choosing a higher operation point voltage (c.f. Figure 23) or by reducing the EAMs length (c.f. Figure 14).

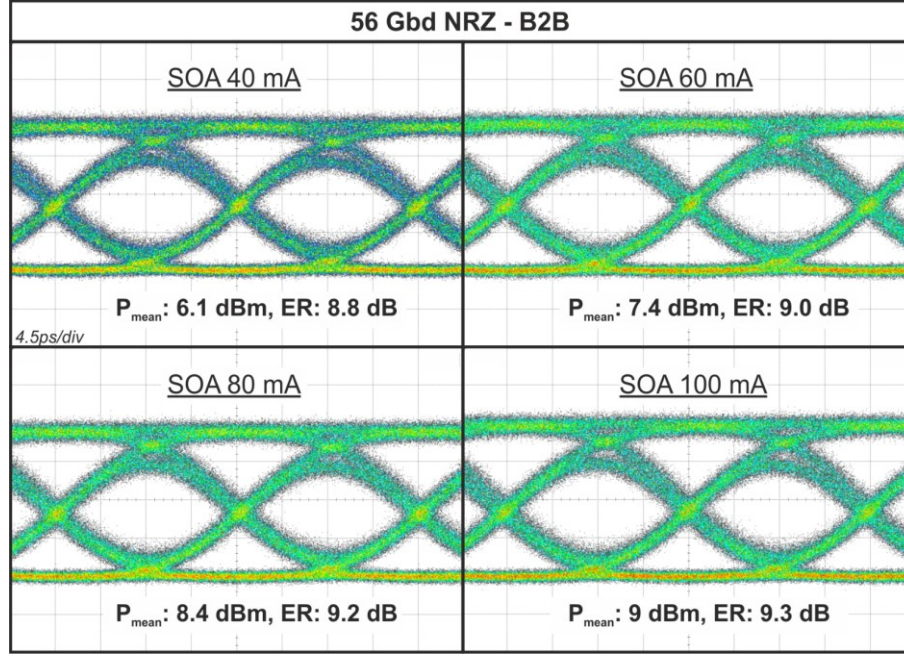


Figure 30: 56 GBd NRZ back-to-back optical eye diagrams of high power EML for different SOA currents. PRBS $2^{31}-1$, $V_{pp} = 2 \text{ V}$, $V_{EAM} = -0.85 \text{ V}$, $I_{DFB} = 80 \text{ mA}$, $T = 50 \text{ }^{\circ}\text{C}$.

2.3.2 EML Array

As described in section 2.2.2, the EML array is designed to operate at four different wavelength channels that span over 7.5 nm in the L-band. To achieve equal performance over all wavelength channels, the EML array comprises integrated SOAs and different EAM lengths. In the following, the DC and RF characteristic of the EML array is investigated, with a focus on the uniformity of channel performance. Parts of these results have been previously published in [52], [53].

DC Characterization

To provide the high single-mode yield that is required for array structures, the EML array design comprises anti-reflection coated back facets (c.f. section 2.2.2). To evaluate the effectiveness of this approach, a yield analysis for the side mode suppression ratio (SMSR) is performed on full laser bars. For a given minimum SMSR of 35 dB, the individual EMLs show a single-mode yield of 97.5% (cf. Figure 31). Since all EML in a functional array have to be single-mode, the single-mode yield of the $N=4$ array corresponds to $(97.5\%)^{N=4} = 90\%$. The average SMSR was 45 dB. It should be noted that this value might be slightly higher because SMSR values exceeding 50 dB could not be measured due to the limited sensitivity of the optical spectrum analyzer that was used.

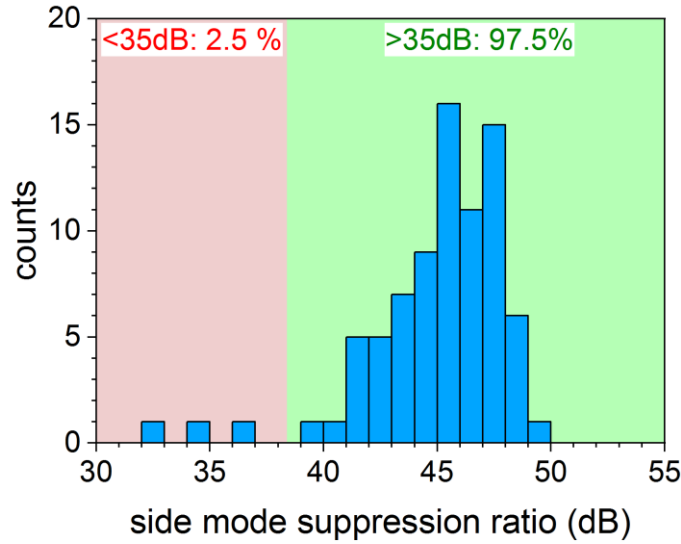


Figure 31: Histogram of side mode suppression ratio for EML Array type devices. Each count corresponds to an individual EML of an array. Measured with an automated bar test system. Total sample count = 80, $I_{DFB} = 80$ mA, $I_{SOA} = 0$ mA, $V_{EAM} =$ open contact, $T = 20$ °C.

The pre-characterized laser bars were diced into 4-arrays that were then mounted on heatsinks for detailed characterization. Figure 32 (a) shows the optical spectra of such an EML array. The wavelength of the EMLs in the array range from 1569.4 nm to 1576.9 nm with a wavelength spacing of 2.5 nm. A high SMSR exceeding 40 dB is achieved for all four wavelengths. Figure 32 (b) shows the wavelength shift that occurs due to electrical heating when the output power is changed via tuning of either the DFB or the SOA current. Here the integrated SOA shows a great advantage regarding wavelength division multiplexing applications that require accurate wavelength control. As the SOA is integrated at a distance to the DFB grating (c.f. Figure 20), it allows adjusting the optical output power over several dB with a shift of the lasing wavelength of less than 0.1 nm (c.f. Figure 31 (b) “SOA tuning”). On the other hand, it allows for wavelength tunability by changing the DFB current and adjusting the SOA current to maintain a constant output power. For the device shown here, the tuning range is estimated to be about ± 0.2 nm (c.f. Figure 31 (b) “DFB tuning”).

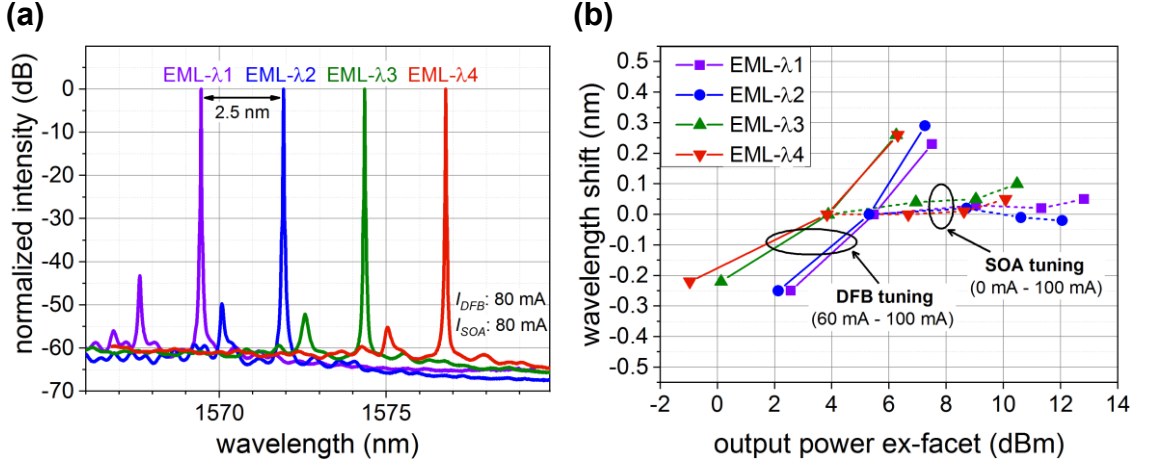


Figure 32: Measured optical spectra of the EML array (a) and wavelength shift versus optical output power for different DFB and SOA currents (b). V_{EAM} = open contact, $T = 20$ °C.

Figure 33 (a) shows the measured output power versus DFB current for a constant SOA current of 40 mA. The EML exhibit a threshold current from 33 mA (EML-λ1) to 50 mA (EML-λ4). The difference in threshold currents corresponds to the difference in wavelength detuning to the gain maximum of the identical active layer epitaxy. By setting different SOA currents for each EML, an equal output power over all four EMLs can be achieved. The different wavelength detuning of each EML also results in a difference in the operation point bias voltage from -1.1 V to -1.5 V (c.f. Figure 33 (b)). Due to a reduced overlap integral of the electron and hole wave functions at high voltages (c.f. section 2.1.2), the extinction ratio is reduced with increasing operation point voltage. By choosing two different EAM section lengths of 80 μ m and 100 μ m to compensate for the reduction, a static extinction ratio in the range of 6 dB/V to 8 dB/V is maintained over the whole array (c.f. Figure 33 (b)).

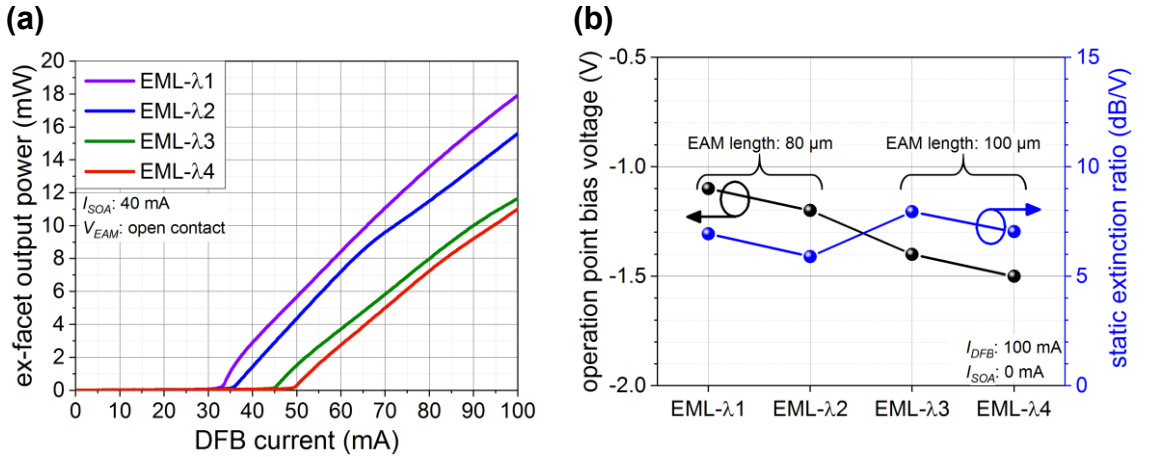


Figure 33: Measured cw ex-facet output power versus DFB current (a), operation point bias voltage, and corresponding static extinction ratio at operation point (b) of the EML array. $T = 20$ °C.

Small-Signal Characterization

Figure 34 shows the frequency response measurement of the EML array for different SOA currents and with the EAM bias set to the operation point bias voltages. With increasing SOA current, the influence of optical feedback is visible in the form of strong resonant peaks around 7 GHz, which can be attributed to residual reflection from the front facet. It has been shown in section 2.2.1 and 2.3.1 that such optical feedback can be significantly reduced with a new facet design, which should be preferred for future EML array generations. From Figure 34, it is not possible to exactly quantify the optical feedback strength because it depends on the optical phase of the reflected light (c.f. equation (21)), which is not known. On a qualitative measure, it can be seen that EML- λ_1 and EML- λ_2 seem to experience stronger optical feedback than EML- λ_3 and EML- λ_4 (c.f. Figure 34). This can be explained by the shorter EAM length and the lower wavelength detuning of EML- λ_1 and EML- λ_2 , which results in a lower EAM absorption and a higher SOA amplification of optical feedback light. Additional to the optical feedback, the curves in Figure 34 exhibit SOA saturation in the form of a drop in magnitude towards 0 GHz.

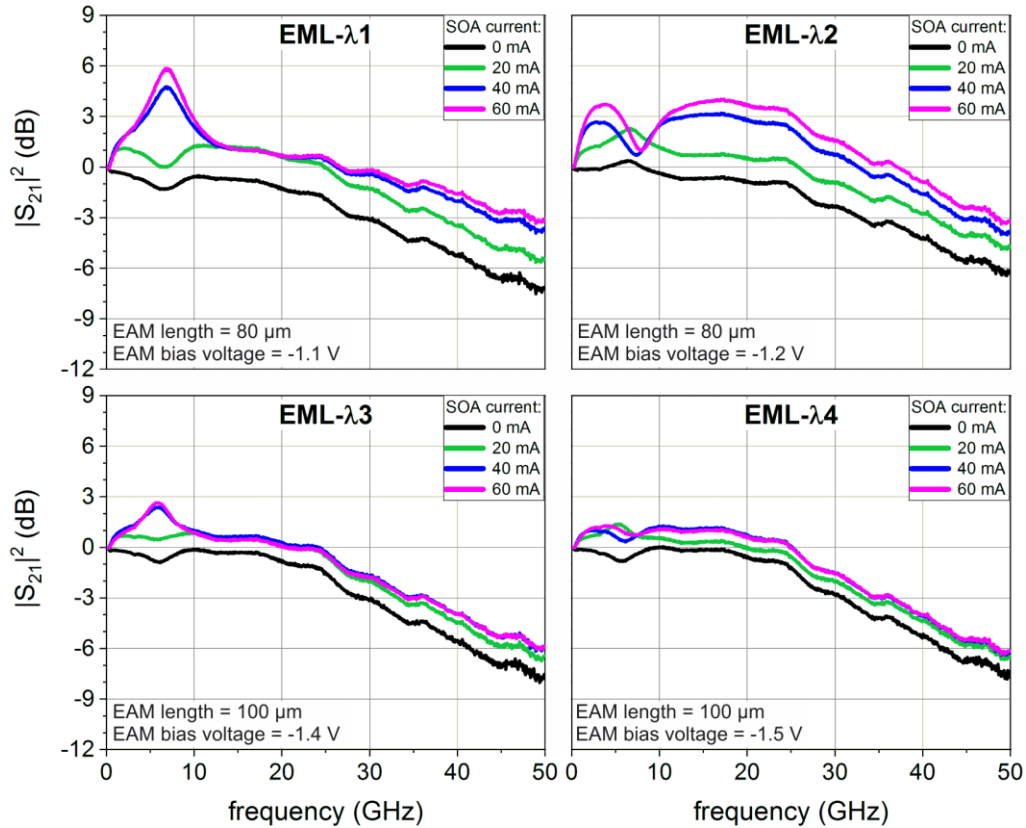


Figure 34: Measured frequency response of the EML array for different SOA currents. $I_{DFB} = 100$ mA, $T = 20$ °C.

The strong influence of optical feedback together with SOA saturation makes curve fitting with (34) challenging because less fitting parameters can be fixed and thus results become ambiguous. For very strong optical feedback and SOA saturation (e.g. $SOA \geq 40$ mA in Figure 34) the model from which (34) was derived also seems to be at its limit, as curve fitting in this regime yielded inconclusive results. To resolve these issues, the measured frequency response and the reflection coefficient were simultaneously fitted with the fitting functions (34) and (12), respectively (c.f. Figure 35). A Levenberg-Marquardt algorithm with parameters shared for both fitting functions was used. Because the reflection coefficient (12) is a purely electrical function, it allows decoupling the electrical parameters, such as the EAM capacitance C_{EAM} , from optical parameters, such as the optical feedback strength A_F .

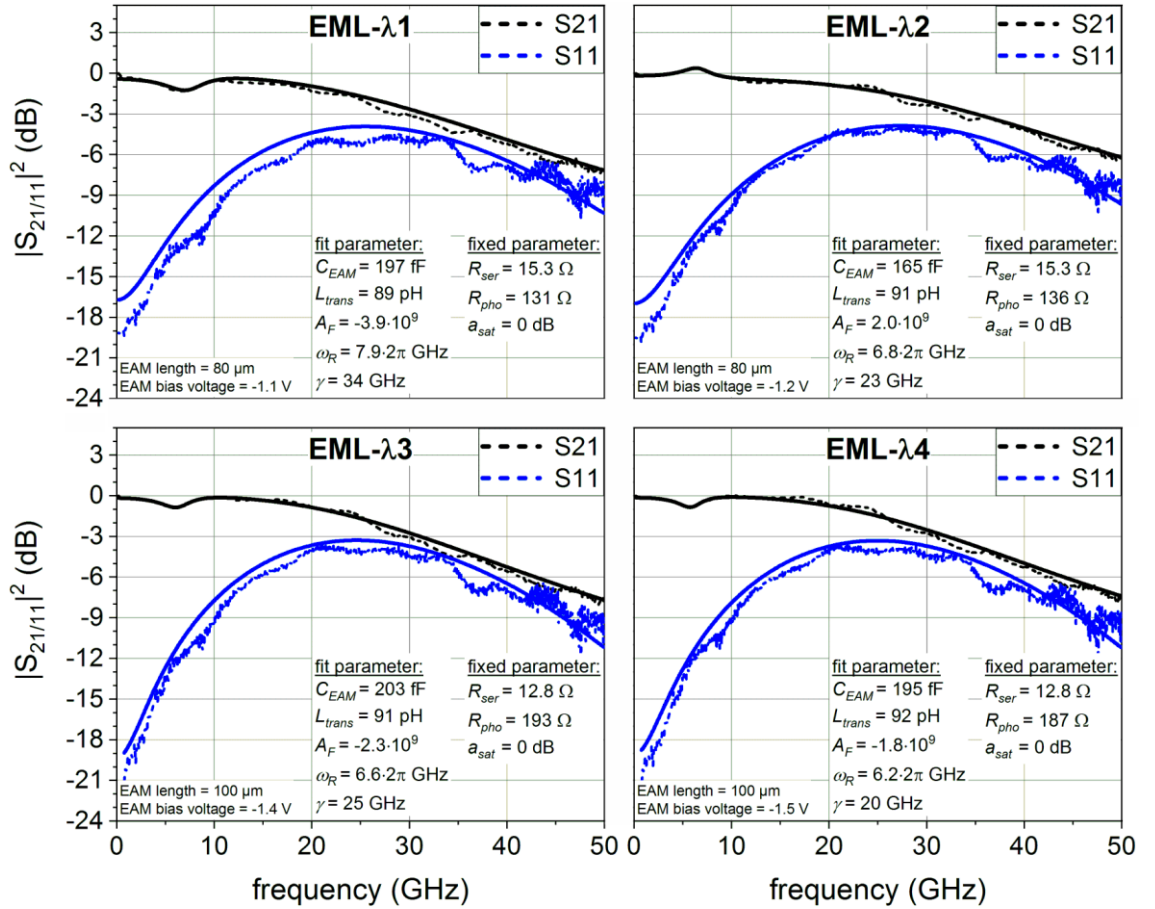


Figure 35: Measured (dashed lines) and fitted (solid lines) frequency response (black lines) and electrical reflection coefficient (blue lines) of the EML array. Functions (34) and (12) were used as fitting functions with shared fitting parameters. Additional fixed parameters are given in Table 5 of Appendix 1. $I_{DFB} = 100$ mA, $I_{SOA} = 0$ mA $T = 20$ °C.

The extracted EAM capacitance C_{EAM} and 3dB bandwidth for the fitted curves in Figure 35 are shown in Figure 36 (a). The higher operation point voltage and lower optical power (c.f. Figure 33) of the EMLs with longer wavelengths generally leads to a lower capacitance and

higher bandwidth (c.f. section 2.1.5). Due to the different EAM section lengths of 80 μm for EML- λ_1 and EML- λ_2 and 100 μm for EML- λ_3 and EML- λ_4 , the bandwidth of EML- λ_1 and EML- λ_2 is increased and thus an equal performance over the array is achieved. The capacitance ranges from 165 fF for EML- λ_2 to 203 fF for EML- λ_3 with a corresponding 3dB bandwidth of 35 GHz to 31 GHz, respectively. After fixing the electrical parameters based on the fitting results for 0 mA SOA current shown in Figure 35, the frequency response curves at higher SOA currents were fitted with variable optical parameters. The corresponding results for the saturation factor a_{sat} are shown in Figure 36 (b). Similar to the results for the high power EML (c.f. Figure 25 (a)), the SOA saturation increases with SOA current. EML- λ_1 and EML- λ_2 show a stronger saturation than EML- λ_3 and EML- λ_4 , which can be attributed to the lower EAM absorption and the higher SOA amplification, due to the shorter EAM section and shorter wavelength detuning, respectively. EML- λ_2 exhibits a particularly strong saturation, although this result is physically inconclusive and believed to be caused by the mentioned limits of the fitting function in the high optical feedback and high saturation regime.

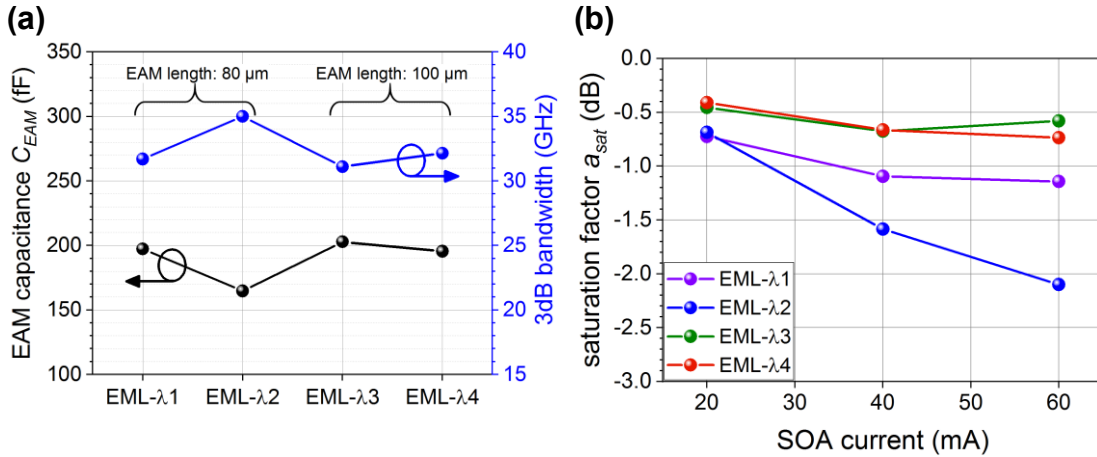


Figure 36: EAM capacitance and 3 dB bandwidth (a) of fitting function shown in Figure 35. Saturation factor (b) extracted via fitting. Function (34) was used as fitting function. Additional fixed parameters are given in Table 5 of Appendix 1. $I_{\text{DFB}} = 100 \text{ mA}$, $T = 50 \text{ }^\circ\text{C}$.

Large Signal - 56 GBd NRZ and 28 GBd PAM4

In this section, the EML arrays capability for 56 GBd NRZ and 28 GBd PAM4 transmissions will be investigated and the results of the two modulation formats compared. Both modulation formats yield the same data rate of 56 Gbit/s, which results in an aggregated data rate of 224 Gbit/s for the full array. The same measurement setup as shown in Figure 26 was used, with the electrical filter removed. For the generation of the PAM4 signal, two 28 GBd NRZ outputs of the PRBS source were combined with a passive electrical power combiner.

A -6dB attenuator was inserted at one of the outputs to achieve four equidistant power levels. To keep the complexity for the signal generation as comparable as possible for the two modulation formats, no other additional electronics such as digital-analog converter or otherwise was used. The corresponding electrical eyes for the two modulation formats are shown in Figure 37.

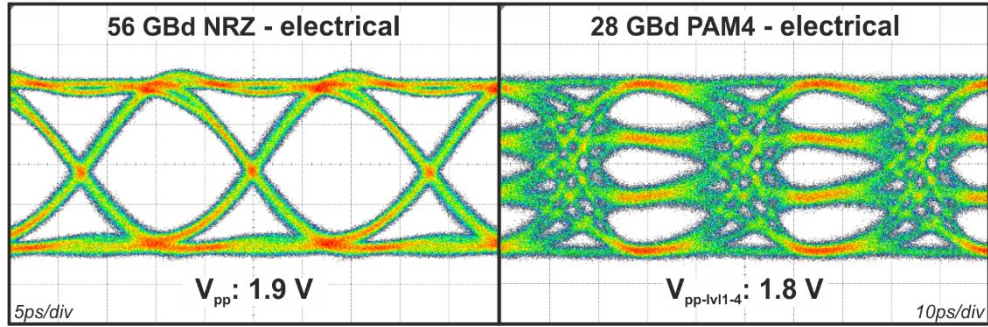


Figure 37: Electrical eye diagrams for 56 GBd NRZ (left) and 28 GBd PAM4 (right). For the generation of the 28 GBd PAM4 signal, two 28 GBd NRZ signals are combined with a passive electrical power combiner and a -6 dB attenuator.

For the following experiments, a constant DFB current of 100 mA was chosen for all EMLs in the array and the SOA currents were adjusted to give an equal output power around 8 dBm for all four EMLs (c.f. Figure 38). This moderately high power level was chosen to keep the influence of optical feedback sufficiently low. Higher mean output powers up to 10 dBm and higher (c.f. Figure 38) should be feasible for future device generations by using the new facet design with reduced optical feedback that was presented in section 2.2.1. It should be noted that the power levels of the EML array shown in Figure 38 cannot be compared directly to the power levels of the high power EML shown in Figure 27 as they operate at different temperatures of 20 °C and 50 °C, respectively.

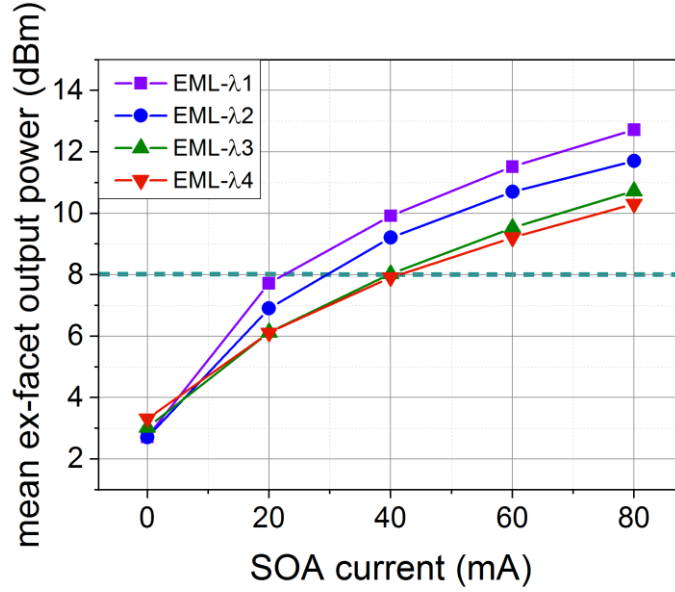


Figure 38: Mean ex-facet output power for high-speed modulation of the EML array. The dashed line indicates the power level chosen for further large signal measurements. 50 GBd NRZ, PRBS $2^{31}-1$, $I_{DFB} = 100$ mA, $V_{EAM-\lambda1} = -1.2$ V, $V_{EAM-\lambda2/\lambda3} = -1.3$ V, $V_{EAM-\lambda4} = -1.4$ V, $V_{pp} = 2$ V, $T = 20$ °C.

Figure 39 shows the measured optical eyes for each EML of the EML array operated separately with a 56 GBd NRZ (a) and 28 GBd PAM4 (b) signal. To verify that the EML array does not exhibit electrical crosstalk, neighboring EMLs were operated simultaneously with a decorrelated signal, which showed no effect on eye quality. The EAM bias was set to values close to the operation point bias voltage to achieve symmetric eye openings. For the 56 GBd NRZ operation, a homogenous performance over the full EML array is achieved (c.f. Figure 39 (a)). All four EML exhibit a clear eye-opening with a mean ex-facet output power around 8 dBm and a dynamic extinction ratio exceeding 7 dB. For the 28 GBd PAM4 operation, the array also shows good uniformity, although EML-λ3 exhibits slightly more noise than the other EMLs (c.f. Figure 39 (b)). The different power levels of all EMLs are nearly equidistant, with the outer levels being a bit closer together due to the typical nonlinearity of EMLs.

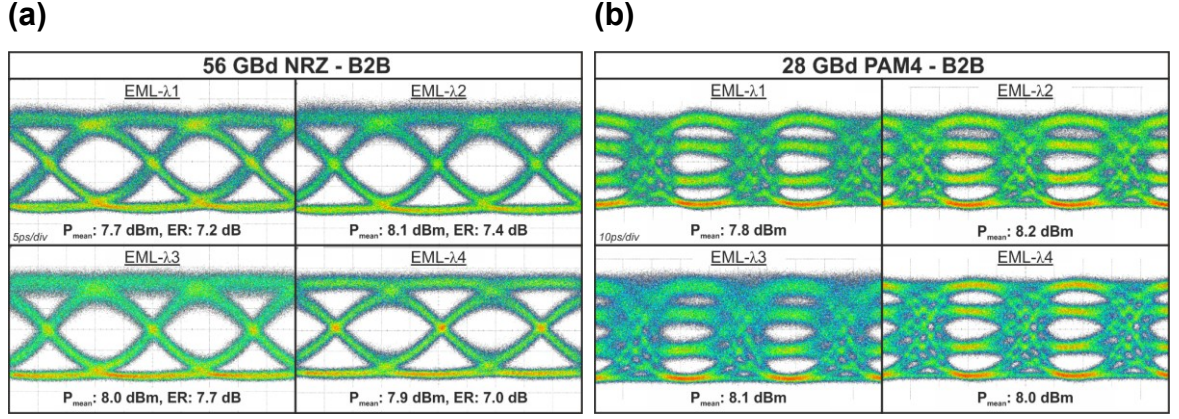


Figure 39: 56 GBd NRZ (a) and 28 GBd PAM4 (b) back-to-back optical eye diagrams for each EML in the EML array. $I_{\text{DFB}} = 100$ mA, $I_{\text{SOA-}\lambda_1} = 20$ mA, $I_{\text{SOA-}\lambda_2} = 30$ mA, $I_{\text{SOA-}\lambda_3/\lambda_4} = 40$ mA, $T = 20$ °C, (a): PRBS 23¹-1, $V_{pp} = 1.9$ V, $V_{\text{EAM-}\lambda_1} = -1.2$ V, $V_{\text{EAM-}\lambda_2/\lambda_3} = -1.3$ V, $V_{\text{EAM-}\lambda_4} = -1.4$ V, (b): PRBS 15¹-1, $V_{pp} = 1.8$ V, $V_{\text{EAM-}\lambda_1/\lambda_2/\lambda_3} = -1.3$ V, $V_{\text{EAM-}\lambda_4} = -1.4$ V.

Furthermore, the fiber transmission performance for the two modulation formats was tested (c.f. Figure 40 and Figure 41). Different lengths of single-mode fiber were inserted before the EDFA in Figure 26 and the sampling scope was replaced with a real-time oscilloscope (DSA-Z634A) for bit error rate (BER) analysis. The BER analysis was carried out with offline digital post-processing including clock recovery, 31-tap finite impulse response (FIR) equalizer, and bit error counting. The BER without applying the FIR equalizer is shown for reference. For each BER analysis, about $1.45 \cdot 10^6$ symbols were measured, resulting in a minimum BER limit of $6.9 \cdot 10^{-7}$. For the 56 GBd NRZ modulation, the array shows a nearly identical BER for all four channels (c.f. Figure 40). The 7% forward error correction (FEC) threshold is reached at about 1.5 km without equalizer and at around 2.5 km with equalizer. For comparison, a distance about twice as long (~ 5 km) is reached for the equalized 28 GBd PAM4 signal (c.f. Figure 41). This demonstrates an advantage of the PAM4 modulation format. Because the baud rate is only half of the data rate, the signal degradation through fiber dispersion is reduced compared to the NRZ modulation format. As already indicated in the back-to-back measurement (Figure 39 (b)), EML- λ_3 exhibits an increased BER compared to the other EMLs (Figure 41). With equalization, this difference is reduced and overall a uniform performance over the four EMLs is achieved. In conclusion, the PAM4 modulation format can significantly increase transmission distance and thus could be a preferred alternative to the NRZ format, especially in dispersion sensitive regimes such as the L-band. A drawback of PAM4 is that it requires two NRZ signals that need to be combined. By using a passive electrical combiner scheme, as demonstrated here, this added complexity can be kept to a minimum.

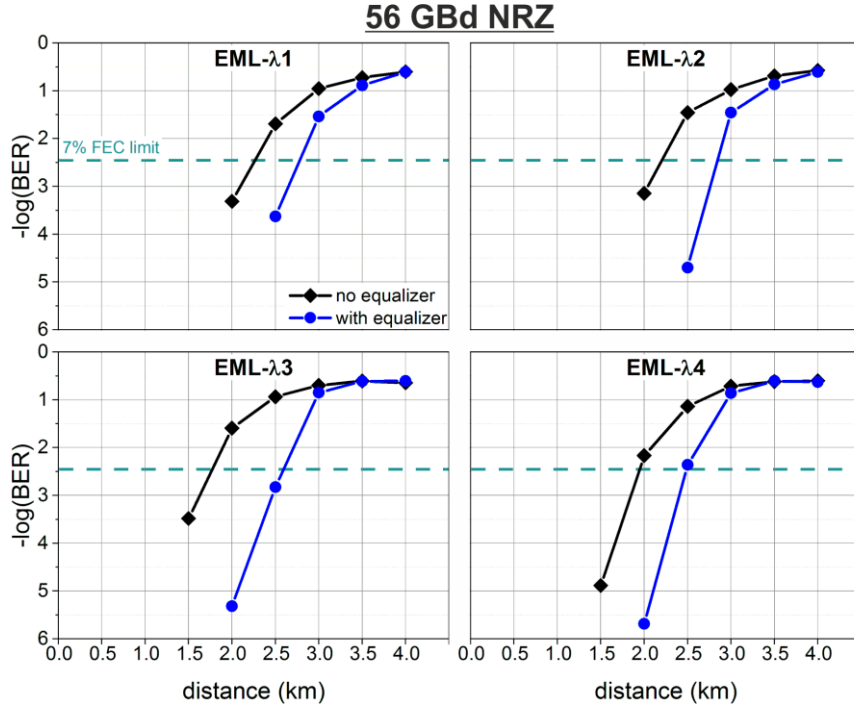


Figure 40: Bit error ratio vs. transmission distance for each EML in the EML array modulated with 56 GBd NRZ. A dashed line indicates the 7% FEC threshold. PRBS $2^{15}-1$, $I_{DFB} = 100$ mA, $I_{SOA-\lambda1} = 20$ mA, $I_{SOA-\lambda2} = 30$ mA, $I_{SOA-\lambda3/\lambda4} = 40$ mA, $V_{pp} = 1.9$ V, $V_{EAM-\lambda1} = -1.2$ V, $V_{EAM-\lambda2/\lambda3} = -1.3$ V, $V_{EAM-\lambda4} = -1.4$ V, equalizer: 31-tap FIR, $T = 20$ °C.

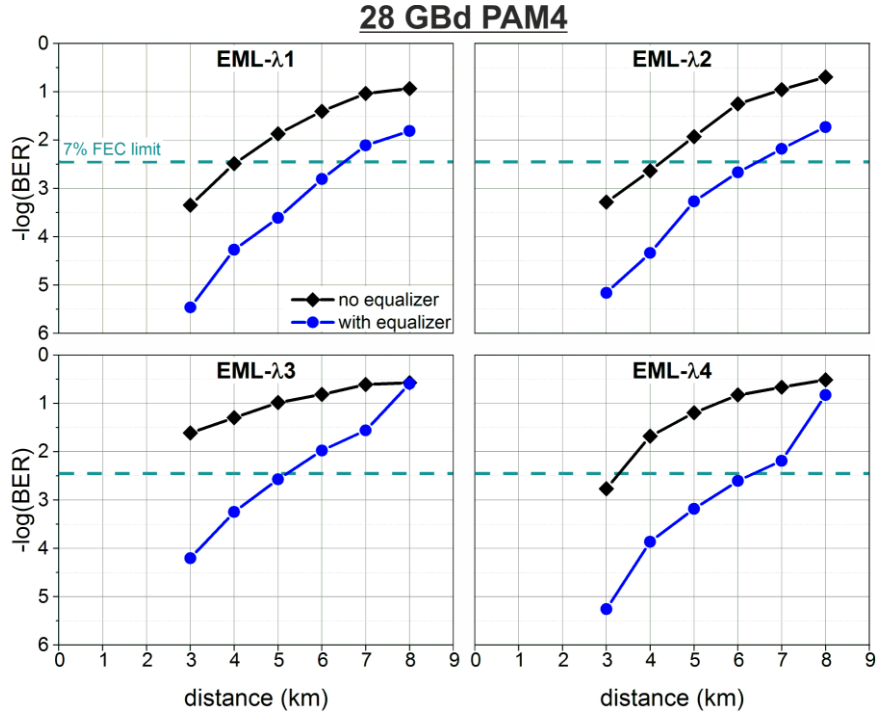


Figure 41: Bit error ratio vs. transmission distance for each EML in the EML array modulated with 28 GBd PAM4. A dashed line indicates the 7% FEC threshold. PRBS $2^{15}-1$, $I_{DFB} = 100$ mA, $I_{SOA-\lambda1} = 20$ mA, $I_{SOA-\lambda2} = 30$ mA, $I_{SOA-\lambda3/\lambda4} = 40$ mA, $V_{pp} = 1.8$ V, $V_{EAM-\lambda1/\lambda2/\lambda3} = -1.3$ V, $V_{EAM-\lambda4} = -1.4$ V, equalizer: 31-tap FIR, $T = 20$ °C.

In conclusion, the concept of integrating SOAs and varying the EAM length has proven to be an effective method for achieving equal performance for EML arrays with wavelength channels that span over 7.5 nm. In section 4, this concept will be taken one step further by applying it to an EML array with wavelength channels that span over 13.6 nm.

3. Hybridly Integrated Lasers

3.1 Fundamentals

3.1.1 III-V Integration to Silicon-Based Photonic Platforms

To date, there are multiple methods for integration of III-V material to silicon-based photonic platforms. In this section, a brief overview of the four most established methods is given with an outline of their general pros and cons (c.f. Table 1). After this section, the focus will lie on the flip-chip method that is used for this work.

Table 1: Overview of the pros and cons of different hybrid integration methods.

Method	Scalability	Simplicity	Device Performance
Heterogeneous Integration	++	-	-
Edge Coupling	--	+	++
Micro-Optical Packaging	-	-	++
Flip-Chip Integration	+	+	+

Heterogeneous Integration

Heterogeneous integration in photonics typically refers to the integration of III-V material to a silicon photonics wafer with subsequent processing of the wafer. This is a contrast to hybrid integration, where fully processed III-V and silicon-based photonic chips are integrated. The heterogeneous integration starts with the bonding of III-V wafer pieces or full wafers onto a silicon-based wafer (c.f. Figure 42). The bond is typically realized via covalent direct bonding or with a thin adhesive layer such as BCB [54]–[56]. After bonding, the silicon wafer is processed together with the III-V material in a CMOS fab and afterwards diced into individual hybrid chips. The biggest advantage of this method is its scalability. Since all wafer processing steps are carried out on a silicon wafer, it allows taking full advantage of the large scale processing capabilities of modern CMOS foundries. It is also the method that is most relaxed regarding optical alignment as this is done on a lithographic level during processing. The coupling of light from the III-V material to the silicon layers is usually done via evanescent coupling. The main challenges of the heterogeneous integration method are to achieve a strong bond with good thermal properties between the III-V and silicon material, and to find good compromises for processing that accommodate both material systems.

These challenges typically result in a disadvantage regarding overall device performance, when compared to separately processed chips.

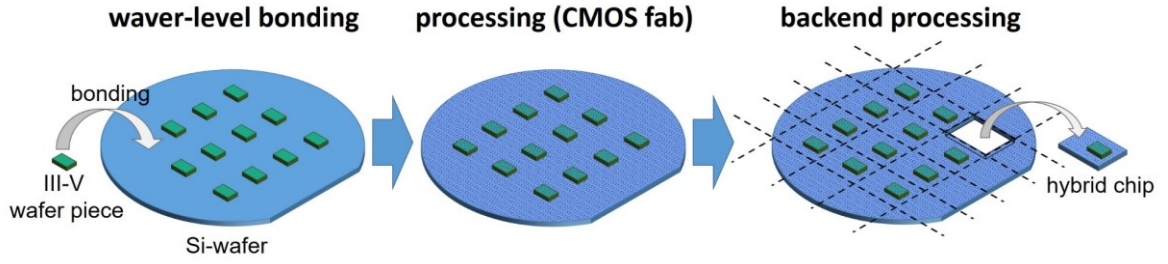


Figure 42: Schematic illustration of heterogeneous integration. The III-V material is bonded on a wafer-level with subsequent processing of the wafer.

Edge Coupling

In this work, the hybrid integration method of edge coupling refers to the assembly of fully processed III-V and silicon-based chips in an edge-to-edge fashion as depicted in Figure 43. This assembly method requires that the optical waveguides lead to the chip edges. The waveguide facets are aligned for the coupling of light from one chip to the other via butt-coupling. The alignment is carried out with one of the chips placed on a multi-axis positioning stage with ideally all six degrees of freedom. Typically, the axes are aligned by using the III-V chip either as a light source or as a photodetector to get a feedback signal for an active alignment loop. After alignment, the chip edges are glued together, with the glue also acting as index matching material. For stability, the hybrid chip is then mounted on a common carrier. As no compromises regarding wafer processing have to be made, this method can yield an overall excellent device performance [57], [58]. In addition, the side-by-side placement of the chips allows for a good thermal connection to the heatsink for both chips. The biggest drawback of this method is its low scalability. Each chip has to be handled individually right until the end, so there is only minimal time and cost reduction with larger numbers. Another disadvantage is that the III-V components can only be placed at the edges of the silicon-based chip, which can be a critical issue for larger PICs with a complex waveguide routing structure.

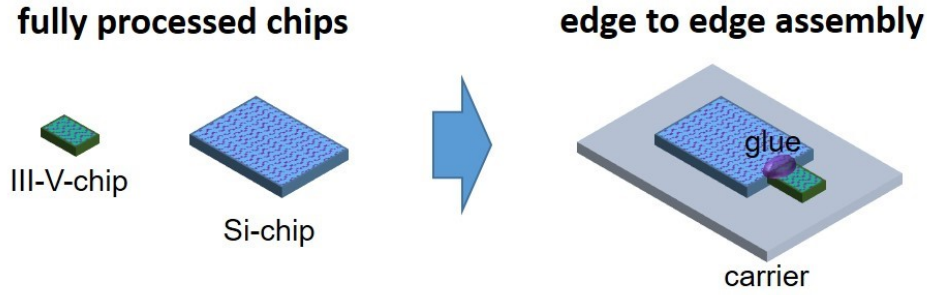


Figure 43: Schematic illustration of hybrid integration via edge coupling of fully processed III-V and Si-chips.

Micro-Optical Packaging

The utilization of micro-optical packaging is one of the most sophisticated methods for hybrid integration [59], [60]. It is also one of the first to be commercially successful on a larger scale [61]. For this hybrid integration method, the III-V chip is mounted on a micro-optical bench that comprises multiple optical components such as lenses and prisms (c.f. Figure 44 (left)). The optical components focus the light and guide it from the III-V chip towards the bottom of the micro-optical bench where it couples to the silicon-based wafer e.g. via grating couplers. Placing a cap on the micro-optical bench allows for hermetic sealing. These sealed micro-packages are then assembled on wafer-level to fully processed silicon-based wafers that are diced after assembly to individual hybrid chips. Since the III-V to silicon assembly and most of the backend processing is done on a wafer-level, it allows for improved scalability compared to the edge coupling approach. It can yield very good device performance as no compromises during wafer processing have to be made. Of the methods shown here, it is the only one that allows the integration of an optical isolator, which significantly relaxes the issue of optical feedback. The bottleneck of this approach is the complexity of the micro-optical package. It requires the individual assembly of multiple components which limits scalability and drives packaging costs.

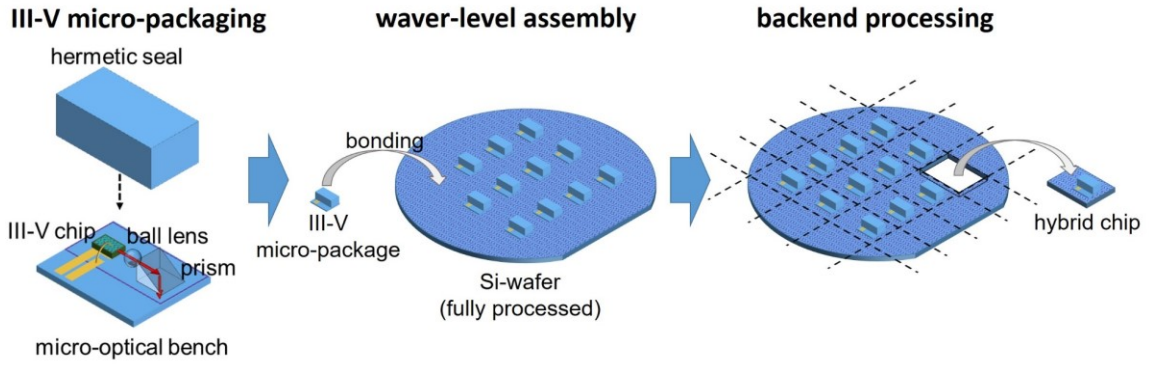


Figure 44: Schematic illustration of hybrid integration via micro-optical packaging. The III-V chips are mounted in micro-optical packages that are bonded on wafer-level onto a silicon-based wafer.

Flip-Chip Integration

In this work, the hybrid integration method of flip-chip integration refers to the integration of III-V chips, with the chips' top surface facing downwards, into etched recesses on fully processed silicon-based wafers or wafer pieces as depicted in Figure 45. The etched recesses comprise bonding pads for the electrical and mechanical connection between the III-V chip and the silicon-based wafer. Light is coupled from one chip to the other via butt-coupling. Mechanical alignment stops on both chips allow for passive vertical alignment [62], [63]. With an advanced solder reflow process, full passive alignment via alignment stops can be realized [64]. The advantage of the flip-chip integration method is that it combines good scalability, with a simple assembly process and good overall device performance. The scalability is high because assembly can be performed on the wafer-level without the need for micro-packaging. The assembly process is simple because it requires only two components and passive alignment is used. Good overall device performance can be achieved because no compromise regarding the III-V and silicon wafer processing has to be made. The most critical aspect of the flip-chip integration method is its assembly process. Although the principle of the assembly process is simple, it requires achieving simultaneously an electrical, mechanical, and optical connection between the III-V and silicon chip. With the typically very tight optical alignment tolerances, a sophisticated assembly process is necessary to yield good and reproducible results. The hybridly integrated devices demonstrated in this work were assembled using the flip-chip integration method. Details regarding the used assembly method and the integration interface design are given in sections 3.2 and 3.3.

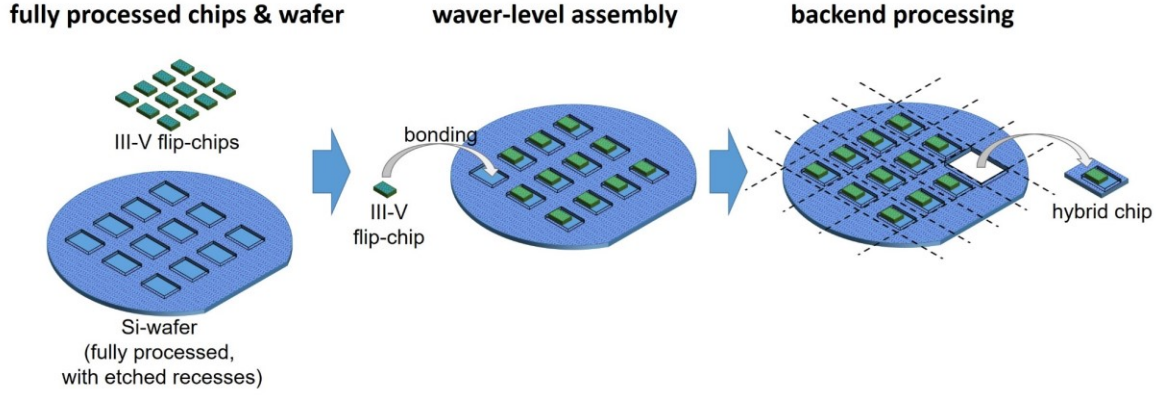


Figure 45: Schematic illustration of hybrid integration via the flip-chip integration method. The III-V chips are flip-chip integrated on wafer-level into etched recesses on a fully processed silicon-based wafer.

3.1.2 Optical Chip-to-Chip Coupling

In this section, the theoretical background for optical chip-to-chip coupling via butt-coupling is described. Analytical expressions for calculating the chip-to-chip coupling efficiency and the alignment tolerances are given for Gaussian modes. Optical modes of semiconductor waveguides are typically not exact Gaussian shape but Gaussian approximation has proven very effective for most practical applications.

Coupling Efficiency and Alignment Tolerance

The two key parameters for chip-to-chip coupling are the coupling efficiency and the alignment tolerance. The higher the coupling efficiency, the more light couples from one chip to the other, and the higher the alignment tolerance, the easier it is to align the chips to optimum coupling efficiency. To realize a high coupling efficiency, the optical mode sizes of the chips need to be matched. Joyce and DeLoach have shown that for Gaussian modes the coupling efficiency relates to the mode sizes with [65]

$$\eta_a = \tau_x \tau_y, \quad \tau_{x,y} = \frac{2}{\sqrt{\left(\frac{\tilde{\omega}_{x,y}}{\omega_{x,y}} + \frac{\omega_{x,y}}{\tilde{\omega}_{x,y}}\right)^2 + \left(\frac{\lambda d_z}{\pi \tilde{\omega}_{x,y} \omega_{x,y}}\right)^2}} \quad (37)$$

where η_a is the power coupling efficiency of the two aligned modes, $\tau_{x,y}$ is the coupling efficiency within one plane, $\tilde{\omega}_{x,y}$ and $\omega_{x,y}$ are the beam waists of the two optical modes, λ is the wavelength and d_z is the distance of the modes in the z-direction. The subscripts x and

y correspond to the x - z and the y - z plane, respectively. The used definition of the coordinate system and the Gaussian beam waist are shown in Figure 46.

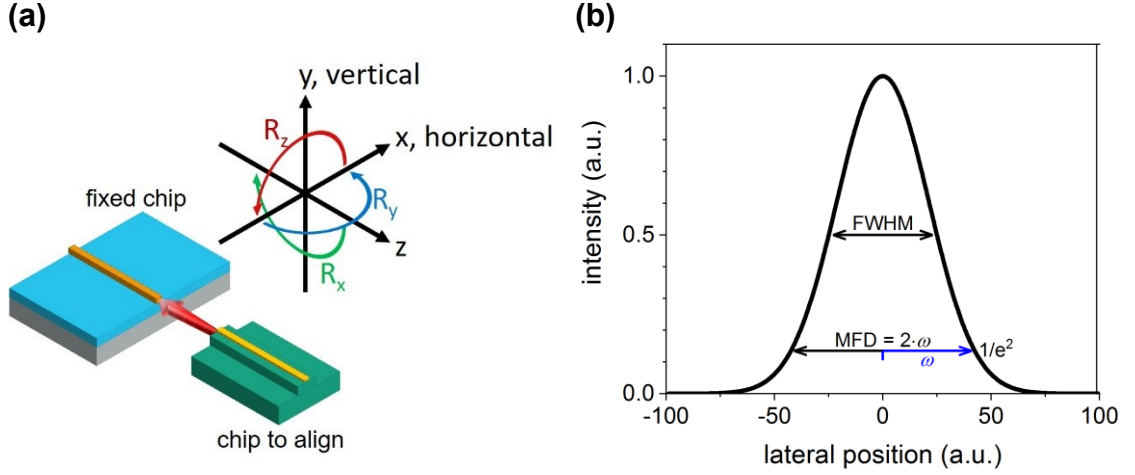


Figure 46: Coordinate system (a) used within this work. The movable chip is aligned via translation and rotation along the shown axes. Definition of full width half maximum (FWHM), mode field diameter (MFD), and beam waist ω for a Gaussian mode intensity profile (b).

Based on equation (37), the maximum coupling efficiency is achieved if the mode sizes ω are equal, and the coupling efficiency reduces with the distance d_z . The dependence on d_z is larger for smaller mode sizes and longer wavelengths, which can be explained by the correspondingly larger beam divergence. As the light propagates from one chip to the other, the beam divergence leads to a widening of the mode and an increased curvature of the phase fronts, which reduces coupling efficiency. To include misalignment in the x and y direction, equation (37) is extended to [65]

$$\eta = \tau_x \tau_y e^{-\frac{d_x^2}{a_x^2}} e^{-\frac{d_y^2}{a_y^2}},$$

$$a_{x,y} = \frac{\sqrt{2}}{\sqrt{\tau_{x,y}^2 \left(\frac{1}{\tilde{\omega}_{x,y}^2} + \frac{1}{\omega_{x,y}^2} \right)}}, \quad (38)$$

where η is the power coupling efficiency and d_x and d_y are the misalignment in x and y direction, respectively. The constant $a_{x,y}$ describes the lateral misalignment at which the coupling efficiency is reduced to e^{-1} and thus gives a measure of the alignment tolerance. From equation (38) one can see that alignment tolerance is increased with larger mode sizes ω and with a reduced coupling efficiency $\tau_{x,y}$.

Alignment for Tilted Waveguides

To reduce unwanted optical feedback from the chip-to-chip interface, it is common to introduce tilted waveguides at the chip facets (c.f. Figure 47).

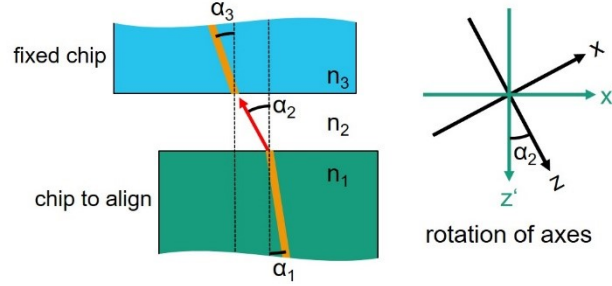


Figure 47: Chip-to-chip coupling for waveguides that are tilted in the x - z plane. Orange lines and a red arrow indicate the direction of the optical waveguides and the optical beam, respectively, n_1 and n_3 correspond to the effective indices of the chips waveguides. n_2 is the refractive index of the material in between the chips. On the right, the axes related to the alignment stage (z' , x') are rotated to the axes related to the optical beam emission (z , x).

If the correct relation between the waveguide angles is chosen and the tilt of the beam emission between the chips is considered, the same coupling efficiency as for straight waveguides can be achieved. For a given waveguide tilt angle α_1 , the corresponding tilt angles for α_2 and α_3 can be derived with Snell's law

$$\begin{aligned} n_1 \sin \alpha_1 &= n_2 \sin \alpha_2 = n_3 \sin \alpha_3 , \\ \alpha_2 &= \sin^{-1} \left(\frac{n_1}{n_2} \sin \alpha_1 \right) , \\ \alpha_3 &= \sin^{-1} \left(\frac{n_1}{n_3} \sin \alpha_1 \right) , \end{aligned} \tag{39}$$

where α_1 , α_3 and n_1 , n_3 correspond to the tilt angles and effective indices of the two waveguides, respectively. α_2 and n_2 correspond to the beam emission angle and the refractive index of the material between the chips, respectively. To achieve the highest coupling efficiency, the relation between the waveguide tilt angles α_1 and α_3 that are given in (39) should be used for chip design. The angle of the beam emission α_2 is not relevant for chip design, but has to be considered during the alignment process. Typically the axes of the alignment stage (c.f. Figure 47 (x' , z')) are oriented with the z' -axis parallel to the normal of the chip facets. For the expression of the coupling efficiency (38), the coordinate system is orientated with the z -axis parallel to the beam emission (c.f. Figure 47 (x , z)). Rotation of the axes by the angle of the beam emission α_2 allows to use (38) with the new coordinates

$$\begin{aligned} x &= x' \cos \alpha_2 + z' \sin \alpha_2, \\ z &= z' \cos \alpha_2 - x' \sin \alpha_2. \end{aligned} \tag{40}$$

The beam emission angle α_2 also has to be considered, when the chips are assembled with a distance $d_{z'}$ between the chip edges and index matching material is applied. By applying index matching material, the refractive index n_2 between the chip changes and thus α_2 changes (c.f. (39)). This has the consequence that the chip position with the highest coupling efficiency changes depending on the refractive index of the material between the chips. This is relevant for assembly processes where the optical alignment step has to be carried out in air, and in a later step, index-matching material is applied. The corresponding positioning error can be accounted for, by applying a deliberate misalignment in the x' -direction during the alignment step. For a refractive index \tilde{n}_2 of the index matching material, the new beam emission angle $\tilde{\alpha}_2$ is calculated with (39) and the required misalignment in air that is needed to achieve optimum alignment for index matching material is calculated with

$$d_{x'} = d_{z'}(\tan \alpha_2 - \tan \tilde{\alpha}_2). \tag{41}$$

3.2 Design and Simulation

This section describes the design of the devices used for the flip-chip hybrid integration process developed within this work. To date, similar processes have been developed by other scientific groups for the hybrid-flip chip integration of III-V chips to SOI- or SiO₂-platforms [62], [63], [66]–[69]. The process developed in this work is the first to be used for the flip-chip hybrid integration of III-V chips to the SiN based photonic platform TriPleX.

3.2.1 III-V Lasers and Gain Chips

Device Structure

The III-V based DFB lasers and gain chips have the same fundamental layout (c.f. Figure 48). Each chip has reference surfaces at each side that are used as vertical alignment stops in the hybrid assembly. The surface of the alignment stops are etched with a selective etch process to guarantee an exact height relative to the optical waveguide. The visual alignment marks at the front facet are defined with the same mask as the buried optical waveguide to

allow precise visual alignment relative to the optical mode. The visual alignment marks have the same tilt as the optical waveguide to maintain the same relative position independent of the cleaving accuracy. The optical waveguide has a buried heterostructure (BH) with p-n current-blocking layers and InGaAsP MQW active layers. The waveguide towards the front facet acts as an SOA and simultaneously as a spot-size converter (SSC). For the DFB laser chip variants, the straight waveguide at the back has a complex coupled grating. For the gain chip variants, the waveguide is without grating. The chip design allows for the cleaving of single chips and array chips. The front facet is anti-reflection (AR) coated to minimize residual reflection. The back facet is either high-reflection coated in the case of gain chips and single DFB chips or anti-reflection coated for DFB arrays. The latter allows for a high single-mode yield, which is critical for array chips. Chips were fabricated with either AuSn (80%/20%) as the top layer, as shown in Figure 48, or with a pure gold top layer.

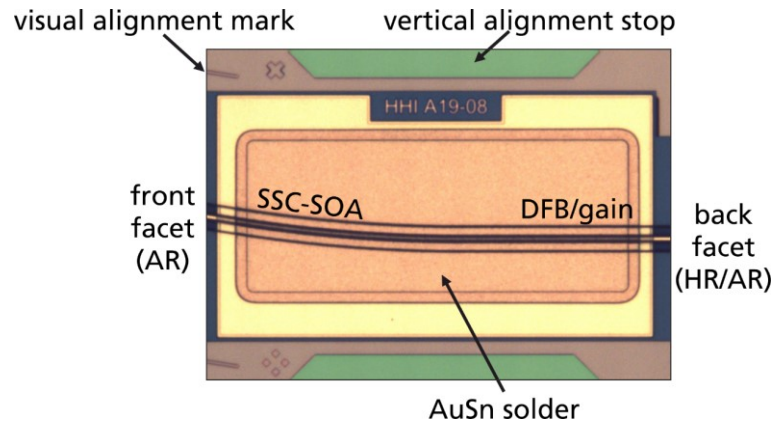


Figure 48: Top view of fabricated III-V chip for flip-chip hybrid integration. Reference surfaces that are used as vertical alignment stops are highlighted in green. The front facet is anti-reflection coated (AR). The back facet is high-reflection coated (HR) in the case of gain chips and single DFB, or AR coated in the case of DFB arrays. Chip dimensions are 700 μm x 500 μm .

Spot-Size Converter

A linear inverse taper design was chosen for the III-V based SSC. For inverse tapered SSCs, the two most critical parameters are the waveguide dimensions at the tip of the SSC and the length of the SSC. The waveguide dimensions at the tip define the size of the optical mode, and the length of the SSC has to be long enough to assure adiabatic mode size conversion for low propagation losses. The design target of the SSC was to achieve highest coupling efficiency to a Gaussian mode with 3.5 μm MFD. For the DFB lasers and gain chips, HHI-standard epitaxial designs are chosen, which define a fixed waveguide height. The optimum waveguide width is evaluated by calculating the coupling efficiency to a Gaussian mode with the simulation tool RSoft (c.f. Figure 49 (a)). Both device types show about -0.3 dB as the

highest coupling efficiency. Due to the different epitaxial designs, the DFB laser and gain chip exhibit their highest coupling efficiency at different SSC tip widths. The DFB lasers waveguide is slightly stronger guiding, which is why a smaller width is required. To keep the fabrication process simple, a compromise with an SSC tip width of $0.6\ \mu\text{m}$ was chosen for the design of both device types. The estimated coupling efficiency to a Gaussian mode with $3.5\ \mu\text{m}$ MFD is then around $-0.4\ \text{dB}$ for both device types. Figure 49 (b) shows the efficiency of how much of the light that has propagated through the SSC couples to the optical mode at the SSC tip. If the SSC is too short, the light will not be able to fully transform to the optical mode at the SSC tip, which indicates that the light is not tapered adiabatically. Figure 49 (b) shows that for lengths smaller than $100\ \mu\text{m}$, the SSC becomes significantly non-adiabatic. To guarantee adiabatic tapering, a minimum design length of $200\ \mu\text{m}$ is chosen for all DFB laser and gain chip designs.

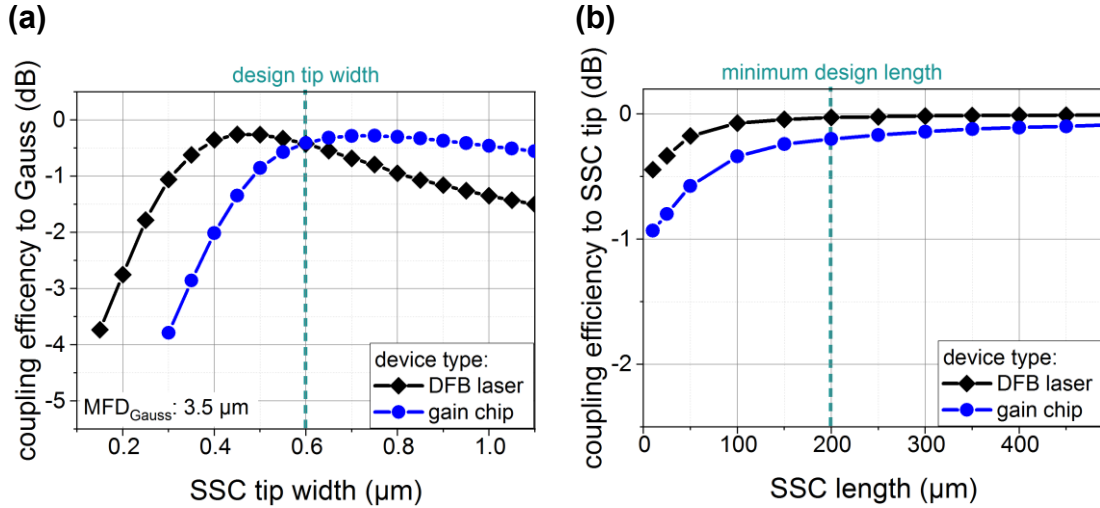


Figure 49: Calculated coupling efficiency of SSC tip mode to a Gaussian mode (a) and coupling efficiency of light that has propagated through the SSC to the SSC tip mode (b). Simulated with RSoft.

For the chosen SSC tip width of $0.6\ \mu\text{m}$, the alignment tolerance is evaluated (Figure 50). The simulation results show in both lateral directions a -1dB alignment tolerance of about $1.6\ \mu\text{m}$ and $1.8\ \mu\text{m}$ for the DFB laser and the gain chip design, respectively. The calculated alignment tolerances comply with the placement accuracy of state of the art high precision die bonders, which specify absolute placement accuracies of smaller than $\pm 0.5\ \mu\text{m}$ [70], [71]. The gain chips exhibit a slightly larger tolerance, due to their larger mode size. The simulated mode fields were near-circular with mode field diameters of $2.5\ \mu\text{m}$ and $3.9\ \mu\text{m}$ for the DFB laser and the gain chip, respectively.

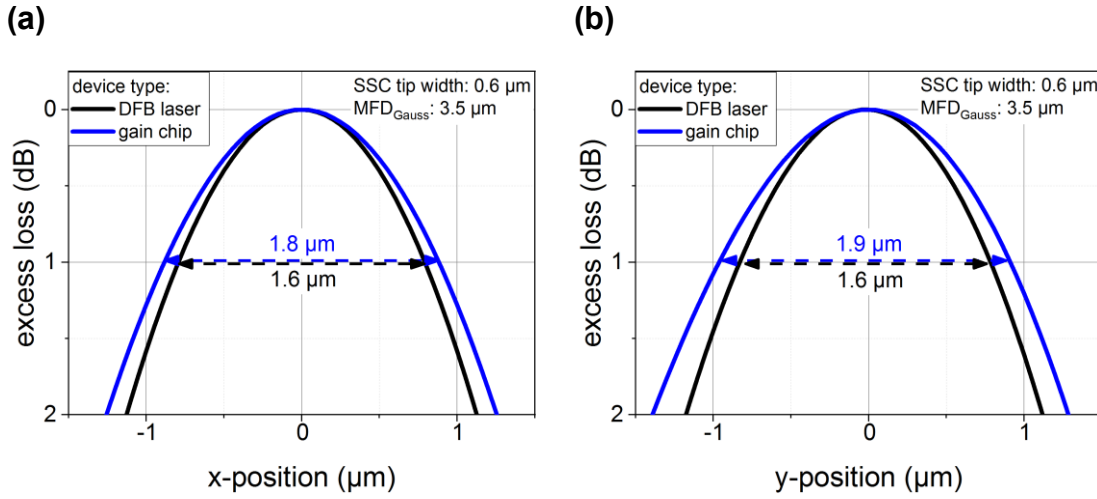


Figure 50: Calculated excess loss for lateral misalignment in the x-direction (a) and the y-direction (b) for coupling between the SSC tip mode and a Gaussian mode with MFD: 3.5 μm. Simulated with RSoft.

3.2.2 SiN TriPleX

Flip-Chip Integration Evaluation Chip

Special SiN TriPleX evaluation chips were fabricated for the development of the flip-chip hybrid integration process. They comprise a row of etched recesses for the flip-chip integration of multiple III-V chips and arrays (c.f. Figure 51). The output light of the III-V chips is coupled to individual SiN waveguides that have SSCs matched to a Gaussian mode with 3.5 μm MFD. The SiN waveguides lead to the SiN chip edge with SSCs that are matched to cleaved standard single-mode fiber. The etched recesses are etched down to the Si-substrate to provide space for the III-V chip and to give a direct thermal connection to the substrate (c.f. Figure 51 (right)). The complete etching through the SiO₂ layer is highly beneficial regarding thermal management because of the roughly a hundred times lower thermal conductivity of SiO₂ compared to the Si-substrate [72], [73]. SiO₂ pedestals with a defined height relative to the SiN waveguide are situated at the sides as mechanical alignment stops for passive alignment in the vertical direction (c.f. Figure 51 (right)). The III-V chips are bonded to gold bond pads on the SiN TriPleX chip with AuSn solder that is applied on the III-V chip or alternatively with a gold sinter paste [74] that is applied to the SiN TriPleX chip.

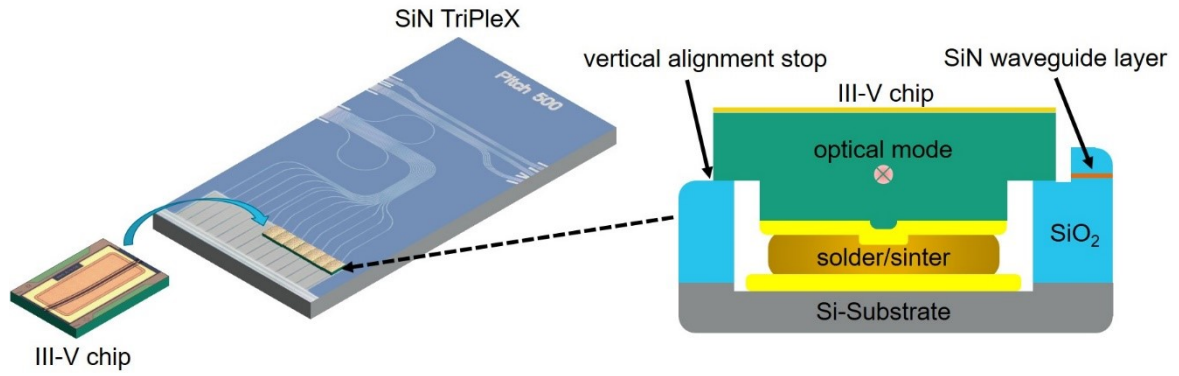


Figure 51: Flip-chip hybrid integration of III-V chips to a SiN TriPleX evaluation chip (left) and schematic cross-section, which is oriented perpendicular to the direction of the III-V optical waveguide (right).

Hybrid Tunable Laser

A practical application of the flip-chip hybrid integration process is demonstrated in this work by the assembly of a hybrid tunable laser. The laser consists of a SiN TriPleX external cavity with a flip-chip integrated III-V gain chip (c.f. Figure 52). The III-V gain chip is integrated into an etched recess that has the same cross-section as shown in Figure 51. The external cavity comprises two ring resonators (ring#1, #2) with slightly different circumferences to allow wavelength tuning via the Vernier effect. The individual rings are tuned via electronic heaters (c.f. Figure 52 (yellow in top)). The directional couplers (dc#5, #6) of ring#2 are designed with an identical coupling coefficient to achieve critical coupling with ideally no light passing towards output #1 and #2. The directional couplers (dc#3, #4) of ring#1 are designed with slightly different coupling coefficients to allow light to couple out of the laser cavity. The output light is combined on one of the two outputs (#3, #4) by adjusting the phase via electrical heaters at the arms of dc#1. The electrical heater at the arm of dc#7 is used to adjust the roundtrip phase inside the cavity.

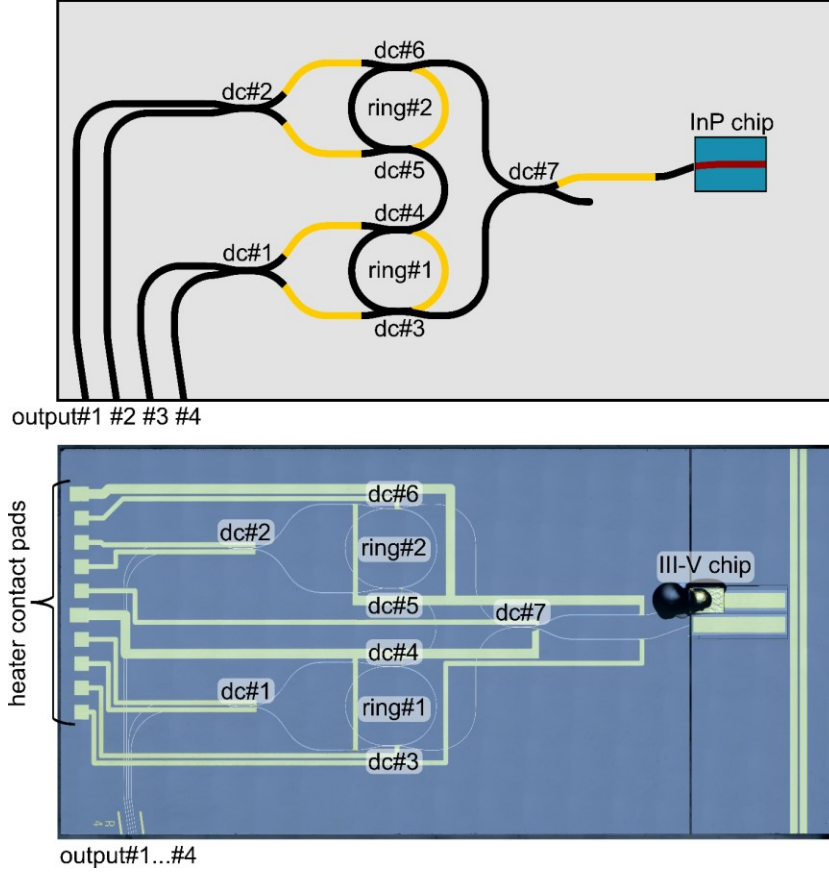


Figure 52: Schematic (top) and photograph with SiN waveguides highlighted in white (bottom) of hybrid tunable laser comprising a SiN TriPleX external cavity and a flip-chip integrated III-V gain chip with index matching glue applied. The external cavity comprises two ring resonators (ring#1, #2) that are connected via directional couplers (dc#1-#7) and optical waveguides. The yellow lines in the schematic (top) indicate electronic heaters that allow phase tuning of the rings (ring#1, #2) and the individual arms of the directional couplers (dc#1, #2, #7). Chip dimensions are 16 mm x 8 mm.

3.3 Experimental Characterization

This section describes the experimental characterization for the flip-chip hybrid integration of III-V DFB lasers and gain chips to SiN TriPleX. First, the optical far-field of the individual components is analyzed, to evaluate the quality of the optical mode matching. Next, three different assembly methods are investigated for the integration of III-V DFB lasers to SiN TriPleX evaluation chips. Finally, the assembly method with the most promising results is used for the assembly of a hybridly integrated tunable laser by integrating a III-V gain section to a SiN TriPleX external cavity. Parts of these results have been published in [75]–[77].

3.3.1 Optical Far Field

For an efficient coupling of light in hybrid integration, mode matching between the optical modes at the chip-to-chip interface is required. To achieve good mode matching with relaxed alignment tolerance, SSCs are integrated at the facets on the III-V and SiN TriPleX side (c.f. section 3.2). How good the optical modes of the SSCs are matched, can be evaluated by measuring the far-field emission and deriving an approximation for the size of the corresponding optical near-field (c.f. Figure 53). The MFDs of the optical near-field modes are derived from the far fields FWHM with a Gaussian approximation [78]

$$MFD = \frac{\lambda}{\pi \frac{\tan(FWHM/2)}{\sqrt{2 \ln(2)}}} \quad (42)$$

The MFDs derived from the optical far-fields show for all three device types near-circular mode profiles with the III-V devices showing slightly larger MFDs in the vertical than in the horizontal direction (c.f. Figure 53). The III-V DFB laser exhibits in both directions a smaller MFD than the gain chip, which can be explained by the stronger guiding of the epitaxial layer design compared to that of the gain chips as described in section 3.2.1.

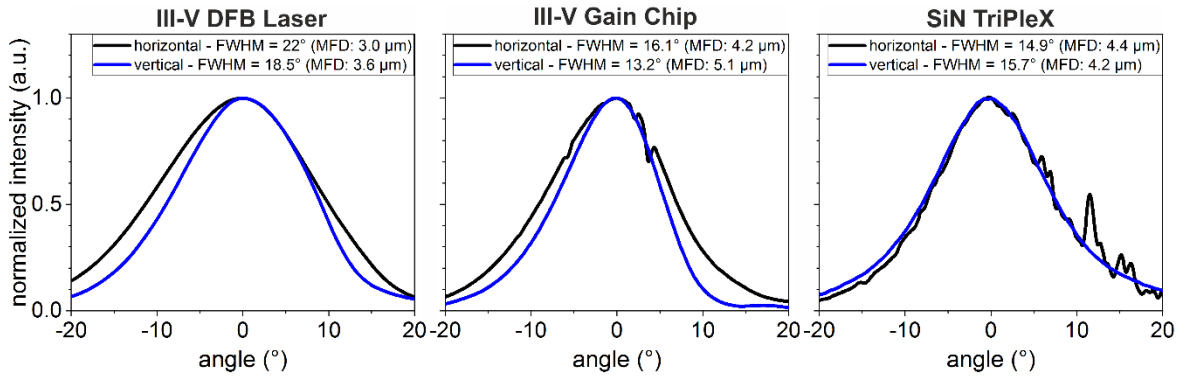


Figure 53: Measured optical far-field of III-V and SiN TriPleX spot-size converters. The FWHM far-field angle and the corresponding near-field MFD, derived with Gaussian approximation, is given in the legend. $I_{DFB} = 100 \text{ mA}$, $I_{\text{gain chip}} = 100 \text{ mA}$, $\lambda_{\text{SiN TriPleX}} = 1550 \text{ nm}$, $T = 20 \text{ °C}$.

Based on the MFD derived from the far-field measurement in Figure 53, Equation (38) is used to calculate the theoretical coupling efficiency and alignment tolerance for the chip-to-chip coupling. The results for coupling III-V devices to SiN TriPleX are shown in Table 2 for the ideal case of zero distance between the chips ($d_{z'} = 0 \text{ μm}$) and for the case with a safety distance ($d_{z'} = 6 \text{ μm}$). Corresponding to the assembly processes shown in section 3.3.2 and 3.3.3, the material between the chips is assumed to be air ($n_2 = 1$) for the

DFB laser and index matching glue ($n_2 = 1.5$) for the gain chip. The theoretical coupling efficiency between DFB laser and SiN TriPleX is -1.2 dB for a distance of 6 μm between the chips and increases up to -0.4 dB when the facets are put close together ($d_{z'} = 0 \mu\text{m}$). A higher coupling efficiency of -0.1 dB ($d_{z'} = 0 \mu\text{m}$) is achieved for the gain chip due to a better matching of the mode sizes (c.f. Figure 53). At 6 μm facet distance the coupling efficiency for the gain chip is -0.3 dB, which is a much lower reduction than for the DFB laser. This can be explained by the smaller beam divergence of the gain chip resulting from its larger mode size and the use of index matching glue. It should be noted that the values shown in Table 2 are theoretical values only with the assumption of ideal Gaussian modes. The real optical modes will not have an ideal Gaussian shape and thus the measured coupling efficiency is expected to be slightly lower. The -1 dB alignment tolerance ranges from 2 μm to 2.6 μm with larger tolerances for the gain chip and increased facet distance. The alignment tolerance is larger than expected from the simulation (c.f. Figure 50), which relates to the slightly larger mode sizes of the fabricated chips (c.f. Figure 53) compared to design.

Table 2: Theoretical coupling efficiency and -1dB alignment tolerance for coupling between III-V chips to SiN TriPleX. Equation (38) with MFDs derived from far-field measurement (c.f. Figure 53) is used. A refractive index of $n_2 = 1$ is assumed for the DFB laser and $n_2 = 1.5$ for the gain chip. $\lambda = 1550 \text{ nm}$.

Device Type	Coupling Efficiency ($d_{z'} = 0 \mu\text{m}$)	-1dB Alignment Tolerance ($d_{z'} = 0 \mu\text{m}$)	Coupling Efficiency ($d_{z'} = 6 \mu\text{m}$)	-1dB Alignment Tolerance ($d_{z'} = 6 \mu\text{m}$)
III-V DFB Laser	-0.4 dB	2.0 μm (horizontal) 2.1 μm (vertical)	-1.2 dB	2.3 μm (horizontal) 2.4 μm (vertical)
III-V Gain Chip	-0.1 dB	2.4 μm (horizontal) 2.5 μm (vertical)	-0.3 dB	2.5 μm (horizontal) 2.6 μm (vertical)

3.3.2 Hybridly Integrated III-V Laser

In this section, the flip-chip hybrid integration process developed within this work is experimentally evaluated by the hybrid assembly of III-V DFB laser components to SiN TriPleX evaluation chips. Three different hybrid assembly methods are investigated. All hybrid assemblies were carried out using a manual die-bonder (FINEPLACER lambda).

Classical Active Alignment with AuSn Solder Bonding

In this assembly method, a current is applied to the III-V chip, and light that couples to the SiN waveguide is used as a feedback signal for the active alignment of the chips. This

corresponds to the common way of active alignment and thus is referred to as classical active alignment within this work. The basic setup is depicted in Figure 54 (a). The III-V chip is held by the vacuum tool of the bonding machine (FINEPLACER lambda) and placed in the etched recess on the SiN TriPleX chip. The III-V laser is passively aligned in three degrees of freedom (y , R_x , R_z in Figure 46) via the vertical alignment stops. The distance of the chips in z' -direction and the rotation of the chips in R_y -direction are manually aligned by using a visual overlay image of the III-V and the SiN TriPleX chips. For the remaining and most critical degree of freedom in the horizontal direction (x'), classical active alignment is used. A current is applied to the III-V chip by connecting the vacuum tool and the SiN TriPleX bonding pad to a current source (c.f. Figure 54 (a)). The III-V chips have a 3 μm thick AuSn metallization layer that is thick enough so that it gets in contact with the SiN TriPleX bonding pad when the III-V chip is placed into the etched recess. The vertical alignment stops are then not yet in contact and the chips have a vertical misalignment of about 1 μm . The misalignment is small enough so that some light couples into the SiN TriPleX waveguide and can be used as a feedback signal for the horizontal active alignment. The light is measured with a cleaved single-mode fiber at the SiN TriPleX chips output facet. To apply this process on a wafer-scale, extra waveguides that are accessed via grating couplers [79] or nano-printed optical probes [80] could be implemented for probing. After placing the III-V chip on different positions to determine the optimum horizontal position, the soldering process is started. The soldering process starts by removing the vacuum tool from the III-V chip and heating the vacuum tool and the substrate to elevated temperatures (c.f. Figure 54 (b)). The substrate temperature is kept slightly below the eutectic temperature of AuSn to prevent it from melting. Removing the bonding tool from the III-V chip prevents misalignment that is caused by the thermal expansion of the bonding machines materials. After the system has thermally settled, the substrate temperature is increased above the eutectic temperature of AuSn and the vacuum tool is pressed onto the III-V chip. The AuSn then forms a solder bond between the chips and the III-V chip is passively aligned in the vertical direction by pressing down on the mechanical alignment stops. The vacuum tool is removed after a short time to mitigate misalignment through thermal expansion. Finally, the substrate is cooled to solidify the AuSn solder bond. The process is carried out in an air environment. The full heating cycle, including cooling, takes about 700 seconds.

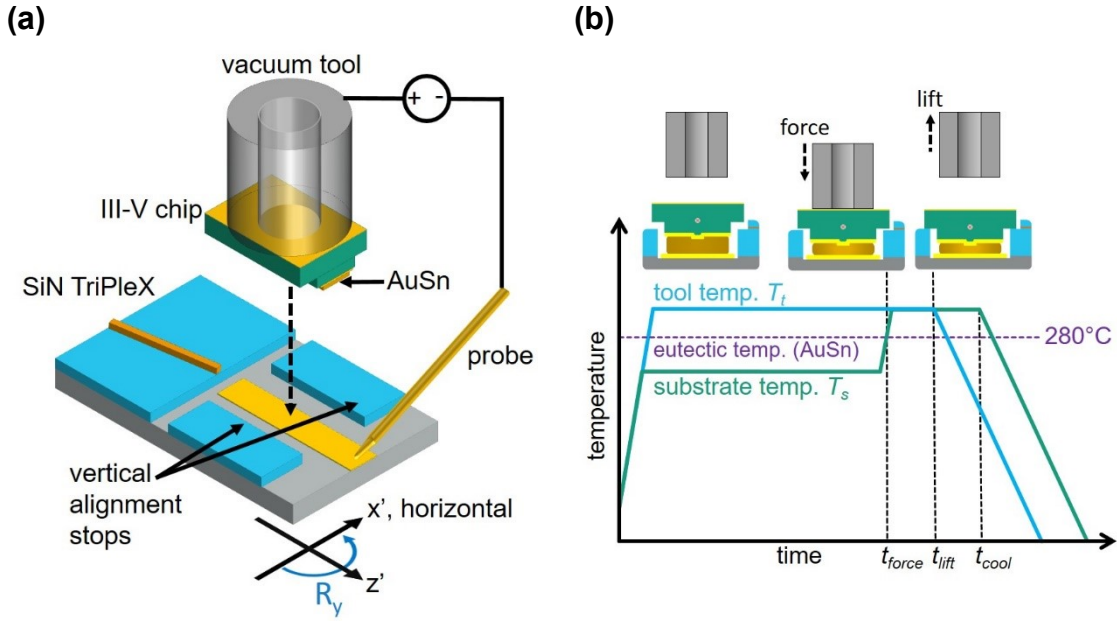


Figure 54: Schematic illustration of the setup for the classical active alignment method (a) and the heating cycle used for the AuSn solder bonding (b) $t_{force} = 150$ s, $t_{lift} = 230$ s, $t_{cool} = 400$ s, $T_s = 260$ °C, $T_t = 330$ °C, force = 1 N.

Figure 55 (a) shows exemplarily the excess coupling loss for classical active alignment in the horizontal direction with a distance $d_{z'} = 6$ μ m between the chips to prevent facet damage. The measured values (black circles) show good agreement to the theoretical curve (blue line), which is based on Gaussian approximation. In the future, the overall processing time could be reduced by taking fewer measurement points and determining the optimum position based on the theoretical curve. For the bonding machine used here (FINEPLACER lambda), the time from one measurement point to the next takes about 10 s.

Figure 55 (b) shows the measured chip-to-chip coupling efficiency for three individual III-V DFB lasers that were consecutively integrated using the classical active alignment method with AuSn solder bonding. The coupling efficiency was measured by comparing the pulsed facet output power of the III-V laser before hybrid assembly with the pulsed output power at the SiN TriPleX output facet after hybrid assembly. The devices exhibit a coupling efficiency of around -3.2 dB with less than 0.4 dB deviation from the average value. This suggests a good reproducibility of the process, but more samples would be required for an accurate evaluation. The average coupling efficiency is 2 dB lower than the -1.2 dB expected from the results of the far-field measurements (c.f. Table 2). This difference can be attributed to non-perfect horizontal/vertical alignment, non-Gaussian beams, and residual reflections of the not AR-coated waveguide facets on SiN TriPleX. Coupling efficiencies up to -1.5 dB are achieved for the alternative assembly methods (c.f. Figure 58 (a), Figure 60 (b)). These alternative assembly methods differ primarily in their horizontal alignment accuracy. It is

therefore estimated that the classical active alignment method with AuSn solder bonding comprises up to 1.7 dB reduction of coupling efficiency due to horizontal misalignment. For the given alignment tolerance (c.f. Figure 55 (a)), this corresponds to about 1.5 μm misalignment in one direction. A possible explanation for the misalignment is thermal expansion of the bonding machine when the vacuum tool is in contact with the III-V chip during the soldering process (c.f. t_{force} to t_{lift} in Figure 54 (b)). This issue could be mitigated in the future by using a bonding machine with a localized heating process such as laser-assisted die bonding [52] where thermal expansion is much less significant. Additionally, this would allow omitting the waiting time for thermal expansion to settle (time until t_{force} in Figure 54 (b)) which would significantly reduce processing time.

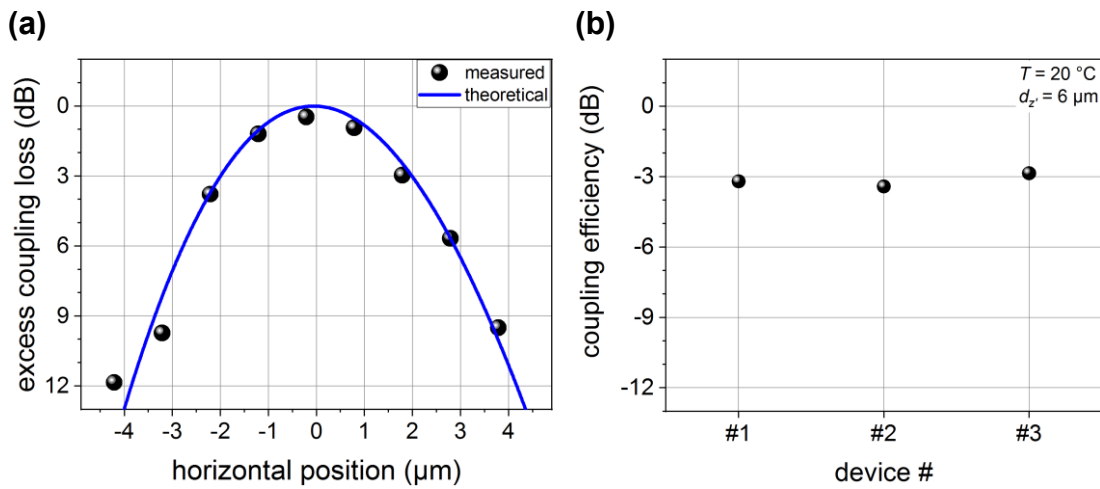


Figure 55: Excess coupling loss (a) for classical active alignment in the horizontal direction. Measurements (a, circles) are based on measured SiN TriPleX relative output power. Theory (a, blue line) is based on Gaussian approximation (38) with MFDs derived from far-field measurements (c.f. Figure 53). Measured chip-to-chip coupling efficiency (b) for three III-V DFB laser devices hybridly integrated to SiN TriPleX with classical active alignment and AuSn solder bonding. $d_z = 6\text{ }\mu\text{m}$, $T = 20\text{ }^{\circ}\text{C}$.

Next, the thermal properties of the AuSn solder bond are investigated. For a hybridly integrated chip, the thermal resistance between the integrated III-V DFB laser and a heatsink is measured to be 81 K/W (c.f. Figure 56 (a)). For comparison, similar DFB lasers that were solder bonded p-side down on an AuSn coated aluminum nitride submount exhibited a thermal resistance of about 55 K/W. This difference is larger than expected and cannot be explained purely by the thermal resistance of the silicon substrate. Figure 56 (b) shows an example of a III-V chip that was mechanically removed after it was bonded to a SiN TriPleX chip with the AuSn solder process. The connection of AuSn to the SiN TriPleX Au bonding pad seems to be very inhomogeneous with some areas showing no sign of a metallic bond between the AuSn and the Au bonding pad. Such areas are expected to have a very low

thermal conductivity, which can explain the large measured thermal resistance. Possible reasons for the poor quality of the solder joint are oxidization or other contaminations of the metallic surfaces before the soldering process or oxidization during the process. In the future, this could be avoided by surface cleaning (e.g. ultrasonic cleaning or ion sputtering) before the soldering process and using an inert gas atmosphere (e.g. nitrogen) during the soldering process.

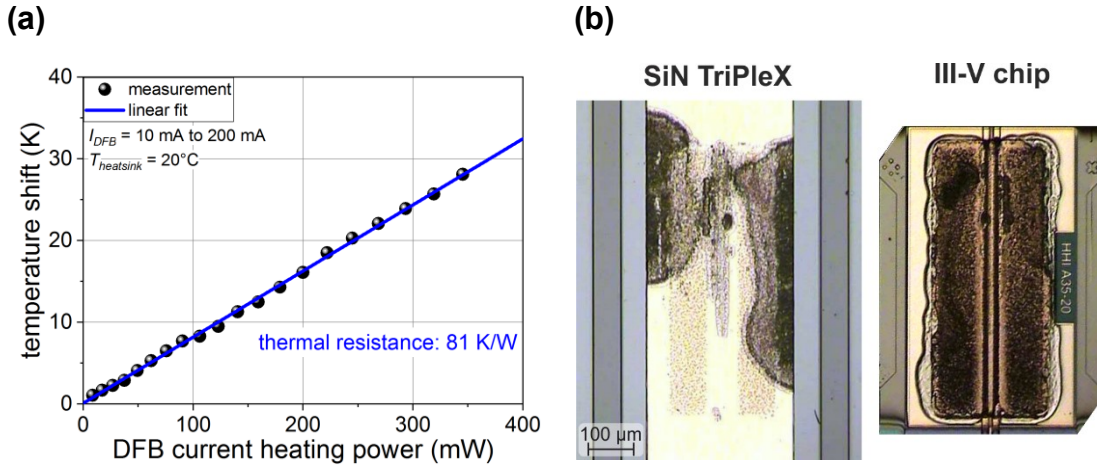


Figure 56: (a): Temperature shift versus DFB current heating power for a III-V DFB laser hybridly integrated to SiN TriPleX with the AuSn solder process. The temperature shift is extracted from the measured lasing wavelength with the relation of 0.1 nm/K. The DFB current heating power corresponds to the electrical power applied to the DFB laser minus the measured optical facet power. The hybridly integrated chip was placed on a copper heatsink. (b): Mechanically removed III-V test chip after AuSn solder bonding to SiN TriPleX bonding pad.

Visual Alignment with Gold Sinter Paste Bonding

For the assembly method described in this section, a gold sinter paste (AuroFUSETM) is used instead of the AuSn solder shown in the previous section. The paste consists of gold nanoparticles (average particle size: $\sim 300 \text{ nm}$) mixed with an organic solvent [74]. The key advantage of using the gold sinter paste instead of AuSn solder is that it is fluid at room temperature. This allows decoupling the optical alignment process from the soldering/sintering process, which prevents the issue of optical misalignment from thermal expansion. The biggest drawback is that the gold sinter paste is nonconductive before it has been sintered. For the flip-chip assembly used in this work, this means that it is not possible to apply a current to the III-V chip and thus alternatives to classical active alignment have to be found. One alternative is to perform the full optical alignment via visual overlay images, which is referred to here as visual alignment. The III-V and the SiN TriPleX chip comprise special alignment marks that allow visual alignment of the SiN waveguide to the nonvisible

buried waveguide of the III-V chip. Figure 57 (a) shows an example of the overlay image with an inset where the visual alignment marks are highlighted in white. A distance of $6\text{ }\mu\text{m}$ is set between the chips to prevent facet damage. The visual alignment marks are manually aligned based on a beam emission angle of 29.6° calculated with (39). Before the III-V chip is placed down, a thin layer of gold sinter paste is applied with a needlepoint (c.f. Figure 57 (b)). The gold sinter paste is spread over an area only about half the size of the bonding pad to prevent the paste from being squeezed onto the vertical alignment stops or the optical facets when the III-V chip is placed down. After visual alignment and application of the gold sinter paste, the III-V chip is placed down with a force of 0.3 N so the vertical alignment stops get in contact. The vacuum tool, which holds the III-V chip, is then removed and the whole substrate is heated to $250\text{ }^\circ\text{C}$ for 20 minutes to form a solid gold connection between the chips via sintering. For the results shown here, this process was performed individually for each bonded chip. An option to reduce processing time in the future would be to consecutively place several III-V chips on SiN TriPleX and then carry out the sintering process for several chips at once.

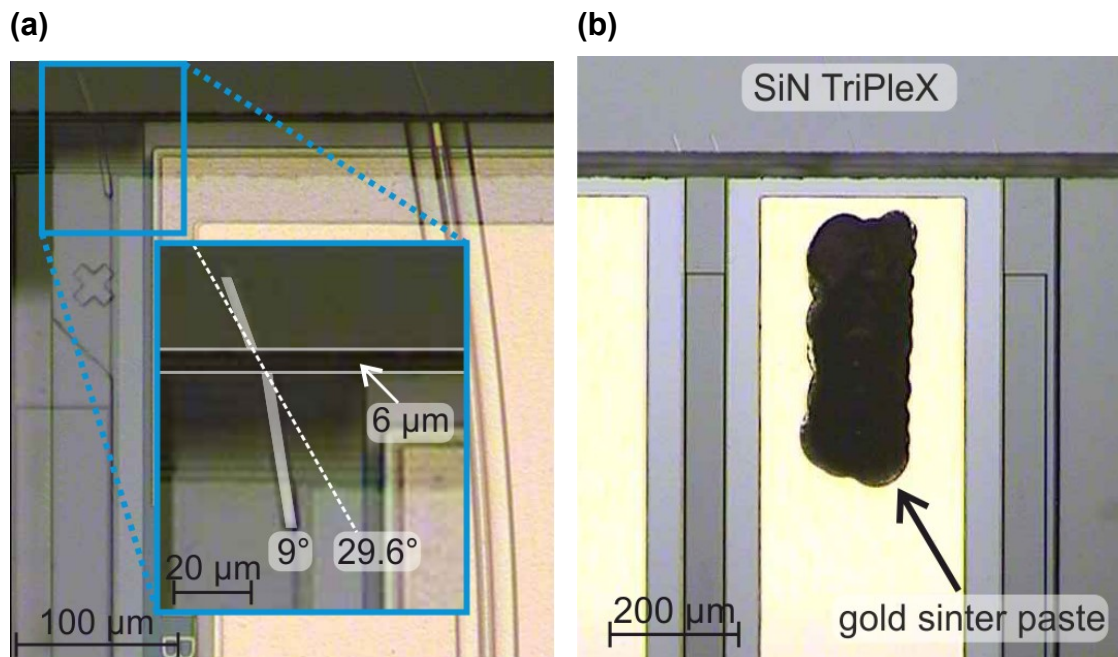


Figure 57: Visual alignment via overlay image of III-V chip and SiN TriPleX (a). Visual alignment marks are shown highlighted in white in the magnified inset. Photograph of gold sinter paste applied to bonding pad of SiN TriPleX (b).

Figure 58 (a) shows the measured chip-to-chip coupling efficiency for five individual III-V DFB laser chips that were consecutively integrated with visual alignment and gold sinter paste bonding. The coupling efficiency was measured by comparing the pulsed facet output power of the III-V lasers before hybrid assembly with the pulsed output power of the SiN

TriPleX output facet after hybrid assembly. The results show that the visual alignment method allows for a high coupling efficiency up to -1.6 dB, but it suffers from poor reproducibility with the lowest coupling efficiency being -7.5 dB. Assuming that the coupling efficiency for optimum alignment is around -1.5 dB (c.f. Figure 60 (b)), the excess coupling loss is up to 6 dB. This corresponds to about 2.8 μm misalignment in the horizontal direction (c.f. Figure 55). This can be explained only partly by the placement accuracy of the bonding machine, which is given by the supplier's spec sheet with $\pm 0.5 \mu\text{m}$. Before each hybrid assembly, the machine's placement accuracy was verified with special reference structures. Based on the practical experience with the visual alignment process, the misalignment is believed to be caused primarily by the inaccurate alignment of the visual alignment marks in the overlay image. For the given image quality (c.f. Figure 57 (a)), it has proven difficult for a human operator to identify the chip edges and visual alignment marks on a micrometer scale. With better image quality and with the aid of image recognition software a higher reproducibility is expected.

Based on the measured shift of the DFB lasing wavelength, the thermal resistance was evaluated with 53 K/W (c.f. Figure 58 (b)). This is significantly lower than for the AuSn process (c.f. Figure 56 (a)) and indicates that the gold sinter paste forms a solid metallic bond between the III-V chips to the SiN TriPleX bonding pads.

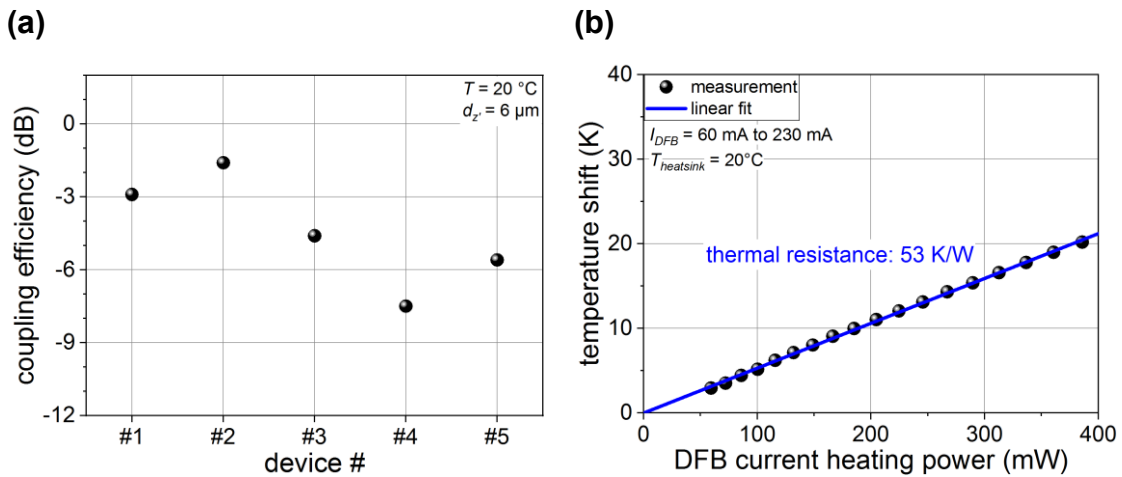


Figure 58: Measured chip-to-chip coupling efficiency (a) and thermal resistance for III-V DFB lasers hybridly integrated to SiN TriPleX with visual alignment and gold sinter paste bonding. The temperature shift is extracted from the measured lasing wavelength with the relation of 0.1 nm/K. The DFB current heating power corresponds to the electrical power applied to the DFB laser minus the measured optical facet power. The hybridly integrated chips were placed on a copper heatsink.

OBR Alignment with Gold Sinter Paste Bonding

In this section, a novel alignment technique utilizing optical backscatter reflectometry (OBR) is demonstrated. Within this work, this alignment technique is referred to as OBR alignment. OBR alignment has the advantage that it is a form of active alignment where the active feedback signal corresponds to the chip-to-chip coupling efficiency but no electrical connections to the chips are required. As such, OBR alignment is suitable for the alignment of active as well as passive components and allows the use of the nonconductive gold sinter paste (AuroFUSE™) described in the previous section. The setup for the OBR alignment technique is shown schematically in Figure 59 (a). The III-V chip is placed with a coarse visual pre-alignment into the etched recess of the SiN TriPleX chip. An optical backscatter reflectometer (Luna OBR 4600) is connected via cleaved single-mode fiber to the output waveguides of the SiN TriPleX chip. To apply this process on a wafer-scale, extra waveguides that are accessed via grating couplers [79] or nano-printed optical probes [80] could be implemented for probing. The reflectometer uses wavelength-swept optical frequency domain reflectometry (OFDR) to measure the reflected amplitude versus time of flight, which is scaled to a distance for a given group index. The highest available wavelength range of 1601 nm to 1613 nm is chosen to minimize absorption in III-V chip. The signal measured by the reflectometer is shown exemplarily in the inset of Figure 59 (a). It shows a large reflection around 2038 mm that corresponds to the fiber-to-chip interface and a smaller reflection around 2050 mm that corresponds to the chip-to-chip interface. This is followed by two additional reflections that were only visible when the III-V chip was placed down. These two reflections correspond to reflections from within the III-V chip. The first of the two is related to the effective index change between the SOA and the DFB section of the III-V chip. The second is related to the III-V chips back facet, which was anti-reflection coated for the shown example. The amplitude of reflections measured by the reflectometer depends on the related reflection coefficient and the optical losses on the path from and to the reflectometer. Since the loss of the path to a reflection from within the III-V chip includes the chip-to-chip coupling efficiency, the reflections amplitude R can be expressed with

$$R = R' - 2\eta_{excess}, \quad (43)$$

where R' is the measured reflection amplitude in dB for optimum horizontal alignment and η_{excess} is the excess chip-to-chip coupling loss in dB due to horizontal misalignment. As such, the amplitude of a reflection from within the chip can be used as an active feedback signal for the optical alignment process. Figure 59 (b) shows exemplarily the excess coupling loss

extracted from the reflection amplitude at the SOA/DFB interface of a III-V DFB laser for different horizontal positions on the SiN TriPleX chip. The theoretical excess coupling loss (blue line) based on Gaussian approximation shows good agreement with the measurement (black circles) and the position of highest coupling efficiency can be identified. After the OBR alignment process, gold sinter paste is applied to the SiN TriPleX bonding pad as described in the previous section and the III-V chip is placed down with a force of 0.3 N. The vacuum tool is then removed from the III-V chip and the substrate is heated to 250 °C for 20 min for sintering of the gold paste.

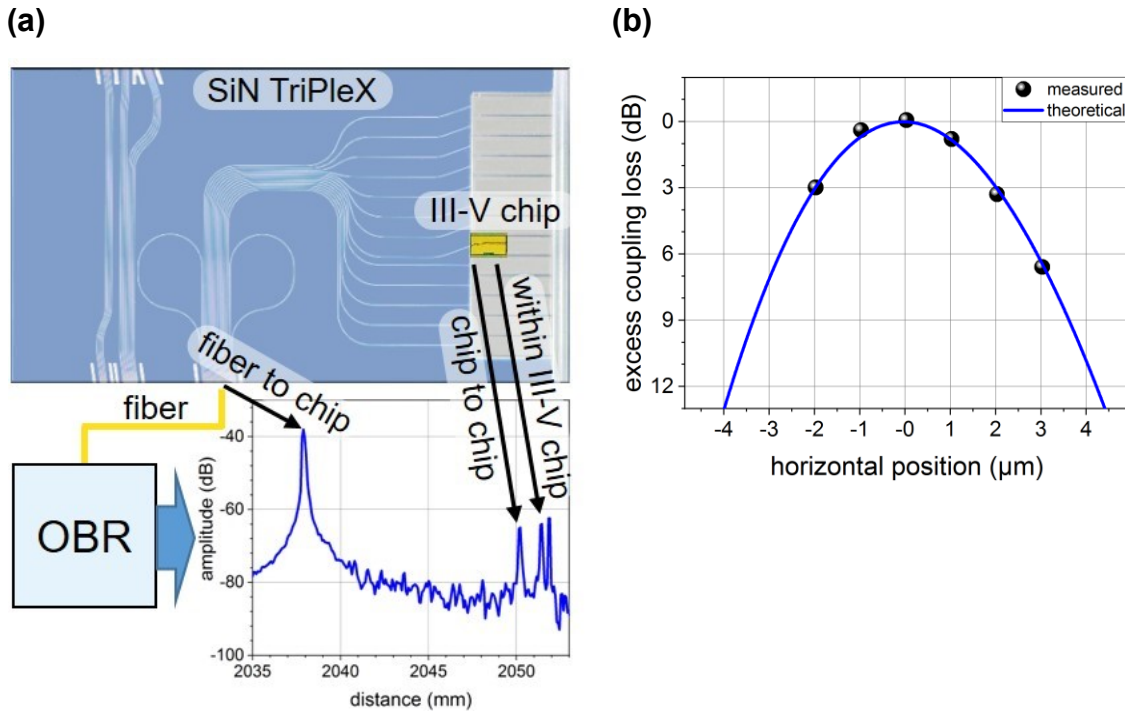


Figure 59: (a): Schematic setup for OBR alignment. The optical backscatter reflectometer (OBR) is connected to the SiN TriPleX chip via cleaved single-mode fiber. The measured reflection amplitude versus distance ($n_g = 1.5$) is shown in the inset. (b): Excess coupling loss versus horizontal position of III-V chip. Measurements (circles) are calculated with (43) from reflection amplitudes measured within the III-V chip. Theory (blue line) is based on Gaussian approximation (38) with MFDs derived from far-field measurements (c.f. Figure 53). $d_z = 6 \mu\text{m}$, $T = 20 \text{ }^\circ\text{C}$.

Figure 60 (a) shows an example of several III-V DFB lasers integrated to a SiN TriPleX evaluation chip using the OBR alignment method with gold sinter paste bonding. The coupling efficiency was measured for 18 consecutively integrated III-V DFB lasers by comparing the pulsed facet output power of the III-V lasers before hybrid assembly with the pulsed output power of the SiN TriPleX output facet after hybrid assembly (Figure 60 (b)). The integrated chips exhibit a coupling efficiency with an average of -2.1 dB and the assembly process shows good reproducibility with a standard deviation of 0.35 dB. The variations in coupling efficiency are expected to be primarily caused by horizontal/vertical

misalignment or imperfections of the InP or SiN TriPleX facets. The highest measured coupling efficiency is -1.5 dB, which is close to the theoretical value of -1.2 dB given in Table 2. The overall coupling efficiency could be further improved by reducing the safety distance between the chips, which is currently set to 6 μm . Based on the coupling efficiency estimated with Gaussian approximation (c.f. Table 2), up to 0.8 dB improvement is possible. This would result in a highest coupling efficiency of -0.7 dB. Additional improvement could be achieved by fine-tuning of the SSC designs for better mode matching.

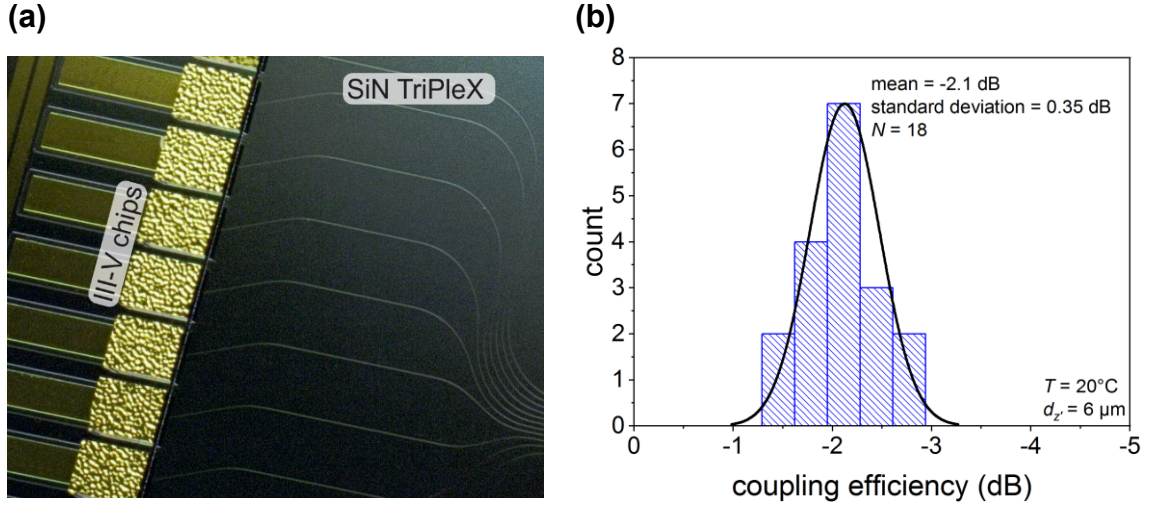


Figure 60: Photograph (a) and histogram of measured coupling efficiency (b) of III-V DFB lasers hybridly integrated via OBR alignment and gold sinter paste bonding.

The presented flip-chip hybrid integration process has the advantage that it allows the integration of III-V chip arrays without added complexity compared to single-chip integration. The mechanical alignment stops passively align the full array in the vertical direction. In the horizontal direction, the array is aligned by the alignment of a single device in the array. Figure 61 (a) shows an example of a III-V array with four DFB lasers, which is hybridly integrated to the SiN TriPleX evaluation chip. In total, three separate arrays were hybridly integrated using the OBR alignment method with gold sinter paste bonding. The coupling loss for each laser in the array was measured by comparing the pulsed facet output power of the III-V lasers before hybrid assembly with the pulsed output power of the SiN TriPleX output facets after hybrid assembly (c.f. Figure 61 (b)). The arrays exhibit an equally high average coupling efficiency of -2.3 dB, -2.4 dB, and -2.2 dB for array#1, array#2, and array#3, respectively. Array#1 shows the smallest variation of coupling efficiency within the array with less than 0.1 dB from largest to smallest value. Array#3 shows the largest variation with up to 1.3 dB. The alternating pattern of coupling efficiency for array#3 indicates that the variation is not caused by vertical misalignment. Vertical misalignment is expected to cause a monotonical change of coupling efficiency within the array. Horizontal misalignment

is also unlikely because the horizontal alignment within a single array is defined by lithographic accuracy. A possible explanation is the occurrence of imperfections at the SiN TriPleX facet. This is indicated by the irregular scattering of light at the SiN chips facet in Figure 61 (a) and by the roughness of the SiN chips facet in Figure 57 (a, b). This issue could be resolved in the future by optimizing the SiN TriPleX facet processing or by covering the facets with index matching material. Overall, the integration of full III-V chip arrays yields a performance that is equivalent to single-chip integration.

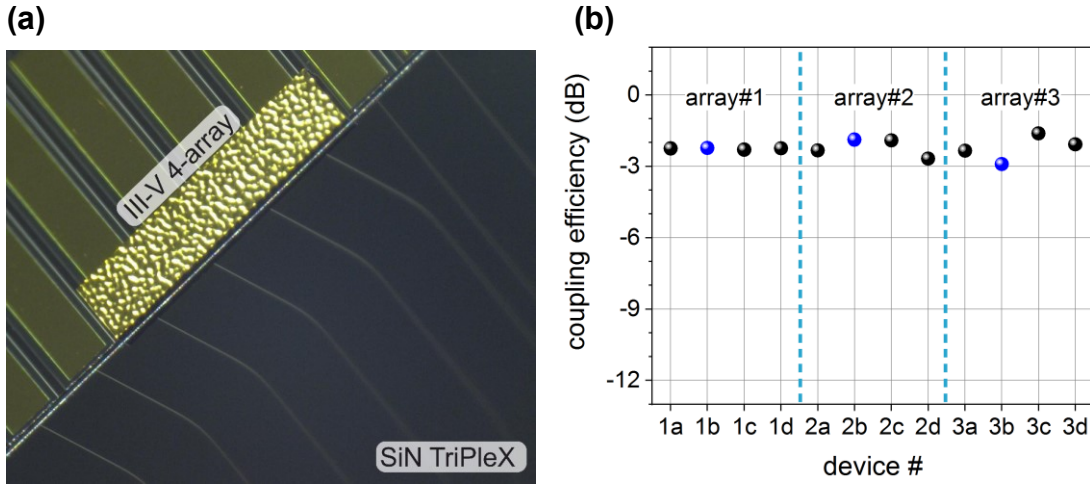


Figure 61: Photograph (a) and measured coupling efficiency (b) of III-V DFB laser arrays hybridly integrated via OBR alignment and gold sinter paste bonding. III-V DFB devices that were used for the OBR alignment are marked as blue circles.

Figure 62 (a) shows exemplarily the measured optical power coupled to the SiN TriPleX waveguide for an individual III-V DFB laser integrated via OBR alignment and gold sinter paste bonding. The device's threshold current ranges from 6 mA (20 °C) to 25 mA (85 °C). A CW optical power of more than 60 mW is coupled to the SiN TriPleX waveguide with a chip-to-chip coupling efficiency of -1.6 dB. Up to 25 mW is achieved at an elevated temperature of 85 °C, which can be attributed to the good thermal properties of the gold sinter paste bonded chip. A thermal resistance of 52 K/W was measured by evaluating the shift of the lasing wavelength with increasing DFB current. Figure 62 (b) shows the measured wavelength for 20 °C and 85 °C heatsink temperature with the corresponding SMSR for all temperatures shown in the inset. The device exhibits an SMSR exceeding 40 dB over the full operating range without any abrupt changes or mode jumps. This indicates that for the III-V DFB laser integration, optical feedback from the chip-to-chip interface is sufficiently reduced by the tilted waveguide design together with the anti-reflection coated III-V facet. It should be noted, that the SiN TriPleX facet is uncoated and no index matching material was used.

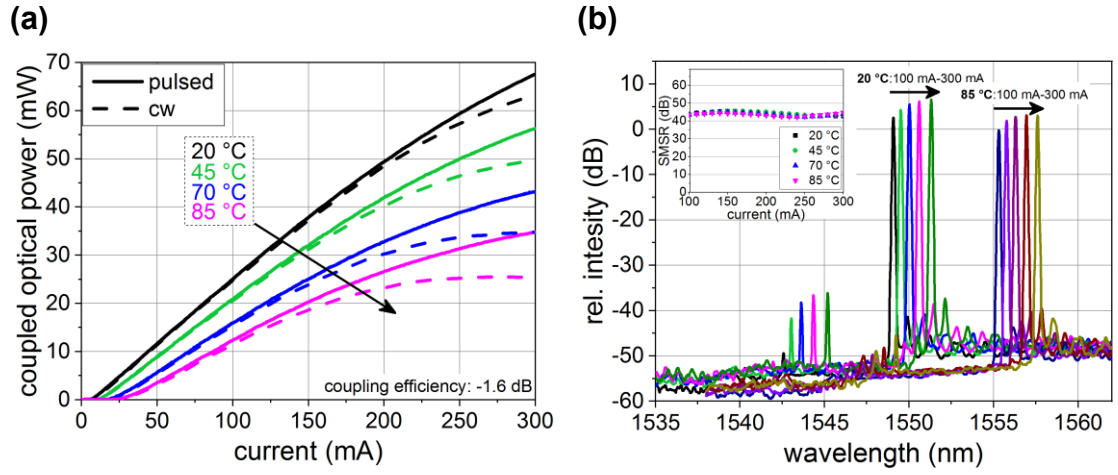


Figure 62: Measured optical power coupled to SiN TriPleX (a) and optical spectra (b) for a III-V DFB laser hybridly integrated via OBR alignment and gold sinter paste bonding. The spectral side mode suppression ratio (SMSR) is shown in the inset of (b). The III-V DFB laser is 700 μm long with anti-reflection coated front facet and high-reflection coated back facet.

3.3.3 Hybridly Integrated Tunable Laser

In this section, the flip-chip hybrid integration process developed within this work is evaluated with regard to the integration of III-V chips to complex SiN TriPleX PICs, by demonstrating the assembly of a hybridly integrated tunable laser. The OBR alignment method with gold sinter paste bonding is used, as it has proven to yield the best performance regarding coupling efficiency and thermal properties (c.f. section 3.3.2).

Assembly Process

A 700 μm long III-V gain chip (c.f. section 3.2.1) is hybridly integrated to a SiN TriPleX external cavity (c.f. section 3.2.2) via OBR alignment with gold sinter paste bonding (c.f. section 3.3.2). To mitigate any internal reflections for the hybrid laser, index matching glue (Vitalit 1528) is applied to the chip-to-chip interface after the bonding. The front facet of the III-V gain chip is anti-reflection coated against $n = 1.5$. For the OBR alignment, the optical backscatter reflectometer is connected to output#1 (c.f. Figure 52) of the SiN TriPleX external cavity. Due to its complex waveguide structure, the measured OBR signal (c.f. Figure 63) yields much more peaks than the signal measured at the evaluation chip from the previous section (c.f. Figure 59). The OBR signal of the external cavity shows a large reflection peak at the beginning that is followed by multiple equidistant peaks with a linear dropping amplitude (c.f. Figure 63 (left)). The large peak at the beginning corresponds to the fiber to SiN TriPleX chip interface. The equidistant peaks with dropping amplitude

correspond to light that is guided back to the optical backscatter reflectometer through circulation in one of the rings. As such, these peaks do not correspond to actual reflections and are referred to here as circulations C_N . By ignoring the circulations in the measured signal, one can identify peaks that correspond to actual reflections in the chip. The inset on the right of Figure 63 shows the measured OBR signal at the distance that corresponds to the position of SiN to III-V chip-to-chip interface. Without the III-V gain chip placed into the etched recess on the SiN TriPleX chip, a single reflection peak R_{SiN} that corresponds to the reflection at the SiN TriPleX facet is visible (c.f. Figure 63 (right, top)). By placing the III-V gain chip in front of the SiN TriPleX facet a second peak $R_{\text{III-V}}$ that corresponds to the HR coated back facet of the III-V gain chip appears (c.f. Figure 63 (right, middle)). The amplitude of $R_{\text{III-V}}$ is related to the excess chip-to-chip coupling loss with (43) and as such can be used as an active feedback signal for the alignment. Figure 64 shows the corresponding measured excess coupling loss (black circles) and the theoretical curves assuming air (blue line) or index matching glue (green line) as material between the facets. The alignment is carried out in air because index matching glue would not withstand the heat of the bonding process. The theoretical curve in air (blue line) shows good agreement with the measurement and the optimum coupling position can be identified. The III-V chip is then placed on a position with an intentional misalignment $d_{x'}$, based on (41), so an optimum coupling efficiency is achieved when index matching glue is applied after the bonding (green line). The corresponding measured OBR signal is shown in Figure 63 (right, middle). The III-V chip is bonded to the SiN TriPleX chip using gold sinter paste as described in section 3.3.2. After the bonding process, index matching glue is applied to the facets (c.f. Figure 52 (bottom)). After the application of the index matching glue, the reflection amplitude $R_{\text{III-V}}$ increases by 3.1 dB (c.f. Figure 63 (right, middle & bottom)), which corresponds to 1.55 dB improvement in chip-to-chip coupling efficiency (c.f. (43)). This finding agrees well with the theoretical curves based on Gaussian approximation that yield an estimated difference of 1.3 dB in coupling efficiency when index matching glue is applied (c.f. Figure 64 green curve & blue curve at $d_{x'}$). By looking at the amplitude of R_{SiN} one can see a reduction of around 7.5 dB, which correlates to a reduced reflection coefficient of the SiN TriPleX to III-V chip-to-chip interface due to index matching. Thus, the OBR alignment method allows simultaneously monitoring the coupling efficiency and reflection strength of the chip-to-chip interface. Overall, the OBR alignment method proves to be well suited for the alignment of III-V chips to complex PICs such as external cavities.

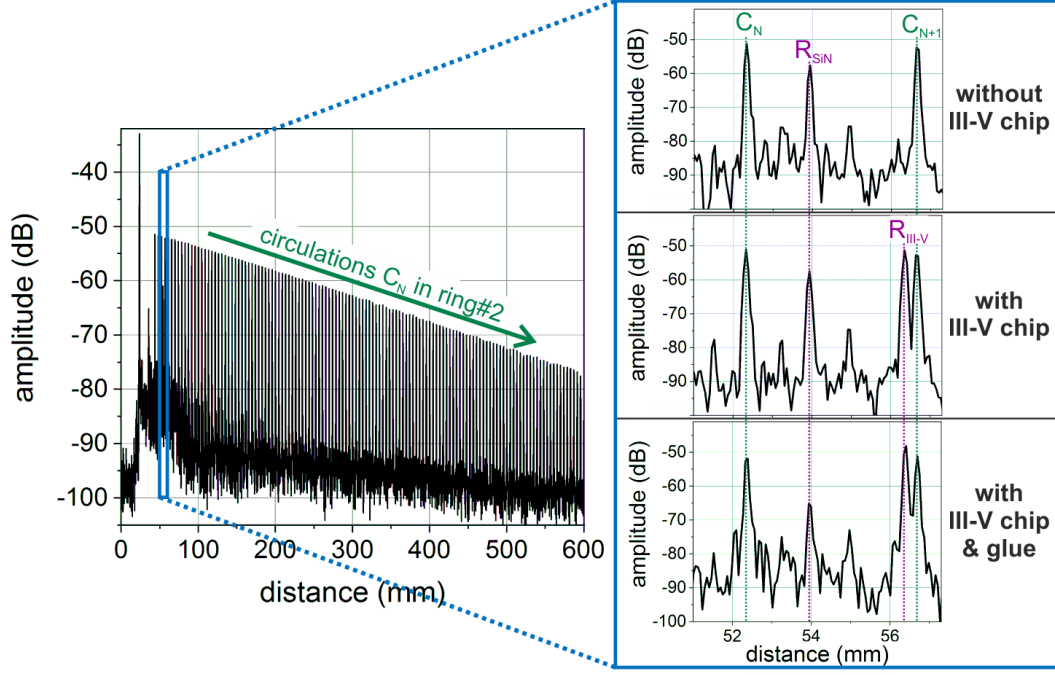


Figure 63: Measured reflection amplitude versus distance ($n_g = 1$) for OBR alignment of III-V gain chip to SiN TriPleX external cavity. The inset shows the reflection amplitude at the position of the chip-to-chip interface without the III-V chip placed down (top), with the III-V chip placed down (middle) and with bonded III-V chip and index matching glue applied (bottom). Peaks marked with C_N correspond to circulations in ring#2, R_{SiN} corresponds to the reflection from the SiN TriPleX facet, and R_{III-V} to the reflection from the III-V gain chips back facet. The signal is measured at output #1 (c.f. Figure 52). $\lambda_{scanrange} = 1590.67 \text{ nm}$ to 1613.00 nm , $T = 20 \text{ }^\circ\text{C}$.

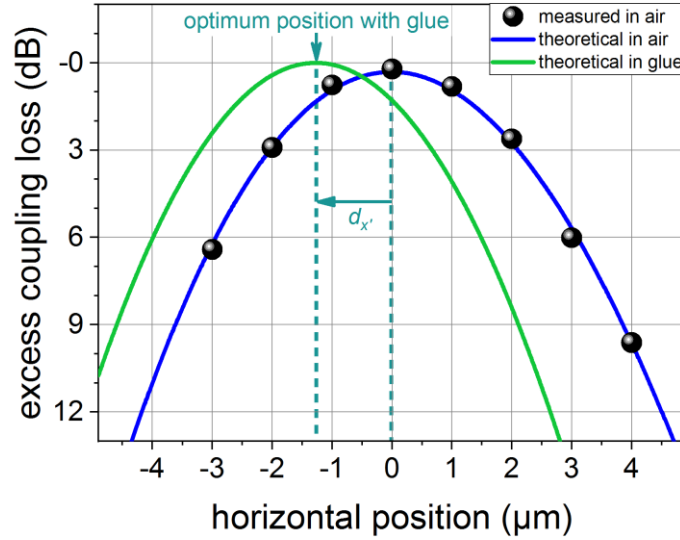


Figure 64: Excess coupling loss versus horizontal position of III-V gain chip for hybrid integration to SiN TriPleX external cavity with OBR alignment. Measurements (circles) are based on measured amplitude R_{III-V} in Figure 63. Theory (blue line, green line) is based on Gaussian approximation (38) with MFDs derived from far-field measurements (c.f. Figure 53). For the theoretical curve in glue (green line) a horizontal misalignment $d_{x'} = 1.25 \text{ } \mu\text{m}$, based on (41), is assumed. $d_{z'} = 6 \text{ } \mu\text{m}$, $T = 20 \text{ }^\circ\text{C}$.

Tunable Laser Performance

In this section, a basic experimental characterization of the tunable laser performance will be given. Figure 65 (a) shows the measured pulsed output power of the hybridly integrated tunable laser before and after the index matching glue is applied. With index matching glue, the device exhibits a threshold current of 10 mA, a slope efficiency of around 0.22 W/A, and a pulsed optical output power exceeding 60 mW (c.f. Figure 65 (a, green curve)). Without index matching glue, the threshold current is 13 mA and the slope efficiency 0.17 W/A (c.f. Figure 65 (a, blue curve)). This confirms the previous finding from the OBR measurement that the coupling efficiency is improved with index matching glue and indicates that the intentional misalignment d_x was chosen correctly. Because the chip-to-chip interface lies within the laser cavity, it is difficult to measure the exact chip-to-chip coupling efficiency for the hybrid laser. Based on the theoretical coupling efficiency of -0.3 dB (c.f. Table 2) and assuming a similar difference between theory and experiment as found for integrated III-V DFB lasers (c.f. section 3.3.2), the chip-to-chip coupling efficiency for the tunable laser is estimated to be around -1 dB to -1.5 dB.

To evaluate the tuning capability of the device, an electrical current was applied to the heaters of the ring resonators. The tunable laser is capable of full C-band tuning (c.f. Figure 65 (b)). By applying an electrical power up to 530 mW to the heaters of ring#1 and ring#2 the wavelength is tuned from 1529.4 nm to 1568.5 nm. The relative peak intensity varies up to 1.5 dB over the whole tuning range. By applying electrical power to the heaters of the directional coupler dc#1 (c.f. Figure 52) the optical power at output#4 could be adjusted and the peak intensity equalized.

The hybridly integrated tunable laser is a promising candidate for tunable laser sources in modern communication and sensing applications. Compared to fully III-V based tunable lasers it offers a price advantage because the large external cavity, which is required for widely tunable lasers, is fabricated with the low-cost material SiN TriPleX. Due to the extremely low loss of SiN TriPleX waveguides, these hybrid lasers are capable of achieving ultra-low linewidth [81], which makes them of particular interest for applications in sensing or coherent communication.

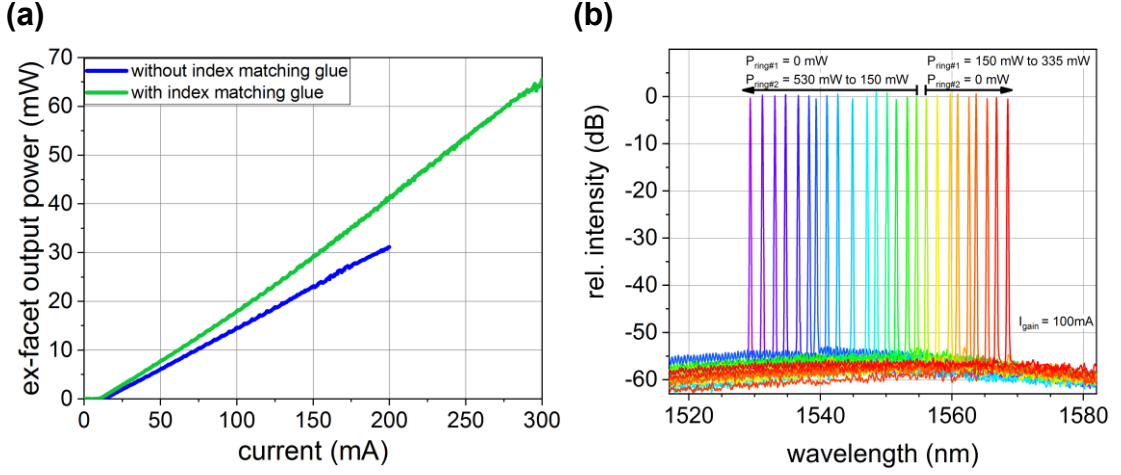


Figure 65: Measured pulsed output power (a) and optical spectra (b) of hybridly integrated tunable laser. Output power was measured at output#1-4 with an integrating sphere. Optical spectra were measured with single-mode fiber at output#4. $T = 20^\circ\text{C}$.

PIC Characterization via OBR Signal

In the previous sections, it was demonstrated how optical backscatter reflectometry can be used for the optical chip-to-chip alignment. In this section, the potential for simultaneously using the measured OBR signal for PIC characterization is investigated. As shown in Figure 63, the OBR signal that is measured at the SiN TriPleX external cavity shows multiple equidistant peaks, referred to here as circulations C_N , that correspond to light that is guided back to the optical backscatter reflectometer via circulation in one of the rings. The OBR signal measured at output#1 or output#2 is dominated by circulations corresponding to ring#2 and the signal measured at output#3 or output#4 is dominated by circulations corresponding to ring#1 (c.f. Figure 52 (top)). The subscript N corresponds to the number of round trips in the ring resonator. By converting the measured distance of each peak to a corresponding time of flight, the round trip time in the rings can be derived (c.f. Figure 66 (a)). The average round trip time corresponds to the slope of the linear fit in Figure 66 (a) which is 28.91 ps and 29.08 ps for ring#1 and ring#2, respectively. For the given ring circumferences (ring#1: 5600 μm , ring#2: 5631.64 μm) the effective group index of the SiN TriPleX waveguide can be calculated with $n_g = 1.544$.

From Figure 63 (left) one can see that the amplitude of the circulations C_N drops linearly. This can be explained by the fact that for each circulation in the ring, the light in the ring is attenuated by waveguide losses and out-coupling via the directional couplers. Thus, the average round trip loss can be derived from the slope of the linear fit on the amplitude of the circulations C_N shown in Figure 66 (b). The round trip loss of ring#1 and ring#2 is 0.270 dB

and 0.188 dB, respectively. This fits well with the out-coupling loss that was targeted in the design, which was 0.265 dB and 0.175 dB for ring#1 and ring#2, respectively. The difference of 0.005 dB and 0.013 dB can be attributed to waveguide losses, fabrication tolerances, and measurement error.

In conclusion, it was demonstrated that by analyzing the measured OBR signal during the alignment process, detailed information on the SiN TriPleX PIC can be derived and deviations from the design target can be identified. This could be used to rule out defect PICs prior to the assembly process, which can reduce overall processing time and cost.

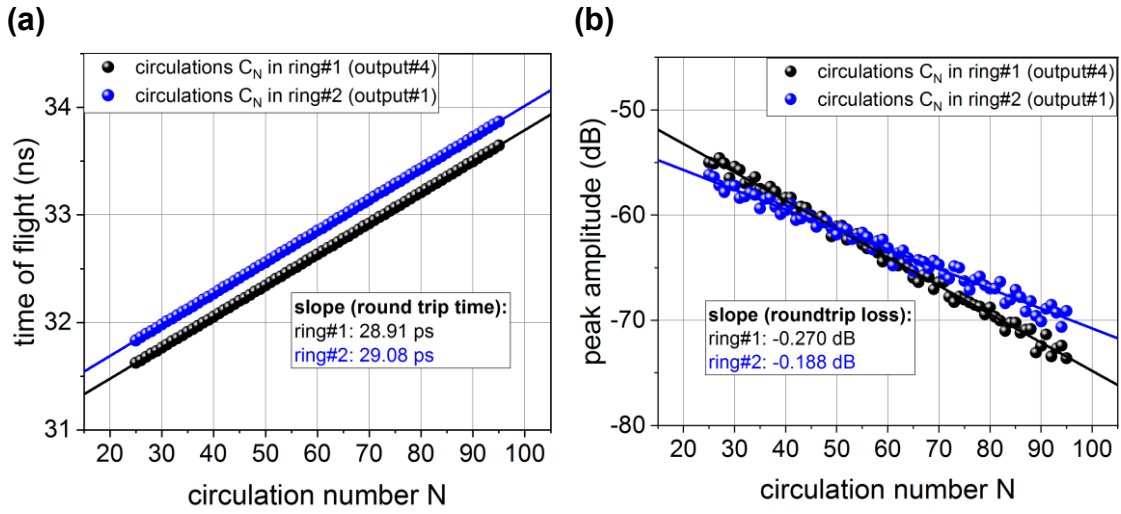


Figure 66: Measured time of flight (a) and peak amplitude (b) for circulations C_N in the OBR signal. Circulation number N corresponds to the number of round trips in the ring. $\lambda_{scanrange} = 1550$ nm to 1551.3 nm, $T = 20$ °C.

4. Hybridly Integrated EML Array

In this section, a novel hybridly integrated EML array is demonstrated. It combines the fundamental design of the EML array described in section 2.2.2 with the flip-chip hybrid integration scheme described in section 3. The hybrid EML array operates in the O-band with a wavelengths matched to the LAN wavelength division multiplexing (WDM) grid to address modern Terabit Ethernet (TbE) applications [82]. The goal in this thesis is to evaluate the feasibility of the design concept of this hybridly integrated EML array.

4.1 Design and Simulation

4.1.1 EML Array for Hybrid Integration

The basic layout of the EML array for hybrid integration is similar to that of the EML array described in section 2.2.2, so the following focuses on describing the differences in the design.

The EML array for hybrid integration comprises four EMLs at four different target wavelengths in the O-band (c.f. Figure 67) with a wavelength spacing of ~ 4.53 nm (800 GHz). The array is designed with identical active layers (c.f. Figure 3 (a)), which keep fabrication complexity low. In order to account for the different wavelength detuning of the EMLs, the EAM section length is varied over the array (EAM- λ_1 : 80 μm , EAM- λ_2 : 90 μm , EAM- λ_3 : 100 μm , EAM- λ_4 : 110 μm). The SOA length is varied corresponding to the different EAM section length (SOA- λ_1 : 170 μm , SOA- λ_2 : 160 μm , SOA- λ_3 : 150 μm , SOA- λ_4 : 140 μm). The DFB lasers have a length of 350 μm and DFB, EAM and SOA are separated by 20 μm long separation sections. The targeted operation temperature is 45 °C for semi-cooled operation. To allow for flip-chip hybrid integration, the EML array design includes SSCs, vertical alignment stops, and AuSn metallization (c.f. Figure 67). The 230 μm long SSCs (c.f. section 4.1.2) are integrated at the front facet for mode matching and increased alignment tolerance. Between the EMLs there are vertical alignment stops (highlighted green in Figure 67), which are defined by a selective etch process to provide a highly precise height relative to the optical waveguide. The AuSn metallization (highlighted orange in Figure 67) is applied to the DFB, SOA and EAM contact pads for flip-chip solder bonding to the SiN TriPleX PIC. Additional device variants, without AuSn metallization, are fabricated for gold sinter paste bonding. All bonding pads (DFB, SOA, EAM) are designed to have the same height. The back facet of the array is anti-reflection coated against air

($n = 1$) for high single mode yield. The front facet is anti-reflection coated against index matching glue ($n = 1.5$) to minimize optical back reflection from the chip-to-chip interface. Index matching glue is applied to the chip-to-chip interface after assembly, due to the known high sensitivity of EMLs regarding optical feedback.

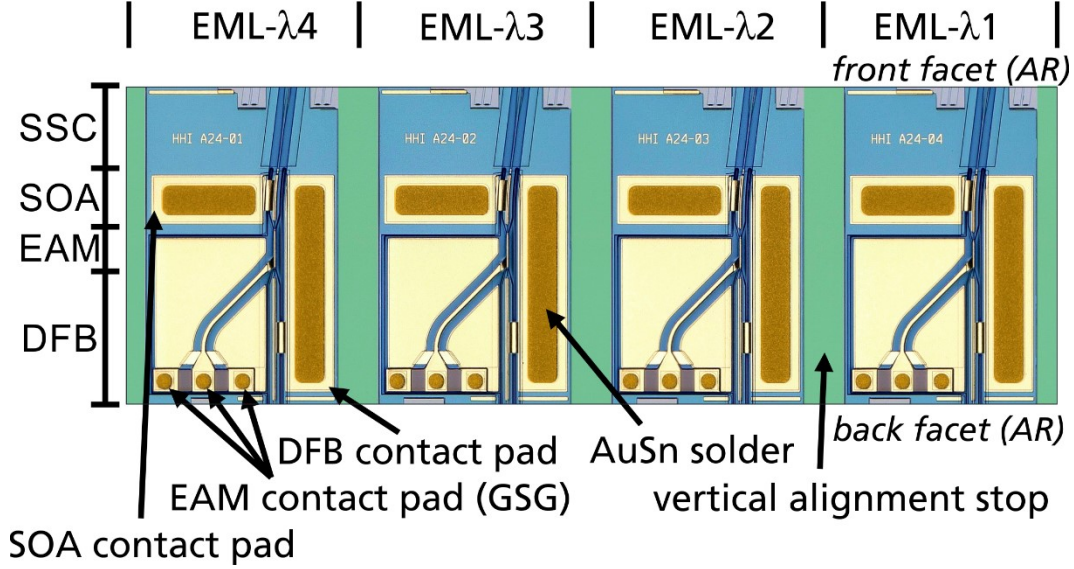


Figure 67: Top view of a fabricated EML array chip for flip-chip hybrid integration. Areas for passive vertical alignment are highlighted in green. AuSn metallization is highlighted in orange. Different chip variants with and without AuSn metallization were fabricated. Target wavelengths are λ_1 : 1295.56 nm, λ_2 : 1300.05 nm, λ_3 : 1304.58 nm, λ_4 : 1309.14 nm. Chip dimensions are 2560 μm x 870 μm .

4.1.2 EML Spot Size Converter

The layout of the integrated EML spot size converter is shown in Figure 68. The small asymmetric input mode (c.f. Figure 68 (left)), which corresponds to the mode of the ridge waveguide type active SOA section, is converted to the symmetrical mode of a buried waveguide with a mode size around 3.5 μm (c.f. Figure 68 (right)). The transition from the ridge waveguide to the buried waveguide is accomplished by a continuous widening of the ridge width w_{ridge} and a simultaneous narrowing of the buried waveguide width w_{buried} (c.f. Figure 68 (middle)). The widening/narrowing is carried out in a two-step process ($L1$, $L2$) to allow for a quick change of waveguide width where the waveguide is wide and a slow change where the waveguide is narrow. That way, the SSC can be designed with a smaller length and still be adiabatic.

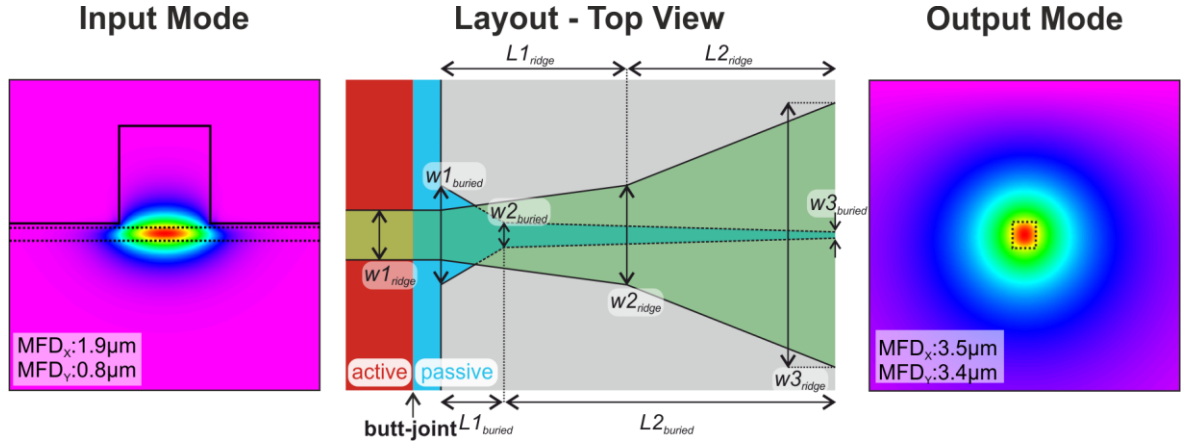


Figure 68: Schematic layout (middle) of spot size converter for hybrid integration EML Array. The input mode (left) of a ridge waveguide is converted to a circular output mode (right) of a buried waveguide. Semiconductor to air borders are indicated with solid lines, waveguide layers with dotted lines. The optical modes are simulated with RSoft.

In the area of the SSC, the InGaAlAs based active layers are etched away and an InGaAsP based passive waveguide layer (bandgap: 1050 nm) is regrown (c.f. Figure 68 (middle)). At the butt-joint, where the light couples from the active to the passive section, the ridge waveguide width $w1_{ridge}$ is kept constant. To maximize the coupling efficiency, the butt-joint transmission was simulated for different thicknesses $t_{passive}$ of the passive waveguide (c.f. Figure 69 (a)). The highest coupling efficiency of -0.13 dB is achieved for a thickness of 0.55 μm . The butt-joint interface also shows high tolerance regarding fabrications errors on the waveguide thickness with less than 0.03 dB excess loss for 100 nm deviation.

The design target for the SSC is to achieve optimum coupling efficiency to a circular Gaussian mode with 3.5 μm MFD. By varying the SSC tip width $w3_{buried}$, the size of the EMLs SSC output mode and thus the coupling efficiency to the Gaussian mode is adjusted (Figure 69 (b)). An optimum mode coupling efficiency of -0.33 dB is achieved for a waveguide width $w3_{buried}$ of 0.41 μm . The simulation results indicate that the fabrication tolerance regarding waveguide width is very strict, with up to 0.5 dB excess loss for 100 nm deviation. To keep fabrication errors to a minimum, an on-wafer ebeam lithography process was used for the structuring of the buried waveguide. For better comparison with the simulation results presented in the next paragraph, it should be noted that the results shown in Figure 69 (b) correspond to the coupling efficiency of optical modes that correspond to infinitely long straight waveguides. For a tapered waveguide of finite length, the fabrication tolerance towards small waveguide widths can be larger because the propagating mode does not expand to its full size over the length of the tapered waveguide.

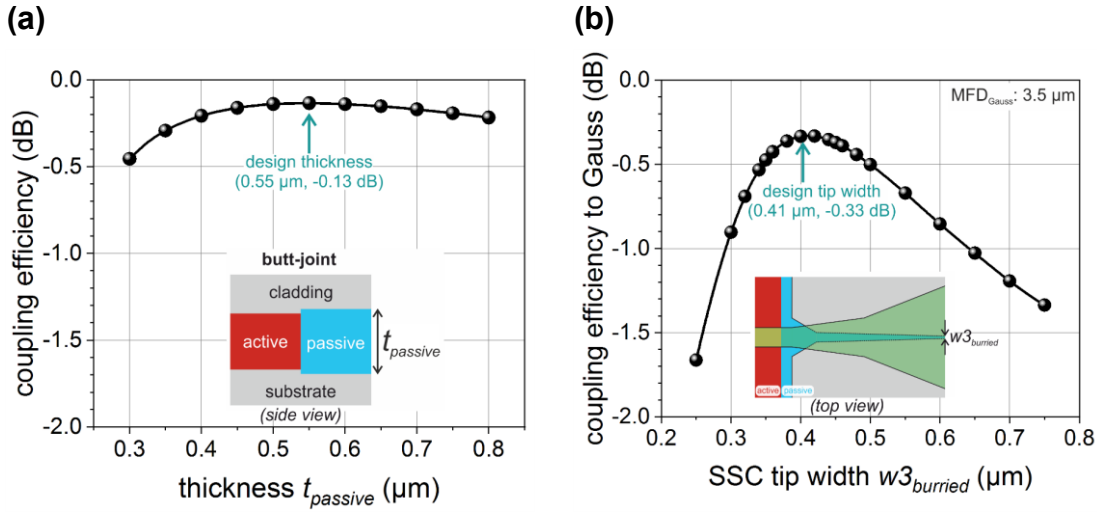


Figure 69: Calculated coupling efficiency of active to passive waveguide mode (a) and SSC tip mode to a Gaussian mode (b) for different waveguide thickness t_{passive} and SSC tip width $w3_{\text{buried}}$, respectively. Simulated with RSoft.

After finding the optimum input and output waveguide structure, the waveguide structure for the transition from input to output is determined. For this, the beam propagation through the SSC was simulated for different variations of the parameters $w1_{\text{buried}}$, $w2_{\text{buried}}$, $L1_{\text{buried}}$, $L2_{\text{buried}}$, $w2_{\text{ridge}}$, $w3_{\text{ridge}}$, $L1_{\text{ridge}}$, $L2_{\text{ridge}}$ in Figure 68 (middle) and the coupling efficiency to a 3.5 μm large Gaussian after propagation was calculated. The optimization process was focused on achieving high coupling efficiency with high fabrication tolerance at minimal SSC length. This extensive process will not be shown here in full detail but an example of a critical aspect of the SSC optimization is given. Figure 70 (a, black diamonds) shows the calculated coupling efficiency with the SSC design optimized for highest coupling efficiency. Although the coupling efficiency at the targeted waveguide width (w_{buried} error = 0) is high, it is intolerant to fabrication errors towards small waveguide widths. By increasing the waveguide width $w2_{\text{buried}}$ from 0.9 μm to 1.7 μm , the coupling efficiency at the target waveguide width is slightly decreased by about 0.1 dB, but the fabrication tolerance towards small waveguide widths is significantly enhanced (Figure 70 (a, blue circles)). Based on the simulation results, the expected total coupling efficiency of the SSC to a 3.5 μm large Gaussian mode is -0.67 dB assuming no waveguide width error. The total coupling efficiency comprises of -0.13 dB for the butt-joint and -0.54 dB for the propagation through the SSC with subsequent coupling to the Gaussian mode. For the simulation, perfectly smooth waveguides without optical material absorption were assumed. The real coupling efficiency is expected to be a bit lower.

Another critical aspect regarding fabrication tolerance of the SSC is lithographic misalignment. As it is not possible to structure the ridge waveguide and the buried waveguide

with the same lithography, there will be some alignment error between the two lithographies. Figure 70 (b) shows the calculated coupling efficiency for different lithographic alignment errors. The SSC design proves to be sufficiently tolerant to misalignment with a drop of coupling efficiency by less than 0.2 dB for alignment errors up to 0.3 μm , which is expected to be within the alignment accuracy of the fabrication process.

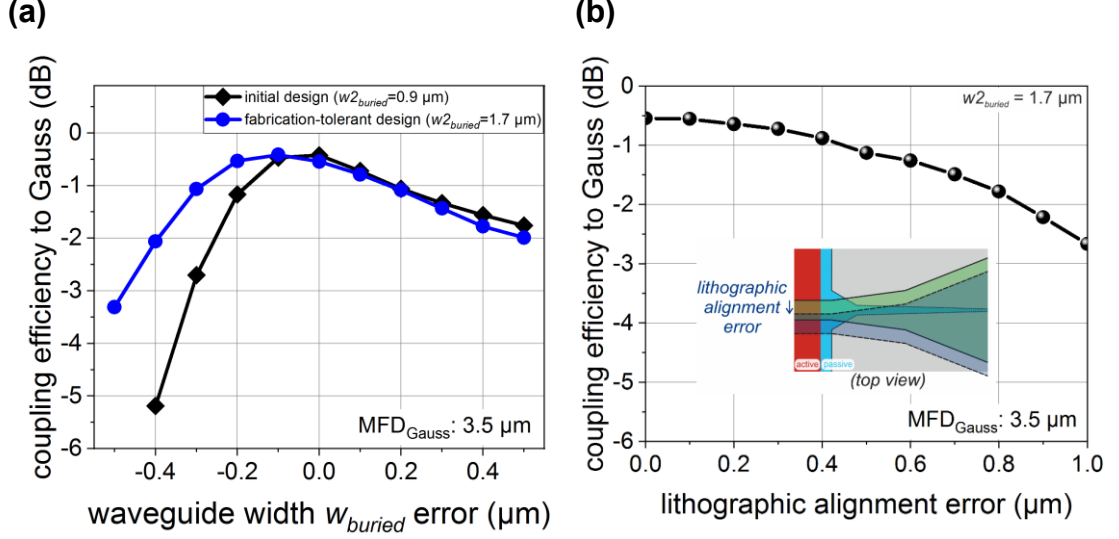


Figure 70: Calculated coupling efficiency to Gaussian mode after propagation through passive SSC section, for different waveguide width error (a) and mask alignment error (b). The waveguide width w_{buried} error corresponds to an equal deviation of $w_{1,buried}$, $w_{2,buried}$, and $w_{3,buried}$ from their target values. Simulated with RSoft.

4.1.3 SiN TriPlex Multiplexer

Figure 71 shows a photograph (left) and a schematic (right) of the SiN TriPlex multiplexer chip with hybridly integrated III-V EML array. The EML array is flip-chip bonded into an etched recess on SiN TriPlex with the same fundamental design as used for the III-V DFB and gain chip integration described in section 3.2.2. The etched recess comprises mechanical alignment stops for passive vertical alignment and gold metalized bonding pads for the electrical and mechanical connection to the EML array. For each EML in the array, there are three separate bonding pads for the ground-signal-ground contacts of the EAM and a large L-shaped bonding pad that connects both the DFB and SOA section. That way, a single current source is sufficient to drive the DFB and SOA sections for each EML. The SiN TriPlex multiplexer comprises multiple Mach-Zehnder interferometers (MZIs) with different arm length differences ΔL (c.f. Figure 71 (right)). The Mach-Zehnder interferometers are designed with directional couplers with 50:50 splitting ratio and heating electrodes at one arm of each MZI. MZI#2 has symmetrical arm lengths and functions as a crossing (i.e. the bottom input of MZI#2 couples to the top output of MZI#2 and the top

input to the bottom output). MZI#1 and MZI#3 have asymmetric arms with an arm length difference of ΔL that results in a periodic transmission spectrum with a free spectral range (FSR) equal to four times the channel distance (i.e. $3200 \text{ GHz} \triangleq \sim 18 \text{ nm}$). That way channel λ_1 is combined with λ_3 and λ_2 is combined with λ_4 to a single output of MZI#1 and MZI#3, respectively. The combined outputs are guided to MZI#4, which has a transmission spectrum with an FSR of two times the channel distance (i.e. $1600 \text{ GHz} \triangleq \sim 9 \text{ nm}$) to combine all wavelength channels to a single output (output#2 or output#3). The electrical heaters of the MZI allow phase tuning of more than 2π and thus the transmission spectra of the MZI can be shifted by a full FSR. The SiN waveguides at the EML to SiN interface comprise integrated SSCs for mode matching to a Gaussian mode with MFD of $3.5 \mu\text{m}$. The output waveguides (output#1 to #4) have SSCs for mode matching to cleaved standard single-mode fiber (MFD $\sim 9.2 \mu\text{m}$).

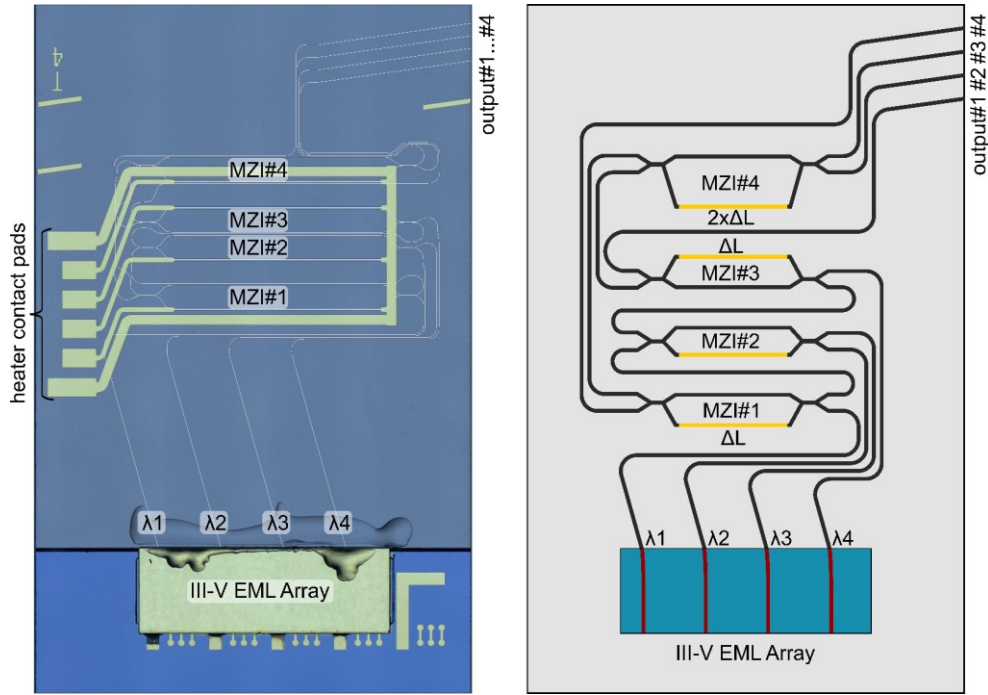


Figure 71: Photograph with SiN waveguides highlighted in white (left) and schematic (right) of SiN TriPleX multiplexer PIC with flip-chip integrated III-V EML array and applied index matching glue. The multiplexer PIC comprises four Mach-Zehnder interferometers (MZI#1 to #4) with different asymmetries in arm length (ΔL). The yellow lines in the schematic (right) indicate electronic heaters for phase tuning. Chip dimensions are $4.5 \text{ mm} \times 7 \text{ mm}$.

4.2 Experimental Characterization

In this section, the EML array for flip-chip hybrid integration is experimentally investigated. First, the performance of the different wavelength channels is evaluated. Next, the coupling

efficiency of the integrated spot-size converter is measured. Finally, the EML array is hybridly flip-chip integrated to the SiN TriPleX multiplexer PIC.

4.2.1 Wavelength Channel Performance

The EML array for flip-chip hybrid integration comprises four wavelength channels in the O-band with a targeted wavelength span of 13.6 nm. With the identical active layer approach (c.f. Figure 3 (a)) used here, the wide wavelength range requires the EML at longer wavelengths to operate at a high detuning to the gain maximum. For the EML array demonstrated here, the two EMLs with shorter wavelengths (EML- λ_1 , EML- λ_2) exhibit a threshold current below 65 mA with comparable optical output power exceeding 35 mW at 40 mA SOA current (c.f. Figure 72 (a)). The two EMLs with longer wavelengths (EML- λ_3 , EML- λ_4) show significantly higher threshold currents and lower maximum output power. For EML- λ_4 , the DFB threshold current is 119 mA and the maximum output power is 13 mW at 40 mA SOA current. Such a large difference in performance indicates that, for the given wavelength span, the difference in detuning is too high and the identical epitaxial layer design is at its limit. The performance could be slightly improved by choosing an epitaxial design with a gain maximum at a longer wavelength. However, this approach is limited because it also leads to an increased EAM insertion loss for the shorter wavelength channels. In Figure 72 (a) the influence of insertion loss on the shortest wavelength channel is visible in the decrease of slope efficiency for EML- λ_1 compared to EML- λ_2 . Overall, the EML array demonstrated here proves functional, but an alternative epitaxial design is recommended if a wider wavelength range or a higher uniformity of the output power levels are desired. With a more complex epitaxial design (e.g. Figure 3 (c)-(f)), the gain and absorption maxima for the DFB/SOA and EAM sections could be adjusted individually.

In order to compensate for the typically lower extinction ratio at long wavelength channels, the EAM length is varied from 80 μm to 110 μm over the array. The experimental results show that the chosen EAM lengths allow for a static extinction ratio exceeding 5.5 dB/V with less than 1.5 dB/V variation over the full array (c.f. Figure 72 (b)). The operation point bias voltage of the array varies from -0.8 V to -1.6 V for the shortest (EML- λ_1) to the longest (EML- λ_2) wavelength channel (c.f. Figure 72 (b)), respectively. This is as expected and correlates to the wavelength detuning of each EML.

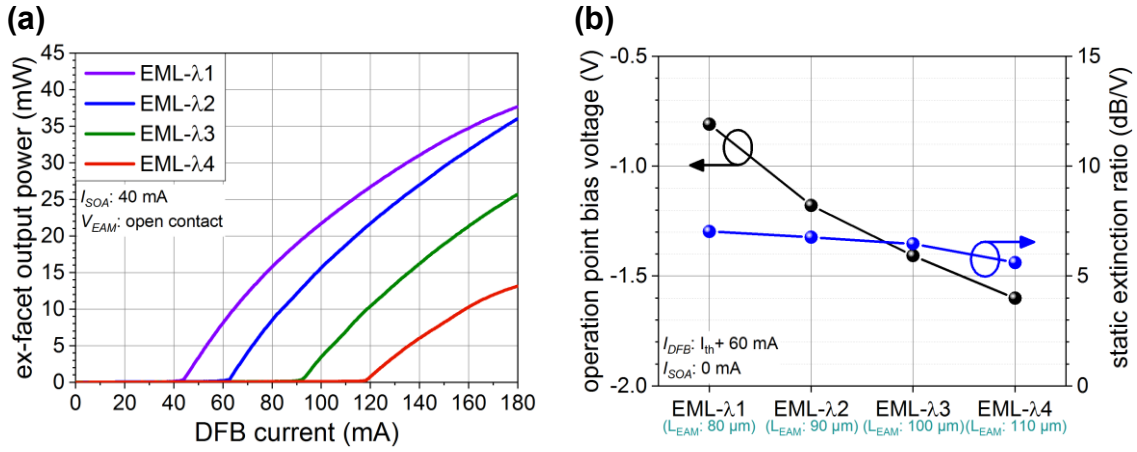


Figure 72: Measured cw ex-facet output power versus DFB current (a), operation point bias voltage and corresponding static extinction ratio at operation point (b) of the EML array for hybrid integration. Chips mounted p-side up on diamond heatsink. $T = 45$ °C.

When the EAM length is varied to equalize the extinction ratio, one has to consider that the EAM capacitance increases with EAM length (c.f. equation (36)). Accordingly, a balance between extinction ratio and modulation bandwidth has to be found. Figure 73 shows the measured frequency response and reflection coefficient at the operation point bias for each EML in the array. For each EML, the frequency response and reflection coefficient are simultaneously fitted with (34) and (12), respectively, using a Levenberg-Marquardt algorithm with parameters shared for both fitting functions. Due to the increasing EAM length, the EAM capacitance increases from 165 fF to 186 fF for EML-λ1 to EML-λ4 (c.f. Figure 73). It is interesting to see that the capacitance increases much less than the proportional increase of the EAM length would suggest according to (36). This can be explained by a reduced capacitance per unit length for the EMLs with longer wavelengths. The EMLs with longer wavelengths have a higher operation point voltage (c.f. Figure 72 (b)), which leads to a reduced carrier pileup and an increased space charge region. Together with the fact that the longer EAM exhibit a reduced series resistance, results in a near identical 3dB bandwidth around 35 GHz for all four wavelength channels in the array (c.f. Figure 73). The frequency response curves in Figure 73 show a slight influence of optical feedback in the form of a local maximum/minimum around 5 GHz. This can be attributed to a reflection on the EML arrays front facet because the measurement was carried out in air and the front facet is anti-reflection coated against index matching glue.

To conclude, using different EAM lengths according to the different detunings in the identical epitaxial layer design is an effective method for achieving equal extinction ratio and modulation bandwidth for wavelength channels that span over 13.6 nm. With regard to

the lasing threshold and optical output power, an epitaxial layer design that allows individual adjustment of the bandgap is recommended.

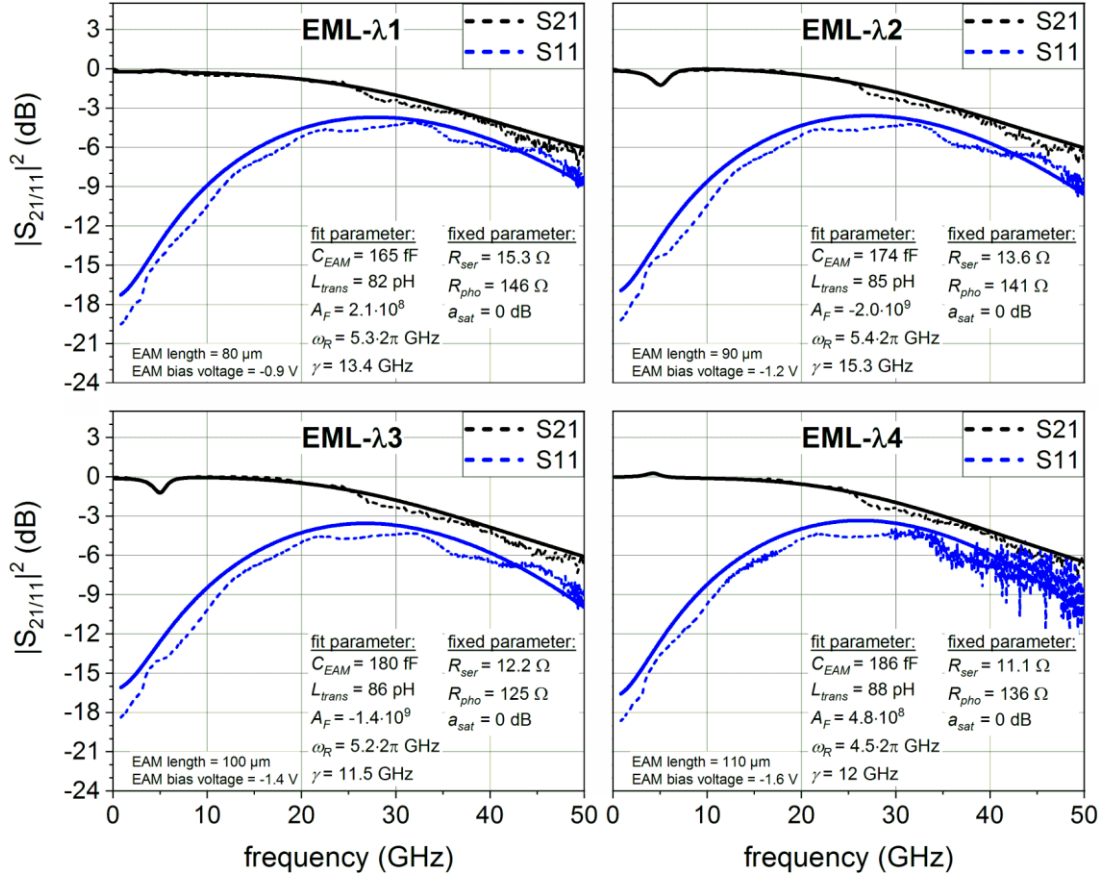


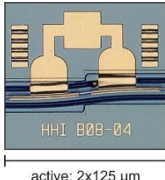
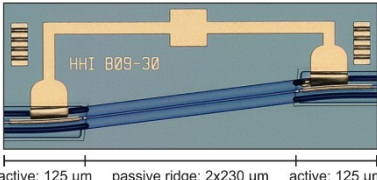
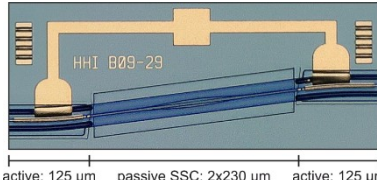
Figure 73: Measured (dashed lines) and fitted (solid lines) frequency response (black lines) and electrical reflection coefficient (blue lines) of the EML array for hybrid integration. Functions (34) and (12) were used as fitting functions with shared fitting parameters. Additional fixed parameters are given in Table 5 of Appendix 1. Chips mounted p-side up on diamond heatsink. $I_{DFB} = I_{th} + 60$ mA, $I_{SOA} = 0$ mA, $T = 45$ °C.

4.2.2 Spot Size Converter

To evaluate the optical losses from the propagation through the SSC of the EML array, special Fabry-Pérot type test structures were fabricated and the internal optical loss was measured (c.f. Table 3). The first test structure is a simple Fabry-Pérot laser with a single active waveguide that has the same geometry as the SOA section of the EML array (c.f. Table 3 (simple)). The second test structure comprises the same waveguide section as the “simple” structure but with a passive waveguide section with twice the SSC length (2×230 μm) integrated between two active sections (c.f. Table 3 (butt-joint & ridge)). The passive section has the same ridge waveguide structure as the active section. The measured internal loss for the “butt-joint & ridge” type is 0.9 dB higher than for the “simple” structure. Half of that (0.45 dB) corresponds to the loss at a single active to passive butt-joint interface and the

scattering and absorption loss from propagation through 230 μm of passive ridge waveguide. The third test structure is the same as the second test structure but the passive section comprises two full SSCs identical to the ones integrated to the EML array (c.f. Table 3 (butt-joint & SSC)). As such, the passive waveguide transforms over the total length from a ridge waveguide type to a buried waveguide type and vice versa. The internal loss compared to the “butt-joint & ridge” structure is 0.1 dB higher, which corresponds to additional loss from the waveguide transformation. Half of this (0.05 dB) corresponds to the loss from waveguide transformation for a single SSC. Such low loss indicates that the waveguide transformation is adiabatic and that the lithographic misalignment between the ridge and the buried waveguide is very low. In total, the measured loss of a single SSC is 0.5 dB. This includes the losses from the active to passive butt-joint interface and propagation losses through the SSC.

Table 3: Fabry-Pérot type test structures and corresponding internal optical loss. The internal optical loss was calculated by measurement of the external quantum efficiency for different device lengths as described in [83]. Different device lengths were achieved by cleaving of double-bars (2 x total device length) and single-bars (1 x total device length). A facet reflectivity of $R = 0.28$ is assumed.

Type	simple	Butt-joint & ridge	Butt-joint & SSC
Layout			
Internal Loss	2.4 dB	3.3 dB	3.4 dB

To evaluate the SSC coupling efficiency to the targeted 3.5 μm large Gaussian mode, the coupling efficiency to a lensed single-mode fiber with a nominal spot size of 3.5 μm was measured for EML arrays with integrated SSCs (c.f. Figure 74). For lensed single-mode fibers, a near Gaussian mode field can be assumed [84]. The SSCs were fabricated with deliberate offsets to the buried waveguide widths w_{buried} from -0.2 μm to +0.2 μm . The highest coupling efficiency of -1 dB is achieved for a waveguide width offset of 0 μm . This indicates that the fabricated waveguide width is very close to the target width. Together with the 0.5 dB of butt-joint and propagation loss measured with the Fabry-Pérot test structures, the total SSC coupling efficiency to the lensed fiber is -1.5 dB. This is about 1 dB higher than estimated from the simulation (c.f. Figure 70 (a)), which can be attributed to a combination of fabrication inaccuracy, scattering and absorption losses, and a non-Gaussian shape of the lensed fiber mode. The measured values in Figure 74 show slightly less fabrication tolerance regarding the waveguide width w_{buried} than estimated from simulation

(c.f. Figure 70 (a)). The qualitative behavior is similar to the simulation with higher fabrication tolerance towards larger waveguide widths. Overall, the results in Figure 74 indicate that the optical mode for zero waveguide width offset is closely matched to the targeted Gaussian mode with an MFD of 3.5 μm .

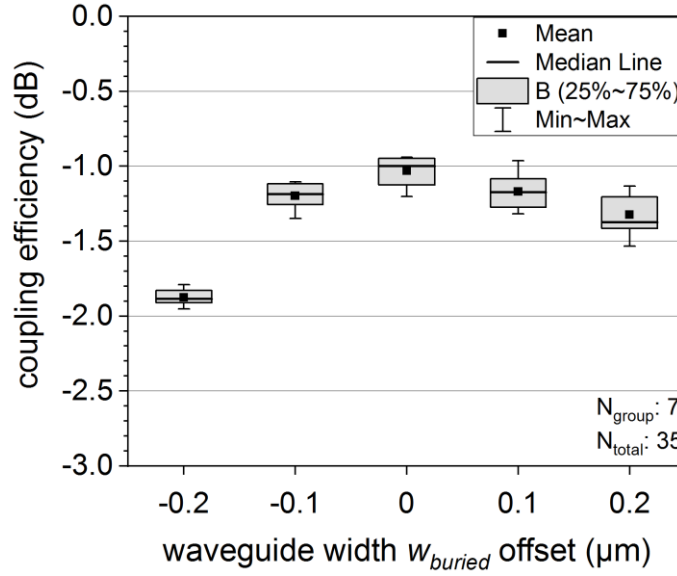


Figure 74: Measured coupling efficiency of EML array devices for hybrid integration coupled to lensed single-mode fiber with a nominal spot size of 3.5 μm . Coupling efficiency was calculated by comparing the optical power coupled to the lensed fiber with the power measured with an integrating sphere.

4.2.3 Hybrid Integration

The first experiments for hybrid integration of EML arrays were carried out using classical alignment with AuSn soldering (c.f. section 3.3.2). Unfortunately, the AuSn method proved unsuccessful due to multiple bonding pads exhibiting open contacts after the soldering process. This can be attributed to the irregular quality of the AuSn solder process (c.f. Figure 56(b)). The use of a nitrogen atmosphere to mitigate oxidization yielded no significant improvement. Further development of the AuSn soldering process is required for it to be suitable for EML array integration.

With the OBR alignment method with gold sinter paste bonding (c.f. section 3.3.2), it was possible to integrate full EML arrays with electrical and mechanical connections for all DFB and SOA contacts. The EAM contacts could not be successfully connected due to short circuits between the EAMs ground-signal-ground contacts. The gold sinter paste was applied with a 5 μm large needlepoint, which did not allow to dispense the material in amounts that were reproducibly small enough to prevent overspilling to adjacent contacts when the chips

were put into contact. In the future, this issue could be addressed by designing the contact pad layout with more tolerance for overspill or by implementing mechanical barriers (e.g. with an extra BCB layer). The optical alignment was carried out similar to the DFB array integration described in section 3.3.2, by aligning a single device in the array using the OBR alignment method (c.f. Figure 75). For the theoretical curve (c.f. Figure 75 (blue line)), a fixed horizontal MFD of $3.5\ \mu\text{m}$ is assumed for the EML array based on the results in Figure 74. The horizontal MFD of the SiN TriPleX facet is set to $10\ \mu\text{m}$ in Figure 75 for the best fit to the measurement. Such a large difference to the target of $3.5\ \mu\text{m}$ is unexpected and cannot be explained by usual fabrication tolerances. It is assumed that either a fabrication error occurred or that some unnoticed effect leads to the measured curve shown in Figure 75. Assuming the estimated MFD for the SiN TriPleX chip is correct, the large mode field has the benefit of a large alignment tolerance of $3.9\ \mu\text{m}$ (-1dB -tolerance in Figure 75 (blue line)). The downside is that the large mode size mismatch significantly reduces the coupling efficiency. After determining the position for the highest coupling efficiency in air, the EML array is placed with an intentional offset of $d_x = 0.75\ \mu\text{m}$ to achieve the highest coupling efficiency when index matching glue is applied (c.f. Figure 75 (green line)). The bonding process is then carried out as described in section 3.3.2 and index matching glue (Vitalit 1528) is applied to the EML arrays facets.

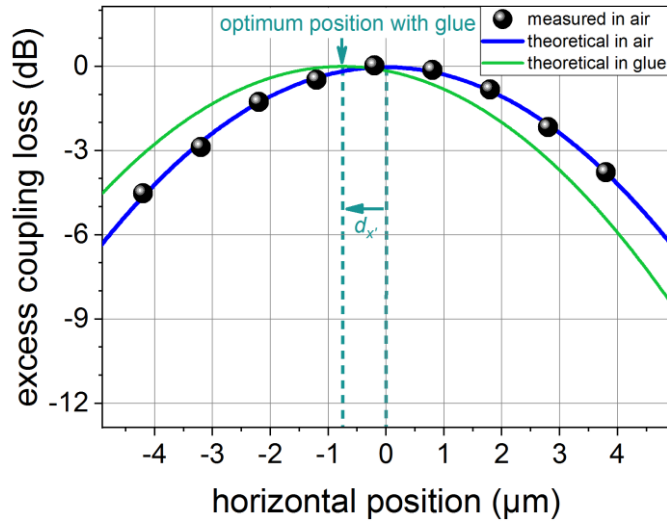


Figure 75: Excess coupling loss versus horizontal position of III-V EML array for hybrid integration to SiN TriPleX multiplexer with OBR alignment. Measurements (circles) are calculated with (43) from the amplitude of a reflection within the EML device. Theory (blue line, green line) is based on Gaussian approximation (38) with horizontal MFDs of $3.5\ \mu\text{m}$ and $10\ \mu\text{m}$ for the EML array and SiN TriPleX chip, respectively. For the theoretical curve in glue (green line) a horizontal misalignment $d_x = 0.75\ \mu\text{m}$, based on (41), is assumed. $d_z = 6\ \mu\text{m}$, $T = 20\ ^\circ\text{C}$.

Figure 76 (a) shows the coupled optical power of an EML array integrated to the SiN TriPleX multiplexer chip with OBR alignment and gold sinter paste bonding. The optical power was measured at all outputs of the SiN TriPleX multiplexer chip (c.f. Figure 71) with an integrating sphere and thus includes the optical losses within the SiN TriPleX chip. As pointed out in section 4.1.3, the SiN TriPleX bonding pads connect the DFB and SOA sections in parallel, and thus a single current is applied for both sections. In consequence, the DFB+SOA threshold currents in Figure 76 (a) are increased compared to the DFB threshold currents in Figure 72 (a). With a current of 180 mA the integrated EML array multiplexer chip achieves an output power of 15 mW for the shortest wavelength channel and 3.5 mW for the longest (c.f. Figure 76 (a)). This is about 3 dB less than the optical power that was measured directly at the facets of comparable EML array structures. The optical loss corresponding to the SiN TriPleX chips is estimated with 0.5 dB, which comprises the waveguide propagation loss and the loss from Fresnel reflection at the SiN StriPleX output facet. This results in an estimated chip-to-chip coupling efficiency of -2.5 dB. Based on the results derived from Figure 75, it is estimated that mode mismatching has the largest contribution to the coupling loss. Increased coupling efficiency is expected by reducing the mode mismatch in the future.

After measuring the total optical power, the spectral characteristic of the device is characterized. For this, a cleaved single-mode fiber is connected with index-matching oil to output #3 in Figure 71. The DFB+SOA currents are set to an equal power level of 3 mW for all wavelength channels (c.f. Figure 76 (a, dashed line)). The electrical heating powers of the Mach-Zehnder interferometers (MZI#1 to #4) are adjusted for highest output power at output #3. The measured optical spectrum shows that the optical modes of the four EMLs in the array are multiplexed onto one waveguide (output#3) with an optical peak power variation of less than 0.1 dB (c.f. Figure 76 (b)). For each mode, a high SMSR exceeding 40 dB is achieved. The four modes are near equidistant with a wavelength spacing close to the target of ~ 4.53 nm (800 GHz). On average, the wavelengths of the modes are about 1.5 nm larger than the targeted LAN WDM grid (target - λ_1 : 1295.56 nm, λ_2 : 1300.05 nm, λ_3 : 1304.58 nm, λ_4 : 1309.14 nm). Based on these measurement results, the DFB grating period can be adjusted in future designs to mitigate the wavelength offset. The total optical power measured in the fiber was 10 mW, which corresponds to a chip-to-fiber coupling efficiency of around -0.8 dB. In this first device generation, the total electrical power that is required for the phase tuning of the SiN-based MZI is 1029 mW. In future designs, phase offsets can be introduced by adjusting the pathlength differences in the MZI arms, which would reduce the required heating power.

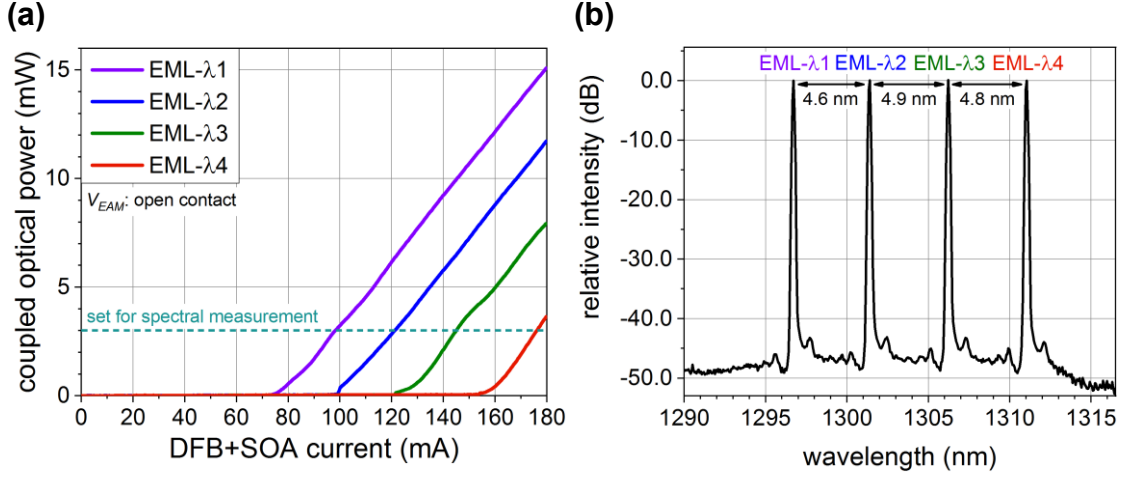


Figure 76: CW optical power versus DFB+SOA current (a) and optical spectrum (b) measured at the output facets of SiN TriPlex multiplexer with hybridly integrated EML array. The optical power (a) is measured with an integrating sphere at all outputs, the spectrum (b) is measured with a cleaved single-mode fiber at output #3 (c.f. Figure 71). (b): $I_{DFB+SOA}$ = 99 mA (EML-λ1), 121 mA (EML-λ2), 146 mA (EML-λ3), 176 mA (EML-λ4); P_{heat} : 445 mW (MZI#1), 188 mW (MZI#2), 220 mW (MZI#3), 176 mW (MZI#4); (a, b): $T = 45^\circ\text{C}$.

5. Conclusion and Outlook

After extensive research on individual semiconductor optical devices, photonic integration offers a way to push technological boundaries further. This thesis provides a particular contribution to this evolution. III-V based EML devices with SOAs as monolithically integrated transmitters with increased output power in single-chip and array variants were presented. A new III-V to SiN TriPlex hybrid integration process with advanced alignment techniques for minimum optical coupling losses was developed.

Targeting current 10 Gbit/s PON applications, a III-V based EML with monolithically integrated SOA for high optical output power at semi-cooled operation (50°C) was presented. The device comprises an identical epitaxial layer design, which keeps fabrication costs low. Based on simulations and experimental results from previously fabricated structures, critical design parameters were identified and an optimized design was generated. An improved SOA output facet design is presented with a more than 20 dB increased optical return loss. The increased optical return loss allows operating the SOA at a higher gain, without risking signal degradation from amplified optical feedback. Devices with the new design were fabricated and experimentally characterized. For the evaluation of the small-signal measurements of the EML with integrated SOAs, a dedicated frequency response function was derived. It comprises a sophisticated equivalent circuit model of the EML and includes the effects of optical feedback and SOA saturation. The fabricated EML with integrated SOA achieved up to 9.5 dBm mean optical output power in the L-band with

a dynamic extinction ratio that exceeded 12 dB at 10 GBd NRZ modulation. This makes it an ideal candidate as a transmitter chip for PON applications [49], [50]. The upwards compatibility of the device was shown by demonstrating up to 56 GBd NRZ operation.

The application of the low-cost identical epitaxial layer design to multiwavelength EML arrays was investigated. It was shown that with the monolithic integration of SOAs and the careful adjustment of the EAM length, an equal performance could be achieved for different wavelength channels spanning over 7.5 nm in the L-band. The integrated SOAs allow adjusting the optical output power of each wavelength channel with negligible influence of electrical heating on the lasing wavelength. By choosing different EAM lengths for the different wavelength channels, a uniform performance on bandwidth and extinction ratio is achieved. The EML array is capable of transmitting an aggregated bitrate of 224 Gbit/s, which was demonstrated for 4 x 56 GBd NRZ and 4 x 28 GBd PAM4 fiber transmission. It was shown that PAM4 can significantly increase the transmission distance (from 2.5 km to 5 km) in the dispersion sensitive L-band. The primary limitation of the current EML array design was that it suffered from optical feedback from the SOAs output facet. In the future, this limitation can be overcome by applying the new SOA output facet design that was developed in this thesis.

For the first time, a wafer-scale compatible process for flip-chip hybrid integration of III-V chips to SiN TriPleX was developed. It comprises mechanical alignment stops with epitaxial accuracy for passive vertical alignment, which simplifies the assembly process and enables array integration with no added complexity compared to single chips. A novel method of utilizing optical backscatter reflectometry for active horizontal alignment was presented. It allows overcoming the electrical contacting limitations of classical active alignment. The hybrid integration of III-V DFB lasers to SiN TriPleX waveguides was demonstrated with an averaged chip-to-chip coupling efficiency of -2.1 dB and good reproducibility. The integrated lasers are capable of delivering a record optical power exceeding 60 mW at 1550 nm coupled to the SiN waveguide and operate up to a temperature of 85 °C. The flip-chip hybrid integration process proves to be suitable for the integration with complex SiN PICs, which was demonstrated by the assembly of a hybrid tunable laser. Furthermore, it was shown that defective PICs could be identified before assembly by analyzing the optical backscatter signal. The hybrid tunable laser consists of a III-V gain chip that is hybridly integrated to a SiN TriPleX external cavity. The assembled device exhibited an estimated chip-to-chip coupling efficiency of -1 dB to -1.5 dB, optical output power up to 60 mW, and full C-band tunability. It is a promising candidate for tunable laser sources in modern communication or sensing applications. To make the presented flip-chip hybrid integration

process suitable for commercial applications, the next step is to implement automation. Modern fully automated die bonders are capable of performing all steps that are required for the assembly process and allow for much higher throughput and reproducibility than what could be achieved here manually. Carried out automatically and on a wafer-scale, the flip-chip hybrid integration process offers a low-cost solution for the fabrication of high-performing hybrid chips.

The findings on EML arrays and hybrid integration were taken one step further by developing a III-V EML array for hybrid integration to a SiN TriPleX multiplexer PIC. The wavelength channels of the EML array span over 13.6 nm in the O-band and are matched to the LAN WDM grid to address the needs of modern Terabit Ethernet applications [82]. It was shown that the concept of adjusting the EAM length to achieve equal bandwidth and extinction ratio for the different wavelength channels works well for the given wavelength range. All channels exhibited a modulation bandwidth around 35 GHz with a static extinction ratio exceeding 5 dB/V. For the optical output power, a significant difference between the wavelength channels was observed, which shows that the identical epitaxial layer design is at its limits. For future EML array designs, which address a similar or wider wavelength range, an epitaxial layer design that allows individual bandgap engineering is recommended. The EML array is designed for flip-chip hybrid integration and comprises fabrication-tolerant spot-size converters for efficient chip-to-chip coupling. The hybrid integration of an EML array to a SiN TriPleX multiplexer chip was demonstrated. All wavelength channels of the array were successfully multiplexed on a single output with a side mode suppression ratio exceeding 40 dB for all channels. With the current design, it was not possible to achieve an electrical connection for the contact pads of the EAM. In the future, this can be addressed by adjusting the pad layout for gold sinter paste bonding or further development of the AuSn soldering process.

This work developed a generic process for flip-chip hybrid integration of III-V components to SiN TriPleX. The fundamental steps of the process are designed to be independent of the type of III-V component that is to be integrated. This allows using the same process for the integration of different types of III-V components on the same SiN TriPleX PIC. By extending the variety of III-V components that are compatible with flip-chip hybrid integration, a hybrid PIC designer would be completely free in choosing the best material system for each component in the PIC. The design freedom could be further increased by applying the process to other photonic platforms such as silicon on insulator or polymer, which could be readily done. By standardizing the process and making it suitable for

automated assembly on a wafer-scale it has the potential to become the standard solution for commercial hybrid integration applications.

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List of Abbreviations

ASE	amplified spontaneous emission
BER	bit error rate
BH	buried heterostructure
CMOS	complementary metal oxide semiconductor
CW	continuous wave
DC	direct current
DML	directly modulated laser
DFB	distributed feedback laser
EAM	electroabsorption modulator
EML	electroabsorption modulated laser

FEC	forward error correction
FIR	finite impulse response
FSR	free spectral range
GSG	ground-signal-ground
HF	high frequency
IC	Integrated circuit
MFD	mode field diameter
MQW	multiple quantum well
MZI	Mach-Zehnder interferometer
OBR	optical backscatter reflectometry
PAM	pulse amplitude modulation
PIC	photonic integrated circuit
PON	passive optical network
QCSE	quantum-confined Stark effect
RF	radio frequency
SAG	selective area growth
SMSR	side mode suppression ratio
SOA	semiconductor optical amplifier
SOI	silicon-on-insulator
SSC	spot size converter

Published Work

Publications with published results of this work

1. **M. Theurer**, M. Moehrle, A. Sigmund, K.-O. Velthaus, R.M. Oldenbeuving, L. Wevers, F.M. Postma, R. Mateman, F. Schreuder, D. Geskus, K. Worhoff, R. Dekker, R.G. Heideman, and M. Schell, “Flip-Chip Integration of InP to SiN Photonic Integrated Circuits,” *J. Lightwave Technol.*, vol. 38, no. 9, pp. 2630–2636, May 2020, doi: 10.1109/JLT.2020.2972065.
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Patents

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Appendix

1. Fitting Parameters

Table 4: Fixed fitting parameters for S21/S11 measurement of high power EML devices. Z_1 , R_{term} and C_{DC} are taken from suppliers spec sheets. C_{probe} and L_{probe} were extracted from S11 measurement on the RF-probe in open circuit and short circuit configuration. C_{pad} and C_{trans} are the calculated capacitances of parallel plate capacitors for the respective pad and transmission line geometries. L_{trans} was extracted from S11 measurements on EAMs contacted with the RF-probe. R_{ser} corresponds to the measured differential resistance of EAMs operated with forward current.

Parameter	Symbol	Value
Source impedance	Z_1	50 Ohm
RF-probe termination resistance	R_{term}	50 Ohm
RF-probe DC blocking capacitance	C_{DC}	10 nF
RF-probe parasitic capacitance	C_{probe}	38 fF
RF-probe inductance	L_{probe}	82 pH
EAM pad capacitance	C_{pad}	32 fF
EAM transmission line capacitance	C_{trans}	37 fF
EAM transmission line inductance	L_{trans}	45 pH
EAM series resistance	R_{ser}	13.2 Ohm

Table 5: Fixed fitting parameters for S21/S11 measurement of EML Array devices. Z_1 , R_{term} and C_{DC} are taken from suppliers spec sheets. C_{probe} and L_{probe} were extracted from S11 measurement on RF-probe in open circuit and short circuit configuration. C_{pad} and C_{trans} are the calculated capacitances of parallel plate capacitors for the respective pad and transmission line geometries. R_{ser} corresponds to the measured differential resistance of EAMs operated with forward current.

Parameter	Symbol	Value
Source impedance	Z_1	50 Ohm
RF-probe termination resistance	R_{term}	50 Ohm
RF-probe DC blocking capacitance	C_{DC}	10 nF
RF-probe parasitic capacitance	C_{probe}	38 fF
RF-probe inductance	L_{probe}	82 pH
EAM pad capacitance	C_{pad}	47 fF
EAM transmission line capacitance	C_{trans}	29 fF

Table 6: VPI transmission-line model parameters used for VPI simulation of integrated SOA.

Parameter	Value
Active region thickness MQW	56 nm
Active region thickness SCH	100 nm
Current injection efficiency	0.9
Internal loss	1500 m^{-1}
Internal loss carrier dependence	$1.5 \cdot 10^{-22} \text{ m}^2$
Confinement factor MQW	0.105
Confinement factor SCH	0.1
Gain coefficient logarithmic	85000 m^{-1}
Nonlinear gain coefficient	$5.17 \cdot 10^{-23} \text{ m}^3$
Nonlinear gain time constant	$5 \cdot 10^{-13} \text{ s}$
Transparency carrier density	$2.35 \cdot 10^{24} \text{ m}^{-3}$
Linear recombination	$1 \cdot 10^8 \text{ s}^{-1}$
Bimolecular recombination	$1 \cdot 10^{-16} \text{ m}^3 \text{ s}^{-1}$
Auger recombination	$4 \cdot 10^{-41} \text{ m}^6 \text{ s}^{-1}$
Carrier capture time constant	$1.54 \cdot 10^{-11} \text{ s}$
Carrier escape time constant	$8 \cdot 10^{-10} \text{ s}$
NoiseCoupling	$1 \cdot 10^{-6}$