A 9-bit, 45mW, 0.05mm^2 Source-Series-Terminated DAC Driver with Echo Canceller in 22nm CMOS for In-Vehicle Communication

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For my parents, maman and baba, who wanted their son to have a Dr. -Ing. title.

Abstract

The increasing amount of data transferring within a vehicle is driven by the expanding applications implemented on it, initiated the use of Ethernet as a new standard within the automotive industry to not only increase the data rate but also take into account the strict constraints within the automotive environment such as robustness and electromagnetic interference, etc.

The introduction of Automotive Ethernet (AE) standards started with 100Base-T1 with a data rate of 100 Mb/s. Later, under the task force IEEE P802.3ch, standards up to the data rate of 10 Gb/s are established. The focus of this work is the study of the physical layer of the transceiver suitable for the AE standards from the data rate of 1 Gb/s to 10 Gb/s. This work presents an SST 9-bit TX-DAC driver, that is fully compliant to the new Automotive Ethernet (AE) Standard IEEE P802.3ch for the data rate up to 10 Gb/s. The TX driver design incorporates a highly-correlated timing-matched 9-bit echo DAC canceler (EC-DAC) to eliminate up-to 24.3dB of the transmit power from the RX path, due to the full-duplex transmission scheme. The TX-EC-DAC driver combination inherently provides 100Ω differential termination and possesses a PVT calibration scheme covering up to 3 sigma process variation with a resolution of 1.5Ω. Designed and fabricated in a 22nm FD-SOI technology, the TX-DAC enables a 1Vppd PAM4 signal swing with raw data rates up to 11.2Gb/s and Nyquist tone sine wave linearity SFDR of better than 50dBc. The driver pair is backward compatible with all relevant AE Standards 10/5/2.5/1GBase-T1 and occupies the smallest area of only $0.05mm^2$. The 9-bit TX-EC-DAC combination dissipates 3/42mW from dual 0.8/1.2V power supply with a power efficiency of 2mW/Gb/s per DAC.

(Keywords: SST driver, TX-DAC, Echo canceling, Automotive Ethernet, NGAUTO, IEEE P802.3ch.)

Abstrakt

Die Erhöhung der Datenmenge, die innerhalb eines Autos übertragen werden, wird durch zunehmend integrierte Anwendungen angetrieben. Dies hat, um nicht nur die Datenrate zu erhöhen, sondern auch die strikten Auflagen innerhalb des Automobils wie Robustheit, elektromagnetische Interferenz usw. zu berücksichtigen, die Verwendung von Ethernet als neuen Standard in der Automobilindustrie eingeleitet.

Die Einführung von Automotive Ethernet (AE) Standards begann mit 100Base-T1 mit einer Datenrate von 100 Mb/s. Anschließend wurden von der Task Force IEEE P802.3ch Standards für Datenraten von bis zu 10 Gb/s festgelegt. Der Schwerpunkt dieser Dissertation liegt auf der Eignungsanalyse der physikalischen Schicht des Transceivers für Datenraten von 1 Gb/s bis zu 10 Gb/s. In dieser Arbeit wird ein AE Standard IEEE P802.3ch kompatibler 9-Bit TX-DAC Treiber für Datenraten von bis zu 10 Gb/s vorgestellt. Das Design des TX Treibers beinhaltet einen hoch-korrelierten zeitlich-angepassten 9-Bit Echo-DAC-Unterdrücker (EU-DAC) der aufgrund des Vollduplexübertragungsschema bis zu 24.3dB von der Sendeleistung aus dem Empfangspfad eliminiert. Die TX-EU-DAC Treiberkombination hat eine 100Ω differenzielle Terminierung und beinhaltet ein Kalibrierungsschema das bis zu 3 Sigma Prozessvariationen mit einer Auflösung von 1.5Ω abdeckt. Entworfen und gefertigt wurde der TX-DAC in einer 22nm FD-SOI Technologie und ermöglicht einen 1Vppd PAM4 Signalpegel mit einer Rohdatenrate von bis zu 11.2Gb/s und einer Nyquist Sinuswellentonlinearität von besser als 50dBc. Das Treiberpaar ist abwärtskompatibel mit allen relevanten AE Standards 0/5/2.5/1GBase-T1 und benötigt eine Fläche von nur $0.05mm^2$. Die 9-bit TX-EC-DAC Kombination verbraucht 3/42mW von einer doppelten 0.8/1.2V Spannungsquelle mit einer Energieeffizienz von 2mW/Gb/s pro DAC.

List of Own Publications

[1] **Hossein Ghafarian** and Friedel Gerfers. **A digital calibration technique canceling non-linear switch and package impedance effects of a 1.6 GS/s TX-DAC in 28 nm CMOS**. In *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–4. IEEE, 2017.

[2] **Hossein Ghafarian** and Friedel Gerfers. **Analysis and compensation technique canceling non-linear switch and package impedance effects of a 3.2 GS/s TX-DAC**. In *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 1172–1175. IEEE, 2017.

[3] Helia Ordouei, **Hossein Ghafarian**, and Friedel Gerfers. **Analysis of package impedance effects on the linearity of source series terminated DACs**. In *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 250–253. IEEE, 2018.

[4] **Hossein Ghafarian**, Helia Ordouei, and Friedel Gerfers. **Impedance calibration technique canceling process and temperature variation in source terminated DAC Drivers in 22nm FDSOI**. In *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 113–116. IEEE, 2019.

[5] Friedel Gerfers, Nima Lotfi, Enne Wittenhagen, **Hossein Ghafarian**, Yuan Tian, and Marcel Runge. **Body-Bias techniques in CMOS 22FDX® for mixed-signal circuits and systems**. In *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pages 466–469. IEEE, 2019.

[6] Enne Wittenhagen, Marcel Runge, Nima Lotfi, **Hossein Ghafarian**, Yuan Tian, and Friedel Gerfers. **Advanced mixed signal concepts exploiting the strong body-bias rffect in CMOS 22FDX**. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 68(1), 2021.

[7] **Hossein Ghafarian**, Suhas Shivaprakash, Sanaz Mortazavi, Philipp Scholz, Nima Lotfi, and Friedel Gerfers. **A 9-bit, 45mW, 0.05mm2 source-series-terminated DAC driver with echo canceller in 22nm CMOS for in-vehicle communication**. *IEEE Solid-State Circuits Letters*, 2021.

Contents

1 Introduction

The amount of data transferred has greatly increased with the development of the Internet of Things (IoT) and connectivity between different devices and sub-components. The automotive industry has also evolved with the same rate, adding new features and applications such as driver assisting to self-driving cars and car as a node in a network which uses dozens of sensors around the car [1]. The data from these sensors need to be transferred to the Central Unit (CU) to process and further actuate the target components in the car. In order to transfer the data, various networking technologies such as Controller Area Network (CAN), Local Interconnect Network (LIN), Media Oriented Systems Transport (MOST), FlexRay, etc., have been developed. However, the data throughput of the aforementioned automotive standards is not sufficient for the amount of data being transferred today [2]. Therefore, Ethernet protocol, considered a well-established networking technology, was introduced to the automotive industry to meet the need for a higher data transmission speed.

The automotive industry has successfully introduced 100 Mb/s Ethernet for in-vehicle networks (IVN). The standard IEEE 802.3ch comprises a highly integrated full-duplex multi-speed (1/2.5/5 and 10Gbit/s) IVN PHY+MAC, which needs to meet stringent functional safety requirements (ISO 26262, ASIL- B, etc.) [3].

Realizing Ethernet in the automotive environment requires designing the Physical layer (PHY) to comply with the strict automotive environment standards and focus on different priorities such as power consumption and area in the design, compared to the conventional Ethernet transceivers used in commercial computers. PHY consists of two main components: Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA), which divide the digital and analog signal processing domains, respectively.

The PMA prepares the signal to be transmitted on the channel via the transmitter, as well as receiving the signal to be decoded for the PCS. The focus of this work is on the analog functionality component of the PHY, presenting the design and implementation of the transmitter within the PMA to comply with the aforementioned Automotive Ethernet (AE) standards.

State-of-the-art of Ethernet transceivers often drives the twisted-pair line (STP/UTP) (shielded/unshielded) directly using a high resolution transmit Digital to Analog Converter (TX-DAC) driver enabling spectral shaping and equalization. TX drivers dissipate most of the power within an Ethernet PHY as they drive the 100 Ω line. Therefore a power-efficient driver implementation is of prime interest. Furthermore, the TX-DAC resolution should not

only enable the minimum modulation level of PAM4, defined by MultiGBase-T1 standard [4], but also gives the transmitter an extra headroom to perform pre-equalization and power spectrum output shaping.

Given the full-duplex operation, the transmit signal is in the transceiver with the received signal. In order to decode the received signal, the transmit signal power should be subtracted, requiring the implementation of a hybrid solution. Therefore, a transmitter solution satisfying these requirements is one of the main challenges within the PHY implementation, becoming the main focus of this work.

In order to provide a better understanding of the current state of the automotive industry and the requirements set for the Ethernet networking technology, especially the requirements related to the transmitter, the second chapter explains a brief history of networking technologies within the automotive industry. It also presents the requirements of interest on different components of a complying Automotive Ethernet PHY for MultiGBase-T1 (2.5 Gb/s, 5 Gb/s and 10 Gb/s) standards.

The third chapter presents a detailed discussion on the available high-speed Digital-to-Analog Converters (DACs), which can be used for the PHY transmitter. First, to analyze the DACs, some of the static and dynamic properties of the DAC performance is introduced. Next, the two main DAC implementations for the target application, named current-mode DAC and voltage-mode DAC, are introduced. Then, the performance of the DACs is compared in detail to decide on the most optimum solution for the target application.After the analysis, the Source Series Terminated (SST) DAC was found to be the optimum choice to be implemented. The architecture of the proposed SST DAC is studied in detail by highlighting the challenges limiting the performance of the proposed DAC, and possible solutions are presented.

In the fourth chapter, the detailed design of the 9-bit SST DAC operating at 5.6 GS/s is shown. The solutions presented in the third chapter for each of the challenges are utilized and are calculated to fit for the target design. Moreover, simulation results are presented to characterize the DAC meeting the required performance.

The fifth chapter addresses both the characterization setup as well as measurement results to verify the compliance of the proposed TX-DAC to the requirements set by the AE standards.

Finally, a design summary including a state-of-the-art SST driver comparison is presented with the conclusion, in the final chapter.

2 Automotive Ethernet

In this chapter, a brief history of the automotive industry's data communication standards is introduced, highlighting the Ethernet standard family. The general architecture of the physical layer within an Ethernet transceiver is introduced and with a detailed study of the requirements and characteristics of parts highlighted in this work.

2.1 Brief History of In-car Networking Standards Within Automotive Industry

The need for in-car networking started by introducing sensors and actuators in the car. Automotive manufacturers, however, started developing different standards to enable data communication within the car. The introduction of different standards brought the disadvantage of smaller volumes for the semiconductor vendors, which in turn increases the product's price for each of these solutions.

As time goes by the automotive industry started converging, and today, there is still a variety of networking technologies in use. The main technologies mostly used in cars these days are briefly introduced here and compared with each other in terms of data rate, robustness, and target use case.

2.1.1 Controller Area Network (CAN)

CAN is a bus system in which all Electronic Control Units (ECUs) are connected and share the same wiring, as shown in Fig. 2.1. The decision in which the ECU gets access to the medium is based on the priority level of the message transmitted by the ECU. Nowadays, two different CAN versions are integrated into cars: the High-Speed CAN, used for data rates up to 1 Mbps (HS CAN), and Low-Speed CAN (LS CAN), used for data rates up to 125 kbps. The CAN technology uses Unshielded Twisted Pair (UTP) cables and is a robust choice that allows ECUs in almost all areas of a car to be connected.

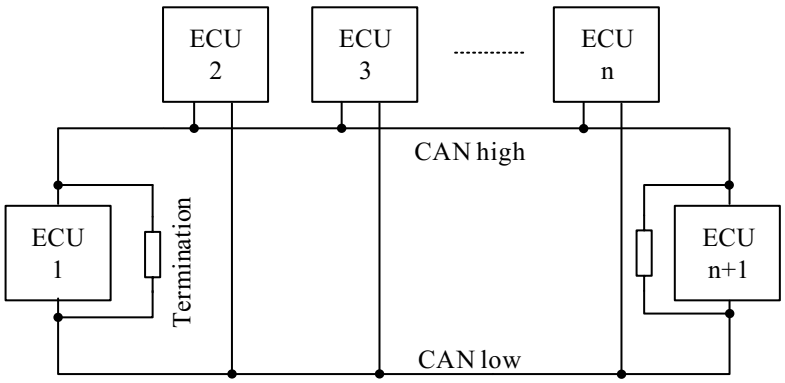


Figure 2.1: Typical CAN network diagram.

2.1.2 Local Interconnect Network (LIN)

LIN is a cost-efficient solution used for cost-sensitive applications and has few requirements such as basic control of power windows, central locks, etc. LIN is designed as a single-ended, i.e., 1-wire, a system with simple hardware for the transceiver. Single-ended signaling limits immunity and increases emission. Therefore to meet the Electro-Magnetic Compatibility (EMC) requirements, the maximum data rate is limited to 19.2 kbps. An example of a LIN network is depicted in Fig. 2.2 shows up to 16 ECUs sharing the bus, and the Master-Slave concept governs the channel access.

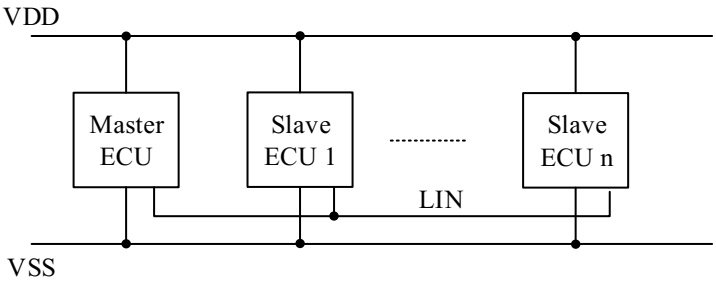


Figure 2.2: Typical LIN network diagram.

2.1.3 Media Oriented Systems Transport (MOST)

MOST protocol is the response of the automotive industry with the demand to increase the data rate. Using the optical fibers as the medium was the choice to promise the expected

data rate with an EMC compliant solution at a reasonable cost. The MOST protocol is more complicated than the aforementioned CAN or LIN. MOST uses a ring topology as shown in Fig. 2.3 which can handle up to 64 ECUs. The maximum data rate of 13.8 Mbps is possible with this protocol with a unidirectional communication on the fiber.

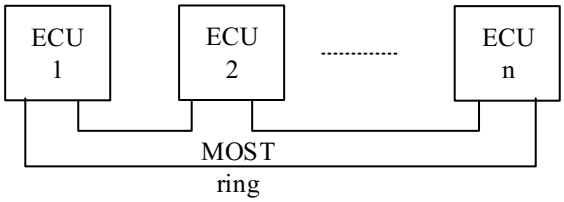


Figure 2.3: Typical MOST network ring.

2.1.4 FlexRay

The FlexRay protocol was developed for X-by-Wire applications, eliminating all mechanical fallbacks from the car and having pure electric functions. The key requirements of FlexRay are reliability, determinism, and redundancy, while the gross data rate of FlexRay is 10 Mbps. FlexRay transmits a differential signal on UTP. A small FlexRay system consists of four to five ECUs with linear topology, and with the use of an "active star/star coupler", it is possible to combine several linear topologies in one network as shown in Fig. 2.4 [5].

2.1.5 Automotive Ethernet

Several factors resulted in the introduction of yet another technology: Ethernet for the in-car networking technologies. The most important factor is the increase in the demand for higher data rates [6]. With the trend that the automotive industry is heading, data-driven applications have been added to the car, such as driver assistants, cameras, infotainment systems, etc. Each of these technologies has been provided by one of the previously introduced in-car networking technologies. However, the data rates become the limit and adapting these technologies for higher data rates increases costs. Moreover, various technologies connected through a central gateway to update the software become a challenge as the time it takes to update the software can reach a day due to the low data rate [5].

As a well-established networking standard, Ethernet was the most suitable option to be adapted to be used within in-car networking. The technology provides a sufficient data rate, available in computers and laptops, cost-efficient, and networking technology that enables the idea of handling the car as a node in a larger network. Moreover, a unified network provides convergence of automotive functions with user interface technologies and creates an economy of scale to have a single technology across the industry. Replacing also

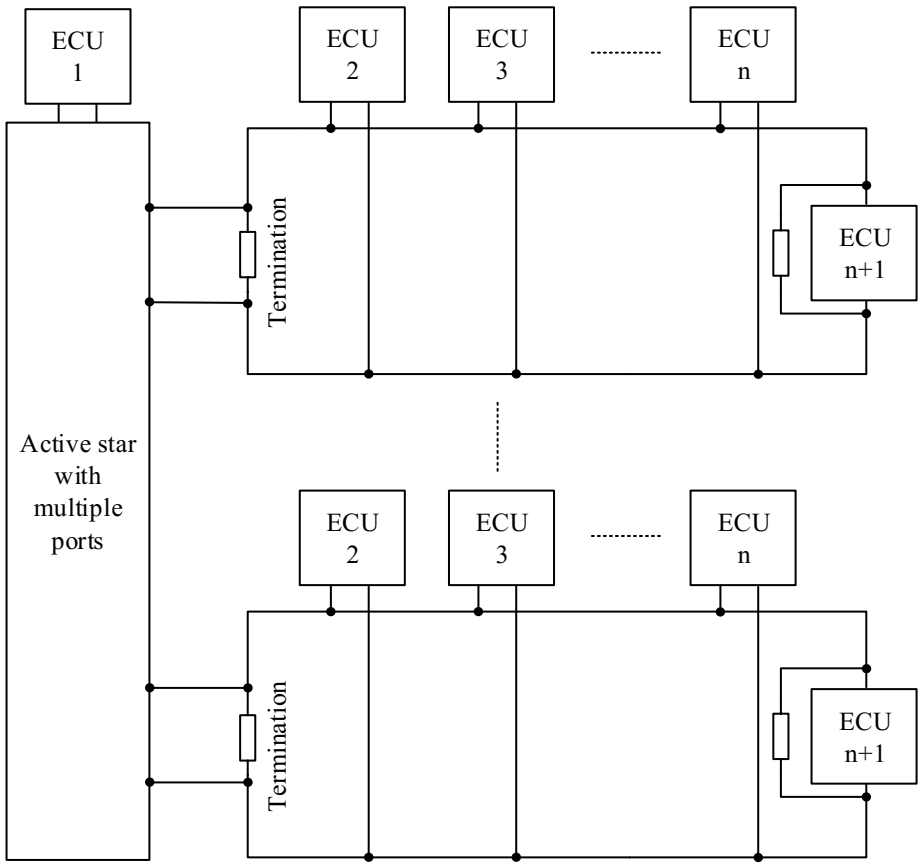


Figure 2.4: Typical large FlexRay network diagram with active star.

previously introduced technologies with a single high-speed protocol enhances the flexibility and scalability of in-car networks. Fig. 2.5 shows the use cases where Ethernet can be implemented and replace the older technologies to create a single unified technology across the car.

Ethernet communications are made with differential signaling, improving the robustness and enabling intelligent modulation and filtering on the data. The Automotive Ethernet was introduced with the data rate of 100 Mb/s and the further scaling of this technology to higher data rates is taken by the Institute of Electrical and Electronics Engineer (IEEE).

2.1.6 Comparison of In-car Standards and Outlook

The comparison of the introduced in-car networking technologies is shown in Table. 2.1 in terms of data rate, robustness and target use. Fig. 2.6 shows the timing diagram regarding when each of the technologies is introduced and comparing the data rate of them together.

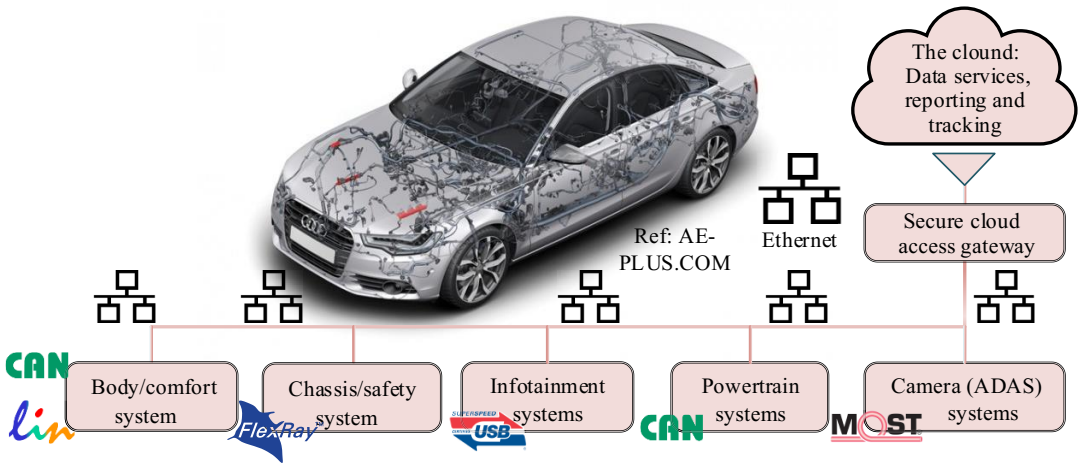


Figure 2.5: Showing the current in-car networking technologies with their use case in a car and how Ethernet can replace these standards by the ruse of a single technology across the car.

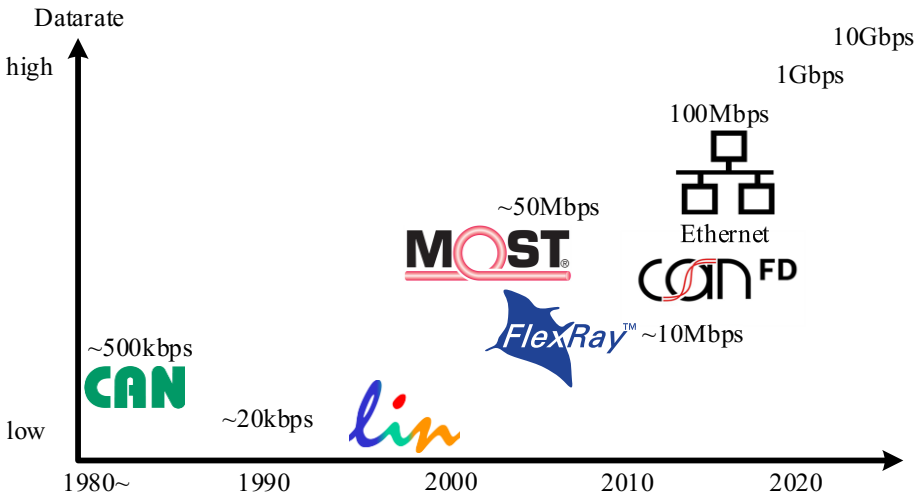


Figure 2.6: Time diagram showing the introduction of the in-car networking standards and comparing the data rate of the technologies.

2.2 IEEE803.2 Ethernet Standard Family

IEEE802.3 is a working group within IEEE that defines the Physical Layer (PHY) and data link layer's Media Access Control (MAC) of wired Ethernet.

Automotive Ethernet for 100 Mb/s, once introduced by Broadcom Inc. as the name of BroadR-Reach, was moved to the IEEE standardization working group. This change was

Technology	Data rate	Robustness	Target use
CAN	500 kbps	Differential signalling	Robust ECU control
LIN	19.2 kbps	Small data rate	Low cost control
MOST	<25,50,150 Mbps shared	Optical medium	Complex, high-end audio
FlexRay	< 10 Mbps shared	Differential signalling	X-by-Wire
Ethernet	0.1,1,2.5,5,10 Gbps	Differential signalling	High data rates

Table 2.1: Comparison of discussed in-car networking technologies [5].

made to make this technology open to all vendors, which remove the monopoly of one company providing the technology and favoring the customer to have a better price [5].

2.2.1 100Base-T1,1000Base-T1 and NGAUTO Standards

100BASE-T1, which stands for Automotive Ethernet standard with a data rate of 100 Mb/s over a single unshielded twisted pair, was the first series of the Ethernet standards for in-car networking approved in 2015 [6]. But, with the ever-growing amount of data being transferred within a car, a higher data rate was soon in the standardization process and approved by 2016 to enable 1 Gb/s over a single unshielded twisted pair named as 1000BASE-T1.

Quickly, the race for higher data rates leads to introducing higher data rates of 2.5 Gb/s, 5 Gb/s and 10 Gb/s over a single shielded twisted pair which named 2.5/5/10G-BASE-T1, respectively and got approved by June 2020 [7].

Fig. 2.7 depicts the Ethernet model defined by IEEE802.3 and the International Standards Organization (ISO) Open System Interconnection (OSI) reference model. This model shows where the PHY is defined in the Ethernet model and highlights its different components: physical coding sublayer, physical medium attachment, and auto-negotiation (optional). The Medium in this model is the cable, which for data rates higher than 1 Gb/s is a single STP cable and for lower and equal to 1 Gb/s data rate is a single UTP cable.

2.3 Transceiver Architecture

The transceiver architecture showing detailed units within the PHY and MDI is depicted in Fig. 2.8. Different components of such a transceiver are briefly introduced here.

2.3.1 PHY

The PHY is divided into PCS and PMA, which separate the digital and analog functions, respectively. The PHY is normally implemented in a single semiconductor.

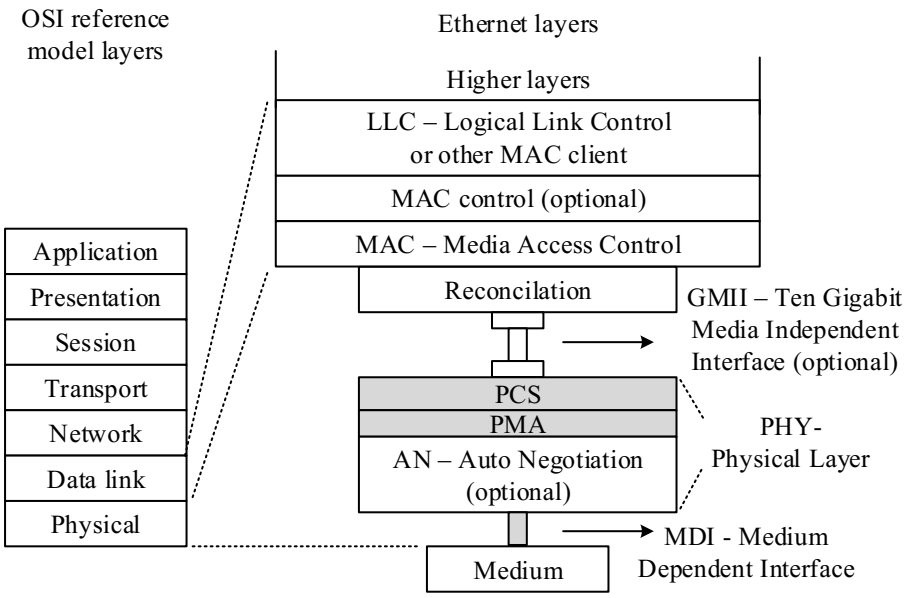


Figure 2.7: Relation of IEEE802.3 Ethernet model and the ISO OSI reference model [4].

PCS

The PCS receives data from Gigabit Media Independent Interface (GMII) and encodes the input data for the transmitters within the PMA. The input data encoding includes the Pulse Amplitude Modulation (PAM) depending on the data rate standard, scrambling, pulse shaping the signal, etc. The encoding applied to the input data is to increase the robustness of the data transmission and shape the signal spectrum by encoding to complying with the requirements set by the standard [5]. Furthermore, the data received from the PMA goes through a Forward Error Correction (FEC) block to decode the errors.

PMA

The PMA prepares the signal for the transmission on the channel via the transmitter. In addition, it outfits the received signal to be decoded by the PCS. The DAC transfer the coded digital PAM signal into the analog signal to be transferred on the channel. In the proposed architecture shown in Fig. 2.8, there is an identical DAC to the TX-DAC named EC-DAC, which makes the echo cancellation via the passive hybrid. A hybrid in a full-duplex operation is essential since the received signal and transmit signal are applied on the same channel. Therefore, using a hybrid, the transmit signal is eliminated from the received signal before feeding into the receiver. The detailed discussion of the use of the hybrid and the EC-DAC is discussed in 3.5. The transmit signal is then fed to the Medium

Dependent Interface (MDI), which consists of a Common Mode (CM) filter, Common Mode Choke (CMC), and a DC block. After removing the TX power from the received signal, a Low Pass Filter (LPF) is applied to the signal to limit the bandwidth to eliminate the unnecessary noise from the channel. After the LPF, a Programmable Gain Amplifier (PGA) is used to amplify the input signal before feeding it into the Analog to Digital Converter (ADC) to relax the resolution requirements of the ADC. The digital data is then fed to the PCS.

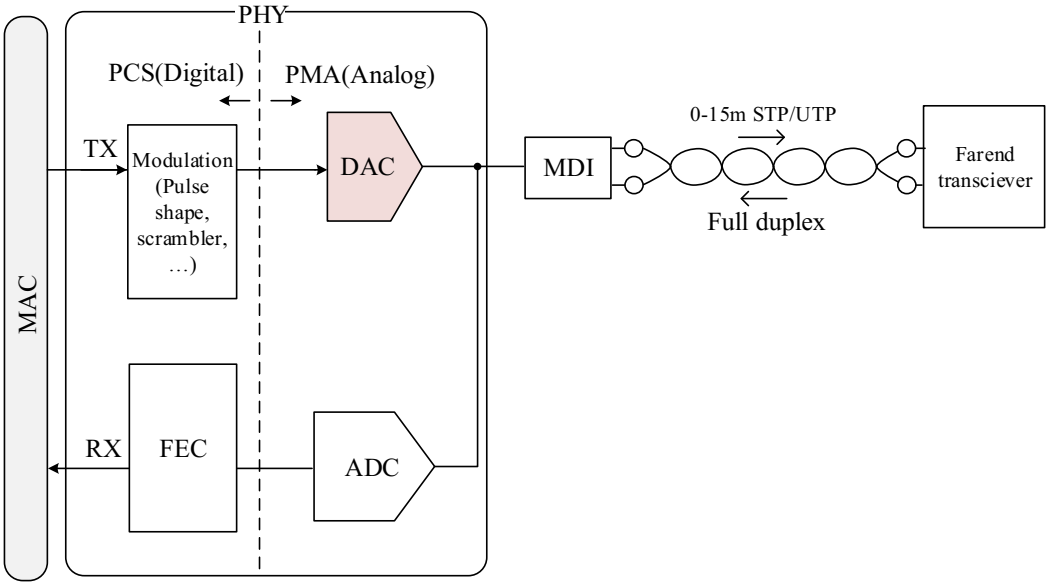


Figure 2.8: The architecture of the Ethernet transceiver showing the units within the PHY and MDI.

2.3.2 Cables

The medium approved for data rates higher than 1 Gb/s is a shielded twisted pair, whereas, for data rates equal or lower than 1 Gb/s, unshielded twisted pair is approved. The shielded twisted pair has a higher bandwidth than the unshielded twisted pair as well as better noise immunity. With increasing 10 fold the data rate and only increasing the modulation level from PAM-3 in 1000Base-T1 to PAM-4 for MultiGBase-T1, the bandwidth needs to increase as well.

STP S-parameter

The S-parameter of a 10 m STP cable suitable for MultiG-BASET1 standards is depicted in Fig. 2.9. The STP link segment should be within the approved limits for the S_{12}, the

insertion loss, and the S_{11}, the return loss defined by MultiG-BASET1 standard. The insertion loss of each of the link segment should be within

$$IL_{\text{limit,MultiG-BASET1}} \geq 0.002f + 0.68f^{0.45}[dB] \tag{2.1}$$

where f is the frequency in MHz. Furthermore, to limit the noise at the receiver due to the impedance mismatch, each link segment should be within an acceptable return loss range of

$$RL_{\text{limit,MultiG-BASET1}}(f) \geq \begin{cases} 20 & dB \quad 1 < f \leq 480/2^N \\ 20 - log_{10}((2^N \times f)/480) & dB \quad 480/2^N < f \leq 3000 \\ 12 - 3N & dB \quad 3000 < f \leq 4000 \end{cases} \tag{2.2}$$

where f is the frequency in MHz and

$$N = \begin{cases} 0 & IL_{\text{STP}}(3\,\text{GHz}) > 15\,\text{dB} \\ 1 & IL_{\text{STP}}(3\,\text{GHz}) \leq 15\,\text{dB} \end{cases} . \tag{2.3}$$

In the case of the 10 m STP link segment shown in Fig. 2.9, $IL_{\text{STP}}(3\,\text{GHz}) \leq 15\,\text{dB}$, hence N=1.

2.3.3 Full Duplex Operation

One of the main challenges of true full-duplex operation is that the received signal, which is highly attenuated on the 10m UTP/STP, should be detected with a BER less than 1E-12 while simultaneously superimposed with the full-scale transmit signal on the same line. Therefore, the use of an active or passive hybrid is beneficial.

A full-duplex operation on the medium in Automotive Ethernet enables transmitting and receiving data at the same time, effectively doubling the effective data rate on the single STP medium. However, in a full-duplex operation, the TX power of a PHY is present on the medium together with the TX power from the PHY on the far-end. Hence, the use of a hybrid to eliminate TX power is required. The detailed discussion on the implementation of a hybrid is presented in Sec. 3.5. As proposed in Fig. 2.8, a DAC duplicate, EC-DAC, is used to cancel the TX-DAC power echo at the receiver.

2.3.4 Transmitter Requirements

The transmitter with the PMA should provide a maximum of 1 V peak-peak differential output signal when the output is terminated with a 100 Ω resistive load [4]. Therefore, in order to maximize the power transmission efficiency, the transmitter should be self terminated to 100 Ω to meet the return loss requirement at the MDI shown in Sec. 2.6. The

transmitter should provide a PAM4 signal for Multi-GBASE-T1, therefore, the transmitter should have a resolution of at least 2-bit. However, in order to have a Relative Level Mismatch ratio (RLM) of greater than 0.95, a minimum of 4-bit is required. Moreover, the stringent requirement of the transmit signal to comply with Power Spectral Density (PSD) and EMC mask, as well as implementing pre-equalization on the TX data for the channel, a higher resolution on the DAC is required. The bandwidth of the transmitter requires to be at least 5.6 GHz to enable PAM4 signaling for the maximum data rate of 10 Gb/s.

PSD

The PSD masks defined by MultiG-BASET1 are dependent on the peak emission requirements, set by Original Equipment Manufacturers (OEMs). The established limit for radiated emission field strength within the frequency range of 70 MHz-1 GHz is 15 dBμV according to [8]. The transmit peak-peak amplitude of 1 V also affects the PSD mask and considering the system variation and loss effects and required safety margin, the TX power range is within -0.5 dBm to 2 dBm [9]. Given the emission requirements and the signal amplitude, the PSD masks defined for different data rates within MultiG-BASET1 are suggested as shown in Fig. 2.10.

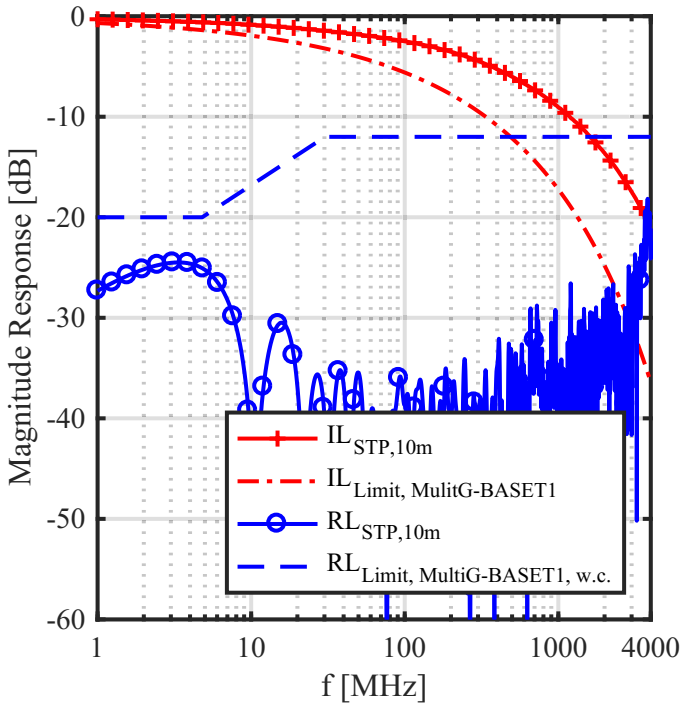


Figure 2.9: S-parameter of a 10 m STP cable and the limit lines for insertion loss and return loss for the worst-case corner. Limit lines are taken from the IEEE802.3 for MultiG-BASET1 standards [4].

$$PSD_{\mathrm{U}}(f) = \begin{cases} -90 - K & dBm/Hz \quad 0 < f \leq 600 \times S \\ -89 - K - \frac{f}{600 \times S} & dBm/Hz \quad 600 \times S < f \leq 3000 \times S \\ -82 - K - \frac{f}{250 \times S} & dBm/Hz \quad 3000 \times S < f \leq 5500 \times S \end{cases} \tag{2.4}$$

$$PSD_{\mathrm{U}}(f) = \begin{cases} -96 - K & dBm/Hz \quad 5 < f \leq 400 \times S \\ -95 - K - \frac{f}{400 \times S} & dBm/Hz \quad 400 \times S < f \leq 2000 \times S \\ -90 - K - \frac{f}{200 \times S} & dBm/Hz \quad 2000 \times S < f \leq 3000 \times S \end{cases} \tag{2.5}$$

where f is the frequency in MHz.

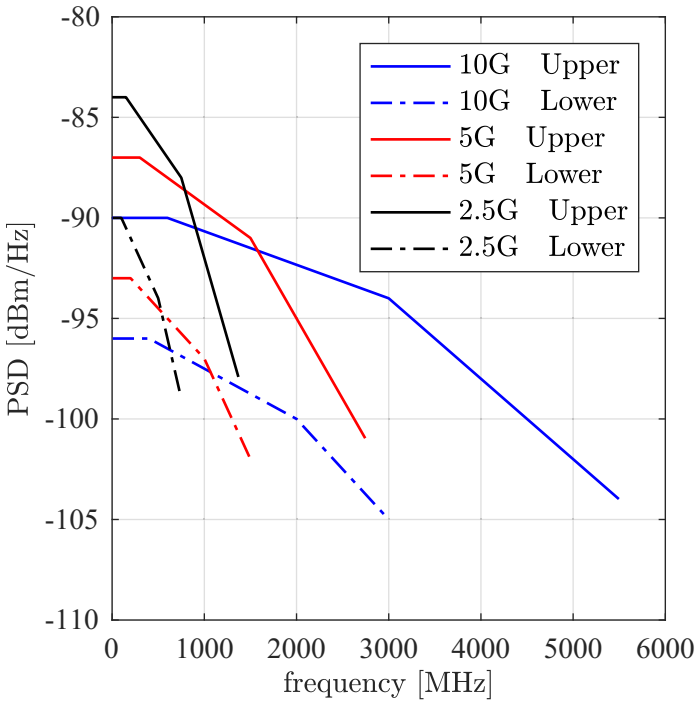


Figure 2.10: The upper and lower mask for the transmit power spectral density for 10GBASE-T1, 5GBASE-T1 and 2.5GBASE-T1 [7].

Return Loss

One of the main requirements in the MDI is the return loss, shown in Fig. 2.11. This transmitter design has a major effect on the return loss in MDI by matching the driver's termination to the cable. According to the -20 dB return loss limit line at DC frequencies up to 500 MHz, it can be calculated that the capacitance mismatch between the TX output

and the load is allowed up to 320 fF. It means that by assuming a 1 pF load capacitance, the TX output capacitance can vary in the range of 680 fF up to 1.32 pF.

$$RL_{\mathrm{MDI}}(f) \leq \begin{cases} 20 - 20\log_{10}\frac{10}{f} & dB \quad 1 \leq f \leq 10 \\ 20 & dB \quad 10 \leq f \leq 500 \\ 12 - 10\log_{10}\frac{f}{3000} & dB \quad 500 \leq f \leq 3000 \\ 12 - 20\log_{10}\frac{f}{3000} & dB \quad 3000 \leq f \leq 4000 \end{cases} \tag{2.6}$$

where f is the frequency in MHz.

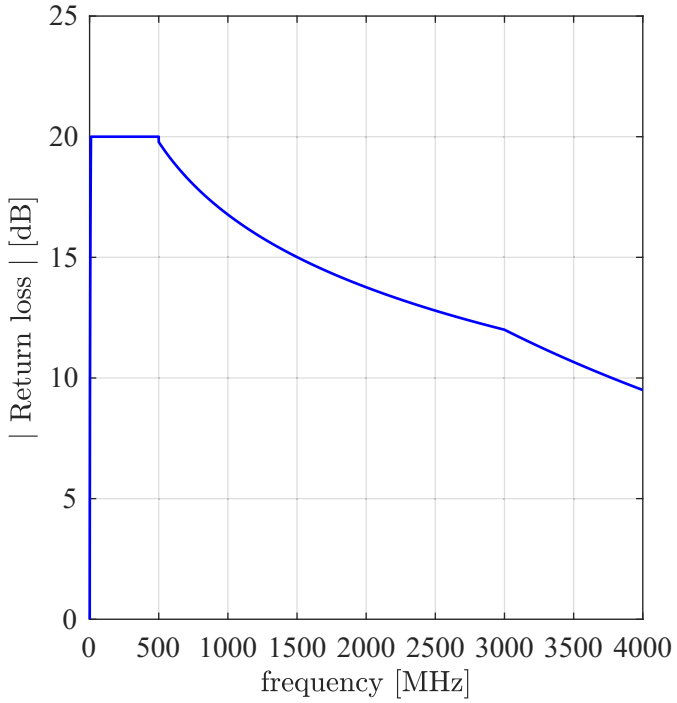


Figure 2.11: MDI return loss mask according to Eq. 2.6 for 10GBASE-T1, 5GBASE-T1 and 2.5GBASE-T1 [7].

2.3.5 EMC Requirements

The electromagnetic environment of a vehicle moving changes continuously, which can affect the operating of the Ethernet technology. This comes as a security and reliability issue to consider the system's immunity to electromagnetic interference.

The automotive EMC standards used worldwide are published by organizations, IEC/CISPR, and ISO [10]. In an automotive environment, according to the standard set by MultiG-BASET1 the PHY should meet the following requirements [4]:

- Radiated/conducted emissions: CISPR 25, IEC 61967-1, IEC 61967-4 and IEC 61000-4-21
- Radiated/conducted immunity: ISO 11452, IEC 62132-1, IEC 62132-4 and IEC 61000-4-21
- Electrostatic discharge: ISO 10605, IEC 61000-4-2 and IEC 61000-4-3
- Electrical disturbance: IEC 62215-3, ISO 7637-2 and ISO 7637-3.

Each of the test setup and limit values should be adjusted to each specific application.

3 High Speed DACs

Firstly in this chapter, some of the DAC performance measures which can be calculated and simulated to characterize its performance are introduced. After that, two types of DAC realization, current-mode DAC and voltage-mode DAC, which can directly drive the channel in an Ethernet transceiver at high speed and resolution, are introduced. Each DAC type is discussed in detail to enable comparison based on performance, linearity, power, and silicon area. Next, source series terminated DAC architecture is studied in detail, discussing the challenges in the use of such DAC with possible solutions.

3.1 DAC Performance Parameters

A DAC inputs a digital discrete signal and transforms it into a continuous analog signal. The analog signal on the output works as an information carrier in which digital data is modulated. Implementing this circuit using CMOS technology not only modulates the digital input signal to the output but also some of the non-idealities showing up as noise on the output signal. These non-idealities can be due to process mismatch, settling error, noise, parasitics limiting the signal bandwidth, non-linear impedance characteristics, etc. Here some of the standard measures that characterize the DAC performance due to these error sources are introduced. These measures divide into two categories of static and dynamic properties based on the source of the error.

3.1.1 Static Properties

Resolution

Fig. 3.1 shows the DC characteristic of a 2-bit DAC. The output voltage levels for an ideal case without any static error is shown in Fig. 3.1 where the straight line has no deviation and each step of the output curve increase with each digital input sequence with an exact step size named Δ. In this example, the output amplitude level of 0 corresponds to the Least Significant Bit (LSB), and the output amplitude level of 3 corresponds to the Most Significant Bit (MSB). The defined Δ shows the amplitude level increase by one LSB as well. The output LSB step compared to the full-scale output is referred to as the DAC's resolution:

$$Res. = \frac{FS}{\Delta} \tag{3.1}$$

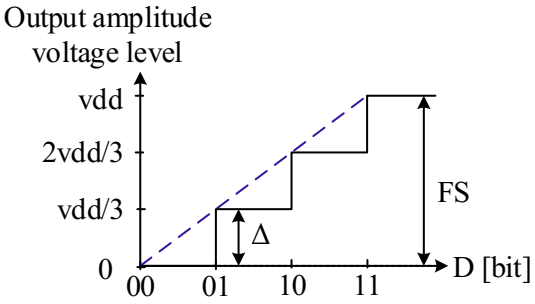


Figure 3.1: Simple 2-bit ideal output amplitude level DAC static characteristic.

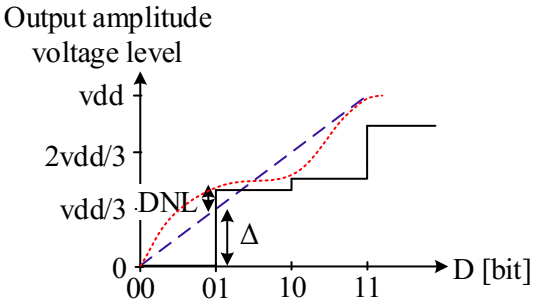


Figure 3.2: Simple 2-bit output amplitude voltage level DAC static characteristic with non-idealities showing the deviation from the ideal curve and DNL measures.

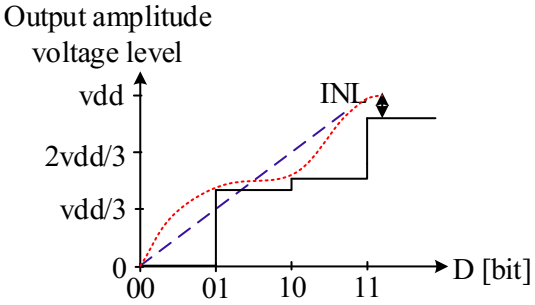


Figure 3.3: Simple 2-bit output amplitude level DAC static characteristic with non-idealities showing the deviation from the ideal curve and INL measures.

Static Performance

The static properties of a DAC are due to noise or distortion, which are present at lower frequencies and are data-independent, meaning no memory effect from previous data settling. These types of measures set the best case performance for a DAC as it shows

the possible performance without high-frequency non-idealities degrading the performance. The main static properties studied in this work are: gain error, Differential (DNL), and Integral non-linearities (INL). The gain error is the deviation of the input to the output curve from the straight line, which is desired for a perfect digital to analog converter DC characteristic. As input digital code is incremented, an error is introduced as shown in Fig. 3.2 and Fig. 3.3 which also highlight the DNL and INL error at the binary digital input code of *01* and *10*, respectively. DNL error considers the differential error added to the output DC characteristic on top of the expected Δ increase. However, the INL error shows the total deviation of the analog value from the ideal value. DNL and INL error across the digital input code D can be written as:

$$DNL_{\mathrm{D}} = INL_{\mathrm{D}} - INL_{\mathrm{D-1}} \tag{3.2}$$

and

$$INL_{\mathrm{D}} = INL_0 + \sum_{D=0}^{2^N-1} DNL_{\mathrm{D}} \tag{3.3}$$

where N is the number of bits.

3.1.2 Dynamic Properties

The dynamic properties show the effects of dominating at higher frequencies and introducing errors into the output signal. These types of properties are signal-dependent such as settling error, slewing, jitter, glitches, power supply noise coupling, etc. Here some of the main parameters describing the DAC performance, specifically used in communication theory, are introduced, such as signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), signal to noise and distortion ratio (SNDR), the effective number of bits (ENOB), etc.

In order to calculate the dynamic properties, a Fast Fourier Transform (FFT) is performed on the analog output signal of the DAC. A simulated frequency spectrum is shown in Fig. 3.4 where a single tone sinusoidal signal is input into a non-linear DAC. The spectrum is shown up to half of the sampling frequency of 2.8 GHz (Nyquist frequency=1.4 GHz). The frequency spectrum is scaled so that the main tone is at zero. The odd harmonics of the main tone, such as 3rd and 5th harmonics, are visible in this spectrum, standing out from the noise floor. The even harmonics are damped since the non-linear DAC under simulation is fully differential. The noise floor is a result of the quantization noise. Above the noise floor, the distortions due to the non-linear effects of the DAC are visible as well.

Signal-to-Noise Ratio (SNR)

The power ratio of the main signal and the total noise within a defined frequency band, excluding the harmonic components, provides the SNR ratio:

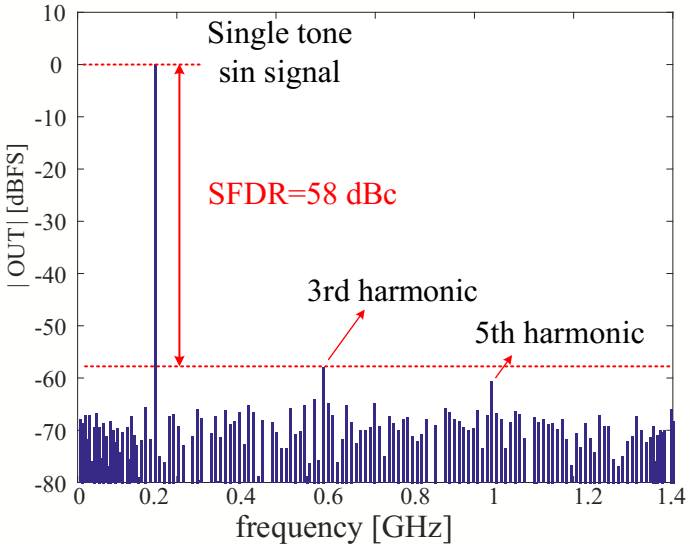


Figure 3.4: The frequency spectrum of a DAC running at 2.8 GS/s with a single tone sinusoidal signal at its input highlighting SFDR measure and noise floor.

$$SNR = 10 \cdot log_{10} \frac{P_\mathrm{s}}{P_\mathrm{n}} [dB] \tag{3.4}$$

where P_s is the signal power and P_n is the noise power.

Spurious-Free Dynamic Range (SFDR)

The SFDR ratio is the ratio of the main signal power and the largest spurious signal within a defined frequency band as

$$SFDR = 10 \cdot log_{10} \frac{P_\mathrm{s}}{P_\mathrm{x}} [dB] \tag{3.5}$$

where P_s is the signal power and P_x is the spurious power. Normally the largest spurious showing up in the spectrum for a differential DAC is the first odd harmonic, the 3rd harmonic.

Signal-to-Noise and Distortion Ratio (SNDR)

The SNDR is the ratio of the signal power and the total noise and distortion power within a certain frequency band as

$$SNDR = 10 \cdot log_{10} \frac{P_{\mathrm{s}}}{P_{\mathrm{n}} + \sum_{k=2}^{\infty}} P_{\mathrm{k}}[dB] \tag{3.6}$$

where P_{s} is the signal power, P_{n} is the noise power and P_{k} is the power of the k-th harmonic.

Effective Number of Bits (ENOB)

Certain number of bits that SNDR corresponds to is named as ENOB and calculated as:

$$ENOB = \frac{SNDR - 1.76dB}{6.02dB}[bit]. \tag{3.7}$$

3.2 DAC Circuit Implementations

Converting digital data into analog waveform to directly drive a differential impedance of $100\,\Omega$ of a channel is done generally through two architecture types of DACs, namely as voltage-mode and current-mode. In selecting the DACs proposed to be used in this application, it is essential that the minimum peak-peak differential output voltage of $1\,\mathrm{V}$ is satisfied. This means a differential current of $\pm 5\,\mathrm{mA}$ should be supplied between the differential outputs. Therefore the driver should be capable of delivering such rail to rail electrical current change in a limited time to settle defined by the operating frequency. Thus, the two architectures introduced here are the most common options for high-resolution and high-speed demand.

3.2.1 Current-Mode DAC

Current-mode DACs, as the name suggests, as the name suggests, provides a current signal in their output. A simple binary-weighted current-switching DAC is illustrated in Fig. 3.5. Each binary input bit controls a binary-weighted current source scaled to a unit value, I_{b}. LSB cell is denoted by D_0 and MSB cell by $D_{\mathrm{N}-1}$ for an N-bit DAC. Therefore, the output current of such binary-weighted current-switching DAC is written as:

$$I_{\mathrm{TX}} = D_0 \cdot I_{\mathrm{b}} + D_1 \cdot 2I_{\mathrm{b}} + ... + D_{\mathrm{N}-1} \cdot 2^{(N-1)} I_{\mathrm{b}}. \tag{3.8}$$

The current-steering DAC presented in Fig. 3.5 suffers from dynamic errors. The biasing current cells in this architecture are realized with current mirror switches. When each of the binary-weighted switches turns off, the drain-source voltage on the connected current mirror switch drops to zero. When the corresponding binary-weighted switch turns on again, it

draws a transient current from the output node, introducing an error on the output current, I_{TX}. Moreover, the switching activity also introduces fluctuations to the ground voltage, which can cause dynamic non-linearities with the presence of parasitic capacitance and inductance on the ground.

In order to mitigate the aforementioned dynamic errors, the use of current-steering DACs is introduced. A simple circuit implementation of a 1-bit current-steering DAC is shown in Fig. 3.6. Here, the tail current I_{b} is steered to the left (DP=1) or the right (DN=1) by the differential pair. Therefore, the voltage fluctuation due to the switching activities across the drain-source voltage of the current mirror switch realizing I_{b} is mitigated. Moreover, the differential characteristic of this architecture is also a necessity for driving the differential UTP/STP channels in the target application. In Fig. 3.6, the model of the channel with the impedance Z_{out}, as well as termination resistors R_{L}, is depicted as well, as these components are necessary for the use of such current-steering DAC for the target application here, to drive a $100\,\Omega$ channel. The use of R_{T} provides the self-termination of this driver to match the channel impedance, providing efficient power transmission.

One drawback of using current-steering DAC is to ensure that the current mirror switches are operating in the saturation region. Therefore at least one drain-source voltage is subtracted from the supply voltage vdd, limiting output voltage swing. The current mirrors are required to operate in the saturation region to function well for the purpose of current mirroring [11].

A general circuit implementation of an N-bit binary-weighted current-steering DAC is shown in Fig. 3.7. By injecting I_{TX} current into a channel with a known impedance, a defined output voltage can be sensed across the channel. The digital input code in this differential circuit implementation is shown with complementary signals DP[N-1:0] and DN[N-1:0]. The operation of the switches in this architecture is categorized as class-A since not all the current that is drawn is injected into the channel and part of this current is injected into the local termination, R_{T}.

The current drawn from the supply is shown. It is constant across the digital input code, one of the major advantages of this architecture in high-speed applications. A constant current drawn from the supply mitigates the noise that can be introduced on the supply rails due to the parasitic capacitance and inductance from the chip packaging and the DAC implementation in silicon. These topics are covered in more detail in the following sections.

Segmentation

The binary-weighted architecture shown in Fig. 3.5 and Fig. 3.6 can exhibit a large error or non-monotonicity when the binary input code transition from 011...1 to 100...0, which comes from the mismatch between the current mirror cells [11]. This transition has only 1 LSB change on the output, however, if the accumulated mismatch of the current mirror cells from I_{b}, $2I_{\mathrm{b}}$,...,$2^{N-2}I_{\mathrm{b}}$ is higher than 1 LSB to $2^{N-1}I_{\mathrm{b}}$, a non-monotonicity has occurred in

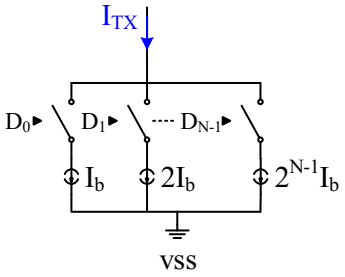


Figure 3.5: Simple binary-weighted current-switching DAC.

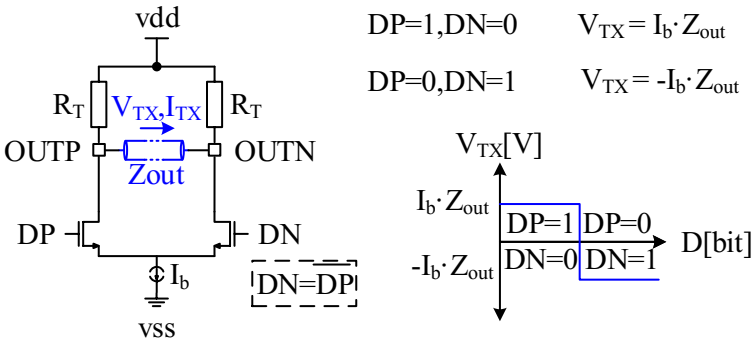


Figure 3.6: Circuit implementation of a 1-bit current-steering DAC.

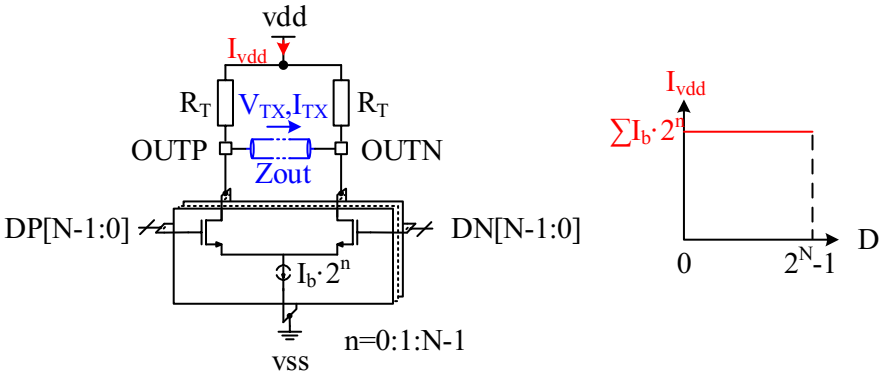


Figure 3.7: General circuit implementation of an N-bit current-steering DAC with the current drawn from its power supply plotted across the input digital code.

the transfer function. In order to prevent these errors from happening, a segmented DAC architecture is proposed as shown in Fig. 3.8. In a segmented DAC, $2^N - 1$ thermo-weighted cells are needed. Since all current mirror cells have the same current, a better matching can be achieved comparing to current-mirrors in binary-weighted cells. The same approach can also be considered with the current-steering architecture.

Partial Segmentation

One main drawback of the full segmentation of the DAC is the increase in the silicon area as each LSB current-mirror cell is designed carefully to minimize the mismatch, as well as increasing the complexity of the coding. Therefore, a trade-off between the binary-weighted and thermo- or unary-weighted should be met in a partially segmented DAC. In a partially segmented DAC, MSB cells are unary-weighted and LSB cells, binary-weighted. This brings a trade-off between the linearity of the DAC, power, and area utilized by it.

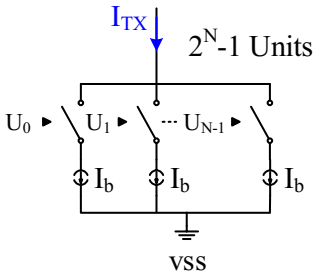


Figure 3.8: A simple unary current-switching DAC.

Performance, Linearity, Power and Area

By adding all the bias currents across all the cells of a current-steering DAC, the total static power consumption of the main DAC driver can be calculated as:

$$P_{\text{cons.,CM}} = \sum_{n=0}^{n=N} I_{\text{b}} 2^{n-1} \cdot \text{vdd} = (2^N - 1) I_{\text{b}} \cdot \text{vdd}. \tag{3.9}$$

Since the current is steered in each cell from one output to the other output in an incident of data change, the total power being drawn from the supply is constant. These types of DACs have the advantage of having current sources to charge and discharge the parasitic capacitors at the outputs fast, hence making it one of the most common DAC implementation for high-speed applications.

The linearity of this DAC is limited to the output impedance of the switches, matching between the switches and bias currents across cells, the timing of the differential controlling signals of DP and DN, clock, data feed-through, etc. Moreover, with scaling down the technology, less headroom is available for switches and the biasing current mirrors.

The area regarding these DACs is mainly addressed to the current mirrors providing a bias current to all the cells. These current mirrors are designed with higher channel length than other devices to minimize the matching effect. Hence, the area of a current-mode DAC is mainly enlarged by the requirement to match the current-mirrors.

3.2.2 Voltage-Mode DAC

Voltage-mode DACs, as the name suggests, provides a voltage signal in their output. Since such DAC should drive a $100\,\Omega$ differential impedance modeled of the channel, the voltage output signal provided on the output should be capable of delivering such current. Therefore, a resistive type of voltage division is applied rather than capacitive voltage division, which cannot drive the resistive load at high speeds. Voltage-mode DACs use series termination to match the output impedance Z_{out} of the channel. A simple 1-bit inverter-based voltage-mode DAC with series termination impedance R_{T} is shown in Fig. 3.9. The switches are sized so that the on-resistance of NMOS and PMOS switches are equal ($R_{\text{onN}} = R_{\text{onP}}$). This resistance is mentioned as R_{on} throughout this section for simplicity.

To meet the signal integrity, the sum of the termination impedances switches on-resistance R_{on} and series resistor R_{T} should be equal to the single-ended impedance of the channel $\frac{Zout}{2}$:

$$R_{\text{on}} + R_{\text{T}} = \frac{Zout}{2}. \tag{3.10}$$

In the 1-bit DAC shown in Fig. 3.9, the output driver voltage V_{TX} toggles between $\frac{\text{vdd}}{2}$ when DP=0 (DN=1) and $-\frac{\text{vdd}}{2}$ when DP=1 (DN=0). This type of voltage-mode architecture is know for the high-swing (rail to rail output voltage swing) and low-impedance switches.

Fig. 3.10 shows a 2-bit inverter-based voltage-mode DAC. In this case, the LSB cell has a termination impedance value of $2R_{\text{T}}$ and on-resistance switches of the LSB cell are also sized to be $2R_{\text{on}}$ comparing to the MSB cell. In the case of the 2-bit architecture, to meet the signal integrity, the parallel combination of the sum of series termination impedances should be equal to the single-ended impedance of the channel $\frac{Zout}{2}$:

$$(R_{\text{on}} + R_{\text{T}}) \parallel 2 \cdot (R_{\text{on}} + R_{\text{T}}) = \frac{Zout}{2}. \tag{3.11}$$

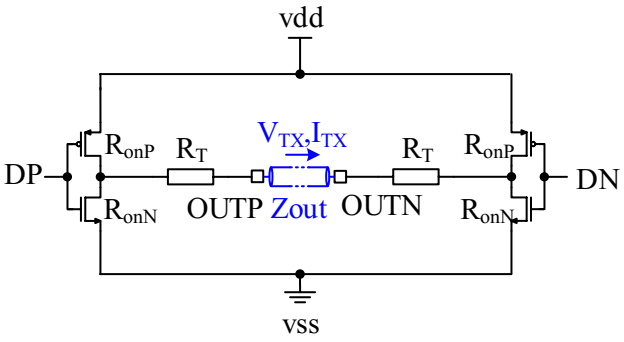


Figure 3.9: Circuit implementation of a simple 1-bit inverter base voltage-mode DAC.

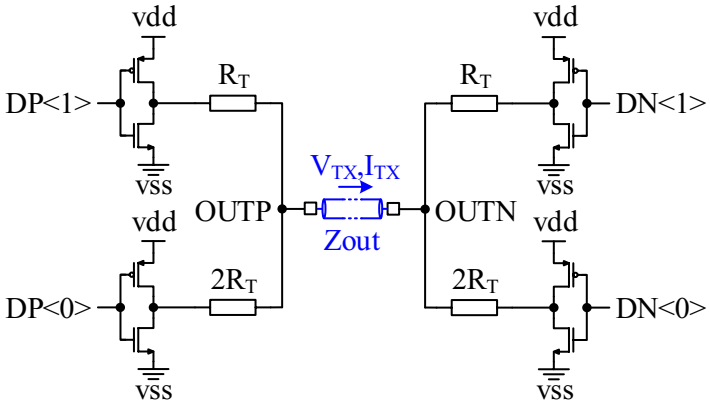


Figure 3.10: Circuit implementation of a 2-bit inverter base voltage-mode DAC.

One of the major drawbacks in the voltage-mode DAC shown in Fig. 3.9 is the size of the switches to meet the termination impedance. Normally the switches are sized so that their contribution to the termination impedance is negligible comparing to the termination resistor R_{T}. This is due to the fact of minimizing the on-resistance non-linearities in the DAC operation. Therefore, an alternative implementation with a low-swing output voltage and high-impedance switches is shown in Fig. 3.11 [12]. In this architecture, all devices are NMOS devices, and to meet the signal integrity, the devices are sized so that the on-resistance of each device when enabled is equal to $\frac{Zout}{2}$:

$$R_{\mathrm{on}} = \frac{Zout}{2}. \tag{3.12}$$

Noted that in this architecture, the effective V_{GS} of the devices on the top and the bottom are different and should be considered for the switch sizing.

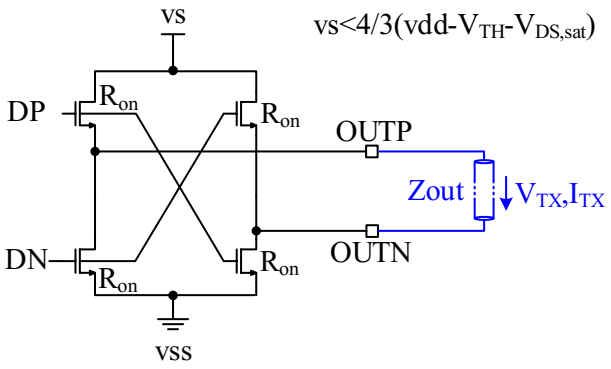


Figure 3.11: Circuit implementation of a simple 1-bit low-swing voltage-mode DAC.

Another major drawback of the voltage-mode DAC shown in Fig. 3.9 is the high transient crow-bar currents drawn from the power supply due to the inherent architecture of the inverter. The architecture shown in Fig. 3.12 brings the termination resistor R_T in the push-pull path, lowering the crow-bar current. However, this comes as a drawback of increasing the DAC area and lowering the output bandwidth by doubling the parasitic capacitance at the output node. Moreover, the parasitic capacitance between the drain of the switches and R_T, results in slower settling on the output nodes.

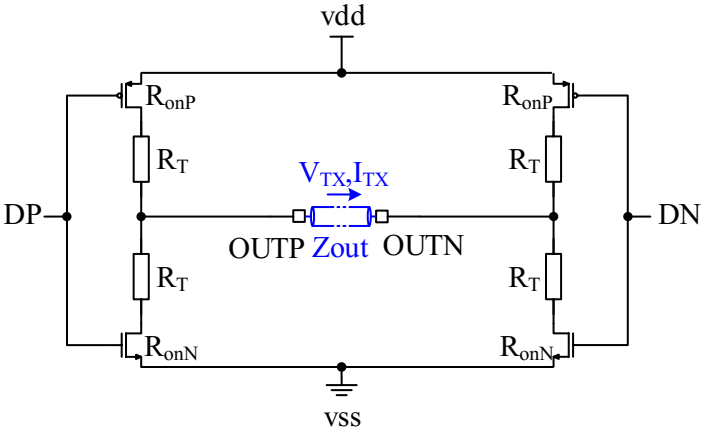


Figure 3.12: Circuit implementation of a simple 1-bit inverter base voltage-mode DAC with termination resistor R_T in the push-pull path.

N-bit Source Series Terminated DAC

A general circuit implementation of a simple voltage-mode DAC is shown in Fig. 3.13. The current drawn from the power supply showing a parabolic shape across the digital input code is also depicted. This type of DAC is usually called source series terminated (SST)

DAC. As the name suggests, the device is in series with the termination of the DAC. The operation of the switches in this DAC is a class-B mode of operation, and the push-pull mode of operation enables to inject all the current that goes through the supply into the channel. The parabolic shape of the power supply current is one of the inherent features of such DAC which can cause noise on the power supply with PRBS code as the digital input code and drawing a code-dependent current from the power supply. This code-dependent current drawn from the supply can in turn introduce a code-dependent noise on the power supply. In order to overcome this drawback, one can implement a dummy DAC with a reverse parabolic shape to the one shown in Fig. 3.13, to make the total current drawn from supply independent of the digital input code as in Fig. 3.7. However, this comes with doubling the power consumption of the SST DAC which makes it less attractive to the current-steering DAC alternative.

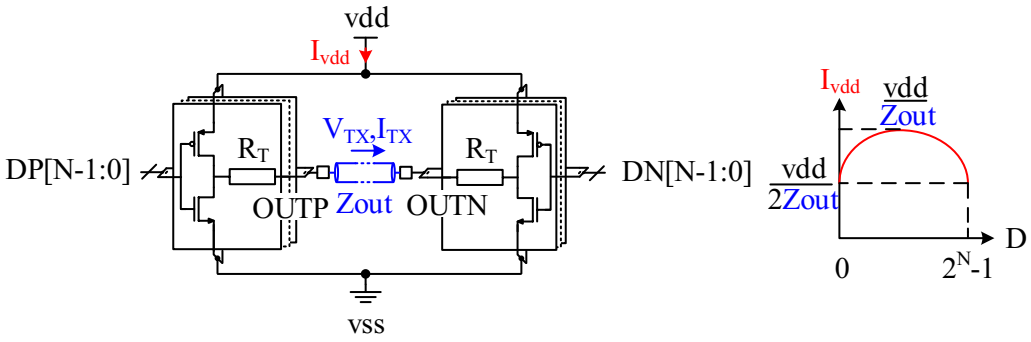


Figure 3.13: General circuit implementation of an N-bit voltage-mode DAC showing as well the current drawn from the power supply across the digital input code.

Performance, Linearity, Power and Area

To calculate the static power consumption of the voltage-mode DAC, an integral on the current drawn from the power supply shown in Fig. 3.13 across digital input code. The range of the power consumption of this DAC is calculated as:

$$P_{\text{cons.,VM}} = [\frac{\text{vdd}^2}{4R_\text{T}}, \frac{\text{vdd}^2}{2R_\text{T}}] \tag{3.13}$$

where R_T is assumed $50\,\Omega$.

The average energy consumption of the DAC also depends on the digital coding applied to the input signal, as if the communication channel used more the average code range instead of the sides for its modulation. Therefore, the average power consumption is closer to its maximum value in the range defined in Eq. 3.13.

The linearity of this DAC is influenced by several factors such as termination impedance linearity, power supply voltage modulation due to the parabolic shape of current demand, matching between the switches, etc.

The area that this DAC requires is mainly driven by the switches and the termination resistance R_{T}.

3.3 Comparison of Voltage-Mode and Current-Mode DACs

To decide which of these type of DAC is the optimum choice, a summarized comparison of the two can make this more clear.

In terms of power, VM DACs are more power efficient using class-B operation, delivering all the current to the channel. In contrast, CM DACs use class-A operation, and part of the current is wasted in the parallel termination structure. To more accurately compare the power consumption of the two, it is assumed that both DACs provide a 1 V peak-peak differential voltage on the channel. Providing this differential output voltage requires vdd = 1 V for VM DAC architecture. The parallel and series termination resistors R_{T} is assumed equal to 50 Ω and the impedance of the switches are ignored.

Therefore based on Eq. 3.13, the power consumption range of a VM driver is within [5 mW − 10 mW].

However, providing the same differential output voltage form CM driver requires total bias current of $\sum_{n=0}^{n=N-1} I_{\mathrm{b}} \cdot 2^n \approx 20\,\mathrm{mA}$ which gives 20 mW as the total static power consumption.

It can be concluded that VM DACs are inherently at least two times and up to four times more power-efficient than CM DACs.

In terms of area, VM DACs inherently are smaller due to the use of a lower number of devices used in its architecture. The current mirror array in CM DACs consumes most of its area as the switches in these current mirrors are designed with a big area to minimize the mismatch error between these switches.

In terms of noise sensitivity, CM DACs are less sensitive to supply noise and support a higher data rate [13]. The current drawn from the power supply of a VM DAC is data-dependent. Thus a data-dependent noise can be modulated on the power supply, depending on the power supply impedance powering this DAC. Moreover, the crow-bar current in VM DACs when both pull-up and -down paths are conducting can create transient current spikes on the current drawn from the power supply I_{vdd}. Therefore CM DAC has the advantage of a more relaxed requirement on the supply.

The output voltage of VM DACs is limited to the supply voltage level vdd, whereas in CM DACs, the output voltage is limited by the biasing current I_{b}. Therefore the technology scaling going toward lower supply voltage makes the use of VM DACs more challenging.

3.4 SST DAC

Source series terminated DAC proves to be an optimum choice for the target application. The most important factor influencing this choice is the power consumption of such DAC, which can be at least two times and up to four times more efficient than the other possibility, CM DAC. In this section, the SST DAC architecture with few modifications from the general architecture is shown in Fig. 3.13 is presented. The challenges of designing this DAC to meet the requirements are discussed and possible solutions are presented. After that, in the next chapter, the implementation of such solutions is presented and backed up with simulation and measurement results.

3.4.1 Architecture and Requirements

The general architecture of an N-bit SST DAC is shown in Fig. 3.14. Unlike the circuit schematic is shown in Fig. 3.13, in this architecture, the termination resistance R_{T} is shared in both pull-up and pull-down paths. This lowers the crow-bar current by approximately five times [14]. Details of this modification and the effects are discussed in detail in this chapter. Each of the SST units' termination impedance is built from two components, a resistor R_{T} in series with MOSFET switches (resistance value $R_{\mathrm{onN,P}}$). In this circuit schematic, all the SST cells are binarily segmented, meaning from MSB cells to LSB cells, with each incrementation, the cell's impedance is doubled. Furthermore, the parallel of all the unit cells on each side, OUTP, and OUTN should provide a single-ended termination impedance of $50\,\Omega$, matching the impedance of the channel. The channel model of the differential twisted pair (UTP or STP cable) is assumed ideally as $R_{\mathrm{ch}} = 100\,\Omega$.

$$R_{\mathrm{MSB}} = R_{\mathrm{onP}} + R_{\mathrm{T}} = R_{\mathrm{onN}} + R_{\mathrm{T}} = R_{\mathrm{on}} + R_{\mathrm{T}} \tag{3.14}$$

$$R_{\mathrm{LSB}} = R_{\mathrm{MSB}} \times 2^{N-1} = (R_{\mathrm{on}} + R_{\mathrm{T}}) \times 2^{N-1}. \tag{3.15}$$

Parallel combination of all cells gives:

$$\frac{1}{R_{\mathrm{L}}} = \frac{1}{R_{\mathrm{MSB}}} \sum_{i=0}^{N-1} 2^{-i} = \frac{1}{R_{\mathrm{MSB}}} + \frac{1}{2 \times R_{\mathrm{MSB}}} + ... \tag{3.16}$$

with the assumption of high number of bits, the approximate value for R_{MSB} is:

$$R_{\mathrm{MSB}} \approx 2 \times R_{\mathrm{L}} = 100\,\Omega. \tag{3.17}$$

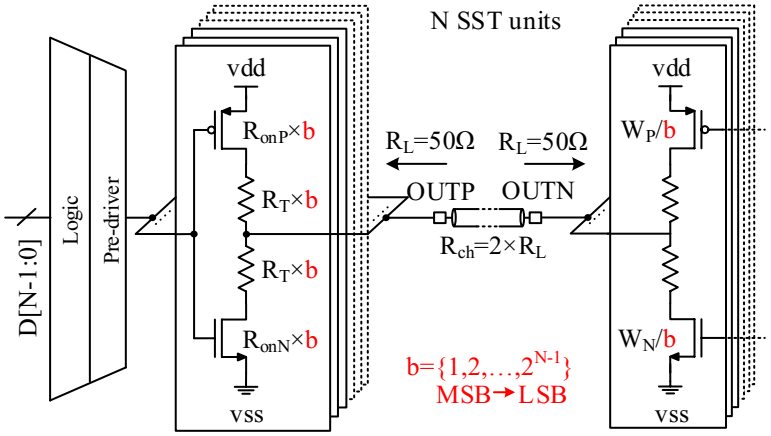


Figure 3.14: The circuit schematic of an N-bit SST DAC [15].

3.4.2 Performance, Linearity, Power and Area

Sharing the termination impedance between the active and passive devices, unlike architecture shown in Fig. 3.13, comes with few advantages and disadvantages. The biggest benefit, in this case, is enabling higher operating speed with lower dynamic power consumption. Making the switches big so that it reaches almost zero on-resistance, the capacitance at the gate of these devices requires spending a lot of dynamic power and area to drive the gates, which causes a more stringent requirement on the power supply to provide these high peaks of transient current. This limits the choice of the type of packaging that can be used to place the die and connect the power supply with more expensive solutions. Therefore, active devices participating in the termination come with the advantage of lower power, lower area, and cheaper packaging solutions.

On the other hand, active device on-resistance R_{on} is highly non-linear comparing to passive devices such as poly resistors. The non-linearity of such devices comes mainly as the dependence of R_{on} on the voltage drop across it, which is data-dependent in the SST DAC architecture. Therefore a data-dependent non-linearity is added to the termination impedance. This data-dependent variation on the termination impedance not only makes the matching for the target return loss presented in Sec. 2.3.4 challenging but also causes deviation of the analog output voltage level from its ideal value, increasing the INL error. Therefore, the linearity of this DAC is dependent on the ratio in which the termination impedance is divided between the passive to active components $r_{\text{RM}} = \frac{R_{\text{T}}}{R_{\text{on}}}$. The choice of this ratio is discussed in detail in the next section.

3.4.3 Linearity Limitations

To design an SST DAC, one should consider this trade-off between power, area, package expenses, and linearity. By studying the sources of non-linearity, careful study of the active to passive termination ratio, and the packaging effect, it is shown that this linearity limitation can improve by using the source degeneration effect of active devices. In this case, the mathematical model of a simplified SST DAC is presented to study the static effect of such non-linearities and the improvements which can be suggested. A brief explanation of this approach is presented in [15].

Active to Passive Termination Ratio

The trade-off between area/power and linearity performance is given by the ratio between the passive and active termination portion $r_{\mathrm{RM}} = \frac{R_{\mathrm{T}}}{R_{\mathrm{on}}}$. Therefore, the resistance of each (active and passive) portion considering a total termination resistance of $50\,\Omega$ is

$$R_{\mathrm{on}} = \frac{R_{\mathrm{MSB}}}{r_{\mathrm{RM}} + 1} \approx \frac{100\,\Omega}{r_{\mathrm{RM}} + 1}, \tag{3.18}$$

$$R_{\mathrm{T}} = \frac{r_{\mathrm{RM}} \times R_{\mathrm{MSB}}}{r_{\mathrm{RM}} + 1} \approx \frac{r_{\mathrm{RM}} \times 100\,\Omega}{r_{\mathrm{RM}} + 1}. \tag{3.19}$$

To study the static linearity of the DAC, a resistive model is developed shown in Fig. 3.15 to study the non-linear effect of the MOSFET switches.

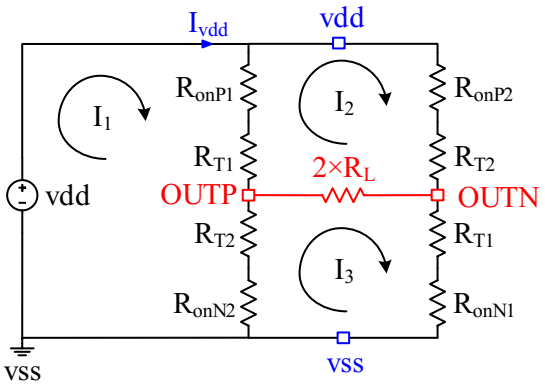


Figure 3.15: The equivalent resistive model of the SST DAC.

To study the effect of the switch non-linearities, the first analysis assumes linear switch resistance. The on-resistance R_{on} in the linear region and it is modeled as

$$R_{\text{on}} = \frac{V_{\text{DS}}}{I_{\text{D}}} = \frac{V_{\text{DS}}}{\mu C'_{\text{OX}} \left(\frac{W}{L}\right) \left(V_{\text{GS}} - V_{\text{TH}} - \frac{V_{\text{DS}}}{2}\right) \cdot V_{\text{DS}}}. \tag{3.20}$$

Assuming the drain-source voltage much smaller than the overdrive voltage, R_{on} is simplified as

$$R_{\text{oni}} = \frac{1}{\mu_i C'_{\text{OXi}} \left(\frac{W}{L}\right)_{\text{i}} (V_{\text{GSi}} - V_{\text{THi}})} \text{ , i} = \text{N, P} \tag{3.21}$$

where shows no dependency on V_{DS}.

The simplified resistor model for active and passive devices as a function of the digital input code, the number of bits, and the ratio of passive to active termination r_{RM} is calculated as:

$$R_{\text{oni1}} = R_{\text{on}} \times \frac{2^N - 1}{D} \text{ , } R_{\text{oni2}} = R_{\text{on}} \times \frac{2^N - 1}{2^N - 1 - D} \text{ , i} = \text{N, P} \tag{3.22}$$

$$R_{\text{T1}} = R_{\text{T}} \times \frac{2^N - 1}{D} \text{ , } R_{\text{T2}} = R_{\text{T}} \times \frac{2^N - 1}{2^N - 1 - D} \tag{3.23}$$

where N is the number of bits, D is the digital input code value within the range of zero to $2^N - 1$ and R_{on} and R_{T} are given in Eq. 3.18, 3.19. By solving the three Kirchhoff's Voltage Law (KVL) loops (as shown in Fig. 3.15):

$$I_1 : \text{vdd} + (I_{\text{vdd}} - I_2) \cdot (R_{\text{onP1}} + R_{\text{T1}}) + (I_{\text{vdd}} - I_3) \cdot (R_{\text{onP2}} + R_{\text{T2}}) = 0; \tag{3.24}$$

$$I_2 : I_2 \cdot (R_{\text{onP2}} + R_{\text{T2}}) + (I_2 - I_3) \cdot 2 \times R_L + (I_2 - I_{\text{vdd}}) \cdot (R_{\text{T1}} + R_{\text{onP1}}) = 0; \tag{3.25}$$

$$I_3 : I_3 \cdot (R_{\text{onN1}} + R_{\text{T2}}) + (I_3 - I_{\text{vdd}}) \cdot (R_{\text{onN2}} + R_{\text{T2}}) + (I_3 - I_2) \cdot 2 \times R_{\text{L}} = 0. \tag{3.26}$$

Solving these three KVL loops yields the supply current:

$$I_{\text{vdd}} = \frac{\text{vdd}}{R_{\text{L}}} \cdot \left(\frac{-D^2}{(2^N - 1)^2} + \frac{D}{2^N - 1} + \frac{1}{4}\right). \tag{3.27}$$

$$V_{\text{OUT}} = OUTP - OUTN = \text{vdd} \cdot (\frac{1}{2} - \frac{D}{2^N - 1}) = \text{vdd} \cdot (\frac{1}{2} - \frac{D}{2^N - 1}) \tag{3.28}$$

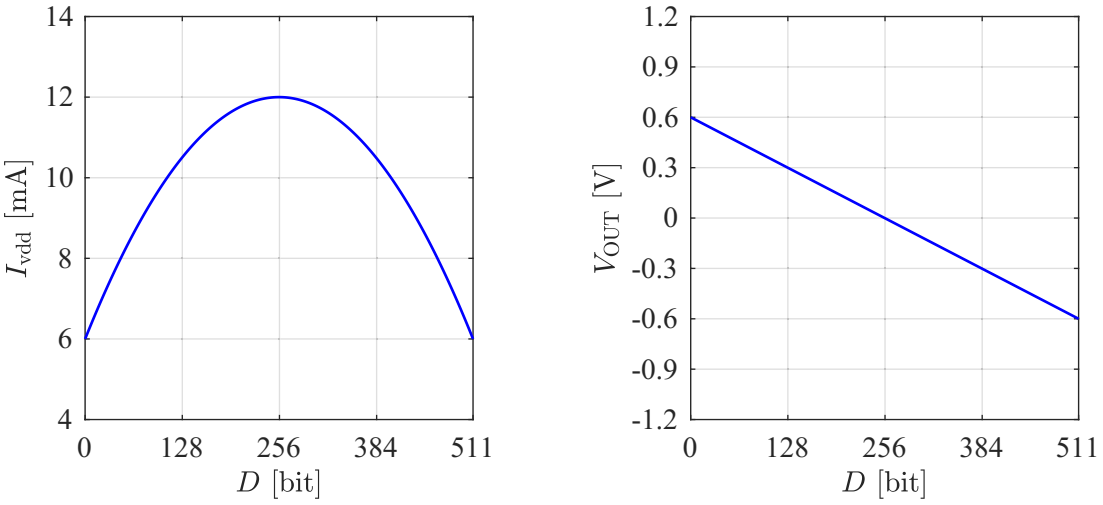
This shows a fully linear output curve with zero INL error. Calculating for D=0 and D=511, the two rails of the DAC output, one can derive:

$$V_{\text{OUT,diff,peak}-\text{peak}} = \text{vdd} \cdot (\frac{1}{2} - (-\frac{1}{2}) = \text{vdd}. \tag{3.29}$$

For the target application of $V_{\text{OUT,diff,peak}-\text{peak}} > 1\,\text{V}$ in this work, it is possible to conclude that the minimum supply voltage to use for such SST architecture is 1 V. However, there are other design considerations regarding PVT calibration discussed in the next subsection, which lowers down the differential output voltage level. Hence to compensate for the drop in the differential output voltage level, the supply voltage is increased to 1.2 V.

The supply current and the output voltage are plotted across the digital input code shown

if Fig. 3.16(a) and Fig. 3.16(b), respectively. It is assumed for a 9-bit DAC with a supply voltage of 1.2 V in this plot.



(a) (b)

Figure 3.16: The power supply current (a) and the DAC output voltage (b) across digital input code.

Switch Operating Region

So far, the non-linear behavior of the SST DAC is studied assuming the switches are perfectly linear. However, the drain-source voltage of the switches is data-dependent and introduces a first-order non-linearity, which is considered in the following model.

The minimum and maximum drain-source voltage variation of the switches is derived as a function of r_{RM} showing the range which switch is operating across the digital input code

$$V_{\mathrm{DS,min}} = \frac{\mathrm{vdd}}{4\,(r_{\mathrm{RM}}+1)}\ ,\ V_{\mathrm{DS,max}} = \frac{3\cdot\mathrm{vdd}}{4\,(r_{\mathrm{RM}}+1)}. \tag{3.30}$$

It becomes clear that the smaller the ratio r_{RM}, the larger the V_{DS} variation across the digital input code. Therefore, choosing a lower r_{RM} ratio, the operating region of the switches moves toward the saturation region, causing more non-linear on-resistance of the switch, as shown in Fig. 3.17. The on-resistance model, introduced in Eg. 3.20 can be rewritten to add the drain-source voltage dependency as:

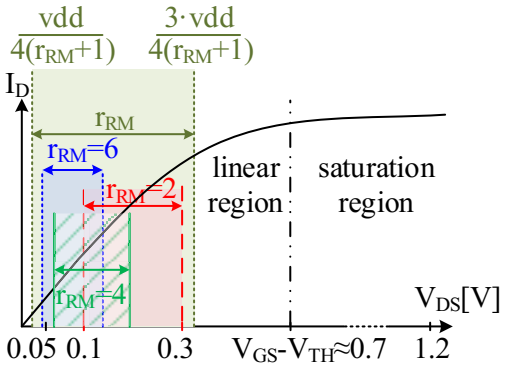


Figure 3.17: The I-V curve of a MOSFET switch highlighting The operating region of the switches with different r_{RM}.

$$R_{\mathrm{on}} = \frac{1}{\mu C'_{\mathrm{ox}} \left(\frac{W}{L}\right) \left(V_{\mathrm{GS}} - V_{\mathrm{TH}} - \frac{V_{\mathrm{DS}}}{2}\right)} \tag{3.31}$$

where $0 < V_{\mathrm{DS}} < (V_{\mathrm{GS}} - V_{\mathrm{TH}})$. It can be rearranged as:

$$R_{\mathrm{on}} = \frac{\frac{1}{\beta \cdot V_{\mathrm{od}}}}{1 - \frac{V_{\mathrm{DS}}}{2V_{\mathrm{od}}}} = \frac{1}{\beta \cdot V_{\mathrm{od}}} \cdot \frac{1}{1-u} \tag{3.32}$$

where $\beta = \mu C'_{\mathrm{ox}} \left(\frac{W}{L}\right)$, $V_{\mathrm{od}} = V_{\mathrm{GS}} - V_{\mathrm{TH}}$ and $u = \frac{V_{\mathrm{DS}}}{2V_{\mathrm{od}}}$. Applying a Taylor series expansion on Eq. 3.32, one obtains

$$R_{\mathrm{on}} = \frac{1}{4\beta V_{\mathrm{od}}^3} \cdot V_{\mathrm{DS}}^2 + \frac{1}{2\beta V_{\mathrm{od}}^2} \cdot V_{\mathrm{DS}} + \frac{1}{\beta V_{\mathrm{od}}} \tag{3.33}$$

and

$$\frac{W}{L} = \frac{\frac{1}{4V_{\mathrm{od}}^3} \cdot V_{\mathrm{DS}}^2 + \frac{1}{2V_{\mathrm{od}}^2} \cdot V_{\mathrm{DS}} + \frac{1}{V_{\mathrm{od}}}}{\mu C'_{\mathrm{ox}} \cdot R_{\mathrm{MSB}} / (r_{\mathrm{RM}} + 1)}. \tag{3.34}$$

Finally, minimizing the W/L (decrease active device area and in addition to that its gate capacitance), the overdrive voltage V_{od} should be maximized, and r_{RM} should be minimized.

To calculate the INL error of the DAC for different r_{RM} ratios, the W/L ratio of the switches is calculated and replaced in R_{on} devices modeled in Fig. 3.15.

In order to calculate the W/L ratio based on Eq. 3.34, $\mu_{\mathrm{P}} C'_{\mathrm{ox}} = 20\,\frac{\mu\mathrm{A}}{\mathrm{V}^2}$ and $\mu_{\mathrm{N}} C'_{\mathrm{ox}} = 40\,\frac{\mu\mathrm{A}}{\mathrm{V}^2}$ for PMOS and NMOS devices are assumed, respectively. Furthermore, V_{DS} assumed in Eq. 3.34, is for middle of the digital input code, D=256. At this point, the output differential voltage is approximately zero and the voltage on each of the outputs is half of the supply voltage. In this case, one can derive:

$$V_{\mathrm{DS,D=256}} = \frac{1.2}{2 \cdot (1 + r_{\mathrm{RM}})} \tag{3.35}$$

where vdd = 1.2 V.

The calculated W/L ratio for each NMOS and PMOS devices with

$r_{\mathrm{RM}} = 2$:

$$(W/L)_{\mathrm{P}} = 47, (W/L)_{\mathrm{N}} = 23.5 \tag{3.36}$$

,$r_{\mathrm{RM}} = 4$:

$$(W/L)_{\mathrm{P}} = 94, (W/L)_{\mathrm{N}} = 47 \tag{3.37}$$

and $r_{\mathrm{RM}} = 6$:

$$(W/L)_{\mathrm{P}} = 188, (W/L)_{\mathrm{N}} = 94. \tag{3.38}$$

The obtained INL error for $r_{\mathrm{RM}} = 2$, $r_{\mathrm{RM}} = 4$ and $r_{\mathrm{RM}} = 6$ is depicted in Fig. 3.18 with the peak-peak INL error of 1.92 LSB, 0.97 LSB and 0.65 LSB, respectively. Furthermore, the DNL error with the single ended output impedance of each of the differential outputs for $r_{\mathrm{RM}} = 2, 4$ and 6 are depicted in Fig. 3.19, Fig. 3.20 and Fig. 3.21, respectively.

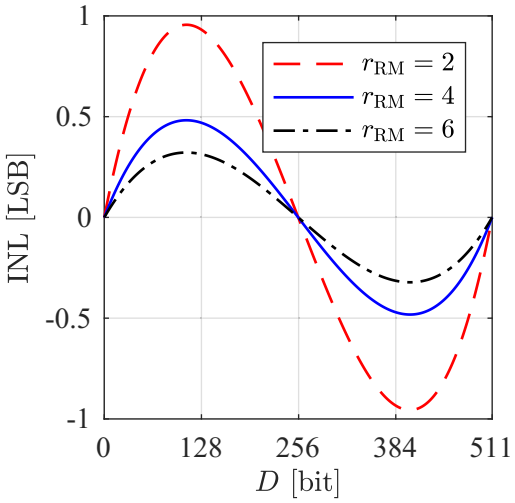
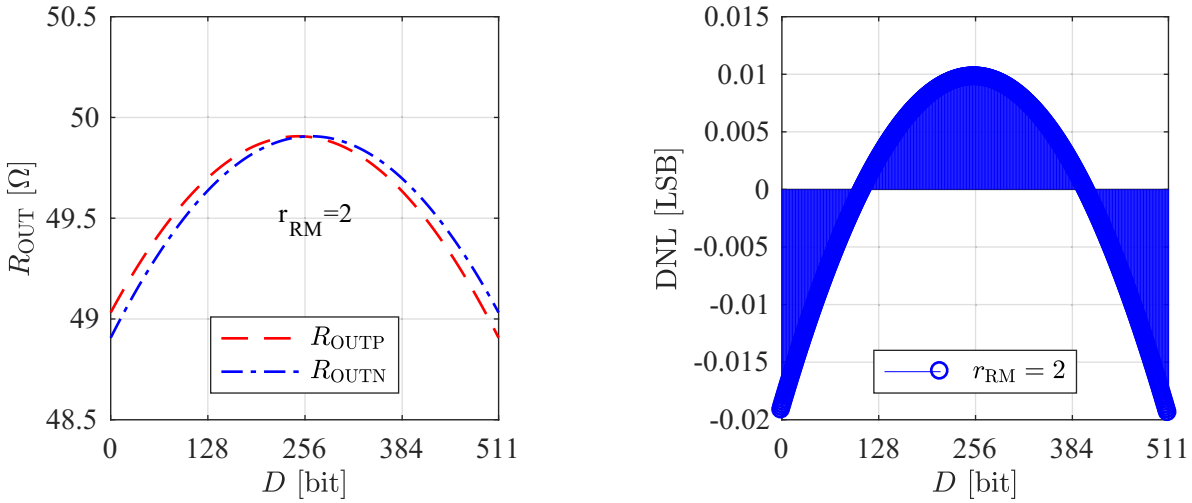


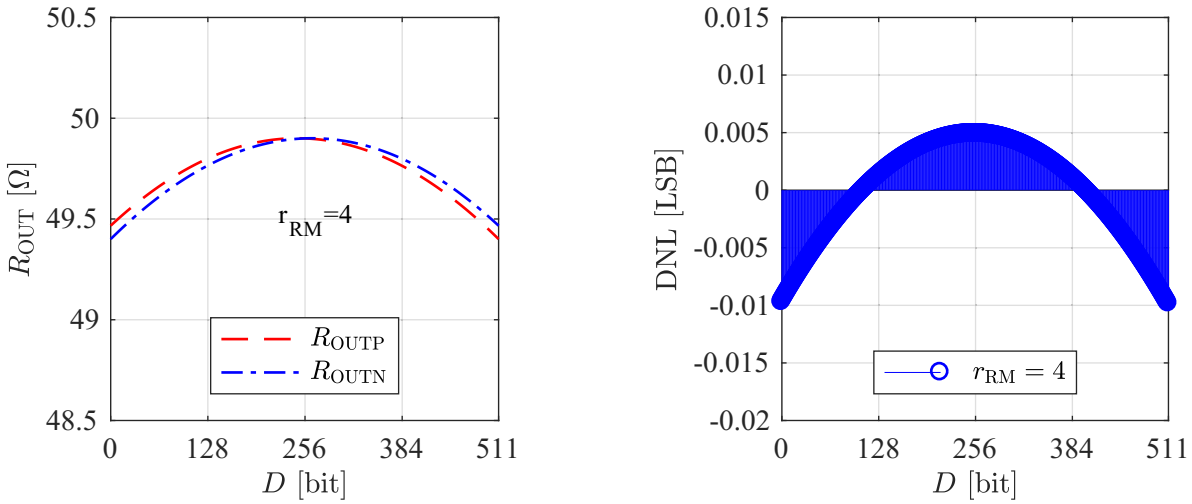
Figure 3.18: INL error of the SST DAC across $r_{\mathrm{RM}} = 2, 4$ and 6 with the peak-peak INL error of 1.92 LSB, 0.97 LSB and 0.65 LSB, respectively.

The choice of the ratio r_{RM} comes with the trade-off between power/area and non-linearity. Moreover, the size of the switches defines as well the input capacitance for the pre-driver stage. The larger the input capacitance, the slope at the gate of the active switches within the SST unit, limits the output is settling as well, which at high-frequency operation, can



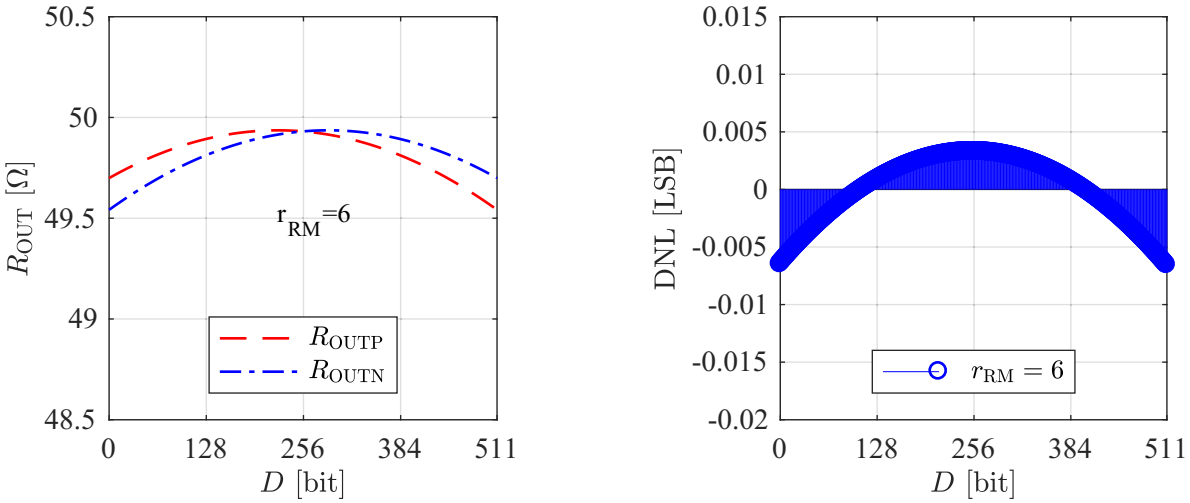
(a) (b)

Figure 3.19: Single ended termination impedance of the differential output (a) and the DNL error (b) across digital input code with $r_{\mathrm{RM}} = 2$.



(a) (b)

Figure 3.20: Single ended termination impedance of the differential output (a) and the DNL error (b) across digital input code with $r_{\mathrm{RM}} = 4$,.



(a) (b)

Figure 3.21: Single ended termination impedance of the differential output (a) and the DNL error (b) across digital input code with $r_{\mathrm{RM}} = 6$,.

make the settling at the outputs slower. In turn, a lower slope makes the eye of the PAM modulated signal via the DAC smaller.

QFN Packaging Effect on Power Supply

Given the data-dependent current drawn from the power supply of the SST DAC, the power supply impedance becomes critical. The power supply impedance is a compound of the combination of the on-chip, off-chip, and the electrical connection between the two. Off-chip effects where the power supply is connected from the printed-circuit-board (PCB) are neglected here since it is assumed big off-chip discrete decoupling capacitors mitigates the effects.

The connection between the chip and PCB is defined by the package. To lower down the cost, weight, and size of the packaging, making this solution a more efficient solution for the automotive industry, quad flat no-lead (QFN) packages are favorable to high-performance alternatives such as ball grid array (BGA) [16]. However, operating at higher operational speed, the parasitics and bond wires of QFN packages can limit the linearity of the SST DAC. Therefore, the parasitics and bond wires of the QFN package are modeled to study their effect and optimizing the linearity performance. A QFN-60 package is considered with a cavity size of 5.3 mm × 5.3 mm and a die size of 2.5 mm × 2 mm. The gold bond wires assumed to have an average length of 2 mm with diameter of 30.48 μm.

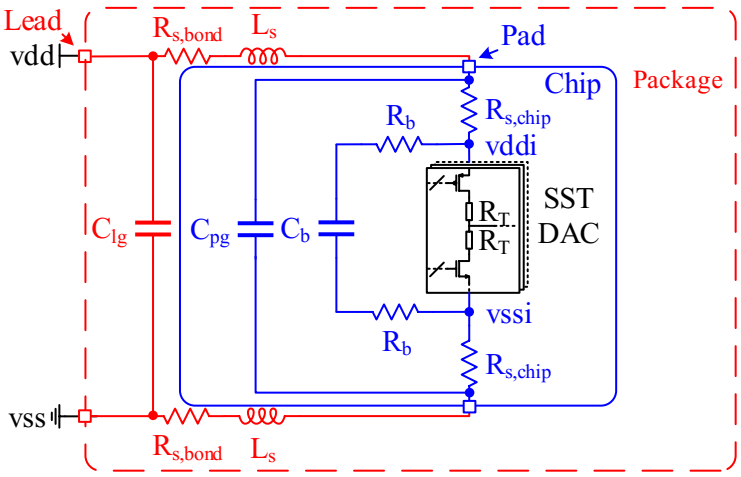


Figure 3.22: The circuit schematic of the SST DAC model with a simplified circuit model of the supply impedance mesh including on-chip series resistance $R_{\mathrm{s,chip}}$ and bond wire impedance $R_{\mathrm{s,bond}}$ and L_{s}.

A simplified circuit schematic of the supply impedance mesh, including on-chip and bond wire parasitics, is shown in Fig. 3.22. The bond wire connecting the external power supply vdd at the lead to the pad is modeled with a series inductance L_{s} and series resistance $R_{\mathrm{s,bond}}$. The on-chip supply impedance from the pad to the switches within the SST unit is modeled with a series resistor $R_{\mathrm{s,chip}}$ which sum up the resistance due to the solder connection at the pad as well as the on-chip supply mesh connecting the pads to the DAC.

The capacitors C_{lg} and C_{pg} are the parasitic capacitors connecting lead to ground and pad to ground, respectively. However, these parasitic capacitors are negligible comparing to the off-chip and on-chip decoupling capacitors. The decoupling capacitor C_{b} is integrated on-chip to mitigate the dynamic effects on the on-chip power supply due to the transient crow-bar current as well as the data-dependent current drawn by the SST unit. These capacitors are placed as close as possible to the core of the SST DAC. But, due to the impedance of integrated impedance mesh and vias, a series resistance of R_{b} is modeled across the decoupling capacitor C_{b}.

The transfer function of the on-chip to off-chip power supply can be written as:

$$\frac{\mathrm{vddi}-\mathrm{vssi}}{\mathrm{vdd}-\mathrm{vss}}(s)=\frac{R_{\mathrm{SST}}\parallel(R_{\mathrm{b}}+\frac{1}{C_{\mathrm{b}}s})}{R_{\mathrm{SST}}\parallel(R_{\mathrm{b}}+\frac{1}{C_{\mathrm{b}}s})+R_{\mathrm{s}}+L_{\mathrm{s}}s} \tag{3.39}$$

where R_{SST} is the modelled resistance of the SST driver and can vary from $100\,\Omega$ to $200\,\Omega$ as a function of the digital input code. R_{s} is the sum of series resistances of $R_{\mathrm{s,bond}}$ and $R_{\mathrm{s,chip}}$. After simplification, the transfer function is

$$\frac{\text{vddi} - \text{vssi}}{\text{vdd} - \text{vss}}(s) = \frac{s \cdot R_\text{b} + \frac{1}{L_\text{s} C_\text{b}}}{s^2 + s \cdot \frac{R_\text{s}+R_\text{b}}{L_\text{s}} + \frac{1}{L_\text{s} C_\text{b}}}. \tag{3.40}$$

To simplify this third order low pass filter (LPF) transfer function, the location of the zero s_Z is allocated as

$$s_\text{Z} = -\omega_\text{Z} = -\frac{1}{R_\text{b} L_\text{s} C_\text{b}}. \tag{3.41}$$

This zero is much higher than the resonance frequency of $L_\text{s}C_\text{b}$ and can be neglected. By comparing the transfer function with a standard second-order RLC LPF

$$\frac{\frac{1}{L_\text{s} C_\text{b}}}{s^2 + s \cdot \frac{R_\text{s}+R_\text{b}}{L} + \frac{1}{L_\text{s} C_\text{b}}} = \frac{\omega_0^2}{s^2 + s \cdot 2\zeta\omega_0 + \omega_0^2} \tag{3.42}$$

the natural frequency ω_0 and the damping ratio ζ is derived as

$$\omega_0 = \sqrt{\frac{1}{L_\text{s} C_\text{b}}} \quad \& \quad \zeta = \frac{R_\text{s} + R_\text{b}}{2} \cdot \sqrt{\frac{C_\text{b}}{L_\text{s}}}. \tag{3.43}$$

The resonance frequency defined by L_s and C_b. The use of the QFN package limits optimizing the inductance of the bond wire as for a 2 mm of the gold bond wire, its expected an inductance of 2 nH. The decoupling capacitor C_b is maximized to mitigate the dynamic effects of transient current drawn from the supply, and, based on the area available on the die, an approximate value of 200 pF is expected. However, to optimize the linearity of this transfer function is possible to increase the damping factor.

The parameters R_s and R_b defined by the parasitics of the package and on-chip supply mesh can be studied to see manipulating their value to increase it with on-chip techniques can improve this damping factor. A technique is proposed in [14] utilize the parasitics of R_b to increase from approximately 10 fold to increase the damping factor and therewith increasing linearity. However, increasing R_b decouples the capacitor C_b from the power supply, which in turn makes its decoupling effect weak.

The next possible option is to increase R_s. This impedance is composed of $R_\text{s,bond}$ and $R_\text{s,chip}$. A technique is presented in [15] to use this resistor to cancel the non-linearity of the switches by adding a non-linearity with the reverse effect. This technique is discussed in detail in the next subsection.

Source Degeneration

In order to study the static effect of the series source impedance on the non-linearity of the SST DAC, the equivalent resistive model is shown in Fig. 3.23. In this model, the inductance of bond wires L_s and decoupling capacitor C_b are excluded from studying

frequency-independent effects of the supply series impedance. To simplify the analysis, only the series impedance on vdd is shown. However, splitting it in half and placing it on both rails does not change the result. Furthermore, since the voltage drop on R_s makes the internal positive supply directly at the SST DAC different from the external supply, it is named as vddi.

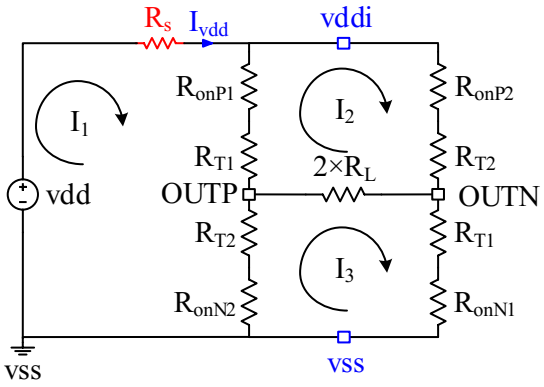


Figure 3.23: The equivalent resistive model of the SST DAC with series source impedance of R_s.

In this case, only one of the KVL loops which were derived previously based on Fig. 3.15 changes and can be rewritten as:

$$I_1 : \mathrm{vdd} + I_\mathrm{vdd} \cdot R_s + (I_\mathrm{vdd} - I_2) \cdot (R_{onP1} + R_{T1}) + (I_\mathrm{vdd} - I_3) \cdot (R_{onP2} + R_{T2}) = 0. \quad (3.44)$$

Solving the three KVL loops with this change yields the supply current as:

$$I_\mathrm{vdd} = \mathrm{vdd} \cdot \frac{-D^2 + (2^N - 1)D + (2^N - 1)^2/4}{R_\mathrm{L} \cdot (2^N - 1)^2 + R_\mathrm{s} \cdot (-D^2 + (2^N - 1)D + (2^N - 1)^2/4)}. \quad (3.45)$$

The internal supply voltage level vddi can be then calculated as:

$$\mathrm{vddi} = \mathrm{vdd} - R_\mathrm{s} \cdot I_\mathrm{vdd}. \quad (3.46)$$

It becomes evident that the inherent code dependent characteristic of the supply current in this SST DAC is present in the internal supply voltage level due to the code dependent voltage drop on R_s.

Looking at the static non-linearity of the SST DAC and assuming ideal switches without any voltage dependency on its drain-source, INL and DNL error can be calculated for $R_s = 0, 1\& \quad 2\,\Omega$ and is plotted in Fig. 3.24 and Fig. 3.25, respectively.

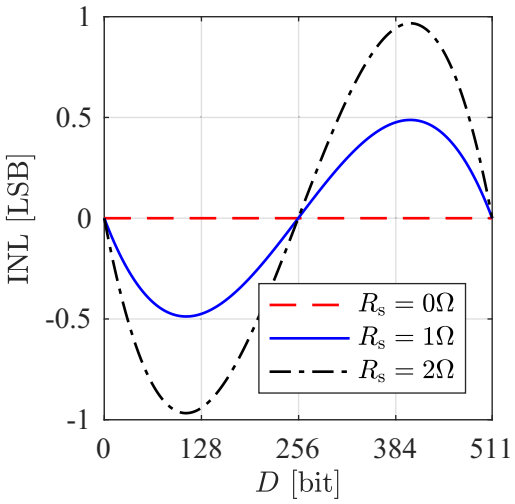


Figure 3.24: INL error of the SST DAC with ideal switches but non-zero series supply impedance R_s.

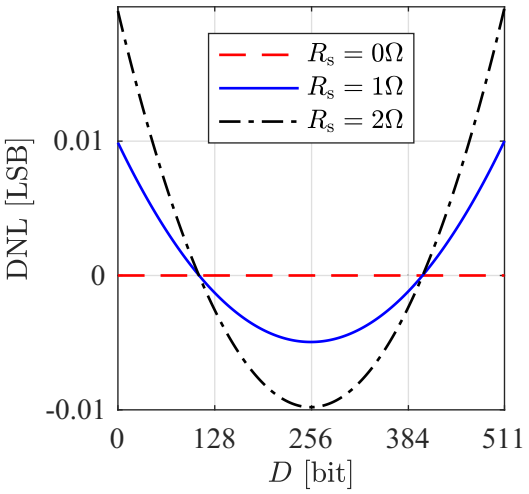


Figure 3.25: DNL error of the SST DAC with ideal switches but non-zero series supply impedance R_s.

Looking at the 3rd order non-linearity of the INL error in Fig. 3.24 and Fig. 3.18, one can

see the reverse polarity of the curves. In one case, there is no supply impedance but with non-ideal switches as in Fig. 3.18 and in the other case, ideal switches but with non-zero series supply impedance as in Fig. 3.24.

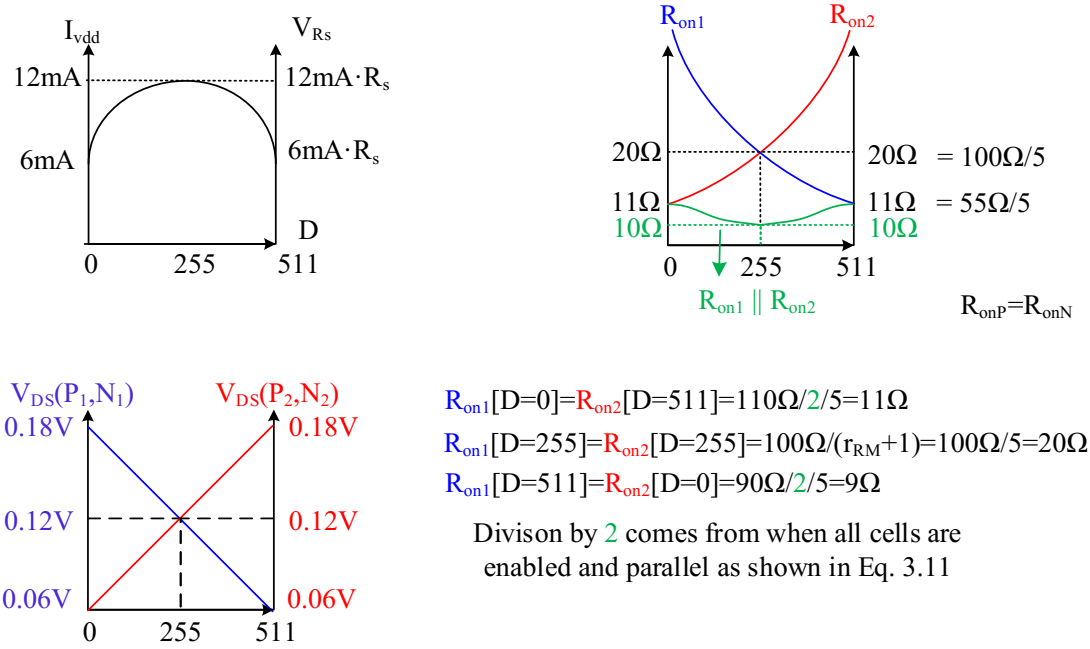


Figure 3.26: Simplified SST model with series supply resistance, showing the parabolic behaviour of the voltage drop on supply series resistance and $R_{on1} \parallel R_{on2}$ of the termination switches on each of the outputs. In this model, a 9-bit SST DAC with the supply voltage is 1.2 V and nominal R_{on} in the MSB cell (calculated in Eq. 3.18 with r_{RM}=4) is equal to 20 Ω.

This qualitative comparison suggests that series supply impedance can mitigate the non-linear switch effect on the overall INL error. To quantitatively calculate the series supply impedance R_s in an SST DAC with non-ideal switches to cancel out the R_{on} voltage dependency non-linearity, one has to look at R_{on} variation across the digital input code D.

The switches are sized to have the nominal impedance at the mid-code. Still, towards minimum or maximum code D, the enabled switches will experience a higher V_{DS}, therefore a higher R_{on}. This, in turn, increases the voltage drop on enabled R_{on}, resulting in a lower DAC differential output voltage from the nominal value, fundamentally limiting the DAC linearity.

The parallel combination of the enabled switches $R_{on1} \parallel R_{on2}$ is highlighted in Fig. 3.26. To mitigate this effect, a series supply resistance R_s is used as shown in Fig. 3.23.

The voltage drop on R_s follows the same parabolic behavior as the supply current as shown in Fig. 3.16(a), with a lower voltage drop on the min. and max. code D, providing a higher internal rail-to-rail supply voltage (vddi-vss), increasing the DAC differential output, and thus canceling the non-linearity due to the R_{on} dependency on V_{DS}. Fig. 3.26 reveals the same parabolic behaviour of the $R_{on1} \parallel R_{on2}$, with reverse polarity, as the voltage drop on the supply series resistance V_{Rs}. Hence, equalising the peak-peak voltage drop variations on R_s and R_{on}, the added non-linearity through source degeneration technique cancels the inherent non-linearity caused by the switches as

$$R_s \cdot \Delta I_{vdd(D=0-255)} = \Delta R_{on(D=0-255)} \cdot \frac{I_{vdd(D=255)}}{2} \tag{3.47}$$

where the supply current variation ΔI_{vdd} and the slice impedance variation ΔR_{on} are from $D = 0$ to $D = 255$ and is equal to 6 mA and 1 Ω, respectively. The current on all enabled slices at mid-code D is half the full-scale current and is equal to 6 mA. The supply and ground series resistance of R_s =1Ω is then calculated and realized with the careful layout of the supply mesh, including all impedance parasitics of metal routing down to the source of the switches.

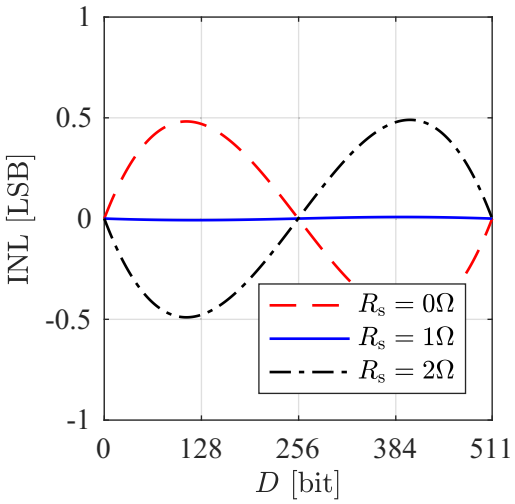


Figure 3.27: INL error of the SST DAC with non-ideal switches with $r_{RM} = 4$ and with non-zero series supply impedance R_s.

In order to verify the calculated $R_s = 1\,\Omega$ based on Eq. 3.47, the model shown in Fig. 3.23 with non-ideal switches and sweeping R_s is plotted in Fig. 3.27. It is shown that $R_s = 1$ which is the sum of all impedances on the power supply rail cancels out the non-linearity of the switches with $r_{RM} = 4$.

The design of Rs should be done by the careful layout of the top-level power mesh bringing it down to the switches.

3.4.4 PVT Problems and Solutions

The termination impedance of SST DAC is the compound of on-chip active and passive devices. The devices contributing to the output termination, poly resistors, and MOS devices vary across process corners and temperature variation, changing its impedance characteristic.

In order to guarantee an efficient power transmission to the channel, the SST DAC impedance should match within a defined range of deviation. This includes temperature ranging from $-40°C$ to $+80°C$ and process corners of $\pm 3\sigma$ from slow-slow (SS) corner to fast-fast (FF) corner. This deviation from the perfect matching increases the return loss, which can violate the return loss limit line defined by IEEE 802.3 standards discussed in Sec. 2.3.4. Therefore, a calibration technique to match the impedance is necessary. A set of possible techniques to overcome this problem is presented in [17] and summarized here.

Body Biasing of the Switches

The use of the flip well in GF22 technology enables a wide range of biasing the bulk voltage of the switches shown in Fig. 3.28. The bulk-source voltage can be biased from $V_{\mathrm{BS,P}} = -2\,\mathrm{V} - \mathrm{vdd}$ to $0\,\mathrm{V}$ for the PMOS and $V_{\mathrm{BS,N}} = -\mathrm{vdd}$ to 2V for the NMOS. Changes on the bulk of the switches can, in turn, change the threshold voltage of the MOS devices as

$$V_{\mathrm{TH}} = V_{\mathrm{TH,fb}} + \gamma[\sqrt{2\Phi_S - V_{\mathrm{BS}}} - \sqrt{2\Phi_S}] \tag{3.48}$$

where $V_{\mathrm{TH,fb}}$ is the forward-biased threshold, Φ_S is the surface potential in strong inversion and γ is the body-effect coefficient. The change in the threshold voltage of the MOS device changes its current, which modifies the on-resistance as shown in Eq. 3.20. Therefore, it shows the reverse square relation of the on-resistance to the bulk-source voltage $R_{\mathrm{on}} \propto \frac{1}{\sqrt{V_{\mathrm{BS}}}}$. This impedance variation is only possible on the active portion of the termination.

The termination in the design of the SST DAC is divided between the passive and active devices with a ratio of r_{RM}. Therefore, choosing a larger r_{RM} limits the impedance variation on the switches and therewith the termination impedance. This comes as a trade-off between linearity and the use of the body-biasing technique. In [17] shows that the use of body-biasing for the SST DAC suitable for the application of this work only covers $\pm\sigma$ of the process variations. The simulation data showing the process and temperature impedance variation for the implemented SST DAC is shown in Sec. 4.4.

Digital Cell Calibration

A conventional technique of canceling the variation of the MOS switches is to place an array of binary-weighted switches as shown in Fig. 3.29 [18]. It is shown in [17] that the use of

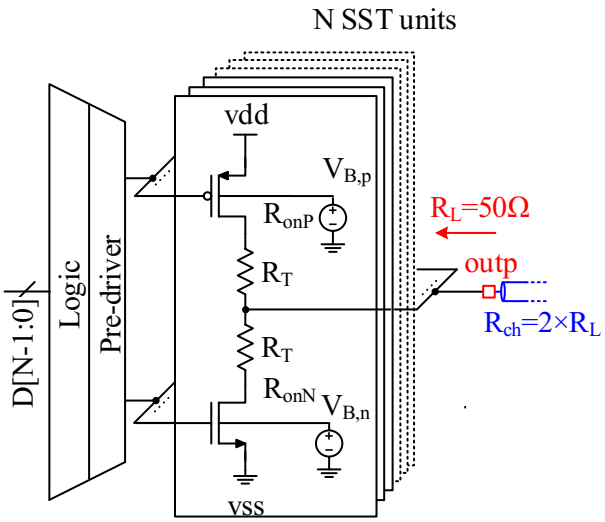


Figure 3.28: The circuit schematic of an N-bit SST DAC with body biasing of the switches.

this technique with the use of three binary weighted coded switches enables an impedance calibration over a full range of $\pm 3\sigma$ process corner variation and temperature variation. The main drawback of this technique is the limiting of settling behavior by adding more switches in the push-up and pull-down path. The extra parasitic added not only slows down the settling behavior limiting the operating frequency but also can create asymmetry between unit cells which in turn increases the mismatch between the unit cells.

Parallel Branches

The other approach is the use of weighted parallel branches in parallel to the main DAC as shown in Fig. 3.30. In this approach, the N_{PB} weighted branch is connected in parallel to each of the outputs and statically controlled. The parallel branches enabled are constantly consuming a static current, which comes as a drawback of using this technique. Moreover, the parallel branches lower down the peak-peak output voltage as well. However, on the other hand, the constant flow of static current in parallel can improve the linearity of the DAC, both statical (INL) and dynamical (SFDR).

The use of the parallel branches lowers down the peak-peak voltage variation and reduces voltage variation on the switches, which in turn mitigates its non-linear effect. Moreover, a constant flow of current drawn from the supply helps to lower the effect of transient current spikes drawn from supply due to the crow-bar current of the unit cells within the main DAC. In Sec. 4.4 a careful design of the parallel branches is studied, and the advantages and disadvantages of this technique are shown numerically based on the implemented design and simulated.

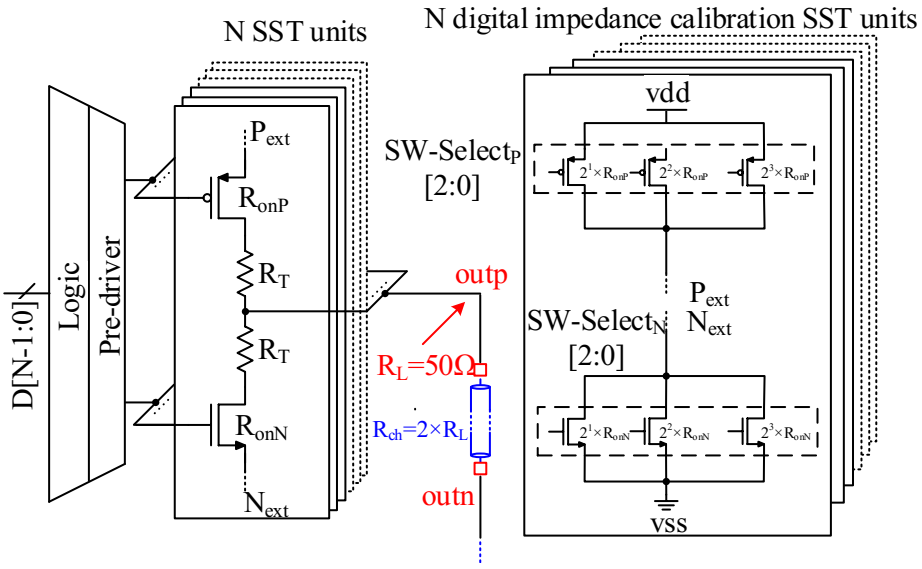


Figure 3.29: The circuit schematic of an N-bit SST DAC showing the digital impedance calibration of 3 binary switches in series to each side of each SST unit.

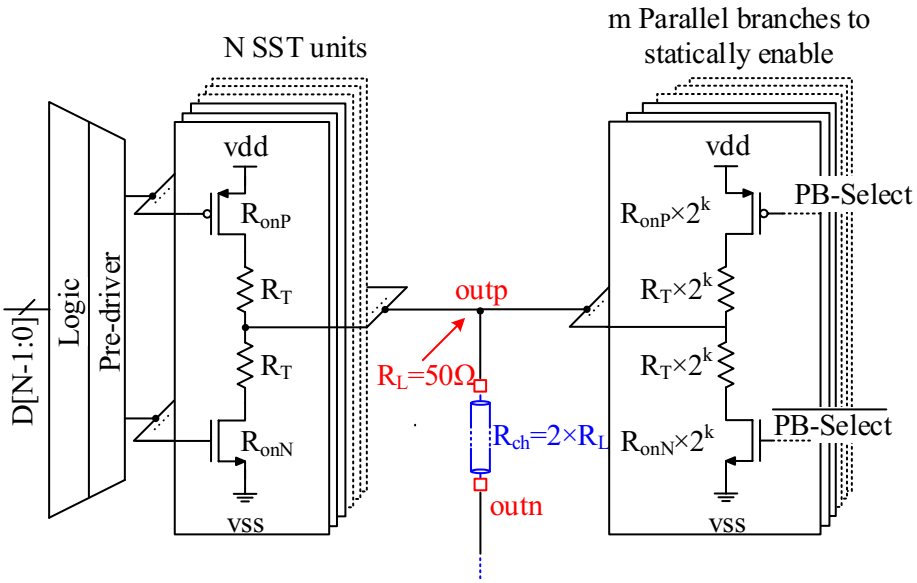


Figure 3.30: The circuit schematic of an N-bit SST DAC with m binary weighted parallel branches.

3.4.5 Ground Scheme Problem

The supply mesh impedance in SST DAC is a dominant factor limiting the performance. The noise which is generated on the power supply can modulate into the output voltage, causing distortion. To minimize the effect of this noise, not only the use of closely

implemented decoupling capacitors is considered, but also recognizing noisy blocks and separating their supply. Therefore to ideally remove the digital noise modulating on the output voltage, a separate ground supply named avss and two core and I/O supply voltage of avdd and avdd12, respectively is introduced. All critical blocks are supplied with these supplies. In contrast, the rest of the blocks are supplied with a digital supply rail named dvss for the digital ground and dvdd and dvdd12 for core and I/O supply voltages, respectively. The distribution of such a supply scheme is discussed in detail and highlighted in the implemented DAC in Sec. 4.1.1.

3.5 SST Echo cancellation

One of the main challenges of true full-duplex operation is that the received signal, which is highly attenuated on the 10m UTP/STP, should be detected with a BER less than 1E-12 while simultaneously superimposed with the full-scale transmit signal on the same line. Therefore, the use of an active or passive hybrid is essential. The insertion loss of the TX signal is shown in Fig. 2.9 shows a worst-case insertion loss of 18 dB for 10GBase-T1 standard.

The echo cancellation type intended to be used in this work is a linear cancellation. Non-linear cancellation has a better performance but comes with considerable complexity in the implementation [19] which is out of the scope of this work. Although linear cancellation demand a high linearity requirement on the TX DAC used to drive the line.

3.5.1 Requirements

The SNDR after the analog front-end (AFE) and post echo cancellation based on the system analysis should be at least 20 dB. This estimation is based on the operation of PAM4 modulation on a 1 V peak-peak differential signal achieving a BER less than 1E-12 on the transceiver.

The main noise sources contributing to the received signal are a residual echo, alien cross talk, and inherent AFE device noises. If it is assumed that each of these noise sources contributes equally, it can be concluded that the residual echo should be approx. 5 dB lower than the noise limit.

Therefore, the echo cancellation needs to cancel 43 dB (18 dB (IL) + 20 dB (SNDR) + 5 dB (noise share)) of the transmit signal at the receiver to achieve the target BER. Also, a highly linear TX-DAC coupled with a well-matched transmit signal is required to maximize the post hybrid linearity.

3.5.2 Passive vs Active Hybrid

There are two possible ways to implement this hybrid interface using passive and active elements shown in Fig. 3.31 and Fig. 3.32, respectively.

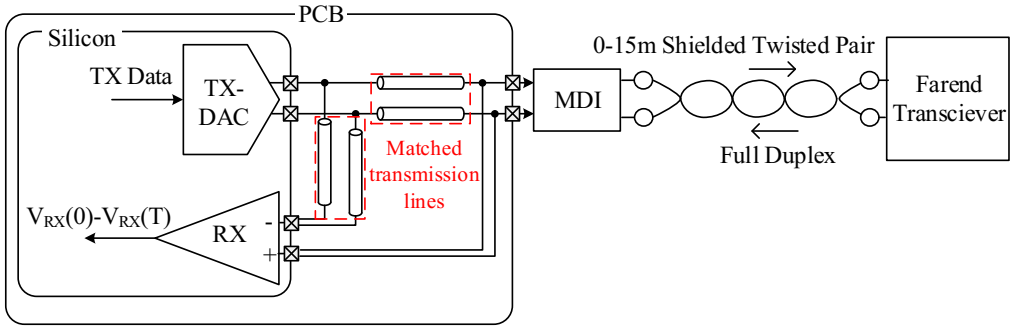


Figure 3.31: Hybrid architecture using passive PCB traces [20].

The use of passive hybrid implementation requires the use of long traces of matched transmission lines. The main drawback of using this technique is the big size of PCB implementation, especially for automotive applications, where the area and weight of the solution is a critical point. Moreover, the use of PCB traces increases the parasitic capacitors on the DAC output, which limits the operating speed of the DAC. Furthermore, the use of the transmission lines increases different parasitic capacitance at the output of the TX-DAC, at the MDI, and at the Input of the RX, which in turn creates mismatched slopes on the settling of the signal. This requires using passive elements to match these slopes to minimizing the residual error but with the cost of further increasing parasitic capacitance at the nodes mentioned above.

On the other hand, using an active hybrid solution lowers down the area consumed compared to the passive solution. The parasitic capacitors on the traces are substantially smaller than long PCB traces in a passive hybrid solution, which does not limit the slope of the transmit signal. However, this active solution uses an extra DAC that doubles power consumption on the transmit side. Furthermore, the use of EC-DAC requires a well-matched layout to be sensitive to static and dynamic mismatch effects between both DACs as well as matched output bandwidth. Therefore, to match the EC- and TX-DAC, careful design in input data timing should be applied to satisfy these challenges.

3.5.3 Analog vs Digital Echo Canceller

However, due to the inherent mismatch between the TX and EC signal as well as the error added due to the non-linearity of the adder shown in Fig. 3.32, residuals of the TX signal with much lower amplitude are present at the input of the RX. To better cancel out these

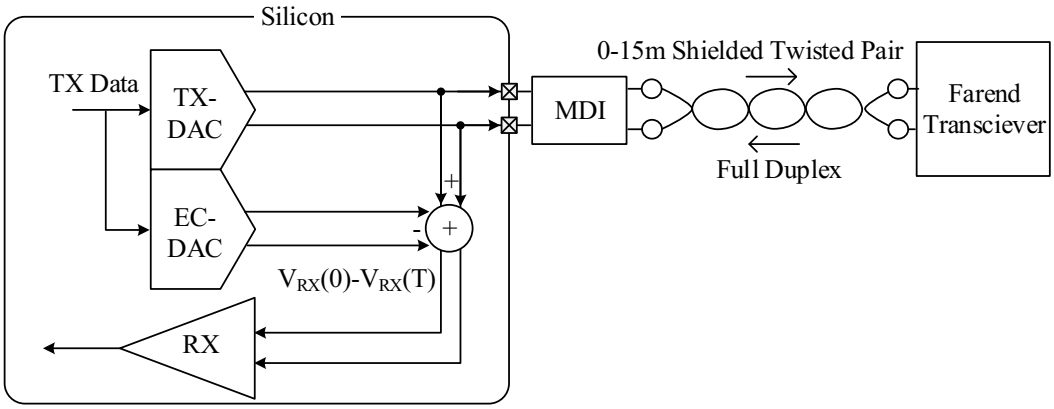


Figure 3.32: Dedicated EC-DAC used to perform hybrid function.

echo residuals, one can remove it in the analog domain and the digital domain as shown in Fig. 3.33 and Fig. 3.34, respectively. In this approach, in order to match the impedance of the TX-DAC and EC-DAC, the layout of each of their unit cells are placed as close as possible to minimize the impedance mismatch due to process variation.

An extra EC-DAC named here EC-DAC B is placed in the analog domain, which receives the TX data through an adaptive FIR filter. In this approach, EC-DAC B can be implemented with a lower resolution than the main DAC to save the use of the silicon area and power consumption. However, the lower the resolution, the more is the remaining residual at RX. Furthermore, the use of the FIR filter can be either a single-tap and multi-tap. The use of multi-tap comes with an advantage of better cancellation and therewith lower error residual but comes with the cost of extra silicon area and power consumption.

In the digital domain, the same technique is used but after RX. This lowers down the complexity of the design on the TX side of the PHY, as well as saving silicon area and power consumption. However, it increases the RX side requirement, demanding a higher SNDR on the ADC used in RX.

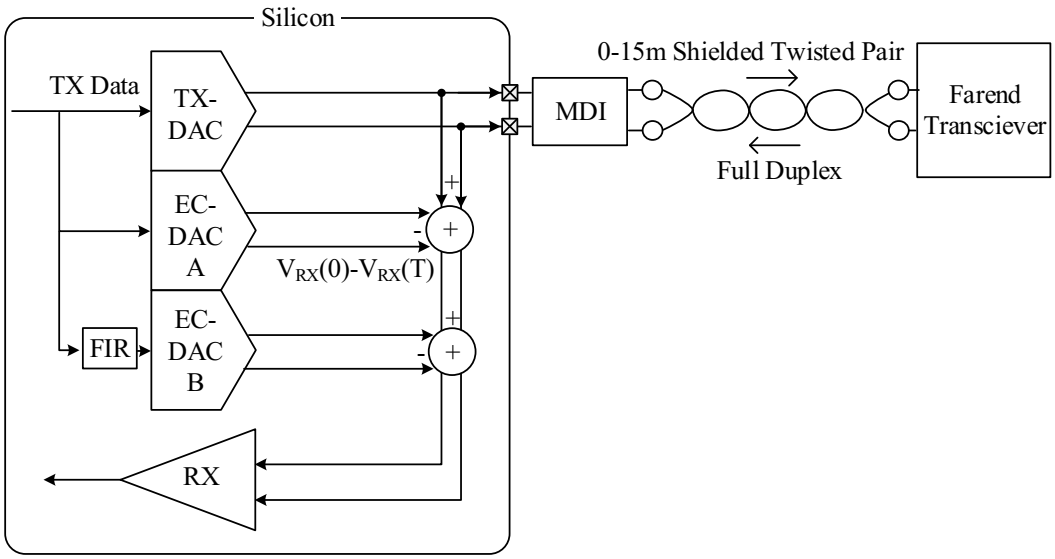


Figure 3.33: Dedicated EC-DAC B with and adaptive FIR filter used to remove TX residuals before RX [19].

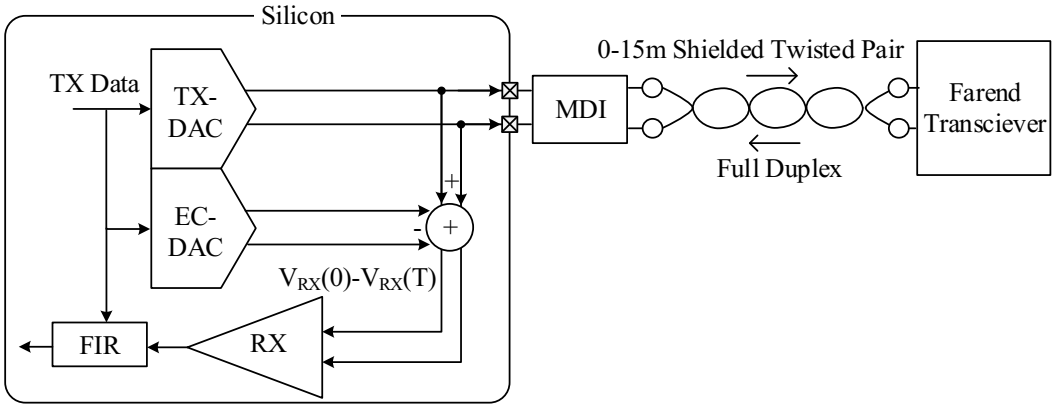


Figure 3.34: FIR Filter done on the digital domain after RX to remove the remaining TX residual.

4 Design and Implementation of a 9-bit 6GS/s Source Series Terminated DAC

In this chapter, the design aspects of the 9-bit SST DAC pair is discussed in detail. The high performance of such DAC is only enabled when taking into account these improvements in the design.

4.1 DAC Architecture

The top-level architecture of the DAC pair is shown in Fig. 4.1. 9-bit long input data (Di<8:0>), as well as the input clock signal (Clki), are the inputs of the main DAC pair block. The power supply levels have a range from the core voltage of 0.8 V and the I/O voltage level of 1.2 V. The input data first is decoded into unary-binary segmented data and level shifted from the core voltage to the I/O voltage. The input clock signal is buffered and phase tuned via a two-bit phase selection signal (SPI_PHB<1:0>). The four settings on the clock phase selector enable tuning the phase of the sampled data via first the latches. This way, it is guaranteed to sample the data once it settled, independent of the delay added due to level shifters and decoders. Having a higher range of phase selection can enable a better sampling point, however, the added complexity, area, and power consumption compromises the benefit of implementing it.

Furthermore, two latching stages (digital pre-latch and final analog latch) operating on opposite clock edges eliminate data-dependent delay variations and memory effects [21] originating from the binary-unary decoder, data level shifter, and latches.

Once the data is synchronized, the last buffer stage uses a pair of inverter for positive and negative inputs of the DAC pair.

4.1.1 Power Supply Implementation Scheme

The grounding scheme of the block is distributed into two analog and digital nodes, named avss and dvss, respectively. By separating the grounding scheme, the coupling of the supply noise due to the digital block switching is minimized. The main driver pair and pre-drivers, last latch stage, and the clock path that can directly couple the supply noise into the output signal spectrum share the same ground signal named avss. The rest of the digital signal

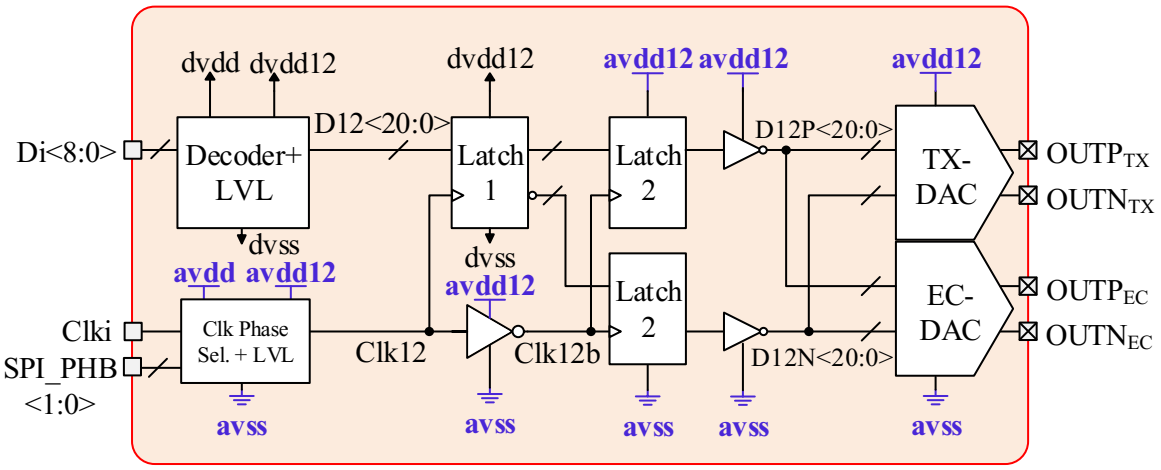


Figure 4.1: The top-level architecture of the 9-bit SST DAC pair, showing digital decoding and time synchronization scheme as well as power supply distribution across the architecture.

decoding and level shifting, as well as the first level of data synchronization by latch 1, share the same ground signal named dvss. The same power supply distribution strategy on the positive voltage levels is applied on both core and I/O voltage levels. Therefore, to follow the grounding scheme, the sensitive analog power supply signals are highlighted with blue color as shown in Fig. 4.1.

The analog power supply named as signals avdd12 and avss are sensitive to noise and can degrade the DAC performance. Moreover, the impedance of these supplies from the source to the supply rails on the chip and down to the source of the MOSFETs in the SST driver not only shows voltage drop due to the power drawn. It also shows other parasitics, such as inductance, which can affect the dynamic performance of the DAC across the frequency range. A detailed study of these effects is discussed in Sec. 3.4.3.

4.2 Unary and Binary Segmentation

The core architecture of the 9-bit SST TX-EC-DAC is segmented into a 4-bit unary and 5-bit binary. The 4-bit unary results in 15 unit cells. Thus, to compromise between the linearity and area/power consumption, 9-bit break down to 4-bit unary and 5-bit binary.

More unary bits result in a higher overall dynamic performance at the price of doubling the number of unit cells, which in turn increases the dynamic power consumption by driving double the number of gates and larger layout area, resulting in more parasitics due to the

long signal paths. Less unary cells, on the other hand, limits the dynamic linearity of the DAC. This can be caused by the large glitches while gating MSB cells at the Nyquist rate. Moreover, the matching between the unit cells of unary cells enables a better echo-canceling behavior between TX- and EC-DAC, which is discussed more in Sec. 4.5. On the other hand, binary cells have small device sizes, making them more prone to process mismatch. Therefore, one sees the trade-off in the design of the unary and binary segmentation to balance the linearity and hardware complexity [22].

However, if we consider the 4-bit unary and 5-bit binary SST DAC architecture as shown in Fig. 4.2, It's accurate to write:

$$\frac{1}{R_{\mathrm{L}}} = \frac{1}{R_{\mathrm{MSB}}} \sum_{i=1}^{5} (2^4 - 1) + 2^{-i} = \frac{15}{R_{\mathrm{MSB}}} + \frac{1}{2 \times R_{\mathrm{MSB}}} + ... \tag{4.1}$$

where the factor $(2^4 - 1)$ comes from the unary cells. Therefore the approximate value for R_{MSB} yields:

$$R_{\mathrm{MSB}} = (\sum_{i=1}^{5} 2^{-i} + 15) \times R_{\mathrm{L}} = 15.97 \times 50\,\Omega \approx 800\,\Omega. \tag{4.2}$$

4.3 Active to Passive Ratio

Given the detailed study of the passive to active impedance ratio r_{RM} discussed in Sec. 3.4.3, the ratio of $r_{\mathrm{RM}} = 4$ is chosen. For this ratio, the impedance of the switches and poly resistors is then given as:

$$R_{\mathrm{on}} = \frac{R_{\mathrm{MSB}}}{r_{\mathrm{RM}} + 1} = \frac{800\,\Omega}{5} = 160\,\Omega, \tag{4.3}$$

$$R_{\mathrm{T}} = \frac{r_{\mathrm{RM}} \times R_{\mathrm{MSB}}}{r_{\mathrm{RM}} + 1} = \frac{4 \times 800\,\Omega}{5} = 640\,\Omega. \tag{4.4}$$

The circuit schematic of the 9-bit SST TX-EC-DAC segmented into 4-bit unary and 5-bit binary is shown in Fig. 4.2. The power supply rails,avdd12i and avssi refers to internal power supplies. The EC-DAC is controlled with the same input digital signal as the TX-DAC here with differential input digital signal of D12P<20:0> and D12N<20:0>.

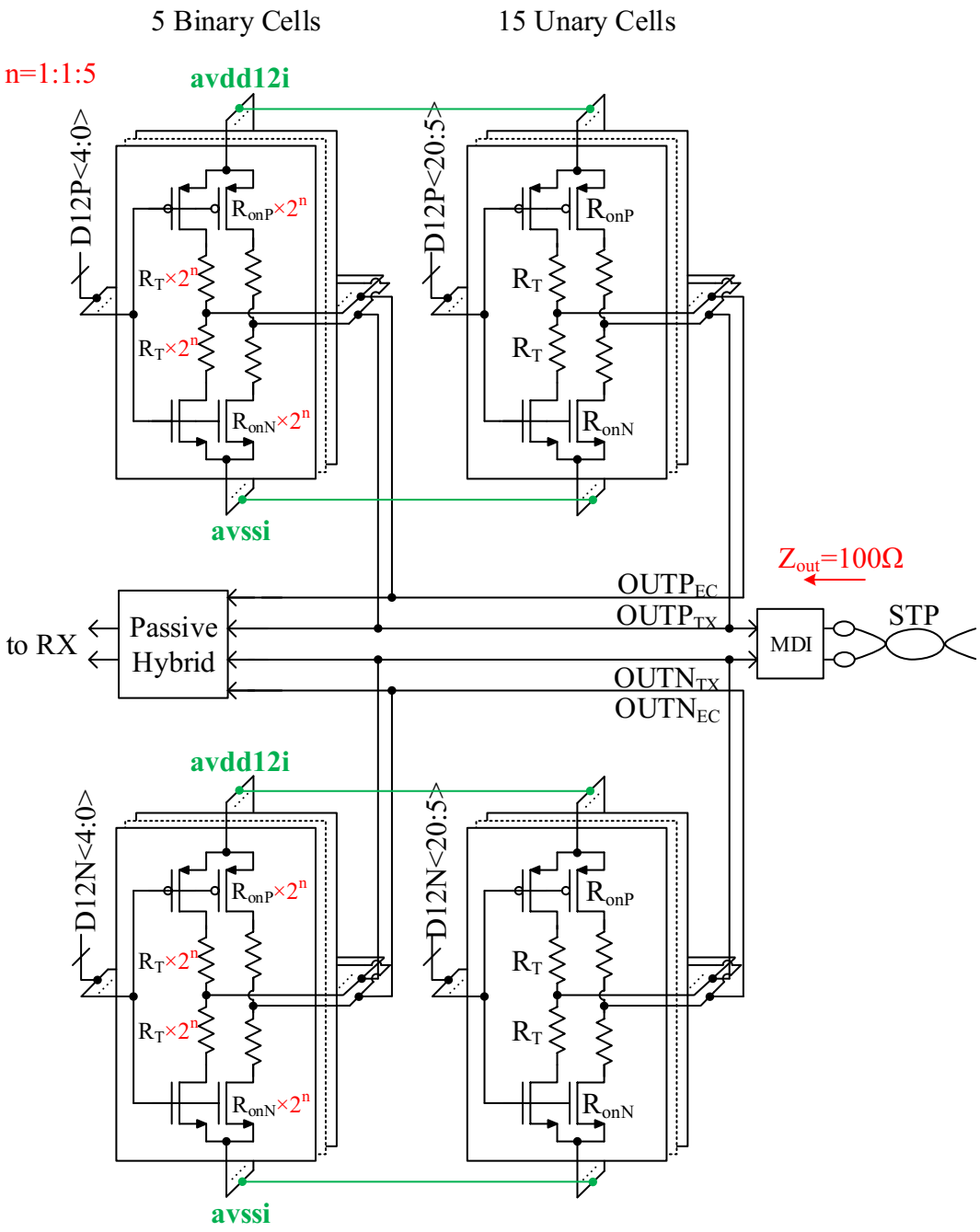


Figure 4.2: The circuit schematic of the 9-bit SST TX-EC-DAC segmented into 4-bit unary and 5-bit binary.

4.3.1 Crow-bar Current Reduction

One of the main changes to the general architecture of an SST DAC is shown in Fig. 3.13 is moving the termination resistor to the push-pull path. This resistor in the path reduces the crowbar current up-to 8 times compared to the conventional architecture, as shown in Fig. 4.3. The crowbar current peaks drawn during the transition at the gate of the switch and the use of QFN packages introducing bond wires to the power supply path introduce noise on the supply and the outputs. However, moving the termination resistor inside the push-pull path doubles the resistors needed to be implemented, increasing the silicon area and parasitics capacitance at the output node.

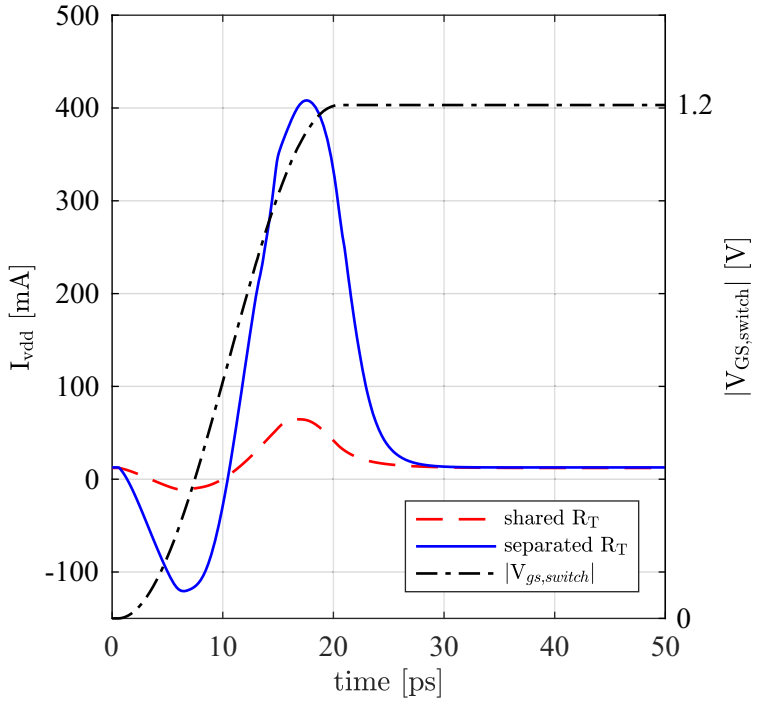


Figure 4.3: The crowbar current drawn from the supply, comparing the effect of using of termination resistor in and out of the push-pull path.

4.4 Termination Calibration

The termination of each of the outputs relies on the parallel combination of the sum of the impedance of active and passive devices. These devices vary across process corners and temperature variation, which changes the impedance of the devices and the termination impedance of the driver accordingly. Therefore, matching the termination between the driver and the channel is important as the better the impedance matching. The power

transmission between the driver and channel is more efficient, which minimizes the return loss caused at MDI and the channel that should be within the approved range as discussed in 2.3.4.

To calibrate for these variations, the SST DAC shown in Fig. 4.2 is simulated considering variations in the process corner and temperature of all devices and measuring the impedance variation. The simulation results at fast-fast, typical-typical, and slow-slow corners for NMOS and PMOS devices, respectively at a cold temperature of $-40\,°\mathrm{C}$ (C) and hot temperature of $125\,°\mathrm{C}$ (H) are shown in Fig. 4.4. The simulation results show an approximate $20\,\%$ variation of the termination impedance from its typical value due to a 3σ process and temperature variation.

Three techniques to calibrate the termination impedance are presented in Sec. 3.4.4. Given the wide range of termination impedance variation of approx. $20\,\%$, using the parallel branch technique is the most suited. Using body biasing of the MOS switches, given the chosen ratio of r_{RM} does offer the only calibration of the termination impedance for 1σ variation.

Given the pros and cons discussed in Sec. 3.4.4, the use of parallel branches technique is chosen to be implemented.

To calculate the number of parallel branches needed to cover the impedance variation of $20\,\%$, one can approximate based on Eq. 4.2, an additional 4 unary cells are required. In addition, to enable higher resolution of impedance calibration, 8 half unary cells are chosen as shown in Fig. 4.5. Therefore, four calibration cells should be enabled for the typical corner, eight calibration cells for the slow corner, and none of the fast corner calibration cells. By adding 4 calibration cells to the typical corner, the MSB impedance changes as:

$$R_{\mathrm{MSB}} = (\sum_{i=1}^{5} 2^{-i} + 15 + 4/2) \times R_{\mathrm{L}} = 17.97 \times 50\,\Omega \approx 900\,\Omega. \tag{4.5}$$

and impedance of active and passive devices is recalculated as

$$R_{\mathrm{on}} = \frac{R_{\mathrm{MSB}}}{r_{\mathrm{RM}} + 1} = \frac{900\,\Omega}{5} = 180\,\Omega, \tag{4.6}$$

$$R_{\mathrm{T}} = \frac{r_{\mathrm{RM}} \times R_{\mathrm{MSB}}}{r_{\mathrm{RM}} + 1} = \frac{4 \times 900\,\Omega}{5} = 720\,\Omega. \tag{4.7}$$

4.5 Echo Canceller Pair

The use of EC-DAC enables an active cancellation of the TX-data as shown in Fig. 3.34. The EC-DAC uses the locally timing-matched TX-data by sharing the same input signal path with the minimum physical distance between the TX and EC DAC cells in the layout.

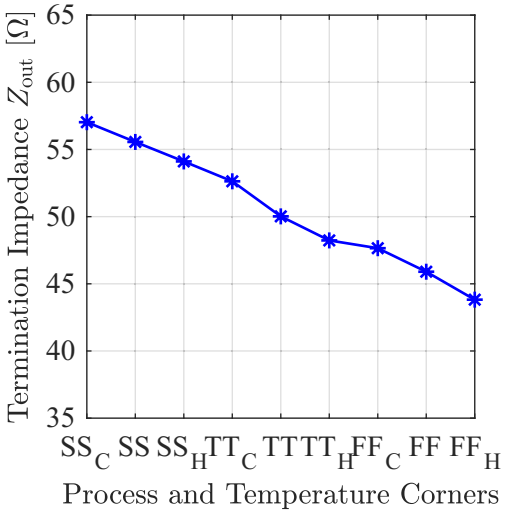


Figure 4.4: Termination impedance Z_{out} pre-calibrated across corner (slow, typical, fast) and temperature (cold, hot).

The key challenges of a full-duplex automotive transmitter with inherent interference canceller are

- high resolution of SST driver to enable power spectral shaping;
- matched output bandwidth >5 GHz between the TX-DAC and EC-DAC;
- sensitivity to static and dynamic mismatch effects between the TX-DAC and EC-DAC;
- TX-DAC should meet stringent transmit (PSD) and emission mask requirements defined by MultiG-BASET1 in 2.3.4 and 2.3.5;
- output impedance matching of 100 Ω across PVT variation;
- high power consumption of the TX-EC-DAC driver combination.

To match the EC and TX DAC, all digital data processing including the last sensitive analog pre-driver is shared between each pair of cells of the DACs. In the layout, the cells are placed tightly closed to each other, minimizing any process mismatch between them.

Timing and Offset

Moreover, the mismatch caused by the process on these switches can create a timing mismatch between the cells. The timing mismatch in this design not only affects the

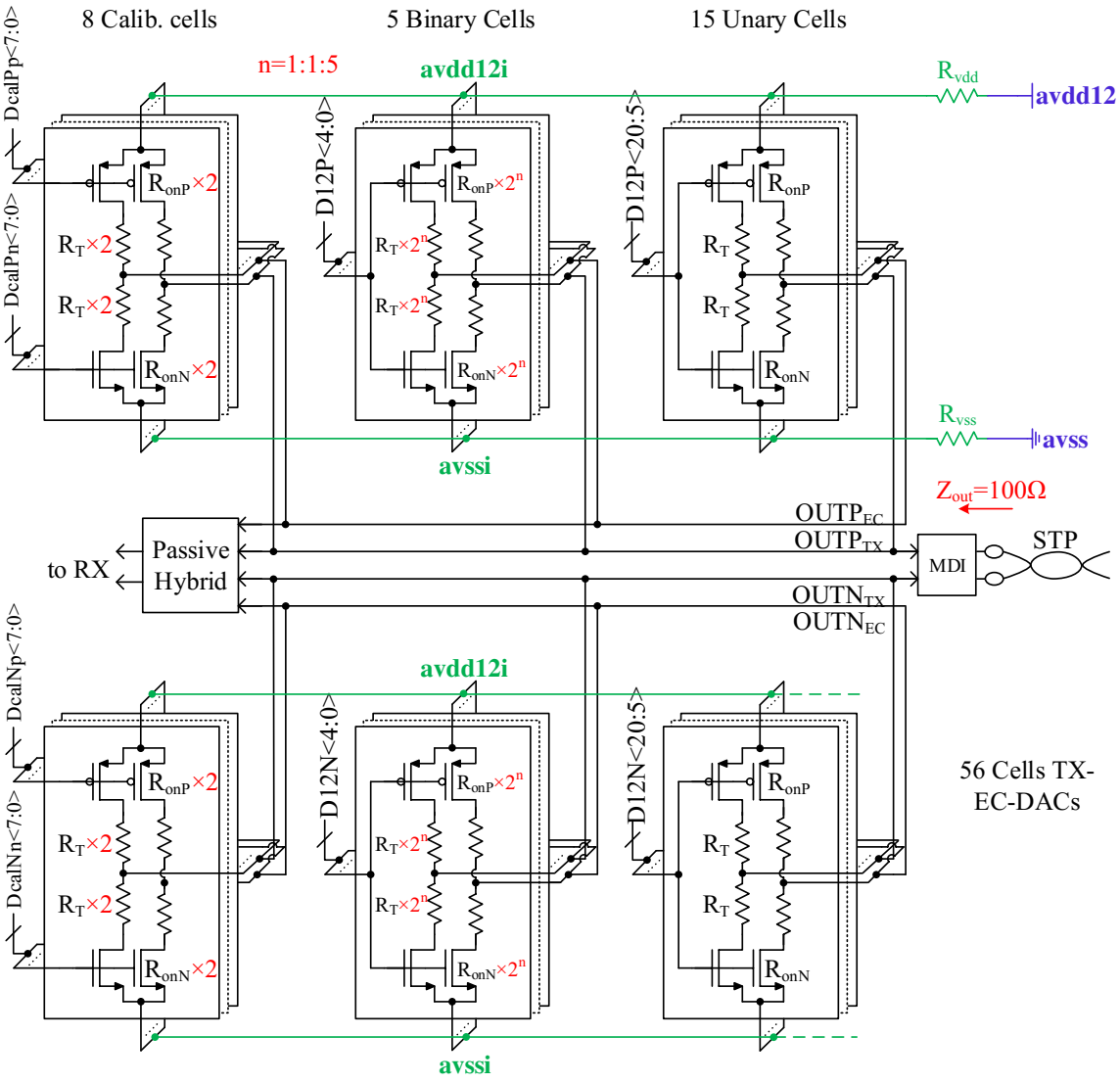


Figure 4.5: The circuit schematic of the 9-bit SST TX-EC-DAC segmented into 4-bit unary and 5-bit binary with 8 calibration cells with the weight of half the unary cell.

jitter on the eye diagram at the cross point but also it affects the echo canceling at the receiver. Therefore, the size of the switches can not be too small so that the mismatch, limits the required performance for the transceiver.

4.6 SST DAC Cell Design Consideration

The process GF 22 nm operates at a core voltage of 0.8 V. This supply voltage level using SST drivers does not enable the peak-peak differential output voltage level of 1 V defined

by MultiG-BASET1 for automotive Ethernet as calculated in 3.29. Therefore, the use of I/O devices within this process enables it.

The device type chosen out of the library for these devices named *ugslvtnfet* and *ugslvtpfet*. These devices are considered with the lowest threshold voltage, which enables faster switching for the driver.

The process uses a flip well, which enables having a wider range to bias the well. Moreover, this flip well technology has a superior $AV_{\mathrm{TH}} = 1.2\,\mu\mathrm{V}\cdot\mu\mathrm{m}$. The minimum channel length these devices are offered is 70 nm. So given the minimum length designed, the calculated W/L ratio for NMOS and PMOS devices is based on Eq. 3.37 are:

$$(W/L)_{\mathrm{P}} = \frac{6.58\,\mu\mathrm{m}}{70\,\mathrm{nm}}, (W/L)_{\mathrm{N}} = \frac{3.29\,\mu\mathrm{m}}{70\,\mathrm{nm}}. \tag{4.8}$$

The area calculated for PMOS and NMOS switches is approximate $0.46\,\mu\mathrm{m}^2$ and $0.23\,\mu\mathrm{m}^2$, respectively. Since both of the NMOS and PMOS devices' gates share the same pre-driver, the sum of their area to calculate the input offset is of interest. Given these sizes, one can calculate σ of the input offset at the gate of the switches based on

$$\sigma_{\mathrm{VTH,P}} = \frac{AV_{\mathrm{TH,P}}}{\sqrt{W_{\mathrm{P}}\cdot L_{\mathrm{P}}}} = \frac{1.2\,\mathrm{mV}\cdot\mu\mathrm{m}}{\sqrt{(6.58\mu m)\cdot 0.07\mu m}} = 1.8\,\mathrm{mV}, \tag{4.9}$$

$$\sigma_{\mathrm{VTH,N}} = \frac{AV_{\mathrm{TH,N}}}{\sqrt{W_{\mathrm{N}}\cdot L_{\mathrm{N}}}} = \frac{1.2\,\mathrm{mV}\cdot\mu\mathrm{m}}{\sqrt{(3.29\mu m)\cdot 0.07\mu m}} = 2.5\,\mathrm{mV}, \tag{4.10}$$

$$\sigma_{\mathrm{VTH}} = \sqrt{{\sigma_{\mathrm{VTH,N}}}^2 + {\sigma_{\mathrm{VTH,P}}}^2} = 3\,\mathrm{mV}. \tag{4.11}$$

The ratio of the active to passive area, r_{RM} of 4 is chosen, resulting the input offset of the MSB cell $V_{\mathrm{os}} = 3\times\sigma_{\mathrm{VTH}} = 9\,\mathrm{mV}$. Then, to calculate the jitter which this offset of these switches can cause, one can assume that two cells, either two MSBs or MSB and LSB pair, if one has $+V_{\mathrm{os}}$ and the other $-V_{\mathrm{os}}$, the cross at the output of the driver, will have a timing difference of:

$$t_{\mathrm{jitter}} = \frac{2\times V_{\mathrm{os}}\cdot t_{\mathrm{rise,pre-driver}}}{V_{\mathrm{OUT,diff,peak-peak}}}. \tag{4.12}$$

assuming that $t_{\mathrm{rise,pre-driver}} = 30\,\mathrm{ps}$ and $V_{\mathrm{OUT,diff,peak-peak}} = 1.2\,\mathrm{V}$ gives $t_{\mathrm{jitter}} = 200\,\mathrm{fs}$. For a 9-bit DAC, this amount of jitter, only driven from the devices, is acceptable for our application.

One can go with bigger switch sizes by choosing a higher r_{RM} or bigger channel length for the devices. However, the gate capacitance of the devices increases linearly with the total area, which increases the dynamic power consumption and limits the rise time of the pre-driver stage, $t_{\mathrm{rise,pre-driver}}$. Increasing $t_{\mathrm{rise,pre-driver}}$ increases further the jitter, t_{jitter} which shows to be counter-effective in this case.

4.6.1 Unit Cell Layout and Design Consideration

The design of the MSB unit cell is of prime importance. How to divide the number of fingers an active or passive device constitutes sets the capability to use a basic cell as the main building block of all unary and binary cells. Moreover, having the basic cell sharing along with all other cells guarantees the same active area implementation across the whole DAC. This, in turn, enables a good matching between all unary and binary cells, as each has the same footprint in the silicon up-to upper metal layers.

The metal layers which are available in the selected process are Two metal planes (M1-2), five copper planes (C1-5), one plane (JA), two top-level thick copper planes (QA, QB), and the uppermost thick plane (LB), which gives a metal stack of 11 layers.

The basic cell between all MSB cells and LSB cells share the same silicon footprint as for active and passive devices up to metal C1. From the metal stack of C1, the upper-level connection between devices is routed to enable LSB and MSB cells, all using the same basic cell.

The MSB cell devices, active and passive, are chosen to be sliced into 16 parallel devices. So, the layout structure of the unary cells can be used in the binary cells as well by changing the connection between the parallel devices. The same layout structure for all the cells minimizes the mismatch between the unary and binary cells. Therefore, the MSB cell has 16 MOS devices and resistors in parallel with each other. Binary cells then have 8, 4, 2, 1, and 1/2 of the devices connected in parallel in the signal path.

For LSB by 1/2 device, two of the devices are connected in series with each other. Connecting the devices in series with each other in LSB cell slows down the settling of the cell by having two devices in series, degrading the DAC ENOB. 32 parallel devices is not possible since each device finger width for NMOS devices is lower than the minimum width possible and on the other hand. 8 devices in parallel would then require the LSB to have four devices in series with each other, while four devices in series show to not gain any additional bit in the ENOB by simulating the analog extracted layout. Therefore, 16 parallel devices are the right trade-off for the highest ENOB in a 9-bit DAC.

4.6.2 Simulating the Device Sizes

The size of the switches is calculated as in Eq. 4.8. However, this calculation is based on the approximation made on the device model, and it is more accurate to simulate the impedance of the cells to size the NMOS, PMOS, and the poly resistors. For this, the MSB cell is biased to be at the exact digital mid code as shown in Fig. 4.6.

The exact digital mid code in an N-bit DAC with a large bit number gives a zero voltage drop on the channel and zero current going into the channel. In this case, the output voltage level of each of the positive or negative slice of DAC is set to half the supply voltage. To

simulate this setup, the output of a unary slice is biased to half of the supply voltage while once conducting on the push path and once on the pull path. At this static setup, the current going through the devices is measured, and the impedance of each of the devices is calculated. The size of the MOS switches and the poly resistor is then derived as:

$$(W/L)_{\mathrm{P}} = 16 \times \frac{520\,\mathrm{nm}}{70\,\mathrm{nm}}, \quad (W/L)_{\mathrm{N}} = 16 \times \frac{320\,\mathrm{nm}}{70\,\mathrm{nm}}, \quad (W/L)_{\mathrm{RT}} = 16 \times \frac{360\,\mathrm{nm}}{5.3\,\mu\mathrm{m}}. \quad (4.13)$$

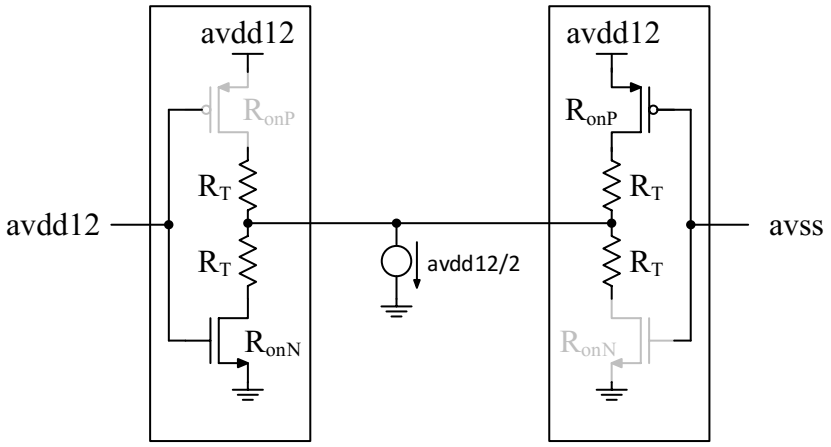


Figure 4.6: The circuit schematic of basing a unary cell to simulate the size of the devices achieving the desired impedance while the DAC is operating at the digital mid code.

The resistor chosen for the cells for the passive part of the termination impedance is poly-poly resistors. This type of resistor offers a highly linear impedance across the frequency range and voltage drop on it. Moreover, it has a high resistance per area. The minimum length possible for resistors is 360 nm. Based on Eq. 3.19, $R_{\mathrm{T}} = 4/5 \times 900\,\Omega = 720\,\Omega$. Given the number of fingers in parallel is chosen to be 16, the impedance of each finger is then 11.52 KΩ with each finger with the width of 360 nm and the length of 5.3 μm.

The mismatch factor $A_{\mathrm{r}} = 2.26\,\Omega\mu\mathrm{m}$ gives

$$\sigma_{\mathrm{RT}} = \frac{AV_{\mathrm{r}}}{\sqrt{W \cdot L}} = \frac{2.26\,\Omega \cdot \mu\mathrm{m}}{\sqrt{(16 \times 0.36\mu m) \cdot 5.3\mu m}} = 0.41\,\Omega. \quad (4.14)$$

which gives a maximum difference of 1.2 Ω between MSB cells with a nominal impedance of 720 Ω which is negligible for the DAC resolution targeted in this work.

4.7 Pre-driver

The pre-driver is depicted in Fig. 4.7 as a simple CMOS inverter. This inverter is shared between both TX- and EC-DAC individual units. Thus, the timing mismatch is minimized between the two DACs outputs, which yield a better power cancellation performance at the RX. This inverter stage shares the same supplies as the units of the DAC, avdd12 and avss which makes sure the digital noise on the digital supplies does not get coupled into the outputs.

The strength of the pre-driver is designed so that a rise time of $t_{\mathrm{rise,pre-driver}} = 30\,\mathrm{ps}$ is achieved with $(W/L)_{\mathrm{P}} = 2 \times \frac{2um}{70nm}$ and $(W/L)_{\mathrm{N}} = 1 \times \frac{2um}{70nm}$. Faster rise time yields a faster settling time on the outputs, which increases the average ENOB of the DAC. However, the strength of the inverter is as well limited not only by the gate capacitance of the units within the DAC but also by the parasitic capacitances of the inverter itself.

Moreover stronger inverter means higher crow-bar currents drawn from the analog supply, which adds more noise to the outputs. The supplies that will be discussed in detail in Sec. 5.3 are connected with bond wires, and current peaks drawn from the supply causes oscillation on the analog supplies, which is coupled to the outputs through the drivers and shows as non-linearities in the spectrum of the outputs.

4.7.1 Time Synchronizing Blocks

The timing of the digital signals driving the DAC units is crucial in the settling behavior of the outputs. Unsynchronized signals result in the output signal to be the sum of unsynchronized DAC units, which introduce slower settling time. The timing mismatch on the digital cells can be caused by the decoder as well as the level shifter.

Two latching stages are shown in Fig. 4.7 (digital pre-latch and final analog latch) operating on opposite clock edges to eliminate data-dependent delay variations. In addition, this eliminates memory effects [21] originating from the binary-unary decoder and data level shifter. The size of the devices within the latch and the pre-driver is depicted in Fig. 4.8

4.8 Level Shifter

The devices used in the main drivers operate with 1.2 V (I/O devices) to meet the demanded 1 V peak-peak voltage. However, these devices have a minimum 70 nm gate length. The digital core of the DAC can, however, use the minimum gate length of 22 nm of this process to take advantage of the fast speed of the switches to multiplex the digital input code feeding into from the DDS (Direct Digital Synthesizer). It also decodes the 9-bit into 5-bit unary and 4-bit binary signal with lower dynamic power consumption and more relaxed timing margins. Therefore once this digital signal processing is done, by use of a level

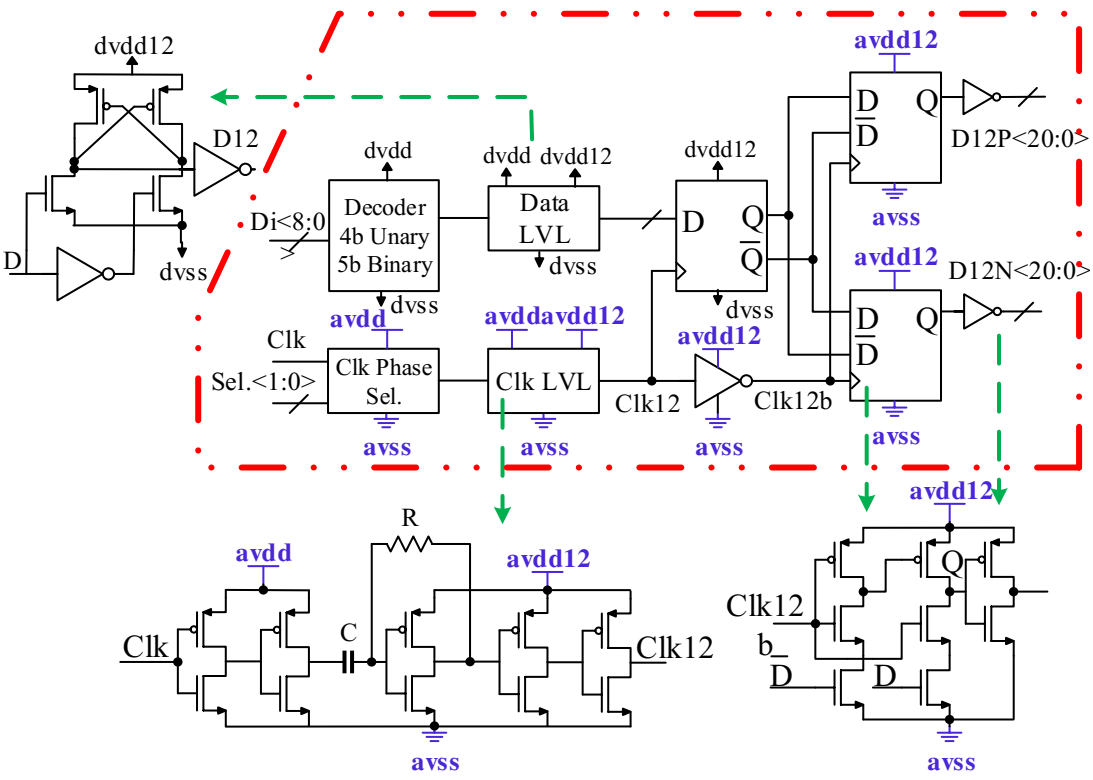


Figure 4.7: The circuit schematic of pre-driver, latches and level shifters.

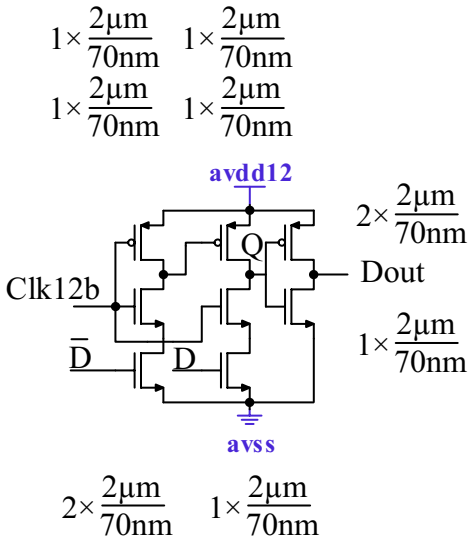


Figure 4.8: The circuit schematic of the latch showing the size of the devices.

shifter, the voltage levels are translated to 1.2 V and to the two stages of the latches as shown in Fig. 4.7.

The data level shifters use a standard positive cross-coupled inverter to translate the digital 0.8 V into 1.2 V. In this stage, all supplies used are digital supply rails (dvdd, dvdd12 and dvss) to isolate the noise of the digital processing from the analog supply rail.

The clock level shifter uses a series of two stages of level shifters supplied with avdd and avdd12 and a coupling capacitor in between with resistive feedback as shown in Fig. 4.7. Resistive feedback provides a DC path to the immediate inverter stage after the coupling capacitor, bringing the average DC voltage to the middle of the avdd12 and avss supply rail.

The design of the resistive feedback and coupling capacitor is considered as a high pass filter and the bandwidth of the filter is set by $\frac{1}{2\pi RC}$. In the case of the capacitor, it should be taken into account that it should be considerably bigger than the parasitic capacitances at the immediate inverter after it to maintain most of the amplitude of the voltage division on the gate of the transistors it drives.

The output buffer of the clock level shifter is designed strong enough to drive the input clock buffer of 20 input clock buffer of the latches corresponding to all unary and binary cells, as well as considering the parasitic capacitance of the routing path.

To achieve a 30 ps rise time of the clock signal at the input clock buffer of each latch, the last stage of the clock level shifter is sized as $(W/L)_{\mathrm{P}} = 32 \times \frac{1um}{70nm}$ and $(W/L)_{\mathrm{N}} = 16 \times \frac{1um}{70nm}$. Therefore, the rest of the clock level shifter is scaled accordingly to minimize the delay and maintain the rise time. Hence, the size of the switches for the inverter with the resistive feedback between its input and output is $(W/L)_{\mathrm{P}} = 16 \times \frac{1um}{70nm}$ and $(W/L)_{\mathrm{N}} = 8 \times \frac{1um}{70nm}$.

Taking into account the parasitic capacitance at the gate of the inverter to be approximately 40 fF, the AC coupling capacitor of the high pass filter is chosen to be C=400 fF to deliver more than 90 % of the voltage variation on it to the gate of the inverter. The bandwidth of the high pass filter is set to 120 MHz, sufficient to operate for the lowest data rate of 1 Gb/s defined by 1000Base-T1. This gives the resistive feedback value of approximately 3 KΩ. The size of the devices of the level shifters mentioned is shown in Fig. 4.9.

4.9 SST DACs and LVL Layout Floor Plan

The layout floorplan of a SST unit is shown in Fig. 4.10 consisting of TX and EC cells with their differential output pairs. TX and EC cells are placed as close as possible to each other to minimize the process variation and share the same latch and pre-driver signalling, minimizing timing mismatch between TX and EC output signals. Moreover, to reduce TX-EC DAC width, the 34 unit cells (including some dummy cells) are arranged in 2 full rows, still keeping the clock distribution and output signal summation simple. Four output

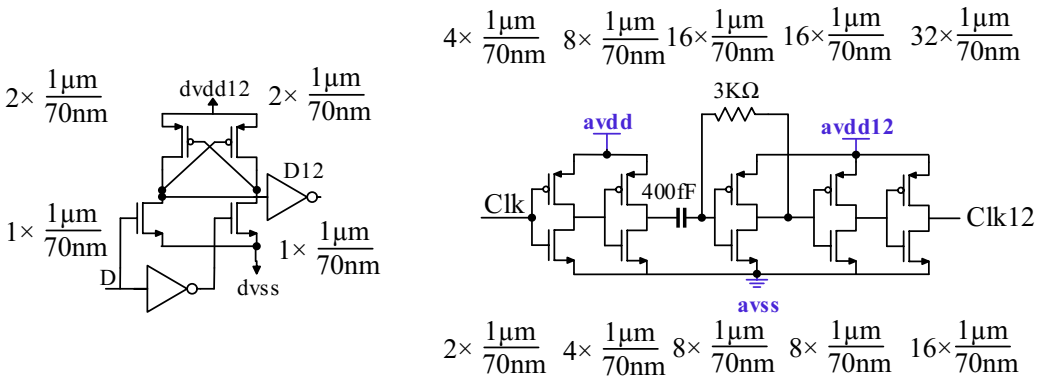


Figure 4.9: The circuit schematic of the level shifters showing the size of the devices.

lanes (i.e. differential TX- and EC-DAC output pairs) connecting across 2 SST rows to the pads in the middle, interchange their location within the output lanes to average out coupled noise from the neighbouring lanes.

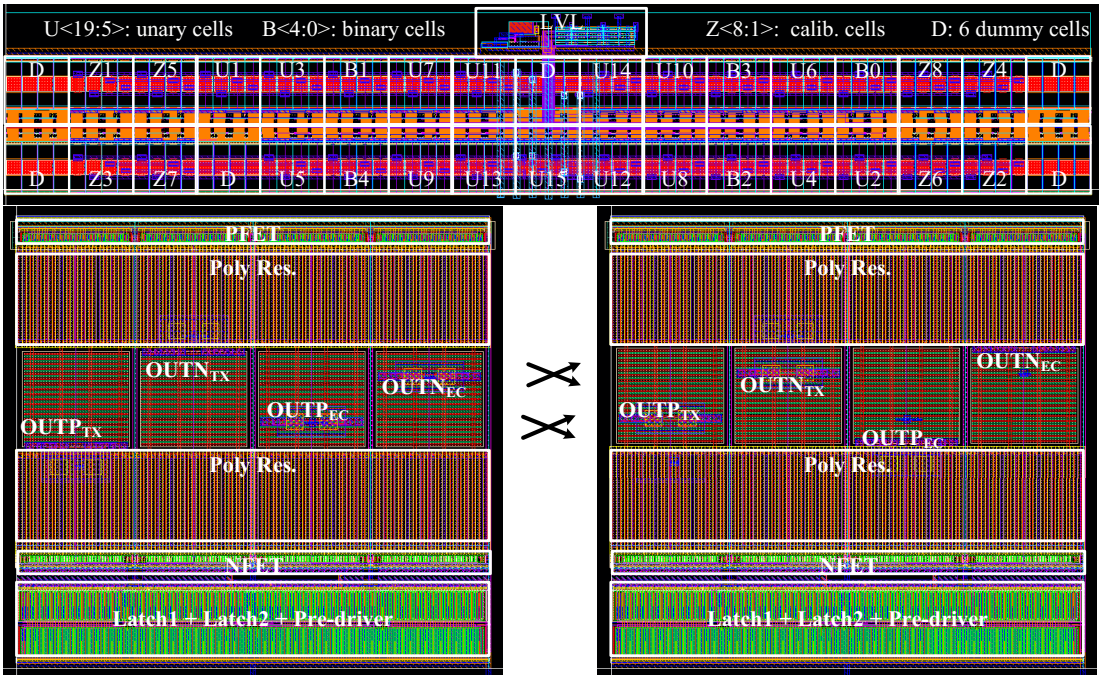


Figure 4.10: TX-EC DACs layout.

4.10 Digital Decoder

The architecture of the digital decoder is depicted in Fig. 4.11. The digital input code is fed from the DDS interface with a length of 9-bit Di<8:0> inputs to the block. The binary part of the input signal Di<4:0> is latched on the falling edge of the clock cycle while the unary part of the input signal Di<8:5> is fed into the 4-bit thermo-decoder. Later, the binary signal and thermo-decoded signal samples on the rising edge of the clock signal and feed to the output as Dout<19:0>.

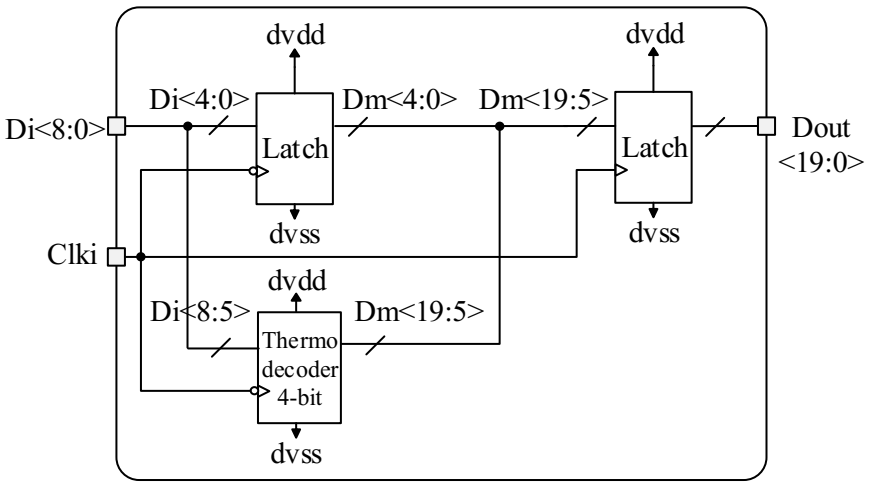


Figure 4.11: The architecture of the digital decoder with 9-bit length input Di<8:0> and mixed thermo/binary decoded signal Dout<19:0> as the output.

The detailed circuit schematic of the 4-bit thermo-decoder is shown in Fig. 4.12. The main constrain on the design of such a thermo-decoder is the latency of the output to the input signal to be less than half a clock cycle (with the assumption of the maximum data rate, half of a clock cycle is approximately 90 ps). Considering this latency, the merging of the binary and the thermo-decoded in the top-level architecture of the decoder is enabled. In addition, Given the 4-bit thermo-decoder architecture here use two cascaded stages of thermo-decoding before the last stage clock decoder bt0, one has to maintain:

$$t_{\mathrm{bt2}} + t_{\mathrm{bt1}} < T_{\mathrm{s}}/2,$$

and

$$t_{\mathrm{bt0}} < T_{\mathrm{s}}/2,$$

,

where T_s is the period of the maximum clock frequency used in the DAC. For the maximum data rate of 11.2 Gb/s needed for 10GBase-T1, the clock frequency $f_s = 5.6$ GHz. Therefore $T_s \approx 180$ ps.

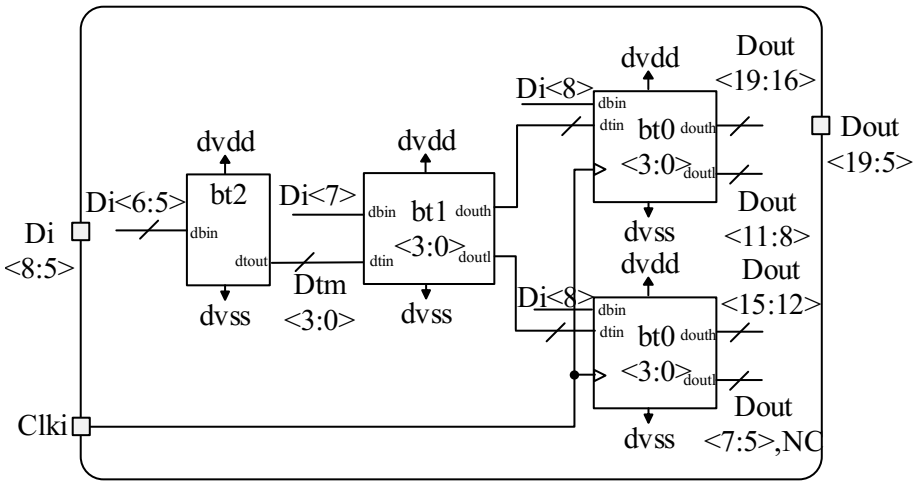


Figure 4.12: Circuit schematic of the 4-bit thermo decoder consisting of three main digital blocks, bt2, bt1 and bt0.

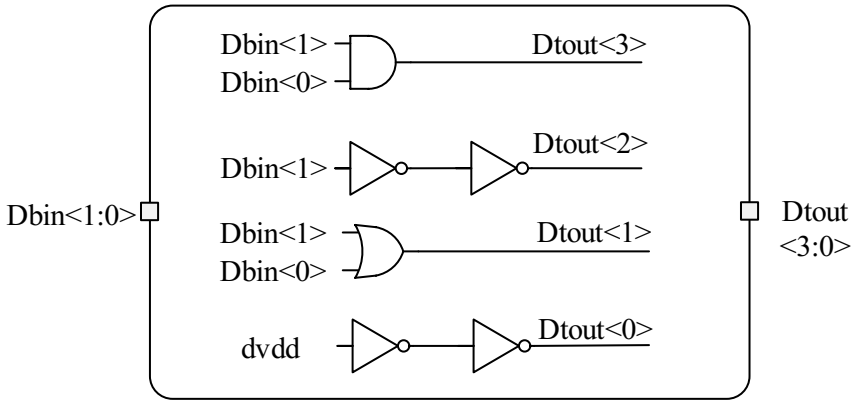


Figure 4.13: The circuit schematic of bt2 digital block.

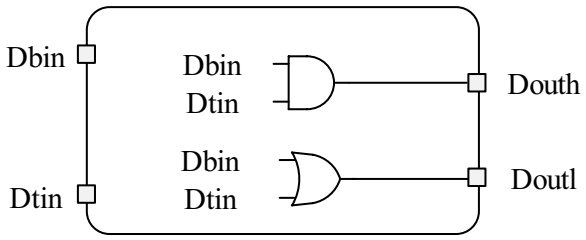


Figure 4.14: The circuit schematic of bt1 digital block.

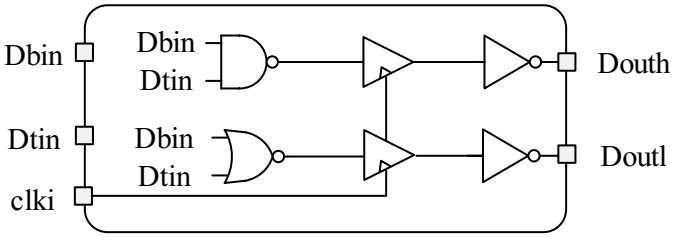


Figure 4.15: The circuit schematic of bt0 digital block.

4.11 DDS Interface

Aiming to feed the input data into the DACs and test the performance, a direct digital synthesizer is used. The DDS is implemented on the test chip and includes a set of data in the memory to feed a single tone sinusoidal signal into the DAC. Therefore, it is possible to look at the spectrum of such a single tone sinusoidal signal and analyze the dynamic performance of the DAC. Moreover, the DDS has a 9-bit wide 256-word memory, which is possible to write in with a Serial Peripheral Interface (SPI). To facilitate the design of the DDS to meet timing constraints, it operates with 1/8 of the sampling frequency of the DACs.

To retrieve the data from the DDS and feed it to the decoder, the data should be multiplexed. Thus, the top-level structure of the multiplexer for the DDS interface is depicted in Fig. 4.16.

First, to eliminate any timing difference between the present data at the digital core of the DAC, the data is sampled with a latch with the clock signal sourced from the DDS. The timing difference of the signal can be caused due to the layout mismatch between the metal routes bringing the signal in. These signal routes can not be minimized by placing the DDS too close to the DAC since the digital noise that is injected into the substrate due to the activities in the DDS can couple into the analog signals and affect the performance of the DAC. Therefore, a distance of at least 100 μm is considered between the DDS block and DACs to minimize this noise.

Moreover, a guard ring is placed around the DACs to collect as much noise as possible from the substrate. Once the signals are sampled with the DDS clock signal, Clks the data is fed into a multiplexer, MUX 8:1, and then sampled with the internal clock signal of the DAC, Clki. However, to make sure the signal is correctly sampled in case the phase of the Clks and Clki with the latency added by the immediate latch on the input data from the DDS and MUX 8:1 happen to be aligned. Therefore, a phase selector with 2-bit input, SPI_PHA<1:0> is used to select a phase of Clki with every 90 degrees different from each other.

4.12 Simulation Results

In this section, the simulation test bench setups to characterize the designed TX DAC in Cadence Virtuoso® environment is presented. To verify the drawn layout for the DACs, an analog extracted model of the DACs, including the power supply mesh and pads, is used for the simulations. Moreover, the bond wires of the QFN package are modeled as mentioned in 5.3 and are included in the simulation setup.

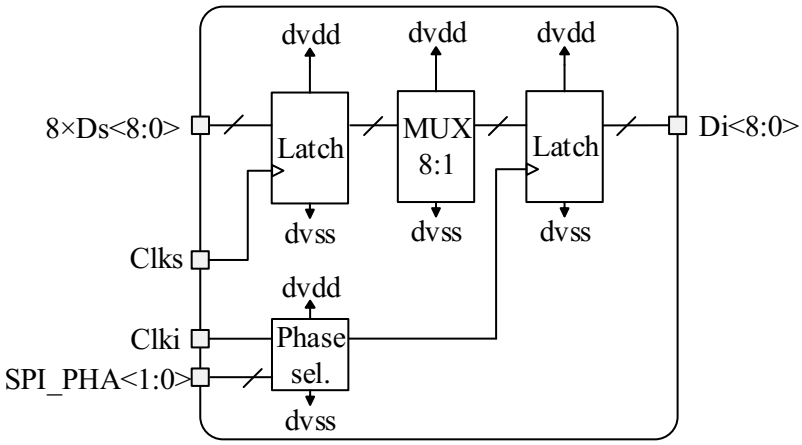


Figure 4.16: The circuit schematic of the DDS interface.

4.12.1 Echo Canceling Performance

Normally an on-chip hybrid is needed to subtract the outputs of the DACs and delivering the signal to the RX. However, the design of the hybrid is not in the scope of this work, and each of the outputs of the DACs is connected to a pad and then bonded to the QFN package.

In the simulations, the outputs of the DACs are subtracted from each other. This gives the residual error due to the mismatch between the two DACs, mainly originated from the layout of the output paths, bringing the signals from the active area of the silicon substrate up to the top layer metal LB on the pads. Moreover, neighbouring metal paths to the outputs of the DACs can bring alien noise coupled into it, which is not exactly identical for both DACs, although careful layout strategies are implemented to mitigate these effects. As mentioned in Sec. 3.5.1, the echo cancellation requires cancelling at least 43 dB of the transmit power for the target application. The mathematical subtraction of the TX-DAC and EC-DAC for each of the operating frequencies in the scope of this work is depicted in Fig. 4.17, Fig. 4.18, Fig. 4.19 and Fig. 4.20.

The residual errors and transmission power reductions at RX simulated at different bit rates are summarized in Tab. 4.1. The simulation results shows that the echo cancellation performance satisfies the minimum 43 dB transmit power reduction required by the hybrid.

Bit-rate [Gb/s]	peak-peak error residue [mV]	power reduction [dB]
11.2	5.88	44.61
5.6	5.33	45.46
2.8	5.4	45.35
1.125	2.74	51.24

Table 4.1: The residue errors and transmission power reductions at RX, simulated at different sampling speeds and data rates.

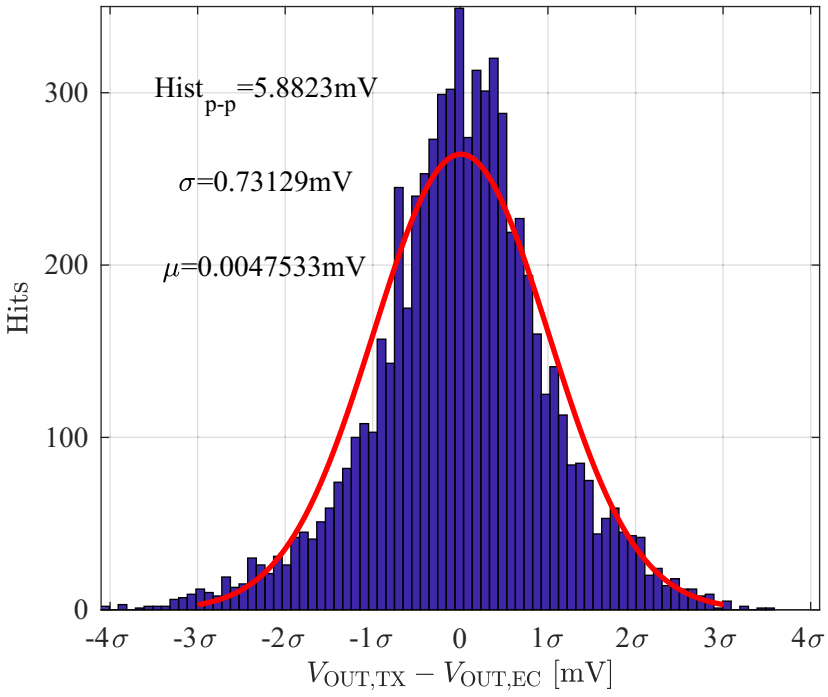


Figure 4.17: TX differential output signal subtracted from EC differential output signal at 11.2 Gb/s suitable for 10GBase-T1. The peak-peak residue error is 5.88 mV with a sigma of 0.73 mV, respectively. This leads to 44.61 dB of transmit power reduction at the RX input.

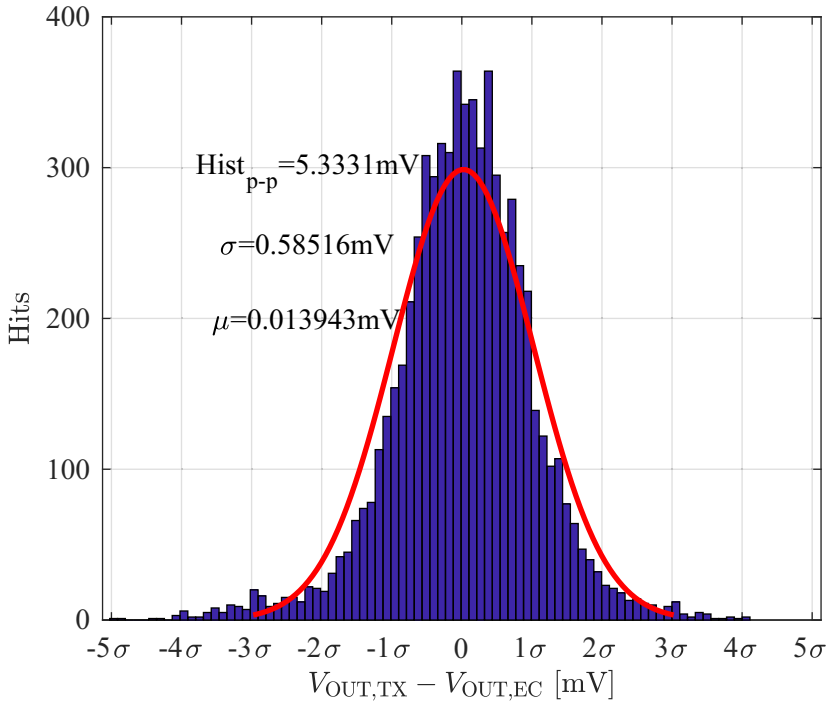


Figure 4.18: TX differential output signal subtracted from EC differential output signal at 5.6 Gb/s suitable for 5GBase-T1.The peak-peak residue error is 5.33 mV with a sigma of 0.58 mV, respectively. This leads to 45.46 dB of transmit power reduction at the RX input.

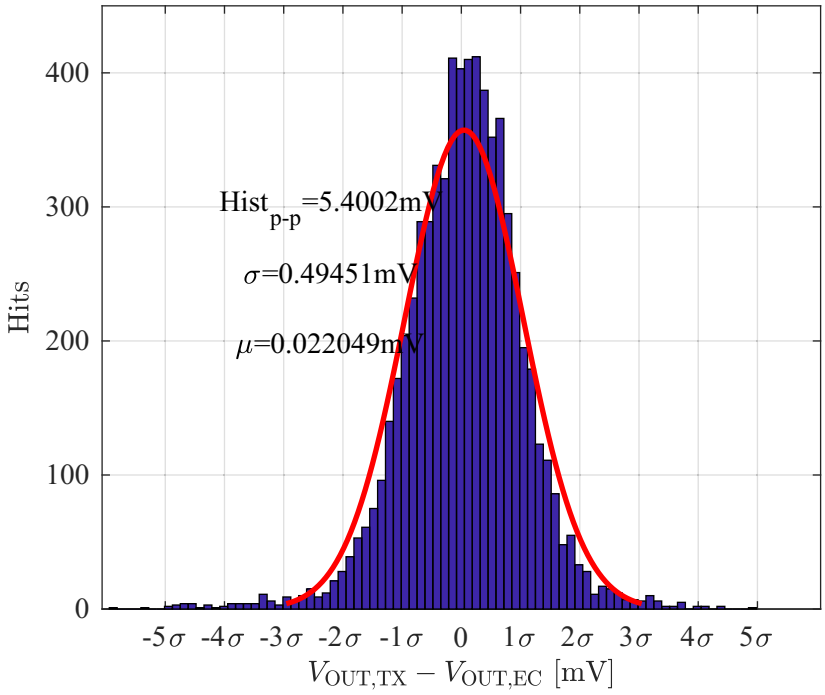


Figure 4.19: TX differential output signal subtracted from EC differential output signal at 2.8 Gb/s suitable for 2.5GBase-T1. The peak-peak residue error is 5.4 mV with a sigma of 0.49 mV, respectively. This leads to 45.35 dB of transmit power reduction at the RX input.

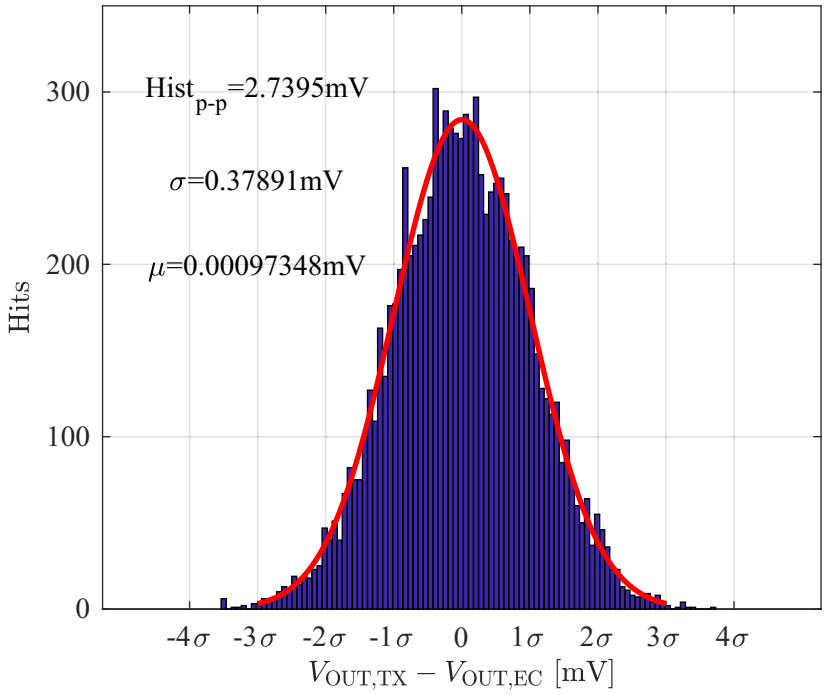


Figure 4.20: TX differential output signal subtracted from EC differential output signal at 1.125 Gb/s suitable for 1GBase-T1. The peak-peak residue error is 2.74 mV with a sigma of 0.38 mV, respectively. This leads to 51.24 dB of transmit power reduction at the RX input.

4.12.2 Static Properties

The static properties to characterize the DAC is summarized in Sec. 3.1.1. The static linearity of the DAC is simulated here to show the INL and DNL error across the digital input code. The INL simulation results shows a peak-peak INL error of 0.125 LSB shown in Fig. 4.21 with maximum DNL error of 0.02 LSB as shown in Fig. 4.22. Static linearity simulation results verify that the DAC performance at low frequencies is sufficient for the intended 9-bit DAC and not limiting the linearity of the DAC at frequencies closer to Nyquist.

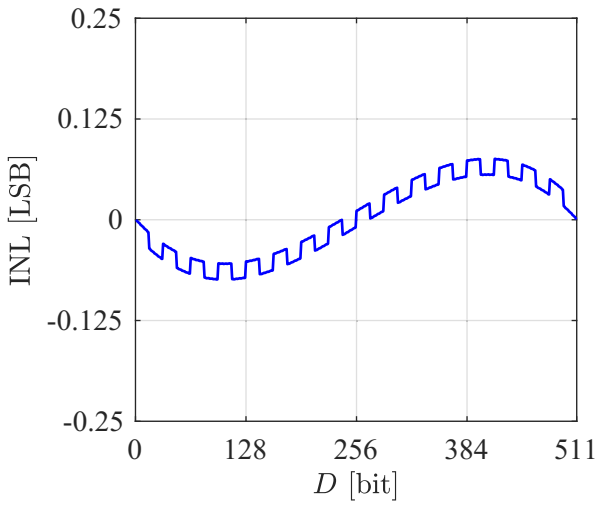


Figure 4.21: .

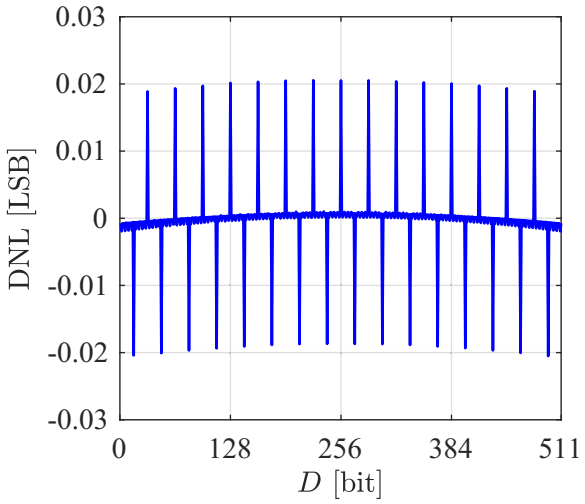


Figure 4.22: .

4.12.3 Dynamic Properties

The dynamic properties of a DAC which is of interest in this work is discussed in Sec. 3.1.2.

Spectrum Analysis

In order to calculate the ENOB of the TX-DAC across low frequencies to the Nyquist frequency at different sampling rates, the analog extracted model of the DAC is simulated, and the properties such as ENOB, SNR, and SFDR are calculated based on the frequency spectrum of the TX-DAC differential output. The frequency spectrum of the TX-DAC operating at 5.6 GS/s inputting a low-frequency and a high-frequency single-tone sinusoidal signal is plotted in Fig. 4.23 and Fig. 4.24, respectively.

The ENOB and SFDR of the TX-DAC operating at 5.6 GS/s while sweeping the input frequency tone from a low-frequency tone to near Nyquist frequency is depicted in Fig. 4.25 and Fig. 4.26, respectively. The simulation results show that the TX-DAC has an ENOB of approximately 8 bits at lower frequencies and it drops to 6.8 bits at Nyquist frequency. This drop in the ENOB with an increase of the input frequency tone is mainly caused by the increase in the distortions close to the Nyquist frequency. These distortions are caused mainly by the noise from the power supplies, coupling into the TX-DAC output, and degrading the SNR performance.

The SFDR performance of the TX-DAC with input tone at near Nyquist frequency shows to be higher than 53 dBC which is limited by the third harmonic but not limiting the overall ENOB performance of the DAC.

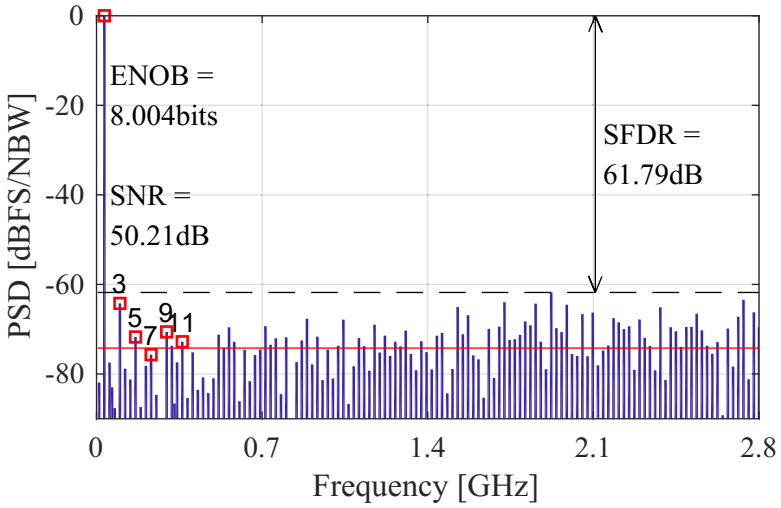


Figure 4.23: The spectrum analysis of the TX-DAC operating at 5.6 GS/s inputting a low-frequency single-tone sinusoidal signal, annotating the ENOB, SNR, and SFDR parameters.

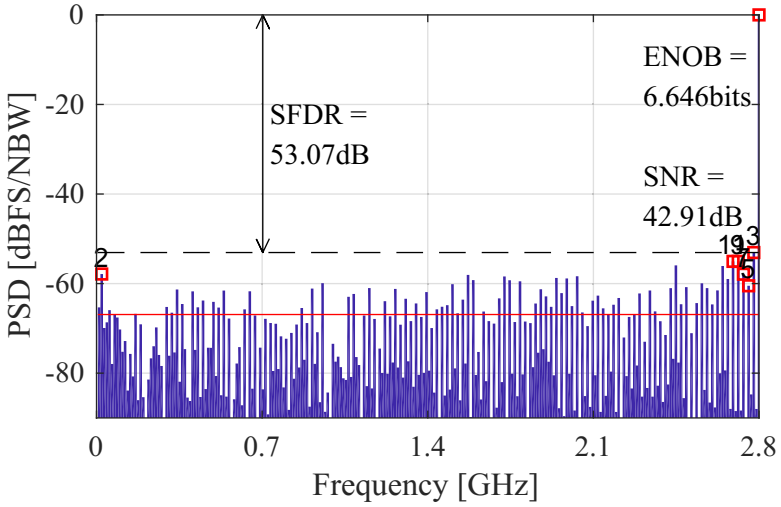


Figure 4.24: The spectrum analysis of the TX-DAC operating at 5.6 GS/s inputting a high-frequency single-tone sinusoidal signal, annotating the ENOB, SNR, and SFDR parameters.

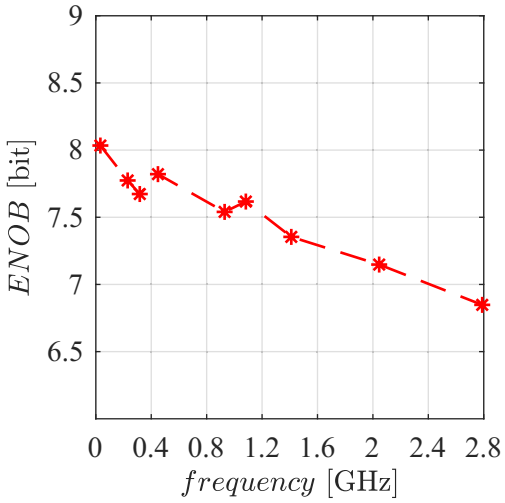


Figure 4.25: ENOB of TX-DAC analog extracted model simulated operating at 5.6 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist.

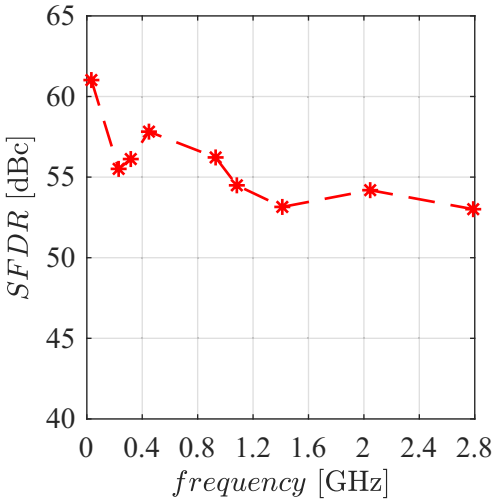


Figure 4.26: SFDR of TX-DAC analog extracted model simulated operating at 5.6 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist.

The frequency spectrum of the TX-DAC operating at 2.8 GS/s inputting a low-frequency and a high-frequency single-tone sinusoidal signal is plotted in Fig. 4.27 and Fig. 4.28, respectively. Moreover, the ENOB and SFDR of the TX-DAC operating at 2.8 GS/s while sweeping the input frequency tone from a low-frequency tone to near Nyquist frequency is depicted in Fig. 4.29 and Fig. 4.30, respectively. ENOB of the TX-DAC at the sampling rate of 2.8 GS/s shows to be higher than 8 bits across the input sinusoidal frequency tone and the SFDR well over 54 dBc.

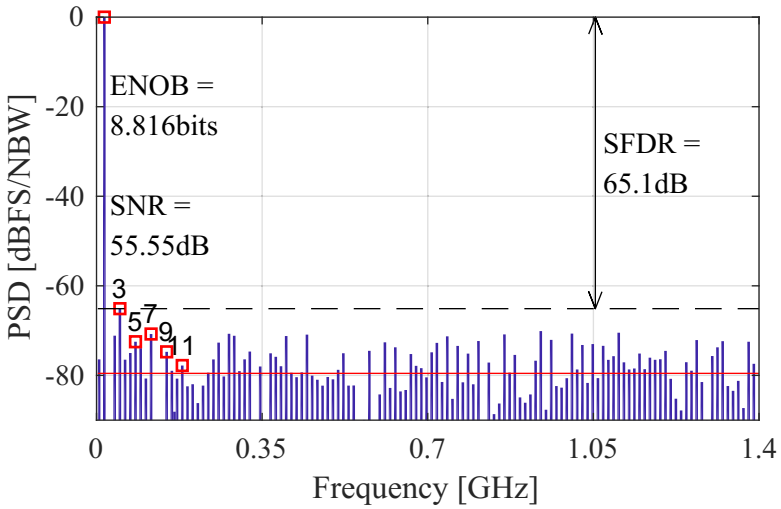


Figure 4.27: The spectrum analysis of the TX-DAC operating at 2.8 GS/s inputting a low-frequency single-tone sinusoidal signal, annotating the ENOB, SNR, and SFDR parameters.

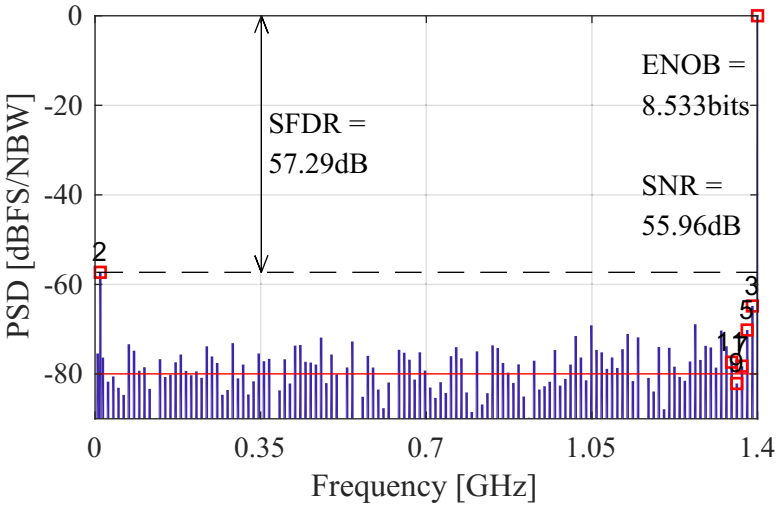


Figure 4.28: The spectrum analysis of the TX-DAC operating at 2.8 GS/s inputting a high-frequency single-tone sinusoidal signal, annotating the ENOB, SNR, and SFDR parameters.

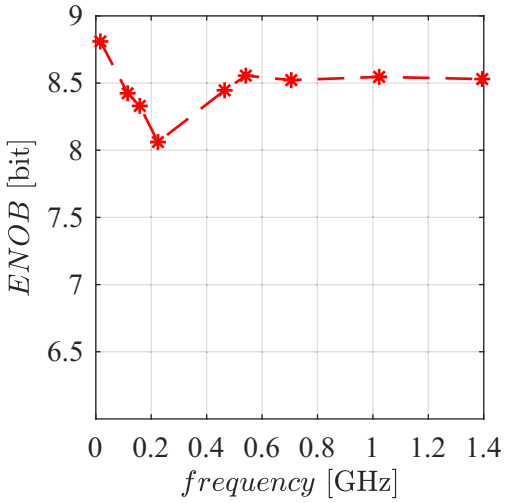


Figure 4.29: ENOB of TX-DAC analog extracted model simulated operating at 2.8 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist.

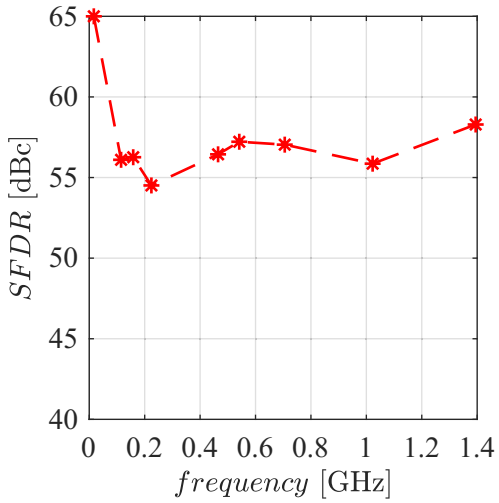


Figure 4.30: SFDR of TX-DAC analog extracted model simulated operating at 2.8 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist.

The frequency spectrum of the TX-DAC operating at 1.4 GS/s inputting a low-frequency and a high-frequency single-tone sinusoidal signal is plotted in Fig. 4.31 and Fig. 4.32, respectively. Moreover, the ENOB and SFDR of the TX-DAC operating at 1.4 GS/s while sweeping the input frequency tone from a low-frequency tone to near Nyquist frequency is depicted in Fig. 4.33 and Fig. 4.33, respectively. ENOB of the TX-DAC at the sampling rate of 1.4 GS/s shows to be higher than 8.4 bits across the input sinusoidal frequency tone and the SFDR well over 56 dBc.

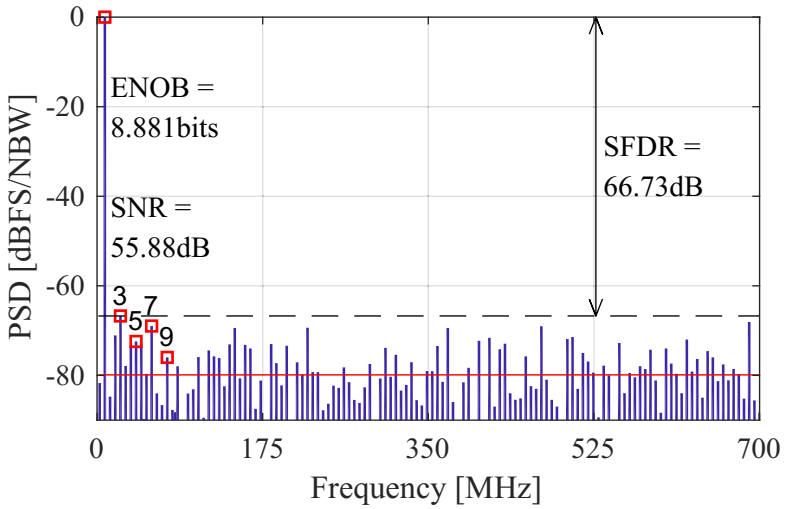


Figure 4.31: The spectrum analysis of the TX-DAC operating at 1.4 GS/s inputting a low-frequency single-tone sinusoidal signal, annotating the ENOB, SNR, and SFDR parameters.

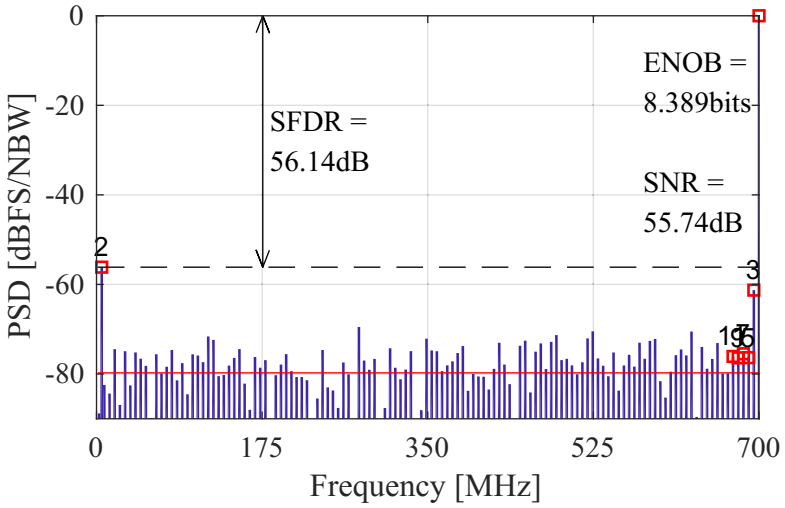


Figure 4.32: The spectrum analysis of the TX-DAC operating at 1.4 GS/s inputting a high-frequency single-tone sinusoidal signal, annotating the ENOB, SNR, and SFDR parameters.

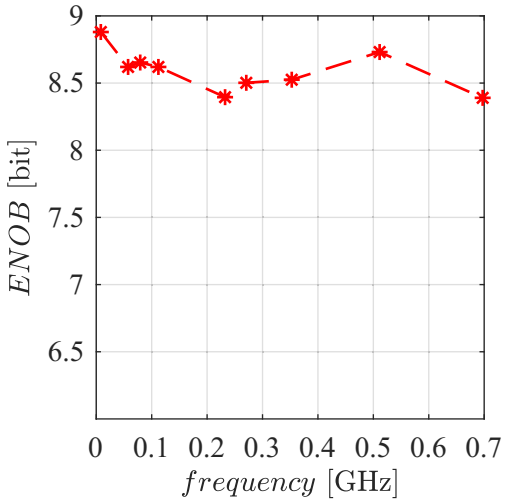


Figure 4.33: ENOB of TX-DAC analog extracted model simulated operating at 1.4 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist.

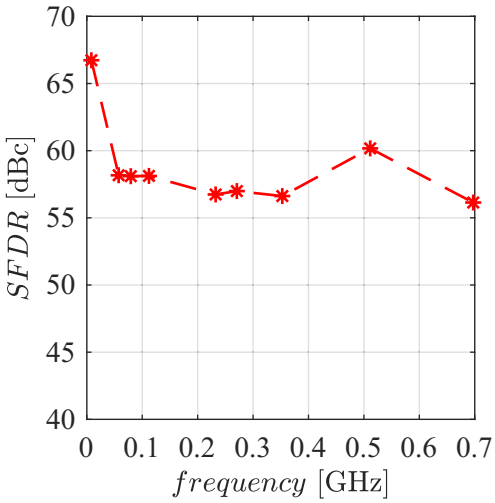


Figure 4.34: SFDR of TX-DAC analog extracted model simulated operating at 1.4 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist.

The frequency spectrum of the TX-DAC operating at 750 MS/s inputting a low-frequency and a high-frequency single-tone sinusoidal signal is plotted in Fig. 4.35 and Fig. 4.36, respectively. Moreover, the ENOB and SFDR of the TX-DAC operating at 750 MS/s while sweeping the input frequency tone from a low-frequency tone to near Nyquist frequency is depicted in Fig. 4.37 and Fig. 4.37, respectively.

ENOB of the TX-DAC at the sampling rate of 750 MS/s shows to be higher than 7.1 bits across the input sinusoidal frequency tone and the SFDR well over 45 dBc. The main reason of the sharp drop in the performance of the TX-DAC at lower frequencies is due to the high pass filter on the PCB due to the AC coupling capacitor, which sets the bandwidth to 318 KHz which directly limits the measured performance of the TX-DAC for the sampling rate of 750 MS/s. The use of AC coupling capacitor is discussed in detail in Sec. 5.2.

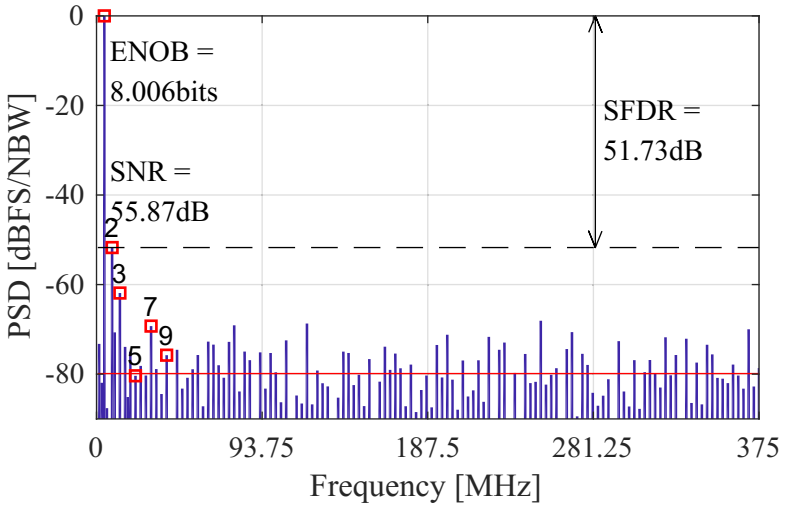


Figure 4.35: The spectrum analysis of the TX-DAC operating at 750 MS/s inputting a low-frequency single-tone sinusoidal signal, annotating the ENOB, SNR, and SFDR parameters.

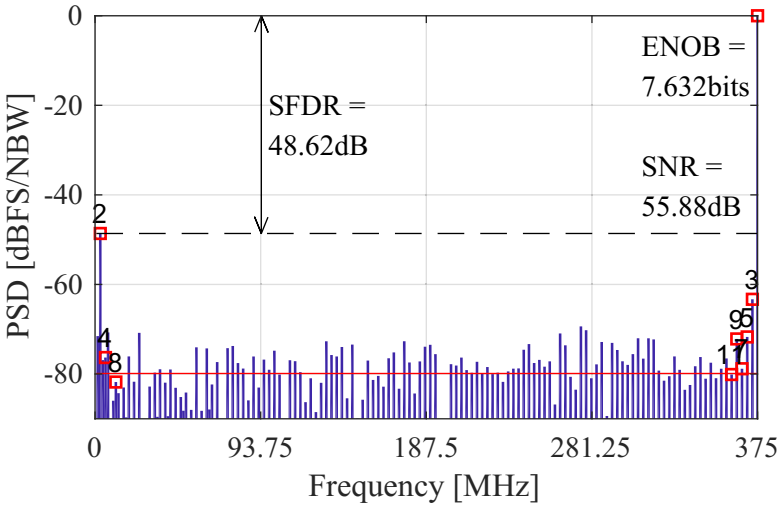


Figure 4.36: The spectrum analysis of the TX-DAC operating at 750 MS/s inputting a high-frequency single-tone sinusoidal signal, annotating the ENOB, SNR, and SFDR parameters.

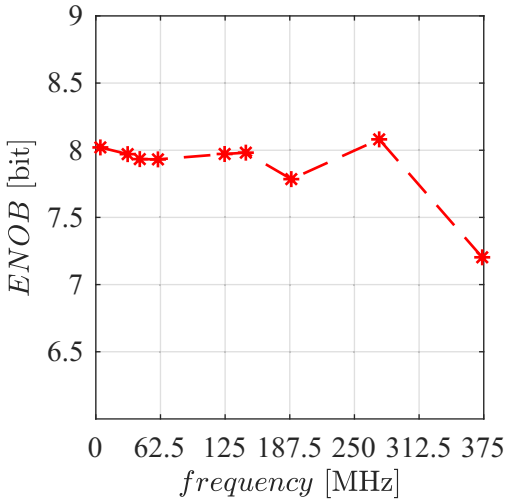


Figure 4.37: ENOB of TX-DAC analog extracted model simulated operating at 750 MS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist.

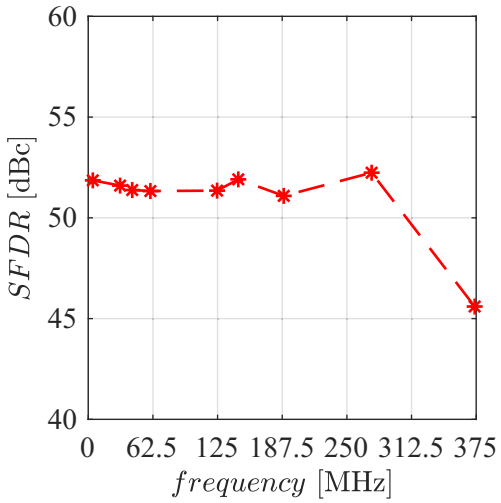


Figure 4.38: SFDR of TX-DAC analog extracted model simulated operating at 750 MS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist.

Common Mode Spectrum

The common-mode noise simulation of the DAC differential outputs sums the signal power of the two outputs together to show how the common-mode signal power looks like.

Due to the parasitic capacitors between the gate of the termination switches within the DAC and the outputs, the event of driving the gate of these switches synchronized with the clock signal can generate an injection of the charge to the output signal. Thus, by analyzing the power spectrum of the common-mode signal, the power of the clock feedthrough shows itself at the multiplies of the sampling frequency.

In the simulation setup, the differential outputs are mathematically added together, giving the common mode signal and the PSD of the signal is calculated. The simulation results for the power combination at the rate of 5.6 GBaud/s is shown in Fig. 4.39 with 34.9 dBc attenuation of the clock feed through. Moreover, the simulation results for 2.8 Gbaud/s, 1.4 GBaud/s and 750 MBaud/s are plotted in Fig. 4.40, Fig. 4.41 and Fig. 4.42, respectively. It can be notices shows an attenuation of 35.5 dBc, 39.8 dBc and 44.7 dBc in the clock feed through, respectively.

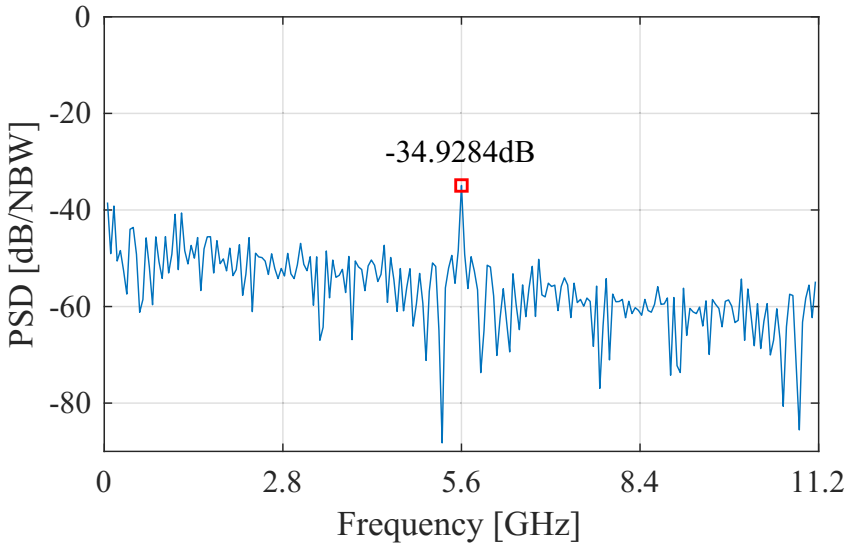


Figure 4.39: Simulated TX common-mode output signal operating at 5.6 Gbaud/s showing 34.9 dBc attenuation of clock feed through.

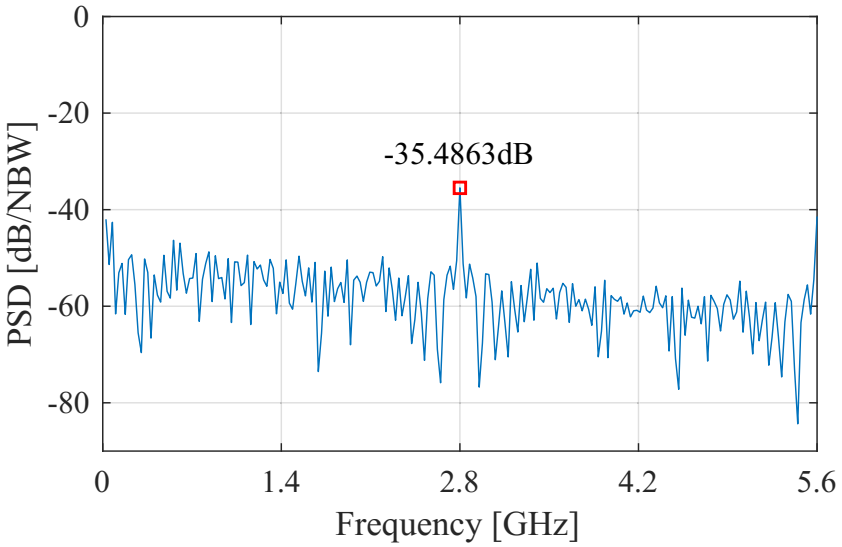


Figure 4.40: Simulated TX common-mode output signal operating at 2.8 Gbaud/s showing 35.5 dBc attenuation of clock feed through.

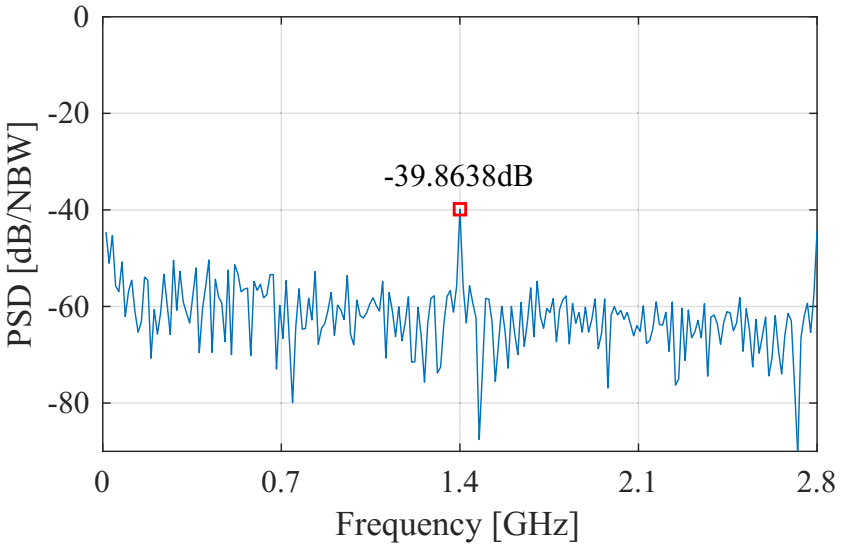


Figure 4.41: Simulated TX common-mode output signal operating at 1.4 Gbaud/s showing 39.8 dBc attenuation of clock feed through.

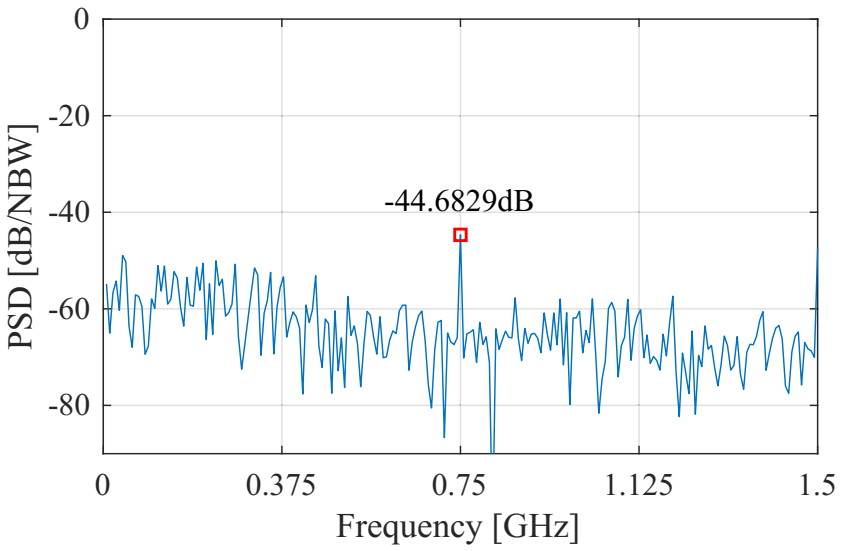


Figure 4.42: Simulated TX common-mode output signal operating at 750 Mbaud/s showing 44.7 dBc attenuation of clock feed through.

4.12.4 Eye Diagram

To verify the TX-DAC capability to be used within Automotive Ethernet transceiver, its layout is made and a simulation is performed with the analog extracted parasitics included in the model. The results of the eye diagram should show the required differential peak-peak output voltage of 1 V with sufficient eye-opening to identify the PAM modulated data up to the data rate of 11.2 Gb/s.

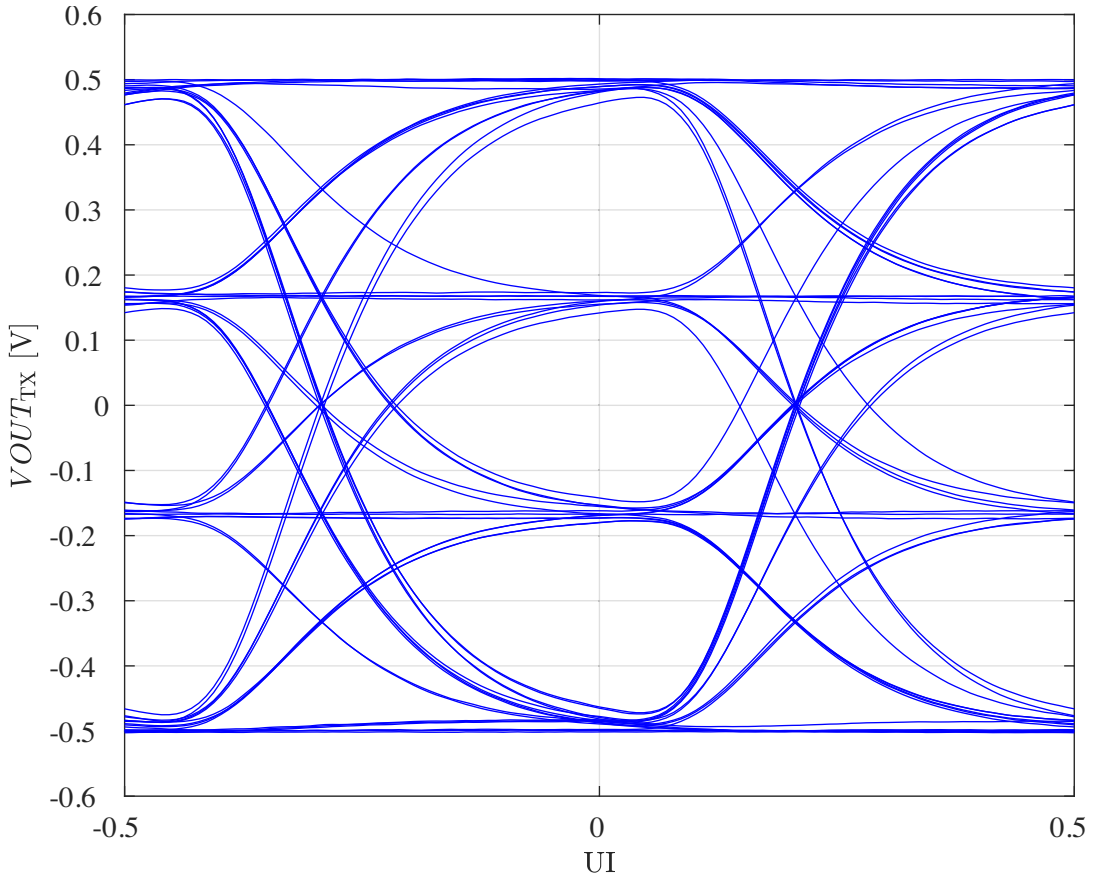


Figure 4.43: The eye diagram of the TX-DAC simulated with the analog extracted model at the data rate of 11.2 Gb/s.

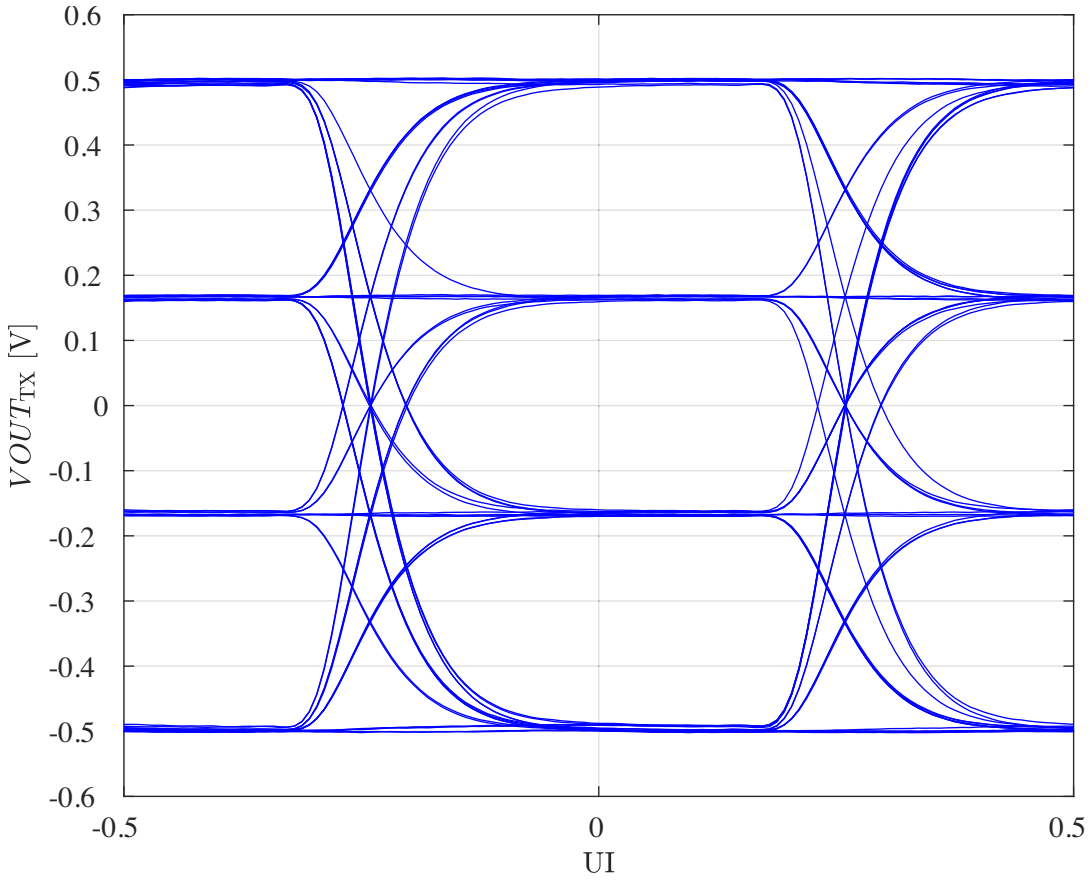


Figure 4.44: The eye diagram of the TX-DAC simulated with the analog extracted model at the data rate of 5.6 Gb/s.

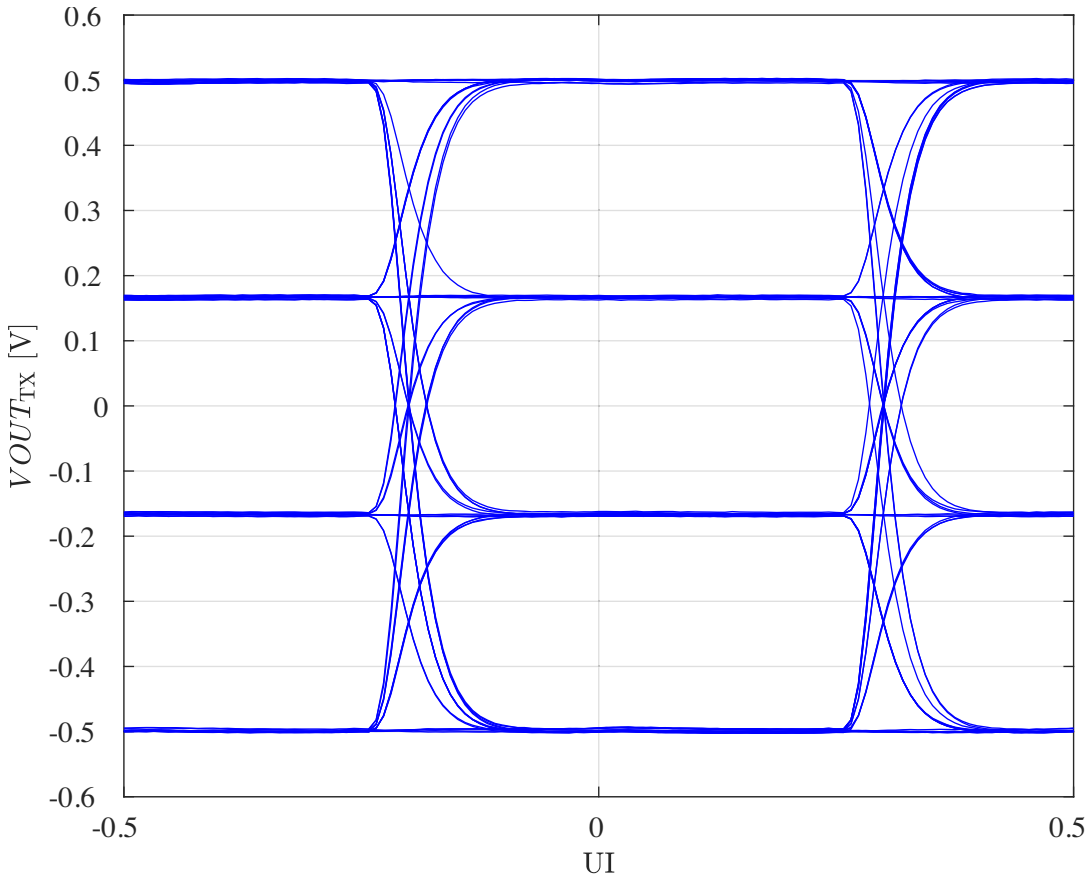


Figure 4.45: The eye diagram of the TX-DAC simulated with the analog extracted model at the data rate of 2.8 Gb/s.

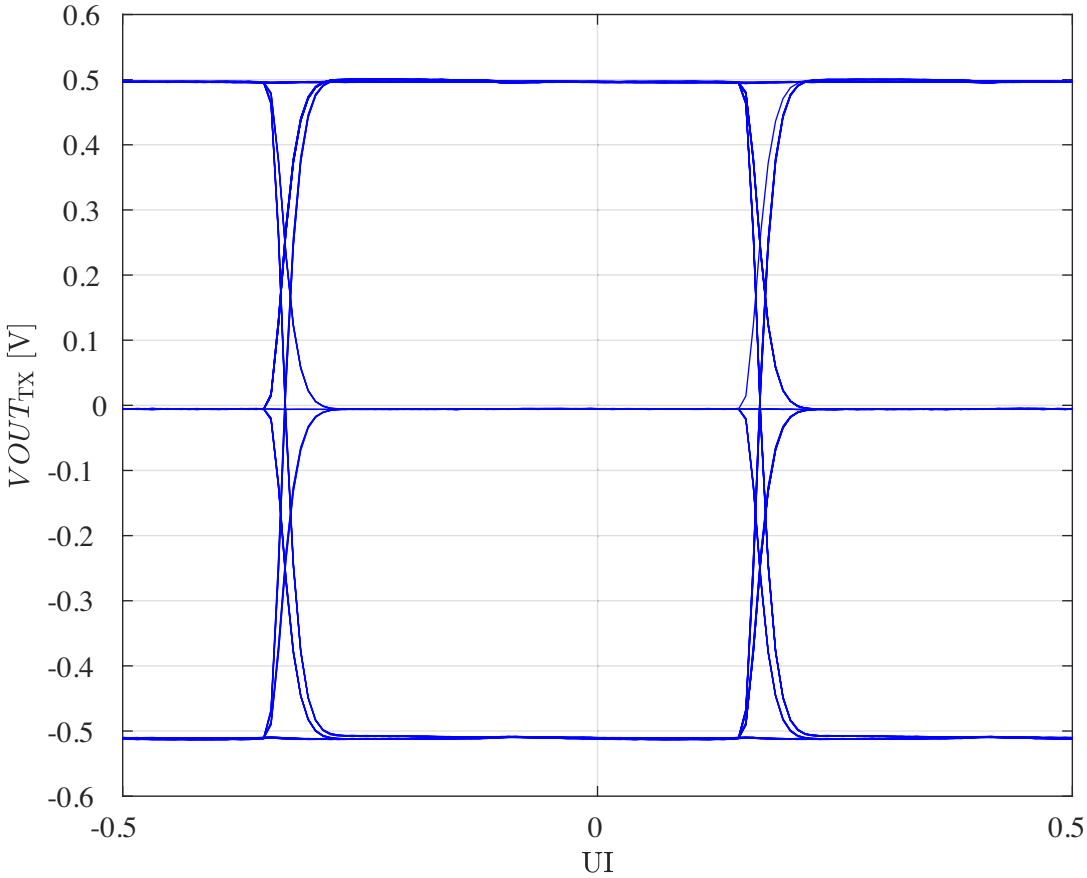


Figure 4.46: The eye diagram of the TX-DAC simulated with the analog extracted model at the data rate of 1.125 Gb/s.

4.12.5 Power Consumption

The power consumption of the DAC pair is calculated at different operating frequencies and is summarized in Table. 4.2 for each of the analog and digital power supplies for 1.2 V and 0.8 V voltage levels. The total power consumption for the maximum data rate of 11.2 Gbps is 44 mW, resulting in 1.96 mW/Gb/s for each of the DACs. The highest power consumption out of the listed supplies, avdd12 as the main driver supply driving the channel, consumes the most power.

Data rate	avdd12	avdd	dvdd12	dvdd	Total
11.2 Gbps	37 mW	2.2 mW	1 mW	3.8 mW	44 mW
5.6 Gbps	29.6 mW	1.6 mW	0.8 mW	2.6 mW	34.6 mW
2.8 Gbps	26.9 mW	1.2 mW	0.7 mW	2.1 mW	31.9 mW
1.125 Gbps	24.4 mW	1.1 mW	0.6 mW	1.9 mW	28 mW

Table 4.2: Power consumption of the TX-DAC and EC-DAC pair from its four separated supplies and the total power consumption simulated at different data rates.

5 Measurments

In this chapter first, the setup in order to test the fabricated chip is discussed. To connect the input and output signals as well as power supplies, a package solution is chosen and the Printed Circuit Board (PCB) to characterize such chip is discussed. Moreover, the echo cancellation performance of the DAC is tested and characterized as well as automotive Ethernet compliance tests on the TX side of the transceiver.

5.1 Test Chip

In order to test the chip, a package solution with a QFN 60-pin package is chosen. The bond wires within the packaged chip have 1 mil diameter and are out of gold. The test chip is shown in Fig. 5.1.

In order to minimize the bond wire length on the outputs of the DACs, the test chip is placed with an offset in the cavity of the QFN package as shown in Fig. 5.1. It is considered that the mismatch between the length of the bond wires between the TX and EC outputs to be minimized. The long bond wires on the outputs of the DAC are not desired as they limit the bandwidth of the output signals and add non-linearity between the differential outputs due to their mismatch in impedance. Moreover, the s-parameter test to measure the return loss of the outputs is affected as well by the bond wires. This will be discussed in detail in Sec. 5.5.4.

The blocks on the test chip are the SPI slave, Direct Digital Synthesizer (DDS), clock squarer, and TX-EC-DACs with its dedicated digital processing unit.

The DDS feeds the DACs with digital input signals, enabling the characterization of the dynamic performance of the DAC as well as PAM digital values to perform eye diagram analysis on the DAC. The characterization of the dynamic performance is done by feeding the values of a single tone sinusoidal signal.

The DDS inputs and 8-bit low-frequency digital bus registers from the SPI enable changing the frequency of the single tone sinusoidal waveform. Moreover, the DDS has an 8-bit wide 256 words memory registers, which are programmable via the SPI. The use of these memory registers enable loading PRBS PAM waveform values into the DACs to perform eye diagram analysis.

The SPI slave on-chip is a bridge between the SPI master, which translates the data from the USB port and brings it to the inputs registers in the DDS and TX-EX-DACs. The TX-EC-DACs use the DC registers from the SPI slave to set the number of parallel branches enabled to calibrate the output driver impedance across corners as discussed in Sec. 4.4. Moreover, the SPI registers enable selecting the phase of the clock signal to sample the data coming from the DDS as discussed in Sec. 4.11.

The clock squarer inputs a differential sinusoidal signal from a signal generator up to the frequency of 5.6 GHz. The clock squarer is low jitter limiting amplifier which provides the clock signal with rise/fall time less than 10 ps for 100 fF capacitance as the load for the maximum peak-peak jitter of 90 fs [23].

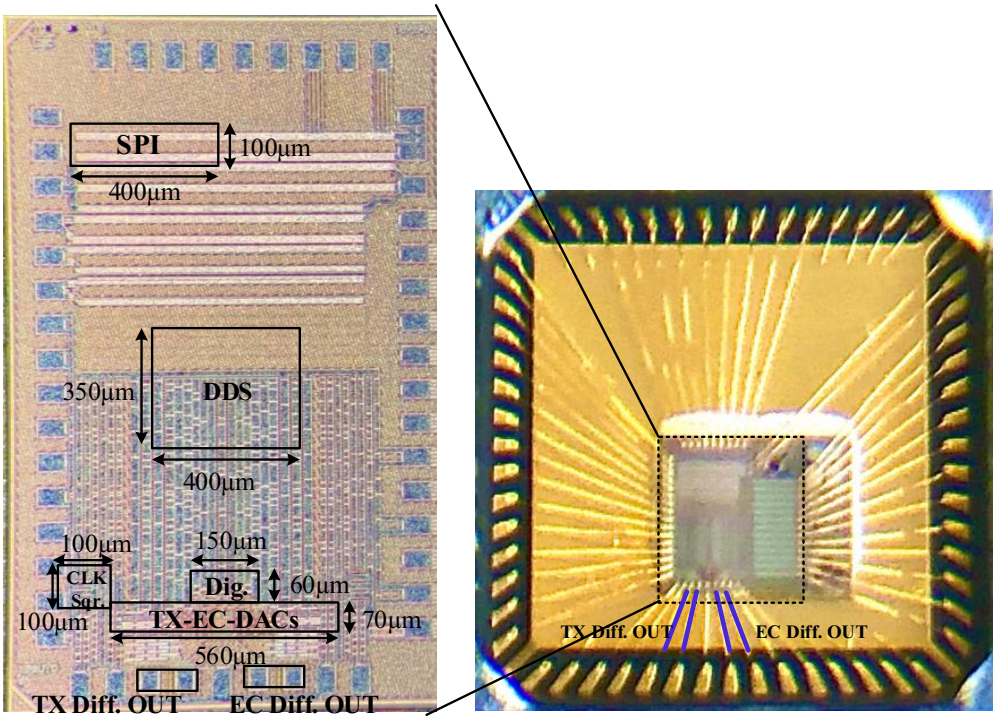


Figure 5.1: The chip photo showing DACs, clock squarer, DDS and SPI.

5.2 PCB Design

In order to design the PCB to test the chip, different signals that need to be connected on the chip are introduced and are shown on the fabricated PCB as depicted in Fig. 5.2. The power supplies for the test chip are as:

- avdd for the clk squarer and DACs
- avdd12 and dvdd12 for DACs
- dvdd for DACs
- dvdd_dig for DDS and SPI
- dvdd18 for SPI

It is noticed that the digital power supply of the DACs and the rest of the digital blocks on the chip are separated to minimize the digital noise from the digital blocks, DDS, and SPI that can be coupled into the sensitive analog supplies. Furthermore, the SPI is controlled via SPI master that bridged USB-to-SPI via CP2130 [24] communicating with 1.8 V supply level.

The SPI master communicates with the SPI slave via on-chip level shifters provided by using standard pads for the SPI digital data communication. Therefore, two supply levels of 1.8 V and 0.8 V are provided on the PCB board to operate the on-chip level shifters and SPI slave.

A connector is placed on the PCB, which provides the data communication signals necessary for the SPI slave. The detailed design of the SPI slave and how this communication is carried out is out of the scope of this work to be included here.

The differential input of the clock squarer and the differential outputs of TX-DAC and EC-DAC are connected to SMA female connector via a transmission line. The transmission lines are carefully designed and laid out so that the differential signals has an impedance of 100 Ω and single-ended impedance of 50 Ω. These values match the outputs of the TX-EC-DACs as well as the input of the measurement unit.

Given the parameters set by the PCB provider - each of the transmission lines with the width of 0.2 mm and with 0.13 mm distance from each other and 0.1 mm distance from the ground plane filling around it - it gives differential impedance of 102.827 Ω and single-ended impedance of 49.8925 Ω. Considering the limitations of the grid set by the PCB provider, this is the closest possible design to the nominal impedance required with the selected PCB vendor.

Moreover, there is an AC coupling capacitor 10 nF placed in series in the transmission line path to block any DC current going to the outputs of the DAC or the inputs of the clock squarer, damaging the gate of the input devices. The choice of the coupling capacitor should be the ones that are highly linear and with a low series impedance to mitigate the non-linearity, which it can add to the outputs of the DACs. Finally, this series capacitor with the impedance of the transmission line behaves like a high pass filter with the cut-off frequency of

$$f_{\mathrm{3dB,HPF}} = \frac{1}{2\pi 10nF \times 50\Omega} = 318.3\,\mathrm{KHz} \tag{5.1}$$

which given the operating frequency of the inputs and the outputs is not a limiting factor.

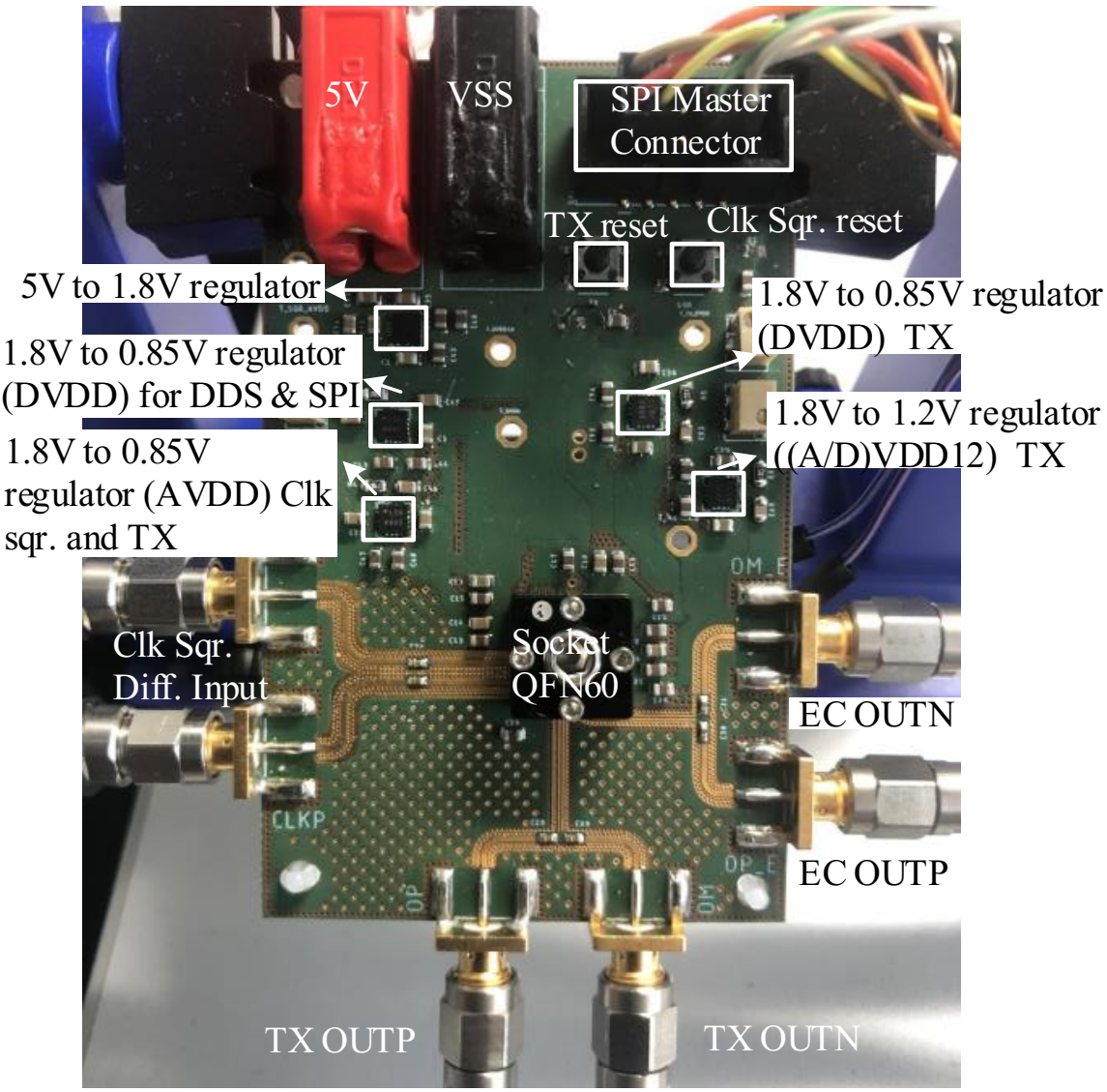


Figure 5.2: The board with a 5 V power supply input, 5 onboard high-speed voltage regulators, an SPI master connector, and 6 SMA connectors for the clock squarer differential input signal and the TX and EC differential output signals.

5.3 QFN Packaging

As mentioned in detail in Sec. 3.4.3, QFN-60 package shown in Fig. 5.3 with a cavity size of 5.3 mm × 5.3 mm and a die size of 2.5 mm × 2 mm is chosen to connect the die to test. The die is placed with an offset to the center to have shorter bond wires on the lower bottom of the package, where the outputs of the DACs are connected. The reasoning for this choice is discussed in detail in Sec. 5.1.

The simplified circuit schematic of Fig. 3.22 shows how the bond wires are modeled in the supplied mesh. The gold bond wires assumed to have an average length of 2 mm with diameter of 30.48 μm. The estimated inductance and resistance for a 2 mm of this bond wire is estimated to be $L_s = 2\,\text{nH}$ and $R_{s,\text{bond}} = 200\,\text{m}\Omega$.

To mitigate the effect of the inductance of the bond wire, the decoupling capacitance possible to be implemented on-chip is maximized. Thus, arrays of PMOS devices with its gate connected to the ground and the drain and source connected to positive supply voltage are used. Also, to increase the capacitance further, a metal sandwich of 8 metal layers is closely implemented on top of it.

The silicon area around the DACs is covered with such decoupling capacitors to damp the inductance effect. Furthermore, the impedance of the bond wire can be used in the source degeneration technique discussed in detail in Sec. 3.4.3.

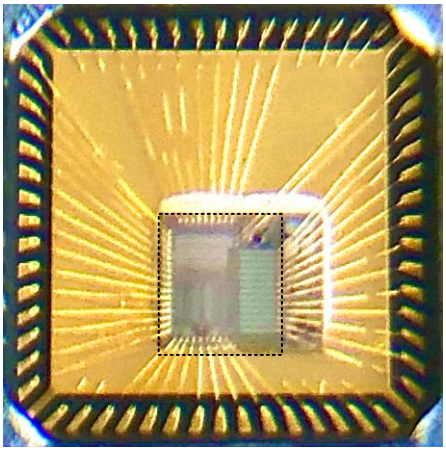


Figure 5.3: The image of the QFN-60 package used with the silicon die bonded.

5.3.1 Source Degeneration Technique

It was shown that to cancel out the INL error caused due to the non-linearity of the switches with a variation of its drain-source voltage, a total of 1 Ω can be used in the power supply

mesh path. Given the bond wire of each of the supply rails, contribute $R_{\mathrm{s,bond}} = 200\,\mathrm{m\Omega}$ to the series impedance on the supply, it is enough to include another $R_{\mathrm{s,chip}} = 300\,\mathrm{m\Omega}$ on each of the positive and negative supply rails of avdd12. The implementation of this impedance is possible with careful layout of the supply rails from the pads down to the source node of the switches.

5.3.2 Echo Canceling Performance

In order to test the echo canceling performance of the DAC pair, an on-chip hybrid is needed to carry out the subtraction and measure the output residue of the TX-DAC and EC-DAC subtraction. However, the design and implementation of the on-chip hybrid are not in the scope of this work.

To test the echo canceling performance, all four outputs of the DAC pair are connected to a sampling scope. The sampling scope has a bandwidth of 8 GHz which is higher than the maximum sampling frequency of 5.6 GHz operating the DACs.

A PRBS PAM4 signal is fed into the DACs and the TX differential outputs are mathematically subtracted from the EC differential outputs to test the echo cancellation performance. Considering that, using this approach is not the same as using an on-chip hybrid, as different possible sources of mismatch can degrade the performance. Such possible mismatch sources are a mismatch between the bond wire lengths or the connection on the outputs, mismatch between the transmission lines due to the process, the mismatch between the AC coupling capacitors on the outputs, the mismatch between the connectors and cables connecting the output signals to the sampling scope.

The mathematical subtraction of the TX-DAC and EC-DAC for each of the operating frequencies in the scope of this work is depicted in Fig. 5.4, Fig. 5.5, Fig. 5.6 and Fig. 5.7.

The residue errors and transmission power reductions at RX measured at different bit rates are summarized in Tab. 5.1.

Bit-rate [Gb/s]	peak-peak error residue [mV]	power reduction [dB]
11.2	61.09	24.28
5.6	50.16	25.99
2.8	47.19	26.52
1.125	43.46	27.24

Table 5.1: The residue errors and transmission power reductions at RX, measured at different sampling speeds and data rates.

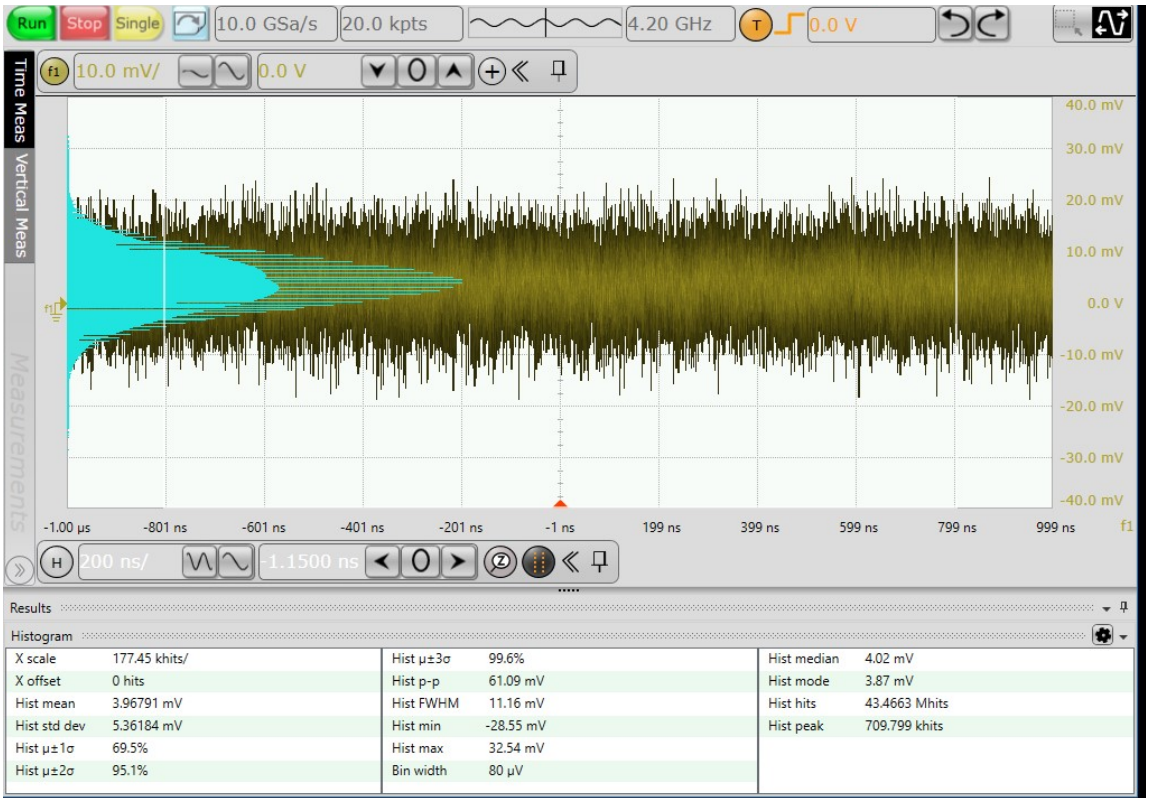


Figure 5.4: TX differential output signal subtracted from EC differential output signal at 11.2 Gb/s suitable for 10GBase-T1. The peak-peak residue error is 61.09 mV with a sigma of 5.36 mV, respectively. This leads to 24.28 dB of transmit power reduction at the RX input.

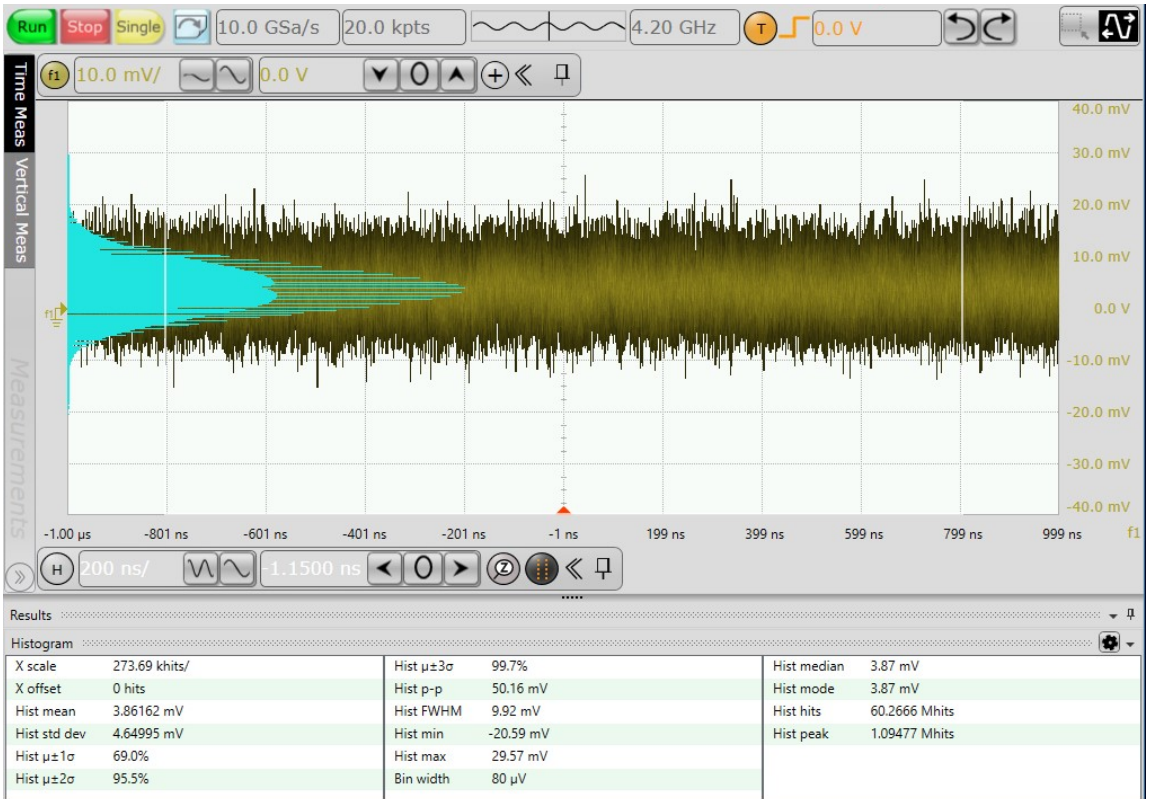


Figure 5.5: TX differential output signal subtracted from EC differential output signal at 5.6 Gb/s suitable for 5GBase-T1.The peak-peak residue error is 50.16 mV with a sigma of 4.65 mV, respectively. This leads to 25.99 dB of transmit power reduction at the RX input.

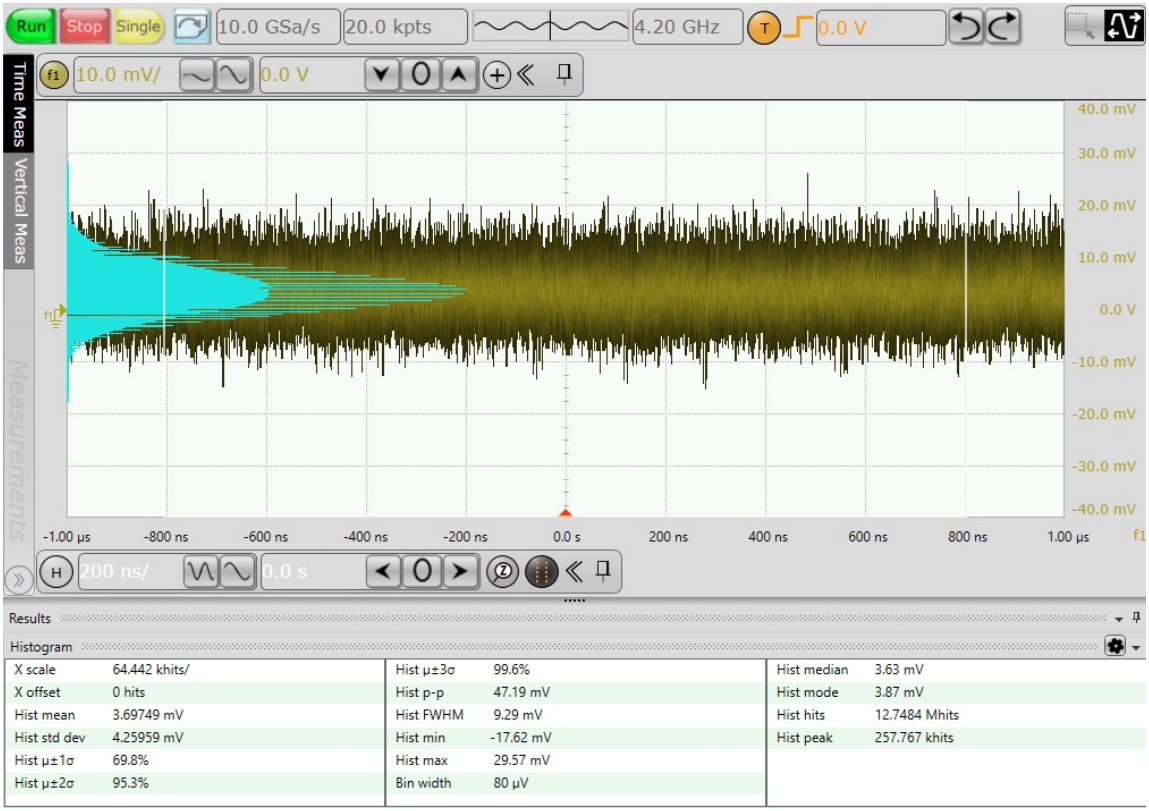


Figure 5.6: TX differential output signal subtracted from EC differential output signal at 2.8 Gb/s suitable for 2.5GBase-T1. The peak-peak residue error is 47.19 mV with a sigma of 4.26 mV, respectively. This leads to 26.52 dB of transmit power reduction at the RX input.

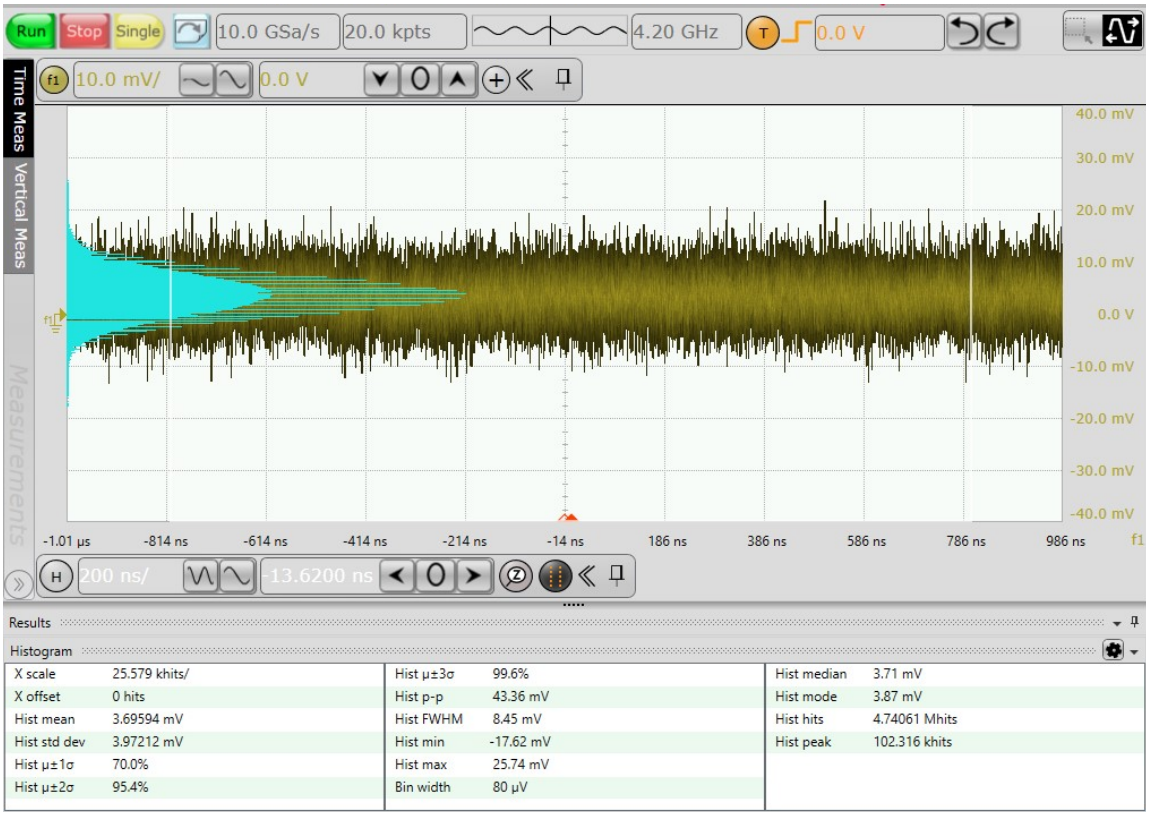


Figure 5.7: TX differential output signal subtracted from EC differential output signal at 1.125 Gb/s suitable for 1GBase-T1. The peak-peak residue error is 43.36 mV with a sigma of 3.97 mV, respectively. This leads to 27.24 dB of transmit power reduction at the RX input.

5.4 Dynamic DAC Properties

5.4.1 Differential Signal

To characterize the dynamic properties of the DAC, the differential outputs of the TX-DAC is connected to a differential to single-ended balun while the outputs of the EC-DAC is terminated. The single-ended node of the balun is connected to a spectrum analyzer.

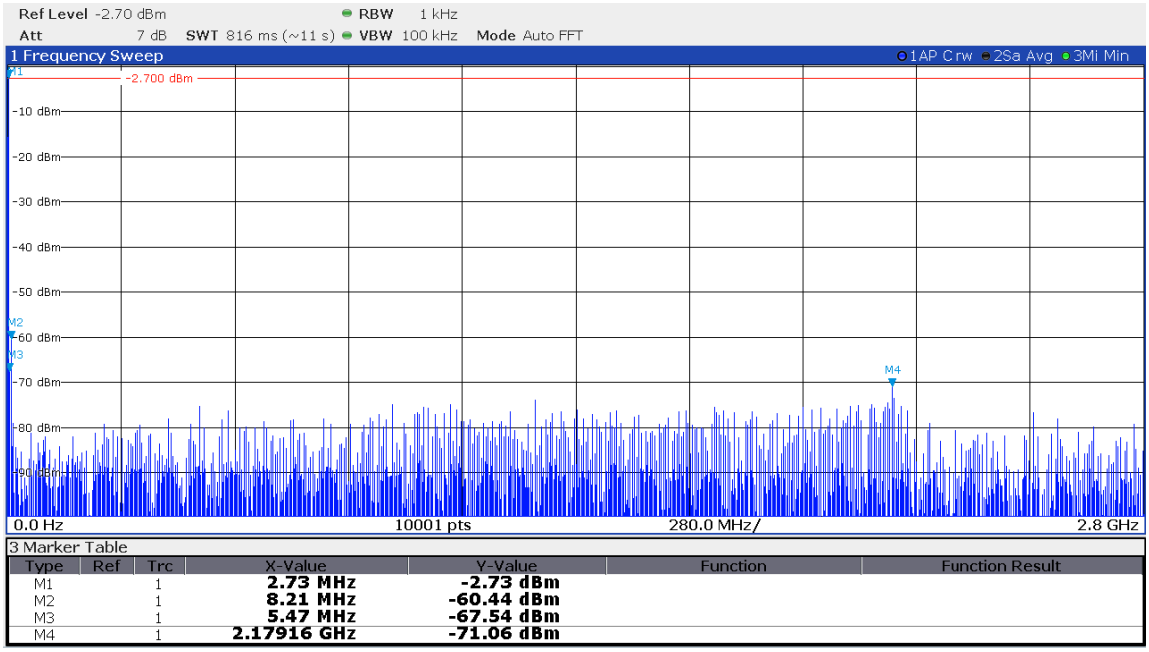
While the output of the spectrum analyzer can accurately verify the SFDR of the DAC by finding the highest frequency component on the frequency spectrum after the main signal, calculating ENOB and SNR is not done directly on the spectrum analyzer. Therefore, the data is fed into a calculator to give the measured SNR and ENOB for each of the measurements. The screenshot of the spectrum analyzer and the annotated frequency spectrum which is full scaled to bring the main signal frequency component to 0 dB are plotted in Fig. 5.8 and Fig. 5.9 operating at 5.6 GS/s.

Moreover, both the measured and the simulated ENOB and SFDR of the TX-DAC operating at 5.6 GS/s while sweeping the input frequency tone from a low-frequency tone to near Nyquist frequency is depicted in Fig. 5.10 and Fig. 5.11, respectively. The measured ENOB shows to be higher than 6.8 bits across the frequency spectrum range up to Nyquist frequency, and the measured SFDR is higher than 50 dB across the frequency spectrum range up to Nyquist frequency. The difference between the analog extracted simulations and measurements shows to be not consistent over the frequency range with having more differences between 400 MHz and 2 GHz.

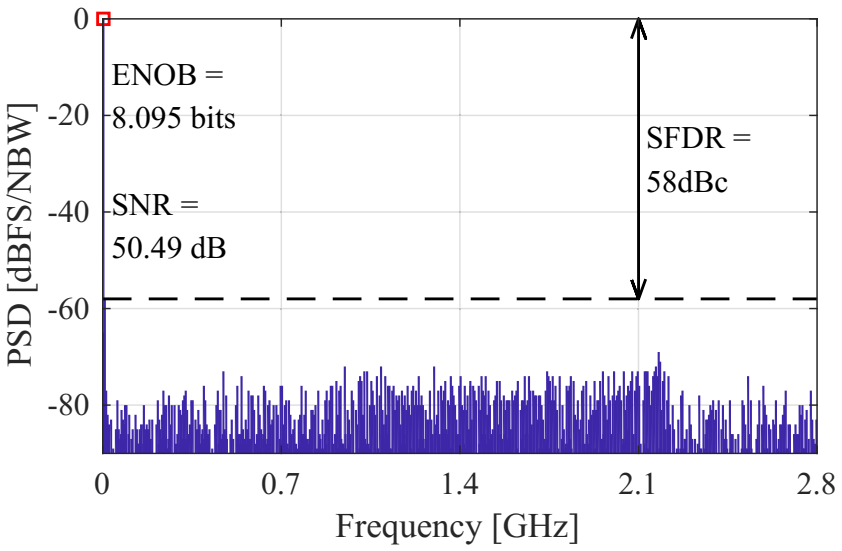
The frequency spectrum of the TX-DAC measured operating at 2.8 GS/s inputting a low-frequency and a high-frequency single-tone sinusoidal signal is plotted in Fig. 5.12 and Fig. 5.13, respectively. Moreover, both the measured and the simulated ENOB and SFDR of the TX-DAC operating at 2.8 GS/s while sweeping the input frequency tone from a low-frequency tone to near Nyquist frequency is depicted in Fig. 5.14 and Fig. 5.15, respectively.

The measured ENOB shows to be higher than 7.5 bits across the frequency spectrum range up to Nyquist frequency, and the measured SFDR is higher than 55 dB across the frequency spectrum range up to Nyquist frequency. The difference between the analog extracted simulations and measurements shows to be not consistent over the frequency range, with ENOB difference increasing as the input frequency tone due to the drop on SNR.

The frequency spectrum of the TX-DAC measured operating at 1.4 GS/s inputting a low-frequency and a high-frequency single-tone sinusoidal signal is plotted in Fig. 5.16 and Fig. 5.17, respectively. Moreover, both the measured and the simulated ENOB and SFDR of the TX-DAC operating at 1.4 GS/s while sweeping the input frequency tone from a low-frequency tone to near Nyquist frequency is depicted in Fig. 5.18 and Fig. 5.19, respectively. The measured ENOB shows to be higher than 7.5 bits across the frequency spectrum range up to Nyquist frequency and the measured SFDR is higher than 49 dB across the frequency spectrum range up to Nyquist frequency.

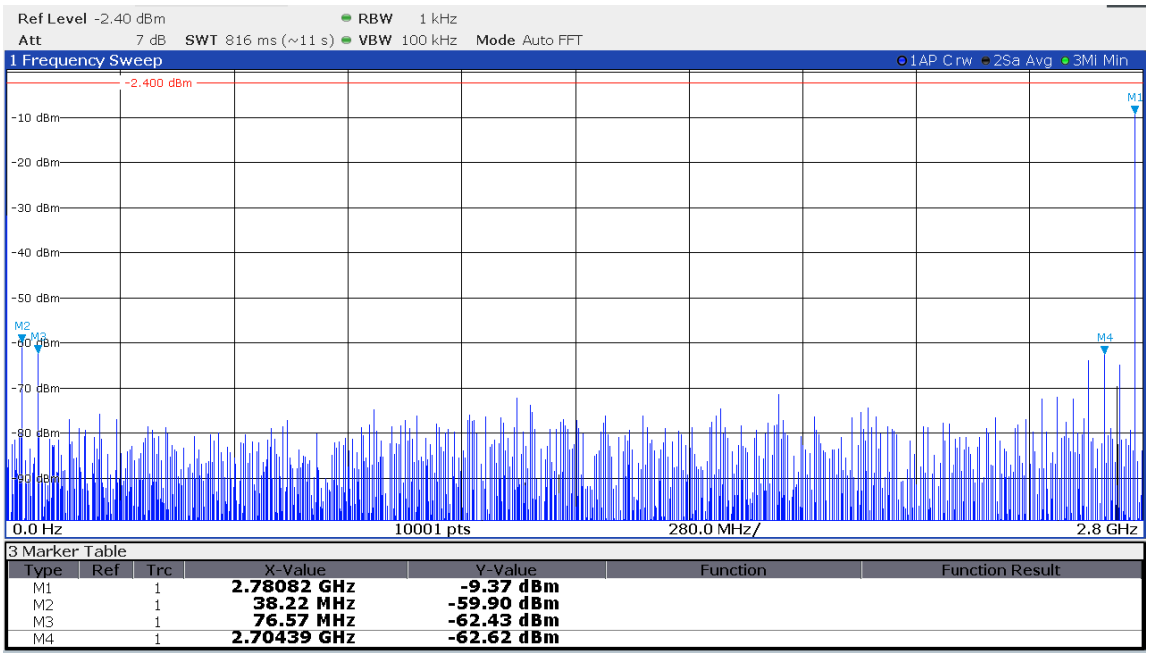


(a) Spectrum analyzer.

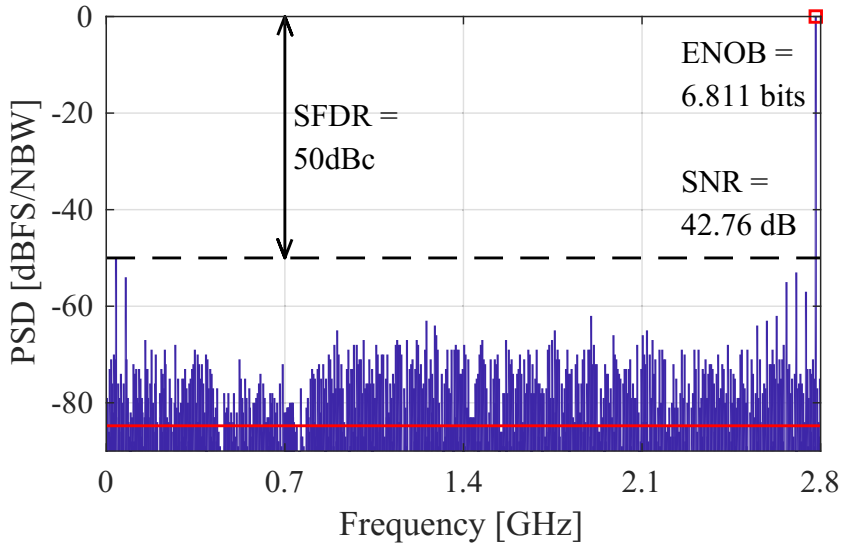


(b) Full scale annotated result.

Figure 5.8: The spectrum analysis of the TX-DAC operating at 5.6 GS/s inputting a low-frequency single-tone sinusoidal signal with (a) showing the spectrum analyzer screenshot and (b) the same data plotted with the full-scale signal, annotating the ENOB, SNR, and SFDR parameters.



(a) Spectrum analyzer.



(b) Full scale annotated result.

Figure 5.9: The spectrum analysis of the TX-DAC operating at 5.6 GS/s inputting a high-frequency single-tone sinusoidal signal with (a) showing the spectrum analyzer screenshot and (b) the same data plotted with the full-scale signal, annotating the ENOB, SNR, and SFDR parameters.

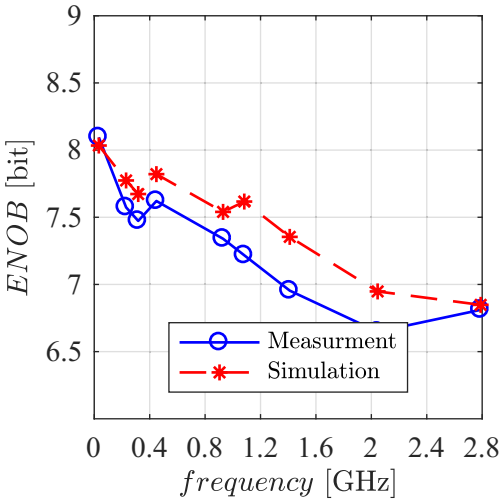


Figure 5.10: ENOB of TX-DAC measured operating at 5.6 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist with to the analog extracted simulation results.

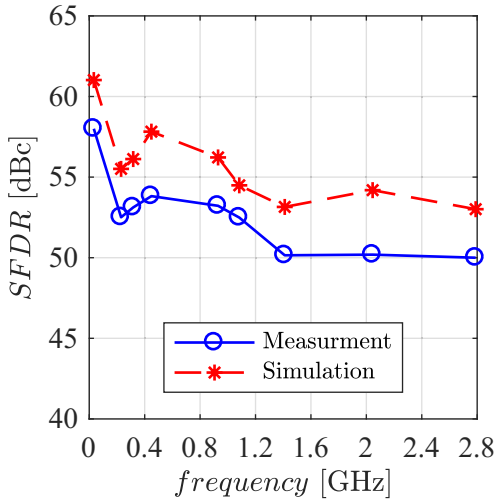
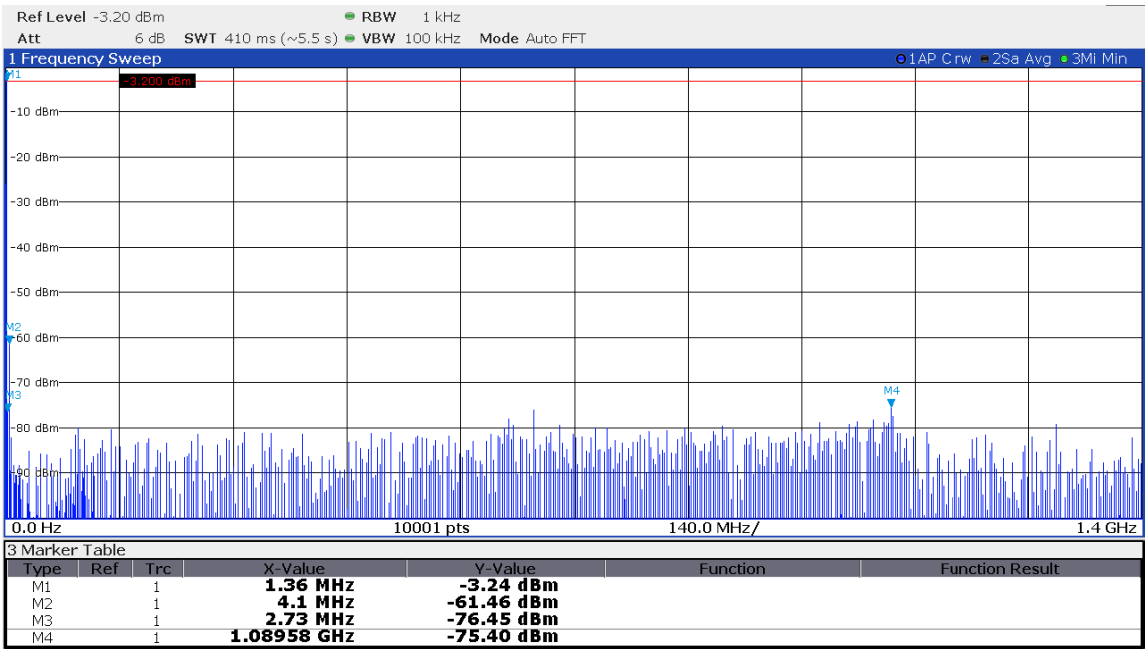
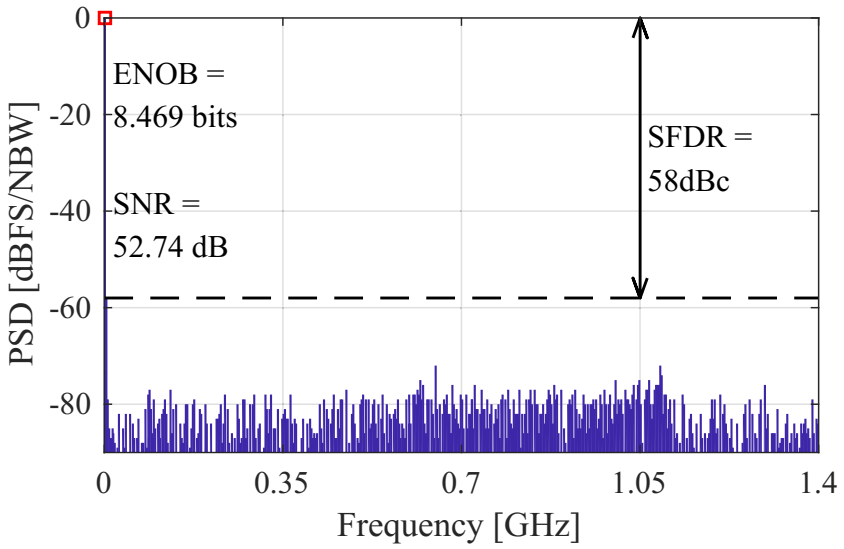


Figure 5.11: SFDR of TX-DAC measured operating at 5.6 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist with to the analog extracted simulation results.

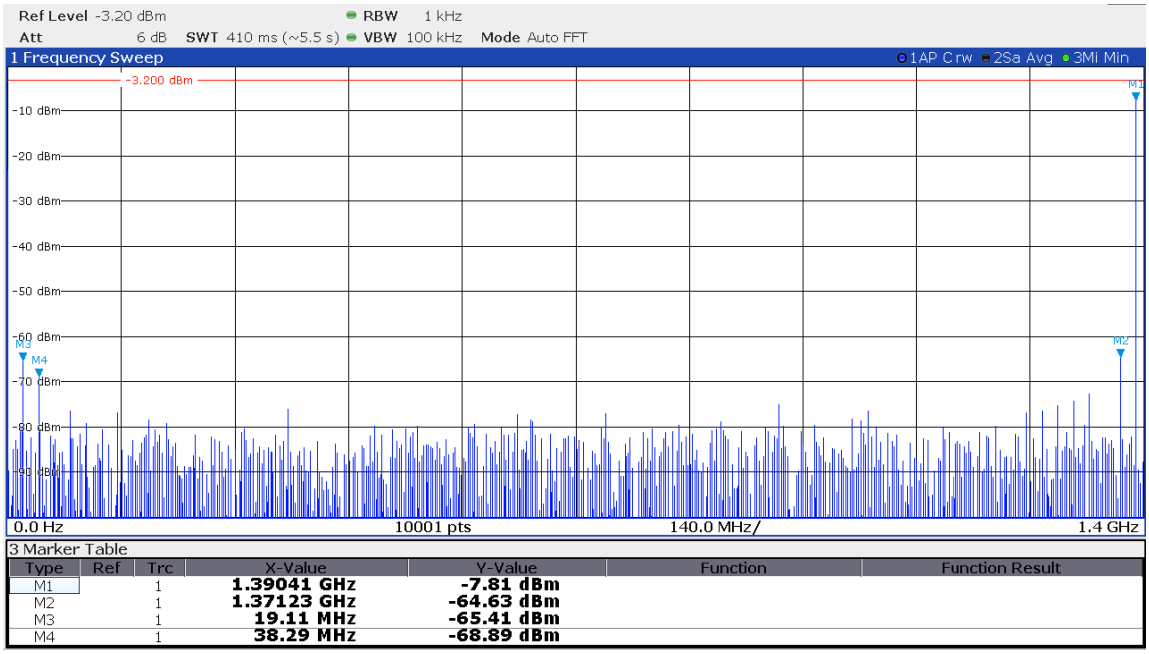


(a) Spectrum analyzer.

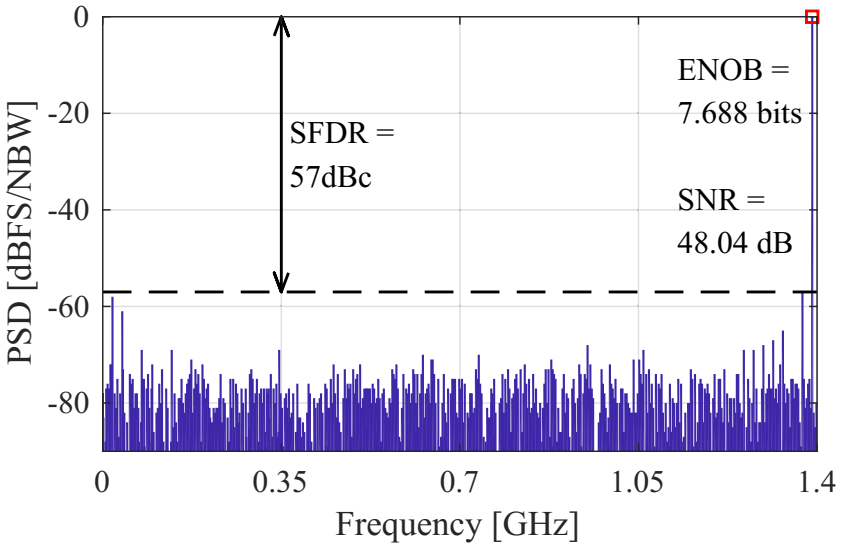


(b) Full scale annotated result.

Figure 5.12: The spectrum analysis of the TX-DAC operating at 2.8 GS/s inputting a low-frequency single-tone sinusoidal signal with (a) showing the spectrum analyzer screenshot and (b) the same data plotted with the full-scale signal, annotating the ENOB, SNR, and SFDR parameters.



(a) Spectrum analyzer.



(b) Full scale annotated result.

Figure 5.13: The spectrum analysis of the TX-DAC operating at 2.8 GS/s inputting a high-frequency single-tone sinusoidal signal with (a) showing the spectrum analyzer screenshot and (b) the same data plotted with the full-scale signal, annotating the ENOB, SNR, and SFDR parameters.

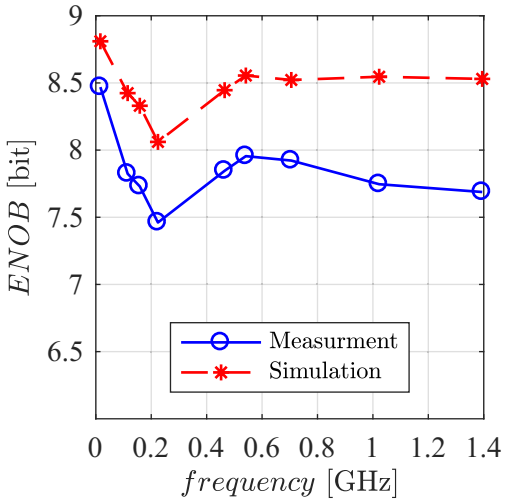


Figure 5.14: ENOB of TX-DAC measured operating at 2.8 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist with to the analog extracted simulation results.

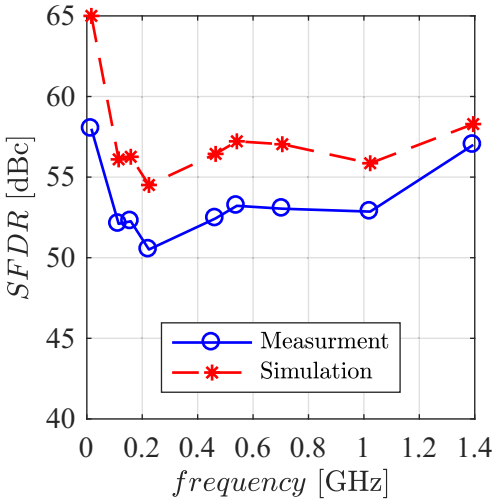
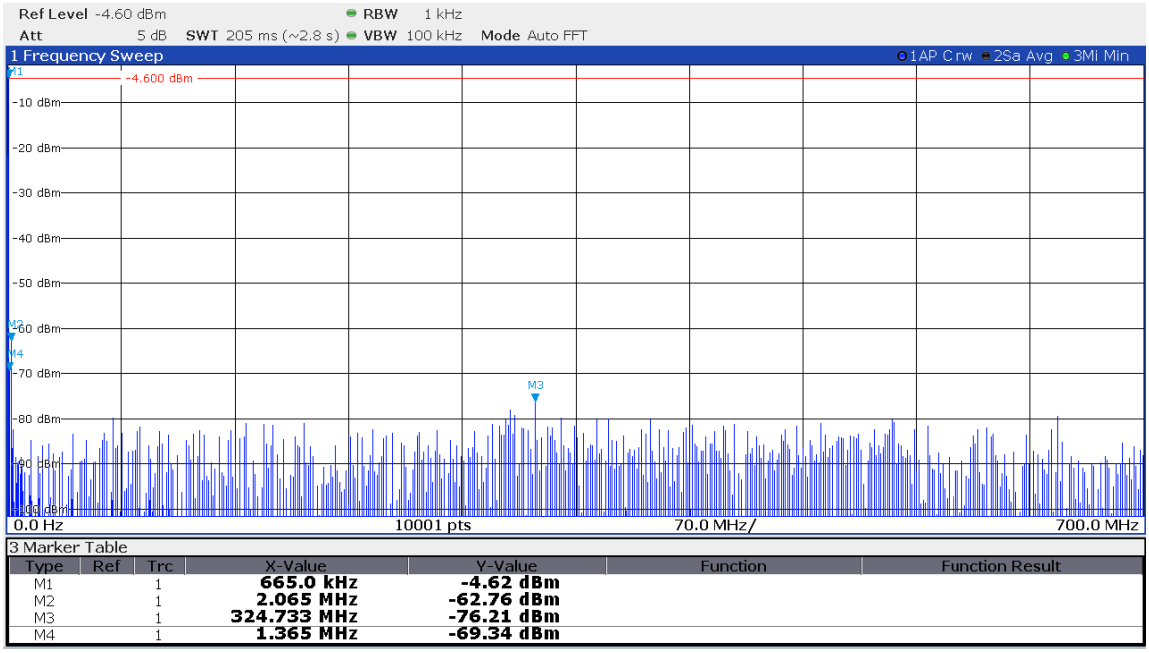
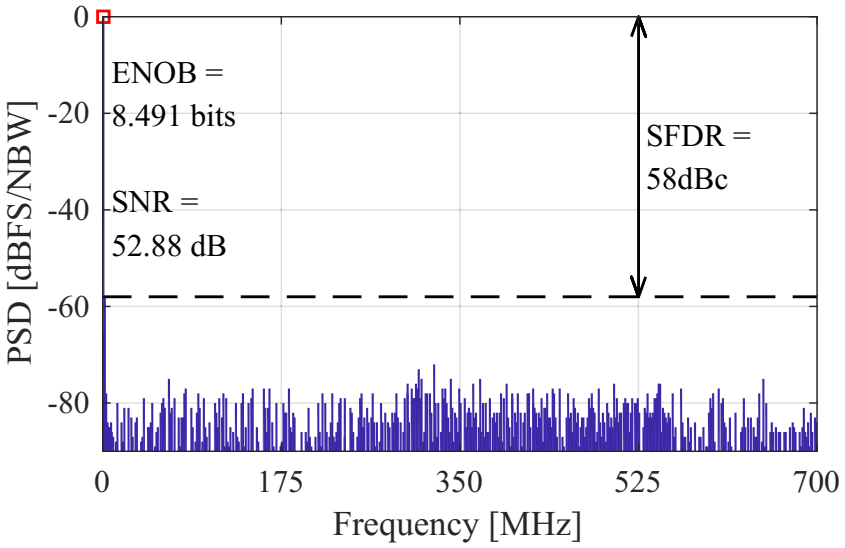


Figure 5.15: SFDR of TX-DAC measured operating at 2.8 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist with to the analog extracted simulation results.

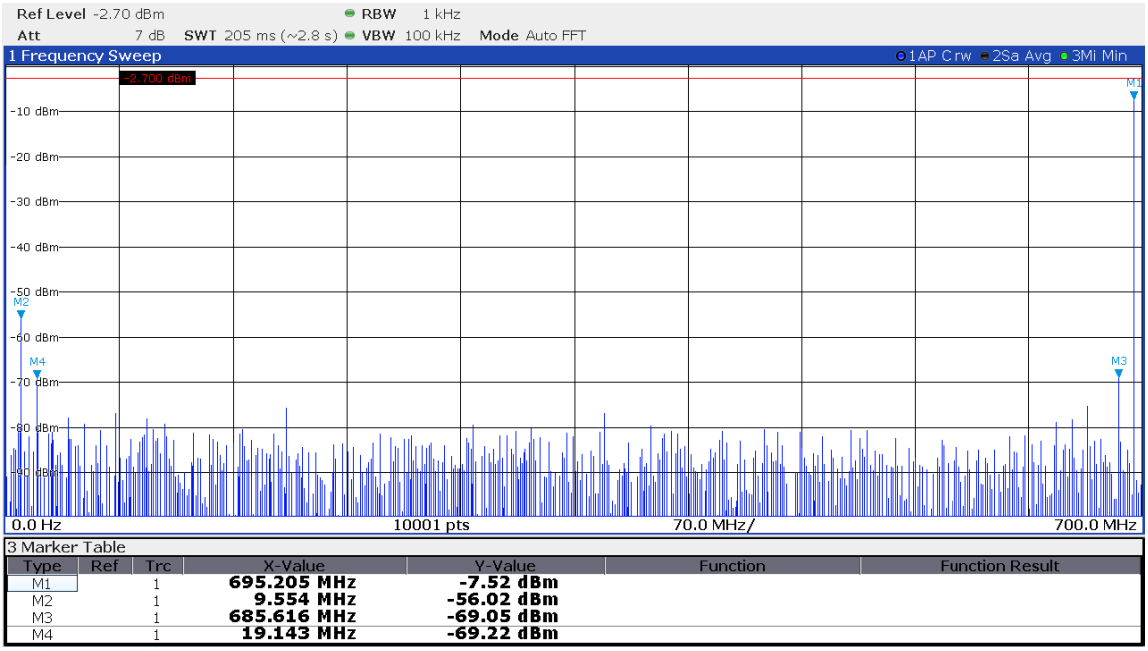


(a) Spectrum analyzer.

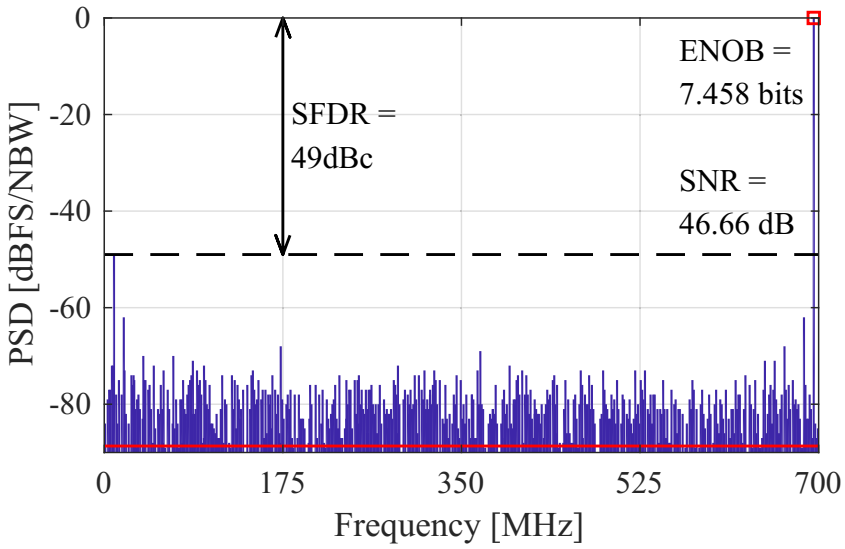


(b) Full scale annotated result.

Figure 5.16: The spectrum analysis of the TX-DAC operating at 1.4 GS/s inputting a low-frequency single-tone sinusoidal signal with (a) showing the spectrum analyzer screenshot and (b) the same data plotted with the full-scale signal, annotating the ENOB, SNR, and SFDR parameters.



(a) Spectrum analyzer.



(b) Full scale annotated result.

Figure 5.17: The spectrum analysis of the TX-DAC operating at 1.4 GS/s inputting a high-frequency single-tone sinusoidal signal with (a) showing the spectrum analyzer screenshot and (b) the same data plotted with the full-scale signal, annotating the ENOB, SNR, and SFDR parameters.

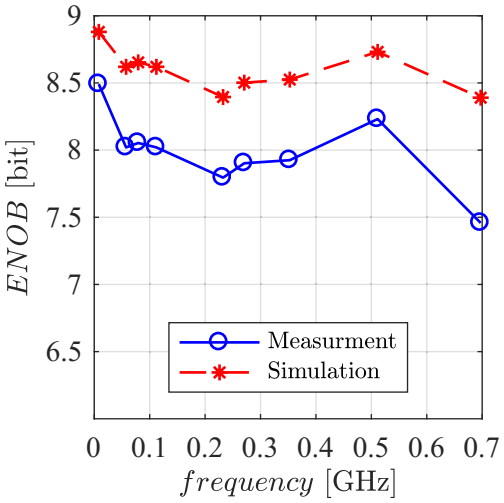


Figure 5.18: ENOB of TX-DAC measured operating at 1.4 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist with to the analog extracted simulation results.

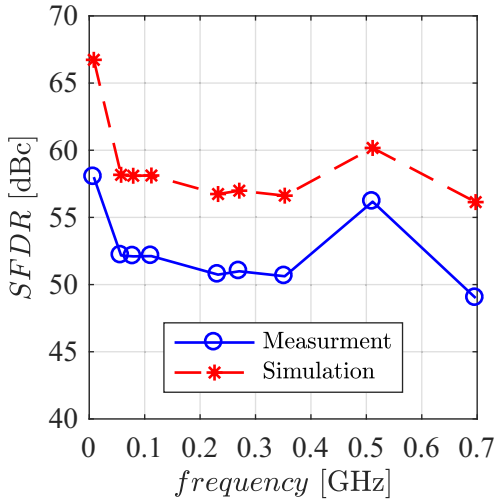


Figure 5.19: SFDR of TX-DAC measured operating at 1.4 GS/s inputting a single tone sinusoidal signal with frequency tone sweeping up to Nyquist with to the analog extracted simulation results.

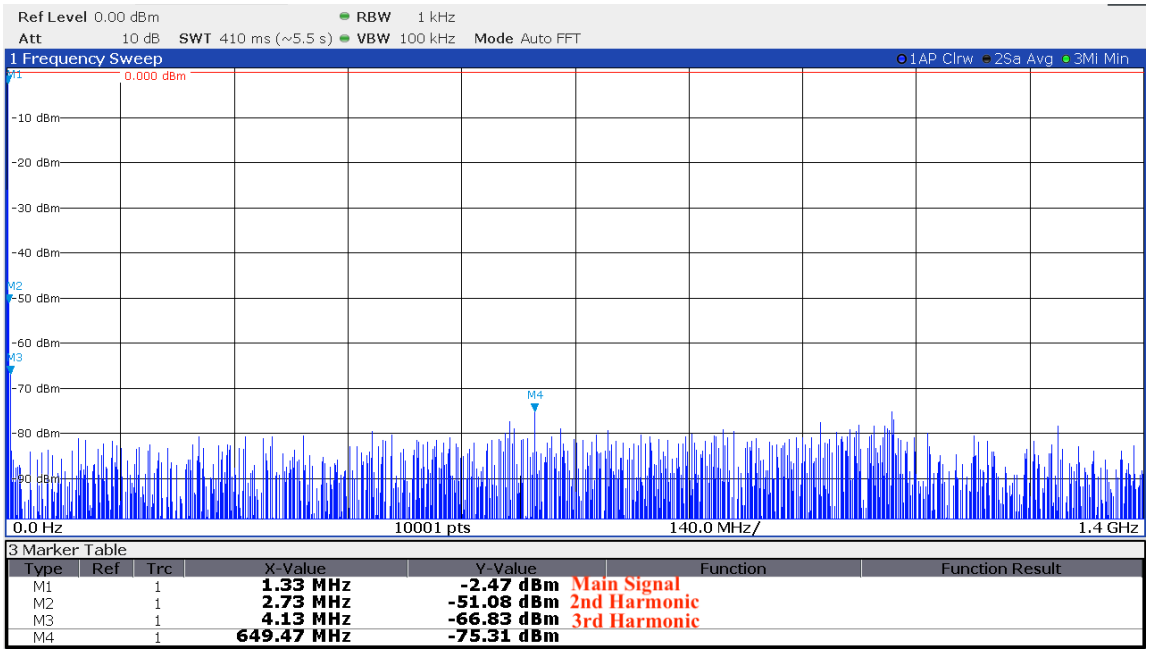
5.4.2 Single Ended Signal

In order to measure the performance of the differential signalling in reducing the even harmonics of the main signal, here the measured spectrum analysis for both the single-ended signal and the differential signal inputting a low-frequency and high-frequency single-tone sinusoidal signal are shown in Fig. 5.20 and Fig. 5.21, respectively for operating at 2.8 GS/s and in Fig. 5.22 and Fig. 5.23, respectively for operating at 5.6 GS/s.

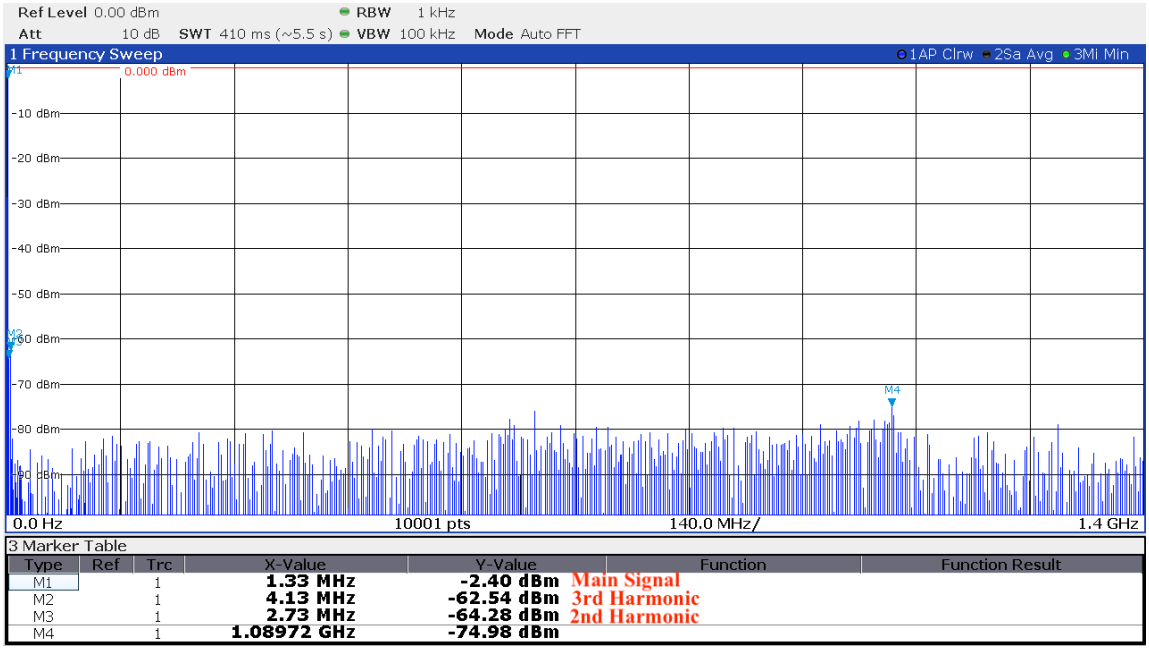
It is important to mention that the spectrum analysis shown in the figures here are measured with a packaged chip that is fully encapsulated. However, in all other measurements in this work, a packaged chip is not encapsulated and the medium surrounding the bond wires is air. Therefore, the spectrum analysis of the differential signaling in this section shows worse linearity comparing to the previous section, where differential signaling was presented.

The worsening of the performance is caused due to the encapsulation of the package, which increases the parasitic capacitance between the bond wires and worsens the interference between the output signals and power supply signals.

In each of the figures below, three frequency components are marked and numbered with their corresponding harmonic. At the operating frequency of 2.8 GS/s and 5.6 GS/s, the differential signalling comparing to the single-ended signalling shows an improved 2nd harmonic of 13 dB for inputting low-frequency sinusoidal signal and 19 dB for inputting high-frequency sinusoidal signal. It shows that the differential signaling performance in lowering the even harmonics is independent of the operating sample rate which shows the robustness of the layout design against high-frequency effects.

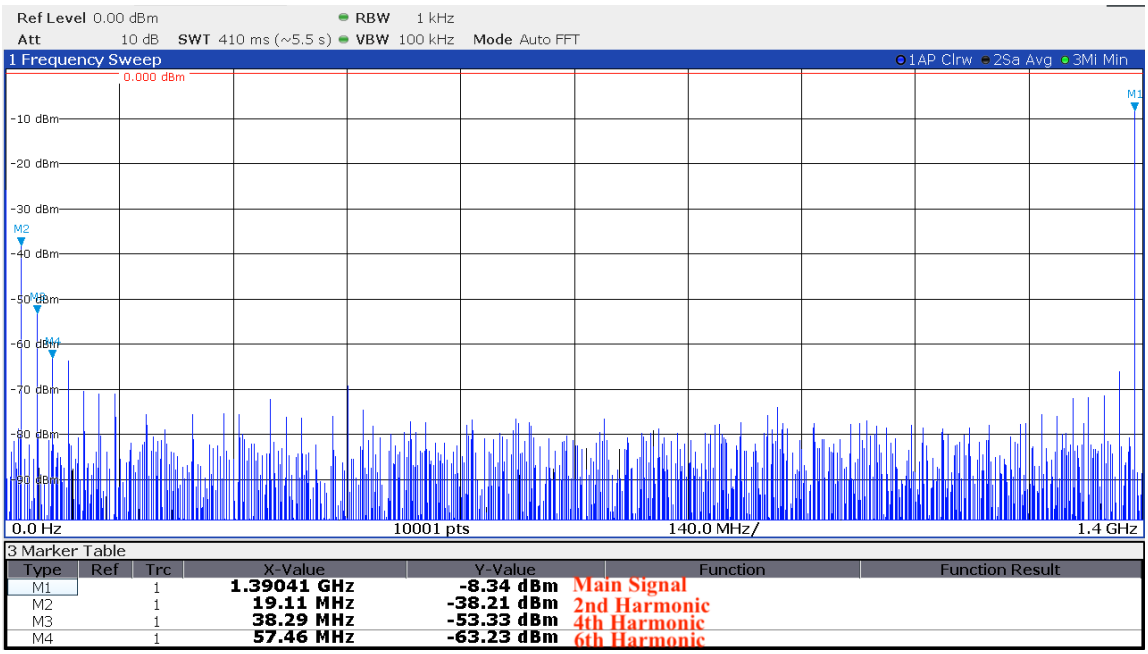


(a) Single ended output signal measurement.

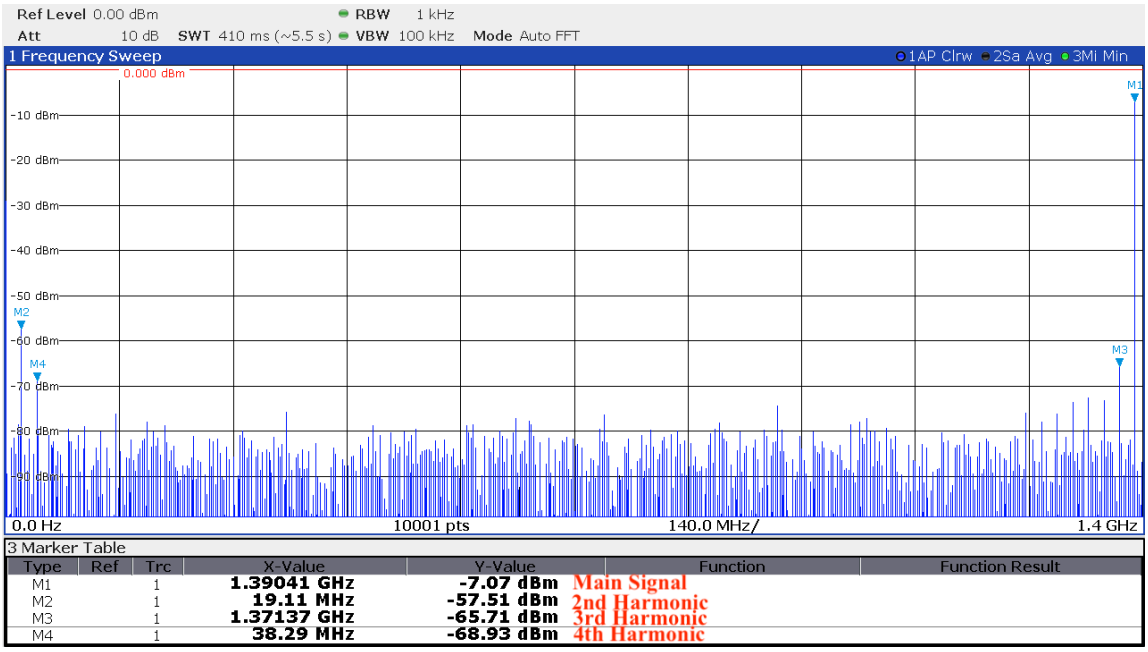


(b) Differential output signal measurement.

Figure 5.20: The spectrum analysis of the TX-DAC operating at 2.8 GS/s inputting a low-frequency single-tone sinusoidal signal (a) while only a single ended output is connected to the spectrum analyzer and (b) the differential output connected through a differential to single ended balun to the spectrum analyzer.

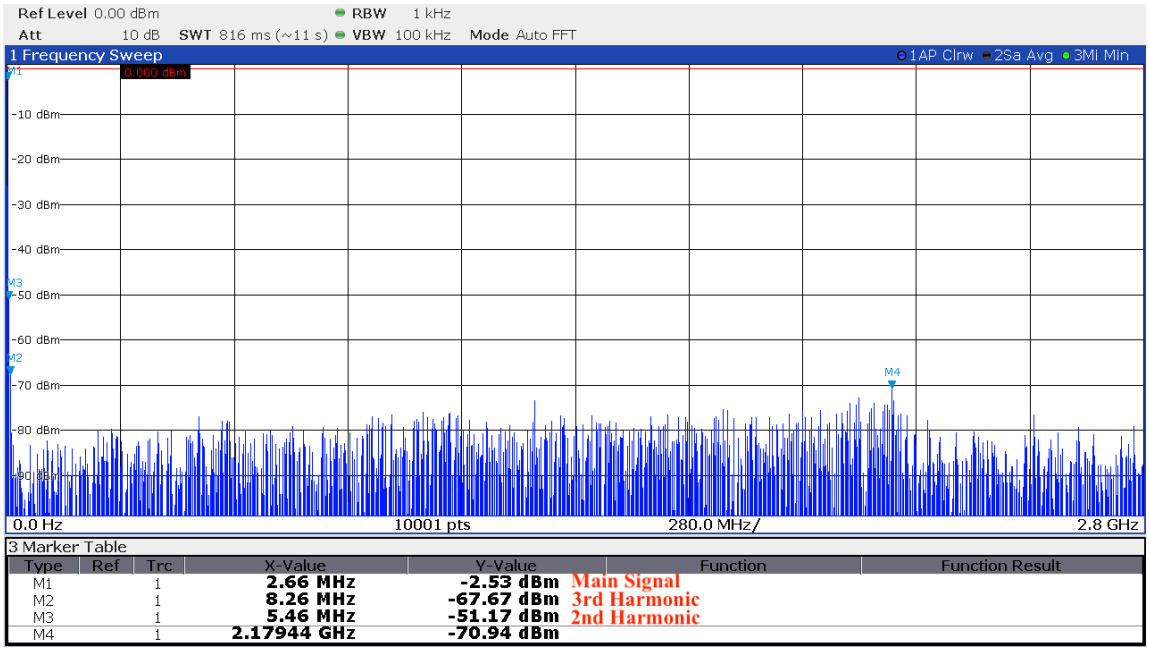


(a) Single ended output signal measurement.

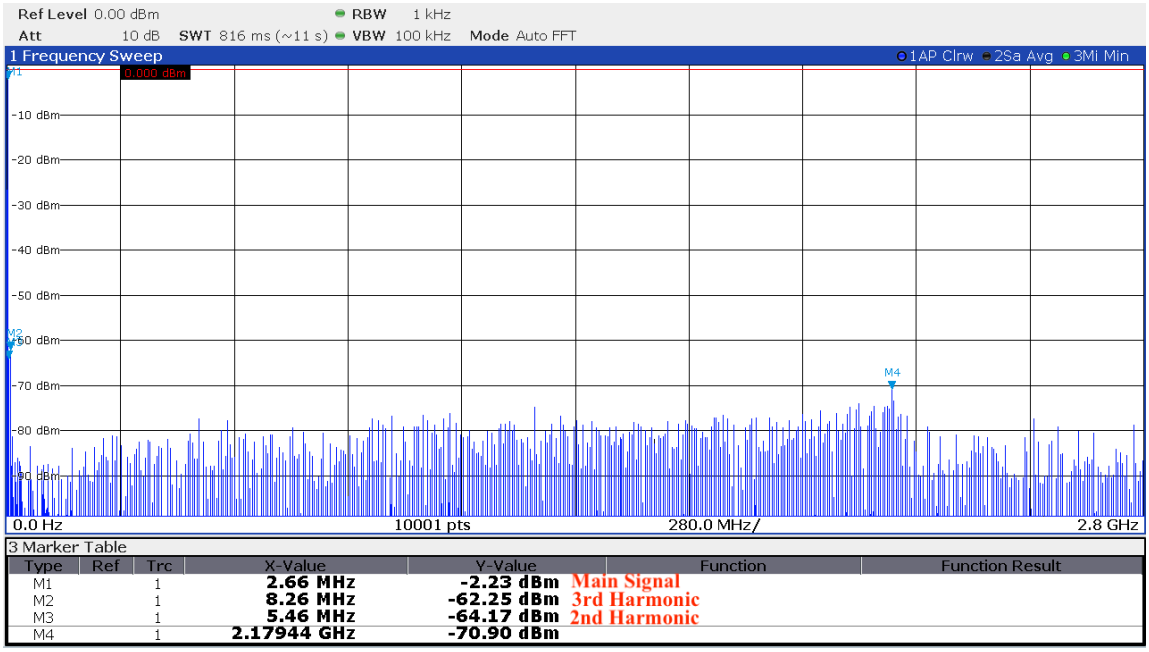


(b) Differential output signal measurement.

Figure 5.21: The spectrum analysis of the TX-DAC operating at 2.8 GS/s inputting a high-frequency single-tone sinusoidal signal (a) while only a single ended output is connected to the spectrum analyzer and (b) the differential output connected through a differential to single ended balun to the spectrum analyzer.

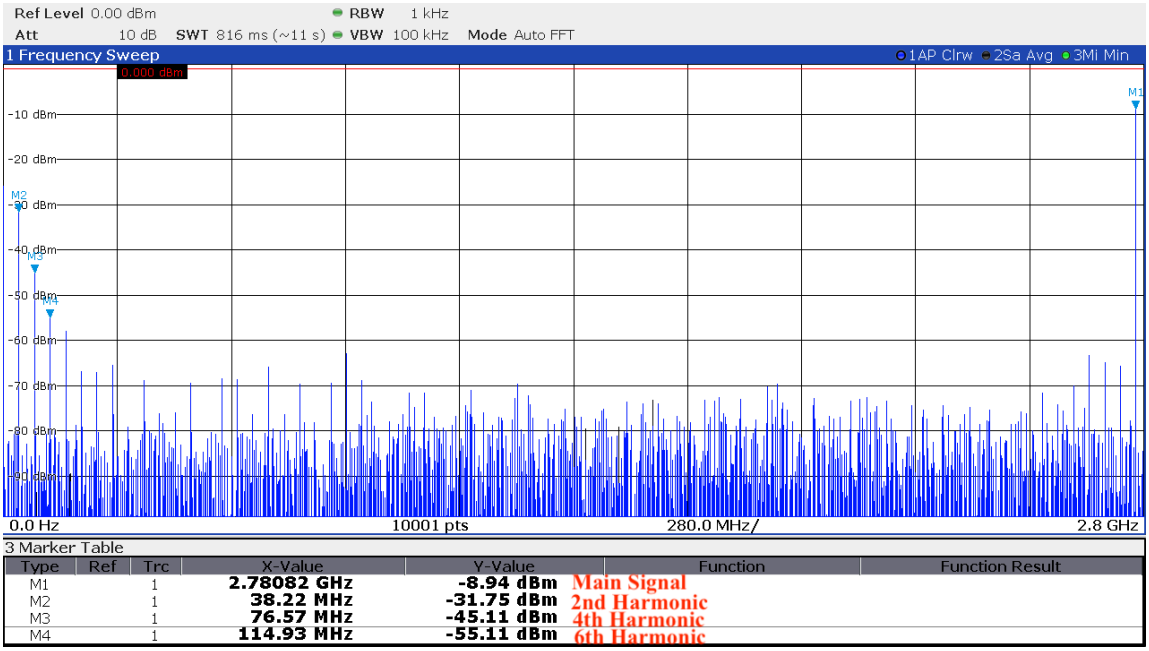


(a) Single ended output signal measurement.

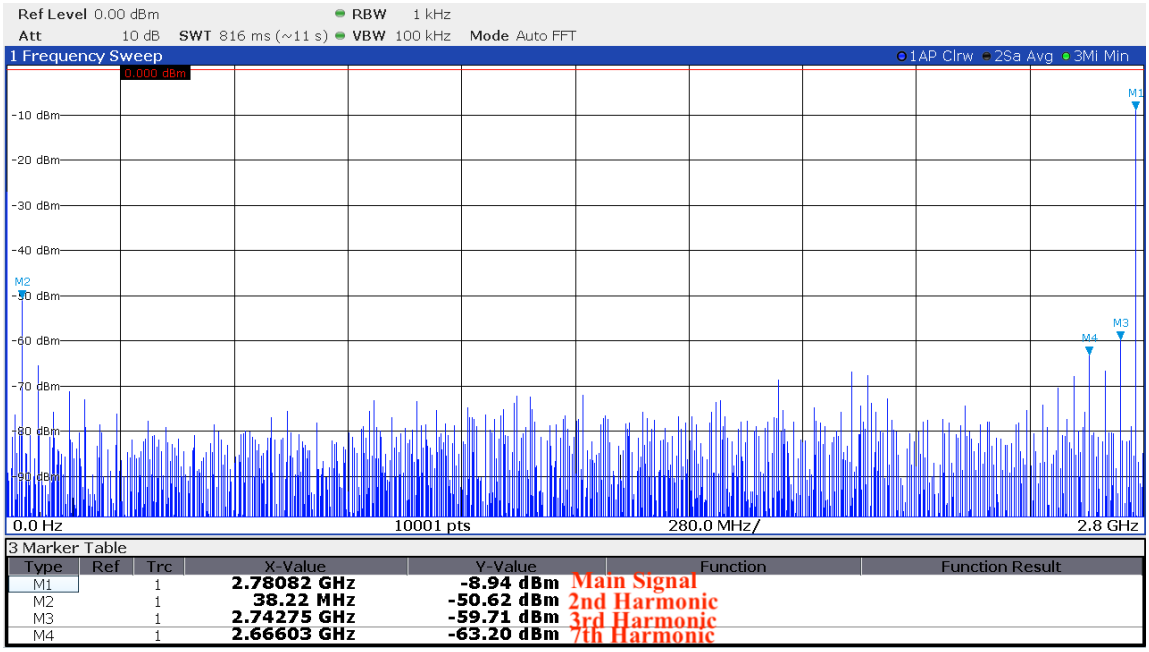


(b) Differential output signal measurement.

Figure 5.22: The spectrum analysis of the TX-DAC operating at 5.6 GS/s inputting a low-frequency single-tone sinusoidal signal (a) while only a single ended output is connected to the spectrum analyzer and (b) the differential output connected through a differential to single ended balun to the spectrum analyzer.



(a) Single ended output signal measurement.



(b) Differential output signal measurement.

Figure 5.23: The spectrum analysis of the TX-DAC operating at 5.6 GS/s inputting a high-frequency single-tone sinusoidal signal (a) while only a single ended output is connected to the spectrum analyzer and (b) the differential output connected through a differential to single ended balun to the spectrum analyzer.

5.5 1000Base-T1 and NGAUTO Compliance Tests

To verify the functionality of the transmitter, a set of compliance tests, introduced in Sec. 2 are carried out and measurement results are presented.

5.5.1 Eye Diagram

The eye diagram is a feature of the oscilloscope generated by overlaying sweeps of the different segments of a long data stream triggered by a master clock. In this work, the trigger signal is retrieved from the data stream using a Phase-Locked Loop (PLL) to regenerate the clock signal. An eye diagram is a common indicator of the quality of the signal in a high-speed communication link such as Automotive Ethernet, the scope of this work here.

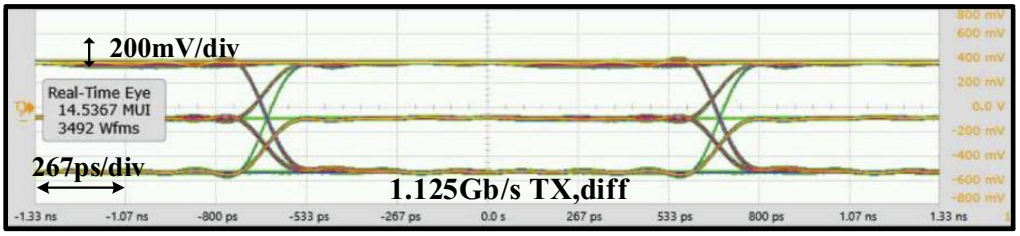


Figure 5.24: Eye diagrams showing PRBS data of PAM-3 running at 1.25 Gb/s.

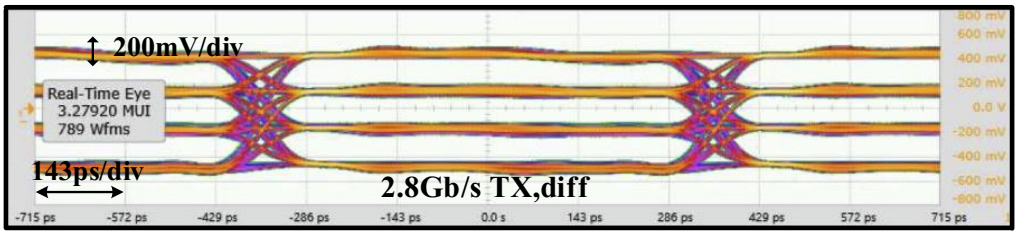


Figure 5.25: Eye diagrams showing PRBS data PAM-4 operating at 2.8 Gb/s.

The results of the eye diagram measurements show the required differential peak-peak output voltage of 1 V with sufficient eye-opening to identify the PAM modulated data up to the data rate of 11.2 Gb/s. The measured eye diagrams correlate well with the simulated results.

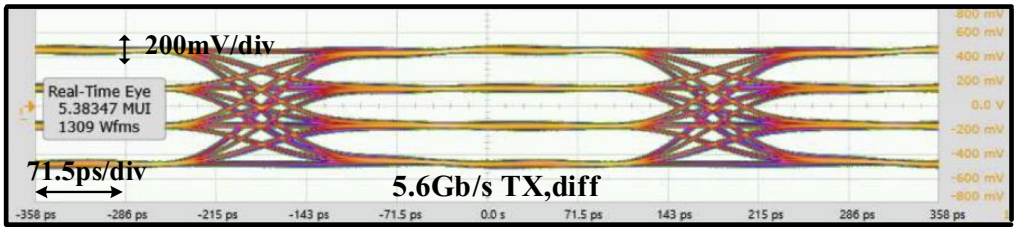


Figure 5.26: Eye diagrams showing PRBS data PAM-4 operating at 5.6 Gb/s.

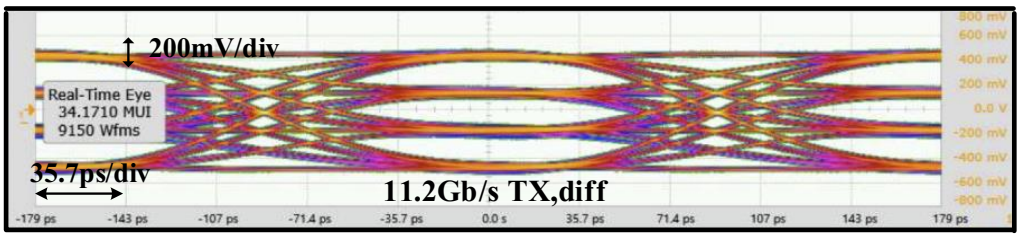


Figure 5.27: Eye diagrams showing PRBS data PAM-4 operating at 11.2 Gb/s.

Measurements

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
Eye width(1-3)	1.25833 ns	866.558 ps	0.0 s	1.27292 ns	1.27292 ns	583.640 ps	366
V p-p(1-3)	934 mV	933.0 mV	927 mV	934 mV	8 mV	1.6 mV	366
DutCyc dist(1-3)	Edge?	----------	----------	----------	----------	----------	0
Crossing %(1-3)	54.8%	52.7%	42.3%	58.0%	15.7%	3.84%	366
Q-factor(1-3)	1.63	1.649	1.63	1.69	60 m	22 m	366
Eye jit p-p(1-3)	10.09 ps	6.038 ps	0.0 s	28.96 ps	28.96 ps	8.927 ps	366

Figure 5.28: Eye diagram measurement results of the PRBS data of PAM-3 running at 1.25 Gb/s shown in Fig. 5.24.

Measurements

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
Eye width(1-3)	647.05 ps	648.902 ps	647.05 ps	658.23 ps	11.18 ps	1.965 ps	29
V p-p(1-3)	1.027 V	1.0248 V	997 mV	1.027 V	30 mV	5.7 mV	29
DutCyc dist(1-3)	4%	4.0%	4%	4%	1%	0.1%	29
Crossing %(1-3)	47.8%	44.3%	37.5%	70.5%	33.0%	6.08%	29
Q-factor(1-3)	1.95	1.740	1.53	2.15	620 m	182 m	29
Eye jit p-p(1-3)	105.80 ps	105.283 ps	102.29 ps	105.87 ps	3.58 ps	631 fs	29

Figure 5.29: Eye diagram measurement results of the PRBS data of PAM-4 running at 2.8 Gb/s shown in Fig. 5.25.

Measurements

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
1 Eye width(1-3)	259.83 ps	260.646 ps	259.83 ps	263.18 ps	3.35 ps	749 fs	227
2 V p-p(1-3)	1.00640 V	1.00594 V	999.88 mV	1.01478 V	14.90 mV	1.8465 mV	4597
3 DutCyc dist(1-3)	3%	2.6%	3%	3%	0%	0.0%	227
4 Crossing %(1-3)	49.0%	48.8%	26.4%	75.2%	48.7%	4.90%	227
5 Q-factor(1-3)	1.97	1.969	1.63	2.25	620 m	47 m	227
6 Eye jit p-p(1-3)	24.85 ps	24.849 ps	23.67 ps	25.28 ps	1.61 ps	151 fs	227

Figure 5.30: Eye diagram measurement results of the PRBS data of PAM-4 running at 5.6 Gb/s shown in Fig. 5.26.

Measurements

Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
6 Eye width(1-3)	121.46 ps	121.642 ps	121.46 ps	127.06 ps	5.60 ps	556 fs	247
1 V p-p(1-3)	1.034 V	1.0339 V	1.006 V	1.034 V	28 mV	2.2 mV	247
2 DutCyc dist(1-3)	6%	5.5%	5%	6%	1%	0.2%	247
4 Crossing %(1-3)	49.0%	33.7%	26.0%	72.9%	46.9%	11.4%	247
3 Q-factor(1-3)	2.00	1.875	1.73	2.00	270 m	84 m	247
5 Eye jit p-p(1-3)	14.26 ps	14.249 ps	13.44 ps	16.08 ps	2.64 ps	431 fs	247

Figure 5.31: Eye diagram measurement results of the PRBS data of PAM-4 running at 11.2 Gb/s shown in Fig. 5.27.

5.5.2 Common Mode Measurement

The measurement setup in this case, uses a power combiner on the differential outputs and feed the single ended common mode signal to the spectrum analyzer. The measurement result for the power combination at the rate of 5.6 GBaud/s is shown in Fig. 5.32 with 32 dBc attenuation of the clock feed through. Moreover, the mesurment results for 2.8 Gbaud/s and 1.4 GBaud/s are plotted in Fig. 5.33 and Fig. 5.34, respectively and shows 33 dBc and 39 dBc attenuation of the clock feed through, respectively. The measurement results shows to be very close to the simulated results with the maximum 3 dBc higher clock feed thorugh measured at the sampling rate of 5.6 GBaud/s comparing to the simulated results.

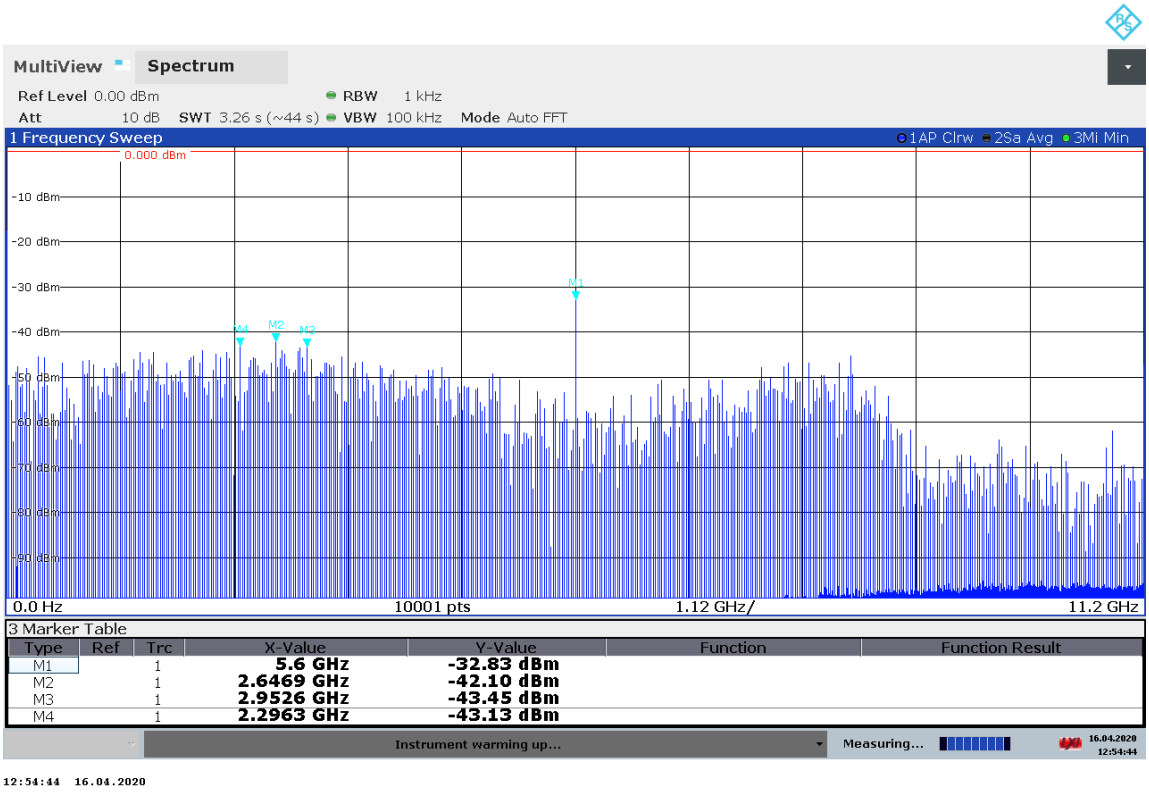


Figure 5.32: TX common-mode output signal operating at 5.6 Gbaud/s showing 32 dBc attenuation of clock feed through.

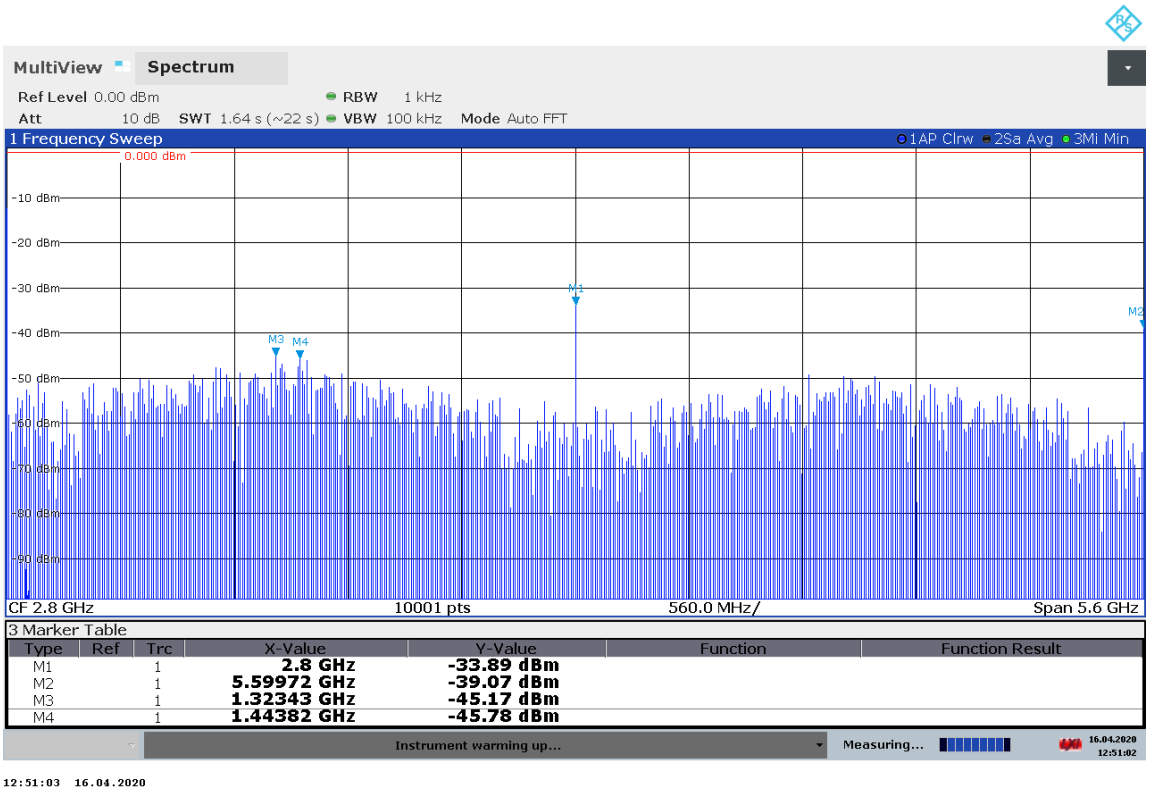


Figure 5.33: TX common-mode output signal operating at 2.8 Gbaud/s showing 33 dBc attenuation of clock feed through.

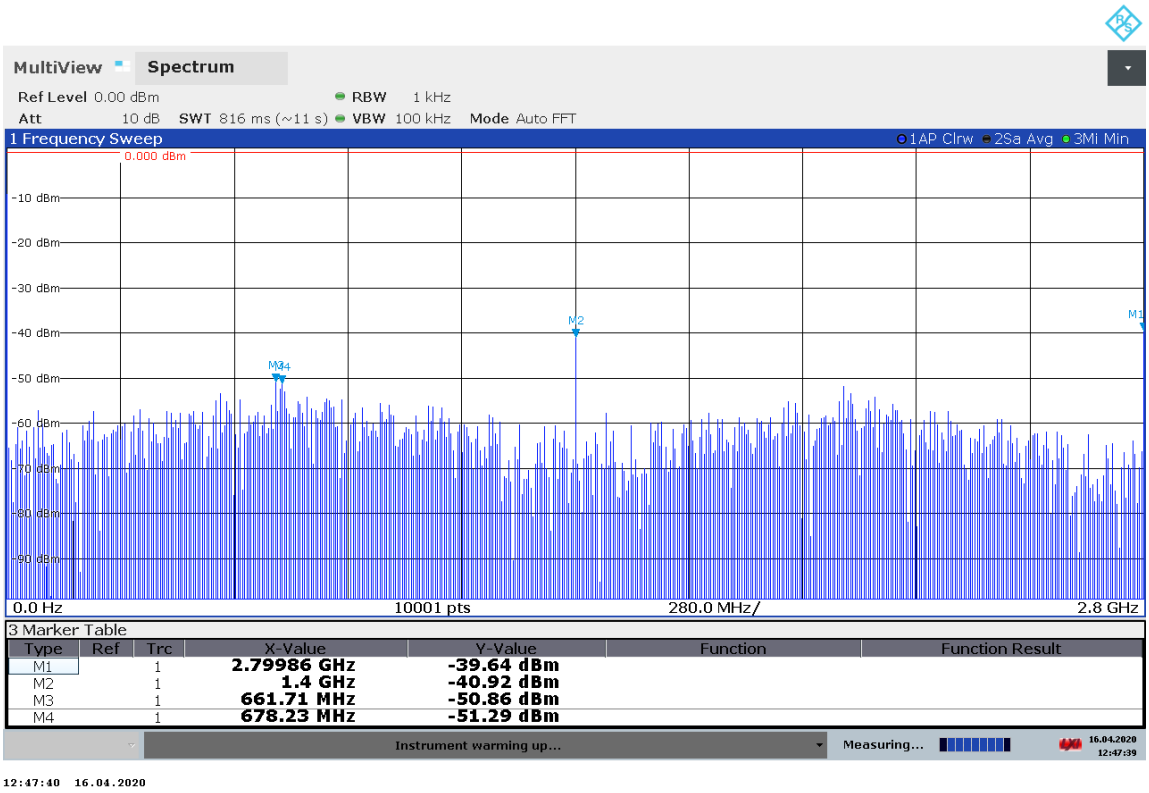


Figure 5.34: TX common-mode output signal operating at 1.4 Gbaud/s showing 39 dBc attenuation of clock feed through.

5.5.3 Transmitter Output PSD

As mentioned in Sec. 2.3.4, the power spectrum density of the TX output should be within certain limits set by the Automotive Ethernet standards. Therefore, to test the chip, the outputs of the TX-DAC is connected through a differential to single-ended 50 Ω terminated balun to a spectrum analyzer. A PRBS waveform is loaded to the TX-DAC and the PSD of the output is plotted in Fig. 5.35, Fig. 5.36 and Fig. 5.37 with the PSD limit lines defined by the Automotive Ethernet standards with different data rates.

Figure 5.35: The power spectral density analysis of the PRBS data of PAM-4 running at 11.2 Gb/s and the IEEE Automotive Ethernet limit lines plotted on the graph as well.

Figure 5.36: The power spectral density analysis of the PRBS data of PAM-4 running at 5.6 Gb/s and the IEEE Automotive Ethernet limit lines plotted on the graph as well.

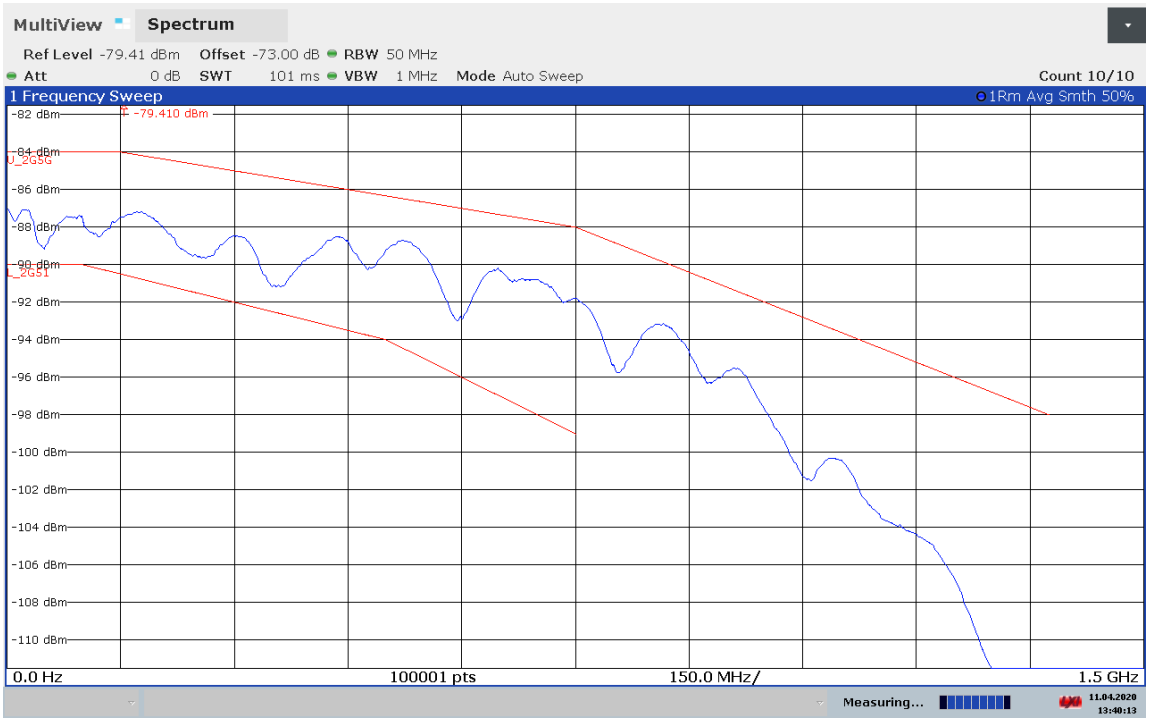


Figure 5.37: The power spectral density analysis of the PRBS data of PAM-4 running at 2.8 Gb/s and the IEEE Automotive Ethernet limit lines plotted on the graph as well.

5.5.4 Return Loss

To measure the return loss of the DAC driver, the S22 of the DAC differential outputs is measured via a vector analyzer. The limit line for the return loss at the MDI is shown in Sec. 2.3.4.

Since MDI implementation is not in the scope of this work, the return loss of the DAC driver is measured and verified to be within the defined limit lines. However, the outputs of the DAC driver are connected to the vector analyzer through the bond wires within the QFN package. Therefore, the frequency effect of these components should also be considered in the modeling of these parasitics and de-embedded from the measurement results.

The dominant parasitic components modeled here is the bond wire inductance of the QFN package $L_{\text{bondwire}} = 2.5\,\text{nH}$ as shown in Fig. 5.38 as well as the S22 measured up to 4 GHz directly at the TX-DAC outputs on the PCB. The default setup of the Zcal=4, meaning 4 half unary cells in parallel to the outputs shows DC impedance of 50.1 Ω measured at 10 MHz. The DC impedance of other setups measured at 10 MHz from Zcal=0 to Zcal=8 are plotted in Fig. 5.39. As mentioned in Sec. 4.4 Zcal=0 means no parallel branch is connected in parallel to the outputs and Zcal=8 means 8 parallel branches with a weight of half unary cell each are connected to the outputs. The DC impedance variation with the changing of the number of parallel branches enabled shows to cover the whole range of PVT variation shown in Fig. 4.4 with the calibration resolution of 1.5 Ω.

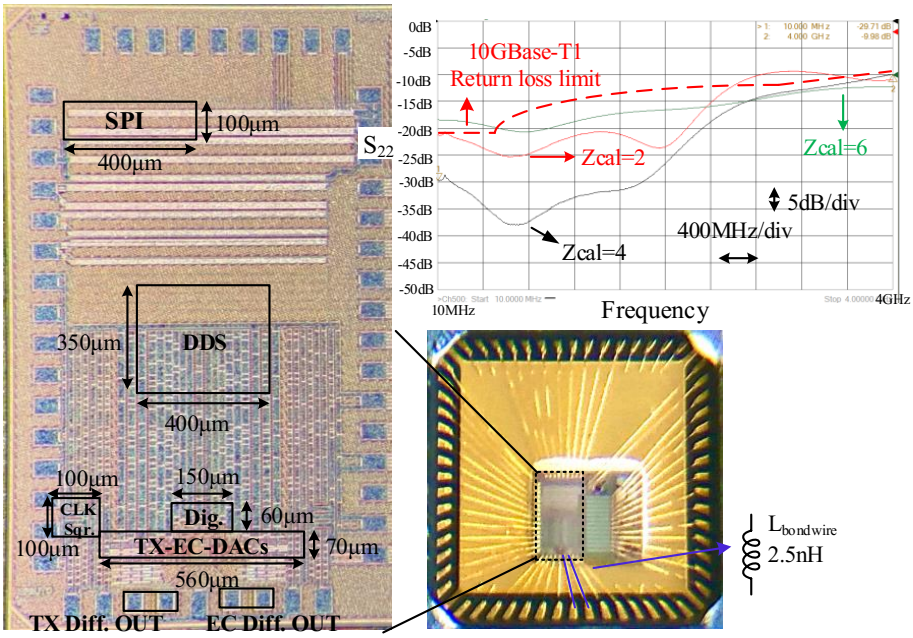


Figure 5.38: Measured S22 directly at the TX-DAC packaged output measured up to 4 GHz with a default Zcal=4, complying to 10GBase-T1 return loss limit line with DC impedance of 50.1 Ω measured at 10 MHz.

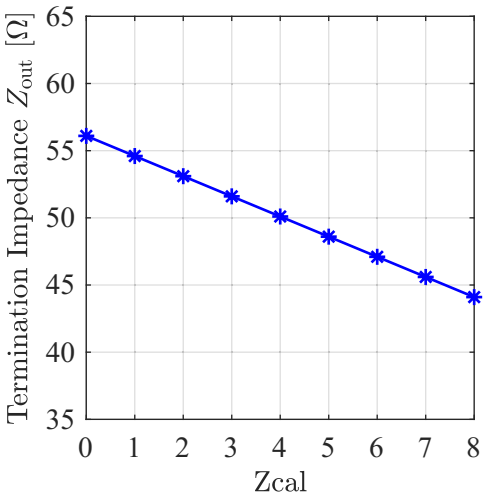


Figure 5.39: Measured DC impedance at 10 MHz directly at the TX-DAC outputs on the PCB driven from the S22 measurements for all 9 calibration setup for the termination impedance.

5.6 TX Performance Comparison

The 9-bit TX-EC-DAC combination dissipates 42mW and 3mW from a 1.2V and 0.8V power supply, respectively. Table. 5.40 summarizes the results of this design in comparison with previous works using SST DACs and drivers at similar operating speed. The proposed DAC driver and echo canceler show despite the DAC complexity, the best power efficiency of 2 mW/Gb/s, the highest resolution of 2 mV, and smallest form factor per DAC of 0.025 mm^2.

	This work	[25]	[26]	[27]
Technology	22nm CMOS FDSOI	45nm CMOS SOI	65nm CMOS SOI	45nm CMOS FDSOI
DAC Architecture	SST full-rate	SST half-rate	SST full-rate	SST full-rate
Supply voltage [V]	0.8/1.2	1-1.65	1/1.8	1
Driver resolution [bits]	9	2	2	2
Nyquist Linearity (SFDR) [dBFS]	54.4	-	-	-
Equalization Resolution [mV]	2	33	N/A	125[1]
Nr. of Taps	0-5	1[2]	2	4
PAM level	PAM4/6/8	PAM2	PAM4	PAM4
Diff. Eye Height [Vppd]	1	0.8	1	1.3
Max. Data Rate [Gb/s]	11.2	7.4	3	45
Efficiency [mW/Gb/s]	2[3]	4.32	12.43	2.6
Area [mm^2]	0.05[4]	0.18[5]	0.035	0.28
Echo Cancellation [dB]	24.4 up to 5.6GHz[6]	-	15 up to 1GHz[7]	-

[1] Estimated from architecture.
[2] Single-tap equalizer but a multi-tap design.
[3] 45mW/2/11.2Gb/s: 45mW for TX+EC-DAC.
[4] Area of TX+EC-DAC combination.
[5] Area estimated from picture.
[6] Measured with the scope off-chip hybrid.
[7] Measured with on-chip hybrid.

Figure 5.40: TX performance comparison with other SST drivers.

6 Conclusion

In this work, a brief history of automotive networking technologies are presented by introducing automotive Ethernet as the new networking technology to meet the higher demand for data throughput within in-vehicle communication. The automotive Ethernet standards from a data rate of 100 Mb/s to 10 Gb/s are introduced with the selected required tests for the PHY implementation, focusing on the functionality of the transmitter.

Next, two high-speed DACs suitable to use as the transmitter, directly driving the channel, are introduced and compared. SST DACs showed to be the optimum solution in terms of power consumption and silicon area but with several challenges. These challenges, such as the termination switch non-linearity, packaging impedance effects, PVT effect on the outputs termination impedance, are discussed in detail and possible solutions are presented. Furthermore, the full-duplex operation mode results in the problem of having the TX power on the receive path, and a solution to have an extra identical DAC named echo canceling DAC is presented to directly subtract the TX power through a hybrid at the receiver. In the following chapter, the fourth chapter, the detailed design and implementation of the proposed 9-bit dual supply 0.8 V/1.2 V SST TX-DAC and EC-DAC, providing differential 1 Vppd PAM4 output swing is presented.

The proposed DACs with taking advantage of a power-supply-based degeneration techniques and adopting a passive to active device termination ratio of r_{RM}=4, achieved high power efficiency of 2 mW/Gb/s, high static and dynamic linearity (SFDR DC= 60 dBc and SFDR Nyquist=50 dBc). The highly correlated EC-DAC design and layout provides more than 24.3 dB of interference cancellation.

In addition, both DACs operate beyond 11.2 Gb/s and consume a total power consumption of 42 mW and 3 mW from a 1.2 V and 0.8 V supply, respectively. The TX-DAC design and layout provide 32 dBc of common-mode attenuation of clock feed through. Considering PAM-4 signal transmission, this leads to a power efficiency for the 9-bit transmit DAC of 2 mW/Gb/s. The tests for the transmitter defined by MultiGBase-T1 are performed and the measurement results showing the compliance of the TX-DAC to PSD masks, return loss limit lines are presented.

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