DISTORTION in MICROWAVE CLASS-S POWER AMPLIFIERS

vorgelegt von
M. Sc. Eng.
Dhamia AL-Mozani
geb. in Bagdad

Von der Fakultät IV - Elektrotechnik und Informatik
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Promotionsausschuss:

Vorsitzender: Prof. Dr.- Ing. Friedel Gerfers
Gutachter 1: Prof. Dr. -Ing. Wolfgang Heinrich
Gutachter 2: Prof. Dr. -Ing. Matthias Rudolph
Gutachter 3: Prof. Dr.- Ing. Manfred Berroth

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To my husband Ali and my children Lillian and Elia

without whom this work would have been completed two years earlier

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Abstract

To tackle the critical challenge in microwave transmitters of achieving high efficiency at higher power back-offs, class-S power amplifier, as promising class of operation, attracts the attention since some time ago. It provides a theoretical efficiency of 100% regardless of power back-off which is required nowadays in wireless communication infrastructure. The current work focused on the class-S amplifiers of the voltage mode topology (VMCS) within the 900 MHz band. The research was first directed to the impact of the output network optimization on the overall performance of class-S PA. Two output networks have been designed and realized: the first with lumped elements (capacitors and inductors) and the second with bond-wires and capacitors. The results showed that improved higher harmonics suppression due to the bond-wire realization could enhance the drain efficiency of class-S to a certain level while maintaining the same output power. The main research work deals with the linearity of class-S PA. An analysis of the static distortion, that is; static amplitude-to amplitude (AM-AM) conversion and static amplitude-to-phase conversion (AM-PM) was conducted. Load-pull measurements have been performed to help better understanding of the load optimization approach on the linearity in general. Bandpass Delta Sigma Modulated (BPDSM) signal and Pulse Width Modulated (PWM) signal have been used as driving signals of the amplifier for different signal back-offs. The results prove particularly that AM-AM/ AM-PM conversion increases as signal amplitude decreases (contrary to linear PAs) or as the pulses become shorter in time. In this way the presented work contributes a basic aspect to the understanding of class-S PAs.

Zusammenfassung

Im Zuge der Entwicklung von Mikrowellen-Leistungsverstärkern, die auch bei mittleren Leistungen deutlich unterhalb des Maximalwerts einen hohen Wirkungsgrad liefern, sind Klasse-S-Verstärker seit einiger Zeit in den Blickpunkt des Interesses gerückt. Sie ermöglichen einen theoretischen Wirkungsgrad von 100 % unabhängig vom Leistungsniveau, was für die heutige und künftige Mobilfunkinfrastruktur sehr interessant ist. Die vorliegende Arbeit konzentriert sich auf Klasse-S-Verstärker mit Voltage-Mode-Topologie (VMCS) innerhalb des 900-MHz-Bandes. Zuerst wurde der Einfluss der Ausgangsnetzwerkoptimierung auf die Gesamtleistungsverstärkung des Klasse-S-Leistungsverstärkers untersucht. Zwei verschiedene Ausgangsnetzwerke wurden hergestellt und verglichen, eines mit konzentrierten Bauelementen (Kondensatoren und Spulen) und eines mit Bonddrähten und Kondensatoren. Es zeigte sich, das die Bonddraht-Version durch die verbesserte Oberwellenunterdrückung den Drain-Wirkungsgrad bis zu einem gewissen Grad verbessern kann, wobei dieselbe Ausgangsleistung erhalten bleibt. Den Hauptuntersuchungsgegenstand bildet die Linearität des Klasse-S-Leistungsverstärkers. Dabei wurden die statischen Verzerrungen, d. h. die statische AM-AM- und AM-PM-Konversion untersucht. Load-Pull-Messungen dienten dazu, die Wirkung der Lastoptimierung auf die Linearität im allgemeinen zu verstehen. Als Eingangssignale für den Verstärker wurden Bandpass-delta-sigma- (BPDSM) und pulsweitenmodulierte (PWM) Signale verschiedener Leistungsstufen benutzt. Die Ergebnisse zeigten insbesondere, dass die AM-AM- und AM-PM-Konversions-Werte ansteigen, wenn die Signalamplitude sinkt (im Gegen-

satz zu linearen Leistungsverstärkern) oder wenn die Pulse zeitlich kürzer werden. Somit liefert die vorgelegte Arbeit einen grundlegenden Beitrag zum Verständnis der Klasse-S-Leistungsverstärker im Mikrowellenbereich.

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Chapter 1

Introduction

The wireless communication technology revolutionizes the way the people living and communicate. In recent, a huge growth in wireless communication subscribers has been recorded. Cisco reported that by the end of 2019, the number of mobile users will reach 5.2 billion up from 4.3 billion in 2014. And by the year 2019, there will be nearly 1.5 mobile devices per capita (11 billion mobile-connected devices). The new services that have been appeared like music downloads and access to the Internet via cell phones involve progressively data transmission rates over wireless communication infrastructure. Cisco (in its Visual Networking Index (VNI) that released in February 2014) reported that by 2019, the average traffic per mobile-connected user device will be 2.8 GB/month compared to 359 MB/month in 2014 [1].

Meanwhile, the frequency spectrum designated for wireless communication is constant. Therefore, and with the increasing number of wireless users and the intense traffic, it becomes more and more crowded as many subscribers use the wireless communication system via their wireless device. Fig. 1.1 exhibits the user subscriptions per 100 inhabitants for the years 2001 till 2014.

In the year 2001, the fixed telephone and the mobile-cellular subscriptions were 16% both. After that, the cellular services dominate and reach the highest level

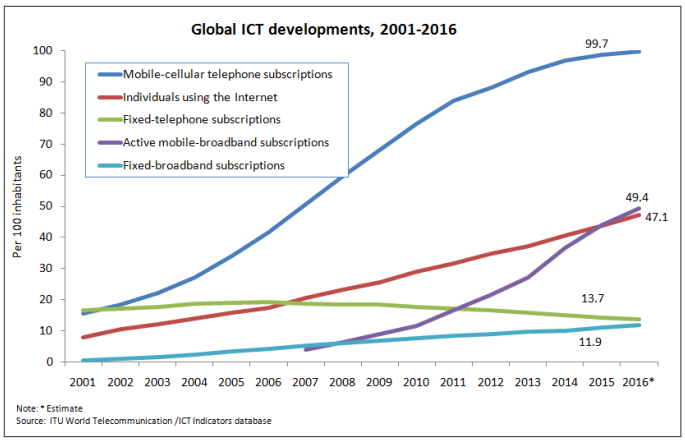

Fig. 1.1: Global communication subscription for different services [2]

(99.7%) of subscription compared to the other services. One can notice that the fixed telephone services show no progress since 15 years! The internet contribution jumps to be 47.1% in 2016 where it was only 8% in 2001. In 2007 and when the smart phones came to invade our lives, the access to the internet via them increased from only 4% in the year 2007 to 49.4% in 2016. Whereas, the fixed broadband contribution (cable modem, DSL, fibre-to-the-home/building, and other fixed services) shows an increment as well (from 0.6% in 2001 to 12% in 2016), but at much lower values than the mobile access.

To cope with the revolutionary increase in the wireless services demands and to use the wireless spectrum efficiently, communication standards have been developed and improved over the years of wireless evolution. The wireless communication networks standards like TDMA, CDMA, WiMAX and LTE, see Fig. 1.2, were introduced to enhance the spectral efficiency [3].

Each standard belongs to a certain generation in the evolution of the services and technologies. Since the '80 last century (1 G) until today (4 G and beyond), the wireless industry witnessed a phenomenal growth, both in terms of mobile technology and its subscribers, refer to Fig. 1.1 and Fig. 1.2. There have been services, instead of stand-alone systems, like telephony, internet, television, radio

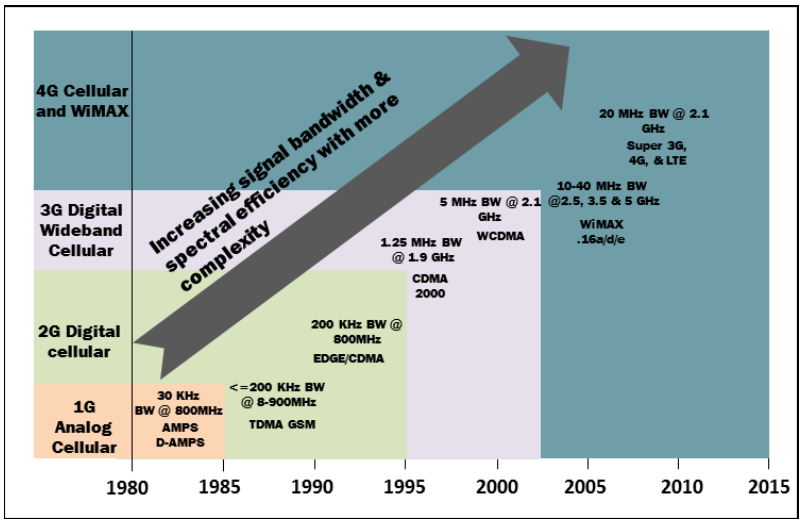

Fig. 1.2: Evolution of wireless communication standards [3]

broadcast, and emails, users can access through one single mobile device.

This consistently growing demand for higher data bit-rates accompanied with severe spectral mask requirements with the needs of low power consumption put a heavy burden to the field of Power Amplifier (PA) design. One of the most energy hungry components of a base station is the power amplifier unit.

In general, base stations vary in shape and size, Fig. 1.3 exhibits a multi-standard base station of Airbus Defense and Space, but they share the main seven subsystems: antennas and feed cables, the PA unit, RF transceiver, processing unit, backhaul, cooling system and the AC-DC power supply. This structure can be varied according to the base station type: Macro, Micro, or Pico base station.

In some cases the PA and their cooling occupy half the base station volume. The PA and RF/ microwave transceiver account for nearly to 60% of the total power consumption in the base station [4]. Therefore special consideration should be made when designing the RF PAs.

The PA determines the limits of the transmission capability of the wireless system. Recently, with the appearance of the highly data rates standards, such as

Fig. 1.3: Airbus Defense and Space reveals its multi-standard Tetrapol narrowband base station (©Airbus Defense and Space 2014)

Wideband Code Division Multiple Access (WCDMA) of 3G systems, High Speed Packet Access (HSPA) of 3G too, and Long Term Evolution (LTE) of the 4G, signal envelope is not constant anymore. It has a time-varying profile that consequently results in a difference between peak and average power. PAPR is defined as the ratio between the peak modulated output power to its long- term time average:

$$PAPR = 10 \cdot log_{10} \frac{P_{max}}{P_{average}} \qquad [dB] \tag{1.1}$$

PAPR is also denoted as power back-off (BO). Different signal standards have different operation BOs. For 2G systems like GSM and GPRS, signal has normally 0dB BO, while for 2.5G systems, known as Enhanced Data Rate for Global GSM Evolution (EDGE), BO equals 3.2 dB, where it reaches 3.5 dB-9 dB,6.5 dB-10 dB, and 8.5 dB-13 dB for 3G (WCDMA), 3.5G (HSPA), and 4G (LTE/ LTE-A) systems, respectively.

Linear power amplifiers are not able to achieve high back-off power without a significant degradation of drain/ power added efficiency. Drain/ collector efficiency can be described as the ratio of RF/ microwave output power P_{out} to the input direct current (DC) power of the drain/ collector node P_{DC}:

$$\eta_D = \frac{P_{out}}{P_{DC}} \qquad [\%] \tag{1.2}$$

Drain efficiency in some cases does not give a comprehensive understanding of the overall performance of the amplifier since it neglects the incident RF/ microwave input power. Equation 1.3 gives a definition of PAE and clarifies the relation between PAE, η_D, and Gain (G). It could be clearly concluded that in single stage PAs, PAE is an important figure of merit since the gain in those circuit is low.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \cdot \ 100 \ = \eta_D \cdot \ (1 - \frac{1}{G}) \cdot \ 100 \qquad [\%] \tag{1.3}$$

As the signal is backed-off, drain/ collector efficiency and power added efficiency drop rapidly. This happens because efficiency of PA normally maximizes at saturated output power and decreases as the input power is reduced or backed-off.

Modern wireless base stations usually include class-AB or Doherty PAs which are conventional PAs, i.e. linear PAs. The overall efficiency for class AB amplifier's final stage, for example, lies between 50% and 78% at full load and it decreases when light load is used. However, as PAPR increases, a small amount of the DC

consumption is converted to heat since efficiency is at its maximum level when saturated power is reached and drops when the input power backed-off. Meanwhile, high distortion may exist if the PA is injected with high power levels of PAPR. The PA is aimed to maintain high linearity at back-off case or at least has an appropriate level of distortion based on the desired applicable specification. There is a tradeoff between efficiency of PA and its linearity. During the linear operation of PA, see the blue line in Fig. 1.4, increasing input power by 10% results in 10% more output power. In real PA of modern base stations, this is not the case. Increasing input power, to a certain level, will make a deviation of the ideal response of the PA. That occurs near the saturation point of the PA where efficiency is high and power is saturated.

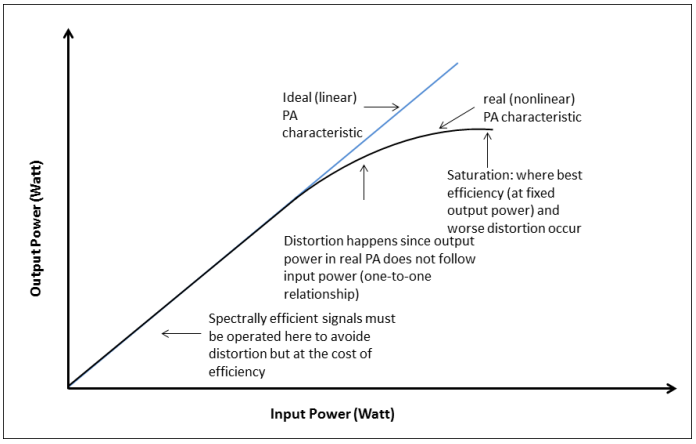

Fig. 1.4: Power amplifier input and output power characteristics

Traditional PAs do not maintain efficient behavior and react linearly with high average output power region, therefore new advanced concepts of PA class of operation was at the high spot since some time. Doherty, envelope tracking, and lately class-S have attracted more and more attention academically and industrially, with Doherty clearly dominating the present base-station deployments.

To have an insight of the challenges the Information and Communication Technology (ICT) developments face, it would be wise to have an eye on some facts and numbers of energy consumption and its consequences on our world. Since the

introduction of cellular networks, in late 1970s, most the attention was focused on spectral efficiency and maintaining Quality of Service (QoS). Plus, the cost for communication services has been increased since the appearance of smart phones and tablets which usually provide services of high data rates exchange in which more energy consumption is needed. This matters both planet and wallet, therefore the new research concept was emerged that is called green IT. The term "green" is a synonym of the endeavors to minimize the emission of CO_2, but in ICT (Information Communication Technology), "green ICT" involves the increasing efforts by researchers to reduce the operating cost and save energy.

ICT is assumed to contribute a bout 2% of global carbon dioxide emission and to account for around 10% of global electricity consumption. Carbon dioxide emission of ICT is roughly equal to the emission comes from aviation industry and one fourth of that of cars globally. The rate of emission is increasing over years, it is estimated to double to 4% by the year 2020 [5].

Different paths are there to achieve green ICT. One way is by using renewable energy, turning off some components in the BS selectively during non-peak traffic hour, *sleep mode*, or improving the hardware part of BSs, in particular, PAs. More than 80% of the PA input power is converted to heat and the useful power is only about 5% to 20% of the input power [7]. Cost will increase if efficient power components are used in BSs and will be even more in large coverage areas or when higher power efficiency is needed. For instance, a PA unit for small cell of WCDMA or LTE BSs, which covers around 2 km, costs nearly to $75 [6].

New techniques were introduced to cope with the challenges mentioned earlier. Power efficiency draws the attraction of most manufactures and research institutes to increase the battery life time of cell phones and the power consumption of base stations, for both ecological and economical reasons.

At the *Ferdinand-Braun-Institut für Höchstfrequenztechnik (FBH)*, the activities have been on the Class-S Power Amplifier (CSPA). In principle, class-S is a switch-

ing PA, just like other switching amplifiers (class-E, class F, class-D etc), that depends on the idea of using the transistor as a switch. That is, the transistor switches between two states: On-state and OFF-state. Switch Mode Power Amplifiers SMPAs have very high efficiency which theoretically can reach 100% [8].

Class-S is very close to class-D, instead of an analogue input drive in the case of class-D, class-S has a fully binary or digital input signal and thus requires broadband behavior of the PA. The input signal can be Pulse Width Modulated (PWM), band-pass Delta-Sigma Modulated (DSM), or using other pulse modulation schemes discretized in amplitude. The final stage of a Class-S PA can be designed based on voltage or current switching (VMCS or CMCS).

According to the class-S scheme, the wanted analog input signal is encoded into a binary pulse sequence using a certain modulator. This binary pulse train then feeds the power-switching final-stage amplifiers, which in turn amplify it to the proper power level. In the ideal case, in the power stages no overlapping occurs between current and voltage waveforms and hence no power loss exists, which leads to a 100% efficiency independently of the power back-off. A band-pass resonator is required at the output network to pick the required signal frequency suppressing the out-of-band spectrum and thus restoring the wanted analog signal.

Since broadband operation is required, Monolithic Microwave Integrated Circuit (MMIC) is advantageous. Different technologies have been presented so far. In this work, class-S is realized using Gallium Nitride (GaN) High-Electron-Mobility Transistor (HEMT) due to its combination of high breakdown voltage and high speed [9, 10].

Therefore, a voltage mode class-S PA is designed in the 900MHz band and analyzed with different output networks. The MMIC used for realization the complete module of class-S PA was developed outside the frame of this thesis and was already reported in [11]. Two output network approaches are followed. The first network is designed with conventional lumped elements, inductors and capaci-

tors, while the second network is designed using bond-wires (BWs) instead of the inductors in the first version. Load-pull investigations of class-S PA as well as measurements are accomplished as a takeoff point for nonlinearity analysis.

In chapter 2, the theory of class-S PA is presented as an excellent counterpart for conventional linear PAs. Modes of operation are also mentioned to have a clear view of the possible switching mechanism class-S can handle. Properties and nature of driving input signals, like Band-Pass Delta-Sigma (BPDS) modulated signal and PWM signal will be discussed too in the same chapter. Output network functionality and the need for new art of filtering is also clarified in details.

The design of both output networks, simulation, modelling of the BWs one, and realization as a stand alone filter is discussed in chapter 3. The complete class- S hybrid module's design and measurements are part of the same chapter too.

As for any other PA, a linearity investigation is important to evaluate the performance of the device and to set the best conditions the Device Under Test (DUT) is to be operated. Following the classical design approach, load-pull measurements were performed and analyzed, as described in chapter 4. This forms the basis for the most important topic presented in this thesis, which is the analysis of distortions in the class-S PA in Chapter 5. Amplitude and phase distortion (AM-AM and AM-PM) are used to describe the linearity of the VMCS module. Simulation results serve as a tool to understand the basic effects and to study the influence of circuit elements. The AM-AM/AM-PM for the best pair of circuit parameters are measured using spectrum analyzer (AM-AM) and an oscilloscope (AM-PM). To conclude the overall work, chapter 6 explains and summarizes the most substantial points and recommends for further future improvements.

Chapter 2

Understanding the Class-S PA Concept

2.1 Linear and Switch Power Amplification

To best figure out the switch mode operating mechanism, it is preferable to compare it with conventional power amplifiers like class-A, class-B, or class-AB. In those amplifiers, the transistor is biased to a certain operating point and moves along the designated loadline as in Fig.2.1 (blue line). Dissipated losses are introduced as a result. In switch mode power amplifiers, the transistor works in the saturation/ pinch-off regions. That is, at the very ends of the I-V characteristic curve. In ideal case, the transistor, here it functions as a switch, passes either current or voltage at a time. In this case, no overlapping in time occurs between voltage and current. Therefore, losses are zero and efficiency is 100%. But, there is always an overlapping between voltage and current (red line in Fig.2.1) and hence the 100% efficiency can not be obtained. In Fig. 2.1, one can see the well-known power amplifier characteristics (drain-source current (I_{DS}) vs. drain-source voltage (V_{DS})).

The transistor can be replaced by ideal switch to understand the mechanism of switching in class-S power amplifier. When the switch is OFF, only voltage is provided at the output and when it is ON, only current passes through. Fig. 2.2illus-

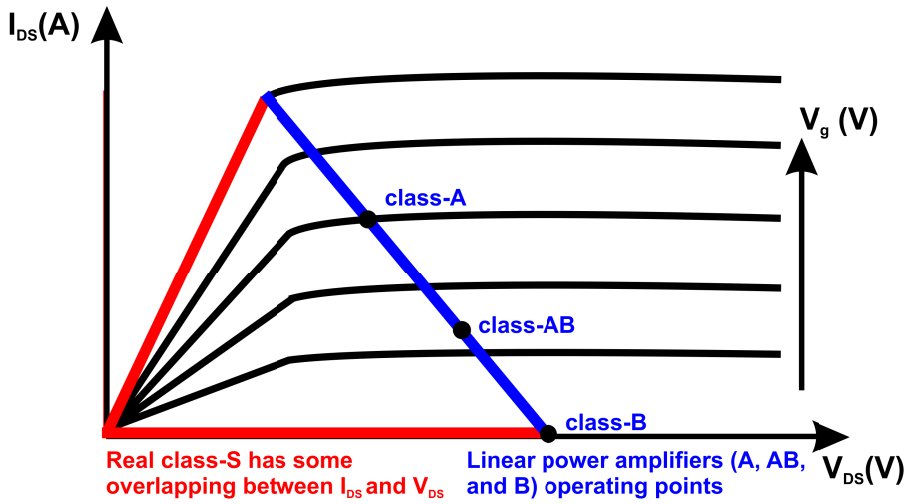

Fig. 2.1: Loadline and operation points of linear power amplifiers , A, AB, and B (pointed at the blue line) and switch mode power amplifiers (red line)

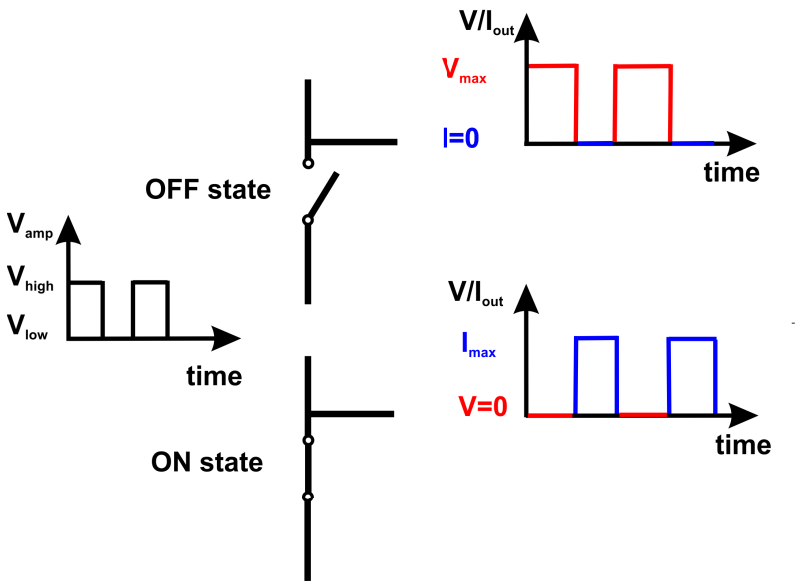

Fig. 2.2: Ideal switch functionality as an approximation of switch mode power amplifier voltage and current in ON/OFF states

trates this main principle and shows what happens when the switch (transistor)

closes or opens.

The resonator (Band Pass Filter (BPF)) helps to reconstruct the original sinusoidal shape signal out of the broadband spectrum and provides good blocking for harmonics from reaching the load. Hence, only fundamental current and voltage are generated at the load.

In reality, as we know, there is no perfection or ideality! The transistor has some losses as the switch does. Those losses come mainly from the imperfect-switch functionality of the transistor which includes the ON-Resistor when the transistor closes (R_{ON}), the finite transition time (non-zero) of the imperfect switch (slower switching amplifier), parasitic capacitance (C_{DS}) at the output when the transistor switched OFF (discharging), and of course the losses arise from the PA complete module like driver losses and filter losses. Hence, any efforts to improve class-S efficiency should be directed in the path of minimizing loss sources mentioned already.

2.2 Class-S Power Amplifier as a Complete System

According to the class-S scheme, refer to Fig. 2.3, the main parts in class-S system are:

- Digital modulator (BP-DSM, PWM)
- Driver and power amplification unit (normally MMIC)
- Output network (BPF)

The analog input signal is converted into a two-state binary pulse sequence using a certain modulator like Band-Pass Delta-Sigma modulator (BP-DSM) [12] or Pulse Width Modulator (PWM) [13]. The modulator oversamples the signal frequency so that the sampling rate (f_{sample}) is equal (PWM) or may become multiples of the signal frequency (f_0).

The fully digital pulse train then feeds the power-switching final stage amplifiers, which in turn amplify it to the proper power level. The power amplifier final-stage could be realized to switch either current (Current Mode Class-S CMCS) or voltage (Voltage Mode Class-S VMCS). A band-pass resonator is required at the output network to filter out the required signal frequency and thus to restore the analog input signal. In the ideal case ,when R_{ON} and C_{DS} are Zero, high power switches exist, and no dissipated losses in PA stages or output network are produced, then no overlapping occurs between current and voltage waveforms and hence no power loss exists. This leads to a 100% efficiency, independently of the power back-off.

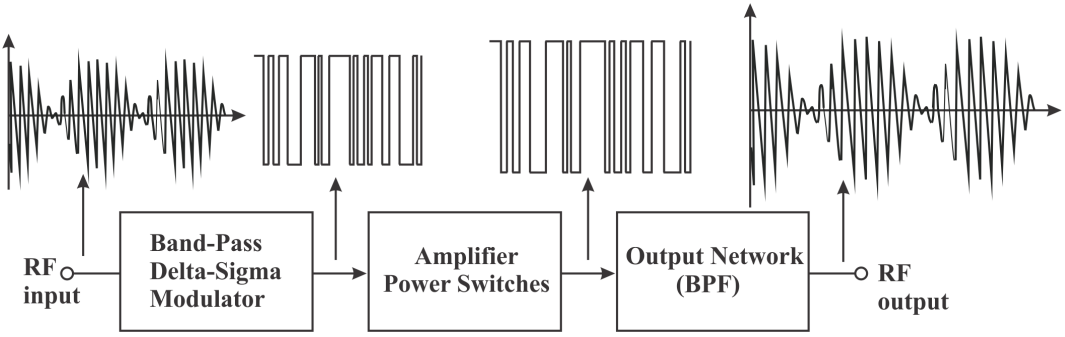

Fig. 2.3: The class-S system architecture

Despite this promising performance, class-S amplifiers in the microwave range have not been intensively explored so far. Constraints are introduced due to the fact that the class-S concept needs high speed, high-power and broadband transistors to fulfill efficient switching conditions. GaN-HEMT technology is promising in this concern since it offers high breakdown voltage and high speed as well [10, 9], but its potential for class-S has still to be fully clarified.

2.2.1 Digital Modulator

To prepare the analog signal to drive class-S power amplifier, it should be converted to a two-states digital form. The process of conversion is primarily accomplished using certain digital modulator. In this work, two types of signals have

been used as an input to drive class-S power amplifier, a band-pass delta-sigma-$\Delta\Sigma$ (BPDS) signal and PWM signals. An introduction for each signal will be introduced.

2.2.1.1 Band-Pass Delta-Sigma Modulated (BP-DSM) Signal

It is well-known that the channel capacity (C), in which a certain signal with certain bandwidth (B) is transmitted through, is equal to the binary logarithm of the signal (S)-to-noise (N) ratio (SNR) plus one, multiplied by signal bandwidth f_b:

$$C = B \cdot log_2(1 + \frac{S}{N}) = f_{\mathrm{b}} \cdot log_2(1 + SNR) \qquad [bits/sec] \tag{2.1}$$

On the other hand, Nyquist rate ($f_{Nyquist}$) assumes that the number of samples per time unit that could be transmitted is limited to twice the signal bandwidth (f_b)

$$f_{\mathrm{Nyquist}} = 2 \cdot f_{\mathrm{b}} \qquad [samples/sec] \tag{2.2}$$

In Digital Signal Processing (DSP), digitizing a sampled signal with constant amplitude (quantization) and force it to have the closest quantization value, leads to some quantization errors known as quantization noise. Here, the best justification to explore the DSP errors is the so called *SNR*. *SNR* is simply the ratio between the power of the wanted P_s signal to the power of the noise P_e in decibels:

$$SNR = 10 \cdot log_{10}(\frac{P_{\mathrm{s}}}{P_{\mathrm{e}}}) \qquad [dB] \tag{2.3}$$

To reduce the spectral density of the quantization noise, so that the noise within the required signal bandwidth (f_b)) is minimized (less noise floor), the signal should be oversampled far beyond Nyquist rate. This technique is known as oversampling. Keeping in mind that this process maintains the overall noise power

and the overall *SNR* (in-and-outside f_b) constant. Oversampling ratio (*OSR*) is defined as the ratio between the sampling frequency ($f_{sampling}$) and two times the signal bandwidth (f_b):

$$OSR = \frac{f_{\text{sampling}}}{2 \cdot f_{\text{b}}} >> 1 \tag{2.4}$$

Fig. 2.4 depicts that for every doubling of oversampling ratio (OSR=1,2,4, and 16), the quantization noise is reduced by 3 dB (i.e. 0.5 bits/octave) [14].

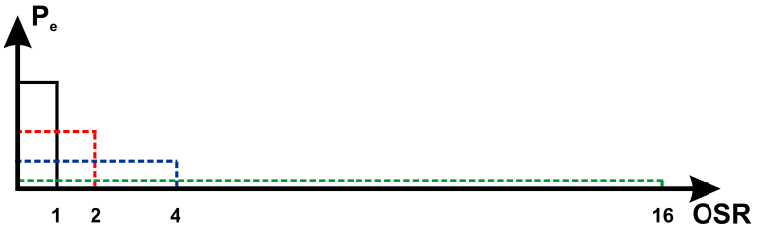

Fig. 2.4: Power spectral density of the quantizer (P_e) as a function of OSR

Oversampling is very useful when it comes to anti-aliasing filter. As the noise floor spread over larger frequency range, more relaxed-transition-band requirements is needed for anti-aliasing filter. Moreover, 0.5 bits improved resolution of DSP is obtained for each 3 dB SNR enhancement [14].

The main principle of BP-DSM is to oversample the signal. The resulting noise due to underampling is decreased by a process known as *noise shaping* which is employed by $\Delta\Sigma$ modulator . $\Delta\Sigma$ Modulator consists of a loop filter $H_1(Z)$, a 1-bit quantizer (comparator) and a feedback loop. Fig. 2.5 shows the block diagram of a 1-loop $\Delta\Sigma$ modulator [15, 16].

The quantized output signal y_n is compared with the input analog signal x_n by error minimizing feedback loop. The loop filter will pass only those frequencies, generated from the difference between the input and output signals, within the signal band (f_0) and suppresses all other frequencies. The outcome of this weighting

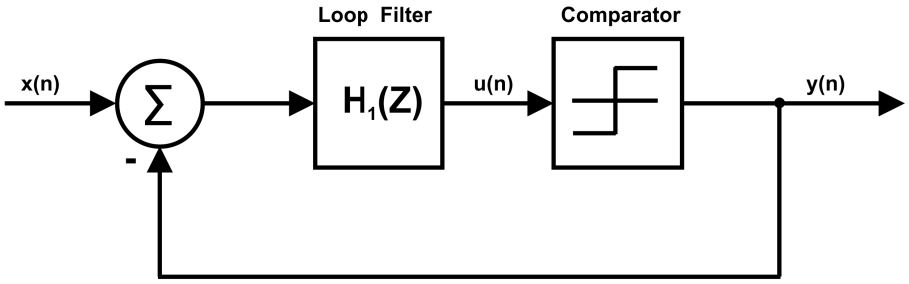

Fig. 2.5: Delta-Sigma modulator block diagram

process is then passed to the comparator which in turn generates the next output value y_n. This technique is then repeated for the next comparison value.

Noise shaping strategy produces the noise around the signal frequency in different formats depending on the type of the loop filter which is used. For low-pass $\Delta\Sigma$ modulation an integrator is required while for a band-pass modulation, a resonator is the right choice. Low-pass $\Delta\Sigma$ is used for lower frequencies near the DC region. It needs sampling rates considerably higher than the signal frequency (f_0). For switching amplifiers in the microwave region, low-pass $\Delta\Sigma$ is not suitable since the sampling frequencies would be too high. Therefore, only BPDS modulator could be used.

The output signal of a $\Delta\Sigma$ modulator is noise-shaped in a way that the noise around the signal f_0 forms a *notch* as it is shown in Fig. 2.6.

The signal can be sampled at lower sampling rate and the noise can be even better shaped if more feedback loops are used (e.g. double-loop $\Delta\Sigma$ Modulator) . This costs the designer more in the stability and complexity sides of the circuit.

2.2.1.2 Pulse Width Modulated (PWM) Signal

$\Delta\Sigma$ was considered as the favorite modulation approach, but the wideband noise around and close to f_0 limits the usable bandwidth and leads to high requirements for the reconstruction filter plus the low coding efficiency of BPDS modulated signal. Therefore a PWM signal was produced as an alternative candidate

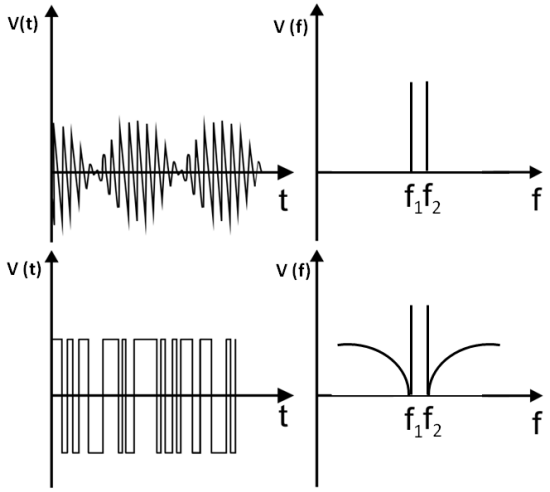

Fig. 2.6: Time and frequency domains of an analog two-tone signal before and after $\Delta\Sigma$ modulation

which does not need such narrow band filter and has higher coding efficiency.

A PWM or square wave (SqW) modulated signal is a signal which consists of a train of pulses the duration of which is varied. The amplitude of the pulses themselves is constant, but the amplitude of the encoded signal is controlled by the width of the pulses or the rate of their occurrence. While the standard pulse-width modulation applies sampling frequencies much higher than the signal frequency, which can be outruled for microwave purposes, another possibility is to choose the standard repetition rate of the pulses equal to the carrier frequency. The amplitude and the phase of an encoded signal are in this case represented by the width and timing (position) of the pulses. By this mean, any complex input signal can be coded into a time-continuous but amplitude-discrete output signal suited for switch-mode amplification.

The principle of encoding the amplitude is illustrated in Fig. 2.7, where a sinusoidal signal with two amplitudes is represented by rectangular pulses with different duty cycle. In order to evaluate the result after the output filter, the PWM signal

a_n, shown in Fig. 2.7 is decomposed into a superposition of different frequency sine signals (harmonics) as in equation 2.5:

$$a_n = \frac{4V_p}{\pi}\Big(\sin(wt) + \frac{1}{3}\sin(3wt) + \frac{1}{5}\sin(5wt) + ...\Big) \tag{2.5}$$

Where:

V_p the amplitude of the pulses (PWM)

w is the angular frequency in radian per second and equal to $2\pi.\frac{1}{T}$

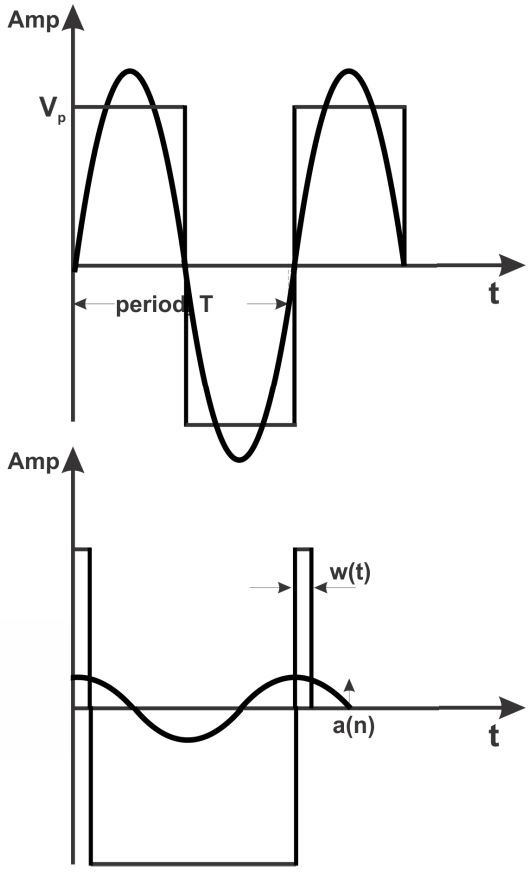

Fig. 2.7: Time domain representation of a bipolar non return to zero (Bipolar-NRZ) PWM signal and its fundamental component

After filtering, only the spectrum around the signal frequency remains. The

amplitude of the resulting sinusoidal signal is given by the Fourier coefficient of first order. The maximum amplitude of a sinusoidal signal that can be encoded in a pulse train of given amplitude, according to equation 2.5, is equal to $\frac{4V_p}{\pi}$ which could be approximated to 1.27 V_p. In this regard, an important figure of merit derived which is called Amplitude Coding Efficiency (ACE). ACE is defined as the ratio between the maximum signal amplitude (A_{signal}) at the input of the modulator and its maxima in the binary pulse train (A_{pulse}) [17].

$$ACE = \frac{A_{\text{signal}}}{A_{\text{pulse}}} \tag{2.6}$$

For PWM signal, maximum ACE that could be obtained is 1.27 for +1V_p . For BPDS signal, ACE is much lower than that of the PWM signal. The maximum coded amplitude for BPDS modulated signal of amplitude +1V_p is equal to 0.8 which almost the half of PWM signal.

Another criterion of an efficient DSP is the Power Coding Efficiency η_c which is denoted as the ratio between the desired in-band RF power to the total power of the modulated signal.

$$\eta_c = \frac{P_{\text{signal}}}{P_{\text{total}}} \cdot 100 \qquad [\%] \tag{2.7}$$

Power coding efficiency can be determined by integration of the in-band power vs. the total output power, which is suited for measurements.

In this work, the PWM and the BPDS signals used are software-generated. PWM signals are originated with the help of Advanced Design System (ADS), while the BPDS signals are generated using Matlab tools.

2.2.2 Driver and Power Amplification Unit

Class-S power amplifier can be designed and realized in two configuration, depending on the switching parameter (current or voltage), a Voltage Mode Class-S (VMCS) and Current Mode Class-S (CMCS). In this work, the main focus is on the VMCS topology which is realized using GaN HEMT transistors (FBH process) with a bandpass output network. The transistors used in the driver stages as well as in the final stage are all monolithic integrated on one chip (MMIC).

2.2.2.1 Current Mode Configuration

The basic schematic of CMCS power amplifier is shown in Fig. 2.8. The two transistors are commonly grounded from the source node. The final stage amplifiers are fed through their gates with a 180° phase shifted signals with the same amplitude (swing) due to their common grounding. The signal amplitude should have a maximum amplitude of $\approx 1V$ for switching the amplifier ON and $\leq -4V$ for switching it OFF depends on the pinch-off voltage of the GaN- HEMT transistor, here FBH GaN-process is considered.

CMCS is drain-feeded through a constant current sources. When Tr_1 is OFF (open), the current from Q_1 (I_Q) flows through the load Z_L and then it will be added to the current of Q_2 (I_Q) so that the maximum current passes through Tr_2 will be:

$$I_{\text{max}} = 2 \cdot I_{\text{Q}} \qquad [mA] \tag{2.8}$$

By taking maximum amplitude of the drain-source voltage (V_{DS}), and amplitude coding efficiency (ACE), and the load Z_L, the current flows in the load is calculated by using the formula:

$$I_L = \frac{V_{max}}{\frac{1}{2} Z_L \cdot ACE} \qquad [mA] \tag{2.9}$$

Considering I_{max}, which is the maximum current the transistor can handle, T_2 is conducting (ON) with a finite drain source ON resistance $R_{DS,ON}$ and drain source

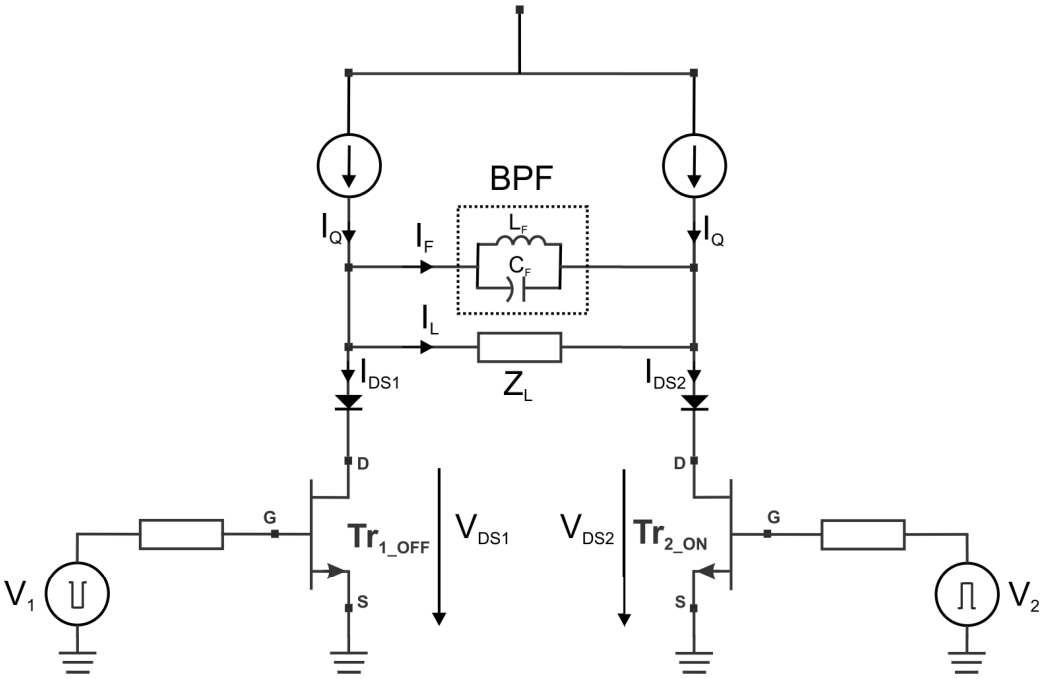

Fig. 2.8: Current mode configuration

capacitance C_{DS}. When Tr_2 is OFF, or Tr_1 is ON, the same procedure occurs but the other way round.

The current in the transistor I_{DS} has a square wave form while that in the load I_L is, in the ideal case, sinusoidal through the presence of the parallel LC network. The voltage across the switched-OFF transistor is sinusoidal since the resonator circuit shorts all the harmonics except the fundamental frequency component (f_0). For a periodic input signal, the drain-source voltage V_{DS} is half-rectified sinusoids while in the case of a non-periodic signal (BPDS), a negative part of V_{DS} appears. Since realistic transistors cannot ensure the OFF-state for negative drain-source voltages, free-wheeling diodes need to be inserted in the drain node of the transistor. The presence of the diodes in the drain prevents negative voltages across the OFF-transistor due to its reverse state operation.

The diode conducts in the forward region of its IV- characteristics, while it blocks when it is reverse biased [18]. The actual operation of the diode (no-negative

part of V_{DS} exists) depends on the switching time of the diode. Hence, diodes with very short switching times and low on-resistance must be employed since the on-resistance can causes considerable losses (always one transistor is in the ON-state carrying the current I_{max}).

Having a constant current source for the current mode topology is a big challenge compared to the voltage source used in the voltage mode topology (section 2.2.2.2). It is less efficient as well, especially in the back-off case, since the power loss in the ON-resistor stays constant as the signal amplitude decreases. Another disadvantage of the current mode configuration is its differential output which needs a balun to convert the differential output signal (balanced signal) out of the filter to a single ended (unbalanced) signal to pass to the load Z_L.

2.2.2.2 Voltage Mode Configuration

The second topology of class-S power amplifier is the voltage mode topology which presented in Fig. 2.9. Here the amplifier works in a push-pull concept in which one of the transistors push the current in the load while the other pulls it back.

The two input signals at the gate have 180° phase difference. Therefore, one of the transistors is switched ON while the other is switched OFF. In voltage mode architecture, the source of the upper transistor Tr_1 is connected to the drain of the second one Tr_2.The supply voltage V_{DD} is applied to the drain of the upper transistor $Tr_1$and the source of the lower transistor is grounded. Hence, the driving voltage of the upper transistor has to be applied between the gate and a floating source while for the lower transistor it is referenced to ground. This is one of the drawbacks of the voltage mode configuration, the asymmetry of the input driving voltage and the floating reference of the upper transistor. Therefore, the upper transistor should have larger input potential compared to the lower one since it has a floating ground. More precisely, the voltage at the input of the upper transistor Tr_1 should swing between the applied drain voltage V_{DD} and a voltage lower

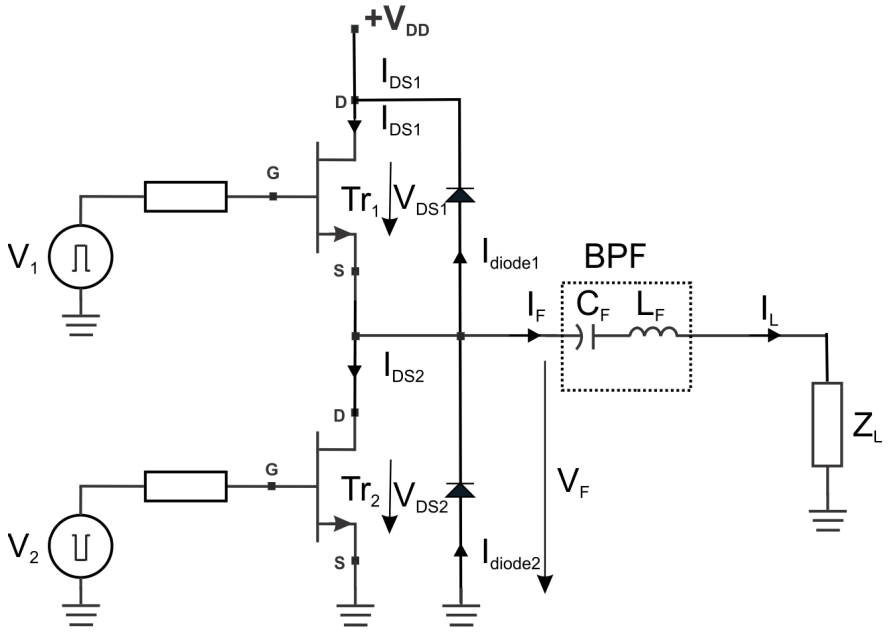

Fig. 2.9: Voltage mode configuration

than the pinch-off voltage of the transistor $V_{pinch\text{-}off}$, to ensure the proper ON-OFF switching.

In our work, to ensure that the transistor is witched ON, the gate-source voltage V_{GS} of that transistor is made between 0..1 V. And for the OFF state, V_{GS} should be less than the pinch-off voltage of the transistor used, typically – 4V is chosen.

Another disadvantage of the voltage mode topology is the unavoidable loss associated with its drain-source capacitance C_{DS} which charges as the transistor switched OFF and discharges through the drain-source path as it goes ON. This energy is lost and can be calculated using the integral of the whole energy (charges) that stored in the capacitance:

$$E_{C_{DS}} = \frac{1}{2} C_{DS} V_{DD}^2 \qquad [joules] \tag{2.10}$$

The power lost in the drain-source capacitance, equation 2.11, is then the amount of energy consumed per unit time:

$$P_{C_{DS}} = \frac{dE_{C_{DS}}}{dt} \qquad [Watt] \tag{2.11}$$

Assuming a periodic signal (10 signal), when the upper transistor Tr_1 is ON, the whole voltage of the drain V_{DD} is applied to the lower transistor Tr_2, so the current passes through $R_{DS,ON1}$ to the load Z_L through the series filter that shapes the current to its form and force it then to be half-sinusoidal. The filter provides higher impedance to all higher harmonics (odd harmonics) and zero (ideally) impedance to the fundamental f_0. In the second half cycle, Tr_2 is now ON and the voltage now applied to the upper one Tr_1 so that the floating node between the source of Tr_1 and the drain of Tr_2 has zero voltage. The current that has been charged the resonator capacitance is now back (discharging of C_F) in the opposite direction (for transistors it remains positive) and completes the other half-sinusoidal shape.

As in the current mode architecture, free-wheeling diodes that placed in reverse direction from drain to source should be used in principle. As the input signal is non-periodic (as the case of a BPDS), backward current (negative current) is expected and this will cause additional loss through the ON resistor $R_{DS,ON}$ since the current will swing between Imax and -Imax. Furthermore, the drain-source voltage across the lower OFF transistor, when the upper is ON and all the drain voltage V_{DD} passes to the lower one, exceeds V_{DD}. There is a short period of time when both transistors are ON, when the voltage at the floating node equal to the pinch-off voltage of the transistor that is OFF by the moment, resulting in a short-circuit between the DC power supply and ground. A large current, called shoot-through current may be produced, which causes energy loss.

Typical VMCS uses free-wheeling diodes parallel to each transistor for protection from backwards current I_{DS} (a negative I_{DS} in Fig. 2.9) for non-periodic signals like BPDS. In this case, the diode capacitance C_{diode} will be added to the transistor's drain source capacitance C_{DS} and causes further loss that degrades the amplifier efficiency. Thus, and to enhance the efficiency, the protection diodes are removed. It

was proved that removing the diodes did no tremendous damage to the transistor as the transistor is rigid enough to a such short-term transitions [19].

2.2.3 The Output Network of Digital Class-S PA

For reconstructing the analog signal out of the broadband stream, a band-pass filter is required at the output of the amplifier. A conventional resonator is sufficient for this purpose. It means that a simple LC network can do the function of picking up our desired frequency from its spectrum. Here, traditional design analysis could be performed, quality factor, transmission bandwidth, and S-parameters losses. To cover all the necessary aspects, however, input impedance Z_0 of the network is of great importance, since it forms the impedance of the final stage transistors.

The quality factor (Q) for the series tank is expressed in equation 2.12. While for the parallel tank, is represented by equation 2.13.

$$Q = \frac{\omega_0 \cdot L}{R} = \frac{1}{R} \cdot \sqrt{\frac{L}{C}} = \frac{Z_0}{R} \tag{2.12}$$

$$Q = \omega_0 \cdot C \cdot R = \frac{R}{\sqrt{\frac{L}{C}}} = \frac{R}{Z_0} \tag{2.13}$$

Where $Z_0 = \sqrt{\frac{L}{C}}$ is the characteristic impedance of the LC network, ω_0 is the angular resonance frequency. As inductor's value increases, quality factor improves as a result. On the other hand, reducing capacitance leads to the same goal as well.

Series tank is normally used in voltage mode switching (VMCS) while parallel tank is used in the current mode one (CMCS) as explained in section 2.2.2. Quality factor could be expressed in term of the 3dB bandwidth as follows:

$$Q = \frac{f_0}{\Delta f} \tag{2.14}$$

For the design of class-S output network, we have used commercial inductors and capacitance (Coilcraft aircore inductors and ATC capacitors). The values of the lumped elements which are suitable for the 900 MHz operation frequency with high Q are quite limited and that adds more restriction to the design of the output network of class-S PA since high voltage and current are expected.

A series band-pass filter is the one required for the voltage switching class-S. Here, studying the S-parameters are all-important. Ideal input reflection (S_{ii}) coefficient should be small at signal frequency and impedance should be high everywhere else. Transmission coefficient is reversed, that is, it should be very high at the signal frequency and small at other frequencies. By this means, we are sure that all the desired signal passes to the load without any reflection and all harmonics are blocked, hence ideally an open is presented to the final stage for those frequencies.

The other factor to be observed is the input impedance of the network. The optimum load impedance (refer to chapter 4, Fig. 4.6) should give an optimum impedance the transistor sees on the input side of the output network. In other words, impedance transformation must offer optimum impedance at the input of the network when selecting the optimum load one.

Optimum impedance can be calculated using equation 2.15 in terms of maximum current of the transistor, maximum applied voltage and amplitude coding efficiency:

$$Z_L = \frac{1}{2}\frac{V_{max}}{I_{max}} \cdot ACE \qquad [mA] \tag{2.15}$$

In our case and for our frequency of 900 MHz, maximum applied voltage (V_{DD}) of 50 V, and maximum current the transistor can bear (we assume a final stage transistor of 1 mm size) of 800 mA, optimum impedance for BPDS signal with 0.8 ACE is found to be 25 Ω. If the 50 Ω at the load is enough to give the 25 Ω at the input of the filter, no matching network is required. Otherwise, a matching network

is needed to match the impedance of the input port of the output network with that of the output..

In this work, we have chosen two different impedances for two different output networks, see next chapter. A compromise between power, efficiency and modulation scheme should be considered when selecting the optimum impedance. No matching network was necessary since the 50 Ω at the output gave us the needed optimum impedances at the input of the LC tank.

For current mode switching, a parallel tank is needed. Other parameters are important here. Even and odd mode impedances are the crucial factors in the design of the output network. A balun is needed in the current mode topology to convert the balanced signal (differential) to a unbalanced one (single ended).

Chapter 3

VMCS Output Network Optimization Techniques

3.1 VMCS Demonstrator and Design Challenge

In this chapter, an attempt to deal with the demanding output network of voltage mode class-S power amplifier is presented. The restrictions of having relatively broad-band filters using discrete elements forced the attention to go to other realization techniques. Distributed elements provide better perforance compared to SMD elements, in general, in terms of steeper slopes and narrower bandwidth responses, at the expense of larger size. Hence, and for a well comparison, two filters have been designed, realized, and measured. The first network is a bandpass filter which includes conventional lumped elements (discrete capacitors and inductors) while the second one has capacitors and bond-wires, the latter replace the inductors in the first case to allow having narrow profiles and shifting the self resonance frequency (SRF) to a higher frequencies.

When it comes to the output network, ideally, the band-pass filter at the output of the final stage must have an infinite impedance at all harmonics as illustrated in Fig. 3.1. Only at the fundamental frequency component (f_0) the filter should have an input impedance equal to the optimum value for the final stage (Z_{opt}), which depends on the transistor sizes etc. In this work and for a 900 MHz signal

frequency, the optimum impedance was realized to be around 28 Ω for the lumped filter. The ideal calculations for the lumped filter and for a BPDS case stated a 25 Ω optimum impedance, see last chapter. Due to the fact that we had only a 50 Ω load at the output port of the filter, only a 28 Ω impedance was reached. To have exactly 25 Ω, a matching network had to be inserted, and more insertion loss had to be considered. The same fact has been taken into account in the bond-wire network case, hence we have accepted an input impedance of 40 Ω which we can get by inserting the 50 Ω port at the output.

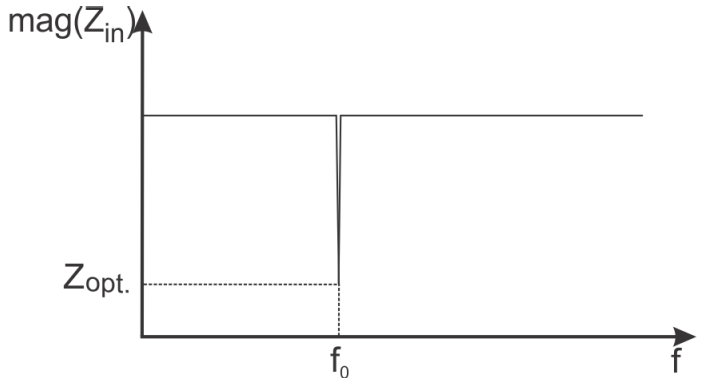

Fig. 3.1: Ideal behavior of the band-pass filter of class-S power amplifier

3.1.1 Drivers and Power-Switch MMIC

Two demonstrators have been designed and realized for an operating frequency of 900 MHz. Fig. 3.2 exemplifies the voltage mode class-S architecture without protection diodes. The BP-DSM bit sequence is preamplified to the proper level needed to drive the following stages ON and OFF. The final stage uses the voltage mode class-D topology with transistors Tr_1 and Tr_2, all of them operate in a digital mode. The output network reconstructs the wanted signal at f_0 from the bit sequence. The filter forces the output current I_F to be approximately sinusoidal while keeping the output voltage in the digital form (rectangular), equivalent to the digital bit stream. That is, ideally, the filter should present to the output stage an infinitely high impedance at all spectral components except that at the operating frequency f_0.

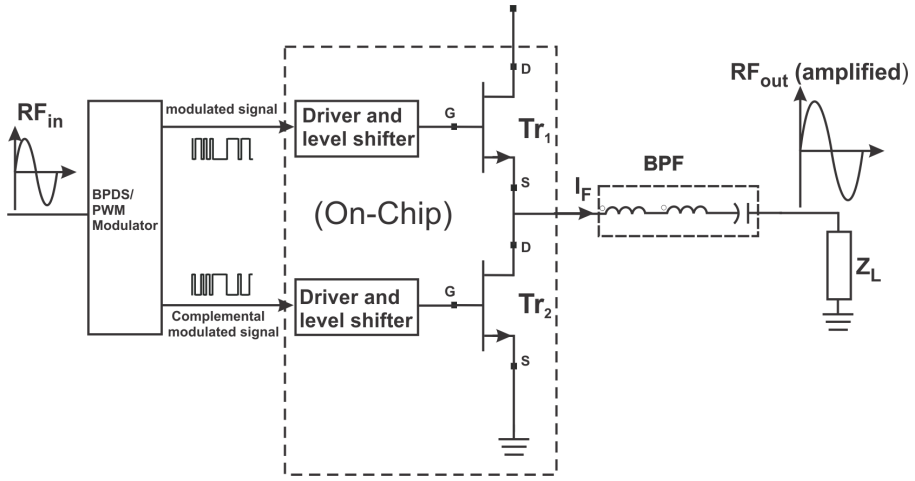

Fig. 3.2: Schematic of the voltage mode class-S power amplifier approach stating its main parts

For the selected frequency f_0 of 900 MHz, the voltage mode class-S module was designed, fabricated and measured. The MMIC (drivers plus switching stage) was already available and is shown in Fig. 3.3. The driver and the final switching stage, which is required for the amplification of the BPDSM bit stream, was fabricated using the FBH GaN-HEMT MMIC process with 0.25μm gate length. The basic structure has been reported in [11] already for a 0.5μm gate process. Fig. 3.3 illustrates the structure and shows the two main parts, the driver and the final stage switches.

VMCS PAs needs an appropriate driver to amplify the input signal, which is in this case the output digital signal of the BPDSM/ PWM modulator. Each of the driver transistors (T_{pre1}, T_{pre2}, and T_{pre3}) was realized using 4x125 μm gate width while both final stage push-pull transistors use 4x250 μm gate width. The circuit was designed employing time-domain simulations, applying the advanced design system (ADS) and a Chalmers (Angelov) large-signal transistor model, developed for the specifics of AlGaN/GaN HEMTs [20].

As shown in Fig. 3.3, the level shifter (driver) has mainly two transistor configurations: the first is a common source amplifier (a) with a resistor (R_1), and the second is a differential amplifier (b) with passive loads (R_2 and R_3), both ensur-

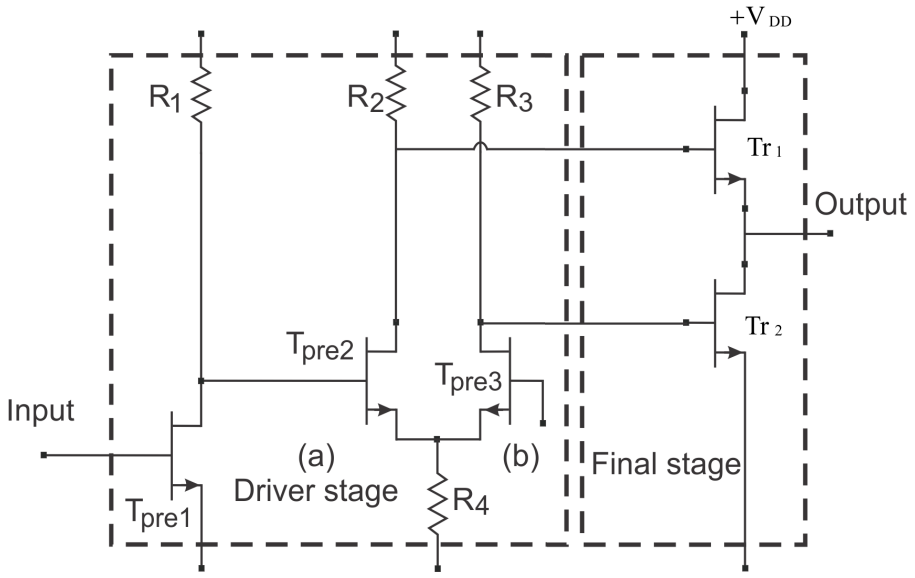

Fig. 3.3: The power switch GaN-HEMT MMIC including driver and final stage

ing broadband characteristics. The first transistor(T_{pre1}) amplifies the BPDS signal, which then is directed to one input of the differential amplifier transistors (T_{pre2}). The gate of the second transistor of the differential stage is directly connected to ground (RF-wise). The two transistors' sources (T_{pre2} and T_{pre3}) are fed through R_4 thus approximating a broadband constant-current source biasing. The first two stages are not yet optimized for low DC consumption. Particularly, the above-mentioned current source should be replaced by a transistor-based one to keep dissipated power low.

The small input signal amplitude (2.5 $V_{p\text{-}p}$) at T_{pre1} is amplified to feed both final stage transistor's gate inputs. Upper transistor gate input amplitude swings between drain supply voltage (V_{DD}) and a voltage selected to be lower than the pinch-off voltage of the transistor $V_{pinch\text{-}off}$ (here about -4 V). The other transistor input swing does not need to be such large, but only 1 V...–4 V, since the source of the lower transistor is grounded (see 2.2.2.2).

3.1.2 Hybrid Lumped Tank: Design Specification and Measurements Results

The lumped band-pass filter was fabricated as a planar hybrid circuit with SMD components on RO4003C PCB laminate (ε_r=3.55) with a thickness of 800μm and an inductor thickness of 17μm. The complete demonstrator (GaN MMIC plus output resonator) was mounted on a copper heat-sink. The MMIC chip is soldered to the heat-sink and connected to the output filter by bond-wires.

Calibration difficulties (different interconnection types: on wafer at the input and SMA connector at the output) are the reason for not having a complete small signal measurement of the filter. But one-port measurements were performed and the corresponding S-parameters will be discussed in the following section.

Two types of measurements were performed: small signal measurements of the output filter and large-signal measurements of the whole amplifier (MMIC and hybrid network), equivalent to the desired class-S operation regime.

3.1.2.1 Small Signal Measurements of the Output Filter

Fig. 3.4 and Fig. 3.5 present the input and output reflection coefficients and the input impedance (simulated and measured) of the band-pass filter. The agreement between simulation and measurements is good. As expected, the bandwidth is reasonable but not ideally narrow, as the order of the filter is restricted due to the limited quality factor of the lumped elements available for planar realization.

An input reflection coefficient of -11 dB is obtained at 900 MHz and input impedance shows good agreement near to 30 Ω, the optimum impedance needed for the switching stage. Because of calibration limitations mentioned previously, Fig. 3.4 shows only the simulated value for the insertion loss (0.4 dB at 900 MHz).

Having a narrow filter characteristics, low reflection at the operating frequency f_0, and high impedance at all frequencies other than f_0 is a key point for the performance of a class-S power amplifier.

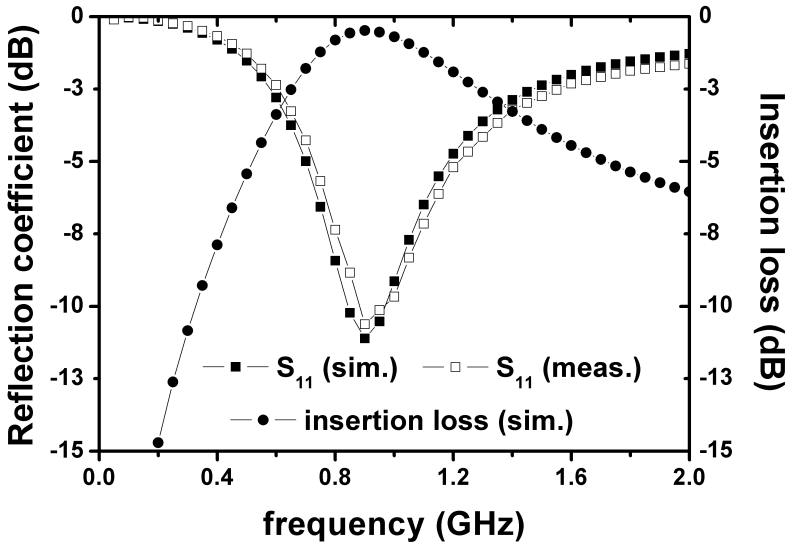

Fig. 3.4: Simulated and measured S-parameters of the output network

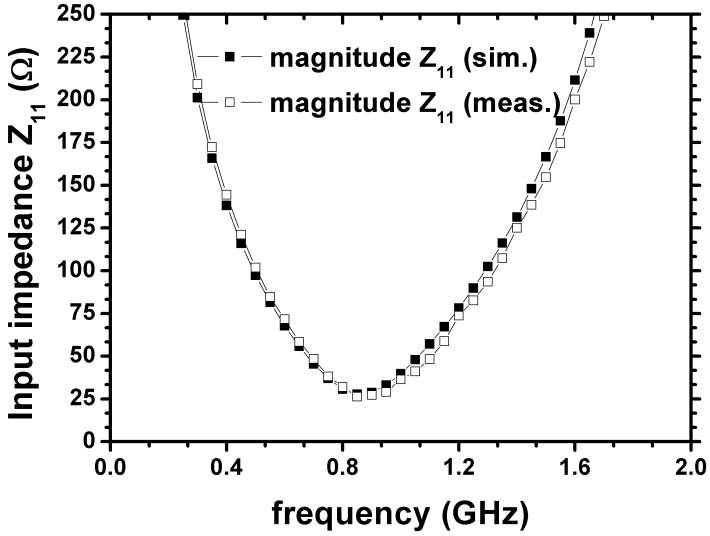

Fig. 3.5: Simulated and measured input impedance (Z_{11}) of the output network

3.1.2.2 Large Signal Measurements of the Demonstrator

The realized module is shown in Fig. 3.6. The class-S amplifier was measured by applying a bit sequence corresponding to a constant-amplitude 900 MHz directly to the GaN MMIC using on-wafer probe tips. The bit stream is generated using Matlab and then loaded into a bit pattern generator. The output port of the module

is formed by an SMA connector.

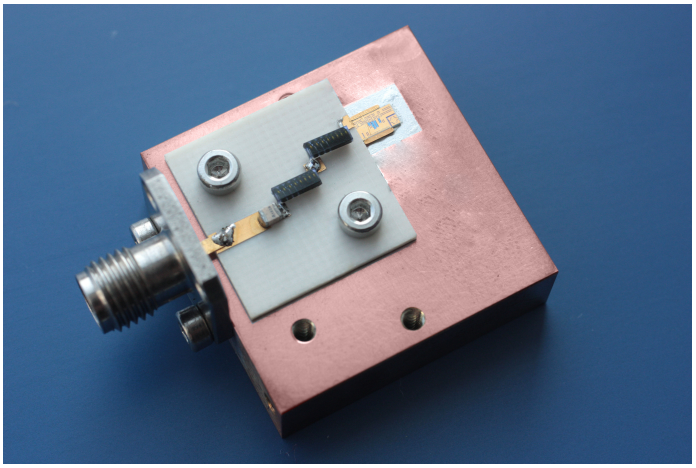

Fig. 3.6: Photo of realized module of VMCS power amplifier with its main parts: GaN pre-amplifier and power switch MMIC and the output band-pass filter

Two types of signals were studied: First, a BPDSM signal with its highest stable amplitude (referred to as "0" dB back-off or full-scale signal) at a bit rate of 3.6 Gbps. For this case, the final-stage DC supply voltage V_{DD} is varied and the output power and drain efficiency (the ratio between output power and DC consumption of the final stage) are reported. In Fig. 3.7, the measured output power at 900 MHz and the related efficiency are plotted as a function of the applied supply voltage V_{DD}. The amplifier delivers an output power of 1.1 W at a drain efficiency of 21%. The efficiency peaks at a value of 33% for 0.3 W output power. It is intentional to display the output power in Watts rather than dBms, since this gives an indication how linearly the power changes with different variables and conditions.

Benchmarking these values at the time of work, one finds that different results have been presented in recent years for class-S power amplifiers with standard BPDSM signal operation. For the voltage-mode version (VMCS) and for a 450 MHz PA, output power/drain efficiency were recorded to be 3.4 W/38%. Maximum efficiency was 52% with 0.5 W output power [11]. The H-bridge topology for 900 MHz frequency band exhibited 2.82 W/22% with maximum efficiency of 27%/1W [12]. The current mode version showed 8.7 W output power and 34% efficiency for

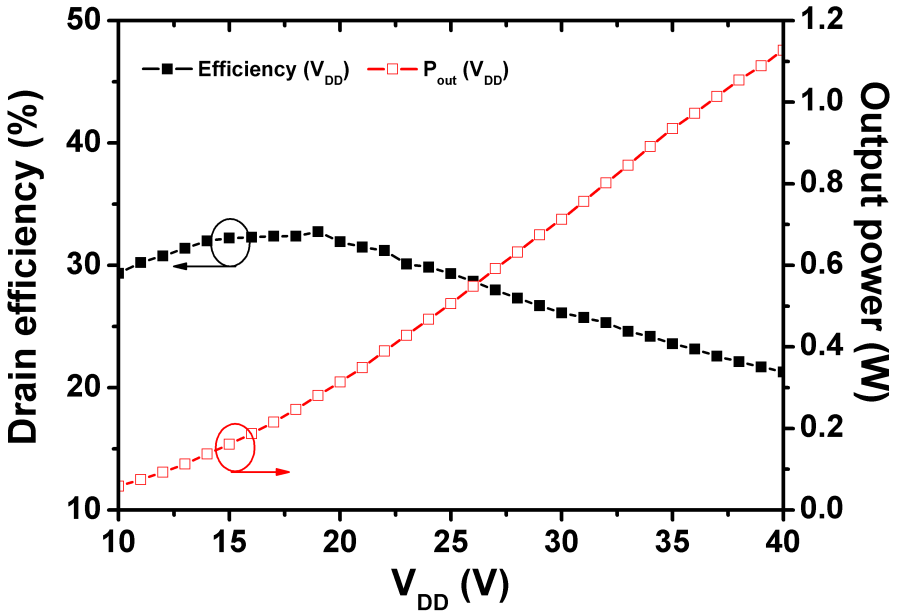

Fig. 3.7: Output power (P_{out}) and final stage drain efficiency of the realized VMCS module as a function of supply voltage (V_{DD}) of the final stage, for full-scale BPDSM signal (0 dB back-off)

the 450 MHz band [21] while for the 955 MHz band with 8.5 dB PAPR and 10 MHz BW, a 5.77 W/33 % was obtained and efficiency was at a maximum of 38.5 % with 1.2 W output power [37].

At 900 MHz, 2.3 W output power with 42% efficiency were reached by CMCS topology [22]. Hence, one can state that for voltage-mode class-S power amplifiers at 900 MHz, the values obtained in this work were best-in-class concerning output power and efficiency using standard BPDSM signal in 2012.

In a second step, further investigations were performed in order to verify the influence of the coding efficiency. We consider here the amplitude coding efficiency ACE, which denotes the ratio between the maximum amplitude of the encoded signal A_{signal} and that of binary pulse train $A_{digital}$. For this purpose, a classical 900 MHz square-wave signal with 50% duty cycle is applied at the input, which is equivalent to a 1.8 Gbps “101010” bit sequence. Again, as in Fig. 3.7, the DC supply

V_{DD} is varied and output power and efficiency are measured. Fig. 3.8 shows the results. The data for BPDSM signal are plotted as well to be compared with that of the square-wave signal (sqw.).

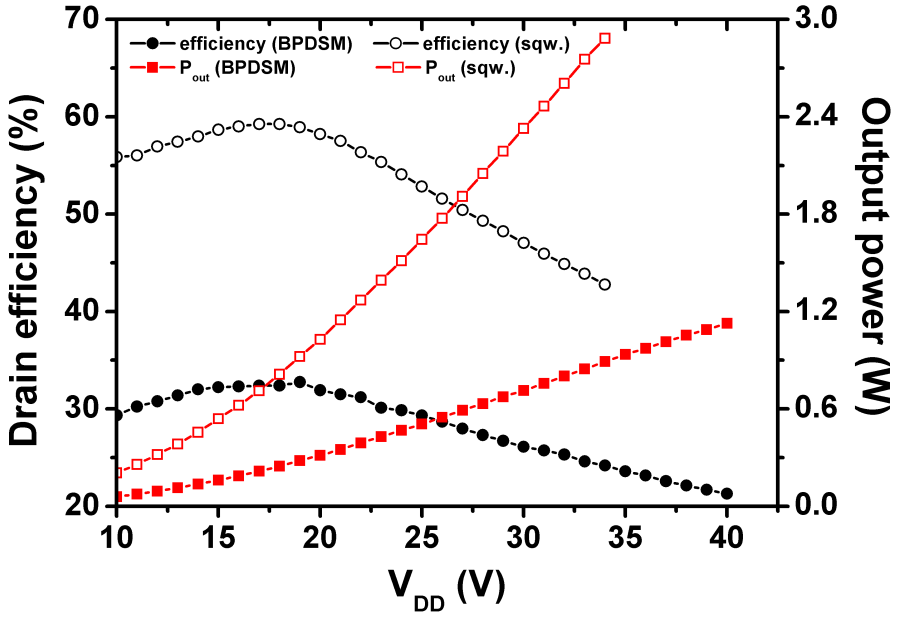

Fig. 3.8: Output power (P_{out}) and final stage drain efficiency of the realized VMCS module as a function of supply voltage (V_{DD}) of the final stage, for both BPDSM and square-wave (sqw.) signals (the BPDSM data correspond to that of Fig. 3.7)

For the square-wave case, almost 3 W output power at a V_{DD} of 34 V (restricted by current limitations) with an efficiency of 43% are reached. A maximum efficiency of 59% is obtained at an output power of 0.8 W. This performance is significantly better than that of the BPDS case, both in terms of output power (3W against 1.1W) and efficiency (43% against 21%). This can be explained by the higher amplitude coding efficiency of the square-wave signal.

Switching losses related to the drain-source capacitance (C_{DS}) are determined by the binary voltage and thus do not vary with the amplitude of the encoded signal. Thus, the coding scheme with the higher coding efficiency leads to better efficiency since the same encoded signal amplitude is realized at a lower loss level [13].

3.1.3 Hybrid Bond-Wires Tank: Design, EM Simulation and Measurements Results

To overcome the limited Q-factor of SMD elements, a bond wire-based filter version was studied and realized. For this purpose, a voltage-mode class-S (VMCS) power amplifier module at 900 MHz was designed and measured, which uses a bond-wire output network. First, a single loop (wire) was investigated, its verified model is then applied and demonstrated for a higher number of wires (four in our case). The next section describes design methodology and measurement results of the proposed models.

3.1.3.1 Bond-Wire Network Design and Realization

According to the class-S requirements, the output network should show high impedance at all frequencies except that of the signal (f_0). The performance of a lumped filter with SMD elements is not enough in this regard because the common lumped inductors involve strong parasitics which corrupt their behavior at higher frequencies due to self-resonance frequencies etc. Our approach is based on the idea of shifting the self-resonance frequency of the inductors as high as possible so that the input impedance beyond the signal frequency gets higher in value.

First, a single bond-wire has been modelled using a measurement-based model as presented in Fig. 3.9. An EM simulation was made to predict the bond-wire behavior regarding input reflections at both ports and the insertion loss. Fig. 3.10 illustrates the realized design of the single bond-wire structure and its proposed EM simulation model.

The model shown in Fig. 3.9 has been extended to include all other parameters , Fig 3.11, that exist in the measured structure, Fig. 3.12. Two submounts (C_{sub}), two bond-wires connecting the submounts to the main bond-wire (C_1, L_1, C_2, C_3,L_2, C_4), plus the main structure with its pads (L_{bond}, C_{bond}). Pads used in the model are the one provided by ADS simulation tool.

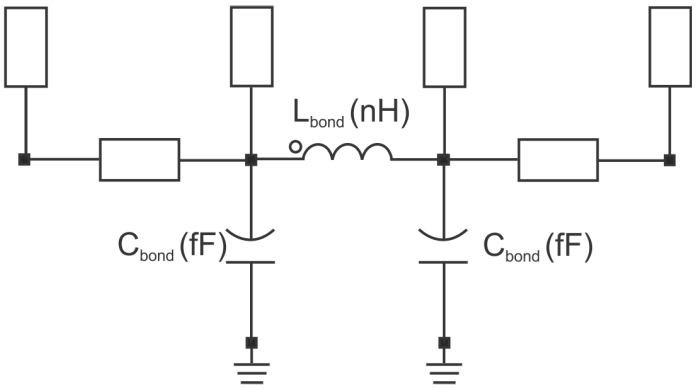

Fig. 3.9: The proposed bond-wire model schematic

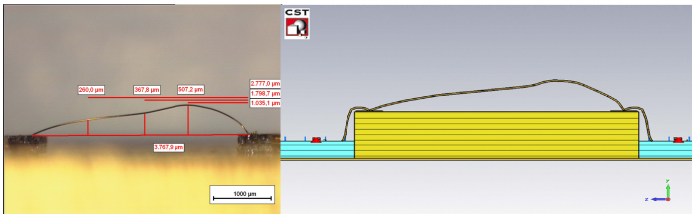

Fig. 3.10: The realized bond-wire

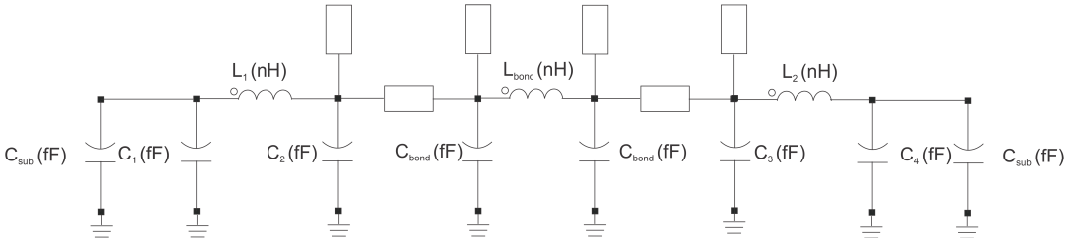

Fig. 3.11: The complete bond-wire model

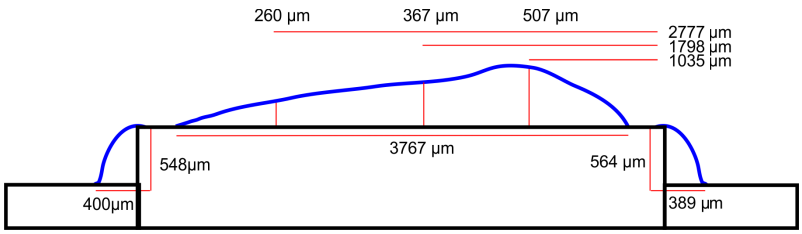

Fig. 3.12: The realized measured structure

The length of the bond wire and the distance the bond wire expands, determine its height (H) and inductance per unit length (L). According to equations 3.1 and

3.2, the inductance value increases with the wire length while the capacitance value is inversely proportional to the bond wire height [23].

$$C = \frac{2\pi\varepsilon}{cosh^{-1}\frac{H}{r}} \tag{3.1}$$

$$L = \frac{\mu}{2\pi} cosh^{-1}\frac{H}{r} \tag{3.2}$$

Where L is the inductance per unit length, and C is the capacitance to ground. The computed values are exact for a wire of infinite length with radius (r) placed at height (H) above an infinite ground plane. Whereas, ε is the permittivity and μ is the permeability of the medium around the bond-wire.

The measured S-parameters and the EM simulation results can be seen from Fig. 3.13 and Fig. 3.14. Good agreement between measurement and simulation can be noticed.

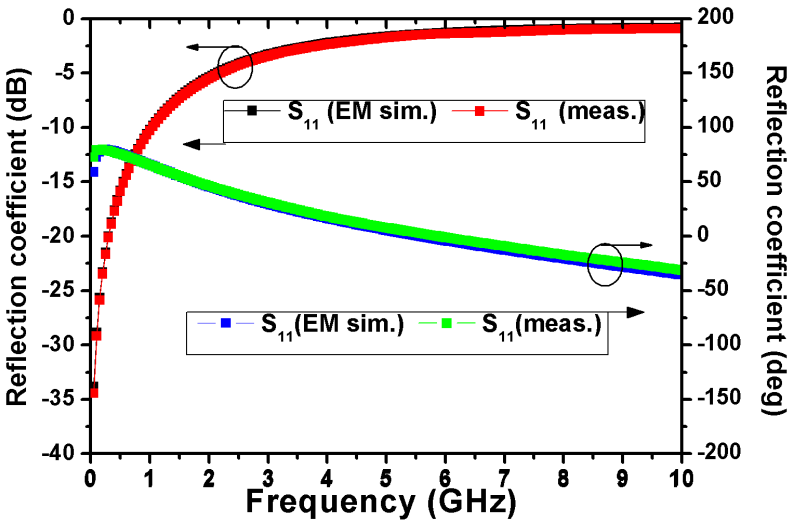

Fig. 3.13: Measured and EM simulated reflection coefficients of the bond-wire structure shown in Fig. 3.12

In a second step, a structure with four bond-wires in series was built (see Fig. 3.15). It was planned to realize about the same value of inductance we had for the

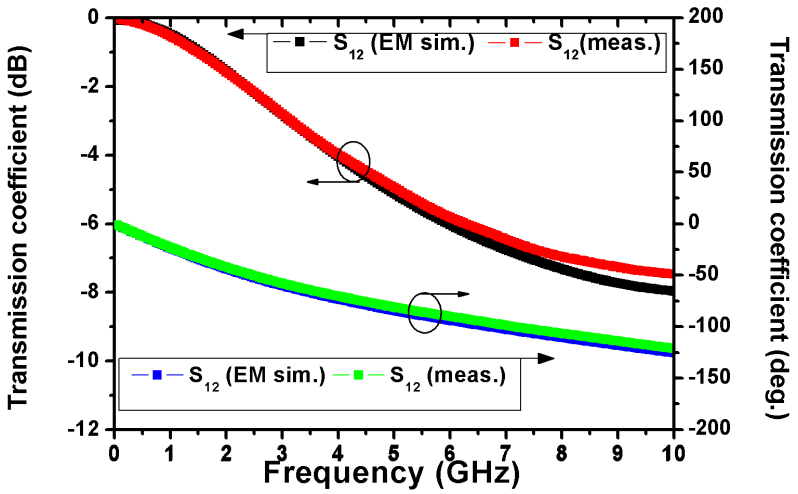

Fig. 3.14: Measured and EM simulated transmission coefficients of the bond-wire structure shown in Fig. 3.11

lumped filter case in Sec. 3.1.2, therefore the selection of four bond-wires has been made. In this way, a correct comparison between the two filters topologies could be performed under the same conditions (same L and C values).

This structure was measured and again we obtain good matching between simulation and measurement data, refer to Fig. 3.16 and Fig. 3.17.

The output filter for the class-S PA was designed by using four bond-wires (standard FBH 25 μm gold wedge bond-wire process) combined with an SMD capacitor. The network was realized on a Rogers PCB laminate (ε_r=3.55) with 800 μm substrate thickness and 17 μm conducting strip. It was mounted on a copper heatsink.

3.1.3.2 Bond-Wire Output Network Measurement

As a first step, the designed and realized output network was measured under small signal excitation to examine input reflection and input impedance. The output port (SMA port) was terminated with 50 Ω impedance. Fig. 3.18 displays a comparison between input reflection coefficient of the bondwire network and the conventional lumped version.

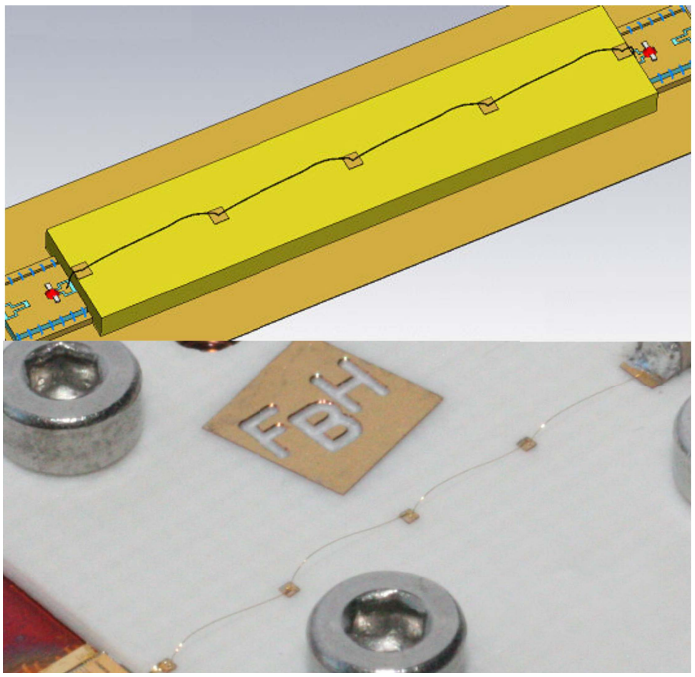

Fig. 3.15: Structure with four bond-wires: EM simulation layout and the realized structure

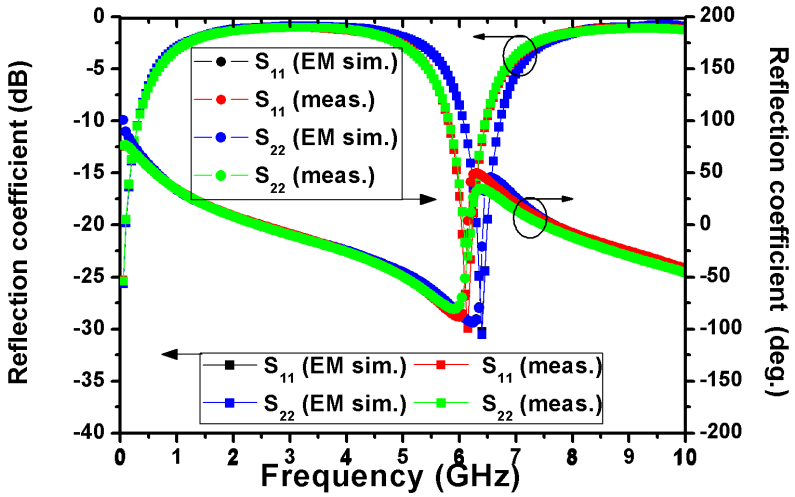

Fig. 3.16: Measured and EM simulated reflection coefficients structure shown in Fig. 3.15

Input reflection at the input port (S_{11}) shows better matching at the signal frequency f_0 (900 MHz) for the bondwire case, -20 dB compared to around –11 dB.

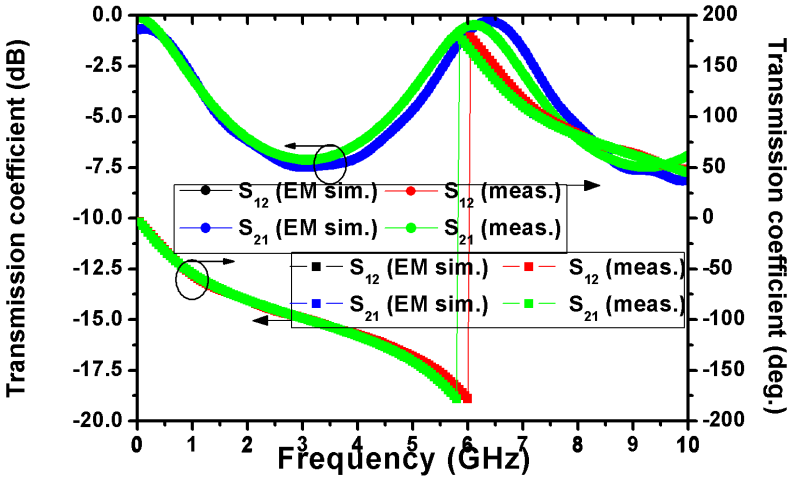

Fig. 3.17: Measured and EM simulated transmission coefficients of the structure shown in Fig. 3.15

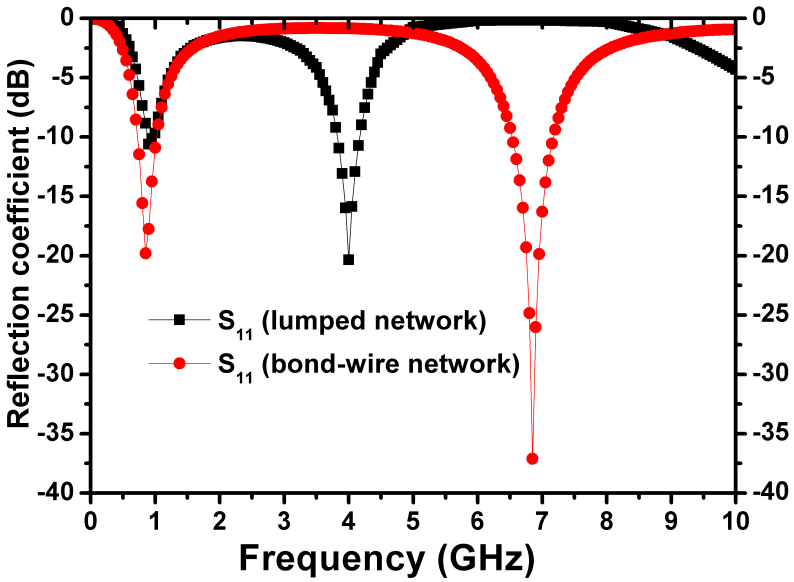

Fig. 3.18: Reflection at input port for conventional lumped and proposed bondwire networks

Moreover, the parasitic resonances are shifted towards higher frequencies, the first one from 4 GHz for the lumped network to almost 7 GHz, i.e., the 7th harmonic of the intended signal frequency of 1 GHz.

Fig. 3.19 presents the same data as Fig. 3.18, but in terms of input impedance

instead of reflection factor. As can be seen, the bond-wire version yields higher input impedance values up to more than 4 GHz than its lumped counterpart. Particularly, it shows higher suppression for the 3rd harmonic. These improvements correspond with the expectations. They should reduce power loss outside the signal band and thus increase the efficiency of the voltage digital mode class- S.

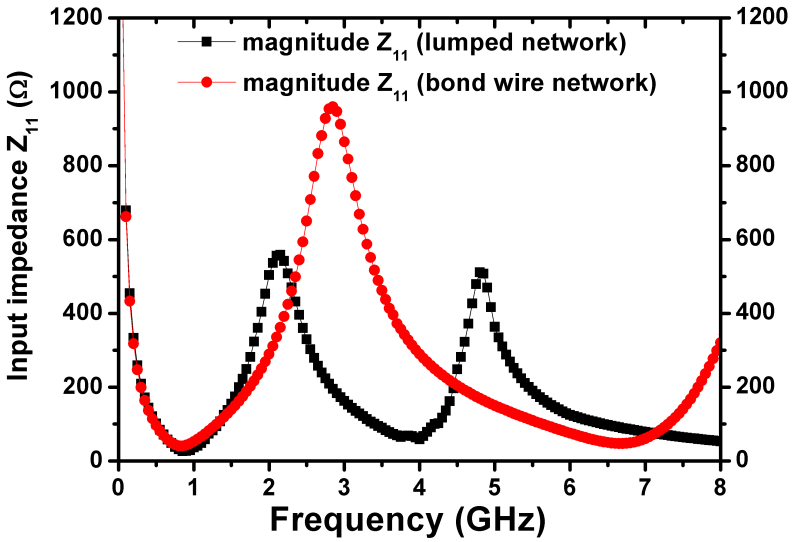

Fig. 3.19: Impedance at input port for conventional lumped and proposed bond-wire networks

3.1.3.3 Voltage Mode Digital Class-S with Proposed Filter

The complete module was realized using a VMCS GaN MMIC, [11], and the bond-wire output network described above. Fig. 3.20 shows the demonstrator.

A BPDS signal (full-scale) was used as input signal, and the amplifier was operated over a range of MMIC supply voltages. The measured output power and efficiency data are plotted in Fig. 3.21. The figure includes also efficiency and power results of a class-S PA with an equivalent lumped output network (L-C network), measured for the same excitation signal. Note that drain efficiency here refers to the drain efficiency of the final stage only.

For the supply voltage range until 21 V, one can see that the demonstrator with

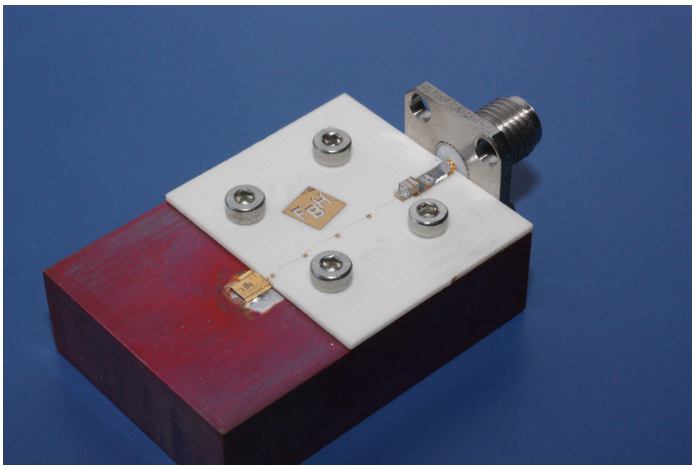

Fig. 3.20: Class-S power amplifier with bond-wire filter

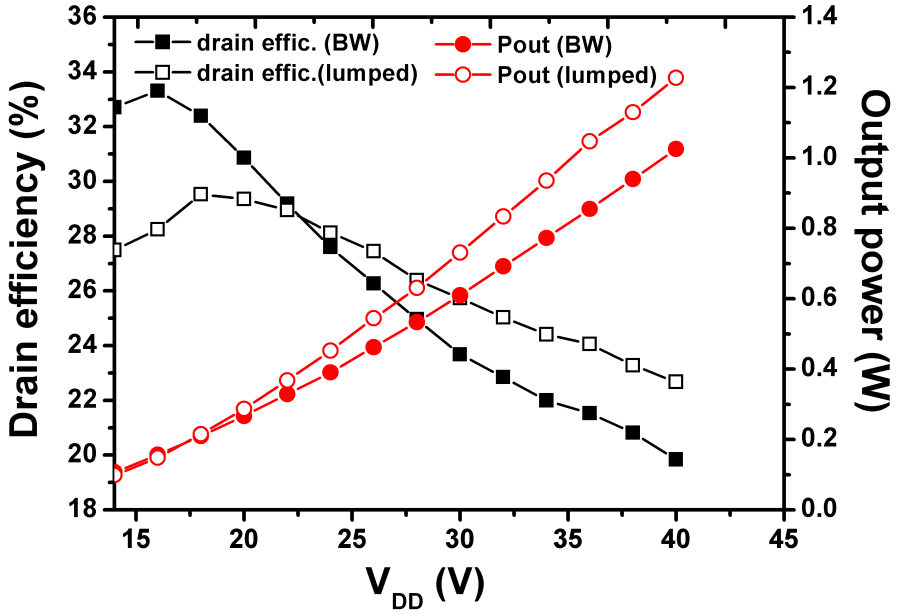

Fig. 3.21: Power and final-stage drain-efficiency of the class-S PA with two different output networks: bond-wire (BW) and lumped ones

bond-wire network shows enhanced efficiency over that of the lumped one. But one observes a drop in output power with growing supply voltage so that for higher voltages (and output powers) the lumped version achieves more favorable results.

From previous work we know that the decrease in efficiency for increasing supply voltage is in most cases related to thermal effects, because the output power as well as the dissipated power increases with supply voltage, which leads to higher junction temperature and thus worse efficiency and reduced output power.

Due to the excellent thermal properties of the SiC MMIC substrate, it is not the substrate itself but mounting and soldering of the MMIC which plays a key role here and thus the differences in efficiency are clouded by the uncertainty of the actual thermal resistance. Hence one can explain the results of Fig. 3.21 as follows:

- For supply voltages below 20 V, thermal aspects play a minor role, and we see the improvements due to the bond-wire filter, which are related to its better broadband impedance behavior (see Fig 3.18 and Fig. 3.19).
- For higher supply voltages, the thermal effects dominate and the improvements of the bond-wire filter are offset by the spread in thermal resistance of the MMIC between the two modules

The approach used in this paper is new, thus a state-of-the art is not included as a result [24].

Chapter 4

Load Pull Measurements for Digital Microwave Power Amplifiers

4.1 Some Basic Facts

As it has been explained, the increasing growth in wireless communication standards puts a huge demand on the power amplifier unit in modern base stations, in terms of output power, efficiency, gain, and linearity.

Therefore, the design of power amplifiers has become a top research subject. To provide good efficiency, output power, and linearity, a concrete and reliable set of design parameters is needed. Recent simulation tools have improved and accelerated the PA design process but there are still restrictions. One is the accuracy and rigidity of the transistor model. Both measurement-based models and polynomial-based models [25, 26] show deficiencies.

A pragmatic solution to overcome this limitation is the source and load pull techniques that deliver measurement data on the nonlinear transistor behavior. In this work the focus is on the output part of the device where the power and efficiency are mainly determined by the proper termination.

An additional target behind dealing and applying load-pull measurement on class-S digital microwave PAs is to obtain information on the amplifier's linearity and distortion bahavior, i.e., the amplitude-amplitude (AM-AM) and amplitude-phase (AM-PM) distortions (this is the topic of the next chapter 5).

In general, the load-pull set-up is a system where the performance of a device under test (DUT) is characterized dependent on varying the impedance at its output port. In the context of power amplifier design, nonlinearity and distortion plays a major role in determining the best loading condition of the DUT. Those conditions are different from the loading condition of the linear case which can be extracted from the S-parameters. The load-pull technique helps pinpointing the optimum loading conditions experimentally while physically varying the load (output) reflection coefficient Γ_{L}. Fig. 4.1 depicts the basic principle behind the load/source pull technique. A tuner at the input/output ports (either active or passive tuners can be used) along with other measurement controlling components are used to tune the impedance at the load/source ports to match the desired optimum impedance.

The reflection coefficient at output port Γ_{L}, in which we are mainly interested, is defined as the ratio between the incident and reflected traveling waves, a_2 and b_2, see equation 4.1. It could be described by the desired matching impedance Z_{L} and the correspondent characteristic impedance of the system Z_0, equation 4.2 , typically taken to be 50 Ω.

Load-pull measurements can be classified as either passive or active. In the passive case, the one used in this work, the impedance is synthesized by varying the reflection coefficient of the impedance controlling element (the tuner) while in the active technique the reflection coefficient is controlled by injecting a signal which in turn controls the gain around the active structure.

$$\Gamma_L = \frac{a_2}{b_2} \tag{4.1}$$

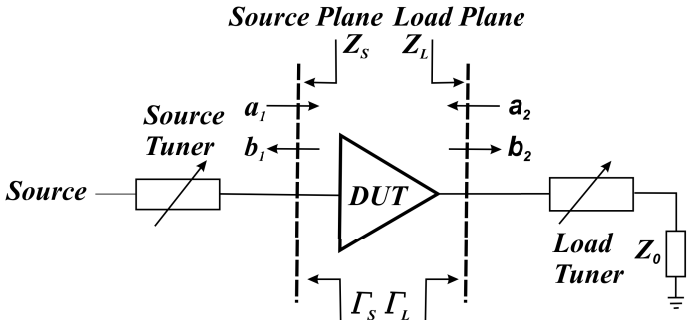

Fig. 4.1: Reflection coefficient at source and load ports

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{4.2}$$

4.2 Load Pull Measurement Technique for Hybrid-Digital PA

For the characterization of microwave class-S digital power amplifier, the setup shown in Fig. 4.2 was built up. Before launching the measurements, the DUT was substituted by a Thru and the input signal was observed at different positions to ensure that the stimulus is fine enough and distortion-free. The first plane of observation is at the input side of the DUT after the driver. There we can see whether the shape of the input signal is of accepted profile, see Fig. 4.3a. The second position is at the very input of the DUT at reference plane 1. Again, the recorded signal is not corrupted too much after passing the attenuator, the directional coupler, and the bias-tee, as it is shown in Fig. 4.3b. The last plane of observation is the output before the oscilloscope and the signal there has the shape of Fig. 4.3c. The circuit under consideration here is the class-S PA with lumped output network, as described in chapter 3.

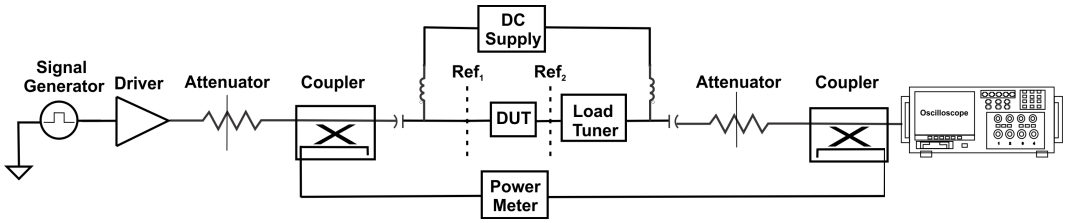

Fig. 4.2: Load-pull measurement setup for digital microwave PA

4.2.1 Load Pull Measurements of Digital PA with Lumped Output Network

The digital class-S with lumped tank, see section 3.1.2, is first measured under load-pull environment without and with controlling second and third harmonics, which are the closest to the fundamental and most important.

The case without harmonics control and for a typical 1.8 Gbps periodic square-wave input signal with 3.5 $V_{P\text{-}P}$, 20 V drain applied voltage,, yields maximum output power contours of 30.2 dBm with 46 % drain efficiency (represented by a black point) and a maximum drain efficiency of 65% with 28 dBm power (represented by red point), refer to Fig. 4.4. Peak power impedance is located in the capacitive part of smith chart while efficiency optimum impedance is located in the inductive part. We measured also the 50 Ω case during the load-pull characterization. Although data at this particular load impedance are already known (chapter 3), having them is still worthy since it adds more reliability to our previous work. In comparison to it, an output power of 29.8 dBm and a drain efficiency of 54% were obtained (30 dBm and 58% are recorded earlier). The slight change might be due to the different and long path of the signal to the amplifier in the load-pull measurement case, which might deform the square-wave profile and causes extra imperfection in switching behavior compared to a direct signal applied from the pattern generator in the measurement of chapter 3.

The output signal at the load for maximum power case is presented in Fig. 4.5, small ripples appear, which is an indication of higher frequency components passing to the load due to insufficient reflection at the filter.

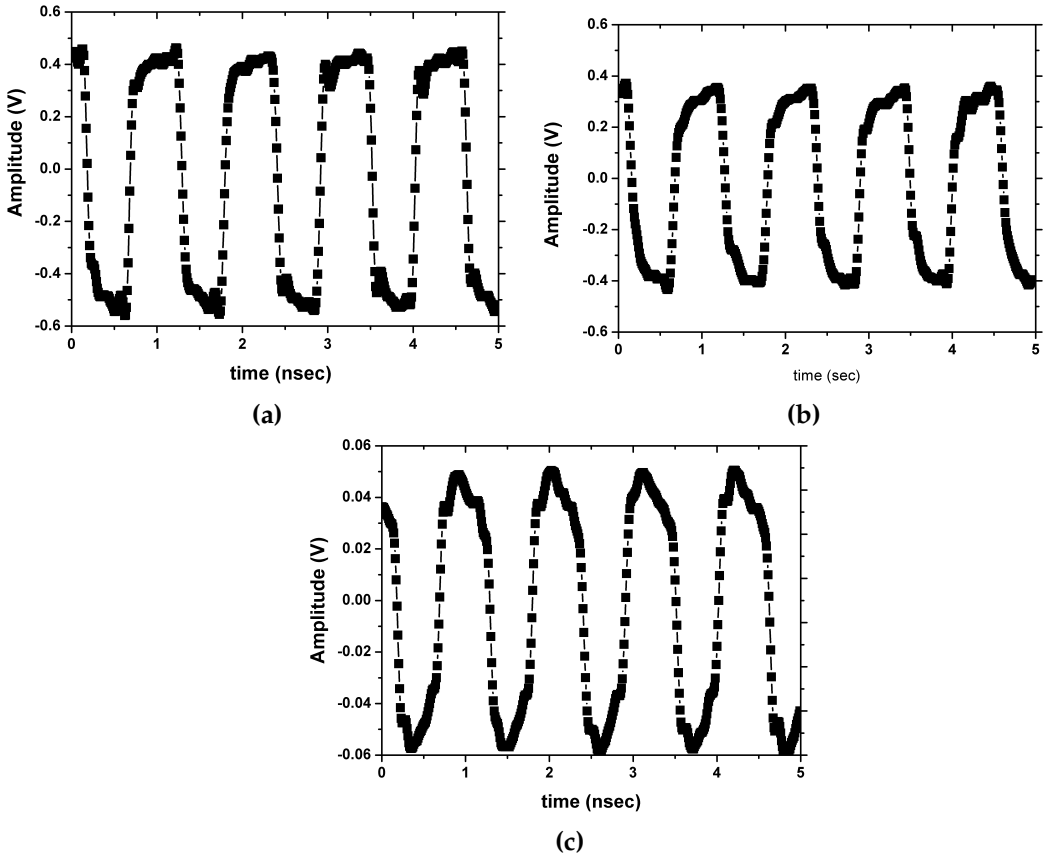

Fig. 4.3: Stimulus signal as it is recorded at different positions in the load-pull measurement setup, at the DUT input after the driver (a), at reference plane 1 (b), and at the input of the oscilloscope (c), with a Thru replacing the DUT

For the sake of analysing the data obtained from of the load pull characterization, a simulation bench of a simple two port circuit was built to extract the transistor's optimum impedance and the obtained impedance $Z_{LP(opt)}$ is used at port 2, as is viewed in Fig. 4.6. This way, one can find which impedance is best for the transistor to see ($Z_{in\,(opt)}$).

Important to look for, rather than which impedance the transistor sees, is the reflection coefficients on both ports, that is, at the input/output of the lumped network S_{11}, S_{22} plus transmission coefficient S_{21} that indicates the insertion loss of the output network. For optimum power impedance case, the input reflection co-

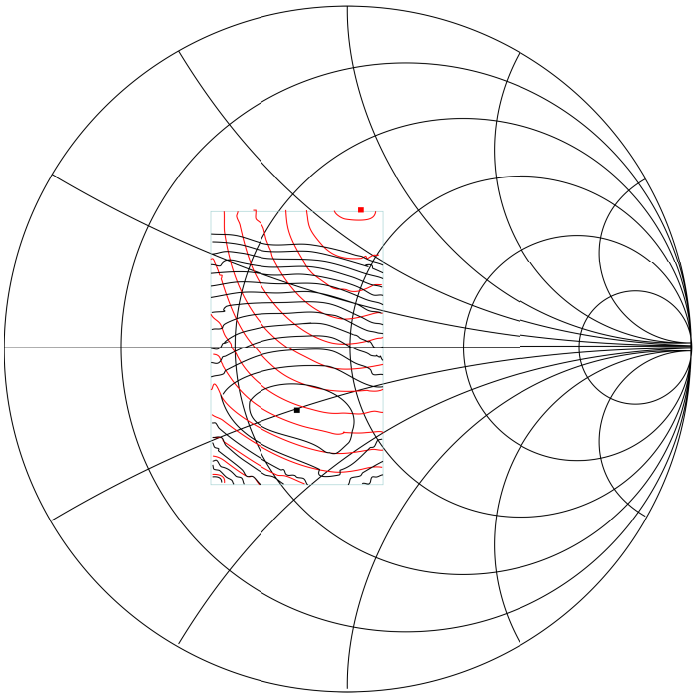

Fig. 4.4: Load-pull measurement contours, power maximises at the black point and drain efficiency at the red one, for class-S amplifier for the case of lumped element network with no control over harmonics

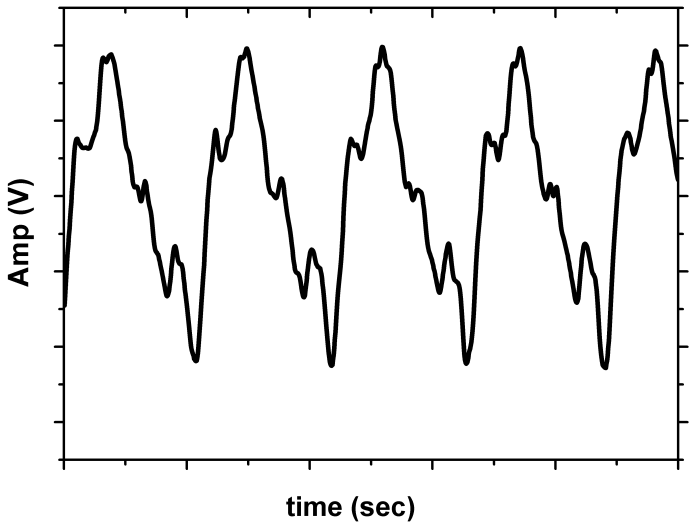

Fig. 4.5: Output signal waveform for digital PA with lumped network and without harmonic control for the optimum power impedance case

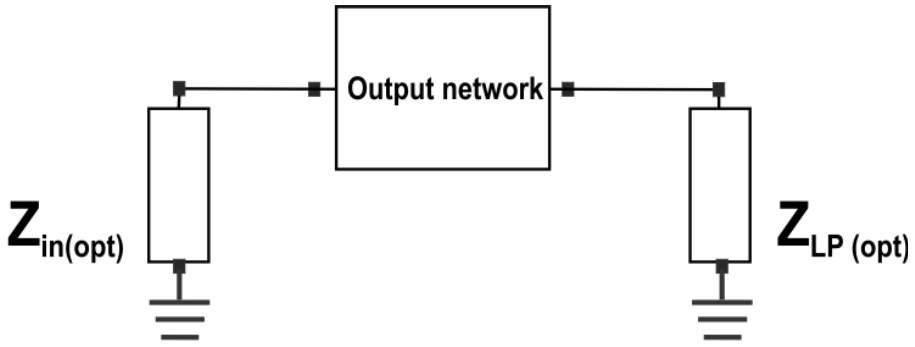

Fig. 4.6: Simulation bench of two-port network for extracting optimum transistor's impedance

efficient S_{11} is about 17 dB while that of the output port S_{22} reaches 16.4 dB, see Fig. 4.7. S_{21} is found for this step almost 0.27 dB. Those values are considered to be acceptable (better than 15 dB for reflection and 0.5 dB for insertion losses).

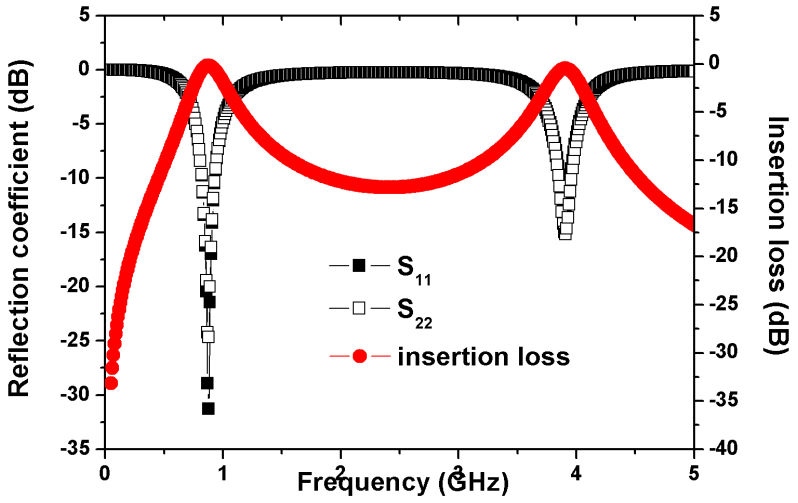

Fig. 4.7: Reflection and transmission coefficients for optimum power impedance

For optimum efficiency impedance case, Fig. 4.8, the value of S_{11}, for our operating frequency 900 MHz, expresses too much loss compared to the previous case of optimum power impedance, Fig. 4.7). Insertion loss increases as well. This degradation in performance belongs to the fact that optimum efficiency impedance is located in the inductance part of smith chart . That is, the inductive part of the impedance (Z_{opt}=R+jX_L) shifts the resonance frequency to a lower value. While the

capacitive part (Z_{opt}=R-jX_C) in the optimum power case is added in series to the filter's capacitor value, and hence no remarkable change occurs.

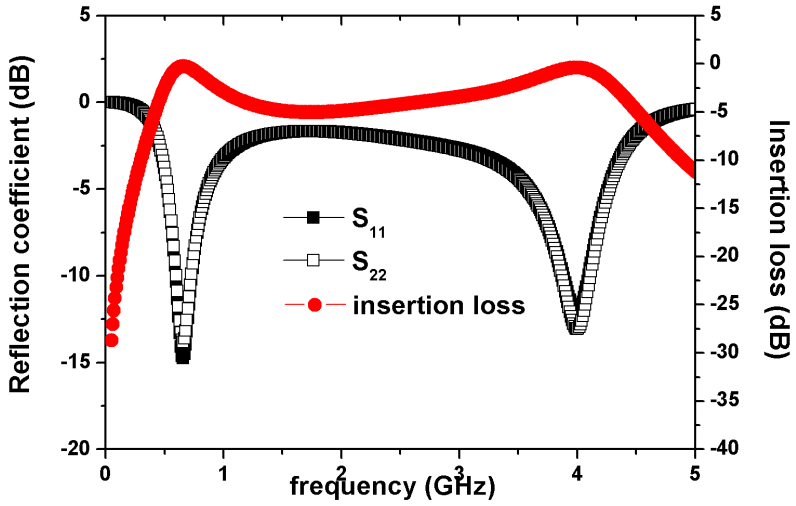

Fig. 4.8: Reflection and transmission coefficients for optimum efficiency impedance

A second set of measurements was performed by having harmonics control over the second and the third harmonic components which are considered in digital signal (square-wave profile) the most dominant ones. The second harmonic was first shorted and the third one was opened. This yields with the same inputs (a square-wave signal of 3.5 $_{P-P}$), 50% duty cycle, 1.8 Gbps, and 20 V_{DD}) to similar contours to the case without harmonics control, with slightly shift of power/ efficiency optimums as it is shown in Fig. 4.9. Here, best power was found to be 30.11 dBm (40%) and best drain efficiency was 63% (28 dBm). Output signal is seen in Fig. 4.10. Again we do not have a pure sinusoidal because of some harmonics pass to the load.

Lastly, for lumped tank, the shorting and opening of the second and third harmonics are interchanged, that is, the second one is open and the third is shorted. Maximum power and efficiency are not changed, 30 dBm (46%) and 63% (28.3 dBm). Thus, it is concluded that controlling harmonics (that pass to the load due to the imperfect filter suppression) does not improve power and drain efficiency noticeably. As a result, we did not investigate the reflection and transmission losses

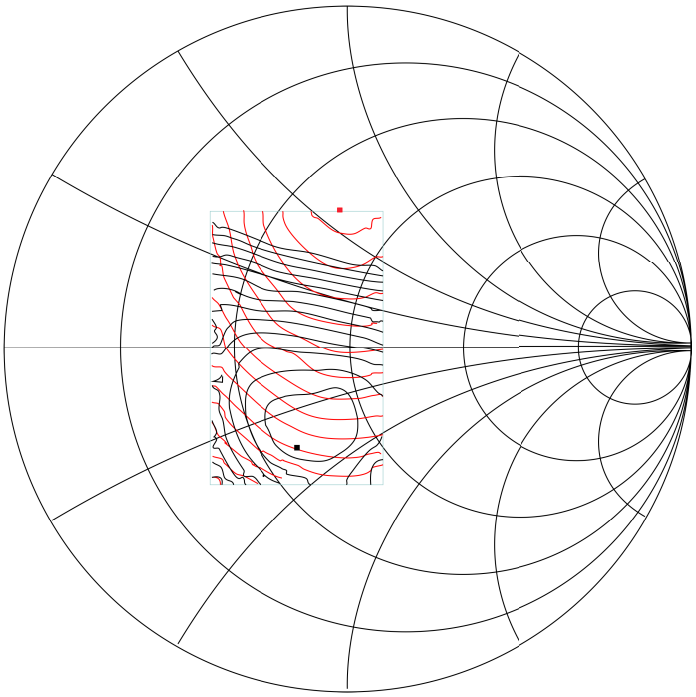

Fig. 4.9: Load-pull measurement contours for class-S amplifier with lumped element network with second harmonic shorted and third opened

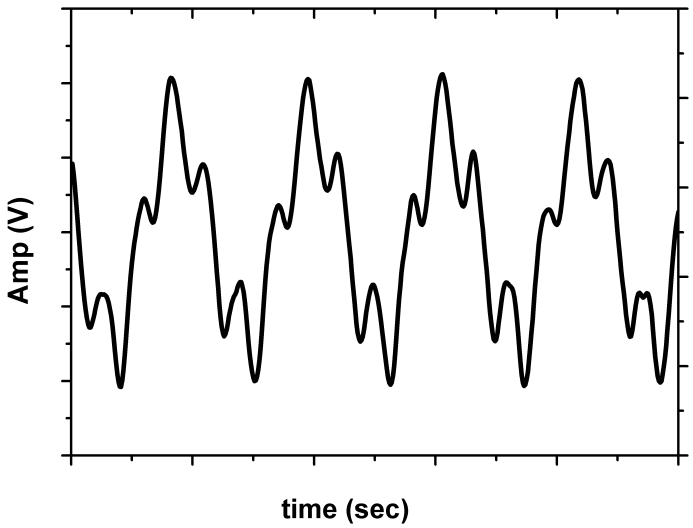

Fig. 4.10: Output signal waveform for digital PA with lumped network and with second harmonic shorted and third opened

for those two cases.

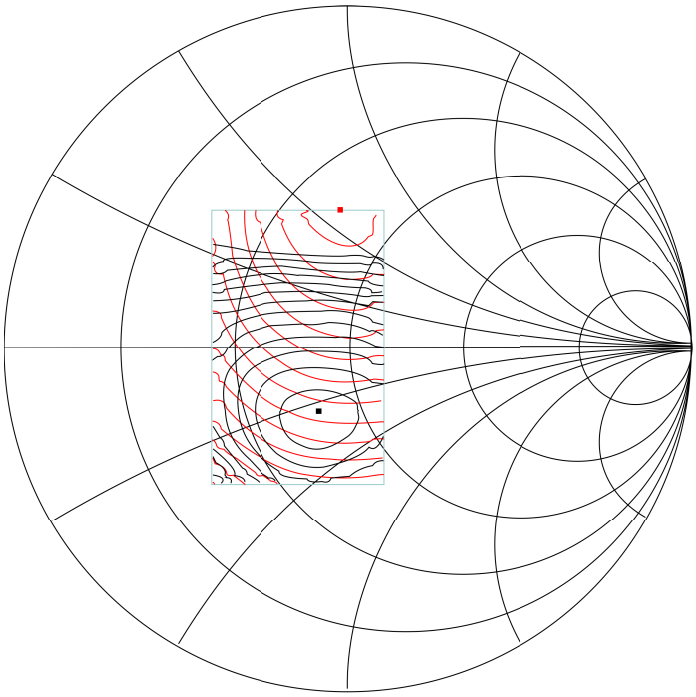

Fig. 4.11: Load-pull measurement contours for class-S amplifier with lumped element network with second harmonic opened and third shorted

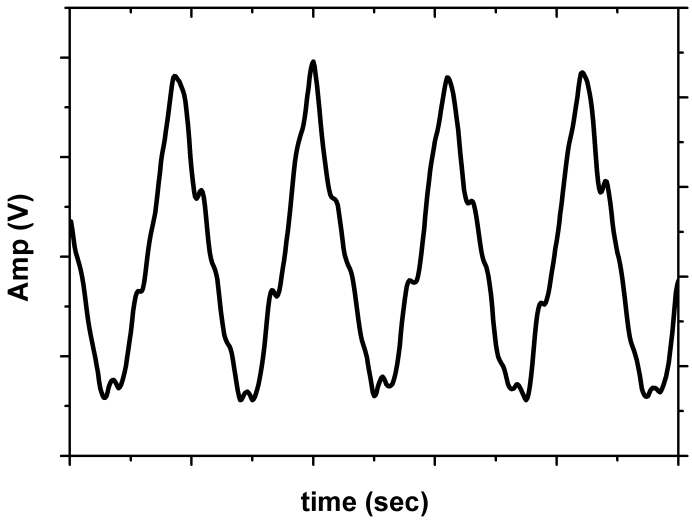

Fig. 4.12: Output signal waveform for digital PA with lumped network and with second harmonic opened and third shorted

Looking at the load-pull results, we can conclude that proper termination can influence the overall performance of a class-S PA. In the measurement without har-

monics control, about 0.4 dB improvement was reached compared to the 50 Ω case. Drain efficiency (final stage only) improves by 11%. The second case, which imposes shortening second harmonic and opening the third, has similar enhancement: 0.41 dB more power and 9.5% better efficiency. The last case (second harmonic is opened and third is shorted) exhibits 0.3 dB with 9.8% extra drain efficiency.

Optimum loading does not only mean improvements in output power and efficiency, but it also contributes to a better output signal (before filtering) shape which in turn affects the linearity and distortion of the switching amplifier. Since the mechanisms behind the distortions in the case of the digital PA differ basically from that of the analog PA, they are studied in more details in the following chapter using their well-known amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) characteristics as a gauge.

Chapter 5

Linearity and Distortion Analysis of Class-S Power Amplifier

5.1 Efficienct Transmission Systems Demands

Output power, efficiency, and, above all, linearity are the crucial factors for any wireless transmitter. Output power is the criterion for spatial coverage or cell size, efficiency determines the battery lifetime for portable mobile devices and energy cost of base stations, and linearity is of great importance not only for data rate, but also for mitigating interference with nearby channels and for holding the transmitted signal within a predefined spectral mask [27]. Any nonlinearity in the power amplifier will lead to spreading of transmission spectrum which is also called "spectral regrowth". Spectral regrowth could be minimized if signals with constant envelope modulation techniques were used, but this approach suffers from the quite low data rate/ bandwidth ratio which is known as "spectral efficiency".

For spectral efficient communication systems, more complicated modulation techniques have been introduced, see chapter 1. Such a modulated signal, like LTE-Advanced, uses OFDM techniques that provide high spectral efficiency but require higher PAPR which can reach 10 dB back-off. Although the power amplifier is operated in the back-off region, it is necessary in state-of-the-art mobile communication systems to maintain efficiency and linearity.

Since the information is contained in amplitude and phase, nonlinear PA introduces errors in both quantities and can cause severe degradation of the system performance. The relevant quantities are amplitude error or amplitude conversion (AM-AM), also known as gain compression in linear PAs, and phase error or phase conversion (AM-PM). AM-AM is the nonlinear relationship between the (encoded) RF signal amplitude at the input of the modulator and the resulting RF signal amplitude at the RF power amplifier output. Deviation from the linear response is demanded to be as small as possible. AM-PM refers to the phase change between the modulator input signal and the amplifier output signal as the amplitude of the input signal alters [28, 29]. Linearization techniques like Digital Pre-Distortion (DPD) are used commercially to mitigate the distortion effects.

5.2 Linear vs. Nonlinear Systems

Electrical systems can be classified into linear or nonlinear systems, with or without memory effects. As an example: memoryless systems are those with linear or nonlinear resistors and when introducing an energy storage element such as a capacitor to that system, it makes it linear/ nonlinear with memory effects. Capacitors and inductors are considered as memory-introducing elements since the voltages/ currents at a specific time do not depend only on the currents/ voltages at that instantaneous value but also on previous values of those currents/ voltages. The voltage across the capacitor is the integral of the current from time -∞ to time t over the capacitor's value:

$$v(t) = \frac{1}{C}\int_{-\infty}^{t} i(\tau)d\tau \qquad [V] \tag{5.1}$$

Similarly, the current passing through an inductor is the integral of the inductor's voltage from time -∞ to time t over the inductor's value:

$$i(t) = \frac{1}{L}\int_{-\infty}^{t} v(\tau)d\tau \qquad [A] \tag{5.2}$$

In this regard, one can conclude that the time response of the circuit is not instantaneous, but takes longer time depending on the system's length of memory. In frequency domain, this can be considered as a frequency-dependent amplitude and phase shift.

Linear systems are those systems having their output linearly proportional to their input. A power amplifier is considered linear if it has an output which is linearly-dependent on its input (dashed line in Fig. 5.1). While nonlinear systems or PAs are those whose output is a nonlinear function of the input (solid line in Fig. 5.1).

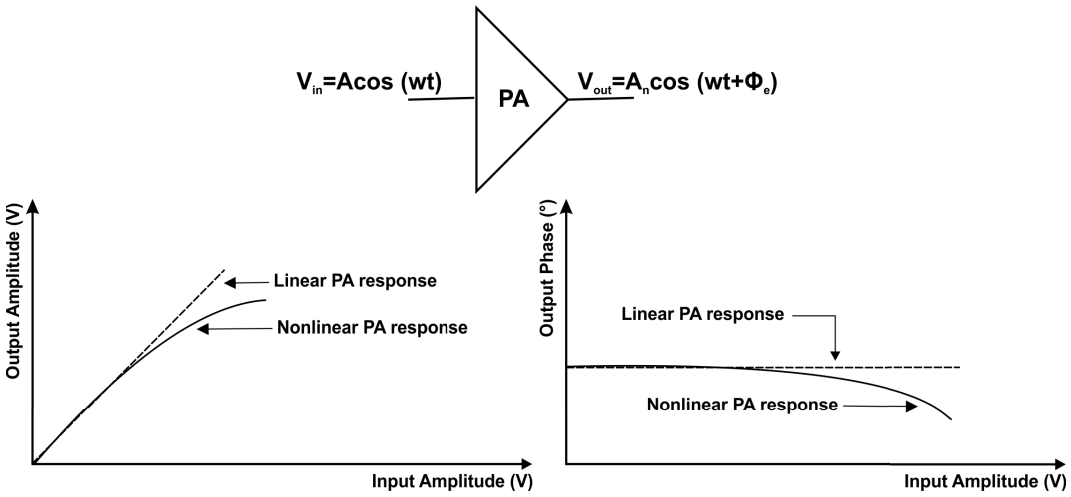

Fig. 5.1: Linear and nonlinear PAs

where A_n is the output value of the PA's amplitude and ϕ_e is the phase added by the nonlinear PA.

In this work, nonlinearity of class-S power amplifier that causes distortion to the amplified signal is analysed and discussed. Different signals with different back-offs have been used to further investigate distortion issues from various aspects. AM-AM conversion is calculated by taking the deviation from the linear slope of the signal. First, linear output amplitude is calculated by finding the linear slope based on a certain reference point which is 0 dB back-off or full-scale (FS). Linear

PA slope is calculated using:

$$a = \frac{V_{out,FS}}{V_{in,FS}} \qquad [V] \tag{5.3}$$

and linear PA amplitude is found by:

$$V_{out}(linear) = aV_{in} \qquad [V] \tag{5.4}$$

in this way, the linear amplifier's output amplitude is determined at each back-off (input amplitude) using equation 5.4. AM-AM conversion of the power amplifier i.e., the deviation from the ideal linear gain, is then the absolute difference between amplifier's actual output amplitude and the linear calculated amplitude multiplied by 100%.

$$AM - AM\ conversion = \frac{|V_{out}(linear) - V_{out}(actual)|}{V_{out}(linear)} \cdot 100 \qquad [\%] \tag{5.5}$$

On the other hand, AM-PM is determined by finding the phase error Φ_E referenced to full-scale, see equation 5.7. This can be calculated by taking the difference between input and output phase (ϕ_{diff}) of the amplifier at each back-off, equation 5.6, and then subtract this quantity from full-scale case.

$$\phi_{diff} = \phi_{out} - \phi_{in} \qquad [^\circ] \tag{5.6}$$

$$\phi_E = \phi_{diff} - \phi_{diff(FS)} \qquad [^\circ] \tag{5.7}$$

In the next section, amplitudes of the signal are referenced to the power back-off values by calculating them using the equation:

$$BO = P_n - P_{FS} \qquad [dB] \tag{5.8}$$

5.3 Origins of Distortion in Digital PAs

Contrary to analog power amplifiers, signal amplitude does not play a major role in digital PA distortion since amplitude is discretized and has only two states. In contrast, non-ideal switching (i.e., changes in the waveform shape) is the factor that counts here. This non-ideality is the result of different error sources: limited resolution of the modulator, delays (timing errors) added by driver and final stage, finite switching rate. In our case, we are dealing with simple input signals generated by software using a pattern generator so that the input signal is almost ideal: this allows excluding modulator nonlinearities, so that we are left with circuit- induced distortions only. This can be the delay of a pulse, which will cause a phase error in the output signal, or the deviation of a pulse shape from its ideal rectangular shape, which will change its spectral contents and thus may affect the resulting analog signal amplitude. If the time constants for ON and OFF switching are different, the pulse width is corrupted. A particular demanding case is very short pulses. If pulse width approaches the order of the switching times of the circuit, the resulting output signal is no longer a pulse and may be absorbed by the PA completely.

This is to illustrate the various non-idealities in a switching circuit and its influence on the output signal. The resulting distortion, however, depends on the way how the signal information is encoded in the pulse sequence. Hence, it is not possible to study distortion for a certain class-S switching PA in general; the results always refer to a certain modulation scheme. In this work, three modulation types are used: Pulse Width Modulation (PWM) with varying width of the pulse (PWM-C) but constant repetition rate, PWM with constant pulse width but varying the time between two pulses (PWM-V), and Band-Pass Delta Sigma modulation (BP-DSM).

The investigations are restricted to the quasi-static case, i.e., the encoded signal is a continuous-wave tone. Varying its amplitude and monitoring amplitude and phase of the resulting output signal yield the AM-AM and AM-PM curves, respectively. The quasi-static regime is helpful in identifying the main effects and the underlying mechanisms.

5.4 AM-AM and AM-PM Conversion

In the first step, the class-S PA conversion caused by amplitude (AM-AM) and that caused by phase (AM-PM) have been analyzed in simulation using Advanced Design System (ADS). AM-AM/ AM-PM conversion, output power, and efficiency are observed at each stage to see which part of the complete circuit contributes to the highest distortion. Then the other parts are added successively. Two versions of class-S circuits have been investigated, one is a single ended driver topology where the differential pair is source-fed with fixed current source, the same circuit as that used in chapter 3, see Fig. 3.3. This circuit was the first version of the driver circuit and is used only to study the major distortion source in the complete class-S demonstrator.

The other topology is with a differential pair which is fed by a fixed voltage source. This is similar to the version which is used in the measurements later on, but with two RF inputs.

Different input signals are used to drive the power amplifier:

- Pulse Width Modulated signal with two forms of switching events [17]
  - Varying the width of the pulse, with fixed repetition rate
  - Varying the time interval between pulses with constant width of the pulse
- BP-DSM Signal

5.4.1 Class-S Topology With Single Input Driver

As mentioned earlier, the circuit used in this analysis is the version given in the design of output network which is presented in chapter 3. Final stage transistor's size is 1 mm GaN (4x250 µm), while the differential pair and the pre-amplifier have 500 µm transistor's size (4x125 µm) each. A prior check is made to examine how transient and harmonic balance simulation agree. It shows a very good match between the two. The initial study is performed using harmonic balance simulation, just to save time which is one of the drawbacks of transient simulation. The complete circuit, which will be used in the measurement, is simulated by transient simulation at the end.

A PWM signal with constant repetition period T and varying width t_w (PWM-C) is applied. Fig. 5.2 illustrates the basic principle. In this kind of modulation, amplitude information is encoded in the pulse width, which decreases with amplitude. An input signal with different peak-peak $V_{P\text{-}P}$ amplitudes is used at the input. This is because we study the distortion at one stage only (final stage), two-stages (differential plus final stages), and three-stages (pre-amplifier, differential, and final stages). Therefore we applied the required peak-peak potential ($V_{P\text{-}P}$) to drive that circuit.

In the beginning, only the final stage shown in Fig. 5.3 is simulated. The upper final stage is driven with a square wave signal of a value between (V_{DD}+1) and -10 V. This lower negative voltage is needed to ensure that the amplifier switches OFF properly since it has a floating ground. The lower transistor has a gate voltage between 1V and -10 V which is enough due to the fixed ground at its source node. Drain voltage V_{DD} is chosen to be 40 V and an ideal filter is inserted at the output. An optimum impedance of 40 Ω is chosen as a load and inserted directly without any matching network to provide an ideal environment for the power amplifier.

The fundamental signal is extracted out of the broadband signal (modulated signal) by applying Fast Fourier Transformation (FFT) in ADS software, which em-

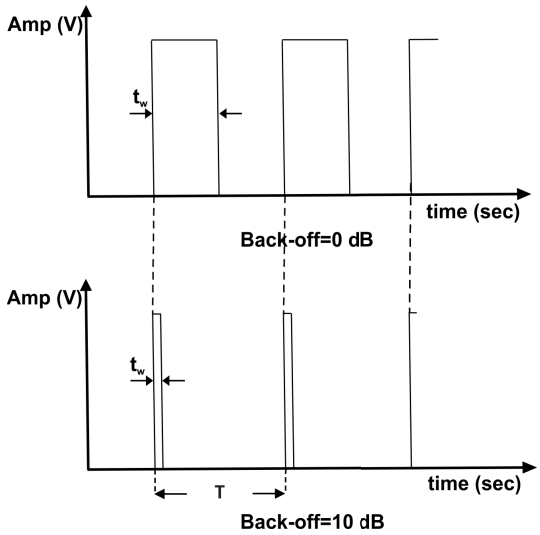

Fig. 5.2: Pulse-width modulated signal with constant repetition period and varying width for two encoded input signal amplitudes: 0 dB and 10 dB back-off

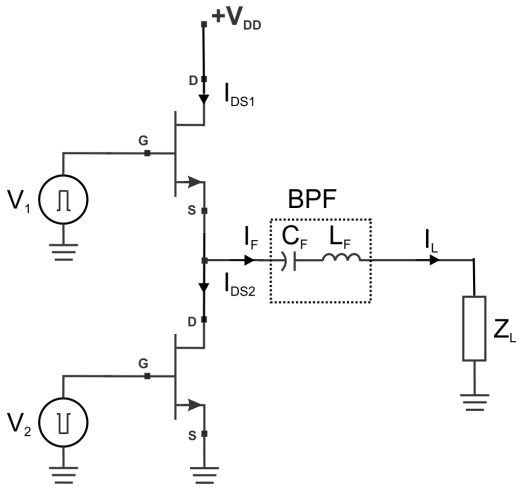

Fig. 5.3: Final stage voltage mode class-S

ulates an ideal bandpass filter.

Initial investigations were made observing input/output amplitude relationship as input amplitude (power back-off) changes. In Fig. 5.6, it can be seen that the input/output amplitude graph for the final stage only has an almost linear response, red line, except at very small amplitudes. The deviation from the linear slope which is calculated using equation 5.5 and presented in Fig. 5.7 has very

small value that increases as the input amplitude reduces. At 10.3 V input amplitude which corresponds to a back-off of around 10 dB, AM-AM conversion is equal to 2.8% which is still below 5%. It increases as the amplitude or the width of the pulse tw reduces further and reaches 63% at 43 dB back-off (input amplitude= 0.229V, t_w=2.5 psec).

AM-PM has been analyzed as well. The phase error ϕ_E is almost linear and remains around 0° for almost all amplitudes as it is shown in Fig. 5.8. It has a maximum value of 1.4° at 43 dB back-off. The single stage case exhibits no voltage amplification which is not a necessity for power amplifiers.

As a second step, a driver was added to the final stage, using a differential pair with a single input, as it is displayed in Fig. 5.4. Input swings have been chosen so that the final stage gate-source voltage V_{GS} has the required value for proper switching (V_{GS} ON > 0V, V_{GS} OFF⩽-3V. The same input amplitudes (back-offs) have been applied and again the input/output amplitudes as well as conversion and phase error have been studied. A dramatic jump in AM-AM/ AM-PM conversion can be observed .

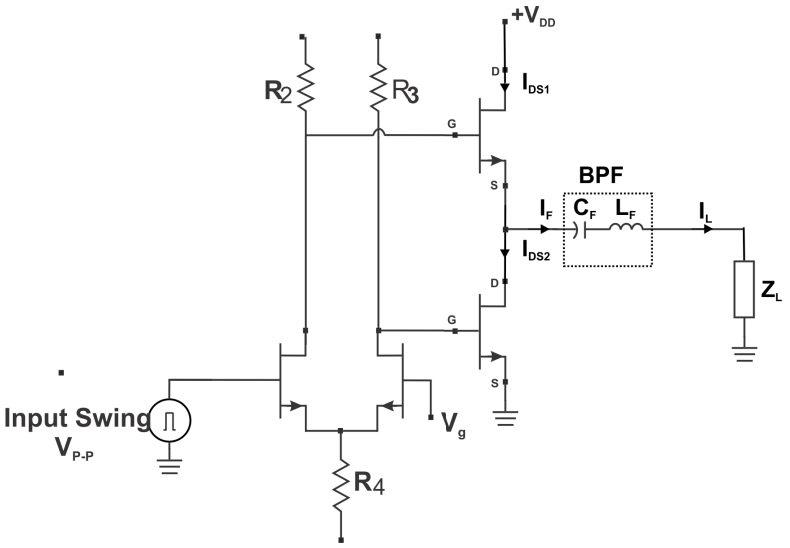

Fig. 5.4: Two-stages voltage mode class-S

As it is presented in Fig. 5.6, the relationship is no longer linear in the 0...10 dB back-off range. Output amplitude, see Fig. 5.7 deviates strongly from the linear response of the amplifier. At around 15 dB back-off, AM-AM conversion reaches 93% and continues to worsen for lower amplitudes. The same behaviour can be observed in AM-PM (Φ_E) which exceeds 5° (maximum acceptable phase distortion in OFDM transmitters [29]) already very early at 2.9 dB (6.1 V) back-off.

Finally, a pre-amplifier is added and the complete demonstrator of Fig. 5.5 is simulated for AM-AM/AM-PM conversion analysis. It is obvious that there is no big difference between the 2-stages case and that of 3-stages. The input/output amplitude graph shows similar deviations from linear pre-calculated amplifier slope as the 2-stages case.

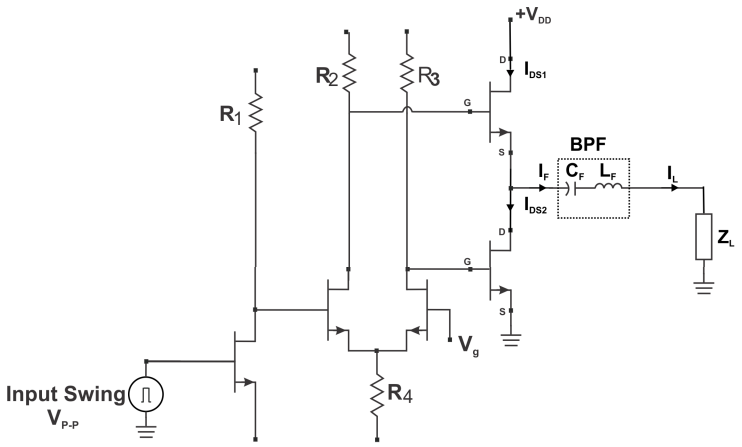

Fig. 5.5: Three-stages voltage mode class-S with single RF input

AM-AM conversion at 15 dB back-off is 99% and phase error is 5° at 2.9 dB back-off (same as 2-stages case). Out of that, one can conclude that adding the preamplifier stage does not do much harm to the PA from the distortion point of view. The differential pair is the stage that contributes the largest part of AM-AM/AM-PM conversion. Hence, in the next analyses , the two-stages case (final stage plus first driver) is considered for class-S PA distortion investigation.

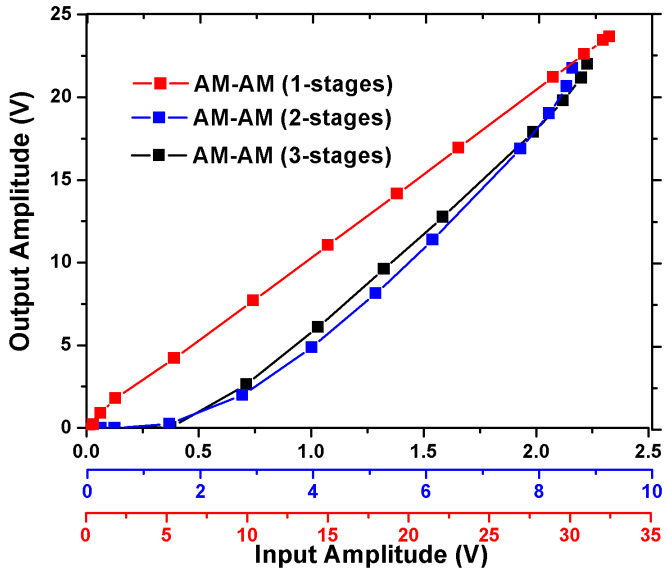

Fig. 5.6: Input/output amplitude response of VMCS PA for 1-3 stages with PWM (varying pulse width) excitation signal

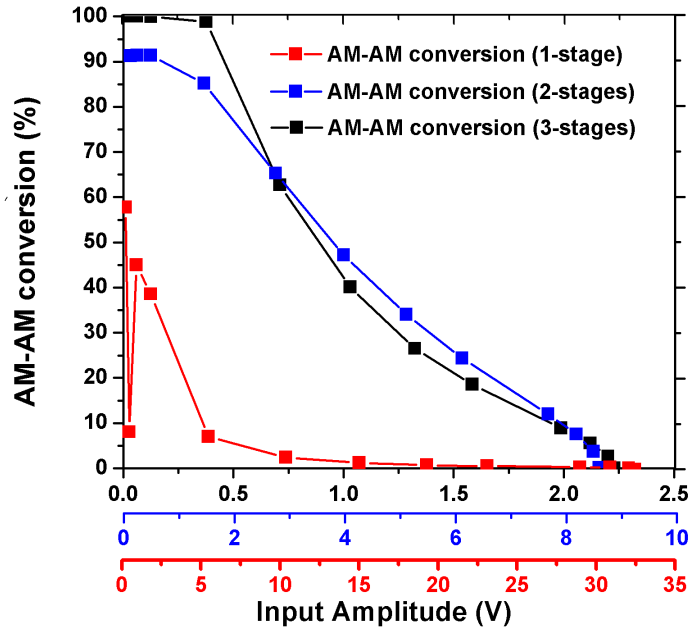

Fig. 5.7: Quasi-static AM-AM conversion comparison of VMCS PA for 1-3 stages with PWM (varying pulse width) excitation signal

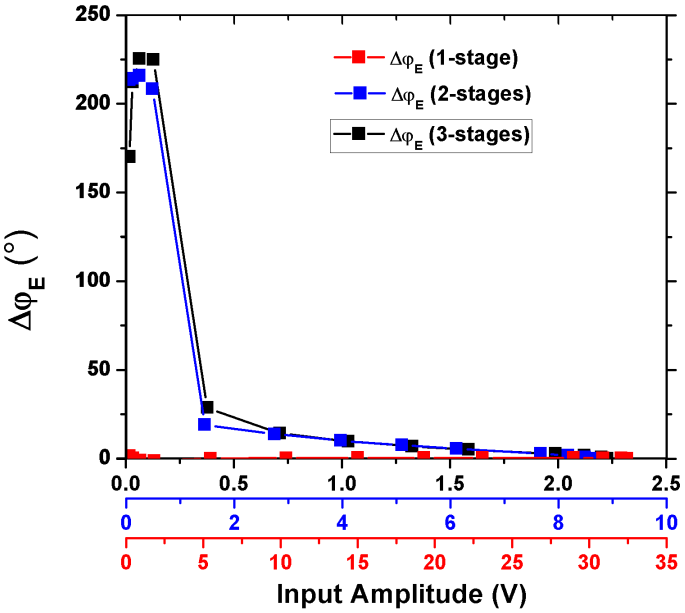

Fig. 5.8: Phase error $\Delta\Phi_E$ comparison of VMCS PA for 1-3 stages with PWM (varying pulse width) excitation signal

5.4.2 Class-S Topology With Dual Input Driver

In this study, the circuit which is used is the one shown in Fig. 5.9 which is similar to the one shown in Fig. 5.4 but with two RF inputs at the differential pair instead of only one. It has two stages: final stage and the differential pair. Initial simulations were made to decide which source to be used to feed the differential pair source node, current or voltage source.

Class-S behaviour has been observed at Pulse-Width Modulated signal (PWM) with varying pulse width. Different back-offs have been recorded: 0 dB (full-scale), 6.7 dB, 9.9 dB, 15.4 dB, and 37 dB. Fig. 5.10 presents the resulting deviations from linear response. The circuit with voltage source exhibits better AM-AM performance than the current source version, except at the highest back-off. The same behaviour can be noticed in the phase error Φ_E graph shown in Fig. 5.10. At all back-offs, error in phase does not exceed 5° for the circuit with voltage source while it is 5.5° at 6.7 dB, 18.5° at 37 dB for the current source version. Adding the current

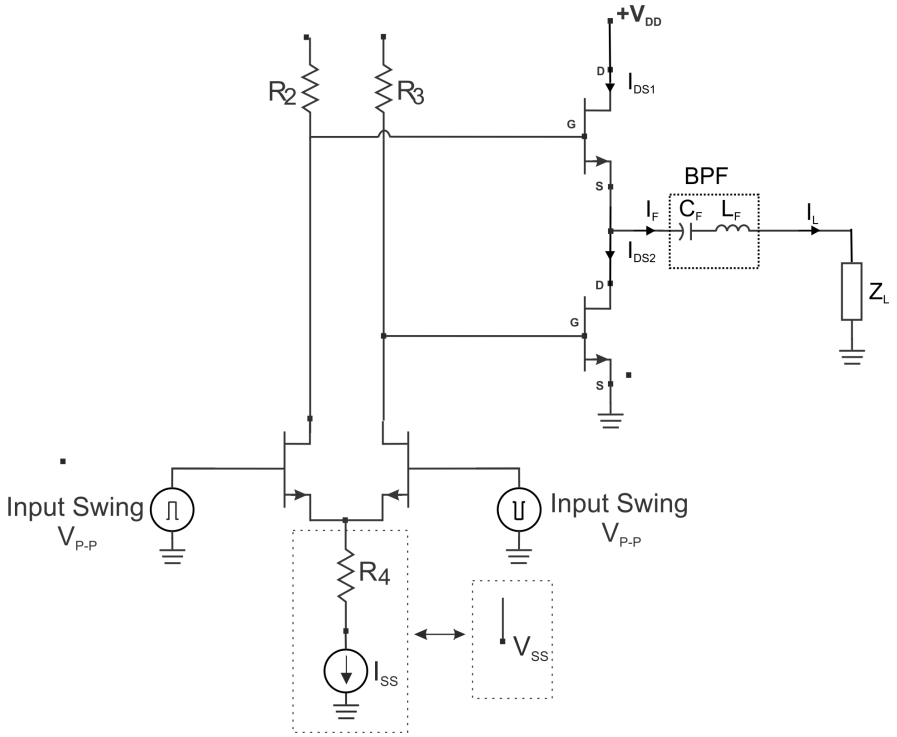

Fig. 5.9: Two-stages voltage mode class-S with dual RF inputs under PWM (varying pulse width) excitation

source with its resistor did affect the circuit negatively from the distortion point of view. Current sources are more complicated and less efficient than the voltage ones. Plus, resistors in general increase the rise time of the signal at the source point ($\tau = RC$ where C is the source capacitance) [30] and this shapes the gate-source voltage V_{GS} signal in no exact square-wave profile (distorted), which in turn means more AM-AM and AM-PM distortion of the VMCS PA. Therefore, the circuit with voltage source is the one which is considered for the next investigations. The distortion is presented in the following.

5.4.3 AM-AM/AM-PM Conversion of Dual-Input Two-Stages Class-S driven by PWM signal

As it is already presented in section 2.2.1.2, the PWM signal is widely used to drive switching amplifiers, especially class-D PAs. In this section, the signal is used

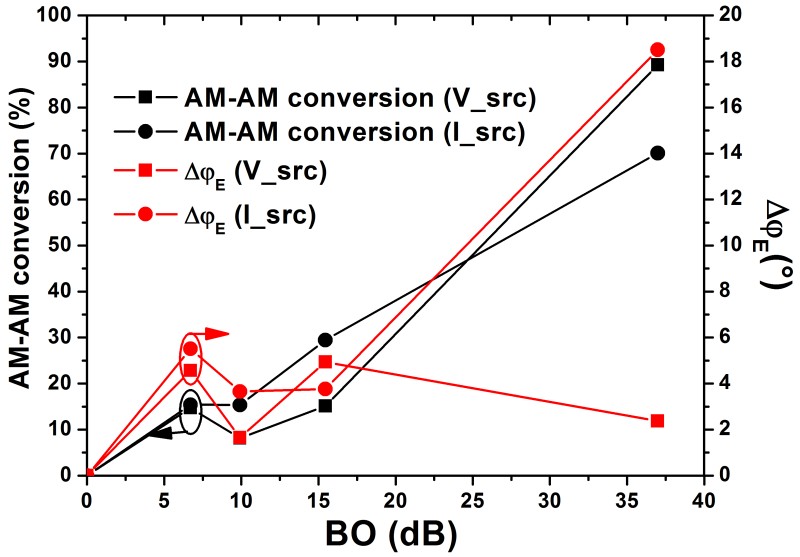

Fig. 5.10: AM-AM conversion and phase error $\Delta\Phi_E$ for two-stages class-S with voltage and current source under PWM (varying pulse width) excitation

in two forms: one with constant period T but varying pulse width t_w and the other with a constant pulse width and varying period T. The main target is to find the optimum differential driver resistors (R_2 and R_3) and inductors (which inserted in series with the resistors) constellation that produces a compromise between linearity and efficiency of the class-S power amplifier. Introducing inductors leads to a lower required applied voltage for switching the final stage properly. Thus, decreasing the DC current consumption which lowers the dissipated DC power . Worth mentioning that introducing inductors limits the bandwidth by reducing the cut-off frequency to a lower value.

The approach is performed by fixing one resistor and optimizing the other. R_2 and R_3 initial values were taken differently for each modulation scheme.

5.4.3.1 Pulse Width Modulation with Constant Repetition Rate (PWM-C)

For the first case (fixed T and varying t_w) and for each value of R_2, R_3 has been tuned. Voltages and currents are observed at each stage to ensure the required switching conditions. AM-AM conversion, phase error, drain efficiency and power

are presented in figures 5.11 and 5.12. When talking about distortion in the amplitude signal (AM-AM), one should consider the following points:

- As the resistor value increases, the rise-fall time of the signal (τ=RC) increases. This leads to a deformation of the signal shape and consequently the signal does not reach the required voltage needed for complete switching ON/OFF. Slow switching brings the two transistor to be ON at the same time and more overlapping occurs between voltage and current which causes a lower efficiency.

- When the resistor value decreases, switching time improves (less rise-fall time τ). But, the current consumption increases which lead to a lower efficiency. Another aspect to be considered is that I_{dmax} of the driver stage cannot pull down its drain voltage properly. As a result, the respective final-stage transistor does not switch OFF fully.

- Any increase in the gate current (lower final stage transistor as an example) will be accompanied by some current from the gate to the source of the other transistor (upper final stage) and a voltage drop will be generated in that transistor (which theoretically in its OFF stage) in the opposite direction from its V_{DS}, so that the transistor does not reach the required voltage level (V_{DD}) for the OFF state and will not switch OFF properly

- The output voltage before the filter V_F decreases in amplitude with lower resistor values because the driver cannot switch OFF final stage transistor properly (as mentioned previously) and thus the two output voltage levels for ON and OFF degrade, i.e., ON decreases and OFF increases

All those factors play a significant role in the AM-AM and AM-PM conversion. Amplitude conversion depends strongly on the shape and amplitude of the amplified signal compared to the driven input signal. Phase conversion is affected by the position of the sinusoidal output signal with regard to the original position of the sinusoidal input signal.

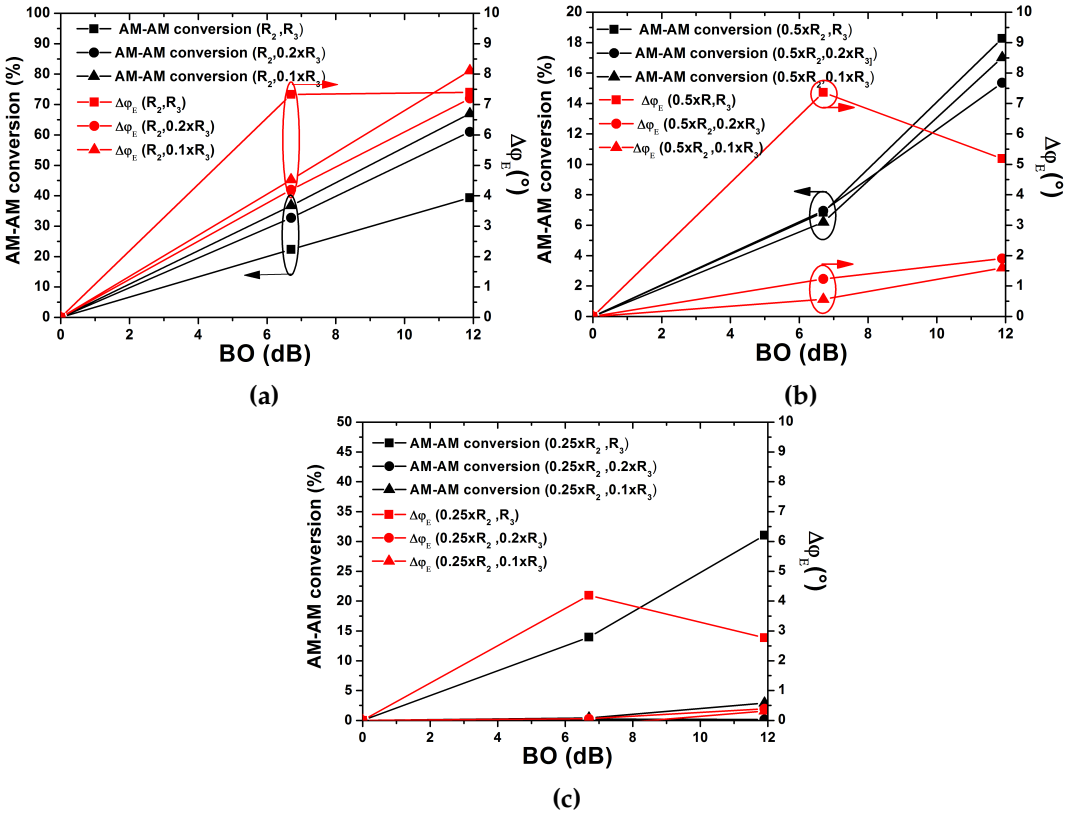

Fig. 5.11: Quasi-static AM-AM conversion and phase error $\Delta\Phi_E$ of PWM-C input signal for various driver resistors constellation (R_2=200 Ω, R_3=50 Ω)

When observing Fig. 5.11, one can conclude that decreasing upper driver drain resistor R_2 (see R_2 in Fig. 5.11 for the three graphs) improves the amplitude conversion which is taken referenced to full-scale or 0 dB case. R_2/ R_3 are taken equal to 200 Ω/ 50 Ω. Best case is seen to be with the pair of 0.25xR_2,0.2xR_3 where amplitude conversion is at lowest level (almost zero).

Changing lower driver resistor R_3 does not cause a significant improvement in the AM-AM conversion in most cases as it is seen in the same figure. Only in graph (c) and at 12 dB for example, it reduced AM-AM conversion from 31% for 0.25xR_2,R_3 to 0% for 0.25xR_2,0.2xR_3 resistor's pair.

The phase conversion for the same resistor's constellation is found to be at min-

imum at 0.25xR_2,0.2xR_3 and 0.25xR_2,0.1xR_3 pairs, where phase error equals almost 0° .

On the other hand, all pairs with R_3=1 show almost the worst phase error. In our opinion, the impact comes from the fact that output signal V_F (before the filter) shifts its position as the rise and fall time changes. That is, as the resistor gets higher in value, τ (τ=RC) gets higher too. In this regard, the pairs 0.2xR_3 and 0.1xR_3 produce lower conversion since the output voltage V_F has less τ compared to the case with R_3=1.

The second part of the investigation is the output power and drain efficiency of the circuit. Drain efficiency (final stage only) depends on the loss that occurs during switching as well as the current in ON-state, i.e., output power. In Fig. 5.12, values of power and efficiency are the best for resistor's pairs of R_3=1. It shows the impact of lowering the resistor's value which leads to a lower efficiency as R_3 gets lower in value.

The same principle applies for upper final stage driver's drain resistor R_2. As R_2 increases, better output power could be obtained until a certain value then the impact of rise-fall time introduced. Optimum output power is found for the pair 0.5xR_2, R_3. Drain efficiency, on the other hand, is best found at R_2=1. The other two values, 0.5xR_2 and 0.25xR_2, exhibit smaller input gate swing and consequently lower efficiency.

5.4.3.2 Pulse Width Modulation with Varying Time Period (PWM-V)

In this type of modulation, the time between two pulses is the quantity which changes while the pulse width remains fixed, Fig. 5.13 explains the principle providing the pulse sequences for cw tones with 0 dB, 6 dB, and 12 dB back-off. In view of the results of the previous subsection, this property is clearly an advantage because it avoids short pulses. Again R_2,R_3 are taken to be equal to 200 Ω/ 50Ω.

As a first step, the study investigates the digital power amplifier's response, re-

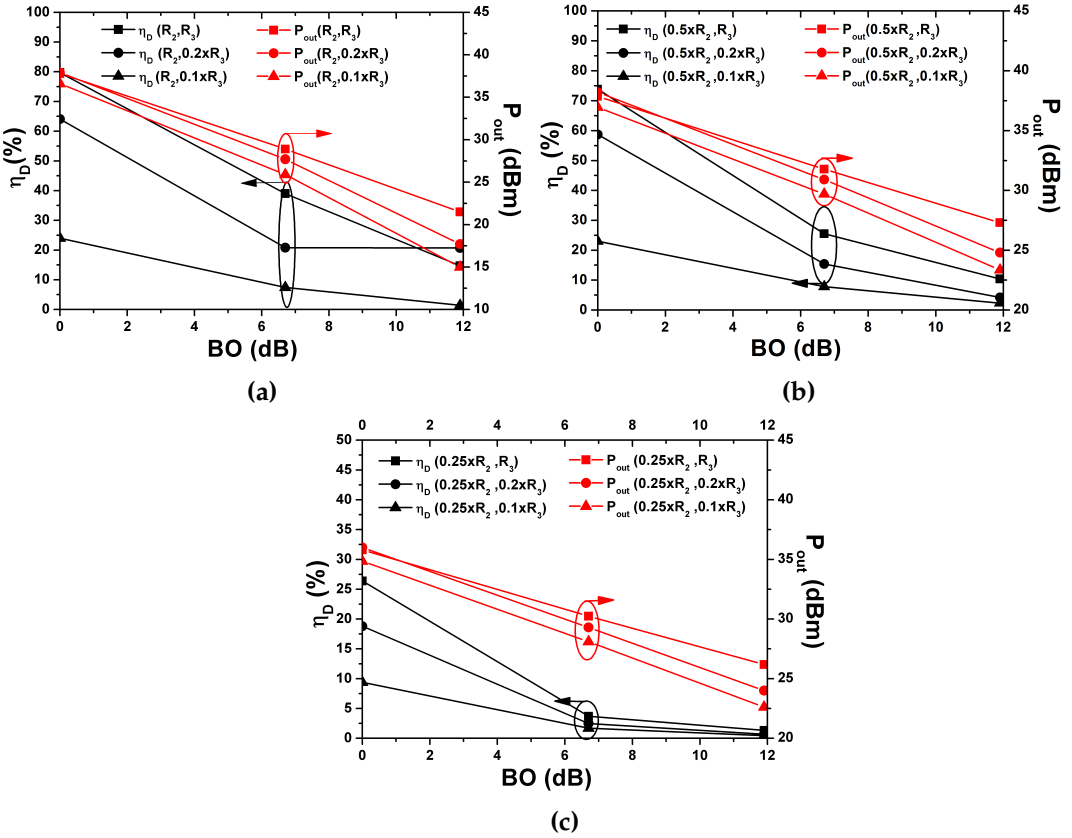

Fig. 5.12: Drain efficiency and output power of PWM-C signal for various driver resistors constellation (R_2=200 Ω, R_3=50 Ω)

garding conversion, with different resistor pairs, as already explained with PWM-C. It is broadened afterwards to take the impact of adding an inductor in the differential pair drain path (in series with the resistor), which is a simple measure to improve switching speed.

Conversion was found at its lowest value with the pair R_2,R_3 (200Ω/ 50 Ω). As the case in subsection 5.4.3.1, increasing the resistor value does increase the AM-AM conversion, see Fig. 5.14. For doubling R_2, conversion increases by four times, from 2% to 8% at 40 dB back-off. Also, by increasing R_3 1.5 times, conversion becomes two times more, that is from 2% to 4%.

Phase error was found worse too, as resistor increases in value. Phase error

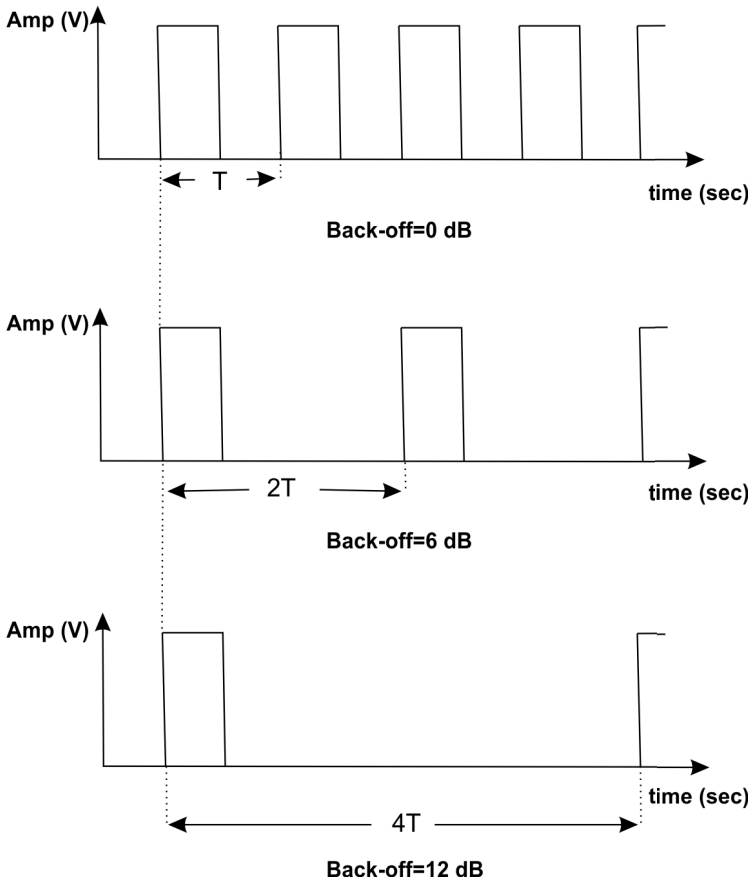

Fig. 5.13: Pulse-width modulated signal with varying time between the pulses and constant pulse width for 0 dB, 6 dB, and 12 dB back-off.

remains less than 5° which is within the allowed range (the maximum acceptable AM-PM distortion in modern OFDM transmitters [28, 29]).

Output power and drain efficiency are presented in Fig. 5.15. While there is no obvious difference in output power for the different resistors' pair, drain efficiency η_D tends to increase for the higher values of drain resistor ($1.5xR_2$,$1.5xR_3$ and $2xR_2$,R_3). That is due to the limited ON-resistance of the drivers which increases the OFF state gate-source voltage V_{gs} of the final stage.

Considering optimum resistor values, $R_{2,3}$ is now connected with an inductor in series L (nH). Adding an inductor in the path of the final stage gate signal enhances

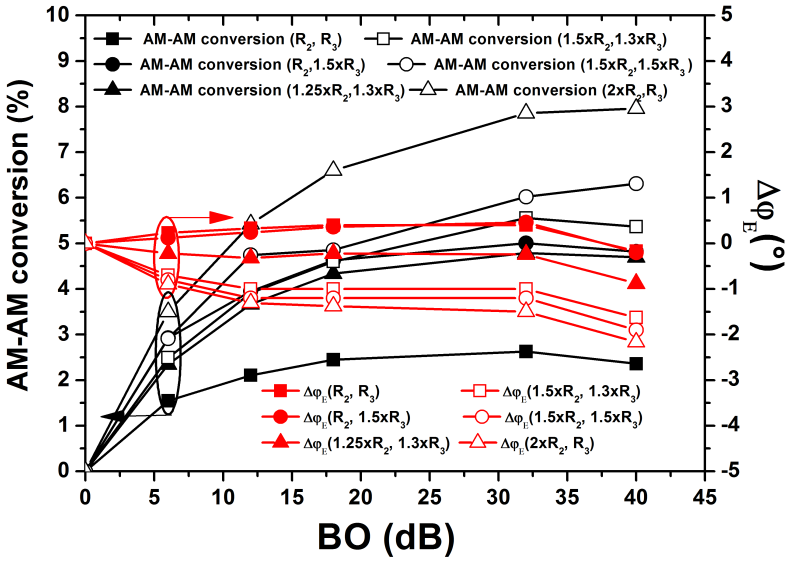

Fig. 5.14: Quasi-static AM-AM conversion and phase error $\Delta\Phi_E$ of PWM-V input signal for various driver resistors constellation (R_2=200 Ω, R_3=50 Ω)

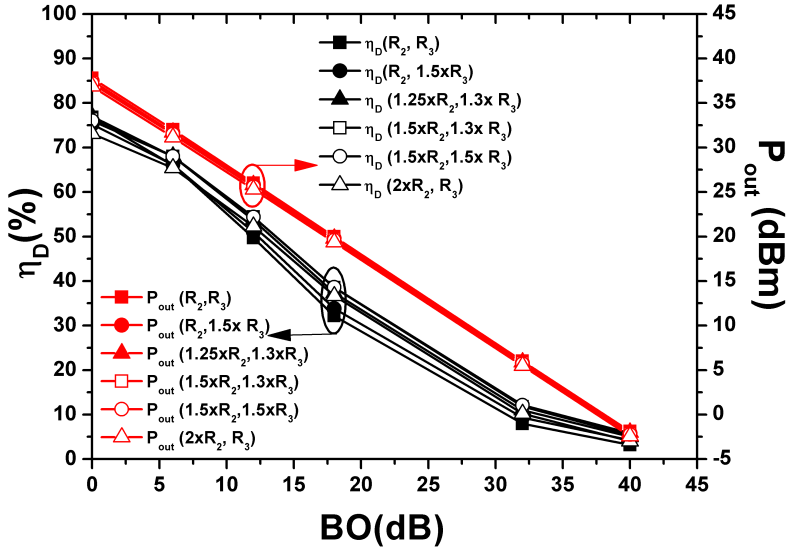

Fig. 5.15: Drain efficiency and output power of PWM-V signal for various driver resistors constellation (R_2=200 Ω, R_3=50 Ω)

the shape of the driving signal as is explained in Fig. 5.16.

The current waveform shape is transformed from semi-square wave to semi triangle due to the charging and discharging of the inductor, Fig. 5.17, (energy stor-

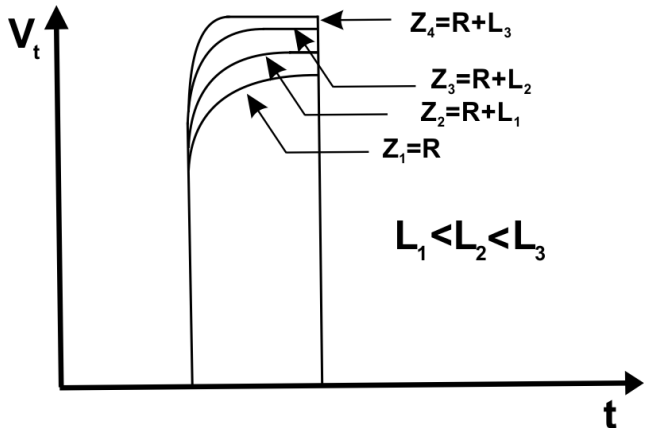

Fig. 5.16: Final stage gate input signal with inductor impact on amplitude and shape for the short pulse case

age element) in the ON/OFF states of the differential pair, as the inductor general equation explains:

$$V_L = L \cdot \frac{di}{dt} \qquad [V] \tag{5.9}$$

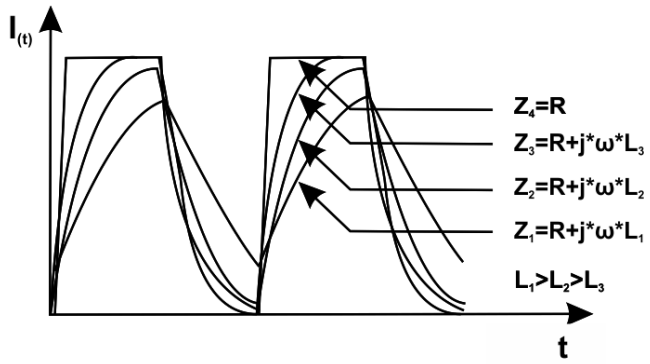

Fig. 5.17: Differential amplifier drain current with inductor impact on amplitude and shape

In this work, focus is directed to the AM-AM/AM-PM conversion when inserting an inductor. Details on PAE improvement using inductors are described in [31].

The value of the inductor is increased in such a way that it is appropriate to the value of the resistor it is connected to. In other words, the value is selected so that

the influence of adding the inductor would not be surpassed by the value of the resistor. R_2/ R_3 pair is now taken to be 300 Ω/ 50 Ω, L_1, L_2 is equal to 25 nH and 50 nH. Amplitude conversion is presented in Fig. 5.18. Conversion was found at minimum for R_2+j*ω*L_2 and phase conversion as well. In all cases, AM-AM and AM-PM conversion remain within the limit, 5% and 5° respectively.

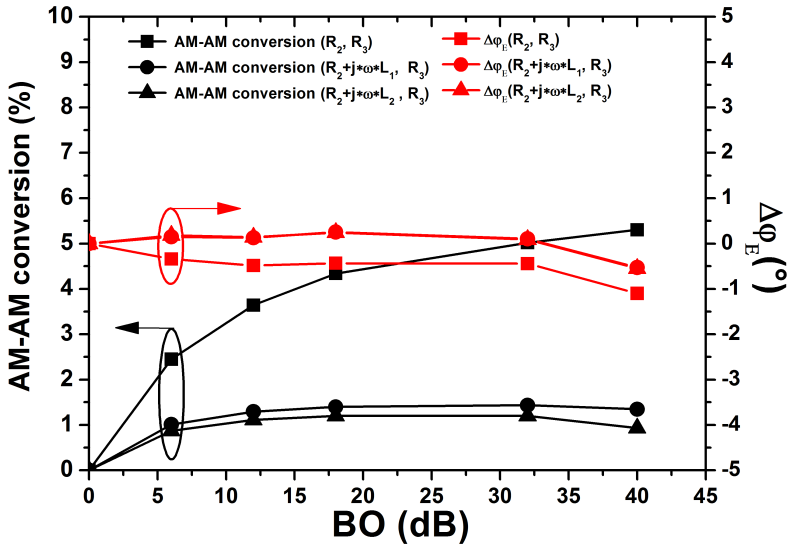

Fig. 5.18: Quasi-static AM-AM conversion and phase error $\Delta\Phi_E$ of PWM-V input signal for different inductors connected in series with R_2 (R_2=300 Ω, R_3=50 Ω, L_1=25 nH, L_2=50 nH)

Fig. 5.19 shows the output power and efficiency response of the amplifier. Output power does not differ too much and drain efficiency exhibit slight improvement when adding inductor.

Similarly, now R_3 is connected with an inductor. Here, we prefer to tune R_2 as well to expand the area of finding the optimums. R_2/R_3 are taken to be 200Ω/ 75 Ω while L_1,L_2, and L_3 have the values of 5 nH, 25 nH and 50 nH respectively. Amplitude conversion is at its best level for the case of (R_2, R_3+j*ω*L_1), see Fig. 5.20. Phase error and efficiency seem to be optimum for all values. Output power is not affected, which is expected, by adding an inductor in the path of input final stage devices, refer to figures 5.20 5.21.

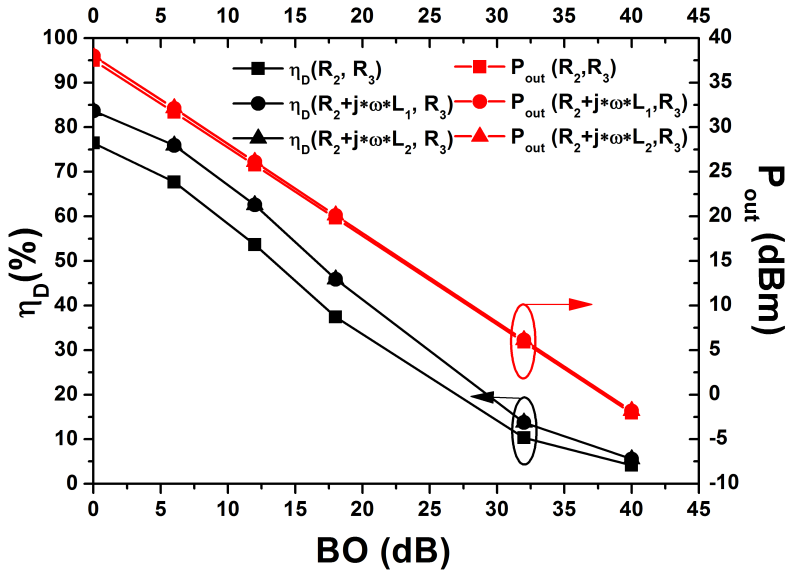

Fig. 5.19: Drain efficiency and output power of PWM-V input signal for different inductors connected in series with R_2 (R_2=300 Ω, R_3=50 Ω, L_1=25 nH, L_2=50 nH)

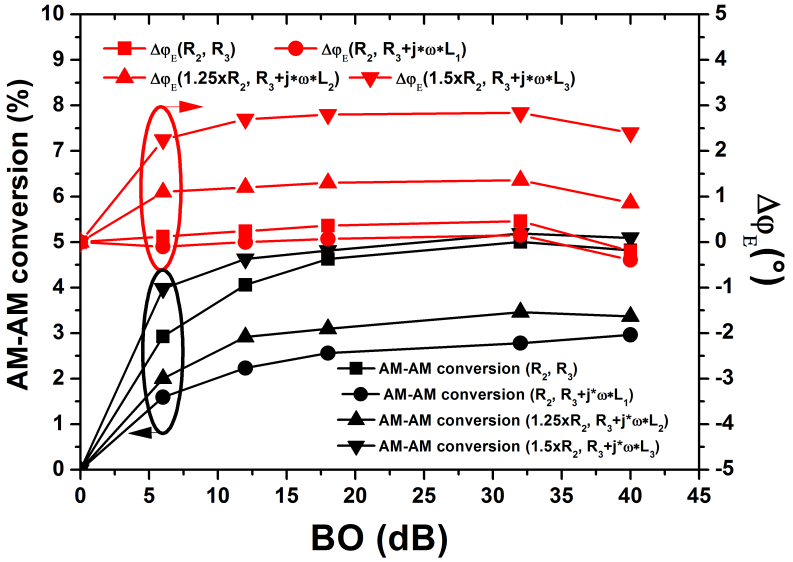

Fig. 5.20: Quasi-static AM-AM conversion and phase error $\Delta\Phi_E$ of PWM-V input signal for different inductors connected in series with R_3 (R_2=200 Ω, R_3=75 Ω, L_1=5 nH,L_2=25 nH, L_3=50 nH)

In a last step, both optimum inductors and resistor values (R_2, R_3 and L_1, and L_2) are used (R_2=300 Ω, R_3= 75 Ω, L_1= 50 nH, and L_2=5nH). Conversion, efficiency and

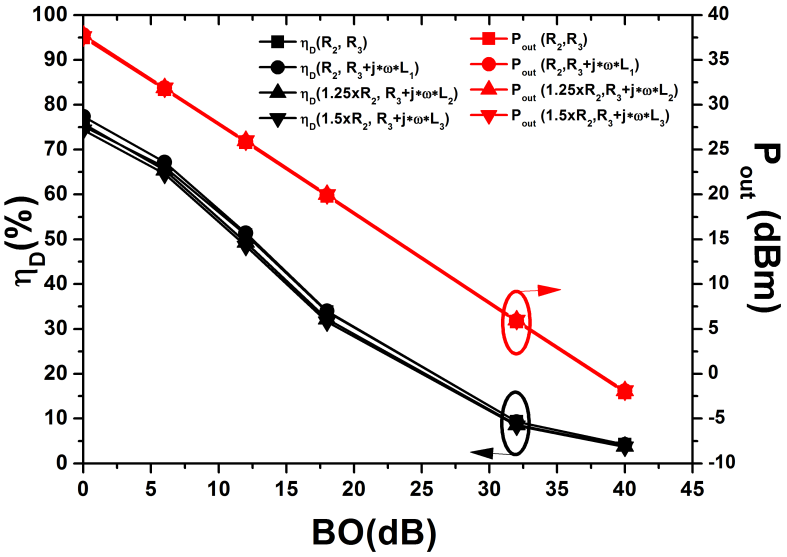

Fig. 5.21: Drain efficiency and output power of PWM-V input signal for different inductors connected in series with R_3 (R_2=200 Ω, R_3=75 Ω, L_1=5 nH,L_2=25 nH, L_3=50 nH)

output power for the two-stages digital PA, regarding PWM-V modulated signal are shown in figures 5.22 and 5.23..

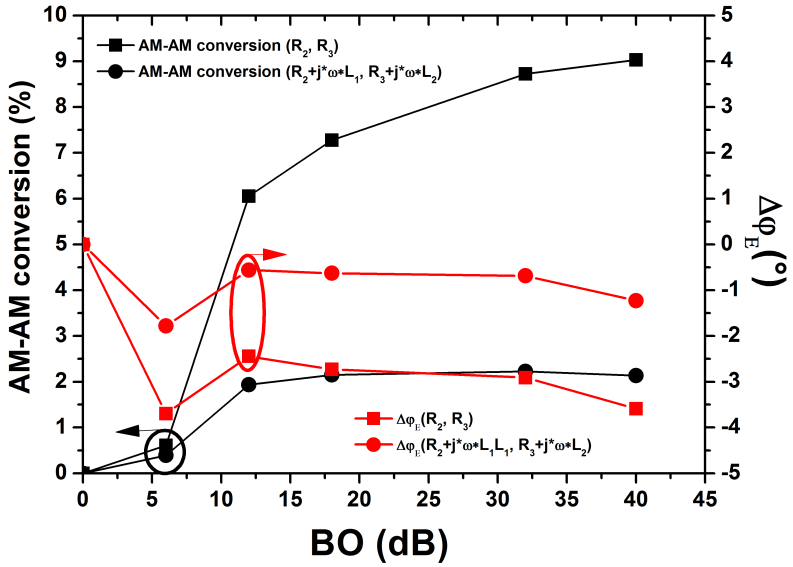

Fig. 5.22: Quasi-static AM-AM conversion and phase error $\Delta\Phi_E$ of PWM-V input signal for optimum resistor and inductor values (R_2=300 Ω, R_3=75 Ω, L_1=50 nH,L_2=5 nH)

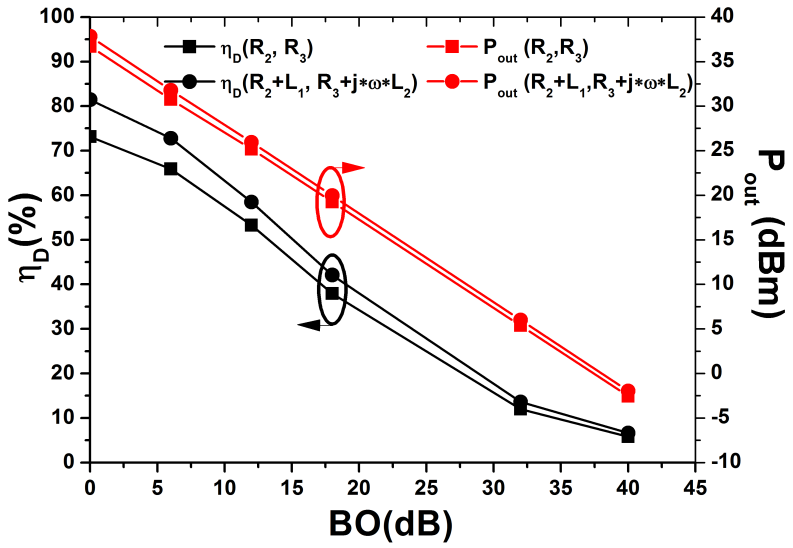

Fig. 5.23: Drain efficiency and output power of PWM-V input signal for optimum resistor and inductor values (R_2=300 Ω, R_3=75 Ω, L_1=50 nH,L_2=5 nH)

With respect to the AM-AM/ AM-PM conversion, it is clear that the circuit with inductors has less distortion, a maximum around 2% at 40 dB back-off and phase error is less than 2° for all back-off values considered.

Output power is 1 dB more for the version with inductors while efficiency is almost 7% more at full-scale and the difference decreases as BO increases.

5.4.3.3 Band-Pass Delta-Sigma Signal (BPDS)

BPDS signal is the third type of modulated signals which have been used to drive the two-stages digital power amplifier described in this work. The 180° phase difference input signals are realized digitally as a bit sequence, as was already explained in section 2.2.1.1. The goals of the investigations are the same as in the previous subsections, that is, studying distortions and finding the best compromise between amplitude/ phase conversion in terms of the second stage (differential pair) impedances.

Regarding AM-AM conversion, adjusting R_3 is investigated first. The best value for the drain resistor R_3 of the differential transistor that drives the lower final stage

device appears to be at (R_2,R_3) which are taken equal to 200 Ω/ 35 Ω, see Fig. 5.24, with 3% maximum conversion at 32 dB back-off. However, AM-PM conversion is within the limits for the first three pairs: (R_2,R_3), (R_2/1.43 x R_3), and (R_2/2.14 x R_3) until 32 dB and then, at 40 dB, it increases beyond 5° for all resistors' pairs. One can notice two influences: rise-fall time τ as R increases, and gate current increment as R decreases, refer to 5.4.3.1.

Drain efficiency and power are at their maximums for (R_2,R_3), (R_2/1.43 x R_3). The impact of τ is the dominant factor for the deterioration of power and efficiency, i.e., increasing τ leads to a non-perfect sharp signal edge which means less power and consequently less efficiency.

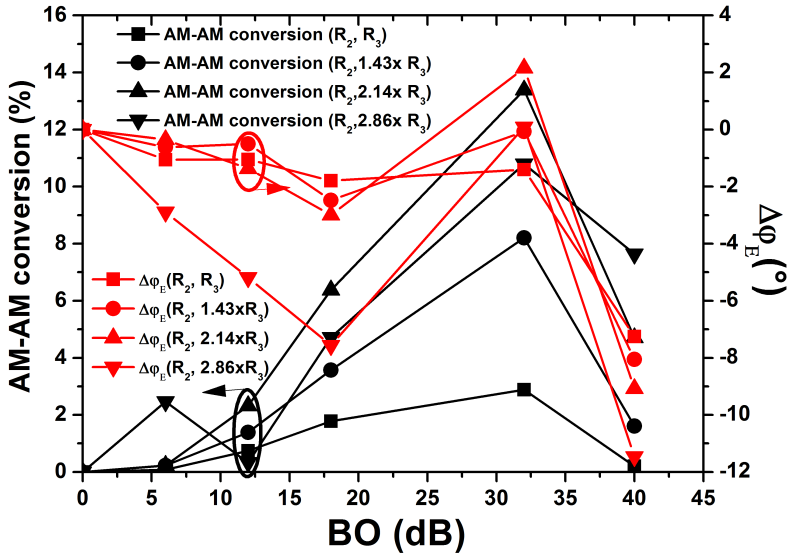

Fig. 5.24: Quasi-static AM-AM conversion and phase error $\Delta\Phi_E$ of BPDS input signal for various R_3 constellation (R_2=200 Ω, R_3=35 Ω)

Similarly, R_2 is optimized the same way. R_2/R_3 pair is now taken to be equal to 100 Ω/ 35 Ω. Best choice for AM-AM conversion is the pair of (2xR_2,R_3) with around 3% as a maximum at 32 dB back-off while that for AM-PM is found at (R_2,R_3) and (2 x R_2,R_3) although it exceeds 5° for the latter. Efficiency and power are optimum for (2 x R_2,R_3) of 57% and 34 dBm respectively.

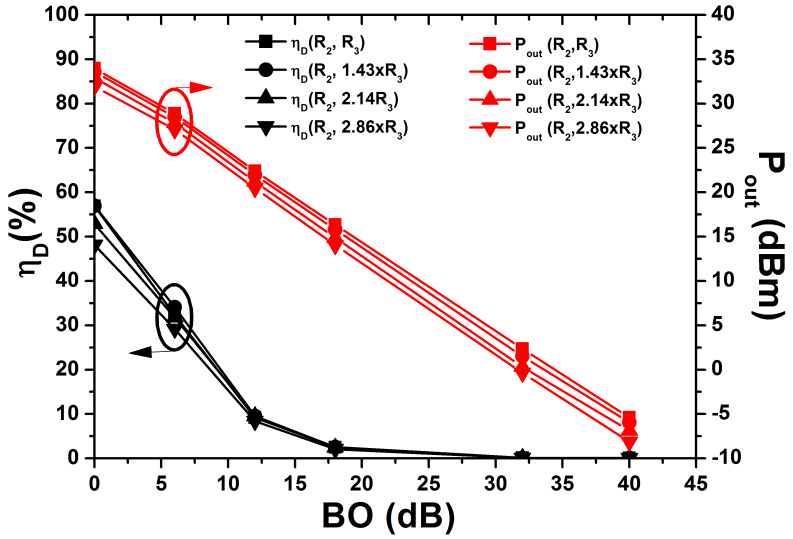

Fig. 5.25: Drain efficiency and output power of BPDS input signal for various R_3 constellation (R_2=200 Ω, R_3=35 Ω)

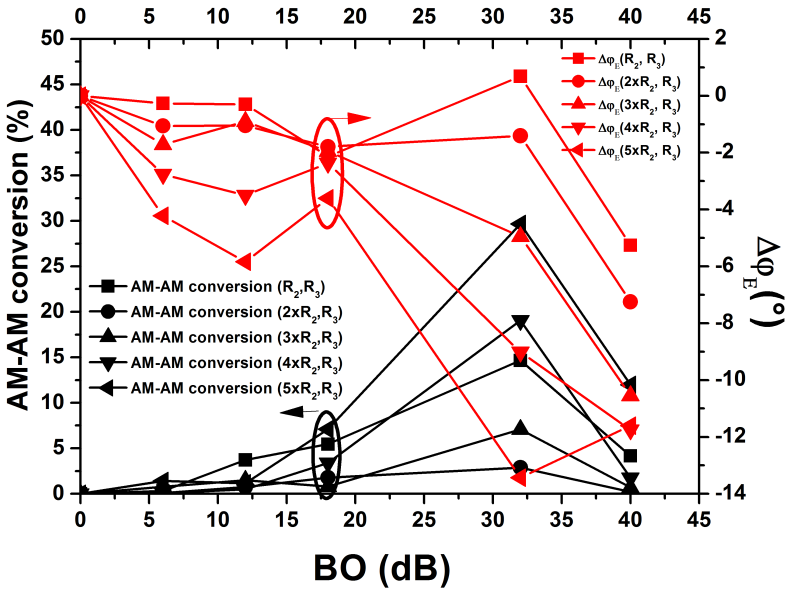

Fig. 5.26: Quasi-static AM-AM conversion and phase error $\Delta\Phi_E$ of BPDS input signal for various R_2 constellation (R_2=100 Ω, R_3=35 Ω)

For the case of adding an inductor to R_3, the influence is described in 5.4.3.2. In this case R_2/R_3 equal to 200 Ω/35 Ω and L_1 ,L_2 , and L_3 are 5nH, 25nH, and 50 nH respectively.

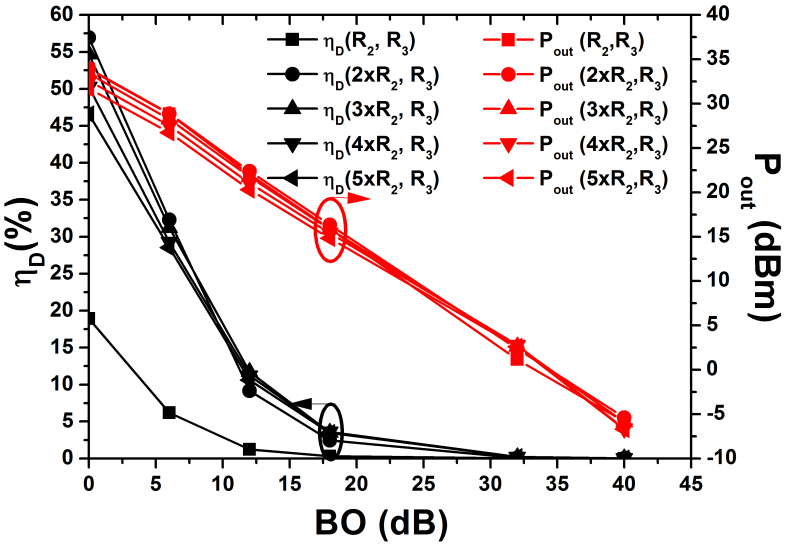

Fig. 5.27: Drain efficiency and output power of BPDS input signal for various R_2 constellation (R_2=100 Ω, R_3=35 Ω)

As it is displayed in Fig. 5.28, adding L_1 has the minimum amplitude conversion. The optimum impedance (R_3+j*ω*L_1) exhibits a maximum conversion of almost 1 % till 32 dB. For the extreme 40 dB case, it is about 6%.

Phase distortion is not that critical for all impedances up to 32 dB. All values are less than 5° which for modern OFDM transmitters are within the tolerated limit.

Output power and drain efficiency, Fig.5.29, are at their best values for the impedance R_3+j*ω*L_1 with 62% and 34 dBm each (FS).

For the R_2 branch, it seems that adding an inductor has a negative effect on the distortion, refer to Fig. 5.30. R_2/R_3 pair here is also equal to 200 Ω/ 35 Ω and L_1, L_2, and L_3 are equal to 5nH, 15nH and 25 nH. The inductor increases the upper edge of the input gate swing V_{g1} (Fig. 2.9) above V_{DD} value which means that V_{DS2} has a peak-peak amplitude between 0V and a value more than V_{DD}. In other words, V_{DS2} has partly a waveform glitch, as is explained in Fig. 5.31, that increases with inductor value and adds more distortion to the switching output signal V_{DS2}.

When talking about drain efficiency η_D, Fig. 5.32, the pair (R_2+j*ω*L_3, R_3) ex-

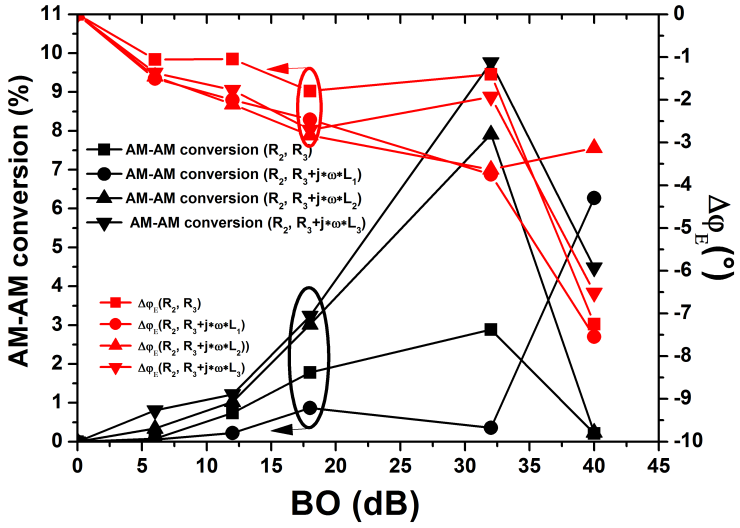

Fig. 5.28: Quasi-static AM-AM conversion and phase error $\Delta\Phi_E$ of BPDS input signal for various inductors connected in series with R_3 (R_2=200 Ω, R_3=35 Ω, L_1=5 nH, L_2=25 nH, L_3=50 nH)

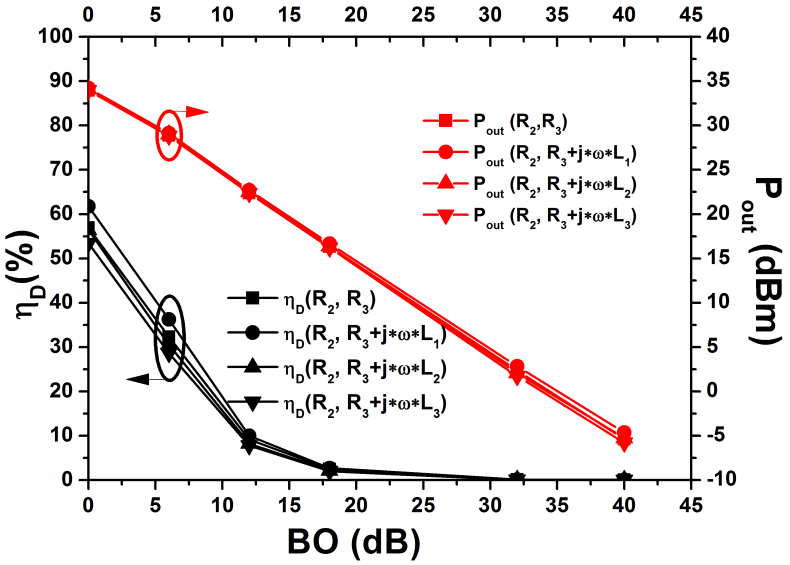

Fig. 5.29: Drain efficiency and output power of BPDS input signal for various inductor values connected in series with R_3 (R_2=200 Ω, R_3=35 Ω, L_1=5 nH, L_2=25 nH, L_3=50 nH)

hibits the best efficiency values over back-off while output power seems to be unchanged for all pairs. This improvement in efficiency comes from the fact that as

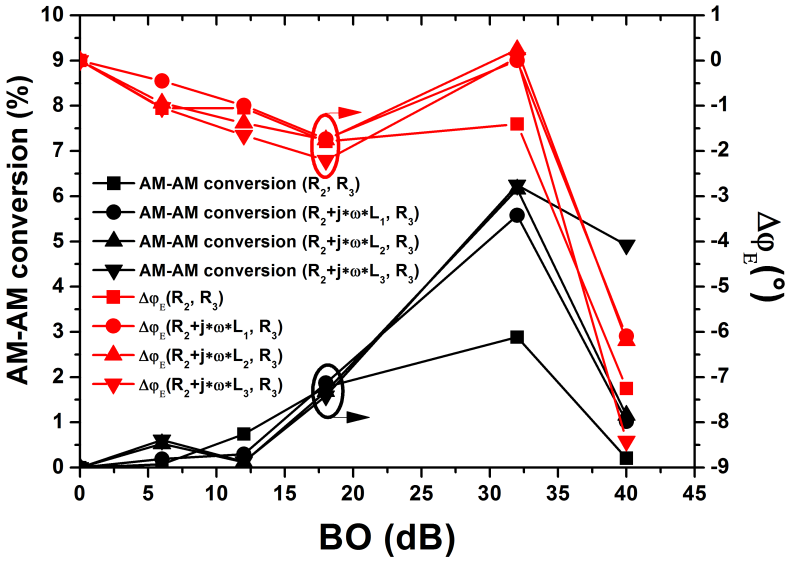

Fig. 5.30: Quasi-static AM-AM conversion and phase error $\Delta\Phi_E$ of BPDS input signal for various inductor values connected in series with R_2 (R_2=200 Ω, R_3=35 Ω, L_1=5 nH, L_2=15 nH, L_3=25 nH)

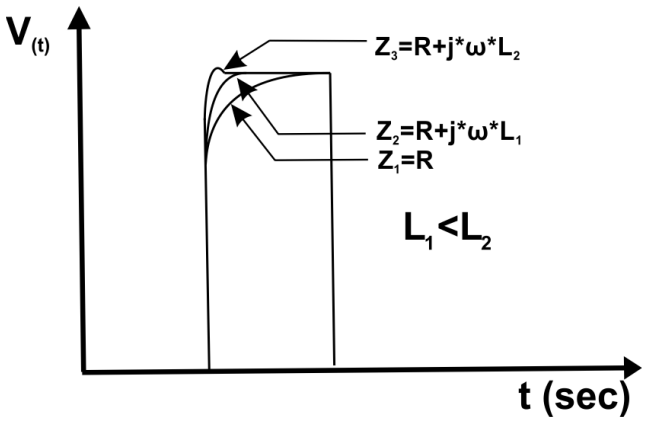

Fig. 5.31: Digital PA output voltage before the filter of BPDS input signal for various inductors connected in series with R

the inductor's value increases, the gate-source voltage V_{GS} of the final switching stage becomes more squared-wave and thus switching conditions are improved.

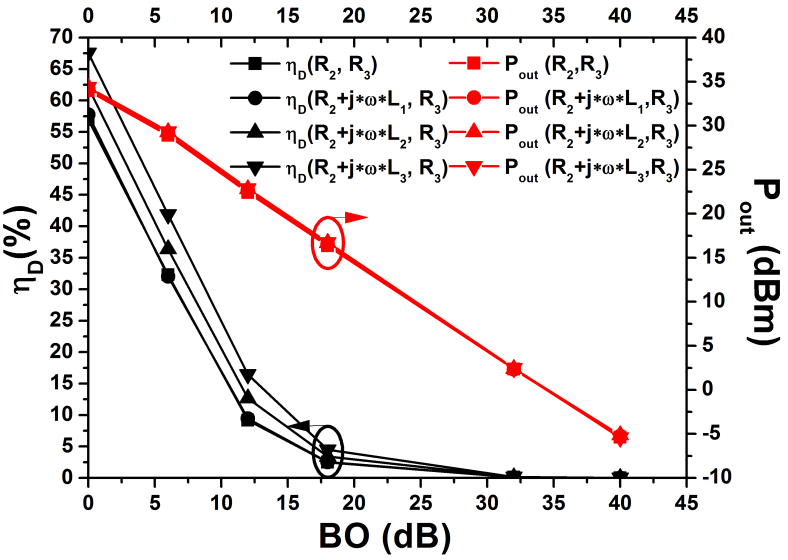

Fig. 5.32: Drain efficiency and output power of BPDS input signal for various inductor values connected in series with R_2 (R_2=200 Ω, R_3=35 Ω, L_1=5 nH, L_2=15 nH, L_3=25 nH)

5.5 Measurement Verification: The PA Module

The digital PA module used for experimental verification is shown in Fig. 5.33. The schematic of the GaN MMIC power switch is shown in Fig. 5.33. The circuit is similar to the one presented in [32] but with some differences. A resistor replaces the inductor in the upper differential transistor's drain (R_5), an additional resistor is connected in series with the lower one (R_6), a feedback capacitor (C_1), and a fourth stage (two stages are for the pre-driver) is added compared to the three-stage design in [32]. It consists of two cascaded common-source pre-amplifiers that feed the differential pair, which in turn drives the final stage. Ideally, the voltage at the output should show rectangular pulses with very steep slopes and zero switching delay so that the analog signal can be restored by the band-pass filter without distortions. In reality, however, this is not the case, which is to be studied in the following.

The realized MMIC is shown in Fig. 5.34. The key component is a power-switch MMIC, fabricated using the 0.25 µm FBH GaN process. It is mounted on a hy-

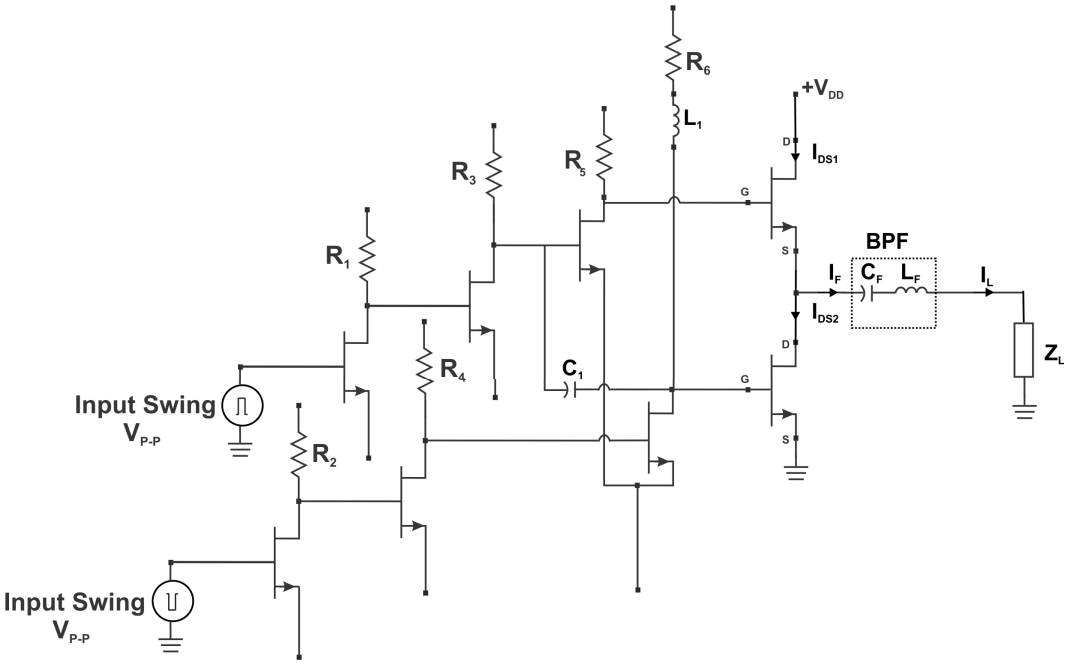

Fig. 5.33: Schematic diagram of the power switch (inputs are operated differentially)

brid board together with the blocking capacitors, the output network and connectors. The output network provides the band-pass filtering and matches the output impedance to 50 Ω. The filter is realized with SMD elements. The amplifier is designed for the 900 MHz band. It is operated at a final-stage supply voltage of 40 V and delivers up to 2.8 W in output power. One should add that the MMIC is not particularly optimized for fast switching or power efficiency but well suited to study the basic effects.

5.5.1 Measurement Results

In the following, both simulated and measured results for the AM-AM and AM-PM conversion are presented and discussed. For this purpose, pulse sequences with CW-tones of various amplitudes encoded according to the respective modulation scheme are fed to the input of the PA module described above. The resulting output signal after the bandpass filter is detected. Because of the CW input, the

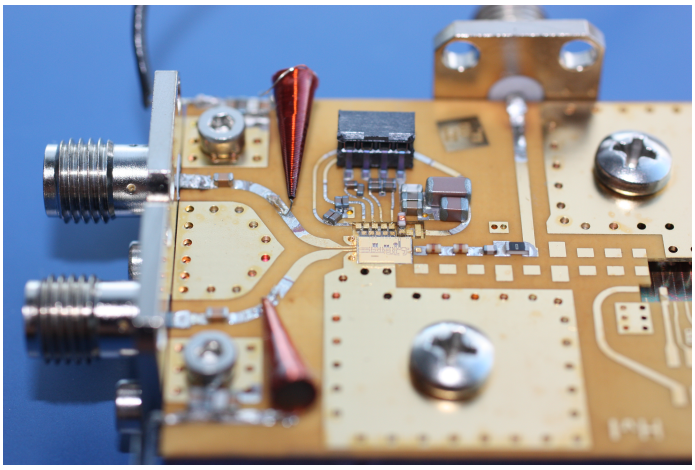

Fig. 5.34: The digital PA module

encoded signal is a sinusoidal one, so that amplitude and phase can be determined uniquely.

In measurements, this is done using an oscilloscope, performing an FFT on the time-domain signal and evaluating the complex amplitude at the signal frequency. In simulation, the entire module including the MMIC is analyzed by means of non-linear transient simulation in the time domain. The GaN-HEMTs are described by a conventional large-signal approach used for analog circuits, the FBH Angelov model (for details see the intrinsic model in [33]). The resulting data on frequency and complex amplitude are then extracted as in the measurement case.

5.5.1.1 Pulse Width Modulation with Constant Repetition Rate (PWM-C)

In this case, a PWM signal with constant repetition period T and varying pulse width tw (PWM-C) is applied. In this kind of modulation, amplitude information is encoded in the pulse width, which decreases with amplitude (see Fig. 5.2).

Input signals with back-off values of 0 dB (full-scale, FS), 2.1 dB, 4.1 dB, and 7.2 dB are used for driving the power amplifier. The resulting conversion in amplitude (AM-AM) and phase (AM-PM) are measured using a spectrum analyser (for power measurements) and an oscilloscope (for amplitude and phase measure-

ments using FFT). Simulation data are treated accordingly. The results are plotted in Fig. 5.35. One observes that distortion grows significantly with BO, i.e, as amplitude decreases, which can be explained easily: in time domain, increasing BO means shorter pulses. The transistors, however, are not able to switch fast enough when the pulse width minimizes. Eventually, rise and fall times become dominant and the resulting pulse width is more the result of parasitics than of the encoded input amplitude. As one can see from the measured data in Fig. 5.35, AM-AM conversion remains below 5% only for back-offs up to 4.1 dB. For higher BO values, AM-AM conversion increases substantially to 20% at a back-off of 7.2 dB. The AM-PM shows even stronger degradation behavior than AM-AM as 5° phase error are exceeded already at 2.1 dB back-off.

The simulation results agree with the measured ones reasonably well, except for the AM-AM data for the highest back-off value. This deviation can be explained through the fact that there is a relatively sharp boundary, below which the output signal vanishes due to parasitics. The value of this boundary is, among others, related to the threshold voltage of the GaN HEMTs, which shows relatively large tolerances and thus can be described by the model with only limited accuracy.

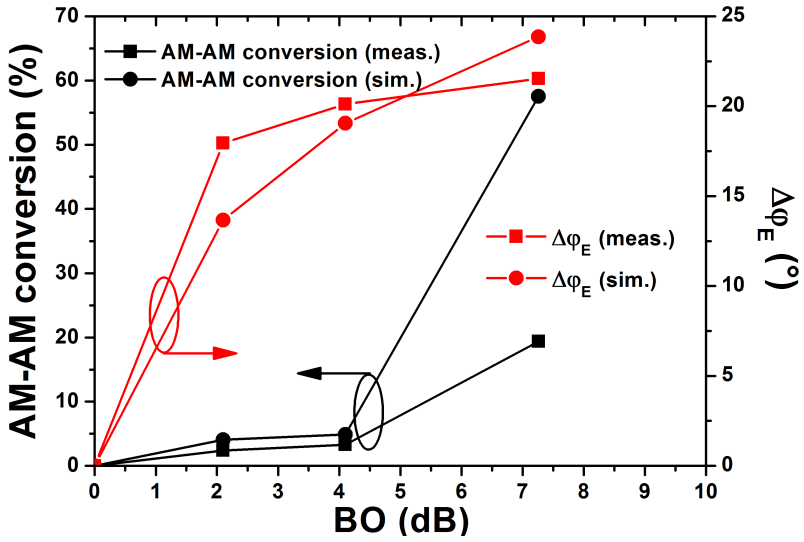

Fig. 5.35: Quasi-static AM-AM and AM-PM conversion vs. back-off for PWM-C modulation (measurements and simulation).

For the sake of completeness, Fig. 5.36 presents the measured output power P_{out} as a function of input back-off. Full-scale power is 34.6 dBm. One clearly identifies the deviation from the linear curve for back-off values above 4.1 dB, when output power is lower than the linear value because the actual pulse width is more and more compromised by switching time of the amplifier and other parasitics.

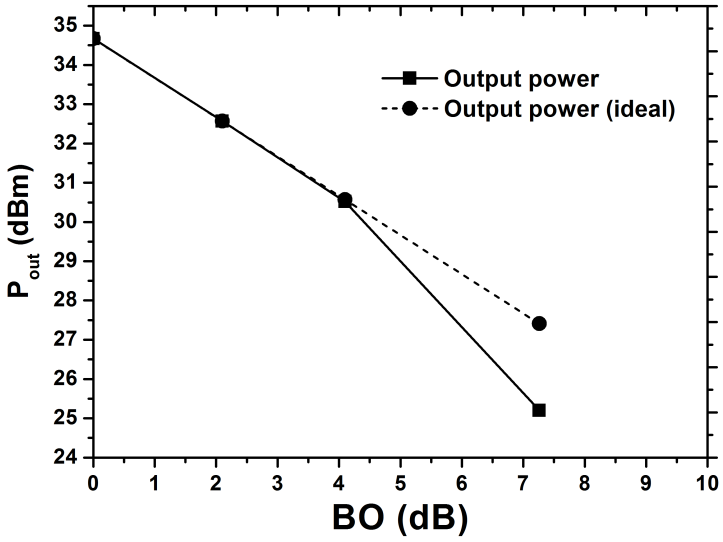

Fig. 5.36: Measured output power vs. back-off for PWM-C modulation

Given the results of figures 5.35 and 5.36 one concludes that the conventional PWM with varying pulse width is not a good choice for microwave digital PAs since it puts strong demands on the switching speed of the power switch, which are difficult to meet because of the transistor limitations in terms of power and cut-off frequency.

5.5.1.2 Pulse Width Modulation with Varying Time Period (PWM-V)

In this type of modulation, the time between two pulses is the quantity which changes while the pulse width remains fixed. In view of the results of the previous subsection, this property is clearly an advantage because it avoids short pulses. Fig.

5.13 explains the principle providing the pulse sequences for cw tones with 0 dB, 6 dB, and 12 dB back-off.

Fig. 5.37 presents the AM-AM and AM-PM conversion curves, determined as for PWM-C. Output power is plotted in Fig. 5.38.

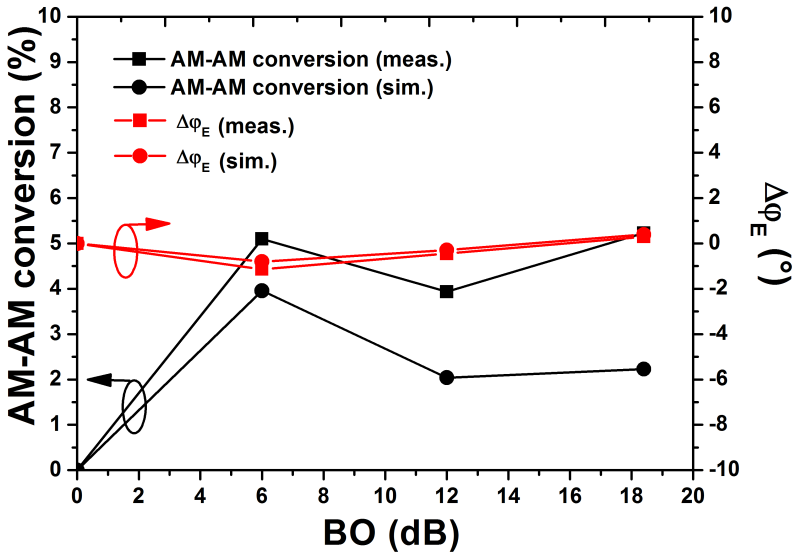

Fig. 5.37: Quasi-static AM-AM and AM-PM conversion vs. back-off for PWM-V modulation (measurements and simulation).

AM-AM conversion shows far lower values than for the previous modulation type PWM-C (see Fig. 5.35)). Maximum amplitude conversion is reached at 18.4 dB back-off with only 5.2%. For the phase error, all values were found to be less than 5° (the maximum acceptable AM-PM distortion in modern OFDM transmitters [28, 29]), which is significantly lower than for the PWM-C case.

Measurement and simulation data agree well. AM-AM conversion is slightly underestimated by simulation but the qualitative behavior is the same and the differences are smaller than 3%, which is in the accuracy range of the transistor models.

The behavior of output power in Fig. 5.38 supports this finding. One observes an almost linear curve within the entire back-off range up to 18.4 dB. Summarizing,

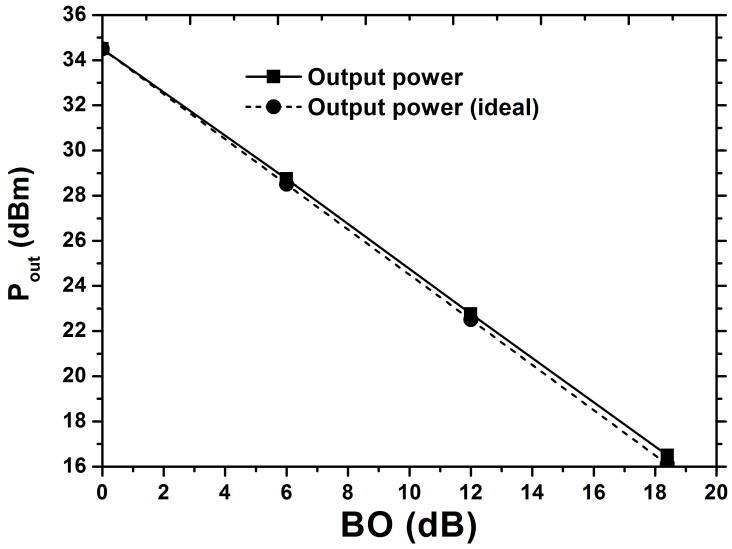

Fig. 5.38: Measured output power vs. back-off for PWM-V modulation

it is interesting to note how strongly modulation influences the resulting linearity behavior for the same power switching circuit. Employing PWM-V instead of PWM-C and thus avoiding shortening of pulses changes the situation completely and greatly improves linearity performance. One should note, however, that this does not come for free since PWM-V, due to its denser spectrum, puts stronger demands on the output filter.

5.5.1.3 Band-Pass Delta-Sigma Modulated Signal (BPDSM)

The well-known BPDS modulation creates a signal that, for our considerations, can be considered as a mixture of the two modulation schemes discussed before, PWM-C and PWM-V. It has short pulses as well as long ones but the widths of each bit is fixed, so there is a lower limit of pulse width. Moreover, it is a truly digital signal since both time and amplitude are discretized. Therefore, one expects amplitude and phase distortion values in between the other two schemes. On the other hand, as is well known, the coding efficiency of BPDS is lower than that of the PWM version, so overall PA efficiency degrades.

Fig. 5.39 and Fig. 5.40 present the AM-AM/ AM-PM curves and output power for BPDS signal excitation with a sampling rate of 4 times the signal frequency f_0 (about 3.6 Gbit/sec).

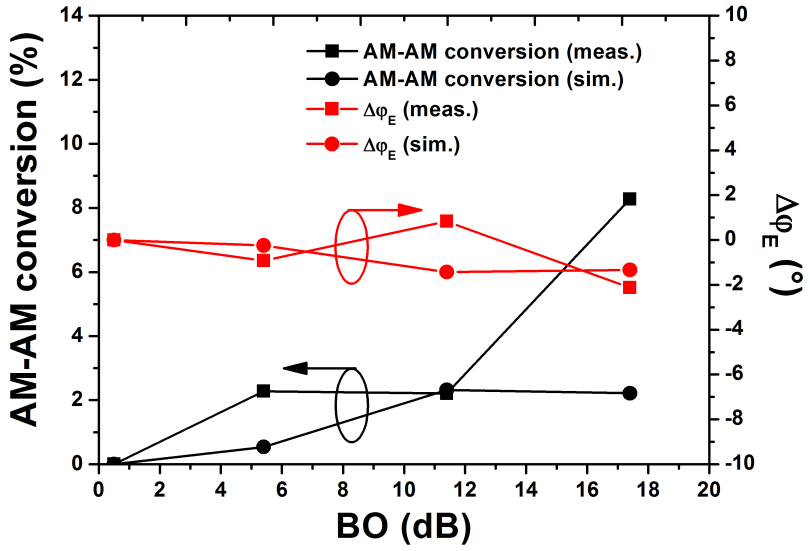

Fig. 5.39: Quasi-static AM-AM and AM-PM conversion vs. back-off for BPDS modulation (measurements and simulation).

As could be expected, amplitude distortion increases as input signal amplitude is reduced and the maximum of 8% deviation from the ideal linear response is reached for highest back-off. Phase error stays below 5° for the entire back-off range investigated. As for the previous case, agreement between simulation and measurements is good, except for the AM-AM value at the highest back-off (ca. 6%). We could not detect a special root cause for this other than the general accuracy limitations of particularly the nonlinear transistor description.

When examining the output power graph, we can see the effect of the low amplitude coding efficiency for BPDS compared to PWM-C and PWM-V. A full-scale output power of only 30.5 dBm is obtained, about 5 dB below the values for PWM-C and PWM-V. This is exactly what one expects since for a given maximum pulse

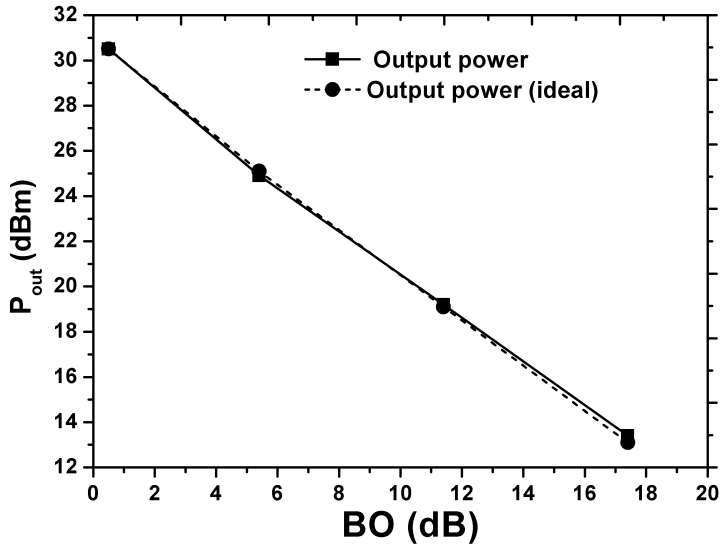

Fig. 5.40: Measured output power vs. back-off for BPDS modulation

voltage amplitude u_0 of the power switch the full-scale amplitude of the PWM reaches $4/\pi$ x u_0, in contrast to about 0.7 x u_0 for the maximum stable signal of a standard BPDS modulator [34].

Chapter 6

Summary and future work

6.1 Summary and contributions

This work is part of class-S digital power amplifier development effort made by the Digital PA Lab at the Ferdinand-Braun-Institut, Leibniz- Institut für Höchstfrequenztechnik (FBH). The main target was to contribute, for this type of switching power amplifiers, results on output network optimization and to perform a basic study on distortions in terms of AM-AM and AM-PM conversion.

The class-S is based on a realization for the 900 MHz frequency band using a class-D voltage-mode topology for the final stage. The power switch was fabricated as MMIC using the FBH GaN-HEMT process with 0.25 µm gate length. In a first part, different designs for the output filter were investigated. One design used purely commercial SMD elements (ATC capacitors and Coilcraft inductors). The other design is based on the idea of using bond-wires instead of inductors in the LC tank to increase the self-resonance frequency for better suppression of harmonics. The bond-wire has been modeled using EM simulation and was then composed to a four-sections structure to provide the needed inductance value close to the inductor's value used in the lumped element filter used before. The network was realized on a Rogers PCB laminate (ε=3.55) with 800 µm substrate thickness and a 17 µm conducting strip and was mounted on a copper heat-sink.

Comparing the lumped network with the bond-wire based one, measurements showed results in favor for the latter. The new method delivered better impedance characteristics and better reflection coefficients at the signal band and, particularly, higher impedance at harmonics with shifting the self-resonant frequency from almost 4 GHz (lumped case) to about 6.8 GHz. The measurements of the bond-wire filter in the complete class-S module showed better efficiency than the SMD version with almost 33% maximum drain efficiency compared to 28% for the SMD version. This was true only up to a certain supply voltage (≈23 V). Then drain efficiency degraded. However, this degradation is attributed to inappropriate mounting of the MMIC chip. Thus, the advantages for the bond-wire realization could be verified experimentally.

The second and more important part of the work was studying digital class-S PA with regard to its nonlinear behavior. To start with, we have measured the PA under load-pull environment to investigate the influence of a matched impedance, including a reactance instead of a pure resistive load, on power and efficiency. The results proved that controlling the harmonics plays no role but power and efficiency can be improved by using a complex matched load. Almost 0.4 dB more power could be obtained by using a load with a capacitive reactance part and 11% more drain efficiency when using an inductive complex load. However, these improvements are achieved at the expense of increased distortion. Hence, for our work, load-pull was only a gateway for the distortion analysis which is a core topic of interest for class-S PAs.

Nonlinearity analysis of digital PAs differs basically from the conventional PA one. In most digital PAs, for instance, nonlinearity increases as amplitude decreases (increased back-off) while in conventional PAs one has the inverse behavior. In order to enhance understanding of the basic effects, the investigations were focused on the quasi-static case. In other words, signals with time-constant amplitude and phase were encoded covering the practical range of amplitude and phase. Band-pass delta-sigma (BPDS) and two different pulse-width modulation (PWM)

schemes were used for coding. Amplitude and phase distortion are the two measures of linearity we considered. I.e., deviation from the linear amplitude response of the PA determined the AM-AM conversion while the change between input and output phase described by AM-PM conversion.

In order to better understand the origin of distortions, the analysis was expanded on the amplifier level scrutinizing the behavior of its three stages: preamplifier, driver, and final stage. Simulations revealed that the most critical stage is the driver which in many cases does not deliver the proper input voltage to the final-stage transistors. Accordingly, for most investigations a 2-stage version (driver and final-stage) was simulated to save simulation time since the preamplifier proved to have no strong distortion.

Amplitude and phase conversion (AM-AM and AM-PM) were first analysed with ADS simulation tools. Signals with different back-off were used at the input of the amplifier, applying PWM signals with two different switching characteristics as well as BPDS .

Each modulation scheme has different properties and thus leads to a different optimum for the values of the circuit elements of the driver, more precisely the drain loads of the differential driver circuit, which can be pure resistors or combinations of resistors with inductors. For these drain impedances, a compromise between and the best values for each modulation type was finally selected and with them the digital PA was realized. Measurements of this module were compared with its simulation (complete demonstrator with four stages instead of two).

The results show the switching characteristics of the final-stage and the drivers play the key role determining linearity of the class-S PA. More precisely, the quality of the signal at the inputs of the final stage transistors, the rise and fall times and other non-ideal characteristics is decisive. This implies that the pulse width should be limited to a lower bound in order to avoid strong linearity degradation due to the non-ideal switching times of the PA. Thus, a PWM version with varying

pulse width shows unacceptable high amplitude and phase distortion already at relatively low back-off values. On the other hand, a PWM variant where the width of the pulse is fixed and only the period is changing exhibits advantageous linearity performance with AM-AM below 6% and AM-PM below 2° for the back- off range up to about 20 dB. BPDS modulation, due to its lower bound in pulse width, comes close to this level with AM-AM below 8% and AM-PM up to 2°. The simulations results could be verified by measurements, time-domain simulations using a conventional large-signal GaN- HEMT transistor model yielded good accuracy in most cases.

The outcomes of the results obtained have improved the understanding of where nonlinearities in the class-S PA originate from and what are the circuit details that need to be worked on to reduce distortions. Overall, however, one has to state that linearity is a key feature in digital PA design, but only one among a few others. It has to be considered together with output power level power efficiency, and the efforts on circuit size and output filter. And it depends basically on the coding scheme used. Optimum performance can be achieved only if all these aspects are accounted for. Particularly, in switch circuit design one must optimize the combination of switching speed and power efficiency.

6.2 Future work

The efforts made in this work was to establish a good and concrete understanding of the class-S digital PA concept and its AM-AM/ AM-PM conversion. Further investigation are definitely a must to exploit this knowledge for improved circuit and module design, combining linearity and efficiency requirements. One possible path is to improve filter characteristics, which relaxes requirements on other sides. A work published in [35] was part of this attempt. However, the focus should be on the driver circuit, which is most critical for switching and at the same time consumes a lot of power, thus governing the power added efficiency (PAE) of the complete digital PA.

In linearity analysis, the next step to go is to go beyond the quasi-static analysis as used in this work. Realistic test signals like WCDMA and WiMAX are to be employed to study the digital PA under real-world transmission conditions. Here **A**djacent **C**hannel **P**ower **R**atio ACPR (or **A**djacent **C**hannel **L**eakage **R**atio ACLR) and **E**rror **V**ector **M**agnitude (EVM) are the key measures describing nonlinearities.

Another technique to minimize the nonlinearity is by using **D**igital **P**re **D**istortion (DPD) techniques. To this end, one has to note that applying the standard DPD methods developed for analog amplifiers allow improvements in linearity [36] but are certainly not the optimum choice given the completely different distortion behavior. This appears to be an interesting new field for research.

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