High-Performance Transceiver Front-Ends in SiGe Technologies for 400 Gb/s Optical Links

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zur Erlangung des akademischen Grades

Doktor der Ingenieurwissenschaften
-Dr.-Ing.-

genehmigte Dissertation

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Tag der wissenschaftlichen Aussprache: 11. April 2019

Berlin 2019

I lovingly dedicate this thesis to my parents, Luis and Marisa, who with their own efforts and sacrifices, have allowed me to reach this far.

Con todo mi cariño, dedico esta tesis a mis padres, Luis y Marisa, que con su esfuerzo y sacrificio me han permitido llegar hasta aquí.

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Acknowledgements

The accomplishment of this thesis brings the conclusion to one very important section of my life during which I have experienced tremendous growth, both at a professional and at a (more important) personal level. I heartly wish to acknowledge several remarkable individuals who have contributed to my reaching this point.

I would like to express my most sincere gratitude to my supervisor, Prof. Dietmar Kissinger, who has been an essential reference figure for me during this time. He has provided me the support and motivation necessary to stay on track in this long road and has helped me channeling my efforts by defining clear goals and priorities. He has given me complete freedom to pursue various ideas without objection and has always encouraged me to aim high. I heartly wish to thank him for believing in me and my potential possibly more than I do myself, and for always keep creating opportunities for me to expand professionally.

My most sincere appreciation goes also to my second advisor Prof. Cagri Ulusoy for his mentoring and guidance, which has helped me to shape the majority of this thesis. His knowledge and his vision have challenged me to think more deeply, and his genuine enthusiasm and optimism for what we do have encouraged me to reach more broadly. 2015 has been my most productive year ever! From Cagri I learnt the right way of working in terms of fairness, accuracy and responsibility which has made me a better scientist. I feel very fortunate for having worked with him.

I would also like to thank Prof. Dr.-Ing. Friedel Gerfers for agreeing to review this thesis, and for providing insightful comments and recommendations.

My BIG, most heartfelt thanks go to (now, Dr.!) Pedro Rito, with whom I had the luck to start in parallel the IHP journey. I wouldn't have made it this far without him. His knowledge, his generosity and commitment to work and to helping others have been amazing to witness. It would be *spatially* impossible to recall all the ways in which he has helped me throughout this time; he has been my primary resource for solving my electronics questions and his friendship out of office has been essential to making this period very enriching and joyful. I feel tremendously blessed for having shared this long PhD journey with you! Your brilliance, open-mindedness, dedication and kindness are overwhelming! I look forward to seeing how far you'll reach!

I wish to thank Dr. Daniel Micusik for hiring me in the first place!! Daniel was my first supervisor and put his trust on me when it must have been very difficult to do so... I heartly wish to thank him for his faith in my learning curve. Daniel brought to Pedro and I a work-methodology that has proven extremely useful, and we absorbed much from him in those first two years. I value especially the working-ethics, integrity and enthusiasm that he always transmitted to us. With his deep knowledge and charisma he has inspired me to continue this

path. I must extend my acknowledgment to Prof. Lars Zimmermann and to the Photonics department, for creating an exceptional collaborative environment, and to all the colleagues in the Circuit Design department for sharing their wisdom, knowledge and experience. Thank you also to Manja, who made all the administrative work so easy.

Crossing paths with Subhajit has been the biggest gift that the PhD time has brought to me, for which I am inmensely grateful. His friendship has become a pillar in all these years, and his advice and continuous support in so many levels have been central in the completion of this thesis (and, actually, in my life endeavours). He has closely witnessed my ups and downs and has shown a natural talent for dealing with them, helping me to keep things in perspective. Every single page of this thesis has gone under his eyes :) Subhajit, thank you for being so present! You are beyond amazing and I am forever grateful.

Rahul, thank you for your friendship! you have been responsible for a significant part of my happiness (and wild laughter) in Frankfurt (Oder)! Miljana, I loved our long chats! and thank you, of course, to my friends at home, Vanessa and Silvia, for making things stay the same, despite the distance.

Finalmente ... con todo mi corazón, quiero agradecer a mis padres su apoyo incondicional, aliento e inspiración, y el haberme dado la oportunidad de perseguir mis sueños y aspiraciones profesionales. Gracias por entender la distancia, por ser tan *avanzados* en tantos aspectos y por animarme siempre cuando me cansa el camino. Gracias por las conversaciones diarias! y por creer en mi: es por vosotros que soy lo que soy. Gracias a mi hermano, por estar ahí cuando yo estoy lejos. Gracias a mi abuela, mi eterna admiradora! Y a mis abuelos, os recuerdo; sé que estaríais orgullosos de mi. Gracias, GRACIAS, por vuestro amor inmenso! No puedo expresar con palabras cuánto significa para mi.

It seems about time to close this life chapter. IHP has given me all the great opportunities that a PhD student should have and opened up incredible paths ahead of me. Cherishing all my experiences in the past years, I look forward to move onto the new journey!

Frankfurt (Oder), September 2018.

Zusammenfassung

Die optische Glasfaserkommunikation ist ein wichtiger Bestandteil in der heutigen industriellen Entwicklung und des wirtschaftlichen Fortschrittes in unserer modernen Gesellschaft geworden. Um die Anforderungen des zunehmenden Datenverkehrs zu erfüllen, die für Anwendungen wie das Internet der Dinge (IoT) und Cloud-Computing benötigt werden, müssen die Bandbreite, die Leistungsaufnahme und die Baugröβe solcher Systeme weiter skaliert werden. Für die nächste 400 Gb/s Generation und nachfolgende optische 1 Tb/s Transponder sind elektronische Frontends als Schnittstelle zu den optischen Übertragungselementen ein untrennbarer Bestandteil, der die Gesamtsystemleistung entscheidend beeinflusst. Die vorliegende Arbeit untersucht neuartige Schaltungskonzepte und Methoden mit dem Ziel der Verbesserung verschiedener Leistungsparameter wie Datenrate, Energieverbrauch und Eigenrauschen von elektronischen Breitbandschaltungen in optischen Transceivern. Als Ergebnis präsentiert diese Arbeit mehrere integrierte Schaltungen in verschiedenen Knoten einer modernen SiGe:C BiCMOS Technologie die den Stand der Technik signifikant verbessern.

Auf der Senderseite (Transmitter, Tx) wird der traditionelle, aber leistungshungrige, Ansatz zur Erzeugung höherwertiger Modulationsformate mit Hilfe von linearen Treibern in Kombination mit einem externen Digital-zu-Analog-Umsetzer (DAC) aufgegriffen und durch die Einführung eines energieeffizienten Tx-Moduls mit integrierter 4-b DAC-Funktionalität deutlich verbessert. Dabei werden zwei Integrationskonzepte untersucht: Ein hybrides Konzept, in dem ein I/Q InP Mach-Zehnder-Modulator (MZM) zusammen mit einem SiGe BiCMOS Treiber integriert wird, welches eine 256-Quadratur-Amplituden-Modulation (QAM) mit einer Symbolrate von bis zu 32 GBd ermöglicht, die in einem Rekord-Energieverbrauch-pro-Bit von lediglich 6.4 pJ/bit resultiert, und ein monolithisch integrierter elektronisch-photonischer Transmitter, der für den Betrieb einer 4-Level Pulse-Amplituden-Modulation (PAM-4) bis 37 GBd geeignet ist, der bisher höchsten Symbolrate unter Verwendung von Silizium-Photonik-Modulatoren. Die Hybridlösung findet dabei Anwendung bei den klassischen Telekommunikationsreichweiten, während der monolithisch integrierte Tx eine kostengünstige Lösung für Applikationen mit kurzer Reichweite wie Datenzentren bietet. Erfolgreiche elektro-optische (E/O) Messungen wurden für beide Prototypen durchgeführt.

Auf der Empfängerseite (Receiver, Rx) liegt der Schwerpunkt der Arbeit auf der Untersuchung besonders rauscharmer linearer Transimpedanzverstärker (TIA) mit einer hohen Bandbreite. Dabei wird eine rauscharme Designmethodik vorgestellt und darauf basierend TIA-Implementierungen mit weniger als $10\,\mathrm{pA}/\sqrt{Hz}$ mittlerer eingangsbezogener Rauschleistungsdichte bei einer Datenrate von 100 Gb/s aufgezeigt. Mittels der vorgeschlagenen Vorgehensweise werden darüber hinaus innovative Rx-Konzepte für energieeffiziente Module präsentiert: Ein Benchmark-TIA, der eine Bandbreite von 60 GHz mit weniger als $5.5\,\mathrm{pA}/\sqrt{Hz}$ Rauschleistungsdichte erreicht, und eine spezifische Lösung für ein PAM-4 Rx-Frontend mit einem integrierten Flash-Analog-Digital-Umsetzer (ADC), der PAM-4 Signale mit einer Datenrate von bis 100 Gb/s demodulieren kann. Zuletzt wird erstmals ein TIA in einer Folded-Kaskode-Architektur unter Zuhilfenahme von bipolaren pnp-Transistoren vorgestellt, um die Vorteile einer komplementären Technologie in energieeffizienten Hochgeschwindigkeits-Empfänger-Frontends zu demonstrieren.

Abstract

Optical fiber communication has become the key enabler of today's industrial development, economic progress and modern society. In order to support the increasing data traffic demands required for applications such as the Internet-of-Things (IoT) and Cloud Computing, the bandwidth, power consumption and space density of current systems all need to scale further. For the next generation 400 Gb/s and soon also 1 Tb/s optical transponders, the electronic front-ends that are directly interfacing the photonic devices, are an integral part and strongly influence the overall system performance. This thesis investigates circuit-level methods for enhancing different performance metrics such as high data rate, low power consumption and low noise in various broadband circuits for optical transceivers. Several contributions to the state-of-the-art in such integrated circuits (ICs) are proposed and implemented in different nodes of a modern SiGe:C BiCMOS technology platform.

On the transmitter (Tx) side, the traditional but power-hungry approach used for generating high-order modulation formats based on linear driver amplifiers together with an external digital-to-analog converter (DAC) is revisited. Here, the implementation of energy-efficient Tx modules featuring integrated 4-b DAC functionality is presented. Two integration concepts are explored: a hybrid one, which incorportates an I/Q InP Mach-Zehnder modulator (MZM) together with a SiGe BiCMOS driver demonstrating up to 32 GBd 256-quadrature-amplitude-modulation (QAM) signal modulation with record low energy-per-bit of 6.4 pJ/bit and a monolithically integrated photonics Tx capable of up to 37 GBd pulse-amplitude-modulation (PAM)-4 operation, which is the highest among silicon-photonics (SiPh) modulators. The hybrid solution targets telecom reach, while the monolithically integrated Tx provides a low-cost solution for short range applications. Electro-optical (E/O) measurement results are available for both prototypes.

On the receiver (Rx) side, the focus lies on the development of low noise, high-bandwidth linear transimpedance amplifiers (TIAs). A low noise design methodology is described, and TIA implementations featuring less than 10 pA/$\sqrt{Hz}$ averaged input referred current noise density while operating at 100 Gb/s data rate are demonstrated. Based on the proposed design methodology, supplementary advanced Rx concepts towards power-efficient modules are presented: a benchmarking TIA which achieves 60 GHz bandwidth with <5.5 pA/$\sqrt{Hz}$ and a custom solution for a PAM-4 Rx front-end integrating a 2-bit flash analog-to-digital-converter (ADC) capable of demodulating signals at up to 100 Gb/s data rate. Finally, a TIA in folded-cascode architecture which makes use of pnp transistors in order to explore the benefits of a complementary technology in power-efficient high-speed Rx front-ends is also described.

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1 Introduction

1.1 The Zettabyte era: Trends and perspective

The advent of the internet in the 1990s caused a sudden global leap in the access and diffusion of information, both in the commercial (business) and domestic sectors. This led to the transition towards the *Information Age* and an economy based on information technology. The World Wide Web, used initially as a simple electronic billboard, morphed into an interactive consumer exchange platform; e-mail became customary and other traditional media businesses, such as book publishing, music and TV, also experienced the impact of the digitization of information. Enterprises in different domains started exploring the possibilities of capitalization on this new paradigm and led to the establishment of the *connected life* within the social fabric. Since the 2010s, the increase in the number of users and the diversification of connected devices (PCs, tablets, TVs, smartphones), have caused the internet ecosystem to expand rapidly. New applications such as web storage, file sharing, internet video, video-on-demand (VOD) or more recently cloud computing, have grown dramatically [1]; *Big Data* and the *Internet-of-Things (IoT)* are becoming a reality. This trend can be observed in the Cisco forecast in Figure 1.1: Global IP traffic is expected to increase nearly 3-fold between 2016 and 2021, with data-centers alone accounting for approximately 70% of the traffic concentration, making them the backbone of today's electronic society. In order to provide satisfactory user experience, this scenario requires essentially one thing: Higher transfer data rates.

Optical fiber communication technologies are the enabling factor behind such growth. Figure 1.2 shows how the B·L product has increased by a factor of 10^{18} with the emergence of different technologies. B stands for bit-rate and L is the distance at which the signal needs to be regenerated to preserve fidelity (repeater distance). It is evident to see the change in slope that occured around 1980, when optical fibers were first used. Optical fiber is ligther, thinner and provides higher bandwidth and lower loss than electrical wiring. Featuring less than 0.25 dB/km attenuation around the emission wavelength of 1550 nm it enables transmission at up to Tb/s data rates across thousands of kilometers [2, 3]. Due to its non-metallic character it is also inmune to electromagnetic interference and crosstalk. High-paralellism techniques such as wave-length division multiplexing (WDM) or space division multiplexing (SDM) can significantly increase the aggregate bandwidth, making it several orders of magnitude faster

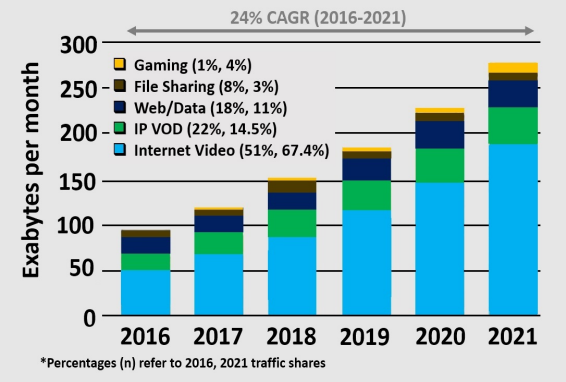


Figure 1.1: Cisco forecast for global IP traffic growth from 2016 to 2021 [6].

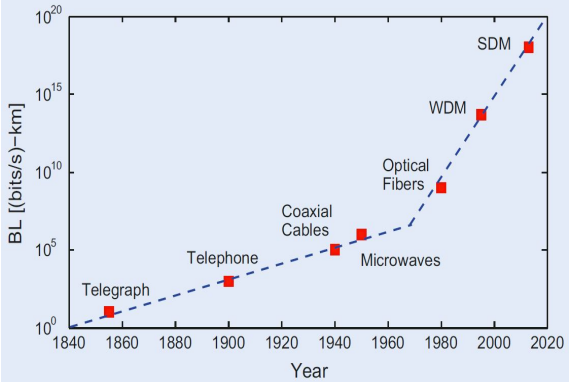


Figure 1.2: Historical increase in the B·L product with new technologies [2].

than electrical wiring [2, 4, 5]. The disadvantage of optical communication is the transceiver cost, rendering it traditionally more profitable for the long-haul backbone networks, where production volumes are small and margins from equipment manufacturers are large. In the data-center communication market, volumes are enormous, and growing with time, leading to high pricing pressure. Here, recent advancements in silicon-photonics (SiPh) promise cheaper and scaled optics allowing optical communications to conquer more territory.

1.2 Topography of optical fiber networks

The architecture of optical networks in Germany is shown in Figure 1.3 [7], and is traditionally divided into three groups based on the targeted distance: (i) core or long-haul networks, (ii) metro or regional networks and (iii) access networks. Access networks are at the lowest level of the hierarchy, and incorporate the connections of the subscribers to their particular service providers. These networks are currently dominated by copper and radio connections, although the migration towards optical links has already started. Typical data rates in access networks are several hundred Mb/s and evolving towards 1 Gb/s [8]. The aggregated data from access networks is routed to the next level of the hierarchy, the metro or regional networks. These networks connect different local providers together and are based on optical fiber connections. Their internal routing is evolving from typical ring or star topology, as depicted in Figure 1.3, towards meshed architecture featuring redundancy for improved capacity and reliability. Finally, the core networks are at the top of the hierarchy and are responsible for transporting data aggregated by several metro networks, connecting countries with each other.

The recent evolution in cloud computing and data-centers has introduced a new domain in metro networks, termed data-center interconnects (DCI). Two primary types can be distinguished: telecom- DCI and metro- DCI (datacom), which together include the traffic within a data-center, between geographically distant data-centers and from data-center to user. Almost all computation from consumer electronics are directed to data-centers, and enterprises are also shifting most of their computing power outside, outsourcing it to data-centers for cloud and distributed computing.

DCIs are mainly point-to-point links featuring differentiated transmission schemes. In the telecom networks, which cover distances of several hundred km, the maximization of

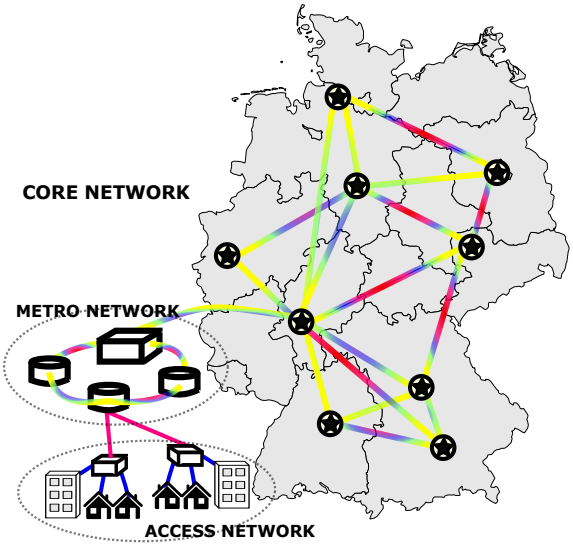


Figure 1.3: Architecture of optical networks in Germany. Adapted from [7].

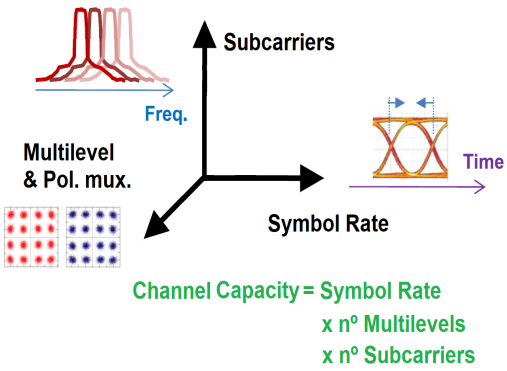


Figure 1.4: Dimensions for increasing channel capacity. Adapted from [9].

the product of spectral efficiency and distance is of primary importance. These networks have traditionally relied on WDM, which allows for capacity increase without infrastructure modification. However, upcoming standards such as 400 Gb/s and 1 Tb/s [10] cannot be sustainably accommodated by successively multiplexing lower speed carriers on different wavelengths, limited by power dissipation, form-factor and system complexity. Next generation transceivers must, therefore, resort to alternative dimensions to increase data throughput, namely: the use of digital coherent transmission schemes and/or the increase in the baud rate, as depicted in Figure 1.4. Digital coherent technologies make use of coherent detection together with digital signal processing (DSP), enabling the use of high-order modulation formats such as phase-shift-keying (PSK) and quadrature-amplitude-modulation (QAM), which provide better spectral utilization. Together with digital equalization techniques, such schemes allow for compensation of the fiber impairments in the telecom link. However, they are more susceptible to noise and non-linearities, featuring low optical signal-to-noise-ratio (OSNR) tolerance which limits the maximum achievable reach. On the other hand, higher baud rates relax the degradation in OSNR, but must resort to innovative circuit-level techniques and further advancements in high-speed electronics in order to increase the analog bandwidth.

Meanwhile, short reach optical modems, called "small form-factor pluggables", cover distances ranging from 100 m to 80 km and the key aspect in this arena is the cost and footprint reduction. Thus, datacom communication resorts mainly to intensity-modulation/direct-detection (IM/DD) formats, due to their relative system-level simplicity. Here, strict requirements in terms of low power dissipation and small form factor for pluggable modules must be considered. Thus, for the datacom transceivers, the challenge is to support high bit rates per optical carrier while using low-cost components and low-power electronics, leaving limited power budget for eventual DSP usage to clean up the signals.

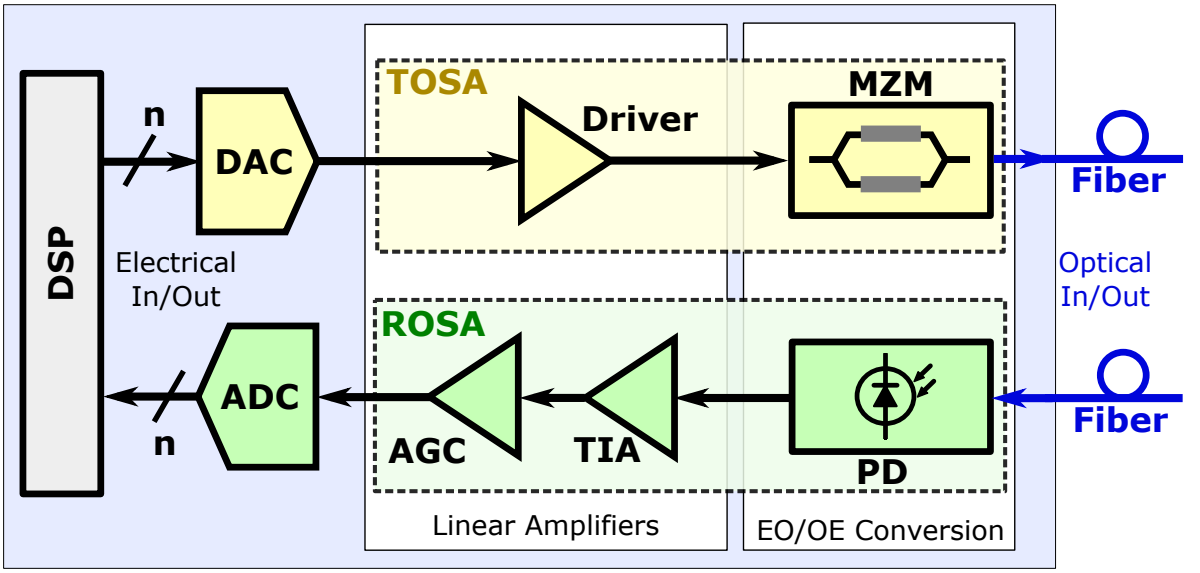


Figure 1.5: Simplified block diagram of a DSP-based optical transceiver.

1.3 Optical transceivers overview

Optical transmitters (Txs) and receivers (Rxs) are required to switch between the optical and the electrical domains. Figure 1.5 shows the simplified block diagram of a DSP-based optical transceiver, which is the preferred architecture since the last decade when DSP and data-converters became sufficiently fast [11, 12]. The DSP is the first block of the transmitter, encoding the data according to a modulation format suitable to the particular application. This binary data is converted into an analog signal by the high-speed digital-to-analog converter (DAC) and is then amplified linearly to the specific swing required to drive an electro-optical (E/O) modulator at a sufficient extinction ratio (ER). The ER is the ratio between the optical power of the logical "1" and the logical "0", and determines the signal-to-noise-ratio (SNR) of the link. Finally, the E/O modulator converts the information to the optical domain; the optical carrier is in this way modulated with an envelope that resembles the electrical data. The Rx is responsible for demodulating this envelope information from the optical carrier and converting it back to ditigal values. A photodiode (PD) receives the optical power and transforms it into an electrical current. This current is converted to the voltage domain with a transimpedance amplifier (TIA); the automatic gain control (AGC) provides additional voltage gain to amplify the signal in order to meet the sensitivity of the analog-to-digital-converter (ADC) where the signals are digitized. Lastly, the DSP decodes the data, leaving it ready for further processing. The transceiver is often built around a transmitter optical sub-assembly (TOSA) and a receiver optical sub-assembly (ROSA), which are small packages containing the E/O and the electrical front-end devices as indicated in Figure 1.5, as well as some other optical parts such as lenses and means for optical fiber alignment.

The hardware realizations of such transceivers pose many challenges due to the high-operating frequency, wide bandwidth and low noise requirements, which have led to commercial modules being historically dominated by III-V compound semiconductor technologies such as gallium arsenide (GaAs) and indium phosphide (InP). However, for low-cost, mass-market electronics, silicon technologies (Complementary Metal-Oxide-Semiconductor (CMOS) and

SiGe) are preferred. While CMOS provides cost advantages in mass production and lower power consumption, especially for digital circuits, SiGe Bipolar Complementary Metal-Oxide-Semiconductor (BiCMOS) features better noise characteristics and higher breakdown voltages at comparable f_T [13] and is the platform of choice for the prototypes described in this thesis.

1.4 Scope and organization of the thesis

This work focuses on the development of high-performance front-end analog integrated circuits (ICs) (modulator drivers and TIAs), making use of different nodes of the SiGe:C BiCMOS technology of IHP, for the next generation of datacom and telecom optical transceivers. Circuit-level methods for enhancing different performance metrics such as high data rate, low power consumption and low noise are described and demonstrated through the characterization of the fabricated prototypes. The thesis is comprised of total six chapters. After this introduction, it is organized as follows:

Chapter 2 starts with an overview of the E/O components used in the transceiver modules. Greater detail is given in the description of the E/O modulator, since it is used for the implementation of the Tx modules described in Chapter 3. The theoretical basics of high-speed broadband circuit design, essential to understand the module implementations reported in the subsequent chapters, are presented. A brief description of the different integration approaches and the technology nodes in which the ICs are fabricated are provided as well.

Chapter 3 presents the implementation of Tx modules featuring integrated 4-b DAC functionality. The first part of the chapter describes a hybrid assembly which incorporates an InP segmented Mach-Zehnder modulator (SEMZM) together with a SiGe BiCMOS driver demonstrating up to 32 GBd 256-QAM signal modulation with record low energy dissipated per bit. In the second part of the chapter, the same concept is implemented in the electronic-photonic-integrated-circuit (EPIC) platform of IHP, demonstrating up to 37 GBd PAM-4 operation, which is the highest baud-rate reported to date among silicon-based modulators.

Chapter 4 describes a design technique for TIAs, which permits simultaneous low noise and high-bandwidth performance. The method is then verified by means of two analogous TIA implementations in the SG13S and SG13G2 processes with designs that feature less than $10\,\mathrm{pA}/\sqrt{Hz}$ averaged input referred current noise density while operating at 100 Gb/s data rate.

Chapter 5 presents advanced Rx architectures aiming at power-efficient modules, based on the low noise design technique described in Chapter 4. First, a benchmarking TIA which achieves 60 GHz bandwidth and integrated input referred noise current density lower than $5.5\,\mathrm{pA}/\sqrt{Hz}$ is described. High Rx sensitivity is key to a power-efficient optical link. Second, the SG13G2 TIA from Chapter 4 is used to implement a custom solution for a pulse-amplitude-modulation (PAM)-4 Rx front-end capable of demodulating signals at up to 100 Gb/s data rate. Finally, a TIA in folded-cascode architecture which makes use of pnp transistors is

described, exploring the benefits of a complementary technology in power-efficient high-speed Rx front-ends.

Chapter 6 draws conclusions and provides an outlook of future technical challenges for optical communication systems.

2

Optical Transceivers Fundamentals

2.1 Electro-optical devices

The electro-optical (E/O) devices, namely the photodetector on the receiver (Rx) and the E/O modulator on the transmitter (Tx) enable the transfer between the electrical and the optical domains and their characteristics largely determine the transceiver's performance and design. Furthermore, co-integration and co-design of these elements with the front-end electronics can potentially improve the overall system performance.

2.1.1 Photodetector

The photodectector transforms the optical signal into electrical current, and it must feature a large response to the received light, sufficiently large bandwidth (BW) for the incoming signal and generate as low noise as possible. One of the most widely used photodetectors is the *p-i-n* photodiode, shown in Figure 2.1a. It consists of a p-n junction with a layer of intrinsic (undoped or lightly doped) semiconductor material sandwiched between the p- and the n-doped materials. The junction is reverse biased with $-V_{PIN}$ to create a strong electric field in the intrinsic layer. Photons with the proper energy (i.e. $hc/\lambda > E_g$, where E_g is the bandgap energy of the absorption material) enter through a hole in the top electrode (anode), pass through the p-doped material and reach the i-layer. Here they are able to push electrons from the valence band to the conduction band creating electron-hole pairs. These pairs become separated by the strong electric drift field with the holes travelling to the negative terminal and the electrons travelling to the positive terminal, as indicated in Figure 2.1a. As a result, the photocurrent i_{PIN} appears at the diode terminals. The *quantum efficiency (η)* is the fraction of incident photons that stimulate an electron-hole pair contributing to the photocurrent. An ideal photodetector has a 100% quantum efficiency, with $\eta = 1$. η depends on the width W of the absorption layer: The wider W, the higher are the chances of absorbing a photon. It also depends on how much light is coupled from the fiber into the detector. Thus, sub-optimal fiber coupling, surface reflection and absorption of the photons as heat or loss due to recombination (as opposed to contributing to the photocurrent) all reduce the η from its ideal value [14].

Electrically, the photodiode (PD) is measured by its *responsivity*, given by $R = I/P$ in A/W, where I is the generated electrical current and P is incident optical power. The

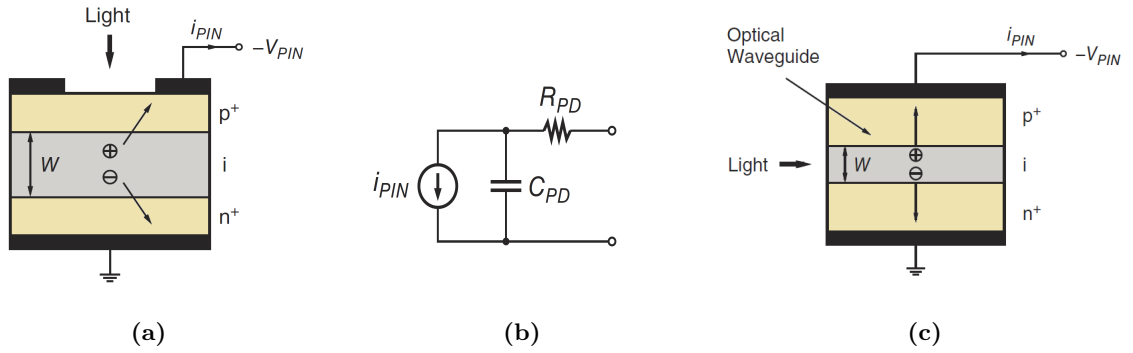


Figure 2.1: (a) Vertically illuminated p-i-n photodetector cross-section, (b) corresponding electrical equivalent and (c) waveguide p-i-n photodetector [14].

responsivity is related to the quantum efficiency by the photon energy (hc/λ) and the electron charge q, through (2.1).

$$R = \eta \frac{\lambda q}{hc} \tag{2.1}$$

From this relationship, it is obvious to see that R is proportional to η, and in the same way, longer width of the intrinsic region W will increase the R. However, the value of W also determines the time it takes for the carriers to traverse the absorption layer, and thus, a longer W increases the transit time and reduces the speed of the PD. The transit time depends also on the strength of the electric field: with increasing field strength, the carrier velocity increases and saturates at $V_{c,sat}$. Therefore, the reverse bias voltage ($-V_{PIN}$), must be high enough such that velocity saturation is reached. On the other hand, smaller W not only degrades R but may also limit the BW by increasing the capacitance of the PD, C_{PD}, since it reduces the distance between the electrodes (i.e. the capacitor plates). The C_{PD} together with the contact and spreading resistances, modelled by R_{PD}, as in Figure 2.1b, create also an RC-limiting time constant. The overall BW of the pin PD is limited by the transit-time and this RC-constant, both having inverse relationships with W: If the absorption layer is made thinner to reduce the transit time, the diode capacitance gets larger, and the RC constant becomes more dominant. The BW of the p-i-n PD is modelled by (2.2).

$$BW_{PIN} = \frac{1}{2\pi(W/3.5v_{c,sat} + R_{PD}C_{PD})} \tag{2.2}$$

Waveguide or edge-coupled PDs, as depicted in Figure 2.1c solve this trade-off between η and BW by illuminating the PD from the side, rather than from the top. In this way, the η is controlled by the horizontal dimension, which can be made large, while the transit time is controlled by the vertical dimension W, which can be made small. However, due to the reduced dimensions of the W to make the diode faster, it is difficult to efficienctly couple the light. Another kind of PD used in optical communication at low speeds is the avalanche photodiode (APD). In these PDs and extra p-layer is inserted to provide optical gain by avalanche multiplication of the electron-hole pairs. APDs feature much higher responsivity than pin PDs but at the expense of more optical noise (excess noise factor); they also require much higher bias voltages to sustain the avalanche multiplication.

2.1.2 Optical modulator

On the Tx side, laser diodes with external modulation are typically used as the optical source for high-capacity and long-span transmission systems. The optical intensity of the semiconductor laser can be modulated internally, via the bias current (direct modulation). However, turning the laser on and off creates electrical and thermal stress, frequency chirp (i.e. output frequency varies with time) and reduced operational lifetimes. In addition, direct modulation of a laser induces oscillations on the rising edge of the pulse (relaxation oscillation) which limit the maximum modulation frequency, typically ranging from 1 to 10 GHz for a vertical cavity surface emitting laser (VCSEL) [15]. These impairments are mitigated by external modulation, where the laser diode is biased to produce a continuous wave (CW) output (i.e. unmodulated) and an external optical modulator placed next to the laser converts the CW light into a data-coded pulse train with correct modulation format. Furthermore, in this way a single light source can feed multiple channels via individual modulators, reducing the power budget of the system.

External modulators are made of materials whose optical properties can be modified by an applied external electrical field. In electro-absorption (EA) modulators, carrier injection is used to induce absorption, which directly modulates the intensity of a propagating mode. These modulators are thus not a suitable choice when simultaneous phase modulation is desired, as in coherent applications. Control over the refractive index of the modulator material can be used to shift the relative phase of two propagating waves such that constructive or destructive interference is produced. This is the principle used in Mach-Zehnder modulators (MZMs) which will be explained in detail in the following section. Alternatively, if a resonant structure is implemented, the change in the refractive index will induce a change in the resonant condition, thus allowing the device to be switched between on- and off- resonance states at a given wavelength. Such devices are called ring-modulators [16]. Although they allow for very compact sizes, they are functional only on a very narrow band, around 100 pm, compared to MZMs, which feature optical bandwidths of more than 20 nm. Narrowband devices are very sensitive to fabrication tolerances and temperature variations, which limits their application. Thus, MZM interferometers are the most commonly used optical modulators in practice, permitting simultaneous phase and amplitude modulation and featuring broad optical bandwidth and zero or tunable frequency chirp [17].

2.2 Mach-Zehnder modulator

A MZM is an interference-based optical modulator in which the phase difference between two arms is controlled by an external electrical signal and transformed into amplitude modulation due to the interferometric principle. The block diagram of a standard MZM is depicted in Figure 2.2. The incoming light is coupled into the input waveguide of the modulator and split into two equal parts with the help of a coupler (typically a multi-mode interference (MMI) coupler) and then routed into two waveguides. The two light beams travel through the active areas of the modulator. These active areas are structured as p-n junctions which under reverse bias conditions deplete the waveguide of carriers causing a change in the refractive index and absorption. It is here where the interaction between the electrical signal and the optical wave

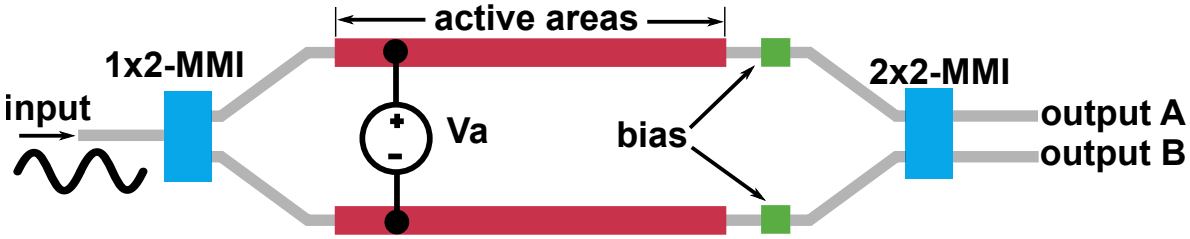


Figure 2.2: MZM block diagram.

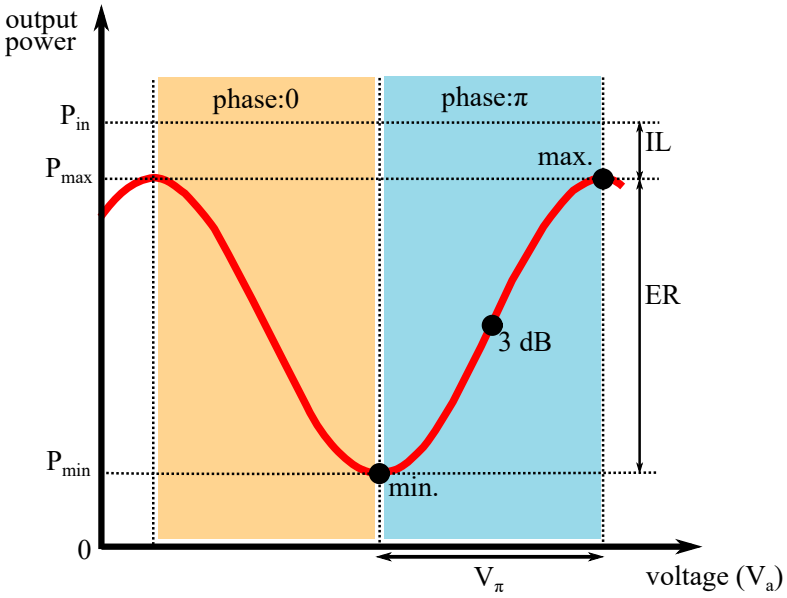


Figure 2.3: MZM power transfer function and most common bias points. Depending on the selected modulation format, the modulator is biased in either the 3 dB or the min. point.

occurs and the relative phase difference is generated in accordance with the applied external voltage V_a. In the last step, the light is recombined using again an appropiate interference structure where the two incoming beams interfere with each other. When the differential phase shift between the two arms equals $\pm\pi$, destructive interference occurs, corresponding to the "0" or off-state for the modulator, delivering no light at the output. Conversely, if the relative phase between the two arms is 0° constructive interference will occur, and the output intensity will ideally be the same as that at the input. Between these two cases, the output intensity will vary in accordance with the difference in phase between both arms. In this way phase modulation is turned into intensity modulation [17].

The field applied to the active waveguides induces a change of the material refractive index which is proportional to the field's amplitude and therefore, to the applied voltage V_a. The voltage required to induce a π phase shift across a phase shifter of length L is known as the V_π. The product $V_\pi L$ determines the E/O modulation efficiency, and is an intuitive metric to compare designs. This product depends on several design parameters, including those that directly affect the overlap between the optical and the electrical mode, e.g. the intrinsic region thickness (IRT) and the junction materials. In order to obtain high efficiency, the $V_\pi L$ product should be minimized. Therefore, an efficient MZM requires a shorter active length than a less efficient one, for the same voltage. Similarly, when the active length has already been fixed, a more efficient modulator will require a lower drive voltage to achieve full modulation depth.

The power transfer characteristic of the MZM is depicted in Figure 2.3. It is a non-linear function, leading to a strong dependency of the modulator behavior on the selected operating (working) point. The operating point of the modulator will be chosen in accordance with the targeted modulation format and is adjusted through the bias section of the modulator. This bias section is connected to an external DC voltage. For example, for amplitude modulation the MZM is typically biased in the middle of the linear region (i.e. at the 3 dB point or quadrature point), and driven with an electrical signal of limited amplitude. This ensures that the non-linear extremities of the transfer function are not reached and no distortion of the modulated signal is introduced. Further influences of the working point in the modulation format will be explained later. Apart from the $V_\pi L$ product, the performance of the MZM is quantified also with the insertion loss (IL) and the extinction ratio (ER). The IL of a MZM is defined as the ratio between the maximum optical power guided to the output P_{max} and the optical power fed at the input P_{in}, and it provides a measure of how much light is lost. The losses are caused by passive effects such as reflection, absorption and mode-coupling losses, and contribute to the link budget. The ER expresses the modulation depth of the device and is defined as P_{max}/P_{min}, where P_{min} is the optical power level seen at the output when the MZM is in the off state.

Small, high-efficiency and high-speed MZMs with low optical losses are available with III-V materials. In particular, InP modulators exhibit a smaller footprint and a lower driving voltage with respect to polymer and $LiNbO_3$ counterparts [18]. Emerging SiPh MZMs show lower performance in terms of efficiency and achievable bandwidth, although recent developments have also demonstrated high-speed capability [19, 20]. In this work, both InP and SiPh MZMs have been explored for the implementation of different Tx modules. Their particular characteristics and electrical equivalents are described in greater detail in Chapter 3.

2.2.1 MZM driving: electrode configurations

MZMs are commonly driven in the so-called push-pull configuration in order to achieve chirp-free operation [17]. This applies to two-path interferometric devices in which the two arms are driven in antiphase (i.e. V_1=-V_2, with V_1 and V_2 being the voltages applied to each arm of the modulator), keeping the phase of the optical output constant. In this way, the MZM renders itself naturally to differential driving configurations (V_a= V_1-V_2). The differential modulating signal is applied to the modulator through the electrodes which are deposited over the optical waveguide. As mentioned previously, the electrodes or active areas are p-n junctions operated in reverse bias condition which can be modelled by the junction capacitance. Several electrode configurations have been developed to electrically drive the MZMs at high speeds. Those can be broadly categorized into:

a. Driving the whole modulator as a lumped element, as it is the typical case for resonant ring modulators [21] or very short MZMs.

b. Driving of travelling-wave-electrode (TWE) MZM [22].

c. Driving of segmented Mach-Zehnder modulators (SEMZMs) [23, 24].

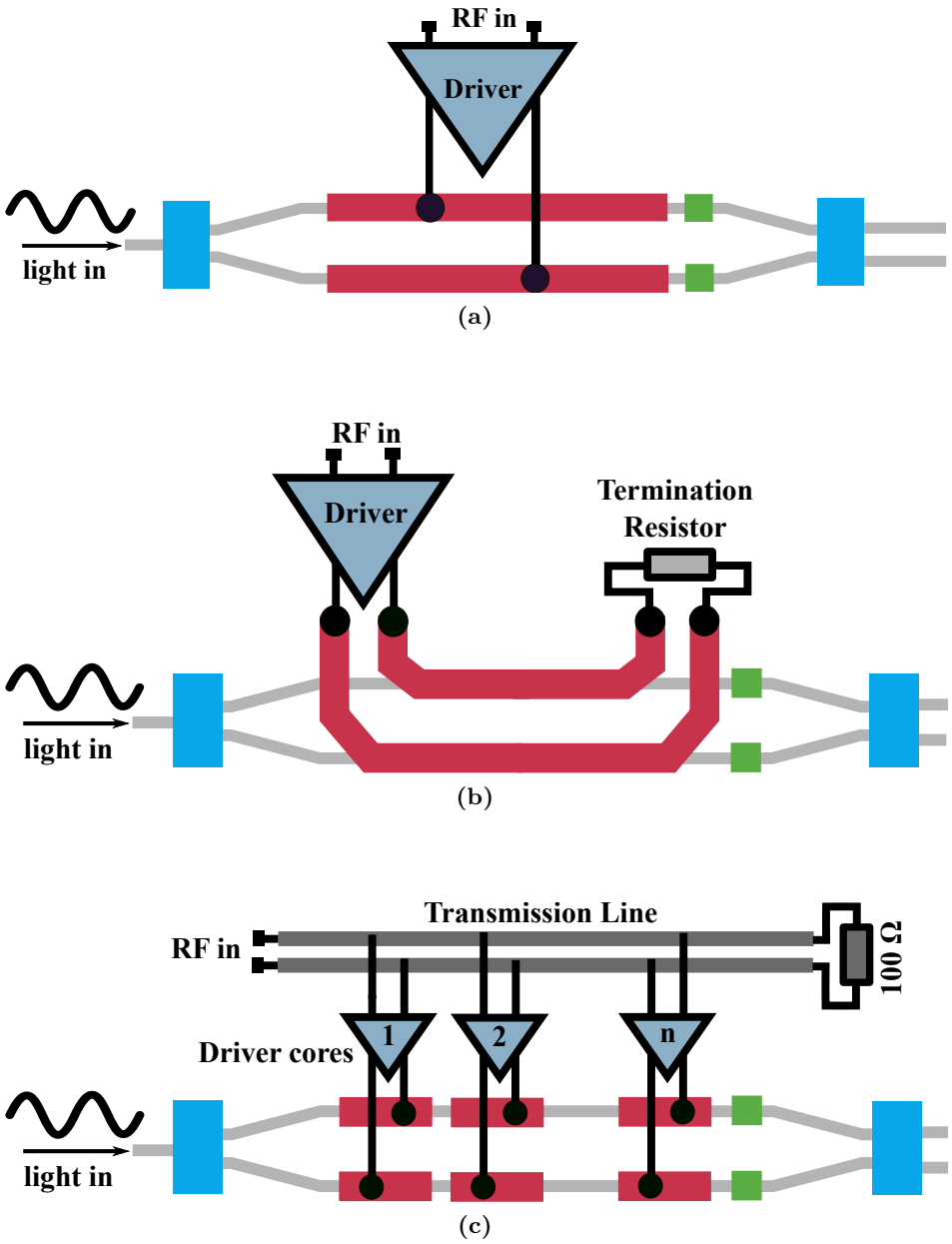


Figure 2.4: MZM driving schemes: (a) lumped electrode, (b) TWE and (c) SEMZM.

The lumped element configuration (Figure 2.4a) requires the modulator to be very short in order to satisfy the lumped condition up to reasonable frequencies ($L \sim \lambda/10$, with λ being the wavelength corresponding to the maximum targeted RF operating frequency). Therefore, for the same $V_\pi L$ product and comparable frequency of operation, this approach requires low L and high driving voltages that are difficult to achieve; thus obtaining high ERs and high operation speeds becomes challenging. High-speed modulators are commonly driven following the TWE approach (Figure 2.4b), as an evolution from the precedent lumped devices. In this configuration, instead of a large lumped capacitance, the capacitive load is distributed along a transmission line that transforms the reactive (capacitive) behavior of the modulator into a resistive behavior. This line is driven from one end, and it is electrically modeled by a resistor equivalent to the characteristic impedance of the line (Z_0, typically 50 Ω). In this way, the modulators can be made longer, and for the same $V_\pi L$ product they require lower driving voltages. The bandwidth of such a structure is limited by its RC constant. For long

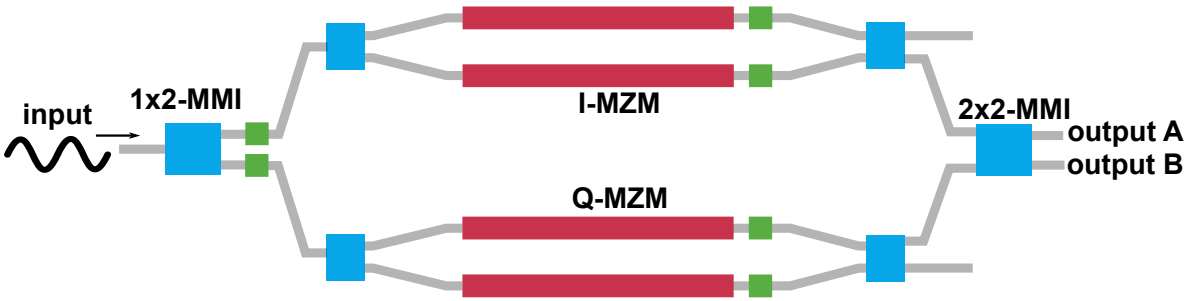


Figure 2.5: IQ-MZM block diagram.

modulators, the performance is also degraded as the parts of the line that are further away from the launching end of the electrical signal are less efficient due to the RF losses. For high speeds, accurate velocity matching of the electrical and optical signal paths must be satisfied: The electrical signal must propagate in the same direction and at precisely the same speed as the optical wave, permitting the phase modulation to accumulate monotonically regardless of frequency. For the TWE approach, with increasing frequency and modulator length, velocity mismatch may cause phase walk-off between the two arms resulting in the cancellation of initial modulation by subsequent anti-phase modulation [25] and ultimately in bandwidth reduction. High-frequency signals suffer also from larger losses while travelling through the TWE. To address these issues, the segmented modulator approach (Figure 2.4c), has been proposed [23]. In the SEMZM, the modulator is divided into segments, small enough to keep their physical dimensions well below a wavelength of an electrical signal travelling down the line. The electrical equivalent of each lumped segment is given mainly by a capacitance, which is then directly driven by a dedicated driver core. Each driver core senses its input voltage from the signal travelling along the transmission line. Ideally, with this scheme the same voltage can be effectively applied along the whole of the modulator length, since this configuration allows for re-generation (loss compensation) of the high-frequency data signal that has been attenuated by travelling through the line. Thus, the length of the modulator L, can be extended beyond limitation, rendering lower required driving voltages. Moreover, having the delay under control on the driver side, velocity matching between optical and electrical waves can be guaranteed, increasing the total performance of the modulator chip. With this approach RF and electro-optic design are effectively decoupled: the transmission line is isolated from the modulator and can be independently designed and optimized considering the constraints from the electrical side. This is the configuration used in this work; in Chapter 3 the role of the number of segments and its relation to the driving voltage, maximum speed and power dissipation is analyzed.

2.2.2 High-order modulation formats generation

Emerging technologies for long-haul and telecom links make use of high-order modulation formats, in combination with coherent detection and digital signal processing (DSP). With coherent detection, all parameters of the optical field (amplitude, phase and polarization) are available in the electrical domain, allowing for the detection of arbitrary modulation formats and constellations. Furthermore, the preservation of the temporal phase enables the use of DSP for the effective compensation of the fiber impairments, i.e. the chromatic dispersion,

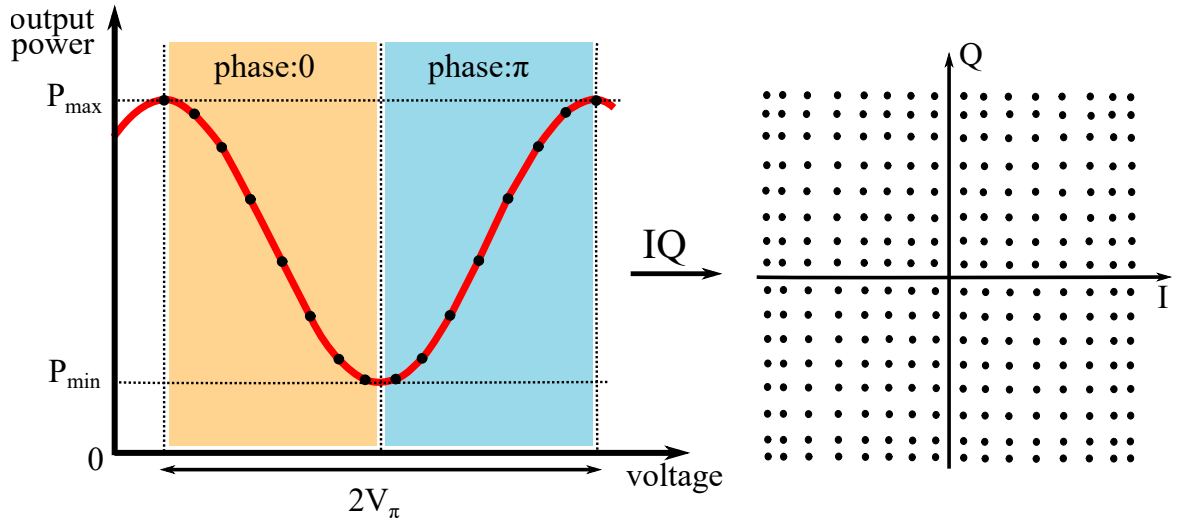


Figure 2.6: Generation of 256-QAM with I/Q-MZM. Adapted from [30].

polarization mode dispersion and nonlinearities, permitting the system to operate closer to the ultimate limits of spectral efficiency. On the other hand, when employing these advanced transmission schemes, the complexity of the Txs and Rxs increases, and also higher hardware costs have to be weighed in [26, 27]. The power dissipation required for signal processing contributes significantly to the overall energy requirements of the transceiver, and can reach up to 50% of the total consumption [28]. Due to these reasons, in datacom links direct detection techniques are preferred.

Optical high-order modulation formats can be generated by many different transmitter configurations, whereby, the optical complexity can be reduced through increased electrical complexity and viceversa [29]. By operating the MZM in a dual-drive mode, applying signals to both arms, quadrature-amplitude-modulation (QAM) signals can be generated. However, in this case the modulator is not driven in push-pull fashion, which causes significant chirping of the optical signal and will reduce its performance. A single MZM can be used to modulate the amplitude or the phase of the optical signal. For concurrent multi-amplitude and multi-phase modulation, nested MZM structures, also referred to as "I/Q-MZM", are typically used [30]. The block diagram of such an I/Q-MZM is depicted in Figure 2.5. The I/Q-MZM is composed of two parallel MZMs sharing a single optical input and a single optical output. The two modulators are referred to as the children, while the I/Q ensemble is referred to as the parent. Before and after the children, additional MMIs are inserted to serve as splitters and couplers, respectively. Additionally, the second MMI introduces a phase shift of $\pi/2$ for one of its inputs and thus ensures orthogonality between both branches. Residual undesired phase differences between the two children signals are compensated, thanks to an additional biasing section inserted at parent level [30]. Both children are driven with multilevel signals, which are multiplexed by the parent generating the I/Q signal which transports information in both its amplitude and phase without requiring additional bandwidth. This is the preferred method for generating QAM signals. A convenient representation of amplitude and phase modulated signals can be obtained via the constellation diagram. This diagram results from combining the information contained in the I- and Q- signal symbols on a complex plane, as seen in Figure 2.6. Higher-order modulation schemes are associated to diagrams that are more

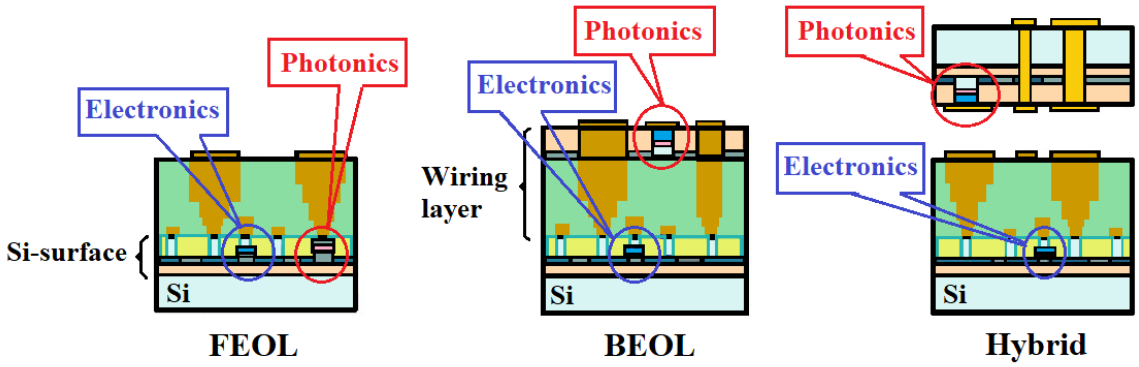


Figure 2.7: Schematic cross sections of integration between photonic and electronic circuits. Adapted from [33].

crowded with a larger amount of information conveyed by each constellation point (i.e. the number of bits per symbol). I/Q modulators are biased in the minimum point and typically driven with $2V_\pi$ in order to maximize ER, although the entire complex plane can be covered also with arbitrarily small driving voltage swings. Figure 2.6 represents the generation of a 256-QAM format with an I/Q modulator: on the left side, the characteristic of a single MZM (children) with 16 states divided into two groups of 8 intensity levels is represented; on the right side the corresponding constellation diagram is plotted. The constellation points are unequally spaced because of the non-linearity of the MZM transfer function, when driven with full swing.

Another approach for the generation of QAM signals involves placing two I/Q modulators in sequence, in order to create a "tandem I/Q modulator". By driving each of them with binary signals and underdriving one of them by 6 dB, a QAM-16 signal can be generated [31]. Alternatively the I/Q modulators can be placed in parallel and the output of one of them can be attenuated by 6 dB [32]. These methods require only binary driving signals, shifting the complexity from the electrical to the optical domain.

2.3 Photonics and electronics integration schemes

There are two types of integration methods for merging photonics with electronics: hybrid integration and monolithic integration, which can be done either in the front-end-of-line (FEOL) or in the back-end-of-line (BEOL). Their schematic representation is depicted in Figure 2.7.

In the hybrid integration approach, electronic-only chips are combined with photonic-only chips. This enables to individually choose the best-performing devices from any available technology, and to design, fabricate and test them separately before the final assembly. This scheme can improve product yields and does not suffer from interference between the electronic and photonic devices during the manufacturing. Thus, the integration challenge is low and can stimulate horizontal specialization. However, the flexibility in picking the best devices can be hindered by the lack of a proper design kit which allows opto-electronic co-simulation to ensure best combined performance. Moreover, the assembly effort and cost are high and the assembly-induced parasitics (wire-bonds or flip-chip bumps, additional pads and ESD protection) can dominate and limit the overall performance.

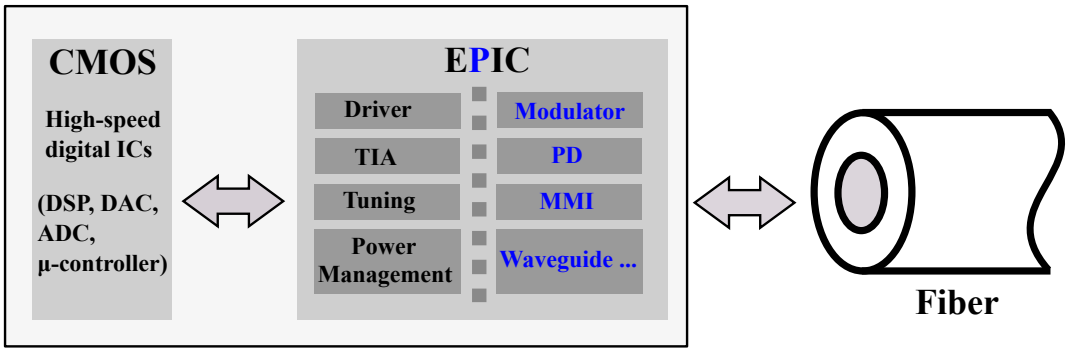


Figure 2.8: Multi-chip solution for optical communications link with EPIC [34].

In contrast, in a monolithic integration approach there are no double manufacturing and assembly efforts, lowering the costs per system. In BEOL integration, also called zero-change approach, the photonic circuits are integrated on the wiring layer by a back-end process. Although this scheme has been demonstrated in unmodified state-of-the-art CMOS [35], the photonic devices show only poor performance, due to the higher design constraints. In FEOL both electronic and photonic chips are integrated near the surface of a silicon substrate by a front-end process. This allows for shortest possible interconnects between photonics and electronics, leading to best high-speed performance and shrinking form-factors. However, this approach requires very strict compatibilities such that the additional fabrication steps for the photonic devices do not impact the underlying electronic baseline process. This leaves only little room for optimization of the devices and provides low flexibility for the integration of new devices or adaptation to other more scaled baseline technology [34].

Independently of the chosen integration approach, communication systems will require high-speed digital circuitry to implement DSP, digital-to-analog converters (DACs) etc., typically realized in highly scaled CMOS technologies, making multi-chip solutions inevitable. However, in monolithic integration, only the assembly of a suitable CMOS chip with an electronic-photonic-integrated-circuit (EPIC) chip is required, without passing RF signals through the chip-to-chip interconnects, as depicted in Figure 2.8. In contrast, the hybrid approach requires the assembly of the photonic with the RF electronics plus the digital CMOS chip incurring in additional assembly effort and packaging complexity.

2.4 Technology platform

The choice of semiconductor technology is inseparable from the intended application and circuit design requirements. On the Tx side, to encode the optical carrier reliably, drivers capable of high-speed broadband operation while delivering large output swings are required. On the Rx side, devices featuring low-noise and high-speed are desirable. Commercial products are typically implemented in III-V compound semiconductor technologies such as gallium arsenide (GaAs) [37] and indium phosphide (InP) [38], which provide very high performance, but are not suitable for cost-sensitive mass-market applications. For lower-cost implementations in silicon, two major options remain: CMOS and SiGe. CMOS provides advantages in terms of cost and low power dissipation, however, at a comparable lithography node they feature

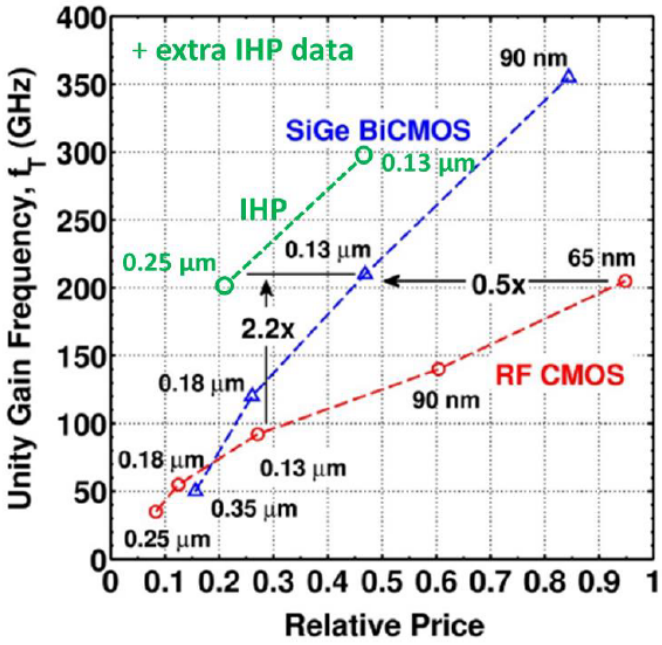


Figure 2.9: Comparison between BiCMOS and CMOS technologies with respect to RF performance vs. cost [36].

lower breakdown voltages and worse noise characteristics than SiGe HBTs, which significantly penalizes circuit performance [13]. The integrated circuits (ICs) presented in this work are all implemented in different nodes of the IHP SiGe BiCMOS platform, which provide a good trade-off between high-frequency device performance and manufacturing costs as seen in Figure 2.9. Compared to RF CMOS where a unity gain frequency f_T of about 200 GHz is achieved in the 65 nm node, the same value is reached in SiGe BiCMOS already in the 250 nm node. Hence, for the same RF performance the fabrication costs are lower. At the same price, SiGe BiCMOS offers more than double the RF performance compared to RF CMOS [39]. Moreover, although the CMOS part provides only modest speed, digital IP blocks allow for convenient implementation of complex control and tuning circuitry on-chip.

The availability of such advanced BiCMOS technologies facilitates the design and demonstration of leading-edge circuits operating at unprecedented speeds. Moreover, the higher operating speed can be traded-off for lower power dissipation or other performance metrics. The characteristics of the different IHP processes used to implement the devices presented in this thesis are described in the following.

SG13S and SG13G2 The SG13S [40] and SG13G2 [41] processes are state-of-the-art 0.13 μm BiCMOS technologies featuring very high RF performance with f_T/f_{max}=250/340 GHz and f_T/f_{max}=300/500 GHz, respectively. The SG13G2 process is not yet qualified, and is therefore susceptible to experiencing larger deviations from the model predictions. Both processes have an available back-end of line stack of seven metal layers, including MIM capacitors. Five thin metal layers are based on 130 nm design rules and two top metal layers with 2 μm and 3 μm thickness, are suitable for RF passive components design.

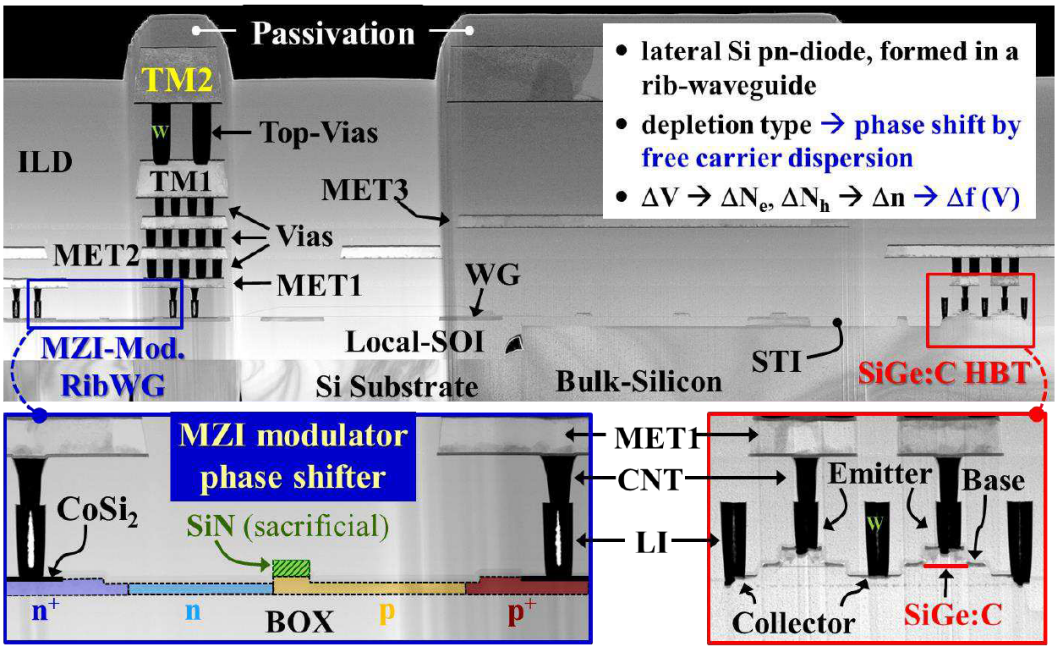


Figure 2.10: Photonic BiCMOS cross-sections illustrating monolithically integrated transmitter components: Phase-shifter of a Mach-Zehnder interference modulator on SOI and a SiGe HBT fabricated in an adjacent bulk region [34].

Parameter	SG13S	SG13G2	SG25H4-EPIC	SG25H3P (npn / pnp)
peak f_{max}	340 GHz	500 GHz	190 GHz	180 / 120 GHz
peak f_T	250 GHz	300 GHz	190 GHz	110 / 90 GHz
BV_{CEO}	1.7 V	1.7 V	1.9 V	2.3 / -2.5 V
BV_{CBO}	5 V	4.8 V	4.5 V	6 / -4 V
β	900	650	270	150 / 100
MIM capacitor	1.5 fF/µm²	1.5 fF/µm²	1 fF/µm²	1 fF/µm²
n^+ poly Resistor	-	-	210 Ω/□	210 Ω/□
p^+ poly Resistor	250 Ω/□	250 Ω/□	280 Ω/□	280 Ω/□
area price /mm²	6300 €	7300 €	6600 €	5800 €

Table 2.1: Performance parameters of different technology processes.

SG25H4-EPIC The SG25H4 EPIC from IHP is a new monolithic EPIC technology [34] which combines high-performance BiCMOS technology with high-speed photonic devices. The photonic devices such as waveguides, modulators and Ge photodiodes are realized in the FEOL, at the same level of the transistors. The baseline BiCMOS technology for photonic integration is a 250 nm technology featuring f_T/f_{max}=190/190 GHz and five metal layers, with two thick top metals for passives design. Initially an 8 inch silicon-on-insulator (SOI) wafer with a top Si layer of 220 nm and a buried oxide (BOX) layer of 2 μm is used. Then a module called "local SOI" is implemented in the process flow to produce SOI and bulk regions located close to each other [42]. The SOI areas are used for the fabrication of the photonic components, while the electronic devices are formed on bulk Si regions. In Figure 2.10 the core devices of a monolithically integrated Tx are shown: The phase-shifter of a MZM on SOI next to the SiGe HBTs on bulk-Si.

SG25-H3P The SG25-H3P belongs also to the 250 nm technology family of IHP and provides complementary pnp and npn transistors with matched performance [43], featuring f_T/f_{max}=110 GHz/180 GHz for the npn and f_T/f_{max}=95 GHz/140 GHz for the pnp transistor, respectively. The layer stack comprises five metal layers, with two thick top-metals for passives design. As will be demonstrated in Chapter 5, the availability of both npn- and pnp-type transistors in a complementary BiCMOS process is a promissing route to applications that demand simultaneous low-power and high-speed performance.

The parameters of the different processes are compared in Table 2.1.

2.5 Circuit design considerations

Similarly to what the RF design paradigm experienced in the early 1990s, in the optical domain also modular, general-purpose building blocks are being replaced by end-to-end solutions that benefit from device/circuit/architecture co-design. However, optical systems are different from RF systems in many aspects, and issues such as the random nature of data, the broad spectrum of signals and the existence of very low frequency components demand specific circuit techniques [44]. In this section, fundamental design aspects of broadband high-speed analog ICs for optical communications are discussed, which allow to better extract the whole potential of the advanced SiGe:C HBT technologies. The techniques described in the following are then used for the implementation of the MZM modulator drivers and transimpedance amplifier (TIA) designs described in the subsequent chapters.

2.5.1 Broadband circuit design

Optical communication circuits need to work from nearly DC (∼30 kHz) up to a very high corner frequency. This requirement for broadband operation comes with some restrictions for the circuit design:

1. Transistor loads need to be resistive: stages with inductive loads have no gain at DC and active loads typically have insufficient high-frequency properties as they make use of slower p-type devices.

2. DC-coupling between stages is required since DC blocks with sufficiently low cut-off frequency are too bulky to be integrated on-chip.

3. It is recommended to apply the principle of strong impedance mismatching between succeeding stages (transimpedance (TIS)-transadmittance (TAS) principle) [45]. This reduces the influence of parasitic capacitances as well as the influence of the strongly frequency-dependent input and output impedances of the different stages, resulting in a higher cut-off frequency. Emitter followers in between stages are often used for this decoupling purpose [45].

Few combinations of standard stage topologies will satisfy these requirements, and the challenge will be to make use of suitable circuit techniques in order to extend this limited solution-space and meet the performance goals.

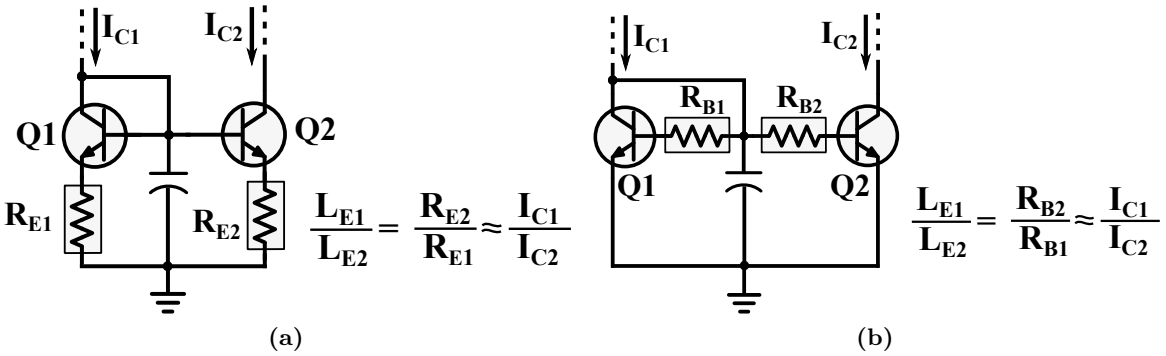


Figure 2.11: Biasing scheme with current mirrors: (a) with emitter degeneration resistors and (b) with base resistors.

Biasing: Biasing of the IC stages is based on constant current sources implemented with typical current mirror structures, which accurately replicate the current from a stable reference. This results in superior insensitivity of circuit performance to variations in power supply and temperature. Emitter degeneration, as depicted in Figure 2.11a is used in the current mirrors in order to improve the current matching and to boost the output resistance [46]. The voltage drop in these resistors its typically selected as $\sim 10 \times V_T$, thus $\sim 250\,\mathrm{mV}$. Alternatively, if there is no headroom available to accommodate the degeneration resistors, large resistors can be added to the bases of transistors as in Figure 2.11b. This works in a similar way, improving the mirroring matching and serves also to mitigate possible signal leakage or disturbances thanks to the low-pass filtering effect created with these resistors and the capacitors placed at the base connection.

Differential signaling: All the circuits presented in this thesis are differential, offering a number of important advantages over their single-ended counterparts. Differential signals result from the transmission of pairs of balanced signals, with identical amplitude but opposite polarity. Any external disturbance will affect both signal paths equally. As the information is coded in the difference of the transferred signals, equally coupled signals are suppressed as a common-mode disturbance. Thus, differential circuits feature improved immunity to supply and substrate noise and superior rejection of parasitically coupled signals. They are also immune to supply and ground inductance, featuring reduced crosstalk and instability problems which also allows for simpler mounting techniques and more robust designs. Even-order harmonics are inherently reduced, rendering lower distortion. Moreover, compared to single-ended stages, they only need half of the voltage swing accross the load resistors, which translates into steeper pulse edges and higher achievable data rates with improved eye diagrams [45].

In terms of circuit design, two main provisions need to be made to achieve differentiality: both signal paths need to be as equal as possible and the circuit may only amplify the differential signal, i.e. the common-mode needs to be suppressed as best as possible. Thus, any stage of an amplifier circuit needs to be composed of two identical transistors, one in each signal path and those transistors need a common reference point which is identical to the common mode of the input signal. Differential pairs and derived cells meet these requirements: As seen in Figure 2.12a, the reference of both transistors is the floating base node and if the tail current source is ideal, the differential pair features infinite common-mode rejection. The

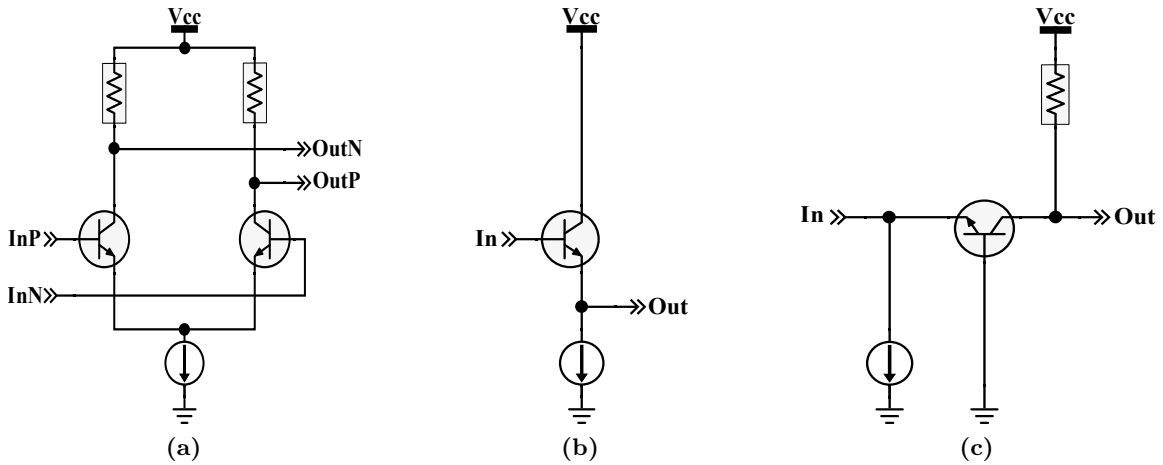


Figure 2.12: Basic transistors stages: (a) differential pair, (b) common-collector stage and (c) common-base stage.

other two basic topologies, collector and base stages, depicted in Figures 2.12 b and c, can also be used in differential amplifier designs, with the reference node being (small-signal) ground. However, they amplify the common-mode signals and thus, the common-mode must then be effectively suppressed in other stages such that on-chip common-mode disturbances are avoided [47].

Broadband matching: Reflection of electromagnetic waves occurs due to changes in the characteristic impedance of the propagating medium (Z_0). Such reflections are unwanted in high-speed systems, since they increase the timing jitter, signal distortion and even cause instability. These problems can be overcome by approximately matching both ends of the link or by exactly matching one end only. The first measure is preferred at high operating frequencies, even though it increases power dissipation, since the second method cannot be realized with enough accuracy [48]. In terms of circuit design requirements, this means that all input and output impedances need to be as close as possible to the standard 50 Ω impedance of the outer world. It is worth noting that this requirement applies to the input of the driver and the output of the TIA, since the other interfaces are connected to the E/O components (namely the SE-MZM and the PD), which are high-impedance lumped elements. Typically, it is required that the magnitude of input and output reflection coefficients (S11 and S22) is lower than -10 dB over the operating bandwidth, which means that the reflected wave is smaller than 0.1 times the amplitude of the incident wave [49]. Due to the stronger influence of the parasitic elements at the higher frequencies (specially in the output transistors driving the 50 Ω load, which are big in size), ensuring broadband matching over the entire (ideally large) bandwidth is not trivial, and it requires significant design effort. Inductive peaking can be effectively used for broadband matching up to very high frequencies, as will be described in the particular IC implementations.

2.5.2 High-speed design techniques

In the following, different techniques for maximizing the high-speed performance of broadband circuits are reviewed.

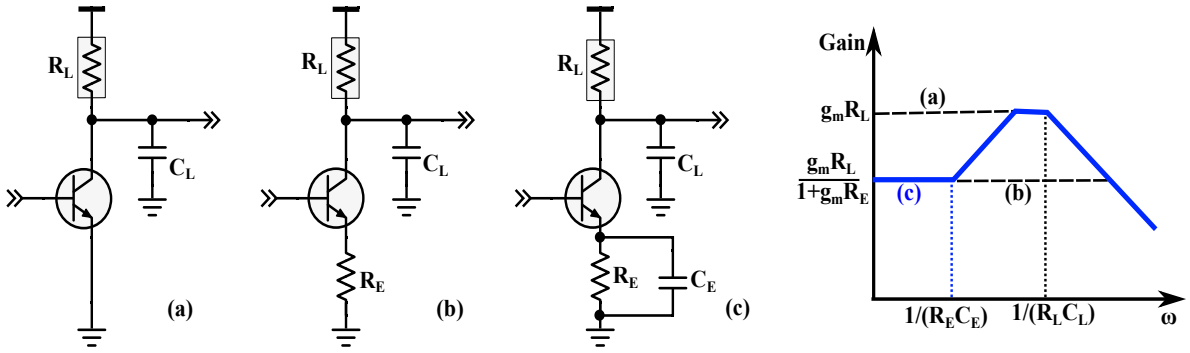


Figure 2.13: Series feedback implementation: (a) typical common-emitter stage, (b) common-emitter stage with resistive degeneration, (c) common-emitter stage with resistive-capacitive degeneration, (d) transfer function.

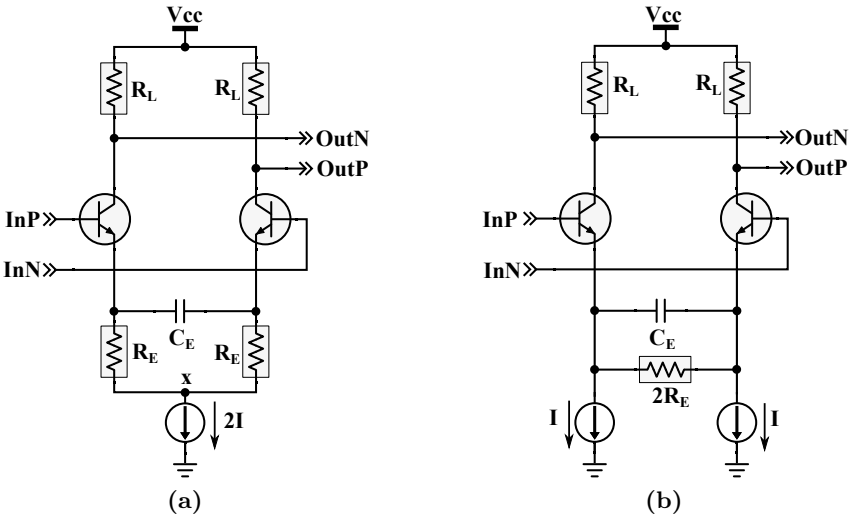


Figure 2.14: Capacitive emitter degeneration implementation in a differential pair: (a) in series and (b) parallel configuration.

Series feedback with capacitive emitter degeneration: Series feedback, as illustrated in Figure 2.13, is a well-known technique used to speed up the input pole created by the base resistance and the base-emitter capacitance (C_{BE}) by a factor of $(1 + g_m R_E)$. The low frequency gain also drops by the same factor which is why this technique is also used to increase the amplifier linear dynamic range. Moreover, R_E introduces a new high-frequency pole into the transfer function, which, if left uncompensated reduces the bandwidth of the stage. This pole can be compensated by adding the emitter degeneration capacitor C_E in parallel to the resistor, as indicated in Figure 2.13, which adds a zero at $f = \frac{1}{2\pi R_E C_E}$. This zero can be set independently of the gain to a low frequency where it cancels out the first pole of the stage, extending the bandwidth (this is known as emitter peaking). C_E should not be made too large in order not to cause undersirable signal distortions.

In a differential pair, the resistive-capacitive degeneration can be implemented in series as in Figure 2.14a or in parallel, as in Figure 2.14b, where the current source is split in half, with a $2R_E$ resistor connected in between. The parallel configuration has the advantage of not requiring any headroom sacrifice to accommodate the resistor, however, as far as the noise is concerned, both current sources are uncorrelated, unlike in the series configuration where the current source provides a perfectly balanced scenario contributing only to the common-mode

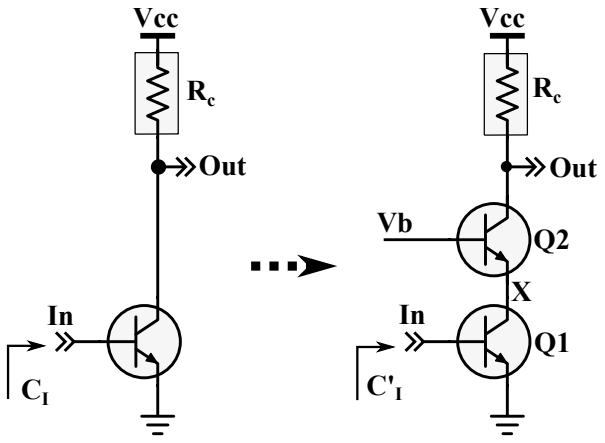


Figure 2.15: Common-emitter stage with cascode transistors [50].

noise. The series configuration produces a virtual ground in node X, at the common-point of the resistors, which isolates the noise from the current-source and ground connection.

Miller reduction with cascoding: According to the Miller effect, a feedback capacitance C across an amplifier with gain A contributes a capacitance equal to $(1 - A)C$ to the input capacitance. If the gain of the stage is negative, as in a common-emitter stage, then this expression becomes $(1 + A)C$. In a common-emitter stage, the total input capacitance C_I represented in Figure 2.15 is comprised of the base emitter capactiance C_{BE} and the Miller capacitance, which is the C_{BC}, multiplied by the gain plus one:

$$C_I = C_{BE} + (1 + A)C_{BC} \tag{2.3}$$

The Miller capacitance contribution can become very large, and severely limit the bandwidth. It can be suppressed by connecting the collector of the input transistor Q1 to a low impedance node, which effectively reduces the gain that multiplies C_{BC}. This can be done, by stacking the cascode transistor Q2 on top of the main transistor Q1. The input impedance of the emitter of Q2 is given by $\sim \frac{1}{g_{m2}}$, thus the voltage gain from the input to node X reduces from $A \approx g_{m1}R_C$ to $A_X \approx g_{m1}/g_{m2} \approx 1$ and the input capacitance becomes only $C_I = C_{BE} + 2C_{BC}$. In addition to suppressing the Miller capacitance, cascoding provides other advantages: it increases the output resistance at the collector of Q2 and hence the stage gain, it improves the isolation between input and output and it can prevent the avalanche breakdown of Q1 by dividing its collector emitter voltage between Q1 and Q2. On the other side, it reduces the voltage headroom, requiring a higher operating voltage [50].

Negative capacitance compensation: The creation of a negative capacitance in parallel with the input capacitance of one stage effectively reduces its value as well. A negative capacitance can be created by exploiting the Miller effect, by connecting a regular capacitance C_N across a non-inverting amplifier with a gain larger than one ($A > 1$), as indicated in Figure 2.16a. In this way, the Miller capacitance $(1 - A)\, C_N$ is negative and the input capacitance C_I at each node is reduced to (2.4) [50]:

$$C'_I = C_I + (-A + 1)C_N \tag{2.4}$$

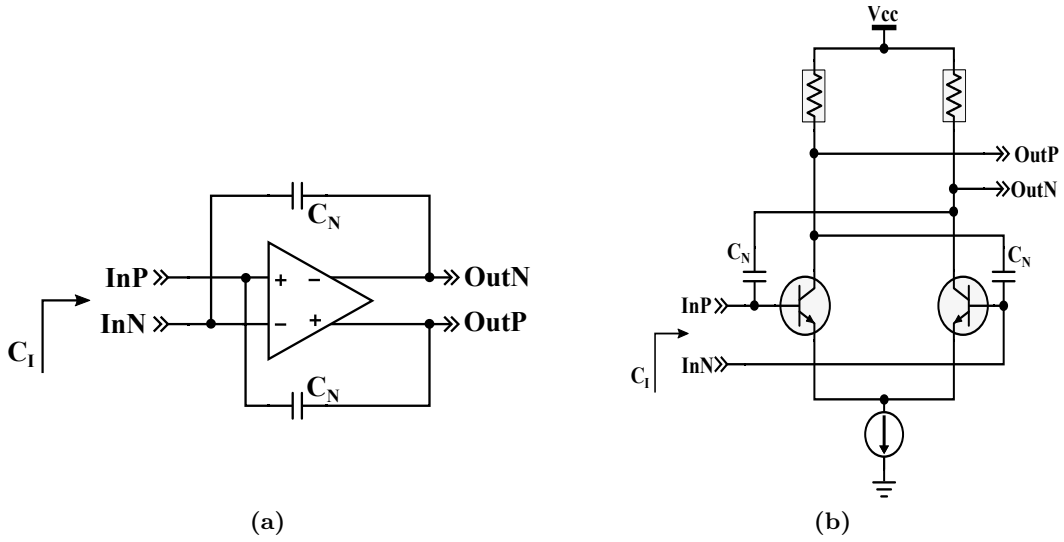


Figure 2.16: Negative Miller capacitance compensation: (a) concept and (b) implementation in differential pair.

where A is the gain of the stage. It is worth noticing that these capacitors provide positive feedback; if they are made too large, the overall capacitance at the input node may become negative, causing instability. In the differential pair implementation represented in Figure 2.16b, the C_{BC} capacitance of the transistors is multiplied by $(A + 1)$ due to the Miller effect and appears as part of the input. If C_N is selected $\sim C_{BC}$, the produced negative Miller will neutralize the effect of the parasitic C_{BC}. One limitation of this technique is the fact that at frequencies approaching the bandwidth of the stage, the amplitude of the output signal drops and its phase is no longer aligned with the input signal, which reduces the Miller capacitance. Moreover, the C_N represents an additional load at the output, which reduces the bandwidth of the stage [50].

Inductive peaking: This technique makes use of one or more inductors at a given node in order to compensate the node's capacitance, eliminating the bandwidth limitation due to the RC constant without consuming additional power. The upper limit for this technique will be imposed by the signal distortion caused if the capacitance is overcompensated. This method can be implemented in four main different configurations, depending on the number of inductors used: shunt, series, shunt-series and T-coil peaking [51, 49]. All of them are represented in Figure 2.17 in the order of increasing number of inductors, for a general common-emitter stage. C_T represents the parasitic capacitance of the transistor and C_L the load capacitance of the next stage.

In the shunt-peaking configuration, as depicted in Figure 2.17a, an inductor L_1 is connected in series with the load resistor R_L and partially tunes out the load capacitance $C = C_T + C_L$. At the frequency where the gain would roll-off because of the output pole ($\omega = 1/R_L \cdot C$) the load impedance starts to go up because of the inductive component ($Z(j\omega) = R_L + j\omega L_1$). Thus, the inductor introduces a zero in the transfer function of the stage extending the bandwidth [52]. The bandwidth extension can be also understood as a consequence of the inductor delaying the current flow to the resistance branch so that more current initially charges the load capacitance,

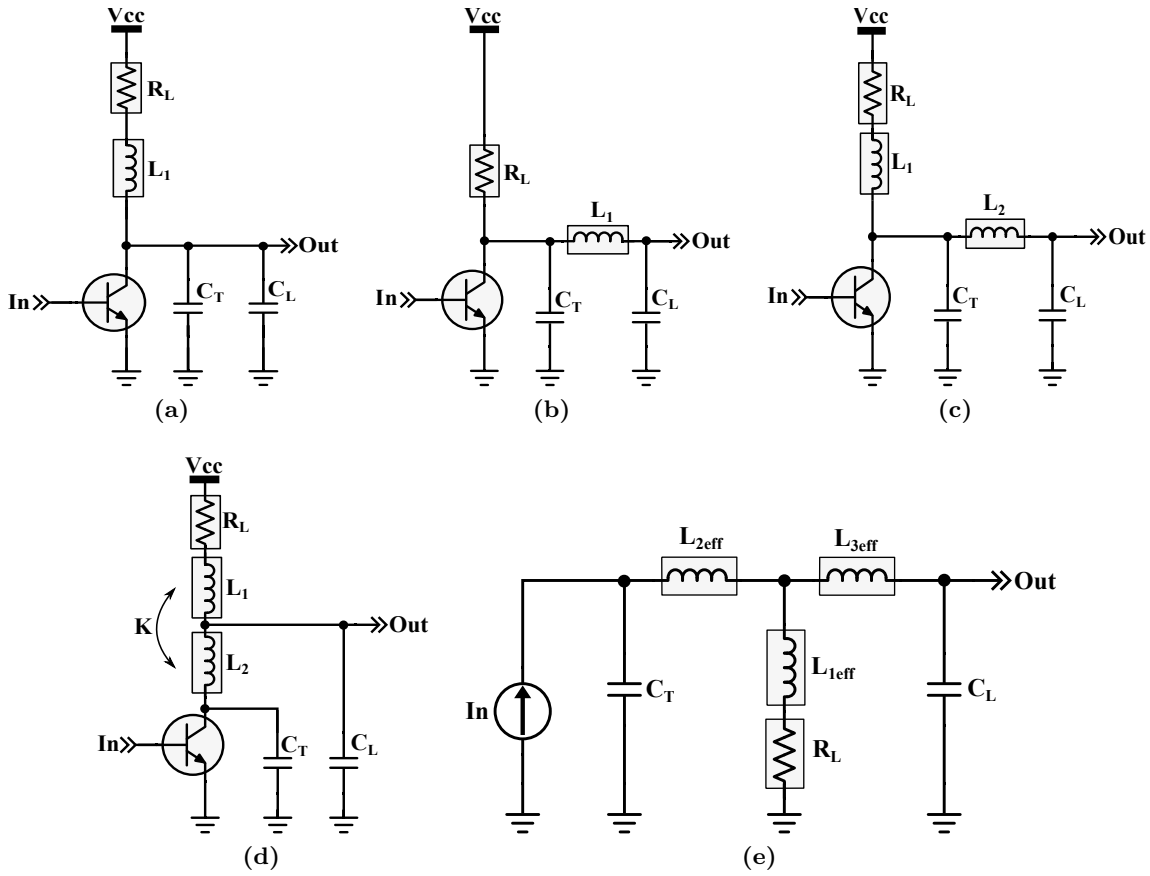


Figure 2.17: Different inductive peaking configurations: (a) shunt peaking, (b) series peaking, (c) shunt-series peaking, (d) T-coil peaking and (e) equivalent circuit model from T-coil peaking.

reducing the rise-time [53]. The position of L_1 can be changed and connected to the supply instead; this is preferred if shunt-peaking is used alone since its parasitic capacitance in this case does not add to the load capacitance. The series peaking configuration, represented in Figure 2.17b is another common method, which works similarly to the shunt peaking and also makes use of a single inductor. L_1 is used here to separate the load bound capacitances (C_L) from the transistor-bound capacitances (C_T). This configuration is more effective than the previous one, in designs where C_T is significant [54, 55]. Both techniques combined give rise to the shunt-series peaking configuration, as represented in Figure 2.17c, which can achieve bandwidth extension ratios (BWERs) as high as 3.5 for 1.8 dB peaking [56].

In general, while using more inductors leads to higher BWERs, the parasitic capacitances of these inductors, the additional delay and area may counteract the bandwidth improvement. The peaking structures must be chosen depending on the particular situation. The optimal peaking inductances can be chosen as $L = mR_L^2C$; the scale factor m is determined by the peaking configuration and the particular design goal. For shunt peaking, a factor of $m = 1/\sqrt{2}$ gives the maximum BWER of 1.84, with 1.5 dB peaking [57]. For a maximally flat gain response with this technique, m should be set to $m = 1/(1+\sqrt{2})$, but the BWER is reduced to 1.72 [52]. When the inductor is connected in series with the load resistor, the quality factor, which accounts for the different loss mechanisms, is uncritical and inductors with low quality factors of 5 or 6 provide good BWERs. However, its self-resonance frequency, given by $f_{SR} = 1/(2\pi\sqrt{LC_P})$, with C_P representing the parasitic capacitance of the inductor to the

substrate, limits its useful frequency range, and it should be approximately kept a factor of two above the stage bandwidth [50]. For the practical implementation, the initial values of the inductive structures are estimated with such formula, and are afterwards optimized with EM simulations, performed in ADS Momentum. Through the EM simulations, S-parameter models describing the behavior of all on-chip passives such as inductors, pads and transmission lines are produced. These S-parameter files are then included in the circuit simulator (i.e. Cadence Spectre).

T-coil peaking, as shown in Figure 2.17d is the most advanced method, and results in the highest BWERs [51, 52]. This method makes use of two coupled inductors, with coupling factor k, and the resulting negative mutual inductance M, as represented in the equivalent circuit of Figure 2.17e, where L_{1eff}=L_1+M, L_{2eff}=L_2+M and L_{3eff}=-M, with $M = k\sqrt{L_1 L_2}$. Depending on the particular capacitance distribution across the inductor network, symmetric ($L_1 = L_2$) or asymmetric ($L_1 \neq L_2$) T-coil peaking might be chosen. It has also been shown that if the transistor capacitance (C_T) occupies more than 40% of the total load capacitance, a similar T-coil network with the opposite polarity coupling coefficient (negative k, resulting in positive L_{3eff}) is more effective [53]. The coupling coefficient, k, can be theoretically chosen between 0 and 1, and in general the BWER is higher with higher k, although practical on-chip inductors can only feature k in the order of 0.8 [49].

3

Transmitter Modules with Integrated DAC Functionality

The classical approach for generating high-order modulation formats based on Mach-Zehnder modulators (MZMs) relies on fast linear driver amplifiers with direct interface to the external digital-to-analog converter (DAC) (recall Figure 1.5). Such an implementation can be very power hungry due to the requirements for linearity on the driver and the power consumption from the DAC module itself. More customized solutions with lower power dissipation while offering comparable resolutions are desired for those application areas such as datacom scenarios where these parameters are limiting factors. In this context, this chapter describes the design and characterization of transmitter (Tx) modules featuring 4-b digital to analog conversion performed in the optical domain. By supressing the need for the external DAC, this approach paves the way to new low-power, low-cost solutions with high spectral utilization and compact size.

3.1 Introduction

Different transmitter configurations for generating multilevel signals based on segmented Mach-Zehnder modulator (SEMZM) can be adopted. The classical implementation, as depicted in Figure 3.1a makes use of an external DAC module which combines the n- uncorrelated bit streams into a multilevel analog signal that is first amplified by the linear drivers and then fed to the MZM. This implementation offers a high-degree of flexibility on the system level, enabling pre-compensation in the digital domain with high-speed DACs with high-granularity which are readily available in the market. It also minimizes the number of high-speed tracks to the transmitter optical sub-assembly (TOSA). The major disadvantages in this approach are the additional cost from the DAC module and the high power consumption derived from the linearity requirements in the drivers and the power dissipation of the DAC itself, which can range up to several hundreds of mW [58]. In contrast to telecom links, the advantages of ditigal pre-compensation in datacom applications might not override the excess cost and increased power budget.

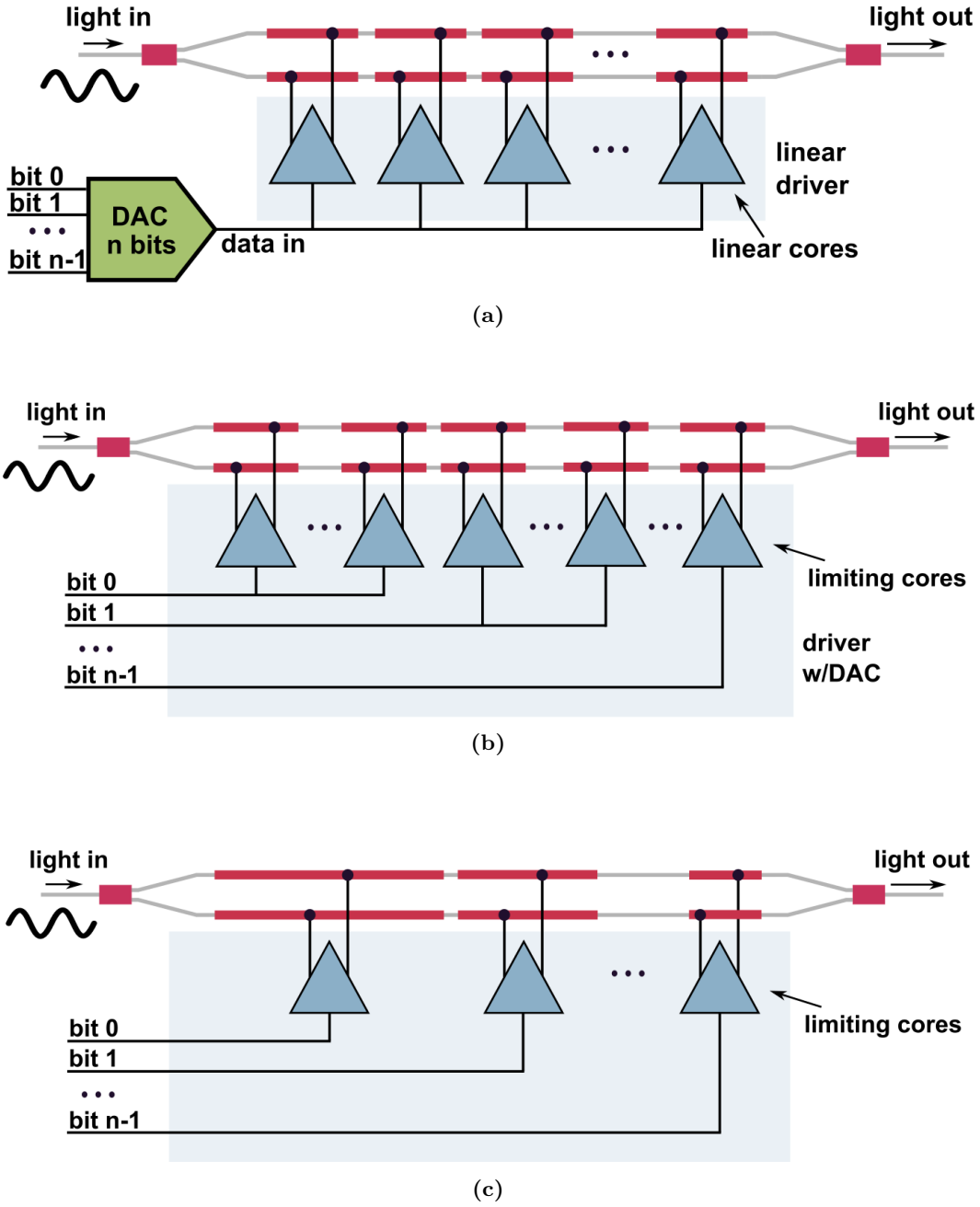


Figure 3.1: Transmitter configurations with SEMZMs: (a) linear driving approach, (b) driver with integrated n-bits DAC (c) modulator with thermocode-weighted segmentation.

Alternatively, by exploiting the segmented nature of the modulator, multilevel signals can be generaded without the need for external DAC. A SEMZM, inherently enables the so-called optical-DAC due to the capability of accessing every segment independently. As represented in Figure 3.1b, the integrated DAC functionality is realized within the driver chips through a wired binary-to-thermocode (B2T) encoder scheme and limiting cores. The driver chip takes in a binary n-bit word and encodes it into the $2^n - 1$ array of driver cores which are grouped in a thermocode-weighted fashion. Depending on the number of driver cores that are switched on at a given instant according to the input data stream, a different equivalent SEMZM active length will be contributing to the optical output. In this way, the effective interaction length is altered, resulting in a multilevel optical output. The driver cores are, therefore, required to

deliver only on-off-keying (OOK) stimuli, eliminating the requirement for amplifier linearity and paving the way for more energy-efficient topologies.

The encoder can also be built by constructing the modulator with segments of different (thermocode-weighted) lengths, driven by limiting driver cores [59]. This lends minimum number of required segments for the same resolution, which simplifies the driver configuration. However, the segments feature different electrical characteristics, which makes this approach more convenient for very efficient modulators with low capacitance, such that identical drivers can still be used. The length of the most significant bit (MSB) will determine the bandwidth (BW) of the module. This concept was proposed as early as in 1980 by Papuchon et al. [24] and has been used for demonstration of 28 GBd pulse-amplitude-modulation (PAM)-4 signals by using a 2-b SiPh SEMZM [60], with energy efficiency of 4.8 pJ/bit as well as for 28 GBd 16-quadrature-amplitude-modulation (QAM) signals by using 2-b SiPh SEMZMs in I/Q configuration with 8.9 pJ/bit [59].

In the subsequent sections, Tx modules with integrated 4-bit optical-DAC functionality are described, following the concept presented in Figure 3.1b. The modules are based on two different integration approaches: a hybrid approach that makes use of an InP I/Q-SEMZM together with SiGe:C BiCMOS drivers featuring 6.4 pJ/bit energy efficiency while operating at 512 Gb/s net data rate; a monolithically integrated prototype implemented in the EPIC platform which demonstrates 37 GBd PAM-4 operation, which is the highest among SiPh modulators. With 4-bits integrated DAC, the modules allow for a wide range of modulation formats, and the SiGe HBT drivers are able to provide larger output swings than high speed CMOS digital drivers at similar f_T, improving the optimization and co-design possibilities.

3.2 Hybrid I/Q Tx module with InP SEMZM

The block diagram of the hybrid Tx module is depicted in Figure 3.2. For I/Q modulation it comprises two BiCMOS drivers, wire-bonded in signal-signal configuration to a $(2^4 - 1)$ 15-segment InP I/Q-SEMZM. The module is designed for emitting at a wavelength of 1550 nm, in the optical C band. The I and Q drivers were fabricated in the SG13S technology and are identical mirrored versions of each other. The SEMZM is driven differentially, in push-pull manner.

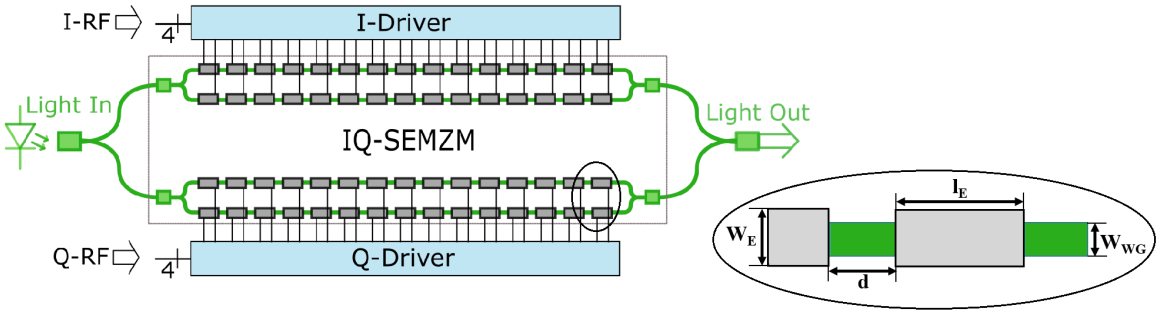


Figure 3.2: Simplified block diagram of the Tx module.

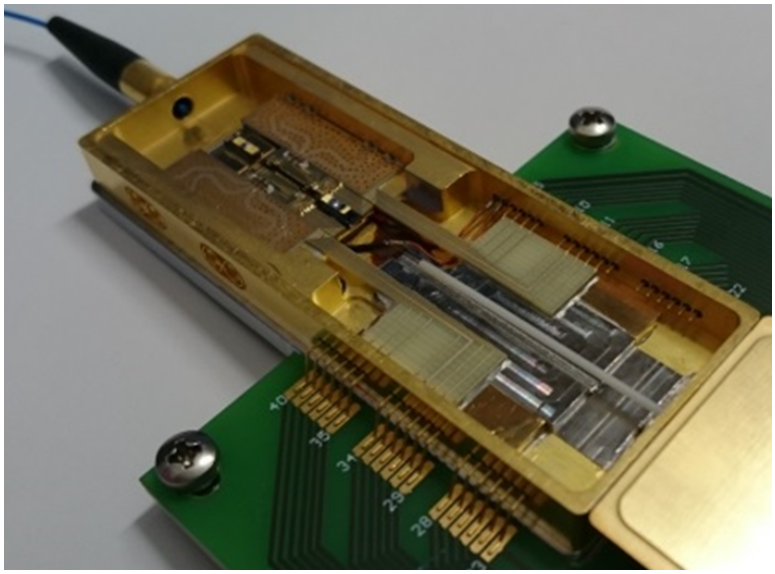
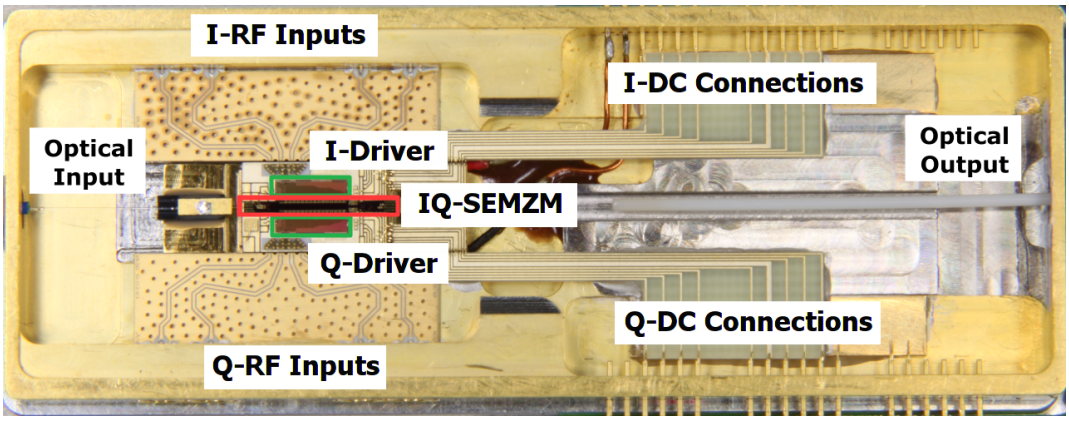
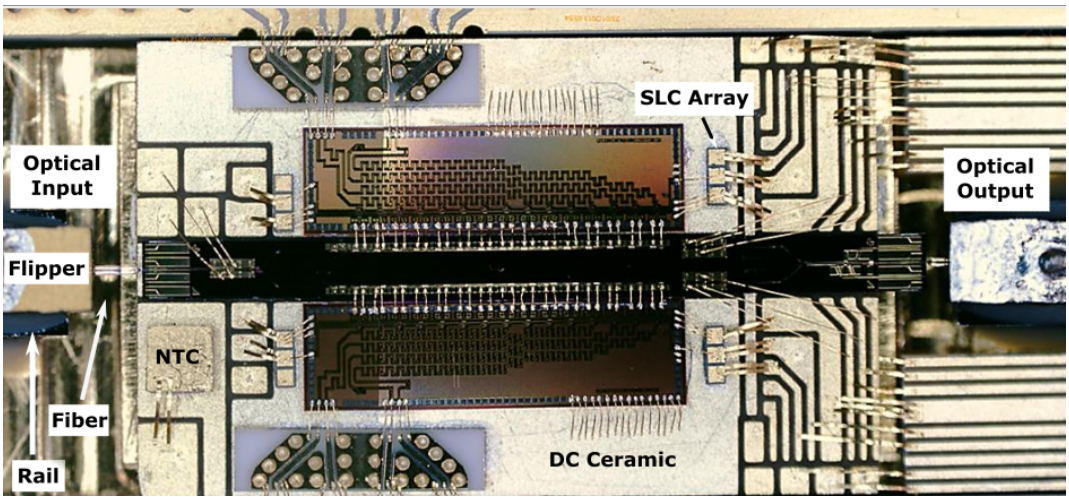


Figure 3.3: Picture of the packaged module.



(a)



(b)

Figure 3.4: (a) Close-up picture of the package with the IQ-SEMZM marked in red and the driver ICs in green. (b) Detailed view of InP IQ-SEMZM and BiCMOS drivers bonding.

3.2.1 Package characteristics

In Figure 3.3 the photo of the complete packaged Tx module is presented. Figure 3.4a provides a close up look where all the blocks are indicated and Figure 3.4b is a magnified image where

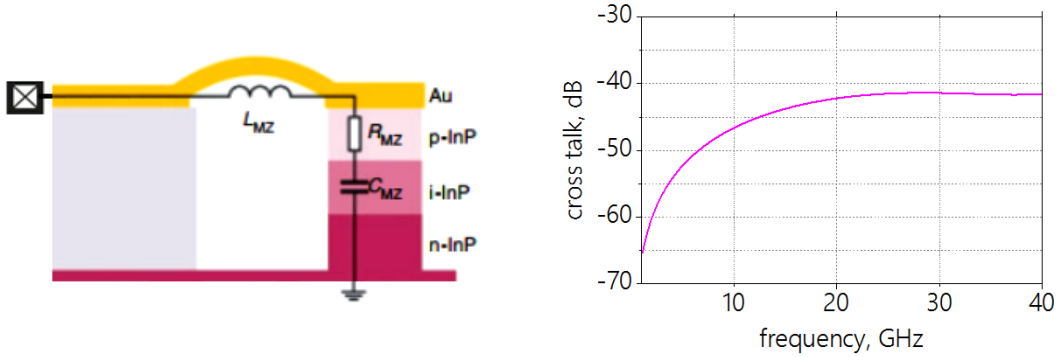
the two drivers wire-bonded to the modulator can be observed. Both the I/Q-SEMZM and the BiCMOS drivers are assembled in an Optical-Internetworking-Forum (OIF) compliant module, allowing measurements in a standard system environment without major adaptations. The hybrid-assembled OIF type1-like module has a footprint of 28 mm x 76 mm (gold box only) and offers 8 single-ended RF inputs, 4 per segmented driver. Besides high-frequency GPPO RF connections, the package (Figure 3.4a) offers 36 DC pins, 18 per MZM to provide the necessary biasing voltages to the modulators and drivers. The two ICs are placed on a DC circuit board plus carrier. A Peltier element, made out of Kovar, offering a high thermal conductivity coefficient of expansion which fits to the material composition of the driver and modulator, is attached to this carrier, stabilizing the temperature of the whole assembly. The optical coupling is provided on both short sides of the package with a fiber feedthrough. Flipper-rail assembly plus an adapted fiber with a spot size of about 3.5 μm are employed, allowing for high precision stable coupling efficiency over a large temperature range. 50 Ω single-ended RF lines route the data inputs down to the drivers in a skew-free and low-loss fashion.

3.2.2 InP SEMZM: electrical modeling

The employed InP SEMZM [63] comprises I/O spot-size converters, deeply-etched ridge waveguides, a dedicated biasing section and splitters and couplers obtained using multi-mode interference (MMI) couplers. The p-i-n junction of the SEMZM is operated in reverse bias condition which is obtained through the common n-layer with additional biasing electrodes. As will be derived from the next section, the modulator is 4.5 mm long, and is divided into 15 sections of 300 μm with an active length of 225 μm each. Figure 3.5a shows the cross-section of one segment. Isolation between segments is accomplished by epitaxial re-growth. The p-conducting InP layer (p-InP in Figure 3.5a) on top of the intrinsic region (i-InP) is etched away in between the segments where i-InP is then grown by selective epitaxial re-growth. This results in excellent electrical separation between adjacent segments, ensuring that no cross-talk effects take place. Figure 3.5b illustrates the cross-talk for adjacent segments of the modulator. The lumped equivalent of each segment is given by a series RLC network ($R_{MZ}\sim$ 2.5 Ω, $L_{MZ}\sim$ 26 pH, $C_{MZ}\sim$ 180 fF), as depicted in Figure 3.5a. The values for these elements, are extracted from the characterization of the stand-alone MZM. C_{MZ} is approximated by a constant capacitor, which is a safe enough assumption in p-i-n diodes where the thickness of the i-region mainly determines the capacitance with only small voltage dependence from the depletion into the p and n regions. R_{MZ} accounts for the series resistance of both contacts and junction.

With the described dimensions, the segments can be considered as lumped up to frequencies in the range of 29 GHz, according to a $\frac{\lambda}{10}$ criteria as in (3.1) and no propagation effects need to be taken into consideration [64]. In (3.1), f is the frequency the wave propagates with and f_{max} corresponds to the limiting case of the maximum frequency of operation that complies with the lumped criteria. It has been considered $n_{EL} \sim 3.5$ as the refractive index in the electrode.

$$L_{SEG} \ll \frac{\lambda}{10} \rightarrow L_{SEG} \ll \frac{1}{10} \cdot \frac{c}{n_{EL} \cdot f} \rightarrow f_{max} = 29\,GHz \tag{3.1}$$



(a) (b)

Figure 3.5: (a) MZM segment cross section and (b) cross-talk between adjacent segments.

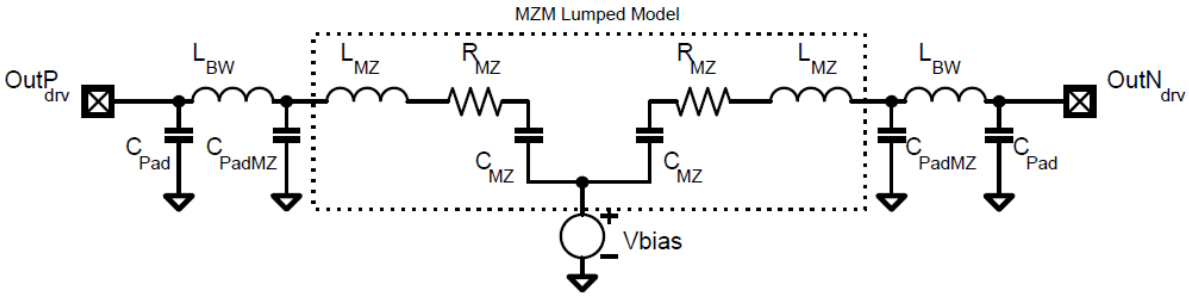


Figure 3.6: MZM segment and interconnect electrical model.

The physical interface between the driver and the modulator, chosen to allow for a simple wire-bonding technique, needs also to be accurately represented and accounted for. Figure 3.6 depicts the electrical model of the modulator segment together with the interconnect parasitics arising from the hybrid integration: The capacitance of the pads of both driver and modulator (C_{Pad}~35,fF, C_{PadMZ}~25 fF) and the bond-wire inductance (L_{BW}). The bias of the modulator is applied through the virtual ground. The main components in such network are the capacitance of the segment (C_{MZ}) which determines the time required to charge and discharge the intrinsic region of the diode, and the bond wire inductance (L_{BW} ~200 pH, determined by the minimum distance between the two chips) which, as will be seen in the next section, is responsible for peaking effects that need to be considered.

The DC optical insertion loss (IL) of the device is 8 dB from fiber to fiber. The measured DC modulation efficiency is 0.33 V · cm and a $V\pi IL$ of 10.8 VdB is obtained, at best biasing condition. The speed at which the optical wave propagates in the waveguide is given by (3.2).

$$v_{WG} = \frac{c}{n_{WG}} = 81\,\mu m/ps \tag{3.2}$$

This results in an optical delay per 300 μm segment of 3.7 ps, with n_{WG} ~3.5 being the optical refractive index.

3.2.3 Segmentation and hybrid integration impact

While offering higher flexibility and larger room for optimization than a traditional travelling-wave-electrode (TWE) design, in a SEMZM, modulator and driver design parameters become

much more interdependent and call for a careful design procedure and co-development of both parts in order to reach the full potential of the module. In this section the strategy used to find the optimum parameters in terms of the peak-to-peak voltage delivered by the driver (V_{App}), MZM length (L) and number of segments (n), as well as the performance limits imposed by the hybrid integration will be described.

As seen in Chapter 2, in a MZM the obtainable phase shift, which translates into the amplitude modulation index, depends on the length of the junction and the voltage delivered by the driver. This is governed by the modulator's efficiency ($Eff = f(IRT) = V\pi L$). For the generation of high order coherent modulation formats, a 2π phase shift is targeted in order to bias the MZM in the minimum point, obtaining highest extinction ratio (ER), together with low power dissipation and high operation speed. In the case of non-coherent modulation formats, such as m-PAM, the MZM is typically biased in the quadrature point, and a $V_{App} \leq V\pi$ is sufficient to obtain the highest ER; higher voltage would cause the outer levels to overlap.

On the modulator side, the main design constraints are the IL which must be kept sufficiently low and increases directly with L, and the length of the segments, which must be small enough in order to be considered lumped according to a $\frac{\lambda}{10}$ criteria as in (3.1). On the driver side, the delivered differential voltage must be kept lower than 3.5 Vpp due to the breakdown limit of the transistor ($2 \times BV_{CEO}$). At the same time, since the MZM segment is modelled mainly as a capacitive element, the driver must be able to handle the capacitance per segment at sufficient high speed. This capacitance is directly proportional to the length of each segment for a given efficiency, according to (3.3):

$$C_{MZ} = \epsilon \frac{W_E L_E}{IRT} = cte \cdot L_E \tag{3.3}$$

W_E is the thickness of the electrode, $\epsilon \frac{W_E}{IRT}$ is constant for a given efficiency and $L_E = \frac{L}{n}$ is the length of the electrode as sketched in Figure 3.2. Due to the parallel combination of the segments, the total capacitance can be written as $C_{TOT} = C_{MZ} \cdot n$. According to these constraints, from the MZM's $V\pi L$ product, to accomplish the targeted $V_{App} = 2V\pi$, it follows that the minimum modulator length must be $L \geq 2\,\text{mm}$, due to the BV_{CEO} limit from the driver. Moreover, the total equivalent capacitance per segment that the driver needs to handle (C_{SEG}) is given by the sum of the capacitances of the segment itself and the parasitic capacitances of the pads ($C_{Pads} = C_{Pad} + C_{PadMZ}$) as $C_{SEG} = C_{MZ} + C_{Pads}$. Considering negligible the effect of R_{MZ}, due to its small value, the current needed at the driver's output stage in order to provide an output swing of V_{App} at the C_{MZ} terminals is given by:

$$I_{SEG/2} = \frac{V_{App}}{R_c} \tag{3.4}$$

where $I_{SEG/2}$ stands for the current circulating in each of the differential half circuits, and R_c is the collector resistor. Moreover, to attain a sufficient BW of operation, enough to support a bit rate (BR) of $BR = BW/0.7$ [50], the collector resistor must be small enough to be able to move charge on and off the capacitor in less than one period of the data stream:

$$R_c \leq \frac{1}{2\pi C_{SEG} \cdot BW} \tag{3.5}$$

considering the limiting case with the highest value of R_c and substituting 3.5 into 3.4:

$$I_{SEG/2} = V_{App} \cdot 2\pi \cdot C_{SEG} \cdot BW \tag{3.6}$$

The supply voltage of the driver's output stage is given by (3.7), where η depends on the particular topology (i.e. the number of stacked transistors in the output stage):

$$Vcc = V_{App} + \eta V_{CEsat} \tag{3.7}$$

The power dissipated per segment is then:

$$P_{SEG} = \frac{1}{2} \cdot I_{SEG} \cdot Vcc = \frac{1}{2} \cdot 2 \cdot I_{SEG/2} \cdot Vcc = I_{SEG/2} \cdot Vcc \tag{3.8}$$

where it has been considered that in driving a modulator with a real digital signal, it is reasonable to expect equal number of charge/discharge cycles, (i.e. equal probability of ones and zeros to occur). The total power dissipation can be calculated as n-times the power dissipated per segment, $P_{TOT} = n \cdot P_{SEG}$. Using the expressions for $I_{SEG/2}$ in 3.6 and Vcc in 3.7 in the power equation we obtain:

$$P_{TOT} = n \cdot (V_{App} \cdot 2\pi \cdot C_{SEG} \cdot BW)(V_{App} + \eta V_{CEsat}) \tag{3.9}$$

Opterating and replacing C_{SEG} lends:

$$P_{TOT} = 2\pi \cdot BW \cdot V_{App}(V_{App} + \eta V_{CEsat})(n \cdot C_{Pads} + C_{TOT}) \tag{3.10}$$

Replacing constant (cte) terms:

$$P_{TOT} = cte \cdot BW(V_{App}^2 + cte \cdot V_{App})(n \cdot C_{Pads} + cte \cdot L) \tag{3.11}$$

From (3.11), it becomes evident that power dissipation increases with data rate. Moreover, some insight is gained on how the different design parameters contribute to power dissipation:

- Due to the $n \cdot C_{Pads}$ factor, which accounts for the undesirable power spent in the capacitance of the pads, for a given L power dissipation increases when the modulator is divided into a larger number of segments, although the maximum frequency of operation (f_{max}) is higher (3.1).
- As the energy dissipated increases quadratically with the voltage delivered by the driver, but only linearly with the length of the modulator, longer modulators will result in lower power consumption.

These dependencies between the different parameters are graphically collected in Figure 3.7. As 4-bits of resolution are targeted, a minimum number of 15 segments (2^4-1) is required, or integer multiples of this number. In Figure 3.7, it is shown how the power dissipation (P) and the maximum achievable speed (f_{max}, satisfying (3.1)) change with the length of the modulator, for two different number of segments n=15 and n=30, which comply with the 4-bits of resolution condition. It can be seen how shorter modulators dissipate larger amount of power and that for a given length (i.e. L = 6 mm), a larger number of segments leads as

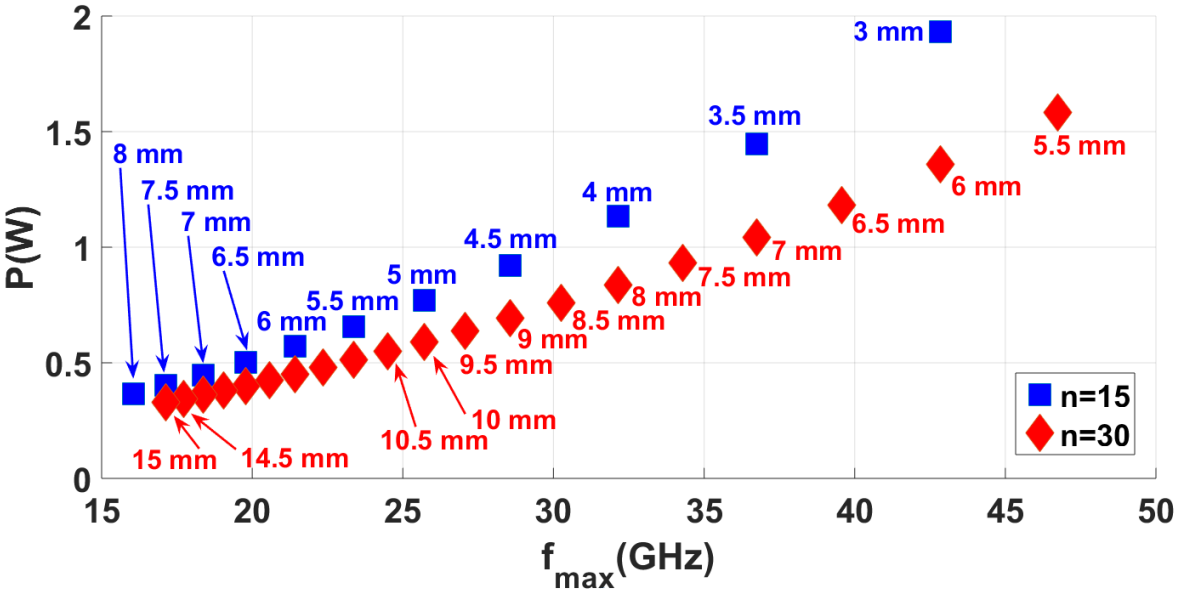


Figure 3.7: Dependency between power dissipation (P) and maximum frequency of operation (f_{max}) (complying with $\lambda/10$ criteria), with MZM length and number of segments.

well to larger power dissipation. Therefore, the best choice will be to target moderately long modulators with lowest number of segments that are able to render f_{max} greater than the target BW and desired resolution: for a BW $\sim$ f_{max} $\sim$ 32 GHz, with n=30 a much longer modulator is needed with very less improvement in power consumption.

The length of the segment is, however, not the only limiting factor in the achievable BW. Another important effect, coming from the hybrid integration must be examined as well: the inductance of the bond-wire in series with the capacitance of the segment creates a RLC series network, with natural frequency f_0, as in (3.12) which limits the maximum attainable speed.

$$f_0 = \frac{1}{2\pi\sqrt{L_{BW} \cdot C_{MZ}}} \tag{3.12}$$

According to a typical second order low pass filter response, at f_0 a peaking effect is observed, and the voltage applied on the capacitor is magnified and becomes larger than what is provided by the driving source (Q-times larger, being Q the quality factor of the resonating circuit), inducing more phase shift. Above the resonant frequency the signal is steeply attenuated which will limit the maximum attainable speeds. As the bond-wire length is set by packaging constraints, (i.e. minimum distance that the chips can be put close to each other), to push this resonant peak to higher frequencies, the capacitance of the segment must be reduced. For a selected L this would imply increasing n which, according to 3.7 would translate into power dissipation penalty.

After all these considerations, for the final design, a total length of 4.5 mm for the modulator is targeted, divided into 15 sections of 300 μm with an active length of 225 μm each, which translates into a total active length of 3.375 mm. The resonance frequency coming from the hybrid integration in such segments would occur at f_0=26 GHz sufficient for symbol rates in the order of 40 GBd. From the DC modulation efficiency of the MZM, ($V\pi L = 0.33\,Vcm$), with the selected segment length, a corresponding $2\,V\pi$ $\sim$2 V can be extracted, which is the differential output voltage that the driver must provide. In a practical scenario however, this

efficiency will slightly change depending on the biasing condition of the MZM (Vbias), which trades off high efficiency with low IL. In order to have enough room to find the best operating condition, at the driver a $V_{Appd} = 2.5\,\text{Vpp}$ maximum differential output voltage is targeted.

3.2.4 Driver design and stand-alone performance

The block diagram of the driver is sketched in Figure 3.8. Each driver has 15 differential outputs and 4 single ended inputs and operates from two different supplies Vcc=2 V and Vbias=3 V. Figure 3.9 shows the I and Q drivers microphotograph, with a total area of $7.5\,\text{mm}^2$, each. In the following the individual blocks are described.

B2T Encoder -Input Transmission Lines: The wired B2T encoding scheme is implemented in each driver by adequately routing four transmission lines, such that each of them distribute the input binary data stream to a thermocode-weighted amount of driver cores. The first of these lines drives the first 8 segments corresponding to the MSB, the second line drives segments 9 to 12, the third line is connected to segments 13 and 14, and the fourth line goes to segment 15 which is the least significant bit (LSB). In this way, a certain number of driver cores will be switched on, tracking the input bit stream. The lines are implemented as microstrip transmission lines, in the top most layer of the technology stack with $3\,\mu$m thickness and feature $0.35\,\text{dB/mm}$ @ $40\,\text{GHz}$ loss. The impedance of the lines is slightly higher than $50\,\Omega$ (i.e. $Z_0 \sim 52\,\Omega$), such that when loaded with the driver cores they can absorb their input capacitance with the Z_0 falling to the desired $50\,\Omega$. They are designed in a modular approach, with two different blocks that are periodically repeated: *segment* and *down-turn*. The *segment* has a pitch of $300\,\mu$m and, as seen in Figure 3.9, follows a serpentine pattern with two bends in order to achieve velocity matching between the optical and electrical waves. In this way, the electrical delay per segment is increased matching the optical delay per segment of 3.7 ps. The *down-turn* occupies as well a $300\,\mu$m pitch, however it is designed such that while maintaining characteristic impedance and delay same as the segment block, serves to bring the longer lines down in the vertical direction in order to feed the driver cores. At the inputs, as seen in Figure 3.9, the lines are designed such that they equalize the delays between the different RF paths caused by pad-frame constraints, so that all bits are synchronized.

Each of the input lines is terminated by a $50\,\Omega$ resistor connected directly to the common mode voltage (Ref_CMI) of 1.35 V. This voltage is produced on-chip as indicated in Figure 3.10, following a straightforward implementation based on a low-dropout (LDO) regulator

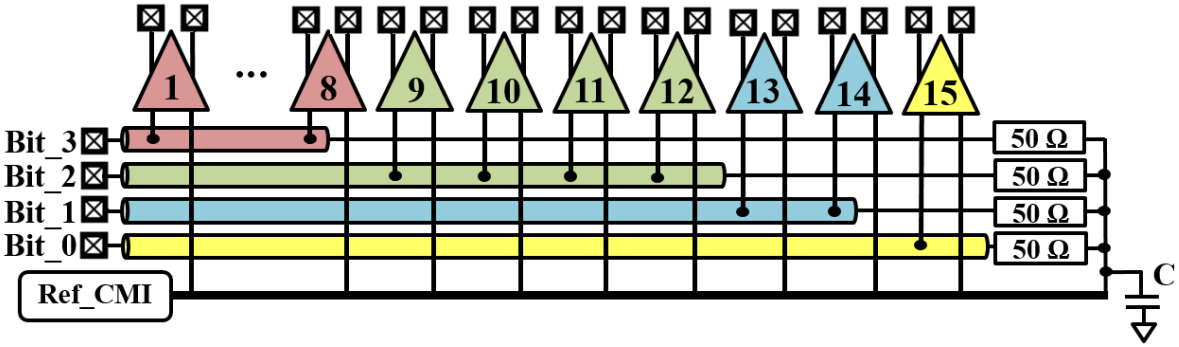
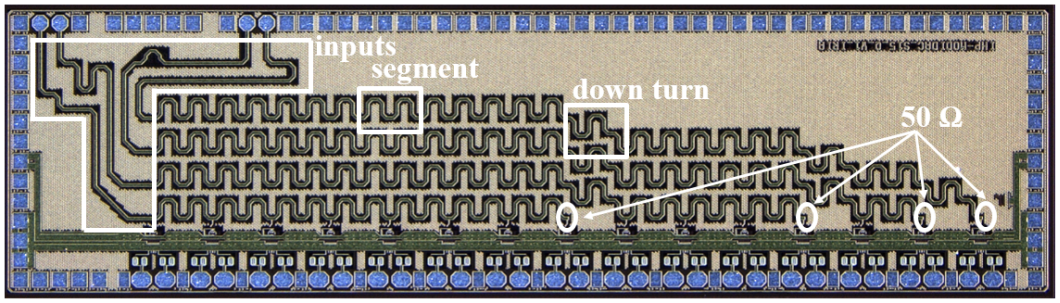
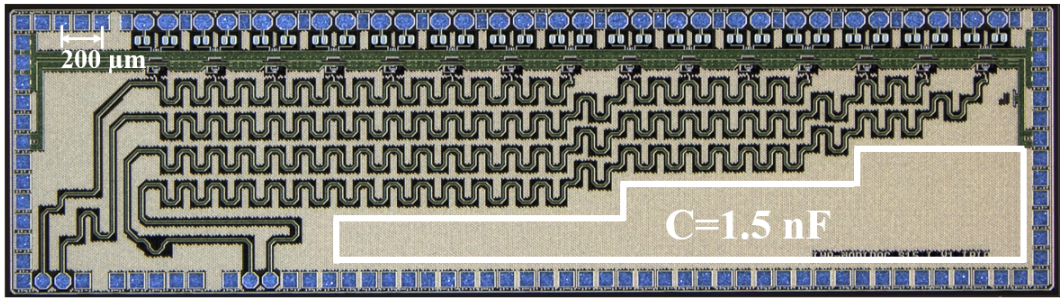


Figure 3.8: Simplified block diagram of the driver IC.



(a)



(b)

Figure 3.9: Michrophotograph of (a) Q and (b) I drivers.

together with a Brokaw bandgap reference. This stage, which dissipates a negligible amount of power ($\sim 0.5\,\mathrm{mW}$), avoids extra power dissipation, compared to a Ref_CMI produced from a resistive divider. Due to the lack of an ideal virtual ground being the lines single ended, the required AC-ground for the $50\,\Omega$ termination resistors is given by an on chip capacitor of 1.5 nF, which is sufficient to bring the low cut-off frequency down to 100 MHz. This low cut-off frequency can be further decreased by an off-chip parallel capacitor connected to a pad reserved for this purpose.

Driver Cores: The topology of each of the cores is sketched in Figure 3.11. It is a switching amplifier based on a pseudo-differential architecture, comprising two stages: a pre-driver followed by the output stage, which performs the switching, dissipating the 80% of the power. In the high logic level, the output transistors (Q10, Q11) are open and C_{SEG} is charged by

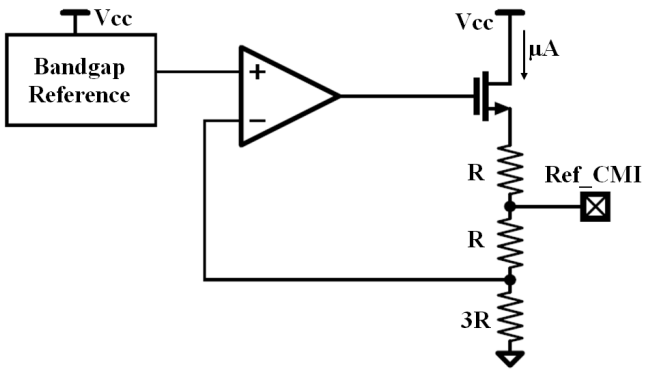


Figure 3.10: Generation of Ref_CMI.

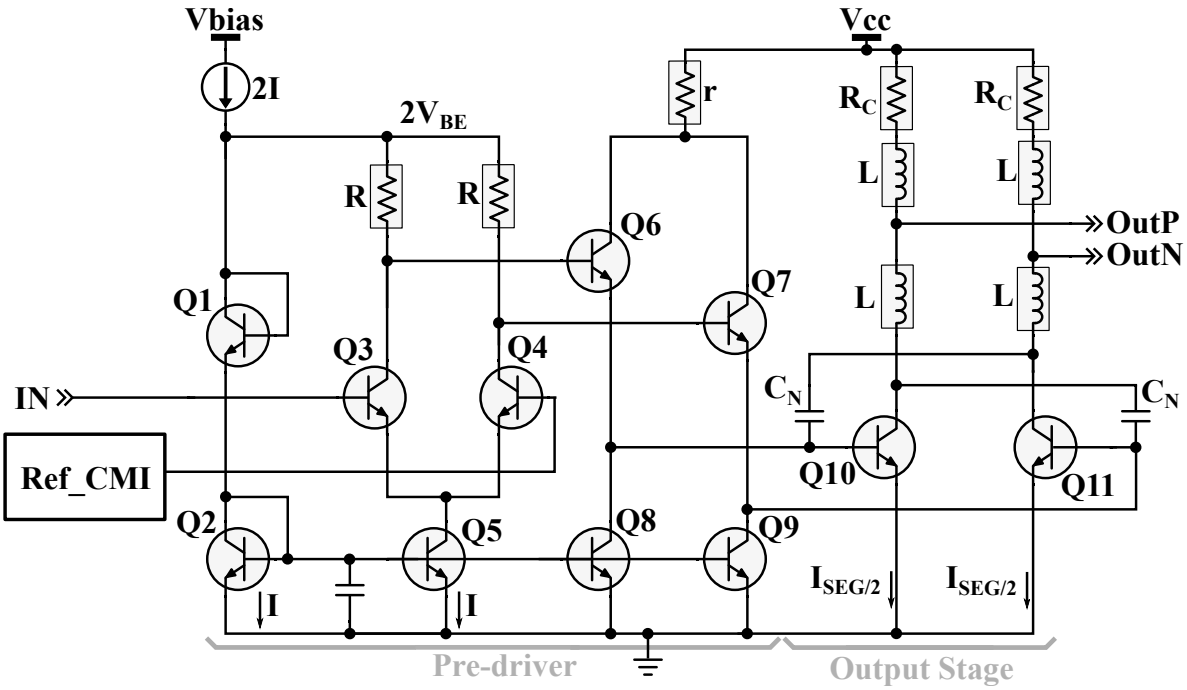


Figure 3.11: Driver schematic.

the $I_{SEG/2}$ through the Rc resistors up to a final voltage of Vcc while in the low logic level the capacitance is discharged through the transistors operating close to saturation.

Output Stage: Compared to a typical implementation with a differential pair in the output stage [65], the output voltage in this topology is allowed to range down to V_{CEsat} above ground. This is achieved by removing the current source of the differential pair (Q10, Q11), which otherwise would force the minimum output voltage to around 1 V above ground, therefore, allowing for a reduction in the supply voltage of the same magnitude. Without current source, the current level developed at the output transistors is defined by the architecture implemented in the pre-driver. In order to deliver the required $V_{App} \sim 1.25$ V, the necessary current biasing is given by (3.4): $I_{SEG/2}$ =1.25/Rc. Moreover, to attain a BR of 40 Gb/s, according to (3.5) and the relation of BR and BW [50], we come to Rc = 23 Ω which would lead to $I_{SEG/2}$ = 54 mA. Considering that a supply voltage of Vcc∼ 2 V is required, the power dissipation per segment would amount to 108 mW, or to ∼ 1.62 W for the 15 cores, without taking into account the pre-driver consumption. The power dissipation in this output stage was however reduced by around 50% by means of the inductive peaking techniques implemented.

Apart from the effect of the bond wire inductance, which is the primary contribution, the bandwidth of the driver cores was further enhanced through the use of additional on-chip inductive peaking. Two independent inductors (negligible coupling factor) with value of L∼180 pH were designed, which together with the bond wire inductance that appears in series at the output give rise to an inductive network equivalent to that achieved by a T-coil, as seen in Chapter 2. In order to reduce the parasitic capacitance, they were fabricated in the top most layer of the technology stack, which is the thickest and farthest from the substrate. The value of each inductor was initially approximated by $0.4R^2C_{SEG} \sim 220$ pH, with $m = 1/(1+\sqrt{2})$ ∼0.4, for maximally flat gain, and were further optimized after electromagnetic (EM) simulations considering the full model of the load with the contribution of the bond-wire inductance as well

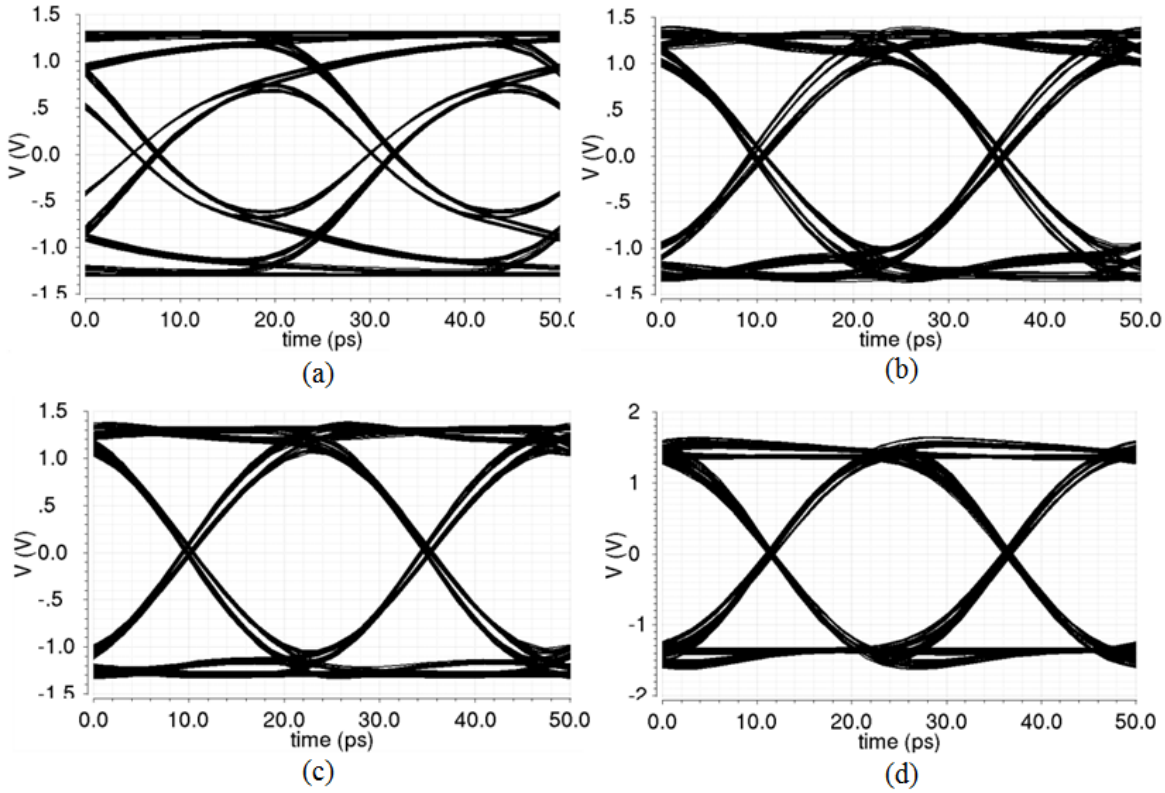


Figure 3.12: Simulation results for the eye diagram at 40 Gb/s with (a) no peaking structure, (b) bond-wire only, (c) bond-wire together with inductive peaking on-chip, and (d) bond-wire together with inductive peaking and negative capacitance.

as the driver parasitics. Inductors from adjacent segments are separated by 85 μm distance. In order to improve the isolation and avoid any cross-talk effects in between segments, a grounded metal stripe of 45 μm width was placed in between the inductors. After EM simulations the cross-talk between contiguous inductors was better than -45 dB until 40 GHz. In this way, the peaking structures (on-chip peaking and bond-wire) provide an equalization effect for the higher frequencies permitting the output stage to be designed with lower bandwidth. This allows for an increase in Rc, reducing the $I_{SEG/2}$ necessary for delivering the required voltage at the output, which leads to lower power dissipation. A final value for the Rc of 48 Ω was achieved, which translates into a necessary $I_{SEG/2}$ of 26 mA, and a maximum power dissipation in the output stage of 52 mW per segment.

To further improve the performance, negative capacitance compensation, with $C_N \sim$ 12 fF, was also employed. This technique was kept to a minimum, due to the risk of oscillation because of the positive feedback effect. The accumulated action of these techniques can be seen in Figure 3.12, which displays the simulated differential electrical eye diagram at the capacitor of one of the segments at 40 Gb/s; it can be clearly seen how the eye progressively opens with each additional contribution.

Pre-driver: Without current source, the adequate base voltages for the output transistors are produced through the input differential pair (Q3, Q4) and emitter followers (Q6, Q7), which set an output level for the high signal state of approximately $2V_{BE}$ above ground. The bias current 2I from the Vbias supply, controls the current level developed at the output transistors [66]. The same emitter areas of Q2 and Q5 allow this current to divide equally

Parameter	Value	Parameter	Value
Q (1-5)	$1{\times}0.12{\times}0.48\,\mu m^2$	L	180 pH
Q (6-7)	$5{\times}0.12{\times}0.48\,\mu m^2$	C_N	12 fF
Q (8-9)	$2{\times}0.12{\times}0.48\,\mu m^2$	R	250 Ω
Q (10-11)	$12{\times}0.12{\times}0.48\,\mu m^2$	I	1.25 mA
Rc	48 Ω	V_{INpp}	4 × 500 mV
$I_{SEG/2}$	26 mA	V_{OUTppd}	15× 2.5 V
Vcc	2 V	$P_{COREmax}$	65 mW
Vbias	3 V	P_{driver}	0.97 W

Table 3.1: Driver design parameters summary.

between the two branches. Half of the current flows through the diodes setting the supply of the differential pair Q3, Q4 to $2V_{BE}$, and the remainder current forms the tail current of the Q3, Q4 pair. Moreover, this differential pair, which has one input set to the DC common mode voltage (Ref_CMI), converts the input RF signal from single ended to differential.

It is important to notice that, although the input transmission lines are several mm long, (for the LSB until segment 15 the line is ∼10 mm long) an inherent benefit of this switching topology is the relative insensitivity to the losses in the input signal: as long as sufficient signal swing is guaranteed to perform the switching, the driver is able to restore the full voltage at the output providing virtually equal output voltage across the whole modulator length. On the contrary, in a linear topology, where the driver amplifies the input signal, the implementation of long modulators becomes more challenging as the losses along the line need to be compensated. After considering the losses in the input lines, the minimum signal required at the input is 250 mVpp. The transistors in the input differential pair are of the smallest size and represent a negligible load to the lines which has been considered in the design of those. Driver design parameters are summarized in Table 3.1.

In [67], which is the first implementation of a driver for a SEMZM in the literature, the authors deduce a lower limit for the power required to charge and discharge the MZM capacitance for data transmission, given by the following equation:

$$P_{MIN} = 2 \cdot (1.5)(\frac{BR}{4}) \cdot C_{SEG} \cdot V_{App}^2 \tag{3.13}$$

In their implementation they achieve a power consumption which is 20 times higher than this limit. For the driver presented here, according to (3.13) the limiting value would be given by 12 mW at 40 Gb/s, and our design provides less than 6 times higher power dissipation than this limit, which depicts the overall technology advancement in this field.

Driver electrical characterization: Both I and Q drivers were independently characterized in the electrical domain via on-wafer probing, both in the time and frequency domains.

Large signal measurements were performed operating with PRBS31, and eye diagrams were measured up to 40 Gb/s from all outputs with the Keysight wide bandwidth oscilloscope 86100D. It must be kept in mind that during these measurements the driver is loaded with 50 Ω instead of the capacitive SEMZM segment model. In this way the R_C ∼48 Ω is in parallel with a 50 Ω resistor and the differential output voltage decreases to 1.2 Vpp. Figure 3.13 presents

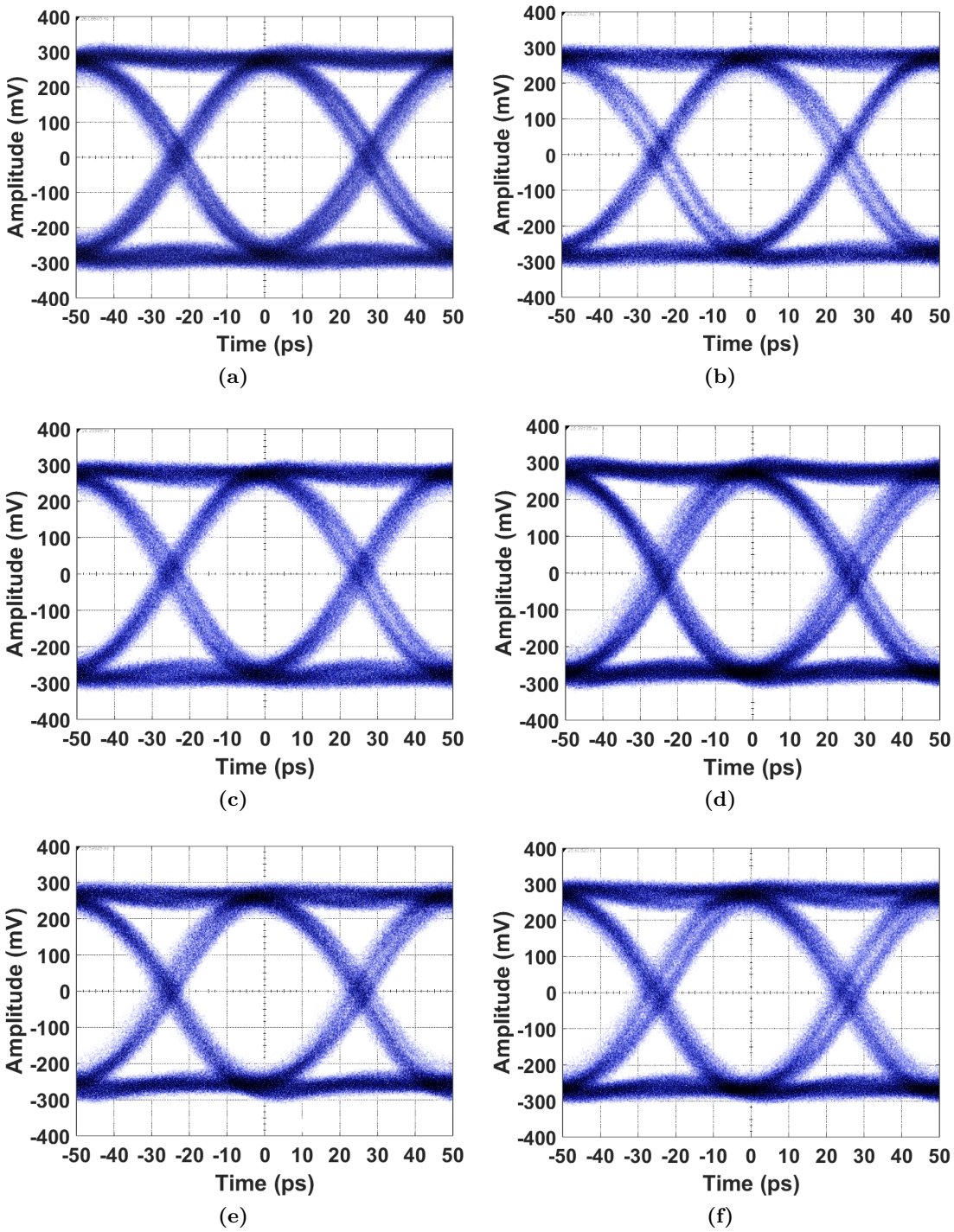
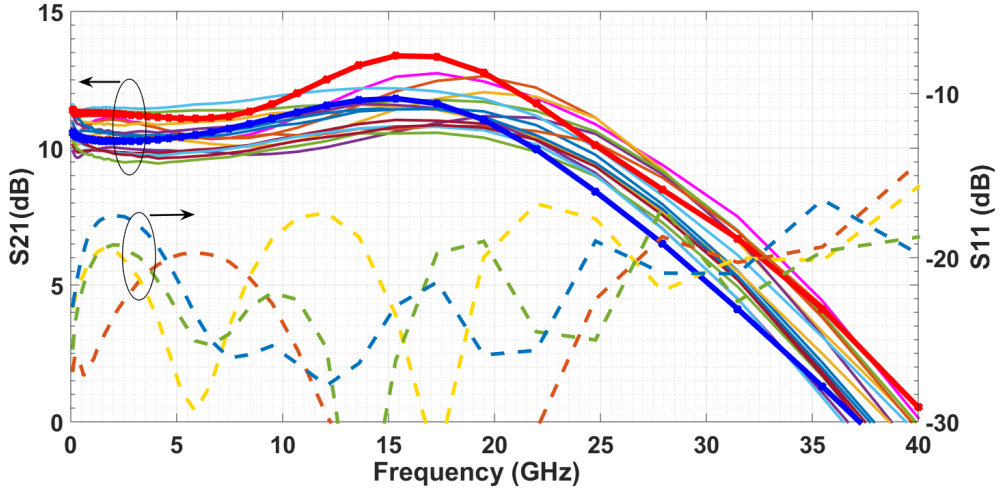


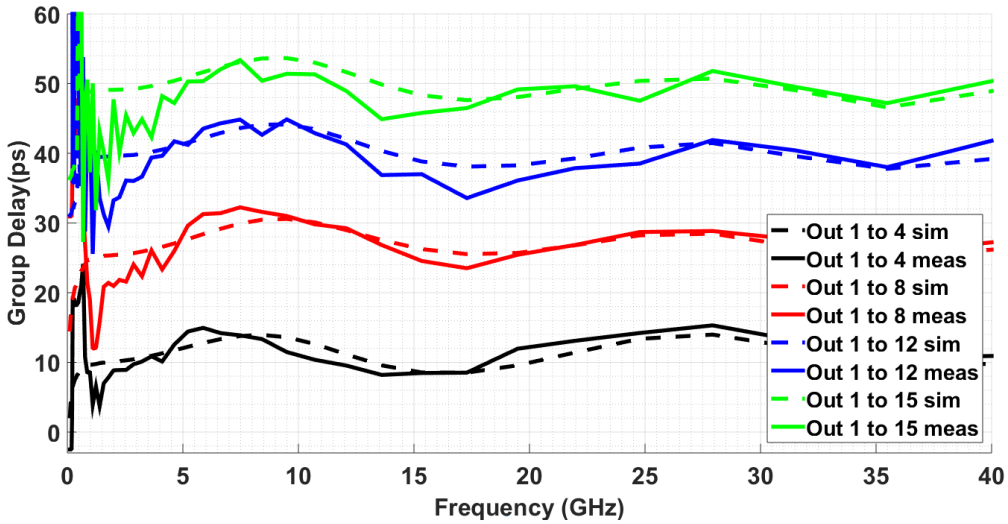
Figure 3.13: Eye diagram measurements @40 Gb/s from: the I-driver, (a) output 1 (b) output 8, (c) output 15 and from the Q-driver, (d) output 1, (e) output 8, (f) output 15.

summarized results from alternative outputs of the drivers. It can be seen how the outputs of the drivers are identical in amplitude and wave-shape for both I and Q drivers. The output amplitude from the measurements is 600 mVpp differential, measured with 6 dB attenuation which indicates that the required output voltage is being delivered, meeting the targeted 2.5 Vpp on the MZM load.

Small signal S-parameter measurements were performed using a Rhode Schwarz ZVA67 VNA with -25 dBm input power. Figure 3.14a shows the comparison of the measured S21 for



(a)



(b)

Figure 3.14: (a) Measured S11 from all inputs and measured S21 from all outputs vs. simulated S21 from output 1 (red*) and output 15 (blue*) and (b) measured vs. simulated group delay.

all channels with port 2 differential, and the simulated curves for outputs 1 and 15. All curves are in good agreement. It must be recalled that in small signal operation the drivers are not fully switching and therefore these results must be assessed from a qualitative point of view, only. Figure 3.14a displays as well the input matching of the four input distributor lines, where it can be seen that the S11 is well 50 Ω matched from 100 MHz to 40 GHz, indicating the good AC-ground that is achieved through the on-chip capacitor. Figure 3.14b shows the measured group delay between driver segments, from outputs 1 to 4, 1 to 8, 1 to 12 and 1 to 15. The measured values are in excellent agreement with the simulated curves. From these results it can be extracted that the required 3.7 ps delay between adjacent channels necessary to match the optical delay is accurately attained.

3.2.5 Functionality verification

The full functionality of the Tx module was experimentally verified through electro-optical (E/O) measurements both in the time and frequency domains.

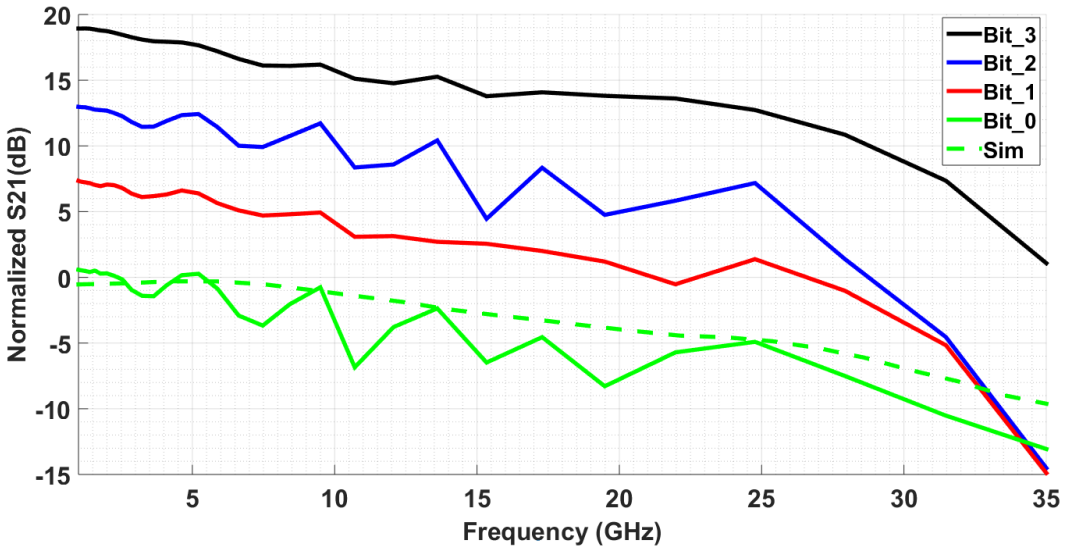


Figure 3.15: E/O S21 SEMZMs vs. simulated electrical S21 on last segment only.

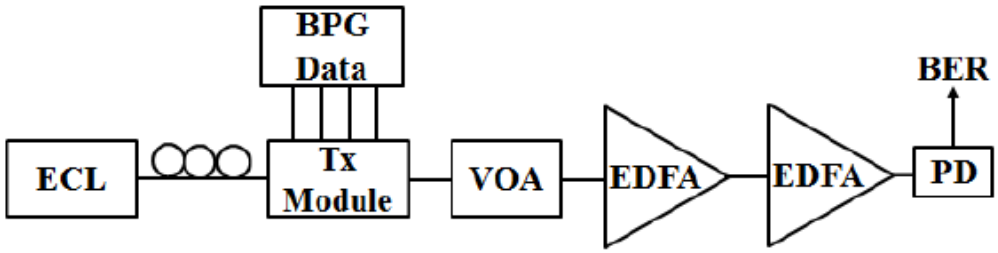


Figure 3.16: E/O setup for m-PAM measurements.

S-Parameters Measurements: E/O S-Parameters were measured from each of the four driver inputs down to the optical output of the SEMZM using -30 dBm input power. The normalized S21 results are presented in Figure 3.15. The S21 for the LSB is compared with the electrical S21 of output 15, being both curves in good agreement. With the other bits, as the S21 is the result of the accumulated effect of more than one segment, this comparison is not possible in our simulation environment. From the figure, the 6 dB drop in gain between adjacent bits can be observed, as each of them drives half number of segments, and also the predicted peaking at around 26 GHz due to the combined effect of bond-wire inductance and C_{MZ} is distinguishable. In terms of performance in the frequency domain however, it must be recalled that in small signal operation, the drivers are not fully switching, and therefore quantitative information in terms of BW cannot be extracted from these curves.

Large signal measurements: Depending on the number of bits connected at the input, the module allows for a wide range of modulation formats. Signal generation experiments of both intensity modulation formats (m-PAM) as well as coherent modulation formats (m-QAM) have been performed.

For the m-PAM formats, a single SEMZM from the I/Q, biased in the quadrature point, is employed. The B2B setup for these measurements is described in Figure 3.16. Four single-ended PRBS31 signals are provided at the inputs of the I-driver with the bit pattern generator (BPG). An external cavity laser (ECL) at 1550 nm is used as continuous wave laser source. After

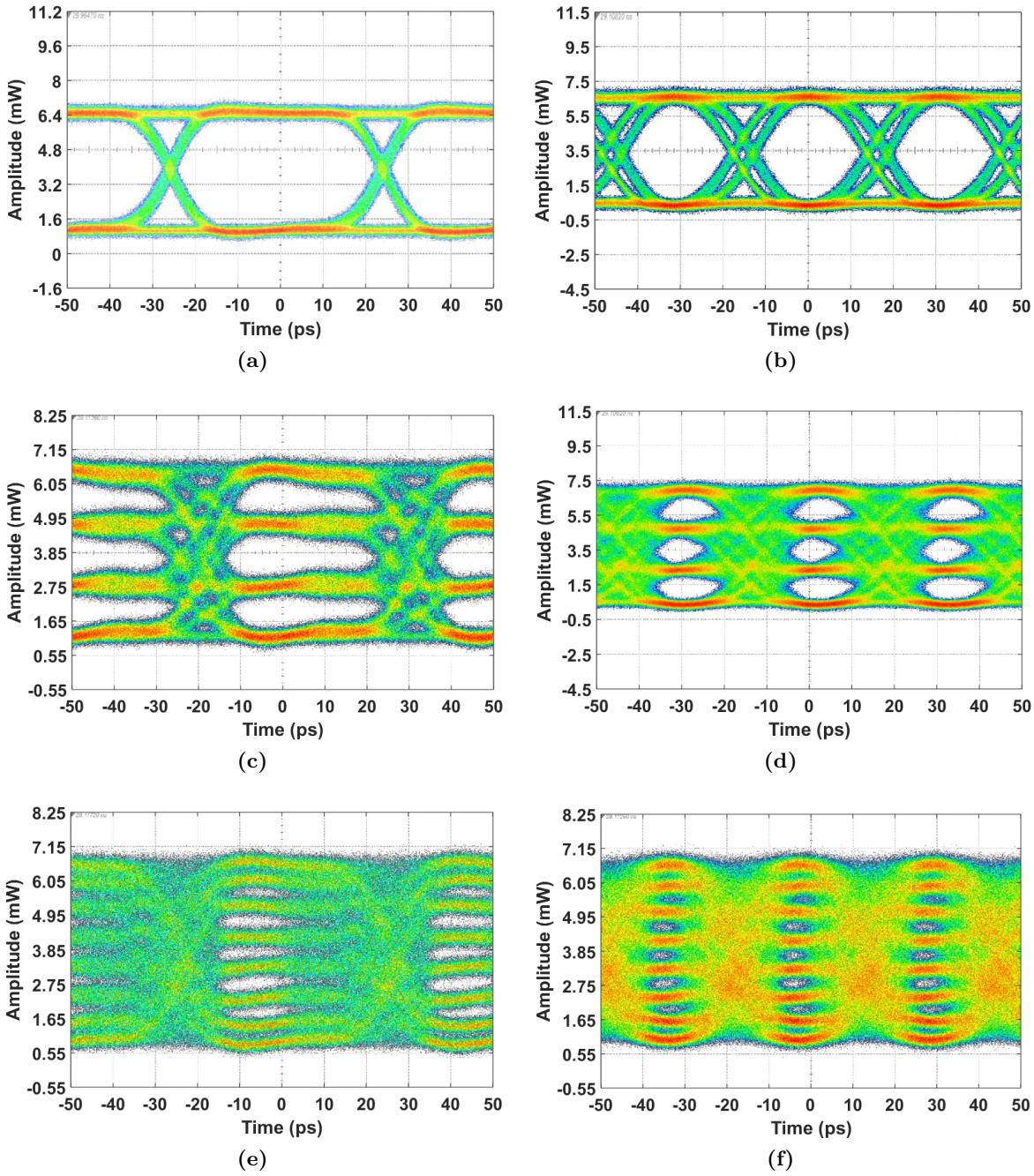


Figure 3.17: E/O eye diagrams: (a) OOK @20 GBd, (b) OOK @32 GBd, (c) 4-PAM @20 GBd, (d) 4-PAM @32 GBd, (e) 8-PAM @20 GBd and (f) 8-PAM @32 GBd.

the Tx module the optical signal travels through a variable optical attenuator (VOA) and erbium-doped fiber amplifiers (EDFA) which control the optical signal-to-noise-ratio (OSNR). After going through an additional EDFA a photodiode (PD) is employed for detection. A blind equalizer is employed off-line before error counting. Signal generation with OOK, (1-bit), 4-PAM (2-bits) and 8-PAM (3-bits) modulation formats are demonstrated. In 4-bits operation, 16 clear and distinguishable levels could not be received as the outer levels start overlapping. This occurs when the applied voltage is much higher than the V_π because of the the MZM's transfer function (recall Figure 2.3). Figure 3.17 shows the eye diagrams at 20 GBd and 32 GBd for the different formats. The corresponding bit-error-rate (BER) measurements for the 32 GBd

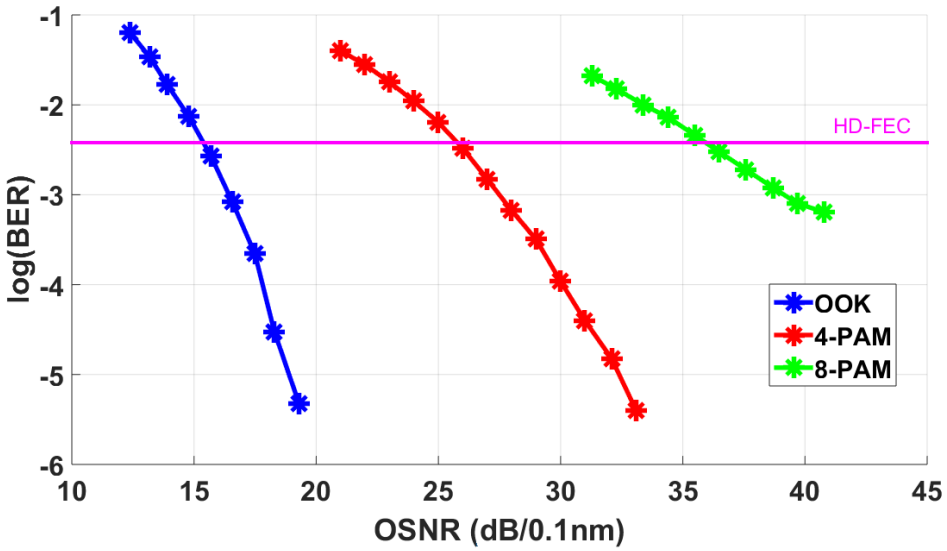


Figure 3.18: BER vs. OSNR curves for the direct detection experiments where a single SEMZM is driven at 32 GBd.

eye diagrams are presented in Figure 3.18 as a function of the OSNR. Power dissipation is 0.917 W for OOK, 0.837 W for 4-PAM and 0.572 W for 8-PAM, respectively, optimized for lowest BER. Power dissipation reduces with increasing PAM order, in spite of the higher number of drivers connected, because the voltage applied was reduced (lowering Vbias supply) in order not to reach saturation or level-overlapping in the modulator.

From Figure 3.18 it can be seen how the error floor of the transmitted data is well below the hard-decision threshold forward-error-correction (HD-FEC) of commercially available FEC algorithms. This FEC threshold represents the minimal quality of uncoded transmission for which the FEC algorithm is effective. The higher the overhead, the higher uncoded BER can be tolerated. Typically, 3.8×10^{-3} is the minimum uncoded BER when using 7% overhead (HD-FEC) and 2.2×10^{-2} when using 21% overhead FEC (SD-FEC) [68].

For the coherent measurements, both SEMZMs in the I/Q ensemble are employed, with the modulator biased on the minimum point. 16-QAM and 64-QAM signal generation is demonstrated where, by encoding the possible data values in two orthogonal electric field components, the spectral efficiency is increased 4 and 6 times respectively, as compared to traditional OOK transmission. For the 16-QAM measurements, only 2-bit streams are turned on for the I and the Q modulators each. The other inputs are left open. For the 64-QAM experiment, all the bit inputs are activated for both modulators. Of these, 3-bits are employed for data transmission whereas the LSB (Bit_0)is used to compensate for design and fabrication mismatches and to move the constellation ponts closer to their ideal position on the IQ plane.

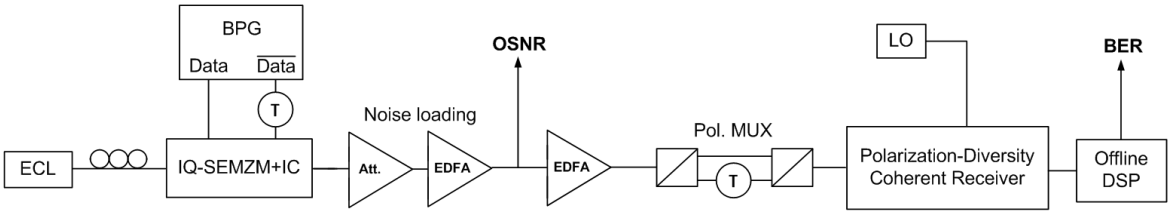


Figure 3.19: Experimental setup for the dual-polarization 32 GBd m-QAM B2B measurements.

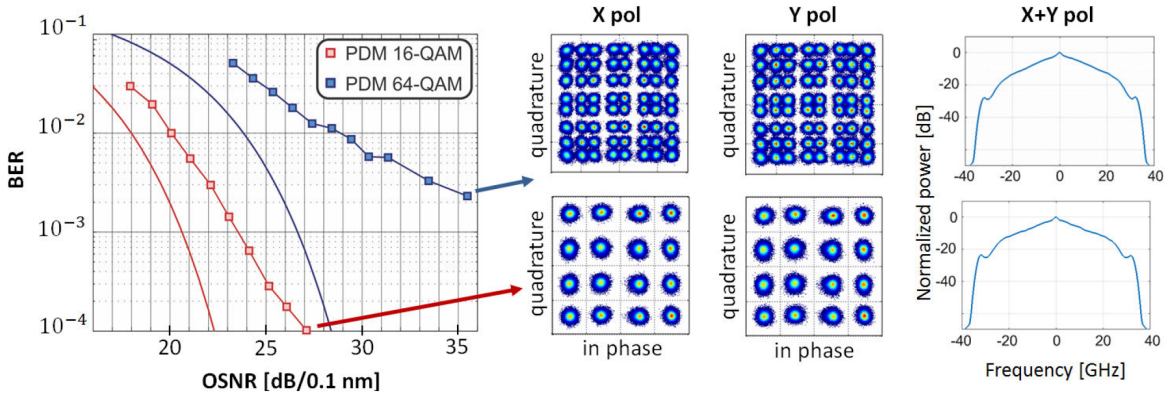


Figure 3.20: BER vs. OSNR curves of the PDM 16-QAM and PDM 64-QAM signals together with the theoretical limits, the correspondent IQ constellations at maximum OSNR and the received power spectra after the ADC. Symbols represent measured BER values and solid lines the theoretical BER in an AWGN channel.

This compensation is performed in a static fashion, by ecoding Bit_0 into the RF data, feeding it into the same sequance of Bit_1 in each one of the I and Q modulators. The back-to-back (B2B) experimental setup for these measurements is shown in Figure 3.19. A 4-differential channel BPG is employed to generate the 8 required PRBS31 bit streams. Because of the limited number of data channels, the positive BPG outputs are connected directly to the I-inputs, whereas the Q-data is connected to the negative BPG outputs and decorrelated through electrical delay lines of sufficient length. After the transmitter module, the optical signal travels through a noise loading stage to vary the OSNR, an EDFA and a polarization multiplexer. This multiplexer includes 2.6 m of fiber to decorrelate the two polarizations. The detection is performed with a polarization-diversity coherent receiver. The signal is digitalized with a real-time sampling scope with 33 GHz bandwidth and digital signal processing (DSP) is performed off-line. The DSP includes optical frontend correction and chromatic dispersion (CD) compensation. An adaptive 2×2 MIMO time domain equalizer is used for polarization de multiplexing and to compensate for the residual CD. The carrier phase is recovered based on blind phase search algorithm. An additional 4×4 adaptive equalizer based on decision directed least mean squared algorithm is used to compensate for residual timing skew. Finally, decision based on minimum Euclidean distance is performed followed by symbol-to-bit de mapping and bit errors counting. The received BER curves versus OSNR for the two PDM modulation schemes are shown in Figure 3.20. The 32 GBd constellations for X and Y-polarizations at maximum OSNR after offline DSP are also depicted, together with the received power spectra after ADC.

The PDM-16-QAM implementation penalty with respect to the theoretical OSNR requirements for an ideal additive white Gaussian noise (AWGN) channel at a BER of 3.8×10^{-3}, i.e. the HD-FEC threshold, is equal to 3 dB. At the SD-FEC threshold the penalty is as little as 2 dB. At the same BER level, the penalty for the PDM-64-QAM signal is lower than 4 dB. The PDM-64-QAM signal was transmitted over 80 km of standard single mode fiber (SSMF). The received BER, equal to 9.1×10^{-3}, was measured to be below the SD-FEC threshold and can be thus transmitted error-free with 21% of overhead. The transmitted gross data rate amounts to 384 Gb/s with 1.5 W power dissipation which translates into an energy per bit of 7.8 pJ/bit, calculated for the single polarization only.

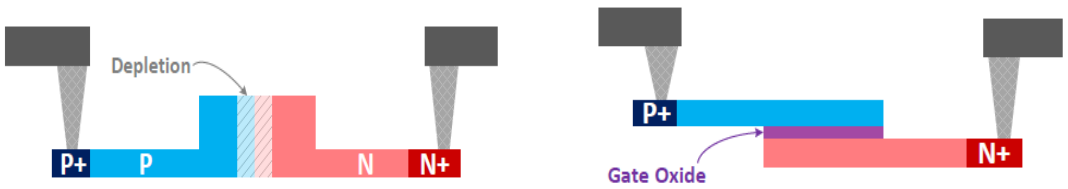
Finally, the generation and transmission over 120 km of SSMF of 256-QAM signals at symbol rate of 32 GBd has been demonstrated with this module, as described in [69]. This is the highest order modulation format demonstrated to date at such speed and translates to a line rate of 512 Gb/s with energy-per-bit of 6.4 pJ/bit.

3.3 Monolithically integrated Tx module with SiPh SEMZM

Silicon photonics technology, capable of manipulating electrons and photons on the same platform, promises higher functionality on a single chip, enabling large scale integrated photonic circuits. Due to the inherent CMOS compatibility, the investment and expertise developed in the electronics area (i.e. processing, wafer-level testing and chip packaging) can be revamped for data transmission. Thus, since the early years of the technology, the driving force behind the commercial deployment of silicon-photonics (SiPh) has been the optical interconnects for data-centers. Since the beginning of the 2000s, extensive research is being conducted in order to improve the performance of SiPh lasers, photodiodes, modulators, waveguides and couplers. In fact, all the photonics devices necessary to build a complete photonic transceiver are avaliable, except for the laser source, which remains challenging. However, also in this point, the use of bonding and epitaxial growth of III-V materials on silicon have been accomplished, creating so called hybrid silicon lasers. Silicon couplers and waveguides, achieve propagation losses of less than 1 dB/cm [70]. Very fast photodiodes, with bandwidth exceeding several tens of GHz have been also demonstrated [71, 72].

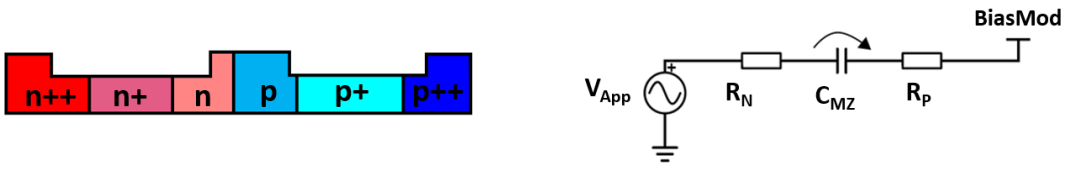
3.3.1 SiPh Mach-Zehnder modulator

On the modulator side, while InP-based MZMs make use of various E/O effects such as Pockels and Kerr effects, these phenomena are absent in unstrained silicon, and modulation achieved by means of the plasma dispersion effect, in which free-carrier density variations induce changes in the excess loss and in the refractive index [73]. Two different mechanisms are used for the free-carrier manipulation, namely depletion or accumulation. The first, represented in Figure 3.21a, uses a lateral pn-junction embedded in a rib waveguide. The diode works under reverse bias where the width of the depletion region changes as a function of the voltage across the diode. Since there exists no free carrier in the depletion region, the effective index of the waveguide also changes with the voltage. The second mechanism, represented in Figure 3.21b, is based on a silicon-insulator-silicon capacitor (SISCAP) structure with a very thin oxide layer (5



(a) (b)

Figure 3.21: Cross-section of: (a) depletion-type and (b) accumulation-type phase shifters [73].



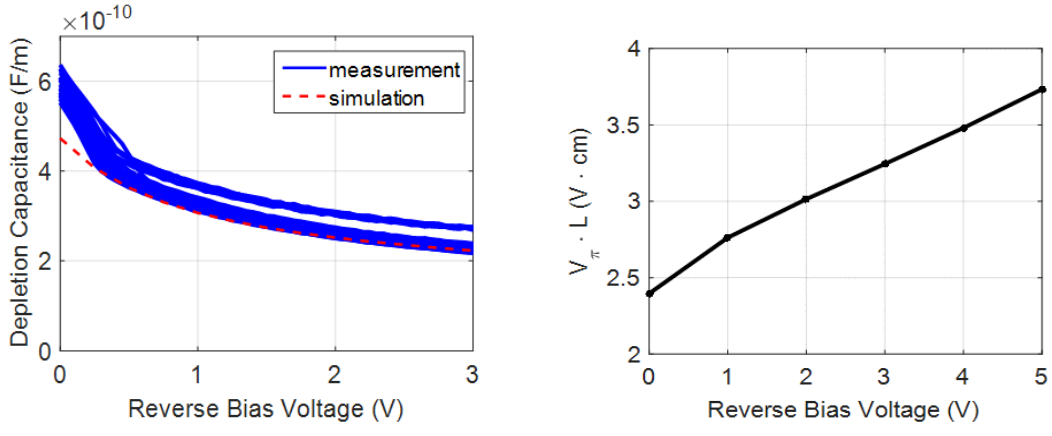
(a) (b)

Figure 3.22: SiPh MZM segment: (a) cross section, (b) electrical model.

to 10 nm) between a SOI layer in the bottom and a poly-Si on the top. The accumulated charges on the top and bottom of the oxide capacitor are changed by the applied voltage for phase modulation. Due to the better mode overlap and higher free-carrier densities, the modulation efficiency of SISCAP is an order of magnitude higher than that of the depletion mode phase shifter, but also has a significantly higher absorption loss and capacitance. Depletion-type MZMs are the most popular for high-speed operation in the generic SiPh processes because they are easy to implement and do not require process customization [20, 73].

3.3.1.1 Si SEMZM: electrical modeling

The SiPh SEMZM available in the IHP EPIC platform, is a depletion-type MZM with an efficiency of 2.9 Vcm at a reverse bias voltage of $\sim 1.5\,V$ and ~10 dB/cm IL. The light is coupled in and out of the chip using two standard grating couplers. The MZM structure implemented in the Tx module has a length of 5.7 mm and is divided into 15 equal segments of 380 μm. Each segment has an active length of 378 μm and the separation between segments is 2 μm. These segments can be considered as lumped up to ~38 GHz, according to the $\frac{\lambda}{10}$ criteria, considering a microwave index of 2.1. The electrical equivalent is given by a series resistance and a load capacitance, as depicted in Figure 3.22b with the values of 25 Ω for $R_p + R_n$ and 150 fF for C_{MZ} for a reverse bias of 1.5 V. The operating point of the MZM is set by 1.5 mm long thermal tuning sections (resistive heaters with R~ 120 Ω). A reduction of around 50% (from the initial 50 Ω) in the series resistance has been achieved by the inclusion of additional implants (n++, p++), as shown in the cross section depicted in Figure 3.22a, at



(a) (b)

Figure 3.23: (a) Capacitance and (b) efficiency of the modulator with reverse bias voltage.

the expense of less than 20% increase in the IL, and without influence in the MZM efficiency. An external DC voltage is applied from the outside to the p-sides in order to set the reverse bias voltage of the junction. In Figure 3.23 the measured and simulated depletion capacitance and the efficiency change with applied voltage is shown. The measurement curve represents multiple chips in order to show the deviation from the simulated curve.

3.3.1.2 E/O co-simulation

One of the major advantages of the monolithically integrated approach is the availability of a E/O co-simulation environment. Such co-simulation incorporates the electrical and optical domains together in one simulation [74] permitting the evaluation of the ensembled behavior and easing design optimization. Two main properties are modeled in this simulation: the electrical equivalent of the modulator and the E/O conversion. The electrical equivalent accounts for the junction capacitance and resistance, originated from the carrier transport dynamics, and determine the overall bandwidth of the Tx module. The modeling of the E/O conversion provides a simulation test-bench, where it is possible to have an optical output to analyze the full Tx performance and compare it with E/O measurements. The optical components such as phase shifters, MMIs and DC tuning sections are implemented into Cadence Virtuoso by creating instances using VerilogA. The segmented driver is also simulated in the same platform and consequently the optical and electrical components are easily combined together so as to predict the overall E/O response.

3.3.2 Tx module implementation

The implementation of this Tx module is analogous to the hybrid implementation described in section 3.2. In this case, since C_{Pad}=0, (3.11) becomes as in (3.14). It can be seen that the power consumption increases quadratically with the delivered voltage but only linearly with the MZM length. Therefore, in terms of power consumption only, longer modulators would be beneficial. However, due to the low efficiency of the Si-depletion MZM, very long modulators would also incur in too high IL, and beyond a certain L, RF losses along the transmission line become also a limiting factor. As a compromise, 3.3 Vppd for V_A and a modulator of 5.7 mm length are selected.

$$P_{TOT} = cte \cdot BW(V_{App}^2 + cte \cdot V_{App}) \cdot L \tag{3.14}$$

The block diagram of this module is presented in Figure 3.24a, comprising as well 15 segments to achieve the 4-bit resolution. The RF inputs that conform the B2T encoder are routed with 50 Ω single-ended transmission lines which enables the on-wafer verification of all bits with a quad probe. The length of the line between segments was designed to overcome the difference between the electrical and optical microwave indexes, with values of 3.6 and 2.1 respectively, matching the resulting optical delay per segment of 4.6 ps. As in the previous case, each line is terminated by a 50 Ω resistor, connected to the common mode voltage (Ref_CMI) that is produced on chip from a LDO with a bandgap reference. An on chip capacitor (C in Figure 3.24a) of 1.8 nF is used to bring the required AC ground down to a low cut-off frequency of 100 MHz which can be further de-creased by an on-board capacitor connected to a

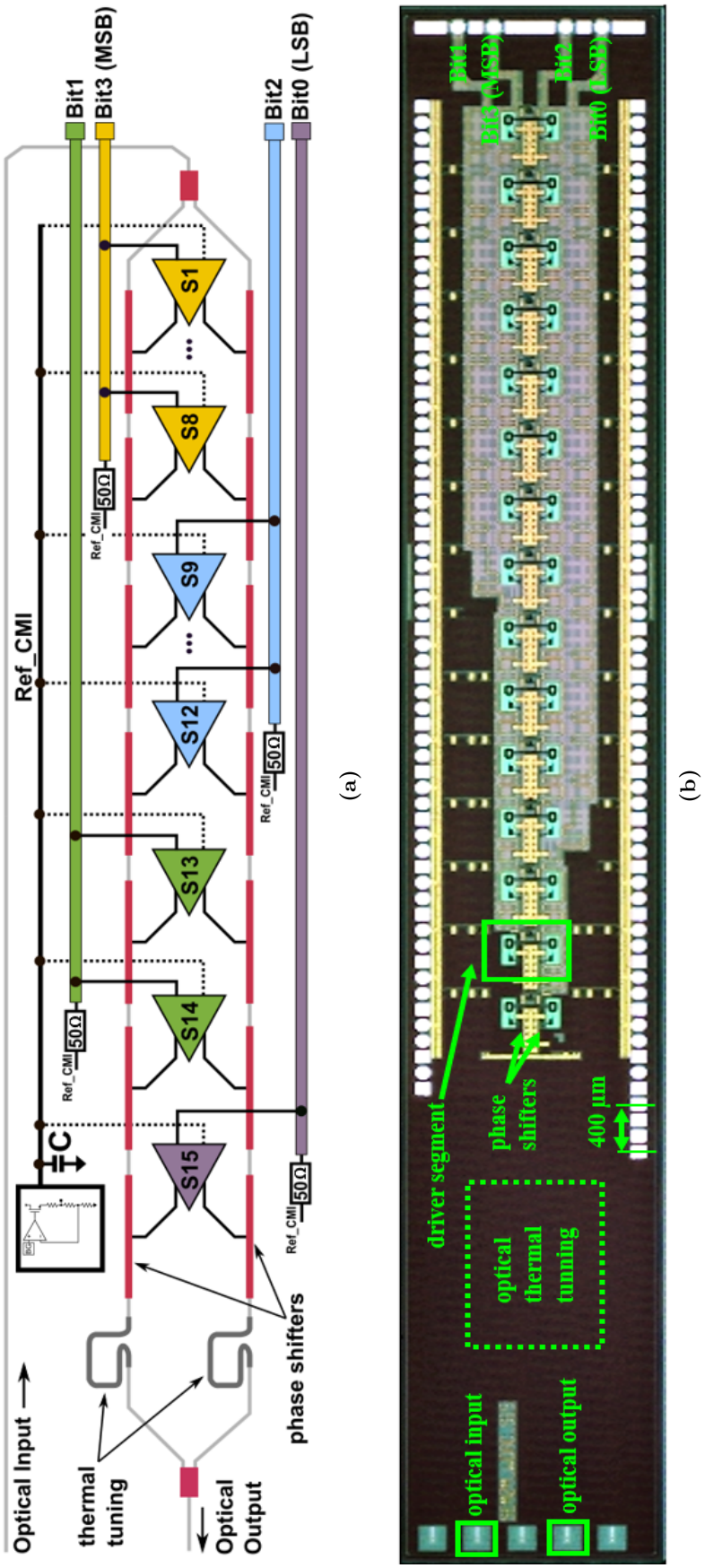


Figure 3.24: EPIC Tx with integrated 4-b DAC: (a) block diagram and (b) corresponding chip microphotograph.

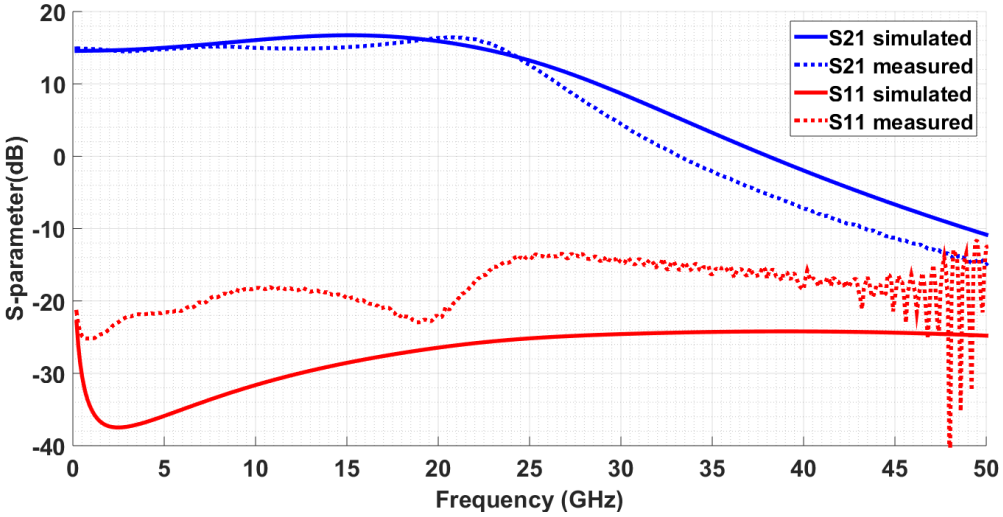


Figure 3.25: Measured vs. simulated S-parameters of driver core.

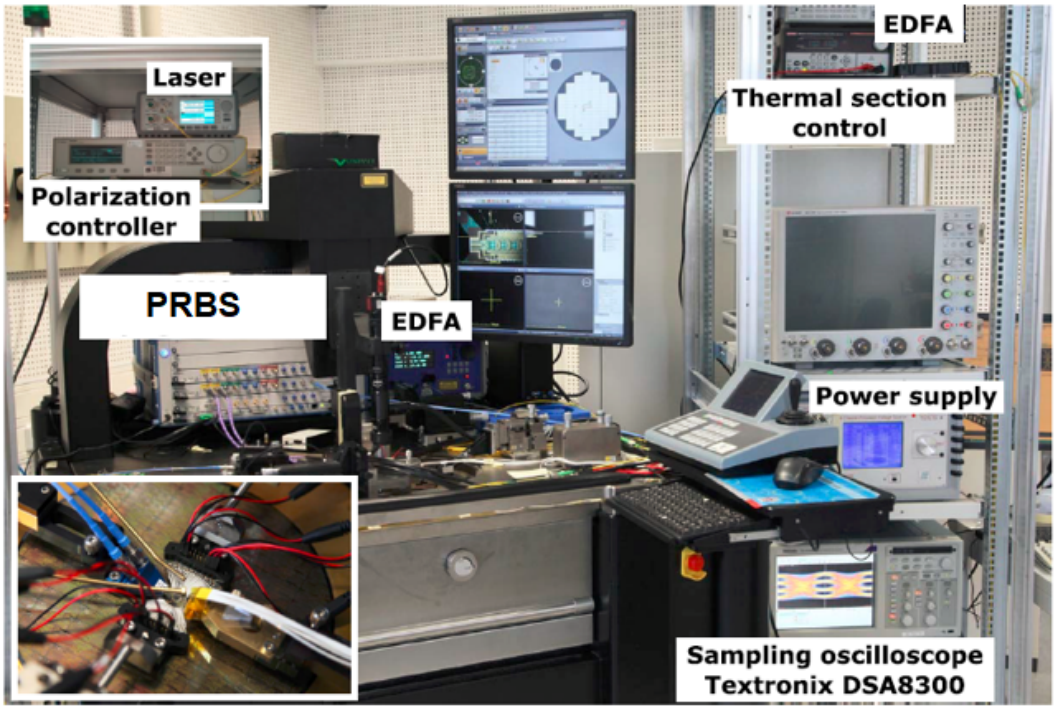


Figure 3.26: On-wafer E/O measurements setup.

reserved pad. The driver core design is also analogous to the previous case, but the sizing of the components and peaking structures has been optimized for this technology and to handle the larger series resistance of the modulator. Negative capacitance compensation with C_N ∼36 fF, as well as T-coil peaking with (L∼220 pH, k∼0.5) were used. The driver delivers 3.3 Vppd to the MZM and each core dissipates ∼85 mW. Figure 3.24b shows the chip microphotograph, with area of 14.5 mm^2. Since in this case there are no constraints on the layout, the driver is positioned in the middle, between the modulator arms, for optimal symmetry. The optical interface can be seen on the left side.

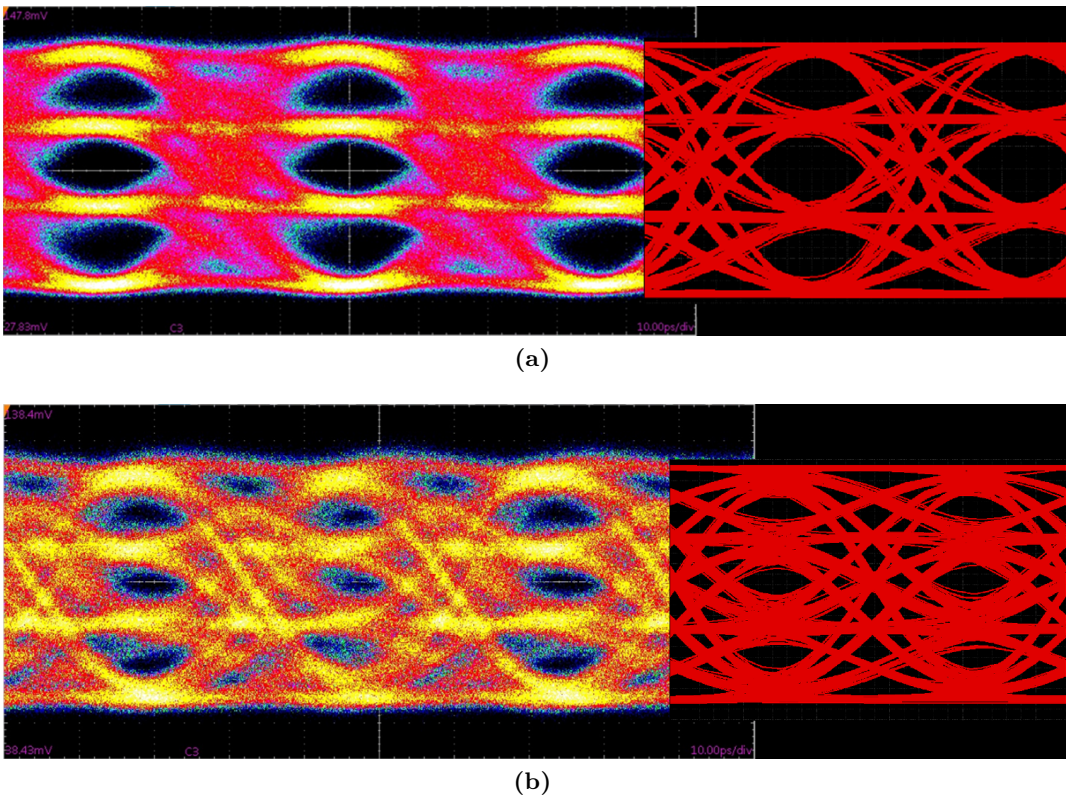


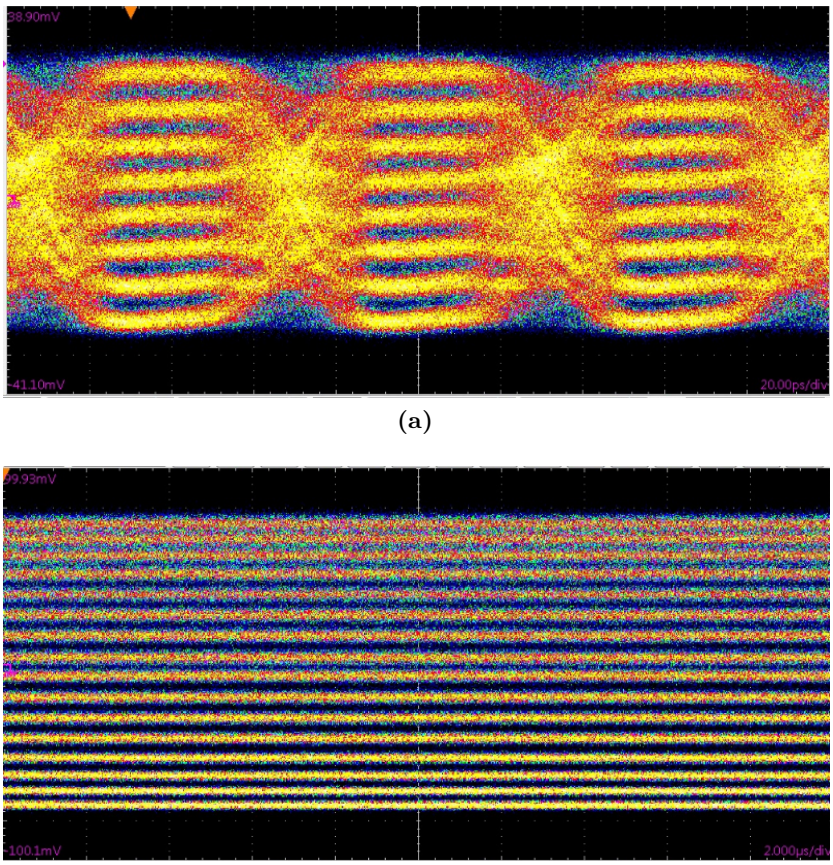
Figure 3.27: Measured PRBS31 E/O eye diagrams: (a) at 28 GBd and (b) at 37 GBd, compared to post-layout co-simulation results.

3.3.3 Functionality verification

In addition to the integrated Tx, a chip containing only one segment of the multichannel driver, without modulator load, was fabricated and electrically characterized in the frequency domain. Small signal S-parameter results are presented in Figure 3.25, compared to post-layout simulation results. Input matching is better than -10 dB up to 50 GHz.

E/O characterization of the Tx in the time domain in 2-bit operation has been carried out via on-wafer probing with the MZM biased in the quadrature point. A 1550 nm laser signal was amplified with an EDFA and fed to the optical input. At the output a second EDFA was used to amplify the signal before the PD connected to the input of the sampling scope. At the electrical input, two de-correlated PRBS31 patterns were connected to the Bit_3 and Bit_2 inputs (according to Figure 3.24a), with an amplitude of 600 mVpp. A photo of the E/O measurement setup is presented in Figure 3.26. Figure 3.27 shows the E/O eye diagrams of the PAM-4 modulation at 28 and 37 GBd compared to the co-simulation results. The closing in the 37 GBd middle eyes is attributed to imperfect synchronization between the inputs. The total power consumption in this configuration amounts to 1 W which translates into an efficiency of 13.5 pJ/bit at 74 Gb/s.

To confirm the full functionality of the 4-bits, the operation of the other two Bit_1 and Bit_0 (LSB) was also verified at low speed, producing PAM-8 eye diagrams as seen in Figure 3.28a and PAM-16, as in Figure 3.28b, when all four bits are connected.



(a)

(b)

Figure 3.28: Measured PRBS31 E/O eye diagrams: (a) PAM-8 at 16 GBd and PAM-16 at 1 GBd.

3.4 Comparison with state-of-the-art

Table 3.2 presents a summary on the performance of recently published Tx modules based on the same optical-DAC principle which so far has been explored in the literature by means of CMOS electronics only. State-of-the-art modules are based on the hybrid integration of short Si SEMZMs together with drivers in advanced CMOS nodes. Very high efficiencies of up to 2.8 pJ/bit have been demonstrated by underdriving the MZM, which significantly limits the transmission reach. By using high speed BiCMOS drivers, the here presented hybrid Tx module has enabled the signal generation with the highest order modulation format (256-QAM) at the highest speed (32 GBd) with record low energy-per-bit of 6.4 pJ/bit, among the coherent modules, transmitted over 120 km of SMF. The EPIC module demonstrates the highest transmission speed among silicon-based modulators, at the expense of a higher power dissipation attributed to the higher Vπ ratio delivered and to the lower efficiency of the MZM. Such performance evidences the suitability of the driving scheme with fast SiGe HBT drivers towards the realization of fully driven devices in small area at high speeds, in order to achieve high ERs essential for coherent applications.

3.5 Summary

Two Tx modules, an hybrid one and a monolithically integrated one, both featuring 4-bit integrated DAC functionality have been presented. The hybrid Tx module comprises an

Ref.	[59]	[60]	[75]	[76]	This-Hybrid	This-EPIC
Year	2015	2015	2016	2016	2016	2018
Driver Technology	40 nm CMOS	90 nm CMOS	32 nm CMOS	0.13 um RF CMOS	0.13 um BiCMOS	0.25 um BiCMOS
Data-rate (GBd)	28	28	23	16	32	37
MZM-type	SiPh Accumul.	SiPh Depletion	SiPh Depletion	SiPh Depletion	InP	SiPh Depletion
VπL (Vcm)	0.2	1.47	2.04	-	0.33	2.9
Wavelength (nm)	1550	1300	1300	-	1550	1550
IL (dB)	25	5	-	-	8	-
MZM length (mm)	1	3	1.8	3	3.375	5.67
nº bits	2	2	2	2	4	4
Out Swing (Vppd)	1 (0.5Vπ)	2.2 (0.44Vπ)	2 (0.17Vπ)	4	2.5 (2Vπ)	3.3 (0.65Vπ)
Modulation Format	16-QAM	4-PAM	4-PAM	4-PAM	256-QAM	4-PAM
Power (W)	0.5	0.27	0.13	0.38	1.64	1
Energy per bit (pJ/bit)	8.9	4.8	2.8	9.8	6.4	13.5

Table 3.2: State-of-the-art comparison of Tx with integrated DAC.

InP I/Q-SEMZM and two 0.13 μm SiGe:C BiCMOS drivers integrated in a package with footprint of 28 mm $\times$ 76 mm. The drivers deliver up to 2.5 Vpp differential output voltage while dissipating less than 1 W of power each, at maximum. The electrical performance of the stand-alone drivers has been characterized and clear eye diagrams up to 40 Gb/s data rate are reported. Signal generation and transmission over 120 km of SMF of DP 256-QAM at 32 GBd has been demonstrated with 6.4 pJ/bit energy consumption. The hybrid module demonstrates the highest order modulation format with record low energy-per-bit among the coherent modules. The monolithically integrated Tx was fabricated in the 0.25 μm SiGe:C BiCMOS EPIC technology. The driver delivers 3.3 Vppd to the modulator, while dissipating 1.27 W. The module occupies an area of 14.5 mm^2 and features 13.5 pJ/bit energy efficiency at 37 GBd in PAM-4 (2-b) operation. This is the highest baud rate demonstrated among depletion-type Si MZMs, evidencing the advantages of the proposed driving approach with HBT transistors.

4

Low-Noise Differential Receiver Front-Ends

On the receiver (Rx) side of the optical transceiver, the transimpedance amplifier (TIA) as the front-end device, is the most critical building block and it significantly influences the signal quality and overall system performance. In particular, the sensitivity of the TIA will determine the power level at which the channel needs to operate (i.e. the tolerable channel loss) and thus, the development of a low-noise TIA is the key to creating a low-power optical link, already from the transmitter (Tx) side. Alternatively, for a given transmit power, higher sensitivity allows data transmission over longer distances. Apart from optical communications, high-sensitivity TIAs are required in a broad range of other applications: particle/raditation detector chips, vision sensor chips, biological sensor chips, motion sensors in MEMS and wideband radio receivers. This chapter describes the design methodology for differential linear TIAs optimized for low averaged input referred noise current density while preserving large bandwidth for high-speed, high-sensitivity operation.

4.1 Introduction

The goal of the TIA in the optical Rx is to amplify the electrical current produced by the photodiode (PD) and convert it to a voltage level reliable for the decision circuit while adding as low noise as possible, maximizing the bandwidth and minimizing the power consumption [77]. Simultaneous sensitivity and bandwidth optimization is still a fundamental challenge in TIA design. TIA topologies featuring very low input impedance such as common-base or regulated cascode [78] aim at relaxing the effect of the input capacitance for enhancing the bandwidth, but they incur in high current noise contribution, degrading the sensitivity [14]. Shunt-feedback TIAs are well-known for their low-noise characteristics, and are the workhorse for bipolar TIA implementations. However, high-frequency operation requirement limits the maximum value of the feedback resistor [50] and therefore, the maximum sensitivity. In conventional system dimensioning, the input impedance of the shunt-feedback TIA is chosen according to the input

capacitance so that the small-signal bandwidth (BW) corresponding to the RC-constant at the input node satisfies the rule of thumb (4.1), where B stands for the target data-rate.

$$BW_{3dB} \sim \frac{2}{3}B \tag{4.1}$$

If the bandwidth of the receiver is wide enough such that the signal waveform remains undistorted, the signal picks up a lot of noise, which translates into a low receiver sensitivity. Alternatively, if the BW of the receiver is too narrow such that most of the noise gets filtered out, the signal suffers from inter-symbol-interference (ISI). ISI impacts negatively the sensitvity as well, by reducing the signal swing in a bit-pattern dependent manner [14]. The rule of thumb (4.1) is typically chosen as a compromise between low ISI and good noise performance. To break this tie between noise and BW, different techniques such as π-network matching at the input or between stages [54] use inductors to tune out the parasitic capacitances, effectively extending the bandwidth without integrating the noise at higher frequencies. However, the effect is still moderate: $22.42\,\mathrm{pA}/\sqrt{Hz}$ for 50 GHz bandwidth in 65 nm CMOS [79]. A more effective approach based on post-amplifier equalization has been introduced in [80] and exploited in 65 nm CMOS for the first time in [78] and [81], for improving sensitivity without sacrificing bandwidth, achieving $15.3\,\mathrm{pA}/\sqrt{Hz}$ for 18 GHz bandwidth in [78] and $17.8\,\mathrm{pA}/\sqrt{Hz}$ with 21.4 GHz bandwidth in [81]. The TIA topology described next makes use of a low-bandwidth shunt-feedback input transimpedance stage which integrates substantially less noise, together with multi-stage equalization and input series peaking, which recover the target bandwidth. The proposed design methodology is then verified by means of analogous TIA implementations in the SG13S and SG13G2 processes (in the following referred as 13S-TIA and G2-TIA, respectively) in order to evaluate the technology role and limitations in the circuit performance. The noise-bandwidth trade-off is shown to be surpassed, with designs that feature less than $10\,\mathrm{pA}/\sqrt{Hz}$ averaged input referred current noise density while operating at 100 Gb/s data rate. The implemented ICs are well matched at the input and output to 50 Ω by means of reactive structures and can also be seen as general-purpose low-noise cascadable gain blocks for different applications [82].

4.2 Low-noise design methodology

4.2.1 Noise sources

The overall noise performance of an amplifier is closely related to the noise characteristics of the individual devices that form the amplifier circuit. Three major noise sources are present in any realizable amplifier:

Thermal noise: This noise, also called Johnson noise [83], is present in resistances, and results from the thermally induced random fluctuations in the charge carriers. At temperatures above absolute zero, the amount of random motion induced in the carriers of the resistor material is a direct function of the temperature. As a whole, the resistor will exhibit charge neutrality, but on a microscopic level the agitated free carriers originate local charge gradients which produce a wideband random voltage fluctuation appearing in series with the resistance.

The power spectral density for the thermal noise is essentially that of white-noise and it exhibits Gaussian statistics [84]. The open circuit RMS voltage is given by :

$$V_n \leq \sqrt{4kTBWR} \quad V_{rms} \tag{4.2}$$

where k is Boltzmann's constant (1.38×10^{-23} J/^{0}K), T is the absolute temperature in Kelvin and BW is the observation bandwidth in Hz. This noise is present in all electronic devices containing a resistance that dissipates energy. It can be modelled using the superposition principle by replacing the noisy resistor with the combination of a noise-free resistor either in series with a voltage-noise generator or in parallel with a current-noise generator. In the voltage-noise model, the spectral density increases with increasing R, as in (4.2), while in the current-noise model the current noise spectral density decreases with increasing R.

Shot noise: An electrical current is composed of individual carriers each transporting q coulombs of charge through the circuit. The shot noise is associated with the passage of these carriers accross a potential barrier [85]. Potential barriers occur in p-n junctions in semiconductor diodes and junction transistors and therefore electronic shot-noise is associated with each diode or junction transistor used in the TIA circuitry. The shot noise is described by a Gaussian distribution with a white power spectral density [84]. Because this noise is associated with current flow, it is naturally modeled as a current-noise source in parallel with the device. The normalized power spectral density of electronic shot-noise is given by:

$$I_n^2(f) \leq 2qI_{DC} \quad A^2/Hz \tag{4.3}$$

where q is the electronic charge, 1.602×10^{-19} C, and I_{DC} is the current flowing.

1/f noise: This kind of noise, also known as Flicker noise, appears in virtually all electronic devices. It is usually thought to be originated by the imperfections in the semiconductor materials [86]. It appears only at very low frequencies, and it is typically very small in Silicon bipolar transistors in which the 1/f noise becomes noticeable in the tens of KHz region [84]. Thus, it is not of concern for optical Rx design, since it will appear below the low cut-off frequency.

4.2.2 Circuit techniques

In the following, the analysis of the noise and bandwidth relationship for the case of a classical shunt-feedback TIA topology in a bipolar front-end is presented. The design constraints of this implementation are discussed and shed light into the extent up to which an equalization method as the one used here transcends the aforementioned noise-bandwidth compromise.

In Figure 4.1, a shunt-feedback TIA with post-amplification is presented with the main noise sources annotated as corresponding to a bipolar implementation. For the general case of a second-order system comprising a core amplifier with gain A, and cut-off frequency f_0,

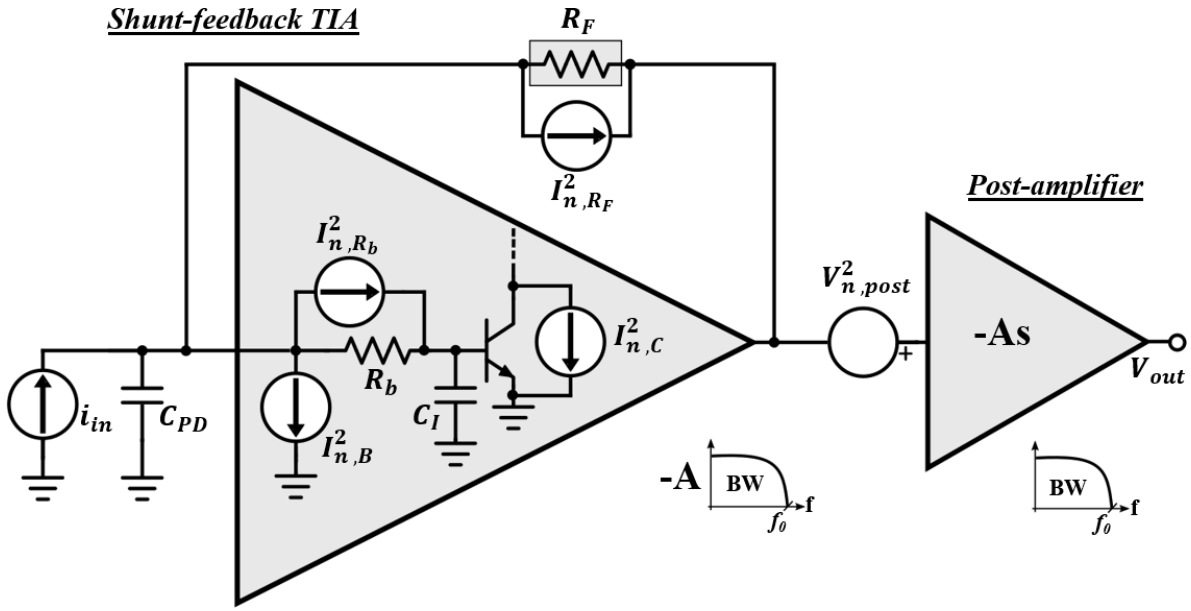


Figure 4.1: Front-end of optical receiver in classical cascaded approach comprising bipolar shunt-feedback TIA stage and post-amplifier.

the transimpedance limit, formulated as in (4.4), derived in [87], describes the maximum transimpedance gain that a TIA can attain for a given BW and technology (f_T):

$$\begin{aligned} R_F &\leq Af_0/(2\pi C_T BW^2) \\ R_F &\sim f_T/(2\pi C_T BW^2) \end{aligned} \tag{4.4}$$

where C_T is the total input capacitance obtained as the sum of the parallel input capacitance of the amplifier (C_I) and the capacitance of the photodiode (C_{PD}). Inequality (4.4) reveals that the transimpedance degrades quadratically with the bandwidth, and not linearly, if the input capacitance is constant. The transimpedance limit produces a rapid degradation of the sensitivity in high bandwidth applications, since for a desired BW it sets an upper bound to R_F which, as will be shown in the following, is one of the dominant noise sources. The contributions to the input referred noise in Figure 4.1 are as follows: $I^2_{n,R_F} = 4kT/R_F$ is the feedback resistor thermal noise and contributes directly to the input. From the amplifier, there is the shot noise generated by the base current which is given by $I^2_{n,B} = 2qI_C/\beta$ and adds directly to the input; the shot noise generated by the collector current, given by $I^2_{n,C} = 2qI_C$ and the thermal noise generated by the intrinsic base resistance, given by $I^2_{n,R_b} = 4kT/R_b$, and both must be referred to the input [50]. Finally, the noise of the post-amplifier stage is modeled with voltage source $V^2_{n,post}$, and must be divided by the TIA transimpedance transfer function $|Z_T(s)|$ to find its contribution in the input noise. It is also assumed that the gain of the core amplifier is $A \gg 1$, so that the noise contributions of the amplifier load can be neglected and $|Z_T(s)|$ equals R_F at low frequency [50]. The total input referred noise spectrum for the case of shunt-feedback TIA with post-amplification $I^2_{n,in,TOT}$, is given by:

$$I^2_{n,in,TOT} = I^2_{n,R_F} + I^2_{n,amp} + I^2_{n,post} \tag{4.5}$$

where [50]:

$$I_{n,amp}^2(f) = \frac{2qI_C}{\beta} + 4kTR_b\left(\frac{1}{R_F^2} + (2\pi f C_{PD})^2\right) + \frac{2qI_C}{g_m^2}\left(\frac{1}{R_F^2} + (2\pi f C_T)^2\right) \tag{4.6}$$

neglecting base shot noise it results:

$$I_{n,amp}^2(f) = \frac{4kTR_b}{R_F^2} + \frac{2qI_C}{g_m^2 R_F^2} + \frac{2qI_C(2\pi C_T)^2}{g_m^2} f^2 + 4kTR_b(2\pi C_{PD})^2 f^2 \tag{4.7}$$

For calculating the contribution from the post-amplifier, $Z_T(s)$ must be obtained. Considering the typical case of a shunt-feedback TIA with a Butterworth response for maximally flat gain, the TIA frequency response is given by [50]:

$$|Z_T(s)|^2 \approx R_F^2 / \left|1 + \frac{s}{2\pi BW}\right|^4 \tag{4.8}$$

and then, the post-amplifier contribution to the input noise will be given by:

$$I_{n,post}^2(f) = \frac{V_{n,post}^2}{R_F^2}\left(1 + \left(\frac{f}{BW}\right)^4\right) \tag{4.9}$$

and therefore, the total noise:

$$\begin{aligned} I_{n,in,TOT}^2 = {} & \frac{4kT}{R_F} + \frac{4kTR_b}{R_F^2} + \frac{2qI_C}{g_m^2 R_F^2} + \frac{2qI_C(2\pi C_T)^2}{g_m^2} f^2 \\ & + 4kTR_b(2\pi C_{PD})^2 f^2 + \frac{V_{n,post}^2}{R_F^2} + \frac{V_{n,post}^2}{R_F^2}\left(\frac{f}{BW}\right)^4 \end{aligned} \tag{4.10}$$

where the most dominant components, correspond to the white thermal noise contribution of the feedback resistor and the f^2 term of the base resistance. From (4.4) and (4.10) the trade-off between bandwidth and noise in this implementation becomes evident, and standalone minimization of the dominant noise contributors in (4.10) would directly degrade the bandwidth: increasing R_F reduces its thermal noise but reduces the bandwidth quadratically; reducing the base resistance (R_b) of the input transistors by augmenting their size increases the input capacitance and deviates the biasing condition from the peak f_T, both effects reducing bandwidth, and for the same I_C increases the collector noise. It is here that the benefit of post-amplifier equalization strikes in by effectively decoupling these two entities. Instead of having both stages with the same BW, the input stage is designed with a lower bandwidth (BW/n), and the post-amplifier provides peaking at the higher frequencies, equalizing the gain such that the total bandwidth is restored to BW. In this case, from (4.4) the feedback resistor

in the TIA must increase proportionally to n^2 in order to keep the same transimpedance gain − BW product. Replacing in (4.10) the term R_F with $n^2 R_F$ and BW with (BW/n) then:

$$\begin{aligned} I^2_{n,in,TOT} = &\frac{4kT}{n^2 R_F} + \frac{4kTR_b}{n^4 R_F^2} + \frac{2qI_C}{g_m^2 n^4 R_F^2} + \frac{2qI_C(2\pi C_T)^2}{g_m^2} f^2 \\ &+4kTR_b(2\pi C_{PD})^2 f^2 + \frac{V^2_{n,post}}{n^4 R_F^2} + \frac{V^2_{n,post}}{n^4 R_F^2}\left(\frac{f}{BW/n}\right)^4 = \\ &\frac{4kT}{n^2 R_F} + \frac{4kTR_b}{n^4 R_F^2} + \frac{2qI_C}{g_m^2 n^4 R_F^2} + \frac{2qI_C(2\pi C_T)^2}{g_m^2} f^2 \\ &+4kTR_b(2\pi C_{PD})^2 f^2 + \frac{V^2_{n,post}}{n^4 R_F^2} + \frac{V^2_{n,post}}{R_F^2}\left(\frac{f}{BW}\right)^4 \end{aligned} \tag{4.11}$$

It can be seen how the frequency dependent terms (f^2 and f^4) from (4.11) are the same as in (4.10) but the thermal noise from the feedback resistor has been reduced by a factor of n^2 and the other DC noise components from the amplifier and post-amplifier noise have been reduced by a factor of n^4, which even for low values of n, essentially eliminates them. Therefore, although the post-amplifier contributes now with in-band input-referred noise starting the ramp-up at f=BW/n, having reduced its DC noise magnitude by an n^4 factor, its contribution to the input-referred noise amounts, on the whole, to a lower value. This can be clearly seen in Figure 4.2.

This approach will be useful as far as the post-amplifier is able to restore the bandwidth; if too aggressive peaking is used, it might be difficult to preserve gain and group delay flatness over frequency, inducing data-dependent jitter which compromises signal integrity and pulse fidelity. This effectively limits the extent of bandwidth reduction of the first stage. Following this approach, the TIAs presented in the next section target to achieve a low noise level at the input while still maintaning a bandwidth above $\sim 45\,\mathrm{GHz}$.

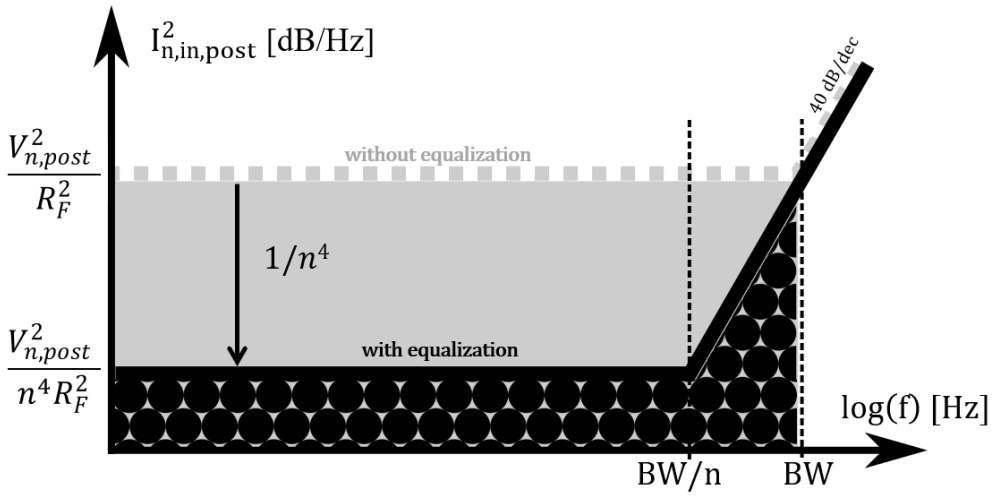


Figure 4.2: Graphic representation of contribution of post-amplifier noise over frequency.

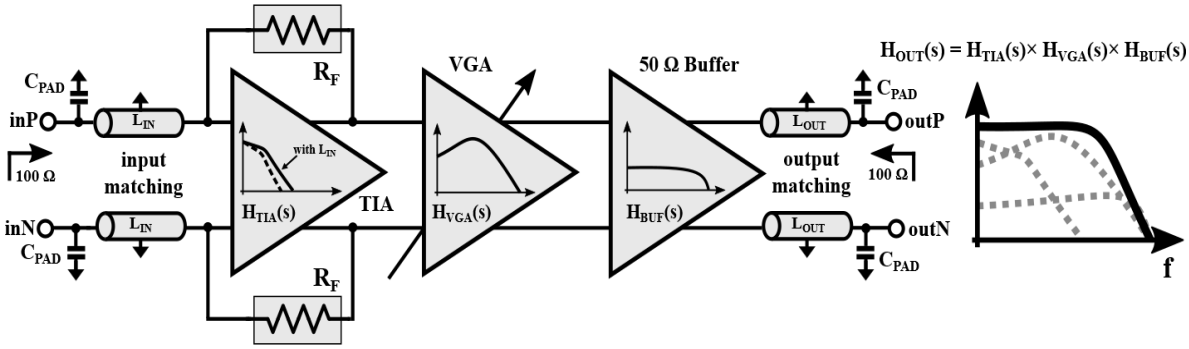


Figure 4.3: Block diagram of the TIAs.

4.2.3 Technology role

The noise performance of HBTs, expressed in terms of the minimum noise figure (NF_{min}), is strongly dependent upon both the DC current gain (β) and the f_T/f_{max} figures, as given by (4.12) from [88] where n is the collector current quality factor and R_e is the emitter resistance.

$$NF_{min} = 1 + \frac{n}{\beta} + \frac{f}{f_T}\sqrt{\frac{2qI_c(R_e + R_b)}{kT}(1 + \frac{f_T^2}{\beta f^2}) + \frac{n^2 f_T^2}{\beta f^2}} \tag{4.12}$$

Since the SG13G2 technology features lower β, the noise performance at the lower frequencies will be limited. On the other hand, due to the higher f_T and lower R_b (from the higher f_{max} [88]) than the SG13S process, the $NFmin$ with increasing frequency will be lower. This has been graphically represented in [89] for both processes at 25 GHz, and it can be seen that for collector current densities above $5\,mA/\mu m^2$ the NF_{min} from the SG13G2 technology is $\sim 1\,dB$ lower than for the SG13S. Below that biasing condition, however, the lowest NF_{min} is achieved, with both technologies performing similarly in terms of noise.

4.3 Transimpedance amplifiers with sub-10pA/$\sqrt{Hz}$ at 100 Gb/s

The block diagram of the TIAs is depicted in Figure 4.3 and it comprises five blocks: input matching structures, input transimpedance stage, variable-gain-amplifier (VGA), 50 Ω buffer and output matching structures. The amplification is divided in three stages: the input TIA stage amplifies the low frequency part and will feature a bandwidth that is less than two times the value of the total bandwidth finally achieved. The second stage, a VGA with capacitive degeneration, has a bandpass-like characteristic providing peaking in the middle frequency range. Shunt peaking is used in the output buffer and series peaking is used at the input of the TIA, in order to raise the transimpedance gain at the higher frequencies. The input inductor has the additional benefit of improving the high frequency matching since 50 Ω interface is targeted.

4.3.1 Circuit implementation

The design follows a fully differential linear architecture suitable for a coherent receiver implementation. As described in Chapter 2, on the Rx, differential signaling is especially

Parameter	Value	Parameter	Value
L1	2 µm×370 µm	R_{E1}	40 Ω
L2	0	R_{E2}	17 Ω
L3	0	Q1-Q2	8×120×840 nm^2
L4	2 µm×120 µm	Q3-Q4	4×120×840 nm^2
L5	6 µm×350 µm	Q5-Q10	4×120×840 nm^2
R_F	550 Ω	Q11-Q12	2×120×840 nm^2
R_{C1}	130 Ω	Q13-Q14	8×120×840 nm^2
R_{C2}	150 Ω	C_{deg}	10×974×800 nm^2

Table 4.1: 13S-TIA design parameters summary.

Parameter	Value	Parameter	Value
L1	2 µm×60 µm	R_{E1}	40 Ω
L2	2 µm×240 µm	R_{E2}	18 Ω
L3	2 µm×140 µm	Q1-Q2	10×70×900 nm^2
L4	2 µm×130 µm	Q3-Q4	5×70×900 nm^2
L5	5 µm×330 µm	Q5-Q10	6×70×900 nm^2
R_F	480 Ω	Q11-Q12	5×70×900 nm^2
R_{C1}	160 Ω	Q13-Q14	10×70×900 nm^2
R_{C2}	150 Ω	C_{deg}	10×974×800 nm^2

Table 4.2: G2-TIA design parameters summary.

desirable as it brings improved immunity to power-supply and substrate noise and superior rejection to parasitically copuled signals. Vulnerability to common-mode noises would be particularly severe in applications involving multi-channel parallel optical receivers for above 100 Gb/s and therefore, fully differential signaling is required already at the input stage of the Rx. Differential input TIAs find application in Rxs with balanced detectors as sketched in Figure 4.4. Moreover, they can produce twice the voltage swing, compared with single-ended TIAs, which is desirable for low-voltage systems and they avoid the need for a reference voltage to connect to the post-amplifier stages. The differential TIA responds to the differential photocurrent as $V_{OutP} - V_{OutN} = Z_T / I_{diff}$. The two matched photodetectors present a balanced input impedance, such that any noise on the power supply or substrate will couple equally to both inputs. The analysis made in the previous section remains valid for the differential case [14], by replacing single-ended voltages and currents by the differential ones.

The complete schematic of the RF path of the implemented TIAs is presented in Figure 4.5. A common-emitter shunt-feedback topology with constant transimpedance gain was selected for the input TIA stage, with transistors (Q1-Q2). In a variable transimpedance stage, a MOS transistor working in the triode region is connected in parallel to the R_F; by changing the gate potential of the MOS transistor, the equivalent feedback impedance can be tuned. However, in this case the gain of the main amplifier formed by the Q1-Q2 pair and the collector resistor R_c has to be accordingly adjusted in order to keep stability (using a second MOS transistor in parallel), which complicates the gain control circuitry [90]. Therefore, a constant transimpedance stage followed by a VGA is preferred. A variable transimpedance stage at the input is required in applications with a very high dynamic range such as burst-mode TIAs

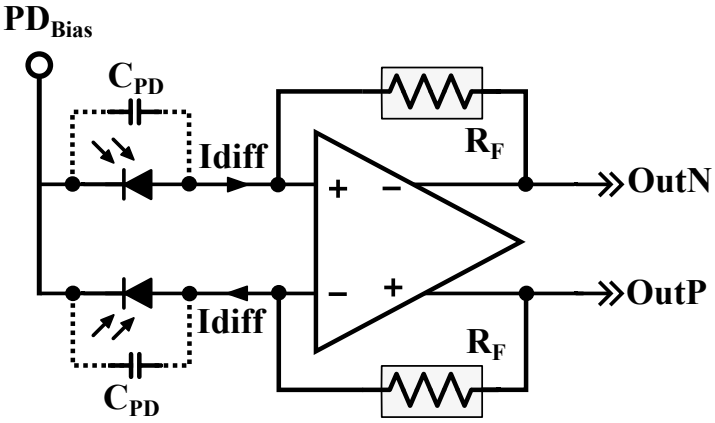


Figure 4.4: Rx with balanced inputs.

[14]. Emitter followers (Q3-Q4) precede the feedback resistors and the second stage, for level shifting and buffering. This input stage is biased with a tail current that might be adjusted with the BiasI pin which controls as well the bias of the second stage. The biasing of the input stage is set to $\sim$5 mA/μm^2 collector current density, which according to [89] falls in the region of lowest NF_{min}.

Following the TIA, a VGA is used to maintain linearity, reducing jitter and pulse width distortion for high input currents. The VGA provides a 15 dB gain-controlled range while maintaining constant bandwidth during gain tuning. A current-steering topology has been used to meet these requirements, where the gain is controlled with the Vc-Vcb difference. This topology was preferred over a conventional Gilbert-cell based VGA because having only one collector connected to the load resistors it features larger bandwidth. The Vc-Vcb difference is generated with the circuit presented in Figure 4.6, which by using a bandgap reference requires only one external control voltage (GC) for the gain tuning.

Resistive degeneration was used with resistors $R_{E1} \sim 40\,\Omega$ to improve the linearity of this stage. A degeneration capacitor C_{deg} is included in parallel with resistors R_{E1} to introduce a high frequency zero responsible for the gain peaking in the mid-band frequency range, as explained in Chapter 2. C_{deg} is implemented as a varactor which allows for a $\pm$35% tuning range to accommodate possible process variations. The typical value is set in both cases to 220 fF. In the maximum gain setting the VGAs provide 9 dB DC gain. Emitter followers (Q11, Q12) are used for level shifting and to drive the large transistors of the output buffer.

The output buffer is a common-emitter differential pair with 50 Ω loads which provides broadband matching at the output and delivers an output voltage of $\sim$1 Vppd to the 25 Ω equivalent load. This headroom is responsible for the large power dissipated in the buffer alone, which amounts to 40% of the total. Degeneration resistors were used to improve the linearity. The buffer provides 0 dB gain; shunt peaking was used at the supply to boost the gain at the higher frequencies in order to equalize the VGA roll-off. At the output, inductors L5 where inserted in series and are used to improve the matching at the high frequencies, compensating the degradation caused by the capacitance of the output transistors (Q13-Q14) and the effect of the pad capacitances (25 fF).

The inductors at the input (L1, L2, L3) are used to extend the bandwidth by compensating the dominant pole produced by the input impedance of the first stage and the pad capacitance.

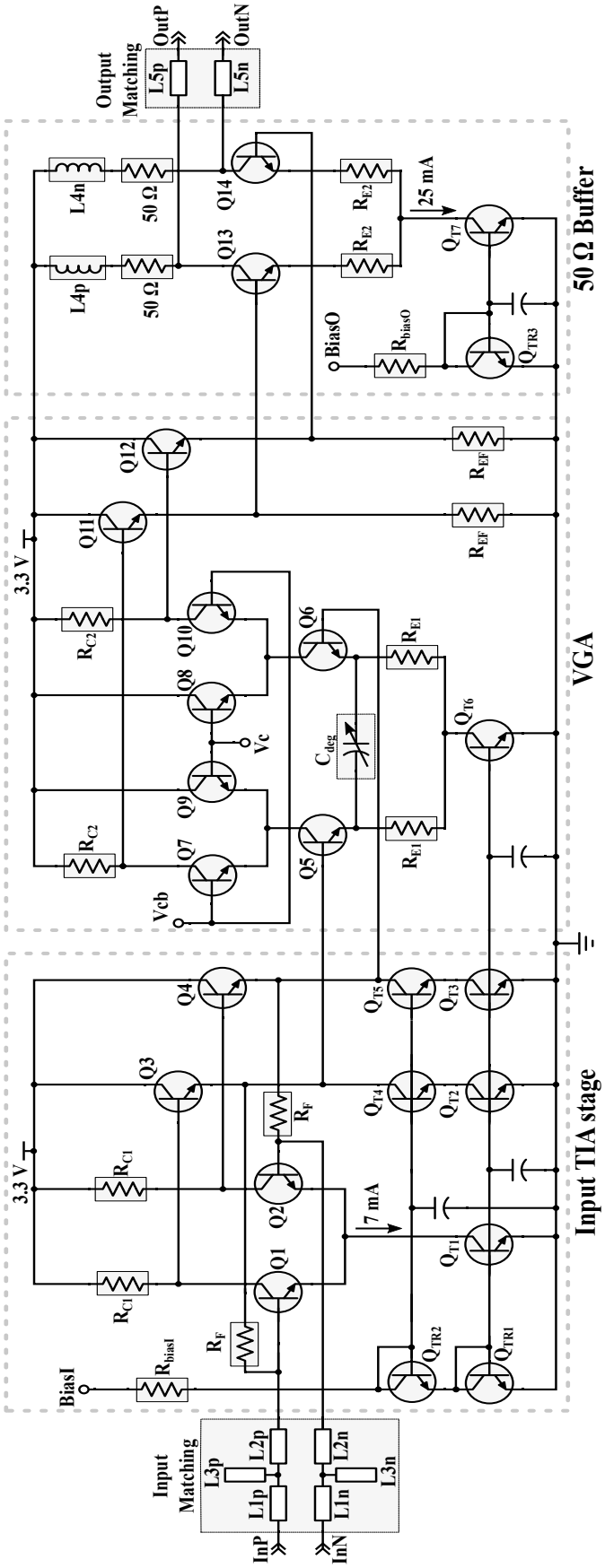


Figure 4.5: Schematic of the TIAs.

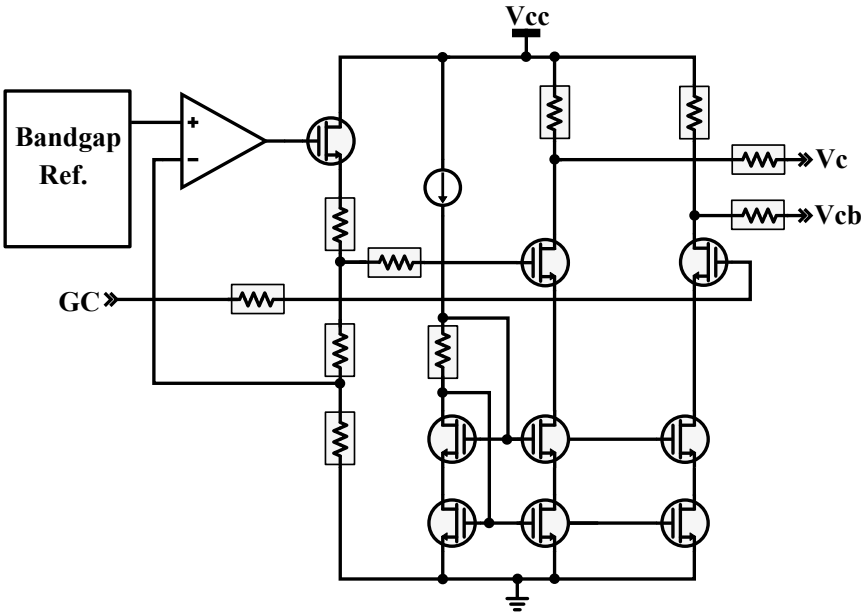
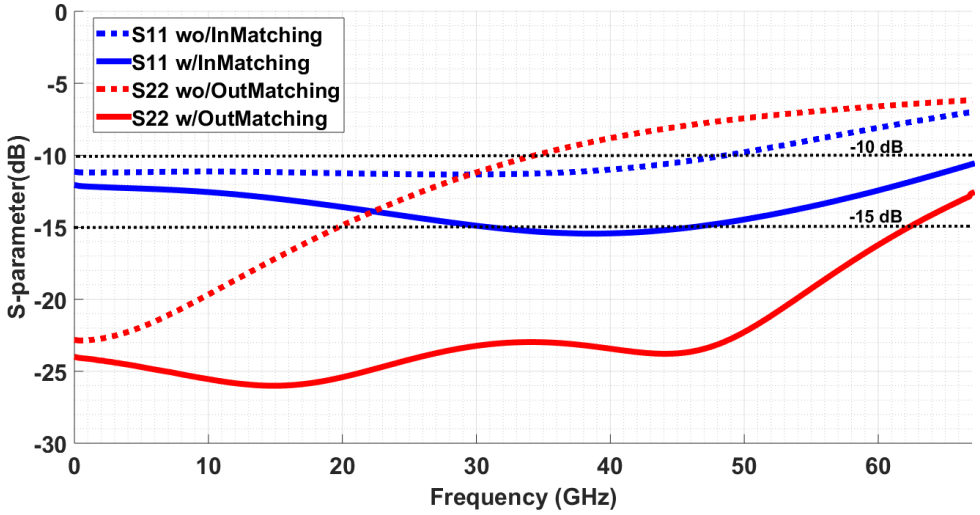


Figure 4.6: Gain control circuitry.

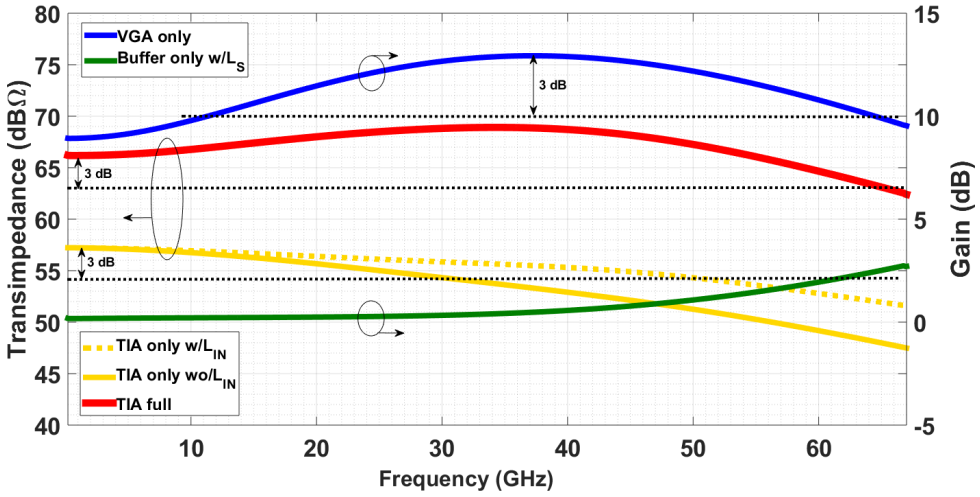
The value of these inductors was chosen so as to guarantee broadband 50 Ω matching mainly to allow characterization of the ICs in a conventional measurement environment. If used more aggressively, higher bandwidth extention ratio (BWER) could be achieved, but the S11 would be deteriorated, as will be demonstrated in Chapter 5.

In the 13S-TIA only one inductor was used (L2 = L3 = 0), while in the G2-TIA, which features a larger bandwidth, a broader frequency range was covered using a single-stub network. The peaking produced by all the reactive components was carefully controlled. Since the TIAs must be able to process broadband random data, peaking would translate into ringing in the eye diagram, largely deteriorating the performance, especially in the case of multilevel signals. In the presence of an external PD, the value of these inductors should be tuned to absorb the added parasitic capacitances of the PD and the pad. Moreover, all the inductors in the circuit have been designed as microstrip transmission lines with ground shield. The shield was implemented in the bottom-most metal layer so as to minimize the capacitance added to the signal trace. This reduces significantly the Q-factor, and hence the magnitude of the peaking, and moreover improves the modelling accuracy against variations in the characteristics of the substrate. It also provides layout flexibility in placing components next to each other since the coupling is reduced, and allows for an uninterrupted ground mesh covering the entire chip. The effect of the inductors at the input and output in the S11 and S22 of the G2-TIA can be seen in Figure 4.7a.

The noise-bandwidth optimization was an iterative process. The averaged input referred current noise density, bandwidth, input/output matching, gain ripple and group delay variation were monitored while minimizing the dominant noise contributors. The target low average input referred current noise density was obtained when the contributions from collector noise and thermal noise from the base resistance of the input transistors and the thermal noise from the feedback resistor become comparable and together amount to $\sim 45\%$ of the total noise. The contribution of each stage to the total bandwidth equalization can be observed in Figure 4.7b for the G2-TIA example. The input stage has a bandwidth that is 2.2 times less



(a)



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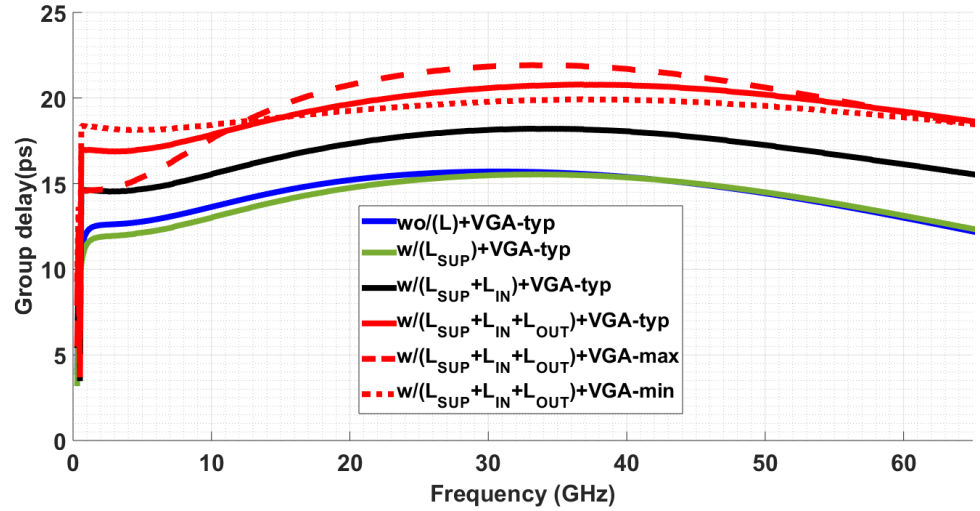


(c)

Figure 4.7: Post-layout simulation results from G2-TIA: (a) effect of input and output matching structures, (b) gain over frequency for different stages and (c) group delay with different reactive components added to the RF path.

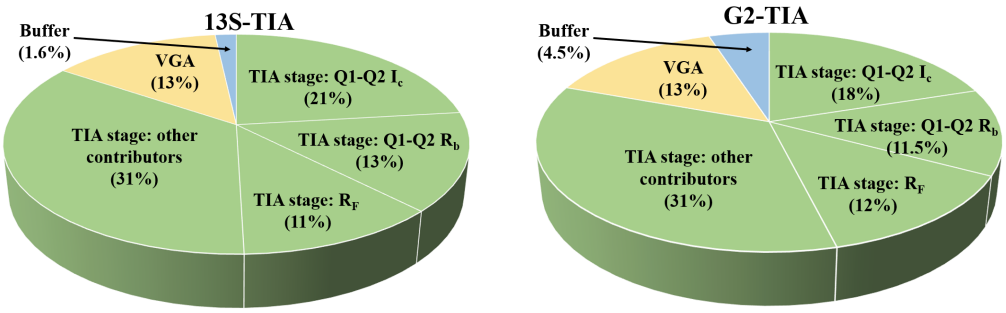


Figure 4.8: Distribution of the different noise contributions in the integrated input referred noise: (a) from the 13S-TIA and (b) from G2-TIA.

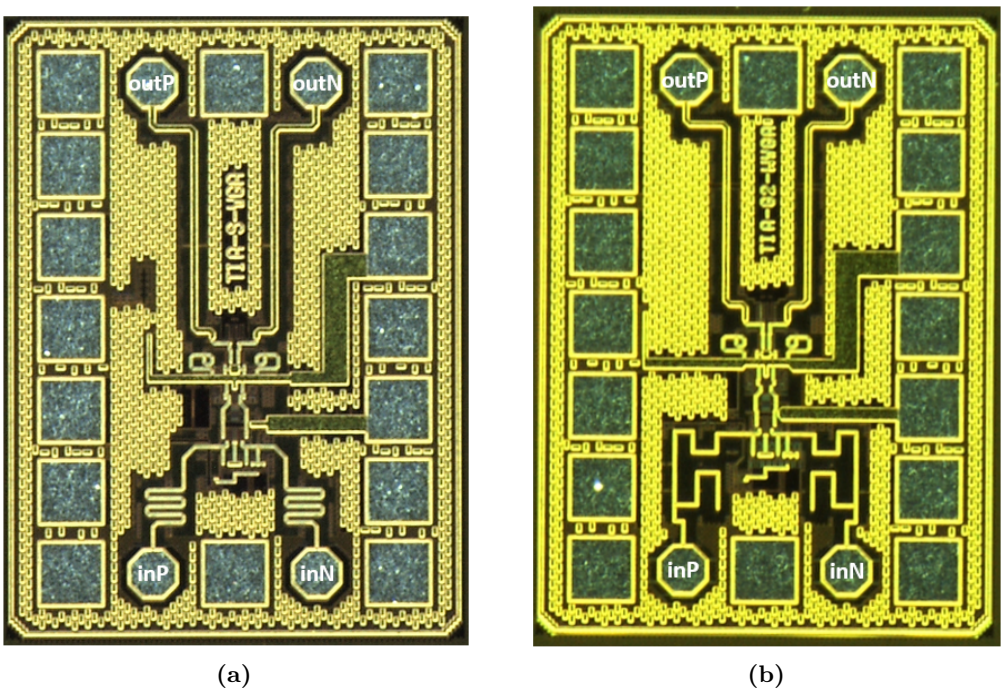
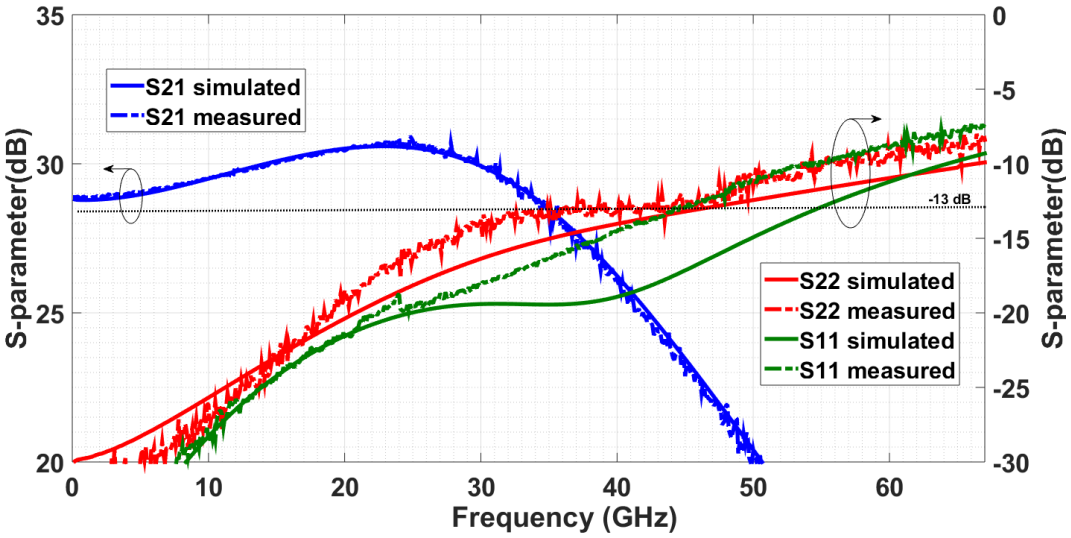


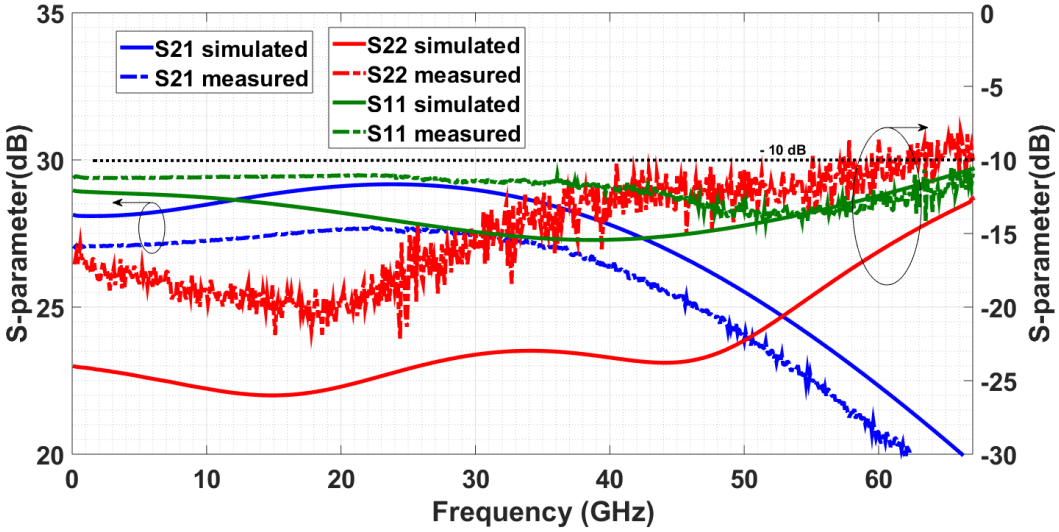
Figure 4.9: Chip microphotographs: (a) from 13S-TIA and (b) from G2-TIA.

than the total bandwidth finally achieved, which is recovered by the VGA in the mid-band and by the peaking effect of the input reactive structures and the output buffer in the high frequency range. In Figure 4.7c the group delay variation corresponding to a different number of components added to the RF path is depicted; it can be seen that the most critical variation arises from the peaking capacitor in the VGA; the designed inductors add a constant delay at all frequencies, without inducing delay variation.

Figure 4.8a and 4.8b depict the distribution of the top contributors in the integrated input-referred noise. The number of noise contributors considered accounts for $\sim 90\%$ of the total integrated input-referred noise. It can be seen how the input stage clearly dominates the total noise, despite the large peaking used in the VGA for equalization. The contribution from RF becomes now comparable to the second order terms from (4.11). The slice labelled as "TIA-stage: other contributors" in the pie chart represents the noise from other sources not modelled in (4.11), such as the base resistances of Q3-Q4, or the emitter-resistance noise from



(a)



(b)

Figure 4.10: Measured vs. simulated S-parameters: (a) of 13S-TIA and (b) of G2-TIA.

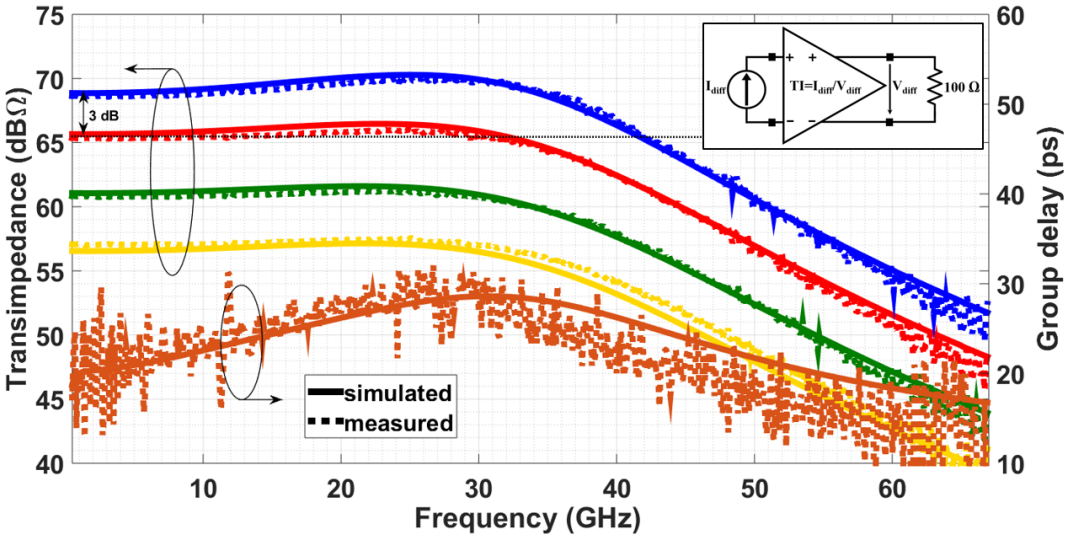
Q1-Q2, for example, each with very small contribution in the total noise, and that now, due to the reduction in the previously much larger sources, become more visible. Both ICs dissipate 150 mW power from a 3.3 V supply.

In Figures 4.9a and 4.8b the chip microphotographs of the 13S and G2 TIAs are presented, where all the described reactive structures can be clearly distinguished. Both chips have identical pad-frame and occupy 0.42 mm^2 area.

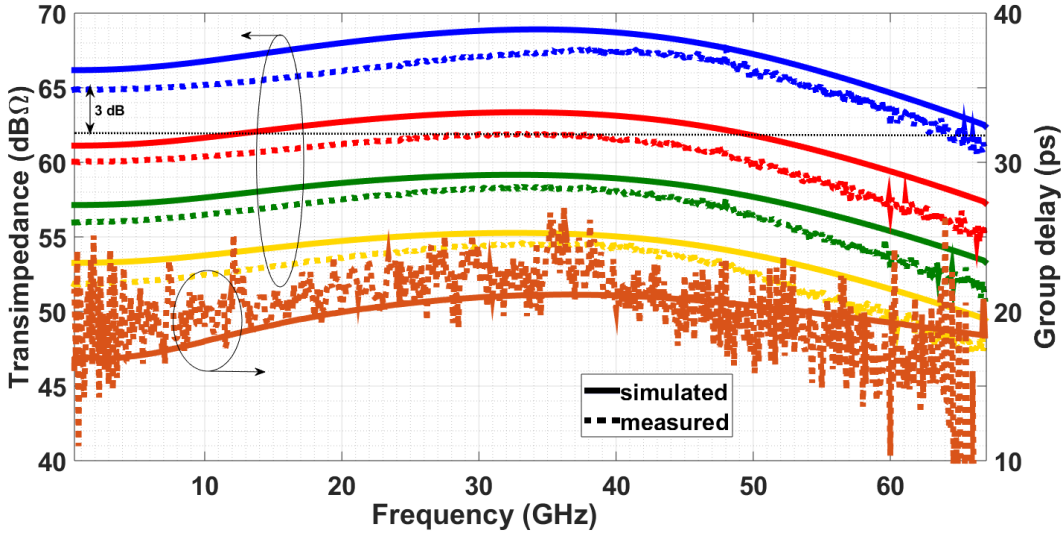
4.3.2 Functionality verification

The functionality of the TIAs was verified in the electrical domain. S-parameters, eye diagram, total harmonic distortion (THD) and noise measurements were carried out, via on-wafer probing, as described in the following.

S-parameters: In the frequency domain, 4-port, true-differential, S-parameters measurements up to 67 GHz were performed with -40 dBm of input power using a Rhode & Schwarz



(a)

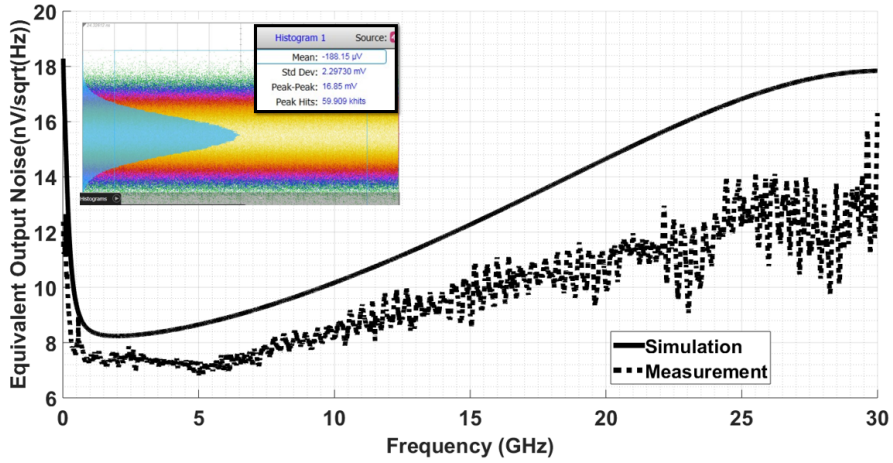


(b)

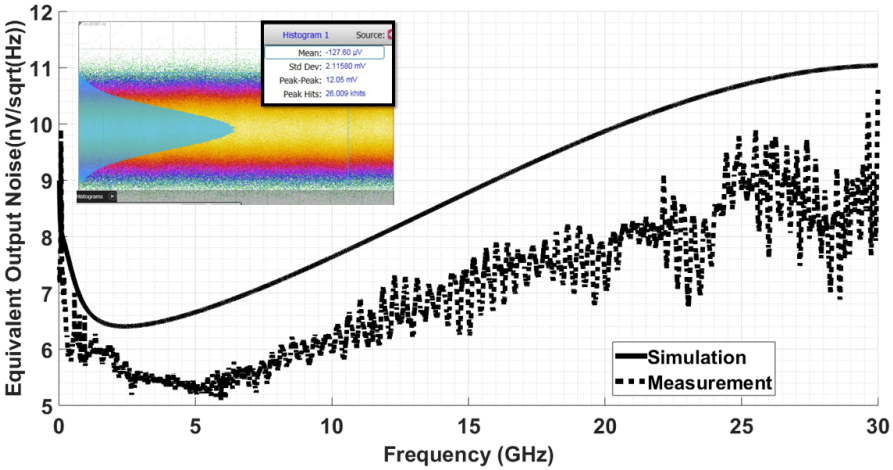
Figure 4.11: Measured vs. simulated transimpedance with gain control and group delay: (a) of 13S-TIA and (b) of G2-TIA.

ZVA67 VNA . The results, are presented in Figure 4.10a and 4.10b for the 13S and G2 TIAs, respectively. The 13S-TIA results are in excellent agreement with the simulation, and both input and output return loss are better than 13 dB up to 45 GHz. The G2-TIA S-parameters measurements are also in good agreement with the simulation, with a slight gain deviation of 1.2 dB already from DC due to process variations. $|S11|$ and $|S22|$ are better than 10 dB in the whole measurement span. The ripple observed in the measured results is due to the very small input powers used to avoid the saturation of the amplifiers.

The open-load transimpedance gain (TI) has been extracted from the S-parameters as $TI = V_{diff}/I_{diff}$, as indicated in the inset of Figure 4.12a [91, 92]. The results from both TIAs are depicted in Figures 4.11a and 4.11b, compared to the simulation results. The 13S-TIA showed 68.5 dBΩ of differential transimpedance, with 42 GHz bandwidth, while the G2-TIA features a smaller transimpedance gain of 65 dBΩ but 36% higher bandwidth, reaching the 3-dB point only at 66 GHz. The corresponding group delay from each TIA is presented in



(a)



(b)

Figure 4.12: Measured vs. simulated output-referred noise voltage spectral density: (a) from 13S-TIA and (b) from G2-TIA. Inset in figures displays integrated output noise from the histogram function of the oscilloscope.

the same figures, derived from the phase of the S21 forward transmission coefficient, with an aperture value of 5. It can be seen that in both cases measurements and simulation are in very good agreement, and both TIAs feature a low group delay variation of ±5 ps within the respective bandwidths.

Noise: To characterize the noise of the IC, two sets of measurements were performed. With the input of the TIA left open, using the histogram function of the Keysight 86100D oscilloscope, the integrated noise at one output of the TIA was measured, as shown in the insets of Figures 4.12a and 4.12b, with the other output terminated off-chip to 50 Ω. For a fair comparison, the bandwidth of the sampling head was set to 50 GHz for measuring the 13S-TIA, while for the G2-TIA it was set to the maximum of 70 GHz. Since the noise at the two outputs of a multistage differential amplifier is highly anticorrelated [50], the integrated input referred noise can be calculated as (4.13).

$$I_{n,in} = \frac{2\sqrt{(2.3\,mV)^2 - (0.7\,mV)^2}}{68.5\,dB\Omega} = 1.64\,\mu A_{rms} \tag{4.13}$$

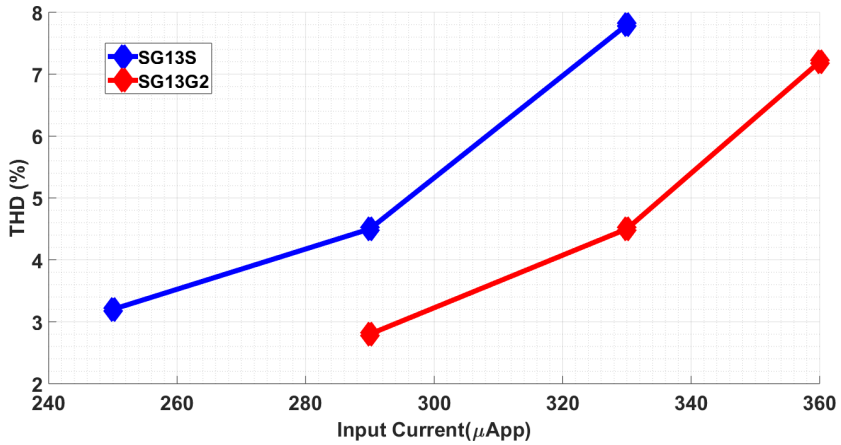


Figure 4.13: Measured THD @1 GHz for different input currents in the maximum gain condition.

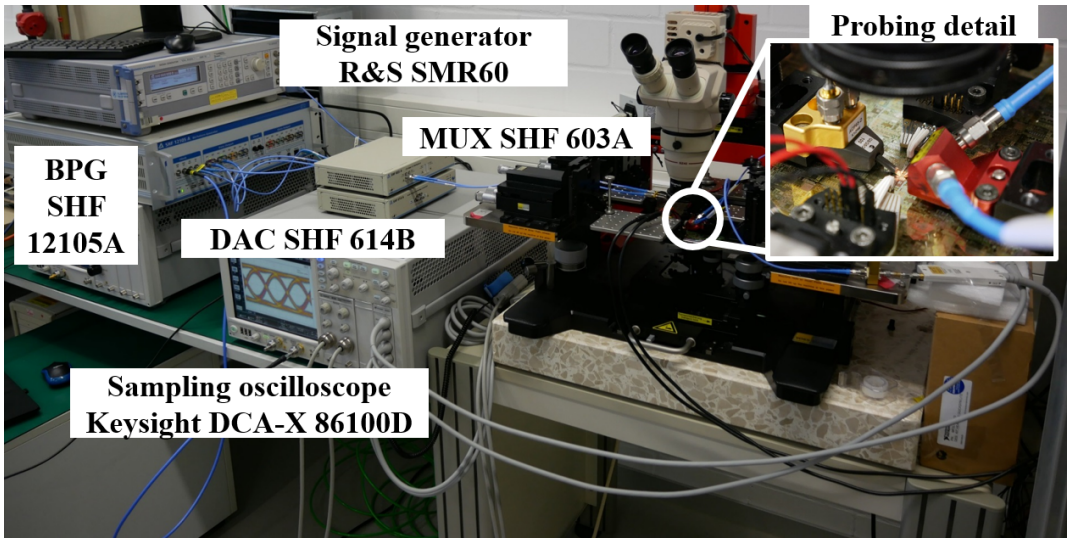


Figure 4.14: Time domain measurement setup using 67 GHz components (adaptors, cables, DC-blocks, attenuators).

Then the average input referred noise density is given by 4.14:

$$I_{n,avg} = \frac{I_{n,in}}{\sqrt{42\,GHz}} = 8\,pA/\sqrt{Hz} \tag{4.14}$$

The measured integrated output noise of the 13S-TIA was 2.3 mV_{rms}, which followed by the subtraction of the noise of the oscilloscope module itself (0.7 mV_{rms}) translates into a differential integrated input-referred current noise of 1.64 μA_{rms} and average input referred current noise density of 8 $pA/\sqrt{Hz}$. With similar procedure the G2-TIA featured a slightly lower averaged input-referred current noise density value of 7.6 $pA/\sqrt{Hz}$. In addition, the equivalent output-referred noise voltage spectral density up to 30 GHz was also measured as reported in Figure 4.12 compared to the simulation results. These values were obtained with a Rhode & Schwarz FSV30 spectrum analyzer after performing a noise calibration, with the receiver in open input. Simulation and measurement are in good agreement; the slight deviation between both curves is partially attributed to built-in error in the loss de-embedding procedure, from differences in the actual insertion loss of the components present in the setup and the values reported in the datasheets. The larger deviation in the G2-TIA is attributed to

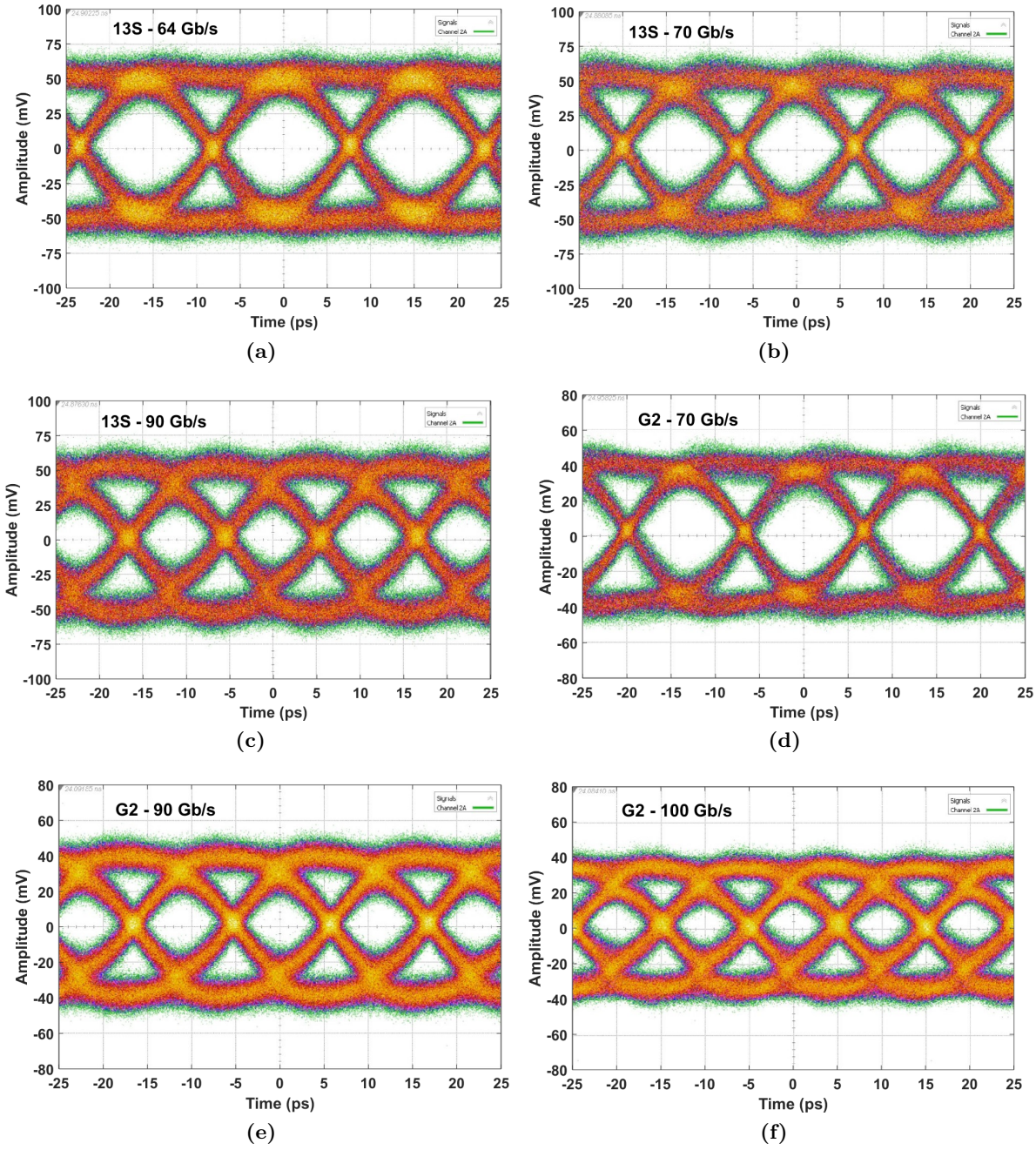


Figure 4.15: Time-domain single-ended measurement results @100 μApp NRZ PRBS31 for 13S-TIA: (a) at 64 Gb/s, (b) at 70 Gb/s and (c) at 90 Gb/s, and for G2-TIA (d) at 70 Gb/s, (e) at 90 Gb/s and (f) at 100 Gb/s.

the observed process variations. The measured results are also in line with the output-referred noise spectral density obtained from the oscilloscope measurements, i.e. 11 nV/$\sqrt{Hz}$ for the 13S-TIA and 7 nV/$\sqrt{Hz}$ for the G2-TIA.

Linearity: The linearity of the TIA was characterized by measuring THD at 1 GHz, considering 10 harmonics. For this setup, at the input a Rhode & Schwarz SMR60 signal generator was used and the signal was split and converted to differential using a Marki broadband balun up to 67 GHz. At the output, a similar balun combines the signal which is applied to a 50 GHz Agilent E4448A spectrum analyzer. After de-embedding the losses at

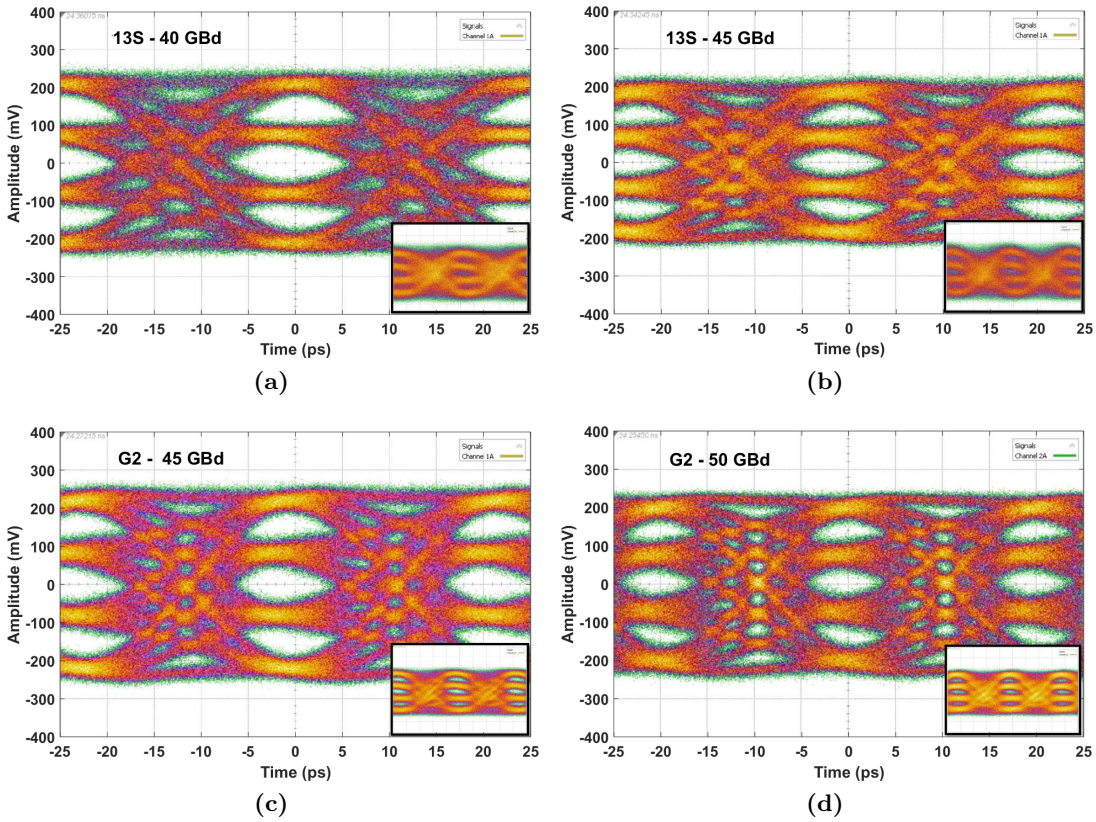


Figure 4.16: Time-domain single-ended measurement results of PAM-4 PRBS31 for 13S-TIA at (a) 40 GBd and (b) 45 GBd and for G2-TIA at (c) 45 GBd and (d) 50 GBd.

input and output, the THD values were obtained for different input currents as presented in Figure 4.13). The TIAs remain linear with THD below 5% in the maximum gain condition for input currents in the range of 300 μApp and 800 mVppd output voltage. Due to the lower transimpedance gain, the G2-TIA shows a larger linear range.

Eye diagram: In the time domain, a SHF 12105A bit pattern generator (BPG) together with a SHF 603A multiplexer (MUX) were used to produce the input signals that were applied to the TIAs, as seen in the setup photo depicted in Figure 4.14.

The MUX doubles the on-off-keying data-rate from two channels of the BPG. At the input, after the MUX output, a set of attenuators and a pair of DC-blocks were used, after which two phase-matched 0.5 m RF cables guide the differential signal to the input probe. At the output two similar cables are used between the output and the oscilloscope sampling heads. DC-blocks are also inserted at the output. All these cascaded components at input and output, with 67 GHz bandwidth each, significantly deteriorate the eye diagrams, since no pre-emphasis techniques were used to compensate for the setup losses. Despite these limitations, wide open single-ended eye diagrams measured with PRBS31 and input signals as low as 100 μApp are presented in Figures 4.15a to 4.15f, up to 90 Gb/s and 100 Gb/s data rate, for the 13S and G2 TIAs, respectively, in agreement with the small-signal bandwidths. Wide open eyes at these data-rates with such a small amplitude are also a sign of the good sensitivity of the TIAs.

PAM-4 measurements were as well conducted. Using the same setup described before, the MUX was replaced with a 6-bit DAC SHF 614B, using six channels of the BPG. The

Ref.	Year	Technology	f_T (GHz)	SE/S2D[1] /Diff.	Linear/ Limit.	PD (fF)	TI (dBΩ)	BW (GHz)	Noise ($pA/\sqrt{Hz}$)	Power (mW)
[79]	2014	65 nm CMOS	-	Diff.	Limit.	50	52	50	22.42	49.2
[78]	2014	65 nm CMOS	-	S2D	Limit.	160	83	18	15.3	93
[81]	2014	65 nm CMOS	-	SE	Limit.	N/A	76.8	21.4	17.8	137.5
[93]	2017	130 nm BiCMOS	300	Diff.	Linear	N/A	62	60	5.5	85
[94]	2016	250 nm CBiCMOS	110/95	Diff.	Linear	N/A	52.5	32	13.1	70
[95]	2013	130 nm BiCMOS	-	Diff.	Limit.	65	76.5	23	15.8	68
[96]	2014	65 nm CMOS	-	SE	Limit.	N/A	42	24	16	3
[97]	2015	55 nm CMOS	330	SE	Linear	N/A	-	92	17.7[2]	48
[91]	2016	130 nm BiCMOS	-	Diff.	Linear	N/A	77	34	20	285
[98]	2016	130 nm BiCMOS	-	S2D	Limit.	N/A	72	38.4	14.8	261
[99]	2014	130 nm BiCMOS	200	SE	Limit.	N/A	55	86	20.4	89
[47]	2010	250 nm BiCMOS	180	S2D	Limit.	>100	75.5	37.6	20	150
[100]	2012	250 nm BiCMOS	180	S2D	Limit.	100	70.8	20.5	18	57
[101]	2015	130 nm BiCMOS	300	SE	Limit.	N/A	65	53.8	12.34[3]	21.2
[102]	2004	InGaAs-InP	160	Diff.	Limit.	N/A	56	47	35	484
[103]	2013	InP	300	Diff.	Linear	N/A	55	107	44[3]	360
This-13S	**2017**	**130 nm BiCMOS**	**250**	**Diff.**	**Linear**	**N/A**	**68.5**	**42**	**8**	**150**
This-G2	**2017**	**130 nm BiCMOS**	**300**	**Diff.**	**Linear**	**N/A**	**65**	**66**	**7.6**	**150**

Table 4.3: Measured performance compared with prior published work.

single-ended output eye-diagrams with PAM-4 modulation are shown in Figures 4.16a to 4.16d, for input currents such that the TIAs deliver ∼800 mVppd at the output. It can be seen how open eye diagrams with equally spaced levels were obtained, at 45 GBd and 50 GBd for the 13S and G2 TIAs, respectively. The input eye-diagrams, with 310 μApp for the 13S TIA and 420 μApp for the G2-TIA are shown in the inset of the figures for comparison. Both TIAs have clear capability of delivering above 100 Gb/s data-rate in PAM-4 multilevel format.

Technology comparison: SG13S vs SG13G2: From (4.4), in a shunt-feedback TIA implementation, an increase of ∼30% in the transimpedance (TI) - bandwidth product, $TI{*}BW^2$, is expected in the G2-TIA from the f_T technology improvement considering also a 15% reduction in the input capacitance owing to the smaller G2 transistors. Such an improvement has indeed been observed in the fabricated chips, with the $TI * BW^2$ product experiencing a slightly higher 40% enhancement in the G2-TIA, due to the increased optimization flexibility that the design methodology offers, despite the lower transimpedance gain. The averaged input referred current noise density is, however, very similar in both TIAs. This comparable performance in terms of noise, is attributed to the design methodology. Both TIAs have been designed with a factor n∼2 from (4.11). The feedback resistor (R_F) is also similar in both TIAs and the input stage has been biased with low collector current density, rendering a similar noise contribution from the transistors in the low frequency range as well. However, the higher f_T/f_{max} reduces the contributions of the f^2 and f^4 components in (4.11) in the SG13G2 implementation, which translates into a slightly lower input referred noise current noise density when averaged over the bandwidth. The similar noise at the low frequencies can be seen from Figure 4.12a and 4.12b, where the difference in the output-referred voltage noise at 30 GHz corresponds to the lower 3.5 dBΩ transimpedance gain in the G2-TIA, rendering similar input-referred noise values.

4.4 Comparison with state-of-the-art

Table 4.3 shows a comparison of the designed amplifiers with state-of-the-art TIAs in different technologies. The proposed designs feature the lowest average input referred current noise density, with similar transimpedance gain and without significantly deteriorating bandwidth or power dissipation characteristics compared to other CMOS and InP solutions. This evidences the strength of the design methodology in surpassing the noise-bandwidth trade-off. Reference [93], which exhibits a lower input referred current noise density of 5.5 pA/$\sqrt{Hz}$, follows the same design technique here described. To achieve such a low value, the VGA was removed and strong input series peaking was utilized at the expense of deteriorating the input 50 Ω matching, making it only suitable for a high-impedance optical interface. This design will be explained in detail in the following Chapter 5. It is also worth noting that the performance of the here described TIAs in terms of bandwidth and sensitivity can only be maintained in a real application if the PD is closely integrated with the TIA and assumes a similar capacitance as the pads currently present in the layout (∼25 fF). This would be feasible, for example, with Ge PDs, which show bandwidths above 70 GHz with capacitances lower than 15 fF, much smaller than III-V discrete photodiodes at similar data-rates [104].

4.5 Summary

The design methodology and circuit implementation of TIAs featuring low averaged input referred current noise density without compromising the TIA bandwidth have been presented. Two analogous TIA designs implemented in the SG13S and SG13G2 processes have been described, and illustrate the technology role in the key performance metrics of the amplifiers. The 13S-TIA features 68.5 dBΩ differential transimpedance gain, 42 GHz 3-dB bandwidth and 8 pA/$\sqrt{Hz}$ averaged input referred current noise density while the G2-TIA provides 65 dBΩ differential transimpedance gain, 66 GHz 3-dB bandwidth and 7.6 pA/$\sqrt{Hz}$. Measured THD in both TIAs in maximum gain condition is better than 5% for 800 mVppd output swing and input currents in the order of 300 μApp. Both circuits dissipate 150 mW of power and are shown to operate at up to 100 Gb/s data rate with clean PRBS31 NRZ and PAM-4 eye diagrams. The TIAs exhibit the lowest averaged input referred current noise density shown to date at a bandwidth capable of supporting 100 Gb/s net data-rate, surpassing other silicon-based and InP implementations. Such performance has been enabled both by the low-noise technology and by the adopted design methodology, which allows to effectively overcome the classical noise-bandwidth trade-off.

5

Advanced Receiver Architectures for Power Efficient Modules

The low noise design methodology described in Chapter 4 is applied here to the development of three different receiver (Rx) concepts for power-efficient modules. This is a key parameter in cost reduction and heat dissipation management in the ever more aggressively miniaturized parts, needed to increase the port count in the data-center switch. The first design is a benchmarking two-stage transimpedance amplifier (TIA) implemented in the SG13G2 tehcnology, which demonstrates record 5.5 pA/$\sqrt{Hz}$ average input referred current noise density while sustaining 60 GHz bandwidth. Next, the G2-TIA from Chapter 4 is integrated together with a 2-bit analog-to-digital-converter (ADC) rendering an area and power-efficient solution for pulse-amplitude-modulation (PAM)-4 optical Rxs capable of demodulating up to 100 Gb/s signals. The last part of the chapter concludes the investigation on low-power implementations by exploring the benefits of high-speed pnp transistors in TIA design, in the SG25-H3P complementary process.

5.1 Introduction

Data-center infrastructures will need to handle Tb/s communication per carrier at every level of the architecture hierarchy [105]. As such, the current 100 Gb/s standard, is being surpassed by 400 Gb/s and 1 Tb/s systems [106, 107]. The analog bandwidth of optical and electrical components cannot support such data rates with conventional non-return-to-zero (NRZ) modulation and to resolve the required upgrade in throughput, higher-order modulation formats are being implemented. However, as seen in Chapter 1, while in telecom links digital coherent detection techniques are preferred for overcoming the imperfections of the longer fiber links, datacom communication resorts mainly to intensity-modulation/direct-detection (IM/DD) formats due to their relative system-level simplicity, potential for increased energy efficiency and lower area and cost requirements [108]. In particular, PAM-4 modulation format, which packs 2-b/symbol doubling the throughput for the same baud rate in comparison to NRZ formats, is expected to be the main workforce for 400 Gb/s systems, and the strong drive in standards towards adopting PAM-4 for 400 Gb/s Ethernet reflects this trend in industry [109, 110, 111]. The general idea is to achieve 100 Gb/s per wavelength, and use 4× parallel

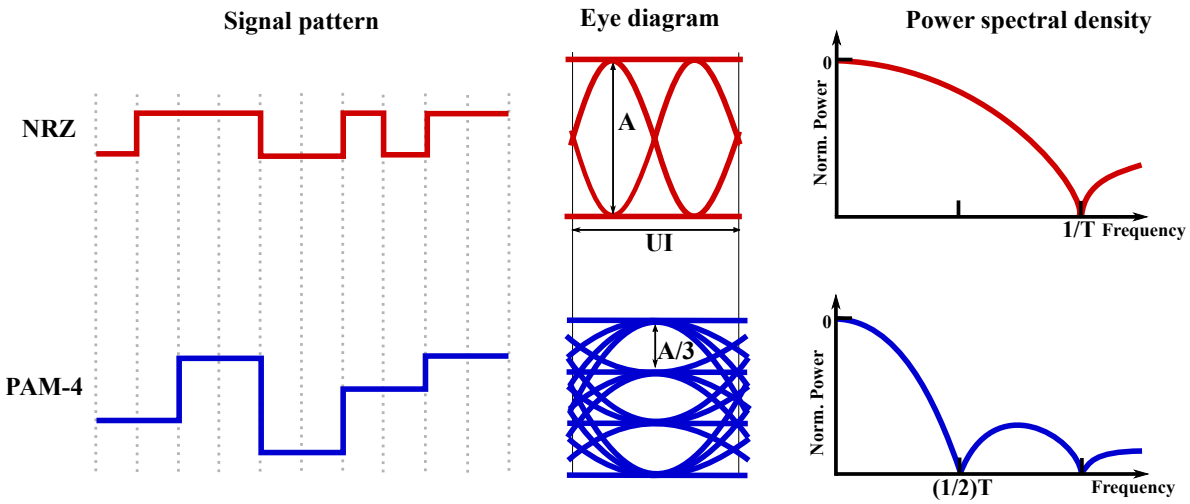


Figure 5.1: Schematic representation of NRZ vs. PAM-4 signal patterns, resulting eye diagrams and corresponding power spectral densities.

optics, in a grid of coarse wavelength division multiplexing (CWDM), to achieve 400 Gb/s [112]. Future Tb/s links may require higher-order PAM and finer WDM grid for higher spectral efficiency and transmission capacity.

The adoption of high-speed multilevel PAM-4 format comes at the expense of increased design challenges for the Rx. In Figure 5.1, both NRZ and PAM-4 formats are represented, and from the power spectral density it is seen that the Nyquist frequency is half for the PAM-4 format. Many benefits are associated with halving the Nyquist frequency: it allows double density of data, it provides higher resolution for the same oversampling rate, and by having the same noise spread over a wider frequency, the noise power in the bandwidth is reduced. However, although the Nyquist frequency is half, the eye width is, in reality, only between $\frac{1}{2}$UI and $\frac{1}{3}$UI, far less than 2 times of a NRZ eye width. This penalty is caused by the data-dependent jitter introduced in the PAM-4 format by the transitions between non-adjacent signal levels, thereby narrowing the eye [113]. In the vertical eye opening, there is a 9.6 dB degradation in the signal-to-noise-ratio (SNR) due to the swing shrinking (from 1 to 1/3 compared to NRZ, ($SNR = 10log10(\frac{1}{3}) \sim 9.6\,dB$) [114]. In practice further degradation will arise due to non-linearity, and up to 11 dB SNR penalty should be considered. All of this demands high-speed, linear TIA designs introducing low inter-symbol-interference (ISI) and with good noise management. Although forward error correction (FEC) can relax the final SNR requirement, the lowest noise at the Rx is always desirable, since it will improve the sensitivity and link budget. In this regard, in the first part of this chapter, the low noise performance of the SG13G2 technology is benchmarked by implementing a linear wideband TIA, featuring record 5.5 pA/$\sqrt{Hz}$ low noise performance at 60 GHz bandwidth, which furthermore evidences the technology suitablity for addressing future challenges of fiber-optics applications.

In addition to low noise performance, with the increase in port count within the data-center switch, another important aspect is to not overdesign the performance of the components in the Rx. More tailored designs, with contained power dissipation and reduced footprint and complexity are required in order to provide viable solutions. Moreover, although state-of-the-art ADCs fabricated in advanced Complementary Metal-Oxide-Semiconductor (CMOS) nodes have been shown to operate at very high speeds and resolutions [115, 116], the sub-1V supply

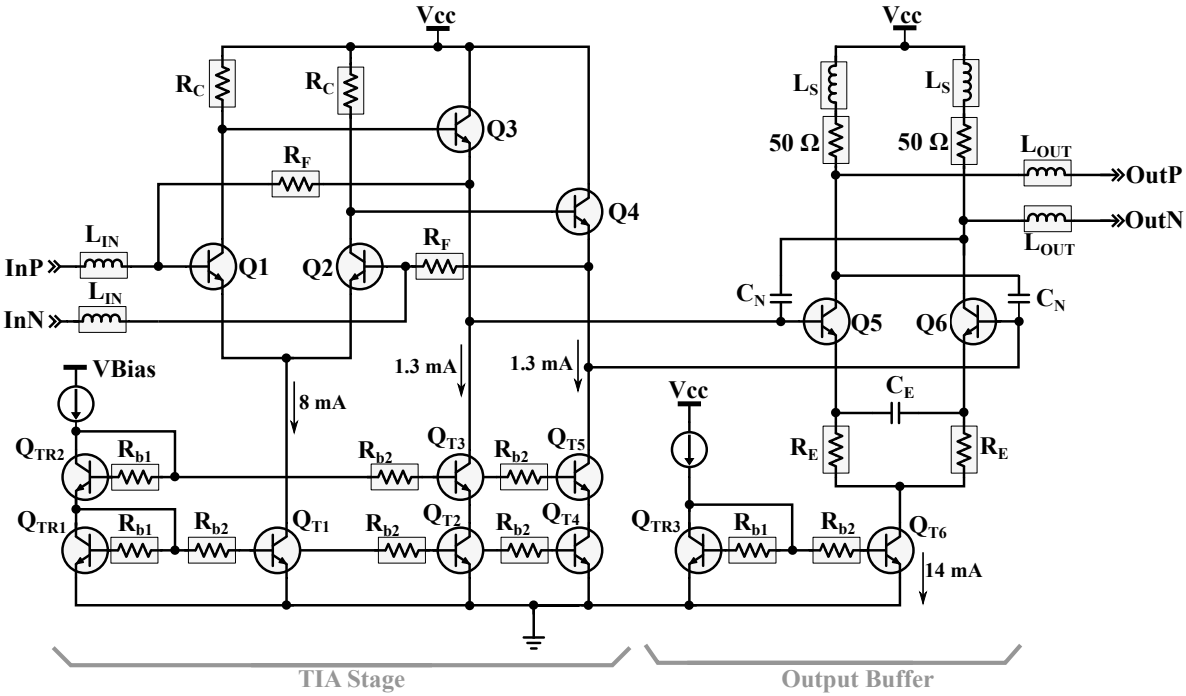


Figure 5.2: Schematic of the benchmarking TIA.

voltages imposed by the scaled CMOS technologies restrict the signal swing, such that threshold voltage mismatch, total harmonic distortion (THD), and noise requirements become more stringent and difficult to achieve. In light of these limitations, SiGe BiCMOS analog interface circuits still hold the potential to achieve overall better performance. The second part of this chapter presents a custom solution for PAM-4 optical Rxs that combines the high-performance G2-TIA from Chapter 4 together with an application-tailored a 2-bit ADC. This approach renders an area and power-efficient solution for PAM-4 optical Rxs capable of demodulating up to 100 Gb/s signals while dissipating only 650 mW of power.

As a final aspect, the last section of the chapter delves more into the issue of power optimization from a technology point of view. In this regard, the availability of a high-speed complementary bipolar technology with pnp and npn HBTs with matched performance may offer new opportunities [88, 117, 118] for power consumption optimization. Active pnp loads have been proven useful in replacing the load resistors of an amplifier gain stage, reducing the required voltage supply, with reported bandwidths of 2.5 GHz [117]. Likewise, pnp HBTs have been used to fabricate push-pull amplifiers [117] or switching amplifiers operated at a maximum speed of 7.5 Gb/s [118]. However, the potential of complementary bipolar technology remains unexplored in the upper GHz range. This path is investigated in the last section of this chapter with the implementation of a TIA in folded cascode architecture by making use of the complementary 0.25 μm SiGe:C BiCMOS technology of IHP, process H3P. This topology will be shown to feature increased bandwidth without power dissipation penalty while exhibiting good noise performance compared to other implementations in more advanced technologies.

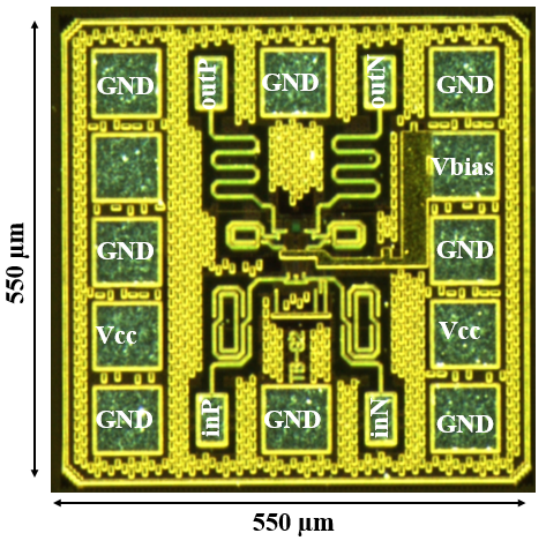


Figure 5.3: Chip microphotograph.

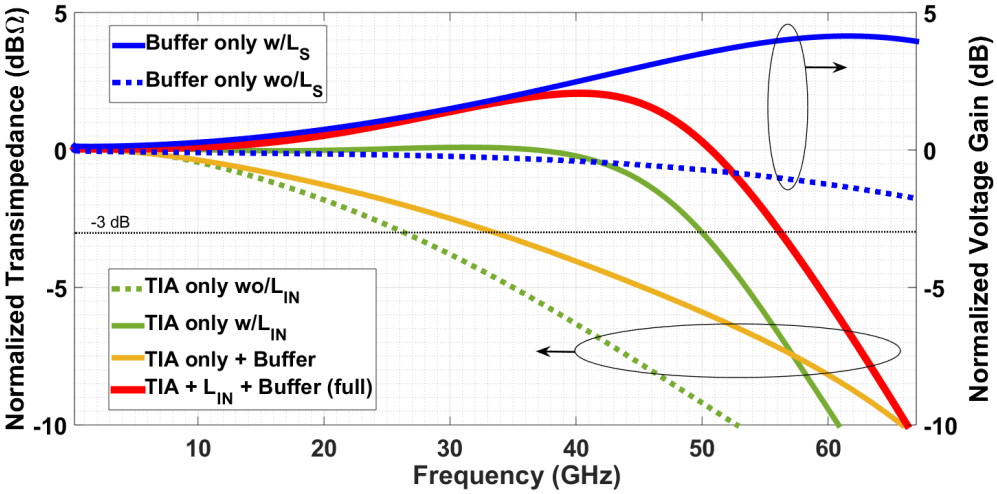


Figure 5.4: Post-layout simulation results of normalized gain over frequency for different stages.

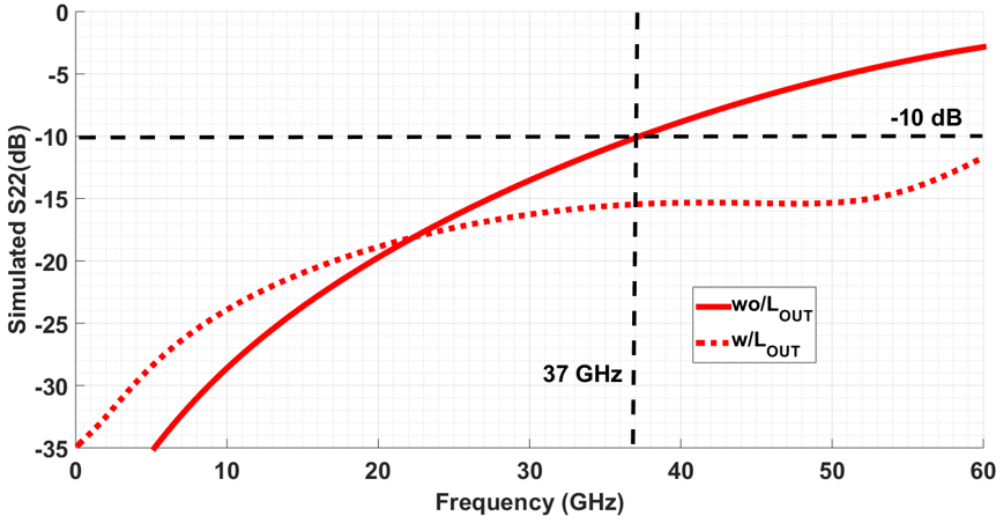


Figure 5.5: Effect of L_{OUT} on the output matching.

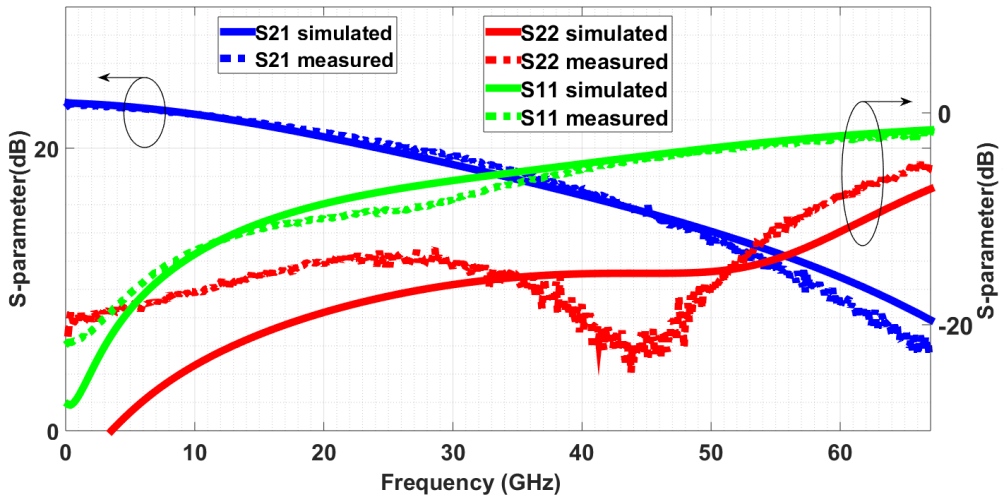


Figure 5.6: S-parameters measured vs. simulated.

5.2 Benchmarking TIA with less than 5.5 pA/$\sqrt{Hz}$

A TIA which benchmarks the low noise performance of the SG13G2 technology while featuring 60 GHz bandwidth has been implemented. In order to achieve lowest noise, a two-stage design which minimizes the number of transistors in the signal path was selected for this purpose, as described in the following.

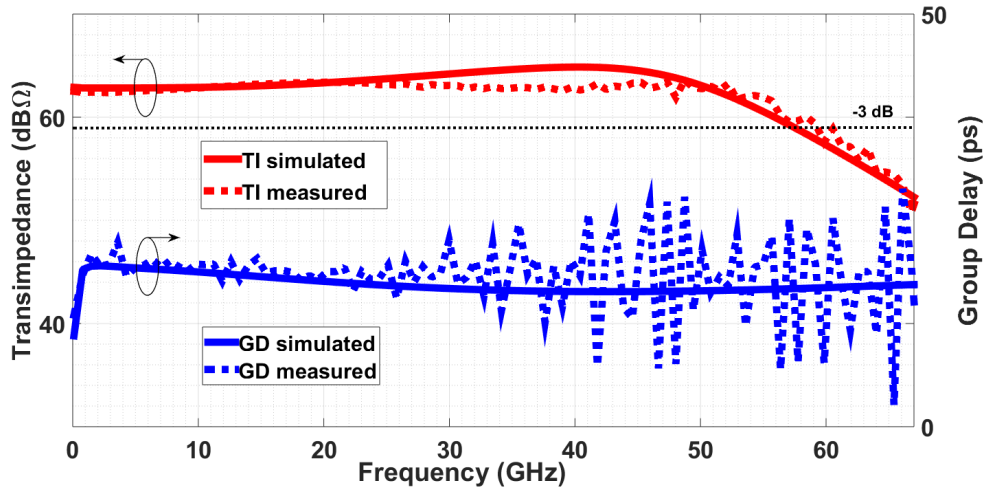


Figure 5.7: Transimpedance and group delay measured vs. simulated.

5.2.1 Circuit implementation

The schematic of this design is presented in Figure 5.2: the input TIA stage is followed directly by a 50 Ω buffer without post-amplification. The corresponding chip microphotograph is presented in Figure 5.3 occupying a pad-limited total area of 0.30 mm^2.

The input stage adopts the same common-emitter shunt-feedback topology as for the TIAs described in Chapter 4, but with $R_F \sim 600\,\Omega$, compared to the 480 Ω used in the G2-TIA from the previous chapter. The high gain of this stage effectively shields the noise from the following stage. The values of R_F and the sizing and biasing of Q1 and Q2 were selected for lowest

equivalent input-referred noise and high gain at the cost of achieving only a reduced bandwidth of 26 GHz for the TIA stage alone. The impairment in the bandwidth is here compensated by using large inductive peaking in series at the input, with $L_{IN} \sim 500\,pH$, which provides a 48% bandwidth increase. The value of this inductor was selected for a pad capacitance of 25 fF, and is optimized for low gain ripple and group delay variation, and sufficiently high self-resonance frequency (120 GHz). The output buffer also makes use of shunt inductive peaking with $L_S \sim 100$ pH and capacitive degeneration with $C_E \sim 180\,fF$, which contribute to a 17% bandwidth enhancement. Negative capacitance compensation with $C_N \sim 20\,fF$ was also employed, to reduce the effective capacitance seen at the output of the TIA stage. The peaking in the buffer was carefully controlled, to avoid deterioration in the output matching.

Both input inductance and output buffer combined have an equalizing effect, restoring the bandwidth from 26 GHz from the TIA stage alone to ~ 57 GHz for the full amplifier. The effect of each of these elements and the overall response are depicted in Figure 5.4, from the post-layout simulations. A third inductor $L_{OUT} \sim 200\,pH$ at the output compensates the effect of the capacitance of the output pad and the capacitances of the output transistors (Q5, Q6), improving the output matching in the high frequency range. The effect of L_{OUT} in the S22 is depicted in Figure 5.5. The total power dissipation of the IC is 85 mW from a 3.3 V supply, from which 46 mW are dissipated in the output buffer.

5.2.2 Functionality verification

The circuit was characterized in the electrical domain via on-wafer probing. The results from the 4-port S-Parameters measurements, obtained with a Rhode & Schwarz ZVA67 VNA, presented in Figure 5.6 show a good agreement between measurement and simulation. The output matching is better than -10 dB up to 55 GHz. The extracted transimpedance gain (TI) is depicted in Figure 5.7, compared to the simulation results. The TIA showed 62.5 dBΩ differential transimpedance, with 60 GHz bandwidth. In Figure 5.7 measured vs. simulated group delay are also presented. Although the measured results are very noisy, since they are derived from the sampled phase data, they are seen to follow closely the expected simulation result, which has a small variation of ±2 ps within the bandwidth.

Two sets of measurements were performed to characterize the noise of the IC. The single ended integrated noise at the output of the TIA was measured with the histogram function of the Keysight 86100D oscilloscope, as shown in the inset of Figure 5.8. The bandwidth of the remote sampling heads was set to 70 GHz. The measured integrated output noise of the TIA was $1.487\,mV_{rms}$, which after subtraction of the noise of the oscilloscope module itself, characterized with open input ($1.19\,mV_{rms}$), translates into a differential integrated input-referred current noise of 1.33 μArms and average input referred current noise density of $5.46\,pA/\sqrt{Hz}$. In addition, the equivalent output-referred noise voltage spectral density up to 30 GHz is reported in Figure 5.8 and compared to the simulation results. Simulation and measurement are in very good agreement, and are also in line with the output-referred noise spectral density obtained from the oscilloscope measurements as in equation 5.1.

$$V_{n,out} = \frac{\sqrt{(1.487mV)^2 - (1.19mV^2)}}{\sqrt{60GHz}} = 3.6nV/\sqrt{Hz} \tag{5.1}$$

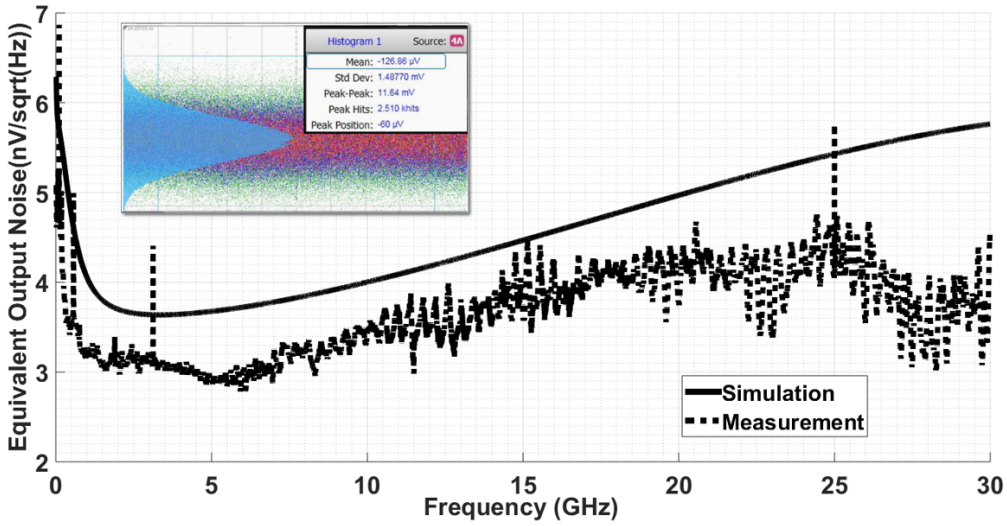


Figure 5.8: Measured output-referred noise voltage spectral density. Figure inset shows measured integrated output noise from the histogram function of the oscilloscope.

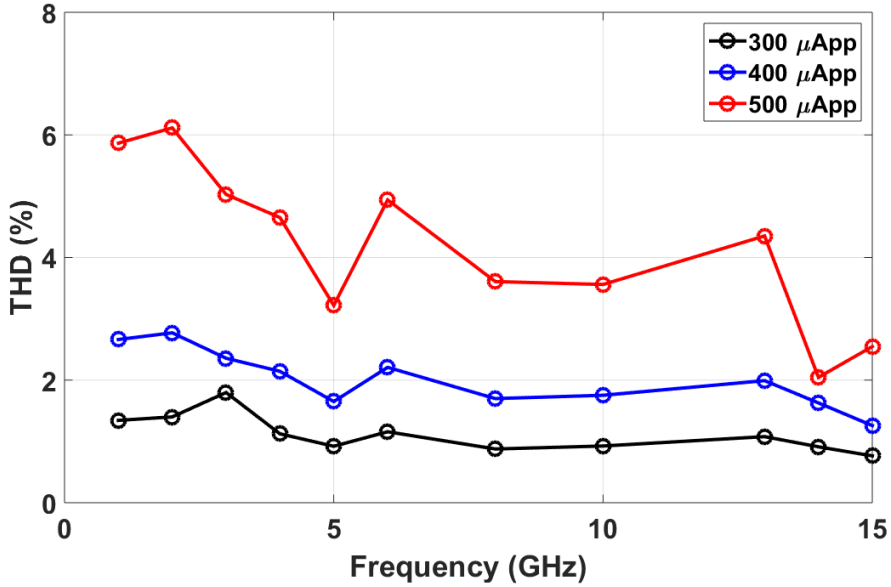


Figure 5.9: Measured THD over frequency for different input currents.

The linearity of the TIA was characterized by measuring differential THD up to 15 GHz, considering 10 harmonics (@1 GHz), as explained in Chapter 4. The THD values were obtained for different input currents as presented in Figure 5.9. The TIA remains linear with THD below 3% for input currents up to 400 μApp and 450 mVppd output voltage.

In the time domain, the TIA was measured operating with PRBS31 up to 56 Gb/s for different input currents as shown in Figure 5.10a to 5.10c. The single-ended eye opening amounts to 250 mVpp. Using a Keysight M8195A arbitrary waveform generator, PRBS7 PAM-4 eye diagrams up to 30 GBd were also obtained, as depicted in Figure 5.10d, showing minimal distortion when compared to the input signal represented in the inset, which furthermore demonstrates the linearity of the chip.

As seen in Chapter 4, Table 4.3, Ref. [93], the IC features the lowest average input referred current noise density compared to other state-of-the-art modules, with similar transimpedance gain and without significantly deteriorating bandwidth and power dissipation characteristics.

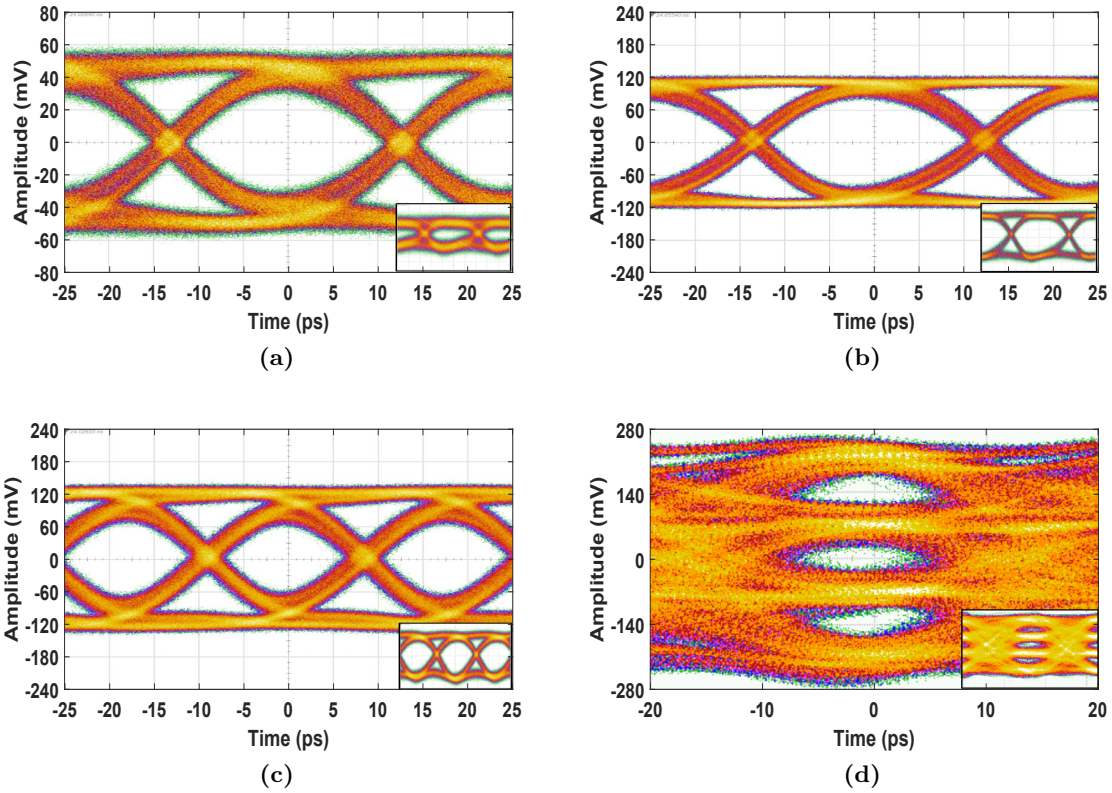


Figure 5.10: Time domain measurement results of PRBS31 NRZ eye diagrams from single-ended output at (a) 40 Gb/s @170 μApp, (b) 40 Gb/s @500 μApp, (c) 56 Gb/s @500 μApp and (d) of PRBS7 PAM-4 eye diagram from differential output at 30 GBd @400 μApp. Insets depict the corresponding input signal.

This design methodology is shown to effectively surpass the noise-bandwidth trade-off in the TIA front-end. However, the gain-linearity compromise remains, and a disadvangate of the proposed approach is the reduction in the TIA linear dynamic range. This is not too relevant for IM/DD formats such as PAM-4, but it is crucial for coherent applications making use of higher order modulation schemes. It can be resolved with a more efficient gain control technique in the first stage, similar to the typical approach used in burst-mode TIAs [119] which need to cover very large input dynamic ranges.

5.3 100 Gb/s PAM-4 Rx front-end

A custom solution for PAM-4 optical receivers that integrates the linear G2-TIA design described in Chapter 4, together with a 2-bit flash ADC is presented in this section. This Rx is designed to demodulate up to 100 Gb/s PAM-4 input signals while dissipating 650 mW of power. As seen in Table 5.1, although recent ADCs with very high sampling-rates and resolutions are available in the market, they dissipate very large power and consume significant area. Moreover, as discussed in Section 5.1, SiGe BiCMOS technologies are a good candidate to achieve overall better Rx performance than their CMOS counterparts, considering the design constraints imposed by the PAM-4 modulation format. In this way, the proposed approach combines the high performance of a SiGe BiCMOS front-end, together with an application-tailored ADC,

allowing for optimization in terms of power consumption and device miniaturization for the next-generation 400 Gb/s optical links.

Source/Foundry	Technology	Year	Rx-DSP integr.?	ADC Concept	Resolution (bits)	Max. Sampling Rate (GSamples/s)	Die Size (mm^2)	Power (W)
Agilent	180-nm CMOS	2003	No	PL	8	35	14×14	9
Nortel/ STM	130-nm SiGe BiCMOS	2006	No	FL	5	22	1.8×2.5	3
Alcatel-Lucent	180-nm SiGe BiCMOS	2008	No	FL	5	24	2.6×3.3	3.3
Nortel	90-nm CMOS	2008	Yes	TI-SAR	6	24	4×4	1.2
Micram	SiGe HBT/BiCMOS	2010	Yes	SR	6	34	1×2.6	2
Ciena	65-nm CMOS	2010	Yes	TI-SAR	6	40	4×4	1.5
Fujitsu	65-nm CMOS	2010	Yes	TI-SAR	8	56	–	2
Fujitsu	40-nm CMOS	2012	Yes	TI-SAR	8	65	–	1.2
Fujitsu	28-nm CMOS	2013	Yes	TI-SAR	8	92	–	<1

Table 5.1: Evolution of ADCs applied in optical transceivers or instrumentation [61].

5.3.1 Circuit implementation

The block diagram of the PAM-4 Rx is depicted in Figure 5.11. The TIA consisting of an input transimpedance stage and a VGA, converts the multilevel low input currents to the voltage domain, providing the full-scale amplitude to facilitate the ADC operation. Next, the 2-bit ADC demodulates the signal providing a binary output. Input and output inductors with value of 210 pH, are used for bandwidth enhancement and matching purposes. The inductors were carefully designed to limit frequency peaking and group delay variation, which are especially detrimental in multilevel modulation formats. The TIA design has been described in Chapter 4; the input matching structures have been adapted for this design, due to the differences in the padframe.

5.3.2 2-bit flash ADC

The implemented 2-bit ADC, as depicted in Figure 5.12, utilizes a fully differential flash architecture which is the preferred choice for high-speed, low-resolution ADCs, achieving the highest sampling rates [120]. The first stage, interfacing the analog and digital domains, is the quantizer block, which detects the 2^2-1 thresholds. It comprises a differential emitter follower stage followed by a resistor ladder which drives 3 comparator stages in parallel [121]. In the maximum gain condition, the full-scale single-ended voltage is 500 mVpp, and the quantization

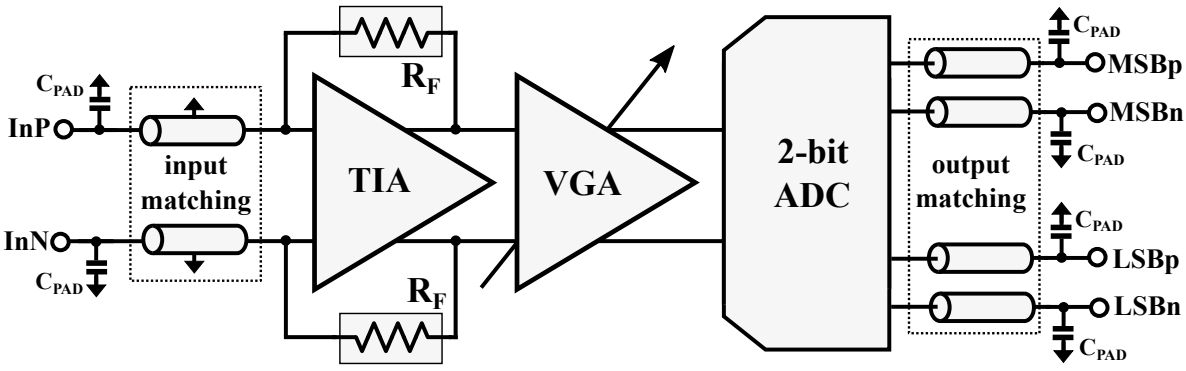


Figure 5.11: Block diagram of the PAM-4 receiver.

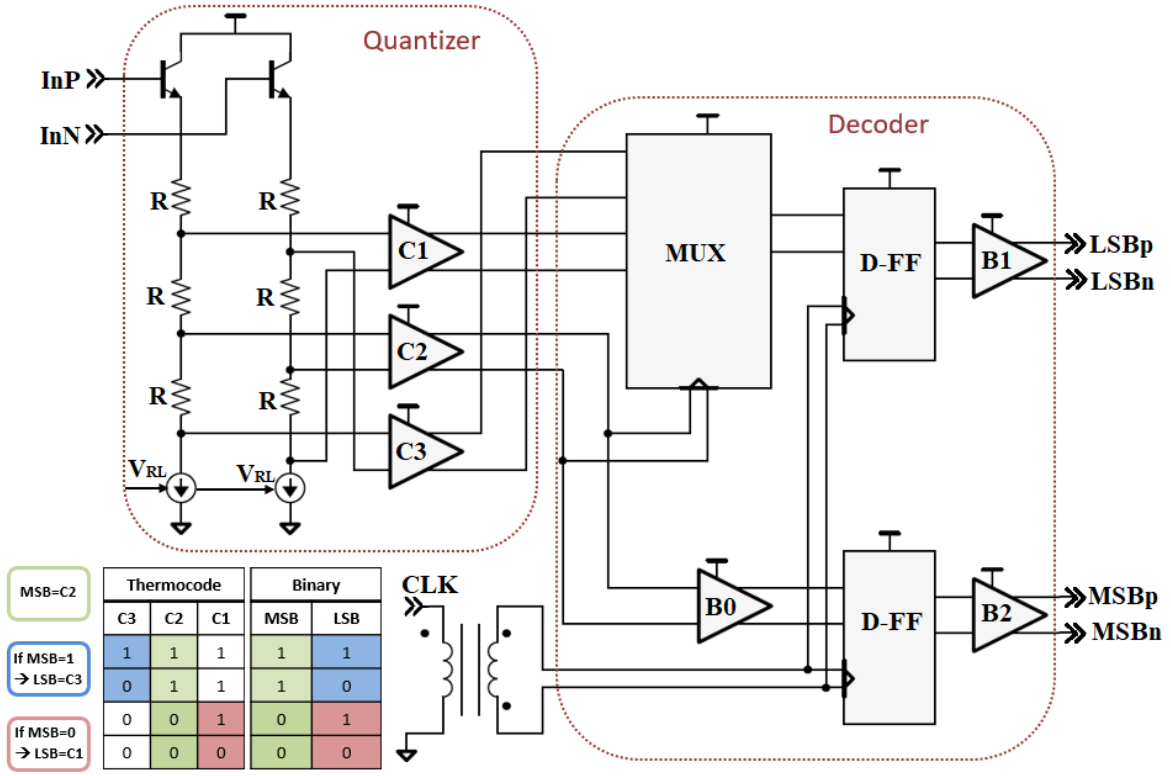


Figure 5.12: Schematic of the 2-bit flash ADC.

step is 110 mVpp, which can be controlled with the V_{RL} pin by changing the current circulating through the tap-resistors (R=18 Ω). In this quantizer, the differential output voltage ($v_{out,i}$) at each tap of the ladder represents already the result of the comparison of the input voltage (v_{in}) with the i^{th} reference level:

$$v_{out,i} = v_{in} - (i - 2^{b-1}V_{LSB}) \tag{5.2}$$

where $V_{LSB} = 2RI$ is the quantization step given by the tap resistance R and the tail current of the emitter follower. The comparators C1 to C3 are ordinary current switches (i.e. differential pairs without degeneration resistors operating in limiting mode). The second stage consists of a multiplexer-based decoder, which transforms the thermometer code output of the quantizer into binary according to the truth table depicted in Figure 5.12 [122]. The most significant bit (MSB), is given directly by the output of the C2 comparator and is used as select line for the 2:1 multiplexer. The schematic of the ECL multiplexer is depicted in Figure 5.13. The output is set by the emitter-coupled pair Q1-Q2 or Q3-Q4 depending on whether the tail current from Q_{T1} is steered by transistor Q1 or Q2, i.e. when the select signal is high or low [123]. The MUX stage is followed by emitter followers Q7-Q8 and output differential pair Q9-Q10 which operates in large signal mode as a limiter improving the pulse shape.

The MUX-based decoder is among the fastest circuits in a particular technology, since it employs current steering and does not contain any feedback loop requiring settling [90]. However, in this implementation, where no particular measures have been taken in order to avoid simultaneous transitions in both inputs of the MUX, or to guarantee alignment of the inputs with the select signal (selP, selN), the MUX outputs will experience glitches or

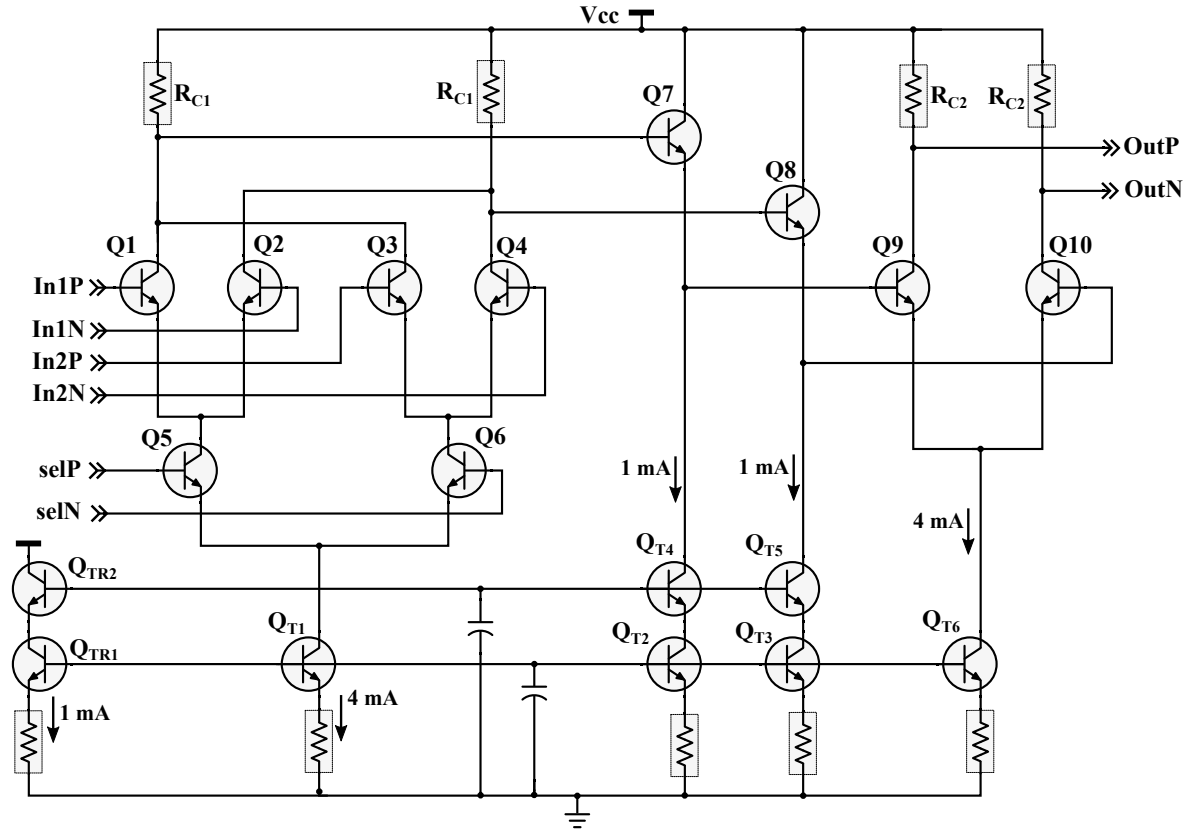


Figure 5.13: Schematic of the 2:1 MUX.

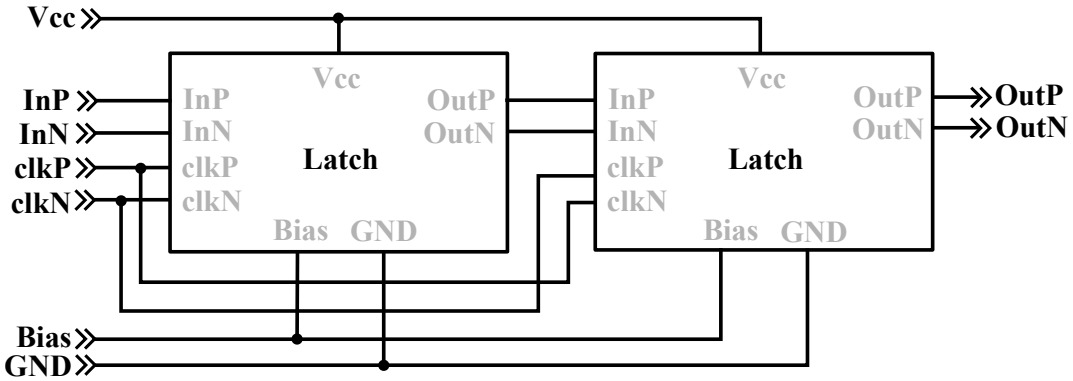


Figure 5.14: Schematic of the D-FF.

pulse-width distortion if such events occur. To prevent this issue and reduce the probability of a metastable digital output, the differential signals are re-timed by means of D-type flip-flops which hold the inputs at stable digital values between each sample. The flip-flops consist of two CML latches placed in a master-slave configuration, as seen in Figure 5.14, [124]. The MSB is delayed by buffer B0 which compensates the MUX delay in order to synchronize it with the least significant bit (LSB), which is required since both share the same clock.

The required differential clock signal is obtained from an available single-ended source and converted to differential by an on-chip Marchand balun. The balun can operate at clock frequencies from 20 to 60 GHz, which is the range where the phase difference between the outputs is close to 180°, the insertion loss varies from 4.7 to 6.3 dB and the input return loss is better than 7 dB based on simulation results. The clock signal is routed with 100 Ω differential transmission lines in a star manner, and is terminated with 2×50 Ω resistors in the center

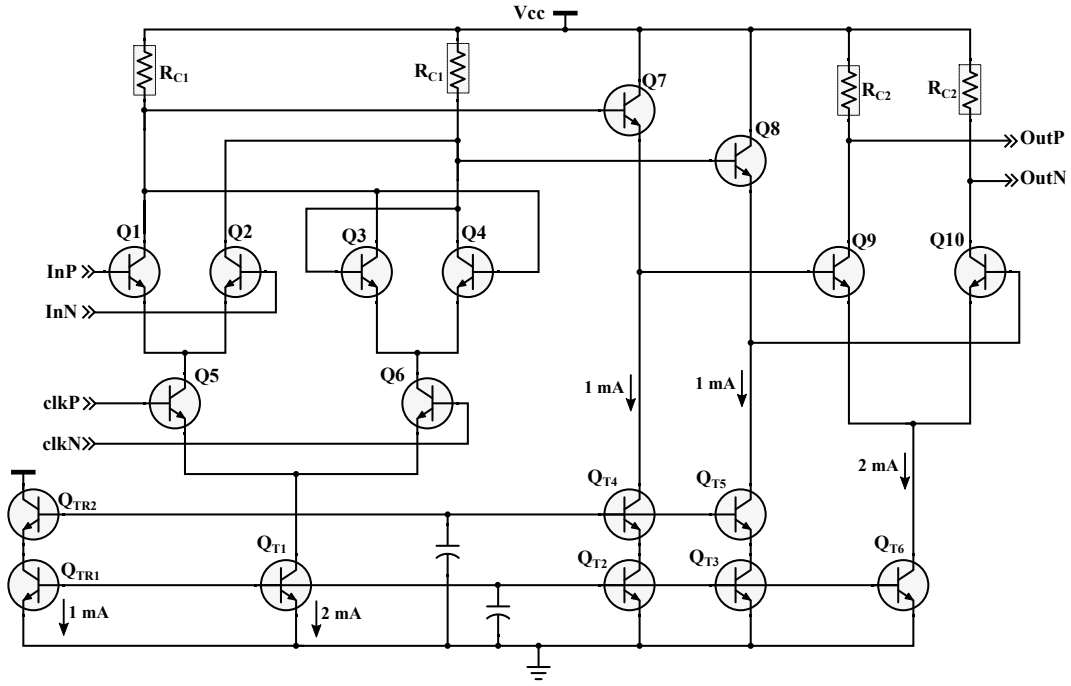


Figure 5.15: Schematic of the latch.

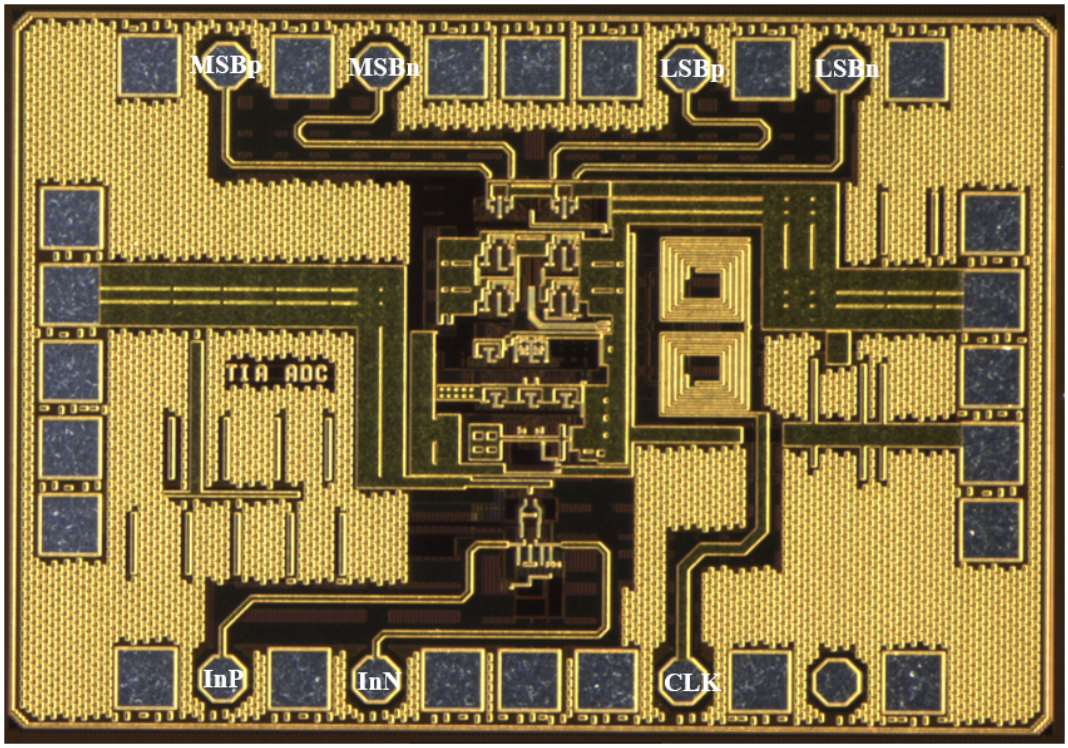


Figure 5.16: Chip microphotograph.

point of the D-FFs. The propagation delay in the clock signal path from this point of the transmission line termination and the four D-FFs has been also equalized.

The latches, as depicted in Figure 5.15 are implemented using a standard CML logic topology [123, 125]. As in the MUX design, the value of the collector resistor Rc1$\sim 100\Omega$ is chosen as a trade-off between the required switching speed and sufficient current value to achieve an amplitude of 250 mVpp [125]. They share the same reference "Bias" and are followed

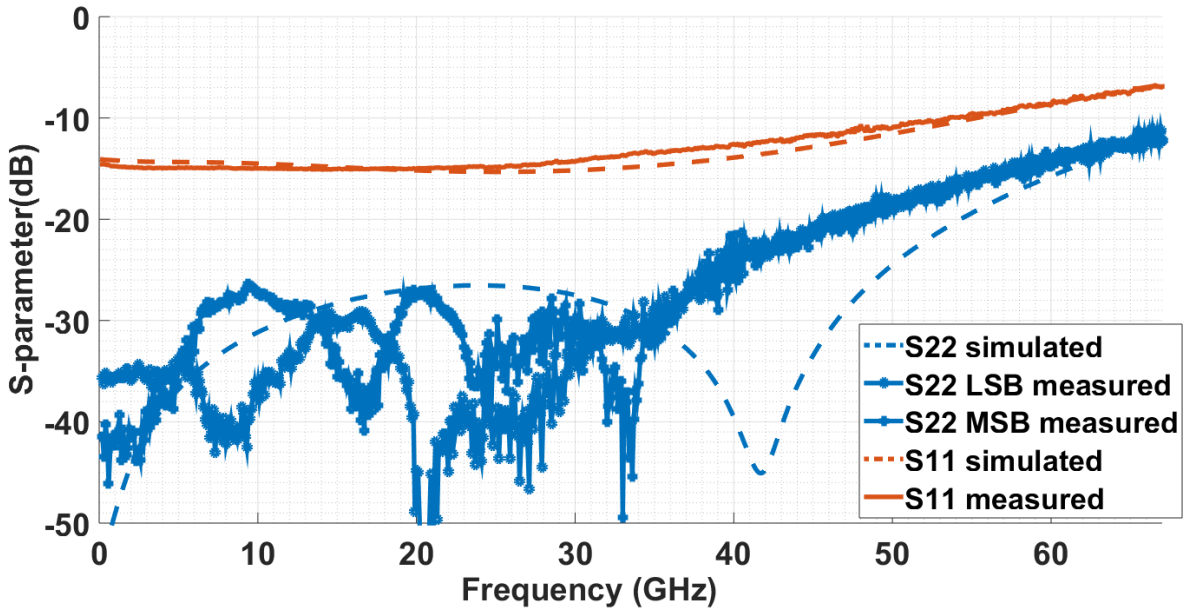


Figure 5.17: S-parameter measurement results vs. simulation from the PAM-4 receiver input and output matching.

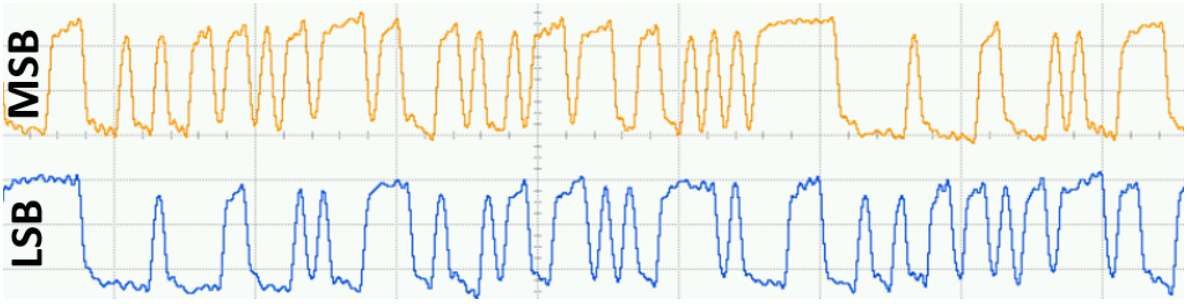


Figure 5.18: MSB and LSB PRBS7 decorrelated patterns at 24 GBd.

by common-collector stages Q7-Q8 and limiting amplifier Q9-Q10 to improve the pulse fidelity. All the transistors are biased with the same high current density of 1.8 mA per finger in order to increase the switching speed. The ADC dissipates 580 mW from the 3.6 V supply. The full chip, depicted in Figure 5.16, occupies an area of 1.25 mm^2.

5.3.3 Functionality verification

The receiver was characterized in the electrical domain via on-wafer probing. From the 4-port differential S-parameter measurements, performed up to 67 GHz using a Rhode & Schwarz ZVA67 VNA with -35 dBm input power, the output matching from both MSB and LSB outputs is presented in Figure 5.17. Both outputs feature S22 better than -20 dB up to 50 GHz.

In the time domain, two different sets of measurements were performed. The appropriate demodulation of PAM-4 input signals has been verified up to 24 GBd; higher baud rates could not be measured due to the degradation in the quality of the input signal. For this setup a Keysight M8195A AWG was used to generate the PAM-4 input and the clock while the outputs of both MSB and LSB were monitored in the Keysight DSA-Z 634A real time oscilloscope. Due to the long connections, the clock signal was amplified after the AWG with

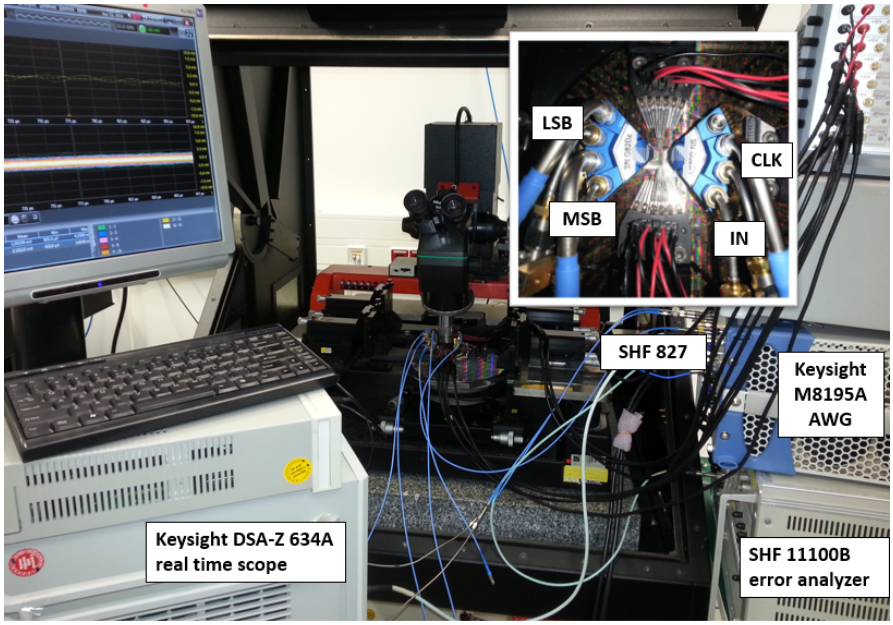


Figure 5.19: Time-domain measurement setup.

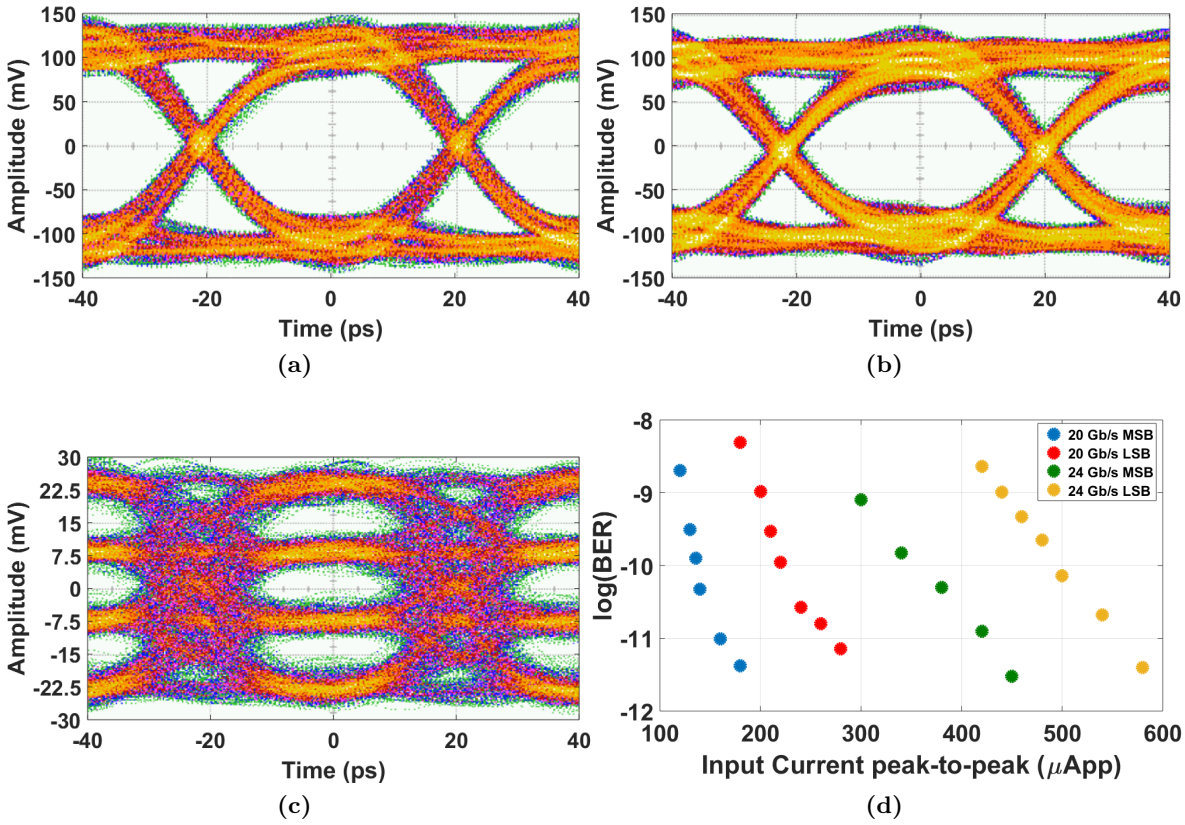


Figure 5.20: 24 GBd single-ended error-free recovered eye diagrams from (a) MSB and (b) LSB. (c) PAM-4 input signal. (d) BER measurements.

an SHF 827 ultra-broadband RF amplifier. The obtained patterns of MSB and LSB showing the appropriate conversion of the two decorrelated PRBS7 patterns are shown in Figure 5.18.

The recovered error-free eye diagrams at 24 GBd from both MSB and LSB are shown in Figures 5.20a and 5.20b, respectively. The corresponding PAM-4 input signal generated by the

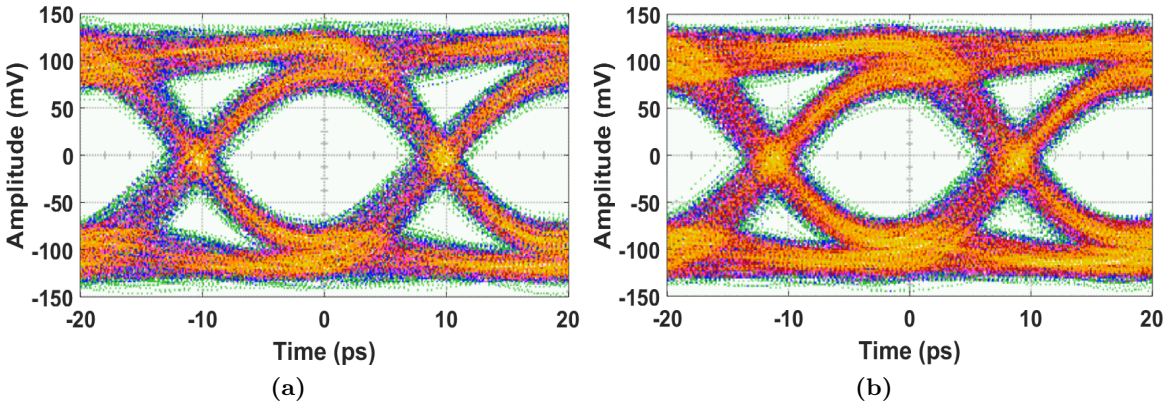


Figure 5.21: Single-ended NRZ eye diagrams at 50 Gb/s from (a) MSB and (b) LSB.

AWG is shown in Figure 5.20c, limited to its analog bandwidth of 17 GHz. The bit outputs were then fed to the SHF 11100B error analyzer and the BER at 20 GBd and 24 GBd was measured, with results presented in Figure 5.20d. BERs of $4 \cdot 10^{-12}/1 \cdot 10^{-13}$ for the LSB/MSB, respectively were obtained at 24 GBd when applying 580 μApp input signals. Since the ADC is asynchronous and the LSB is obtained from the MSB, the BERs of both bits are different. The MSB has better sensitivity than the LSB and a BER of $3 \cdot 10^{-12}$ for the MSB was measured with 450 μApp input signal.

Another set of measurements was performed to verify the high-speed operation of the IC in spite of the mentioned setup limitations. Using the SHF 12100B bit-pattern-generator, a NRZ signal at 50 Gb/s was generated. An Agilent E8257D signal generator produced the 50 GHz clock signal for the BPG. An external phase shifter (Spectrum Microwave OPS-002DC1312) was used to synchronize the clock. The corresponding single-ended eye diagrams at the outputs for both MSB and LSB are shown in Figures 5.21a and 5.21b, demonstrating the potential of the implemented receiver to operate at up to 100 Gb/s raw data rate. The "coarse" clock alignment available, limited these measurements to 50 Gb/s data rate; post-layout simulation shows correct operation at up to 56 GBd. Thus, the proposed approach, featuring state-of-the-art TIA and dedicated 2-bit ADC, allows for a more custom and optimized design in terms of power consumption and footprint, required for the next-generation 400 Gb/s optical links.

5.4 Folded cascode TIA using pnp HBTs

The availability of a high-speed complementary BiCMOS process, with pnp and npn transistors with matched performance is very desirable for RF applications. It offers the opportunity for designing push-pull circuits and active loads for analog applications which improve the power consumption of the circuits, as demonstrated in several examples at low frequencies [117, 118]. However, in most technologies, only the npn transistors are optimized and the pnp are usually "free", i.e. with no added process steps to guarantee similar high performance metrics as for the npn, and thus are not suitable to be used at high frequencies [126]. The IHP 0.25 μm SiGe:C BiCMOS technology, process H3P [43], as described in Chapter 2, offers high-speed matched pnp and npn transistors, and thus enables the use of designs based on complementary architectures.

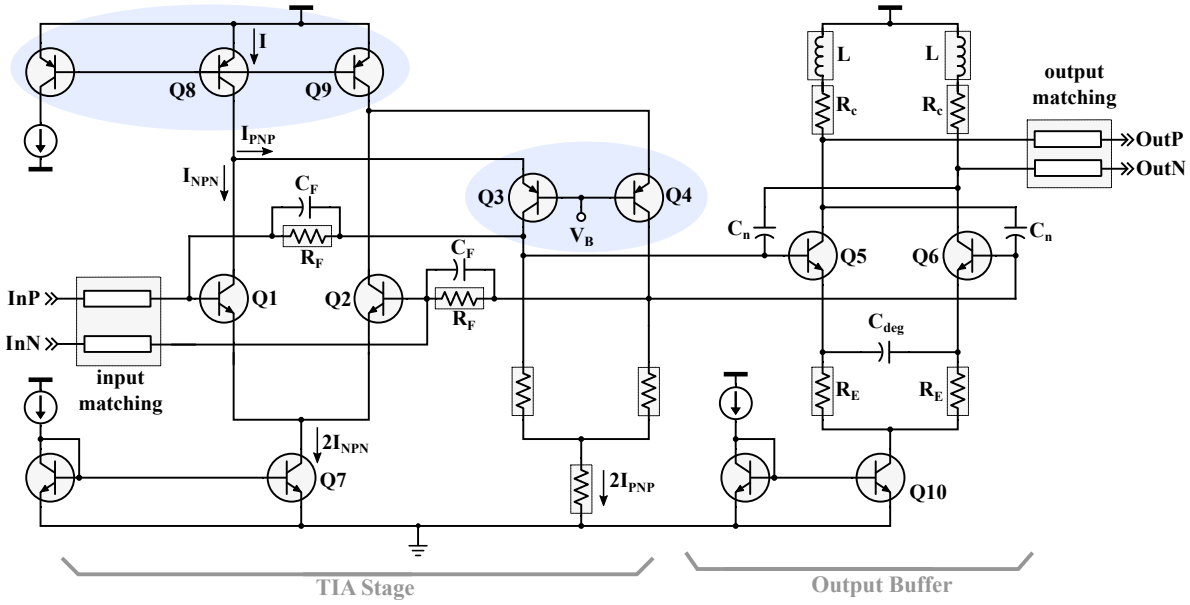


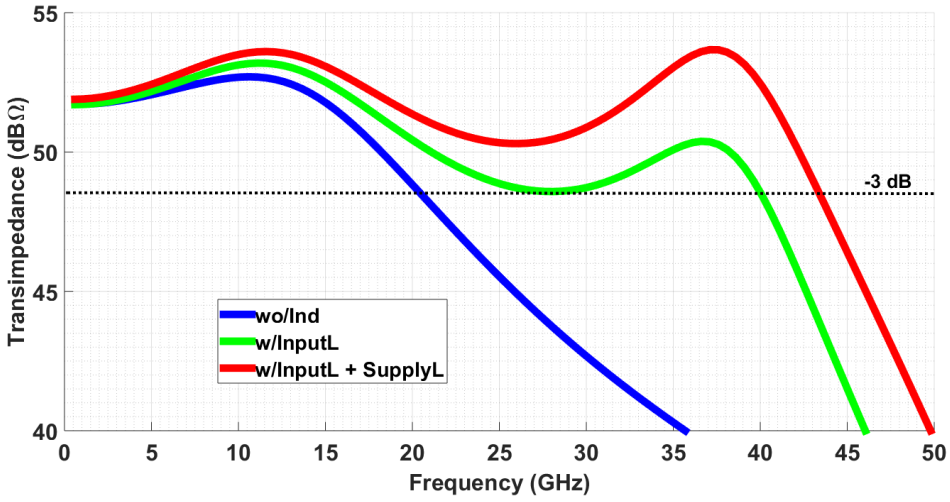
Figure 5.22: TIA stage and 50 Ω buffer schematic.

In particular, in the optical Rx such complementary architectures can prove very beneficial. Cascode configurations are well known for enhancing the TIA bandwidth [50], however at the expense of an increased voltage supply needed to accommodate the stacked transistors. Alternative implementations aiming at enhanced performance under low voltage supply resort to folded cascode and regulated cascode configurations commonly used for high-speed TIAs in CMOS technologies [127]. Given the availability of pnp transistors, this approach can be exploited as well in bipolar technologies, leading to potentially more power-efficient designs than npn-only implementations. In this section, a TIA implemented in a folded cascode architecture enabled by the use of the complementary technology of IHP is presented. The selected topology allows for low voltage operation coupled with enhanced bandwidth and sufficient low noise performance, emphasizing the optimization opportunities that a fast complementary technology has to offer in RF applications.

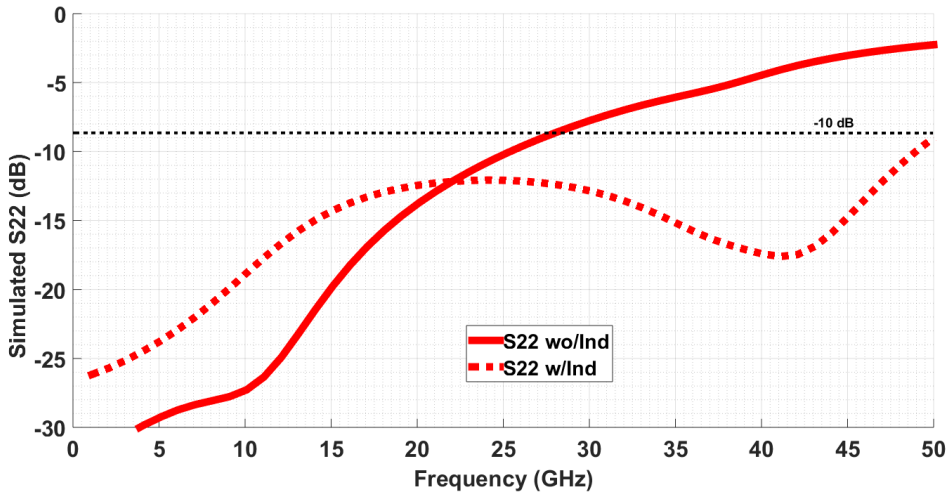
5.4.1 Circuit implementation

The schematic of the implemented TIA is depicted in Figure 5.22. It comprises two stages: an input TIA stage followed directly by a 50 Ω buffer, without post-amplification, similar to the TIA described in section 5.2. The total power dissipation of the TIA is 70 mW, from which 32 mW are dissipated in the output buffer.

Input and output inductors were used for matching purposes and bandwidth enhancement, with values of 490 pH and 300 pH respectively. The output inductor is implemented as a microstrip transmission line. The effect of these inductors can be seen in Figures 5.23a and 5.23b. In the TIA stage, the cascode configuration of the pairs Q1-Q3 and Q2-Q4 reduces the Miller effect due to the unitary gain of the common-emitter transistors (Q1, Q2), minimizing the input node capacitance. This allows for for bigger sizing of the input transistors (Q1, Q2) which translates into better noise performance. In Figure 5.24a and 5.24b a typical shunt-feedback TIA with common-emitter and npn-only cascode configuration, respectively, are depicted. It can be easily seen how through the implementation of the cascode devices



(a)



(b)

Figure 5.23: Effect of the inductors in (a) bandwidth and (b) output matching.

(Q3, Q4) with pnp HBTs, the supply needs not to be increased for this topology, as is the case in a conventional npn-only cascode implementation (Figure 5.24b). The current source (Q6, Q7) required for the biasing of the Q3- Q4 pair is also implemented via pnp transistors which consumes significantly lower voltage overhead than if large resistors were required. The feedback resistor, $R_F \sim 280\,\Omega$, is connected between the collector nodes of the common-emitter and common-base transistor pairs, with negligible dc current flow.

This value is carefully chosen as a trade-off between a high transimpedance gain, sufficient bandwidth and minimized noise contribution. This resistor is in parallel with a capacitor $C_F \sim 12\,\text{fF}$ which reduces the impedance of the feedback network at high frequencies, compensating the raising transimpedance gain in order to attain a flat frequency response. The implemented architecture circumvents the need for emitter follower, required in the shunt feedback topology with common emitter input stage for voltage level shifting (Figure 5.24a), leading to a power dissipation of the same magnitude with the benefit of increased bandwidth. On the other hand, when compared to npn-only cascode implementations, the complementary folded cascode features less power dissipation due to the lower supply voltage and lack of emitter followers, while exhibiting similar enhanced bandwidth.

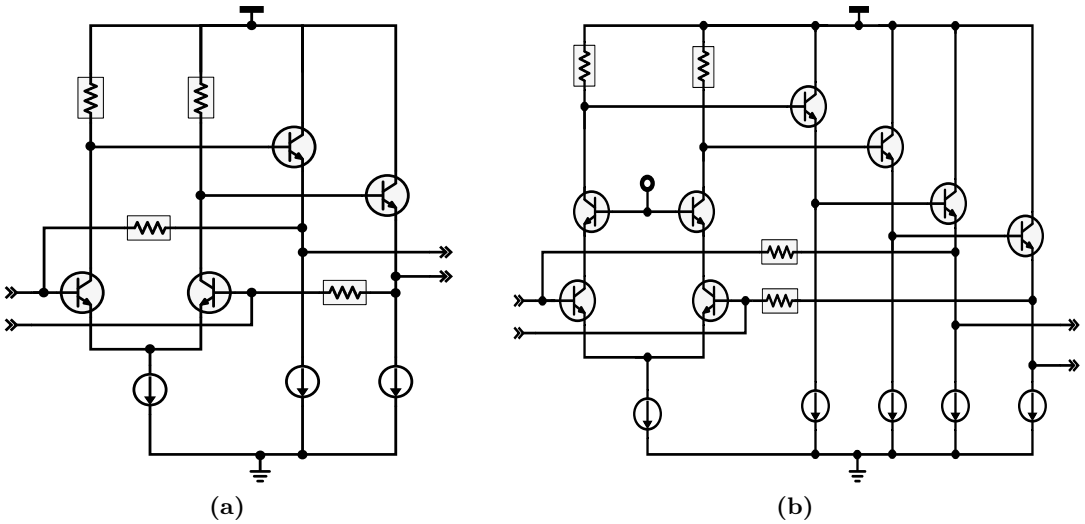


Figure 5.24: Schematic of (a) common-emitter shunt-feedback TIA and (b) npn-only cascode TIA.

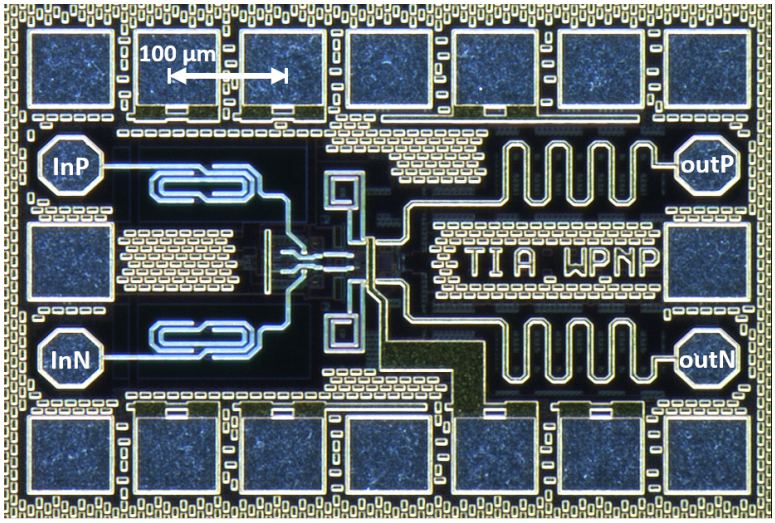


Figure 5.25: Chip microphotograph.

The output buffer is designed as a common emitter stage with resistive degeneration. Inductive peaking with L∼170 pH as well as capacitive degeneration with C_{deg}∼ 100 fF were implemented for bandwidth enhancement. Negative capacitance compensation was as well employed, with C_n∼25 fF, to reduce the effective capacitance seen at the Q3 and Q4 collector nodes, eliminating the need for intermediate buffering with the input TIA stage. The peaking in the output buffer was kept to a minimum, to avoid deterioration in the output matching. This stage provides 0 dB gain.

The chip microphotograph is presented in Figure 5.25 occupying a total area of 0.32 mm^2. The reactive (inductive) structures can be clearly distinguished.

5.4.2 Functionality verification

The circuit was characterized in the electrical domain via on-wafer probing. Four port S-parameter measurements were performed with -35 dBm of input power. The results, presented in Figure 5.26, show a good agreement between measurement and simulation.

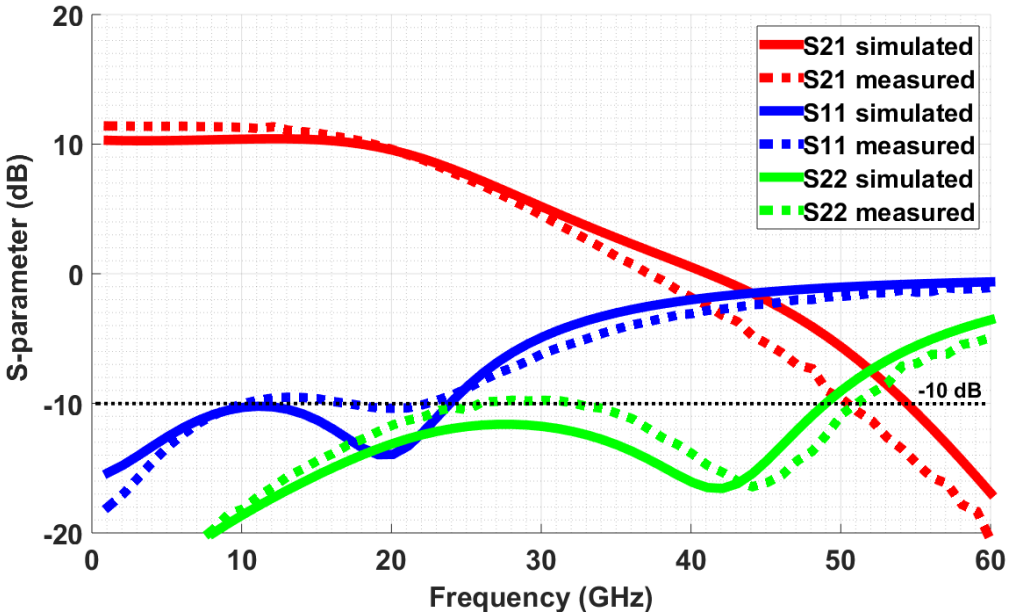


Figure 5.26: S-parameters measured vs. simulated.

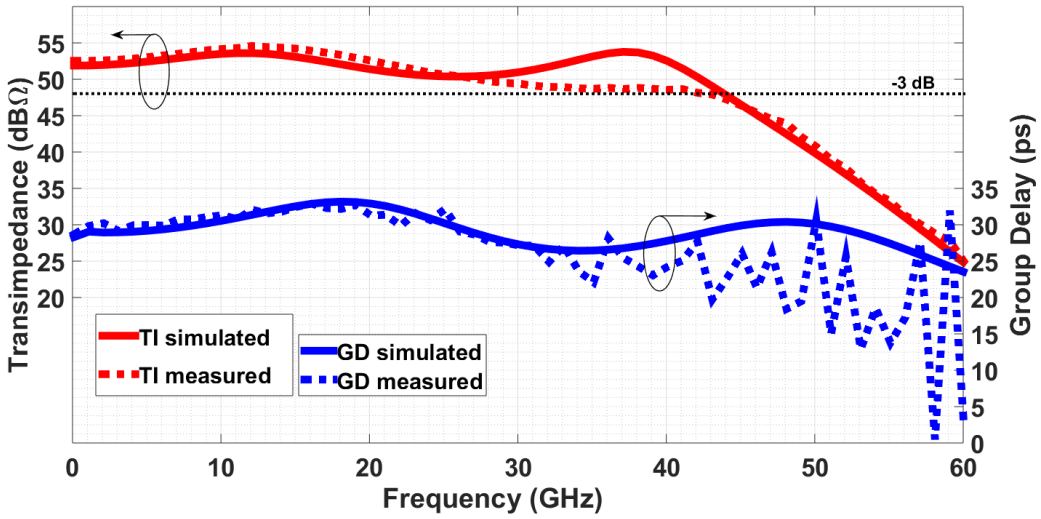
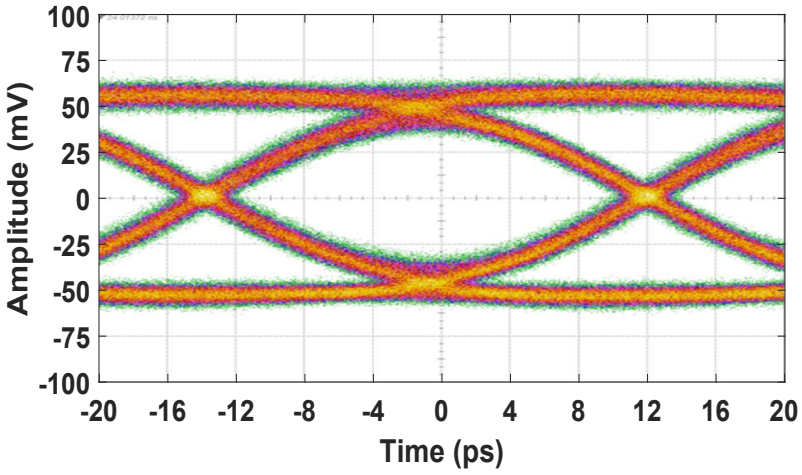


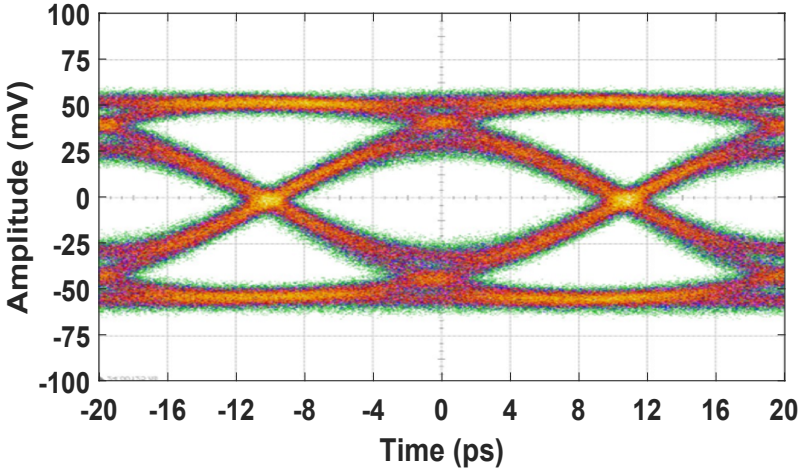
Figure 5.27: Transimpedance and group delay measured vs. simulated.

The output matching is better than -10 dB up to 50 GHz. The transimpedance gain (TI) was extracted from the S-paramteters and is depicted in Figure 5.27, compared to the simulation results. The TIA showed 52.5 dBΩ differential transimpedance, with 32 GHz bandwidth. After this point however, only a drop of less than 1 dB in the TI is observed up to 42 GHz. Moreover, phase linearity, represented by a flat group-delay response, has not been overlooked: in spite of the several reactive components and peaking schemes that were implemented, in Figure 5.27 measured vs. simulated group delay are presented, showing a small variation of ±5 ps within the bandwidth.

Time domain measurements were performed, operating with PRBS31 when applying 76 mVppd at the input, obtaining clear eye diagrams up to 50 Gb/s, as shown in Figures 5.28a and 5.28b. The single-ended eye opening amounts to 100 mV resulting in a 200 mV differential output swing. The single-ended noise of the TIA in open input was measured using the histogram function of the oscilloscope. The measured integrated output noise of the



(a)



(b)

Figure 5.28: Measured single-ended eye diagrams: (a) at 40Gb/s and (b) at 50 Gb/s.

TIA was 0.81 mVrms, which after subtraction of the noise of the oscilloscope module itself (0.64 mVrms) translates into a differential integrated input referred current noise of 2.35 μArms and average input referred current noise density of 13.1 pA/$\sqrt{Hz}$.

The proposed TIA implementation, based on a complementary bipolar design approach, offers very high speed without compromising on power dissipation while featuring sufficient low noise performance. In Chapter 4, Table 4.3, this IC was included as reference [94], and it can be seen how the design outperforms several other implementations in faster technologies in terms of data rate and low noise behavior, while featuring lower power dissipation. Moreover, this is the first time pnp transistors are used at such speed.

5.5 Summary

Based on the TIA low noise design approach described in Chapter 4, here three different Rx concepts aiming at the implementation of power efficient modules for the next generation 400 Gb/s datacom links have been described. The first one is a wideband linear TIA, implemented in the SG13G2 technology, which exhibits a differential transimpedance gain of

62.5 dBΩ and a 3 dB bandwidth of 60 GHz, with a measured differential average input referred current noise density of 5.46 pA/$\sqrt{Hz}$ and 85 mW power dissipation. This amplifier exhibits state-of-the-art low noise performance among >50 Gb/s-class silicon-based TIAs, which is a benchmark enabled by the fast technology node used, with f_T=300 GHz, as well as the described circuit-level techniques. Next, a PAM-4 receiver comprising the linear G2-TIA stage described in Chapter 4, together with a custom 2-bit flash ADC, was presented. This Rx, designed to operate at up to 100 Gb/s data rate, dissipates 650 mW and the demodulation of PRBS7 PAM-4 input signals has been demonstrated up to 24 GBd with measured BERs of $4{\cdot}10^{-12}/1{\cdot}10^{-13}$ for the LSB/MSB, respectively, with input signals as low as 580 μApp. This approach, featuring application-tailored state-of-the-art TIA and dedicated 2-bit ADC, allows for an optimized design in terms of power consumption and footprint. The last part of the chapter continued the investigation on low power implementations and explored the benefits of high-speed pnp transistors in TIA design. Here, the design characterization of a folded cascode TIA, implemented in the 0.25 μm SiGe:C BiCMOS technology of IHP, process H3P, which offers high-speed complementary transistors with matched performances, has been presented. The amplifier exhibits a differential transimpedance gain of 52.5 dBΩ and a 3 dB bandwidth of 32 GHz, with a measured differential average input referred current noise density of 13.1 pA/$\sqrt{Hz}$ and 70 mW power dissipation. The folded cascode implementation, enabled by the availability of fast pnp HBTs, allowed for increased bandwidth without power dissipation penalty while exhibiting good noise performance.

6

Conclusions

Global IP traffic between and within data-centers continues growing year after year, driven by a variety of applications such as 4G/5G mobile data, data intensive web and cloud services. To support such growth, the underlying optical networks will need to scale in complexity, and bandwidth, evolving from current 100 Gb/s standards towards 400 Gb/s and 1 Tb/s systems. The electronic front-ends that are directly interfacing the photonics devices of such transceivers are an integral part, and strongly influence the overall performance. In this work, different high-performance front-end analog integrated circuits (ICs) have been developed, by making use of different nodes of the SiGe:C BiCMOS technology of IHP, aiming at the next generation of 400 Gb/s datacom and telecom systems. Circuit-level methods for enhancing different performance metrics such as high data rate, low-power consumption and low noise have been presented and demonstrated through the characterization of the fabricated prototypes.

On the transmitter (Tx) side, the improvement of metrics such as the energy requirement per bit and device footprint while maximizing bandwidth and extinction ratio (ER) remains non-trivial. Here the concept of optical-digital-to-analog converter (DAC)enabled by the use of segmented Mach-Zehnder modulators (SEMZMs) has been presented. Two modules featuring integrated 4-b DAC functionality have been implemented. The first one is based on a hybrid integration approach incorporating an I/Q InP SEMZM together with a SiGe BiCMOS driver in the SG13S technology. The assembly demonstrated up to 32 GBd dual polarization 256-QAM signal modulation and transmission over 120 km of SMF with record low 6.4 pJ/bit energy dissipation per bit. This module represents the current state-of-the-art among coherent Tx modules, in terms of low energy-per-bit at such speed. However, hybrid configurations are not ideal for data-center applications where cost and area requirements are very strict. Here, SiPh remains the most promising candidate, due to the unique combination of low fabrication costs, low area requirements and prospective performance enhancements resulting from electronic-photonic integration. Therefore, in the second module the same optical-DAC concept has been applied in the electronic-photonic-integrated-circuit (EPIC) platform of IHP, for the realization of a monolithically integrated Tx comprising a SiPh depletion-type MZM and driver in SG25H4 technology. This module was capable of up to 37 GBd PAM-4 operation, which is the highest baud-rate reported to date among silicon-based modulators. The corresponding energy-per-bit was as low as 13.5 pJ/bit.

On the receiver (Rx) side the focus was on the minimization of the input-referred noise in high-speed transimpedance amplifier (TIA) devices. A design technique for TIAs was presented, which permits simultaneous low-noise and high-bandwidth performance. This methodology was verified by means of analogous TIA implementations in the SG13S and SG13G2 processes in order to evaluate as well the impact of the technology node. These designs featured less than $10\,\mathrm{pA}/\sqrt{Hz}$ averaged input referred current noise density while operating at 100 Gb/s data rate. Using this low-noise design technique, advanced receiver concepts, tailored towards power efficient modules have been presented. A benchmark TIA featuring 60 GHz bandwidth and record low integrated input referred noise density of $5.5\,\mathrm{pA}/\sqrt{Hz}$ was developed. The SG13G2 TIA was then used to implement a custom solution for a PAM-4 Rx front-end capable of demodulating signals at up to 100 Gb/s data rate. Finally, a TIA in folded-cascode architecture which makes use of pnp transistors was presented, exploring the benefits of a complementary technology in power-efficient high-speed Rx front-ends.

SiGe BiCMOS technology has been shown to be capable of providing a path for the realization of high-performance low-cost transceiver modules operating at high data rates. Performance will continue to improve with the aggressive roadmap for these technologies. Cost reduction follows from the higher density integration capabilities and the compatibility with SiPh monolithical integration, enabling higher functionality. Still, several challenges remain to be resolved. On the Tx side, although huge advancements are being made, hybrid solutions still deliver better performance, and innovative means for improving the performance of such modules at the device level are needed, in order to become a competitive alternative. On the Rx side, future implementations should focus on the issue of linearity enhancement towards coherent receiver modules capable of demodulating the signal and correctly extract phase and amplitude information without distortion. Here novel gain control techniques and variable-gain-amplifier (VGA) architectures at the circuit level should be investigated.

In the next years, with more demanding requirements in aggregate data rates and link distances, silicon-photonics (SiPh) is expected to eventually become the preferred solution. The compatibility of SiPh with existing CMOS manufacturing infrastructure for a cost-effective mass production of optoelectronic circuits, is a clear asset and key competitive advantage compared to other integrated photonic technologies. Innovative high-performance solutions in the front-end ICs will be desirable to leverage the limitations of silicon as an optical material. The desirable physical manifestation of the optical transceiver would be as an optoelectronic integrated circuit fabricate monolithically in silicon, combining photonic functionality and electronic intelligence.

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2. **I. García López**, A. Aimone, P. Rito, S. Alreesh, T. Brast, V. Höhns, G. Fiol, M. Gruner, J. K. Fischer, J. Honecker, A. G. Steffan, M. Schell, A. Awny, A. C. Ulusoy and D. Kissinger, "High-Speed Ultralow-Power Hybrid Optical Transmitter Module with InP I/Q-SEMZM and BiCMOS Drivers With 4-b Integrated DAC," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4598-4610, Dec. 2016.

3. **I. García López**, A. Aimone, S. Alreesh, P. Rito, T. Brast, V. Höhns, G. Fiol, M. Gruner, J. K. Fischer, J. Honecker, A. G. Steffan, D. Kissinger, A. C. Ulusoy and M. Schell, "DAC-Free Ultralow-Power Dual-Polarization 64-QAM Transmission at 32 GBd with Hybrid InP IQ SEMZM and BiCMOS Drivers Module", in *IEEE Journal of Lightwave Technology*, vol. 35, no. 3, pp. 404-410, Feb.1, 1 2017.

4. **I. García López**, P. Rito, A. Awny, M. Ko, D. Kissinger and A. C. Ulusoy, "A DC-75-GHz Bandwidth and 54 $dB\Omega$ Gain TIA With 10.9 $\mathrm{pA}/\sqrt{Hz}$ in 130-nm SiGe:C BiCMOS," in *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 1, pp. 61-63, Jan. 2018.

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8. P. Rito, **I. García López**, A. Awny, M. Ko, A. C. Ulusoy and D. Kissinger, "A DC-90-GHz 4-V_{pp} Modulator Driver in a 0.13-μm SiGe:C BiCMOS Process," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 12, pp. 5192-5202, Dec. 2017.

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Honors and Awards:

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- **WYMPHD Forum, 2nd Prize**, IEEE International Conference on Electronics, Circuits and Systems (ICECS) 2014, Marseille, France.

Acronyms

ADC analog-to-digital-converter.
AGC automatic gain control.
APD avalanche photodiode.

B2T binary-to-thermocode.
BEOL back-end-of-line.
BiCMOS Bipolar Complementary Metal-Oxide-Semiconductor.
BR bit rate.
BW bandwidth.

DAC digital-to-analog converter.
DCI data-center interconnects.
DSP digital signal processing.

EA electro-absorption.
EM electromagnetic.
E/O electro-optical.
EPIC electronic-photonic-integrated-circuit.
ER extinction ratio.

FEOL front-end-of-line.

IC integrated circuit.
IL insertion loss.
IM/DD intensity-modulation/direct-detection.
IRT intrinsic region thickness.

LDO low-dropout.
LSB least significant bit.

MMI multi-mode interference.
MSB most significant bit.
MZM Mach-Zehnder modulator.

NRZ non-return-to-zero.

OIF Optical-Internetworking-Forum.
OOK on-off-keying.
OSNR optical signal-to-noise-ratio.

PAM pulse-amplitude-modulation.
PD photodiode.
PSK phase-shift-keying.

QAM quadrature-amplitude-modulation.

ROSA receiver optical sub-assembly.
Rx receiver.

SDM space division multiplexing.
SEMZM segmented Mach-Zehnder modulator.
SiPh silicon-photonics.
SNR signal-to-noise-ratio.
SOI silicon-on-insulator.

THD total harmonic distortion.
TIA transimpedance amplifier.
TOSA transmitter optical sub-assembly.
TWE travelling-wave-electrode.
TWE-MZM travelling-wave electrode Mach-Zehnder modulator.
Tx transmitter.

VGA variable-gain-amplifier.

WDM wave-length division multiplexing.