Fully Integrated BiCMOS High-Voltage Driver Circuits for On-Chip RF-MEMS Switch Matrices

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Abstract

In this work, building blocks required to control electrostatically actuated radio frequency micro- electro- mechanical system (RF-MEMS) matrices were developed and integrated into demonstrator circuits. The realized chips include the high-voltage (HV) generation and switching units integrated together with the RF-MEMS switches. To the author's knowledge, this work is the first to present monolithically integrated radio frequency systems for operating frequencies above 20 GHz consisting of RF-MEMS switches, on-chip HV generation circuits and an HV switch matrix. The developed HV circuits could be further used as driver for electrostatically actuated microfluidic pumps or valves.

Three on-chip HV generation concepts are analyzed: the latched charge pump (CP), the Dickson CP and the Greinacher-Cockroft-Walton (GCW) topology. The designed Dickson CP provides two output voltages which are required to bias the HV switch matrix. The clock tree of the Dickson CP is modified to synchronize the two high-voltage outputs resulting in a minimized voltage ripple between these two outputs. Output voltages greater than 40 V are generated.

A simple HV switching circuit based on a high-voltage npn silicon germanium (SiGe) heterojunction bipolar transistor (HBT) is presented. As an alternative approach, HV inverters consisting of lateral drift metal oxide semiconductor (NLDMOS and PLDMOS) transistors, enabling operating voltages up to 50 V, are fabricated. Level shifter (LS) circuits, required to drive the PLDMOS transistor, are analyzed regarding steady state leakage current and circuit complexity. Transient simulations of the designed LS core show a rise and fall time of 200 ps.

A K-band (27 – 40 GHz) RF-MEMS-based single-pole double-throw (SPDT) switch chip is realized applying two different HV concepts: (a) one CP per RF-MEMS and discharging with NLDMOS transistors (b) single CP combined with HV switches. Furthermore, a V-band (40 – 75 GHz) impedance tuning circuit comprising four RF-MEMS switches, driven by four HV switches and powered by a single CP is realized in this work. Measured scattering parameters of all demonstrator circuits verify the successful actuation of the RF-MEMS switches driven by the integrated HV generation and switching circuitry.

Zusammenfassung

In dieser Arbeit wurden Bausteine zur Steuerung elektrostatisch betätigter Radio Frequenz Mikro- elektro- mechanisches system (RF-MEMS) Matrizen entwickelt und in Demonstratorschaltungen integriert. In den realisierten Chips sind die Hochvolt(HV)erzeugungs- und Schalteinheiten zusammen mit den RF-MEMS Schaltern monolithisch integriert. Nach bestem Wissen des Autors stellt diese Arbeit erstmalig monolithisch integrierte Hochfrequenzsysteme für Betriebsfrequenzen größer 20 GHz vor, die aus RF-MEMS Schaltern, Ladungspumpe und einer Hochvoltschaltmatrix bestehen. Die entwickelten HV-Systeme sind auch als Treiber für elektrostatisch betätigte Mikrofluidikpumpen oder -ventile einsetzbar.

Drei integrierbare Ladungspumpenkonzepte wurden analysiert: die "latched" Ladungspumpe (CP), die "Dickson-" und die "Greinacher-Cockroft-Walton (GCW)"-Topologie. Die entwickelte "Dickson" CP stellt zwei Ausgangsspannungen zur Verfügung, die für die Arbeitspunkteinstellung der HV-Schaltmatrix erforderlich sind. Um die beiden Hochspannungsausgänge zu synchronisieren, wurde die Verschaltung des Taktsignals modifiziert. Dadurch konnte die Spannungswelligkeit zwischen diesen beiden Ausgängen minimierten werden. Mit den entworfenen Ladungspumpen können Spannungen bis 40 V erzeugt werden.

In dieser Arbeit wird eine einfache Hochspannungsschaltung auf Basis eines Hochvolt NPN Silizium-Germanium (SiGe) Heterojunction-Bipolartransistors (HBT) vorgestellt. Alternativ dazu wurden HV-Schalter realisiert, die aus lateralen Drift-Metall-oxid-Halbleiter-Transistoren (NLDMOS und PLDMOS) bestehen und Betriebsspannungen bis zu 50 V ermöglichen. Verschiedene Level-Shifter (LS) Schaltungen, die zum Steuern des PLDMOS-Transistors erforderlich sind, wurden hinsichtlich des Ruhestromes und der Komplexität der Schaltung analysiert.

Für das K-Band (27 – 40 GHz) wurde eine auf RF-MEMS basierende Single Pole Double Throw (SPDT) Schaltung mit zwei verschiedenen HV-Konzepten realisiert: (a) eine CP pro RF-MEMS und Entladung mit NLDMOS-Transistoren (b) ein CP kombiniert mit HV-Schaltern. Darüber hinaus wurde in dieser Arbeit eine V-Band (40 – 75 GHz) Impedanzabstimmschaltung mit vier RF-MEMS-Schaltern realisiert, die von vier HV-Schaltern angesteuert und von einer einzelnen CP versorgt wird. Gemessene Streuparameter aller Demonstratorschaltungen bestätigen das erfolgreiche Betätigen der durch die integrierte Hochspannungserzeugungs- und -schalttechnik angesteuerten RF-MEMS Schalter.

Contents

Glossary

ADS™	Keysight Advanced Design System
AlCu	Aluminum Copper
BBM	Break-Before-Make
BEOL	Back End Of Line
BiCMOS	Bipolar Complementary Metal Oxid Semiconductor
CCLS	Charge Coupled Level Shifter
CoSi	Cobalt Silicide
C-V	Capacitance versus Voltage
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
CTS	Charge Transfer Stage
DC	Direct Current
DCVSL	Differential Cascode Voltage Switch Logic
DMOS	Double Diffused Metal Oxide Semiconductor
DMTL	Distributed MEMS Transmission Line
DVC	Digital Variable Capacitor
ESL	Etch Stop Layer
FEOL	Front End Of Line
FIB	Focused Ion Beam
GCW	Greinacher-Cockroft-Walton
GSG	Ground Signal Ground
GSGSG	Ground Signal Ground Signal Ground

HBT	Heterojunction Bipolar Transistor
HiSIM_HV	Hiroshima-University STARC IGFET model
HV	High-Voltage
I^2C	Inter-Integrated Circuit Bus
ISS	Impedance Standard Substrate
I-V	Current versus Voltage
ILD	Inter Layer Dielectric
ITRS	International Technology Roadmap for Semiconductors
LCD	Liquid Crystal Display
LDD	Lightly Doped Drain
LDHBT	Lateral Drift Heterojunction Bipolar Transistor
LDMOS	Lateral Drift Metal Oxide Semiconductor
LNA	Low Noise Amplifier
LPD	Liquid Powder Display
LS	Level Shifter
LV	Low-Voltage
MEMS	Micro-Electro-Mechanical System
MIM	Metal-Insulator-Metal
MISO	Master In Slave Out
MOS	Metal Oxide Semiconductor
MOSI	Master Out Slave In
NLDMOS	N-type Lateral Drift Metal Oxide Semiconductor
NMOS	N-type Metal Oxide Semiconductor
NOC	Non-Overlapping Clock
NW	N-Well
PA	Power Amplifier
PCB	Printed Circuit Board
PDK	Process Design Kit
PLDMOS	P-type Lateral Drift Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor

PSP	Penn State-Philips surface potential MOS compact model
PW	P-Well
PW-block	drawing layer for P-well implantation
RF	Radio Frequency
RF-MEMS	Radio Frequency Micro-Electro-Mechanical System
RO	Ring Oscillator
SCLK	Serial CLocK
SEM	Scanning Electron Microscopy
SG13	0.13 µm SiGe:C BiCMOS
SIC	Selectively Implanted Collector
SiO_2	Silicon Dioxide
SMU	Source Measurement Unit
SOA	Safe Operating Area
SOLT	Short Open Load Thru
S-parameter	Scattering parameter
SG25	0.25 µm SiGe:C BiCMOS
SiGe	Silicon Germanium
SiP	System in Package
SOI	Silicon On Insulator
SP4T	Single-Pole Four-Throw
SPDT	Single-Pole Double-Throw
SPI	Serial Peripheral Interface bus
SPnT	Single-Pole Multiple-Throw
SPST	Single-Pole Single-Throw
SRAM	Static Random-Access memory
SS	Slave Select
STI	Shallow Trench Isolation
VCO	Voltage Controlled Oscillator
VIA	Vertical Interconnect Access
VNA	Vector Network Analyzer
WLE	Wafer Level Encapsulation

List of Symbols

A_E	Emitter area	μm^2
BV_{CBO}	Collector-base breakdown voltage (open emitter)	V
BV_{CEO}	Collector-emitter breakdown voltage (open base)	V
BV_{DS}	Drain-Source breakdown voltage	V
BV_{GOx}	Gate oxide breakdown voltage	V
BV_{GS}	Gate-Source breakdown voltage	V
C_G	Gate capacitance	F
C_{OUT}	Output capacitance	F
C_{Ox}	Oxide capacitance	F
C_S	Stray capacitance	F
C_{stage}	Stage capacitance	F
ε_{Si}	Permittivity of silicon $= 11.7 \cdot 8.854 \cdot 10^{-12}$	$^F/_m$
f_{Clk}	Clock signal frequency	Hz
f_{Max}	Maximum oscillation frequency	Hz
f_T	Maximum transit frequency	Hz
γ	Body effect coefficient	$\sqrt{V}$
β	Transconductance parameter	$^A/_{V^2}$
μ_n	Mobility of the electrons	$^{cm^2}/_{Vs}$
$HS\Delta$	HS_V_{DD} - HS_V_{SS}	V
I_B	Base current	A
I_C	Collector current	A
I_{DD}	Supply current	A

I_{sub}	Substrate current	A
I_{CP}	Charge pump output current	A
I_D	Drain current	A
HS_I_{DD}	High-Side supply current	A
$I_{D,max}$	Maximum drain current	A
IL	Insertion loss	dB
I_{Load}	Load current	A
I_{OUT}	Output current	A
HS_I_{SS}	High-Side supply current	A
$\lambda/4$	Quarter wave length	m
q	Elementary charge $= 1.602 \cdot 10^{-19}$	C
R_{CB}	Collector-Base resistance	Ω
R_{Load}	Load resistor	Ω
R_S	Stage resistance	Ω
S_{11}	RF signal reflection at port 1	dB
S_{21}	RF signal transmission	dB
S_{22}	RF signal reflection at port 2	dB
$\tau_{R,F}$	Signal rise or fall time	s
V_{DD}	Supply voltage	V
V_{tune}	Tuning voltage	V
V_0	Ideal charge pump voltage	V
V_{BE}	Base-Emitter voltage	V
V_C	Collector voltage	V
V_{CB}	Collector-Base voltage	V
V_{CE}	Collector-emitter voltage	V
V_{Clk}	Clock signal amplitude	V
V_{CP}	Charge pump output voltage	V
V_{ctrl}	Control voltage	V
HS_V_{DD}	High-side bias voltage	V

V_{DS}	Drain-Source voltage	V
V_{E}	Emitter voltage	V
V_{ES}	Emitter-Substrate voltage	V
V_{fb}	Flat-band voltage	V
V_{GS}	Gate-Source voltage	V
V_{IN}	Input voltage	V
V_{LScore}	Level shifter core voltage	V
V_{LSout}	Level shifter output voltage	V
$V_{LSout.m}$	Level shifter output voltage (measured)	V
$V_{LSout.s}$	Level shifter output voltage (simulated)	V
V_{MEMS}	MEMS actuation voltage	V
V_{OUT}	Output voltage	V
V_{rpl}	Voltage ripple	V
V_{SB}	Source-Bulk voltage	V
HS_V_{SS}	High-side bias voltage	V
V_{th}	Threshold voltage	V
V_{th0}	Zero-bias threshold voltage	V

1 Introduction

1.1 Motivation and Objective

In the last decade, significant progress on radio frequency micro- electro- mechanical system switch (RF-MEMS) switch-based devices paved the way for using these devices not only for niche applications but also for consumer electronics. micro-electro-mechanical system (MEMS)-based tuners are meanwhile considered one of the key components for next generation mobile applications [1], [2]. Despite the fact that reliability [3] and packaging challenges are the main bottlenecks for RF-MEMS switch devices, the developments in the last years clearly show the potential use of these devices in consumer electronics [4]–[8].

Embedded RF-MEMS switches in the silicon germanium (SiGe) bipolar complementary metal oxid semiconductor (BiCMOS) technologies [9], [10] are essential components to design single chip radio frequency micro systems [11], [12] at millimeter-wave frequencies. The integration of an RF-MEMS switch into a complementary metal oxid semiconductor (CMOS) or BiCMOS platform allows the combination with the control electronics on the same chip.

In general, electrostatically actuated RF-MEMS switches require high voltages. High-voltage control electronics and MEMS devices are often combined using the system in package (SiP) approach [13]–[16], resulting in an increased assembly effort. Such high voltages can be generated also in a BiCMOS platform, as demonstrated in [17].

A challenge is the switching of the high-voltage for the MEMS actuation, since typical RF BiCMOS technologies do not include high-voltage devices. Different solutions e.g. discharge resistor [17], stacking of low-voltage (LV) CMOS transistors [18] are proposed to overcome this problem. In [11], the replacement of the energy wasting discharge resistor used in [17] and [12] by a dual mode charge pump [19] is described. Thus, a circuit with two RF-MEMS single-pole single-throws (SPSTs) switches requires four charge pumps and four oscillators, which results in a significant increase of the chip area and power consumption.

For RF-MEMS switch matrix applications like phase shifters [20]–[22], capacitor banks [23]–[25], impedance matching circuits [20], [26], tunable filters [22], redundancy switch matrices in satellites [27], [28] or single-pole multiple-throw (SPnT) [15], [29], the required layout area for multiple charge pumps, oscillators and their control logic is remarkable. This can be reduced by using a single charge pump (CP) in conjunction with a high-voltage (HV) switch matrix based on lateral drift metal oxide semiconductor (LDMOS) inverters. The chip size of an RF-MEMS switch-based impedance tuning circuit combined with the on-chip HV circuitries enables the integration into an RF-probe used for on-wafer noise parameter and load-pull measurements. Furthermore, the HV switch matrix can be used to drive electrostatically actuated micropumps and valves in microfluidic applications.
The objective of this work is the development of a high-voltage source and a low-power high-voltage switch matrix to drive an electrostatically actuated RF-MEMS switch array. With the monolithically integrated high-voltage generation and switching circuitry, the assembly and wiring effort, which is necessary to control the RF-MEMS switch matrix, can be drastically reduced. To the best of the author's knowledge, beside this work, there are no other monolithically integrated radio frequency systems above 20 GHz consisting of RF-MEMS switches, on-chip high-voltage generation, and high-voltage switch matrix reported so far.

1.2 Integrated RF-MEMS Switch Actuation Circuits

Electrode voltages for integrated electrostatically actuated MEMS are in the range of 20 V and above and hence significantly higher than the bias voltage of the integrated BiCMOS circuitries. Therefore, HV transistors like LDMOS or circuit concepts like stacked CMOS are required. Further challenges with the integration of the switching and charge pumps for high-voltage generation are the minimization of the layout area and the power consumption required by these circuits.
If every single electrostatically actuated MEMS is controlled by a dedicated CP, the chip size will increase significantly for MEMS matrix applications. The integrated RF-MEMS switches in [11], [12], [17], [30] are driven by a dedicated CP. The charge pump in [12], [17] is based on a modified Dickson [31] circuitry and the charge pumps used in [11], [30] are based on so called "latched charge pump" [19]. This approach simplifies the design procedure, since the same CP cell is placed multiple times. The power consumption scales with the number of actuated MEMS, which is economic

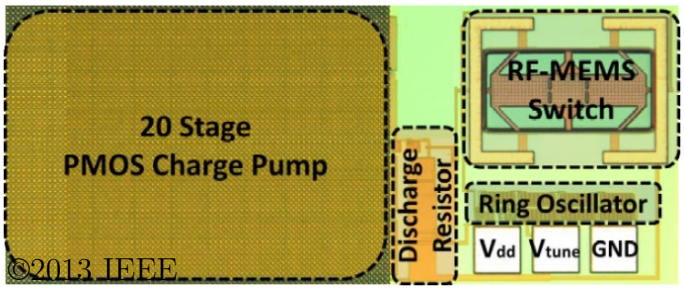


Figure 1.1: Single CP and discharge resistor for one RF-MEMS switch [17].

if only a few MEMS of the matrix are active and the remaining part is in "off-state". Once the MEMS is actuated (latched), the clock frequency and amplitude of the clock signal generator could be decreased, which results in a reduced output voltage of the CP, hence the power consumption is reduced. Having a dedicated CP for each MEMS will result in an increased pull-in time caused by the ramp-up time of the CP. To reset an electrostatically actuated MEMS, the electrode-membrane capacitor needs to be discharged. A simple approach using a high-ohmic resistor is applied in the circuit shown in Fig. 1.1 [17]. A decreased value for the resistor will cause a reduced discharge time of the MEMS. On the other hand, the actuation time of the RF-MEMS switch is increased, since the rise time of the CP is influenced by the discharge resistor. With a load resistance of 250 kΩ, the switch-off time is in the range of 30 µs. Since the resistor is a permanent load for the CP, the leakage current at 40 V output voltage is 8 µA with 5 MΩ load resistance and 160 µA with 250 kΩ. Thus, the power consumption in actuation mode for a single CP in [17] is in the range of 12 mW to 75 mW. In release mode (up–state), the power consumption is zero, since the CP is off. This concept is also applied in [12] where a RF-MEMS-based SPDT switch is driven by two charge pumps in combination with 1 MΩ discharge resistors. To avoid the permanent leakage current, the energy-wasting discharge resistor can be replaced by a second CP to discharge [19] the electrode capacitance. A single stage (charge transfer stage (CTS)) comprising the charging and discharging stage is depicted in Fig. 1.2. Therefore, two CPs and two clock generators are required to control a single RF-MEMS switch. In Fig. 1.3, the layout of a single RF-MEMS switch combined with a dual mode CP is depicted [30]. This method decreases the power consumption at the cost of an additional CP. For a single-pole double-throw (SPDT), consisting of two RF-MEMS switches to be controlled, four CPs are required. Another concept to reduce the leakage

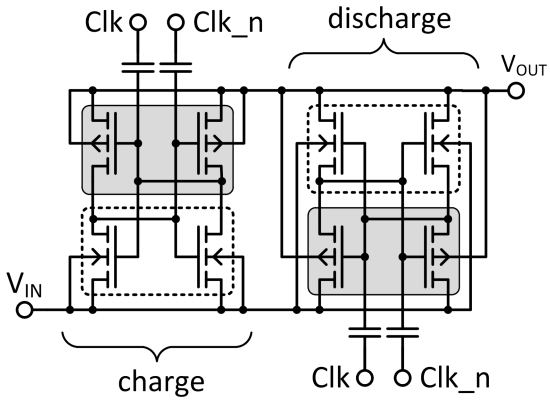
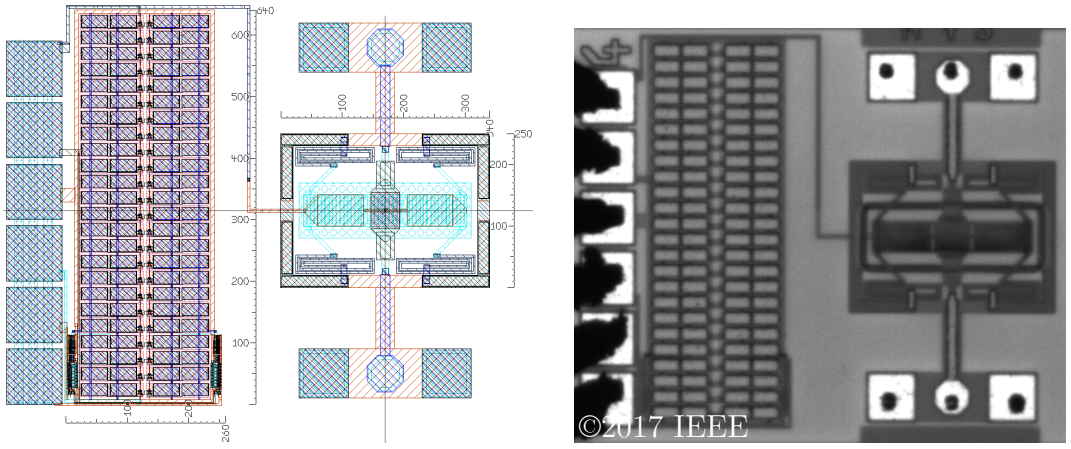


Figure 1.2: Charge pump stage described in [19]. One stage consists of two CTS based on [32]. One stage is used to increase and the second stage to decrease the output voltage (the dashed line symbolizes an isolated p-well and the gray area indicates the n-well).



(a) (b)

Figure 1.3: Layout (a) and chip micrograph (b) of a dual mode CP combined with an SG25 RF-MEMS SPST switch [30]. In comparison to the RF-MEMS switch, the layout area required by the CP is significantly bigger.

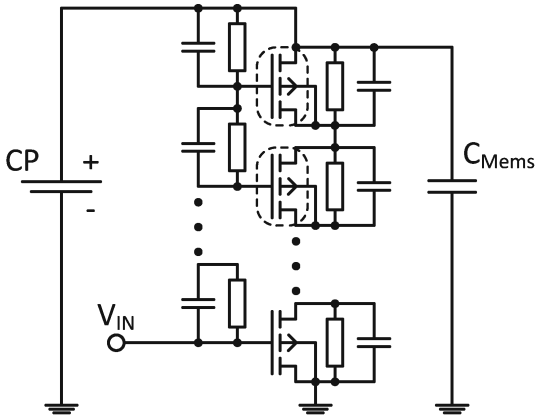


Figure 1.4: Discharge circuitry based on stacked MOS for a single MEMS. The dashed regions symbolize an isolated p-well. The voltage supply represents the charge pump (CP).

current is to replace the discharge resistor or the discharge pump with a stack of isolated N-type metal oxid semiconductor (NMOS) transistors. Every transistor must be placed in a separate isolated well using a triple well process or a silicon on insulator (SOI) technology. To avoid the breakdown of the low-voltage NMOS transistor, the design of the biasing network is critical [18], [33]–[35]. The number of required transistors depends on the drain-source breakdown voltage and the output voltage of the CP. The resistive and capacitive voltage divider circuit shown in Fig. 1.4 [18], [36] are necessary to set and keep the source, drain and gate voltages below their breakdown levels. The drawback of this concept is the leakage current caused by the voltage divider. As a rule of thumb, the minimum number of required stages can be estimated by dividing the maximum output voltage of the CP by half the drain-source breakdown voltage of the low-voltage metal oxid semiconductor (MOS) transistors $\left(N = \frac{Vout_{CP}}{BV_{DS}/2}\right)$. The usability of this concept strongly depends on the availability of isolated transistors and the complexity of the discharge circuitry.

If an HV-LDMOS or HV-bipolar module is available in the technology, the discharge resistor or the discharge pump can be replaced by a single N-type lateral drift metal oxide semiconductor (NLDMOS) or a npn lateral drift heterojunction bipolar transistor (LDHBT). This results in reduced power consumption and minimized layout area for the CP. Compared to the previously described concepts, the HV transistor as the discharge unit is the most compact and energy-efficient solution for MEMS control circuitry.

Due to the need of multiple CPs, the aforementioned circuit concepts are applicable to systems with a few MEMS. Independent from the concepts described above, the capacitors in the CP and the MEMS electrode are discharged in reset mode (up-state). Hence, the lost charge needs to be generated whenever the MEMS is set into "active mode" (down-state).

1.3 Concepts for High-Voltage Switch Matrices

In this section, high-voltage switch matrices to drive electrostatically actuated MEMS arrays are analyzed. A 16 channel 300 V switch matrix using SOI technology is described in [37]. The system is assembled on a micro-printed circuit board (PCB) together with an additional DC-DC converter and a microcontroller while the MEMS matrix is on a separate chip. A capacitor bank for a frequency range from 500 MHz to 3 GHz is realized using a post-CMOS MEMS process in [25]. The HV distribution network is based on 30 V CMOS transistors and combined with the CP on a single silicon chip. In [2], aperture tuned antennas for 3G-4G applications using MEMS digital variable capacitor (DVC), developed by Cavendish Kinetics [7], are described. The existence of a high-voltage switching matrix is not mentioned. Nevertheless, a patent [38] of an integrated CP can be found. The company Wispry (now AAC Technologies) [8] has developed a capacitor bank [39] to be used in smart phones (850, 1800 and 2100 MHz). The capacitance can be controlled by an integrated serial peripheral interface bus (SPI). Without providing any details about the integrated CP and the HV switching, the authors mention the technology which offers high-voltage transistors. Like Cavendish, Wispry [8] holds a patent [40] for the CP. In [15] a single-pole four-throw (SP4T) operating from DC to 26 GHz developed by Analog Devices is described. The co-packaged HV driver chip is based on a double diffused metal oxide semiconductor (DMOS) process.
In table 1.1, several concepts are shown and compared according to their usability for MEMS matrix applications. The concepts are rated based on four different criteria:

1. Layout Area (estimated chip size)
2. Power Consumption
3. Technology (complexity and required devices)
4. Switching Time

For the highest rating, the symbol "++" is used and the lowest rating is illustrated with "– –". Additionally, comments are included in the table to provide an explanation.
To decrease the power consumption of the CP, a control circuit is required. This is recommended for the "single CP" approach, since the CP is constantly active. For applications including only a few electrostatically actuated MEMS devices, a less complex technology with LV CMOS transistors can be chosen. An HV switch matrix is required for applications with several RF-MEMS switches like impedance matching or tuning circuitries, SPnT switches or phase shifters. To summarize the comparison, it can be stated that it is mandatory to use a high-voltage switch matrix for MEMS matrix applications.

Table 1.1: Comparison of monolithically integrated driver circuit concepts for RF-MEMS switch matrix applications.

	Dedicated CP for every MEMS combined with				**Single CP** combined with
	Discharge resistor	Discharge pump	Stacked LV-NMOS	HV-NLDMOS HV-HBT	HV-Switch matrix
Layout area	– – **big CP to compensate ohmic loss**	– – **Two CPs**	– **bias network for LV-NMOS**	+ **Compact transistor**	+ + **Single CP and compact HV-switches**
Power consumption	– – **ohmic loss causes leakage current**	– **One CP is permanently active**	– **Leakage current in bias network**	+ + **no bias network**	– **CP is permanently active**
Switching time	– – **slow due to ohmic loss**	– **Depends on CP and C_{Load}**			+ + **Fast HV-inverters**
Technology	+ + **CMOS**	+ **Triple well or SOI**		– **HV-transistor required**	– – **HV N- and PLDMOS required**
References	[12], [17], [41]	[11], [30]	[18], [36]	This work section 5.1.1	<10 GHz [25], [42], [43] ≥ 10 GHz section 5.1.2 [44] section 5.2 [45]

1.4 Thesis Organization

In this thesis, high-voltage generation and switching circuits for on-chip RF-MEMS switch actuation are analyzed and demonstrator circuits are realized. The circuits are fabricated in a triple well 0.25 µm SiGe:C BiCMOS process [46]. Several modules are realized within this technology: flash memory-, an LDMOS- [47], [48], an HV heterojunction bipolar transistor (HBT)- [49], [50] and an RF-MEMS switch module [9], [51].

In chapter 2, the high-voltage transistors LDMOS and LDHBT are described. The process flow of both devices is explained briefly and measured DC characteristics for both transistor types are presented. Secondly, the embedded RF-MEMS switch device is described. The brief description of the RF-MEMS switch process flow is enhanced with figures showing characteristic capacitance versus voltage (C-V) and scattering parameter (S-parameter) data.

The integrated CP generates the actuation voltage for the RF-MEMS switches and provides the bias voltage for the high-voltage switches. In section 3.2, on-chip charge pump topologies are analyzed. To control an HV inverter consisting of a low gate oxide breakdown voltage (BV_{GOx}) P-type lateral drift metal oxide semiconductor (PLDMOS) and an NLDMOS transistor a level shifting circuit is mandatory. In section 3.3, different concepts for high-voltage level shifting circuitries, required to control the high-voltage inverter, are analyzed and schematic diagrams of the circuits are shown. Since the level shifter is biased by an integrated charge pump, the main criteria was the Direct current (DC) leakage current which influences the power consumption of the level shifter.

In chapter 4, the designed circuitries required for the HV generation and switching are described. In section 4.1, the oscillator circuit providing the clock signal for the CP is described. In section 4.2.1, transient circuit simulation results of the previously analyzed CP types are presented and compared, based on the generated output voltage for various load conditions, second output voltage, circuit complexity and required layout area. Based on this comparison, a Dickson type CP was designed and is presented in section 4.2. After the description of the HV generation circuitries, the HV switching circuitries are presented. Firstly, a circuit based on HV LDHBTs is presented in section 4.3. As an alternative high-voltage switch, an LDMOS-based HV inverter including the mandatory level shifter circuit is described in section 4.4.1.

In chapter 5, the designed demonstrator chips are described and measurement re-

sults are presented. Initially, an alternative approach without high-voltage switching circuitry: an RF-MEMS-based SPDT switch driven by two charge pumps and discharged by two NLDMOS transistors is designed and realized. Secondly, an RF-MEMS-based SPDT switch is designed and presented in section 5.1.2 which includes the high-voltage LDMOS inverters and a CP to control the embedded RF-MEMS switches. Lastly, an RF-MEMS-based impedance tuning circuit comprising four HV switches and powered by a single on-chip CP is described in section 5.2. The operation of the on-chip high-voltage generation and switching circuitry is demonstrated by the measured S-parameters for various combinations of activated RF-MEMS switches.

2 HV Transistors and RF-MEMS in a SiGe:C BiCMOS Technology

Two different high-voltage transistor types (LDMOS and HBT) are used in this work to drive the embedded RF-MEMS switch. In the following sections the HV devices and the embedded RF-MEMS switch are described in more detail and measured data is provided.

2.1 High-Voltage Complementary LDMOS

A p-type and an n-type LDMOS are the core transistors of a high-voltage inverter, which is designed in this work to control the RF-MEMS switch actuation voltage. The 0.25 µm SiGe:C BiCMOS process [46] is based on a low ohmic p-doped silicon substrate. Deep n-doped regions are mandatory for fabricating a high-voltage PLDMOS transistor. The challenge for the fabrication of PLDMOS transistrors is to realize a very deep n-doped well (n-well) region in the p-doped silicon substrate. With the available implantation tool, the maximum depth for an n-well is approximately 1 µm. Therefore, the high-energy phosphorus implantation step is outsourced.

2.1.1 Process Integration of the High-Voltage LDMOS Transistors

In this section, the fabrication of modularly integrated high-voltage LDMOS transistors are described. Based on the experiences for processing of high-voltage LDMOS [47] the process flow was optimized and partially reordered. The cross-section of the symmetric HV-NLDMOS is shown in Fig. 2.1 and the cross-section of the symmetric HV-PLDMOS is shown in Fig. 2.2. An overview of the process flow for the HV LDMOS as described later on is shown in Fig. 2.3.

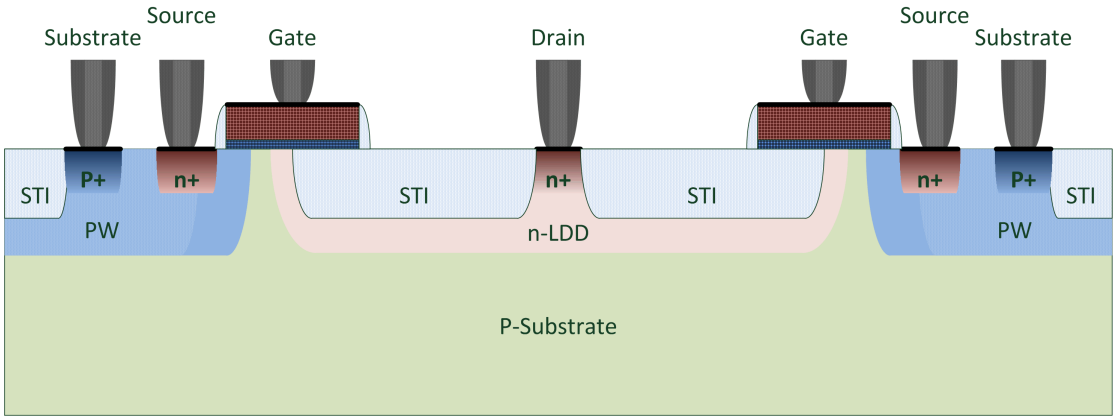


Figure 2.1: Cross-section of the symmetric HV-NLDMOS with a shared drain contact. (STI: shallow trench isolation, PW: p-doped well, n-LDD: lightly n-doped drain region, p+: highly p-doped region, n+: highly n-doped region).

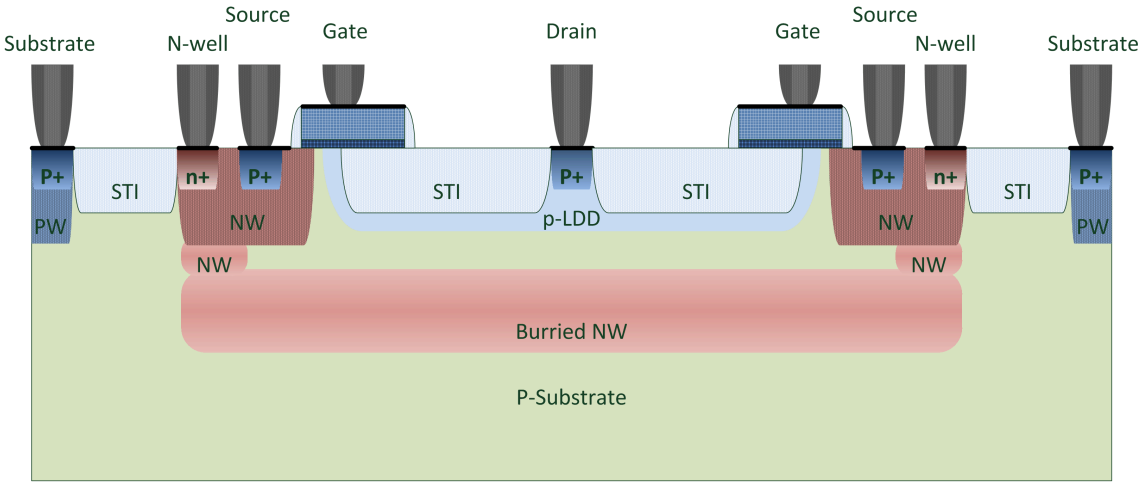


Figure 2.2: Cross-section of the symmetric double gate HV-PLDMOS with a shared drain, surrounded with a substrate contact ring. (STI: shallow trench isolation, p-LDD: lightly p-doped drain region, NW: n-doped well, p+: highly p-doped region, n+: highly n-doped region).

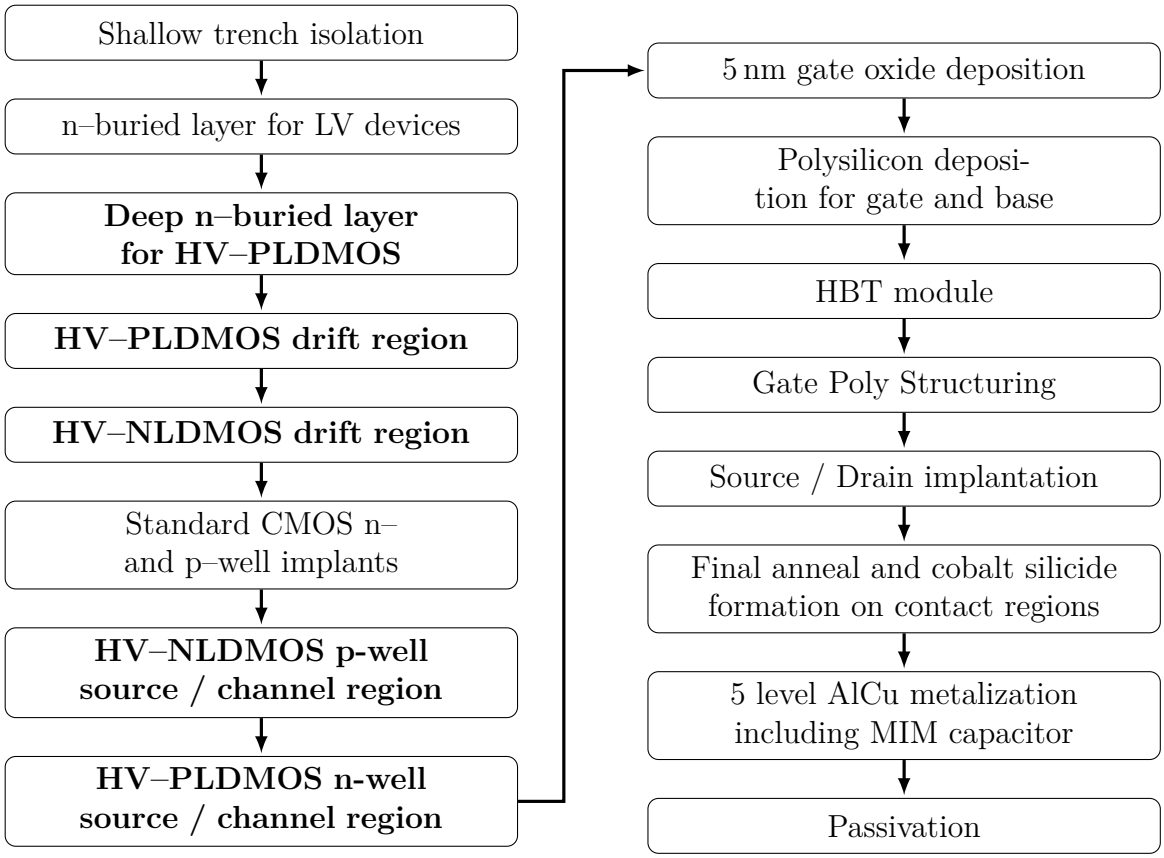


Figure 2.3: Process flow diagram of base SiGe:C BiCMOS process including the HV LDMOS module. The bold fields indicate the five additional mask steps necessary for HV LDMOS preparation.

The process starts with the definition of silicon dioxide regions (shallow trench isolation (STI)) by dry etching trenches into silicon substrate and refilling these trenches with silicon dioxide. After removing the silicon nitride, used as the masking layer for the previous step, 3 µm thick photo-resist is deposited, exposed and developed based on the mask for the n-buried layer. The n-doped buried layer was implanted with an energy of 750 keV with a phosphorus dose of $5 \times 10^{13}\,\mathrm{cm}^{-1}$. Thereafter, a high-energy implantation step is performed to form deep n-well regions which are essential for high-voltage PLDMOS. For high-energy implantation in the 3 – 6 MeV range, a 10 µm thick layer of photo-resist is necessary to protect the remaining parts of the chip. At the time of fabrication, two external facilities with different implanter tools were available. Therefore, two wafers are processed with an implantation energy of 3 MeV and a phosphorus dose of $1 \times 10^{13}\,\mathrm{cm}^{-1}$, as well as three wafers with an implantation energy of 6 MeV and a phosphorus dose of $2 \times 10^{13}\,\mathrm{cm}^{-1}$. The p-lightly doped drain (LDD) drift region located beneath the shallow trench oxide of the high-voltage PLDMOS is formed by several implantation steps with various energies and boron doses. The n-LDD drift region of the high-voltage NLDMOS is formed by a set of implantation steps with several energies and phosphorus doses. Rapid thermal annealing steps reduce the crystallographic damages due to the previous implantation steps. Several boron implants are performed to define the p-well (PW) regions (substrate) for the low-voltage NMOS devices and the high-voltage NLDMOS transistors. To define the doping concentration in the source and the drift region of the high-voltage PLDMOS transistor, a set of phosphorus implantation steps with various energies and angles is performed. Thereafter, a series of boron enriched implantations with varying angles are performed to adjust the doping concentration in the source and drift region of the high-voltage NLDMOS transistors. These tilted implantation steps are used to perform the so called “pocket implant” and are not part of the previous flow used in [47]. Before the deposition of the gate oxide used for all MOS structures, a thermal annealing step is performed to recover the crystallographic structure affected by the previous implantations. After the annealing step, polycrystalline silicon is deposited to form the gates of the low and high-voltage MOS devices, the polysilicon resistors and the HBT base regions. One more annealing step is applied before continuing with the HBT module, which includes the etching of the emitter window, collector implantation, SiGe:C epitaxy for the base and deposition of arsenic doped amorphous silicon for the emitter. After the npn HBT module, the previously deposited polycrystalline silicon is structured

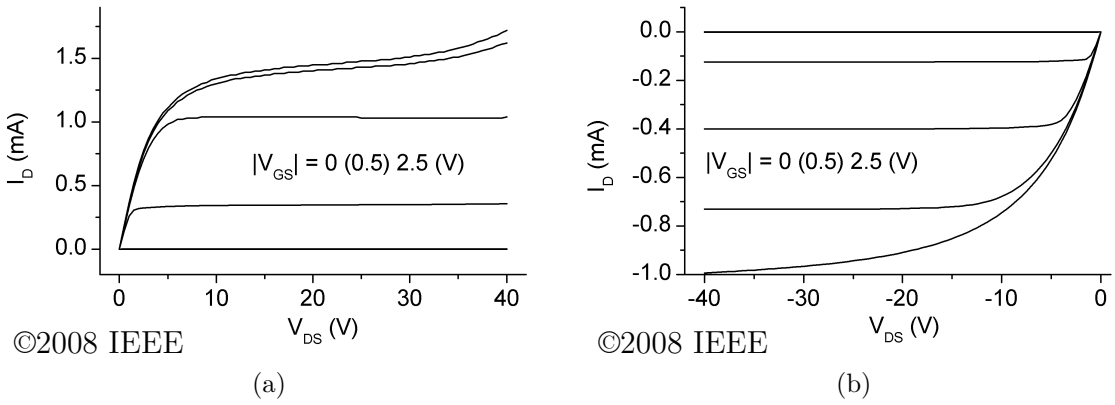


Figure 2.4: Forward output characteristic (drain current (I_D) as a function of drain-source voltage (V_{DS}) and gate-source voltage (V_{GS})) of the NLDMOS (a) and the HV-PLDMOS (b) transistor [47].

to form the gates of the MOS devices, the polysilicon resistors and the external base region of the HBTs. Thereafter, a low-energy arsenic implantation step with subsequent phosphorus-enriched implantation is used for doping the source, drain and gate regions of the NMOS transistors, collector contact of the npn HBT and the polysilicon resistors. Afterwards, a series of implantation steps are performed to define p-doped regions for the source, drain and gate regions of the PMOS transistors, external base contact of the npn HBT and the polysilicon resistors. The previously mentioned areas are coated with cobalt silicide before fabricating the contact plugs. The following process steps for the back end of line (BEOL) module comprising five aluminum copper (aluminum copper (AlCu)) metal layers, tungsten vertical interconnect accesss (VIAs) and the RF-MEMS switch module are described more detailed in chapter 2.3.

2.1.2 DC-Characteristics

In this section, the DC characteristics of the HV PLDMOS and the HV NLDMOS is described. In Fig. 2.4 the output characteristics (drain current (I_D) versus drain-source voltage (V_{DS}) with the gate-source voltage as parameter ($|V_{GS}|$= 0 V (0.5 V) 2.5 V)) of the HV-PLDMOS and NLDMOS transistor are depicted. With a gate-source voltage of 1.5 V the HV-NLDMOS transistor remains in the safe operating area (SOA) without showing breakdown up to 40 V. The HV-PLDMOS transistor can be biased with $V_{GS} = 2$ V.

In Fig. 2.5 the drain-source breakdown characteristics for both types of high-voltage

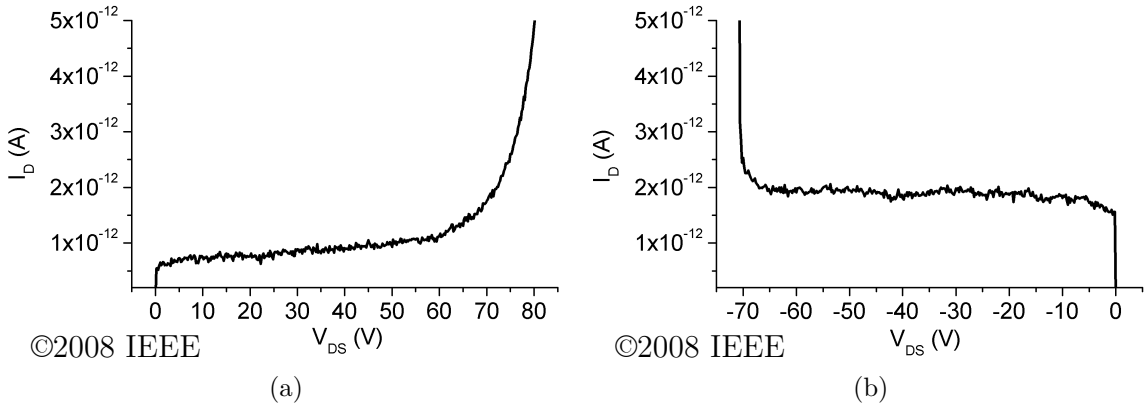


Figure 2.5: Drain-Source breakdown characteristic (drain current(I_D) versus drain-source voltage(V_{DS})) of the HV-NLDMOS (a) and the PLDMOS (b) transistor biased at a gate voltage $|V_{GS}|= 0\,V$ [47].

LDMOS transistors are shown. For these measurements, the gate-source voltage (V_{GS}) is set to 0 V. The breakdown (increased drain current) for the PLDMOS starts at $|V_{DS}|>70\,V$ while the NLDMOS can be biased up to $V_{DS} = 80\,V$.
In general, transistors with high-breakdown voltages have inferior high-frequency properties. Since the gate oxide thickness of the HV-LDMOS is 5 nm, equivalent to the LV-CMOS transistors, the gate-source capacitance is minimized at the cost of a maximum gate-source voltage $V_{GS} = 2.5\,V$.

2.1.3 Conclusion

In this section, the process flow of the HV PLDMOS and NLDMOS transistor is described and measured DC characteristics are shown. In contrast to the previous HV-LDMOS process, the implantation of the deeply buried n-well required for the HV-PLDMOS was performed before the LV CMOS n- and p-well implantation. Two additional masks are used in this process flow for the n-LDD and p-LDD implantations. This enables the use of different doses, energy levels and tilt compared to the standard CMOS n- and p-well dopings. With these additional masks, the fabrication of the LDD regions and the well region can be independently controlled. The measured drain-source breakdown voltage of $BV_{DS} = 70\,V$ for the PLDMOS and 80 V for the NLDMOS transistor prove their usability as high-voltage devices for a DC switch matrix.

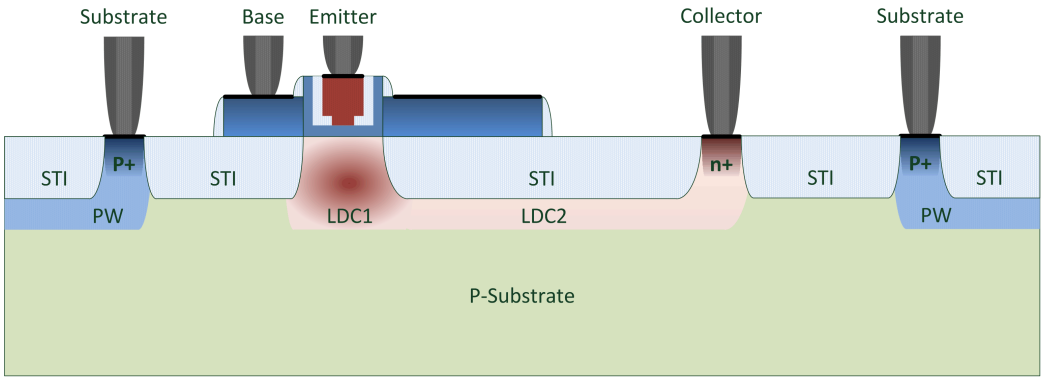


Figure 2.6: Cross-section of the LDHBT. The region LDC2 defines the collector drift region to increase the BV_{CEO} of the device. (STI: shallow trench isolation, PW: p-doped well, p+: highly p-doped region, n+: highly n-doped region).

2.2 High-Voltage Bipolar Transistor

In section 2.1, the fabrication of the SG25 HV-LDMOS transistors is described and the measured DC characteristics are shown. A second high-voltage transistor developed in this technology is a bipolar transistor. Several low-voltage SiGe:C npn HBTs are realized in this 0.25 µm BiCMOS process [52]. The highest collector-emitter breakdown voltage (BV_{CEO}) for an SiGe:C npn HBT is 7 V. To increase the BV_{CEO}, the collector of the HBT is modified resulting in a so called LDHBT (lateral drift region heterojunction bipolar transistor) [49], [50]. In general, the cost for an increased BV_{CEO} required for this application is a decreased f_T and f_{Max}.

2.2.1 Process Integration of the npn LDHBT

The npn LDHBT has an equivalent base-emitter construction like the low voltage SiGe:C HBTs described in [52]. Due to the modified collector, the BV_{CEO} could be increased up to 50 V. A schematic cross-section is depicted in Fig. 2.6. To achieve a superior breakdown voltage, the collector doping profile of the LV HBT is modified and an additional lateral drift region (LDC2) for the collector is introduced. The breakdown voltage of the LDHBT can be varied by changing the length of the lateral drift region. The construction of the lateral collector drift region is comparable with the lateral drain drift region of an NLDMOS device described in section 2.1. An overview of the BiCMOS process flow including the LDHBT module is shown in Fig. 2.7.

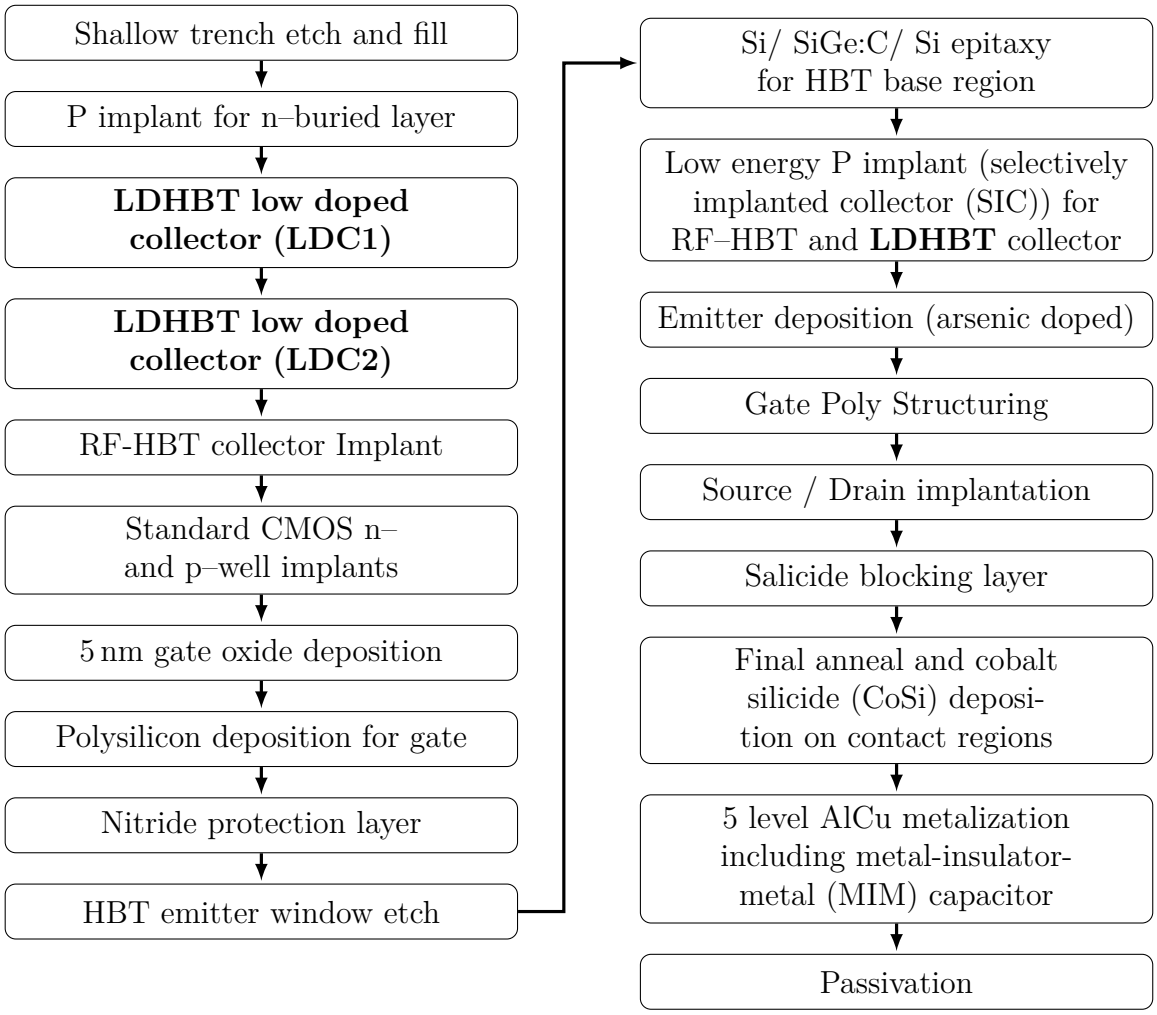


Figure 2.7: Process flow diagram of base SiGe:C BiCMOS process with LDHBT module. The bold fields indicate the additional mask steps necessary for LDHBT preparation [49], [50].

Two additional masks (LDC1, LDC2) are used in three extra mask steps (in bold) for preparation of the LDHBT. Firstly, the shallow trench areas (STI) are etched into the lightly p-doped silicon substrate and refilled with silicon dioxide (SiO_2). As the second mask step, the high-dose phosphorus implant for the n-buried layer is performed. Hereafter, the collector area (LDC1) for the LDHBT is patterned and an additional series of phosphorus implantations are applied to define the collector region of the high-voltage HBT. These steps are followed by another implantation step to form the collector drift region (LCD2). Now, photoresist is deposited and patterned to enable the low dose phosphorus implantations for the collector of the high-speed HBTs. Hereafter, a series of boron-rich implantation steps are applied to form the p-well regions. These regions are needed to fabricate the NMOS transistors or to define isolated p-well regions. To fabricate the n-well regions, a series of Phosphorus implantation steps with different energies and doses are applied. Now, the complete wafer is covered with a 5 nm gate oxide for the MOS devices, followed by the deposition of polycrystalline silicon used for the gates of the MOS devices and the polysilicon resistors. Afterwards, photoresist is deposited and double exposed based on the HBT emitter window mask and the LDHBT emitter window mask (LDC1). The previously deposited polysilicon is now removed using a dry etching process. Now, monocrystalline silicon germanium is grown in the emitter windows using epitaxy to form the base region of the HBTs. The fabrication of the emitter is started with a low-pressure chemical vapor deposition of SiO_2 and a n-doped amorphous silicon layer on top of the base region. These steps are followed by the fabrication of the spacers at the emitter edge using a reactive ion etching process. A last n-doped implantation step (SIC) is performed to form the inner collector region. Subsequently, the emitter region is filled with highly arsenic doped amorphous silicon by chemical vapor deposition. Hereafter, the polycrystalline silicon for the gates of the MOS devices, the polysilicon resistors, and the external HBT base link are structured. A low-energy arsenic implantation and a phosphorus implantation is used to form the source and drain regions of the NMOS transistors. In the next steps, the source, gate and drain regions of the P-type metal oxid semiconductor (PMOS) transistors and the external base of the HBT are implanted. The front end of line (FEOL) components are finalized by a last thermal anneal step and the deposition of CoSi on the source, drain, gate areas of the MOS devices, on the emitter, collector, base regions of the HBTs, on the contact area of the polysilicon resistors and on the substrate contact regions.

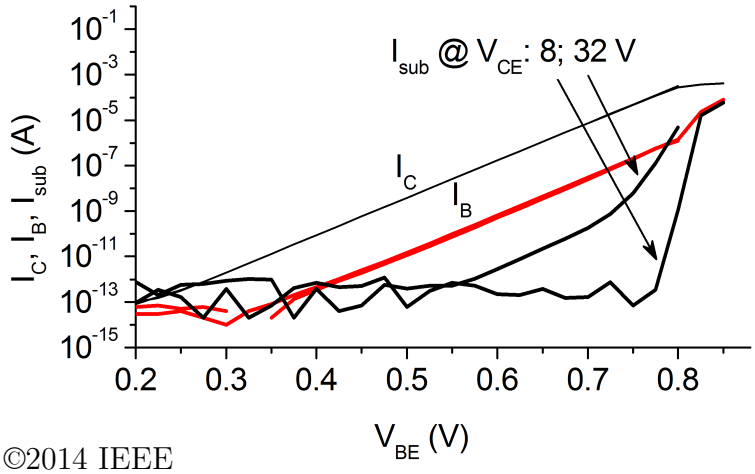
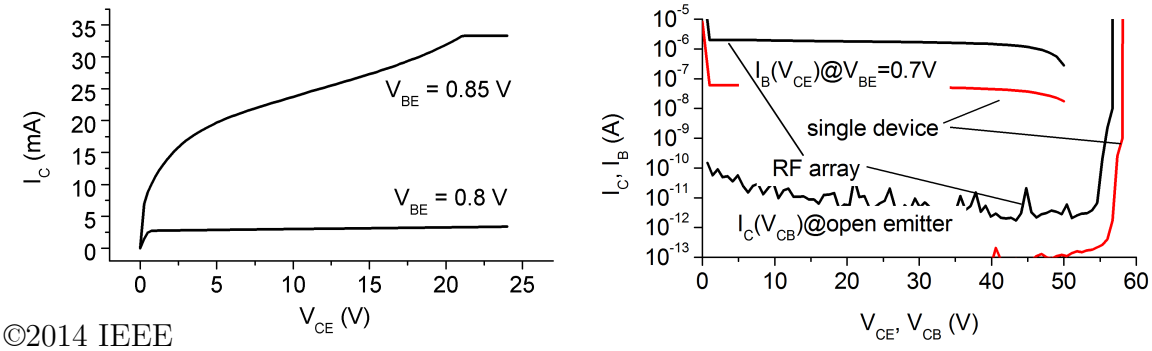


Figure 2.8: Forward Gummel characteristic (collector (I_C)-, base (I_B)-, substrate (I_{sub}) current versus base-emitter voltage (V_{BE})) for a single (A_E=1.76 µm^2) npn LDHBT for collector-emitter voltages V_{CE}=8 and 32 V [50].

2.2.2 DC Characteristics

Measured Gummel characteristics: collector current (I_C) and base current (I_B) versus base-emitter voltage (V_{BE}) for different collector-emitter voltages (V_{CE}) are depicted in Fig. 2.8. While the current gain (I_C/I_B) remains stable, the substrate current (I_{sub}) is significantly increased at higher collector-emitter voltages. This indicates the influence of the parasitic substrate pnp transistor (emitter: base (npn HBT); base: collector (npn HBT); collector: p-substrate). Further process optimizations in the collector region of the npn transistor are necessary to decrease the current gain of the parasitic pnp transistor, resulting in a reduced substrate current. The output characteristic $I_C(V_{CE}, V_{BE})$ of the high-voltage npn transistor is depicted in Fig. 2.9(a). For a LDHBT array with a total emitter area A_E=88.2 µm^2 a collector current >30 mA is measured at V_{CE}=20 V and V_{BE}=0.85 V. The onset of the base current (I_B) reversal (depicted in Fig. 2.9(b)) from the output characteristic $I_C(V_{CE}, V_{BE}$=0.7 V) is used to determine the collector-emitter breakdown voltage (BV_{CEO}) of the LDHBT. With this method a BV_{CEO} >51 V is extracted. To determine the collector-base breakdown voltage (BV_{CBO}), the emitter is not contacted and the collector-base diode is biased in reverse mode. Thus, the emitter is floating at an undefined voltage. The resulting collector current (I_C) versus collector-base voltage (V_{CB}) is shown in Fig. 2.9(b). At a collector-base voltage greater than 56 V, the collector current is increasing significantly.



(a) (b)

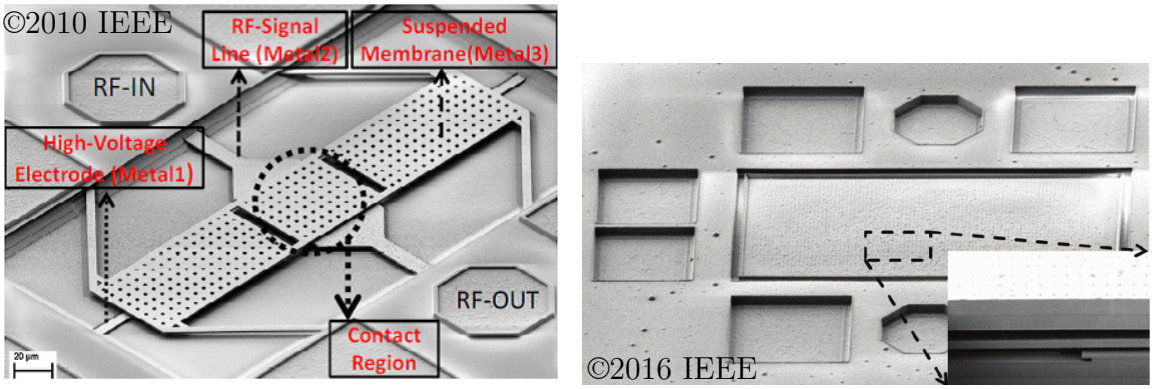
Figure 2.9: (a) LDHBT DC forward output characteristic (collector current (I_C) versus collector-emitter voltage (V_{CE}) and base-emitter voltage (V_{BE})) of an array consisting of 50 single HBTs resulting in a total A_E of 88.2 µm^2. (b) Measured breakdown voltages BV_{CEO} =51 V (base current (I_B) versus collector-emitter voltage (V_{CE}) and BV_{CBO}=56 V (collector current (I_C) versus collector-base voltage (V_{CB})) of a single LDHBT array of 50 single devices [50].

2.2.3 Conclusion

In this section, the process flow and the DC characteristics of an HV npn HBT, modularly integrated in a 0.25 µm SiGe BiCMOS technology, is described. According to the measured breakdown voltages (BV_{CBO} and BV_{CEO}) of the described HV-LDHBT it was estimated that the npn transistor is also suitable to be used as a high-voltage switch. Compared to the HV NLDMOS transistor described in [47] the high-frequency performance of the npn LDHBT [50] is inferior but superior compared to the combination of NLDMOS and PLDMOS transistor. Since the npn LDHBT is used in a DC switch matrix the, high-frequency parameters f_T and f_{Max} are less important. Thus, it is reasonable to design an experimental circuit based on the presented high-voltage bipolar transistor.

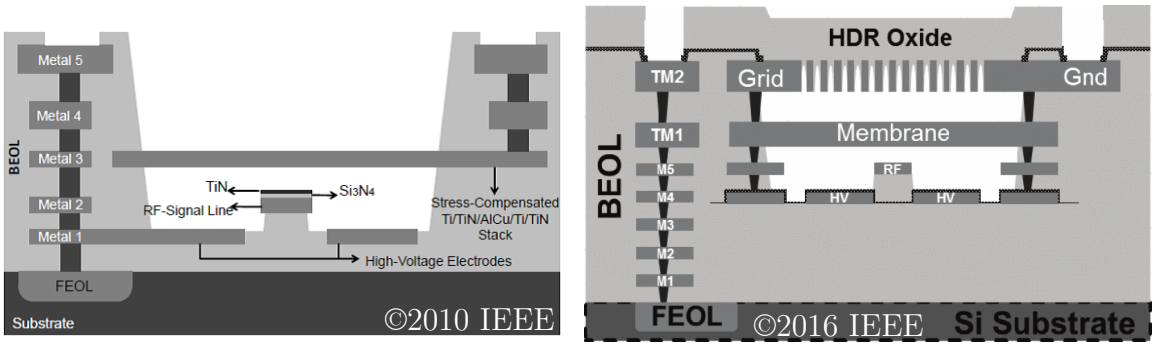
2.3 Embedded RF-MEMS Switch

Embedded RF-MEMS switches are part of the "More than Moore" strategy proposed by the international technology roadmap for semiconductors (ITRS) [53]. An overview of different processing approaches and how these mechanical devices can be embedded or combined with a CMOS or BiCMOS technology is given in [54]. One possibility is to use the existing BEOL metalization layers of the BiCMOS process. A few additional processing steps are required to release the movable part of the MEMS construction and for the encapsulation of the MEMS device.
In Fig. 2.10(a) and Fig. 2.10(b) Scanning electron microscopy (SEM) images of the SG25(a) and the 0.13 µm SiGe:C BiCMOS (SG13)(b) RF-MEMS switches are depicted. Due to the wafer level encapsulation (WLE) of the SG13 RF-MEMS switch, the movable membrane is covered. A Focused ion beam (FIB) cut is applied to enable a view into the cavity. These devices are optimized for frequencies starting from 30 GHz (SG25 [9], [41]) up to 240 GHz (SG13 [55], [56]). In general, these devices are variable capacitors with a fixed (RF signal line) and a movable (membrane) electrode. Since the fixed plate is the RF signal line and the movable second plate is connected to ground, the RF signal transmission can be modulated. As most of the RF-MEMS switches, the membrane is electrostatically actuated. The high actuation voltage is applied to dedicated electrodes adjacent to the RF signal line, minimizing the dielectric charging of the isolation layer deposited on top of the RF signal line. Therefore, stiction or latching of the RF-MEMS switch membrane due to dielectric charging is avoided. Additionally, dedicated high-voltage electrodes avoid the implementation of DC-blocks to protect the active circuits from the MEMS actuation voltage. Furthermore, the bandwidth of the RF-MEMS switch is not limited by the DC-blocks.



(a) (b)

Figure 2.10: SEM images of the (a) SG25 RF-MEMS switch [57] and (b) encapsulated SG13 RF-MEMS switch [10]. The cross-section in the lower right corner shows the etched cavity (released membrane) and the encapsulation.



(a) (b)

Figure 2.11: Cross-section of BEOL embedded (a) SG25 RF-MEMS switch [58] with the membrane realized in the metal 3 level and (b) SG13 RF-MEMS switch with wafer level encapsulation [10]. The high-voltage electrodes (HV) are in metal 4 (M4) layer while metal 5 (M5) is used for the RF signal line.

2.3.1 Process Integration

The RF-MEMS switches are integrated using the existing metalization layers of the BiCMOS technologies. Cross-sections of the 0.25 µm SiGe BiCMOS (SG25) and the 0.13 µm SiGe BiCMOS (SG13) RF-MEMS switches are shown in Fig. 2.11(a) and Fig. 2.11(b). The FEOL includes the bipolar, CMOS, LDMOS devices and polysilicon resistors. MIM capacitors, inductors and RF-MEMS switches are part of the BEOL. It should be noted that the RF-MEMS switch module does not affect the parameters of the FEOL transistors. Thus, the fabrication of the 0.25 µm FEOL is not described here but can be found in [46], section 2.2 and section 2.1.
A brief description of the 0.25 µm BEOL process comprising five metalization layers is given. The flow diagram is depicted in Fig. 2.12.
After the FEOL is processed, the first inter layer dielectric (ILD)-0 is deposited and patterned to define contact regions. The contact regions are filled with tungsten followed by the deposition of AlCu as the first metalization layer (metal1 (M1)). A thin layer of silicon nitride (Si_3N_4) is deposited on top of the RF-MEMS switch electrodes located in metal1 to define an etch stop layer (ESL). The ESL prevents under etching during the membrane-releasing step and avoids an electrical contact between electrode and membrane. This step was specifically introduced for the RF-MEMS switch module. After this, the next ILD-1 layer is deposited, structured and filled with tungsten to define the VIAs, followed by the deposition and structuring of metal2 (M2) to define the RF-MEMS switch RF signal line. To prevent an electrical and mechanical contact between the RF-MEMS switch RF signal line and the moving membrane and to define the contact capacitance, a further silicon nitride layer is deposited directly on the RF-MEMS switch signal line. This layer is also used as an insulation layer for the MIM capacitor. Subsequently, the next ILD-2 layer is deposited, structured and filled with tungsten to define VIA2, followed by the deposition and structuring of metal3 (M3) to define the RF-MEMS switch membrane. The fabrication of VIA3, metal4 (M4), VIA4 and metal5 (M5) is similar to the previously described metalization steps. After the final deposition of the passivation layer, areas including a RF-MEMS switch are defined using an additional mask. The movable membrane is released by removing firstly the passivation, by applying an etching process, followed by a further etching step to remove the silicon dioxide.
Applying an electrode voltage in the range of 20 – 40 V is sufficient to actuate the RF-MEMS switch implemented in the 0.25 µm process [9], [41]. For an increased

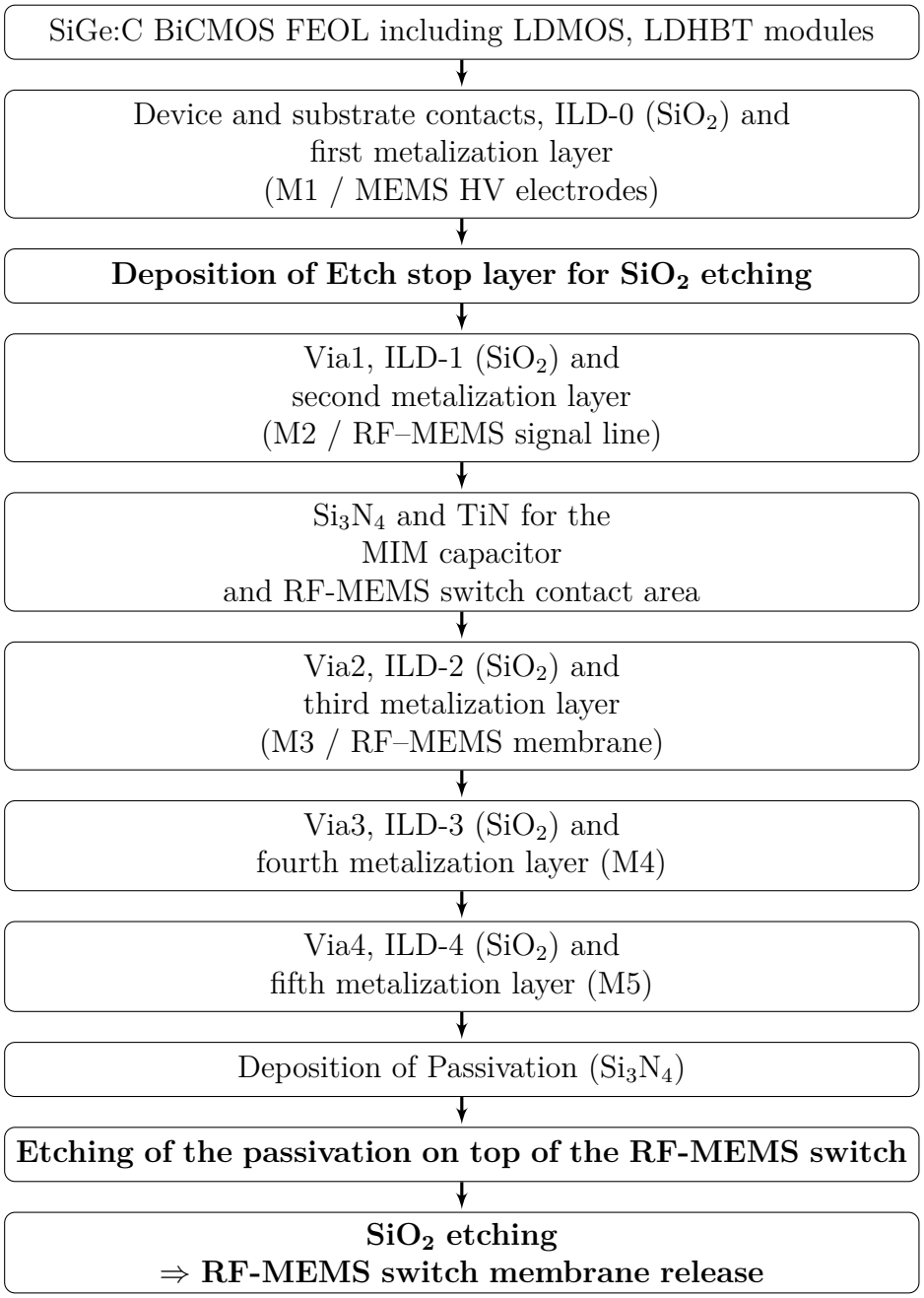


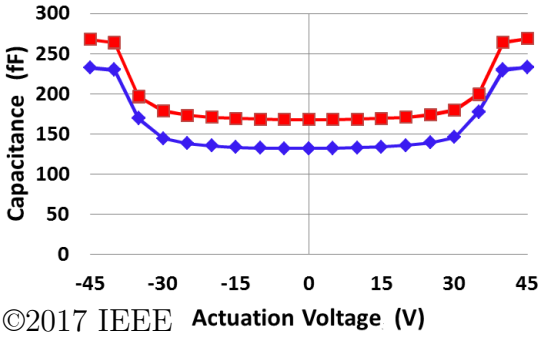
Figure 2.12: Process flow diagram of SG25 RF-MEMS switch. One additional mask is necessary for releasing the RF-MEMS switch membrane.

mechanical stability and a reduced oxide etching time (membrane release), the membrane of the SG13 RF-MEMS switch is realized in a thicker metalization layer (TM1 shown in Fig. 2.11(b)) - hence, the required actuation voltage is increased to 60 V [59]. The increased actuation voltage complicates the design of the on-chip charge pump and high-voltage switching circuitries. Therefore, high-voltage transistors and circuitries with higher operating voltages must be developed for the 0.13 µm technology.

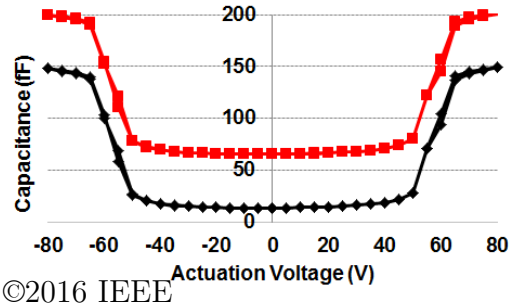
2.3.2 CV and RF Characteristics

In Fig. 2.13(a), the measured C-V characteristics of a single SG25 RF-MEMS switch [30] are depicted. The red trace shows the measured capacitance of the encapsulated RF-MEMS switch and the blue trace indicates the capacitance without silicon cap. For an electrode voltage greater than 30 V, the RF-MEMS switch membrane is electrostatically pulled towards the RF signal line. Resulting in an increased value for the measured capacitance. The closest membrane to signal distance (isolation-state) is obtained with an electrode voltage of 45 V. In Fig. 2.13(b) the measured C-V characteristics of an embedded SG13 RF-MEMS switch [10] is shown. The red trace shows the un-deembedded RF-MEMS switch contact capacitance (including the coupling of the RF signal line to the silicon substrate) and the black trace shows the deembedded RF-MEMS switch contact capacitance. Due to the larger electrode to membrane distance and the increased stiffness of the membrane, compared to the SG25 RF-MEMS switch, the pull-in (isolation-state) occures at approximately 50 V. The extracted RF-MEMS switch "up-state" (black trace, V = 0 V) capacitance is 13 fF and the average "down-state" capacitance is 149 fF, resulting in a down to up (C_{on}/C_{off}) ratio of 11.

The measured and simulated S_{21} for the isolation (down)- and transmission (up)-state of a SG25 RF-MEMS switch is shown in Fig. 2.14(a). In Fig. 2.14(b) the measured and simulated behavior for the isolation (S_{21})- and transmission (IL)-state of a 140 GHz SG13 RF-MEMS switch is depicted. The black trace is S_{21} and the blue trace $IL = 10 \cdot \log\left(|S_{21}|^2/(1-|S_{11}|^2)\right)$ considers the back-scattered RF signal (S_{11}).



(a)

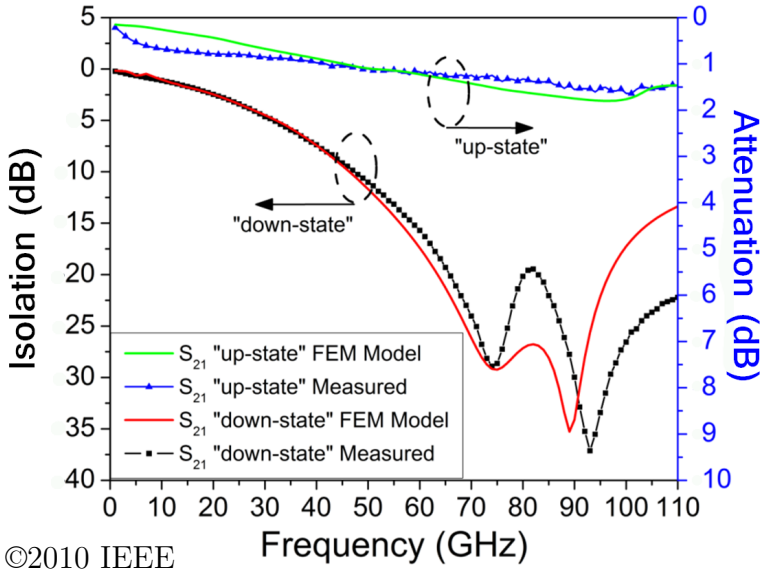


(b)

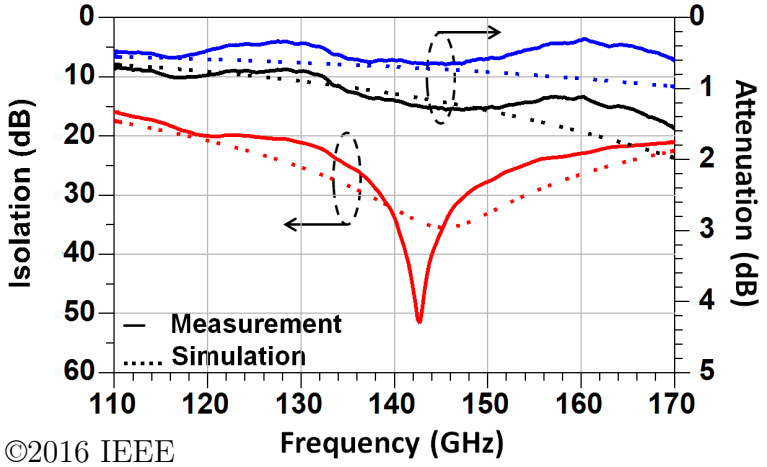
Figure 2.13: Measured C-V characteristics of a (a) SG25 RF-MEMS switch [30] (before (blue) and after (red) encapsulation) and (b) SG13 RF-MEMS switch. The measured capacitance (red trace) includes the signal line to substrate capacitance. The black trace shows the extracted RF-MEMS switch contact capacitance [10].

2.3.3 Conclusion

The process flow of the embedded RF-MEMS switch is described in this section. Measured C-V and Radio frequency (RF) characteristics are shown.



(a)



(b)

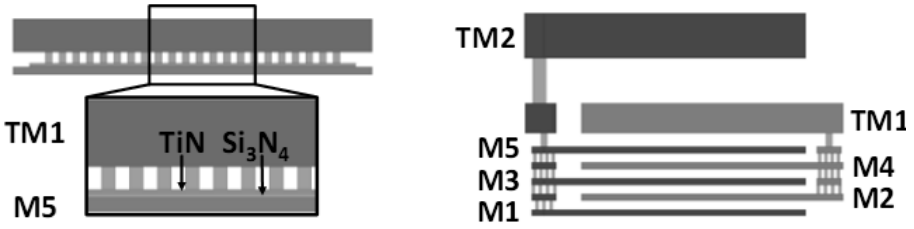
Figure 2.14: Measured and simulated isolation (down-state) and RF signal attenuation (up-state) (S_{21}) of embedded (a) SG25 RF-MEMS switch [58] and (b) SG13 RF-MEMS switch with wafer level encapsulation [10]. The blue trace $\left(\text{insertion loss}(IL) = 10 \cdot \log\left(|S_{21}|^2/(1-|S_{11}|^2)\right)\right)$ considers the reflected RF signal S_{11}.

3 High-Voltage Building Blocks

The high-voltage transistors described in section 2.2 and section 2.1 are the core elements in the on-chip HV switching units. In this chapter, the high-voltage building blocks: the high-voltage capacitors, the charge pump and the level shifter are described and analyzed.
Since the actuation voltage required by the embedded RF-MEMS switch exceeds the breakdown voltage of the available MIM capacitors, a high-voltage capacitor which employs the metallization layers of the BEOL is described in section 3.1. These capacitors are part of the HV generation circuitry (CP). Different on-chip CP topologies are described and analyzed in section 3.2. The CP must provide a stable output voltage for various load conditions. Furthermore, a second output voltage is required to bias the HV switching circuitry.
For controlling the HV PLDMOS transistor with its maximum gate-source voltage of 2.5 V, a level shifter circuit is required. Therefore, different level shifter (LS) circuitries are described and analyzed in section 3.3. A minimum DC current consumption is the major selection criteria, since the level shifter (LS) is powered by the integrated CP.

3.1 Integrated High-Voltage Capacitors

Since the voltage drop across the capacitors can exceed the breakdown limit in the charge pump and in the level shifter circuit, high-voltage capacitors are required. A serial combination of low-voltage BEOL MIM capacitors (cross-section depicted in Fig. 3.1(a)) will increase the maximum operating voltage with a decreasing total capacitance ($1/C_{tot} = \sum_1^n 1/C_n$). The operating voltage will be devided equally over identical sized capacitors ($V = \sum_1^n V_n$). By increasing the number of serial connected capacitors, the required chip area is also increased resulting in a decreasing capacitance per chip area ratio. In [60] a geometrically complex multi-metal capacitor with staggered "finger"-structure as a high-voltage capacitor is described. The electric field spreads vertically and horizontally, resulting in an inreased capacitance



(a) (b)

Figure 3.1: Cross-section of a (a) MIM and a (b) stacked metal capacitor [61].

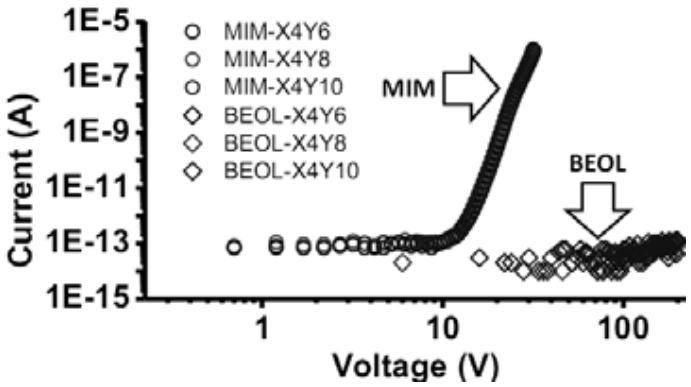


Figure 3.2: Measured leakage current of a MIM and a stacked metal capacitor (BEOL) [61].

per area ratio. Using the metallization of the BEOL, a parallel plate capacitor (cross-section is shown in Fig. 3.1(b)) is designed [61]. The thicknesses of the ILD layers between the different metal layers ranges from 0.55 – 2 µm. Therefore, the silicon dioxide (ILD-1) thickness of 0.55 µm between metal1 and metal2 limits the operating voltage. Since the distances between the metallization layers (electrode of the capacitor) are larger compared to the MIM capacitor, the breakdown voltage is increased at the cost of a decreased capacitance per area ratio from 1.5 fF/µm^2 (MIM) to 0.3 fF/µm^2. The aforementioned capacitance per area ratio includes a change of the dielectric constant of $\epsilon_r = 7$ for silicon nitride (Si_3N_4) and $\epsilon_r = 4.1$ for silicon dioxide (SiO_2). The dielectric strength of both materials is in the range of 10^7 V/cm. current versus voltage (I-V) measurements (depicted in Fig. 3.2) up to 200 V could not cause a breakdown of the stacked metal capacitor while a current of 1 µA @ 30 V is measured for a single MIM capacitor. Accepting a leakage current of 1 pA @ 100 V will result in a serial combination of 10 MIM capacitors. A charge pump based on the stacked metal approach (7 metalization layers) provides an output voltage up to 70 V [61].

3.2 On-Chip High-Voltage Charge Pumps

Depending on the availability of external high-voltage sources like 28 V or 50 V or even higher [62], [63] in satellite [64] applications or base stations [65] an, integrated high-voltage source is mandatory to drive the MEMS. The required output voltage of the integrated charge pump depends on the actuation voltage of the MEMS switch. In this work the target output voltage of the charge pump is in the range of 30–40 V. Independent from the circuit concept the most obvious parameter is the number of charge transfer stages (CTS) and the voltage gain per stage. There are various parameters which influence the output voltage of the charge pump shown in the symbolic equation 3.1.

$$V_{OUT} = f(CTS, clock, CP_{Load}, V_{IN}) \tag{3.1}$$

The output voltage (V_{OUT}) is not necessarily proportional to the clock frequency (f_{Clk}) and amplitude (V_{Clk}). In fact, the optimum clock frequency depends on the dimension of the capacitors used in the CTSs. A further important boundary condition is the targeted output power which depends on the load impedance (CP_{Load}) of the CP. Furthermore, the output voltage of the CP must not drop below the actuation voltage of the RF-MEMS switch for varying load impedances. The last parameter in the equation is the input voltage (V_{IN}) of the CP which is mostly connected to the bias supply. This input can be used to fine-tune the output voltage of the CP.

To minimize the modulation of the RF-MEMS switch membrane position which influences the capacitance, a low-voltage ripple on the charge pump output is necessary. On the other hand, this voltage ripple enables the usage of a capacitive voltage divider as feedback circuit to control the CP. Depending on the application, additional intermediate output voltages are necessary. In case of a HV switching matrix connected to the CP and driven by level shifters (described in section 3.3.3) a second output voltage (HS_V_{SS}) is required. To avoid the breakdown of the connected low voltage (LV) MOS transistors, the voltage offset ($HS\Delta$=V_{OUT} - HS_V_{SS}) must not exceed the BV_{GOx} and BV_{DS} of the LV MOS transistors.

In the next sections, three charge pump topologies are described and analyzed with regard to the following aspects:

- two-phase clock signal
- maximum output voltage (V_{OUT}) and load current
- additional output voltage (HS_V_{SS})
- ratio (HSΔ = V_{OUT} - HS_V_{SS} < BV_{GOx}) and voltage ripple
- compatibility with available process

3.2.1 Dickson Charge Pump

The schematics of a Dickson charge pump [66] is shown in 3.3. A differential clock signal (Clk, Clk_n) is required to drive the CP. The diode-connected low-voltage NMOS transistors must be placed in isolated p-well regions to avoid the breakdown of the NMOS transistors and to avoid an increased threshold voltage (V_{th}) due to the body effect with an increasing number of stages and output voltage.

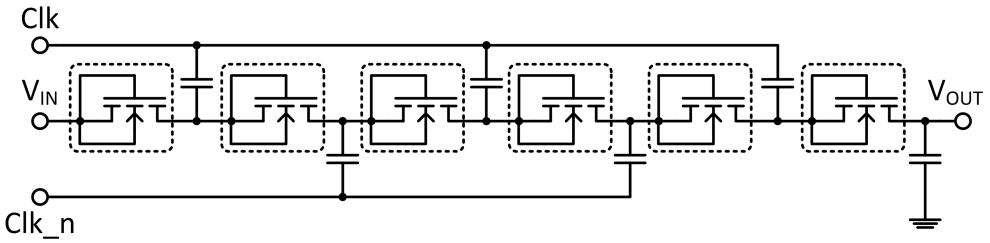


Figure 3.3: Six stage Dickson charge pump [66] using NMOS-based CTS. Low voltage MOS transistors must be placed in separated isolated p-wells (dashed line) to avoid the device breakdown and to avoid a modulation of V_{th} due to the body effect.

A parasitic capacitance to substrate (C_S) leads to a reduction of the voltage gain. BEOL MIM capacitors or stacked metal capacitors have a decreased substrate coupling compared to p-n junction capacitances. Thus, BEOL capacitors (section 3.1) are preferred even though they have a lower capacitance per area ratio.
A charge pump can be defined by an ideal voltage source (V_0) and a resistor (R_S). The generated output voltage (V_{OUT}) therefore depends on V_0 and the voltage drop across the stage resistance (R_S) caused by the load current (I_{OUT}) (equation 3.2). The equation 3.3 to calculate the generated voltage (V_0) for the Dickson CP is based

on [66]. If BEOL capacitors are used for the CP design, the C_S can be neglected. Thus, equation 3.3 can be simplified to estimate the generated voltage. The equivalent resistance (R_S) in equation 3.2 can be calculated using equation 3.4 or the simplified version assuming that $C \gg C_S$. Based on equation 3.5, the ripple (V_{rpl}) of the generated voltage is calculated. The load resistance (R_{Load}) represents the connected circuitries e.g. high-voltage switching circuitries. The higher the load current the faster the output capacitors (C_{OUT}) are discharged. Thus, the voltage ripple is increasing, which can be compensated by increasing the clock frequency (f_{Clk}). To estimate the number of stages (N) required for a defined output voltage (V_{OUT}) equation 3.3 can be rearranged resulting in equation 3.6.

$$V_{OUT} = V_0 - I_{OUT} \cdot R_S \tag{3.2}$$

$$\begin{aligned} V_0 &= V_{IN} - V_{th} + N\left[\left(\frac{C}{C + C_S}\right) \cdot V_{Clk} - V_{th}\right] \\ &\text{with } C \gg C_S \\ V_0 &\approx V_{IN} - V_{th} + N\left[V_{Clk} - V_{th}\right] \end{aligned} \tag{3.3}$$

$$\begin{aligned} R_S &= \frac{N}{(C + C_S)\, f_{Clk}} \\ &\text{with } C \gg C_S \\ R_S &\approx \frac{N}{C \cdot f_{Clk}} \end{aligned} \tag{3.4}$$

$$V_{rpl} = \frac{V_{OUT}}{f_{Clk} \cdot R_{Load} \cdot C_{OUT}} \tag{3.5}$$

$$N = \frac{V_0 - V_{IN} + V_{th}}{V_{Clk} - V_{th}} \tag{3.6}$$

These equations can also be applied for Dickson CP including the modified CTS described in [31]. The charge transfer stage (depicted in Fig. 3.4) is based on PMOS transistors.

To avoid the body effect (substrate bias or backgate effect) which changes the threshold voltage of the PMOS transistor, two additional PMOS transistors are integrated to adjust the body (n-well) voltage, resulting in a source-body voltage $V_{SB} \approx 0\,V$. Therefore, the threshold voltage V_{th} of the PMOS transistors in every stage remains

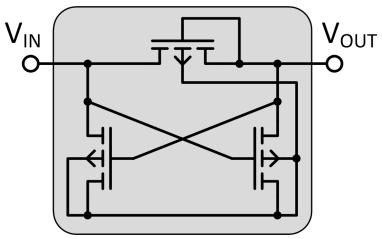


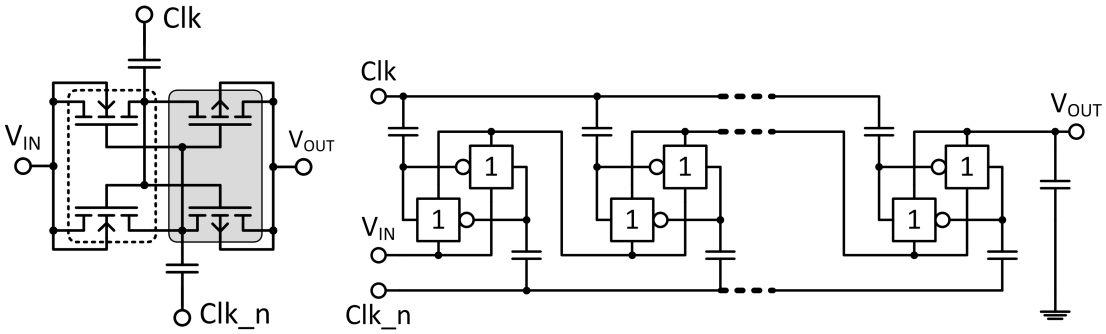
Figure 3.4: Modified Dickson CTS to adjust the threshold voltage (V_{th}) of the MOS transistor [31]. The PMOS transistors are placed in an n-well surrounded by a low doped p-region to increase the n-well to substrate breakdown voltage.

unchanged, resulting in a minimized voltage drop in each stage. Equation 3.7 can be used to calculate the effective threshold voltage (V_{th}) for an NMOS or PMOS transistor.

$$V_{th} = V_{th0} \pm \gamma \left(\sqrt{|2V_{fb}| + V_{SB}} - \sqrt{|2V_{fb}|} \right) \tag{3.7}$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_{A,D}}}{C_{Ox}} \tag{3.8}$$

The equation contains the Zero-bias threshold voltage (V_{th0}), the Source to body voltage (V_{SB}), the body effect coefficient (γ, equation 3.8) and the flat-band voltage (V_{fb}). Furthermore, the physical constants permittivity of silicon (ε_{Si}) and the elementary charge (q) are included. In [67], [68], a detailed analysis is provided and further examples are given considering this effect.



(a) (b)

Figure 3.5: (a) Single CTS latched CP described in [32] (the dashed line symbolizes an isolated p-well and the grey area indicates the n-well) and (b) schematics of a N-stage latched CP.

3.2.2 Latched Charge Pump

The schematics of a single CP stage is shown in Fig. 3.5(a). With its two cross coupled CMOS inverters, the topology of the CP is equal to a CMOS static random-access memory (SRAM) cell (latch). Hence, this topology is named as latched CP. A charge pump with three stages is described in [32]. An extended version is described in [19] where two charge pumps are combined. One CP is used to increase the voltage while the second is configured in reverse mode to decrease the output voltage. In this approach two independent clock generator circuits are implemented. Similarly to the Dickson CP, the latched CP requires capacitors with sufficiently high breakdown voltage. A difference to the Dickson CP is the need of two capacitors per stage. This fact causes also an increased sensitivity regarding the stray capacitance.
The generated output voltage (V_{OUT}) can be calculated using equation 3.9. The voltage gain per stage (ΔV) is multiplied by the number of stages and the input voltage (V_{IN}) is added.

$$V_{OUT} = V_{IN} + N \cdot \Delta V \tag{3.9}$$

The voltage gain (shown in equation 3.10) is proportional to the clock signal amplitude (V_{Clk}) and is reduced by the voltage drop caused by the equivalent stage resistance (R_S).

$$\Delta V = V_{Clk} \cdot \frac{C}{C + C_S} - R_S \cdot I_{OUT}$$
$$\text{with } C \gg C_S$$
$$\Delta V = V_{Clk} - R_S \cdot I_{OUT} \tag{3.10}$$

Equation 3.11 shows the dependence of the stage resistance on the clock frequency, stage capacitance and switch resistance (R_{switch}).

$$R_S = \frac{1}{f_{Clk} \cdot C} + R_{switch} \tag{3.11}$$

According to equation 3.12, the output voltage ripple (V_{rpl}) can be decreased by increasing the clock frequency (f_{Clk}). In [69] the concept of two parallel CPs biased with two anti-phase clock signals is mentioned to reduce the ripple of V_{OUT}. One drawback of this approach is the increased complexity of the CP circuitry. To keep the same chip size, the stage capacitance needs to be halved, resulting in an inferior stage capacitance to stray capacitance (C_S) ratio which will decrease the voltage gain per stage. Equation 3.13 can be used to estimate the number of stages (N) required for a defined output voltage (V_{OUT}).

$$V_{rpl} = \frac{V_{OUT}}{f_{Clk} \cdot R_{Load} \cdot C_{OUT}} \tag{3.12}$$

$$\text{with equation 3.9, 3.10 and 3.11}$$
$$N = \frac{V_{OUT} - V_{IN}}{V_{Clk} - (1/f_{Clk} \cdot C + R_{switch}) \cdot I_{OUT}} \tag{3.13}$$

3.2.3 Greinacher-Cockroft-Walton Charge Pump

The original concept presented in [70] and [71] is based on discrete components and was adapted in [72] to be used in microelectronic circuits. The Greinacher-Cockroft-Walton (GCW) CP is considered because of the relaxed conditions regarding the operating voltage for the capacitors. Therefore, stacking of MIM capacitors or bulky staggered finger backend capacitors are not needed, which results in a small layout size. Similar to the latched CP, each stage requires two capacitors. A single GCW CP stage is shown in Fig. 3.6(a) and in Fig. 3.6(b) a n-stage CP including the PMOS

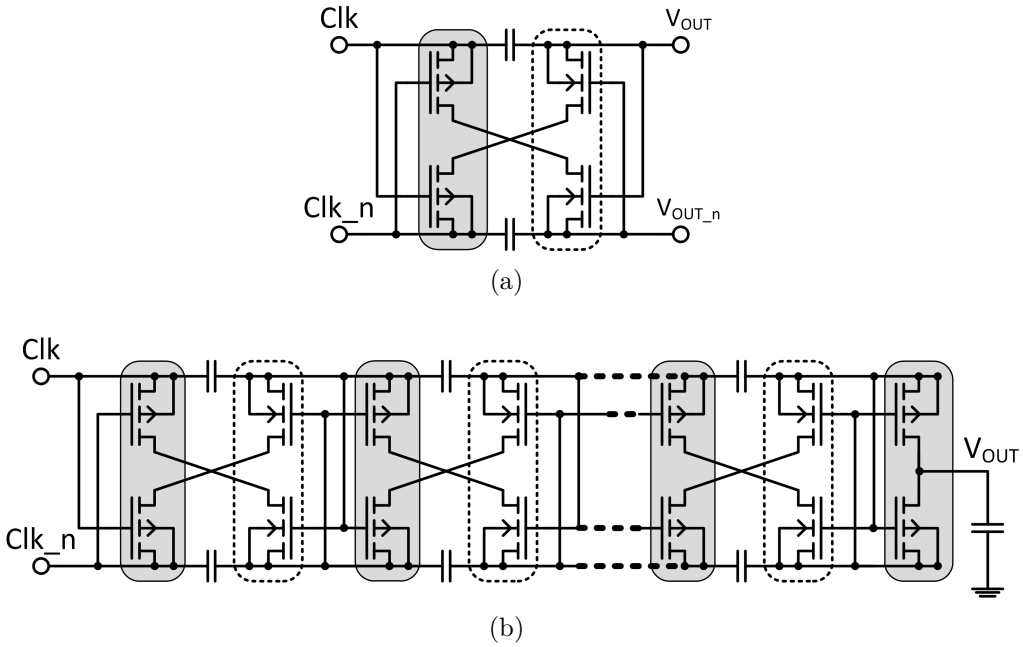


Figure 3.6: (a) Modified Greinacher-Cockroft-Walton charge transfer block for integrated circuit applications presented in [72] and (b) schematics with N stages including output stage and load capacitor (the dashed line symbolizes an isolated p-well and the gray area indicates the n-well).

output stage is depicted. The NMOS transistors are surrounded by a dashed line which symbolizes an isolated p-well and the gray area arround the PMOS transistors represents the n-well. A detailed description and measurement results of an integrated GCW charge pump can be found in [72]. According to [73], the Greinacher-Cockroft-Walton CP has a large voltage gain which reduces the number of stages (N) and capacitors, resulting in a minimized layout size. Since the CP is loaded by the MEMS Electrode capacitance and power efficient high-voltage inverters, the high output impedance (Z=f(N^3)) of the GCW must be considered during the design process. The following equations 3.14 and 3.15 were taken from [72].

$$V_{OUT} = (N+1)\,V_{DD} - \Delta V - \sum_{n=1}^{N} \frac{n \cdot I_{OUT}}{C_n \cdot f_{Clk}} \tag{3.14}$$

ΔV is the voltage loss caused by the stray capacitance (C_S) and increases exponentially with the number of stages. In the Dickson CP, the voltage loss due to stray capacitance is increasing linearly. The authors of [72] mention the usage of MIM capacitors located in the metallization of the BEOL to minimize the stray capaci-

tance and hence the voltage loss. Therefore the output voltage of the charge pump can be estimated as follows (equation 3.15).

$$\text{with } C \gg C_S$$
$$V_{OUT} = (N+1)\, V_{DD} - \sum_{n=1}^{N} \frac{n \cdot I_{OUT}}{C_n \cdot f_{Clk}} \tag{3.15}$$

3.2.4 Conclusion

The three analyzed CPs have advantages and disadvantages. In comparison to the latched CP, the modified Dickson CP based on PMOS transistors does not require a triple well process. Nevertheless, high-voltage capacitors are mandatory for both CP topologies. This is the advantage of the GCW CP, which does not require HV capacitors. On the other hand, the GCW charge pump has a higher output impedance. Therefore, the presented CPs are further analyzed and compared, based on circuit simulation results in section 4.2.1.

3.3 Integrated High-Voltage Level Shifter

Level shifter circuits are required to generate the high-voltage control signal (gate-source voltage) for the PLDMOS transistors which are part of the high-voltage inverter. The output voltage swing of the circuit must be adapted to the connected PLDMOS transistors with their low gate-source breakdown voltage (BV_{GS}). The major requirement for the design of a level shifter powered by an on-chip charge pump is to minimize the power consumption. If the level shifter is combined with a charge pump, the circuit must have a DC current leakage per HV node below 1 µA. Otherwise, the charge pump needs to be designed for higher output power levels, resulting in an increased layout area. Furthermore, the efficiency of the HV generation and switching circuitry is decreased.
Fast high-voltage level shifter topologies are also used in DC/DC converters. In contrast to the DC/DC converters where only a single but fast level shifter (LS) is needed, several compact and less complex LS are required in RF-MEMS control matrix applications. The authors of [74] present a rather complex level shifter with an average DC current leakage of 100 µA. In [75] a charge coupled level shifter (CCLS) is described with a current consumption below 1 µA. The drawback of this circuit is the need of an external 10 µF capacitor. The idea in [76] is similar to [75]: a capacitively coupled level shifter without off chip components. For HV switch matrix applications, a compromise between control circuit complexity, speed and power consumption needs to be found. In the following sections, various topologies are described and analyzed for their usability in combination with an on-chip charge pump. The main criteria for the level shifter circuit are shown with decreasing priority in the following list:

1. no off-chip components
2. low power consumption (permanent leakage current)
3. low circuit complexity
4. switching speed

3.3.1 DC Coupled Level Shifter

A simple high-voltage level shifter with negligible steady state current consumption and CMOS like operation is presented in [77]. The key components are PLDMOS transistors offering a BV_{GOx} as high as the bias voltage. Due to the thick gate oxide of the PLDMOS transistors, the switching rise and fall time of this approach is low. Another drawback is the availability of thick gate oxide PLDMOS transistors, since only thin gate oxide, as used for low-voltage MOS transistors, is available in the same process. Thick gate oxide PLDMOS transistors are not implemented in IHP's SiGe BiCMOS process.

The schematics of the most common used level shifter in DC/DC converter is shown in Fig. 3.7. The maximum current is limited by a current mirror and two PMOS transistors in diode configuration are used to set the high-side voltage swing. This topology has a constant steady state current, which is a big drawback for low power applications but can be limited with a current mirror. Using a current mirror, the high-side voltage swing will be reduced, which can be compensated using two PMOS transistors connected in diode configuration (enclosed in dashed line). Furthermore, the source potential of the not isolated NLDMOS transistors (M1, M2) is increased due to the current mirror and therefore the threshold voltage is influenced (body effect). The level shifter of [78] was realized in a SOI process which offers isolated high-voltage transistors. Another possibility is to design the circuit in a triple well process like [79]. In contrast to the aforementioned topologies, the circuits in [74] do not include a current mirror. This causes a high leakage current and cannot be used in conjunction with a low power charge pump.

A very fast level shifter using a comparator in the high-side is presented in [80]. Since one of the two branches is always conductive, a constant static current is drawn from the power supply. The fast 50 V level shifter is designed for a DC/DC buck converter and has a current consumption of 300 µA. This current consumption needs to be scaled by a factor of 100 to be in a usable range for a RF-MEMS control matrix. Therefore, this circuit cannot be combined with a low power charge pump.

3.3.2 Pulse-Triggered Level Shifter

Instead of applying a constant control signal, only short pulses are applied to change the output state of the pulse-triggered level shifter. Using a pulsed control signal will significantly reduce the current consumption of the level shifter. The advantage

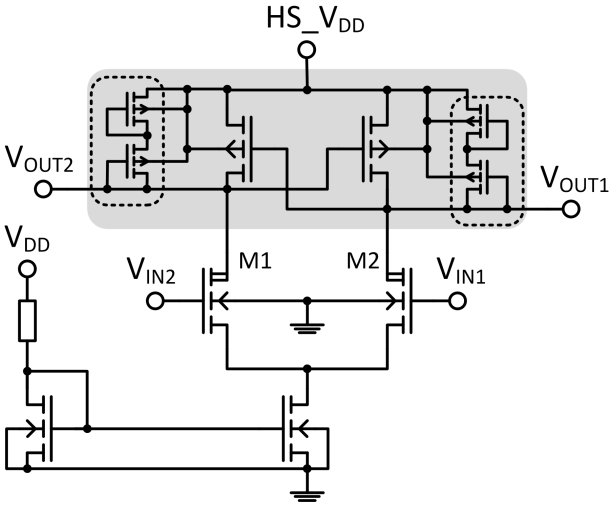


Figure 3.7: Conventional level shifter with NLDMOS (M1,2) to switch the high voltage. The current is limited with a current mirror. To set the output voltage swing two PMOS transistors in diode configuration (enclosed in dashed line) are used. The gray area symbolizes the N-well.

is a reduced steady state current with the need of a pulse generation circuitry and a memory element to store the output state. In [81], a high-voltage driver for 80 x 104 bistable matrix Liquid crystal display (LCD) was developed. The level shifter depends on the capacitor as a memory element and can be used if the load impedance is very high. An output buffer is required for low-ohmic loads to prevent the discharging of the memory capacitor. In [76] a pulse-triggered level shifter with very low static current is described. To store the output state of the level shifter a RS flip flop is implemented. The high-side includes Zener diodes which are often not available as an integrated device. As described in [82], the circuit shown in Fig. 3.7 can be controlled with a pulsed complementary control signal at (In1, 2). The functionality of the level shifter is like [81] and depends on the capacitor as a memory element. The switching speed is dependent on the charging and discharging time of the memory- and load capacitance. This concept was used in a high-voltage driver matrix with 160 outputs as a driving circuit for Liquid powder displays (LPDs). Limiting the current to the µA range which can be provided by the charge pump will reduce the output signal amplitude. The schematic of a pulse-triggered level shifter presented in [83] is depicted in Fig. 3.8. The circuit employs NLDMOS transistors to bridge the voltage gap between high-side and low-side part. Since the gate of the NLDMOS transistor is connected to V_{DD}, the transistor is always conductive. The source follower operation of M5,6 causes a minimum voltage swing at the drain

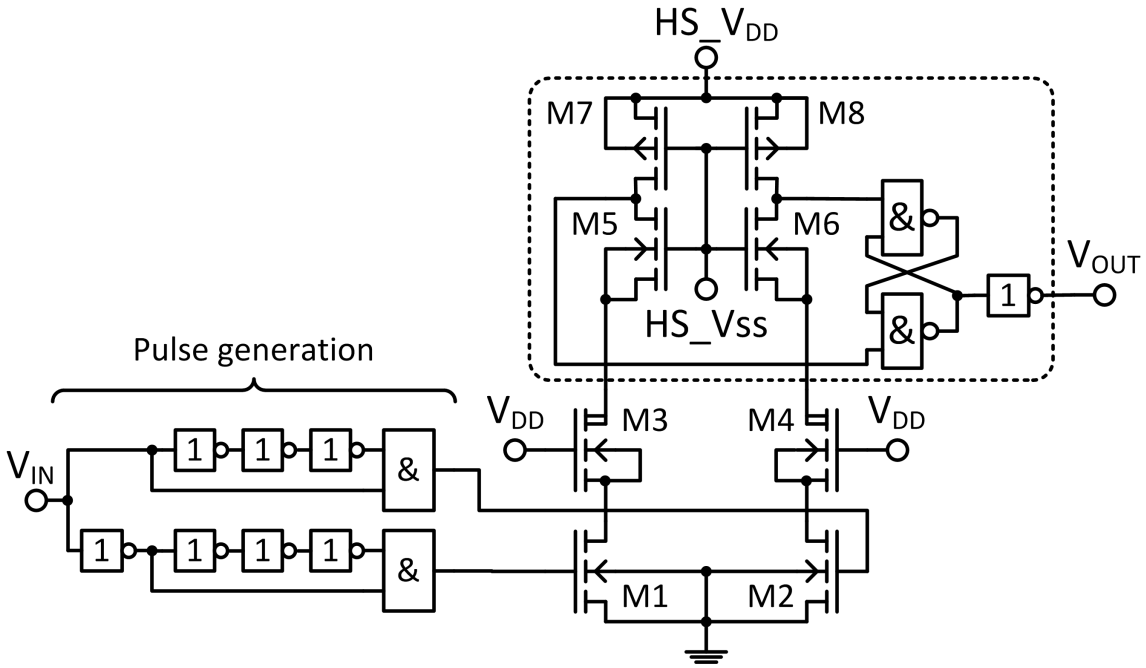


Figure 3.8: Pulse-triggered level shifter presented in [83]. An NLDMOS transistor is introduced to isolate the high-side (dashed line) part from the low-side.

of M3,4, improving the speed by minimizing the transferred charge in the drain of M3,4. In [84] a 50 V pulse triggered level shifter including high-side latch is described. MOS transistors with various breakdown voltages (BV_{GOx}/BV_{DS}) are used, which limits the possible technologies to realize this circuitry.

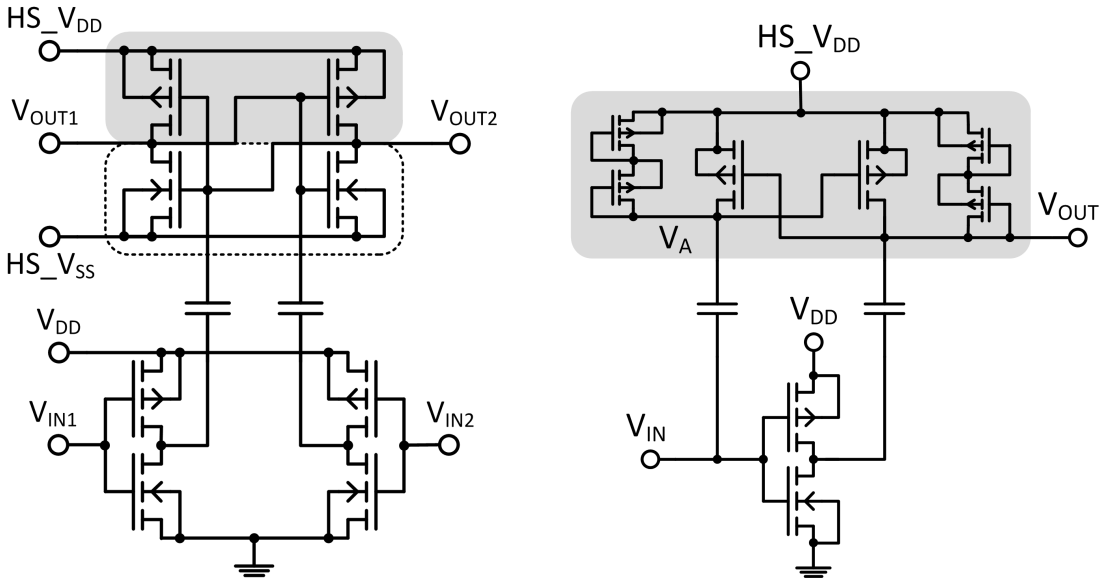


Figure 3.9: Circuit diagram of capacitively coupled level shifter equivalent to (a) [78], [85] and (b) [86]. The capacitors isolate the low-voltage part from the high-voltage part. The dashed line symbolizes an isolated p-well and the gray area indicates the n-well.

3.3.3 Capacitively Coupled Level Shifter

In [85] a capacitively decoupled LS topology for negative voltages is proposed. The advantage of this approach is the suppressed steady state current due to the introduced capacitors and the isolation of two different voltage domains from each other. The maximum voltage depends on the breakdown voltage of the capacitors and can be easily multiplied by connecting multiple capacitors in series. Depending on the operating voltages, the high-side transistors have to be isolated from the p-substrate (low-side) by either using a SOI process [76] or applying a junction isolation. Thus, high-voltage transistors are not required for this level shifter circuit. To minimize the charging and discharging time which reduces the switching speed of the level shifter, the size of the coupling capacitor should be minimized. A similar topology for positive voltages is described in [76], [86]. The equation 3.18 from [86] defines the capacitance of the coupling capacitors as a multiple of the gate capacitance (C_G) of the high-side MOS transistor. The calculation is based on charge conservation. The blocking capacitors provide the charge (Q) required to switch the high-side

transistors.

$$\Delta Q = \Delta Q_G \tag{3.16}$$

$$C \cdot (V_A - HS\_V_{DD} + V_{DD}) = C_G \cdot (HS\_V_{DD} - V_A) \tag{3.17}$$

$$\text{with} \qquad V_A = HS\_V_{DD} - 2V_{th}$$

$$C = C_G \frac{2V_{th}}{V_{DD} - 2V_{th}} \tag{3.18}$$

A narrow gate width should be chosen to minimize the size of the coupling capacitors. In [76] (equation 3.19) the capacitance of the coupling capacitors is related to the maximum drain current ($I_{D,max}$) of a high-side transistor in a certain time period e.g. rise or fall time ($\tau_{R,F}$).

$$C = \frac{Q}{V} = \frac{I_{D,max} \cdot \tau_{R,F}}{V_{DD}/2} = \frac{\beta \left(V_{DD} - V_{th}\right)^2 \tau_{R,F}}{3 \cdot V_{DD}} \tag{3.19}$$

with

$$\beta = \mu_n C_{Ox} \frac{W}{L} \qquad ; V_{DD} = HS\_V_{DD} - HS\_V_{SS}$$

The transconductance parameter β of an NMOS transistor is calculated using the electron mobility μ_n, the oxide capacitance C_{Ox} and the ratio between gate width (W) and length (L).
Since the two branches in the level shifter circuit are designed symmetrically, the state of the high-side is unknown after power on. Therefore, an initial switching is mandatory. To avoid this uncertainty, the authors of [75] describe an asymmetrical approach. When switching on, an additional circuitry is required to charge an off-chip coupling capacitor.

3.3.4 Conclusion

The permanent DC current in a DC coupled high-voltage level shifter can be minimized but it cannot be avoided when using a current mirror. Therefore, this topology is not suited to be driven by a low-power CP.
Pulse-triggered level shifters are also DC coupled LSs. A memory cell to store the output state and a set/reset pulse generation circuitry is required. Since the circuit is controlled with pulses, the current consumption depends on the control signal slew rate, pulse width and frequency.
Like the pulse-triggered level shifters, the capacitively coupled level shifter offers a very low steady state leakage current but can be realized without LDMOS transistors. The voltage offset is blocked by capacitors instead of using NLDMOS transistors. Depending on the voltage offset, multiple MIM capacitors must be connected in series, which causes an increased chip area. The circuit complexity of the capacitively coupled level shifter is comparable with the pulse controlled LS.

4 High-Voltage Generation and Switching Circuits

In this chapter the realized HV generation and switching circuitries are described and their measured performance is presented. Firstly, the designed differential oscillator circuit is presented in section 4.1. The oscillator generates a complementary clock signal which is required to drive the integrated CP.
Based on circuit simulation results, the three different CP topologies desribed in section 3.2 are compared. As a result of these comparative simulations, a modified Dickson type charge pump is designed. The realized CP (section 4.2) provides the actuation voltage for the RF-MEMS switches and the operating voltage for the HV switching circuitry.
In section 4.3, a simple high-voltage switching circuit is presented, using the npn LDHBT transistor (described in section 2.2). An alternative high-voltage switching circuitry, comprising the HV LDMOS transistors (section 2.1), is described in section 4.4.

4.1 Differential Oscillator

All CPs described in section 3.2 require a differential clock signal. Figure 4.1 shows the schematics of a basic ring oscillator (RO) built of inverter stages and additional output stages to provide a complementary output signal (V_{OUT_p}, V_{OUT_n}).

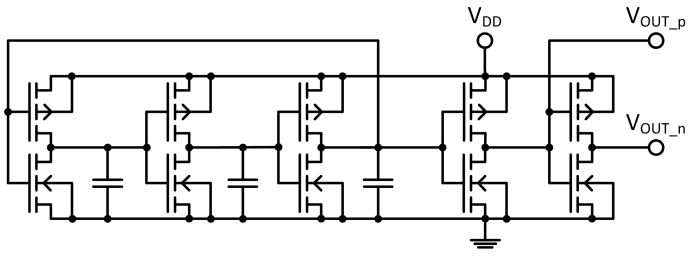


Figure 4.1: Basic ring oscillator with complementary output signal.

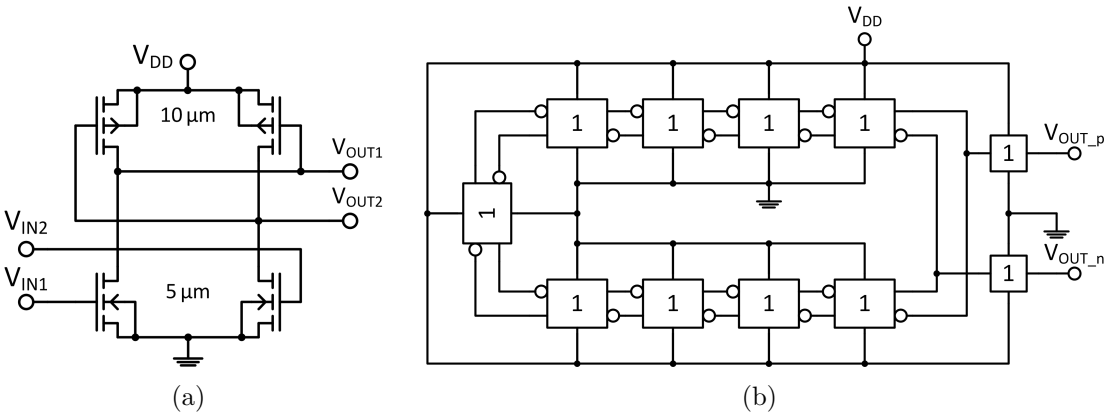
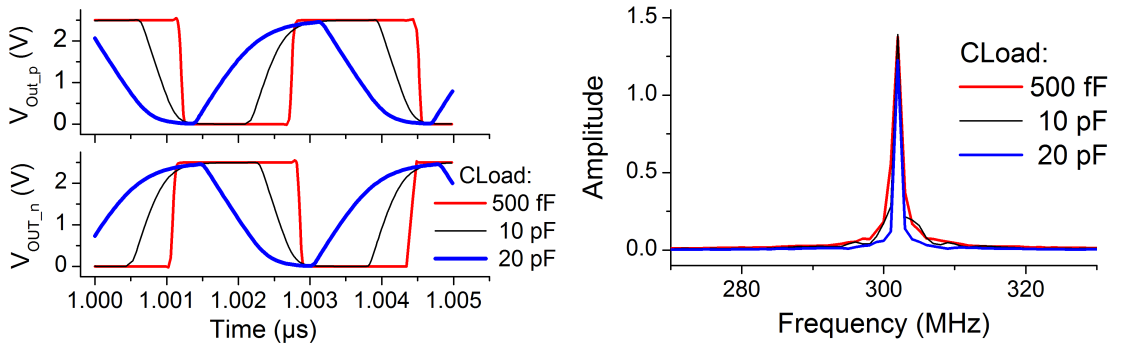


Figure 4.2: (a) Schematics of differential DCVSL inverter stage and (b) RO based on the inverter including buffer stage.

The generated frequency ($f = 1/(2\tau \cdot N)$) depends on the delay time (τ) of a single stage and the number of stages (N) where N must be an odd number. The oscillation frequency can be influenced by the introduction of load capacitors between the stages as shown in Fig. 4.1. Another approach to control the oscillation frequency is used in the "current starved ring RO". In this topology, the current of every stage is controlled using a current mirror. Increasing the current results in an increased oscillation frequency and vice versa.

To operate the CP at optimum efficiency, a non-overlapping differential clock signal is required while the phase noise and stability of the voltage controlled oscillator (VCO) is less important. The signal output V_{OUT_n} in Fig. 4.1 has a time shift according to the delay of the last inverter stage, which will decrease the efficiency of the CP. Therefore, the inverter stages are designed based on differential cascode voltage switch logic (DCVSL) depicted in Fig. 4.2(a). The target oscillation frequency is defined as 300 MHz, since the CP described later on (section 4.2) is optimized for this frequency. An important parameter to adjust the center frequency is the gate width of the PMOS transistor. An increased gate width results in a decreased oscillation frequency.

In Fig. 4.2(b), the schematics of the designed differential nine stage ring oscillator with output buffer is depicted. The output buffer is implemented as cascade of three CMOS inverter stages to drive the CP. The gate width of the NMOS / PMOS transistor in the last stage is 100 µm / 200 µm, strong enough to charge the capacitance of the CP. Transient simulation data for different load capacitance is depicted in Fig. 4.3(a). The slew rate of the output signal is decreasing with increasing load im-



(a) (b)

Figure 4.3: Transient simulation results: a) transient output voltages b) calculated oscillation frequency of the differential RO including buffer stages for different capacitive load conditions.

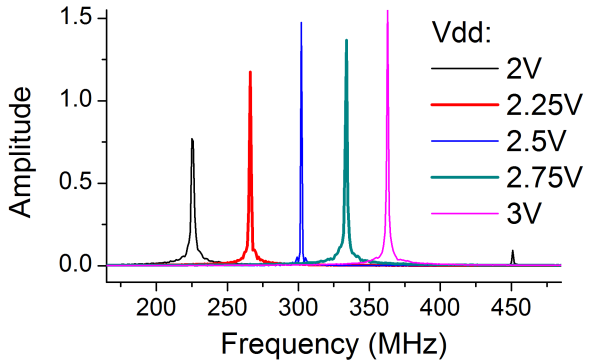


Figure 4.4: Simulated oscillation frequency of the differential DCVSL RO including buffer stages for different bias conditions (V_{DD}). The frequency spectrum is calculated using the ADS^{TM} time to frequency function (fs).

pedance while the oscillation frequency remains stable (Fig. 4.3(b)). For the 500 fF load condition, the "on-time" period is longer than the "off-time" period, which causes a short overlap of V_{OUT_n} and V_{Out_p}. Since the load capacitance caused by the CP is in the range of 20 pF, the slew rate is decreased, resulting in a decreased signal overlap.

In Fig. 4.4 the oscillation frequency of the designed DCVSL RO versus bias voltage is depicted. With increasing supply voltage (V_{DD}) the frequency and signal amplitude are increasing which, can be used to adjust the generated output voltage of the CP.

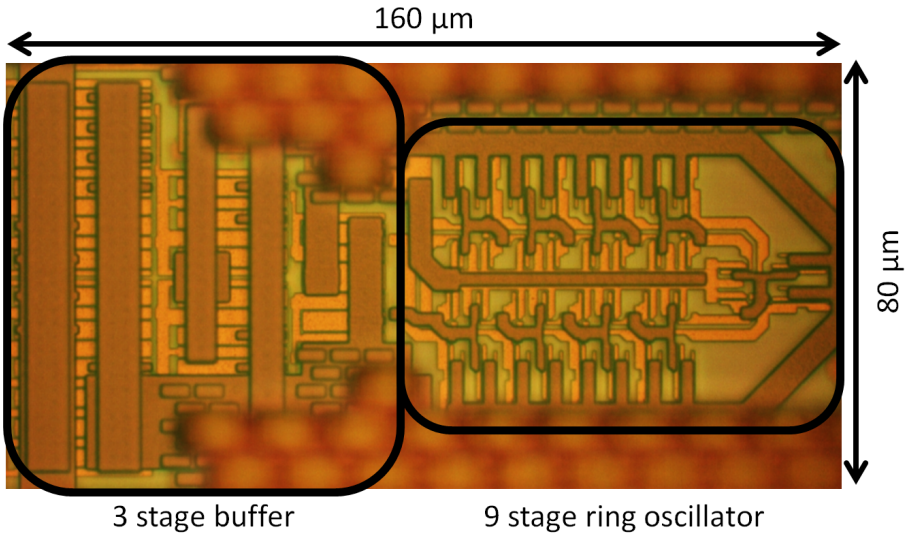


Figure 4.5: Chip micrograph of differential 9 stage ring oscillator including a 3 stage buffer.

A chip micrograph of the designed ring oscillator and additional output buffer is depicted in Fig. 4.5. Without bondpads, the chip size of the RO is only 160 µm x 80 µm.

The functionality of the realized ring oscillator is tested indirectly by measuring the generated output voltage of the driven charge pump. The generated CP output voltage depending on the applied voltage (V_{DD}) is depicted in section 4.2.2 Fig. 4.21.

4.2 Charge Pump for On-chip High-Voltage Generation

4.2.1 Comparative Circuit Simulations for Various Charge Pump Topologies

To compare the different topologies described in section 3.2, transient simulations are performed in Keysight advanced design system (ADS^{TM}) using a SG25 process design kit including Penn State-Philips surface potential MOS compact models (PSPs) for the MOS transistors. The biasing conditions (input voltage, clock frequency and amplitude) are the same for all topologies. To achieve an output voltage (V_{OUT} = HS_V_{DD}) in the range of 30 V, the number of stages and the capacitors of each stage were designed accordingly. For the HV switch driving circuitry, a second decreased output voltage (HS_V_{SS}) with an offset (HSΔ = HS_V_{DD} - HS_V_{SS}) less than the BV_{GS} and BV_{DS} is required to bias the low voltage CMOS transistors integrated in the level shifter circuit. Connecting a resistive voltage divider at the output of the CP will provide a second output. The drawback of the resistive divider network is the additional permanent leakage current which needs to be provided by the CP. Thus, the output voltage of a previous stage (N-1 or N-2) of the described charge pumps is analyzed regarding offset voltage and voltage ripple.
The clock frequency is 300 MHz and the amplitude is set to 2.7 V for all simulations. Since the Greinacher-Cockroft-Walton CP has no additional DC input, the input voltage (V_{IN}) of the Dickson (Fig. 3.3) and the latched (Fig. 3.5(b)) CP are set to 0 V. Different load conditions ranging from 10 GΩ (unloaded) down to 50 kΩ while the load capacitance is kept at 1.7 pF are simulated to compare the charge pumps. The simulation setup for the modified Dickson type CP is depicted in Fig. 4.6. 20 stages are sufficient to achieve 32 V (HS_V_{DD}) with the Dickson type CP. For the first 10 stages, the capacitance is set to 1.5 pF and the remaining 10 stages are set to 0.75 pF. A relative voltage drop of 13 % is simulated (depicted in Fig. 4.7(a)) if both outputs HS_V_{DD} and HS_V_{SS} are terminated with a 1 MΩ resistor compared to the unloaded condition, which is represented by a 10 GΩ load resistor. An important design parameter, required to bias the level shifter, is the voltage offset (HSΔ) and a low ripple of HSΔ. For the high-impedance condition (10 GΩ), the simulated voltage offset is 2 V with a ripple of 48 mV (see Fig. 4.7(b)). An important difference compared to the schematics shown in Fig. 3.3 is the connection of the clock signal

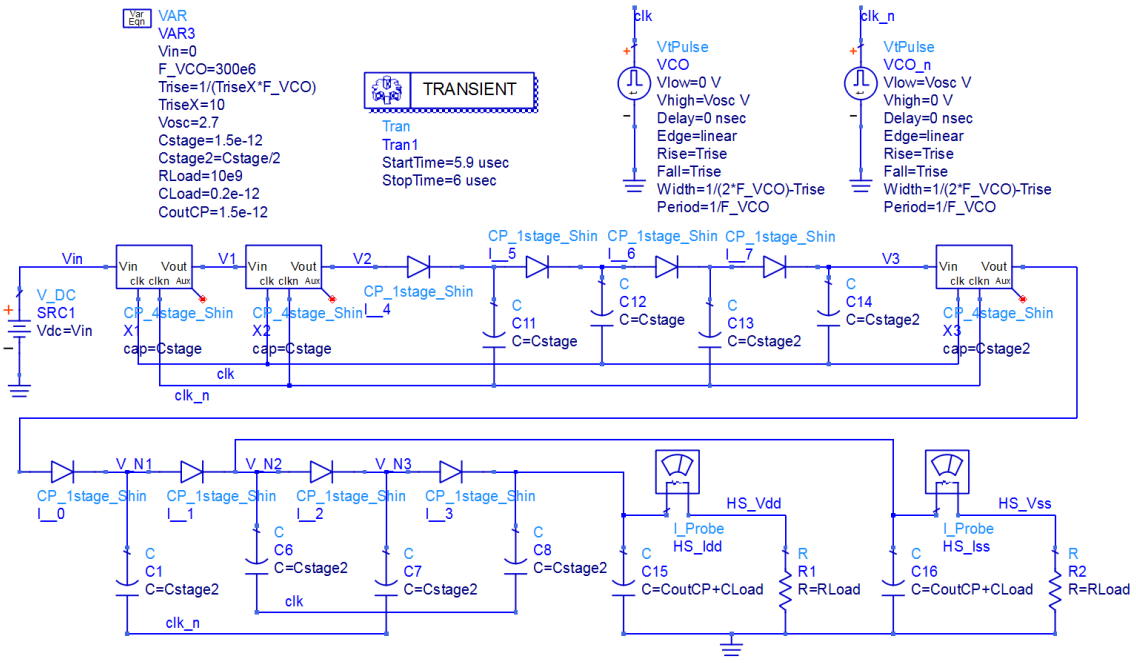
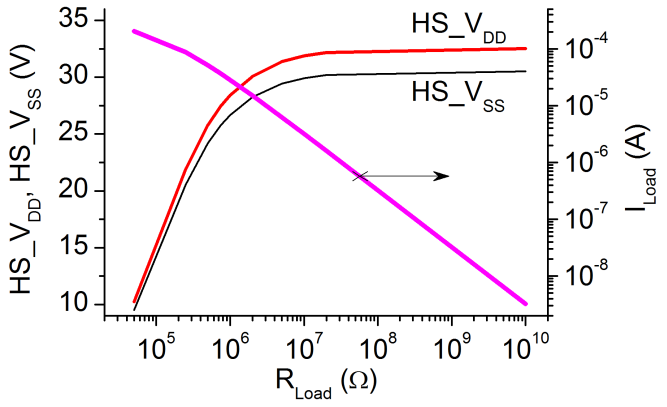
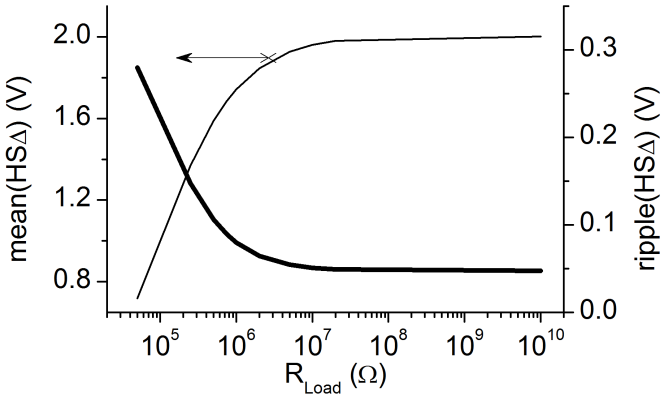


Figure 4.6: Simulation setup in ADS^{TM} for the Dickson CP including PMOS transistor based CTSs. The schematics of a single stage is shown in Fig. 3.4.

to the output of the CP. This will synchronize both output voltages HS_V_{DD} and HS_V_{SS}, resulting in an increased voltage ripple of HS_V_{DD} but decreases the voltage ripple of HSΔ significantly. The ramp-up time of the Dickson CP depends on the loading condition and is in the range of 5 µs, which is in the range of the RF-MEMS switching time. Compared to the latched and the GCW CP, the Dickson topology offers the lowest voltage gain per stage of 1.6 V. The layout area required is comparable to the latched CP.



(a)



(b)

Figure 4.7: Simulated output voltages and current (I_{Load}) as a function of the load resistance (R_{Load}) of a modified Dickson CP. (a) CP output voltage (mean(HS_V_{DD})) and second output (mean(HS_V_{SS})) (b) voltage offset (HSΔ) between the CP output voltage (HS_V_{DD}) and the second output voltage (HS_V_{SS}) and voltage ripple of HSΔ.

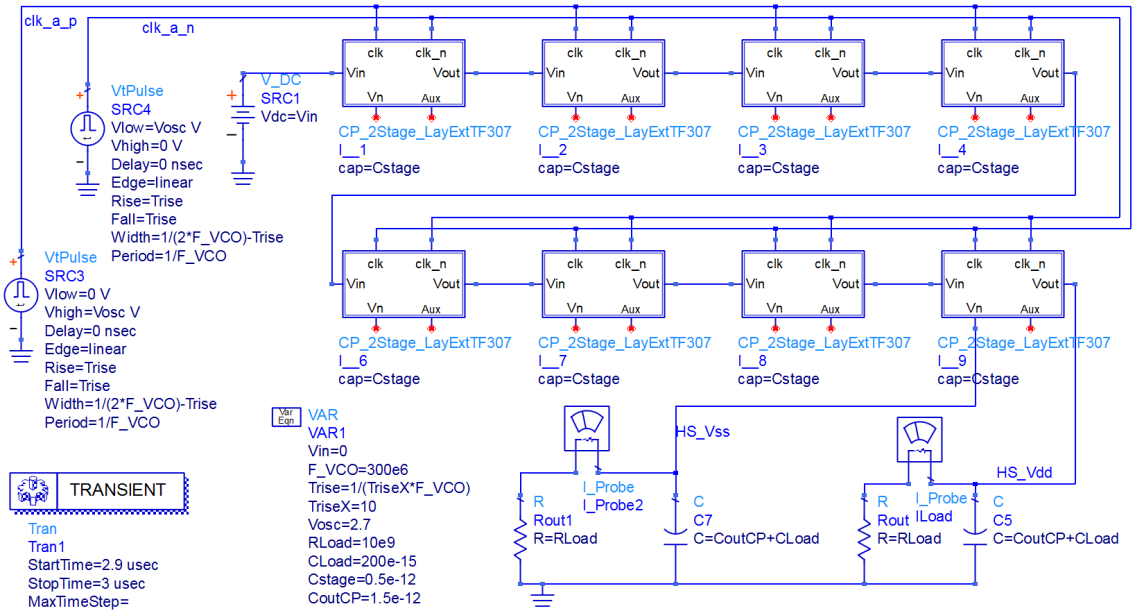
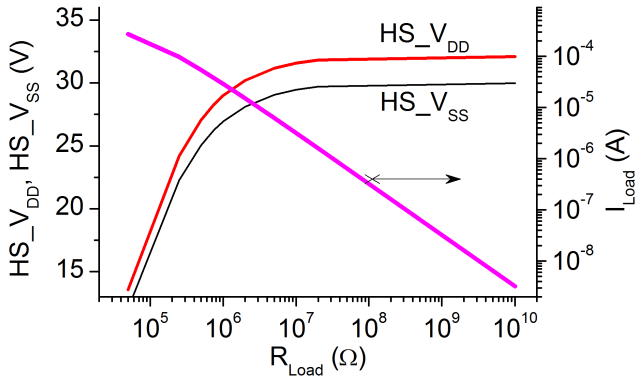


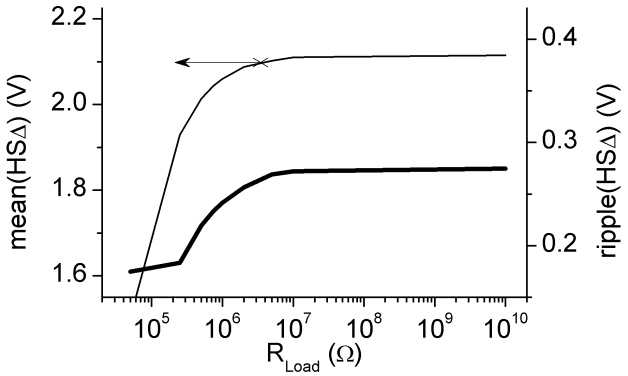
Figure 4.8: Simulation setup in ADS^{TM} for the latched CP. The schematics of a single stage is shown in Fig. 3.5(a).

The simulation setup for the latched CP is depicted in Fig. 4.8. According to circuit simulations, the latched charge pump has a voltage gain of 2 V per stage. A cascade of 16 stages comprising 32 capacitors (500 fF) is sufficient to achieve an output voltage of 32 V. Even though two capacitors per stage are required in this topology, the smaller stage capacitance and the decreased number of stages result in a similar chip size compared to the Dickson CP.

The circuit offers a halved ramp-up time compared to the Dickson CP due to the decreased capacitance. The latched CP is best suited to operate in direct combination with a single MEMS switch applied in the demonstrator circuit described in section 5.1.1. Circuit simulations show a very good current source capability of this CP resulting in a 10 % voltage drop with a R_{Load}=1 MΩ compared to R_{Load}=10 GΩ. The only drawback of this charge pump is the high ripple of HSΔ which causes permanent charging / discharging currents and a fluctuation of the bias voltage for the level shifter circuitry. The output synchronization used for the Dickson CP is not applicable, since the circuit nodes for the clock signal and the stage output of the latched CTS are different. In [69] the concept of two parallel CPs biased with anti-phase clock signals is mentioned to reduce the voltage ripple of V_{OUT}. To achieve a similar chip size, the stage capacitance needs to be halved, resulting in an inferior stage to stray capacitance (C_S) ratio, which will decrease the voltage gain per stage.



(a)



(b)

Figure 4.9: Simulated output voltages and current (I_{Load}) as a function of the load resistance (R_{Load}) of a latched CP. (a) CP output voltage (mean(HS_V_{DD})) and second output (mean(HS_V_{SS})) (b) offset voltage (HSΔ) between the CP output voltage (HS_V_{DD}) and the second output voltage (HS_V_{SS}) and voltage ripple of HSΔ.

Transient circuit simulation results of this concept do not show a decreased voltage ripple of V_{OUT} and HSΔ. Furthermore, the output voltage compared to Fig. 4.9 is decreased.

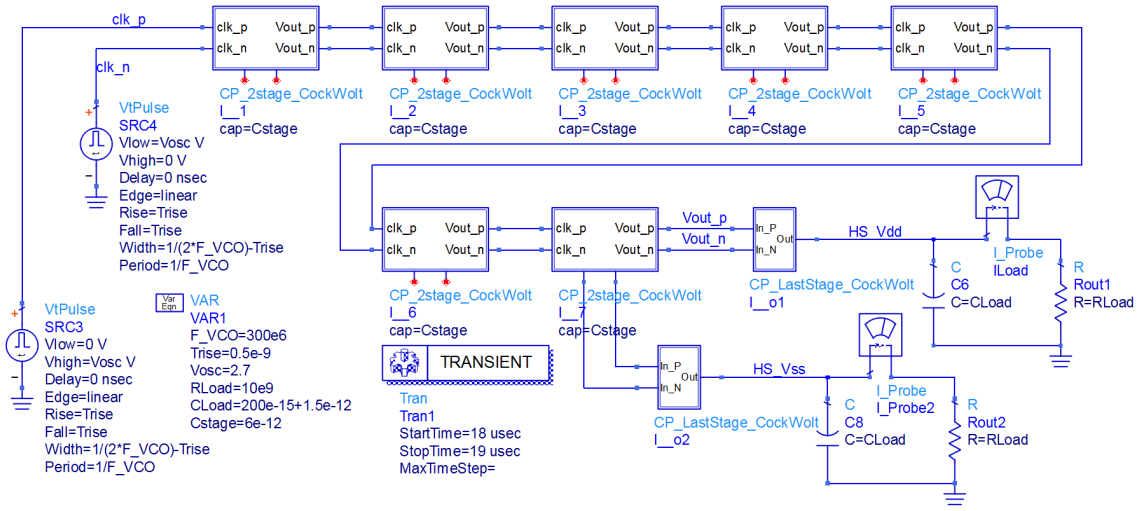
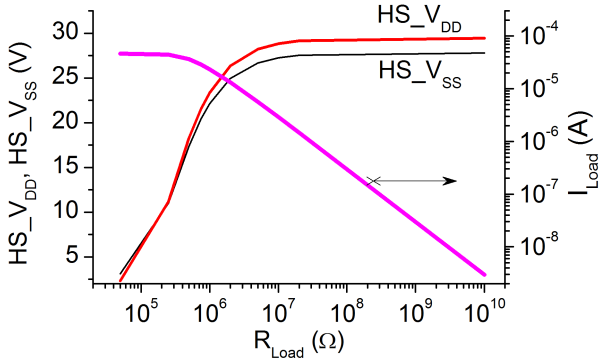


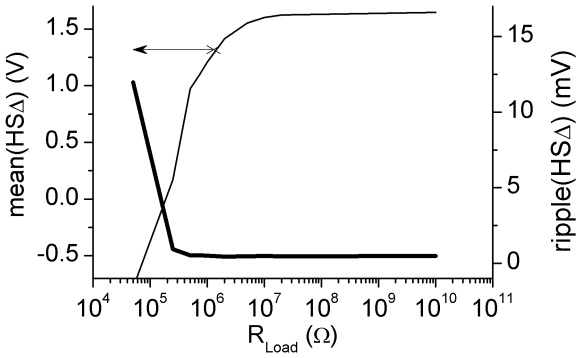
Figure 4.10: Simulation setup in ADS^{TM} for the GCW CP. The schematics of a single stage is shown in Fig. 3.6(a).

The simulation setup for the GCW CP is depicted in Fig. 4.10. The advantage of the GCW CP is the very low ripple in the generated output voltages and it is best suited for MEMS based VCOs, since small changes in the MEMS capacitance due to the ripple of the CP will affect the phase noise of the VCO. A difference of the GCW topology is the lack of an additional DC input like Dickson or latched CP. The GCW topology has fewer stages with very large stage capacitors, resulting in a doubled chip size compared to the Dickson and latched CP.

By increasing the number of stages the gain per stage is decreasing. Nevertheless, a high-voltage gain of 2.1 V per stage is simulated for a 14 stage charge pump. The ramp-up time is increasing with the number of stages and stage capacitance, resulting in a significantly higher ramp-up time (approx. 20 times) compared to the Dickson CP. The biggest drawback of this topology is the 20 % voltage drop if both outputs (HS_V_{DD} and HS_V_{SS}) are terminated with a 1 MΩ resistor. Even with an increasing number of stages the generated output voltage is decreasing for R_{Load}=1 MΩ (depicted in Fig. 4.12). Therefore, the GCW CP could be combined with a single MEMS but is not suitable in conjunction with a high-voltage switch matrix with a power consumption in the range of 20 µA.



(a)



(b)

Figure 4.11: Simulated output voltages and current (I_{Load}) as a function of the load resistance (R_{Load}) of a Greinacher-Cockroft-Walton CP [72]. (a) CP output voltage (mean(HS_V_{DD})) and second output (mean(HS_V_{SS})) (b) offset voltage (HSΔ) between the CP output voltage (HS_V_{DD}) and the second output (HS_V_{SS}) and voltage ripple of HSΔ.

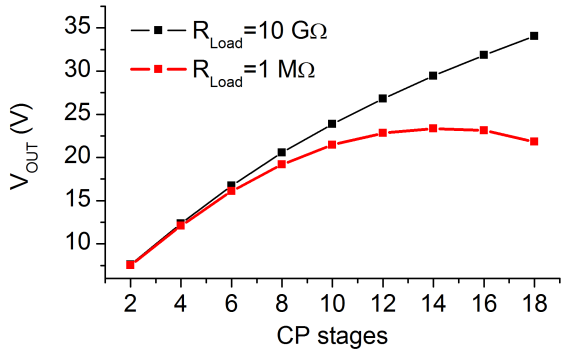


Figure 4.12: Simulated output voltage (V_{OUT}) depending on the number of CP stages and load current caused by a load resistor (R_{Load}).

Table 4.1: Comparison of the analyzed on-chip charge pumps at 1 MΩ load condition. The values in **bold** highlight the advantages and the numbers shown in *italic* show the drawbacks of the circuit.

CP-type	stages	chip size in mm^2	HS_V_{DD} in V	HSΔ in V	HSΔ_ripple in mV
latched CP	16	0.05	**29**	2.1	*242*
GCW	14	*0.2*	*23.4*	*1.2*	**0.5**
Dickson	20	0.05	28.4	1.7	80

In table 4.1 the main properties of the three compared charge pumps are listed. The values for the main (HS_V_{DD}) and second (HS_V_{SS}) output are simulated data based on 1 MΩ load resistors. The values in **bold** highlight the advantages and the numbers in *italic* show the drawbacks of the specific circuit. The latched CP has the best current source capabilities with the drawback of a high voltage ripple of HSΔ. The Greinacher-Cockroft-Walton CP has a very low ripple but requires a doubled layout area. Compared to the unloaded (10 GΩ) condition, the output voltage is decreased to 80 %, which is not sufficient to actuate an RF-MEMS switch described in section 2.3.

In Fig. 4.13, the resulting chip size caused by the number of stages and MIM capacitors of the charge pumps is depicted. While the Dickson and the latched CP have similar performance with similar chip size, the GCW circuit requires relatively large capacitor values, resulting in a doubled layout area. Since the latched CP offers the fastest ramp-up time, this charge pump type is used to drive a single RF-MEMS switch applied in section 5.1.1. The Dickson CP is a compromise between layout area, voltage ripple of HSΔ and therefore used for the demonstrator circuits including a single CP described in section 5.1.2 and section 5.2.

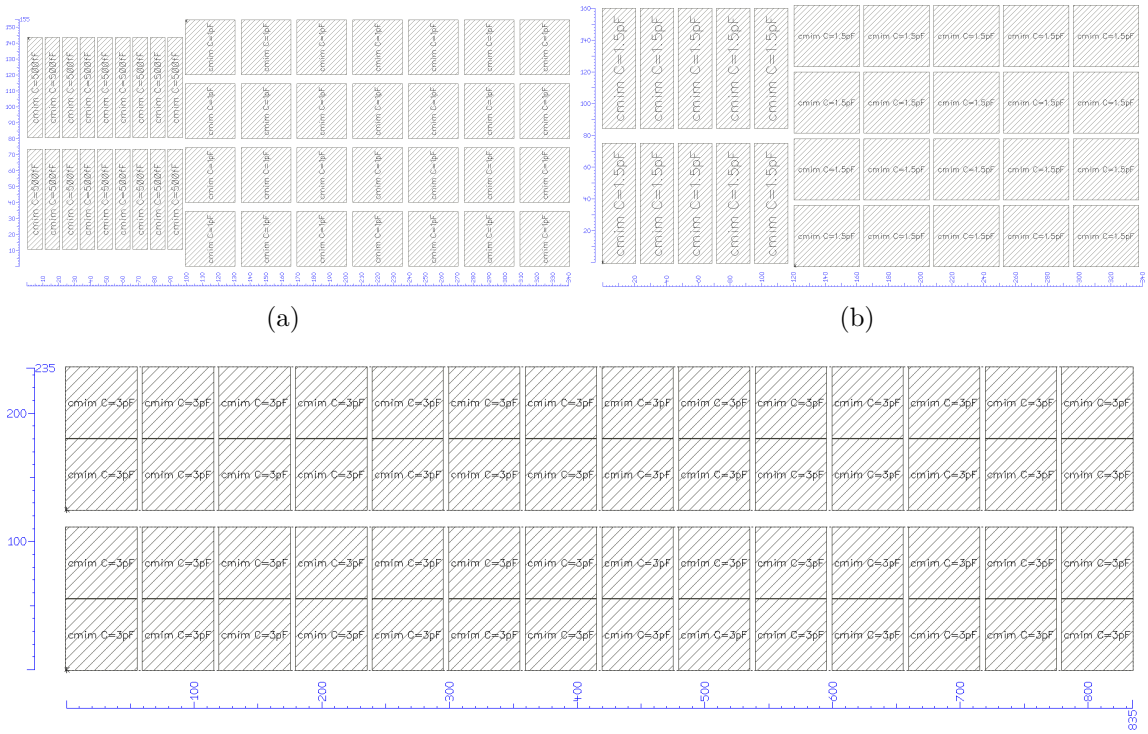


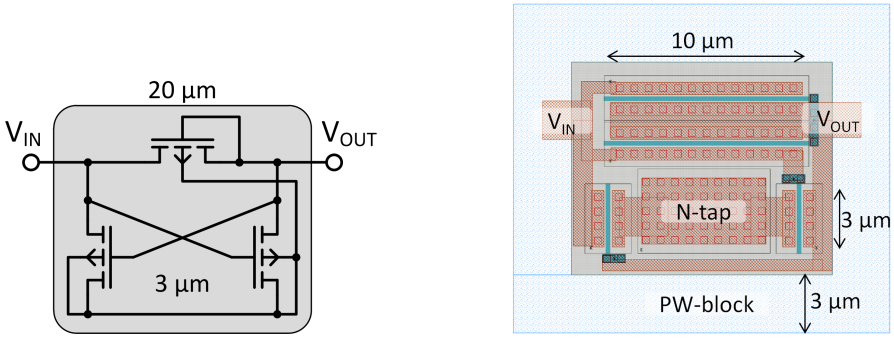
Figure 4.13: Comparison of layout areas for different CP types with similar performance: (a) 16 stage latched CP with 0.5 pF capacitor per stage; (b) 20 stage Dickson CP with 1.5 pF capacitor for the low-voltage stages and 0.75 pF high-voltage stages and (c) 14 stage Greinacher-Cockroft-Walton (GCW) CP with 6 pF capacitance per stage.

4.2.2 Charge Pump Design

The structure of the CP designed in this work is based on the Dickson topology [31], [66] described in section 3.2.1. As analyzed in section 4.2.1, this circuitry offers the best compromise between layout area, output voltages (main and second), output impedance and voltage ripple. The CP stages (Fig. 4.14(a)) are based on LV PMOS transistors described in [31] to enable the operation at elevated bias voltages and to avoid the degradation of V_{th} due to the body effect. In Fig. 4.14(b) the layout of a single CTS is depicted. The total width of the double gate PMOS transistor used as the transfer switch is 20 µm to minimize the resistive loss in transfer mode. As described in section 3.2.1, the two 3 µm wide PMOS transistor are biasing the n-well to avoid the substrate effect. Therefore, a rise of the threshold voltage with increasing operating voltage is avoided. A further detail shown in Fig. 4.14(b) is the 3 µm wide ring (PW-block) surrounding the n-well to enable a sufficient breakdown voltage of the n-well - p-substrate diode of more than 50 V. The dependency of the breakdown voltage on the drawn width of the PW-block area is described more detailed in [17].
Connecting the clock signal to the output (in contrast to Fig. 3.3) of the CP, the output voltage (HS_V_{DD}) and the second voltage (HS_V_{SS}) are synchronized, resulting in a low ripple of HSΔ = HS_V_{DD} – HS_V_{SS}. The offset of HS_V_{SS} is not exceeding the low-voltage CMOS breakdown limits (BV_{DS}, BV_{GOx}), which is required for the level shifter and the high-voltage PLDMOS.
Assuming an unloaded CP, $C_{stage} \gg C_S$ and an input voltage = 0 V, the simplified equation 3.6 is applied to estimate the number of stages for a given output voltage.

$$N = \frac{V_0}{V_{Clk} - V_{th}} = \frac{40\,V}{2.5\,V - 0.5\,V} = 20 \tag{4.1}$$

Additionally, an ideal non-overlapping clock signal (V_{Clk}) is assumed. According to equation 4.1, 20 stages are sufficient to generate 40 V at the CP output under ideal conditions. As already shown in the comparative simulations in section 4.2.1, 32 V is a more realistic value for a 20 stage CP. In Fig. 4.16(a) the dependency of the output voltage on the stage capacitance is shown. A stage capacitance in the range of 2 – 2.5 pF is the optimum for this specific CP. The mean value of HSΔ is not exceeding the low-voltage CMOS limits (BV_{DS}, BV_{GOx}) and the voltage ripple of HSΔ is approx. 45 mV. As a trade-off between stage capacitance, operating voltage, and layout area, the first 10 stages are equipped with a single MIM capacitor



(a) (b)

Figure 4.14: (a) Dickson CTS based on [31]. The double gate PMOS used as transfer gate has a total gate width of 20 µm. The gate width of NW (gray area) biasing transistors is 3 µm. (b) Layout snapshot with surrounding 3 µm wide PW-block ring to increase the n-well to p-substrate breakdown voltage.

with 2.3 pF and the remaining 10 stages contain a serial combination of two MIM capacitors, resulting in a decreased total capacitance of 1.5 pF. In Fig. 4.15 the block diagram of the designed CP is shown. In contrast to the Dickson topology, the clock signal is also connected to the output of the last stage. This will synchronize both CP outputs at the cost of an increased ripple at the output of the CP (HS_V_{DD}). This ripple will not affect the actuation of the RF-MEMS switch and must be accepted to ensure a reliable operation of the level shifter and the gate-source voltage of the PLDMOS transistors.

In Fig. 4.17(a), the output voltage versus CP load is depicted. Since the capacitance per stage is almost doubled compared to the simulation results in Fig. 4.7, the generated output voltages (HS_V_{DD} and HS_V_{SS}) are raised by 2.5 V. The correlation between generated voltage and stage capacitance is not predicted by equation 3.3. The mean value of HSΔ never exceeds the low-voltage CMOS limits (BV_{DS}, BV_{GOx}) and the voltage ripple of HSΔ is below 100 mV for a load current up to 58 µA for HS_V_{DD} and 54 µA for HS_V_{SS}.

The current CP is optimized for a clock frequency of 300 MHz, as can be seen in Fig. 4.18. An increased clock frequency results in decreasing output voltages HS_V_{DD} and HS_V_{SS} while the voltage ripple of HSΔ is not affected.

As can be seen in the simplified equation 4.1, the generated output voltage of the CP is propotional to clock amplitude. The linear relation between clock signal amplitude and generated voltages HS_V_{DD} and HS_V_{SS} is depicted in Fig. 4.19(a). Changing the

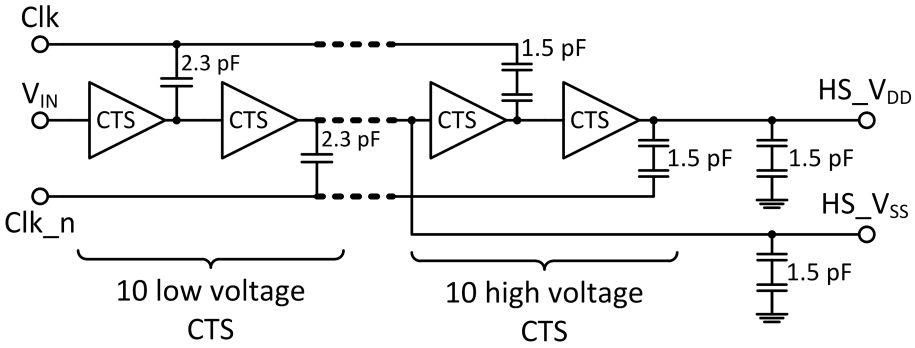


Figure 4.15: Block diagram of a 20 stage Dickson CP with two outputs based on Shin's CTS (see Fig. 4.14). To reduce the CP chip size area 10 low-voltage stages consisting of a single MIM capacitor and 10 high-voltage stages using two stacked MIM capacitors are combined.

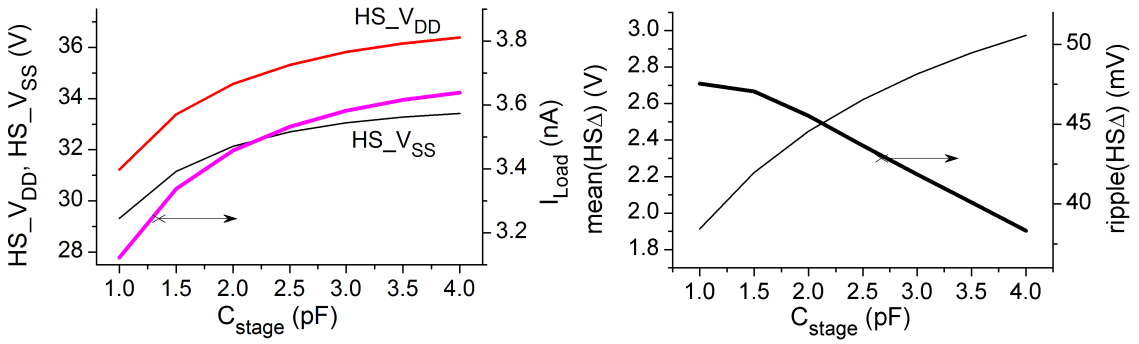
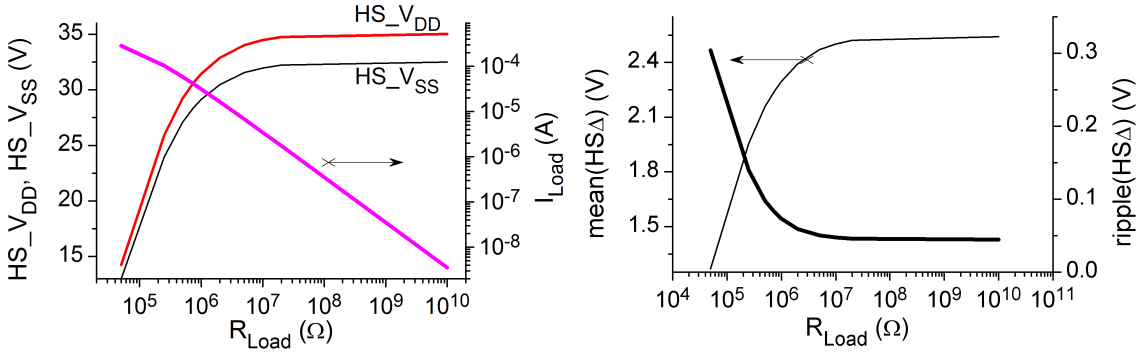
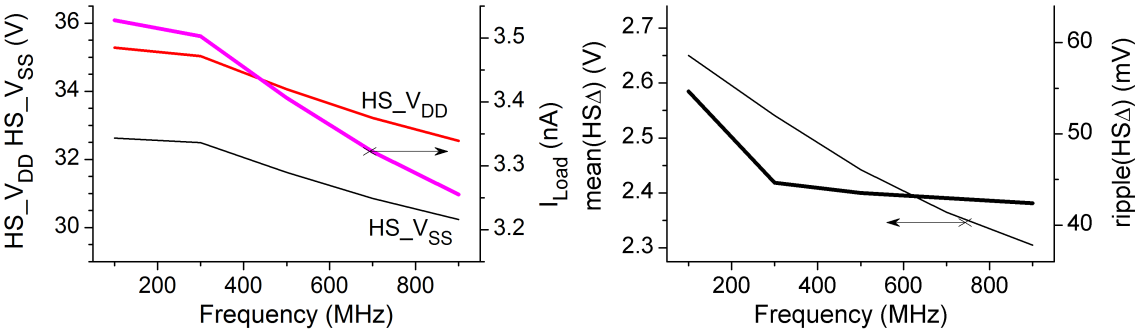


Figure 4.16: Simulated output voltages and current (I_{Load}) as a function of the stage capacitance (C_{stage}) of a Dickson CP. (a) CP output voltage (mean(HS_V_{DD})) and second output (mean(HS_V_{SS})) (b) voltage offset (HSΔ) between CP output voltage (HS_V_{DD}) and second output (HS_V_{SS}) and voltage ripple of HSΔ.



(a) (b)

Figure 4.17: Simulated output voltages and current (I_{Load}) of the final Dickson CP with a stage capacitance of 2.32 pF and 1.5 pF as a function of load resistance (R_{Load}). (a) CP output voltage (mean(HS_V_{DD})) and second output (mean(HS_V_{SS})) (b) voltage offset (HSΔ) between the CP output voltage (HS_V_{DD}) and the second output voltage (HS_V_{SS}) and voltage ripple of HSΔ.



(a) (b)

Figure 4.18: Simulated output voltages and current (I_{Load}) of a Dickson CP as a function of clock frequency with a stage capacitance of 2.32 pF and 1.5 pF. (a) CP output voltage (mean(HS_V_{DD})) and secondary voltage (mean(HS_V_{SS})) (b) voltage offset (HSΔ) between the CP output voltage (HS_V_{DD}) and the secondary voltage (HS_V_{SS}) and voltage ripple of HSΔ.

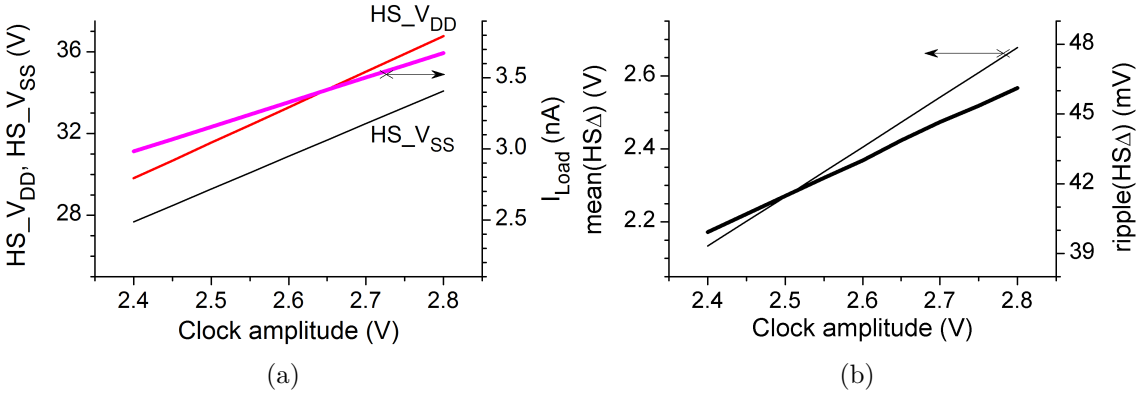


Figure 4.19: Simulated output voltages and current (I_{Load}) of a Dickson CP with a stage capacitance of 2.32 pF and 1.5 pF as a function of the clock signal amplitude. (a) CP output voltage (mean(HS_V_{DD})) and secondary voltage (mean(HS_V_{SS})) (b) voltage offset (HSΔ) between the CP output voltage (HS_V_{DD}) and the secondary voltage (HS_V_{SS}) and voltage ripple of HSΔ.

clock signal amplitude in the range of 0.4 V the HS_V_{DD} varies between 30 V and 37 V. It is worth mentioning that HSΔ exceeds the BV_{DS} and BV_{GOx} of 2.5 V for a clock amplitude >2.7 V. This fact may cause an accelerated degradation of the low-voltage CMOS transistors.

A layout snapshot of the designed CP is depicted in Fig. 4.20. As the capacitors define the chip size of the charge pump, the required silicon area is 0.115 mm^2.

The measured output voltage (HS_V_{DD}) as a function of the ring oscillator bias voltage (V_{DD}) and the load current (I_{Load}) is depicted in Fig. 4.21. The ripple in the generated voltage is not found in the transient circuit simulations (clock frequency sweep: Fig. 4.18, clock amplitude sweep: Fig. 4.19) because a correlation between clock frequency and amplitude was not considered. Additionally, the input voltage (V_{IN}) of the CP was kept at 0 V, while V_{IN} was synchronized with V_{DD} during the circuit characterization.

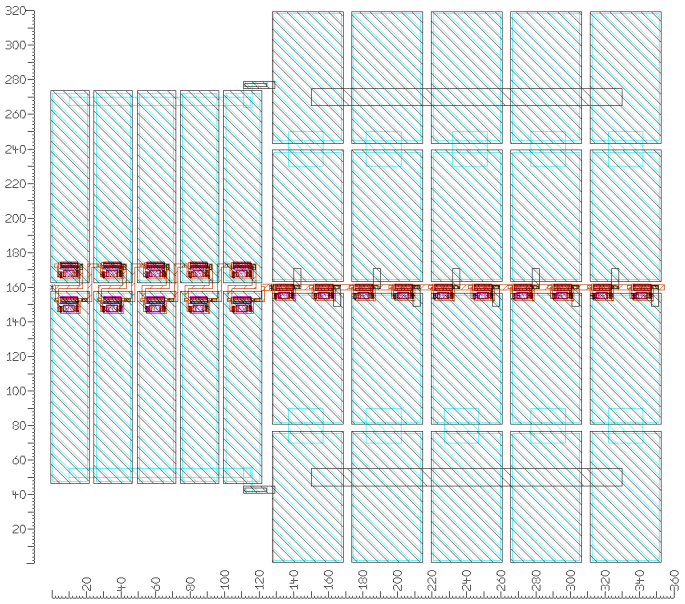


Figure 4.20: Layout size of the 20 stage Dickson CP (10 medium-voltage stages comprising a single MIM capacitor and 10 high-voltage stages using a stack of two MIM capacitors).

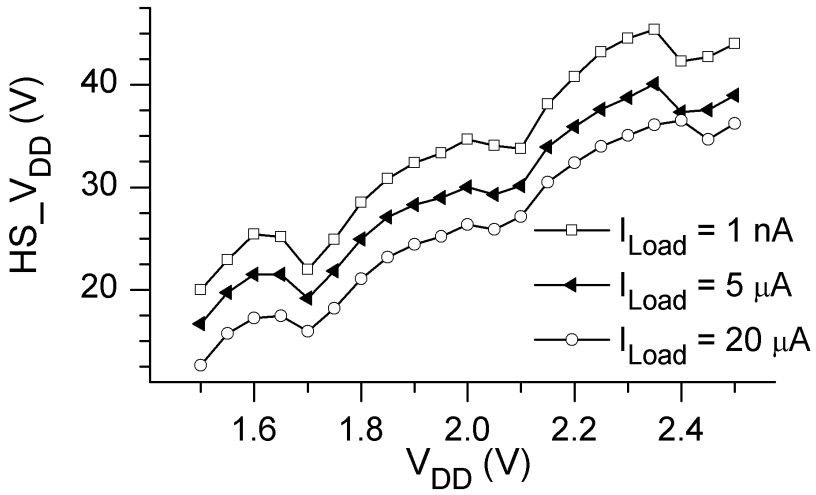


Figure 4.21: Measured output voltage (HS_V_{DD}) of the designed CP versus VCO bias (V_{DD}) and load current (I_{Load}). The input voltage (V_{IN}) of the CP is synchronized with V_{DD}.

4.2.3 Conclusion

Output voltages in the range of 40 V can be generated with the designed CP. The measured output voltage is 10 V higher compared to the transient circuit simulation. This can be explained with a $V_{IN} = V_{DD}$ during the characterization and the correlation between output voltage and clock signal frequency and amplitude. Measurements under different load conditions prove the voltage source capability of the designed CP for MEMS matrix applications. Since the integrated differential ring oscillator generates the orthogonal clock signal, the functionality of the oscillator is indirectly verified.

4.3 HV Switch Circuit based on LDHBTs

Using the high-voltage npn HBT described in section 2.2, a simple MEMS driving circuit consisting of three transistors and two resistors is described in this section. The schematics of the HV switch basesd on SiGe HBT is depicted in Fig. 4.22. For a control voltage (V_{ctrl}) less than 0.7 V LDHBT1 is assumed as isolating and the resulting base voltage of LDHBT2 is equal to the supply voltage (V_{CP}). Thus V_{CP} is transfered to the MEMS electrodes (see equation 4.2). If the control voltage (V_{ctrl}) is greater than 0.7 V the LDHBT1 is assumed as a short and the base of LDHBT2 and the emitter of LDHBT3 are shorted to ground. Therefore the MEMS electrode capacitance is discharged via LDHBT3 (see equation 4.3).

$$\text{down-state: } V_{ctrl} \leq 0.7\,V \Rightarrow V_{MEMS} = V_{CP} - 0.7\,V \tag{4.2}$$

$$\text{up-state: } V_{ctrl} \geq 0.7\,V \Rightarrow V_{MEMS} = 0.7\,V \tag{4.3}$$

This circuit can be used to switch the high MEMS actuation voltage. A maximum discharge current can be asumed as $V_{CP}/10\,k\Omega = 40\,V/10\,k\Omega = 4\,mA$. Regarding the RF-MEMS switch release time in [17] (250 kΩ discharge resistor), this circuit will significantly decrease the release time and therefore improve the switching speed of the MEMS-based system.

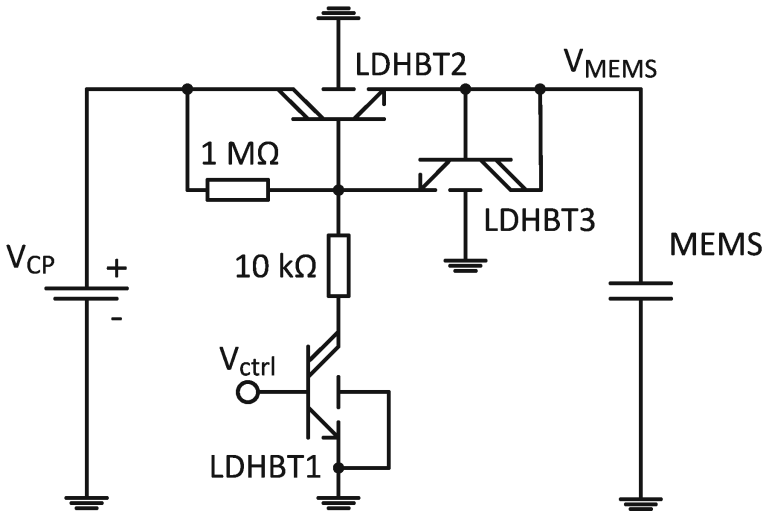
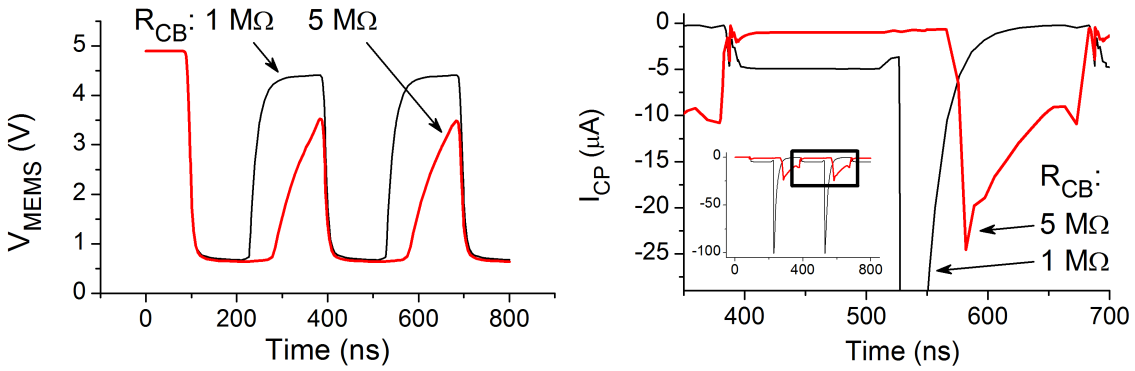


Figure 4.22: Schematics of HV transfer and discharge circuit based on high-voltage bipolar transistors.



(a) (b)

Figure 4.23: Feasability test: (a) transient simulation of the output voltage (V_{MEMS}) using a low-voltage HBT model for different values (1 MΩ and 5 MΩ) for the collector-base resistor (R_{CB}) for the LDHBT2. The current (I_{CP}) drawn (b) in discharge mode is 5 µA based on the 1 MΩ resistor.

4.3.1 Circuit, Simulation and Layout

Since there is no model available for the LDHBT, a model of a 7 V BV_{CEO} HBT is used for predictive simulations. Circuit simulations are performed at V_{CP}=5 V using the above mentioned HBT model. The results of a transient simulation are shown in Fig. 4.23. In discharge mode, a leakage current of 5 µA is simulated, which can be simply proven as follows: I_{CP}= V_{CP}/(1 MΩ + 10 kΩ)= 5 V/1.01 MΩ= 5 µA. Increasing the collector-base resistance from 1 MΩ to 5 MΩ the leakage current drawn from the charge pump is decreased significantly at the cost of an increased rise time. On the other hand, the current peaks of I_{CP} are reduced from 100 µA to 25 µA using a 5 MΩ resistor.

In Fig. 4.24 the layout of the proposed circuit is depicted. Each LDHBT consists of 50 single devices, resulting in a total A_E of 88.2 µm^2. The chip size of the LDHBT based charge / discharge ciruit is 190 µm x 180 µm. The collector current I_C at V_{BE}= 0.85 V and V_{CE}=32 V of a single LDHBT (A_E= 1.76 µm^2) shown in forward Gummel plot (Fig. 2.8) is 1 mA. Thus, the used LDHBT array can drive enough current in MEMS discharge mode.

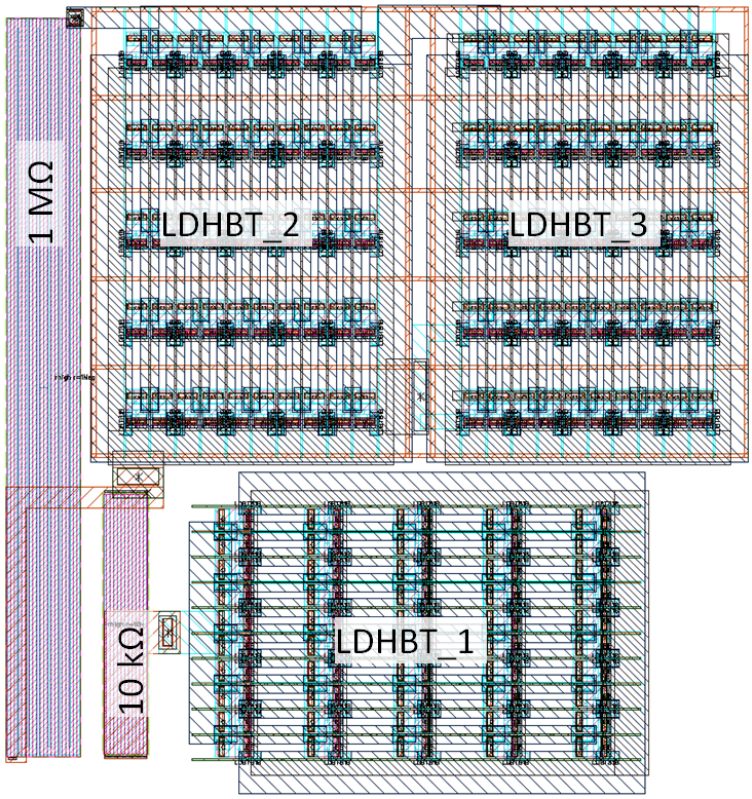


Figure 4.24: Layout of the HV charge / discharge circuit based on npn LDHBTs.

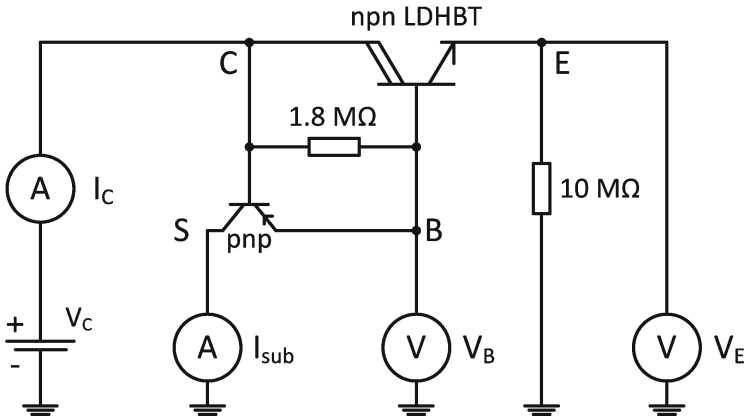


Figure 4.25: Setup to measure the high-side behavior of the HBT in common base configuration (LDHBT2& 3 in Fig. 4.22). The pnp transistor represents the parasitic substrate transistor.

4.3.2 DC-Characterization

The setup to measure the substrate current and breakdown behavior is shown in Fig. 4.25. In contrast to the circuit depicted in Fig. 4.22 with an electrical connection between bulk silicon (p-substrate) and ground, a test structure including a single emitter device with a separated substrate contact was tested. Thus, the substrate current (I_{sub}) can be measured.

As a reference, the measured substrate current (I_{sub}), collector current (I_C) and the output voltage (V_E) for a low-voltage HBT (BV_{CEO}=7 V) are plotted versus the collector voltage (V_C) in Fig. 4.26. The influence of the parasitic substrate transistor occurs at 26 V.

The measured substrate current (I_{sub}), collector current (I_C) and the output voltage (V_E) versus the collector voltage (V_C) for the high-voltage HBT are depicted in Fig. 4.27. For bias voltages >5 V, the substrate current starts to increase which is by far too low for the desired application. In contrast to the BV_{CEO} and BV_{CBO} measurements shown in Fig. 2.9(b) where the LDHBT is operated in common emitter mode, the transistor has very low breakdown voltage when the emitter-substrate voltage is V_{ES}>0 V (high-side operation). Placing the LDHBT in an isolated p-well, the emitter can be connected with the floating substrate. Thus, the emitter-substrate voltage is forced to 0 V, which would improve the high-side capability.

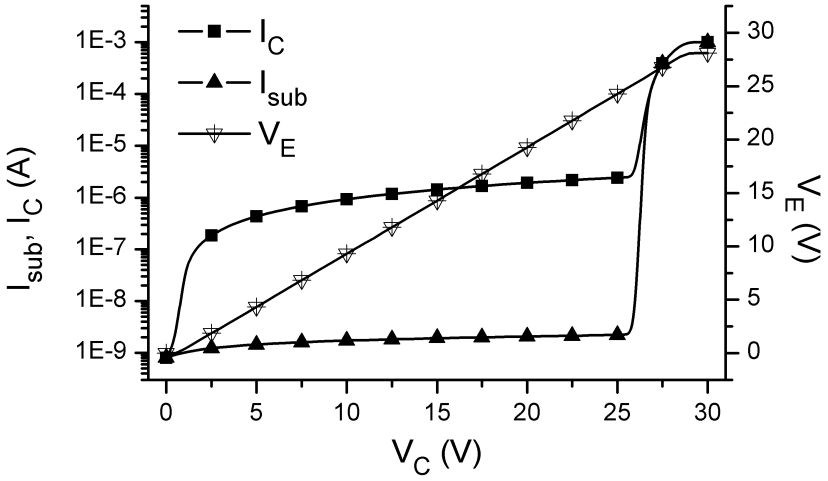


Figure 4.26: Measured high-side behavior (collector(I_C)-, substrate current(I_{sub}) and emitter voltage (V_E) versus collector voltage (V_C)) of a SiGe:C HBT with high collector doping (BV_{CEO}=7 V). A linear increase of the output voltage (V_E) is measured. The measured substrate current is drastically increasing after ∼26 V, which is caused by the parasitic pnp transistor.

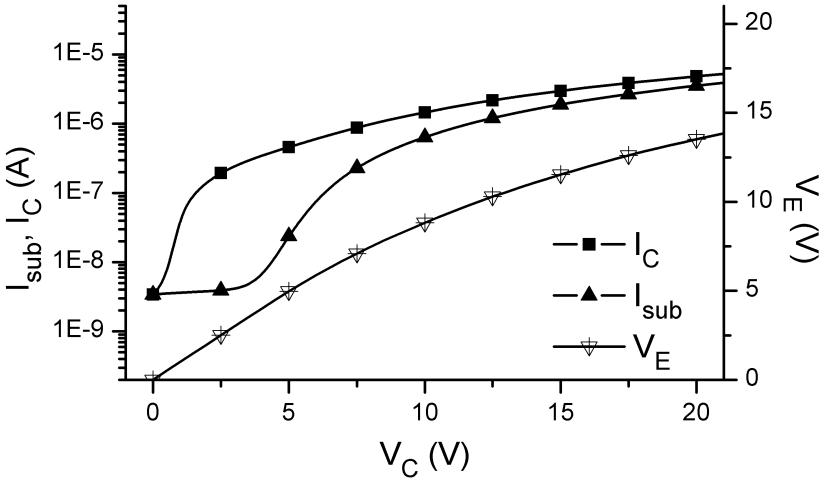


Figure 4.27: Measured high-side behavior (collector(I_C)-, substrate current(I_{sub}) and emitter voltage (V_E) of the LDHBT with low collector doping (BV_{CEO}=50 V). The measured substrate current is already increasing at V_C ∼5 V.

4.3.3 Conclusion

A simple HV switching circuit based on three high-voltage HBTs and two resistors is presented. Further improvements are mandatory to decrease the leakage current drawn from the CP by a factor of 10 in discharge mode. This can be achieved by increasing the resistance from 1 MΩ to 10 MΩ at the cost of an increased rise time. The increase of the resistor layout is compensated by minimized LDHBT arrays. In high-side operation mode, the low collector doping required for a high BV_{CEO} significantly decreases the breakdown of the collector-substrate diode. This effect was proven by measuring of similar HBTs differing in the collector doping but having an equivalent base-emitter construction. Thus, the transfer HBTs (LDHBT2,3 in Fig. 4.22) must be placed in an isolated p-well, which is currently not available. Therefore, the development on the LDHBT-based high-voltage switch has to be postponed until an isolated LDHBT is developed.

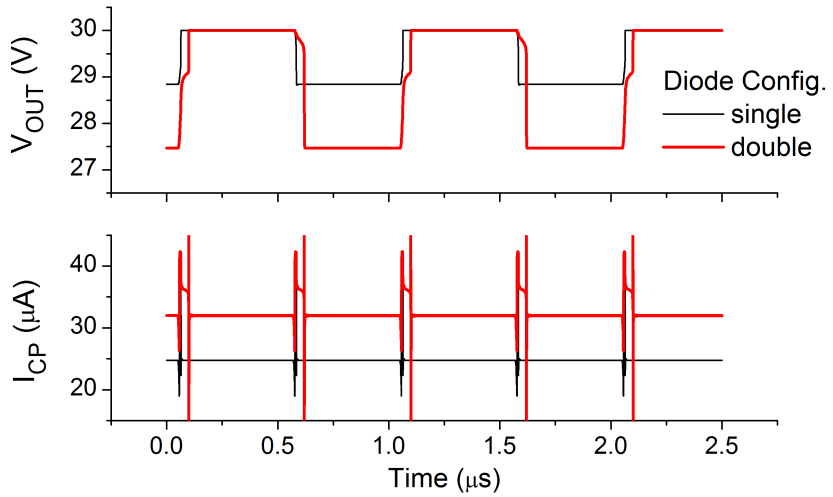


Figure 4.28: Transient simulation of a current-controlled level shifter depicted in Fig. 3.7. The current (I_{CP}) needs to be provided by the on-chip CP. The traces for V_{OUT} is the voltage swing at the output of the level shifter if a single or two diode-connected MOS transistors are used.

4.4 HV Switch based on LDMOS Inverter

In the following sections, the developed HV inverter based on LDMOS transistors and the necessary driving circuitry (level shifter) is described. This is an alternative approach to the HV switching circuit based on the LDHBTs. The current drawn from the CP is reduced at the cost of an increased circuit design and processing effort (high energy implantation step).

4.4.1 Level Shifter

The level shifter provides the control signal for the PLDMOS transistor in the HV-LDMOS inverter enabling the design of high-voltage switch matrices. A single CP is sufficient for several RF-MEMS switches and will result in a reduced chip size for the HV generation and switching matrix.
Based on circuit simulations, the steady state current of a DC coupled LS (section 3.3.1 Fig. 3.7) can be reduced to 20 – 30 µA (Fig. 4.28) while keeping an output amplitude in the range of 1 – 2.5 V. Nevertheless, a current consumption of 30 µA for a single LS is too much for high-voltage switch matrix applications powered by a single on-chip CP.
The block diagram of the level shifter circuit designed in this work is depicted in

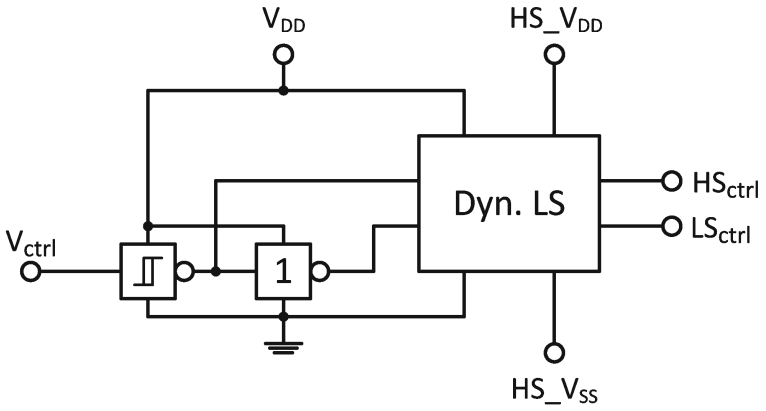
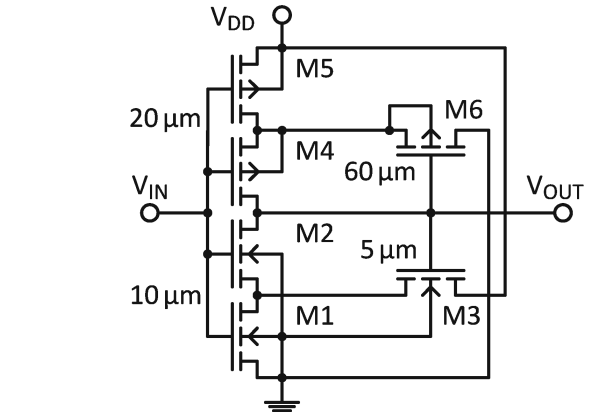


Figure 4.29: Block diagram of a capacitively coupled level shifter including Schmitt-trigger to shape the input pulse and inverter to generate the inverted control signal for the level shifter.

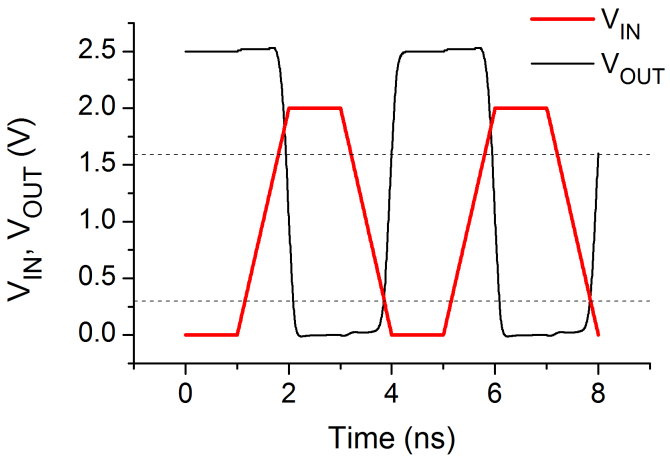
Fig. 4.29.

The functionality of the capacitively coupled level shifter strongly depends on the slope of the control signal. Thus, a control signal shaping Schmitt-trigger circuit (depicted in Fig. 4.30(a)) was designed and integrated. Additionally, the circuit minimizes the false switching of the level shifter due to an unstable input signal. Equations 4.4 and 4.5 are based on [68] while the gate length ($L_{M1–6}$) is not included, since it is kept at the minimum of 0.25 µm. To calculate the gate widths (W_{M3}, W_{M6}) of the transistors (M3, M6) the trigger voltages are defined as V_{SPH}=1.6 V and V_{SPL}=0.3 V. Transient simulation results are depicted in Fig. 4.30(b) to verify the functionality of the circuit and to prove the calculated gate width for M3 and M6.

$$
\begin{aligned}
L_{M1} = L_{M2} = L_{M3} = L_{M4} = L_{M5} = L_{M6} &= 0.25\,\mu m \\
W_{M1} = W_{M2} &= 10\,\mu m \\
W_{M4} = W_{M5} &= 20\,\mu m \\
W_{M3} = {}^{W_{M1}}\Big/\left[\tfrac{Vdd-V_{SPH}}{V_{SPH}-V_{thn}}\right]^2 &= 5\,\mu m \qquad (4.4) \\
W_{M6} = {}^{W_{M5}}\Big/\left[\tfrac{V_{SPL}}{Vdd-V_{SPL}-V_{thp}}\right]^2 &= 60\,\mu m \qquad (4.5)
\end{aligned}
$$



(a)



(b)

Figure 4.30: (a) Schematics and (b) transient simulation of designed Schmitt-Trigger. The trigger levels 0.3 V and 1.6 V are marked with a dotted line.

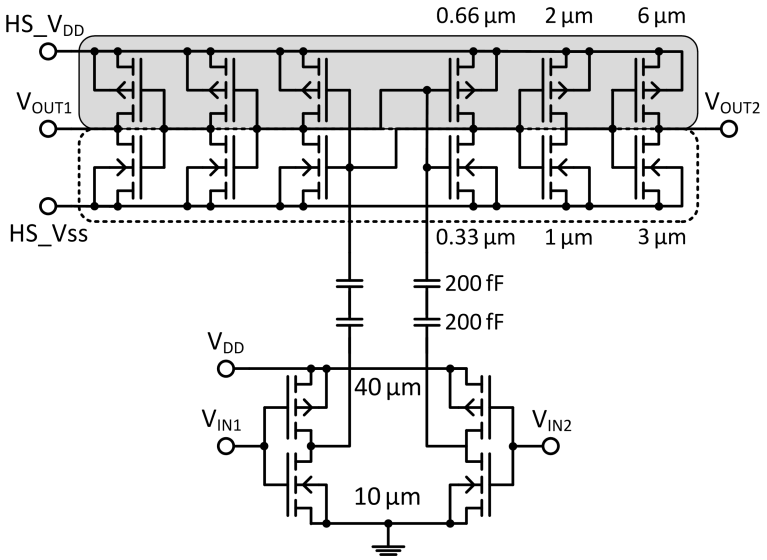


Figure 4.31: Capacitively coupled level shifter including buffer stages in the high-voltage domain. The dashed line symbolizes an isolated p-well and the gray area indicates the n-well. The numbers indicate the gate width of the PMOS and NMOS transistors.

In contrast to [75], the LS circuit in this work is designed fully symmetrical. The schematics of the capacitively coupled level shifter including buffer stages is shown in Fig. 4.31. Two capacitors are connected in series to prevent the breakdown of the MIM capacitor. To transfer the signal slope properly from the low-side inverter across the 100 fF coupling capacitance to the high-side, the low-side driver is designed with 60 times wider gate width than the high-side inverters/latch. Since the NMOS transistors of the high-side latch are low-voltage devices, they are placed into an isolated p-well. The increased n-well to p-substrate isolation for the PMOS transistors is realized by a ring without p-well doping surrounding the n-well regions. Since HS_V_{DD} and HS_V_{SS} of the level shifter core and the high-side buffer stage are combined in the layout, only the total static current could be measured. The measured current is mainly caused by the 1 MΩ input resistor of the oscilloscope. During the characterization, the output was predominantly in HV state (42 V), thus a current of 42 µA is measured at HS_V_{DD} while the current at HS_V_{SS} was in the nA range.

The simulated current spikes of the level shifter core are depicted in Fig. 4.32. The transient simulation shows a high current at the beginning, which is caused by the undefined state of the high-side latch. Thus, an initialization of the level shifter circuitry is mandatory. After a single switching event, the simulated current settled

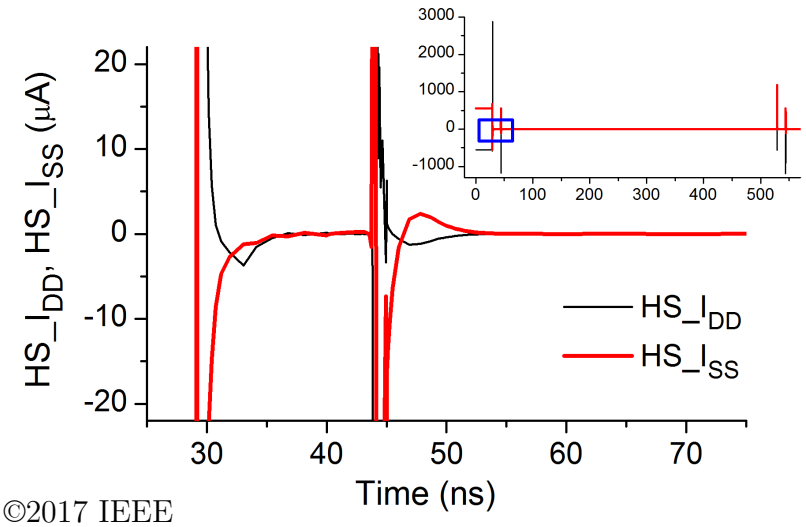


Figure 4.32: Simulated transient currents (HS_V_{DD}, HS_V_{SS}) of the level shifter high-side without output buffer stages. The simulated currents, 10 ns after the switching event, are below 0.5 µA. In the beginning, the high-side stage is in undefined state and the currents are high [87].

below 0.5 µA within 10 ns.

Fig. 4.33 illustrates the comparison of the level shifter output signal and the level shifter core. The signal rise and fall time of the level shifter core (V_{LScore}) providing the control signal for the PLDMOS transistor of the HV inverter, is in the range of picoseconds. Due to the parasitic impedance caused by the measurement setup, the output signal rise and fall time (V_{LSout}) is increased to 5 µs.

A chip micrograph of the designed level shifter circuit with additional output buffer to drive the measurement equipment is shown in Fig. 4.34. The chip size of the level shifter core designed to drive the PLDMOS transistor is 130 µm x 65 µm.

The measurements were performed on wafer using a LeCroy 6100A oscilloscope, a pulse generator HP8114A and a semiconductor parameter analyzer Agilent 4156C as a DC supply. To test the functionality and speed of the level shifter 10 ns pulses (Signal pin “Vctrl” in Fig. 4.29) were applied. The bias voltage for high-side Vdd (HS_V_{DD}) was set to 42 V and 40 V for high-side Vss (HS_V_{SS}). For testability, a chain of three inverter stages (marked as ”Buffer“ in Fig. 4.34) is mandatory to drive the high capacitive load caused by the coaxial cables and the input of the oscilloscope. The inverter stages consist of isolated NMOS and PMOS transistors with a gate width of 10 µm/20 µm (NMOS/PMOS) for the first stage. The gate width of the following two stages is scaled by a factor of three. The output buffer

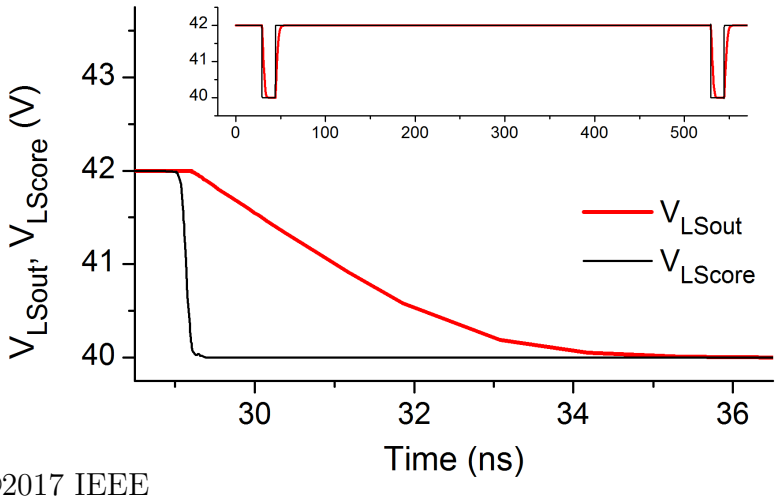


Figure 4.33: Comparison of the simulated switching speed of the level shifter core (V_{LScore}) and the output signal of the circuit (V_{LSout}) loaded with the parasitic impedance caused by the measurement setup [87].

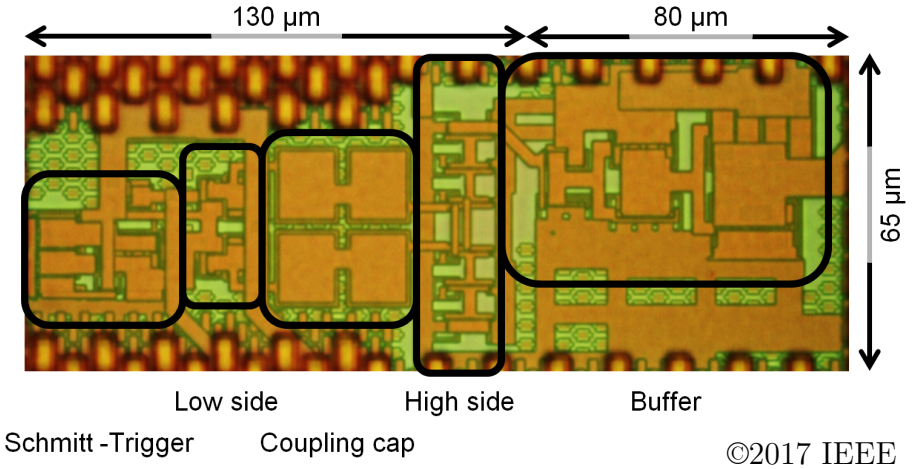


Figure 4.34: Chip micrograph of the fabricated level shifter. The different blocks Schmitt-trigger, low-side CMOS inverter (driver), stacked MIM (coupling cap), high-side CMOS latch and high-side buffer are marked [87].

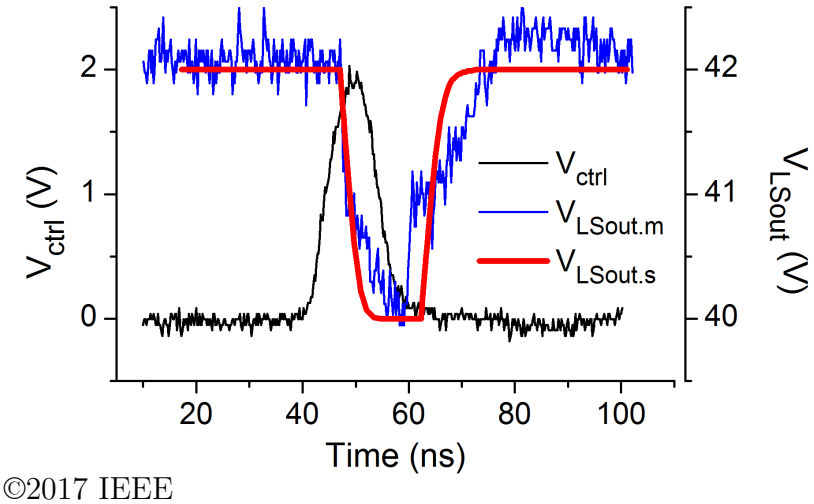


Figure 4.35: Measured ($V_{LSout.m}$) and simulated ($V_{LSout.s}$) transient output signal of the level shifter. The trace "V_{ctrl}" represents the input signal of the level shifter. The simulation considers a capacitive load of 65 pF in parallel with a 1 MΩ resistor caused by the coaxial cable and the oscilloscope [87].

of the level shifter was contacted with a ground signal ground (GSG) Probe and connected via a coaxial cable to the 1 MΩ terminated input of the oscilloscope. The estimated capacitance of the coaxial cable and the input of the oscilloscope is in the range of 65 pF. In conjunction with the 1 MΩ termination, the output signal shape is significantly influenced. In Fig. 4.35 the measured output signal of the level shifter ($V_{LSout.m}$) is depicted together with the simulated data ($V_{LSout.s}$). When analyzing the measured data, it is mandatory to consider signal reflection due to impedance mismatch.

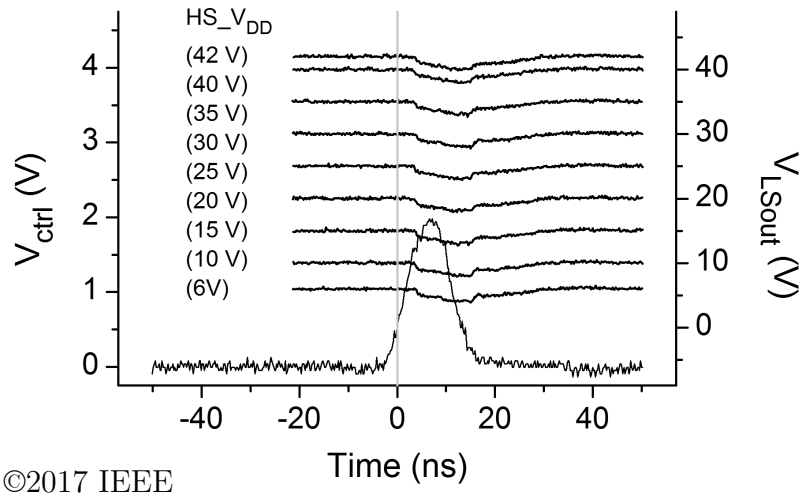


Figure 4.36: Measured output signal (V_{LSout}) of the capacitively coupled level shifter for different high-side bias voltages (HS_V_{DD} and HS_V_{SS} = HS_V_{DD} - 2 V). The grey vertical line indicates the 0.3 V trigger level of the oscilloscope on the control signal (V_{ctrl}) [87].

To test the level shifter at different high-side biases, the voltage for HS_V_{DD} was swept from 6 V up to 42 V while HS_V_{SS} was swept with an offset of 2 V from 4 V up to 40 V. The measured traces depicted in Fig. 4.36 show a reliable operation for a broad range of high-side bias voltages.

Conclusion

A fast high-voltage level shifter with a quiescent current consumption below 500 nA was designed in this work. The symmetric design makes an initial switching necessary to set the undefined or floating high-side output to defined state. The current leakage is mainly caused by the resistive load and not by the level shifter itself. Transient simulations of the level shifter core, as the driver for the high-voltage LDMOS inverter, show a rise and fall time in the range of 200 ps. The measured and simulated rise and fall time of the level shifter combined with an output buffer is in the range of 15 ns. The parasitic impedance of the measurement setup is 65 pF in parallel with 1 MΩ input resistance of the oscilloscope. The measurements prove a reliable operation for a broad range of high-side bias voltages from 6 V up to 42 V. The switching speed of the circuit is independent from the high-side bias voltage.

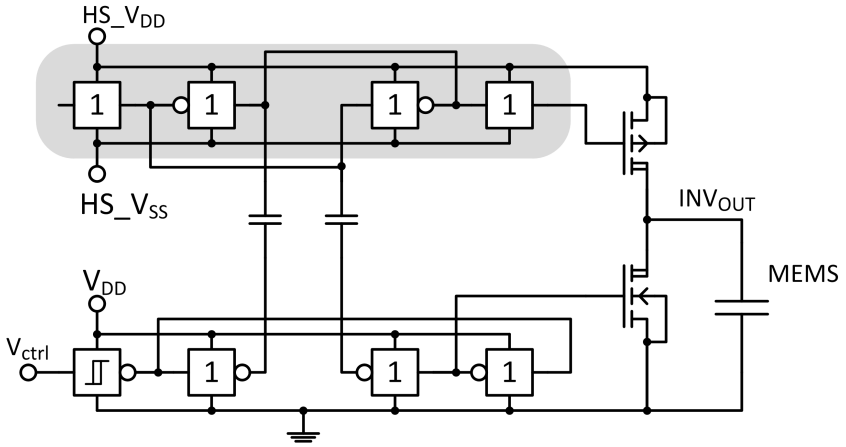


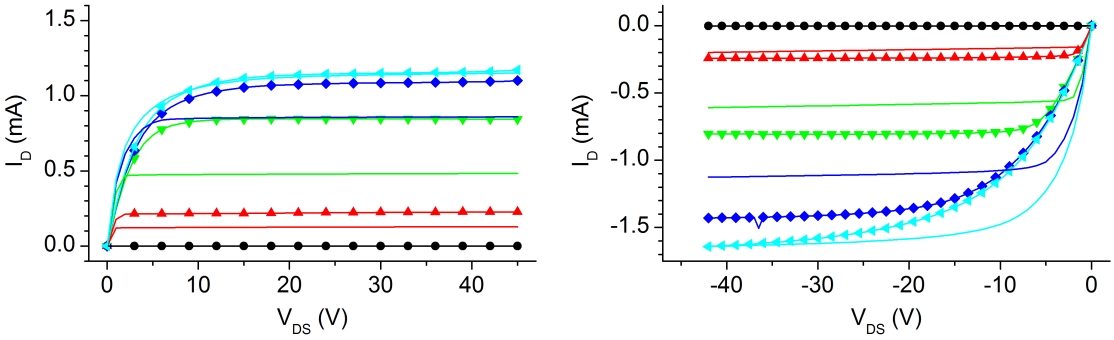
Figure 4.37: Block diagram of the high-voltage LDMOS inverter including Schmitt-trigger, level shifter and LDMOS transistors. The area highlighted in gray symbolizes the high-voltage domain.

4.4.2 HV Level Shifter Combined with HV Inverter

The level shifter (described in section 4.4.1) provides the gate control signal for the HV-PLDMOS (see block diagram in Fig. 4.37). Since the HV-LDMOS inverter charges and discharges the small RF-MEMS switch electrode capacitance of approximately 200 fF, the total gate width of the PLDMOS transistor is designed with 10 µm and the gate width of the NLDMOS transistor is designed with 5.3 µm gate width.

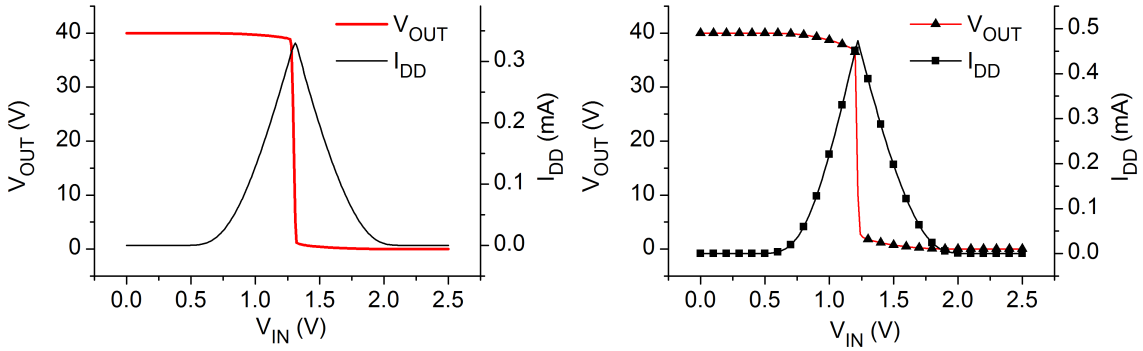
LDMOS Model Verification

Like in the case of the HV npn LDHBT, no model is available for the HV LDMOS transistors. To enable circuit simulations, available Hiroshima-University STARC IGFET model (HiSIM_HV) models for 20 V PLDMOS and NLDMOS transistors were evaluated. Since the transistors are operated in digital mode (V_{GS}=0 V or 2.5 V), the required model accuracy is low. DC simulations are performed and compared with measured output characteristics of the HV LDMOS transistors to verify the usability of these models for higher operating voltages. The measured and simulated forward output characteristics are depicted in Fig. 4.38. The gate width of both transistors was adjusted to fit the measured drain current at V_{DS}=42 V and V_{GS}=2.5 V. Using the extracted gate width, an LDMOS inverter is simulated (Fig. 4.39(a)). The simulation shows symmetric behavior and is very similar compared to the measured characteristics depicted in Fig. 4.39(b).



(a) (b)

Figure 4.38: Measured (symbols) and simulated (line) forward output characteristics (drain current (I_D) versus drain-source voltage ($|V_{DS}|$>20 V) and gate-source voltage (V_{GS})) of the (a) 20 V NLDMOS and (b) 20 V PLDMOS transistors provided by the PDK to check the model convergency or breakdown effects. The gate width of the model is adjusted (decreased) resulting in a similar drain current for V_{GS} = 2.5 V.



(a) (b)

Figure 4.39: Model verification of 20 V PDK LDMOS transistor models. (a) Simulated and (b) measured inverter characteristics (output voltage (V_{OUT}) and current (I_{DD}) versus input voltage (V_{IN})) at a biasing voltage of 40 V.

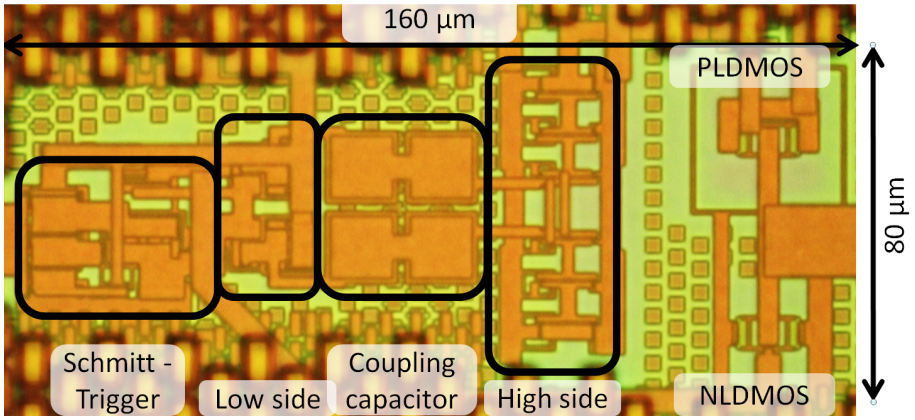


Figure 4.40: Chip micrograph of the fabricated high-voltage inverter circuit combined with the level shifter.

Layout and Characterization

In Fig. 4.40 the chip micrograph is depicted. The chip size of the compact LDMOS inverter including driver circuit is 160 µm x 80 µm. The only difference compared to the circuit shown in Fig. 4.34 is the replacement of the output buffer with the high-voltage LDMOS inverter.

All measurements were performed on wafer using a LeCroy 6100A oscilloscope, a pulse generator HP8114A and a semiconductor parameter analyzer Agilent 4156C as a DC supply. Since the gate widths of the LDMOS transistors are sufficiently dimensioned to charge and discharge the RF-MEMS switch electrode capacitance, the circuit performance is degraded while driving the parasitic capacitance of the test equipment. Therefore, the period time of the control signal was increased to 5 µs to prove the functionality of the circuit. A 200 kHz square wave signal with 2 V amplitude was applied to the input V_{ctrl} (Fig. 4.37) and HS_V_{DD} and HS_V_{SS} were set to 42 V and 40 V respectively. The measured and simulated transient LDMOS inverter output voltage (V_{OUT}) is shown in Fig. 4.41. The simulation is in very good agreement with the measurement while the capacitance of the coaxial cable and the input of the oscilloscope (in the range of 65 pF) is considered during circuit simulation. A rise time of 2.5 µs and a fall time of 2 µs can be extracted. Re-simulating with the RF-MEMS electrode capacitance of 200 fF, the rise (charge) and fall (discharge) times are drastically decreased to 10 ns and 8 ns respectively. The measured data of the level shifter circuit (combined with an output buffer) shown in Fig. 4.35 confirm the simulated rise and fall time of 10 ns and 8 ns.

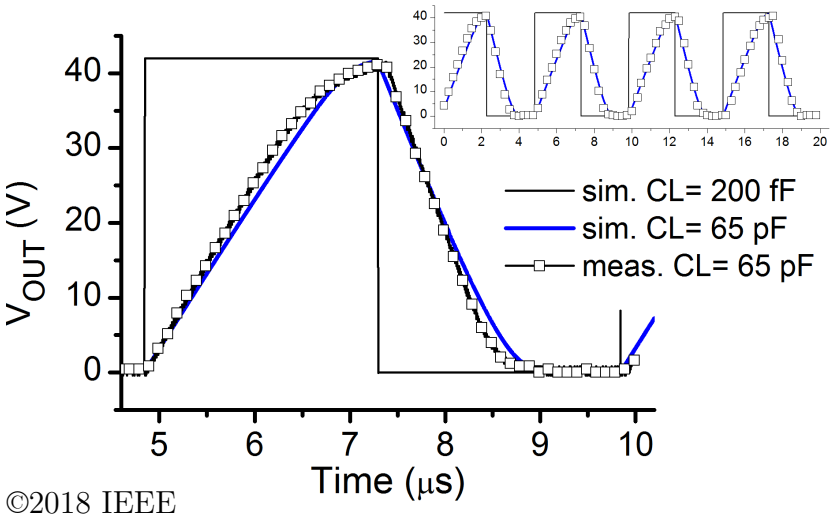


Figure 4.41: Measured and simulated output signal (V_{OUT}) of the LDMOS inverter. The estimated load capacitance (CL) is 65 pF in parallel to the 1 MΩ input resistance of the oscilloscope. The simulation is in very good agreement with the measurement. A rise time of 2.5 µs and fall time of 2 µs can be extracted. Replacing the parasitic load of the measurement equipment with the RF-MEMS electrode capacitance of 200 fF the rise and fall time is drastically decreased to 10 ns and 8 ns respectively [44].

4.4.3 Conclusion

A compact LDMOS inverter including driver circuit (LS) with a chip size of 160 µm x 80 µm is presented. Compared to the LDHBT-based circuit only half of the silicon area is required by the LDMOS inverter including control circuitry. Measurements prove the functionality of the developed high-voltage LDMOS inverter driven by the level shifter circuit. The timing of the control signals for the PLDMOS and NLDMOS transistor is not optimized, which causes an unnecessary cross current [88] during the switching event. To decrease this cross current an additional circuit, known as non-overlapping clock (NOC) circuit, can be implemented to realize the break-before-make (BBM)[89], [90] methodology.

5 Demonstrator Circuits

The developed circuit blocks: CP (section 4.2) and HV switch (section 4.4.2) are integrated in an RF-MEMS-based K-band SPDT switch presented in [30]. Two different HV generation and switching concepts are realized in these SPDT circuits and described in section 5.1.1 and section 5.1.2. In contrast to [30], the high-voltage generation and switching circuitries are integrated together with the RF-MEMS based SPDT switch in a single chip.
In section 5.2, an impedance tuning circuit based on RF-MEMS switches for the frequency range between 40 GHz and 60 GHz is presented. A single CP in combination with four HV switches is integrated in the demonstrator chip. The functionality of the designed RF-MEMS switches driven by the integrated HV circuitry is proven by measured S-parameters.

5.1 RF-MEMS-based SPDT Switch with On-Chip Actuation Circuitry

An RF-MEMS based SPDT switch is the simplest version of an RF multiway switch and used to route the RF signal between different functional blocks [91]. An SPDT switch is used to connect the antenna to the power amplifier (PA) or to the low noise amplifier (LNA) [12]. SPDT switches can also be found in phase shifter circuits [92] to route the RF signal to different delay lines. Furthermore, the SPDT switch is a core element of multipath RF switches (SPnTs). The layout of the RF signal line and the RF-MEMS switches for the two following SPDT switch demonstrator circuits is similar to [30] and therefore not further analyzed and described here. In contrast to this work, the RF-MEMS switch actuation voltage in [30] is provided by an external voltage source. The aim of the demonstrator circuits desribed in section 5.1.1 and section 5.1.2 is to show two different integrated HV generation and switching concepts and to emphasize the advantages and disadvantages using these topologies for MEMS matrix applications.

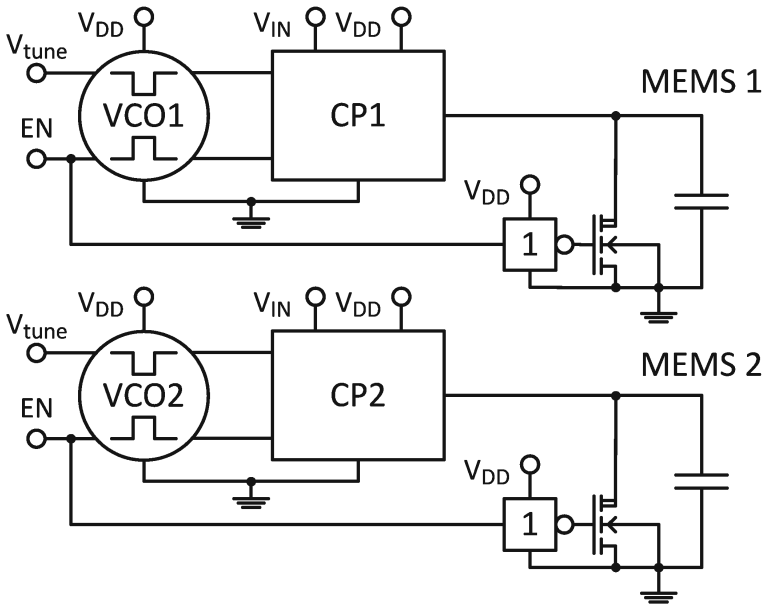


Figure 5.1: Block diagram of the high-voltage circuitry to actuate the MEMS independently. Each block consists of an oscillator, a charge pump and an NLDMOS transistor.

5.1.1 SPDT Switch Driven by Two Charge Pumps

In Fig. 5.1 an overview of the functional HV blocks (two RF-MEMS switches, two CPs, and two discharge NLDMOS transistors) is depicted. In contrast to [12], NLDMOS transistors instead of the energy consuming discharge resistors are integrated. The 12 stage CP is based on the topology described in section 3.2.2 and comprises the stacked metal capacitors described in section 3.1. HV NLDMOS transistors were integrated to replace the dis-CP, resulting in a minimized chip size required by the dual mode CP (Fig. 1.3). This will reduce the occupied CP chip area by a factor of two. The layout, including labels for the circuit and pads, is shown in Fig. 5.2. Filler structures are excluded to enable a detailed view of the chip. Extra pads are added for circuit analysis and testing purposes of the individual circuit blocks (CP, NLDMOS transistors). Without these pads, the number of required pads can be decreased to five (V_{DD}, V_{tune}, V_{IN}, Vg_nLD1&2). In Fig. 5.3, the micrograph of the fabricated circuit is shown. The total size of the SPDT switch including the pads is 1.38 mm^2. This is mainly caused by the RF components, since the HV blocks are placed inside the RF signal line. With the additional bias pads for the high-voltage generation circuitries, the overall chip size is increased by 8 %.

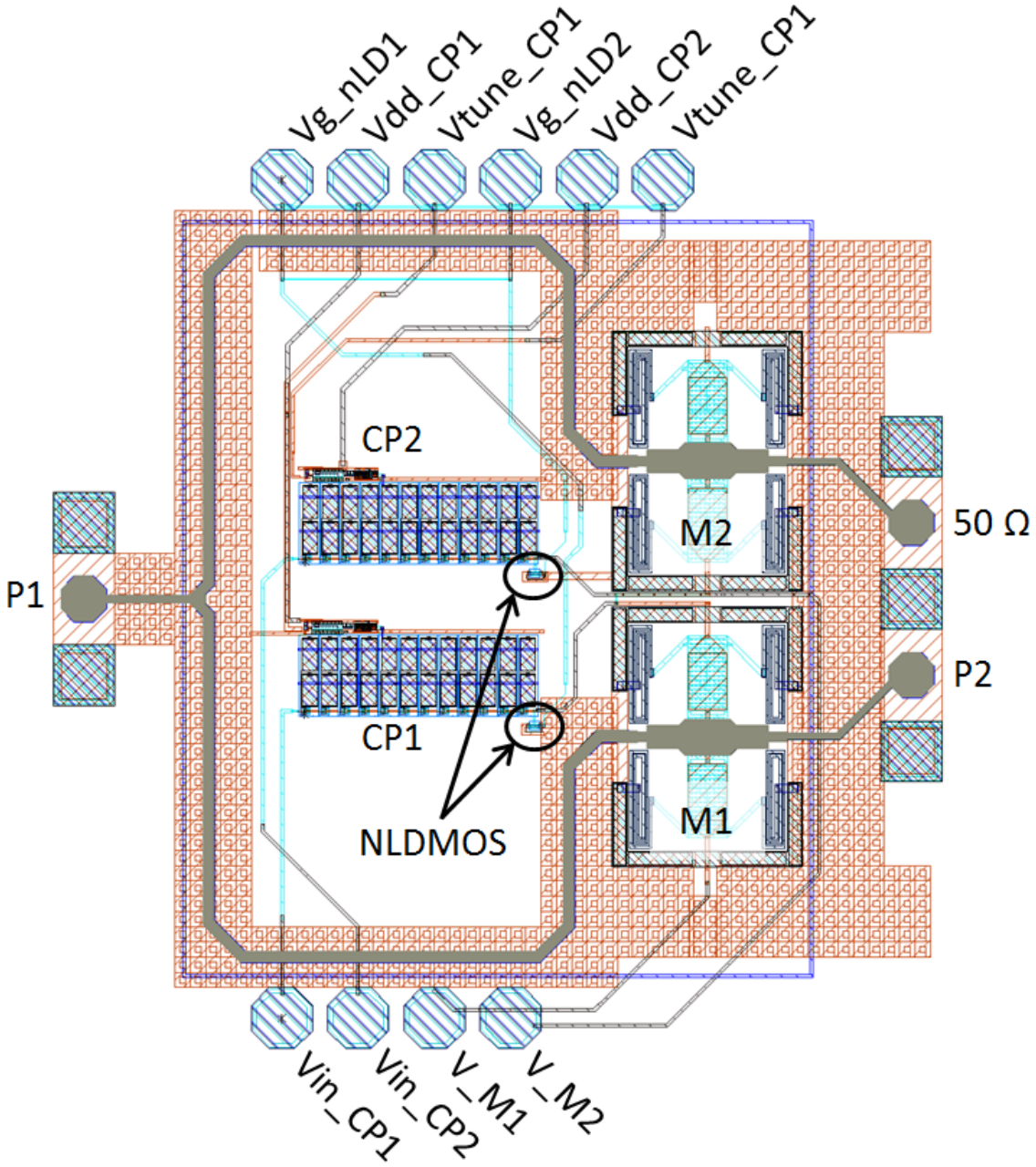


Figure 5.2: The layout of the designed SPDT switch with two independent "latched"- type charge pumps containing stacked metal capacitors. The discharge pumps are replaced by two HV NLDMOS transistors. The filler structures are not shown to enable the view on the circuit.

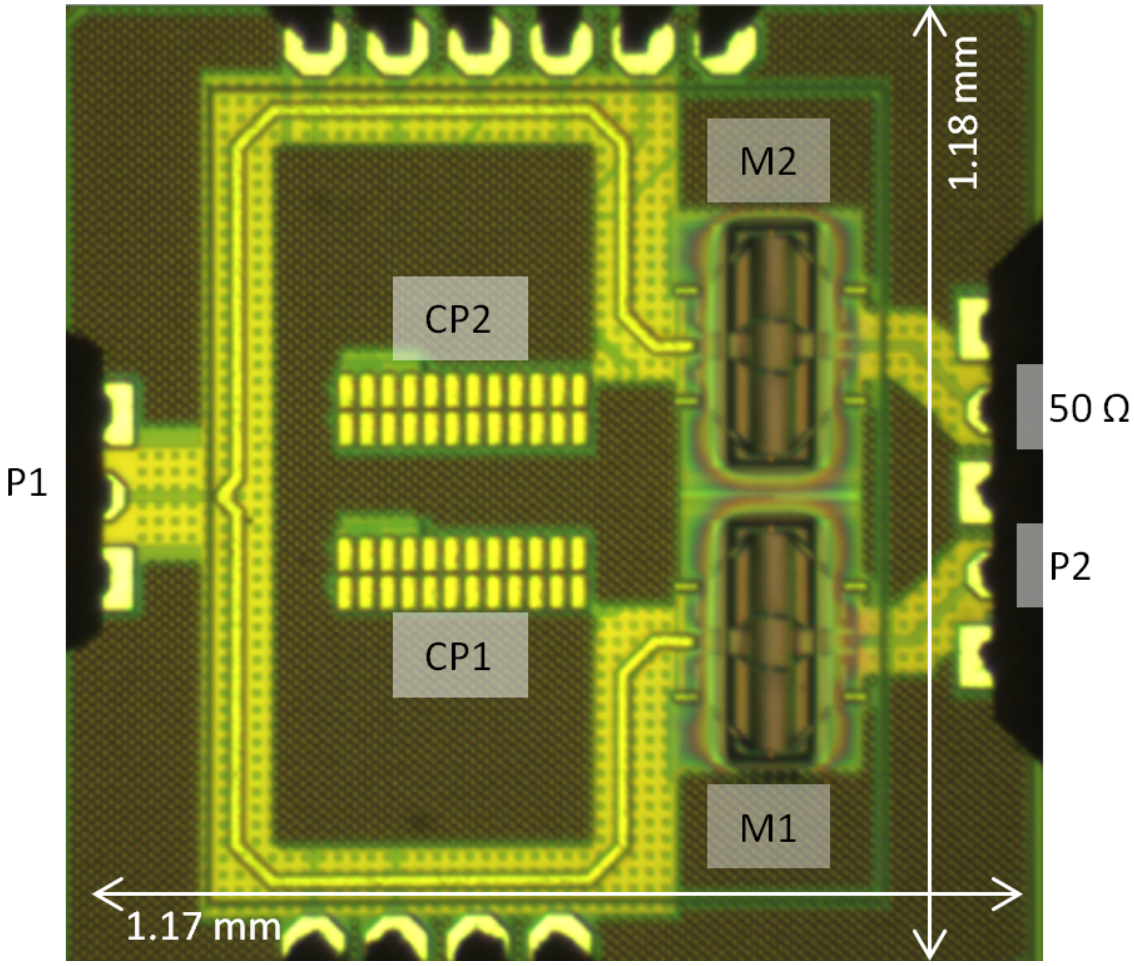
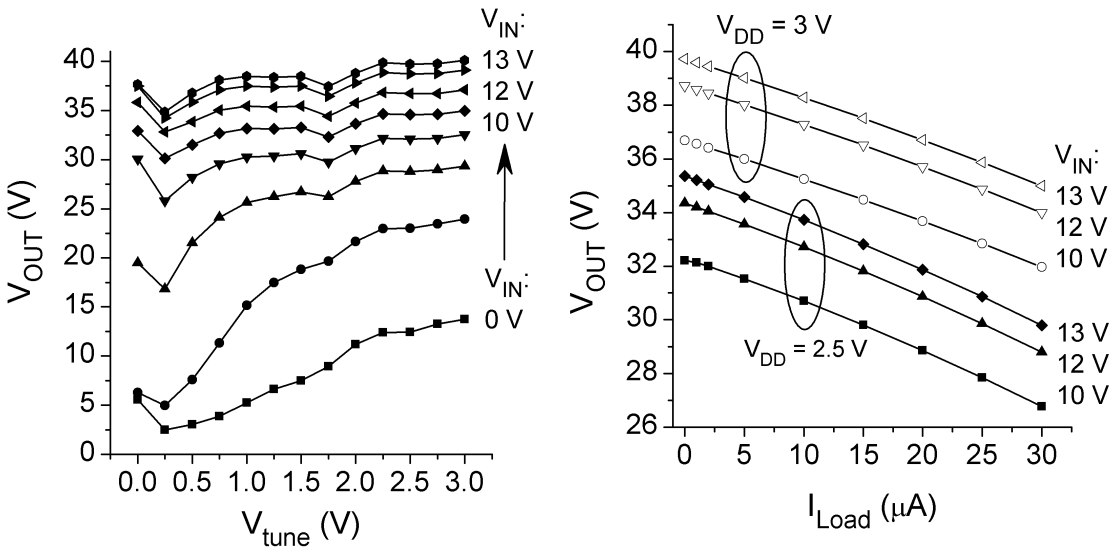


Figure 5.3: Chip micrograph of the fabricated RF-MEMS-based K-band SPDT switch circuit driven by two charge pumps (CP1, 2) and HV NLDMOS transistors to discharge the RF-MEMS switch electrode. The location of the HV NLDMOS transistors is shown in Fig. 5.2.



(a) (b)

Figure 5.4: (a) Measured CP output voltage (V_{OUT}) versus tuning voltage (V_{tune}) and input voltage (V_{IN}) with a constant biasing voltage (V_{DD}=3 V) and load current (I_{Load}=1 nA).
(b) Measured CP output voltage (V_{OUT}) versus load current (I_{Load}), input voltage (V_{IN}) and biasing voltage (V_{DD}) with a constant tuning voltage (V_{tune}=2.5 V). Using an SMU, the CP load current was set to values ranging from 1 nA to 30 µA.

Charge Pump Characterization

In Fig. 5.4 the output voltage of one integrated CP is depicted as a function of load current (I_{Load}), tuning voltage (V_{tune}), input voltage (V_{IN}) and bias voltage (V_{DD}). Measurements show that the implemented CP can generate and handle an output voltage of 40 V. In Fig. 5.4(a) a nonlinear increase of the CP output voltage (V_{OUT}) with a linearly increasing V_{IN} is measured. This behavior could not be verified by circuit simulation. For an input voltage V_{IN}=2 V, the tuning range of the CP output voltage is 15 V. The output voltage is inversely proportional to the drawn output current (Fig. 5.4(b)) e.g. providing 40 V with 1 nA load current and 36 V with a load current of 30 uA. An output voltage of 25 V can be achieved by setting V_{IN}=4 V, V_{tune} and V_{DD}=2.5 V and I_{Load}=1 nA. In order to achieve an output voltage of 40 V while keeping V_{IN} in the range of V_{DD}, the number of CTSs must be increased from 12 to 20.

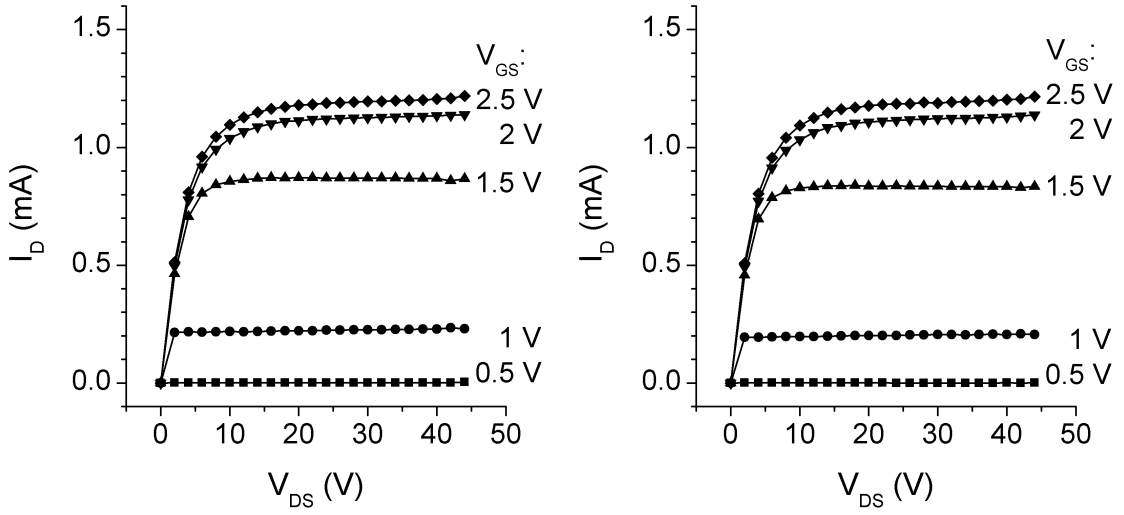


Figure 5.5: In situ measured forward output characteristics (drain current (I_D) versus drain-source voltage (V_{DS}) and gate-source voltage (V_{GS})) of both discharge NLDMOS transistors. The equivalent discharge resistance at 40 V is 33 kΩ.

DC Characterization of the Integrated NLDMOS Transistors

To prove the successful implementation of the NLDMOS transistors as a functional replacement for the dis-CP, the DC characteristic was measured. The total gate width of the NLDMOS transistors is 5.3 µm. The in situ measured forward output characteristics are depicted in Fig. 5.5. At V_{DS}=40 V, a maximum drain current ($I_{D,max}$) of 1.2 mA can be driven by the symmetric double gate (see cross-section in Fig. 2.2) NLDMOS transistors. This discharge current is equivalent to a current caused by a resistor with 33 kΩ and results in a shortened MEMS release (switch off) time. In [17], a release time of less than 25 µs is achieved by the integration of a 250 kΩ discharge resistor.

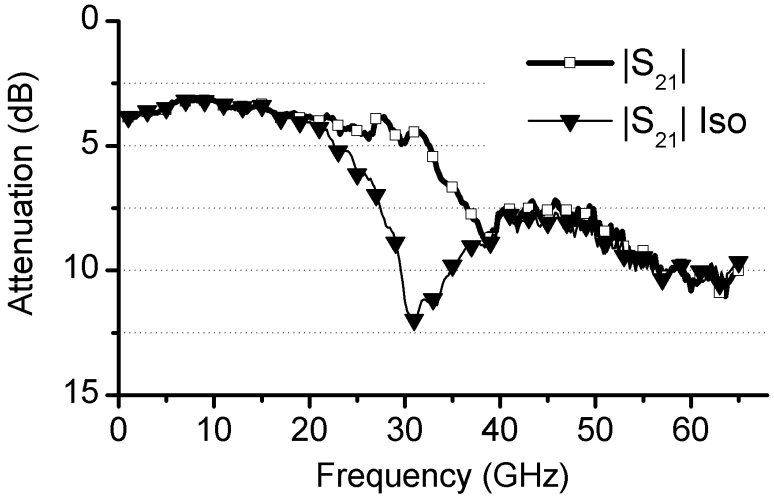


Figure 5.6: Measured signal attenuation of isolation state ($|S_{21}|$ Iso) and transmission state ($|S_{21}|$) between port1 and port2. The port numbers are indicated in the chip micrograph in Fig. 5.3.

Functional Testing of the Demonstrator Chip

To demonstrate the successful implementation and functionality of the CP and the NLDMOS transistors, the 2-port S-parameters of the RF-MEMS-based SPDT switch were measured. To measure a three terminal SPDT switch with a two port 67 GHz vector network analyzer (VNA), one output was terminated with a 50 Ω load resistor (see Fig. 5.2 or Fig. 5.3) connected to the second signal connector of the ground signal ground signal ground (GSGSG) RF probe. An impedance standard substrate (ISS) compatible with a GSG and a GSGSG RF probe was chosen to perform the Short open load thru (SOLT) calibration. The measured S-parameter represented by S_{21} in dB is depicted in Fig. 5.6. It can be clearly distinguished between the isolation state (M1-active & M2-up) and the transmission state (M1-up & M2-active), which verifies the operation of both CPs and both NLDMOS transistors.

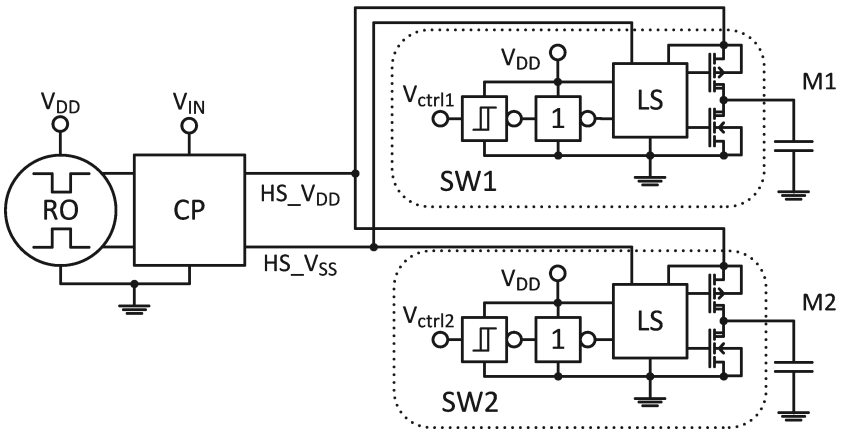


Figure 5.7: Block diagram of a single (shared) high-voltage generation circuitry (CP) and two HV switches (SW1, 2). The CP constantly provides two output voltages (HS_V_{DD} and HS_V_{SS}) to bias the level shifters and the LDMOS inverters.

5.1.2 SPDT driven by a Single Charge Pump and two HV Switches

In contrast to MEMS matrix applications where the multiple CP approach used in the previous section requires too much chip area, the same RF-MEMS-based SPDT switch is actuated using a single CP in combination with two HV switches. An overview with the functional blocks is depicted in Fig. 5.7: a CP (section 4.2) powered by a RO (section 4.1) and two HV switches (section 4.4.2) to actuate two RF-MEMS switches.

The layout of the designed circuit including pad labels is depicted in Fig. 5.8. In order to enable a detailed view into the circuit and its functional blocks, the filler structures are not shown. In Fig. 5.9 the chip micrograph is depicted. Since the HV circuitry is placed inside the RF signal line, like in the first demonstrator circuit (section 5.1.1), the chip size is 1.38 mm^2.

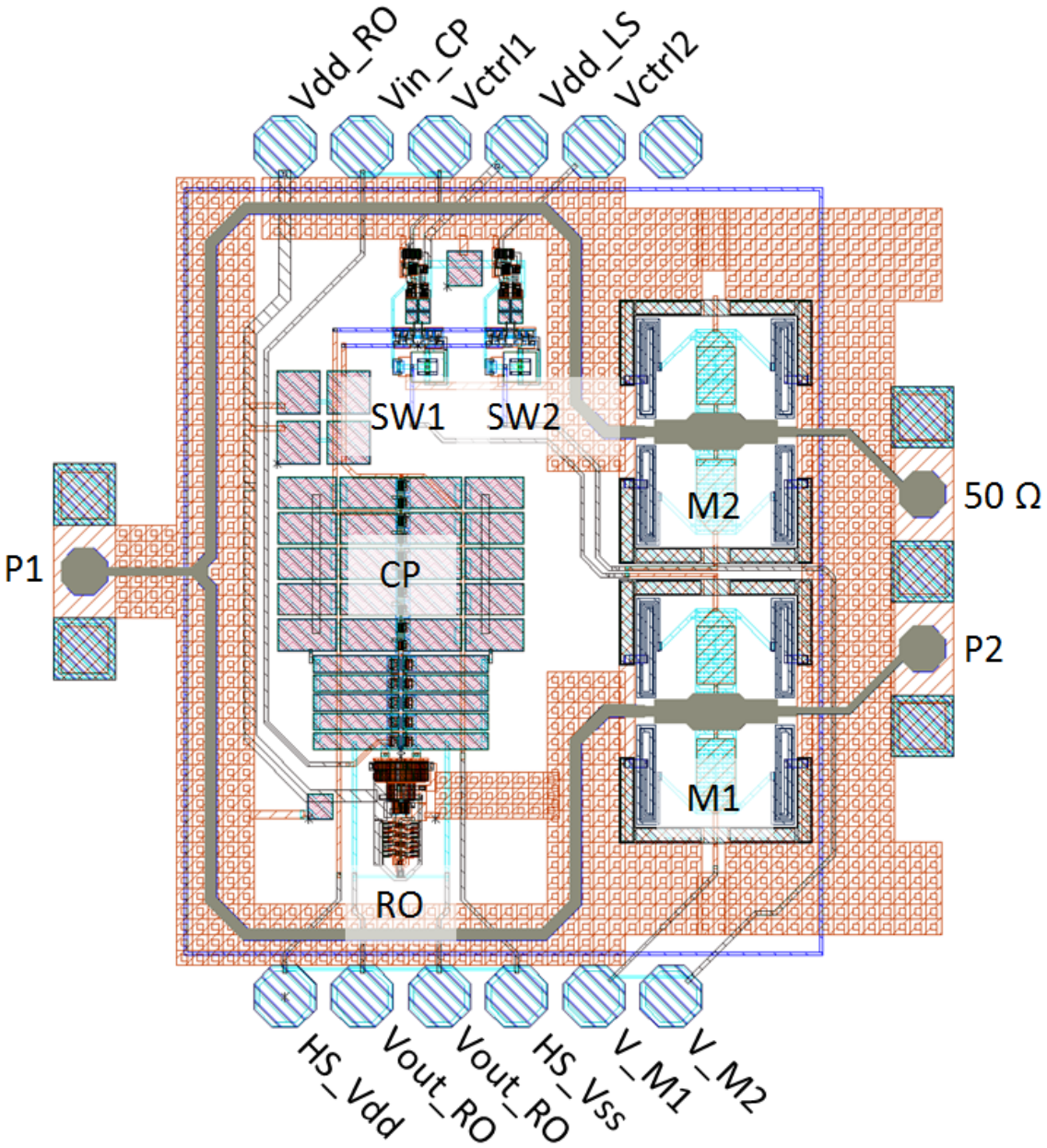


Figure 5.8: Layout of the designed SPDT based on two RF-MEMS switches (M1, M2), charge pump (CP), ring oscillator (RO) and two high-voltage switches (SW1, SW2). The two RF ports of the VNA are P1 & P2. To show more details of the circuit, the filler structures are faded out.

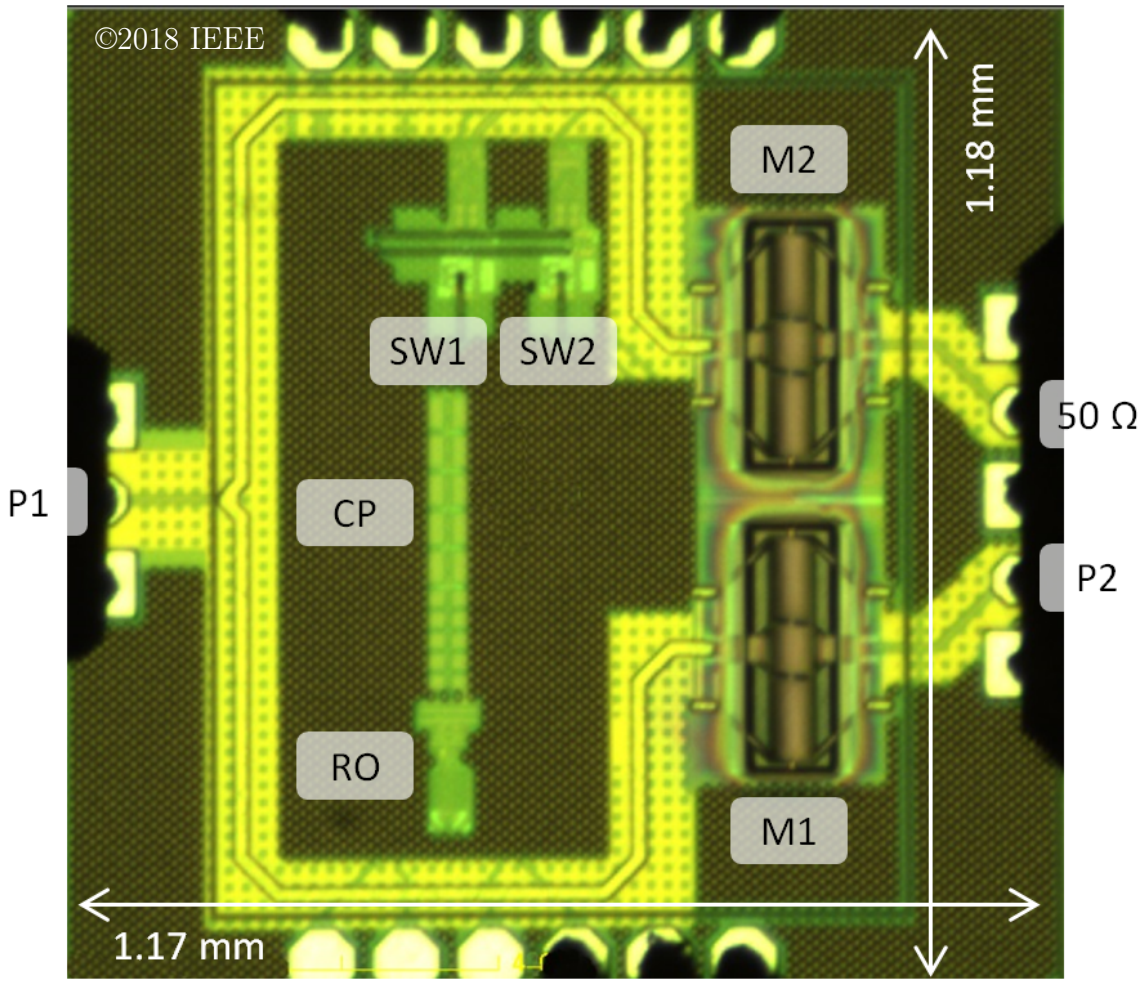


Figure 5.9: Chip micrograph of the fabricated RF-MEMS-based K-band SPDT switch circuit including two LDMOS inverters (SW1,2), one charge pump (CP) and a differential ring oscillator (RO) [44].

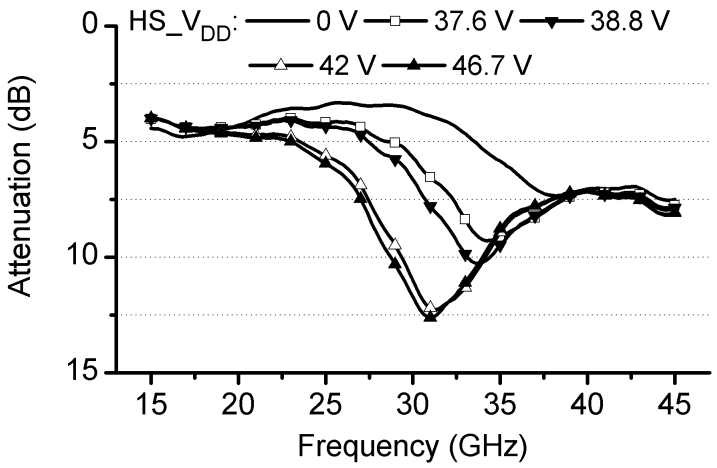


Figure 5.10: Measured RF signal attenuation for the isolation state ($|S_{21}|$) between port1 (P1) and port2 (P2) for different actuation voltages.

Functional Testing of the Demonstrator Chip

To demonstrate the whole system, two-port S-parameters up to 65 GHz were measured on-wafer to test the successful actuation of both RF-MEMS switches of the SPDT. The remaining RF pad was terminated with 50 Ω. A two-port Agilent vector network analyzer (E8361A) was calibrated using a differential impedance standard substrate applying the SOLT method.

The on-chip charge pump (CP) provides the actuation voltage for the embedded RF-MEMS switches and the bias voltage for the HV switches. To define the optimum RF-MEMS switch actuation voltage, the RF signal attenuation (S_{21}) for different charge pump bias conditions was measured. Since the output voltage (HS_V_{DD}) of the charge pump varies with the clock frequency and amplitude of the ring oscillator, the bias voltage (V_{DD}) of the RO was swept starting from 2.5 V up to 2.9 V to find the optimum bias voltage. The measured RF signal attenuation versus CP output voltage is depicted in Fig. 5.10. Increasing the CP output voltage from 42 V to 46.7 V does not result in an increased attenuation. Thus, the on-chip RO and the charge pump (V_{IN}) were biased at 2.7 V to generate a voltage of 42 V. In continuous operating mode, the measured current consumption of the ring oscillator and the charge pump was 9.6 mA.

In Fig. 5.11, the signal attenuation from port1 (P1) to port2 (P2) depending on the SPDT switch state are depicted. The port numbers are shown in Fig. 5.9. The measured S-parameters demonstrate the successful actuation of the integrated RF-

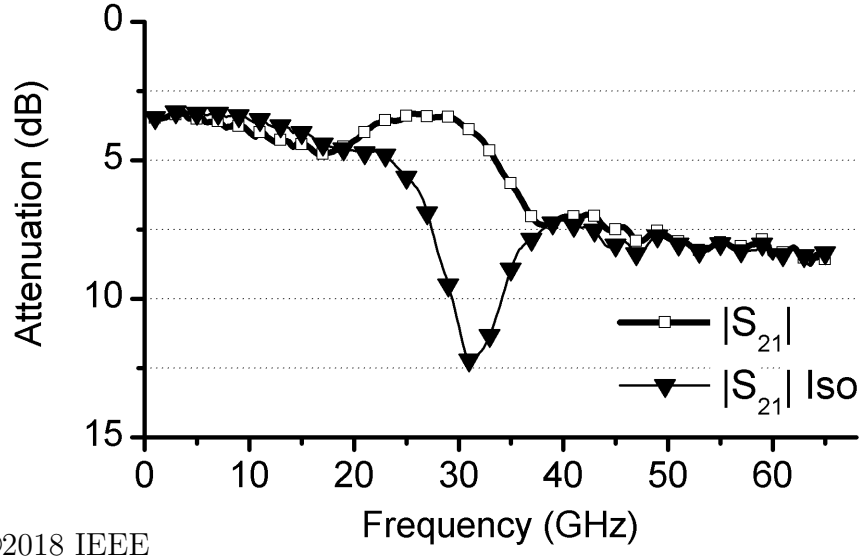


Figure 5.11: Measured RF signal attenuation of the isolation state ($|S_{21}|$Iso) and the transmission state ($|S_{21}|$) between port1 and port2. The port numbers are shown in the chip micrograph in Fig. 5.9. The measurement proves the successful actuation of both RF-MEMS included in the SPDT switch [44].

MEMS switches. The difference between the transmission and isolation-state at 30 GHz is 14 dB. This value clearly verifies the functionality of the integrated CP and the high-voltage switches.

5.1.3 Conclusion

Both high-voltage generation and switching concepts, implemented in the presented demonstrator vehicles, show successful operation. If an NLDMOS transistor with sufficiently high breakdown voltage is available, the dis-CP can be replaced. Thus, the silicon area required by the HV generation circuitry will be halved. The drawback is that the NLDMOS requires two extra masks and therefore additional preparation effort and costs. It depends on the available process modules (HV transistors) and the designer's preferences to use the double-CP approach or using a single CP in combination with HV switches. If building blocks for the CP and the HV inverter are available as a library element in the PDK, the design effort for both RF-MEMS switch SPDT demonstrators is reduced to "place and route".
For the K-band SPDT switch with the relatively long RF signal lines (quarter wavelength $\lambda/4$), the RF-MEMS switch actuation circuits in both demonstrator systems could be placed "inside" the RF- signal line. Thus, the layout area required in both cases (with and without HV circuitry) is similar. Nevertheless, the layout area required by the latched CP, used in section 5.1.1, will be increased for future designs, since the number of stages needs to be increased to increase the output voltage. For higher frequency applications with shorter RF signal lines, the HV generation and switching circuitries have to be placed in close proximity to the RF components. It can be concluded that for applications comprising only two RF-MEMS switches, the layout area required by the double- or single CP concept is similar.

5.2 RF-MEMS-based Impedance Tuner with On-Chip Actuation Circuitry

Impedance tuning systems based on stubs or distributed MEMS transmission lines (DMTLs) are used at higher frequencies [4], [93], [94]. RF-MEMS-based V- and W-band impedance tuners comprising several switched MEMS capacitors are described in [95], [96]. These double- and triple-stub impedance tuners are small enough to fit into a wafer probe used for on-wafer noise parameter and load-pull measurements [97], [98]. Those circuits do not have an integrated HV generation and switching circuitry which would simplify the wiring effort and reduce the number of cables required to control the integrated RF-MEMS switches attached to the small wafer probe. An integrated high-voltage generation and switch matrix controlled via a serial bus interface would significantly reduce the wiring effort. To demonstrate a fully integrated system, a V-Band single-stub impedance tuning circuit comprising four RF-MEMS switches, a charge pump and the essential HV switches is developed and fabricated. The designed circuit has 16 possible states starting from all RF-MEMS switches in up-position and ending with all MEMS in down-state (actuated). Since the integrated HV switches are controlled applying CMOS voltage levels of 2.5 V, the presented system can be combined with a serial bus interface (e.g. inter-integrated circuit bus (I^2C) or SPI). The on-chip generated charge pump output voltage is measured and the function of the high-voltage switching and generation circuitry is shown by the measurement of the S-parameters for various activation states of the integrated RF-MEMS switches.

5.2.1 Circuit Description

The RF signal line is designed as a T-structure (single stub) with the open end connected to ground. Four RF-MEMS switches acting as switchable capacitors are placed along the RF signal line. An actuated RF-MEMS switch will increase the capacitive coupling between the signal line and ground, resulting in a change of the scattering parameter of the stub.

A side effect of the shorted circuit stub topology is the protection of the VNA ports from high DC voltages. This is the worst case scenario with low probability because the MEMS electrodes are coated with an isolating layer and the membrane of the RF-MEMS switch is connected to ground. Even the on-chip charge pump is

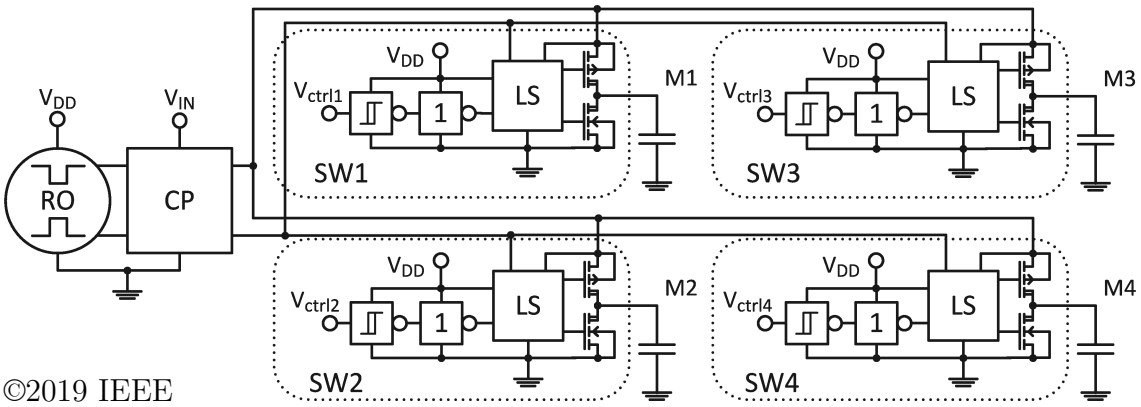


Figure 5.12: Block diagram of the high-voltage switch matrix to control the RF-MEMS switch based impedance tuner chip. The circuit includes four LDMOS-based HV switches (SW1–4) biased by a single CP [45].

possibly not powerful enough to destroy the bias tees of the VNA. But this depends also on the charge stored in the on-chip capacitors and in the coaxial cables of the measurement setup.

The block diagram of the designed HV generation and switching circuitry is shown in Fig. 5.12. A single CP provides the bias voltage for the four HV switch units (SW1–4). The HV switch units consist of a Schmitt-Trigger, an inverter, a level shifter and the LDMOS output stage.

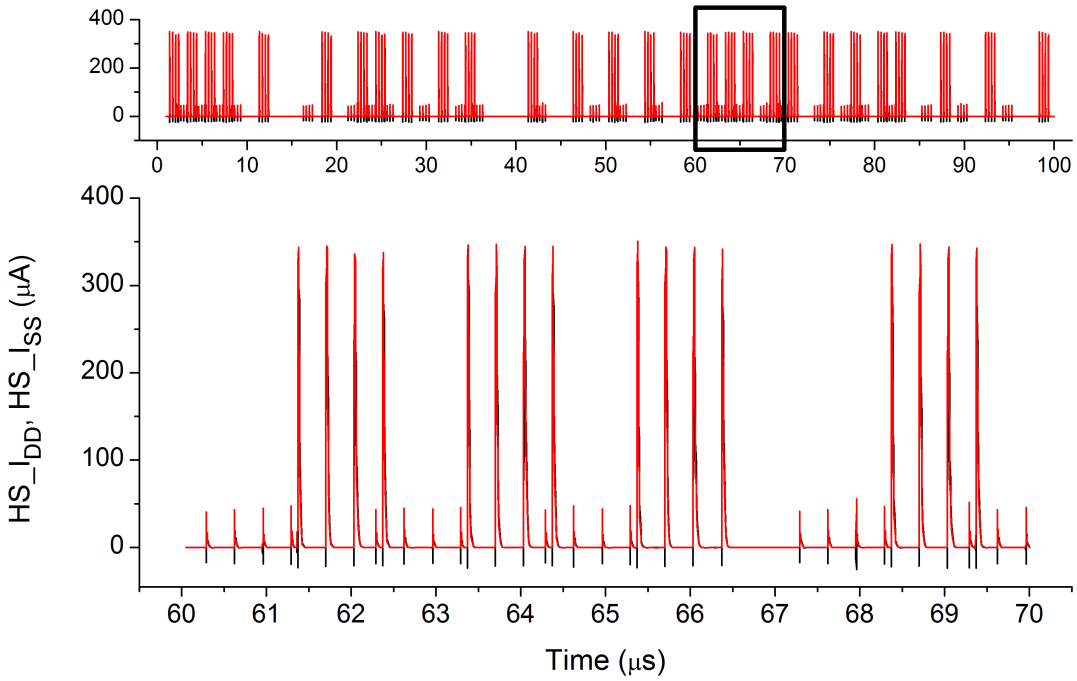


Figure 5.13: Transient simulation of the CP output currents (HS_I_{DD}, HS_I_{SS}). All four HV switches are controlled by a random signal. The mean current of HS_I_{DD} is 37.6 µA and 19.5 µA for HS_I_{SS}.

5.2.2 Circuit Simulation and Layout

To estimate the current drawn from the on-chip charge pump, a transient circuit simulation is performed and the results are depicted in Fig. 5.13. The four high-voltage switches are controlled by a random signal. Every switching event causes a peak current in the range of 350 µA which results in a mean current of 37.6 µA for HS_I_{DD} and 19.5 µA for the HS_I_{SS} output. To decrease the amplitude of the current peaks, the overlap of the NLDMOS and PLDMOS transistor control signals must be reduced by the integration of BBM logic.

A chip micrograph of the fabricated impedance tuner is depicted in Fig. 5.14. Most of the DC pads are used to characterize the sub-circuits (RO, CP, SW1–4) and are not required to operate the circuit. The impedance tuner can be operated using only six pads (VDD_RO, VDD_INV, Vctrl1–4). Integrating an SPI with its four signal lines (master out slave in (MOSI), master in slave out (MISO), serial clock (SCLK) and slave select (SS)) would not increase the total number of pads (cables), since Vctrl1–4 are now controlled by the SPI.

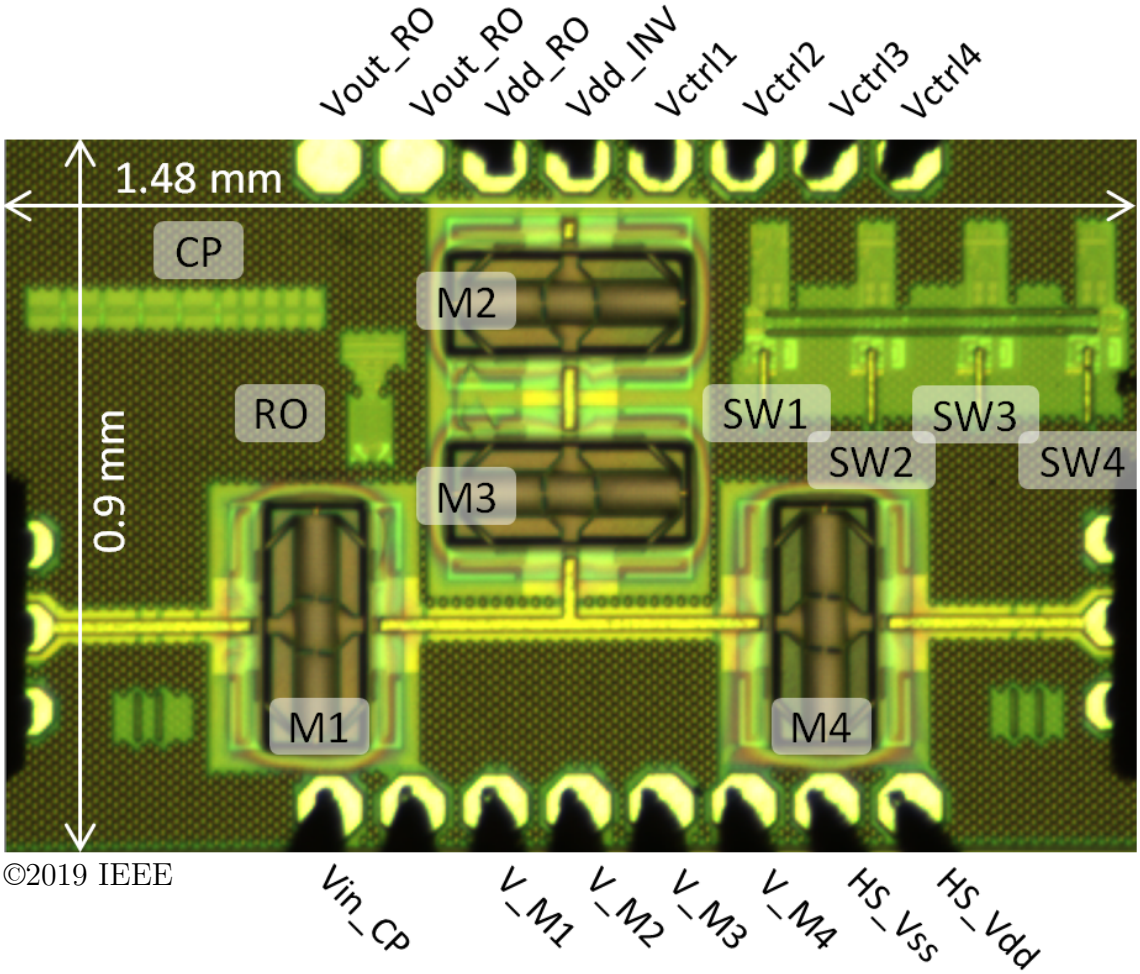


Figure 5.14: Chip micrograph of the fabricated RF-MEMS (M1–4) based impedance tuner circuit including four LDMOS inverters (SW1–4), a differential ring oscillator (RO) and the charge pump (CP) [45]. The obligatory filler structures are partly hiding the control circuitry.

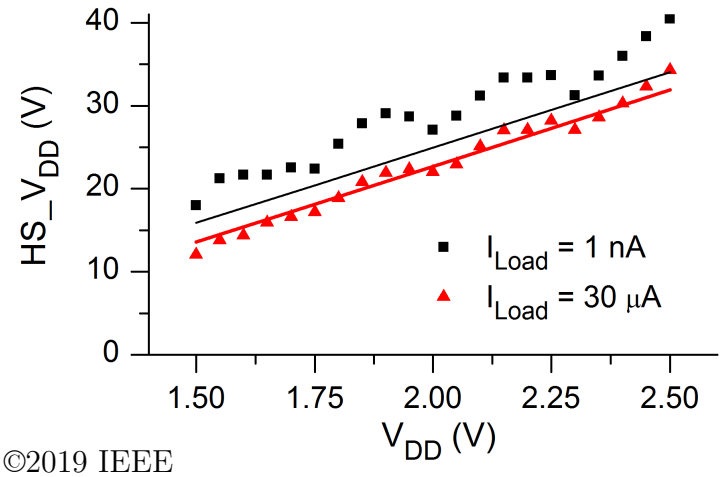


Figure 5.15: Measured (symbols) and simulated (line) CP output voltage (HS_V_{DD}) versus bias (V_{DD}) for different load currents (I_{Load}). The CP input voltage (V_{IN}) is synchronized with V_{DD} [45].

5.2.3 Circuit Characterization

To test the CP for different load conditions, an output current was forced using a source measurement unit (Agilent E5270B). The measured and simulated output voltage of the integrated CP for different bias voltages (1.5 V≤Vdd≤2.5 V) and load conditions (ILoad=1 nA, 30 µA) is depicted in Fig. 5.15. The ripple in the CP output voltage can be explained by the bias (Vdd) dependency of the clock frequency and amplitude. Since the charge pump is optimized for a certain clock frequency, the generated voltage is decreasing with an increasing clock signal. However, this effect is partly compensated with the increased clock amplitude. With a bias voltage of 2.5 V an output voltage in the range of 40 V is measured. Compared to the data shown in Fig. 4.21, this CP is connected to the integrated HV switching circuitry. Hence, it is providing in addition to the load current (ILoad), the bias current for the integrated circuitry. The influence of an increased load current (ILoad) (Fig. 5.16) results in a decreased output voltage and causes an increased bias current. This current level is reached with a high switching frequency as shown in Fig. 5.13 or with the switching of several high-voltage switches simultaneously. As expected, the bias current (I_{DD}), which is depicted in Fig. 5.16, is increasing with increasing ring oscillator bias voltage (Vdd).

In Fig. 5.17, a more detailed view on the dependency of the generated output voltage (HS_V_{DD}) versus the bias voltage (V_{DD}≥2.5 V) of the ring oscillator is depicted. For these measurements, the charge pump input voltage (V_{IN}) was synchronized with

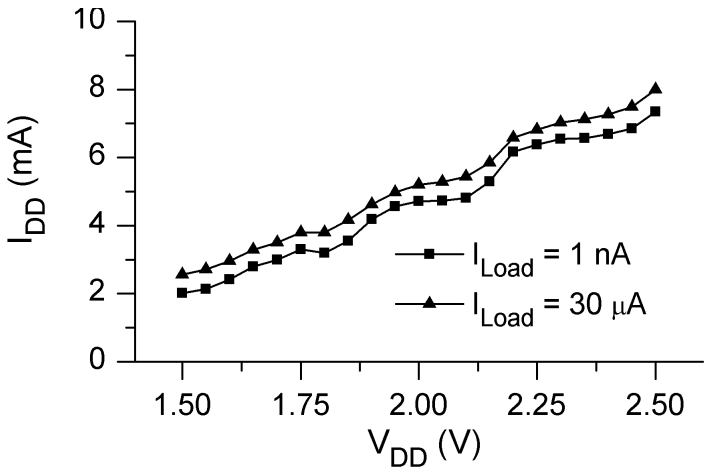


Figure 5.16: Measured current consumption (I_{DD}) versus bias voltage (V_{DD}) and load current (I_{Load}) of the chip (CP + LS + RO).

the bias voltage (V_{DD}) and the external load current was kept below 1 nA. The generated CP output voltage is very sensitive on the supply voltage (V_{DD}) of the RO. A change of V_{DD} from 2.48 V to 2.54 V results in a raise of 4 V at the CP output voltage. The measured change in the generated output voltage is larger than the expectations based on the simulation results shown in Fig. 4.19(a). This can be explained with the measured CP output voltage ripple shown in Fig. 5.15. In continuous operating mode, the measured current consumption of the ring oscillator and the charge pump ranges from 8.2 mA (V_{DD} = 2.48 V) up to 8.4 mA (V_{DD} = 2.54 V). With a bias voltage of V_{DD} = 2.5 V an output voltage (HS_V_{DD}) of 38.4 V is measured.

As the final demonstration of the whole system, S-parameters up to 67 GHz were measured on-wafer to test the successful actuation of the embedded RF-MEMS switches. For the on-wafer S-parameter measurements, a two-port vector network analyzer (Agilent E8361A) was calibrated using an impedance standard substrate applying the SOLT method. The measured RF signal reflection S_{22} of the impedance tuning chip with all RF-MEMS switches actuated is depicted in Fig. 5.18. The odd values for the generated voltage (HS_V_{DD}) listed in the plot are due to the swept bias (V_{DD} = 0 V, 2.48 V – 2.54 V) of the oscillator. The high-pass characteristic of the shorted stub transmission line causes a large RF signal reflection at frequencies below 10 GHz. For measurement frequencies above 20 GHz, the influence of the actuation voltage (HS_V_{DD}) on the circuit behavior is obvious. A decreasing small signal reflection (S_{22}) with increasing actuation voltage is measured. Thus, the state

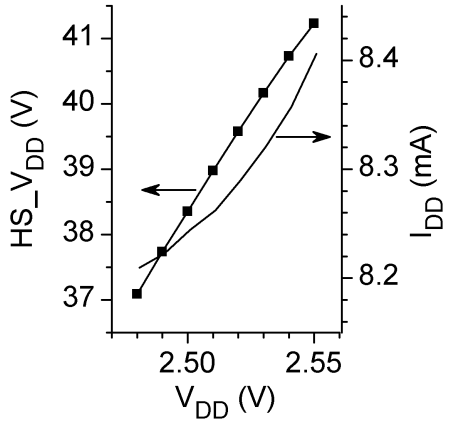


Figure 5.17: Measured CP output voltage (HS_V_{DD}) and current consumption (I_{DD}) depending on the bias condition (V_{DD}) of the RO.

"M1234_dn" (M1,2,3,4: down-state) causes a broadband matching in the Ka-band (27 – 40 GHz). Increasing the actuation voltage above 40.2 V does not improve the signal reflection (S_{22}) significantly. Therefore, for further S-parameter measurements the on-chip ring oscillator is biased at $V_{DD} = 2.53$ V to generate a charge pump output voltage of 40.2 V.

In Fig. 5.19, the small signal reflection S_{22} for eight selected RF-MEMS switch acutation states is depicted. The state "M1_up_M234_dn" (M1: up-state; M2,3,4: down-state) causes a strong resonance at 41 GHz for S_{22}. On the other hand, if M2 is deactivated while the state of M1,M3 and M4 are kept unchanged (state "M12_up_M34_dn"), the optimum matching frequency is shifted to 45 GHz. Resonances for S_{11} and S_{22} can be created at similar frequencies with complementary RF-MEMS actuation states. Exchanging the state of M4 and M1 while M2 and M3 remain unchanged will cause a resonance at the same frequency at the opposite port. The state "M34_up_M12_dn" (M3, 4: passive (low capacitance) and M1, 2: active (high capacitance)) causes a minimum signal reflection (S_{11} in Fig. 5.20) at 48 GHz. The small differences between S_{11} and S_{22} can be explained with the performance difference of the RF-MEMS switches as a result of process variations. The measured S-parameters of the impedance tuner circuit prove the HV generation and switching, resulting in an individual actuation of the integrated RF-MEMS switches.

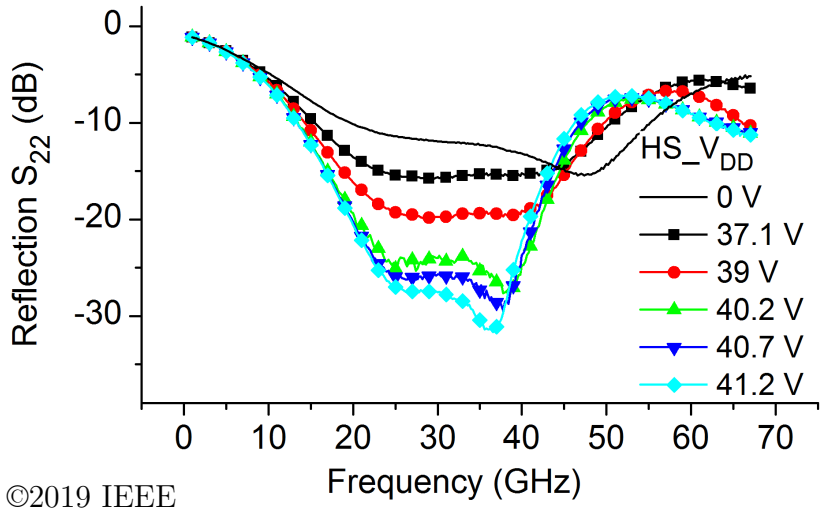


Figure 5.18: Measured RF signal reflection (S_{22}) of the impedance tuning circuit versus frequency for different CP output voltages (HS_V_{DD}). All RF-MEMS switches are actuated [45].

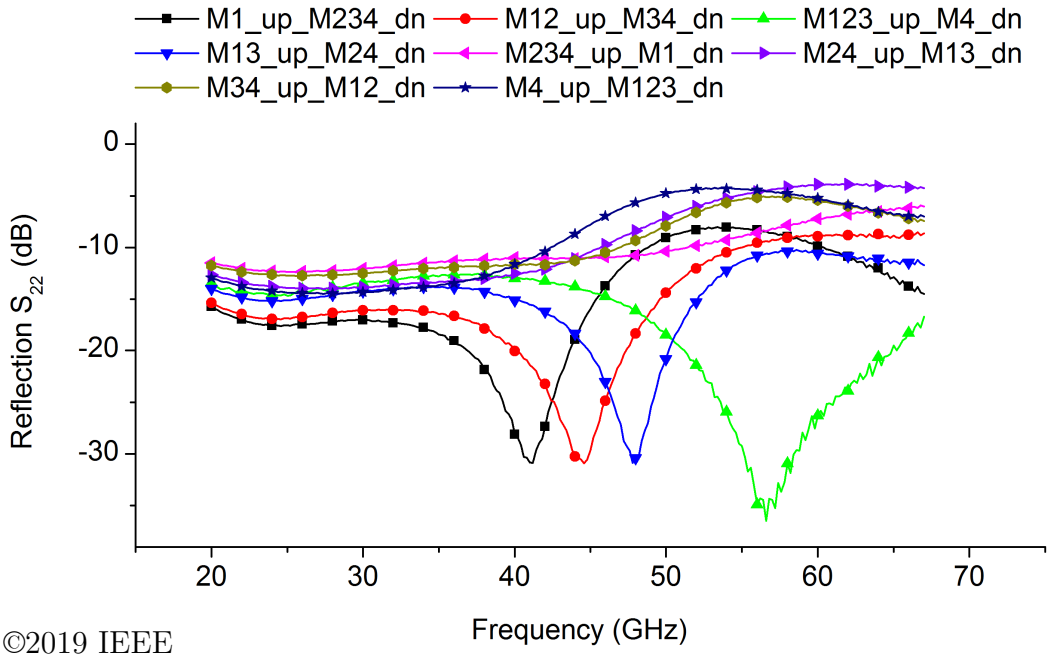


Figure 5.19: Measured RF signal reflection (S_{22}) for different RF-MEMS switch actuation states. The complementary impedance state for "M1_up_M234_dn" is "M4_up_M123_dn" (Fig. 5.20) [45].

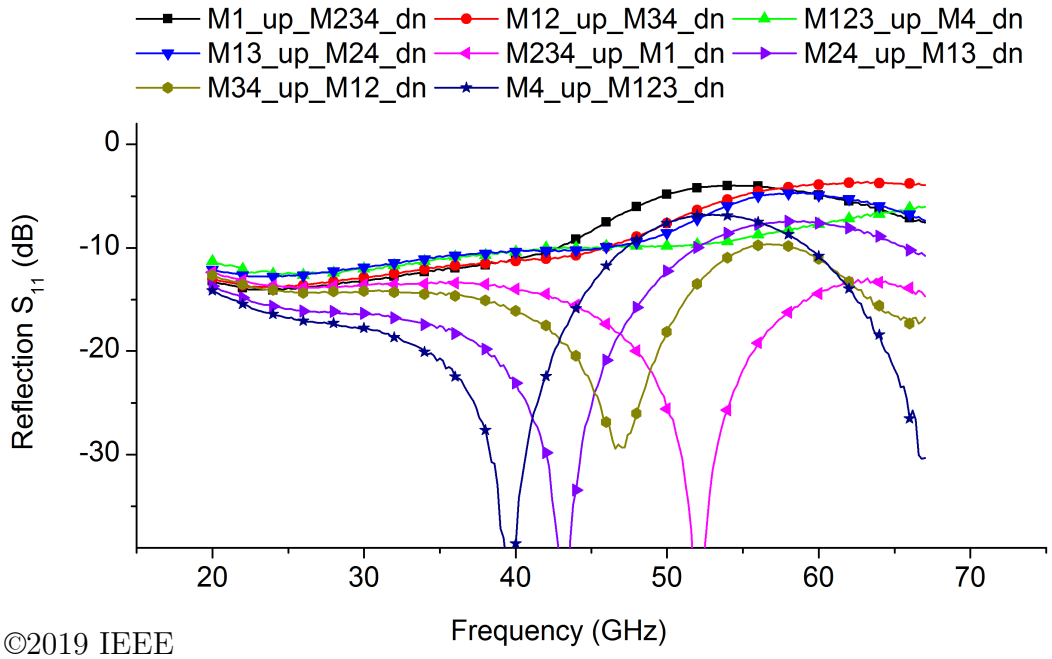


Figure 5.20: Measured RF signal reflection (S_{11}) for different RF-MEMS switch actuation states. For the state "M1_up_M234_dn" the RF-MEMS switch1 is not active and the RF-MEMS switch2, 3, 4 are activated [45].

5.2.4 Conclusion

The demonstrator chip: an impedance tuning circuit in the V-band (40 – 75 GHz), containing a charge pump and four LDMOS-based HV switches driving the four integrated RF-MEMS switches is realized and successfully tested. Four compact LDMOS inverters including a driver circuit (capacitively coupled level shifter) are integrated in the circuitry. Voltages in the range of 40 V are generated and switched on-chip. Depending on the combination of activated RF-MEMS switches, the matching frequency can be changed. A higher number of impedance states, required for on-wafer load-pull and noise parameter measurements, can be achieved by increasing the number of RF-MEMS switches and HV switches. The measured S-parameters demonstrate the individual actuation of the embedded RF-MEMS switches controlled by the integrated high-voltage switches while the CP is constantly providing the actuation voltage for the RF-MEMS switches and the bias voltage for the four HV LDMOS inverters.

6 Conclusion and Outlook

In this work, building blocks required to control electrostatically actuated RF-MEMS switches were developed and integrated in demonstrator circuits. These chips include the HV generation and switching units integrated together with the RF-MEMS switches. To the author's knowledge, monolithically integrated RF systems for operating frequencies greater than 20 GHz consisting of RF-MEMS switches, on-chip high-voltage generation circuits and a high-voltage switch matrix are presented for the first time. Regarding MEMS matrix applications, the usability of the following two approaches were analyzed and realized:

- one CP per MEMS
- single CP and multiple HV switches

The CPs designed in this work are based on the "modified Dickson" and "Latched" topology and voltages greater than 40 V were generated on-chip. LV PMOS transistors were used in the charge transfer stages of the Dickson CP. This topology yields the best trade-off between layout area, output voltages (main (HS_V_{DD}) and secondary (HS_V_{SS})), voltage offset (HSΔ = HS_V_{DD} - HS_V_{SS}), voltage ripple of HSΔ and output impedance.
The implemented ring oscillator consists of 9 differential inverter stages based on DCVSL logic. Since the charge pump was designed for a clock frequency of 300 MHz, the ring oscillator was designed accordingly.
A simple HV switching circuit based on three HV npn HBTs and two resistors was evaluated. Further improvements are mandatory to decrease the leakage current drawn from the CP in discharge mode. Due to the breakdown behavior for emitter-substrate voltages (V_{ES}) >5 V, the high-voltage LDHBTs must be placed in an isolated p-well. Since such an isolated high-voltage LDHBT is currently not available, the developments based on the LDHBT transistor have to be postponed. Alternatively, an LDMOS-based high-voltage switch was designed and integrated in the demonstrator chips. For applications requiring very fast actuation of the embedded RF-MEMS switches, the LDMOS inverter concept in combination with

a single CP has proven to be the best choice. To drive a HV PLDMOS transistor, a fast level shifter with a quiescent current leakage below 500 nA was designed. Transient simulations of the level shifter core show very short rise and fall times in the range of 200 ps. The measurements prove a reliable operation for a broad range of bias voltages from 6 V up to 42 V while the switching speed of the circuit remains stable.

A compact LDMOS inverter including the driver circuit (LS) with a chip size of 160 µm x 80 µm is presented. Currently, the timing of the control signals (BBM methodology) for the PLDMOS and NLDMOS transistor is still not optimal, which causes high cross currents during the switching event.

The functionality of the HV generation and switching circuitries implemented in both SPDT demonstrator vehicles could be successfully verified. By replacing the discharge element in the CP by an NLDMOS transistor, the silicon area required by the HV generation circuitry is halved. For applications comprising only two RF-MEMS switches, the layout area required by the double- and the single shared CP concept is comparable.

The third demonstrator circuit: an impedance tuning circuit in the V-band (40 – 75 GHz), containing a single CP and four LDMOS-based HV switches controlling the four integrated RF-MEMS switches was realized and tested successfully. The actuation of the RF-MEMS switches was proven by the S-parameter measurements for various combinations of actuated RF-MEMS switches.

The presented HV generation and switch matrix approach can also be integrated in other applications such as electrostatically or piezoelectrically actuated valves or pumps in microfluidics.

The efficiency of the HV generation circuitry can be further improved. By integrating a capacitive voltage divider connected to the CP output, a feedback signal can be generated to control the clock signal generator, resulting in a decreased power consumption while the CP output voltage remains constant. The cross current in the HV inverter can be further reduced by implementing additional logic (BBM methodology) to minimize the overlapping of the control signals for the NLDMOS and PLDMOS transistors.

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List of Figures

List of Tables

Eidesstattliche Erklärung

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