^{28}Si, Ge Epitaxy for Qubits

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an der Fakultät II - Mathematik und Naturwissenschaften
der Technischen Universität Berlin
zur Erlangung des akademischen Grades

Doktor der Ingenieurwissenschaften
- Dr. Ing. -

genehmigte Dissertation

Promotionsausschuss:

Vorsitzender: **Prof. Dr. Michael Lehmann**
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Tag der wissenschaftlichen Aussprache: 14. März 2023

Berlin 2023

Abstract

Silicon (Si), Germanium (Ge) related materials such as SiGe heterostructures or silicon-on-insulator structures (SOI) stand out as excellent material platforms for spin qubits or optical quantum emitters. To achieve the high-performance devices built on these materials, there are two main paths to go for material optimisation. One is using isotopically enriched materials, such as enriched with ^{28}Si, to achieve a nuclear spin depleted environment. Another one is improving the crystal quality of the materials by reducing defects, such as pits on the layers or dislocations at the interfaces. Both paths have been explored within the scope of this work:

- First, an isotope engineered molecular beam epitaxy (MBE) was established with ^{28}Si monocrystal as source material. A hybrid method combining this isotope engineered MBE / chemical vapour deposition (CVD) was applied to grow ^{28}SiGe/^{28}Si(10 nm)/^{28}SiGe heterostructures for electron spin qubits and ^{28}SiGe/Ge(20 nm)/^{28}SiGe heterostructures for hole spin qubits. Here, the thick relaxed SiGe substrates are realised by CVD and the ^{28}SiGe/^{28}Si/^{28}SiGe stacks or the ^{28}SiGe/Ge/^{28}SiGe stacks are grown by the isotope engineered MBE. The CVD growth in this work is undertaken by Dr. Yamamoto in IHP and a research group from Siltronic. A ^{28}Si quantum well layer with ^{29}Si concentration as low as 200 ppm is achieved within a ^{28}SiGe/^{28}Si/^{28}SiGe heterostructure. This ^{28}Si quantum well layer has 1.2 % tensile strain, that is fully strained respective to the relaxed $^{28}Si_{0.7}Ge_{0.3}$ substrate, which was shown in the reciprocal space maps by X-ray diffraction (XRD). In the case of the grown ^{28}SiGe/Ge/^{28}SiGe heterostructure for hole spin qubits, the Ge quantum well layer has 1.3 % compressive strain, that is also fully strained according to the reciprocal space maps.

  The isotope engineered MBE was also applied in the growth of a high-quality ^{28}SOI for optical quantum emitters. A 400 nm ^{28}Si layer was grown on a 70 nm thin SOI

seed. The ^{28}SOI shows low surface roughness of 3.4 Å. There rippels on the surface due to unintentional miscut of the substrate. SIMS reveals ^{29}Si concentration in the ^{28}Si homoepitaxial layer is below 60 ppm.

- Second, the dislocations in the SiGe heterostructures have been investigated regarding the misfit dislocation formation, kinetics, and interactions.

  The critical thickness for the plastic relaxation of the Si quantum well layer embedded in a SiGe/Si/SiGe heterostructure for qubits is studied by plan-view transmission electron microscopy (TEM) and electron channelling contrast imaging (ECCI). Misfit dislocation segments have been observed in the CVD grown SiGe/Si(10 nm)/SiGe heterostructures with both high ($1.4 \times 10^7\,\mathrm{cm}^{-2}$) and low ($3 \times 10^5\,\mathrm{cm}^{-2}$) threading dislocation densities. This misfit dislocations form the glide of pre-existing threading dislocations at the interface of the Si quantum well layer, when the Si quantum well layer thickness beyond a critical value h_c ($h_c = 8.5$ nm in this material system) given by the Matthews-Blakeslee criterion. A Burgers vector analysis was conducted based on the TEM images. The analysis reveals the misfit dislocations are mostly 60° dislocations with Burgers vectors $\frac{a}{2}\langle 1\,0\,1\rangle$ that are split into partials $\frac{a}{6}\langle 1\,1\,2\rangle$ due to the tensile strain field of the Si quantum well layer. By reducing the quantum well thickness from 10 nm to 5 nm below critical thickness, misfit dislocations can be avoided. We discuss the consequences of our findings for the layer stack design of SiGe/Si/SiGe heterostructures for usage in qubits.

  Furthermore, the misfit dislocation propagation kinetics and interactions have been studied by annealing the strained Si or Ge layers grown by MBE and investigating these layers in ECCI. The strained Si layers have been annealed at temperatures from 500 °C to 600 °C in an ultra high vacuum chamber. The strained Ge layers have been annealed temperatures from 300 °C to 400 °C in the same chamber. The misfit dislocations in these annealed layers were imaged by ECCI. The results confirm that the misfit dislocation propagation is a thermally activated process following an Arrhenius-type law for the propagation velocity v: $v = v_0(\sigma)\exp\left(-\frac{E_a(\sigma)}{kT}\right)$. The activation energies $E_a(\sigma)$ is obtained as 0.49 ± 0.01 eV for the tensile strained Si and 0.39 ± 0.10 eV for the compressively strained Ge in this work. These observations imply that it is possible to suppress the misfit dislocation formation kinetically by reducing the temperatures during the SiGe heterostructure epitaxy and post-epitaxy processes in order to develop the low-defect materials for the well-functional SiGe-based spin qubits.

Zusammenfassung

Mit Silizium (Si) und Germanium (Ge) verwandte Materialien wie SiGe-Heterostrukturen oder Silizium-auf-Isolator-Strukturen (SOI) eignen sich hervorragend als Materialplattform für Spin-Qubits oder Quantenemitter. Um die auf diesen Materialien aufgebauten Hochleistungs-Qubits zu erreichen, gibt es zwei Hauptpfade für die Materialoptimierung. Der eine ist die Verwendung von kernspinverarmten Materialien, d. h. von isotopenangereicherten Materialien, z. B. angereichert mit ^{28}Si. Ein weiterer Weg ist die Verbesserung der Kristallqualität der Materialien durch die Verringerung von Defekten, wie Grübchen auf den Schichten oder Versetzungen an den Grenzflächen. Beide Wege wurden im Rahmen dieser Arbeit erforscht:

- Zunächst wurde eine isotopengestützte Molekularstrahlepitaxie (MBE) mit ^{28}Si-Einkristall als Quelle etabliert. Eine Hybridmethode, die diese isotopengestützte MBE mit chemischer Gasphasenabscheidung (CVD) kombiniert, wurde angewandt, um ^{28}SiGe/^{28}Si(10 nm)/^{28}SiGe-Heterostrukturen für Elektronen-Spin-Qubits und ^{28}SiGe/Ge(20 nm)/^{28}SiGe-Heterostrukturen für Löcher-Spin-Qubits zu erzeugen. Hier werden die dicken entspannten SiGe-Substrate durch CVD realisiert und die ^{28}SiGe/^{28}Si/^{28}SiGe-Stapel oder die ^{28}SiGe/Ge/^{28}SiGe-Stapel werden durch isotopengestützte MBE gewachsen. Das CVD-Wachstum in dieser Arbeit wird von Dr. Yamamoto im IHP und einer Forschungsgruppe von Siltronic durchgeführt. In einer ^{28}SiGe/^{28}Si/^{28}SiGe-Heterostruktur wird eine ^{28}Si-Quantentopfschicht mit einer ^{29}Si-Konzentration von nur 200 ppm erreicht. Diese ^{28}Si-Quantentopfschicht weist eine Zugspannung von 1,2 % auf, die im Vergleich zum entspannten $^{28}Si_{0,7}Ge_{0,3}$-Substrat vollständig verformt ist, was in den reziproken Raumkarten durch Röntgenbeugung (XRD) gezeigt wurde. Im Falle der gewachsenen ^{28}SiGe/Ge/^{28}SiGe-Heterostruktur für Loch-Spin-Qubits weist die Ge-Quantentopf-Schicht eine Druckspannung von 1,3 % auf, die laut den reziproken Raumkarten auch voll verformt ist.

Die isotopengestützte MBE wurde auch für das Wachstum eines hochwertigen ^{28}SOI für optische Quantenemitter eingesetzt. Eine 400 nm ^{28}Si-Schicht wurde auf einem 70 nm dünnen SOI-Keim aufgewachsen. Das ^{28}SOI weist eine geringe Oberflächenrauhigkeit von 3,4 Å auf. Auf der Oberfläche befinden sich Welle, die auf einen unbeabsichtigten Fehlschnitt des Substrats zurückzuführen sind. SIMS zeigt, dass die ^{29}Si-Konzentration in der homoepitaktischen ^{28}Si-Schicht unter 60 ppm liegt. Die resultierende Schicht weist eine hohe kristalline Qualität, eine niedrige Defektkonzentration und eine geringe Oberflächenrauhigkeit auf. Dieses ^{28}SOI ist ein vielversprechendes Material für die Integration von optischen Quantenemittern in verlustarmen nanophotonischen Wellenleitern, die frei von Kernspins sind.

- Zweitens wurden die Versetzungen in den SiGe-Heterostrukturen hinsichtlich der Bildung von Fehlpassungsversetzungen, der Kinetik und der Wechselwirkungen untersucht. Wir schlagen einige optimierte Parameter vor, z. B. die Dicke oder die Wachstumstemperaturen, um die Fehlpassungsversetzungsnetzwerke an der Grenzfläche der Si- und Ge-Quantentopfschichten zu minimieren.

  Die kritische Dicke für die plastische Relaxation der Si-Quantentopfschicht, die in einer SiGe/Si/SiGe-Heterostruktur für Qubits eingebettet ist, wurde mit Hilfe der Transmissions-Elektronenmikroskopie (TEM) in Draufsicht und der Elektronenkontrastdarstellung (ECCI) untersucht. Fehlpassungsversetzungssegmente wurden in den CVD-gewachsenen SiGe/Si(10 nm)/SiGe-Heterostrukturen sowohl mit hohen ($1{,}4 \times 10^7\,\mathrm{cm}^{-2}$) als auch mit niedrigen ($3 \times 10^5\,\mathrm{cm}^{-2}$) Durchstoßversetzungsdichten beobachtet. Diese Fehlpassungsversetzungen bilden das Gleiten bereits vorhandener Durchstoßversetzungen an der Grenzfläche der Si-Quantentopfschicht, wenn die Dicke der Si-Quantentopfschicht einen kritischen Wert h_c ($h_c = 8{,}5$ nm in diesem Materialsystem) überschreitet, der durch das Matthews-Blakeslee-Kriterium gegeben ist. Anhand der TEM-Bilder wurde eine Burgers-Vektor-Analyse durchgeführt. Die Analyse zeigt, dass es sich bei den Fehlpassungsversetzungen hauptsächlich um 60°-Versetzungen mit Burgers-Vektoren $\frac{a}{2}\langle 1\,0\,1\rangle$, die aufgrund des Zugspannungsfeldes der Si-Quantentopfschicht in Teilbereiche $\frac{a}{6}\langle 1\,1\,2\rangle$ aufgeteilt sind. Durch Reduzierung der Quantentopfdicke von 10 nm auf 5 nm unterhalb der kritischen Dicke können Fehlpassungsversetzungen vermieden werden. Wir diskutieren die Konsequenzen unserer Erkenntnisse für das Schichtstapeldesign von SiGe/Si/SiGe-Heterostrukturen zur Verwendung in Qubits.

  Darüber hinaus wurden die Kinetik der Versetzungsausbreitung und die Wechselwirkungen untersucht, indem die durch MBE gewachsenen verspannten Si- oder Ge-

Schichten getempert und im ECCI untersucht wurden. Die verspannten Si-Schichten wurden bei Temperaturen von 500 °C bis 600 °C in einer Ultrahochvakuumkammer getempert. Die verspannten Ge-Schichten wurden bei Temperaturen von 300 °C bis 400 °C in der gleichen Kammer geheizt. Die Fehlpassungsversetzungen in diesen geglühten Schichten wurden mit ECCI abgebildet. Die Ergebnisse bestätigen, dass die Ausbreitung von Fehlpassungsversetzungen ein thermisch aktivierter Prozess ist, der einem Gesetz vom Typ Arrhenius für die Ausbreitungsgeschwindigkeit v folgt: $v = v_0(\sigma) \exp\left(-\frac{E_a(\sigma)}{kT}\right)$. Die Aktivierungsenergien $E_a(\sigma)$ werden in dieser Arbeit mit $0{,}49 \pm 0{,}01$ eV für das zugbelastete Si und $0{,}39 \pm 0{,}10$ eV für das druckbelastete Ge ermittelt. Diese Beobachtungen deuten darauf hin, dass es möglich ist, die Bildung von Fehlpassungsversetzungen kinetisch zu unterdrücken, indem die Temperaturen während der SiGe-Heterostruktur-Epitaxie und der Post-Epitaxie-Prozesse reduziert werden, um defektarme Materialien für gut funktionierende SiGe-basierte Spin-Qubits zu entwickeln.

Scientific Visibility

Publications

The following papers originated within the framework of this work:

- Yujia Liu, Stephan Rinner, Thilo Remmele, Owen Ernst, Andreas Reiserer, and Torsten Boeck. ^{28}Silicon-on-insulator for optically interfaced quantum emitters. Journal of Crystal Growth, 2022. [1]

- Yujia Liu, Kevin-Peter Gradwohl, Chen-Hsun Lu, Thilo Remmele, Yuji Yamamoto, Marvin Hartwig Zoellner, Thomas Schroeder, Torsten Boeck, Houari Amari, Carsten Richter, and Martin Albrecht. Role of critical thickness in SiGe/Si/SiGe heterostructure design for qubits. Journal of Applied Physics, 2022. [2]

- Yujia Liu, Kevin-Peter Gradwohl, Chen-Hsun Lu, Yuji Yamamoto, Thilo Remmele, Cedric Corley-Wiciak, Thomas Teubner, Carsten Richter, Martin Albrecht, and Torsten Boeck. Viewing SiGe Heterostructure for Qubits with Dislocation Theory. ECS Transactions, 2022. [3]

- Yujia Liu, Kevin-Peter Gradwohl, Chen-Hsun Lu, Yuji Yamamoto, Thilo Remmele, Cedric Corley-Wiciak, Thomas Teubner, Carsten Richter, Martin Albrecht, and Torsten Boeck. Growth of ^{28}Si Quantum Well Layers for Qubits by a Hybrid MBE/CVD Technique. Submitted, 2022. [4]

- Yujia Liu, Kevin-Peter Gradwohl, Chen-Hsun Lu, Kaspars Dadzis, Yuji Yamamoto, Lucas Becker, Peter Storck, Thilo Remmele, Torsten Boeck, Carsten Richter, and Martin Albrecht. Strain relaxation from annealing of SiGe heterostructures for qubits. Submitted, 2022. [5]

- Owen C. Ernst, Yujia Liu, and Torsten Boeck. Leveraging dewetting models rather than nucleation models: Current crystallographic challenges in interfacial and nanomaterials research Contemporary and prospective opportunities to exploit dewetting theory for energy conversion devices and quantum computing. Zeitschrift fur Kristallographie - Crystalline Material, 2022. [6]

- Kevin-Peter Gradwohl, Chen-Hsun Lu, Yujia Liu, Carsten Richter, Torsten Boeck, Jens Martin, and Martin Albrecht. Strain relaxation in SiGe heterostructures for quantum technologies by a geometric Monte Carlo approach. Physica Status Solidi Rapid Research Letters, 2022. [7]

Conference Contributions

The following conference contributions originated from this work and were presented by the author:

- Yujia Liu. Strained ^{28}Si for quantum circuits by MBE-CVD combined growth. Oral talk, European material research society, September 2021, Online event.

- Yujia Liu, Thilo Remmele, Thomas Teubner, Nikolay V. Abrosimov, Martin Albrecht, Torsten Boeck. Isotopicallly Engineered MBE Growth of Strained ^{28}Si for Quantum Circuits. Poster, International Conference for Molecular Beam Epitaxy, September 2021, Online event.

- Yujia Liu, Thilo Remmele, Carsten Richter, Thomas Teubner, Nikolay V. Abrosimov, Martin Albrecht, Wolfgang M. Klesse, Torsten Boeck. Strained ^{28}Si for Quantum Circuits by MBE-CVD Combined Growth. Oral talk and poster, Jung Deutsche Gesellschaft für Kristallzüchtung und Kristallwachstum, October 2021

- Yujia Liu, Kevin-Peter Gradwohl, Carsten Richter, Thilo Remmele, Martin Albrecht, Torsten Boeck. ^{28}Si trifft auf Quantentechnologie - Rechner der naechsten Generation. Oral talk, Vertrauenswuerdige Elektronik, March 2022, BMBF online event.

- Yujia Liu, Kevin-Peter Gradwohl, Torsten Boeck, Chenhsun Lu, Thilo Remmele, Carsten Richter, Martin Albrecht. From isotopic purity to lattice perfection: Growth

of SiGe heterostructures for quantum technologies. Oral talk, IKZ workshop SiGe based materials for quantum technology, May 2022, Berlin, Germany.

- Yujia Liu, Kevin Peter Gradwohl, Thilo Remmele, Martin Albrecht, Carsten Richter, Torsten Boeck. Isotope engineered Group IV Epitaxy for Qubits. Poster, Quantum computation hardware and software summer school, June 2022, Laussane, Switzerland.

- Yujia Liu, Kevin-Peter Gradwohl, Chen-Hsun Lu, Thilo Remmele, Yuji Yamamoto, Marvin Hartwig Zoellner, Thomas Schroeder, Torsten Boeck, Houari Amari, Carsten Richter, and Martin Albrecht. Viewing SiGe Heterostructure for Qubits with Dislocation Theory. Oral talk, ECS meeting , October 2022, Atlanta, United States.

Contents

I think there is a world market for
maybe five computers.

Thomas Watson,
chairman of IBM, 1943

1 Introduction

Respective to the Stone Age, the Bronze Age and the Iron Age, the time we are living in now could be commonly referred as the Silicon Age. The two powerful legs to stand in the Silicon Age are software and hardware of modern computers. The software is developed based on established computational logic equivalent to the abstract model of a Turing machine. The hardware on the other hand, is made of silicon (Si) monocrystal, or more widely speaking, semiconductors. This makes it possible that modern computers can execute an enormous amount of mathematical calculations, which surpass the abilities of the human brain in terms of capacity and speed.

Nowadays, physicists, mathematicians and computer scientists strenuously pursue computation models beyond Turing machines, one of that is quantum computing. There is again a huge chance to extend the role of Si, together with its sister in the periodic table, germanium (Ge), as the basic materials for quantum computers. There are several material platforms based on Si, Ge to realise physical quantum computers, such as SiGe/Si/SiGe heterostructures for electron spin qubits, SiGe/Ge/SiGe heterostructures for hole spin qubits, and Si-on-insulator (SOI) for optical quantum emitters. Among these material platforms, isotope enriched materials play an important role. In this work, we apply enriched ^{28}Si to grow the materials mentioned above. This not only provides a nuclear spin depleted environment for the electron spin qubits but also potentially leads to a narrow emission in the optical quantum emitters. Besides, we will also exam carefully the SiGe heterostructures for qubits with the perspective from material science.

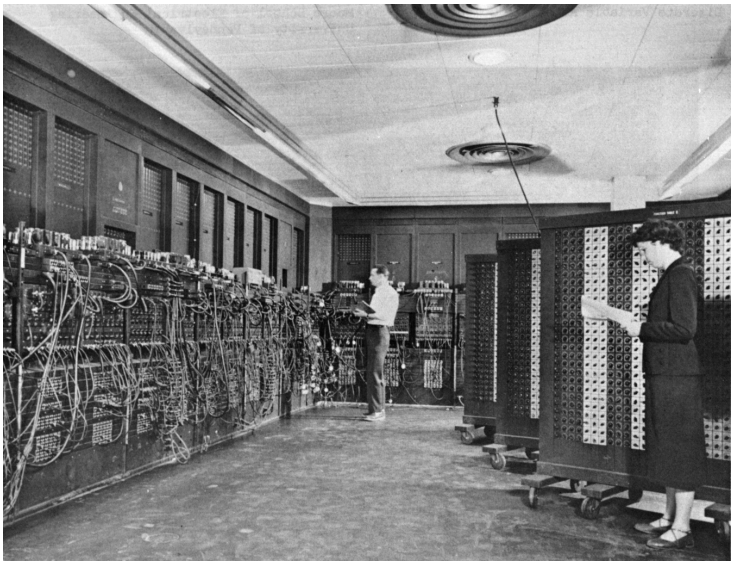
1.1 Group IV Semiconductors: From Classical Computers to Quantum Computers

The first electronic programmable computer, the Electronic Numerical Integrator and Computer (ENIAC) in Figure 1.1 (a), was built during World War II [8]. The ENIAC contains around 18,000 vacuum tubes as its building blocks. The replacement of bulky vacuum tubes with compact semiconductor transistors changed the game of computer hardware. This made the computer portable and more performant by increasing computational power and decreasing the size. Group IV semiconductors have been the leading actors during the development of transistors. The first transistor (Figure 1.1 (b)) was invented based on Ge in 1947 by Bell Laboratories [9, 10] and the first integrated circuits (Figure 1.1 (c)) were also built based on Ge in 1958 by Texas Instruments [11, 12]. The scientists, who have invented these two technologies, have won the Nobel Prizes in physics in 1956 (Shockley, Bardeen and Brattain) and 2000 (Kilby). Later on, Si transistors took over the baton [13] and have become the mainstream till now because of their great properties. Si has a higher bandgap than Ge resulting in higher operating temperatures and fewer leakage currents of transistors. Besides, Si is the second-most abundant element across the earth. Because of this, the production of Si transistors is quite economic. Furthermore, SiO_2 is a good option for a stable dielectric layer in transistors, in contrast to Ge oxides. All of these lead to the marvellous performance of Si transistors. Since 1970s, the commercial integrated circuits follow well with the Moore's law: the number of transistors in a dense integrated circuits doubles about every two years [14]. So far, the semiconductor industry has managed to build billions of transistors on a single chip and shrink the single transistor size down to several nanometers [15].

The classical model of computation is based on the Turing machine invented in 1936 by Alan Turing. During the rapid-paced development of physical computers, the exploration of computation models didn't pause. Quantum computing was proposed in the 1980s as information processing based on quantum mechanics [16]. The smallest building block in a quantum computer is called quantum bit, or qubit for short. As it is illustrated in Figure 1.2, a bit for a classical computer has a state of either 0 or 1. A qubit has also computational basis states $|0\rangle$ and $|1\rangle$, but can additionally be in a linear combinations of $|0\rangle$ and $|1\rangle$, called superposition state:

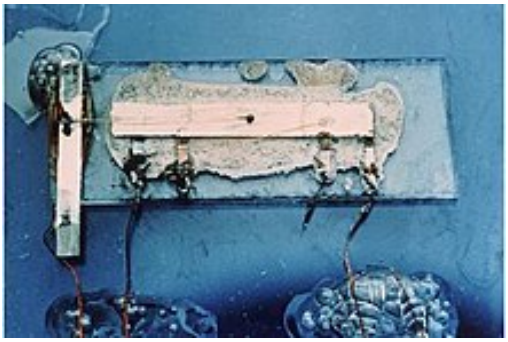
$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle\,. \tag{1.1}$$

Here, α and β are complex numbers called the amplitudes of $|0\rangle$ and $|1\rangle$ which satisfy $|\alpha|^2 + |\beta|^2 = 1$ so that each qubit state is normalised. The state of a qubit can be



(a)

(b)



(c)

Figure 1.1: (a) Two programmers are operating the first electronic programmable computer ENIAC [8]. (b) The first transistor made of Ge working as a point contact transistor [10]. (c) The first integrated circuit made of Ge [12].

represented as a normalised vector in a two dimensional complex vector space, which can be visualised as a sphere (so called Bloch sphere). Within a quantum system containing n qubits, the basis states are of the form $|x_1x_2...x_n\rangle$, where $x_1, x_2, ..., x_n$ can be either 0 or 1. The state of this quantum system $|\psi\rangle$ has 2^n complex coefficients,

$$|\psi\rangle = \sum \alpha_i \, |x_1x_2...x_n\rangle \,, \tag{1.2}$$

which means it can be in a superposition of 2^n basis states. Compared to a classical computer with n bits, it can be only in one of 2^n states. This brings the evolutionary computational power with quantum computer.

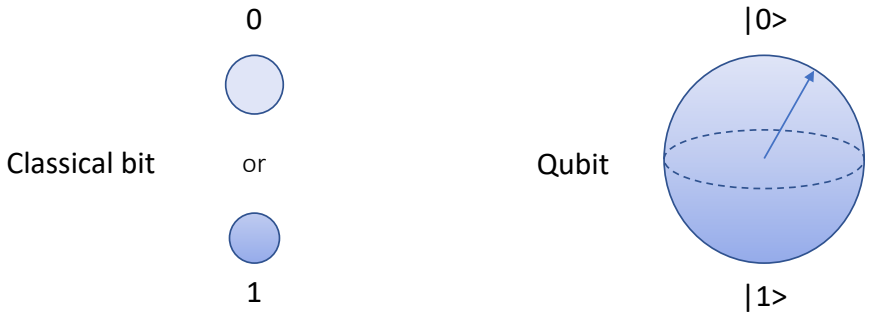


Figure 1.2: Compared to a bit in classical computers that can be either in a state of 0 or 1, a qubit has computational basis states $|0\rangle$ and $|1\rangle$ but can also be in a superposition of $|0\rangle$ and $|1\rangle$.

Later on people have demonstrated that some problems can be theoretically solved more efficiently by a quantum computer, such as the integer prime factorization problem [17] and unstructured database search [18]. Scientists have proposed and attempted various physical realisations to bring quantum computers from a theoretical concept to reality. In 2000, DiVincenzo proposed five criteria for achieving quantum computing physically [19]: scalable, initialisable, having long coherence time, having a "universal" set of quantum gates, and measurable. So far, most breakthroughs in quantum computer realisations were carried out with superconducting qubits. IBM launched a 433-qubit quantum processer Osprey in 2022 [20]. Trapped-ion quantum computer is chasing with a recently announced 20-qubit system built by Quantinuum [21]. However, there are some natural difficulties of these systems towards real-world applications of quantum computers, for example, extending the coherence time in superconducting quantum computers and

speeding up the gates in trapped-ion quantum computers [22]. The competition and exploration of physical solutions as well as efficient algorithms for quantum computers are still ongoing.

During the exploration of quantum computer realisation, group IV semiconductors stand out again as excellent candidates [23, 24]. These material platforms are convincing because they are compatible with the massive established Si semiconductor transistor industries and the qubits built on these material platforms own quite small sizes resulting in a high potential for scalability [25]. A further advantage of group IV semiconductors in quantum computers is that their major isotopes are nuclear spin free, which already gives a relatively low-noise environment compared to the III-V semiconductors. The stable isotopes with nuclear spins, such as ^{29}Si and ^{73}Ge can be further reduced by isotopic purification [26, 27]. According both theoretical calculation [28, 29] and experimental results [30], the coherence time of electron spins can be extended exponentially by introducing the isotope enriched materials with depleted nuclear spins[1].

We will discuss two systems based on Group IV semiconductors for the physical realisation of quantum computers. The following provides a brief overview of each one.

1) Spin qubits: single electrons or holes can be confined by combining quantum well and top gates to form quantum dots. Then, their spins can be used as qubits. Such charges can be confined at either the interface between the group IV semiconductors and their oxides [31] or the interface between the group IV semiconductors and the group IV alloys, for example, Si/SiGe [32] or Ge/SiGe [33]. Noticeably, some remaining challenges are waiting to be solved in these systems, such as minimising the defects in the material systems to improve the qubit behaviours.

2) Photonic qubits: though group IV semiconductors are indirect semiconductors, there are still some promising ways of building single photon emitters based on the emission from the defects in Si [34]. These defects can be structural defects and introduced dopants. The emission light peak width in Si is remarkably shaper by utilising isotopically enriched ^{28}Si to reduce the phonon dispersion broadening [35]. One of the key aspects for better scalability of these systems is to control these defects locally and quantitatively [36].

Time will tell if the group IV semiconductors continue their legendary story from classic computers to quantum computers. Nevertheless, we will demonstrate some group IV

[1] Both theoretical calculation and experimental results in the citations are based on the electron spin bound to donors.

semiconductor material systems for quantum hardware, the growth processes, and the characterisation results. Besides, we will also inspect scientific and technological challenges from a material science perspective on these systems.

1.2 Electron Spin Qubits in Tensile Si

Before DiVincenzo proposed the famous criteria for quantum computer hardware, he also had one great idea together with Loss [37], that qubits can be physically realised with the spins of electrons in quantum dots. Following, Friesen et al. presented that SiGe heterostructures can be the material systems to host the electron spin qubits [38]. The proposed system is quite close to the common layer stacks applied by the scientific communities nowadays [32, 39] as well as in section 4.1.

Principle

The applied layer stack of SiGe heterostructures for qubits in this work is shown in Figure 1.3 where a thin undoped Si layer is epitaxially grown between two relaxed SiGe layers. The thin Si layer should be fully strained when its thickness is low and the bottom strain-relaxed SiGe substrate is way thicker than the Si layer. In this case, the thin Si layer between $Si_{0.7}Ge_{0.3}$ layers is 1.3 % tensile strained. The quantum well in the conduction band forms in the strained Si layer. The electrons are confined two-dimensionally at the upper interface of the Si quantum well layer via an applied bias voltage. When the local electrostatic field is applied through the post-epitaxy fabricated top gates, the electrons are further confined in the lateral dimension as quantum dots. In this case, we can use the spin states of the confined electrons, up $|\uparrow\rangle$ and down $|\downarrow\rangle$, as the quantum states $|0\rangle$ and $|1\rangle$ for qubits. The universal gate operation on these kinds of qubits can be performed by spin resonance in magnetic field.

Regarding to the read-out of the spin states of the electrons, it is quite challenging to read out the spin states directly because the magnetic dipole of electrons is too small. Fortunately, there are other possibilities to access the spin states of the electrons when we look at the Si conduction band in the energy diagram in detail (Figure 1.4). Upon the biaxial tensile strain, the six-fold conduction band valley degeneracy in bulk Si is reduced to a four-fold valley ($\pm x$ and $\pm y$) and two-fold valley ($\pm z$). Quantum confinement further

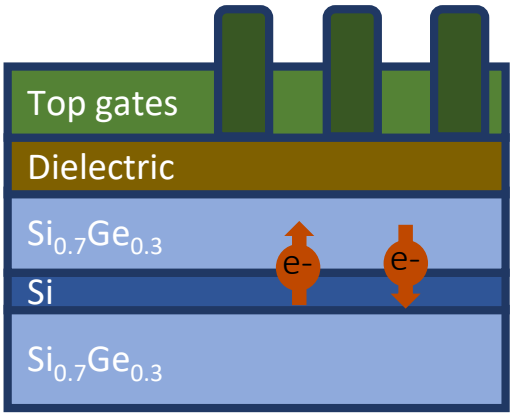


Figure 1.3: The quantum-dot architecture of the SiGe/Si/SiGe heterostructure for electron spin qubits.

reduces this degeneracy to a non degenerate valley. The energy difference between the two lower valleys are called valley splitting. The valley splitting can be enhanced via a magnetic field applied [40]. In the non-degenerate valley, the electron spin levels of $|\uparrow\rangle$ and $|\downarrow\rangle$ are further split with each other [41]. The correlation of the electron spin state with its energy state makes it possible that the spin states of electrons can be read out by measuring the energy states of the electrons. That significantly eases the initialisation and measurements of the qubits.

^{28}Si

Apart from the already mentioned advantages of the compatibility to Si transistor industry and the small footprint in section 1.1, the electron spin qubits built on SiGe heterostructures benefit from that the isotope majority of Si, ^{28}Si, is nuclear spin free. Therefore, the hyperfine decoherence from nuclear spins on electron spins in this system is significantly reduced, when compared with the similar quantum-dot electron spin qubits based on III-V semiconductors. If the depletion of the stable isotope with nuclear spin, ^{29}Si, is introduced in this system with already developed isotope engineering [26], the coherence time of the electron spin can be further prolonged in order of magnitude [28].

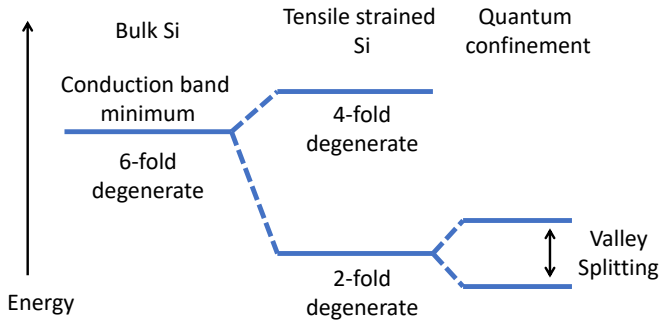


Figure 1.4: Valley splitting in a Si quantum well layer.

Material Requirements

In order to provide proper material systems for electron spin qubits, several crucial requirements need to be achieved in the SiGe heterostructures. Firstly, the Si quantum well layer should have not only isotopic but also chemical high purity. The unintentional dopants in the Si quantum well can increase unwanted magnetic noises [28] and charge noises [39]. Next, the structural defects in the SiGe heterostructures need also to be minimised in order to achieve large-scale homogeneity within the Si quantum well layer (discussed in chapter 5).

Epitaxy

So far, several research groups have successfully built electron spin qubits based on the SiGe heterostructures [32, 42, 43, 44]. During their SiGe heterostructures fabrications, commonly, thick relaxed SiGe substrates are grown on Si (0 0 1) substrate as virtual substrates and then SiGe/Si/SiGe heterostructures are grown upon the relaxed SiGe substrates. The heterostructures in these works were either grown by chemical vapour deposition (CVD) [32, 42] or molecular beam epitaxy (MBE) [43, 44]. Comparing the two methods, MBE can be carried out at a relatively low temperature, which can slow down some defects formation kinetically (discussed later in subsection 5.2.2). Respectively, the CVD growth has usually higher growth rates and is more economic for the thick SiGe buffer layer. Apart from that, CVD is the more popular technique applied in the

industry because the wafer scale in Si, Ge related CVD is up to 12 inch and the MBE is a rather academic method with a limited wafer size up to 8 inch. In the past, transistors based on SiGe heterostructures were successfully manufactured by the hybrid growth of MBE and CVD combining their advantages [45, 46].

In this work, the SiGe heterostructures grown by an MBE/CVD hybrid technique for electron spin qubits are presented. Here, a thick relaxed SiGe substrate is grown by CVD. An isotope engineered MBE is applied to grow ^{28}SiGe/^{28}Si/^{28}SiGe heterostructures on the relaxed SiGe substrate. Besides, the effects of some essential growth parameters on the material quality, such as growth temperatures and layer thicknesses, are also discussed.

1.3 Hole Spin Qubits in Compressive Ge

As discussed above about the advantages of Si over Ge when used as transistor material. However, the competition of the materials for qubits is complex. Strained Ge in SiGe heterostructure opens the possibility to host hole spin qubits in an undoped environment.

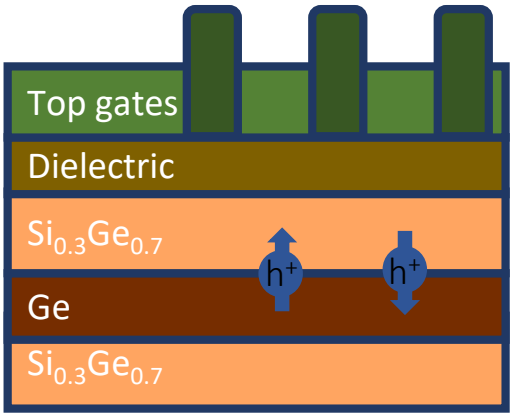


Figure 1.5: The quantum-dot architecture of the SiGe/Ge/SiGe heterostructure for hole spin qubits.

The SiGe heterostructures for hole spin qubits studied in this work (Figure 1.5) are quite similar to the heterostructures for electron spin qubits but the contents of Si and Ge are reversed. Holes can be confined in the Ge layer through the quantum well in the valence band two dimensionally by a top gate and further confined into quantum dots with barrier gates. Under compressive strain, the Ge valence band of the heavy hole and light hole split from each other. Therefore, the holes will stay further in the heavy hole valence band in this structure. The spin states up $|\uparrow\rangle$ and down $|\downarrow\rangle$ of the holes can be utilised as qubits.

The hole spin qubits hosted in compressively strained Ge layers have several additional advantages as electron spin qubits built in tensile Si layers. Firstly, the holes in Ge has much lower effective mass and do not have low energy valley states, this eases the device fabrication [47]. Low charge noise and low disorder of holes in Germanium provides a quite environment and enables reproducibility [48]. Also, the hole spin qubits in Ge provides the possibility for hybrid superconductor-semiconductor quantum system since the ohmic contacts for holes in Ge can be made of aluminium (Al) [33]. Besides, the spin-orbit coupling in the heavy hole valence band is strong. This results that the coherence time of the hole spin can be longer than the electron spin [49]. The strong spin-orbit coupling as well leads that the spin manipulation and read-out can be performed by introducing a radio frequency electric field [50]. Because of this, the micro magnetic field is not necessary for this system. The same as Si, Ge offers the possibility of nuclear spin free environment by depleting the minor isotope ^{73}Ge via an isotope enrichment technique, which can reduce the hyperfine interactions between the hole and nuclear spins [51]. Though, to which degree the nuclear spin free Ge can increase the coherence time of the hole spin qubit is still a remaining question [52].

The SiGe heterostructures for hole spin qubits hosted in a Ge quantum well are mostly fabricated by CVD [53, 54, 55, 56, 57]. The low-temperature hole mobility in the two dimensional hole gas (2DHG) is up to millions of $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [56].

In this work, the SiGe heterostructures illustrated in Figure 1.5 were realised by a MBE/CVD hybrid technique.

Table 1.1: Some examples of the emitters in Si. ZPL here presents zero phonon line transition wavelength.

	Emitters	ZPL	Crystalline structures	Reference
Color centers	C center	789 meV (1571 nm)	One interstitial carbon and one interstitial oxygen	[35]
	G center	969 meV (1280 nm)	One substitutional carbon, one interstitial carbon and one interstitial Si	[35, 36, 67]
	W center	1018 meV (1218 nm)	Three interstitial Si	[68]
	T center	935 meV (1326 nm)	Two substitutional carbon, one interstitial hydrogen	[65]
Donors	$^{77}Se^{+}$	427 meV (2904 nm)	Ionized dopant	[69]
	Er^{3+}	810 meV (1530 nm)	Rare earth dopant	[70, 71, 72, 73]

1.4 Silicon Quantum Emitters

Photonic qubits are one of the early ideas for the physical realisation of quantum computers [58]. The material pioneers for photonic qubits are III-V semiconductors [59, 60, 61]. Using Si for the photonic qubits doesn't seem intuitive because Si is an indirect semiconductor. In the last decade, some optically active emitters and single emissive dopants were explored in crystalline Si. Some examples of the emitters and optical active dopants are listed in Table 1.1. The emission wavelength of these emitters is mostly within the optical communication bands[2]. These scientific results are convincing that Si has the possibility to be used as material platforms to serve quantum computers and quantum networks. These emitters in Si can be both applied in single photon sources [36] and also directly as spin centres [63, 64, 65]. ^{28}Si play an essential role in these applications. Firstly, the emission linewidth is narrowed significantly in the emitter hosted in isotopically enriched ^{28}Si by eliminate the inhomogeneous isotope broadening [35]. Next, the spin centres in the nuclear spin depleted environment of ^{28}Si enriched materials have relatively long coherence time when compared to natural Si [66].

[2]The optical communication bands ranges from 1260 nm to 1625 nm due to the low loss and low dispersion in the common applied optical fibres [62].

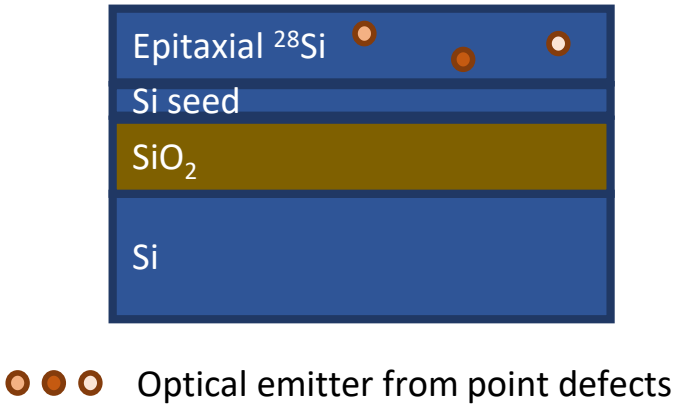


Figure 1.6: Th ^{28}SOI for optical quantum emitters.

Both single photon sources and also spin centre emitters are commonly built on the Si-on-insulator (SOI) waveguides, where the light can be confined and transmitted within the top Si layer with low optical loss and the device fabrication is uncomplicated [74, 75]. To integrate a high quality ^{28}Si layer for optical quantum emitters into SOI wafers, an economical way to go is to grow a homoepitaxial ^{28}Si layer on a commercial thin SOI substrate, as it is shown in Figure 1.6 [36]. ^{28}Si epitaxial layers on SOI wafers (^{28}SOI) have been grown with CVD by Laboratoire Charles Coulomb with isotopic purity $>$ 99.99 % [68], as well as commercially by Lawrence Semiconductors with isotopic purity $>$ 99.9 % [76]. MBE is an alternative method to achieve high-crystal-quality and high-isotope-purity ^{28}SOI wafers due to its clean growth environment in ultra high vacuum (UHV). The MBE grown ^{28}SOI is discussed in this work (see in section 4.3).

1.5 Isotope Enrichment and Processing for Group IV Semiconductors

As mentioned above, the isotope enriched group IV semiconductors are the key materials for their applications in quantum technologies.

Natural Si is composed of three stable isotopes 92.23 % ^{28}Si, 4.67 % ^{29}Si, and 3.10 % ^{30}Si

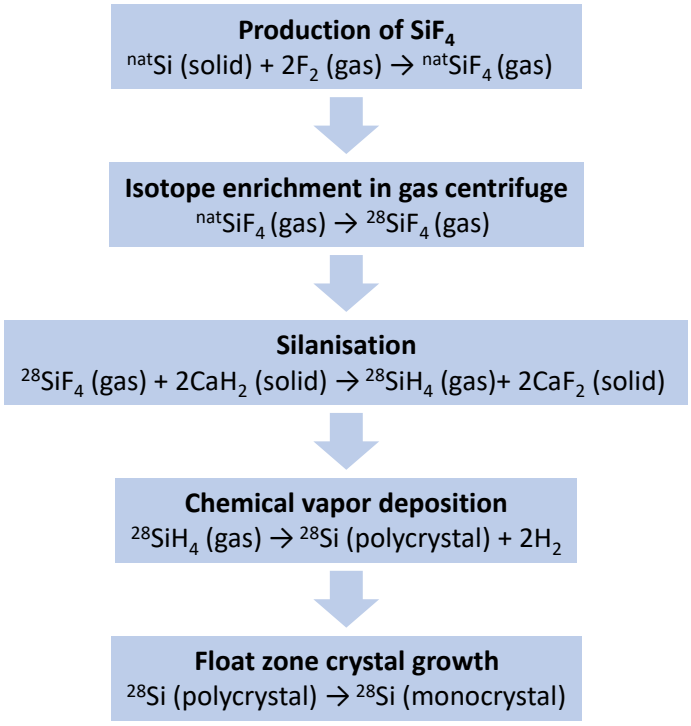


Figure 1.7: Main technological steps of the ^{28}Si crystal production (^{nat}Si: Si of natural isotopic composition).

[78]. Both ^{28}Si and ^{30}Si are free of nuclear spin, while ^{29}Si has nuclear spin $\frac{1}{2}$. In the researches of isotope enriched Si for qubits, mostly ^{28}Si is applied because of its natural abundance. Till now, the isotope enrichment and processing of ^{28}Si have been successfully developed at Institute of Chemistry of High-Purity Substances of the Russian Academy of Sciences and Leibniz-Institut für Kristallzüchtung for various projects, such as the production of the ^{28}Si spheres to define the Avogadro constant [79, 77, 80, 26].

The production of the high purity ^{28}Si single crystal from Si of natural isotopic composition (^{nat}Si) is illustrated in Figure 1.7, where the essential step is separating $^{28}SiF_4$ from $^{nat}SiF_4$ by using gas centrifuges. SiF_4 is applied here because fluorine (F) has only one isotope ^{19}F. During the production, $^{nat}SiF_4$ gas is firstly obtained from the fluorination of ^{nat}Si. Three cycles of the gas centrifuge are applied to reach high isotope purity as well as chemical purity of $^{28}SiF_4$. Afterwards, $^{28}SiF_4$ is converted to $^{28}SiH_4$ by passing through a layer of mechanically dispersed CaH_2 in a hydrogen environment, that is the silanisation process. The $^{28}SiH_4$ is further purified by cryofiltration and periodic low-temperature

(a) (b)

Figure 1.8: (a) Polycrystalline ^{28}Si rod of in the deposition apparatus; (b) Float-zone grown monocrystalline ^{28}Si with [0 0 1] as growth direction [77, 26].

rectification. The ^{28}Si polycrystal is deposited from high-purity $^{28}SiH_4$ by CVD on an isotope enriched ^{28}Si rod as seed, so that the diameter of the rod increases 10 times from the growth and the final ^{28}Si polycrystal product is shown in Figure 1.8 (a). Finally, a floating zone technique is applied for the growth of a dislocation-free ^{28}Si single crystal to keep the isotopic enrichment as well as to achieve higher chemical purity (Figure 1.8 (b)). The isotopic compositions of the $^{28}SiF_4$ gas and the ^{28}Si monocrystal are monitored by an advanced laser mass spectrometry technique [81, 82].

This kind of ^{28}Si float-zone single crystal is proved to have high isotopic, high chemical purity, and high crystalline perfection [26]. It is well suited as source materials for the MBE growth of ^{28}Si related layers for qubits.

An experiment is a question which science poses to nature and a measurement is the recording of nature's answer.

Max Planck

2 Experimental Methods

2.1 Epitaxy

Epitaxy is a crystal growth technique, that new crystal layers or nanostructures are grown on the existed crystal substrates. The new crystals have defined orientation as the substrates. Epitaxy is commonly applied in the semiconductor academy and industry to realise the semiconductor alloys or the semiconductor low dimensional structures.

Two epitaxy techniques for the Si, Ge growth are applied in this work: MBE and CVD. Following, some overviews of these two techniques are outlined and also the experimental details of the growth are described.

2.1.1 Isotope Engineered Molecular Beam Epitaxy

We have discussed above the advantages of isotopically enriched group IV semiconductors on the SiGe heterostructure for qubits as well as Si quantum photonics. An isotopically engineered MBE is applied on the growth of the structures mentioned above for quantum technologies.

MBE Overview

MBE is a widely applied deposition technique in ultra high vacuum (UHV) for epitaxial film growth [83, 84, 85]. During MBE, vapourised materials are transported as molecular beams (in the case of Si, Ge, atom beams are more accurate instead of molecular beams)

in a UHV environment down to 1×10^{-10} mbar on a heated wafer, where the epitaxial film growth happens.

Due to the extremely low chamber pressure, the growth rate can be as low as sub-nanometer per second scale. This results in controllable growth and consequently eases the growth of nanostructures and multilayers. The MBE growth of high-purity layers takes also advantage of the absence of the carrier gas. Furthermore, the UHV environment makes many in-situ measurements possible, such as reflection high-energy electron diffraction and Auger electron spectroscopy. On the other hand, MBE is not a common technique for large scale industry yet because of its low throughput, high expense from high system requirements, and high maintenance demands.

Talking particularly for Si, Ge MBE, there are several choices of sources to deliver clean vapours. In the case of Si, electron beam evaporators and sublimation sources with resistive heating are often applied. The growth rate offered by the electron beam evaporator is higher, especially when a large quantity of source materials are applied. Ge has a lower melting point than Si, which makes the effusion cell for Ge evaporation possible. However, the crucible selection should be careful to avoid contamination. Nevertheless, electron beam evaporators are also suitable for Ge evaporation.

^{28}Si Source Materials and Set-up

An isotope engineered MBE (Figure 2.1) was established with ^{28}Si source material. The ^{28}Si source was produced by recycling the remaining material from the production of the ^{28}Si spheres for Avogadro constant definition (section 1.5). A photo of the original ^{28}Si crystal for the spheres is presented in Figure 2.2 (a). After the cutting of the two ^{28}Si spheres, large amount of precious high-purity ^{28}Si is left. The remaining ^{28}Si is then cut into pieces, regrown to a monocrystal by a Czochralski method, and then put through twice float zone refining to reach higher chemical purity. The final ^{28}Si monocrystal for MBE source is grown as a cylinder shape.

In MBE, both ^{28}Si and Ge sources here were provided by electron beam evaporators from Dr. Eberl MBE-Komponenten GmbH. The existed cylinder-shape ^{28}Si float-zone crystal is smaller than the crucible of the commercial electron beam evaporator. To apply the ^{28}Si float-zone crystal as the source material into the electron beam evaporator, it is integrated into a natural Si crucible shown in Figure 2.2 (b). The electron beam

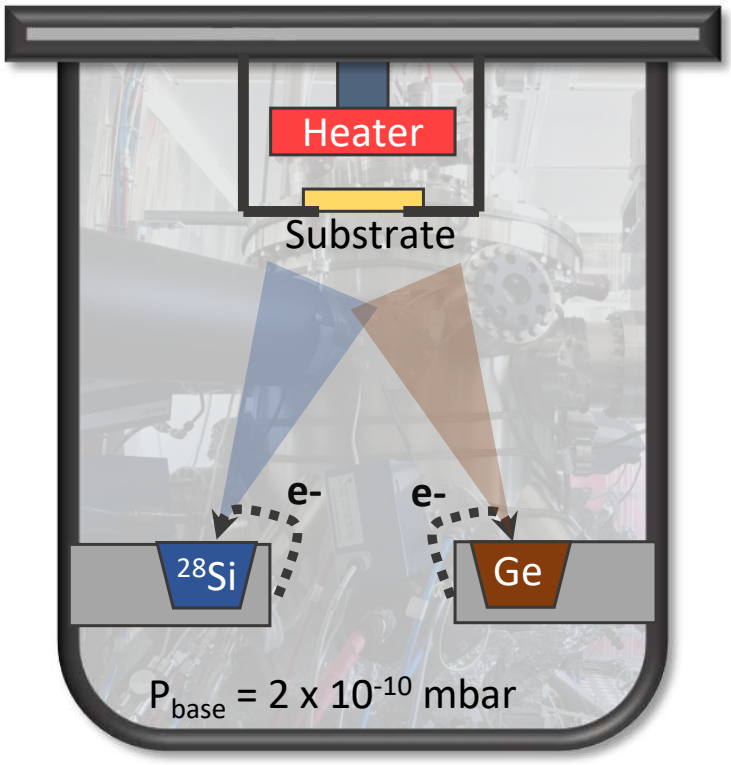
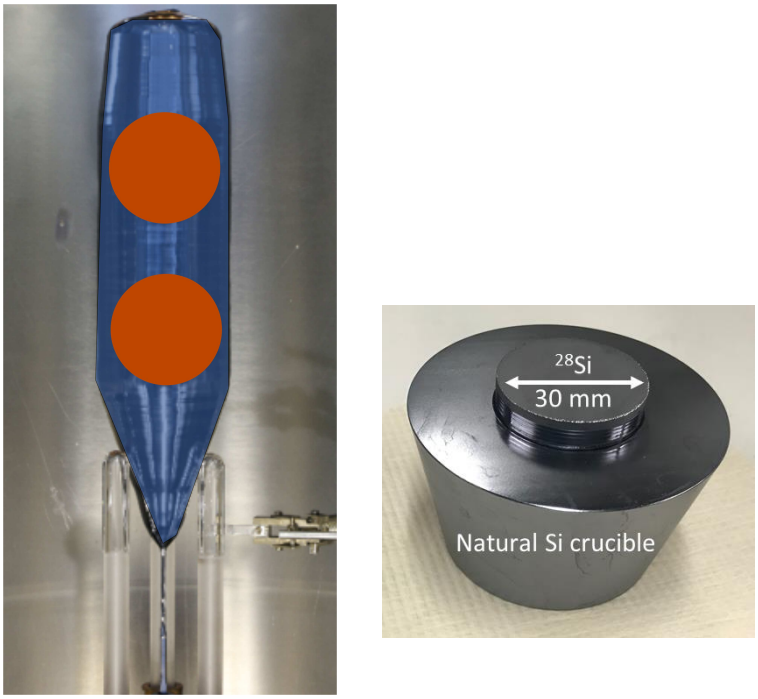


Figure 2.1: Schematic of a MBE with a photo of the MBE applied in the background.

is focused on the middle of the ^{28}Si crystal. The growth rates of both ^{28}Si and Ge sources are calibrated with an oscillating quartz crystal and additionally by an ex-situ X-ray reflectivity thickness measurements of amorphous ^{28}Si layers on Ge substrates or amorphous Ge layers on Si substrates deposited at room temperature. The calibration process is reported carefully by Lange [86].

Besides the ^{28}Si source material newly integrated into MBE, the details of each components in this MBE chamber are well described in the dissertations from Schmidtbauer and Lange [87, 86]. Briefly summarising, the MBE growth was performed in a UHV chamber with a base pressure of 2×10^{-10} mbar. The pressure is maintained by a turbomolecular pump and a cryopump. During the growth, the pressure increases to around several 10^{-9} mbar due to the substrate heating and the source evaporation. The sample needs to pass a load lock chamber (1×10^{-6} mbar), a preparation chamber (1×10^{-8} mbar), and



(a) (b)

Figure 2.2: (a) The float-zone ^{28}Si single crystal for both defining Avogadro constant, marked with two orange circles, and source materials of MBE growth, marked in blue. (b) The ^{28}Si source on the natural Si crucible.

a transfer chamber (1×10^{-9} mbar) to reach the MBE chamber. The residual gases can be in-situ monitored by two mass spectrometers (Microvision 2 from MKS). The sample can be heated by a pyrolytic graphite heater.

Apart from the previous dissertations from our group, a hydrogen atom beam source [88] is applied for in-situ surface preparation. The atomic hydrogen is produced when the hydrogen gas goes through a tube heated with a filament up to 1500 °C. The hydrogen gas is obtained from a water cracker PROTON® ON SITE Hydrogen G200. After the water cracking reaction into H_2 and O_2 gases, the O_2 and H_2O in the flow is filtered so that the purity of H_2 is as high as 99.9995 %.

Substrates

Three types of substrates were applied in the MBE growth: relaxed $Si_{0.7}Ge_{0.3}$ substrates, relaxed $Si_{0.3}Ge_{0.7}$ substrates and thin SOI substrates. They all have the surface orientation as (0 0 1) without intentional offcut.

The relaxed $Si_{0.7}Ge_{0.3}$ substrates and the relaxed $Si_{0.3}Ge_{0.7}$ substrates are cut into $25 \times 25\,mm^2$ from CVD grown 200 mm wafers and 300 mm wafers. The growth processes for these relaxed SiGe substrates are described in detail in section 2.1.2.

The commercial SOI substrate is fabricated with Smartcut technique. The template Si layer and the buried oxide layer have thicknesses of 70 nm and 2 µm respectively.

Surface Preparation

In this work, a reliable surface preparation combining ex-situ wet chemical cleaning and in-situ atomic hydrogen irradiation is developed for both SOI and relaxed $Si_{0.7}Ge_{0.3}$ substrates. The importance and the development of the surface preparation are presented section 3.1. Here, the developed preparation process is described.

In the wet chemical part, a standard surface preparation involving sulfuric acid / hydrogen peroxide mixture [89, 90] is applied. The substrates are first cleaned in acetone for one minute with ultrasonic to remove greasy contaminations. The contaminated acetone often leaves residuals on the substrates if without any treatment. To avoid this, the substrates are cleaned afterwards immediately in isopropanol for one more minute with ultrasonic. After these two step organic solution cleaning, the substrates are rinsing with deionised water. Then, the substrates are put into the freshly mixed solution of H_2SO_4:H_2O_2(31 %) with a 4 : 1 ratio for 10 min. This step is meant to remove the organic contamination on the substrates by oxidising the contamination. A thin SiO_x layer will also form on the Si substrate surface during this oxidation process. Afterwards, the substrates are rinsed in the deionised water for 1 min. At the end of the wet chemical cleaning process, the substrates are put into 0.5 % HF solution for 1 min to remove the oxides on the substrate surface. To reduce the experimental risk from the HF solution, the solution is diluted with running deionised water for around 2 min. The substrates are hydrophobic after the wet chemical cleaning, which indicates the hydrogen terminated surfaces. The cleaned substrates are inserted into the load lock of the UHV system without blow dry.

The air exposure of the substrate is limited to less than 1 min. The deionised water applied here has resistivity more than $15 \times 10^6\,\Omega\,\mathrm{cm}$, indicating ultra high purity. The chemicals acetone, H_2SO_4, H_2O_2(31 %) and HF(40 %) have purity grades of very large scale integration (VLSI) quality Selectipur®. The isopropanol has a higher purity grade of super large scale integration (SLSI) quality Selectipur®. They are all from BASF.

After wet chemical cleaning, an in-situ surface preparation is performed on the substrates in the MBE chamber in order to achieve epitaxy ready substrates, including thermal annealing and atomic hydrogen irradiation. The substrates are heated up to 700 °C. Following, the atomic hydrogen irradiation of the substrate surface is performed for 5 min. The atomic hydrogen source was described in the set-up part above. During the irradiation, the pressure in the chamber increases from around 10^{-9} mbar to 3×10^{-7} mbar to ensure enough atomic hydrogen arriving at the substrate surface.

The wet chemical cleaning for relaxed $Si_{0.3}Ge_{0.7}$ substrates is slightly different. The first cleaning process of the ultrasonic bath with organic solutions is the same. Then, the oxide on the substrates were removed by a mixed solution of HF:HCl:H_2O with 2:1:4 ratio for 30 sec. The substrates surface was reoxidised by a mixed solution of $NH_3{\cdot}H_2O$:H_2O_2:H_2O with 1:1:4 ratio for 30 sec. These two steps are repeated once. The final oxide on the surface was removed by a mixed solution of HF:HCl:H_2O with a $2:1:4$ ratio for 20 sec and a mixed solution of HF:H_2O with 1:4 ratio for 20 sec. The substrates are supposed to exhibit hydrophobic surfaces. However, there is often little residual water on the relaxed $Si_{0.3}Ge_{0.7}$ substrate, whereas normally no residual water occurs on the relaxed $Si_{0.7}Ge_{0.3}$ substrates or the SOI. Therefore, blow dry is required here. After a short dip in deionised water to avoid the risk from the high-concentration HF, the substrate surface was blow dried and then put into the UHV system. Except the chemicals mentioned in two paragraph before, the chemicals $NH_3{\cdot}H_2O$(30 %) and HCl(36 %) have purity grades of very large scale integration (VLSI) quality Selectipur® from BASF.

Growth Processes

An example of a $^{28}Si_{0.7}Ge_{0.3}$ heterostructure on a relaxed $Si_{0.7}Ge_{0.3}$ substrate for electron spin qubits is schematically illustrated in Figure 2.3 (a). The MBE growth process of this heterostructure corresponding to the growth temperature is presented in Figure 2.3 (b). The substrate is cleaned ex-situ and in-situ at 700 °C as described above. Then the sample temperature is cooled down to 500 °C for growth. Firstly, a 300 nm thick

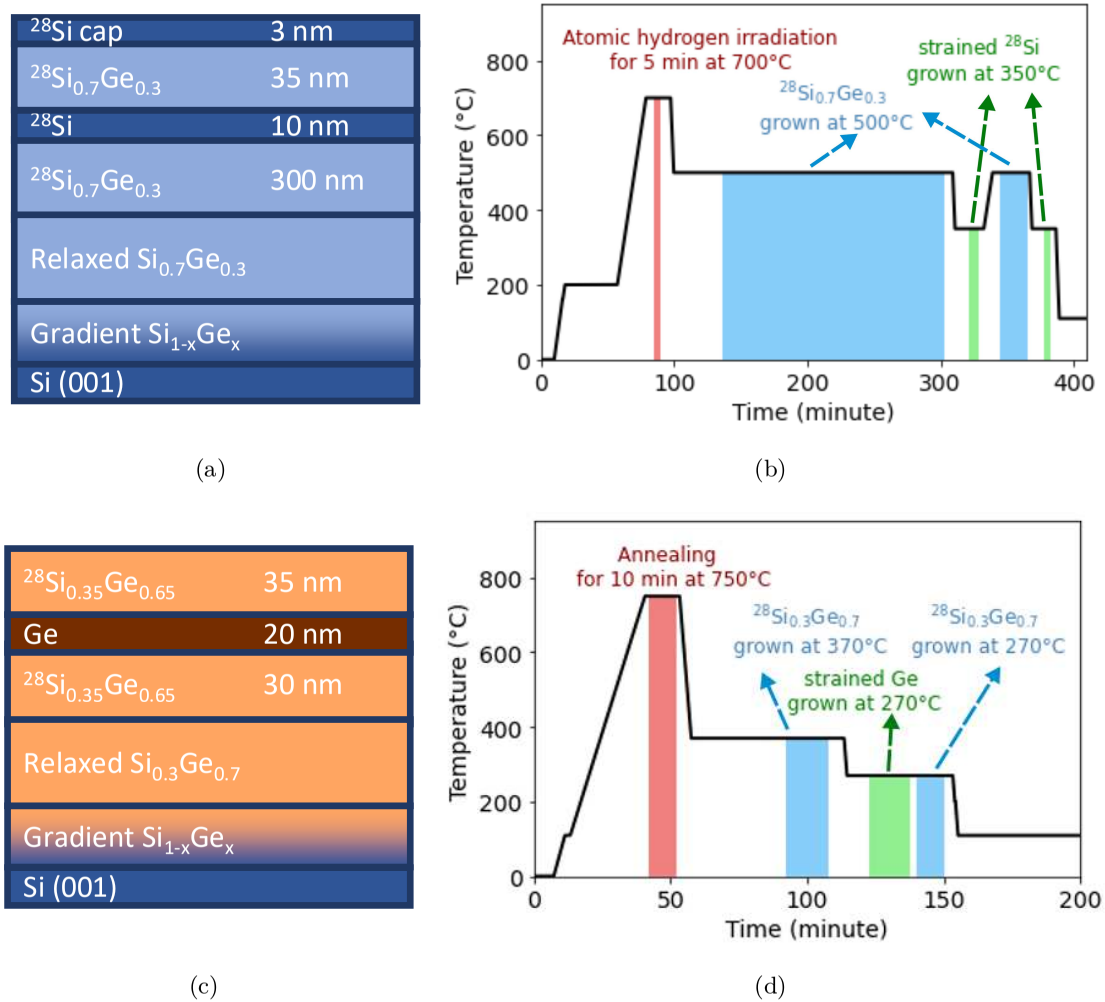


Figure 2.3: (a) An example of a schematic $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ heterostructure on a relaxed $Si_{0.7}Ge_{0.3}$ substrate for electron spin qubits and (b) its MBE growth process corresponding to growth temperature . (c) An example of a schematic $^{28}Si_{0.3}Ge_{0.7}/Ge/^{28}Si_{0.3}Ge_{0.7}$ heterostructure prototype on a relaxed $Si_{0.3}Ge_{0.7}$ substrate for hole spin qubits and (d) its MBE growth process corresponding to growth temperature.

$^{28}Si_{0.7}Ge_{0.3}$ layer was grown at 500 °C with a deposition rate of 0.03 nm s^{-1}. Next, the growth of the 10 nm ^{28}Si quantum well layer was carried out at 350 °C with a rate of 0.02 nm s^{-1}. Afterwards, a 35 nm thick $^{28}Si_{0.7}Ge_{0.3}$ cladding layer was grown under the same condition as the lower $^{28}Si_{0.7}Ge_{0.3}$ layer. In the end, a 3 nm protective ^{28}Si cap layer was deposited on top under the same condition as the Si quantum well layer. The ramping up and down rates for the temperature are 0.5 °C s^{-1} and 2 °C s^{-1}. Though, the cool down of the temperature is normally slower because the cooling is not as quick as 2 °C s^{-1} due to the lack of heat convection and conduction in the UHV environment.

In the case of ^{28}SOI growth, the surface preparation is the same as it is for a relaxed $Si_{0.7}Ge_{0.3}$ substrate. The process is simplified as a 400 nm ^{28}Si epitaxial layer is grown on a 70 nm thin SOI seed layer with a rate of 0.02 nm s^{-1} at 500 °C.

Figure 2.3 (c) and (d) show the schematic layer stack and also the MBE growth process example of a $^{28}Si_{0.3}Ge_{0.7}$ heterostructure on a relaxed $Si_{0.3}Ge_{0.7}$ substrate for hole spin qubits. After ex-situ wet chemical cleaning, the substrate is heated up and annealed at 750 °C for 10 min. Following, the substrate is cooled down to 370 °C. The 30 nm $^{28}Si_{0.3}Ge_{0.7}$ was grown with an applied growth rate of 0.033 nm s^{-1} at 370 °C. Afterwards, 20 nm Ge was grown at 270 °C with a growth rate of 0.023 nm s^{-1}. In the end, the top 35 nm $^{28}Si_{0.3}Ge_{0.7}$ layer was grown at 270 °C also with 0.033 nm s^{-1}.

2.1.2 Reduced Pressure Chemical Vapor Deposition

In the following, SiGe epitaxy by reduced pressure CVD is briefly introduced. Further information can be found in a book chapter written by Tillack and Murota [91].

The CVD growth in this work is either performed by the colleagues in IHP or the colleagues in Siltronic.

CVD Overview

CVD is the key technique to realise SiGe epitaxy on a large wafer scale beyond 200 mm. In the early time, CVD growth of Si films was commonly performed at high temperatures above 1000 °C [92]. By applying the CVD in UHV chambers, the growth temperature is successfully reduced to around 500 °C for high quality layers [93, 94, 95]. The reduction of

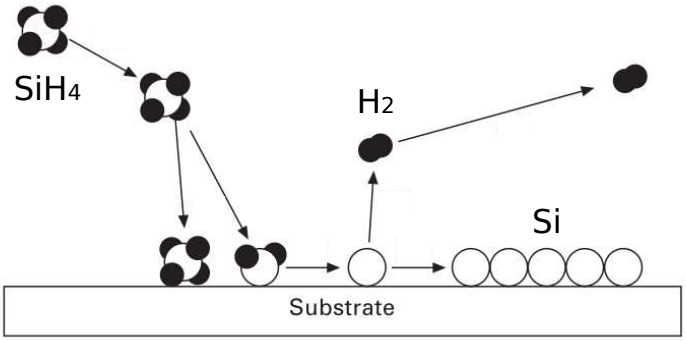


Figure 2.4: CVD reactions of Si, Ge epitaxy on a substrate. The drawing is copied from [91].

the growth temperature suppresses the oxygen and moisture levels, and also the diffusion of the atoms in the film. This growth temperature reduction consequently makes the growth of sophisticated SiGe heterostructures possible. The integration of the hot wall technology [96] and the load lock [97] to the CVD growth chamber makes it possible to perform CVD growth of Si film in a chamber with higher pressure than a UHV chamber. Nowadays, uniform Si films or SiGe heterostructures can be grown in high-throughput commercial CVD chambers on a large scale such as 300 mm [98].

The CVD reaction of Si, Ge epitaxy is illustrated in Figure 2.4. The precursors are often SiH_4, Si_2H_6, SiH_2Cl_2, GeH_4, and optionally some gas for doping. The precursors are transported with the carrier gas onto the wafer and adsorbed or chemisorbed at the wafer surface. The chemical reactions happen at the hot wafer surface, resulting in the epitaxial layer growth. The volatile reaction products are released from the wafer after the reactions and transported out with carrier gas.

Set-up

The epitaxial growth of SiGe/Si/SiGe heterostructures investigated in subsection 5.2.1 and also the relaxed $Si_{0.7}Ge_{0.3}$ substrates described in section 2.1.1 were carried out on 200 mm (0 0 1) Si wafer by utilising an ASM Epsilon 2000^{TM} reduced pressure CVD system (Figure 2.5). Respectively, the relaxed $Si_{0.3}Ge_{0.7}$ substrates were grown on a 300 mm (0 0 1) Si wafer in an ASM Epsilon 3200^{TM} CVD system. In these systems, the substrates are heated with halogen tungsten lamps.

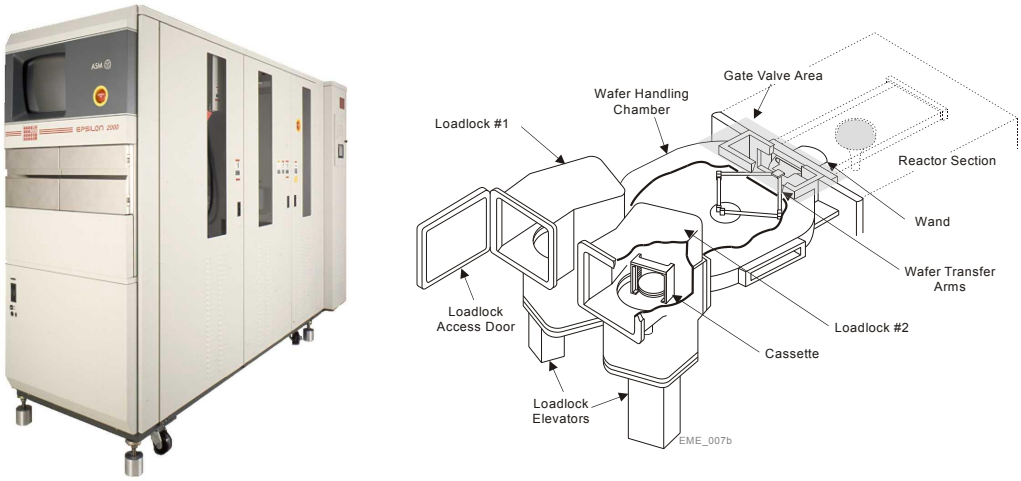


Figure 2.5: Example of an ASM Epsilon 2000^{TM} single wafer RPCVD reactor and the corresponding schematic illustration [99].

Growth

In the case of the relaxed $Si_{0.7}Ge_{0.3}$ substrate, the Si wafer is loaded into the reduced pressure CVD reactor after HF cleaning and baked at 1000 °C in H_2 to remove the residual oxide. Then, the wafer is cooled down to the SiGe growth temperature. In the case of relaxed $Si_{0.7}Ge_{0.3}$ buffer growth, step-gradient SiGe layers were deposited using a SiH_4-GeH_4 gas mixture with H_2 carrier gas. Finally, a thick 30 % constant composition SiGe layer is deposited. In order to enhance relaxation and improve the crystal quality of the relaxed SiGe buffer, annealing in H_2 is performed after each SiGe deposition step. Afterwards, the periodic surface roughness (often called cross hatch pattern) was removed by a chemical mechanical polish.

For the SiGe/Si/SiGe heterostructures, the strained Si layer is deposited using a H_2-SiH_4 gas mixture at 700 °C on the top of the relaxed $Si_{0.7}Ge_{0.3}$ buffers. An upper $Si_{0.7}Ge_{0.3}$ cap is deposited using the same process condition followed by an additional 2 nm Si cap for surface protection.

The epitaxial growth of the relaxed $Si_{0.3}Ge_{0.7}$ substrates [100, 101] performed with the precursor gases $GeCl_4$, SiH_2Cl_2 as well as H_2 as carrier gas at atmospheric pressure and at temperatures more than 800 °C. The substrate consists of a 4.9 µm graded part

with an average grade rate of around 15 % µm^{-1} from $Si_{0.3}Ge_{0.7}$ and a 1.6 µm constant composition layer of $Si_{0.3}Ge_{0.7}$. The same as above, a post-epitaxy chemical mechanical polishing removed the cross hatch surface roughness.

2.2 Heterostructure Characterisation

2.2.1 X-ray Diffraction

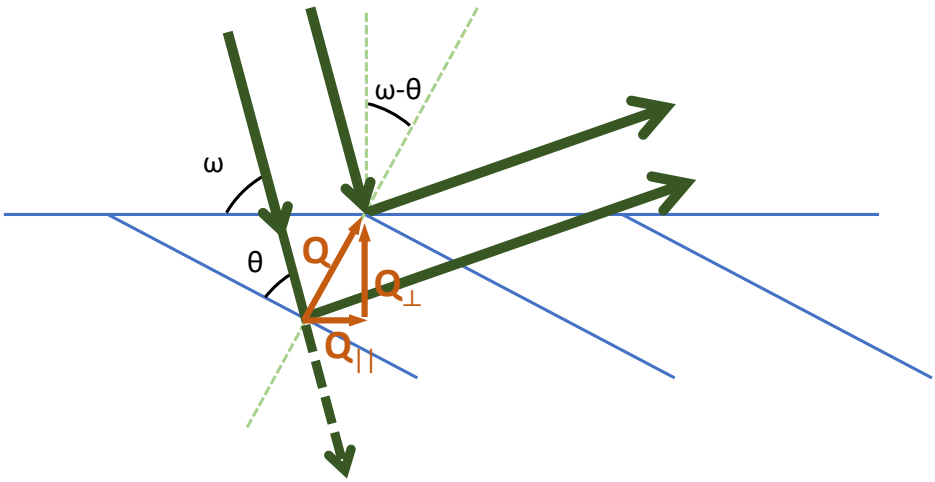


Figure 2.6: Schematic of the Bragg's law about the XRD at an asymmetric reflection.

Monochromatic and parallel X-ray beams can be diffracted at crystal planes (Figure 2.6), which is called X-ray diffraction (XRD). According to Bragg's law, the diffraction happens at constructive interference,

$$n\lambda = 2d_{hkl}\sin(\theta). \tag{2.1}$$

Here, n describes the order of constructive interference, λ is the X-ray wavelength, d_{hkl} is the crystal plane spacing with miller index (h k l), θ is the incident beam angle. Bragg's law can be also written as the scattering vector of the crystal planes $\mathbf{Q}$ equals to the difference of the scattered and incident X-ray wavevectors $\mathbf{K}_{s,i}$,

$$\mathbf{Q} = \mathbf{K}_s - \mathbf{K}_i. \tag{2.2}$$

The $\mathbf{Q}$ and $\mathbf{K}_{s,\,i}$ are calculated by

$$|\mathbf{Q}| = \frac{2\pi}{d_{hkl}}, \tag{2.3}$$

$$|\mathbf{K}_{s,\,i}| = \frac{2\pi}{\lambda}, \tag{2.4}$$

$$|\mathbf{K}_s - \mathbf{K}_i| = \frac{4\pi}{\lambda}\sin(\theta). \tag{2.5}$$

$\mathbf{Q}$ can be also written in terms of the components $\mathbf{Q}_{x,\,y,\,z}$ in reciprocal space, which are equal to the reciprocal vectors $h\mathbf{r}_1, k\mathbf{r}_2, l\mathbf{r}_3$ for the diffracted crystal planes,

$$\begin{aligned}\mathbf{Q} &= \mathbf{Q}_x + \mathbf{Q}_y + \mathbf{Q}_z \\ &= h\mathbf{r}_1 + k\mathbf{r}_2 + l\mathbf{r}_3 \\ &= h \cdot 2\pi\frac{\mathbf{a}_2 \times \mathbf{a}_3}{\mathbf{a}_1 \cdot (\mathbf{a}_2 \times \mathbf{a}_3)} + k \cdot 2\pi\frac{\mathbf{a}_3 \times \mathbf{a}_1}{\mathbf{a}_1 \cdot (\mathbf{a}_2 \times \mathbf{a}_3)} + l \cdot 2\pi\frac{\mathbf{a}_1 \times \mathbf{a}_2}{\mathbf{a}_1 \cdot (\mathbf{a}_2 \times \mathbf{a}_3)}.\end{aligned} \tag{2.6}$$

where $\mathbf{a}_{1,\,2,\,3}$ are the lattice vectors and $\mathbf{r}_{1,\,2,\,3}$ are the reciprocal lattice vectors.

By two-dimensional X-ray scanning in 2θ and ω, the reciprocal lattice vector components $\mathbf{Q}_{\parallel,\,\perp}$of certain reflections from certain crystal planes and furthermore the lattice vectors, strains, and compositions of the crystal can be investigated. This method is called reciprocal space mapping. The reciprocal lattice vector components $\mathbf{Q}_{\parallel,\,\perp}$ are the in-plane and out-of-plane components of the scattering vector $\mathbf{Q}$ (Figure 2.6). This means,

$$\mathbf{Q}_{\parallel} = \mathbf{Q}_x + \mathbf{Q}_y, \tag{2.7}$$

$$\mathbf{Q}_{\perp} = \mathbf{Q}_z. \tag{2.8}$$

As it is illustrated in Figure 2.6, the conversion from the two-dimensional X-ray scanning in 2θ and ω to the reciprocal space map is given by

$$\begin{aligned}|\mathbf{Q}_{\parallel}| &= |\mathbf{Q}|\sin(\omega - \theta) \\ &= \frac{4\pi}{\lambda}\sin(\theta)\sin(\omega - \theta),\end{aligned} \tag{2.9}$$

$$\begin{aligned}|\mathbf{Q}_{\perp}| &= |\mathbf{Q}|\cos(\omega - \theta) \\ &= \frac{4\pi}{\lambda}\sin(\theta)\cos(\omega - \theta).\end{aligned} \tag{2.10}$$

In heterostructures, each layer with different lattice parameters has its own reflections for each set of crystal planes in the reciprocal space map.

In this work, XRD reciprocal space mapping analysis was applied to analyze the strain and composition of the layers in the SiGe heterostructure with a Rigaku Smartlab diffractometer. In the XRD measurement, a Cu-K_{a1} X-ray source and a HyPix-3000 position sensitive area detector for fast two-dimensional mapping were employed.

2.2.2 Transimission Electron Microscopy

To investigate the objects within nm scale, such as the heterostructures in Figure 1.3 and Figure 1.5, microscopy with fine resolutions is demanded. The microscopic resolution d of the microscopy depends on its wavelength λ and the numerical aperture NA of the optical component [102],

$$d = \frac{\lambda}{2\,NA}. \tag{2.11}$$

In an optical microscope, $\lambda > 380\,\text{nm}$, that means the resolution of an optical microscope is also in the range of hundreds of nm.

Respectively, a beam of accelerated electrons can be also used as the illumination source for microscopy, which is called electron microscopy. Electron microscopy can reach high resolution with the electron beam of lower wavelength λ, which consists of electrons with high energies E. According to de Broglie equation [103],

$$\lambda = \frac{h}{mv}, \tag{2.12}$$

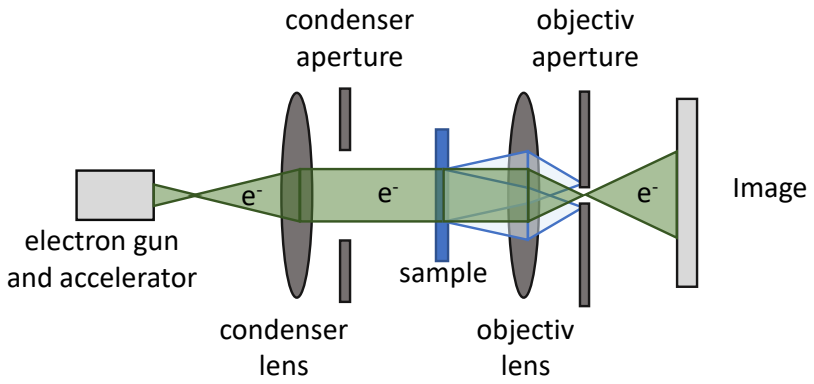
$$E = eU = \frac{1}{2}mv^2. \tag{2.13}$$

Here, h is the Planck constant, m, v, e is the electron mass, velocity, charge, and U is the acceleration voltage applied. The wavelength λ of the electrons of tens of keV scanning electron microscopy (SEM) or hundreds of keV in transmission electron microscopy (TEM) are around 0.01 nm to 0.1 nm, that yields much higher resolution than optical microscopes. Compared to the optical lens often made by concave and convex glasses, the lens in electron microscopy consists of electromagnetic fields.

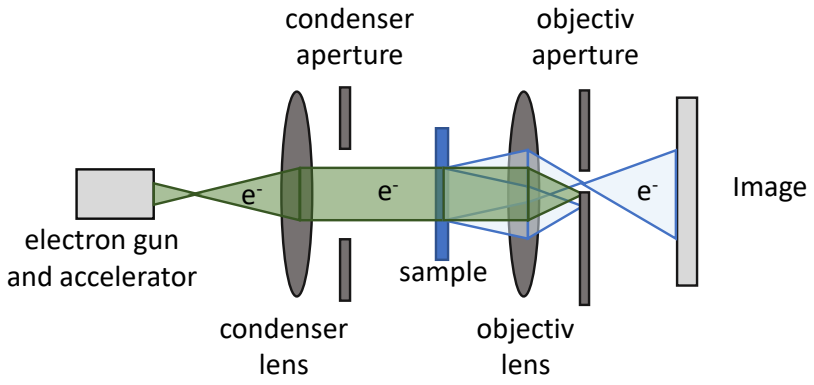
One of the main characterisation methods applied in this work is TEM. In particular, high angle annular dark field (HAADF) scanning TEM (STEM) is applied for cross-section view of the SiGe heterostructures and the bright field TEM is applied for the plan-view TEM for defect investigation, particularly, dislocation analysis.

Bright Field TEM

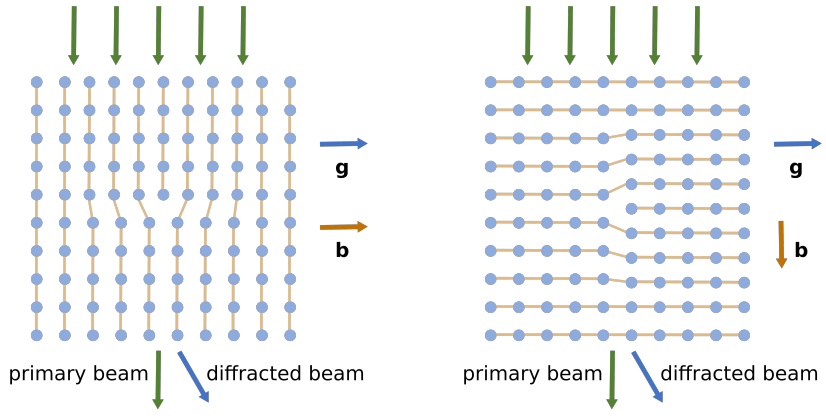
The bright field TEM is schematically illustrated in Figure 2.7. The electrons are emitted from a tungsten filament and then accelerated with a voltage of several hundred kV.



(a)



(b)



(c) (d)

Figure 2.7: Optic ray diagrams for performing (a) rudimentary bright field and (b) diffraction bright field imaging in TEM. The visibility of the dislocations with Burgers vectors $\mathbf{b}$ in the diffraction condition of $\mathbf{g}$: (c) the dislocation is visible when $\mathbf{g} \cdot \mathbf{b} \neq 0$; (d) the dislocation is invisible when $\mathbf{g} \cdot \mathbf{b} = 0$.

A parallel electron beam is collimated by the condenser lens and the aperture. This high-energy electron beam can transmit a sample up to several µm [104]. Afterwards, the objective lens is applied to converge the beams through the sample. In the rudimentary bright field TEM imaging mode (Figure 2.7 (a)), the primary beam through the sample is utilized, that means the objective lens will only let the primary beam through and forms the image.

Similar to the description of XRD in subsection 2.2.1, the coherent electrons can be diffracted by the crystal sample at certain planes with the diffraction vector **g**. The diffracted beam can also be applied to image the sample (Figure 2.7 (b)). The lattice displacement induced by lattice defects leads to contrasts in the images of the diffracted beams [105]. This allows for analysis of defects, such as dislocations (Figure 2.7 (c)). The lattice displacement **R** induced by dislocations in the general case (screw, edge and mixed) is:

$$\mathbf{R} = c_1\mathbf{b} + c_2\mathbf{b}_e + c_3\mathbf{b} \times \mathbf{l}. \tag{2.14}$$

Here, $c_{1,2,3}$ are material related parameters, **b** is the Burgers vector of the dislocation, $\mathbf{b}_e$ is the Burgers vector of the dislocation edge component, and **l** is the unit vector along the dislocation line. When

$$\mathbf{g} \cdot \mathbf{R} = 0, \tag{2.15}$$

the amplitude of the diffracted beams is not influenced by the lattice displacement of the dislocation. This leads to the invisibility of the dislocation in the image.

Mostly, the dislocation is invisible already when

$$\mathbf{g} \cdot \mathbf{b} = 0, \tag{2.16}$$

is satisfied. For a screw dislocation, $\mathbf{b} \times \mathbf{l}$ has the same direction as **b** and it has no edge component. Therefore, when Equation (2.16) and Equation (2.15) are fulfilled automatically at the same time. For a dislocation containing some edge component, it remains a weak contrast when Equation (2.16) is fulfilled, but

$$\mathbf{g} \cdot \mathbf{b} \times \mathbf{l} \neq 0, \tag{2.17}$$

However, this weak contrast is also barely detectable since $c_{2,3}$ are much smaller than c_1 in Equation (2.14).

According to this, the Burgers vector of the dislocations can be analysed based on the visibilities of the dislocations in different diffraction conditions.

HAADF STEM

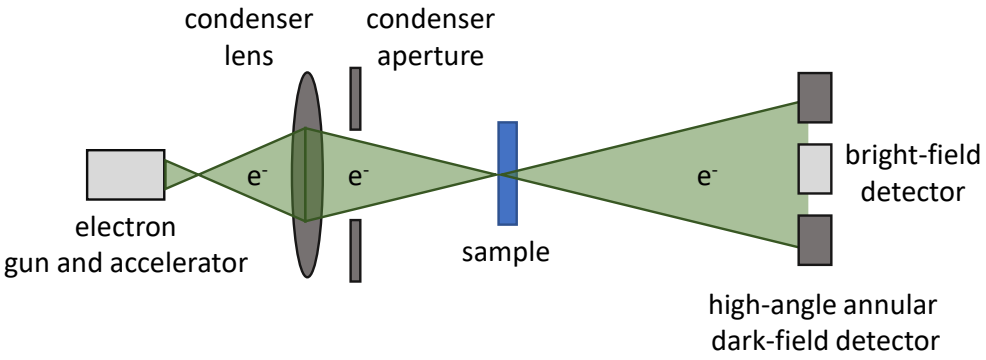


Figure 2.8: Optic ray diagrams for performing STEM.

The imaging mechanism of a STEM is quite different from TEM. In STEM, an electron beam is converged and focused on the sample by the condenser lens and aperture. The transmitted beam through the sample is divergent. The sample imaging is performed by scanning the sample with the focused electron beam and detecting the primary electrons and the scattered electrons in low angles (bright field imaging) or detecting the scattered electron in higher angles (dark field imaging). A high angle annular dark field (HAADF) detector typically located at around several tens of mrad is often applied in STEM, where the exact angle depends on the STEM geometry. The signal from the coherently (Bragg) scattered electrons is weak at high angles. Instead, the electrons scattered by thermal diffuse, which means by phonons, are dominated. The thermal diffuse scattering increases with the atomic number Z of the sample [106, 107]. This results in contrasts in HAADF STEM images of samples with different atomic numbers, called Z-contrasts. These contrasts can be applied for quantitative analysis of the local alloy compositions of the TEM samples.

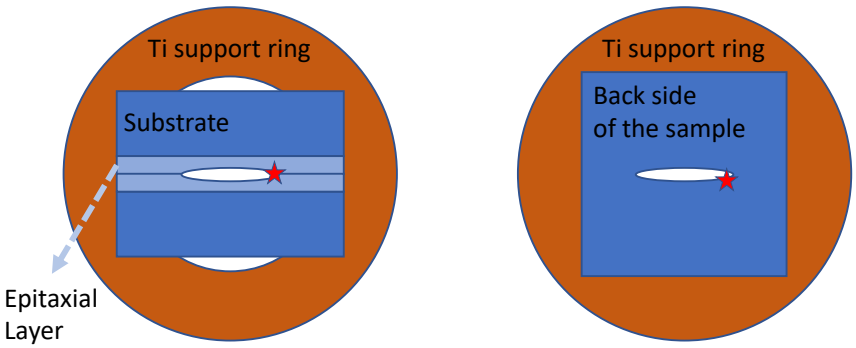
Set-up

In this work, TEM and STEM measurements have been performed with an FEI Titan 80-300 operated at an acceleration voltage of 300 KeV. The microscope is equipped with an aberration corrector for the objective lens and a field emission gun (FEG) as the electron source.

STEM imaging has been performed with a focused, convergent beam. STEM-HAADF images have been recorded with a Fishione model 3000 annular detector.

TEM Sample Preparations

Semiconductor samples for TEM and STEM need to be thinned down to hundreds of nm to reach decent signals of transmitted electrons [105].



(a) (b)

Figure 2.9: Schematic diagram showing the geometry of (a) cross-section and (b) plan-view specimens prepared for TEM investigation. The areas of interest are highlighted with stars.

In this work, the cross-view TEM sample (Figure 2.9 (a)) are prepared by the processes listed below:

i. Two pieces are cut from the samples glued face to face with regards to the epitaxial layers by Gatan G1 two-component epoxy resin and heated to 150 °C.

ii. The face to face sample piece is further cut and thinned down by polishing on several diamond lapping foils with decreasing grain sizes from 30 µm down to 0.1 µm.

iii. The polished side is glued on a titanium (Ti) support ring and further thinned down from the other side to $10 - 20$ µm also with the same diamond lapping foils with grain sizes down to 0.1 µm.

iv. The sample is put into a Gatan precision ion polishing system for ion milling with two Ar^+ ion beams at an energy of 3 kV and at ±4° incident angle. When the hole is obtained in the center of the sample, the ion milling is switched to a cleaning process by step-wise lowering the ion energy down to 0.1 kV and increasing the angle to 7° to remove amorphous materials on the sample created from the ion milling.

It is worth mentioning that, the amorphous materials on the TEM sample can hinder the quantitative analysis, for example, the atomic composition analysis and the interface diffusion analysis [108].

The cross-section sample for STEM imaging is typically prepared by a surface direction of [1 1 0].

The plan-view TEM sample (Figure 2.9 (b)) preparation technique is similar to the cross-view TEM. Instead of glueing a face to face sticked sample on the Ti support ring, a sample piece is glued on a ring with the epitaxial layer side facing the ring. Only the back side of the sample is polished. Respectively, during ion milling on the plan-view TEM sample, the two ion beams mill the sample from the top at a 5° incident angle.

2.2.3 Scanning Electron Microscopy

SEM has a similar configuration as TEM (Figure 2.10 (a)), except that the electron beam (several keV to several tens of keV) has much less energy than TEM (normally more than hundreds of keV). The convergent primary beam is focused on the sample and generates secondary electrons as well as backscattered electrons. By scanning the sample with the primary beam, the sample information like surface topography, composition or defects can be explored.

Electron Channelling Constrast Imaging

In this work, we focus on the electron channelling contrast imaging (ECCI) technique in SEM [109, 110]. The primary electrons can channel into the crystal planes at certain angles (Figure 2.10 (b)), which are called open channels. Respectively, at certain angles, the primary electrons are backscattered (Figure 2.10 (c)), which are called close channels.

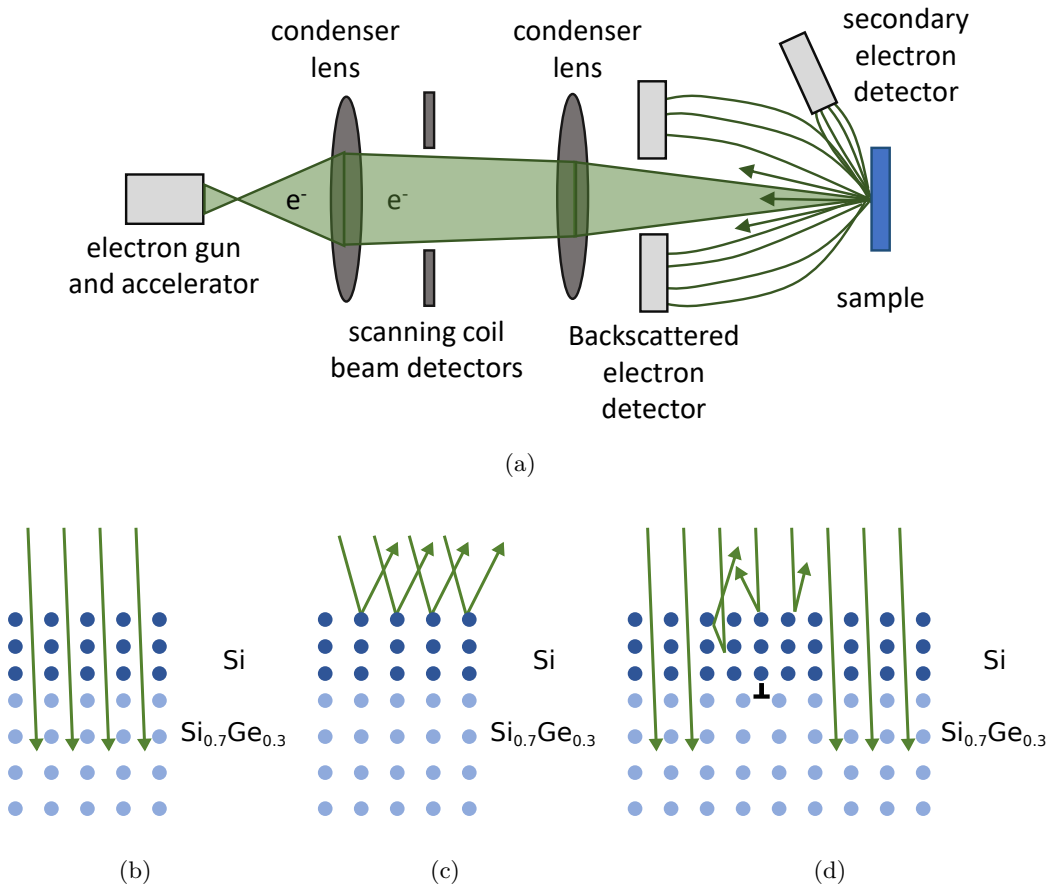


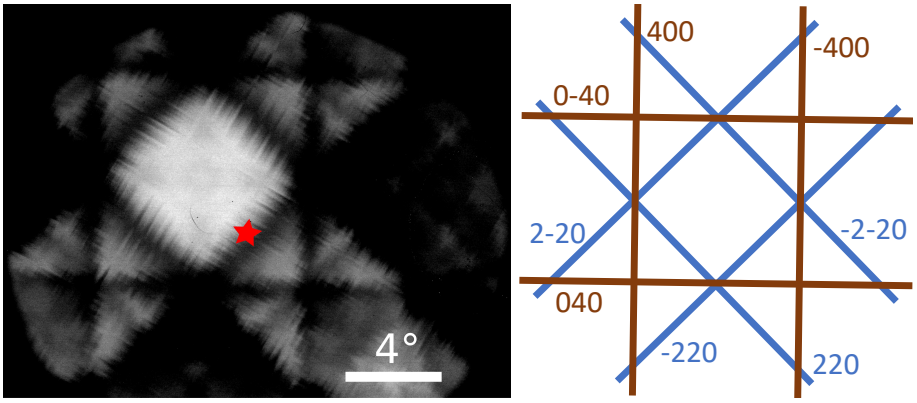
Figure 2.10: (a) Optic ray diagrams for performing SEM. Schematic representations of the electron channelling situations in crystals: (b) open channel, (c) closed channel, (d) dislocation induced conversion from open channel to close channel.

A crystal defect, such as a dislocation can induce the conversion from open channel to close channel (Figure 2.10 (d)) and cause the contrast in the image. Therefore, by collecting the backscattered electrons, it is able to probe the dislocations in the crystal structures.

During ECCI measurement, electron channelling pattern is formed at low magnification due to the Kikuchi diffraction[1] of the incident electrons (Figure 2.11 (a)). When the diffraction condition is satisfied, the channelling is in an open channel, resulting in a dark line, called Kikuchi line. The Kikuchi lines are indexed in (Figure 2.11 (b)) regarding to

[1]Kikuchi diffraction originates from multiple coherent and incoherent scattering processes in crystal, in contrast that Bragg diffraction originates of coherent scattering in crystal.

the diffractions. By transitioning to the higher magnification with defined diffractions in the electron channelling patterns, we can image the defects like dislocations by the diffraction contrasts in the images. The Burgers vector analysis of the dislocations is also possible by comparing the dislocation contrasts when applying certain diffraction conditions [111, 112].



(a) (b)

Figure 2.11: (a) Experimental electron channeling patterns and (b) its corresponded indexed diagram. The ECCI image with higher magnification at the point marked with a star in (a) is shown in Figure 5.9 (a).

One example of the electron channelling patterns and its related diffractions are shown in Figure 2.11. By zooming in the area marked with the star, ECCI image in Figure 5.9 (a) is obtained under the diffraction at $\bar{2}\,2\,0$.

Set-up

ECCI measurements were performed in a Thermo Fisher Scientific's Apreo scanning electron microscope (SEM), operated at 5...10 kV, and an approximate beam current of 3.2 nA. The images were taken by an in-lens detector which is located at the entry of the pole piece and acts as an integrated annular backscattered electron detector. It allows for backscatter imaging at voltages as low as 2 kV.

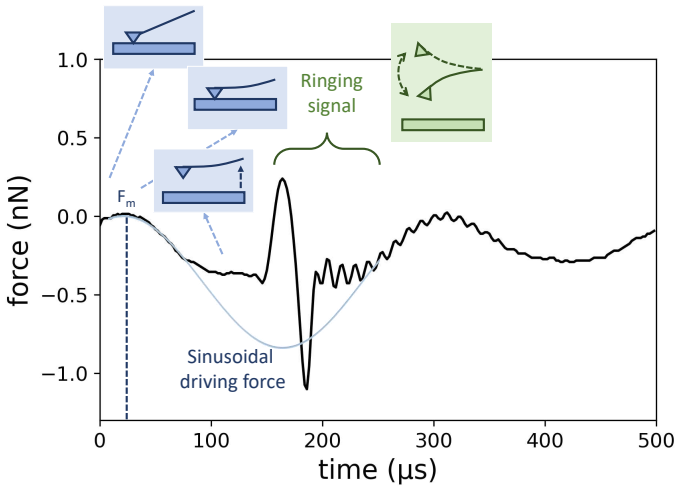
2.2.4 Atomic Force Microscopy

Atomic force microscopy (AFM) is a sensitive method to investigate the physical properties of the sample surface. The general information of AFM can be found in the book chapter written by de Pablo [113]. Here, we will briefly introduce the ScanAsyst^{TM} mode of AFM applied in this work. ScanAsyst^{TM} is a highly automated mode based on the Peak Force Tapping^{TM} technique. Both ScanAsyst^{TM} and Peak Force Tapping^{TM} are developed by Bruker-Nano Inc.

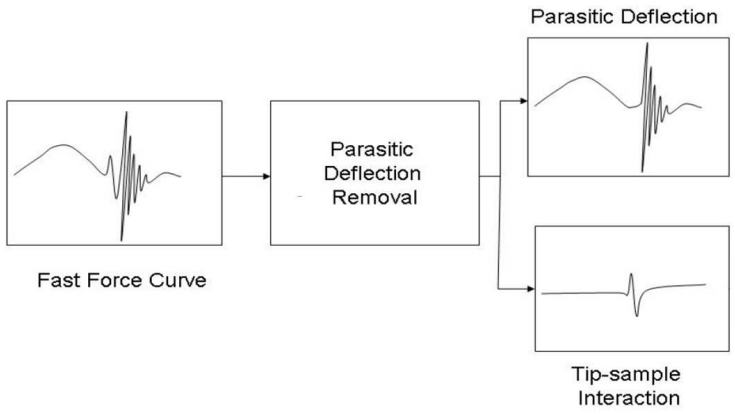
At every measurement point of AFM measurement with Peak Force Tapping^{TM} mode, a fast force curve is applied and recorded on the AFM cantilever for analysis [114, 115]. One exemplary fast force curve measured in this work is presented in Figure 2.12 (a). Firstly, a sinusoidal wave is applied on the driving force. The maximum interaction force $\mathbf{F}_m$ happens during a half period of the sinusoidal wave. After a half period of the sinusoidal wave, the cantilever is moved away from the sample. During removing the cantilever, the force is oscillated due to the cantilever resonance so that the ringing signal is obtained. The frequency of the ringing signal is much higher than the driving sinusoidal wave. Through this way, the ringing signal and the sinusoidal driving force are separated from each other. Through a separation of both the sinusoidal driving force signal and the ringing signal (both contributing to parasitic deflection) from the force signal by algorithm, the signal of the interaction between the tip and sample can be extracted. One exemplary analysis process from the reference[114] is shown in Figure 2.12 (b). From the signal of interaction between the tip and the sample, the sample topography can be analysed.

ScanAsyst^{TM} mode is further developed based on Peak Force Tapping^{TM} mode, that the scan parameters, such as setpoint and scan rate, are automatically adjusted during the measurement by intelligent algorithms.

In this work, a Bruker ICON AFM is applied. All the topographical AFM measurements were performed in ScanAsyst^{TM} mode.



(a)



(b)

Figure 2.12: (a) An exemplary fast force curve at an AFM measurement point in the Peak Force Tapping™ mode. The movements of the cantilever are also illustrated here. (b) Schematics of the parasitic deflection signal removal from fast force curve in Peak Force Tapping™ mode, reproduced from [114] with permission.

2.2.5 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy (SIMS) is often applied to analyse the composition, as well as the impurity concentrations of solid materials. Both time-of-flight (ToF) SIMS and dynamic SIMS are applied in this work. Both SIMS measurements occur in a high vacuum at roughly 10^{-6} mbar.

In ToF SIMS (Figure 2.13 (a)), the accelerated primary ions from the analysis ion gun scan the sample surface and then release the secondary ions from the sample out, including the atomic ions and cluster ions. The ions fly passing by a reflector to the detector. The flight time depends on the mass of the ions - the heavier ions fly slower. Therefore, the ion amount versus mass can be analysed by detecting the ion dose versus time. Afterwards, the quantitative concentration is determined by comparing the signal with the reference sample. The reference sample consists of the same materials as the measurement sample but the amount of atoms of interest in the reference sample is known. Here, the energy of the primary ion beam of the analysis ion gun is so small that the sample is not etched much from it. To get the depth profile of the composition or the impurity concentration, the solid materials are etched for every measurement point by ion beams with higher power from a sputter gun than the analysis ion gun.

In the ToF SIMS applied, the analysis ion beam consists Bi^+ ions of 25 kV, 1 pA, while the sputter ion beam consists Cs^+ ions of 1 kV, tens of nA. The analysis scan area is $100 \times 100\,\mu m^2$, while the sputter scan area is more than four times larger than the analysis scan area.

In dynamic SIMS (Figure 2.13 (b)), the primary ion beam has much higher power than the primary ion beam in ToF SIMS. It acts both as an analysis ion beam and a sputter ion beam. The sample is etched and analysed at the same time when the primary ions are sputtered on the sample. The secondary ions go through an electrostatic field working as an energy filter and a magnetic field working as a mass filter. Only the ions with a single charge and also a selected mass can arrive in the detector. This means that only limited atoms or clusters with certain atomic masses can be analysed in each dynamic SIMS measurement, whereas the atomic masses over the whole spectrum can be analysed in ToF SIMS. By comparing the signal intensity with the reference sample and also measuring ex-situ the etching depth by a depth profile, the depth profiler of atoms with certain masses can be obtained.

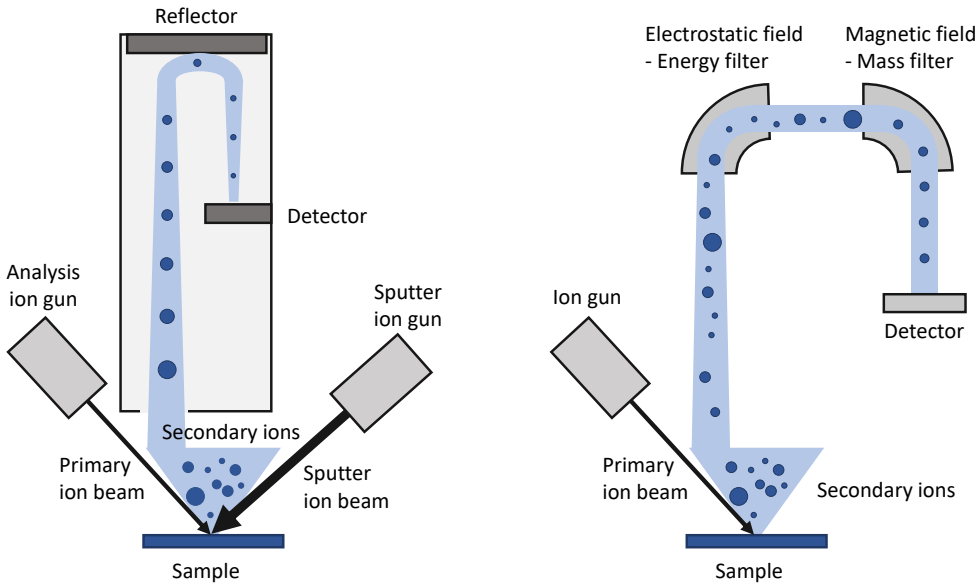


Figure 2.13: Schematic of (a) ToF-SIMS and (b) dynamic SIMS.

In the dynamic SIMS applied, the ion beam consists of Cs^+ ions of 14.5 kV, that is a sum of 10 kV acceleration energy and also 4.5 kV energy on the sample.

In this work, SIMS was applied to detect the isotopic impurities of Si, as well as the chemical impurities such as carbon and oxygen in Si and Ge related epitaxial layer.

God made the bulk; the surface was invented by the devil.

Wolfgang Pauli

3 Development for Isotope Engineered Molecular Beam Epitaxy

Despite the technical establishment and routine maintenance of isotope engineered MBE, such as UHV leakage inspection, source refilling and bake out, several scientific developments have been performed for the MBE growth. In this chapter, the development of reliable surface preparation processes of ^{28}SOI and $^{28}Si_{0.7}Ge_{0.3}$ substrates is demonstrated. Also, the ^{28}Si solid source evaporation in isotope engineered MBE is investigated.

3.1 Reliable Surface Preparation

One of the key processes to realise a high-quality ^{28}SiGe heterostructure for qubits or a high-quality ^{28}SOI with the isotope engineered MBE is to achieve epitaxy ready substrates with low impurities on the surface. This needs the development of reliable surface preparation processes. Both CVD grown SiGe substrates and SOI substrates mentioned in section 2.1.1 are exposed to air for sevaral days or up to sevaral months before the MBE growth. Hence, the surfaces are oxidised and also absorb organic contaminations [116, 117]. If no proper substrate surface preparation is performed to remove the impurities, defects, such as pits, mounds [118], and dislocations [119] can form in the epitaxial layers.

In this work, the surface cleaning process of $Si_{0.7}Ge_{0.3}$ substrates and SOI substrates has been focused on rather than $Si_{0.3}Ge_{0.7}$ substrates. The first two types of substrates behave close to Si substrates but $Si_{0.3}Ge_{0.7}$ substrates behave close to Ge substrates. An uncomplicated surface cleaning of Ge substrates without special treatment, such as ion sputtering, is even till now still an unsolved scientific question in the community [120].

Rapid annealing at more than 1000 °C is a typical and efficient pre-epitaxy preparation for Si substrates [121, 117] to remove both oxygen and carbon impurities on the surface. However, the annealing budget for the SOI substrates is quite low because the Si top layers on the thin SOI substrates dewet during annealing at 900 °C [122]. Annealing at over 1000 °C can also change the surface topography of $^{28}Si_{0.7}Ge_{0.3}$ substrates because of dislocation dynamics [123]. For these substrates, surface preparation processes at relatively low temperatures are required.

Atomic hydrogen irradiation is proposed to remove the carbon and oxygen impurities on the Si surface at around 700 °C [124, 125]. There are conflicting conclusions about the effect of atomic hydrogen irradiation on removing the carbon and oxygen impurities on Si surfaces in the works of Shimomura et al. [124] and Aßmuth et al. [125], whereas their results both show that atomic hydrogen irradiation is efficient to provide epitaxy ready Si surfaces.

The following discussions in the next paragraphs deal with the defects in the epitaxial layers induced by contaminations on the substrate. A reliable surface preparation combining an ex-situ wet chemical process and in-situ atomic hydrogen irradiation is then demonstrated.

Defects in Epitaxial Layer Induced by Contamination on Substrates

The surfaces of SOI substrates and the $Si_{0.7}Ge_{0.3}$ substrates behave close to Si. Let's have a look on the defects in (0 0 1) Si homoepitaxy induced by contaminations on the substrate surfaces.

Some former research works already show, that the surface topographies after pre-epitaxy annealing at temperatures between 800 °C and 1000 °C indicate the contaminations on the substrate surface. Jones and Palermo's work illustrates Si-on-Si nanostructures caused by annealing Si substrate with carbon contaminations and residual oxide in a UHV environment [126]. The same phenomenon was also observed by annealing SOI substrate [122].

To examine the contaminations on the (0 0 1) Si substrate before and after wet chemical cleaning in our lab, annealing in an MBE chamber was performed on these substrates with and without wet chemical annealing. The surface topographies of the Si substrates after

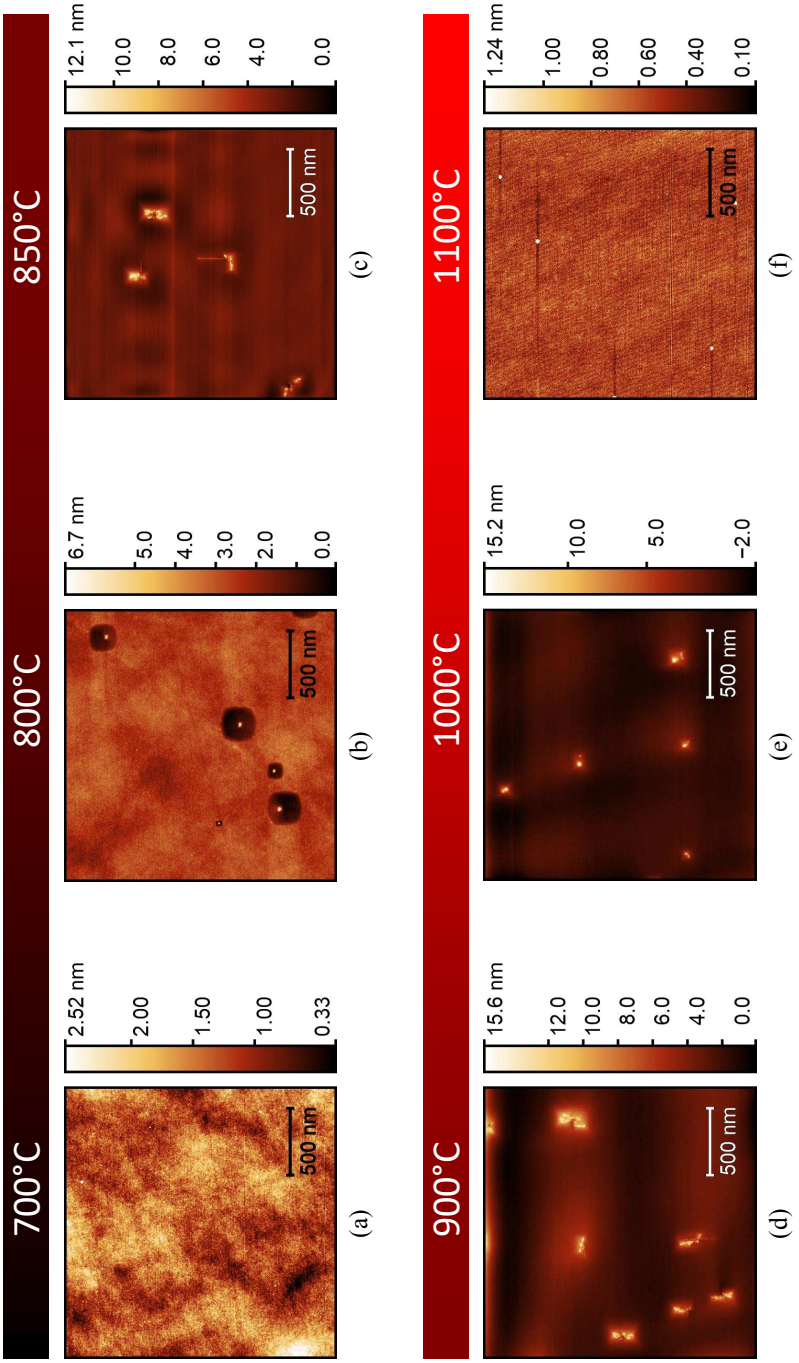


Figure 3.1: Surface topographies of Si substrates after annealing at different temperatures for 10 min. These are measured by AFM. The annealing temperatures are indicated above the image.

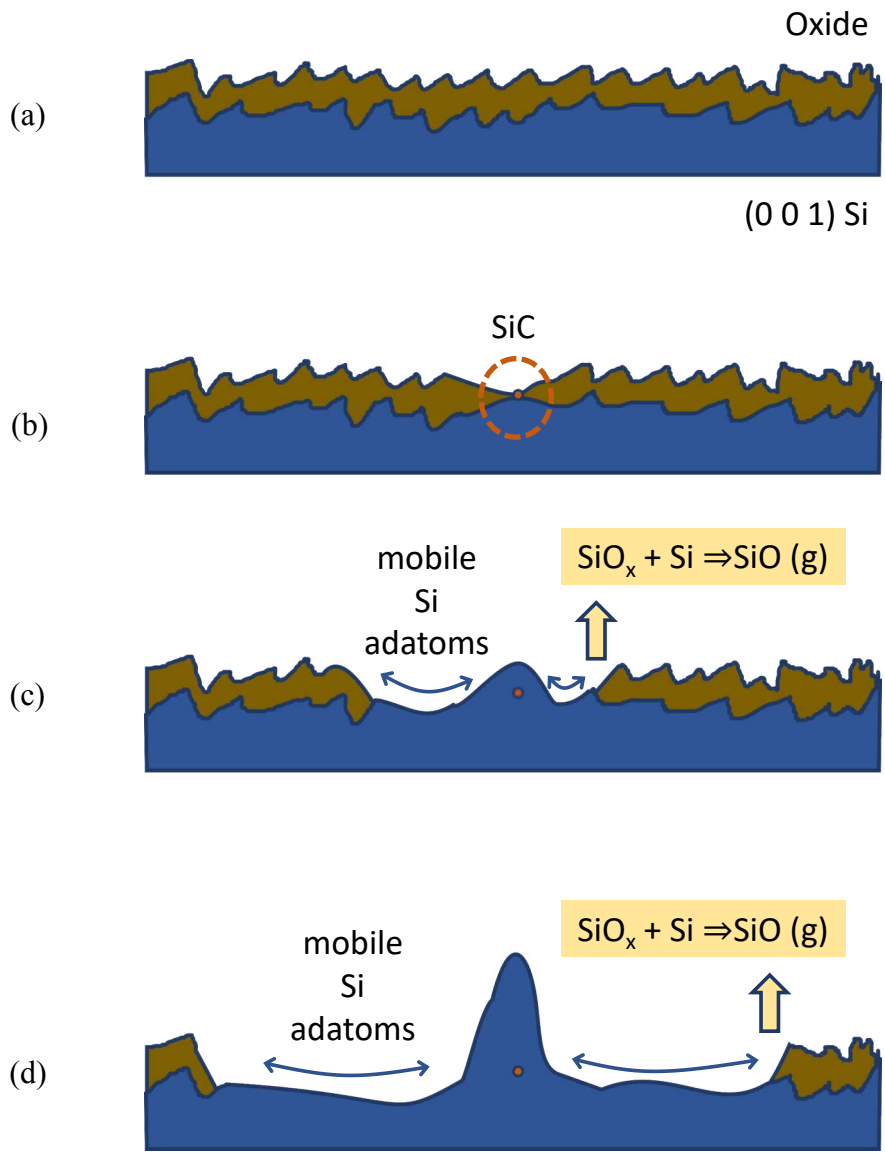


Figure 3.2: Mechanism Si-on-Si nanostructure formation. (a) A (0 0 1) Si substrate with native oxide on its surface. (b) During annealing in a UHV environment, SiC forms at relatively low temperature. (c) At around 800 °C, the native oxide starts to decompose preferably around the SiC since the decomposition spot here is exposed to the vacuum. Si adatoms on the surface are mobile where the oxide is already decomposed on the surface. And the mobile Si adatoms get trapped around SiC. (d) When being annealed further, the oxide void on the surface becomes larger and in the middle of the void, the Si-on-Si nanostructure gets larger around the SiC. The experimental results corresponding to this mechanism are presented in Figure 3.1. The mechanism is proposed by Jones et al. [126].

annealing at different temperatures were investigated by ex-situ AFM. The results are shown in Figure 3.1. Figure 3.1 (a) - (f) show the development of Si-on-Si nanostructure caused by both carbon contaminations and residual oxide on a (0 0 1) Si substrate without wet chemical cleaning. The development of these nanostructures can be understood according to the mechanism described by Jones and Palermo [126]. This mechanism is illustrated in Figure 3.2. Below 800 °C, the carbon contaminations react with Si and SiC spots are built randomly on the Si substrate. When the annealing temperature is elevated to 800 °C, the oxide starts to decompose according to the reaction,

$$\mathrm{SiO}_x + \mathrm{Si} \Rightarrow \mathrm{SiO\,(g)}. \tag{3.1}$$

This reaction happens firstly on the spot where SiC already formed and then in the area around this spot because the interfaces of Si and SiO_x are exposed to vacuum here. A void with the oxide-free area is created around SiC (Figure 3.1 (b)) due to the oxide decomposition. When the temperature rises further, several processes occur: the oxide decomposition continues around the void - the reaction happens preferably here because the SiO (g) can easily evaporate into the vapours where the interface between Si and SiO_x is exposed to the vacuum in stead at other locations on the surface; inside the oxide-free void, Si atoms are mobile; when the mobile Si meets the SiC, the SiC acts as a barrier then the Si atoms are trapped here and form nanostructures: At 850 °C, the oxide is completely decomposed and the nanostructures remain (Figure 3.1 (c)). At temperatures higher than 900 °C, the Si-on-Si nanostructures start to diffuse and become smaller (Figure 3.1 (e) and (f)). For the sample in Figure 3.1 (c), energy dispersive X-ray spectroscopy in SEM was performed: no detectable foreign elements as Si was found. We cannot exclude the presence of carbon because carbon is hard to detect in energy dispersive X-ray spectroscopy due to its rather small atomic number and the big excitation volume of energy dispersive X-ray in SEM.

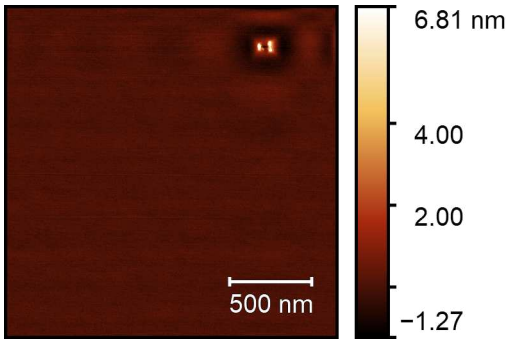


Figure 3.3: Surface topography of (0 0 1) Si substrate after wet chemical cleaning and annealing at 900 °C for 10 min, measured by AFM.

The Si substrate after the wet chemical cleaning process was also annealed at 900 °C. The same Si-on-Si nanostructures described above were observed except the density of these nanostructures was around 10 times less than the substrate without wet chemical cleaning. This indicates that there are still some carbon and oxide contaminations on the Si substrate after wet chemical cleaning.

The epitaxy growth of 50 nm ^{28}Si layers was grown by MBE at 500 °C on (0 0 1) Si substrate after wet chemical cleaning and pre-epitaxy annealing at different temperatures to examine the effect of the surface preparation on the epitaxial layers. The surface morphologies of these epitaxial layers are investigated by AFM and the results are presented in Figure 3.4. The epitaxial layer without pre-annealing doesn't coalesce (Figure 3.4 (a)). Though the epitaxial layer coalescence with a pre-epitaxy annealing at 700 °C or 900 °C, some square-like pits present on the epitaxial layer (Figure 3.4 (b), (d)). The pit marked in the blue rectangular in Figure 3.4 (b) is exhibited three dimensionally in Figure 3.4 (c). No clear facet can be observed in the pit. A smooth ^{28}Si epitaxial layer can be obtained without pits on top with a pre-annealing temperature of 1100 °C.

The pits formation mechanism was described by Sato et al. in 2005 [118]. When there are few SiC spots present on the Si substrate surface, the SiC spot acts as a pinpoint. It is difficult for Si to grow directly on these SiC spot. Then, pits form. It is also presumable that the Si-on-Si nanostructures in Figure 3.3 disturb the layer growth of Si and then pits form. With high pre-epitaxy annealing temperature as 1100 °C, both carbon contamination and oxide are removed [127]. Consequently, a smooth ^{28}Si epitaxy layer can be grown on a (0 0 1) Si substrate after it was annealed at 1100 °C.

Till here, it is clear that the non reliable surface preparation of Si substrates can cause the Si-on-Si nanostructures after annealing and later on the defects on the epitaxial layers.

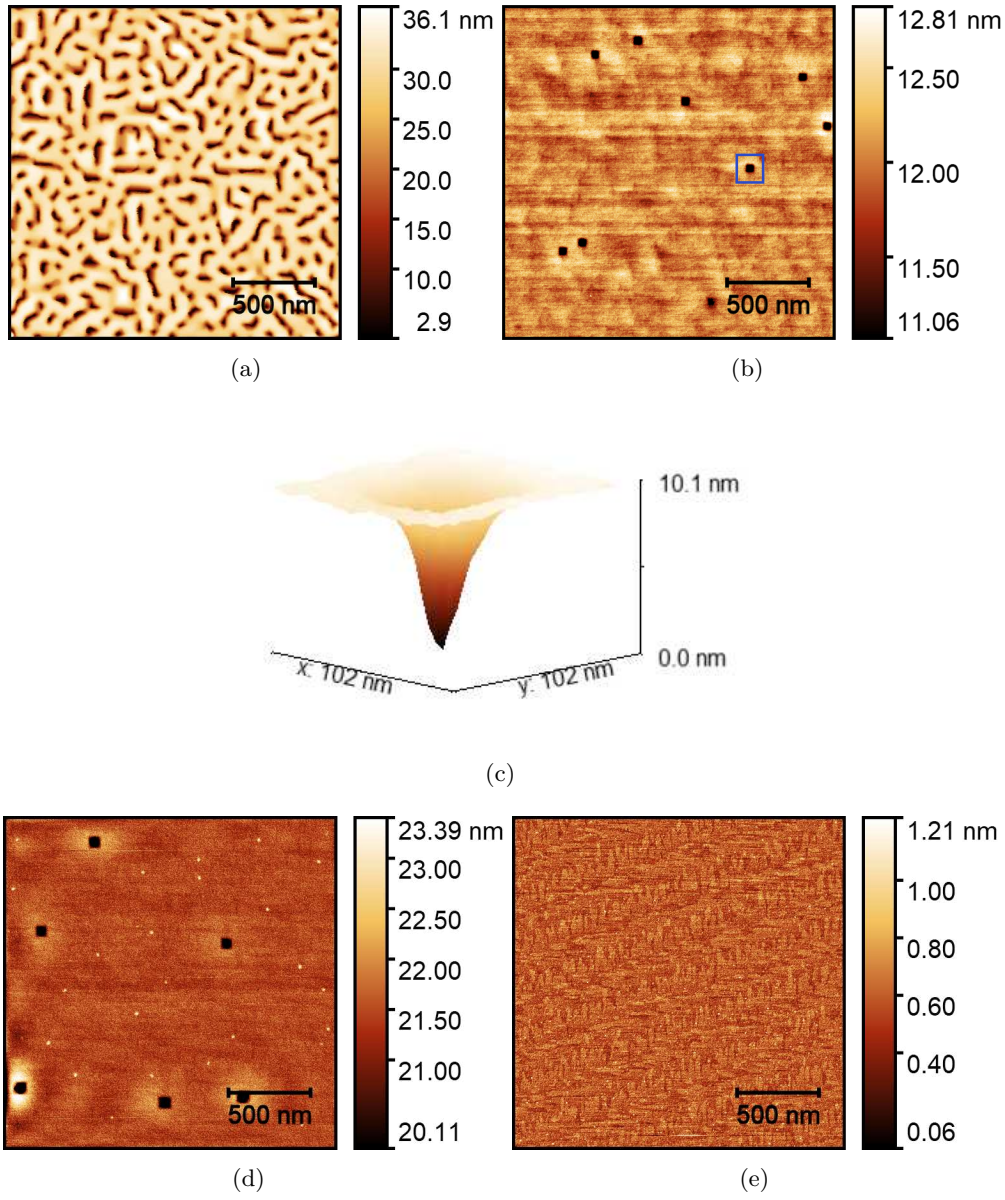
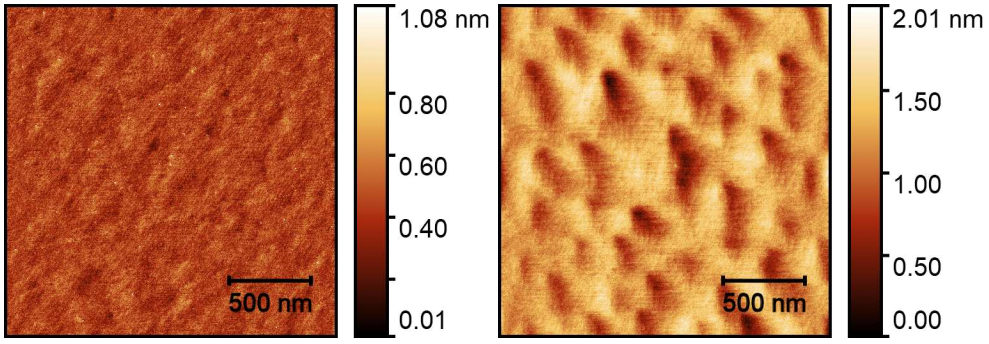


Figure 3.4: Surface topography measured by AFM of 50 nm Si homoepitaxial on Si substrates without (a) or with pre-annealing at 700 °C (b), 900 °C (d), and 1100 °C (e). The pit in the blue rectangle in (b) is zoomed in to exhibit in (c). All the substrates are cleaned by the wet chemical process before the annealing.

Reliable Surface Preparation by Atomic Hydrogen Irradiation

So far, it suggests that the wet chemical cleaning in our lab is not sufficient to obtain a clean Si substrate surface. Only by introducing one more pre-epitaxy annealing on the substrate at a temperature as high as 1100 °C, a ^{28}Si homoepitaxial layer can grow coalescently without pits. However, for quantum technologies, not only Si homoepitaxy on Si substrate is needed but also on SOI substrate or SiGe epitaxy on relaxed SiGe substrate. The pre-epitaxy annealing temperature should not be higher than 700 °C to avoid either the dewetting of the Si seed layer on SOI substrate [122] or the surface roughening of SiGe substrate due to the dislocation dynamics [123]. In this case, an in-situ pre-epitaxial process of hydrogen irradiation at 700 °C is introduced. The works by Shimomura et al. [124] and Assmuth et al. [125] show that hydrogen irradiation at around 700 °C is promising to remove the carbon and oxide irradiation of the Si substrate.

The surface topographies of the (0 0 1) Si substrate after wet chemical cleaning and hydrogen irradiation at 700 °C and the Si homoepitaxial layer grown on the same substrate after the same surface preparation are presented in Figure 3.5. It shows that the hydrogen irradiation doesn't damage to the Si substrate and also contributes to a coalescent ^{28}Si homoepitaxial layer without pits. This indicates that the combined ex-situ and in-situ surface cleaning brings an epitaxy ready, carbon and oxide contamination depleted surface.



(a) (b)

Figure 3.5: Surface topography measured by AFM of (0 0 1) Si substrate (a) after an ex-situ wet chemical cleaning and in-situ hydrogen irradiation at 700 °C and a 50 nm Si grown on this kind of substrate (b).

The surface preparation combining ex-situ wet chemical cleaning and in-situ atomic

hydrogen irradiation works also well on the SOI and $Si_{0.7}Ge_{0.3}$ substrates. The results are presented in section 4.3 and section 4.1. Low-defect epitaxial ^{28}Si layers or $^{28}Si_{0.7}Ge_{0.3}$ layers were grown by MBE coalescently without pits on the (0 0 1) SOI or $Si_{0.7}Ge_{0.3}$ substrates.

To prove the efficiency of the combined ex-situ wet chemical cleaning and in-situ atomic hydrogen irradiation cleaning technique on the relaxed $Si_{0.7}Ge_{0.3}$ substrates, two stacks as in Figure 2.3 (a) were grown by MBE on two $Si_{0.7}Ge_{0.3}$ substrates scribed from one wafer. The $Si_{0.7}Ge_{0.3}$ substrate of sample A was prepared only by wet chemical cleaning before the MBE growth, whereas the substrate of sample B was prepared by both wet chemical cleaning and in-situ annealing and atomic hydrogen irradiation at 700 °C inside the MBE chamber. From the interfacial impurity concentrations measured by dynamic SIMS in Figure 3.6, the oxygen concentration is reduced from 4000 ppm to 22 ppm and the carbon concentration is reduced from 280 ppm to 68 ppm through the annealing and atomic hydrogen irradiation at 700 °C. This convinces that the additional in-situ surface preparation leads to epitaxy ready $Si_{0.7}Ge_{0.3}$ substrates with low impurity concentrations.

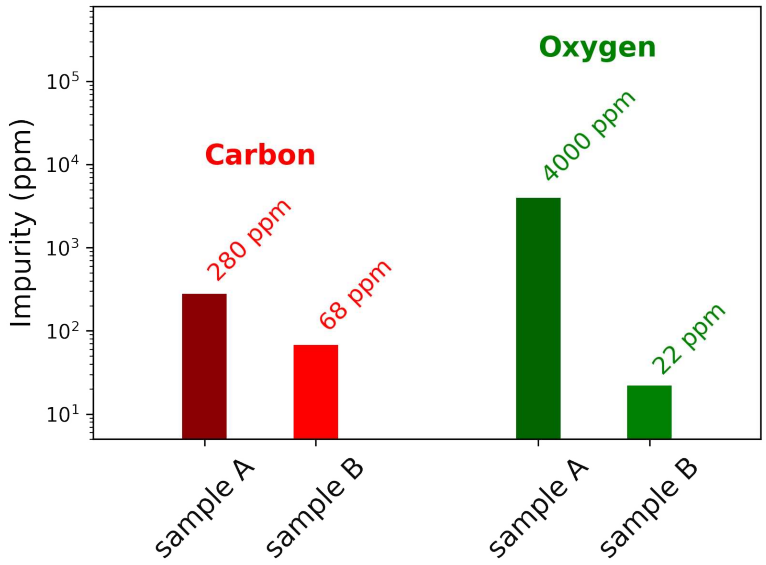


Figure 3.6: Interfacial carbon and oxygen concentrations at the interfaces of the CVD grown $Si_{0.7}Ge_{0.3}$ substrates and the MBE grown $^{28}Si_{0.7}Ge_{0.3}$ stacks, measured by dynamic SIMS. The $Si_{0.7}Ge_{0.3}$ substrate of sample A was prepared only by wet chemical cleaning, whereas the $Si_{0.7}Ge_{0.3}$ substrate of sample B was prepared by both wet chemical cleaning and in-situ atomic hydrogen irradiation.

Conclusion

Here, we investigate that the formation of the pits on the epitaxial layer surface is related to inefficient ex-situ wet chemical surface cleaning. Then, a reliable surface preparation combining the ex-situ wet chemical cleaning and in-situ atomic hydrogen irradiation is developed for Si substrate, which is proved to be equally efficient for CVD grown $Si_{0.7}Ge_{0.3}$ substrates and SOI substrate. SIMS measurements show that the in-situ surface preparation significantly reduces the carbon and oxygen concentrations at the interface between the CVD grown $Si_{0.7}Ge_{0.3}$ substrates and the MBE grown $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ heterostructures.

3.2 ^{28}Si Evaporation

After around 125 h MBE growth at an average growth rate of $0.02\,nm\,s^{-1}$, the ^{28}Si single crystal source (Figure 2.2 (b)) was depleted. The photos of a depleted ^{28}Si crystal source and its cross-section after cutting are presented in Figure 3.7 (a) and (b). Compared to Figure 2.2 (b) before the evaporation, there is a visible hole through the ^{28}Si cylinder. The ^{28}Si source is not bounded to the crucible after all the evaporation.

Though only a part of the ^{28}Si source was evaporated, the focus of evaporation on a small spot in the middle of the ^{28}Si source means to the avoid the Si diffusion between the crucible and the source. This is successful that the ^{28}Si source is not too hot to bound the source and the crucible. Besides, the rest of the ^{28}Si source can still be recycled as it is described in section 2.1.1.

A piece of the remaining ^{28}Si material is cut from dynamic SIMS measurements, in order to investigate the possible diffusion of the isotopic impurities ^{29}Si and ^{30}Si from the natural Si crucible into the ^{28}Si source. Before the measurement, the ^{28}Si piece is polished by the diamond foils as described in section 2.2.2 into 0.1 µm and etched by a mixture of HF:HNO_3:CH_3COOH as 1:3:2. The SIMS measurements were carried out at three locations on the ^{28}Si piece, that are listed in Figure 3.7 (b).

The SIMS measurement results of the remaining ^{28}Si source, as well as the results of MBE grown epitaxial ^{28}Si layer in ^{28}SOI from section 4.3 are listed in Figure 3.7 (c). The ^{29}Si in all the measurement points of the remaining ^{28}Si materials as well as the

MBE grown epitaxial layer are about 60 ppm. Respectively, the ^{30}Si levels are all below 5 ppm. There is no significant gradient of the isotopic impurity levels in the remaining ^{28}Si materials, which indicates the diffusion between the natural Si crucible and the ^{28}Si source is very limited. It is also expected because the source and the crucible are not bonded after the depletion of the ^{28}Si source.

The impurity levels from the ^{28}Si source materials and the ^{28}Si epitaxial layer are consistent. This means the isotopic impurities obtained from MBE growth don't have a significant contribution.

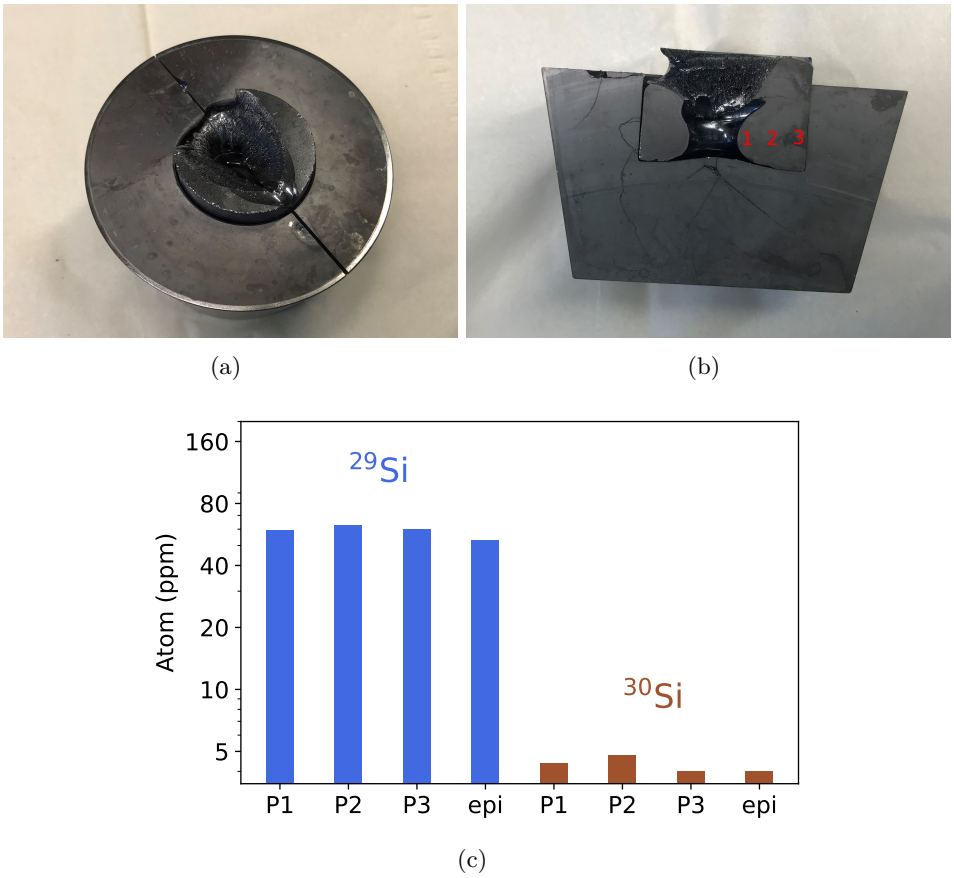


Figure 3.7: Depleted ^{28}Si source material on the natural Si crucible from (a) top view and (b) cross view after being cut. The SIMS results (c) of isotopic impurities ^{29}Si and ^{30}Si at the three measurement points of the remaining ^{28}Si materials, where P1-3 correspond to the points indicated in the cross-view (b). The SIMS results of the epitaxial ^{28}Si layer of ^{28}SOI in Figure 4.8 (a) are also listed here with the label "epi" for comparison.

Software comes from heaven when you have good hardware.

Ken Olsen

4 Epitaxial Growth of ^{28}Si, Ge Layers for Qubits

In this chapter, the results of ^{28}SiGe heterostructures for electron or hole spin qubits grown by hybrid isotope engineered MBE and CVD are presented, as well as the results of ^{28}SOI for optical quantum emitters grown by the same isotope engineered MBE.

4.1 ^{28}SiGe Heterostructures for Electron Spin Qubits

In this research, a hybrid MBE/CVD growth of a ^{28}Si quantum well layer for qubits is demonstrated. XRD, SIMS and electron microscopy were applied to investigate the epitaxial heterostructures in terms of strain, isotopic impurities and structural defects, respectively.

The cross-section HAADF-STEM image of the $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ heterostructure for electron spin qubits is shown in Figure 4.1 (a). This heterostructure was grown by the MBE/CVD hybrid technique, where the CVD grown $Si_{0.7}Ge_{0.3}$ substrate is prepared only by a wet chemical cleaning process described in section 2.1.1. The growth condition is described in section 2.1.1. There is a layer with increased Ge content at the interface between the MBE grown stack and the CVD grown $Si_{0.7}Ge_{0.3}$ substrate indicated by a brighter contrast, which likely results from the wet chemical cleaning. In the oxidation step of the wet-chemical cleaning, Si is oxidised quicker and therefore consumed quicker, leading to an increase of the Ge composition on the surface [130].

The SIMS measurement in Figure 4.1 (b) shows the concentration-depth profile of ^{29}Si. The concentration drops significantly from 40 000 ppm (4 %) to 200 ppm from the CVD grown $Si_{0.7}Ge_{0.3}$ substrate to the MBE grown $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ stack. The increase of the ^{29}Si concentration from the source material (40 ppm) to the epitaxial stack

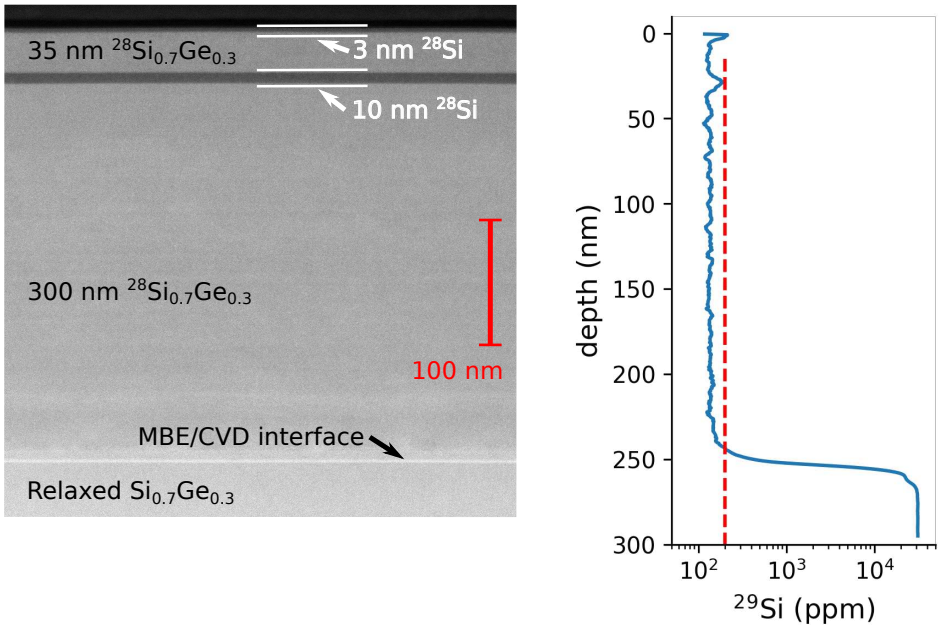
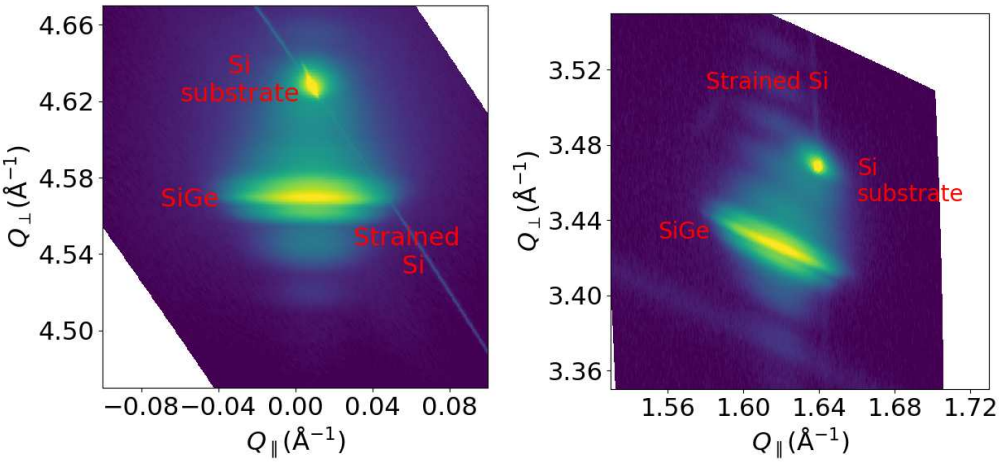


Figure 4.1: (a) HAADF-STEM cross-section view of the $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ heterostructure. (b) Depth profile of the isotopic impurity ^{29}Si inside $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ on the relaxed $Si_{0.7}Ge_{0.3}$ substrate measured by SIMS. The small peak of ^{29}Si concentration at the ^{28}Si quantum well layer can be originated for two reason: i. Si contents of the ^{28}Si quantum well layer and the $^{28}Si_{0.7}Ge_{0.3}$ layers are different; ii. the sputtering rates of SIMS at the ^{28}Si quantum well layer and the $^{28}Si_{0.7}Ge_{0.3}$ layers are different, whereas the SIMS data is analysed based on a Si reference sample.

is not clear, but results possibly from the Ge source since high purity Ge production involves natural Si [27].

The growth methods, parameters of embedded ^{28}Si quantum well layers in SiGe heterostructure for qubits, as well as the ^{29}Si concentrations in these ^{28}Si quantum well layers are compared in Table 4.1. The growth temperatures in MBE are way lower than the growth temperatures applied in CVD. Besides, the low ^{29}Si concentration in the ^{28}Si quantum well layer here is outstandingly low compared to the other works, which results in a quiet environment for the qubits.

The strain of the layers in the Si/SiGe heterostructure was analysed by XRD utilising the 0 0 4 and 1 1 3 reflections. The reciprocal space maps of these reflections are shown in Figure 4.2. The reflections of each layer are indicated in the images. The relaxed



(a) (b)

Figure 4.2: Reciprocal space maps of the 0 0 4 (a) and 1 1 3 (b) reflections measured by XRD on the $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ heterostructure. $\mathbf{Q}_\perp$ and $\mathbf{Q}_\parallel$ are the out-of-plane (along [0 0 1]) and in-plane (along [1 1 0]) X-ray scattering vectors. The reflections of the layer stacks were indicated within the images.

SiGe substrate has a larger lattice parameter than the Si substrate. Therefore, its reflections have smaller values of the scattering vector modulus $|\mathbf{Q}|$ than the reflections of the Si substrate. To verify if the SiGe substrate is fully relaxed, the in-plane and out-of-plane lattice parameters are calculated with the following equations and compared by assuming the in-plane lattice parameters $\mathbf{a}_1$ and $\mathbf{a}_2$ are equal because of the biaxial strain accommodated in the ^{28}Si quantum well layer:

$$\mathbf{Q}_{004}^2 = \left(0 \times \frac{2\pi}{\mathbf{a}_1}\right)^2 + \left(0 \times \frac{2\pi}{\mathbf{a}_2}\right)^2 + \left(4 \times \frac{2\pi}{\mathbf{a}_3}\right)^2, \tag{4.1}$$

$$\mathbf{Q}_{113}^2 = \left(1 \times \frac{2\pi}{\mathbf{a}_1}\right)^2 + \left(1 \times \frac{2\pi}{\mathbf{a}_2}\right)^2 + \left(3 \times \frac{2\pi}{\mathbf{a}_3}\right)^2. \tag{4.2}$$

The in-plane and out-of-plane lattice parameters are given from the calculation as 5.5002 Å and 5.5004 Å. Since the in-plane and out-of-plane lattice parameters are quasi equal to each other, it can be concluded that the SiGe is fully relaxed and it has a Ge composition of 33 % according to the dependence of SiGe lattice parameter $\mathbf{a}_1$ on the Ge composition x [131]:

$$|\mathbf{a}| = 5.431 + 0.20x + 0.027x^2. \tag{4.3}$$

Along the in-plane scattering vector $|\mathbf{Q}_\parallel|$, there is one broad peak along the out-of-plane scattering vector $|\mathbf{Q}_\perp|$ with oscillations in reflection 1 1 3 (Figure 4.2 (b)). This broad

peak results from the Si quantum well layer and the oscillation originates from the interference between its interfaces. Since the values of $|\mathbf{Q}_{\parallel}|$ of the reflections of the Si quantum well layer and the SiGe substrates are equal, it can be concluded that no relaxation is detectable by XRD in the Si quantum well layer.

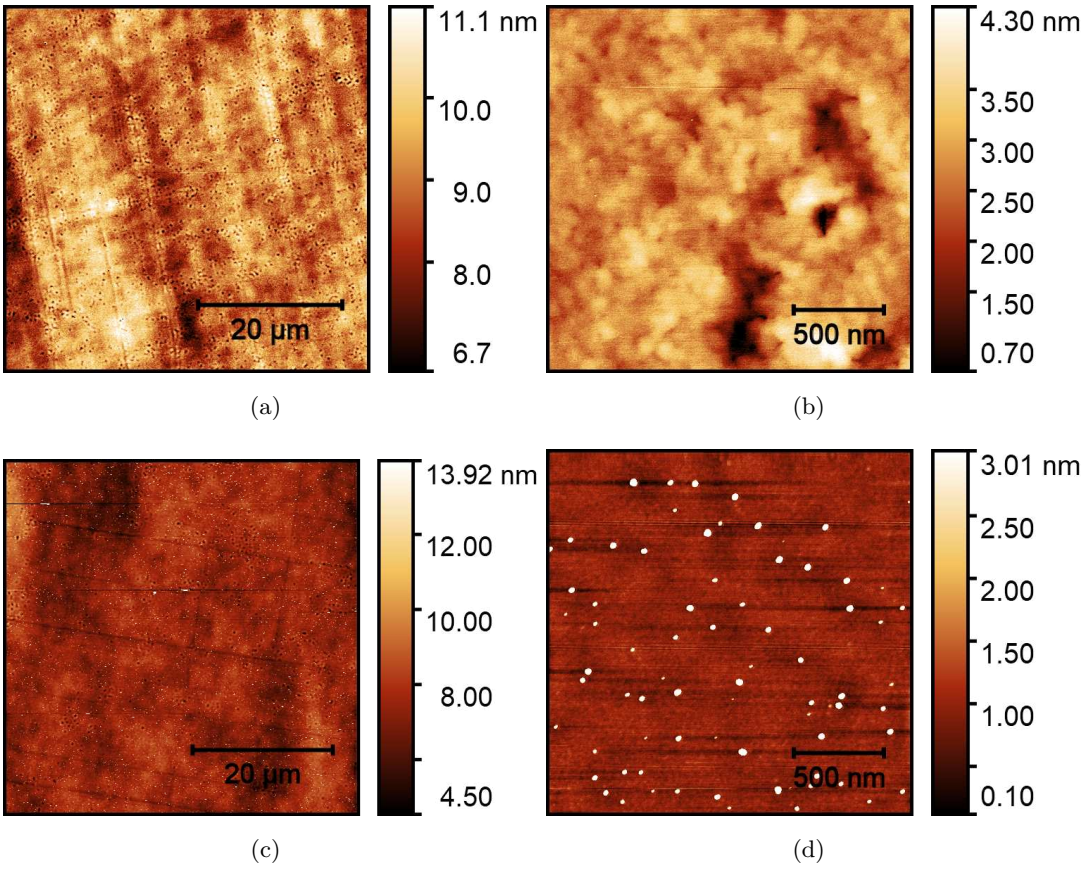


Figure 4.3: Surface topography of the $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ heterostructure investigated by AFM: (a) on an area of $50 \times 50\,\mu m^2$; (b) on an area of $2 \times 2\,\mu m^2$. Surface topography of the relaxed $Si_{0.7}Ge_{0.3}$ substrate also investigated by AFM for comparison: (c) on an area of $50 \times 50\,\mu m^2$; (d) on an area of $2 \times 2\,\mu m^2$. There are some particle like structures on the substrate since the substrate is not cleaned yet.

The surface topography of the $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ and its CVD grown $Si_{0.7}Ge_{0.3}$

substrate measured by AFM is shown in Figure 4.3. The $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ has a root mean square surface roughness of 1 nm over a $50 \times 50\,\mu m^2$ region in Figure 4.3 (a). The low interface roughness possibly results from the CMP process on the relaxed $Si_{0.7}Ge_{0.3}$ substrate after CVD growth. Some flat pits occur on the surface with a density around $7 \times 10^7\,cm^{-2}$. An AFM image with higher resolution is shown in Figure 4.3 (b). The pits here are similar to the pits observed by Egawa et al. [132] and the authors propose that these pits can be related to the threading dislocations from the relaxed $Si_{0.7}Ge_{0.3}$ substrate since the density of the pits and threading dislocations are similar. That is also the same case in our study, that the threading dislocation density investigated by Secco etch pits counting is around $8 \times 10^7\,cm^{-2}$, close to the pit density mentioned above $7 \times 10^7\,cm^{-2}$. Comparing the substrate presented in Figure 4.3 (c) and (d), the surface topography and also the density of the pits are the same in the $Si_{0.7}Ge_{0.3}$ substrate. This indicates that the surface topography, which are rich of pits, on this ^{28}SiGe heterostructures is probably originated from the CVD grown $Si_{0.7}Ge_{0.3}$ substrate and related to the threading dislocations. The AFM image of the $Si_{0.7}Ge_{0.3}$ substrate presents that there are some particle like structures on the substrates, which can be explained from the exposure to the air after the CVD growth.

In summary, a hybrid MBE/CVD technique is successfully developed to grow fully strained ^{28}Si quantum well layers in $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ heterostructures on (0 0 1) Si substrates. The exemplary $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ heterostructure has a ^{29}Si isotopic impurity content as low as 200 ppm.

Table 4.1: Comparison between the growth methods for embedded undoped ^{28}Si quantum well layers in similar SiGe heterostructures for electron spin qubits, as well as the thicknesses and the ^{29}Si concentrations of the Si quantum well (QW) layers from literature and this work.

	Group	Method	Growth temperature	Si QW layer thickness	^{29}Si concentration in Si QW layers	^{29}Si concentration in source/precursor	Reference
1	TU Delft	CVD	600...750 °C	8 nm	800 ppm		[128]
2	Princeton University	CVD	650 °C	5 nm		800 ppm	[129]
3	Regensburg University	MBE	500 °C for SiGe, 350 °C for Si QW	12 nm		60 ppm	[44]
4	Our group (SiGe heterostructures) studied in subsection 5.2.1	CVD	700 °C	10 nm		Natural Si applied	
5	Our group (SiGe heterostructures) presented in this chapter	Hybrid MBE/CVD	500 °C for SiGe, 350 °C for Si QW	10 nm	200 ppm	60 ppm	

4.2 ^{28}SiGe Heterostructures for Hole Spin Qubits

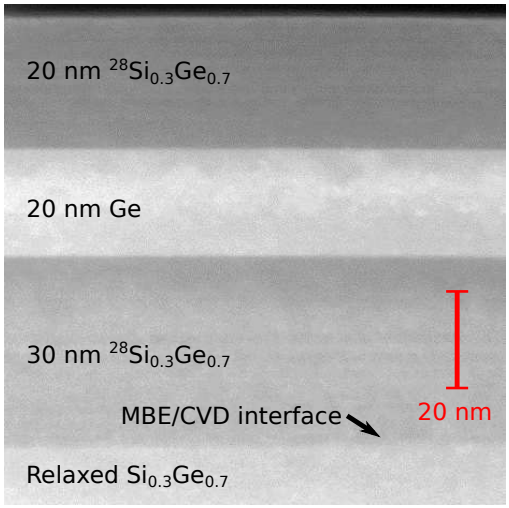


Figure 4.4: HAADF-STEM cross-section view of the $^{28}Si_{0.3}Ge_{0.7}$/Ge/$^{28}Si_{0.3}Ge_{0.7}$ heterostructure on a relaxed $Si_{0.3}Ge_{0.7}$ substrate.

In this research, the hybrid MBE/CVD technique was also applied in the growth of ^{28}SiGe/Ge/^{28}SiGe heterostructures for hole spin qubits.

The HAADF-STEM image of the ^{28}SiGe heterostructure for hole spin qubit grown on a relaxed $Si_{0.3}Ge_{0.7}$ substrate in this study is shown in Figure 4.4. No obvious defects are observed in the TEM image. Noticeably, there are some dark cloud like clusters inside the Ge quantum well layer, which indicates that some Si atoms are presumably located inside the Ge quantum well layer. Besides, the ^{28}SiGe substrates also have lower contrasts as the relaxed $Si_{0.3}Ge_{0.7}$ substrate. This suggests that the Ge content is slightly lower than 0.7 in the ^{28}SiGe substrate.

The strain of the layers in the ^{28}SiGe heterostructure shown in Figure 4.4 was analysed by XRD utilising the 0 0 4 and 2 2 4 reflections. The reciprocal space maps of these reflections are shown in Figure 4.5. The reflections of each layer are indicated in the images. Similar to the ^{28}SiGe heterostructure in section 4.1, the relaxed $Si_{0.3}Ge_{0.7}$ substrate with larger lattice parameters is located at the bottom left side by the Si substrate peak. By applying the same calculation as described in section 4.1, the values of the the in-plane and out-of-plane lattice parameters of the $Si_{0.3}Ge_{0.7}$ substrate are 5.5841 Å and 5.5718 Å respectively. This indicates that some $Si_{0.3}Ge_{0.7}$ layers have a lower content of Ge and are slightly compressive. Combining the observation in Figure 4.4, the ^{28}SiGe layers

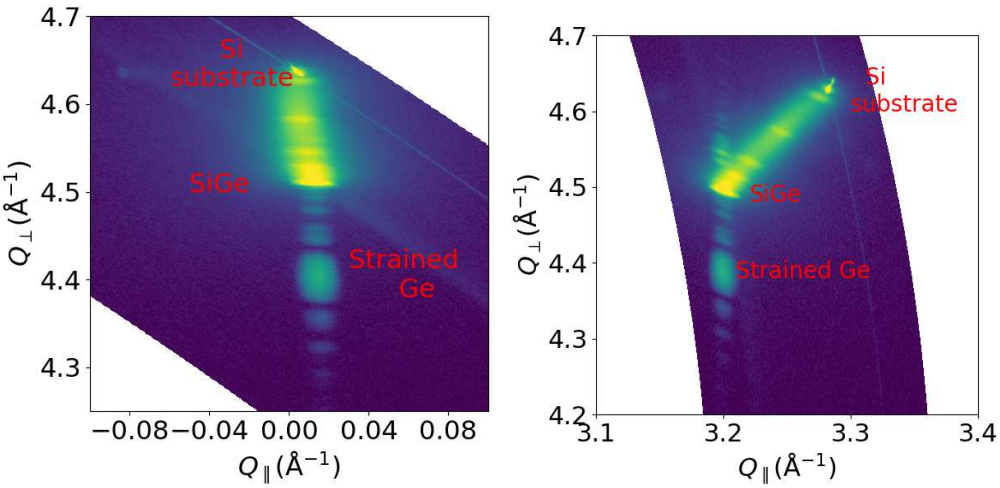


Figure 4.5: Reciprocal space maps of the 0 0 4 (a) and 2 2 4 (b) reflections measured by XRD on the $^{28}Si_{0.3}Ge_{0.7}$/Ge/$^{28}Si_{0.3}Ge_{0.7}$ heterostructure. $Q_\perp$ and $Q_\parallel$ are the out-of-plane (along [0 0 1]) and in-plane (along [1 1 0]) X-ray scattering vectors. The reflections of the layer stacks were indicated within the images.

presumably have a Ge content lower than 0.7. The in-plane lattice parameter of the ^{28}SiGe should be the same as the relaxed $Si_{0.3}Ge_{0.7}$. By applying the in-plane lattice parameter 5.5841 Å into Equation (4.3), the Ge content is calculated as 0.70, which agrees well with the aimed Ge content in the relaxed substrate. By applying the out-of-plane lattice parameter 5.5718 Å into Equation (4.3), the ^{28}SiGe is calculated to have a Ge content of 0.65. Along the in-plane scattering vector $\mathbf{Q}_\parallel$, there is one broad peak along the out-of-plane scattering vector $\mathbf{Q}_\perp$ with oscillations in reflection 2 2 4 (Figure 4.5 (b)). This broad peak results from the Ge quantum well layer and the oscillation originates from the interference between its interfaces. Different from the fatigue reflection of the Si quantum well layer in Figure 4.2 (b), the reflection of the Ge quantum well layer has higher contrast. An explanation for this can be that the Ge quantum well layer is twice thicker than the Si quantum well layer, with the thickness of 20 nm and 10 nm respectively. Since the Ge quantum well layer reflection has the same $\mathbf{Q}_\parallel$ as the SiGe, it can be concluded that no relaxation can be observed in Ge quantum well layer by XRD.

The surface topographies of the ^{28}SiGe/Ge/^{28}SiGe heterostructure and its CVD grown $Si_{0.3}Ge_{0.7}$ substrate are investigated in Figure 4.6. Long-period topographic cross hatch patterns occur on the ^{28}SiGe heterostructure surface. Respectively, there are barely cross

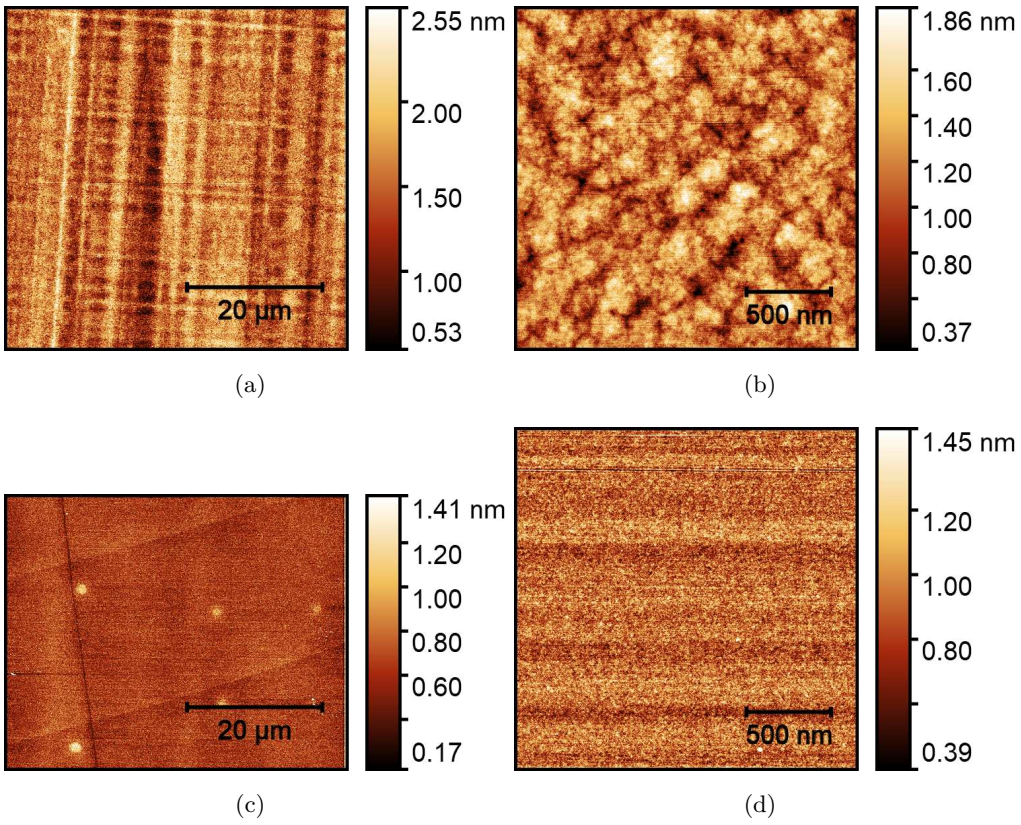


Figure 4.6: Surface topography of the ^{28}SiGe/Ge/^{28}SiGe heterostructure investigated by AFM: (a) on an area of $50 \times 50\,\mu m^2$; (b) on an area of $2 \times 2\,\mu m^2$. Surface topography of the relaxed $Si_{0.3}Ge_{0.7}$ substrate also investigated by AFM for comparison: (c) on an area of $40 \times 50\,\mu m^2$; (d) on an area of $2 \times 2\,\mu m^2$. There are some particle like structures on the substrate since the substrate is not cleaned yet.

hatch patterns on the $Si_{0.3}Ge_{0.7}$ substrate because of the chemical mechanical polishing. Microscopically, the ^{28}SiGe heterostructure has a root mean square roughness of 220 pm over a $2 \times 2\,\mu m^2$ region. It is rougher than the $Si_{0.3}Ge_{0.7}$ substrate with a root mean square roughness of 150 pm over a $2 \times 2\,\mu m^2$ region.

In conclusion, the MBE/CVD hybrid technique developed for $^{28}Si_{0.7}Ge_{0.3}$/^{28}Si/ $^{28}Si_{0.7}Ge_{0.3}$ heterostructures can also be applied in the growth of a fully strained Ge quantum well layers in ^{28}SiGe/Ge/^{28}SiGe for hole spin qubits on (0 0 1) Si substrates. However, the growth process still needs optimisation, for example, the controlling of the Ge content.

4.3 ^{28}Silicon-on-insulator for Infrared Quantum Emitters

The isotope engineered MBE was also engaged for the growth of ^{28}SOI: a 400 nm thin isotopically enriched ^{28}Si layers was grown on a 70 nm thin SOI seed. The resulting structure is intended to be applied for optical quantum emitters (section 1.4). The substrate applied, the pre-epitaxial cleaning and the growth process are introduced in section 2.1.1.

To use the obtained ^{28}SOI chips for the integration of optically interfaced quantum emitters with good coherence and narrow inhomogeneous linewidth, the following key requirements have to be fulfilled. First, the surface should exhibit a smooth topography to allow for the fabrication of low-loss waveguides [75]. Second, the ^{28}Si device layer of the chips should be of high crystalline quality, which includes a low concentration of other Si isotopes and impurity atoms. These properties of the ^{28}SOI are investigated in the following.

Surface Topography

The surface topography of the ^{28}SOI chip measured by AFM is shown in Figure 4.7. There are small ripples at the surface with a height of a few nanometers and a characteristic length scale of a few hundred nanometers. These ripples can originate from a slight miscut of the seed layer. This surface topography development was studied by Myslivcek et al. [133]: when the substrate miscut is small, Si adatoms tend to move to the lower terraces during epitaxial growth; in this case, the surface terrace is broadened and ripples form on the surface. When the epitaxial layer becomes thicker, the ripple spacing gets larger and zipper like structures form among the ripples. According to the additional measurements of X-ray reflection and XRD, the offcut of the substrate is $0.450 \pm 0.001°$.

The surface roughness of the grown layer is 3.4 Å, slightly larger than that of the seed SOI wafer, 2.1 Å. Still, it is comparable to the typical sidewall roughness achieved in nanophotonic waveguides fabricated by lithography and reactive ion etching [75], which means that it will not lead to a major increase of the backscattering loss in typical experiments. If a further reduction of the roughness is still required, one could grow the layer at an increased temperature [133], or introduce a post-epitaxial smoothing step [134].

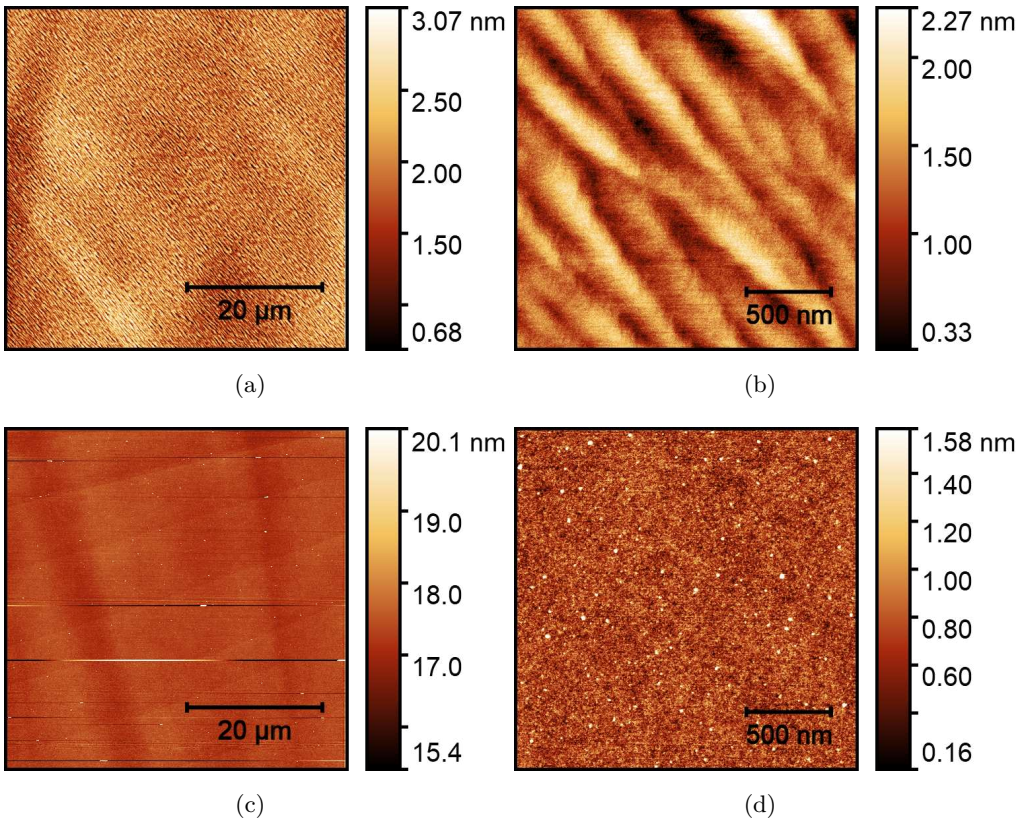
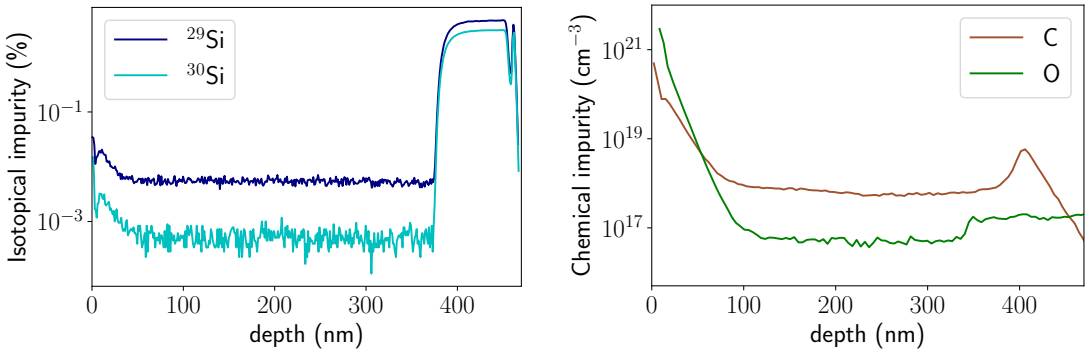


Figure 4.7: Surface topography of the grown ^{28}SOI chips, characterised by AFM: (a) on a large scale of $50 \times 50\,\mu m^2$, an root mean square roughness of 3.4 Å is obtained. (b) on a smaller scale of $2 \times 2\,\mu m^2$. Besides, the surface topography of the SOI seed layer is shown in (c) and (b) on different scales.

Isotopic and Chemical Purity

The isotopic and chemical purities of the epitaxial layer are measured by a dynamic SIMS described in subsection 2.2.5. As shown in Figure 4.8 (a), the Si seed layer at a depth of more than 380 nm contains 4.7 % ^{29}Si and 3.1 % ^{30}Si, which matches the isotopic content in natural Si. In the epitaxial layer, the concentration is reduced to 0.006 % (60 ppm) ^{29}Si and 0.0004 % (4 ppm) ^{30}Si. Thus, the isotopically enriched ^{28}Si source material will allow for a reduction of the nuclear spin density in nanophotonic waveguides by about three orders of magnitude, offering a great promise for the control of single emitters with ultra low spectral diffusion in suited resonators [135].

The chemical purity of the grown layer was also investigated by SIMS. Typical impu-



(a) (b)

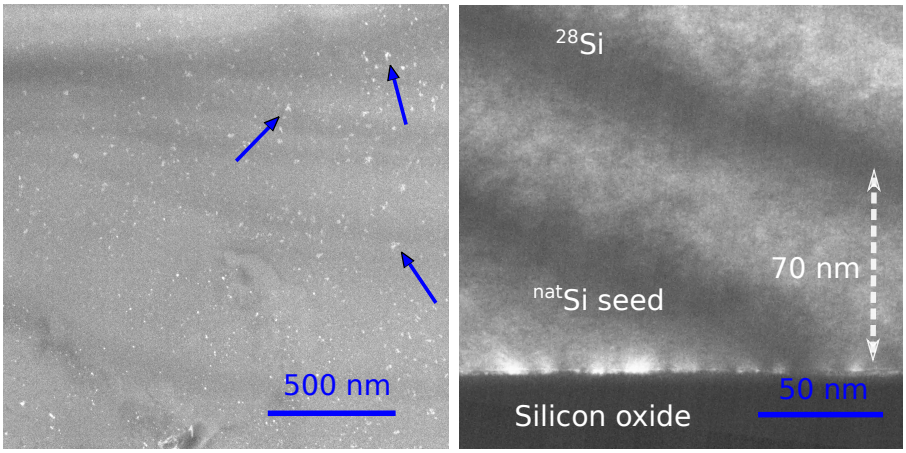
Figure 4.8: Purity of the ^{28}SOI chips as a function of depth, measured by SIMS. (a) Isotopic purity. The end of the epitaxial layer can be seen as a steep increase of the fraction of ^{29}Si and ^{30}Si isotopes. (b) Chemical purity. The main expected impurities, carbon and oxygen, have a low concentration in the epitaxial layer of around $5 \times 10^{17}\,\mathrm{cm}^{-3}$ and $5 \times 10^{16}\,\mathrm{cm}^{-3}$. The increase of the carbon and oxygen concentration close to the surface area can be due to the re-deposition during the SIMS measurements. The carbon and oxygen level increase in the seed layer as deep as around 370 nm

rities present in MBE grown materials are carbon and oxygen, which have a residual concentration of around $5 \times 10^{17}\,\mathrm{cm}^{-3}$ and $5 \times 10^{16}\,\mathrm{cm}^{-3}$ (Figure 4.8 (b)). The SIMS measurements were performed at the centre of the layer. These are comparable to the values in earlier MBE grown Si layers [136]. At the interface to the seed layer, there is a small peak ($\sim 5 \times 10^{18}\,\mathrm{cm}^{-3}$) of carbon, but no significant increase of the oxygen concentration. This means that the pre-epitaxial wet chemical cleaning and hydrogen irradiation was effective in completely removing the oxide layer. The interfacial carbon level is also not high. This indicates that the surface preparation provies a clean growth interface without significant contamination.

Structural Perfection Characterisation

Next, the crystalline quality of the grown layer is investigated by TEM. A dark field plan view TEM is applied to image the ^{28}SOI and the result is shown in Figure 4.9 (a). In the investigated area ($\sim 2 \times 2\ \mu\mathrm{m}^2$), no defect such as dislocation is observed. At the marked locations, there are some local strain inhomogeneities, which can be attributed to the interface of the Si oxide and Si seed layer. Similar strain inhomogeneities are also observed in the dark-field cross-view TEM in Figure 4.9 (b). They are only found

in the region around 20 nm above the Si oxide. Above, the Si layer shows good strain homogeneity. There is no observable interface of the epitaxial ^{28}Si layer and Si seed in Figure 4.9 (b), testifying high-quality crystalline growth.



(a) (b)

Figure 4.9: Dark-field TEM images of ^{28}SOI in plan-view (a) and cross-view (b). The homogeneity of the grown layer testifies high-quality crystalline growth. Only at the interface between the Si seed layer and the buried oxide, strain inhomogeneities are observed as black and white contrasts. These strain inhomogeneities can be the reason that the contrasts in the plan view TEM image, which are marked by blue arrows in (a).

Conclusion

In summary, ^{28}SOI is successfully grown by isotope engineered MBE in this work. The performed analysis lets us expect a high crystalline perfection of the top layer, such that no significant optical loss is expected from lattice defects [137] in nanophotonic waveguides fabricated from the grown layer. In the future, selective doping or ion implantation can be used to generate optically active emitters [71, 73]. The emitters built on this epitaxial layer are supposed to have low optical loss thanks to the surface smoothness. Similar to previous works in bulk crystals, the inhomogeneous linewidth of these emitters will probably be reduced compared to crystals with mixed isotopes [35], and the spin coherence of the spin centres will be increased by the absence of ^{29}Si nuclear spins [138]. With respect to the ^{29}Si concentration, the results in section 3.2 indicate that the isotopic purity of the source material could be completely transferred to the grown top layer. This

opens exciting perspectives for the fabrication of the optical quantum emitters based on this kind of ^{28}SOI.

The important thing in science is not so much to obtain new facts as to discover new ways of thinking about them.

William Lawrence Bragg

5 Misfit Dislocations in SiGe Heterostructures for Qubits

The spin states of electrons in Si quantum well layers or holes in Ge quantum well layers in SiGe heterostructures are outstanding candidates for large-scale integration of fault-tolerant qubits for solid state-based quantum computing (chapter 1). Hereby, the strained quantum well layers are fabricated by pseudomorphic growth of Si and Ge on SiGe. The respective band valley (conduction band in Si quantum well or valence band in Ge quantum well) degeneracy is partially lifted through the biaxial strain applied as a prerequisite for eventual qubit operation. The local variations of this strain (for example, by misfit dislocations illustrated in Figure 5.1 (b)) cause local variations of the valley splitting [139, 140] and also bring charge noises, which were shown to influence the quantum coherence of qubit states negatively [141]. Hence, it is of superior importance for the quality of qubits to achieve sufficient and homogeneous strain in the quantum well layers. This can only be achieved by a deep understanding and ultimately the prevention of the strain relaxation accompanied by the misfit dislocation formation, propagation and interactions in such quantum well layers.

5.1 General Concepts

The misfit dislocations in SiGe heterostructures have been well studied in the last century. Here, the formation, the characteristics, the propagation kinetics and the interaction of misfit dislocations are briefly introduced in the following parts.

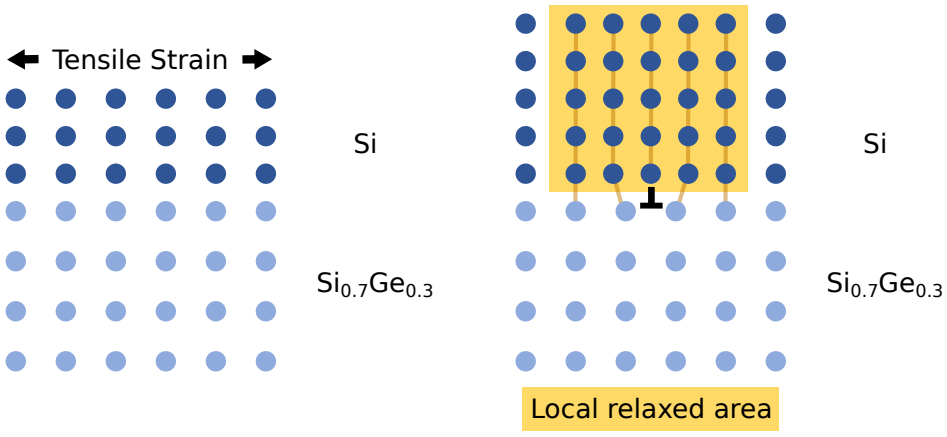


Figure 5.1: Schematic illustrations of (a) a tensile strained Si layer on relaxed $Si_{0.7}Ge_{0.3}$ substrate and (b) the plastic strain relaxation via misfit dislocation formation at the interface of the strained Si layer when the Si layer is thicker.

5.1.1 Misfit Dislocation Formation: Matthews-Blakeslee Criterion

A thin layer with misfit pseudomorphically grown on a thick substrate is elastically strained. The example can be as a Si layer on a relaxed SiGe substrate in Figure 5.1 (a). The in-plane lattice parameter of the elastically strained layer is equal to that of the substrate. The strain can be tensile when the lattice constant of the layer is smaller than that of the substrate, or compressive when the lattice constant of the layer is larger. The strained geometry stores elastic strain energy because the interatomic bonds in the epitaxy layer are stretched or compressed. In the case of the covalent bonds in Si and Ge, the interatomic bonds even rotated. When the layer is thicker than a critical thickness h_c, misfit dislocation forms at the interface of the layer and the substrate to reduce this elastic strain energy due to the energetic favourite (Figure 5.1 (b)).

The classical concept of misfit dislocation formation by threading dislocation gliding has been presented by Matthews and Blakeslee [142]. The formation mechanism is illustrated in the inset in Figure 5.2. Here, a pre-existing threading dislocation is bent at the interface between a strained layer and the substrate once the Peach-Köhler force $\mathbf{F_E}$ acts on the threading segment in the layer. The line tension of the threading dislocation acts as the resistive force $\mathbf{F_L}$ against $\mathbf{F_E}$. The force $\mathbf{F_E}$ scales linearly with the dislocation length, which scales with the strained layer thickness. When the thickness of the strained

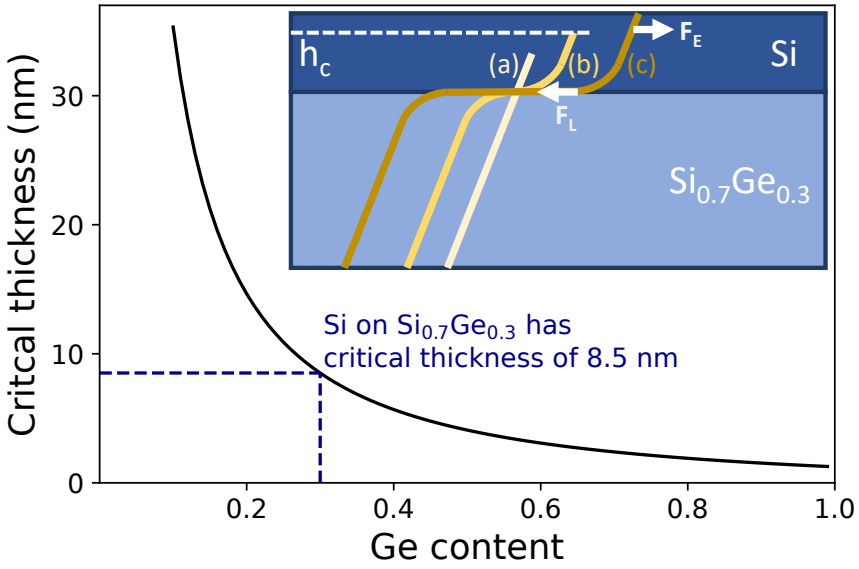


Figure 5.2: Critical thickness of an epitaxial Si layer as a function of Ge content x in relaxed $Si_{1-x}Ge_x$ substrate. The inset illustrates the propagation of a grown-in threading dislocation forming a misfit dislocation: (a) if no misfit is present, the threading dislocation tends to be straight; (b) when the misfit strain is present, the threading dislocation tends to bend; (c) once the epitaxial layer exceeds a certain critical thickness, the force from the misfit strain exerted on the threading dislocation $\mathbf{F_E}$ is larger than the force resulting from the extension of the dislocation $\mathbf{F_L}$. Hence, the threading dislocation glides leaving behind a misfit dislocation segment in the interface.

layer, that is Si layer here, is beyond a critical value h_c, $\mathbf{F_L}$ cannot compensate $\mathbf{F_E}$ anymore and a misfit dislocation segment forms.

The critical thickness can be calculated by the balance between the force exerted on threading dislocation by misfit strain $\mathbf{F_E}$ and the line tension of the misfit dislocation generated at the interface $\mathbf{F_L}$. To calculate the critical thickness h_c for a Si quantum well layer on a $Si_{0.7}Ge_{0.3}$ relaxed buffer, the adaption of the criterion in SiGe materials presented by People and Bean based on the Matthews-Blakeslee theory [143] is applied:

$$h_c \approx \frac{|\mathbf{b}|}{4\pi f(1+\nu)}(\ln \frac{h_c}{|\mathbf{b}|} + 1), \tag{5.1}$$

where $|\mathbf{b}| = 0.384\,\text{nm}$ is the Burgers vector, $\nu = 0.28$ is the Poisson ratio and f is the misfit in Si. This equation is adjusted for epitaxial layers on thick substrates, which corresponds to our case of a Si thin film on the thick SiGe virtual substrates.

The critical thickness of Si depends on the mismatch strain and hence on the Ge content in the substrate. This dependency is plotted for a fully relaxed SiGe buffer in Figure 5.2. The strained Si on $Si_{0.7}Ge_{0.3}$ has a critical thickness of 8.5 nm, where $Si_{0.7}Ge_{0.3}$ is the commonly used relaxed substrate for Si electron spin qubits [32, 144].

One should mention that strained $Si_{1-x}Ge_x$ layers on dislocation free Si substrates can be grown coherently and fully strained far beyond this thickness. This is due to the absence of threading dislocations, which means that dislocations that can relax the strain have to nucleate first. This nucleation of dislocations has a higher thermal activation barrier than threading dislocation gliding [143, 145]. For this reason, the nucleation of the dislocation happens rarely outside of a high temperature or high strain condition. Comparably, the misfit dislocation formation by threading dislocation gliding can occur in a moderate condition.

The results in subsection 5.2.1 show that, where sufficient threading dislocations are present, the Matthews Blaskeslee criterion is met and the relaxation of the quantum well layer depends on the threading dislocation density in the buffer. The results also show that threading dislocations are pinned when intersecting other perpendicular misfit dislocations in this case, because the thickness of the quantum well layer is not thick enough that the dislocations cannot overcome the glide barrier, which results in a particular arrangement of the misfit dislocations.

5.1.2 Misfit Dislcoation Characteristics

To further understand the misfit dislocations in the SiGe heterostructures containing a tensile strained Si quantum well layer or a compressively strained Ge quantum well layer, we need to have a closer look at the typical misfit dislocation characteristics in these layers.

Let's first start at the general dislocation characteristics in Si and Ge. Si and Ge have a diamond-type lattice structure. That means, it consists of two face centred cell (FCC) structures with a shift of $\frac{1}{4}[1\,1\,1]$ relative to each other. The dislocation gliding normally follows the glide system of a crystal. That means both the dislocation line and its Burgers vector locate in the glide plane. The Burgers vector follows the glide directions. The glide planes, usually the planes with the highest atomic packing factors, are $\{1\,1\,1\}$ in the diamond-type crystal. The glide direction usually corresponds to the shortest lattice translation vectors in the glide plane. This means that the direction contains the most atoms per length, is $\langle 1\,1\,0\rangle$ here.

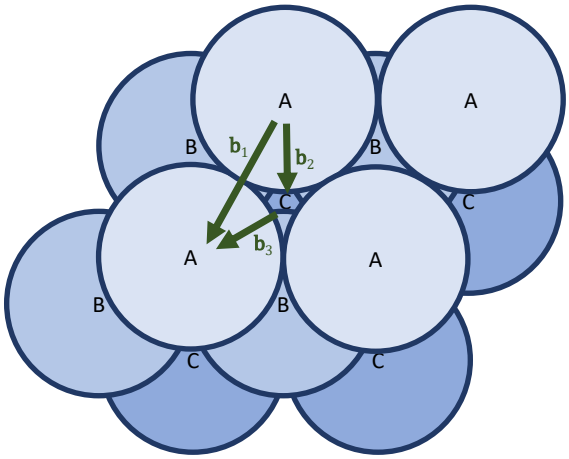


Figure 5.3: Glide on a $\{1\,1\,1\}$ plane of a diamond type crystal. A perfect dislocation with Burgers vector $\mathbf{b}_1 = \frac{a}{2}\langle 1\,1\,0\rangle$. The extra half plane consists two $\{1\,1\,0\}$ planes. A perfect dislocation can split into two Shockley partial dislocation $\mathbf{b}_{2,\,3} = \frac{a}{6}\langle 2\,1\,1\rangle$.

The glide in a diamond-type crystal is illustrated in Figure 5.3. The $\{1\,1\,1\}$ planes of a diamond-type crystal have a three-fold stacking sequence ABCABC and further. A dislocation can glide from A site to A site with a Burgers vector $\mathbf{b}_1 = \frac{a}{2}\langle 1\,1\,0\rangle$ in

Figure 5.3, which is called perfect dislocation. It can also split into two partial dislocations corresponding to Burgers vectors $\mathbf{b}_{2,3}$ as $\frac{a}{6}\langle 2\,1\,1\rangle$. In order to discuss the energy favourite of the dislocation configuration, the energy E of the stress field originated by dislocations [146] is introduced here, which consists of two parts, namely the energy in the core and the elastic energy outside the core,

$$\begin{aligned} E &= E_{\text{core}} + E_{\text{elastic}} \\ &= \beta G\mathbf{b}^2 + \alpha G\mathbf{b}^2. \end{aligned} \tag{5.2}$$

Here, α and β depend on the dislocation type. α is approximately $0.5 - 1.0$ and normally $\beta << \alpha$, G is the shear modulus and $\mathbf{b}$ is the Burgers vector. Here, it is obvious that E is proportional to $\mathbf{b}^2$. In the case of the perfect dislocation splitting in Figure 5.3, the elastic energy sum of two partial dislocations from splitting is smaller than the elastic energy of a perfect dislocation, because

$$E_{b_1} \propto \mathbf{b}_1^2 = \frac{a^2}{2}, \tag{5.3}$$

$$E_{b_{2,3}} \propto \mathbf{b}_2^2 + \mathbf{b}_3^2 = \frac{a^2}{3}. \tag{5.4}$$

Therefore, the dislocation splitting is energetically favourable in diamond-type crystals.

During the misfit dislocation splitting in diamond-type crystals, not only energy favourite but also strain relaxation efficiency needs to be taken into consideration.

As it is illustrated in Figure 5.1, the misfit dislocation forms at the interface between two mismatched layers to relax the strain. In the diamond-type crystal, the misfit dislocation lines are along $\langle 1\,1\,0\rangle$ in-plane direction at the interface. According to the discussion above, the Burgers vectors $\mathbf{b}$ are $\frac{a}{2}\langle 1\,1\,0\rangle$. Therefore, the dislocation types can be edge (also called 90° because the Burgers vector $\mathbf{b}$ is 90° relative to the dislocation line direction $\mathbf{l}$), screw and also mixed of edge and screw (also called 60° because the Burgers vector $\mathbf{b}$ is 60° relative to the dislocation line direction $\mathbf{l}$). Since the screw dislocation does not help the strain relaxation and the 90° dislocations have the highest core energy, the 60° types make up commonly the majority of misfit dislocations [147, 148]. The 90° dislocations are present exceptionally in the layer with high strain [149, 150, 151].

The 60° dislocations can also be split into two partials. We take the dislocation along $[\bar{1}\,1\,0]$ with a Burgers vector $\mathbf{b}_1 = \frac{a}{2}[\bar{1}\,0\,1]$ upon the tensile strain as an example (Figure 5.4). Here, the extra half planes are in the epitaxial layer side for the strain releasing. The 60° can split into a 90° and a 30° partial dislocation, indicated with Burgers vectors $\mathbf{b}_2$ and

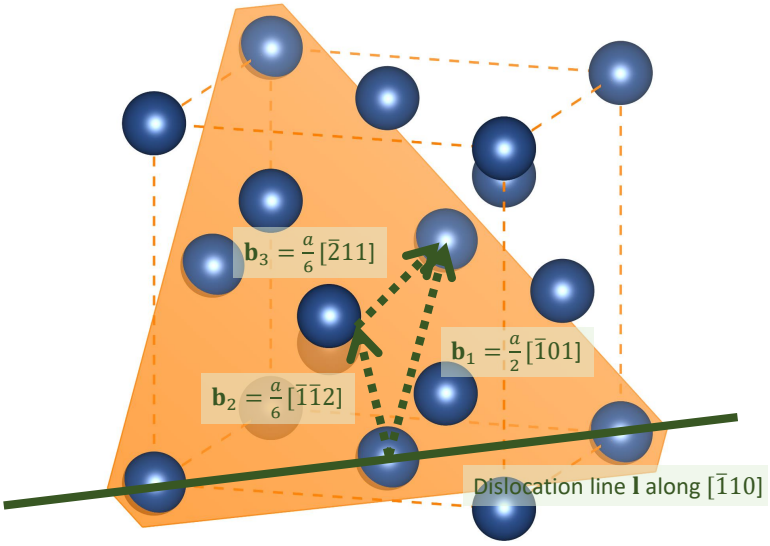


Figure 5.4: A 60° misfit dislocation ($\mathbf{b}_1 = \frac{a}{2}[\bar{1}\,0\,1]$), illustrated as the solid green line, splitting into two partials ($\mathbf{b}_{2,3}$) drawm in a unit cell of a diamond type crystal. The unit cell is drawn in software Vesta with the data from [152].

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$\mathbf{b}_3$,

$$\frac{a}{2}[\bar{1}\,0\,1] \rightarrow \frac{a}{6}[\bar{1}\,\bar{1}\,2] + \frac{a}{6}[\bar{2}\,1\,1]. \tag{5.5}$$

The 90° partial nucleates at first and the 30° partial follows. The 90° partial releases more strain than the 30° partial, so the dislocation splitting is also energetically favourite. Therefore, the 60° dislocations in the tensile strained layer tend to split.

It is another case in a compressive layer where the extra half planes are in the substrate side. In this case, all the directions of the Burgers vectors in Figure 5.4 are reversed. The 30° partial nucleates first and the 90° partial next. The first 30° partial cannot release enough strain so that the 90° partial nucleates immediately. This means the 60° dislocations in a compressively strained layer tend to not split in order to release the strain promptly.

This causes that the misfit dislocations in the compressive layers can easily cross slip so that the dislocation line direction $\mathbf{l}$ changes between $[1\,1\,0]$ and $[1\,\bar{1}\,0]$. Respectively, the misfit dislocations in the tensile strained layer tend to be straight.

5.1.3 Misfit Dislocation Kinetics: Dodson-Tsao Mechanism

The strain relaxation due to misfit dislocation propagation by threading dislocation gliding is a thermally activated process [153]. The velocity of the propagation v can be written as a simple Arrhenius-type law

$$v = v_0(\sigma) \exp\left(-\frac{E_a(\sigma)}{kT}\right). \tag{5.6}$$

The pre-exponential factor $v_0(\sigma)$ and the activation energy $E_a(\sigma)$ depend on the material and the stress applied σ. Besides, k is the Boltzmann constant and T is the temperature applied. The stress-dependence of $E_a(\sigma)$ can be expressed as

$$E_a(\sigma) = E_0\left(1 - \frac{|\sigma|}{\tau_0}\right). \tag{5.7}$$

Here, E_0 is the propagation activation energy at zero stress. τ_0 is the so-called zero-temperature flow stress, which is roughly 5-10 % of the shear modulus in semiconductors [154] while it is around 1 % in metals. The stress here is related to the misfit strain ϵ in the layer by:

$$\sigma = 2\epsilon\mu\frac{1+\nu}{1-\nu}, \tag{5.8}$$

where μ is the shear modulus, and ν is the Poisson's ratio.

Hence, according to Equation (5.6) and Equation (5.7), the propagation velocity increases with the temperature and the stress.

This stress-dependent misfit dislocation propagation kinetics stated by Dodson and Tsao was experimentally verified by the relaxation of SiGe films grown by MBE on Si substrate [155, 156, 157].

In subsection 5.2.2, the misfit dislocation propagation in the strained Si layer on a relaxed $Si_{0.7}Ge_{0.3}$ substrate during post-growth annealing at different temperatures is investigated by ECCI. By plotting the dislocation propagation velocities over the inverse temperature, an Arrhenius-type plot is obtained, from which the activation barriers of the propagation are extracted. The same experiment was performed at the strained Ge layer grown by MBE at 270 °C on the relaxed $Si_{0.3}Ge_{0.7}$ buffer.

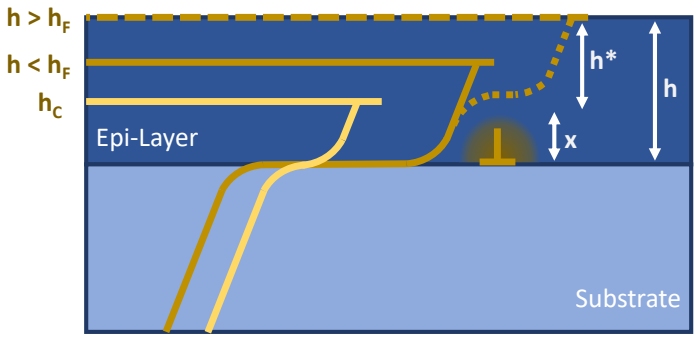


Figure 5.5: Schematic diagram showing the blocking mechanism on the misfit dislocation propagation from a perpendicular misfit dislocation. When the epitaxial layer with misfit exceeds the critical thickness h_c defined by the Matthews-Blakeslee criterion in subsection 5.1.1, misfit dislocation forms and propagates. This propagation can be blocked by a strain field induced by a pre-existed perpendicular misfit dislocation. The blocking effect of the perpendicular misfit dislocation getting weaker at the location far from this misfit dislocation. If the layer is above h_F defined by the Freund criterion, the threading dislocation can overcome the barrier from the perpendicular misfit dislocation and glide to propagate the misfit dislocation further (dashed line), that is called unblocking.

5.1.4 Misfit Dislocation Interaction: Freund Criterion

During the misfit dislocation propagation in the strained layer, it can interact with other misfit dislocations at the interface. This interaction can block the propagation because of the strain field associated with the other misfit dislocation (Figure 5.5). When the layer is grown thicker, the force from the misfit strain on the misfit dislocation propagation increases and can overcome the blocking effect from the other misfit dislocation. That leads to the unblocking of the propagation (illustrated with the dashed line in Figure 5.5).

Freund proposes a simple model [158] to calculate the criterion for the bypass of the misfit dislocation propagation above the other misfit dislocations as follows. The strain originated from the other misfit dislocation to compensate the misfit strain ϵ at the distance x from the heterointerface is

$$|\epsilon_{\mathbf{int}}| = \frac{1}{2\pi}\frac{|\mathbf{b}|}{x}, \tag{5.9}$$

where b is the Burgers vector of the dislocation. Therefore, the effective strain $\epsilon_{\mathbf{eff}}$ at the

distance x from the heterointerface is

$$\epsilon_{\mathbf{eff}} = \epsilon - \epsilon_{\mathbf{int}}, \tag{5.10}$$

where ϵ is the misfit strain. The remaining distance to the surface is denoted by

$$h_* = h - x. \tag{5.11}$$

The propagation is unblocked, when the effective strain fits the rudimentary critical condition for the threading dislocation above x to glide. The simplified critical condition from Freund can be written as

$$|\epsilon_{\mathbf{eff}}| = \frac{|\mathbf{b}|}{4\pi h_*} \ln \frac{8h_*}{|\mathbf{b}|}, \tag{5.12}$$

where the dislocation cutoff radius as $\frac{|\mathbf{b}|}{4}$ is considered and poison ratio $\nu = 0.3$ in Si, Ge related material system is applied. Combining Equation (5.9), Equation (5.10) and Equation (5.12),

(5.13)

The condition to get the minimal ϵ respective to h_* is given by

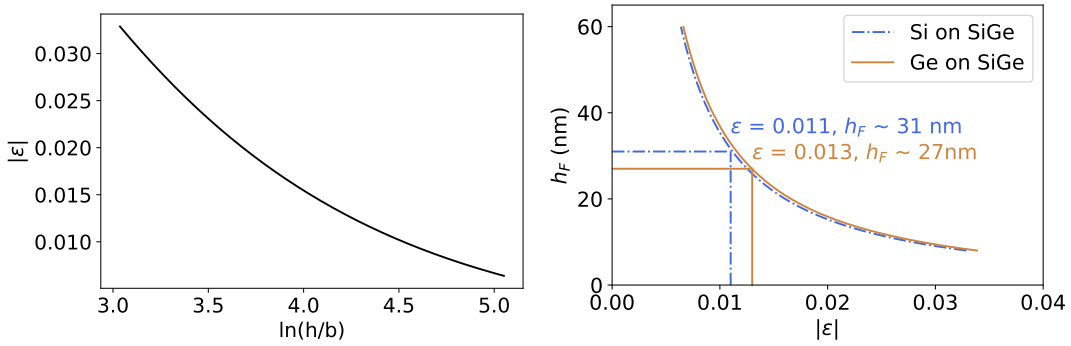
$$\frac{d|\epsilon|}{dh_*} = 0. \tag{5.14}$$

By solving for h_* and substituting h_* into Equation (5.13), the minimal misfit strain ϵ can be obtained. In Figure 5.6, ϵ is plotted regarding to the layer thickness for the unblocking mechanism with the strained Si and Ge layers. The critical thicknesses of dislocation blocking in the 1.1 % strained Si layer and the 1.3 % strained Ge layer are addressed with dashed lines because they are the samples investigated in this work.

Noticeably, the blocking criterion depends also on the Burgers vectors of the misfit dislocations. Freund states that the critical thickness of the blocking in this simple model is expected slightly higher with a ratio of 30 %.

The blocking and unblocking effects are experimentally observed already in SiGe films on Si [159, 145].

In subsection 5.2.2, it shows that the misfit dislocation propagation blocking by other misfit dislocations occurs in the tensile strained 10 nm Si layers on relaxed $Si_{0.7}Ge_{0.3}$ substrates but not in the 20 nm Ge layers on relaxed $Si_{0.3}Ge_{0.7}$ substrates, which has a good agreement with the criterion proposed by Freund [158].



(a) (b)

Figure 5.6: (a) The minimal misfit strain $|\epsilon|$ forcing the misfit dislocation propagation to bypass the barrier of the perpendicular misfit dislocation in the epitaxial layer with certain thickness $h/|\mathbf{b}|$, calculated from Equation (5.13). (b) The critical thickness h_F converted from $h/|\mathbf{b}|$ for the unblocking of the propagation regards to certain strain ϵ in the system of Si or Ge layer on relaxed SiGe substrates.

5.1.5 Strain Relaxation

The strain relaxation ϵ_{relax} by misfit dislocations in epitaxial layers can be described [142] as

$$|\epsilon_{\text{relax}}| = \frac{|\mathbf{b}|}{\gamma d_{\text{MD}}}, \tag{5.15}$$

where $\mathbf{b}$ is the Burgers vector of the dislocations and d_{MD} is the misfit dislocation spacing. γ depends on the relaxation efficiency of the misfit dislocations, that is related to the dislocation type. For the 60° misfit dislocations in diamond-type semiconductors, $\gamma = 2$. It reveals that the strain in the layer gets more relaxed with denser misfit dislocations.

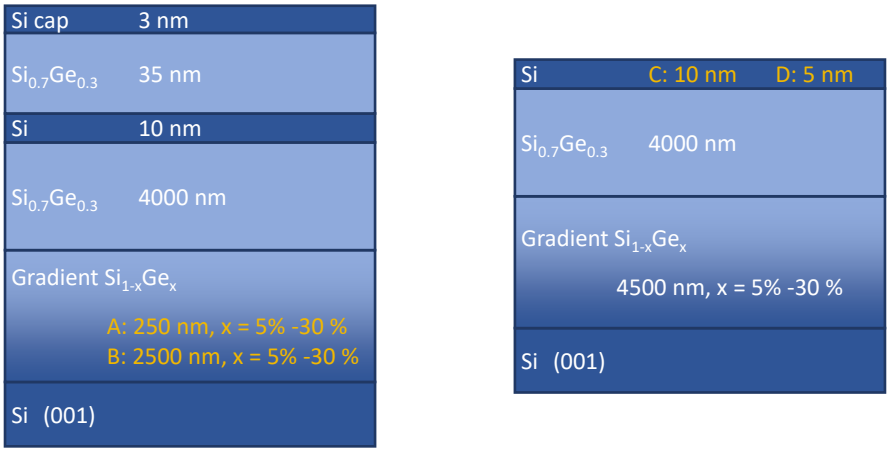
5.2 Results And Discussions

5.2.1 Role of Critical Thickness in SiGe/Si/SiGe Heterostructure Design for Qubits

Here, we present a detailed experimental study on the misfit dislocation formation in tensile strained Si quantum well layers and present a simple model that accounts for dislo-

cation pinning in these thin layers and quantitatively reproduces the observed dislocation network. This work is based on the contrast analysis of the dislocation distribution by TEM and ECCI. We study identical heterostructures grown on relaxed SiGe substrate with different threading dislocation densities as well as samples with quantum well layers of different thicknesses on identical buffers. It shows that misfit dislocations form above the critical thickness defined by the Matthews–Blakeslee criterion.

Samples Applied



(a) (b)

Figure 5.7: Schematic structure of the investigated SiGe/Si/SiGe heterostructure: (a) samples A and B with the different bottom SiGe buffer layers, indicated by the yellow text; (b) samples C and D with the different Si top layer thickness, indicated by the yellow text.

Epitaxial growth of the four SiGe heterostructures investigated in this chapter was carried out by utilising a reduced pressure CVD system. The growth processes are exhibited in section 2.1.2. The schematic layer stacks of the samples are listed in Figure 5.7. Samples A and B in Figure 5.7 (a) are rudimentary SiGe/Si/SiGe heterostructures for qubits. The gradient $Si_{1-x}Ge_x$ layers are designed differently resulting in the different threading dislocation density levels between samples A and B. Samples C and D are grown to investigate the role of critical thickness on the strain relaxation in the Si quantum well layers. The layers above the Si strained layers are left out in samples C and D to ease the ECCI investigation.

TEM (section 2.2.2) and ECCI (section 2.2.3) were applied to characterise the sample.

Misfit Dislocation Observation in SiGe/Si/SiGe Heterostructures

Figure 5.8 presents typical examples of TEM bright field images taken under different diffraction conditions to analyse the dislocation distribution in SiGe/Si/SiGe. Here, it is focused on the impact of the different threading dislocation densities in buffers A and B on the relaxation of the Si quantum well layer. According to the results from defect selective etching, the relaxed buffer of sample A has a threading dislocation density of $1.4 \times 10^7\,\mathrm{cm}^{-2}$ (Figure 5.8 (a) and (b)) and the relaxed buffer of sample B has threading dislocation density of $3 \times 10^5\,\mathrm{cm}^{-2}$ (Figure 5.8 (d) and (e)). For clarity, bright field images using $2\,2\,0$ and $2\,\bar{2}\,0$ reflections are shown here exclusively, since they already express the main features. The dislocations are numbered consecutively. The main features of the both samples can be discussed by taking as an example the dislocations 2, 8 and 9. Dislocation 2 has a long threading segment at the right hand side coming from the buffer. It bends into the $(0\,0\,1)$ plane and forms a misfit segment lying along the $[1\,\bar{1}\,0]$ direction. It has a short threading segment at the left end. The long misfit segment has a characteristic double contrast in the $2\,2\,0$ and appears as a single line in $2\,\bar{2}\,0$ reflection. From the geometry, that means the length of the threading segments, it can be concluded that the long segment at the right hand side is a threading dislocation that comes from the SiGe buffer and forms the misfit dislocation at the interface of the quantum well layer, while the left hand threading segment is the one that penetrates the surface. The double contrast is due to the splitting of a perfect 60° dislocation, for example,

$$\frac{a}{2}[1\,0\,1] \rightarrow \frac{a}{6}[1\,1\,2] + \frac{a}{6}[2\,\bar{1}\,1]. \tag{5.16}$$

Dislocation 8 has very similar contrast behaviour, which means it is split to two partial dislocations, for example,

$$\frac{a}{2}[1\;0\;1] \rightarrow \frac{a}{6}[1\,\bar{1}\,2] + \frac{a}{6}[2\,1\,1]. \tag{5.17}$$

Respectively, the dislocation 9 vanishes at the $2\,2\,0$ and is present at the $2\,\bar{2}\,0$ reflection. This indicates that the dislocation 9 is a 90° dislocation, or more specifically a Lomer dislocation [160]. From the spatial arrangement of dislocation 9, it may infer that it has formed by the interaction between the 60° dislocations 5 and 10 [151]. Similarly, the 90° dislocation 19 can be explained by a reaction between the 60° dislocations 14 and 20. All dislocations analysed in samples A and B can be assigned to these basic characteristics

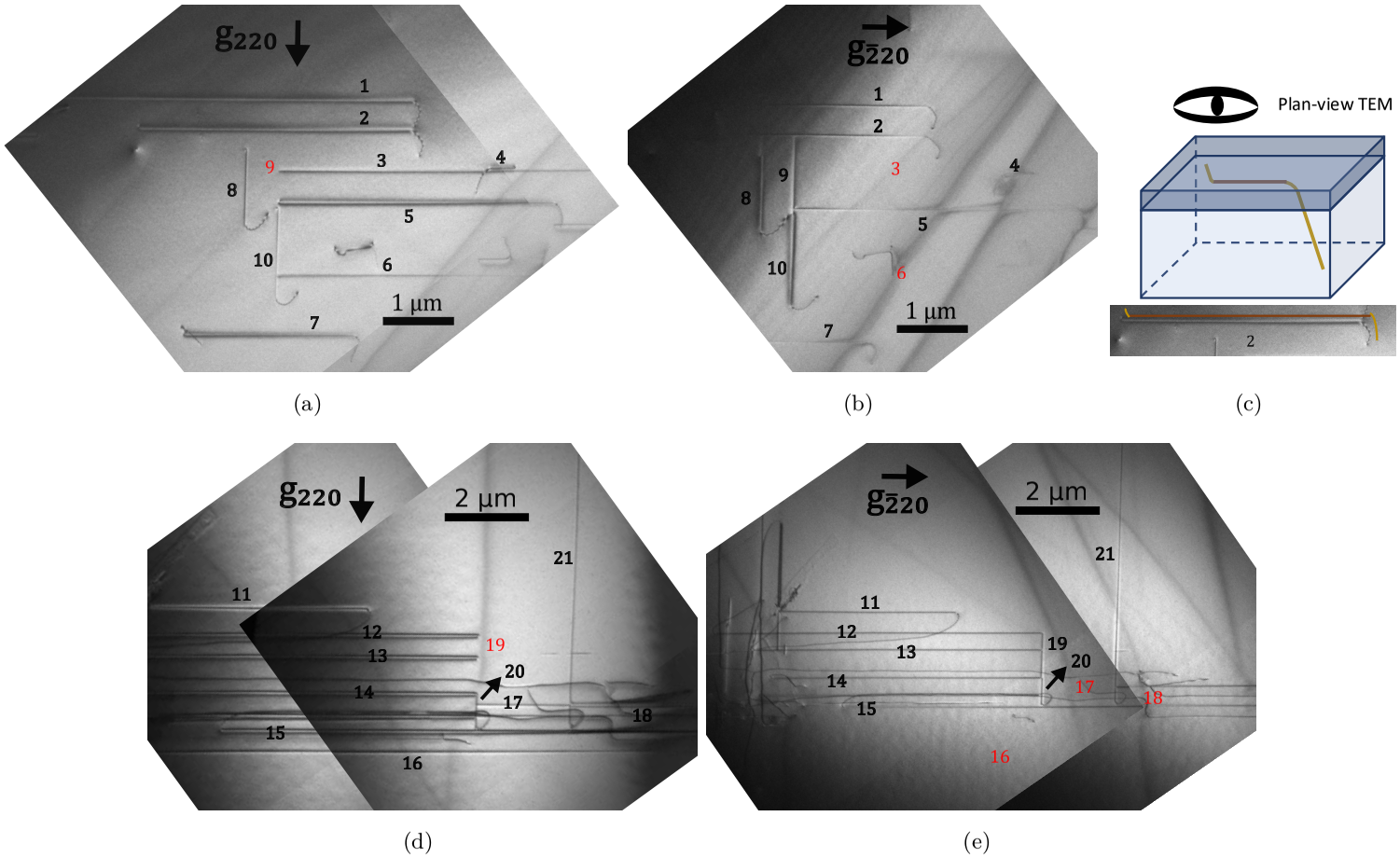


Figure 5.8: Plan-view TEM images of SiGe/Si/SiGe heterostructures on different SiGe virtual substrates: (a) and (b) presenting sample A with a virtual substrate having a threading dislocation density of $1 \times 10^7\,\mathrm{cm}^{-2}$; (c) 3D construction of misfit dislocation formation due to the bending of threading dislocation in Figure 5.2 corresponding to the dislocation 2 observed by plan-view TEM in (a); (d) and (e) presenting sample B with a virtual substrate having with a threading dislocation density of $3 \times 10^5\,\mathrm{cm}^{-2}$. The diffraction vectors **g** are indicated by black arrows. The misfit dislocations are numbered consecutively, whereas the invisible dislocations are numbered in red colour. The crystallographic orientations of the misfit dislocations are noted in Table 5.1.

for a detailed analysis as is shown in Table 5.1. All 60° misfit dislocations are a result of the bending of pre-existing threading dislocation in the buffer: The misfit dislocations are split into Shockley partials. In the TEM images such as Figure 5.8 over areas of $5\times7\,\mu m^2$ and $10\times15\,\mu m^2$, it is clear that 70 % of the misfit dislocations are 60° dislocations while 30 % are 90° dislocations. Noticeably, dislocations 5, 6 and 3 are blocked at dislocations 9 and 10.

Table 5.1: Summary of the Burgers vector analysis for misfit dislocations of sample A and B depicted in Figure 5.8. The "✓" indicates the visibility of the misfit dislocations in the respective diffraction conditions or that they split into dislocation partials, while the "✗" indicates invisibility or that they do not split. The last column of the table presents the dislocation types.

sample	dislocation #	line direction	$\mathbf{g}_{220}$	$\mathbf{g}_{\bar{2}20}$	split	type
A	1	$[1\,\bar{1}\,0]$	✓	✓	✓	60°
	2	$[1\,\bar{1}\,0]$	✓	✓	✓	60°
	3	$[1\,\bar{1}\,0]$	✓	✗	✗	90°
	4	$[1\,\bar{1}\,0]$	✓	✓	✗	60°
	5	$[1\,\bar{1}\,0]$	✓	✓	✓	60°
	6	$[1\,\bar{1}\,0]$	✓	✗	✓	90°
	7	$[1\,\bar{1}\,0]$	✓	✓	✓	60°
	8	$[1\,1\,0]$	✓	✓	✓	60°
	9	$[1\,1\,0]$	✗	✓	✗	90°
	10	$[1\,1\,0]$	✓	✓	✓	60°
B	11	$[1\,\bar{1}\,0]$	✓	✓	✗	60°
	12	$[1\,\bar{1}\,0]$	✓	✓	✓	60°
	13	$[1\,\bar{1}\,0]$	✓	✓	✓	60°
	14	$[1\,\bar{1}\,0]$	✓	✓	✓	60°
	15	$[1\,\bar{1}\,0]$	✓	✓	✓	60°
	16	$[1\,\bar{1}\,0]$	✓	✗	✗	90°
	17	$[1\,\bar{1}\,0]$	✓	✗	✗	90°
	18	$[1\,\bar{1}\,0]$	✓	✗	✗	90°
	19	$[1\,1\,0]$	✗	✓	✗	90°
	20	$[1\,1\,0]$	✓	✓	✓	60°
	21	$[1\,1\,0]$	✓	✓	✗	60°

Samples A and B show qualitatively a similar structure but are distinguished quantitatively by the spacing of the misfit dislocations d_{MD} at the interface. Table 5.2 compares the

threading dislocation spacings d_{TD} obtained from defect-selective etching of the buffer to the misfit dislocations spacing d_{MD} obtained from the TEM images. Here,

$$d_{\mathrm{MD}} = \frac{\mathrm{A}}{\sum l_i}, \tag{5.18}$$

where l_i is the length of each individual misfit dislocation and A is the area of the image. The sum is performed over all misfit dislocations in the images of each sample. The threading dislocation spacing d_{TD} is calculated from the threading dislocation density according to:

$$d_{\mathrm{TD}} = \frac{1}{\sqrt{\mathrm{TDD}}}. \tag{5.19}$$

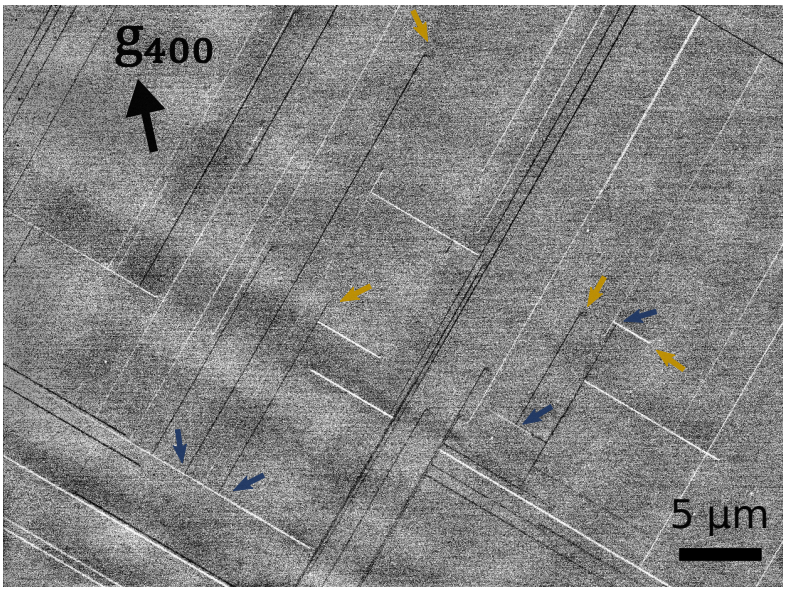
TDD is threading dislocation density. The threading dislocation spacing d_{TD} is around three times the misfit dislocation spacing d_{MD} in both samples A and B. The strain relaxation $\epsilon_{\mathrm{relax}}$ in these layers is also calculated by the relaxation dependence on the misfit dislocation spacing d_{MD} in Equation (5.15).

Table 5.2: Quantitative evaluation on the dislocations in the SiGe heterostructures. Here, d_{TD} and d_{MD} infer threading dislocation spacing and misfit dislocation spacing. The strain relaxation $\epsilon_{\mathrm{relax}}$ in the Si layers inside these samples are calculated with Equation (5.15).

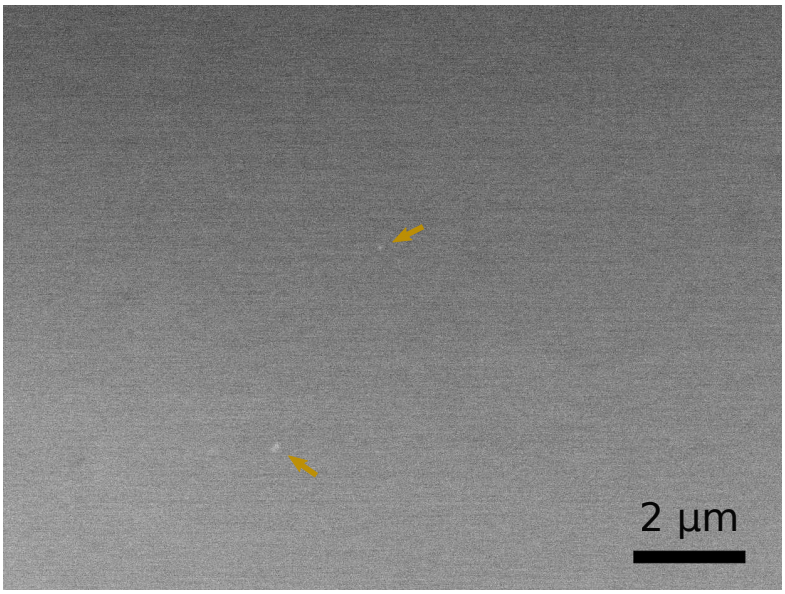
Sample	d_{TD}	d_{MD}	$\frac{d_{\mathrm{TD}}}{d_{\mathrm{MD}}}$	$\epsilon_{\mathrm{relax}}$
A	3.2 µm	1.1 µm	2.91	0.02 %
B	18.3 µm	6.4 µm	2.86	0.003 %
C	6.2 µm	1.8 µm	3.4	0.01 %

Thickness Effects on Dislocations in Strained Si Layers

The analysis above has shown that the 10 nm thick quantum well layer exceeds the critical thickness and that each individual threading dislocation transforms into a misfit dislocation according to the model proposed by Matthews and Blakeslee. In the following, the results from Si quantum well layers with thicknesses above (10 nm) and below (5 nm) the critical thickness (8.5 nm) according to the Matthews-Blakeslee criterion grown on identical $Si_{0.7}Ge_{0.3}$ buffer layers with a threading dislocation density of $8 \times 10^6\,\mathrm{cm}^{-2}$ are presented. For analysis of the relaxation by misfit dislocations, this work relies on ECCI, which is sensitive to dislocations located in the sample stack close to the surface and permits to scan large areas compared to TEM.



(a)



(b)

Figure 5.9: Electron channelling contrast images showing dislocations in Si/SiGe heterostructure: (a) sample C - 10 nm Si on relaxed SiGe buffer; (b) sample D - 5 nm Si on relaxed SiGe buffer. In sample C, misfit dislocations are present as lines with bright or dark contrast. Yellow arrows indicate examples of threading dislocations. Blue arrows indicate the examples when misfit dislocations meet other perpendicular misfit dislocations.

Figure 5.9 (a) shows a typical ECCI image of sample C using the 4 0 0 reflection. Two perpendicular sets of misfit dislocations aligned with [1 1 0] and [1 $\bar{1}$ 0] are visible. Similar to the results obtained by TEM, those misfit dislocations are related to threading dislocation segments at one of their ends (examples are indicated with yellow arrows). In almost all cases, the other end is an intersection with another, perpendicular misfit dislocation line (examples are indicated with blue arrows). Figure 5.9 (b) shows a corresponding ECCI image of sample D under identical imaging conditions. Here, no misfit dislocations can be observed, but a few spots with contrast indicated by yellow arrows can be threading dislocations.

In order to compare our results with samples A and B, the misfit and threading dislocation spacing of sample C from Figure 5.9 (a) is quantified in Table 5.2. The factor between the threading dislocation spacing and the misfit dislocation spacing in sample C is 2.95, similar to sample A and sample B. This striking similarity in the factor among all the samples suggests that there is a distinct relation between threading dislocation spacing and misfit dislocation spacing, independent of the threading dislocation density of the buffer. This relation has been investigated in detail by a geometric Monte Carlo approach by Dr. Gradwohl from our group [7].

Strain Relaxation in Si Quantum Well Layer

From the misfit dislocation formation mechanism by Matthews and Blakeslee, every pre-existing threading dislocation is a source of a misfit dislocation. Therefore, the misfit dislocation network in the strained layer is related to the threading dislocation density. On the other hand, the misfit dislocation network is also affected by the blocking interactions between the misfit dislocations.

The experiment results above show the correlation between the threading dislocation density and the misfit dislocation spacing. This is statistically presented in Table 5.2. Combining with Equation (5.15), the threading dislocation density further affects strain relaxation by its effect on the misfit dislocation spacing.

Here, we will further visualise the correlation between the threading dislocation density and the relaxation in the epitaxial layer with some calculations. Here, the geometry is taken of a sample as a square of $200 \times 200\,\mathrm{mm}^2$ with edges along $\langle 1\,1\,0 \rangle$. Two different conditions are considered here:

- The first condition is that the blocking interaction between misfit dislocations happens. According to the statistic listed in Table 5.2 and also a Monte Carlo simulation performed by Dr. Gradwohl [2], the threading dislocation spacing and the misfit dislocation spacing have a roughly constant ratio around 3 and are independent of the sample size. Merging Equation (5.15), Equation (5.19) and the constant ratio together, the correlation of relaxation and threading dislocation density TDD can be written as

$$\begin{aligned}\epsilon_{\text{relax}} &= \frac{|\mathbf{b}|}{\gamma d_{\text{MD}}} \\ &= \frac{|\mathbf{b}|}{2 \cdot \frac{1}{3}\sqrt{\frac{1}{\text{TDD}}}} \\ &= \frac{3}{2}|\mathbf{b}|\sqrt{\text{TDD}}.\end{aligned} \tag{5.20}$$

- The second condition is that the blocking interaction between misfit dislocations does not happen. The misfit dislocation can extend till the end of the wafer. In this case, the average misfit dislocation length is assumed as the half size of the wafer. Since in this case, the wafer is $a^2 = 200 \times 200\,\text{mm}$ square, the average length of misfit dislocation is reasonably assumed as $\frac{a}{2} = 100\,\text{mm}$. The number of misfit dislocations equals the number of threading dislocations x which means

$$x = \text{TDD} \cdot a^2. \tag{5.21}$$

  According to Equation (5.18), the misfit dislocation density MDD and misfit dislocation spacing d_{MD} are

$$\text{MDD} = \frac{x \cdot \frac{a}{2}}{a^2} = \frac{x}{2a}, \tag{5.22}$$

$$d_{\text{MD}} = \frac{1}{\text{MDD}} = \frac{2a}{x}. \tag{5.23}$$

  Introducing this into Equation (5.15), the relaxation when the misfit dislocations don't block each other is

$$\begin{aligned}\epsilon_{\text{relax}} &= \frac{|\mathbf{b}|}{\gamma d_{\text{MD}}} \\ &= \frac{|\mathbf{b}| \cdot a \cdot \text{TDD}}{4}.\end{aligned} \tag{5.24}$$

The correlations between relaxation and threading dislocation density in both conditions with (Equation (5.20)) or without (Equation (5.24)) blocking interaction between misfit

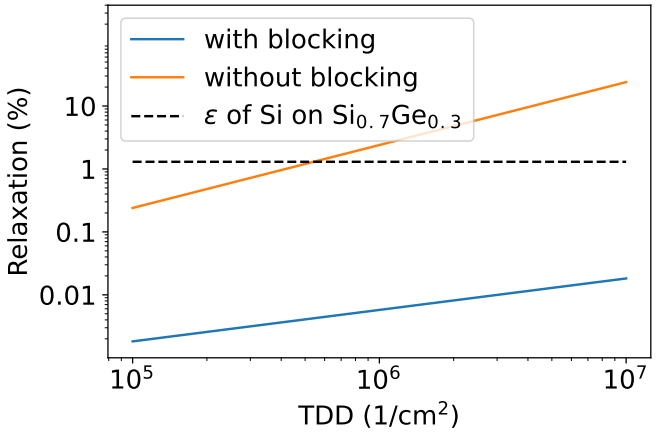


Figure 5.10: The dependence of the strain relaxation in the Si layer on $Si_{0.7}Ge_{0.3}$ substrates on the threading dislocation density in two conditions: the blocking interaction happens between the misfit dislocations (blue line); the blocking interaction doesn't happen between misfit dislocations (orange line). The misfit strain of the Si on $Si_{0.7}Ge_{0.3}$ is 1.1 % marked as the black dash line.

dislocations are plotted in Figure 5.10. The misfit strain level of the unrelaxed Si on $Si_{0.7}Ge_{0.3}$ is also indicated in Figure 5.10. From here, the relaxation with blocking effect is more than two magnitudes less than without blocking. Without blocking effect, the Si on $Si_{0.7}Ge_{0.3}$ can reach fully relaxation with threading dislocation density of $1 \times 10^6\,\mathrm{cm}^{-2}$. Respectively, when the misfit dislocations block others, the relaxation stays in the range of 0.01 % even when the substrate has a threading dislocation density of $1 \times 10^7\,\mathrm{cm}^{-2}$.

Here, only square geometry is applied. With conventional circular geometry for wafers, more geometric effects need to be taken into consideration.

Conclusion

To conclude the misfit dislocation generation mechanism in SiGe/Si/SiGe heterostructures, the main electron microscopy results in Figure 5.8 and Figure 5.9 are summarised:

- All Si quantum well layers that are thicker than the critical thickness given by the Matthews-Blaskeslee criterion (samples A, B, C) exhibit misfit dislocations at the interface between the quantum well layer and the relaxed buffer.

- All analysed misfit dislocations in samples A, B and C have a line direction along in-plane $\langle 1\,1\,0 \rangle$. These misfit dislocation segments form due to the glide of threading dislocations pre-existing in the relaxed SiGe buffer as described by Matthews and Blakeslee.

- The majority of the misfit dislocations in samples A and B (70 %) are 60° dislocations, while the rest are Lomer dislocations.

- Most 60° dislocations are split into Shockley partials. The splitting of 60° dislocation is a typical feature of misfit dislocations accommodating at tensile strain due to the competition between energetic favourite and strain releasing efficiency of partial dislocations subsection 5.1.2. Therefore, it can be concluded that these misfit dislocations are located at the tensile strained layer, which means at the interface between the SiGe buffer layer and the Si quantum well layer.

- Dislocations that meet perpendicular misfit dislocations at the interface are blocked and cannot further extend at the given quantum well layer thicknesses.

- Quantitative evaluation of the threading dislocation spacing and the misfit dislocation spacing shows that their ratio has a factor of approximately 3 (Table 5.2), independent of the threading dislocation density in the respective buffer. This was simulated by a Monte Carlo method [2].

From these findings, it can be concluded that the presence of threading dislocations in the relaxed buffer leads to the formation of misfit dislocation segments at the interface of the Si quantum well layer, as soon as the critical thickness of the quantum well layer as defined by Matthews and Blakeslee is exceeded. Also, at the given thickness of the quantum well layer, misfit dislocations block the glide of threading dislocations and thus the further extension of misfit dislocations [159]. It is worth mentioning that the blocking mechanism can be overcome when a thicker quantum well layer is grown. When the layer thickness is beyond another critical value, the forces from misfit strain on the threading dislocation segments are greater than the blocking forces from the perpendicular misfit dislocations, which results in the unblocking of the misfit dislocation. According to the theoretical work of Freund [158], this other critical thickness of the quantum well layer studied here is around 20 nm for dislocation unblocking. The quantum well layers in SiGe/Si/SiGe heterostructures for qubit applications are commonly way below this value.

The mechanism of misfit dislocation formation from threading dislocation gliding was often purposely promoted for the strain relaxations in epitaxial layers in order to minimise the generation of new threading dislocations during the strain relaxation, such as epitaxial Ge or SiGe layers on Si (001) substrates [161, 162, 145]. However, a fully strained Si quantum well layer is required here for qubits, so the occurrence of this mechanism is not desired.

These findings are relevant for the design of SiGe/Si/SiGe heterostructures for spin qubits, since dislocations at the interface of the quantum well layer lead to strong local fluctuations of strain and thus the valley splitting of the Si conduction band [140, 163, 164]. While threading dislocations in these structures might be tolerable to a certain degree because they only make up a small area, misfit running inside the Si quantum well layer interface affects a large fraction of the film and will likely have a negative impact on the qubit device. Although a higher valley splitting of the Si conduction bands is realised through a higher Ge concentration in the SiGe buffer, which leads to larger tensile strain, the critical thickness for plastic relaxation will at the same time be reduced, as shown in Figure 5.2. Therefore, a trade-off balancing these two effects needs to be made.

Regarding the kinetics, the activation barrier of the misfit dislocation formation due to pre-existing threading dislocation gliding when exceeding the critical thickness is low. The activation energy may easily be overcome by the CVD growth temperature. A way to prevent relaxation in these structures exhibiting threading dislocations could be to reduce growth at temperatures low enough to prevent dislocation glide. MBE gives the possibility to perform the growth at temperatures as low as 350 °C. However, the post-growth processing temperatures that are currently used in semiconductor device fabrication highly exceed this temperature and hence pose a limit to this approach. These are discussed in detail in subsection 5.2.2.

Methodologically, our work shows that electron channelling contrast imaging is a versatile tool for analysing the relaxation of epitaxial layers at an early stage and in thin layers, where conventional XRD techniques are not sensitive enough [165].

5.2.2 Strain Relaxation from Annealing of SiGe Heterostructures for Qubits

In this work, we investigate the misfit dislocation propagation in the strained ^{28}Si layer grown on a $Si_{0.7}Ge_{0.3}$ substrate at 350 °C by MBE during post-growth annealing at

temperatures from 500 °C to 600 °C by ECCI. By plotting the dislocation propagation velocities over the inverse temperature, we obtained an Arrhenius-type plot, from which the activation barriers of the propagation are extracted. The same experiment was performed at the strained Ge layer grown by MBE at 270 °C on the relaxed $Si_{0.3}Ge_{0.7}$ buffer. The annealing temperatures were from 300 °C to 400 °C The misfit dislocation propagation blocking by other misfit dislocations occurs in the 10 nm ^{28}Si but not in the 20 nm Ge, which has a good agreement with the criterion proposed by subsection 5.1.4. Our results show that strain relaxation happens not only during the epitaxial growth but also during the post-growth annealing. Based on these observations, we can propose that the misfit dislocation propagation in ^{28}Si or Ge quantum well layer for qubits can be suppressed kinetically by reducing the epitaxy temperature and the temperature applied in post-epitaxy device fabrication processes.

Samples Applied

The epitaxial growth of the SiGe heterostructures in this chapter was carried out by a hybrid MBE/CVD technique (chapter 2). The relaxed $Si_{0.7}Ge_{0.3}$ and $Si_{0.3}Ge_{0.7}$ substrates were grown on (0 0 1) Si wafers by reduced pressure and atmospheric CVD respectively (section 2.1.2). Chemical Mechanical Polishing (CMP) was used to remove the cross hatch surface roughness of the relaxed buffer layers. The $Si_{0.7}Ge_{0.3}$ substrate has a threading dislocation density of around $1 \times 10^7\,cm^{-2}$, while the $Si_{0.3}Ge_{0.7}$ substrate has a threading dislocation density of $5 \times 10^5\,cm^{-2}$. Surface preparations combining wet chemical cleaning and in-situ annealing and atom hydrogen irradiation at 700 °C were done on these SiGe substrates. Afterwards, 10 nm ^{28}Si / 50 nm $^{28}Si_{0.7}Ge_{0.3}$ or 20 nm Ge / 30 nm $^{28}Si_{0.3}Ge_{0.7}$ was grown above these relaxed SiGe substrates by the isotope engineered MBE. The sketches of these epitaxial layers are shown in Figure 5.11 (a) and (f). The detailed growth processes are described in section 2.1.1 and section 2.1.2.

The annealing of the strained ^{28}Si and Ge layers was performed on the pieces from the same wafer in a UHV chamber with a vacuum of around 1×10^{-7} mbar at different temperatures for 10 min. Before annealing, the heater was preheated for at least 10 min and the sample was delivered into the annealing position within 1 min. After annealing, the sample was removed out from the annealing position immediately.

To investigate the defects in these layers, ECCI was performed at 10 kV and 3.2 nA for the misfit dislocation detection in the layer stacks close to the surfaces.

Results

Figure 5.11 presents the schematics of the studied strained ^{28}Si layer as well as the strained Ge layer. The ^{28}Si layer has 1.1 % tensile strain and the Ge layer has 1.3 % compressive strain [131]. Figure 5.11 (b) - (e) show the ECCI images of the misfit dislocation network in the as-grown and post-growth annealed ^{28}Si layers. The orthogonal dislocations lie along two $\langle 1\,1\,0 \rangle$ directions at the interface between the strained layers and the relaxed SiGe buffer and their average misfit dislocation length develops with the increasing annealing temperatures. Figure 5.11 (g) - (j) respectively show the misfit dislocation network in the strained Ge layer. The misfit dislocation networks show similar development with increasing post-growth annealing temperatures.

The misfit dislocation propagation velocities can be computed by dividing the average misfit dislocation lengths by the annealing time, 10 min. The measured velocities are plotted on Arrhenius curves in Figure 5.12 in regards to the modified annealing temperatures. The fitted activation energy from Equation (5.7) of the threading dislocation gliding is 0.49 ± 0.01 eV in the strained ^{28}Si and 0.39 ± 0.10 eV in the strained Ge, where the errors are extracted from the linear regression fitting. The temperature modification is performed considering the heat radiation exchange between the graphite heater and the emission character from the molybdenum sample holder, which is described in detail in the end of this chapter.

The theoretical values of the activation energies of the misfit dislocation propagation calculated from Dodson-Tsao law (subsection 5.1.3) and their experimental values from Figure 5.12 are listed in Table 5.3. The theoretical activation energies have big ranges because τ_0 in Equation (5.7) is 5-10 % of the shear modulus in semiconductors. Table 5.3 shows the agreement between the theoretical and the experimental activation energies.

It is worth mentioning that there are some characteristic differences between the misfit dislocation networks in the strained ^{28}Si layers and in the strained Ge layers. In Figure 5.11 (g), the misfit dislocations often end when they meet other perpendicular misfit dislocations. That is not the case in Figure 5.11 (j), where the perpendicular misfit dislocations intersect each other. This feature of the misfit dislocation network in ^{28}Si matches well with the blocking mechanism between the perpendicular misfit dislocations, which was also observed on the strained Si layer grown by CVD (subsection 5.2.1). The misfit dislocation propagation is blocked by perpendicular misfit dislocations. The reason why the misfit dislocations in the strained Ge layer overcome this blocking mechanism is

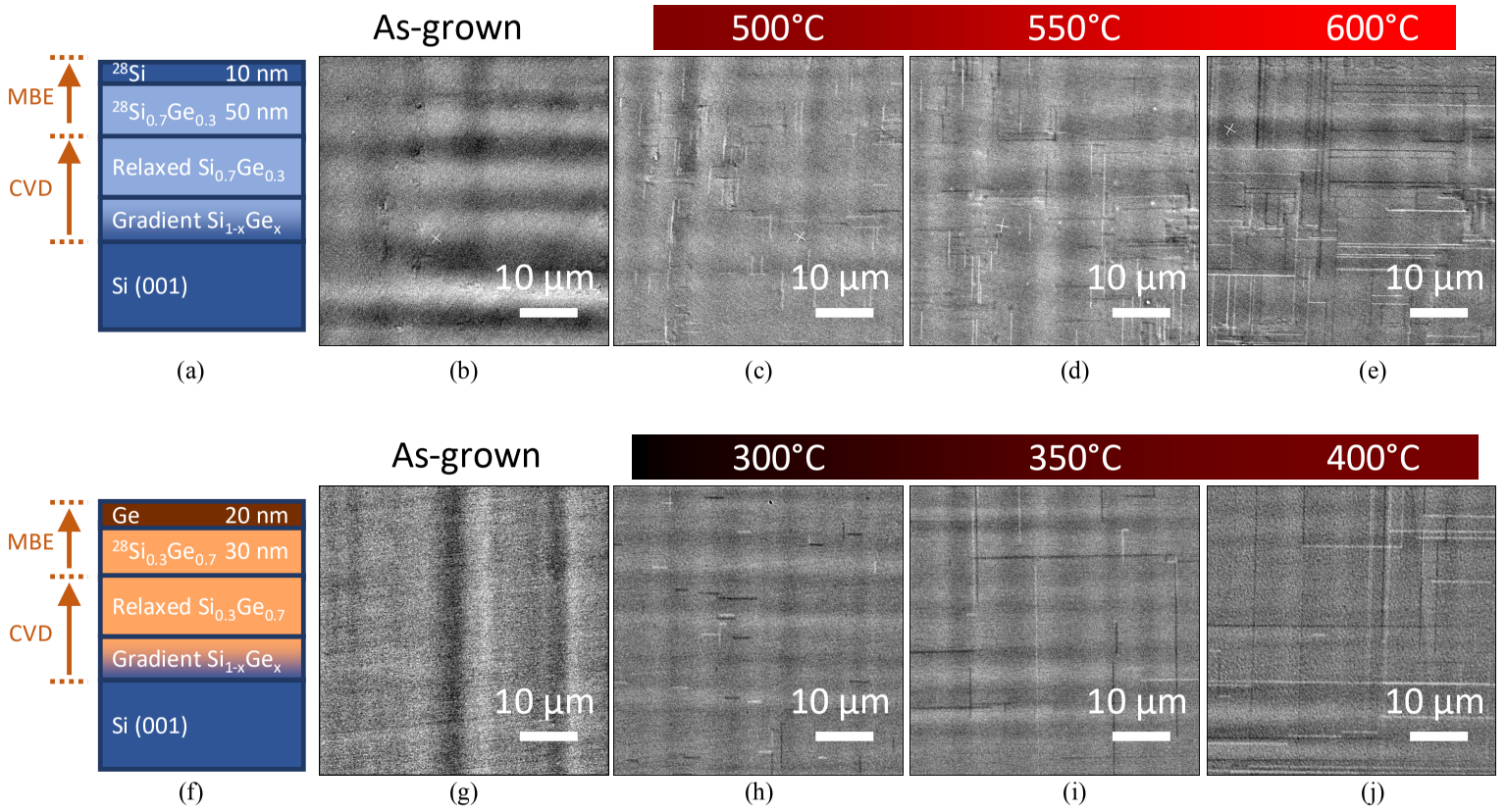
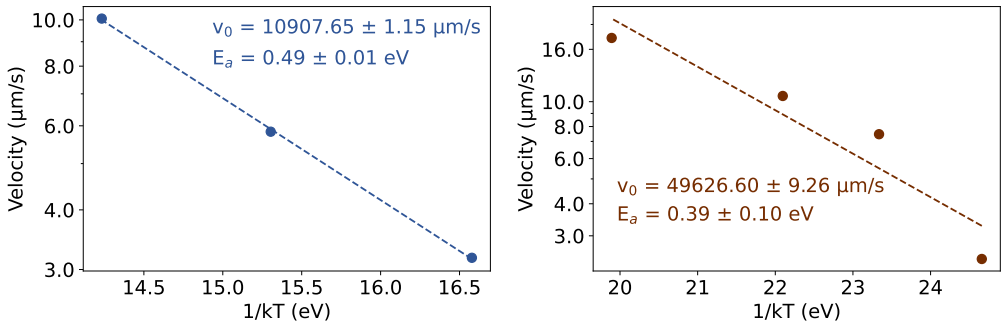


Figure 5.11: Schematic cross sections of the strained ^{28}Si (a) and Ge (f) layers on relaxed SiGe substrates realised by a hybrid MBE/CVD technique. ECCI images showing misfit dislocations in the strained ^{28}Si and Ge layers: (b) the as-grown ^{28}Si layer presents no misfit dislocation; the misfit dislocations form in the ^{28}Si layer through the annealing at temperatures from 500 °C to 600 °C (c - e) for 10 min; Similarly, the as-grown Ge layer presents no misfit dislocation (g); the misfit dislocations form in the Ge layer through the annealing at temperatures from 300 °C to 400 °C (h - j) for 10 min. The annealing temperatures are indicated above the ECCI images.



(a) (b)

Figure 5.12: The Arrhenius-type plots of the misfit dislocation propagation in the strained ^{28}Si layer (a) and in the strained Ge layer (b). The measurements are fitted into Equation (5.6), where the v_0 and E_a from fitting are listed in the figures.

Table 5.3: The experimental and theoretical activation energies of the misfit dislocation propagation.

Material System	Strain	E_a (Experimental)	E_a (Theoretical)
10 nm strained ^{28}Si on relaxed $Si_{0.7}Ge_{0.3}$	1.1 % tensile	0.49 ± 0.01 eV	0.44 ... 1.32 eV *
20 nm strained Ge on relaxed $Si_{0.3}Ge_{0.7}$	1.3 % compressive	0.39 ± 0.10 eV	0.14 ... 0.87 eV *

*The variant energies are calculated based on the fact that the zero-temperature flow stress τ_0 in Equation (5.7) is roughly 5-10 % of the shear modulus in semiconductors [154].

that the Ge layer is thicker than the ^{28}Si layer. The thickness of the Ge layer, 20 nm, is approaching the critical value for the unblocking mechanism.

These blocking and unblocking mechanisms from the dislocation interactions can also influence the experimental propagation velocity measurement and further the derived activation energies in Table 5.3. The average dislocation lengths measured in the experiment are likely shorter due to the blocking [155, 166]. This can explain why the experimental activation energy in the strained ^{28}Si layer lies on the lower end of the theoretical range, respectively the experimental activation energy in the strained Ge layer lies in the middle of the theoretical activation energy range.

Discussions and Conclusions

Combining the results in this chapter, several thoughts regarding the misfit dislocations in SiGe heterostructures for qubits occur:

- When the ^{28}Si or Ge quantum well layers in SiGe heterostructures for qubits are above the critical thickness of misfit dislocation formation defined by Matthew-Blakeslee criterion, the epitaxial growth of the heterostructures by MBE performed at low temperatures can suppress the misfit dislocation formation kinetically in comparison to CVD, which generally utilises higher growth temperatures.

- Even though the growth can happen at a lower temperature in MBE, the post-growth processes like the oxide layer deposition often happen at 300 °C [167, 168]; the ohmic contact for the Ge layer often happens at around 400 °C [169] and for the Si layer happens at 700 °C [32]. These post-growth processes can potentially activate the misfit dislocation propagation.

- According to our findings, a thermal budget for the post-growth processes can be reasonably suggested as $0.5\,T_m$ according to the study of Dodson and Tsao [170, 171]. If the post-growth annealing must access this thermal budget, shortening the annealing time is also a way to suppress the misfit dislocation propagation kinetically.

In summary, the misfit dislocation kinetics and interactions are studied. The MBE as-grown strained ^{28}Si and Ge layer on relaxed SiGe substrate are free of misfit dislocations even though their thicknesses are above the critical thickness. Misfit dislocations form at the interface of the strained layers due to the gliding of the pre-existing threading dislocations during the post-growth annealing. The misfit dislocation propagation velocity increases with the annealing temperatures exponentially. The activation energies of the propagation are derived from the Arrhenius-type equation and they agree well with the stress-dependent dislocation kinetics stated by Dodson and Tsao [153]. Furthermore, the misfit dislocation propagation in the strained ^{28}Si layer is blocked by the perpendicular misfit dislocations, whereas the propagation in the strained Ge layer is unblocked. These facts can be explained by the thickness difference between the stained ^{28}Si and the strained Ge layers. The strained ^{28}Si layer here is quite thin so that the misfit dislocation

propagation cannot overcome the strain barrier from the other perpendicular misfit dislocation. It is the other case in the strained Ge layer here.

Together, this work can enable the understanding of the strain relaxation process with misfit dislocation formation and propagation in the SiGe heterostructures for both electron spin qubits and hole spin qubits.

Temperature Modification

According to the Dodson-Tsao law (Equation (5.6)), the activation energies E_a can be obtained from the functional dependency of the misfit dislocation propagation velocity on the annealing temperature. The annealing experiments were done by putting the samples on a molybdenum holder under a pre-heated heater and taking the sample with the holder out of the heating immediately after annealing for 10 min. Since the samples take time for heat-up and cool-down, just taking the dislocation propagation velocities calculated with 10 min and the respective preset annealing temperatures into the Equation (5.6) would lead to a systematic error in the activation energy. Hence, it is necessary to determine the temperature history of the samples as a function of time, which is done here. And then the annealing temperatures can be modified and then applied into the Equation (5.6).

We applied the temperature modification with the molybdenum holder because the molybdenum holder is ten times bigger than the samples. This means in the text, T means both the temperature of the molybdenum holder and the sample.

Generally, the misfit dislocation length L can be obtained by integrating Equation (5.6),

$$L = \int_{t_0}^{t} v_0 \exp\left(\frac{-E_a}{kT(t)}\right) dt, \tag{5.25}$$

where t is the time and $T(t)$ is the temperature of the sample (also the sample holder) regards to time including the heating up and cooling down. When $T(t)$ is substituted with a fixed modified temperature T^* and t is substituted with a fixed time $t^* = 10\,\text{min}$, it can be rewritten as

$$L = v_0 \exp(\frac{-E_a}{kT^*})t^*. \tag{5.26}$$

Now T^* can be determined combining Equation (5.25) and Equation (5.26) . The remaining question here is the temperature history $T(t)$.

Several conditions are assumed to solve the $T(t)$: In the calculation, only the heat radiation is considered. The heat convection by gas motion is ignored because the annealing happens in UHV. The heat conduction is ignored because only a small part of the substrate holder is touched with the supporting ring. The radiation of the MBE chamber is ignored because it is cold. Besides, a one dimensional model is applied here since the annealing happens in the middle of the substrate holder and the temperature is likely homogeneous horizontally.

The heat power $P(T)$ the molybdenum holder obtained equals to the heat radiation from the heater P_{heater} minus the emitted heat on two sides of the holder P_{holder}. Since the surface area of the holder and the heater are the same,

$$\begin{aligned} P(T) &= P_{\text{heater}} - P_{\text{holder}} \\ &= \epsilon_{\text{heater}}\,\sigma\,{T_{\text{heater}}}^4 - 2\epsilon_{\text{Mo}}\,\sigma\,T^4. \end{aligned} \tag{5.27}$$

where ϵ is emissivity and σ is Stefan-Boltzmann constant. Here, $\epsilon_{\text{heater}} = 1$ and $\epsilon_{\text{Mo}} = 0.2$ for molybdenum holder [172].

Since the heater is switched on in advance and its temperature is held constant by a power control in the experiment, it is assumed that the temperature of the heater stays the same when the holder is added. When the holder temperature T reaches the set (target) temperatures, the system is in equilibrium. So,

$$P(T_{\text{set}}) = \epsilon_{\text{heater}}\,\sigma\,{T_{\text{heater}}}^4 - 2\epsilon_{\text{Mo}}\,\sigma\,{T_{\text{set}}}^4 = 0, \tag{5.28}$$

that tells the heater temperature T_{heater} by each set temperature T_{set}.

During the heat-up and cool-down processes, the heat absorbed by the holder results in a temperature increase of the holder,

$$CdT = P(T)dt, \tag{5.29}$$

where C is the heat capacity of the molybdenum holder and can be calculated with the holder thickness (2 mm), the specific heat ($0.25\,\text{J}\,\text{g}^{-1}\,\text{K}^{-1}$) and the density ($10.2\,\text{g}\,\text{cm}^{-3}$) from molybdenum.

We substitute $P(T)$ from Equation (5.27) into Equation (5.29) and do the integration, then get:

$$CdT = (\epsilon_{\text{heater}}\,\sigma{T_{\text{heater}}}^4 - 2\epsilon_{\text{Mo}}\,\sigma\,T^4)dt, \tag{5.30}$$

$$\int_{T_0}^{T} \frac{C}{\epsilon_{\text{heater}}\,\sigma{T_{\text{heater}}}^4 - 2\epsilon_{\text{Mo}}\,\sigma\,T^4} dT = \int_{t_0}^{t} dt. \tag{5.31}$$

By numerically solving the ordinary differential equation Equation (5.31), we can get the temperature T over the time t.

For the cooling down when the sample with molybdenum holder is taken away from the holder, therefore,

$$P_{\text{heater}} = 0. \tag{5.32}$$

Now, Equation (5.27) is rewritten as,

$$P(T) = 0 - 2\epsilon_{\text{Mo}}\sigma T^4. \tag{5.33}$$

Do the same substitution $P(T)$ from Equation (5.33) into Equation (5.29) and do the integration, we can get the temperature T over the time t during cooling down.

Taking the experimental annealing time 10 min and also the cooling, the temperature versus time is plotted in Figure 5.13. The cooling time is chosen for 10 min with the reason that the misfit dislocation propagation velocity decrease with temperature exponentially thus lower temperature range is not essential. With $T(t)$, the misfit dislocation length L and the modified temperature T^* can be calculated with Equation (5.31) and Equation (5.26) subsequently regards to each preset temperature T_{set}.

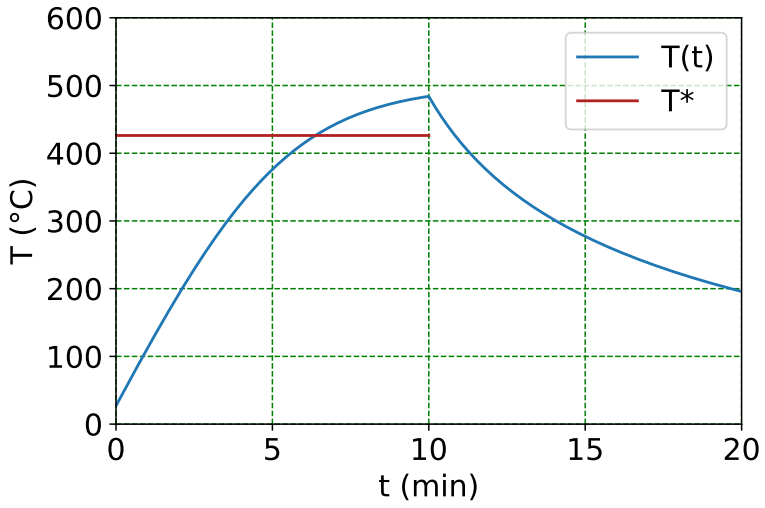


Figure 5.13: Simulation of molybdenum holder temperature T during the heat-up and cool-down processes at the set temperature $T_{\text{set}} = 500\,°\text{C}$. The modified temperature T^* over $t^* = 10\,\text{min}$ is also sketched.

A tourist follows a trail; a mountaineer finds one.

Reinhold Messner

6 Summary and Outlook

Summary

The most important results of this work are summarised as follows.

- Concerning the epitaxial growth:

  - An isotope engineered MBE was established with ^{28}Si source. This MBE is applied on the growth of ^{28}Si quantum well layers for electron spin qubits, Ge quantum well layers for hole spin qubits, and ^{28}SOI for optical quantum emitters.

  - A reliable surface preparation for CVD grown $Si_{0.7}Ge_{0.3}$ substrates and also thin SOI substrate combining the ex-situ wet chemical cleaning and the in-situ annealing and atomic hydrogen irradiation was developed. The in-situ surface preparation significantly reduces the carbon and oxygen concentrations at the interface between these substrates and the epitaxial layers on top.

  - The strained ^{28}Si quantum well layers for electron spin qubits were successfully grown on (0 0 1) Si substrates by a hybrid MBE/CVD technique. Here, the thick relaxed $Si_{0.7}Ge_{0.3}$ virtual substrates are grown by CVD and the $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ stack are grown by the isotope engineered MBE. The isotope enrichment of ^{28}Si in the functional layer stacks is realised by applying a ^{28}Si solid source. The exemplary $^{28}Si_{0.7}Ge_{0.3}/^{28}Si/^{28}Si_{0.7}Ge_{0.3}$ heterostructure has a ^{29}Si isotopic impurity content as low as 200 ppm.

  - The same hybrid MBE/CVD technique was applied to grow compressively strained Ge quantum well layers for hole spin qubits. The prototype of

$^{28}Si_{0.3}Ge_{0.7}/Ge/^{28}Si_{0.3}Ge_{0.7}$ heterostructures show that the Ge quantum well layer has a sharp interface and is fully strained.

- Besides, a ^{28}SOI for optical quantum emitters was also successfully grown by the isotope engineered MBE. The epitaxial ^{28}Si layer on top shows a high crystalline perfection without obvious defects and also high surface smoothness. The optical quantum emitters built on the ^{28}SOI are supposed to offer a sharp emission line and high spin coherence.

- In order to understand the misfit dislocations at the interface of the Si, Ge quantum well layers and further optimise the heterostructure design and growth processes, the misfit dislocation formation, propagation and blocking interactions were studied:

  - The conventional SiGe heterostructures for electron spin qubits normally utilise a 10 nm strained Si on $Si_{0.3}Ge_{0.7}$. According to Matthews-Blakeslee theory, the strained Si on SiGe has a critical thickness of 8.5 nm. This means that the strained Si in conventional SiGe heterostructures for electron qubits exceeds the critical thickness and the pre-existing threading dislocations glide under this condition to form misfit dislocations. These are also observed on the SiGe heterostructures for electron spin qubits grown by CVD in this work. The further investigation shows that when the Si thickness is reduced below the critical thickness, no misfit dislocation forms.

    Based on these results, we suggest reducing the thickness of the Si quantum well layers for qubits to avoid the misfit dislocation formation.

  - Unlike CVD grown samples, the MBE grown strained ^{28}Si layer on a relaxed SiGe substrate is free of misfit dislocations even when it exceeds the critical thickness. The same applies on the MBE grown strained Ge layer. The misfit dislocations in these strained ^{28}Si or Ge layers occur after post-growth annealing. The misfit dislocations get longer, when the annealing temperatures increase and the annealing times remain the same. This means that the misfit dislocation propagation velocities increase with the annealing temperatures. The activation barriers of the propagation are extracted from the Arrehnius-type fitting and agree well with the stress-dependent dislocation kinetics proposed by Dodson and Tsao [153].

    Based on these results, it can be concluded that misfit dislocations in Si, Ge

quantum well layers for qubits can be suppressed kinetically. Nevertheless, the annealing in the post-growth process is risky for the misfit dislocation formation.

Besides the propagation kinetics, it was also noticed that the misfit dislocation blocking interactions occur in the tensile ^{28}Si layer but not in the compressive Ge layer. According to the theoretical calculation, the reason for this difference is that the compressive Ge layer here is so thick that the misfit dislocation propagation can overcome the blocking barrier from the perpendicular misfit dislocations.

All in all, this study not only demonstrates the successful growth of ^{28}SiGe heterostructures for spin qubits and ^{28}SOI, but also investigates the defects, or more precisely, the misfit dislocations in SiGe heterostructures for qubits. These results enable the understanding and further process optimisation of SiGe heterostructures in the eyes of material science.

Outlook

During the study, several more ideas occur beyond the scope of this work. They are listed below, which might inspire future researchers:

- The isotope engineered MBE in this work has been applied for various materials. This means that the chemical impurity and the isotopic impurities can originate from the chamber and accommodate into the epitaxial heterostructures. This can negatively influence the qubits built on these materials. For this reason, transferring the MBE growth into a clean chamber is necessary to achieve high purity.

- In this study, only isotopically enriched ^{28}Si was applied but not isotopically enriched Ge. In SiGe heterostructures for hole spin qubits, the holes are located in the strained Ge layer. Therefore, it makes sense to apply further isotopically enriched Ge except ^{73}Ge in the future work because only ^{73}Ge has nuclear spin among the stable isotopes from Ge.

- This study has been mostly focused on SiGe heterostructures for electron spin qubits, since it has a longer history than SiGe heterostructures for hole spin qubits. The growth of SiGe heterostructures for hole spin qubits was attempted and the

kinetics of the dislocations in this Ge quantum well layer was investigated. However, there are still some process related challenges to be solved and some scientific questions to be answered.

- Related to the process, the surface of the Ge rich SiGe heterostructure probably acts more like Ge. So far, the cleaning of the Ge surface with limited tools, such as ex-situ wet chemical cleaning and in-situ atomic hydrogen irradiation in our lab, is actually still a difficult challenge even among the scientific community. This means, to achieve a relatively clean surface of a relaxed SiGe substrate is one of the first steps to achieve SiGe heterostructures for high performance qubits.

- The conventional strained Ge quantum well layers in SiGe heterostructures for hole spin qubits are around 20 nm, which already exceed the critical thickness. However, holes, here actually heavy holes in Ge, have much lighter effective mass than electrons in Si, this means that to confine the holes, a thicker Ge quantum well layer is needed. Therefore, the path to reduce the Ge quantum well layer thickness to avoid the misfit dislocation formation might not be feasible. It is worth studying how the misfit dislocations influence the performance of the hole spin qubit devices built on the Ge quantum well layers.

- Concerning the SiGe heterostructure for electron spin qubits

  - As we already discussed in subsection 5.2.2, the lower temperature growth can though suppress the misfit dislocation elongation kinetically, but it can also lead to the risk of point defect because of the reduction of surface diffusion velocity of the adatoms. On the other hand, the extremely slow growth rate can extend the time of the surface diffusion of adatoms. At this point, we can summarise the question rising:

    * Is the low-temperature growth the suited one for the SiGe heterostructures for electron spin qubits, in other words, will any point defects generate during the low-temperature growth?

    * If yes, will a low growth rate help to suppress the point defects generation?

  - To solve these questions, the right characterisation method needs to be explored to further inspect the point defects. Possible options can be photoluminescence or using Hall measurement at the two dimensional electron gas formed in the Si quantum well layers.

- In general, to build devices on the ^{28}SiGe heterostructures and ^{28}SOI would be interesting to obtain feedback on these materials.

Although there are several questions left, that is the real life in science, when we solve one question, there are often several more to come. John Green said "What I love about science is that as you learn, you don't really get answers. You just get better questions."

Nevertheless, it is a great honour that I can contribute some of my work to investigate some questions in my thesis and then propose these questions in the end, in order to welcome the bright future of Si, Ge related materials for qubits.

A Acknowledge

Finishing PhD is a long journey. In this journey, I have occured some difficulties but also met many friends.

The ones I need to thank most for my thesis are my supervisors Dr. Kevin-Peter Gradwohl and Dr. Torsten Boeck. Not only I have learned a lot of Kevin but also work with him was joyful. I really appreciate his passion, profession and also patience. I wish him, and I am sure, that he will have a happy and successful career as well as his life. Torsten brings me into this scientific topic, and always supports me not only professionally but also mentally. He has accompanied me not only the good time but also the hard time.

Thanks for Prof. Thomas Schröder. Thomas not only pays my salaries to support my expensive life in Berlin, but also concern and support my career in IKZ and in the future. Thanks for Prof. Matthias Bickermann, Prof. Gang Niu patiently read my thesis and help to bring my promotion into the end. Thanks for Prof. Lehmann to be the chairman of my defence, I am looking forward to meet you.

Dr. Martin Albrecht and Dr. Carsten Richter have tought me much knowledge about the crystallography and characterization. Scientifically, they are quite critical, but I enjoyed a lot of these, even the standard sentences, "it's stupid." from Martin and "I don't believe it." from Carsten.

Chenhsun Lu and Thilo Remmele have help me not only by imaging my numerous samples in electron microscopies, but also accomplish my knowledges by the spontaneous discussions.

Thanks for the techinical and scientific supports from Hans-Peter Schramm and Dr. Thomas Teubner. They are not the talkative people in the institute. But if I asked for

something, they always offer the kindest help for me.

Dr. Nikolay Abrosimov is also one of the people I must say thanks to. He has not only provided the ^{28}Si source materials but also done the internal review work of some papers from me. His work about ^{28}Si opens not only the window for my work, but also many works all over the world.

Thanks for Dr. Jens Martin, Dr. Frank Brunner, Stefan Püschel, Dr. David Uebel and Dr. Owen Ernst to read my thesis and give careful comments. You are the first one to give me the feedbacks. They are quite helpful.

Thanks for Dr. Saud Bin Anooz to measure some samples from me with ellipsometry to get the layer thicknesses. Thanks for Albert Kwasniewski by helping some X-ray measurements.

Special thanks for the colleges Aykut Baki, Daniel Pfützenreuter, Ta-Shun Chou, Setareh Zahedi-Azad and many others in IKZ, with whom, we drink a lot of coffee and some ideas are also from the coffee breaks. I am so glad that most of us have already finished our PhD and some soon. I wish all of you a bright future.

The cooperations with IHP, Siltronic, RWTH Aachen and also MPQ are also great. I am really glad that I got to know these excellent groups and also work with them. They are the MT and PT groups in IHP, epitaxy research group in Siltronic, Dr. Schreiber's group in RWTH Aachen and also Prof. Reiserer's group in MPQ. Especially the discussions with Wolfgang from IHP and Andreas from MPQ help me to go through the hard time of my PhD.

In the end, thanks for my Colin, who have brought me a lot of un-overcooked foods in these years. He has been the private quantum computer teacher as well as the private editor for my thesis. We went through a lot together these years.

Thanks for my parents, even though I haven't met them during my PhD due to the Corona pandemic, your unconditional supports for whatever my decision have given and give me a lot of power beyond physics.

B Declaration

Independence declaration

Hereby, I confirm that I have prepared this thesis independently by myself. All information taken from other sources and being reproduced in this thesis are referenced.

Publication declaration

Parts of the texts and images in the thesis are reproduced from the published papers:

- Yujia Liu, Stephan Rinner, Thilo Remmele, Owen Ernst, Andreas Reiserer, and Torsten Boeck. ^{28}Silicon-on-insulator for optically interfaced quantum emitters. Journal of Crystal Growth, 2022. [1]
  with the permission of Elsevier, all rights reserved
  (https://www.sciencedirect.com/science/article/pii/S0022024822002214);

  My contribution in this publication: the idea initiation, the project management, the sample growth, the AFM measurement, the preparation of TEM sample as well as the image analysis, the manuscript writing for these related part (2, 3.1...3.3).

- Yujia Liu, Kevin-Peter Gradwohl, Chen-Hsun Lu, Thilo Remmele, Yuji Yamamoto, Marvin Hartwig Zoellner, Thomas Schroeder, Torsten Boeck, Houari Amari, Carsten Richter, and Martin Albrecht. Role of critical thickness in SiGe/Si/SiGe heterostructure design for qubits. Journal of Applied Physics, 2022. [2]
  with the permission of AIP Publishing, all rights reserved
  (https://aip.scitation.org/doi/10.1063/5.0101753);

My contribution in this publication: the idea initiation, the project management, the TEM sample preparation and TEM image analysis, the manuscript writing except one part "C. Relationship between misfit and threading dislocation spacing based on geometric considerations" .

- Yujia Liu, Kevin-Peter Gradwohl, Chen-Hsun Lu, Yuji Yamamoto, Thilo Remmele, Cedric Corley-Wiciak, Thomas Teubner, Carsten Richter, Martin Albrecht, and Torsten Boeck. Viewing SiGe Heterostructure for Qubits with Dislocation Theory. ECS Transactions, 2022. [4]
  with the permission of The Electrochemical Society, all rights reserved
  (https://iopscience.iop.org/article/10.1149/10904.0189ecst).

  My contribution in this publication: the idea initiation, the project management, the sample growth TEM sample preparation and TEM image analysis, the XRD measurement and analysis, the ECCI result interpretation, the manuscript writing .

Teamwork declaration

The people having contributions to this work are listed below:

Kevin-Peter Gradwohl: $^{28}Si_{0.3}Ge_{0.7}$/Ge/$^{28}Si_{0.3}Ge_{0.7}$ growth (with Author together)

Chen-Hsun Lu: TEM investigation and ECCI investigation

Thilo Remmele: TEM investigation

Martin Albrecht: TEM investigation

Carsten Richter: XRD investigation (with Author together)

Yuji Yamamoto: CVD growth of $Si_{0.7}Ge_{0.3}$ substrates and $Si_{0.7}Ge_{0.3}$/Si/$Si_{0.7}Ge_{0.3}$ heterostructures in subsection 5.2.1.

Lucas Becker & Peter Storck: CVD growth of $Si_{0.3}Ge_{0.7}$ substrates

SIMS measurements were performed in RTG GmbH and IHP GmbH (managed by Cedric Corley-Wiciak)

March 21, 2023, Berlin

Yujia Liu

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[3] Yujia Liu, Kevin-Peter Gradwohl, Chen-Hsu Lu, Yuji Yamamoto, Thilo Remmele, Cedric Corley-Wiciak, Thomas Teubner, Carsten Richter, Martin Albrecht, and Torsten Boeck. Viewing SiGe Heterostructure for Qubits with Dislocation Theory. *ECS Transactions*.

[4] Yujia Liu, Kevin-Peter Gradwohl, Chen-Hsu Lu, Yuji Yamamoto, Thilo Remmele, Cedric Corley-Wiciak, Thomas Teubner, Carsten Richter, Martin Albrecht, and Torsten Boeck. Growth of 28Si Quantum Well Layers for Qubits by a Hybrid MBE/CVD Technique. *Submitted*, 2022.

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