Novel Methodologies for Efficient and Accurate Modeling and Optimization of System-in-Package Modules for RF/High-Speed Applications

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To

my mother,
Sarah Ako Enow

and

in the loving memory of my maternal grandmother,
Mama Lydia Ebangha Enow.

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Abstract

As consumer demands continuously push for multifunctional, smaller, cheaper and higher performance convergent microelectronic systems with sensing, computing and communications functions, efficient, cost-effective and reliable packaging and integration technologies are needed, so as to meet these demands. Since system-in-package (SiP) technology enables the integration of heterogeneous functions (e.g., RF, high-speed digital processing, memory, sensors, etc.) in a compact package module, thereby simultaneously reducing cost and space, it has emerged as the packaging technology to be used for the design of such systems.

However, as operating frequencies continuously creep up the radio frequency (RF)/microwave band and the complexity of SiP modules steadily increases, it becomes increasingly challenging to properly design these modules to be capable of supporting broadband signals without degrading signal integrity (SI) to unacceptable limits. In this GHz-age, package/board parasitics that have not been considered critical up till now may severely degrade the quality and timing of signals, resulting in system malfunctioning or even failure. To prevent this, novel design measures that account for the parasitic effects of all interconnecting components along complete signal paths in SiP modules at RF/microwave frequencies must be used at the beginning of the design cycle.

In this work, a novel approach, the M3-approach (methodologies->modeling->measures), for optimal, cost-effective and reliable electrical design of SiP modules as well as other complex chip packages and boards for RF and high-speed applications was developed and illustrated using a ball grid array (BGA) package module as an example.

First of all, novel methodologies for efficient and accurate wideband modeling of each package/board component as well as for complete signal paths were developed. Multilumped modeling, which is traditionally used for uniform transmission lines, where only the fundamental mode (e.g., TEM or quasi-TEM) exists, was successfully applied for the first time to develop wideband models for complete signal paths in complex SiP modules, where both the fundamental as well as higher-order modes (HOMs) exist. Since the multilumped modeling technique generally entails a segmentation of the uniform transmission line, separate modeling of each portion and cascading the results to increase bandwidth, the complete signal paths in the SiP module also had to be segmented at points where only the fundamental mode exists. For this purpose, a novel methodology was first developed to define the electrical boundaries of all geometrical discontinuities (e.g., flip chip interconnects, bends on package traces, vias, BGA balls…) along an entire signal path, i.e., the points away from the physical boundaries of each discontinuity where fields of HOMs, excited at the discontinuity vanish or become insignificant (end of discontinuity effect), and the fundamental mode continues unperturbed. Based on these boundaries, the path was then segmented and novel modeling techniques were used to extract wideband models for each segment. For example, a methodology was developed for the first time to efficiently model

bump arrays at RF/microwave frequencies, irrespective of the number of bumps in the array. Furthermore, a hybrid modeling approach was also developed and used for wideband modeling of each interconnecting segment, so as to accurately account for both the fundamental mode as well as HOMs. In order to validate the extracted models, test samples were designed, fabricated and measured. For each segment, a good correlation was obtained between theory and experiment. All the separately extracted and validated models were then cascaded to generate a wideband model that accounts for the parasitic effects of all interconnecting components along complete signal paths. This wideband model was also experimentally validated.

Using these validated wideband models, several SI analyses were performed in the pre-layout stage, so as to track-down potential causes of two of the most dominant SI problems – reflections and cross-talk. Based on the results of these studies, critical components responsible for performance degradation were deduced. Measures to ensure optimal choice, design and placement of these components were then developed. Finally, these measures were used to optimize the RF performance of the entire module for frequencies up to 30 GHz.

Applying the M3-approach developed in this work at the beginning of the design cycle of SiP modules or any other complex chip package/board leads to the elimination of re-design efforts and place/route iterations. Consequently, time-to-market as well as cost is considerably reduced, while performance is optimized.

Keywords: SiP module, BGA package, signal integrity, M3-approach, multilumped modeling, electrical boundaries of discontinuities, end of discontinuity effects, wideband models.

Zusammenfassung

Um den stetig wachsenden Bedarf an multifunktionalen, kleineren, preiswerteren und leistungsfähigeren mikroelektronischen Systemen zu erfüllen, werden effiziente, zuverlässige und kostengünstige Packaging- und Integrationskonzepte benötigt. Da das System-in-Package (SiP) Konzept die Integration heterogener Funktionen (z.B. HF, High-Speed-Digital, Speicher, Sensoren usw.) in einem kompakten Modul, bei gleichzeitiger Reduktion von Kosten und Platzbedarf, ermöglicht, ist es zu einer führenden Packaging-Technologie für neue Entwicklungen geworden.

Aber mit steigenden Taktfrequenzen und der zunehmenden Komplexität von SiP Modulen wird es immer schwieriger, SiP Module erfolgreich zu entwerfen, im Hinblick darauf, dass sie schnelle Signale übertragen können, ohne die Integrität der Signale zu zerstören. Im GHz-Zeitalter verursachen sogar kleine Verbindungskomponenten, entlang eines Signalpfads die bisher als „nicht kritisch“ betrachtet wurden, Signalintegritätsprobleme in SiP Modulen, die dazu führen können, dass das gesamte Sub-System nach dem Aufbau nicht (einwandfrei) funktioniert. Da es immer sehr schwierig und vor allem teuer ist, solche Probleme und ihre Ursachen nach dem Aufbau des Gehäuses zu identifizieren und zu lösen, ist es unbedingt erforderlich, Entwurfsregeln am Anfang der Designphase einzusetzen, die die parasitären Effekte aller Komponenten entlang des vollständigen Signalpfades bei Mikrowellen-Frequenzen berücksichtigen.

In dieser Arbeit wurde ein neuer Ansatz, der M3-Ansatz (Methodiken-> Modelle-> Maßnahmen), entwickelt, um einen optimalen, kostengünstigen und zuverlässigen elektrischen Entwurf von SiP Modulen, sowie von anderen komplexen Chip Gehäusen und PCBs für HF/High-Speed Anwendungen, zu gewährleisten, und Anhand eines Ball Grid Array (BGA) Moduls illustriert.

Zuerst wurden neue Methodiken entwickelt, um akkurate und breitbandige Modelle für vollständige Signalpfade in SiP Modulen entwickeln zu können. Das Verfahren des ‚Multi-Lumped Modeling’, welches bis jetzt nur für gleichförmige Leitungen (bei denen lediglich die TEM/Quasi-TEM Mode vorhanden ist) benutzt wurde, wurde hier zum ersten Mal erfolgreich angewandt, um breitbandige Modelle für vollständige Signalpfade in komplexen SiP Modulen effizient und akkurat zu entwickeln, in denen sowohl TEM/Quasi-TEM als auch höhere Moden vorhanden sind. Da ‚Multi-Lumped-Modeling’ generell eine Segmentierung der Leitung, die Modellierung jedes Segments und schließlich eine Kaskadierung der Modelle zur Erhöhung der Bandbreite erfordert, müssen die Signalpfade in den SiP Modulen an den Orten, wo lediglich die TEM/Quasi-TEM Mode auftritt, segmentiert werden. Daher wurde zuerst eine neue Methodik entwickelt, um die tatsächlichen Endpunkte jeder Diskontinuität (z.B. Flip Chip Verbindungen, Ecken, Vias, BGA Balls...), also den genauen Abstand der elektrischen Grenze einer Diskontinuität, an dem die Felder der höheren Moden, die an der Diskontinuität angeregt werden, verschwinden oder unbedeutend werden (Ende des Diskontinuitätseffekts), zu definieren. Ab dieser Grenze existiert nur noch die TEM/Quasi-

TEM Mode. Basierend auf den Endpunkten der Diskontinuitäten wurden die Signalpfade zerlegt und neue Methoden entwickelt, um breitbandige Modelle für jede Komponente zu extrahieren. Zum Beispiel wurde zum ersten Mal eine Methodik entwickelt, um ein Bumparray – unabhängig von der Anzahl der Bumps in dem Array – zu modellieren. Ferner wurde eine hybride Modellierungsmethodologie für jedes Segment entwickelt, um sowohl die Einflüsse der TEM/Quasi-TEM als auch der höheren Moden zu berücksichtigen. Um die extrahierten Modelle zu validieren, wurden Testaufbauten entwickelt und vermessen. Für jede Komponente wurde eine gute Übereinstimmung zwischen Theorie und Experiment beobachtet. Die validierten Modelle aller Komponenten wurden dann kaskadiert, um ein breitbandiges Modell des vollständigen Signalpfades zu erzeugen. Mit Hilfe eines solchen Modells können die parasitären Effekte aller Komponenten entlang des Pfades erfasst werden. Dieses Model wurde ebenfalls experimentell validiert.

Die validierten Modelle wurden benutzt, um Signalintegritätsanalysen in der „Pre-layout" Phase durchzuführen, um die Ursache von zwei dominanten Signalintegritätsprobleme (Reflexionen und Übersprechen) vor dem Aufbau des Gehäuses identifizieren zu können. Basierend auf den erzielten Ergebnissen wurden kritische Komponenten, die für die Verschlechterung der Systemleistungsfähigkeit verantwortlich sind, definiert. Entwurfsmaßnahmen, die eine optimale Wahl, einen optimalen Entwurf und eine optimale Platzierung dieser Komponenten ermöglichen, wurden abgeleitet. Diese Maßnahmen wurden dann benutzt, um die HF-Leistungsfähigkeit des gesamten Moduls bis 30 GHz zu optimieren.

Der Einsatz des M3-Ansatzes, der in dieser Arbeit entwickelt wurde, am Anfang des Entwicklungsprozesses eines SiP Moduls sowie von anderen komplexen Chip Gehäusen und PCBs, führt zu einem kostengünstigen, zuverlässigen und optimierten Entwurf von SiP Modulen.

Schlagwörter: SiP Module, BGA-Gehäuse, Signalintegrität, M3-Ansatz, Multilumped Modeling, Ende des Diskontinuitätseffekts, Elektrische Grenze einer Diskontinuität, Breitbandige Modelle.

Contents

Chapter 1

Introduction

1.1 Motivation and Goal

Due to the ever increasing demand for multifunctional, smaller, cheaper and higher performance convergent systems with sensing, computing and communication functions, SiP has become a compelling technology to be used for the design of present and next generation microelectronic products. This is mainly because it enables the integration of heterogeneous functions (e.g., RF, high-speed digital processing, memory, sensors, etc.) in a compact package module. Other advantages of this promising packaging technology include the following:

- Low system cost by eliminating multiple packages for individual chips while leveraging the existing packaging and SMT assembly manufacturing infrastructure.
- Small size factor by providing a platform for the integration of active devices, integrated and embedded passives.
- SiP enables the system designer to mix and match integrated circuit (IC) technologies in order to optimize the performance of each functional block.
- Reduced time-to-market.
  - o Changes can be made to the SiP without changing the system board.
  - o Design flexibility and easy redesign.
- The SiP solution reduces the complexity of the motherboard by moving the routing complexity to the package structure [1]-[3].

However, as operating frequencies continuously creep up the RF/microwave band and the complexity of SiP modules steadily increases, it becomes increasingly challenging to properly design these modules to be capable of supporting broadband signals without degrading system performance to unacceptable limits. In this GHz age, parasitic effects (that have not been considered critical up till now) arising from package/board discontinuities e.g., vias and bends

(used to achieve the required integration density by facilitating vertical and horizontal routing), from undesired electromagnetic (EM) coupling (due to the compact placement of package/board components so as to achieve the miniaturization goals) as well as from technological fluctuations (which normally occur during the fabrication process), may severely degrade the quality and timing of signals as they propagate within the module (e.g., from chip to chip or chip to board). Some of the SI problems that may occur include reflections, cross-talk, rise time degradation, over-/undershoot, simultaneous switching noise, signal attenuation, etc. When these problems occur, noise margin requirements may not be satisfied. Diagnosing and solving these problems after the package is developed is very difficult, if not impossible, and extremely expensive. Neglecting them, on the other hand, may lead to a mal-functioning of the entire system or even system failure. Hence, there is a need for novel design measures which take into consideration critical aspects that determine the level of SI maintained within SiP modules at RF/microwave frequencies. These design measures can then be implemented at the pre-layout stage, so as to prevent the occurrence of SI problems after the package is built, thereby saving time and money.

In order to develop these measures, efficient and accurate wideband models for complete signal paths within these packages as well for each package component are needed to perform rigorous SI analyses. Such analyses enable potential SI problems to be identified and eliminated, before they even occur in the actual design.

The main goal of this dissertation, therefore, is to develop a novel approach that enables the extraction of optimal and reliable design measures for SiP modules as well as other complex chip packages and boards for RF and high-speed applications. This entails developing novel modeling methodologies that lead to the extraction of accurate wideband models for complete signal paths, experimentally validating these models, using the validated models to perform SI analysis and finally, based on the extracted results, deduce optimal and reliable design measures.

A cross-sectional view of an SiP module, illustrating signal transmission paths from chip to chip and chip to board is shown in Figure 1. 1.

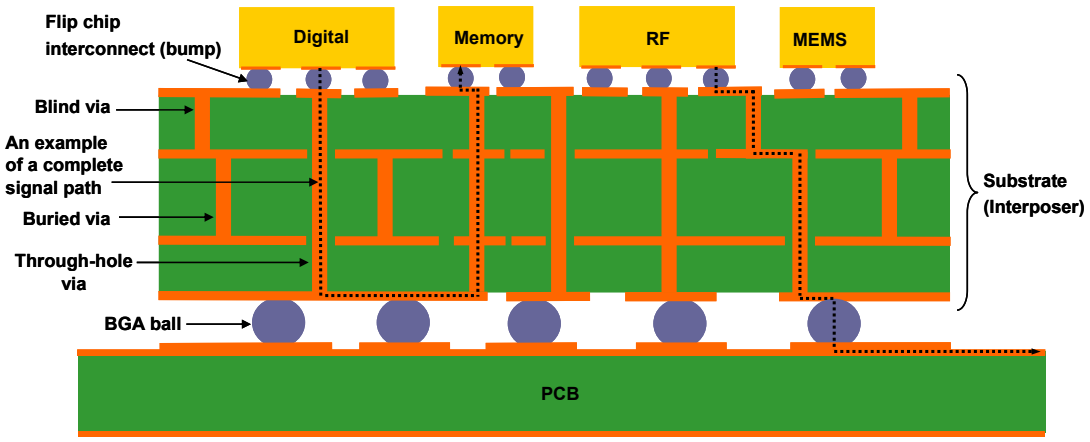

Figure 1. 1: Cross-sectional view of an SiP module, illustrating complete signal paths.

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Chapter 2

State-of-the-Art in Modeling of System-in-Package Modules

2.1 Modeling of Complete Signal Paths

In order to illustrate the conventional approaches that have been used up-to-date to model complete signal paths in SiP modules as well as other complex chip packages and boards, a BGA package module will be considered as an example.

Conventional BGA package models are extracted using either analytical, numerical or measurement techniques. For example, using a set of analytical formulas based on static approximations of Maxwell's equations, computer programs that generate a simple model of the package parasitics were developed in [4] and [5]. Although such programs are believed to speed up the modeling process by eliminating much of the complexity involved with 3D EM field solvers, they are not capable of accounting for frequency-dependent parasitic effects that occur in geometrically complex structures like SiP modules, especially at RF/microwave frequencies. To account for these effects, 3D full-wave EM field computations which involve the use of numerical techniques (e.g., the finite element method) to solve the wave equation without invoking any static/quasi-static approximations were used in some publications (e.g., in [7]). However, in these works complete signal paths within these modules were modeled by uniting all interconnecting components along the paths and considering them as a single component. Such an approach, similar to the extraction of package parasitics through RF measurements of the entire package, as was done in, for example [8] to [15], prevents a comprehensive understanding of the parasitic effects contributed by each interconnecting component. Consequently, a systematic optimization of the package performance can not be carried out. Furthermore, the bandwidths of the extracted fixed-value single lumped element models are very small, because they are valid only up to a frequency where the length of the signal path is smaller than approximately $1/10^{th}$ of the wavelength of the propagating signal. Above such frequencies, the lumped approximation breaks down. To overcome these limitations, the complete path must be properly segmented and each interconnecting component separately modeled. However, up to date, no method has been proposed in any published literature to segment complete signal paths in these modules. In [16] - [18], for example, the need for a physical segmentation of complete paths was

clearly mentioned, but neither was any method proposed to segment these paths nor was a model developed for the paths. In other contributions (e.g., [19]-[26]), only one or a few interconnecting components along these paths were selected and modeled while the rest were neglected. Consequently, using the extracted models, SI problems caused by all interconnecting components along a complete signal transmission path cannot be tracked down.

As can be seen from the above analysis, despite the huge efforts dedicated to modeling of complete signal paths in SiP modules and other complex chip packages and boards, there is still a pressing need for a method that will lead to the development of wideband models which account for the parasitic effects of all interconnecting components along complete signal paths at RF/microwave frequencies. One of the goals of this dissertation is to meet this need.

2.2 Modeling of Interconnecting Components

To enable optimal solutions to be chosen for each interconnecting component, an in-depth analysis of these components must be carried out separately.

2.2.1 Chip-to-Package Interconnections

The three most commonly used methods for interconnecting chips and packages or boards are wire bonding, tape-automated bonding and flip chip interconnects (or bumps). Among these methods, bumps provide the shortest possible leads, lowest inductance, highest frequency, best noise control, highest density, greatest number of I/Os, smallest device footprints and lowest profile [27].

To increase the signal density as well as to reduce the entire package size, these bumps are designed in arrays. However, due to the close proximity of bumps in these arrays, an interaction of their EM fields leads to cross-talk and other signal degrading effects, which may degrade the performance of the entire package, especially at RF/microwave frequencies. To prevent system failure, these effects must be well investigated and compensated for, at the beginning of the design process. In order to achieve this goal, accurate wideband models for bump arrays are needed.

Within the last two decades, much effort has been dedicated to R&D of flip chip interconnects for RF/high-speed applications. For example, in [28]–[41], a variety of time and frequency-domain numerical techniques were employed to study the effects of design parameters such as bump height, bump diameter, geometry of the feeding lines and the material properties of the underfill, which determine the electrical performance of these transitions. However, although all the field computation techniques used in these works unravel the RF/microwave properties of the bumps and their surroundings, they fail to provide a direct relationship between critical electrical parameters of a bump (e.g., its inductance) and its geometry – information needed for the development of realistic circuit models to be used for SPICE simulations. Equivalent circuit models of bumps are more important (than S-parameters extracted from the field

computations) in understanding and predicting the electrical behavior of the flip chip assembly, and for design rule development. Consequently, based on the field computation results of flip chip interconnects, their equivalent circuit models were extracted, for example in [42]-[45]. Using a combination of EM field computation results, circuit models and RF measurements, statistical methods were used in [46] for the development of parameterized models for flip chip interconnects. Since these models relate the geometrical and electrical parameters of the interconnects using simple mathematical functions, they can be used to tune the needed parameters so as to achieve optimal electrical performance of flip chip interconnects. Other methods that have been applied for optimizing the performance of flip chip transitions involve using staggered bumps and compensation networks realized through high and low impedance sections of the feeding lines (e.g., in [47]-[51]).

However, in all these publications, the focus has been only on the development of techniques for understanding and enhancing the RF/microwave performance of single bumps. No method has been proposed to develop electrical models for bump arrays. One of the objectives of this work is to develop a methodology for modeling and analyzing bump arrays at RF/microwave frequencies.

2.2.2 Package/Board Components

As stated in section 1.1, geometrical discontinuities such as vias and bends are very important package/board components used to increase the integration density of SiP modules. Since these discontinuities distort the EM field pattern on uniform traces resulting in SI problems, their effects must also be well investigated and compensated for, at the beginning of the design cycle. To reach this goal, thorough RF/microwave modeling and measurement of realistic configurations of these components is required. However, efficient modeling or measurement of any geometrical discontinuity at RF/microwave frequencies can only be guaranteed, if its electrical boundaries can be accurately defined, i.e., if the points away from a discontinuity where the higher-order modes (HOMs) excited at the discontinuity vanish or become insignificant, are known.

For more than half a century now, planar geometrical discontinuities have been rigorously studied in many R&D institutions around the world. In 1955, A. A. Oliner [52] derived some analytical expressions to determine the equivalent circuit parameters of various discontinuities in a balanced strip transmission line. Since then, other researchers have used a variety of techniques to evaluate the change in capacitance (arising from the altered electric field distribution) and inductance (due to the changed magnetic field distribution) in the vicinity of discontinuities. For example, in [53]-[64], quasi-static methods were used for the extraction of the static capacitances and low-frequency inductances of vias and bends, respectively. These extracted parameters can be used to develop equivalent circuit models for these discontinuities, so as to better understand their impact on signal behavior. However, at higher frequencies, quasi-static approaches suffer significant errors because they fail to account for the interaction of the stored electric and magnetic energies in the vicinity of the discontinuity.

To account for these limitations, the wave equation must be completely solved subject to the appropriate boundary conditions, without invoking any quasi-static assumptions. This was done using full-wave techniques in, for example, [65]-[71], leading to frequency-dependent characteristics of these discontinuities. Unfortunately, the boundaries of the discontinuities were not defined in any of these publications. This implies that the degree of EM field distortion in the vicinity of the discontinuity has been estimated so far by guess work, because the distance away from the physical limits of the discontinuity where the HOMs reach wasn't defined. Therefore, the length of the line interconnecting the discontinuity and the port was also chosen through guess work, which can lead to erroneous results. This also applies to cases where measurement techniques were used for the characterization of geometrical discontinuities (e.g., [72] and [73]). In [74] – [79], the frequency-dependent characteristics of discontinuities were also extracted using planar waveguide models. But here too, the boundaries of discontinuities were not defined. In all of the above mentioned works, it was assumed that the electrical boundaries are the same as the physical boundaries of the discontinuities.

Coupled with the fact that no method has been proposed in any published literature to define the electrical boundaries of any geometrical discontinuity, most of the contributions made so far also fail to provide design guidelines that can be used for the development of realistic substrates and boards in SiP modules and other complex chip packages and boards. For example, in [80] – [86], a signal via is considered as an "island" and the capacitances and inductances associated with the via are extracted under the assumption that there is no other via in the vicinity of the signal via. In other cases (e.g., [87] and [88]), even the interconnecting traces are neglected while computing the parasitic capacitances and inductances of the signal via. Predicting the performance of a signal via based on such assumptions can be misleading, because the effects of other components found in the immediate vicinity of the via (e.g., ground or interplane vias, decoupling capacitors, etc. used for returning current) determines the electrical characteristics of the via and hence, play a very important role in determining its actual transmission behavior, especially at RF/microwave frequencies.

One of the objectives of this work is to develop a methodology for defining the electrical boundaries of discontinuities, so as to accurately account for their parasitic effects.

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Chapter 3

Development of Novel Methodologies for Efficient and Accurate Modeling and Optimization of System-in-Package Modules at RF/Microwave Frequencies

3.1 Methodology for Efficient and Accurate Wideband Modeling of Complete Signal Paths and all Interconnecting Segments

In this section, a methodology developed for the extraction of enhanced (wideband) models for complete signal paths as well as all interconnecting segments in SiP modules and other complex chip packages and boards at RF/microwave frequencies will be presented. These wideband models exceed the frequency range of fixed-value single lumped element models that have been used up-to-date for these modules. The wideband modeling technique that will be used in this work is called multilumped modeling.

So far, multilumped modeling has been applied only to uniform transmission lines where only the fundamental mode of propagation e.g., transverse electromagnetic (TEM) or quasi-TEM, is present throughout the line. If such a uniform transmission line is, for example, two times too long for a lumped model, then using the multilumped modeling approach, the line will simply be segmented into two halves and each of the portions will be separately modeled. Because each section is half the length of the original, the bandwidth is doubled. This process can be extended to provide the needed bandwidth for an interconnect of any length [89].

However, SiP modules are very complex 3D structures, consisting almost entirely of geometrical discontinuities that excite higher-order modes (HOMs). So, unlike in uniform transmission lines where only a single wave mode exists, there is a combination of fundamental and an infinite number of HOMs in SiP modules. Consequently, multilumped modeling can not be applied directly.

To be able to apply multilumped modeling for wideband modeling of SiP modules, the following methodology is needed:

- The electrical boundaries of all discontinuities along the entire signal path must first be defined. Discontinuity is used in this work to describe any package/board component that

distorts the EM field pattern on uniform transmission lines, e.g., flip chip interconnects, wirebonds, vias, bends on package/board traces, BGA balls, etc.

- After defining the boundaries of each discontinuity, the entire signal path can then be partitioned into interconnecting segments, just like a uniform transmission line. A segment is used in this dissertation to describe a geometrical discontinuity (e.g., a via) together with its uniform interconnecting traces, long enough to allow the fields of HOMs excited at the discontinuity to vanish or be considered insignificant.

- Based on the segmentation, thorough EM modeling of each segment must be carried out, taking into consideration EM coupling between neighboring signal paths. A hybrid modeling technique has to be used to develop wideband models for each package/board segment, i.e., distributed models to characterize (quasi) TEM modes on uniform traces and lumped element models to account for the evanescent energy associated with the HOMs in the vicinity of each discontinuity along the path. Since the chip-to-package as well as package-to-board interconnections are mostly designed in arrays (so as to reduce package size and increase signal density), a methodology for the development of wideband models for these arrays must also be developed.

- The extracted models must be experimentally validated, because they are based on numerical electromagnetics. For this purpose, test structures have to be designed, fabricated and measured within the frequency range of interest. The models, as well as the hybrid modeling technique, are said to be validated only if there is a good correlation between theory and measurement.

- After validation, these models can then be cascaded to generate a wideband model that accounts for parasitic contribution of each interconnecting package/board component along complete signal paths in the SiP module.

- Finally, such a wideband model for complete signal paths must also be experimentally validated by designing and measuring a test module.

This methodology is summarized in Figure 3. 1. An elaborate discussion will be presented in the following sections.

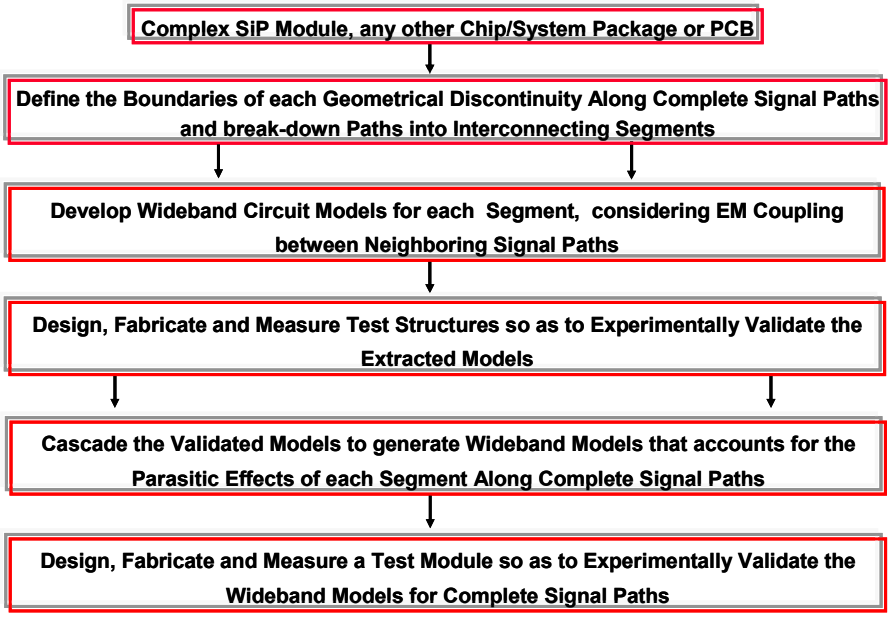

Figure 3. 1: Methodology for the development of wideband models for complete signal paths in complex SiP modules as well as any other chip/system package or multilayered PCB.

3.1.1 Defining the Electrical Boundaries of Discontinuities

3.1.1.1 Electromagnetic (EM) Field Behavior at a Discontinuity

Before proposing a methodology for defining the electrical boundaries of geometrical discontinuities, let's first take a closer look at what exactly happens at a discontinuity.

Consider a signal excited at port 1, and propagating in a TEM or quasi-TEM mode along a package/board trace with a discontinuity (e.g., a 90° bend in this case), towards port 2 as shown in Figure 3. 2. As long as the cross section seen by the signal at any point in time is the same as the cross-section for which the TEM or quasi-TEM mode was defined at port 1, the signal continues propagating and/or attenuating in the longitudinal direction without any change in the transverse direction.

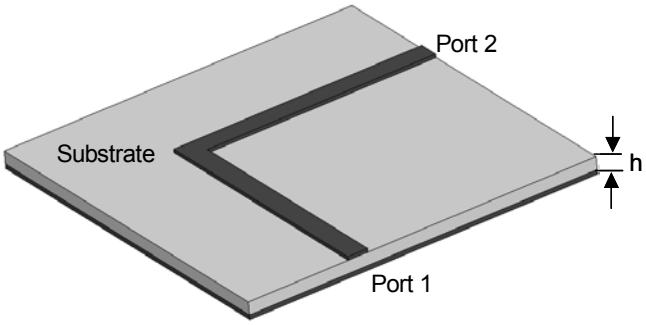

Figure 3. 2: A micostrip package/board trace with a 90° bend (h=substrate thickness).

However, when the signal meets a discontinuity a scattered field is excited, such that the total field, consisting of the original incident and the scattered field, matches all the necessary

boundary conditions. In the vicinity of the discontinuity, the scattered field decomposes into various modes of the interconnecting traces. One of these modes is the fundamental mode (i.e., TEM or quasi-TEM, depending on the configuration of the line) and the others are HOMs. Since the cutoff frequency of the fundamental mode is zero, the scattered TEM or quasi-TEM mode will be propagating. When viewed from port 1, it is considered as a wave reflected by the discontinuity. The excited HOMs can only be propagating if the operating frequency is higher than the cut-off frequency of the lowest-order (Lo-) HOM. Below this frequency, all HOMs are evanescent or non-propagating. In this case, the fields of the HOMs will decay exponentially with distance away from the discontinuity, and at a sufficient distance, they will vanish, leaving the fundamental mode unperturbed. Points away from the discontinuity, from which mainly the fundamental mode is present, define the end of the discontinuity effect and will be termed electrical boundaries of discontinuities in this work.

3.1.1.2 Some Reasons for Defining the Electrical Boundaries of Discontinuities

In the following paragraphs, some of the reasons for the need to accurately defining the boundaries of discontinuities will be outlined.

- In order to prevent or track-down and solve SI problems in electronic packages and boards, accurate wideband models for complete signal paths within these subsystems are needed. As briefly explained at the beginning of this chapter, the development of such models involves the use of multilumped modeling, whereby the signal paths are segmented, followed by an extraction of lumped models for each segment and then cascading the resulting models to increase bandwidth. However, since electronic packages and boards consist almost entirely of discontinuities, this segmentation can only be done at points away from each discontinuity where fields of HOMs have vanished or are considered insignificant and mainly the TEM mode is present. This is mainly because lumped/distributed element modeling is based on TEM wave theory. As will be illustrated in the next chapter, without defining the electrical boundaries of these discontinuities, a conventional circuit-theory-based analysis fails to accurately capture the effects of a discontinuity. Consequently, defining the electrical boundaries of each package/board discontinuity is a pre-requisite for efficient and accurate wideband modeling and analysis of complete signal paths in electronic packages and boards for RF/high-speed applications.

- Secondly, to perform 3D full-wave EM field computations of discontinuities using conventional field solvers, they are connected to ports using uniform transmission lines (e.g., microstrip, stripline...), which represent the actual configuration of traces in the package or board. The length of the transmission line used for this interconnection depends on the electrical boundaries of the discontinuity under consideration, and it determines the accuracy, duration and memory requirements of the field computation. If the transmission line is too short, then HOMs excited at the discontinuity will be captured at the ports. This will lead to erroneous results. If the transmission line is longer than required, then the field computation

time and memory required will increase, leading either to unsuccessful computations due to insufficient memory or computations that may run for days, instead of just a few hours.

- Lastly, in designing test structures for the characterization (through RF measurements) of geometrical discontinuities in chip packages and boards, appropriate lengths of transmission lines are also needed to interconnect the device under test and adapters on which the probes are contacted. If these lines are too long, then the overall size of the test board will increase, leading to more cost. Further more, the measurement results will be more prone to errors, because longer lines are more sensitive to technological tolerances that occur during the fabrication process, especially at RF/microwave frequencies. On the other hand, if the lines are too short, then HOMs excited at the discontinuity will be captured at the ports of the vector network analyzer, leading to erroneous results. The most appropriate length of line required to minimize cost, while simultaneously ensuring efficient and accurate RF/microwave characterization depends on the electrical boundaries of the discontinuity under consideration.

3.1.1.3 Methodology for Defining the Electrical Boundaries of Discontinuities

In order to define the points away from the physical boundaries of a discontinuity where the fields of HOMs vanish, hence the electrical boundaries of the discontinuity, the following methodology was used: First of all, the cut-off frequency of Lo-HOM that is excited on the interconnecting traces was computed, to make sure that the HOMs are not propagating. This was then followed by a computation of the attenuation constant, α, of this Lo HOM. Using α, the range of existence of fields of the excited HOMs (from the point of excitation away, towards the end of the trace) was deduced. Since the end of the discontinuity effect marks an end of the disturbance of the fundamental mode by the HOMs, the effect of the excited HOMs on the fundamental mode was studied with the aid of a 3D full-wave solver, taking into consideration the range of existence of the fields of HOMs computed from α. From the field computation results, the variation of power propagated by the fundamental mode was critically studied using the Poynting theorem. It was deduced, that in the immediate vicinity of the discontinuity where the fields of the evanescent modes are still too large, the imaginary part of the Poynting theorem is also very large. But, it decays exponentially with distance away from the discontinuity since these fields also decay exponentially. The end of the discontinuity effect is marked by a small and approximately constant value of this imaginary part and the field distribution on the trace then resembles that of a uniform transmission line. This variation in power was also seen in the extracted S-parameters, since these S-parameters were derived from power. As the end of the discontinuity effect approached, the magnitude of the reflection coefficient of the S-parameter, computed at a single frequency point when only the fundamental mode is excited, remain approximately constant.
In the following subsections, an elaborate discussion of this methodology will be presented.

I. 2D EM Field Analysis of the Interconnecting Traces

As mentioned in the section 3.1.1.1, the scattered field excited at the discontinuity decomposes into the fundamental and HOMs of the interconnecting traces. Therefore, to be able to define how far these HOMs can go away from the point of excitation (i.e., from the position of discontinuity), it is of vital importance to first of all analyze only the uniform interconnecting traces, so as to be able to know when the HOMs they support become propagating, and how they attenuate along the trace. This analysis involves determining the cut-off frequency of the Lo-HOM, computing its attenuation constant as well as the range of existence of its fields necessary for carrying out the 3D EM field computation necessary for defining the electrical boundaries of discontinuities.

1. Computation of the Cutoff Frequency of Lo-HOM

In order to determine the cutoff frequency of HOMs, Maxwell's equations have to be completely solved. However, due to the complicated field structure in most planar transmission lines, it is generally not possible to obtain analytical solutions of Maxwell's equations for these structures, in which the total effects of all modes are taken into consideration. So, numerical techniques are always applied. But, in order to understand and predict the behavior of these HOMs, analytical solutions are needed. For this reason, planar transmission lines are approximated using waveguides, because analytical solutions of Maxwell's equations for these waveguides are feasible. One of the most important waveguide used for such analysis is the parallel plate waveguide (PPWG) since it can be used to approximate the behavior of many planar transmission lines. For example, a PPWG is used to model the propagation of HOMs in striplines [90]. Furthermore, a microstrip line can be approximated by a section of a PPWG, neglecting fringing, and the relationship between HOMs and the quasi-TEM mode in a microstrip line is analogous to the relationship of transverse electric (TE) and transverse magnetic (TM) modes to the TEM mode in a PPWG [91]. Therefore, a PPWG will be used in the following paragraphs to illustrate the derivation of fields of HOMs in planar traces used in SiP modules, their cutoff frequency as well as the dependency of the cutoff frequency on the cross-section of the interconnecting traces.

Figure 3. 3 shows the geometry of a PPWG.

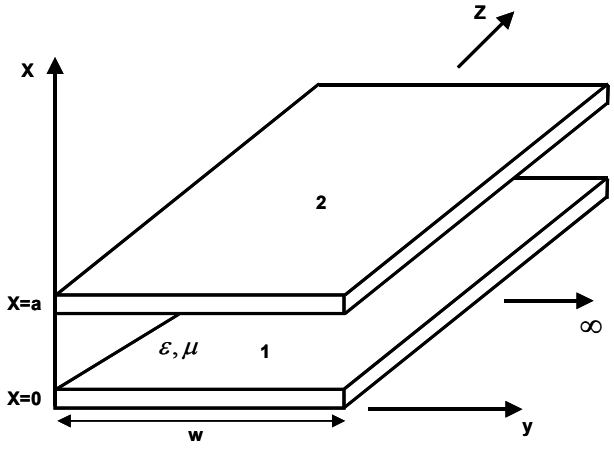

Figure 3. 3: Geometry of a PPWG.

The two perfectly conducting plates, designated as 1&2, lie in the y-z plane and are located at $x = 0$ and $x = a$. The field in the space between these planes is characterized by ε and μ, and is assumed to be homogenous (since $w \gg a$). In order to obtain the complete solutions for these fields, the following procedure is necessary. Determination of:

- Field components of the propagating waves in a given direction.
- Field components of the various modes that can be supported and their propagation constants.
- Cutoff frequency of these modes.

Determination of Field Components of the Propagating Waves

In order to determine these field components, Maxwell's as well as the wave equations must first be expanded.

Maxwell's equations for sinusoidal excitations are given by (3.1) and (3.2).

$$\nabla \times \vec{E} = -j\omega\mu\vec{H} \tag{3.1}$$

$$\nabla \times \vec{H} = j\omega\varepsilon\vec{E} \tag{3.2}$$

Expanding these equations and noting that $\partial/\partial y = 0$ (since the plates are assumed to be infinite in the y-direction) gives the following:

$$\frac{\partial E_y}{\partial z} = j\omega\mu H_x \tag{3.3}$$

$$\frac{\partial E_x}{\partial z} - \frac{\partial E_z}{\partial x} = -j\omega\mu H_y \tag{3.4}$$

$$\frac{\partial E_y}{\partial x} = -j\omega\mu H_z \tag{3.5}$$

$$\frac{\partial H_y}{\partial z} = -j\omega\varepsilon E_x \tag{3.6}$$

$$\frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x} = j\omega\varepsilon E_y \tag{3.7}$$

$$\frac{\partial H_y}{\partial x} = j\omega\varepsilon E_z \tag{3.8}$$

Expanding the wave equation, given by (3.9) and (3.10), under the same condition as (3.1) and (3.2), yields (3.11) and (3.12).

$$\nabla^2 \vec{E} + \omega^2 \mu\varepsilon \vec{E} = 0 \tag{3.9}$$

$$\nabla^2 \vec{H} + \omega^2 \mu\varepsilon \vec{H} = 0 \tag{3.10}$$

$$\frac{\partial^2 \vec{E}}{\partial x^2} + \frac{\partial^2 \vec{E}}{\partial z^2} + \omega^2 \mu\varepsilon \vec{E} = 0 \tag{3.11}$$

$$\frac{\partial^2 \vec{H}}{\partial x^2} + \frac{\partial^2 \vec{H}}{\partial z^2} + \omega^2 \mu\varepsilon \vec{H} = 0 \tag{3.12}$$

Now, assume propagation to be in the z-direction such that

$$\vec{E}(x, y, z) = \vec{E'}(x, y) e^{-\gamma z} \ , \tag{3.13}$$

where γ is the propagation constant (to be determined). Substituting this into (3.3)-(3.8) as well as in (3.11) and (3.12) yields

$$\gamma E_y' = -j\omega\mu H_x' \tag{3.14}$$

$$-\gamma E_x' - \frac{\partial E_z'}{\partial x} = -j\omega\mu H_y' \tag{3.15}$$

$$\frac{\partial E_y'}{\partial x} = -j\omega\mu H_z' \tag{3.16}$$

$$\gamma H_y' = j\omega\varepsilon E_x' \tag{3.17}$$

$$-\gamma H_x' - \frac{\partial H_z'}{\partial x} = -j\omega\mu E_y' \tag{3.18}$$

$$\frac{\partial H_y'}{\partial x} = j\omega\varepsilon E_z' \tag{3.19}$$

and

$$\frac{\partial^2 \vec{E'}}{\partial x^2} + \left(\gamma^2 + \omega^2 \mu\varepsilon\right) \vec{E'} = 0 \tag{3.20}$$

$$\frac{\partial^2 \overrightarrow{H'}}{\partial x^2} + \left(\gamma^2 + \omega^2 \mu\varepsilon\right)\overrightarrow{H'} = 0 \tag{3.21}$$

From the foregoing equations, it will now be solved for E_x, H_x, E_y and H_y in terms of E_z and H_z, since propagation was assumed to be in the z-direction. This is be done by simply manipulating (3.14) to (3.19), as shown in the example below.

From (3.14),

$$E_y' = -j\frac{\omega\mu}{\gamma}H_x \tag{3.22}$$

and from (3.18)

$$H_x' = -j\frac{\omega\varepsilon}{\gamma}E_y' - \frac{1}{\gamma}\frac{\partial H_z'}{\partial x} \tag{3.23}$$

Substituting (3.23) in (3.22) yields

$$E_y' = \frac{j\omega\mu}{h^2}\frac{\partial H_z'}{\partial x} \tag{3.24}$$

Similarly, by combining other relations, the remaining field components can be found.

$$H_y' = -\frac{j\omega\varepsilon}{h^2}\frac{\partial E_z'}{\partial x} \tag{3.25}$$

$$E_x' = -\frac{\gamma}{h^2}\frac{\partial E_z'}{\partial x} \tag{3.26}$$

$$H_x' = -\frac{\gamma}{h^2}\frac{\partial H_z'}{\partial x} \tag{3.27}$$

where

$$h^2 = \gamma^2 + \omega^2\mu\varepsilon \tag{3.28}$$

(3.24) – (3.27) give the field components for waves propagating in the z-direction. These field components are functions of only x because of the following reasons:

- There can be no variation in the y-direction due to the assumption that the plates are infinite in the y-direction
- Propagation was assumed to be in the z-direction.

Hence, the partial derivatives in (3.14) - (3.27) can be replaced by ordinary derivatives.

Determination of Field Components of the various Modes that can be Supported and their Propagation Constant

The **TE mode (also referred to as the H-waves)** assumes that the electric field is confined in the x-y plane, so that $E_z = 0$. Implementing this condition in (3.24)-(3.27) leads to the disappearance of $E_x^{'}$ and $H_y^{'}$ (since they are functions of E_z), and the wave equation in (3.20) then reduces to

$$\frac{d^2 E_y^{'}}{dx^2} + h^2 E_y^{'} = 0 \ , \tag{3.29}$$

whose general solution is

$$E_y^{'} = A\sin(hx) + B\cos(hx). \tag{3.30}$$

The boundary conditions are that the electric field tangential to the surfaces of the plates is zero.

$$\Rightarrow E_y = 0\,|_{x=0, x=a} \tag{3.31}$$

Setting $E_y = 0$ at $x = 0$ in (3.30) leads to $B = 0$.

$E_y = 0$ at $x = a$ results in $A\sin(ha) = 0$. This condition requires that:

Either

$A = 0$, in which case nothing is left,

or

$\sin(ha) = 0$, which is satisfied by the condition

$ha = m\pi$

for $m = 0, 1, 2, 3...$

Thus, the solution for E_y which satisfies the boundary condition is

$$E_y = A\sin\left(\frac{m\pi x}{a}\right)e^{-\gamma z} \quad . \tag{3.32}$$

Substituting (3.32) in (3.14) and (3.16) yields the other field components of the TE mode.

From (3.14)

$$H_x = \frac{\gamma}{-j\omega\mu}E_y = j\frac{\gamma}{\omega\mu}E_y$$

$$\Rightarrow H_x = j\frac{\gamma}{\omega\mu}A\sin\left(\frac{m\pi x}{a}\right)e^{-\gamma z} \tag{3.33}$$

and from (3.16)

$$H_z = \frac{1}{-j\omega\mu}\frac{\partial E_y}{\partial x} = j\frac{1}{\omega\mu}\frac{\partial E_y}{\partial x}$$

$$\Rightarrow H_z = j\frac{m\pi}{\omega\mu a}\cos\left(\frac{m\pi x}{a}\right)e^{-\gamma z} \tag{3.34}$$

From (3.32)-(3.34), it can be seen that there is an infinite number of solutions (modes) for the various integral values of m, each with a different field distribution.

From (3.28), the propagation constant becomes

$$\gamma^2 = h^2 - \omega^2\mu\varepsilon$$

$$\Rightarrow \gamma = \sqrt{h^2 - \omega^2\mu\varepsilon}$$

but since $h = \frac{m\pi}{a}$

$$\Rightarrow \gamma = \sqrt{\left(\frac{m\pi}{a}\right)^2 - \omega^2\mu\varepsilon} \tag{3.35}$$

For the lowest-order mode, i.e., $m = 0$, all field components of the TE mode vanish. This can be seen by setting $m = 0$ in (3.32)-(3.34). So, there is no TE_0 mode. It implies the Lo-HOM in this case is TE_1. Its cutoff frequency will be given in the next sub-section.

The **TM mode (also referred to as the E-waves)** has the magnetic field confined to the transverse x-y plane, so that $H_z = 0$. Carrying out the same development as in the previous section gives the non-zero field components of the TM mode as:

$$H_y = C\cos\left(\frac{n\pi x}{a}\right)e^{-\gamma z} \tag{3.36}$$

$$E_x = -j\frac{\gamma}{\omega\varepsilon}C\cos\left(\frac{n\pi x}{a}\right)e^{-\gamma z} \tag{3.37}$$

$$E_z = j\frac{h}{\omega\varepsilon}C\sin\left(\frac{n\pi x}{a}\right)e^{-\gamma z} \tag{3.38}$$

where $n = 0,1,2...$

The propagation constant is also given by (3.35) with m replaced by n.

In contrast to the TM mode, there exist a TM_0 mode for $n = 0$, because substituting $n = 0,1,2...$ in (3.36) – (3.38) leads to the disappearance of only E_z, but not E_x and H_y. In this case, the propagation constant and the field vectors reduce to

$$\begin{aligned}\gamma &= j\omega\sqrt{\mu\varepsilon} \\ &= j\beta\end{aligned} \tag{3.39}$$

$$H_y = Ce^{-j\beta z} \tag{3.40}$$

$$\begin{aligned}E_x &= -j\frac{\gamma}{\omega\varepsilon}Ce^{-j\beta z} \\ &= \sqrt{\frac{\mu}{\varepsilon}}Ce^{-j\beta z}\end{aligned} \tag{3.41}$$

$$E_z = 0 \tag{3.42}$$

However, this is the TEM mode. Therefore the TM_0 mode is equivalent to the TEM mode. It implies the Lo-HOM in this case is the TM_1 mode. Its cutoff frequency will also be given in the next sub-section.

Determination of the Cutoff Frequency

For the Lo-HOMs and other HOMs to be able to propagate, the propagation constant must be imaginary, such as $\gamma = j\beta_z$ (or at least have a non-zero imaginary part) such that when the phasor form in (3.13) is converted to the time domain by multiplying by $e^{j\omega t}$ and taking the

real part, then $\cos(\omega t - \beta_z z)$ will be obtained, which clearly represents propagation in the z-direction. From (3.35), this would mean

$$\omega^2 \mu\varepsilon \geq h^2$$

$$\Rightarrow \omega \geq \frac{1}{\sqrt{\mu\varepsilon}} \frac{n\pi}{a} \tag{3.43}$$

The cutoff frequency can then be obtained from (3.43) as

$$f_{TE_n, TM_n} = \frac{n}{2a\sqrt{\mu\varepsilon}} \tag{3.44}$$

where n designates the order of the mode. Therefore, for the Lo-HOM (TE_1 and TM_1), n will be replaced by 1 and the cutoff frequency will then be given as:

$$\begin{aligned} f_{TE_1, TM_1} &= \frac{1}{2a\sqrt{\mu\varepsilon}} \\ &= \frac{v}{2a} \end{aligned} \tag{3.45}$$

From (3.44), it can be seen that the second Lo-HOM (e.g., TM_2) has a cutoff frequency equal to twice the value of TM_1, TM_3 has a cutoff frequency three times that of TM_1, and so on. This explains why it is sufficient to determine only the cutoff frequency of the Lo-HOM, when defining the electrical boundaries of discontinuities. If these modes are not propagating, then other HOMs can not also propagate.

Since *a* represents the substrate thickness, it can be deduced from (3.45) that the Lo-HOM can only propagate if this thickness is greater than, or equal to half the wavelength of the propagating signal. This indicates that for SiP modules used for RF/high-speed applications with very thin dielectric substrates, HOMs can not propagate. Once excited, they will always decay exponentially with distance away from the point of excitation.

However, it must be noted that since the PPWG neglects the fringing fields that occur in planar transmission lines, the equation for the determination of the cutoff frequency for HOMs given in (3.44) must be regarded as a rough approximation when applied to planar lines. A much better, though still approximate formula, for the computation of the cutoff frequency of the microstrip lines which take into consideration the effective width that results from fringing fields, is given as [92]

$$f_{g, HOM_m} = \frac{c_0 m}{2w_{eff}\sqrt{\varepsilon_{r\_eff}}} \tag{3.46}$$

where c_0 is the speed of light, m designates the order of the mode, ε_{r_eff} is the effective relative dielectric constant and w_{eff} is the effective width of the conductor which includes the scattered edge fields. w_{eff} is given by

$$w_{eff} = \frac{\eta_0 h}{Z_L \sqrt{\varepsilon_{r\_eff}}} = \frac{\eta_0 h}{Z_{L0}} \tag{3.47}$$

where $\eta_0 (\approx 120\pi\,\Omega)$ is the intrinsic impedance of free space, h is the substrate thickness, $Z_{L0} = Z_L\left(\varepsilon_r = 1\right)$ is the characteristics impedance of a transmission line in free space.
Substituting (3.47) into (3.46) results in the following relationship for the cutoff frequency:

$$f_{g,HOM_m} = \frac{Z_L c_0 m}{2\eta_0 h},$$

where $Z_L = \frac{Z_{L0}}{\sqrt{\varepsilon_{r\_eff}}}$.
However, for a more accurate computation of the cutoff frequency of any planar transmission line, an EM field solver that takes into consideration the fringing fields, the non-ideal properties of the conductor as well as the substrate must be used.

2. Computation of the Attenuation Constant of Lo-HOM and Definition of the Range of Existence of its Fields Necessary for 3D EM Field Analysis

As illustrated in the previous section, the HOMs excited by discontinuities in SiP packages and other chip and system packages as well as multi-layered boards can not propagate. In these cases, γ is almost entirely "real", with a negligible β-component. Thus, from (3.35),

$$\gamma \approx \alpha = \sqrt{\left(\frac{m\pi}{a}\right)^2 - \omega^2 \mu\varepsilon} \tag{3.48}$$

and by substituting $m = 1$ yields α for the Lo-HOM.
Since α is given per unit length, the variation of the field intensity with distance along the transmission line can then be deduced from α, as will be shown in the following paragraphs. From this variation, the range of the field necessary for 3D EM analysis will then be deduced.
As can be seen from (3.32) – (3.34) as well as from (3.36) – (3.38), all field components of the HOMs have a general form given as (assuming propagation is in the z-direction):

$$\begin{aligned} X_{x,y\,or\,z} &= X_0\, e^{-\gamma z} \\ &= X_0\, e^{-\alpha z}\, e^{-j\beta z} \end{aligned} \tag{3.49}$$

where X_0 is the magnitude of the field component. Since $\gamma \approx \alpha$,

$$X_{x,y\,or\,z} = X_0 e^{-\alpha z} \quad , \tag{3.50}$$

indicating that the modes attenuate as a function of $e^{-\alpha z}$, assuming propagation in the z-direction.

From (3.50), the distance, l, away from the point of excitation where the field components of a given mode attenuate to a particular value can then easily be computed. For example, at a distance of $8/5\alpha$ away from the point of excitation, the fields of the mode attenuate to approximately 20% of the original value. Using (3.50), numerous investigations were performed and the range of existence of fields of HOMs necessary for 3D EM field analysis of the segment was defined as:

$$\frac{1}{10\alpha} \le l \le \frac{23}{5\alpha} \tag{3.51}$$

The electrical boundaries of discontinuities lie within this range. To define these boundaries, 12 data points, corresponding to 12 lengths of the interconnecting trace, have to be chosen and used for the 3D field analysis, from which the variation of power in the fundamental mode can be examined. For example, these points can be chosen as follows:

- Use eight lengths within the range where the fields attenuate to approximately 90% and 10% respectively, of their original values. This range is given by $1/10\alpha \le l \le 11/5\alpha$. Move in steps of $3/10\alpha$.

- Within the range where the fields attenuate to approximately 10% and 1%, respectively of their original value, use four lengths. This range is given by $11/5\alpha \le l \le 23/5\alpha$. Move in steps of $3/5\alpha$. Such a range, where the fields of the Lo-HOM attenuate to about 1% is taken into consideration so as to account for hybrid modes that may also be excited, as in the case of microstrip lines. Remember: Hybrid modes are considered as a combination of TE and TM modes.

II) 3D EM Field Analysis of the Interconnecting Traces and Discontinuity

Different discontinuities excite different modes (or combination of modes) and they all affect the fundamental mode differently. So, the electrical boundaries of any particular discontinuity can only be defined if the effect of the HOMs, (excited by that particular discontinuity) on the fundamental mode is studied. This can only be achieved through 3D EM field analysis and examination of power variation.

1. Full-wave EM Field Computation of Complete Segment and Examination of Power Variation

Since an infinite number of HOMs can be excited by a discontinuity, it is not possible to define the electrical boundaries of discontinuities by defining the exact point where each mode vanishes. For this reason, the methodology used to define the electrical boundaries of discontinuities in this work is based on the fact that the HOMs disturb the fundamental mode. Hence, the electrical boundaries of a discontinuity are characterized by an end of this disturbance.

To be able to define an end of the field disturbance caused by HOMs, the variation of power within the range defined in (3.51) must first be examined. For this purpose, the Poynting theorem, given in (3.52), where $\varepsilon = \varepsilon' - j\varepsilon''$ and $\mu = \mu' - j\mu''$ are allowed to be complex to account for loss, if any, is used.

$$-\frac{1}{2}\int_v\left(\vec{E}\cdot\vec{J_s}^{*}+\vec{H}^{*}\cdot\vec{M}_s\right)dv=\frac{1}{2}\oint_s\vec{E}\times\vec{H}^{*}\cdot d\vec{s}+\frac{\sigma}{2}\int_v\left|\vec{E}\right|^2dv+\frac{\omega}{2}\int_v\left(\varepsilon''\left|\vec{E}\right|^2+\mu''\left|\vec{H}\right|^2\right)dv + j\frac{\omega}{2}\int_v\left(\mu'\left|\vec{H}\right|^2-\varepsilon'\left|\vec{E}\right|^2\right)dv \tag{3.52}$$

The integral on the left hand side represents the complex power P_s, delivered by the electric source current, $\vec{J_s}$ and the magnetic source current, $\vec{M}_s$, inside the surface, S. The first integral on the right hand side represents complex power flow P_o, while the second and third integrals represent the time-average power dissipated P_l in the volume, V, due to conductivity, dielectric and magnetic losses – sometimes referred as Joule's law. The last integral represents stored magnetic and electric energies. With these definitions, the Poynting theorem can be re-written as

$$P_s = P_o + P_l + 2j\omega\left(W_m - W_e\right) \tag{3.53}$$

In words, this complex power balance equation states that the power delivered by the sources P_s is equal to the sum of the power transmitted through the surface P_o, the power lost to heat in the volume P_l, and 2ω times the net reactive energy stored in the volume [90].

In the immediate vicinity of the discontinuity, the imaginary part of the Poynting theorem, given by (3.53) is very large due to the presence of the reactive energy stored by the evanescent modes. As the distance away from the discontinuity increases, this imaginary part reduces very rapidly, due to the exponential decay of the fields of the HOMs. The electrical boundaries of discontinuities are characterized by a very small and steady component of this imaginary part and from these boundaries onwards, the current and field distributions on the trace resemble those of an infinitely long transmission line where only the TEM mode is present.

This variation in power, as we move away from the discontinuity, can also be seen in S-parameters since S-parameters can be derived directly from power. For example, $|S_{nn}|^2$ is equal to the ratio of power reflected from, to power incident on, an n-port. However, for the computation of these S-parameters, a numerical technique (e.g., the finite element method) that solves the complete wave equation must be used so as to take into consideration the effects of all the modes. Prior to performing such a computation, an accurate EM model of the discontinuity and its interconnecting traces must first be defined. This involves creating the geometry, assigning the material parameters, setting-up the necessary boundary conditions, defining the source of excitation and the frequency of interest. Only the fundamental mode has to be excited at the ports, since only the effects of the HOMs on this fundamental mode are of interest in defining the boundaries of the discontinuities. Furthermore, to prevent the frequency-dependent losses, given by P_l in (3.53), if any, from overshadowing the results, the S-parameters have to be computed only at a single frequency point – the highest frequency of interest. After the field computation, the extracted S-parameters shouldn't be renormalized to any impedance, since this may influence the results. In the next chapter, it will be explained how S-parameters were computed in this work.

III) Definition of the Electrical Boundaries of Discontinuities

Different lengths of the interconnecting traces needed for the field computations are taken from (3.51). At the end of the field computations, $|S_{nn}|$ is plotted against these lengths. From this plot, it will then be seen that as the electrical boundaries of the discontinuity is approached, $|S_{nn}|$ converges to a particular value and then becomes constant for a while.

Therefore, the electrical boundaries of discontinuities, represented by l_{bod}, can be defined as follows:

If

$$|S_{nn}|_l - |S_{nn}|_{l+\Delta l} \approx 0\,, \tag{3.54}$$

then $l = l_{bod}$.

Depending on the problem at hand, the electrical boundaries of a discontinuity can also be defined as the point away from the discontinuity where $|S_{nn}|$ changes by less than a self defined limit, e.g., 5%. In this case,

If

$$|S_{nn}|_l - |S_{nn}|_{l+\Delta l} \approx x \tag{3.55}$$

and

$$\frac{x}{|S_{nn}|_{l+\Delta l}} \leq 0.05 \tag{3.56}$$

then $l = l_{bod}$.

This methodology to define the electrical boundaries of geometrical discontinuities is summarized in Figure 3. 4.

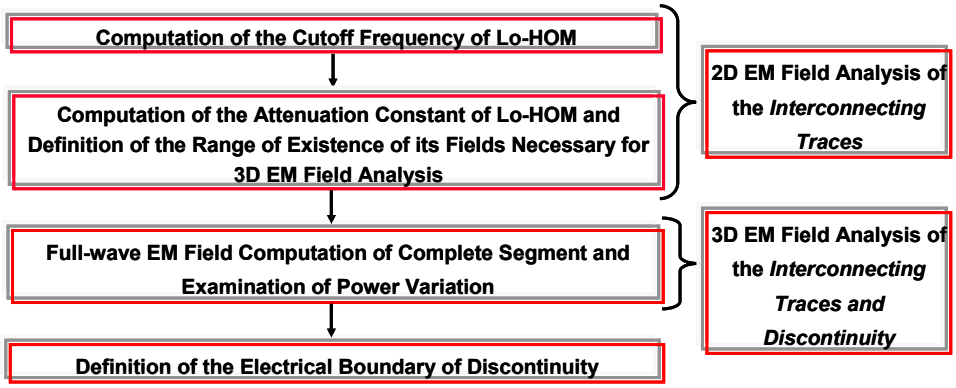

Figure 3. 4: Methodology for defining the electrical boundaries of Discontinuities.

Based on the boundaries of each discontinuity, the complete signal path has to be partitioned into interconnecting segments, so that efficient and accurate wideband models for each segment can be developed. The methodology used for modeling each segment will be discussed in the next section.

3.1.2 Efficient Wideband Modeling of Interconnecting Segments

In this section, the techniques used to efficiently and accurately model each interconnecting segment will be presented. The general methodology for all package/board interconnects will first be discussed, followed by the technique developed to model first and second level interconnections in arrays.

3.1.2.1 Modeling Methodology for Package/Board Interconnects

Examples of components that can be efficiently and accurately modeled using the methodology that will be presented in this section are:

- First Level Interconnects
    - E.g. flip chip interconnects, wire bonds, ribbon bands…
- Board Level Interconnects
    - E.g., bends, vias…
- Second Level Interconnects
    - E.g., solder balls, pins, connectors…

Each of these components is connected to a uniform trace, and together with these traces, they form the entire lengths of signal paths running from chip to chip, chip to board or from one component to another. In order to develop an efficient and accurate wideband model for these discontinuities, the following methodology is required:

- **Definition of the Electrical Boundaries of the Discontinuity:** This must be done at the beginning of the modeling process using the methodology presented in the previous section, because it provides very important information needed to develop accurate wideband models.
  - For example, it tells us exactly where the effects of the component begin and end in the needed frequency range. Consider the package trace with a 90° bend shown in Figure 3. 5. At microwave frequencies, the effects of the bend do not end at its physical boundaries (i.e., at AA_1) but extend towards BB_1 and CC_1 and even beyond, depending on the operating frequency.

  - Knowledge of the electrical boundaries of a discontinuity also enables field computations to be performed very efficiently. Without defining these boundaries, the positions of ports 1 and 2 in Figure 3. 5 will be defined through guess work.

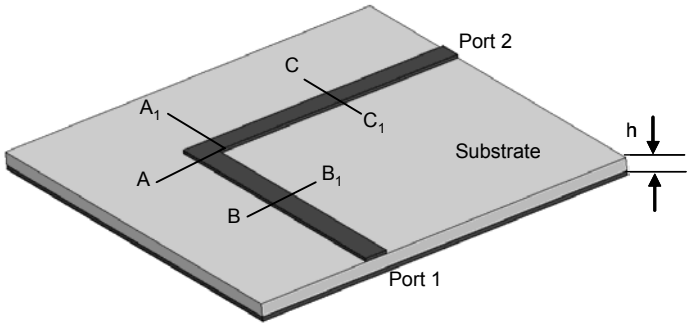

Figure 3. 5: Using a trace with a 90° bend to illustrate the importance of defining the electrical boundaries of discontinuities.

  - Based on the definition of the beginning and end of a component, a segment (comprising of the physical component and interconnecting traces on both sides, long enough to allow the HOMs excited at the discontinuity to vanish) is defined. The segment will then be used for the EM field computations.

- **3D EM Field Computation of Segment – Extraction of S-Parameters:** Due to the high integration density and hence, complexity of substrates in SiP modules, current distributions in the vicinity of a segment are generally not known. Consequently, analytical methods can not be used to compute the needed field quantities because they assume that all time derivatives are zero, which is only true for static cases. So full-wave EM field solvers (which employ numerical techniques to generate approximate solutions of Maxwell's equations in the entire problem region) have to be used to model these

segments and the metallizations around them in a more realistic way, taking into consideration all the return paths associated with the signal current. The solutions of such full-wave computations are normally exported as S-parameters, and contain all field components describing the modes associated with the segment, i.e., the HOMs as a result of the 3D component and TEM or quasi-TEM modes due to the uniform interconnecting traces.

- **Development of an Efficient Wideband Circuit Model for the Segment – Hybrid Modeling:** For the circuit model to be able to accurately account for the parasitic behavior of the segment, it must contain elements that capture the effects of both the TEM or quasi-TEM modes as well as the HOMs. In order to determine the circuit elements that represent the evanescent modes, their field or wave impedances must first be computed. The wave impedance of the TE modes is given as $Z_{TE} = -E_y / H_x$ [93]. Substituting (3.32) and (3.33) results in:

$$Z_{TE} = -\frac{A\sin\left(\frac{m\pi x}{a}\right) e^{-\gamma z}}{\frac{1}{j}\frac{\gamma}{\omega\mu} A\sin\left(\frac{m\pi x}{a}\right) e^{-\gamma z}} = \frac{j\omega\mu}{\gamma} \tag{3.57}$$

For evanescent modes, γ is purely real and Z_{TE} is reactively inductive. Thus, due to the presence of the evanescent TE modes, the interconnecting traces behave as an inductive storage element.

The wave impedance of the TM modes is given as $Z_{TM} = E_x / H_y$ [93]. Substituting (3.36) and (3.37) results in:

$$Z_{TM} = \frac{-j\frac{\gamma}{\omega\varepsilon} C\cos\left(\frac{n\pi x}{a}\right) e^{-\gamma z}}{C\cos\left(\frac{n\pi x}{a}\right) e^{-\gamma z}} = -j\frac{\gamma}{\omega\varepsilon} \tag{3.58}$$

For evanescent modes, γ is purely real and Z_{TM} is reactively capacitive. Thus, due to the presence of the evanescent TM modes, the interconnecting traces behave as a capacitive storage element.

Consequently, the circuit model for the segment must consist of lumped capacitors and inductors (for the evanescent HOMs) as well as transmission line models (for the TEM or quasi-TEM mode). Such a model that combines both distributed and lumped element models is known as a hybrid model. An example is shown in Figure 3. 6. The T-model in sub-segment 2 represents the EM energy stored in the HOMs as well as any losses that may occur.

Sub-segments 1&3 characterize the TEM or quasi-TEM modes on the uniform interconnecting traces. For an extraction of the circuit parameters, the following procedure has to be used:

- Per unit length parameters (i.e., inductance, capacitance…) distributed over the entire length of the uniform interconnecting traces must first be separately extracted from 2D EM field computations of a cross-section of a uniform transmission line having the same geometrical and material configuration as that of the interconnecting trace of the segment. The circuit values for each complete length of trace can then be obtained by multiplying the per unit length parameters by the entire trace length.

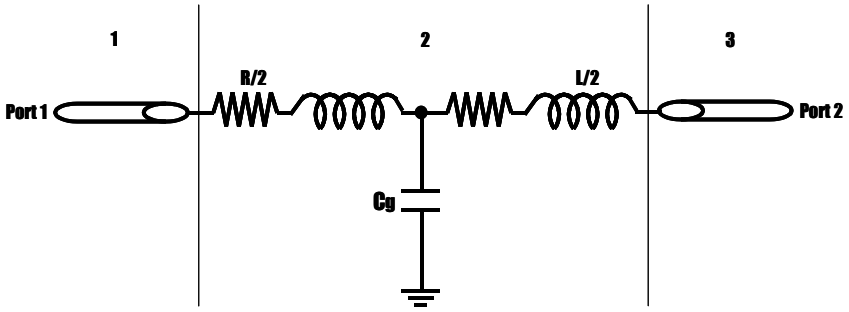

Figure 3. 6: Hybrid model used for characterizing a package/board component in an SiP module.

- These extracted values are used to characterize sub-segments 1 and 3 in Figure 3. 6, and values of the lumped inductors and capacitor in sub-segment 2 can then be obtained through a circuit optimization process.

This methodology for efficient and accurate modeling of package/board components is summarized in Figure 3. 7.

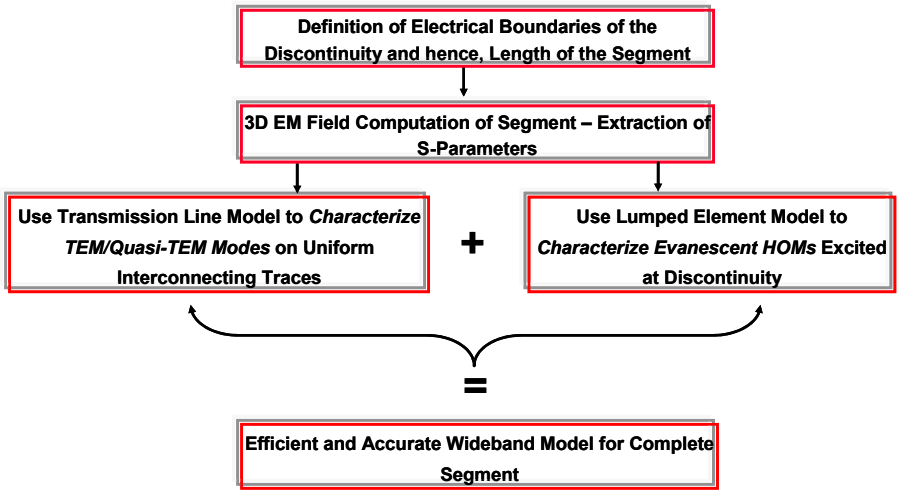

Figure 3. 7: Methodology for efficient and accurate wideband modeling of package/board components (Note: segment=discontinuity+ interconnecting traces).

3.1.2.2 Modeling Methodology for Arrays of First & Second Level Interconnects

Solder bumps are used for the interconnection of flip chips onto packages or boards (first level interconnections), as well as for the interconnection of packages on to boards (second level interconnections). Apart from their difference in size (the second level interconnect bumps being much larger), these bumps are geometrically and materially identical. Consequently, the same methodology was developed in this work to model both bumps in arrays, irrespective of the number of bumps in the array.
Figure 3. 8 presents a schematic view of such an array. For efficient and accurately modeling of this array, the following methodology is required:

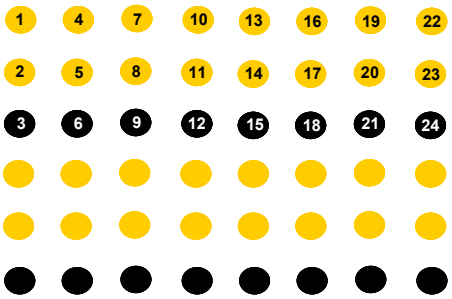

Figure 3. 8: Top schematic view of a bump array.

- EM and Equivalent Circuit Modeling of a Single Signal Bump.
  - Investigate and deduce optimal bump geometry for efficient and accurate EM modeling – Extract the inductance (L) and Resistance (R) of the bump.
  - Investigate the effects of a nearby power/ground bump (e.g., bump 6) on the RF/microwave characteristics of a signal bump (e.g., bump 5).
  - Since all bumps are assumed to be geometrically and materially the same, L&R extracted from any bump can be used to characterize any other bump in the array.
- Extraction of Coupling Capacitance (C) and Mutual Inductance (M) Between a Bump and its Neighbors, both in Parallel as well as in Diagonal Directions.
  - For example, C&M between 1&4, 1&7, 1&10, 1&5…
  - Due to technological constraints (e.g., small pitch) and the presence of power/ground bumps, coupling is always limited to between a bump and its immediate or next-but-one neighbor (e.g., between 1&4 or 1&7).
- Based on the Results of Coupling, Define Basic Repeatable Tile.
  - For example, if in the horizontal direction, coupling between bumps 1&7 can be neglected, in the vertical direction, the coupling ends between 1&2 and in the diagonal

direction, ground bump 9 limits coupling to between bumps 1&5, then the basic repeatable tile is as shown in Figure 3. 9.

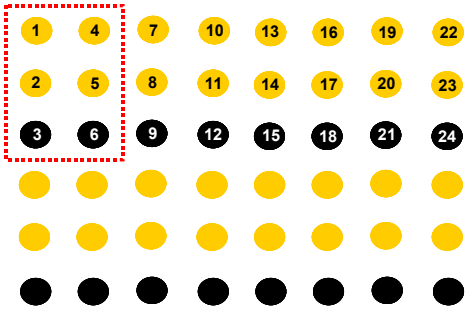

Figure 3. 9: Bump array showing basic repeatable tile.

- Investigate Passivity
  - For example, if mutual coupling between a bump and its "next-but-one" neighbor can be neglected, it implies in the L&C matrices, this coupling will be assigned a zero, which might cause the matrix to be active. Active inductance matrices can cause non-convergence of the circuit simulation, with computation of ever-growing voltages, and most dangerously, reasonable but incorrect results. So, before further using any of these matrices, it must first be investigated for passivity.
- Use Values of Parameters Extracted from Basic Repeatable Tile to Characterize Bump Array.
  - For example, in the case shown in Figure 3. 9, only L&R from a single bump, as well as C&M from two parallel and diagonal bumps are needed to characterize the complete array.

This methodology for modeling bump arrays, irrespective of the number of bumps in the array is summarized in Figure 3. 10.

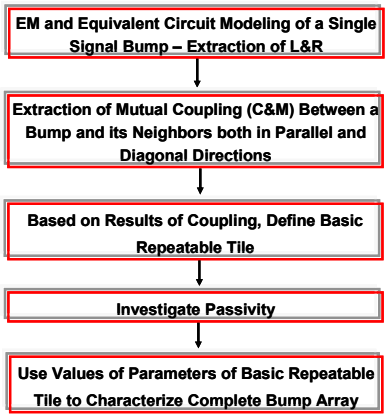

Figure 3. 10: Methodology for modeling of bump arrays, irrespective of the number of bumps in the array.

In the next chapter, this methodology will be illustrated with bump arrays used for the interconnection of flip chips onto packages of SiP modules. In the following section, the technique used to derive the criteria for passivity will be presented.

Investigating Passivity of Inductance Matrices

Generally, a dense inductance matrix completely filled out through a consistent EM field computation (without numerical errors) or measurement is not likely to be active. However, matrices constructed from partial results or by combination of results generated from several techniques can easily be active. Since in using values of electrical parameters extracted from a basic repeatable tile to characterize a bump array, values of mutual inductances considered negligible are set to zero, it is of vital importance to check if these L-matrices are passive.

In order to develop a criterion for testing the passivity of inductance matrix, the instantaneous power delivered p(t) to an inductance matrix is first considered. It is given by:

$$p(t) = \bar{i}^{T}(t)\bar{v}(t), \tag{3.59}$$

where the superscript T denotes the matrix transpose.

Substituting $\bar{v} = \bar{\bar{L}}\frac{d\bar{i}}{dt}$ in (3.59) to eliminate the voltage results in

$$p(t) = \bar{i}^{T}(t)\bar{\bar{L}}\frac{d\bar{i}(t)}{dt}, \tag{3.60}$$

where $\bar{\bar{L}}$ is the inductance matrix, whose diagonalized form is given as:

$$\bar{\bar{L}} = \bar{\bar{T}}\bar{\bar{\lambda}}\bar{\bar{T}}^{T} \tag{3.61}$$

with $\bar{\bar{T}}$ being an orthogonal matrix. Substituting equation (3.61) into (3.60) leads to

$$p(t) = \bar{i}^{T}(t)\bar{\bar{T}}\bar{\bar{\lambda}}\bar{\bar{T}}^{T}\frac{d\bar{i}(t)}{dt}. \tag{3.62}$$

Introducing the modal currents $\bar{i}_m$ ($\bar{i}_m = \bar{\bar{T}}^{T}\bar{i}$) gives the following simplified expression for the instantaneous power

$$p(t) = \bar{i}_m^{T}(t)\bar{\bar{\lambda}}\frac{d\bar{i}_m^{T}(t)}{dt}. \tag{3.63}$$

Since $\bar{\bar{\lambda}}$ is diagonal, (3.63) then simplifies to

$$p(t) = \sum_{k=1}^{N} \lambda_k i_{mk}(t) \frac{di_{mk}(t)}{dt}. \tag{3.64}$$

This implies, the total power is the sum of powers in each mode.
For the inductance matrix to be passive, the total power delivered to the matrix from the start of time must be positive at any given time. Mathematically, this means

$$E(t) = \int_{-\infty}^{t} p(\tau) d\tau \geq 0 \ \forall t. \tag{3.65}$$

Integrating (3.64) gives

$$E(t) = \int_{-\infty}^{t} \sum_{k=1}^{N} \lambda_k i_{mk}(\tau) \frac{di_{mk}(\tau)}{d\tau} d\tau. \tag{3.66}$$

Interchanging the integral and summation, and assuming the currents are initially zero, then integration yields

$$E(t) = \frac{1}{2} \sum_{k=1}^{N} \lambda_k i_{mk}^2(t). \tag{3.67}$$

$i_{mk}^2(t) \geq 0$ always. So for $E(t) \geq 0$ for any arbitrary time, in general

$$\lambda_k \geq 0 \ \forall \ k \tag{3.68}$$

is required.

Therefore, the inductance matrix is passive only when all of its eigenvalues are greater than or equal to zero. However, a zero eigenvalue represents a shorted modal voltage. So in practice, positive eigenvalues are needed.
Unlike inductance matrices which can be active, capacitance matrices are always passive. Practically, this means that capacitance matrices can be assembled or simplified, such as deleting small terms, without worrying about an active matrix [89].

3.1.3 Cascading the Interconnecting Segments to Generate Wideband Models for Complete Signal Paths

Generally, cascaded sections of two-ports (see Figure 3. 11) can be analyzed by multiplying T-matrices of individual sections to yield the T-matrix of the overall network, as shown in (3.69).

Figure 3. 11: A cascade of two-port components.

$$[T] = [T]_1 [T]_2 \ldots [T]_N \tag{3.69}$$

Each wideband model developed in this work is represented by a set of S-parameters. However, S-matrices cannot be cascaded, because some of the variables at the port are independent while the rest are dependent. Therefore, the S-matrices obtained from each segment must first be converted to **transfer scattering or T-parameters** using the following relationship.

$$T_{11} = \frac{(-S_{11}S_{22} + S_{12}S_{21})}{S_{21}} \tag{3.70}$$

$$T_{12} = \frac{S_{11}}{S_{21}} \tag{3.71}$$

$$T_{21} = \frac{-S_{22}}{S_{21}} \tag{3.72}$$

$$T_{22} = \frac{1}{S_{21}} \tag{3.73}$$

The T-matrices from all interconnecting segments are then multiplied to generate T-matrices of the complete signal path, which are finally re-converted using (3.74) – (3.77), to obtain S-matrices of the complete path.

$$S_{11} = \frac{T_{12}}{T_{22}} \tag{3.74}$$

$$S_{12} = T_{11} - \left(\frac{T_{12}T_{21}}{T_{22}} \right) \tag{3.75}$$

$$S_{21} = \frac{1}{T_{22}} \tag{3.76}$$

$$S_{22} = \frac{-T_{21}}{T_{22}} \tag{3.77}$$

For analyzing cascaded networks, ABCD parameters can also be used. However, T-matrix representations are preferred to ABCD representations because of the following considerations: The calculations required for the transformation from S-matrix to T-matrix are slightly less complex than those required from S-matrix to ABCD matrix transformations. Also, T-parameters are defined in terms of wave variables normalized with respect to impedances at various ports exactly in the same way as for S-parameters. This allows an easier interchange to two representations [94].

3.2 Methodology for Optimizing RF Performance

The main goal of optimizing the performance of SiP modules as well as other chip and system packages is to create electrically transparent interconnections between chips in a sub-system or system, so as to maintain SI. This performance optimization can only be achieved if reflections and distortions along single signal paths, as well as undesired EM coupling between neighboring paths can be reduced to within acceptable limits. Since these SI problems are mostly caused either by improperly designed and/or wrong choice of package components or materials within the frequency range of interest, they can be minimized, if appropriate design measures are implemented at the beginning of the design cycle [95].
In this section, methodologies developed to minimize reflections and signal distortions as well as cross-talk will be presented.

3.2.1 Minimizing Reflections and Distortions

The following methodology is required to minimize reflections and distortions:

3.2.1.1 Identification of the Potential Causes of Reflections and Distortions

Generally, reflections and distortions are caused by impedance mismatch along signal paths. In order to develop design rules to minimize these SI problems, the particular components which contribute the greatest amount of reflections that may violate the noise margin, must first be identified. For this purpose, wideband models that account for the parasitic contribution of each package/board component along complete signal paths must be developed. The methodology presented in section 3.1 leads to the development of exactly such models.
Using these wideband models, the impact of each package/board component as well as the effect of its technological tolerances can then be easily studied.

3.2.1.2 Deduction of Critical Components and Development of Design Measures to Optimize their RF Performances

Based on the results of investigations aimed at studying the effects of different package/board components, components causing the greatest amount of reflections and signal distortions can then be identified, and termed critical components within a given frequency band.
Since the reflections and distortions caused by these critical components are as a result of their geometrical and material configurations, the following design measures can be used to keep these SI problems within acceptable limits, thereby optimizing their respective RF performances.

- **Optimal Choice and Design of Critical Components:** The optimal choice is obtained by comparing various technologies of a given component that can be used to achieve the same design goal. For example, for the interconnection of traces between signal layers in a multi-layered substrate, there is a possibility of using either buried, blind or through-hole

vias. However, the amount of reflections generated depends on the choice of via made. If all the vias are capacitive (i.e., if the characteristic impedance of each via is less than that of the interconnecting traces), then through-hole vias might be preferable, since buried as well as blind vias have the disadvantage that additional capacitances are built between any of the reference planes and the annular ring(s), thereby further reducing the characteristics impedance of the via and causing more mismatch. On the other hand, if all the vias are inductive (i.e., if the characteristics impedance of each via is greater than that of the interconnecting traces), then either a buried or blind via might be preferable, because through-hole vias have the disadvantage of being longer, thus resulting in more signal inductance and hence, further increasing the characteristics impedance of the via and causing more mismatch. So prior to making the final decision on the layer stack-up, a comparative study must first be made. Once the optimal choice of the critical component is obtained, then an optimal design must also be achieved. For example, if a through-hole via is the chosen capacitive via, then design measures must then be deduced to increase the characteristics impedance of the via, so as to better match it to that of the interconnecting trace. An example of such a design rule involves using interplane vias to interconnect the reference planes, so that they can serve as return paths for the signal currents. By placing these interplane vias further away from the signal via, the loop inductance increases and consequently, the characteristics impedance of the via also increases, leading to a better impedance controlled component. This increases the RF performance of the via, as well as the entire module.

- **Consideration of the Effects of Technological Tolerances at the Beginning of the Design Cycle:** Based on the results of the sensitivity studies performed when investigating the impact of technological tolerances, tighter design guidelines have to be in-cooperated at the beginning of the design cycle so as to prevent the material and/or geometrical parameters of the critical components from fluctuating out of the desired range, thereby keeping the amount of additional reflection caused within acceptable limits. This also increases the RF performance of the component under consideration.

3.2.1.3 Use Optimized Configurations of Critical Components to Minimize Reflections and Distortions in the Entire Module

Once design measures have been developed to optimize the RF performance of the critical components, they can then be implemented at the beginning of the design cycle, to minimize reflections and distortions that occur in the entire module, thereby optimizing its RF performance. The level of optimization achieved for the entire module can easily be observed at the circuit simulation level by using the wideband model that accounts for the parasitic contribution of all interconnecting segments along the entire signal path. By comparing the reflection and transmission behavior of a signal propagating through the complete path before and after values of electrical parameters representing the optimized component(s) are used, the improvement in the electrical behavior of the entire module can easily be noticed.

The methodology developed to minimize reflections and distortions in SiP modules as well as other chip or system packages is summarized in Figure 3. 12.

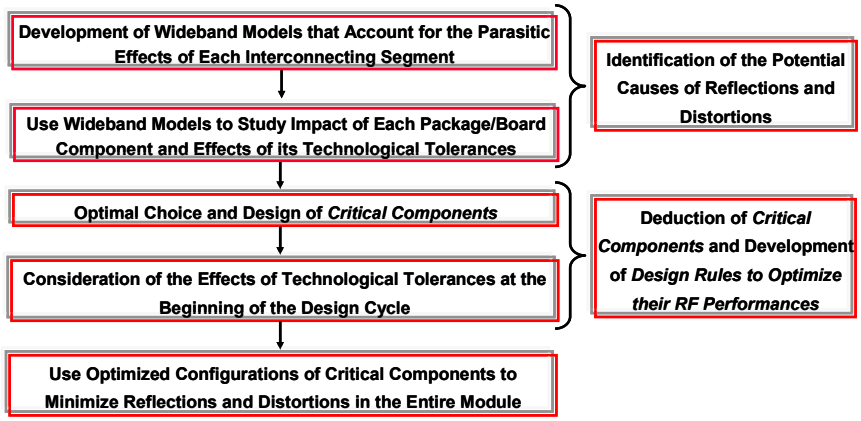

Figure 3. 12: Methodology to minimize reflections and distortions in SiP modules as well as in other chip and system packages.

3.2.2 Minimizing Cross-talk

The easiest way to minimize cross-talk (which occurs as a result of undesired EM coupling between neighboring components) is to keep the components very far apart. However, due to technological and cost limitations, it is not always possible to keep components too far apart so as to reduce cross-talk to within acceptable limits. So, alternative techniques must be developed.

In this work, methods to minimize cross-talk between package traces as well as between vias were developed. These methods will be discussed in the following two sections.

3.2.2.1 Minimizing Cross-talk between Package/Board Traces

EM coupling between neighboring traces can be described in terms of near- and far-end cross talk, commonly known as NEXT and FEXT, respectively. (3.78) and (3.79) present equations that can be used to estimate the amount of NEXT and FEXT that occurs in package/board traces.

$$NEXT = \frac{V_b}{V_a} = K_b = \frac{1}{4} * \left(\frac{C_{ML}}{C_L} + \frac{L_{ML}}{L_L} \right) \tag{3.78}$$

$$FEXT = \frac{V_f}{V_a} = \frac{length}{rise\,time} * K_f = \frac{length}{rise\,time} * \frac{1}{2v} * \left(\frac{C_{ML}}{C_L} - \frac{L_{ML}}{L_L} \right) \tag{3.79}$$

where

$$K_f = \frac{1}{2v} * \left(\frac{C_{ML}}{C_L} - \frac{L_{ML}}{L_L} \right)$$

V_b =Maximum voltage on quiet line, V_a =Maximum voltage on active line

K_b =Backward coefficient

C_{ML} =Mutual capacitance per length

C_L =Capacitance per length of signal trace

L_{ML} =Mutual inductance per length

L_L =Inductance per length of signal trace

V_f = Voltage at the far end of the quiet line, V_a =Voltage on the signal line

K_f =Far end coupling coefficient (depends only on intrinsic terms)

v=speed of the signal on the line

As can be seen from these equations, both NEXT and FEXT depend on intrinsic terms that are based on the cross-sections of the coupled lines. These coupling terms depend on the layer stack-up (especially substrate thickness), substrate material and distance of separation between the traces. To achieve a given characteristics impedance, a fixed ratio of trace width to substrate thickness is always used. Therefore, attempting to reduce the substrate thickness (so as to minimize cross-talk) after the characteristics impedance has already been defined, leads to a creation of impedance mismatch right at the input port. However, for a given line impedance, an optimal substrate technology can be chosen, so as to reduce the capacitive coupling that occurs between the traces and hence minimizing cross-talk.
In the following paragraphs, the methodology to minimize cross-talk, based on the appropriate choice of substrate material is given.

- **Computation of the Inductance (L) and Capacitance (C) Matrices of the Coupled Traces for Different Substrate Technologies:** These matrices contain all the information about the cross-sections of the coupled lines needed for cross-talk analysis. For each substrate technology, vary the distance of separation between the lines as a function of the line width (e.g., vary S between w and 6w: where S is the distance of separation and w is the line width). In order to achieve a fair comparison, the characteristics impedances of all the traces designed in the different technologies must be the same (e.g., they must all be 50Ω traces).

- **Computation of the Coefficients of Cross-talk:** Based on the extracted L and C-matrices, compute the coefficients of backward and forward cross-talk, using the relationships given in (3.78) and (3.79). Deduce the dependency of these coefficients on S.

- **Deduce Optimal Substrate Technology, Based on Available Noise Margin:** For example, if the noise margin allocated for cross-talk is 5%, then less than 2% coupling must occur between any two neighboring traces so as to meet the noise margin. The substrate material that meets this requirement with the smallest S will be chosen as the

substrate technology of choice. Substrates with smaller dielectric constants have more advantages here.

The coupling lengths between adjacent traces must also be kept to a minimum in order to further minimize FEXT. Very sensitive lines should always be routed in stripline.

3.2.2.1 Minimizing Cross-talk between Vias

In order to minimize cross-talk between vias, the following methodology is required:

- **Develop an EM and a Wideband Circuit Model for Coupled Vias** using the techniques presented in section 3.1.2. Extract the coupling capacitance and mutual inductance between the aggressor and its victim, both being signal vias.

- **Use Interplane Power/Ground Vias to Minimize Inductance:** By placing interplane vias quite close on the sides of the signal vias reduces their respective inductances, because bringing an interplane via closer to any of the signal vias causes an increase in the partial mutual inductance between the interplane via and the signal via. This larger partial mutual inductance then acts to decrease the total number of field line loops around each via. Hence, the loop self-inductance of the signal via falls. This can also be explained using the equation below [96]:

$$L_{loop} = L_a + L_b - 2L_{ab} \tag{3.80}$$

where,

L_{loop} = the loop self-inductance of the signal and interplane via

L_a = partial self-inductance of signal via

L_b = partial self-inductance of interplane via

L_{ab} = partial mutual inductance between signal and interplane via

As the distance between the signal and interplane via decreases, the partial mutual inductance increases (i.e., the term $2L_{ab}$ becomes larger). Consequently, L_{loop} decreases.

Approximately three interplane vias, equally spaced beside each signal via can be used. The circuit model developed can always be used to extract the inductance of each signal via.

- **Use Interplane Vias between Signal Vias to Minimize Magnetic Field Intensity:** As signal current flows down the aggressor, a voltage is induced in the interplane via, which causes return current to flow through the interplane via. This current also produces magnetic fields that cancel the original magnetic fields, thereby reducing the total magnetic field intensity between the aggressor and the victim. Consequently, cross-talk is also minimized. Depending on the configurations of the signal and interplane vias, this

technique leads to more than 50% cross-talk reduction in vias, even if only one interplane via is used in between the signal vias.

As will be illustrated in the next chapter, the capacitive coupling between vias in chip packages and PCBs is very small and can be neglected.

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Chapter 4

Illustrating the Novel Modeling Methodologies for System-in-Package Modules: Case Study – BGA Package Module

4.1 BGA Packages

The present miniaturization trend towards higher-performance, smaller and lighter products has resulted in an increasing demand for smaller component packages and/or higher pin counts. In order to accommodate the increasing number of I/Os needed, conventional IC packages, e.g., the Quad Flat Pack (QFP), are forced to have an ever finer lead pitch with thinner and more fragile leads. BGA packages, on the other hand, satisfy the I/O demand using a far coarser pitch by taking advantage of the area under the package for solder sphere interconnections. Additionally, the package size and board real estate required are usually smaller for BGA packages. Consequently, they are ideally suited for low-cost and high-volume applications where package size and performance are of major importance. As a result of these advantages, BGA package modules have received widespread acceptance in the packaging industry. It is for this reason that they were chosen to illustrate the novel modeling and optimization methodologies for SiP modules, developed in this work. Typical BGA applications include: notebook computers, personal digital assistants (PDAs), mobile telephone handsets, high-density disk drives, camcorders, digital cameras, etc [97], [98].

Over the years, a great variety of BGA packages has evolved. This variety can be roughly classified into three different categories (based on the material or technology used to fabricate them) namely: plastic, ceramic and tape BGAs [99]. Their cross-sectional views are shown in Figure 4. 1.

The plastic BGA (PBGA) is the industry description of what is sometimes referred to as Motorola's OverMolded Pad Array Carrier or OMPAC. It was developed by Motorola in the late 1980's for use in Motorola products with space limitations such as radios, pagers and cellular telephones. The PBGA package is based on a printed circuit board substrate or "lead frame" fabricated of Bismaleimide Triazine (BT) epoxy/glass laminate. The silicon chip containing the integrated circuits is either wire- or flip chip bonded to the top side of the substrate. In the example shown in Figure 4. 1, wire bonds are used for the interconnection

between the chip and the substrate. Traces from the wire bond pads take the signals to vias, which carry them to circular solder pads on the bottom side of the substrate. An over mold (or possibly a liquid or "glob-op" encapsulation) is then performed to completely cover the chip, wires and substrate wire bond pads. The bottom side solder pads are laid out on a square or rectangular grid with a pitch of about 1 mm. Solder balls are then attached to the pads. Almost universally, the solder balls used on PBGAs are 63% Sn/37% Pb eutectic, melting at approximately 180°C. With eutectic solder balls, the assembly is very robust. Through the solder balls, signals go to the printed circuit board (PCB) level. At this level, typical packaging structures include daughter card, motherboard or back plane. The signals then continue to another system component, such as an ASIC (Application Specific Integrated Circuit) chip, a memory module or a termination block [99] – [101].
A comprehensive discussion of the BGA packaging technology can be found in many publications (e.g., in [102]).

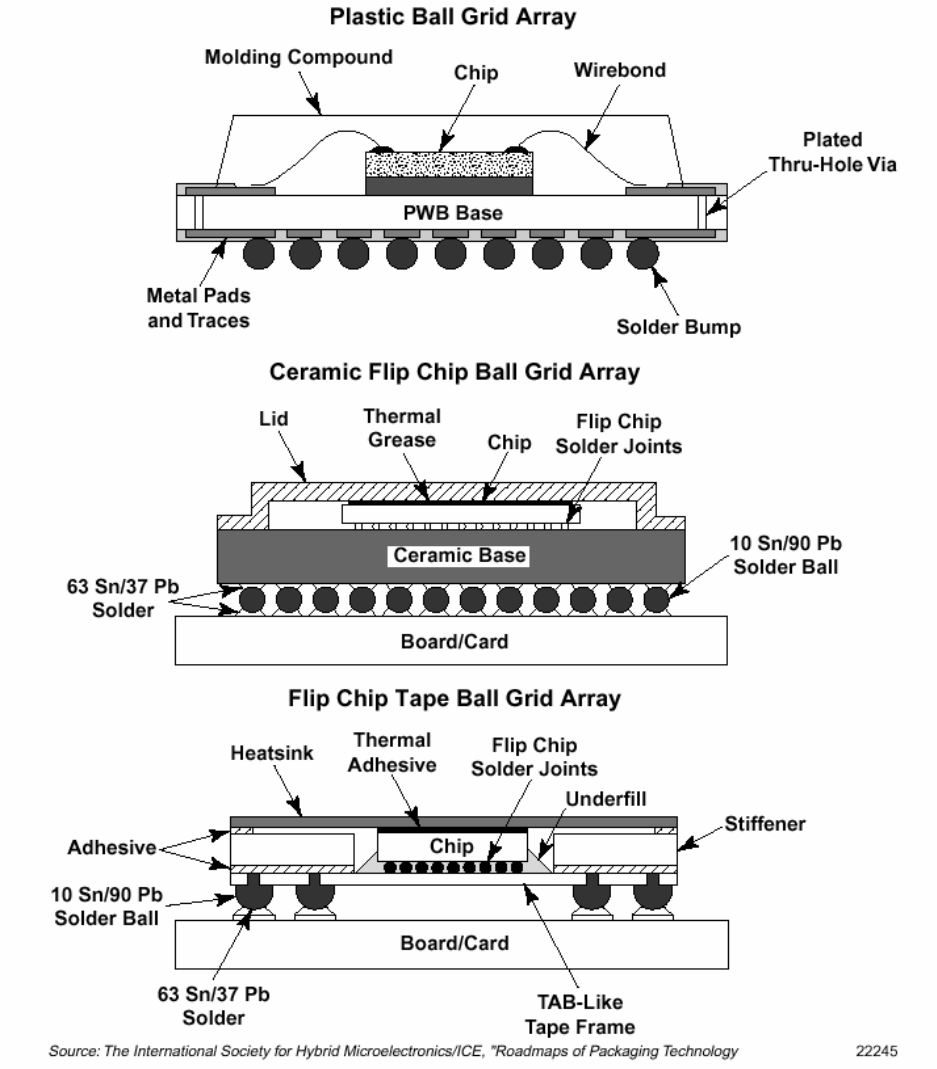

Figure 4. 1: Three BGA families [99].

4.2 Development of Wideband Models for Complete Signal Paths (Chip-to-Board) in BGA Package Modules

In this section, the novel modeling methodologies presented in section 3.1 will be used to develop a wideband model for complete signal paths (chip-to-board) as well as for each interconnecting segment in a BGA package module. Figure 4. 2 shows a schematic view of a flip chip BGA package, illustrating the complete signal path from chip to board that has to be modeled and simulated. For illustrative reasons, the dielectric layers above plane 1 and below plane 2 (in the substrate) are not shown in the figure. The complete path consist of flip chip interconnects (interconnecting the chip and the package), uniform package traces and bends, through-hole vias (interconnecting signal layers within the package) and BGA balls (interconnecting the package and the board – PCB).

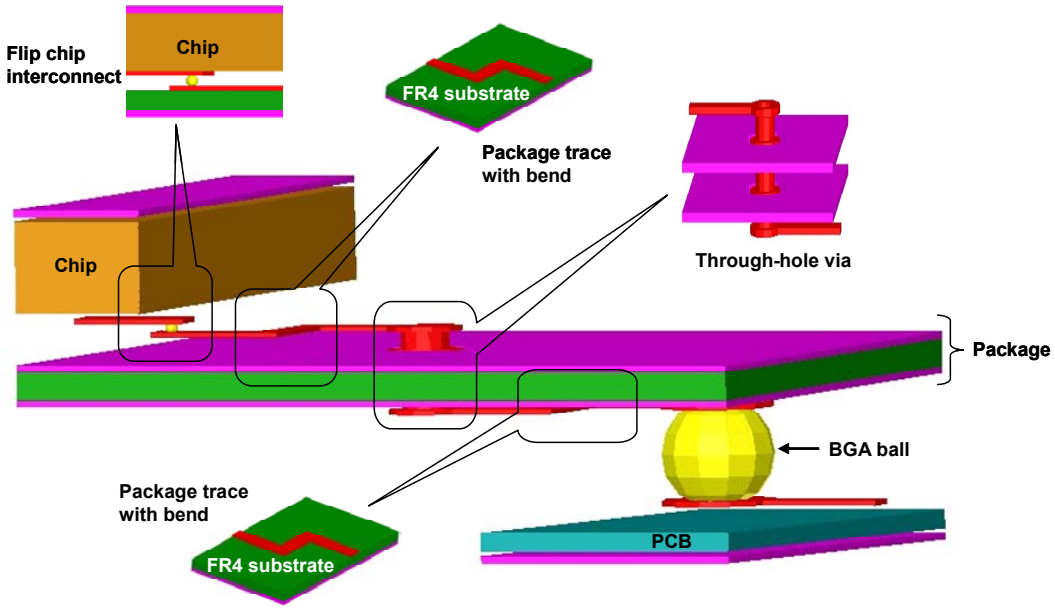

Figure 4. 2: Schematic view of a flip-chip BGA package illustrating the complete signal path from chip to board.

4.2.1 Defining the Electrical Boundaries of Discontinuities and Segmentation of Complete Path

For an illustration of the methodology developed for defining the electrical boundaries of discontinuities, a through-hole via, whose cross-sectional view is shown in Figure 4. 3, was used as an example. The via interconnects two uniform 50 Ω microstrip traces (each being 175 μm wide and 27 μm thick), on layers 1 (L1) and 4 (L4), in a four-layered FR4 substrate (ε_r=4.2, tan δ=0.007). The inner layers (L2 & L3) are used as power/ground planes. Each of the pre-peg layers has a thickness of h1=100 μm, and the core is 150 μm (h2) thick. The

diameters of the via hole (D1) and pad (D2) are 200 μm and 400 μm, respectively. The interplane via shown on the left of the through-hole via is used to interconnect the two inner reference planes, in the case that they are at the same potential. Otherwise, decoupling capacitors are used.

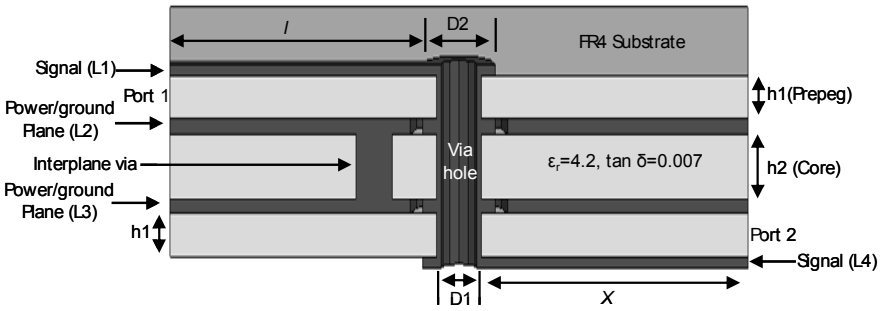

Figure 4. 3: Cross-sectional view of via and interconnecting traces.

In order to define the electrical boundaries of the signal via, the following procedure was used:

1. 2D EM Field Analysis of the Interconnecting Microstrip Traces

Considering the geometrical and material parameters of the microstrip traces given in the previous paragraph, the cutoff frequency of the Lo-HOM was computed to be approximately 200 GHz. That means, all HOMs excited below this frequency decay at a sufficient distance away from the point of excitation (the via in this case). To define this distance, α of the Lo-HOM was computed at 30GHz (highest frequency considered in this work to illustrate methodology) to be approximately 1.48 E+03 Np/m. Then using (3.51), the range of existence of fields necessary for 3D EM field analysis was defined. Within this range, 12 data points, corresponding to 12 different lengths of the interconnecting microstrip traces, as stipulated in section 3.1, were also defined.

2. 3D EM Field Analysis of the Interconnecting Traces and Via

Using each of the lengths of the interconnecting traces defined above, 3D EM field computations were performed for the whole segment using Ansoft's High Frequency Structure Simulator (HFSS) – a full-wave EM field solver that employs the finite element method to solve Maxwell's equations, leading to the generation of S-parameters. However, prior to performing each field computation, an EM model of the segment was first set-up. An example of such a model is shown in Figure 4. 4.

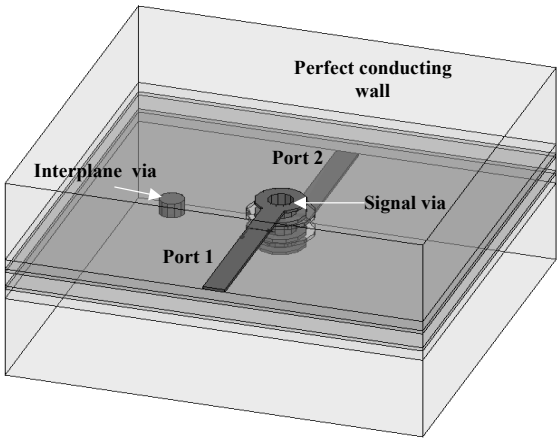

Figure 4. 4: An example of a 3D model of the via segment that was used for EM field computations.

Perfect electric boundary conditions were used, i.e., the 3D model is surrounded by perfect conducting walls or surfaces. Wave ports were used as the sources of excitation and uniform transmission line that represents the microstrip traces on the package/board were used to connect the wave ports to the via.

To compute the S-parameters associated with the model, HFSS first divides the structure into a number of relatively coarse tetrahedra, each having four triangles. The vertices of objects are then used as the initial set of tetrahedra vertices. Other points are added to serve as the vertices of tetrahedra only as needed to create a robust mesh.

The excitation field pattern at each port is then computed. Since each port is connected to the via through a uniform microstrip transmission line that has the same cross-section as the port, the excitation field is therefore the field associated with waves propagating along the transmission line to which the port is connected. For this purpose, HFSS solves the wave equation for $\vec{E}$, which is derived from Maxwell's equations and obtains the field pattern in the form of a phasor solution, $\vec{E}(x,y)$. It also solves independently for $\vec{H}(x,y)$ using the corresponding wave equation in $\vec{H}$. These phasor solutions are independent of z and t; only after being multiplied by $e^{\gamma z}$ do they become traveling waves. Since the computation of the excitation field pattern is treated as a 2D finite element problem, the 2D mesh on the port's face is refined and the $\vec{E}$ and $\vec{H}$ fields are recomputed. To determine if the 2D solution is accurate, HFSS solves the following equations:

$$\nabla \times \vec{H} = \sigma \vec{E} + j\omega\varepsilon \vec{E} \tag{4.1}$$

$$\nabla \times \vec{E} = -j\omega\varepsilon \vec{H} \tag{4.2}$$

It then compares the results obtained for $\vec{E}$ and $\vec{H}$ from the solution of the wave equations to those obtained from (4.1) and (4.2), respectively. If the reciprocal comparison falls within

an acceptable tolerance, the solution is accepted. Otherwise, the 2D mesh on the port is further refined and HFSS performs another iteration. To obtain optimal port accuracy of the field computations performed in this work, the impact of the port accuracy on the computed port impedances was computed. Based on these computations, the accuracies of the port computations were set to 0.005%.

From the computed $\vec{E}$ and $\vec{H}$ at the ports, HFSS then computes the power associated with the field excitation. Using this field excitation, the full EM field pattern inside the structure is then computed, assuming that one mode is excited at a time. During the computation, a fraction of the excited power is reflected back to the ports and some is transmitted. The full field pattern at a port is the sum of the port's excitation field and all reflected/transmitted fields. Based on field patterns at each port, the generalized S-parameters, which describe what fraction of power associated with a given field excitation is transmitted or reflected at each port, are computed. It is possible for a 3D field solution generated by an excitation signal of one specific mode to contain reflections of higher order modes which arise due to discontinuities in the structure.

Since the computation of the 3D field solution is also treated as a 3D finite element problem, the solution is refined until the convergence criterion (the needed delta S) is met. Delta S is the change in magnitude of S-parameters between two consecutive passes. If the magnitude and phase of all S-parameters change by an amount less than the maximum delta S per pass value from one iteration to the next, the adaptive process stops. Otherwise it continues until the requested number of passes is completed. The maximum delta S is defined as [103].

$$Max_{ij}\left[mag\left(S_{ij}^{N}-S_{ij}^{N-1}\right)\right] \tag{4.3}$$

where i and j cover all matrix entries and N represents the pass number.

The value of delta S used determines the accuracy of the field computations. Hence, prior to the actual field computations, the impact of different values of delta S on the computed S-parameters as well as the extracted electrical parameters were first investigated and based on the results of these investigations an optimal value of delta S was chosen. For example, 0.003 was used as an optimal value for the via whose dimensions are given in section 4.2.1.

The EM field computations were performed for different values of l and a fixed value of x (see Figure 4. 3).

Apart from the S-parameters used to define the electrical boundaries of discontinuities, all other S-parameters computed in this work were renormalized to appropriate port impedances. Unless otherwise stated, the port impedance used was 50 Ω.

3. Definition of the Electrical Boundaries of the Via

At the end of each field computation, an S-matrix was extracted. $|S_{11}|$ at 30 GHz from each matrix was plotted against the corresponding length and the graph shown in Figure 4. 5 was obtained.

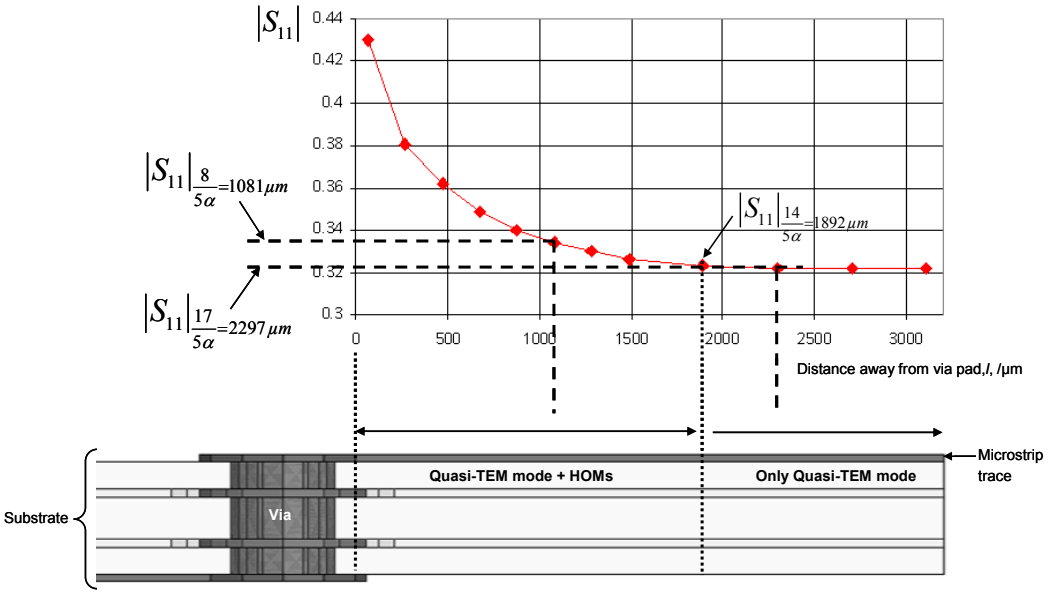

Figure 4. 5: Variation of $|S_{11}|$ at 30 GHz with distance away from via pad.

As expected, $|S_{11}|$ changes very rapidly in the via of the discontinuity due to the presence of the fields of HOMs. But from a distance of $8/5\alpha$, corresponding to 1.081mm away from the via pad, $|S_{11}|$ changes by less than 5%. It becomes approximately constant at $14/5\alpha$ (=1.892 mm), signifying the disappearance of the fields of HOMs. Therefore, according to (3.54), since

$$|S_{11}|_{l=\frac{14}{5\alpha}=1892\mu m} = 0.323$$

and

$$|S_{11}|_{l+\Delta l\left(=\frac{3}{5\alpha}\right)=\frac{17}{5\alpha}=2297\mu m} = 0.322 = \text{Constant}$$

then

$$|S_{11}|_{l=\frac{14}{5\alpha}=1892\mu m} - |S_{11}|_{l+\Delta l\left(=\frac{3}{5\alpha}\right)=\frac{17}{5\alpha}=2297\mu m} \approx 0,$$

Signifying that $l = l_{bod}$

$\Rightarrow$ The electrical boundaries of the via are at a distance of $\frac{14}{5\alpha} = 1892\mu m$ away from the via pad.

However, depending on the problem at hand, these boundaries can also be defined as points away from the via pad where $|S_{11}|$ changes by less than a self-defined limit, e.g., 5% [104]. In this case, applying (3.55) and (3.56) yields the following:

Given

$$\left|S_{11}\right|_{l1=\frac{8}{5\alpha}=1081\mu m} = 0.334,$$

$$\left|S_{11}\right|_{l1+\Delta l\left(=\frac{9}{5\alpha}\right)=\frac{17}{5\alpha}=2297\mu m} = 0.322 = \text{constant}$$

and

$$\left|S_{11}\right|_{l1=\frac{8}{5\alpha}=1081\mu m} - \left|S_{11}\right|_{l1+\Delta l\left(=\frac{9}{5\alpha}\right)=\frac{17}{5\alpha}=2297\mu m} \approx 12,$$

then

$$\frac{12}{\left|S_{11}\right|_{l1+\Delta l\left(=\frac{9}{5\alpha}\right)=\frac{17}{5\alpha}=2297\mu m}} \approx 0.0373 < 0.05$$

Signifying that $l1 = l_{bod}$

$\Rightarrow$ Considering the 5% limit, the electrical boundaries of the via are at a distance of $\frac{8}{5\alpha} = 1081\mu m$ away from the via pad.

Following the general methodology presented in section 3.1, the electrical boundaries of all other discontinuities in the BGA package module were defined. Examples are shown in Figure 4. 6 and Figure 4. 7 for the case of a BGA ball and a 90° bend, respectively, where the electrical boundaries are defined at 30 GHz.

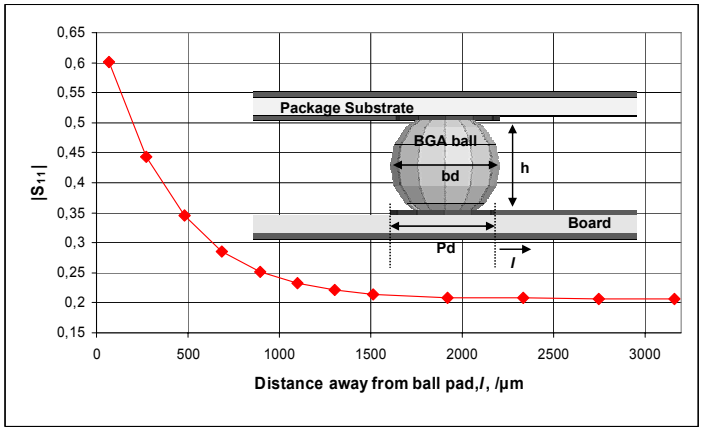

Figure 4. 6: Illustrating the electrical boundaries of discontinuities of a BGA ball with the following dimensions: Ball diameter (bd) =600µm, ball height (h) =500 µm and pad diameter (pd) =500 µm. Actual boundary of ball is at a distance of 14/5α (=1.924 mm). However, at 11/5α (=1.511 mm), $|S_{11}|$ changes by less than 5%.

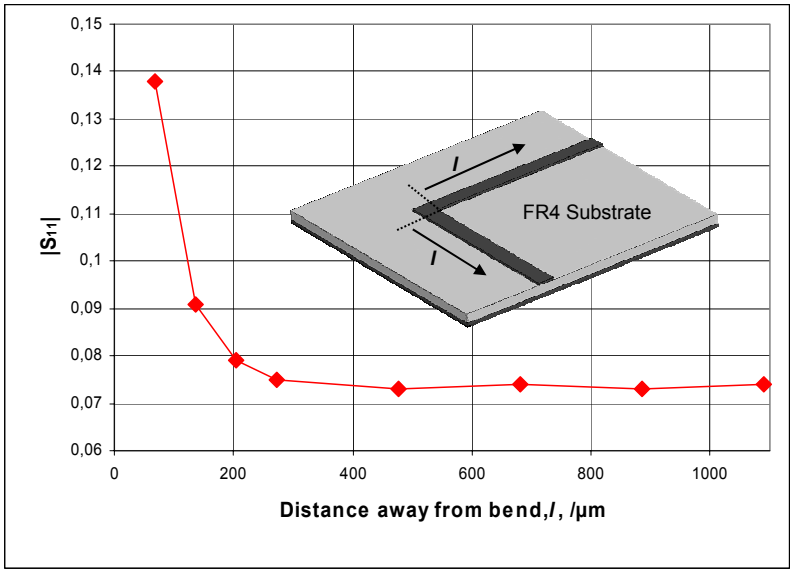

Figure 4. 7: Illustrating the electrical boundaries of discontinuities of a 90° bend. Boundary of bend is at a distance of 7/10α (=0.477 mm), since $|S_{11}|$ changes by less than 5%.

Based on the definition of the electrical boundaries of each discontinuity, the entire signal path (chip-to-board) was partitioned into interconnecting segments and each segment was efficiently and accurately modeled. In the following section, the modeling methodologies applied to each segment will be illustrated.

4.2.2 Wideband Modeling of Interconnecting Segments

In this section, the novel methodologies developed for wideband modeling of each interconnecting segment, starting from chip-to-substrate interconnects, through substrate components to substrate-to-board interconnects, will be illustrated.

4.2.2.1 Modeling of Bump Arrays – Illustration and Validation of Modeling Methodology

For an illustration of the modeling methodology developed in section 3.1.2.2, the bump pattern shown in Figure 4. 8 was used. This pattern is used in most flip chip packages to reduce cross-talk e.g., in [105], because the power/ground bumps limit EM coupling to between two neighboring bumps.

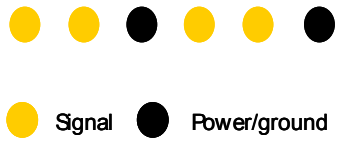

Figure 4. 8: Basic bump pattern to manage cross-talk.

Depending on the required number of I/Os, this basic pattern can be extended to form a larger bump array, as shown in Figure 4. 9. The pitch between the bumps is 100 µm in this example. As seen in this figure, bumps 1-6 form the repeatable basic tile. For the characterization of this array, the following procedure was used.

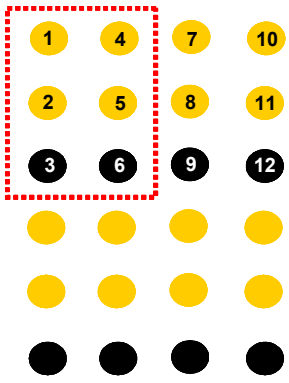

Figure 4. 9: Bump array consisting of 24 bumps.

1. EM and Equivalent Circuit Modeling of a Single Bump

Investigations to deduce optimal bump geometry for efficient EM modeling will first be presented, followed by a discussion on the effects of a power/ground bump on the RF/microwave characteristics of a signal bump.

Investigations to Deduce an Optimal Bump Configuration for Efficient EM Modeling

The shape of the bump used in an EM model of a flip chip configuration determines the duration of the field computation and memory used. In this section, a comparison is made between the commonly used bump shapes in EM modeling - spherical and cylindrical. From the results obtained, a choice will be made on the bump shape that will be used throughout this work.

EM Field Computation of a Single-Bumped Flip Chip – Comparison between Cylindrical and Spherical Bumps

In Figure 4. 10, 3D models of two single-bumped flip chip configurations used for EM field computations are shown. **The only difference between these models is the different shapes of bumps used – cylindrical and spherical. Both bumps have the same height (=75µm) and the same maximum diameter (=60 µm).** To reduce reflections at the transition, the width of the feeding lines were designed to match the dimensions of the bumps. These feeding lines used the back sides of the chip and substrate, respectively, as references since a PEC boundary was used. Wave ports were used as sources of excitations and the field computations were performed from 1GHz to 30 GHz. For both bump models, the same number of iterations was used as the convergence criteria.

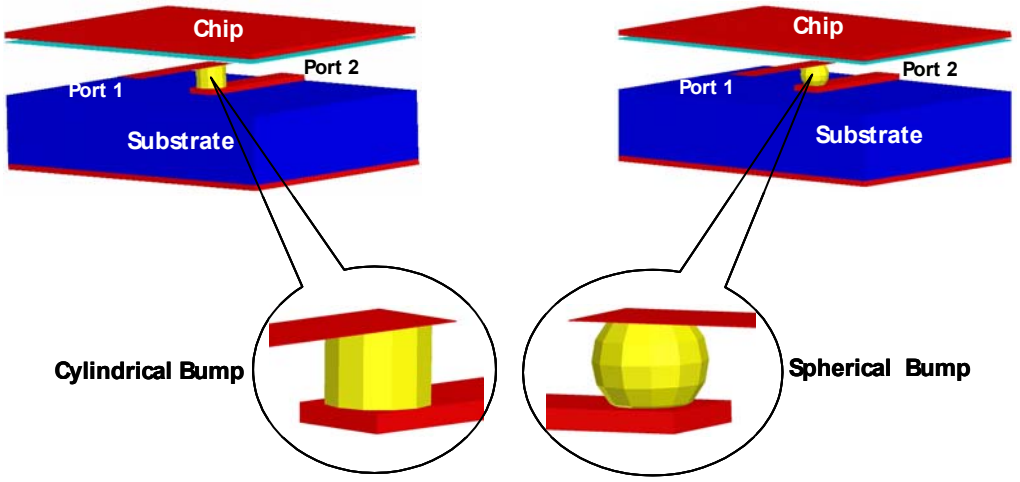

Figure 4. 10: 3D models of a single-bumped flip chip used for EM field computations. Each bump has a height and diameter of 75 µm and 100 µm, respectively. In this figure and all other figures in which a 3D model of a flip chip configuration is shown, the chip is suspended only for illustrative reasons.

At the end of the field computations, S-parameters describing the frequency-dependent behavior of each model were extracted. Since we are interested only in the RF/microwave characteristics of the bumps in this case (because the main objective of the investigations is to characterize a bump array), effects of feeding lines used for signal propagation into and out of the bump were de-embedded, leaving the bump with quadratic pads. However, for the development of the circuit model for the complete signal path, an equivalent circuit model of

the bump segment (not only the bump) is needed. Consequently, the bump with the required length of interconnecting traces necessary for the fields of HOMs to be negligible was considered after the field computation.

In order to understand the effects of bump shape on the field computations, the computed data extracted from both bumps was compared. As can be seen in Table 4. 1, the computation time for the flip chip configuration with a spherical bump is 43% more than that with a cylindrical bump and approximately 40% more memory was used. This can be attributed to the fact that, the difference in shape between the bumps leads to a difference in the entire problem region to be discretized, with the spherical bump demanding more computing power and hence, memory.

	Cylindrical bump	Spherical bump	Difference in %
Approx. computation time (CPU time)/ hours	4	7	43
Required memory	638 MB	1GB	40

Table 4. 1: Comparison of computed data for single-bumped flip chip models with cylindrical and spherical bumps.

Despite the huge difference in computation time and memory between the two bump configurations, the difference in their S-parameters is negligible, as can be seen in Figure 4. 11. Consequently, it would be expected that the difference between their inductance and resistance values also be very small. This will be verified in the next section.

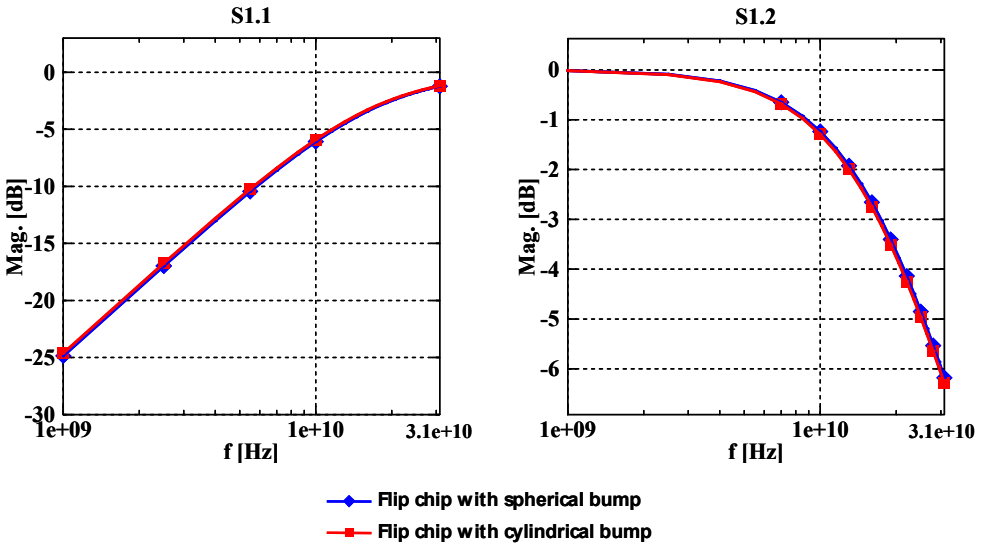

Figure 4. 11: Comparison of S-parameters from field computations of single-bumped flip chip models with cylindrical and spherical bumps.

Equivalent Circuit Modeling and Extraction of L and R

Based on the field computation results, two methods were used for the extraction of L and R. Both methods rely on the fact that a lumped element model (e.g., a π-network) is sufficient to capture the RF/microwave characteristics of the bump, since it is electrically short compared to the wavelength of the propagating signal. If approximately the same values are obtained for L and R using these two methods, then only the faster one will be used further in this work.

In the first approach, a linear circuit simulator (Ansoft's Serenade 8.5) was used, together with the π- model shown in Figure 4. 12.

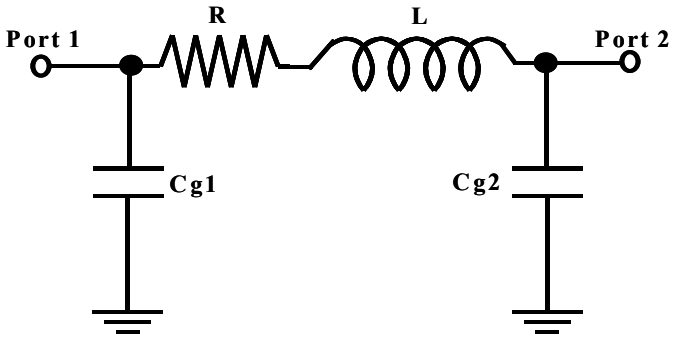

Figure 4. 12: Equivalent circuit model of a single bump.

In this circuit model, the bump is represented by the series connection of R and L. Based on the computed and de-embedded S-matrices of this bump, values of the circuit parameters were obtained through the gradient and random optimization processes. Approximately 26 pH and 16 mΩ (at 2.5 GHz) were obtained for the spherical bump, and 23 pH and 13 mΩ (at 2.5 GHz) for the cylindrical bump, respectively. Due to the extremely small optimization error obtained (approximately 0.01% for both cases), a very good correlation was obtained between S-parameters from the field computations and circuit optimizations, as shown in the example in Figure 4. 13.

Since the L-R model of the bump is independent of any substrate technology, there is no need to repeat the extraction process when a different substrate is used.

The capacitors connected to ground (Cg1 and Cg2) designate parasitic capacitances between the quadratic pads and the substrate/chip ground metalizations, respectively. Due to the very small chip thickness used (3 μm) and the small quadratic pad, a negligible capacitance value of 0.4E-06pF was obtained for Cg2. Approximately 0.1 pF was obtained for Cg1 (substrate thickness used = 229 μm).

Since this work focuses on the modeling of bumps, results of investigations performed for the characterization and optimization of pads will not be presented here.

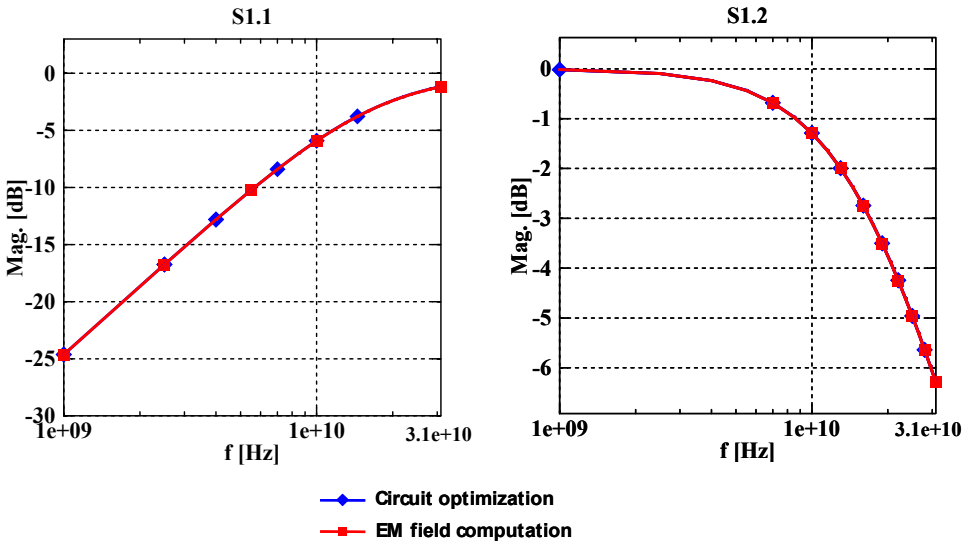

Figure 4. 13: Comparison of the reflection and transmission coefficients of S-parameters from EM field computation and circuit optimization of a single bump.

In the second approach to extract L and R, the computed and de-embedded S-matrices were converted to Y-matrices, from which components of the π-network were calculated for each frequency, as illustrated below:

- The computed S-parameters were first converted to Y-parameters using the following relationships:

$$Y_{11} = Y_0 \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \tag{4.4}$$

$$Y_{12} = Y_0 \frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \tag{4.5}$$

$$Y_{21} = Y_0 \frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \tag{4.6}$$

$$Y_{22} = Y_0 \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \tag{4.7}$$

- The Y-matrix for the π-network shown in Figure 4. 14 is given as

$$\overline{\overline{Y}} = \begin{bmatrix} y_1 + y_2 & -y_2 \\ -y_2 & y_2 + y_3 \end{bmatrix} . \tag{4.8}$$

$$But, \overline{\overline{Y}} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$$

$$\Rightarrow y_1 = Y_{11} + Y_{12} \tag{4.9}$$

$$y_2 = -Y_{12} \tag{4.10}$$

$$y_3 = Y_{22} + Y_{12} \tag{4.11}$$

- L and R were then derived from (4.10) as follows:

$$Since\ z_2 = R + j\omega L = \frac{1}{y_2},$$

$$\Rightarrow R = -\mathrm{Re}\left[\frac{1}{y_2}\right] \tag{4.12}$$

$$L = \frac{-\mathrm{Im}\left[\frac{1}{y_2}\right]}{2 * \pi * f} \tag{4.13}$$

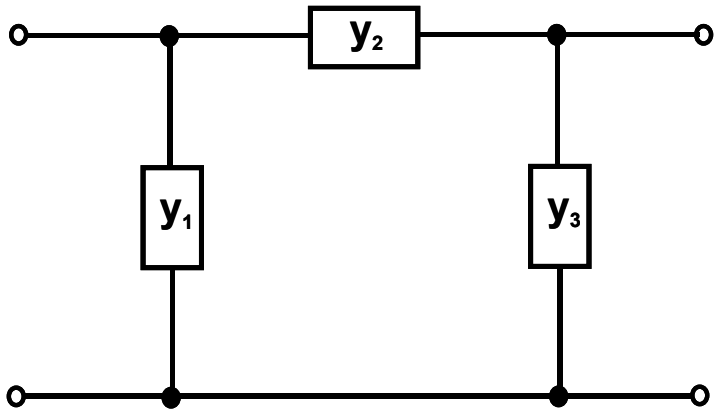

Figure 4. 14: π-network for implementing a 2*2 matrix.

- Finally, using (4.12) and (4.13), values of L and R were computed for all frequencies (1 GHz to 31 GHz). The variation of L and R with frequency is shown for both bumps in Figure 4. 15 and Figure 4. 16, respectively.

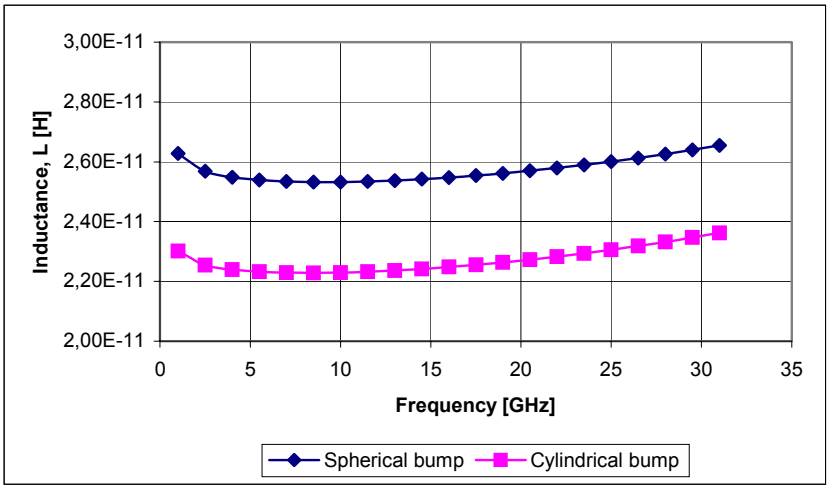

Figure 4. 15: Variation of L of cylindrical and spherical bumps with frequency. The slight increase in inductance with frequency from about 25GHz signifies a break-down of the quasi-static assumption considered in the pi- model used to extract the inductance.

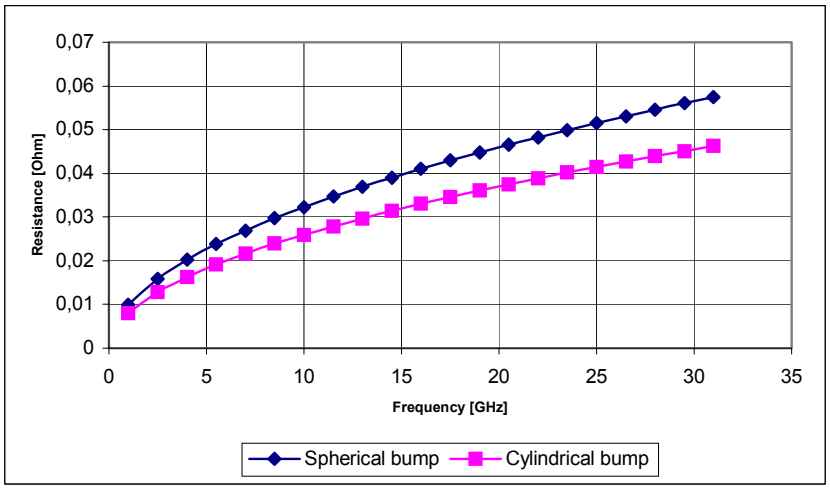

Figure 4. 16: Variation of R of cylindrical and spherical bumps with frequency.

- Since L is relatively constant within this frequency range for both cases (between 22.3pH and 23.6 pH for the cylindrical bump and between 25.3 pH and 26.5 pH for the spherical bump), an average value was calculated for each case. This resulted to approximately 23 pH and 26 pH for the cylindrical bump and spherical bumps, respectively – exactly the same values obtained using the circuit optimization approach.

- R, on the other hand, varies approximately proportional to the square root of frequency, as expected. Consequently, only single frequency values can be compared. Considering 2.5GHz as an example, approximately 16 mΩ and 13 mΩ were obtained for the spherical and cylindrical bumps, respectively – exactly the same values obtained using the circuit optimization approach.

Finally, based on the results obtained, the following conclusions were made:

- Any of the two approaches can be used to extract values of electrical parameters of a single bump. However, since the circuit optimization process is much faster, it will be used in the remaining sections of this chapter.

- Due to the extremely large differences in computation time and memory and the negligible differences in the extracted electrical parameters of both bumps, cylindrical bumps were chosen for further investigations in this work.

For all other investigations, a cylindrical bump of height and diameter of 50.8 μm was used. Using the circuit optimization approach, the following values were extracted.

Electrical Parameter	Approx. Value
L [pH]	18
R [mΩ] at 2.5 GHz	16
Cg1 [pF]	0.1
Cg2 [pF]	0.4 E-06

Table 3. 1: Values of electrical parameters of a cylindrical bump of height and diameter of 50.8 μm.

Effects of a Power/Ground Bump on the RF/Microwave Characteristics of a Signal Bump

In flip chip packages, power/ground bumps are used to provide power to the core of the chip as well as to shield sensitive signal paths from noise induced by neighboring circuitry. When placed at close proximity with signal bumps, they may serve as paths for the return current, thereby influencing the inductances of these signal bumps. The extend to which a power/ground bump affects the RF/microwave characteristics of signal bumps depends on quite a number of factors amongst which is the geometry of the bumps, material properties of the surrounding medium, frequency of propagating signal and their distance of separation.

To facilitate the characterization of bump arrays, values of electrical parameters extracted from any single signal bump must be able to be used to characterize any other signal bump in the array, wherever its position. However, this is only possible when the impact of neighboring power/ground bumps on the RF/microwave characteristics of a signal bump can

be neglected. In order to understand the effects of a power/ground bump placed at a distance of 100 µm away from the signal bump, the following approach was used:

- An EM model of a single signal bump (see Figure 4. 17 - left) was set-up and EM field computations were performed from 1 GHz to 30 GHz.

- Another EM model of a signal bump together with a power/ground bump (pitch=100 µm) was also set-up (see Figure 4. 17: 3D models of a single bump in the presence (right) and absence (left) of a power/ground bump - right) and field computations were performed under the same conditions and within the same frequency range as the single signal bump.

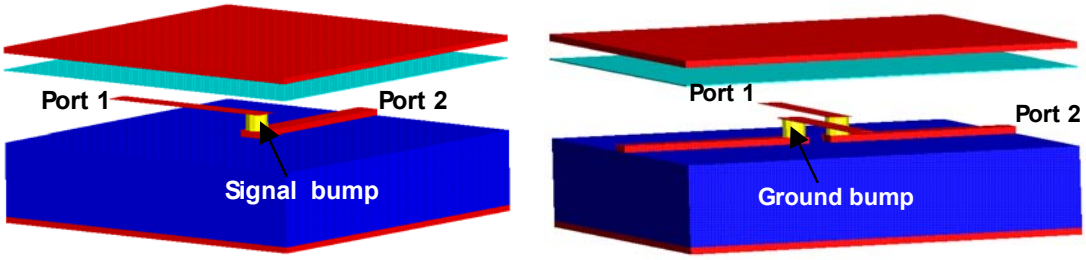

Figure 4. 17: 3D models of a single bump in the presence (right) and absence (left) of a power/ground bump

- S-parameters extracted from both field computations were de-embedded so as to exclude the effects of the feeding lines. A comparison between these S-parameters (see Figure 4. 18) revealed, that at a distance of 100 µm, effects of a power/ground bump on both the reflection and transmission coefficients of the S-parameters of a single signal bump can be neglected.

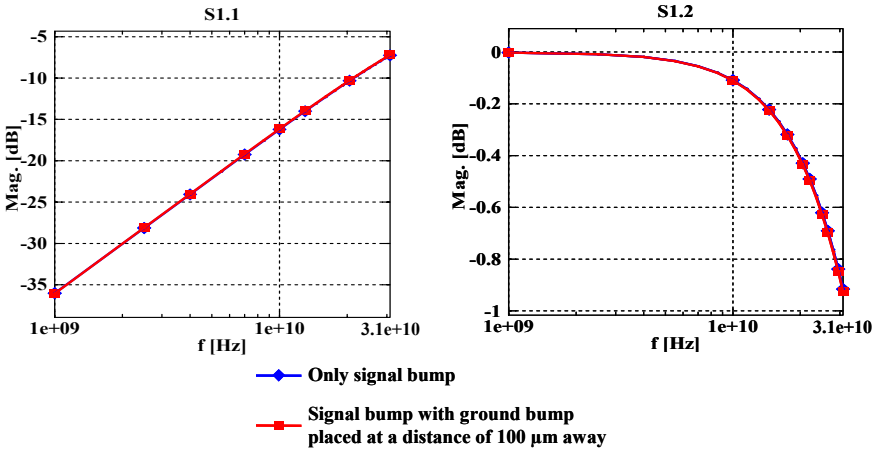

Figure 4. 18: S_{11} and S_{12} showing the negligible effects of a power/ground bump placed at a distance of 100 µm away from the signal bump.

- Based on the de-embedded S-parameters, values of L and R were extracted using the circuit optimization approach described in the previous section. As expected, values of R

were identical, but there was a slight difference between the extracted values of L. Approximately 18 pH was obtained as the inductance of the signal bump in the absence of a ground bump and approximately 16 pH in the presence of a ground bump. However, since the inductance of a bump is very small relative to other package components, this difference can be neglected.

From the results obtained in this section, it can be concluded that electrical parameters extracted from any single signal bump in the array can be used to characterize any other bump.

2. EM and Equivalent Circuit Modeling of Two-Coupled Bumps – Extraction of Cp, Mp, Cd and Md

After an extraction of L and R from a single bump, the mutual inductance (M) and coupling capacitance (C) between any two nearby bumps must also be accounted for. As shown in Figure 4. 9, these bumps can either be placed in parallel or diagonally to each other. EM coupling between both interconnect arrangements must be separately examined.

For both configurations, two different two-port EM models - "open" and "short" - were designed for the extraction of C and M, respectively. This technique was justified by comparing values of C and M obtained from a four-port configuration of two-coupled bumps with those separately extracted from two-port "short" and "open" models of two-coupled bumps, respectively. Using these two different two-port EM models instead of a single four-port model has the advantage that values of C and M obtained from field computations can be validated using RF measurement results of test samples performed with a two-port vector network analyzer, commonly found in most RF labs.

In the "short" arrangement M is dominant, because a metal plane places both bumps at ground potential. Since this hinders the existence of electric field lines between the bumps, the "short" model is not suitable for the extraction of C. Hence, the "open" model, in which both bumps are separated, was used for the extraction of C [106].

For the extraction of Cp and Mp from two parallel bumps, field computations were performed using the "open" and "short" EM models under the same conditions as the single-bumped flip chip. Based on the extracted S-parameters, equivalent circuit models for both configurations were developed.

The 3D models used as well as their corresponding circuit models are shown in Figure 4. 19 and Figure 4. 20, respectively. In these circuit models, values of electrical parameters obtained from a single bump were used to characterize each bump in these models. Through circuit optimization, approximately 5.4 pH and 1.6 fF were obtained for Mp and Cp, respectively. As can be seen in Figure 4. 21, a very good correlation was obtained between the S-parameters extracted from EM field computation and circuit optimization for the extraction of Mp from 1 GHz to 30 GHz. However, for the extraction of Cp, a good

correlation was obtained only up to 15 GHz, as shown in Figure 4. 22. A more complicated model is needed to extend the bandwidth above this frequency.

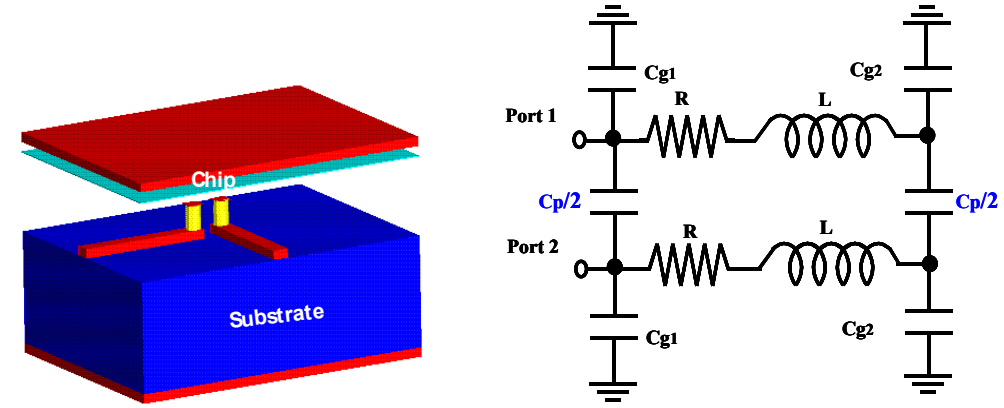

Figure 4. 19: 3D and equivalent circuit models of an "open" arrangement of two-coupled bumps flip chip.

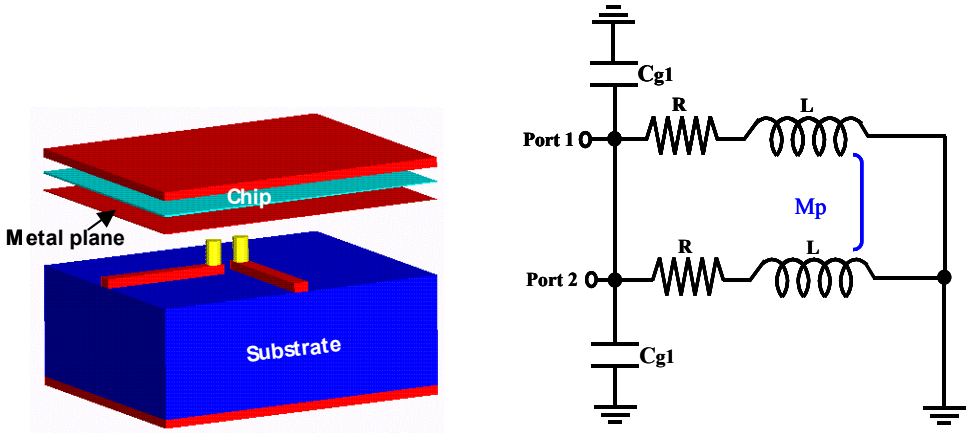

Figure 4. 20: 3D and equivalent circuit models of a "short" arrangement of two-coupled bumps flip chip.

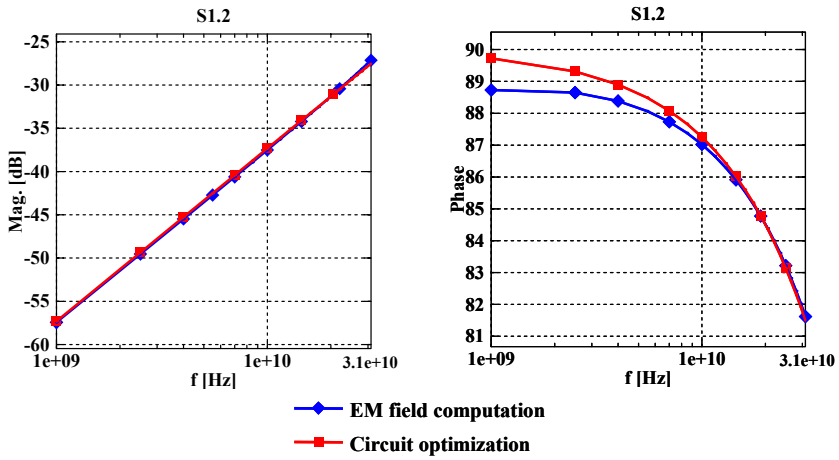

Figure 4. 21: Comparison of the magnitude and phase of S_{12} from EM field computation and circuit optimization of two-coupled bumps – "short" arrangement considered as an example.

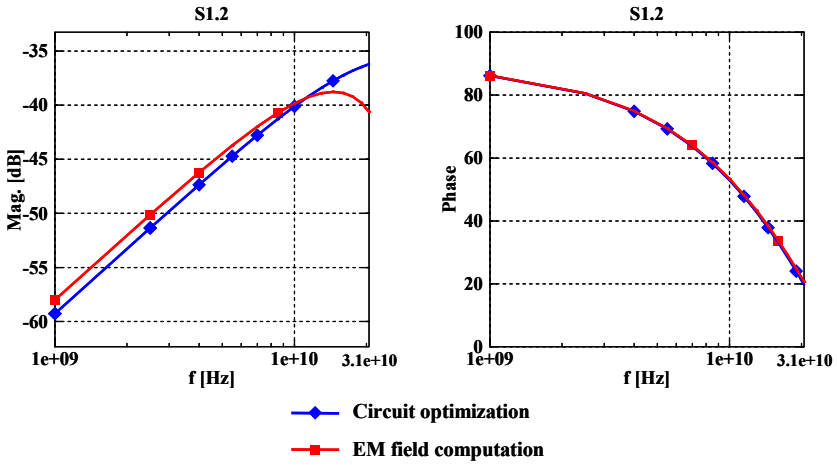

Figure 4. 22: Comparison of the magnitude and phase of S_{12} from EM field computation and circuit optimization of two-coupled bumps – "open" arrangement considered as an example.

For the extraction of Cd and Md from two diagonal bumps, a triangular configuration of three-coupled bumps was used. For illustrative reasons, only the bumps and their electrical coupling parameters are shown in Figure 4. 23. The 3D models of this triangular configuration were used to perform field computations under the same conditions as the single and two-coupled bumps flip chip. Based on the computation results, an equivalent circuit model, as shown in Figure 4. 24 was developed for the extraction of both Cd and Md. In this circuit model, Mp and Cp (represented as two times Cp/2), extracted from two parallel bumps, were used to characterize EM coupling between bumps 1&4 and bumps 4&5, respectively. Circuit optimizations were then performed (without considering Md) and 0.97 fF was obtained for Cd. For the extraction of Md, Cp/2s and Cd/2s were not considered, and the Cg2s were short-circuited. Approximately 2.9 pH was then extracted for Md. A good correlation was obtained between S-parameters from the circuit optimization, in which Md and Cd were extracted and those obtained from EM field computations of their respective models. In Figure 4. 25, this comparison is shown where the "short" model is considered as an example.

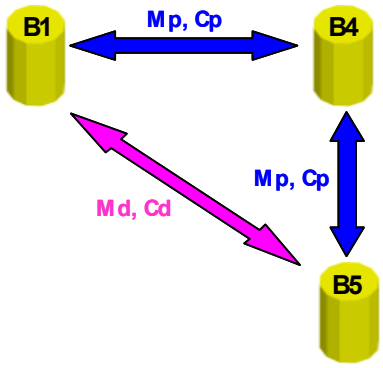

Figure 4. 23: Schematic representation of a triangular arrangement of three-coupled bumps and their coupling parameters.

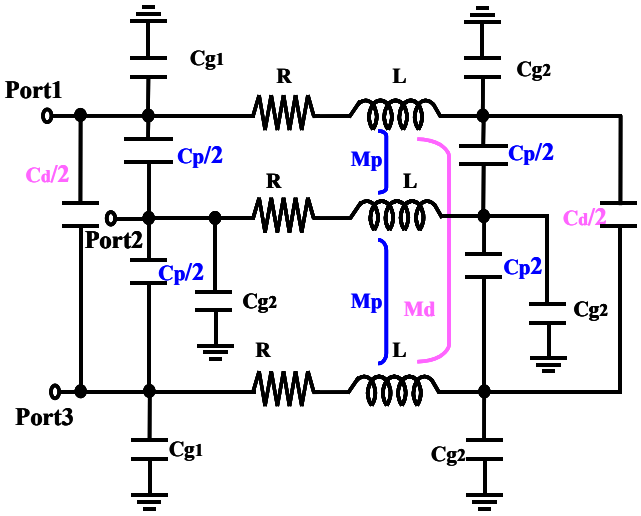

Figure 4. 24: Equivalent circuit model of three-coupled bumps.

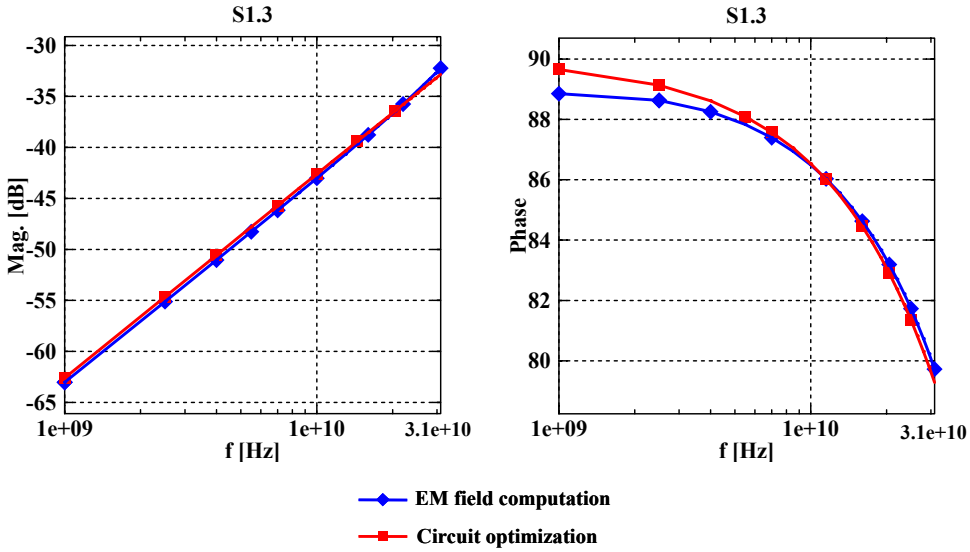

Figure 4. 25: Comparison of the magnitude and phase of S_{13} from EM field computation and circuit optimization of three-coupled bumps in a triangular arrangement – "short" model considered as an example.

3. Characterization of Three-coupled Bumps using Values of Electrical Parameters Extracted from Single and Two-coupled Bumps

Due to the superposition principle, which is as a result of the linearity property of field equations, all the results obtained so far can be applied to multiple bump configurations. In this section, values of electrical parameters extracted from single and two-coupled bumps will be used to characterize an arrangement of three-coupled parallel bumps. In order to reach this goal, the following procedure was used for both "short" and "open" configurations:

- EM field computations were performed using 3D models of three-coupled parallel bumps (schematic representation shown in Figure 4. 26). The equivalent circuit model presented in Figure 4. 24 was used for the circuit optimizations.

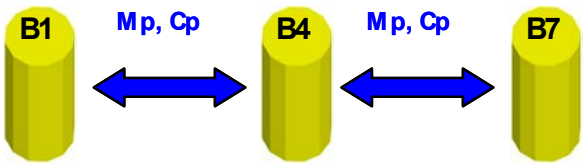

Figure 4. 26: Schematic representation of three-coupled bumps and their coupling parameters.

- Values of R, L and Cp and Mp characterizing a single bump and EM coupling between any two parallel bumps, respectively, were assigned to their respective components in the equivalent circuit model. C_{13} and M_{13}, substituting Cds and Mds in Figure 4. 24, and designating EM coupling between outwardly-placed bumps, were each assigned a value of zero, implying that this coupling is not considered.

- A comparison was then made between S-parameters extracted from EM field computation of three parallel bumps, and circuit analysis in which Cp and Mp were used to characterize three parallel bumps while C_{13} and M_{13} were set to zero. Results of this comparison are shown in Figure 4. 27, in which the "short" configuration is considered as an example. Due to symmetrical arrangement of the bumps, $S_{12} = S_{23}$.

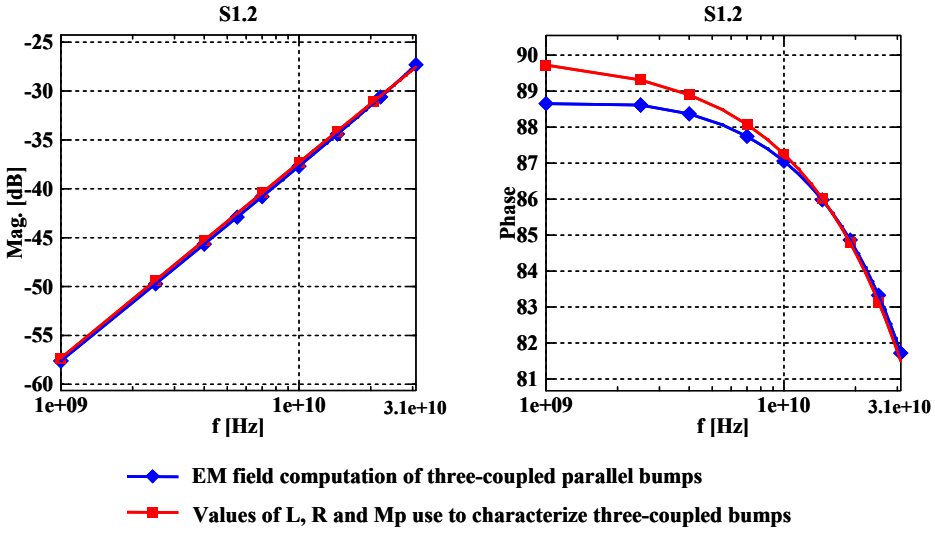

Figure 4. 27: Characterization of three-coupled parallel bumps using values of electrical parameters from single and two-coupled bumps.

- A good correlation was obtained between S-parameters from both sources. From this results, the following conclusions were drawn:

- Values of electrical parameters extracted from single and two-coupled bumps can be used to accurately characterize three-coupled parallel bumps.
- For typical bump pitches used in most high-speed packages, EM coupling between a bump and its "next but one" neighbor can be neglected. This coupling was neglected in this work because its values lie between –79dB at 1GHz and –44dB at 30 GHz, for the "open" arrangement and between –65dB at 1GHz and –34dB at 31 GHz, for the "short" configuration.

Investigating Passivity

Based on the criterion developed in section 3.1.2.2, the inductance matrix of the three-coupled bumps was tested for passivity. This matrix was first computed in [pH] as given below:

$$\overline{\overline{L}} = \begin{bmatrix} 18 & 5.4 & 0 \\ 5.4 & 18 & 5.4 \\ 0 & 5.4 & 18 \end{bmatrix}.$$

Then, its eigenvalues were also computed in [pH] to be

$$\lambda = \begin{bmatrix} 25.6368 & 18 & 10.3636 \end{bmatrix}.$$

Since all the eigenvalues are greater than zero, it implies that the inductance matrix of the three-coupled parallel bump is passive. A passive circuit is stable, can not generate energy and can be connected to other passive circuits without risk of instability.

4. Characterization of Bump Arrays using Values of Electrical Parameters Extracted from Single and Two-coupled Bumps – Validation of Modeling Methodology

Equipped with values of the required electrical parameters as well as a comprehensive understanding of the RF/microwave behavior of single and coupled signal bumps in the presence and absence of ground/power bumps, we are now set to validate the proposed modeling methodology for bump arrays. An array consisting of four coupled bumps was chosen to validate the methodology because it forms the basic repeatable tile of the signal bumps as shown in Figure 4. 9.

EM field computations using 3D models of this array were performed and its equivalent circuit model was developed. A schematic view of the bump array and its equivalent circuit model are shown in Figure 4. 28 and Figure 4. 29.

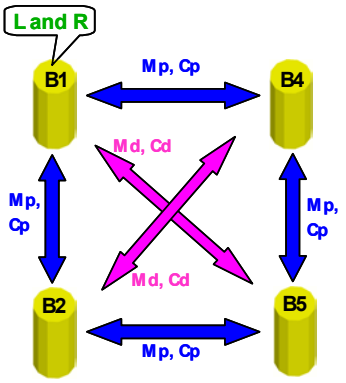

Figure 4. 28: Schematic representation of an array of four-coupled bumps, showing all electrical parameters needed for its characterization.

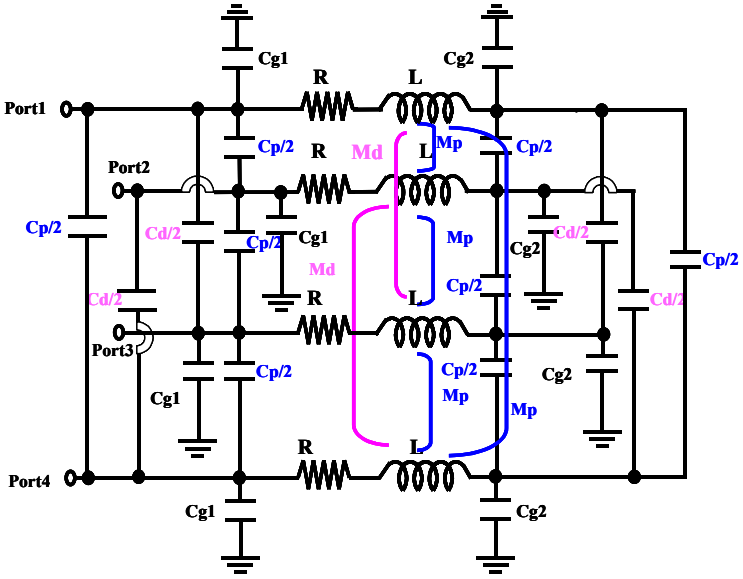

Figure 4. 29: Equivalent circuit model of an array of four-coupled bumps.

To each electrical component in this model, values of electrical parameters obtained from a single and two-coupled bumps flip chip interconnects were assigned as follows:

- L and R from a single bump were used to characterize each bump in the array,
- Cp and Mp extracted from two parallel bumps were used to characterize EM coupling between any two parallel bumps in the array i.e., between bumps 1&2, 2&5, 4&5 and 1&4.
- Cd and Md obtained from two diagonal bumps were used to characterize EM coupling between any two diagonal bumps in the array i.e., between bumps 1&5 and bumps 2&4.
- A linear circuit analysis was then performed (no optimization) and the resulting S-parameters characterizing the bump array were extracted. A comparison was then made

between these S-parameters and those obtained from EM field computation of the bump array. This comparison is presented in Figure 4. 30 and Figure 4. 31 in which the "short" configuration is considered as an example. An excellent correlation was obtained.

This good correlation was also observed when the "open" configuration of four-coupled bumps was considered. It confirms the fact that a complete bump array can be completely characterized using electrical parameters extracted from single and two-coupled bumps, thus validating the modeling methodology [107] - [109].

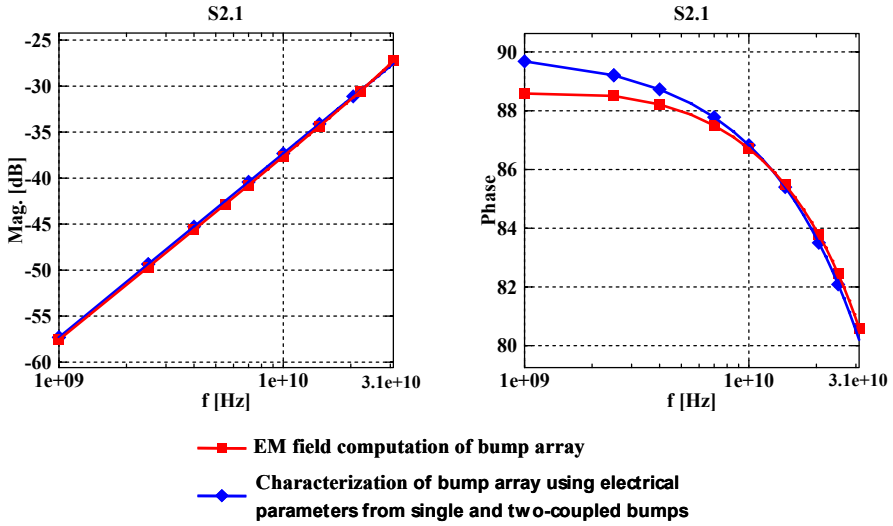

Figure 4. 30: Characterizing a bump array using electrical parameters from a single and two-coupled flip chip interconnects: S_{21} considered for the "short" arrangement as an example.

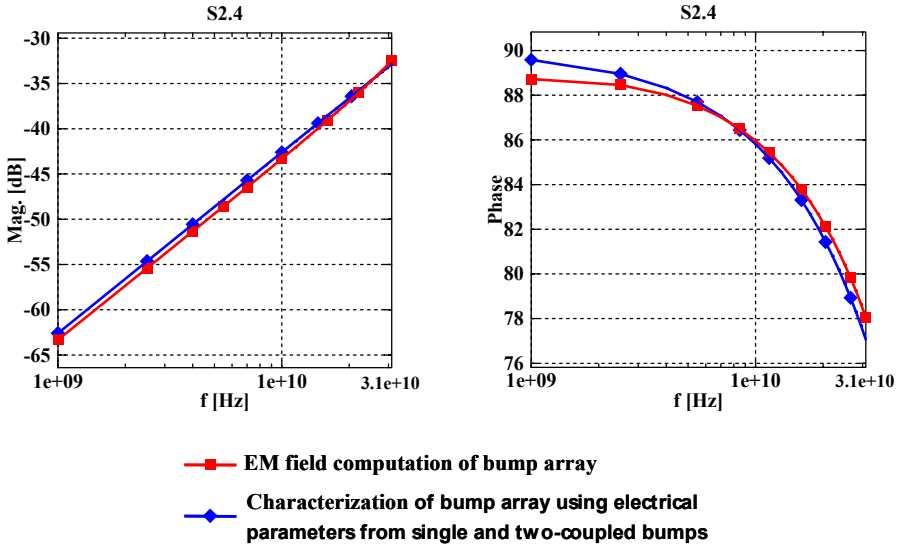

Figure 4. 31: Characterizing a bump array using electrical parameters from a single and two-coupled flip chip interconnects: S_{24} considered for the "short" arrangement as an example.

4.2.2.2 Package/Board Components

The substrate (interposer) was designed as a low-cost FR4 material (εr=4.2, tanδ=0.007). It consist of four metal layers (see Figure 4. 32), with core and prepeg thickness of 150µm and 100µm, respectively. The first and fourth layers were used for signal routing, while the inner layers served as ground/power planes. As a result of the layer stack-up, the package traces were realized as microstrip lines (width=175 µm), with bends so as to facilitate the routing. For an interconnection of the signal layers, through-hole vias were used.

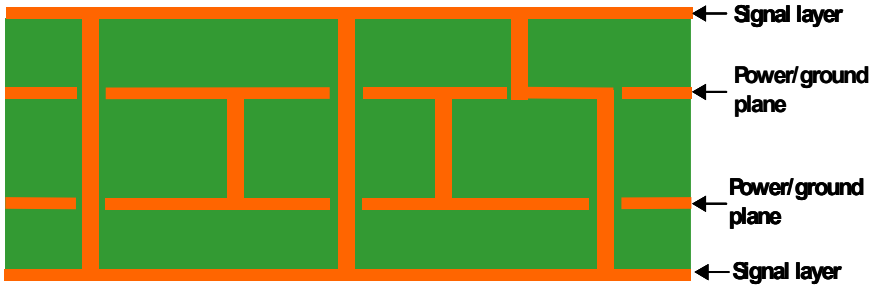

Figure 4. 32: Schematic view of the four-layered substrate that was used as the interposer.

In the following subsections, the modeling methodology presented in section 3.1.2.1 will be used to develop wideband circuit models for bends and vias.

1. Modeling of Multiple Bend Segments

In order to model multiple bends along a signal path, an accurate model of a single bend segment must first be developed. Once this model is obtained, it can then be cascaded to generate a model for multiple bend segments. The development of an accurate model of the bend segment commences the definition of the end of discontinuity effects caused by the bend, so as to accurately define the length of the segment. In section 4.2.1, it was found that the electrical boundaries of a bend at 30 GHz is at a distance of 0.477 mm away from the physical boundary of the bend, implying that a minimum of this length must be considered for the field computations. In this case, a distance of 1mm was used. Based on the field computation of the 90° bend (using its 3D model shown in Figure 4. 33), S-parameters were extracted. The circuit model shown in Figure 3.6 was used for the extraction of the circuit parameters of the bend segment.

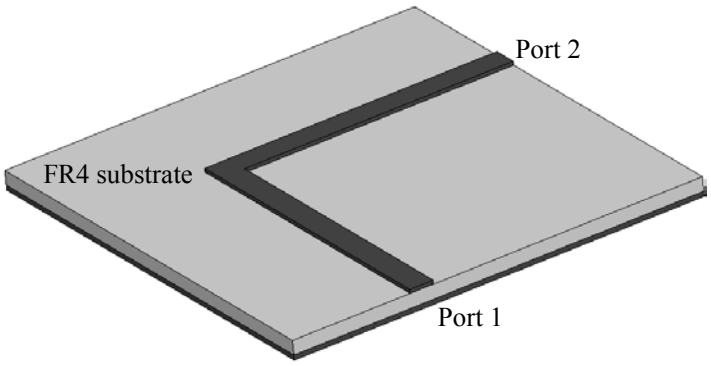

Figure 4. 33: 3D model of a 90° bend segment that was used for the field computations.

Following the methodology presented in section 3.1.2.1, approximately 15 pH, 23 fF and 12 mΩ (at 5.5 GHz) were obtained for the inductance, capacitance and resistance of the bend discontinuity, respectively. As can be seen in Figure 4. 34, a good correlation was obtained between S-parameters from the circuit optimization and the field computation of the bend segment for frequencies up to 30 GHz. In this case, the interconnecting segments were modeled using transmission line models. Depending on the frequency range of application, the circuit model in Figure 3.6 can be simplified by neglecting some of the electrical parameters.

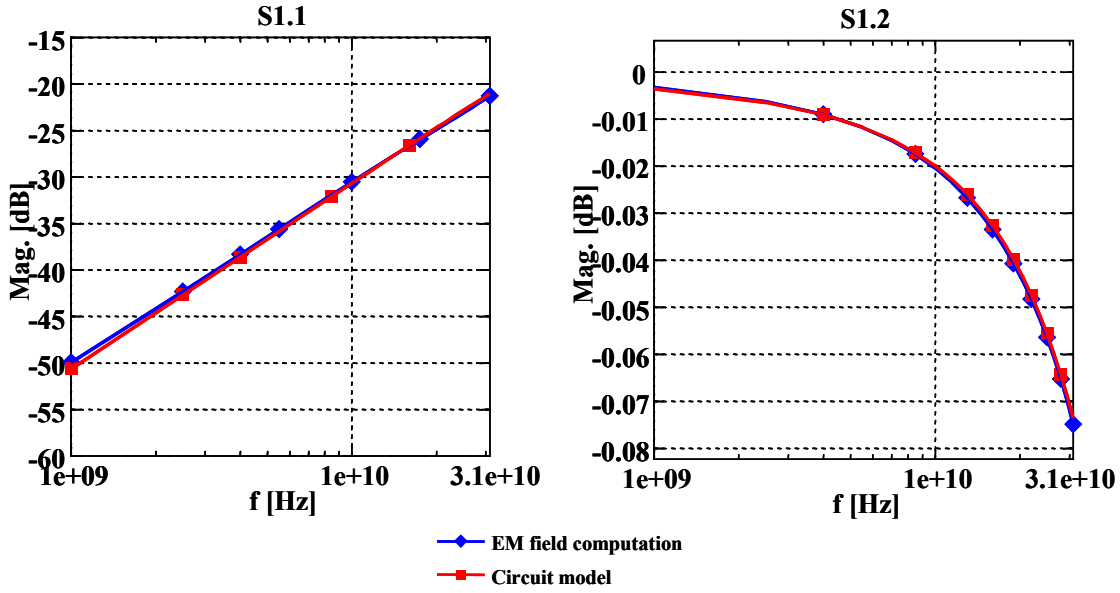

Figure 4. 34: Comparison of the reflection and transmission coefficients of S-parameters obtained from EM field computation and circuit optimization for the extraction of electrical parameters of a 90° bend.

Now, to prove that an EM as well as a circuit model of multiple bend segments can be deduced once the end of the discontinuity effect of a single bend is defined, the following approach was used:

Consider a signal path consisting of two 90° bends shown in Figure 4. 35. The distance between the bends is 2mm. The distance from each bend to the end of the substrate is 1mm such that the entire length of the signal path is 4 mm. Based on the definition of the electrical boundaries of a bend segment, this signal path was broken-down into two bend segments and field computations were performed only for a single segment. The resulting S-matrices were then converted to T-matrices, multiplied together and then re-converted to generate the S-matrices of the entire signal path. This leads to a great reduction in the computation time and memory used. To serve as a reference, EM field computation of the complete path was also performed and S-parameters extracted.

Based on S-parameters extracted from a single bend segment, an equivalent circuit model was developed. A cascade of this single model to characterize the complete signal path is shown in Figure 4. 36.

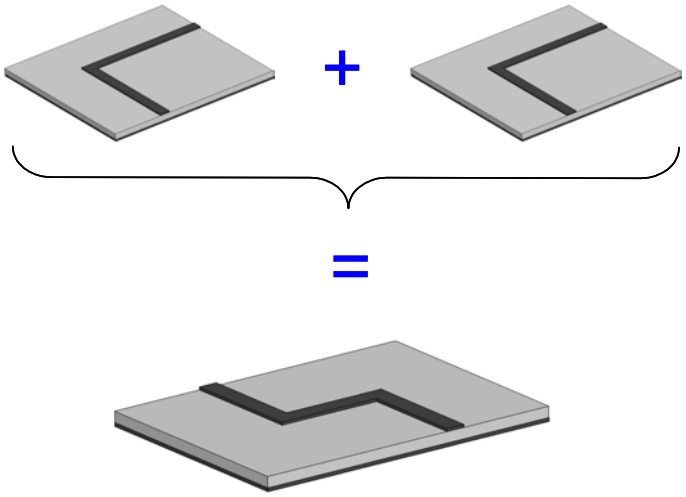

Figure 4. 35: 3D models of microstrip package traces with 90° bends.

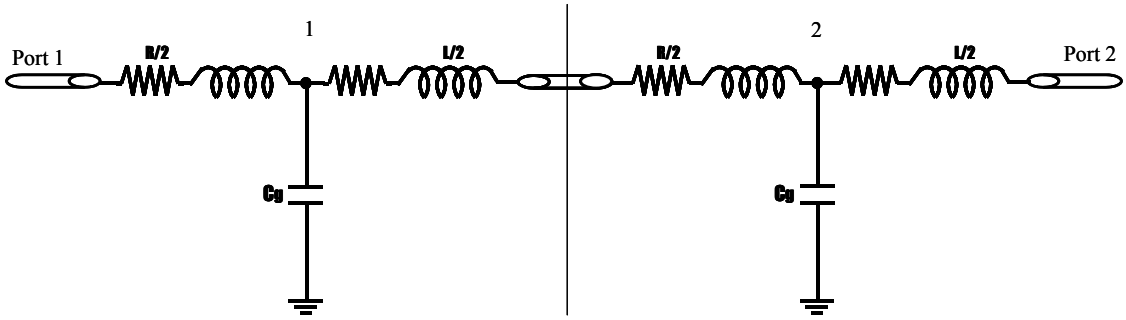

Figure 4. 36: Cascade of circuit models from two 90° bend segments to characterize the complete path.

S-parameters extracted from this cascade were compared with those obtained from a cascade of the EM models of the single bend segments to characterize the path as well as with those obtained from the field computation of the complete signal path. As can be seen in Figure 4. 37, a very good correlation was obtained between these curves, thus confirming the fact that a cascade of models of single bend segments can be used to model a complete signal path. The resonance that occurs at about 25 GHz signifies the fact that at this frequency, the length of the signal path is about half the wavelength of the propagating signal.

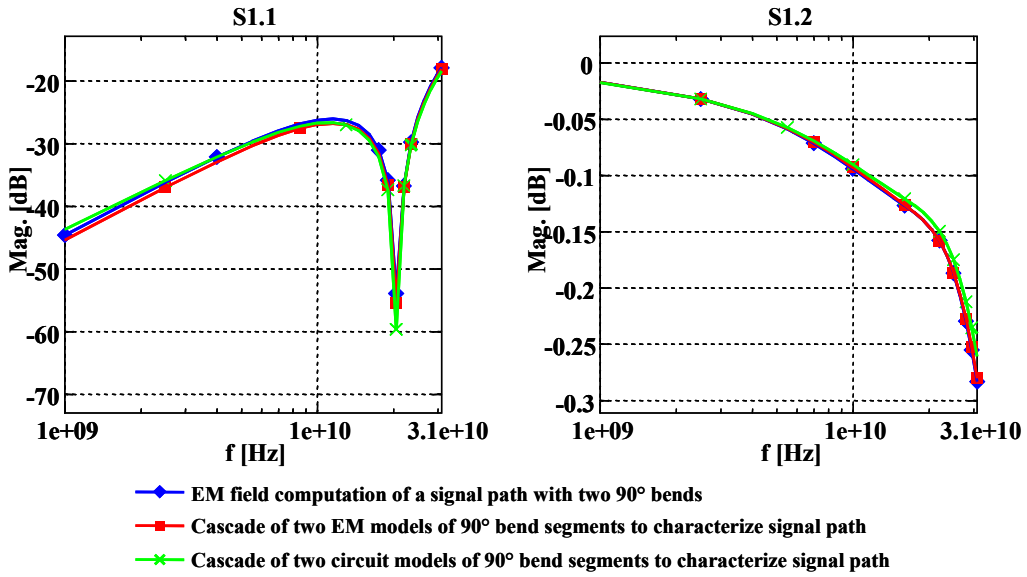

Figure 4. 37: Comparison of S_{11} and S_{12} from EM field computation of a signal path with two 90° bends, a cascade of two EM models of 90° bend segments and from a cascade of two circuit models of 90° single bend segments to characterize the entire signal path.

In cases where two discontinuities are placed very close together, the HOMs excited from one discontinuity couple to the second discontinuity and the effects of both discontinuities can not be separated. In such cases, both discontinuities should be modeled as one discontinuity.

2. Modeling of Vias

Just like any other package discontinuity, the end of the discontinuity effect of the via was first defined before the actual EM field computation was carried out. The methodology used and results obtained were presented in section 4.2.1.

Based on the extracted S-parameters, an equivalent circuit model for the via was developed (see Figure 4. 38).

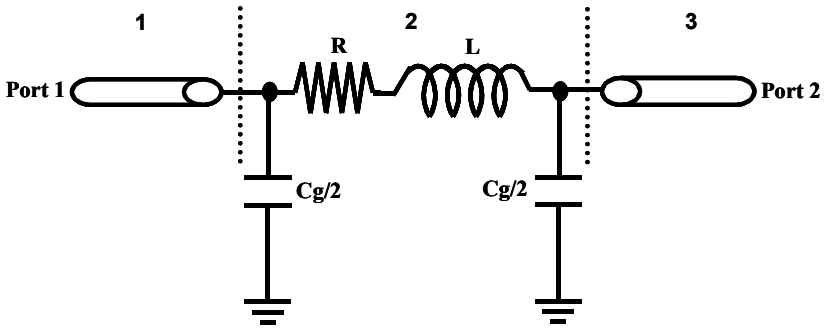

Figure 4. 38: Equivalent circuit model of a via segment.

The systematic approach applied for bends in the previous section was also used here to extract the circuit parameters of the signal via. Approximately 148 pH, 28 mΩ (at 25GHz) and 85 fF were obtained for L, R and Cg/2, respectively. As can be seen in Figure 4. 39, the proposed circuit model can accurately account for the RF behavior of the via up to 25 GHz. There slight difference of less than 0.4 dB between the circuit optimization and field computation results at frequencies between 25 GHz and 30 GHz is as a result of the fact that at such frequencies, the lumped element model becomes inadequate to capture the effects of the via

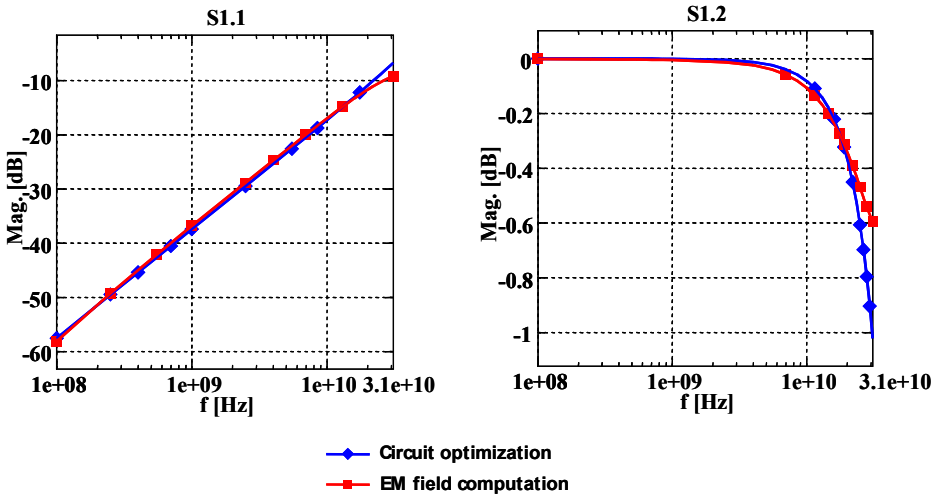

Figure 4. 39: Comparison of S_{11} and S_{12} from EM field computation and circuit optimization of a through-hole via (microstrip-microstrip transition).

When two signal vias are placed in close proximity, there is an interaction of their EM fields, leading to cross-talk and other SI problems. In order to capture this coupling, accurate circuit models of two-coupled signal vias are needed within the frequency range of interest.

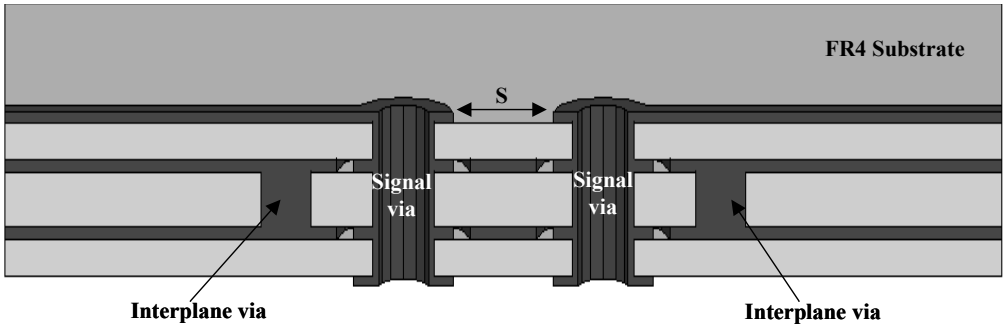

Figure 4. 40: Cross-sectional view of a 3D model of two-coupled signal vias and their interplane vias used for return current. For illustrative reasons, only two interconnecting traces are shown and the other two are left out.

For the development of such models, EM field computations were performed using the 3D model shown in Figure 4. 40. From the field computation results, an equivalent circuit model (see Figure 4. 41) was developed. In this model, values of electrical parameters extracted from a single signal via were used to characterize each of the signal vias. A linear circuit optimization process was then carried out using the S-parameters obtained from the EM field computation of the two-coupled signal vias and values of coupling capacitance (Cc) and mutual inductance (M) between the vias were obtained. Considering a pad-pad separation, S, of 0.54 mm, approximately 9 pH was obtained. At this distance of separation, Cc can be neglected because it is smaller than 0.001 fF. To validate the extracted circuit model, a comparison was made between S-parameters obtained from the optimization process and the field computation results. As can be seen in Figure 4. 42, a good correlation was obtained between S-parameters from both sources.

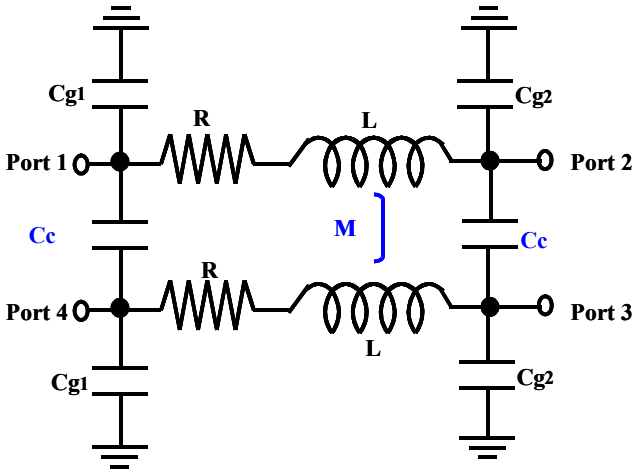

Figure 4. 41: Circuit model used for the extraction of Cc and M from two-coupled vias.

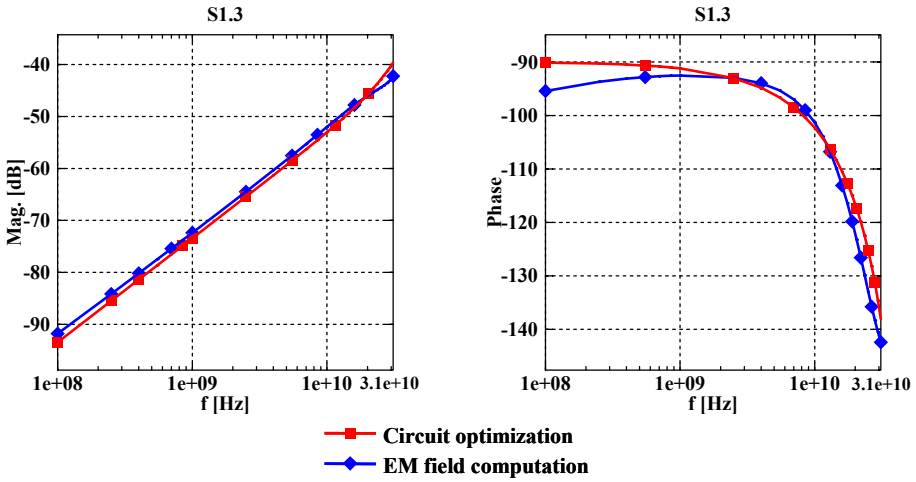

Figure 4. 42: Comparison coupling parameters extracted from EM field computation and circuit optimization of two-coupled signal vias (S= 540 µm): S_{13} considered as an example.

4.2.2.3 Package-to-Board Interconnects

BGA balls are used for the interconnection of the package onto the board. In most BGA packages, they are the biggest interconnecting components along the signal path and hence, cause the greatest signal distortion. Apart from the difference in their sizes, BGA balls and flip chip interconnects are very identical. Consequently, the modeling approach used for flip chip interconnects in arrays was also used for BGA balls, and will there fore not be repeated here. Only the most important results will be presented in this section.

Like any other component along the path, the modeling approach started with investigations to define of the end of discontinuity effect caused by a BGA ball. Considering a ball of max. diameter and height of 600 µm and 500 µm, respectively, it was found that at a distance of 1.924 mm away from the ball pad, fields of HOMs exited at the pad vanish. From this distance, the fundamental mode continues undisturbed. Figure 4. 43 shows a side view of a BGA ball, where h stands for the ball height, b_d, ball diameter and P_d the pad diameter (=500 µm in this work). Figure 4. 6 depicts the variation of $|S_{11}|$ with distance away from the pad of the BGA ball.

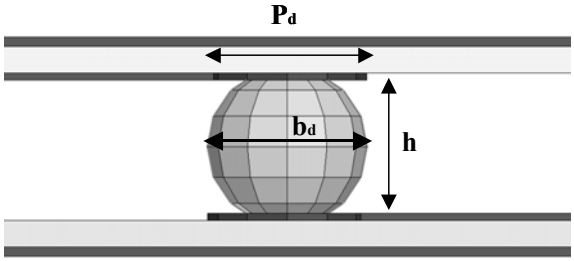

Figure 4. 43: Side view of BGA ball.

For the extraction of electrical parameters of a single BGA ball, the 3D model shown in Figure 4. 44 was used. The ground ball shown in the model served as the return path of the

signal current. Based on the EM field computation results, the circuit parameters of the ball were extracted using the same circuit model as for vias (see Figure 4. 38). Approximately 0.2 nH and 16 mΩ were extracted for L and R, respectively. 0.02 pF was also obtained as the total capacitance between the ball pads and the reference planes. A comparison between S-parameters obtained from the circuit optimization in which values of the circuit parameters were extracted and from the field computation is shown in Figure 4. 45. As can be seen in this figure, a very good correlation was obtained.

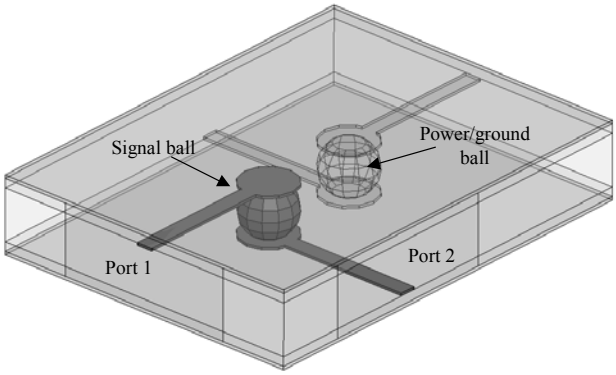

Figure 4. 44: 3D model of BGA ball that was used for the EM field computations.

To extract the coupling parameters between two-coupled signal balls, EM field computations and circuit optimizations were performed using the models shown in Figure 4. 46 and Figure 4. 41, respectively. For a pitch of 0.5 mm, approximately 0.2 fF and 0.4 nH were extracted for Cc and M, respectively. Figure 4. 47 shows a good correlation between S-parameters obtained from EM field computation of the coupled balls, and from the circuit optimization process in which the coupling parameters were extracted. This validates the circuit model used.

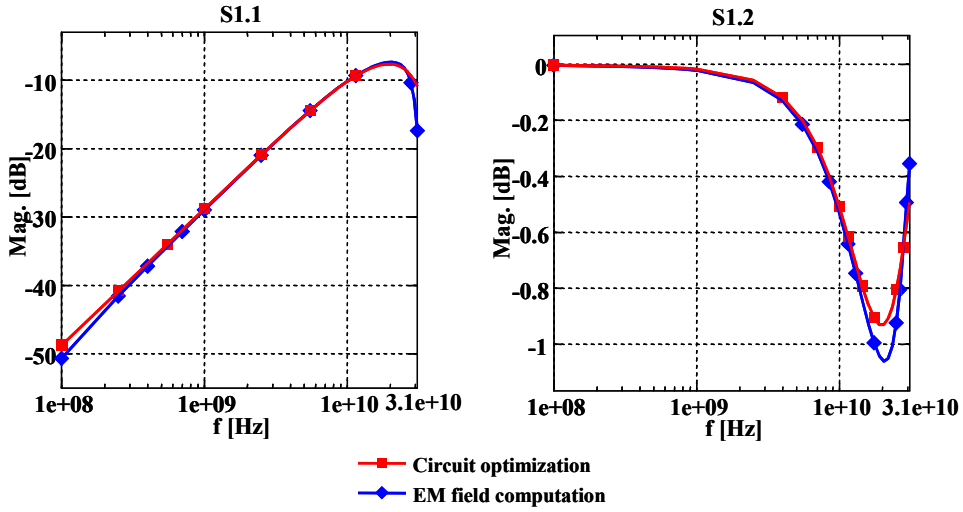

Figure 4. 45: Comparison of S_{11} and S_{12} extracted from the field computation and circuit optimization processes used for the extraction of electrical parameters of a BGA ball.

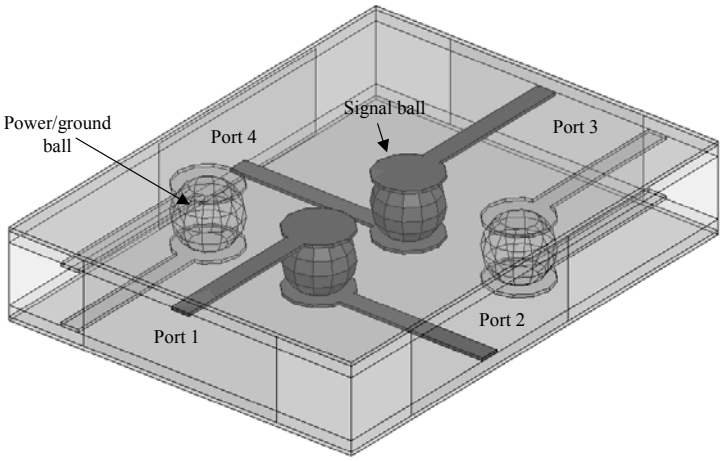

Figure 4. 46: 3D model of two-coupled signal BGA balls and their respective return paths.

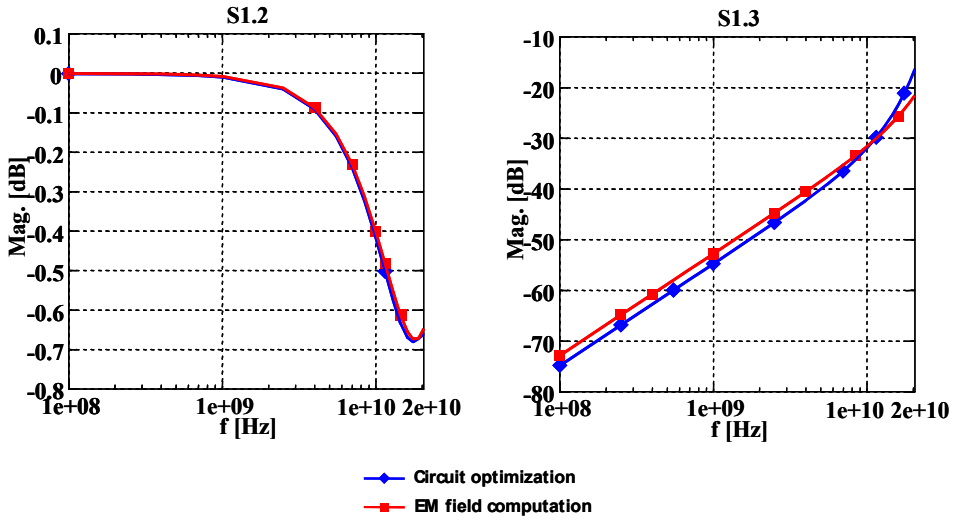

Figure 4. 47: Comparison of S_{12} and S_{13} extracted from the field computation and circuit optimization for the extraction of coupling parameters from two BGA balls.

Using the equivalent circuit model of coupled BGA balls (see Figure 4. 41), effects of the variation of the pitch on Cc and M was studied and the results obtained are shown in Figure 4. 48. and Figure 4. 49. As expected, the coupling capacitance falls rapidly with increasing pitch. The inductive coupling on the other hand remains strong even at a pitch of 1mm. By increasing the distance of separation between the balls as well as using balls with smaller ball and pad dimension, this coupling can be reduced to within acceptable limits.

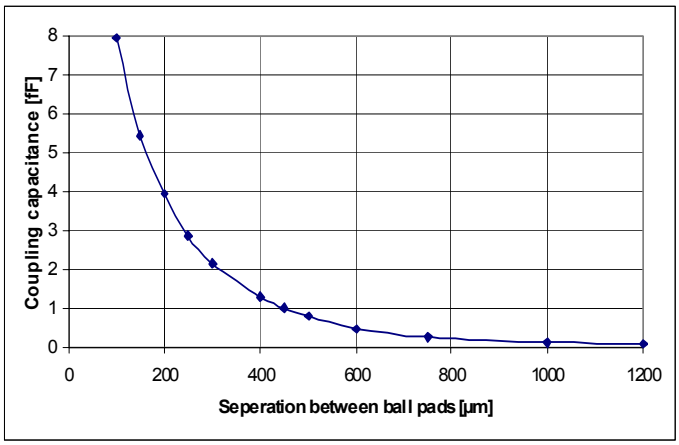

Figure 4. 48: Variation of Cc with pitch between two signal BGA balls.

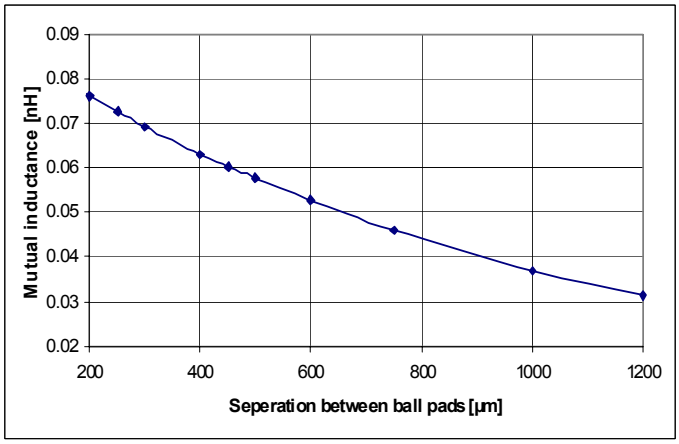

Figure 4. 49: Variation of M with pitch between two signal BGA balls.

4.2.2.4 Comparison of Values of Electrical Parameters Extracted from Package/Board Components using Conventional Methods and the Method Proposed in this Work

Since no method has been developed up till date to define the electrical boundaries of geometrical discontinues, values of electrical parameters extracted for these discontinuities so far using modeling techniques in the published literature (e.g., in [52] – [88] and [110]-[111]) account only for the field distortion that occurs within the physical boundaries of a discontinuity (e.g., within AA_1 in Figure 3. 5) and fail to capture the effects of the HOMs that extend beyond such boundaries. Consequently, the accuracy of these methods is very limited, because the reactive energy stored by HOMs, as demonstrated in section 3.1.2.1, can not be accounted for. Hence, the effects of these discontinuities on the RF performance of packages and boards are underestimated and thus, can not be accurately compensated for, during the design phase. In the following paragraph, the error made using conventional modeling techniques to extract the values of electrical parameters will be estimated, using a 90° bend as an example.

Consider the following formulas given in, for example [110], and used for the computation of L and C of a bend.

For $w/h < 1$

$$\frac{C_{bend}}{w} = \frac{(14\varepsilon_r + 12.5)\,w/h - (1.83\varepsilon_r - 2.25)}{\sqrt{w/h}} \tag{4.14}$$

For $w/h \geq 1$

$$\frac{C_{bend}}{w} = (9.5\varepsilon_r + 12.5)\,w/h + 5.2\varepsilon_r + 7.0 \tag{4.15}$$

$$\frac{L}{h} = 100\left(4\sqrt{(w/h)} - 4.21\right) \tag{4.16}$$

where C_{bend} is the capacitance of the bend given in [pF], L is the inductance in [nH], w is the width of the conductor, h is the substrate thickness and ε_r is the dielectric constant of the substrate.

These formulas were used to compute L and C for the bend geometry shown in Figure 4. 33. In this case, w=175 μm, h=100 μm and ε_r=4.2. Consequently, (4.15) was used for C_{bend}, since $w/h = 1.75 > 1$. The calculations yielded approximately 17 fF and 10 pH for C and L, respectively. These values were compared with values of L and C extracted using the novel methodology developed in this dissertation. As can be seen in Table 4. 2 approximately 26% error is made in the calculation of C and 33% error in L, if the conventional methods are used, due the reasons given above. This error increases proportionally to the number of discontinuities and since modern chip packages and PCBs consist almost entirely of geometrical discontinuities, conventional modeling techniques can not be used to accurately predict the impact of these discontinuities, especially for RF and high-speed applications.

	Extracted using conventional methods	Extracted using novel method	Error made if conventional methods are used [%]
L[pH]	10	15	33
C[fF]	17	23	26

Table 4. 2: Comparison of L and C values of bends extracted using conventional methods and the novel method developed in this dissertation for frequencies up to 30 GHz.

4.2.3 Wideband Model for Complete Signal Paths in a BGA Package Module

In Figure 4. 50, a wideband model of the complete signal path (chip-to-board) is shown. This model was obtained by cascading all the separately developed models of the various interconnecting segments along the complete signal path. A comparison between S-parameters extracted from the cascade of the validated models from different segments and from EM field computation of the entire package, in which only one signal path was considered, is depicted in Figure 4. 51. This comparison shows a good correlation between both curves, thus validating the equivalent circuit model developed for complete signal path in a BGA package module. It should be noted, that for the development of this circuit model, only discontinuities and their connecting traces just long enough to allow the HOMs to decay, were considered. However, in situations where very long uniform package/board traces are used to interconnect the discontinuities, the equivalent circuit model of the complete path must be extended. This can be achieved by simply inserting transmission line models (that characterize the actual trace configuration) between the circuit models of any two discontinuities [112] – [114].

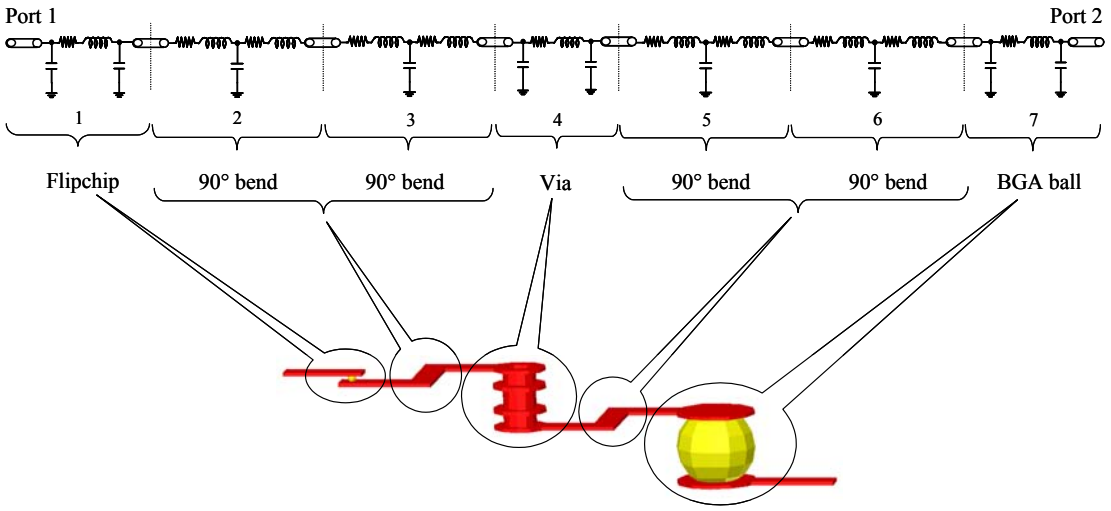

Figure 4. 50: Equivalent circuit model of the complete signal path (chip-to-board) in a BGA package. For illustrative reasons, the chip and dielectric layers of the interposer and board are not shown.

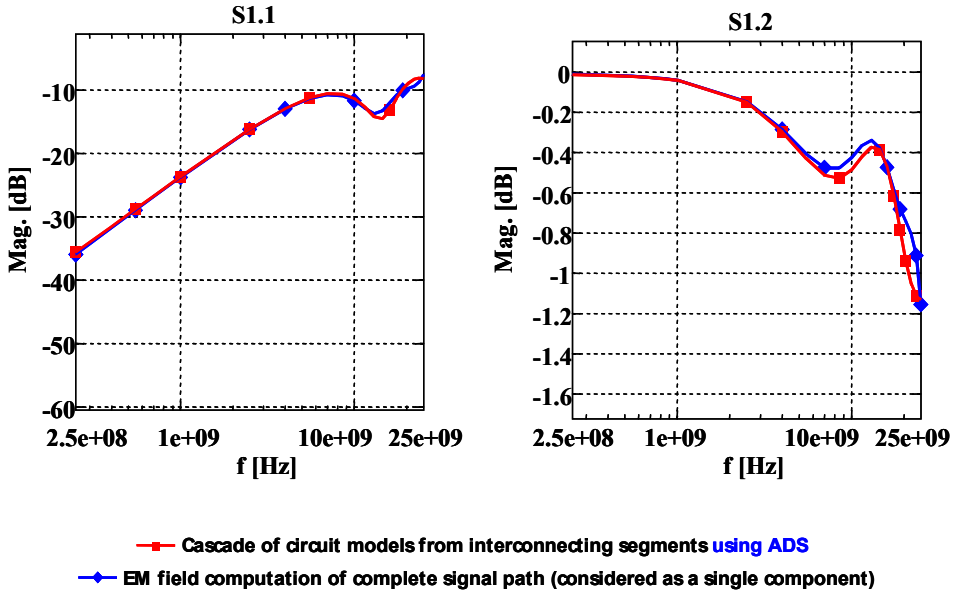

Figure 4. 51: Comparison of S-parameters obtained from equivalent circuit model and EM field computation of complete signal path.

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Chapter 5

Experimental Validation

5.1 Design of Test Samples

Since all the wideband models developed in the previous chapter are based on numerical electromagnetics, they must be experimentally validated. For this reason, test structures were designed, fabricated and measured. In this section, the methods used to design each package/board component will be discussed.

5.1.1 Chip-to-Package Interconnections

Figure 5. 1 presents a schematic representation of the layout of single and two-coupled bumps. SBFC designates single-bumped flip chip and CBFC stands for two-coupled bumps flip chip structures.

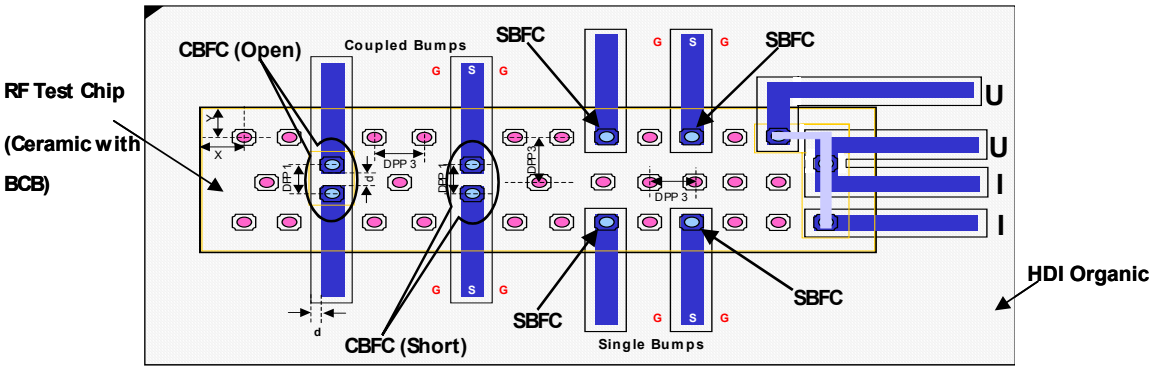

Figure 5. 1: Test sample design showing single and coupled flip chip interconnects of HDI-organic substrates.

To facilitate the placement of probes during RF measurements, feeding lines were included in the design. However, since the bump discontinuity to be characterized is too small, great care was taken so as to prevent parasitic effects of these feeding lines from dominating the RF behavior of the bump. This was achieved by designing single bumps to have only one feeding line and the other end of the bump was grounded. The two-coupled bumps were designed as

"short" and "open" for reasons already discussed in section 4.2.2.1. In order to remove the effects of the feeding lines, de-embedding structures must be used. They were also designed on the substrate.

The test chips were fabricated by thin-film processes on ceramic substrates. All metal layers were formed by sputtering, electroplating and etching of the plating base. Copper was chosen as the first metal layer directly on the substrate, followed by BCB layer as dielectric with via holes to connect the ground, second metal layer of copper with signal lines and a second BCB layer to serve as solder mask. Eutectic PbSn63 solder was plated as mushroom type and reflowed for bumping. Three plated solder heights (55, 75 and 100 µm) were chosen to realize all bond heights required for DOE in combination with the size of the substrate pads.

Flip chip bonding was performed on an organic HDI board with Cu, Ni and flash Au metallization. Pads were solder masked-defined, designed with diameters of 150, 175 and 200 µm. Figure 5. 2 depicts an image of the HDI panel.

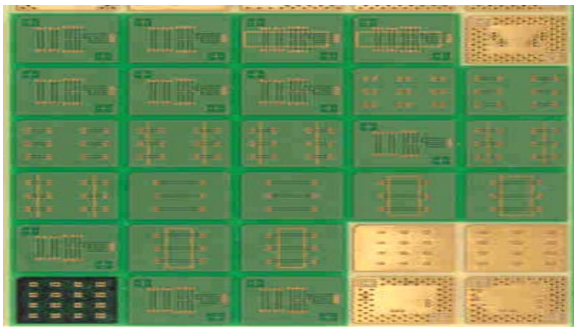

Figure 5. 2: HDI panel with 24 flip chip and five full Au metallized substrates as well as a test structure.

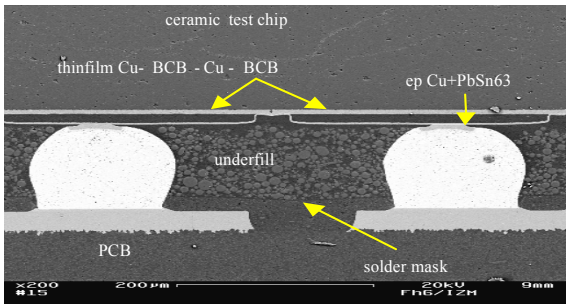

Figure 5. 3: SEM image of a cross section of a flip chip bonded and underfilled assembly with test structure.

The diced and singulated test chips were placed with a manual flip chip bonder into applied flux on the substrate. The assemblies were then reflowed in an infrared oven under activated nitrogen atmosphere and some of the samples were subsequently underfilled. The cross section in Figure 5. 3 shows the RF test structure of an underfilled flip chip. Geometrical data taken from cross-sections were compared with design data and used for further validation [106].

5.1.2 Package/Board Components

The design as well as schematic view of the layer stack-up was presented in section 4.2.2.2. Prior to designing each substrate/board component, its electrical boundaries were first defined, so as to determine the exact length of the traces interconnecting the device under test (DUT) and the adapters on which the probes are contacted.

5.2 RF Measurements and Analysis of Results

The RF measurements were performed from 100 MHz to 25 GHz. The measurement set-up consists of a VNA (HP 8510B), a probe station and a pair of coplanar probes (pitch=300 μm) connected to the VNA using coaxial cables. Figure 5. 4 shows a simplified schematic view of this measurement equipment, when the signal is delivered to port 1. It consists of a signal generator, test set with two coaxial measurement ports, a processing and display unit. The test set consists of a reflectometer which separates the incident and reflected waves at the measurement port. The signal source generates a time-harmonic signal with a specified frequency which can be swept over a selected bandwidth. The signal incident on the DUT is measured by coupling a small fraction of it to the reference port in the test set. The rest of the incident signal propagates through the test set and measurement cables to the DUT. The DUT reflects a part of it (the reflected signal) which propagates back to the test-set where it is directed to the test port of the test-set. In the measurement unit, the reflected wave is divided by the incident wave, resulting in S_{11}, when the generator is connected to port 1 of the DUT. The incident minus the reflected power is partly dissipated in the DUT incase it is lossy, partly transmitted through it. The transmitted signal also arrives in the test-set after propagation through a measurement cable. Again, the transmitted wave is divided by the incident wave delivering S_{21}. In the same way, S_{22} and S_{12} are measured when the generator is connected to port 2 [115].

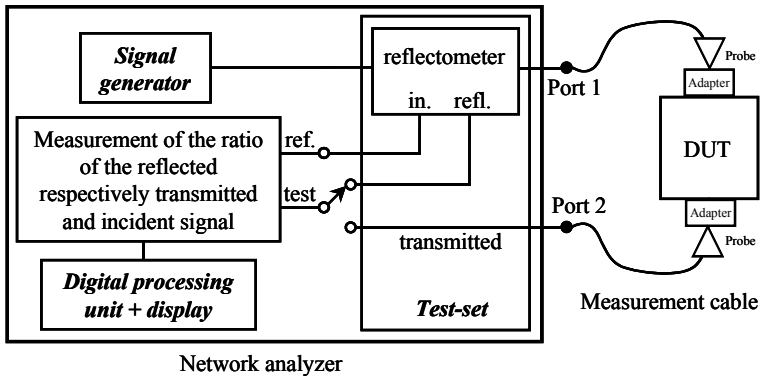

Figure 5. 4: Schematic view of VNA including DUT, adapters and probes.

Since the measurement equipment introduces many errors, it was calibrated prior to the measurement of the test structures. Calibration de-embeds imperfection in the system by

measuring known quantities called standards. Through the measurement of these standards, the system's imperfections can be isolated, quantified and mathematically removed [116]. Commonly used calibration methods include the SOLT (Short-Open-Load-Thru), TRL (Thru-Reflect-Line), LRM (Line-reflect-Match) and LRRM (Line-Reflect-Reflect-Match). Due to its high degree of accuracy, the LRRM method was used in this work together with a calibration substrate from Cascade Microtech on which the standards to be measured are fabricated.

After the calibration process, the test samples of all BGA package components were then measured. A schematic view of the test structure to be measured (DUT), the adapters and probes used for the measurement is shown in Figure 5. 5.

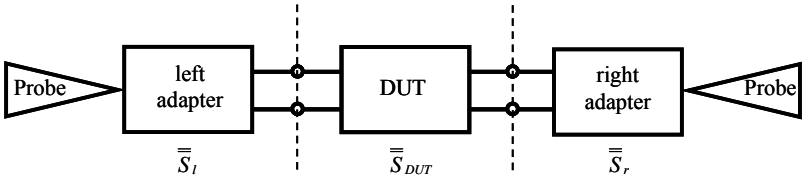

Figure 5. 5: Schematic view of measurement set-up consisting of adapters, DUT and probes.

As shown in this figure, the adapters provide the connection between the coplanar probes and the DUT. This implies, the measured S-parameters contain the effects of the adapters as well. In order to extract the RF characteristics of the DUT alone, the effects of the adapters must be removed. This was achieved through de-embedding, as will be illustrated in the following paragraphs.

From a measurement of the entire arrangement shown in Figure 5. 5, S-parameters were obtained. Since this arrangement represents a cascaded network, it is preferable to work with T-parameters. In order to obtain S-parameters of the DUT from the measured S-parameters, the S-parameters of the left and right adapter, as well as those of the entire arrangement were converted to their T-equivalents. Through matrix multiplication, T-parameters of the DUT were obtained.

$$\overline{\overline{S}}_l \rightarrow \overline{\overline{T}}_l$$
$$\overline{\overline{S}}_m \rightarrow \overline{\overline{T}}_m$$
$$\overline{\overline{S}}_r \rightarrow \overline{\overline{T}}_r$$

Then from,

$$\overline{\overline{T}}_m = \overline{\overline{T}}_l \cdot \overline{\overline{T}}_{DUT} \cdot \overline{\overline{T}}_r \tag{5.1}$$

$$\Rightarrow \overline{\overline{T}}_{DUT} = \overline{\overline{T}}_l^{-1} \cdot \overline{\overline{T}}_m \cdot \overline{\overline{T}}_r^{-1} \tag{5.2}$$

where

$\overline{\overline{S}}_l$ and $\overline{\overline{T}}_l$ are S- and T-matrices of the left adapter,

$\overline{\overline{S}}_r$ and $\overline{\overline{T}}_r$ are S- and T-matrices of the right adapter,

$\overline{\overline{T}}_{DUT}$ is the T-matrix of the DUT and

$\overline{\overline{S}}_m$ and $\overline{\overline{T}}_m$ are S- and T-matrices of the entire arrangement shown in Figure 5. 5.

From (5.2), it implies that S-parameters and hence, T-parameters of the adapters must be available in order to obtain the S-parameters of the DUT. For this purpose, adapter samples (e.g., open and through) were also designed on the same test board on which the test structures of the BGA components were designed. An example of a through adapter that was designed and measured in this work is shown in Figure 5. 6. In this example, the signal line, designated as S, is 100 µm wide and 2.6 mm long. Each of the two ground pads, represented by the letter G, is 0.7 mm long and at least 0.3 mm wide. The distance of separation between the signal line and ground pads, designated as d, was chosen such that GSG probes having a pitch of 300 µm can properly contact the adapters. In the design, interplane vias were used to interconnect ground pads and the reference plane in layer 2. A 0.6 mm thick FR4 substrate was used.

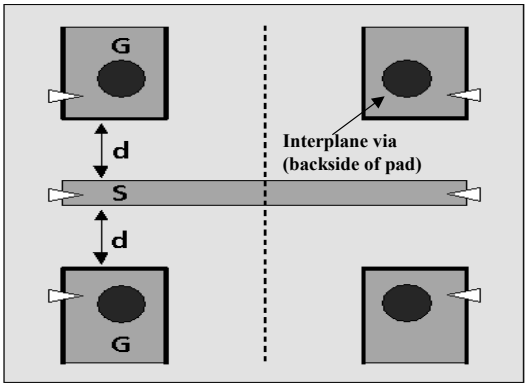

Figure 5. 6: Schematic view of a through adapter structure.

In order to obtain the RF characteristics of the left and right adapters, the through adapter was first modeled using the equivalent circuit model shown in Figure 5. 7.

Based on the measured S-parameters of the through adapter, values of the electrical parameters of this circuit model were extracted through an optimization process using Ansoft's Serenade. To validate the circuit model, a comparison was made between S-parameters obtained from RF measurement and circuit optimization of the adapter. As can be seen in Figure 5. 8, a very good correlation was obtained between S-parameters from both sources, thereby validating the circuit model.

S-parameters of the single adapters (see Figure 5. 7 - bottom) were read out and converted to T-parameters. They were then used in (5.2) to obtain the T-parameters of the DUT. Finally,

$\overline{\overline{T}}_{DUT}$ was then converted to $\overline{\overline{S}}_{DUT}$. The S-parameters of the DUT were then used to validate the modeling approach of each component. This will be illustrated in the next section.

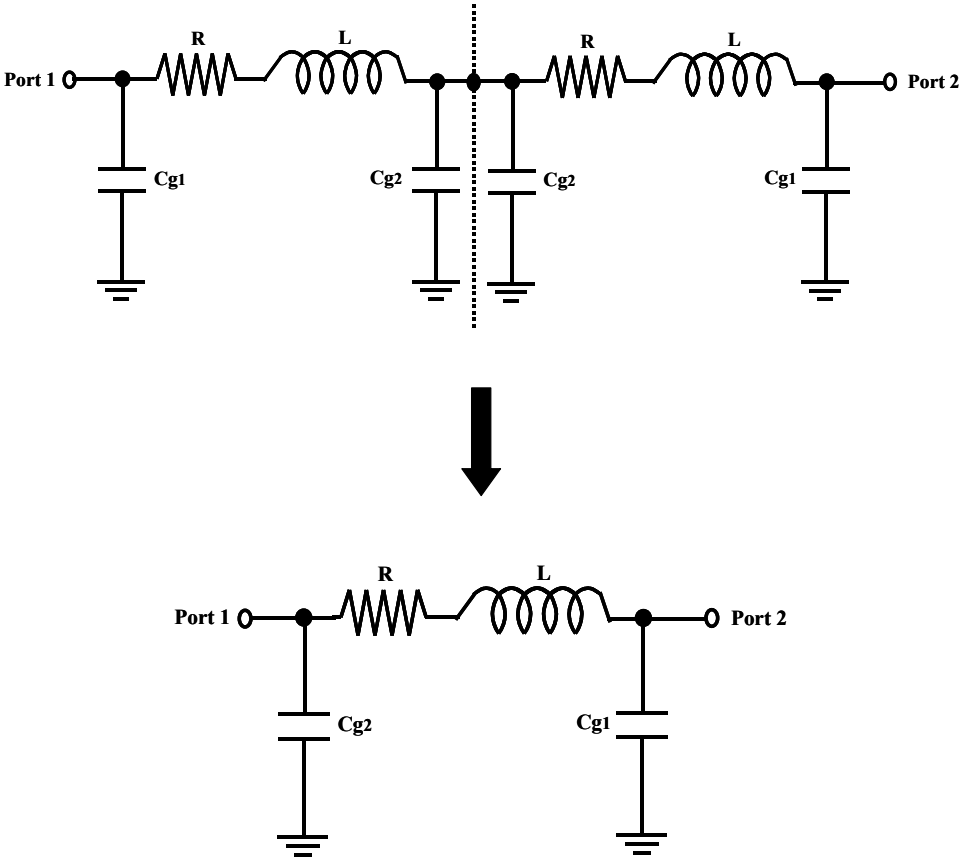

Figure 5. 7: Equivalent circuit model of through adapter structure (top) and single adapter (bottom).

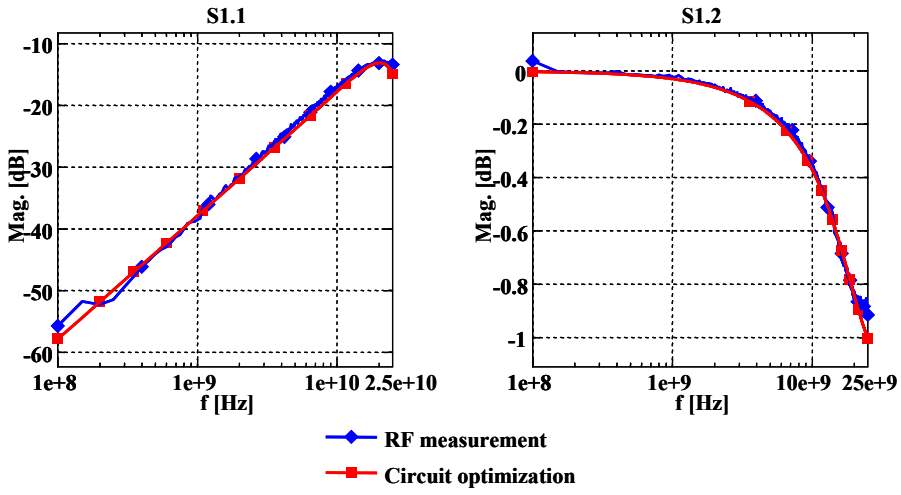

Figure 5. 8: Comparison of $|S_{11}|$ and $|S_{12}|$ from RF measurement and circuit optimization of through adapter structure from 100 MHz to 25 GHz.

5.3 Validation of Modeling Approach for Interconnecting Segments and for Complete Signal Paths

5.3.1 Chip-to-Package Interconnections

In section 4.2.2.1, it was proven that a bump array can be characterized using values of electrical parameters from single and two-coupled bumps. The goal of this section is to compare the simulated and experimental values of electrical parameters for these bump configurations.

5.3.1.1 Single Bumps

Since the single bumps were designed as one-port configurations, only the reflection coefficients could be measured. Based on the extracted values of S_{11}, values of L and R were extracted as follows:

From

$$S_{11} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{5.3}$$

$$S_{11}Z_L + S_{11}Z_0 = Z_L - Z_0$$

or (5.4)

$$Z_L\left(S_{11} - 1\right) + Z_0\left(S_{11} + 1\right) = 0$$

$$\Rightarrow \; Z_L = -Z_0\left(\frac{S_{11} + 1}{S_{11} - 1}\right) \tag{5.5}$$

Substituting for $S_{11} = a + jb$ in (5.5) results in the following expression for Z_L:

$$Z_L = -Z_0\left[\frac{(a+1) + jb}{(a-1) + jb}\right]$$

or

$$Z_L = -Z_0\left[\frac{a^2 + b^2 - 1}{(a-1)^2 + b^2} + j\frac{2\ \ b}{(a-1)^2 + b^2}\right] \tag{5.6}$$

where Z_L represents the load and Z_o is the characteristics impedance.

$$Z_L = R + j\omega L \tag{5.7}$$

Equating the real and imaginary parts of (5.6) and (5.7) results in expressions for R and L.

$$R = -Z_0\left[\frac{a^2+b^2-1}{(a-1)^2+b^2}\right] \tag{5.8}$$

$$L = \frac{Z_0}{\omega}\left[\frac{2\ \ b}{(a-1)^2+b^2}\right] \tag{5.9}$$

whereby $\omega = 2\pi f$.

(5.8) and (5.9) were then used for the extraction of L and R from the measured S-parameters. Considering L as an example, Figure 5. 9 shows its variation with frequency for three bump configurations.

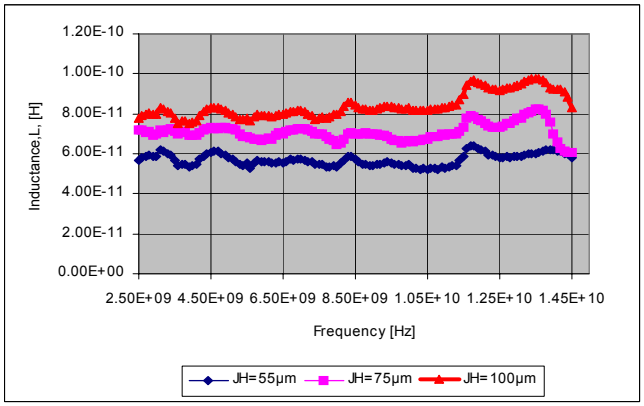

Figure 5. 9: Variation of L with frequency for bumps of heights 55 µm, 75 µm and 100 µm.

As expected, L is proportional to the bump height and it is relatively constant within the measured frequency band. Hence, an average value was calculated for each sample and used for comparison with the field computation results. This comparison is shown in Table 5. 1, where a very good correlation can be seen between EM field computation and RF measurement results.

JH/ µm	D1/ µm	D2/ µm	L /nH parameterized	L /nH measured
55	100	175	0.065	0.066
75	60	150	0.068	0.071
	80	175	0.066	0.065
100	60	150	0.074	0.075

Table 5. 1: Comparison between values of L obtained from EM field computation and RF measurement of test samples.

It should be noted that the comparison was actually made between a parameterized RF model of the bump and measurement results. Parameterized bump models, based on statistical design of experiment and full-wave EM field computations were developed. These models mathematically relate the geometrical and material parameters of the bumps to relevant electrical parameters. As an example, the parameterized L-model of a single bump is given in (5.10).

$$L[H] = f(JH, D1, D2) = a_0 + a_1 JH + a_2 D1 + a_3 D2 + a_4 JH \cdot D1 + a_5 JH \cdot D2 + a_6 D1 \cdot D2 + \ldots \qquad (5.10)$$

where JH represents the bump height, D1 and D2 designate the bump diameters in contact with the chip and substrate pads, respectively. The coefficients, $a_{i,}$ were estimated by adequate statistical algorithms, and eventually validated by statistical methods, test simulations and test sample checks.

The complete methodology that was used for the development and validation of these models can be found in [106].

5.3.1.2 Coupled Bumps

A linear circuit simulator (Ansoft's Serenade 8.5) was used for the extraction of M and Ck from measured S-parameters.

A comparison between the measured and field computed values of M is shown in Table 5. 2.

JH / µm	D1 / µm	D2 / µm	DPP/ µm	M /nH parameterized	M /nH measured
55	60	175	305	1.21E-03	2.52E-03
	60	200	330	1.09E-03	2.32E-03

Table 5. 2: Comparison between values of M obtained from EM field computation and RF measurement of test samples.

The differences between these values and those obtained using the parameterized model can be attributed either to numerical errors during field computations or measurement reproducibility, because the values are too small.

From an analysis of the measurement results, it was found out that, for HDI-organic substrates, capacitive coupling in flip chip transitions is mainly as a result of pads and must thus, be considered in pads model library. This can be explained as follows:

The total coupling capacitance (Ck_{total}) in a flip chip transition consists of the capacitance due to the pads (Ck_{pads}) and bumps (Ck_{bumps}). In accordance with design rules for HDI substrates, pads must be much bigger than bumps, such that they overlap by 2.5mil on the sides of the bump, as seen in Figure 5. 10. This causes Ck_{pads} to be much greater than $Ck_{bump,}$ resulting in an almost insignificance influence of an underfill on the RF behavior of coupled flip chip interconnects on HDI substrates. This can be seen in Table 5. 3, which presents a comparison between measured Ck-values in the presence and absence of an underfill [106].

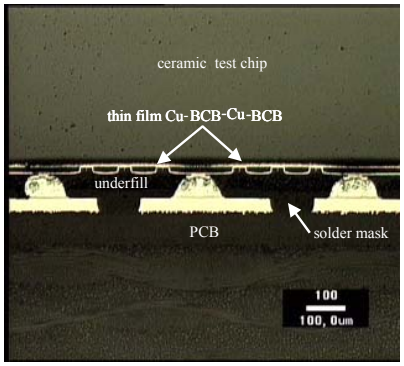

Figure 5. 10: SEM image of a flip chip bonded and underfilled assembly with test structure – Illustration of size of pads and their contribution to capacitive coupling in a flip chip transition.

JH / µm	D1 / µm	D2 / µm	DPP/ µm	Ck /pF measured (Without underfill)	Ck /pF measured (With underfill)
75	100	175	305	9.31E-03	9.46E-03
100	60	150	360	8.84E-03	9.23E-03

Table 5. 3: Comparison of measured values of Ck – with and without an underfill.

5.3.2 Package/Board Components

The package traces with bends were measured from 100 MHz to 25 GHz while the vias and their interconnecting traces were measured from 100 MHz to 10 GHz. After the RF measurements, the adapter structures were de-embedded using the technique illustrated in section 5.2 and the required S-parameters were extracted. These S-parameters were then compared with those obtained from EM field computations (see Figure 5. 11 and Figure 5. 12

for the trace with a 45° bend and a via segment, respectively). As can be seen from this comparison, a good correlation was obtained between S-parameters from both sources, thus validating the models used. The discrepancy between measurement and simulation from 100 MHz to about 200 MHz in Figure 5. 11 is due to the limitation in accuracy of the vector network analyzer.

It is worth mentioning that large technological fluctuations occurred during the fabrication of the test samples, as revealed by their cross-sectional views. For the comparison shown here, the EM field computations were performed with approximate geometrical values obtained from the measurement of these cross-sections. The slight discrepancies between measurement and field simulation are also because of these fluctuations.

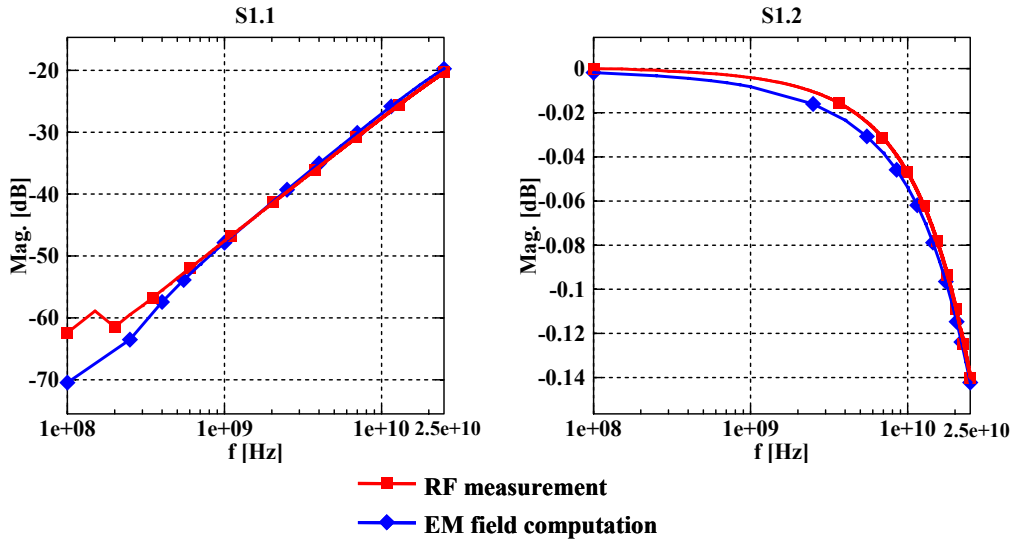

Figure 5. 11: Comparison of measurement and EM field computation results for a microstrip trace with double 45° bends.

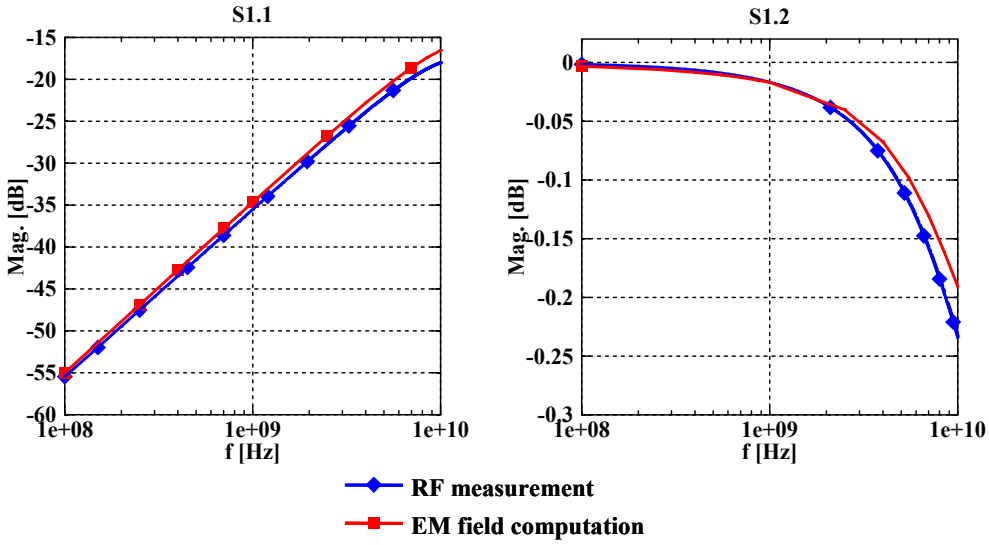

Figure 5. 12: Comparison of measurement and EM field computation results for a via segment.

5.3.3 Complete Signal Paths

In the previous section, a comparison was made between EM field computation and RF measurement results of single components. In this section, theory and measurement for the case where the complete signal path within the substrate is characterized by a cascade of interconnecting components will be compared. Actually, this comparison was initially meant to be carried out for the entire signal path from chip to board. However, due to fabrication errors that occurred in the second level interconnects, only signal paths within the substrate were properly fabricated. Cross-sectional snap-shots of the signal BGA balls revealed that they were not properly soldered, so in most of the cases, the interposer lied directly on the PCB. Hence, only samples with complete signal paths within the BGA substrate itself were used for the validation.

Figure 5. 13 shows the measurement set-up of a test sample, illustrating the complete signal path within the substrate. As can be seen in this figure, the signal path consists of traces with two via transitions. After the measurement of this complete path, the left and right adapters were de-embedded and S-parameters characterizing only the signal path were obtained. EM field computations of each via segment were also performed using the 3D model shown in Figure 5. 14 and S-parameters were also extracted.

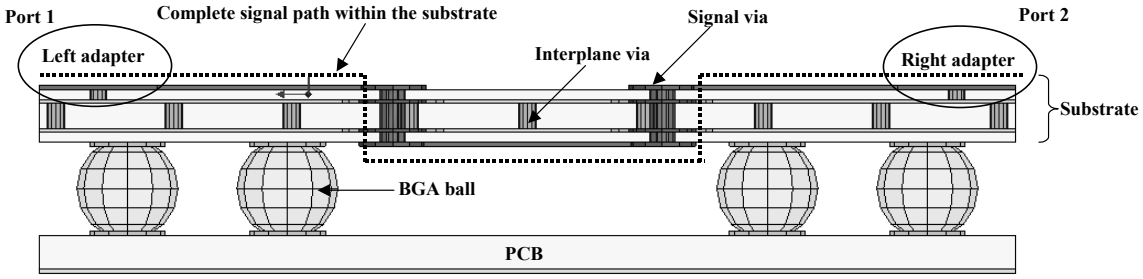

Figure 5. 13: Cross-sectional view of BGA package showing complete signal path within the substrate.

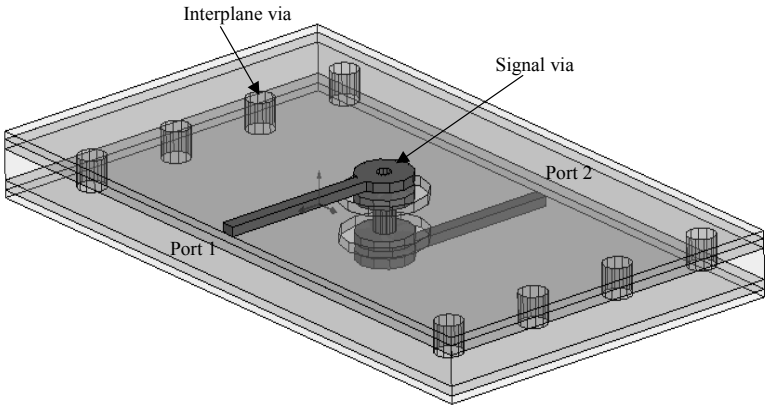

Figure 5. 14: 3D model used for EM field computation of half the length of the signal path within the substrate.

Assuming that the configuration of the measured complete signal path is symmetrical, the S-parameters extracted from the EM field computation of a single segment were cascaded to generate S-parameters of the complete path. Lastly, EM field computation of the complete signal path, as shown in Figure 5. 13 was also performed and S-parameters extracted. S-parameters obtained from all the three cases were then compared. As can be seen in Figure 5. 15 and Figure 5. 16, a good correlation was obtained between these S-parameters, thus validating the modeling approach used for complete signal paths in this work. The slight discrepancy seen is mainly as a result of the fact, that due to technological errors, the complete signal path fabricated was not as symmetrical as assumed. Besides, so many fluctuations occurred during the fabrication of the test samples. They were not all considered in the EM field computations.

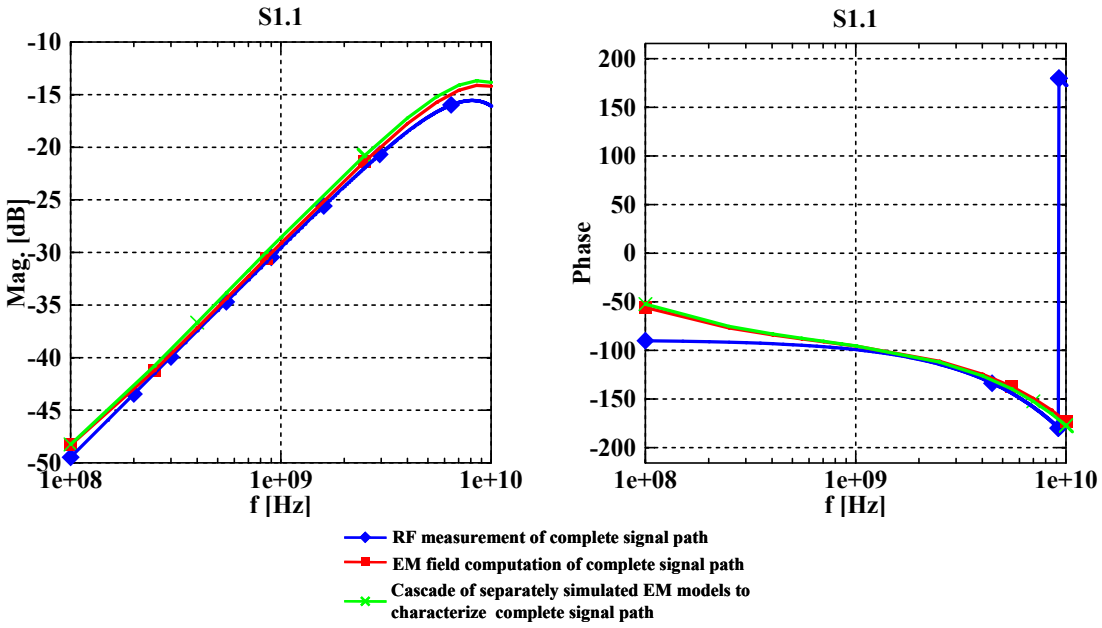

Figure 5. 15: Comparison of S-parameters obtained from measurement of a complete signal path within the substrate with those obtained from EM field computation of the complete path as well as a cascade of separately simulated EM models to characterize the same path – S_{11} considered.

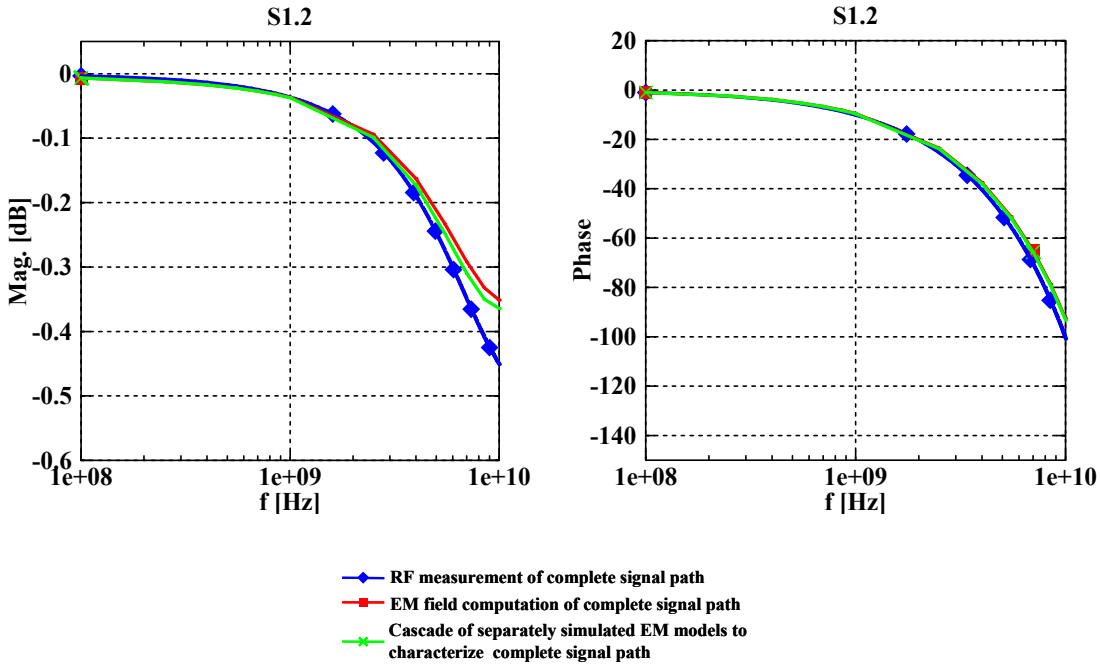

Figure 5. 16: Comparison of S-parameters obtained from measurement of a complete signal path within the substrate with those obtained from EM field computation of the complete path as well as a cascade of separately simulated EM models to characterize the same path – S_{12} considered.

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Chapter 6

Illustrating the Novel Methodology for Optimizing the RF Performance of System-in-Package Modules: Case Study – BGA Package Module

6.1 Minimizing Reflections and Distortions

6.1.1 Identification of the Potential Causes of Reflections and Distortions

Before proposing design rules to minimize reflections, their root causes must first be identified. This will be done in sections 6.1.1.1 and 6.1.1.2 by studying the impact of discontinuity effects of substrate/board components as well as the effects of technological tolerances of each interconnecting component.

6.1.1.1 Impact of Discontinuity Effects of Substrate/Board Components

The wideband model (developed and validated in the previous two chapters), which accounts for the parasitic effects of all interconnecting components along complete signal paths in BGA modules, was used for this study. For convenience, this model is shown in Figure 6. 1.

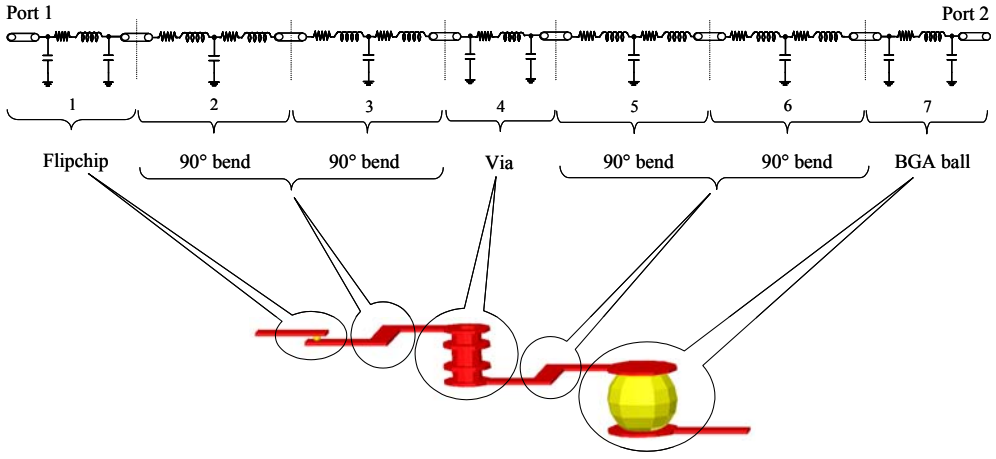

Figure 6. 1: Equivalent circuit model of the complete signal path (chip-to-board) in a BGA package module. For illustrative reasons, the chip and dielectric layers of the interposer and board are not shown.

The general approach used for this study is as follows: The equivalent circuit model of the component under consideration is simply replaced with a transmission line model which represents a uniform trace having the same length as the component. By comparing properties of the signal which propagates through the path in the presence and absence of the component, its impact on the signal quality is easily noticed.
For an illustration of this method, the discontinuities shown in Figure 6. 2 and a 2.4 mm long microstrip signal path within the substrate were considered as examples.

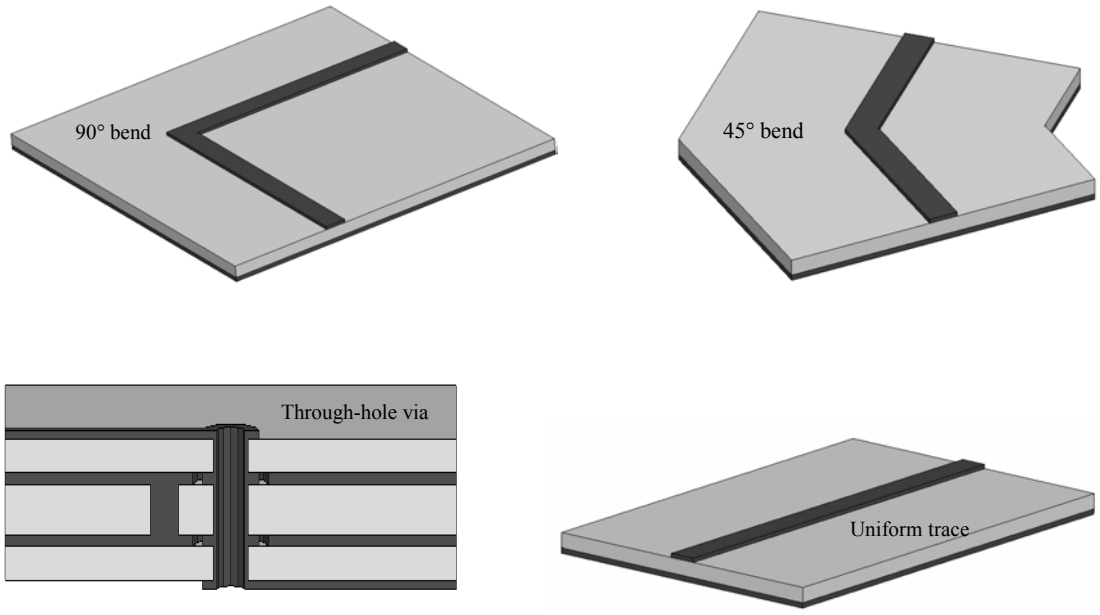

Figure 6. 2: 3D model of a 90° bend, 45° bend, a through-hole via and a uniform microstrip trace.

Consequently, segments one and seven in the circuit model in Figure 6. 1 were initially ignored. In order to investigate the effects of four bends, this circuit model was further reduced by ignoring segment 4, and transmission line models in the remaining segments were adjusted so as to achieve a total path length of 2.4 mm. Values of electrical parameters of each bend were assigned to their respective components in this circuit model and S-parameters characterizing the path were then extracted. The number of bends was gradually reduced, one at a time, by replacing each equivalent circuit model of a bend with a transmission line model that represents a uniform trace having the same length as the bend. Each time a bend was removed from the path, new S-parameters were extracted. 45° and 90° bends were separately investigated. The equivalent circuit model of the uniform signal path (whose 3D model is also shown in Figure 6. 2) that served as the reference was obtained by replacing equivalent circuit models of all four bends with a transmission line model of a uniform trace of equal length as the bends. S-parameters characterizing this signal path were also extracted.
Now, to understand the effects of bends in the presence of any other discontinuity, the effects of bends were compared with that of a via. To investigate the effects of vias on the signal

path, only segment 4 in the circuit model in Figure 6. 1 was used and transmission line models of the uniform interconnecting traces were extended, so as to achieve a 2.4 mm long signal path. S-parameters characterizing this path were then extracted.

Finally, a comparison was made between S-parameters characterizing the effects of the discontinuities (bends and vias) and those of the reference path. The results of this comparison are shown in Figure 6. 3. Due to the presence of a 90° bend, $|S_{11}|$ increases by approximately 4 dB from about 2.5 GHz to 20 GHz. A 45° bend on the other hand causes an approximate increase of 1 dB. As the number of bends increases, the fraction of signal reflected increases steadily with frequency. For example, four 90° bends along the path cause more than 10% of the propagating signal to be reflected at frequencies above 10 GHz. However, as can be seen in Figure 6. 3, this amount of reflection is slightly less than that caused by a single through-hole via.

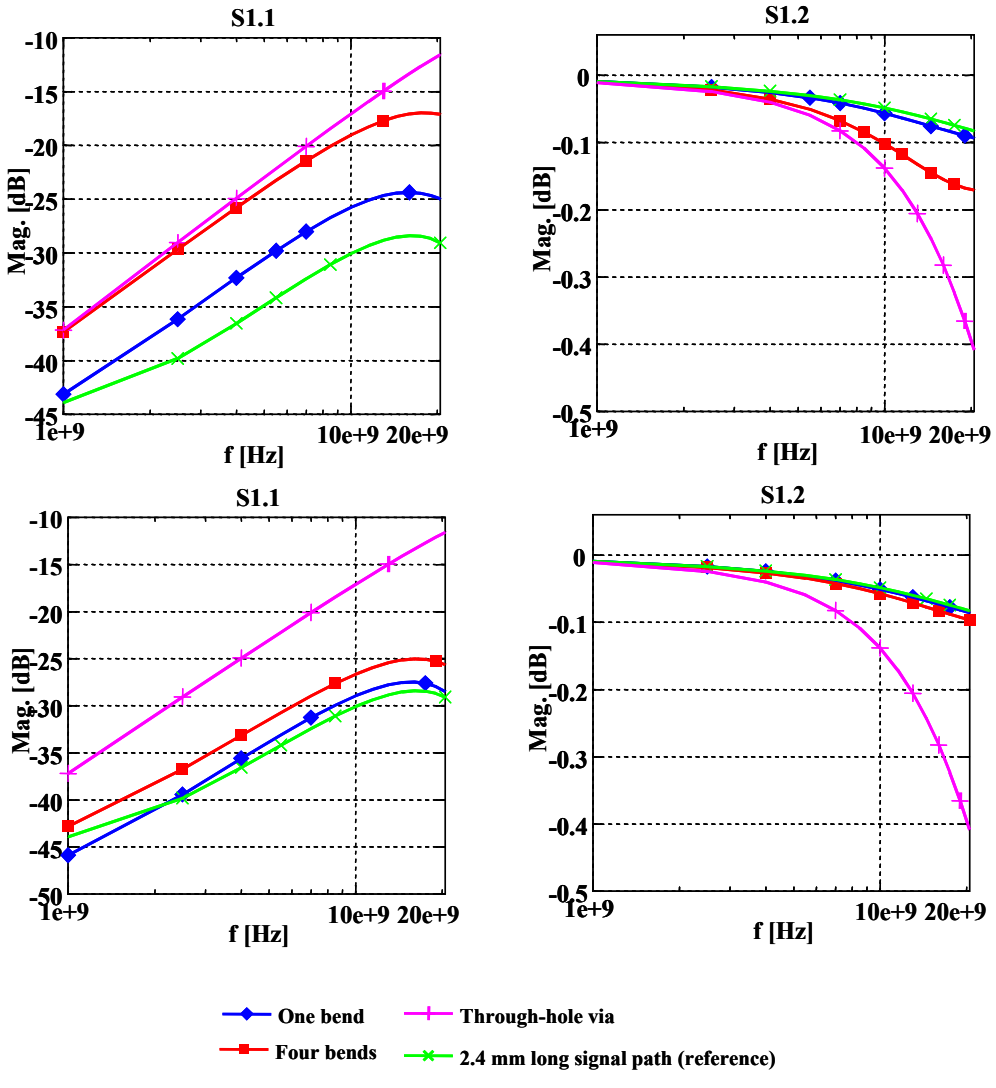

Figure 6. 3: Effects of bends and vias on $|S_{11}|$ of a 2.4 mm long microstrip trace - Top: 90° bends considered, Bottom: 45° bends considered.

These results show that the presence of any other discontinuity (e.g., a via) along a path overshadows the effects of up to four bends. Consequently, if the entire signal path in a BGA package module (chip-to-board) is considered, then the effects may be ignored, depending on the speed of the propagating signal. For example, for frequencies up to 25 GHz, the effects of at least four 45° bends on the reflection and transmission coefficients of the S-parameters of the complete signal path can be neglected, as shown in Figure 6. 4 [111].

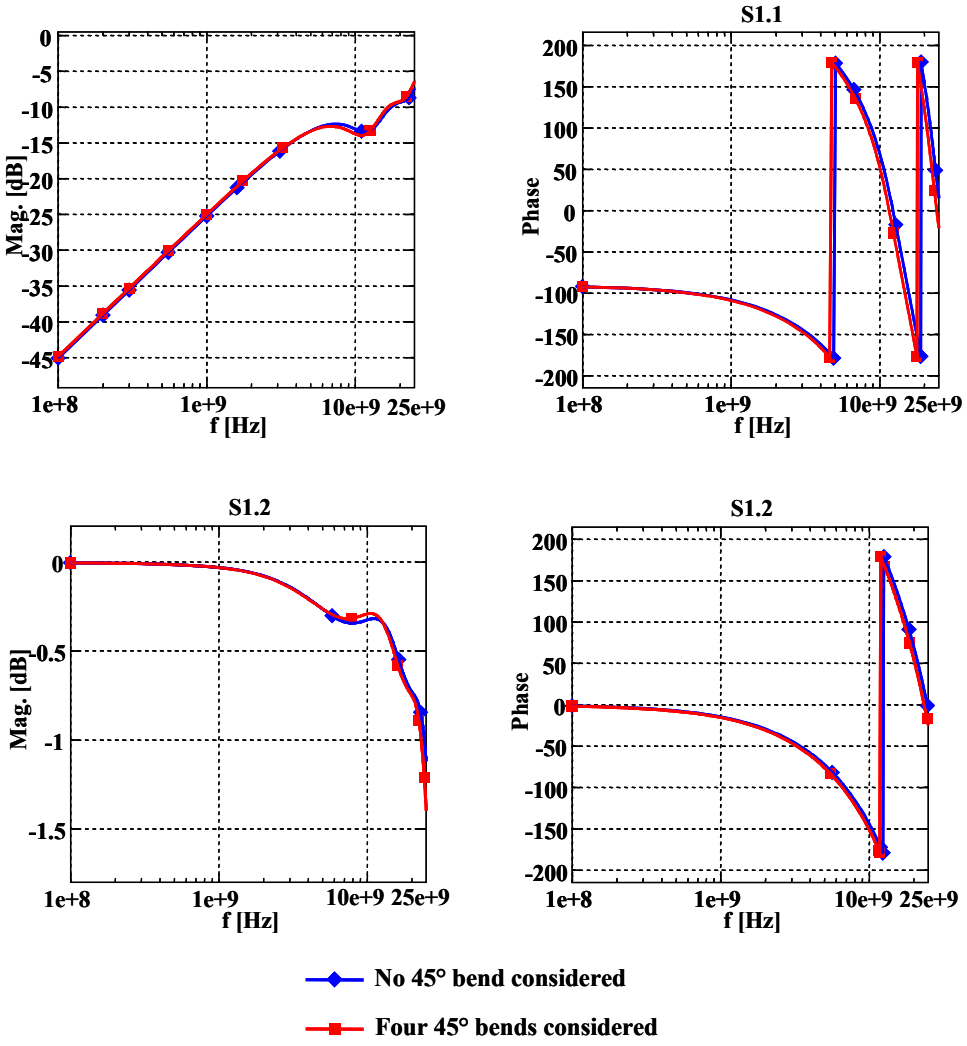

Figure 6. 4: Illustrating the negligible effects of 45° bends on the reflection and transmission behavior of the complete signal path.

From these investigations, the following design guidelines were deduced:

- For applications above 10 GHz, use less than four 90° bends along a signal path less than or equal to 2.5 mm long, so as to keep reflections less than 10%.

- 45° bends should be used instead of 90° and chamfered 90°bends, whenever possible.

- For frequencies up to 15 GHz, six 45° bends can be used along signal path less than or equal to 2.5 mm and less than 10% of the signal will be reflected.

- For typical 50 Ω lines, the presence of other discontinuities along the path overshadows the effects of multiple bends.

    - For example, the effects of at least four 45° bends on the RF performance of complete signal paths can be neglected for frequencies up to 25 GHz.
- One through-hole via causes more reflection than four 90° bends.

6.1.1.2 Impact of Technological Tolerances of all Interconnecting Components

When geometrical and material parameters of components fluctuate during the fabrication process, their RF characteristics also change. This may, for example, lead to unexpected impedance mismatch between interconnecting components, resulting in additional signal reflections that were not taken into consideration during the design phase. When this occurs, the normal functioning of the system can no longer be guaranteed. In order to develop design guidelines that can be used to prevent such occurrences, the impact of technological fluctuations on each component as well as on the entire signal path must be critically investigated at the beginning of the design cycle. To reach this goal, the following approach was used:

For each component, a design space which defines the technological parameters of interest and the range in which they are allowed to vary was first set-up. Using standard values of these parameters, a full-wave EM field computation was performed, from which values of the required electrical parameters were extracted using an appropriate equivalent circuit model of the component under investigation. These values then served as reference. Each time a geometrical or material parameter was changed, field computations were performed and new electrical parameter values were also extracted. These values were then compared with the reference, so as to understand the effects of the change on the electrical characteristics of the component. Since previous investigations revealed, that effects of an interaction of geometrical and/or material parameters within the defined design space can be neglected, this interaction will not be presented in this work.

To understand the effects of technological fluctuations of each component on the RF behavior of the entire signal path, the equivalent circuit model in Figure 6. 1 was used. Values of electrical parameters obtained from, for example, a 10% change in the diameter of a via hole, were inserted into the equivalent circuit model of the via, while the other circuit models contain the reference values. S-parameters characterizing the complete path were then extracted and compared with those obtained when all circuit parameters along the path contain only reference values. From this comparison, it will then be evident if a change in the geometrical or material parameter of the component under consideration has an impact on the reflection and transmission behavior of the entire signal path.

In the following subsections, a summary of results obtained using the approach outlined above will be presented.

I) Chip-to-Package Interconnects

With regards to flip chip interconnects, which were used as the first level interconnections in this work, the geometrical parameters of interest and their standard values considered for this sensitivity studies are as follows: bump height=50 µm and bump diameter=60 µm. These values were used to perform EM field computations using the model shown Figure 4.17 (left). From the field computation results, approximately 0.03 nH and 25 mΩ (at 5.5 GHz) were obtained for L and R, respectively, through an optimization of the equivalent circuit model of the bump, shown in segment 1 in Figure 6. 1.

The bump height and diameter were then varied and each time a change was made, new values of L and R were extracted. The results of these investigations revealed, that a 10% variation in the height as well as diameter of the bump causes a change of less than 5% in L and R. All fluctuations in L and R are directly proportional to changes in the bump height, but inversely proportional to the bump diameter.

Since bumps are much smaller than other components along the signal path, the effects of up to 30% fluctuation in their diameters and heights on the magnitude of the reflection and transmission coefficients of the S-parameters (S_{11} and S_{12}) of the entire signal path can be neglected. As can be seen in Figure 6. 5, the curve representing the effects of a 30% change in the bump diameter lies exactly over the curve extracted when only reference values were used in the equivalent circuit model in Figure 6. 1.

From these investigations, the following guideline was deduced: For frequencies up to 25 GHz, the impact of up to 30 % fluctuation in the bump geometry can be neglected, if the signal path is not disconnected through this fluctuation.

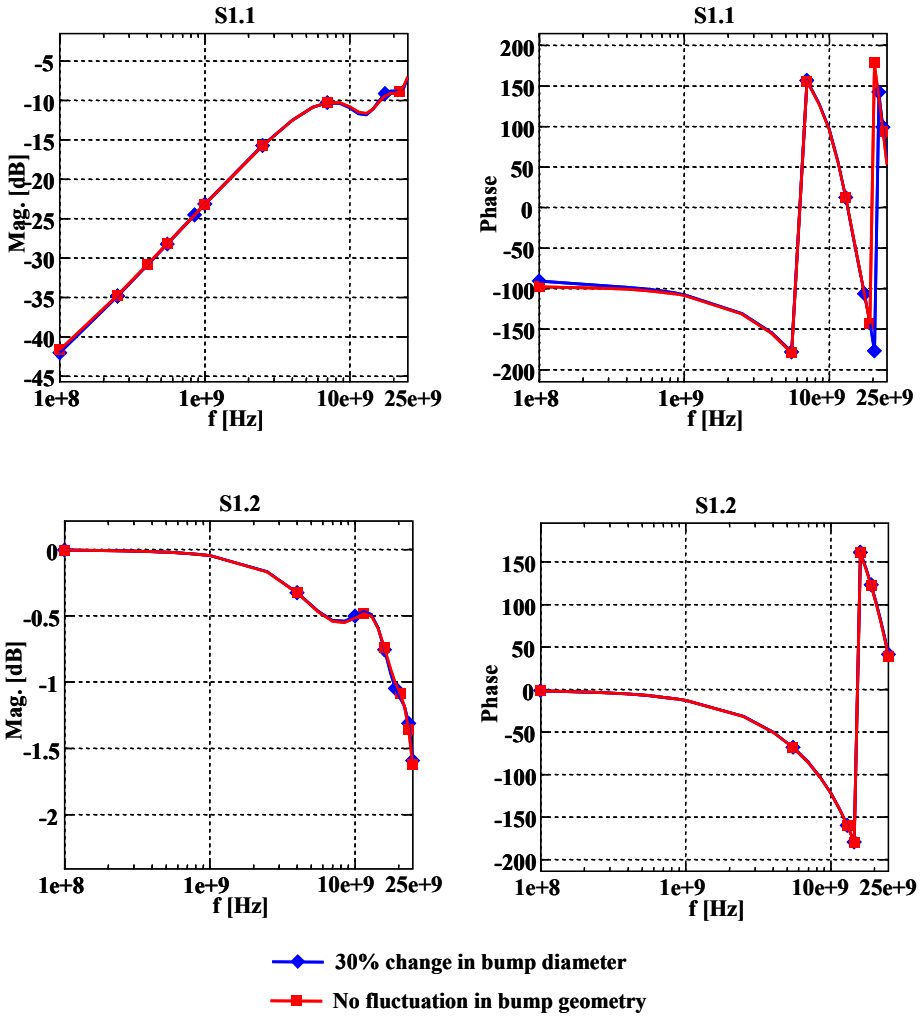

Figure 6. 5: Comparing the reflection and transmission behavior of the complete path, when effects of 30% variation in bump diameter are considered and when they are neglected.

II) Package/Board Components

The pacakge/board components considered for this sensitivity analysis are uniform package traces and vias. For each of these components, its geometrical and material parameters were varied from 10 to 30%.

1. Package Traces

In order to capture the effects of fluctuations in line geometry and material on its characteristics impedance, a 2D EM field analysis was carried out.

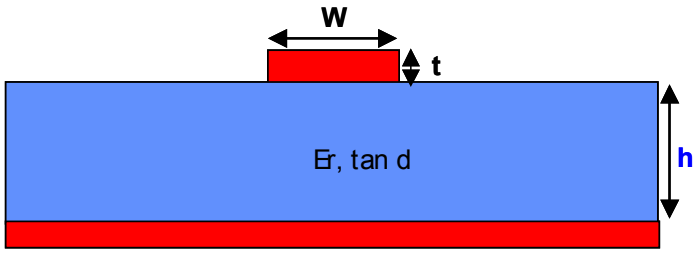

Figure 6. 6: Cross-sectional view of microstrip line used for sensitivity analysis.

A cross-sectional view of the microstrip line considered in this study and its parameter of interest are shown in Figure 6. 6. Using Maxwell 2D Extractor, an EM field field computation was performed each time a parameter was changed. The results revealed that the effects of up to 30% fluctuation in t and tan δ can be neglected, because they cause less than 5% change in Z. The most significant variation in Z was caused by fluctuations in h and w, followed by ε_r. Z changes by less than 10% if either h, w or t fluctuates by 10% and by approximately 15% if either w or h changes by 30%. Consequently, to keep fluctuations of Z below 10%, care must be taken during the fabrication process to keep changes in w, h and ε_r below 10%.

To understand the effects of fluctuations of the dominant line parameters on the RF performance of the package, a 3D EM field analysis of the entire signal path was carried out. W, h and t were separately varied from 0% to 30% and S-parameters characterizing each of these changes were extracted. These results reveal that a 30% change in either h, w or ε_r causes about 3 dB change in $|S_{11}|$ of the complete signal path. This variation in S_{11} is directly proportional to changes in w and t, and inversely proportional to changes in h. In Figure 6. 7, the effects of a 30% variation in w on the magnitude of S_{11} are shown, as an example.

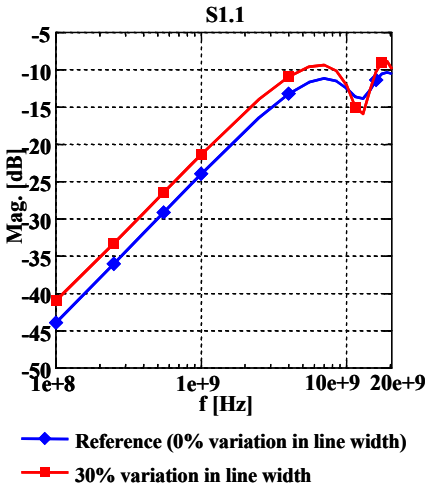

Figure 6. 7: Comparing $|S_{11}|$ of the complete path, when effects of 30% variation in line width (w) are considered and when they are neglected.

2. Through-hole Vias

The capacitance of a via is strongly affected by ε_r, pad diameter and space to ground. A 10% change in ε_r and space to ground causes less than 10% fluctuation in C, while a 10% change in the pad diameter causes approximately 10% variation in C. C varies by approximately 10-

15%, 20-25% and 25-30% if the space to ground, ε_r and pad diameter, respectively, fluctuates by 30%.

The inductance as well as capacitance of a via are highly dependent on the length of the via, which in turn depends on the dielectric thickness. But, varying the thickness of either both prepeg layers or core by 10%, causes less than 5% change in L and C. However, if prepeg and core layers simultaneously fluctuate, then both L and C will vary considerably. Such a change must be prevented, whenever possible. Fluctuations in pad diameter, space to ground as well as hole diameter also slightly affect L. For example, 30% variation in hole and pad diameters causes approximately 10% and 10-15% change in L, respectively. Changing the space to ground by 30% leads to approximately 5% fluctuation in L.

Effects of up to 30% variation in tan δ on both L and C can be neglected. This also applies to the hole displacement, if actually the interconnecting signal trace is not disconnected by such a fluctuation.

To capture the effects of fluctuations in any via parameter on the complete signal path, values of L and C resulting from a variation of the parameter in question were inserted into the equivalent circuit model of the via in segment 4 in Figure 6. 1. In Figure 6. 8, effects of 30% variation in space-to-ground on the reflection and transmission behavior of the complete signal path is shown as an example. At lower frequencies, the change in space-to-ground can be neglected, but at frequencies above 10 GHz, the impact of this change on the magnitude of S_{11} slowly becomes evident.

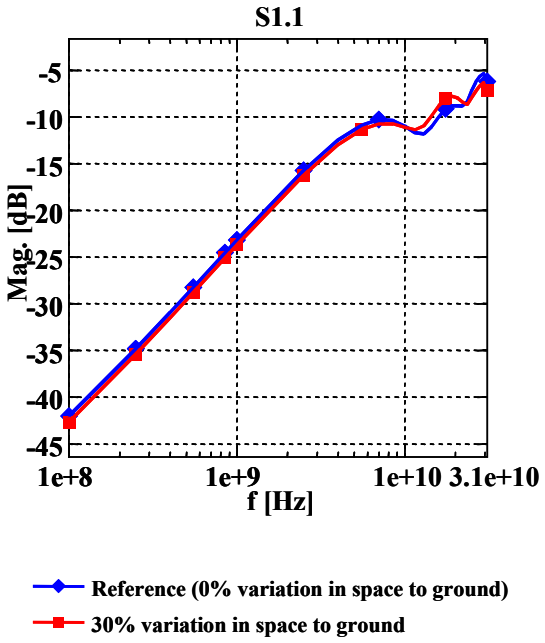

Figure 6. 8: Comparing $|S_{11}|$ of the complete path, when effects of 30% variation in space to ground are considered and when they are neglected.

III) Package-to-Board Interconnects

Since BGA balls are the largest components along the signal path, with a diameter of 600 µm and length of 500 µm, any fluctuations in their geometry causes more impact on the RF performance of the package than any other interconnecting component. Considering first the impact of the fluctuations on the electrical parameters of the ball itself. While a 10% variation in ball height causes approximately 10% variation in L, a 10% fluctuation in the ball diameter causes slightly less variation in L as the ball height. However, if the ball diameter varies by 30%, L will vary by approximately 20%. A 30% fluctuation of ball height must be prevented whenever possible, because it causes more than 30% fluctuation in L.

Now, considering the complete signal path, the impact of a 30% variation in ball height becomes evident only from frequencies above 5 GHz, as can be seen in Figure 6. 9. For example, a 30% change in ball height causes approximately 20% fluctuation in $|S_{12}|$ at 10 GHz and approximately 30% change at 30 GHz.

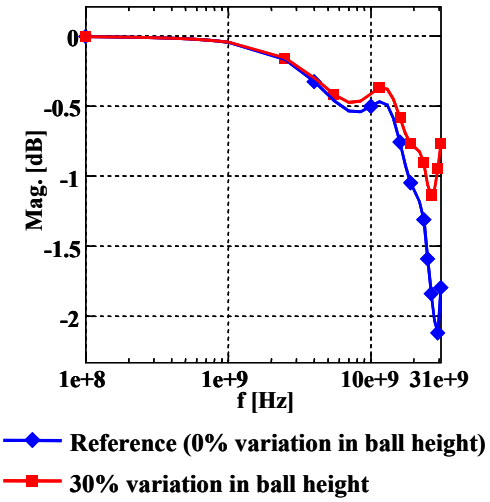

Figure 6. 9: Comparing $|S_{12}|$ of the complete path, when effects of 30% variation in ball height are considered and when they are neglected.

6.1.2 Deduction of Critical Components and Development of Design Measures to Optimize their RF Performances

Based on the results of investigations presented in the previous sections, it can be deduced that due to their sizes, flip chip interconnects have the least significant effect. Since 90° bends, vias and BGA balls have the most dominant effects, they'll be termed critical components. In the following paragraphs, design measures to minimize the parasitic effects caused by these components will be presented.

6.1.2.1 Optimal Choice and Design of Critical Components

Considering the package/board discontinuities as examples, this section will illustrate how reflections and distortions can be minimized by using optimal choice and design of each component.

1. Optimal Choice

In section 6.1.1.1, the effects of different configurations of bends and a through-hole via were compared. This comparative study led to the following conclusions (summarized):

- 45° bends are the optimal choice of discontinuity to be used to facilitate horizontal routing, because they cause less reflections and distortions than 90° or chamfered 90° bends. Their effects on the RF performance of the entire signal path in a BGA package module can even be neglected for frequencies up to 25 GHz.

- One through-hole via used for vertical routing causes more reflections and distortions than at least four 90° bends or six 45° bends along a signal path of the same length.

Therefore, more efforts have to be concentrated on developing concepts to minimize the discontinuity effects of vias.
In order to have an optimal choice of via for a given transition, a comparative study of the different via configurations that can be used for this transition must first be made.

Comparison between Blind, Buried and Through-hole Vias

From most publications (e.g., [117]), it is believed, that through-hole vias cause more reflections than buried and blind vias. However, this is not always the case. In the following sub-sections, it will be shown for frequencies up to 30GHz, that depending on the layer stack-up and via configuration, discontinuity effects of buried and blind vias can be greater than those of through-hole vias. Since the main aim of investigations presented in this section is just to compare the degree of signal reflections caused by vias, only the signal vias are considered in the EM model. The planes are connected by means of perfect conducting walls that enclose the via model. Since these walls are used as return paths, the same distance was considered between the signal via and the conducting walls in all the via models.

Blind and Through-hole Vias

They were used to interconnect two 50 Ω microstrip and stripline traces in layers 1 and 3, respectively. Apart from the fact that the through-hole via goes through the entire length of the substrate and the blind via ends in layer 3, both vias are geometrically the same. Figure 6. 10 presents cross-sectional views of their 3D models that were used for the EM field computations. The computations were performed using the same tool and within the same frequency range. A comparison of their S-parameters (see Figure 6. 11) reveals, that the

through-hole via produces less reflection than the blind via. This can be explained as follows: The presence of the reference plane beneath the blind via increases the parasitic capacitance of the via, thus reducing its characteristics impedance (see Table 6. 1). Consequently, the impedance mismatch between the 50 Ω interconnecting traces and the blind via increases, leading to more signal reflections.

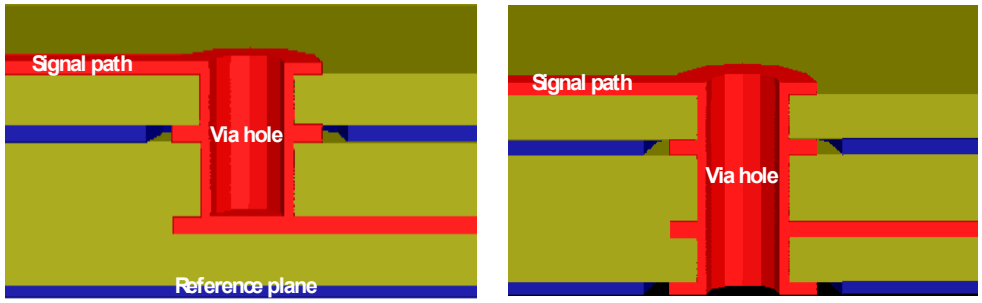

Figure 6. 10: 3D models of blind (left) and through-hole (right) vias used for a microstrip to strip line transition.

	L/H	C/F	Z/Ω
Blind via	1.4E-10	1.8E-13	28.1
Through-hole via	1.5E-10	1.6E-13	30.5

Table 6. 1: Approximate L, C and Z values for blind and through-hole vias interconnecting microstrip and stripline traces in layers 1 and 3, respectively.

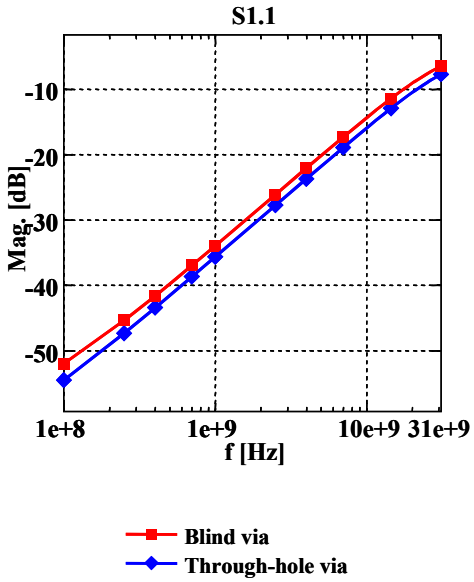

Figure 6. 11: Comparing blind and through-hole vias used for a microstrip to stripline transition – $|S_{11}|$ considered.

Since in this case the through-hole via causes less reflection than the blind via, it is the optimal choice to be used to optimize the RF performance of the package module.

Buried and Through-hole Vias

In this case, both vias were used for the interconnection of two 50 Ω embedded coplanar lines in layers 2 and 3. Cross-sectional views of their 3D models used for the EM field computations are shown in Figure 6. 12.

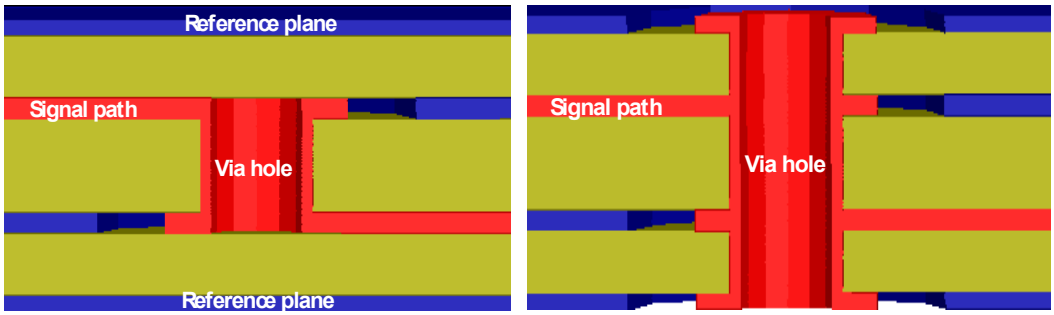

Figure 6. 12: 3D models of buried (left) and through-hole (right) vias used for an embedded coplanar to embedded coplanar transition.

A comparison of their S-parameters (see Figure 6. 13) at the end of the field computations reveals, that the buried via causes more signal reflections than the through-hole via. This is mainly due to the same reason as to why the blind via causes more reflections than the through-hole via. However, the impedance mismatch is greater between the buried via and the 50 Ω traces because of the presence of two reference planes, beneath and above the via.

In Table 6. 2, approximate values of L, C and Z obtained for buried and through-hole vias are presented.

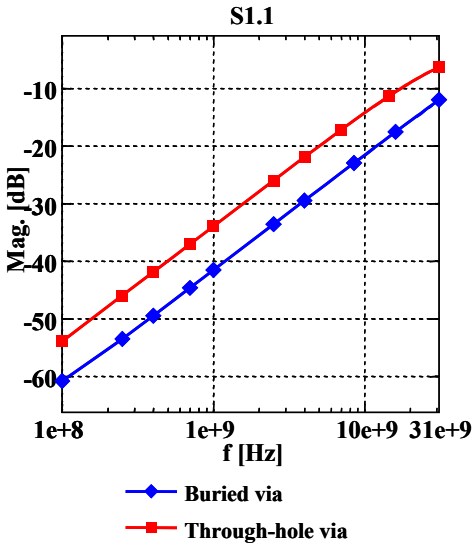

Figure 6. 13: Comparing buried and through-hole vias used for an embedded coplanar to embedded coplanar transition - $|S_{11}|$ considered.

	L/H	C/F	Z/Ω
Buried via	1.0E-10	1.7E-13	24.9
Through-hole via	1.5E-10	1.1E-13	36.5

Table 6. 2: Approximate L, C and Z values for buried and through-hole vias, interconnecting two embedded coplanar traces in layers 2 and 3.

Since in this case the through-hole via causes less reflection than the buried via, it is the optimal choice to be used to optimize the RF performance of the package module.

2. Optimal Design - Design Recommendations

It has been shown in the previous section, that for capacitive buried and blind vias, the presence of reference plane(s) above and/or beneath the vias increases the impedance mismatch between the via and interconnecting traces, leading to more signal reflections. Hence, any design measures taken to reduce the capacitances or increase the inductances of these vias consequently reduces their parasitic effects. Since these capacitance and inductances are mostly determined by the structure of the layer stack-up, the via structure and its environment, the design recommendations proposed in this section must be implemented at the beginning of the development cycle (in the pre-layout phase), when decisions on the choice of package components and the structure of the layer stack-up to be used are being made.

To reduce discontinuity effects of vias, the following guidelines can be used [118]:

- Adjust the pad/hole ratio. This is applicable to buried, blind and through-hole vias.
- The vertical distance between blind and buried vias and the nearest reference plane(s) must be increased or decreased accordingly, so as to match the via and trace impedances.
- Use interplane vias to control the inductance of the via, hence its impedance.
- Eliminate pads at reference planes and/or logically increase the size of the clearance hole, so as to decrease the via capacitance and hence increase its characteristics impedance. This can be used to match the impedance of capacitive vias and their connecting traces.
- If possible, holes can be bored in the reference plane(s), directly above and/or underneath buried and blind via pads.
- Use smaller vias, whenever possible.

In the following sub-sections, the first three design recommendations will be illustrated.

I) Adjust the Pad/Hole Ratio

Depending on whether the via is capacitive or inductive, the pad/hole ratio can be adjusted to reduce the impedance mismatch between the via and the connecting trace.

Considering a capacitive via as an example, a smaller pad/hole ratio (smaller annular ring) must be used. For blind and buried vias, this leads to a reduction in the capacitance between the via and the reference planes(s) below and/or above the via. Consequently, the impedance mismatch between the via and the connecting trace is reduced. Figure 6. 14 shows the top view of a blind/buried via with a reference plane.

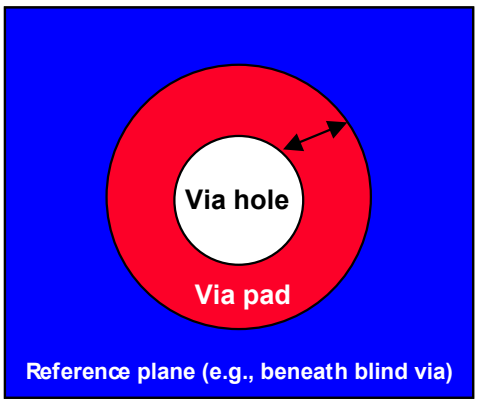

Figure 6. 14: Top view of a blind or buried via

In Figure 6. 15, reflection coefficients of S-parameters of the blind via and buried vias presented in Figure 6. 10 and Figure 6. 12, respectively, are shown for pad/hole ratios ranging from 1.5:1 to 4:1. Considering the buried via as an example, increasing the pad/hole ratio from 1.5:1 to 4:1 increases the signal reflection from approximately 6% to about 34% at 5GHz.

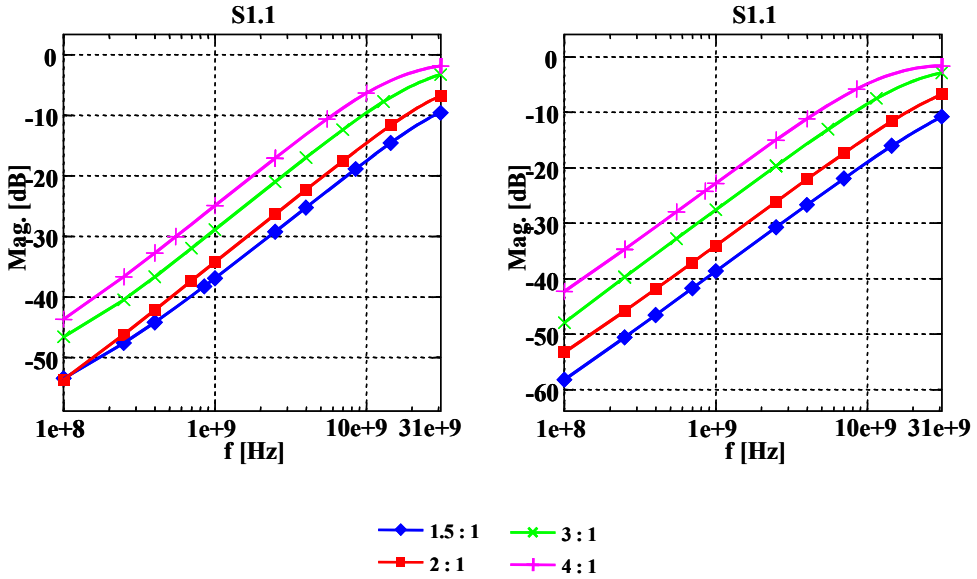

Figure 6. 15: $|S_{11}|$ of blind (left) and buried (right) vias with pad/hole ratios ranging from 1.5:1 to 4:1.

II) Adjust the Vertical Distance between Via and Reference Plane (s)

This design measure will be illustrated using the blind via shown in Figure 6. 10. The vertical distances between the via pad and the reference planes beneath and above the via were gradually increased from one-quarter to three-quarters the dimension of the diameter of the via pad. Each time this variation was made, the width of the connecting trace was adjusted to achieve 50 Ω. EM field computations of the resulting via configurations were performed and their extracted S-parameters were compared.

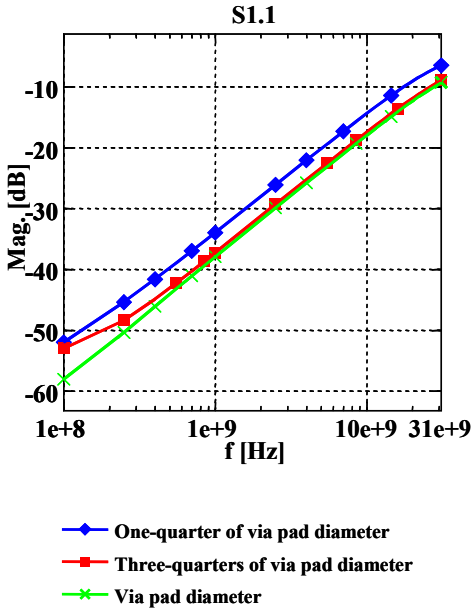

Figure 6. 16: $|S_{11}|$ of blind via for varying vertical distance between via and reference plane.

This comparison, as shown in Figure 6. 16 , reveals that the greater the distance between the via pad and the reference plane, the smaller the impedance mismatch between the via and the interconnecting trace. An increase in the vertical distance from one-quarter to three-quarters of the via pad diameter reduces the signal reflection from about 10% to 7% at 5GHz. However, from a separation of three-quarters the via pad diameter, the change in the amount of signal reflection caused becomes insignificant.

III) Use Interplane Vias to Control Inductance of Signal Vias

Interplane vias are used to interconnect power/ground layers in BGA packages as well as in other IC packages and multilayered boards in the case where both planes have the same potential. Each interplane via placed in the vicinity of a signal via serves as a path for the signal return current. Since the inductance of a signal via depends on the location of the return path associated with that signal via, it implies the via inductance and hence, its impedance can be tuned by a careful placement of interplane vias. To illustrate this fact, a 3D model (see Figure 6. 17) was set-up and the position of the interplane via was moved from a distance of 0.17 mm to 0.57 mm away from the signal via.

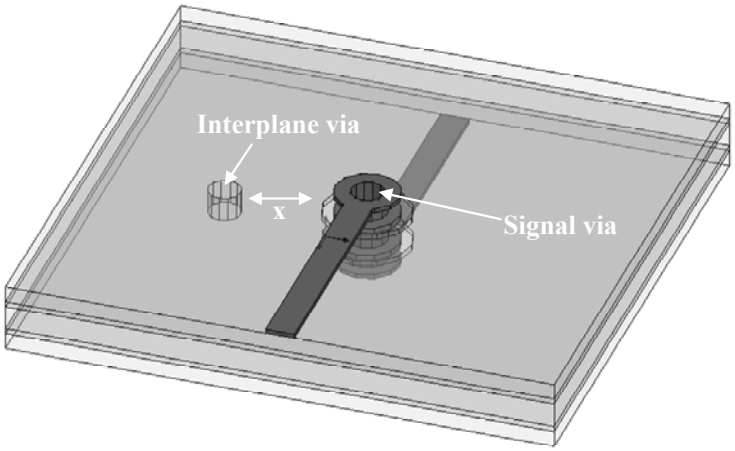

Figure 6. 17: 3D model of a signal via and an interplane via used for return current.

After each field computation, the circuit model of the via, developed and validated in the previous chapter was used for the extraction of its electrical parameters. As expected, the via capacitance remains approximately constant at about 170 fF, while its inductance increases steadily with distance away from the signal via, as can be seen in Figure 6. 18. The fact that the inductance of the signal via decreases as the interplane via is moved towards the signal via can be explained as follows: Bringing the interplane via closer to the signal via causes an increase in the partial mutual inductance between the vias. This larger partial mutual inductance then acts to decrease the total number of field line loops around each via.

This variation in the inductance of the signal via affects its impedance. Depending on whether the via is capacitive ($Z_{via} < Z_{trace}$) or inductive ($Z_{via} > Z_{trace}$), the interplane via can be kept further away or brought closer so as to increase or decrease the inductance of the signal via, thereby matching its characteristics impedance to that of the interconnecting trace. This then leads to a reduction in the amount of reflection that occurs, leading to better transmission characteristics of the via. Considering a capacitive via as an example, Figure 6. 19 shows an improvement in the magnitude of the transmission coefficient for frequencies greater than 10 GHz as the interplane via is moved from 0.17 mm to 0.57 mm away from the signal via.

In most designs, the planes are always interconnected using many interplane vias. In such cases, the inductance of the signal via becomes a function of the position of all nearby vias. Therefore, the inductance of the signal via, and hence its impedance can also be tuned by increasing or decreasing the number and arrangement of interplane vias in the vicinity of the signal via, as illustrated in the following example.

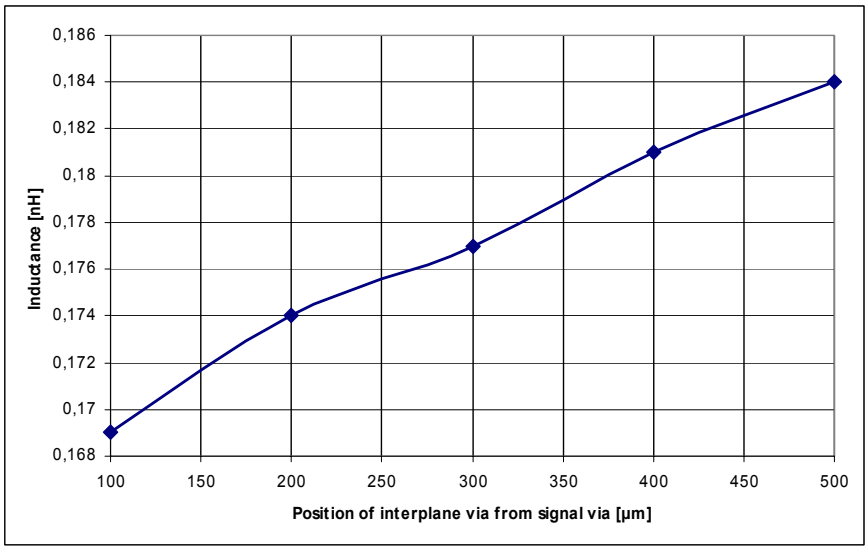

Figure 6. 18: Variation of the inductance of a signal via with the position, x, of interplane via away from the signal via.

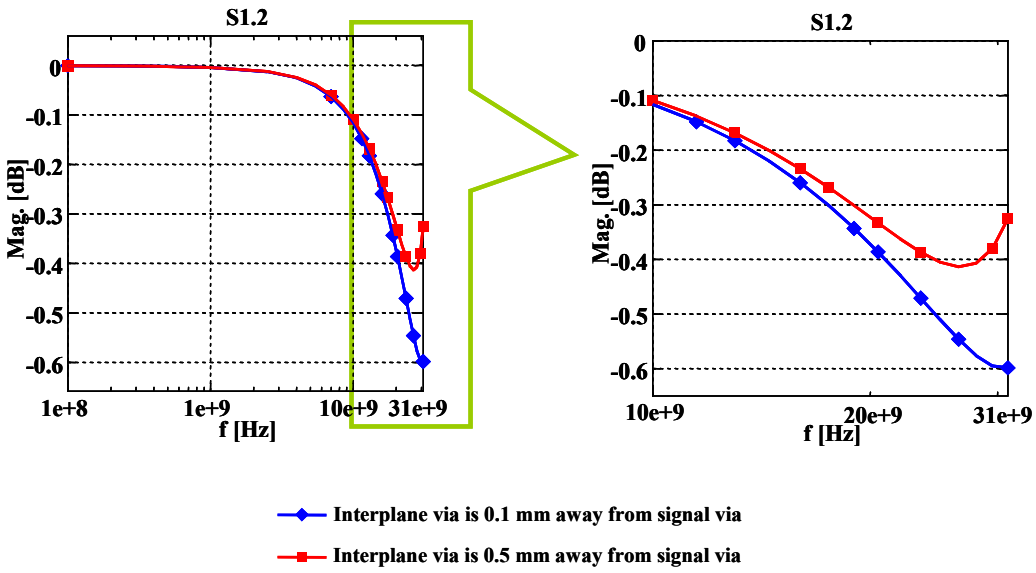

Figure 6. 19: Comparison of $|S_{12}|$ of a signal via with interplane the via placed at a distance of 0.17 mm and 0.57 mm away from the signal via.

In a circular manner, the number of interplane vias was gradually increased from one to four (one at a time), all the vias being at a distance of 0.17 mm away from the signal via. Each time an interplane via was added, a new EM field computation was performed. Figure 6. 20 shows the EM model in the case where four interplane vias were considered.

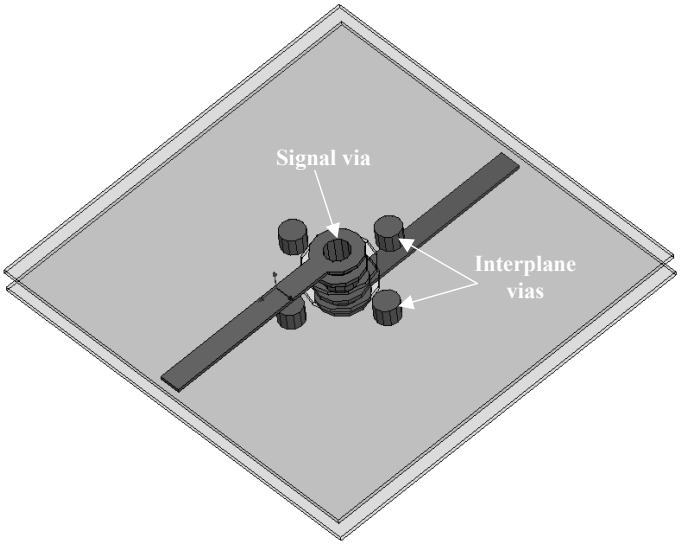

Figure 6. 20: 3D model of a signal via with four interplane vias used for return current. For illustrative reasons, the substrate layers are not shown.

From the computed S-parameters, the inductance and capacitance of the signal via were extracted. The results revealed that an increase in the number of interplane vias from one to four leads to an approximate decrease of 14% in inductance (see Figure 6. 21). Since the four interplane vias form a kind of a shield around the signal via, preventing stray EM fields, it implies the addition of other interplane vias behind the "shield" will have negligible influence on the via inductance. For example, by adding four more interplane vias, as shown in Figure 6. 22, leads to less than 1% change in the inductance of the signal via. By adding eight more interplane vias behind the "shield" consisting of eight interplane vias, making it a total of 16 interplane vias, causes approximately no change in the inductance value. In all these cases, the capacitance still remains approximately constant.

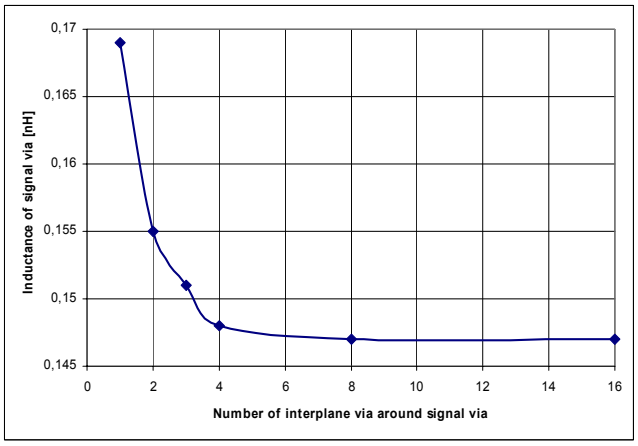

Figure 6. 21: Variation of the inductance of a signal via with the number and arrangement of interplane vias in the vicinity of the signal via.

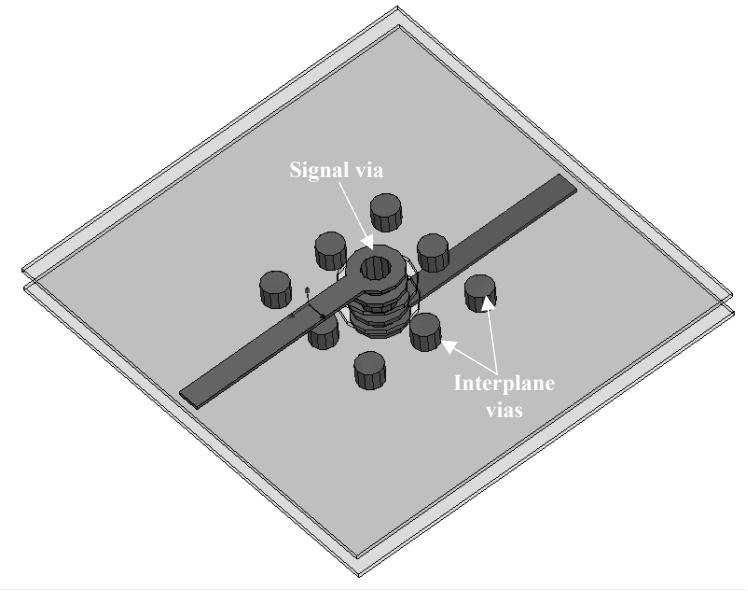

Figure 6. 22: 3D model of a signal via with eight interplane vias used for return current. For illustrative reasons, the substrate layers are not shown.

It can therefore be concluded that the first four interplane vias around the signal via, spaced at equal distances exert the lions share of influence upon the via inductance and hence its impedance. This technique of shielding signal vias with interplane vias was also used to reduce EM coupling between neighboring signal vias. This will be discussed in section 6.2.2.

6.1.2.2 Consideration of the Effects of Technological Tolerances at the Beginning of the Design Cycle

The sensitivity studies performed in section 6.1.1.2 revealed that fluctuations that occur during the fabrication process have a large impact on the RF performance of the critical components as well as on that of the entire module. Consequently, tight design measure must be used during the placement and routing of these components, so as to prevent these fluctuations. For example, for a via, keep fluctuations in pad diameter, space to ground, via height and dielectric constant of substrate less than 10% to keep fluctuations in the electrical parameters of the via, and hence those of the entire signal path, less than 10%. For a BGA ball, keep fluctuations in ball geometry (especially the height) less than 10% to keep its inductance less than 10%. Secondly, especially for applications above 5 GHz, great care must be taken to keep changes in ball height less than 30% so as to prevent the reflection and transmission behavior of the entire package from fluctuating by less than 30%.

6.1.3 Using Optimized Configurations of Critical Components to Minimize Reflections and Distortions in the Entire Module

By optimizing the performance of critical components, the RF performance of the entire module is automatically optimized. In order to know the amount of reflections and distortions minimized, a wideband circuit model that accounts for the parasitic effects of all package components is required (see Figure 6. 1). Values of electrical parameters of the segment that have been optimized will simply be inserted into this model, while electrical parameters of all other components are held constant. A comparison of the signal quality before and after the insertion of the optimized values reveals the level of optimization achieved. This is illustrated in Figure 6. 23, where an optimization of the performance of a blind via led to an optimization of the entire performance of the module. By reducing the pad-hole ratio from 4:1 to 1.5:1, the magnitude of the reflection coefficient is reduced by approximately 4dB throughout the frequency range considered. So, if all the critical components are considered, then the RF performance of the module will be greatly enhanced.

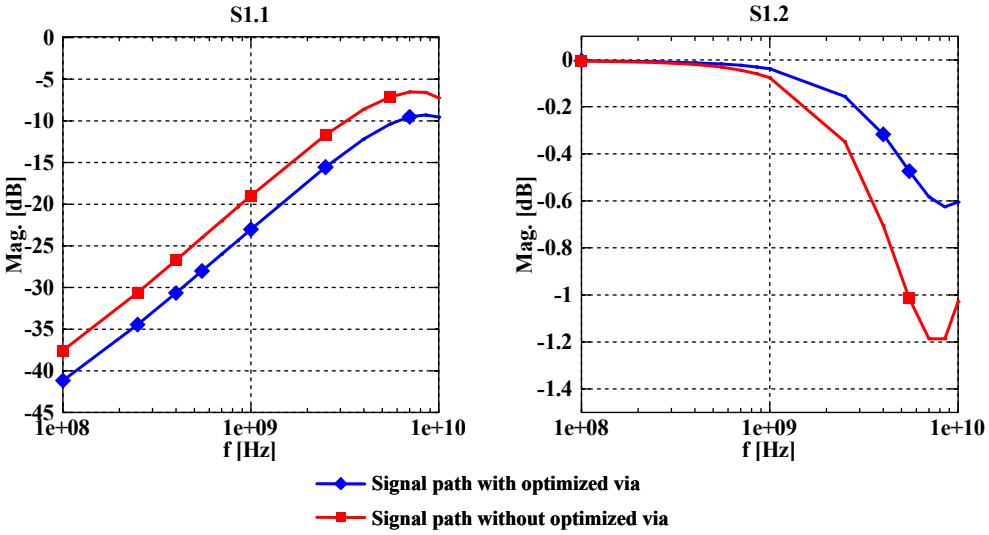

Figure 6. 23: Illustrating how the RF performance of a BGA module is optimized by optimizing the performance of a via.

6.2 Minimizing Cross-talk

In this section, techniques developed to minimize cross-talk between package traces and vias, developed in section 3.2.2, will be illustrated.

6.2.1 Minimizing Cross-talk between Package Traces

(3.78) and (3.79) describe the relationship between NEXT and FEXT, and the factors upon which they depend.

Considering NEXT as an example, it can be seen from (3.78) that the material properties of the substrate technology used play an integral role in determining NEXT. So in this work, an optimal substrate technology to reduce NEXT will be used. In order to make the choice of the material to be used, the following analysis was carried out:

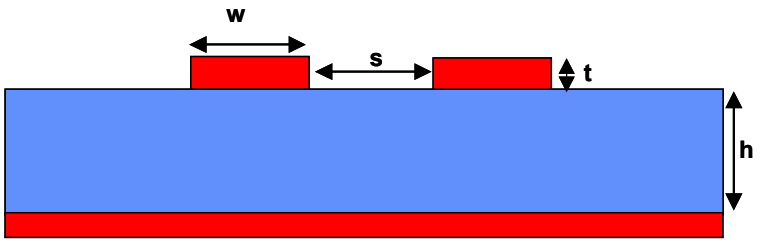

Figure 6. 24: Cross-sectional view of two-coupled microstrip traces.

Consider two-coupled microstrip lines shown in Figure 6. 24, as an example. In this Figure, *w* represents the trace width, t, the trace thickness, *s*, the distance of separation between the traces and h the substrate thickness. Now, to determine whether coupling between these lines for a given *s* is acceptable, the total noise margin must first be known. Typically, the noise margin is about 15% of the total voltage swing, but varies among device families. Of this 15%, about 5% of the swing is typically allocated to cross-talk. Since it was shown in [119] that irrespective of the number of aggressors coupling to a victim trace, more than 95% of the coupled noise is included if coupling from two adjacent aggressor lines is considered, it implies the spacing between any two adjacent lines must be large enough for NEXT to be less than 2%, so as to maintain the required noise margin. With this in mind, 2D EM field computations were performed for two coupled package traces on FR4, thick and thin film substrates. The electrical parameters of these substrates used for the field computations are shown in Table 6. 3 [120]. In all three cases considered, each transmission line was designed to have a characteristics impedance of 50 Ω, taking into consideration the geometrical limits of each technology. Using Maxwell 2D Extractor, the inductance and capacitance matrices of the coupled lines in each of these substrate technologies were computed. From these matrices, the cross-talk coefficients were obtained using the relationships in (3.78) and (3.79). In Figure 6. 25, the extracted coefficients of back-ward cross-talk, k_b, are plotted against the separation between the signal traces.

	Organic Substrate	Thick film Substrate	Thin film Substrate
	FR4	AL_2O_3 Ceramic 96%	AL_2O_3 Ceramic 99%
ε_r	4.2	9.2	10.2
tan δ	0.007	0.0023	0.0023

Table 6. 3: Relevant electrical parameters of FR4, thick and thin film substrates used for cross-talk analysis.

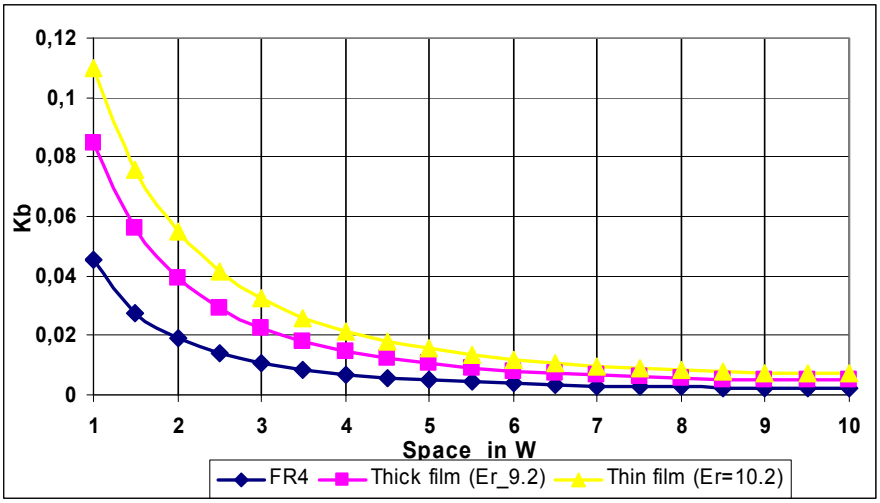

Figure 6. 25: Comparison of K_b for two-coupled microstrip lines in FR4, thick and thin film substrates.

Now, considering the cross-talk spec of 2%, it can be seen from Figure 6. 25 that a minimum separation of 2*w* is needed for two-coupled microstrip lines on FR4 substrate to satisfy the noise margin. However, for this same trace separation, NEXT increases by approximately 110% and 190%, if Al_2O_3 ceramic (thick film) and Al_2O_3 ceramic (thin film) substrates, respectively are used as the substrate material. These results show that the lower the relative dielectric constant of the material, the lower the cross-talk for the same routing pitch. In order to satisfy the 2% cross-talk spec, a minimum trace separation of $3^{1/2}w$ is required for Al_2O_3 ceramic (Thick film) and $4^{1/2}w$ for Al_2O_3 ceramic (thin film) substrates. Implying that the lower the relative dielectric constant of the material used, the tighter the routing pitch for the same cross-talk spec. Consequently, in order to reduce the size and cost of the board used, lower dielectric constants should be used whenever possible. However, the final decision on the choice of substrate used also depends on quite a number of other factors.

FEXT depends on the intrinsic terms that are based on the cross-section of the coupled lines as well as on two extrinsic terms – coupling length and rise time, as can be seen in (3.79). Hence, in addition to increasing the distance of separation between the lines, the maximum coupling length must also be reduced in order to reduce FEXT. Adding dielectric materials

above microstrip lines reduces FEXT and it is recommended that very sensitive lines should be routed in strip line.

6.2.2 Minimizing Cross-talk between Vias

It was shown in [121] that EM coupling between vias can be stronger than coupling between traces and is therefore not negligible in SI analysis of high-speed electronics packages. However, no design guidelines were proposed to reduce this coupling. In this work, a simple technique based on the principle of shielding EM energy from the signal via was used to reduce cross-talk. From the results of the investigations, an optimal arrangement of vias to reduce cross-talk is proposed.

Since cross-talk results from the interaction of magnetic flux from neighboring signal vias, it can be controlled if the flux from the aggressor is controlled. As illustrated in section 6.1.2.1, the magnetic flux of a single signal via can be controlled through optimal placement of interplane vias around the signal via in a circular manner. To deduce the most optimal arrangement of these interplane vias in the case of two-coupled signal vias, three configurations were examined using HFSS. The 3D models used for field computations are shown in Figure 6. 26 and in Figure 6. 27, the coupling coefficients of S-parameters extracted from these configurations are compared.

As expected, the least amount of EM coupling between the signal vias occurs in the case where each of the signal vias is shielded with three interplane vias and there is an additional interplane via between the signal vias (see Figure 6. 26 – buttom). The presence of this interplane via reduces the magnetic flux intensity between the signal vias, thereby reducing considerably the inductive coupling that occurs. Using the equivalent circuit model of two-coupled vias, shown in Figure 4.41, mutual inductances between the signal vias were extracted for all three cases. 9 pH, 4 pH and 2 pH were obtained for the configuration on the top left, top right and bottom, respectively. A comparison of these values revealed that by moving from the configuration shown in Figure 6. 26 – left to that in Figure 6. 26 – right, the inductive coupling reduces by approximately 55%. This great reduction in the mutual inductance is attributed mainly to the presence of the interplane via between the signal vias. Moving from the configuraton shown in Figure 6. 26 – right to the configuration in Figure 6. 26 – bottom, leads to a reduction in mutual inductance of approximately 50%. This is mainly due to the increase in the number of interplane vias which shield each of the signal vias, thereby reducing its inductance and automatically, the mutual inductance between the vias. Finally, moving from the configuration shown in Figure 6. 26 – top left to the configuration in Figure 6. 26 – bottom leads to a reduction in mutual inductance of approximately 75%.

From these investigations, it can be seen that through optimal placement of interplane vias in a package, the inductive coupling between neighboring vias can be reduced by up to 75%.

Therefore use at least four ground vias (preferably interplane plane vias whereever possible) to shield vias carrying high-speed signals so as to prevent EM coupling to other package components.

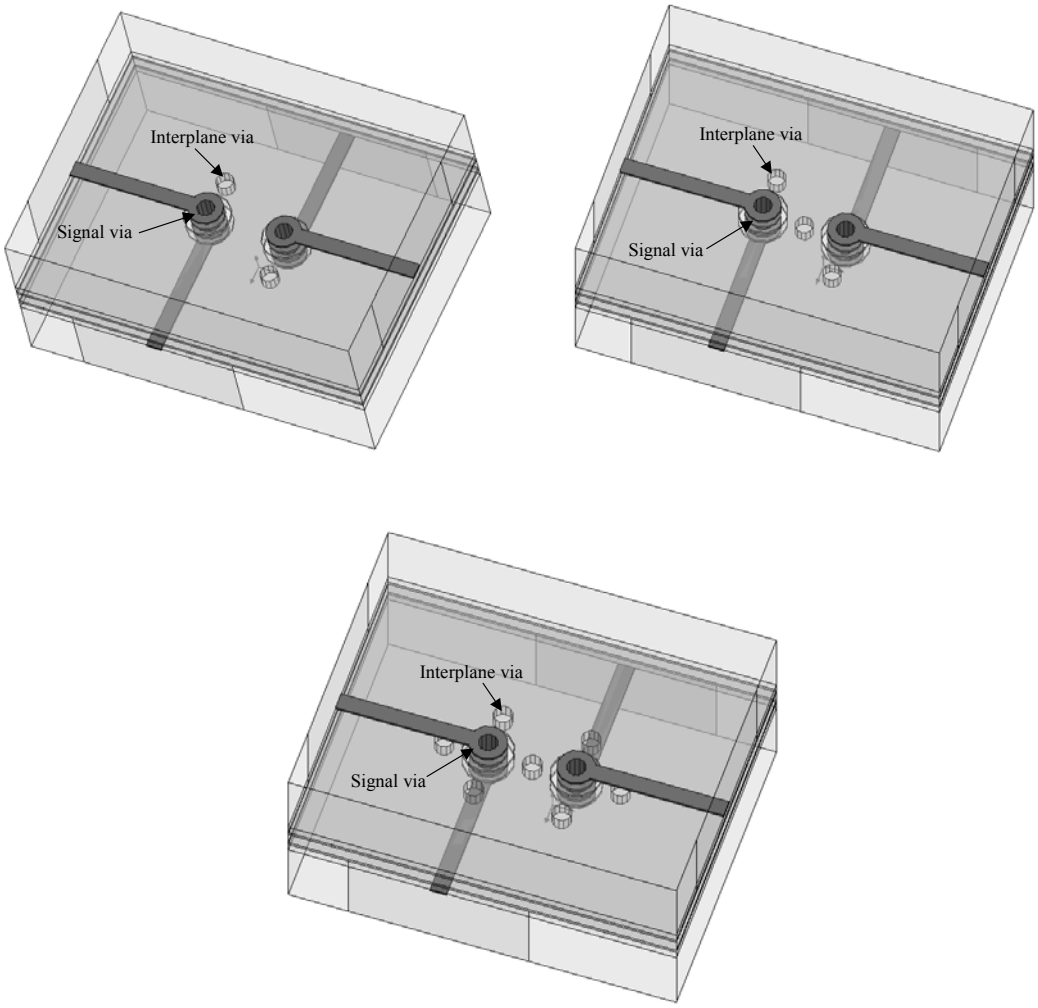

Figure 6. 26: 3D models used for investigating cross-talk between neighboring signal vias.

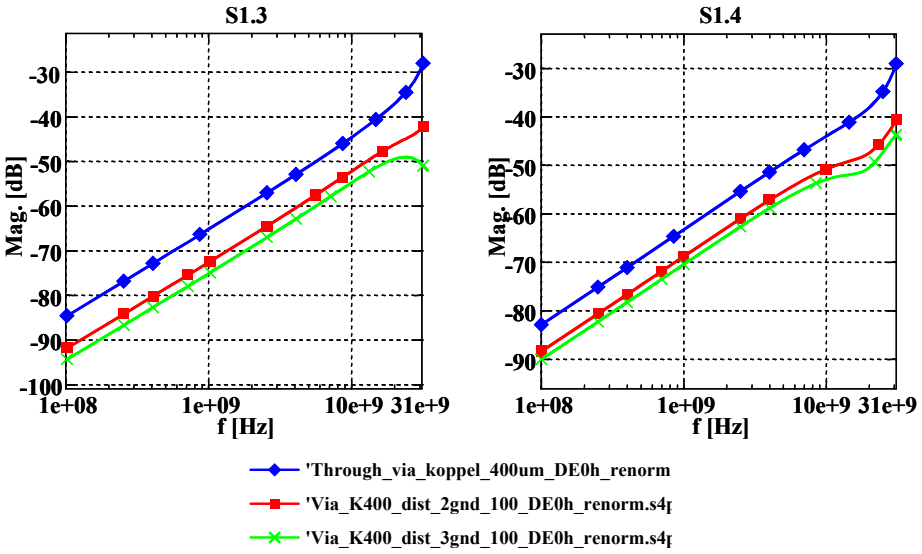

Figure 6. 27: S-parameters designating EM coupling between two-coupled signal vias for the three configurations shown in Figure 6. 26.

6.3 References

[117] Antonio, G., et al, "S-parameters characterization of through, blind, and buried via holes", *IEEE Transactions on Mobile Computing*, Volume: 2, Issue: 2, Pages: 174-184, April-June, 2003.

[118] Ndip I., John W., Reichl H., "RF/microwave modeling and comparison of buried, blind and through-hole vias", *6th IEEE Electronics Packaging Technology Conference (EPTC 2004)*, Singapore, December 8-10, 2004, pp. 643 – 648.

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[121] Zhao J., Fang J., „Significance of electromagnetic coupling through vias in electronics packaging", *6th IEEE Topical Meeting on Electronic Performance of Electronic Packaging*, pp. 135-138, 1997.

Chapter 7

Summary and Conclusions

In this work, a novel approach, the M3-approach (methodologies->modeling->measures), for optimal, cost-effective and reliable electrical design of SiP modules as well as other complex chip packages and boards for RF and high-speed applications was developed and illustrated using a ball grid array (BGA) package module as an example.
With the aid of the novel methodologies developed and illustrated in this work, it is now possible for the first time ever to:

1. Develop wideband models for complete signal paths in SiP modules and other advanced chip packages as well as multilayered PCBs that account for the parasitic effects of all interconnecting components at microwave frequencies. These models can be used to track-down and solve signal integrity problems before they occur in the actual design, thereby saving time and money.

2. Define the electrical boundaries of all geometrical discontinuities in electronic packages and PCBs. Defining these boundaries enable the following:

   a. **Wideband modeling of complete signal paths in SiP modules and other advanced chip packages as well as multilayered PCBs***:* In order to develop wideband models for these paths, the paths must first be segmented, followed by an extraction of lumped/distributed element models for each segment and then cascading the resulting models to increase bandwidth. However, since electronic packages and boards consist almost entirely of discontinuities, this segmentation can only be done at points away from each discontinuity where fields of HOMs have vanished or are considered insignificant and mainly the TEM mode is present. This is mainly because lumped/distributed element modeling is based on TEM wave theory. As was illustrated in section 4.2.2.4, without defining the electrical boundaries of these discontinuities, a conventional circuit-theory-based analysis fails to accurately capture the effects of a discontinuity. Consequently, defining the electrical boundaries of each package/board discontinuity is a pre-requisite for efficient and accurate wideband

modeling and analysis of complete signal paths in electronic packages and boards for RF/high-speed applications.

b. **Efficient and accurate EM field computation of package and PCB components:** To perform 3D full-wave EM field computations of package/board components using conventional EM field solvers, they are connected to ports using uniform transmission lines (e.g., microstrip, stripline...), which represent the actual configuration of traces in the package or board. The length of the transmission line used for this interconnection depends on the electrical boundaries of the discontinuity under consideration, and it determines the accuracy, duration and memory requirements of the field computation. If the transmission line is too short, HOMs excited at the discontinuity will be captured at the ports. This may lead to erroneous results. If the line is longer than required, then the field computation time and memory required will increase, leading either to unsuccessful computations due to insufficient memory or computations that may run for days, instead of just a few hours.

c. **Accurate and cost-effective RF design of test structures:** In designing test structures for RF measurements of package/board components, appropriate lengths of uniform transmission lines are also needed to interconnect the device under test and adapters on which the probes are contacted. If these lines are too long, then the overall size of the test board will increase, leading to more cost. Further more, the measurement results will be more prone to errors, because longer lines are more sensitive to technological tolerances which occur during the fabrication process, especially at RF/microwave frequencies. On the other hand, if the lines are too short, then HOMs excited at the discontinuity will be captured at the ports of the vector network analyzer, leading to erroneous results. The most appropriate length of line required to minimize cost, while simultaneously ensuring accurate RF/microwave characterization depends on the electrical boundaries of the discontinuity under consideration.

3. Characterize bump arrays, irrespective of the number of bumps in the array. This facilitates a thorough analysis of cross-talk in an earlier stage of the design cycle. Based on the results obtained, design measures to minimize cross-talk can then be derived and implemented.

The methodologies, models and measures developed in this work also enable

1. accurate assessment and choice of the most optimal technology,
2. controlled, reliable and cost-effective design,
3. parameterization of all components along complete signal paths (chip-to-board) for efficient and accurate system-level signal integrity analysis and an

4. implementation as a pre-layout algorithm in an EDA/CAD tool for comprehensive system design.

Some of the design guidelines developed for minimizing reflections and cross-talk are summarized below:

1. Minimizing Reflections

    a. Optimal choice and design of discontinuities

        i. Use 45° bends to facilitate horizontal routing, instead of 90° or chamfered 90° bends, whenever possible.

        ii. For the interconnection of signal layers in multilayered substrates, use through-hole vias instead of buried or blind vias of the same size, if the vias are capacitive. If they are inductive, then use either buried or blind vias, depending on the layer stack-up.

        iii. One through-hole via used for vertical routing causes more reflections than at least four 90° bends or six 45° bends along a signal path of the same length. Hence, more effort has to be concentrated on minimizing the discontinuity effects of vias.

        iv. The following measures should be applied to reduce via effects:

            1. Adjust the pad/hole ratio to match impedance of interconnecting traces to that of via. This is applicable to buried, blind and through-hole vias.

            2. The vertical distance between blind and buried vias and the nearest reference plane(s) must be increased or decreased accordingly, so as to match the via and trace impedances.

            3. Use interplane or ground vias to control the inductance of a signal via, hence its impedance.

            4. Eliminate pads at reference planes and/or logically increase the size of the clearance hole, so as to decrease the via capacitance and hence increase its characteristics impedance. This can be used to match the impedance of capacitive vias and their connecting traces.

            5. If possible, holes can be bored in the reference plane(s), directly above and/or underneath buried and blind via pads.

6. Use smaller vias, whenever possible.

b. Maximum number of bends before SI problems occur

   i. For applications above 10 GHz use less than four 90° bends along a signal path less than or equal to 2.5 mm to keep reflections less than 10 %.

   ii. Effects of at least four 45° bends on the RF performance of the entire module can be neglected for frequencies up to 25 GHz. For higher frequencies and more bends, perform 3D analysis, prior to design.

c. Maximum allowable technological fluctuations

   i. For frequencies up to 25 GHz, the impact of up to 30 % fluctuation in the geometry of a flip chip can be neglected, if the signal path is not disconnected through this fluctuation.

   ii. Keep changes in w, h and ε_r below 10% to keep fluctuations of the characteristics impedance as well as the reflection coefficient < 10%.

   iii. Keep fluctuations in pad diameter, space-to-ground, via height and dielectric constant of substrate < 10% to keep fluctuations in the electrical parameters of the via, and hence those of the entire signal path, < 10%.

   iv. Effects of up to 30% variation in tan δ on both L and C of a via can be neglected. This also applies to the hole displacement, if the interconnecting signal trace is not disconnected by such a fluctuation.

   v. Keep fluctuations in geometry of a signal BGA ball (especially the height) < 10% to keep its inductance less than 10%. Secondly, especially for applications above 5 GHz, great care must be taken to keep changes in ball height < 30% so as to prevent the reflection and transmission behavior of the entire package from fluctuating by up to 30%.

2. Minimizing Cross-talk

a. Minimum pitch between signal paths

   i. Use substrates with lower relative dielectric constants. The lower the dielectric constant, the tighter the routing pitch for the same cross-talk

spec. Hence, in order to reduce the size and cost of the board used, lower dielectric constants should be used whenever possible.

ii. To keep NEXT less than 2%, a minimum trace separation of $2w$, $3^{1/2}$ w and $4^{1/2}$ w are needed for 50 Ω lines in FR4, Al_2O_3 ceramic (thick film) and Al_2O_3 ceramic (thin film) substrates.

b. Optimal arrangement of signal and power/ground vias

i. Use at least three power/ground or interplane vias beside the aggressor via and one power/ground or interplane via between the victim and aggressor to reduce cross-talk by at least 50%.

Applying the M3-approach developed in this work at the beginning of the design cycle of SiP modules or any other complex chip package/board leads to the elimination of re-design efforts and place/route iterations. Consequently, time-to-market as well as cost is considerably reduced, while performance is optimized.

List of Figures

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International Awards, Published Papers and Invited Talks

I) Awards

1) **Best Paper of Session Award** at the 36th International Symposium on Microelectronics (**IMAPS 2003**) in Boston, MA, U.S.A., Nov. 16-20, 2003, for the paper entitled "*A Novel Modelling Methodology of Bump Arrays for RF and High-Speed Applications*".

2) **2005 Best Poster Paper Award** at the 55th IEEE Electronics Components and Technology Conference (**ECTC 2005**) in Lake Buena Vista, FL, U.S.A., May 31 - June 3, 2005, for the paper entitled, "*Effects of Discontinuities and Technological Fluctuations on the RF Performance of BGA Packages*".

3) **Silver Leaf Certificate Award** at the 2nd IEEE Conference on Ph.D. Research in Microelectronics and Electronics (**PRIME 2006**) in Otranto (Lecce), Italy, June 11-15, 2006, for the paper entitled, "*A Novel Methodology for Defining the Boundaries of Geometrical Discontinuities in Electronic Packages*".

II) Published Papers

2003

[1] Ndip I., et al., "RF Modelling of Single and Coupled Flip Chip Interconnects on HDI Substrates", *14th European Microelectronics and Packaging Conference & Exhibition (IMAPS Europe)*, June 23-25, 2003, pp. 190-195.

[2] Ndip I., Sommer G., John W., Reichl H., "A Novel Modelling Methodology of Bump Arrays for RF and High-Speed Applications", *36th International Symposium on Microelectronics (IMAPS 2003)*, Boston, November 16-20, 2003, pp.992-997.

2004

[3] Ndip I., Sommer G., John W., Reichl H., "Bump Arrays for RF Applications", *Advanced Packaging*, pp. 31- 33, May 2004, Nashua, NH, U.S.A.

[4] Ndip I., Sommer G., John W., Reichl H., "Methodology for Efficient Modeling of BGA Packages at RF/Microwave Frequencies", *37th International Symposium on Microelectronics (IMAPS 2004)*, Long Beach, CA, U.S.A, November 16-20, 2004.

[5] Ndip I., John W., Reichl H., "RF/Microwave Modeling and Comparison of Buried, Blind and Through-Hole Vias", *6th IEEE Electronics Packaging Technology Conference (EPTC 2004)*, Singapore, December 8-10, 2004, pp. 643 – 648.

2005

[6] Ndip I., Sommer G., John W., Reichl H., "Characterization of Bump Arrays at RF/Microwave Frequencies", *Elsevier Journal of Microelectronics Reliability*, vol. 45, Issue 3-4, March-April 2005, pp. 551-558.

[7] Ndip I., John W., Reichl H., "Effects of Discontinuities and Technological Fluctuations on the RF Performance of BGA Packages", *55th IEEE Electronics Components and Technology Conference (ECTC 2005)*, Lake Buena Vista, FL, U.S.A, May 31 - June 3, 2005, pp.1769 – 1775.

[8] Ndip I., John W., Reichl H., Thiede A., "A Novel Approach for Modeling and Optimization of BGA Packages", *IEEE Conference on Ph.D. Research in Microelectronics and Electronics (IEEE PRIME 2005)*, July 25-28, 2005, Lausanne, Switzerland, pp. 437-440.

[9] Ndip I., John W., Reichl H., "Efficient RF/Microwave Modeling of Discontinuities in Chip Packages and Boards", *35th IEEE European Microwave Conference (European Microwave Week 2005)*, Paris, France, October 3 - 7, 2005, pp. 165 – 168.

[10] Ndip I., John W., Reichl H., "Modeling and Optimization of SiP Modules for RF/High-Speed Applications", *ENCAST Workshop*, Zurich, Switzerland, November 8 - 9, 2005.

[11] Ndip I., John W., Reichl H., "Minimizing Reflections and Cross-Talk in Chip Packages", *7th IEEE Electronics Packaging and Technology Conference (EPTC 2005)*, Singapore, December 7 - 9, 2005, pp. 43 – 48.

2006

[12] Ndip I., Reichl H., Guttowski S., "A Novel Methodology for Defining the Boundaries of Geometrical Discontinuities in Electronic Packages" *IEEE Conference on Ph.D. Research in Microelectronics and Electronics (IEEE PRIME 2006)*, June 11-15, 2006, Otranto (Lecce), Italy, pp. 193-196.

[13] Ndip I., Guttowski S., Reichl H., "RF/Microwave Modeling of SiP Modules – A Novel Approach" *39th International Symposium on Microelectronics (IMAPS 2006)*, San Diego, CA, U.S.A, October 8-12, 2006.

2007

[14] Ndip I., Guttowski S., Reichl H., "Accurate Characterization of Package and Board Components for Efficient System Level Signal Integrity Analysis" Accepted for Presentation and Publication at the *2007 IEEE International Symposium on EMC*, Honolulu, Hawaii, U.S.A, July 8-13, 2007.

III) Invited Talks/Guest Speaker

2005

[15] Ndip I., John W., Reichl H., "Development of Wideband Models for Complete Signal Paths in Multi-Layered Chip Packages and Boards" *Agilent's Seminar on Using ADS for Signal Integrity Design,* Winnersh, (UK) Boeblingen (Germany), Hannover, (Germany) Aalborg (Denmark) Rome (Italy), June 13-17, 2005.

[16] Ndip I., John W., Reichl H., "Wideband Modeling and Optimization of Complete Signal Paths in IC Packages and Boards" *Agilent's Workshop,* Paderborn, Germany September 22, 2005.

[17] Ndip I., John W., Reichl H., "A Novel Methodology for Efficient Modeling and Optimization of Complete Signal Paths in IC Packages and PCBs", *Zuken's 3rd European Design Automation Conference (ZEDAC)*, Cologne, Germany, November 7 - 8, 2005.

[18] Ndip I., John W., Reichl H., "Wideband Modeling and Optimization of SiP Modules for RF/High-Speed Applications" *5th International Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo),* Munich, Germany, November 28 – 30, 2005.

2006

[19] Ndip I., Guttowski S., Reichl H., "RF Design Considerations for High-Speed Packages and PCBs" Accepted for Publication in *Zuken's 4th European Design Automation Conference (ZEDAC 2006)*, Ulm, Germany, October 24 - 26, 2006.

2007

[20] Ndip I., Maaß U., Salhi F., "Optimaler elektrische Entwurf von Chip Gehäusen, Leiterplatten und eingebetteten passiven Komponenten unter Verwendung des M3-Ansatzes" Accepted for Presentation and Publication at *SMT/Hybrid/Packaging 2007-Exibition and Conference*, Nürnberg, Germany, April 24 - 26, 2007.

Short Biography

Ivan Ndip

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Ivan Ndip was born on the 16th of December 1976 in Ossing-Manyu, Cameroon. He obtained his M.Sc. and Ph.D. (Summa Cum Laude) degrees in Electrical Engineering from the Technical University Berlin in 2002 and 2006, respectively.

In 2000, he joined Fraunhofer IZM Berlin and was engaged, up to 2002, in RF/microwave characterization of chip-to-package interconnections and transmission lines. From 2002 to 2005, Ivan Ndip conducted his doctoral research on wideband modeling & optimization of System-in-Package modules under the supervision of Prof. Dr.-Ing. Dr.-Ing. E.h. Herbert Reichl, while simultaneously working as a Research Engineer on signal integrity design of electronic packages/boards as well as on antennas. He was also affiliated with the Chair for High Frequency Electronics, University of Paderborn.

In June 2005, Ivan Ndip was appointed as Group Manager of RF Modeling & Simulation Group – a position he held till January 2006. During this period, he developed novel R&D concepts that led to the establishment of a new research group, RF & High-Speed System Design Group, at Fraunhofer IZM. Since February 2006, he has been Group Manager of RF & High-Speed System Design, where he works on, and leads R&D projects that currently focus on electrical design, characterization and analysis of microelectronic packages/boards, embedded passives and integrated antennas.

At the 36th International Symposium on Microelectronics (IMAPS 2003) in Boston, U.S.A., Ivan Ndip received *Best Paper of Session Award* for his contribution in the field of modeling and characterization of bump arrays. He was also recipient of the *2005 ECTC Best Poster Paper Award* for his work on the impact of discontinuities and technological fluctuations on RF performance of BGA packages, presented at the 55th IEEE Electronic Components and Technology Conference (ECTC 2005) in Lake Buena Vista, FL, U.S.A. In recognition of the significant quality of his doctoral research work, Ivan Ndip also received a *Silver Leaf Certificate Award* at the IEEE Conference on Ph.D. Research in Microelectronics and Electronics (PRIME 2006) in Otranto (Lecce), Italy, for his excellent paper that presented for the first time ever, a methodology for defining the electrical boundaries of all geometrical discontinuities in electronic packages and PCBs.

Ivan Ndip is a member of the International Microelectronics and Packaging Society (IMAPS), the Institute of Electrical and Electronics Engineers (IEEE) and the Association of German Electrical Engineers (VDE).