Interdigitated Back Contact Silicon Heterojunction Solar Cells

From the Laboratory to Industrial Processes

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Abstract

This work follows two routes: the first one explores the efficiency potential of IBC SHJ solar cells built with a rather complex process, the second one shows ways to make this efficiency potential actually industrially accessible by developing an appropriate, simplified manufacturing process.

In chapter 4, both manufacturing processes are discussed. In the first part, the established photolithography process is extensively described, emphasising its complexity, and subtle but crucial optimisations to the process are introduced: improved photoresist adhesion, evaporation-based metallisation increasing the reliability of the ITO etch process and, most importantly, the non-destructive protective layer etching.

The second part of chapter 4 describes the development of an industrially viable manufacturing process based on structured silicon wafers serving as shadow masks to pattern a-Si:H and nc-Si:H in-situ during the PECVD deposition process. Challenges arising from the laser-ablation based mask manufacturing, the accuracy and fidelity of the patterned layers, and the alignment system are analysed and discussed: tapering effects caused by the surface diffusion of SiH_3 radicals under the masks were found to limit the fidelity of the patterned layers, making adjustments to the cell design with respect to the contact finger widths and metallisation gaps necessary. Furthermore, an alignment system based on laser-drilling holes, matching with the metal pins on a custom-made aluminium carrier, into the respective wafers was developed.

The results of the various IBC-SHJ solar cells built during this work are presented and analysed in chapter 5. Photolithography-based cells with a direct, annealed aluminium metallisation achieve considerably better results than equivalent cells with an ITO/Ag metallisation (efficiency of 20.7 vs. 19.2 %). With an improved front side passivation the aluminium-based cells reach efficiencies up 22 %. The properties of the Al/a-Si:H contact system strongly depend on the annealing time and temperature. Moderate annealing likely leads to the formation of an intermediate aluminium silicide and initialises the crystallisation of the doped a-Si:H layers, which results in the reduction of the contact resistivity and thus in an increase of the FF. Extended annealing leads to strong interdiffusion between the aluminium and amorphous silicon layers eventually resulting in the disintegration of the latter and thus the deterioration of the passivation quality. In these cases, the consequential V_{OC} losses cannot be compensated by the increase of the FF.

The second part of chapter 5 focuses on the development of photolithography-based solar cells with TCO contacts. Owing to a different front-side layer stack, prioritising passivating over optical properties, as well as optimised a-Si:H deposition processes and film thicknesses, the efficiency of ITO-based IBC SHJ solar cells was increased by

4 %abs, from 19.2 to 23.2 %. Calculations of the implied FF and Suns-V_{OC} measurements indicate that the solar cells are mainly limited by high series resistances leading to FF values well below 80 %. Based on TLM measurements, the contact resistivities, in particular the one of the p-contact stack, were identified to be the main series resistance contributor. Thinning the intrinsic a-Si:H passivation layers and switching to a textured rear side led to substantial improvements of both the contact resistivities and the FF. Additionally, AZO was investigated as an alternative TCO material replacing ITO. The latter was found to form a better contact to the p-type a-Si:H layers, likely related to its higher work function, while the former yielded a better optical response resulting in a higher j_{SC}. Moreover, initial results of IBC SHJ solar cells with a WO_X interlayer between the p-type a-Si:H emitter and the TCO (ITO in this case) show slightly lowered p-contact resistivities, indicating the potential of high work function metal oxides as emitter contact materials.

In the last part of the chapter the very first results of IBC SHJ solar cells manufactured with the shadow mask process are presented. Cells with a screen-printed metallisation on an AZO layer reach decent V_{OC} and j_{SC} values (41 mA/cm^2, 700 mV). However, the efficiency does not exceed 10 %, as the corresponding jV curves are strongly S-shaped and the jV-derived FF is limited to values around 30 %. The latter is most likely related to a malfunctioning emitter/TCO contact or a too thick intrinsic a-Si:H passivation layer. A second batch of solar cells built with a further developed shadow mask process – optimised alignment system, a-Si:H processes identical to the ones used for the best photolithography-based solar cells and a more accurately patterned ITO/Ag metallisation – yielded solar cells with efficiencies up to 17, and FF values up to 66 %. V_{OC} values are particularly low (616 mV), as the emitter passivation degrades during the metallisation.

Chapter 6 discusses the prospects of IBC SHJ solar cells with respect to industrial fabrication and marketability. With respect to high-efficiency concepts aiming for cell efficiencies above 25 %, top- and rear-contacted SHJ solar cells are identified to likely be the main competitor for IBC SHJ solar cells. The latter can only succeed if simple manufacturing processes are employed. Based on the state of IBC SHJ research, shadow-mask based processes show the most potential, as the complexity of the manufacturing process does not substantially differ from standard SHJ processes and cell efficiencies close to 24 % have been demonstrated. The implications of a shadow mask process on the contact geometry of IBC SHJ solar cells (larger contact finger widths and metallisation gaps) are also analysed with a simulation study. The results indicate only minor efficiency losses due to process related contact geometry adjustments.

Zusammenfassung

Einseitig kontaktierte Silizium-Heterostruktursolarzellen (IBC-SHJ) haben das Potential höchste Wirkungsgrade zu erreichen. Diese Arbeit beschäftigt sich mit den Herstellungsprozessen sowie der Optimierung des Kontaktdesigns derartiger Solarzellen. Der Fokus lag hierbei einerseits auf der Weiterentwicklung und Verbesserung des etablierten Photolithographieprozesses sowie andererseits auf der Entwicklung eines alternativen, industriekompatiblen Herstellungsverfahrens, basierend auf der Strukturierung amorpher und nanokristalliner Siliziumschichten in situ mittels geeigneter Schattenmasken während der jeweiligen PECVD-Prozesse (Schattenmaskenprozess).

Die im vierten Kapitel beschriebenen Verbesserungen des Photolithographieprozesses umfassen die Lackhaftung, die Reproduzierbarkeit des ITO-Ätzschrittes und das Vermeiden der Degradation der frontseitigen Antireflexschicht während des Ätzens der darauf befindlichen a-Si-Schutzschicht. Der zweite Teil des vierten Kapitels befasst sich mit der Entwicklung des Schattenmaskenprozesses. Durch Laserstrukturierung wurden hierfür geeignete Masken aus Siliziumwafern hergestellt sowie zwei Alignierverfahren entworfen und hinsichtlich ihrer Genaugikeit und Praktikabilität analysiert. Die Strukturtreue der durch die Masken abgeschiedenen a-Si-Schichten wurde mittels Raman-Profilmessungen analysiert. PECVD-Prozesse, in denen die Schichtdeposition durch die Diffusion der SiH_3-Radikale hin zur Oberfläche limitiert ist, zeigten diesbezüglich bessere Ergebnisse als Prozesse, in denen SiH_3-Radikale vermehrt auf der Oberfläche unter die Maske diffundieren können.

Die Eigenschaften der für diese Arbeit hergestellten IBC-SHJ Solarzellen werden im fünften Kapitel vorgestellt. Dabei lag der Fokus im Speziellen auf der Optimierung der Rückkontaktstrukturen der mit dem Photolithographieprozess hergestellten Solarzellen. Solarzellen mit direkten, getemperten Al/a-Si:H-Kontakten erreichten höhere Wirkungsgerade als entsprechende Referenzzellen mit konventionellen ITO/Ag-Kontakten (19,2 zu 20,7 %). Durch eine verbesserte Frontseitenpassivierung konnte die Effizienz der aluminiumbasierten Solarzellen auf bis zu 22 % erhöht werden. Die Eigenschaften des Al/a-Si:H-Kontaktes hängen maßgeblich von der Temperatur und Zeitdauer des Temperschrittes ab. Moderates Tempern ($T = 150$ bis 160 °C, 20 bis 30 Minuten) führt zur Bildung eines Aluminiumsilizides sowie einer partiellen Kristallisation des amorphen Ausgangsmaterials. Beide Effekte verringern den Kontaktwiderstand zwischen der Aluminiummetallisierung und den dotierten a-Si:H-Schichten, wodurch der Füllfaktor steigt. Wird die Temperatur des Temperschrittes weiter erhöht, kommt es verstärkt zu Diffusionsprozessen zwischen den Aluminium- sowie den amorphem Siliziumschichten und in der Folge zu einer teilweisen Auflösung letzterer. Der daraus resultierende Verlust der Oberflächenpassivierung und die folgliche Reduktion der Leerlaufspannung können

in der Regel nicht durch einen weiteren Anstieg des Füllfaktors ausgeglichen werden, sodass die Effizienz der Solarzelle wieder sinkt.
Der zweite Teil des fünften Kapitels beschreibt den Optimierungsprozess von IBC-SHJ-Solarzellen mit TCO-basierten Kontakten. Durch das Einfügen einer amorphen Siliziumschicht wurden die Passivierungseigenschaften des frontseitigen Schichtstapels substantiell verbessert. Des Weiteren wurden die PECVD-Prozesse und die Schichtdicken der rückseitigen a-Si:H-Schichten optimiert. Folglich konnte die Effizienz von Solarzellen mit ITO/Ag-Kontakten um 4 %abs, von 19,2 auf 23,2 % erhöht werden. Mittels einer Füllfaktoranalyse – Vergleich von implizitem und Pseudo-Füllfaktor – wurde der Serienwiderstand als dominanter Verlustmechanismus identifiziert. TLM-Messungen zeigen, dass hohe Serienwiderstände zu einem großen Teil auf einen entsprechend hohen Kontaktwiderstand des p-Kontaktes zurückzuführen sind. Ein Reduktion des letzteren konnte durch eine Verringerung der Schichtdicke der intrinsischen a-Si:H-Passivierschicht erreicht werden, eine Reduktion des gesamten Serienwiderstandes durch den Einsatz einer texturierten anstelle einer planaren Rückseitenoberfläche. Zudem wurde aluminiumdotiertes Zinkoxid (AZO) als alternatives TCO-Material untersucht. Im Vergleich zu ITO weist AZO eine höhere Transparenz im nahen Infrarotbereich auf, wodurch die parasitäre Absorption an der Zellrückseite vermindert wird. Dieser Vorteil wird jedoch durch einen hohen Kontaktwiderstand zum p-dotierten a-Si:H-Emitter kontrastiert. Letzteres führt zu einer Reduktion des Füllfaktors. Des Weiteren wurde Wolframoxid als Emitter-exklusives Kontaktmaterial untersucht. Erste Solarzellen mit einer dünnen Wolframoxidschicht zwischen dem p-dotiertem a-Si:H-Emitter und der TCO-Schicht (ITO) erreichten Effizienzen auf dem Niveau der entsprechenden Referenzzellen (Standardkontakt ITO/Ag), und wiesen darüber hinaus tendenziell niedrigere p-Kontaktwiderstände auf.
Im letzten Teil des fünften Kapitels werden die initialen Ergebnisse von mittels Schattenmaskenprozess hergestellten IBC-SHJ-Solarzellen diskutiert. Zellen mit einer Siebdruckmetallisierung und einem AZO-Schicht als TCO erreichen Leerlaufspannungen von 700 mV und Kurzschlusstromdichten von über 40 $\mathrm{mA/cm^2}$. Die Effzienz ist mit 10 % jedoch sehr niedrig, da der Füllfaktor lediglich Werte von etwa 30 % erreicht – als Folge von stark S-förmigen UI-Kennlinien, potentiell verursacht durch einen unzureichenden Emitter/TCO-Tunnelkontakt oder eine zu dicke intrinsische a-Si:H-Passivierschicht. Mit einem verbesserten Aligniersystem sowie den für die photolithographiebasierten Solarzellen optimierten PECVD-Prozessen konnte die Effizienz auf 17 % erhöht werden, die Füllfaktorenwerte gar verdoppelt (66 %). Die Effizienz dieser Zellen ist maßgeblich durch die niedrige Leerlaufspannung (616 mV) limitiert, als Folge der Degradation der Emitter-Passivierung während des Metallisierungsprozesses.

Im sechsten Kapitel werden Methoden der industriellen Fertigung von IBC-SHJ-Solarzellen sowie ihre daraus potentiell resultierende Marktfähigkeit diskutiert. Um in der Klasse der Solarzellentechnologien mit einem Effizienzpotential größer als 25 % vor allem gegen beidseitig kontaktierte SHJ-Solarzellen bestehen zu können, müssen drastisch vereinfachte Herstellungsverfahren für IBC-SHJ-Solarzellen entwickeln werden. Diesbezüglich zeigen Verfahren basierend auf Schattenmasken, den aktuellen Forschungsstand betrachtend, das größte Potential, sowohl was die Prozesskomplexität als auch bereits erreichte Effizienzen (bis zu 24 %) betrifft. Mittels einer Simulationsstudie wird des Weiteren gezeigt, dass die für die Applikation eines Schattenmaskenprozesses notwendigen Anpassungen der Kontaktgeometrie (insbesondere breitere Kontaktfinger und Metallisierungsabstände) zu lediglich marginalen Effizienzverlusten führen.

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Chapter 1

Introduction

The exploitation of earth's fossil resources in the last two centuries allowed the countries in the Western hemisphere to experience an enormous economical and industrial growth [1]. In the 21st century the emerging economies of Asia and Africa are set to follow the same route, with population numbers exceeding the Western example by far. Thus, despite dwindling fossil resources, mankind's increasing demand for energy is not expected to stabilise anytime soon [2]. The fossil fuel based industrialisation has also led to alarming levels of air pollution, destruction of nature, political tensions and to a rapid increase of Earth's average temperature [3–6].

Photovoltaic (PV) technologies are one of the main alternatives to fossil energy, as they use a reliable source of energy, the sun's irradiation, without negatively impacting the environment by CO_2 and other emissions.

Since the first solar cells were built in the 1950s [7], the cumulative installed solar power has steadily increased, with silicon solar cells being the major contributor [8]. At the end of 2016, 320 GWp of PV capacity were installed worldwide, with an increase of roughly 77 GWp compared to 2015, from which 93 % relied on solar cells based on crystalline silicon [9].

The semiconductor silicon is a well-understood material, owing to its longtime use in various industries, in particular the transistor and microchip industry, its abundance and its non-toxicity. The power conversion efficiency of silicon-based solar cells has seen consistent improvements throughout the last decades, culminating in Kaneka corporation's recent achievement of a solar cell with an efficiency of 26.7 % [10]. This result is very close to the practical limit of 29.4 % as calculated for a silicon-based single-junction solar cell [11, 12]. The theoretical maximum for such a device amounts to 32 %, known as the Shockley-Queisser limit [13].

While in general, silicon solar cells are comparatively simple devices, achieving an efficiency of 20 % and higher requires advanced technologies. These technologies

mainly revolve around increasing light absorption, by introducing textured surfaces and anti-reflection coatings [14, 15], suppressing the recombination of photogenerated charge carriers, by improving passivation and eliminating material defects [16], and improving charge carrier transport properties, by choosing more conductive materials.

The classic concept for a silicon-based solar cell, featuring a diffused junction (homojunction), inherently lacks passivation. With the addition of dedicated passivation layers between the highly doped emitter and BSF regions in the silicon material and the metallisation, an increase in open circuit voltage (V_{OC}) of up to 725 mV is possible [17–19], still falling roughly 35 mV short of the theoretical maximum for silicon [20]. The highest efficiency with diffused junctions was published by the Fraunhofer Institute for Solar Energy Systems in 2017, achieving 25.7 % [19]. This also marks the highest efficiency for a two-side contacted silicon-based solar cell.

The heterojunction concept, pioneered by Sanyo in the early 1990s, represents an alternative to the aforementioned homojunction concept [21]. The emitter layer, responsible for collecting the photogenerated minority carriers, is formed by adding a layer of hydrogenated amorphous silicon (a-Si:H) on-top of the crystalline silicon wafer, with the former being doped contrary to the latter. If an intrinsic, hydrogenated amorphous silicon buffer layer between the crystalline wafer and the amorphous emitter is used, outstanding passivation quality and thus V_{OC} values up to 750 mV are feasible [22].

In order to maximise the light absorption of a solar cell, any losses at the side facing the sun (the cell's front side) should be avoided. In two-side contacted solar cells, the front metal grid inflicts optical losses, as it usually consists of non-transparent materials shadowing part of the front side and thus preventing a significant portion of the incoming light from passing through to the crystalline silicon absorber. These losses are further exacerbated by the underlying emitter, which accounts for further losses due to recombination: in a diffused junction charge carriers created by high-energetic photons are more likely to recombine in the highly doped emitter regions [23]; in a heterojunction the charge carriers generated in the defect-rich a-Si:H emitter rather recombine than contribute to the external current [24].

Both these effects can be avoided, if a back contact (BC) architecture is considered. With both contacts moved to the rear side of the device, the front side can be fully optimised considering only optical and passivating properties, increasing the photogenerated current, usually expressed as the short circuit current density j_{SC}.

For a long time the company Sunpower has been the most prominent advocate for the BC architecture, commercialising back contacted solar cells with passivated contacts, and achieving cell efficiencies of up to 25 % [25, 26]. The heterojunction concept and the back contact approach were first combined by Lu in 2007 [27], and since 2014, with

Panasonic achieving an efficiency of 25.6 % [28], the connection of these two technologies has held the world record for the most efficient single-junction silicon based solar cell. Panasonic's result was surpassed by the aforementioned Japanese company Kaneka in early 2017, by achieving 26.3 % at first and only months later exceeding their own record with 26.6 then 26.7 % [10, 29, 30].

The drawback of any back-contacted architecture is the increase in manufacturing complexity. Having both contacts on the same side of the device necessitates methods to structure the corresponding contact regions. In case of a homojunction approach this means to locally diffuse the p and n^+ regions into the wafer material, while for the heterojunction concept, the additional doped layers need to be structured either after or during their deposition, without harming their properties or those of affected surfaces. Furthermore, practical considerations about the contact geometry must be made. This includes determining the rear side area fraction allocated to one or the other contact, and the area fraction sacrificed for gaps, necessary to separate the contacts. Processing and contact design are not two problems to be solved independently, but are closely interconnected. Oftentimes the structuring method of choice limits the minimum or maximum feature size of certain aspects of the rear side geometry.

This Thesis

The work presented in the following illustrates a solar cell optimisation process through the example of silicon wafer based back-contacted heterojunction (BC SHJ) solar cells. The overall aim is to increase the cell efficiency by optimising the back contact geometry of these cells with respect to their passivation quality, contact resistivity, the consequential total series resistance and their optical properties. In addition to that an industrially viable manufacturing process is proposed and analysed with respect to its inherent limitations.

Chapter 2 describes the basic properties of the used materials and the principles of solar cell operation.
In Chapter 3 the technological background with regards to structuring and deposition techniques, the different characterisation methods and the simulation software Sentaurus is introduced and validated. Moreover, the two-dimensional model of an BC SHJ solar cell is outlined. The model serves as a basis for the simulation of BC SHJ solar cells with direct aluminium/a-Si:H contacts and for a simulation study exploring the impact of the rear side contact geometry.
Chapter 4 describes the manufacturing processes of BC SHJ solar cells. At first, the established photolithography process is explained as well as the improvements

introduced during the course of this work. Additionally the development of an alternative, industrially viable process based on shadow masks is outlined.

In Chapter 5 the results of solar cells featuring different contact materials and manufacturing processes are presented and analysed. This incorporates photolithography based BC SHJ solar cells with direct aluminium/a-Si:H contacts or contacts based on transparent conductive oxides (TCO) as well as solar cells built with the shadow mask process.

Chapter 6 discusses the prospects of BC SHJ solar cells, by comparing the technology to other high-efficiency solar cell concepts with respect to potential mass production and marketability. Existing industrially viable approaches to manufacture BC SHJ solar cells are briefly outlined, additionally the impact of wider contact geometries, inherent to these industry-compatible processes, are evaluated by simulation.

The key results of this work can be summarised as follows:

- Annealed direct aluminium/a-Si:H represent a simple and effective option for high-efficiency BC SHJ solar cells, as they exhibit low contact resistivities and thus high fill factor (FF) values. Annealing times and temperatures are critical as extended annealing leads to strong interdiffusion of aluminium and amorphous silicon resulting in the disintegration of the amorphous silicon layers and the destruction of the passivation. With moderate annealing the passivation remains unharmed while the contact resistivity improves drastically, likely owing to the formation of a thin aluminium silicide layer.

- The efficiency of BC SHJ solar cells with indium tin oxide (ITO) contacts was improved by 4 %abs (from 19.2 to 23.2 %), by optimising the photolithography process, implementing a new front side layer stack and using optimised rear side a-Si:H layers. Additionally alternative TCO materials were evaluated: particularly transparent aluminium-doped zinc oxide (AZO) reduces the parasitic absorption at the rear side and thus increases the j_{SC} of the respective solar cells, but on the expense of the FF; the FF and the contact resistivity of initial solar cells with a tungsten oxide interlayer between the a-Si:H emitter and the ITO layer are on a par or slightly better than the ones of conventional ITO based solar cells, but parasitic absorption in the WO_X layer reduces the j_{SC}. Using textured instead of polished rear sides enhances the optical response of the rear side and improves the solar cell's j_{SC}. It also increases the effective cell area, leading to a moderate increase of the FF.

- Initial solar cells built with the shadow mask process achieve efficiency values up to 17 %, illustrating the general viability of the process. PECVD deposited a-Si:H layers patterned in-situ with shadow masks exhibit tapering and underdeposition effects impairing the fidelity of the patterned layers. The extent of these effects depends on the properties of the respective a-Si:H deposition process. If the latter is limited by the diffusion of SiH_3 radicals to the substrate's surface, the fidelity of the deposited layers is high. As a consequence of the tapering effects, solar cells built with the shadow mask process have to feature wider BSF and emitter widths as well as metallisation gaps. The impact of the wider contact geometry is evaluated with a simulation study: despite the larger contact geometry corresponding losses are small compared to the losses related to the p-contact resistivity.

Chapter 2

Fundamentals

In this chapter the properties of the relevant materials and the operating principle of solar cells in general are described.

2.1 Materials and Interfaces

2.1.1 Crystalline Silicon

In this section, the properties of crystalline silicon are briefly explained, as it represents the core material of the solar cells discussed in this work. For a more in-depth discourse, the reader is referred to [31] and [32].

The positive nucleus of a silicon atom is surrounded by its 14 electrons, each occupying a distinct energy level. The silicon atoms are arranged in a diamond type cubic crystal structure that is repeated alongside the entire silicon bulk (crystalline silicon, c-Si). Since the positive nuclei of the atoms are no longer isolated, but positioned in a periodic lattice, the energy levels of the corresponding electrons overlap and form quasi-continuous energy bands. In silicon, such as in every other inorganic semiconductor, an energy gap exists between the highest occupied energy band - valence band E_V - and the lowest unoccupied energy band - conduction band E_C. In silicon, this *band gap* E_G amounts to a value of 1.12 eV, being the minimum energy that has to be transferred to an electron in the valence band to be excited to the conduction band. A photon therefore can be absorbed by a silicon crystal, if its energy is larger than the aforementioned band gap. However, since silicon is an indirect semiconductor, meaning in the momentum space, or k-space (see Figure 2.1), its valence band maximum and conduction band minimum are not at the same position, an additional amount of momentum is needed to absorb a photon with the minimal energy of 1.12 eV at room temperature (a direct transfer would be possible at an energy of 3.4 eV). This necessary momentum transfer

reduces the probability of absorption and thus lowers silicon's absorption coefficient. As a consequence, comparatively thick layers of crystalline silicon (in the range of 100 to 300 µm) are needed to provide sufficient absorption for solar cell applications.

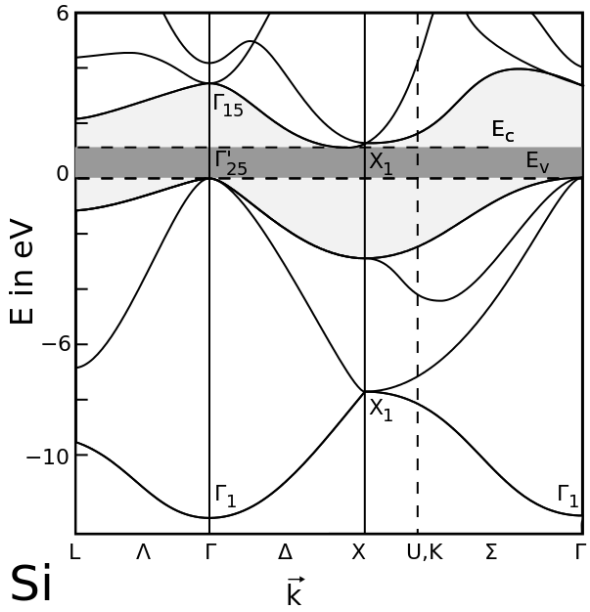


Figure 2.1: Silicon band structure in k-space, reworked by [33], after [34].

The absorbed photon creates a Wannier-Mott exciton, a weakly bound electron-hole pair. With binding energies in the order of 0.01 eV [35], the exciton is effectively immediately split up, creating an unbound electron in the conduction band and an equivalent hole in the valence band, both able to contribute to charge transfer. Collecting and transferring these photogenerated, free charge carriers to an external circuit is the purpose of a solar cell device.

Doping

In a silicon crystal, each silicon atom forms four covalent bonds. It is possible to replace a certain amount of silicon atoms with foreign atoms, whose outer shell contains either less (acceptor material) or more (donor material) electrons. If an element with five outer shell electrons is brought into the silicon crystal lattice, all four silicon bonds will be saturated, leaving one of the donor's bonds open. If the energy level of the donor's outer shell electrons is close to silicon's conduction band, the donor atom is usually ionised at room temperature, releasing its excess electron into the conduction band of the silicon crystal, where it is available for charge transport. This process is called n-doping. Typical elements for n-doping are phosphorus and arsenic.

The reverse process, p-doping, involves an element with three outer shell electrons, whose energy level is close to valence band of silicon. The acceptor atom attracts an

electron from the valence band of silicon, leaving a hole behind. Typical p-doping materials are boron and aluminium.

Doping concentrations are usually in the order of 10^{15} to 10^{16} atoms per cm^3, with silicon's intrinsic electron and hole densities each being $10^{10}\,cm^{-3}$ at room temperature. In doped semiconductors one then differentiates between majority and minority charge carriers.

Recombination

If the silicon crystal is not contacted by an external circuit, meaning that the extraction of the photogenerated charge carriers is not possible, they will eventually recombine. In silicon, three main types of recombination can be identified (see Figure 2.2):

Shockley-Read-Hall (SRH) recombination describes the recombination across a defect energetically positioned in the band gap. In the bulk, these defects are caused by impurities or crystal dislocations. At the surface of the silicon crystal, open silicon bonds act as very effective mid-gap recombination centres. The transferred energy is then transformed into lattice vibrations [36, 37].

Auger recombination describes a recombination process that involves three charge carriers: an electron in the conduction band might transfer its energy to another conduction band electron and then recombine with a hole in the valence band. The energy receiving electron is excited to higher energetic position within the conduction band, from which it thermalises back to the conduction band edge. Its energy is lost as heat.

Radiative recombination describes the inverse process to absorption. An electron in the conduction band recombines with a hole in the valence band and emits a photon with an energy corresponding to the band gap of the semiconductor (1.12 eV for silicon). Due to silicon being an indirect semiconductor, radiative recombination is usually not the dominating recombination process.

At low injection levels, meaning that the equilibrium majority charge carriers outnumber the light generated excess carriers, SRH recombination dominates. At high injection, where the excess carriers outnumber the equilibrium majority charge carriers, Auger recombination is predominant.

Each recombination method is attributed with a corresponding recombination rate expressed by an inverse time constant $\frac{1}{\tau_i}$. The reciprocal sum of all recombination time

constants constitutes the inverse of the effective lifetime τ_{eff}, an important parameter to quantify the passivation quality:

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{rad}}} + \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{SRH}}} + \frac{1}{\tau_{\text{Surface}}}. \tag{2.1}$$

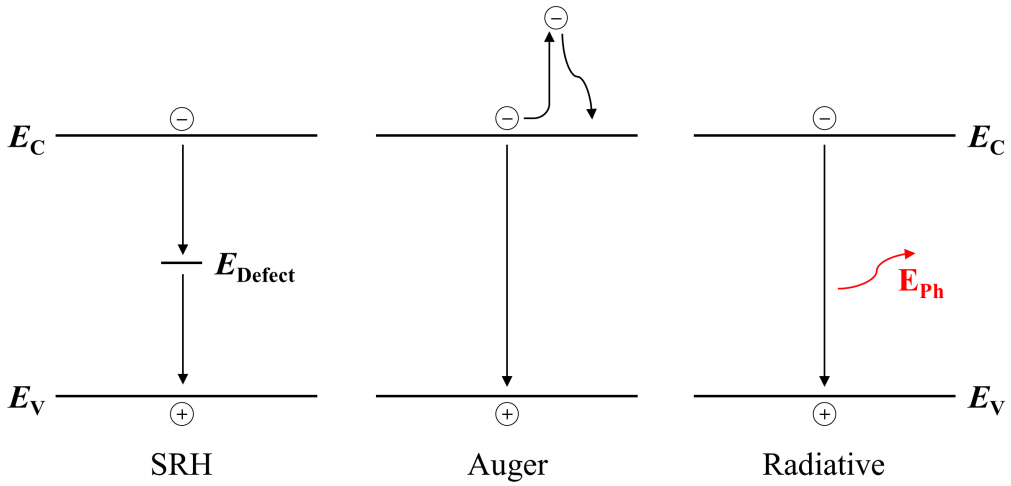


Figure 2.2: Modes of recombination in silicon.

2.1.2 Amorphous Silicon

In amorphous silicon (a-Si), the silicon atoms are not bound in a well-ordered crystal lattice, but arranged in sp^3-hybrid orbitals with the corresponding close range order. In the absence of a long range order, a large number of nanosized voids and unsaturated silicon, so-called dangling bonds lead to a high defect density in the material bulk (see Figure 2.3) [38, 39]. These defects can be passivated by introducing hydrogen into the material (a-Si:H), which fills the nanovoids, saturates open silicon bonds and breaks weak silicon-silicon bonds to replace them with more stable silicon-hydrogen bonds [40–42]. The fundamental differences between amorphous and crystalline silicon with respect to their morphology and composition have a notable impact on their physical properties [43]. Its band gap is greater, with values ranging from 1.5 to 1.9 eV, depending on the hydrogen concentration in the material [44]. It is possible to dope amorphous silicon with the same elements that are used for crystalline silicon, namely phosphorus and boron [45]. However, the doping efficiency is low, because the amorphous network will rather fully integrate the dopant atoms, than allowing them to ionise and contribute a free electron or hole to the conduction or valence band, respectively. Consequently, at similar doping densities, the conductivity of amorphous silicon is orders of magnitude lower than the one of its crystalline counterpart [46].

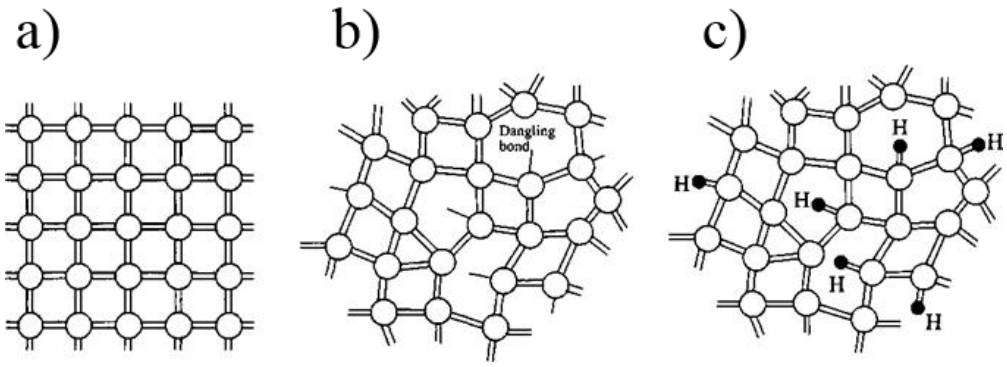


Figure 2.3: a) Crystalline silicon b) Amorphous silicon with dangling bonds c) Hydrogenated amorphous silicon [47].

2.1.3 Heterojunction Interfaces

If two semiconductors featuring different band gaps are brought in contact, a heterojunction interface is formed. In equilibrium conditions, the band structures of both materials align with respect to a constant, common Fermi level. Figure 2.4 exemplifies a heterojunction interface between a crystalline and an amorphous silicon layer. Band bending and band offsets depend on the doping levels of the two materials and the amount and charge of interfacial surface states. The conduction band offset for an a-Si:H/c-Si heterojunction was determined to be around 200 meV [48]. Corresponding valence band offsets range between 200 and 450 mV, again depending on the doping of both the a-Si:H and c-Si layer [44, 49].

2.1.4 Contact Materials

In the context of this work, the materials that facilitate the extraction of charge carriers from the silicon layers (in this case the doped amorphous or nanocrystalline silicon layers) are denoted as contact materials. These are typically materials with high conductivities, such as metals or materials with metallic properties, e.g. degenerate semiconductors. According to the simple Schottky model, metals and semiconductors form Schottky contacts characterised by the band alignment that arises from the difference between the metal's work function and the semiconductor's electron affinity, resulting in the formation of an accumulation, neutral (flat band), depletion or inversion interface [50]. Ohmic contacts, as desired for solar cells, are ideally free from any barriers, which corresponds to the accumulation case. In reality metal-semiconductor contacts do not obey the simple Schottky model, as acceptor (or donor) surface states capture the metal's excess electrons (or holes) and thus barely affect the Fermi level within the semiconductor. Consequently the barrier height is hardly related to the metal's

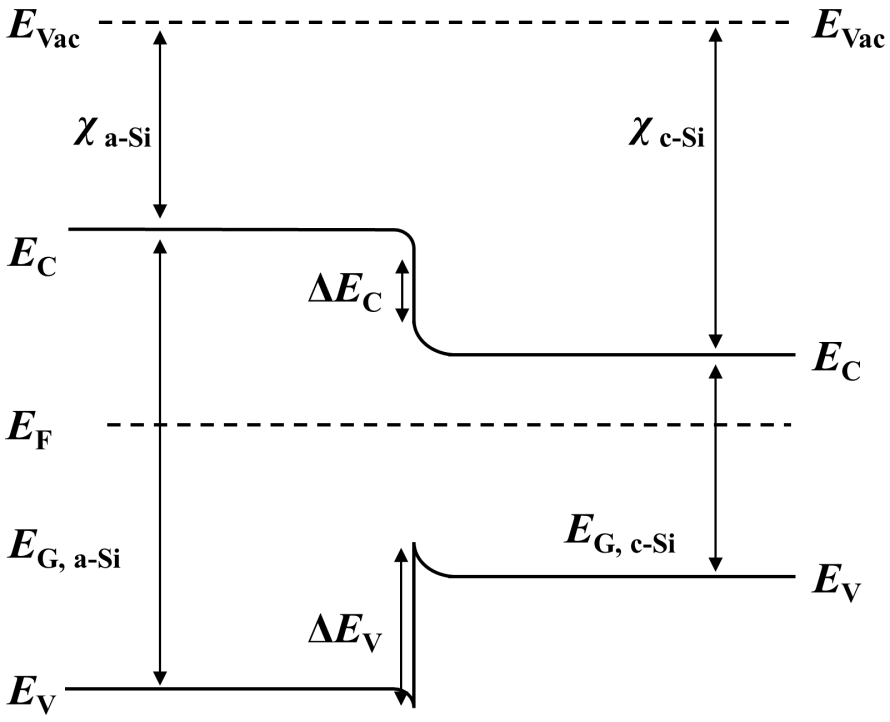


Figure 2.4: Not drawn to scale band lineup of an amorphous/crystalline silicon interface, with the vacuum level E_{Vac}, the conduction band E_{C}, the valence E_{V}, the electron affinities $\chi_{\mathrm{c-Si}}$ and $\chi_{\mathrm{a-Si}}$, the band offsets ΔE_{C} and ΔE_{V} and the corresponding band gaps denoted.

work function, but to the amount of surface states pinning the Fermi level. Metal-semiconductor contacts exhibiting ohmic behaviour are therefore achieved by using highly doped semiconductors. In these cases, the space charge region at the interface becomes narrow enough to allow sufficient tunnelling through the barrier as a current transport mechanism [51].

In this work, the following materials were used to contact highly doped p- and n-type a-Si:H layers:

Indium tin oxide (ITO) belongs to the group of transparent conductive oxides (TCO). It is an n-type degenerate semiconductor featuring a wide band gap of around 4 eV. Being transparent in the visible range of the solar spectrum, infrared light can be absorbed due to free carrier absorption, a process that depends heavily on the amount of charge carriers being present in the conduction band [24, 52]. Its Fermi level is positioned in the conduction band, hence it exhibits metallic properties. Its work function is usually in the range of 4.4 to 4.8 eV [53].

Aluminium-doped zinc oxide (AZO) is a TCO material that exhibits similar properties to ITO. Its conductivity and thus also transparency depends heavily on the

amount of aluminium in the material. Given similar conductivity values to ITO, it is usually more transparent, but features lower work function values. [54, 55].

Tungsten oxide (WO_X) is an n-type semiconductor belonging to the group of transition metal oxides [56]. Depending on the oxygen concentration, WO_X features a high band gap, and more importantly a high work function above 5.5 eV, making it a promising candidate to form a carrier-selective recombination contact with p-type amorphous silicon [57].

Silver and **aluminium** are both metal materials exhibiting high – in case of silver the highest among all metals – values of electrical and thermal conductivity, as well as reflectivity. The work function of silver ranges between 4.3 and 4.7 eV while the one for aluminium is slightly lower with approximately 4.1 eV.

2.2 Solar Cells

A solar cell is a device that converts the energy of absorbed photons into electrical charge carriers, that can be driven through an external electric load. Various types of solar cells exist, based on different classes of materials [10]. This chapter solely focuses on solar cells based on crystalline silicon.

2.2.1 Basic structure

A basic silicon solar cell consists of an either p- or n-doped silicon absorber layer with a thickness typically in the order of 100 to 300 µm, a much thinner emitter layer of the opposite polarity and contact layers, extracting the photogenerated charge carriers [7,58]. Between the absorber and the emitter layer, a pn-junction is formed. Light enters the solar cell through the side that is not fully metallised and is absorbed in the silicon bulk, generating electron-hole pairs. The generated minority charge carriers then diffuse towards the pn-junction where they are swept across the space charge region by the junction's internal electrical field and subsequently extracted through the metal contact. An equivalent amount of majority charge carriers is simultaneously extracted at the n-contact resulting in a net current flow, that can be driven through an external electric load. It is apparent that in an efficient solar cell the recombination of generated minority carriers should be prevented, as otherwise they are not able to contribute to the external current. In the very simple solar cell, shown in Figure 2.5, both the p- and the n-contact are formed by directly contacting a metal with the silicon emitter and the absorber, respectively. This results in poorly passivated surfaces acting as highly

recombination-active zones, thus limiting the open circuit voltage of these cells to values of around 650 mV [23, 59].

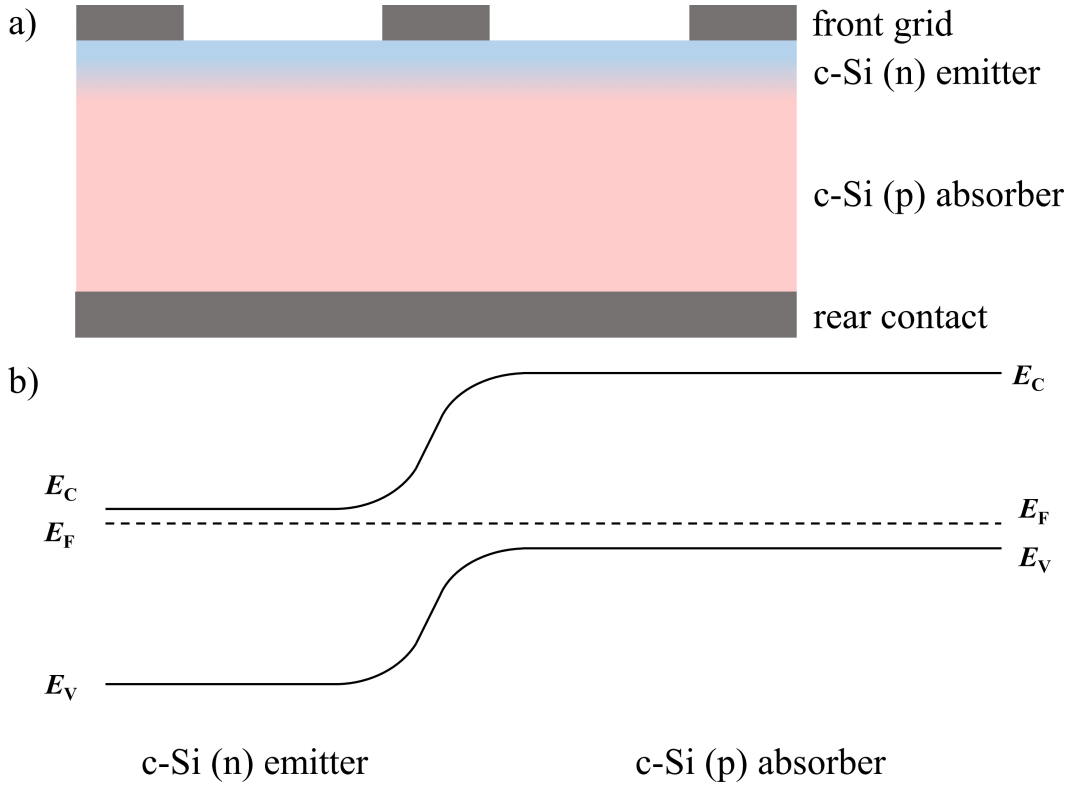


Figure 2.5: a) Not drawn to scale structure of a simple silicon solar cell, based on a crystalline p-type absorber, a diffused n-type emitter, and a direct metallisation. b) Band diagram of the simple silicon solar cell (without metallisation, not drawn to scale)

2.2.2 Heterojunction Solar Cells

In a heterojunction solar cell the usually n-doped c-Si absorber is passivated on each side by an intrinsic a-Si:H layer, saturating open silicon bonds at the surface of the silicon crystal [16]. The chemical passivation of the absorber's surfaces reduces the recombination within the bulk to a minimum resulting in high minority carrier lifetimes [60]. The addition of an n-doped a-Si:H layer at the n-contact further increases the passivation quality by adding a field-effect, meaning the accumulation of majority and the depletion of minority charge carriers at this interface (back surface field, BSF contact). On the other side a p-doped a-Si:H layer on-top of the intrinsic passivation layer induces a thin inversion layer in the c-Si absorber thus forming the pn-junction needed for efficient charge carrier extraction [61, 62]. The band offsets mentioned in subsection 2.1.3 and the band bending induced by the doped layers on either side of the wafer result in the formation of energetic barriers. The large energy barrier in

the valence band at the n-contact repels holes, while the energy barrier and the band bending in the conduction band at the p-contact repel electrons. The width of the otherwise counterproductive energetic barriers alongside the extraction direction of either charge carrier (conduction band at the n-contact, valence band at the p-contact) is decreased by the band bending so that the corresponding charge carriers can overcome these barriers either by tunnelling, hopping transport or thermionic emission [46, 63–65].

In a front-emitter, mono-facial silicon heterojunction (SHJ) solar cell, light enters the cell through the emitter side, which is therefore contacted with a metal grid. The n-contact metallisation acts as a rear reflector and is thus fully metallised. On both sides a TCO layer is placed in-between the a-Si:H layers and silver electrodes. The TCO layer on the n-side enhances the optical response of the rear reflector by suppressing plasmonic absorption at an otherwise direct silver-silicon interface [52, 66]. At the p-side, the TCO provides the lateral conductivity necessary to allow the minority charge carriers to reach the metal grid fingers, as the p-type a-Si:H layer lacks conductivity. The front TCO also needs to be as transparent as possible to avoid parasitic absorption. Since high conductivity and high transparency are contradicting requirements, the front TCO design always involves a trade-off between these two properties. The situation is further exacerbated as the front-TCO also functions as an anti-reflection layer, thus the layer thickness has a rather small interval (70 to 80 nm in case of ITO) [24].

Figure 2.6 visualises the layer stack and the corresponding band diagram.

2.2.3 Interdigitated Back Contact Solar Cells

In a back contacted solar cell, both the emitter and the absorber are contacted at the device's rear side, i.e. the side facing away from the illumination. This allows to optimise the front side solely with respect to its optical and passivating properties, which is especially beneficial for SHJ solar cells since the non-ideal, multipurpose front-TCO is omitted [27, 67, 68]. The absence of a metal grid – inflicting shadowing losses, and emitter or BSF layers – parasitically absorbing part of the incoming light, at the front side leads to an increase in light absorption in the c-Si absorber material.

The two contacts at the rear side of back contacted cells are usually patterned as interdigitated finger structures, with busbars collecting the respective charge carriers at opposite sides of the cell [69]. The interdigitated approach also allows to describe the basic contact geometry with a small set of parameters, namely the pitch as the sum of the widths of both contacts, the emitter coverage as the percentage of the rear-side area that is covered by the emitter contact and the total cell area (in this approach, potential gaps between the contacts and the metallisation coverage of the contact areas are neglected, however these are usually small compared to the overall dimensions

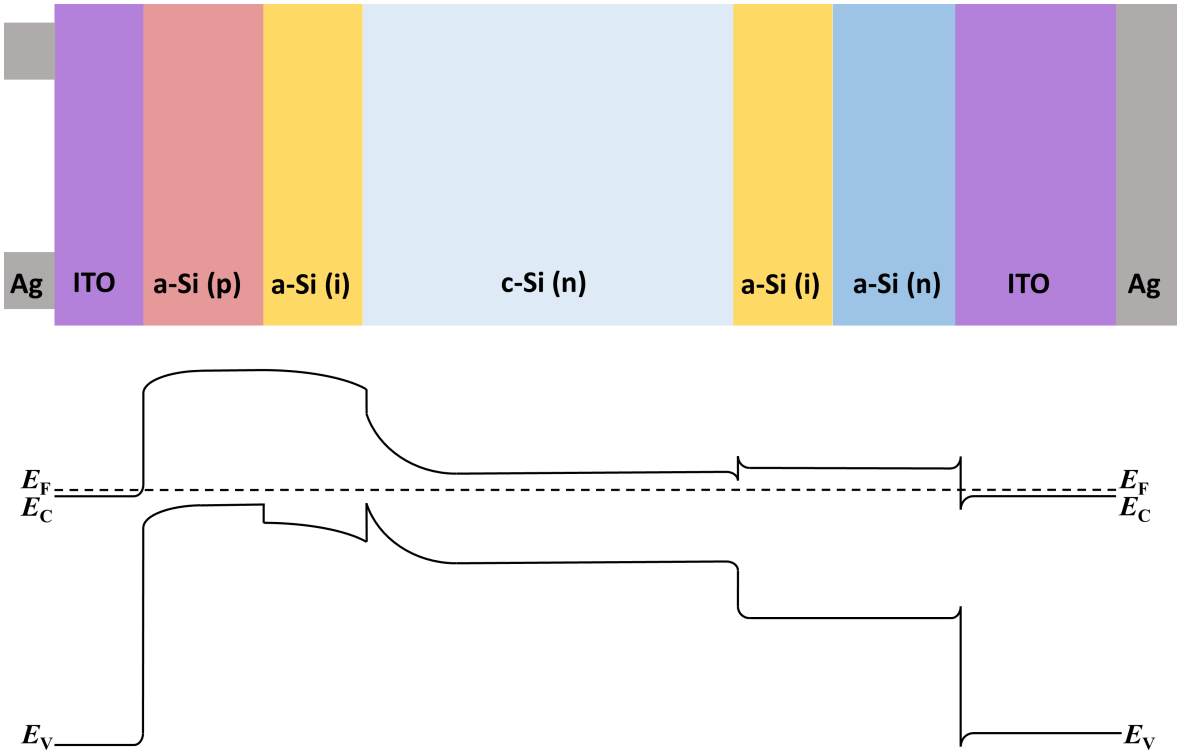


Figure 2.6: Not drawn to scale structure and band diagram of a front-emitter, monofacial silicon heterojunction solar cell. The n-type c-Si absorber is passivated by intrinsic a-Si:H layers. Emitter and BSF contact are formed by p- and n-doped a-Si:H layers, the metallisation in this case consists of an ITO/Ag stack on both sides. In the band diagram the conduction band E_C, the valence band E_V and Fermi level E_F are denoted.

of the finger structures) [70]. Figure 2.7 a shows the schematic of an interdigitated back-contact silicon heterojunction solar cell, Figure 2.7 b illustrates the interdigitated structure and the key parameters.

Point contacts are an alternative option to the interdigitated pattern. However the metallisation is usually more complicated, as the point contacted areas are fully surrounded by the contact area of the other polarity. Hence additional layers have to be added, one to connect the different point contacts and one to isolate this connection layer from the contact area of opposing polarity [71, 72].

2.2.4 Basic Parameters and Equivalent Circuit

Containing a pn-junction, a solar cell is a particular type of diode. In a simple equivalent circuit, shown in Figure 2.8, this diode is accompanied by an ideal current source, representing the photogenerated current j_{Ph} and the series and the parallel resistances R_S and R_P, representing the ohmic losses within the device. The following

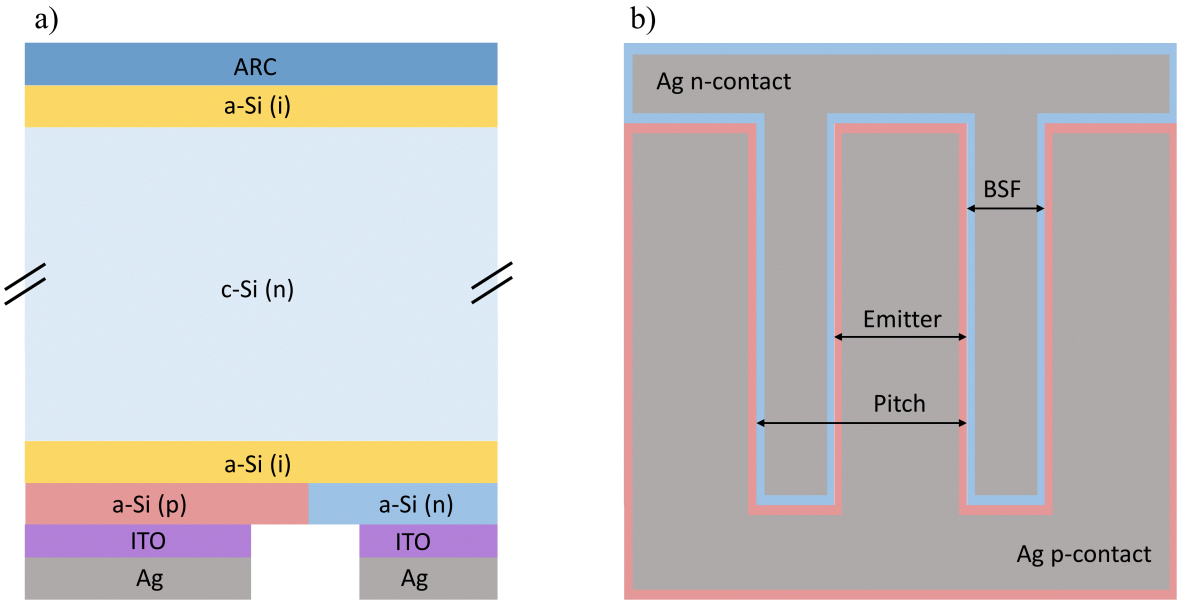


Figure 2.7: a) Not drawn to scale layer stack of an interdigitated silicon heterojunction solar cell. The c-Si (n) absorber is still passivated by intrinsic a-Si:H on both sides. The doped a-Si:H layers, forming the emitter and BSF contacts, are placed at the rear side of the device. The metallisation still consists of an ITO/Ag stack for both contacts. b) Rear side view with interdigitated structure: the pitch equals the sum of the emitter and the BSF width – both contacts are almost fully metallised, leaving a small metallisation gap in-between them.

equation describes the current-density–voltage relation of the equivalent circuit in Figure 2.8 [73]:

$$j(V) = j_0 \left(\exp\left(\frac{q(V - jR_\mathrm{S})}{mkT}\right) - 1 \right) + \frac{V - jR_\mathrm{S}}{R_\mathrm{P}} - j_\mathrm{Ph} \tag{2.2}$$

Here k represents the Boltzmann constant, T the temperature, q the elementary charge, V the external voltage, m the ideality factor, j_Ph the external photocurrent, and j_0 the reverse bias saturation current. The latter represents the cumulative recombination within the device in equilibrium conditions and is therefore linked to the diode's or rather solar cell's material quality. The ideality factor m accounts for deviations from the ideal diode equation ($m = 1$), that only considers recombination mechanisms proportional to the charge carrier density product. In reality the recombination in a solar cell is governed by multiple mechanisms that do not necessarily obey this relation, for instance recombination mechanism predominantly occurring at higher injection levels (Auger, SRH recombination incorporating majority carriers). Hence, both j_0 and m need to be adjusted accordingly.

The magnitude of the series resistance R_S depends on the resistance of the different materials conducting the current and the contact resistivity of the respective interfaces. It is thus influenced by the doping level of the bulk, emitter and BSF layers as well as the conductivity of the TCO and metallisation layers. R_P represents current paths bypassing the pn-junctions in the form of shunts between the two contacts. Typical current-density–voltage (jV) characteristics of a solar cell with different values for R_S and R_P are shown in Figure 2.9.

From the jV curve it is possible to extract the solar cell's characteristic parameters:

The **open circuit voltage** (V_{OC}), at which the internal recombination currents within the solar cell exactly compensate the photogenerated current, resulting in zero external current. The maximum possible V_{OC} for a silicon solar cell was calculated to be 761 mV, assuming a practically perfect diode (very low j_0, $m = 2/3$) and taking only Auger recombination as an intrinsic recombination mechanism into account [12].

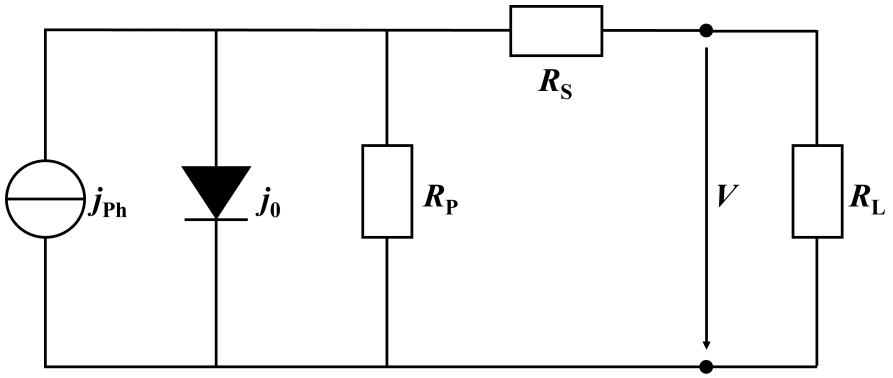


Figure 2.8: Equivalent circuit of a solar cell, consisting of a diode representing the pn-junction, an ideal current source for the photogenerated current and the resistances R_P and R_S, representing ohmic losses.

The **short circuit current density** (j_{SC}) describes the current density measured at $V = 0$, at which practically all photogenerated charge carriers recombine over the external shunt. Since the recombination current within the diode at $V = 0$ is usually negligible, the j_{SC} is basically equal to j_{Ph} and therefore a good figure of merit for the absorption capabilities of the solar cell. Taking into account silicon's band gap of 1.12 eV and assuming an AM1.5G irradiation, the theoretical maximum j_{SC} is 46 mA/cm^2, with the practical limit being 43.3 mA/cm^2 [12, 13].

The **maximum power point** (MPP) voltage V_{mpp} and current density j_{mpp} are the voltage or current density values at which the product of V and j maximises. The product of V_{mpp} and j_{mpp} divided by the power input P_{in} (100 mW/cm^2 under AM1.5G conditions) yields the solar cell's **efficiency** η. Although the MPP-values ultimately

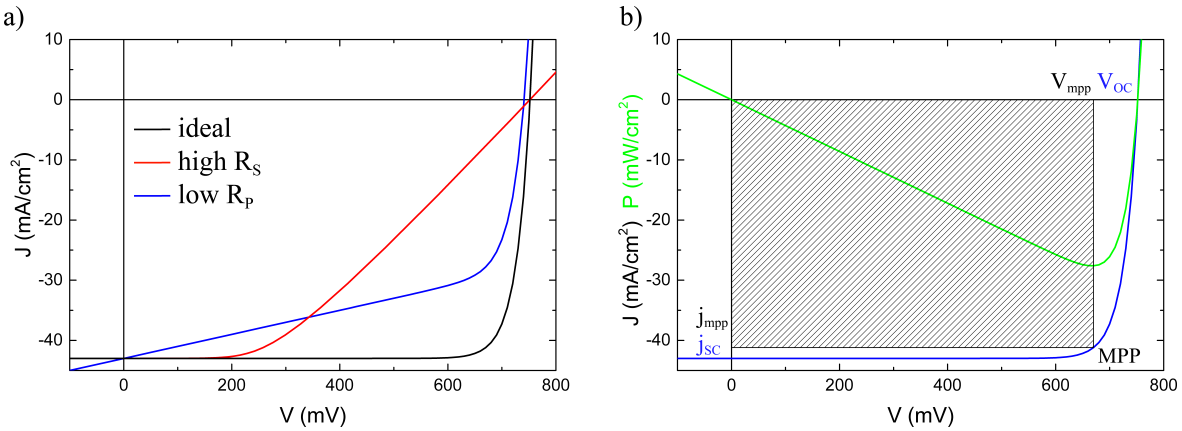


Figure 2.9: a) Influence of high R_S and low R_P values on an otherwise typical jV curve. b) Visualisation of the characteristic parameters of a jV curve, with the power square dashed.

determine the solar cell's efficiency, they are not very well suited for characterisation and comparison of different solar cells or technologies. In real world operation, the MPP will change over time and outer conditions, therefore the attached power inverters track the MPP of the corresponding modules.

To circumvent the use of MPP-values, the **fill factor** (FF) is introduced as another figure of merit. It is calculated by dividing the MPP-product by the product of the V_{OC} and the j_{SC}:

$$FF = \frac{V_{mpp} \cdot j_{mpp}}{V_{OC} \cdot j_{SC}} \tag{2.3}$$

As Figure 2.9 shows, the FF is impacted by both the R_P and the R_S, but also high recombination within the device can have a detrimental effect on the FF. To optimise the FF and analyse contributions to FF losses is one of the major challenges when developing efficient solar cells. Richter *et al.* estimate the maximum achievable fill factor for silicon-based solar cell to 89.3 % [12].

Using the aforementioned parameters it is possible to calculate the solar cell's efficiency η as follows:

$$\eta = \frac{V_{mpp} \cdot j_{mpp}}{P_{in}} = \frac{FF \cdot V_{OC} \cdot j_{SC}}{P_{in}} \tag{2.4}$$

The latter expression only contains parameters that can either be backtracked to physical properties of the device (optical properties and resulting absorption in the case of the j_{SC} and semiconductor properties and passivation quality in case of the V_{OC}) or, in case of the FF, are at least comparable among different solar cells and solar cell technologies. With the aforementioned maximum values for each parameters, the maximum achievable efficiency for a silicon-based solar cell amounts to 29.4 % [12].

Chapter 3

Fabrication, Characterisation and Simulation

In this chapter the technological background with respect to deposition and patterning techniques is outlined. Furthermore, the used characterisation methods are briefly explained. At last, the simulation software Sentaurus TCAD is introduced and validated.

3.1 Deposition and Patterning Techniques

For the preparation of interdigitated back contact silicon heterojunction (IBC SHJ) solar cells, it is necessary to deposit and accurately structure thin layers with thicknesses ranging from a few nanometres to a couple of micrometres. In the following, the basics of deposition and patterning techniques relevant for SHJ solar cell manufacturing are described in general. The specific processes that were used to build the solar cells presented in this thesis are discussed extensively in chapter 4.

3.1.1 Deposition

This section focuses on deposition techniques that are typical for the manufacturing of SHJ solar cells.

Plasma-enhanced chemical vapour deposition (PECVD) is a technique to deposit solid thin films. A plasma discharge is created between two conductive electrodes, either by applying direct current (DC) or alternating current (AC), with the latter being the more common. The discharge ionises a significant portion of the precursor gas's atoms or molecules. These radicals are then transported towards the substrate's surface, where they are adsorbed and surface diffuse until they react with the surface's

atoms forming a layer. In case of a-Si:H deposition, the precursor gas is usually silane (SiH_4), with hydrogen (H_2) being added further hydrogenate the layer [74]. Doped layers can be formed by adding the corresponding precursor gases, e.g. phosphine (PH_3) for n-doping or diborane (B_2H_6) for p-doping.
A PECVD process is characterised by multiple parameters. Small changes in precursor composition, gas pressure, plasma power, substrate temperature, electrode distance and deposition time can have a drastic influence on the deposited layer's properties [75–77]. A carefully optimised PECVD process is therefore a major requirement for a functioning heterojunction solar cell manufacturing process.

Sputter Deposition is part of the group of processes subsumed as physical vapour deposition (PVD) processes, in which a material in a condensed phase is transformed into a vapour phase and subsequently into a condensed phase again. In a sputter process, the initial condensed phase exists in the from of a sputter target. Between the substrate, e.g. a silicon wafer, and the sputter target a plasma is ignited containing an ionised inert gas like argon, either by DC or AC voltage. The ions of the inert gas then impact onto the target's surface ejecting atoms from it. Depending on gas pressure and temperature, the ejected ionised atoms either ballistically fly towards the substrate or collide with the inert gas's atoms and diffuse towards the substrate (and its surroundings). Reactive gases can be added to the sputtering gas in order to influence the composition of the sputtered layer [78]. An indium tin oxide (ITO) layer, for instance, can be sputtered from an indium tin target, with oxygen added to the process gas. Depending on the plasma power, a sputter process is likely to inflict physical damage to the substrate's surface. This has to be taken into account especially when TCO layers are sputtered onto thin a-Si:H passivation layers on silicon wafers [79].

Thermal Evaporation is a PVD process, in which a solid material is evaporated in a vacuum chamber. The evaporated material then travels towards the substrate's surface, where it condenses again. In contrast to sputtering, thermal evaporation will not inflict physical damage to the substrate's surface, however high process temperatures as well as the condensation or crystallisation enthalpy might have an annealing effect on the substrate.

3.1.2 Patterning

In order to manufacture back contacted solar cells, the contacted side needs to be patterned in an appropriate way. Many patterning methods with varying degrees of complexity and accuracy exist, usually the latter depends on the former. Patterning

can be done in-situ, combining deposition and patterning in one process, or after the deposition, removing parts of a deposited layer by means of etching. The following sections focus on pattering techniques used to structure layers relevant for the fabrication of SHJ solar cells. These are a-Si:H, TCO and metal films.

Photolithography is a widely used and accurate patterning technique [80]. The layer to be structured is coated with a thin layer of a photoactive resist. Through a mask, the resist is then partly exposed to light and afterwards put into a developer solution. Depending on the type of resist, positive or negative, the parts that were exposed to light are dissolved during the developing or insensitive to the developer solution. In the latter case the unexposed parts of the resist are dissolved. As a result, the structure of the mask (or its negative) is transferred to the resist layer. In a subsequent step, parts not covered by resist are etched, either by using wet chemicals or dry etching methods like reactive ion etching (RIE) [81]. Depending on the masking approach, the mask can be in direct contact with the substrate or projected onto it through a system of lenses, the minimum feature achievable with this method is in the order of a few nanometres (modern computer chips with transistor channel widths in the range of 10 to 20 nm are commercially available [82]). Since for photovoltaic applications the minimal needed dimensions are in the range of a few micrometers, contact masking is sufficient. Owing to the many process steps (usually involving multiple annealing, etching and rinsing steps) photolithography is a lengthy process and thus not regarded as an industrially viable manufacturing method for high volume solar cell fabrication.

Shadow Masking In contrast to photolithography, where the layer is structured after its full-area deposition, the use of shadow masks enables in-situ patterning. To avoid or minimise tapering effects at the structure's edges, the masks should to be as thin as possible. At the same time they have to exhibit a certain amount of mechanical stability. Furthermore, the masks have to withstand the process conditions with regards to elevated temperatures or the presence of a plasma. As the masks will be directly placed onto the substrate, they must not contaminate or alter the surface of the substrate or the conditions in the process chamber. The deposition process itself also has to be compatible with the masking approach. If the film growth on the substrate's surface is governed by surface diffusion processes, which is possible for both PECVD and sputtering processes, undesired deposition under the mask represents a serious issue. If multiple masks in subsequent steps are used, a suitable alignment method is necessary. To maintain the desired simplicity of the process, the masks will be fixed mechanically in most cases, either by clamps or pin holes. This procedure results in several micrometers of alignment inaccuracy.

As a consequence of all these requirements the minimal feature size for a shadow mask based process is more likely to be in the range of hundreds of micrometers.

Laser Ablation The variety of lasers with different characteristics in terms of wavelength, pulse width and power enables many different laser-based patterning techniques. Lasers can be used to directly ablate single a-Si layers from c-Si substrates [83]. However, direct ablation incorporates the risk of damaging the underlying silicon surface so that its repassivation with intrinsic a-Si:H is either more difficult, insufficient or impossible. In most cases, laser ablation is used to structure protective or sacrificial layers that then function as masking layers for subsequent etching processes [84–86].
In theory laser ablation related patterning techniques are less complex compared to a photolithography process. Their industrial viability mostly depends on the complexity of the non-laser process steps, such as the deposition of multiple, potentially intricate sacrificial layers or etching steps still involving wet chemicals.

Screen Printing is a method primarily used to deposit in-situ structured metal layers. A metal paste, usually based on silver or aluminium particles, is pressed onto the substrate through a screen. The screens are made of a fine synthetic mesh, in which the application of a blocking stencil, being impenetrable for the paste, defines the desired structure. A squeegee then presses the paste through the penetrable parts of the screen transferring it onto the substrate. The minimum feature size, in the range of tens of micrometers, is limited by the expansion of the paste during the annealing after printing [87, 88].
Screen printing can also be used to apply etch resists, thus replacing the light exposure and resist developing part of the photolithography process.

3.2 Characterisation

The knowledge of the silicon-specific physical limitations allows to determine the solar cell technology's efficiency potential. Loss mechanisms hindering the exploitation of this potential can be identified by various characterisation methods.

In the following, the different methods used to characterise the solar cells presented in this work are briefly described.

3.2.1 jV measurements

To determine the solar cell's efficiency by measuring its light jV curve, a solar simulator is used. The class AAA Wacom WXS-156S-L2 simulates the terrestrial solar spectrum

using both a tungsten and a xenon lamp [89]. During the measurements, the solar cells are mounted in a water-cooled (maintaining a temperature of 25 °C), custom measuring chuck, masking everything but the cell area. Dark jV curves were measured using the same setup with the entire wafer covered.

3.2.2 TrPCD

The transient photoconductance decay method (TrPCD) is used to determine the effective minority charge carrier lifetime τ_{eff} of a passivated, non-metallised silicon wafer. A flash unit emitting mostly infrared photons generates a certain amount of excess carriers within the device thus leading to an increased conductivity within the wafer, which decays shortly afterwards as the excess carriers recombine. The increase of the wafer's conductivity is detected by the changing inductance of a coil, placed below the wafer. The coil is part of an oscillating circuit, which, as a consequence of the shift in inductance, changes its frequency [90]. The TrPCD measurements were conducted using a WCT-100 wafer-lifetime tool by Sinton Instruments.

Since the wafer's thickness and silicon's charge carrier mobilities are known, the amount of excess carriers Δn can be calculated directly from the measured increase in conductivity. Given minority charge carrier lifetimes far greater than the decay time of the flash, the injection dependant effective charge carrier lifetime is then the result of the division of the measured excess charge carrier density by its temporal gradient [91]:

$$\tau_{\text{eff}}(\Delta n) = \frac{\Delta n}{|\frac{\partial \Delta n}{\partial t}|} \tag{3.1}$$

Implied Fill Factor

The result of the TrPCD measurement $\tau_{\text{eff}}(\Delta n)$ can be used to calculate an implied jV curve based on the passivation properties of the silicon wafer and an assumed photogenerated current density j_{Ph} [92]. The voltage is directly calculated from the excess charge carrier density Δn, as it is, under optimal conditions, equal to the Fermi level separation induced by the photogenerated excess carriers [93]:

$$V = \frac{kT}{q} \ln\left((n_0 + \Delta n)(p_0 + \Delta n)/{n_i}^2\right) \tag{3.2}$$

Here k is the Boltzmann constant, T the temperature and q the elementary charge. The current is then calculated from the difference between the assumed photogenerated current density and the recombination rate given by effective lifetime measurement:

$$j = j_{\mathrm{Ph}} - qd\Delta n/\tau_{\mathrm{eff}}(\Delta n) \tag{3.3}$$

Here d represents the wafer's thickness. From the resulting implied jV curve the implied fill factor (iFF) can be determined. The iFF does not include loss mechanisms arising from a potential degradation of the passivation during the subsequent metallisation process or from transport barriers respectively series resistance effects. It therefore represents an upper limit for the achievable FF based on the passivation quality provided by the a-Si:H deposition and patterning processes.

3.2.3 Photoluminescence

In a photoluminescence measurement (PL) a passivated wafer is exposed to a light source emitting photons with an energy greater than the wafer's band gap. Depending on the optical properties of the wafer's surface and its thickness, a certain amount of these photons will be absorbed by the wafer. The absorbed photons generate charge carriers, which eventually recombine, given the fact that the wafer is not contacted. In a wafer with a high charge carrier bulk lifetime and high quality surface passivation, a large portion of the photogenerated charge carriers will recombine radiatively, emitting photons with an energy corresponding to the wafer material's band gap. A photodiode can then detect the emitted photons. The intensity of the emitted light directly relates to the passivation quality of the wafer. If an array of photodiodes (e.g. a camera sensor) is used, the passivation quality of the wafer can be spatially resolved. Well passivated areas on the wafer, where radiative recombination dominates, will appear bright, defect-rich areas, where SRH recombination is predominant, dark.

The setup used for this work is equipped with light emitting diodes emitting light with a wavelength of 650 nm. An optical filter blocking light with wavelengths up to 800 nm is attached to the corresponding camera, ensuring that only radiative recombination is captured. The setup did not allow to differentiate between recombination within the bulk or at the surface. Since only high-quality float-zone silicon wafers were used, dark areas were mainly caused by improper surface passivation. While it is possible to calibrate PL setups in order to gain quantitative information about the passivation quality, for instance an effective lifetime analogue to the aforementioned TrPCD method, PL measurement results in this work were only used for qualitative comparisons among different wafer samples.

3.2.4 Suns-V_{OC}

The V_{OC} of a solar cell strongly depends on the illumination intensity I. By altering the latter, it is therefore possible to generate an I–V_{OC} curve. Assuming a linear relation between I and the j_{SC}, the curve can be transformed into a j_{SC}–V_{OC} curve, where the j_{SC} at AM1.5G illumination is set to the expected or measured value for the specific solar cell technology (i.e., 41.5 mA/cm^2 for an IBC SHJ solar cell in this work). The fill factor of this pseudo jV curve is called pseudo fill factor (pFF) [94]. Since the Suns-V_{OC} curve is measured entirely under open circuit conditions with no current extracted from the device, the pFF is not influenced by series resistance related losses. Hence the difference between the FF extracted from the normal jV curve and the pFF is a good indicator for series resistance related loss contributions to the FF (if the latter is not limited by S-shapes resulting from non-linear transport barriers). On the other hand, a significant difference between the pFF and the iFF indicates a potential degradation of the passivation during the metallisation process.

Suns-V_{OC} curves were measured using the respective Suns-V_{OC} accessory station to Sinton Instrument's WCT-100 wafer-lifetime tool.

3.2.5 Transfer Length Method

The transfer length method (TLM) allows to determine the contact resistivity of a layer stack consisting of two or more layers [95, 96]. The layers are structured into multiple, parallel stripes of equal area and shape, but differing in spacing (see Figure 3.1). The resistance of two neighbouring stripes is then plotted over their respective distance. If the contacts between all layers are ohmic, the resulting curve follows a linear trend. By extrapolating the curve the resistance value R_C, representing the resistance for a distance of zero, can be determined as half of the intersection with the ordinate. The half of the absolute value of the intersection with the abscissa gives the so-called transfer length L_T [97]. Taking into account the geometry of the stripes, the contact resistivity ρ_C can be calculated using the following equation [98]:

$$\rho_C = R_C L_T w \frac{1}{\coth(t/L_T)} \tag{3.4}$$

Here w represents the width of the stripes and t their length. Knowing R_C and L_T it is also possible to determine the sheet resistance $R_\square$ of the material between the stripes:

$$R_\square = \frac{R_C}{L_T} w \tag{3.5}$$

$R_{\square}$ represents the superposition of the sheet resistances of the materials between the two fingers, that contribute to the current transport. In most cases one material features a much lower resistance than the others and thus represents the dominant current path. For instance, in case of silver metal stripes on top of an ITO layer and a silicon wafer substrate, the TLM method will provide the resistivity of the ITO/Ag contact and the sheet resistance of the ITO, as it is usually significantly more conductive than the wafer bulk. If the ITO is structured together with the silver fingers, the contact resistivity extracted by the TLM method will be a superposition of the both contacts, silicon/ITO and ITO/Ag, with the latter likely being orders of magnitude lower than the former. Furthermore, the resistance of the current path within the silicon wafer will be extracted. This value usually correlates to the wafer's nominal resistivity, however in the presence of doped a-Si:H layers on the c-Si wafer, between the TLM stripes, the accumulation of majority charge carriers in the wafer might affect the resistance of the wafer current path.

The jV curves between the respective metal stripes were measured using the 4-point probes method, thus eliminating any resistance contribution arising from the contact resistance between the probes and the metal stripes.

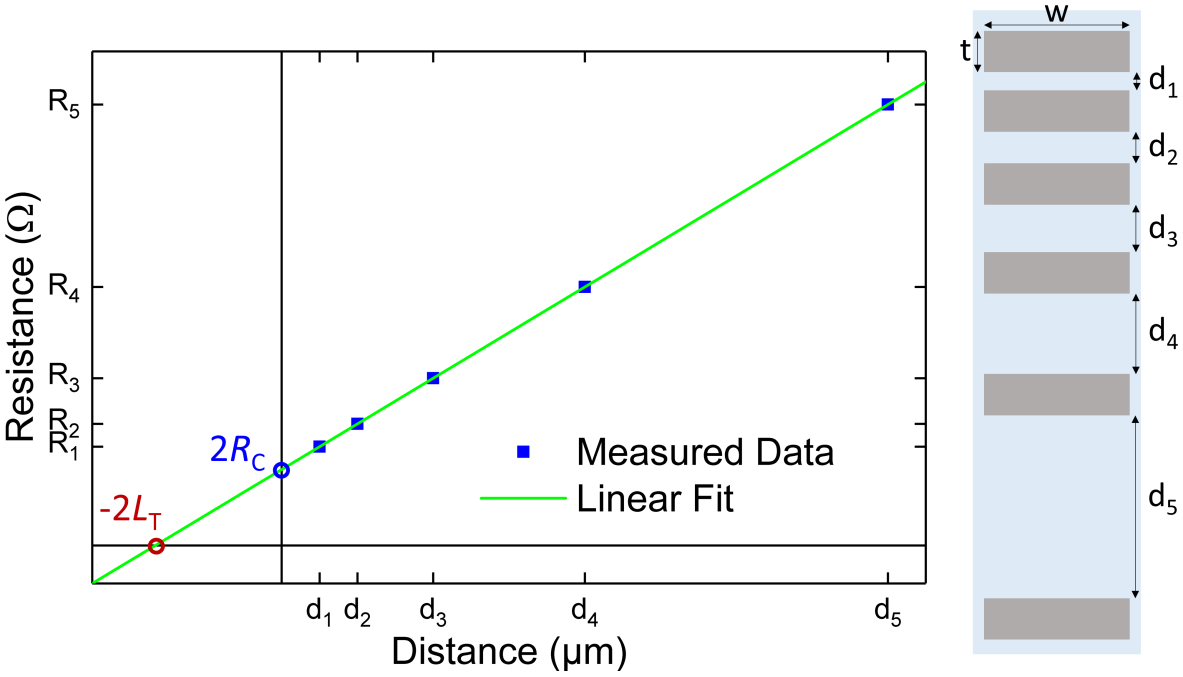


Figure 3.1: Determination of the TLM method's characteristic parameters R_{C} and L_{T} based on measured resistance values and linear fitting; the corresponding TLM structure is depicted on the right side.

3.2.6 Series Resistance Calculation

The total series resistance of a solar cell (as depicted in Figure 2.8) can be determined in many different ways [99]. For this work, two methods were primarily used. The first one compares the voltage values of the Suns-V_{OC} curve and the light jV curve at the maximum power point of the latter. Since the Suns-V_{OC} curve is not affected by series resistance related losses [94], the voltage difference ΔV_{Suns} divided by the j_{mpp} yields the series resistance $R_{S,Suns}$ [100]:

$$R_{S,Suns} = \frac{\Delta V_{Suns}}{|j_{mpp}|} \tag{3.6}$$

For this method to function properly, it is beneficial to perform both the jV and the Suns-V_{OC} measurement under the same conditions, with respect to contacting, temperature control and masking of the cell. This was not the case in this work, as the jV curve was measured with a solar simulator and the Suns-V_{OC} curve with a flash device. Slight deviations in cell temperature and less accurate cell area masking resulted in higher V_{OC} values for the Suns-V_{OC} measurement. If this V_{OC} difference is in the range of ΔV_{Suns}, the induced error for the calculation of $R_{S,Suns}$ is large. Consequently, the Suns-V_{OC} curve was shifted towards lower abscissa values until the V_{OC} values of both measurements were equal. Since the dependence between the V_{OC} and V_{mpp} of the Suns-V_{OC} curve is not linear, as this correction method assumes, the error is reduced but not entirely eliminated. However, a reduction in V_{OC} by 20 mV (no shadowing compared to accurate shadowing of the cell area) resulted in a V_{mpp} decrease of 17 mV, indicating an almost linear dependency. Thus the remaining error is expected to be marginal.

In the second method the Suns-V_{OC} curve is replaced by the dark jV curve, shifted by subtracting the j_{SC}, so that ΔV_{dark} and consequently $R_{S,light\_dark}$ can be determined accordingly [101, 102]:

$$R_{S,light\_dark} = \frac{\Delta V_{dark}}{|j_{mpp}|} \tag{3.7}$$

The dark jV curve is indeed measured with the same setup as the light jV curve, but even if the current at $|j_{SC} - j_{mpp}|$ is small, the dark curve is not free from series resistance effects. Thus a correction parameter is introduced, based on the virtual V_{OC} of the shifted dark curve $V_{OC,dark}$, the V_{OC} of the light jV curve and the j_{SC} [103]:

$$R_{S,dark} = \frac{V_{OC,dark} - V_{OC}}{|j_{SC}|} \tag{3.8}$$

The corrected equation for the dark jV approach is then:

$$R_{\mathrm{S,light\_dark,corr}} = \frac{\Delta V_{\mathrm{dark}} - (|j_{\mathrm{SC}}| - |j_{\mathrm{mpp}}|) R_{\mathrm{S,dark}}}{|j_{\mathrm{mpp}}|} \tag{3.9}$$

The accuracy of this method is limited by the accuracy of $R_{\mathrm{S,dark}}$, which is only an approximation of the resistance impacting the dark jV curve. However, according to Pysch *et al.*, the two methods presented yield the most reliable results [99]. Both methods are visualised in Figure 3.2.

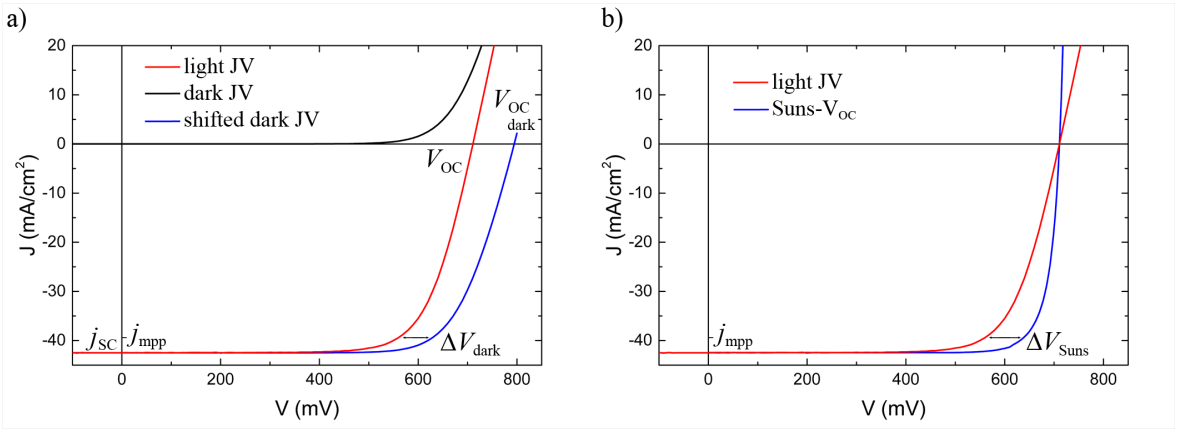


Figure 3.2: Visualisation of a) the dark jV comparison method and b) the Suns-V_{OC} comparison method to determine the series resistance, including relevant parameters.

3.2.7 Quantum Efficiency

The quantum efficiency (QE) of a solar cell indicates its capability of transforming an incoming photon with a specific energy into free charge carriers able to contribute to an external current. The prefix *external* is used if the absorption properties of the solar cell are taken into account, and consequently *internal* if only absorbed photons are considered.

The external quantum efficiency (EQE) is measured by exposing the solar cell to a light source through a monochromator that is tunable in the wavelength range relevant for the device under test (from 300 nm to 1200 nm in case of a silicon solar cell). The measured current per incoming power represents the spectral responsivity $SR(\lambda)$ (in A/W) of the solar cell. For each wavelength, the measured current divided by the elementary charge q equals the electrons per second contributing to the external current,

while the input power divided by the corresponding photon energy equals the incoming photons per second. Thus the EQE can be calculated by dividing these two rates:

$$EQE(\lambda) = SR(\lambda) \cdot \frac{1}{q} \cdot \frac{hc}{\lambda} \equiv \frac{\text{electrons/second}}{\text{photons/second}} \tag{3.10}$$

Here h represents the Planck constant, c the speed of light and λ the corresponding wavelength. In contrast to the EQE, the IQE does not take the reduction in input power due to an imperfect absorption into account. The absorption of a solar cell is reduced by reflection and transmission losses, $R(\lambda)$ and $T(\lambda)$. Hence the internal quantum efficiency (IQE) is calculated as follows:

$$IQE = \frac{EQE}{1 - R(\lambda) - T(\lambda)} \tag{3.11}$$

Two custom QE setups were used in this work. The first one features a spot size of $6\,\text{mm}^2$, generated from a dual-lamp setup (a halogen and a Xenon lamp). The second setup is equipped with only one halogen lamp, but its light spot covers an area greater than $25\,\text{cm}^2$, allowing to fully illuminate the entire cell area (accurate cell shading is necessary). While the first setup features a higher accuracy in the wavelength range below 450 nm, the amount of illuminated emitter or BSF area cannot be determined owing to the size of the light spot being only slightly larger than individual emitter or BSF fingers. In the absence of a specific EQE cell that features an emitter ratio of 100 % (see subsection 4.2.1), the second setup is therefore favourable.

Reflection measurements

The reflection properties of the corresponding solar cells were measured with a UV-VIS spectrometer. The solar cell is mounted onto an integrating sphere and then exposed to a monochromatic measurement beam, with wavelengths ranging from 300 to 1200 nm.

Transmission was regarded as being negligible, since the solar cells consist of at least 250 µm thick wafers with an almost entirely metallised rear side (metal coverage of 94 to 95 %, depending on the emitter to BSF ratio).

3.2.8 Raman Spectroscopy

Raman spectroscopy is used to examine the structural properties of a material. The sample is exposed to a laser light source preferably emitting photons with an energy higher than the sample material's band gap (resonant Raman spectroscopy) and thus interact with the material's phonons causing the emission of energy-shifted photons (Stokes-Raman scattering). The energy difference between the incident and the emitted

photons contains information about the material's properties. Raman spectroscopy is often used to determine the crystallinity of a sample. For instance, in crystalline silicon Anti-Stokes shifted photons cause a narrow peak 520 cm^{-1} wave numbers shifted from the original peak of the incident laser light, while in amorphous silicon a broader peak shifted by 480 cm^{-1} can be observed [104].

In this work, Raman spectroscopy was used to determine the thickness of amorphous silicon layers on crystalline silicon substrates, based on a method developed by Ledinský et al. [105]. Amorphous silicon on top of crystalline silicon attenuates the c-Si peak at 520 cm^{-1} by partially absorbing both the incident and the emitted photons. If the absorption coefficient α of the amorphous silicon layer is known, its thickness d can be calculated using the Lambert-Beer law:

$$d = \frac{\ln(I_0/I)}{2\alpha} \tag{3.12}$$

Here I_0 represents the intensity (shifted by 520 cm^{-1}) measured on a bare silicon surface, and I the intensity attenuated by the overlayer of amorphous silicon.

Raman measurements were performed on a MonoVista SP-2500i tool from Spectroscopy & Imaging (S & I GmbH), using a stimulation wavelength of 532 nm. The spot size is approximately 10 μm, the integration time was set to 10 s.

3.2.9 Constant Final-State Yield Spectroscopy

Constant final-state yield spectroscopy (CFSYS) is a photoelectron spectroscopy (PES) method used to determine the density of occupied states within the valence band and the band gap of amorphous silicon. In contrast to conventional PES methods (ultra-violet, UPS and x-ray, XPS) the excitation energy of the photons the sample is exposed to is the variable parameter, whereas the kinetic energy at which the analyser detects the emitted electrons, is fixed [106]. This value is then chosen in a way that only electrons with an energy slightly higher than the sample's work function are detected. Since the excitation energy is varied between 6 and 7.5 eV, the information depth reaches 5 to 10 nm into the investigated layer, thus the measurement is less affected by surface states. The setup used for this work contains a Xenon high pressure lamp with a double monochromator, providing a sufficient photon flux up to 7.5 eV. The resulting energy interval (from E_F to about -3.5 eV) allows only states in the band gap and close to the valence band edge of a-Si:H to be included in the measurement [107, 108].

3.3 Simulation

Simulation constitutes an integral part of solar cell optimisation. It allows to analyse the influence of a plethora of parameters and their variation, discovering or verifying trends that experimentally could not or only vaguely be observed. This holds true in particular for back-contacted silicon heterojunction solar cells that are built using complex and thus time-consuming manufacturing methods, especially if photolithography processes are involved. The simulations performed for this work did not aim to quantitatively replicate experimental results, but confirm trends and determine or rather explore areas worthwile of optimisation.

In the following, the general characteristics and capabilities of the simulation tool Sentaurus TCAD will be presented, followed by a detailed description of the actual modelling of an interdigitated back contact silicon heterojunction solar cell device, its simulation and the validation of the simulation software.

3.3.1 Sentaurus TCAD

In contrast to both-side contacted solar cells, where the current flow can be assumed to be one-dimensional (1D), a proper simulation of back contacted solar cells requires a two-dimensional (2D) or in case of point contacts a three-dimensional (3D) representation of the solar cell device. Prior to this work, the tool AFORS-HET was specifically developed to simulate SHJ interfaces and corresponding solar cells [65]. Since AFORS-HET is limited to 1D-models, the simulations in this work were performed with Sentaurus TCAD, a commercial and comprehensive tool for semiconductor simulation [109]. The data used to model amorphous silicon within AFORS-HET – incorporating physical properties like band gaps, density of states and defect distributions – was transferred to Sentaurus, which lacks a proper built-in a-Si model. The SHJ simulations performed with Sentaurus were then validated by replicating 1D-simulation results obtained with AFORS-HET.

The Sentaurus TCAD software suite contains multiple modules, from which the structure editor (SDE) and the device simulator (Sentaurus Device or SDevice) are the most relevant for this work. The semiconductor devices, numerically simulated by SDevice, are represented by a meshed and thus discretised model. Input (material type and properties etc.) and output (electric potentials, charge carriers etc.) parameters of the numerical equations are then assigned to each mesh point. Values of any simulated physical quantity between these points are obtained by interpolation.

Electrical simulation Each device simulation starts by solving the Poisson equation to determine the electrostatic potential within each mesh point of the device, preferably in equilibrium conditions. In case of a silicon solar cell, the equation reads

$$\epsilon\nabla^2\phi = -q(p - n + N_\mathrm{D} - N_\mathrm{A}) - \rho_\mathrm{trap}, \tag{3.13}$$

where, ϵ represents the electrical permittivity, q the elementary charge, n and p the electron and hole densities, N_D and N_A the concentration of ionised donors and acceptors, respectively, and ρ_trap the charge density due to traps and fixed charges [32]. Electron and hole densities are calculated from the corresponding density of states and (quasi)-Fermi potentials. For improved physical accuracy and since Fermi levels close to band edges are common for highly doped semiconductors, Fermi statistics instead of the Boltzmann approximation were used. In contrast to the ionised donor and acceptor densities and the trap densities, the electron and hole densities represent mobile charge carriers. The models used to describe their transport obey the continuity equations and thus charge conservation:

$$\nabla \cdot \vec{J}_\mathrm{n} = qR_\mathrm{net} + q\frac{\partial n}{\partial t} \qquad -\nabla \cdot \vec{J}_\mathrm{p} = qR_\mathrm{net} + q\frac{\partial p}{\partial t} \tag{3.14}$$

Here $\vec{J}_\mathrm{n}$ and $\vec{J}_\mathrm{p}$ represent the electron and hole current density and R_net the net recombination rate, indicating the sum of all generation and recombination processes within the device. $\partial n/\partial t$ and $\partial p/\partial t$ equal zero, as no transient simulations were performed. $\vec{J}_\mathrm{n}$ and $\vec{J}_\mathrm{p}$ are calculated using the drift-diffusion model. The corresponding equations read as follows:

$$\vec{J}_\mathrm{n} = -nq\mu_\mathrm{n}\nabla\Phi_\mathrm{n} \qquad \vec{J}_\mathrm{p} = -pq\mu_\mathrm{p}\nabla\Phi_\mathrm{p} \tag{3.15}$$

Here μ_n and μ_p represent the electron and hole mobilities and Φ_n and Φ_p the electron and hole quasi-Fermi potential, respectively.

As discussed in section 2.1.1, the primary recombination mechanisms within silicon are SRH, Auger and radiative recombination. In the simulations for this work, the SRH recombination in crystalline silicon is quantified by simply setting an effective lifetime τ_eff. Recombination at a-Si/c-Si interfaces depends on the defect densities of the corresponding a-Si layer. At other interfaces (like a passivating silicon nitride layer) a surface recombination velocity S_front may be defined (if in a symmetrical passivated sample $\tau_\mathrm{bulk} >> \tau_\mathrm{surf}$, then $\tau_\mathrm{eff} \approx \tau_\mathrm{surf}$ and $S_\mathrm{front} \approx d_\mathrm{Wafer}/2\tau_\mathrm{surf}$). Auger and radiative recombination are calculated in accordance with the parameterisation of Richter et al. [110] (implemented by D. Carrió [72]).

Optical simulations The optical generation rate within the simulated device is either provided by an external generation profile, transferred from a corresponding AFORS-HET simulation (and thus mainly based on the Lambert-Beer law, perfect internal reflection and rays thus passing the absorber multiple times) or by Sentaurus' own simple application of the Lambert-Beer-law (optical beam absorption method). In the latter case, Sentaurus extracts the optical data of the layer stack and then calculates the absorption for a given amount of wavelength values and intensities – the solar spectrum in this case.

Boundary conditions Boundaries without contacts exhibit reflective boundary conditions, meaning that all potentials and current densities at the edges of the simulation domain equal zero.

External contacts are regarded as ohmic with no contact resistance attached to them. As a result, external voltages are applied without any further contact resistance related losses.

3.3.2 Definition of Device Geometry and Parameters

The actual solar cell structure was created using the Sentaurus Structure Editor (SDE). The output file of SDE contains the device's geometry, its static properties (material type, doping profiles) and the meshed grid. This file then serves as the input for the simulator SDevice. Figure 3.3 shows the process flow among the different tools.

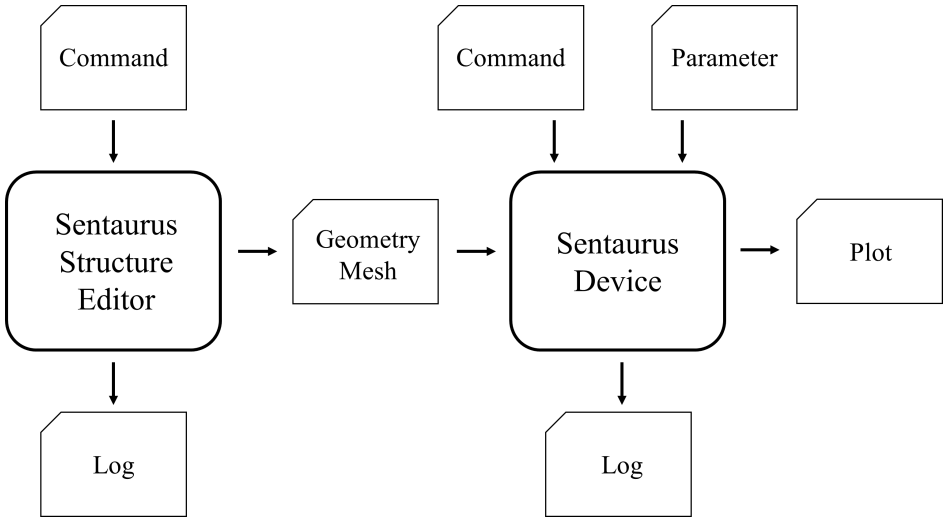


Figure 3.3: Sentaurus tool flow.

The dimensions of the simulation domain match the geometry of the corresponding experimental cells, with respect to the pitch, the overlap of n- and p-fingers and the

metallisation gap. The width of the corresponding contact fingers is only half of its real world equivalent, as the simulation domain functions as a symmetric unit cell, enabled by the inner boundary conditions.

Since an interdigitated approach is used for the contact geometry of the back contacted SHJ solar cells, a 2D representation, as shown in Figure 3.4, is sufficient. The substrate is formed by a 260 μm thick silicon layer with a standard width of 600 μm, corresponding to a 1.2 mm real world pitch. A 5 nm SiO_2 layer acts as front side passivation, with a fixed $S_{\text{front}} = 5\,\text{cm/s}$. Since within Sentaurus, amorphous silicon is not available as a material type, the rear side contact layers - intrinsic as well as p-type and n-type amorphous silicon - are modelled using the material type *polysilicon*. The intrinsic a-Si equivalent features a thickness of 5 nm, the doped ones a thickness of 20 nm each. The width of the contact layers corresponds to the emitter coverage values featured in the photolithography masks of the experimental cell. These range from 86 to 52 %. The overlap, inherent to the experimental design, has a standard width of 15 μm. The metal contacts are simulated using 1.5 μm silver layers. The metallisation gap's standard width is 40 μm, accounting for an experimentally determined etch loss of 5 μm per side, which is added to the 30 μm design width. Since a TCO at the rear side is primarily used to optimise the solar cell's optical properties, it was omitted in the simulated structure, as the main objective of the simulation was to optimise the rear side geometry rather than including a perfectly accurate optical model. Moreover, potentially non-ohmic characteristics of the a-Si/TCO interfaces were not regarded to be relevant for simulations primarily aiming to optimise the contact geometry.

The doping density applied to the crystalline silicon substrate yields a specific wafer resistivity of 3 Ωcm, in line with the 1 to 5 Ωcm of the wafers used for the experimental solar cells. The doping densities of the corresponding a-Si layers were chosen so that the energetic difference between the quasi-Fermi level and the appropriate band edge equalled the corresponding value in AFORS-HET for both polarities. All doping densities are applied as constant profiles across the total area of the respective layer, as in neither the c-Si wafer nor the thin a-Si layers, a variation in doping efficiency with layer thickness is expected.

Figure 3.4 shows the layer stack of the simulation domain as well as the unit cell excerpt from the real world contact geometry. Table 3.1 summarises the parameters for each layer in the standard configuration.

Table 3.1: Thicknesses and doping densities of each layer

	c-Si	i a-Si	n a-Si	p a-Si	SiO_2	Ag
thickness (μm)	260	0.005	0.02	0.02	0.005	1.5
doping density (cm^{-3})	$1.559 \cdot 10^{15}$	10^3	$7.084 \cdot 10^{19}$	$7.74 \cdot 10^{19}$	/	/

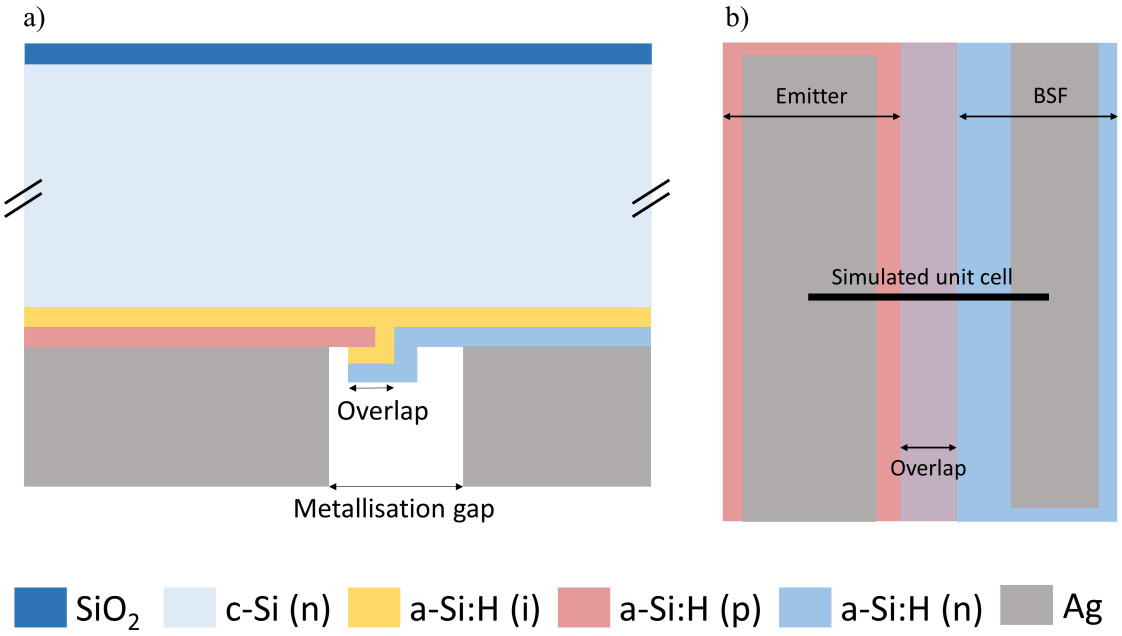


Figure 3.4: Not drawn to scale side view (a) and plain view of the rear side (b) of the simulation domain; the simulated emitter and BSF width correspond to half of the real world values.

If an external file is used for the optical generation within the structure, it needs to be implemented in SDE. The optical generation is only applied to the silicon bulk layer, hence the optical properties of the remaining layers are not relevant.

Finding proper meshing settings is a vital part of the structure design. A fine mesh improves the accuracy of the simulation, but can lead to prolonged computing time. A sparse mesh results in lower computing time, but degrades the simulation's accuracy and might also cause convergence issues. The Sentaurus manual recommends to set particularly dense meshes in areas of high current density, high electric fields and high charge generation. The first two points relate to the contact areas, especially the n-contact that, usually being the contact with less area, extracts the same amount of current density per total area as the p-contact. Charge generation happens mostly in the first few micrometers of the silicon wafer at the front, followed by an exponential decay (Lambert-Beer law). The meshing strategy is outlined in Appendix B.

3.3.3 Device Simulation

The SDevice simulator receives three input files. The file generated by SDE contains the geometry of the simulation domain, the material types, the doping profiles, and the mesh, as discussed in detail in the previous section. The parameters of the different material types are listed in a dedicated file. Furthermore the properties of certain interfaces are specified. Table 3.2 lists selected parameters used to model crystalline

and amorphous silicon (χ refers to the electron affinity and N_C and N_V to the density of states in the conduction and valence band, respectively). The description of the a-Si defect states, both the band tails and the mid-gap states, can be found in Appendix B.

Table 3.2: Silicon parameters

	E_G eV	χ eV	N_C cm^{-3}	N_V cm^{-3}	μ_n cm^2/Vs	μ_p cm^2/Vs	τ_{eff} ms
c-Si	1.124	4.05	$2.843 \cdot 10^{19}$	$2.682 \cdot 10^{19}$	1041	412.9	10
a-Si	1.72	3.9	10^{20}	10^{20}	20	5	/

The command file contains information about the physical models and the simulation setup (an equilibrium simulation or a voltage sweep). A standard jV curve simulation starts by solving the Poisson equation coupled with the calculation of the electron and hole densities, and then repeats this procedure for the gradually increased voltage values applied to the p-contact.

Tunnelling Since the simulated device features hetero-interfaces including band offsets, tunnelling through thin barriers is a non-negligible transport path within such a device. To simulate the tunnelling transport path through the intrinsic amorphous silicon passivation layer, Sentaurus' non-local tunnelling model (NLM) was used. The NLM works by defining a non-local mesh in the command file, and assigning it to the corresponding interface alongside a distance value indicating the maximum extension of the non-local mesh. Apart from the specified distance, the tunnelling probability depends on the tunnelling masses assigned to the materials forming the interface (set to $0.1\, m_0$ for both electrons and holes in accordance with [111]) and the corresponding band structure. The calculations are based on the WKB tunnelling probability model and an additional model based on the Schrödinger equation. A detailed description of both approaches can be found in [112] and the Sentaurus Device User Guide (page 684) [109].

3.3.4 Validation with AFORS-HET

As already mentioned in subsection 3.3.1, Sentaurus lacks a proper integration of amorphous silicon as a material type. Based on Sentaurus's polysilicon material class, a-Si is emulated by adjusting various parameters (Table 3.2), especially the band gap, the charge carrier mobilities and the defect distribution. The corresponding values are taken from the tool AFORS-HET that was specifically developed to simulate 1D a-Si/c-Si heterojunction solar cells. The aim of the validation is to replicate the results of a comparable AFORS-HET simulation in order to confirm the successful modelling of amorphous silicon within Sentaurus. To reduce the influence of geometry and

Table 3.3: AFORS-HET vs. Sentaurus jV parameter

	V_{OC} (mV)	j_{SC} (mA/cm^2)	FF (%)	η (%)
AFORS-HET	715.7	39.78	79.09	22.52
Sentaurus	717.0	39.77	78.63	22.42

meshing in particular, the test structure is kept very simple: a 1D, both side contacted heterojunction. Since the used version of AFORS-HET does not feature a tunnelling implementation, it is omitted in the Sentaurus structure. Figure 3.5 shows the layer stack of the test structure. The two simulation results are compared with respect to their band diagrams in dark equilibrium conditions and the solar cell parameters extracted from a light jV curve with the same generation profile. The difference between the band edges and the Fermi level yield very similar results for both simulation tools (3 neV for c-Si, a maximum difference of 5 meV for the band bending within the a-Si layers). These small deviations are likely caused by mesh variations and a slight difference in how accurate both tools solve the equations determining the band structure (Boltzmann statistics were used in both simulations). The jV parameters of both simulated cells are also in good agreement, as the data in Table 3.3 and the almost identical jV curves, depicted in Figure 3.6, show.

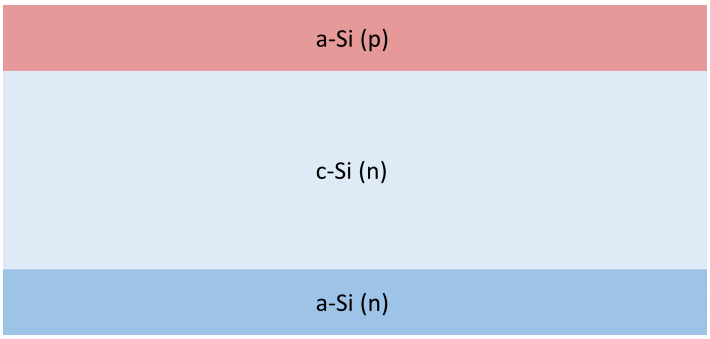


Figure 3.5: Layer stack simulated in AFORS-HET and Sentaurus to validate the amorphous silicon integration.

Although not completely identical, the good agreement of the two simulation results indicates a successful integration of amorphous silicon into Sentaurus and thus justifies its use for the simulation of further, more complicated heterojunction solar cell devices.

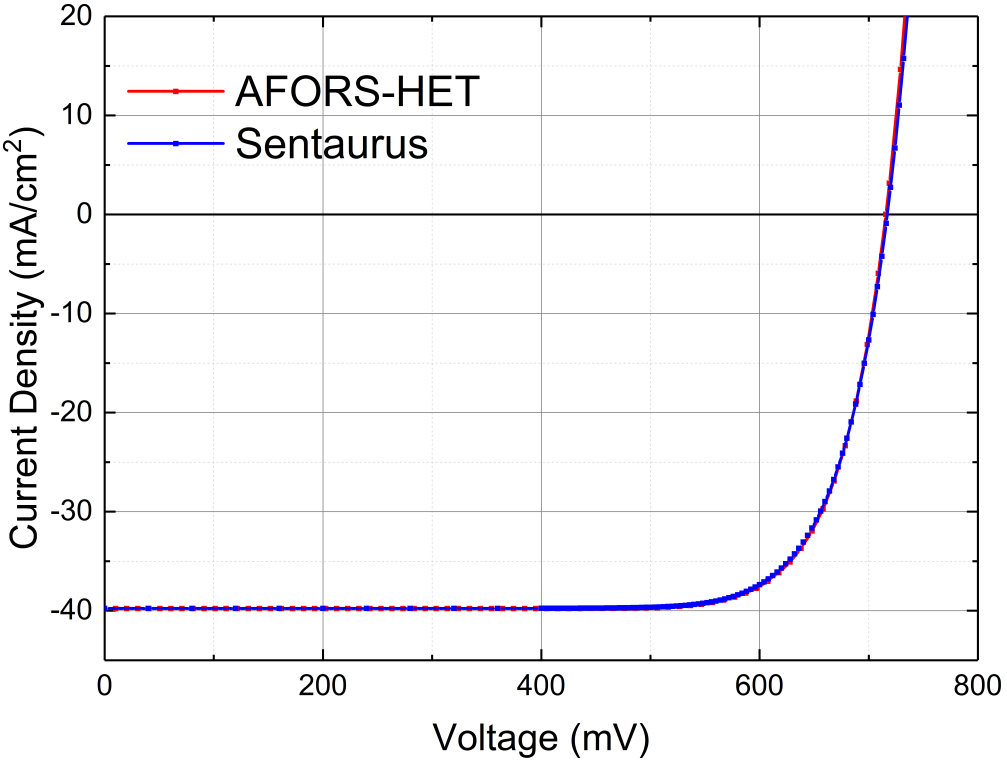


Figure 3.6: Two jV curves, generated by the simulation of an identical structure in AFORS-HET and Sentaurus, respectively.

Chapter 4

Process Development for IBC SHJ Solar Cells

The manufacturing of standard heterojunction solar cells is a rather straight-forward process. It involves the initial wafer cleaning and the consecutive full-area deposition of thin amorphous silicon, TCO, and metal films, from which only the metallisation layer at the front and in some instances the underlying TCO require to be patterned (by means of in-situ shadow masking and screen-printing).

For back contacted heterojunction solar cells, as described in subsection 2.2.3 and depicted in Figure 2.7, the necessity to structure multiple layers at the rear side of the device increases the complexity of the manufacturing process substantially. The following chapter describes two possible manufacturing methods, which differ drastically in both their level of patterning accuracy and their complexity:

The **photolithography** process serves as a reference process as it yields the most accurate patterning results. This comes at the price of high complexity. Since it mainly requires wet chemical etching processes to pattern the corresponding layers, the resistance of all other layers exposed to the specific etchant needs to be taken into consideration. As a consequence, additional layers are necessary to protect chemically vulnerable layers. Furthermore, the use of wet-chemical etching processes entails the need for multiple wet-chemical cleaning steps between the deposition steps.

The **shadow mask** process uses silicon hard masks during the PECVD depositions to structure the amorphous silicon layers in-situ. The accuracy of this patterning technique and the achievable minimum feature size mainly depend on the quality of both mask and alignment method. Subsequent metallisation layers can be deposited by screen printing, thus completely avoiding any wet-chemical steps apart from the initial

wafer cleaning. Despite being largely outperformed by photolithography with respect to patterning accuracy and minimum feature size, shadow-mask based techniques are a potential candidate for an industry-compatible manufacturing process for IBC SHJ solar cells.

4.1 Methods and Tools

In the following, the specific methods and tools used to manufacture the solar cells presented in this work are described.

4.1.1 PECVD

Plasma-enhanced chemical vapour deposition, as described in section 3.1.1, is the most vital technology in order to build high-efficiency silicon heterojunction solar cells. During the the course of this work, three different PECVD tools were used:

The **FAP** tool was a PECVD cluster tool manufactured by FAP, Dresden, with a parallel plate PECVD tool operating at radio frequency, consisting of two process chambers, assigned to the deposition of intrinsic (RF, 13.56 MHz) and doped (RF, 60 MHz) amorphous silicon layers, respectively. The chamber pressure for SiH_4 based processes was usually 0.5 mbar with gas flows of 10 sccm for SiH_4 and 2 sccm for the doping precursor gases (diborane, B_2H_6 and phosphine, PH_3). The hydrogen plasma following the intrinsic a-Si deposition was performed at a chamber pressure of 1 mbar with a H_2 gas flow of 20 sccm. The plasma power density equated to 19 mW/cm^2 for the a-Si deposition processes and to 56 mW/cm^2 for the H_2 plasma process. Process temperatures were set to 190 °C for the intrinsic layer processes and 135 °C for the doped layer processes. Solar cells built with this tool are also presented in [113] and [114].

The **AltaCVD** tool from Altatech is a cluster tool with a parallel plate RF-PECVD operating at 13.56 MHz as well. Since the AltaCVD tool was only set up during the work for this thesis, process optimisation remains an ongoing process to this date. Hence, no fixed and optimised process parameters can be listed. The initial version of the AltaCVD tool was designed to work with higher pressure values and gas flows compared to the FAP tool, resulting in chamber pressures of up to 5 mbar and gas flows reaching 60 sccm for SiH_4 and 40 sccm for B_2H_6, respectively. In later stages, the gas supply and vacuum system was overhauled in order to lower the chamber pressures and gas flows and thus decrease the deposition rate, enhancing control and reproducibility of thin layer depositions. Process temperatures are around 200 °C in general, the plasma power

density is around 18 mW/cm^2. In contrast to the FAP tool, one of the two available process chambers was used for the deposition of intrinsic and p-type a-Si:H layers, the other for n-type a-Si:H and silicon oxide layers.

The **AKT** tool (AKT1600 by Applied Materials) is another cluster tool with a parallel plate RF-PECVD, operating at 13.56 MHz. Compared to the aforementioned FAP and AltaCVD tool, which were both built solely for research purposes, the AKT tool is a semi-industrial multi-substrate system, being capable of storing six carriers at once with each carrier supporting up to four wafers with a diameter of up to 5″ (alternatively one larger M2 sized wafer). In accordance with the much larger process chambers, high gas flows are needed: up to 300 sccm for SiH_4 and H_2, and 100 respectively 6 sccm for B_2H_6 and PH_3. Process temperatures range from 190 °C to 205 °C, power densities from 13 (15) mW/cm^2 for intrinsic (p-type) amorphous silicon layers to 190 mW/cm^2 for nanocrystalline processes. AKT-based amorphous and nanocrystalline silicon layers are also discussed in [115–118].

While there is a chronological component to the reason why three different PECVD tools were used during this work, contrasting the FAP and the AKT tool allows to pinpoint advantages and disadvantages for both. The FAP tool excels with respect to its flexibility. Being mainly manually controlled, quick changes to single process parameters are easy to implement. On the other hand, the lack of automation regarding the process sequences impaired the reproducibility and required the operator's presence for a comparably large amount of time. This is further exacerbated by the fact that only one wafer per run can be processed.

Being a semi-industrial system, the AKT tool is almost fully automated, granting excellent reproducibility and a high wafer throughput. Furthermore, since the AKT tool is primarily used for the standard heterojunction solar cell baseline of the PVcomB institute, the degree to which both amorphous but also nanocrystalline silicon processes are available and sufficiently optimised constitutes another significant reason to favour it.

The AltaCVD tool offers a similar level of automation as the AKT tool. Since the AltaCVD tool lacks sufficiently optimised deposition recipes, its potential could not be fully exploited.

4.1.2 Deposition of Contact Materials

Contact materials such as TCO and metal layers were deposited using the following processes. Sputter deposition, as described in section 3.1.1, was used for all TCO

materials – indium tin oxide (ITO), aluminium-doped zinc oxide (AZO) and tungsten oxide (WO_X) – and occasionally to form a silver seed layer. Thermal evaporation (see section 3.1.1) was used to deposit aluminium layers onto doped amorphous silicon layers, silver layers onto TCO layers or thicken initially sputtered silver layers. In very few cases screen printing was used to apply a silver paste onto a TCO layer.

Sputtering

ITO layers were fabricated using MicroSys 200 PVD RF-sputter tool manufactured by Roth & Rau. The tool consists of a dedicated loadlock with a base pressure in the range of $1{\cdot}10^{-6}$ mbar and a process chamber with a base pressure around $5{\cdot}10^{-7}$ mbar. The three targets, placed above the rotating substrate holder, have a diameter of $2''$, leading to an imperfect thickness homogeneity on $4''$ wafers (up to 20 % deviation). ITO and WO_X are sputtered at a plasma power of 70 W from an indium tin or a tungsten target, respectively. For the former 0.2 % O_2 is added to the Ar/O_2 sputter gas mixture, for the latter variable amounts of oxygen were used.

AZO and silver layers were sputtered in a Leybold Optics large-area inline DC-sputter tool using either a ZnO:Al target with 1 % doping and adding 0.35 % oxygen to the Ar/O_2 sputter gas mixture or a silver target in a pure Ar plasma.

All sputter processes were performed at room temperature, hence as-deposited layers are amorphous.

Evaporation

Silver and aluminium were evaporated under high vacuum conditions in a Creavac evaporation system, using resistive heating of a tungsten crucible. The distance between the material source and the wafers amounts to approximately 50 cm. For an increased layer homogeneity, the wafers are rotating during the evaporation process. The film thickness control is provided by a quartz crystal.

Screen-printing

Silver-polymer pastes were printed in a Baccini screen printer, with a screen-to-sample distance of 2.5 mm, an applied pressure of 65 N and a printing speed of 150 mm/s.

4.1.3 Laser Ablation

In order to fit the wafers with completed solar cells into the custom made measurement chuck – providing accurate shadowing and four-point contacting – two of the wafer's edges are cut off using a ROFIN-BAASEL Lasertech tool. The laser operates in pulsed

mode with a pulse length of 12 ps at a frequency of 50 Hz, with a wavelength of 1064 nm and a scribing speed of 15 mm/s. The number of scribes depends on the thickness and the surface properties of the corresponding wafer.

The same laser tool was also used to fabricate the silicon masks for the shadow mask patterning process and to prepare wafers for the alignment procedures (e.g. cutting of edges or laser cutting of holes).

4.2 Photolithography Process

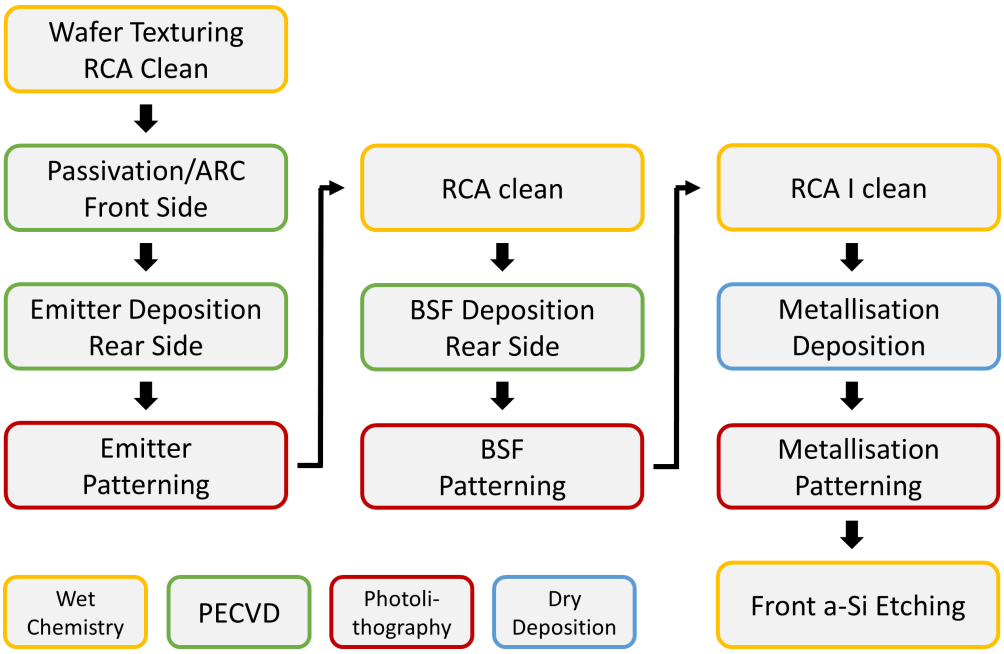


Figure 4.1: Process sequence of the photolithography process.

The following subchapter represents an extensive description of the IBC SHJ solar cell manufacturing process, in which the patterning of the rear-side layers is based on photolithography processes. Here, a single photolithography process describes the sequence of applying a photoresist layer to a wafer, structuring this photoresist layer by means of UV light exposure and developing, and eventually etching one or more layers being partly covered by the structured resist. Fabricating a complete IBC SHJ solar cell requires at least three of these photolithography processes, as the emitter, the BSF layer and the metallisation layer stack are all patterned individually. Hereafter, the term *photolithography process* without the prefix *single* refers to the entire manufacturing process of the solar cell rather than just one individual patterning step. Figure 4.1 visualises the process flow of the photolithography process.

The overall process sequence is based on general guidelines that were established at the institute prior to this work. During the course of this work, the following adjustments were made to improve the quality and the reproducibility of the process:

Improved Photoresist Adhesion For a functioning photolithography process, proper adhesion of the photoresist to the layer to be structured is vital. Silicon layers are covered with a native oxide that exhibits hydrophilic properties resulting in insufficient photoresist adhesion potentially leading to the presence of micrometre sized air bubbles. These bubbles then act as lenses during the subsequent UV light exposure, deflecting light towards their centre. Consequently the photoresist near to the air bubble's edges is not or only insufficiently exposed and remains on the substrate during the developing. The adhesion can be improved by exposing the substrates to a hexamethyldisilazane (HMDS) atmosphere prior to the photoresist deposition. However this method did not produce reliable results, hence a mandatory dip in hydrofluoric acid (HF, 1 % in H_2O) was established as a new standard procedure.

Direct Silver Evaporation Prior to this work, silver seed layers with a thickness of up to 400 nm were sputtered onto the rear side ITO layers to provide sufficient adhesion of the silver layer. In a subsequent step, the sputtered silver layer was thickened by thermal evaporation to achieve the desired total thickness of approximately 1.5 μm. Owing to the thermal energy input of the silver sputter process, it is assumed that at least the surface region of the underlying ITO starts to crystallise. To etch this region, it is necessary to increase the concentration of the etchant (usually hydrochloric acid). The etch rate for the amorphous parts of the ITO is then too high to enable a controlled etch process. Consequently undesired etching below the photoresist/silver layer stack (underetching) is hardly to avoid. This results in a poor fidelity with respect to the pattern or even the complete detachment of the silver overlayers. The partial crystallisation of the ITO layer can be prevented, if instead of sputtering a silver seed layer, the entire silver layer is directly evaporated onto the ITO. Adhesion problems could not be observed, likely benefiting from the fact that the contact fingers are at least 130 μm wide.

Non-destructive Protection Layer Etching Until the end of the manufacturing process, the front side layers forming the anti-reflective coating (usually silicon nitride) are protected by a layer of intrinsic amorphous silicon. Prior to this work, the protective a-Si layer was removed before the patterning of the rear side metallisation layers using an acidic solution based on phosphoric and nitric acid, but also including a small portion of hydrofluoric acid. This solution does not only provide a high etch

rate for amorphous silicon but also for most silicon nitride derivatives. Consequently the selective etching of the two materials is an almost impossible task, resulting in the degradation of the front side layer stack, both with respect to its optical and passivation properties. Low concentration alkaline solutions like tetramethylammonium hydroxide (TMAH 2.5 wt% in H_2O) or sodium hydroxide (NaOH 0.6 wt% in H_2O) do not etch silicon nitride and therefore represent a viable alternative to acidic solutions.

In the following the individual steps of a *single* photolithography process are described. The respective etch processes are outlined in the subsequent material-specific sections.

Resist deposition

The photoresist layers are applied by spin coating. The spinning speed and time depend on the substrate's surface. The used positive resist, AZ4533 from Microchemicals, yields a layer thickness of 3.3 μm for a spinning speed of 4000 rpm. This is sufficient for planar substrates. For textured surfaces on which the height of the random pyramids might exceed 5 μm, the spinning speed is adjusted to 800 rpm, resulting in a thickness of approximately 7 μm (thickness increases with the square root of the spinning speed). Although only the layers on the rear side of the solar cell device need to be patterned, a protective photoresist layer is also put onto the device's front side. To guarantee sufficient photoresist adhesion, a clean, particle free and hydrophobic surface is of vital importance. The substrates are therefore initially heated to break OH-bonds being present on the oxidised silicon surface. Additionally, before spin-coating the rear side photoresist layer, the wafers are dipped in hydrofluoric acid (HF, 1 %) to further improve the hydrophobic nature of their surface. After spin coating, the photoresist layer contains a significant portion of solvent molecules. In a drying step lasting 30 minutes at maximum, these solvent molecules diffuse towards the resist's surface. In a subsequent temperature step ("soft bake", 90–100 °C), either done in an oven or on a hotplate, the solvent molecules then evaporate leaving a solid photoresist layer behind. Afterwards, if one or both photoresist layers were spin coated at 800 rpm, the resulting photoresist bulge at the edges is removed by applying a jet of acetone onto the edge of the spinning substrate. Thus, during the exposure, the mask can be pressed flat onto the substrate and gaps between the two are avoided.

UV light exposure

Since the photoreaction triggering the increase in solubility of the photoresist requires water molecules, the substrates are exposed to a humid atmosphere (air humidity of at least 65 %) for 15 to 20 minutes. The rehydrated substrates are then mounted into

a mask aligner and exposed to light with a wavelength of 365 nm and an intensity of 20 mW/cm^2. The exposure time depends on the thickness of the photoresist layer (7 s for 3 μm thick and 20 s for 7 μm thick photoresist layers).

Developing

The light-exposed photoresist layers are then developed in an alkaline solution. Sodium hydroxide with concentration of 0.6 % usually dissolves 3 μm thick photoresist layers in 35 to 45 s, for 7 μm thick layers the time increases to 80 to 90 s. To further increase the chemical robustness of the photoresist layer, an additional temperature step ("hard bake", 110–115 °C) follows.

Resist removal

After etching, the photoresist is removed by rinsing the substrates in acetone, isopropyl alcohol and and deionised water.

4.2.1 Cell Layout

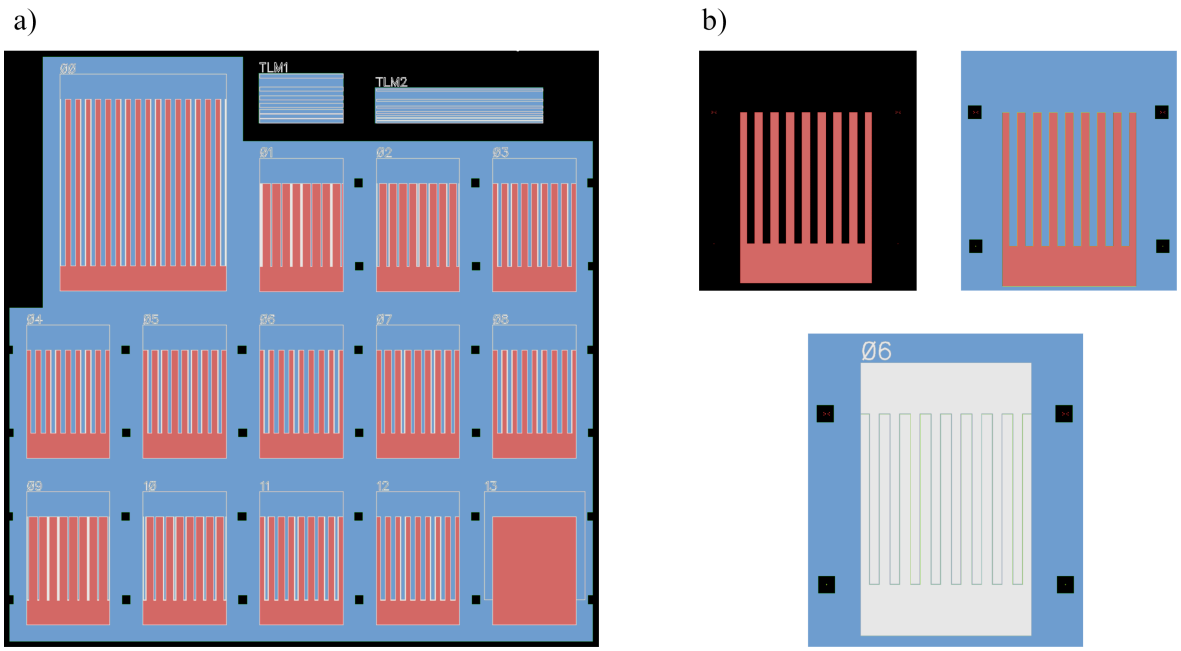


Figure 4.2: Mask layout for the photolithography process: a) all masks shown en bloc, emitter in red, BSF in blue, metallisation as a white outline for better visibility b) a single cell, with identical colour scheme.

The layout of the solar cells is defined by the layout of the photolithography masks. The masks used to manufacture the presented solar cells were designed prior to this

work by Jan Haschke [119]. The design incorporates a total of 14 cells on a 4″ wafer, 13 with a cell area of 1 cm^2 and one with a cell area of 4 cm^2, not including the bus bars. The cells all feature an interdigitated contact pattern with a pitch of 1.2 mm and differ with respect to their emitter-to-BSF ratio. Figure 4.2 visualises the arrangement of the cells on the wafer and Table 4.1 summarises the variations of the emitter coverage. Cell 13 features an emitter coverage of 100 %, which is useful for EQE measurements: in most EQE setups the actual light spot is small compared to the cell area; if the spot illuminates mainly the BSF area, the extraction efficiency is likely to be lower compared to illuminating the emitter area only. Measuring the EQE on cell 13 therefore results in an upper limit EQE result, as the entire cell area consists of emitter area.

Table 4.1: Solar cell geometry parameter

cell number	emitter coverage (%)	cell area (cm^2)	pitch (mm)
1,9	86	1	1.2
2,10	77	1	1.2
3,5,7,11	65	1	1.2
4,6,8,12	52	1	1.2
0	52	4	1.2
13 (EQE)	100	1	/

To preserve the passivation quality across the entire cell area, it is necessary to prevent thin intrinsic a-Si:H layers from being directly exposed to air or the TCO sputter deposition processes. Therefore the emitter and the BSF contact fingers form a narrow, 15 μm wide overlap. The overlap also helps to compensate underetching effects that could otherwise, in case of an overlap-free design, lead to gaps between the n-type and p-type a-Si:H regions, as depicted in Figure 4.3 (a certain amount of underetching, referring to the etching of the layer below the photoresist mask, has to be taken into account for wet-chemical processes, especially if the etching is not entirely homogeneous; for the etch processes used in this work, underetching in the range of up to 5 μm was observed). Moreover, the BSF layer does not only cover the regions between the emitter fingers and the corresponding busbar area, but is extended towards the area between the cells, thus preserving the passivation there as well.

4.2.2 Wafer Preparation

All solar cells were processed on 4″ float-zone crystalline silicon wafers with a nominal resistivity of 1 to 5 Ωcm. The front side was always textured to reduce reflection and thus increase absorption. The rear side was either polished or textured. All wafers were textured in-house using an IPA free solution based on potassium hydroxide (*Alka-Tex*

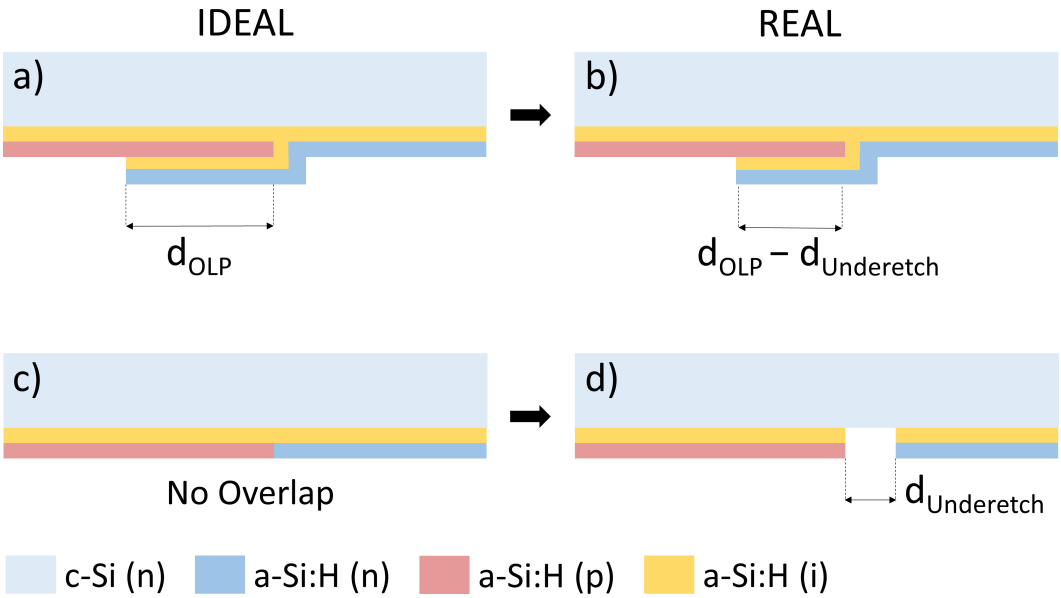


Figure 4.3: Overlap and underetching: a) and c) represent the ideal cases, in which there is either an overlap with the defined width d_{OLP} or perfect alignment without an overlap; in reality etch processes based on wet chemicals always exhibit a certain amount of underetching, resulting in the reduction of the overlap width by $d_{Underetch}$ (b); if there is no overlap in the first place, underetching leads to gaps in the wafer passivation (d).

free by GP Solar [120]). During the texturing process, polished rear sides were protected by a PECVD grown SiO_2 layer with a thickness of 0.5 to 1 μm.

In general, the wafer manufacturer (TOPSil in this case) delivered the wafers in two conditions: *as cut* (no further processing of the wafer's surface after it was cut from the crystalline silicon boule) or single-side polished with the non-polished side exhibiting a homogeneous, cobblestone-like surface structure. As a consequence of this difference in surface conditions, the texturing processes did not yield identical results in terms of the pyramids' size and distribution. Double-sided textured wafers, based on the *as-cut* material, featured usually much larger pyramids than their single-side polished counterparts. These larger pyramids are likely the consequence of the unintentional initiation of pyramid-growth during the preceding saw-damage-etch (sde) process. During the actual texturing process, the sde-grown pyramids then continue to grow, making them larger than intended. However, the pyramid size, especially the height, has a strong influence on both PECVD and photolithography processes.

Owing to the increase in surface area, textured surfaces require longer deposition times for the same layer thickness. Since the growth conditions in valleys, on side walls and tips of the pyramids differ, the resulting layer thickness also depends on the overall size and shape of the pyramids. Especially pyramid valleys and faceted

pyramid sides are prone to epitaxial growth, which is detrimental for the passivation quality [121]. If the disparity in pyramid size on the same wafer is high, meaning there are few large pyramids more or less homogeneously distributed among many smaller ones, it can become very difficult to deposit an a-Si:H layer that features an appropriate layer thickness and passivates the textured surface sufficiently.

In a photolithography process, it is vital that the entire surface is initially covered by the photoresist layer. As outlined in section 4.2, the AZ4533 photoresist achieves its maximum layer thickness of roughly 7 μm with a spinning speed of 800 rpm. Lower spinning speeds result in an inhomogeneous deposition. Textured surfaces, featuring pyramids higher than 7 μm, require the subsequent deposition of two photoresist layers to be fully covered. This drastically increases the process time in general and at the same time decreases the accuracy, due to longer exposure and developing times.

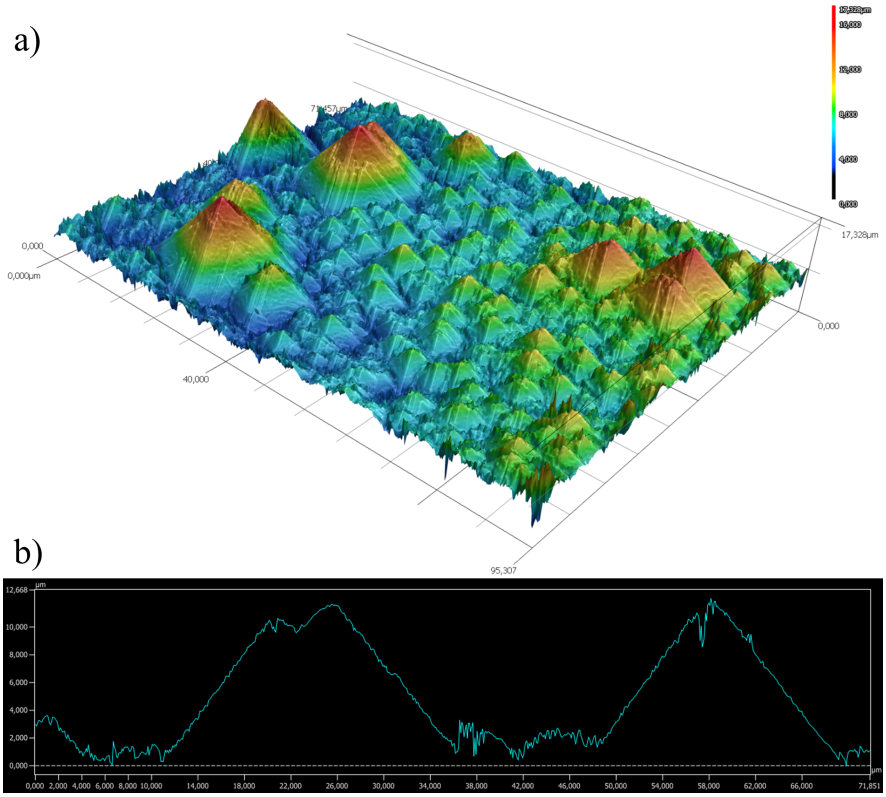


Figure 4.4: a) Microscopic image of a sub-optimally textured surface with inhomogeneous pyramid sizes (many small ones, a few large ones) b) Profile measurement indicating a pyramid height of up to 10 μm.

Textured surfaces with homogeneously sized pyramids are therefore of great importance, especially if the particular surface represents the rear side of the solar cell. Figure 4.4 shows microscopic images of differently sized pyramids indicating suboptimal surface conditions. Despite the disparity in pyramid size not always being as extreme as shown in Figure 4.4, inhomogeneously textured surfaces remained an issue for all

solar cells featuring textured rear sides. In recent texturing processes, the concentration and temperature of the solutions used for the sde process were adjusted in order to avoid the premature pyramid growth. Consequently, homogeneously textured surfaces were achieved.

RCA Clean

Before each deposition step, the wafers are cleaned using the RCA method developed in 1965 by the Radio Corporation of America (published in 1970, [122]). The RCA sequence involves two baths removing both organic and metallic contaminants at the wafers' surfaces. The first bath contains ammonium hydroxide and hydrogen peroxide (NH_4OH:H_2O_2:H_2O, 1:4:20) and leads to the formation of thin silicon dioxide layer, incorporating and underetching organic residues and surface particles. The second bath contains hydrochloric acid and hydrogen peroxide (HCl:H_2O_2:H_2O, 1:1:6). It removes metallic contaminants and forms a thin protective layer that is removed directly before the corresponding deposition step. The first bath is heated up to 70 °C during the process, the second to 80 °C. In-between both steps the wafers are dipped in hydrofluoric acid (HF, 1 % in H_2O) in order to remove the oxide from the first step.

The RCA clean is an essential step for each heterojunction solar cell process, as it determines the potential of the subsequent passivation by intrinsic amorphous silicon. Due to the heavy use of organic components during a photolithography process (photoresist, acetone etc.) and the resulting organic residues on the substrate, an RCA clean is necessary after each patterning or rather before each subsequent deposition step. The materials forming the respective layers at the front and the rear side of the solar cell have to either withstand the RCA procedure or be protected. Vulnerable front side layers (mostly silicon nitride) are therefore covered by a protective intrinsic amorphous silicon, as they would otherwise be etched by the HF-dip between the two RCA baths. An RCA clean, however, working by oxidising and reducing the silicon's surface, also etches amorphous silicon, in particular intrinsic and n-type a-Si. This effect has to be taken into account when depositing the aforementioned protection layers and n-type BSF layers as well. Alternatively lowering the temperature of the first RCA step, at the expense of cleaning efficiency, reduces the silicon etching effect [123].

4.2.3 Layer Deposition and Patterning

After the initial texturing process and the subsequent RCA clean, different layers are alternately deposited and patterned. In the following, each layer deposition step will be described.

Front Side Passivation and Anti-reflective Coating

Although not the primary focus of this work, the quality of the front side of an IBC SHJ solar cell is of vital importance. In this work two different approaches for the front sides were investigated: a double-layer silicon nitride (SiN_X) stack (provided by the Institute for Solar Research Hameln, ISFH) and a single-layer SiN anti-reflective coating (ARC) with an underlying intrinsic a-Si:H passivation layer (processed in-house). Since silicon nitride features a wider band gap than amorphous silicon, the SiN_X based front side stack provided by the ISFH leads to less parastic absorption. Furthermore, the use of two SiN_X layers allows for a better refractive index grading resulting in less reflection in the lower wavelength range, as depicted in Figure 4.5 a. While being optically superior, the passivation quality provided by the SiN_X stack is mediocre. A sample symmetrically deposited with the ISFH SiN_X stack achieved an effective minority carrier density lifetime in the range of 1 ms at a excess charge carrier density of $1{\cdot}10^{15}\,cm^{-3}$ (iV_{OC} 706 mV, iFF 80.3 %), a cell precursor with the in-house front side and emitter passivated rear side at least 3.5 ms at the same injection level (iV_{OC} 726 mV, iFF 83.6 %, see Figure 4.5 b).

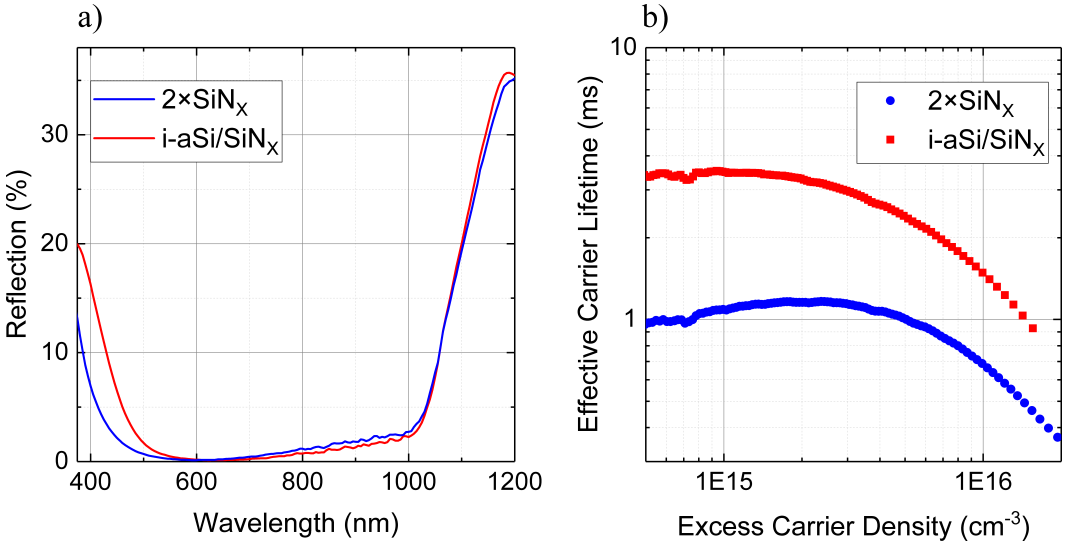


Figure 4.5: a) Reflection spectrum of the double-layer SiN_X and the a-Si:H/SiN_X front side; owing to the better refractive index grading, the former performs better in the lower wavelength range b) lifetime curve of a sample symmetrically passivated with the double-layer SiN_X front side (blue) and a cell precursor with the a-Si:H/SiN_X front side and an emitter rear side passivation.

The in-house a-Si:H/SiN_X front side layer stack was deposited in the AKT tool by PECVD. An initial 15 nm thick intrinsic a-Si:H layer, hydrogenated with a H_2 plasma process, passivates the c-Si surface. It is followed by a 70 nm thick SiN_X ARC layer with a refractive index of 1.92. To protect the SiN_X layer from the subsequent etching

and cleaning steps, an additional 100 nm thick intrinsic a-Si layer is deposited. All three steps are carried out without breaking the vacuum.

p-type a-Si:H Emitter

P-type a-Si:H emitter layers were deposited either in the FAP or in the AKT PECVD cluster tool. The *emitter deposition* step always incorporates the deposition of an intrinsic a-Si:H passivation layer and the subsequent emitter layer, both in one run without breaking the vacuum, if the AKT tool is used. It is also referred to as the deposition of the *(i,p)-stack*.

In both PECVD tools, the intrinsic a-Si:H layer is hydrogenated by an H_2 plasma, saturating open silicon bonds as well as breaking weak silicon–silicon bonds and replacing them with more stable silicon–hydrogen bonds. To achieve a thickness of 5 nm, the loss in thickness arising from the H_2 plasma etching has to be taken into account (0.2 nm in the FAP, approximately 4 nm in the AKT tool). The thickness of the emitter layer depends on the subsequent metallisation process. In case of an aluminium metallisation, the emitter should be at least 20 nm thick, as aluminium tends to diffuse into the amorphous silicon layers even at comparably low temperatures (150 °C) [124, 125]. To cope with the sputter damage the ITO deposition inflicts, the total thickness of the rear side a-Si:H stack should be in the range of 15 nm, meaning that the emitter layer should at least feature a thickness of 10 nm.

Emitter layers deposited in the FAP tool feature a homogeneous doping profile and resulting conductivity values of around $1{\cdot}10^{-5}$ S/cm. In the AKT tool, multiple emitter process recipes are available. The *non-graded* emitter process exhibits a homogeneous doping profile as well, with conductivity values of $2.6{\cdot}10^{-5}$ S/cm. The second process, the *graded* emitter, addresses the problem that emitter layers with a high conductivity significantly degrade the passivation quality of the underlying intrinsic a-Si:H layer, as the band bending induced in the c-Si wafer shifts the Fermi level in the intrinsic a-Si:H towards the valence band, thus increasing the amount of unsaturated defect states in it [61, 126, 127]. At the same time, lower doped emitter layers are less capable of forming an efficient tunnel-recombination contact with the degenerate n-semiconductor TCO materials [63]. The graded emitter process therefore deposits a thinner, lower doped emitter layer first, to form a less degrading contact to the intrinsic a-Si:H passivation layer, followed by a thicker and more conductive layer, suited to form an efficient contact to the TCO.

If the in-house front side stack, as described in section 4.2.3, was used, the textured and RCA cleaned wafers were coated in two consecutive runs. The three front side layers were deposited first, the wafers were then unloaded, flipped, and immediately

loaded back into the machine to then be deposited with the emitter contact stack. If the ISFH front side was used, the wafers were initially deposited with the protective front side intrinsic a-Si, RCA cleaned and then the corresponding emitter contact stack was deposited.

After the deposition of both the front and the rear side, the wafer is fully passivated. This allows to measure the effective minority carrier lifetime with TrPCD and investigate the spatial passivation quality with photoluminescence measurements (PL). Figure 4.6 shows the minority charge carrier lifetime curves and the corresponding PL images of two (i,p)-passivated cell precursors after the deposition, sample A and B. Sample A features a thicker intrinsic a-Si:H passivation layers, hence the initial passivation is slightly better. These values and images then act as a reference at later process stages, and their change allows to analyse the influence of the following process steps.

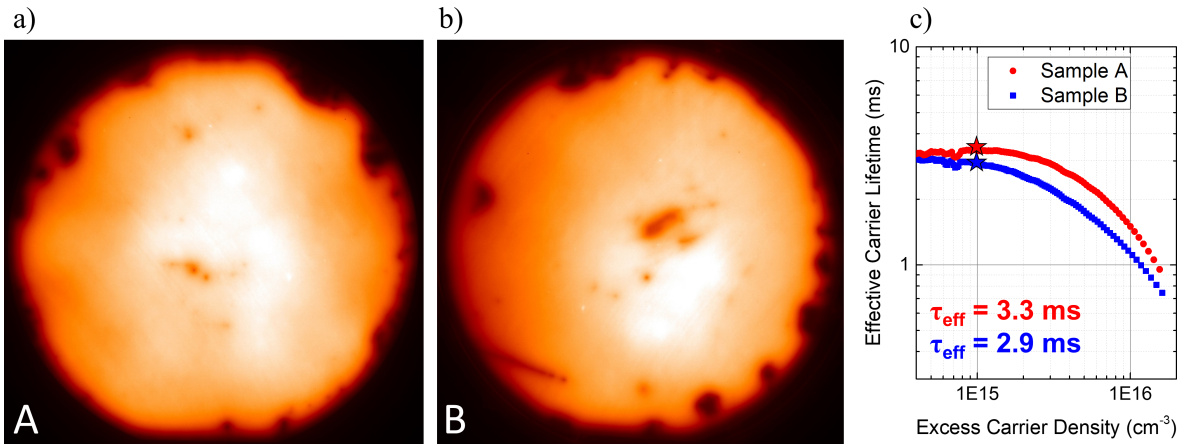


Figure 4.6: Photoluminescence images of two samples, A and B, after the initial passivation, front side i-aSi/SiN_X and rear side emitter (i,p)-stack, sample A features a slightly thicker rear side intrinsic a-Si:H layer; c) the corresponding TrPCD lifetime curves indicating a similar level of passivation (sample A: iV_{OC} 726 mV, iFF 83.6 %; sample B: iV_{OC} 720 mV, iFF 83.4 %).

The (i,p)-stack is then patterned using the photolithography method. The p-type amorphous silicon is etched by an acidic solution based on phosphoric and nitric acid, also including a small portion of hydrofluoric acid. It features a high etching rate for amorphous (regardless of polarity) and a low etching rate for crystalline silicon, resulting in a sufficient etch selectivity between a-Si and c-Si. During the etching, the front side needs to be protected by a photoresist layer, as otherwise the etchant would remove both the protective a-Si and the silicon nitride layer underneath.

n-type a-Si:H or nc-Si:H BSF

Analogous to the p-type emitter deposition, the n-type BSF deposition is always combined with an intrinsic a-Si:H passivation layer, and thus may also be denoted as the *(i,n)-stack*. The considerations with respect to the thickness do not differ from the ones for the emitter, meaning that in general the intrinsic a-Si:H layer should be 5 nm thick and the BSF layer 10 respectively 20 nm, depending on the metallisation.

In contrast to the always fully amorphous emitter layers, both amorphous and nanocrystalline BSF layers were used, the former deposited in the FAP, the latter in the AKT tool. Nanocrystalline layers feature much higher conductivity values (30 S/cm vs. $5{\cdot}10^{-3}$ S/cm for n-type a-Si:H), owing to their partly crystalline nature. Consequently the contact resistivity to the TCO layer is improved [117, 118]. As emitter and the BSF layers overlap, increased conductivity in either layer also increases the risk of a shunt across the overlap. Since the overlap region is narrow, both layers very thin, and the emitter still amorphous, thus exhibiting a low conductivity, the decrease in shunt resistance does not deteriorate the solar cell's performance. However, if both emitter and BSF layers were nanocrystalline (initial processes exist, see [116]), shunting issues might arise.

The PECVD process used to grow hydrogenated nanocrystalline silicon (nc-Si:H) layers starts with a strong hydrogen plasma, rendering a dedicated H_2 plasma process to hydrogenate the underlying intrinsic a-Si layer unnecessary. Since this initial H_2 plasma differs from the dedicated ones used in the emitter process (higher power in a shorter time period), its etching rate changes. Thus, using a nanocrystalline PECVD process for the BSF layer also requires a readjustment of the deposition time of the intrinsic a-Si layer below. Apart from that, it is also possible to intentionally reduce the thickness of intrinsic a-Si layer below the BSF layer, as the latter one does not degrade but increases the passivation quality by adding a field effect. For the solar cells manufactured using the FAP tool, the thickness target for the intrinsic a-Si:H passivation layer under both the emitter and the BSF was 5 nm, as this was determined to be the optimum value [128]. Intrinsic a-Si:H layers for solar cells manufactured with AKT tool are in the same range (inferred from the assumed deposition rates), but adjustments based on empirical lifetime tests were made.

Figure 4.7 shows lifetime curves and PL images corresponding to the samples shown in Figure 4.6, here after the deposition of the (i,n)-stack. This particular lifetime measurement represents an upper limit, as the patterned emitter layer is fully covered by the BSF layer, leading to an artificial increase of the passivation quality in the emitter regions by neutralising the influence of the p-layer on the Fermi level of the intrinsic a-Si:H layer.

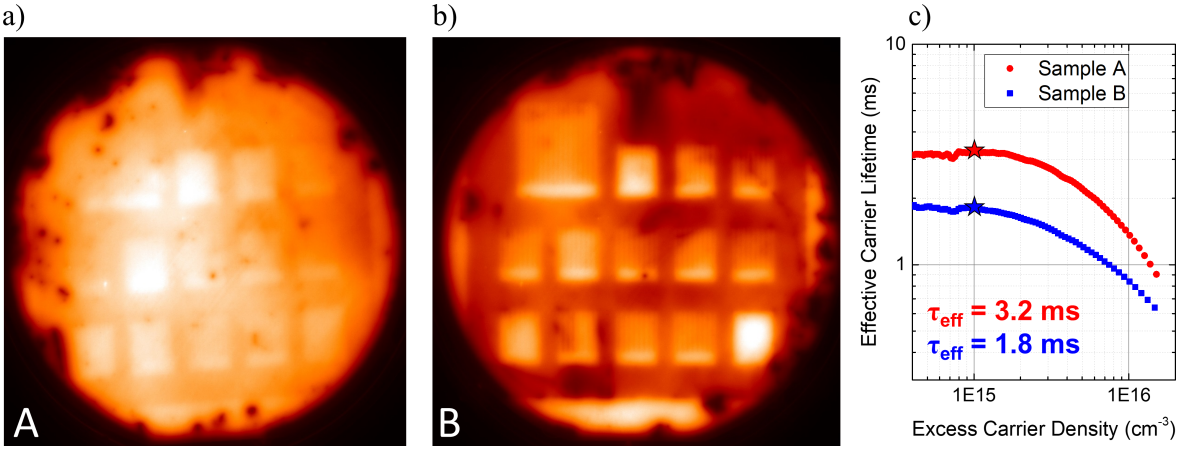


Figure 4.7: PL images of the two samples, A and B, after the repassivation with the BSF (i,n)-stack; the emitter regions are clearly visible, owing to the excess (i,n)-stack on top of the patterned emitter increasing the passivation quality. The (i,n)-stack on sample B does not passivate as well as the one from sample A, due to its thinner intrinsic a-Si:H passivation layer. This is also reflected in the TrPCD lifetime data (c), where sample B drops off while sample A remains at the level measured after the initial passivation (sample A: iV_{OC} 725 mV, iFF 83.5 %; sample B: iV_{OC} 711 mV, iFF 82.3 %).

Selective etching The BSF layer, regardless of its structural properties, amorphous or nanocrystalline, is etched with alkaline solutions like sodium hydroxide (NaOH) or tetramethylammonium hydroxide (TMAH). With concentrations as low as 0.6 wt% for NaOH and 2.5 wt% for TMAH (both in H_2O), these solutions will exhibit a sufficiently high etch rate for intrinsic and n-type a-Si:H/nc-Si:H layers (preceded by an HF-Dip to remove native oxide), but a much lower one for p-type materials. It is therefore possible to etch off the excess BSF layer on-top of the p-type emitter layer without notably affecting the latter. The effect is described in very detail in [129] and [130]. In short: during the etching a single silicon atom is removed from the lattice by bonding with four negative OH ions from the electrolyte:

$$\mathrm{Si} + 4\,\mathrm{OH}^- \longrightarrow \mathrm{Si(OH)_4} + 4\,\mathrm{e}^- \tag{4.1}$$

The four excess electrons remain in the conduction band very close to the surface of the silicon, where they are available to reduce water and create new OH^- ions (see Equation 4.2), which then proceed to bond with silicon atoms from the lattice, as indicated in Equation 4.1. Thus an ongoing silicon etch process is initiated.

$$4\,\mathrm{H_2O} + 4\,\mathrm{e}^- \longrightarrow 4\,\mathrm{OH}^- + 2\,\mathrm{H_2} \tag{4.2}$$

If the surface of the material to be etched is sufficiently p-doped, the space charge region formed between the silicon surface and the electrolyte becomes very thin. This results in the inversion layer at the silicon's surface being too narrow to confine the four electrons created by the initial reaction. Thus the majority of them will rather tunnel-recombine with holes in the valence band. Consequently the amount of newly created OH^- ions is not sufficient to uphold the initial oxidation reaction.

A similar a-Si:H structuring process, where the p-type layer acts as an etch stop, was published by Nakamura *et al.* in 2014 [131]. Their IBC SHJ solar cell achieved an efficiency of 25.1 %. This procedure also illustrates the necessity of an overlap region. If the corresponding mask layouts just complemented each other perfectly without an overlap region, inaccuracies during the alignment or slight underetching effects would result in narrow regions between the contact fingers, where the alkaline solution would be able to etch down to the c-Si surface, leaving behind unpassivated regions in the cell area (see also Figure 4.3).

Contrasting NaOH and TMAH, the latter was found to etch more homogeneously and with a slightly higher etch rate than the former. In addition to that, using the fully organic TMAH solution does not involve the risk of introducing metallic contaminants to the sample.

After etching the BSF layer, the patterning of the rear side a-Si:H/nc-Si:H layers is completed. Once again it is possible to measure the passivation quality, quantitatively with TrPCD and qualitatively with PL. Figure 4.8 shows the corresponding lifetime curves and PL images after the patterning of the BSF layer. As apparent in the PL image, the mask layout leads to small unpassivated regions in-between the cells, around the alignment markers. Therefore and in contrast to the measurements after the deposition of the BSF layer, the TrPCD measurement here represents a lower limit of the lifetime, as the measured area contains some of these unpassivated spots acting as recombination centres.

TCO and Metal

The ITO sputtered in the MicroSys 200 PVD sputter tool was originally developed to serve as a front side TCO for standard SHJ solar cells [132]. The resistivity amounts to approximately $4{\cdot}10^{-4}\,\Omega$cm and the absorption in the near-IR (800 to 1500 nm) is in the range of 20 %. Since this particular ITO is sputtered from a $2''$ target, the homogeneity on a $4''$ wafer is not ideal. While a layer thickness of 150 nm was usually targeted, the inhomogeneous colour impression of the layer indicates deviations down to the range of 100 nm. As the ITO is used on the cell's rear side, these thickness differences might

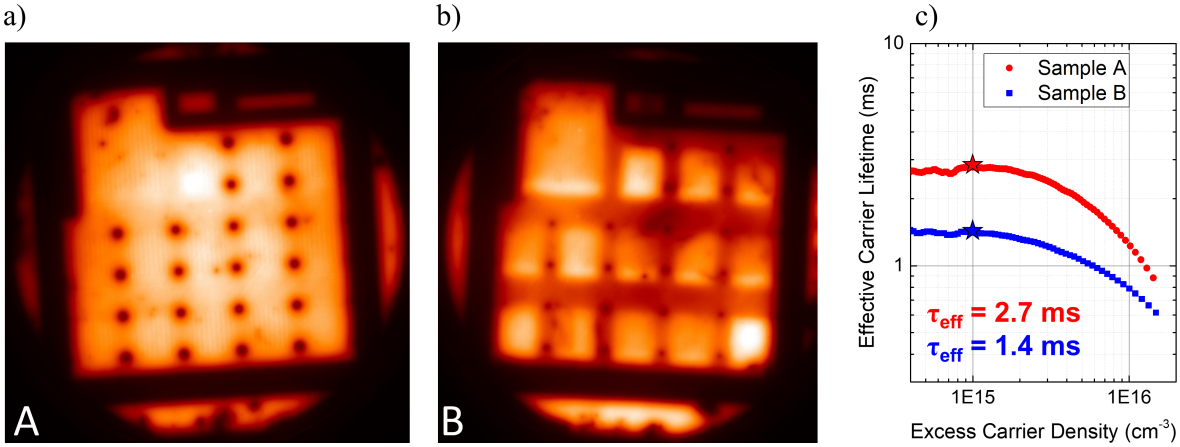


Figure 4.8: PL images of the two samples, A and B, after the patterning of the (i,n)-stack – sample A shows a very homogeneous level of passivation across the entire wafer, while it is very apparent that in the case of sample B the passivation of the emitter regions is better than the one in the BSF ones, owing to the thickness difference of the intrinsic a-Si:H passivation layer. The lifetime values in c) decrease for both samples, as the TrPCD measurement is slightly affected by the non-passivated areas (black dots) between the cells, indicating the regions of the alignment markers (sample A: iV_{OC} 722 mV, iFF 83.1 %; sample B: iV_{OC} 709 mV, iFF 81.5 %).

have a very minor influence on the j_{SC} of the solar cell, which was not regarded as significant.

AZO layers were deposited with a constant thickness of 70 nm. With only 1 % Al doping in the ZnO target, AZO excels in terms of transmission in the NIR, on the expense of conductivity, when compared to ITO.

The WO_X process was optimised by Mews and Lemaire [133]. The oxygen concentration in the process was kept to a minimum as conductivity was prioritised over transmission. The thickness of the WO_X layers amounts to 20 nm, and they were always used in conjunction with a 100 nm ITO layer on top.

The TCO deposition is usually followed by the deposition of roughly 1.5 μm silver. To guarantee good adhesion between the Ag and the ITO layer, the initial 400 nm Ag are sputtered. The final thickness is then achieved by Ag evaporation. In more recent cell series, the Ag sputter step was omitted, as the adhesion of the evaporated silver was sufficient for this particular IBC process (featuring rather large finger widths). In case of an aluminium metallisation, the 1.5 μm thick layer was directly evaporated onto the a-Si:H/nc-Si:H layers.

Etching Silver is etched by a solution based on ammonium hydroxide and hydrogen peroxide (NH_4OH:H_2O_2:H_2O 1:1:4). Aluminium was etched by an acidic solution based on nitric acid and acetic acid, at a temperature of 40 to 60 °C.

ITO is usually etched by hydrochloric acid (HCl, 25 %). Depending on the concentration and prior processes, the etch rate of the ITO can be very high. Thus underetching issues can occur, especially as the visual feedback of the etching process is limited – the corresponding ITO structure is entirely covered by the Ag layer. It was also observed that the used HCl solution etches ITO deposited onto n-type nc-Si:H much faster than ITO on p-type and intrinsic a-Si:H or n-type c-Si. While this phenomenon was not further investigated, a possible cause could be related to a difference in surface roughness – p-type a-Si:H layers usually exhibit a much rougher surface than their n-type counterparts. However, this theory is not necessarily backed by the observations on etching speed regarding intrinsic a-Si:H and n-type c-Si surfaces. On the other hand, ITO layers on which silver layers were sputtered often exhibited an increased etch resistivity. It is assumed that the thermal energy input by the sputter atom's kinetic energy initiated the crystallisation of at least the first few nanometres of the respective ITO layer.

AZO is also etched in HCl, albeit at a much lower concentration (2 % is sufficient). In many cases, AZO was already removed by the preceding Ag etching process.

Figure 4.9 shows the PL images after metallisation of two samples already shown in previous sections. The images are captured from the front side, as the almost fully metallised rear side (in cell areas) would otherwise block any incoming and outgoing light.

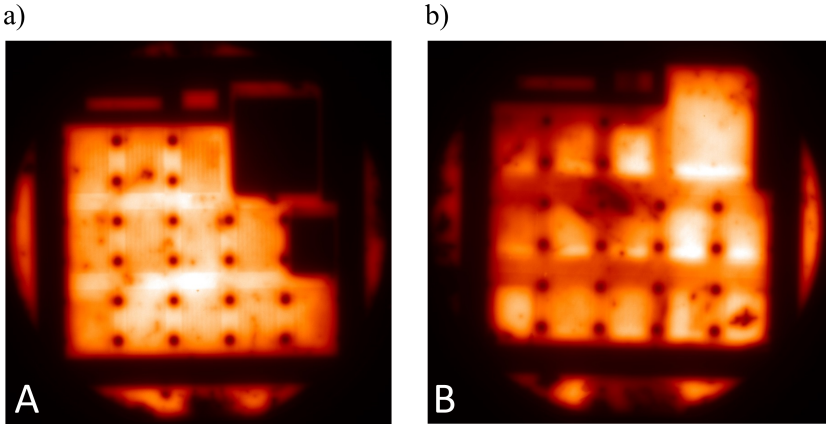


Figure 4.9: PL images of two samples, A and B, after metallisation and thus captured from the front side, unlike the previous images. On sample A the two dark cells in the top- and mid-right are shunted. The better BSF passivation of sample A remains clearly visible.

WO_X requires an additional patterning step, as it acts as an interlayer only between the p-type a-Si:H emitter and the ITO used as a TCO. After deposition, the WO_X layer is patterned with a photolithography process based on the mask used for the patterning

of the emitter. In contrast to ITO, WO_X is comparably stable in acidic solutions like HCl and HF. In alkaline solutions like NaOH (0.6 wt% in H_2O) however, the 20 nm WO_X layer can be removed within a few seconds, indicating a very high etch rate. Since NaOH is used as a developer solution, the WO_X layer is directly etched during the development of the UV-exposed photoresist layer. After removal of the photoresist and a brief HF-dip, ITO and Ag are deposited and patterned as described above. Since the WO_X pattern equals the one of the emitter, the entire overlap area and thus half the metallisation gap are still covered by WO_X. To avoid possible shunting and other parasitic effects arising from the a-Si:H/nc-Si:H/WO_X layer stack, the excess WO_X is removed by dipping the wafers into an NaOH bath a second time. The patterned layer can be seen in a PL image in Figure 4.10. Since WO_X absorbs both part of incoming (PL-LEDs) and outgoing light (radiative recombination), areas with WO_X appear darker. These areas are also sharply defined, indicating that this darkening is only an optical effect and not caused by lifetime degradation.

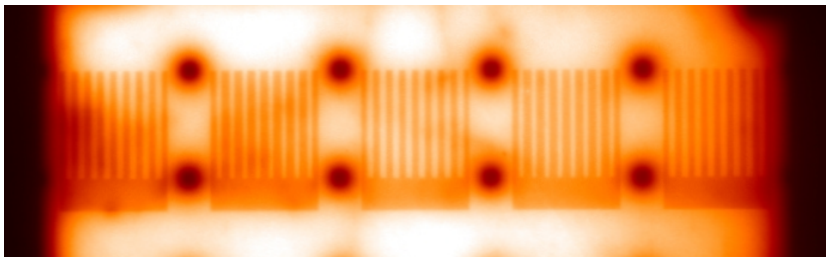


Figure 4.10: Excerpt of a PL image showing a sample with patterned WO_X. The WO_X layer on-top of the emitter structure absorbs both the incoming and the outgoing light of the PL measurement, thus it appears darker than the remaining area. Its structure is sharply defined indicating that the darkening is indeed an optical and not an electrical effect.

RCA 1 clean During this work, multiple solar cells were built in which either an RCA 1 cleaning step or just an HF-dip (1 % in H_2O) was performed prior to the deposition of ITO. While the solar cell results show no particularly clear trend, it is empirically concluded that at least an RCA 1 cleaning step should be performed prior to the deposition of ITO, as the preceding photolithography process introduces organic contaminants to the surface of the a-Si:H or nc-Si:H layers. Removing these contaminants will most likely lower the risk of S-shaped jV curves arising from a malfunctioning tunnel-recombination contact between the p-type a-Si:H emitter and the n-type ITO layer [63]. In cases where the RCA 1 clean before the ITO deposition was omitted, and the solar cells did not exhibit S-shaped jV curves, it is assumed that extended storage times led to the formation of a native oxide enclosing the organic

contaminants. While certainly not being as effective as a proper RCA 1 clean, the removal of this native oxide by the obligatory HF-dip before the ITO deposition could have been sufficient for the formation of a working tunnel-recombination contact.

4.2.4 Final Steps

After patterning the metallisation stack, the rear side of the solar cells is completed. Before measuring, the front side protective a-Si layer needs to be removed, and the wafer's edges need to be cut in order to fit the wafer into the custom measuring chuck that aligns cells and external contacts. Additionally, to improve the contact resistivity of the metallisation to the amorphous or nanocrystalline silicon layers, the wafers are annealed on a hotplate. Solar cells with a direct aluminium/a-Si:H contact are annealed at temperatures ranging from 150 to 170 °C (variable duration), cells with a TCO-based contacts at 190 (AZO) or 200 °C (ITO, WO_X) for 5 to 10 minutes [134].

The front side a-Si layer is etched with alkaline solutions, preferably TMAH, as these do not impact the underlying silicon nitride ARC layer – unlike the acidic solution used to etch the emitter layer. During the etching process, the rear side has to be protected with a photoresist layer, as TMAH would otherwise etch the exposed n-type nc-Si:H layers between the cells and in the metallisation gap, thus destroying the passivation. Since the native oxide on the front side a-Si is removed by an HF-dip prior to the TMAH etching, the photoresist layer also protects the rear side ITO from being etched by the HF.

A wafer ready to be measured is shown in Figure 4.11. The laser-cut edges have a minimal distance of 3 mm to the cell's edges, therefore laser-induced degradation of the passivation in cell areas is avoided.

4.3 Shadow Mask Process

First shadow mask based processes used to pattern the rear side of an IBC SHJ solar cell were reported in 2007 and 2008 [135, 136], and later in 2011 [137]. In 2014, Tomasi *et al.* presented 21 % efficient mask based IBC SHJ solar cells, and increased this value to 22 % in 2017 [138, 139]. Later in the same year, Paviet-Salomon et al. reported on further improvements of this particular mask based solar cell concept by achieving an efficiency of 23.9 % [140].

The shadow mask based process presented in this work was developed to serve as an alternative to the established photolithography process described in the previous section. Although the latter yields accurate patterning of thin films, long processing times (two to three weeks per cell batch on average) limit the number of experiments

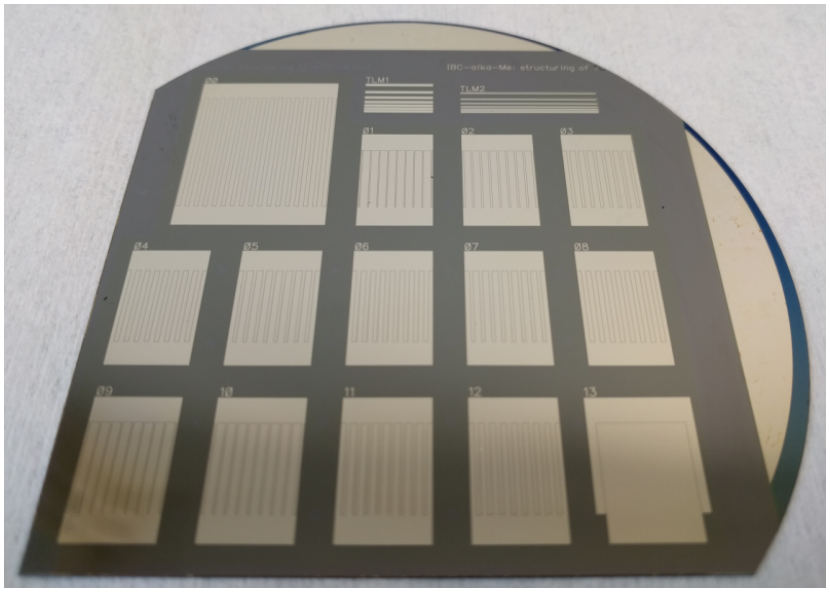


Figure 4.11: Photograph of the planar rear side of a finished wafer with IBC SHJ solar cells, manufactured with the photolithography process. The left and bottom edge are cut off to fit the wafer into the custom measurement chuck.

and thus insights gained in a given amount of time. Owing to the heavy use of wet chemicals during a photolithography process, the choice of materials is also limited to those that can either withstand or be protected from the various etching and cleaning steps. Furthermore, in contrast to photolithography, in-situ shadow masking is a simple, scalable and thus potentially industrially viable method to process IBC SHJ solar cells.

The main goal was therefore to create a simple and fast process that, while by no means being as accurate as its photolithography counterpart, still allows to vary certain key parameters or materials of the IBC SHJ solar cell structure and test the outcome experimentally in a short period of time. The works cited above have also shown that IBC SHJ solar cells built with mask based process are capable of achieving efficiencies close to 24 %. However a consistent study of efficiency limiting factors specifically introduced by mask based patterning techniques is lacking. This additionally incentivised the development of a mask based process. The comparison of the photolithography and the shadow mask based process, both relying on the same vertical layer stack but differing drastically in terms of the horizontal patterning dimensions, will allow to identify the fundamental limitations introduced by the masking approach.

Process Sequence

The wafers are prepared as described in subsection 4.2.2, including a single RCA clean and one HF-dip before the initial deposition. The deposition sequence then should be as follows: deposition of the standard front side (see section 4.2.3, without protective

a-Si layer), unloading from the PECVD tool and flipping of the substrates in order to deposit their rear side, full-area deposition of an intrinsic a-Si:H passivation layer, unloading and applying the BSF mask, deposition of the BSF layer through the mask, unloading and applying the emitter mask, deposition of the emitter layer through the mask. Since the unloading and mask application steps can be done in less than a minute, additional HF-dips should not be necessary (and not possible, as they would also etch the unprotected front side SiN_X layer; alternatively the ARC is deposited in the very end). The entire deposition sequence can be completed in one day, resulting in a cell precursor with a completed front side and patterned emitter/BSF layers on the rear side. The equivalent precursor processed using photolithography requires two separate deposition respectively patterning processes and an additional RCA clean in-between. To maintain an industrially compatible process, the subsequent metallisation process involves a full-area TCO sputter process followed by the screen printing of a silver paste. The latter then acts as an etching mask to pattern the underlying TCO with hydrochloric acid, which neither affects the front side SiN_X layer nor the screen-printed silver layer (with respect to the concentration and time scale needed for the TCO etching). The process sequence is visualised in Figure 4.12.

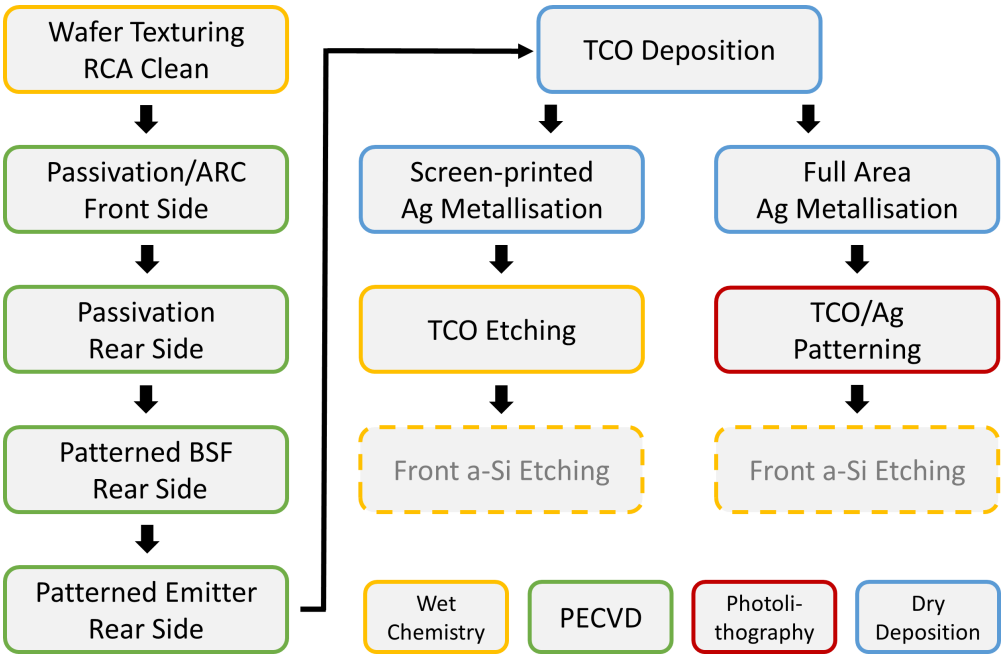


Figure 4.12: Process sequence of the shadow mask process, including an alternative metallisation scheme based on a photolithography process (see section 4.3.5). Front a-Si deposition and etching is only necessary if an HF-dip between the last a-Si:H deposition and the TCO deposition is required.

The following subchapters will describe and discuss the steps that were conducted to realise the process sequence outlined above. These steps include the manufacturing and design of masks by laser patterning, the development of a reliable alignment procedure, the adjustment of the PECVD processes and subsequent thin film analysis and the design of a functioning metallisation scheme.

4.3.1 Laser Ablation of Silicon

The shadow masks used in the PECVD processes to in-situ pattern emitter and BSF layers are made of crystalline silicon. Having both the cell wafer and the mask consist of the same material ensures minimal disturbance of the PECVD plasma and marginal contamination of the wafer's surface as well as an identical level of thermal expansion of cell and mask wafer during the process. Furthermore, c-Si wafers featuring a variety of surfaces and thicknesses were available in large numbers.

Laser ablation is used to cut the emitter and BSF structures into the silicon wafers. To locally ablate silicon material from a wafer, pulsed laser light (see subsection 4.1.3) is focused on the wafer's surface. The energy of the absorbed laser photons leads to a rapid increase of surface temperature, as thermal conduction is a process too slow to distribute the thermal energy within the bulk of the material. As a consequence, the heated surface evaporates abruptly.

The amount of energy that is absorbed by the silicon wafer, and thus the ablation efficiency, depends on the optical properties of its surface. Polished wafers reflect more laser light than randomly etched or textured ones. In case of laser drilling a hole into a wafer or cutting off its edges, the thickness of the respective wafer plays a crucial role. However, the amount of repetitions of single laser scribes necessary to cut through a wafer do not linearly depend on its thickness. Since it is not possible to refocus the laser beam during the laser ablating process, the laser spot will lose focus as more material is ablated from the silicon wafer. Furthermore the laser-induced evaporation of silicon material leads to the formation of dust-like amorphous silicon particles that are deposited around the ablation area. These particles can optically interfere with laser light by reflection or diffraction.

Alongside these laser ablation related considerations, the mask must exhibit a sufficient amount of mechanical stability that allows quick manual handling. At the same time, the masks should be as thin as possible, to reduce tapering effects at the edges of the deposited finger structures (see subsection 4.3.3).

Mask-wafer Preparation Czochralski wafers in as-cut condition with a thickness of roughly 150 μm proved to be suitable for the manufacturing of the masks. The

amount of necessary laser scribes (14) is comparably low (more than 40 are needed for wafers with an average thickness of 250 μm). The mechanical stability is sufficient, as the wafer size and cell area are limited to 4″ and 4 cm^2, respectively, resulting in free standing finger structures with a maximum length of 2 cm (1 cm for the majority of cells featuring a cell area of 1 cm^2).

Cell-wafer Preparation Cell wafers were prepared according to subsection 4.2.2, with the exception of an additional laser ablation step before the initial RCA clean. In this laser step, either holes or edges are cut into the corresponding wafer to allow a proper alignment between the masks and the cell wafers during the subsequent PEVCD processes.

4.3.2 Mask Layout

The mask layout resembles the one of the photolithography masks in terms of the cell arrangement and the corresponding cell areas. This ensures the compatibility of the measurement equipment and increases the comparability of the two approaches. However, in contrast to the photolithography process, where the masks consist of a thick glass plate coated with an opaque chromium pattern, the silicon hard masks are formed after the respective emitter and BSF patterns. Thus mechanical stability is a major factor limiting the possible dimensions of the contact geometry. To increase the overall stability and also decrease the manufacturing time for each mask, the amount of cells was reduced to 8 (from the former 14). Further, the minimum possible width for free standing silicon fingers with a length of 1 to 2 cm was found to be approximately 500 μm. Consequently the width of the BSF contact was set to 500 μm, and the one of the emitter contact to 1.2 mm, resulting in a pitch of 1.7 mm. Compared to the photolithography masks, the pitch is increased by 500 μm (42 %), but the emitter coverage remains in a similar range. Figure 4.13 contains a schematic of the mask and cell layout and a photograph of an emitter mask.

Overlap formation Owing to the inherent constant offset of the laser tool, the real world dimensions of the silicon masks differ slightly from the design values. The mask openings representing both the emitter and the BSF fingers are roughly 60 μm wider than originally intended. As a consequence, without taking underdeposition effects into account and assuming perfect alignment, the formation of a symmetrical overlap with a width of 30 μm is expected. The layer thickness in the overlap region varies as it depends on the extent of tapering effects at the edges of the contact fingers (see subsection 4.3.3).

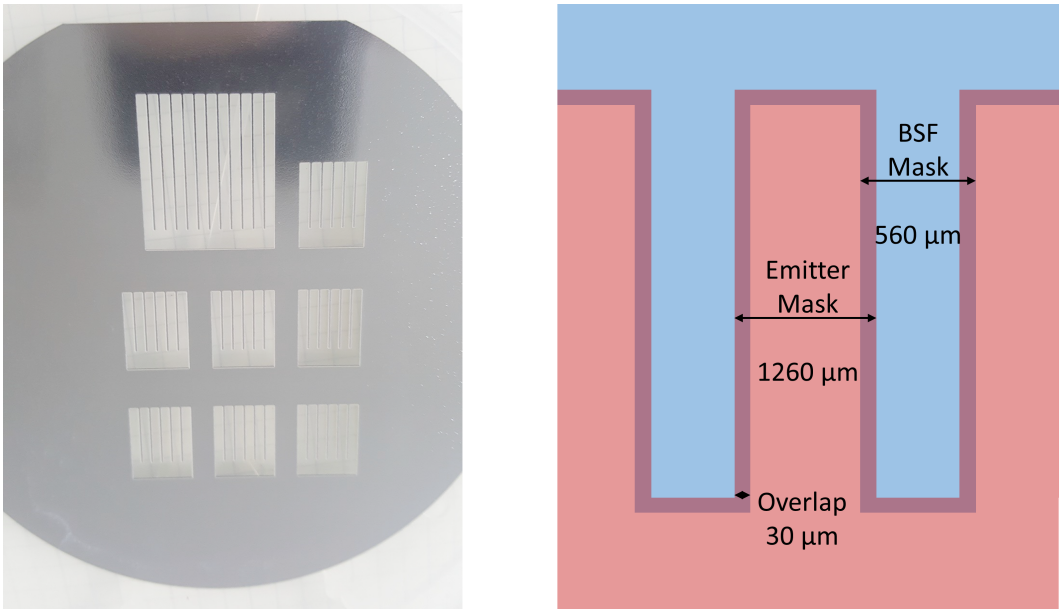


Figure 4.13: (Left) Photograph of an emitter mask featuring openings with a width of 1260 μm [141]. (Right) Schematic of the mask layout: the corresponding BSF mask's openings have a width of 560 μm, resulting in a symmetrical design overlap of 30 μm.

Thermal stability Together with the cell wafers, the silicon masks are exposed to rapid temperature gradients during the PECVD processes (from room temperature to 200 °C in less than a minute, under vacuum conditions). Initial tests showed that laser-structured silicon masks immediately break when put into the PECVD process chamber without precautions. During the laser-ablation process, parts of the silicon wafer close to the edges of the corresponding cell structures will experience a rapid amorphisation, inducing stress in the crystal lattice, in the worst case leading to wafer breakage due to the incorporation of large amounts of defects and dislocations [142]. It is assumed that the presence of the internal tensions in combination with the rapid input of external thermal energy leads to the breakage of the mask in the PECVD chamber. To counter this effect, prior to the initial PECVD process the silicon masks were slowly heated up to 600 °C on a hotplate (in steps of 50 °C with a dwell time of three minutes). Afterwards, to remove dust and other contaminants from the surface, the masks are dipped into a bath of hydrofluoric acid (HF 1 % in H_2O) for 60 s.

4.3.3 Thin Film Analysis

Incorporating silicon masks into the PECVD process of depositing amorphous or nanocrystalline silicon layers onto a crystalline silicon wafer (or another thin amorphous layer) will not only impact the film's thickness but also requires proper analysis of the resulting profile. This is a particularly challenging task as the magnitude of the vertical

dimension (the thickness) is in the range of tens of nanometres while the one of the horizontal dimension (the profile) is in the range of a a couple of hundreds micrometers (up to millimetres, if more than one contact finger is analysed). The thickness of amorphous silicon layers can be determined by spectral ellipsometry or atomic force microscopy (AFM). Transmission electron microscopy is another accurate but also time-consuming method. All these methods lack the capability of spatially resolving the measurements in an accurate and convenient way. While stylus profilometry is suited to measure longer distances in the range of several hundred micrometers and more, the resolution of the available setups was not sufficient in order to obtain results with a high enough signal to noise ratio.

The Raman method described in subsection 3.2.8 allows to measure both the profile, over a distance of several millimetres, and the thickness with a nanometre-resolution.

Deposition under the Mask

The silicon layer growth in a PECVD process can be roughly described as follows: SiH_3 radicals are generated from the SiH_4 plasma; these radicals are then transported to the substrate's surface. This surface will for the most part be passivated by hydrogen, since the substrate was treated with hydrofluoric acid (HF) before the process and attached precursor molecules are also saturated with hydrogen. Silicon film growth, however, only happens, if the incoming SiH_3 radicals bond to dangling silicon bonds from the surface. At higher temperatures (>350 °C), two neighbouring hydrogen atoms might spontaneously recombine and desorb from the surface leaving two silicon dangling bonds behind. At the temperatures the PECVD processes used for this work operated (around 200 °C), this is not expected to be the dominating procedure. If the SiH_3 radicals are not immediately chemisorbed by silicon dangling bonds the radicals will diffuse on the H-passivated surface until they either form Si-Si-bonds or recombine with an H-atom, forming SiH_4 again and desorb. The latter case still contributes to the film growth, as the SiH_3 radical extracts a hydrogen atom from the surface allowing another SiH_3 radical to form an Si-Si bond with the remaining silicon dangling bond [143].

For a functioning in-situ PECVD patterning process, it is important to keep the diffusion length of the SiH_3 radicals on the substrate's surface as small as possible, as otherwise they might diffuse under the mask, thus depositing amorphous silicon in masked areas. It was observed that the extent of this undesired deposition depends on the process parameters, which were different on the PECVD tools used here (see subsection 4.1.1). PECVD processes exhibiting high gas flows (AKT and initial Altatech processes) showed a good fidelity between the mask and resulting a-Si:H layers, while processes with lower gas flows (reworked Altatech processes) lead to washed-out a-Si:H

patterns owing to strong underdeposition. It is assumed that by increasing the gas flow (and keeping the remaining process parameters more or less constant) the deposition process is limited by the diffusion of SiH_3 radicals towards the surface, thus restricting the amount of unbound SiH_3 radicals on the substrate's surface that are able to diffuse under the mask [77]. Therefore the amount of underdeposition is kept at a reasonable level.

Figure 4.14 a shows two separate normalised profile measurements in the same graph - the mask widths of the corresponding fingers, 1260 μm for the p- and 560 μm for the n-contact, are indicated as well. Due to underdeposition effects, the intentional overlap of 30 μm increases to values of above 100 μm. Since these layers were already processed with high gas flows, a further improvement would require a redesign of at least one of the masks. Figure 4.14 b contrasts the profile of mask-patterned a-Si:H layer with the one patterned by photolithography. The extent of the underdeposition as well as the tapering effect reducing the thickness of the mask-patterned layer is clearly visible. In Figure 4.15 a an example of a p-structure processed with a low gas flow is shown: the underdeposition results in a continuous amorphous silicon layer with a modulated thickness induced by the mask. In-between the finger structures, the thickness of the p-type a-Si:H layer exceeds 10 % of the layer's maximum thickness.

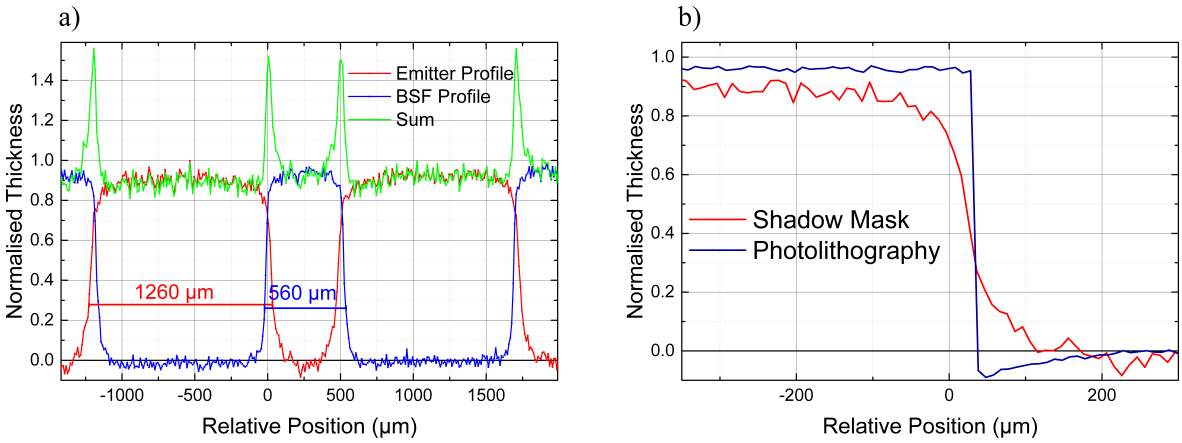


Figure 4.14: a) Separate Raman profile measurements of emitter and BSF structures, with a normalised thickness. Overlap and underdeposition effects are clearly visible, leading to thickness spikes in the overlap area (sum graph). b) Comparison of edges created with photolithography and shadow masking.

The polarity of the substrate seems to have an influence on the extent of underdeposition as well. Figure 4.15 b shows the Raman profile of an emitter finger (p-type a-Si:H) deposited onto a p-type c-Si wafer with a high gas flow process (AKT). The profile is in very good agreement with the mask and virtually no parasitic deposition is measured. As seen in Figure 4.14, n-type a-Si:H fingers on n-type c-Si wafers still

exhibit a measurable amount of underdeposition. Since p-type a-Si:H grows faster than intrinsic or n-type a-Si:H, owing to the catalytic effect of hydroboron (BH_3) radicals [144], a difference with respect to the corresponding diffusion behaviour and thus parasitic deposition effects can be expected. However there is no obvious explanation for the polarity of the substrate to limit the surface diffusivity of the SiH_3 radicals. As PECVD grown nanocrystalline layers, patterned in-situ with masks, show far less underdeposition effects than their amorphous counterparts, a possible explanation is that the p-type a-Si:H process (designed to be deposited on an intrinsic a-Si:H surface) might actually have resulted in epitaxial growth on the p-type c-Si wafer. Since the solar cells presented in this work were exclusively built on n-type c-Si wafers, this phenomenon was not further investigated.

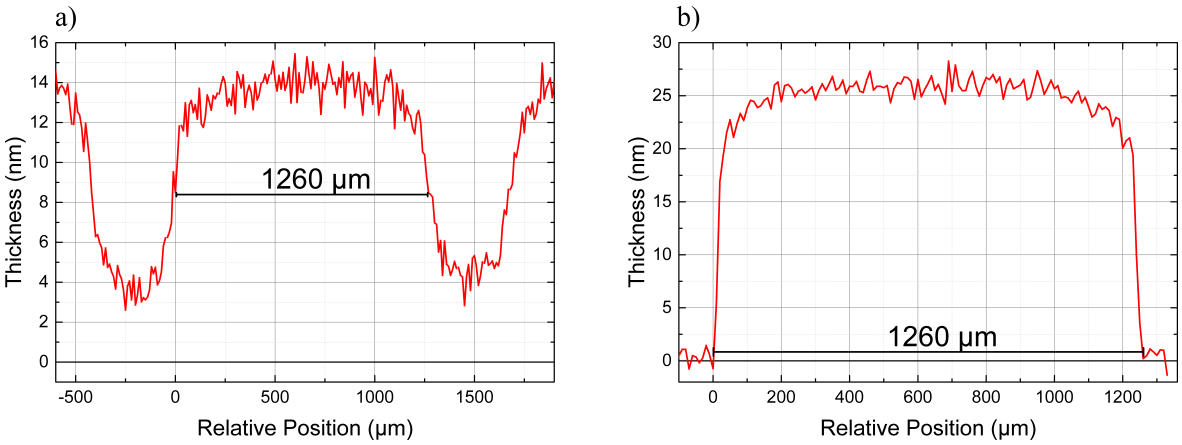


Figure 4.15: a) Deposition of p-type a-Si:H on n-type c-Si with a low gas flow process: severe underdeposition leads to a continuous a-Si:H layer. b) Deposition of p-type a-Si:H on p-type c-Si with a high gas flow process: the deposited structure is in almost perfect agreement with the mask.

Film Thickness

The deposition through masks also affects the thickness of the layer, both its absolute value and its homogeneity. The peak thickness values determined by the Raman method (measured in the middle of the corresponding contact fingers) were roughly 60 % lower compared to layers deposited under the same conditions but without masking (assuming an error of around 3 nm, due to low Raman integration times). Therefore deposition times need to be adjusted accordingly. The tapering in the vicinity of the mask's edges is clearly visible in Figure 4.14. While too thin emitter respectively BSF layers could potentially lead to an insufficient protection of the underlying intrinsic a-Si:H layer during the subsequent sputter processes, the overlap inherent to the mask design and the parasitic underdeposition result in a strongly increased thickness in the overlap region, as the sum graph in Figure 4.14 a indicates.

To sum up, the thin film analysis by Raman profile measurements revealed that for high gas flow PECVD processes the mask-based in-situ patterning yields suitable results. Undesired underdeposition is a notable issue, especially for low gas flow PECVD processes, but remains significant for high gas flow processes as well. To counter the unintended increase of the overlap width from a design value of 30 μm up to well above 100 μm, the mask design has to be altered. A reduction of the emitter finger width by roughly 150 μm might already be sufficient.

4.3.4 Alignment Procedures

The accuracy of the respective alignment method directly influences the design considerations with respect to the rear side geometry. Alongside the accuracy of the mask-based PECVD in-situ patterning, discussed in the previous section, it represents another factor limiting the possible minimum feature size. While the alignment accuracy of the photolithography process is in the range of a few micrometres, owing to the use of optical microscopy and remote-controlled moving stations, a similar level of accuracy is difficult to realise for a silicon mask based process. In contrast to the photolithography process, the available time to align the second mask on the structure based on the first mask constitutes a limiting factor, as the subsequent PECVD process requires an oxide-free surface (and further HF-dips should be avoided). Simplicity, ease of application and reproducibility are therefore major requirements that at the same time potentially restrict the alignment accuracy.

Any alignment procedure capable of holding the cell wafer and the corresponding mask at fixed positions in a PECVD tool not necessarily built for this particular application involves the manufacturing of custom substrate carriers. During the development of the shadow mask process, two carrier-based alignment methods were evaluated.

Edge Method

The edge method is based on aligning wafer edges orthogonal to each other to a milled-out step in a custom-made aluminium carrier, shown in Figure 4.16. In an initial step, two edges in a 90 ° angle are laser-cut into both the mask and the corresponding cell wafers. These edges then act as a reference for the subsequent cell structures. Before loading into the PECVD loadlock, both the cell wafer and the mask on top are pushed towards one corner of the custom carrier, ideally resulting in their respective edges being aligned to each other (visualised in Figure 4.17).

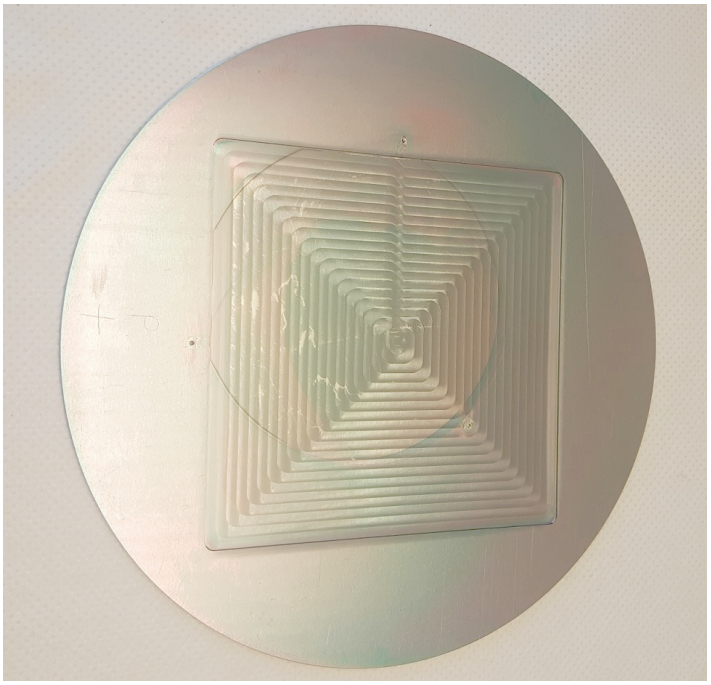


Figure 4.16: Custom made aluminium carrier featuring a milled-out square; its edges serve as a reference in order to align cell and mask wafer [141].

Initial tests revealed that micrometre-scale gaps between the carrier edge and the wafer edges, vibrations originating from the vacuum pumps of the PECVD system, and the difference in thermal expansion between aluminium and silicon resulted in rather large alignment inaccuracies (see Figure 4.18 a). To prevent the system's vibrations from moving the wafers during the process, the cell wafer/mask stack was weighted with pieces of glass. As this turned out to be insufficient, the custom carrier was modified by adding three steel clamps screwed around the wafer area, pressing cell wafer and mask down onto the carrier and thus keeping both in one place. As Figure 4.18 b shows, it was then possible to achieve an adequate alignment accuracy, however at the expense of drastically complicating the mask application. Further tests revealed a poor reproducibility of the result shown in Figure 4.18 b, likely related to the complex manual handling of pushing the cell wafer/mask stack perfectly towards the carrier's edge and at the same time tightening the clamps without moving neither cell wafer nor mask. Furthermore, the difference in thermal expansion remains an issue, as aluminium's thermal expansion coefficient is almost ten times higher than the one of silicon. A temperature increase of 250 K (representing an upper temperature limit for common a-Si:H PECVD processes) results in the expansion of a silicon wafer with a nominal diameter of 10 cm by approximately 60 μm, while the same distance in aluminium expands by roughly 550 μm. Even if only a fraction of this discrepancy contributes to

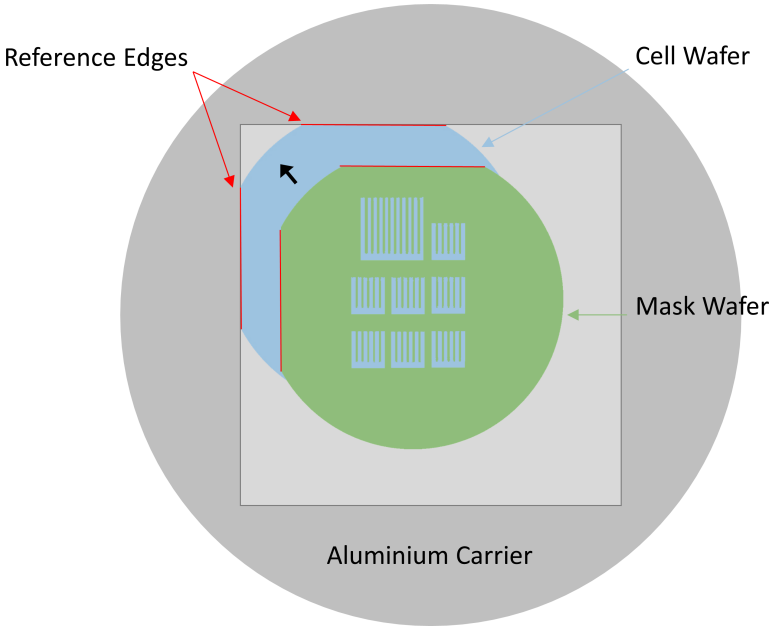


Figure 4.17: Edge alignment method: both cell and mask wafer are pushed towards the reference edges of the custom aluminium carrier.

the alignment inaccuracy, a mask design aiming for an overlap width of 30 μm is thus difficult to implement.

Pin-to-Hole Method

The pin-to-hole method is based on laser-cutting two holes into the cell as well as the mask wafers and using pins passing through these holes to align both on top of each other. The pins are made of stainless steel and are fixed to a customised aluminium carrier.

The steel pins feature a diameter of 2 mm with an inherent inaccuracy of 10 μm. Their height of 700 μm (600 μm fully cylindrical, 100 μm rounded cap) is well above the sum of the thicknesses of cell and mask wafers (typically 250 μm for cell wafers and 150 μm for mask wafers) minimising the risk of the mask sliding off of one or both of the pins.

The diameter of the pin holes in the corresponding wafers was set to be 10 μm larger than the one of the pins themselves. Although this difference contributes to the inaccuracy of the alignment method, it is necessary to limit the amount of mechanical strain the wafers are exposed to during manual handling. The laser-cutting of holes into the wafers makes them more fragile, thus any mechanical strain increases the probability of wafer breakage during subsequent processing steps. Since the presence of one fully circular hole ensures that the respective wafers can only be displaced by rotating around that pin, the hole for the second pin only needs to limit the wafer's movement in the

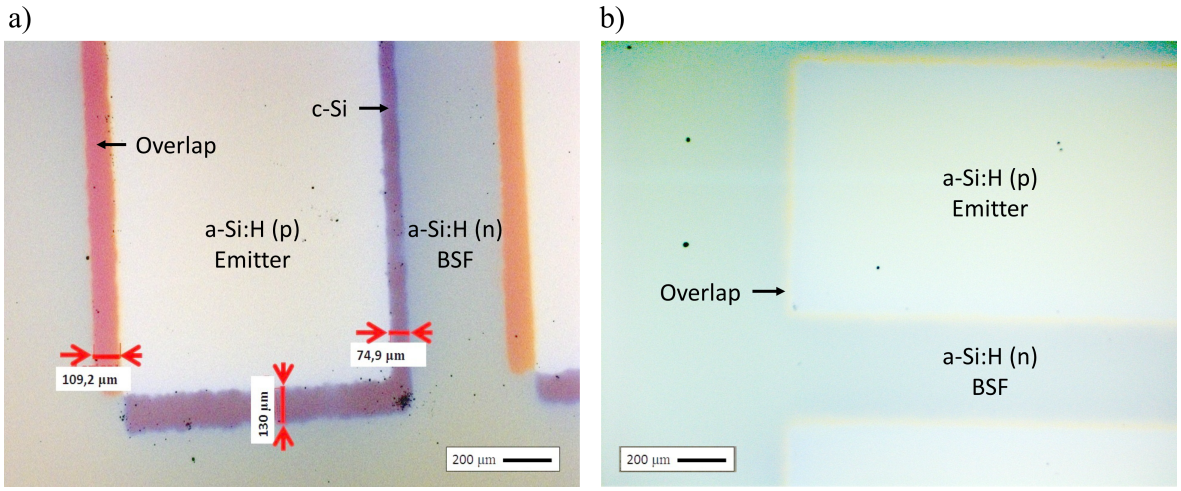


Figure 4.18: a) Severely misaligned emitter and BSF test structures, revealing the underlying c-Si wafer. b) Well aligned emitter and BSF structures featuring a symmetric, visible overlap of around 30 μm [141].

direction perpendicular to the axis formed by connecting the two pins (see Figure 4.19). Along this axis the second hole can be extended resulting in an oblong shape. The distance between the centre of the two holes is 82 mm, enabling the use of 4″ wafers.

Thermal expansion As stated in the previous section, the use of different materials featuring drastically different thermal expansion coefficients potentially contributes to the inaccuracy of the corresponding alignment method. Analogous to the consideration for the edge method, a PECVD process related temperature increase by 250 K is assumed. The diameter of the holes increases by roughly 1 μm, the one of the pins by 5 μm. Since the initial spacing between pin and hole is set to 10 μm, the stronger expansion of the pin does in fact reduce the inaccuracy of the alignment method without breaking the wafers (it still prolongs the time needed to switch masks, as the whole arrangement of carrier with pins and stacked cell and mask wafers needs to cool down before the wafers can be removed without the risk of breaking either wafer or mask). The expansion of the entire aluminium carrier leads to an increase of the distance between the two pins by approximately 500 μm. Although this is partly compensated by the distance between the holes on the wafers increasing by 50 μm, the oblong shaped hole has to be designed accordingly. Figure 4.20 shows the position of the pin within the oblong hole at room temperature and at an elevated temperature, with the thermal expansion effect being clearly visible.

In contrast to the edge method, the strong difference in thermal expansion between silicon and aluminium does not impact the alignment inaccuracy of the pin-to-hole method, as the relative position of cell and mask wafer to each other remains the same,

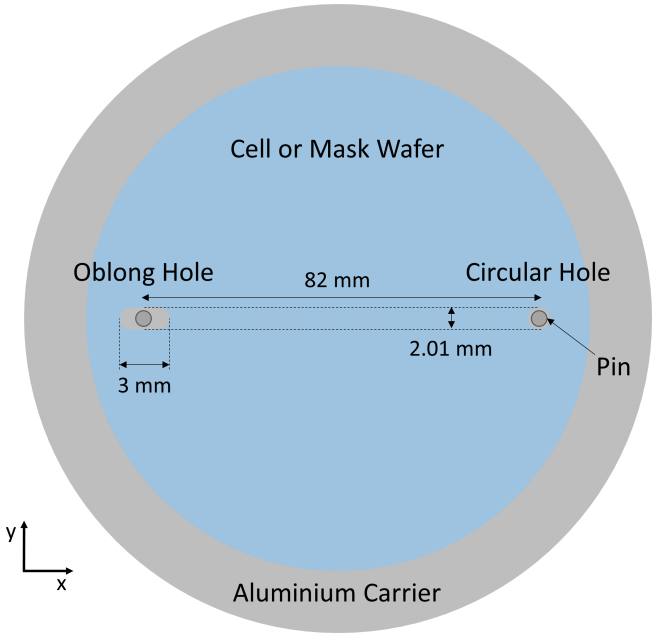


Figure 4.19: Schematic of the pin based alignment system: the pin in the circular hole prevents the wafer from moving in the x- or y-direction, while the pin in the oblong hole prevents rotational movement. The diameter of the pins is 2 mm.

and the expansion of the aluminium carrier is neutralised by the oblong shaped hole. Since cell wafers and masks are both made of crystalline silicon, a potential difference in thermal expansion is expected to be negligible. Figure 4.21 visualises the extent of inaccuracy arising from the considerations outlined above.

Laser-induced inaccuracy While the position of the laser beam can be set with an accuracy of roughly 1 μm, the laser process still contributes to the overall inaccuracy of the alignment method. Since the laser beam's width is 10 μm, the silicon's exact rupture point varies within an interval of +/- 5 μm (as the laser beam profile is Gaussian, a rupture point towards the middle of the beam is still expected to have a higher probability). The variance in energy dissipation on the wafer is further exacerbated by the different surface conditions of cell and mask wafers: the former are either textured or polished, while the latter are usually as-cut. Polished and as-cut wafers will reflect more light than textured ones, while for the latter the increased amount of absorbed energy affects larger areas due to enhanced scattering effects. As a consequence, the diameter of the laser cut holes may vary within a few micrometres despite identical laser process parameters. This is significant, as the tolerance between the pin and pin hole is set to be only 10 μm, and it decreases further at elevated temperatures. With an average of 8 μm this value tends to be slightly smaller than the design value for cell wafers, while mask wafers exhibit the opposite with average values of 15 μm. This

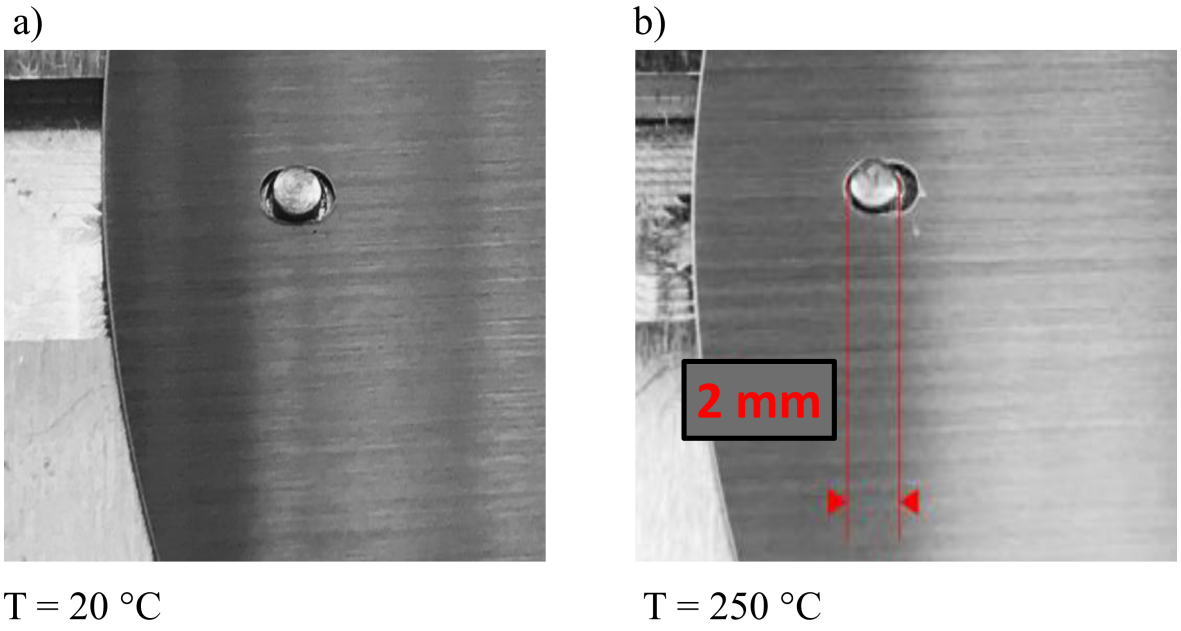


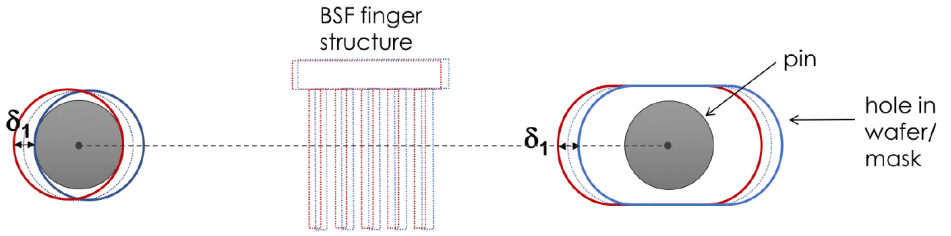
Figure 4.20: Thermally induced movement of the alignment pin in the oblong hole in a wafer [145].

difference contributes to the overall alignment inaccuracy as the tolerance around the pins is substantially greater for the mask wafers.

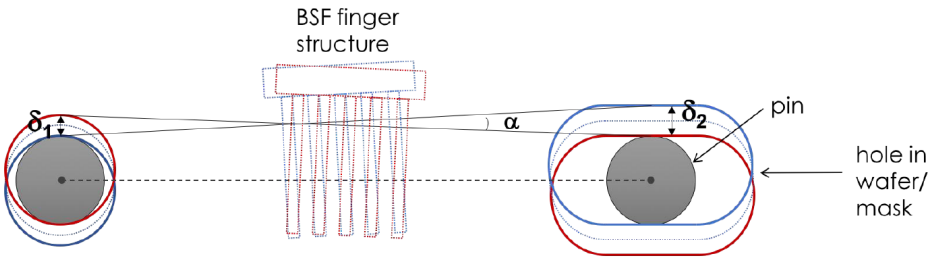
Experimental results Compared to the edge method, the pin-to-hole method yields very reproducible results. With optical microscopy the width of the (visible) overlap area was determined to be around 30 to 40 μm, well within the expected range and on par with the best results achieved with the edge method. Figure 4.22 shows a PL image of a cell precursor patterned with the shadow mask process. In contrast to the PL images depicted in the photolithography process section, there are much more marks at the edges of the wafer arising from the increased amount of manual handling and the laser-cut holes. The masks themselves do not seem to have a negative impact on the passivation, as the cell area and their close surrounding are well passivated.

4.3.5 Contact Formation

While it would be desirable to pattern both the TCO and the metallisation in-situ, this is particularly difficult for the former. TCO materials are usually deposited using sputter processes that tend to exhibit strong tapering and underdeposition effects when in-situ masking is used. Furthermore the carriers in the available sputter tools (see section 4.1.2) consisted of either silicon or glass, which complicated the introduction of an alignment method comparable to the ones described in the previous section. Hence



(a) Shift



(b) Tilt

Figure 4.21: Visualisation of the maximum inaccuracy of the pin-to-hole alignment: the inaccuracy in x- any y-direction is determined by δ_1, the maximum angular inaccuracy α_{max} by the arctangent of δ_2/d (if $\delta_2 > \delta_1$ and d equals the distance of the pins). Assuming the design values $\delta_1 = \delta_2 = 10\,\mu$m and $d = 82\,$mm α_{max} equals 0.007° [145].

TCO layers were deposited full-area and etched afterwards with the subsequent metal or other additional layers acting as an etch mask.

Screen Printing of Metallisation Layers

Screen printing allows the deposition of in-situ patterned metal layers on large areas. It is therefore the method of choice for industry-compatible manufacturing processes.

The screen designed for this particular process features different nominal metallisation gap widths ranging from 200 μm up to 600 μm. These values exceed their photolithography equivalent (30 μm) by far, owing to the difference in emitter/BSF layer overlap width between the two manufacturing methods (15 μm for the photolithography process and at least 30 μm, likely up to 100 μm if underdeposition effects are considered, for the shadow mask based process). Furthermore, the eventual metallisation gap width is also influenced by the expansion of the silver paste during the thermal curing process following the screen printing deposition. Depending on the type of paste, the width of the corresponding metal fingers is expected to increase by up to 40 μm, resulting in a minimum metallisation gap width of roughly 160 μm. Silver pastes do not only differ with respect to their expansion coefficients but also in their respective porosity. Since

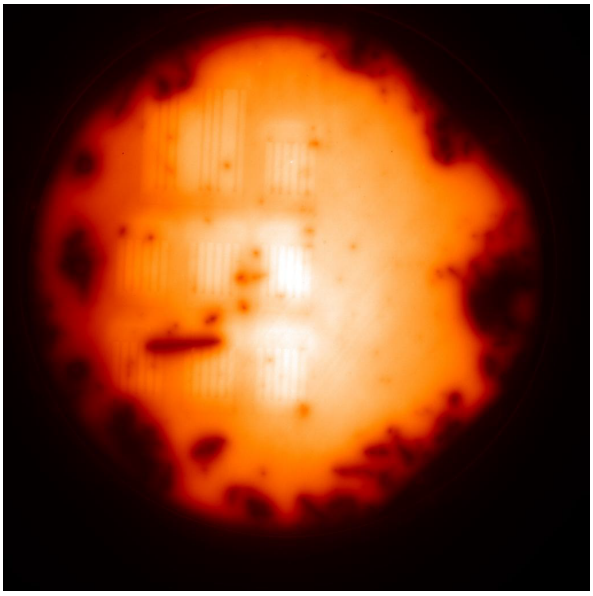


Figure 4.22: PL image of cell precursor structured with the shadow mask process. The masks do not have a negative impact on the passivation of the cell area and the immediate surroundings. However, the laser-cut holes and manual handling result in dark spots at the wafer's edges.

the silver layer has to serve as etching mask during the wet-chemical etching process of the underlying TCO layer, it is vital that the paste fully covers the entire contact area.

It is also possible to deposit the metal layer full-area and subsequently screen print an organic resist layer serving as an etch-mask for both the TCO and the metallisation. This method is advantageous if thinner, but denser and more homogeneous metal layers are preferred, or the available metals pastes do not meet the requirements in terms of adhesion, conductivity, expansion and porosity. It would also enable the use of an aluminium metallisation as there are no low-temperature aluminium pastes available. On the other hand, it increases the complexity of the overall metallisation process, as, alongside the obligatory TCO etching process, both the etching of the metal layer and the eventual removal of the resist layer are based on wet-chemical processes.

Alignment The initially developed procedure to align the screen-printed metallisation with the emitter/BSF patterns resembles the one outlined in section 4.3.4. The camera of the screen-printing system detects the two edges of the wafer serving as a reference for the positioning of the metallisation pattern. Non-ideal wafer edges, as they usually exhibit a certain roughness, and the camera's difficulties in reliably focusing the top and not the bottom edge of the respective wafer result in inherent inaccuracies of this particular alignment method. As a consequence, offset values have to be defined in an initial calibration procedure prior to each screen-printing process sequence. The offset

values are determined by evaluating the position of the metal layer screen printed onto test samples with respect to the emitter/BSF structures. Although actual cell wafer samples could serve as test samples, since just printed paste can easily be removed again, dedicated test wafers are necessary, as the TCO layer on the cell wafer samples obscures the emitter/BSF pattern when analysed by optical microscopy.

As Figure 4.23 a shows, it is possible to deposit well aligned silver layers with screen printing and the aforementioned alignment method. However, the paste used in this example is very porous leading to a high surface roughness and also potentially causing parasitic etching through holes. Furthermore, insufficient adhesion of the paste was a common occurrence (see Figure 4.23 b).

Organic resist printing was evaluated on test samples yielding promising results in terms of layer stability in the corresponding etching solutions. The process needs further optimisation with respect to adhesion problems due to the high viscosity of the organic paste and difficulties in removing the resist layer after etching.

The alignment approach outlined above is neither suited for research nor for industry processes. Within the course of the development of the pin-to-hole alignment method (see section 4.3.4), additional laser-cut holes were added to the mask design, which are expected to be reliably detected by the camera setup of the screen printing system. In this case, initial calibration steps determining offset values by using test samples could be avoided, increasing the accuracy and reproducibility of the alignment procedure.

There are no fundamental issues preventing the introduction of a high quality screen-printing process to metallise mask-based patterned IBC SHJ cell precursors. However further optimisation efforts were postponed in favour of a complementary method.

Pseudo-Photolithography

The pseudo-photolithography method combines the photoresist layer preparation and patterning outlined in section 4.2 with the pin-to-hole alignment method described in section 4.3.4. TCO and metal layers are deposited full-area onto the mask-based patterned rear side, followed by the deposition of a negative photoresist layer by spin coating. Instead of illuminating the photoresist through glass-based masks mounted into the mask aligner, laser-structured silicon wafers are used as masks. These masks resemble the emitter and BSF deposition masks, but are modified with respect to their dimensions: larger silicon finger widths resulting in narrower gaps. During the light exposure, the metallised cell wafer coated with the negative photoresist layer and one of the two masks are placed onto the corresponding custom carrier providing the pin-based alignment. In the subsequent exposure step only the photoresist on the respective

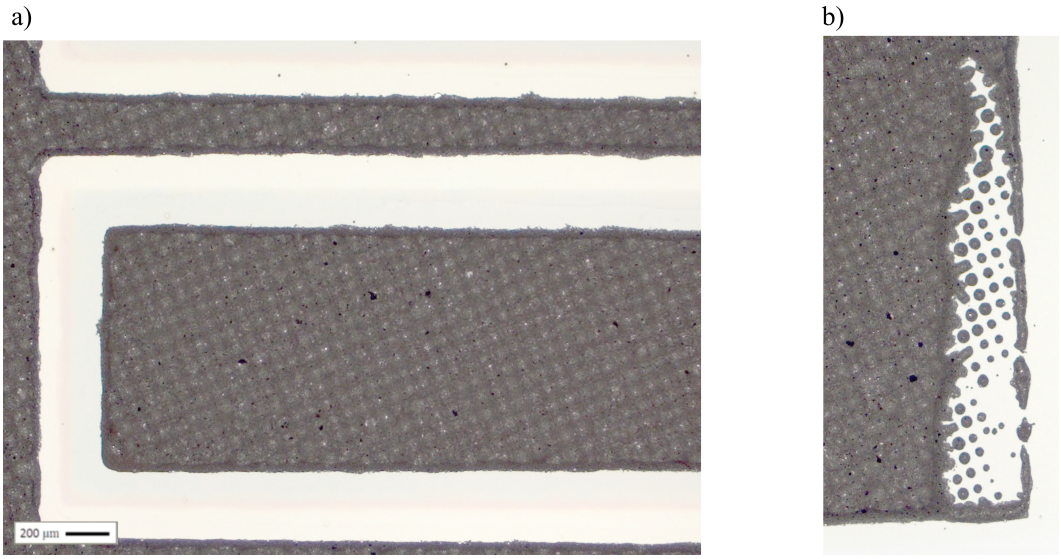


Figure 4.23: a) Accurately aligned screen-printed metallisation layer b) Poor adhesion of the screen-printed layer

contact finger/busbar is hardened by the UV light. The process is repeated with the other mask and the photoresist is developed afterwards. The result is a photoresist layer protecting emitter and BSF regions and the corresponding busbars but revealing a metallisation gap in-between. The extent of this gap is determined by the modification of the silicon finger width on the respective masks. Figure 4.24 shows a schematic of both masks stacked on-top of each other and thus indicating the gap region being shaded in both exposure steps.

After the development of the photoresist, silver and TCO layers are etched analogously to the procedure described in section 4.2.3. The photoresist layer is then stripped in acetone, isopropyl alcohol and deionised water.

The pseudo-photolithography approach can be regarded as a place-holder process for an optimised screen-printing method. Since the influence of the emitter and BSF patterning on the performance is of greater interest than the one of different metallisation schemes, it is furthermore favourable to use a patterning process that is very similar to the photolithography based one, at least in the initial stages of the process development. Moreover, in contrast to the screens for the screen-printing process, equivalent silicon metallisation masks can be manufactured in-house, making design changes and adjustments much easier.

4.3.6 Final Steps

Since the time period between the deposition of the a-Si:H layers and the subsequent TCO deposition was comparably long, samples were usually treated with hydrofluoric

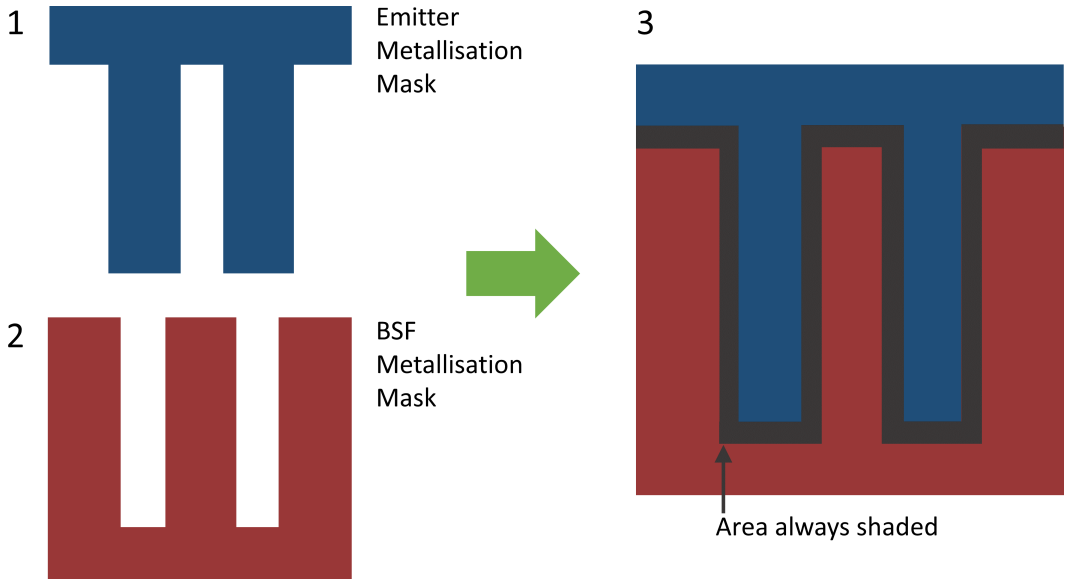


Figure 4.24: Two-step exposure: the negative photoresist layer is illuminated through the BSF, then the emitter metallisation mask (or vice versa). The corresponding finger widths are chosen so that the eventual metallisation gap region is shaded in both exposure steps.

acid before the TCO deposition to remove any native oxide. Consequently the solar cell's front side had to be protected with an amorphous silicon layer, analogous to the photolithography process. The finalisation process is thus identical to the one described in subsection 4.2.4. A completed cell manufactured with the shadow mask process is depicted in Figure 4.25.

4.4 Chapter Summary

In this chapter two manufacturing methods for IBC SHJ solar cells are presented. The first part describes the established *photolithography process* in detail and outlines the key improvements made during the course of this work: improved photoresist adhesion by introducing a mandatory HF-dip before photoresist deposition; omitting silver sputtering in order to avoid the partial crystallisation of the underlying ITO layers thus ensuring homogeneous etch rates for the latter; using alkaline etchants for the removal of the protective front side a-Si layer to prevent damage to the front SiN_X layer and preserve the passivation capabilities of the front side layer stack. The *photolithography process* yields accurately patterned layers, with minimum feature sizes of about 5 to 10 μm and corresponding solar cells have achieved efficiencies up to 23.2 % (see Figure 4.26). Owing to the amount process steps, resulting in long process times and the required quantities of wet chemicals (photoresist, solutions for multiple cleaning

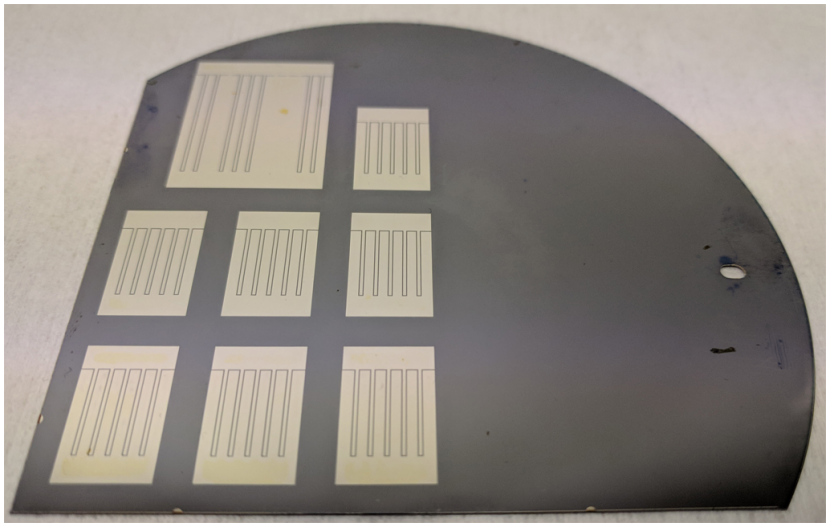


Figure 4.25: Photograph of the planar rear side of a finished wafer with IBC SHJ solar cells, manufactured with the shadow mask process. Left and bottom edges are cut off to fit the wafer into the custom measurement chuck, aligning cell busbars and external contacts. On the right side of the image, the oblong hole used for the alignment procedure is visible.

and etching steps), the *photolithography process* cannot be regarded as industrially viable, but serves as a reference process to explore the efficiency limits of the IBC SHJ technology.

To provide an industrially viable approach to IBC SHJ solar cell manufacturing, the second part of the chapter describes the development of a manufacturing process based on the in-situ patterning of PECVD deposited a-Si:H layers with *shadow masks*. The shadow masks consist of crystalline silicon wafers, the respective mask patterns are cut into the wafers by laser ablation. The minimum feature size of the *shadow mask process* is roughly two orders of magnitude higher than the one of the *photolithography process*, owing to stability requirements of the masks, unintentional a-Si deposition in masked areas during the PECVD process (underdeposition) and the limited accuracy of the alignment system. Raman-spectroscopy-based profilometry measurements of the patterned a-Si:H layers revealed that the amount of underdeposition depends on the characteristics of the a-Si:H PECVD process. Deposition processes with high gas flows that presumably are limited by the diffusion of SiH_3 radicals towards the substrate rather than surface diffusion on the substrate exhibit far less underdeposition. To align the second mask on the pattern of the first mask, a system combining steel pins on a custom aluminium carrier and appropriate alignment holes, laser-drilled into both the mask and the cell wafer, was implemented. This pin-to-hole method was found to be sufficient in terms of accuracy and ease to application. With screen printing and a photolithography-like patterning process based on silicon shadow masks as well, two

metallisation approaches are introduced and tested. The latter one excels in terms of accuracy and customisability and thus serves as a placeholder process for the industrially viable, but not yet optimised screen-printing process. First solar cells built with the *photolithography process* achieved efficiencies up to 17 %.

The efficiency progress for both IBC SHJ solar cells built with either manufacturing process is depicted in Figure 4.26.

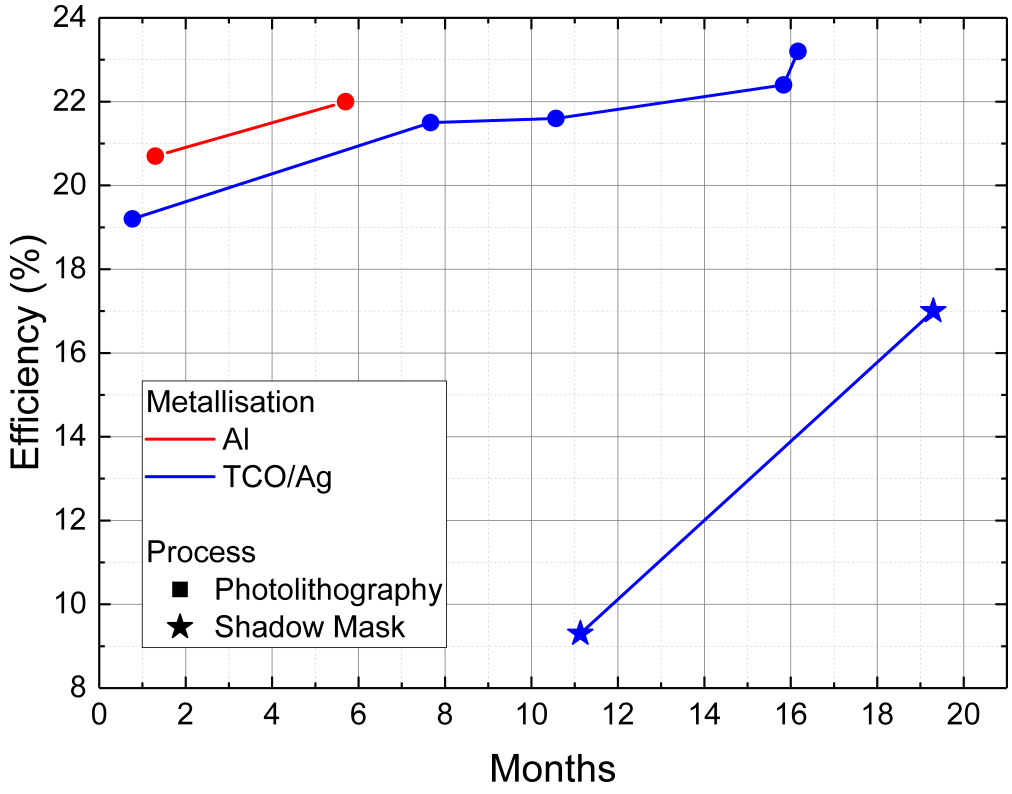


Figure 4.26: Solar cell efficiency increase for different metallisation materials and manufacturing processes.

Chapter 5

Device Optimisation and Analysis

5.1 Introduction

The following chapter outlines the optimisation process of the photolithography-based IBC SHJ solar cells, with a particular emphasis on different contact materials, and moreover presents initial results of the transfer of this optimised design to solar cells built with the shadow mask process. The performance of the solar cells is determined by the following factors: the quality of the passivation, including the front side layer stack and the rear side amorphous silicon layers; the quality of the patterning process with respect to the accuracy (cell design, overlap width, metallisation gap) and the potential degradation of the passivation during the process; the current transport capabilities of the rear side contact stack and metallisation.

The initial section of the chapter, **Characterisation Approach**, comments on the different methods used for characterisation, especially with respect to the analysis of the series resistance.

The second section of the chapter, **Simple Aluminium Contacts**, discusses photolithography-based IBC SHJ solar cells with a direct aluminium metallisation on the amorphous silicon emitter and BSF layers, compared to a reference device with an ITO/Ag metallisation and an otherwise identical layer structure. The respective layer stacks for both the Al and ITO/Ag reference device are shown in Figure 5.1. It is shown that annealed Al/a-Si:H interfaces yield low contact resistivities resulting in FF values of up to 78 % and efficiency values of up to 22 %. Based on photoelectron spectroscopy measurements, simulation studies, and results from literature, the decrease in contact resistivity is explained by the formation of an intermediate silicide phase initiating the partial crystallisation of the a-Si:H layers. Extended annealing leads to a pronounced

interdiffusion of amorphous silicon and aluminium resulting in the disintegration of the a-Si:H layers and deterioration of the underlying passivation layer, which severely affects the V_{OC} of the solar cell. Annealed Al/a-Si:H contacts are therefore characterised by the trade-off between low contact resistivities resulting in high FF values and the necessity to maintain a proper passivation quality in order to avoid the deterioration of the V_{OC}. The results are based on the publications [146] and [147].

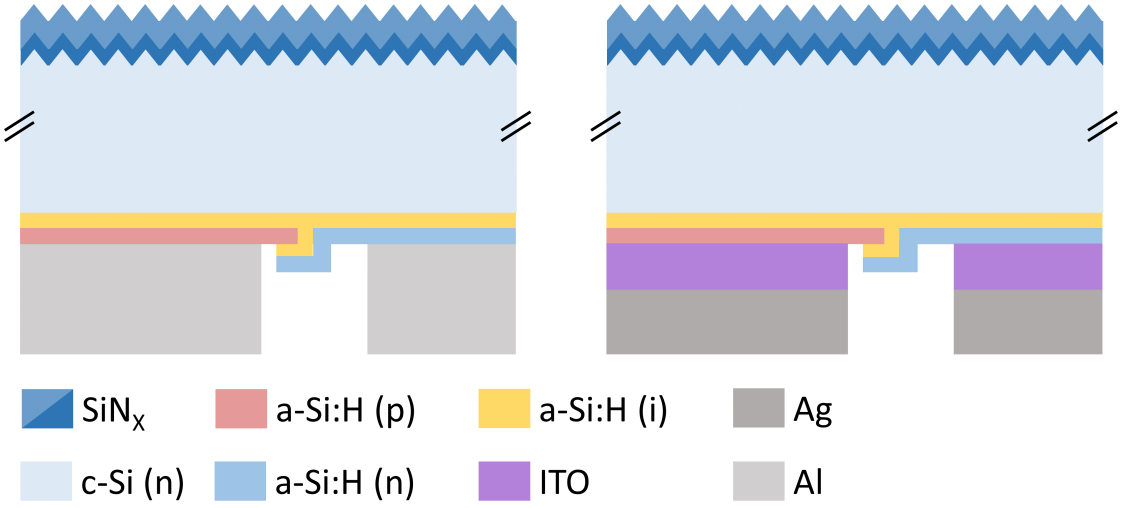


Figure 5.1: Layer stack of the Al (left) and the ITO/Ag reference device (right) - the front side consists of a stack of two SiN_X layers, the two structures differ only with respect to their metallisation: a direct aluminium metallisation versus an ITO/Ag stack.

The third section of the chapter, **Cells with TCO Contacts**, focuses on IBC SHJ solar cells, built with the photolithography process, that feature a TCO-based metallisation. In this section the different measures responsible for improving the efficiency of these solar cells by 4 %abs (from 19.2 to 23.2 %) are described and analysed. These measures are: a new front side layer stack prioritising passivation quality; optimised emitter and BSF layers, resulting in a better rear side passivation and a better contact to the respective TCO material; using a textured rear side to increase the contact area; evaluating the TCO materials aluminium-doped zinc oxide (AZO) and tungsten oxide (WO_X) as an alternative or a complement to indium tin oxide (ITO) and analysing the FF limitations arising from the contact resistivities of both the emitter/TCO and the BSF/TCO contact. The corresponding cell structures are depicted in Figure 5.2. Parts of the data presented in this section have been published in [148].

The final section of the chapter, **Non-Photolithography Solar Cells**, presents and discusses the initial results of IBC SHJ solar cells built with the shadow mask

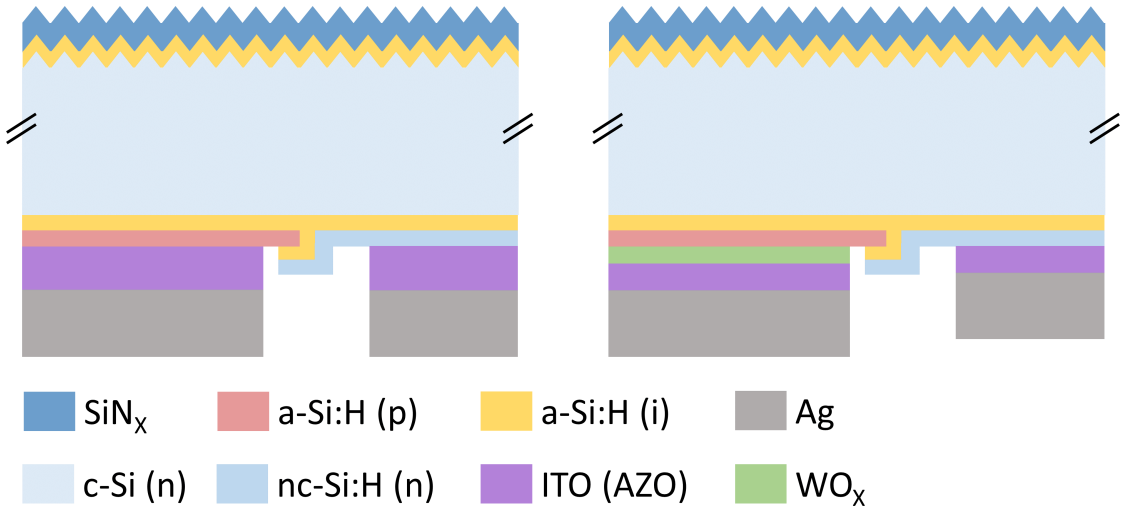


Figure 5.2: Layer stack of the IBC SHJ solar cells featuring an ITO or an AZO contact, respectively (left) or an additional WO_X layer at the p-contact (right). The front side layer stack consists of an intrinsic a-Si:H passivation layer and a SiN_X ARC, the BSF layer of a nanocrystalline Si:H layer.

process outlined in section 4.3.

The different structure variations are also listed and compared in Table 5.1. The emitter layer always consists of p-type a-Si:H, hence it is not mentioned in the table.

Table 5.1: Solar Cell structure variation

Front Side	PECVD	BSF	Metallisation	Rear Side	Process*
2×SiN_X	FAP	a-Si:H (n)	Al	polished	PL
2×SiN_X	FAP	a-Si:H (n)	ITO/Ag	polished	PL
a-Si:H/SiN_X	AKT	nc-Si:H (n)	ITO/Ag	polished	PL
a-Si:H/SiN_X	AKT	nc-Si:H (n)	ITO/Ag	polished	PL
a-Si:H/SiN_X	AKT	nc-Si:H (n)	AZO/Ag	polished	PL
a-Si:H/SiN_X	AKT	nc-Si:H (n)	ITO/Ag	textured	PL
a-Si:H/SiN_X	AKT	nc-Si:H (n)	WO_X/ITO/Ag**	polished	PL
a-Si:H/SiN_X	Altatech	a-Si:H (n)	AZO/Ag	polished	SM
a-Si:H/SiN_X	AKT	nc-Si:H (n)	ITO/Ag	polished	SM

*PL: Photolithography, SM: Shadow Mask
**WO_X only on emitter

5.2 Characterisation Approach

The solar cells presented in this chapter are usually analysed based on their illuminated jV characteristics and the resulting key parameters: open-circuit voltage (V_{OC}),

short-circuit current density (j_{SC}), fill factor (FF) and efficiency (η). Additional characterisation methods are outlined in the following.

5.2.1 Absence of Statistical Deviations

The solar cell parameters listed in this chapter usually represent the best result obtained for the corresponding cell structure and statistical deviations are not given. As outlined in subsection 4.2.1, each wafer contains 13 solar cells, from which at most four are identical (regarding cell area and emitter/BSF ratio), which severely limits the amount of directly comparable results necessary for proper statistics. Furthermore, the manufacturing processes used (both the photolithography and the shadow mask one) involve an extensive amount of manual handling, potentially degrading parts of wafers more than others. Consequently, it cannot be guaranteed that all solar cells on the respective wafer were treated exactly the same. The respective top results are expected to be affected the least by these erratic degradation effects and therefore regarded as a better measure for the potential of the respective technology.

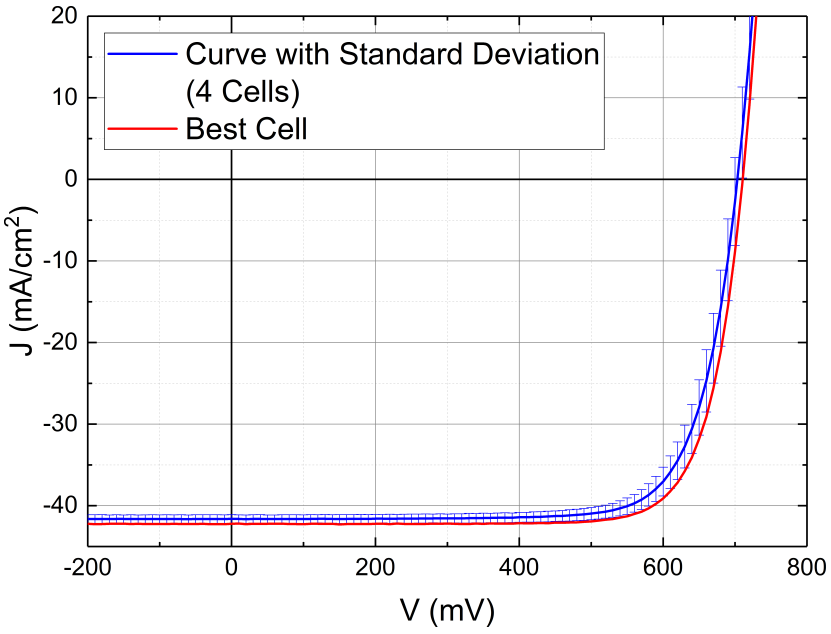


Figure 5.3: Comparison between a jV curve constructed from four jV curves of seemingly identical solar cells and the appropriate jV curve of the best solar cell.

Figure 5.3 shows a jV curve constructed from four cell results and the appropriate best case curve. The large deviations apparent in this example are largely the consequence of a single bad cell dragging down the average result, illustrating the problem arising from statistics based on too few individual data points.

5.2.2 Analysis of the Contact Resistivity

The analysis of the solar cell devices presented in this chapter focuses mainly on their fill factor. SHJ solar cells are prone charge carrier transport issues owing to the intrinsic a-Si:H passivation layer [128], band offsets [46, 149] and emitter/TCO tunnel-recombination contacts [63, 150, 151]. Using a back-contacted architecture and hence reducing the total contact area increases the difficulty of this task further.

The maximum achievable FF of a SHJ solar cell (implied, iFF) can be calculated based on the corresponding wafer's passivation quality (before metallisation), more specifically on the ratio between the respective effective minority charge carrier lifetimes at the MPP and V_{OC} injection level (see subsection 3.2.2). Constructing series resistance free pseudo-jV curves for completed solar cells, using the Suns-V_{OC} method (see subsection 3.2.4), allows to calculate the pseudo-FF (pFF). A large difference between iFF and pFF hints the potential degradation of the passivation during the metallisation process, a low shunt resistance, or both. Consequently the difference between the pFF and the FF extracted from a standard illuminated jV curve represents the losses related to the series resistance of the solar cell. For the solar cells analysed in this work, the latter usually dominates. Quantifying the different contributions to the series resistance is therefore of utmost importance for the development of IBC SHJ solar cells. The two methods used to determine the total series resistance are outlined in subsection 3.2.6.

In an IBC SHJ solar cell, the c-Si bulk represents the only region with significant lateral current flow. Taking into account the solar cell's geometry (wafer thickness, emitter and BSF widths) as well as the wafer's resistivity, the bulk-related series resistance contribution can be approximated to a maximum of $65\,\mathrm{m\Omega cm^2}$ for the photolithography based solar cells (assuming majority carrier flow only parallel to the cell's surface, see [152]). Owing to its very low conductivity, the emitter contributes around $30\,\mathrm{m\Omega cm^2}$, with the exact value depending on the eventual thickness. The conductivities of the BSF and TCO materials are sufficiently high to render their series resistance contribution negligible, given their thickness values are in the nanometre range. The same applies for the metallisation, as the cell area is rather small ($1\,\mathrm{cm^2}$). Thus for the contact geometry of the photolithography based solar cells, the contact resistivities of the a-Si:H/c-Si and the a-Si:H/TCO interfaces (respectively nc-Si:H instead of a-Si:H) are the main contributors to the series resistance.

As outlined in subsection 3.2.5 the contact resistivity of a specific layer stack can be determined with the TLM method. Corresponding n-type TLM structures are part of the photolithography mask layout resulting in an identical layer stack compared to the one of the respective solar cells. Equivalent TLM structures on p-type c-Si wafers were built as well, but neither the wafer material, with respect to its surface and

specific resistivity, nor the process conditions are necessarily identical. This reduces the accuracy of an already inherently imprecise measurement technique further. Especially if polished surfaces (in accordance with the cell wafers) were used, the absence of linear jV characteristics (ohmic contact) impeded the application of the TLM method. Table 5.2 nevertheless summarises the average results of various TLM measurements of exemplary contact stacks allowing to identify trends and tendencies.

Table 5.2: TLM results

contact layer stack	$\rho_{N,TLM}$ Ωcm^2	$\rho_{P,TLM}$ Ωcm^2	surface condition
i a-Si/n a-Si:H/ITO	0.12 - 0.13	n/a	polished
i a-Si/n a-Si:H/Al*	0.07 - 0.08	n/a	polished
i a-Si/n nc-Si:H/ITO	0.08 - 0.09	n/a	polished
i a-Si/n nc-Si:H/AZO	0.06 - 0.07	n/a	polished
i a-Si/n nc-Si:H/ITO	0.03 - 0.05	n/a	textured
i a-Si/n nc-Si:H/AZO	0.04 - 0.06	n/a	textured
i a-Si/p a-Si:H/ITO	n/a	1.27**	polished
i a-Si/p a-Si:H/WO_X/ITO	n/a	1.07**	polished
i a-Si/p a-Si:H/ITO	n/a	0.17 - 0.28	textured
i a-Si/p a-Si:H/AZO	n/a	0.67 - 1.43	textured
i a-Si/p a-Si:H/WO_X/ITO	n/a	0.15 - 0.35	textured

*annealed without damaging passivation
**poor contact linearity

The results for n-type TLM structures show little deviations, as both ITO and AZO form perfectly ohmic contacts to the n-type a-Si:H and nc-Si:H layers. ITO performs better with nanocrystalline silicon than with amorphous silicon, a clear advantage for either ITO or AZO cannot be identified. The validity of the values extracted from measurements of the polished p-type TLM structures is questionable, owing to the poor contact linearity.

Switching to textured surfaces, a general decrease in contact resistivity is observed, as the corresponding TLM structures were built without adjusting the deposition time of the a-Si:H processes, resulting in thinner intrinsic a-Si:H layers. Linearity issues are still a common occurrence when measuring p-type TLM structures, thus the high spread. Despite these issues, the aggregated TLM results illustrate that the contact resistivity of the n-contact is substantially lower than the one of the respective p-contact.

The resulting share of the contact resistance for the n-contact can be calculated by dividing the measured contact resistivity by the respective BSF ratio or contact fraction. In absence of a valid TLM measurement, the equivalent for the p-contact can be estimated by subtracting the n-contact resistance (and $0.1\,\Omega cm^2$ accounting for

current transport losses in the wafer and the emitter) from the total series resistance. The result multiplied by the area fraction of the p-contact (emitter ratio, equal to $1-\text{BSF ratio}$) then gives the corresponding p-contact resistivity.

It is noteworthy that the accuracy of the calculated and measured data, namely the series resistance and the p- and n-contact resistivities, is poor, which is naturally translated to any calculated parameters based on these initial values. However, this refers more to the absolute magnitude of the respective values rather than their order. FF, Δ(pFF,FF), series resistance, and contact resistivity of the different cells yield a consistent picture, as for instance smaller contact resistivities (TLM) correspond to lower series resistances (Suns-V_{OC}, dark-JV comparison method) and higher FF values (jV curves).

The contact resistivity values listed above have certain implications on the optimal contact geometry. To reduce the overall contact resistivity, the majority of the rear side should be attributed to the p-contact. To determine to which extent the emitter ratio should be increased, the series resistance contribution of the contact resistivity of both contacts, $R_{S,CR}$, can be expressed in the following form:

$$R_{S,CR} = \frac{\rho_p}{A_p} + \frac{\rho_n}{A_n} \tag{5.1}$$

Here ρ_p and ρ_n represent the contact resistivity of the p- and the n-contact, respectively. A_p and A_n represent the corresponding area fractions. Assuming $A_n = 1 - A_p$, $R_{S,CR}$ becomes minimal if A_p is set that the following applies:

$$\frac{\partial R_{S,CR}}{\partial A_p} = \frac{\rho_n}{(A_p-1)^2} - \frac{\rho_p}{{A_p}^2} \stackrel{!}{=} 0 \tag{5.2}$$

The area fraction yielding the minimum total contact resistivity is then:

$$A_{p,min} = \frac{\sqrt{\rho_p}}{\sqrt{\rho_p}+\sqrt{\rho_n}} \tag{5.3}$$

Figure 5.4 shows the plot of $A_{p,min}$ over the p-contact resistivity for three different n-contact resistivities. The latter correspond to values derived from the TLM measurements. The graphs show that even for a very large discrepancy in p and n-contact resistivity (factor 30), extreme emitter ratios (above 90 %) are unfavourable.

Apart from the p- and n-contact resistivity the optimal emitter-to-BSF ratio also depends on the wafer properties and the surface passivation quality for both contact

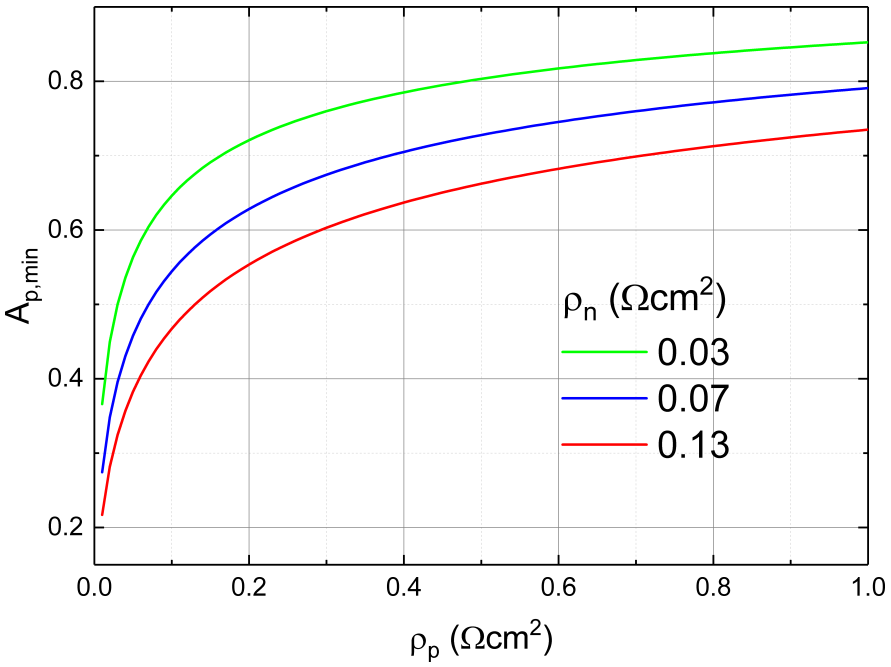


Figure 5.4: Emitter or p-contact area fraction yielding the minimum contact resistance over the corresponding p-contact resistivity for three different n-contact resistivities. For the values measured (see Table 5.2), the optimal emitter fraction lies between 60 to 80 %.

regions. To minimise recombination losses in the bulk the distance photogenerated minority carriers have to travel towards their respective contact should be kept as short as possible. Hence larger emitter ratios are beneficial in that regard as well. Conversely the passivation quality is usually worse in the p-type emitter regions, as p-type a-Si:H tends to degrade the underlying intrinsic a-Si:H passivation [127, 153]. For larger pitch values the aforementioned approximation for the bulk-related contribution to the series resistance is no longer valid, and thus also the assumption of the series resistance mainly limited by the contact resistivities.

5.2.3 S-Shapes

The aforementioned methods to analyse the FF and corresponding losses based on Suns-V_{OC} measurements and series resistance extraction rely on the validity of the superposition principle. As already outlined in subsection 2.2.4, a solar cell under illumination can be modelled as the superposition of a diode and an external current source, where the jV characteristics of the former depend on the temperature and the applied voltage (see Equation 2.2), and the latter only on the charge carrier generation induced by the external illumination (neglecting series and shunt resistance effects). This is not necessarily the case for a heterojunction device, as the band offsets at the

a-Si:H/c-Si interface, especially the valence band offset ΔE_V at the p-contact, represent non-linear transport barriers. Chavali *et al.* describe the jV characteristics of a SHJ solar cell by introducing the voltage V_1, at which the top of the a-Si:H valence band at the interface is aligned with the c-Si valence band at the depletion edge [154]. Depending on the influence of the photogenerated charge carriers on the electro-potential at the a-Si:H/c-Si interface, V_1 might differ in dark and light conditions. In dark conditions, the current at $V >= V_1$ depends on the valence band barrier observed from the emitter side. This barrier is a result of the band bending within the amorphous silicon, which itself is relatively independent from the applied voltage. The latter affects mainly the degree of inversion at the c-Si side of the interface. Consequently the diode current under dark conditions saturates for $V >= V_1$. Under light conditions the valence band offset ΔE_V becomes the limiting factor for the extraction of the photogenerated minority charge carriers at voltages greater V_1, hence an inflection point in the corresponding jV curve can be observed.

The presence of an S-shape in the jV curve of a SHJ solar cell depends on the magnitude of V_1 (under light). If V_1 is sufficiently high ($V_1 > V_{OC}$), the resulting inflection point does not limit the jV response in the relevant voltage range ($V < V_{OC}$). If V_1 is significantly lower than V_{OC}, the resulting S-shape will deteriorate the FF. In this case, the asymmetric barriers limiting the current under dark and light conditions also invalidate the superposition principle outlined above.

The magnitude of V_1 depends on the band bending in the c-Si induced by the emitter and thus on the doping level of the emitter layer. A too thick inversion layer reduces the emitter-induced band bending as well.

S-shapes can also be triggered by parasitic counterdiodes arising from Schottky contacts or malfunctioning tunnel-recombination junctions between the p-type emitter and the n-type TCO [150]. To enable efficient tunnelling from the valence band of the emitter to the conduction band of the TCO, strong band bending at the a-Si:H/TCO interface is necessary, which is again related to the doping level of the emitter layer [63]. The presence of a strongly n-doped TCO at the p-contact of the solar cell (wafer, emitter and TCO form a npn-structure) might also decrease the band bending in the c-Si wafer, if the p-layer is too thin.

Both S-shape mechanisms are therefore related to the doping of the emitter layer, indicating the importance of the p-type a-Si:H optimisation process. The solar cells presented in the following do not suffer from S-shapes, barring one exception. Hence analysing their results using methods based on the validity of the superposition principle is justified.

5.3 Cells with Direct Aluminium/a-Si:H Contacts

Solar cells were built on single-side polished float-zone wafers using the photolithography process outlined in section 4.2. The front side layer stack consisting of a SiN_X double-layer (10 nm with refractive index of $n = 2.4$ and 90 nm with $n = 1.96$) was deposited at the Institute for Solar Research Hameln (ISFH). In total two batches (hereafter denoted as batch 1 or b1 and batch 2 or b2) were produced, the second roughly 12 months after the first. The effective lifetime of the corresponding, symmetrically deposited reference samples did not exceed 1 ms for batch 1 and 1.5 ms for batch 2, thus limiting the V_{OC} and FF potential (low iFF). Batch 1 also featured a rear side passivation consisting of a 12.6 nm thick thermal oxide (grown at $T = 900°C$) and a 100 nm thick SiN_x layer. Before applying the initial a-Si:H layers (the intrinsic/p-type stack) this passivating layer stack was patterned in an additional photolithography step (etched with buffered hydrofluoric acid, BOE 7:1) removing it in the cell regions. For batch 2 this particular rear side passivation stack was omitted to reduce the amount of necessary photolithography steps. Instead of this dedicated passivation layer, the passivation between the different cell areas was provided by the BSF layer stack (see subsection 4.2.1).

PECVD processes were performed in the FAP tool (see subsection 4.1.1), with thickness target values of 5 nm for the intrinsic and 20 nm for the doped amorphous silicon layers, respectively. Aluminium contact layers with a thickness of 1.5 μm, were directly evaporated onto the patterned emitter/BSF layers. During the course of the measurements, the solar cells were annealed on two different hotplates, hereafter denoted as HP1 and HP2: given the identical set temperature T_{SET}, HP1 is expected to lead to a more homogeneous temperature distribution in the wafer, as it features a heat-reflecting lid. The corresponding annealing temperatures are therefore given an index, indicating the respective hotplate, e.g. $T = 150°C_1$ refers to an annealing process on HP1 with a set temperature of 150 °C, while $T = 150°C_2$ refers to the equivalent on HP2. In general batch 1 devices were annealed on HP1, batch 2 ones on HP2.

The ITO/Ag reference device features the batch 1 front side layer stack and a PECVD layer configuration identical to the one of the solar cells with the a direct aluminium metallisation. The approximately 150 nm thick ITO layer was sputtered in the MicroSys 200 PVD system, the initial 400 nm Ag in the Leybold Optics tool (see section 4.1.2). On top of this sputtered layer another silver layer was deposited by thermal evaporation resulting in a total silver layer thickness of roughly 2 μm.

5.3.1 Illuminated Current–Voltage Measurements

Table 5.3 lists the jV parameters of the ITO/Ag reference cell, the best cell from batch 1 and the two best cells from batch 2, including the corresponding annealing times (t_{ann}) and temperatures (T_{SET}, referring to HP1 or HP2). The respective emitter ratio values, defined as the emitter width divided by the pitch, are given as well.

Table 5.3: jV parameters (solar cells under illumination)

	$t_{\mathrm{ann}}\|T_{\mathrm{SET}}$	j_{SC}	V_{OC}	FF	Emitter ratio	η
	m|°C$_{\mathrm{x}}$	mA/cm^2	mV	%	%	%
ITO/Ag	$5\|200_1$	40.5	687	69.1	65	19.2
Al b1	$5\|150_1$	40.5	684	72.9	65	20.2
	$+10\|150_1$	40.5	649	78.7		20.7
Al b2	$5\|150_2$	41.6	696	73.8	65	21.4
	$+30\|150_2+10\|160_2$	41.9	699	75.1		22.0
	$+10\|170_2$	41.6	660	78.2		21.5
Al2 b2	$35\|150_2+8\|160_2$	41.6	703	75.2	77	22.0

Impact of the Front Side Passivation

Batch 2 solar cells feature j_{SC} values roughly 1 mA/cm^2 higher than the ones of batch 1. Likewise, the batch 2 V_{OC} values, after the initial annealing, improve by around 15 mV. Both differences can be attributed to the improved front side passivation. Figure 5.5 shows the EQE and IQE curves as well as the spatially resolved reflection of the aluminium-contacted solar cells. The latter is similar among the two batches, even showing a slight advantage for batch 1 in the infrared wavelength range. In the range between 600 and 1000 nm, the batch 2 front side reflects marginally less light than the one of batch 1. The EQE and IQE curves reveal a more significant change: the IQE of the batch 1 solar cell peaks at around 95 %, indicating recombination losses owing to an insufficiently passivated front side. On the contrary batch 2 solar cells achieve IQE values close to 100 % in the more important wavelength region from 500 to 1000 nm. The gain in j_{SC} is therefore not a consequence of improved optical properties, but improved electrical properties with respect to the passivation quality. This also leads to the aforementioned increase of the initial V_{OC}. With longer annealing times, the V_{OC} eventually decreases as the degraded rear side passivation becomes the limiting factor.

Annealing-induced Changes of Fill Factor and Series Resistance

As described in section 3.2.2 and 5.2.2, the fill factor is analysed by identifying its limits given by the initial passivation, i.e. determining the implied FF from lifetime data and

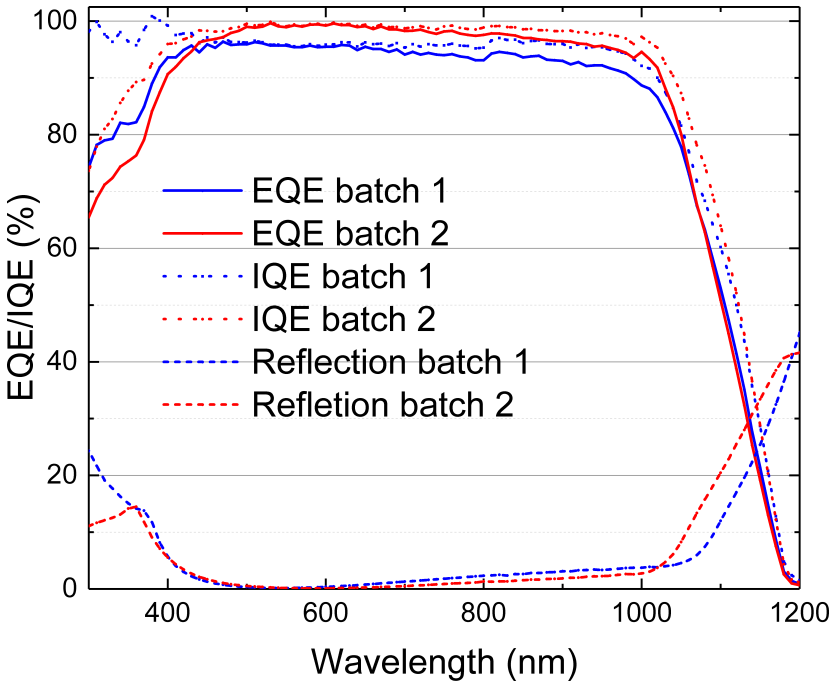


Figure 5.5: EQE, IQE and reflection spectra of the solar cells featuring a direct aluminium metallisation (Copyright (2017) The Japan Society of Applied Physics [147]).

the pseudo FF from Suns-V_{OC} measurements. A comparison of all three values (iFF, pFF and jV-derived FF, visualised in Figure 5.6) then allows to quantify the relative contribution of series resistance and non-series resistance related FF losses. Table 5.4 lists the relevant FF values, if available, for the different solar cells as well as the series resistance extracted with the dark-jV comparison method, described in subsection 3.2.6.

For the ITO/Ag reference solar cell, lifetime data obtained after the deposition of the BSF layer stack (intrinsic and n-type a-Si:H) yields an implied FF of 81.5 %. With 80.1 % the pFF is close to the iFF, indicating that the non-series-resistance related losses are comparably small. The FF extracted from the jV measurement is 69.1 %, resulting in a difference between the pFF and the FF of 11 %abs. The jV curve depicted in Figure 5.7 reveals that this pronounced difference not only originates from an ohmic series resistance, but also from a slightly S-shaped jV curve. As described in subsection 5.2.3, too thick intrinsic a-Si:H layer can lead to S-shaped jV curves, however, since corresponding solar cells with a direct Al/a-Si:H metallisation and identical intrinsic a-Si:H layers did not show this phenomenon, it is more likely related to a malfunctioning tunnel-recombination contact between the p-type a-Si:H and the n-type ITO. Typically insufficient doping of the p-type a-Si:H emitter results in an inadequate amount of band bending at the TCO interface. Thus the energetic difference between the ITO conduction and emitter valence band is too high and does not allow efficient tunnelling of holes extracted from the c-Si wafer. This type of transport barrier

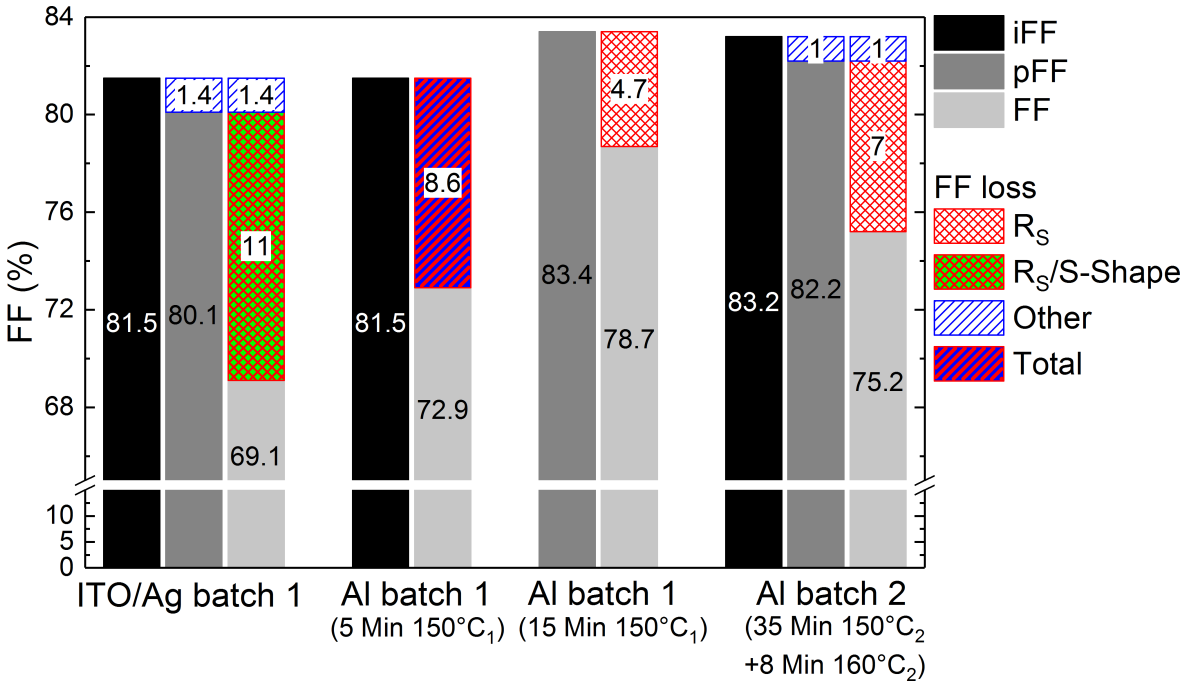


Figure 5.6: Visualisation of the implied-, the pseudo- and the jV-derived fill factor (iFF, pFF, FF) as well as the related losses for the aluminium contacted solar cells and the ITO/Ag reference cell. The index of the temperature unit refers to the hotplate used, HP1 or HP2.

exhibits a non-linear behaviour, leading to S-shaped jV curves [63]. As outlined in subsection 5.2.3, the superposition principle, a necessary condition for the application of the calculation of the series resistance and the aforementioned FF analysis, is no longer valid for this particular cell. Hence, there is a caveat to the high series resistance value of the ITO/Ag solar cell listed in Table 5.4 and the large difference between pFF and jV-derived FF cannot be solely attributed to the series resistance.

Table 5.4: FF analysis

	$t_{ann}\|T_{SET}$ m|°C_x	iFF %	pFF %	FF %	|pFF - FF| %abs	$R_{Ser,Total}$ Ωcm^2
ITO/Ag	5|200_1	81.5	80.1	69.1	11.0	2.1*
Al b1	5|150_1	81.5	/	72.9	/	1.5
	+10|150_1	/	83.4	78.7	4.7	0.5
Al2 b2	35|150_2+8|160_2	83.2	82.2	75.2	7.0	1.2

*S-shape afflicted

For the batch 1 Al cell, the same kind of analysis is not straightforward either. Since the two batch 1 wafers were treated exactly the same until the deposition of the metallisation, the iFF is equal to the ITO/Ag device. However, the pFF is higher

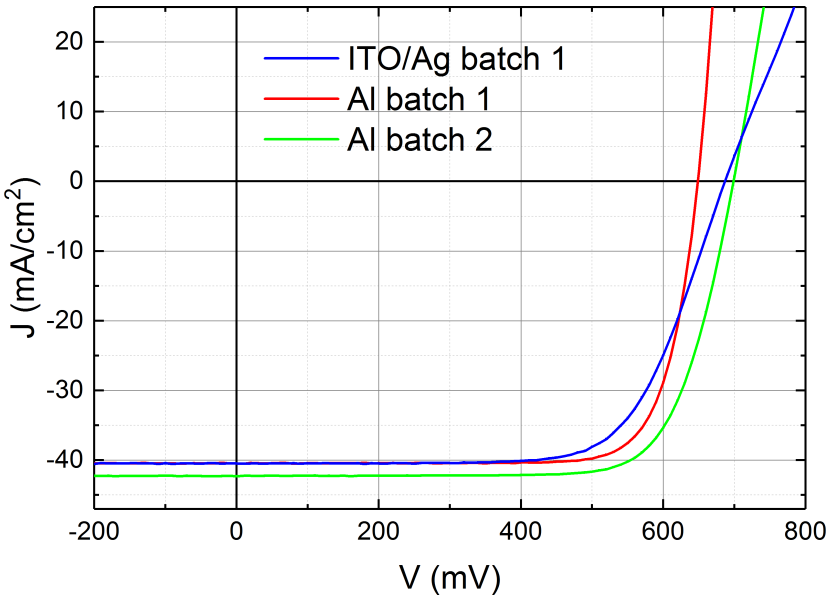


Figure 5.7: jV curves of the solar cells listed in Table 5.4 under 1-Sun illumination – the current of the Al batch 2 cell is slightly overestimated owing to improper shading of neighbouring cells during the measurement. The values given in the respective tables are corrected (Copyright (2017) The Japan Society of Applied Physics [147]).

than the iFF, as the Suns-V_{OC} measurement was done after the prolonged annealing, which greatly altered the characteristics of the cell in terms of contact resistivity and passivation quality. It is therefore impossible to determine the contribution of the non-ohmic losses to the FF after five minutes of annealing. By comparing the iFF of the batch 1 Al cell to the jV-derived FF after five minutes of annealing, the total FF losses at this stage (8.6 %abs) can be determined. If then the non-ohmic losses are assumed to be on a similar level as for the ITO/Ag device, one can regard almost all of the total loss as ohmic. A comparison of the pFF to the measured FF of the corresponding device after 15 minutes of annealing then reveals ohmic losses of 4.7 %abs, indicating that pro-longed annealing significantly lowers the series resistance of the corresponding solar cell and thus increases the FF. For the batch 2 Al cells, the improved front side passivation yields an iFF value of 83.2 %, almost 2 %abs higher than the one for the batch 1 devices. A more careful annealing allowed to increase the FF without deteriorating the V_{OC} and thus the passivation quality (in fact a slight increase in V_{OC} is observed, likely related to the annealing of the intrinsic a-Si:H layer). The pFF compares to the iFF as expected by being 1 %abs lower, indicating small non-series-resistance related losses. The difference between the pFF and the FF amounts to 7 %abs.

As shown in Figure 5.6, the FF analysis revealed that the FF losses of all solar cells presented so far are dominated by the series resistance. The series resistance values for

the Al cells heavily depend on the amount of annealing but values as low as $0.5\,\Omega\mathrm{cm}^2$ illustrate the potential of the aluminium metallisation.

Table 5.5: R_S analysis

	$t_{\mathrm{ann}}\|T_{\mathrm{SET}}$ Min|°C$_x$	$R_{\mathrm{Ser,Total}}$ $\Omega\mathrm{cm}^2$	BSF ratio %	$\rho_{\mathrm{N,TLM}}$ $\Omega\mathrm{cm}^2$	$R_{\mathrm{Ser,N}}$ $\Omega\mathrm{cm}^2$	$R_{\mathrm{Ser,P}}$ $\Omega\mathrm{cm}^2$	$\rho_{\mathrm{P,calc}}$ $\Omega\mathrm{cm}^2$
ITO/Ag	$5\|200_1$	2.1*	35	0.12	0.35	1.65*	1.07*
Al b1	$5\|150_1$	1.5	35	0.11	0.32	1.08	0.70
	$+10\|150_1$	0.5		0.05	0.14	0.26	0.17
Al2 b2	$35\|150_2+8\|160_2$	1.2	23	0.07	0.30	0.80	0.62

*S-shape afflicted

To further investigate the different contributions to the series resistance, TLM measurements of the n-contact were performed, either with test structures on the cell wafers itself or on identically processed wafers. Table 5.5 lists all relevant parameters: $R_{\mathrm{Ser,Total}}$ represents the total series resistance, extracted by the dark-jV comparison method; the *BSF ratio* is determined by dividing the BSF width by the pitch; $\rho_{\mathrm{N,TLM}}$ is the n-contact resistivity extracted by the TLM measurement; $R_{\mathrm{Ser,N}}$ the series resistance contribution of the n-contact, as the result of the division of $\rho_{\mathrm{N,TLM}}$ and *BSF ratio*; $R_{\mathrm{Ser,P}}$ is the result of the subtraction of $R_{\mathrm{Ser,N}}$ and $0.1\,\Omega\mathrm{cm}^2$ (accounting for bulk related losses, see subsection 5.2.2) from $R_{\mathrm{Ser,N}}$; at last $\rho_{\mathrm{P,calc}}$ results from dividing $R_{\mathrm{Ser,P}}$ by the emitter ratio ($1-$*BSF ratio*).

For all cells the p-contact features a greater resistivity than the n-contact. Again a caveat must be added to the results for the ITO/Ag reference device, as the S-shaped jV curve invalidates the extraction method for the total series resistance. Nevertheless, the TLM measurement of the n-contact, and thus the respective values for the parameters $\rho_{\mathrm{N,TLM}}$ and $R_{\mathrm{Ser,N}}$ are not affected by the S-shape. The value of $\rho_{\mathrm{N,TLM}}$ of the ITO/Ag reference ($0.12\,\Omega\mathrm{cm}^2$) is almost identical to the one of the batch 1 Al device annealed for five minutes ($0.11\,\Omega\mathrm{cm}^2$), which indicates that the measured difference in FF (3.8 %abs) most likely arises from a difference in the p-contact.

Annealing the Al contact leads to a distinct reduction of the contact resistivities for both polarities. Extended annealing, as performed on the batch 1 solar cell, halves the BSF contact resistivity (0.11 to $0.05\,\Omega\mathrm{cm}^2$) but quarters the one of the p-contact (0.70 to $0.17\,\Omega\mathrm{cm}^2$). Moderately annealed cells, like the batch 2 example, still feature a pronounced discrepancy between the emitter and the BSF contact resistivity (0.62 vs $0.07\,\Omega\mathrm{cm}^2$). This indicates that the strong decrease of the p-contact resistivity observed in the case of the extended annealing comes at the cost of a deteriorated passivation quality.

The annealing of the Al contact and the consequential increase of the FF and decrease of the V_{OC} result in a trade-off situation. The annealing time and temperature needed to achieve the maximum efficiency are initially unknown. The batch 1 and batch 2 devices analysed above represent two opposing cases. The batch 1 solar cell achieves a higher efficiency by sacrificing a significant amount of V_{OC} (roughly 40 mV) as it gains more from the resulting FF increase (almost 6 %abs). Conversely the moderate annealing of the batch 2 solar cell leads to an equally moderate increase of the FF, but also a stable V_{OC}. The measurement results suggest that the V_{OC} values resulting from an extended annealing do not depend on the initial V_{OC} level, hence the efficiency of solar cells with an initially superior passivation quality (batch 2 devices in this case) is affected stronger by the decrease in V_{OC} upon annealing, as the more pronounced loss cannot be compensated by the gain in FF. This effect is also visualised Figure 5.8, depicting the different development of the V_{OC}, the FF, and the efficiency during the annealing procedure for both solar cell batches. The batch 1 solar cell achieves its maximum efficiency after a pronounced drop in V_{OC}, as the FF increase compensates the V_{OC} loss. Further annealing degrades the performance, as the FF saturates. The batch 2 solar cell experiences a slow and steady increase in both V_{OC} and FF, until the efficiency reaches a plateau. Further annealing strongly increases the FF, but the V_{OC} losses cannot be compensated.

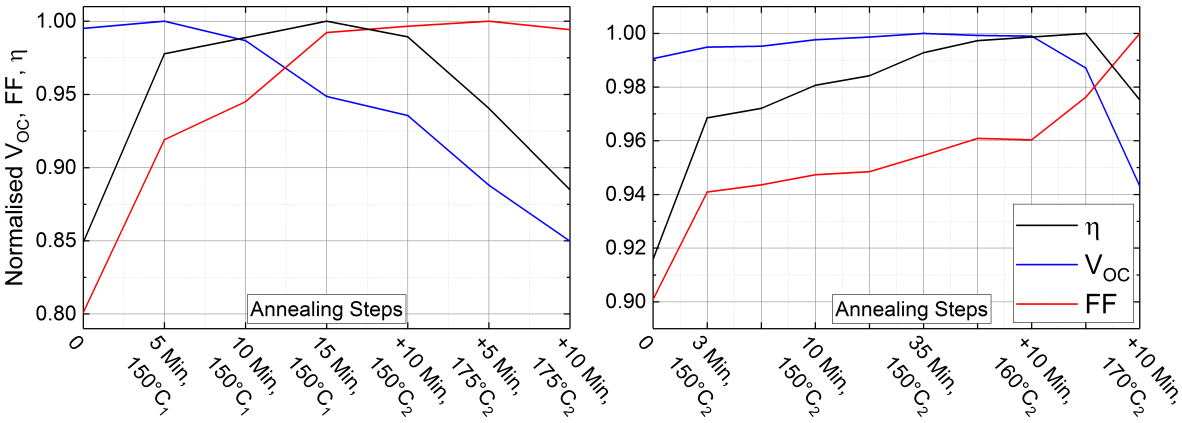


Figure 5.8: Normalised development of the V_{OC}, FF, and η during the annealing procedure. The graph on the left refers to a batch 1 solar cell, the one on the right to a batch 2 solar cell.

5.3.2 Aluminium-interacted Silicon Surfaces

The interaction of aluminium with amorphous silicon layers following the annealing at different temperatures has been studied thoroughly by many researchers. Ishihara *et al.* [155] reported the presence of pits in amorphous silicon layers as a consequence

of interdiffusion effects between aluminium and amorphous silicon at temperatures as low as 170°C. Furthermore the resulting contact resistivity was determined to be as low as $0.001\,\Omega\mathrm{cm}^2$. Haque *et al.* [124, 125] studied extensively the aluminium-induced crystallisation of amorphous silicon layers and the subsequent changes in their electrical properties at temperatures ranging from 150 to 300 °C. They observed the start of Al/a-Si:H interaction at temperatures as low as 150 °C and the onset of aluminium-induced crystallisation of the amorphous silicon layers at 180 °C. In the temperature range between 150 and 180 °C an $\mathrm{Al_XSi}$ mixed phase at the interface forms, lowering the contact resistivity drastically. A subsequent study describes the effect of Al-induced p-type doping – temperatures around 200 °C are sufficient to counterdope n-type a-Si:H layers. Hentzell *et al.* [156] stated the existence of an aluminium silicide, starting to form at a temperature of approximately 170 °C, prior to the silicon crystallisation. This silicide features unique structural properties and is stable up to temperatures of approximately 300 °C (following the crystallisation of the a-Si:H layer). Ashtikar *et al.* [157] studied the reaction of hydrogenated a-Si:H with aluminium, the formation of an aluminium silicide, and the crystallographic properties of the latter. An aluminium silicide was already observed at room temperature – crystallisation initiates at temperatures around 200 °C and is completed at 300 °C, resulting in the formation of polycrystalline and porous silicon films. During the gradual crystallisation process, the metastable silicide layer facilitates the interdiffusion of Al and Si into each other.

Aluminium-induced crystallisation and aluminium contacts on amorphous silicon layers are also used in different homojunction solar cell devices: Schaper *et al.* [158] developed a contact system based on the local exchange of aluminium and amorphous silicon. The rear side of their device is passivated with a 30 nm thick a-Si:H layer, onto which structured 15 μm thick aluminium finger stripes are deposited. In a subsequent deposition step performed at 325 °C the amorphous silicon under the aluminium fully dissolves into the latter resulting in the formation of localised ohmic Al contacts to the c-Si wafer. Bullock *et al.* [159] introduced an amorphous silicon layer in-between the diffused junctions and the aluminium contact layers of a homojunction c-Si solar cell, as an alternative to the tunnel oxide found in conventional TOPCon or PERC cells. The increase in passivation quality resulted in V_{OC} gains of up to 50 mV, while the contact resistivity increased to $0.05\,\Omega\mathrm{cm}^2$ for n^+ and to $0.1\,\Omega\mathrm{cm}^2$ for p^+ surfaces. The current transport through the the a-Si-passivated Al contact was described to occur through a combination of tunnelling and aluminium protrusions through the passivation layer contacting the c-Si wafer.

The aluminium electrodes in the IBC SHJ devices presented in this work are annealed at comparatively low temperatures: a full crystallisation or a complete removal of the amorphous layers due to diffusion into the much thicker Al layer is thus neither expected nor intended. Annealing the corresponding solar cells at a temperature of 150 °C$_2$ for extended periods of time (up to 35 minutes) led to a significant improvement in the FF and minor improvements in V_{OC}. Referring to the findings of Haque and Ashkitar, probably a thin Al silicide layer forms at the interface, mostly enhancing the contact resistivity without deteriorating the passivating effect of the intrinsic amorphous silicon layer. Increasing the annealing temperature up to 170 °C should initiate the crystallisation of the a-Si:H material and strong interdiffusion between the aluminium and the a-Si:H layers. In this phase, the contact resistivity continues to decrease, as indicated by the increasing FF; however, due to the continuous diffusion process of aluminium, defects are introduced into the band gap of the amorphous silicon, degrading the passivation of the crystalline silicon surface. Although the Al defects probably enhance the p-type doping in the emitter region, they will lower the n-type doping in the BSF regions, reducing the field effect passivation at this interface; prolonged annealing might also lead to counterdoping of the n-type a-Si:H regions. All these effects eventually result in a substantial reduction in V_{OC}. A further increase in annealing temperature then results in a strong diffusion of the amorphous silicon material into the Al layer, leaving behind either voids or regions consisting of aluminium, as depicted in Figure 5.9, showing an SEM image of the a-Si:H surface after extended annealing and subsequent removal of the Al layer.

Photoelectron Spectroscopy

To further examine the influence of the Al annealing on the amorphous silicon layers, test structures equivalent to the solar cell contact system were fabricated (featuring a layer stack of aluminium, p-type a-Si:H and n-type c-Si) and subsequently analysed by near UV photoelectron spectroscopy in the constant final state mode (CFSYS, see subsection 3.2.9). The first sample underwent the same treatment that led to the drastic decrease of the V_{OC}, i.e., an annealing of 15 minutes at a temperature of 150 °C$_1$ (on hotplate 1). Afterwards the aluminium layer was etched back to reveal the aluminium-interacted amorphous silicon surface. The second sample was processed the same way, but not annealed. It therefore serves as a reference sample that was only modified by the chemical Al etching process but not by the temperature-driven aluminium interdiffusion process. Figure 5.10 shows the CFSYS spectra of the two samples, alongside a third spectrum measured on an RCA cleaned and subsequently HF-dipped n-type c-Si wafer. It is possible to fit the spectrum of the first sample (annealed and etched back) as the

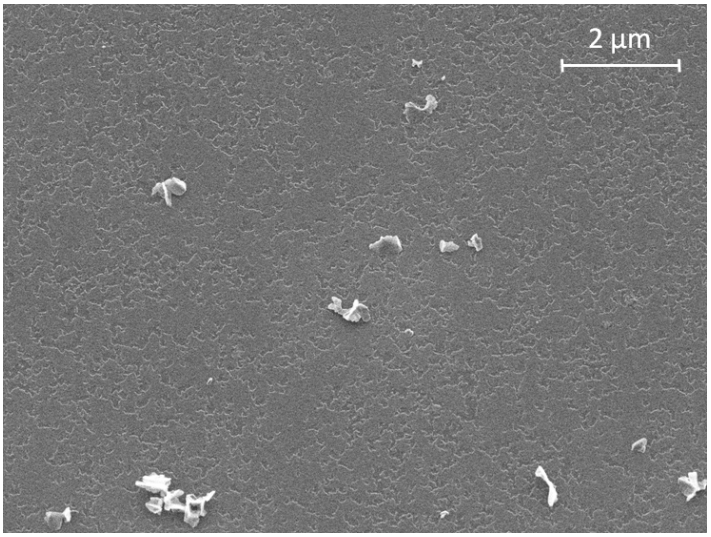


Figure 5.9: SEM image of the amorphous silicon surface after the removal of extensively annealed aluminium. The darker areas are pits in the amorphous silicon layer and the white flakes are believed to be residues of the Al silicide layer (Copyright (2017) The Japan Society of Applied Physics [147]).

sum of the shifted and scaled spectra of the second (etched back without annealing) and third (plain n-type c-Si) sample, using the following equation:

$$Cnt(E) = C_{\mathrm{a-Si}} \cdot Cnt_{\mathrm{a-Si}}(E - \Delta E_{\mathrm{a-Si}}) + C_{\mathrm{c-Si}} \cdot Cnt_{\mathrm{c-Si}}(E - \Delta E_{\mathrm{c-Si}}) \tag{5.4}$$

$Cnt_x(E)$ refers to the experimental energy resolved photoelectron counts of the reference spectra, $C_{\mathrm{a-Si}}$ and $C_{\mathrm{c-Si}}$ are the fit parameters, here the scaling constants of the two spectra, and $\Delta E_{\mathrm{c-Si}}$ and $\Delta E_{\mathrm{c-Si}}$ are the shifts of the corresponding spectra along the energy axis. With these shift values it is possible to calculate the valence band offset ΔE_{V} of the corresponding structure, e.g. the a-Si:H/c-Si interface:

$$\Delta E_{\mathrm{V}} = \Delta E_{\mathrm{a-Si}} + \Delta E_{\mathrm{c-Si}} - (E_{\mathrm{F}} - E_{\mathrm{V}})_{\mathrm{a-Si}} - (E_{\mathrm{F}} - E_{\mathrm{V}})_{\mathrm{c-Si}} \tag{5.5}$$

E_{F} refers to the Fermi energy and E_V to the respective valence band energy of the amorphous or crystalline silicon. For the spectra and the fit shown in Figure 5.10 ΔE_{V} equals 0.45 eV. This value is consistent with previous calculations for a-Si:H/c-Si heterointerfaces using the same method [49]. With regards to the SEM image in Figure 5.9, it can be concluded that the spectrum measured for the annealed and etched back sample results from an a-Si:H layer with a thickness of mostly above 2 nm (information depth of the measurement method) and small regions where it falls below 2 nm, which yields the c-Si contribution in the corresponding fit. Since the measurement of the second and the third sample were performed on different days

and the measured data was not corrected with respect to the different illumination conditions, the percentage of the exposed c-Si surface cannot be calculated by the two fitting parameters $C_{\mathrm{a-Si}}$ and $C_{\mathrm{c-Si}}$. The spectrum of the annealed and etched back sample also shows a signal 0.2 eV above the Fermi level ($E_{\mathrm{bind}} = 0$), most likely related to occupied gap states of the c-Si substrate. The energetic difference between these states and the equivalent ones of the n-type c-Si curve corresponds to the built-in potential (500 to 600 mV) at the interface between the n-type c-Si and the p-type a-Si:H.

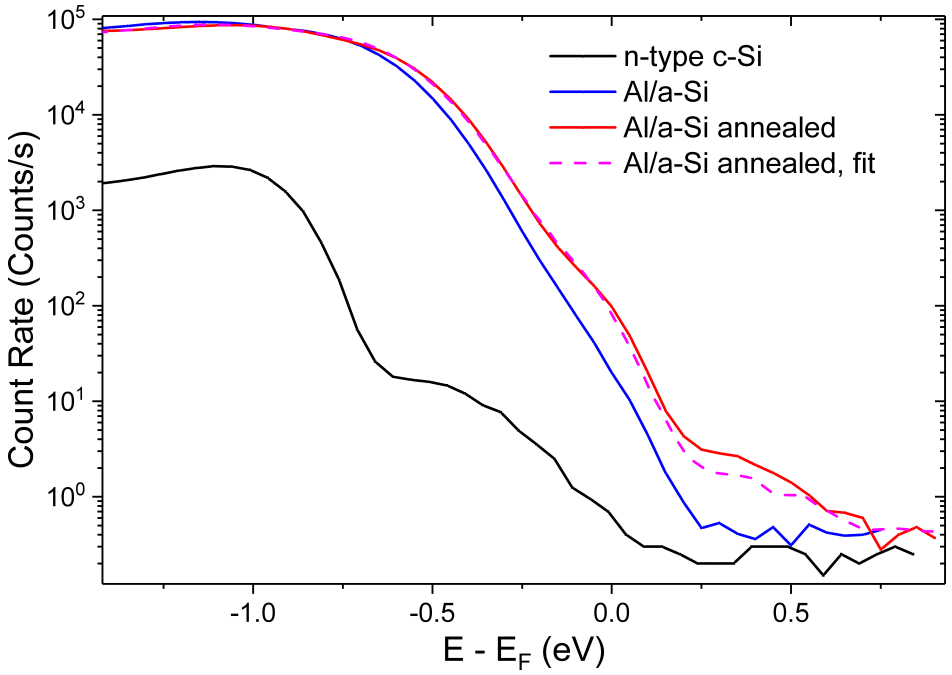


Figure 5.10: CFSYS spectra, where the red curve represents the Al-interacted a-Si:H sample, the blue curve the non-annealed, non-interacted a-Si:H sample and the black curve a plain n-type c-Si sample; the dashed curve shows the fit of the blue and black curves, being in good agreement with the red curve, thus indicating that the red curve depicts a measurement of a partly disintegrated a-Si:H layer on a c-Si surface (Copyright (2017) The Japan Society of Applied Physics [147]).

5.3.3 Simulation of Annealed Al/a-Si:H Contacts

Based on the phenomenological analysis in subsection 5.3.1, the cited literature, and the CFSYS measurements in subsection 5.3.2, the main physical phenomena expected to affect the performance of the IBC SHJ solar cells featuring annealed, direct aluminium/a-Si:H contacts are the formation of an aluminium silicide, followed by the partial crystallisation of the amorphous silicon and the formation of Al defects in the a-Si:H material. The CFSYS measurements suggest that prolonged annealing below 200 °C

damages the integrity of the a-Si:H layers significantly. Referring to the pits seen in the SEM image (Figure 5.9) it is possible to approximate the area heavily affected by the Al interaction to a maximum of 20 %. On the basis of this approximation, numerical simulations of the IBC SHJ devices were conducted, by introducing a modified region with increased charge carrier mobility and increased defect density into the a-Si:H contact layers. The former accounts for the partial crystallisation and the latter for the introduction of Al defects. Figure 5.11 depicts the corresponding unit cell with the modified regions indicated. The charge carrier mobilities were increased by a factor of 10 (from 5 to 50 $cm^2V^{-1}s^{-1}$ for the minority carriers, from 20 to 200 $cm^2V^{-1}s^{-1}$ for the majority carriers), which is in accordance with the measurement results from Nast *et al.* for polysilicon layers on glass, created from amorphous silicon by aluminium-induced crystallisation (glass/Al/a-Si to glass/poly-Si/Al) [160]. The value thus represents an upper limit as it refers to a fully crystallised layer. The parameters for Al defects in silicon layers were determined by Rosenits *et al.* [161]; the energetic position of the defect was then altered to account for the larger band gap of amorphous silicon (the defect parameters are listed in Appendix B).

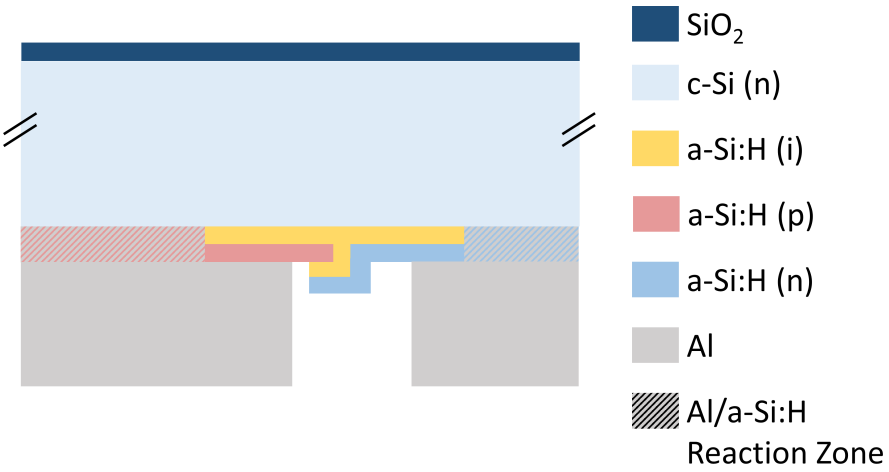


Figure 5.11: Simulated unit cell: ruled areas represent the aluminium interacted, modified regions with increased charge carrier mobility and Al defect densities. *Al/a-Si:H reaction zone* refers to the ratio of the total contact width that was modified.

Although the simulation setup produces reasonable results when compared with an experimental setup, it was not the objective to fully reproduce the corresponding measurements, but to confirm the experimental trends qualitatively. Despite the rather vague approximations made to incorporate the changes induced by the Al annealing, the trends for FF and V_{OC} observed in the measurements are clearly present in the simulation results: without any modification, the simulated cell achieves a V_{OC} of 733 mV and a FF value of 69.8 %. Although the V_{OC} is significantly higher than that in real cells, most likely owing to the very good front side passivation and the absence of

edge recombination, the FF is very close to values usually measured for non-annealed devices. As shown in Figure 5.12 a, increasing the charge carrier mobility leads to a significant increase in FF, also scaling with the ratio of the Al/a-Si:H reaction zone. In addition, the increase in FF was obtained without adding any additional Al defects, which is consistent with the measurement results suggesting that the increase in FF occurs prior to the deterioration of the V_{OC}. The maximum simulated FF increase (up to 77 %) is in good agreement with the measurement results obtained after extended annealing (15 minutes, $T = 150°C_1$). The effect of introducing an Al defect level into the band gap of the a-Si:H layers with a variable defect density is shown in Figure 5.12 b. Increasing the Al defect density up to values of the order of the doping density (charge carrier mobilities kept at the evaluated maximum values) leads to a strong decrease in V_{OC}, depending on the modified area fraction as well. The losses of 50 to 60 mV are again in good agreement with the measurement results of the annealed devices.

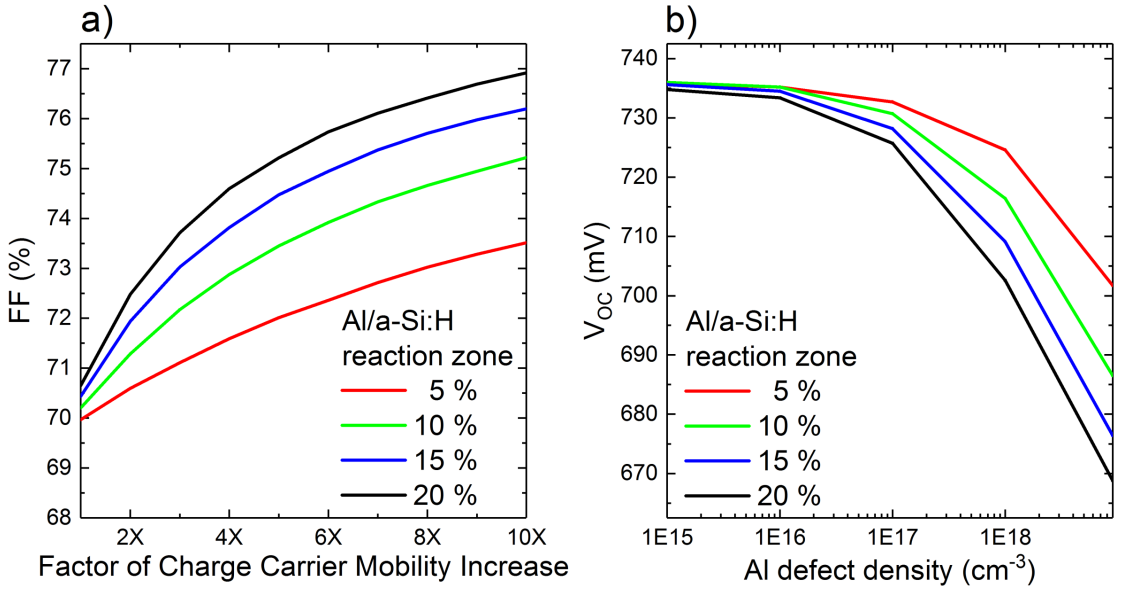


Figure 5.12: Simulated FF and V_{OC} trends following (a) the increase of the charge carrier mobility and (b) the introduction of a mid-gap Al-defect level with varying defect densities, both for a given percentage of the respective Al/a-Si:H reaction zones (Copyright (2017) The Japan Society of Applied Physics [147]).

5.3.4 Conclusions

The results presented in this subchapter show that a simple, direct aluminium metallisation is a viable option for high-efficiency IBC SHJ solar cells. A particular emphasis has to be put on the annealing procedure, as the final performance of the solar cell depends on the improvements in contact resistivity without unnecessarily deteriorating

the passivation quality. As surmised from literature findings, moderate annealing leads to the formation of an intermediate silicide layer between the aluminium and the amorphous silicon and initialises the crystallisation of the latter. Both effects are beneficial for the contact resistivity as the series resistance decreases and the FF increases. Extended annealing will lead to the disintegration of the amorphous silicon layers as strong interdiffusion takes place. The consequential decrease in V_{OC} cannot be compensated by a further FF increase, especially for well passivated solar cells with high initial V_{OC} values.

5.4 Cells with TCO/Metal Contacts

Contact stacks consisting of a transparent conductive oxide and a metal layer represent the standard configuration for silicon heterojunction solar cells. For most of the published high-efficiency solar cells ($\eta > 25\,\%$), the exact metallisation stack is not disclosed, however Adachi *et al.* [162] (two-side contacted SHJ cell) and Masuko *et al.* [28] (IBC SHJ cell) explicitly state using TCO contact layers. As outlined in subsection 2.2.2, the poor conductivity of the amorphous silicon layers necessitates the utilisation of a front side TCO layer providing sufficient lateral conductivity for the extracted charge carriers to reach the respective metallisation grid. Moreover, Holman *et al.* [52] have shown that an ITO layer is also favourable at the rear side of a SHJ solar cell, as it improves the optical response by suppressing plasmonic absorption effects occurring at direct metal/silicon interfaces. The latter effect is particularly relevant for IBC SHJ solar cells.

In the previous subchapter, the presented ITO/Ag cell served as a reference device for the solar cells with a direct aluminium metallisation, as it featured identical n- respectively p-type amorphous silicon layers (deposited in the FAP tool). The efficiency of this solar cell, 19.2 %, is limited by various factors. The j_{SC} of 40.5 mA/cm^2 is too low for an IBC device, as comparable solar cells exhibit values at least 1 to 2 mA/cm^2 higher. This indicates imperfect optical properties or an insufficient front-side passivation. The latter also results in a V_{OC} of 687 mV, contrasting the fact that SHJ solar cells are able to achieve V_{OC} values of up to 750 mV [22]. Additionally, with 69.1 % the FF is particularly low, as it is limited by a high series resistance exacerbated by a non-linear transport barrier that results in an S-shaped jV curve (see Figure 5.7).

The optimisation of the manufacturing process and the cell structure have led to significant improvements in the j_{SC}, the V_{OC} and most notably the FF of the TCO-based IBC SHJ solar cells. The respective solar cells results are presented and discussed in this subchapter.

5.4.1 Variation of TCO Materials

TCO materials differ with respect to their transparency, conductivity and work function. In an IBC solar cell, the TCO layers are mainly exposed to near-infrared light that is not absorbed during its first pass through the silicon wafer material. Ideally it is reflected by the metal electrodes and then absorbed on subsequent passes. Being reflected by the rear side metallisation, the light thus passes through the TCO layer twice causing parastic absorption. Rear side TCO layers are usually 70 to 150 nm thick to sufficiently suppress parasitic plasmonic absorption at the silicon interface [66]. Since the lateral current flow is negligible, the series resistance contribution of the TCO's bulk remains fairly limited, as conductivity values are in the sub-mΩcm and thicknesses in the nanometre range. The same does not apply for the TCO/a-Si:H interface. The transport properties of the interface and the resulting contact resistivity heavily depend on the respective band alignment. Figure 5.13 shows the results of a simulation study of an n-type c-Si wafer, symmetrically passivated with intrinsic a-Si:H [163]. On either side the wafer is contacted with a carrier-selective Schottky contact. The FF of this archetypal SHJ structure is then simulated independently varying the contact work function for the respective contact (the work function of the other contact is kept at an ideal value, i.e. 3 eV for the n-contact or 6 eV for the p-contact). Once the contact work function of the p-contact drops below the ionisation potential of the contacted material, the FF starts to decrease, and equivalently if the contact work function of the n-contact increases above the corresponding electron affinity. In these cases a transport barrier forms at either contact impeding the extraction of the respective charge carriers. In reality the situation is more complex, as the resulting barrier height not only depends on the work function and the electron affinity/ionisation potential of the respective materials, but also on the doping of the contacted material and surface states (see subsection 2.1.4). However, already this simplified example illustrates that the p- and n-contact have contradicting requirements regarding TCO materials capable of forming a contact with good current extraction properties (i.e. low transport barrier).

During the course of this work, three different TCO materials were evaluated: indium-tin oxide (ITO), aluminium-doped zinc oxide (AZO), and tungsten oxide (WO_X).

Indium Tin Oxide As already outlined in section 4.2.3, the ITO process used for the solar cells presented in this work was originally optimised towards the application of a front side TCO for standard SHJ solar cells. Hence the ITO layers feature a rather low specific resistivity of approximately $4{\cdot}10^{-4}\,\Omega$cm, with a charge carrier density of around $6{\cdot}10^{20}\,\mathrm{cm}^{-3}$ [132]. The latter is particularly high, which leads to a significant

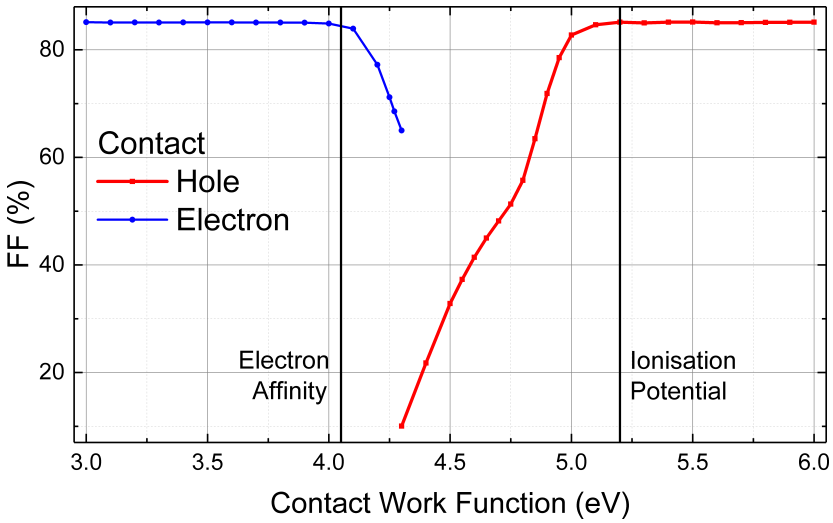


Figure 5.13: Simulation of the work function dependency of the fill factor for both contacts. Ideally the electron/hole contact features a work function being lower/higher than the corresponding electron affinity/ionisation potential [163].

amount of free carrier absorption resulting in roughly 20 % of parasitic absorption in the near infrared wavelength range.

To sufficiently suppress plasmonic absorption at the silver surface, the respective ITO layers have a thickness greater than 100 nm [52].

Aluminium-doped Zinc Oxide The AZO used in this work features a specific resistivity of around $5{\cdot}10^{-3}\,\Omega$cm, which is considerably higher than the one of the corresponding ITO [115]. With an AZO layer thickness of 70 nm, the bulk resistance of the AZO layer is still expected to be negligible. Since the work function of AZO is usually lower than the one of ITO ($\Delta W_{\mathrm{F}} \approx 200 - 400\,eV$), the contact resistivity to the p-type a-Si:H emitter is expected to be worse compared to its ITO pendant. Furthermore contact materials with the lower work functions lead to a decrease of the band bending, induced by the p-type a-Si:H emitter, within the n-type c-Si wafer and a reduction of charge carrier lifetime at lower injection levels. Both reduces the FF potential of the solar cell [151].

Tungsten Oxide features a high work function (>5 eV) and should thus be suitable to form an excellent contact to the p-type a-Si:H emitter (see Figure 5.13). WO_X is only one of multiple candidates to not only replace ITO as the standard TCO on top of p-type a-Si:H emitter layers, but also replace the a-Si:H emitter itself, as the band bending necessary to extract minority charge carriers from the n-type c-Si wafer can also be induced by the corresponding metal oxide. Alongside WO_X, materials

like vanadium and molybdenum oxide have been evaluated in various heterojunction configurations [164–168].

In this work, WO_X layers are used as a thin interlayer between the p-type a-Si:H emitter and the ITO. A layer thickness of 20 nm was chosen to minimise parasitic absorption in the WO_X layer while also maintaining the high work function at the a-Si:H interface, as for thinner layers the presence of the ITO nullifies the effect of the WO_X [163].

The properties of the WO_X layer heavily depend on the amount of oxygen present in the tungsten sputter process. Figure 5.14 shows the oxygen dependency of the conductivity and the absorption of the corresponding WO_X layers. Very oxidic WO_X layers exhibit a rather high specific resistivity values in the range of 50 Ωcm, which is orders of magnitudes higher than the ones for ITO and AZO. The transmission values in these cases are on a level similar to the one of ITO. Decreasing the oxygen gas flow in the process drastically decreases the resistivity but also increases the parasitic absorption considerably. The tungsten oxide layers used in the IBC SHJ solar cells presented in this work were deposited with a very low oxygen gas flow of 1 sccm in order to yield optimal electrical properties.

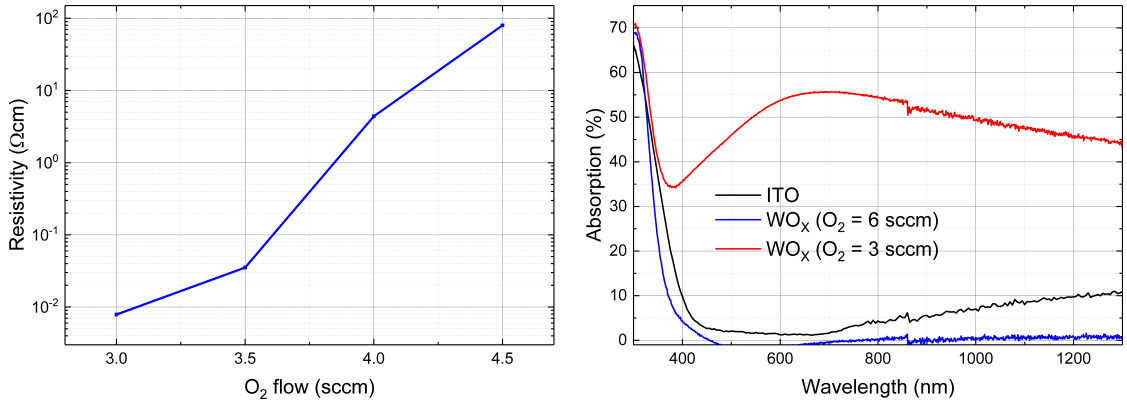


Figure 5.14: a) Dependency of the resistivity of WO_X layers on the O_2 gas flow: the resistivity increases by several orders of magnitude when the O_2 gas flow is increased from 3 to 4.5 sccm. b) Absorption spectra of two WO_X layers sputtered with different O_2 gas flows compared to an ITO reference: the transparency of WO_X layers decreases with lowering the O_2 gas flow [133].

5.4.2 a-Si:H Passivated Front Side

The solar cells presented in the previous subchapter all featured a front side layer stack consisting of two silicon nitride layers, differing in thickness and refractive index (see section 4.2.3). While yielding decent optical properties, as illustrated by the reflection data in Figure 5.15, the effective lifetime of symmetrically passivated test samples did

not exceed 1.5 ms (1 ms for the batch 1 devices including the ITO/Ag reference cell analysed in section 5.3). The lack in passivation quality limits both V_{OC} and FF. The FF benefits particularly from higher effective minority charge carrier lifetimes, as the currently achieved V_{OC} values are closer to the respective Auger-limit than the ones for the FF ($FF_{Auger} = 89.3\,\%$, $V_{OC,Auger} = 761\,mV$).

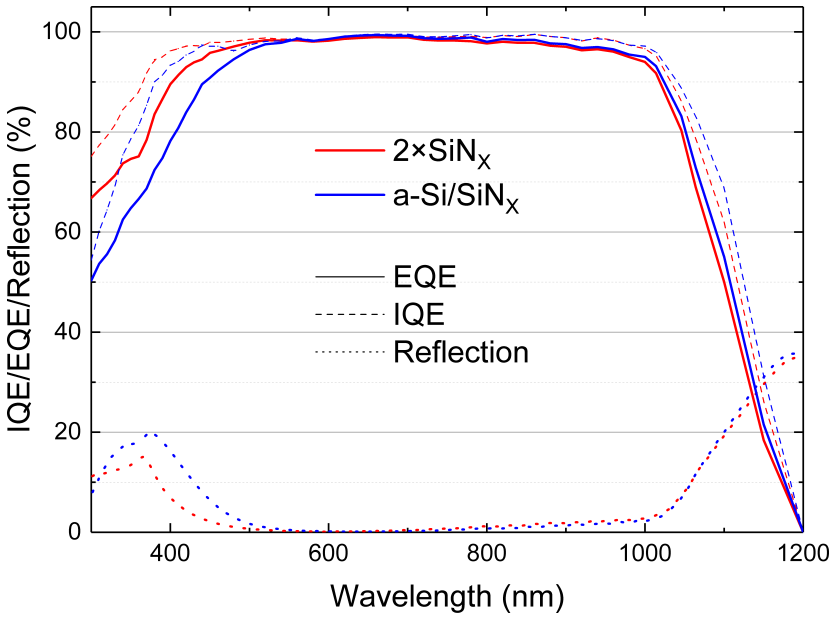


Figure 5.15: EQE, IQE and reflection spectra of the double-layer SiN_X and the a-Si:H passivated front side [148].

To improve the passivation quality of the front side layer stack, the passivating silicon nitride was therefore replaced by an intrinsic a-Si:H layer, providing a much better passivation quality (cell precursor effective lifetimes of up to 6 ms). A single SiN_X layer on top of the intrinsic a-Si:H then ensures the necessary anti-reflective properties. Figure 5.15 shows the EQE, IQE and reflection spectra for an Al cell (batch 2), featuring the double-layer SiN_X front side, and an ITO/Ag cell featuring the a-Si:H passivated front side.

A stack of two SiN_X layers allows for a better refractive index grading, leading to a lower reflection in the wavelength range below 500 nm. This is also reflected in the EQE signal, which in this region is considerably lower for the front side featuring an intrinsic a-Si:H passivation. Since the band gap of amorphous silicon is smaller than the one of silicon nitride (1.7 eV vs. 5 eV), the a-Si:H passivation layer parasitically absorbs part of the incoming light, visualised by the difference of the IQE spectra in the lower wavelength range. The integration of the respective EQE curves yields j_{SC} values of about 41.5 mA/cm^2 for both approaches, indicating that the ITO/Ag device, featuring the a-Si:H passivated front side, compensates the losses in the lower wavelength range

(worse reflection and increased parasitic absorption) by mitigating plasmonic absorption losses at the rear side ($\Delta j_{SC,<500nm} = -0.4\,mA/cm^2$, $\Delta j_{SC,>1000nm} = +0.3\,mA/cm^2$). The j_{SC} value of $41.5\,mA/cm^2$ is still approximately $1\,mA/cm^2$ lower than the one of the best IBC SHJ solar cell published. Combining the batch 2 double-layer silicon nitride front side with an ITO/Ag rear side metallisation might partially reduce this gap, but at the expense of passivation quality and thus V_{OC} and FF. To maintain the level of passivation of the front side layer stack while improving its optical properties the thickness of the a-Si:H and the refractive index of the SiN_X layer need to be optimised further. The addition of multiple anti-reflective layers represents another viable optimisation option.

The solar cells analysed in the following all feature the a-Si:H passivated front side as presented in this section and 4.2.3.

5.4.3 Emitter/BSF Variation

The a-Si:H passivated front side layer stack is deposited in the AKT (see subsection 4.1.1), prior to the initial emitter layer stack. The latter differs from its FAP tool counterpart, as it is more conductive ($2.6{\cdot}10^{-5}$ vs. $1{\cdot}10^{-5}\,S/cm$) while also incorporating a graded doping profile. The doping density within the initially deposited layer is comparably low, to affect the Fermi level within the underlying intrinsic a-Si:H layer as little as possible and thus mitigating the degradation of the passivation quality [61, 127]. The subsequently deposited layer features a rather high doping density to facilitate the formation of a tunnel-recombination contact with a TCO material usually being a degenerate n-doped semiconductor [63].

The BSF layer based on n-type amorphous silicon was replaced by a hydrogenated nanocrystalline silicon (nc-Si:H) layer. The latter's conductivity values are four orders of magnitude higher than the ones of its amorphous pendant ($30\,S/cm$ vs. $5\cdot10^{-3}\,S/cm$) [118]. This drastic increase is expected to further lower the contact resistivity to the ITO layers and reduce the overall series resistance. This is indeed reflected by TLM measurements – $0.12\,\Omega cm^2$ for n-type a-Si:H/ITO and $0.08\,\Omega cm^2$ for n-type nc-Si:H/ITO – however, a potential difference between the two TLM structures with respect to the thickness of the intrinsic a-Si:H layers might have skewed the results. Since the solar cells presented in this thesis were essentially never limited by the BSF contact, the actual influence of the nc-Si:H was not fully investigated. The increased conductivity of the BSF layer also influences the shunt resistance. Emitter and BSF layer overlap, thus in the case of an nc-Si:H BSF layer, only the p-type a-Si:H emitter acts as a sufficiently insulating barrier between the two contacts. Consequently the usage of a p-type nanocrystalline emitter would require either the BSF to be amorphous

again or redesigning of the contact geometry involving an insulation layer in-between emitter and BSF.

5.4.4 Illuminated Current–Voltage Measurements

V_{OC} and j_{SC} Table 5.6 lists the jV parameters of IBC SHJ solar cells having identical a-Si:H/nc-Si:H layers, but different TCO configurations. Furthermore, the data of the initially presented ITO/Ag reference solar cell, already analysed in subsection 5.3.1, is shown. It is apparent that the increase in passivation quality, a consequence of introducing an intrinsic a-Si:H passivation layer to the front side layer stack as well as using different PECVD recipes for the rear side a-Si:H layers, resulted in a drastic increase in V_{OC} (almost 30 mV). The V_{OC} values of the solar cells listed above are still limited by their small cell area (1 cm^2) and the relatively thick wafers (280 μm). The photolithography mask design also includes one cell with an area of 4 cm^2. These cells have achieved V_{OC} values of up to 719 mV, but their FF is limited by an unfavourable emitter ratio (52 %). Standard SHJ solar cells with a cell area of 4 cm^2, built on thinner Czochralski wafers with identical a-Si:H recipes (apart from the emitter/BSF deposition time), regularly reach V_{OC} values above 730 mV [116, 117].

Table 5.6: jV parameters (solar cells under illumination)

TCO	j_{SC} mA/cm^2	V_{OC} mV	FF %	η %
ITO (old)	40.5	687	69.1	19.2
ITO*	41.5	711	73.1	21.5
ITO	42.0	716	74.5	22.4
AZO	41.9	715	72.2	21.6
WO_X/ITO	41.3	713	74.8	22.0

*non-graded emitter

As already stated in subsection 5.4.2, the a-Si:H passivated front side in combination with the rear side ITO yields j_{SC} values of around 41.5 mA/cm^2. AZO layers at the rear side, being more transparent and in this particular cell thinner than the ITO equivalent (70 nm vs. 150 nm), lead to j_{SC} values up to 41.9 mA/cm^2. EQE measurements of the corresponding solar cells, depicted in Figure 5.16, verify that the increased j_{SC} can be ascribed to the better near-infrared response of the AZO cell: subtracting the integrated EQE data with a wavelength greater than 1000 nm of the AZO cell from the ITO cell equals an advantage of 0.4 mA/cm^2 in favour of the former.

The second ITO cell listed in Table 5.6 exhibits an unusually high j_{SC} value of 42.0 mA/cm^2, despite using the same ITO as a rear side TCO. This is contradicting to

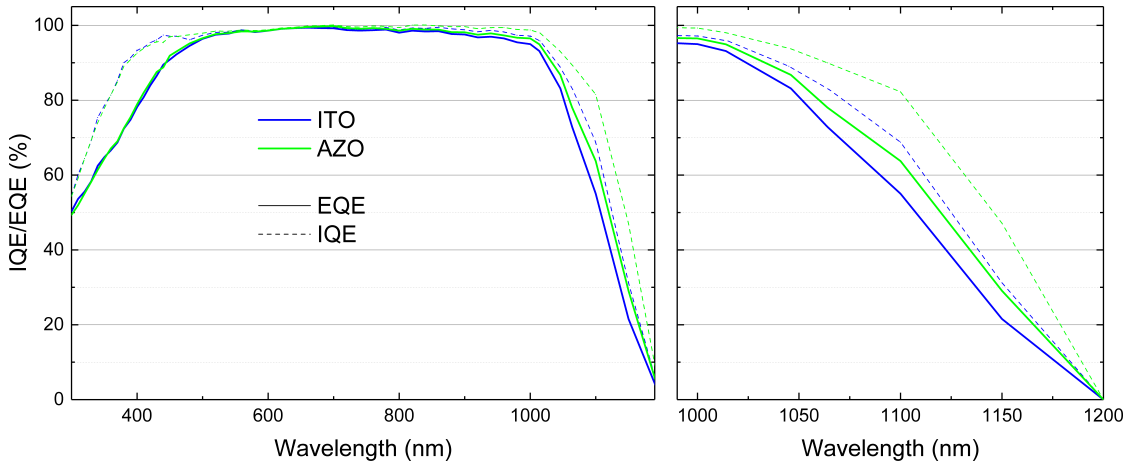


Figure 5.16: EQE and IQE spectra of the ITO (non-graded emitter) and AZO cell. a) Since both cells feature the same front side and a-Si:H passivation there are little to no differences in the lower and medium wavelength range. b) Owing to its higher transparency the AZO cell suffers less from parasitic absorption hence the EQE/IQE signal is higher in the wavelength range greater 1000 nm [148].

the other ITO cells built with the same process and structure that all average around 41.5 mA/cm^2 (+/- 0.2 mA/cm^2). While the manual calibration of the solar simulator induces a certain inaccuracy, deviations of 0.5 mA/cm^2 are rather unusual.

Including a 20 nm WO_X layer in-between the p-type a-Si:H emitter and the rear side ITO layer reduces the j_{SC}. Being sputtered with a low oxygen gas flows, the WO_X layer absorbs a significant amount of the infrared light. As only the p-contact area is affected, the eventual loss also depends on the emitter ratio. With this value being only 52 % for this particular cell, the loss in j_{SC} is comparatively small (0.2 mA/cm^2).

Fill Factor Analogous to section 5.3.1, the fill factor and the related loss contributions can be analysed by comparing the implied FF, the pseudo FF and the FF extracted from the jV measurements. The corresponding data alongside the respective series resistances (averaged from the two methods described in subsection 3.2.6) is shown in Table 5.7. The two depicted ITO cells differ with respect to their emitter layer: the cell featuring a graded emitter exhibits a slightly lower series resistance and thus a higher FF than the one without, likely related to an improved tunnel-recombination contact between the emitter and the ITO layer. This assumption is further backed as the pFF values of both cells are identical and the iFF values are close together, indicating a similar level of passivation.

The AZO cell listed in Table 5.7 differs from the one listed in Table 5.6, as the latter was damaged during the EQE measurement prior to the Suns-V_{OC} measurement. The cell with a FF of 72.2 % exhibits an emitter ratio of 77 %, the one with a FF of 71.2 %

Table 5.7: FF analysis

TCO	iFF %	pFF %	FF %	|pFF - FF| %abs	$R_{\mathrm{Ser,Total}}$* $\Omega\mathrm{cm}^2$	Emitter ratio %
ITO**	83.5	83.4	73.1	10.3	1.8	65
ITO	84.1	83.4	74.5	8.9	1.5	65
AZO***	83.6	83.8	71.2	12.6	2.2	86
$\mathrm{WO_X}$/ITO	84.3	83.6	74.8	8.8	1.4	52

*averaged from two methods
**non-graded emitter
***different cell compared to Table 5.6

an emitter ratio of 86 %. V_{OC} and j_{SC} are identical. The reduced FF of the AZO cells is likely related to the lower work function of AZO material and the thus less efficient tunnel-recombination contact to the p-type a-Si:H emitter. The FF losses of the AZO cells seem to be entirely driven by series resistance related effects, as the iFF and the pFF are practically identical (the latter is even higher than the former, which is likely a result of measurement inaccuracies).

At first glance the results of the cell containing $\mathrm{WO_X}$ do not differ from the equivalent ITO cell (graded emitter one). Both the series resistance and the FF are in the same range with minor deviations being explained by measurement inaccuracies. However the fact that the best cell result is achieved with an emitter ratio of 52 % hints at the possibility of a further improved p-contact resistivity, as the optimum ratio for pure ITO cells is usually in the range of 65 %.

Series Resistance Table 5.8 contains a breakdown of the series resistance including the contributions of the two contacts for the solar cells listed in Table 5.7. Analogous to the analysis in section 5.3.1, the n-contact resistivity, $\rho_{\mathrm{N,TLM}}$, is measured using the TLM method with corresponding structures on the wafers next to the cells. The resulting share of the contact resistance for the n-contact, $R_{\mathrm{Ser,N}}$, is then calculated by dividing the measured contact resistivity by the respective *BSF ratio* or contact fraction. The equivalent for the p-contact, $R_{\mathrm{Ser,P}}$, is given by the subtraction of $R_{\mathrm{Ser,N}}$ and $0.1\,\Omega\mathrm{cm}^2$ (transport losses in the wafer/emitter) from the total series resistance $R_{\mathrm{Ser,Total}}$, as obtained from applying the methods described in subsection 3.2.6. The result multiplied by the area fraction of the p-contact (emitter ratio, equal to $1-$ *BSF ratio*) gives the calculated p-contact resistivity $\rho_{\mathrm{P,calc}}$. Compared to the measured p-contact resistivities listed in Table 5.2, the calculated values are roughly in the same range. Inaccuracies and deviations between the calculated and the measured contact resistivities are likely

related to the poor linearity of the jV characteristics for some TLM measurements and furthermore, also arise from the fact that separate p-type TLM samples had to be manufactured instead of being a byproduct of the solar cell fabrication, as it is the case for the n-type ones. The necessity to use p-type c-Si wafers results in different growth conditions of the a-Si:H layers. Different wafer surfaces further constitute another vital difference (textured AZO-TLM samples vs. polished AZO solar cells).

Table 5.8: R_S analysis

TCO	$R_{Ser,Total}$ Ωcm^2	BSF ratio %	$\rho_{N,TLM}$ Ωcm^2	$R_{Ser,N}$ Ωcm^2	$R_{Ser,P}$ Ωcm^2	$\rho_{P,calc}$ Ωcm^2
ITO*	1.8	35	0.08	0.23	1.47	0.96
ITO	1.5	35	0.08	0.23	1.17	0.76
AZO	2.2	14	0.06	0.43	1.67	1.44
WO_X/ITO	1.4	48	0.08	0.23	1.13	0.59

*non-graded emitter

Nevertheless the trend of substantially lower contact resistivities for the n-contacts, as already observed for the solar cells with a direct aluminium/a-Si:H contact, is present for the TCO-based solar cells as well. Comparing the calculated p-contact resistivities of the different TCO/emitter combinations, significant differences can be observed. The contact resistivity between the ITO and the graded emitter is approximately 20 % lower than the one without a graded emitter. Including a WO_X layer in-between the two further improves the contact resistivity by 22 %. In contrast, the p-contact resistivity of the AZO/emitter interface is almost twice as high as the one for the ITO (both featuring a graded emitter). To achieve FF values reasonably close to the ones of the ITO cells, the high contact resistivity is compensated by increasing the ratio of the p-contact area.

5.4.5 Solar Cells with a Textured Rear Side

The introduction of a new front side and the switch to AKT-based a-Si:H and nc-Si:H layers have led to an improvement of the cell efficiency by roughly 3 %abs (see Table 5.6). According to the analysis of the FF and the series resistance, the cell performance is still strongly limited by the latter, and here by the p-contact resistivity in particular.

Switching from a polished to a textured rear side should lead to a decrease of the overall series resistance, as the effective area of textured surfaces is larger than the one of polished ones. Depending on the size, shape and distribution of the pyramids the effective area increases by up to 70 %. Assuming constant contact resistivities, the

increase in area should lower the resulting total contact resistance by the same amount, thus also decreasing the overall series resistance.

Textured rear sides also yield an advantage in terms of the optical properties of the solar cell's rear side, as the light reflected at the rear metal electrodes is scattered, which enhances the optical response and thus increases the j_{SC}.

A drawback of using textured rear sides is the increased manufacturing complexity. Using polished surfaces simplifies the alignment procedure of the photolithography process, which is based on optical microscopy and thus depends on the reflection properties of the rear side. Furthermore, amorphous and nanocrystalline silicon layers exhibit a greater thickness homogeneity when deposited on polished surfaces, as the growth conditions are equal across the entire surface. On a surface textured with random pyramids, different growth conditions apply to the valleys, the sides, and the top of the respective pyramids leading to thickness inhomogeneities, especially if the pyramids itself vary with respect to their size (see also subsection 4.2.2).

Table 5.9: jV parameters (solar cells under illumination)

	j_{SC} mA/cm^2	V_{OC} mV	iFF %	pFF %	FF %	$R_{Ser,Total}$ Ωcm^2	Emitter ratio %	η %
ITO/tex	42.2	719	83.1	82.1	76.1	1.1	52	23.1

The alkaline etch process used to texture the rear side yielded mostly pyramids with an average height around 1 μm, but also including a significant amount exhibiting heights up to 6 μm and faceted sides that are prone to epitaxial growth and thus more difficult to passivate. Therefore the initial passivation quality is worse compared to polished samples. Additionally thickness of the intrinsic layer for the repassivation step (BSF deposition after emitter structuring) had to be increased in order to maintain the initial passivation level. Consequently the n-contact resistivity increased to 0.11 Ωcm^2, which partially compensates the FF gain expected from the increased effective area, hence the modest increase in FF (1.6 %abs, from 74.5 to 76.1 %). Table 5.9 lists the relevant parameters of the IBC SHJ solar cell with a textured rear side. Given the initially measured passivation level ($\tau_{eff} \approx 1.5$ ms), the V_{OC} is remarkably high. Since the TrPCD measurement refers to the middle portion of the wafer rather than to the specific cell, it is possible that the passivation level in the actual cell area is higher than the TrPCD measurement suggests. The improved light scattering at the rear side is reflected by a j_{SC} greater than 42 mA/cm^2.

5.4.6 Optimising Intrinsic a-Si:H Layer Thickness

The measures outlined in the previous chapters (optimised front side layer stack and a-Si:H rear side layers, different TCO materials) focused mainly on improving the FF by increasing the passivation level and optimising the emitter/TCO interface. As outlined in subsection 5.2.3, the intrinsic a-Si:H passivation layer, an integral part of a SHJ structure, can have a drastic influence on the solar cell's FF. As described in subsection 2.2.2, the width of the energetic barriers caused by the presence of the intrinsic a-Si:H layer (the valence band offset ΔE_{V} for the holes, and the conduction band offset ΔE_{C} for the electrons) is usually decreased by the band bending induced by the doped emitter and BSF layers. Consequently, the charge carriers can overcome these barriers either by thermionic emission, hopping or tunnelling [46]. A too thick intrinsic a-Si:H layer will impede these transport mechanisms, eventually leading to an S-shaped jV curve. The jV curves of the solar cells presented so far did not exhibit S-shapes (with the exception of the initial ITO/Ag cell), indicating decent current extraction. On the other hand, too thin intrinsic a-Si:H layers result in an insufficient passivation quality, deteriorating both the V_{OC} and the FF.

Further optimisation of the intrinsic a-Si:H layers thus aims to reduce its thickness while still maintaining a sufficient passivation level. Since it is difficult to accurately measure the thickness of these very thin a-Si:H layers (the absolute thickness is in the range of 4 to 6 nm), an empirical optimisation was performed, involving the fabrication of lifetime samples with varying deposition times.

Table 5.10: jV parameters (solar cells under illumination)

	j_{SC}	V_{OC}	iFF	pFF	FF	$R_{\mathrm{Ser,Total}}$	Emitter ratio	η
	mA/cm^2	mV	%	%	%	Ωcm^2	%	%
ITO/opt.	41.3	713	82.9	82.6	78.5	0.6	65	23.2

Table 5.10 lists the parameters of an IBC SHJ solar cell featuring a polished rear side and a substantially thinner intrinsic a-Si:H layer (reduction of the deposition time from 28 to 22 s), compared to the solar cells analysed in subsection 5.4.4. The j_{SC} as well as the V_{OC} value are slightly lower than the average of previous ITO cells (715 mV, 41.5 mA/cm^2), but these deficiencies are overcompensated by an FF of 78.5 %. The high FF value is the result of a drastically decreased series resistance. The n-contact resistivity measured with the TLM structure on the cell wafer amounts to 0.03 Ωcm^2. The calculation of the corresponding p-contact resistivity yields 0.27 Ωcm^2, which is well in the range of the values measured with respective *textured* p-type TLM structures.

5.4.7 Conclusions

The results can be summarised as follows: the efficiency of the TCO based IBC SHJ solar cells was improved by 4 %abs, from 19.2 % to 23.2 %. The increase in V_{OC} (+30 mV) and j_{SC} (+1 mA/cm^2) can be largely attributed to the drastic increase in passivation quality as a result of improved a-Si:H deposition recipes and the introduction of an a-Si:H passivation layer at the front side. FF values increased the most (+9.4 %abs), both by providing a higher FF potential (implied FF) as a result of the improved passivation quality and by drastically reducing the series resistance. The latter depends mostly on the contact resistivity of the amorphous or nanocrystalline silicon layers to the TCO material, as the bulk lifetime within the wafer is sufficiently high, resulting in a minority carrier diffusion length in the range of the pitch of the photolithography based solar cells (1.2 mm). TLM measurements have shown, that both ITO and AZO are able to form sufficiently good contacts to the nc-Si:H BSF layer (<0.06 Ωcm^2). On the p-side, the contact resistivity between the graded a-Si:H emitter and the ITO averages around 0.25 Ωcm^2, which is considerably higher than its n-counterpart. Owing to its lower work function, AZO exhibits a much higher contact resistivity to the same emitter layer than ITO (around 0.75 Ωcm^2 on average). As a result of the discrepancy between the n- and p-contact resistivity, solar cells with an emitter ratio between 64 % and 77 % tend to be more efficient than the ones with a roughly equal distribution of n- and p-contact area. As the dependency of the emitter ratio on the contact resistivities follows a square-root function, emitter ratios greater than 80 % are only beneficial if the p-contact resistivity is at least 20 times higher than its n-counterpart, hence solar cells with the highest emitter ratio (86 %) usually did not yield the highest efficiencies.

Initial tests with WO_X layers in-between emitter and ITO yield promising results, as FF and p-contact resistivity values are on a similar if not slightly better level than the ones of comparable ITO cells. In its current state, the WO_X layer's lack of transparency has a detrimental effect on the j_{SC}, thus further optimisation is necessary.

The thickness optimisation of the intrinsic a-Si:H passivation layer is of utmost importance. Substantially reducing the thickness of this layer, without deteriorating the passivation quality, increased the FF by around 4 %abs for solar cells with a polished rear side.

Switching to a textured rear side leads to an effective increase of the rear side area, with positive effects for the V_{OC}, the j_{SC}, and the FF. To fully exploit the potential of textured rear sides, a texturing process yielding a more homogeneous distribution of equally sized and non-faceted pyramids is necessary.

In comparison to Kaneka's world record cell, the current solar cell design primarily lacks FF (78.5 vs. 84.9 %) and V_{OC} (713 vs. 738 mV) [30]. To a large extent the

latter is limited by the small cell area (1 cm^2) and the wafer thickness (280 μm) [169]. Increasing the FF further poses a much greater challenge. Kaneka's cell features both a very high iFF and pFF (86.6 and 85.8 %), and an extremely low series resistance of approximately 0.2 Ωcm^2. To improve the iFF/pFF of the current solar cell design, the lifetime degradation induced by the different patterning processes - passivation, etching, cleaning, repassivation, as illustrated in subsection 4.2.3 - needs to be addressed. Switching to a shadow mask process and thus omitting the unfavourable repassivation step necessary in the photolithography process, represents a possible solution. A reduction in series resistance relies on further decreasing the contact resistivity of the silicon/TCO interface, especially on the emitter side. Using a dedicated TCO material for the p-contact, i.e., a metal oxide like WO_X, might be a solution for this particular problem.

5.5 Non-Photolithography Solar Cells

The IBC SHJ solar cell results presented in the following were manufactured with the shadow mask process, described in section 4.3. As the process itself has not been optimised, these initial results primarily illustrate the general viability of the shadow mask approach while at the same time revealing existing flaws.

Initial shadow mask based IBC SHJ solar cells were manufactured using the Altatech-PECVD tool, owing to its greater customisation possibilities and better availability. Being set up only months before these experiments, the respective a-Si:H process recipes at the time exhibited a different degree of optimisation compared to the AKT ones, resulting in an efficiency difference of roughly 3 %abs for corresponding standard SHJ solar cells. PL and lifetime data after the a-Si:H deposition, depicted in Figure 5.17, nevertheless indicate a sufficient level of passivation. The large amount of dark spots on the PL image is likely related to the manual handling during the edge alignment procedure (see section 4.3.4).

The metallisation stack consists of a sputtered AZO layer and a screen-printed silver layer. AZO was chosen over ITO as it does not crystallise during the obligatory curing step following the printing of the silver paste (190 °C for several minutes) thus simplifying the subsequent etching process.

Table 5.11 lists the parameters of three mask based IBC SHJ solar cells. The corresponding jV curves are shown in Figure 5.18. V_{OC} and j_{SC} both reach an acceptable level ($\approx$700 mV and >40 mA/cm^2) with the V_{OC} being on a par with Altatech-based standard SHJ solar cells and only approximately 15 mV behind the AKT-based pho-

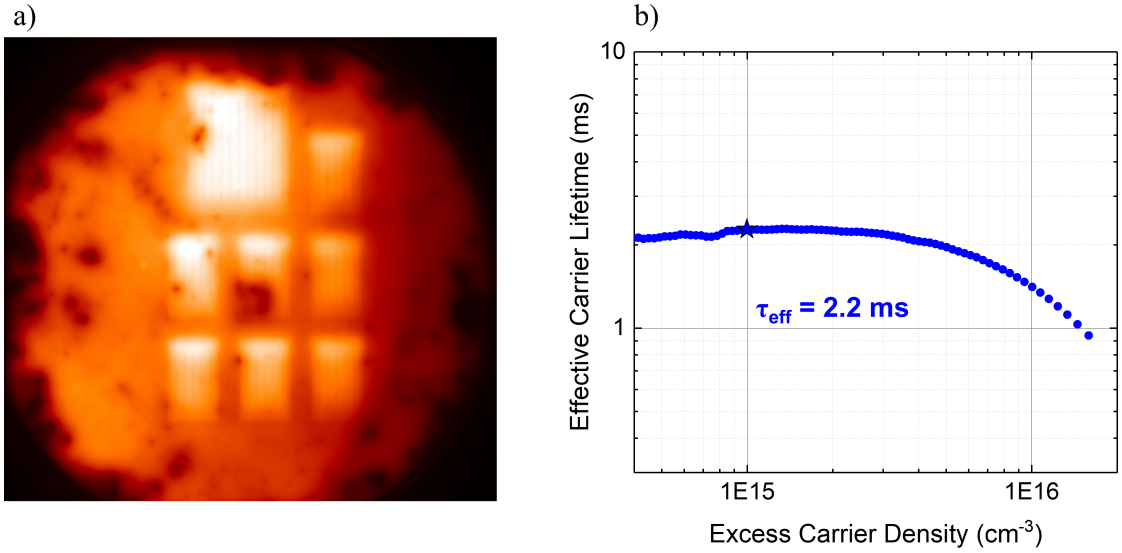


Figure 5.17: a) PL image of the respective cell precursor after the deposition of the patterned a-Si:H layers. b) TrPCD measurement.

Table 5.11: jV parameters (solar cells under illumination)

Metallisation Gap μm	j_{SC} mA/cm^2	V_{OC} mV	pFF %	FF %	η %
200	41.4	699	83.3	28.8	8.3
400	41.2	702	83.3	32.2	9.3
600	40.8	695	n/a	29.6	8.4

tolithography reference devices. In contrast to that the FF (32.2 % at maximum) is particularly low. Although larger metallisation gaps are expected to be detrimental to the FF as the series resistance increases, the contact geometry does not seem to be a limiting factor. The highest FF is achieved with a metallisation gap of 400 μm, and the FF difference between a metallisation gap of 200 and 600 μm is insignificant. The strongly S-shaped jV curves rather point to a non-linear transport barrier either related to an intrinsic a-Si:H layer being too thick or a malfunctioning emitter/TCO tunnel-recombination contact. The latter is likely, as the analysis in the previous subchapter showed that this particular AZO forms a comparatively poor contact to the AKT-based a-Si:H emitter. With the less conductive Altatech emitter the conditions for a working tunnel-recombination contact are impaired further, as the latter relies on the very strong band bending at the emitter/TCO interface. Since the Altatech tool, in its early days, exhibited rather high fluctuations of the deposition rate within a the first few seconds of the process, a too thick intrinsic a-Si:H passivation layer remains a possibility as well.

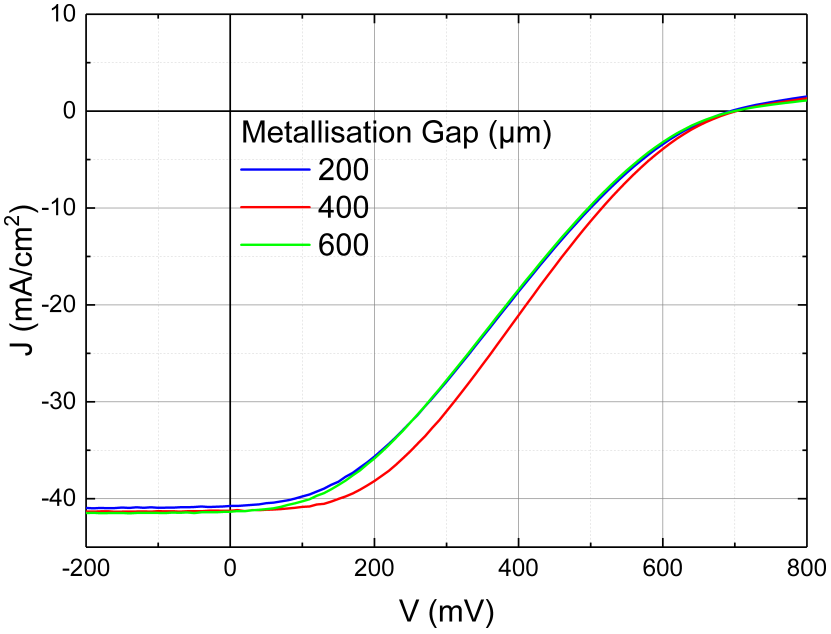


Figure 5.18: jV curves of the first batch of IBC SHJ solar cells manufactured by the shadow mask process. The cells differ only with respect to their metallisation gap.

The second batch of mask based IBC SHJ solar cells was manufactured using standard AKT recipes (identical to the ones used for photolithography-based solar cells), the pin hole alignment method (see section 4.3.4), and an ITO/Ag metallisation patterned with the pseudo-photolithography approach (see section 4.3.5). In contrast to the screen-printing approach the latter allows for very narrow metallisation gaps, which is favourable in order to reduce the series resistance by increasing the contact area and decreasing the distance charge carriers have to travel within the wafer to reach their respective contact. However, if the simultaneous presence of narrow metallisation gaps and underdeposition effects lead to the metallisation of overlap regions, the solar cell is shunted, as the jV-curve in Figure 5.19 demonstrates. In combination with AKT a-Si:H processes that exhibit little underdeposition effects, the metallisation gap was enlarged to values of at least 120 μm ensuring non-metallised overlap regions and thus shunt-free solar cells.

Table 5.12: jV parameters (solar cells under illumination)

Metallisation Gap μm	j_{SC} mA/cm^2	V_{OC} mV	iFF %	pFF %	FF %	$R_{Ser,Total}$ Ωcm^2	η %
120 - 150	41.7	616	83.8	81.1	66.3	1.5 - 2.3	17.0
120 - 150	41.4	617	83.8	80.6	65.1	n/a	16.6

The lifetime data and the PL image of the related cell precursor, patterned with shadow masks using the pin-hole alignment method, are shown in Figure 5.20. The solar

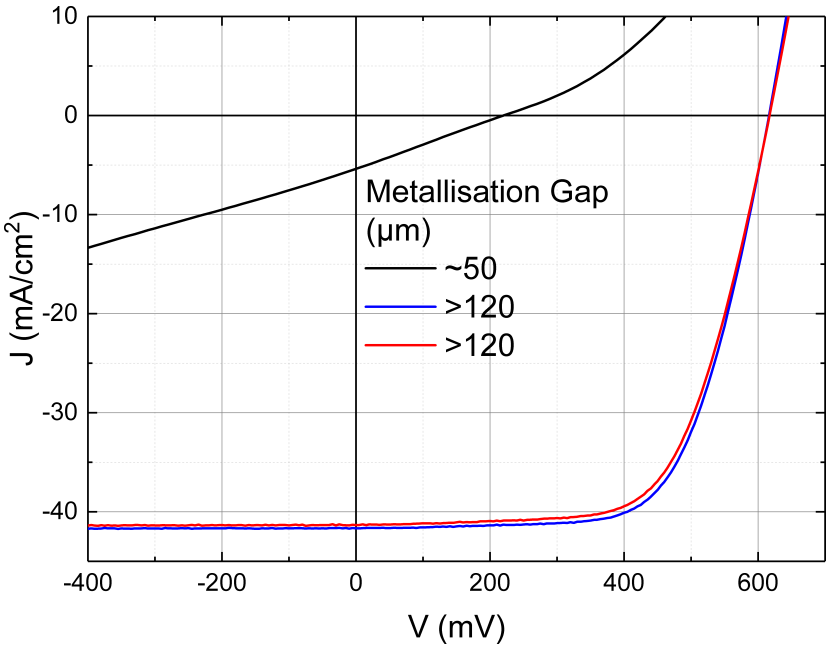


Figure 5.19: jV curves of the second batch of IBC SHJ solar cells manufactured the shadow mask process. Metallisation gaps significantly smaller than 100 μm lead to the metallisation of overlap regions and thus severe shunting.

cell parameters are summarised in Table 5.12. In comparison to the initial mask based cells, the V_{OC} is approximately 80 mV lower, while the FF is roughly twice as high. The latter is the consequence of using the AKT a-Si:H processes guaranteeing optimal intrinsic a-Si:H thicknesses and an efficient emitter/TCO contact. The low V_{OC} is likely caused by an insufficient emitter passivation, as apparent in the PL image, where the emitter regions appear considerably darker than the BSF ones and surrounding regions passivated by intrinsic a-Si:H only. The exact reason for the passivation loss in the emitter regions is unknown. It may arise from a contamination effect, as during the initial BSF deposition the BSF mask is in direct contact with the intrinsic a-Si:H passivation layer in the designated emitter regions. The silicon hard masks are not RCA cleaned, but only annealed at up to 600 °C, dipped into hydrofluoric acid (HF, 1 % in H_2O), and afterwards stored under normal atmospheric conditions. To reduce the possibility of contamination in future processes, the BSF and the emitter mask should be coated with intrinsic a-Si before the respective patterning processes.

5.5.1 Conclusions

The initial results of the solar cells manufactured with different variations of the shadow mask process are promising. Patterned cell precursors exhibited effective minority charge carrier lifetimes of up to 4 ms, and solar cells V_{OC} values above 700 mV. While

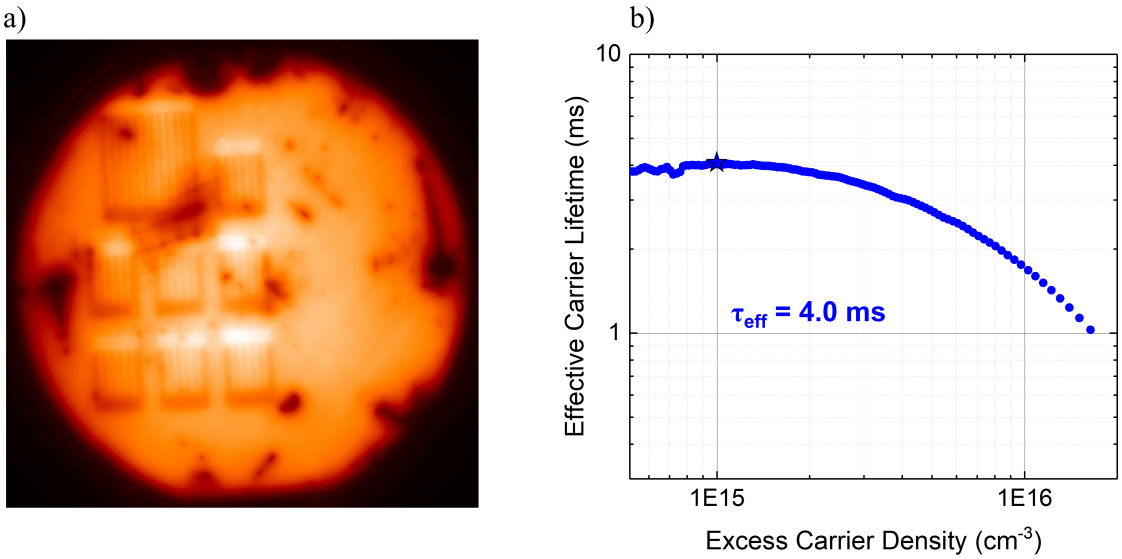


Figure 5.20: a) PL image of the respective cell precursor after the deposition of the patterned a-Si:H layers. b) TrPCD measurement.

certainly not beneficial, metallisation gaps in the range of 100 to 200 μm most likely lead to an only moderate increase in series resistance. Since the FF values of the best performing solar cells are also limited by an insufficient emitter passivation, it is difficult to differentiate between these two loss contributions. The emitter passivation loss might be related to contamination effects arising from the mask material, but additional experiments are necessary to confirm this assumption.

To further develop and improve the process, aiming for lower overlap widths and metallisation gaps, a general optimisation of the design of the masks or screens used for both the a-Si:H patterning and the metallisation is necessary.

5.6 Chapter Summary

The majority of this chapter is dedicated to the optimisation of IBC SHJ solar cells built with the photolithography process. A particular emphasis is put on the back contact design, especially the metallisation.

Cells with direct aluminium/a-Si:H contacts outperform their equivalent ITO/Ag counterparts (19.2 vs. 20.7 % efficiency), and with an improved front side passivation, aluminium-based cells achieve efficiencies up to 22 %. The performance of the aluminium-based cells depends strongly on the annealing time and temperature. Moderate annealing (150 to 160 °C, 10 to 30 minutes) results in the formation of an intermediate silicide layer between the aluminium and the amorphous silicon, also initialising the crystallisation of the latter. The contact resistivity benefits from both these effects, consequently leading

to a decrease of the overall series resistance and an increase of the FF. Further annealing, in particular at higher temperatures (170 °C and more), results in the disintegration of the amorphous silicon layers as the consequence of strong interdiffusion effects. Following the lack of passivation, a substantial decrease of the V_{OC}, which is not compensated by a further FF increase, can be observed.

The efficiency analysis of the ITO/Ag reference device revealed limitations concerning the passivation quality (as indicated by a low iFF, V_{OC}) and j_{SC}) and the high series resistance (low FF). The latter is mainly the result of a high p-contact resistivity, the former relates to a poorly passivated front side. By replacing the front side layer stack based on a SiN_X double-layer with one consisting of an intrinsic a-Si:H passivation layer and a single-layer SiN_X ARC, the passivation quality was substantially improved, yielding cell precursor effective lifetimes of up to 6 instead of the former 1 to 1.5 ms. Contact resistivities to the TCO were improved by increasing the conductivity of both the emitter and the BSF layer (in the latter case by switching to a nanocrystalline instead of an amorphous one). Additionally different TCO materials were evaluated: the highly conductive ITO forms a good contact to the p-type emitter layer, but also limits the j_{SC}, due to parasitic absorption in the near infrared wavelength range; the very transparent AZO shows the inverse behaviour, as compared to equivalent ITO devices the j_{SC} increases by 0.4 ma/cm^2, but the FF suffers from a strong increase of the p-contact resistivity. A WO_X layer between the emitter and the TCO layer decreases the p-contact resistivity slightly, but also the j_{SC}, as the amount of oxygen in the layer is low favouring conductivity over transparency. A further reduction in the overall series resistance is achieved by decreasing the thickness of the intrinsic a-Si:H passivation layer at the rear side, thus enhancing the charge carrier extraction from the wafer, and also by switching from a polished to a textured rear side, which enlarges the contact area.

The first IBC SHJ solar cells based on the shadow mask process, outlined in section 4.3, achieved V_{OC} values above 700 mV and j_{SC} above 40 mA/cm^2, but the efficiency (around 10 %) is strongly limited by very low FF values (around 30 %) resulting from S-shaped jV curves. The latter are most likely the consequence of a malfunctioning emitter/TCO contact or a too thick intrinsic a-Si:H passivation layer. In a second batch, the efficiency was improved to 17 %, owing to a reworked metallisation scheme and rear side amorphous (nanocrystalline, respectively) layers equivalent to the ones used in the best photolithography-based cells. While the FF of these cells improved drastically (up to 66 %), the V_{OC} decreased substantially (down to 616 mV), as a consequence of the degradation of the emitter passivation during the metallisation process.

Chapter 6

Prospects of IBC SHJ Solar Cells

It is apparent that the efficiency growth potential for interdigitated back contact heterojunction solar cells is limited. With an efficiency of 26.7 % recent results of IBC SHJ solar cells are remarkably close to the modelled theoretical limit of 29.4 %. While an efficiency increase up to efficiencies above 27 % is certainly within the realms of possibility, the main future challenge with respect to the IBC SHJ technology is not solely to further push the boundaries in terms of efficiency but also to establish a manufacturing process enabling the mass production of IBC SHJ solar cells with the already achieved efficiencies at competitive costs.

This chapter thus describes and evaluates industry-compatible manufacturing methods for IBC SHJ solar cells and the ensuing implications on the design of the rear side contact geometry.

Silicon-based High-Efficiency Technologies

Manufacturing processes for back contact solar cells are inherently more complex than the ones for two-side contacted solar cells. While there might also be slight advantages in terms of cell interconnection (with respect to module fabrication), this increase in complexity needs to be compensated by providing a gain in efficiency. Apart from IBC SHJ solar cells, efficiency values above 25 % have been achieved with multiple technologies [19, 26, 30, 162]. Among these Sunpower's homojunction approach with passivated contacts represents another IBC proponent [26]. However, its exact processing sequence is undisclosed. Other high-efficiency technologies are two-side contacted solar cells either with passivated (PERL, TOPCon [19, 170]) or heterojunction contacts. Especially the latter are a promising candidate for mass production, as these high efficiencies were already achieved on industry-scale cell areas (>150 cm^2). PERC solar cells, based on p-type multi- and monocrystalline wafers, are already adapted for mass production, but the limited efficiency of these solar cell technologies (slightly above

22 % [10, 171]) justifies the exploration of concepts exceeding 25 % efficiency: already modest increases in cell efficiency result in a significant decrease in the levelised cost of energy (LCOE) of the solar cell technology [172].

Table 6.1 lists the record efficiencies of the aforementioned, different solar cell technologies. Only solar cells with cell areas above 100 cm^2 are listed to emphasise the industrial viability of the respective technology.

Table 6.1: Silicon solar cell efficiency comparison (cell area greater 100 cm^2)

Cell Concept	Area* (cm^2)	Wafer doping	Efficiency (%)	Manufacturer
Multi-PERC	245.8 (ta)	p-type	22.0	Jinko Solar [10]
Mono-PERC	243.2 (ta)	p-type	22.6	Trina Solar [171]
IBC	153.5 (ta)	n-type	25.2	Sunpower [26]
Standard SHJ	151.9 (ap)	n-type	25.1	Kaneka [162]
IBC SHJ	179.7 (da)	n-type	26.6	Kaneka [30]

*(ta) total area, (ap) aperture area, (da) designated illumination area [10]

Comparing IBC and two-side contacted silicon heterojunction solar cells, the efficiency gap is much smaller (26.7 vs 25.1 %), and thus is the margin for a more cost-intensive IBC processing. Hence a case can be made that the main competitor for IBC SHJ solar cells, with respect to future high-efficiency concepts, is the standard SHJ solar cell [173].

IBC and two-side SHJ approaches share certain heterojunction-specific advantages: heterojunction processes do not require high-temperature (greater 200 °C) process steps and SHJ solar cells feature a better temperature coefficient, owing to their higher V_{OC} values. Heterojunction-specific cell processing challenges revolve mainly around contacting and metallisation. Screen-printed metallisation layers can only be cured at temperatures not exceeding 250 °C to avoid damaging the a-Si:H layers. As a consequence more expensive silver pastes have to be used instead of aluminium ones. Furthermore, two-side contacted SHJ solar cells require the use of a TCO, preferably on both sides of the cell. At the front side the TCO has to fulfil multiple contradictory requirements (high conductivity and transparency at a fixed thickness) that currently are best met by ITO, a comparably expensive material. However, a lot of research effort is put into finding potential alternatives (see also section 5.4). Using an IBC approach might alleviate the latter problem, as TCO layers are only present at the rear side of the solar cell, allowing a more flexible design with respect to the TCO's thickness and conductivity. Apart from that, there are no inherent process-related advantages for IBC SHJ solar cells, hence limiting the increase in processing complexity is paramount.

SHJ solar cells are usually built using n-type c-Si wafers. As the solar cell market in its current state is dominated by p-type technologies (PERC), an increase in the demand for n-type wafers will most likely lead to a shortage in supply, which increases cost, at least until wafer manufacturers have increased their capacities. Another issue related to the use of n-type wafers are thermal donors that are formed by the accumulation of oxygen impurities within the wafer. Especially standard n-type Czochralski wafers exhibit this phenomenon, as they contain a large amount of oxygen impurities. Thermal donors can act as effective recombination centres, affecting the wafer's bulk lifetime and thus decrease the solar cell's performance [174].

In contrast to PERC processes that are a further development of the conventional c-Si solar cell manufacturing process (diffused junction), setting up a SHJ process requires the acquisition of a variety of new tools (Wet-chemical treatment, suitable PECVD and PVD tools), which leads to considerable initial costs (capital expenditure, CAPEX). As already pointed out above, ITO-based TCO layers and the increased amount of silver consumption (in particular for IBC SHJ solar cells with almost fully metallised rear sides) represent substantial, SHJ-specific cost factors. In this regard, the introduction of alternative TCO materials and copper-based metallisation schemes would contribute significantly to the cost reduction of SHJ solar cell processes [175].

6.1 From Laboratory to Industrial Production

Laboratory solar cells are usually built to explore the limits of a certain technology, and thus process complexity or rather simplicity is not a primary concern. Cell areas are limited as the manufacturing equipment is specifically designed for flexible research purposes rather than providing a high throughput of large wafers.

As presented in section 4.3, it is also possible to develop and design a process that specifically focuses on industrial viability. Here industrial viability arises from avoiding high temperature deposition processes, limiting the use of (hazardous) wet chemicals and reducing the overall process time (reducing the number of annealing and curing steps, thus increase the wafer throughput). In the context of solar cell processing, photolithography based patterning methods have to be avoided. Moreover, the corresponding solar cells should feature large cell areas, ideally equal to the size of the industry-sized wafers (usually greater than $200\,\mathrm{cm}^2$).

In the following, published and industrially viable approaches for the manufacturing of IBC SHJ solar cells are reviewed with respect to their operating principle and potential.

6.1.1 In-situ Masking

As shown in section 4.3, in-situ masking represents a viable alternative to photolithography based thin film patterning. However tapering effects and requirements with respect to the physical stability of the mask material limit the achievable minimum feature size.

Two-Mask Approach

The shadow mask process introduced in section 4.3 meets most of the requirements for an industry-compatible process outlined above. The use of wet chemicals is limited to an initial RCA cleaning and a short TCO etch in the latter stages of the process. Furthermore, the overall process time is substantially reduced, compared to the photolithography approach. In section 4.3 cell areas were kept at small values ($1\,\mathrm{cm}^2$) for practical reasons, however there is no fundamental obstacle preventing the realisation of larger cells, apart from the stability of the corresponding silicon hard masks. In an eventual industrial process, using a different, potentially flexible mask material might be beneficial.

In terms of PECVD processing time, the need to align the second mask on the structure patterned with the initial mask based process might pose a serious challenge. If wafer throughput numbers for standard industry solar cell processes are regarded as a reference (greater than 2000 wafers per hour [176]), the time needed for this alignment step has to be minimal, which is particularly difficult to realise considering the fragility of the mask and the required accuracy.

Tunnel-junction IBC

Tomasi et al. have developed a shadow mask based process addressing the alignment time issue by avoiding it altogether [139]. The process is based on the substrate dependent growth process of nanocrystalline silicon. After the passivation of the rear side with an intrinsic a-Si:H layer, an n-type nanocrystalline silicon layer is PECVD-deposited and patterned in-situ using a shadow mask. Afterwards a p-type silicon layer is deposited full area by PECVD. On top of the intrinsic a-Si:H regions the p-layer grows mainly amorphous forming the (i,p)-emitter stack. In the n-type nanocrystalline silicon regions, the p-layer immediately grows nanocrystalline, thus forming an intraband tunnel-junction BSF contact capable of extracting electrons. Owing to the initial amorphous growth in the emitter regions, the conductivity between the two regions is low enough to prevent detrimental shunting effects. The metallisation stack, TCO and silver, is patterned by applying a resist layer by inkjet printing and subsequent wet-chemical etching. The resulting cell structure is depicted in Figure 6.1.

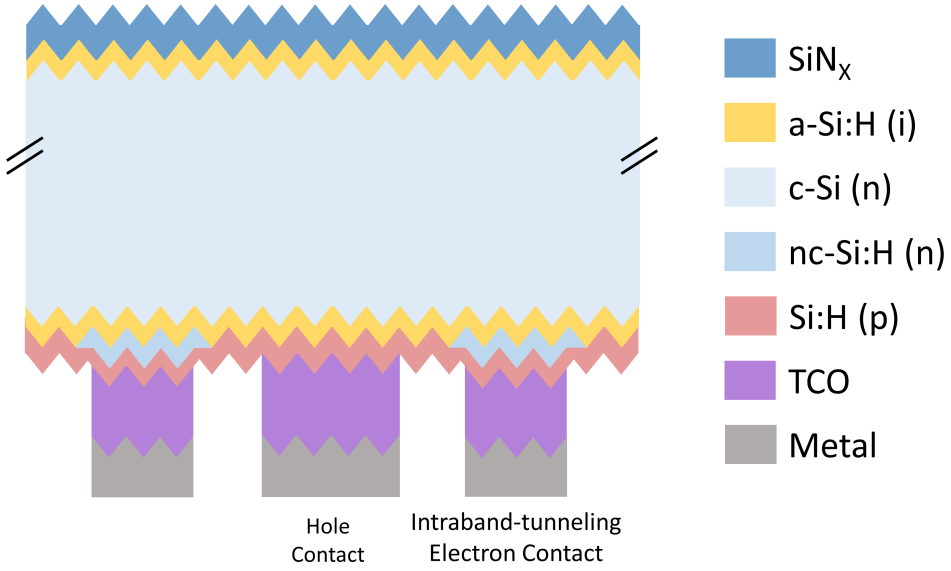


Figure 6.1: Tunnel-IBC SHJ solar cell: the n-contact is formed by an intraband tunnel-junction consisting of a stack of n- and p-type nc-Si:H. In the p-contact regions, the p-type Si:H initially grows amorphous, thus avoiding shunting the cell [139].

The tunnel-junction IBC process circumvents multiple problems that a two-mask process, such as the one presented in section 4.3, suffers from. First of all, the a-Si:H patterning process is self-aligned as only one mask is used. Consequently, tapering effects, as discussed in subsection 4.3.3, affect only the layer deposited through the mask, in this case the n-contact layer. Related issues such as large overlap regions do not need to be addressed, as overlapping p- and n-layers are inherent to the design of the BSF contact. Furthermore, the TCO can be optimised solely for the contact to one particular type of silicon, in this case the p-type nanocrystalline one. TLM measurements on TCO contacted tunnel-junction stacks yield contact resistivities as low as $10\,\mathrm{m\Omega cm^2}$, indicating that this interface does not limit the solar cell's performance.

The main challenge of this particular architecture is optimising the nanocrystalline silicon deposition processes. The n-type layer must be sufficiently doped to shield the c-Si regions from the electrical potential of the p-type layer on top, to preserve the charge carrier selectivity of the n-contact. Additionally it must exhibit a high crystallinity to ensure the immediate nanocrystalline growth of the subsequent p-type layer enabling a functioning tunnel-junction contact. On the contrary, the p-layer at first has to exhibit a certain amount of amorphous growth in the emitter regions resulting in a low lateral conductivity, to prevent a low-resistive current path between emitter and BSF regions that potentially leads to shunts. The nucleation layer growing in the emitter region prior to the initial crystallites serves as a sufficient insulator between the two contacts. However it is usually of poor electrical quality and with a thickness of up

to 10 nm might practically increase the effective thickness of the intrinsic a-Si:H layer, thus limiting the FF.

In [139], initial solar cells with a cell area of 9 cm^2 yield efficiencies of up to 22.6 %, featuring high V_{OC} values of 728 mV, but only moderate j_{SC} and FF values (40.7 mA/cm^2 and 76.4 %). By improving the nanocrystalline layers, efficiency values up to 23.9 % were achieved, featuring high V_{OC} and j_{SC} values (735 mV and 41.6 mA/cm^2) and a decent FF (78.2 %) [140]. Having a pseudo-FF of above 85 % the solar cell is clearly limited by the series resistance, which amounts to 1.5 Ωcm^2. With a contact resistivity of roughly 400 $m\Omega cm^2$, the p-contact accounts for 61 % of the total series resistance. The second largest contributor is the substrate (28 %), most likely related to a large pitch and an imperfect emitter to BSF ratio (51 %). The series resistance contributions of the n-contact (4 %) and the metallisation grid (7 %) are comparably small.

The tunnel-junction based IBC SHJ process is a remarkably simple manufacturing method fulfilling most of the requirements for an industrially viable process. A further reduction in the usage of wet-chemicals can be achieved by replacing the inkjet-based metallisation procedure with a screen-printing method. Initial solar cell results are promising, despite being limited by the emitter contact resistivity. The high value of the latter might be inherent to the selective growth process of the p-type nanocrystalline layers as the thick nucleation layer in the emitter regions likely represents a significant transport barrier for the minority charge carriers.

6.1.2 Laser Ablation

The general principle of laser-based patterning processes and the physics of laser-silicon interaction have already been discussed in section 3.1.2 and 4.3.1. Laser ablation based patterning techniques excel in terms of flexibility and process speed. There is also almost no limit with respect to the wafer size. Compared to in-situ masking and photolithography approaches, the accuracy of laser ablation based processes is closer to the latter, which is beneficial in terms of achievable minimum feature size and design options regarding the contact geometry: Ring *et al.* present laser-processed solar cells with a BSF width of 58 μm and a pitch of 600 μm, thus featuring smaller structures than the photolithography-based cells presented in this work [84] (see also Figure 6.2). Laser ablation is also a contactless and very localised process, affecting only the intended device regions. Owing to the large amount of available laser systems (different wavelengths) and settings (power, pulse frequency, scanning speed etc.) the process can be adapted to many applications and materials.

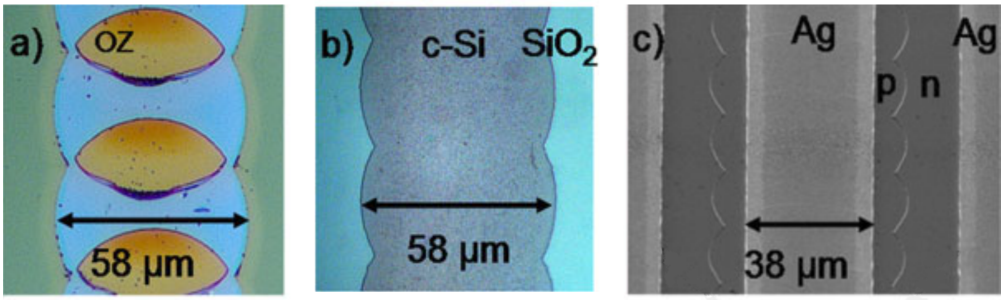


Figure 6.2: a) Optical microscopy image of a) overlap zones in a laser-scribed line (step I in Figure 6.3), b) after emitter etch (step II) and c) after lift-off and metallisation patterning [84].

Despite this extraordinary flexibility of laser systems, direct ablation of amorphous from crystalline silicon mostly results in surfaces that are very difficult, if not impossible to properly repassivate with intrinsic a-Si:H layers. Therefore laser based patterning processes are usually used to pattern specific masking layers on top of sacrificial layers that absorb most of the excess laser power. Thus the damage to the a-Si:H/c-Si interface due to laser absorption is substantially reduced. The patterning of the functional layers (e.g. a-Si:H emitter and BSF layers) is realised using conventional techniques such as wet-chemical etching.

A typical laser ablation based patterning process is depicted in Figure 6.3. On top of the BSF respectively emitter stack a thick SiO_2 sacrificial layer capped with another amorphous silicon layer is placed. Only the latter is directly patterned by laser ablation. Since the laser usually operates in pulsed mode, laser spots will overlap during the scribing of line-shaped openings. In these overlap zones (OZ) the doubled amount of the original laser power is applied to the overall layer stack (see Figure 6.2). Hence the optimisation of the laser power is particularly difficult: it has to be sufficiently high to properly ablate the masking layer and low enough to avoid damage to the a-Si:H passivation in the overlap zones. Often multiple sacrificial layers are necessary to account for the latter.

In one specific variant of the laser ablation based approach, developed at HZB, Ring *et al.* expanded their 250 nm thick SiO_2 sacrificial layer by adding another 20 to 40 nm thick a-Si layer covered by another 40 nm SiO_2 and the corresponding a-Si mask layer [84]. The ablation of the mask layer is followed by a wet-chemical etch of the emitter layer and a subsequent deposition of the BSF. The latter is then patterned using a self-aligned lift-off process by etching the sacrificial SiO_2 layer. In comparison to the single SiO_2 sacrificial layer, the double-layer prevented the degradation of the a-Si:H passivation more efficiently, especially on n-type substrates, indicated by implied-V_{OC} values of up to 716 mV. However, final cells exhibited rather low V_{OC} values of 689 mV

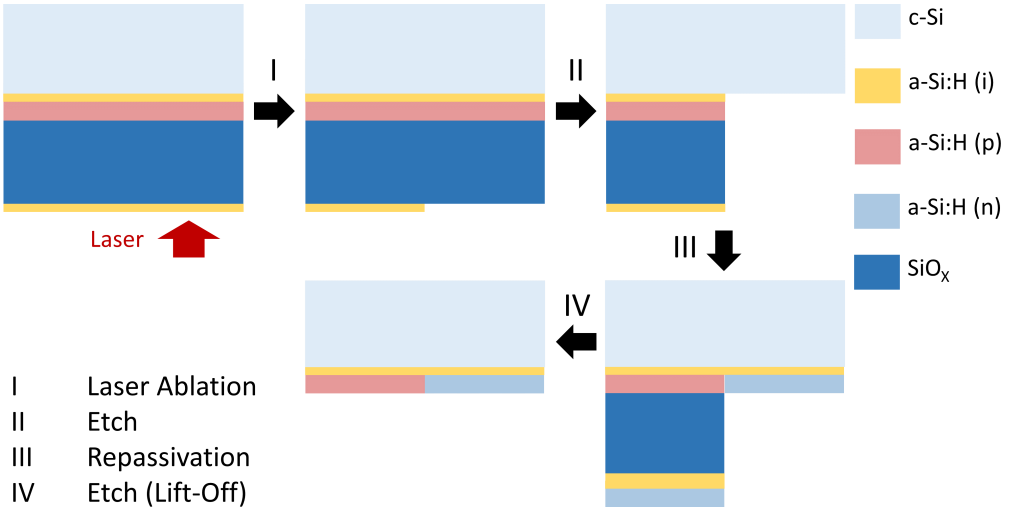


Figure 6.3: Typical laser ablation based patterning process: initially an a-Si protection layer is patterned by laser ablation (I), followed by a wet-chemical etch of the underlying sacrificial and emitter layer (II); the etched region is then repassivated with the BSF layer stack (III), followed by etching the sacrificial layer in a lift-off process (IV).

for p-type wafers and 648 mV for n-type wafers. The discrepancy between the implied and the final V_{OC} values are attributed to a non-ideal cell design and unoptimised sputter processes.

Harrison *et al.* developed a process where both the emitter and the BSF are patterned by two separate laser-ablation steps [83]. Here the sacrificial and the mask layer, the former consisting of SiO_2, the latter of intrinsic a-Si and p-type a-Si, are placed onto an (i,n)-passivated n-type c-Si wafer. The mask layer stack is then patterned by laser ablation, primarily removing the p-type a-Si in the designated emitter region leaving behind residues of intrinsic a-Si below. In a subsequent step these intrinsic a-Si residues are etched using an alkaline solution (intrinsic a-Si:H and BSF) and hydrofluoric acid (SiO_2), not affecting the p-type a-Si in the non-ablated regions. After the deposition of the emitter stack, the process is repeated for the BSF region. Respective solar cells yield efficiencies of 20.6 % for a cell area of 18 cm^2 and 18.9 % for a cell area of 101 cm^2. The cell performance is mainly limited by low FF values (72.1 % at maximum), which are explained by still existing laser damage, and a lack of process uniformity for large cell areas.

To prevent laser damage to the a-Si:H passivation Xu *et al.* used a sequence of SiO_X and SiN_X layers forming a distributed Bragg reflector (DBR), instead of a single SiO_X sacrificial layer [177]. The wavelength of the DBR is set according to the wavelength of the laser system. The overall process flow is similar to the one presented by Ring *et al.*, also incorporating a lift-off process for a self-aligned BSF patterning. Owing to the increased reflection of the DBR, the laser-induced damage to the a-Si:H/c-Si

interface is mostly prevented, apart from overlap zones. To reduce the area of these overlap zones, the laser processing speed is increased. Solar cells manufactured with this process achieve efficiencies up to 21.8 % featuring V_{OC} values of 724 mV, which indicates negligible laser damage to the passivation. A moderate FF of 72.6 %, caused by a high series resistance, limits the efficiency.

To sum up, laser ablation based processes have proven to be a viable option for IBC SHJ solar cell manufacturing. However to prevent the laser process from damaging the a-Si:H passivation, the application of multiple additional layers is necessary, which increases the process complexity substantially. Moreover, current processes mainly rely on wet-chemical etching for patterning. All-dry lithography free processes using reactive ion etching, inter alia, are investigated, but related solar cell results, especially on larger wafer sizes, have yet to be published [178].

6.2 Implications on the Contact Geometry

The photolithography technique allows to pattern thin films with an unrivalled accuracy, with minimum feature sizes in the micrometre range and below. Switching to industrially viable patterning methods, be it laser or mask based, thus means to rework photolithography based contact designs of IBC SHJ solar cells with respect to additional process-related constraints.

To estimate the losses caused by increasing the pitch, emitter, BSF, potential overlap width, and metallisation gaps, several simulation studies were performed.

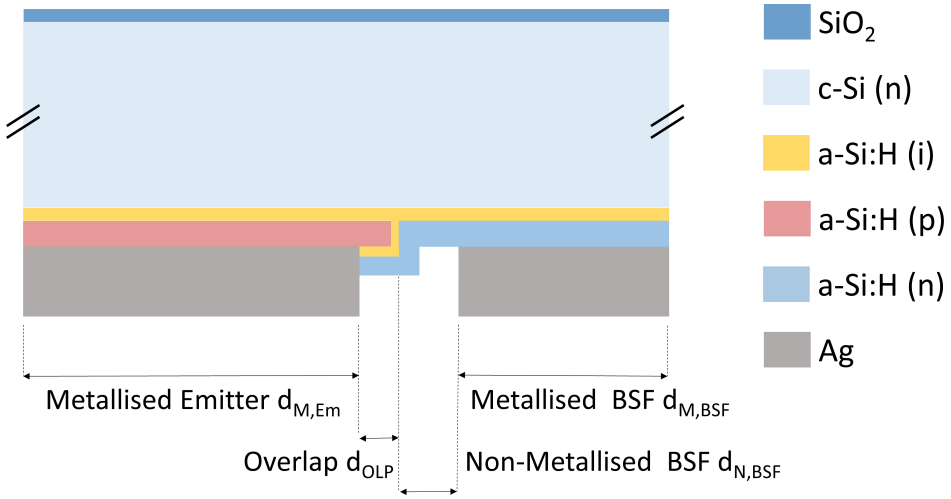


Figure 6.4: Simulated unit cell, with the characteristic geometry parameters indicated: metallised emitter and BSF, as well as the overlap and non-metallised BSF region.

Simulated Model The unit cell depicted in Figure 6.4 represents the starting point for the simulation studies. It is modelled after the geometry of the best performing solar cells from chapter 5. The geometry and cell parameters are listed in Table 6.2. The given width values for the real world solar cell refer to the design of the photolithography mask, thus not incorporating underetching effects that usually account for deviations of not more than 5 μm. The width values of the simulated solar cells refer to the dimensions of the particular unit cells, which are modelled after the real world dimensions of the respective solar cells. In case of the photolithography-based design, an accurate representation based on the dimensions of the photolithography masks is possible. In case of solar cells built with the shadow mask process, the listed widths values are approximated based on microscopy images and Raman measurements, as the strong tapering effects observed for a-Si:H layers patterned by in-situ shadow masking (see subsection 4.3.3) make a more accurate description impossible. Doping density and thicknesses of the a-Si:H layers were set to yield realistic values for the p- and n-contact resistivities (330 mΩcm^2 for the p-contact and 20 mΩcm^2 for the n-contact), the remaining parameters are listed in section 3.3 and Appendix B.

Table 6.2: Comparison of real world and simulated solar cells

Cell	$d_{M,Em}$ μm	$d_{M,BSF}$ μm	d_{OLP} μm	$d_{N,BSF}$ μm	j_{SC} mA/cm^2	V_{OC} mV	FF %	η %
Real Cell*	756	384	15	15	41.3	713	78.5	23.20
Sent.PL**	756	384	15	15	39.3	737	78.5	22.74
Sent.Mask***	1040	360	100	50	39.4	736	77.7	22.51

*Real Cell: best performing photolithography-based solar cell
**Sent.PL: simulated equivalent of *Real Cell*
***Sent.Mask: simulated shadow-mask-based solar cell

In Table 6.2 the parameters $d_{M,Em}$ and $d_{M,BSF}$ refer to the widths of the metallised emitter and BSF regions, respectively; d_{OLP} represents the width of the overlap region, and $d_{N,BSF}$ the width of the non-metallised BSF region that is not part of the overlap region (the sum of d_{OLP} and $d_{N,BSF}$ gives the metallisation gap of the solar cell).

Comparing the real world and the simulated solar cell, there are substantial differences with respect to the j_{SC} and the V_{OC}. The difference in the former can be explained by the simple Lambert-Beer-based absorption model that was used in the simulation: it does not account for photons reflected at the rear side of the solar cell, hence the simulated current is lower than the one of the real device. Since the simulation study focuses on the impact of the contact geometry on the electrical rather than the optical properties of the solar cell, the modelling of the latter was not prioritised. The

higher V_{OC} of the simulated solar cell is likely related to the absence of edge-related losses present in the accurately shaded real-world solar cell. In fact, values around 737 mV were also achieved on actual solar cells without proper shading of the cell area. Owing to the realistic contact resistivities the parameter that is influenced the most by variations of the contact geometry, the FF, is identical for both the simulated and the real solar cell.

If a mask based process is used, overlap and metallisation gap widths in the range of 15 to 30 μm are difficult to realise. For the solar cells manufactured with the shadow mask process presented in section 4.3, the overlap width is assumed to be in the range of 100 μm, with a total metallisation gap of up to 150 μm. Owing to the strong tapering effects (see subsection 4.3.3), an accurate overlap width is difficult to determine. Furthermore, the pitch of the mask based cells was increased from 1.2 to 1.7 mm.

If the overlap and the overall metallisation gap width is kept constant and only the pitch is increased, the simulated efficiency remains rather constant; a minor decrease in FF can be observed. With realistic overlap/metallisation gap widths (comparing *Sent.PL* and *Sent.Mask* in Table 6.2) the drop in FF (0.8 %abs) is more substantial.

6.2.1 Fill Factor Limitations

In order to investigate the contact geometry related limitations of the fill factor, an extended simulation study was performed, using the parameters outlined above and in section 3.3 and Appendix B, respectively. As described in chapter 5, the fill factor is strongly influenced by the series resistance. Major contributors to the series resistance are the contact resistivities arising from the a-Si:H/TCO interfaces, the bulk resistivity of the wafer, and the mean path photogenerated minority carriers have to travel through the wafer to reach the p-contact.

An analytic method to determine the optimum emitter ratio based on only the p- and the n-contact resistivity was already presented in subsection 5.2.2. However, in this case the influence of the wafer resistivity and the pitch were not taken into account. Figure 6.5 shows the dependency of the FF on the metallised emitter ratio (metallised emitter width divided by the pitch) for five fixed metallised BSF widths (*simulated curves*) next to the curve based only on the contact resistivity (*calculated curve*, see subsection 5.2.2). The contact resistivities are identical for all curves (330 mΩcm^2 for the p-contact and 20 mΩcm^2 for the n-contact). The total metallisation gap was set to 10 μm (5 μm overlap, 5 μm non-metallised BSF region). The difference between the simulated curves and the calculated one can be attributed to the bulk related contribution to the series resistance. This is consistent with the trend observed for the different metallised BSF widths: simulated curves of cells with large pitches (greater BSF width)

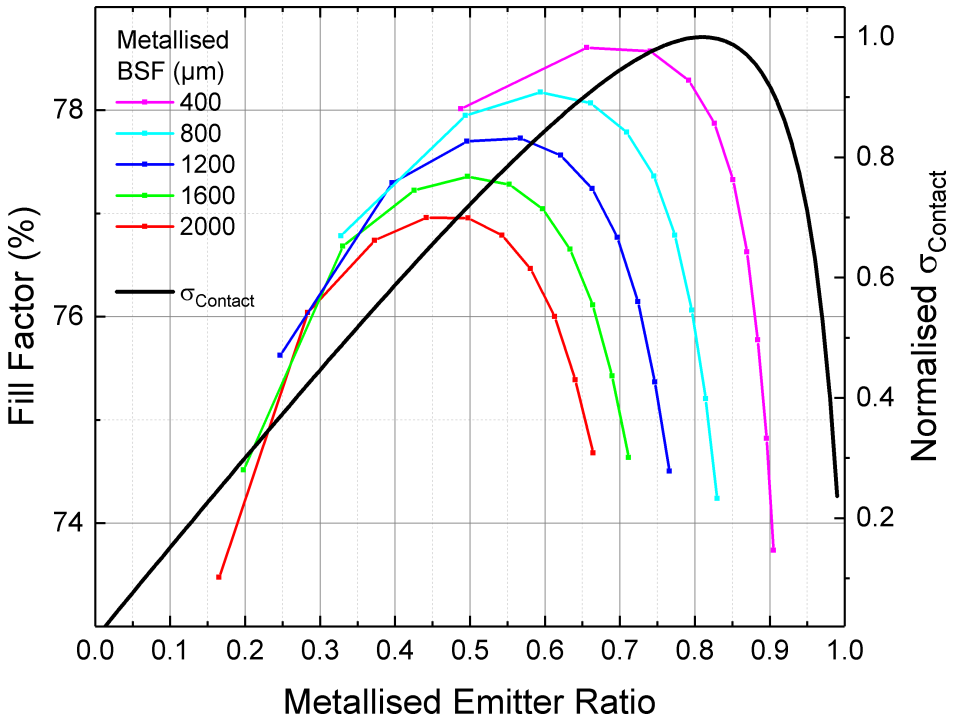


Figure 6.5: Dependency of the simulated fill factor on the metallised emitter ratio for five different metallised BSF width (coloured curves); the black curve represents the inverse, emitter ratio dependant series resistance contribution arising from the p- and the n-contact resistivity.

deviate more from the calculated curve and vice versa. A simulated curve with an infinitesimally small BSF width or pitch, respectively, resulting in practically no lateral transport of either charge carrier type in the wafer and thus only a constant bulk related series resistance contribution, is expected to converge towards the calculated curve.

To analyse the bulk contribution to the series resistance in more detail, the analytic model outlined in subsection 5.2.2 is extended by introducing a bulk-related series resistance parameter, depending on the bulk resistivity and the contact geometry:

$$R_{\mathrm{S,Total}} \approx \frac{\rho_p}{A_p} + \frac{\rho_n}{A_n} + R_{\mathrm{Bulk}} \tag{6.1}$$

Again ρ_p and ρ_n represent the contact resistivity of the p- and the n-contact, respectively, and A_p and A_n their corresponding area fractions. R_{Bulk} is approximated using the expression proposed in [152]:

$$R_{\mathrm{Bulk}} = \frac{(d_{\mathrm{M,Em}} + d_{\mathrm{Gap}})(d_{\mathrm{M,Em}} + d_{\mathrm{Gap}} + d_{\mathrm{M,BSF}})}{3t_{\mathrm{W}}} \frac{\rho_B N_D}{(N_D + \Delta p)} \tag{6.2}$$

The expression includes the already introduced geometry parameters representing the metallised emitter and BSF width; d_{Gap} is given by the sum of d_{OLP} and $d_{\mathrm{N,BSF}}$, t_{W} is the thickness of the wafer; ρ_B represents the wafer's bulk resistivity, N_D the dopant concentration and Δp the average excess minority carrier concentration at MPP conditions (the respective values are listed in Appendix B).

Assuming that the FF is dominated by resistive losses, the minima of the approximated $R_{\mathrm{S,Total}}$ should correspond to the simulated FF maxima shown in Figure 6.5, for a given contact geometry (BSF width and emitter ratio). Figure 6.6 shows that the simple analytic series resistance model is able to reproduce the trend given by the simulated results. The analytic model overestimates the influence of the bulk resistivity slightly, as it delivers lower optimum metallised emitter ratios than the simulation, especially for small and large BSF widths.

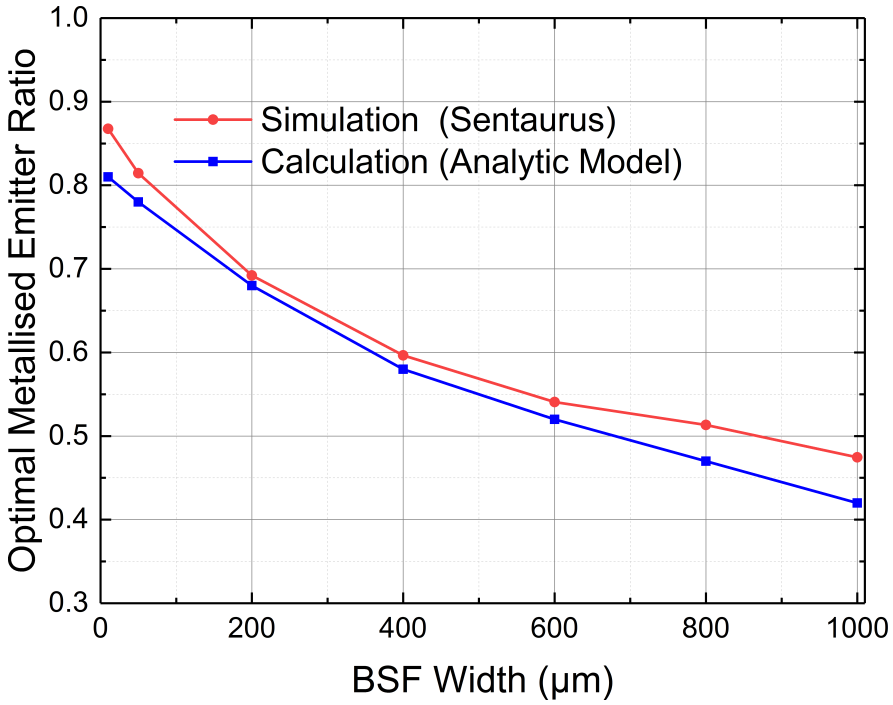


Figure 6.6: Optimum emitter ratios for different metallised BSF widths, with respect to either maximum FF values (Sentaurus simulation) or minimum series resistance values (analytic model).

With the analytic model delivering results being very similar to simulated ones, it can be used to approximate the total series resistance for different contact geometries and analyse the influence of the other parameters, such as the contact resistivities, without running a full-fledged numerical 2D simulation. Remodelling the best photolithography-based cell from chapter 5 (*Real Cell* in Table 6.2), the analytically modelled $R_{\mathrm{S,Total}}$ amounts to $0.63\,\Omega\mathrm{cm}^2$, which corresponds very well to the series resistance values extracted by the dark jV and the Suns-V_{OC} method ($0.6\,\Omega\mathrm{cm}^2$ averaged, compare

Table 5.10). With 0.72 Ωcm^2 the value for the cell with a contact geometry modelled according to the mask based cells presented in section 5.5 (*Sent.Mask* in Table 6.2) is only slightly higher than the photolithography equivalent, being in line with the modest FF decrease seen in the simulation (0.8 %abs).

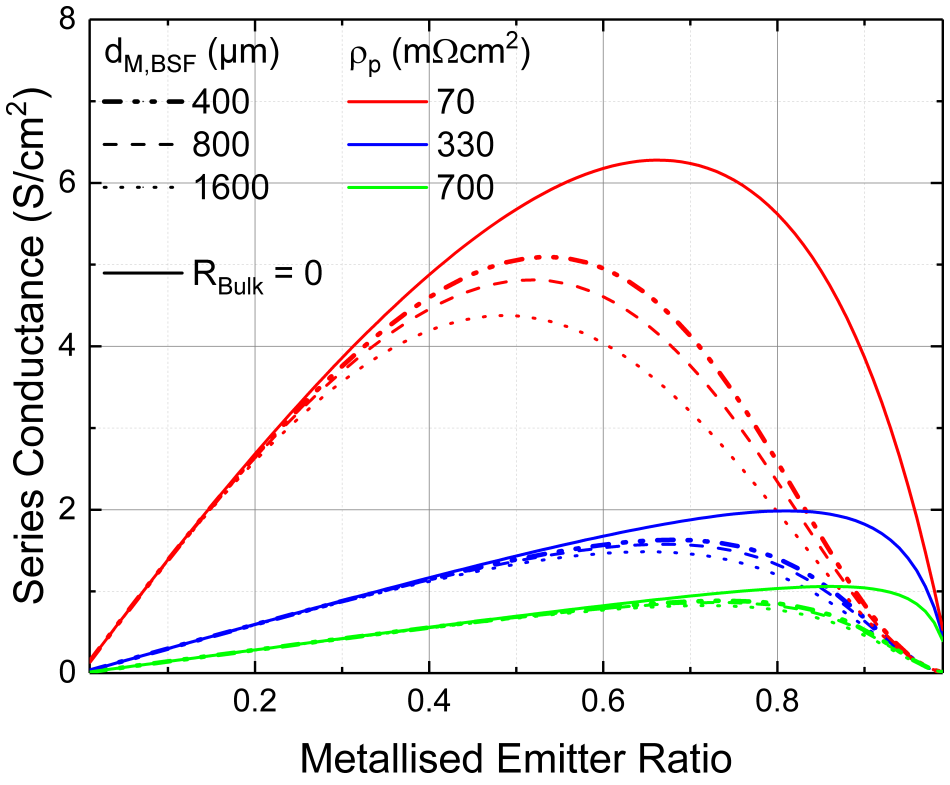


Figure 6.7: The inverse series resistance (series conductance) vs. the metallised emitter ratio, calculated with the analytic model outlined above, for multiple metallised BSF widths ($d_{M,BSF}$) and p-contact resistivities (ρ_p); additionally the series conductance curve depending only on the contact resistivities is shown ($R_{Bulk} = 0$), corresponding to $\sigma_{Contact}$ in Figure 6.5.

Based on the analytic model, Figure 6.7 visualises the strong impact of the p-contact resistivity on the overall series resistance. The inverse series resistance (series conductance, for better comparability to Figure 6.5 and 6.8) is plotted for different p-contact resistivities (70, 330, and 700 mΩcm^2) and BSF widths (400, 800, and 1600 μm as well as $d_{M,BSF} = 0\,\mu$m, equivalent to $R_{Bulk} = 0$). The n-contact resistivity was kept at a constant value of $\rho_n = 20$ mΩcm^2. With respect to the chosen parameters, the p-contact resistivity has clearly the most impact on the overall series resistance. Naturally the impact of the contact geometry (BSF width and emitter ratio) becomes more relevant, as the total contact resistivity decreases. Both the variation of the contact resistivity and the geometry influence the optimum emitter ratio, hence to exploit the potential of improvements in one parameter (e.g. contact resistivity), the other (contact

geometry) should be adjusted as well. This is also reflected in simulated results, shown in Table 6.3. A cell with a BSF width of 400 μm achieves a FF of 78.3 %. Decreasing the p-contact resistivity from 330 to 70 mΩcm^2 increases the FF by 1.2 %abs. If then additionally the metallised emitter ratio is decreased (reducing the pitch from 2020 to 880 μm), the FF increases to 80.1 %, gaining another 0.6 %abs. With the pitch kept constant at a value of 2020 μm (in this case the BSF width is increased to 904 μm), the FF still improves by 0.4 %abs, showing the importance of the emitter ratio.

Table 6.3: FF trends

Parameter Change	m-emr* %	$d_{M,BSF}$ μm	pitch μm	ρ_p mΩcm^2	ρ_n mΩcm^2	FF %
initial	79.2	400	2020	330	20	78.3
$\rho_p \downarrow$	79.2	400	2020	70	20	79.5
$\rho_p \downarrow$, m-emr $\downarrow$, pitch $\downarrow$	54.3	400	880	70	20	80.1
$\rho_p \downarrow$, m-emr $\downarrow$, $d_{M,BSF} \uparrow$	54.3	904	2020	70	20	79.9

*m-emr is an abbreviation for the metallised emitter ratio.

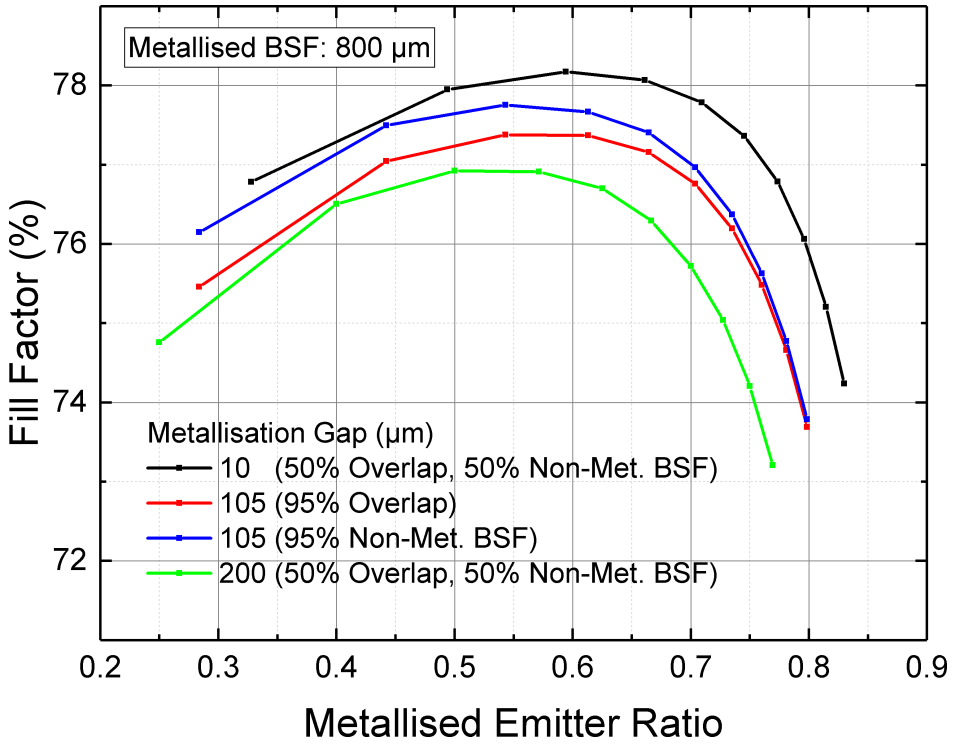


Figure 6.8: Dependency of the simulated fill factor on the metallised emitter ratio for different metallisation gap configurations.

Figure 6.8 visualises the impact of the metallisation gap on the FF for different metallised emitter ratios at a fixed metallised BSF width of 800 μm (corresponding to an

industrial mask process). Ideally the metallisation gap is as small as possible, however constraints with respect to the manufacturing process make larger gaps inevitable. The gap should mainly consist of non-metallised BSF rather than an overlap region, as the latter deteriorates the performance further. The overlap region represents a parasitic p-i-n diode on top of the silicon wafer. Since the overlap area is not metallised, the corresponding diode is in open-circuit conditions (assuming poor lateral conductivity of the a-Si:H layers) and thus in blocking mode. Nevertheless it represents an additional recombination path for minority charge carriers generated in its vicinity.

The detrimental influence of the overlap region is particularly significant at lower metallised emitter ratios, as in these cases the share of overlap area per total cell area is greater. Consequently for larger metallised emitter ratios, the difference between a gap formed by an overlap or a non-metallised BSF region decreases.

Comparing the graphs in Figure 6.5, it is apparent that the optimal emitter ratio substantially differs between mask (larger pitch and metallised BSF widths) and photolithography (smaller pitch and metallised BSF widths) based IBC SHJ solar cells. The smaller pitch values of the latter allow emitter ratios of up to 80 % before bulk related losses become significant. In these cases the maximum FF is mainly limited by the p- and the n-contact resistivity, as already illustrated by the results of the photolithography-based solar cells presented in chapter 5. Larger pitch values and metallisation gaps are inherent disadvantages of mask based manufacturing processes and losses in the bulk lead to optimum emitter ratios around 50 to 60 %, despite the p-contact resistivity being much larger than its n-counterpart.

The dominant effect of a decreased p-contact resistivity is shown in Figure 6.7 and Table 6.3. The results obtained from simulation and analytic modelling suggest that the performance of mask-based solar cells is not limited, but only slightly reduced by the necessity for a larger contact geometry. Given realistic (700 and 330 $\mathrm{m\Omega cm^2}$) and optimistic (70 $\mathrm{m\Omega cm^2}$) values, the influence of the contact resistivity still overshadows the one of the contact geometry.

6.3 Conclusions

The IBC SHJ solar cells featuring the highest efficiencies are built with photolithography-based processes. Accurate patterning schemes, yielding minimal overlap and overall metallisation gap values as well as small pitch values reducing bulk-related losses, are beneficial for achieving high efficiencies. However, as shown in the simulation study, the fill factor decrease following the contact geometry adjustments inevitable for an

industrially viable process only amounts to 0.2 to 0.8 %abs, depending on the presumed contact resistivities.

With laser- and mask-based processes industrially viable alternatives to the established photolithography approach are available. The complexity of the mask-based processes suggested in section 4.3 and by Tomasi *et al.* (see section 6.1.1) is only marginally higher than the one for a standard two-side contacted SHJ solar cell process. At the same time these processes meet the requirements with respect to large cell areas and minimal use of wet chemicals. Initial solar cell results (almost 24 % efficiency for the tunnel-junction approach) are promising, albeit still limited by low fill factor values.

Chapter 7

Conclusions and Outlook

This work follows two routes: the first one explores the efficiency potential of IBC SHJ solar cells built with a rather complex process, the second one shows ways to make this efficiency potential actually industrially accessible by developing an appropriate, simplified manufacturing process.

In chapter 4, both manufacturing processes are discussed. In the first part, the established photolithography process is extensively described, emphasising its complexity, and subtle but crucial optimisations to the process are introduced: improved photoresist adhesion by introducing a mandatory HF-dip before the photoresist deposition, evaporation-based metallisation increasing the reliability of the ITO etch process and, most importantly, the non-destructive protective layer etching by using alkaline etchants.

The second part of chapter 4 describes the development of an industrially viable manufacturing process based on structured silicon wafers serving as shadow masks to pattern a-Si:H and nc-Si:H in-situ during the PECVD deposition process. 150 μm thick silicon wafers serve as a suitable mask material, nevertheless the minimum feature size is limited to around 500 μm, as otherwise the mechanical stability of the mask cannot be guaranteed. Comparing the two developed alignment systems, the pin-to-hole method, which is based on laser-drilled holes in the respective wafers and matching metal pins on a custom-made aluminium carrier, is superior as it is easy to apply and inherently compensates for the thermal expansion of the different components (cell and mask wafer as well as the aluminium carrier). The fidelity of the patterned layers depends strongly on the PECVD deposition process. Processes exhibiting high gas flows are beneficial, as the silicon deposition is limited by the diffusion of SiH_3 radicals towards the substrate's surface thus preventing extended surface diffusion of the radicals that results in undesired deposition under the mask. However, both the limited accuracy of the alignment process and the imperfect fidelity of the patterned layers necessitate

adjustments to the cell design with respect to the contact finger widths and metallisation gaps.

The results of the various IBC-SHJ solar cells built during this work are presented and analysed in chapter 5. Photolithography-based cells with a direct, annealed aluminium metallisation achieve considerably better results than equivalent cells with an ITO/Ag metallisation (efficiency of 20.7 vs. 19.2 %). With an improved front side passivation the aluminium-based cells reach efficiencies up 22 %. The properties of the Al/a-Si:H contact system strongly depend on the annealing time and temperature. Moderate annealing likely leads to the formation of an intermediate aluminium silicide and initialises the crystallisation of the doped a-Si:H layers, which results in the reduction of the contact resistivity and thus in an increase of the FF. Extended annealing leads to strong interdiffusion between the aluminium and amorphous silicon layers eventually resulting in the disintegration of the latter and thus the deterioration of the passivation quality. In these cases, the consequential V_{OC} losses cannot be compensated by the increase of the FF.

The second part of chapter 5 focuses on the development of photolithography-based solar cells with TCO contacts. By introducing an intrinsic a-Si:H passivation layer to the front side layer stack, a nanocrystalline BSF layer and optimised a-Si:H emitter layers to the rear side, the efficiency of ITO-based IBC SHJ solar cells was increased by 4 %abs, from 19.2 to 23.2 %. Calculations of the implied FF and Suns-V_{OC} measurements indicate that the solar cells are mainly limited by high series resistances leading to FF values well below 80 %. Based on TLM measurements, the contact resistivities, in particular the one of the p-contact stack, were identified to be the main series resistance contributor. Thinning the intrinsic a-Si:H passivation layers and switching to a textured rear side led to substantial improvements of both the contact resistivities and the FF. Additionally, AZO was investigated as an alternative TCO material replacing ITO. The latter was found to form a better contact to the p-type a-Si:H layers, likely related to its higher work function, while the former yielded a better optical response resulting in a higher j_{SC}. Moreover, initial results of IBC SHJ solar cells with a $\mathrm{WO_X}$ interlayer between the p-type a-Si:H emitter and the TCO (ITO in this case) show slightly lowered p-contact resistivities, indicating the potential of high work function metal oxides as emitter contact materials.

In the last part of the chapter the very first results of IBC SHJ solar cells manufactured with the shadow mask process are presented. Cells with a screen-printed metallisation on an AZO layer reach decent V_{OC} and j_{SC} values (41 $\mathrm{mA/cm^2}$, 700 mV). However, the efficiency does not exceed 10 %, as the corresponding jV curves are strongly S-shaped limiting the jV-derived FF to values around 30 %. The latter is most

likely related to a malfunctioning emitter/TCO contact or a too thick intrinsic a-Si:H passivation layer. A second batch of solar cells built with a further developed shadow mask process – pin-to-hole alignment system, a-Si:H processes identical to the ones used for the best photolithography-based solar cells and a more accurately patterned ITO/Ag metallisation – yielded solar cells with efficiencies up to 17, and FF values up to 66 %. V_{OC} values are particularly low (616 mV), as the emitter passivation degrades during the metallisation.

Chapter 6 discusses the prospects of IBC SHJ solar cells with respect to industrial fabrication and marketability. With respect to high-efficiency concepts aiming for cell efficiencies above 25 %, top- and rear-contacted SHJ solar cells are identified to likely be the main competitor for IBC SHJ solar cells. The latter can only succeed if simple manufacturing processes are employed. Based on the state of IBC SHJ research, shadow-mask based processes show the most potential, as the complexity of the manufacturing process does not substantially differ from standard SHJ processes and cell efficiencies close to 24 % have been demonstrated. The implications of a shadow mask process on the contact geometry of IBC SHJ solar cells (larger contact finger widths and metallisation gaps) are also analysed with a simulation study. The results indicate only minor efficiency losses due to process related contact geometry adjustments.

Outlook

With 26.7 %, Kaneka's IBC SHJ solar cell is the most efficient silicon-based single-junction solar cell, significantly outperforming the solar cells presented in this work, which feature a maximum efficiency of 23.2 %. To close the gap, primarily the V_{OC} and the FF need to be improved. The V_{OC} is mainly limited by the small cell area and the wafer thickness, hence improvements in that regard can be realised by a redesign of the cell layout incorporating larger cells, and by choosing thinner wafers. Conversely, improvements in the FF require both a substantial increase of the passivation level, to achieve implied FF values of 85 % and more, and a drastic reduction of the contact resistivities, to reduce the series resistance. With respect to the latter, selective contacts based on high work function metal oxides might play a crucial role in improving the emitter/TCO interface.

While the race for efficiency is vital in order to fully understand the potential and the limitations of the IBC SHJ technology, the more important challenge refers to the transfer of this knowledge to industrially viable processes. Laser-ablation and shadow mask based patterning processes are two alternatives to the established photolithography-based approach. In particular the combination of patterning by shadow masks and

tunnel-junctions shows great potential, as it is a self-aligned process requiring only one masking step [139]. A further development of the two-mask approach, presented in this work, might involve not only the deposition, but also plasma-etching through masks and thus potentially alleviate problems arising from tapering effects and alignment inaccuracies.

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Appendices

Appendix A

Abbreviations and Symbols

a-Si:H	hydrogenated amorphous silicon
AZO	aluminium doped zinc oxide
B_2H_6	diborane
BC SHJ	back-contact silicon heterojunction
BSF	back-surface field
CFSYS	constant final-state yield spectroscopy
c-Si	crystalline silicon
χ_{a-Si}	electron affinity of amorphous silicon
χ_{c-Si}	electron affinity of crystalline silicon
d_{Gap}	width of the metallisation gap
$d_{M,BSF}$	width of the metallised back surface field region
$d_{N,BSF}$	width of the non-metallised back surface field region
$d_{M,Em}$	width of the metallised emitter region
d_{OLP}	width of the overlap region
ΔE_C	conduction band offset
ΔE_V	valence band offset
Δn	excess charge carrier density
DBR	distributed Bragg reflector
E_A	electron affinity
E_F	Fermi level
E_G	band gap
E_V	valence band edge
E_{Vac}	vacuum energy
η	solar cell efficiency
EQE	external quantum efficiency
HCl	hydrochloric acid
HMDS	hexamethyldisilazane
H_2O_2	hydrogen peroxide
IBC	interdigitated back contact
IBC SHJ	interdigitated back contact silicon heterojunction
iFF	implied fill factor
IQE	internal quantum efficiency
ISFH	Institute for Solar Research Hameln

ITO	indium tin-oxide
iV_{OC}	implied open circuit voltage
j_0	reverse bias saturation current
j_{mpp}	current density at the maximum power point
j_{Ph}	photocurrent
j_{SC}	solar cell short circuit current
jV	current density–voltage
k	Boltzmann constant
L_{T}	transfer length
λ	wavelength
$\mu_{n,p}$	mobility of holes (p), or electrons (n)
m	ideality factor
MPP	maximum power point
n	electron density
N_{A}	acceptor density
N_{D}	donor density
n_0	equilibrium electron density
n_i	intrinsic electron density
NaOH	sodium hydroxide
nc-Si	nanocrystalline silicon
NH_4OH	ammonium hydroxide
NIR	near-infrared wavelength range
OZ	overlap zone
p	hole density
p_0	equilibrium hole density
ϕ	work function
PCD	photoconductance decay (measurements)
PECVD	plasma-enhanced chemical vapour deposition
PERC	passivated emitter rear contact
PES	photoelectron spectroscopy
pFF	pseudo fill factor
PH_3	phosphine
PL	Photoluminescence
PV	Photovoltaic
PVD	physical vapour deposition
q	elementary charge
QE	quantum efficiency
$R_{\square}$	sheet resistance
R_{C}	contact resistance
R_{P}	parallel resistance
R_{S}	series resistance
$R_{\mathrm{Ser,Total}}$	total series resistance
$R_{\mathrm{Ser,N}}$	series resistance contribution of the n-contact
$R_{\mathrm{Ser,P}}$	series resistance contribution of the p-contact
RCA	Radio Corporation America
ρ_{C}	contact resistivity

ρ_{n}	n-contact resistivity
$\rho_{\mathrm{N,TLM}}$	measured n-contact resistivity
ρ_{p}	p-contact resistivity
$\rho_{\mathrm{P,calc}}$	calculated p-contact resistivity
$\rho_{\mathrm{P,TLM}}$	measured p-contact resistivity
$\sigma_{\mathrm{Contact}}$	contact conductivity
S_{front}	front surface recombination velocity
SDE	Sentaurus Structure Editor
sde	saw-damage-etch
SEM	scanning electron microscopy
SHJ	silicon hetero junction
SiH_3	silyl, a silane radical
SiH_4	silane
SiN_X	silicon nitride of stoichiometry X
SiO_2	silicon dioxide
SiO_X	silicon oxide of stoichiometry X
SRH	Shockley-Read-Hall
T	temperature
t_{ann}	annealing time
T_{SET}	set annealing temperature
τ	(minority) charge carrier lifetime
τ_{bulk}	bulk charge carrier lifetime
τ_{eff}	effective (minority) charge carrier lifetime
τ_{surf}	surface charge carrier lifetime
TCAD	technology computer aided design
TCO	transparent conductive oxide
TLM	transfer length method
TMAH	tetramethylammonium hydroxide
TOPCon	Tunnel Oxide Passivated Contact
TrPCD	transient photo conductance decay
UPS	ultra-violet photoelectron spectroscopy
V_{mpp}	voltage at the maximum power point
V_{OC}	open circuit voltage
WF	work function
WO_X	tungsten oxide of stoichiometry X
XPS	x-ray photoelectron spectroscopy
ZnO:Al	aluminium-doped zinc oxide

Appendix B

Simulation Parameters

Meshing Parameters

Table B.1 lists the minimum and maximum mesh dimensions for the selected layers and regions. The x-values refer to the spacing in the horizontal direction of the unit cell depicted in Figure 3.4 a, the y-values to the vertical direction.
The mesh is particularly dense at both the rear and the front side, as these are areas of high current density, high electric fields and high charge generation. In case of the front mesh, there is no change in optical generation in the direction parallel to the front side, hence the enhanced mesh density is mainly applied to the direction . At the rear side, especially close to the overlap/metallisation gap, current densities and electric fields have significant horizontal components, which is also reflected by the meshing strategy.

Table B.1: Meshing parameters

	x_{min} (μm)	x_{max} (μm)	y_{min} (μm)	y_{max} (μm)
c-Si front	5	5	0.05	0.75
c-Si bulk	3	8	3	8
c-Si contact	0.1	3	0.1	3
a-Si	0.001	5	0.001	5

a-Si:H Defect Parameters

The Tables B.2, B.3 and B.4 list the defect definitions for the respective a-Si:H layers.

Table B.2: Defect definitions for **intrinsic** a-Si:H

Conduction Band Tail	Total States: $1.8285714 \cdot 10^{21}\,\mathrm{cm}^{-3}$ Characteristic Energy: 0.035 eV e/h Capture Cross Section: $7 \cdot 10^{-16}\,\mathrm{cm}^2$
Valence Band Tail	Total States: $1.88 \cdot 10^{21}\,\mathrm{cm}^{-3}$ Characteristic Energy: 0.035 eV e/h Capture Cross Section: $7 \cdot 10^{-16}\,\mathrm{cm}^2$
Gaussian Donor	Total states: $1.3852163 \cdot 10^{16}\,\mathrm{cm}^{-3}$ E_V - E_{Peak}: 0.89 eV e/h Capture Cross Section: $3 \cdot 10^{-14}/3 \cdot 10^{-15}\,\mathrm{cm}^2$ Correlation Energy: 0.144 eV
Gaussian Acceptor	Total states: $1.3852163 \cdot 10^{16}\,\mathrm{cm}^{-3}$ E_V - E_{Peak}: 1.09 eV e/h Capture Cross Section: $3 \cdot 10^{-15}/3 \cdot 10^{-14}\,\mathrm{cm}^2$ Correlation Energy: 0.144 eV

Table B.3: Defect definitions for **n-type** a-Si:H

Conduction Band Tail	Total States: $2 \cdot 10^{21}\,\mathrm{cm}^{-3}$ Characteristic Energy: 0.068 eV e/h Capture Cross Section: $7 \cdot 10^{-16}\,\mathrm{cm}^2$
Valence Band Tail	Total States: $2 \cdot 10^{21}\,\mathrm{cm}^{-3}$ Characteristic Energy: 0.094 eV e/h Capture Cross Section: $7 \cdot 10^{-16}\,\mathrm{cm}^2$
Gaussian Donor	Total states: $1.3108103 \cdot 10^{20}\,\mathrm{cm}^{-3}$ E_V - E_{Peak}: 0.5 eV e/h Capture Cross Section: $3 \cdot 10^{-14}/3 \cdot 10^{-15}\,\mathrm{cm}^2$ Correlation Energy: 0.21 eV
Gaussian Acceptor	Total states: $1.3108103 \cdot 10^{20}\,\mathrm{cm}^{-3}$ E_V - E_{Peak}: 0.6 eV e/h Capture Cross Section: $3 \cdot 10^{-15}/3 \cdot 10^{-14}\,\mathrm{cm}^2$ Correlation Energy: 0.21 eV

Table B.4: Defect definitions for **p-type** a-Si:H

Conduction Band Tail	Total States: $2{\cdot}10^{21}\,\mathrm{cm}^{-3}$ Characteristic Energy: 0.08 eV e/h Capture Cross Section: $7{\cdot}10^{-16}\,\mathrm{cm}^2$
Valence Band Tail	Total States: $2{\cdot}10^{21}\,\mathrm{cm}^{-3}$ Characteristic Energy: 0.12 eV e/h Capture Cross Section: $7{\cdot}10^{-16}\,\mathrm{cm}^2$
Gaussian Donor	Total states: $1.3108103{\cdot}10^{20}\,\mathrm{cm}^{-3}$ E_V - E_{Peak}: 1.1 eV e/h Capture Cross Section: $3{\cdot}10^{-14}/3{\cdot}10^{-15}\,\mathrm{cm}^2$ Correlation Energy: 0.21 eV
Gaussian Acceptor	Total states: $1.3108103{\cdot}10^{20}\,\mathrm{cm}^{-3}$ E_V - E_{Peak}: 1.2 eV e/h Capture Cross Section: $3{\cdot}10^{-15}/3{\cdot}10^{-14}\,\mathrm{cm}^2$ Correlation Energy: 0.21 eV

Table B.5: Defect definitions for **Al defects** in a-Si:H

Level Acceptor	Total States: variable (0 to $9{\cdot}10^{18}\,\mathrm{cm}^{-3}$) E_V - E_{Defect}: 0.886 eV e/h Capture Cross Section: $3.1{\cdot}10^{-10}/3.6{\cdot}10^{-13}\,\mathrm{cm}^2$

Geometry Variation

Table B.6 lists the parameters that were adjusted for the simulations presented in section 6.2, compared to the ones outlined in section 3.3.

Table B.6: Parameter adjustments

ρ_p ($m\Omega cm^2$)	p-type a-Si:H N_A (cm^{-3})	intrinsic a-Si thickness below p-contact (nm)	S_{front} (cm/s)
330	$7.74 \cdot 10^{19}$	0.001	10
70	$8.24 \cdot 10^{19}$	0.001	10

Table B.7 lists the parameters that were used for the calculation of R_{Bulk} in section 6.2.

Table B.7: R_{Bulk} parameters

ρ_B Ωcm	N_D cm^{-3}	t_W μm	Δp cm^{-3}
3	$1.559 \cdot 10^{15}$	260	$1 \cdot 10^{15}$

Appendix C

Publications

Peer-reviewed Articles

- Johann-Christoph Stang, Thijs Franssen, Jan Haschke, Mathias Mews, Agnes Merkle, Robby Peibst, Bernd Rech, Lars Korte
  Optimised Metallisation for Interdigitated Back Contact Silicon Heterojunction Solar Cells
  Solar Rapid Research Letters (1), 1700021 (2017)

- Johann-Christoph Stang, Jan Haschke, Mathias Mews, Agnes Merkle, Robby Peibst, Bernd Rech, Lars Korte
  Aluminium Metallisation for Interdigitated Back Contact Silicon Heterojunction Solar Cells
  Japanese Journal of Applied Physics (56), 08MB22 (2017)

Proceeding Articles

- Johann-Christoph Stang, Max-Sebastian Hendrichs, Agnes Merkle, Robby Peibst, Bernd Stannowski, Lars Korte, Bernd Rech
  ITO-free Metallization for Interdigitated Back Contact Silicon Heterojunction Solar Cells
  Energy Procedia 124, 379-383 (2017)

Oral Presentations at International Conferences

- Johann-Christoph Stang, Thijs Franssen, Jan Haschke, Mathias Mews, Agnes Merkle, Robby Peibst, Bernd Rech, Lars Korte
  Optimised Metallisation for Interdigitated Back Contact Silicon Heterojunction Solar Cells
  26^{th} Photovoltaic Science and Engineering Conference "PVSEC",
  Singapore, 27^{th} October 2016

Poster Presentations at International Conferences

- Johann-Christoph Stang, Max-Sebastian Hendrichs, Agnes Merkle, Robby Peibst, Bernd Stannowski, Lars Korte, Bernd Rech
  ITO-free Metallization for Interdigitated Back Contact Silicon Heterojunction Solar Cells
  7^{th} International Conference on Crystalline Silicon Photovoltaics "SiliconPV",
  Freiburg, Germany, 5^{th} April 2017

Appendix D

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