High-Speed InP Heterojunction Bipolar Transistors and Integrated Circuits in Transferred Substrate Technology

vorgelegt von

Diplom - Physiker

Tomas Krämer

aus Stuttgart

Von der Fakultät IV - Elektrotechnik und Informatik
der Technischen Universität Berlin
zur Erlangung des akademischen Grades
Doktor der Naturwissenschaften
– Dr. rer. nat. –
genehmigte Dissertation

Promotionsausschuss:

Vorsitzender: Prof. Dr.-Ing. Heino Henke

Berichter: Prof. Dr. rer. nat. Günther Tränkle

Berichter: Prof. Dr.-Ing. Dr.-Ing. E.h. Herbert Reichl

Tag der wissenschaftlichen Aussprache: 03.05.2010

Berlin 2010

D 83

Acknowledgement

For my work I am indebted to many people. I want to thank Prof. Günther Tränkle. He lead me to this exciting field of research, gave me guidance in regular meetings and dedicated substantial resources of the Ferdinand Braun Institute to the project. Dr. Hans-Joachim Würfl backed the work by his continuous conceptual and personal support. He had confidence in my action and was always willing to share his profound technological knowledge. I would like to thank Dr. Chafik Meliani, Dr. Franz-Josef Schmückle, Dr. Matthias Rudolph and Dr. Friedrich Lenk for the team-work in circuit design, simulation, device modeling and layout, respectively. Dr. Richard Lossy, Kim Seon-Ohk, Dr. Peter Wolter introduced me to process technology. Dr. Andre Maaßdorf, Dr. Amy Liu and Dr. Frank Brunner provided the epitaxy. Dr. Michael Mai and Steffen Schulz conducted the majority of DC and RF measurements. Prof. Mark J.W. Rodwell inspired me with his comprehensive research on InP HBTs. Finally, I am grateful for my friends, family and Friederike. We enjoyed wonderful off time during these years.

Zusammenfassung

Die Entwicklung von Transistoren mit mehreren hundert Gigahertz (GHz) Betriebsfrequenz erschließt neue Anwendungen bei bildgebenden Systemen und in der breitbandigen Datenübertragung. Dank ihrer hervorragenden Materialeigenschaften nehmen InP-basierte Transistoren mit Grenzfrequenzen jenseits von 400 GHz eine Vorreiterrolle bei Höchstfrequenzanwendungen ein.

Im Rahmen der Arbeit wurde ein Verfahren zur Herstellung von InP/InGaAs/InP Doppel-Hetero-Bipolar-Transistoren (DHBT) entwickelt. Dabei wurden die Höchstfrequenzeigenschaften der Bauelemente mittels einer 3" Substrat-Transfer-Technologie (TS) optimiert. Diese ermöglicht den zueinander ausgerichteten, lithographischen Zugang zur Vorder- und Rückseite der DHBT Schichtstruktur. So kann ein linearer Aufbau des Bauelementes realisiert werden, ohne die dominanten parasitären Elemente herkömmlicher HBT Zuschnitte in Kauf nehmen zu müssen. Aus Kleinsignalextraktionen ergibt sich eine Halbierung der Basis – Kollektor Kapazität bezüglich nahezu baugleicher DHBTs, bei denen einmal lediglich der Kollektor unter der Basismetallisierung nicht entfernt wurde. Der wesentliche Schritt, der den direkten Zugang zuerst zur Vorder- und anschließend zur Rückseite gewährleistet, ist der Transfer des epitaktischen Schichtsystems vom 3" InP Wafer auf ein unabhängiges Trägersubstrat. Dazu wurde ein robustes Klebeverfahren mittels Benzocyclobuten (BCB) entwickelt, das eine homogene Kompositmatrix aus funktionaler DHBT Struktur und Trägersubstrat liefert, ohne durch Einschlüsse oder Bruchstellen in der Epitaxie limitiert zu sein. Einhergehend zur innovativen Formgebung der Transistoren werden Mikrostreifenleiterbahnen bereitgestellt. Im Schaltungsverbund unterstützt die dreidimensionale Integration von passiven Elementen und Komponenten auf dem Transfersubstrat die Funktionalität der Transistoren.

Die optimierte Bauelementtopologie schlägt sich in exzellenten Leistungsmerkmalen nieder. Transistoren mit einer Emitterfläche von $0.8 \times 5\,\mu m^2$ weisen ein $f_T = 420\,GHz$ und $f_{max} = 450\,GHz$ bei einer Durchbruchsspannung von $BV_{CEO} > 4.5\,V$ auf. Sie übernehmen damit die technologische Führerschaft doppelseitig prozessierter Höchstfrequenztransistoren. Sonstige HBTs mit vergleichbaren Emitterbreiten weisen deutlich geringere Werte von f_T und f_{max} auf. Gleichzeitig besitzen die

gefertigten Transistoren Arbeitspunkte jenseits von 100 mW und eine Ausgangsleistung $P_{out} > 13.5$ dBm bei 77 GHz im Sättigungsbetrieb. Das sind Spitzenwerte für Transistoren mit Grenzfrequenzen jenseits von 400 GHz. Desweiteren konnte die Tragfähigkeit ihrer Stromdichte auf $j_C > 18$ mA/µm^2 bezüglich publizierter TS HBTs versechsfacht werden. Dies ist ein wichtiger Beitrag, um die hervorragenden Hochfrequenz- und Leistungskennzahlen der Transistoren zu erzielen.

Konsistente Klein- und Großsignalmodellierung gemeinsam mit hoher Ausbeute und homogenen Bauelementeigenschaften über den 3" Wafer zeigen das Potential der TS Technologie für den Schaltungsentwurf. Deshalb wurde der TS DHBT Prozess zu einer MMIC-kompatiblen Technologie mit passiven Schaltungselementen weiterentwickelt. Vorabsimulationen und Modellierungen der passiven Elemente wurden zusammen mit den Transistormodellen zum Schaltungsentwurf genutzt und in anschließenden Messungen bestätigt. So sind Wanderwellenverstärker in TS Technologie konzipiert und mit einer Breitbandverstärkung von $G = 12.8$ dB und 3-dB Grenzfrequenz bis zu $f_c = 70$ GHz gefertigt worden – bis dato unerreicht für TS Breitbandverstärker.

Abstract

Research in high-speed transistors is driven by applications in imaging and wide band communication. Recent advances of InP-based transistors with several hundred gigahertz (GHz) operating frequencies qualify them for key components in such systems. Their outstanding properties make them the material system of choice for transistors exceeding 400 GHz.

This work examines design and performance issues of InP/InGaAs/InP double heterojunction bipolar transistors (DHBT). A transferred substrate (TS) technology has been developed to optimize high frequency performance. The 3" wafer-level process provides lithographic access to both the front- and backside of DHBT epitaxy aligned to each other. The resulting linear device set-up eliminates dominant transistor parasitics and relaxes design trade-offs. Small-signal extractions reveal a 50% reduced collector–base capacitance, when compared to equivalent DHBTs without collector backside removal. The essential step for gaining frontal access to both sides of the epitaxial structure is the substrate transfer. Therefore, a robust adhesive wafer bonding procedure via benzocyclobutene (BCB) has been developed. It yields for the first time a homogenous, crack and void-free composite matrix of functional InP DHBT epitaxy, transferred in a wafer-level scale. Along with the innovative TS DHBT set-up, a microstrip environment is provided, and the three-dimensional integration of passive elements and components on the transfer wafer supports functionality of the active devices.

The optimized device topology manifests in excellent device performance. Transistors of $0.8 \times 5\,\mu m^2$ emitter area feature $f_T =$ 420 GHz and $f_{max} =$ 450 GHz at breakdown voltages $BV_{CEO} > 4.5$ V. The devices define the cutting edge of double side processed millimeter-wave transistors. All other HBTs of comparable emitter width show significantly lower f_T and f_{max}. The more than six-fold increase in current density to 18 mA/μm^2 overcomes the limitation of previously reported TS HBTs and is an important contribution to outstanding high frequency and power performance of the devices. Transistors of $0.8 \times 5\,\mu m^2$ emitter area combine very high frequency performance with saturated output power $P_{out} > 13.5$ dBm at 77 GHz and DC power handling over 100 mW. To the author's knowledge, these are record values for transistors with f_T and f_{max} over 400 GHz. In addition, consistent small- and large-signal modeling, together with high yield and homogeneous device characteristics over the 3" wafer are demonstrated.

Finally, TS processing has been developed to a fully monolithic microwave integrated circuit (MMIC) compatible technology. Predictive simulation and modeling of passive elements are consistent with final measurements. Together with the transistor models, they have been utilized for circuit design. Traveling-wave amplifiers (TWA) have been designed and realized in the TS environment. They demonstrate a broadband gain $G = 12.8\,\mathrm{dB}$ within 3-dB cutoff frequency up to $f_c = 70\,\mathrm{GHz}$. This is the highest proven bandwidth of a broadband amplifier in TS technology.

Contents

1 Introduction

Research in high-speed transistors is driven by applications in imaging and wide band communication. The long-term aim is to open up the "terahertz gap" – the almost unutilized range between optics and electronics from 0.1 to 3 THz of the electromagnetic spectrum. This range of millimeter und submillimeter wavelength provides wider bandwidth, improved spatial resolution, and concealed objects can be made detectable due to specific absorption and transmission properties [1]. Imaging systems are projected in medical, security and industrial inspection [2]. The atmospheric attenuation windows at 94, 140, 220 and 340 GHz allow for high-resolution radar assistance in fog, dust or smoke [3]. Further applications are in wireless high bit-rate and secure short-range communications [4].

Recent advances of InP heterojunction bipolar transistors (HBT) with several hundred gigahertz operating frequencies qualify them for key components in such systems e.g. for amplifier stages and local oscillators. Compared to SiGe bipolar transistors, they achieve higher bandwidth at less demanding scaling nodes and attain higher breakdown voltage at a given device bandwidth.

These advantages originate from the high electron mobility of the InGaAs base [5], [6], larger valence band separation of the emitter–base heterojunction and thus increased base doping up to the epitaxial limit of incorporation [7], as well as higher peak electron velocity and breakdown field of the InP collector [8], [9]. Silicon on the other hand scores with high quality native oxide, important for device passivation. Table 1.1 summarizes key material parameters of selected semiconductors.

TABLE 1.1

MATERIAL PROPERTIES OF SELECTED SEMICONDUCTORS AT $T = 300$ K.

	Si [10]	Ge [10]	GaAs [11]	InP [12]	$In_{0.53}Ga_{0.47}As$ [6]	GaN [13]
bandgap (eV)	1.12	0.66	1.42	1.35	0.75	3.4
hole mobility (cm^2/Vs)	450	1800	400	140	300	30
electron mobility (cm^2/Vs)	1450	3900	8500	4600	12000	1000
electron peak velocity ($\times 10^7$ cm/s)	1	0.6	2	2.5	3	3.1
breakdown field (V/µm)	30	10	40	50	20	500

Nevertheless III-V technologies face constant pressure from silicon roadmaps [14]. The more than fifty years of collaborative efforts in developing Si processes and equipment not only result in lower cost and much higher scales of integration, but also is able to partly compensate for superior material properties available in compound semiconductors. To stay ahead, InP HBTs require continued development and adaptation in terms of device scaling together with surface passivation and yield as well as improved contact and thermal resistances. Up to now, SiGe HBTs of $0.12 \times 2.5\,\mu m^2$ emitter area have demonstrated highest current gain cutoff frequency $f_T = 300\,GHz$ and maximum oscillation frequency $f_{max} = 350\,GHz$ at collector current $I_C = 5.7\,mA$ and breakdown voltage $BV_{CEO} = 1.7\,V$ [15], [16], while $0.8 \times 5\,\mu m^2$ InP HBTs of this work feature $f_T = 420\,GHz$ and $f_{max} = 450\,GHz$ at $I_C = 27\,mA$ and $BV_{CEO} > 4.5\,V$. The InP HBTs of 0.8 µm minimum feature size are far from their scaling limit, and operating frequencies beyond one THz appear to be feasible in Chapter 7 by scaling down the transistors.

In the lower range of high frequency operation, InP transistors compete with GaN high electron mobility transistors (HEMT) in terms of power performance [17]. Record GaN HEMTs of 60 nm gate length and $2 \times 50\,\mu m$ width show peak values of $f_T = 190\,GHz$ at drain–source voltage $V_{DS} = 4\,V$ and $f_{max} = 240\,GHz$ at $V_{DS} = 10\,V$, with maximal drain–source currents $I_{DS}{}^{max} = 160\,mA$ [18], [19]. Within this work, first triple finger InP HBTs of $3 \times 0.8 \times 9\,\mu m^2$ emitter area simultaneously demonstrate an $f_T = 320\,GHz$ and $f_{max} = 340\,GHz$ at $V_{CE} = 2.1\,V$ with maximum collector current $I_C{}^{max} > 270\,mA$ – even though epitaxy was not optimized for power performance. In the end, the key arguments of low cost and very high yield for SiGe HBTs as well as the superior power handling capability of GaN HEMTs fade when aggressively scaled to approach high frequency performance of InP transistors.

In recent years, InP-based HEMTs as well as HBTs demonstrated highest operating frequencies [20], [21], [22], [23]. Each device concept has its applications, where its specific set of technology metrics excels over the other. For instance, HBTs are preferred for millimeter-wave oscillators. They feature very reproducible DC parameters scalable by epitaxial design rather than lithographic layout, superior transconductance and linearity, lower phase noise, but higher overall noise figure. HEMTs on the other hand are suited e.g. for low-noise amplifiers.

In this work, InP double heterojunction bipolar transistors (DHBT) have been developed in transferred substrate technology (TS) to optimize high frequency performance. The 3" wafer-level process provides lithographic access to both, front- and backside of the transistors, aligned to each other. Thus, emitter and collector contact are scalable in proportion to each other, independent of the base width. The resulting linear device set-up eliminates dominant transistor parasitics and relaxes design trade-offs. The essential step for gaining frontal access to both sides of the epitaxial DHBT structure is the substrate transfer procedure. Along with the innovative TS DHBT set-up, the three-dimensional (3D) integration of passive elements and operational components on the transfer wafer supports functionality of the active devices and paves the way towards highly functional composite electronics, e.g. of wafer-level, 3D heterogeneous integrated circuits. The TS approach is concordant with the ITRS trend line, favoring double side processes in the future to push the limits beyond conventional device performance: "… the ultimate MOSFET is projected to be the multiple-gate device" [24]. Corresponding processes are currently explored for Si-based transistors [25], [26].

Chapter 2 introduces the DHBT concept and TS device topology. The relevant figures of merits are identified. Device design is discussed in detail to assess key limiters and optimize transistor performance by the TS approach. The technological aspects of this work are presented in Chapter 3 – from epitaxy design and mask set layout to device processing. Process modules specific to the TS technology are motivated and described in detail. The fabricated transistors are evaluated and benchmarked in Chapter 4 in terms of yield, DC, RF and power performance. Large and small-signal models are derived for parameter extraction and circuit design. Chapter 5 reports on monolithic microwave integrated circuits (MMIC) results – from the conception of passive elements to the realization of complete circuits in TS technology. Chapter 6 summarizes the work and Chapter 7 briefly discusses advanced process modules for continued increase in bandwidth, assessing future TS DHBT capabilities, based on scaling laws, device results and models of this work.

2 HBT Theory & Design

In this Chapter, the DHBT concept und device topology is introduced, figures of merit for high-speed operation are specified and their dependence on device layout and band gap engineering techniques is investigated. Thermal effects and their impact on device design are discussed. Finally, key technological challenges to improve DHBT high frequency performance are identified.

2.1 HBT Concept

An HBT consists of three fundamental layers on top of each other: emitter, base and collector. The following discussion of high-speed InP HBTs focuses on npn transistors since electrons have higher charge carrier mobility. Basically the emitter sends out electrons, the base modulates the current and the collector drains them. The key point is that a small variation in base current I_B is transformed to a larger change in collector current I_C. The ratio is referred to as current gain $\beta = I_C / I_B$. The mechanisms that tend to reduce the current gain are the recombination of electrons with holes, either in the emitter–base space charge region or in the p-doped base and the reverse injection of holes from the base into the emitter.

What sets HBTs apart from bipolar junction transistors is the customized band engineering of the heterojunctions. In addition to the doping profile, the adequate composition of semiconductor material with different band gaps acts as a driving force on electrons and holes to control their distribution and flow almost separately [7]. If the wide band gap emitter and a narrow band gap base line up according to Fig. 2.1, an additional potential barrier in the valence band ΔE_V is formed that suppresses hole injection from the base into the emitter. This band offset at the heterointerface is the essence of an HBT and results in an exponentially enhanced current gain [27]:

$$\beta = \frac{I_C}{I_B} \propto \frac{N_E}{N_B} \cdot \exp^{\Delta E_V / kT} \tag{2.1.1}$$

Assuming constant current gain, the quotient of N_E / N_B can be lowered by the exponential factor as compared to simple bipolar junction transistors. Since $\Delta E_V \gg kT$ high base doping N_B allows thinning the base for reduced vertical transit times while maintaining its lateral sheet resistance, and lower emitter doping N_E reduces the junction capacitance for increased device speed.

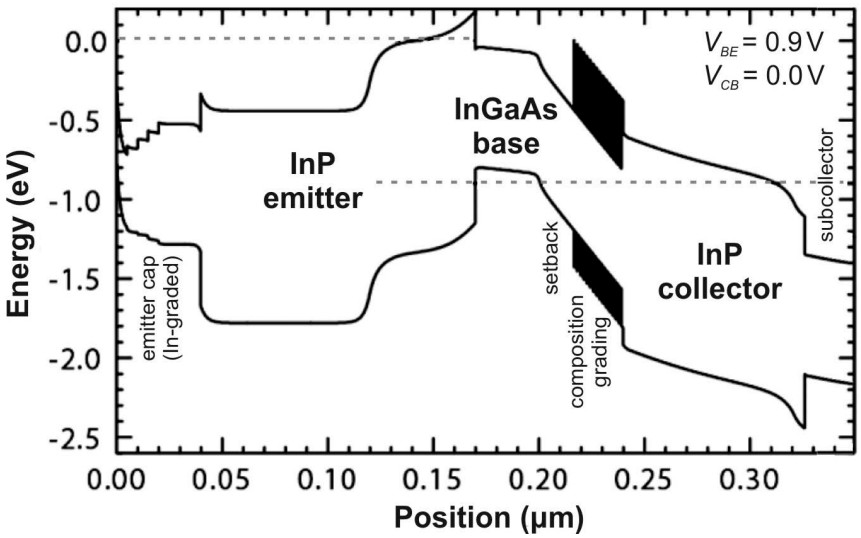

Fig. 2.1 Energy band diagram of TS DHBT epitaxial structure #724 of page 37.

2.2 Device Topology

The HBT is a vertical current transport device. Electrons flow from the emitter to the collector perpendicular to the epitaxial structure. The material growth focuses on composition, doping level and layer thickness. Critical device dimensions can be defined by the precision of epitaxial growth instead of lithography, e.g. charge carrier transit times are reduced by thinning the semiconductor layer stack. A typical heterostructure of this work is shown in Table 3.2 on page 37.

Afterwards, the epitaxial layer system is processed to define the lateral dimensions of the transistors. The lateral layout of the metal contacts has decisive influence on *RC* charging times and thus high-speed performance [28]. Lateral down scaling of HBTs reduces the capacitance along with the device area and minimizes access resistances, but contact resistances are increased. Besides the epitaxial structure and lateral dimensions that also affect thermal management and yield, process parameters e.g. for mesa underetch and contact resistivities have an important impact too.

The TS HBT set-up fabricated in this work is sketched in Fig. 2.2, vis-à-vis to a standard triple mesa HBT in Fig. 2.3. The following discussions will refer to the geometrical and parasitic parameters assigned in the figures. Vertical dimensions are indicated by the thickness d, whereas horizontal dimensions are labeled by the width W. The emitter, base and collector are electrically

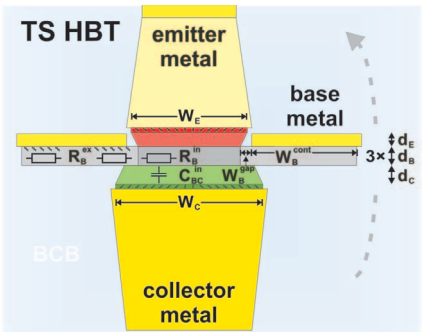

Fig. 2.2 TS HBT set-up with parasitics.

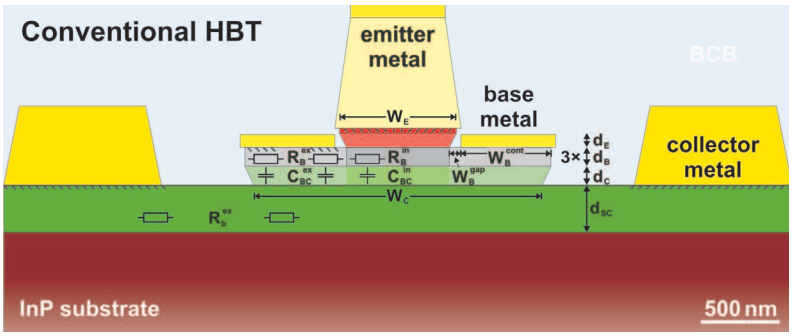

Fig. 2.3 Conventional triple mesa HBT set-up with parasitics.

linked by a metal-semiconductor contact to their respective interconnects. Once electrical contacts have been made, device layers are isolated by mesa formation. Because the emitter metal is the topmost layer, its contact lies congruent with the transistor junctions, the active region of the device. The base however must be accessed externally through a contact that resides adjacent to the emitter stripe. Spreading resistance underneath the emitter mesa within the intrinsic part of the base is so far unavoidable. The horizontal gap between the base contact and emitter mesa, as well as the contact itself adds additional extrinsic resistances.

Minimizing the emitter–base gap will reduce unwanted base gap resistance $R_{B,gap}$. Therefore, self-aligned base contacts are employed. After the emitter contact is formed, the emitter mesa is etched down to the base. During the emitter mesa etch, an undercut is formed. The undercut serves as a shadow-mask such that the base metal can be deposited overtop the emitter metal and its adjacent periphery to contact the base. Thus, only the emitter mesa undercut of ~50 nm contributes to $R_{B,gap}$. However, for self-aligned base contacts, the metal thickness is restricted by the emitter mesa height. The width of the base contacts has a lower limit, determined by the ohmic transfer length L_t of the base, by the access resistance and inductance of the base metal and by technological aspects as alignment and yield.

For a conventional triple mesa HBT, the base mesa ($W_{B,tot} = 2\,W_{B,cont} + 2\,W_{B,gap} + W_E$) defines the minimal width of the collector mesa and hence the collector–base capacitance C_{BC}. The intrinsic collector is the active region underneath the emitter mesa, where collector current I_C flows.

The rest is the extrinsic part. The subcollector is again accessed externally, this time adjacent to the base contacts, shaping a pyramidal device set-up. To drain the electrons below the base to the non-self-aligned contacts, the subcollector is several hundred nanometers thick.

For a TS HBT, the extrinsic collector–base capacitance does not exist at all. Here contacts and mesa of emitter and base are processed from the front side. Next, the wafer is mounted upside down on a new support. After removing the epitaxial substrate, the collector is defined by lithography almost congruent to the emitter from the backside and independent of the base width. The resulting linear instead of pyramidal device set-up eliminates the dominant collector–base capacitance C_{BC} to its intrinsic fraction $C_{BC,in}$ and relaxes design trade-offs. A lateral electroconductive subcollector is not required and the span of the base contacts becomes uncritical. Motivation and benefits of the TS process are further discussed in section 2.4.3d. Fabrication details are given in section 3.4.

2.3 Figures of Merit

2.3.1 Current Gain Cutoff Frequency f_T

The HBT current gain cutoff frequency f_T is defined as the frequency at which the common-emitter small-signal current gain h_{21} decreases to unity [29].

$$\frac{1}{2\pi f_T} = \tau_B + \tau_C + (R_E + R_C)C_{BC} + \frac{\eta_C kT}{qI_C}\left(C_{jBE} + C_{BC}\right) \tag{2.3.1}$$

τ_B and τ_C are the base and collector transit times. R_E and R_C are the series resistance of the emitter and collector. C_{BC} is the collector–base capacitance, C_{jBE} the emitter–base depletion capacitance and $(\eta_C kT/qI_C)^{-1}$ the transconductance g_m of the HBT. The two-port parameter h_{21} is determined with base and collector under short-circuit condition. As the heterostructure is vertically scaled down, base and collector transit delay decreases. However, the charging time of collector–base capacitance increases. Regardless of the value of f_T, transistors cannot provide power gain at frequencies above f_{max} and a good design should pay attention to both.

2.3.2 Maximum Oscillation Frequency f_{max}

The HBT maximum oscillation frequency f_{max} is the frequency at which the unilateral power gain of the transistor rolls off to unity [30].

$$f_{max} = \sqrt{\frac{f_T}{8\pi\,[RC]_{eff}}} \tag{2.3.2}$$

The collector–base junction of a conventional triple mesa HBT is a distributed network, shown in Fig. 2.3, and $[RC]_{eff}$ represents its effective, weighted time constant [31]. Usually the base resistance is much larger than the emitter and collector resistances. Their effects become secondary and only the distributed collector–base network needs to be considered. Each component of C_{BC} should only account for the resistance in its path when determining the charging time constant. Utilizing the expressions R_B of (2.4.6) and C_{BC} of (2.4.13) results in:

$$\begin{aligned}[RC]_{eff} = \; & R_B C_{BC,in} + \left(R_{B,cont} + \tfrac{1}{2} R_{B,gap}\right) C_{BC,gap} + R_{B,vert} C_{BC,ex} \\ & + R_{B,pad} C_{BC,pad}\end{aligned} \tag{2.3.3}$$

The collector–base capacitance underneath the emitter stripe $C_{BC,in}$ is charged through the entire base resistance R_B. The interstitial capacitance $C_{BC,gap}$ between the emitter mesa and base contact is charged through ($R_{B,cont} + R_{B,gap}/2$). The extrinsic collector–base capacitance $C_{BC,ex}$ underneath the base metal is charged by currents traversing vertically through the contact of the resistivity $\rho_{B,c}$ ($\Omega\mu m^2$) above it, having a resistance $R_{B,vert} = \rho_{B,c}/(2L_E W_{B,cont})$. Just as the base, access pad capacitance $C_{BC,pad}$ is charged through $R_{B,pad} = \rho_{B,c}/A_{pad}$. The TS process minimizes the collector–base junction to its intrinsic fraction $R_B C_{BC,in}$, described in section 2.4.3d. The f_T and f_{max} of a transistor are often cited to give a first-order summary of the device transit delays and magnitude of its dominant parasitics. Within this study, it is intended to develop a device technology that satisfies both. The theoretical background of DHBT designs to maximize and balance f_T and f_{max} is described below.

2.4 HBT Design

2.4.1 Emitter

a. Emitter Resistance

The delay term $R_E C_{BC}$ in (2.3.1) is an important limiter of f_T. The metal-semiconductor contact $R_{E,cont}$ dominates the emitter resistance R_E, with a small contribution from the emitter mesa $R_{E,mesa}$.

$$R_E = R_{E,cont} + R_{E,mesa}$$
$$R_{E,cont} = \frac{\rho_{E,c}}{A_{E,cont}} \quad , \qquad R_{E,mesa} = \rho_{E,mesa}\frac{d_E}{A_{jE}} \tag{2.4.1}$$

In which $\rho_{E,c}$ is the specific emitter contact resistance and $\rho_{E,mesa}$ is the resistivity in the mesa region. For submicron scaling however, the emitter junction area A_{jE} has to be considered. Lateral undercut of the contact area $A_{E,cont}$ during the wet etch and surface depletion at the low doped emitter junction consumes an increasing fraction. Additionally, self-aligned base contacts require a minimum height of the mesa d_E, which cannot be scaled down according to the emitter width.

The ohmic contact resistance can be minimized through the combined use of a narrow band gap semiconductor that is highly doped, proper surface preparation before metal deposition to reduce surface states, and choice of interfacial metal [32]. Compared to the subcollector, defects due to lattice mismatch or high doping levels are of less concern since the emitter cap is the topmost layer of epitaxial growth.

b. Emitter Capacitance

The emitter–base layer system determines the emitter charging time $(kT/q)\cdot C_{jBE}/I_C$ in (2.3.1). Two opposing mechanism have to be traded off. On the one hand, a high electron density $n_{(x)}$ must be present within the emitter–base junction to support high current density without a substantial potential drop V_{BE} in the depletion layer. Thus, spread and charge storage of the depletion layer is minimized. On the other hand, lower emitter doping N_E widens the depletion region X_{BE} to reduce the depletion capacitance C_{jBE}^*, with a base doping $N_B \gg N_E$.

$$C_{jBE}{}^{*} = \frac{\varepsilon_{InP} A_{jE}}{X_{BE\,(V_{BE})}} = \sqrt{\frac{\varepsilon_{InP}\, q\, N_E\, {A_{jE}}^2}{2(\Phi_{BE} - V_{BE})}} \tag{2.4.2}$$

The total emitter–base capacitance C_{jBE} reveals the trade-off [33].

$$\frac{kT}{q} \cdot \frac{C_{jBE}}{I_C} = \frac{kT}{q} \cdot \frac{\varepsilon_{InP}\, A_{jE}}{X_{BE}\, I_C} + \frac{\gamma\, X_{BE}\, d_B}{D_n} \cdot \int_0^1 \frac{n_{(\xi X_{BE})}}{n_{(X_{BE})}} \xi^2 \mathrm{d}\xi\,, \qquad \xi = \frac{x}{X_{BE}} \tag{2.4.3}$$

The first term describes the depletion capacitance and is minimized by high bias current densities $j = I_C/A_{jE}$. Whereas the second term reflects stored charge carriers within the depletion layer and is reduced by shrinking the depletion layer X_{BE} or base thickness d_B. D_n is the diffusivity of electrons in the base and γ is a factor involving the base band gap grading ($\gamma \approx 1$, for ungraded base).

c. Emitter–Base Grade

Under normal operation, the emitter–base junction is forward biased. This lowers the emitter–base potential and injects electrons into the base. The abrupt emitter–base junction in an InP/InGaAs HBT shows a conduction band spike which impedes the electron flow. If the hetero-junction between base and emitter is optimally graded, the conduction band spike can be removed and all its band gap difference occurs in the valence band [34]. The additional valence barrier improves blocking of hole injection into the emitter and thus decreasing the turn-on voltage. However, grading presents many challenges and the grade design of the biased emitter–base junction is not straightforward [35]. For an abrupt emitter–base junction it can be argued that tunneling can substantially lower the launching threshold [36]. The electrons that surmount the conduction band spike are injected into the base. The ballistic transport reduces the base and collector transit times [37].

2.4.2 Base

a. Base Transit Time

The time it takes for an electron entering from the emitter to traverse across the base is the base transit time τ_B:

$$\tau_B = \frac{{d_B}^2}{2D_n} + \frac{d_B}{v_{B,exit}} \tag{2.4.4}$$

In the limit of small base thickness d_B (~20 nm) the transport is not purely governed by the electron minority diffusivity D_n in the base [38]. The concentration of electrons on the collector side becomes dependent on the velocity with which they exit the base. The second term $d_B / v_{B,exit}$ accounts for the exit velocity proportional to the thermionic emission velocity $v_{B,exit} \propto (2k_BT/\pi m_e^*)^{1/2}$ [37]. This transit time calculation assumes uniform composition and doping in the base.

To reduce τ_B, an intrinsic electric field can be established to accelerate electrons across the base by band gap [39] or doping grading [40], [41]. In band gap grading, the material composition is changed throughout the base. In doping grading, the base doping level is changed – heavily doped at the emitter interface and lower doped at the collector. Assuming the grading of the base conduction band is linear, (2.4.4) is rewritten as [42],

$$\tau_B = \frac{{d_B}^2}{D_n} \cdot \left[1 - \frac{kT}{\Delta E}\left(1 - \exp^{-\Delta E/kT} \right) \right] + \frac{d_B}{v_{B,exit}} \cdot \left(1 - \exp^{-\Delta E/kT} \right) \tag{2.4.5}$$

where ΔE is the energy difference across the base conduction band. The DHBTs in this work employ a grade producing a $\Delta E \approx 50$ meV. This in turn reduces τ_B by 50% compared to an ungraded base. Derived from the drift-diffusion relationship, (2.4.5) is only accurate if the predicted τ_B is large in comparison with the momentum relaxation time. It does not consider hot carrier or quasi-ballistic transport in the base due to the abrupt InP/InGaAs emitter – base junction [43].

b. Base Resistance

Three components of the HBTs in Fig. 2.2 and Fig. 2.3 contribute to the base resistance R_B and lower f_{max} in (2.3.2). These are the metal-semiconductor contact resistance $R_{B,cont}$, the gap resistance $R_{B,gap}$ between base contact and emitter mesa and the intrinsic spreading resistance $R_{B,in}$ under the emitter [33].

$$R_B = R_{B,cont} + R_{B,gap} + R_{B,in} \tag{2.4.6}$$

$$R_{B,cont} = \sqrt{\rho_{B,s}\rho_{B,c}} / 2L_E \cdot \coth\left[W_{B,cont}/L_t\right]$$
$$R_{B,gap} = \rho_{B,s} W_{B,gap} / 2L_E$$
$$R_{B,in} = \rho_{B,s} W_E / 12L_E$$

L_E is the emitter length, $\rho_{B,s}$ (Ω/sq.) and $\rho_{B,c}$ (Ωμm^2) are the specific sheet and contact resistivities of the base and $L_t = (\rho_{B,c}/\rho_{B,s})^{1/2}$ is the ohmic transfer length. The intrinsic base resistance $R_{B,in}$ depends on emitter width W_E. This is an important argument for HBT down scaling. For state-of-the art triple mesa HBT technology, the lower limit of the base contact width $W_{B,cont}{}^{min}$ is around 0.4 μm. It is determined by the ohmic transfer length L_t to prevent exponential increases of $R_{B,cont}$ in Fig. 2.4, by access resistance and inductance of the base metal and by technological aspect as alignment and yield. This limit also governs the extrinsic collector – base capacitance of a conventional DHBT in section 2.4.3d underneath the base. To show more clearly how the base resistance varies with the emitter and base dimensions, (2.4.6) can be rewritten.

$$R_B = \frac{\rho_{B,s}}{2L_E} \cdot \left(L_t \coth\left[\frac{W_{B,cont}}{L_t}\right] + W_{B,gap} + \frac{W_E}{6} \right) \tag{2.4.7}$$

Compared to the emitter or collector resistance, the base sheet resistivity $\rho_{B,s} = (q\mu_h N_B d_B)^{-1}$ is significant. The reason for this is the low hole mobility $\mu_{h,base} \approx 50\,\mathrm{cm}^2/\mathrm{Vs}$ and minimized base thickness $d_B < 40\,\mathrm{nm}$ for optimized transit times. As the base becomes progressively thinner, surface depletion in the gap region becomes an issue [44]. Extensive base doping $N_B > 5{\cdot}10^{19}\,\mathrm{cm}^{-3}$ reduces the sheet resistivity and improves contact resistivity. The self-aligned base contacts keep the gap spacing $W_{B,gap}$ narrow.

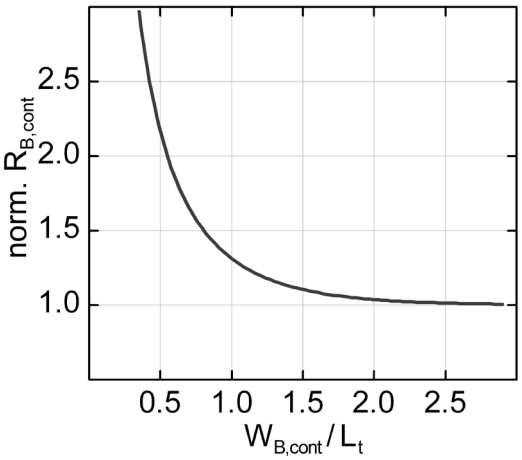

Fig. 2.4 Normalized dependence of the base contact resistance $R_{B,cont}$ on the ratio of contact width $W_{B,cont}$ to ohmic transfer length L_t.

2.4.3 Collector

The collector is probably the region of an HBT, which is changed most to suit the designer's goal. A thicker collector directly translates into higher breakdown voltage for power devices. A thinner collector results in shorter transit times and thus higher f_T, but increased C_{BC} and thus decreased f_{max}. The doping level can be raised to enhance the current tolerance or be lowered to achieve full depletion over a wider biasing range. In this work, the collector is designed to be fully depleted at zero bias.

HBT can be divided into two types of collector. The single heterojunction bipolar transistor (SHBT) uses the same material in the base and the collector, e.g. lattice matched $In_{0.53}Ga_{0.47}As$. The double heterojunction bipolar transistor (DHBT) uses instead a wider band gap material such as InP in the collector. SHBTs have achieved impressive device performance [45] and are comparably easier to design and grow. The main advantage of a wide band gap collector is the increased critical electric field. For InP, it is more than double that of $In_{0.53}Ga_{0.47}As$. Since the electric field in the depleted collector is inversely proportional to the layer's thickness, InP can provide a thinner collector for a required breakdown voltage and, hence, relax the fundamental trade-off between breakdown and transit time [46]. In addition, heat management becomes a critical issue at high current densities. InP shows a thermal conductivity in Table 2.1 of more than one order of magnitude above $In_{0.53}Ga_{0.47}As$.

According to the band lineup of the base in Fig. 2.5, DHBTs are divided into type-I and type-II. For type-I DHBTs, the lowered conduction band lineup $\Delta E_c = 0.25\,\text{eV}$ of the base causes a barrier at the abrupt base–collector heterojunction which hinders the electrons from entering the collector [47]. It must be removed, otherwise the device performance will be severely degraded. Type-II DHBTs feature an elevated conduction band lineup e.g. of the GaAsSb base and, therefore, do not show current blocking [48], [49].

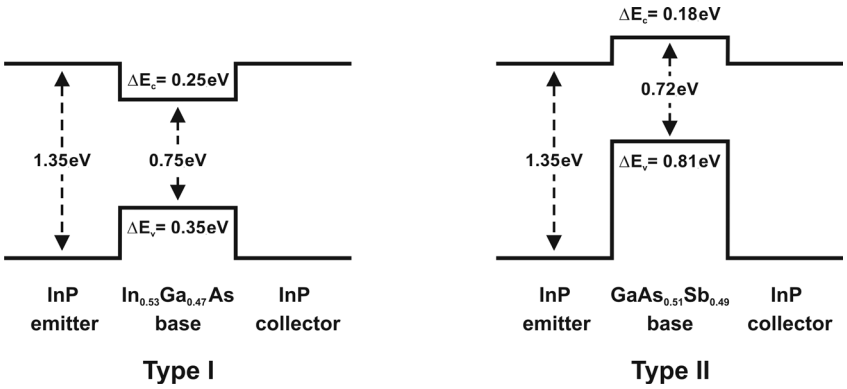

Fig. 2.5 Schematic band lineup of InP-based DHBT material systems [50], [51].

a. Collector Grade

In order to prevent current blocking in type-I InP/$In_{0.53}Ga_{0.47}As$/InP DHBTs, the impeding barrier is removed by grading the energy gap from the base to the collector. Three major approaches exist to smooth out the conduction band discontinuity.

- The first approach is to keep a setback layer of $In_{0.53}Ga_{0.47}As$ next to the base and switch over to InP further down in the collector. If the potential drop from the conduction band in the base down to the onset of InP is in excess of the discontinuity offset, much of the current blocking effect will be removed [47].
- The second approach employs $In_{1-x}Ga_xAs_yP_{1-y}$ quaternary, by varying the composition and, hence, band structure from $In_{0.53}Ga_{0.47}As$ to InP more continuously [52].
- The third approach uses a chirped superlattice of e.g. thin $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ layers creating a tunable intermediate band gap [53], [54].

Any of these approaches requires careful design and implementation in order to eliminate deleterious effects of the conduction band offset on the DC and RF performances.

The DHBTs in this work utilize an InP/$In_{0.53}Ga_{0.47}As$/InP stack of emitter, base and collector with a type-I conduction band discontinuity. They make use of the superlattice as well as the quaternary approach, each combined with a setback. The superlattice acts to smooth out the energy discontinuity such that there is no effective potential drop across the length of the grade d_{grade}. To establish the required electric field across the graded region, a dipole is incorporated between the p^+ base ahead and a subsequent n^+ pulse layer [55]. The sheet charge density N_δ and layer thickness d_δ can be estimated by [56]:

$$N_\delta d_\delta = \frac{\varepsilon_0 \varepsilon_r \Delta E_c}{q^2 d_{grade}} \tag{2.4.8}$$

To ensure electrons traverse through the grading and are not reflected, kinetic energy is supplied to them over the setback region. This requires an additional potential drop of the order ΔE_c, not included in (2.4.8).

b. Collector Transit Time

Electrons injected from the base into the collector induce a displacement current across the junction capacitance. This renders the collector signal delay τ_C less than the time an individual electron requires to transit the collector thickness d_C. While the time of flight only depends on the average velocity, the signal delay depends on the velocity profile. For a general velocity profile $v_{(x)}$, the mean delay is given by [57], [58]:

$$\tau_C = \int_0^{d_C} \frac{1 - x/d_C}{v_{(x)}}\, dx \;=:\; \frac{d_C}{2v_C} \tag{2.4.9}$$

Thus, the velocity in the collector nearest to the base is most important. The velocity in this region is also relevant for the base transit time in the term of the base exit velocity $v_{B,exit}$ in (2.4.4). Assuming an equidistant step profile of two different velocities v_1 and v_2 provides an instructive example. The comparative scenarios of $v_1 = v$, $v_2 = v/2$ and vice versa result in a 40% difference of τ_C. This underlines the need for properly designed collector grades.

c. *Maximum Current Density (Kirk Effect)*

The emitter–base and collector–base charging times in (2.3.1) decrease with increasing current density. Since Kirk effect limits the maximum current density, it plays an important role in limiting the bandwidth of DHBTs. As the collector current density $j_{(x)}$ is increased, the injected electrons screen the space charge of the collector doping N_C and alter the electric field. To estimate how the current density bias the band structure, Poisson's equation is modified to account for the injected charge distribution by the second term,

$$-\frac{d^2\Phi}{dx^2} = \frac{dE}{dx} = \frac{1}{\varepsilon_0 \varepsilon_r} \cdot \left[qN_C - \frac{j_{(x)}}{v_{(x)}} \right] \tag{2.4.10}$$

where $v_{(x)}$ is the electron velocity in the collector. The Kirk current threshold j_{Kirk} is reached when the potential of the collector region adjacent to the base ($x = 0$) equals the sum of junction built-in potential Φ_{bi} and applied voltage V_{CB} and the electric field becomes zero ($E_{(x=0)} = 0$). Assuming $j_{(x)}$ and $v_{(x)} = v_C$ to be constant and integrating twice (2.4.10) over the fully depleted collector of thickness d_C with the Kirk boundary conditions yields [59]:

$$j_{Kirk} = 2\varepsilon_0 \varepsilon_r v_C \cdot \frac{(\Phi_{bi} + V_{CB})}{{d_C}^2} + v_C \cdot qN_C \tag{2.4.11}$$

By increasing the current density $j > j_{max}$, the boundary condition $E_{(x)} = 0$ extends into the collector. For SHBTs, holes are no longer confined to the base region as the conduction and valence bands progressively flatten within the collector. Due to the base push-out, the base transit time τ_B and collector–base capacitance C_{BC} increase, while the collector transit time τ_C slightly decreases. This is the classical definition of the Kirk effect [60].

For DHBTs, the valence band discontinuity at the base–collector heterojunction blocks holes from entering the collector region. This prevents holes from compensating the excessive electron density. Thus, an electric field is generated which acts in reverse to the injected collector current. This current barrier will cause a collapse in the current gain and the retarded electron velocity will significantly increase τ_C – a phenomenon not experienced by SHBTs.

One might be led to raise the Kirk current threshold just by increasing the collector doping. However, it should be low enough to avoid depletion layer collapse ($E_{(x=d_C)}=0$) at minimum operation bias $V_{CB,min}$ and zero current ($j=0$), in order not to increase the collector–base capacitance. From (2.4.11) this is satisfied when:

$$N_{C,max} = \frac{2\varepsilon_0\varepsilon_r}{q} \cdot \frac{(\Phi_{bi} + V_{CB,min})}{{d_C}^2} \tag{2.4.12}$$

The important conclusion of (2.4.11) and (2.4.12) is the $1/{d_C}^2$–dependence of the Kirk current j_{Kirk} for the vertical scaling of collector thickness d_C. If a setback and a dipole field across the grade are incorporated, the respective potential drops over them consume $\Phi_{setback}$ and Φ_{grade}. Consequently, the collector doping in (2.4.12) has to be reduced by $2N_\delta d_\delta \cdot (d_{setback} + d_{grade})/{d_C}^2$, where N_δ and d_δ are the doping concentration and thickness of the pulse layer in (2.4.8) and $d_{setback}$ and d_{grade} are the thickness of setback and grade. This can be a significant reduction of maximum collector doping and must be accounted for in the epitaxial design.

d. Collector–Base Capacitance and Charging Time

Reducing the collector–base capacitance in (2.3.1) and (2.3.2) is a key issue to improve RF device performance. From the viewpoint of a device designer, the collector–base junction A_{jC} is only required underneath the emitter mesa area A_{jE}, where current flows [61]. TS DHBTs in Fig. 2.2 are capable of implementing this ideal shape $A_{jE}=A_{jC}$ and eliminating the collector–base capacitance C_{BC} of conventional triple mesa DHBTs in Fig. 2.3, with

$$C_{BC} = C_{BC,in} + C_{BC,gap} + C_{BC,ex} + C_{BC,pad} \tag{2.4.13}$$

$$C_{BC,in} = \frac{\varepsilon_0\varepsilon_r L_E W_E}{d_C}, \qquad C_{BC,gap} = \frac{2\varepsilon_0\varepsilon_r L_E W_{B,gap}}{d_C}$$

$$C_{BC,ex} = \frac{2\varepsilon_0\varepsilon_r L_E W_{B,cont}}{d_C}, \qquad C_{BC,pad} = \frac{\varepsilon_0\varepsilon_r A_{pad}}{d_C}$$

to its intrinsic fraction $C_{BC,in}$. L_E and W_E are the length and width of the emitter junction, $W_{B,cont}$ is the width of the base metal, $W_{B,gap}$ the spacing between base contact and emitter mesa, d_C is the collector thickness and A_{pad} is the base pad area, which can be a significant fraction of downsized

DHBTs. From the perspective of a given technology, the DHBT scaling limit is the minimum feature size. It governs the dimensions of W_E, $W_{B,cont}$, A_{pad}. Thus $C_{BC,in}$, $C_{BC,ex}$, $C_{BC,pad}$ are at least of the same order of magnitude. Note, the collector–base capacitance of TS DHBTs can be directly scaled with the emitter width, whereas for conventional DHBTs it cannot. There, it is restricted in first approximation by the minimum width of the base contacts $W_{B,cont}{}^{min}$ of section 2.4.2b and its extrinsic capacitance underneath. The mesa under the base pad, responsible for the base pad capacitance $C_{BC,pad}$, can be completely removed during backside processing of TS DHBTs. Consequently, the TS technology can realize a significant reduction to $C_{BC} = C_{BC,in}$.

For TS DHBTs, the charging time $[RC]_{eff}$ in (2.3.3) simplifies, with the base resistance R_B of (2.4.6) and the total collector–base capacitance of $C_{BC} = C_{BC,in}$ in (2.4.13).

$$[RC]_{eff} = \frac{1}{2}\varepsilon_0\varepsilon_r\,\rho_{B,s}\left[L_t\coth\left(\frac{W_B}{L_t}\right) + W_{B,gap} + \frac{W_E}{6}\right]\cdot\frac{W_E}{d_C} \tag{2.4.14}$$

Vertical scaling of the collector thickness d_C, e.g. to increase j_{Kirk} (2.4.11) and f_T (2.4.1), can now be balanced by lateral scaling of emitter and collector junction widths. With submicron scaling, the first summand in (2.4.14) dominates, and $f_{max} \propto W_E{}^{-1/2}$ increases as the inverse square root of the process minimum feature size. Scaling conventional DHBTs beyond $W_{B,cont}{}^{min}$, the extrinsic parasitics of R_B and C_{BC} dominate, imposing fundamental restrictions for f_{max}.

e. Subcollector Resistance

The subcollector drains the electrons of the collector to the contact metal. It also serves as thermal shunt, since the collector–base junction is the main source of power dissipation in DHBTs [62]. Therefore, the subcollector design has to account for electrical and thermal resistance. To improve the ohmic contact, a highly doped $In_{0.53}Ga_{0.47}As$ layer is used. It is kept thin to minimize the thermal resistance. Compared to the emitter cap, doping levels are decreased, since defects within subsequent grown epitaxial layers are of concern. Indium-rich, narrow band gap contacts are not introduced, because of their lattice mismatch.

The subcollector of the TS DHBT in Fig. 2.2 differs from the conventional set-up in Fig. 2.3 just as the collector does in the previous section. The subcollector is similar to the emitter contact and parameters are assigned analog to (2.4.1).

$$R_C = R_{C,cont} + R_{C,mesa}$$
$$R_{C,cont} = \frac{\rho_{C,c}}{A_{C,cont}}\ , \qquad R_{C,mesa} = \rho_{C,mesa}\frac{d_C}{A_{jC}} \tag{2.4.15}$$

A several hundred nanometer thick subcollector as for conventional DHBTs is not required to drain off the electrons below the base to the external contacts. The direct metal contact underneath the intrinsic collector of TS DHBTs eliminates the extrinsic collector–base capacitance, bypasses the lateral access resistance of the subcollector and provides a metal heat sink for thermal dissipation in the collector. For additional heat sinking, the metal contacts could be enlarged.

2.5 Thermal Management

2.5.1 Power Dissipation & Heat Sinking

InP DHBTs require high current densities for high-speed operation. Thermal management becomes a critical issue, since thermally-driven failures limit current densities. DHBTs generate heat primarily in the collector depletion region and in the upper portions of the subcollector, where energetic electrons undergo scattering [62]. Besides the Kirk effect, this can limit the maximum operating current density [63]. It is instructive to examine the dissipated power P_D in the collector region underneath the emitter area A_{jE}, when operating at the Kirk current threshold j_{Kirk} set by (2.4.11) with (2.4.12). Under normal operating conditions, the conduction band difference between the base and subcollector is about V_{CE}. Then the dissipated power density P_D/A_{jE} is approximately:

$$P_D/A_{jE} \approx j_{\mathrm{Kirk}} V_{CE} = 4\varepsilon_0\varepsilon_r v_C \cdot {V_{CE}}^2/{d_C}^2 \tag{2.5.1}$$

The resulting temperature rise $\Delta T = R_{th} \cdot P_D$ depends on the thermal resistance R_{th} and thus on device geometry and layer structure [64], [65]. Multi emitter finger designs have to account for additional mutual thermal coupling [66]. Smaller devices generally show higher thermal resistance, since the dissipated power density and, therefore, temperature is increased at equal power levels. In the device, heat is removed by thermal conduction. The TS DHBT provides two major paths

– the heat sink of emitter and collector contact metal. Sidewalls are passivated by dielectric material with marginal thermal conductivity. The thermal properties of constitutive materials are displayed in Table 2.1. They reveal the trade-off between electrical and thermal contact optimization. Low bandgap ternary materials like InGaAs produce reduced ohmic but increased thermal resistance contacts. Accordingly, the layer thickness is minimized. In addition, the thermal conductivity κ of InP and InGaAs decreases with lattice temperature by $\kappa \propto T^{-n}$, ($n_{InP} = 1.55$, $n_{In_{0.47}Ga_{0.53}As} = 1.37$) [67]. Heavy doping in GaAs reduces the thermal conductivity [68] and a similar effect will occur in InP and InGaAs, but no experimental data is available. Schottky contacts deposited directly on the InP collector could be an alternative [69].

TABLE 2.1

THERMAL PROPERTIES AT ROOM TEMPERATURE OF SELECTED MATERIALS.

Material	**Thermal Conductivity ($Wm^{-1}K^{-1}$)**	**Thermal Expansion ($10^{-6}\cdot K^{-1}$)**	**Reference**
InP	67	4.6	[70]
$In_{0.47}Ga_{0.53}As$	5	5.66	[71]
AlN (ceramic)	>170	4.5	[72]
SiN_x (PECVD)	~1.2	~2.5	[73]
BCB (polymer)	~0.3	~45	[74]
Au	315	14.2	
Pt	72	9	
Ti	22	8.9	
Si	156	2.6	[75]
GaAs	45	6	[11]

2.5.2 Thermal Effects

An important self-heating effect in DHBTs is the emitter–base voltage regression. Here the emitter–base voltage V_{BE} required to maintain a certain collector current I_C decreases ($\partial V_{BE}/\partial I_C|_{V_{CE}=const} < 0$) as the junction temperature rises with the dissipated power $P_D = I_C V_{CE} + I_B V_{BE}$. When driven by constant emitter–base voltage V_{BE}, the regression introduces a threshold of thermal instability that limits the biasing range of safe operation [76].

$$I_c < \frac{\eta kT/q}{\theta R_{th} V_{CE} - R_E} \tag{2.5.2}$$

Where R_{th} is the device thermal resistance, $\theta = -\partial V_{BE}/\partial T|_{I_c=const}$ the thermo-electric feedback coefficient and R_E the emitter resistance. Beyond this limit, an arbitrary inhomogeneous temperature distribution of the emitter base junction (e.g. due to inherent geometrical discontinuities of finite emitter dimensions or multifinger set-up) enhances local current flow in hotter regions. This again generates additional heat on site and current concentration, stimulating a local thermal-electric feedback loop [77], which may cause thermal runaway [78]. Optimized heat sinking of the emitter junction and emitter ballasting are options to extend the biasing area of safe operation in (2.5.2). However, additional ballast resistance delays the charging time $R_E C_{BC}$ of f_T in (2.3.1).

Another drive for premature breakdown by elevated junction temperature is the increased hole current, injected back from the collector into the base [79]. Narrow band gap InGaAs setback and InGaAs/InAlAs grade, incorporated in the collector, can substantially contribute to this current [80], [81].

The temperature rise also reduces the transconductance $qI_C/(\eta_C kT)$ in (2.3.1) and prolongs electron transit time τ_C in the collector, since enhanced scattering retards the saturated velocity. A 75 K temperature rise due to self-heating, reduces f_T by approx. 10%. [82]. Further on, device self-heating affects reliability due to the Arrhenius relationship between temperature and median-time-to-failure [83].

2.6 Scaling Guidelines

The previous sections reviewed the relevant DHBT transit and RC delays. From the inter-dependent results, instructive scaling guidelines for device design are derived here, to increase bandwidth by a factor α [33]. The starting point is to reduce all significant transit delays and capacitances of the TS DHBT by an appropriate factor α^{-x}, while maintaining constant all resistances R, operating voltages V, collector current I_C and transconductance $g_m = qI_C/(\eta_C kT)$. Resistivities ρ, current densities j and electric fields E will already be increased by the geometrical scaling.

Reducing the collector depletion layer thickness d_C by α^{-1} (2.4.9) and base thickness d_B by slightly more than $\alpha^{-1/2}$ (2.4.4) will reduce the transit delays τ_C and τ_B by the desired factor α^{-1}. Despite the layer reduction in d_C, the intended decrease of the collector–base capacitance C_{BC} by α^{-1}, can be achieved by lateral down scaling of both emitter and collector junction area A_{jE} and A_{jC} proportional to α^{-2} (2.4.13). The TS process paves the way for this straightforward measure. Either the lengths L or widths W of the junction areas $A_j = LW$ can be readjusted. The variation of base resistance R_B in (2.4.7) and considerations of thermal resistance R_{th} with DHBT geometry determine the choice for the width.

The lateral scaling of the emitter width shortens the intrinsic current path underneath the emitter by α^{-2}, whereas the base thinning increases the sheet resistance $\rho_{B,s} \propto \alpha^{1/2}$. This results in an intrinsic base resistance $R_{B,in}$ lowered by $\alpha^{-3/2}$, but an increase in gap resistance $R_{B,gap} \propto \alpha^{1/2}$ and horizontal contact resistance $R_{B,cont} \propto \alpha^{1/4}$ (2.4.6). Next scaling generation will retain the total R_B but as the base becomes progressively thinner, surface depletion in the gap region becomes an issue. In addition, the cumulative relevance of surface recombination with down scaling has to be accounted for. For TS HBTs, the spread of the base on top of the collector does not determine the collector–base junction area. Therefore, scaling is not limited by critical downsizing of the base contacts width proportional to α^{-2}, as it is for conventional triple mesa HBTs to obey the requisite reduction in C_{BC}.

Note that if the narrow band gap InGaAs setback and InGaAs/InAlAs grade layers become a significant fraction of the total depletion layer thickness during collector thinning by α^{-1}, the critical electric field across them may be reached before doing so in the larger band gap InP layer. The DHBT benefit of increased collector breakdown voltage will be negated unless the narrow band gap layers are thinned accordingly.

Lateral and vertical scaling of $A_{jE} \propto \alpha^{-2}$ and $d_B \propto \alpha^{-1/2}$ provided, the term of the stored charge carriers in (2.4.3) require the depletion region X_{BE} thinned by $\alpha^{-1/2}$ to ensure a total emitter–base capacitance C_{jBE} proportional to α^{-1}. Meanwhile, the first term, corresponding to the depletion capacitance, adjusts more than required by $\alpha^{-3/2}$.

To keep the emitter resistance R_E constant while reducing the emitter junction area A_{jE} proportional to α^{-2}, the contact and mesa resistivities $\rho_{E,c}$ and $\rho_{E,mesa}$ must be lowered by the same factor (2.4.1). This applies also to the collector resistance R_C of the TS DHBT and is a key technological challenge. Novel surface cleaning and metallization procedures reported in [84] could provide the required improvements, beyond standard ex situ deposited lift-off contacts. Moreover, the collector of the TS DHBT could employ a Schottky contact [69].

Because intrinsic areas are shrunk by α^{-2} for the desired bandwidth improvement and operating current I_C is kept constant, the current densities j_C rise by α^2. This is feasible within the bounds of the Kirk effect as the collector d_C was thinned by α^{-1} and $j_{Kirk} \propto d_C^{-2}$ (2.4.11). However, the rigorous increase in current density translates into quadratic growth of dissipated power density $P_D/A_{jE} \propto \alpha^2$ in (2.5.1). Thermal aspects of device design are an important supplement to geometry scaling. Cooperative heating, in densely packed integrated circuits only magnifies the concern of intra- and inter-device thermal management. It is obligatory to minimize the resulting temperature rise since thermo-electric effects in section 2.5.1 are detrimental to HBT performance. Limits to bias current density imposed by reliability concerns, dissipated power density and loss in breakdown voltage with reduced collector thickness $\propto \alpha^{-1}$ could thwart scaling for higher bandwidth.

3 Transferred Substrate Technology

First, the transferred substrate (TS) approach is introduced and an overview over previous work is given. Then, the TS DHBT development of this work is presented from epitaxial growth to layout design and process technology, with a focus on the substrate transfer procedure itself.

3.1 Introduction

The majority of published InP HBTs are based on conventional emitter-up, triple mesa structures comparable to Fig. 2.3. To access the functional epitaxial layers underneath each other electrically requires a succession of separated contacts. In general, the contact width and their lateral spacing widen the footprint of the device, shaping a triangular profile. The initial (emitter) contact defines the intrinsic HBT region where current flows. The configuration of the subsequent contacts adds extrinsic capacitances and access resistances, deteriorating RF performance of the device. Most significant in conventional HBT structures is the extrinsic collector–base capacitance $C_{BC,ex}$ in (2.4.13).

Several approaches have been reported that directly address the reduction of the extrinsic collector–base capacitance $C_{BC,ex}$. For conventional processes, the lower limit of the base contact width $W_{B,cont}{}^{min}$ is around 0.4 µm. It is determined by the ohmic transfer length, the access resistance and inductance of the base metal as well as by technological aspects of alignment and yield. Minimized ohmic transfer length relies on improved base contact technology [85]. With the help of dielectric sidewall spacer [86], [87], T-shaped emitter [88] or L-shaped base metal [89], access resistance can be reduced by thicker base metallization. Selective wet etch is employed to remove the extrinsic collector–base junction. But lateral mesa undercut to form a cantilever base [90] or to isolate the base pad capacitance by a micro airbridge [91], raises reliability issues and is difficult to control over the wafer in amount and uniformity. In advance to collector growth, the subcollector has been patterned to implement a conductive layer just underneath the intrinsic region by selective implantation [92], [93], regrowth [94], [95] or buried metal [96]. Dielectric spacers [97], [98] under the

base contacts have been employed to reduce the extrinsic capacitance. And inverted collector-up structures provided lithographic access to the subcollector on top [99], [100], but at the cost of an extrinsic emitter–base junction. However, all these approaches imply technological compromises and, finally, could not outperform the emitter-up, triple mesa concept to become a standard.

The TS process of this work provides aligned lithographic access to both front- and backside of the device in order to eliminate the dominant collector–base capacitance to its intrinsic fraction. To scale down the collector junction reproducibly into submicron dimensions independent of the base width, it utilizes the proven excellence of lithographic patterning. The essential step to gain access to both sides of the epitaxial structure is the substrate transfer. Here, the wafer is mounted upside down onto a new carrier. After removing the epitaxial substrate, the collector mesa is defined lithographically from the backside, congruent to the emitter, on the opposite sides of the base. The only remaining semiconductor material of the original wafer is the functional epitaxial structure within each individual transistor, embedded in benzocyclobutene (BCB). The linear instead of triangular device profile in Fig. 2.2 distinguishes the TS DHBT from traditional ones. Potential objections may be that the substrate transfer departs from traditional DHBT's fabrication schemes, it adds additional process steps and the backside lithography relies on precise alignment to the front side, hence is scalable accordingly. On the other hand, this TS process does not only offer a fundamentally improved device design. Along with the device set-up, a construction kit for passive elements in manifold 3D configurations is provided to support functionality of the active devices. Within 3D integrated circuits [101] the vias are able to provide interconnections to operational elements on the transfer wafer and could implement a platform for heterogeneous integration [102].

In the Group of Prof. Rodwell at UCSB, eleven Ph.D. students worked from 1995–2003 at the development of InP HBTs in TS technology [103], [104], [105], [106], [107]. They achieved maximal values [108] of oscillation frequency $f_{max} = 462\,\text{GHz}$, $f_T = 139\,\text{GHz}$ at $j_C = 1.5\,\text{mA}/\mu\text{m}^2$ and $V_{CE} = 1.8\,\text{V}$ [109]. The TS DHBT featured 8 µm emitter length and a ratio of 0.5 µm emitter to 1 µm collector metal width. Emitter width undercut was 0.1 µm. The highest cutoff frequency was $f_T = 295\,\text{GHz}$, $f_{max} = 295\,\text{GHz}$, at $j_C = 1.5\,\text{mA}/\mu\text{m}^2$ and $V_{CE} = 1\,\text{V}$. The emitter mesa was $1 \times 8\,\mu\text{m}^2$ and collector mesa $2 \times 8.5\,\mu\text{m}^2$ [110].

At last, they employed a metal bonding scheme, in which the In_{60}/Pb_{40} -solder covered the complete bonding interface, serving also as common ground and heat spreader. “Although transferred substrate HBT technology has been improved since its first demonstration, low device yield still prevents the development of larger scale MMICs.” [111]. Besides general complications [112], major sources of device failure were inadequate backside alignment tolerances, excessive post bonding wafer shrinkage [113] and mesa cracks causing e.g. open emitter–base junctions [114]. Later, failure mechanisms were related to solder bonding and substrate removal. “Often the BCB cracks, because of the high temperature and pressure experienced by the wafer from the soldering bonder or pockets of air get trapped between the InP host and carrier wafer. In the areas where this occurs, device and circuit yield is zero” [115]. Bonds suffer from void formation, poor reproducibility, low thickness homogeneity [116] and mechanical stress of the composite matrix causing self-destruction of the protection layers during substrate removal [117], [118]. In addition, the TS DHBTs could only handle half of the current density of comparable triple mesa ones, because of inferior thermal characteristics [111]. In the end, these complications motivated them to quit the TS technology and continue with conventional triple mesa DHBTs.

Other Ph.D. students tried to implement TS HBT processes but faced major limitations in terms of yield, performance and heat sinking [119], [120], [121]. Further on, InAlAs/InGaAs HEMTs [122] and low power Si bipolar transistors [123], [124] were realized in TS technology to improve RF performance. In the following, the development of a TS technology for InP DHBTs is presented which essentially overcomes the reported handicaps.

3.2 Epitaxy

DHBT fabrication starts with epitaxial layer growth. The major electron transport occurs perpendicular to the layer stack. This allows critical device dimensions to be controlled by the precision of material growth rather than lithography. The impact of epitaxial design on transport properties is discussed in section 2.4. Here, the layer composition and growth techniques of the investigated heterostructures are motivated.

In principle, the layer compositions of this work are similar to conventional DHBTs, but with reduced subcollector thickness and additional etch stop layers for the substrate removal at the bottom. Initially, material was grown in-house by metalorganic vapor phase epitaxy (MOVPE) in

an AIX2400G3 planetary reactor. Common precursors such as trimethyl-indium (TMIn) $In(CH_3)_3$, triethyl-gallium (TEGa) $Ga(C_2H_5)_3$, arsine AsH_3, phosphine PH_3 and disilane Si_2H_6 were used. Lattice matched growth bases on partly pyrolysed molecules in the gas phase, which diffuse towards the heated substrate. Epilayers were characterized by in situ ellipsometry, X-ray diffraction, photoluminescence, Hall measurements and electrochemical capacitance voltage measurements (ECV). All layer systems were grown on (100) InP, Fe-doped semi-insulating, 3" substrates. Table 3.1 shows a typical TS DHBT heterostructure, grown by MOVPE at FBH.

TABLE 3.1

TS DHBT LAYER STRUCTURE #520 GROWN BY MOVPE.

Description	Material	Doping (cm^{-3})	Thickness (nm)
emitter cap	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{19}$ Si	30
n+-emitter	InP	$2 \cdot 10^{19}$ Si	60
stabilization cap	$In_{0.53}Ga_{0.47}As$	$6 \cdot 10^{17}$ Si	5
emitter	InP	$6 \cdot 10^{17}$ Si	30
p-base	$In_{0.49}Ga_{0.51}As$ – $In_{0.54}Ga_{0.46}As$	$3 \cdot 10^{19}$ C	30
setback	$In_{0.53}Ga_{0.47}As$	$\sim 10^{16} \cdot$Si	30
quaternary	$In_{0.77}Ga_{0.23}As_{0.50}P_{0.50}$	$\sim 10^{16}$ Si	20
collector	InP	$\sim 10^{15}$ Si	100
n+-collector	"	10^{19} Si	15
subcollector	$In_{0.53}Ga_{0.47}As$	10^{19} Si	30
etch stop II	InP	n.i.d.*	50
etch stop I	$In_{0.53}Ga_{0.47}As$	n.i.d.*	150

* non intentionally doped (n.i.d.)

Later, devices were grown by molecular beam epitaxy (MBE), where Knudsen furnaces generate atomic or molecular beams under ultra-high vacuum, which impinge onto the heated substrate, at rates adequate for epitaxial growth. Compared to the MOVPE grown, the InP/InGaAs/InP DHBTs show superior base doping and no hydrogen passivation. Table 3.2 lists a typical TS DHBT layer stack grown by MBE. Other layer structures processed within this work had variations in cap doping levels, emitter design and base – collector grading.

TABLE 3.2

TS DHBT LAYER STRUCTURE #724 GROWN BY MBE[1].

Description	Material	Doping (cm^{-3})	Thickness (nm)
emitter cap	$In_{0.85}Ga_{0.15}As$ – $In_{0.53}Ga_{0.47}As$	$>5\cdot10^{19}$ Si – $4\cdot10^{19}$ Si	30
n+-emitter	InP	$3\cdot10^{19}$ Si	80
emitter	"	$-5\cdot10^{17}$ Si	50
p-base	$In_{0.53}Ga_{0.47}As$	$7\cdot10^{19} - 4\cdot10^{19}$ C	30
setback	$In_{0.53}Ga_{0.47}As$	$6.5\cdot10^{16}$ Si	20
grade	$In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$	$6.5\cdot10^{16}$ Si	24
delta doping	InP	$2.75\cdot10^{18}$ Si	3
collector	"	$6.5\cdot10^{16}$ Si	73
n+-collector	"	10^{19} Si	5
subcollector	$In_{0.53}Ga_{0.47}As$	$3\cdot10^{19}$ Si	30
etch stop II	InP	n.i.d.*	50
etch stop I	$In_{0.53}Ga_{0.47}As$	n.i.d.*	150

* non intentionally doped (n.i.d.)

[1] from IQE Inc., Bethlehem, PA 18015, USA

3.2.1 Emitter

The ohmic contact resistance of heavily doped emitter cap depends on the doping level and barrier height [32]. Therefore, emitter cap and subcollector utilize low bandgap, highly doped InGaAs as contact layers. The emitter cap is the topmost layer of epitaxial growth. Therefore, defects due to lattice mismatch or high doping levels are of less concern compared to the sub-collector. For the later grown devices, the emitter cap is step-graded from $In_{0.53}Ga_{0.47}As$ to more narrow bandgap $In_{0.85}Ga_{0.15}As$. The maximum doping level of n-type $In_xGa_{1-x}As$ increases additionally with the In mole concentration [125].

The InP emitter is partitioned in a high doped region to support high current density without substantial potential drop, while adjacent to the base a low doped region maintains depletion width to ensure an adequate depletion capacitance. The thickness and doping of each partition must be carefully designed. An improper trade-off can lead to rapid increases in emitter resistance or poor high frequency performance due to high emitter junction capacitance, respectively. An abrupt InP/InGaAs emitter–base junction was adopted for its simplicity.

3.2.2 Base

From a designer point of view, the base of a high-speed DHBT ought to be thin ($\leq 40\,\mathrm{nm}$) for decreased base transit time and increased gain, while at the same time the base resistance must be kept to a minimum. Base doping was maximized to reduce base sheet and contact resistance. First, doping levels of $2\cdot10^{19}\,\mathrm{cm}^{-3}$ were realized in the MOVPE, while later values of up to $7\cdot10^{19}\,\mathrm{cm}^{-3}$ were employed in the MBE. Carbon doping of the p-InGaAs base is chosen over beryllium or zinc. It offers a lower diffusion coefficient [126], higher activated doping levels [127] and is a weak n-type dopant in InP [128]. The latter enables an abrupt p-n junction, which coincides with the crystallographic heterojunction, even at very high base doping levels [38].

The base is graded to reduce the transit time in (2.4.5). Either a bandgap or doping grade is utilized to introduce a potential drop of $\sim 50\,\mathrm{meV}$ to accelerate electron transport. The MOVPE grown heterostructures employ a compositionally graded base. The Indium fraction changes from 49% at the emitter to 54% at the collector interface. Whereas the MBE grown structures feature dopant grading, with heavy doping ($7\cdot10^{19}\,\mathrm{cm}^{-3}$) at the emitter and lower doping ($4\cdot10^{19}\,\mathrm{cm}^{-3}$) at the collector interface.

Hydrogen passivation can be a severe problem with carbon doping of InGaAs. If hydrogen is incorporated into the InGaAs base during growth or subsequent processing, it binds to the carbon dopants, reducing the effective doping level. In addition, scattering at the passivated carbon atoms reduces the electron mobility. Lower gain, due to lower base mobility, as well as higher base resistance, due to lower effective doping level are the consequences. For carbon doped InGaAs grown by MOVPE, out diffusion of hydrogen through annealing is paramount due to the hydrogen containing precursors [129]. In situ annealing under nitrogen has been performed at 525 °C and 575 °C subsequent to the growth of the base and 5 nm InGaAs cap layer, respectively. The thin InGaAs layer was implemented to stabilize the InP emitter surface during the annealing. A C-doped GaAsSb base grown by MOVPE does not exhibit any hydrogen passivation problem when used under proper in situ annealing conditions [130]. For MBE grown material, the precursors do not contain hydrogen. However, hydrogen incorporation can still occur during processing steps such as PECVD or RIE.

3.2.3 Collector

The conduction band discontinuity of type-I InP/InGaAs/InP DHBTs is removed by grading the energy gap between base and collector in order to prevent current blocking. Two different grading schemes were investigated. The first method utilizes a 20 nm quaternary $In_{0.77}Ga_{0.23}As_{0.50}P_{0.50}$ layer as intermediate bandgap material (1 eV), combined with a 30 nm $In_{0.53}Ga_{0.47}As$ setback to prevent an impeding barrier in the transition region [131]. The second grading method employs a MBE grown, 20 nm $In_{0.53}Ga_{0.47}As$ setback followed by a chirped superlattice of $In_{0.53}Ga_{0.47}As / In_{0.52}Al_{0.48}As$ of 24 nm total thickness and 1.5 nm period. Since a continuous compositional grading is difficult to grow, the short period superlattice of alternating materials with varying layer thickness ratio is chosen [54]. The grade is terminated by a delta doped n-InP(Si) layer, which generates a field that neutralizes the quasi-field associated with the grade. The collector regions are designed to be fully depleted at zero bias. Doping levels of the subcollector were lowered compared to the emitter cap, to reduce defects within subsequent grown epitaxial layers. Indium-rich, narrow band gap contacts were not introduced, because of their lattice mismatch. A several hundred nanometer thick subcollector as for conventional DHBTs is not required.

3.3 Mask Set Layout

The mask set layout defines all lateral dimensions. The succession of lithographic patterning, in conjunction with subsequent processing, shapes the three-dimensional device structure. The mask design incorporates the expertise of process margins, aberrations and tolerances. It is adapted according to first hand experiences and experimental variations. This section gives an overview over the layout components. Additional layout details of the DHBTs as well as of passive elements and MMICs are given in section 3.4, section 5.1 and 5.2, respectively.

Within this work, 4 lots of 6 epitaxial wafers each were processed. The individual sets of $8-18$ masks were designed and fabricated in-house. The layout of the last process run is shown exemplarily in Fig. 3.1. The arrangement is divided into 4 main sectors: single DHBTs, MMICs, passive elements and process control monitoring topologies (PCM). The layout size of $9 \times 9.6\,\mathrm{mm}^2$ yields 48 stepper shots on a 3" wafer. The 196 single TS DHBTs per shot are defined by ~ 50 geometric parameters. They are divided into three scaling families in respect to process margins (ambitious, medium, relaxed). Besides a set of fixed baseline transistors, 20 parameters were varied in a programmable layout scheme within each family in order to identify critical dimension in terms of performance and yield. The majority are single finger DHBTs – emitter metal width varies between $0.7-2\,\mu\mathrm{m}$, contact lengths are between $4-20\,\mu\mathrm{m}$. The TS MMICs comprise 12 modifications of oscillators and 6 of traveling-wave amplifiers. The passive elements consist of micro strips, crossings and T-junction, as well as capacitors, resistors, multi-layer transformers, filter and RF calibration structures (open/short/through/load). The PCM section features alignment, edge shift, resolution, etch profile and RIE interferometric monitoring structures. Sheet resistance (metal, semiconductor), contact resistance (metal/semiconductor, metal/metal), interconnection topologies as well as large diodes and DHBTs were electrically characterized to monitor the process.

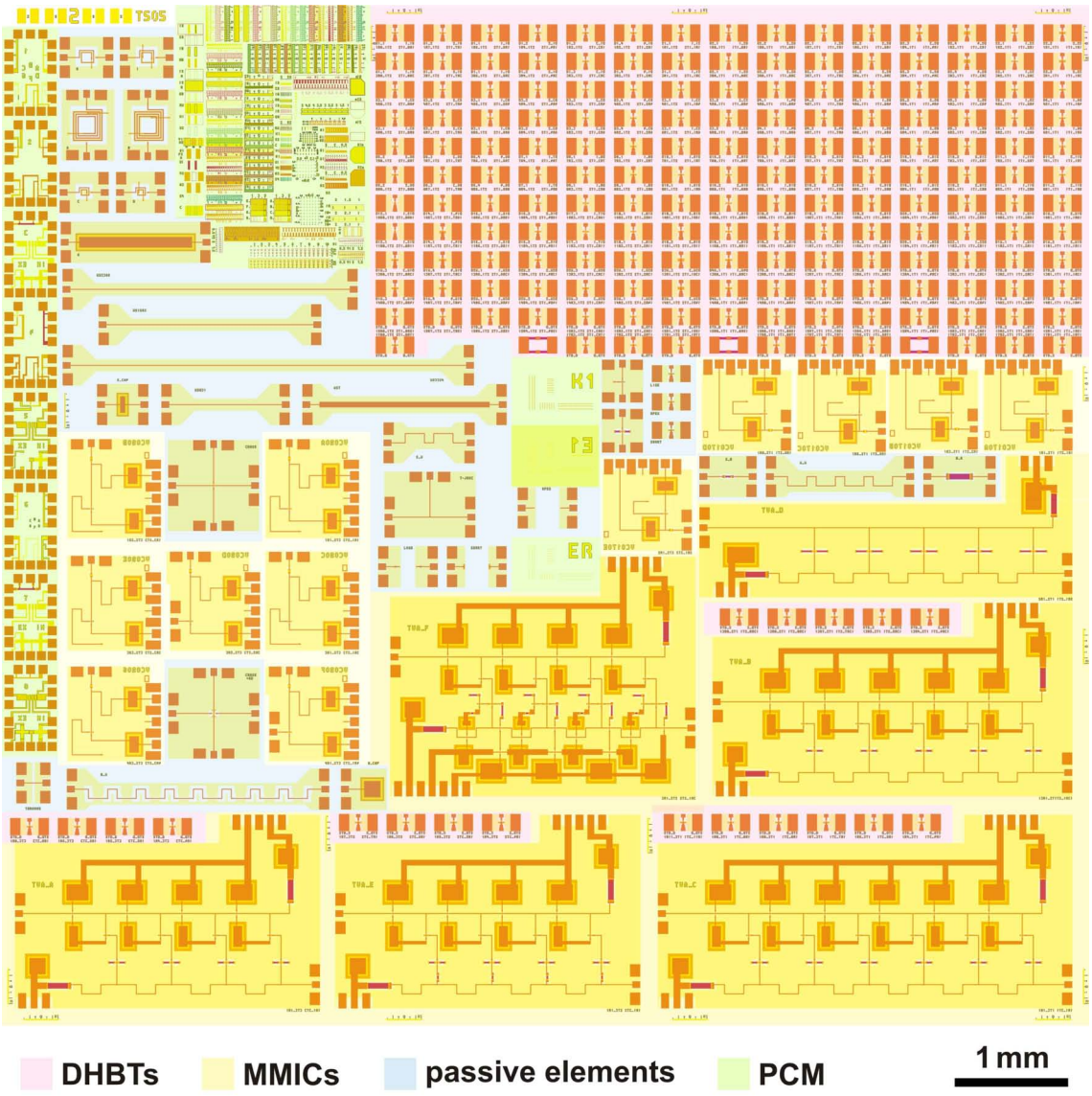

Fig. 3.1 TS mask set layout.

3.4 Process Flow

Processing defines the lateral dimension of the epitaxial layer stack via the mask set layout, shaping the three-dimensional device structure. The conception and implementation was an integral part of this work. The individual process steps were standardized to be carried out by technicians. The detailed process manual is given in the appendix A.

3.4.1 Emitter

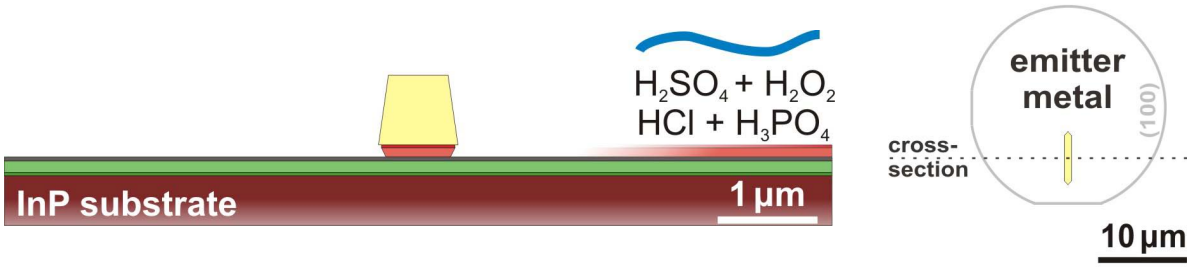

Fig. 3.2 Schematic cross-section as well as top-view of the emitter metallization and mesa etch. The dot line indicates the cutting plane of the cross-section. The wafer contour defines the crystallographic orientation of the emitter metal.

Processing begins similar to conventional DHBTs. Lithography for metallization utilizes image reversal photoresist in conjunction with lift-off technique. Non-alloyed ohmics are utilized to contact the emitter, base and collector. The narrowest lateral device feature is the emitter metal width. It varies between $0.7-2\,\mu m$. Contact lengths are between $4-20\,\mu m$. Alignment marks, deposited with the emitter metal on the 3" wafer, guide all successive process steps.

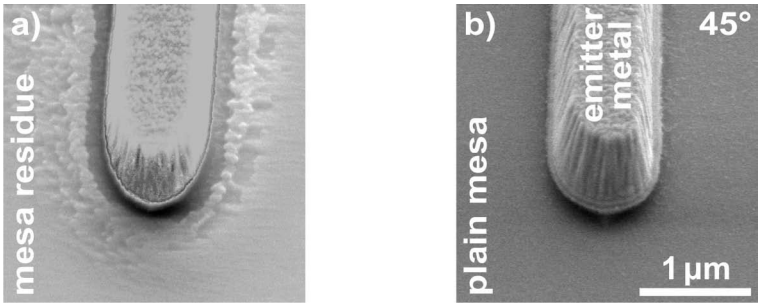

Fig. 3.3 DHBT emitter mesa etched in a) standard b) low lit environment.

During the timed wet etch down to the base, the emitter metal in Fig. 3.2 serves as a mask for the emitter mesa. The greenish InGaAs cap layer is removed by $H_2SO_4(96\%) : H_2O_2(30\%) : H_2O = 1:8:500$ and the reddish InP emitter by $HCl(37\%) : H_3PO_4(85\%) = 1:10$, monitored by visual inspection [132], [133]. Dimmed light during emitter mesa etch ensures minimized over-etch times without mesa residuals around the emitter metallization, see Fig. 3.3 a, b). Due to the very thin base layer of 30 nm, excellent etch selectivity between the InP emitter and InGaAs base is required.

Despite high selectivity in vertical direction, wet etching must carefully be controlled, because of lateral undercut along the contact metals as well as at their ends. On the one hand, the mesa undercut enables self-aligned base metallization defined by the emitter contact edges. On the other hand, excessive undercut increases the base gap resistance of (2.4.6) and may compromise yield. In particular, the profile and etch rate dependence on the crystal orientation of InP shapes an anisotropic mesa [134]. To reduce the mesa undercut, emitters are orientated perpendicular to the major flat along the [011] crystal direction of the (100) wafer plane. Hexagonal emitter contacts eliminate the protruding mesa profile at the ends of multi-micron emitters [135]. This prevents short-circuits during the self-aligned base metallization. Unlike the <011> directions perpendicular and parallel to the emitter metal, the lateral etching rate of the <001> directions 45° to the emitters are not inhibited during vertical mesa wet etch of (100) InP wafer planes. For deep submicron emitters the uninhibited 45° lateral undercut at the end of the emitter fingers can become critical, suggesting an at least partly dry etch approach.

3.4.2 Base

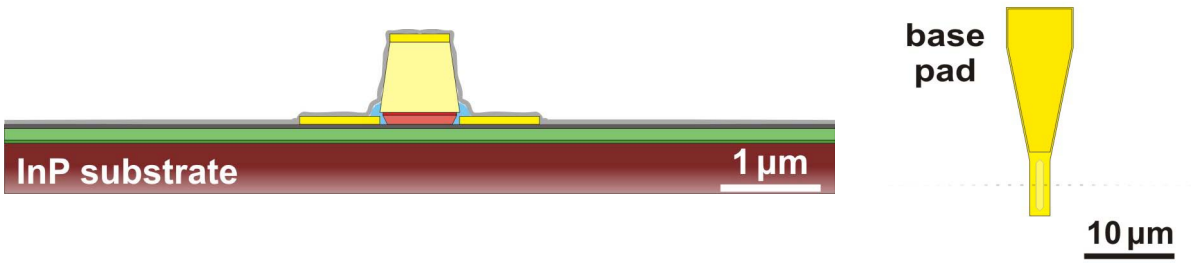

Fig. 3.4 Cross-section and top-view of base metallization with passivation.

Self-aligned base contacts in Fig. 3.4 minimize the lateral distance to the active device area. Their spacing is defined by the wet etch undercut of the emitter mesa. According to the emitter mesa height, the base metal thickness is adjusted to avoid emitter–base short-circuits. On the other hand, a too thin base metallization, especially for long emitter fingers, undermines RF performance. The self-aligned base contacts extend 0.5–0.8 µm on each side of the emitter metal. Their width is determined by technological aspects as alignment and yield, access resistance and

inductance of the base metal and the ohmic transfer length. The surface of the emitter–base junction is passivated by BCB. The base pad provides the foundation which is contacted by an electroplated via during the backside process. A second metal on top of the pad reinforces mechanical strength and decreases its electrical resistance. For the TS process, the spread of the base metal is uncritical. It is not traded off against an extrinsic collector–base capacitance $C_{BC,ex}$+ $C_{BC,pad}$ underneath. Therefore, aggressive down scaling of base contacts and pads, micro airbridges [91] or wrapped base metallization [136] to minimize parasitic capacitances are not required.

3.4.3 Planarization

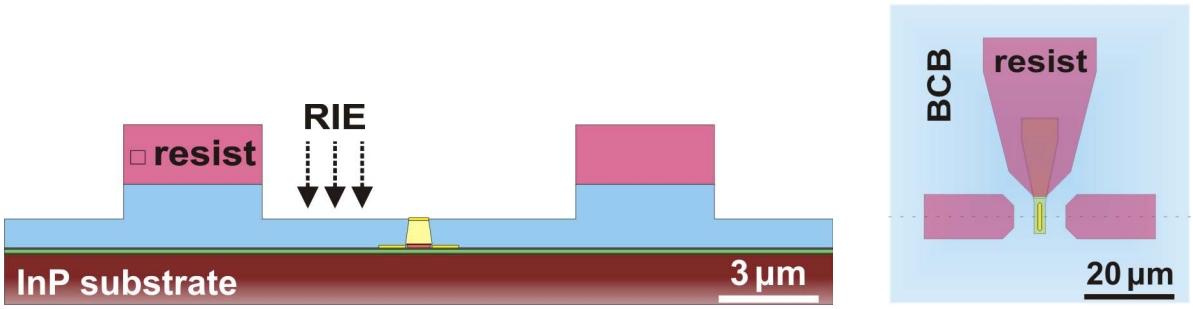

Fig. 3.5 Cross-section and top-view of BCB planarization and RIE etchback.

Planarization of the device in Fig. 3.5 is done by BCB accompanied by reactive ion etch (SF_6/O_2) to uncover the emitter contacts. An in situ etch-back control by laser interferometry guarantees process margins of ±25 nm over the 3" wafer, demonstrated in Fig. 3.6. A SiN_x tie layer improves the BCB adhesion on metal, semiconductor, and aluminum nitride (AlN) significantly.

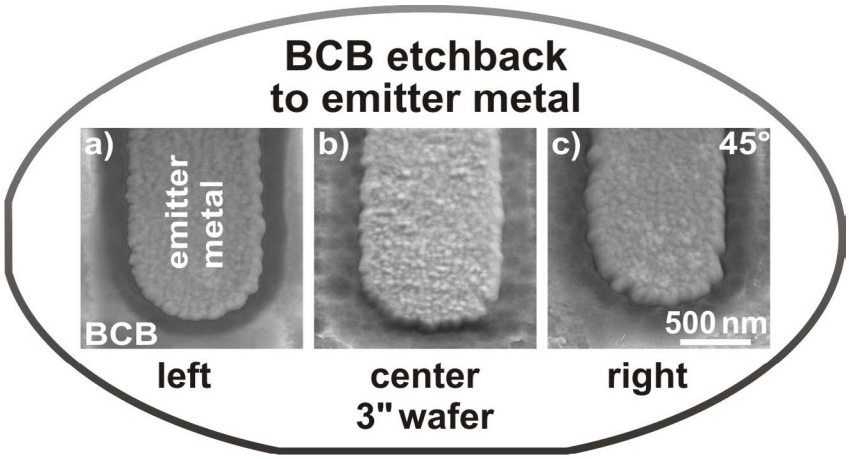

Fig. 3.6 **Homogenous BCB etchback to uncover the emitter metal, process margins are within ±25 nm over the 3" wafer.**

3.4.4 Ground & Interconnects

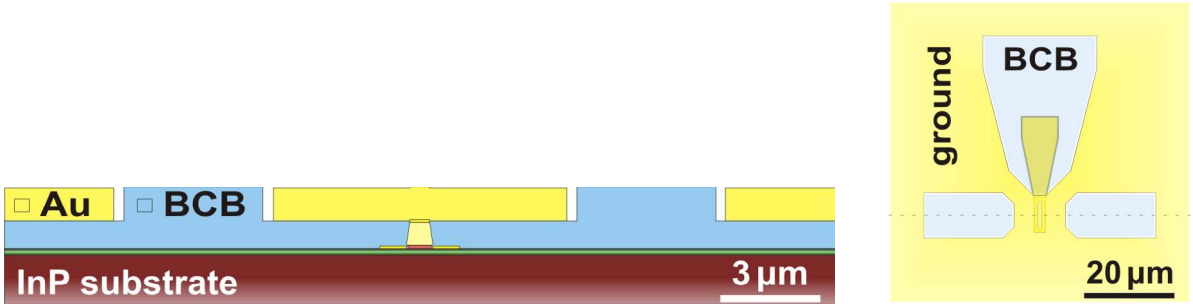

Fig. 3.7 **Cross-section and top-view of planarized ground metallization.**

The etchback scheme allows a massive emitter connection, independent of lateral alignment tolerances and compatible to device scaling. The patterned ground metallization in Fig. 3.7, also serving as heat spreader, completes the front side process. Notches in the ground anticipate thermal vias and interconnects to the transfer substrate or reduce e.g. the base pad capacitance. At the end of the TS process, the ground is situated between the transfer substrate and active device.

3.4.5 Wafer Bonding & Substrate Removal

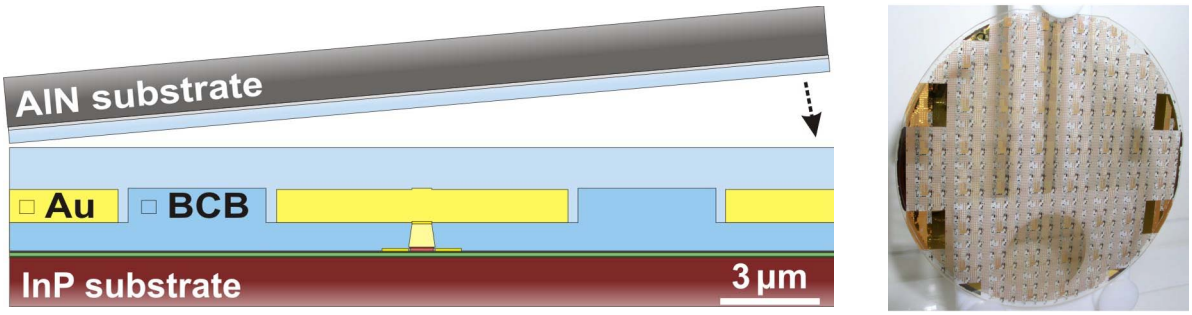

Fig. 3.8 Schematic cross-section of bond interfaces and photo of demonstrator with TS DHBTs after substrate removal on a 3" glass wafer, to evaluate wafer bonding alignment.

The wafer bonding in Fig. 3.8 marks the departure from conventional DHBT fabrication. To gain access to both sides of the epitaxial structure, wafer bonding is an essential step of the TS process and is further characterized in section 3.5. The semiprocessed DHBTs on the 3" InP substrate are bonded simultaneously upside down onto an AlN wafer via a 2 µm layer of BCB. The initial alignment marks are simultaneously transferred onto the new substrate. They are the lithographic reference for the front- as well as backside process. The post bonding alignment tolerance between the InP wafer and transfer substrate is below 20 µm. It does not limit the TS process. As a matter of convenience, the offset should be less than one hundred microns – the automatic search range of the stepper –. If required e.g. for 3D integrated circuits, alignment accuracy of BCB wafer bonds can be down to 2 µm [137] and the AlN substrate can finally be thinned to 30µm, for mechanically flexible electronics.

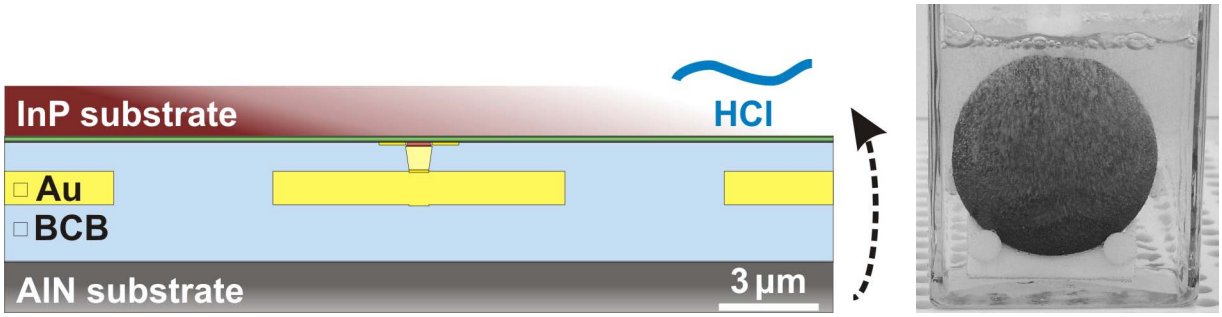

Fig. 3.9 Schematic cross-section and photo of InP substrate removal in hydrochloric acid.

To uncover the backside of the epitaxial layers in Fig. 3.9, the InP substrate is removed at a rate of 25 µm/min in concentrated hydrochloric acid (HCl) at 40 °C down to the 150 nm thick InGaAs etchstop. InP produces ascending bubbles of phosphine (PH_3) in hydrochloric acid. To counteract etch irregularities due to the resulting drift, the upright wafer is rotated in plane. Caution, before its decomposition in ambient air, phosphine is very toxic! Proper exhaustion is monitored by PH_3 sensors. At the beginning of the etchback, ridges occasionally develop from initial surface contaminations unintentionally masking the backside of the InP wafer. They should be removed at appearance e.g. by a scalpel, since their (111) planes will scarcely etch. The exposed epitaxial layer does not show cracks due to mechanical stress of the composite bond matrix. Even minimal failures would result in a well detectable wet etch attack of the underlying epitaxial layers by the concentrated HCl.

3.4.6 Collector

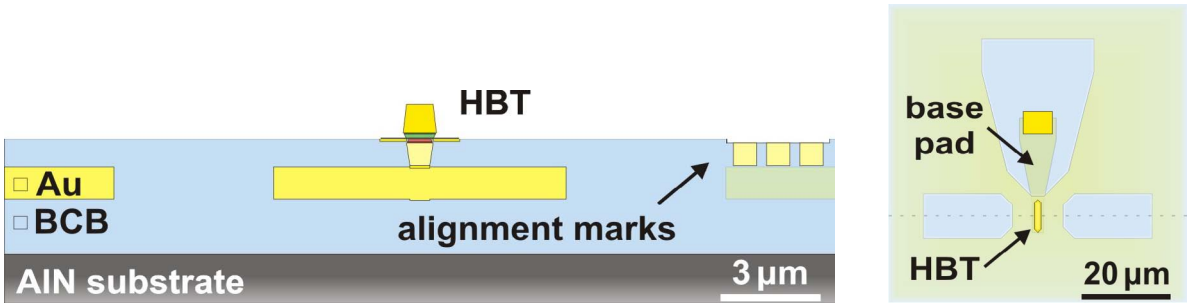

Fig. 3.10 Cross-section and top-view of the collector lithography, congruent alignment to the emitter metal.

After removing the epitaxial substrate, the collector in Fig. 3.10 is defined from the backside, congruent to the emitter, on the opposite sides of the base by stepper lithography [138]. The collector metal can be independently scaled according to the electrical or thermal requirements. With lithographic access to front- and backside of the epitaxial structure, equal design rules apply for emitter and collector contact. Thus, processing sequences are similar. Semiconductor material, which is not essential for the DHBTs e.g. the extrinsic collector underneath the base contacts, is removed to reduce parasitics. The only remaining material of the original wafer is the functional epitaxial structure within each transistor of Fig. 3.11. The resulting linear instead of triangular

device profile distinguishes the TS DHBT from traditional ones. Initially, the mechanical stability of the freestanding base mesa, embedded in BCB and the alignment accuracy of the backside process were questioned to be potential show-stoppers for the TS process. However, neither yield is dominated by mechanical base cut off, nor is the back-to-front side alignment insufficient. After substrate removal and also during gradual backside mesa formation, remaining epitaxial layers demonstrate homogenous appearance without signs of layer breaking and anticipate wet etching [139]. Only the masks of the backside lithography are adapted to the expansion during wafer bonding by a factor of 163 ± 3 ppm, constant over all TS runs [140]. Then the collector to emitter alignment accuracy of better than 100 nm over the 3" wafer is even within the stepper specifications of a conventional process.

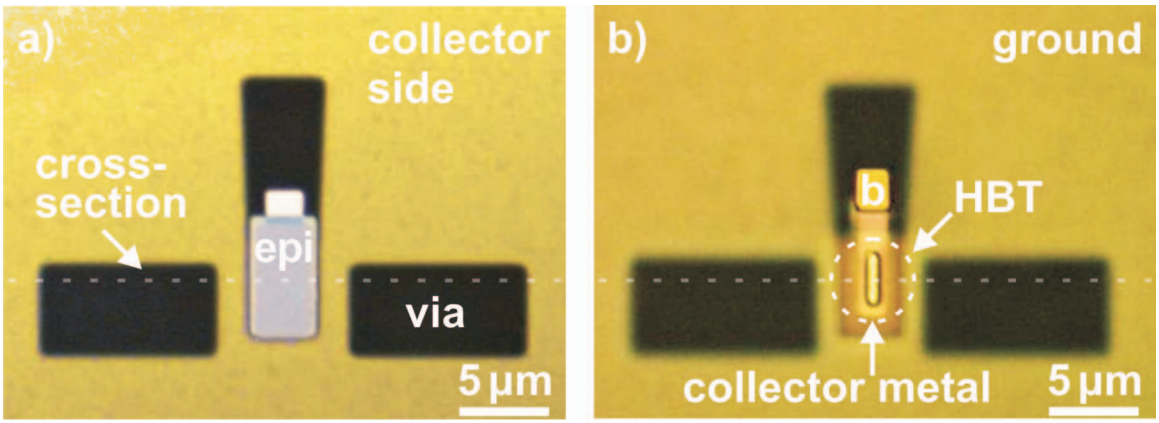

Fig. 3.11 Top-view during collector side processing, both with ground metal underneath a) backside of flipped epitaxy b) after collector metallization and mesa etch.

3.4.7 Periphery

Despite the non-planar nature of DHBTs, the TS process is designed to maintain low topology during transistor lithography. The centered base layer is the reference plane for the subsequent process steps of the three-dimensional device configuration. For the periphery, BCB planarization levels out the topologies. After the DHBTs are completed and encapsulated, the planar process scheme is left behind. In a single step, via holes open up access to the different layers of device terminals and the transfer substrate in Fig. 3.12. The required topology and resolution is achieved by an aluminum hard mask. Afterwards, the Al is removed by a dip of KOH (50%) : H_2O = 1 : 10.

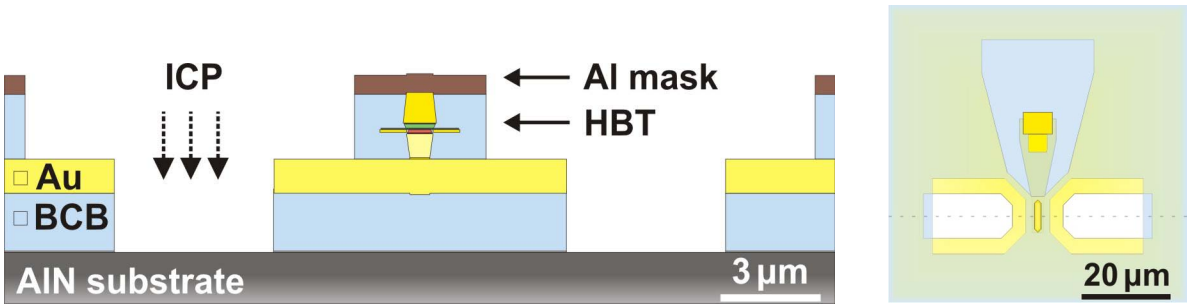

Fig. 3.12 Cross-section and top-view of via hole formation to contact the device terminals and transfer substrate.

To avoid step coverage issues of evaporated metal, electroplating is employed for any vertical interconnection of the TS process. The electroplated metallization in Fig. 3.13 provides 1.2 µm minimum feature size while covering 6 µm topology to process interconnections and vias to the AlN substrate simultaneously. It is crucial not to employ hydrofluoric acid during the backside process, since it diffuses and attacks the BCB bond interfaces. Therefore, the adhesion layer of the plating base consists of TiW, dissolvable in H_2O_2 at 40 °C, instead of Ti.

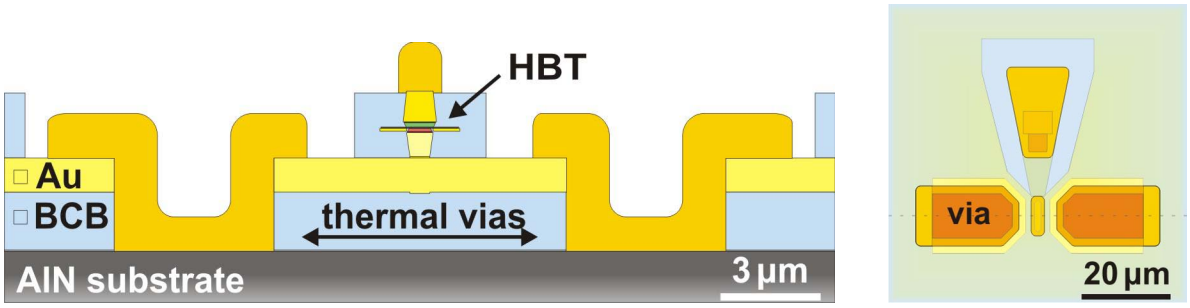

Fig. 3.13 Cross-section and top-view of the electroplated interconnects and vias.

Thermal vias to the AlN substrate and interconnects to the device terminals are processed together. Single DHBTs are now ready for measurement. Fig. 3.14 shows a focused ion beam (FIB) cross-section of a TS DHBT. At present, no wafer bonding alignment is required for the thermal vias or NiCr resistors on the AlN substrate, since they are fabricated exclusively after wafer bonding within the backside process.

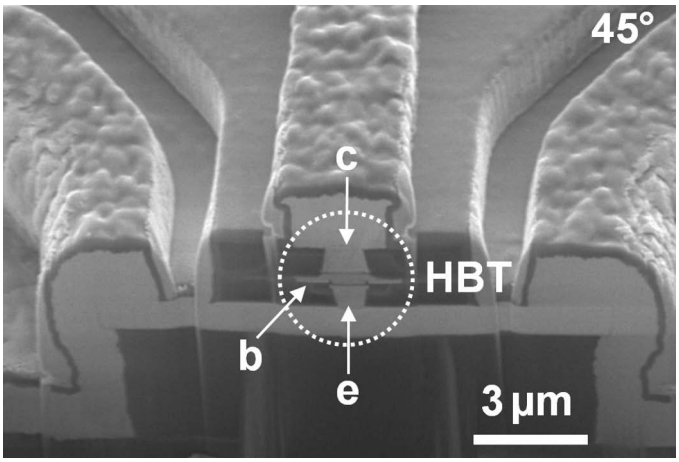

Fig. 3.14 Focused ion beam cross-section of a transferred substrate DHBT in process. The cutting plane corresponds to the previous sketches of cross-sections.

Increasing the microstrip width w, lowers the line attenuation α. Simultaneously, the distance to ground d is extended to maintain constant impedance. The dependence of the width $w_{(d)}$ and attenuation $\alpha_{(d)}$ on the ground distance d is simulated in Fig. 3.15 for a 50 Ω-environment. A reasonable trade-off between periphery set-up and line attenuation is a 14 µm wide microstrip in Fig. 3.16, raised by an additional BCB layer to a distance of 5.25 µm from ground. The ground underneath the DHBTs electrically decouples the whole configuration from the substrate. The 4 µm thick galvanization is the main interconnection layer also serving as heat spreader for the transistors.

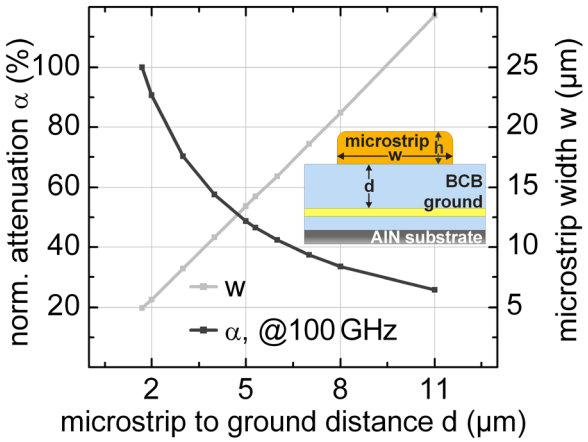

Fig. 3.15 Dependence of width w and attenuation α (at 100 GHz) on the ground distance d for a 50 Ω microstrip of height h = 4 µm. Inset: Microstrip configuration.

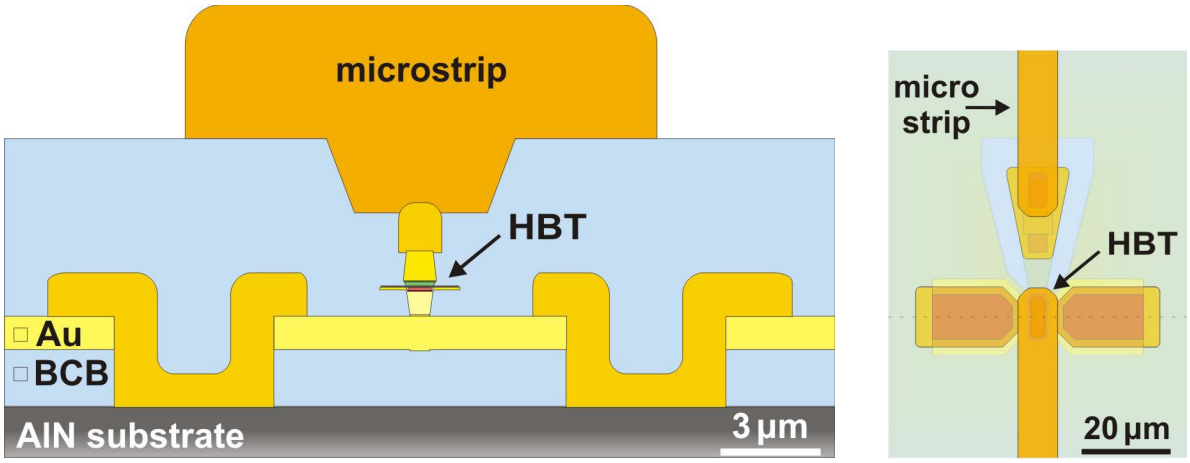

Fig. 3.16 Cross-section and top-view with final interconnection layer forming the microstrip.

Thin film microstrip lines, NiCr resistors (15 Ω/sq) on the AlN substrate and SiN_x capacitors (0.23 F/µm^2), illustrated in Fig. 3.17, complete the MMIC process. The airbridge-free, multi-level metallization scheme of the TS process almost comes along with the device set-up. It offers three major wiring layers, separated by BCB, as well as cross-connections to each other and to the transfer substrate. Within 3D integrated circuits vias can also provide wiring to operational elements on the transfer wafer. Thus, a construction kit for passive elements in manifold 3D configurations is available to support functionality of the active devices.

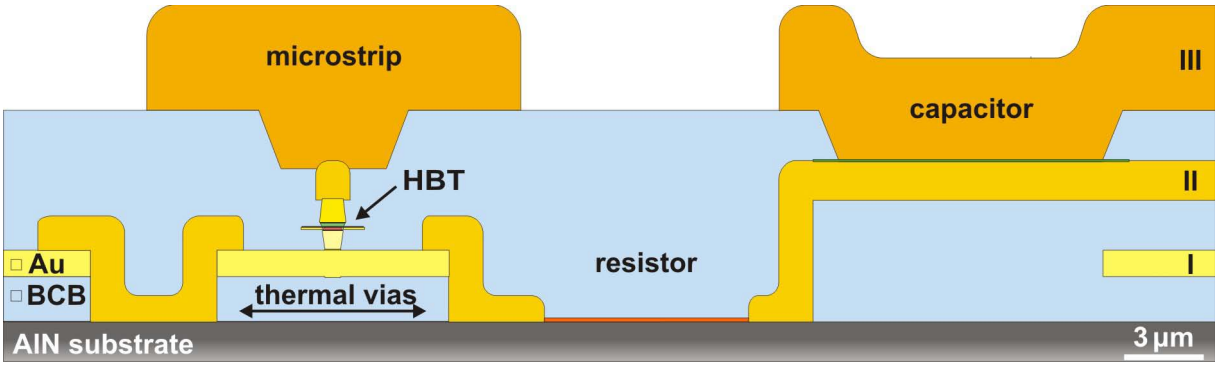

Fig. 3.17 Schematic cross-section of the TS technology platform ready for MMIC processing, consisting of TS DHBT, microstrip, NiCr resistor, MIM capacitor and three major wiring layers.

3.5 Wafer Bonding

Wafer bonding refers to the process of joining two wafer size substrates. It adds significant flexibility to the micro-fabrication tool set of wafer-level parallel processing and is a key component of the TS technology. Several techniques are employed for wafer bonding. Their demands on surface preparation, bonding pressure and temperature can be reduced significantly with the assistance of polymer, glass or metal interlayers, while maintaining the required bond strength. Optional bonding methods are summarized below:

3.5.1 Types of Bonding

a. Fusion

Wafer fusion, also referred to as direct wafer bonding, involves no bonding intermediate [141], [142]. Instead, the bonding surfaces have to be extremely flat and clean. They are activated either chemically [143] or by plasma treatment [144]. To obtain strong bonds, high temperature annealing 600 – 1200 °C is employed. Room temperature bonding schemes with special surface treatments have also been reported [145]. Wafer fusion is commercially used for silicon on insulator (SOI) production [146].

b. Anodic

Anodic or field assisted bonding requires an electron conducting material e.g. silicon and a material with ion conductivity e.g. alkali-containing glass [147]. The wafer pair is heated to 180 – 500 °C, while a voltage of 200 – 1500 V is applied to mobilize the ions [148]. Surface roughness less than a few nanometers is required. The voltage creates a large electric field that pulls the wafer surfaces into intimate contact and fuses them together. Anodic bonding usually leads to strong and hermetic bonds and is widely used for microsensor fabrication [149]. However, it involves high electric fields and mobile alkali ions, imposing a threat to high performance electronics.

c. Polymer

Polymer or adhesive bonding utilizes an intermediate polymer layer to wet the bonding surfaces and glue various substrates together. A comprehensive review of adhesive wafer bonding is given in [150]. Moderate bonding parameters make adhesive wafer bonding compatible with III-V processing – neither excessive heat or pressure nor electric fields or mobile ions are required to obtain strong bonds. Sophisticated surface treatments are not required. The interlayer can even compensate structures and particles of several microns due to the good planarization and wetting properties of most adhesives. The polymer interlayer makes wafer bonding more independent of specific substrate properties and the elastic properties of polymers are able to reduce stress in the bonds [151]. Due to moderate bonding temperatures, a wide range of different materials can be joined. The multitude of available polymer materials compatible with standard clean room processing and the ability to tailor their properties make this approach very versatile for specific demands. Furthermore, it is simple, robust and low cost. This set of capabilities makes polymer wafer bonding the procedure of choice for this work, even though the poor electrical and thermal conductivity of polymers requires additional measures for electrical and thermal vias to the transfer substrate.

d. Glass

Glass frit bonding uses an inorganic, "low" temperature melting glass as intermediate bonding layer [152]. The glass paste with organic binders is deposited by e.g. screen-printing, spraying or spin coating [153]. After the wafers are brought into intimate contact and heated to 400 – 1100 °C, the glass reflows and creates hermetic bonds. Although glass frit has got a couple of pros in common with polymer bonding, the required temperatures are critical to incorporate in III-V processing.

e. Metal

Similar to polymer and glass, metals can be the base of wafer bonds. In solder bonding, metals or metal-alloys are deposited usually on both wafers [154]. The bonding surfaces are brought into contact and heated to the melting temperature of the solder. The solder reflows, conforms over non-planar features and realizes strong bonds.

Eutectic bonding is a variation of solder bonding, in which the reduced melting temperatures of alloys are utilized to join dissimilar materials. When the respective materials are brought into contact at temperatures beyond their eutectic point, rapid interdiffusion occurs. An eutectic alloy forms spontaneously, with the melting point much lower than that of the individual materials and lower than any other of their compositions. Common hard solders are Au-Sn (217 – 420 °C) [155], Au-Ge (360 °C) [156], Au-Si (363 °C) [157].

Thermo-compression bonding joins metal surfaces under high pressure (~ 300 MPa) at elevated temperatures (300 – 500 °C) to achieve plastic deformation of the intermediate metals below their melting point. Instead of heat, ultrasonic energy is also applied [158]. Common material combinations are Au to Au [159], Cu to Cu [160].

Metal bonding can join various wafer materials at fairly low temperatures by hermetic bonds. It is used extensively for e.g. flip chip or wire bonding, but it is difficult to obtain complete bonding over large areas due to native oxides, which prevent bonding at the metal interfaces. Besides the mechanical bond, metal-based approaches can also provide electrical connections and heat sinking. A laterally structured and aligned metal/polymer bonding scheme could provide independent, vertical interconnects underneath the transferred devices to implement high density 3D integrated circuits with directly integrated heat sinking [161].

3.5.2 Bonding Materials

The main advantages of polymer wafer bonding are insensitivity to surface topology, modest bonding temperature and pressure to form routinely strong bonds as well as compatibility into III-V processing. Various polymeric glues, such as divinylsiloxane bisbenzocyclobutene (BCB) [162], [163], [164], epoxy [165], [166], photoresist [167], polymethylmethacrylate (PMMA) [168], polyimide [169], parylene [170], fluoropolymer [171], fluorinated poly-arylene-ether [172], polydimethylsiloxane (PDMS) [173], methylsilsesquioxane (MSSQ) [174], liquid crystal polymer (LCP) [175] and wax [176] have been proposed for wafer bonding.

However, BCB was identified to match best the requirements of this work. BCB is a thermosetting polymer that undergoes cross-linking during the curing process to form a stable polymeric network [177]. The required thermal budget below 250 °C is compatible with the transistor processing. BCB flows for a short time during the cure, but does not remelt below its glass

transition temperature $T_g > 350\,°C$ afterwards. It is chemical resistant to acids, bases or solvents of subsequent process steps and can be selectivity patterned by RIE. Proper adhesion between the intermediate adhesive and bonding interfaces as well as good cohesion within the polymer to prevent interfacial delamination and cohesion failure is achieved [178]. Bonds are not deteriorated by shrinkage or volatile by-products e.g. trapped in voids while hardening the polymer after the wafers are joined [162]. BCB is not only a suitable bonding agent but also an excellent inter-layer dielectric. Table 3.3 summarizes characteristic properties.

TABLE 3.3

CHARACTERISTIC PROPERTIES OF BCB, CYCLOTENE™ 3022 SERIES FROM DOW CHEMICALS [179].

dielectric constant ε_r :	2.5 @ 20 GHz	degree of planarization :	>90 %, [180]
dissipation factor $tan\delta$:	0.002 @ 20 GHz	spin-on thickness :	0.1 – 26 µm
breakdown voltage V_{br} :	$5.3 \cdot 10^6\,Vcm^{-1}$	spin-on solvent :	mesitylene
volume resistivity ρ :	$10^{19}\,\Omega cm$	shrinkage during cure :	<5 %
curing temp. range :	200 – 300 °C	tensile modulus :	2.9 ± 0.2 GPa
glass transition temp. T_g :	>350 °C	tensile strength :	87 ± 7 MPa
thermal conductivity κ :	$0.29\,Wm^{-1}K^{-1}$ @ RT	tensile elongation :	8 ± 2.5 %
thermal expansion :	$42\,ppmK^{-1}$ @ RT	poisson's ratio :	0.34

The bond between two substrates is established at elevated temperatures while curing the BCB at 250 °C. When the wafer stack cools down to room temperature, dissimilar thermal expansion of the substrates induces strain. Sintered AlN [1] is chosen as transfer substrate because of its thermal expansion of $4.6\,ppmK^{-1}$, closely matched to InP, high thermal conductivity $>170\,Wm^{-1}K^{-1}$, good high frequency properties and low cost [72]. Transparent borosilicate wafers [2] with a thermal expansion of $4.5\,ppmK^{-1}$ and thermal conductivity of $0.93\,Wm^{-1}K^{-1}$ are employed to inspect homogeneity and alignment of the wafer bonding.

[1] from Toshiba (TAN 170), 3" wafer made by P/M Industries, 14320 NW Science Park Drive, Portland OR 97229, USA

[2] from Schott (AF 45), 3" wafer manufactured by Plan Optik, 56479 Elsoff, Germany

3.5.3 Bonding Procedure

Wafer bonding consists of three major steps: preparation of adhesion layers, wafer to wafer alignment and bonding along with BCB cure. Directly before the InP and AlN substrates are spin-coated with BCB [1], a SiN_x tie layer is deposited in the PECVD and AP 3000 [2] is applied to improve adhesion. The BCB, dissolved in mesitylene, planarizes remaining topology and produces a very planar and homogenous coating. Backside rinse and edge bead removal are advisable. A subsequent bake drives out solvents and volatiles from the intermediate polymer to prevent them from getting trapped and deteriorating the bond interface.

The wafers are aligned to each other in a commercial EVG-420 SmartView™ system sketched in Fig. 3.18 [181]. The method registers marks of the top and bottom wafer on a precision stage, moves them into alignment and clamps the wafer stack separated in a fixture.

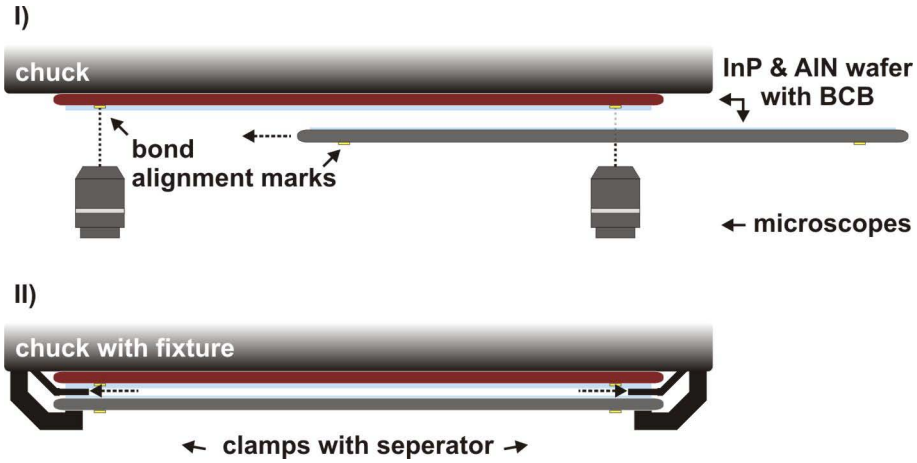

Fig. 3.18 I) Alignment of wafers before bonding by the SmartView™ method. II) Aligned wafers are separated and clamped in the transfer fixture.

Pre-bonding alignment is in the range of 1 µm. Reported post-bond alignment accuracy can be down to 2 µm [137]. But if the 35% crosslinked BCB is not pre-cured to achieve better planarization and stronger bonds, it is getting soft during curing. Then, unavoidable shear forces between

[1] from Dow Chemicals (Cyclotene 3022-35 series resin)
[2] adhesion promoter for Cyclotene from Dow Chemicals

the bond chucks result in post-bond tolerances in the range of 20 µm. However, the TS process requires only an offset less than 100 µm, as a matter of convenience, to be within the automatic stepper search range for the backside process.

Bonding is done in a commercial EVG-501 wafer bonder. Bonding pressure, temperature, chamber vacuum and their chronology are significant parameters to achieve homogenous bonds over the whole wafer. Table 3.4 lists the parameter sequence of the bonding recipe.

TABLE 3.4

PARAMETER SEQUENCE OF WAFER BONDING PROCEDURE.

N_2 purge & pump
pump vacuum $5 \cdot 10^{-6}$ bar
contact pressure 550 N
N_2 purge to 0.5 bar
heat up to 200 °C @ 10 °C/min
heat up to 240 °C @ 5 °C/min
wait 120 min
cool down to 140 °C @ 10 °C/min
contact pressure off
vent

The bond chamber is loaded with the aligned wafer stack, purged with N_2 and evacuated to 10^{-6} bar in order to prevent voids of air being trapped between the wafers during bonding as well as oxidation of BCB while curing. The 3" wafer pair is forced into intimate contact at uniaxial pressure of 550 N to promote the deformation and adaptation of the BCB. Higher bonding pressures increase the conceivable deformation of the BCB and the wafers. However, increased pressures cause higher stress and the InP wafer may crack. Non-uniformities in bonding pressure may result in thickness variation of the intermediate polymer. A graphite plate padding between the stiff bond chucks helps to distribute the pressure more evenly. Then the wafer stack is heated through top and bottom chuck to cure the BCB at 240 °C for 2h at unmodified pressure. Unconverted BCB monomers

undergo a ring-opening process that allows polymer chains to form. The fraction of converted BCB is a function of curing time and temperature, and can be expressed as [182]:

$$\ln\left(\frac{f_{(t)}}{f_0}\right) = -\int_{t=0}^{t} \alpha_{1,2} \cdot \exp\left[-\frac{E_a}{R}\left(T_{(t)}^{-1} - T_V^{-1}\right)\right] dt \qquad (3.5.1)$$

Where f_0 is the initial [1] and $f_{(t)}$ the temporary fraction of unconverted BCB and $T_{(t)}$ is the temperature profile over time t. The activation energy for BCB is $E_a = 36.04 \cdot 10^3$ cal/mol and $\bar{R} = 1.9858775$ cal/(mol K) is the universal gas constant ($N_A k$). T_V is the vitrification temperature (~483 K for slowly ramped cure cycles). The reaction rate $\alpha_{1,2}$ is 1.35 h^{-1} for $T < T_V$ and 0.2 h^{-1} for $T \geq T_V$. Fast curing cycles with elevated temperatures may lead to non-uniform heating, incomplete curing and increased stress, frozen in the wafer bonds [183]. The commonly used razor blade test is a pragmatic approach to evaluate qualitatively the wafer bond strength. The insertion of a blade in between a bonded wafer stack results in an opening length, correlated to the adhesive surface energy [184]. The developed process sequence finally yield wafer bonds, too strong to be evaluated quantitatively by this method, since the edge of the InP substrate cracks before being separated by the blade. These bonds proved to be sufficiently strong for the subsequent processing. After the InP substrate removal, the bond interfaces are inspected in detail. Fig. 3.19 demonstrates the homogeneous and void-free wafer bond of TS DHBTs on a 3" AlN substrate. BCB fracture reported in other TS approaches [115], e.g. due to mechanical stress of solder bonding, does not appear.

3.6 Summary

A wafer-level, TS process has been developed to optimize high frequency performance of InP DHBTs. It provides lithographic access to both, front- and backside of the transistors, aligned to each other. Thus, emitter and collector contact are scalable in proportion to each other, independent of the base width. The back-to-front side alignment accuracy in the stepper line of better than 100 nm over the 3" wafer is even within the specifications of a conventional process. The resulting linear device set-up eliminates dominant transistor parasitics and relaxes design trade-offs.

[1] 65 % for Cyclotene 3022-35 series

The essential step to gain access to both sides of the epitaxial structure is the substrate transfer. Therefore, a robust adhesive wafer bonding procedure has been developed via BCB. It yields for the first time in a wafer-level scale a homogenous, crack and void-free composite matrix of functional InP DHBT epitaxy embedded in BCB on the transfer substrate. Along with the innovative DHBT set-up, the 3D integration of passive elements and operational components on the transfer wafer supports functionality of the active devices and paves the way towards highly functional composite electronics e.g. of 3D heterogeneous integrated circuits.

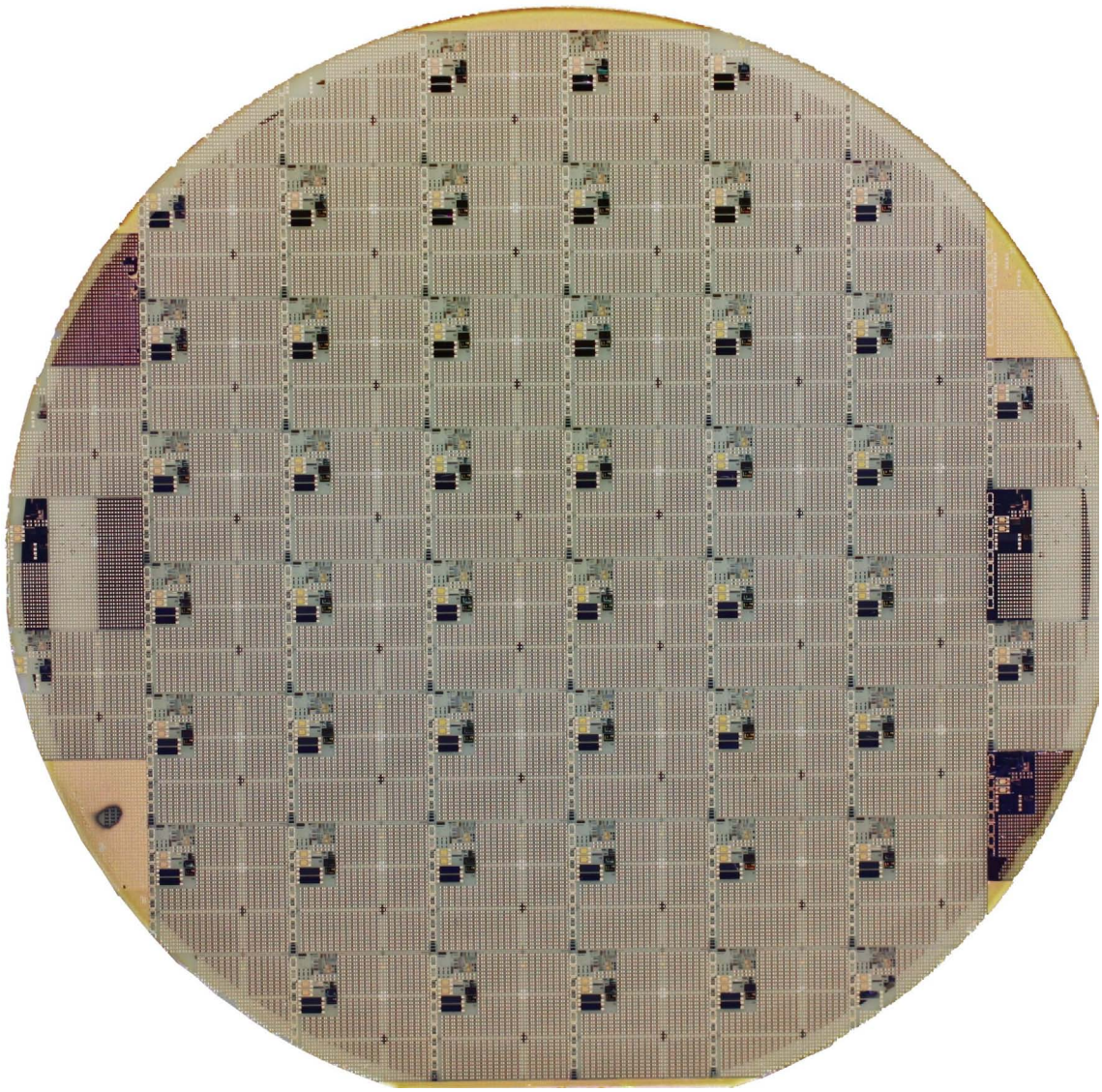

Fig. 3.19 Homogeneous and void-free 3" wafer bond of fully processed TS DHBTs on AlN substrate.

4 Transferred Substrate DHBT Results

DC and high frequency characteristics of the TS DHBTs are evaluated in this Chapter to quantify their performance and yield, to model them and extract critical parameters. All measurements were performed on-wafer, under ambient, non-pulsed biasing conditions. Within the variety of epitaxial, layout and technological modifications, the focus is on the latest thus best performing transistors. Epitaxy bases on #724 of Table 3.2 unless otherwise specified. To document the evolution of TS device development, results from three representative wafers with different layer structures are presented in the subsequent sections. In addition, diagnostic test structures are evaluated to monitor key device parameters during the process. Layout and process modifications are described if relevant for the device characteristics. Fig. 4.1 shows the baseline TS DHBT in its periphery set-up.

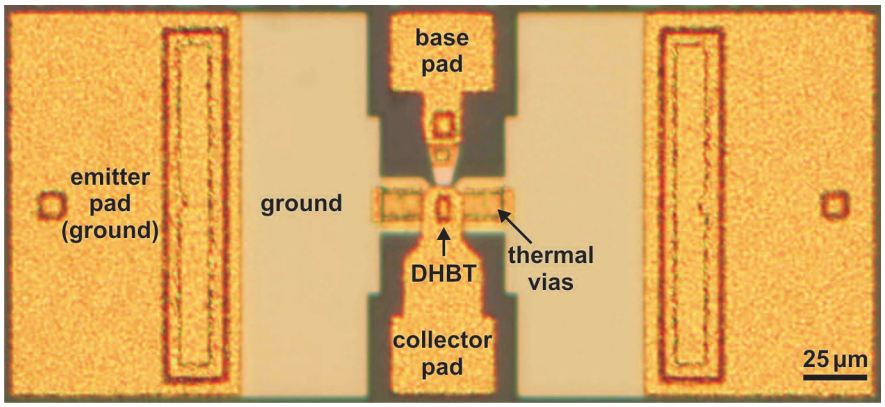

Fig. 4.1 Periphery set-up of baseline TS DHBT with $0.8 \times 5\,\mu m^2$ emitter size.

4.1 Process Control Monitoring (PCM)

Transmission line measurements (TLM) are performed to monitor the emitter, base and sub-collector resistances during fabrication [185]. Most critical for DHBTs are the base sheet and contact resistance. The TLM pattern in Fig. 4.2 consists of 5 contact pads, placed at increasing spacing. The intermediate gaps of 3, 6, 9, 12 µm are sidewise isolated by a bordering mesa. A multi-point measurement set-up determines the electrical resistance between the ohmic contacts. It depends on the metal–epitaxial contact resistivity ρ_c ($\Omega\mu m^2$), epitaxial sheet resistivity ρ_s (Ω/sq) and contact width W_c according to [186].

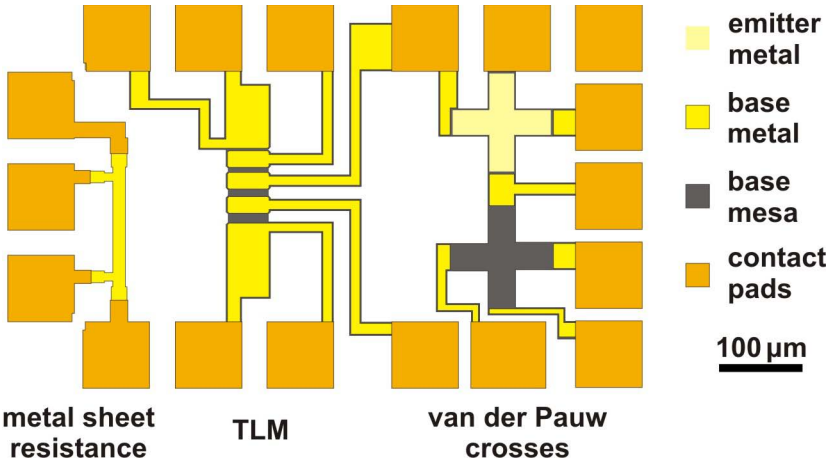

Fig. 4.2 **Diagnostic PCM pattern to evaluate metal sheet resistance, with TLM and van der Pauw crosses.**

The geometric separation x of the probe pads results in cumulative sheet resistances, but unchanged contact resistance R_c.

$$R_{TLM}(\mathrm{x}) = \frac{\rho_s}{W_c} \cdot \mathrm{x} + 2R_c \tag{4.1.1}$$

By plotting the resistances $R_{TLM}(x)$ versus the spacing, the sheet resistivity correlates to the slope.

$$\rho_s = \frac{\mathrm{d}R_{TLM}}{\mathrm{dx}} \cdot W_c \tag{4.1.2}$$

The contact resistivity can be extracted from the extrapolated intercept $R_{TLM}(x = 0)$ of the linear fit – the resistance value for zero spacing.

$$R_c = \frac{\sqrt{\rho_s \rho_c}}{W_c} \cdot \coth\left[\frac{L_c}{L_t}\right] \tag{4.1.3}$$

For the TLM pad lengths $L_c \approx 20\,\mu\mathrm{m}$, and ohmic transfer length $L_t = (\rho_c/\rho_s)^{1/2}$, with $L_c \gg L_t$, (4.1.3) reduces to:

$$\rho_c = \frac{1}{\rho_s}\left(\frac{R_{TLM\,(\mathrm{x}=0)}}{2} \cdot W_c\right)^2 \tag{4.1.4}$$

Photolithographic deviations of pad spacing Δx are critical for contact resistivity extraction. Especially for the base with a high sheet but low contact resistivity, SEM inspection of the TLM dimensions minimizes the extrapolation error.

TABLE 4.1

IMPROVEMENT OF CONTACT AND SHEET RESISTIVITY FROM EPITAXY #520 TO #724 OF SECTION 3.2 .

	emitter cap	**base**	**subcollector**
contact resistivity ρ_c ($\Omega\mu m^2$),	30 – 5	170 – 60	30 – 15
sheet resistivity ρ_s (Ω/sq)		1200 – 750 at 30 nm thickness	

The optimization of resistivities during TS device development from epitaxy #520 to #724 is given in Table 4.1. An In-rich emitter cap and optimized surface preparation of emitter and subcollector resulted in state-of-the art n-InGaAs DHBT contacts of 5 $\Omega\mu m^2$ and 15 $\Omega\mu m^2$, respectively. Since electron transport in the emitter and subcollector is vertical for TS DHBTs, their sheet resistivities are not specified. The base contact resistivity is less critical for the TS technology but could be subject to improvement [85]. The base sheet resistance of 30 nm p-InGaAs was lowered from 1200 to 750 Ω/sq by the transition from MOVPE to MBE epitaxy. The latter shows superior base doping and no hydrogen passivation, s. section 3.2.2.

4.2 DC Characteristics

In this section, the Gummel and common-emitter *I-V* characteristics of the InP/InGaAs/InP TS DHBTs are presented. DC measurements were performed on a semi-automatic wafer prober equipped with curve tracer system. Since TS DHBTs have large bandwidth, devices may oscillate during DC measurements. This is avoided by using a measurement set-up with shielded connections and controlled microwave impedances. Microwave probes are used to contact the devices during DC characterization. Bias-T's provide isolation from the multimeters through the inductor and a 50 Ω-termination through the capacitor. The arrangement is shown in Fig. 4.3.

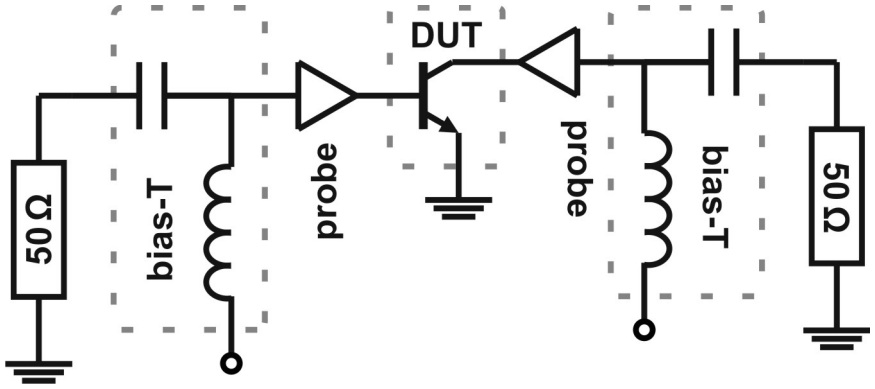

Fig. 4.3 Schematic DC measurement set-up.

Gummel plots are combined representations of transistor current I_C and I_B versus emitter–base voltage V_{BE} at constant collector–base bias V_{CB} on a semi-logarithmic scale. A number of device parameters such as DC current gain, ideality factors, leakage currents and series resistances can be directly evaluated either quantitatively or qualitatively. Fig. 4.4 shows the representative Gummel plot of a $0.8 \times 5\,\mu m^2$ emitter area TS DHBT using epitaxy #724 in Table 3.2. The device exhibits maximum current gain $\beta > 40$, with ideality factors $\eta_C \approx 1.1$ for collector–base and $\eta_B \approx 1.36$ for abrupt emitter–base junction, respectively. Leakage currents are below 0.1 nA.

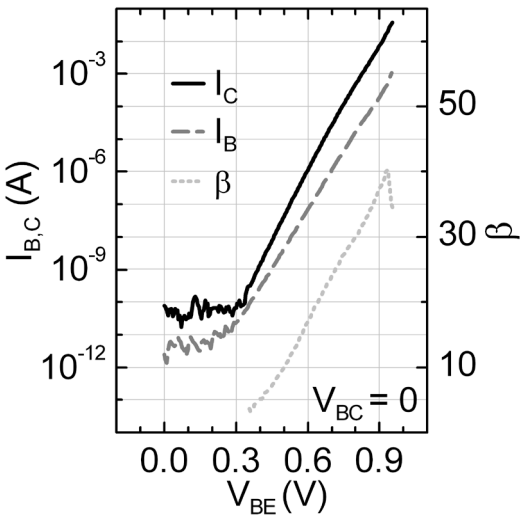

Fig. 4.4 Gummel plot of $0.8 \times 5\,\mu m^2$ TS DHBT of epitaxy #724.

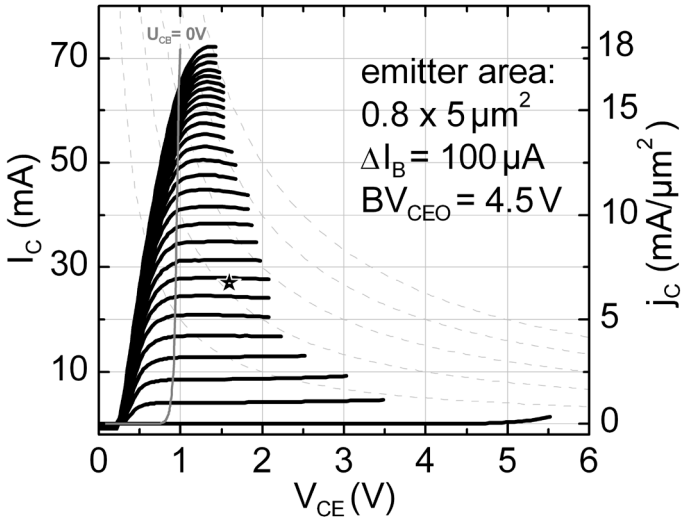

Fig. 4.5 Common-emitter *I-V* plot of $0.8 \times 5\,\mu m^2$ TS DHBT of epitaxy #724.

The corresponding common-emitter *I-V* curves in Fig. 4.5 also demonstrate well-behaved DC characteristics. The transistor features an offset voltage $V_{CE,offset} = 0.22\,\mathrm{V}$, moderate knee voltages and common-emitter breakdown at $BV_{CEO} > 4.5\,\mathrm{V}$ ($j_C \coloneqq 10\,\mu\mathrm{A}/\mu\mathrm{m}^2$). The non-zero value of $V_{CE,offset}$ reflects the difference between the abrupt emitter–base and graded collector–base junction of the DHBT. If these junctions were identical, the device would be symmetrical and $V_{CE,offset} = 0\,\mathrm{V}$. Maximum collector current is 72 mA, corresponding to $18\,\mathrm{mA}/\mu\mathrm{m}^2$. This is the highest current density, demonstrated by a transferred substrate approach [187], [188]. The more than six-fold increase compared to previously reported ones is a significant contribution to improved high frequency and power performance as discussed in section 2.6. The transistor spans a wide area of safe operation. Maximum DC power of over 100 mW demonstrates adequate heat sinking and is the highest reported for a transistor with f_T and f_{max} over 400 GHz, compare Table 4.2. The asterisks in Fig. 4.5 and Fig. 4.6 indicate optimal biasing for high frequency performance. Development of TS DHBTs is reflected in Fig. 4.6. Besides epitaxial improvement from #520 to #724 of section 3.2, an additional 4 µm thick galvanization layer optimized heat sinking for increased current handling capability and device resistances were reduced according to Table 4.1 .

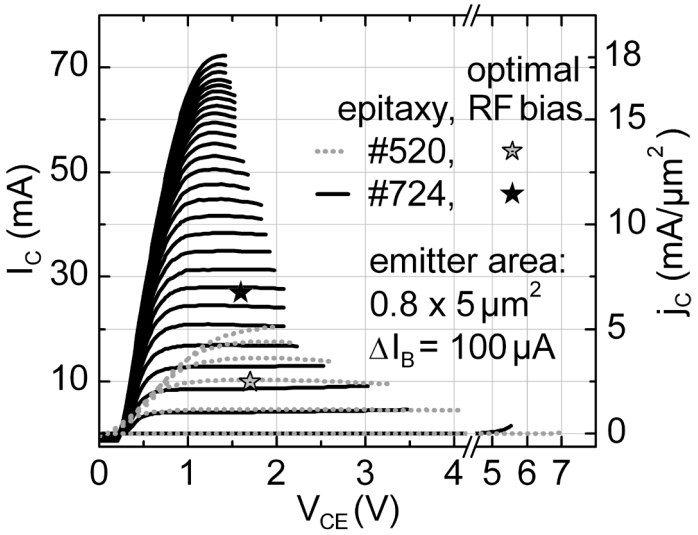

Fig. 4.6 Development of *I-V* characteristics for successive TS DHBT process runs.

4.3 High Frequency Characteristics

Devices were characterized up to 110 GHz by non-cooled, on-wafer measurements using an Agilent N5250 network analyzer. The calibration to the probe tips was performed via off-wafer LRM$^+$ calibration technique on a ceramic impedance standard substrate [189], [190]. For all results presented here, peripheral device parasitics have not been deembedded.

Fig. 4.7 shows the RF results of the previously characterized TS DHBT on wafer #724. The short-circuit current gain ($|h_{21}|^2$) and maximum unilateral gain (MUG) are calculated from the S-parameters. Transistors with extrapolated cutoff frequency f_T = 420 GHz and maximum oscillation frequency f_{max} = 450 GHz were realized at I_C = 27 mA and V_{CE} = 1.6 V. A similar epitaxial design with increased base doping and consequently 15% reduced base sheet resistance yields an f_T = 410 GHz and f_{max} = 480 GHz at I_C = 26 mA and V_{CE} = 1.6 V in Fig. 4.20. These are the highest f_T and f_{max} achieved by transferred substrate transistors [109], [110], [191]. Balancing power and speed, the $0.8 \times 5\,\mu m^2$ emitter of the TS DHBTs still maintains a substantial scaling potential according to section 2.6 to enhance high frequency performance.

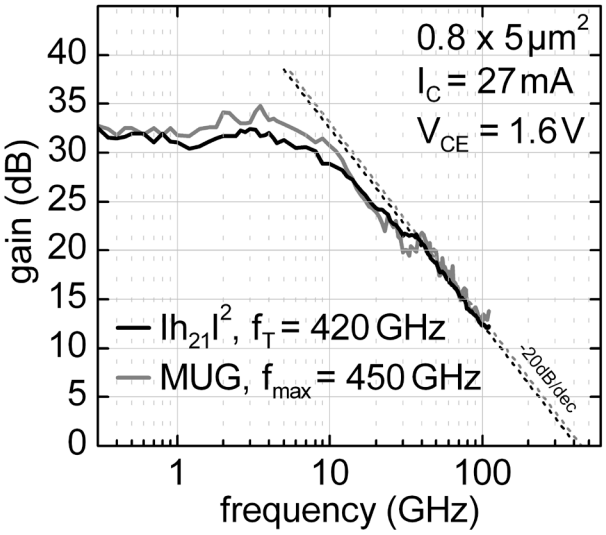

Fig. 4.7 Microwave gain $|h_{21}|^2$ and MUG with extrapolated f_T and f_{max} of a $0.8 \times 5\,\mu m^2$ emitter area TS DHBT of epitaxy #724.

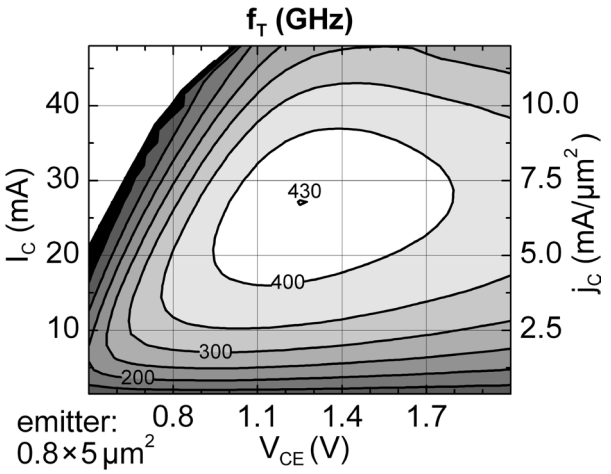

Fig. 4.8 f_T **under variable biasing of a** $0.8\times5\,\mu m^2$ **emitter TS DHBT.**

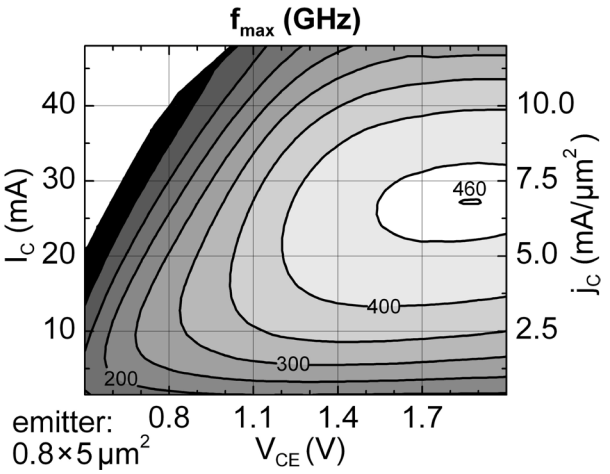

Fig. 4.9 f_{max} **under variable biasing of a** $0.8\times5\,\mu m^2$ **emitter TS DHBT.**

The characteristic f_T and f_{max} in Fig. 4.8 and Fig. 4.9 under variable biasing highlights the wide range of high frequency operation of the device. They were evaluated by extrapolating each measurement point with −20 dB/dec and calculating the arithmetic mean over the converging interval of $40-110\,\mathrm{GHz}$.

The benchmark in Fig. 4.10 is the international comparison of state-of-the-art InP HBT high frequency performance. Contour lines of constant reduced sum $(f_T^{-1}+f_{max}^{-1})^{-1}$ mark the figure of merit proposed in [192] to evaluate the ratio of f_T and f_{max}. The connecting line indicates the TS DHBT development within the successive process runs of this work. TS HBTs are represented by diamonds, whereas conventional triple mesa HBTs are labeled by dots. The biasing power $P = I_C \cdot V_{CE}$ is represented by the grayscale of the symbols. Respective HBT emitter widths are given in parentheses. The superscripts indicate the order of cross-references to Table 4.2, where further information on the HBTs is provided.

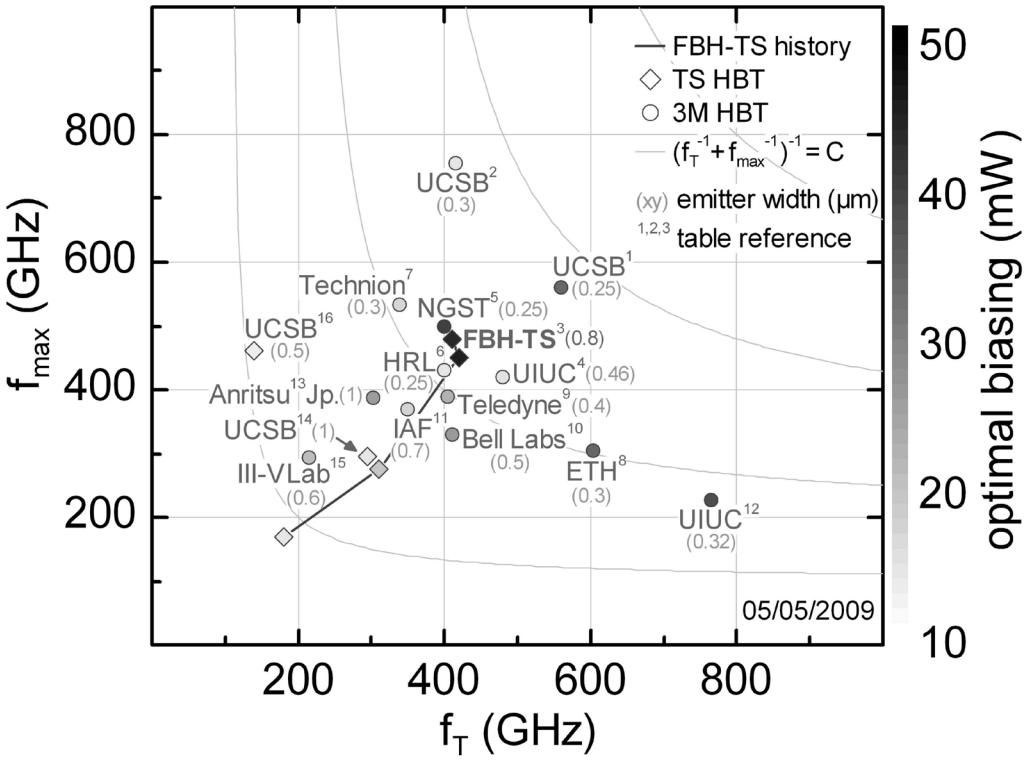

Fig. 4.10 Comparison of high frequency performance of state-of-the-art InP HBTs.

This work initiated the TS DHBT process at the FBH. Since then, major performance improvements have been accomplished. Meanwhile, the devices define the cutting edge of double side processed millimeter-wave transistors. Within state-of-the-art high-speed HBTs, the TS devices demonstrate highest power handling capability of optimal biasing, while not falling short of RF performance. Other HBTs of comparable emitter width show significantly lower f_T and f_{max}. As compared to the conventional HBTs in its vicinity, the two to three-times wider emitter provides a substantial scaling potential. In addition, the common-emitter *I-V* curves in Fig. 4.5 reveal considerable headroom of the technology for more aggressive biasing of down-scaled devices.

TABLE 4.2

COMPARISON OF STATE-OF-THE-ART INP HBTS.

f_T (GHz)	f_{max} (GHz)	I_C (mA)	V_{CE} (V)	BV_{CEO} (V)	Emitter Width W_E (µm)	Emitter Length L_E (µm)	$\frac{I_C \cdot V_{CE}}{W_E \cdot L_E}$ (mW/µm^2)	Institution	Ref.
560	560	22	1.45	3.3	0.25	5.5	23.2	UCSB[1]	[22]
416	755	6.98	1.74	4.6	0.3	2	20.2	UCSB[2]	[193]
420	450	27	1.6	4.5	0.8	5	10.8	TS FBH[3]	[194]
410	480	26	1.6	>5	0.8	5	10.4	"	[195]
310	275	10	1.7	>6	0.8	5	4.3	"	[196]
180	170	9.6	1.25	6.5	0.8	6	2.5	"	[197]
480	420	10.8	1.18	3.2	0.46	3.1	8.9	UIUC[4]	[23]
400	500	21	<1.8	>4	0.25	12	<12.6	NGST[5]	[198]
400	430	8.1	1.5	4.7	0.25	4	12.2	HRL[6]	[199]
338	534	9.1	1.6	>3	0.3	3	16.2	Technion[7]	[200]
603	305	32	1	4.2	0.3	11.5	9.3	ETH[8]	[201]
405	392	13.4	1.5	>4	0.4	5	10.1	Teledyne[9]	[87]
410	330	12	<2	–	0.5	4	<12	Bell Labs[10]	[202]
350	370	10	1.5	4.5	0.7	4	5.4	IAF[11]	[203]
765	227	35.9	~1	1.6	0.32	6	~18.7	UIUC[12]	[204]
302	388	17	1.4	6.2	1	5	4.8	Anritsu, Jp.[13]	[205]
295	295	12	1	>1.5	1	8	1.5	TS UCSB[14]	[110]
214	293	11.7	1.6	>6	0.6	5	6.2	III V Lab[15]	[206]
139	462	6	1.8	~8	0.5	8	2.7	TS UCSB[16]	[109]

suffix of institutions correlates to labels in Fig. 4.10

4.4 Power Performance

In order to estimate the power capabilities of TS DHBTs, they were characterized by large-signal measurements in a 50 Ω set-up. The power level of the input signal from a Gunn oscillator at 77 GHz is set by an attenuator. The in- and output of the device in common-emitter mode are connected by calibrated waveguides. Finally, the output signal is evaluated by a power sensor (Agilent W8486A). Device impedances, derived from S-parameter measurements, are Z_{in} = 15-j3 Ω and Z_{out} = 45-j10 Ω. The TS DHBT of $0.8 \times 5\,\mu m^2$ emitter area demonstrates a saturated output power P_{out} = 13.5 dBm (5.6 mW/μm^2) in Fig. 4.11. To the author's knowledge, the maximum output power of >13.5 dBm at 77 GHz is a record value for transistors with f_T and f_{max} over 400 GHz.

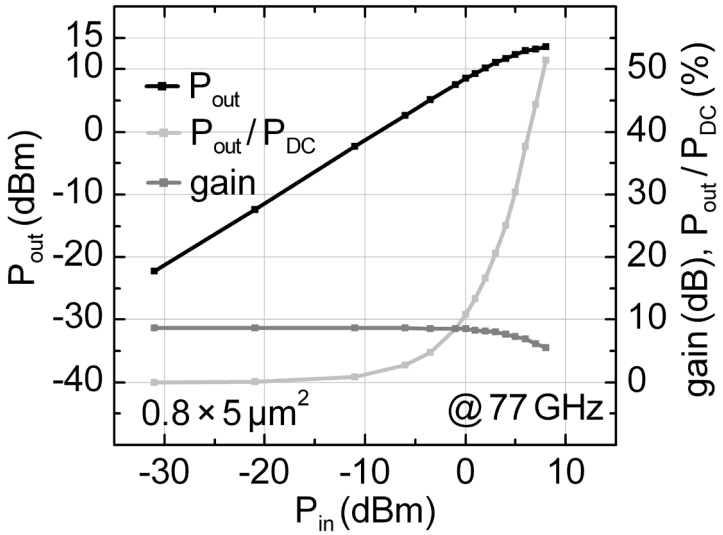

Fig. 4.11 Power measurement of a $0.8 \times 5\,\mu m^2$ emitter area TS DHBT in a 50 Ω set-up.

Since additional output power for a given epitaxy is achieved by increasing currents, power HBTs are set up in multiple finger topologies composed of several parallel emitter fingers. Most power HBTs in literature have been designed in so-called "fishbone" configuration [207], in which each emitter finger has a separate base mesa. Besides thermal and wiring issues, this complex configuration is chosen for conventional multi-finger devices to prevent excess collector–base capacitance C_{BC}. High current densities for optimal power and high frequency performance result in increased heat generation. Thermal coupling between the fingers may degrade transport properties and overall device characteristics compared to the single finger cell [66].

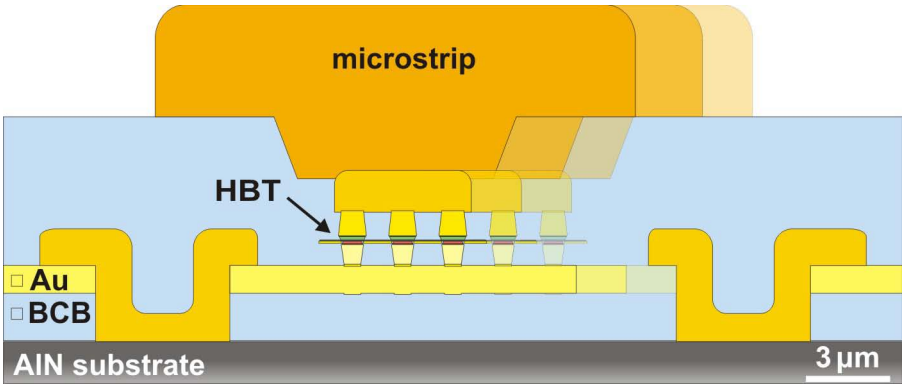

Fig. 4.12 Cross-section of a multi-finger TS DHBT with modular sequencing of transistor cells.

Scaling up the number of subcells in a multi-finger TS DHBT is far less complicated as shown in Fig. 4.12. Emitter and collector are accessed from the opposite side of epitaxy. No geometric constriction limits the parallel sequencing of the basic transistor cell. In between the planar inter-connect metallization of emitter and collector, the modular DHBT cells remain down-scalable for improved bandwidth and heat distribution. In principal, the interconnect metallization can be reinforced up to several microns according to thermal and electrical requirements. The straight-forward device design avoids interconnection parasitics by massive simplified wiring and results in very compact layouts. This is a major inherent advantage of this TS approach for high frequency, high power applications. For longer emitter fingers, a SiN_x spacer technology is advisable [87], since the resistance of the thin self-aligned base metallization degrades f_{max}.

Multi-finger TS DHBTs of $3 \times 0.8 \times 9\,\mu m^2$ emitter area in Fig. 4.13 and Fig. 4.14 show an f_T and f_{max} over 340 GHz at $I_C = 100$ mA and $V_{CE} = 1.6$ V. They demonstrate maximum biasing power density of $p = 12.5\,mW/\mu m^2$ and best f_T and f_{max} results for HBTs beyond $I_C = 100$ mA operation [208], [209], [210], [211], [212]. For operating frequencies around 100 GHz, this means that the output power should scale almost linear with the size of the transistor. However, their input and output impedances are less adapted to the 50 Ω set-up and no practical load pull measurement system existed in the power / frequency range of interest. Therefore, they have not been evaluated in this regard. The fact that no current collapse is observed in the biasing range up to $I_C = 135$ mA ($6.25\,mA/\mu m^2$) and $V_{CE} = 2$ V highlights the adequate thermal embedding of the devices [213]. Additional ballasting resistance is not required.

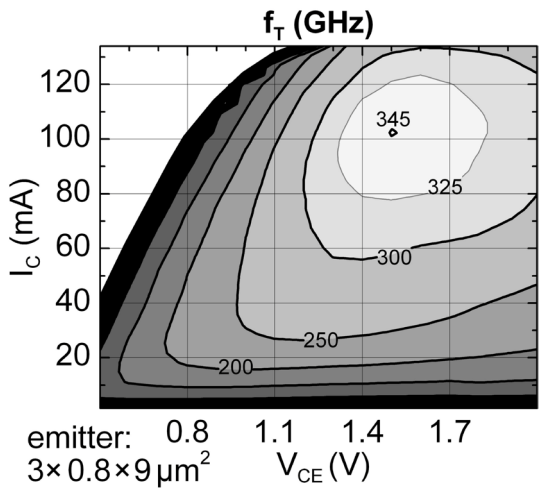

Fig. 4.13 f_T **under variable biasing of a multi-finger TS DHBT.**

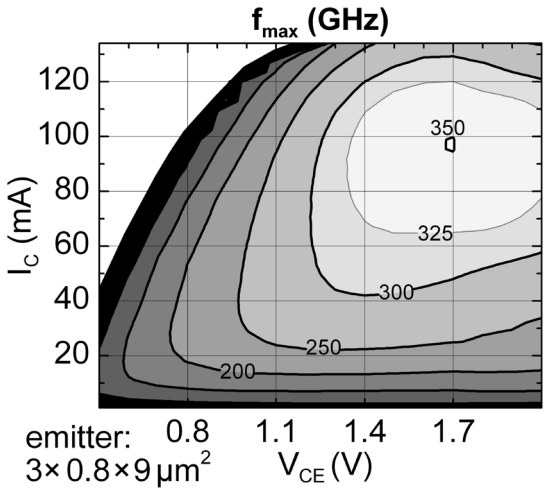

Fig. 4.14 f_{max} **under variable biasing of a multi-finger TS DHBT.**

4.5 Device Yield

Limited yield is a serious concern of previously reported TS processes. On the one hand, device failure was related to the employed bonding scheme and substrate removal [115], [119]. Bonds suffer from void formation, poor reproducibility, low thickness homogeneity [116] and mechanical stress of the composite matrix causing self-destruction of the protection layers during substrate removal [117], [118]. On the other hand, insufficient backside alignment, excessive post bonding wafer shrinkage [113] and mesa cracks [114], besides more general complications [112] motivated several groups to quit the TS technology finally again, in spite of the foreseen benefits. In addition, the TS HBTs were able to handle only a fraction of the current density of comparable triple mesa ones, required for maximum high frequency and power performance, because of thermal limitations [111], [120], [121].

Already early process runs of epitaxy #520 could demonstrate high yield and homogeneous device characteristics over a 3" wafer [196]. For each stepper shot, the cutoff frequency f_T and maximum oscillation frequency f_{max} of the identical TS DHBT within each shot is given in the wafer maps of Fig. 4.15 and Fig. 4.16. The arithmetic mean over the wafer of f_T = 300 GHz ±3 %$_{SD}$ and f_{max} = 250 GHz ±5 %$_{SD}$ reflects the reproducibility of the devices with a $0.8 \times 5\,\mu m^2$ emitter area.

Major factors of improvement are the adhesive bonding scheme by BCB, tie layers of SiN_x for improved BCB adhesion, etch stop layers, matched thermal expansion of the transfer substrates and adequate thermal embedding of the devices.

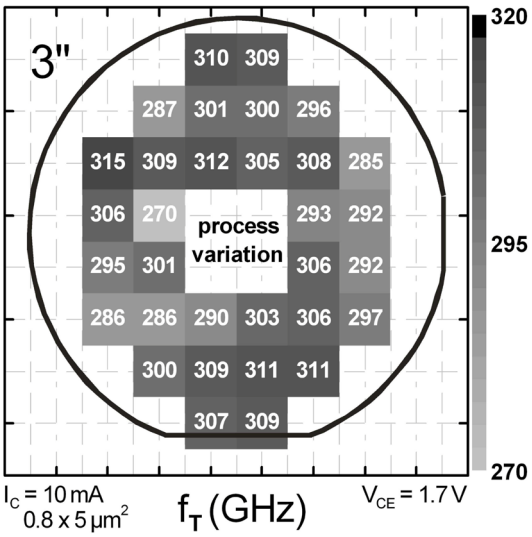

Fig. 4.15 Wafer map of f_T, epitaxy #520.

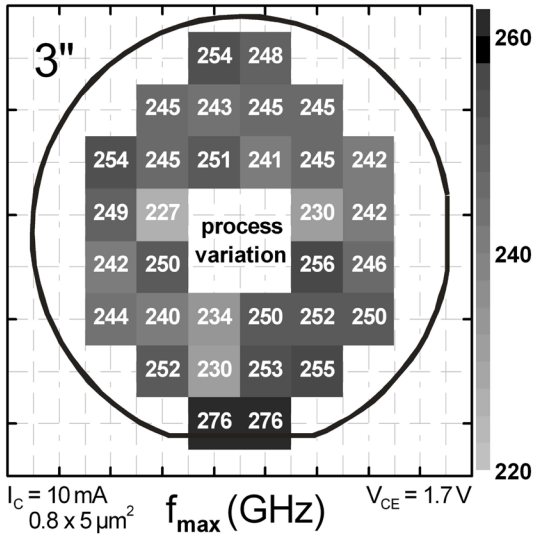

Fig. 4.16 Wafer map of f_{max}, epitaxy #520.

4.6 Device Modeling

4.6.1 Small-Signal Modeling

Transistor models are employed to describe device performance for parameter extraction and circuit simulation. The equivalent circuit in Fig. 4.17 is a simplified representation of the distributed *RC* elements within the HBT. The correlation of its components to device physics allows an effective feedback from parameter extraction to device fabrication. The corresponding T-model is a pragmatic tool to evaluate transistor properties under small-signal excitation. It is a current-controlled model based on the complex and frequency dependent current transfer ration α of the emitter current I_e, accounting for the current gain and phase delay of the device. The inner transistor is identified with emitter–base C_{be} and collector–base intrinsic $C_{bc}{}^{in}$ and extrinsic $C_{bc}{}^{ex}$ capacitance, as well as base layer resistance R_{b2} and differential emitter–base resistance R_{be}, whereas emitter, base, collector resistances (R_e, R_b, R_c) inductances (L_e, L_b, L_c) and capacitances ($C_{b,pad}$ and $C_{cb,pad}$) of contacts, feed lines and pads account for the periphery.

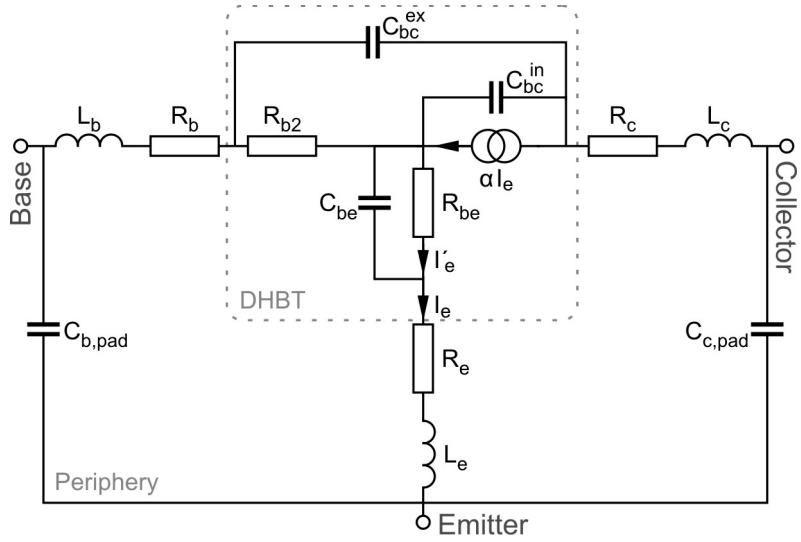

Fig. 4.17 Small-signal equivalent circuit including parasitic elements.

TABLE 4.3

SMALL-SIGNAL EQUIVALENT CIRCUIT ELEMENTS OF $0.8 \times 5\,\mu m^2$ TS DHBT AT $V_{CE} = 2$ V.

extrinsic elements							
$C_{b,pad}$ (fF)	$C_{c,pad}$ (fF)	R_b (Ω)	R_c (Ω)	R_e (Ω)	L_b (pH)	L_c (pH)	L_e (pH)
9.6	1.6	2.0	3.5	2.2	30	32	0
intrinsic elements							
I_C (mA)	R_{b2} (Ω)	C_{be} (pF)	R_{be} (Ω)	$C_{bc}{}^{in}$ (fF)	$C_{bc}{}^{ex}$ (f F)	τ (ps)	α
2.4	45	0.1	19.8	3.1	8.8	0.80	0.964
5.6	43	0.3	8.1	2.2	9.2	0.57	0.968
8.8	42	0.6	4.6	1.8	9.2	0.47	0.969
12.1	42	1.0	3.0	1.6	9.1	0.40	0.970
15.6	41	1.8	2.1	1.5	9.0	0.37	0.971
18.9	41	2.3	1.6	1.4	8.9	0.35	0.971
22.4	40	1.8	1.3	1.4	8.9	0.34	0.971
25.7	40	–	1.0	1.4	8.9	0.34	0.971
28.4	39	–	0.8	1.5	8.9	0.35	0.970

The parameters provided in Table 4.3 were extracted from S-parameters by an analytical algorithm [214]. The epitaxial design of the device is similar to #724 in Table 3.2, but with increased base doping and consequently 15% reduced base sheet resistance. Fig. 4.18 and Fig. 4.19 show Gummel plots and common-emitter output *I-V* curves of the $0.8 \times 5\,\mu m^2$ emitter TS DHBT. The transistor demonstrates a peak current gain $\beta > 30$ and a common-emitter breakdown voltage $BV_{CEO} > 5.5\,V$. The maximum collector current is 44 mA, corresponding to 11 mA/μm^2. The cutoff frequency $f_T = 410\,GHz$ and maximum oscillation frequency $f_{max} = 480\,GHz$ at $I_C = 26\,mA$ and $V_{CE} = 1.6\,V$ were evaluated in Fig. 4.20 again by extrapolating each measurement point with −20 dB/dec roll-off and calculating the arithmetic mean over the converging interval of 40 – 110 GHz.

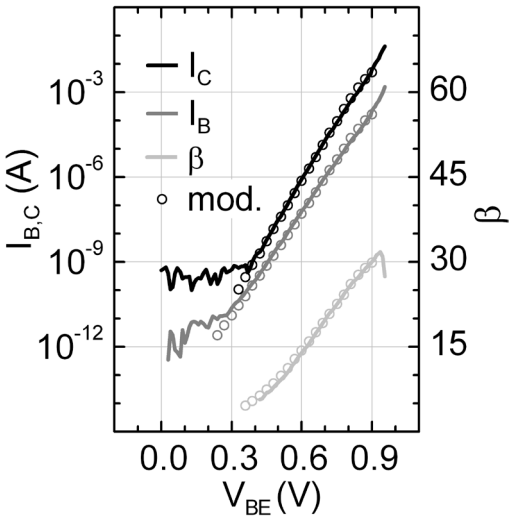

Fig. 4.18 Measured (lines) and modeled (symbols) Gummel plot.

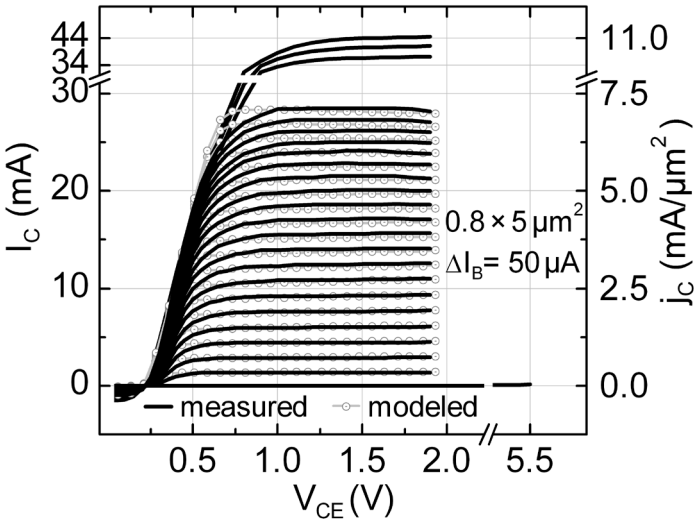

Fig. 4.19 Measured (lines) and modeled (symbols) common-emitter *I-V* plot.

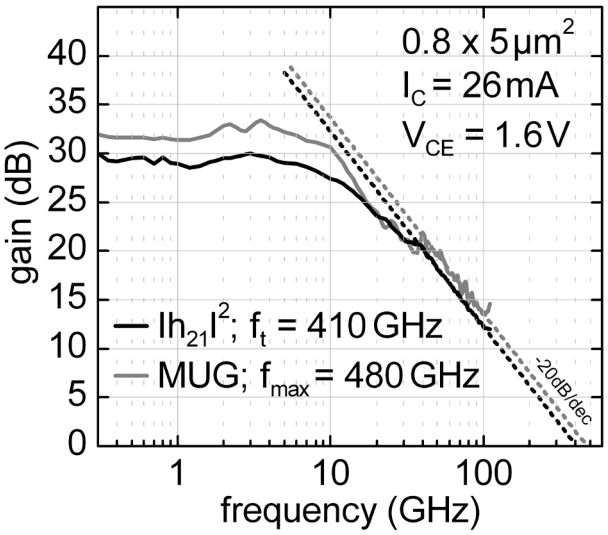

Fig. 4.20 Microwave gain $|h_{21}|^2$ and MUG with extrapolated f_T and f_{max} of a $0.8 \times 5\,\mu m^2$ emitter area TS DHBT of epitaxy #725.

All equivalent circuit elements are nondispersive, except for the current gain α that is defined by $\alpha := \alpha_0 \cdot e^{-j\omega\tau}$, with DC current gain α_0 and time delay τ. Since the transit frequency of the transistors is significantly higher than the upper frequency limit even though S-parameters were measured up to 110 GHz, it is not possible to determine unambiguously whether the phase shift observed in α is caused by the time delay τ or by a cutoff frequency ω_α. Therefore, only τ is given that describes the total intrinsic time delay. The equivalent circuit splits the total collector–base capacitance $C_{bc} = C_{bc}{}^{in} + C_{bc}{}^{ex}$ into an intrinsic and extrinsic part. For the TS DHBT this subdivision describes the *RC* network directly underneath the collector metal. The geometrical interpretation of the elements is not as straight forward as for a conventional triple mesa device set-up, but it allows to separate between the base contact R_b and base layer R_{b2} resistance. The values given in Table 4.3 reveal that the DHBTs take full advantage of the TS process. For example, the extrinsic and intrinsic base resistances are always less than 50 Ω and the value of the total collector–base capacitance as low as 11 fF for the TS DHBT with $0.8 \times 5\,\mu m^2$ emitter and $1 \times 5.5\,\mu m^2$ collector mesa area.

Without collector removal, TS DHBTs show a more than 50% higher total collector–base capacitance during small-signal extraction. Cutoff frequencies f_T and f_{max} are shown in Fig. 4.21 for a wide range of bias points. Values extrapolated from S-parameter measurements are compared with values calculated from the small-signal equivalent circuit according to [215], [216]:

$$\frac{1}{2\pi f_T} \approx \tau + (R_e + R_{be} + R_c) \cdot (C_{bc}^{in} + C_{bc}^{ex} + C_{c,pad}) \tag{4.6.1}$$

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi \left[R_{b2} C_{bc}^{in} + R_b \left(C_{bc}^{in} + C_{bc}^{ex}\right)\right]}} \tag{4.6.2}$$

The curves obtained by the two approaches show a difference of less than 10%, which confirms that the extrapolations from S-parameters and the extracted small-signal equivalent circuits provide reliable data. Based on the extracted TS DHBT model, critical parameters to improve high frequency performance are identified, process optimizations are assessed and their results are projected in Chapter 7 by remodeling.

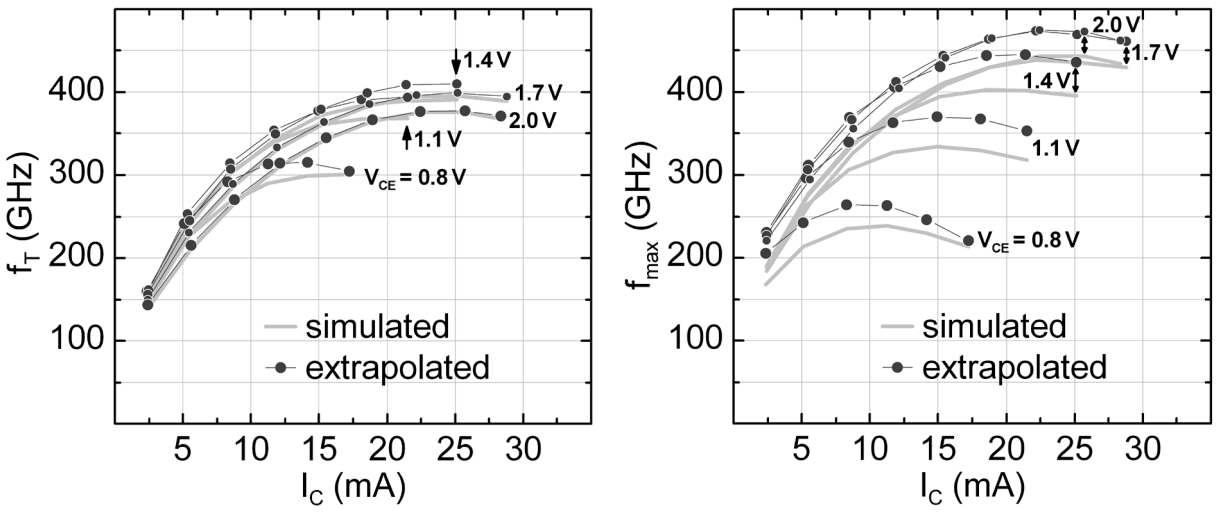

Fig. 4.21 f_T and f_{max} under variable biasing of a 0.8 × 5 µm² DHBT, calculated (lines) from equivalent circuit and extrapolated (symbols) from S-parameters at V_{CE} = 0.8–2 V.

4.6.2 Large-Signal Modeling

To model transistors for circuit design beyond small-signal operation, a more complex model is required. A nonlinear representation was determined for the TS DHBTs, based on the "FBH HBT" model [216]. Among other features, the large-signal model accounts for non-ideal base currents, self-heating, and bias dependence of the collector transit time. The model is available in Verilog-A. All simulations were performed by relying on a commercial circuit simulator. Fig. 4.22 illustrates the corresponding large-signal equivalent circuit. Components not relevant for modeling accuracy of the TS DHBTs are disabled and represented in gray.

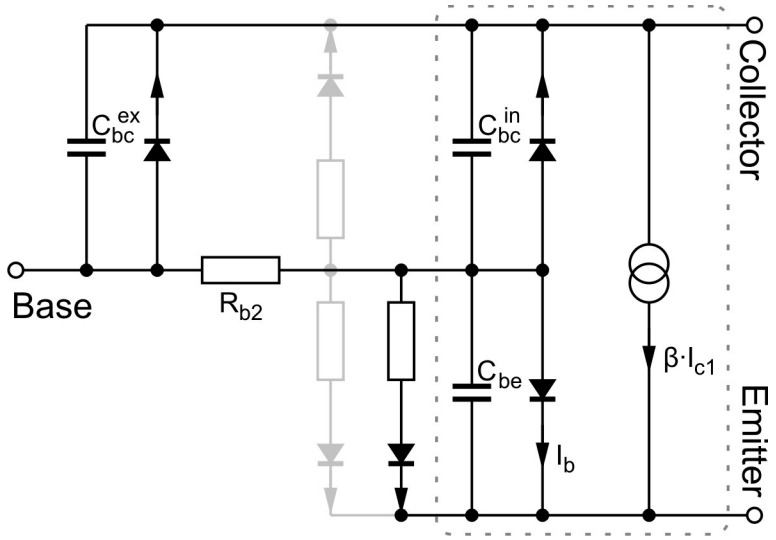

Fig. 4.22 Equivalent circuit of the FBH large-signal DC model, components not employed for modeling are in gray.

Good agreement between simulations and measurements is seen in Fig. 4.18 and Fig. 4.19 for Gummel plots and common-emitter output *I-V* curves. Only comparisons with the simulated data reveal that current blocking is observed at the DHBTs at low voltages and high currents. This effect is caused by a potential barrier formed at the base-collector p-n junction under these bias conditions. However, the deviation from measurement is not significant even in this region. Therefore, it has not yet been considered to augment the FBH HBT model by a quasi-saturation model, as known from literature [217].

Small-signal equivalent circuits were extracted for a number of bias points in order to determine the charge functions governing the RF behavior by integrating small-signal capacitances and time constants. Fig. 4.23 provides a comparison of measured and simulated S-parameters of the $0.8 \times 5\,\mu m^2$ DHBT, at $V_{CE} = 2\,V$ and $I_C = 15, 20, 25\,mA$. The simulation closely matches the measured data well up to 110 GHz. Although the FBH HBT model was developed focusing on GaAs HBTs, it proves to be suited for the InP-based TS DHBTs despite their transit time showing a slightly different shape depending on collector current. Consistent large-signal modeling of the TS DHBTs proves the availability of the technology for advanced millimeter-wave circuit design.

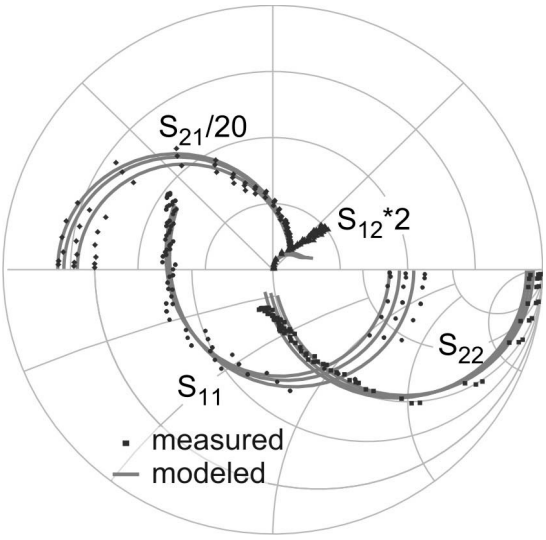

Fig. 4.23 Measured and modeled S-parameters of a $0.8 \times 5\,\mu m^2$ TS DHBT, $f = 50\,MHz - 110\,GHz$, $V_{CE} = 2\,V$, $I_C = 15, 20, 25\,mA$.

4.7 Summary

The TS process provides a linear device set-up that eliminates dominant transistor parasitics and relaxes design trade-offs. For TS DHBTs without collector backside removal, small-signal extractions reveal a 50% higher collector–base capacitance. The optimized device topology manifests in excellent device performance.

Transistors of $0.8 \times 5\,\mu m^2$ emitter area feature $f_T = 420\,GHz$ and $f_{max} = 450\,GHz$ at a breakdown voltage $BV_{CEO} > 4.5\,V$. The devices define the cutting edge of double side processed millimeter-wave transistors. Within state-of-the-art high-speed HBTs, the TS devices demonstrate highest power handling for optimal biasing, while not falling short of RF performance. Other HBTs of comparable emitter width show significantly lower f_T and f_{max}.

The more than six-fold increase in current density to $18\,mA/\mu m^2$ compensates the limitation of previously reported TS HBTs as compared to conventional ones. The $0.8 \times 5\,\mu m^2$ emitter transistors combine very high frequency performance with saturated output power $P_{out} > 13.5\,dBm$ at 77 GHz and DC power handling over 100 mW, but also maintain a substantial scaling potential to enhance high-speed operation.

The straightforward device set-up of multi-finger TS DHBTs enables parallel sequencing of the basic transistor cell. The compact layout simplifies wiring and avoids additional interconnection parasitic while scaling up the transistor for millimeter-wave power operation. Consistent small- and large-signal transistor modeling, together with high yield and homogeneous device characteristics over the 3" wafer provide a promising tool kit for high-speed circuit design.

5 Circuit Design & Results

Traveling-wave amplifiers (TWA) are building blocks in high bit-rate and high frequency transmission chains. For these applications, it is a key issue to combine high frequency performance and power capabilities with adequate yield [218], [219]. The TWAs presented here demonstrate the ability of the TS technology to meet these requirements. They are distinctive demonstrators to evaluate a technology in terms of performance, uniformity and yield.

In this Chapter, the TS Process is developed to a full MMIC compatible technology. A complete set of metal–insulator–metal (MIM) capacitors, NiCr resistors, spiral inductors and interconnects, including microstrip transmission lines, crossings and bends have been developed in the multi-level wiring scheme. Precise descriptive and predictive models of the passive elements are required for reliable circuit design. Thus, electromagnetic simulations of the passive elements were performed to optimize them and investigate parasitic effects at intended operating frequencies. Their equivalent circuit models have been derived in ADS software for circuit design and validated by test structures. Together with the transistor models of section 4.6, they have then been used as a design kit for circuit simulation. Finally, TWAs have been designed and realized, while their architecture was adapted to the advantages and particularities of the TS approach.

5.1 Passive Elements

The multi-level metallization scheme of the TS set-up enables the design of passive structures in manifold 3D configurations [220]. Due to the distribution of passive parts in the lateral and vertical directions, structures can be made smaller for space-saving design and improved RF performance. A detailed knowledge of the constitutive passive elements is decisive for circuit design. Therefore, the high frequency characteristics of the passives have been carefully investigated.

5.1.1 Capacitance

Fig. 5.1 shows the S-parameters of a $30 \times 130\,\mu m^2$ blocking MIM capacitor with the bottom plate connected to ground. The thickness of the dielectric SiN_x layer is $d \approx 300\,nm$ with a dielectric constant $\varepsilon_r \approx 7.2$. The electromagnetic simulations are based on a finite difference time domain (FDTD) code from CST [221], while equivalent circuit modeling is done by ADS software. The 0.88 pF capacitors demonstrate consistent measurement, modeling, and simulation up to 110 GHz.

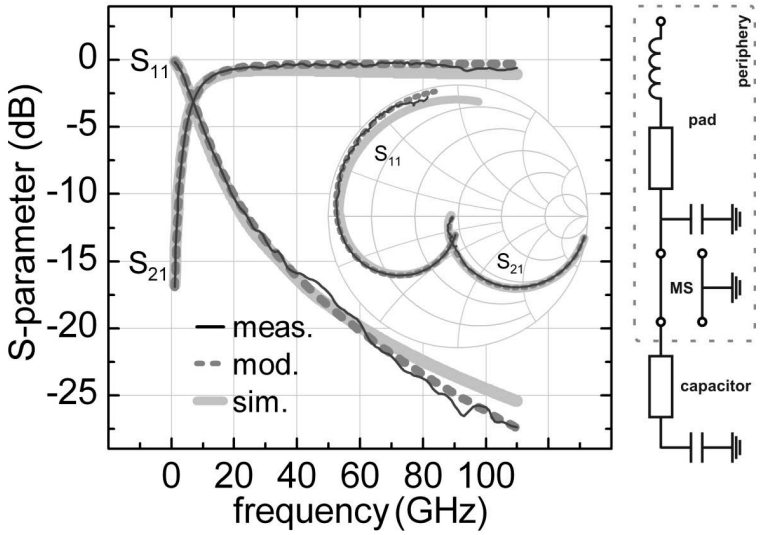

Fig. 5.1 S-parameters of a 0.88 pF blocking capacitor measured, modeled and simulated from 1 – 110 GHz with corresponding equivalent circuit diagram aside.

5.1.2 Resistance

The test resistor of 33 Ω has a width of 55 µm and length of 170 µm. The resistivity of the 300 nm thick NiCr layer was adjusted by the length to width ratio. To enhance heat dissipation, the NiCr was placed on top of the AlN carrier substrate below the ground level. Feeding microstrips were connected through the opening of the ground. S-parameters in Fig. 5.2 demonstrate accurate agreement between measurements, equivalent circuit fittings, and electromagnetic simulations.

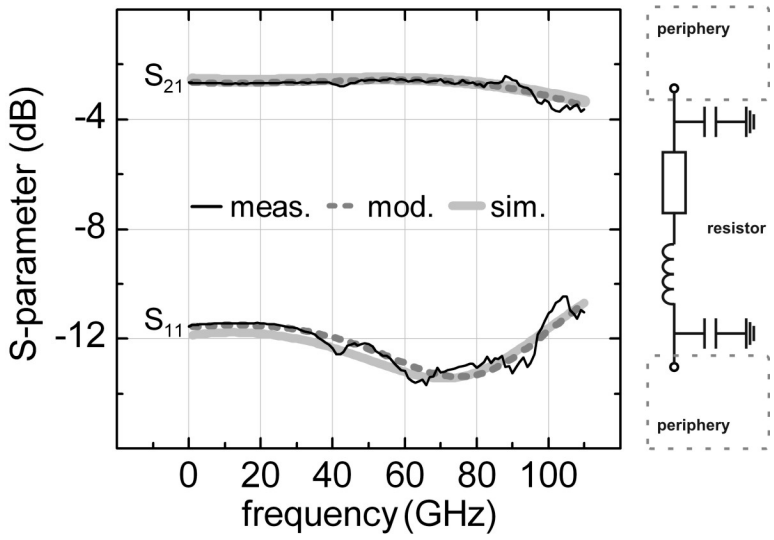

Fig. 5.2 S-parameters of a 33 Ω resistor measured, modeled and simulated. The periphery of the equivalent circuit aside is analog to Fig. 5.1.

5.1.3 Transformer

The capability to distribute passive parts in lateral and vertical direction for improved RF electrical performance and space-saving design is demonstrated by a weakly coupled transformer of $90 \times 90\,\mu m^2$ in size. This transformer consists of two spiral inductors, one below the other, as sketched in the inset of Fig. 5.3. Upper and lower spirals are made of 1.5 loops, separated from each other by 6.5 µm of BCB and feature 8 µm wide metal stripes, with a lateral line distance of 10 µm. The connection to the ground at the center of the spirals leads through a 1.5 µm thick link, almost equally separated between the double-layered inductors. The main application range of the transformer is up to 60 GHz. Beyond 40 GHz, the spatial dimensions of the inductors matter. To model the distributed network, the equivalent circuit of the basic cell in Fig. 5.4 is extended by an appended cell of self- and mutual-inductances as well as capacitances. Prober pads are deembedded. Frequency dependent ohmic losses $R_{i(f)}$ due to the skin effect are included, as for all simulations presented in this Chapter. Fig. 5.3 shows measurement, FDTD simulation, and equivalent circuit fitting results by ADS software. The curves show accurate agreement up to 110 GHz.

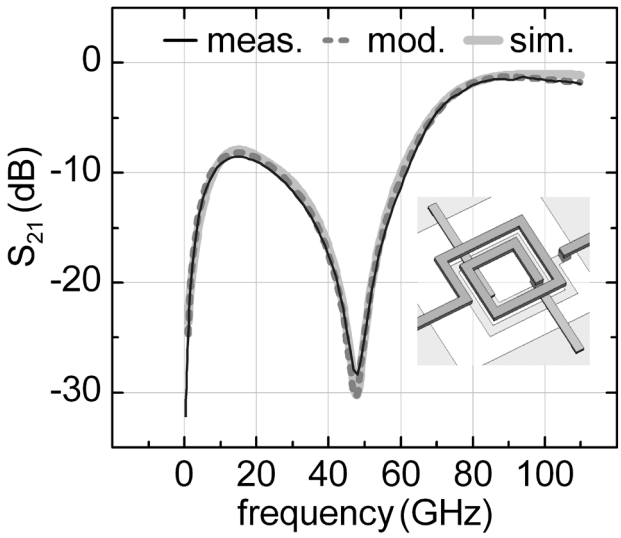

Fig. 5.3 **Comparison between measurement, FDTD simulation and equivalent circuit fit of the transformer with schematic inset of the set-up.**

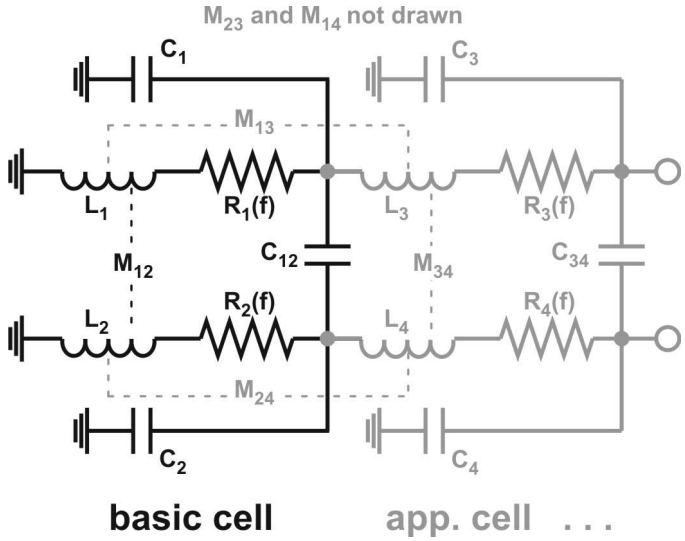

Fig. 5.4 **Equivalent circuit of the transformer extended by self- and mutual-inductances as well as capacitances.**

5.1.4 Interconnects

For the TWAs, a thin film microstrip was chosen as basic line type. This wiring architecture features low ground via inductance, simplifies ground plane distribution and minimizes the risk of higher order modes over an extended frequency range. The microstrip consists of electroplated interconnects, 8 µm wide and 4 µm high, separated from the ground by 5.3 µm of BCB with $\varepsilon_r = 2.7$. Substrate modes are not relevant since the patterned ground shields the supporting substrate underneath.

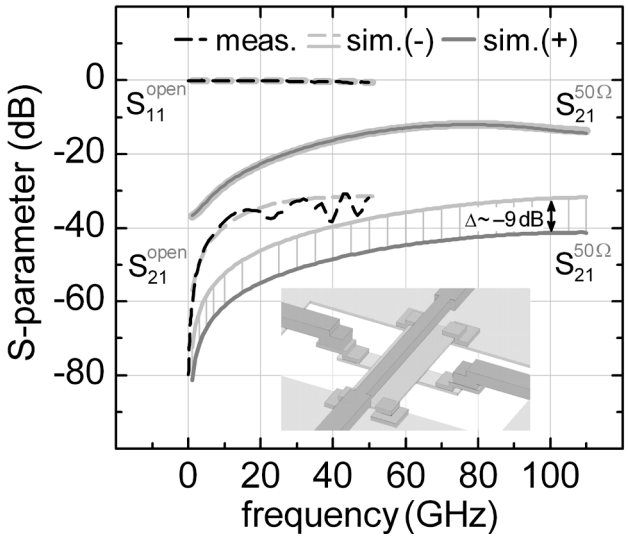

Fig. 5.5 Cross-talk measurements of a crossing compared to simulation:
1) unprobed lines open (dot) / 50 Ω-finished (solid).
2) with (+) / without (-) shielding ground plane in between, s. inset.

TWA line routing requires several crossings. These are made of BCB embedded transmission lines, tunneling perpendicular under the standard microstrip at a distance of 3.5 µm. Cross-talk has been evaluated in Fig. 5.5 by S-parameter measurements up to 50 GHz in an orthogonal input / output probe set-up. Both unprobed lines were left open in order to reflect the available power and, thereby, increase the already low-level transmission for more accurate measurements. The simulations are in line with measurements and estimate a S_{21}-coupling below −31 dB up to 110 GHz for an open termination, as well as for 50 Ω. With increased circuit complexity, shrinking

dimensions and multiple crossings, cross-talk becomes more critical. For further improvements, shielded crossings have been implemented with a decoupling ground layer between the lines. Simulations in Fig. 5.5 reveal a coupling reduction of about −9 dB.

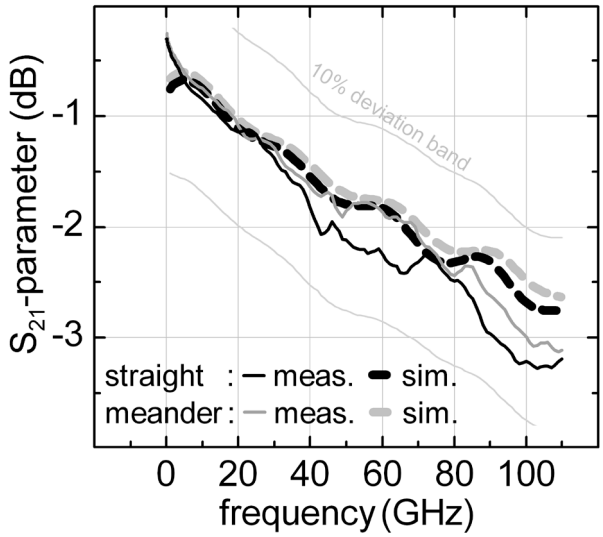

Fig. 5.6 Measured and simulated S_{21} of a meander and straight microstrip line, both of 3328 µm length.

To provide the successive sections of a TWA with the required phase shift, the dimensions of the connecting lines between the sections have to be carefully adjusted. For a compact layout, the microstrips were folded into meanders. Since the folds reduce the effective path length of the waveguide, folded and straight lines of identical length do not have the same phase shift. Since the phase shift is a key parameter in TWA design, a quantitative analysis of the difference between folded and non-folded lines has been performed. Two lines of 3328 µm are compared here. The folded line features eight rectangular meanders of 82 µm edge length, each with a 170 µm separation, and additional 78 µm extensions to both contact pads. The measured results in Fig. 5.6 match well with the respective simulated curves. To account for non-ideal metallization morphology (e.g. grain size, surface roughness), an effective conductivity of 15 MS/m is a reasonable empirical approximation. The phase difference between the straight and meander lines in Fig. 5.7 is about 0.3°/GHz up to 110 GHz. Apart from the phase shift, the S_{21}-parameters of both line types are almost equal. Their attenuation is about 0.9 dB/mm at 110 GHz.

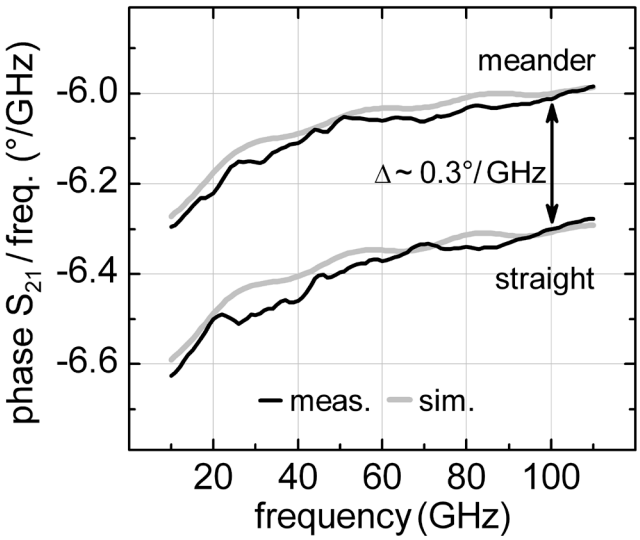

Fig. 5.7 Difference of normalized phase between meander and straight microstrip line, both 3328 µm long.

5.2 TWA Circuit Concept

According to the principle of distributed amplification, a TWA is formed by the parallel connection of amplifying cells via inductors. Input and output capacitances of the active devices together with the inductances and connecting lines form equivalent transmission lines. These artificial input and output lines are designed to have, in principal, 50 Ω characteristic impedance and to achieve flat and equal group delay over the band. Thus, a DHBT-based TWA can be represented by the equivalent circuit in Fig. 5.8. L_b and L_c describe the added inductances to form the input and output artificial transmissions lines, respectively, v_k is the signal voltage swing at the reference plane of each inductor cell, i_k is the generated current for each cell and $y_0 = i_k / v_k$ is the transconductance gain.

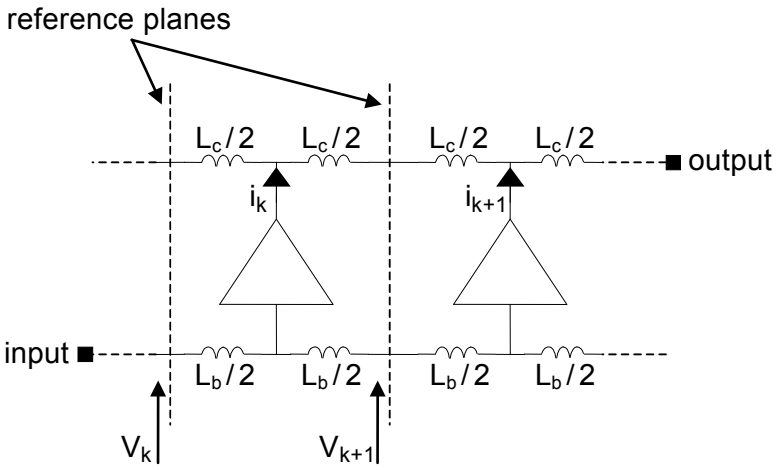

Fig. 5.8 Equivalent small-signal circuit of a TWA.

Fig. 5.9 presents the circuit diagram. The collector (output) line is terminated by a 50 Ω load as is the base (input) line. The backward waves are absorbed in the 50 Ω resistor, which also feeds the base and collector bias of the transistors. The chosen gain cell is a cascode pair. By canceling the Miller effect, the equivalent bridge capacitance between the input and output of the cell becomes smaller than in the case of a simple common-emitter set-up. This provides wider bandwidth. In addition, a feedback resistor at the emitter is used to broaden the bandwidth and to increase the input impedance of the cell. The connection between the transistor and feedback resistor was optimized by integrating them closely together into a compact layout element.

The gain-frequency slope is mainly determined by the unit cell design, in particular the numerical optimization of the emitter feedback resistor (a 5 Ω resistor was used to flatten the gain over the bandwidth) and careful decoupling of the second cascode base. This is a key condition for high frequency operation. The base node was precisely simulated because it can cause the real part of the output impedance to become negative, which can lead to instabilities if it is too sharply decoupled. By means of supplementary resistors added on the artificial transmission lines and

the feedback resistor on the emitter, a smooth decreasing slope gain is achieved. In our design, the base node is locally decoupled with a series dump resistor of a few ohms, a 5 pF capacitor to the nearest emitter, and the base is connected to a longer DC bias line. Thus, floating ground planes due to the dimensions of the circuit will not influence the performances of the amplifier. In addition, the microstrip technology allows us to have real ground planes on all points of the circuit.

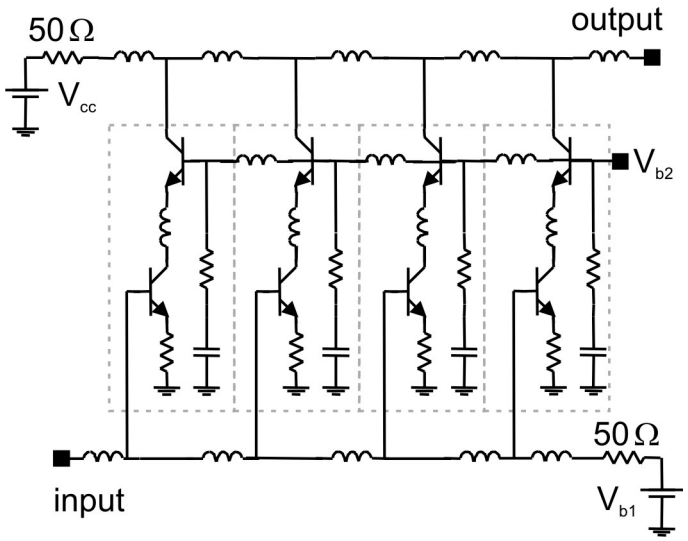

Fig. 5.9 Circuit diagram of the realized TWA.

5.3 TWA Results

The chip photo of the TS TWA is given in Fig. 5.10. On-wafer small-signal measurements in Fig. 5.11 demonstrate 12.8 dB broadband gain with a smooth continuous decrease up to a 3-dB cutoff frequency f_c of 70 GHz. Beyond f_c, the TWA still provides gain to amplify higher frequency components and to improve the waveform by a smooth decrease in time delay. The available headroom in cutoff frequency of the employed $0.8 \times 5\,\mu m^2$ TS DHBTs can be used to further improve the signal waveform by optimizing group delay [222] or to increase the gain at very high bit-rate. The DC power consumption of the circuit is about 105 mW for a 24 mA DC current and about 4.4 V collector voltage.

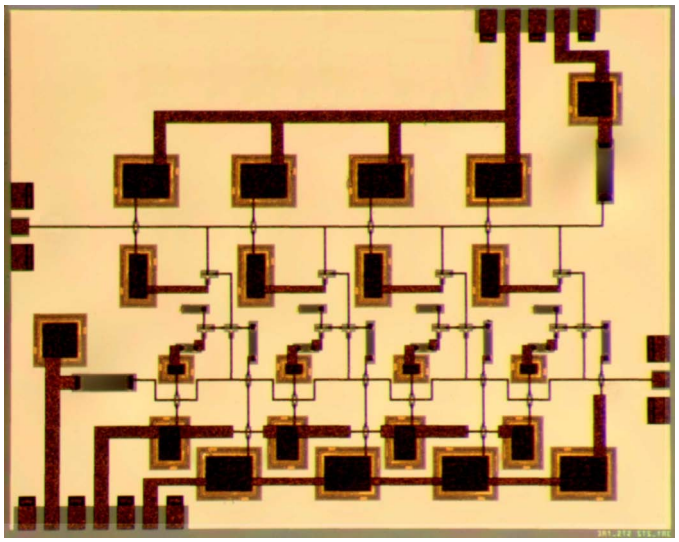

Fig. 5.10 Chip photo of the TWA in TS technology.

Fig. 5.11 also shows the simulated gain of the amplifier. Discontinuities of the TWA such as bends, crossings, and meanders are included. Their ADS compatible models were generated from preceding electromagnetic simulations. Passive elements of section 5.1, such as MIM capacitors NiCr resistors and microstrips, were also simulated and their parasitics were investigated in order to prevent resonances and further limiting effects at high frequencies. All over the bandwidth, the simulated curve shows a smooth decrease of gain. This has been designed in order to keep a relatively constant time delay and a higher gain over the cutoff frequency.

The standard deviation between predicted and measured gain in Fig. 5.11 is less than 2 dB. This is a good result, for the first realization of this TS MMIC, without any refinement iteration for modeling of passive and active elements. The difference in gain is also due to the fact that the transistors, for which we extracted the models, were taken from the previous run with a different epitaxial structure [196]. Very good agreement between simulation and measurement has been obtained in the higher frequency range. The TWA shows the highest proven bandwidth of a broad-band amplifier in a TS technology. The achieved results are at the state-of-the-art of much more mature technologies. They are compared in Table 5.1 by gain and cutoff frequency.

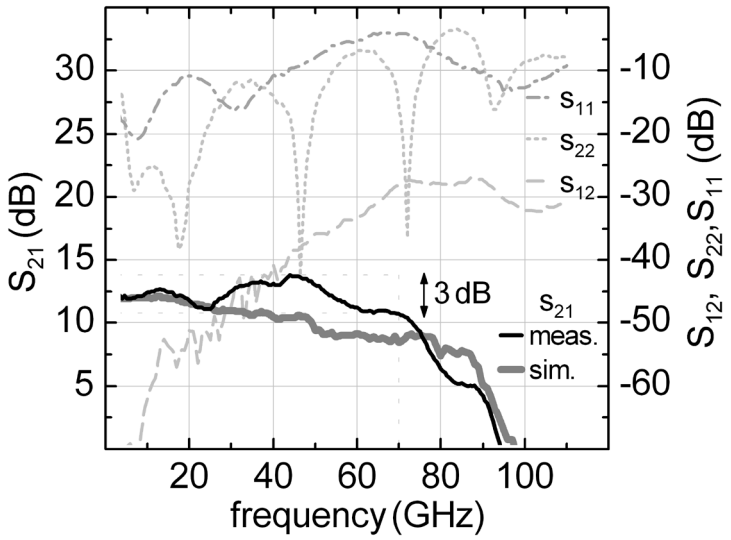

Fig. 5.11 S-parameters of the TWA in TS technology.

TABLE 5.1

STATE-OF-THE-ART INP HBT DISTRIBUTED AMPLIFIERS.

Gain (dB)	3-dB Bandwidth (GHz)	Technology	Reference
12.5	92	SHBT	[223]
14	75	SHBT	[224]
30	60	SHBT	[225]
17	70	DHBT	[223]
9.5	101	DHBT	[226]
17	110	DHBT	[227]
21	95	DHBT	[228]
11	50	TS SHBT	[229]
18	50	TS SHBT	[230]
35	42	TS DHBT	[231]
12.8	70	TS DHBT	this work

5.4 Summary

TS processing has been developed to a full MMIC compatible technology with MIM capacitors, NiCr resistors, spiral inductors and a multi-level wiring scheme. From the conception of passive elements to the realization of complete circuits, predictive modeling, and final measurements are consistent. Broadband amplifiers suitable for high bit-rate transmission systems have been designed and realized using TS DHBT technology. The TWAs demonstrate a broadband gain $G = 12.8\,\mathrm{dB}$ within the 3-dB cutoff frequency up to $f_c = 70\,\mathrm{GHz}$. This is the highest proven bandwidth of a broadband amplifier in TS technology. The TS approach offers excellent performance, relaxes design trade-offs and serves as a platform for complex 3D microintegration. The results prove the availability of the TS technology for advanced millimeter-wave circuit design.

6 Conclusions

A transferred substrate technology (TS) of InP double heterojunction bipolar transistors (DHBT) has been developed from scratch to optimize high frequency performance of the devices. The 3" wafer-level process provides lithographic access to both the front- and backside of the transistors aligned to each other. The back-to-front side alignment accuracy over the 3" wafer of better than 100 nm in the stepper line is even within the specifications of a conventional process. The resulting linear device set-up eliminates dominant transistor parasitics and relaxes design trade-offs. The scaleable device architecture is capable to further increase high frequency and power performance in the future. The essential step for gaining frontal access to both sides of the epitaxial structure is the substrate transfer. Therefore, a robust adhesive wafer bonding procedure via BCB has been realized. It yields for the first time a homogenous, crack and void-free composite matrix of functional InP DHBT epitaxy transferred in wafer-level scale. Along with the innovative DHBT set-up, the three-dimensional (3D) integration of passive elements and operational components on the transfer wafer supports functionality of the active devices and paves the way towards highly functional composite electronics, e.g. of wafer-level, 3D heterogeneous integrated circuits.

This work started TS DHBT processing at the FBH. Henceforward, major performance improvements have been accomplished. Meanwhile, the devices define the cutting edge of double side processed millimeter-wave transistors. The optimized device topology manifests in excellent device performance. Transistors of $0.8 \times 5\,\mu m^2$ emitter area feature $f_T =$ 420 GHz and $f_{max} = 450$ GHz at a breakdown voltage $BV_{CEO} > 4.5$ V. For TS DHBTs, without collector backside removal, small-signal extractions reveal a 50% higher collector – base capacitance C_{BC}. Within state-of-the-art high-speed HBTs, the TS devices demonstrate highest power handling for optimal biasing, while not falling short of RF performance. Other HBTs of comparable emitter width show significantly lower f_T and f_{max}. The more than six-fold increase in current density to 18 mA/μm^2 compensates the limitation of previously reported TS HBTs as compared to conventional ones and is an important contribution to improved high frequency and power performance. The transistors of $0.8 \times 5\,\mu m^2$ emitter area combine very high frequency performance with saturated output power $P_{out} > 13.5$ dBm at 77 GHz and DC power handling over 100 mW, but also maintain a substantial scaling potential to enhance high-speed operation. To the author's knowledge, these are record

values for HBTs with an f_T and f_{max} over 400 GHz. The straightforward device set-up of multi-finger TS DHBTs enables parallel sequencing of the basic transistor cell. The compact layout simplifies wiring and avoids additional interconnection parasitic while scaling up the transistor for millimeter-wave power operation. First multi-finger TS DHBTs of $3\times 0.8\times 9\,\mu m^2$ emitter area show an f_T and f_{max} over 340 GHz at I_C = 100 mA and V_{CE} = 1.6 V. No current collapse is observed in the biasing range up to I_C = 135 mA (6.25 mA/μm^2) and V_{CE} = 2 V. Consistent small- and large-signal transistor modeling, together with high yield and homogeneous device characteristics over the 3" wafer have been demonstrated and provide a promising tool kit for high-speed circuit design.

TS processing has been developed to a full MMIC compatible technology. A complete set of MIM capacitors, NiCr resistors, spiral inductors and a multi-level wiring scheme is provided. Precise models of the passive elements are required for reliable circuit design. Thus, electro-magnetic simulations of the passive elements have been performed to optimize them and investigate parasitic effects at intended operating frequencies. Their equivalent circuit models have been derived in ADS software for circuit design and are validated by test structures. Predictive simulation and modeling are consistent with final measurements. Together with the transistor models, they have been used as design kit for circuit simulation.

Broadband amplifiers are building blocks in high bit-rate and high frequency transmission chains. For these applications, it is a key issue to combine high frequency performance and power capabilities with adequate yield. Traveling-wave amplifiers (TWA) have been designed and realized using TS DHBT technology. They are distinctive demonstrators to evaluate a technology in terms of performance, uniformity and yield. The realized TWAs show the ability of the TS technology to meet these requirements. They demonstrate a broadband gain G = 12.8 dB within a 3-dB cutoff frequency up to f_c = 70 GHz. This is the highest proven bandwidth of a broadband amplifier in a transferred substrate technology. The TS approach offers excellent performance, relaxes design trade-offs and serves as a technology platform for complex 3D microintegration. The presented results prove the availability of the TS technology for advanced millimeter-wave circuit design.

7 Future Work

Signal currents in DHBTs are generated by modulating the electron flow through depletion regions. The resulting displacement currents are coupled to the periphery via metal – semiconductor contacts. Device bandwidth is thus determined by depletion layer transit times and capacitances, by bulk and contact resistivities, and by current handling capabilities as well as device heating. Consequently, bandwidth is increased by lithographic scaling of junction dimensions, thinning of epitaxial layers and by reducing ohmic as well as thermal resistances, according to the guidelines in section 2.6. Further challenges of vertical and lateral down scaling are yield and reliability issues as well as transistor junction passivation to handle the increasing relevance of surface effects on leakage currents and breakdown. An outline of technological measures towards THz performance (10^{12} Hz) of TS DHBTs for millimeter and sub-millimeter-wave application is given below.

In principle, modern electron beam lithography is able to shrink transistor minimum feature size below 100 nm at adequate back-to-front side alignment accuracy [122]. But with shrinking device dimensions process yield, contact resistances and surface passivation become critical aspects of device design. Wet etch mesa undercut of deep submicron transistors is critical especially at the ends of emitter and collector fingers, due to anisotropic etch rates. Mesa formation by ICP-RIE minimizes lateral mesa undercut, but has to be traded off with RIE damage of epitaxy. Dielectric sidewall spacer to separate base and emitter contacts can be formed by conformal deposition over-top the emitter metal and subsequent anisotropic dry etch removal. The procedure is similar to standard Si process schemes. It enables self-aligned base contacts independent of emitter mesa height or undercut [232]. This allows for extended lateral and vertical emitter scaling as well as for increased base metal thickness to reduce line parasitics. Lift-off free metallization schemes are able to improve device scalability into deep submicron dimensions at high yield either by subtractive ion milling [233] or additive electroplating [87]. In addition, contact surfaces do not face litho-graphic processing in advance. Thus, surface preparation of emitter, base and collector is no longer limited by the chemical stability of photoresists. This enables rigorous surface treatment imme-diately before the metallization to improved contact resistances by a factor of 7 – 20 [193], [84].

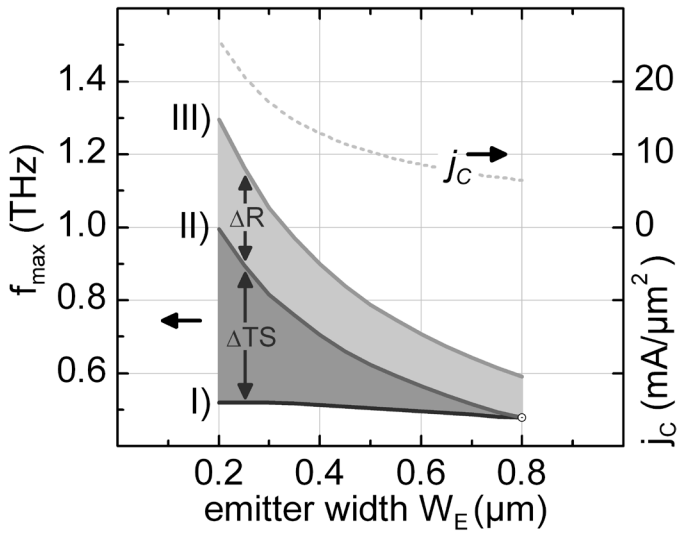

Fig. 7.1 Transistor scaling scenarios, based on TS DHBT results of section 4.6.1, I) without adaption of the collector – representing conventional DHBT scaling behavior II) with adaption of the collector width – demonstrating the TS DHBT scaling potential III) with adaption of the collector width and optimized contact resistivities, together with the respective current density j_C.

Performance improvements of f_{max} are projected in Fig. 7.1, based on the TS DHBT model of section 4.6.1. Formulas derived in section 2.4 account for the geometrical dependence of equivalent circuit parameters. Three scenarios are developed from the starting point of the realized TS DHBTs. Transistor currents and epitaxial parameters are held constant. Feasibility of increasing current density j_C, while scaling emitter width W_E from 0.8 to 0.2 µm, is supported by the 18 mA/µm^2 already demonstrated for 0.8×5 µm^2 emitter TS DHBTs in section 4.2. First, the emitter width is scaled down while the 1 µm-wide collector as well as all contact resistivities $\rho_{E,B,C}$ are held constant. The scaling behavior corresponds most likely to that of conventional state-of-the-art DHBTs. Second, emitter and collector width of the TS DHBT are scaled down simultaneously and thus to the full extent the collector–base capacitance C_{BC}. The third scenario is analog to the second. In addition, it incorporates reported process modules for improved contact resistivities. The contact optimizations alone yield a more than 100 GHz improvement in f_{max}. The overall potential of improving f_{max} open up considerable headroom to also increase f_T by vertical scaling and qualify TS DHBTs for sub-millimeter-wave application. Conventional HBTs of Fig. 4.10 on page 67 lack this perspective. They are already at the 0.3 µm scaling node and beyond, but results are comparable to today's 0.8 µm-TS DHBT technology.

Appendix

A. Process Flow

Front Side Processes:

1) Emitter Contact (E1)
2) Emitter Mesa (E2)
3) Base Metallization (B1)
4) Base Pad Metallization (BP)
5) Passivation I (P1)
6) Ground Metallization (Gd)
7) AlN Wafer (AlN)
8) Wafer Bonding (WB)

Backside Processes:

9) InP Substrate Removal & Opening of the Alignment Marks (SR)
10) Collector Metallization (K1) & Collector Mesa (K2)
11) Passivation II (P2)
12) Vias I (V1)
13) Electroplating I (G1)
14) NiCr Resistors (NiCr)
15) Passivation III (P3)
16) Vias II (V2)
17) Capacitors (C)
18) Electroplating II (G2)

Front Side Processes:

1) Emitter Contact (E1)

E1 Control	macroscopic & microscopic inspection				
E1 Cleaning	rinse dryer				
E1 Bake Out	dehydration bake (200 °C), 30 min; cool down				
E1 Photoresist	AZ 5214 (d = 1.7 µm); 500 rpm, 2 s; 3000 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 30 s				
E1 Stepper Expos.	i-line, 500 mW/cm^2				
	reticle	entry (first)	time	focus	
Structure			70 ms		
Wafer No.			"		
Shot No. vert./hor.			"		
E1 IRB	hot plate (115 °C), 90 s; cool plate (20 °C), 30 s				
E1 Flood Expos.	i-line, 500 mW/cm^2				
	reticle	entry	time	focus	
			280 ms		
E1 Development	MF 86 MX, 60 s; H_2O rinse, 60 s				
E1 O_2-Plasma	50 W, 15 Pa, 60 s				
E1 Oxid Etch	HCl : H_2O = 1 : 10, RT, 15 s; H_2O rinse 2× 30 s				
E1 Metal	Ti/Pt/Au, 25/40/630 nm				
E1 Lift Off	NMP, IPA, H_2O				

2) Emitter Mesa (E2)

E2 Cleaning	H_2O rinse; hot plate (145 °C), 15 min; cool down				self-aligned,
E2 Photoresist	AZ 1518 (d = 2.0 µm); 500 rpm, 2 s, 3500 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 15 s				lithography optional
E2 Stepper Expos.					
	reticle	entry	time	focus	
Structure			150 ms		
E2 PEB Develop.	hot plate (115 °C), 60 s; cool plate (20 °C), 30 s; MF 86 MX, 60 s; H_2O rinse, 60 s				
E2 O_2-Plasma	50 W, 15 Pa, 60 s				
E2 Post Bake	hot plate (115 °C), 10 min; cool down				
E2 InGaAs Mesa Etch of Emitter Cap	H_2SO_4 : H_2O_2 : H_2O = 1 : 8 : 500, RT, low lit; H_2O rinse 2× 120 s				
E2 InP Mesa Etch of Emitter	HCl : H_3PO_4 = 1 : 10, RT, low lit; H_2O rinse 2× 120 s				
E2 Lift	NMP, IPA, H_2O				

3) Base Metallization (B1)

B1 Cleaning	H_2O rinse; hot plate (145 °C), 15 min; cool down				
B1 Photoresist	AZ 5214 (d = 1.4 µm); 500 rpm, 2 s; 4000 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 30 s				
B1 Stepper Expos.					
	reticle	entry	time	focus	
Structure			50 ms		
Bond Marks			"		
B1 IRB	hot plate (115 °C), 90 s; cool plate (20 °C), 30 s				
B1 Flood Expos.					
	reticle	entry	time	focus	
			200 ms		
B1 Development	MF 86 MX, 45 s; H_2O rinse, 60 s				
B1 Oxid Etch	HCl : H_2O = 1 : 10, RT, 15 s; H_2O rinse 2× 30 s				
B1 Metal	Pt/Ti/Pt/Au, 10/15/15/70 nm				
B1 Lift Off	NMP, IPA, H_2O				

4) Base Pad Metallization (BP)

BP Cleaning	H_2O rinse; hot plate (145 °C), 15 min; cool down				
BP Photoresist	AZ 5214 (d = 1.4 µm); 500 rpm, 2 s; 4000 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 30 s				
BP Stepper Expos.					
	reticle	entry	time	focus	
Structure			80 ms		
BP IRB	hot plate (115 °C), 90 s; cool plate (20 °C), 30 s				
BP Flood Expos.					
	reticle	entry	time	focus	
			180 ms		
BP Development	MF 86 MX, 45 s; H_2O rinse, 60 s				
BP O_2-Plasma	50 W, 15 Pa, 60 s				
BP Metal	Ti/Au/Ti, 20/260/20 nm				
BP Lift Off	NMP, IPA, H_2O				

5) Passivation I (P1)

P1 Oxid Etch	H_2SO_4 : H_2O = 1 : 10, RT, 10 s; H_2O rinse 2× 30 s				
P1 Adh. Promoter	AP3000, 500 rpm, 5 s; 5000 rpm, 20 s; hot plate (150 °C), 3 min; cool down				
P1 BCB	Cyclotene 3022-35 (d = 1.5 µm); acc. 100 rpm/s, 3000 rpm, 60 s				
P1 Hard Cure	N_2-oven: from 50 °C to 240 °C in 30 min; 90 min at 240 °C				
P1 Etch Back_1	1) RIE: SF_6 (1 sccm), O_2 (9 sccm), 100 W, 5 Pa, (BCB); 2) RIE: SF_6 (3 sccm), O_2 (7 sccm), 100 W, 1 Pa, (BCB)				self-aligned BCB on emitter-base jct.
P1 Tie Layer	PECVD, SiN_x 100 nm				encapsulation
P1 Adh. Promoter	AP3000, 500 rpm, 5 s; 5000 rpm, 20 s; hot plate (150 °C), 3 min; cool down				
P1 BCB	Cyclotene 3022-35 (d = 2.6 µm); acc. 100 rpm/s, 1000 rpm, 60 s				
P1 Hard Cure	N_2-oven: from 50 °C to 240 °C in 30 min; 90 min at 240 °C				
P1 Photoresist	AZ 1518 (d = 2.8 µm); 500 rpm, 2 s; 2000 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 30 s				
P1 Stepper Expos.					patterned BCB finally levels with ground metal
	reticle	entry	time	focus	
			300 ms		
P1 PEB Develop.	hot plate (115 °C), 60 s; cool plate (20 °C), 30 s; MF 86 MX, 60 s, H_2O rinse, 60 s				
P1 BCB Etch back	1) RIE: SF_6 (1 sccm), O_2 (9 sccm), 100 W, 5 Pa, (BCB); 2) RIE: SF_6 (2 sccm), 50 W, 1 Pa, (SiN_x of emitter metal); 3) RIE: O_2 (10 sccm), 50 W, 30 Pa, 1 min, (resist)				to the top of the emitter metal
P1 Lift	H_2O, NMP, IPA, H_2O				

6) Ground Metallization (Gd)

Gd Cleaning	H_2O rinse; hot plate (145 °C), 15 min; cool down				
Gd Photoresist	AZ 5214 (d = 3.2 µm); 500 rpm, 2 s; 1000 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 30 s				
Gd Stepper Expos.					
	reticle	entry	time	focus	
Structure			100 ms		
Gd IRB	hot plate (115 °C), 90 s; cool plate (20 °C), 30 s				
Gd Flood Expos.					
	reticle	entry	time	focus	
			500 ms		
Gd Development	MF 86 MX, 60 s; H_2O rinse, 60 s				
Gd O_2-Plasma	50 W, 15 Pa, 60 s				
Gd Oxid Etch	HCl : H_2O = 1 : 10, RT, 15 s; H_2O rinse 2× 30 s				
Gd Metal	Ti/Pt/Au/Ti, 20/60/900/20 nm				
Gd Lift Off	NMP, IPA, H_2O				

7) AlN Wafer (AlN)

ALN Control	macroscopic & microscopic inspection of front side (US)				
ALN Photoresist	AZ 1518 (d = 2.8 µm); 500 rpm, 2 s; 2000 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 30 s				
ALN Post Bake	hot plate (140 °C), 5 min; cool down (handle wafer after post bake according to EJ orientation)				
ALN Control	macroscopic & microscopic inspection of backside (EJ)				
ALN O_2-Plasma	50 W, 15 Pa, 5 min				
ALN Photoresist	AZ 5214 (d = 1.4 µm); 500 rpm, 2 s; 4000 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 30 s				
ALN Stepper Exp.					alignment marks for wafer bonding on the backside of 3" AlN substrate
	reticle	entry	time	focus	
Structure			50 ms		
Bond Marks			"		
ALN IRB	hot plate (115 °C), 90 s; cool plate 2 min				
ALN Flood Exp.	reticle	entry	time	focus	
			170 ms		
ALN Develop.	MF 86 MX, 45 s; H_2O rinse, 60 s				
ALN O_2-Plasma	50 W, 15 Pa, 60 s				
ALN Metal	Ti/Au: 30/50 nm (wafer bond alignment marks)				
ALN Lift Off	NMP, IPA, H_2O (handle wafer after lift off according to US orientation)				front- and back-side resist is lifted

8) Wafer Bonding (WB)

InP wafer

WB Cleaning	H_2O rinse; hot plate (145 °C), 15 min; cool down	
WB Tie Layer	PECVD, SiN_x 40 nm	
WB Adh. Promoter	AP3000, 500 rpm, 5 s; 5000 rpm, 20 s; hot plate (150 °C), 3 min; cool down	
WB BCB on InP	Cyclotene 3022-35 (d = 2.6 µm); acc.100 rpm/s, 1000 rpm, 60 s	
WB Bake Out	hot plate (95 °C), 5 min; cool down	

AlN substrate

WB SiN_x Tie Layer	sputter Ar (40 sccm), N_2 (4 sccm), 30 W, 5×10^{-3} mbar, 600 s; SiN_x 40 nm, 400 W, 5×10^{-3} mbar, ca 600 s	
WB Adh. Promoter	AP3000, 500 rpm, 5 s; 5000 rpm, 20 s; hot plate (150 °C), 3 min; cool down	
WB BCB on AlN	Cyclotene 3022-35 (d = 1 µm); acc.100 rpm/s, 6000 rpm, 60 s	
WB Bake Out	hot plate (95 °C), 5 min; cool down	

Wafer Bonding	EVG-420 wafer bonding aligner; EVG-501 wafer bonder, F_{max}= 550 N, T_{max}=240 °C	

Backside Processes:

9) InP Substrate Removal & Opening of the Stepper Alignment Marks (SR)

Substrate Removal	HCl (37%), 40 °C, ~20 min; H_2O rinse				phosphine!
SR Cleaning	H_2O rinse; hot plate (145 °C), 15 min; cool down				
SR Photoresist	AZ 1518 (d = 2.0 µm); 500 rpm, 2 s; 3500 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 30 s				
SR Contact Litho.	EV-420, i-line, 4.3 mW/cm^2				
	reticle	entry	time	focus	
Structure			10.5 s		
SR PEB Develop.	hot plate (115 °C), 60 s; cool plate (20 °C), 30 s; MF 86 MX, 60 s; H_2O rinse, 60 s				
SR O_2-Plasma	50 W, 15 Pa, 60 s				
SR Post Bake	hot plate (115 °C), 10 min; cool down				
SR Mesa Etch	A) H_2SO_4 : H_2O_2 : H_2O = 1 : 1 : 10, RT; H_2O rinse 2× 30 s, B) HCl : H_2O = 1 : 1, RT; H_2O rinse 2× 60 s				iterative etches through epitaxy
SR Lift	NMP, IPA, H_2O				

10) Collector Metallization (K1) & Collector Mesa (K2)

K1 Etch Stop I (InGaAs Removal)	H_2SO_4 : H_2O_2 : H_2O = 1 : 8 : 500, RT; H_2O rinse 2× 60 s				
K1 Etch Stop II (InP Removal)	HCl : H_3PO_4 = 1 : 10, RT; H_2O rinse 2× 120 s				
K1 Cleaning	H_2O rinse; hot plate (145 °C), 15 min; cool down				
K1 Photoresist	AZ 5214 (d = 2.2 µm); 500 rpm, 2 s; 2000 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 30 s				
K1 Stepper Expos.					
	reticle	entry	time	focus	
Structure			65 ms		
Shot No. vert./hor.			"		
K1 IRB	hot plate (115 °C), 90 s; cool plate (20 °C), 30 s				
K1 Flood Expos.					
	reticle	entry	time	focus	
			430 ms		
K1 Development	MF 86 MX, 45 s; H_2O rinse, 60 s				
K1 O_2-Plasma	50 W, 15 Pa, 60 s				
K1 Oxid Etch	HCl : H_2O = 1 : 10, RT, 15 s; H_2O rinse 2× 30 s				
K1 Metal	Ti/Pt/Au, 25/40/835 nm				
K1 Lift Off	NMP, IPA, H_2O				

K2 Mesa Etch InGaAs Subcol.	H_2SO_4 : H_2O_2 : H_2O = 1 : 8 : 500, RT; H_2O rinse 2x 120 s	self-aligned, lithography
K2 Mesa Etch InP Collector	HCl : H_3PO_4 = 1 : 10, RT; H_2O rinse 2x 120 s	optional

11) Passivation II (P2)

P2 Oxid Etch	H_2SO_4 : H_2O = 1 : 10, RT, 10 s; H_2O rinse 2× 30 s				
P2 Adh. Promoter	AP3000, 500 rpm, 5 s; 5000 rpm, 20 s; hot plate (150 °C), 3 min; cool down				
P2 BCB	Cyclotene 3022-35 (d = 1.5 µm); acc. 100 rpm/s, 3000 rpm, 60 s				
P2 Hard Cure	N_2-oven: from 50 °C to 240 °C in 30 min; 90 min at 240 °C				
P2 Etch Back_1	RIE: SF_6 (1 sccm), O_2 (9 sccm), 100 W, 5 Pa, (BCB)				
P2 Photoresist	AZ 1518 (d = 2.0 µm); 500 rpm, 2 s; 3500 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 30 s				
P2 Stepper Expos.					
	reticle	entry	time	focus	
Structure			90 ms		
P2 PEB Develop.	hot plate (115 °C), 60 s; cool plate (20 °C), 30 s; MF 86 MX, 45 s; H_2O rinse, 60 s				
P2 Etch Back_2	1) SF_6 (3 sccm), O_2 (7 sccm), 100 W, 1 Pa, (BCB); 2) RIE: BCl_3 (20 sccm), Ar (10 sccm), 85 W, 1 Pa, (epitaxy); 3) RIE: SF_6 (1 sccm), O_2 (9 sccm), 100 W, 5 Pa, 1 min, (resist)				
P2 Lift	H_2O, NMP, IPA, H_2O				
P2 Bake Out	hot plate (145 °C), 15 min				
P2 Tie Layer	PECVD, SiN_x 100 nm				encapsulation
P2 Adh. Promoter	AP3000, 500 rpm, 5 s; 5000 rpm, 20 s; hot plate (145 °C), 3 min; cool down				
P2 BCB	Cyclotene 3022-35 (d = 2.6 µm); acc. 100 rpm/s, 1000 rpm, 60 s				
P2 Hard Cure	N_2-oven: from 50 °C to 240 °C in 30 min; 90 min at 240 °C				
P2 BCB Etch Back	1) RIE: SF_6 (1 sccm), O_2 (9 sccm), 100 W, 5 Pa (BCB); 2) RIE: SF_6 (2 sccm), 50 W, 1 Pa, (SiN_x);				

12) Vias I (V1)

V1 Cleaning	H_2O rinse; hot plate (145 °C), 15 min; cool down				
V1 Photoresist	AZ 5214 (d = 1.4 µm); 500 rpm, 2 s; 4000 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 30 s				
V1 Stepper Expos.					
	reticle	entry	time	focus	
Structure			80 ms		
V1 IRB	hot plate (115 °C), 90 s; cool plate (20 °C), 30 s				
V1 Flood Expos.					
	reticle	entry	time	focus	
			240 ms		
V1 Development	MF 86 MX, 45 s; H_2O rinse, 60 s				
V1 O_2-Plasma	50 W, 15 Pa, 60 s				
V1 Metal	Al: 500 nm				
V1 Lift Off	NMP, IPA, H_2O				
V1 Via Etch	ICP: SF_6 (9 sccm), O_2 (50 sccm), 0.3 Pa, (BCB)				to AlN substrate
V1 Mask Removal	KOH (50%) : H_2O = 1 : 10, RT, ~135 s +15 s; H_2O rinse 2× 120 s				

13) Electroplating I (G1)

G1 O_2-Plasma	50 W, 15 Pa, 60 s				
G1 Plating base	TiW/Au/TiW, 30/70/30 nm				
G1 Photoresist	AZ nLof 2035 (d = 2 µm); 2300 rpm, 60 s, gyrset; hot plate (110 °C), 60 s; cool plate (20 °C), 30 s				
G1 Stepper Expos.					
	reticle	entry	time	focus	
Structure			80 ms		
G1 PEB Develop.	hot plate (110 °C), 60 s; cool plate (20 °C), 30 s; MF 86 MX, 120 s; H_2O rinse, 60 s				
G1 Post Bake	hot plate (115 °C), 15 min; cool down				
G1 O_2-Plasma	50 W, 15 Pa, 120 s				
G1 TiW Etch_1	TiW etch (30 nm), H_2O_2 (30%), 45 °C; H_2O rinse 2× 60 s				
G1 Electroplating	Au: 1.5 µm				
G1 Lift	NMP, IPA, H_2O				
G1 TiW Etch_2	TiW etch (30 nm), H_2O_2 (30%), 45 °C; H_2O rinse 2× 60 s				
G1 Au Etch	Au-Stripper : H_2O = 1 : 7, RT; H_2O rinse 2× 180 s				
G1 TiW Etch_3	TiW etch (30 nm), H_2O_2 (30%), 45 °C; H_2O rinse 2× 180 s				

14) NiCr Resistors (NiCr)

NiCr Cleaning	H_2O rinse; hot plate (145 °C), 15 min; cool down				
NiCr Photoresist	AZ nLof 2035 (d = 2 µm); 2300 rpm, 60 s, gyrset; hot plate (110 °C), 60 s; cool plate (20 °C), 30 s				
NiCr Stepper Expos.					
	reticle	entry	time	focus	
Structure			90 ms		
NiCr PEB Develop.	hot plate (110 °C), 60 s; cool plate (20 °C), 30 s; MF 86 MX, 120 s; H_2O rinse, 60 s				
NiCr O_2-Plasma	50 W, 15 Pa, 60 s				
NiCr Metal	NiCr: ~10 Ω/sq				
NiCr Lift Off	NMP, IPA, H_2O				

15) Passivation III (P3)

P3 Tie Layer	PECVD, SiN_x 40 nm	
P3 Adh. Promoter	AP3000, 500 rpm, 5 s; 5000 rpm, 20 s; hot plate (150 °C), 3 min; cool down	
P3 BCB	Cyclotene 3022-35 (d = 2.6 µm); acc. 100 rpm/s, 1000 rpm, 60 s	
P3 Hard Cure	N_2-oven: from 50 °C to 240 °C in 30 min; 90 min at 240 °C	
P3 BCB	Cyclotene 3022-35 (d = 1.5 µm); acc. 100 rpm/s, 3000 rpm, 60 s	
P3 Hard Cure	N_2-oven: from 50 °C to 240 °C in 30 min; 180 min at 240 °C	

16) Vias II (V2)

V2 Cleaning	H_2O rinse; hot plate (145 °C), 15 min; cool down				
V2 Photoresist	AZ nLof 2035 (d = 4.5 µm); 2000 rpm, 60 s; hot plate (110 °C), 60 s; cool plate (20 °C), 30 s				
V2 Stepper Expos.					
	reticle	entry	time	focus	
			110 ms		
V2 PEB Develop.	hot plate (110 °C), 60 s; cool plate (20 °C), 30 s; MF 86 MX, 90 s; H_2O rinse, 60 s				
V2 BCB Etch Back	ICP: SF_6 (9 sccm), O_2 (50 sccm), 0.3 Pa, (BCB)				
V2 Lift	NMP, IPA, H_2O				

17) Capacitors (C)

C Cap SiN_x	PECVD, SiN_x 100 nm				
C Photoresist	HMDS, AZ 1518 (d = 2.0 µm); 500 rpm, 2 s, 3500 rpm, 60 s; hot plate (95 °C), 60 s; cool plate (20 °C), 15 s				
C Stepper Expos.					
	reticle	entry	time	focus	
Structure			800 ms		
C PEB Develop.	hot plate (115 °C), 60 s; cool plate (20 °C), 30 s; MF 86 MX, 90 s; H_2O rinse, 60 s				
C Etch back	1) RIE: SF_6 (2 sccm), 50 W, 1 Pa, (SiN_x); 2) RIE: O_2 (10 sccm), 50 W, 30 Pa, 1 min, (resist)				
C Lift	NMP, IPA, H_2O				

18) Electroplating II (G2)

G2 O_2-Plasma	50 W, 15 Pa, 60 s				
G2 Plating base	TiW/Au/TiW, 30/70/30 nm				
G2 Photoresist	AZ nLof 2035 (d = 5.7 µm); 1250 rpm, 60 s; hot plate (110 °C), 60 s; cool plate (20 °C), 30 s				
G2 Stepper Expos.					
	reticle	entry	time	focus	
Structure			700 ms		
G2 PEB Develop.	hot plate (110 °C), 60 s; cool plate (20 °C), 30 s; MF 86 MX, 120 s; H_2O rinse, 60 s				
G2 Post Bake	hot plate (115 °C), 15 min; cool down				
G2 O_2-Plasma	50 W, 15 Pa, 120 s				
G2 TiW Etch_1	TiW etch (30 nm), H_2O_2 (30%), 45 °C; H_2O rinse 2× 60 s				
G2 Electroplating	Au: 4 µm				
G2 Lift	NMP, IPA, H_2O				
G2 TiW Etch_2	TiW etch (30 nm), H_2O_2 (30%), 45 °C; H_2O rinse 2× 60 s				
G2 Au Etch	Au-Stripper : H_2O = 1 : 7, RT; H_2O rinse 2× 180 s				
G2 TiW Etch_3	TiW etch (30 nm), H_2O_2 (30%), 45 °C; H_2O rinse 2× 180 s				

B. Acronyms

3D	three-dimensional
As	arsenic
ADS	advanced design system software (Agilent)
Al	aluminum
AlN	aluminum nitride (ceramic)
Au	gold
BCB	divinylsiloxane bisbenzocyclobutene polymer
DC	direct current, $f = 0\,\mathrm{Hz}$
DHBT	double heterojunction bipolar transistor
FBH	Ferdinand-Braun-Institut für Höchstfrequenztechnik
FIB	focused ion beam
Ga	gallium
GaN	gallium nitride
GaAs	gallium arsenide
Ge	germanium
GHz	gigahertz
$\lvert h_{21} \rvert^2$	short-circuit current gain
H_2O_2	hydrogen peroxide
H_2SO_4	sulfuric acid
H_3PO_4	phosphoric acid
HBT	heterojunction bipolar transistor
HCl	hydrochloric acid
HEMT	high electron mobility transistor
ICP	inductive coupled plasma
In	indium
InGaAs	indium gallium arsenide
InP	indium phosphide
IPA	isopropyl alcohol
IRB	image reversal bake
ITRS	international technology roadmap for semiconductors

KOH	potassium hydroxide
LRM$^+$	advanced line-reflect-match calibration technique
MS	microstrip
MBE	molecular beam epitaxy
MIM	metal – insulator – metal (capacitor)
MMIC	monolithic microwave integrated circuit
MOCVD	metalorganic vapour phase epitaxy
MOSFET	metal-oxide-semiconductor field-effect transistor
MUG	maximum unilateral gain
NiCr	nickel chromium
NMP	1-methyl-2-pyrrolidone
PCM	process control monitoring (topologies)
Pd	palladium
PEB	post exposure bake
PECVD	plasma-enhanced chemical vapor deposition
PH_3	phosphine
Pt	platinum
RF	radio frequency
RIE	reactive ion etch
RT	room temperature
Sb	antimony
SHBT	single heterojunction bipolar transistor
Si	silicon
SiGe	silicon germanium
SiN_x	silicon nitride
SOI	silicon on insulator
Ti	titanium
TiW	titanium tungsten
TLM	transmission line measurements
TS	transferred substrate
TS DHBT	double heterojunction bipolar transistor in transferred substrate technology
TWA	traveling-wave amplifier

C. Symbols

$_{(E,B,C)}$	suffix for emitter, base or collector
A_{cont}	contact area (emitter $_{(E)}$, base $_{(B)}$, collector $_{(C)}$)
A_j	junction area (emitter $_{(E)}$, base $_{(B)}$, collector $_{(C)}$)
A_{mesa}	mesa area (emitter $_{(E)}$, base $_{(B)}$, collector $_{(C)}$)
A_{pad}	base access pad area
$_B$	suffix for base
BV_{CEO}	common-emit breakdown
$_C$	suffix for collector
C_{BC}	total collector–base capacitances
$C_{BC,ex}$	extrinsic collector–base capacitance (underneath the base contacts)
$C_{BC,gap}$	interstitial collector–base capacitance between the emitter mesa and base contact
$C_{BC,in}$	intrinsic collector–base capacitance (underneath the emitter mesa)
$C_{BC,pad}$	collector–base capacitance of base access pad
C_{jBE}	emitter–base junction capacitance
d	thickness of emitter $_{(E)}$, base $_{(B)}$ or collector $_{(C)}$
d_{grade}	grade thickness
D_n	diffusivity of electrons
d_δ	pulse layer thickness
$_E$	suffix for emitter
$E_{(x)}$	electric field
f_c	3-dB cutoff frequency of broadband amplifier gain
f_{max}	maximum oscillation frequency
f_T	current gain cutoff frequency
G	gain of amplifier
g_m	transconductance
h_{21}	small-signal common-emitter current gain, under collector–base short-circuit
I	transistor terminal currents (collector $_{(C)}$, base $_{(B)}$, emitter $_{(E)}$)
j	current density
j_{Kirk}	current density at Kirk threshold
k	Boltzmann constant, $1.380\,6504 \cdot 10^{-23}$ J/K

L	finger length of emitter $_{(E)}$ or collector $_{(C)}$
L_t	ohmic transfer length
m_e^*	electron effective mass
$n_{(x)}$	electron density
N_A	Avogadro constant, $6.02214179 \cdot 10^{23}\,\mathrm{mol}^{-1}$
N	doping concentration (emitter $_{(E)}$, base $_{(B)}$, collector $_{(C)}$)
N_δ	sheet charge density of pulse layer
P	biasing power
p	biasing power density
P_D	dissipated power
P_{out}	saturated output power
q	elementary charge, $1.602176487 \cdot 10^{-19}\,\mathrm{C}$
$\overline{R}$	universal gas constant, $8.314\,472\,\mathrm{J/(mol\,K)} = 1.985\,8775\,\mathrm{cal/(mol\,K)} = N_A k$
R	resistance
R_B	total base resistance
$R_{B,cont}$	horizontal base contact resistance
$R_{B,gap}$	gap resistance between base contact and emitter mesa
$R_{B,in}$	intrinsic base resistance under the emitter mesa
$R_{B,pad}$	base pad charging resistance
$R_{B,vert}$	vertical base contact resistance
R_C	total collector resistance
$[RC]_{eff}$	effective charging time of the distributed collector – base network
$R_{C,cont}$	resistance of collector contact
$R_{C,mesa}$	resistance of collector mesa
R_E	total emitter resistance
$R_{E,cont}$	resistance of emitter contact
$R_{E,mesa}$	resistance of emitter mesa
$R_{i(f)}$	ohmic skin effect losses
R_{th}	thermal resistance
t	time
T	temperature
$v_{(x)}$	electron velocity

$v_{B,exit}$	base exit velocity of electrons
V_{BE}	emitter – base voltage
V_{CB}	collector – base voltage
V_{CE}	collector – emitter voltage
$V_{CE,offset}$	collector – emitter offset voltage
$W_{B,cont}$	base contact width
$W_{B,cont}^{min}$	minimum width of base contacts
$W_{B,gap}$	spacing between base contact and emitter mesa
$W_{B,tot}$	total base width
W_C	collector junction width
W_E	emitter junction width
x	geometric parameter
X_{BE}	emitter – base depletion region
β	current gain
ΔE	energy difference
ΔE_c	potential barrier in the conduction band
ΔE_v	potential barrier in the valence band
ε_0	electric constant, $8.854187817 \cdot 10^{-12}$ As/(Vm)
ε_r	relative permittivity (r = InP, $In_{0.53}Ga_{0.47}As$,…)
η	transistor ideality factor of collector $_{(C)}$ or base $_{(B)}$
θ	thermal-electric feedback coefficient
κ	thermal conductivity
μ_h	hole mobility
ρ_s	specific sheet resistivity (emitter $_{(E)}$, base $_{(B)}$, collector $_{(C)}$)
ρ_c	specific contact resistivity (emitter $_{(E)}$, base $_{(B)}$, collector $_{(C)}$)
ρ_{mesa}	mesa resistivity (emitter $_{(E)}$, collector $_{(C)}$)
τ	transit time (emitter $_{(E)}$, base $_{(B)}$, collector $_{(C)}$)
Φ_{BE}	built in potential of the emitter – base junction
Φ_{bi}	transistor junction built-in potential
Φ_{grade}	potential drop over grade
$\Phi_{setback}$	potential drop over setback

D. List of Figures

E. List of Tables

Bibliography

[1] **D. L. Woolard, E. R. Brown, M. Pepper, and M. Kemp,** *"Terahertz frequency sensing and imaging: A time of reckoning future applications,"* Proc. IEEE, vol. 93, no. 10, pp. 1722 – 1743, Oct. 2005.

[2] **L. Yujiri, M. Shoucri, and P. Moffa,** *"Passive millimeter wave imaging,"* IEEE Microwave Mag., vol. 4, no. 3, pp. 39 – 50, Sept. 2003.

[3] **M. Hägelen, G. Briese, H. Essen, T. Bertuch, P. Knott, and A. Tessmann,** *"A millimetre-wave landing aid approach for helicopters under brown-out conditions,"* Radar Conf., Rome, Italy, 26–30 May 2008, pp. 1 – 4.

[4] **M. Feng, S. C. Shen, D. C. Caruth, and J. J. Huang,** *"Device technologies for RF front-end circuits in next-generation wireless communications,"* Proc. IEEE, vol. 92, no. 2, pp. 354 – 375, Feb. 2004.

[5] **I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan,** *"Band parameters for III–V compound semiconductors and their alloys,"* J. Appl. Phys., vol. 89, no. 11, pp. 5815 – 5875, June 2001.

[6] **P. Bhattacharya,** *Properties of lattice-matched and strained indium gallium arsenide.* London: INSPEC, 1993.

[7] **H. Kroemer,** *"Heterostructure bipolar transistors and integrated circuits,"* Proc. IEEE, vol. 70, no. 1, pp. 13 – 25, Jan. 1982.

[8] **T. Ishibashi,** *"Nonequilibrium electron transport in HBTs,"* IEEE Trans. Electron Devices, vol. 48, no. 11, pp. 2595 – 2605, Nov. 2001.

[9] **T. P. Pearsall,** *Properties, processing and applications of indium phosphide.* London: INSPEC, 1999.

[10] **E. Kasper,** *Properties of strained and relaxed silicon germanium.* London: INSPEC, 1995.

[11] **M. R. Brozel and G. E. Stillman,** *Properties of gallium arsenide,* London: INSPEC, 1996.

[12] **S. Adachi,** *Properties of indium phosphide.* London: INSPEC, 1991.

[13] **S. J. Pearton, J. C. Zolper, R. J. Shul, and F. Ren,** *"GaN: Processing, defects, and devices,"* J. Appl. Phys., vol. 86, no. 1, DOI: 10.1063/1.371145, p. 58, July 1999.

[14] **International Technology Roadmap for Semiconductors (ITRS),** *"Radio frequency and analog/mixed-signal technologies for wireless communications,"* (edition 2007). [On-line], pp. 9 – 10, Available: http://www.itrs.net/Links/2007ITRS/Home2007.htm [Nov. 2008].

[15] **M. Khater, J. S. Rieh, T. Adam, A. Chinthakindi, J. Johnson, R. Krishnasamy, M. Meghelli, F. Pagette, D. Sanderson, C. Schnabel, K. T. Schonenberg, P. Smith, K. Stein, A. Striker, S. J. Jeng, D. Ahlgren, and G. Freeman,** *"SiGe HBT technology with $f_{max}/f_T = 350/300$ GHz and gate delay below 3.3 ps,"* IEEE Int. Electron Devices Meeting, San Francisco, Ca, USA, 13–15 Dec. 2004, pp. 247 – 250.

[16] **B. Heinemann, R. Barth, D. Bolze, J. Drews, P. Formanek, T. Grabolla, U. Haak, W. Hoppner, D. Knoll, K. Kopke, B. Kuck, R. Kurps, S. Marschmeyer, H. H. Richter, H. Rucker, P. Schley, D. Schmidt, W. Winkler, D. Wolansky, H. E. Wulf, and Y. Yamamoto,** *"A low-parasitic collector construction for high-speed SiGe:C HBTs,"* IEEE Int. Electron Devices Meeting, San Francisco, Ca, USA, 13–15 Dec. 2004, pp. 251 – 254.

[17] **U. K. Mishra, L. Shen, T. E. Kazior, and Y. F. Wu,** *"GaN-based RF power devices and amplifiers,"* Proc. IEEE, vol. 96, no. 2, pp. 287 – 305, Feb. 2008.

[18] **M. Higashiwaki, T. Mimura, and T. Matsui,** *"AlGaN/GaN heterostructure field-effect transistors on 4H-SiC substrates with current-gain cutoff frequency of 190 GHz,"* Appl. Phys. Express, vol. 1, pp. 021103-1 – 3, Feb. 2008.

[19] **T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra,** *"AlGaN/GaN high electron mobility transistors with InGaN back-barriers,"* IEEE Electron Device Lett., vol. 27, no. 1, pp. 13 – 15, Jan. 2006.

[20] **R. Lai, W. R. Deal, X. B. Mei, W. Yoshida, J. Lee, L. Dang, J. Wang, Y. M. Kim, P. H. Liu, V. Radisic, M. Lange, T. Gaier, L. Samoska, and A. Fung,** *"Fabrication of InP HEMT devices with extremely high F_{max},"* Indium Phosphide and Related Materials, Versailles, France, 25–29 May 2008.

[21] **A. Leuther, A. Tessmann, H. Massler, R. Lösch, M. Schlechtweg, M. Mikulla, and O. Ambacher,** *"35 nm metamorphic HEMT MMIC technology,"* Indium Phosphide and Related Materials, Versailles, France, 25–29 May 2008.

[22] **E. Lind, A. M. Crook, Z. Griffith, M. J. W. Rodwell, X. M. Fang, D. Loubychev, Y. Wu, J. M. Fastenau, and A. W. K. Liu,** *"560 GHz f_t, f_{max} InGaAs/InP DHBT in a novel dry-etched emitter process,"* IEEE Device Research Conf., Univ. of Notre Dame, South Bend, Illinois, 18–20 June 2007.

[23] **W. Snodgrass and M. Feng,** *"Nano-scale type-II InP/GaAsSb DHBTs to reach THz cutoff frequencies,"* Compound Semicond. Manuf. Technol., Chicago, Illinois, USA, 14–17 Apr. 2008.

[24] **International Technology Roadmap for Semiconductors (ITRS),** *"Process integration, devices & structures,"* (edition 2007). [On-line], pp. 6 + 15, Available: http://www.itrs.net/Links /2007ITRS/Home2007.htm [Nov. 2008].

[25] **H. S. P. Wong, K. K. Chan, and Y. Taur,** *"Self-aligned (top and bottom) double-gate MOSFET with a 25 nm thick silicon channel,"* IEEE Int. Electron Devices Meeting, Washington, DC, USA, 7–10 Dec. 1997, pp. 427 – 430.

[26] **P. M. Solomon, K. W. Guarini, Y. Zhang, K. K. Chan, E. C. Jones, G. M. Cohen, A. Krasnoperova, M. Ronay, O. Dokumaci, H. J. Hovel, J. J. Bucchignano, C. Cabral, C. Lavoie, P. M. Kozlowski, J. S. Newbury, C. P. D'Emic, R. M. Sicina, and J. Benedict,** *"Two gates are better than one [double-gate MOSFET process],"* IEEE Circuits Devices Mag., vol. 19, no. 1, pp. 48 – 62, Jan. 2003.

[27] **W. Liu,** *Handbook of III-V heterojunction bipolar transistors.* New York: Wiley, 1998.

[28] **S. Blayac, M. Riet, J. L. Benchimol, P. Berdaguer, and J. Godin,** *"Geometry effects on RF performances on InP DHBTs for ultrafast integrated circuits,"* Solid-State Device Research Conf., Bordeaux, France, 8–10 Sept. 1998, pp. 540 – 43.

[29] **W. Liu, D. Costa, and J. S. Harris,** *"Derivation of the emitter-collector transit time of heterojunction bipolar transistors,"* Solid-State Electron., vol. 35, no. 4, pp. 541–545, Apr. 1992.

[30] **K. Kurishima,** *"An analytic expression of f_{max} for HBTs,"* IEEE Trans. Electron Devices, vol. 43, no. 12, pp. 2074–2079, Dec. 1996.

[31] **M. Vaidyanathan and D. L. Pulfrey,** *"Extrapolated f_{max} of heterojunction bipolar transistors,"* IEEE Trans. Electron Devices, vol. 46, no. 2, pp. 301–309, Feb. 1999.

[32] **E. H. Rhoderick and R. H. Williams,** *Metal-semiconductor contacts.* Oxford: Clarendon Press, 1988.

[33] **M. J. W. Rodwell, M. Urteaga, T. Mathew, D. Scott, D. Mensa, Q. Lee, J. Guthrie, Y. Betser, S. C. Martin, R. P. Smith, S. Jaganathan, S. Krishnan, S. I. Long, R. Pullela, B. Agarwal, U. Bhattacharya, L. Samoska, and M. Dahlstrom,** *"Submicron scaling of HBTs,"* IEEE Trans. Electron Devices, vol. 48, no. 11, pp. 2606–2624, Nov. 2001.

[34] **J. R. Hayes, F. Capasso, R. J. Malik, A. C. Gossard, and W. Wiegmann,** *"Optimum emitter grading for heterojunction bipolar transistors,"* Appl. Phys. Lett., vol. 43, no. 10, pp. 949–951, Nov. 1983.

[35] **S. Tiwari and D. Frank,** *"Barrier and recombination effects in the base-emitter junction of heterostructure bipolar transistors,"* Appl. Phys. Lett., vol. 52, no. 12, pp. 993–995, Mar. 1988.

[36] **H. Wang and G. I. Ng,** *"Avalanche multiplication in InP/InGaAs double heterojunction bipolar transistors with composite collectors,"* IEEE Trans. Electron Devices, vol. 47 no. 6, pp. 1125–1133, June 2000.

[37] **T. Ishibashi,** *"Nonequilibrium electron transport in HBTs,"* IEEE Trans. Electron Devices, vol. 48, no. 11, pp. 2595–2605, Nov. 2001.

[38] **H. Ito, S. Yamahata, and K. Kurishima,** *"Evaluation of base transit time in ultra-thin carbon-doped base InP/InGaAs heterojunction bipolar transistors,"* Electronics Lett., vol. 32, no. 15, pp. 1413–1415, July 1996.

[39] **M. Ohkubo, J. Osabe, N. Ikeda, and T. Ninomiya,** *"Compositionally graded C-doped $In_{1-x}Ga_xAs$ base in InP/InGaAs D-HBTs grown by MOCVD with low base sheet resistance and high current gain,"* Indium Phosphide and Related Materials, Cape Cod, MA, USA, 11–15 May 1997, pp. 641–644.

[40] **D. C. Streit, A. K. Oki, D. K. Umemoto, L. T. Tran, and K. W. Kobayashi,** *"High performance HBTs with built-in base fields: exponentially graded doping vs. graded composition,"* IEEE Advanced Concepts in High Speed Semiconductor Devices and Circuits, Ithaca, NY, USA, 5–7 Aug. 1991, pp. 325–333.

[41] **K. H. Kwok,** *"Analytical expressions of base transit time for SiGe HBTs with retrograde base profiles,"* Solid-State Electronics, vol. 43, no. 2, pp. 275–283, Feb. 1999.

[42] **H. Kroemer,** *"Two integral relations pertaining to the electron transport through a bipolar transistor with a nonuniform energy gap in the base region,"* Solid-State Electronics, vol. 28, no. 11, pp. 1101–1103, Nov. 1985.

[43] **R. Teissier, J. L. Pelouard, and F. Mollot,** *"Direct measurement of ballistic electron distribution and relaxation length in InP-based heterojunction bipolar transistors using photoluminescence spectroscopy,"* Appl. Phys. Lett., vol. 72, no. 21, pp. 2730 – 2732, May 1998.

[44] **M. Dahlström,** *"Ultra high speed InP heterojunction bipolar transistors,"* Ph.D. dissertation, Royal Institute of Technology, Stockholm, Sweden, July 2003, p. 33.

[45] **M. Feng and W. Snodgrass,** *"Toward THz transistor: Pseudomorphic heterojunction bipolar transistors (PHBT),"* Int. Conf. on Infrared Millimeter Waves and Terahertz Electronics, Shanghai, China, 18–22 Sept. 2006, pp. 548 – 548.

[46] **E. Johnson,** *"Physical limitations on frequency and power parameters of transistors,"* RCA Electronic Components and Devices, Somerville, NJ, USA, Mar. 1965, vol. 13, pp. 27 – 34.

[47] **L. M. Su, N. Grote, R. Kaumanns, and H. Schroeter,** *"NpnN double-heterojunction bipolar transistor on In-GaAsP/InP,"* Appl. Phys. Lett., vol. 47, no. 1, pp. 28 – 30, July 1985.

[48] **J. Hu, X. G. Xu, J. A. H. Stotz, S. P. Watkins, A. E. Curzon, M. L. W. Thewalt, N. Matine, and C. R. Bolognesi,** *"Type II photoluminescence and conduction band offsets of GaAsSb/InGaAs and GaAsSb/InP heterostructures grown by metalorganic vapor phase epitaxy,"* Appl. Phys. Lett., vol. 73, no. 19, pp. 2799 – 2801, Nov. 1998.

[49] **C. R. Bolognesi, M. M. W. Dvorak, P. Yeo, X. G. Xu, and S. P. Watkins,** *"InP/GaAsSb/InP double HBTs: A new alternative for InP-based DHBTs,"* IEEE Trans. Electron Devices, vol. 48, no. 11, pp. 2631 – 2639, Nov. 2001.

[50] **P. Bhattacharya,** *Properties of lattice-matched and strained indium gallium arsenide.* London: INSPEC, 1993, pp. 86 – 87.

[51] **N. Matine, M. W. Dvorak, C. R. Bolognesi, X. Xu, J. Hu, S. P. Watkins, and M. L. W. Thewalt,** *"Nearly ideal InP/GaAsSb/InP double heterojunction bipolar transistors with ballistically launched collector electrons,"* Electronics Lett., vol. 34, no. 17, pp. 1700 – 1702, Aug. 1998.

[52] **S. Yamahata, K. Kurishima, H. Nakajima, T. Kobayashi, and Y. Matsuoka,** *"Ultra-high f_{max} and f_T InP/InGaAs double-heterojunction bipolar transistors with step-graded InGaAsP collector,"* IEEE Gallium Arsenide Integrated Circuit Symposium, Philadelphia, PA, USA, 16–19 Oct. 1994, pp. 345 – 348.

[53] **K. Yang, G. O. Munns, and G. I. Haddad,** *"High f_{max} InP double heterojunction bipolar transistors with chirped InGaAs/InP superlattice base-collector junction grown by CBE,"* IEEE Electron Device Lett., vol. 18, no. 11, pp. 553 – 555, Nov. 1997.

[54] **C. Nguyen, T. Liu, M. Chen, H. C. Sun, and D. Rensch,** *"AlInAs/GaInAs/InP double heterojunction bipolar transistor with a novel base-collector design for power applications,"* IEEE Electron Device Lett., vol. 17, no. 3, pp. 133 – 135, Mar. 1996.

[55] **F. Capasso, A. Y. Cho, K. Mohammed, and P. W. Foy,** *"Doping interface dipoles: Tunable heterojunction barrier heights and band-edge discontinuities by molecular beam epitaxy,"* Appl. Phys. Lett., vol. 46, no. 7, pp. 664 – 666, Apr. 1985.

[56] **H. Kroemer,** *"Heterostructure bipolar transistors: What should we build?,"* J. Vac. Sci. Technol. B, vol. 1, no. 2, pp. 126 – 130, Apr.–June 1983.

[57] **T. Ishibashi,** *"Influence of electron velocity overshoot on collector transit times of HBTs,"* IEEE Trans. Electron Devices, vol. 37, no. 9, pp. 2103 – 2105, Sept. 1990.

[58] **S. E. Laux and W. Lee,** *"Collector signal delay in the presence of velocity overshoot,"* IEEE Electron Device Lett., vol. 11, no. 4, pp. 174 – 176, Apr. 1990.

[59] **H. C. Poon, H. K. Gummel, and D. L. Scharfetter,** *"High injection in epitaxial transistors,"* IEEE Trans. Electron Devices, vol. 16, no. 5, pp. 455 – 457, May 1969.

[60] **C. T. Kirk,** *"A theory of transistor cutoff frequency (f_T) falloff at high current densities,"* IEEE Trans. Electron Devices, vol. 9, no. 2, pp. 164 – 174, Mar. 1962.

[61] **M. Dahlstrom and M. J. W. Rodwell,** *"Current density limits in InP DHBTs: Collector current spreading and effective electron velocity,"* Indium Phosphide and Related Materials, Kagoshima, Japan, 31 May – 4 June 2004, pp. 366 – 369.

[62] **A. Benvenuti, W. M. Coughrau, and M. R. Pinto,** *"A thermal-fully hydrodynamic model for semiconductor devices and applications to III-V HBT simulation,"* IEEE Trans. Electron Devices, vol. 44, no. 9, pp. 1349 – 1359, Sept. 1997.

[63] **N. Nenadovic, L. K. Nanver, and J. W. Slotboom,** *"Electrothermal limitations on the current density of high-frequency bipolar transistors,"* IEEE Trans. Electron Devices, vol. 51, no. 12, pp. 2175 – 2180, Dec. 2004.

[64] **I. Harrison, M. Dahlström, S. Krishnan, Z. Griffith, Y. M. Kim, and M. J. W. Rodwell,** *"Thermal limitations of InP HBTs in 80- and 160-Gb ICs,"* IEEE Trans. Electron Devices, vol. 51, no. 4, pp. 529 – 534, Apr. 2004.

[65] **J. C. Li, P. M. Asbeck, T. Hussain, D. Hitko, C. Fields, and M. Sokolich,** *"Effects of device design on the thermal properties of HBTs,"* Int. Symp. Comp. Semicond., San Diego, CA, USA, 25-27 Aug. 2003, pp. 138 – 143.

[66] **J. J. Liou, L. L. Liou, and C. I. Huang,** *"Analytical model for the AlGaAs/GaAs multi-emitter finger HBT including self-heating and thermal coupling effects,"* IEE Circuits, Devices and Systems, vol. 141, no. 6, pp. 469 – 475, Dec. 1994.

[67] **S. Adachi,** *Physical properties of III-V semiconductor compounds: InP, InAs, GaAs, GaP, InGaAs, and InGaAsP.* New York: Wiley, 1992, p. 55.

[68] **R. K. Willardson,** *"Semiconductors and semimetals," Physics of III-V compounds.* New York: Academic Press, 1966, p. 17.

[69] **U. Bhattacharya, M. J. Mondry, G. Hurtz, J. Guthrie, M. J. W. Rodwell, T. Liu, C. Nguyen, and D. Rensch,** *"100 GHz transferred-substrate Schottky-collector heterojunction bipolar transistor,"* Indium Phosphide and Related Materials, Schwäbisch Gmünd, Germany, 21–25 Apr. 1996, pp. 145 – 148.

[70] **T. P. Pearsall,** *Properties, processing and applications of indium phosphide.* London: INSPEC, 1999, pp. 80 + 78.

[71] **P. Bhattacharya,** *Properties of lattice-matched and strained indium gallium arsenide.* London: INSPEC, 1993, pp. 37 + 41.

[72] **F. Miyashiro, N. Iwase, A. Tsuge, F. Ueno, M. Nakahashi, and T. Takahashi,** *"High thermal conductivity aluminum nitride ceramic substrates and packages,"* IEEE Trans. Compon., Hybrids, Manuf. Technol., vol. 13, no. 2, pp. 313 – 319, June 1990.

[73] **M. W. Horn, R. B. Goodman, and M. Rothschild,** *"Plasma enhanced chemically vapor deposited thin films for microelectromechanical systems applications with tailored optical, thermal, and mechanical properties,"* J. Vac. Sci. Technol. B, vol. 17, no. 3, pp. 1045 – 1049, May 1999.

[74] http://www.dow.com/cyclotene/solution/thermprop.htm : s.n.

[75] **R. Hull,** *Properties of crystalline silicon.* London: INSPEC, 1999, pp. 153 + 165.

[76] **R. P. Arnold and D. S. Zoroglu,** *"A quantitative study of emitter ballasting,"* IEEE Trans. Electron Devices, vol. 21, no. 7, pp. 385 – 391, July 1974.

[77] **W. Liu, H. F. Chau, and E. Beam,** *"Thermal properties and thermal instabilities of InP-based heterojunction bipolar transistors,"* IEEE Trans. Electron Devices, vol. 43, no. 3, pp. 338 – 395, Mar. 1996.

[78] **L. L. Liou, B. Bayraktaroglu, and C. I. Huang,** *"Thermal runaway analysis of high power AlGaAs/GaAs heterojunction bipolar transistors,"* IEEE Advanced Concepts in High Speed Semiconductor Devices and Circuits, Ithaca, NY, USA, 2–4 Aug. 1993, pp. 468 – 77.

[79] **A. Neviani, G. Meneghesso, E. Zanoni, M. Hafizi, and C. Canali,** *"Positive temperature dependence of the electron impact ionization coefficient in $In_{0.53}Ga_{0.47}As/InP$ HBTs,"* IEEE Electron Device Lett., vol. 18, no. 12, pp. 619 – 621, Dec. 1997.

[80] **H. Wang, H. Yang, and K. Radhakrishnan,** *"Temperature-dependent breakdown behavior in InP double heterojunction bipolar transistors (DHBTs) with InGaAs/InP composite collector,"* Indium Phosphide and Related Materials, Stockholm, Sweden, 12–16 May 2002, pp. 189 – 191.

[81] **R. J. Malik, N. Chand, J. Nagle, R. W. Ryan, K. Alavi, and A. Y. Cho,** *"Temperature dependence of common-emitter I-V and collector breakdown voltage characteristics in AlGaAs/GaAs and AlInAs/GaInAs HBTs grown by MBE,"* IEEE Electron Device Lett., vol. 13, no. 11, pp. 557 – 559, Nov. 1992.

[82] **J. C. Li, T. Hussain, D. A. Hitko, P. M. Asbeck, and M. Sokolich,** *"Characterization and modeling of thermal effects in sub-micron InP DHBTs,"* IEEE Comp. Semicond. Integr. Circuit Symp., 30 Oct. – 2 Nov. 2005, pp. 65 – 68.

[83] **K. Kiziloglu, S. Thomas, F. Williams, and B. M. Paine,** *"Reliability and failure criteria for AlInAs/GaInAs/InP HBTs,"* Indium Phosphide and Related Materials, Williamsburg, VA, USA, 14–18 May 2000, pp. 294 – 297.

[84] **A. M. Crook, E. Lind, Z. Griffith, M. J. W. Rodwell, J. D. Zimmerman, A. C. Gossard, and S. R. Bank,** *"Low resistance, nonalloyed ohmic contacts to InGaAs,"* Appl. Phys. Lett., vol. 91, no. 19, pp. 192114, Nov. 2007.

[85] **E. M. Lysczek and S. E. Mohney,** *"Selective deposition of ohmic contacts to p-InGaAs by electroless plating,"* J. Electrochem. Soc., vol. 155, no. 10, pp. H699 – H702, July 2008.

[86] **G. He, J. Howard, M. Le, P. Partyka, B. Li, G. Kim, R. Hess, R. Bryie, R. Lee, S. Rustomji, J. Pepper, M. Kail, M. Helix, R. B. Elder, D. S. Jansen, N. E. Harff, J. F. Prairie, E. S. Daniel, and B. K. Gilbert,** *"Self-aligned InP DHBT with f_T and f_{max} over 300 GHz in a new manufacturable technology,"* IEEE Electron Device Lett., vol. 25, no. 8, pp. 520 – 522, Aug. 2004.

[87] **M. Urteaga, R. Pierson, P. Rowell, M. Choe, D. Mensa, and B. Brar,** *"Advanced InP DHBT process for high speed LSI circuits,"* Indium Phosphide and Related Materials, Versailles, France, 25–29 May 2008.

[88] **D. Cohen Elias, A. Gavrilov, S. Cohen, S. Kraus, A. Sayag, and D. Ritter,** *"Abrupt delta-doped InP/GaInAs/InP DHBTs with 0.45-μm-wide T-shaped emitter contacts,"* IEEE Electron Device Lett., vol. 29, no. 9, pp. 971 – 973, Sept. 2008.

[89] **M. Yanagihara, H. Sakai, Y. Ota, M. Tanabe, K. Inoue, and A. Tamura,** *"253-GHz f_{max} AlGaAs/GaAs HBT with Ni/Ti/Pt/Ti/Pt-contact and L-shaped base electrode,"* IEEE Int. Electron Devices Meeting, Washington, DC, USA, 10–13 Dec. 1995, pp. 807 – 810.

[90] **Y. Miyamoto, J. M. M. Rios, A. G. Dentai, and S. Chandrasekhar,** *"Reduction of base-collector capacitance by undercutting the collector and subcollector in GaInAs/InP DHBTs,"* IEEE Electron Device Lett., vol. 17, no. 3, pp. 97 – 99, Mar. 1996.

[91] **Y. Song and K. Yang,** *"Reduction of extrinsic base-collector capacitance in InP/InGaAs SHBTs using a new base pad design,"* Indium Phosphide and Related Materials, Stockholm, Sweden, 12–16 May 2002, pp. 165 – 168.

[92] **N. Parthasarathy, Z. Griffith, C. Kadow, U. Singisetti, M. J. W. Rodwell, X. M. Fang, D. Loubychev, Y. Wu, J. M. Fastenau, and A. W. K. Liu,** *"Collector-pedestal InGaAs/InP DHBTs fabricated in a single-growth, triple-implant process,"* IEEE Electron Device Lett., vol. 27, no. 5, pp. 313 – 316, May 2006.

[93] **J. C. Li, Z. Lao, M. Y. Chen, R. D. Rajavel, S. Thomas, S. S. Bui, B. Shi, K. V. Guinn, J. R. Duvall, D. A. Hitko, D. H. Chow, and M. Sokolich,** *"200 GHz InP DHBT technology using selectively implanted buried sub-collector (SIBS) for broadband amplifiers,"* Solid-State Electronics, vol. 51, no. 1, pp. 1 – 5, Jan. 2007.

[94] **J. I. Song, M. R. Frei, J. R. Hayes, R. Bhat, and H. M. Cox,** *"Self-aligned InAlAs/InGaAs heterojunction bipolar transistor with a buried subcollector grown by selective epitaxy,"* IEEE Electron Device Lett., vol. 15, no. 4, pp. 123 – 125, Apr. 1994.

[95] **T. Nomura, M. Ohkubo, T. Sekiguchi, and T. Nonimiya,** *"Novel InP/InGaAs D-HBTs with selective multisteps MOCVD regrowth techniques for high-speed application,"* IEEE Int. Electron Devices Meeting, Washington, DC, USA, 7–10 Dec. 1997, pp. 747 – 750.

[96] **T. Arai, Y. Harada, S. Yamagami, Y. Miyamoto, and K. Furuka,** *"C_{BC} reduction in GaInAs/InP buried metal heterojunction bipolar transistor,"* Indium Phosphide and Related Materials, Stockholm, Sweden, 12–16 May 2002, pp. 254 – 257.

[97] **T. Oka, K. Hirata, K. Ouchi, H. Uchiyama, K. Mochizuki, and T. Nakamura,** *"Small-scaled InGaP/GaAs HBTs with WSi/Ti base electrode and buried SiO_2,"* IEEE Trans. Electron Devices, vol. 45, no. 11, pp. 2276 – 2282, Nov. 1998.

[98] **H. Shin, C. Gaessler, and H. Leier,** *"Reduction of base-collector capacitance in InP/InGaAs HBTs using a novel double polyimide planarization process,"* Electron Device Lett., vol. 19, no. 8, pp. 297 – 299, Aug. 1998.

[99] **S. Yamahata, K. Kurishima, T. Kobayashi, and Y. Matsuoka,** *"InP/InGaAs collector-up heterojunction bipolar transistors fabricated using Fe-ion-implantation,"* Indium Phosphide and Related Materials, Sapporo, Japan, 9–13 May 1995, pp. 652 – 655.

[100] **H. C. Tseng and Y. Z. Ye,** *"High-performance, graded-base AlGaAs/InGaAs collector-up heterojunction bipolar transistors using a novel selective area regrowth process,"* IEEE Electron Device Lett., vol. 20, no. 6, pp. 271 – 273, June 1999.

[101] **S. J. Souri, K. Banerjee, A. Mehrotra, and K. C. Saraswat,** *"Multiple Si layer ICs: Motivation, performance analysis, and design implications,"* Design Automation Conf., Los Angeles, CA, USA, 5–9 June 2000, pp. 213 – 220.

[102] **J. C. Li, K. R. Elliott, D. S. Matthews, D. A. Hitko, D. M. Zehnder, Y. Royter, P. R. Patterson, T. Hussain, and J. F. Jensen,** *"100 GHz$^+$ gain-bandwidth differential amplifiers in a wafer scale heterogeneously integrated technology using 250 nm InP DHBTs and 130 nm CMOS,"* Comp. Semicond. Integr. Circuits Symp., Monterey, USA, 12–15 Oct. 2008, pp. 1 – 4.

[103] **U. Bhattacharya,** *"Transferred substrate heterojunction bipolar transistors,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 1996.

[104] **B. Agarwal,** *"Analog integrated circuits with AlInAs/GaInAs transferred-substrate HBTs,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 1998.

[105] **D. Mensa,** *"Improved current-gain cutoff frequency and high gain-bandwidth amplifiers in transferred-substrate HBT technology,"* Ph.D. dissertation, Univ. California, Santa Barbara, 1999.

[106] **S. Jaganathan,** *"High-resolution high-bandwidth sigma-delta ADC in the transferred-substrate HBT technology,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 2000.

[107] **S. Krishnan,** *"A continuous-time sigma-delta A-D converter in an indium phosphide-based HBT technology,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 2002.

[108] **M. Dahlström, X. M. Fang, D. Lubyshev, M. Urteaga, S. Krishnan, N. Parthasarathy, Y. M. Kim, Y. Wu, J. M. Fastenau, W. K. Liu, and M. J. W. Rodwell,** *"Wideband DHBTs using a graded carbon-doped InGaAs base,"* IEEE Electron Device Lett., vol. 24, no. 7, pp. 433 – 435, July 2003.

[109] **S. Lee, M. Urteaga, Y. Wei, Y. Kim, M. Dahlström, S. Krishnan, and M. Rodwell,** *"Ultra high f_{max} InP/InGaAs/InP transferred substrate DHBTs,"* IEEE Device Research Conf., Santa Barbara, CA, USA, 24–26 June 2002, pp. 107 – 108.

[110] **Y. Betser, D. Scott, D. Mensa, S. Jaganathan, T. Mathew, and M. J. W. Rodwell,** "InAlAs/InGaAs HBTs with simultaneously high values of F_t and F_{max} for mixed analog/digital applications," *IEEE Electron Device Lett., vol. 22, no. 2, pp. 56 – 58, Feb. 2001.*

[111] **Y. Wei,** *"Wide bandwidth power heterojunction bipolar transistors and amplifiers,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 2003, p. 111.

[112] **T. Mathew,** *"High-speed digital ICs in transferred-substrate HBT technology,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 2001, pp. 96 – 126.

[113] **Q. Lee,** *"Ultra-high bandwidth heterojunction bipolar transistors and millimeter-wave integrated circuits,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 1999, p. 54.

[114] **R. Pullela,** *"Digital integrated circuits in the transferred substrate HBT technology,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 1998, p. 21.

[115] **Z. Griffith,** *"Ultrahigh speed indium gallium arsenide/indium phosphide DHBT devices and circuits,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 2005, pp. 56 – 57.

[116] **J. R. Guthrie,** *"Metal substrate process and W-band power amplifier integrated circuits in transferred-substrate HBT technology,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 2000, p. 27.

[117] **Y. Wei,** *"Wide bandwidth power heterojunction bipolar transistors and amplifiers,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 2003, p. 107.

[118] **M. Urteaga,** *"Submicron indium phosphide-based heterojunction bipolar transistors,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 2003, pp. 35 – 37.

[119] **S. Topaloglu,** *"Process technology for high speed InP based heterojunction bipolar transistors,"* Ph.D. dissertation, Univ. Duisburg-Essen, Germany, 2006, pp. 131 – 136.

[120] **S. J. Ho,** *"Fabrication and modeling of indium gallium phosphide/gallium arsenide heterojunction bipolar transistor,"* Ph.D. dissertation, Univ. Wisconsin-Madison, USA, 2007, pp. 58 + 108 – 109.

[121] **G. Wang,** *"Enhancing RF performance of power HBTs through novel device design and operation,"* Ph.D. dissertation, Univ. Wisconsin-Madison, USA, 2007, pp. 41 – 43.

[122] **N. Wichmann, S. Bollaert, B. G. Vasallo, X. Wallart, G. Dambrine, and A. Cappy,** *"InP-based InAlAs/InGaAs double-gate transistors beyond conventional HEMT's limitations,"* European Microw. Integr. Circuits Conf., Manchester, UK, 10–13 Sept. 2006, pp. 25 – 28.

[123] **R. Dekker, M. Dumling, J. H. Fock, J. R. Haartsen, H. G. R. Maas, T. M. Michielsen, H. Pohlmann, W. Schnitt, and A. M. H. Tombeur,** *"Substrate Transfer: An enabling technology for system-in-package solutions,"* Bipolar/BiCMOS Circuits and Technol. Meeting, Maastricht, Netherlands, Oct. 2006, pp. 1 – 8.

[124] **L. K. Nanver, N. Nenadovic, V. Alessandro, H. Schellevis, H. W. van Zeijl, R. Dekker, D. B. de Mooij, V. Zieren, and J. W. Slotboom,** *"A back-wafer contacted silicon-on-glass integrated bipolar process. Part I. The conflict electrical versus thermal isolation,"* IEEE Trans. Electron Devices, vol. 51, no. 1, pp. 42 – 50, Jan. 2004.

[125] **T. Nittono, H. Ito, O. Nakajima, and T. Ishibashi,** *"Extremely low resistance non-alloyed ohmic contacts to n-GaAs using compositionally graded $In_xGa_{1-x}As$ layers,"* Jpn. J. Appl. Phys., vol. 25, no. 10, pp. L865 – L867, 1986.

[126] **S. R. Bahl, N. Moll, V. M. Robbins, H. C. Kuo, B. G. Moser, and G. E. Stillman,** *"Be diffusion in InGaAs/InP heterojunction bipolar transistors,"* IEEE Electron Device Lett., vol. 21, no. 7, pp. 332 – 334, July 2000.

[127] **D. I. Lubyshev, J. Neal, W. Z. Cai, M. Micovic, T. S. Mayer, and D. L. Miller,** *"MBE growth of near-infrared InGaAs photodetectors with carbontetrabromide as a p-type dopant,"* IEEE Int. Symp. Comp. Semicond., San Diego, CA, USA, 8–11 Sept. 1997, pp. 395 – 399.

[128] **C. D. Latham, R. Jones, S. Öberg, and P. R. Briddon,** *"Density-functional calculations of carbon doping in III-V compound semiconductors,"* Phys. Rev. B, vol. 63, no. 15, pp. 155202, 2001.

[129] **H. Ito, S. Yamahata, N. Shigekawa, and K. Kurishima,** *"Heavily carbon doped base InP/InGaAs heterojunction bipolar transistors grown by two-step metalorganic chemical vapor deposition,"* Jpn J. Appl. Phys, vol. 35, pp. 6139 – 6144, 1996.

[130] **Y. Oda, N. Watanabe, M. Uchida, K. Kurishima, and T. Kobayashi,** *"C-doped GaAsSb base HBT without hydrogen passivation grown by MOVPE,"* Journal of Crystal Growth, vol. 272, no. 1-4, pp. 700 – 705, 2004.

[131] **K. Kurishima, H. Nakajima, S. Yamahata, T. Kobayashi, and Y. Matsuoka,** *"High-performance Zn-doped-base InP/InGaAs double-heterojunction bipolar transistors grown by metalorganic vapor phase epitaxy,"* Appl. Phys. Lett., vol. 64, no. 9, pp. 1111 – 1113, Feb. 1994.

[132] **A. Stano,** *"Chemical etching characteristics of InGaAs/InP and InAlAs/InP hetero-structures,"* J. Electrochem. Soc., vol. 134, no. 2, pp. 448 – 452, Feb. 1987.

[133] **S. Adachi,** *"Wet etching of InP," Properties of indium phosphide.* London: INSPEC, 1991, pp. 337 – 343.

[134] **N. Matine, M. W. Dvorak, J. L. Pelouard, F. Pardo, and C. R. Bolognesi,** *"InP in HBTs by vertical and lateral wet etching,"* Indium Phosphide and Related Materials, Tsukuba, Japan, 11–15 May 1998, pp. 195 – 198.

[135] **Y. Matsuoka, S. Yamahata, K. Kurishima, and H. Ito,** *"Ultrahigh-speed InP/InGaAs double-heterostructure bipolar transistors and analyses of their operation,"* Jpn. J. Appl. Phys., vol. 35, part 1, no. 11, pp. 5646 – 5654, 1996.

[136] **M. Le, G. He, P. Partyka, B. Li, R. Bryie, S. Rustomji, G. Kim, R. Lee, J. Pepper, M. Helix, R. Milano, R. Elder, D. Jansen, F. Stroili, J. W. Lai, and M. Feng,** *"Self-aligned InP DHBTs for 150 GHz digital and mixed signal circuits,"* Indium Phosphide and Related Materials, Glasgow, Scotland, UK, 8–12 May 2005, pp. 325 – 330.

[137] **F. Niklaus, R. Kumar, J. J. Mc Mahon, J. Yu, J. Q. Lu, T. S. Cale, and R. J Gutmann,** *"Adhesive wafer bonding using partially cured benzocyclobutene for three-dimensional integration,"* J. Electrochem. Soc., vol. 153, no. 4, pp. G291 – G295, Feb. 2006.

[138] **E. M. J. Smeets, F. G. C. Bijnen, J. Slabbekoorn, and H. W. van Zeijl,** *"3D align overlay verification using glass wafers,"* Int. Soc. Opt. Eng., vol. 5641, pp. 152 – 162, Dec. 2004.

[139] **Y. Wei,** *"Wide bandwidth power heterojunction bipolar transistors and amplifiers,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 2003, p. 107.

[140] **T. Mathew,** *"High-speed digital ICs in transferred-substrate HBT technology,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 2001, p. 65.

[141] **M. Alexe and U. Gösele,** *Wafer bonding: applications and technology, 1st ed.* Berlin: Springer, 2004.

[142] **S. S. Iyer and A. J. Auberton-Herve,** *Silicon wafer bonding technology: for VLSI and MEMS applications.* London: Institution of Electrical Engineers, 2002.

[143] **A. Plößl and G. Kräuter,** *"Wafer direct bonding: tailoring adhesion between brittle materials,"* Materials Science and Engineering, vol. R25, pp. 1 – 88, 1999.

[144] **D. Pasquariello and K. Hjort,** *"Plasma-assisted InP-to-Si low temperature wafer bonding,"* IEEE J. Sel. Topics. Quantum Electron., vol. 8, no. 1, pp. 118 – 131, Jan. 2002.

[145] **T. Itoh, H. Okada, H. Takagi, R. Maeda, and T. Suga,** *"Room temperature vacuum sealing using surface activated bonding method,"* Int. Conf. Solid-State Sensors, Actuators and Microsystems, Munich, Germany, 8–12 June 2003, vol. 2, pp. 1828 – 1831.

[146] **M. Bruel,** *"Silicon on insulator material technology,"* Electronics Lett., vol. 31, no. 14, pp. 1201 – 1202, July 1995.

[147] **G. Wallis and D. I. Pomerantz,** *"Field assisted glass-metal sealing,"* J. Appl. Phys., vol. 40, no. 10, pp. 3946 – 3949, Sept. 1969.

[148] **J. Wei, Z. P. Wang, H. Xie, and N. F. Lan,** *"Role of bonding temperature and voltage in silicon-to-glass anodic bonding,"* IEEE Electronics Packaging Technol. Conf., Singapore, 10–12 Dec. 2002, pp. 85 – 90.

[149] **A. V. Chavan and K. D. Wise,** *"A monolithic fully-integrated vacuum-sealed CMOS pressure sensor,"* IEEE Trans. Electron Devices, vol. 49, no. 1, pp. 164 – 169, Jan. 2002.

[150] **F. Niklaus, G. Stemme, J. Q. Lu, and R. J. Gutmann,** *"Adhesive wafer bonding,"* J. Appl. Phys., vol. 99, no. 3, pp. 031101-1 – 28, Feb. 2006.

[151] **A. J. G. Strandjord, W. B. Rogers, Y. Ida, R. R. DeVeillis, S. Shiau, E. S. Moyer, D. M. Scheck, and P. E. Garron,** *"Photosensitive benzocyclobutene for stress-buffer and passivation applications,"* IEEE Electron. Compon. and Technol. Conf., New York, 18–21 May 1997, pp. 1260 – 1268.

[152] **R. Knechtel,** *"Glass frit bonding: an universal technology for wafer level encapsulation and packaging,"* Microsyst. Technol., vol. 12, no. 1-2, pp. 63 – 68, Dec. 2005.

[153] **Y. Liu, T. Cui, R. K. Sunkam, P. J. Coane, M. J. Vasile, and J. Geoettert,** *"Novel approach to form and pattern sol–gel polymethylsilsesquioxane-based spin-on glass thin and thick films,"* Sensors and Actuators B: Chemical, vol. 88, no. 1, pp. 75 – 79, Jan. 2003.

[154] **C. Lee, W. F. Huang, and J. S. Shie,** *"Wafer bonding by low-temperature soldering,"* Sensors and Actuators A: Physical, vol. 85, no. 1-3, pp. 330 – 334, Aug. 2000.

[155] **J. Kim, and C. C. Lee,** *"Fluxless wafer bonding with Sn-rich Sn–Au dual-layer structure,"* Materials Science and Engineering A, vol. 417, no. 1-2, pp. 143 – 148, Feb. 2006.

[156] **Z. Ma, G. L. Zhou, H. Morkoc, L. H. Allen, and K. C. Hsieh,** *"Solid-state reaction-mediated low-temperature bonding of GaAs and InP wafers to Si substrates,"* Appl. Phys. Lett., vol. 64, no. 6, pp. 772 – 774, Feb. 1994.

[157] **R. F. Wolffenbuttel,** *"Low-temperature intermediate Au–Si wafer bonding and eutectic or silicide bond,"* Sensors and Actuators A: Physical, vol. 62, no. 1-3, pp. 680 – 686, July 1997.

[158] **J. Kim, M. Chiao, and L. Lin,** *"Ultrasonic bonding of In/Au and Al/Al for hermetic sealing of MEMS packaging,"* IEEE Micro Electro Mech. Syst., Las Vegas, NV, USA, 20–24 Jan. 2002, pp. 415 – 418.

[159] **M. M. V. Taklo, P. Storas, K. Schjølberg-Henriksen, H. K. Hasting, and H. Jakobsen,** *"Strong, high-yield and low-temperature thermocompression silicon wafer-level bonding with gold,"* J. Micromech. Microeng., vol. 14, no. 7, pp. 884 – 890, July 2004.

[160] **K. N. Chen, S. M. Chang, A. Fan, C. S. Tan, L. C. Shen, and R. Reif,** *"Process development and bonding quality investigations of silicon layer stacking based on copper wafer bonding,"* Appl. Phys. Lett. 87, no. 3, pp. 031909, July 2005.

[161] **J. J. Mc Mahon, J. Q. Lu, and R. J. Gutmann,** *"Wafer bonding of damascene-patterned metal/adhesive redistribution layers for via-first 3D interconnect,"* IEEE Electron. Compon. and Technol. Conf., Lake Buena Vista, FL, USA, 31 May – 3 June 2005, pp. 331 – 336.

[162] **F. Niklaus, P. Enoksson, E. Kälvesten, and G. Stemme,** *"Low temperature full wafer adhesive bonding,"* J. Micromech. Microeng., vol. 11, no. 2, pp. 100 – 107, 2001.

[163] **Y. Kwon and J. Seok,** *"An evaluation process of polymeric adhesive wafer bonding for vertical system integration,"* Jpn. J. Appl. Phys., vol. 44, no. 6A, pp. 3893 – 3902, June 2005.

[164] **M. Wiemer, C. Jia, M. Toepper, and K. Hauck,** *"Wafer bonding with BCB and SU-8 for MEMS packaging,"* Electron. Systemintegration Technol. Conf., Dresden, Germany, Sept. 2006, vol. 2, pp. 1401 – 1405.

[165] **F. J. Blanco, M. Agirregabiria, J. Garcia, J. Berganzo, M. Tijero, M. T. Arroyo, J. M. Ruano, I. Aramburu, and K. Mayora,** *"Novel three-dimensional embedded SU-8 microchannels fabricated using a low temperature full wafer adhesive bonding,"* J. Micromech. Microeng., vol. 14, no. 7, pp. 1047 – 1056, July 2004.

[166] **Y. K. Kim, E. K. Kim, S. W. Kim, and B. K. Ju,** *"Low temperature epoxy bonding for wafer level MEMS packaging,"* Sensors and Actuators A: Physical, vol. 143, no. 2, pp. 323 – 328, May 2008.

[167] **C. T. Pan, H. Yang, S. C. Shen, M. C. Chou, and H. P. Chou,** *"A low-temperature wafer bonding technique using patternable materials,"* J. Micromech. Microeng., vol. 12, no. 5, pp. 611 – 615, Sept. 2002.

[168] **B. Bilenberg, T. Nielsen, B. Clausen, and A. Kristensen,** *"PMMA to SU-8 bonding for polymer based lab-on-a-chip systems with integrated optics,"* J. Micromech. Microeng., vol. 14, no. 6, pp. 814 – 818, 2004.

[169] **A. B. Frazier,** *"Low temperature IC-compatible wafer-to-wafer bonding with embedded micro channels for integrated sensing systems,"* IEEE Circuits and Systems, Rio de Janeiro, Brazil, 13–16 Aug. 1995, vol. 1, pp. 505 – 508.

[170] **H. Kim and K. Najafi,** *"Characterization of low-temperature wafer bonding using thin-film parylene,"* J. Microelectromech. Syst., vol. 14, no. 6, pp. 1347 – 1355, Dec. 2005.

[171] **K. W. Oh, A. Han, S. Bhansali, and C. H. Ahn,** *"A low-temperature bonding technique using spin-on fluorocarbon polymers to assemble microsystems,"* J. Micromech. Microeng., vol. 12, no. 2, pp. 187 – 191, Mar. 2002.

[172] **J. Q. Lu, Y. Kwon, G. Rajagopalan, M. Gupta, J. J. Mc Mahon, K. W. Lee, R. P. Kraft, J. F. Mc Donald, T. S. Cale, R. J. Gutmann, B. Xu, E. Eisenbraun, J. Castracane, and A. Kaloyeros,** *"A wafer-scale 3D IC technology platform using dielectric bonding glues and copper damascene patterned inter-wafer interconnects,"* IEEE Int. Interconnect Technol. Conf., San Francisco, USA, 3–5 June 2002, pp. 78 – 80.

[173] **S. Bhattacharya, A. Datta, J. M. Berg, and S. Gangopadhyay,** *"Studies on surface wettability of poly(dimethyl) siloxane (PDMS) and glass under oxygen-plasma treatment and correlation with bond strength,"* J. Microelectromech. Syst., vol. 14, no. 3, pp. 590 – 597, June 2005.

[174] **D. Goustouridis, K. Minoglou, S. Kolliopoulou, S. Chatzandroulis, P. Morfouli, P. Normanda, and D. Tsoukalas,** *"Low temperature wafer bonding for thin silicon film transfer,"* Sensors and Actuators A: Physical, vol. 110, no. 1-3, pp. 401 – 406, Feb. 2004.

[175] **X. Wang, J. Engel, and C. Liu,** *"Liquid crystal polymer (LCP) for MEMS: processes and applications,"* J. Micromech. Microeng., vol. 13, no. 5, pp. 628 – 633, Sept. 2003.

[176] **H. Nguyen, P. Patterson, H. Toshiyoshi, and M. C. Wu,** *"A substrate-independent wafer transfer technique for surface-micromachined devices,"* IEEE Micro Electro Mech. Syst., Miyazaki, Japan, 23–27 Jan. 2000, pp. 628 – 632.

[177] **S. F. Hahn, S. J. Martin, and M. L. Mc Kelvy,** *"Thermally induced polymerization of an arylvinylbenzocyclobutene monomer,"* Macromolecules, vol. 25, no. 5, pp. 1539 – 1545, Mar. 1992.

[178] **S. Pozder, J. Q. Lu, Y. Kwon, S. Zollner, J. Yu, J. J. Mc Mahon, T. S. Cale, K. Yu, and R. J. Gutmann,** *"Back-end compatibility of bonding and thinning processes for a wafer-level 3D interconnect technology platform,"* Int. Interconnect Technol. Conf., Burlingame, CA, USA, 7–9 June 2004, pp. 102 – 104.

[179] **Dow Chemical Company,** *"Processing procedures for CYCLOTENE 3000 series Dry Etch Resins,"* Product Information Sheet, http://www.dow.com/cyclotene/, Feb. 2005.

[180] **M. T. Bernius, D. C. Burdeaux, C. C. Fulks, P. Garrou, R. H. Heistand, and T. M. Stokich,** *"Planarization with CYCLOTENE 3022 (BCB) polymer coatings,"* Proc. of Materials Research Soc., San Francisco, 12–16 April 1993, vol. 308, p. 517. Available: http://www.dow.com/cyclotene/solution/planar.htm.

[181] **A. R. Mirza,** *"One micron precision, wafer-level aligned bonding for interconnect, MEMS and packaging applications,"* IEEE Electron. Compon. and Technol. Conf., 2000, pp. 676 – 680.

[182] **M. G. Dibbs, P. H. Townsend, T. M. Stokich, B. S. Huber, C. E. Mohler, R. H. Heistand, P. E. Garrou, G. M. Adema, M. J. Berry, and I. Turlik,** *"Cure management of benzocyclobutene dielectric for electronic applications,"* Soc. of Advanced Material Process Engineering Electronics Conf., Baltimore, MD, USA, 22–25 June 1992, pp. 1 – 10.

[183] **P. E. Garrou, R. H. Heistand, M. G. Dibbs, T. A. Manial, C. E. Mohler, T. M. Stokich, P. H. Townsend, G. M. Adema, M. J. Berry, and I. Turlik,** *"Rapid thermal curing of BCB dielectric,"* IEEE Trans. Compon., Hybrids, Manuf. Technol., vol. 16, no. 1, pp. 46 – 52, Feb. 1993.

[184] **O. Vallin, K. Jonsson, and U. Lindberg,** *"Adhesion quantification methods for wafer bonding,"* Materials Science and Engineering, vol. 50, no. 4-5, pp. 109 – 165, Dec. 2005.

[185] **H. J. Ueng, D. B. Janes, and K. J. Webb,** *"Error analysis leading to design criteria for transmission line model characterization of ohmic contacts,"* IEEE Trans. Electron Devices, vol. 48, no. 4, pp. 758 – 766, Apr. 2001.

[186] **R. Williams,** *Modern GaAs processing methods, 2nd ed.* Boston: USA, Artech House, 1990, pp. 230 – 233.

[187] **Q. Lee,** *"Ultra-high bandwidth heterojunction bipolar transistors and millimeter-wave integrated circuits,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 1999, p. 79.

[188] **T. Mathew,** *"High-speed digital ICs in transferred-substrate HBT technology,"* Ph.D. dissertation, Univ. California, Santa Barbara, USA, 2001, p. 43.

[189] **R. F. Scholz, F. Korndorfer, B. Senapati, and A. Rumiantsev,** *"Advanced technique for broadband on-wafer RF device characterization,"* Automatic RF Techniques Group (ARFTG) Conf., Fort Worth, TX, USA, 11. June 2004, pp. 83 – 90.

[190] **R. Doerner and A. Rumiantsev,** *"Verification of the wafer-level LRM+ calibration technique for GaAs applications up to 110 GHz,"* Automatic RF Techniques Group (ARFTG) Conf., Long Beach, CA, USA, 17. June 2005, pp. 15 – 19.

[191] **B. G. Vasallo, N. Wichmann, S. Bollaert, Y. Roelens, A. Cappy, T. Gonzalez, D. Pardo, and J. Mateos,** *"Comparison between the dynamic performance of double- and single-gate AlInAs/InGaAs HEMTs,"* IEEE Trans. Electron Devices, vol. 54, no. 11, pp. 2815 – 2822, Nov. 2007.

[192] **A. Fujihara, Y. Ikenaga, H. Takahashi, M. Kawanaka, and S. Tanaka,** *"High-speed InP/InGaAs DHBTs with ballistic collector launcher structure,"* IEEE Int. Electron Devices Meeting, Washington, DC, USA, 2–5 Dec. 2001, pp. 35.3.1 – 4.

[193] **Z. Griffith, E. Lind, M. J. W. Rodwell, X. M. Fang, D. Loubychev, Y. Wu, J. M. Fastenau, and A. W. K. Liu,** *"Sub-300 nm InGaAs/InP type-I DHBTs with a 150 nm collector, 30 nm base demonstrating 755 GHz f_{max} and 416 GHz f_t,"* Indium Phosphide and Related Materials, Matsue, Japan, 14–18 May 2007, pp. 403 – 406.

[194] **T. Kraemer, C. Meliani, F. J. Schmueckle, J. Wuerfl, and G. Traenkle,** *"Traveling wave amplifiers in transferred substrate InP-HBT technology,"* IEEE Trans. Microw. Theory Tech., vol. 57, no. 9, pp. 2114 – 2121, Sept. 2009.

[195] **T. Kraemer, M. Rudolph, F. J. Schmueckle, J. Wuerfl, and G. Traenkle,** *"InP DHBT process in transferred substrate technology with f_t and f_{max} over 400 GHz,"* IEEE Trans. Electron, vol. 56, no. 9, pp. 1897 – 1903, Sept. 2009.

[196] **T. Kraemer, F. Lenk, A. Maassdorf, H. J. Wuerfl, and G. Traenkle,** *"High yield transferred substrate InP DHBT,"* Indium Phosphide and Related Materials, Matsue, Japan, 14–18 May 2007, pp. 407 – 408.

[197] **T. Kraemer, S. O. Kim, F. Brunner, F. Schnieder, H. J. Wuerfl, and G. Traenkle,** *"Development of InP DHBT via transfer substrate process,"* Workshop on Compound Semicond. Devices and Integr. Circuits, Cardiff, UK, 16–18 May 2005, pp. 79 – 81.

[198] **D. W. Scott, P. C. Chang, D. Sawdai, L. Dang, J. Wang, M. Barsky, W. Phan, B. Chan, B. Oyama, A. Gutierrez-Aitken, and A. Oki,** *"Sub-micrometer InP/InGaAs heterojunction bipolar transistors with f_T = 400 GHz and f_{max} > 500 GHz,"* Indium Phosphide and Related Materials, Princeton, NJ, USA, 7–11 May 2006, pp. 100 – 103.

[199] **T. Hussain, Y. Royter, D. Hitko, M. Montes, M. Madhav, I. Milosavljevic, R. Rajavel, S. Thomas, M. Antcliffe, A. Arthur, Y. Boegeman, M. Sokolich, and P. Asbeck,** *"First demonstration of sub-0.25 µm-width emitter InP-DHBTs with > 400 GHz f_t and > 400 GHz f_{max},"* IEEE Int. Electron Devices Meeting, San Francisco, Ca, USA, 12–15 Dec. 2004, pp. 553 – 556.

[200] **D. Cohen Elias, A. Gavrilov, S. Cohen, S. Kraus, A. Sayag, and D. Ritter,** *"Abrupt delta-doped InP/GaInAs/InP DHBTs with 0.45-µm-wide T-shaped emitter contacts,"* IEEE Electron Device Lett., vol. 29, no. 9, pp. 971 – 973, Sept. 2008.

[201] **H. G. Liu, O. Ostinelli, Y. Zeng, and C. R. Bolognesi,** *"600 GHz InP/GaAsSb/InP DHBTs grown by MOCVD with a Ga(As,Sb) graded-base and $f_T \times BV_{CEO}$ > 2.5 THz-V at room temperature,"* IEEE Int. Electron Devices Meeting, Washington, DC, USA, 10–12 Dec. 2007, pp. 667 – 670.

[202] **N. G. Weimann, V. Houtsma, Y. Baeyens, J. Weiner, A. Tate, J. Frackoviak, and Y. K. Chen,** *"InP DHBT circuits for 100 Gb/s ethernet applications,"* Indium Phosphide and Related Materials, Versailles, France, 25–29 May 2008.

[203] **V. Hurm, F. Benkhelifa, R. Driad, R. Lösch, R. Makon, H. Massler, J. Rosenzweig, M. Schlechtweg, and H. Walcher,** *"InP DHBT-based distributed amplifier for 100 Gbit/s modulator driver operation,"* Electronics Lett., vol. 44, no. 12, pp. 705 – 706, June 2008.

[204] **W. Snodgrass, W. Hafez, N. Harff, and M. Feng,** *"Pseudomorphic InP/InGaAs heterojunction bipolar transistors (PHBTs) experimentally demonstrating f_T = 765 GHz at 25 °C increasing to f_T = 845 GHz at −55 °C,"* IEEE Int. Electron Devices Meeting, San Francisco, CA, USA, 11–13 Dec. 2006, pp. 1 – 4.

[205] **Y. Ohkubo, T. Matsumoto, T. Koji, Y. Amano, A. Takagi, and Y. Matsuoka,** *"High-performance self-aligned InP/InGaAs DHBTs with a passivation ledge utilizing a thin etching stop layer,"* Indium Phosphide and Related Materials, Versailles, France, 25–29 May 2008.

[206] **V. Nodjiadjim, M. Riet, A. Scavennec, P. Berdaguer, J. L. Gentner, J. Godin, P. Bove, and M. Lijadi,** *"Comparative collector design in InGaAs and GaAsSb based InP DHBTs,"* Indium Phosphide and Related Materials, Versailles, France, 25–29 May 2008.

[207] **S. Tanaka, S. Murakami, Y. Amamiya, H. Shimawaki, N. Furuhata, N. Goto, K. Honjo, Y. Ishida, Y. Saito, K. Yamamoto, M. Yajima, R. Temino, and Y. Hisada,** *"High-power, high-efficiency cell design for 26 GHz HBT power amplifier,"* IEEE MTT-S Int. Microw. Symp., San Francisco, CA, USA, 17–21 June 1996, vol. 2, pp. 843 – 846.

[208] **Y. Wei, S. Lee, P. K. Sundararajan, M. Dahlstrom, M. Urteaga, and M. Rodwell,** *"High current (100 mA) InP/InGaAs/InP DHBTs with 330 GHz f_{max},"* Indium Phosphide and Related Materials, Stockholm, Sweden, 12–16 May 2002, pp. 47 – 50.

[209] **V. Nodjiadjim, M. Riet, A. Scavennec, P. Berdaguer, O. Drisse, E. Derouin, J. Godin, P. Bove, and M. Lijadi,** *"InP/GaAsSb/InP multifinger DHBTs for power applications,"* Indium Phosphide and Related Materials, Versailles, France, 25–29 May 2008.

[210] **T. O'Sullivan, M. Urteaga, R. Pierson, and P.M. Asbeck,** *"InP HBT millimeter-wave power amplifier implemented using planar radial power combiner,"* IEEE MTT-S Int. Microw. Symp., Atlanta, GA, USA, 15–20 June 2008, pp. 293 – 296.

[211] **J. Zhi, S. Yong-Bo, C. Wei, L. Xin-Yu, X. An-Huai, and Q. Ming,** *"High current multi-finger InGaAs/InP double heterojunction bipolar transistor with the maximum oscillation frequency 253 GHz,"* Chinese Phys. Lett., vol. 25, pp. 3075 – 3078, Aug. 2008.

[212] **D. Hadziabdic and V. Krozer,** *"Power amplifier technology at microwave and millimeter-wave frequencies: an overview,"* German Microwave Conf., Hamburg-Harburg, Germany, 10–12 Mar. 2008.

[213] **W. Liu and A. Khatibzadeh,** *"The collapse of current gain in multi-finger heterojunction bipolar transistors: its substrate temperature dependence, instability criteria, and modeling,"* IEEE Trans. Electron Devices, vol. 41, no. 10, pp. 1698 – 1707, Oct. 1994.

[214] **F. Lenk and M. Rudolph,** *"New extraction algorithm for GaAs-HBTs with low intrinsic base resistance,"* IEEE MTT-S Int. Microw. Symp., Seattle, Washington, USA, 2–7 June 2002, vol. 2, pp. 725 – 728.

[215] **M. Vaidyanathan and D.L. Pulfrey,** *"Extrapolated f_{max} of heterojunction bipolar transistors,"* IEEE Trans. Electron. Devices, vol. 46, no. 2, pp. 301 – 309, Feb. 1999.

[216] **M. Rudolph,** *Introduction to modeling HBTs.* Boston, MA: Artech House, 2006.

[217] **G.M. Kull, L.W. Nagel, S.W. Lee, P. Lloyd, E.J. Prendergast, and H.K. Dirks,** *"A unified circuit model for bipolar transistors including quasi-saturation effects,"* IEEE Trans. Electron Devices, vol. 32, no. 6, pp. 1103 – 1113, June 1985.

[218] **H. Shigematsu, M. Sato, T. Hirose, and Y. Watanabe,** *"A 54-GHz distributed amplifier with 6-Vpp output for a 40-Gb/s $LiNbO_3$ modulator driver,"* IEEE J. Solid-State Circuits, vol. 37, no. 9, pp. 1100 – 1105, Sept. 2002.

[219] **C. Meliani, M. Rudolph, J. Hilsenbeck, and W. Heinrich,** *"A 40 Gbps broadband amplifier for modulator-driver applications using a GaAs HBT technology,"* Bipolar/BiCMOS Circuits and Technol. Meeting, Montreal, Canada, 13–14 Sept. 2004, pp. 281 – 284.

[220] **K. Zoschke, J. Wolf, M. Töpper, O. Ehrmann, T. Fritzsch, K. Scherpinski, H. Reichl, and F.J. Schmückle,** *"Thin film integration of passives – single components, filters, integrated passive devices,"* IEEE Electron. Compon. and Technol. Conf., Las Vegas, NV, USA, 1–4 June 2004, vol. 1, pp. 294 – 301.

[221] **T. Weiland, M. Timm, and I. Munteanu,** *"A practical guide to 3-D simulation,"* IEEE Microwave Magazine, vol. 9, no. 6, pp. 62 – 75, Dec. 2008.

[222] **M. Häfele, C. Schwörer, K. Beilenhoff, and H. Schumacher,** *"A GaAs PHEMT distributed amplifier with low group delay time variation for 40 GBit/s optical systems,"* European Microw. Integr. Circuits Conf., Munich, Germany, Oct. 2003, pp. 1091 – 1094.

[223] **Y. Baeyens, G. Georgiou, J.S. Weiner, A. Leven, V. Houtsma, P. Paschke, Q. Lee, R.F. Knopf, Y. Yang, L. Chua, C. Chen, C.T. Liu, and Y.K. Chen,** *"InP D-HBT ICs for 40-Gb/s and higher bitrate lightwave transceivers,"* IEEE J. Solid-State Circuits, vol. 37, no. 9, pp. 1152 – 1159, Sept. 2002.

[224] **E. Cohen, Y. Betser, B. Sheinman, S. Cohen, S. Sidorov, A. Gavrilov, and D. Ritter,** *"75 GHz InP HBT distributed amplifier with record figures of merit and low power dissipation,"* IEEE Trans. Electron Devices, vol. 53, no. 2, pp. 392 – 394, Feb. 2006.

[225] **K. W. Kobayashi,** *"State-of-the-art 60 GHz, 3.6 k-ohm transimpedance amplifier for 40 Gb/s and beyond,"* Radio Freq. Integr. Circuits Symp., Philadelphia, PA, 8–10 June 2003, pp. 55 – 58.

[226] **K. Schneider, R. Driad, R. E. Makon, A. Tessmann, R. Aidam, R. Quay, M. Schlechtweg, and G. Weimann,** *"InP/InGaAs-DHBT distributed amplifier MMICs exceeding 80 GHz bandwidth,"* IEEE MTT-S Int. Microw. Symp., Long Beach, CA, 12–17 June 2005, pp. 1591 – 1593.

[227] **Y. Baeyens, N. Weimann, V. Houtsma, J. Weiner, Y. Yang, J. Frackoviak, P. Roux, A. Tate, and Y. K. Chen,** *"Submicron InP D-HBT single-stage distributed amplifier with 17 dB gain and over 110 GHz bandwidth,"* IEEE MTT-S Int. Microw. Symp., San Francisco, CA, 11–16 June 2006, pp. 818 – 821.

[228] **R. Driad, R. E. Makon, V. Hurm, K. Schneider, F. Benkhelifa, R. Lösch, and J. Rosenzweig,** *"InP DHBT-based ICs for 100 Gbit/s data transmission,"* Indium Phosphide and Related Materials, Versailles, France, 25–29 May 2008.

[229] **B. Agarwal, Q. Lee, R. Pullela, D. Mensa, J. Guthrie, and M. J. W. Rodwell,** *"A transferred-substrate HBT wide-band differential amplifier to 50 GHz,"* IEEE Microw. Guided Wave Lett., vol. 8, no. 7, pp. 263 – 265, July 1998.

[230] **D. Mensa,** *"Improved current-gain cutoff frequency and high gain-bandwidth amplifiers in transferred-substrate HBT technology,"* Ph.D. dissertation, Univ. California Santa Barbara, 1999, pp. 98 – 101.

[231] **K. Krishnamurthy, J. Chow, M. J. W. Rodwell, and R. Pullela,** *"0.1–42 GHz InP DHBT distributed amplifiers with 35 dB gain and 15 dBm output,"* Electronics Lett., vol. 39, no. 22, pp. 1594 – 1595, Oct. 2003.

[232] **M. Le, G. He, R. Hess, P. Partyka, B. Li, R. Bryie, S. Rustomji, G. Kim, R. Lee, J. Pepper, M. Helix, R. Milano, R. Elder, D. Jansen, F. Stroili, J-W. Lai, and M. Feng,** *"Self-aligned InP DHBTs for 150 GHz digital and mixed signal circuits,"* Indium Phosphide and Related Materials, Glasgow, Scotland, 8–13 May 2005, pp. 325 – 330.

[233] **X. Li, X. Cao, H. Zhou, C. D. W. Wilkinson, S. Thoms, D. Macintyre, M. Holland, and I. G. Thayne,** *"30 nm tungsten gates etched by a low damage ICP etching for the fabrication of compound semiconductor transistors,"* Microelectronic Eng., vol. 83, no. 4-9, pp. 1152 – 1154, Feb. 2006.

Publications

T. Kraemer, C. Meliani, F. J. Schmueckle, J. Wuerfl, and G. Traenkle, *"Traveling wave amplifiers in transferred substrate InP-HBT technology,"* IEEE Trans. Microw. Theory Tech., vol. 57, no. 9, pp. 2114 – 2121, Sept. 2009.

T. Kraemer, M. Rudolph, F. J. Schmueckle, J. Wuerfl, and G. Traenkle, *"InP DHBT process in transferred substrate technology with f_t and f_{max} over 400 GHz,"* IEEE Trans. Electron Devices, vol. 56, no. 9, pp. 1897 – 1903, Sept. 2009.

T. Kraemer, C. Meliani, F. Lenk, J. Wuerfl, and G. Traenkle, *"Transferred Substrate DHBT of f_t = 410 GHz and f_{max} = 480 GHz for Traveling Wave Amplifiers,"* Indium Phosphide and Related Materials, Versailles, France, 25–29 May 2008.

T. Kraemer, F. Lenk, A. Maassdorf, H. J. Wuerfl, and G. Traenkle, *"High yield transferred substrate InP DHBT,"* Indium Phosphide and Related Materials, Matsue, Japan, 14–18 May 2007, pp. 407 – 408.

T. Kraemer, S. O. Kim, F. Brunner, F. Schnieder, H. J. Wuerfl, and G. Traenkle, *"Development of InP DHBT via transfer substrate process,"* Workshop on Compound Semicond. Devices and Integr. Circuits, Cardiff, UK, 16–18 May 2005, pp. 79 – 81.