Design of Low-Power K-Band Circuits in CMOS Technology

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To my family

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Mohammed Kamal Ali

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Abstract

Millimeter-wave (mm-wave) CMOS transceivers have attracted interest in recent years, especially in the 24 GHz and 60 GHz ISM bands. As indispensable building blocks in a wireless transceiver, frequency generation and conversion circuits are confronted by many design challenges. At mm-wave frequencies, the voltage controlled oscillator (VCO) suffers from a poor phase noise and a limited tuning range, while the frequency divider is usually accompanied by a narrow locking range and high power consumption. Direct down-conversion mixer, on the other hand, suffers from a very poor noise figure as a result of the flicker noise. For the generation of the LO signals with low power consumption, the design of the VCO encounters difficulties. Moreover, the generation of IQ signals with high accuracy over a wide band is much more challenging.

In this dissertation, new techniques and optimized topologies are proposed to improve the performance of mm-wave frequency generation and conversion circuits. Employing a transformer feedback topology, a 24 GHz LC-VCO was designed using 130 nm CMOS technology. It achieves a wide tuning range and consumes one fourth of the power that the conventional LC-VCO requires. The designed transformer feedback VCO has comparable phase noise to the conventional counterpart. Two designs of the mm-wave frequency divider have also been presented. One design is a Ka-band Miller frequency divider in 130 nm CMOS technology. A specific optimization approach was followed to achieve a maximum locking range for low power consumption. The loop gain is maximized over the widest possible frequency range, the Q factor of the load inductor, on the other hand, is chosen such that the third order harmonic is rejected by a required predetermined value. Measurement results of the designed circuits show that their performance compares to the state-of-the-art developments and satisfies the 24 GHz FMCW radar application.

The other design is a 45 GHz static frequency divider using 90 nm CMOS technology. New techniques such as ”inductive peaking”, ”split resistors”, and ”asymmetric sizing of input

transistors" are employed to minimize the power consumption of the divider. Moreover, direct down-conversion mixer is designed. Overcoming the flicker noise effect was a challenge. Novel current bleeding network was therefore proposed. Not only the noise performance is improved but the conversion gain is increased as well. Based on the designed static frequency divider and the direct down-conversion and up-conversion mixers, complete IQ-modulator and demodulator were eventually implemented using 90 *nm* CMOS technology. Measurement results of the designed and tested circuits show that their performance compares to the state-of-the-art developments and satisfies the 60 *GHz* high-data-rate communication application of the IEEE 802.15.3c standard.

Kurzfassung

Die Entwicklung von Millimeterwellen-Transceivern auf Basis moderner CMOS-Technologien steht derzeit weltweit im Fokus von Wissenschaft und Forschung. Dabei sind insbesondere Schaltungen für die ISM-Bänder bei 24 GHz bzw. 60 GHz von Interesse. Beim Entwurf von CMOS-Schaltungen zur Erzeugung und Umsetzung von Frequenzen in diesen Frequenzbereichen ergeben sich zahlreiche unterschiedliche Problemstellungen. So ist einerseits die Performance von spannungsgesteuerten Oszillatoren (VCOs) bei Millimeterwellen-Frequenzen durch ein schlechtes Phasenrauschen sowie durch einen begrenzten Abstimmbereich beeinträchtigt. Anderseits können Frequenzteiler mit großer Bandbreite und geringem Leistungsverbrauch schwierig realisiert werden. Infolge des Flickerrauschens und der einhergehenden schlechten Rauschzahl gestaltet sich des Weiteren auch das direkte Heruntermischen in das Basisband mit sog. *Direct-Down-Conversion*-Mischern als schwierig. Die Erzeugung des LO-Signals bei gleichzeitig geringer Leistungsaufnahme geht mit einigen Schwierigkeiten einher. Zu guter Letzt ist ebenso die Erzeugung von IQ-modulierten Signalen hoher Genauigkeit über größere Bandbreiten eine Herausforderung beim Entwurf solcher Transceiver.

Zur Überwindung dieser Problemstellungen werden in der vorliegenden Dissertation neuartige Methoden und optimierte Schaltungen zur Erzeugung und Umsetzung von Millimeterwellenfrequenzen untersucht. Dies beinhaltet einen 24-GHz-LC-VCO, der auf Basis einer *Transformer-Feedback*-Topologie in einer 130-nm-CMOS-Technologie realisiert wurde. Dieser VCO erreicht einen sehr großen Abstimmbereich und zeichnet sich im Vergleich zu konventionellen LC-VCOs mit einer deutlich reduzierten Leistungsaufnahme bei vergleichbarem Phasenrauschen aus. Des Weiteren sind im Rahmen dieser Arbeit zwei Frequenzteiler entwickelt worden. Der erste Teiler wurde für das Ka-Band in einer 130-nm-CMOS-Technologie entworfen. Dieser sog. Miller-Divider wurde derart optimiert, dass eine maximale Bandbreite bei gleichzeitig minimaler Leistungsaufnahme realisiert werden konnte. Die Schleifenverstärkung wurde über den größt möglichen Frequenzbereich maximiert. Auf der anderen Seite wurde die Güte der Lastinduktivität

derart gewählt, dass die Unterdrückung der 3. Harmonischen auf den erforderlichen Wert gehalten werden konnte. Die mit den realisierten Schaltungen erzielten Messergebnisse entsprechen dem neusten Stand der Technik und genügen den Anforderungen von 24-GHz-FMCW-Radar-Systemen.

Der zweite Frequenzteiler, ein sog. *Static-Divider*, wurde in einer 90-nm-Technologie für eine Frequenz von 45 GHz realisiert. Neuartige Techniken wie *Inductive Peaking*, *Split Resistors* und die asymmetrische Auslegung der Eingangstransistoren wurden hierbei implementiert um die Leistungsaufnahme der Teiler deutlich zu minimieren. Als weiterer Transceiver-Baustein wurde außerdem ein *Direct-Down-Conversion*-Mischer implementiert. Dessen Flickerrauschen konnte durch den Einsatz eines neuartigen *Current-Bleeding*-Netzwerkes verbessert werden. Neben den verbesserten Rauscheigenschaften konnte auf diese Art und Weise außerdem auch ein gesteigerter Konversionsgewinn erzielt werden. Auf Basis des entwickelten *Static-Dividers* sowie der realisierten Mischer konnte schließlich ein kompletter IQ-Modulator bzw. IQ-Demodulator in einer 90-nm-Technologie entworfen werden. Die mit den realisierten Schaltungen erzielten Messergebnisse entsprechen dem neusten Stand von Wissenschaft und Technik und erfüllen die Anforderungen von Nahbereichskommunikationssystemen im 60-GHz-Band gemäß IEEE 802.15.3c.

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List of Abbreviations

3D	Three Dimension
AC	Alternating current
ADS	Advanced Design System
CG	Conversion gain
CMOS	Complementary metal-oxide semiconductor
dB	Decibel
dBm	Decibel referred to milliwatt
DC	Direct current
EM	Electromagnetic
f	Frequency
f_t	Transient frequency
f_{max}	Maximum oscilation frequency
FM	Frequency modulation
g_m	Transconductance of the transistor
G_{max}	Maximum stable gain
Gbps	Giga bit per second
GHz	Gigahertz
HF	High frequency
HFSS	High Frequency Structural Simulation
IC	Integrated circuit
IF	Intermediate frequency
IP3	Third-order intercept point

K	Stability factor
LNA	Low noise amplifier
mA	Milliamperes
MHz	Megahertz
NF	Noise figure
P	Power
P_{1dB}	Input referred 1dB intercept point
PA	Power amplifier
P_{in}	Input power
P_{out}	Output power
PLL	Phase locked loop
Q	Quality factor
RF	Radio frequency
Rx	Receiver
SFD	Static frequency divider
Si	Silicon
Tx	Transmitter
TRx	Transceiver
VCO	Voltage controlled oscillator
W	Width of the MOS transistor

Chapter 1

Introduction

1.1 Motivation

As wireless products, such as wireless networking and localization applications, become a part of people's everyday lives, the need for high performance at lower costs and power consumption become even more important. Overcoming the challenges involved in the design of radio-frequency (RF) transceivers can help satisfy this need. This thesis provides an analysis, design, and characterization of RF circuits for portable applications. The cost of the designs is an important issue, therefore the circuits' layouts were carefully designed in order for the design to occupy small chip area. Battery life, on the other hand, is an important issue for portable applications therefore, optimization procedures are followed to minimize the consumed power.

1.2 Scope of Research

This thesis focuses on the design and characterization various K-band transceiver circuits. The RF circuits were designed using different CMOS technologies; namely, IBM 130 *nm*, and TSMC 90 *nm*. Two different front-ends are to be investigated in this thesis as well; the radar transceiver system, which is designed using the IBM 130 *nm* CMOS technology, and the short range high data rate WLAN transceiver system which is designed based on TSMC 90 *nm* CMOS technology.

Scaling down the size of the transistor shifts its unity gain frequency f_t and its maximum

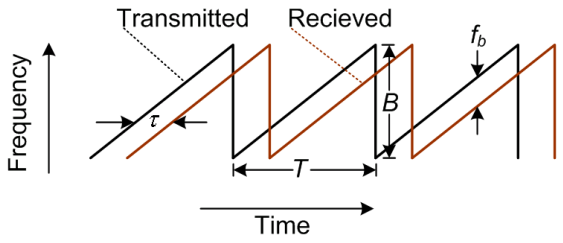


Figure 1.1: Transmit and Receive signals from a point target

oscillation frequency f_{max}. The f_t and f_{max} of the 90 nm CMOS technology are 120 GHz and 150 GHz, respectively; therefore the 90 nm CMOS devices are adequate to impelement the 60 GHz WLAN transceiver front-end.

1.2.1 FMCW Radar Transceiver

Continuous-wave (CW) radar is a type of radar system whereby a known stable frequency CW radio energy is transmitted and then received from any reflecting objects. The main advantage of the CW radar is that energy is not pulsed, they are much simpler to design. Continuous-wave radars have no minimum or maximum range, although the broadcast power level imposes a practical limit on range. CW radar maximizes its total power on a target because the transmitter is broadcasting continuously. Maximum distance in a CW radar is determined by the overall bandwidth and transmitter power. There are two types of CW radars: un-modulated and modulated CW radar.

Frequency-modulated CW radar (FMCW) is a short-range measuring radar capable of determining distance [1]. This increases reliability by providing distance measurement along with speed measurement, which is essential when there is more than one source of reflection arriving at the radar antenna. This kind of radar is often used as ”radar altimeter” to measure exact height during the landing procedure of aircrafts. It is also used as early-warning radar, wave radar, and proximity sensors. Doppler shift is not always required for detection when FM is used. Sawtooth modulation is employed in CWFM radars where range is desired for objects that lack rotating parts.

In a CWFM radar, a chirp signal is transmitted for a certain duration. While it is transmitting,

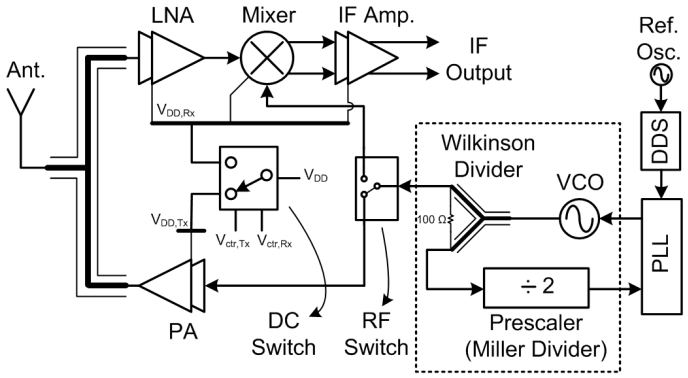


Figure 1.2: Block Diagram of the 24 GHz FMCW Radar Transceiver

the echoes are received by the receiver and mixed with the transmitted signal, and the result is low-pass filtered to produce a superposition of beat frequencies. Fig. 1.1 shows a transmitted and the reflected signals from a point target. The two-way travel time is τ, the bandwidth of the transmit signal is B, and the sweep time is T. At any instance of time, the transmitted and the received signals are multiplied by a mixer. Since multiplying two sinusoidal signals together results in a sum and difference terms, the output signal is then low pass filtered, and only the difference term is left as shown in fig. 1.2 [2] [3]. The frequency of this signal is given by f_b, the beat frequency.

An expression for the beat frequency can easily be found. Using similar triangles and rearranging terms, we obtain the following expression:

$$f_b = \frac{B \cdot \tau}{T} \tag{1.1}$$

since the beat frequency signal is time-limited to T seconds, its spectrum will be a sinc function centered at $f = f_b$, the first zero crossing will occur at $f = \frac{1}{T}$. When multiple targets exist, the result will be a superposition of many beat frequencies. In the frequency domain, two targets beat frequencies can be as close together as $\frac{1}{T}$, substituting in equation 1.1 we have:

$$\Delta\tau = \frac{T \cdot \Delta f_b}{B} \tag{1.2}$$

substituting in $\Delta f_b = \frac{1}{T}$, we have $\Delta\tau = \frac{1}{B}$. Hence, the minimum resolvable separation in time

between two targets is inversely proportional to the bandwidth. The two-way time to a target, τ, and the range to the target, R, are related by the following formula:

$$R = \frac{c \cdot \tau}{2} \tag{1.3}$$

and the range resolution is given by:

$$\Delta R = \frac{c \cdot \Delta\tau}{2} \tag{1.4}$$

where c is the speed of light in air, substituting for $\Delta\tau$ in equation 6.6 gives:

$$\Delta R = \frac{c}{2 \cdot B} \tag{1.5}$$

Since the beat frequency is proportional to τ, and τ is proportional to the range R, knowledge of the beat frequency of any target entails knowledge of the range of that target. With many targets, we can separate them by taking the Fourier Transform of the received signal, and determine the range through frequency.

In contrast to the FMCW radar transceiver design presented in [4], it is desirable to achieve a single antenna TRx. In order to fulfill the single antenna architecture, TRx must be able to switch between the Rx and Tx. In most common architectures the Rx and Tx are connected to the antenna through a switch which either connects the input of the Rx or the output of the Tx to the antenna. In that topology, the switch is located in the most sensitive part of the circuit as both the output power of the PA and the noise figure of the LNA are being affected by the insertion loss of the switch.

In order to avoid RF signal distortion, in this design the switch has been located in the LO path as shown in fig. 1.2. In this case, in the Rx mode, no LO power is being delivered to the Tx and in the Tx mode, no LO power is being delivered to the Rx mixer. Although the isolation of the switches are not infinite, DC supply switching between the Rx and Tx modes, a very high Tx-Rx isolation can be achieved. DC supply switching, beside isolation improvement, can also improve the power efficiency of the TRx.

In this thesis, several RF building blocks for this frond-end transceiver were designed and

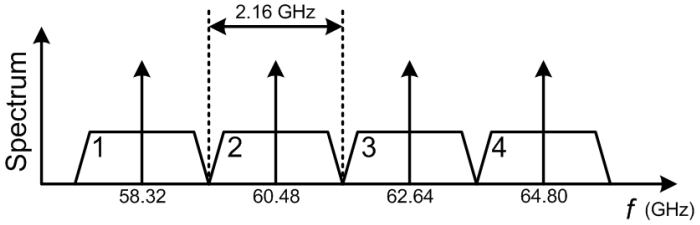


Figure 1.3: Channelization of the IEEE 802.15.3c standard

tested. As shown in fig. 1.2, the marked blocks are the scope of this work.

1.2.2 Short Range High Data Rate WLAN Transceiver

The mm-Wave PHY, is defined for the frequency band of 57 – 66 GHz, as allocated by the regulatory agencies in Europe, Japan, Canada, and the United States as well as any other areas where the regulatory bodies have allocated this band, and is shown in fig. 1.3. Four channels are defined for the PHY, nevertheless regulatory requirements allow fewer in some regions.

A total of three PHYs are defined for the mm-Wave PHY. They are as follows:

- Single Carrier mode in mm-Wave PHY (SC PHY).
- High Speed Interface mode in mmWave PHY (HSI PHY).
- Audio/Visual mode in mmWave PHY (AV PHY).

The SC PHY supports a variety of modulation and coding schemes (MCSs) that support bit rate up to 5 Gb/s. The SC PHY supports a wide range of modulations, $\pi/2$ BPSK, $\pi/2$ QPSK, $\pi/2$ 8-PSK, $\pi/2$ 16-QAM, pre-coded MSK, pre-coded GMSK, on-off keying (OOK), and dual alternate mark inversion (DAMI). The coding schemes included are Reed-Solomon (RS) coding with low-complexity implementation and low-density parity check (LDPC) coding with high error-correcting capability. Code spreading using either linear feedback shift register (LFSR) code or the Golay sequence is also applied to increase the robustness of the system. The HSI PHY, is designed for NLOS operation and uses OFDM with an FEC based on LDPC.

The AV PHY, is designed for NLOS operation and the transmission of uncompressed, high definition video and audio. It uses OFDM modulation with convolutional inner code and a Reed

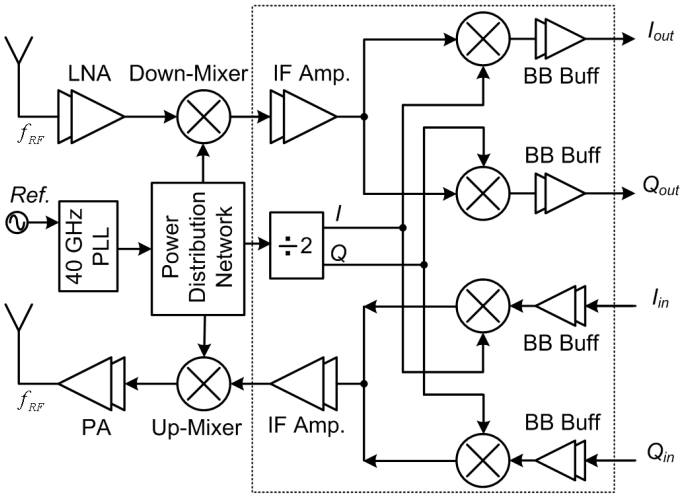


Figure 1.4: Block Diagram of the WLAN Transceiver

Solomon outer code. The AV mode supports omni-directional coverage via the low-rate PHY (LRP) for the purpose of setting up high-throughput connections using the high-rate PHY (HRP).

Different PHYs are a result of demands of different market segments, which were based on the development of the usage models for this standard. For example, one usage model is for kiosk applications. This usage model requires a bit rate of 1.5 Gb/s at a 1 m range. The SC-PHY can provide such a data rate at that short range with less complexity, and thus lower cost than an OFDM PHY. Another usage model required the streaming of uncompressed video. Due to the nature of uncompressed video signals a special PHY, the AV PHY, was selected to provide high throughput. A third usage model uses an ad-hoc system to connect computers and devices around a conference table. In this usage model, all of the devices in the WPAN will have bidirectional, NLOS high speed, low-latency communication, which is provided by the HSI PHY. Mandatory data rates of all those PHYs are selected according to specific usage models. In addition, higher data rates are provided to give options to the implementors so that they can best address the different market segments.

In this thesis, the IQ- modulator and demodulator of the transceiver architecture of fig. 1.2 are designed. The I and Q signals of the LO are generated using wide locking range static frequency divider (SFD) instead of using hybrids which have narrow band for accurate I and Q signals generation. The 40 GHz LO signal is provided by an integer-N PLL, the LO frequencies from the PLL and the divided frequencies fed to the IQ mixers are listed in table 1.1. The IF signals

Channel ID	Start Frequency (GHz)	Center Frequency (GHz)	Stop Frequency (GHz)	LO (GHz)	LO/2 (GHz)
1	57.24	58.32	59.40	38.88	19.44
2	59.40	60.48	61.56	40.32	20.16
3	61.56	62.64	63.72	41.76	20.88
4	63.72	64.80	65.88	43.20	21.6

Table 1.1: mm-Wave PHY chanelization

are fed from the first stage mixer of the receiver path, and fed into an up-conversion mixer for the transmitter path. Finally, the base-band I and Q signals are available from or to DSPs in the receive and transmit paths respectively.

1.3 Differential Signaling

As single-ended and differential signals are compared, it is important to keep the system-level performance metrics in mind for good overall receiver design. A single-ended signal, unbalanced by definition, is measured by the difference between the signal of interest and a constant reference point. The reference point, which is normally ground, serves as the return path for the signal. A problem can be encountered if an error source is introduced into the signal path. Because the ground reference will be unaffected by the injected error, the error is carried forward through the signal. Any signal variation introduced in a single-ended configuration will be difficult to be removed without using overly complex cancellation techniques. Single-ended signals are, therefore, more prone to noise and electromagnetic coupled interference.

Differential signals, on the other hand, are made up of pairs of balanced signals moving at equal but opposite amplitudes around a reference point. The difference between the positive and negative balanced signals corresponds to the composite differential signal. If an error is introduced to a differential system path, it will be added to each of the two balanced signals equally. Because the return path is not a constant reference point, the error will be canceled in the differential signal. Consequently, differential signal chains are less susceptible to noise and interference. This inherent error cancellation also provides better common mode rejection ration

(CMRR) and power supply rejection ratio (PSSR).

In the WLAN Transceiver system, differential signaling is always used for both RF signal and LO signals to overcome the problems of common mode signals and inaccurate power supplies.

1.4 Thesis Organization

The thesis is organized as follows; Chapter 2 presents the background and analysis of various RF circuits such as Miller and static frequency dividers, voltage controlled oscillators, up and down direct-conversion mixers. In chapter 3, an overview of the two CMOS technologies used are represented, metal stacks are shown, device's gain and noise are investigated, and comments on the characterization of the passive components are discussed. In chapter 4, the design procedures and measured data of the 24 GHz circuits are presented, these RF circuits are part of the radar transceiver front-end. Chapters 5 and 6 mainly present the design of both IQ-Modulators and IQ-Demodulators respectively; each circuit, such as, up-conversion, down-conversion mixers, static frequency dividers, IF amplifiers, were separately measured and characterized, then all of the blocks were integrated together to be a part of the complete front-end transceiver. Chapter 7 concludes this work, and a proposal for future work is presented as well.

Chapter 2

RFICs – Essentials and Fundamentals

The theory and analyses of various RF circuits are investigated in this chapter. Frequency dividers are essential parts of frequency synthesizers and clock recovery circuits. Two dividers are presented; a Miller divider designed for the 24 GHz Radar transceiver, and a static frequency divider designed for the 60 GHz WLAN transceiver system. The phase noise of the voltage controlled oscillators is a challenge; sources of phase noise were studied, an optimization procedure for better noise performance was undertaken. Up- and down-conversion mixers are then investigated. When the signal is converted to the vicinity of DC, problems such as flicker noise arise and become a bottleneck. Methods to alleviate these effects are studied.

2.1 Frequency Dividers

2.1.1 Miller Divider

The general key design criteria for frequency dividers are the requirements for low input power, low power consumption, and wide frequency range of correct division. The maximum frequency of operation of static dividers is closely related to and much lower than the device cut-off frequency. Moreover, the power consumption of the static divider increases progressively with the input frequency due to the charging and discharging of capacitances at each clock cycle. On the other hand, regenerative frequency dividers can operate at high frequencies without a proportional

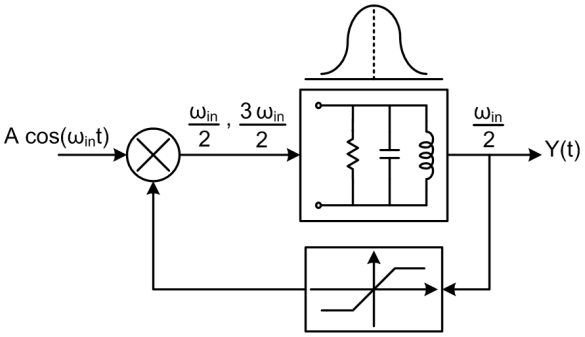


Figure 2.1: Block Diagram of the Miller Divider

increase of power consumption. The high frequency and low power operation of a regenerative frequency divider come at the expense of narrow-band operation and larger chip area due to the utilization of on-chip inductors. In spite of the high frequency and low power operation, the injection locked frequency dividers have narrow frequency range. The dynamic dividers, however, have wider bandwidth than the injection-locked counterpart. Dynamic frequency dividers (DFD) are also known as Miller dividers.

Dynamic frequency dividers or Miller dividers were firstly discovered by Miller in 1939 [5], hence the name Miller divider. They operate on the bases of positive feedback principles; consequently, Barkhausen criterion must be met [6] [7]. The block diagram of the DFD is shown in fig.2.1. For regeneration, a finite signal, e.g. due to thermal noise, must be present in the loop, and the loop gain must be greater than unity; additionally, for zero output with no input the loop gain must be less than unity when the input signal is removed [8] [9]. The oscillation grows until the gain is reduced to unity and amplitude sustains due to nonlinearities. As shown in fig. 2.1, the input signal at ω_{in} is mixed with a feedback signal at $\omega_{in}/2$ to give sidebands at $\omega_{in}/2$ and $3\omega_{in}/2$. The band pass filter selects the lower sideband. The amplifier compensates for loop losses.

While providing an intuitive understanding of the circuit operation, we normally have two methodologies to provide enough selection of the half input frequency signal; low pass filtering, and band pass filtering. The LPF shown in fig. 2.2a fails to stipulate the condition for proper division. For example, the low pass filter may be realized as a first order RC network of fig. 2.2b, a reasonable model of the load seen at the output node of typical mixers [10]. Neglecting

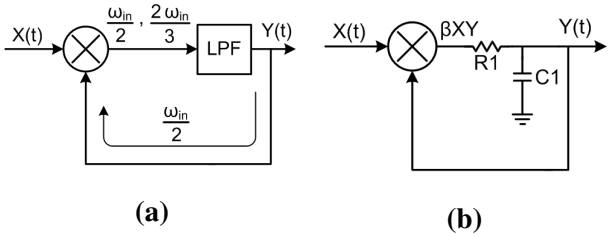


Figure 2.2: Miller Divider (a) Generic Topology (b) Realized with *RC* filter

nonlinearities in the mixer, the node equation at the output node is given by:

$$R_1C_1\frac{dy}{dt}+y=\beta yA\cos(\omega_{in}t) \tag{2.1}$$

where β denotes the mixer conversion factor. The differential equation is first order with constant coefficient and its solution is given by:

$$y(t)=y(0)e^{\left(-\frac{t}{R_1C_1}+\frac{\beta A}{R_1C_1\omega_{in}}sin(\omega_{in}t)\right)} \tag{2.2}$$

Interestingly, it is clear that $y(t)$ decays to zero with a time constant of R_1C_1, and the circuit fails to divide regardless of the value of ω_{in} with respect to the LPF corner frequency, $(R_1C_1)^{-1}$. In other words, $\omega_{in}/2$ is not regenerated even though (R_1C_1) is chosen to attenuate the third harmonic $3\omega_{in}/2$, and even if a noise current at $\omega_{in}/2$ is injected into the loop.

Suppose now that we have the extreme case where all time constants in the loop are negligible, all waveforms are rectangular, and the circuit operates correctly. As illustrated in fig. 2.3b, the mixer output resembles $y(t)$ but shifted by a quarter period, suggesting that inserting a broadband delay in the loop permits correct division. However, the RC network of fig. 2.2b does not satisfy the conditions required in fig. 2.3a. For example, the network cannot provide a phase shift of 90^o at $\omega_{in}/2$ and 270^o at $3\omega_{in}/2$. Furthermore, it attenuates the third harmonic considerably, failing to generate the idealized waveforms shown in fig. 2.3a.

We now study another extreme case where the loop exhibits no delay at $\omega_{in}/2$ but enough selectivity to attenuate the third harmonic [11]. Fig. 2.4 exemplifies this case, with the mixer injecting a current into the parallel tank (i.e. BPF). Solving the node equation at the output node

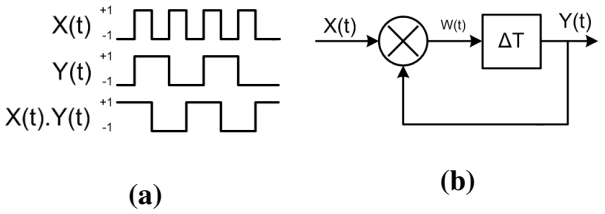


Figure 2.3: Miller divider with wide band phase shifter (a) Waveform (b) Generic Topology

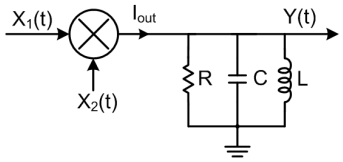


Figure 2.4: Miller divider with BPF

will produce the following:

$$y(t) = Ae^{at} cos\left(\frac{\omega_{in}}{2}t + \theta\right) \tag{2.3}$$

where a is a constant, depending on the loop gain, and is positive only when the loop gain is greater than unity [11]. The positive constant a implies that an exponentially growing sinusoid at half of the input frequency is a possible solution for the system during the transient build-up period. When the oscillations' amplitude is large enough, the devices become nonlinear causing gain compression until it becomes unity and the constant a is finally zero, thus sustainable oscillations will last, whereas the input is applied.

The impact of the third order harmonic on the correct operation is very important. Suppose

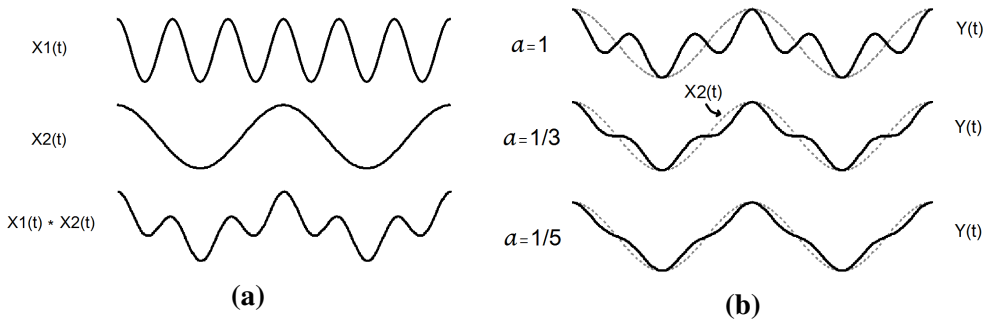


Figure 2.5: (a) Divided and third order harmonic (b) Superimposed waveform for different α

that the peaks of $x_1(t)$ (the required divided output)and $x_2(t)$ (the third order harmonic) have the same amplitude. As depicted in fig. 2.5a, the product waveform displays multiple zero crossings in each period due to the third order harmonic, revealing that such a loop fails to divide if this harmonic is not suppressed sufficiently, i.e., if $y(t)$ does not monotonically rise and fall [10]. Fig. 2.5b illustrates the resulting waveforms for different values of the attenuation factor, α, experienced by the third order harmonic with respect to the fundamental. To eliminate the extraneous zero crossings, we require that the slope of $y(t)$ does not change sign between a positive peak and the next negative peak. Since the output is the superposition of the two tones, thus we have:

$$y(t) = A\left(cos\left(\frac{\omega_{in}}{2}t\right) + \alpha sin\left(\frac{3\omega_{in}}{2}t\right)\right) \tag{2.4}$$

since the third order harmonic exhibits a phase shift of about 90^o, while the required divided output exhibits no shift, then the attenuation α should be less than $\frac{1}{2\sqrt{3}}$.

In summary, proper operation of the Miller divider requires either sufficient broadband phase shift around the loop or enough suppression of the third harmonic. The first alternative is difficult to realize in CMOS technology for the following reasons:

- with the low transconductance of MOS devices, the voltage drop across the load resistors must be large so as to provide enough loop gain
- source followers consume substantial voltage headroom and attenuate the signal
- the limited bandwidth of the source followers prevents the divider from achieving high-speed operation

Fortunately, these issues can be resolved by employing an LC tank as the load in the Miller divider, provided that the small-signal loop gain at half the input frequency is greater than unity.

2.1.2 Static Frequency Divider

Frequency dividers are extensively used for various applications including frequency synthesis and IQ generators. Static frequency dividers (SFD) are commonly used at millimeter-wave (mm-wave) because of their wide operation range; however, they suffer from high power dissipation,

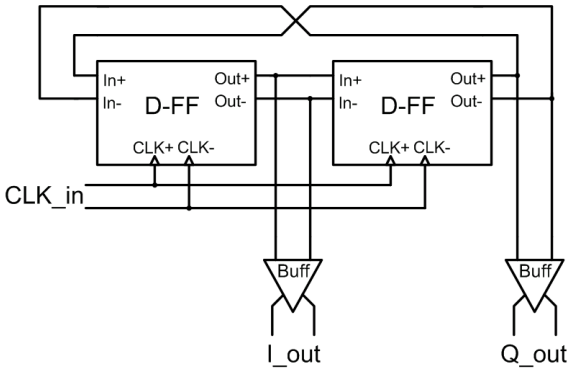


Figure 2.6: Block Diagram of the Static Frequency Divider showing the output buffers of the *I* and *Q* paths

which increases proportional to the operating frequency. Other frequency divider types such as Miller, as well as the injection locking dividers, suffer from narrow operating frequency range. Complex techniques should be used to improve their locking range.

In this design, the (SFD) is used not only as a frequency divider, but as an IQ signal generator as well, as shown in fig. 2.6. Polyphase networks are commonly used as qudrature generators, although imbalance could be minimized over the required frequency range, the polyphoase networks are lossy and noisy circuits. Extra amplifiers should be used to supply enough LO power to the mixer, which require more chip area and more power consumption. The (SFD) can work as a frequency divider while quadrature signals are available at the outputs.

The main target of the (SFD) designers is to achieve the highest possible operation frequency out of the used technology, disregarding the amount of power that the divider needs. For instance, different (SFD) were designed in [12] and [13] with moderate power consumption by using techniques to boost the operation frequency. On the other hand, faster response of the flip-flops is achieved in [14], [15], and [16] with higher power dissipation. A different design technique is used in [17] to further boost the operating frequency by scarifying input sensitivity and power dissipation. In this thesis, techniques will be used to minimize the power consumption where possible. Inductive peaking provides wider bandwidth and can boost the operation frequency. Splitting resistors can speed up the charging and discharging times, thus shortening setup times of the latches. Power consumption can also be minimized through asymmetric transistor sizing, as will be shown below.

2.2 Voltage Controlled Oscillators

Voltage controlled oscillators (VCOs) are critical building blocks in various communication applications such as frequency synthesizers, timing-recovery circuits, and clock generation. One of the most fundamental VCO realizations is LC VCOs. Despite several topologies of the LC VCOs, conventional LC VCOs with cross coupled transistors are most common, owing to their ease of design and simplicity in achieving the conditions of oscillation. Although these conditions are becoming hard to satisfy with frequency increases, techniques are used to boost the g_m of the cross coupled devices.

2.2.1 Principles and Design Issues

Most RF oscillators can be viewed as feedback circuits. Consider the simple linear feedback system depicted in fig. 2.7, with the overall transfere function as follows:

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1-H(s)}. \tag{2.5}$$

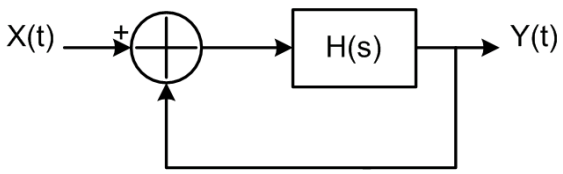


Figure 2.7: Positive feedback oscillatory system

A self-sustaining mechanism arises at the frequency s_o if $H(s_o) = +1$ and the oscillation amplitude remains constant if s_o is purely imaginary, i.e., $H(s_o = j\omega_o) = +1$. Thus, for steady oscillation, two conditions must be simultaneously met at w_o:

- The loop gain, $|H(j\omega_o)|$, must be equal to unity.
- The total phase shift around the loop, $H(j\omega_o)$, must equal to zero or 360^o

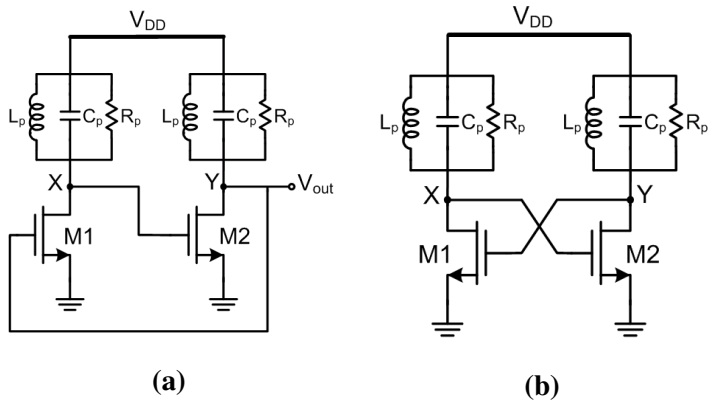


Figure 2.8: (a) Realization of the two-port model (b) Convensional cross-coupled LC VCO

The above conditions are called Barkhausen's criteria [18] [19]. One realization of the above-mentioned concept is shown in fig. 2.8a, a positive feedback system consists of a non-inverting amplifier where input and output are shorted to each other. This configuration is the standard conventional cross-coupled LC VCO as redrawn in fig. 2.8b.

The above view of oscillators is called the "two-port" model [18]. By contrast, the "one-port" model treats the oscillator as two one-port networks connected to each other as shown in fig. 2.9a. Suppose that the tank is a parallel LC tank whose resonance frequency is ω_o and its equivalent resistance is R_p at resonance. The tank by itself does not oscillate indefinitely because some of the stored energy is dissipated in R_p in every cycle. The idea in the one-port model is that an active network generates an impedance equal to $-R_p$ so that the equivalent parallel resistance seen by the intrinsic, lossless resonator is infinite. In essence, the energy lost in R_p is replenished by the active circuit in every cycle, allowing steady oscillation.

One realization of the active negative resistance circuitry is shown in fig. 2.9b, the tank is connected as shown in fig. 2.10a, and the differential version of it is again the conventional LC VCO as shown in fig. 2.10b.

Phase noise, tuning range, and power consumption are the important issues while designing any VCO. However, special attention should be given to the phase noise in order to have the sharp frequency spectrum cause less interference to the nearby channels when the signal is down-converted.

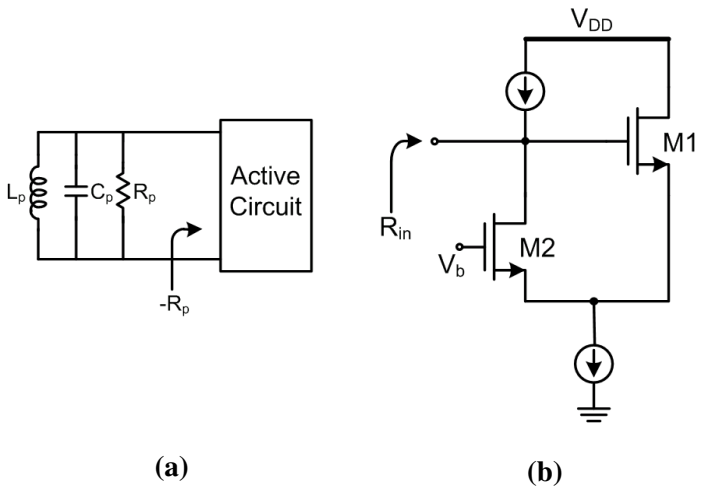


Figure 2.9: (a) One-port model of the LC VCO (b) One Realization of the active negative resistive circuitry

Several noise sources and complicated mechanisms contribute to the noise performance of the VCO. Varactor capacitance variation due to the bias noise causes phase noise through an AM-FM modulation mechanism [20]. Although techniques are used to cancel the bias noise, these are hardly effective at high frequencies. This effect is, however, minor and can be mitigated by either using filtering, which necessitates usage of an extra inductor, or eliminating the current source which deteriorates VCO sensitivity to power supply and process variation.

Switching transistors, on the other hand, have the greatest percentage of contribution to the phase noise. Their thermal and flicker noise appears directly at the output node of the VCO. Flicker noise can, nevertheless, be minimized by maximizing the size of the switching transistors.

Despite the fact that the current source transistor is not directly connected to the oscillating nodes of the VCO, its noise is converted to the neighborhood of the oscillation frequency by the switching transistors. Both high-frequency and flicker noise effects are reduced using larger devices and decoupling capacitors. Low-frequency noise, however, is converted directly to the the VCO's output nodes via the AM-PM mechanism.

Nonlinearity of the switching devices causes generation of 2^{nd} and 3^{rd} harmonics flowing into the low impedance capacitance of the tank, causing in turn a phase imbalance. The oscillator then adjusts its frequency in order to return to its stability condition. Amplitude modulation of the bias of the level of the harmonics, results in variation of phase imbalance level and frequency

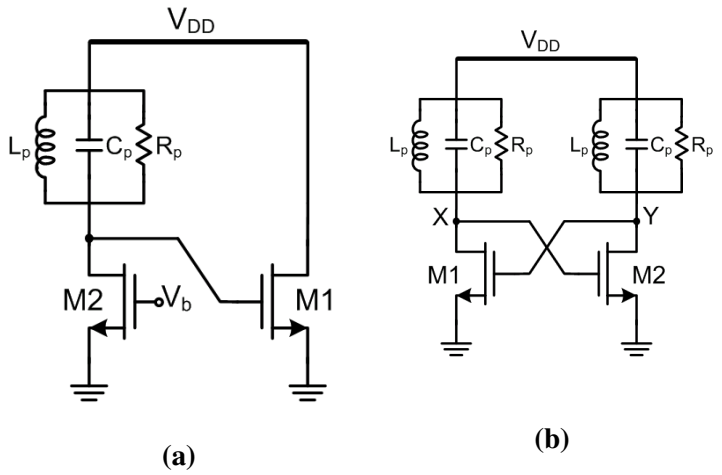


Figure 2.10: (a) Realization of the one-port model (b) Convensional cross-coupled LC VCO

shift. This is called an AM-PM modulation mechanism.

The AM-PM effect can be minimized by increasing the linearity of the switching devices. Linearity increases by narrowing the devices, so that the overdrive voltage is increased. Smaller devices, however, suffer from increased levels of flicker noise. Thus, a trade off between flicker noise and AM-PM mechanism exists, and the proper size should be selected for the minimum possible phase noise.

2.3 Direct Converison Mixer

The mixer is an important building block of a typical front-end circuit, since the frequency translation process will generate some unwanted spurious signals to degrade the signal-to-noise ratio (SNR). The noise becomes an important factor of the mixer. In most transceivers, the noise of the mixer affects the noise of RF front-end system. Therefore, a low noise mixer is very important in the design of front-end transceivers.

For direct conversion receivers, the devices suffer from a very high intrinsic flicker noise. Linear RF circuits are not affected by the flicker noise, such as low noise amplifiers (LNA), since its operating frequency is much higher than the flicker noise corner frequency, but in the mixers, the case is different, because the flicker noise lies in the output band of the mixer, especially, in

low-IF and Zero-IF mixers. For heterodyne receivers the problem is more relaxed, as the final downconversion stage is preceded by a long chain of amplification, thus its noise contribution is lower and the dynamic range is not extremely affected. Nevertheless, the reduction of their flicker noise is required as the output frequency is in the DC vicinity.

Passive mixers have several advantages. They have zero DC power consumption, high linearity and low noise figure. But there are some disadvantages that limit their use in high performance and high dynamic range front ends. The large LO powers are required for driving passive mixers which impose large power consumption for the VCO unit. The isolation between different ports of passive mixers is small and their occupied area on the silicon is large. Beside the above disadvantages the passive mixers impose large losses on the signal. According to the basic Firis formula the noise of the succeeding stages would become as large as the loss of the mixer. This is why the sensitivity of the receivers with a passive mixer is not adequate while the noise figure of the mixer itself is very small. In this thesis, a Gilbert-Cell mixer will be adopted. Techniques will be used to reduce the flicker noise. Power consumption is also an important design target as well as the noise performance.

2.3.1 Gain of the Gilbert-Cell mixer

The Gilbert cell consists of a transconductance or driver stage, which is a differential pair biased at a fixed operating point, and two switching pairs driven by the strong LO signal [21] [22]. Resistive or tuned tank loads can be connected at the output, and degeneration can be used to linearize the transconductance stage. For a double balanced mixer, shown in fig. 2.11, since a large AC drive is applied to the switching pair, the bias of the switch transistors is not fixed but varies periodically with time. When a differential voltage greater than a certain value V_x is applied between the gates of the two transistors, one of them switches off. When the absolute value of the instantaneous LO voltage V_{LO} is lower than V_x, the current of the driver stage is shared between the two devices. In this case, it is desirable to find the drain current of each transistor for a given LO voltage and driver-stage bias current. We will assume that the output conductance of the devices can be neglected, and therefore $M1$ can be modeled with an ideal current source I_B. The

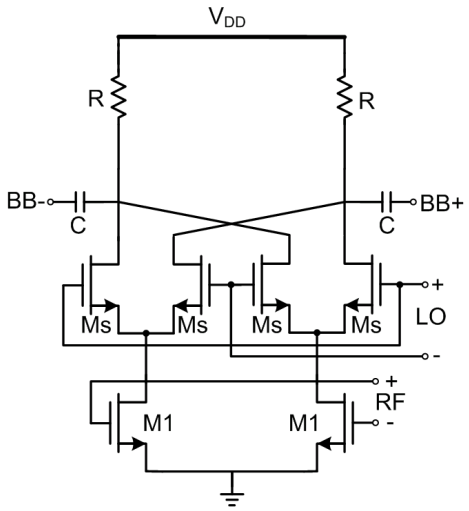


Figure 2.11: Conventional Gilbert-Cell mixer

output current of the single-balanced mixer is a function of the instantaneous LO voltage V_{LO} and the current at the output of the driver stage $I_B + i_s$, with I_B being the bias current and i_s the small-signal current in one single output is as follows:

$$I_{o1} + i_{o1} = I_1 - I_2 = F(V_{LO}(t), I_B + i_s) \tag{2.6}$$

Since i_s is small, a first order Taylor's expansion gives:

$$i_{o1} = \frac{dF}{dI_b}_{I_B} \cdot i_s \tag{2.7}$$

$$i_{o1} = p_1(t) \cdot i_s \tag{2.8}$$

$p_1(t)$ periodic waveform. In a doubly balanced structure, the total output current is as follows:

$$i_{o2} = p_1(t) \cdot (-i_s) \tag{2.9}$$

$$i_o = i_{o1} - i_{o2} = 2p_1(t) \cdot i_s \tag{2.10}$$

During the time interval Δ when the LO voltage is between V_x and $-V_x$ and both transistors are on, $p_1(t)$ depends on , $V_{LO}(t)$, I_B and the IV characteristics of the transistors. $p_1(t)$ can be written

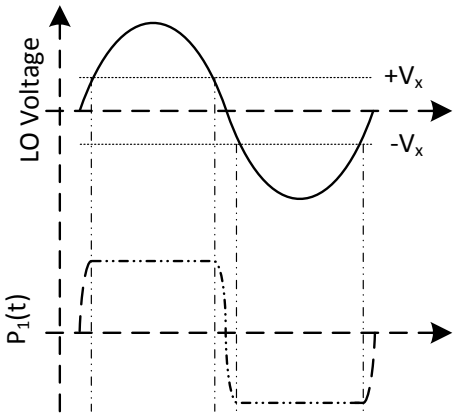


Figure 2.12: Typical waveform of the Taylor series coefficient $p_1(t)$ of the switching pair

as follows:

$$p_1(t) = \frac{g_{m1}(t) - g_{m2}(t)}{g_{m1}(t) + g_{m2}(t)} \tag{2.11}$$

Where $g_{m1}(t)$ and $g_{m2}(t)$ represent the instantaneous small-signal transconductances of the switching transistors. A signal i_s is multiplied by the waveform $p_1(t)$, and therefore the frequency spectrum of the corresponding output is:

$$I_{o1}(\omega) = \sum_{n=-\infty}^{n=\infty} p_{1,n} \cdot I_s(\omega + n\omega_{LO}) \tag{2.12}$$

It is worth noticing that with good device matching, $p_1(t)$ is an odd symmetry (i.e. $p_1(t) = -p_1(t + \frac{T_{LO}}{2})$), with T_{LO} being the LO period, and hence $p_1(t)$ has only odd-order frequency components (See fig. 2.12). Usually the term for $n = 1$ or $n = -1$ is of interest, corresponding to shifting up or down the input signal in the frequency domain by one multiple of the LO frequency, and in this case $C = |p_{1,1}| = |p_{1,-1}|$ represents the conversion gain of the switching pair alone. Since $i_s(t) = g_m \cdot v_{in}(t)$ where $v_{in}(t)$ is the input voltage signal at the gate of the transconductance transistors and g_m is the transconductance of it, the conversion gain of the single-balanced mixer in transconductance form is:

$$g_c = C \cdot g_m \tag{2.13}$$

For high LO amplitude, $p_1(t)$ approaches a square waveform and C approaches $\frac{2}{\pi}$. Assuming $V_{LO} = V_x$ as it should be for proper mixer operation, an estimate for C can be obtained by approximating $p_1(t)$ with a straight line during Δ [22].

$$C = \frac{2}{\pi}\left(\frac{sin(\pi\Delta f_{LO})}{\pi\Delta f_{LO}}\right) \tag{2.14}$$

And V_x is given as follows [23]:

$$V_x = \frac{\alpha I_B}{2K} + \sqrt{\left(\frac{\alpha I_B}{2K}\right)^2 + \frac{I_B}{K}} \tag{2.15}$$

Thus, the mixer gain can be improved by decreasing the bias current I_B, or enlarging the switching transistor size. Limiting bias current can be achieved by using bleeding networks in order to keep g_m of the driver transistors, therefore, conversion gain is unaffected. Increasing the size of the switches helps to decrease V_x and improves its flicker noise contribution; nevertheless, further increasing the size of the transistor adds more parasitic capacitance at the common source nodes. Some of the AC current from the driver transistors is shunted in the parasitic capacitances at the common source node causing degradation for the conversion gain. Therefore, size of the switches should be optimized in order to attain the maximum conversion gain.

Chapter 3

CMOS Devices for RFIC – Technology Overview

3.1 Introduction

In addition to active transistors, RF circuits are composed of various passive components used for impedance matching, resonant circuits, filters, and bias circuitry. The passive components include inductors, capacitors, transmission lines, and resistors. Varactors with appropriate tuning capability are also employed in the VCO. All of these devices can be implemented in standard CMOS technologies using interconnection metals, MOS (Metal-Oxide-Silicon) transistors, and polysilicon layers. However, geometric and process limitations such as the thickness of the metal, the physical distance from the substrate, the maximum metal width and minimum spacing, and the doping concentrations limit the value of the achievable impedance, therefore, the performance of the on-chip passive devices are limited. In this chapter, the properties of the RF components that can be implemented in CMOS technology are discussed, their impact on the circuit performance is presented.

In the CMOS process, aluminum (Al) and copper (Cu) are usually used for the fabrication of the metal traces. The distance between the top metal and the substrate is 16.89 μm for the 130 nm CMOS, and 5.265 μm for the 90 nm CMOS technology. Fig. 3.1(b) and fig. 3.1(a) show the metal stack of the two processes [24] and [25]. The relative permitivity of the silicon substrate is 11.9

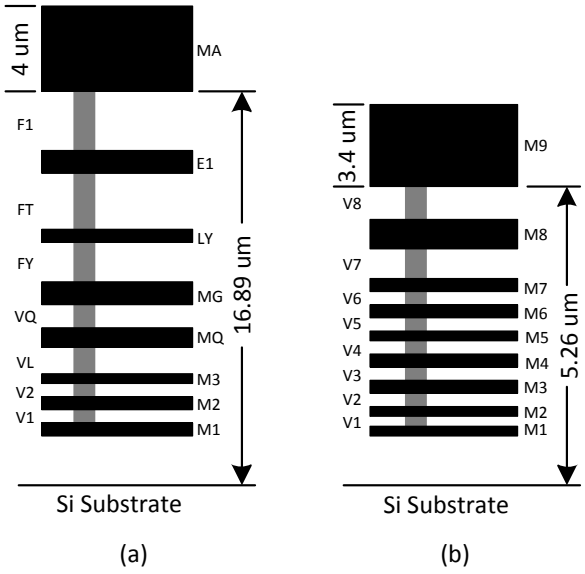


Figure 3.1: Metal Stack of the (a) $130-nm$ Technology [24] and the (b) $90-nm$ Technology [25]

while its conductivity is 10 S/m. The low substrate resistivity and the short distance between the top metal and the substrate significantly limit the RF performance that can be achieved, because of high ohmic metals and lossy dielectrics.

3.2 Active Devices in CMOS Technology

At high frequencies, the effect of the series resistive parasitics have become more significant. Therefore, it is important to include these parasitics in the transistor model in addition to the capacitive parasitics that are already included in the digital CMOS models. Fig. 3.2 shows the MOSFET model.

3.2.1 Gain

The key figure-of-merits characterizing the RF performance of a transistor are the unity gain frequency (f_t) and the maximum oscillation frequency (f_{max}). The unity gain frequency, (f_t), is defined as the frequency where the short-circuited current gain of the transistor is one. This parameter is often used to measure the speed of the device. For MOS transistors, the unity gain

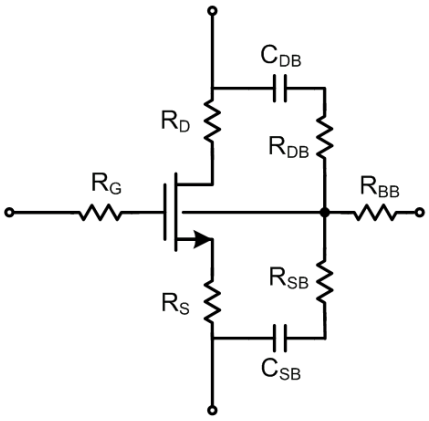


Figure 3.2: On-chip Transistor Model

frequency can be expressed as:

$$f_t = \frac{g_m}{2\pi\sqrt{C_g^2 - (g_m r_i C_{gs} - C_{gd})^2}} \approx \frac{g_m}{2\pi C_g} \tag{3.1}$$

assuming that $|C_g| >> |g_m r_i C_{gs} - C_{gd}|$. Here $C_g = C_{gs} + C_{gd}$. An important observation is that the current gain is independent of the gate resistance of the device. It is shown that f_t is dependent on the drain-source current I_{DS}.

The maximum oscillation frequency, f_{max}, is also important since it indicates the maximum frequency at which useful power gain can be expected from a device. f_{max} is defined as the frequency where the Mason's unilateral gain becomes one. For MOS transistors, the maximum oscillation frequency can be expressed as:

$$f_{max} = \sqrt{\frac{f_t}{8\pi R_{g,i} C_{gd}}} \tag{3.2}$$

It can be predicted that f_{max} varies with $\frac{1}{W}$ and proportional to $\sqrt{g_m}$ [26].

However, the value of f_{max} is determined not only by sizing and bias conditions, but is also highly dependent on resistive losses due to transistor and layout parasitic [27]. By using narrow finger widths, the effect of the gate resistance can be made negligible compared to the other parasitic resistors. Therefore, with optimal layout, f_{max} is not limited by the gate resistance, but is primarily determined by the series source/ drain resistances and substrate losses. Fig. 3.3

shows f_{max} of the 130 nm CMOS transistor. It can be higher than 120 GHz with current density exceeding 40 $\mu A/\mu m$ and finger width in the range 1 μm to 4 μm [28]. Also the device noise performance achieves its optimum in the same range of the finger width.

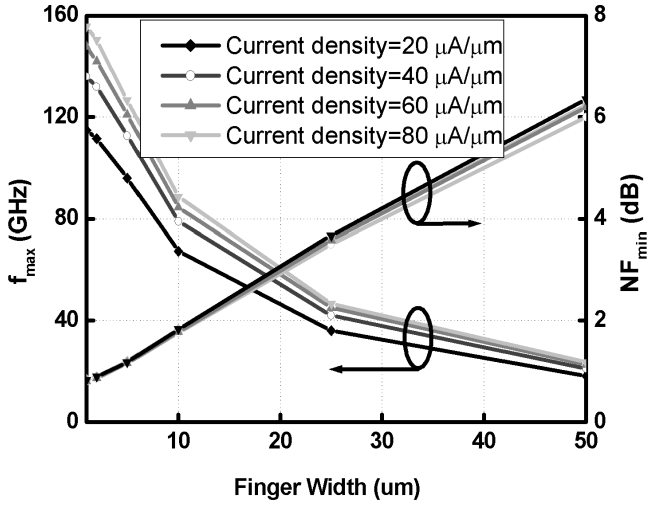


Figure 3.3: Simulated f_{max} and NF_{min} as a function of finger width and biasing current density at a total width of 50 μm

3.2.2 Noise

The high frequency noise of a CMOS transistor is characterized by the minimum noise figure (NF_{min}). For CMOS transistors, the minimum noise figure can be expressed by the following empirical equation [29]:

$$NF_{min} = 1 + K\frac{f}{f_t}\sqrt{\gamma g_m(R_g + R_s)} \tag{3.3}$$

where it has been shown that (NF_{min}) decreases with the device scaling to smaller dimensions, and equation 3.3 indicates that (NF_{min}) decreases as a result of the increased (f_t). Equation 3.3 also indicates that R_g is an important parameter affecting the (NF_{min}) and that transistors should be designed to minimize the value of R_g in order to demonstrate lower (NF_{min}). As shown in fig. 3.3, this can be achieved by decreasing the finger width of the device.

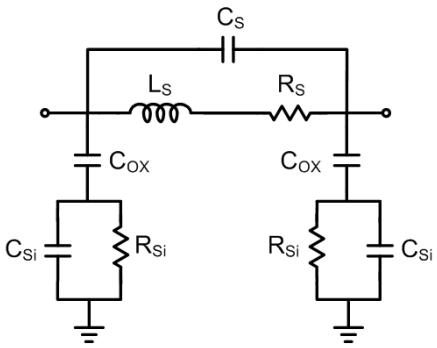


Figure 3.4: On-chip Inductor Model

3.3 Passive Devices in CMOS Technology

3.3.1 Inductor

Fig. 3.4 shows a commonly used equivalent circuit of an on-chip spiral inductor [30]. In this equivalent circuit, L_s represents the inductance of the spiral, R_s is the metal series resistance, and C_s is the series feed forward capacitance that accounts for the capacitance due to the overlaps between the spiral and the underpass. C_{ox} represents the capacitance due to the oxide layers between the inductor metal and substrate, while R_{si} and C_{si} are the resistance and capacitance due to the presence of the substrate. Because the inductor is fabricated over a low resistivity silicon substrate, the actual inductance and quality factor in a circuit vary considerably with the frequency of operation. At low frequencies, the inductor behaves as an inductance with series resistance (metal resistance due to limited conductivity), while at higher frequencies, the inductor is shunted not only by a parasitic capacitance between the inductor turns, but also by the capacitance between the metal layers and the substrate itself. The interplay between the inductance, the parasitic capacitance, and resistance causes the quality factor to rise at low frequencies, reach a peak and then fall off at high frequencies.

In CMOS technology, inductors are usually fabricated as a spiral structure by using the top metal of the process. This is to minimize the parasitic capacitances and as a result increase the self-resonant frequency by maximizing the distance from the inductor metal to the substrate. Several uppermost levels of metals can be used together, as they can be connected in parallel through vias to achieve a very low effective sheet resistance. Alternatively, the metal traces in

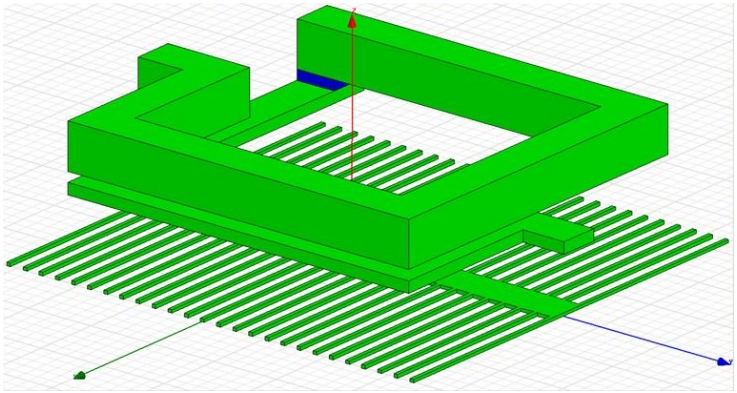


Figure 3.5: On-chip Stacked Inductor for high inductance value per Area

different layers can be connected in series to achieve a high inductance per unit area. An Inductor which is formed by series connection of layers is called stacked inductor and is shown in fig. 3.5. Higher inductance values can be achieved in a smaller area. It suffers, however, from reduced self-resonance frequency and lower quality factors.

The inductance and quality factors of an inductor can be extracted from the admittance (Y) parameters which are calculated from the measured scattering (S) parameters by using the equations below:

$$L_{ind} = -\frac{imag(1/Y_{11})}{\omega} \tag{3.4}$$

$$Q_{ind} = -\frac{imag(Y_{11})}{real(Y_{11})} \tag{3.5}$$

According to the equivalent circuit in fig. 3.4, Y_{11} can be derived by the following equation:

$$Y_{11} = \frac{1}{R_S + j\omega L_S} + j\omega C_S + j\omega C_{OX} || \left(\frac{1}{R_{Si}} + j\omega C_{Si} \right) \tag{3.6}$$

The substrate loss can be reduced by having an opening in the P-well underneath the spiral to increase the resistivity of the substrate or by placing the patterned ground using the lowermost metal layer. The purpose of this shield is to terminate the parasitic electric field entering the substrate. As a result, the inductor parasitic substrate loss becomes smaller. Table 3.1 presents examples of the characteristics of spiral inductors in 90 nm CMOS technology. The achievable values of inductance, quality factors, and operating frequencies are limited and governed by trade-offs. The distance between the top metal and the substrate, and the low resistivity of the

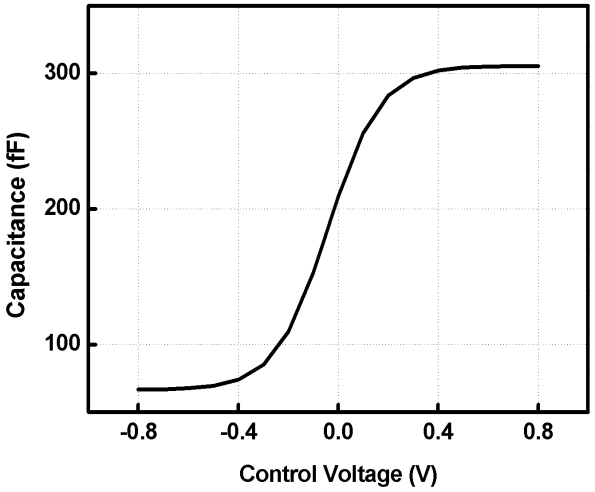


Figure 3.6: MOS capacitance ranges from 35 fF to 310 fF with 40 total number of fingers

substrate limit the performance of any inductors.

L (pH)	Type	Peak (Q)	$f_{Q_{peak}}$ (GHz)	Area $(\mu m \times \mu m)$	Layers
285	Normal	36	32	42×42	M9
	Stacked	10	39	24×24	M7 to M9
510	Normal	19.5	23	50×50	M9
	Stacked	9	25.5	25×25	M6 to M9
835	Normal	15	15	62×62	M9
	Stacked	8	17.5	26×26	M6 to M9

Table 3.1: Simulation of normal and stacked inductors in the 90 nm CMOS technology

3.3.2 CMOS Varactor

Varactors in CMOS technology can be made of transistors by connecting the source and the drain to each others. The transistors operate in both the depletion and the accumulation regions, hence the name accumulation-mode varactor. In this way, the capacitance C_{mos} is monotonically changed. The tuning characteristic of the accumulation mode varactors of the 90 *nm* technologies with a total number of fingers of 40 is shown in fig. 3.6.

The capacitance and quality factor of a varactor can be found using the Y parameters extracted

from the measured scattering parameters and are given by the expressions below:

$$C_{var} = \frac{imag(Y_{11})}{\omega} \tag{3.7}$$

$$Q_{var} = \frac{imag(Y_{11})}{real(Y_{11})} \tag{3.8}$$

In this example, the characteristics of the varactors in the TSMC 90 *nm* CMOS process at 20 GHz is shown. Capacitance range is from 66 fF to 300 fF with the worst case Q factor of 8. The achievable values of capacitance, quality factors, and operating frequencies are limited and governed by trade-offs. While the quality factor of an inductor increases with frequency, the quality factor of a varactor decreases with frequency. Thus, when used in the LC tank of an oscillator, the size of a varactor should be chosen so that its quality factor does not degrade the overall quality factor of the LC tank.

3.3.3 Metal Capacitor

In CMOS technology, capacitors can also be fabricated with two closely placed metals. A metal-insulator-metal (MIM) capacitor is made with two parallel metal plates and an insulating layer between them. Since the bottom plate and adjacent substrate form a parasitic capacitor, this capacitor is non-symmetrical. To minimize the effect of this parasitic capacitance, the two uppermost metal layers are usually used to form an MIM capacitor. The distance between these two metals (0.715 μm for TSMC 90 *nm* processes) is too large to achieve a desirable capacitance per unit area. In reality, extra metal layers are inserted between the two metal layers and connected with the upper layer through vias to decrease the gap between these two metal plates of the capacitor and increase the capacitance value per unit area. As shown in fig. 3.7 [25], capacitor top metal (CTM) and capacitor bottom metal (CBM) are inserted between M7 and M8 and connected to M8 through vias. MIM capacitors of the 90 *nm* CMOS are shielded by a floating metal dummy at M6 and M5.

For decoupling and matching, a constant capacitance with respect to the operating frequency is required. The capacitance of metal capacitors is independent of the applied input voltage, but

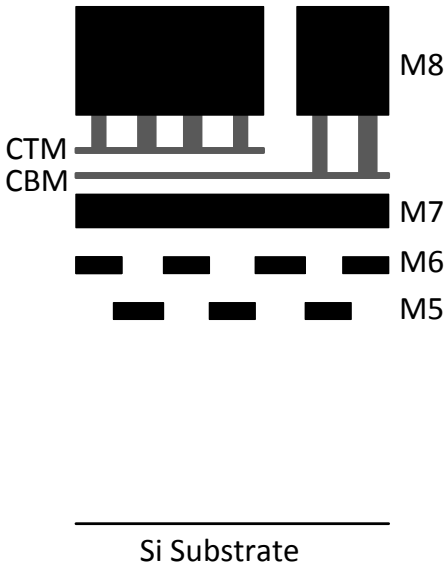


Figure 3.7: On-chip MIM capacitor, capacitor-top-metal and capacitor-bottom-metal are inserted to increase the capacitance per unit area

their capacitance per unit area is less than the MOSFET-based capacitors, and thus less area efficient. Although MOSFET-based capacitors can have higher capacitance density over the MIM capacitor, they suffer from capacitance variations with applied voltage.

The capacitance and quality factor of a MIM capacitor can be measured with the same method as a varactor and are given bey the following equations:

$$C_{var} = \frac{imag(Y_{11})}{\omega} \tag{3.9}$$

$$Q_{var} = \frac{imag(Y_{11})}{real(Y_{11})} \tag{3.10}$$

Table 3.2 shows examples of the characteristics of the metal capacitors in the 90 *nm* CMOS processes. Larger area capacitors have longer metals, this means higher parasitic inductors and thus lower resonance frequency, and higher metal resistance thus lower Q. On the other hand, shrinking the area of the capacitors limits the permissible number of vias that connects both CTM and CBM to M8, this leads to higher series resistance and lower Q. The optimum capacitor value according to Table 3.2 is 215 fF which corresponds to an area of $(10 \times 10)\ \mu m^2$.

C (fF)	Q at 20 GHz	f_r (GHz)	Area ($\mu m \times \mu m$)
35	18	348	4×4
55	22	373	5×5
108	26	188	10×5
215	36	121	10×10
500	21.6	74	15×15
975	12.6	50	20×20
1800	7.2	37	25×25

Table 3.2: Simulation examples of the MIM capacitors in the 90 *nm* CMOS technology

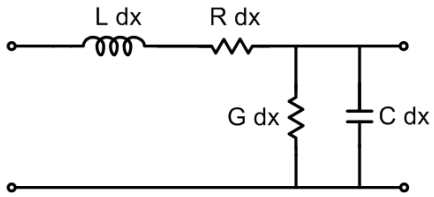


Figure 3.8: Lumped model of the Transmission Line

3.3.4 Transmission Line

A section of a transmission line can be modeled by a lumped circuit model shown in fig. 3.8, where R, L, G, and C are the series resistance, series inductance, shunt conductance, and shunt capacitance per unit length, respectively. When it is assumed that the loss is small, the line can be characterized by following parameters:

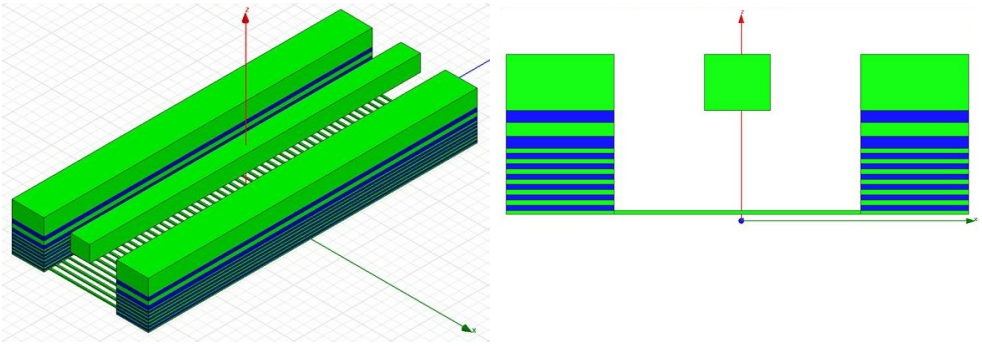
$$Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \approx \sqrt{\frac{L}{C}} \tag{3.11}$$

$$\lambda \approx \frac{2\pi}{\omega_o \sqrt{LC}} \tag{3.12}$$

$$Q_L = \omega_o L / R \tag{3.13}$$

$$Q_C = \omega_o C / G \tag{3.14}$$

where Z_o is the characteristic impedance of the transmission line, λ is the wavelength, Q_L is the inductive quality factor, and Q_C is the capacitive quality factor.



(a) (b)

Figure 3.9: Coplanar waveguide with ground plan

On-chip transmission lines can be made using coplanar waveguide (CPW) with ground plane underneath as shown in fig. 3.9a and fig. 3.9b. The lines are implemented in the uppermost layer to maximize the distance from the low-resistive substrate which has the potential to lower the capacitive quality factor (Q_C). The ground plane helps to prevent the electric field from penetrating into the substrate, thus, the shunt loss is mainly due to the loss tangent of the oxide, resulting in a high capacitive quality factor value. The width of the signal line and the gap between the signal line and ground specify the values of Z_o, Q_L, and Q_C, as shown in the above equations. The existence of the ground shield reduces the distance from the line to the ground plane, leading to narrower 50 Ω lines. As a result, the ohmic loss increase and the inductive quality factor degrades.

3.4 Conclusions

The gain and noise performance of the transistor is significantly affected by the parasitic resistances. Therefore, the layout and size of the transistors should be chosen such that these parasitic resistances are minimized, multi-finger structures with a small width for each finger is an optimum choice.

Passive devices such as inductors, capacitors, varactors, and transmission lines are normally provided by the CMOS technology founder. At high frequency, the performance of these devices is degraded because of the limited metal thickness and the short distance between the metal layer

and the lossy substrate. The trade-off should be considered to achieve the required performance at the required frequency. Varactors are mainly used in the LC tanks of VCOs for frequency tuning. Unlike inductors, the quality factor of a varactor decreases with frequency. Multi-finger varactors can be used to improve their quality factors. Metal-insulator-metal (MIM) capacitors are usually used for decoupling and matching. Therefore, they should be designed so that their self-resonance frequency is higher than the operating frequency of the circuit. This can be achieved by avoiding long metal lines in the capacitors and thus large inductance.

Integrated transmission lines can be implemented with CPW with a ground patterned shield. Shielding prevents the waves to penetrate into the lossy substrate, thus limiting the loss to only the oxide loss tangent. Introducing ground shield increases the Z_o of the lines. Narrowing the lines adjust their Z_o to 50 Ω at the expense of increased metal resistive losses and degraded inductive quality factor Q_L.

Chapter 4

Design of RF Circuits for the 24 GHz FMCW Radar Transceiver

4.1 System Overview

One of the most common Radar topologies is the FMCW radar [2] [3]. The designed transceiver shown in fig. 4.1 is used as a short range automotive radar. Its principle of operation along with its resolution calculation is discussed in the introductory chapter of this thesis. In this work, the Miller divider, and the voltage controlled oscillator are designed and tested to be integrated into the complete front-end transceiver.

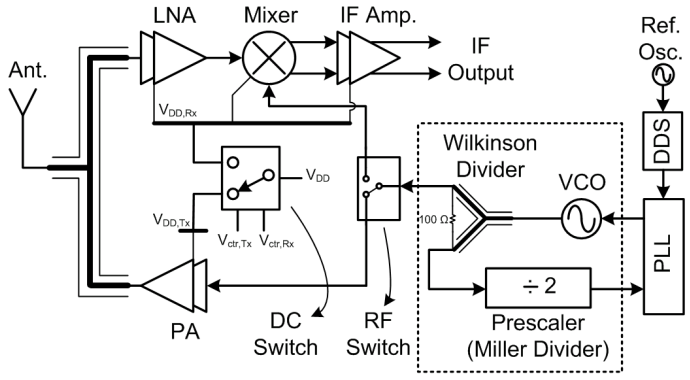


Figure 4.1: Block Diagram of the 24 GHz FMCW Radar Transceiver

4.2 Miller Frequency Divider

4.2.1 Design Approach

The designed Miller divider is designed based on a double balanced Gilbert-Cell mixer with inductive load as shown in fig. 4.2. The inductors L_p are designed to resonate with the output nodes' parasitic capacitances at exactly half the input frequency. These capacitances are: Gate capacitance of the divider transistors, drain capacitances of the switching transistors, and gate capacitances of the following stage.

The feedback capacitance C_{fb} is used only to sample the output voltage signal and feed it back to the gates of the transconductance transistors. Their values therefore must be large enough to behave as RF short-circuit at the desired divided frequency, and thus there is only a negligible effect of the total capacitance at the output nodes. An output on-chip active balun [26] has been utilized to isolate the output node of the divider from the 50 Ω load, and to convert the differential to single ended output.

The required Q of the load inductors determines the required attenuation of the third harmonic as well as the loop gain over the operation range. Assuming for simplicity that the switches are ideal, the equivalent resistance at the output nodes is R, the transconductance of the driver transistors is g_m, and the transfer function of the resonance LC circuit is $H_f(s)$. Thus the open loop gain which must be greater unity is given as follows:

$$gain = \frac{2}{\pi} g_m R H_f(s) \tag{4.1}$$

where

$$H_f(s) = \frac{2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.2}$$

given that $\omega_n = \frac{1}{\sqrt{LC}}$ is half the input frequency, and $2\zeta\omega_n = \frac{1}{RC}$. A value of the lowest Q corresponds to the marginal attenuation for the third order harmonic of $\frac{1}{2\sqrt{3}}$. This value corresponds to the widest frequency range for correct division. Thus, the minimum selectivity of the filter is as

follows:

$$\frac{L^2\omega^2}{L^2\omega^2 + R^2\left(1 - LC\omega^2\right)^2} = \left(\frac{1}{2\sqrt{3}}\right)^2 \tag{4.3}$$

the Q factor of the inductor is expressed as $\frac{R}{L\omega_n}$ and equal to $\mathbf{1.24}$ from the calculation of the previous equation and is shown in [10].

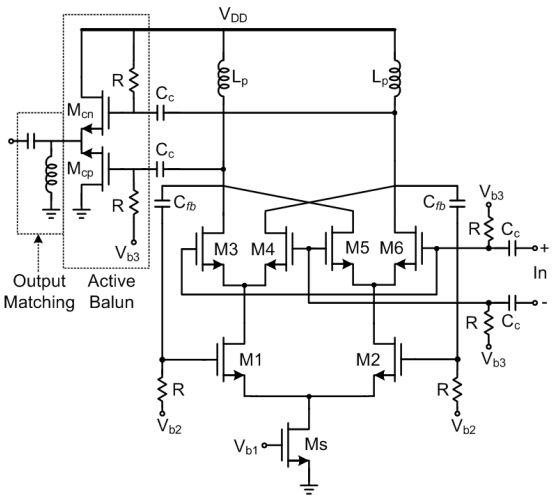


Figure 4.2: Miller divider circuit with active output balun

$W_s\ (\mu m)$	$W_{1,2}\ (\mu m)$	$W_{3,4,5,6}\ (\mu m)$	$W_{cp,cn}\ (\mu m)$	$C_{fb}\ (fF)$
30	60	30	30	600

Table 4.1: Circuit Parameters of the Miller Divider

$L_p\ (pH)$	$R\ (K\Omega)$	$V_{b1}\ (mV)$	$V_{b2}\ (mV)$	$V_{b3}\ (V)$
570	10	600	900	1.2

Table 4.2: Circuit Parameters of the Miller Divider

However, much higher value is required to guarantee enough loop gain, which degrades for the following reasons:

- The parasitic capacitance between the transconductances' drains creates a pole that wastes about half of the small signal drain currents.
- The gradual switching of the switching pairs with the nearly sinusoidal drive converts part of the differential currents into common mode current.

- The load inductors' capacitances and the coupling capacitors make the resonant frequency lower than half the input frequency.

Fig. 4.3 shows the simulation results of the magnitude of the open-loop gain and the third order harmonic attenuation. The frequency range for correct division can be extracted from this figure using the following conditions:

- Magnitude of the voltage gain must be at least unity
- Enough attenuation of the third harmonic

As seen in fig. 4.3, for lower frequencies the third-order attenuation factor α being out of range specifies the lower frequency limit. In our case the rejection is not enough at nearly 38 GHz and beyond. On the other hand, the upper frequency range limitation is specified by the decreasing gain which is going less than unity at about 46 GHz. Note that the voltage gain and the attenuation factor of the third order harmonic of fig. 4.3 are open loop simulated results, meaning that the center frequency is shifted upward.

The load inductors $L_p = 0.57\ nH$ with $Q-$factor of 8.5 resonate with the parasitic capacitances at the output nodes, thus providing 300 Ω equivalent resistance at 14 GHz with negligible effects on voltage headroom.

When maximum gain of the mixer at high frequency is required, the driver transistors must be fast enough to provide the adequate gain. Referring to fig. 3.3 in the previous chapter, transistors

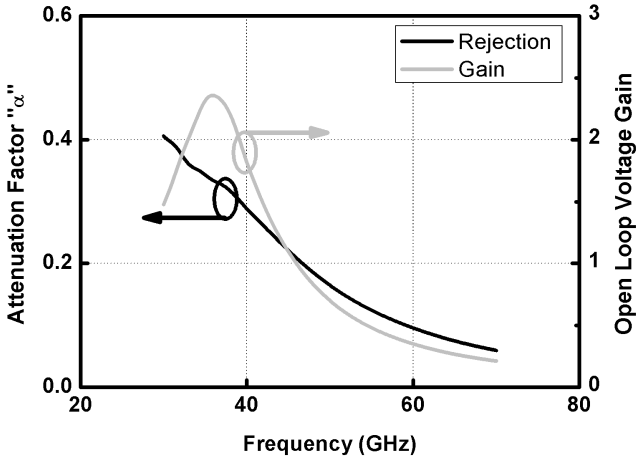


Figure 4.3: Simulated open loop gain and third order harmonic attenuation

should be carefully layed out. Enough current density in a narrow fingered transistors improves their speed.

The total gain of the Gilbert-Cell is also dependent on the current gain of the switching pair. Their function is to convey the AC current coming from the transconductance stage into the load. It is clear that the swing of the LO signal must be large enough to be able to fully commutate the current between both sides of the switches. The current gain is expressed as [31] [**?**] [32]:

$$C = \frac{2}{\pi}\left(\frac{sin(\pi\Delta f_{lo})}{\pi\Delta f_{lo}}\right) \tag{4.4}$$

where $\pi\Delta f_{lo}$ is proportional to the bias current of the switches and inversely proportional to their size. In other words, nearly ideal switching, i.e. $C = \frac{2}{\pi}$, can be achieved by either biasing the switching transistors with as small current as possible, or increasing their size. Increasing the size of the switches over a certain limit means that the parasitic capacitances increase, which leads to slow switching. On the other hand, although lower biasing current increases the switching speed, the gain of the transconductance stage is reduced due to reduced f_{max} of the transconductance devices. Thus, careful design must take care of both current and switching transistor sizes for optimal switching along with the minimum required LO power, which is also a very important design issue.

Fig. 4.4 shows one such optimization process of switching transistor size and bias current. Shown here are the open loop voltage values as a function of the switching transistor size for various bias currents. At lower values of the current it can be seen that the gain is limited by the transconductance transistors. Although at higher values of the biasing current higher gain values are expected, but unfortunately due to the low speed operation of the switching transistors at high bias current the gain is lowered. The rate of the gain decrease is larger than the increase in the transconductance introduced by $M1$ and $M2$. Optimum switch sizes are chosen such that they are wide enough to speed up the switching and at the same time they do not introduce large parasitic which decreases the gain. As shown in fig. 4.4, through this technique an optimum bias current value of 6.5 mA with 30 μm switching transistors has been chosen.

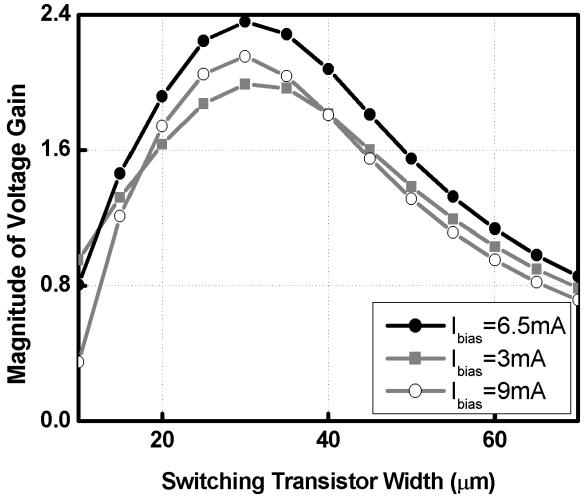


Figure 4.4: Simulated open loop gain versus switching transistor size for different bias current

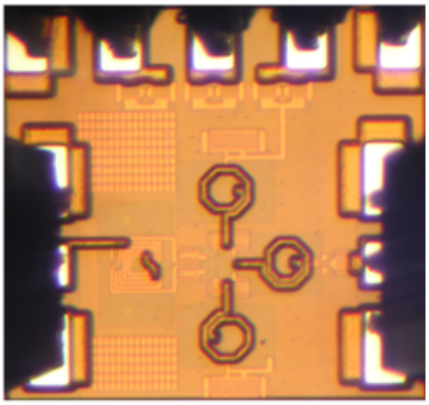


Figure 4.5: Chip micrograph of the realized Miller divider

4.2.2 Measurement Results

The circuit was fabricated using a standard 0.13 μm CMOS technology. The chip occupies a total area of 0.68 $\times$ 0.64 mm^2 including the RF and the DC probing pads. The chip micrograph is shown in fig. 4.5. The divider input signal which is driven in a GSG configuration is shown at the left side of the figure, while the output signal driving a 50 Ω load is on the right. Three biasing voltages are required (refer also to fig. 4.2): V_{dd}, V_{b1}, and V_{b2}; they are provided on the top of the chip. The single ended input is converted into differential signal through passive on-chip balun which in turn attenuates the input signal further by about 5 dB, meaning that the actual required input power is lower than the measured one by this amount.

Fig. 4.6 shows both the measured and simulated sensitivity and operation range of the divider. It can be seen that a minimum input power of 2 dBm is required for a frequency range from 24 GHz to 34 GHz. It is worth mentioning here that the divider fails to correctly divide at frequencies lower than 24 GHz, even though the input power is made much higher. This is as a result of the insufficient suppression of the third order harmonic. Similarly, division ceases above 34 GHz due to the insufficient loop gain, resulting in a bandwidth of 10 GHz.

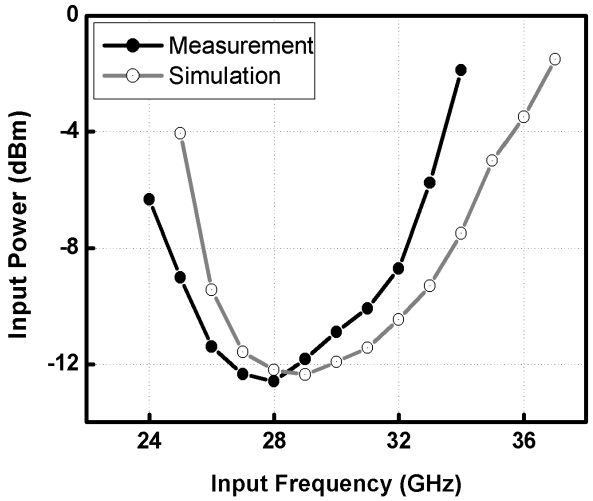


Figure 4.6: Input sensitivity of the Miller divider

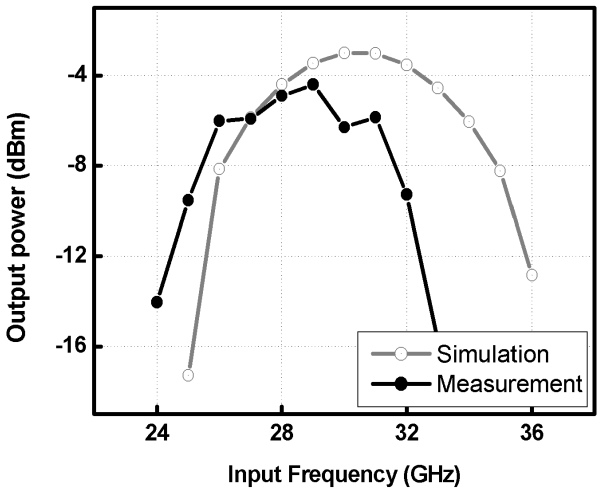


Figure 4.7: Output power of the Miller divider

Fig. 4.7 shows the measured and simulated output power as a function of the input frequency

range at an input power of 0 dBm. The output power values are better than -16 dBm for the whole frequency range. Finally, the output spectrum for input frequency of 28 GHz is plotted in Fig. 4.8. The spectrum shows a measured output power of -8 dBm at an output frequency of 14 GHz.

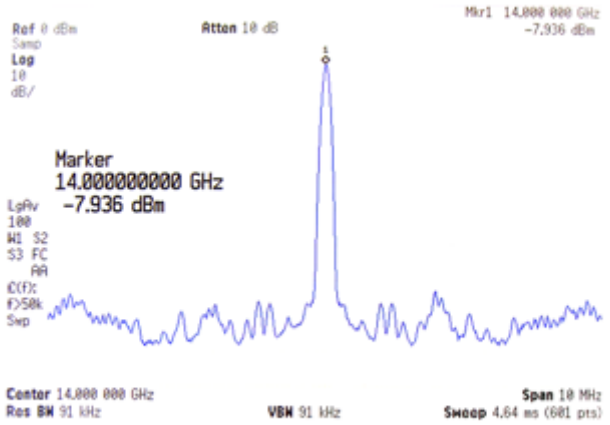


Figure 4.8: Spectrum analyzer's screen shot of the output power of the Miller divider

A comparison of the realized Miller divider with the state-of-the-art results is presented in Table 4.3. With a trade-off between the various critical divider performances including the chip area it can be seen that the realized circuit achieves a very good performance and is comparable to the best reported results.

Performance Parameter	This work	[10]	[33]
CMOS Technology (μm)	0.13	0.18	0.13
Frequency (GHz)	28	40	56.5-72.2
Frequency Range (GHz)	10.0	2.3	15.7
Division Ratio	2	4	2
Input Sensitivity (dBm)	-2	3	0
Output Power (dBm)	-16	-16	-20
Supply Voltage (V)	1.2	2.5	1.0
Power Dissipation (mW)	10.0	16.8	4.7
Chip Area (mm^2)	0.68×0.64	0.50×0.70	0.83×0.51

Table 4.3: Miller divider's performance comparison with the state of the art

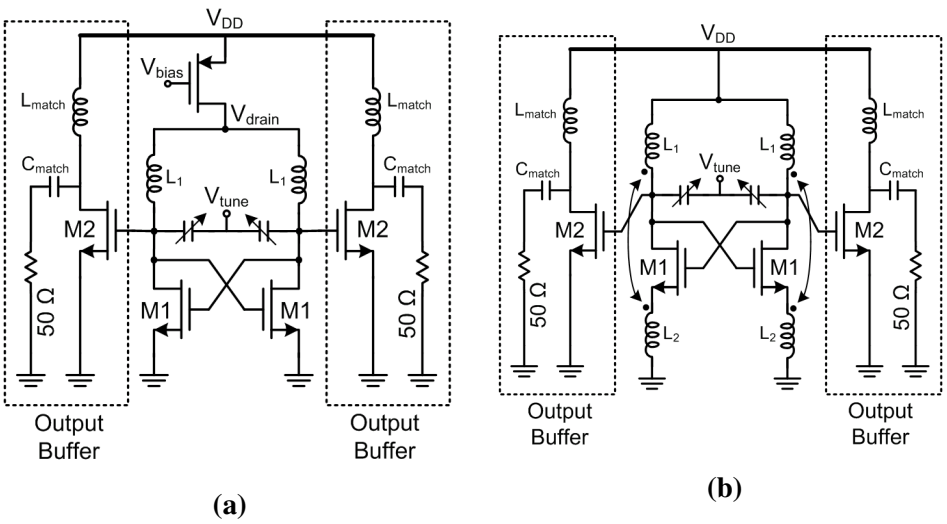


Figure 4.9: (a) Conventional NMOS VCO (b) Transformer Feedback VCO

4.3 Voltage Controlled Oscillator

4.3.1 Conventional and Transformer Feedback VCO's

There are three categories of the cross-coupled transistor VCOs; All PMOS, all NMOS, and a combination of NMOS and PMOS cross-coupled transistors. PMOS VCO topologies have many advantages over the other two in terms of phase noise for two reasons; first, the PMOS device has lower noise than the NMOS counterpart due to the fact that the latter has lower critical field, and thus suffers from velocity saturation more than the PMOS device. Second, the varactors are grounded through a low impedance at low frequency, thus the effect of the low frequency noise coming from the bias transistor is negligible [20]. However, the PMOS device has a much lower f_{max} than the NMOS device. This may lead to higher bias current and increased power consumption as a consequence of larger device size. Narrow tuning range and lower maximum oscillation frequencies are other disadvantages. In other words, with increasing operating frequencies the advantages of the PMOS VCO topologies are more and more lost. Thus, only NMOS transistors were considered. Fig. 4.9a shows a conventional NMOS VCO in

$W_s\ (\mu m)$	$W_1\ (\mu m)$	$W_2\ (\mu m)$	$C_{var}\ (fF)$	$L\ (pH)$	$V_{bias}\ (V)$	$V_{DD}\ (V)$
650	35	10	40 –130	350	1.1	1.2

Table 4.4: Circuit Parameters of the Conventional VCO

$W_1\ (\mu m)$	$W_2\ (\mu m)$	$C_{var}\ fF$	$L_1\ (pH)$	$L_2\ (pH)$	$V_{DD}\ (V)$
30	10	60–170	430	120	0.6

Table 4.5: Circuit Parameters of the Transformer Feedback VCO

which the headroom of the bias transistor limits the peak amplitude of the oscillation that further degrades the phase noise. A PMOS current source is used instead of the NMOS counterpart because of its better noise performance and to limit the tuning voltage to below V_{dd}. However, by utilizing a transformer between the source and drain terminals of the cross coupled transistor the bias transistor can be removed while keeping the VCO noise performance unchanged or even improved. This topology is called transformer feedback VCO (TFVCO) and is shown in fig. 4.9b. The bias noise source and its upconversion mechanism do not exist in the TFVCO. The transformer makes the drain and the source voltages in phase, thus enabling the oscillations to swing below zero [34]. The amount of peak drain voltage improvement is proved in [35] and is dependent of the turn ratio of the transformer. According to Leeson's formula shown below, the benefit is further enhancement of the phase noise at the same supply voltage, or equivalently, the same phase noise at much lower supply voltage.

$$L(f_m) = \frac{2KTR_{eq}F}{A_{o^2}} \left(\frac{f_o}{2Qf_m}\right)^2 \left(1 + \frac{\Delta f_{1/f^3}}{f_m}\right) \tag{4.5}$$

Switching transistors are another important source of noise, they not only contributing noise but converting it from different frequency bands to around the oscillation frequency by the AM-PM conversion mechanism. Nonlinearity of the switch transistors is the main cause of this conversion mechanism. It directly causes second and third harmonic to flow in the low impedance varactors. This causes the VCO to adjust the frequency to achieve the phase balance again. On the other hand, amplitude modulation of the bias modulates the harmonics, causing phase shift variation and hence frequency variation [36]. This effect exists only in the conventional NMOS VCO due to the existence of the bias transistor. The AM-PM conversion can however be minimized by minimizing the size of the switching transistors. The reasons can be explained as follows: Firstly, the overdrive voltage becomes higher; therefore, the device becomes more linear. Secondly, the bandwidth of the device becomes wider, thus higher order distortion decreases. Narrowing the

device width has an implication of increased overdrive and is limited by the voltage headroom needed by the bias transistor and the required transconductance needed to satisfy the conditions of oscillation.

According to Leeson's formula, phase noise is inversely proportional to the square of the oscillation's peak amplitude. This indicates that the phase noise performance of the conventional NMOS VCO is again better than that of the VCO which utilizes both NMOS and PMOS devices. Furthermore, the cross coupled PMOS transistors modulate more and more the varactors capacitance causing further degradation of the phase noise. Minimizing the size of the varactors may mitigate this influence but on the expense of the tuning range [37]. On the other hand, limited output swing of the NMOS and PMOS VCO not only impacts the phase noise but affects the output power that the VCO can deliver as well.

4.3.2 Design Approach

Fig. 4.9a shows a conventional NMOS VCO. It consists of two NMOS cross coupled transistors (M1 and M2) in order to generate the negative resistance needed to compensate for the losses of the LC tank. The value of this resistance is about $-1/g_m$. Its absolute value must be less than the equivalent parallel resistance of the LC tank at resonance so that the oscillations can start. This is particularly difficult at high frequencies because the core transistors cannot be large due to the capacitances they add to the tank. To accommodate core transistors with a sufficient width, the parasitic capacitances connected to the tank must be minimized. At a given operating frequency, the reduced parasitic capacitances also allow inclusion of larger varactors for a wider tuning range. The transistor size limitation can also be alleviated by increasing the Q factor of the tank to lower the losses. Therefore, low parasitic and high Q factor of the resonator circuit, as well as low parasitic and high gain transistor design is needed to increase the maximum VCO operating frequency. The Q factor of the tank not only determines the required transistor width and hence the maximum operation frequency but directly affects the phase noise performance as well.

On the other hand, the TFVCO topology (shown in fig. 4.9b) consists of transistors $M1$ and $M2$ which are also the cross coupled transistors producing the negative resistance to compensate

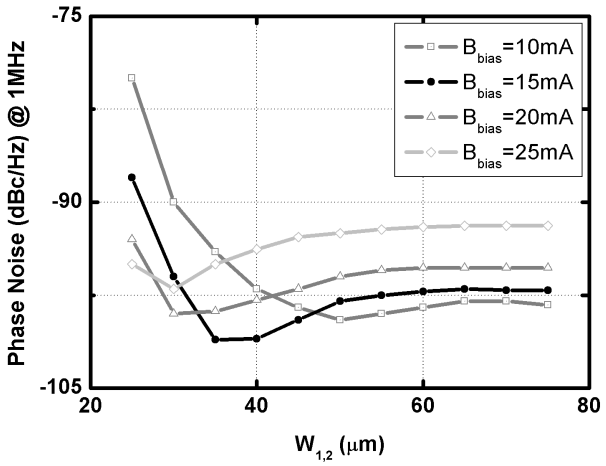


Figure 4.10: Simulated phase noise, at 25 GHz with 1 MHz offset, versus cross-coupled transistor width for different values of bias current

the tank losses. The required g_m is higher than that of the conventional NMOS counterpart for two main reasons: First, the cross coupled transistors are source degenerated by inductors that make the equivalent negative resistance at the same g_m value lower than the conventional one. Second, the Q factor of the transformer is lower than that of the normal inductor, thus higher losses and more g_m are required. To grantee oscillations at much lower supply voltage, the bulk can be biased to decrease the threshold voltage (V_t) of the transistor. To relax the g_m requirement, the transformer has to be carefully designed to attain high Q values.

Fig. 4.10 shows an approach to optimize the phase noise performance of the conventional NMOS VCO. For the switching transistor width $W_{1,2}$ below 25 μm, the VCOs fail to oscillate, especially at lower levels of bias current. On the other hand, increasing the transistor widths increase the parasitics and necessitates smaller varactors to maintain oscillation on the expense of tuning range reduction. As discussed before, to mitigate the effect of the AM-PM conversion caused by the cross coupled transistors, the width of the transistors must be decreased to improve their linearity, however, further decrease of the transistor width impacts their flicker noise. Below the optimum transistor width, the degradation of the flicker noise dominates the improvement of the AM-PM conversion. The best phase noise can be achieved at transistor a width of 35 μm and bias current of 15 mA. The minimum dimensions of varactors used are with 5 gates fingers and 6 active contacts (RX) repetitions for optimum Q factor and widest possible tuning range.

4.3.3 Measurement Results

The two VCO versions were fabricated in a standard 130 nm CMOS technology. Fig. 4.11 shows the tuning range of both VCOs. In the TFVCO larger varactors were used which lead to a wider tuning range at lower frequencies of oscillation. Chip micrographs of the conventional NMOS VCO and the TFVCO are shown in fig. 4.12 and fig. 4.13 respectively. The chip area is $0.55 \times 0.39\ mm^2$ for the conventional NMOS VCO, while the chip area of the TFVCO is $0.58 \times 0.49\ mm^2$ including RF and DC probing pads. For the TFVCO, the bulk of the transistors is connected to a positive voltage in order to allow deep supply down scaling as a result of lower threshold. Therefore, the conventional VCO consumes 23 mW while the TFVCO consumes only 6 mW with a supply voltage of only $0.6\,V$. The measured phase noise of both VCOs are shown in fig. 4.14. Measured and simulated phase noise of the conventional VCO compares to each other at 25 GHz; the size of the transistors is chosen such that the phase noise is optimum as depicted in fig. 4.10 and shown to be $-103\ dBc/Hz$ at an offset of 1 MHz which is the same as obtained in the measurements. The phase noise of the TFVCO is however 5 dBc/Hz worse because of the deep supply voltage down scaling. The transformer is shown in fig. 4.15, both primary and secondary inductor traces are drawn close to each other to increase their coupling coefficient. The patterned ground shield is inserted below the traces to minimize penetration of the field into the lossy substrate. The differential VCO output is probed using a GSSG configuration to drive the 50 Ω load. A common source buffer is used to isolate the VCO output nodes from the low impedance load and to deliver a reasonable amount of power to the output. Probes and cable losses are then de-embedded. A comparison between both versions is presented in table 4.6.

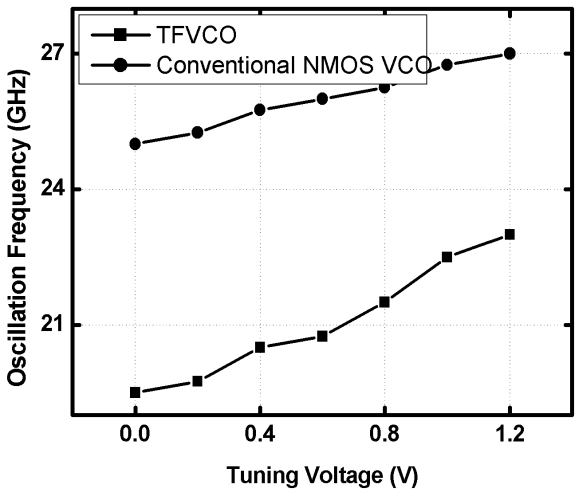


Figure 4.11: Measured tuning range of both conventional and TF VCOs

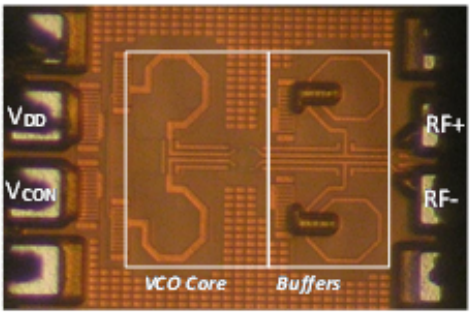


Figure 4.12: Chip micrograph of the all NMOS VCO

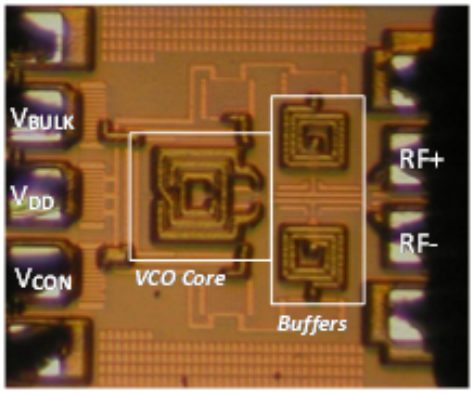


Figure 4.13: Chip micrograph of the Transformer feedback VCO

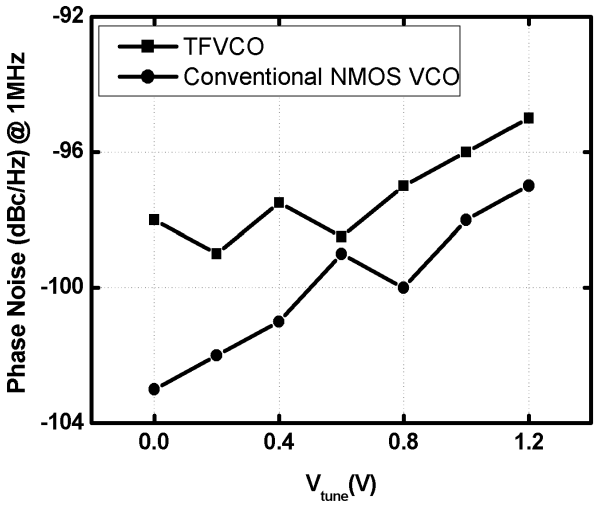


Figure 4.14: Measured phase noise at 1 MHz offset of both all NMOS and TF VCO

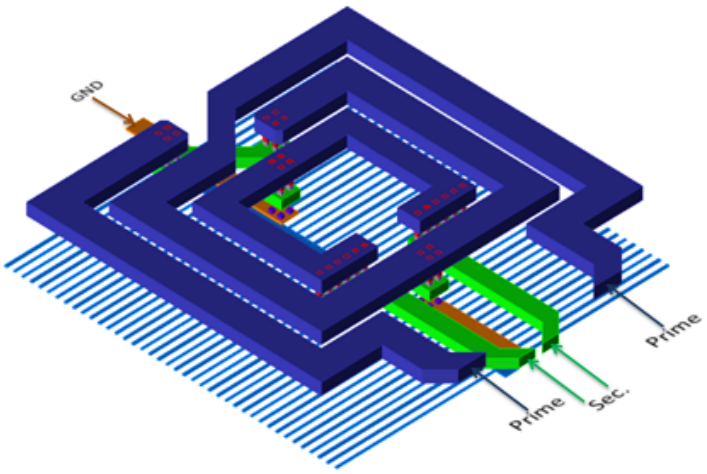


Figure 4.15: Layout of the Transformer, L1 and L2 drawn in the MA and E1 metal layer, respectively

Performance Parameter	This work Conv.	This work TF	[37] Conv.	[35] TF	[38] TF
CMOS Technology (μm)	0.13	0.13	0.13	0.18	0.13
Frequency (GHz)	26	22	59	24	24
Tuning Range (GHz)	1.7	3.7	5.8	0.6	2.2
Phase Noise (dBc/Hz)@$1MHz$	-97.5	-92.5	-89	-100	-113
Tuning Voltage (V)	$0 \Rightarrow 1$	$0 \Rightarrow 1.2$	$0 \Rightarrow 1.5$	$0 \Rightarrow 1.2$	$0 \Rightarrow 1.2$
Supply Voltage (V)	1.2	0.6	1.5	0.65	0.6
Output Power (dBm)	0.5	-3	-10	-13	-10
Power Dissipation (mW)	23	6	9.8	7.8	3
Chip Area (mm^2)	0.39×0.62	0.58×0.49	N.A	0.7×0.6	0.6×0.6

Table 4.6: Performance comparison of the two VCO versions with the state of the art

Chapter 5

Design of the IQ Modulator for the 60 GHz WLAN Transceiver

5.1 System Overview

The first stage of the short-range high data-rate transmitter according to the IEEE 802.15.3c PHY standard is the IQ-modulator (refere to fig. 1.4). The block diagram of the IQ-modulator is shown in fig. 5.1. The 40 GHz LO signal generated by the PLL is fed into the input of the static frequency divider (SFD) to provide wideband quadrature signals at 20 GHz. The direct up-conversion mixers translates the 2 GHz base-band signal into the IF range at around 20 GHz. The mixer outputs are combined together and fed to the IF amplifier whose input is matched to 25 Ω. The SFD operates at the four carrier frequencies as in Table 1.1 with a required input LO power of only 0 dBm.

5.2 Static Frequency Divider

5.2.1 Design Approach

The configuration of a SFD is shown in fig. 2.6. It is realized with two cross-coupled D flip-flops (D-FF), each D-FF is terminated with a small buffer. The two D-FF outputs toggle at every

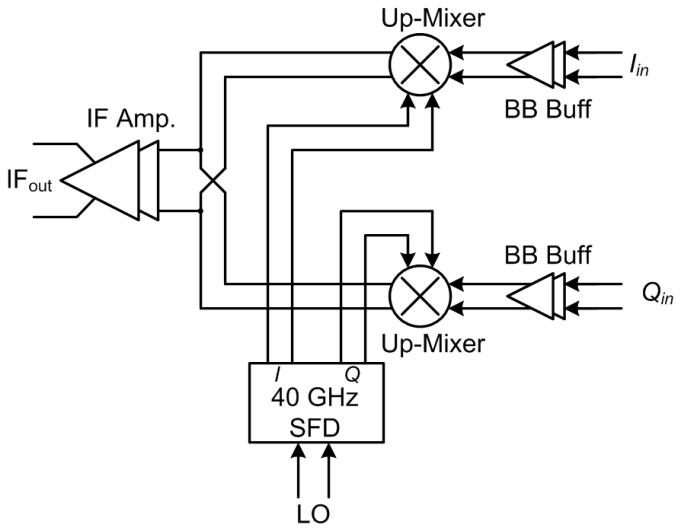


Figure 5.1: Block diagram of the IQ-Modulator

positive and negative going transitions of the clock, thereby generating two quadrature outputs at half the clock frequency. A high speed realization of D-FF is achieved through current-mode logic circuit (CML), using a sensitive differential amplifier or evaluating amplifier, shown in fig. 5.2, and a latching stage responsible for holding the state of the D-FF waiting for the next evaluation phase. During the positive half cycle of the clock, the differential sensor M_{eval} should be fast enough to correctly sample the input, and in the negative clock cycle, the latch circuit M_{latch} is switched on and latches the evaluated value.

Boosting the operation frequency of the SFD was always accomplished by using inductive peaking [14] and split resistors [15]. In this work these techniques are used to shorten the evaluation phase without boosting the gain of the evaluation amplifier or requiring high g_m of the latching devices. In the conventional shunt peaking, inductor and resistor were interchanged so that the inductor is connected directly to the latch drains. In this case the inductor parasitic capacitance to ground cannot be distinguished from the drain capacitance. As a result, the time constant also increases, reducing the latch speed. In this work (fig. 5.2) the inductor is inserted close to the supply. Moreover, stacked inductors could be used to preserve area. The inductor Q is not an issue as it is already in series with another resistor, so its resistive part could be absorbed into it.

In this approach, although having effect on each other, both the evaluating amplifier and

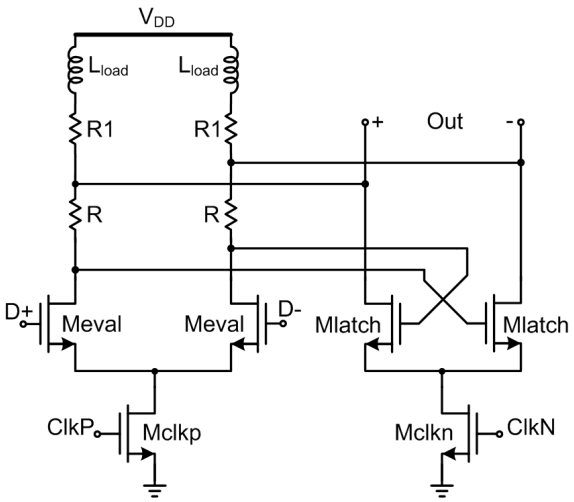


Figure 5.2: Circuit diagram of a single latch

W_{eval} (μm)	W_{latch} (μm)	W_{clkp} (μm)	W_{clkn} (μm)	L_{load} (pH)	R (Ω)	R1 (Ω)
24	6.4	30	15	800	40	20

Table 5.1: Circuit Parameters of the Latch Circuit

the latching circuits are considered separately. The loading of both on each other is taken into account during the design procedure. A design cycle is repeated for optimum sizing and current at the required frequency. The value of the load inductor is chosen such that it resonates with the latch devices' capacitances to oscillate at the free running mode. Splitting ratio is finally decided to provide the fastest possible charging and discharging response. Losses that are compensated by the latch transistors should be kept low to avoid extra current into the latch.

5.2.1.1 Evaluating Amplifier Design

As it becomes selective, the gain of the evaluating amplifier determines the operation range of the SFD; in other words, without using series resistors, gain of the evaluation amplifier is high enough over a narrow band, and thus it correctly evaluates the SFD state over a narrow band of frequencies. Choosing an optimum load resistor is a trade-off between the frequency band of operation and enough gain of the evaluating amplifier. The maximum load resistor value of 60 Ω is selected, so that the rising and falling times of the output nodes are short enough to follow the maximum required operation frequency; at the same time, gain is enough for the lower frequency edge. The design approach for minimum power can begin by selecting the appropriate size for

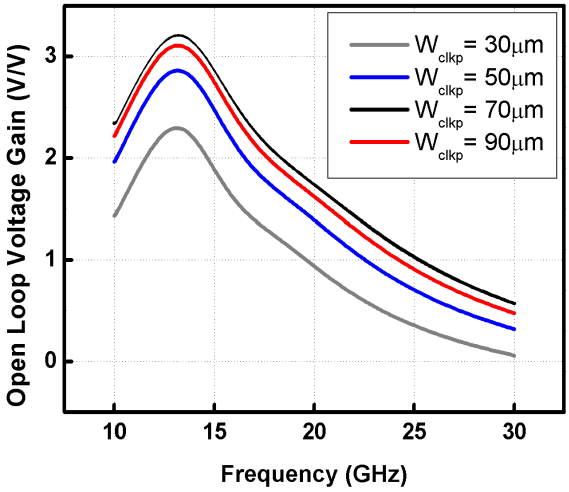


Figure 5.3: Open loop gain of the evaluating amplifier as a function of the tail current transistor size

M_{eval} to provide enough gain, recalling that its size does not significantly affect the speed of the latch [12] but its optimum size can be selected to fine tune the required f_{osc}.

Fig. 5.3 shows a family of gain curves corresponding to different sizes of M_{clkp}. Increasing the DC current boosts the gain of the evaluating amplifier and thus shifts the unity gain frequency upward. Removing the load resistor shifts the amplifier gain curve further up, but with a very narrow range of not more than 2 GHz. For deeper insight into the effect of the amplifier current on the SFD operation, fig. 5.4 shows the effect of M_{clkp} size on both current dissipation and f_{osc}. DC current is directly proportional to the device size M_{clkp}, it can be increased up the point at which the transistor goes into the linear operation. Although the f_{osc} also increases in proportion to current, it increases much slower at higher current. In other words, a couple of GHz can be achieved at the cost of doubling the current dissipation. A transistor M_{clkp} size of 30 μm is selected so that the current is 1.9 mA at an f_{osc} of about 20 GHz.

5.2.1.2 Sizing of the Latch Stage

During the latching phase, both (M_{latch} and M_{clkn}) should operate in saturation while the oscillation condition is satisfied (i.e.$R1 \cdot g_{mlatch} > 1$) and minimum possible latch transistor size for speed consideration. Remember that the losses of the low Q stacked inductor add up to the

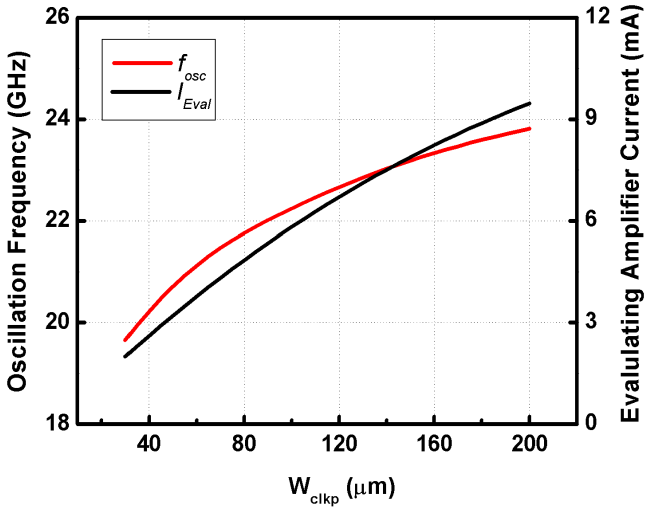


Figure 5.4: Self oscillation frequency of the SFD and evaluating amplifier DC current are proportional to the tail current transistor size

total losses of the load. A reasonable value for $R1$ is initially chosen, taking into account that the decrease of $R1$ might lead to a requirement of larger M_{latch}, thus pulling the frequency of operation down.

The current need not to be the same for the evaluation and the latch phases, the current for the latch network is actually independent of that drawn into the evaluation amplifier. Asymmetric input device sizes design saves much current that was not needed in the cross coupled transistors. Fig. 5.5 depicts the dependency of f_{osc} and the latch DC current on sizes of the cross coupled transistors M_{latch} and the negative clock transistor M_{clkn}. The current of the latch can not be decreased beyond a value that allows for full compensation of the load losses, thus oscillation was not possible at smaller transistor size M_{clkn}. Even higher f_{osc} can be achieved at lower latch current. According to fig. 5.5, M_{clkn} transistor size is chosen to be 15 μm at which the latching stage draws less than 1 mA . The M_{latch} transistor size of 6.4 μm is then selected to achieve the required f_{osc} of about 20 GHz.

5.2.1.3 Design of the Splitting Resistor Ratio

Starting from the fact that the two stage RC networks have shorter rising and falling times than that of single time constant networks, splitting the load resistor improves the setup time of the

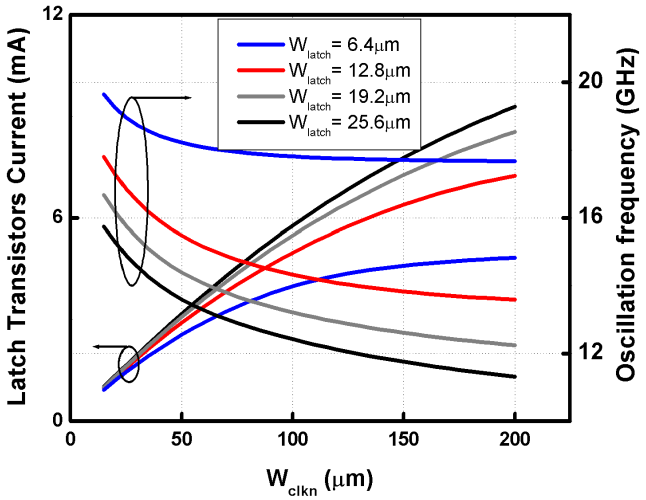


Figure 5.5: Self oscillation frequency and latching transistors DC current varies in accordance to both the tail current device size and cross coupled transistors size

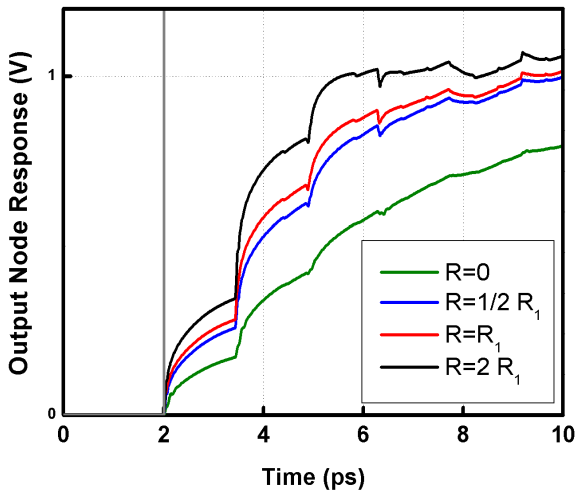


Figure 5.6: Step response of the SFDs output nodes for different splitting ratios of the resistive load

latch, thus increasing the maximum operation frequency [15]. A total load resistance is chosen to be 60 Ω. Lower values necessitate higher current in the latching stage to compensate losses. On the other hand, higher values increases the time constant of charging and discharging the output node capacitance, this slower response translating directly to prolonged setup time and thus decreased frequency of operation. Fig. 5.6 shows a step response of the output nodes for different splitting ratios. The procedure begins by keeping the total value of the load resistor

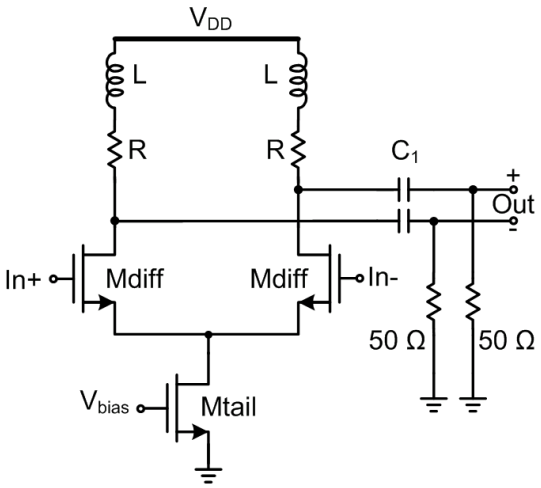


Figure 5.7: Circuit diagram of the output buffer

W_{tail} (μm)	W_{diff} (μm)	L_{load} (pH)	R (Ω)	V_{bias} (mV)
50	10	400	45	700

Table 5.2: Circuit Parameters of the Output Buffer Circuit

unchanged and distributing its value between $R1$ and R as shown in fig. 5.2. As R increases and $R1$ decreases by the same amount, the rise time improves. When R goes greater than $2 \cdot R1$, the SFD stops oscillating, as $R1$ is not enough to maintain oscillations (i.e. $R1 \cdot g_{mlatch} < 1$) and an excess current is needed to boost the latch transconductance. As shown in fig. 5.6, an improvement of about 50 percent of the rise time is achieved. The *RC* time constant circuit can even be split into three or more stages for further response improvement - complexity is a price that should be paid.

5.2.1.4 Output Buffers

This SFD is intended to be used as an IQ signal generator, thus both latches are made symmetrical and both of them are terminated with identical buffers. The buffers are used to isolate the output node of the SFD from the next stage and to provide the 50 Ω output impedance for measurement and integration purposes. Along the design procedure, the loading effect of the buffers on the latches should be taken into consideration, thus they are designed at the beginning and it is taken into account that their sizes should be kept as small as possible to save further power at the required frequency. Fig. 5.7 shows the buffer circuit. Inductive peaking of a resistively loaded

amplifier is a good choice, as it can provide bandwidth extension and can be easily matched. The current consumption of each is 0.5 mA.

5.2.2 IQ Imbalance

Due to integration difficulty or selectivity constraints, band pass filters in the receiver front end are not desired. Instead, image rejection mixers are adopted. In the single quadrature image rejection mixer of fig. 5.8, only the local oscillator signal is generated in I and Q paths. The IQ signal representation of the LO is, mathematically, one impulse at only positive or negative frequency; Thus, the RF signal is shifted down once to the right or to the left, respectively; thus, no overlap of the image over the wanted signal takes place. In reality, due to tolerances and devices mismatching, finite amplitude and phase imperfections exist, thus a residue of LO appears at the positive frequency, as represented in the equations below:

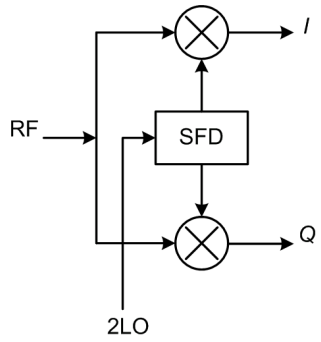


Figure 5.8: Single quadrature down-conversion mixer with a SFD as an IQ local oscillator signal generator

$$LO = A_{LO}e^{-j\omega_{LO}t} + A_{LOp}e^{j\omega_{LO}t} \tag{5.1}$$

$$LO = [A_{LO} + A_{LOp}]cos(\omega_{LO}t) - j[A_{LO} - A_{LOp}]sin(\omega_{LO}t) \tag{5.2}$$

Suppose now that the I and Q of the LO have gain and phase errors of ε and ϕ respectively. Then the LO could be modeled as follows:

$$LO = (1+\varepsilon)cos(\omega_{LO}t + \phi) - jsin(\omega_{LO}t) \tag{5.3}$$

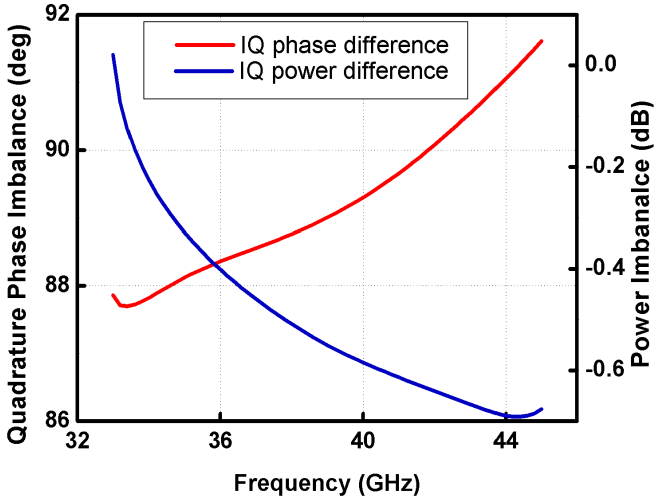


Figure 5.9: Simulated imbalance of IQ amplitude and phase

$$LO = [(1+\varepsilon)cos\phi]cos(\omega_{LO}t) - j[1+j(1+\varepsilon)sin\phi]sin(\omega_{LO}t) \tag{5.4}$$

Equating coefficients of 5.2 and 5.4 yield:

$$A_{LO} = \frac{1}{2}[1+(1+\varepsilon)e^{j\phi}] \tag{5.5}$$

$$A_{LOp} = \frac{1}{2}[-1+(1+\varepsilon)e^{-j\phi}] \tag{5.6}$$

The image rejection ratio IRR in dB can be calculated as follows:

$$IRR = 10log\left|\frac{A_{LO}}{A_{LOp}}\right| \tag{5.7}$$

$$IRR = 10log\left(\frac{1+2(1+\varepsilon)cos\phi+(1+\varepsilon)^2}{1-2(1+\varepsilon)cos\phi+(1+\varepsilon)^2}\right) \tag{5.8}$$

Fig. 5.9 shows the simulated IQ power and phase difference between the quadrature outputs. Maximum phase and power imbalance is 2.5 $^\circ$ and 0.7 dB, respectively. According to equation (8) the IRR is about 29 dB over the specified operation frequency range. The IRR is verified in fig. 5.10.

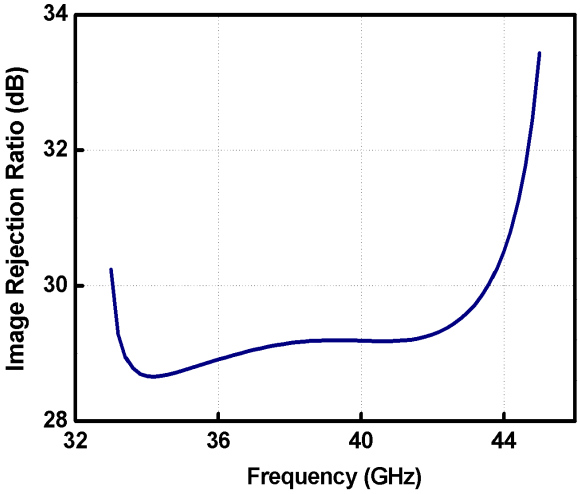


Figure 5.10: Simulated image rejection ratio due to the IQ imbalance

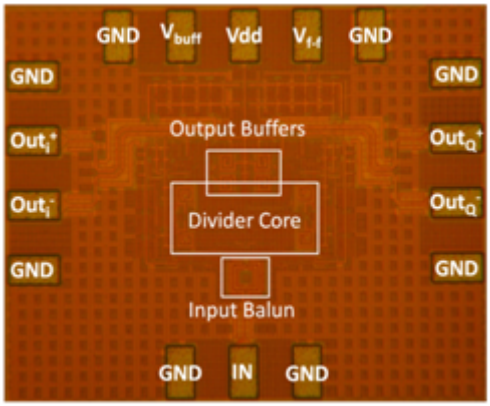


Figure 5.11: Chip micrograph of the SFD showing the pad configuration

5.2.3 Measurement Results

The circuit was fabricated in a 90 *nm* CMOS process. It occupies a chip area of $0.60 \times 0.75\ mm^2$ including probing pads. A micrograph of the frequency divider is shown in fig. 5.11. To ease the on-chip measurement, an on chip passive balun was also designed. A 50 GHz signal generator is used to generate the input. Two differential outputs are available, one is the In-phase and the other is the quadrature-phase outputs, one is terminated to 50 Ω while the other is to be measured. The output spectrum is measured with Agilent Spectrum Analyzer E4440A. With the 1.2 V power supply, the divider circuit draws a current of 6.8 *mA* including the output buffers.

The measured and simulated input sensitivity is shown in fig. 5.12. The cable losses, probe losses, and the on-chip balun loss have been de-embedded. With a -1 dBm input power, the

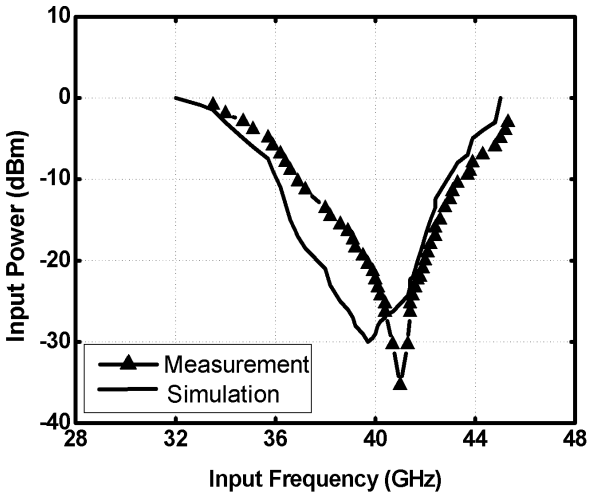


Figure 5.12: Simulated and measured sensitivity curve of the static frequency divider

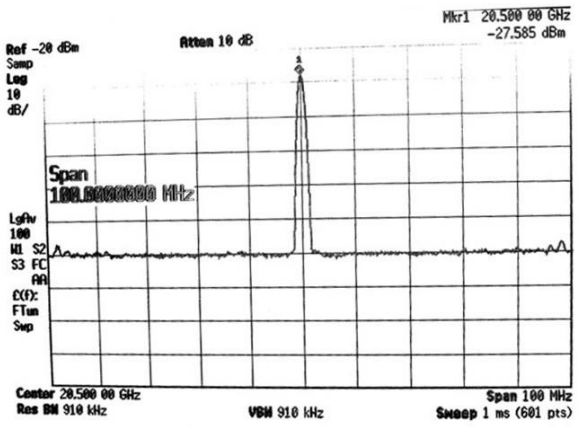


Figure 5.13: Spectrum of the free running SFD

circuit operation range is 12 GHz, from 33.5 GHz to 45.5 GHz. The divider self-oscillating frequency is 20.5 GHz. Fig. 5.13 shows the output spectrum when no input power is applied. Table I summarizes and compares the performance of the developed static divider with other recently published work. It can be noticed, that the power consumption is lowest among the others with comparable and higher operation frequencies. Due to the use of inductive peaking, the circuit becomes more selective, explaining the fact that the locking range is narrower but still sufficiently wideband for our application.

	This work	[12]	[13]	[14]
Technology (nm)	90	130	130	90
Supply (V)	1.2	1.5	1.2	1.2
Power Dissipation	6.9	9	8.4	15.7
Input Power (dBm)	-1	0	0	-1
Operation Frequency (GHz)	33.5 $\Rightarrow$ 45.5	5 $\Rightarrow$ 45	9 $\Rightarrow$ 34	49 $\Rightarrow$ 67
Output Power (dBm)	-16	N.A	N.A	N.A
Chip Area (mm^2)	0.60$\times$0.75	N.A	0.10$\times$0.20	0.68$\times$0.80

Table 5.3: Performance comparison of the SFD with the state of the art

	This work	[15]	[16]	[17]
Technology (nm)	90	90	130	130
Supply (V)	1.2	1.5	1.5	1.5
Power Dissipation	6.9	39.7	32	11.7
Input Power (dBm)	-1	0	N.A	6.5
Operation Frequency (GHz)	33.5 $\Rightarrow$ 45.5	4 $\Rightarrow$ 54	30 $\Rightarrow$ 43.2	31 $\Rightarrow$ 50
Output Power (dBm)	-16	N.A	N.A	N.A
Chip Area (mm^2)	0.60$\times$0.75	1.00$\times$1.00	0.63$\times$1.00	0.96$\times$1.15

Table 5.4: Performance comparison of the SFD with the state of the art

5.3 Direct Up-Conversion Mixer

The direct up-conversion mixer translates the base-band signal up to the IF frequency at 20 GHz. Due to the low frequency base-band signal, the output up converted signal lies in the vicinity of the LO signal frequency. Therefore, the isolation for the LO at the output should high. In other

words, the level of the LO at the IF port should be lower than the up-converted signal. In this sense, a double balanced mixer is used instead of single balanced structure. On the other hand, the IQ modulator should have high conversion gain to provide enough power to the front-end transmitter, thus a Gilbert-cell mixer is used instead of the passive counterpart.

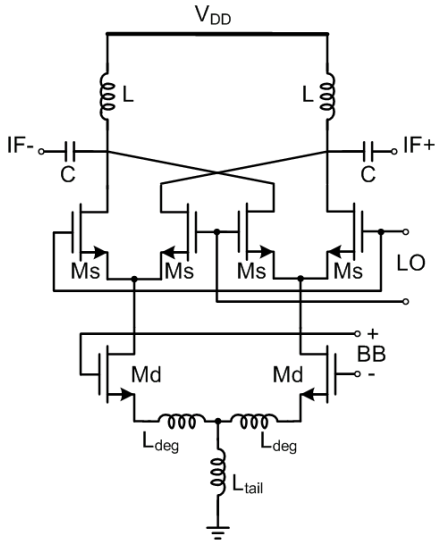


Figure 5.14: Circuit schematic of the up-conversion mixer

$W_d\ (\mu m)$	$W_s\ (\mu m)$	$L\ (pH)$	$C\ (fF)$	$L_{deg}\ (nH)$	$L_{tail}\ (nH)$
155	44	350	105	2	2

Table 5.5: Circuit parameters of the up-conversion mixer

Fig. 5.14 shows a circuit diagram of the up-conversion mixer. The linearity of the mixer is an important issue, especially for more complex modulation schemes where the difference in amplitude between symbols is small. The linearity of the mixer is determined by the transconductance stage. The third order intercept point can be shifted up by using a derivative superposition technique [39]. This method is effective only at a very low frequency, when the parasitics are negligible. In the range of the base-band signal, 2 GHz, it does not working anymore, as a result of the parasitic capacitances which degrade g_m of the driver transistors. The linearity of the up-conversion mixer is improved instead by inserting degeneration inductors. Degeneration shares the input power with the driver transistors (Md), degrading the conversion gain but boosting the compression point.

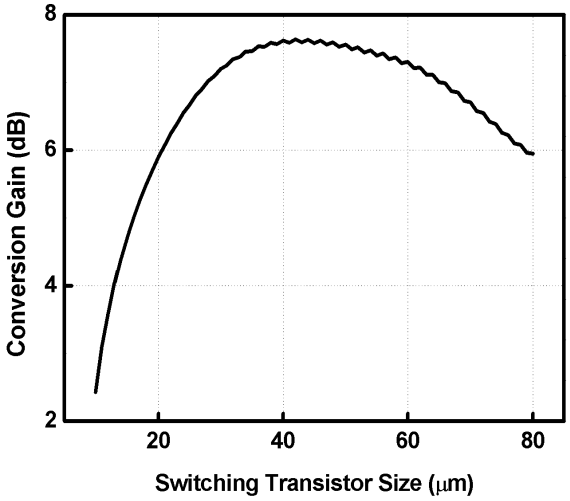


Figure 5.15: Simulation of conversion gain of the up-conversion mixer vs. the size of the switching transistors

5.3.1 Design Approach

Unlike the down-conversion mixers, direct up-conversion mixers do not need peaking inductors at the output nodes of the driver transistors. The capacitance at these nodes is small and most of the RF current flows through the switching transistors (Ms). Nevertheless, increasing the size of the Ms adds up extra capacitances causing more RF current to flow into the parasitic capacitances. Increasing transistor size (Ms) on the other hand results in less gate-source DC voltage and better switching behavior, and hence less loss of the switching transistor current gain. As a result, an optimum size of the switching transistors compromises the switching speed with the RF current loss in the parasitic capacitances. Fig. 5.15 shows an optimum switching transistor size of 44 μm.

Design of the driver transistor's size (Ms) determines directly the power consumption of the mixer as well as the conversion gain. In this design, (Md) is biased with gate voltage of 550 mV, so that the third current derivative is zero; this leads to a maximum possible third order intercept point. Load inductor L is chosen such that it provides maximum conversion gain at around the IF frequency of 20 GHz. The output is then matched to the 50 Ω load.

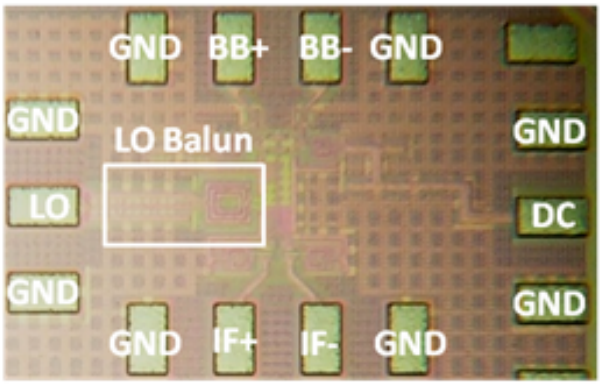


Figure 5.16: Chip micrograph of the up-conversion mixer

5.3.2 Measurement Results

The mixer was fabricated in a 90 nm CMOS process. It occupies an active area of $0.66 \times 0.42\ mm^2$ including probing pads. A micrograph of the Gilbert-Cell mixer with the proposed dynamic current bleeding network is shown in fig. 5.16. To ease the on-chip measurement, an on chip passive balun was also designed and connected to the LO port of the mixer; meanwhile, the RF input of the mixer can be driven single ended because of the tail common mode rejection inductor L_{tail}. Nevertheless, differential base-band signal was generated using off-chip balun and two couplers. Two 50 GHz signal generators are used to generate LO and BB signals. The differential output is probed using differential probe; one of single-ended output is terminated to 50 Ω while the other is connected to the input of the Agilent Spectrum Analyzer E4440A. The cable losses, probe losses, and the on-chip balun loss have been de-embedded. LO power is swept so that the best conversion gain is achieved, maximum gain corresponds to a LO power of 6 dB as shown in fig. 5.17, de-impeding the losses of the integrated passive balun results in an optimum LO power of 1 dBm. Best case conversion gain is 9.5 dB at LO frequency of 24 GHz and base band frequency of 1.5 GHz, measured and simulated conversion gain curves are shown in fig. 5.18. The 1 dB compression point is $-8\ dB$ as shown in fig. 5.19. With the 1.2 V power supply; the core Gilbert-Cell mixer draws a current of 6.3 mA. Tables 5.6 and 5.7 summarize the performance of the direct up-conversion Gilbert-Cell mixer and compare it with the state of the art results.

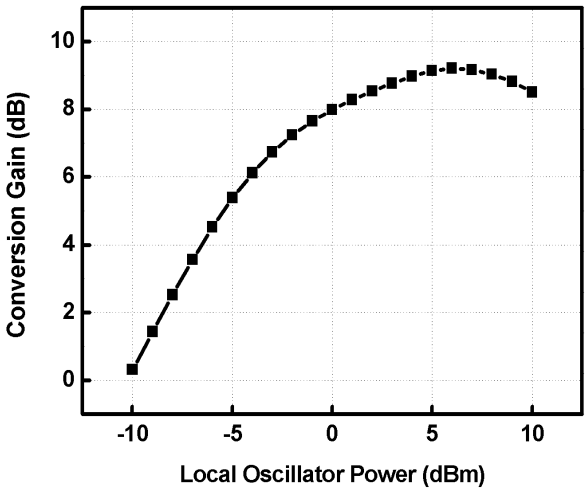


Figure 5.17: Optimum LO power for maximum conversion gain of the up-conversion mixer

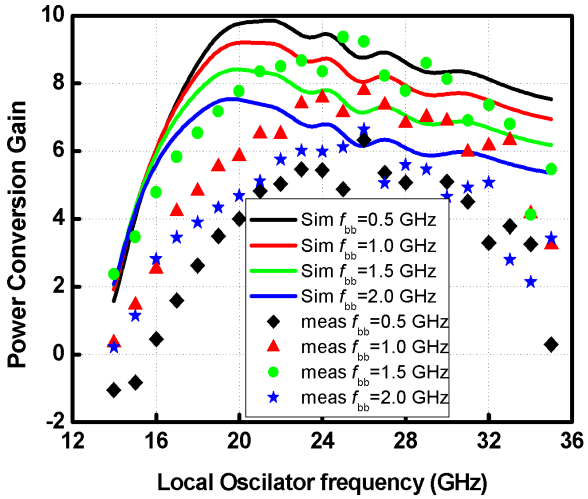


Figure 5.18: Conversion gain of the up-conversion mixer

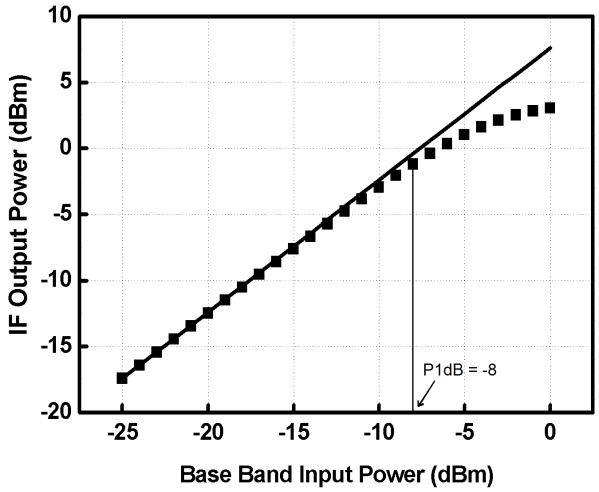


Figure 5.19: $P-1dB$ of the up-conversion mixer

	This work	[40]	[41]	[42]
Technology	90 nm	90 nm	0.13 μm	90 nm
Power Dissipation (mW)	7.56	13.2	8	11.1
Conversion Gain (dB)	9.5	-11	0.7	2
Optimum LO Power (dBm)	1	0	3	5
P_{1dB}(Input Referred) (dBm)	-8	1	-5.8	-14.8
LO Frequency (GHz)	$15 \Rightarrow 35$	40	$22 \Rightarrow 29$	$20 \Rightarrow 26$
Base-Band Frequency (GHz)	$0.01 \Rightarrow 2$	11 (IF)	$1.5 \Rightarrow 3.5$	2.7
Chip Size (mm^2)	0.66×0.42	0.60×1.05	0.68×0.68	0.65×0.57

Table 5.6: Summary and performance comparison of the direct up-conversion mixer

	This work	[43]	[44]
Technology	90 nm	0.13 μm	0.13 μm
Power Dissipation (mW)	7.56	24	2.7
Conversion Gain (dB)	9.5	4	-5.6
Optimum LO Power (dBm)	1	0	N.A
P_{1dB}(Input Referred) (dBm)	-8	-7	-14
LO Frequency (GHz)	$15 \Rightarrow 35$	$59 \Rightarrow 65$	$58.3 \Rightarrow 62.5$
Base-Band Frequency (GHz)	$0.01 \Rightarrow 2$	0.25	$0.05 \Rightarrow 3.5$
Chip Size (mm^2)	0.66×0.42	0.30×0.70	0.88×0.78

Table 5.7: Summary and performance comparison of the direct up-conversion mixer

5.4 IF Amplifier

5.4.1 Cascode Differential Amplifier

The IF signal is amplified before or after complex mixing in the demodulator or modulator respectively. A cascode differential amplifier is adopted in this design, as shown in fig. 5.20. Cascode configuration is better than the common source amplifier in this design. It partially trades-off the gain with better linearity, stability and isolation. The output of the IF amplifier is matched to 25 Ω in order for its output to be equally split between the two inputs of the mixers in the IQ-demodulator circuit, while its input is matched to 25 Ω to receive equal power from the mixer's outputs in the IQ-modulator circuit. Fig. 5.21 and fig. 5.22 show power gain and input output isolation of the IF amplifier, respectively. The power gain is 7 dB while the isolation is a bit less than -10 dB at the frequency of interest. The use of stacked inductors in the input and output matching circuitry makes them highly lossy, especially when it is needed to put extra fillers inside and near to the inductor traces. The effect of these fillers is not included in their EM model to speed up the simulation, and therefore there is a great difference between the simulated and measured gain, input, and output matching.

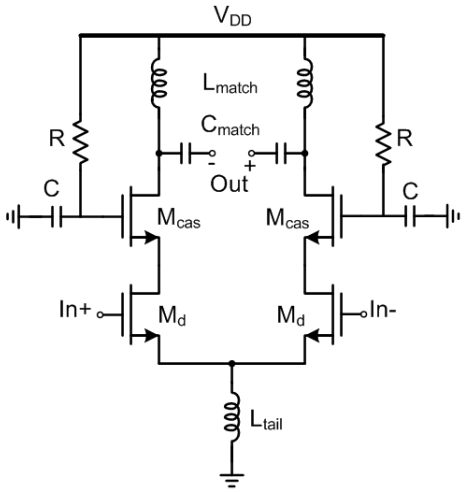


Figure 5.20: Circuit diagram of the cascode IF amplifier

$W_d\ (\mu m)$	$W_{cas}\ (\mu m)$	$L_{match}\ (pH)$	$C_{match}\ (fF)$	$C\ (fF)$	$R\ (K\Omega)$	$L_{tail}\ (nH)$
50	50	390	85	800	1	450

Table 5.8: Circuit parameters of the IF amplifier

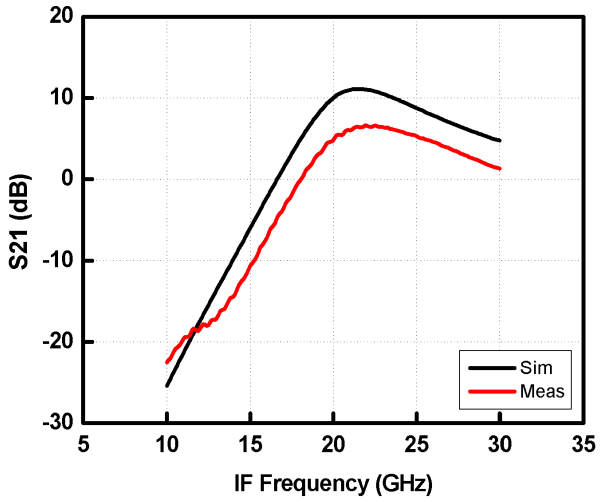


Figure 5.21: Power gain of the IF amplifier

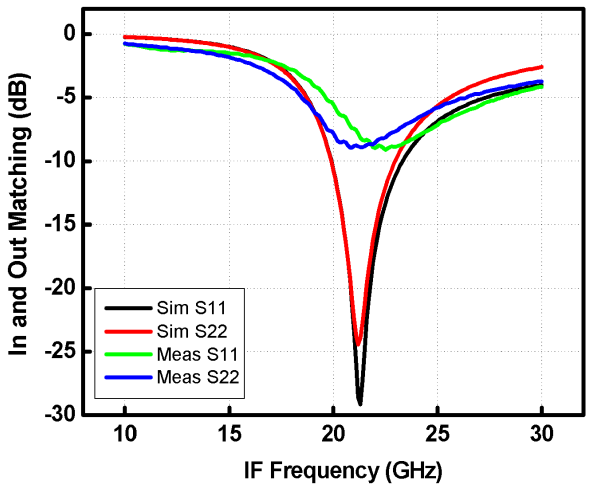


Figure 5.22: Input and output matching of the IF amplifier

5.5 System Integration

Referring to the IQ-Modulator block diagram of fig. 5.1, the mixer should be driven by an enough LO power in order to maintain the highest possible conversion gain. As shown in fig. 5.17, the optimum LO power required by the down-conversion mixer is 1 *dBm*, taking into account the

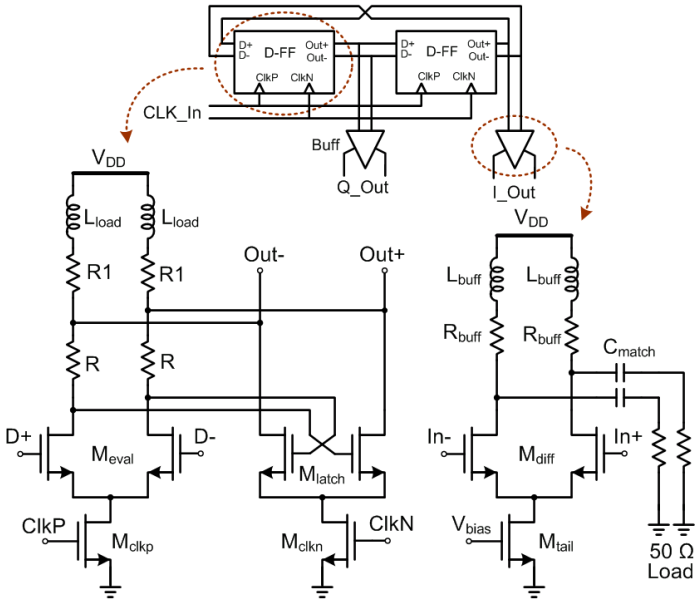


Figure 5.23: Frequency divider and IQ generator for the LO signal

losses of the balun, while the power delivered by the static frequency divider (SFD) is around $-16\ dBm$. In reality, the LO port of the mixer requires voltage swing rather than power level. According to simulations, the voltage swing of the SFD's output is 20 mV, and the required voltage swing that can fully switch the switching transistors of the mixer on and off is 150 mV. Therefore, an amplifier with the load inductor should resonate with the LO port's capacitor of the mixer at the required frequency of operation at around 20 GHz. The block diagram of the SFD and the circuit diagram of both the latch and the output buffer are shown in fig. 5.23; the output buffers are mainly used to isolate the output node of the latch from the high capacitance of the following stage, and to provide matching to the 50 Ω load. When it is integrated in the IQ-Demodulator, there is no need to design a matching network - its output node is directly fed into the gate terminals of the LO buffer of the mixer. The LO buffer, along with the direct down-conversion mixer, is shown in fig. 5.24. The load inductor of the LO buffer, L_{reso}, and the drain capacitance of the buffer from one side, and the gate capacitances of the switches from the other side, constitute a parallel LC resonance network, whose impedance is maximum at around 20 GHz, thus a maximum voltage swing of 450 mV is produced.

As shown in fig. 5.25, the chip micrograph of the complete IQ-Demodulator, the LO buffers are located very close to the LO port of the mixer. The I and Q outputs of the SFD are routed

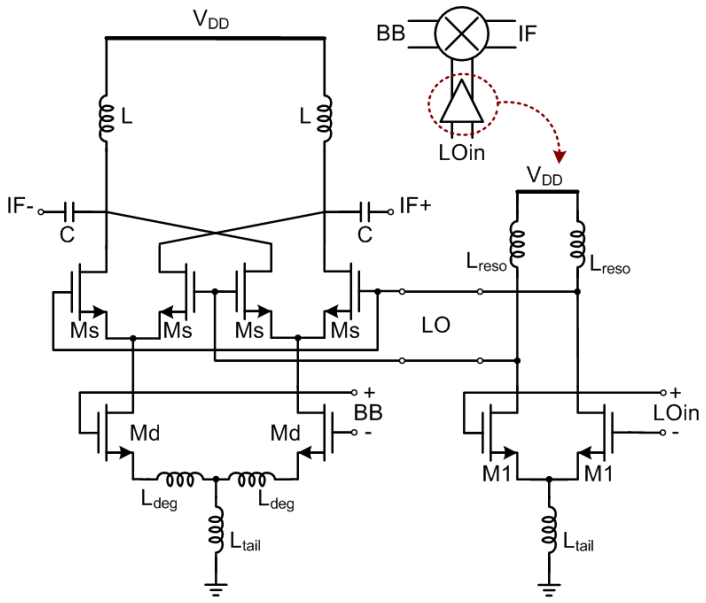


Figure 5.24: Circuit diagram of the up-conversion mixer with the LO buffer

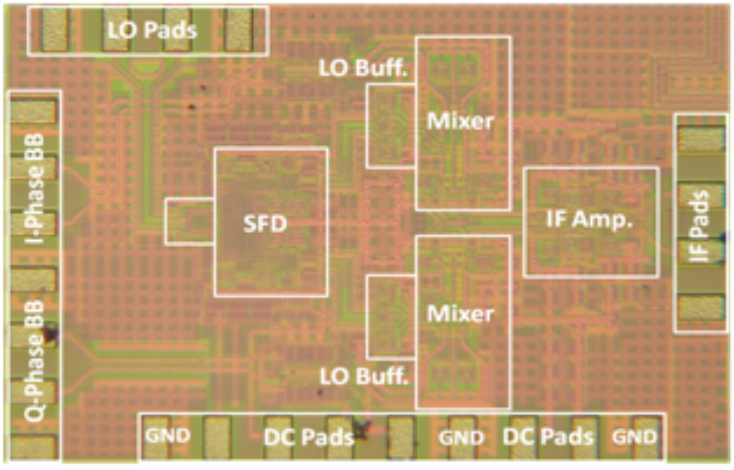


Figure 5.25: The chip micrograph of the IQ-Modulator showing circuit components and probing pads

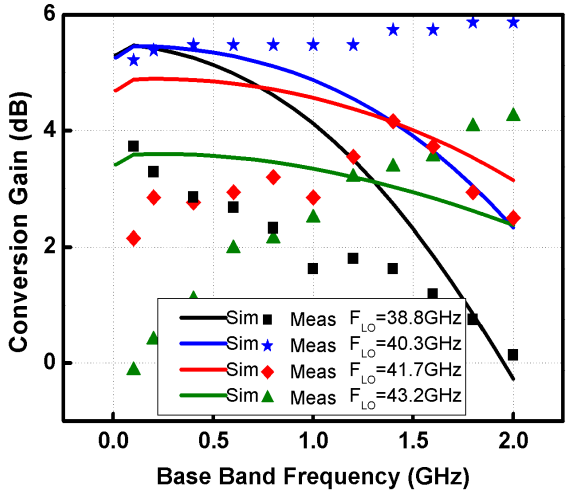


Figure 5.26: Conversion gain of the IQ-Modulator

using transmission lines. The input of the IF amplifier is matched to 25 Ω to receive equal power from the two sides of the IQ-demodulator's mixers.

The IQ-modulator has been fabricated in a TSMC 90 *nm* CMOS process. It occupies an active area of $0.82 \times 1.17\ mm^2$ including probing pads. A micrograph of the Modulator including inputs, outputs, and DC pads is shown in fig. 5.25. To ease the on-chip measurement, an on-chip passive balun was also designed and connected to the input of the SFD; meanwhile, an input balun followed by two line couplers are used to generate two differential quadrature signals to feed the base-band input terminals of the modulator. Two 50 GHz signal generators are used to generate LO and BB signals. The differential output is probed using a differential probe; one of single ended outputs is terminated to 50 Ω while the other is connected to the input of the Agilent Spectrum Analyzer E4440A. The cable losses, probe losses, and the on-chip balun loss have been de-embedded. The best case conversion gain is 6 dB at LO input frequency of 40 GHz and base band frequency of 2 GHz, measured and simulated conversion gain curves are shown in fig. 5.26. The $1-dB$ compression point is $-12\ dBm$. With the 1.2 V power supply, the complete IQ-Modulator consumes a total power of 42 mW including LO buffers and output matching buffers. Tables 5.9 and 5.10 summarize the IQ-demodulator performance and compares it to the state of the art.

	This work	[45]	[46]
Technology	CMOS 90 nm	0.13 μm	0.13 μm
Power Dissipation (mW)	42	75.9	39
Conversion Gain (dB)	6	-6	-6.5
Minimum LO Power (dBm)	-1	N.A	5
P_{1dB}(Input Referred) (dBm)	-12	N.A	-2.5
LO Frequency (GHz)	$33.5 \Rightarrow 45.5$	$20 \Rightarrow 32.5$	$50 \Rightarrow 70$
Base-Band Frequency (GHz)	$0.01 \Rightarrow 2.17$	15	1
Chip Size (mm^2)	0.84×1.15	0.98×0.80	1.08×0.65

Table 5.9: Summary and performance comparison of the IQ-Modulator

	This work	[47]	[48]
Technology	CMOS 90 nm	0.13 μm	90 nm
Power Dissipation (mW)	42	21	0
Conversion Gain (dB)	6	-8	-13
Minimum LO Power (dBm)	-1	4	4
P_{1dB}(Input Referred) (dBm)	-12	-20	
LO Frequency (GHz)	$33.5 \Rightarrow 45.5$	$30 \Rightarrow 65$	$50 \Rightarrow 62$
Base-Band Frequency (GHz)	$0.01 \Rightarrow 2.17$	N.A	0.1
Chip Size (mm^2)	0.84×1.15	0.89×0.56	0.85×0.6

Table 5.10: Summary and performance comparison of the IQ-Modulator

Chapter 6

Design of the IQ Demodulator for 60 GHz WLAN Transceiver

6.1 System Overview

As depicted in fig. 1.4, the IQ-demodulator translates down the IF frequency of 20 GHz, derived from the first down-conversion stage, to the base-band frequency range of 2 GHz in a complex form. The block diagram of the IQ-demodulator is shown in fig. 6.1. The I and Q signal imbalance determines the EVM of the received symbols, therefore, accurate IQ signal is highly demanded especially for high order modulation schemes. The static frequency divider is thus employed to grantee balanced IQ signal over the required wide band of operation. The IF output of the amplifier is matched to 25 Ω. The SFD can operate at the four carrier frequencies as in Table 1.1 with a required input LO power of only 0 dBm.

6.2 Low-Flicker Noise Direct Down-Conversion Mixer

6.2.1 Noise Mechanism and Current Bleeding Network

The dominant noise source of the mixer is the flicker noise of the LO switch stage because the IF signal is located at closed to DC frequency. The flicker noise of the mixers is generated by the

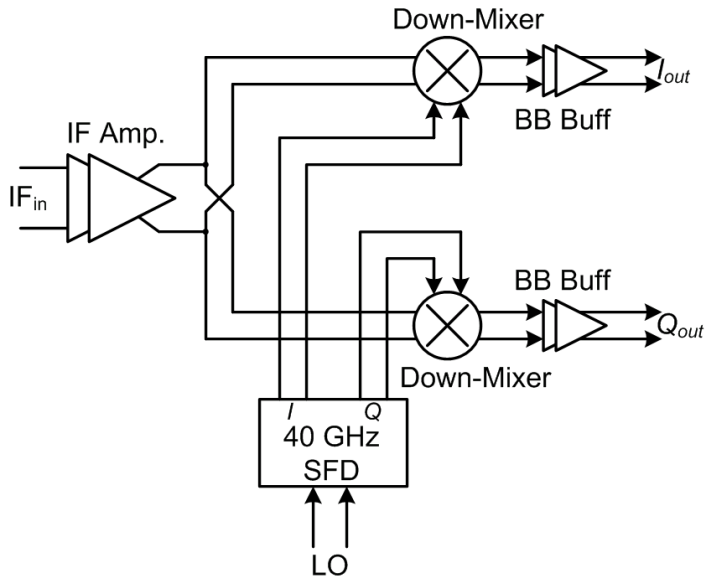


Figure 6.1: Block diagram of the IQ-Demodulator

transconductance stage, switching stage and load stage. Usually, the load stage does not have much effect on flick noise, in fact, flicker noise of the transconductance stage is converted to LO frequency. So flick noise of the mixer is mainly determined by the switching stage. The LO switches generate noise pulse trains by the direct mechanism and the DC average of noise pulse trains is the output flicker noise current as follows [22]:

$$i_{n,out(dir)} = \frac{4I \times V_n}{S \times T} \tag{6.1}$$

$$V_n = \sqrt{2 \times \frac{K_f}{WLC_{ox}f}} \tag{6.2}$$

$$S = \frac{V_n}{\Delta t} \tag{6.3}$$

Where I is the bias current for the RF transconductance stage, T is the LO period, V_n is the equivalent flicker noise of the switching pair and Δt is the slope of the LO signal. W and L are the effective width and length, C_{ox} is the oxide capacitance, f is frequency, and K_f is a process parameter.

In order to decrease flicker noise in the direct mechanism, the size of the switching pairs needs to be increased, and large switching devices increase the parasitic capacitance of the switching

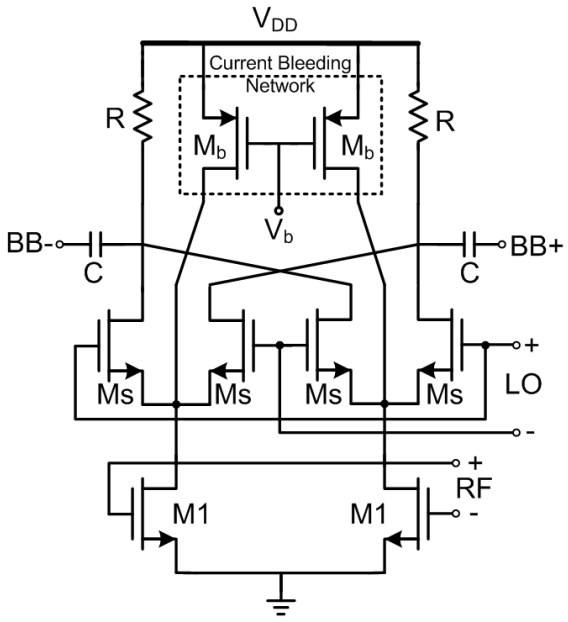


Figure 6.2: Gilbert-Cell mixer with conventional current bleeding network

pairs, resulting in the flicker noise indirectly translating to the output. The second mechanism that generates flicker-noise is the indirect mechanism, flicker-noise mainly depends on the tail capacitance (Cp) at the node between the LO switches and RF transconductance stage. In order to decrease the flicker noise in CMOS active mixers, the bias current of the local oscillator (LO) switches should be small enough to lower the height of the noise pulses [22].

$$i_{o,n(ind)} = \frac{2C_p}{T} V_n \times \frac{4I \times V_n}{g_{ms}^2 + (C_p \omega_{LO})^2} \tag{6.4}$$

Where C_p is the tail capacitance of the node between the LO switches and the RF transconductance stage, T is the LO period, g_{ms} is the transconductance of the LO switches, and V_n is the equivalent flicker noise of the switching pair. According to equation 6.4, the tail capacitance should be small enough to decrease the effect of the indirect mechanism. Therefore, a trade-off between direct and indirect mechanisms necessitates an optimum selection of the switching transistor size. In order to not design high gain low noise mixers, current bleeding networks are commonly used for the direct down-conversion mixers.

Usually, increasing the bias current through the switching stage can lead to a high gain and better linearity. However, when the current through the switching stage becomes higher, the

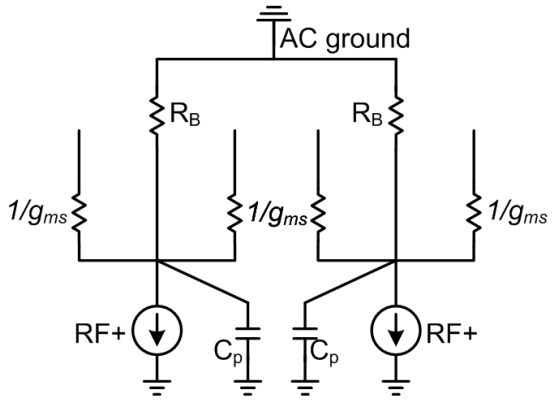


Figure 6.3: Equivalent circuit of the Gilbert-Cell mixer with conventional current bleeding mixer

voltage headroom problems of the load will be present. The current bleeding technique is usually adopted to reduce bias current through the switch, as shown in fig. 6.2. The equivalent circuit is shown in fig. 6.3. By current division, as can be seen from equation 6.5, some RF current flows into the bleeding circuit and it will decrease the conversion gain [22].

$$I_{LO} = \frac{R_B}{R_B + \frac{1}{g_{m1}(t)+g_{m2}(t)}} \times p_1(t) \times i_{RF} \tag{6.5}$$

On the other hand, the output noise current of LO switches is decreased as the bleeding current is increased. If the amount of the bleeding current is increased, the bias current of the LO switches is decreased. As we can see from equation 6.1, the noise current by the direct mechanism is then decreased. However, there are a few drawbacks with the conventional current bleeding technique. As the bias current of the LO switches is reduced, the impedance of the LO switches, as seen from the RF stage, is increased. Therefore, more RF leakage current will flow into the bleeding circuit, decreasing conversion gain. It also allows more RF current to be shunted by the tail capacitance as shown in fig. 6.3. Another drawback that makes this current bleeding network ineffective, is that the tail capacitance C_p increases, making the indirect noise mechanism dominate. The conventional current bleeding technique can reduce the bias current of the LO switches, but flicker noises are still generated by the indirect mechanism (tail capacitance). The tail capacitance C_p is still needed to be reduced. The best way to reduce the tail capacitance is to minimize the size of the LO switches and RF transconductance stages. However, CMOS transistors suffer

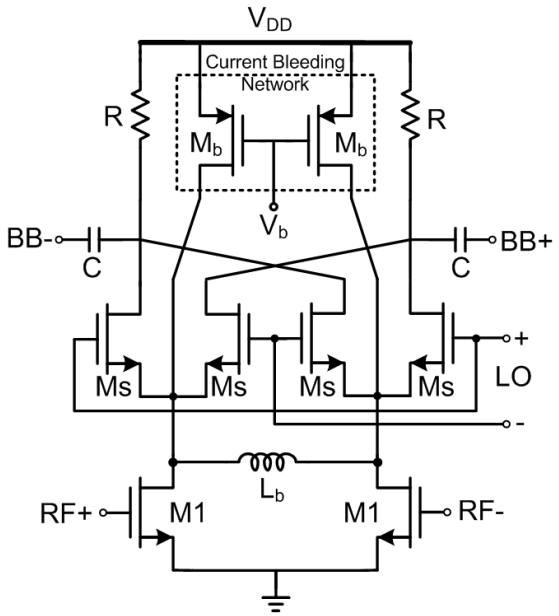


Figure 6.4: Gilbert-Cell mixer with static current bleeding network and one inductor

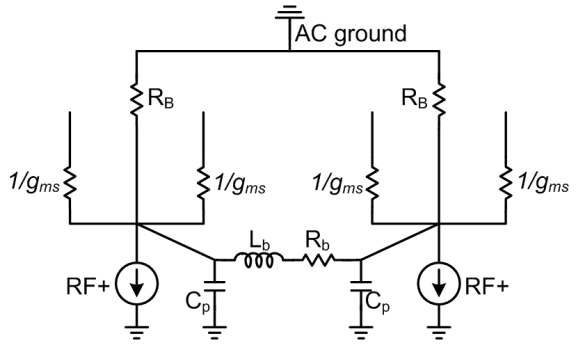


Figure 6.5: Equivalent circuit of Gilbert-Cell mixer with current bleeding and one inductor

from high intrinsic flicker noise, which is inversely proportional to the device area. Therefore, one inductor L is connected between the common source node of the LO switches, as shown in fig. 6.4, to resonate the tail capacitance out. In this way, the conversion gain and flicker noise performance are improved simultaneously under resonant condition. As shown in fig. 6.5, by resonating the tail capacitance with L, the impedance at node A looking into C_p can be high enough to protect some RF current from being shunted by the tail capacitance.

For the resonant circuit, the nonlinear capacitances are padded by the inductor and the

harmonics generated are reduced significantly. The admittance of the resonant circuit is:

$$Y_{in}(\omega) = j\omega_{RF}C_p + \frac{1}{j\omega_{RF}L} = j\omega_{RF}C_p\left(1 - \frac{1}{\omega_{RF}^2 LC_p}\right) \tag{6.6}$$

When the resonant frequency is at RF, the impedance at node A looking into C_p can be high enough to protect some RF current from being shunted by the tail capacitance. This increases the conversion gain by 2 to 3 dB. When the resonant frequency is at 2 RF, we have:

$$2\omega_{RF} = \frac{1}{\sqrt{LC_p}} \tag{6.7}$$

In this case the input admittance of the resonance circuit is $Y_{in}(\omega) = -j\omega_{RF} \cdot 3C_p$. Thus, the effective variation of C_p is reduced by a factor of 3, reducing the nonlinearity. This will improve the linearity. Setting the resonant frequency between RF and 2RF will make a good compromise between the conversion gain and linearity.

The static current injection technique was proposed to reduce the bias current of the LO switches. However, the impedance of the LO switches seen from the RF stage is increased as we reduce the bias current of the LO switches. In addition, RF leakage current flows through the injection circuit, which decreases conversion gain and also allows more RF current to be shunted by the tail capacitance (C_p) at the node between the LO switches and RF transconductance stage. Dynamic Current Injection (DCI) technique has been used in the mixer in order to reduce direct flicker-noise generation. As shown in fig. 6.6, two PMOS, Mb, were used to inject a dynamic current equal to the bias current of each pair of switches at only the switching event. Apart from the instant of switching, current can flow through the switches, reducing their impedance and thus lowering loss of the RF current. A parallel tuning inductor L has been employed to tune out the parasitic tail capacitances C_p to alleviate the indirect flicker noise source.

As shown before, by resonating the tail capacitance with L, the impedance at node A looking into C_p can be high enough to protect some RF current from being shunted by the tail capacitance. We have improved the conversion gain ranging from 2 to 3 dB in simulation by using one inductor. However, there are still two shunted paths for RF current leakage. One is the current bleeding

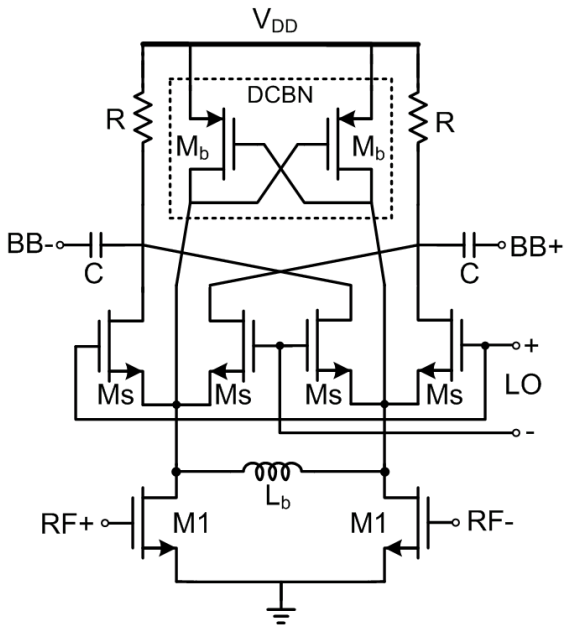


Figure 6.6: Gilbert-Cell mixer with dynamic current bleeding circuit and one inductor

circuit, and the other one is the shunted inductor. In this work, a current bleeding technique with two inductors connected between the common source node of the LO switches and the PMOS is proposed, as shown in fig. 6.7. Therefore, two inductors are connected to the PMOS device to resonate the tail capacitance out, and the conversion gain and flicker-noise performance are improved simultaneously under resonant condition. Another important role of these two inductors is to protect RF current flowing into the current bleeding circuit. This helps RF current flow into the mixer output directly. Therefore, we can achieve more conversion gain than the conventional current bleeding technique.

In the proposed design shown in fig. 6.7, parasitic capacitances of the dynamic bleeding transistors (M_b) are kept separated from the switches common sources by series resonating inductors (L). Therefore, the flicker noise due to the indirect mechanism is not increased; at the same time the DCBN provides the required DC current of the driver stage, minimizing the effect of the direct mechanism. The conversion gain is simultaneously improved, as there are only two paths for the RF driver current to ground: The source impedances of the switches, which is low during the LO period except for its zero crossings, and the resonance network, whose equivalent resistance is 300 Ω.

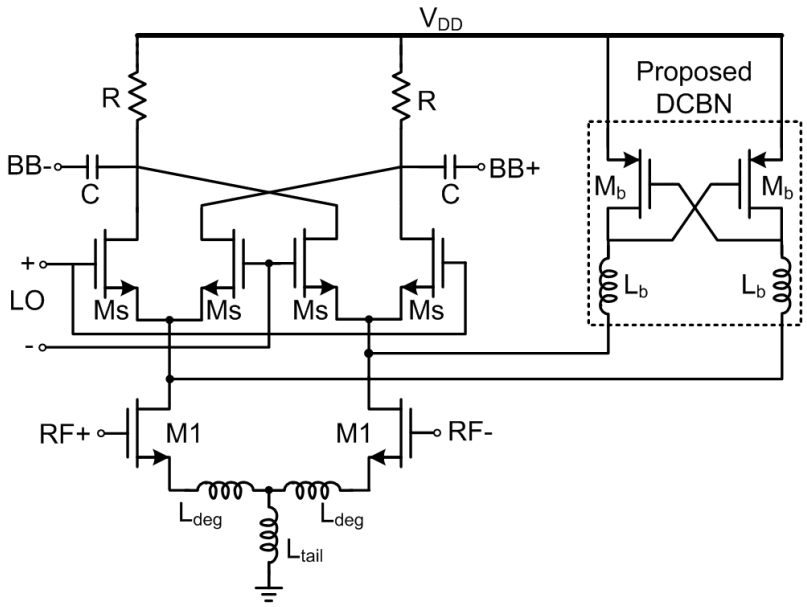


Figure 6.7: Gilbert-Cell mixer with the proposed dynamic current bleeding mixer and two inductors

W_1 (μm)	W_s (μm)	W_b (μm)	L_b (pH)	R (Ω)	I_{bias} (mA)	L_{deg} (pH)	L_{tail} (pH)
60	35	300	420	900	3.6	450	500

Table 6.1: Circuit Parameters of the direct down-conversion mixer

As shown in fig. 6.8, the resonating inductor (L) divides up the total tank capacitance into two series parasitic capacitances; drain and source capacitances of M_s and $M1$, and gate and drain parasitic capacitances of M_b. The series inductors (Ls) in this case are nearly four times larger than the shunt inductor (Lp) in the conventional DCBN for two reasons; firstly because every series inductor (Ls) resonating with the capacitances of only one side, secondly because the total parasitic capacitances are now series to each other instead of being shunted. In this design, Ls is 420 pH while Lp is 125 pH.

Improvement of the noise figure is shown in fig. 6.9. The output channel bandwidth is 10 MHz to 2 GHz while the LO frequency is set to 20 GHz. Both of the designs have the same M_s and M_b sizes, so that the flicker noise by the direct mechanism is the same. Nevertheless, with the proposed DCBN, the noise figure is improved by 8 dB more than the conventional one because of the enhancement of the flicker noise by the indirect mechanism, which resulted from splitting the capacitances at the common sources. Meanwhile, the conversion gain is also improved by

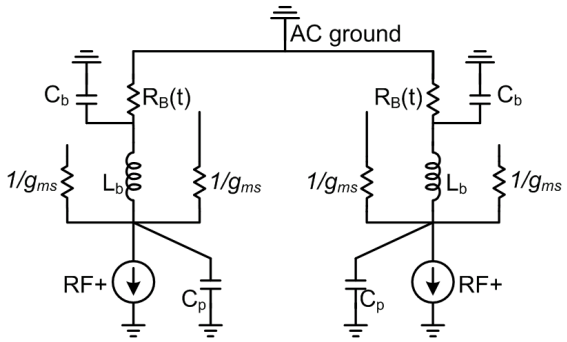


Figure 6.8: Equivalent curcuit of the Gilbert-Cell mixer with dynamic current bleeding network and two series inductors

an average of 6 dB. Driver transistors for both designs $(M1)$ are also made identical, but in the proposed design it is shown that more RF current is benefited in the switching transistors. Fig. 6.10 shows the conversion gain of both designs in the LO frequency range of 18 GHz to 23 GHz at the base band frequency of 1 GHz.

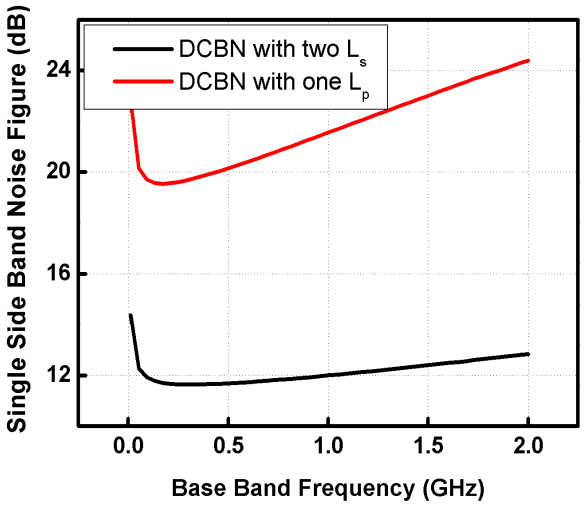


Figure 6.9: Simulated single side band noise figure of the Gilbert-Cell mixer with one shunt and two series inductors

6.2.2 Design Approach

Not only is flicker noise is the important issue in this design, but the linearity and power consumption are of great concern as well. To save power, the size and bias of the driver stage did not need to provide the maximum possible f_t or f_{max}. In this case, the current density of transistor

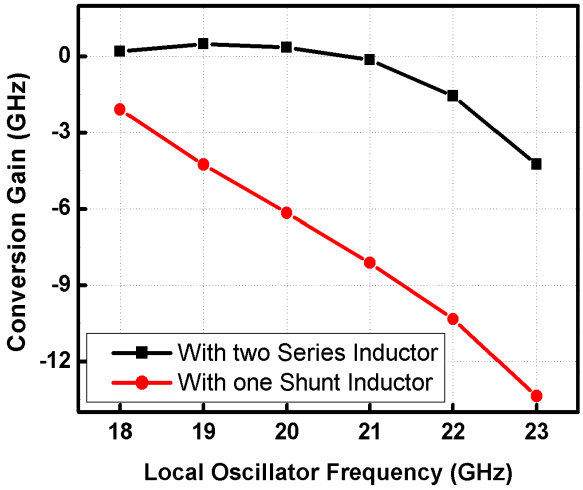


Figure 6.10: Simulated conversion gain of the Gilbert-Cell mixer with one shunt and two series inductors

$M1$ is chosen to be 36 $\mu A/\mu m$; this value provides a reasonable overall conversion gain of 4 dB when the switch transistors are optimized. The PMOS transistors of the DCBN (Mb) are sized so that they provide most of the driver DC current. The switches are biased so that they work in the deep saturation region yet have gate to source voltage that just above its threshold by 50 mV.

The total conversion gain of the mixer is proportional to the RF current gain of the switches from the driver stage to the highly ohmic resistive load, the current gain (C) is as follows [22]:

$$C = \frac{2}{\pi}\left(\frac{sin(\pi\Delta f_{LO})}{(\pi\Delta f_{LO})}\right) \tag{6.8}$$

Where Δ is the time interval in which all the switches are on. The current gain (C) approaches asymptotically the value of $2/\pi$ when Δ approaches zero; this situation can be achieved by biasing the switches so that they are hardly conduct current, and by increasing their size. With these biasing conditions, the switching transistors (Ms) conduct a very small amount of current of 150 μA and the LO voltage swing of 50 mV is enough to fully switch them off. Increasing the size of the switches further shunts more RF current to the common sources parasitic capacitances and causes the gain to drop. The optimum size of the switches is 35 μm as shown in fig. 6.11.

The bleeding transistors (M_b) should supply almost all of the DC current of the $M1$ transistors. They are cross-coupled transistors which should be large enough; therefore, their parasitic

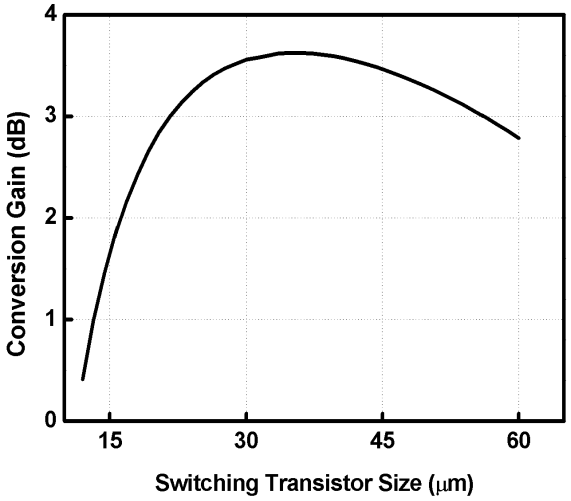


Figure 6.11: Simulated conversion gain of the Gilbert-Cell mixer versus the switching transistor size

capacitance is large compared to the Gilbert-Cell parasitic capacitances. These capacitances are separated from the common sources of the switches by adding series inductors. The inductors and the parasitic capacitances resonate at the RF input frequency to provide high ohmic path to the ground in parallel to the sources of the switches. The size of M_b is 300 μm while the inductor value is 450 pH.

The linearity of the mixer can be improved by inserting degeneration inductors (L_{deg}) whose impedance is compared to g_m of the driver transistors $M1$. L_{deg} is also used for stability and matching reasons. By using the degeneration inductors, the gain is reduced by 3 dB. Instead of using tail current source, which consumes voltage headroom and limits the output voltage swing, an inductor is used for rejecting common mode input. This makes it possible to apply single ended input instead of differential with very small gain loss. Stacked inductors are used to save area, nevertheless, they have lower quality factor and thus reduced gain.

6.2.3 Measurement Results

The circuit was fabricated in a 90 nm CMOS process. It occupies an active area of $0.44 \times 0.72\, mm^2$ including probing pads. A micrograph of the Gilbert-Cell mixer with the proposed dynamic current bleeding network is shown in fig. 6.12. To ease the on-chip measurement, an on chip

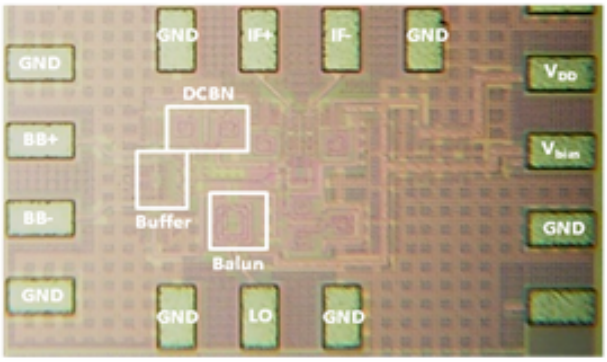


Figure 6.12: Chip micrograph of the direct down-conversion mixer with the proposed DCBN showing the pad configuration

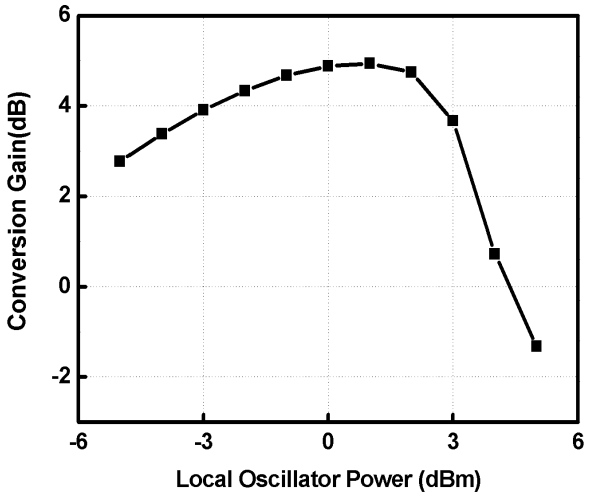


Figure 6.13: Measured conversion gain of the Gilbert-Cell mixer showing the optimum LO input power

passive balun was also designed and connected to the LO port of the mixer; meanwhile, the RF input of the mixer can be single ended driven because of the tail common mode rejection inductor L_{tail}. Two 50 GHz signal generators are used to generate LO and RF signals. The differential output is probed using a differential probe; one of single ended output is terminated to 50 Ω while the other is connected to the input of the Agilent Spectrum Analyzer E4440A through an off-chip coupling capacitor. The cable losses, probe losses, and the on-chip balun loss have been de-embedded. LO power is swept so that the best conversion gain is achieved, maximum gain corresponds to a LO power of 1 dB as shown in fig. 6.13, de-impeding the losses of the integrated passive balun results in an optimum LO power of -4 dBm. Best case conversion gain is 5 dB at LO frequency of 20 GHz and base band frequency of 500 MHz, measured and

simulated conversion gain curves are shown in fig. 6.14. The 1 dB compression point is -12 dB as shown in fig. 6.15. With the 1.2 V power supply; the core Gilbert-Cell mixer draws a current of 3.6 mA. Tables 6.2, 6.3, and 6.4 summarize the performance of the direct down-conversion Gilbert-Cell mixer with the proposed DCBN and compare it with the state of the art results.

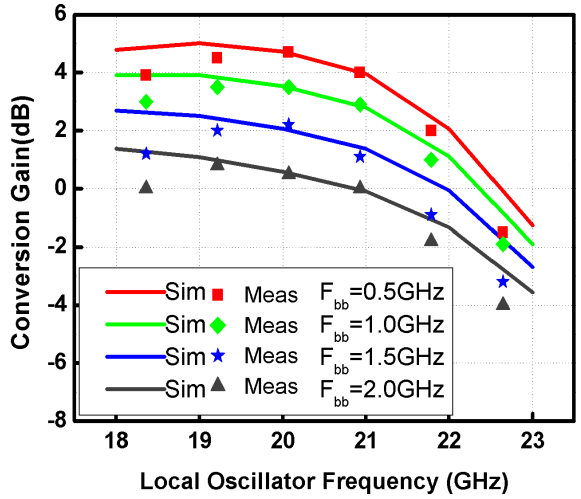


Figure 6.14: Measured and simulated conversion gain of the Gilbert-Cell down-conversion mixer with the proposed DCBN

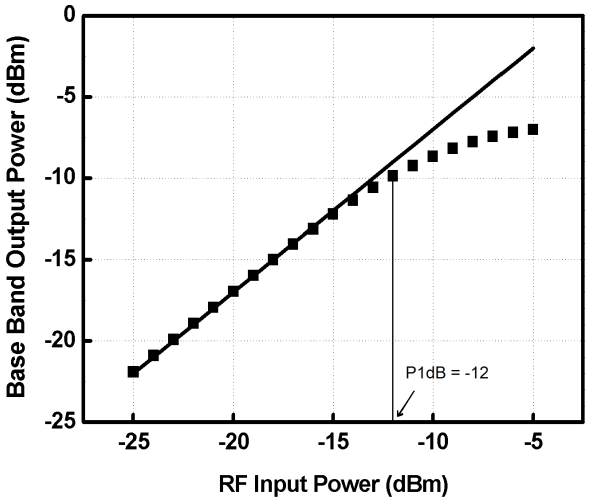


Figure 6.15: The $1-dB$ compression point of the Gilbert-Cell mixer with degeneration inductors

	This work	[49]	[50]
Technology	90 nm	0.18 μm	0.18 μm
Power Dissipation (mW)	4.3	10.8	44.7
Conversion Gain (dB)	5	15	28
Optimum LO Power (dBm)	-4	N.A	-5
P_{1dB}(Input Referred) (dBm)	-12	-14.2	-25
LO Frequency (GHz)	$18 \Rightarrow 23$	5.1	5.1
Base-Band Frequency (GHz)	$0.01 \Rightarrow 2$	0.1	N.A
Current Bleeding Network	Dynamic, two Ind.	Dynamic, one Ind.	Dynamic, one Ind.
SSB Noise Figure (dB)	12 (Simulated)	10.6	7.4
Chip Size (mm^2)	0.44×0.72	1.00×1.10	1.9×1.00

Table 6.2: Summary and performance comparison of the direct down-conversion mixer with the proposed DCBN

	This work	[22]	[51]
Technology	90 nm	0.18 μm	0.18 μm
Power Dissipation (mW)	4.3	7	14
Conversion Gain (dB)	5	16.2	27
Optimum LO Power (dBm)	-4	0	N.A
P_{1dB}(Input Referred) (dBm)	-12	-14	N.A
LO Frequency (GHz)	$18 \Rightarrow 23$	5.2	$4.8 \Rightarrow 5.7$
Base-Band Frequency (GHz)	$0.01 \Rightarrow 2$	N.A	$0.01 \Rightarrow 0.2$
Current Bleeding Network	Dynamic, two Ind.	Static, two Ind.	Dynamic, one Ind.
SSB Noise Figure (dB)	12 (Simulated)	9.8	7.8
Chip Size (mm^2)	0.44×0.72	0.78×0.98	1.11×1.30

Table 6.3: Summary and performance comparison of the direct down-conversion mixer with the proposed DCBN

	This work	[52]	[53]	[54]
Technology	90 nm	0.18 μm	90 nm	0.18 μm
Power Dissipation (mW)	4.3	5.65	38	5.2
Conversion Gain (dB)	5	8	10	18.7
Optimum LO Power (dBm)	-4	N.A	N.A	N.A
P_{1dB}(Input Referred) (dBm)	-12	-8.4	-18.5	-17.6
LO Frequency (GHz)	$18 \Rightarrow 23$	24	$21.6 \Rightarrow 27$	$20 \Rightarrow 25$
Base-Band Frequency (GHz)	$0.01 \Rightarrow 2$	0.05	N.A	N.A
Current Bleeding Network	Dynamic, two Ind.	Static, one Ind.	–	–
SSB Noise Figure (dB)	12 (Simulated)	12.6	11	18
Chip Size (mm^2)	0.44×0.72	1.1×0.98	1.0×0.98	0.18

Table 6.4: Summary and performance comparison of the direct down-conversion mixer with the proposed DCBN

6.3 System Integration

Referring to the IQ-demodulator block diagram of fig. 6.1, the mixer should be driven by enough LO power in order to maintain the highest possible conversion gain. As shown in fig. 6.13, the optimum LO power required by the down-conversion mixer is -4 dBm taking into account the losses of the balun, while the power delivered by the static frequency divider (SFD) is around -16 dBm. In reality, the LO port of the mixer requires voltage swing rather than power level. According to simulations, the voltage swing of the SFD's output is 20 mV, and the required voltage swing that can fully switch the mixer's switching transistors on and off is 50 mV. Therefore, an amplifier's load inductor should resonate with the LO port capacitor of the mixer at the required frequency of operation around 20 GHz. The block diagram of the SFD and the circuit diagram of both the latch and the output buffer are shown in fig. 6.16; the output buffers are used mainly to isolate the output node of the latch from the high capacitance of the following stage, and to provide matching to the 50 Ω load. When it is integrated in the IQ-Demodulator, there is no need to design a matching network, its output node is directly fed into the gate terminals of the LO buffer of the mixer. The LO buffer, along with the direct down-conversion mixer, is shown in fig. 6.17. The load inductor of the LO buffer, L_{reso}, and the drain capacitance of the buffer from one side, and the gate capacitances of the switches from the other side, constitute a parallel LC

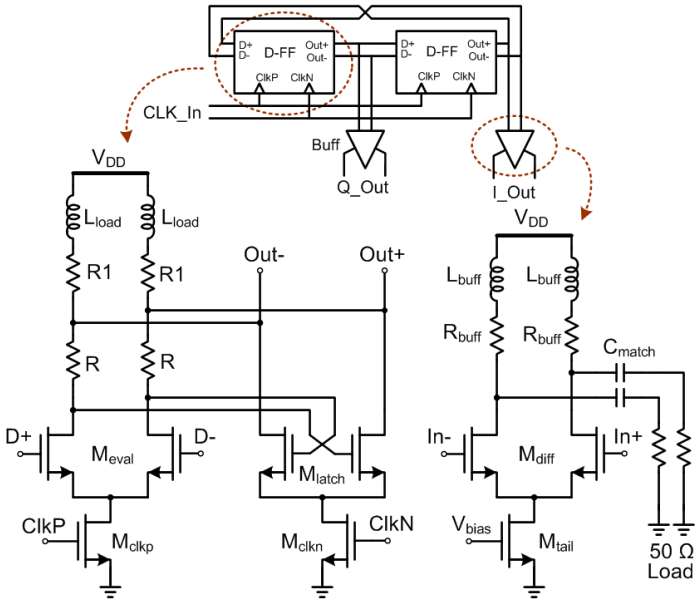


Figure 6.16: Frequency divider and IQ generator for the LO signal

resonance network, whose impedance is maximum at around 20 GHz, thus a maximum voltage swing of 400 mV is produced.

As shown in fig. 6.18, the chip micrograph of the complete IQ-Demodulator, the LO buffers are located very close to the LO port of the mixer. The I and Q outputs of the SFD are routed using transmission lines. The output of the IF amplifier is matched to 25 Ω to equally divide its output power between the two sides of the IQ-demodulator's mixers.

The IQ-Demodulator has been fabricated in a TSMC 90 nm CMOS process. It occupies an active area of $0.84 \times 1.15\ mm^2$ including probing pads. A micrograph of the Demodulator including inputs, outputs, and DC pads is shown in fig. 6.18. To ease the on-chip measurement, an on chip passive balun was also designed and connected to the input of the SFD; meanwhile, the IF input of the IF amplifier can be driven single ended because of the tail common mode rejection inductor. Two 50 GHz signal generators are used to generate LO and IF signals. The differential output is probed using a differential probe; one of single ended outputs is terminated to 50 Ω while the other is connected to the input of the Agilent Spectrum Analyzer E4440A through an off-chip coupling capacitor. While the other differential output is left unconnected. The cable losses, probe losses, and the on-chip balun loss have been de-embedded. Best case conversion gain is 6 dB at LO input frequency of 40 GHz and base band frequency of 500 MHz;

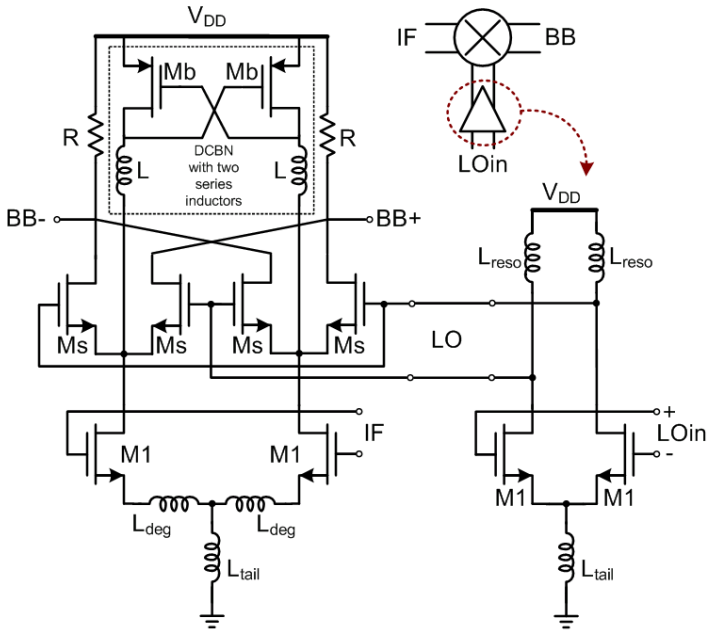


Figure 6.17: Down-conversion mixer with the LO buffer

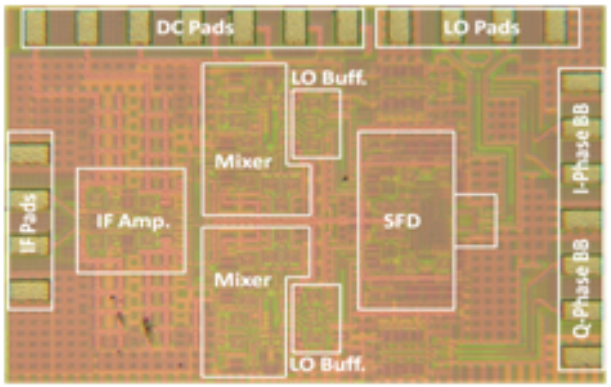


Figure 6.18: The chip micrograph of the IQ-Demodulator showing circuit components and probing pads

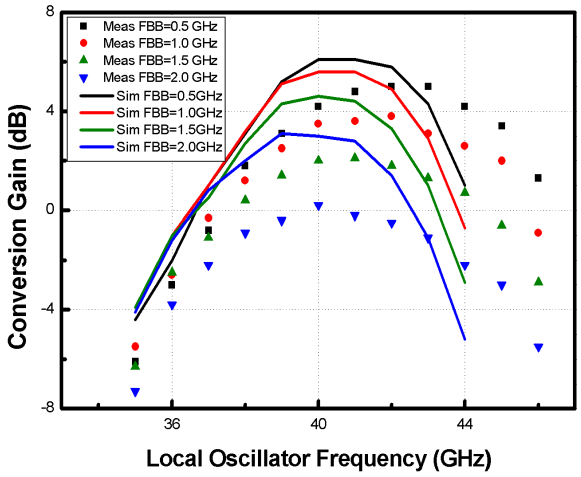


Figure 6.19: Conversion gain of the IQ-Demodulator

	This work	[56]	[55]
Technology	CMOS 90 nm	CMOS 90 nm	CMOS 0.13 μm
Power Dissipation (mW)	50	73	N.A
Conversion Gain (dB)	6	20	-3
Minimum LO Power (dBm)	-1	N.A	8
P_{1dB}(Input Referred) (dBm)	-12	N.A	6
LO Frequency (GHz)	$33.5 \Rightarrow 45.5$	$8.5 \Rightarrow 9.5$	$35 \Rightarrow 50$
Base-Band Frequency (GHz)	$0.01 \Rightarrow 2.17$	N.A	0.01
Chip Size (mm^2)	0.84×1.15	1.05×0.98	0.9×1

Table 6.5: Summary and performance comparison of the IQ-Demodulator

measured and simulated conversion gain curves are shown in fig. 6.19. There are two main reasons causes differences between measured and simulated results: The first is the lossy stacked inductors with relatively low Q factors due to the existence of the fillers, these fillers are not included in the EM model to save the simulation run time. The second is the insufficient power delivered to the LO port of the mixer over the wide frequency range. The $1-dB$ compression point is $-12\ dBm$ with the $1.2\ V$ power supply. The complete IQ-Demodulator consumes a total power of $50\ mW$ including LO buffers and output matching buffers. The relatively low linearity compared to [55] is due to minimum power requirements and the elevated conversion gain value. Table 6.5 summarizes the IQ-demodulator performance and compares it to other state of the art demodulators.

Chapter 7

Conclusions

In this dissertation, new techniques and optimized topologies are proposed to improve the performance of mm-wave frequency generation and conversion circuits. Employing a transformer-feedback topology, a 24 GHz LC-VCO was designed using 130 nm CMOS technology. It achieves a tuning range of 3.7 GHz and consumes only 6 mW which is one fourth of the power that the conventional LC-VCO needs. The designed transformer-feedback VCO has a phase noise of -92.5 dBc/Hz at an offset frequency of 1 MHz which is comparable to that of the conventional counterpart. Two designs of frequency divider have also been presented. One design is a Ka-band Miller frequency divider in 130 nm CMOS technology. A specific optimization approach was followed to achieve a maximum achievable locking range of 10 GHz at a 10 mW of power consumption and a maximum required input power of -2 dBm. The other design, on the other hand, is a 45 GHz static frequency divider using 90 nm CMOS technology. New techniques such as inductive peaking, split resistors, and asymmetric sizing of input transistors are employed to minimize the power consumption of the divider. The locking range of the static divider is 12 GHz, while it consumes only 6.9 mW and requires an input power of 0 dBm as minimum. Moreover, direct down-conversion mixer is investigated and designed. The Flicker noise effect is challenging. New current bleeding network was therefore proposed, not only the noise performance is improved but the conversion gain is increased as well. The noise figure of the mixer is 12 dB, the conversion gain is 5 dB at a power consumption of 4.3 mW, and an optimum LO signal power of -4 dBm.

Based on the designed static frequency divide, the direct down-conversion and up-conversion mixers, complete IQ-modulator and demodulator were eventually demonstrated in 90 nm CMOS technology. It is targeted at a 60 GHz super-heterodyne transceiver for high-data-rate communication application. Measurement results show that the IQ-demodulator operates with a LO frequency of 33.5 to 45.5 GHz, it achieves a conversion gain of 6 dB at a power consumption of only 50 mW. This performance compares favorably with the state-of-the-art developments and satisfies the 60 GHz high-data-rate communication application of the IEEE 802.15.3c standard.

7.1 Future Work

With the increased demand for higher data-rates for wireless LAN, and more complex modulation schemes, front-ends need to attain more linear performance and flat gain over the whole band. Using more advanced technologies, whose substrates have lower losses and transistor having higher f_t and f_{max}, can help to design circuits with relaxed current requirements and higher linearity.

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