# On the Perspectives of SiC MOSFETs in High-Frequency and High-Power Isolated DC/DC Converters 

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von der Fakultät IV - Elektrotechnik und Informatik der Technischen Universität Berlin zur Erlangung des akademischen Grades

Doktor der Ingenieurwissenschaften

- Dr.-Ing.
genehmigte Dissertation

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Tag der wissenschaftlichen Aussprache: 27. August 2018

## Acknowledgements

I would like to express my greatest gratitude to my advisor Prof. Dr. Ing. Sibylle Dieckerhoff for her support and encouragement over the course of my graduate study and research at the Technical University of Berlin. Her knowledge, vision and creative thinking have been a source of inspiration. I appreciate here understanding the most of the difficult times through my studying. I would like to thank all my colleagues at TU Berlin for the pleasant atmosphere and for their kindness.

I would like to thank my committee members; Prof. Dr.-Ing. Uwe Schäfer and Prof. Dr.-Ing. Regine Mallwitz for their reviews and useful feedback.

In addition, I would also like to acknowledge the "Erasmus Mundus Action-2 Avempace I" and Tafila Technical University who gave me the chance to complete my Ph.D. degree.

My parents, any language is too pale and weak to describe my love for you. When I hear their voice this gives me the power to continue. All I can do is to make you feel proud of me. I have done it this time and $I$ will do it in the future.

Finally, but also most importantly, my deepest gratitude and love belong to my dearest wife Alaa and my two lovely children Mohammad and Al-Rayyan, Looking into their faces enough to forget all the difficult times.

Abdullah
Berlin, June 2018


#### Abstract

Increasing demand for efficiency and power density pushes Si-based devices to some of their inherent material limits, including those related to temperature operation, switching frequency, and blocking voltage. Recently, SiC-based power devices are promising candidates for high-power and high-frequency switching applications. Today, SiC MOSFETs are commercially available from several manufacturers. Although technology affiliated with SiC MOSFETs is improving rapidly, many challenges remain, and some of them are investigated in this work. The research work in this dissertation is divided into the three following parts.

Firstly, the static and switching characteristics of the state-of-the-art 1.2 kV planar and double-trench SiC MOSFETs from two different manufacturers are evaluated. The effects of different biasing voltages, DC link voltages, and temperatures are analysed. The characterisation results show that the devices exhibit superior switching performances under different operating conditions. Moreover, several aspects of using the SiC MOSFET's body diode in a DC/DC converter are investigated, comparing the body-diodes of planar and double-trench devices. Reverse recovery is evaluated in switching tests considering the case temperature, switching rate, forward current, and applied voltage. Based on the measurement results, the junction temperature is estimated to guarantee safe operation. A simple electro-thermal model is proposed in order to estimate the maximum allowed switching frequency based on the thermal design of the SiC devices. Using these results, hard- and soft-switching converters are designed, and devices are characterised as being in continuous operation at a very high switching frequency of 1 MHz . Thereafter, the SiC MOSFETs are operated in a continuous mode in a $10 \mathrm{~kW} / 100-250 \mathrm{kHz}$ buck converter, comparing synchronous rectification, the use of the body diode, and the use of an external Schottky diode. Further, the parallel operation of the planar devices is considered. Thus, the paralleling of SiC MOSFETs is investigated before comparing the devices in continuous converter operation. In this regard, the impact of the most common mismatch parameters on the static and dynamic current sharing of the transistors is evaluated, showing that paralleling of


SiC MOSFETs is feasible.
Subsequently, an analytical model of SiC MOSFETs for switching loss optimisation is proposed. The analytical model exhibits relatively close agreement with measurement results under different test conditions. The proposed model tracks the oscillation effectively during both turn-on and -off transitions. This has been achieved by considering the influence of the most crucial parasitic elements in both power and gate loops.

In the second part, a comprehensive short-circuit ruggedness evaluation focusing on different failure modes of the planar and double-trench SiC devices is presented. The effects of different biasing voltages, DC link voltages, and gate resistances are evaluated. Additionally, the temperature-dependence of the short-circuit capability is evaluated, and the associated failure modes are analysed. Subsequently, the design and test of two different methods for overcurrent protection are proposed. The desaturation technique is applied to the SiC MOSFETs and compared to a second method that depends on the stray inductance of the devices.

Finally, the benefits of using SiC devices in continuous high-frequency, high-power DC/DC converters is experimentally evaluated. In this regard, a design optimisation of a high-frequency transformer is introduced, and the impact of different core materials, conductor designs, and winding arrangements are evaluated. A ZVZCS Phase-Shift Full-Bridge unidirectional DC/DC converter is proposed, using only the parasitic leakage inductance of the transformer. Experimental results for a $10 \mathrm{~kW},(100-250) \mathrm{kHz}$ prototype indicate an efficiency of up to $98.1 \%$ for the whole converter. Furthermore, an optimised control method is proposed to minimise the circulation current in the isolated bidirectional dual active bridge DC/DC converter, based on a modified dual-phase-shift control method. This control method is also experimentally compared with traditional single-phase shift control, yielding a significant improvement in efficiency. The experimental results confirm the theoretical analysis and show that the proposed control can enhance the overall converter efficiency and expand the ZVZCS range.

## Zusammenfassung

Die steigende Nachfrage nach Effizienz und Leistungsdichte bringt Si-basierte Leistungsbauteile an einige inhärente Materialgrenzen, die unter anderem mit der Temperaturbelastung, der Schaltfrequenz und der Blockierspannung in Zusammenhang stehen. In jüngster Zeit sind SiC-basierte Leistungsbauelemente vielversprechende Kandidaten für Hochleistungs- und Hochfrequenzanwendungen. Aktuell sind SiC-MOSFETs von mehreren Herstellern im Handel erhältlich. Obwohl sich die Technologie der SiC-MOSFETs rasch verbessert, werden viele Herausforderungen bestehen bleiben. Einige dieser Herausforderungen werden in dieser Arbeit untersucht. Die Untersuchungen in dieser Dissertation gliedern sich in die drei folgenden Teile:

Im ersten Teil erfolgt, die statische und die transiente Charakterisierung der aktuellen $1,2 \mathrm{kV}$ Planarund Doubletrench SiC-MOSFETs verschiedener Hersteller. Die Auswirkungen unterschiedlicher Gatespannungen, Zwischenkreisspannungen und Temperaturen werden analysiert. Die Ergebnisse der Charakterisierung zeigen, dass die Bauteile überlegene Schaltleistungen unter verschiedenen Betriebsbedingungen aufweisen. Darüber hinaus wird der Einsatz der internen SiC-Bodydioden in einem DC/DC-Wandler untersucht, wobei die Unterschiede zwischen Planar- und DoppeltrenchBauteilen aufgezeigt werden. Das Reverse-Recovery-Verhalten wird unter Berücksichtigung der Gehäusetemperatur, der Schaltgeschwindigkeit, des Durchlassstroms und der angelegten Spannung bewertet.

Anhand der Messergebnisse wird die Sperrschichttemperatur geschätzt, damit ein sicherer Betrieb gewährleistet ist. Ein einfaches elektrothermisches Modell wird vorgestellt, um die maximal zulässige Schaltfrequenz auf der Grundlage des thermischen Designs der SiC-Bauteile abzuschätzen. Anhand dieser Ergebnisse werden hart- und weichschaltende Umrichter konzipiert und die Bauteile werden im Dauerbetrieb mit einer sehr hohen Schaltfrequenz von 1 MHz untersucht. Danach werden die SiC-MOSFETs im Dauerbetrieb in einem 10 kW / 100-250 kHz-Tiefsetzsteller betrieben. Dabei wird die Synchrongleichrichtung, die Verwendung der internen Diode und die Verwendung einer externen Schottky-Diode verglichen. Außerdem wird die Parallelisierung von SiC-MOSFETs untersucht, bevor
die Parallelschaltung der verschiedenen Bauelemente ebenso im kontinuierlichen Konverterbetrieb verglichen wird. Es wird der Einfluss der häufigsten Parametervariationen auf die statische und dynamische Stromaufteilung der Transistoren analysiert, was zeigt, dass eine Parallelisierung von SiC-MOSFETs möglich ist.

Anschließend wird ein analytisches Modell der SiC-MOSFETs zur Schaltverlustoptimierung vorgeschlagen. Das analytische Modell zeigt eine relativ enge Übereinstimmung mit den Messergebnissen unter verschiedenen Testbedingungen. Das vorgeschlagene Modell bildet die Schwingungen sowohl beim Ein- als auch beim Ausschalten effektiv nach. Dies wurde durch die Berücksichtigung der wichtigsten parasitären Elemente in Strom- und Gatekreisen erreicht.

Im zweiten Teil wird eine umfassende Bewertung der Kurzschlussfestigkeit mit Fokus auf verschiedene Ausfallmodi der planaren und double-trench SiC-Bauelemente vorgestellt. Die Auswirkungen unterschiedlicher Gatespannungen, Zwischenkreisspannungen und Gate-Widerstände werden ausgewertet. Zusätzlich wird die temperaturabhängige Kurzschlussfähigkeit ausgewertet und die zugehörigen Fehlerfälle werden analysiert. Anschließend wird die Auslegung und Prüfung von zwei verschiedenen Verfahren zum Überstromschutz evaluiert. Die „Desaturation"-Technik wird auf SiC-MOSFETs angewendet und mit einer zweiten Methode verglichen, welche die parasitäre Induktivität der Bauelemente nutzt.

Schließlich wird der Nutzen des Einsatzes von SiC-Bauteilen in kontinuierlichen Hochfrequenz-Hochleistungs-DC/DC-Wandlern experimentell untersucht. In diesem Zusammenhang wird eine Designoptimierung eines Hochfrequenztransformators vorgestellt und der Einfluss verschiedener Kernmaterialien, Leiterausführungen und Wicklungsanordnungen wird bewertet. Es wird ein unidirektionaler ZVZCS Vollbrücken-DC/DC-Wandler vorgestellt, der nur die parasitäre Streuinduktivität des Transformators verwendet. Experimentelle Ergebnisse für einen 10 kW , (100-250) kHz Prototyp zeigen einen Wirkungsgrad von bis zu $98,1 \%$ für den gesamten Umrichter. Abschließend wird ein optimiertes Regelverfahren verwendet, welches auf einem modifizierten Dual-Phase-Shift-Regelverfahren basiert, um den Kreisstrom im isolierten bidirektionalen Dual-Aktiv-Brücken-DC/DC-Wandler zu minimieren. Diese Regelmethode wird experimentell mit der herkömmlichen Single-Phase-ShiftRegelung verglichen. Hierbei zeigt sich eine deutliche Effizienzsteigerung durch die neue Regelmethode. Die experimentellen Ergebnisse bestätigen die theoretische Analyse und zeigen, dass die vorgeschlagene Regelung den Gesamtwirkungsgrad des Umrichters erhöhen und den ZVZCS-Bereich erweitern kann.

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## Nomenclature

## Roman Symbols

| $B_{o p t}$ | Optimal Flux Density |
| :---: | :---: |
| $C_{i s s}$ | MOSFET Input Parasitic Capacitance, $C_{i s s}=C_{g s}+C_{g d}$ |
| $C_{L}$ | Load Inductor Parasitic Capacitance |
| $C_{\text {ossFW }}$ | Output Parasitic Capacitance of the Freewheeling Diode |
| $C_{\text {oss }}$ | MOSFET Output Parasitic Capacitance, $C_{o s s}=C_{d s}+C_{g d}$ |
| $C_{r s s}$ | Reverse Transfer Capacitance, $C_{r s s}=C_{g d}$ |
| $C_{\text {tot }}$ | Parallel Combination of $\mathrm{C}_{\text {ossFW }}$ and $\mathrm{C}_{L}$ |
| $D_{1}$ | Phase-Shift Ratio in the Primary Side |
| $D_{2}$ | Phase-Shift Ratio in the Secondary Side |
| $D_{\text {cycle }}$ | Duty Cycle |
| $d_{e f f}$ | Effective Duty Cycle |
| $D_{F F}$ | Feed-Forward Phase-Shift Compensation |
| $D_{\text {min }}$ | Minimum Phase-Shift Ratio |
| $D_{P I}$ | Output of PI Controller |
| $\Delta B$ | Peak AC Flux Density |


| $\Delta d_{1}$ | The Time where the Primary Current Change from the Maximum (in Positive Direction) to Zero |
| :---: | :---: |
| $\Delta d_{2}$ | The Time where the Primary Current Change from the Zero to Maximum (in Negative Direction) |
| $\Delta D$ | Duty Cycle Loss |
| D | Phase-Shift Ratio |
| $E_{o f f}$ | Turn-off Energy Loss |
| $E_{\text {on }}$ | Turn-on Energy Loss |
| $E_{S C}$ | Short Circuit Critical Energy |
| $E_{s w}$ | Switching Energy Loss |
| $E_{t o t}$ | Total Energy Loss |
| $f_{s w}$ | Switching Frequency |
| $g_{f s}$ | SiC MOSFET Transconductance |
| $i_{\text {ch }}$ | Channel Current |
| $I_{C L}$ | Charging/Discharging Current of the Load Inductor Capacitance |
| $I_{\text {CossFW }}$ | Charging/Discharging Current of the Output Capacitance of the Freewheeling Diode |
| $I_{\text {Coss }}$ | Output Capacitance Charging Current |
| $I_{\text {Diode-Avg }}$ | Diode Average Current |
| $I_{\text {Diode-rms }}$ | Diode RMS Current |
| $I_{d s-r m s}$ | Drain-Source RMS Current |
| $i_{d s 7}$ | Drain-source Current at $t_{7}$ |
| $I_{F}$ | Forward Current |


| $i_{L r}$ | High Frequency Inductor Current |
| :---: | :---: |
| $I_{r r}$ | Reverse Recovery Current |
| $I_{\text {SCMAX }}$ | Maximum Short Circuit Current |
| $I_{S C}$ | Short Circuit Current |
| $L_{D}$ | Internal and External Inductances of the Drain Terminal |
| $L_{G S}$ | Common Source Inductance |
| $L_{G}$ | Internal and External Inductances of the Gate Terminal |
| $L_{L K}$ | Transformer Leakage Inductance |
| $L_{\text {loop }}$ | Power Loop Parasitic Inductance |
| $L_{o}$ | Output Filter Inductor |
| $L_{r-\max }$ | Maximum Series Primary Inductor |
| $L_{\text {Rect }}$ | Inductance of the Rectangular Conductor |
| $L_{r}$ | Total Series Primary Inductor |
| $L_{\text {stray }}$ | Stray Inductance |
| $L_{S}$ | Internal and External Inductances of the Source Terminal |
| $m$ | Conversion Ratio |
| $n_{\text {opt }}$ | Optimal Number of Turns |
| $P_{\text {calorimetric }}$ | Power Loss Measured by Calorimetric Method |
| $P_{\text {Cond }}$ | Conduction Loss |
| $P_{c}$ | Core Loss |
| $P_{\text {DMAX }}$ | Maximum Power Dissipated |
| $Q_{r r}$ | Reverse Recovery Charge |


| $R_{B D}$ | Body-Diode Forward Resistance |
| :---: | :---: |
| $R_{\text {ch }}$ | Channel Resistance |
| $R_{D C}$ | DC Resistance |
| $R_{\text {DSon } 0}$ | On-State Resistance at Room Temperature |
| $R_{\text {DSon }}$ | Static On-State Resistance |
| $R_{\text {gext }}$ | External Gate Resistance |
| $R_{\text {gint }}$ | Internal Gate Resistance |
| $R_{\text {gext-opt }}$ | Optimal External Gate Resistance |
| $R_{G}$ | Gate Resistance (Internal and External Gate Resistances) |
| $R_{L, A C}$ | AC Resistance of the Inductor |
| $R_{\text {loop }}$ | Total Loop Resistance |
| $R_{\text {soft }}$ | Soft Turn-off Resistance |
| $R_{t h, C A}$ | Thermal Resistance of the Dielectric Material |
| $R_{t h-c a}$ | Thermal Resistance from Case to Ambient |
| $R_{\text {th-jc }}$ | Thermal Resistance from Junction to Case |
| $R_{\text {th }}$ | Total Thermal Resistance |
| $R_{T}$ | Diode on-State Resistance |
| $T_{c}$ | Case Temperature |
| $t_{d 1}$ | Time Difference between the Point at which the SC Current Starts to Fall and the Point where the Comparator is Triggered |
| $t_{d 2}$ | The Time required to Turn-off the device Including the SC Current Falling |
|  | Time |
| $T_{D}$ | Dead-Time |


| $T_{h s}$ | Half-Switching Period |
| :---: | :---: |
| $t_{i f}$ | Current Falling-Time |
| $T_{\text {in }}$ | Inlet Liquid Temperature |
| $t_{i r}$ | Current Rising-Time |
| $T_{j}$ | Junction Temperature |
| $T_{\text {out }}$ | Outlet Liquid Temperature |
| $T_{o}$ | Room Temperature ( $25{ }^{\circ} \mathrm{C}$ ) |
| $t_{r r}$ | Reverse Recovery Time |
| $T_{S C-c r t}$ | Critical Short Circuit Time |
| $T_{S C}$ | Short Circuit Time |
| $T_{\text {surface }}$ | Transformer Surface Temperature |
| $t_{v f}$ | Voltage Falling-Time |
| $t_{v r}$ | Voltage Rising-Time |
| $V_{B D F W}$ | Body-Diode Built-in Voltage |
| $V_{\text {drive-off }}$ | Turn-off Gate-Source Voltage |
| $V_{\text {drive-on }}$ | Turn-on Gate-Source Voltage |
| $V_{\text {drive }}$ | Drive Gate-Source Voltage |
| $v_{\text {DSon }}$ | On-State Voltage |
| $v_{f}$ | Diode Forward Voltage |
| $V_{g s-m i n}$ | Minimum Gate-Source Voltage |
| $V_{G S m a x}$ | Gate-Source Voltage Upper Limit |
| $V_{m-o n}$ | Miller Voltage Level during Turn-on |


| $V_{m 1}$ | Miller Voltage Level at $I_{o}$ |
| :--- | :--- |
| $V_{m 2}$ | Miller Voltage Level at $\mathrm{I}_{d s 7}$ |
| $V_{m}$ | Miller Voltage Level |
| $V_{p r e-1}$ | First Pre-charging Reference Voltage |
| $V_{p r e-2}$ | Second Pre-charging Reference Voltage |
| $V_{s d-c h}$ | MOSFET Channel Voltage Drop |
| $V_{t h 1}$ | Threshold Voltage Temperature Coefficient |
| $V_{t h o}$ | Threshold Voltage at Room Temperature |
| $V_{T}$ | Diode on-State Voltage |

## Greek Symbols

$\alpha$,
$\alpha_{r}$
$\eta_{M D P S-M A X}$
$\lambda_{1}$
$\lambda$
$\mu_{0}$
$\omega_{n}$
$\rho$
$\tau_{1}$
$\tau_{2}$
$\varphi$
$\eta_{S P S-M A X} \quad$ Maximum Efficiency Achieved by Single Phase-Shift
Core Loss Coefficient

On-State Resistant Coefficient

Maximum Efficiency Achieved by Modified Dual Phase-Shift

Applied Primary Voltage

Safe Margin for Thermal Limit Calculation

Permeability of the Air

Resonant Frequency

Resistivity of the Copper

Charging Time Constant of the Input Capacitance during Turn-on

Discharging Time Constant of the Input Capacitance during Turn-off

Phase-Shift Angle in Degree

| $\zeta$ | Damping Ratio |
| :---: | :---: |
| Acronyms / Abbreviations |  |
| $B A B-I B$ | Dual Active Bridge Isolated Bidirectional |
| $B D$ | Body Diode |
| C2M | SiC MOSFET C2M0080120D |
| CLC | Closed-Loop Control |
| $D A B$ | Dual Active Bridge |
| DMOSFET | Double-implanted MOSFET |
| DPS | Dual Phase-Shift |
| DPT | Double Pulse Test |
| DUT | Device Under Test |
| EMI | Electromagnetic Interference |
| EPS | Extended Phase-shift |
| ESR | Equivalent Series Resistance |
| $F W D$ | Freewheeling Diode |
| FWL | Freewheeling Loop |
| HF | High Frequency |
| HFI | High Frequency Inductor |
| HFT | High Frequency Transformer |
| HS | Hard Switching |
| MDPS | Modified Dual Phase-Shift |
| NTC | Negative Temperature Coefficient |


| OCP | Overcurrent Protection |
| :---: | :---: |
| $O L-A S$ | Open Loop with Active Secondary Side |
| $O L-P S C$ | Open-Loop Phase-Shift Control |
| OS | Overshoot |
| $P S-F B$ | Phase-Shift Full-Bridge |
| PTC | Positive Temperature Coefficient |
| SBD | Schottky Barrier Diode |
| SC | Short Circuit |
| SCH | SiC MOSFET SCH2080KE |
| $S C T$ | SiC MOSFET SCT3040KL |
| SiC | Silicon Carbide |
| $S O A$ | Safe Operation Area |
| SPS | Single Phase-Shift |
| SR | Synchronous Rectification |
| TPS | Triple Phase-Shift |
| UMOSFET | Double-Trench MOSFET |
| ZCS | Zero-Current Switching |
| ZTP | Zero Temperature Point |
| ZVS | Zero-Voltage Switching |
| ZVZCS | Zero-Voltage Zero-Current Switching |

## Chapter 1

## Introduction

RECENTLY, wide bandgap (WBG) semiconductors such as silicon carbide ( SiC ) and gallium nitride $(\mathrm{GaN})$ have attracted the focus of a great deal of research and development. SiC devices have approximately three times as large a bandgap (3.26 eV) as silicon-based (Si) devices $(1.12 \mathrm{eV})$. Large bandgaps result in much lower leakage currents and higher operating temperatures. Furthermore, the higher breakdown field of the WBG semiconductors allows for a higher doping concentration with thinner blocking layers than those achievable with Si devices. As a consequence, the drift region may be designed to be much thinner, allowing a lower on-state resistance for a given breakdown voltage. Additionally, SiC devices are superior in terms of thermal conductivity, which in turn improves the size of the cooling system [1, 2]. All of these features make SiC-based devices attractive for use in a high-frequency and high-power application.

Nowadays, SiC devices are commercially available from several manufacturers in different packages. Most of the commercial SiC devices are the SiC Schottky diode and SiC MOSFET at rated voltages from 400 V to 1.7 kV . Studies of SiC MOSFETs ranging $2.2 \mathrm{kV}, 3 \mathrm{kV}$ and 3.3 kV can be found in [3-7]. Due to the higher electric field strength, SiC MOSFETs have the ability to increase the blocking voltage. SiC MOSFETs with 10 kV blocking voltage have been developed, and their static and switching performance have been examined in [8-11]. Recent studies have analysed and demonstrated a hybrid DC/DC converter for a medium voltage (MV) application using 15 kV SiC modules [12].

### 1.1 SiC MOSFETs

A significant effort has been devoted to the development of SiC MOSFETs. The common physical structure of SiC MOSFETs is the planar double-implanted MOSFET in 4H-SiC (SiC-DMOSFET). In 2011, Cree Inc. (now Wolfspeed) has released the first commercial SiC planar MOSFET rated 1.2 kV with $80 \mathrm{~m} \Omega$ on-state resistance. Recently, Wolfspeed announced the availability of the third generation, with low-inductance discrete packaging (i.e. TO-247-4 and TO-263-7). Moreover, Rohm Inc. is currently commercialising the third generation of SiC MOSFET with double trench structure (SiC UMOSFET) to improve some issues related to gate oxide robustness and channel mobility. The latest generations of planar and trench devices have exhibited significant improvements in different issues, such as switching speed and reliability. Furthermore, Infineon announced the new 1.2 kV CoolSiC MOSFETs, which have been optimised to combine high reliability with high switching performance [13-15]. Other manufacturers, including General Electric (GE), Mitsubishi and STMicroelectronics (ST), are also developing SiC MOSFETs. With low on-state resistance, low switching loss, and high-temperature capability, SiC MOSFETs allow for a more efficient power conversion.

The fast switching of SiC MOSFETs enables a high-power density converter design with minimal size and cost compared to that achieved by Si-based converters. The fast switching, though, is associated with oscillation phenomena that occur during the dynamic switching process. The switching is more sensitive to the circuit parasitic elements, such as inductance and capacitance in gate and power loops. Therefore, an optimised gate and power loop layout is required to fully utilise the potential of the SiC devices. However, reliability issues associated with SiC MOSFETs is another important topic that must be considered for the application. The main failure mechanisms occurring during short circuit conditions are gate oxide degradation and thermal-runaway.

### 1.2 Research Motivation

The significant improvements in the switching performance of current SiC MOSFETs make them more reliable and superior alternative devices for use in high efficiency and high-power density converters. In spite of the fact that the SiC MOSFETs have many advantages compared to Si-devices, some technological challenges associated with them still require further research:

- Packaging: The device packaging needs to be designed and optimised for high-temperature applications, which still have not yet been developed. In addition, low inductive packaging
is needed to take full advantage of the SiC MOSFETs switching capability and thus further improve their efficiency and reliability [16-18].
- Reliability and robustness: Even in the latest generation of SiC MOSFETs, reliability issues are still encountered. The most critical challenges in this regard are threshold voltage stability [19, 20], gate oxide reliability [21-23], and body-diode degradation [24].
- Measurement technique: as measuring switching waveforms becomes more difficult with a higher switching frequency and a high-power density design, it becomes more difficult to accurately measure switching and conduction losses [25-27].
- Magnetic components: Increasing the switching frequency significantly reduces the physical size of the magnetic components. The magnetic component design for high-frequency applications faces many challenges, such as AC winding loss, the thermal resistance of the magnetic core, the availability of high permeability and low core loss at high temperatures, and the cooling system [28-30].
- Electromagnetic interference (EMI): Elevated levels of switching frequency introduce substantial EMI noise. Compared to Si-devices, the greater change of the rate of the drain-source voltage and current in SiC MOSFETs generates worse EMI and hence a worse switching performance, as well as instability problems [31-34].
- Cost: SiC MOSFETs have a higher price than Si-devices because of the limited availability of large wafers. Their prices are expected to be reduced in the near future as the new generation of these devices starts to be commercialised [18, 35].


### 1.3 Main Objectives and Contributions

The main objectives and contributions of the presented research work are as follows.

- The static and switching characteristics of the state-of-the-art 1.2 kV planar and double-trench SiC MOSFETs from two different manufacturers (CREE and ROHM) are evaluated. The effects of different biasing voltages, DC link voltages, and temperature operating points are analysed.
- The reverse recovery characteristics of the SiC MOSFET's body-diode are investigated and evaluated. Further, several aspects of using the SiC MOSFET's internal diode in a DC/DC
converter are investigated, comparing the body-diodes of planar and double-trench devices. According to the author's knowledge, the reverse recovery of the body-diodes in the trench SiC MOSFET has not yet been investigated in previously published research.
- An analytical model of the SiC MOSFET for switching loss optimisation is presented. The parasitic inductance is considered, as is the nonlinear behaviour of the junction parasitic capacitance and the transconductance. Further, the effect of the case temperature on switching behaviour is investigated. In addition, the diversion phenomenon that occurs because of the displacement current being generated by charging and discharging the parasitic capacitances is presented. The accuracy of the proposed model is validated by experimental results obtained under different operating conditions.
- In order to determine the safe operating area, a simple electro-thermal model is proposed; the maximum switching frequency is estimated according to the thermal limit of the device. Based on these results, hard- and soft-switching converters are designed. The devices are characterised in continuous operation at a very high switching frequency of 1 MHz . Thereafter, to verify the proposed electro-thermal model at a high power, the maximum achievable switching frequency of a 10 kW DC/DC converter is experimentally evaluated.
- The parallel operation of the planar MOSFETs is investigated. Therefore, the impact of parameter mismatch on the static and dynamic current sharing of the transistors is evaluated, showing that paralleling of SiC MOSFETs is feasible. The performance of the parallel connection is temperature dependent. To ensure a safe operation area, the junction temperature is estimated based on the measured and analytically calculated losses.
- An experimental study focusing on the failure modes, due to short circuiting, of planar and trench SiC devices is presented. To the best of the author's knowledge, this is the first study investigating and comparing different failure modes in the double-trench device to the planartechnology device. Additionally, the temperature-dependence of the short-circuit capability is evaluated, and the associated failure modes are presented. Based on these results, the design and test of two different methods for overcurrent protection are evaluated. The desaturation technique is applied to the SiC MOSFETs and compared to a second method that depends on the stray inductance of the devices.
- The benefits of using SiC devices in a high-frequency high-power DC/DC converter is experimentally evaluated. With the help of the small parasitic output capacitance of the SiC devices, a zero-voltage zero-current switching (ZVZCS) Phase-shift Full-Bridge topology is proposed using only the parasitic leakage inductance of the transformer. Experimental results for a 10 $\mathrm{kW},(100-250) \mathrm{kHz}$ prototype indicate an efficiency of up to $98.1 \%$ for the whole converter.
- Finally, an optimised control method (based on a modified dual-phase-shift control ) to minimise the circulation current in the Dual Active Bridge isolated bidirectional DC/DC converter is proposed and experimentally validated. Additionally, a 10 kW high-frequency transformer is optimised to minimise winding and core losses. Different prototypes have been designed, based on differences in core material, conductor type, and winding arrangement.


### 1.4 Dissertation Outline

This dissertation essentially consists of three main parts, as is illustrated in Figure 1.1. The first of these comprises Chapters two to five and is generally focused on investigating and characterising the SiC MOSFETs at different operating conditions in the first and third quadrants. Based on the characterisation results, an analytical switching model is derived to predict both switching performance and switching losses.

The second part focuses on the ruggedness evaluation of the SiC MOSFETs, providing a comparison between the planar and double-trench devices. The analysis of different failure modes is evaluated for both technologies. Afterwards, a design for tow different overcurrent protection are presented. In the last part, which comprises Chapters seven and eight, the high-frequency-link power conversion system with high efficiency is presented. The unidirectional and bidirectional isolated DC/DC converters are selected as application examples to demonstrate the maximum achievable conversion efficiency. The converter design, high-frequency magnetic design, and detailed loss analysis, as well as the experimental verification, are presented for the high-power and high-frequency converters. Finally, Chapter nine concludes by summarising the major contributions of the dissertation and proposing future research.


Figure 1.1: Dissertation Structure.

## Chapter 2

## Static Characteristics

### 2.1 Introduction

FOR the last few decades, Si -based power switches were considered to be the primary solution for power electronics applications. However, Si-based devices are approaching some of their inherent material limits, including those related to operation temperature, switching frequency, and blocking voltage. Recently, SiC-based power devices are considered as candidates for high-power and high-frequency switching applications, and SiC MOSFETs are commercially available from several manufacturers. To fully utilise the potential of these devices, it is necessary to understand their static and dynamic behaviour. Similarly, to ensure their reliability and safe operation, the limiting operating factors of SiC devices should be specified.

In this chapter, the static characteristics of the latest-generation 1.2 kV SiC MOSFETs from wellknown SiC manufacturers (CREE and ROHM) are presented. The static performance in the first and third quadrants are experimentally evaluated. In addition, to utilise their internal diodes as a freewheeling diode, the static characteristics of the SiC MOSFET's internal diode are investigated and discussed.

### 2.2 Devices Under Test

In this work, three different $1.2 \mathrm{kV} \mathrm{SiC} \mathrm{MOSFETs}, \mathrm{TO247} \mathrm{package} ,\mathrm{are} \mathrm{under} \mathrm{test}$.Table 2.1 lists the devices under test (DUTs) and some of their main parameters, extracted from the datasheets. Both C2M and SCH devices are planar double-implanted MOSFETs (DMOSFETs), while the SCT

Table 2.1: Devices Under Test.

| Device / Manufacturer | Marked as | Technology | Die Size $\left[\mathrm{cm}^{2}\right]$ | Continuous Rated Current $25^{\circ} \mathrm{C} / 100^{\circ} \mathrm{C}$ [A] | On-State Resistance [ $\mathrm{m} \Omega$ ] | $\begin{gathered} \mathrm{C}_{i s s} / \mathrm{C}_{\text {oss }} / \mathrm{C}_{r s s} \\ {[\mathrm{pF}]} \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| C2M0080120D / Wolfspeed | C2M | Planar | 0.104 | $36 / 24$ | 80 | 950 / 80 / 7.6 |
| SCH2080KE / ROHM | SCH | Planar with SBD | 0.132 | 40 / 28 | 80 | 1850 / 175 / 20 |
| SCT3040KL / ROHM | SCT | Double Trench | 0.132 | $55 / 39$ | 40 | 1337 / 76 / 27 |

device is a double-trench MOSFET (SiC-UMOSFET) structure. The basic physical structure of the planar and double-trench SiC MOSFETs is shown in Figure 2.1. The on-resistance of the DMOSFET is mainly determined by the sum of the channel and the drift region resistances. The total on-state resistance has an additional component resulting from the JFET region between the implanted P-wells. Furthermore, the on-state resistance includes other resistive components, as illustrated in Figure 2.1, further details can be found in [1,2].

On the other hand, the double-trench technology enables a higher channel density and effectively eliminates the JFET resistance present in the DMOSFET structure. Compared to the planar technology, the cell pitch can be made much smaller in the double-trench structure and hence increases the channel density which reduces its contribution to the on-state resistance. Due to the absence of the JFET resistance and the reduction of the channel resistance, the total on-state resistance is significantly reduced in this technology, e.g., with the same chip area, the on-state resistance of the SCT devices is reduced up to $50 \%(40 \mathrm{~m} \Omega)$ in contrast to the second planar generation $(80 \mathrm{~m} \Omega)[1,2,36,37]$. It should be noted that the SCH2080KE package includes an external anti-parallel SiC Schottky barrier diode (SBD), which dominates the diode's switching behaviour.


Figure 2.1: Basic structure of SiC MOSFET (a) planar [1, 2, 36] and (b) double-trench [37].

### 2.3 First Quadrant Static Characteristics

The output characteristics of the DUTs are measured with different gate-source voltages $\left(V_{g s}\right)$ of up to 22 V and over wide operating case temperatures $\left(T_{c}\right)$ of up to $150^{\circ} \mathrm{C}$. The measured I-V characteristics are depicted in Figure 2.2.


Figure 2.2: Temperature-dependent output characteristics of DUTs: (a) C2M, (b) SCH and (c) SCT.

At low biasing voltage (e.g. $V_{g s}=12 \mathrm{~V}$ ), the slope of the I-V curves increases with temperature, indicating a decrease in on-state resistance. In contrast, in the context of high biasing (e.g. $V_{g s}>16$ V), the slope decreases with increasing temperature, indicating decreasing channel conductivity. This feature is potentially beneficial to the short circuit ruggedness in its limiting of the saturation current and improvement of the device paralleling behaviour. The temperature behaviour of SiC MOSFETs can be explained by the competing properties of the channel resistance ( $R_{c h}$ ), drift-layer resistance ( $R_{d r i f t}$ ) and JFET-region resistance $\left(R_{J F E T}\right)$ [1, 2].

The $R_{D S o n}$ is highly dependent on the biasing voltage, as depicted in Figure 2.3. At low biasing
voltage ( $V_{g s}=14 \mathrm{~V}$ ), the $R_{D S o n}$ of the planar devices, C 2 M and SCH , first shows a reduction and then an increase with temperature. This can be explained by the fact that the overall $R_{D S o n}$ is mainly determined by the contribution of $R_{c h}, R_{J F E T}$, and $R_{d r i f t}$. With low temperature, $R_{c h}$, which has a negative temperature coefficient (NTC), dominates the overall $R_{D S o n}$. The other components ( $R_{J F E T}$ and $R_{\text {drift }}$ ) with positive temperature coefficient (PTC) become more effective at a higher temperature, so that the overall $R_{D S o n}$ increases with temperature. Compared to the planar technology, the doubletrench SiC MOSFET shows a wider PTC, where an increasing in the $R_{D S o n}$ is observed even at low $V_{g s}\left(V_{g s}>12 \mathrm{~V}\right)$, which helps to prevent thermal runaway. This is mainly due to the fact that the $R_{c h}$ in the trench structure is much smaller than the channel contribution within the planar technology [1, 2, 38].


Figure 2.3: Temperature-dependent on-state resistance at $I_{d s}=20 \mathrm{~A}$ : (a) C2M, (b) SCH and (c) SCT.

As shown in Table 2.1, both Rohm devices have the same die size different from the Wolfspeed device. Therefore, since the direct comparison of the $R_{D S o n}$ is difficult, the normalised $R_{D S o n}$ with respect to the die size is evaluated (see Figure 2.4). With same die size, the specific $R_{D S o n}$ of the trench device


Figure 2.4: Specific on-state resistance with different temperatures.
(SCT) (e.g. $5.71 \mathrm{~m} \Omega-\mathrm{cm}^{2}$ at $20 \mathrm{~A} / 25^{\circ} \mathrm{C}$ ) shows a significant improvement compared to SCH (e.g. $10.43 \mathrm{~m} \Omega-\mathrm{cm}^{2}$ at $20 \mathrm{~A} / 25^{\circ} \mathrm{C}$ ). This results from the absence of the JFET-region resistance in this device generation [37]. In addition, due to high current density, the channel resistance $R_{c h}$ in the double-trench device is much smaller than in the planar DMOSFET [1, 2, 38].

At $150^{\circ} \mathrm{C}$, with respect to its room temperature resistance, the $R_{D S o n}$ of the C 2 M device increases by approximately $68 \%\left(+0.45 \mathrm{~m} \Omega /{ }^{\circ} \mathrm{C}\right.$ at $\left.V_{g s}=20 \mathrm{~V}\right)$ compared to $86 \%$ for $\mathrm{SCH}\left(+0.48 \mathrm{~m} \Omega /{ }^{\circ} \mathrm{C}\right.$ at $\left.V_{g s}=20 \mathrm{~V}\right)$ and $\mathrm{SCT}\left(+0.23 \mathrm{~m} \Omega /{ }^{\circ} \mathrm{C}\right.$ at $\left.V_{g s}=18 \mathrm{~V}\right)$. Compared to state-of-the-art high-voltage SiMOSFETs with similar current rating, SiC MOSFETs have a comparably low-temperature sensitivity of the $R_{D S o n}$. For example, at $150^{\circ} \mathrm{C}$, the $R_{D S o n}$ of the Si device IXFN32N120P is 2.5 times its room temperature resistance.

The transfer characteristic of the DUTs at $V_{d s}=10 \mathrm{~V}$ is illustrated in Figure 2.5. It indicates that the transconductance $\left(g_{f s}\right)$ increases with temperature at a fixed biasing voltage. According to [39, 40], this PTC behaviour arises from the increased MOS channel inversion electron density and mobility at high temperature. Therefore, the devices operate with possible thermal instability in the PTC area. In this context, the zero temperature crossing point (ZTP) represents the minimum biasing voltage which discriminates between the stable $\left(\mathrm{dI}_{d s} / \mathrm{dT}_{c}<0\right)$ and unstable $\left(\mathrm{dI}_{d s} / \mathrm{dT}_{c}>0\right)$ thermal areas. As depicted, the biasing voltage corresponding to the ZTPs occurs near 15.5 V for C 2 M and SCH devices and 16.5 V for SCT. In other words, to ensure that the devices operate in the thermally stable area, the minimum biasing gate-source voltage ( $V_{g s-m i n}$ ) should be larger than $\mathrm{V}(\mathrm{ZTP})$. Further, similar to Si-MOSFETs, a decreasing in the gate threshold voltage $\left(V_{t h}\right)$ is observed, see Figure 2.6. The trench device has the highest $V_{t h}$ compared to C 2 M and SCH devices. At $150^{\circ} \mathrm{C}$, the threshold voltage of C 2 M and SCH devices linearly reduces to $\sim 2 \mathrm{~V}$ at $150^{\circ} \mathrm{C}$, compared to $\sim 3.3 \mathrm{~V}$ for the SCT device. Therefore, to
prevent any false turn-on switching resulting from low $V_{t h}$, the SiC devices are recommended to be driven with a negative gate-source voltage.


Figure 2.5: Transfer characteristics for DUTs measured at different case temperatures.


Figure 2.6: Threshold voltage versus case temperature.

### 2.4 Static Internal-Diode Characteristics

The body-diode (BD) in SiC MOSFETs is a SiC PiN diode. Due to the wide band-gap, the intrinsic diode of SiC devices exhibits a higher voltage drop compared with Si-based MOSFETs [1]. Therefore, the conduction losses of the SiC internal-diode are much higher than those of a Si body-diode. The static characteristics of the DUT's body-diode are measured with different biasing voltages and case temperatures, as depicted in Figure 2.7. The body-diode voltage drop $\left(V_{s d}\right)$ is further extracted as a function of temperature and for different negative biasing with constant source-drain current $\left(I_{s d}\right)$ of 20 A , see Figure 2.8.


Figure 2.7: Static characteristics of SiC MOSFET BD with different $T_{c}$ and $V_{g s}$ : (a) C2M, (b) SCH and (c) SCT.


Figure 2.8: BD voltage-drop versus case temperature and different negative biasing voltage for $I_{s d}=$ 20 A.

Unlike SCH and SCT devices, C2M's body-diode voltage-drop shows a NCT, $-4.5 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ at 20A and $V_{g s}=-5 \mathrm{~V}$. According to $[1,2,41]$, this behaviour is due to an increase of the intrinsic carrier concentration at high temperature.

In contrast, due to the co-package with a discrete antiparallel SBD, the SCH device exhibits a PTC in wide current range, $+3.1 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ at 20 A and $V_{g s}=-5 \mathrm{~V}$. On the other hand, the trench device forward-voltage has a relatively small PTC,such as $+0.4 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ at 20 A and $V_{g s}=-2 \mathrm{~V}$.

This is due to the fact that the trench technology enables a significant increase in the channel current density, which results in a lower minority carrier lifetime compared to the planar technology [2]. This is a favourable feature when the parallel operation of SiC MOSFETs is needed. Through balancing the current sharing between the parallel BD, a thermal runaway for all parallel devices is avoided.

### 2.4.1 Static Third-Quadrant Characteristics

The high forward voltage of the internal diodes can be mitigated by operating MOSFETs in the third quadrant, similar to the forward conduction in the first quadrant. Figure 2.9 depicts the static characteristics of DUTs' applying positive biasing voltage.

In the third quadrant, the MOSFET channel is fully turned-on, at high biasing voltage (e.g. $V_{g s} \geq 18$ V). Accordingly, the voltage drop between source-drain terminals is significantly reduced compared with the case of using the body-diode. This effect is more pronounced in the C2M device: using positive biasing, $V_{g s}=20 \mathrm{~V}, V_{s d}$ is reduced by more than $66 \%$ compared with the case of using BD [Test conditions: $V_{g s}=-5 \mathrm{~V}$ and $T_{c}=25^{\circ} \mathrm{C}$ (See Figure 2.7)].

Therefore, it is desirable to reduce the reverse voltage drop, and hence the reverse conduction loss, by turning on the SiC device and operate in synchronous rectification (SR) mode.

The analysis of the third quadrant operation reveals the following two interesting observations.

- Operating in the $3^{\text {rd }}$ quadrant with $V_{g s}=0 \mathrm{~V}$ could lead to the MOSFET channel conducting during the freewheeling period. As shown in Figure 2.9, the channel starts conducting as $V_{d s}$ goes beyond a specific voltage level: $>-2 \mathrm{~V}$ and -1.5 V for C 2 M and SCT devices, respectively. Therefore, the devices are working with new reverse output characteristic, which is the parallel combination of the body-diode and the device channel characteristics. Compared to $V_{g s}=-5 \mathrm{~V}$, the MOSFET current is zero, and thus, the static characteristic depicted in Figure 2.7 shows the body-diode I-V reverse characteristic.

(a) C 2 M

(b) SCH

(c) SCT

Figure 2.9: Static characteristics of $\operatorname{SiC}$ MOSFET in $3^{\text {rd }}$ quadrant with different $T_{c}$ and positive $V_{g s}$ : (a) C2M, (b) SCH and (c) SCT.

- Conversely, when applying SR mode, $V_{g s}=20 \mathrm{~V}$, a current sharing between the MOSFET channel and the internal diode (body-diode or external SBD) is observed. At large load current, the relatively high forward voltage drop between the drain-source terminals forces the internal diode to conduct.

This behaviour is related more to the SCH device. When applying SR mode (see Figure 2.10), the MOSFET channel is conducting the whole current, and no current flows through the external SBD , until the crossing point $\mathrm{X}(0.92 \mathrm{~V}, 13 \mathrm{~A})$.

As the current increases to 13 A , both the SBD and MOSFET are conducting, which means that the voltage drop across the channel exceeds the forward drop voltage of the SBD. Consequently, a new equivalent on-state resistance is obtained, resulting from the parallel combination of


Figure 2.10: $3^{\text {rd }}$ quadrant current sharing between MOSFET channel and internal diode (SBD) of SCH device with $T_{c}=25^{\circ} \mathrm{C}$.
the SBD and MOSFET, which explains the different slopes in the I-V curves. Due to the new parallel combination, the conduction losses decrease compared to SR mode only.

## Chapter 3

## Dynamic Characterisation

### 3.1 Introduction

- IC devices exhibit fast switching, accompanied by undesirable current and voltage ringing during the turn-on and -off processes. Therefore, to achieve optimal utilisation of SiC MOSFETs, it is necessary to fully understand the switching behaviour and the dominating factors in both the turn-on and turn-off dynamic processes. Thus, an accurate model is needed to optimise and accurately predict the switching behaviour of these devices, thus defining their limitation factors, e.g. thermal and switching frequency limits, at different operating conditions.

In this chapter, first, the voltage and current measurement requirements are explained. Secondly, an optimisation procedure is derived for selecting the external gate resistance. Finally, using different freewheeling loop configurations is experimentally analysed, showing the advantages and disadvantages of using body diodes in both planar and trench devices.

### 3.2 Voltage and Current Measurement Requirement

SiC devices can turn-on and -off in a few nanoseconds. Therefore, a high bandwidth measurement equipment is required and should not introduce excessive parasitic elements into the power and driving circuits. For an accurate measurement, a bandwidth margin that is between 3 and 5 times higher than the calculated is typically required. For example, using (3.1), the turn-on rise current $\left(t_{i r}\right)$ with 10 ns requires at least 35 MHz of 3 dB measurement bandwidth [42]. Take a 5 times bandwidth margin, the
measurement technique should have at least 175 MHz bandwidth.
$f_{B W}=\frac{0.35}{t_{i r}}$

Currently, different methods are available to measure the switching current in power semiconductors. These include the Rogowski coil [43], Person current monitor [44], and coaxial current shunt [45]. The limitation of the Rogowski coil is the relatively low bandwidth of 30 MHz . On the other hand, it can measure several kA. Further, the galvanic isolation and the feasibility to place around the current path without affecting the switching behaviour are the main advantages of this method. The coaxial current shunt measures the current by monitoring the voltage drop across a resistor with a bandwidth of up to 2 GHz . Adding the coaxial shunt in power/gate loops leads to extra parasitic inductance that affects the switching behaviour. Additionally, the coaxial current shunt does not provide galvanic isolation, and due to the power dissipation limit, it cannot be used in continuous operation mode [45]. On the other hand, the Pearson current monitor has a galvanic isolation and high bandwidth of up to 200 MHz . To avoid the large physical size of this sensor, a two-stage current measurement method with Pearson 2877 is used, where a ferrite core transformer with 10 turns is used [46]. Table 3.1 summarises the properties of available commercialised current measurement methods.

Table 3.1: Comparison of the current measurements methods.

| Current Technique | Bandwidth | Galvanic Isolation | Ease of Integration | DC Capability | Affects the switching behaviour |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Rogowski Coil | Up to 30 MHz | Yes | Simple | No | No |
| Pearson Sensor | Up to 200 MHz | Yes | Fair | No | Slightly: Two Stage |
| Coaxial Shunt | Up to 2 GHz | No | Simple | Yes | Yes: Stage |

The bandwidth of a Rogowski coil is too low compared to the fast SiC MOSFET. The coaxial current shunt provides sufficient bandwidth, but does not provide galvanic isolation, therefore, attention should be paid to the grounding problem. The Pearson current monitor method is the most attractive option in characterising the SiC devices. Therefore, the two-stage current measurement method is used in this work.

Likewise, a high bandwidth voltage probe is required to measure the high dv/dt switching waveforms. For accurate measurement, the propagation delays in the voltage and current measurement transducers should be de-skewed to avoid any time misalignment and thus inaccuracies in the power loss calculation. Table 3.2 outlines the measurement equipment used in this work.

Table 3.2: Measurement equipment.

| Signal | Measurement Equipment |
| :--- | :--- |
| Drain Current | 200 MHz Pearson 2877 |
| Drain-Source Voltage - Differential | 400 MHz PMK PS-02, Differential Probe |
| Drain-Source Voltage - Ground <br> Gate-Source Voltage - Ground | 500 MHz LeCroy Probe PP007 |
| Oscilloscope | 500 MHz LeCroy High Definition Osci. 2.5 GS/s |

### 3.3 Driving Requirements of SiC Power MOSFETs

During the dynamic process, the fast switching of SiC MOSFETs generates undesirable voltage and current ringing, resulting in higher losses and substantial electromagnetic interference. An appropriate gate driver design is necessary to optimise and control the switching of the SiC devices. The design requirements of the gate-driver are affected by different parameters: gate voltage, gate resistance, and gate driver components. These are comprehensively explained in the following sections.

### 3.3.1 Gate-Source Voltage Level

Compared to Si MOSFETs, SiC devices have a relatively low transconductance. Accordingly, a high gate-source voltage is required to achieve the lowest on-state voltage at high load currents. As depicted in Figure 3.1, the optimal gate-source voltage level, which meets the minimum on-state resistance (minimum on-state voltage), is extracted from the output characteristics of the DUTs (see Section 2.3). Typically, the devices have a gate-source voltage upper limit ( $V_{G S m a x}$ ) (see Table 3.3). Exceeding these limits could damage the devices permanently.

Therefore, considering a $20 \%$ safety margin and accounting for the measured results shown in Figure $3.1,20 \mathrm{~V}$ is used as an optimal gate-source voltage for C 2 M and SCH devices, while 18 V is set for the SCT switch.

Furthermore, the reduction in gate biasing voltage leads to an increase in the $R_{D S o n}$ and reduces the switching speed. In addition, as explained in Section 2.3, the devices biasing with low voltage could lead to possible thermal instability. Thus, the minimum positive biasing voltage for continuous operation is selected to fulfil the condition $\mathrm{V}_{g s}>\mathrm{V}(\mathrm{ZTP})$.

It is recommended to use a negative gate bias voltage to reduce the switching turn-off time and to fully discharge the gate of SiC devices, hence avoiding unwanted turn-on. On the other hand, the negative


Figure 3.1: Variation of $\mathrm{R}_{D S o n}$ at different biasing voltages for different load current: (a) C 2 M , (b) SCH and (c) SCT.
biasing increases the reverse conduction loss through shifting the body-diode forward voltage, as explained in Section 2.4. According to [20, 46-49], due to the trapped holes effect, using continuous high negative biasing voltage for a long time leads to gate threshold instability, through shifting the threshold voltage in the negative direction. Therefore, an optimal negative biasing voltage should be specified. According to the manufacturers information, the maximum negative allowable voltage varies over a range of -10 V to -4 V . According to the measurements presented in Section 2.4 and considering the manufacturer recommendations, the minimum negative biasing voltage is set to -5 V for C2M and SCH devices and -2 V for the SCT device. Finally, the optimal positive and negative biasing voltage levels used in this work are summarised in Table 3.3.

Table 3.3: Optimal parameter selection for gate-driver design.

|  | $V_{G S m a x}$ <br> DUT <br> on $/$ off | $V_{\text {gs-opt }}$ <br> on $/$ off <br> $[\mathrm{V}$ | $R_{\text {gint }}$ <br> $[\Omega]$ | Optimal <br> calculated $R_{\text {gext }}$ <br> $[\Omega]$ | Optimal <br> selected $R_{\text {gext }}$ <br> $[\Omega]$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C2M | $25 /-10$ | $20 /-5$ | 4.7 | $>4.62$ | 5 |
| SCH | $26 /-10$ | $20 /-5$ | 6.3 | $>1.67$ | 2.5 |
| SCT | $22 /-4$ | $18 /-2$ | 7 | $>2.14$ | 2.5 |

### 3.3.2 di/dt and dv/dt Immunity

The dv/dt and di/dt are significantly higher for SiC MOSFETs than Si MOSFETs. The SiC devices are able to switch with a slew rate of up to 100 volts per nanosecond [46, 48]. This high slew rate presents new challenges for the gate driver design. To reduce noise and EMI issues between the input and output signals, a high common mode transient immunity CMTI for signal isolation is needed. In this work, a digital isolator, such as ISO7841, with very low parasitic capacitance ( $<2 \mathrm{pF}$ ) and high dv/dt immunity ( $>100 \mathrm{~V} / \mathrm{ns}$ ) is used. Further, the SiC MOSFET driver is built with the high-speed gate driver IC IXDN609. This driver provides 35 V swing, up to 9 A maximum output current and voltage rise/fall times less than 25 ns . Furthermore, an isolated power supply, providing positive and negative driving voltage, with $<5 \mathrm{pF}$ parasitic capacitance is used.

In addition to the aforementioned requirements, the PCB layout plays an important role in improving the dv/dt immunity. A good PCB layout reduces the parasitic elements, such as parasitic inductance and capacitance. Consequently, it improves the di/dt and dv/dt immunity. A Kelvin-source connection significantly reduces the common source inductance that is shared by power and gate loops, allowing the SiC MOSFET to switch with high di/dt.

### 3.3.3 Optimal External Gate Resistance Selection

The fast switching capability of SiC MOSFET often generates overshoot and switching oscillation, as well EMI emissions [50-53]. Using a large external gate resistance ( $R_{\text {gext }}$ ) leads to a reduction in the overshoot but increased switching losses. In this, the external gate resistance should be carefully selected to ensure that the gate pulse is sufficiently dampened. The optimal $R_{\text {gext }}$ is calculated based on the trade-off between the fast switching time and the gate-source overshoot voltage. The standard double-pulse tester (DPT) (see Figure 3.2-a), is used to derive the analytical expression of the optimal $R_{\text {gext }}$. The optimal $R_{\text {gext }}$ is derived considering the turn-on process.


Figure 3.2: a) DPT circuit and b) Simplified turn-on/charging input capacitance.

For simplicity, the effect of the load current on the gate loop through the common source inductance ( $\mathrm{L}_{S} \mathrm{di}_{d s} / \mathrm{dt}$ ) is neglected and later considered in a safety margin. Figure 3.2-b depicts the equivalent circuit of the charging input capacitance ( $C_{i s s}$ ) sub-interval during a turn-on transition. When the gate voltage $\left(V_{G G}\right)$ is applied, the gate current $\left(I_{g}\right)$ charges the gate-source equivalent input capacitance $\left(C_{i s s}\right.$ $=C_{g s}+C_{g d}$ ). During this period, the power loop does not change, and the load current keeps flowing through the upper freewheeling diode (FWD). Therefore, the circuit equations can be expressed as follows:

$$
\begin{align*}
V_{G G} & =\left(L_{G}+L_{S}\right) \frac{d i_{g}}{d t}+R_{G} i_{g}(t)+v_{g s}(t)  \tag{3.2}\\
i_{g} & =C_{i s s} \frac{d v_{g s}}{d t} \quad\left(C_{i s s} \approx C_{g s}\right) \tag{3.3}
\end{align*}
$$

where $R_{G}$ includes the internal $\left(R_{\text {gint }}\right)$ and external ( $\left.R_{\text {gext }}\right)$ gate resistances, $\left(R_{G}=R_{\text {gint }}+R_{\text {gext }}\right)$. To solve these differential equations, the Laplace transformation is applied:

$$
\begin{equation*}
v_{g s}(s)=\frac{1}{s} \cdot \frac{V_{G G}}{L_{e q} C_{i s s} s^{2}+R_{G} C_{i s s} s+1} \tag{3.4}
\end{equation*}
$$

where
$L_{e q}=\frac{L_{S} L_{D}}{L_{S}+L_{D}}+L_{G}$

Practically, the gate-source voltage behaviour is underdamped. Therefore, the characteristic equation has complex conjugate roots. According to control theory [54], the characteristic equation of (3.4) is:
$0=s^{2}+\frac{R_{G}}{L_{e q}} s+\frac{1}{L_{e q} C_{i s s}}$

Comparing (3.5) with the canonical form of a second order system, the damping ratio $(\zeta)$, which represents the transient response, and the resonant frequency $\left(\omega_{n}\right)$ are expressed respectively as follows:

$$
\begin{align*}
\zeta & =\frac{R_{G}}{2} \sqrt{\frac{C_{i s s}}{L_{e q}}}  \tag{3.6}\\
\omega_{n} & =\frac{1}{\sqrt{C_{i s s} L_{e q}}} \tag{3.7}
\end{align*}
$$

According to the control theory, the general second-order system has three possible damping cases: underdamped $(\zeta<1)$, critically damped $(\zeta=1)$, and overdamped $(\zeta>1)$. The step response of the gate-loop varying damping ratio through using different $R_{G}$ is shown in Figure 3.3, illustrating the different voltage response of the RLC loop. Considering the underdamped response, the overshoot $(O S)$ of the RLC gate-loop can be calculated as follows [54]:
$O S=V_{G G}\left(1+e^{-\frac{\zeta \pi}{\sqrt{1-\zeta^{2}}}}\right)$

Taking into consideration the analysis in Section 3.3.1, the actual $O S$ of the gate voltage should be less than the upper limit voltage $\left(V_{G S m a x}\right)$. Therefore, a safety margin $(\mathrm{M})$ is added to ensure reliable operation.
$V_{G S m a x}=\frac{O S}{1-M}$

Accordingly, substituting (3.9) into (3.8), the damping ratio considering the safety margin is rewritten as follows:

$$
\begin{equation*}
\zeta=\frac{\ln (x)}{\sqrt{(\ln (x))^{2}+\pi^{2}}} \tag{3.10}
\end{equation*}
$$



Figure 3.3: Damping cases of second-order RLC gate-loop circuit.
where
$x=\left[1-\frac{V_{G S m a x}(1-M)}{V_{G G}}\right]$

Finally, by substituting (3.10) into (3.6), the optimal external gate resistance ( $R_{\text {gext }}$ ) can be calculated as as the following:
$R_{g e x t}=2 \sqrt{\frac{L_{e q}}{C_{i s s}}} \frac{\ln (x)}{\sqrt{(\ln (x))^{2}+\pi^{2}}}-R_{\text {gint }}$

Equation (3.11) clearly shows that minimising the gate and the power loops is necessary to dampen oscillations, and to thus increase the switching speed through using low $R_{\text {gext }}$.

The parasitic capacitance $C_{i s s}$ is taken from the datasheet, while the parasitic inductances are calculated as follows: Firstly, they are lumped into two groups: the internal parasitic inductance, which is a result of bonding between the SiC die and the package pads; and the external PCB trace inductance. The internal inductances are extracted from the LTspice model provided by the manufacturer, while the external inductances are analytically estimated using the rectangular conductor $\left(L_{\text {Rect }}\right)$ equation, which represents the PCB trace $[55,56]$ :
$L_{\text {Rect }}=\frac{\mu_{o} l}{2 \pi}\left(\ln \frac{2 l}{w+t}+0.22\left(\frac{w+t}{l}\right)+0.5\right)$
where $\mu_{o}$ is the permeability of air, $l$ is the average length of the path, and $w$ and $t$ are the width and thickness of the trace cross section. The extracted values of the internal and external inductances are given in Table 3.4. Thus, the optimal external gate resistances, considered for the optimal switching taking into account the previous analysis, are summarised in Table 3.3.

Table 3.4: Extracted parasitic inductance.

| Parasitic Terminals | Path Length <br> $(\mathrm{mm})$ | Internal Inductance <br> $(\mathrm{nH})$ | External Inductance <br> $(\mathrm{nH})$ | Total Inductance <br> $(\mathrm{nH})$ |
| :--- | :---: | :---: | :---: | :---: |
| $L_{G}$ | 18 | 8 | 12.2 | 20.8 |
| $L_{D}$ | 35 | 4 | 28.3 | 32.3 |
| $L_{S}$ | 10 | 6.8 | 5.7 | 12.5 |

### 3.4 Switching Characteristics of SiC MOSFETs

The standard double-pulse (DPT) circuit with inductive load is used to evaluate the switching performance of the transistors. The dynamic characterisation is done at different DC link voltages $\left(V_{d c}\right)$, load currents $\left(I_{o}\right)$, external gate resistances $\left(R_{\text {gext }}\right)$, and temperatures $\left(T_{c}\right)$. The schematic of the DPT circuit, as well the typical switching waveforms, are depicted in Figure 3.4. The gate-source voltage


Figure 3.4: DPT circuit: (a) schematic of DPT and (b) typical waveforms.
$\left(V_{g s}\right)$, drain-source voltage $\left(V_{d s}\right)$, and the drain-source current $\left(I_{d s}\right)$ at the end of the first pulse and at the beginning of the second pulse are recorded. This gives the dynamic turn-off and turn-on processes, respectively. The fast voltage/current switching waveforms are captured using the measurement tools listed in Table 3.2. However, the switching characteristics of SiC devices are evaluated with different


Figure 3.5: Freewheeling loop configurations: (a) internal BD, (b) external SBD and (c) SBD parallel to BD .
freewheeling loop (FWL) configurations depicted in Figure 3.5.
Case-I: Using the internal diodes as a FWD.
Case-II: External SiC Schottky diode, e.g. C4D10120A, acts as a FWD in FWL.
Case-III: External SBD connected parallel to the internal diode.
The dynamic behaviour of the DUTs is first measured with the internal-diode, case-I, and using an external SBD, case-II, by testing at 600 V and over a wide load current range. The switching losses are calculated directly from the measurement and are plotted in Figure 3.6 for C2M and SCT devices. At low load current level, the turn-on energy loss $\left(E_{o n}\right)$ using BD exhibits comparable results to


Figure 3.6: Switching energy loss of case-I and -II at $25^{\circ} \mathrm{C}$ : (a) C2M (b) SCT.
case-II, while using SBD reduces the losses at high current, due to a reduction of the reverse recovery effect. On the other hand, the turn-off loss $\left(E_{o f f}\right)$ exhibits a slight reduction using BD . This is mainly due to the current required to discharge the $\mathrm{SBD} / \mathrm{BD}$ junction capacitance, and this discharge current
is subtracted from the load current. Compared with the junction capacitance of the SBD, at 600 V , C2M and SCT devices have respectively approximately 1.8 and 2.4 times greater junction capacitance. Therefore, compared to case-II, a high discharge current is needed to discharge the output capacitance of SCT and C2M body-diodes, which explains the energy difference.

Furthermore, the high-temperature switching of the DUTs is evaluated up to $T_{c}=150^{\circ} \mathrm{C}$. The switching tests are performed with 600 V and up to 30 A load current. Applying case-I, Figure 3.7 depicts the turn-on switching waveforms of C2M and SCT devices. As shown, the turn-on transition of the planar technology is highly sensitive to the temperature, leading to significant increase of $52 \%$ in the turn-on loss, at $150{ }^{\circ} \mathrm{C}$, compared with room temperature value.


Figure 3.7: Impact of the BD on the turn-on switching waveforms with $25^{\circ} \mathrm{C}$ (blue) and $150{ }^{\circ} \mathrm{C}$ (red): a) planar device-C2M and b) double-trench device-SCT.

The reverse recovery characteristics of the planar SiC MOSFET's body-diode worsens as the temperature increases. This is because the reverse recovery current depends on the rate of the minority carrier recombination in the drift region, which is a function of the temperature. A higher temperature leads to an increase of the minority carrier lifetime in the drift region and hence an increase of the recovery current $[1,2,57,58]$. In contrast, the turn-on switching characteristics of the trench SiC MOSFET is less temperature-dependent. This is because the trench technology enables a significant increase in the channel current density, which results in a lower minority carrier lifetime compared to the planar technology [2]. Furthermore, using a SBD in case-II suppresses the reverse recovery of the planar device at high temperature and hence reduces the turn-on loss. Figure 3.8 compares the switching waveforms using the internal BD with case-II. As shown, the switching performance of case-II is less temperature dependent. Contrary to case-I, the turn-on loss reduces as temperature increases. This is a unique feature for these devices, and can be explained based on the PTC of the transconductance


Figure 3.8: Impact of planar BD (black) and SBD on the turn-on switching waveforms with $25^{\circ} \mathrm{C}$ (blue) and $150{ }^{\circ} \mathrm{C}$ (red).
and the NTC of the threshold voltage (see Figures 2.5 and 2.6). Therefore, the plateau voltage will decrease for a given load current, and a faster $\mathrm{di} / \mathrm{dt}$ and $\mathrm{dv} / \mathrm{dt}$ during the turn-on transient is achieved, resulting in lower loss [59, 60].

Further, the switching energy as a function of temperature is extracted and plotted in Figure 3.9. Applying case-I, the turn-off loss slightly increases as temperature increases. This is due to the reduction of the threshold and plateau voltages as temperature increases, causing slower slew voltage and current rates. Using SBD, the total switching energy loss $E_{t o t},\left(E_{t o t}=E_{o n}+E_{o f f}\right)$, is reduced at $150{ }^{\circ} \mathrm{C}$ compared to room temperature by around $12 \%$. On the other hand, the use of the BD exhibits an increase in the $E_{\text {tot }}$ by around $52 \%$ at $150{ }^{\circ} \mathrm{C}$ compared to room temperature, indicating a poor reverse recovery performance.

Lastly, the SCH device, which represents case-III, is evaluated. As expected, the behaviour is similar to case-II, where the internal SBD dominates the diode's switching behaviour. Thus, it can be concluded that the additional anti-parallel SBD, to eliminate the additional turn-on loss at high temperature, is still needed for the planar technology. Even though they have the same die size and using the benefits of SBD, the planar SCH device shows higher switching loss than the trench device (Figure 3.9-b). Therefore, attention must be paid when the antiparallel SBD is used; the higher junction capacitance of the SBD will increase the total output capacitance and hence slow down the switching speed.

### 3.5 Reverse Recovery Characteristic of SiC MOSFET Internal-Diode

The analysis of the previous Section shows that the reverse recovery of the planar devices BD is temperature dependent. Further, to utilise the BD as a freewheeling diode, some other factors, e.g.


Figure 3.9: Switching energy loss as function of temperature at 600 V and 20 A : (a) case-I (b) case-II and case-III.
forward current, input voltage, and gate resistance, are of importance to be considered to evaluate the switching process. Therefore, in addition to the case temperature, this section systematically evaluates the BD reverse recovery based on these operating factors.

As previously mentioned, the SiC MOSFET has an intrinsic PiN body-diode with a relatively high forward voltage compared to Si MOSFET body-diodes. In hard-switching applications, the reverse recovery effect of the PiN diode increases the switching losses in the diode, as well as in the complementary transistor, and in turn limits the switching frequency [1, 2]. For these reasons, manufacturers often recommend using an external parallel SiC SBD which has no reverse recovery current and a relatively low forward voltage drop. However, the SBD will lead to increased packaging complexity and device cost. Therefore, it is a feasible alternative to make use of the reverse conducting properties of the SiC MOSFET, so that the body-diode is only active during transistor dead times. A few publications have discussed the reverse recovery of the planar SiC devices. In [61], a comparison of the intrinsic diode of Si and SiC MOSFETs is presented, focusing on the forward and gate characteristics. Reference [62] investigates reverse recovery behaviour as a function of temperature and forward current and further examines the trade-off between the switching energy and electro-thermal robustness. The reverse recovery of the SiC MOSFET's body-diode at different current commutation slopes and a physics-based diode model is introduced in [41]. All of these studies of reverse recovery issues are based on a planar device technology. However, according to the author's knowledge, the reverse recovery of the body-diodes in the double-trench device has not yet been investigated. In this section, the internal diodes of the planar and trench devices are experimentally characterised in the DPT circuit with inductive load. Switching experiments are conducted up to $700 V_{d c}$ varying the
load current from 5 A to 40 A , and the case temperature from $25^{\circ}$ to $150^{\circ} \mathrm{C}$. Moreover, the recovery performance is evaluated, varying the current commutation slope by using different external gate resistances. Peak reverse recovery current $\left(I_{r r}\right)$, reverse recovery time $\left(t_{r r}\right)$, and total reverse recovery charge $\left(Q_{r r}\right)$ are evaluated at different operating points. Except for the experiments in section D , the optimal external gate resistors are chosen to achieve an optimum of high switching speed and small ringing, see Table 3.3.

## A- Variation of the Forward Current ( $I_{F}$ )

The effect of the forward current $\left(I_{F}\right)$ on the reverse recovery performance of the diodes is investigated at 600 V and $T_{c}=25^{\circ} \mathrm{C}$. Figure 3.10 depicts the current waveforms measured at different $I_{F}$. The switching characteristics of the SiC MOSFETs' body-diode have a very small forward current dependency, reducing the noise that might occur at a high load current. This is different from Si MOSFETs, where the reverse recovery current and other parameters also depend on the forward current.

## 

Figure 3.11 shows the effect of varying $V_{d s}$ on the recovery current of the trench device. The test is conducted with fixed $I_{d s}=20 \mathrm{~A}, T_{c}=25^{\circ} \mathrm{C}$ and variable $V_{d s}$ between 400 V and 600 V . There is only a very small impact on $I_{r r}$ visible. $Q_{r r}$, as well as $t_{r r}$, increase with the blocking voltage in all three investigated devices (see Figure 3.12-a) because the capacitive charge increases with the voltage level. A detailed analysis of this effect can be found in [57].

## $C$ - Variation of the Case Temperature ( $T_{c}$ )

In this test, the results are also obtained for 600 V and 20 A . Figure 3.13 depicts the measured waveforms at two different case temperatures. Due to the co-package with a discrete anti-parallel SBD, the reverse performance of the SCH device shows no noticeable change as the temperature increases. In case of the C 2 M device, $Q_{r r}$ and $t_{r r}$ increase with temperature, a quantitative evaluation of which is given in Figure 3.12-b. As mentioned before, see Section 3.4, this is due to the fact that the reverse recovery current depends on the rate of the minority carrier recombination in the drift region, which is a function of the temperature.

## D- Variation of the Gate Resistance ( $\boldsymbol{R}_{\text {gext }}$ )

In order to vary the current slope $d i / d t$, experiments are conducted with different external $R_{\text {gext }}$ for the low-side SiC MOSFET. Figure 3.14 depicts the results for operation at room temperature. As expected, both reverse current and reverse recovery charge decrease if the gate resistance increases. Comparing the C2M and the SCT device, the SCT trench body-diode exhibits a quite noticeable


Figure 3.10: Reverse recovery current of the SiC MOSFET internal diode a) C2M, b) SCH and c) SCT at 600 V and different $I_{F}$.


Figure 3.11: Reverse recovery current of trench SiC device body-diode at 20 A and different $V_{d s}$.
decrease. Adding SBD in parallel, as in the case of the SCH device, will result in greater energy loss at higher gate resistance due to charging the SBD junction capacitance, which is in parallel with the SiC MOSFET output capacitance $\left(C_{o s s}\right)$.

To summarise, the investigated SCT SiC trench MOSFET has an improved reverse recovery performance. With a well-adapted gate resistance for switching control, the total recovery charge is


Figure 3.12: Reverse recovery parameters of the DUTs at 20 A and a) different $\mathrm{V}_{d s} \mathrm{~b}$ )different $T_{c}$.


Figure 3.13: Reverse recovery current of the SiC MOSFET internal diode a) C2M, b) SCH and c) SCT at $600 \mathrm{~V}, 20 \mathrm{~A}$ and different $T_{c}$.
approximately $25 \%$ higher than for the SCH co-package with additional SBD. The SBDs are usually used to bypass the body-diode and hence eliminate the recovery effect, but also increase the packaging complexity and hence the cost. On the other hand, operating in SR mode could eliminate the need for an external SBD. The reverse current $I_{r r}$ of the trench- and of the planar SiC device show only a small


Figure 3.14: Reverse recovery current of the SiC MOSFET internal diode a) C2M, b) SCH and c) SCT at $600 \mathrm{~V}, 20 \mathrm{~A}$ and different $R_{\text {gext }}$.
dependency on the forward current and the blocking voltage. When compared to the planar technology, the reverse current and charge of the trench device are only slightly dependent on the temperature, which will considerably reduce the switching losses in hard-switching converters. Altogether, it can be concluded that adding SBD in parallel to the trench SiC MOSFET is not necessary.

## Chapter 4

## Analytical Switching Loss Model for SiC MOSFETs

### 4.1 Introduction

AN accurate model is needed to optimise and predict the switching behaviour of the SiC MOSFETs and hence to determine their limitation factors, e.g. thermal and switching frequency limits, at different operating conditions.

A detailed review of SiC MOSFET models presented in the literature is reported in [63], where the available models are categorised into five different levels depending on the modelling method used. The physics-based model of SiC devices is discussed in [64-68]. In most cases, it requires large computational effort and is difficult to use for circuit simulation. For simplicity, assumptions are made to obtain results at a fast simulation speed at the expense of accuracy. Therefore, the trade-off between model accuracy and computational effort is an important factor when special effects occurring in SiC MOSFETs are included.

On the other hand, the analytical model enables quick simulation times. Moreover, a physical insight into the switching device can be included, resulting in high accuracy and a good understanding of switching behaviour. A simple piecewise linear model is presented in [69, 70], where the parasitic inductance and capacitance are not included. Some references use the conventional modelling methods of a Si MOSFET to derive the SiC MOSFET model [71-74]. Authors in [75] propose a sub-circuit model for SiC half-bridge module implemented in circuit simulator PSpice. The proposed model
is used to optimise the switching loss. Some mismatch between model and measurement results are reported. An accurate second-order switching loss model for the high-frequency application is proposed in [76]. The characterisation and modelling of $10-\mathrm{kV} \mathrm{SiC} \mathrm{MOSFET} \mathrm{modules} \mathrm{is} \mathrm{presented} \mathrm{in}$ [77] using the power semiconductor tool in SaberRD.

The nonlinear characteristics of the drain-source capacitance in SiC MOSFETs is studied in [78, 79]. The results show that considering linear dependencies of parasitic capacitances on the voltage will lead to significant deviations between simulated and experimental results. The influence of the parasitic inductance on the oscillation occurring during the dynamic process has been investigated in detail in [71, 80-84].

In this chapter, an analytical model of the SiC MOSFET for switching loss optimisation is presented. The parasitic inductance, as well as the nonlinearity of the junction parasitic capacitance and transconductance, are considered. The effect of the case temperature on switching behaviour is also included and evaluated. In addition, the diversion phenomenon occurring as a result of the displacement current charging and discharging the parasitic capacitances is presented. Finally, the validation of the proposed model with experimental results is described in the last section.

### 4.2 Development of Circuit Model

The DPT circuit is used to derive the analytical model. Figure 4.1 shows the inductive switching circuit of the SiC MOSFET, considering the most crucial parasitic elements. The input and output are modelled as a constant voltage source $\left(V_{i n}\right)$, and constant current source $\left(I_{o}\right)$, respectively. The gate parasitic inductance $\left(L_{G}=L_{g i n t}+L_{g e x t}\right)$ includes the internal device package inductance $\left(L_{g i n t}\right)$ and external PCB trace parasitic inductance ( $L_{g \text { gext }}$ ). Likewise, $L_{S}$ and $L_{D}$ represent the internal and external inductances of the source and drain terminals, respectively. The common source parasitics inductance $\left(L_{G S}\right)$ represents the inductance shared between the gate and power loop. The nonlinear characteristics of input ( $C_{i s s}=C_{g s}+C_{g d}$ ), output ( $C_{o s s}=C_{d s}+C_{g d}$ ), and reverse transfer $\left(C_{r s s}=C_{g d}\right)$ parasitic capacitances of the $\operatorname{SiC}$ MOSFET are modelled as voltage-dependent [70, 74, 78]:
$C_{i o r}(v)=\frac{C_{i o r}}{\left(1+\frac{|v|}{k}\right)^{Y}}$
where $\mathrm{C}_{i o r}$ represents $C_{i s s}, C_{o s s}$ or $C_{r s s}$ at zero voltage; $k$ and $Y$ are two variable coefficients extracted from the datasheet; and $v$ is the applied voltage. The capacitance curves are fitted using the piecewise


Figure 4.1: The inductive switching circuit of SiC MOSFET considering the most crucial parasitics elements.
fitting for different voltage levels. The datasheet curves compared with model curves fitted by (4.1) are shown in Figure 4.2. The curves match well in a wide voltage range. In addition, the device transconductance $\left(g_{f s}\right)$ exhibits a nonlinear behaviour. The transconductance, as well as the threshold voltage parameters, have a temperature dependence (see Figures 2.5 and 2.6). In this study, the temperature dependence of the SiC MOSFET is considered by modelling the temperature-dependent parameters at different operating temperature points. However, the temperature-independent parameters are fixed at their room temperature values. The threshold voltage as a function of temperatures, $T_{c}$, can be expressed as:
$V_{t h}(T)=V_{t h o}+V_{t h 1}\left(T_{C}-T_{o}\right)$
where $V_{t h 0}$ is the threshold voltage at room temperature $T_{o}$ (e.g. for SCT device: $V_{t h 0}=4.2 \mathrm{~V}$ ) and $V_{t h 1}$ is the threshold voltage temperature coefficient $\left(-6.4 \mathrm{mV} /{ }^{\circ} \mathrm{C}\right)$.

### 4.3 Analysis of Turn-on Switching Process

The typical key waveforms of the turn-on process are shown in Figure 4.3. In this analysis, the body-diode of the SiC MOSFET is used in the FWL and a high load current is assumed. The turn-on


Figure 4.2: Comparison of C-V characteristics between datasheet and curve fitting of SCT device.
transition starts at $t_{0}$, where the body-diode is conducting. The turn-on process is divided into four stages, which are thoroughly discussed below.


Figure 4.3: Typical switching waveforms during turn-on and turn-off process.

## A- Delay Turn-On Time $\left(\boldsymbol{t}_{d-o n}\right)$

As the gate voltage ( $V_{\text {drive }}$ ) is applied, $C_{i s s}$ starts being charged. The time constant of the gate voltage's rising $\left(\tau_{1}=R_{G} C_{(\text {iss@600V) })}\right)$ is determined by $C_{i s s}$ and the total gate resistance $R_{G}\left(R_{G}=R_{\text {gint }}+R_{\text {gext }}\right)$. $C_{g d}$ does not play a significant role in this interval because it is relatively small compared to $C_{g s}$. This
interval ends when the gate-source voltage $\left(v_{g s}\right)$ reaches its $V_{t h}$ value. During this stage, the load current circulates through the BD , and the SiC MOSFET does not experience changes in the drain current $\left(i_{d s}\right)$ and drain-source voltage $\left(v_{d s}\right)$. The equivalent circuit of this stage is shown in Figure 4.4 and the following key equations are extracted:

$$
\begin{align*}
V_{d r i v e} & =v_{g s}+R_{G} i_{g}+\left(L_{G}+L_{G S}\right) \frac{d i_{g}}{d t}  \tag{4.3}\\
i_{g} & =C_{i s s} \frac{d v_{g s}}{d t} \tag{4.4}
\end{align*}
$$

## B- Current Rising-Time ( $t_{i r}$ )

In this stage, the channel current $\left(i_{c h}\right)$ starts conducting under control of $v_{g s}$. Simultaneously, $v_{d s}$ decreases as a result of the voltage drop $\left(\Delta V_{\text {drop }}\right)$ across the total power loop parasitic inductance ( $L_{\text {Loop }}$ ) induced by di ${ }_{d s} / \mathrm{dt}$.
$v_{d s}=V_{i n}+V_{f}-L_{\text {loop }} \frac{d i_{d s}}{d t}-L_{G S} \frac{d i_{g}}{d t}$

In this model, the parasitic inductances of the BD are neglected, therefore, $L_{\text {loop }}$ is defined as the sum of parasitic inductances of the lower side switch and the PCB traces.

The common source inductance $\left(L_{G S}\right)$ has a significant effect in this stage. Due to the negative feedback caused by $L_{G S}$, the rate of change of $v_{g s}$ is lower than in the previous stage.

$$
\begin{align*}
V_{d r i v e} & =v_{g s}+R_{G} i_{g}+L_{G} \frac{d i_{g}}{d t}+L_{G S}\left(\frac{d i_{d s}}{d t}+\frac{d i_{g}}{d t}\right)  \tag{4.6}\\
i_{g} & =C_{g s} \frac{d v_{g s}}{d t}+C_{g d}\left(\frac{d v_{g s}}{d t}-\frac{d v_{d s}}{d t}\right) \tag{4.7}
\end{align*}
$$

At the end of this period, $i_{d s}$ reaches $I_{o}$ and can be calculated by adding $i_{c h}\left[i_{c h}=g_{f s}\left(v_{g s}-V_{t h}\right)\right]$ to the discharging current of $C_{o s s}\left[C_{o s s}=C_{g d}+C_{d s}\right]$ :
$i_{d s}=g_{f s}\left(v_{g s}-V_{t h}\right)+C_{o s s} \frac{d v_{d s}}{d t}-C_{g d} \frac{d v_{g s}}{d t}$

It is worth to mention that the nonlinearity of $g_{f s}$ is considered in this phase, while the nonlinearity of the parasitic capacitances can be neglected and a constant capacitance value at a high voltage level (i.e. $V_{\text {in }}=600 \mathrm{~V}$ ) can be assumed.

## $C$ - Voltage Falling-Time ( $\boldsymbol{t}_{v f}$ )

As $i_{d s}$ reaches $i_{o}$, the FWD stops conducting and the reverse recovery process starts. The output parasitic capacitance of the FWD ( $C_{o s s F W}$ ) and the load inductor equivalent parallel capacitance $\left(C_{L}\right)$ start being charged through the forward current $I_{F}\left[I_{F}=I_{d s}-I_{o}\right]$. The nonlinearity of the parasitic capacitance $\left(\mathbf{C}_{i o r}=f(v)\right)$ is considered in this phase. The nonlinear behaviour of $C_{g d}$ has a great impact on the $v_{d s}$ slew rate. The case is similar to interval-B, in addition to (4.5)-(4.8), the following additional equation is obtained:

$$
\begin{equation*}
\frac{d v_{f}}{d t}=\frac{1}{C_{o s s F W}}\left(i_{d s}-I_{o}\right) \tag{4.9}
\end{equation*}
$$

## D- Gate Voltage Rising Period

In this stage, the device is fully turned-on and can be modelled as a resistor, $R_{D S o n} . v_{g s}$ continues to increase with a relatively high time constant $\left(\tau_{2}=R_{G} C_{(i s s @ V D S o n)}, \tau_{2}>\tau_{1}\right)$. The total parallel connection capacitance $\left(C_{t o t}\right)$ of $C_{o s s F W}$ and $C_{L}$ tends to resonate with $L_{L o o p}$. The total loop resistance ( $R_{\text {Loop }}$ ) includes $R_{D S o n}$ and the equivalent series resistance of the PCB traces representing the highfrequency damping resistance dissipating the resonant energy. The differential equations are as follows:
$i_{d s}=I_{o}+C_{o s s} \frac{d v_{d s}}{d t}-C_{g d} \frac{d v_{g s}}{d t}$
$v_{f}=V_{\text {in }}-L_{\text {loop }} \frac{d i_{d s}}{d t}-R_{\text {loop }} i_{d s}$

As $v_{d s}$ reaches the on-state voltage $\left(v_{D S o n}\right)$, the nonlinear behaviour of the parasitic capacitance can be neglected and assumed as a constant at $v_{D S o n}$ level.

### 4.4 Analysis of Turn-off Switching Process

Before the turn-off process starts, the load current conducts through the SiC device, while the BD is blocking the input voltage. As is shown in Figure 4.3, the turn-off process can be divided into four intervals.

## A- Delay Turn-off Time ( $\boldsymbol{t}_{d-o f f}$ )

When the gate voltage is pulled down to $V_{d r i v e-o f f}\left(e . g . V_{d r i v e-o f f}=-2 \mathrm{~V}\right), C_{i s s}$ is being discharged


Figure 4.4: Equivalent circuits during turn-on and -off transitions: a) [stage A-on and D-off], b) [stage B-on and C-off], c) [stage C-on and B-off] and d) [stage D-on and A-off].
with the time constant $\tau_{2}$ dominated by $C_{g s} . v_{d s}$ remains constant at $v_{D S o n}$ level, and $I_{o}$ remains conducting through the MOSFET channel. Since $i_{d s}$ remains unchanged, the effect of $L_{G S}$ can be neglected. At the end of this stage, $v_{g s}$ reduces to the Miller voltage level $V_{m 1}$ :
$V_{m 1}=\left.v_{g s}\right|_{t_{6}}=\frac{i_{d s}}{g_{f s}}+V_{t h}$

The equivalent circuit of this stage is shown in Figure 4.4, from which the following key equations can be derived:

$$
\begin{align*}
V_{d r i v e-o f f} & =v_{g s}+R_{G} i_{g}+\left(L_{G}+L_{G S}\right) \frac{d i_{g}}{d t}  \tag{4.13}\\
i_{g} & =C_{i s s} \frac{d v_{g s}}{d t} \tag{4.14}
\end{align*}
$$



Figure 4.5: Capacitances charging and discharging during voltage rising interval.

## B- Voltage Rising Time ( $t_{v r}$ )

In this stage, $v_{d s}$ increases to $V_{i n}$ with the speed of the slew rated depending primarily on the nonlinearity of $C_{g d}$. As illustrated in Figure 4.5, $C_{\text {tot }}$ is discharged through $I_{F}\left(I_{F}=I_{C L}+I_{\text {CossFW }}\right)$, causing a drop in $i_{d s}$. Whereas the charging current of $C_{g d}$ and $C_{d s}\left(I_{c o s s}=I_{c d s}+I_{c g d}\right)$ makes $I_{c h}$ divert from $I_{d s}\left(I_{c h}<I_{d s}\right)$.

In other words, the discharging current $I_{F}$ of $C_{t o t}$ is subtracted from $I_{o}$, so that the measured $i_{d s}$ decreases from $I_{o}$ to $i_{d s 7}$ at $t_{7}$ (see Figure 4.6). In addition, due to the charging current $i_{\text {coss }}$ of $C_{o s s}, i_{c h}$ drops down to another current level $\left(i_{c h 7}\right)$. Thereby, the new values of $i_{d s 7}$ and $i_{c h 7}$ can be recalculated respectively as follows:

$$
\begin{align*}
& i_{d s 7}=I_{o}-\left(C_{o s s F w}+C_{L}\right) \frac{d v_{d s}}{d t}  \tag{4.15}\\
& i_{c h 7}=i_{d s 7}-C_{o s s} \frac{d v_{d s}}{d t} \tag{4.16}
\end{align*}
$$

The current diversion phenomenon that occurs as a result of the displacement current charging and discharging the parasitic capacitances is explained in more detail in the next section.

Accordingly, at the end of this stage, $v_{g s}$ reaches another voltage level:
$V_{\text {drive }-o f f}=v_{g s}+R_{G} i_{g}+L_{G} \frac{d i_{g}}{d t}+L_{G S}\left(\frac{d i_{d s}}{d t}+\frac{d i_{g}}{d t}\right)$

## C- Current Falling Time $\left(t_{i f}\right)$

As the FWD becomes forward-biased, the current $i_{d s}$ starts to decrease until it reaches zero, while $v_{g s}$ drops to $V_{t h}$ with a time constant $\tau_{1}$. In this stage, the voltage induced across $L_{L o o p}$ adds an extra voltage stress across the SiC MOSFET. Further, the voltage across the BD can be expressed as follows:
$v_{f}=R_{B D}\left(I_{o}-i_{d s}\right)+V_{B D F W}$
where $R_{B D}$ is the body-diode forward resistance and $V_{B D F W}$ is the built-in voltage.

## D- Gate Voltage Falling Period

During this phase, the device operates in the cutoff region, and $v_{g s}$ decreases to $V_{d r i v e-o f f}$. The parasitic inductance tends to resonate with $C_{o s s}$, causing ringing in $v_{d s}$ and $i_{d s}$. This ringing is being dampened by the total high-frequency loop resistance $R_{\text {Loop }}$ existent in the circuit. In this stage, the differential equations that describe the switching behaviour can be derived as follows:
$i_{d s}=C_{o s s} \frac{d v_{d s}}{d t}-C_{g d} \frac{d v_{g s}}{d t}$
$v_{d s}=V_{i n}+v_{f}-L_{\text {loop }} \frac{d i_{d s}}{d t}-L_{G S} \frac{d i_{g}}{d t}-R_{\text {loop }} i_{d s}$

This interval is valid as long as $v_{g s}$ is kept at turn-off voltage level, $\left(v_{g s}=V_{d r i v e-o f f}\right)$.

Finally, the equations at each stage can be written in state-space form:
$\left\{\begin{array}{l}\dot{\boldsymbol{x}}=\boldsymbol{A} x(t)+\boldsymbol{B} \\ x\left(t_{o}\right)=\boldsymbol{x}_{o}\end{array}\right.$

Where $\boldsymbol{A}$ is a $5 \times 5$ matrix, and $\boldsymbol{B}$ is $1 \times 5$ matrix, $\boldsymbol{x}_{o}$ is $5 \times 1$ matrix that includes the initial conditions. By sorting (4.3)-(4.20), a set of nonlinear differential equations is obtained with the following state variables:
$\mathbf{x}=\left[\begin{array}{lllll}v_{d s} & i_{d s} & v_{g s} & i_{g} & v_{f}\end{array}\right]^{T}$
The solutions of these equations are implemented in MATLAB; the final results from each stage
form the initial conditions for the next one. The Matrices $\boldsymbol{A}[5 \times 5]$ and $\boldsymbol{B}[5 \times 1]$, which describe the complete proposed model, are summarised in Appendix B.

### 4.5 Displacement Current Phenomenon During Turn-off Process

The diversion phenomenon, during the turn-off process, occurs as a result of the displacement current charging and discharging the parasitic capacitances. This phenomenon becomes more relevant during stages B-off and C-off, where the strong nonlinear capacitance has a significant effect. However, this effect rarely is discussed and considered for potential incorporation into a model [85].


Figure 4.6: Key turn-off switching waveforms including the displacement current.

During Stage B $\left(t_{6}-t_{7}\right)$ (see Figure 4.6), $v_{d s}$ increases and $C_{t o t}$ is discharged through $I_{F}$ causing $i_{d s}$ drop to $i_{d s 7}$. The dv/dt strongly depends on the nonlinear behaviour of $C_{g d}$ :
$i_{d s 7}(t)=I_{o}-C_{t o t}\left(v_{d s}\right) \frac{V_{i n}-V_{D S o n}}{t_{v r}}$
where $t_{v r}$ represents the voltage rising time which is a function of $C_{g d}$, as will be explained in Section 4.6. Furthermore, the total parasitic inductance $L_{\text {loop }}$ dominates $\mathrm{di}_{d s} / \mathrm{dt}$, resulting in faster $\mathrm{di}_{c h} / \mathrm{dt}$ compared with $\mathrm{di}_{d s} / \mathrm{dt}\left(\mathrm{di}_{d s} / \mathrm{dt}<\mathrm{di}_{c h} / \mathrm{dt}\right)$. In consequence, as is illustrated in Figure $4.6, v_{g s}$ decreases
from $V_{m 1}$ to another miller voltage $V_{m 2}$.
$V_{m 2}=V_{t h}+\frac{i_{o}(t)-\left[C_{t o t}\left(v_{d s}\right)+C_{o s s}\left(v_{d s}\right)\right] \frac{V_{\text {in }}-V_{\text {DSon }}}{t_{v r}}}{g_{f s}}$

Practically, the channel current cannot be measured. Thus, $i_{c h}$ is analytically calculated using (4.24), considering the nonlinear behaviour of the of the parasitic capacitance for a given measured waveform:
$i_{c h}(t)=i_{o}(t)-\left[C_{t o t}\left(v_{d s}\right)+C_{o s s}\left(v_{d s}\right)\right] \frac{V_{i n}-V_{D S o n}}{t_{v r}}$

Consequently, the $C_{o s s}$ charging current diverts from $i_{c h}$, and $i_{c h}<i_{d s}$. Thus, the real turn-off switching energy loss, calculated based on the overlap between $i_{c h}$ and $v_{d s}$, will be smaller than the measured loss, which considers $i_{d s}$ (see Figure 4.6).

According to the aforementioned analysis, different factors can affect the displacement current. The magnitude of displacement current is proportional to the load current level, the voltage slew rate and the parasitic capacitances, as will be discussed in the following.

## A- Load Current

Figure 4.7 depicts the measured switching waveforms including the calculated $i_{c h}$ with two different load currents: $I_{o}=5 \mathrm{~A}$ and 20 A , while fixed $R_{\text {gext }}=3 \Omega$. For both current levels, the falling process of $i_{d s}$ and also $i_{c h}$ is observed during the Miller period. In the case of light load ( $I_{o}=5 \mathrm{~A}$ ), the channel current reaches zero before the moment where $v_{d s}$ reaches $V_{i n}\left(t_{7}\right)$, the remaining $i_{d s}$ flowing through $C_{\text {oss }}$ as illustrated in Figure 4.8.

In contrast, with load current $I_{o}=20 \mathrm{~A}$, the channel current still conducts after $t_{7}$, and $i_{d s 7}$ starts to fall at $t>t_{7}$. In both cases, the green dashed area represents the rate at which charge flows through the output parasitic capacitance (capacitance charging current $I_{\text {coss }}$ ). With low current level, lower miller voltage is expected and higher turn-off time $t_{v r}$ is needed, therefore the charging speed is slower, thus determining the $\mathrm{dv}_{d s} / \mathrm{dt}$. Conversely, at high load current, the sequence of the switching phases is reversed. At fixed gate resistance and temperature, turn-off slew rate $\mathrm{d} i_{d s} / \mathrm{dt}$ and $\mathrm{d} V_{d s} / \mathrm{dt}$ increases with load current, as predicted by (4.12).

## B- Parasitic Capacitance / Different FWL Configurations

Furthermore, to investigate the effect of using different freewheeling configurations and different output parasitic capacitances, SBD with a small capacitance, such as 40 pF , is used as FWD. Compared with the BD case, even with small currents, using SBD enables $i_{c h}$ to conduct after $t_{7}$ and fully turn-off


Figure 4.7: Switching waveforms including $\mathrm{i}_{c h}$ during turn-off using BD and SBD for (a) $\mathrm{I}_{o}=5 \mathrm{~A}$ and (b) $\mathrm{I}_{o}=20 \mathrm{~A}$.


Figure 4.8: SiC MOSFET operation with $I_{o}=5 \mathrm{~A}$ (a) $t<t_{7}$ and (b) $t>t_{7}$.
after $v_{d s}$ reaches $v_{i n}$, leading to increasing turn-off loss. As depicted in Figure 4.7, for simplicity assume the same $\mathrm{d} v_{d s} / \mathrm{dt}$, using small junction capacitance (such as using SBD ) in the FWL reduces the required displacement current, and thus increases $I_{d s}$ at $t_{7}$.

## C- External Gate Resistance

Further, the effect of varying $R_{\text {gext }}$ on the diversion phenomenon is illustrated in Figure 4.9. Different falling current levels of $i_{d s 7}$ are observed. The discharging current $I_{\text {cossFW }}$ shows a noticeable decrease as $R_{\text {gext }}$ increases. As depicted, using $R_{g e x t}=0 \Omega, i_{d s}$ starts falling with $i_{d s 7}=11 \mathrm{~A}$ compared to 17 A at lower $\mathrm{d} v_{d s} / \mathrm{dt}\left(R_{\text {gext }}=33 \Omega\right)$. A small $R_{\text {gext }}$ charges/discharges the parasitic capacitance in short time with high $I_{\text {coss }} / I_{\text {cossFW }}$, respectively. Conversely, due to the large charging/discharging time required, a lower $\mathrm{d} v_{d s} / \mathrm{dt}$ is expected using large $R_{\text {gext }}$. Hence, a small displacement current is achieved, as predicted by (4.22).


Figure 4.9: Measured voltage and current waveforms including displacement current at different gate resistance.

A large $\mathrm{d} i_{c h} / \mathrm{dt}$ could lead to kind of soft or partial soft switching depending on the load current level. Figure 4.10 shows the measured waveforms applying different input voltages and a constant output power $P_{o}=1 \mathrm{~kW}$. The turn-off energy loss is calculated considering the measured $i_{d s}$ and compared with the calculated $i_{c h}$ using (4.24). In all cases, $i_{d s}$ reaches zero before $\mathrm{v}_{d s}=\mathrm{V}_{i n}$, which effectively reduces the turn-off energy $E_{o f f}$. Including the displacement phenomenon, $E_{o f f}$ is reduced by around $60 \%$ at $V_{d s}=800 \mathrm{~V}$. Fast di $\mathrm{ch}_{h} / \mathrm{dt}$ at $V_{d s}=400 \mathrm{~V}$ avoids the additional energy loss comparable to $V_{d s}=$ 800 V , this could be explained by (4.24) where different dv/dt are achieved at the same output power. High dv/dt leads to a reduction in the overlap interval between voltage and channel current, thus minimising the overlap loss interval. [As previously mentioned, using low switching current results in
lower $\mathrm{d} v_{d s} / \mathrm{dt}$, and that explains the low slew rate in Figure 4.10].


Figure 4.10: Turn-off energy loss comparison considering $i_{d s}$ (solid) and $i_{c h}$ (dashed) at $P_{o}=1 \mathrm{~kW}$.

In summary, the measured results show that the charging and discharging currents of the parasitic capacitance should be taken into consideration for an accurate model and cannot be neglected. In addition, the displacement current can be exploited when soft switching is required. The fast $\mathrm{d} i_{c h} / \mathrm{dt}$ could lead to ZCS at a low current levels and partial soft switching at a high current levels.

### 4.6 Switching Time and Switching Loss Calculations

The proposed analytical model is used to calculate the switching time and switching losses depending on the switching waveforms. In each interval, the average gate current and the drain-source voltage slew rate are used to calculate the switching time.

## A) Turn-on Switching Time and Loss Calculation

Through the turn-on transition, the switching losses are calculated during intervals where current is rising $t_{i r}$ and voltage is falling $t_{v f}$. For the $t_{i r}$ period, the average gate current $I_{g i r}$ can be expressed as follows:
$I_{g i r}=\frac{\left(V_{\text {drive }-o n}-0.5\left(V_{m-o n}+V_{t h}\right)-\left(L_{G S} I_{d s}\right) / t_{i r}\right)}{R_{G}}$
Rewriting $t_{i r}$ using (4.7) yields
$t_{i r}=\frac{C_{i s s}\left(V_{m-o n}-V_{t h}\right)+C_{g d}\left(V_{i n}-V_{d s 2}\right)}{I_{g i r}}$
where $V_{d s 2}$ is calculated at $t_{2}$ as follows (see Figure 4.3):
$V_{d s 2}=V_{\text {in }}-L_{\text {loop }} \frac{\Delta i_{d s}}{\Delta t}, \quad$ where $\left.\frac{\Delta i_{d}}{\Delta t}\right|_{t_{i r}}=\frac{I_{o}}{t_{\text {ir }}}$

Solving for $t_{i r}$ using (4.8), (4.25)-(4.27) yields:
$t_{i r}=\frac{-b_{i r}+\sqrt{b_{i r}^{2}-4 a_{i r} c_{i r}}}{2 a_{i r}}$
where:
$a_{i r}=V_{\text {drive }-o n}-0.5\left(V_{m-o n}+V_{t h}\right)$
$b_{i r}=-\left(R_{G} C_{i s s}+g_{f s} L_{G S}\right)\left(V_{m-o n}-V_{t h}\right)$
$c_{i r}=-g_{f s} R_{G} C_{g d} L_{\text {loop }}\left(V_{m-o n}-V_{t h}\right)$

Since $C_{g d} \times L_{\text {loop }}$ is relatively small and can be neglected, $t_{i r}$ can thus be further simplified to the following:
$t_{i r}=\frac{\left(R_{G} C_{i s s}+g_{f s} L_{G S}\right)\left[V_{m-o n}-V_{t h}+\sqrt{V_{m-o n}-V_{t h}}\right]}{2\left[V_{\text {drive }-o n}-0.5\left(V_{m-o n}+V_{t h}\right)\right]}$

In the same manner, during voltage fall time $t_{v f}$, the average gate current $I_{g v f}$ can be expressed as follows:
$I_{g v f}=\frac{V_{d r i v e-o n}-V_{m-o n}-C_{t o t}\left(V_{d s 2}-V_{D S o n}\right) /\left(g_{f s} t_{v f}\right)}{R_{G}}$
$C_{g d}$ significantly increases and strongly influences the voltage slew rate $\mathrm{dv}_{\mathrm{ds}} / \mathrm{dt}$ :
$t_{v f}=\frac{C_{g d}\left(V_{d s 2}-V_{D S o n}\right)}{I_{g v f}}$

Using (4.9), (4.27), (4.30) and (4.31), $t_{v f}$ is solved as:
$t_{v f}=\frac{R_{G} C_{g d}\left(V_{d s 2}-V_{D S o n}\right)+C_{t o t} \frac{\left(V_{d s 2}-V_{D S o n}\right)}{g_{f s}}}{\left(V_{d r i v e-o n}-V_{m-o n}\right)}$

Moreover, the switching energy losses during $t_{i r}$ and $t_{v f}$ are calculated from the switching waveforms:

$$
\begin{equation*}
E_{o n}=E_{o n-t i r}+E_{o n-t v f} \tag{4.33}
\end{equation*}
$$

Where:

$$
\begin{align*}
E_{\text {on-tir }} & =\int^{t_{i r}} i_{d s} v_{d s} d t \\
& =\frac{1}{2} I_{o}\left[t_{i r} V_{\text {in }}-g_{f s} L_{\text {Loop }}\left(V_{m-o n}-V_{t h}\right)\right]  \tag{4.34}\\
E_{\text {on-tvf }} & =\int^{t_{v f}} i_{d s} v_{d s} d t \\
& =\frac{1}{2}\left[t_{v f} I_{o}\left(V_{d s 2}+V_{D S o n}\right)+C_{\text {tot }}\left(V_{d s 2}^{2}-V_{D S o n}^{2}\right)\right] \tag{4.35}
\end{align*}
$$

## B) Turn-off Switching Time and Loss Calculation

Likewise, the switching losses during turn-off process are calculated over $t_{v r}$ and $t_{i f}$ intervals. The average gate current $I_{g v r}$ during $t_{v r}$ is given by the:
$I_{g v r}=\frac{0.5\left(V_{m 1}+V_{m 2}\right)-V_{\text {drive }-o f f}}{R_{G}}$
where $V_{m 1}$ and $V_{m 2}$ are calculated with help of $I_{o}$ and $I_{d s} 7$, respectively. $C_{g d}$ significantly decreases and strongly influences the voltage slew rate $\left(d v_{d s} / d t\right)$ :
$t_{v r}=\frac{C_{g d}\left(V_{i n}-V_{D S o n}\right)}{I_{g v r}}$

Solving for $t_{v r}$ using (4.22)-(4.24), (4.36) and (4.37) yields:
$t_{v r}=\frac{C_{g d} R_{G}\left(V_{i n}-V_{D S o n}\right)+0.5\left(C_{o s s}+C_{t o t}\right) \frac{\left(V_{\text {in }}-V_{D S o n}\right)}{g_{f s}}}{V_{m 1}-V_{d r i v e-o f f}}$
During $t_{i f}, v_{g s}$ drops to $V_{t h}$ with time constant $\tau_{1}$, dominated mainly by $C_{o s s}$. The average gate current $I_{g i f}$ and voltage slew rate $d v_{d s} / d t$ are calculated respectively as:
$I_{g i f}=\frac{0.5\left(V_{m 2}+V_{t h}\right)-V_{d r i v e-o f f}-L_{G S} \frac{\Delta i_{d s 7}}{\Delta t_{i f}}}{R_{G}}$
$t_{i f}=\frac{C_{i s s} I_{d s 7}}{g_{f s} I_{g i f}}$
Solving for $t_{i f}$ using (4.16), (4.18), (4.35), and (4.36) yields:
$t_{i f}=\frac{-b_{i f}+\sqrt{b_{i f}^{2}-4 a_{i f} c_{i f}}}{2 a_{i f}}$
Where:
$a_{i f}=0.5\left(V_{m 2}+V_{t h}\right) g_{f s}-g_{f s} V_{d r i v e-o f f}$
$b_{i f}=-I_{d s 7}\left(g_{f s} L_{G S}+R_{G} C_{i s s}\right)$
$c_{i f}=0$

The switching energy losses during $t_{v r}$ and $t_{i f}$ are calculated from the switching waveforms as follows:

$$
\begin{equation*}
E_{o f f}=E_{o f f-t v r}+E_{o f f-t i f} \tag{4.42}
\end{equation*}
$$

Where:

$$
\begin{align*}
E_{o f f-t v r} & =\int^{t_{v r}} i_{d s} v_{d s} d t \\
& =\frac{1}{2} t_{v r}\left(V_{i n} i_{d s 7}-V_{D S o n} I_{o}\right)  \tag{4.43}\\
E_{o f f-t i f} & =\int^{t_{i f}} i_{d s} v_{d s} d t \\
& =\frac{1}{2}\left[t_{i f} V_{i n} I_{c h}+L_{G S} i_{c h 7}^{2}\right] \tag{4.44}
\end{align*}
$$

### 4.7 Validation and Discussion of the Proposed Model

The experimental validation of the proposed model is carried out by means of DPTs with the SCT device. The parasitic inductances in the power and gate loops are extracted using (3.12). A comparison between the proposed model and measurement results at different input voltages (e.g. $V_{\text {in }}=400 \mathrm{~V}$ and 600 V ) and fixed $R_{\text {gext }}=3 \Omega$ and $T_{c}=25^{\circ} \mathrm{C}$ is depicted in Figure 4.11 and Figure 4.12, respectively. The variable parameters for different input voltages, such as $C_{i o r}(V)$ and $C_{F W}(V)$, are considered.

The analytical model exhibits close agreement with measurement during both turn-on and turn-off transitions.


Figure 4.11: Comparison of analytical and experimental switching waveforms at $V_{d s}=600 \mathrm{~V}, I_{d s}=$ $20 \mathrm{~A}, R_{\text {gext }}=3 \Omega$ and $T_{c}=25^{\circ} \mathrm{C}$, Time base: $20 \mathrm{~ns} /$ div.


Figure 4.12: Comparison of analytical and experimental switching waveforms at $V_{d s}=400 \mathrm{~V}, I_{d s}=$ $20 \mathrm{~A}, R_{\text {gext }}=3 \Omega$ and $T_{c}=25^{\circ} \mathrm{C}$ Time base: $20 \mathrm{~ns} / \mathrm{div}$.

The model is further validated using different gate resistances. Figure 4.13 depicts the measurement and simulated model results at $R_{g}=20 \Omega, V_{i n}=600 \mathrm{~V}$, and $I_{o}=20 \mathrm{~A}$. Compared to Figure $4.11\left(R_{\text {gext }}\right.$ $=3 \Omega$ ), using a large $R_{\text {gext }}$ reduces the switching speed, thereby decreasing the device voltage/current stresses. The gate resistance determines the magnitude of the gate current and thus $\mathrm{di}_{\mathrm{ds}} / \mathrm{dt}^{\text {and }} \mathrm{dv}_{\mathrm{ds}} / \mathrm{dt}$. It should be noted that the reverse recovery effect is considered here. The reverse recovery charge $Q_{r r}$ is calculated based on the measured waveforms and added to the model. The experimental results
show that the reverse recovery charge decreases exponentially with the gate resistance ( $Q_{r r}$ decreases from 360 nC at $R_{\text {gext }}=0 \Omega$ to 80 nC at $R_{\text {gext }}=30 \Omega$ ). In summary, the analytical model effectively tracks the oscillation during both turn-on and turn-off transitions. Furthermore, the switching losses calculated from the analytical model, based on (4.33) and (4.42), are compared with those from the measurement. Figure 4.14 illustrates a comparison between the energy losses calculated from the experimental and analytical models at different gate resistances.


Figure 4.13: Comparison of analytical and experimental switching waveforms at $V_{d s}=600 \mathrm{~V}, I_{d s}=$ 20 A and $R_{\text {gext }}=22 \Omega$, Time base: $50 \mathrm{~ns} /$ div.


Figure 4.14: Switching losses comparison between experimental and calculation results based on the proposed model under influence of $R_{\text {gext }}$ and $I_{d s}=20 \mathrm{~A}$.

At a high current, a slight difference in the turn-on energy loss is observed. This is mainly due to the absence of the physical meaning of the reverse recovery characteristic. The model is further validated at a different load currents (see Figure 4.15-a). Both turn-on and -off switching losses increase with the
load current. The turn-off loss does not increase as fast as the turn-on losses because of the reduction in the turn-off time. According to (4.36)-(4.44), this behaviour is primarily due to the fact that a higher drain current leads to a higher miller voltage, which in turn increases the gate discharge current and hence reduces the turn-off time. The proposed model agrees well with experimental results over a wide load current range. The impact of the displacement current on turn-off energy loss is further depicted in Figure 4.15-a. At $I_{o}=20 \mathrm{~A}$, for example, the case considering displacement phenomenon estimates the $E_{\text {off }}$ around $83 \%$ of the measured value compared to $95 \%$ when the displacement current is excluded. The effect of current diversion is more pronounced at low current. Including displacement current, $I_{o}=5 \mathrm{~A}, E_{\text {off }}$ is analytically estimated around $57 \%$ compared to $86 \%$ at $I_{o}=30 \mathrm{~A}$.


Figure 4.15: Switching losses comparison between experimental and calculation results based on the proposed model under influence of (a) load current and (b) temperature.

Another advantage of SiC devices is their temperature capability. The analytical model is further validated for wide case temperature range ( $T_{c}: 25^{\circ} \mathrm{C}-150^{\circ} \mathrm{C}$ ). The temperature dependency of $g_{f s}$ and $V_{t h}$ are considered. In order to accurately estimate the device losses, the temperature dependence of the reverse recovery charge of the body-diode should be included. The experimental switching losses compared with analytical calculations as a function of $T_{c}$ are shown in Figure 4.15-b.

In summary, the analytical model exhibits quite close agreement with measurement results at different test conditions. Further, the proposed model tracks the oscillation effectively during both turn-on and -off transitions. This has been achieved by considering the influence of the most crucial parasitic elements in both power and gate loops. In addition, the diversion phenomenon is considered and evaluated. Both the measurement and the model results show that the charging and discharging currents of the parasitic capacitance should be taken into consideration and cannot be neglected.

## Chapter 5

## Switching-Frequency and Thermal Limitation

### 5.1 Introduction

THE high thermal conductivity of SiC , combined with low losses, allows the SiC devices to operate at high temperatures and high-frequency conditions. Moreover, high-switching frequency leads to reductions in the size and cost of the passive components, allowing overall power density to be improved. On the other hand, when high power density is required, optimal thermal design becomes more challenging. An inefficient cooling system will limit the utilisation of potential benefits of SiC devices in power converters.

Therefore, in this chapter, a general electro-thermal model for high-power, high-frequency DC/DC converter design is discussed. The frequency and thermal limitations are applied to design a very high switching frequency converter operated continuously with 1 MHz . Subsequently, a $10 \mathrm{~kW} / 100-250$ kHz hard switching converter is designed and tested under different operating conditions, analysing the impact of the body-diode. Furthermore, to increase the output power of the converter, the parallel operation of the considered planar MOSFETs is tested and evaluated.

### 5.2 Electro-Thermal Model

The electro-thermal model integrates both the electrical and thermal performance of the SiC devices. Figure 5.1 illustrates the combined electro-thermal model used to estimate the junction temperature of the SiC MOSFET.


Figure 5.1: Iterative process to calculate maximum allowed frequency and junction temperature.

### 5.2.1 Electrical Model

The electrical part includes the static and switching losses model of SiC MOSFETs. The accuracy of this model is improved by including the temperature-dependent parameters. The analytical power loss model presented in the previous chapter is used to predict the switching loss, while the static loss is calculated using the temperature dependence of $R_{D S o n}$. Analytically, on-state resistance as a function
of junction temperatures, $\left(T_{j}\right)$, can be linearly expressed as follows:
$R_{D S o n}\left(T_{j}\right)=R_{D S o n 0}\left[1+\alpha_{r}\left(T_{j}-T_{o}\right)\right]$
where $R_{D S o n 0}$ is the on-state resistance at room temperature $T_{o}$ (e.g. for SCT device: $R_{D S o n 0}=41 \mathrm{~m} \Omega$ ) and $\alpha_{r}$ is the on-state resistance coefficient (e.g. $\alpha_{S C T}=5.27 \mathrm{~m} \Omega /{ }^{\circ} \mathrm{C}$ ).

Thus, the conduction loss ( $P_{\text {cond }}$ ), at a specific drain-source RMS current ( $I_{d s-r m s}$ ) over the on-time duty cycle, $\left(D_{\text {cycle }}\right)$, can be calculated as:
$P_{\text {cond }}\left(T_{j}\right)=D I_{d s-r m s}^{2} R_{D S o n 0}\left[1+\alpha_{r}\left(T_{j}-T_{o}\right)\right]$

In addition, the switching power loss is calculated with help of the energy losses during turn-on and -off transitions derived in the previous chapter:
$P_{S W}\left(T_{j}\right)=f_{s w}\left[E_{o n}\left(V_{d s}, I_{d s}, T_{j}\right)+E_{o f f}\left(V_{d s}, I_{d s}, T_{j}\right)\right]$
where $f_{s w}$ is the switching frequency.

### 5.2.2 Thermal Model

A water cooling system is used to cool the devices and measure the power loss generated by SiC MOSFETs and diodes based on the calorimetric principle, allowing for the separation of the semiconductor and other losses such as magnetic losses. In this case, the power loss ( $P_{\text {loss }}$ ) of the semiconductor devices can be determined as a function of the temperature difference $(\Delta T)$ between the inlet and outlet water temperature, the heat capacity $\left(c_{p}\right)$, and the mass flow of the liquid $(m)$ :

$$
\begin{equation*}
P_{\text {loss }}=m c_{p} \Delta T \tag{5.4}
\end{equation*}
$$

The SiC devices are mounted on the heatsink with insulation material. This material has a significant effect on the total thermal resistance and hence reduces the maximum allowable power dissipation. Therefore, the thermal resistance ( $R_{t h, C A}$ ) of the dielectric material should be as low as possible and meet other requirements, such as breakdown voltage. Thus, a 6 kV breakdown voltage and a thermal resistance of $0.2^{\circ} \mathrm{C} / \mathrm{W}$ insulation material is used. The equivalent thermal circuit from junction of the

SiC device to the ambient is shown in Figure 5.2.


Figure 5.2: Physical structure of the electro-thermal modelled system.
$P_{\text {loss }}$ is calculated and the junction temperature can be estimated as follows:
$T_{j}=R_{t h} P_{l o s s}+T_{a m b}$
where: $P_{\text {loss }}=P_{\text {cond }}+P_{S W}$,
$R_{t h}\left(=R_{t h-j c}+R_{t h-C A}\right)$ is the total thermal resistance from the junction to case, $R_{t h-j c}$ and the thermal resistance from case to ambient, $R_{t h-C A}$.

Table 5.1 summarises the thermal design parameters. The maximum power dissipated $\left(P_{D M A X}\right)$ of the semiconductors is calculated by rearranging (5.5) as follows:
$P_{D M A X}=\frac{T_{j M A X}-T_{c}}{R_{t h}}$
where $T_{c}$ is the maximum case temperature in continuous operation.
Table 5.1: Thermal Parameters Design.

| DUT | $\mathrm{R}_{t h-j c}$ <br> $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ | $\mathrm{R}_{t h-c a}$ <br> $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ | $\mathrm{T}_{j M A X}$ <br> $\left({ }^{\circ} \mathrm{C}\right)$ | $\mathrm{T}_{c}$ <br> $\left({ }^{\circ} \mathrm{C}\right)$ | $\mathrm{P}_{D M A X}$ <br> W |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C 2 M | 0.6 | 0.2 | 150 | 70 | 100 |
| SCH | 0.44 | 0.2 | 175 | 80 | 148 |
| SCT | 0.44 | 0.2 | 175 | 80 | 148 |

To ensure safe and reliable design, a safety margin $(\lambda)$ of $20 \%$ is assumed. The safety margin includes the effect of the other unmentioned thermal resistances such as the resistance between the heatsink
and liquid (water). Therefore, the relationship between the allowable $f_{s w}$ and the total semiconductor losses should satisfy the following constraint:
$E_{s w} f_{s w}+P_{\text {cond }} \leqslant(1-\lambda) P_{D M A X}$

Rewriting (5.7), the maximum allowable switching frequency $\left(f_{s w-M A X}\right)$ can be estimated as follows:
$f_{s w-M A X}=\frac{P_{D M A X}(1-\lambda)-P_{\text {cond }}}{E_{s w}}$

Accordingly, the relationship between the switching frequency and the achievable output power can easily be calculated. Including the safety margin $(\lambda=20 \%)$, Figure 5.3 depicts the frequency limit operation area of a hard switching application, with an input voltage of 600 V and a controllable duty cycle of 0.67 .


Figure 5.3: Frequency limits of the buck converter operated with $V_{\text {in }}=600 \mathrm{~V}$ and $V_{\text {out }}=400 \mathrm{~V}$.

The SiC devices can operate at a considerably high switching frequency, such as $>1 \mathrm{MHz}$ at 1 kW . On the other hand, in high power operation the switching frequency must be reduced to ensure the thermal limit. Nevertheless, the operating frequency remains high, such as $>100 \mathrm{kHz}$ at 10 kW . Based on these results, a hard- and a soft-switching converter are designed. The devices are first characterised in continuous operation at a very high switching frequency of 1 MHz . To validate the proposed electro-thermal model at a high power, the maximum achievable switching frequency is applied to 10 kW DC/DC converter and experimentally evaluated.

### 5.3 Operation of SiC MOSFETs at 1 MHz for Hard- and Soft-Switching Converters

### 5.3.1 Hard Switching

In the following, the design and operation of a 1 MHz converter is presented. Figure 5.4 shows the schematic circuit of the hard switching buck converter. A SiC Schottky diode (C4D10120) is used as the FWD. Realising fast switching times, a high frequency resonance between the parasitic capacitance of the buck inductor and the stray inductance in the switching power loop will exist. In order to reduce this ringing, a single layer winding inductor is used. The key parameters of the design are given in Table 5.2. A loss prediction based on the DPT results applying 1 MHz switching frequency, a 600 V input voltage, and a 5 A load current ( $D_{\text {cycle }}=50 \%$ ) yields switching losses of $94 \mathrm{~W}, 140 \mathrm{~W}$, and 135 W for C2M, SCH, and SCT devices, respectively. Assuming the thermal properties given in Table 5.1, the SiC MOSFETs operating in hard switching mode are expected to reach the maximum switching frequency of 1 MHz at 1.4 kW without further modifications.


Table 5.2: Key parameters of the buck converter.

| Items | Parameters |
| :---: | :---: |
| Input Voltage $\left(V_{\text {in }}\right)$ | $(400-600) \mathrm{V}$ |
| Output Voltage $\left(V_{\text {out }}\right)$ | $(200-300) \mathrm{V}$ |
| Output power $\left(P_{\text {out }}\right)$ | $(600-1400) \mathrm{W}$ |

Switching Frequency $\left(f_{s w}\right) \quad 1 \mathrm{MHz}$
Figure 5.4: Schematic circuit of hard switching buck converter.

Figure 5.5-a shows the measured switching waveforms for continuous operation of the C2M device at 1 MHz switching frequency, where $V_{\text {in }}=600 \mathrm{~V}$, $V_{\text {out }}=300 \mathrm{~V}$, and $P_{o}=1.4 \mathrm{~kW}$. The key parameters of the measured current and voltage waveforms are compared in Table 5.3. The results show that the switching loss dominates the total converter losses. Due to the fast switching, C2M gives a higher efficiency. To evaluate the overall converter efficiency, the losses in the passive components are calculated based on the equivalent series resistance (ESR) at 1 MHz of the capacitor ( $r_{c r} \approx 0.22 \Omega$ ) and inductor $\left(r_{L} \approx 2.38 \Omega\right)$. The gate driver loss $\left(P_{\text {gate }}\right)$ is also considered; $P_{\text {gate }}\left(P_{\text {gate }}=Q_{g} . V_{g s} . f_{s w}\right)$ depends on the total gate charge $\left(Q_{g}\right)$ of the transistor, switching frequency $\left(f_{s w}\right)$ and driving voltage


Figure 5.5: (a) Main waveforms of the converter running at $600 \mathrm{~V}, 1.4 \mathrm{~kW}$ and (b) Efficiency vs. output power.
$\left(V_{g s}\right)$. Table 5.4 summarises the losses in the hard switching converter operating at 1.4 kW and 1 MHz , while Figure 5.5-b depicts the measured efficiency of the converter at different output power levels.

Table 5.3: Key switching parameters extracted from continuous operation at $1.4 \mathrm{~kW}, 1 \mathrm{MHz}$.

|  | Turn-on |  |  |  | Turn-off |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :---: |
|  | C2M | SCH | SCT | C2M | SCH | SCT |  |
| Rising Time (ns) ${ }^{1}$ | 5 | 20 | 16 | 26 | 39 | 33 |  |
| Falling Time (ns) | 16 | 32 | 24 | 31 | 35 | 33 |  |
| Energy Loss $(\mu \mathrm{J})$ | 61 | 111 | 101 | 28 | 32 | 29 |  |

### 5.3.2 Soft Switching

Soft-switching techniques such as zero-voltage switching (ZVS) reduce the switching losses during high frequency-operation. In this analysis, the half bridge CLL resonant inverter shown in Figure 5.6-a is used. According to the design rules given in [86], the resonant capacitor is selected to 7 nF and the series and the parallel inductor values are $3.5 \mu \mathrm{H}$ and $12 \mu \mathrm{H}$, respectively. The converter is successfully tested at $1 \mathrm{MHz}, 1.7 \mathrm{~kW}$ and 600 V input voltage, $\left(D_{\text {cycle }}=50 \%\right)$, with ZVS operation. The key waveforms of the lower side switch employing the SCH device are shown in 5.6-b. It can be observed that the device turns on at zero voltage, which leads to reduced switching loss and noise. Furthermore, the converter is simulated by LTSpice-IV, using the device model delivered

[^0]Table 5.4: Measured and calculated losses in the hard switching converter at $\approx 1.45 \mathrm{~kW}$ and 1 MHz .

|  | C2M | SCH | SCT |
| :--- | :--- | :--- | :--- |
| $\mathrm{P}_{\text {cond }}(\mathrm{W})$ | 0.9 | 1.2 | 0.55 |
| $\mathrm{P}_{\text {sw }}(\mathrm{W})$ | 89 | 143 | 130 |
| $\mathrm{P}_{\text {gate }}(\mathrm{W})$ | 1.2 | 2.4 | 2.1 |
| $\mathrm{P}_{\text {passive }}(\mathrm{W})$ | 41 | 41 | 41 |
| Converter total Loss $(\mathrm{W})$ | 132 | 188 | 174 |
| $\eta(\%)$ | 91 | 87 | 88 |


(a)

(b)

Figure 5.6: (a) Schematic circuit of CLL converter and (b) main waveforms of the converter running at $600 \mathrm{~V}, 1.7 \mathrm{~kW}$.
by the manufacturer. The key parameters of the test and the simulation are extracted for different input voltages and listed in Table 5.5. The results from the experimental test and simulation exhibit close agreement regarding the switching losses. Figure 5.7 shows the converter's overall efficiency operating at different output power levels. Compared to the hard switching mode, ZVS for example applying C2M device reduces the power losses by $66 \%$ and increases the efficiency from $91 \%$ to $\approx$ $94 \%$ at 1.4 kW . When applying ZVS, the SiC devices exhibit a reduction in losses of approximately

Table 5.5: Key switching parameters for soft switching mode for one MOSFET, ( $E_{\text {on }} \approx 0$.)

|  |  |  | $\mathrm{E}_{\text {off }}(\mu \mathrm{J})$ |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {in }}$ <br> $(\mathrm{V})$ | $\mathrm{I}_{o-r m s}$ | $\mathrm{P}_{\text {out }}$ | (A) | $(\mathrm{W})$ | C 2 M |  | SCH |  |  |
|  |  |  | Exp. | Sim. | Exp. | Sim. | Exp. | Sim. |  |
| 300 | 2.9 | 400 | 7 | 7.5 | 15 | 13 | 12 | 13 |  |
| 400 | 4.0 | 750 | 12 | 13 | 24 | 21 | 17 | 19 |  |
| 500 | 5.1 | 1220 | 19 | 18 | 36 | 32 | 32 | 33 |  |
| 600 | 6 | 1700 | 32 | 28 | 51 | 45 | 44 | 39 |  |

two times, compared to hard switching. The advantages of using the SiC MOSFETs in soft-switching operation at this high frequency are visible.


Figure 5.7: Efficiency versus output power at 1 MHz for the CLL converter.

### 5.4 Operation of SiC MOSFETs in a 10 kW DC/DC Converter

In this section, the SiC MOSFETs are operated in a continuous mode in a $10 \mathrm{~kW} / 100-250 \mathrm{kHz}$ buck converter, comparing the synchronous rectification (SR), the use of the internal diode and the use of an external Schottky diode [87]. The filter inductor ( $L$ ), see Figure 5.4, is designed with the ferrite material N87, based on a double E80 core. The converter specifications used in the test are summarised in Table 5.6.

Table 5.6: Converter Specifications.

| $\mathrm{P}_{o}$ | $(1-10) \mathrm{kW}$ |
| :--- | :--- |
| $\mathrm{V}_{\text {in }}$ | 600 V |
| $\mathrm{~V}_{\text {out }}$ | 400 V |
| $\mathrm{f}_{\text {sw }}$ | $(100-250) \mathrm{kHz}$ |
| Duty Cycle | 0.67 |
| Dead-time | 100 ns |
| Inductance | $300 \mu \mathrm{H}$ |
|  | $\mathrm{N} 87 / 2 \mathrm{xEE} 80$ core |

According to the frequency limitation (see Figure 5.3), first, single chip devices C2M and SCT are operated up to $8 \mathrm{~kW}, 100 \mathrm{kHz}$ under the following conditions:

1) Synchronous rectification $(\mathrm{SR})$ mode
2) Using the body-diode ( BD ) in freewheeling loop
3) Using SBD as freewheeling diode.

### 5.4.1 Power Loss Measurement

In the experimental setup, input and output power are measured with a precision power analyzer LMG670. A water cooling system is used to cool the devices and measure the power loss generated by SiC MOSFETs and diodes, based on the calorimetric principle, allowing to separate semiconductor and inductor losses. To extract the winding losses of the inductor, the rms value of the current and the AC resistance ( $R_{L, A C}$ ) of the inductor are measured. $R_{L, A C}$ is derived as a function of the frequency using a precision LCR meter ST2827C. The conduction losses of the MOSFETs are estimated with help of the measured temperature dependency of $R_{D S o n}$.

### 5.4.2 Experimental Results of Single Chip Operation

Figure 5.8 illustrates the measured efficiency for conditions 1, 2, and 3. In SR mode, with dead-time $\left(T_{D}\right)$ of 100 ns , both body-diodes incur less than 2 W in power loss at 8 kW output power, and an efficiency comparable to the case of an external SBD is achieved.


Figure 5.8: Measured efficiency with single chip at 100 kHz using SR, BD and SBD conditions.

Using the body-diode instead of operating the MOSFETs in SR results in less efficiency with increasing output power. This is due to the relatively high forward voltage of the diode, see Figures 2.7 and 2.8. The effect is more pronounced for the planar device (C2M device). Furthermore, using the planar SiC MOSFETs' body-diode shows less efficiency compared to the double trench' intrinsic diode. As explained in Section 3.4, this mainly due to the fact that the turn-on transition of the planar
device is highly sensitive to the temperature, and therefore a significant increase in turn-on loss is expected at high power.

### 5.4.3 10 kW DC/DC Converter Operation

Since the current rating of the devices is not the same, parallel connection of the C2M MOSFETs is necessary to achieve the required power level of 10 kW . Therefore, the paralleling of SiC MOSFETs is investigated before comparing the devices in the continuous converter operation of 10 kW .

## Parallel Operation in 10 kW DC/DC Converter

The fast switching speed makes parallel operation of SiC MOSFETs more sensitive to parasitic circuit parameters. Unequal current sharing may cause an unequal loss distribution and exceed the SOA. The influence of device mismatch on the parallel operation is first investigated in a standard DPT and then validated in a continuous SR mode. Table 5.7 summarises the properties of six C2M device samples, which were tested to evaluate their on-state resistance and threshold voltage.

Table 5.7: C2M0080120D Characteristics.

|  | SiC-1 | SiC-2 | SiC-3 | SiC-4 | SiC-5 | SiC-6 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {DSon }}(\mathrm{m} \Omega)$ | $78 / 128$ | $87.5 / 142$ | $90 / 153$ | $79.5 / 131$ | $88 / 145$ | $89 / 147$ |
| $25^{\circ} \mathrm{C} / 150{ }^{\circ} \mathrm{C}$ | $78 / 128$ | 8.75 |  |  |  |  |
| $\mathrm{~V}_{\text {th }}(\mathrm{V})$ | 2.72 | 3.44 | 2.73 | 2.25 | 3.05 | 2.77 |
| $\mathrm{R}_{D \text { Son }}$ Mismatch | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ |
| $\mathrm{V}_{\text {th }}$ Mismatch |  |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ |
| Small Mismatch |  |  | $\checkmark$ |  |  |  |

Figure 5.9 depicts the transient current sharing between SiC-3 and SiC-6 samples for a load current $I_{o}$ $=40 \mathrm{~A}$. The devices have similar characteristics, and the measured currents during turn-on and turnoff are approximately identical. A good PCB design leads to reduced circuit mismatches (parasitic inductance in power and gate loops), thus ensuring that a good transient current sharing in parallel connection is achieved.

The influence of extremely different case temperatures is shown in Figure 5.10. The NTC behaviour that results in a higher on-state resistance and therefore a lower steady-state current at higher $T_{c}$ is clear, generally enabling stable parallel operation of SiC MOSFETs. The switching losses during the turn-on and turn-off process are calculated as a function of $T_{c}$ and summarised in Figure 5.11. During


Figure 5.9: (a) Turn-on and (b) turn-off current sharing of SiC-3 and SiC-6. [Time Scale: $50 \mathrm{~ns} / \mathrm{div}$ ].
the turn-off process, the switching energy mismatch increases with the temperature mismatch and reaches around $10 \%$ for a temperature mismatch of $75^{\circ} \mathrm{C}$. The main cause of this is the different turn-off currents, as can be seen in Figure 5.11-b. The influence of a $V_{t h}$ mismatch on transient current


Figure 5.10: (a) Turn-on and (b) turn-off current sharing of SiC-3 and SiC-6 at $I_{o}=40 \mathrm{~A}$ and different $T_{c}$. [Time Scale: $100 \mathrm{~ns} / \mathrm{div}$ ].
sharing is investigated, as is shown in Figure 5.12. Sample SiC-6 with a lower $V_{t h}$ turns-on slightly faster than sample SiC-5 and therefore conducts more current during the turn-on transition. The opposite is true of the turn-off process, where SiC-6 will later turn off the current and consequently incurs a higher turn-off loss. As depicted in the 5.12-b, before turn-off, both devices have the same current, which means, the $V_{t h}$ mismatch does not substantially influence the steady-state current sharing. The measured results show that the parallel devices reach their steady-state current after around 500 ns from turning on the device and that depends on the threshold voltage mismatch value. Further, the influence of extremely different external gate resistances ( $R_{\text {gext }}$ ) on current sharing is shown in Figure 5.13. During the turn-on dynamic process, the device that is controlled with a lower

(a)

(b)

Figure 5.11: (a) Turn-on and (b) turn-off energy loss of SiC-3 and SiC-6 at $I_{o}=40 \mathrm{~A}$ and different $T_{c}$.


Figure 5.12: (a) Turn-on and (b) turn-off current sharing of SiC-5 and SiC-6 with different $V_{t h}$. [Time Scale: $50 \mathrm{~ns} / \mathrm{div}]$.
$R_{\text {gext }}$ switches faster and conducts a higher amount of the load current. In contrast, the device with the high gate resistance $R_{\text {gext }}$ shares the bulk of the drain current during the turn-off process. The resulting switching losses are calculated as a function of $R_{\text {gext }}$ and summarised in Figure 5.14. To be more realistic, a $20 \%$ variation in the switching rate is introduced (SiC-3 is switched with $R_{\text {gext }}=6 \Omega$ and SiC-6 with $R_{\text {gext }}=5 \Omega$ ). Compared to the matching case $\left(E_{\text {Match }}=430 \mu \mathrm{~J}\right)$, the maximum change achieved by switching energies of SiC-3 and SiC-6 are $6 \%\left(E_{3 M i s m}=455 \mu \mathrm{~J}\right)$, and $4 \%$. $\left(E_{6 M i s m}=445\right.$ $\mu \mathrm{J})$, respectively. Therefore, with little difference in the switching rate, the DUTs exhibit relatively reasonable variations in switching energy. Since different $R_{\text {gext }}$ represent a model for unsymmetrical gate drive conditions, the gate loops have to be designed with equal loop lengths in order to minimise the mismatch.


Figure 5.13: (a) Turn-on and (b) turn-off current sharing of SiC-3 and SiC-6 at extremely different external $R_{\text {gest }}$. [Time Scale: $100 \mathrm{~ns} / \mathrm{div}$ ].


Figure 5.14: (a) Turn-on and (b) turn-off energy loss of SiC-3 and SiC-6 at different $R_{\text {gest }}$.

Finally, the influence of on-state resistance on current sharing is investigated. SiC-1 and SiC-3, which have nearly the same $V_{t h}$ and differ in their $R_{D S o n}$, have been selected for this case. As is shown in Figure 5.15, the $R_{D S o n}$ affects the steady state current sharing but has no visible effect on the transient characteristic. The increase of $R_{D S o n}$ with temperature balances the current sharing during continuous parallel operation, thus avoiding a thermal runaway condition.

Generally, the measurement results show that for a realistic device mismatch paralleling of SiC devices is feasible and can be used in the test of 10 kW converter. However, a non-symmetrical layout may lead to relatively high current peaks in the faster switching transistor.


Figure 5.15: (a) Turn-on and (b) turn-off current sharing of SiC-1 and SiC-3 at $I_{o}=40 \mathrm{~A}$ and different $R_{\text {DSon }}$. [Time Scale: $50 \mathrm{~ns} / \mathrm{div}$ ].

## Continuous 10 kW DC/DC Converter Operation

The switching frequency limit of the converter is recalculated using two chips in parallel. As is depicted in Figure 5.16, the use of two parallel C2M chips increases the frequency limit to 260 kHz at 10 kW . Figure 5.17 further details the measured results for parallel C2M devices in SR mode at different switching frequencies. A high efficiency of $98.9 \%$ can be achieved at 100 kHz hard switching.


Figure 5.16: Frequency limits of the parallel operation devices in a buck converter with $V_{\text {in }}=600 \mathrm{~V}$ and $V_{\text {out }}=400 \mathrm{~V}$.

The previous analysis has shown that current sharing between parallel SiC MOSFETS is dependent on device and circuit parameters, as well as the temperature. A mismatch leads to a non-uniform current distribution and may also lead to a thermal imbalance. In a high frequency operation the on-state time might not be sufficient to balance temperature and losses, leading to an increased possibility of thermal runaway. Therefore, to ensure the SOA of the devices in continuous operation, the influence of the


Figure 5.17: Measured efficiency with parallel C2M using SR mode.
temperature must be considered. The procedure set out in the flowchart in Figure 5.18 is proposed for use in estimating the junction temperature. The model uses the steady state calorimetric reading and some initial parameters to derive the dissipated power for each device. Initial parameters, such as thermal resistance $R_{t h}$ and $f_{s w}$ are fixed, while $T_{c}$ and $I_{r m s}$ are updated at each operating point. $5 \%$ is set as a maximum acceptable error between the calorimetric measured ( $P_{\text {calorimetric }}$ ) and analytical calculation $\left(P_{\text {loss }}\right)$ results.
$-5 \% P_{\text {calorimetric }}<|\Delta P|<5 \% P_{\text {calorimetric }}$
where $\Delta P=P_{\text {calorimetric }}-P_{\text {loss }}$
$P_{\text {loss }}$ contains the total analytically calculated switching and conduction losses of the parallel semiconductors. The individual loss distribution for 8 kW output power and a switching frequency of 100 kHz is given in Figure 5.19 . Both the improved body-diode and the reduction of the $R_{D S o n}$ in the trench SiC MOSFET lead to a higher efficiency which is comparable to the paralleled C 2 M configuration. On the other hand, because of the fast switching compared to the SCT, the C2M device generates lower switching losses. A direct comparison of the devices is difficult because of their different chip sizes.

In order to compare the losses for the same current density, the chip size of the C 2 M is scaled to the SCT data (device $\mathrm{C} 2 \mathrm{M}^{*}$ ). A linear scaling law is applied.
$I_{c 2 m}^{*}=I_{S C T} \frac{\text { Die size of } C 2 M}{\text { Die size of } S C T}$


Figure 5.18: Procedure of junction temperature estimation.


Figure 5.19: Loss breakdown at a) 8 kW with SCT, b) 8 kW with single C2M and c) 6.3 kW with C2M* (scaled). (LS-Cond = Low Side Conduction Loss, HS-Cond = High Side Conduction Loss, HS-SW = High Side Switching Loss).

Figures 5.19-c and 5.19-a compare one scaled C2M* device at 6.3 kW (15.75A) with the SCT device at 8 kW (20A). Using the SR mode, the scaled planar device exhibits $20 \%$ reduction in the total (74 W) loss compared to the trench device ( 93 W ).

With the loss data, the semiconductors' junction temperatures $T_{j}$ are estimated. The results are summarised in Figure 5.20. As expected, the highest $T_{j}$ occurs in the configuration that uses a body-diode in the FWL, as well as only a single C2M-chip. For 8 kW output power, $T_{j}=144{ }^{\circ} \mathrm{C}$ is recorded. A comparable $T_{j}$, especially at high power ( $P_{o}>5 \mathrm{~kW}$ ), is achieved when applying SR or an external SBD. This is due to the high temperature dependency of the SBD forward voltage at the high current. In contrast, the single trench device becomes less heated: $T_{j}$ of $155{ }^{\circ} \mathrm{C}$ is achieved at 10 kW , which is $88 \%$ of its maximum junction temperature $\left(T_{j M A X}=175^{\circ} \mathrm{C}\right.$ ). The parallel connection of C2M devices allows for an increase in either the power level or the switching frequency. At 100 kHz , the maximum $T_{j}$ of the parallel C2M transistors is $70 \%$ of the maximum temperature ( $T_{j M A X, C 2 M}$ $=150^{\circ} \mathrm{C}$ ) and is reduced by $32 \%$ compared to the single trench device $\left(T_{j M A C, S C T}=155^{\circ} \mathrm{C}\right)$. This allows for further increases in the switching frequency and stay within the SOA up to 250 kHz at 10 kW .


Figure 5.20: Estimated curves of $T_{J}$ of single and parallel connection.

In summary, the SiC MOSFETs are successfully operated in a continuous mode in a $10 \mathrm{~kW} /(100-250)$ kHz buck converter comparing SR, the use of the internal diode and the use of an external Schottky diode. The loss analysis also shows that operation in SR eliminates the need for an external SBD. Further, parallel operation of the considered planar MOSFET (C2M) devices is needed to achieve 10 kW output power at 100 kHz hard switching. The impact of parameter mismatch on the static and dynamic current sharing of the devices is evaluated, showing that paralleling of SiC devices is feasible and allows to increase power or switching frequency of the test converter.

## Chapter 6

## Short-Circuit Robustness of SiC

## MOSFETs

### 6.1 Introduction

THE potential of the SiC MOSFETs is remarkable. SiC devices offer a number of advantages over Si , such as higher breakdown voltage, higher operating temperature, and lower switching and conduction losses. With these features, a higher power density is expected. Thus, guaranteeing reliability becomes more challenging. However, reliability issues associated with SiC MOSFETs is an important topic that must be considered for the application. Due to a smaller chip area and higher current density, SiC MOSFETs tend to have a lower short circuit time compared to Si devices [88]. Therefore, the short circuit capability and reliability of SiC MOSFETs remain worthy of discussion. In this chapter, an experimental study focusing on different failure modes, due to short-circuiting, on planar and trench SiC devices is presented and compared. The robustness of the planar devices under short-circuit conditions has been investigated, and a set of relevant conclusions have been published [21, 89-94]. However, to the best knowledge of the author, this is the first study to investigate and compare different failure modes in the double-trench (SCT) device and the planar-technology ( C 2 M and SCH ) devices. Additionally, the temperature-dependence of the short-circuit capability is evaluated, and the associated failure modes are presented. The effects of different biasing voltages, DC link voltages, and case temperature are analysed. Further, several SC tests are performed in order to estimate the short circuit critical energy which leads to device failure.

[^1]The second part of this work covers the design and testing of two different methods for overcurrent protection. The desaturation technique is applied to the SiC MOSFETs and compared to a second method that depends on the stray inductance of the devices.

### 6.2 Short-Circuit Behaviour of SiC Power MOSFETs

The short circuit behaviour of SiC MOSFETs is experimentally investigated using the test circuit shown in Figure 6.1. First, the DUT is biased in off-state until the capacitor $C_{i n}(120 \mu \mathrm{~F})$ is charged up to the desired input voltage $\left(V_{i n}\right)$. Subsequently, a single pulse with variable duration is used to turn-on the device. The short circuit current rise is limited by the device characteristics and the parasitic inductance that exists in the power circuit. The circuit parasitic inductance is calculated to approximately 60 nH based on experimental results, including the DUT.


Figure 6.1: Schematic of short-circuit test setup.

The devices are simulated in LTspice-IV using the thermal model delivered by the manufacturer. For example, Figure 6.2 shows a simulation of the SC current and the corresponding simulated junction temperature $T_{j}$ for C 2 M device at a gate-source voltage $V_{g s}=20 \mathrm{~V} /-5 \mathrm{~V}$, short circuit time $T_{S C}=$ $5 \mu$ s and case temperature $T_{c}=25^{\circ} \mathrm{C}$. The SC behaviour can be divided into three modes. Mode M-1 starts at the beginning of the SC pulse. Generally, the short circuit current rise depends on the stray inductance ( $L_{\text {stray }}$ ) in the circuit, and on the transistor and gate driver parameters, including the transfer characteristics (threshold voltage and forward transconductance), gate resistance, and applied gate-source voltage. Since the current in Figure 6.2 continues to increase after the gate is fully biased $\left(V_{g s}=20 \mathrm{~V}\right)$, the stray inductance and thermal effects need to be considered in order to describe the short circuit current characteristics. This conclusion is sustained by the experimental and simulation


Figure 6.2: SC simulation of C2M device at $V_{d s}=600 \mathrm{~V}$ and $R_{\text {gext }}=12 \Omega$.
results given in Figure 6.3-a: it is clear that a change in the external gate resistance (e.g. $R_{\text {gext }}=12$ $\Omega$ to $R_{\text {gext }}=90 \Omega$ ) has only a marginal impact on the peak short circuit current. The gate resistance determines the time constant $\left(R_{G} C_{e q}\right)$ at which the gate is charged, and it thus influences the $\mathrm{di} / \mathrm{dt}$ during the charging process.

The further current rise is dominated by the time constant of the large on-state resistance (close to a current source) in the saturation range and the stray inductance. To visualise the impact of $L_{\text {stray }}$, a large total inductance of 200 nH is realised in the power loop. In this case, the simulation and experimental results of the SC current (Figure 6.3-b) show a larger time constant and a reduced peak SC current than the original circuit with 60 nH inductance. Since the power losses during the short circuit and hence the junction temperatures are different in both cases, the point of time at which the current starts to decrease is also different.

Furthermore, analysing the short circuit current using different DC-link voltages provides further insight into the thermal characteristics of the different SiC MOSFETs. Figure 6.4 shows the impact of the drain-source voltage on the SC current for the DUTs at $R_{\text {gext }}=12 \Omega, T_{S C}=5 \mu$ s and $T_{c}=25^{\circ} \mathrm{C}$. Figure 6.5 depicts a simulation of the SC current compared to the measurement and the corresponding simulated junction temperature for the C2M device. Different rising slopes and peak currents are obtained by varying $V_{d s}$. Apart from differences in the output characteristics and due to the fact that the MOSFET is not an ideal current source, this can be explained by internal thermal effects. As stated above, power losses will lead to self-heating and rising junction temperatures, which are therefore


Figure 6.3: The simulation (dashed) and experimental (solid) SC current with a) different gate resistance and b) different parasitic inductance at $V_{d s}=300 \mathrm{~V}, T_{c}=25^{\circ} \mathrm{C}$ and $V_{g s}=20 \mathrm{~V} /-5 \mathrm{~V}$.


Figure 6.4: Experimental results of SC with $T_{S C}=5 \mu \mathrm{~s}, T_{c}=25^{\circ} \mathrm{C}$ and different dc link voltages for a) $\mathrm{C} 2 \mathrm{M}\left(V_{g s}=20 \mathrm{~V}\right)$, b) $\mathrm{SCH}\left(V_{g s}=20 \mathrm{~V}\right)$ and c) $\operatorname{SCT}\left(V_{g s}=18 \mathrm{~V}\right)$.
directly related to the voltage. At the end of mode M-1 (for definition, see Figure 6.2), the maximum short circuit current ( $I_{S C M A X}$ ) reaches approximately six times the rated value for C2M device and seven times for ROHM devices at $V_{d s}=600 \mathrm{~V}$ and full biasing voltage.

In mode M-2, as is shown in Figure 6.2, the junction temperature further increases because of the


Figure 6.5: Simulation (dashed) of the SC current compared to the measurement (Solid) and the corresponding simulated $T_{J}$ for C2M device.
self-heating, thus the on-state resistance dramatically increases (see Section 2.3). As stated above, the SC current gradually decreases with time. Because of the higher junction temperature and its rate of change, the SC current at $V_{d s}=600 \mathrm{~V}$ decreases faster than for the other levels.

Furthermore, the effect of using different biasing voltage on the SC current is evaluated. The experimental results in Figure 6.6 show that using a higher biasing voltage increases the peak SC current due to the transistor characteristic, and it also achieves a faster recovery to mode M-2. Apart from their output characteristics, DUTs further differ in their chip size and thermal capacitance and in the temperature dependency of the transfer characteristics, leading to the different short circuit current waveforms.

Finally, the impact of the temperature on the SC current is explicitly evaluated for $25^{\circ} \mathrm{C}$ and $150^{\circ} \mathrm{C}$ case temperatures. Figure 6.7 shows the results for the C2M-device. Using full biasing voltage ( $V_{g s}$ $=20 \mathrm{~V}$ ), as previously stated, the JFET and drift region dominate the on-state characteristic. Thus, the total on-resistance increases with temperature and thus decreasing the SC current level [95, 96]. On the other hand, when applying a low biasing voltage, the SC current level shows an increase with temperature. This is because the channel resistance, which has a NTC, is dominant. Since the device is operating with $V_{g s}<V_{g s-\min }$ (see Section 2.3), the SiC MOSFET is expected to work in the instability thermal area, see Figure 2.5. This effect is more pronounced in the SCH device and is depicted in Figure 6.8.


Figure 6.6: Experimental results of SC with $V_{d s}=300 \mathrm{~V}, T_{S C}=20 \mu \mathrm{~s}, T_{c}=25^{\circ} \mathrm{C}$ and different $V_{g s}$ for a) C2M, b) SCH and c) SCT.


Figure 6.7: Experimental SC waveform for $\mathrm{C} 2 \mathrm{M}-$ device with $V_{g s}=20 \mathrm{~V}$ and different $T_{c}$. and different voltage levels.


Figure 6.8: Experimental SC waveform for $\mathrm{SCH}-$ device with $V_{d s}=300 \mathrm{~V}, T_{S C}=15 \mu \mathrm{~s}, V_{g s}=15$ V and different $T_{c}$.

### 6.3 Failure Analysis during Mode-3

In mode M-3, two cases can occur. In the first case, the device successfully turns-off and no thermal runaway is observed after the turn-off process. This case is limited by the SC time period. In our exemplary measurements C 2 M and SCH devices could withstand SC conditions for $8 \mu \mathrm{~s}$ and $14 \mu \mathrm{~s}$,

Table 6.1: Comparison of the critical energy for DUTs at $V_{d s}=600 \mathrm{~V}$.

| DUT | $V_{g s}$ <br> $(\mathrm{~V})$ | Failure $T_{S C}$ <br> $(\mu \mathrm{~s})$ | Critical Energy <br> $(\mathrm{J})$ | Critical energy / Die Area <br> $\left(\mathrm{mJ} / \mathrm{mm}^{2}\right)$ | Failure $T_{S C}$ <br> $(\mu \mathrm{~s})$ | Critical Energy <br> $(\mathrm{J})$ | Critical energy / Die Area <br> $\left.(\mathrm{mJ} / \mathrm{mm})^{\circ}\right)$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $20 /-5$ | 9 | 0.73 | 70.2 | 8.1 | 0.69 | 66.3 |
| SCH-Planar | $20 /-5$ | 15 | 1.45 | 109.8 | 13.9 | 1.31 | 99.2 |
| SCT-Trench | $18 /-2$ | 8 | 1.38 | 104.5 | 6.8 | 1.24 | 93.9 |

respectively (at $V_{g s}=20 \mathrm{~V}, V_{d s}=600 \mathrm{~V}$ and $T_{c}=25^{\circ} \mathrm{C}$ ), while the trench device exhibited a $7 \mu \mathrm{~s} \mathrm{SC}$ withstand time (at $V_{g s}=18 \mathrm{~V}, V_{d s}=600 \mathrm{~V}$ and $T_{c}=25^{\circ} \mathrm{C}$ ).

The SC critical energy ( $E_{S C}$ ) for SiC MOSFETs is estimated by applying different SC durations and calculated based on:

$$
\begin{equation*}
\int_{t_{0}}^{T_{s c}} V_{d s} I_{d s} \cdot d t \tag{6.1}
\end{equation*}
$$

Table 6.1 compares the temperature-dependent SC withstand time and critical energy of the DUTs at the critical failure pulse and $V_{d s}=600 \mathrm{~V}, R_{\text {gext }}=12 \Omega$. For ROHM devices, the critical SC energy per die area indicates that the planar device might be more robust than the trench device. This may be due to the higher current density of the trench device, resulting in accelerated temperature increase and thus lower short-circuit capability.

The second case is a thermal failure that can occur after the device is turned off. Following a successful turn-off, a sudden short circuit between source and gate is observed after a few microseconds, as is shown in Figure 6.9. This means that the device becomes uncontrollable. The results also show an increase of the leakage tail current and a decrease in $V_{g s}$ during the SC test.


Figure 6.9: Different failure modes at $V_{d s}=600 \mathrm{~V}$ and $T_{c}=25^{\circ} \mathrm{C}$.

### 6.3.1 Thermal Runaway of Planar SiC Devices

In order to investigate the failure modes, the SC time was increased after a successful pulse, in gradations of 100 ns until the failure of the device. Figure 6.10 depicts the SC current of the C 2 M device at 600 V with different short circuit pulse-widths and $T_{c}=25^{\circ} \mathrm{C}$. A tail current is observed after turn-off that progressively increases with SC time. This current further increases the thermal stress. At the critical SC time $\left(T_{S C-c r t}=9 \mu s\right)$, a significant leakage current appears, resulting in internal thermal instability and eventually leading to device failure through a short between the gate and source terminals. As illustrated in Figure 6.10, following a successful turn-off and after a failure delay-time of $4 \mu$ s a sudden short circuit between source and gate is observed while the drain-source continues to block the DC input voltage. In addition, the leakage current in the gate-source is further increased with SC time, $\left(>0.15 \mathrm{~A}\right.$ at $\left.T_{S C}=9 \mu \mathrm{~s}\right)$ and results in a large voltage drop across the gate resistance and hence a reduction in the gate-source voltage. This is an indicator that the gate isolation has been damaged and thus that the gate-source voltage cannot reach its full bias [88]. The resistances between the defect device terminals have been measured and tabulated in Table 6.2, showing that the gate oxide is partly damaged while the drain-source appears normal.

Further, the device is tested at an elevated temperature. Figure 6.11 compares the SC failure for two different case temperatures. Different failure mechanisms are observed. As shown, due to the additional thermal stress, the failure SC time is reduced at higher temperature ( $\approx 8 \mu \mathrm{~s}$ ). After a delay-time of $2.4 \mu \mathrm{~s}$, a sudden short circuit between all terminals is observed (see Table 6.2), and the device is no longer able to block the DC input voltage. Unlike $T_{c}=25^{\circ} \mathrm{C}$, the results indicate that both gate oxide and SiC p-n junction are damaged, as the case temperature increased to $T_{c}=150{ }^{\circ} \mathrm{C}$, and the device is fully destroyed.

According to [91], this is due to the temperature dependency of the intrinsic carrier concentration within the depletion region. Because of the fast increase in the intrinsic carrier, a thermal current, which dominates the leakage current, is generated and progressively rises with temperature, thus adding more thermal stress. Therefore, increasing the case temperature will accelerate this process, which is experimentally sustained through the reduction observed in the SC withstand time. Thus, it is expected that the gate oxide and the $4 \mathrm{~h}-\mathrm{SiC}$ are reaching their critical temperatures. Besides this, such behaviour could occur at low case temperature when a long SC time is applied (such as $>9 \mu \mathrm{~s}$ ) as has been reported in [91, 94, 97].

Furthermore, the SC capability of the ROHM planar device (SCH) is evaluated at the same test


Figure 6.10: a) SC current of C2M device and b) enlarged waveforms with $V_{d s}=600 \mathrm{~V}, T_{c}=25^{\circ} \mathrm{C}$, $V_{g s}=20 \mathrm{~V}$ and different $T_{S C}$.

Table 6.2: Resistances measurement after failure cases.

| DUT | $R_{g s}(\Omega)$ | $R_{g d}(\Omega)$ | $R_{d s}(\Omega)$ | Failure |
| :--- | :---: | :---: | :---: | :---: |
| C2M at $25^{\circ} \mathrm{C}$ | 1.8 | $730 \mathrm{k} \Omega$ | $730 \mathrm{k} \Omega$ | Gate-shorted <br> Thermal runaway |
| C2M at $150^{\circ} \mathrm{C}$ | 1.1 | 0.58 | 0.58 | Destruction <br> Thermal runaway <br> Gate-shorted |
| SCH at $25^{\circ} \mathrm{C}$ | 0.85 | $\infty$ | $\infty$ | Thermal runaway <br> Destruction |
| SCT at $25^{\circ} \mathrm{C}$ | Open Terminals | Open Terminals | Open Terminals | Thermal runaway - drain leakage current |
| Destruction |  |  |  |  |



Figure 6.11: Different SC failure modes of C 2 M device at two different case temperatures and $V_{d s}=$ 600 V.
conditions and $T_{c}=25^{\circ} \mathrm{C}$ (see Figure 6.12). Similarly to the C 2 M device, a thermal runaway is observed. However, the failure delay-time is much longer, (10.2 $\mu \mathrm{s}$ ). Compared to C 2 M , less tail
current is measured, which could explain the long failure delay-time. In both devices (C2M and SCH ), the drain-source terminals still block the input voltage, indicating that the gate isolation is responsible for device failure. In this failure case, the degradation in the gate acts as self-protection for the power drain-source terminals in the real power application. This is the case, because the drain-source terminal is still blocking the input voltage and therefore, no SC current flows through the SiC device.


Figure 6.12: a) SC current of SCH device and b) enlarged waveforms with $V_{d s}=600 \mathrm{~V}, T_{c}=25^{\circ} \mathrm{C}$, $V_{g s}=20 \mathrm{~V}$ and different $T_{S C}$.

### 6.3.2 Thermal Runaway of Double-Trench SiC devices

The short circuit capability of the double-trench SiC MOSFET is evaluated under several conditions. Figure 6.13 presents the short-circuit measurements of the trench device at $600 \mathrm{~V}, T_{C}=25^{\circ} \mathrm{C}$, and a positive gate voltage of 18 V . The short-circuit duration is gradually increased, in steps of 100 ns until the failure takes place.

Compared to planar devices, several observations can be made:

- The maximum SC current of trench devices is almost twice that of the planar transistors, and as a consequence, a faster junction temperature rise is expected.
- For the same DC input voltage, and although they have the same die area, the trench device exhibits a smaller SC withstand time, $8 \mu \mathrm{~s}$, than the SCH device, $14 \mu \mathrm{~s}$. It is noted that the trench device has a higher current density. Therefore, the short circuit current density determines a higher junction temperature, meaning that a lower withstand time is expected.
- At the critical SC time $\left(T_{S C-c r t}=8 \mu s\right)$, a high continuous drain leakage current is observed ( $>10 \mathrm{~A}$ ), resulting in additional thermal stress. Due to the expected extremely high junction temperature, references [91, 94, 98], explain the continuous drain-source leakage current by the latch-up of the parasitic bipolar junction transistor. Thus, the remaining drain leakage current is high enough to be responsible for a thermal runaway. Nevertheless, the failure delay-time is almost similar to the SCH planar device ( $\approx 10 \mu \mathrm{~s}$ ).
- More interestingly, unlike planar devices, no gate-shortening is observed in the case of a trench device, indicating a more robust gate structure. This is expected, since the double-trench structure suppresses the high electric field at the gate oxide of the gate trench, which in turn prevents the destruction of the oxide layer [37].


Figure 6.13: a) SC current of SCT-device and b) enlarged waveforms with $V_{d s}=600 \mathrm{~V}, T_{c}=25^{\circ} \mathrm{C}$, $V_{g s}=18 \mathrm{~V}$ and different $T_{S C}$.

On the other hand, the trench technology shows a different SC capability behaviour than planar devices at high temperature $\left(T_{c}=150^{\circ} \mathrm{C}\right)$. As displayed in Figure 6.14 , the device survives with $T_{S C}$ $\leq 6 \mu \mathrm{~s}$, and no degradation is observed. Further increasing the SC time to $7.2 \mu \mathrm{~s}$ leads the device to being partially damaged in the gate oxide, while the thermal breakdown of $4 \mathrm{H}-\mathrm{SiC}$ occurs after a failure delay-time of $\approx 6 \mu \mathrm{~s}$.

In summary, several observations can be made regarding the temperature-dependent SC capability of the trench SiC MOSFET, [the test conditions are: $V_{i n}=600 \mathrm{~V}, T_{c}=150^{\circ} \mathrm{C}, V_{g s}=18 /-2 \mathrm{~V}$ and $R_{\text {gext }}=$ $12 \Omega$ ]:

- No degradations are observed in either gate or drain with $T_{S C} \leq 6 \mu \mathrm{~s}$. The dissipated energy was calculated to 356 and 400 mJ for a SC time of 5 and $6 \mu \mathrm{~s}$, respectively.
- As the SC time increases ( $>6 \mu \mathrm{~s}$ ), a gate oxide degradation is observed, and a continuous gate leakage current is generated, resulting in a large voltage drop across the gate resistance and hence a reduction in the gate-source voltage. As depicted in Figure 6.14, the gate voltage decreases to 15 V at $T_{S C}=7.2 \mu$ s compared with 18 V at nominal operation. Consequently, the SC current level is reduced to the corresponding new gate voltage level.
- More interestingly, a higher gate-source voltage drop is measured than in the case of $T_{c}=25$ ${ }^{\circ} \mathrm{C}$, and no sudden short circuit between gate and source is detected, unlike in the case of planar devices. At the critical SC time, $T_{S C}=7.2 \mu \mathrm{~s}$, the device successfully turns-off, with the SC current corresponding to the new $V_{g s}$. After a delay time of $6 \mu \mathrm{~s}$, a thermal breakdown of the gate oxide and $4 \mathrm{H}-\mathrm{SiC}$ occurs. According to [94, 99], this behaviour is mainly due to the holes trapped in the gate oxide, which are associated with current density. Further increases in the traps result in additional electric fields being created in the channel. Thus, a leakage current path between the oxide and the channel is generated.


Figure 6.14: SC failure mode of trench-device at $T_{c}=150^{\circ} \mathrm{C}$.

Despite this, it can be concluded that the SiC MOSFETs have sufficient ruggedness and can withstand a high SC current at high DC-link voltages. As shown, the critical SC time is affected by increasing DC-link voltage, case temperature, and biasing voltage. In most failure cases, the gate leakage current is responsible for the device thermal runaway issue. However, both technologies exhibit a high short circuit capability, principally, sufficient to design a proper overcurrent protection.

### 6.4 Short Circuit Overcurrent Protection

A fast protection system turning-off a short circuit is needed in order to avoid self-heating of the chip which could potentially result in a destruction of the device. The most common short-circuit protection method is based on sensing the voltage drop $V_{d s}$ across the device. A SC condition can be detected because the expected voltage drop in failure mode is much higher than in normal operation. In [100], a solid state circuit breaker (SSCB) technique is applied to the old generation SiC MOSFET from CREE and compared to the desaturation method which relies on a blanking time delay in order to avoid false triggering. Reference [92] applies the desaturating method to a SiC JFET, using a logic gate with an integrated Schmitt trigger instead of the comparator to increase noise immunity.

In this work, two different overcurrent protection (OCP) circuits are designed and compared. First, the desaturation technique uses a feedback from the biasing voltage instead of the blanking time delay to avoid false triggering. The second method is based on sensing the current through the device. In [101], current sensing is achieved using a shunt resistor in series with the source pin. In this work, the current is monitored by the stray inductance at the source pin instead of the shunt resistor. The circuit diagram for the desaturation technique is shown in Figure 6.15-a. A soft turn-off stage is included to reduce the voltage overshoot caused by the total stray inductance. The biasing voltage is used as feedback to allow for charging of $C_{f}$ during the on-pulse and discharging through $D_{D i s c h}$ during the off-pulse. $R_{1}$ is used to add more damping to also avoid false triggering due to oscillations. With this method, no blanking time is needed. Hence, discharging during the turn-off process will allow $V_{C f}$ to fall below the reference value. When a short circuit occurs, the voltage across the $C_{f}\left(V_{C f}\right)$ increases and is compared to the reference voltage ( $V_{\text {ref }}$ ). This triggers the comparator in order to disable the gate driver IXDN609. Because -5 V negative biasing leads to a high di/dt, $Q_{1}$ is used to softly turn-off the DUT through discharging the gate-source capacitance with a larger resistance $\left(R_{\text {soft }}\right)$. A clamping circuit is included using a zener diode to protect the gate against overvoltages. The second OCP method depends on the voltage measured at the stray inductance of the device. Figure 6.15-b shows the block diagram of this circuit. The only difference between this method and the desaturation technique is in the voltage sensing. A low pass filter (RC-filter) is connected between the root and tips of the package power source lead. When a short circuit occurs, the voltage drop across the stray inductance $L_{\text {stray }}$ increases and can be detected through the RC-filter. The remaining procedure is as described for the desaturation method.


Figure 6.15: Block diagram of overcurrent protection methods: a) desaturation technique and b) stray inductance technique.

### 6.4.1 OCP- Experimental and Simulation Results

Both protection circuits are simulated using LTspice and experimentally tested. A fast comparator is used with 80 ns maximum propagation delay. Based on the measured output characteristics of the devices, 7 V is selected as reference voltage for the desaturation method, which corresponds to a current of 60 A . A hard switching fault (HSF) type is selected to investigate both methods. Figure 6.16 shows a comparison between simulation and experimental results of the stray inductance method under a hard turn-off, tested at $V_{d s}=600 \mathrm{~V}$. The stray inductance is calculated from the measurement,


Figure 6.16: Simulation (solid) and experimental (dashed) results of stray method.


Figure 6.17: Measurement RC-filter voltage vs. drain-source current.
where the voltage across $L_{s t r a y}$ and the turn-on $\mathrm{di}_{d s} / \mathrm{dt}$ are experimentally evaluated. Several tests are performed with different currents, and the stray is calculate to approximately 5 nH . The output voltage of the RC filter $\left(C_{f}=500 \mathrm{pF}\right.$ and $\left.R_{f}=200 \Omega\right)$ is measured at different current levels for the stray

Table 6.3: Comparison between OCP methods ( $R_{\text {gext }}=12 \Omega, V_{g s}=20 /-5 \mathrm{~V}$ and $R_{\text {soft }}=200 \Omega$ ).

| Turn-off Type |  | Desaturation Method |  |  |  | Stray Method |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $I_{\text {Limit }}$ <br> (A) | $t_{d 1}$ <br> (ns) | $\begin{aligned} & t_{d 2} \\ & (\mathrm{~ns}) \end{aligned}$ | $\mathrm{di}_{d s} / \mathrm{dt}$ <br> ( $\mathrm{A} / \mu \mathrm{s}$ ) | $I_{\text {Limit }}$ <br> (A) | $\begin{aligned} & t_{d 1} \\ & (\mathrm{~ns}) \end{aligned}$ | $\begin{aligned} & t_{d 2} \\ & (\mathrm{~ns}) \end{aligned}$ | $\mathrm{di}_{d s} / \mathrm{dt}$ <br> ( $\mathrm{A} / \mu \mathrm{s}$ ) |
| Hard SW | $V_{d s}=600 \mathrm{~V}$ | 120 | 150 | 280 | 740 | 100 | 80 | 180 | 800 |
|  | $V_{d s}=300 \mathrm{~V}$ | 118 | 145 | 270 | 755 | 96 | 70 | 150 | 960 |
| Soft SW | $V_{d s}=600 \mathrm{~V}$ | 135 | 200 | 440 | 433 | 110 | 90 | 350 | 338 |
|  | $V_{d s}=300 \mathrm{~V}$ | 130 | 185 | 410 | 462 | 105 | 85 | 345 | 323 |

inductance method. For high $\mathrm{di}_{d s} / \mathrm{dt}$ in SC tests, Figure 6.17 shows a nearly proportional relationship between the increasing current and output voltage of the RC filter. The experimental waveforms of $V_{g s}, V_{d s}, I_{d s}, V_{c f}, V_{c o m p}$ and the latch signal ( $V_{\text {Latch }}$ ) are reported in Figure 6.18, applying both methods to the C2M-device at $V_{d s}=600 \mathrm{~V}, R_{\text {gext }}=12 \Omega$ and $V_{g s}=20 \mathrm{~V} /-5 \mathrm{~V} .200 \Omega$ soft turn-off resistance $\left(R_{\text {soft }}\right)$ is used and compared to hard switching. The desaturation method can limit the SC current $\left(I_{\text {limit }}\right)$ in hard switching to 120 A within $t_{d 1}=150 \mathrm{~ns}$. The device fully turns-off within $t_{d 2}$ $=280 \mathrm{~ns}$ including the SC current falling time. During soft turn-off, the current is limited to 135 A within $t_{d 1}=200 \mathrm{~ns}$ and $t_{d 2}=440 \mathrm{~ns}$ to fully turn-off (including the falling time). Figure $6.18-\mathrm{b}$ shows the corresponding experimental soft and hard turn-off switching OCP waveforms applying the stray inductance method. 2.3 V is selected as voltage reference value. The same time delays for all ICs are assumed for both methods. The stray method has a faster detection time than the desaturation method. The larger delay in the desaturation method is mainly due to the junction capacitance of the $D_{\text {DESAT }}$ and its reverse recovery characteristics [92,100,101]. Both methods are compared in Table 6.3 for two different input voltages. They exhibit a fast response to the fault current and a high di/dt during the turn-off process. Since the parasitic inductance is relatively low in the power loop $(60 \mathrm{nH})$, the expected overshoot in $V_{d s}$ should be small. The calculation provides an overshoot of 45 V compared to $\approx 50 \mathrm{~V}$ in the experimental test at $V_{d s}=600 \mathrm{~V}$ for the desaturation hard turn-off. Compared to soft turn-off, the overshoot voltage is not extremely high. It can be concluded that the soft turn-off stage is not important to include in this type of fault compared to a fault under load [100]. In conclusion, the desaturation method shows a higher fault response time compared to the stray technique. Using the stray method, the maximum fault current is reduced by approximately $20 \%$. Two fast diodes are required for the desaturation technique. On the other hand, selecting the reference value in the desaturation method is easier than for the stray technique due to the low voltage drop at the source

(b)

Figure 6.18: Experimental results of a) desaturation OCP and b) stray inductance methods for hard (dashed) and soft (solid) turn-off at $V_{d s}=600 \mathrm{~V}, R_{\text {gext }}=12 \Omega$ and $V_{g s}=20 /-5 \mathrm{~V}$.
pin. Generally, the results show that both methods have the capability to detect the SC condition in the considered SiC MOSFETs within 150 ns and 80 ns , respectively, when applying hard turn-off.

## Chapter 7

## Efficiency Analysis of HF PS-ZVZCS Isolated Unidirectional Full-Bridge DC/DC Converter

### 7.1 Introduction

MEDIUM and high power DC-DC converters are of increasing interest in various applications including electromobility, renewable energy power conversion and power distribution in micro-grid systems [103-106]. Due to continuous improvements of power electronics devices and the ability to increase the switching frequency, power density is an important parameter. The adoption of the SiC MOSFETs in power converters promises to improve both the converter efficiency and power density.

The Phase-Shifted Full-Bridge (PS-FB) converter is a feasible and widely used solution for isolated DC/DC converters. The benefits of using SiC devices in PS-FB converter are rarely discussed [107]. Actually, the development of the power converter considering a high efficiency as the main target, has several degrees of freedom. A design optimisation procedure is necessary to obtain the optimal switching frequency and hence an optimal high-frequency magnetic component design. The magnetic components tend to be the bulkiest parts of the high-frequency (HF) power converter, and the magnetic e.g. of the high-frequency transformer (HFT) is considered one of the design limitations to achieve

[^2]a high-power density. High operating switching frequency contributes to volume/weight reduction, but the thermal limit, core, and winding losses of the magnetic components are negatively influenced [108].

In this chapter, a 10 kW PS-FB converter is designed, and the SiC devices are characterised in continuous operation at a high switching frequency of up to 250 kHz . With the help of the small parasitic output capacitance of the SiC devices, a zero-voltage zero-current switching (ZVZCS) topology is proposed using only the parasitic leakage inductance of the transformer. To minimise the rectifier diode voltage spikes, a current fed topology with capacitive output filter is used. Further, the loss calculation and optimisation of the design of different high-frequency transformers (HFT) are presented. Finally, the overall efficiency of the converter is evaluated and a practical method to break down the converter losses based on separating the measured semiconductor and magnetic losses is proposed and compared to an analytical loss model.

### 7.2 PS-ZVS Isolated Unidirectional Full-Bridge DC/DC Converter

The Phase-Shifted Full-Bridge (PS-FB) converter is a feasible and widely used solution for isolated DC/DC converters. Research on this topology often focusses on efficiency improvement and extension of the soft switching properties [109-113]. Practical solutions mainly through adding energy recovery clamp circuits and snubber circuits were proposed to clamp the voltage across the rectifier diodes [109, 114, 115]. Those methods show a significant effect on the voltage spike across the secondary side while increasing control complexity and adding losses. In [116], a current fed topology with capacitive output filter is used to minimise diode rectifier ringing and hence reduce the reverse recovery losses in the secondary rectifier diodes.

### 7.2.1 Operation Principle of PS-FB DC-DC Converter

The PS-FB converter as depicted in Figure 7.1 uses the circuit parasitic elements such as the switch junction capacitance ( $C_{o s s}$ ) and the transformer leakage inductance ( $L_{L K}$ ) to achieve ZVS of the FB switches. The two legs of the FB are operated with a phase shift which enables a resonant discharge of the $\left(C_{\text {oss }}\right)$ of the devices and forces the antiparallel diode to conduct before the conduction of the transistor. ZVS for the leading-leg (M1 and M4) can be achieved even at light loads because the body-diodes MD1 and MD4 can always be turned on by the energy stored in both $L_{L K}$ and the


Figure 7.1: PS-FB converter topology.
output filter inductor $\left(L_{o}\right)$. However, the energy stored in $L_{L K}$ may be insufficient to realise ZVS for the lagging-leg (M2 and M3) at high input voltage and/or light load conditions. To realise ZVS in the lagging-leg, an external auxiliary high frequency inductor (HFI) $L_{A u x}$ is connected in series to the transformer primary side ( $L_{r}=L_{L K}+L_{A u x}$ ). Adding a large auxiliary HFI, though, has several disadvantages such as an increase of the duty cycle loss $(\Delta D)$ and a large circulating current during freewheeling, resulting in high conduction loss and hence limiting the power transfer capability of the converter [109-113]. To overcome these drawbacks, several zero-voltage and zero-current switching (ZVZCS) full-bridge PWM converters have been proposed [107, 109-111, 114-116]. A ZVZCS PWM FB converter achieves ZVS for the leading-leg in a similar manner as in the conventional PS-FB. Forcing the primary current $\left(I_{p}\right)$ to zero during the freewheeling period, ZCS can be realised for the lagging-leg. $C_{o 1}$ is quit small and acts a clamp to suppresses the voltage spike across the rectifier. Most of the proposed methods so far require additional auxiliary circuits and passive elements which in turn increase the complexity of the converter control.

In this work, ZVZCS is achieved using the SiC MOSFETs parasitic output capacitance and the parasitic leakage inductance of the transformer. The capacitive output filter is used to clamp the voltage across the output rectifier. Therefore, no additional auxiliary circuits and passive elements are needed, which results in low losses, low cost and small volume.

## Operating Principle

The main waveforms of the proposed ZVZCS PS-FB converter are shown in Figure 7.2. To achieve ZCS for the lagging leg, the primary current $I_{p}$ is forced to reduce to zero.


Figure 7.2: Simulation: operating waveforms of ZVZCS PS-FB.

At $t_{3}$, the transistor M1 is turned-off and $I_{p}$ charges the parasitic output capacitance of M1 ( $C_{o s s-1}$ ) and discharges $C_{o s s-4}$ and then forward biases the body-diode MD4. Therefore, switches M1 and M4 always achieve ZVS with the help of the total energy stored in $L_{L k}\left(E_{L L K} \propto I_{p}{ }^{2}\right)$. As the primary current becomes zero, the output rectifiers D1 and D2 become reverse biased and no more power is transferred to the load side. With this approach, both reverse recovery and switching losses of
the output rectifier diodes are eliminated. During the interval $\left(t_{3}-t_{4}\right)$, the output capacitance ( $C_{o 2}$ ) supplies the whole load current, so there is no circulating current on the primary side. Compared to the conventional PSFB converter (" $I_{p}$ with $L_{r}$ " waveform in Figure 7.2), the elimination of the circulating current during the freewheeling period will significantly decrease the total losses of the converter, especially for high loads. Since $I_{p}=0$, M2 is turned-off with ZCS at $t_{4}$. After a small dead-time and due to the limitation of the $\mathrm{d} i_{p} / \mathrm{dt}$ caused by $L_{L K}$ [117], M3 will either turn-on with ZVS or in a hard-switching (HS) condition with a relatively small current. Using an external auxiliary HFI, the interval between $\left(t_{4}-t_{6}\right)$ represents the effective loss of duty cycle $\left(\Delta d=\Delta d_{1}+\Delta d_{2}\right)$ caused by the finite slope of the rising and falling edges of the primary current due to the presence of the resonant inductor $L_{r}[117,118]$. During this interval, as indicated in Figure 7.2 with the dashed black line, the primary current changes from $I_{p 2}$ to $-I_{p 1}$.

### 7.3 Power Loss Prediction

### 7.3.1 Analytical Calculation of Switching and Conduction Losses

For high-power and high-switching frequency applications, an accurate measurement of switching and magnetic losses becomes difficult. In this section, first an analytical loss model is derived. The results are compared to a practical method to break down the overall power loss distribution measured directly in the test converter. The power losses are classified mainly to losses due to semiconductors (switching and conduction) and magnetic components (core and windings). For the general case, an analytical power loss equation is derived based on the waveforms shown in Figure 7.2 with the use of an external HFI. For the proposed ZVZCS, this model is valid by setting $\Delta \mathrm{d}$ (approximately) and $I_{p 2}$ to zero (see Figure 7.2). The average value of the conduction losses of a SiC MOSFET is calculated by integration of the instantaneous power loss during a switching period:
$P_{\text {Cond-MOSFET }}=\frac{1}{T_{s}} \int_{0}^{T_{s}}\left(R_{D S o n}\left(T_{c}\right) i_{p}^{2}(t)\right) d t=R_{D S o n} I_{\text {MOS-rms }}^{2}$

The conduction losses in leading and lagging legs are different because the switch waveforms differ. They are calculated based on the rms value of the primary current:

$$
\begin{align*}
I_{p_{-} r m s}^{2} & =\frac{2}{T_{s}} \int_{t 3}^{t 7} i_{p}^{2}(t) d t \\
& =\frac{1}{3}\left[I_{p 1}^{2}\left(d-\Delta d_{1}\right)+I_{p 2}^{2}\left(1-d+\Delta d_{1}\right)+I_{p M A X}^{2}(1-\Delta d)+I_{p 1} I_{p M A X}(d-\Delta d)+I_{p 2} I_{p M A X}(1-d)\right] \tag{7.2}
\end{align*}
$$

The conduction losses of leading $\left(P_{\text {Cond_Lead }}\right)$ and lagging $\left(P_{\text {Cond_Lag }}\right)$ legs can be expressed as:

$$
\begin{align*}
P_{\text {Cond_Lead }} & =2 R_{\text {DSon }} I_{r m s \_ \text {Lead }}^{2} \\
& =\frac{2}{T_{S}} R_{D S o n} \int_{t 4}^{t 7} i_{\text {Lead }}^{2}(t) d t \\
& =\frac{1}{3} R_{D S o n}\left[I_{p 1}^{2}\left(d-\Delta d_{1}\right)+I_{p M A X}^{2}(d-\Delta d)+I_{p 1} I_{M A X}(d-\Delta d)\right]  \tag{7.3}\\
P_{\text {Cond_Lag }} & =2 R_{D S o n} I_{r m s \_L a g}^{2}=\frac{2}{T_{s}} R_{D S o n} \int_{t 4}^{t 8} i_{\text {Lag }}^{2}(t) d t \\
& =\frac{1}{3} R_{D S o n}\left[I_{p 1}^{2}\left(d-\Delta d_{1}\right)+I_{p 2}^{2}(1-d)+I_{p M A X}^{2}(1-\Delta d)+I_{p 1} I_{M A X}(d-\Delta d)+I_{p 2} I_{M A X}(1-d)\right] \tag{7.4}
\end{align*}
$$

As shown in Figure 7.2, both legs are turned-off with different currents. The turn-off losses for leadingand lagging-legs are therefore calculated as follows:
$P_{S W-M O S F E T-L e a d}=\frac{1}{T_{s}} \int^{t_{o f f}}\left(v_{D S}(t) i_{p M A X}(t)\right) d t$
$P_{S W-M O S F E T-L a g}=\frac{1}{T_{s}} \int^{t_{o f f}}\left(v_{D S}(t) i_{p 2}(t)\right) d t$

The losses of the output rectifier diodes can be estimated with the average and rms diode current according to (7.7), using the diode on-state voltage $\left(V_{T}\right)$ and on-state resistance $\left(R_{T}\right)$.
$P_{\text {Rec-Diode }}=V_{T} I_{\text {Diode-Avg }}+R_{T} I_{\text {Diode-rms }}^{2}$

### 7.4 High-Frequency Transformer

In high-power and high-frequency applications, the transformer is a key component. In the considered PS-FB unidirectional DC/DC converter, the high-frequency transformer operates under the conditions given in Table 7.1. The selection of the transformer core and winding wire has been optimised to minimise the core and winding losses. The saturation flux and the losses of the core material have a great impact on the power density and efficiency of the transformer. In high-frequency applications, ferrite materials are preferred because of their lower core loss compared to other materials.

Table 7.1: Converter design specifications.

| Power $\left(P_{o}\right)$ | 10 kW |
| :--- | :--- |
| Input voltage $\left(V_{\text {in }}\right)$ | 600 V |
| Output Voltage $\left(V_{o}\right)$ | $300-400 \mathrm{~V}$ |
| Switch.,Frequency $\left(f_{s w}\right)$ | $100-250 \mathrm{kHz}$ |
| Dead-Time | 140 ns |
|  | -C 2 M 0080120 D |
| SiC MOSFETS | -SCH 208 KE |
|  | $-\mathrm{SCT3040KL}$ |
| Rectifier Diodes | -SCS 240 AE 2 C |
| Turns Ratio $(\mathrm{n})$ | 1.5 |
| Leakage Ind. $\left(L_{L K}\right)$ | $\approx 2 \mu \mathrm{H}$ |
| Auxiliary Ind. $\left(L_{A u x}\right)$ | $(10-30) \mu \mathrm{H}$ |
| Ferrite Material / Core | $-3 \mathrm{~F} 3 / \mathrm{ETD} 59 / 31 / 22$ |
|  | $-\mathrm{N} 87 /$ Double E65/32/27 |

### 7.4.1 Optimal Selection of Flux Density

For a certain core design, the core $\left(P_{c}\right)$ and winding $\left(P_{w}\right)$ losses can be expressed as a function of the flux density [108]:
$P_{c}=A_{c} l_{m} K f_{s w}^{\alpha} \Delta B^{\beta}$
$P_{w}=K_{r} \frac{\lambda_{1}^{2} \rho(M L T)}{4 A_{\text {win }} k_{u} A_{c}^{2}}\left(\frac{1}{\Delta B}\right)^{2} I_{r m s}^{2}$
where $l_{m}$ is the magnetic path length, $A_{c}$ is the core cross section area, $K$ is the core loss coefficient, $\Delta B$ is the peak AC flux density and $\alpha$ and $\beta$ are core loss exponents. Concerning the winding losses,
$K_{r}$ is the normalized value of the AC resistance at $\mathrm{HF}, k_{u}$ is the fill factor, $A_{\text {win }}$ and $A_{c}$ are window and cross section area of the core respectively, $\lambda_{1}$ is the applied primary volt-sec, $M L T$ is the mean length per turn and $\rho$ is the resistivity of copper. At a given frequency, the optimum flux density occurs when the derivative of the total transformer power loss $\left(P_{t o t}=P_{c}+P_{w}\right)$ is zero. This means that the minimum loss can be achieved if we design the core operating at the optimal flux density $B_{\text {opt }}$, as shown in Figure 7.3. It is feasible to solve $\mathrm{dP} / \mathrm{dB}$ and $\mathrm{dP} / \mathrm{dn}$ for the optimal flux density and optimal number of turns ( $n_{\text {opt }}$ ) that minimise the total transformer power loss.
$\Delta B_{o p t}=\left[\frac{K_{r} I_{r m s}^{2} \rho \lambda_{1}^{2} M L T}{4 k_{u} A_{\text {win }} A_{c}^{3} l_{m} \beta K f_{s w}^{\alpha}}\right]^{\frac{1}{\beta+2}}$

$$
\begin{equation*}
n_{\text {opt }}=\left[\frac{\beta K f_{s w}^{\alpha-\beta}\left(\frac{V_{i n}}{2 A_{c}}\right)^{\beta} A_{c} L_{m} k_{u} A_{\text {win }}}{2 \rho k_{r} M L T I_{r m s}^{2}}\right]^{\frac{1}{\beta+2}} \tag{7.11}
\end{equation*}
$$



Figure 7.3: Optimal flux density for minimum total loss for different HFT design.

Two different HFT designs based on different core shapes are analysed. Using 3F3 ferrite material and an ETD59/31/22 core, the optimum flux density is calculated to 168 mT and the number of turns to 18 . This results in 17 W winding and 25 W core losses at 200 kHz . Due to the expected high surface temperature rise of the small ETD-core $\left(\Delta T>85^{\circ} \mathrm{C}\right)$, a second design is performed with a double EE65/32/27 core using N87 material and optimised at 100 kHz . The $\Delta B_{\text {opt }}$ reduces to 133 mT resulting in 19 W winding and 23 W core losses at 100 kHz .

In high-frequency transformers and inductors, winding losses are usually kept under control by using multi-strand high-frequency litz wire or/and copper foil. According to [108], the optimal number of litz-wire strands to minimise the total winding losses should be chosen to have an AC resistance $\left(R_{A C}\right)$ being around two times of its DC resistance $R_{D C}$. With this approach, the ETD transformer windings are made of litz wire. The employed litz wire for both HV and LV sides contains two parallel 1000 strands with a diameter of 0.05 mm . The EE-transformer windings are made of copper foil with a total cross section area of $5.4 \mathrm{~mm}^{2}$. Further, different HFT prototypes using different conductor designs and winding arrangements are presented in Section 7.7.

### 7.5 Power Loss Measurement

In the experimental setup, the input and output power is measured with a precision power analyser LMG670. A water cooling system is used to cool the devices and measure the power loss generated by SiC MOSFETs and diodes, allowing to separate semiconductor and transformer / inductor losses. To extract the winding losses of the transformer and inductor, the rms value of the primary current as well as the total equivalent series resistance (ESR) of the magnetic components are measured. The AC resistance of the magnetic components is measured as a function of the frequency using a precision LCR meter ST2827C. The switching losses of the SiC MOSFETs at given turn-on and -off currents are extracted based on the measured DPT results. In the same manner, the conduction losses of the MOSFETs are estimated with help of the measured temperature dependency of $R_{D S o n}$. The complete procedure of breaking down of the measured losses is summarized in Figure 7.4.

### 7.6 Experimental Results and Discussion

A 10 kW , (100-250) kHz prototype of the ZVZCS-PS-FB DC/DC converter has been built and tested. The converter specifications used in the test are shown in Table 7.1. Figure 7.5 depicts the waveforms of the PS-FB converter at $8 \mathrm{~kW}, 150 \mathrm{kHz}$ using an external HFI $\left(L_{r}=12 \mu \mathrm{H}\right)$. In this case, both legs turn-on with ZVS and turn-off in HS-mode. The circulating current during the freewheeling mode can be observed.

Figure 7.6 and Figure 7.7 illustrate the main waveforms of the proposed ZVZCS at $10 \%(1 \mathrm{~kW})$ and $80 \%(8 \mathrm{~kW})$ load. Using SiC devices, it is obvious that the converter is able to operate with ZVZCS for a wide power rang without any additional active or passive circuit.

(a)

(b)

Figure 7.4: Procedure of power loss breakdown in HF PS-FB converter a) overall losses and b) switching and conduction losses of SiC devices.


Figure 7.5: a) ZVS converter waveforms at 8 kW using $L_{r}=12 \mu \mathrm{H}$ and b) enlarged waveforms.

Under light load condition $\left(P_{o}<2 \mathrm{~kW}\right)$, because of the energy stored in the $L_{L K}\left(E_{L L K} \propto I_{p}{ }^{2}\right)$ is not sufficient to realise soft switching for the SiC devices, both leading and lagging legs are turned-on with a hard switching condition (see Figure 7.6). Compared to the conventional converter, the freewheeling circulating current mode is eliminated which in turn increases the overall efficiency especially at high power level. Using the capacitive output filter, the overshoot in both primary and secondary voltages are clamped to the their corresponding voltage level without using an additional circuit. Because of that, 650 V rectifier diodes are used in the prototype rather than overrated ( 1.2 kV ) diodes [107], reducing the rectifier loss.

The overall efficiency is measured applying the different MOSFETs. Figure 7.8 provides the efficiency


Figure 7.6: a) ZVZCS converter waveforms at $10 \%$ load and b) enlarged waveforms.


Figure 7.7: a) ZVZCS converter waveforms at $80 \%$ load and b) enlarged waveforms.
comparison for the whole converter at $100 \mathrm{kHz}, 200 \mathrm{kHz}$ and 250 kHz . Due to the reduction of the $R_{D S o n}$, applying trench device leads to a higher efficiency at 100 kHz . On the other hand, because of the lower switching energies, using C2M planar device gives a higher efficiency at higher switching frequency. Compared to the conventional converter with $L_{r}=12 \mu \mathrm{H}$, the proposed ZVZCS leads to a higher efficiency for a wide power range. Exemplarily, Figure 7.9 shows the loss distribution at 8 kW using SCH and SCT devices at 100 kHz and 200 kHz . Since no freewheeling circulating current period exists for the ZVZCS setup, the full bridge MOSFET conduction loss is about $9 \%$ of the overall power loss. It is worth mentioning that even at $250 \mathrm{kHz}, \mathrm{SiC}$ devices still operate with acceptable temperature safety margin. The extracted transformer losses show a good agreement with the calculation and optimisation procedure. At 200 kHz , the transformer temperature rise $\left(T_{\text {surface }}>120^{\circ} \mathrm{C}\right)$ limits the maximum output power to 8 kW . To verify the derived analytical power loss model, Table 7.2 gives


Figure 7.8: Measured efficiency of the ZVZCS at (a) 100 kHz , (b) 200 kHz and (c) 250 kHz .
a comparison between the analytical and measured losses at $8 \mathrm{~kW}, 100 \mathrm{kHz}$ using trench device (SCT). The breakdown of the measured losses is in good agreement with analytical/simulation results allowing to predict losses in SiC converters depending on DPT characterisation results and circuit simulation.

Table 7.2: Comparison between measured and calculated losses at $8 \mathrm{~kW}, 100 \mathrm{kHz}$ using MOSFET SCT3040KL.

|  |  | $P_{\text {measured }} /$ Conditions | $P_{\text {Calculation }} /$ Conditions |  |
| :--- | :---: | :---: | :---: | :---: |
| SiC MOS SW (x4) | 63 W | $E_{\text {tot }}\left(I_{d s}\right)+E_{\text {tot }}\left(T_{j}\right)$ | 62 W | Eqt. 7.5 + Eqt. 7.6 and LTspice Sim. |
| SiC MOS Cond. (x4) | 18 W | $R_{\text {DSon }}\left(T_{j}\right)$ | 17 W | Eqt. 7.3 + Eqt. 7.4: $R_{\text {DSon }}=50 \mathrm{~m} \Omega, d_{\text {eff }}=0.88$ |
| HFT-Core | 25 W | Fig. 7.4, ESR measurement | 23 W | Eqt. $7.8+$ Eqt. 7.9: |
| HFT-Wind. | 17 W | and thermal camera | 19 W | Core dimensions from datasheet |
| Rectifier (x4) | 64 W | Calorimetric meth.+ Fig. 7.4 | 60 W | Eqt. 7.7:$I_{\text {Diode-rms }}=20 \mathrm{~A}, I_{\text {Diode-Avg }}=10 \mathrm{~A}$, <br> $R_{T}=17 \mathrm{~m} \Omega, V_{T}=0.8 \mathrm{~V}$ |



Figure 7.9: Loss breakdown at 8 kW with a) SCT-trench and b) SCH-planar devices.

### 7.7 HFT Impact on Total Converter Efficiency

One of the design challenges of the high-density power converter is to optimise the high-density magnetic components. Due to the skin and proximity effects, the non-uniform current distribution over the cross-section of the conductors significantly increases the winding loss.

HFT design criteria and loss optimisation has been presented in Section 7.4. In this section, the influence of different wire types and winding arrangement on the HFT is introduced. In high-frequency transformers and inductors, winding losses are usually kept under control by using multi-strand highfrequency Litz wire or/and copper foil. With its higher width to thickness ratio, the copper foil plate is preferred to use in the high current application. It provides a better heat conduction and thus a good heat transfer to the ambient can be achieved. Optimising the foil thickness will efficiently reduce the skin effect and interleaving the primary and secondary windings minimises the proximity effect [119-122].

On the other hand, using Litz wires reduces the skin and proximity effects and provide a good AC/DC resistance ratio, while a large window area is required. Besides that, due to multi-isolated strands, a higher thermal resistance is expected and thus the cooling of the Litz wire becomes a problem [123-126].

To figure out these issues, different prototypes were built based on a double EE65 core, considering different conductor types and number of turns on primary and secondary sides. Table 7.3 summarises
the main specifications and design parameters of the double EE65 transformer prototypes. Clearly, the ETD59 transformer ( $3.21 \mathrm{~kW} / \mathrm{in}^{2}$, right transformer in Figure 7.10) is considerably smaller than the double EE65 (1.04 kW/in ${ }^{2}$ ) as shown in Figure 7.10. All samples have the same turns ratio (n $=1.5$ ). Samples 1 and C are based on the copper foil on both sides, but have a different number of turns. Reducing the number of turns results in a lower winding loss while a higher core loss is expected. With this assumption, both DC and AC resistance of sample-C reduce by approximately $50 \%$ compared with sample-1. Further, sample-A is a full Litz wire prototype, where the same wire cross section area is used on both sides. Litz as well as copper foil are used in samples B and D,

Table 7.3: HFT samples based on a double EE65/32/27 core.

| Properties / Samples | 1- EE65 | A- EE65 | B- EE65 | C- EE65 | D- EE65 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Core Material | N87 | N87 | N87 | N87 | N87 |
| Primary Turns ( $n_{p}$ ) | 15 | 15 | 15 | 9 | 9 |
| Primary Winding | Copper Foil ( $36 \mathrm{~mm} \times 0.15 \mathrm{~mm}$ ) | 4 litz wires in parallel ( $90 \times \emptyset 0.10 \mathrm{~mm}$ ) | 4 litz wires in parallel $(90 \times \emptyset 0.10 \mathrm{~mm})$ | Copper Foil ( $36 \mathrm{~mm} \times 0.08 \mathrm{~mm}$ ) | 4 litz wires in parallel ( $90 \times \emptyset 0.10 \mathrm{~mm}$ ) |
| Secondary Turns ( $n_{s}$ ) | 10 | 10 | 10 | 6 | 6 |
| Secondary Winding | Copper Foil ( $36 \mathrm{~mm} \times 0.15 \mathrm{~mm}$ ) | 4 litz wires in parallel ( $90 \times \emptyset 0.10 \mathrm{~mm}$ ) | $\begin{gathered} \text { Copper Foil } \\ (36 \mathrm{~mm} \times 0.15 \mathrm{~mm}) \end{gathered}$ | Copper Foil ( $36 \mathrm{~mm} \times 0.08 \mathrm{~mm}$ ) | $\begin{gathered} \text { Copper Foil } \\ (36 \mathrm{~mm} \times 0.15 \mathrm{~mm}) \end{gathered}$ |
| $L_{L K}(\mu \mathrm{H})$ | 1.4 | 2.33 | 1.35 | 0.74 | 0.94 |
| $R_{D C}(\mathrm{~m} \Omega)$ | 30 | 24 | 25 | 13 | 15 |
| $\begin{aligned} & R_{A C}(\mathrm{~m} \Omega) \\ & (100 / 200) \mathrm{kHz} \end{aligned}$ | 82 / 125 | 72 / 100 | $70 / 96$ | 52 / 63 | 53/68 |



Figure 7.10: 10 kW ferrite core HF transformer prototypes
with a different number of turns. The copper foil is used on the secondary side (high current side) to guarantee a sufficient copper area, low DC resistance and a good heat transfer to the ambient. Conversely, to reduce the AC resistance, a Litz wire is used on the primary side. As shown in Table 7.3, mixing the conductor types exhibits a good electrical characteristic through reducing the AC and DC resistance.

### 7.7.1 Experimental Results

In order to verify the theoretical analysis, all samples have been tested using the proposed ZVZCS PSFB converter. The measured efficiency is depicted in Figure 7.11, while the measured surface temperature distribution at 10 kW and 100 kHz are illustrated in Figure 7.12.


Figure 7.11: HFT impact on the total converter efficiency a) 100 kHz and b) 200 kHz .


Figure 7.12: The measured surface temperature distribution of the primary (right) and secondary (left) sides at 10 kW and 100 kHz .

For both switching frequencies, sample-A with full Litz wire shows the worst efficiency and temperature distribution. This is mainly due to the high thermal resistance of this configuration and hence poor heat transfer to the ambient. On the other hand, using the mixed conductors (samples B and D)
gives a high efficiency and almost a uniform temperature distribution for both primary and secondary sides. Figures 7.13 and 7.14 compare the thermal hot spots of the samples A and B at 100 and 200 kHz respectively. Because of the small copper area and different current densities, sample-C shows a non-uniform temperature distribution on the primary and secondary sides (See Appendix C).

According to the manufacturer datasheet, the ferrite cores of all samples are still considered working in the optimal temperature operation $\left(70-110^{\circ} \mathrm{C}\right)$. In a summary, compared to sample-A, using both Litz and copper foil mitigates the effect of winding loss, and an improvement of $0.4 \%$ and $0.8 \%$ are measured for the total converter efficiency at 100 kHz and 200 kHz , respectively.


Figure 7.13: Hot spot temperature of a) sample-A and b) sample-B at 10 kW and 100 kHz


Figure 7.14: Hot spot temperature of a) sample-A and b) sample-B at 8 kW and 200 kHz

## Chapter 8

## SiC-based Dual Active Bridge for High-Efficiency DC/DC Converter

### 8.1 Introduction

The dual-active-bridge isolated bidirectional (DAB-IB) DC/DC converter is well accepted for applications where bidirectional power flow, high power density, and galvanic isolation are required. The DAB-IB has been widely applied to different energy storage systems $[28,127,128]$ as well as to distributed generation [103-105] and automotive applications [129-131].

Modulation control schemes for the dual-active-bridge have recently been an active research area. Several control techniques have been proposed to extend the soft-switching region and to optimise the current stress of the semiconductors. The single phase-shift (SPS) control is commonly employed in many applications. It has one degree of freedom to control the required transmission power. However, the soft-switching range is limited, and the high circulating current through the transformer, together with the transistors, deteriorates the total efficiency of the dual-active-bridge (DAB) converter [103, 131-136]. To cope with these problems, several improved control strategies have been proposed, such as the extended phase shift (EPS) [103], dual phase shift (DPS) [137, 138], and triple phase shift (TPS) [139].

Both EPS and DPS schemes, on the one hand, have two degrees of freedom, which can effectively reduce the current stress and improve the total converter efficiency. Different from the SPS control method, the DPS adjusting the time sequence between the driving signals of diagonal switches of bridges A and B, and both phase-shifts are assumed the same. The output AC voltage of the primary
and secondary thus becomes a three-level wave. However, because the phase-shifts of the bridges are set the same, all the presented solutions show that this control method has suboptimal operating modes and cannot optimise the whole operating zones. On the other hand, three independent control variables are associated with the TPS method, where the power flow is controlled by two inner phase shifts between the legs in the full-bridge and an outer phase shift between the primary and secondary sides. Compared to SPS, all these control methods increase the complexity of the control. In general, the SPS, EPS, and DPS methods can be considered to be special cases of the TPS control. Furthermore, a hybrid control method that uses different control techniques is introduced in [140], where a modified DAB is proposed and a both EPS and TPS controls are used to optimise the switching behaviour. However, this technique increases the complexity of the control implementation.

In this chapter, a modified dual phase shift (MDPS) control method is proposed to overcome the inherent disadvantages of the SPS control and to provide a simple control implementation, compared with other control schemes. First, both methods are theoretically analysed. By analysing the switching behaviour at each switching state, a mathematical model of power losses and current stress is derived and compared for both techniques. In addition, the soft-switching range, including ZVS and ZCS, is evaluated. Furthermore, to limit the inrush starting current, a soft-starting procedure without using external hardware will be presented. Finally, a $6 \mathrm{~kW}, 100 \mathrm{kHz}, \mathrm{DAB}-\mathrm{IB}$ converter is built to validate the effectiveness of the proposed control strategy. The overall efficiency of the converter is evaluated and compared for both control methods.

### 8.2 Single Phase-Shift Modulation

The basic DAB-IB topology is illustrated in Figure 8.1. It consists of two active bridges linked by a high-frequency transformer (HFT) and an external high frequency inductor (HFI) ( $L_{r}$ ). In addition to the galvanic isolation, the HFT provides the required matching voltage level between the input and output sides, while the HFI serves as an energy storage component and helps to realise the soft switching.

Using SPS modulation, the output voltages of the primary and secondary sides are a square wave with a $50 \%$ duty cycle. The power transfer is controlled by adjusting the phase-shift ratio $(D)$ between the AC output voltage of the primary $\left(V_{p}\right)$ and secondary $\left(V_{s}\right)$ sides. The typical waveforms of the DAB-IB under SPS control are illustrated in Figure 8.2, where, $V_{i n}$ and $V_{o}$ are the input and output DC voltages


Figure 8.1: DAB-IB DC/DC converter topology.
respectively, $i_{L r}$ is the HFI current, $n$ represents the turns ratio of the isolated HFT, $V_{s}^{\prime}$ represents the secondary voltage refer to primary side, and $D$ is the phase-shift ratio in a half-switching period $\left(T_{h s}\right)$ [ $D=\phi / \pi$, where $\phi$ is the phase-shift in degree] [103, 131-136].

At each interval, the analytical expression of $i_{L r}$ is given in (8.1), while the inductor currents at each switching times are summarised in (8.2).

$$
\begin{align*}
& i_{L r}(t)= \begin{cases}\frac{V_{o}^{\prime}(m+1)}{L_{r}} t-\frac{V_{o}^{\prime}}{4 f_{s w} L_{r}}(2 D+m-1) & t_{0} \leq t \leq t_{2} \\
\frac{V_{o}^{\prime}(m-1)}{L_{r}} t-\frac{V_{o}^{\prime}}{4 f_{s w} L_{r}}((2 D-1) m+1) & t_{2} \leq t \leq t_{3} \\
\frac{-V_{o}^{\prime}(m+1)}{L_{r}} t+\frac{V_{o}^{\prime}}{4 f_{s w} L_{r}}(2 D+m-1) & t_{5} \leq t \leq t_{5} \\
\frac{V_{o}^{\prime}(1-m)}{L_{r}} t-\frac{V_{o}^{\prime}}{4 f_{s w} L_{r}}((2 D-1) m+1)\end{cases}  \tag{8.1}\\
& \begin{cases}i_{L r}\left(t_{0}\right)=-\frac{V_{o}^{\prime}}{4 f_{s w} L_{r}}(2 D+m-1) & \\
i_{L r}\left(t_{1}\right)=0 \\
i_{L r}\left(t_{2}\right)=\frac{V_{o}^{\prime}}{4 f_{s w} L_{r}}((2 D-1) m+1) & \\
i_{L r}\left(t_{3}\right)=\frac{V_{o}^{\prime}}{4 f_{s w} L_{r}}(2 D+m-1) & \\
i_{L r}\left(t_{4}\right)=0 & V_{L r} \\
i_{L r}\left(t_{5}\right)=-\frac{V_{o}^{\prime}}{4 f_{s w} L_{r}}((2 D-1) m+1) & \end{cases} \tag{8.2}
\end{align*}
$$



Figure 8.2: Typical waveforms of DAB-IB with SPS modulation.
where $V_{o}^{\prime}=n V_{o}$ and $m$ is the conversion ratio ( $m=V_{i n} / V_{o}^{\prime}$ ).
With the assumption that the input and output DC voltages are constant over a switching period, the average output power $\left(P_{o}\right)$ neglecting losses can be calculated as follows:

$$
\begin{align*}
P_{o} & =\frac{2}{T_{s}} \int_{0}^{T_{s} / 2} v_{p}(t) i_{L r}(t) d t \\
& =\frac{2 V_{p}}{T_{s}} \int_{0}^{T_{s} / 2} i_{L r}(t) d t \tag{8.3}
\end{align*}
$$

Substituting (8.1) into (8.3) yields
$P_{o}=\frac{m n^{2} V_{o}^{2}}{2 f_{s w} L_{r}} D(1-|D|) \quad \forall \quad-1<D<1$
where, $P_{o}>0$ indicates power transfer from bridge-A to bridge-B and vice versa for $P_{o}<0$.
The maximum achievable output power $\left(P_{o-\max }\right)$ is obtained at $D=0.5\left(d P_{o} / d D=0\right)$, and determines the upper limit for $L_{r-\max }$ :
$L_{r-\max }=\frac{m n^{2} V_{o}^{2}}{8 f_{s w} P_{o-\max }}$
Increasing the switching frequency dramatically reduces the size of the required inductor and hence reduces the losses. However, to optimise the switching operation, the phase-drift phenomenon that occurs in DAB-IB converter should be avoided. This phenomenon is correlated with the dead-time $\left(T_{D}\right)$, where the transmission power remains at a constant value with increases in the phase-shift angle until the phase shift becomes greater than the dead-time period. Further details about this phenomenon can be found in [132, 141]. In this work, a dead-time of $100 \mathrm{~ns}\left(\varphi=3.6^{\circ}\right.$ at 100 kHz ) is used; therefore, to avoid this issue at low power (e.g. 1 kW ), the minimum auxiliary HFI is calculated using (8.4), to be $37 \mu \mathrm{H}\left(\varphi=3.7^{\circ}\right.$ - see Figure 8.3). To improve the resolution of the phase-shift angle and prevent any EMI problems at low power, a $45 \mu \mathrm{H}\left(\varphi=4.6^{\circ}\right)$ is used during the real test.


Figure 8.3: Variation of auxiliary inductance with phase-shift and output power.

### 8.2.1 ZVS Conditions with SPS Modulation

To guarantee the soft-switching condition, such as ZVS, for both bridges, the minimum inductor current should be high enough to charge/discharge the effective parasitic capacitances ( $C_{e f f}$ ).
$0.5 L_{r} i_{L r}^{2}(t)>0.5 C_{e f f} V_{i n}^{2}$
where $C_{e f f}$ includes the output parasitic capacitance of the SiC MOSFET ( $C_{o s s}$ ) and the transformer winding capacitance $\left(C_{t r}\right)$.

The minimum inductor current required to achieve ZVS for Bridge- A is thus as follows:
$I_{L r}\left(t_{0}\right) \leq 0$

Combining (8.7) with (8.2 and 8.6), the following minimum phase-shift ratio ( $D_{\min }$ ) guarantees the soft switching:
$D_{\min }>\frac{1}{2}\left[1-m\left(1-4 f_{s w} \sqrt{L_{r} C_{e f f}}\right)\right]$

Regarding to Bridge-B, to achieve ZVS operation, the HFI current must be positive as:
$I_{L r}\left(t_{2}\right) \geq 0$

Combining (8.9) with (8.2 and 8.6) yields:
$\left.D_{\text {min }}>\frac{1}{2 m}\left[m+4 f_{s w} \sqrt{L_{r} C_{e f f}}-1\right)\right]$

Therefore, to ensure ZVS operation, conditions (8.8) and (8.10) should be satisfied, otherwise the soft switching will be lost. The ZVS boundary under different values of $m$ is illustrated in Figure 8.4. As demonstrated, for $m=1$, the ZVS can be guaranteed over the whole power range. However, when the conversion voltage ratio does not match $(m \neq 1)$, a narrow soft-switching range is achieved and a hard switching (HS) or partial ZVS will occur.


Figure 8.4: Soft switching boundaries of DAB using SPS modulation.

### 8.2.2 Current Stress and Circulation Current

Applying the SPS modulation, the RMS inductor current as well as the maximum current stress are increased with output power. Both currents become much higher when the voltage amplitudes of the primary and secondary sides do not match ( $\mathrm{m} \neq 1$ ), resulting in higher power losses, a reduction in the range of the soft switching, and therefore a substantial decrease in efficiency.

As depicted in Figure 8.2, and using (8.2), the maximum current stress, which occurs at $t_{3}$, can be expressed as follows:
$\left.i_{\text {Lrmax }}\right|_{t_{3}}=\frac{V_{o}^{\prime}}{4 f_{s w} L_{r}}(2 D+m-1)$
Furthermore, the current RMS value of $I_{L r}$ can be calculated as follows:
$i_{L r-r m s}=\sqrt{\frac{1}{3}\left[I_{2}^{2}\left(D-T_{1}\right)+\left(I_{2}^{2}+I_{3}^{2}+I_{2} I_{3}\right)(1-D)+I_{3}^{2}\left(T_{4}-1\right)\right]}$
where $I_{2}$ and $I_{3}$ are calculated using (8.2) at $t_{2}$ and $t_{3}$ respectively, $T_{1}=2 f_{s w} t_{1}, T_{4}=2 f_{s w} t_{4}$, and
$t_{1}=\frac{2 D+m-1}{4 f_{s w}(m+1)}$
$t_{4}=\frac{2 D+3 m+1}{4 f_{s w}(m+1)}$

The circulating current is related to $L_{r}$, and it increases further when the condition $\mathrm{m} \neq 1$ is applied. Additional details can be found in [103, 137, 138]. In brief, see the red dashed area in Figure 8.2, the inductor current is not always in phase with the primary voltage. Therefore, a certain amount of power is transferred back to the primary side from the converter during $t_{0}$ to $t_{1}$ and $t_{3}$ to $t_{4}$. Increasing the output power will noticeably increase the circulating current and hence increase the winding loss in the magnetic components and the conduction loss in the transistors.

### 8.2.3 Power Loss Prediction

## Conduction and Switching Losses

The average value of the conduction losses of a SiC MOSFET is calculated by integration of the instantaneous power loss during a switching period:
$P_{\text {cond-MOSFET }}=\frac{1}{T_{s}} \int_{0}^{T_{s}}\left(R_{D S o n}\left(T_{c}\right) i_{p}^{2}(t)\right) d t=R_{D S o n} I_{M O S-r m s}^{2}$

To minimise both the body-diode conduction loss and the reverse recovery, the synchronous rectification mode is applied to Bridge-B. According to the key waveforms depicted in Figure 8.2 and using (8.1 and 8.2), the total conduction loss of the SiC devices can be calculated as follows:

$$
\begin{equation*}
P_{\text {cond-MOSFETs }}=\left.2 R_{D S o n} I_{S 1,4-r m s}^{2}\right|_{t_{1}} ^{t_{3}}+\left.2 R_{D S o n} I_{S 2,3-r m s}^{2}\right|_{t_{4}} ^{t_{6}}+\left.2 n R_{D S o n} I_{Q 1,4-r m s}^{2}\right|_{t_{2}} ^{t_{5}}+\left.2 n R_{D S o n} I_{Q 2,3-r m s}^{2}\right|_{t_{5}} ^{t_{8}} \tag{8.14}
\end{equation*}
$$

where

$$
\begin{align*}
I_{S 1,4-r m s}^{2} & =I_{S 2,3-r m s}^{2} \\
& =\frac{1}{6}\left[I_{2}^{2}\left(D-T_{1}\right)+\left(I_{2}^{2}+I_{3}^{2}+I_{2} I_{3}\right)(1-D)\right]  \tag{8.15}\\
I_{Q 1,4-r m s}^{2} & =I_{Q 2,3-r m s}^{2} \\
& =\frac{1}{6}\left[\left(I_{2}^{2}+I_{3}^{2}+I_{2} I_{3}\right)(1-D)+\left(I_{3}^{2}+I_{5}^{2}-I_{3} I_{5}\right) D\right] \tag{8.16}
\end{align*}
$$

In the same manner, during the dead-time interval, the losses of the body-diodes can be estimated with the average and RMS diode currents according to (8.17), using the diode on-state voltage ( $V_{T}$ )
and on-state resistance $\left(R_{T}\right)$.
$P_{B D}=V_{T} I_{\text {Diode-Avg }}+R_{T} I_{\text {Diode-rms }}^{2}$

Assuming ZVS, only $E_{o f f}$ is included. For each device, the turn-off current is calculated using (8.2), and the corresponding loss is estimated using (4.42 to 4.44).
$P_{s w}=2 f_{s w}\left[\left.E_{o f f}\left(S_{2}, S_{3}\right)\right|_{i_{t o}}+\left.E_{o f f}\left(Q_{2}, Q_{3}\right)\right|_{i_{t 2}}+\left.E_{o f f}\left(S_{1}, S_{4}\right)\right|_{i_{t 3}}+\left.E_{o f f}\left(Q_{1}, Q_{4}\right)\right|_{i_{t 5}}\right]$

## HFT Losses

In this application, a more compact HFT design is used, based on a double EE55/28/25 core instead of EE65/32/27, and the new ferrite material 3C97 is used to minimise the core loss. Litz wire with nine turns is used on the primary side, while a copper foil with six turns is applied to the secondary side. Therefore, it is expected that both winding and core losses will decrease. According to the datasheet, using 3C97 core will reduce the core loss by around $30 \%$ compared to N 87 (at $100 \mathrm{kHz}, 100^{\circ} \mathrm{C}$, and 200 mT ). Equations (7.8 and 7.9) are used to calculate the core and winding losses respectively.

### 8.3 Modified Dual Phase-Shift (MDPS) Control

As previously mentioned, the SPS control technique cannot adjust the circulating current and the high current stress. To overcome the disadvantages of the SPS method, a simple control method based on a modified dual phase-shift control is proposed.

The MDPS control is implemented with two degrees of freedom to adjust the time sequence between the gate signals in both bridges. In this method, $\mathrm{D}_{1}$ is the phase-shift between switching S1 and S 4 (primary side), while $\mathrm{D}_{2}$ represents the phase shift between the diagonal control signals of the secondary bridge (Q1 and Q 4$)$. The output AC voltage of the primary and secondary bridges thus becomes a three-level wave. During the zero voltage level, the inductor current $\left(i_{L r}\right)$ is forced to reduce to zero. As a result, the circulating current is eliminated and ZVZCS is achieved for most of the active devices. The proposed control method goes through eight modes during a single switching cycle, each of which is thoroughly discussed below. The key waveforms and the operation modes of the DAB-IB converter applying the proposed control technique are illustrated in Figure 8.5 and 8.6 respectively.


Figure 8.5: Typical waveforms of DAB-IB with MDPS modulation.

## Mode-I $\left(t_{0}-t_{1}\right)$ :

S 2 is turned-off, and the primary current flows through S 3 and $\mathrm{D}_{S 1}$. Therefore, S 1 will turn-on with ZVS. On the secondary side, the current flows through Q2 and Q3 (SR-mode). Moreover, the voltage across $L_{r}$ is clamped at $n V_{o}$, and the primary current decreases until it reaches zero. This substate ends up when S3 and Q2 are turned-off. The equivalent circuit for this substate is depicted in Figure 8.6-a.

## Mode-II $\left(\boldsymbol{t}_{1}-\boldsymbol{t}_{2}\right)$ :

At $t_{1}$, switches S3 and Q2 are turned-off with ZCS. The output capacitance of switch S3 ( $C_{\text {oss }}-S 3$ )
is charged, while $C_{o s s-S 4}$ is discharged. The equivalent circuit is presented in Figure 8.6-b. The secondary voltage decreases quickly to zero. In this substate, the output filter capacitance $\left(C_{o}\right)$ supplies the whole load current. At $t_{2}$, due to the limitation of the $\mathrm{di}_{p} / \mathrm{dt}$ caused by $L_{r}$, the switches S4 and Q1 will turn-on either with ZCS or in an HS condition with a relatively small current.

## Mode-III $\left(\boldsymbol{t}_{2}-\boldsymbol{t}_{3}\right)$ :

In this substate, $i_{L r}$ flows through S 1 and S 4 in the primary side and through Q 1 and Q 3 in the secondary side. This substate ends up when Q3 is turned-off. The equivalent circuit for this substate is illustrated in Figure 8.6-c.
Mode-IV $\left(\boldsymbol{t}_{3}-\boldsymbol{t}_{4}\right)$ :
The primary side remains the same as in Mode-III. At $t_{3}$, Q3 is turned-off, and the dead-time period between Q3 and Q4 starts (see Figure 8.6-d). The output capacitance of switch Q3 ( $C_{\text {oss-Q3 }}$ ) is charged, while $C_{\text {oss }-Q 4}$ is discharged and then forward biases the body-diode DQ4. Thus, the switch Q4 is turned-on with ZVS, and the secondary current flows along paths Q1 and Q4. Furthermore, the voltage across $L_{r}$ is clamped at $V_{i n}-n V_{o}$. This substate ends up when S 1 is turned-off.

Mode-V $\left(\boldsymbol{t}_{4}-\boldsymbol{t}_{5}\right)$ :
At $t_{4}$, the switch S 1 is turned-off (see Figure 8.6-e), and the dead-time period between S 1 and S 2 starts. The primary current flows through S4 and DS2. Therefore, S2 will turn-on with ZVS. The voltage across $L_{r}$ is clamped at $-n V_{o}$, and the primary current decreases until it reaches zero. The secondary side remains the same as that in mode-IV. This substate ends up when S4 and Q1 are turned-off.

## Mode-VI ( $\boldsymbol{t}_{5}-\boldsymbol{t}_{6}$ ):

At $t_{5}, \mathrm{~S} 4$ and Q 1 are turned-off. The current paths of the primary and secondary sides are depicted in Figure 8.6-f. Similarly to mode-II, the switches S3 and Q2 will turn-on either with ZCS or in an HS condition with a relatively small current.

## Mode-VII $\left(t_{6}-t_{7}\right)$ :

In this substate, $i_{L r}$ flows through S2 and S3 in the primary side, while it flows through Q2 and Q4 in the secondary side. The voltage across $L_{r}$ is clamped at $-V_{i n}$. This substate ends up when Q4 is turned-off. The equivalent circuit for this substate is illustrated in Figure $8.6-\mathrm{g}$.

Mode-VIII $\left(\boldsymbol{t}_{7}-\boldsymbol{t}_{8}\right)$ :
At $t_{7}, \mathrm{Q} 4$ is turned-off. The primary current path remains the same as that in the previous mode. During the dead-time period, the secondary current flows through Q 2 and $\mathrm{Q}_{D 3}$. Therefore, Q 3 will turn-on with ZVS. Furthermore, the voltage across $L_{r}$ is clamped at $-V_{i n}+n V_{o}$.


(a) Mode-I

(c) Mode-III

(e) Mode-V

(g) Mode-VII

(b) Mode-II, Dead-Time Period

(d) Mode-IV

(f) Mode-VI, Dead-Time Period

(h) Mode-VIII

Figure 8.6: Operation modes of DAB-IB using the proposed MDPS control.

At each interval, the analytical expression of $i_{L r}$ is given in (8.19), while the inductor currents at each switching time are summarized in (8.20).

$$
\begin{align*}
& i_{L r}(t)= \begin{cases}\frac{V_{o}^{\prime}}{L_{r}} t-\frac{m V_{o}^{\prime}}{4 f_{s w} L_{r}}\left((1-2 m) D_{1}-m D_{2}+(m-1)\right) & t_{0} \leq t \leq t_{1} \\
0 & t_{1} \leq t \leq t_{2} \\
\frac{m V_{o}^{\prime}}{L_{r}} t+\frac{m V_{o}^{\prime}}{4 f_{s w} L_{r}}\left(D_{1}-m D_{2}+(m-1)\right) & t_{2} \leq t \leq t_{3} \\
\frac{V_{o}^{\prime}(m-1)}{L_{r}} t+\frac{m V_{o}^{\prime}}{4 f_{s w} L_{r}}\left(D_{1}+(2-m) D_{2}+(m-1)\right) & t_{3} \leq t \leq t_{4} \\
\frac{-V_{o}^{\prime}}{L_{r}} t+\frac{m V_{o}^{\prime}}{4 f_{s w} L_{r}}\left((1-2 m) D_{1}-m D_{2}+(m-1)\right) & t_{4} \leq t \leq t_{5} \\
0 & t_{5} \leq t \leq t_{6} \\
\frac{-m V_{o}^{\prime}}{L_{r}} t-\frac{m V_{o}^{\prime}}{4 f_{s w} L_{r}}\left(D_{1}-m D_{2}+(m-1)\right) \\
\frac{-V_{o}^{\prime}(m-1)}{L_{r}} t-\frac{m V_{o}^{\prime}}{4 f_{s w} L_{r}}\left(D_{1}+(2-m) D_{2}+(m-1)\right) & t_{7} \leq t \leq t_{8}\end{cases}  \tag{8.19}\\
& \begin{cases}i_{L r}\left(t_{0}\right)=-\frac{m V_{o}^{\prime}}{4 f_{s w} L_{r}}\left((1-2 m) D_{1}-m D_{2}+(m-1)\right) \\
i_{L r}\left(t_{1}\right)=0 & \\
i_{L r}\left(t_{2}\right)=0 & \\
i_{L r}\left(t_{3}\right)=\frac{m V_{o}^{\prime}}{4 f_{s w} L_{r}}\left(D_{1}+(2-m) D_{2}+(m-1)\right) \\
i_{L r}\left(t_{4}\right)=\frac{m V_{o}^{\prime}}{4 f_{s w} L_{r}}\left((1-2 m) D_{1}-m D_{2}+(m-1)\right) \\
i_{L r}\left(t_{5}\right)=0 & i_{L r}\left(t_{6}\right)=0 \\
i_{L r}\left(t_{7}\right)=\frac{m V_{o}^{\prime}}{4 f_{s w} L_{r}}\left(D_{1}+(2-m) D_{2}+(m-1)\right) & \end{cases}  \tag{8.20}\\
& \hline
\end{align*}
$$

Consequently, the average transferred power over single switching period is derived as follows:

$$
\begin{align*}
P_{o} & =\frac{2}{T_{s}} \int_{0}^{T_{s} / 2} v_{p}(t) i_{L r}(t) d t \\
& =\frac{2 V_{p}}{T_{s}} \int_{0}^{T_{s} / 2} i_{L r}(t) d t \tag{8.21}
\end{align*}
$$

Substituting (8.19) into (8.21) yields
$P_{o}=\frac{m n^{2} V_{o}^{2}}{4 f_{s w} L_{r}}\left(\left(D_{1}+D_{2}\right)-D_{1} D_{2}-\left(D_{1}^{2}+D_{2}^{2}\right)\right) \quad \forall \quad D_{1}+D_{2} \leqslant 1$

Taking the derivative value of (8.22), the maximum transmission power can be obtained when the following constraint is satisfied:
$2 D_{1}+D_{2}=1$

The 3-D curves of the transmission power is varied with $D_{1}$ and $D_{2}$, as illustrated in Figure 8.7. As demonstrated, the minimum transferred power can be obtained when $D_{1}=D_{2}=0$.


Figure 8.7: 3-D transmission power varied with $\mathrm{D}_{1}$ and $\mathrm{D}_{2}$. [Case study: $V_{i n}=600 \mathrm{~V}, V_{o}=400 \mathrm{~V}, f_{s w}=$ $100 \mathrm{kHz}, n=1.5$, and $L_{r}=20 \mu \mathrm{H}$.]

Furthermore, with regard to Figure 8.5, the maximum current stress, which occurs at $t_{3}$, can be expressed as follows:
$\left.i_{\text {Lrmax }}\right|_{t_{3}}=\frac{m V_{o}^{\prime}}{4 f_{s w} L_{r}}\left[D_{1}+(2-m) D_{2}+(m-1)\right]$

In the same manner, the primary RMS current passing through the auxiliary inductor $i_{L r}$ can be calculated as follows:
$i_{L r-r m s}=\sqrt{\frac{1}{3}\left[I_{3}^{2} D_{2}+I_{4}^{2} D_{1}+\left(I_{3}^{2}+I_{4}^{2}+I_{3} I_{4}\right)\left(1-D_{1}-D_{2}\right)\right]}$

Last, to calculate the conduction loss in the switches, the RMS switch current (e.g. switch S1) is derived as follows:
$i_{S 1-r m s}^{2}=\frac{1}{6}\left[I_{3}^{2} D_{2}+\left(I_{3}^{2}+I_{4}^{2}+I_{3} I_{4}\right)\left(1-D_{1}-D_{2}\right)\right]$

According to the previous analysis, the combination of $D_{1}$ and $D_{2}$ can minimise the current stress and hence improve the efficiency. Tuning $\mathrm{D}_{1}$ and $\mathrm{D}_{2}$ in a real application might be difficult. Therefore, first, the phase-shift $\mathrm{D}_{2}$ can be estimated from a lookup table implemented in the control system. Using the required power set point and the estimated value of $D_{2}$, the phase-shift $D_{1}$ can be calculated with (8.22) considering the constraint (8.23). Compared with other control schemes, e.g. EPS, DPS and TPS, using MDPS provides a simple control implementation. More interestingly, compared with the SPS method, this combination as well as using a high switching frequency will significantly reduce the size of the required inductor. As with the SPS technique, the upper limit of the auxiliary $\operatorname{HFI}\left(L_{r-\max }\right)$ is calculated at the maximum required power. By substituting (8.22) with (8.23), $L_{r-\max }$ is estimated at $10 \mu \mathrm{H}$. As previously mentioned, the minimum phase-shift time should be larger than the dead-time period. Using $L_{r}=10 \mu \mathrm{H}$, the minimum phase angle (at 1 kW ) is $4.7^{\circ}$, which is larger than the dead-time period $\left(3.7^{\circ}\right)$. Therefore, a total auxiliary inductance of $10 \mu \mathrm{H}$ is used with the MDPS method, compared with $45 \mu \mathrm{H}$ associated with SPS. The expected magnetic losses will thus be reduced.

### 8.4 Closed-Loop Control

To achieve a high efficient power transfer of the DAB-IB, the output voltage should be controlled so that unwanted transient effects can be avoided. In this work, a conventional PI controller is used. A feed-forward compensation is implemented to minimise the sensitivity of the system to the load variations, and the output of the PI controller $\left(D_{P I}\right)$ is added to the feed-forward phase-shift compensation ( $D_{F F}$ ). The control concept is illustrated in Figure 8.8.

Simply, for the SPS method, the feed-forward phase-shift compensation $D_{F F-S P S}$, can be calculated using (8.4) as follows:
$D_{F F-S P S}=\frac{1}{2}\left[1-\sqrt{1-\frac{8 f_{s w} L_{r} I_{o}}{n V_{i n}}}\right]$


Figure 8.8: Closed loop control of the DAB-IB.

Using the predefined value of $\mathrm{D}_{2}$ and the reference required output power, the feed-forward phase-shift compensation of the MDPS technique ( $D_{F F-M D P S}$ ) can be calculated using (8.22) as follows:
$D_{F F-M D P S}=\frac{1}{2}\left[-\left(D_{2}+1\right)+\sqrt{\left(D_{2}+1\right)^{2}+4\left(\frac{4 f_{s w} L_{r}}{n I_{o} V_{i n}}-D_{2}^{2}++D_{2}\right)}\right]$

As indicated, for both techniques, the output current $\left(I_{o}\right)$ as well as the input voltage $\left(V_{i n}\right)$ are used as feedback to update the calculation of the feed-forward phase shift angle. To maintain a constant output voltage, the measured output voltage is compared with a reference voltage ( $V_{o, r e f}$ ), and the voltage error is compensated through the PI controller. Therefore, the PI controller behaves as an auxiliary regulator to re-balance the error originating from the feed-forward calculation.

### 8.5 Soft-Starting Procedure

At the start of the DAB-IB converter, the high inrush current could lead to a saturation of the magnetic components, thereby causing the power MOSFETs to breakdown. To prevent such an inrush current, a soft-starting procedure without additional hardware is proposed. The proposed start-up procedure is divided into three stages:

## 1- Open-loop, phase-shift control (OL-PSC)

In this stage, the primary switches are turned-on with a relatively small duty cycle ( $D_{\text {cycle }}$ ), and they gradually increase to the normal duty cycle (50\%). During this stage, the output voltage is used as feedback to control the increment of the $D_{\text {cycle }}$. The secondary switches are kept off; their body diodes are thus used to charge up the output capacitance. This stage ends when the measured output voltage $\left(V_{\text {meas }}\right)$ reaches the first pre-charging reference voltage $\left(V_{p r e-1}\right)$ ( e.g. $70 \% V_{o}$ ).

## 2- Open loop with active secondary side (OL-AS)

As the measured voltage reaches $V_{\text {pre-1 }}$, the secondary switches are turned-on. The open-loop control is still activated, and a phase shift $D=0$ is applied. The output voltage is increased until the second pre-charging reference voltage ( $V_{\text {pre- }}$ ) is reached (e.g. $90 \% V_{o}$ ).

## 3- Closed-loop control (CLC)

In this stage, the closed loop control is activated. The PI controller regulates the required output voltage, and the feed-forward estimates the required phase-shift angle associated with the desired output power.

At all stages, the output voltage is always monitored. Therefore, if $V_{\text {meas }}$ exceeds the required limits in any stage, the start-up process jumps to the next stage, otherwise, the whole process is disabled.

### 8.6 Experimental Results

To verify the feasibility of the proposed control method, a $6 \mathrm{~kW}, 100 \mathrm{kHz}$, DAB-IB converter was built and tested. A photograph of the prototype is presented in Figure 8.9, and the converter specifications are illustrated in Table 8.1.

The experimental set-up is controlled using dSPACE RTI 1202 MicroLabBox platform. Two voltage transducers (LEM LV-25P) are used to measure the instantaneous input and output voltages, while the output current is measured using the (LEM LA-25 NP) transducer. The voltage/current sensors available for measuring such a power level have significant offset errors and low bandwidth. For example, according to the datasheet, the voltage sensor LV-25P has an accuracy of $0.9 \%$ and a linearity error of $<0.2 \%$, and these percentages are related to the voltage levels and switching frequency. Therefore, the input and output voltages in the test setup are further monitored with a high accuracy digital multimeter (Fluke 8840 A ) of $<0.005 \%$. Thus, the voltages feedback is manually

Table 8.1: DAB-IB converter design specifications.

| Power $\left(P_{o}\right)$ | 6 kW |
| :--- | :--- |
| Input Voltage $\left(V_{\text {in }}\right)$ | 600 V |
| Output Voltage $\left(V_{o}\right)$ | 400 V |
| Switching Frequency $\left(f_{s w}\right)$ | 100 kHz |
| Dead-Time | 100 ns |
| SiC MOSFET | $\mathrm{SCT3040KL}$ |
| Leakage Inductance $\left(L_{L K}\right)$ | $2 \mu \mathrm{H}$ |
| Transformer Turns Ratio $(n)$ | 1.5 |
| ESR (100 kHz) | $40 \mathrm{~m} \Omega$ |
| Auxiliary Inductor $\left(L_{A u x}\right)$ | $(43 \mu \mathrm{H}(\mathrm{SPS}) / 8 \mu \mathrm{H}(\mathrm{MDPS}))$ |
| Ferrite Material / Core | $3 \mathrm{C} 97 /$ double EE55 |



Figure 8.9: A photo of the hardware prototype.
calibrated in the dSPACE control-desk based on the difference voltages measured with the LEM transducers and the accurate digital multimeter. Since the overall accuracy error can increase with increasing the output power, the control output power in the experiment was limited to 6 kW .

The experimental waveforms of the soft-starting process are illustrated in Figure 8.10. An initial duty cycle of $D_{\text {cycle }}=0.22$ was applied to limit the maximum inrush current to $30 \mathrm{~A}\left(I_{\text {inrush-max }}=\frac{V_{\text {in }}}{L_{r}} \Delta t\right)$. As demonstrated, during the OL-PSC period, the secondary side is operated as a diode rectifier (e.g. $V_{g s}=-2 \mathrm{~V}$ ) to charge up the output capacitance. As the output voltage reaches the $V_{p r e-1}$, the SiC MOSFETs on the secondary side are triggered by zero phase shift until $V_{p r e-2}$. As a result, the output
voltage rises smoothly, and the inrush current is therefore limited.


Figure 8.10: Main waveforms during soft-starting: inductor current (blue), output voltage (green), gate-source voltage of switch S2 (red) and Q2 (brown).

The operation waveforms of the converter using the SPS and MDPS methods at 6 kW and 1 kW are illustrated in Figure 8.11 and 8.12 respectively. As depicted, compared with the SPS method, the proposed MDPS eliminates the circulating current. Applying the SPS technique, all switches are turned-on with ZVS and turn-off hard. In contrast, applying MDPS, two switches from each full-bridge are turned-off with HS condition and the rest are turned-on and -off with ZVS or ZCS. Therefore, the switching losses will be reduced and hence the efficiency will be improved. Additionally, the current stress is significantly reduced with MDPS, in comparison with the SPS method, which results in lower conduction loss in both the switches and the magnetic components. The theoretically calculated results of the RMS current and phase-shift angle for both modulations schemes are compared with their measured values. As demonstrated in Figure 8.13, the measured results of both control schemes present a good agreement with the theoretical calculation, which verifies the derived mathematical model. The proposed MDPS control method in turn increases the overall efficiency, especially at a high power level.

Figure 8.14 provides the efficiency comparison of the whole converter using both control methods at 100 kHz . Due to the elimination of the circulation current and the achievement of the soft switching for most of the switching devices, MDPS leads to a higher efficiency. Furthermore, Figure 8.15 illustrates the loss distribution at 6 kW . Compared with SPS, the proposed MDPS reduces the total losses by $37 \%$ in this operation point.
In order to determine the losses for both methods, the turn-off current is calculated based on the


Figure 8.11: Measured operation waveforms at 6 kW and 100 kHz using a) SPS and b) MDPS techniques.
derived mathematical model and the corresponding loss is estimated using (4.42 to 4.44). The turn-off currents are calculated at different switching states according to Table 8.2.

In the same manner, the conduction losses of the SiC switches are estimated with help of the measured temperature dependency of $R_{D S o n}$ (see Figure 2.3) and the calculated RMS current. Furthermore, to breakdown the magnetic losses, the same procedure described in Section 7.4 is used. As demonstrated, applying MDPS control, the total semiconductor losses (eight switches) are $34 \%$ less than those generated with the SPS method. Moreover, eliminating the circulating current using MDPS, the losses


Figure 8.12: Measured operation waveforms at 1 kW and 100 kHz using a) SPS and b) MDPS techniques.
of the magnetic components (HFT and HFI) are $55 \%$ compared to those generated with the SPS technique.

In summary, the proposed MDPS control method was successfully implemented to control a highfrequency converter, yielding significant improvements in the total efficiency. Eliminating the circulation current as well as minimising the current stress are the main advantages of this method. Also, a soft-starting procedure was successfully implemented without additional hardware. In addition, due to the reduction of the $R_{D S o n}$ as well as the achievement of the ZVZCS for most of the devices,


Figure 8.13: Comparison between the theoretically calculated and measured values of a) RMS current and b) phase shift angle ( $D=\frac{\varphi}{\pi}$ )

Table 8.2: Comparison of switching state of each switch using SPS and MDPS techniques.

|  |  | SPS Technique (Figure 8.2) |  | MDPS Technique (Figure 8.5) |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Turn-on | Turn-off | Turn-on | Turn-off |
| Bridge-A | S1 | ZVS at $\mathrm{t}_{1}$ | HS at $\mathrm{t}_{3}$ | ZVS at $\mathrm{t}_{2}$ | HS at $\mathrm{t}_{4}$ |
|  | S4 | ZVS at $\mathrm{t}_{4}$ | HS at $\mathrm{t}_{6}$ | ZVS at $\mathrm{t}_{6}$ | HS at $\mathrm{t}_{8}$ |
|  | S3 | ZVS at $\mathrm{t}_{4}$ | HS at $\mathrm{t}_{6}$ | ZCS at $\mathrm{t}_{6}$ | ZCS at $\mathrm{t}_{9}$ |
|  | S4 | ZVS at $\mathrm{t}_{1}$ | HS at $\mathrm{t}_{3}$ | ZCS at $\mathrm{t}_{2}$ | ZCS at $\mathrm{t}_{5}$ |
| Bridge-B | Q1 | ZVS at $\mathrm{t}_{2}$ | HS at $\mathrm{t}_{5}$ | ZCS at $\mathrm{t}_{2}$ | ZCS at $\mathrm{t}_{5}$ |
|  | Q2 | ZVS at $\mathrm{t}_{5}$ | HS at $\mathrm{t}_{2}$ | ZCS at $\mathrm{t}_{6}$ | ZCS at $\mathrm{t}_{1}$ |
|  | Q3 | ZVS at $t_{5}$ | HS at $\mathrm{t}_{2}$ | ZVS at $\mathrm{t}_{7}+\mathrm{T}_{D}$ | HS at $\mathrm{t}_{3}$ |
|  | Q4 | ZVS at $\mathrm{t}_{2}$ | HS at $\mathrm{t}_{5}$ | ZVS at $\mathrm{t}_{3}+\mathrm{T}_{D}$ | HS at $\mathrm{t}_{7}$ |



Figure 8.14: Measured efficiency of the converter at 100 kHz using SPS and MDPS control methods.


Figure 8.15: Loss breakdown at 6 kW with SPS and MDPS techniques.
applying SiC MOSFETs improves the total efficiency of the whole converter, even at a high switching frequency, with a $98.45 \%$ peak efficiency.

## Chapter 9

## Conclusions and Future Work

### 9.1 Conclusion

In this thesis, extensive static and dynamic characterisations of the up-to-date planar and double-trench SiC MOSFETs are evaluated, showing their superior switching performances at different operating conditions.

The high switching speed aggravates the parasitic effects arising from the interaction with parasitic elements existing in the gate and power loops. Therefore, a simple mathematical model is derived to estimate the optimal external gate resistance required to obtain lower feasible switching losses, while ensuring that the oscillation in the gate-source voltage is reduced sufficiently.

In addition, the reverse recovery characteristics of the SiC MOSFETs body-diode have been investigated and evaluated. Several aspects of using the SiC MOSFETs internal diode in a high-frequency, high-power DC/DC converter are investigated, comparing the body-diodes of planar and double-trench devices. Compared to the planar technology, the reverse recovery current and charge of the trench device are only slightly dependent on the temperature, which considerably reduces the switching losses in hard-switching converters. Therefore, using an anti-parallel SBD to suppress the reverse recovery effect is not necessary.

The parallel operation of the planar MOSFETs is investigated, and the impact of parameter mismatch on the static and dynamic current sharing of the transistors is evaluated, showing that paralleling of SiC MOSFETs is feasible.

To guarantee safe operation, a simple electro-thermal model is proposed to estimate the maximum permitted switching frequency based on the thermal design of the SiC devices. Consequently, hard
and soft-switching converters were designed, and the SiC devices were characterised in continuous operation at a very high switching frequency of 1 MHz . Thereafter, the SiC MOSFETs were operated in a continuous mode in a $10 \mathrm{~kW} /(100-250) \mathrm{kHz}$ hard-switching converter, allowing for comparisons between synchronous rectification, the use of the internal diode, and the use of an external Schottky diode. The results show that the planar SiC MOSFET's body-diode worsens as the temperature increases. Therefore, the antiparallel SBD is recommended in this case to eliminate the recovery effect.

Next, an accurate analytical model of SiC MOSFET for switching loss optimisation is proposed. The analytical model exhibits quite close agreement with the measurement results of different test conditions. This has been achieved by considering the influence of the most crucial parasitic elements in both power and gate loops.
Moreover, the measured results show that the charging and discharging currents of the parasitic capacitance should be taken into consideration and cannot be neglected. Therefore, the diversion phenomenon occurring as a result of the displacement current charging and discharging the parasitic capacitances is included into the model.

In the second part of this work, a comprehensive short-circuit ruggedness evaluation focusing on different failure modes occurring in the planar and double-trench SiC devices was presented and compared. Two different failure mechanisms have been recorded. First, a thermal failure occurred after successful turn-off, where a sudden short circuit between the gate and source terminals is observed. The second failure occurs simultaneously in the gate and drain terminals. The leakage current, resulting from the high SC energy, seems to be responsible for both failure mechanisms. The design and test of two different methods for overcurrent protection are evaluated. The desaturation technique is applied to the SiC MOSFETs and compared to a second method that depends on the stray inductance of the devices. The experimental results show that both methods have the capability to clear the short-circuit current within less than 150 ns .

In the third part, the benefits of using SiC devices in the high-frequency, high-power $\mathrm{DC} / \mathrm{DC}$ converter were experimentally evaluated. The power loss model is used to predict the losses and hence determine the operating limits. With the help of the small parasitic output capacitance of the SiC devices, a ZVZCS Phase-shift Full-Bridge topology is proposed using only the parasitic leakage inductance of the transformer. This results in a lightweight, compact converter. Experimental results from a 10 kW , (100-250) kHz prototype show an efficiency of up to $98.1 \%$ for the whole converter.

In addition, a design and optimisation methodology of a high-frequency, high-power transformer is presented. Different prototypes were built based on different core materials, winding conductors, and winding arrangements. Mixing the conductors types (Litz wire and copper foil) exhibits a good electrical and thermal characteristics.

The proposed loss model is used once again to predict the losses of the dual-active-bridge converter. The benefit of mixing conductor types together with a high efficient ferrite core material (3C97) is used to redesign the transformer, resulting in a highly compact design. A modified dual-phaseshift control modulation for the optimised operation of the dual active bridge isolated bidirectional DC/DC converter is presented. The proposed modulation is experimentally compared with traditional single-phase shift control, yielding a significant improvement in efficiency. The experimental results confirm the theoretical analysis and show that the proposed control can enhance the overall converter efficiency and expand the ZVZCS range.

### 9.2 Future Work

Following this research, the following research opportunities remain for further exploration.

- The proposed analytical model can be extended by considering the physical meaning of the reverse recovery of the body-diode.
- The design of an advanced active gate driver should be prioritised, to allow for current balancing in parallel connection and an active suppression of the oscillations.
- A future work could study the impact of the repetitive short circuit capability on the failure mechanisms especially on the gate oxide reliability and leakage current.
- Another could improve the AC resistance calculation of the Litz wire and copper foil windings by considering a different winding arrangement.
- Lastly, a future work could prioritise the modelling and design of a truly effective EMI filter for high frequency, high power applications.
- Optimising the closed-loop control of the DAB including a high bandwidth sensor (widebandwidth control loops).


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## Appendix A

## Static Characteristics Measurement

## Setup

The schematic output characteristics setup is illustrated in Figure A.1.


Figure A.1: Output characteristics setup.

The drain-source voltage $\left(V_{d s}\right)$, gate-source voltage $\left(V_{g s}\right)$, and drain-source current $\left(I_{d s}\right)$ are measured with high-bandwidth meters listed in Table 3.2. The input voltage $\left(V_{i n}\right)$ is increased in steps of 200 mV while the driving pulse voltage is controlled in steps of 2 V . The case temperature is controlled up to $150{ }^{\circ} \mathrm{C}$. In order to avoid any self-heating, the turn-on pulse is limited $<4 \mu \mathrm{~s}$.

## On-State Resistance Measurement

The on-state resistance ( $R_{D S o n}$ ) is calculated directly from the output characteristics curves. The gate-source voltage is kept at a fixed voltage and the drain-source terminals are connected to a variable DC input voltage. All the measured waveforms are processed in MATLAB.

## Transfer Characteristics

In this test, the drain-source voltage is kept a constant, e.g. 10 V , and the gate-source voltage is controlled up to 20 V in steps of 2 V .

## Threshold Voltage

In this work, the threshold voltage is defined as the minimum voltage required to produce 5 mA drain-source current when the drain and gate terminals are shorted.

Furthermore, a slight variation in the fabrication process of SiC MOSFETs may lead to a variation in the device properties like threshold voltage and the on-state resistance. Therefore, to demonstrate this issue, six random samples from each device are investigated with same test conditions. Their on-state resistance and threshold voltages are evaluated, the results are summarized in Figures A. 2 and A.3. As illustrated, the SiC MOSFETs are more likely operated with a parameter mismatch.


Figure A.2: The measured On-state resistance of different samples at two different $T_{c}$ and $I_{d s}=20 \mathrm{~A}$ : (a) C2M, (b) SCH and (c) SCT.


Figure A.3: The measured threshold voltage of different samples at two different $T_{c}$ : (a) C 2 M , (b) SCH and (c) SCT.

## Appendix B

## Analytical Switching Loss Model

According to the analytical switching model described in Chapter 4, the equations at each stage can be written in state-space form:

$$
\left\{\begin{array}{l}
\dot{\boldsymbol{x}}=\boldsymbol{A} x(t)+\boldsymbol{B}  \tag{B.1}\\
x\left(t_{o}\right)=\boldsymbol{x}_{o}
\end{array}\right.
$$

Where $\boldsymbol{A}$ is a $5 \times 5$ matrix, and $\boldsymbol{B}$ is $1 \times 5$ matrix, $\boldsymbol{x}_{o}$ is $5 \times 1$ matrix includes the initial conditions. By sorting (4.3)-(4.20), the complete state-space matrices are obtained with the following state variables:
$\mathbf{x}=\left[\begin{array}{lllll}v_{d s} & i_{d s} & v_{g s} & i_{g} & v_{f}\end{array}\right]^{T}$

## * Turn-on Switching Process

A- $\quad$ Stage-A (Delay turn-on time)
$\frac{d v_{g s}}{d t}=\frac{1}{C_{i s s}} i_{g}$
$\frac{d i_{g}}{d t}=\frac{1}{a}\left[V_{d r i v e-o n}-v_{g s}-R_{G} i_{g}\right]$

$$
A=\left[\begin{array}{ccccc}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{C_{i s s}} & 0 \\
0 & 0 & -\frac{1}{a} & -\frac{R_{G}}{a} & 0 \\
0 & 0 & 0 & 0 & 0
\end{array}\right] \quad B=\left[\begin{array}{c}
0 \\
0 \\
0 \\
\frac{V_{\text {drive-on }}}{a} \\
0
\end{array}\right]
$$

B- Stage-B (Current Rising-Time)

$$
\begin{align*}
\frac{d v_{d s}}{d t} & =\frac{1}{L}\left[i_{d s}-g_{f s}\left(v_{g s}-V_{t h}\right)+\frac{C_{g d}}{C_{i s s}} i_{g}\right] \\
\frac{d i_{d s}}{d t} & =\frac{1}{b}\left[v_{d s}-V_{\text {in }}-V_{f}+\frac{L_{G S}}{L_{G}+L_{G S}} V_{d r i v e-o n}-\frac{L_{G S}}{L_{G}+L_{G S}} v_{g s}-\frac{L_{G S}}{L_{G}+L_{G S}} R_{G} i_{g}\right] \\
\frac{d v_{g s}}{d t} & =\frac{1}{h}\left[\frac{C_{g d}}{C_{\text {oss }}} i_{d s}-\frac{C_{g d}}{C_{\text {oss }}} g_{f s}\left(v_{g s}-V_{t h}\right)+i_{g}\right] \\
\frac{d i_{g}}{d t} & =\frac{1}{d}\left[V_{\text {drive-on }}-v_{g s}-R_{G} i_{g}-\frac{L_{G S}}{L_{\text {loop }}} V_{\text {in }}-\frac{L_{G S}}{L_{\text {loop }}} V_{f}+\frac{L_{G S}}{L_{\text {loop }}} v_{d s}\right] \tag{B.3}
\end{align*}
$$

$A=\left[\begin{array}{ccccc}0 & \frac{1}{L} & -\frac{g_{f s}}{L} & \frac{C_{g d}}{L C_{\text {iss }}} & 0 \\ \frac{1}{b} & 0 & -\frac{L_{G S}}{b\left(L_{G}+L_{G S}\right)} & -\frac{L_{S S} R_{G}}{b\left(L_{G}+L_{G S}\right)} & 0 \\ 0 & \frac{C_{g d}}{h C_{\text {oss }}} & -\frac{g_{s} C_{g d}}{h C_{\text {oss }}} & \frac{1}{h} & 0 \\ \frac{L_{G S}}{d L_{\text {loop }}} & 0 & -\frac{1}{d} & -\frac{R_{G}}{d} & 0 \\ 0 & 0 & 0 & 0 & 0\end{array}\right] \quad B=\left[\begin{array}{c}\frac{g_{f s}}{L} V_{t h} \\ \frac{1}{b}\left[\frac{L_{G S}}{L_{G}+L_{G S}} V_{\text {drive }}-o n-V_{\text {in }}-V_{f}\right] \\ \frac{g_{f S} C_{g d}}{h C_{\text {oss }}} V_{\text {th }} \\ \frac{1}{d L_{\text {loop }}}\left[L_{\text {loop }} V_{\text {drive }-o n}-L_{G S} V_{\text {in }}-L_{G S} V_{f}\right] \\ 0\end{array}\right]$

C- $\quad$ Stage-C (Voltage Falling-Time)

$$
\begin{align*}
\frac{d v_{d s}}{d t} & =\frac{1}{L}\left[i_{d s}-g_{f s}\left(v_{g s}-V_{t h}\right)+\frac{C_{g d}}{C_{i s s}} i_{g}\right] \\
\frac{d i_{d s}}{d t} & =\frac{1}{b}\left[v_{d s}-V_{i n}+v_{f}+\frac{L_{G S}}{L_{G}+L_{G S}} V_{d r i v e-o n}-\frac{L_{G S}}{L_{G}+L_{G S}} v_{g s}-\frac{L_{G S}}{L_{G}+L_{G S}} R_{G} i_{g}\right] \\
\frac{d v_{g s}}{d t} & =\frac{1}{h}\left[\frac{C_{g d}}{C_{\text {oss }}} i_{d s}-\frac{C_{g d}}{C_{\text {oss }}} g_{f s}\left(v_{g s}-V_{t h}\right)+i_{g}\right] \\
\frac{d i_{g}}{d t} & =\frac{1}{d}\left[V_{\text {drive }-o n}-v_{g s}-R_{G} i_{g}-\frac{L_{G S}}{L_{\text {loop }}} V_{\text {in }}+\frac{L_{G S}}{L_{\text {loop }}} v_{f}+\frac{L_{G S}}{L_{\text {loop }}} v_{d s}\right] \\
\frac{d v_{f}}{d t} & =\frac{1}{C_{\text {oss }-F W}+C_{L}}\left(i_{d s}-I_{o}\right) \tag{B.4}
\end{align*}
$$

$A=\left[\begin{array}{ccccc}0 & \frac{1}{L} & -\frac{g_{f s}}{L} & \frac{C_{g d}}{L C_{\text {iss }}} & 0 \\ \frac{1}{b} & 0 & -\frac{L_{G S}}{b\left(L_{G}+L_{G S}\right)} & -\frac{L_{G S}}{b\left(L_{G}+L_{G S}\right.} R_{G} & \frac{1}{b} \\ 0 & \frac{C_{g d}}{h C_{\text {oss }}} & -\frac{C_{g d}}{h C_{\text {oss }}} g_{f s} & \frac{1}{h} & 0 \\ \frac{L_{G S}}{d L_{\text {loop }}} & 0 & -\frac{1}{d} & -\frac{R_{G}}{d} & \frac{L_{G S}}{d L_{\text {loop }}} \\ 0 & \frac{1}{C_{\text {oss }}-F W+C_{L}} & 0 & 0 & 0\end{array}\right] \quad B=\left[\begin{array}{c}\frac{g_{f s}}{L} V_{t h} \\ \frac{1}{b}\left[\frac{L_{G S}}{L_{G}+L_{G S}} V_{\text {drive }}-o n\right. \\ \frac{C_{g d}}{h C_{\text {oss }}} g_{f s} V_{\text {th }} \\ \frac{1}{d L_{\text {loop }}}\left[L_{\text {looo }} V_{\text {drive }}\right] \\ -\frac{I_{o n}}{C_{\text {oss }}-L_{G W}+C_{L}}\end{array}\right]$

D- $\quad$ Stage-D (Gate Voltage Rising Period)

$$
\begin{align*}
\frac{d v_{d s}}{d t} & =\frac{1}{L}\left[i_{d s}-\frac{v_{d s}}{R_{D S o n}}+\frac{C_{g d}}{C_{i s s}} i_{g}\right] \\
\frac{d i_{d s}}{d t} & =\frac{1}{b}\left[v_{d s}-V_{i n}+v_{f}+\frac{L_{G S}}{L_{G}+L_{G S}} V_{d r i v e-o n}-\frac{L_{G S}}{L_{G}+L_{G S}} v_{g s}-\frac{L_{G S}}{L_{G}+L_{G S}} R_{G} i_{g}\right] \\
\frac{d v_{g s}}{d t} & =\frac{1}{h}\left[\frac{C_{g d}}{C_{\text {oss }}} i_{d s}-\frac{C_{g d}}{C_{o s s}} \frac{v_{d s}}{R_{D S o n}}+i_{g}\right] \\
\frac{d i_{g}}{d t} & =\frac{1}{d}\left[V_{d r i v e-o n}-v_{g s}-R_{G} i_{g}-\frac{L_{G S}}{L_{\text {loop }}} V_{i n}+\frac{L_{G S}}{L_{\text {loop }}} v_{f}+\frac{L_{G S}}{L_{\text {loop }}} v_{d s}\right] \\
\frac{d v_{f}}{d t} & =\frac{1}{C_{\text {oss-FW }}+C_{L}}\left(i_{d s}-I_{o}\right) \tag{B.5}
\end{align*}
$$

$$
A=\left[\begin{array}{ccccc}
-\frac{1}{L R_{D S o n}} & \frac{1}{L} & 0 & \frac{C_{g d}}{L C_{\text {iss }}} & 0 \\
\frac{1}{b} & 0 & -\frac{L_{G S}}{b\left(L_{G}+L_{G S}\right)} & -\frac{L_{S}}{b\left(L_{G}+L_{G S}\right)} R_{G} & \frac{1}{b} \\
-\frac{C_{g d}}{h C_{\text {oss }} R_{\text {Soon }}} & \frac{C_{g d}}{h C_{\text {Coss }}} & 0 & \frac{1}{h} & 0 \\
\frac{L_{G S}}{d L_{\text {loop }}} & 0 & -\frac{1}{d} & -\frac{R_{G}}{d} & \frac{L_{G S}}{d L_{\text {loop }}} \\
0 & \frac{1}{C_{\text {oss }}-F W}+C_{L} & 0 & 0 & 0
\end{array}\right] \quad B=\left[\begin{array}{c}
0 \\
\frac{1}{b}\left[\frac{L_{G S}}{L_{G}+L_{G S}} V_{d r i v e-o n}-V_{\text {in }}\right] \\
0 \\
\frac{1}{d L_{\text {loop }}}\left[L_{\text {loop }} V_{\text {drive-on }}-L_{G S} V_{\text {in }}\right] \\
-\frac{I_{o}}{C_{\text {oss }}-F W+C_{L}}
\end{array}\right]
$$

* Turn-off Switching Process

A- $\quad$ Stage-A (delay turn-off time)

$$
\begin{align*}
\frac{d v_{g s}}{d t} & =\frac{1}{C_{i s s}} i_{g} \\
\frac{d i_{g}}{d t} & =\frac{1}{a}\left[V_{d r i v e-o f f}-v_{g s}-R_{G} i_{g}\right] \tag{B.6}
\end{align*}
$$

$$
A=\left[\begin{array}{ccccc}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{C_{i s s}} & 0 \\
0 & 0 & -\frac{1}{a} & -\frac{R_{G}}{a} & 0 \\
0 & 0 & 0 & 0 & 0
\end{array}\right] \quad B=\left[\begin{array}{c}
0 \\
0 \\
0 \\
\frac{V_{\text {drive-off }}}{a} \\
0
\end{array}\right]
$$

B- $\quad$ Stage-B (Voltage Rising Time)

$$
\begin{align*}
\frac{d v_{d s}}{d t} & =\frac{1}{L}\left[i_{d s}-g_{f s}\left(v_{g s}-V_{t h}\right)+\frac{C_{g d}}{C_{i s s}} i_{g}\right] \\
\frac{d i_{d s}}{d t} & =\frac{1}{b}\left[v_{d s}-V_{i n}+v_{f}+\frac{L_{G S}}{L_{G}+L_{G S}} V_{d r i v e-o f f}-\frac{L_{G S}}{L_{G}+L_{G S}} v_{g s}-\frac{L_{G S}}{L_{G}+L_{G S}} R_{G} i_{g}\right] \\
\frac{d v_{g s}}{d t} & =\frac{1}{h}\left[\frac{C_{g d}}{C_{o s s}} i_{d s}-\frac{C_{g d}}{C_{o s s}} g_{f s}\left(v_{g s}-V_{t h}\right)+i_{g}\right] \\
\frac{d i_{g}}{d t} & =\frac{1}{d}\left[V_{d r i v e-o f f}-v_{g s}-R_{G} i_{g}-\frac{L_{G S}}{L_{l o o p}} V_{\text {in }}+\frac{L_{G S}}{L_{l o o p}} v_{f}+\frac{L_{G S}}{L_{l o o p}} v_{d s}\right] \\
\frac{d v_{f}}{d t} & =\frac{1}{C_{o s s-F W}+C_{L}}\left(i_{d s}-I_{o}\right) \tag{B.7}
\end{align*}
$$

$A=\left[\begin{array}{ccccc}0 & \frac{1}{L} & -\frac{g_{f s}}{L} & \frac{C_{g d}}{L C_{i s s}} & 0 \\ \frac{1}{b} & 0 & -\frac{L_{G S}}{b\left(L_{G}+L_{G S}\right)} & -\frac{L_{G S} R_{G}}{b\left(L_{G}+L_{G S}\right)} & \frac{1}{b} \\ 0 & \frac{C_{g d}}{h C_{o s s}} & -\frac{C_{g d}}{h C_{o s s}} g_{f s} & \frac{1}{h} & 0 \\ \frac{L_{G S}}{d L_{\text {loop }}} & 0 & -\frac{1}{d} & -\frac{R_{G}}{d} & \frac{L_{G S}}{d L_{\text {loop }}} \\ 0 & \frac{1}{C_{\text {oss }-F W}+C_{L}} & 0 & 0 & 0\end{array}\right] \quad B=\left[\begin{array}{c}\frac{g_{f s}}{L} V_{t h} \\ \frac{1}{b}\left[\frac{L_{G S}}{L_{G}+L_{G S}} V_{d r i v e-o f f}-V_{\text {in }}\right] \\ \frac{C_{g d}}{h C_{\text {oss }}} g_{f s} V_{t h} \\ \frac{1}{d L_{\text {loop }}}\left[L_{\text {loop }} V_{d r i v e-o f f}-L_{G S} V_{\text {in }}\right] \\ -\frac{I_{o}}{C_{\text {oss }-F W}+C_{L}}\end{array}\right]$

## C- $\quad$ Stage-C (Current Falling Time)

$$
\begin{align*}
\frac{d v_{d s}}{d t} & =\frac{1}{L}\left[i_{d s}-g_{f s}\left(v_{g s}-V_{t h}\right)+\frac{C_{g d}}{C_{i s s}} i_{g}\right] \\
\frac{d i_{d s}}{d t} & =\frac{1}{b}\left[v_{d s}-V_{i n}-V_{f}+\frac{L_{G S}}{L_{G}+L_{G S}} V_{d r i v e-o f f}-\frac{L_{G S}}{L_{G}+L_{G S}} v_{g s}-\frac{L_{G S}}{L_{G}+L_{G S}} R_{G} i_{g}\right] \\
\frac{d v_{g s}}{d t} & =\frac{1}{h}\left[\frac{C_{g d}}{C_{o s s}} i_{d s}-\frac{C_{g d}}{C_{o s s}} g_{f s}\left(v_{g s}-V_{t h}\right)+i_{g}\right] \\
\frac{d i_{g}}{d t} & =\frac{1}{d}\left[V_{d r i v e-o f f}-v_{g s}-R_{G} i_{g}-\frac{L_{G S}}{L_{l o o p}} V_{\text {in }}-\frac{L_{G S}}{L_{l o o p}} V_{f}+\frac{L_{G S}}{L_{l o o p}} v_{d s}\right] \tag{B.8}
\end{align*}
$$

$A=\left[\begin{array}{ccccc}0 & \frac{1}{L} & -\frac{g_{f s}}{L} & \frac{C_{g d}}{L C_{\text {iss }}} & 0 \\ \frac{1}{b} & 0 & -\frac{L_{G S}}{b\left(L_{G}+L_{G S}\right)} & -\frac{L_{C S} R_{G}}{b\left(L_{G}+L_{G S}\right)} & 0 \\ 0 & \frac{C_{g d}}{h C_{\text {oss }}} & -\frac{C_{g d}}{h C_{\text {oss }}} g_{f s} & \frac{1}{h} & 0 \\ \frac{L_{G S}}{d L_{\text {loop }}} & 0 & -\frac{1}{d} & -\frac{R_{G}}{d} & 0 \\ 0 & 0 & 0 & 0 & 0\end{array}\right] \quad B=\left[\begin{array}{c}\frac{g_{f s}}{L} V_{t h} \\ \frac{1}{b}\left[\frac{L_{G S}}{L_{G}+L_{G S}} V_{\text {drive-off }}-V_{\text {in }}-V_{f}\right] \\ \frac{C_{g d}}{h C_{\text {oss }}} g_{f s} V_{\text {th }} \\ \frac{1}{d L_{\text {loop }}}\left[L_{\text {loop }} V_{\text {drive-off }}-L_{G S} V_{\text {in }}-L_{G S} V_{f}\right] \\ 0\end{array}\right]$

D- Stage-D (Gate Voltage Falling Period)

$$
\begin{align*}
\frac{d v_{d s}}{d t} & =\frac{1}{L}\left[i_{d s}+\frac{C_{g d}}{C_{i s s}} i_{g}\right] \\
\frac{d i_{d s}}{d t} & =\frac{1}{b}\left[v_{d s}-V_{\text {in }}-V_{f}+\frac{L_{G S}}{L_{G}+L_{G S}} V_{d r i v e-o f f}-\frac{L_{G S}}{L_{G}+L_{G S}} v_{g s}-\frac{L_{G S}}{L_{G}+L_{G S}} R_{G} i_{g}\right] \\
\frac{d v_{g s}}{d t} & =\frac{1}{h}\left[i_{g}+\frac{C_{g d}}{C_{\text {oss }}} i_{d s}\right] \\
\frac{d i_{g}}{d t} & =\frac{1}{d}\left[V_{\text {drive }-o f f}-v_{g s}-R_{G} i_{g}-\frac{L_{G S}}{L_{\text {loop }}} V_{\text {in }}-\frac{L_{G S}}{L_{\text {loop }}} V_{f}+\frac{L_{G S}}{L_{\text {loop }}} v_{d s}\right] \tag{B.9}
\end{align*}
$$

$$
A=\left[\begin{array}{ccccc}
0 & \frac{1}{L} & 0 & \frac{C_{g d}}{L C_{\text {iss }}} & 0 \\
\frac{1}{b} & 0 & -\frac{L_{G S}}{b\left(L_{G}+L_{G S}\right)} & -\frac{L_{G S} R_{G}}{b\left(L_{G}+L_{G S}\right)} & 0 \\
0 & \frac{C_{g d}}{h C_{\text {oss }}} & 0 & \frac{1}{h} & 0 \\
\frac{L_{G S}}{d L_{\text {loop }}} & 0 & -\frac{1}{d} & -\frac{R_{G}}{d} & 0 \\
0 & 0 & 0 & 0 & 0
\end{array}\right] \quad B=\left[\begin{array}{c}
0 \\
\frac{1}{b}\left[\frac{L_{G S}}{L_{G}+L_{G S}} V_{d r i v e-o f f}-V_{\text {in }}-V_{f}\right] \\
0 \\
\frac{1}{d L_{\text {loop }}}\left[L_{\text {loop }} V_{\text {drive-off }}-L_{G S} V_{\text {in }}-L_{G S} V_{f}\right] \\
0
\end{array}\right]
$$

where:
$a=L_{G}+L_{G S}$
$b=\frac{L_{G S}^{2}}{L_{G}+L_{G S}}-L_{\text {loop }}$
$d=L_{G}+L_{G S}-\frac{L_{G S}^{2}}{L_{\text {Loop }}}$
$h=C_{i s s}-\frac{C_{g d}^{2}}{C_{\text {oss }}}$
$L=C_{o s s}-\frac{C_{g d}^{2}}{C_{\text {iss }}}$

## Appendix C

## Thermal Performance of HFT

## Prototypes

Following, the thermal performance of the HFT prototypes described in Chapter Seven.


Figure C.1: Hot spot temperature of sample-1 at a) $10 \mathrm{~kW}, 100 \mathrm{kHz}$ and b) $8 \mathrm{~kW}, 200 \mathrm{kHz}$


Figure C.2: Hot spot temperature of sample-A at a) $10 \mathrm{~kW}, 100 \mathrm{kHz}$ and b) $8 \mathrm{~kW}, 200 \mathrm{kHz}$


Figure C.3: Hot spot temperature of sample-B at a) $10 \mathrm{~kW}, 100 \mathrm{kHz}$ and b) $8 \mathrm{~kW}, 200 \mathrm{kHz}$


Figure C.4: Hot spot temperature of sample-C at a) $10 \mathrm{~kW}, 100 \mathrm{kHz}$ and b) $8 \mathrm{~kW}, 200 \mathrm{kHz}$


Figure C.5: Hot spot temperature of sample-D at a) $10 \mathrm{~kW}, 100 \mathrm{kHz}$ and b) $8 \mathrm{~kW}, 200 \mathrm{kHz}$


[^0]:    ${ }^{1}(10-90) \%$ rise and fall times from drain-source current and drain-source voltage are used in the calculations.

[^1]:    ${ }^{1}$ This Chapter is based on Reference [23].

[^2]:    ${ }^{1}$ This Chapter is based on Reference [102].

