

Front-Side Interface Engineering for Liquid-Phase Crystallized Silicon Solar Cells on Glass

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Abstract

Liquid-phase crystallization (LPC) is a process technology to fabricate thin ($< 30 \mu\text{m}$) crystalline silicon layers on glass substrates. To this end, as-deposited amorphous or nano-crystalline silicon layers on glass are molten locally with a high energy density source (laser or electron beam). Subsequently, the silicon cools down and crystallizes. Resulting layers exhibit grains with a length of several centimetres and a width of several millimetres. Solar cells based on LPC-Si are characterized by an open-circuit voltage of up to 661 mV which demonstrates the high electrical quality of the material. Layer stacks composed of e.g. silicon oxide (SiO_x) and silicon nitride (SiN_x) (for example $\text{SiO}_x/\text{SiN}_x/\text{SiO}_x$, short O/N/O) deposited by means of plasma-enhanced chemical vapor deposition (PECVD) are sandwiched between the glass and the silicon. These so called interlayers are crucial for the quality of LPC-Si material, because they are responsible for adhesion of the silicon on the substrate, light coupling into the thin absorber layer, blocking of impurities from the glass and for the passivation of the LPC-Si. In this thesis the focus lies on the development and characterization of the interlayer stack whereby the PECVD method is chosen to profit from the high degree of flexibility of deposition parameters.

Samples with interlayer stacks prepared by PECVD are commonly annealed prior to the crystallization process which is unwanted due to increased manufacturing time. Annealing reduces the amount of hydrogen which otherwise would lead to blistering of the silicon during the crystallization. However, a systematic correlation of interlayer properties such as the hydrogen content and the adhesion properties was not performed prior to this thesis. Therefore, in this thesis it is studied in detail which interlayer properties are crucial to achieve adhesion during the crystallization process. The aim is to develop an interlayer stack using PECVD for LPC-Si solar cells that enables adhesion without extended annealing steps prior to the crystallization process.

Several glass/interlayer/LPC-Si samples are crystallized and sorted with respect to dewetting and adhesion. Corresponding dielectric layers are deposited as single layers on silicon wafers and characterized with regard to their chemical composition and hydrogen content using Fourier-transform infrared spectroscopy (FTIR). The refractive index is determined with spectral

ellipsometry and the residual stress is calculated using Stoney's equation. It is found that the SiN_x layer plays a crucial role for adhesion and that a nitrogen-rich SiN_x layer results in adhesion without annealing the samples prior to crystallization. The concentration of bonded hydrogen does not seem to be crucial for adhesion. However, the bonding configuration of hydrogen is critical. If hydrogen is bonded to nitrogen only, adhesion is observed. If hydrogen is also bonded to silicon atoms, then the layers delaminate. A tensile residual stress in the SiN_x layer of 400 MPa or lower does not hinder adhesion while silicon delaminates when the stress is greater than 400 MPa (tensile or compressive).

It is difficult to determinate the passivation quality at the interface between the interlayer stack and the absorber because the glass substrate blocks one side of the interface of interest. In addition, the thin silicon layers result in a low signal-to-noise ratio making common techniques such as QSSPC not applicable. In this thesis, the passivation mechanism at the buried interface between the interlayer and the LPC-Si is investigated by means of capacitance-voltage measurements that allow the determination of the defect state density at the interface (D_{it}) and the fixed charge density in the interlayer ($Q_{IL,eff}$). To this end, metal-insulator-semiconductor structures are developed that are compatible with capacitance-voltage measurements. A gate electrode made of molybdenum is sandwiched between glass and interlayer. Molybdenum does not hinder the crystallization of the silicon absorber because it has a similar thermal expansion coefficient as compared to glass and silicon.

It is demonstrated that the passivation quality provided by an O/N and O/N/O interlayer is similar to published results obtained with silicon wafers. In particular, the O/N stack results in a high fixed charge density $> 10^{12} \text{ cm}^{-2}$ which is dedicated to the nitrogen-rich character of the SiN_x layer. When the O/N/O stack is used, the fixed charge density and the defect state density is reduced by one order of magnitude in comparison to the O/N stack. Furthermore, it is found that the surface recombination velocity, which is calculated based on the obtained D_{it} and $Q_{IL,eff}$ values using the Shockley-Read-Hall model, is around 10 cm/s and dominated by field-effect passivation for both stacks. Simulated results demonstrate that such a low recombination velocity results in bulk-limited solar cells. Accordingly, solar cells, which differ in the interlayer stack only, this is, O/N and O/N/O, have similar cell parameters.

It is discovered that the passivation quality at the interface is very sensitive to a variation in the fixed charge density, which is dedicated to the high defect state density above $10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$. Furthermore, there is evidence for thermal instabilities of the SiN_x when in direct contact to the LPC-Si. This potentially reduces the cells performance. When a SiO_x is introduced between SiN_x and LPC-Si its thickness influences the passivation quality, this is, with increasing SiO_x thickness D_{it} and $Q_{IL,eff}$ decrease. Thus, in order to profit from field-effect passivation, the SiO_x thickness should be as thin as possible. The deposition rate of the employed SiO_x layer is

1.1 nm/s and thus, it is challenging to deposit an ultra-thin layer and provide stable deposition conditions. The reduction of the deposition rate by a reduction of the silane flow rate led to a reduced cell performance.

In order to realize a capping layer for the SiN_x with well-controllable thickness, plasma-oxidation of the SiN_x layer is tested. Transmission electron microscopy was used to demonstrate that a 10-min long dinitrogen monoxide (N_2O) plasma converted roughly 9 nm of the SiN_x surface into a silicon oxynitride layer. Implementation of such an O/N/ON stack in LPC-Si solar cells with interdigitated back contacts resulted in a record conversion efficiency of 14.2 %.

It is concluded that the further improvement of LPC-Si solar cells on glass should focus on the improvement of the LPC-Si bulk quality. In the framework of this thesis, preliminary experiments are conducted that aim for an improved bulk quality by using high temperature treatments and phosphorous diffusion gettering. The latter is frequently used to improve the bulk quality of multi-crystalline silicon wafers. Photoluminescence images as well as measured open-circuit voltages of test solar cells demonstrate an increase in material quality with respect to reference samples. Further experiments should continue this research.

Zusammenfassung

Die Flüssigphasenkristallisation ist eine Methode zur Herstellung dünner ($< 30 \mu\text{m}$) kristalliner Siliziumschichten auf Glassubstraten. Amorphe oder nanokristalline Siliziumschichten werden auf einem Substrat deponiert und mithilfe eines hochenergetischen Strahls geschmolzen. Im Anschluss kühlt das Silizium ab und kristallisiert aus. Die hergestellten Schichten sind durch große Körner mit einer Länge von mehreren Zentimetern und einer Breite im Millimeterbereich ausgezeichnet. Solarzellen, deren Absorber aus flüssigphasenkristallisierten Siliziumschichten bestehen, erreichen offene Klemmspannungen von 661 mV, wodurch die hohe Materialqualität des Siliziums aufgezeigt wird.

Dielektrische Schichten, welche sich zwischen dem Glassubstrat und dem Absorber befinden, beeinflussen die Materialqualität signifikant. Diese Schichten, welche als Zwischenschichten bezeichnet werden, erfüllen mehrere Aufgaben: sie ermöglichen die Haftung der Siliziumschichten während des Kristallisationsprozesses, sie dienen der Lichteinkopplung in den Absorber, sie verhindern die Diffusion von Verunreinigungen aus dem Glass und sie passivieren die vergrabene Grenzschicht des Siliziums. Schichtstapel bestehend aus Siliziumoxid, Siliziumnitrid, Siliziumoxinitrid, Aluminiumoxid und weiteren Materialien werden erfolgreich als Zwischenschichten in flüssigphasenkristallisierten Dünnschichtsolarzellen eingesetzt.

Zu Beginn dieser Arbeit gab es noch nicht geklärte Fragen in Bezug auf die Zwischenschichten. Zum Beispiel war nicht geklärt, warum manche Zwischenschichten die Haftung des Absorbers ermöglichen und andere hingegen nicht. Es wurde vermutet, dass ein hoher Wasserstoffgehalt in den Zwischenschichten zum Ablösen der Schicht während des Kristallisationsprozesses führt. Deswegen wurden Schichten, welche mithilfe der plasma-unterstützten Gasphasenabscheidung (PECVD) hergestellt wurden, vor dem Kristallisationsprozess ausgeheizt. Jedoch fehlten systematische Untersuchungen zur Korrelation des Wasserstoffgehalts und der Hafteigenschaften. Dieser Frage wird im Rahmen der vorliegenden Arbeit nachgegangen. Es wird nachgewiesen, dass die Siliziumnitrid Schicht einen großen Einfluss auf die Hafteigenschaften hat und dass eine stickstoffreiche Schicht mit einem Brechungsindex von 1.89 eine Haftung ohne vorhergehenden Ausheizschritt ermöglicht. Die Konzentration an gebundenem Wasserstoff scheint eine untergeordnete Rolle zu spielen, wohingegen die Bindungsart des Wasserstoffs wichtig ist. Ist

der Wasserstoff mit einem Siliziumatom verbunden, führt das zu einer Ablösung der Schicht. Wenn der Wasserstoff an ein Stickstoffatom gebunden ist, hält die Schicht. Eine Zugspannung von 400 MPa oder weniger verhindert die Haftung nicht.

Eine weitere offene Frage in Bezug auf die Zwischenschichten in Siliziumsolarzellen betrifft deren Passiviereigenschaften. Dazu zählt die Frage, inwieweit sich Konzepte, welche mit dielektrischen Passivierschichten auf Siliziumwafern beobachtet wurden, auf die vergrabene Grenzfläche in flüssigphasenkristallisierten Solarzellen übertragen lassen. Die Ermittlung der Lebensdauer und damit der Passivierqualität mithilfe von Methoden, welche standardmäßig für Siliziumwafer eingesetzt werden, ist in Siliziumdünnschichtsolarzellen mit hoher Defektdichte nicht möglich. Um die Passivierqualität an der vergrabenen Grenzfläche zu bestimmen, werden Metall-Isolator-Halbleiter Strukturen auf Basis von flüssigphasenkristallisierten Siliziumschichten auf Glas entwickelt, welche Untersuchungen mittels Kapazitäts-Spannungsmessungen ermöglichen. Dazu wird eine Gate-Elektrode aus Molybdän zwischen Glassubstrat und Zwischenschicht eingefügt. Molybdän ermöglicht eine erfolgreiche Kristallisation, da es einen ähnlichen thermischen Ausdehnungskoeffizienten hat wie das Silizium und das Glassubstrat.

Die Untersuchungen zeigen, dass die Passiviereigenschaften von Siliziumoxid und Siliziumnitrid ähnlich sind zu denen, welche aus der Literatur für Siliziumwafer bekannt sind. Insbesondere weist das stickstoffreiche Siliziumnitrid in Kontakt mit dem Silizium eine hohe Dichte fester Ladungen $> 10^{12} \text{ cm}^{-2}$ auf. Wird das Siliziumoxid als Passivierschicht verwendet, ist die Dichte fester Ladungen um eine Größenordnung reduziert. Die Grenzfläche mit Siliziumoxid zeichnet sich durch eine reduzierte Grenzflächen-Defektdichte aus. Das Shockley-Read-Hall Modell wird verwendet, um aus der ermittelten Grenzflächen-Defektdichte und der Dichte fester Ladungen eine Oberflächenrekombinationsgeschwindigkeit zu berechnen. Die Ergebnisse zeigen, dass die Feldeffektpassivierung einen großen Einfluss auf die Passivierqualität hat, sowohl im Falle einer Siliziumnitrid als auch einer Siliziumoxid Passivierschicht. Die Oberflächenrekombinationsgeschwindigkeit liegt bei etwa 10 cm/s. Simulationsergebnisse demonstrieren, dass im Falle einer solchen Passivierqualität Solarzelleneigenschaften durch die Qualität des Absorbers dominiert sind. Entsprechend der Erwartung, zeigen Solarzellen mit Siliziumnitrid oder Siliziumoxid Passivierschicht ein sehr ähnliches Verhalten.

In der Literatur wurde gezeigt, dass die Dicke der Siliziumoxid Passivierschicht zwischen der Siliziumnitrid Schicht und dem Siliziumabsorber einen Einfluss auf die Solarzellenparameter hat. Um von den positiven Ladungen im Siliziumnitrid zu profitieren und gleichzeitig eine geringe Defektdichte zu realisieren, wird die Oberfläche der Siliziumnitrid Schicht mithilfe eines Distickstoffmonoxid (N_2O) oxidiert. Detaillierte Untersuchungen des Grenzflächenbereichs mithilfe von Elektronenmikroskopie demonstrieren die Bildung einer etwa 9 nm dünnen

Siliziumoxinitrid Schicht angrenzend an den Siliziumabsorber. Solarzellen, die auf dem entwickelten Schichtstapel mit plasma-oxidierter Siliziumnitrid Schicht beruhen, weisen einen Rekordwirkungsgrad von 14.2 % auf. Auf Basis der vorliegenden Ergebnisse ist deutlich, dass die weitere Steigerung des Wirkungsgrades durch die Verbesserung der Qualität des Siliziumabsorbers als auch durch die Verbesserung der Qualität der rückseitigen Grenzfläche erreicht wird.

Im Rahmen dieser Arbeit werden Vorversuche unternommen, um die Qualität des Absorbers zu steigern. Dazu wird die Methode des Phosphor-Getterns, welche standardmäßig für die Verbesserung von multi-kristallinen Siliziumwafern eingesetzt wird, getestet. Mithilfe von Lumineszenzmessungen als auch durch Solarzellenparameter können Verbesserungen der Materialqualität im Vergleich zu Referenzproben gezeigt werden. Diese sollten in weiteren Untersuchungen konkretisiert werden.

CHAPTER 1

Introduction

The relevance of research on photovoltaics must be seen in the context of today's global energy system. The energy demand of human kind increased drastically with the age of industrialization that began in the late 18th century (figure 1.1) [1–3]. Today, around 80 % of the energy demand is satisfied by fossil fuels such as coal, oil and gas [2,3]. The combustion of fossil fuels represents by far the largest source of anthropogenic greenhouse gas emissions (about 70 %) [2]. Greenhouse gases in the atmosphere promote global warming which has severe and irreversible impacts across the world [4].

On the other hand, every year around 10^{18} kWh of radiative energy hit the earth, which is orders of magnitude higher than the primary energy consumption on earth (figure 1.1, $\approx 1.5 \times 10^{14}$ kWh in 2015). Several technologies are used to convert this renewable form of energy directly (solar cells, solar thermal collectors) or indirectly (wind turbines, biomass reactors) into electrical, thermal or chemical energy with reduced greenhouse gas emissions as compared to combustion engines.

Among these low-carbon technologies, the photovoltaic technology has several advantages [5]: fast project development and capacity build-up possible, high level of modularity which enables flexibility in terms of size and location of power plants as well as noiseless and reliable, low maintenance operation without on-site emissions. The cumulative global installed photovoltaic capacity is around 300 GW_p [6,7], which is about 1.3 % of the global power generation [6]. Although the share of photovoltaics is still low, its market is growing fast (40 % between 2010 and 2016 [6]) and the technology is seen as a major pillar in the future energy system based on renewable energies [8].

To date, around 93 % of commercially available solar cells are based on crystalline silicon wafers [6]. Silicon is not only abundant, non toxic, highly stable and durable, but it can also

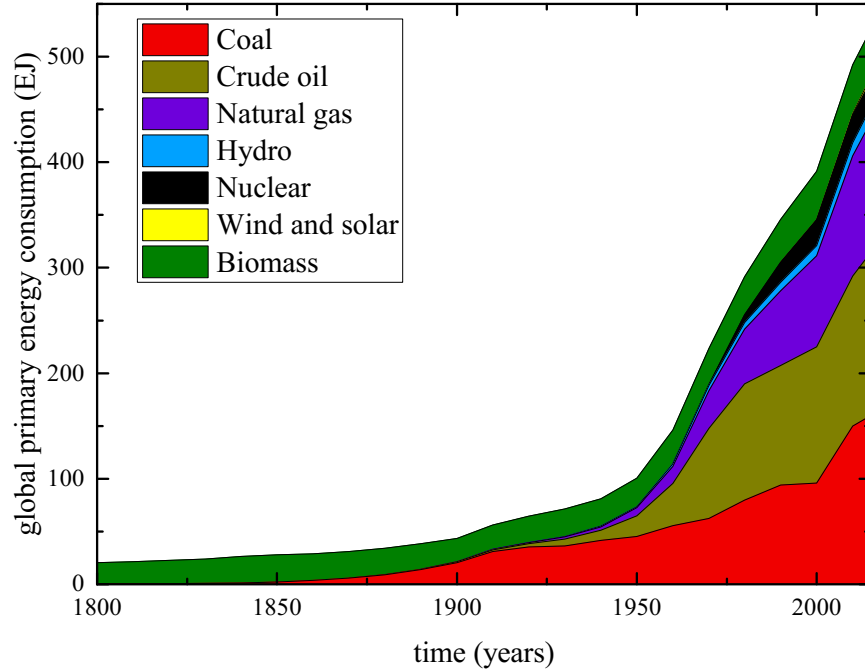


Figure 1.1: Evolution of global primary energy consumption shown as absolute contributions by different energy sources. Data taken from [3].

be fabricated into high-performance solar cells using methods that were developed within the last decades. The current record efficiency of solar cells based on high-quality mono-crystalline silicon wafers is 26.7 % [9]. When cheaper multi-crystalline wafers are used, 21.9 % is achieved [10].

Around 40 % of the overall prize of a solar module is attributed to the silicon material and the wafer manufacturing [11]. In order to reduce the cost of a module, new sawing technologies are developed that aim to reduce the amount of silicon that is lost during the sawing of the ingot into wafers (kerf losses). For example, using a diamond wire instead of a slurry enables the reduction of kerf losses from around 130 μm to about 100 μm per wafer. However, it is predicted that kerf losses still amount to 60 μm in 2027 [11]. The amount of silicon material per wafer is also reduced by thinning the silicon wafers. However, the reduction of the wafer thickness is limited to about 140 μm due to handling and sawing constraints (figure 1.2) [11].

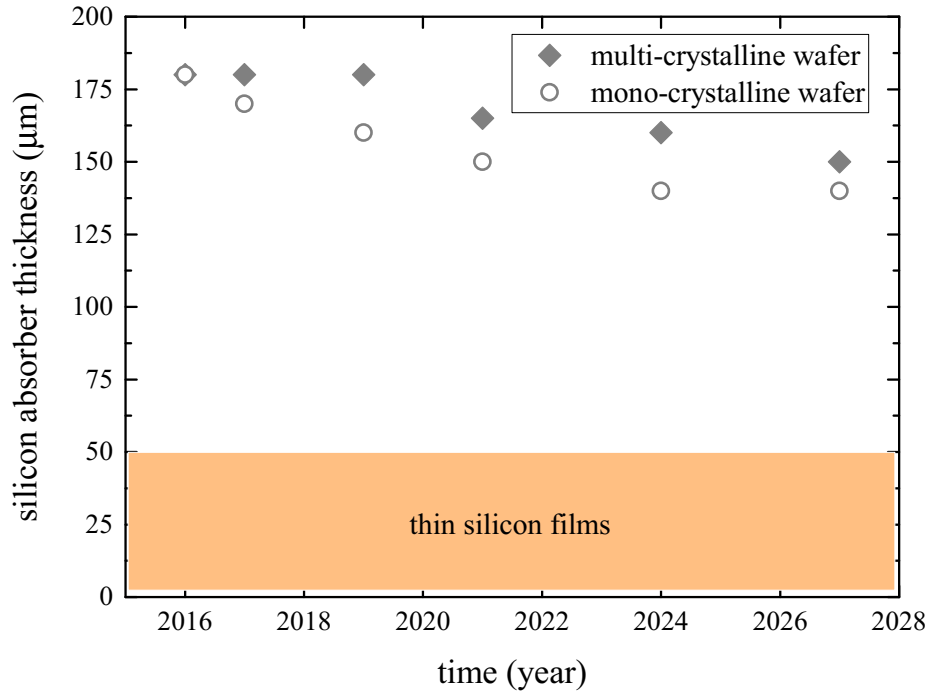


Figure 1.2: Predicted trend for minimum as-cut wafer thickness for mass production of crystalline silicon solar cells and modules. Data taken from [11]. Thin film technologies use absorber thicknesses below approximately 50 μm .

Alternative approaches to realize thin silicon films are desired that overcome the drawbacks observed for the silicon wafer technology, but without any loss in performance. Several approaches are described in the next section.

1.1 Approaches to fabricate thin silicon films

One approach to realize thin silicon absorbers is the layer transfer technique by which pores are etched into a silicon wafer, followed by epitaxial growth of mono-crystalline silicon with tunable thickness between 5 to 50 μm and subsequent lift-off of the epitaxial layer [12, 13]. By using this method, an efficiency of 19 % was demonstrated on basis of a 43 μm thin crystalline silicon solar cell [12]. An epitaxial silicon layer can be bonded to a glass substrate for mechanical support and high quality mono-crystalline silicon layers with a thickness of only 5.5 μm were demonstrated [14].

Thin silicon layers can be deposited directly on top of a substrate such as glass. When the plasma-enhanced chemical vapor deposition (PECVD) method is used for the deposition, as-

grown silicon layers have an amorphous matrix. These amorphous hydrogenated silicon (*a*-Si:H) layers are characterized by a high absorption coefficient and thus, from this perspective, *a*-Si:H layers are well suited as absorber layers. However, the material suffers from a high number of defect states in the band gap (tail states) as well as from a degradation of the cell performance which is explained by the Staebler-Wronski effect [15]. The stabilized record conversion efficiency of solar cells with an *a*-Si:H absorber is 10.1 % [16]. The efficiency can be increased by using micro-crystalline hydrogenated silicon (μ c-Si:H) or a combination of *a*-Si:H and μ c-Si:H as absorber layers. A triple stack of *a*-Si:H/ μ c-Si:H/ μ c-Si:H results in an efficiency of 14.0 % [17].

The open-circuit voltage of solar cells is influenced by the grain size, if the grain size is smaller than the absorber thickness [18,19]. Therefore, it is desirable to increase the crystallographic quality of as-grown silicon layers.

Annealing as-grown silicon layers on glass substrates at around 600 °C for several hours results in thin crystalline silicon layers with grain sizes of a few μ m [20,21]. This approach is called solid-phase crystallization (SPC). CSG Solar AG presented a SPC solar module with an open-circuit voltage of 492 mV and an efficiency of 10.4 % [20]. However, the material has a high density of intragrain defects and despite strong efforts to improve SPC material using treatments such as defect annealing [22], the open-circuit voltage could not be increased above around 500 mV.

Another process by which thin crystalline silicon films can be prepared is called metal induced layer exchange (MILC). The silicon film is deposited on top of a substrate coated with an oxidized aluminium layer (substrate/oxidized aluminium/as-grown silicon). Annealing the stack for one to four hours below the temperature at which the silicon and the aluminium form an eutectic (577 °C) initiates a layer exchange (substrate/crystallized silicon/aluminium) and in parallel the crystallization of the silicon [23,24]. The aluminium, which is now on top of the crystallized silicon, can be removed easily using wet chemical etching. The crystallized silicon exhibits grain sizes between 10 to 100 μ m [23,24]. However, the layers are not appropriate as absorber layers in solar cells, because they are highly p-doped ($\approx 10^{18} \text{ cm}^{-3}$) due to the aluminium [25]. Instead, the silicon layers can be used as high quality seed layers for a subsequent epitaxial thickening to fabricate the active layer for solar cells [26]. Using chemical vapour deposition at 1130 °C for the epitaxial growth, thin film crystalline silicon layers with grain sizes between 5 to 20 μ m are realized and solar cells with an open-circuit voltage of 534 mV [26] and an energy conversion efficiency of 8.5 % [27] are demonstrated.

As-deposited silicon layers on top of a substrate can be converted into crystalline silicon films by liquifying the silicon locally (zone-melting recrystallization (ZMR)). Using silicon films prepared with the ZMR process as seed layer for a subsequent epitaxial growth, grains with

several centimetres in length are obtained. Solar cells based on absorbers prepared with the ZMR process with an open-circuit voltage of 570 mV and a conversion efficiency of around 16 % are realized [28,29]. However, heat sources with low energy density are used to liquify the silicon and pre-heating temperatures of about 1300 °C are needed to obtain appropriate scanning speeds in the cms^{-1} range [30–32]. These high temperatures are not compatible with glass substrates.

The pre-heating temperature can be reduced significantly to about 500 °C when heat sources with a high energy density such as electron or laser beams are employed. Using these heat sources with scanning speeds in the cms^{-1} range for the liquid phase crystallization (LPC) of as-grown silicon films on glass substrates results in grain sizes that are similar to multi-crystalline silicon wafers, this is, several centimetres in length and millimetres in width (figure 1.3) [33].

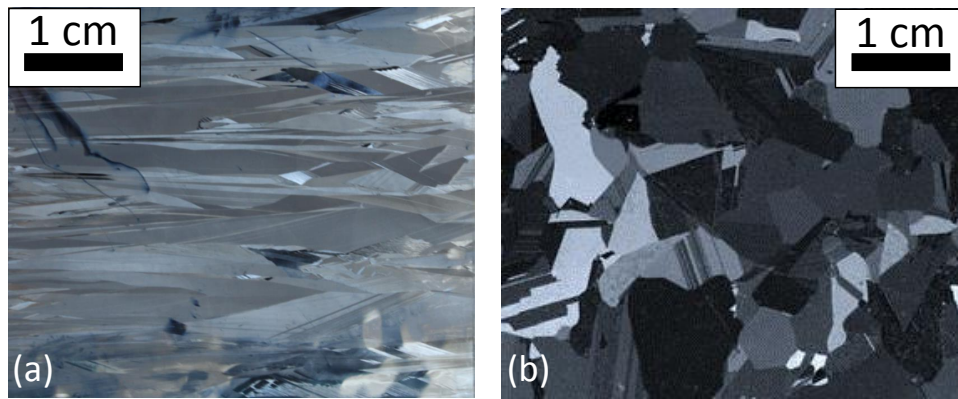


Figure 1.3: Comparison of grain size of (a) a thin LPC-Si layer on a glass substrate and (b) a multi-crystalline silicon wafer (photographs top view).

The electronic quality of LPC-Si layers is exceptional which is demonstrated by an open-circuit voltage of 661 mV [34], which is approaching the record open-circuit voltage obtained with a solar cell based on a multi-crystalline silicon wafer (674 mV) [10].

In the following section, solar cells based on LPC-Si absorbers on glass substrates are introduced briefly. The crucial role of dielectric layers between the glass and the LPC-Si absorbers is highlighted.

1.2 LPC-Si solar cells and role of interlayer stack

In LPC-Si solar cells on glass substrates, around 5 to 30 μm thin liquid-phase crystallized silicon layers are used as absorber layers. Several methods are employed to contact the absorber:

FrontERA [35], point contacts [36] and interdigitated back contacts (IBC) [37]. For all of them, the majority and minority charge carrier contacts are located on the same side of the silicon, because the other side of the absorber is covered by the glass substrate. Aside from the FrontERA concept, contacting schemes are designed for superstrate illumination only, i.e. illumination from the glass side. Figure 1.4 displays a sketch of a typical solar cell with IBC contacts, which is illuminated in superstrate configuration.

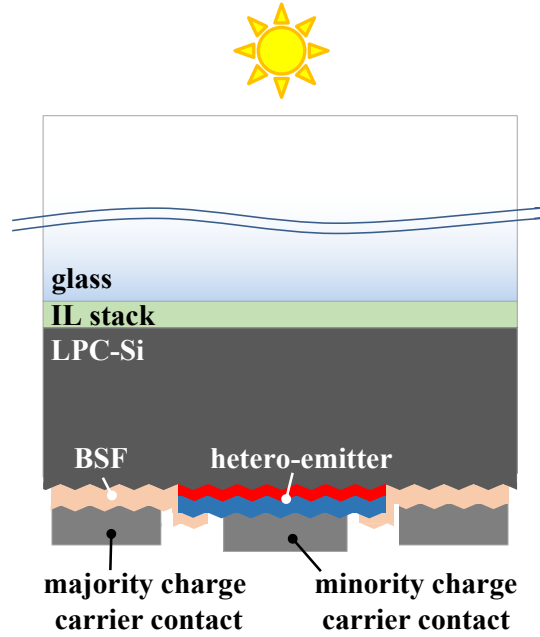


Figure 1.4: Sketch of the cross section of a typical LPC-Si solar cell on a glass substrate with IBC hetero-junction contacts. The back surface field (BSF) passivates the majority charge carrier contact, while the a -Si:H layers in the hetero-emitter passivate the minority charge carrier contact. The interlayer (IL) stack consists of dielectric layers that passivate the front-side of the absorber and also serve other purposes as discussed in the text. The IL stack is crucial for the performance of LPC-Si solar cells on glass.

Dielectric layers sandwiched between the glass substrate and the LPC-Si absorber (called interlayers (ILs)) have a major influence on the LPC-Si material quality, because they serve different purposes [38–40].

A suitable interlayer avoids diffusion of impurities such as metals and oxygen from the glass substrate into the silicon absorber and it should not release impurities by itself. It increases light coupling into the absorber and it passivates the silicon, namely the buried silicon surface towards the glass substrate. A sufficient surface passivation is especially important for thin absorbers due to the high surface-to-volume ratio [41]. Additionally, the interlayer could be used as doping source for the absorber [33]. A fundamental requirement for the interlayer is to maintain chemical and mechanical stability at the melting point of silicon (1414 °C [42]).

Materials that can potentially be used for the interlayer are all carbides, nitrides and oxides [43, p. 45]. In LPC-Si solar cells, amorphous silicon carbide (SiC_x), amorphous aluminium oxide (AlO_x), amorphous hydrogenated silicon oxide (SiO_x), amorphous hydrogenated silicon nitride (SiN_x), amorphous hydrogenated silicon oxinitride (SiO_xN_y) and refractory metals such as tungsten (W) and molybdenum (Mo) were tested. The melting point of all these materials in their stoichiometric form is above the melting point of silicon and thus, the films do not decompose at 1414 °C. It was observed, that SiC_x is a good wetting promoter [33,39], but a poor diffusion barrier and it is highly absorptive [44,45]. SiO_x was found to be very effective in preventing impurity diffusion and furthermore, in passivating the buried LPC-Si surface [38]. SiO_xN_y was also found to be suitable as passivation layer [46]. SiN_x was found to be suitable as anti-reflection coating (ARC) in the superstrate devices [39]. However, SiN_x in direct contact to the silicon absorber was found to be thermally unstable reducing the performance of the cells [45,47].

The best cell performance was achieved when the aforementioned materials were combined in interlayer stacks such as $\text{SiN}_x/\text{SiO}_x/\text{SiO}_x\text{N}_y$ [36,40,46,48–50] (abbreviated as N/O/ON in this work) or $\text{SiO}_x/\text{SiN}_x/\text{SiO}_x$ [38,39,47,51–54] (abbreviated as O/N/O in this work). In these stacks, each layer serves a specific purpose. In the O/N/O stack, the SiO_x layer adjacent to the glass has a thickness of around 200 nm to hinder impurity diffusion, the around 70 nm thin SiN_x film also prevents impurity diffusion and it acts as anti-reflection coating and the roughly 20 nm thin SiO_x layer in contact with the LPC-Si is responsible for passivation. In the N/O/ON stack, the 20 nm thin SiN_x on top of the glass was used as wetting promoter, the 100 nm thin SiO_x layer is the diffusion barrier and the passivation is provided by the SiO_xN_y layer. The dielectric layers were either deposited with reactive RF-magnetron sputtering [38,39,47,51,52] or with PECVD [36,40,46,48–50,53]. To sum up, different materials and different deposition techniques were employed to prepare interlayer stacks for LPC-Si solar cells.

The PECVD method has the advantage, that layer properties can be tuned over a wide range due to the flexibility of the process conditions. However, when the PECVD method was employed for the deposition of the interlayer stack, samples were annealed for up to 24 h before the silicon was crystallized [39,40,46]. The idea was to reduce the hydrogen concentration in the layers which would otherwise prevent the formation of homogeneous crystalline silicon layers due to the explosive effusion of hydrogen during the crystallization process [39,40,46]. However, such a long annealing treatment is unwanted, because it increases manufacturing time of the solar cells. Therefore, it is important to understand in detail which interlayer properties are crucial to achieve adhesion in order to develop an interlayer stack that enables crystallization without extended annealing treatments. Such a systematic study was not done before this thesis.

In LPC-Si solar cells, it is difficult to determine the quality of the absorber and of the interface between the interlayer stack and the absorber. For example, the quasi-steady state photo-conductivity (QSSPC) technique [41,55,56], which is commonly used to determine the bulk lifetime and the surface quality of silicon wafers [57], cannot be applied in LPC-Si material, because the absorber layers are too thin to get a sufficient signal-to-noise ratio. In addition, the measurement signal is reduced due to depletion region modulation effects [58,59]. Also, the high number of bulk defects restrict the reliable determination of the bulk lifetime using the QSSPC technique [60]. The interface between the interlayer stack and the LPC-Si absorber is difficult to access experimentally, for example with capacitance-voltage (C-V) measurements, since the glass substrate blocks one side of the interface of interest.

In order to determine the quality of the absorber and of the interface between the interlayer stack and the absorber, simulations with AFORS-HET, ASPIN3 and TCAD SentaurusTM are applied to model measured solar cell results [19,34,46,53,61,62]. An insight into specific passivation mechanisms was not achieved with these methods. In particular, the defect state density at the interface and the fixed charge density in the interlayer was not known. It was discovered, that the passivation quality at the buried interface is increased upon a post-deposition hydrogen plasma treatment at elevated temperatures [40,46]. However, the microscopic origin of the improvement remained unclear.

1.3 Objectives in this thesis

The objective in this thesis is to address the aforementioned aspects related to the interlayer and the interface between the interlayer and the silicon by clarifying the questions listed below.

1. Which interlayer properties are crucial for adhesion of the silicon layer during the crystallization process? The aim is to develop an interlayer stack for LPC-Si solar cells which enables adhesion without an extended annealing step prior to the crystallization process.
2. What is the character of the passivation at the buried IL/LPC-Si interface? Is the passivation quality dominated by field-effect passivation or by chemical passivation or both? What is the defect state density at the interface? What is the effective fixed charge density in the interlayer? How does the post-deposition hydrogen plasma treatment at elevated temperature influence the passivation mechanism at the interface?
3. How do the developed interlayers perform in fully functional solar cell devices? How does the front-side interface with the developed interlayer stack influence the solar cell performance?

In chapters 2 and 3, the sample preparation and sample characterization is discussed, respectively. Chapter 4 describes the theoretical background of basic concepts that are used in subsequent chapters. In chapter 5, the adhesion properties are addressed. Developed dielectric layers are tested for their optical properties. In chapter 6, the electrical properties of LPC-Si samples are addressed, whereby the passivation quality at the front-side interface as well as LPC-Si solar cells are studied. In chapter 7, approaches are introduced that aim to improve the LPC-Si bulk quality.

CHAPTER 2

Sample Preparation

In this chapter, the methods are described that are used to prepare the samples that are studied in the framework of this thesis.

In section 2.1, the plasma-enhanced chemical vapor deposition (PECVD) method is explained in detail, because it is used to deposit several layers for LPC-Si solar cells, among others, it is used for the development of the interlayer stack.

Section 2.2 describes the post-deposition hydrogen plasma treatment, which is standardly used to passivate defects in LPC-Si. Its effect on the IL/LPC-Si interface quality is examined in more detail in section 6.2.

In sections 2.3 and 2.4, the preparation of LPC-Si solar cells on glass as well as of metal-insulator-semiconductor (MIS) structures based on LPC-Si on glass is presented in detail, respectively. Both structures, LPC-Si solar cells as well as MIS structures, are used to evaluate the passivation quality at the front-side interface between the interlayer stack and the absorber.

Aside from the preparation of LPC-Si-on-glass samples and MIS structures dielectric layers are deposited with a thickness between 150 and 350 nm on double-side polished Czochralski silicon (Cz-Si) wafers with a low conductivity and a thickness between 300 and 350 μm . The single layers are characterized with respect to their stoichiometry, chemical composition and residual stress as described in section 3.2. These layer properties are correlated with the adhesion properties of glass/IL/LPC-Si stacks as well as with passivation properties at the interface between the interlayer and the silicon absorber.

2.1 Plasma enhanced chemical vapour deposition (PECVD)

In order to fabricate silicon hetero-junction LPC-Si solar cells as described in section 2.3, plasma-enhanced chemical vapor deposition (PECVD) is employed to deposit various layers such as the amorphous emitter layers. In this thesis, the PECVD method is selected for the development of the interlayer stack for LPC-Si solar cells because the method offers a high degree of flexibility with respect to layer properties due to multi-fold process parameters.

This section is dedicated to the fundamentals of the PECVD technique focussing on the parallel plate reactor, which is the most common PECVD reactor [43, p. 108-109] and which was used in the framework of this thesis. Figure 2.1 displays (a) a scheme of the PECVD reactor and gas supply and (b) a photograph of the PECVD chamber used for the deposition of the dielectric films ("PC1" in the Von Ardenne CS400PS cluster system, figure 2.3 (b) and (c)).

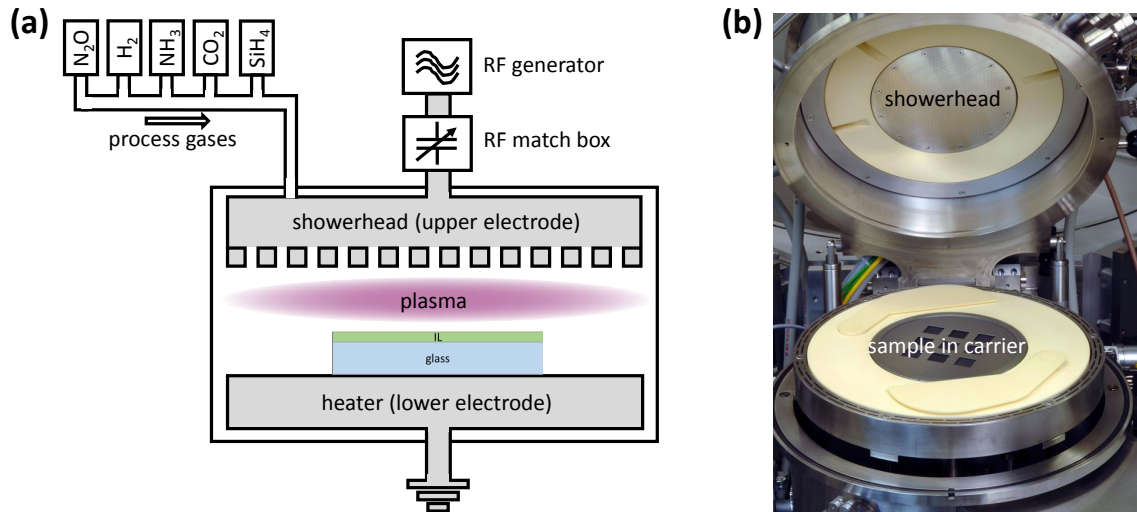


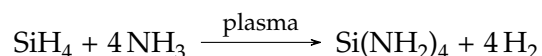
Figure 2.1: PECVD chamber: (a) Scheme of the process chamber with PECVD reactor and gas supply. Only a selection of gases are indicated. The sample rests on a carrier on the lower electrode. After [63]. (b) Photograph of the PECVD chamber used for the deposition of dielectric films.

As depicted in figure 2.1 (a), the PECVD vacuum chamber contains a lower and an upper electrode facing each other. The lower electrode is grounded while the upper electrode is connected to a radio-frequency (RF) match box containing capacitors and a RF generator. The top electrode has holes (called showerhead) through which process gases can enter the chamber.

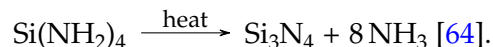
During the deposition process, the substrate to be coated, for example a silicon wafer or a glass, rests on a carrier on the lower electrode. Process gases such as monosilane (SiH_4), ammonia (NH_3), nitrous oxide (N_2O), carbon dioxide (CO_2) or hydrogen (H_2) are fed into the chamber through the showerhead. A RF-signal with a frequency typically between a few kHz and several GHz (in this thesis, 13.56 MHz is used) is applied to the upper electrode which results in the dissociation of the process gas molecules into electrons, positively charged ions, radicals and molecular fragments which form the plasma. The match box matches the impedance of the plasma output with the resistance of the generator to ensure stable plasma conditions. Some of the excited particles return to equilibrium upon spontaneous radiative emission which leads to a characteristic plasma color. Other particles adsorb on the surface of the substrate and react chemically, forming a solid film.

In PECVD processes electric energy is employed to dissociate process gas molecules. In comparison, in thermal chemical vapour deposition (CVD) processes without plasma, the energy to break the bonds is supplied by high temperatures of up to 1200 °C [43, p. 108-109]. The lower deposition temperature in PECVD processes, which can be even close to ambient, is essential for many applications where thermal CVD temperatures would damage the device being fabricated, for example solar cells with *a*-Si:H emitter layers. In PECVD processes the substrate is typically also heated to elevated temperatures depending on the specific film requirements to enhance the surface diffusion in order to support adhesion and density of the deposited film.

Exemplary, one possible chemical pathway for the formation of stoichiometric silicon nitride (Si_3N_4) from a NH_3/SiH_4 mixture is described, which occurs by the dissociation of gas molecules



followed by the surface condensation reaction



The volatile NH_3 molecules returns to the plasma.

A PECVD film is not generally stoichiometric and thus, one typically writes, for example, SiN_x and SiO_x instead of Si_3N_4 and SiO_2 [64].

Due to manifold deposition parameters (composition of gases, RF power, temperature, pressure, distance between electrodes) the PECVD technique can be used to deposit a variety of materials with tunable properties.

2.2 Post-deposition hydrogen plasma treatment (HPT)

In this section, the post-deposition hydrogen plasma treatment (HPT) is described. It is a standard process step in the manufacturing chain of LPC-Si solar cells and it is well documented, that the performance of LPC-Si solar cells on glass is improved strongly when the crystallized samples experience the post-deposition hydrogen plasma treatment [40,46,61]. Its impact on the interface between the interlayer stack and the LPC-Si absorber is studied in section 6.2.

For the treatment, the samples are introduced to a vacuum chamber ("PC5" in figure 2.3) and heated up by halogen lamps, which are mounted below the samples facing the glass substrate. When the desired plateau heater temperature (in this work, 400 or 600 °C) is reached, a direct high-frequency (13.56 MHz) plasma is ignited. The standard process conditions are a process pressure of 2.5 mbar, a RF-power of 50 W and a hydrogen gas flow rate of 50 sccm. After the desired process time (in this work, 15 or 30 min), the heaters are switched off to cool the samples down while the plasma is still active avoiding hydrogen effusion which occurs at temperatures above 400 °C [40]. The plasma is turned off when the heater temperature reaches 300 °C.

In this thesis, different process durations (15 or 30 min) and temperatures (400 or 600 °C) are used. As demonstrated in figure 2.2, when the heater treatment is 400 °C or above during the process, the open-circuit voltages of test cells with 8.5 µm thin absorber layer are similar.

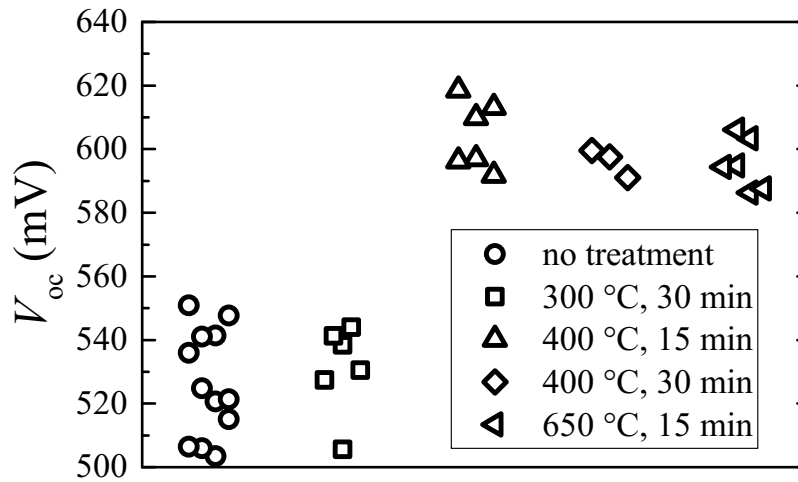


Figure 2.2: Impact of post-deposition hydrogen plasma treatments on the open-circuit voltage of LPC-Si test cells, measured with the sun simulator in superstrate configuration. The interlayer stack is composed of N/O/ON (20/100/80 nm) and the as-deposited absorber thickness is 8.5 µm. The absorbers are deposited with the PECVD method.

2.3 LPC-Si solar cells on glass

At the beginning of this thesis, LPC-Si on glass was fabricated using different approaches. The interlayer stack was deposited using reactive RF-magnetron sputtering or PECVD, the silicon was deposited by electron beam evaporation or PECVD and the crystallization was performed with an electron beam or with a laser beam in atmosphere. Despite the application of different methods, the impurity concentrations in the LPC-Si absorbers were similar [65] and obtained solar cell efficiencies were almost equal, this is, 12.1 % [48] and 11.8 % [38].

The majority of samples presented in this thesis are based on an interlayer stack that is prepared with the PECVD method, and on a silicon absorber deposited with electron beam evaporation. A laser beam in vacuum is employed for crystallization. Below, the process steps are described in detail. All silicon-based layers except of the hetero-emitter layers are deposited in the industrial-type Von Ardenne CS400PS cluster tool. Figure 2.3 (a) displays a photograph and (b) a sketch of the cluster tool, respectively.

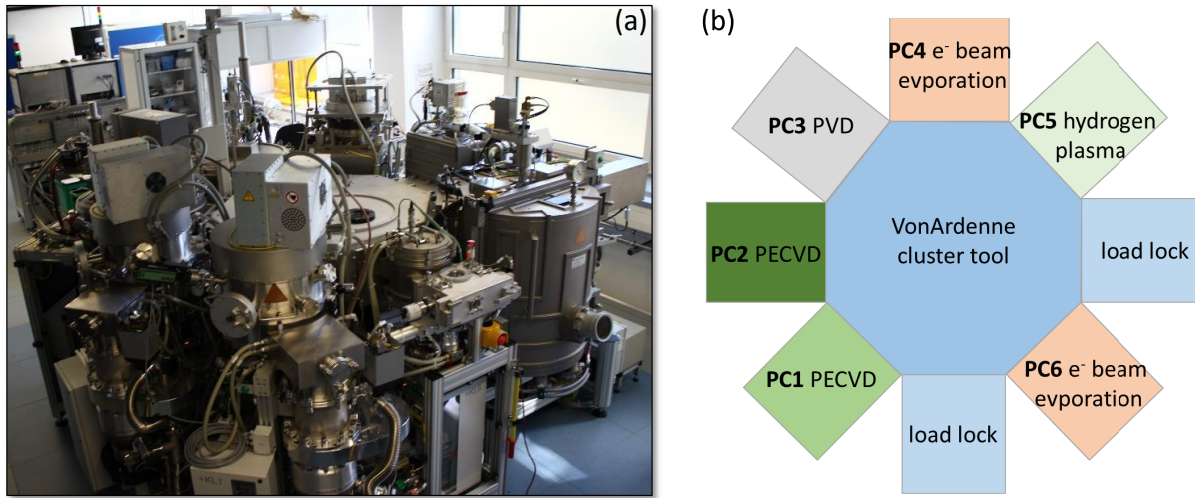


Figure 2.3: Von Ardenne CS400PS cluster tool used for the fabrication of studied LPC-Si samples on glass: (a) Photograph and (b) sketch of the process chambers.

Commercially available, 10 cm × 10 cm boro-aluminosilicate glass (Corning Eagle XG) with a thickness of 1.1 mm is used as substrate. The glass is applicable for LPC-Si processing, because it has a thermal expansion coefficient close to that of poly-crystalline silicon ($2.9 \times 10^{-6} \text{ K}^{-1}$ [66]) over a wide range of temperatures and a softening point around 1000 °C.

The interlayer is deposited using the PECVD chamber "PC1" in the Von Ardenne CS400PS cluster system. The circular electrode area is 314 cm². The base pressure is below 3×10^{-7} mbar.

During the process, the pressure is controlled with a throttle valve and typical pressures range between 0.5 and 1.5 mbar. The RF-power is between 30 W and 220 W. Gas mixtures are $\text{CO}_2/\text{N}_2\text{O}/\text{SiH}_4$ for the SiO_x layers and $\text{N}_2/\text{NH}_3/\text{SiH}_4$ for the SiN_x layers. The heater temperature is varied between 250 and 600 °C. At 600 °C heater temperature, the substrate temperature is around 100 to 150 °C below the heater temperature (figure A.1). All deposition conditions used for the dielectric films are comprised in table A.1. The majority of fabricated samples are placed on a silicon wafer carrier for the PECVD processes. However, as these samples have to be removed from the vacuum tool after the interlayer deposition in order to manually change the sample holder for the subsequent absorber deposition, the tool was modified such, that the same carrier could be used for interlayer and silicon deposition. It is flipped automatically inside the tool and a processing without vacuum break became possible.

On top of the interlayer, intrinsic silicon is deposited using electron beam evaporation at a deposition rate between 500 to 600 nm/min. The silicon absorber is capped with an around 80 nm thin n-doped amorphous hydrogenated silicon ((n) *a*-Si:H) using the PECVD method. Another PECVD chamber ("PC2", figure 2.3 (c)) than the one in which the interlayer stack is deposited is used to avoid cross-contamination. The (n) *a*-Si:H layer serves as dopant source for the absorber and thus, it is called doping layer. Finally, the sample is moved back into the chamber named "PC1" to deposit around 100 nm SiO_x . This layer serves as wetting promoter during the subsequent crystallization process (called capping layer). Prior to crystallization, the 10 cm × 10 cm glasses are cut into four 5 cm × 5 cm samples using a glass cutter.

For the crystallization of the silicon, the sample is introduced to a vacuum chamber and heated to 500 °C (700 to 710 °C heater temperature). After 5 min at 500 °C, the silicon layer is crystallized by sweeping a line-shaped continuous wave infrared diode laser (808 nm, DILAS Diodenlaser GmbH) across the surface. The scanning velocity is 3 mm/s, the optical laser power density is around 1410 W/cm² and the beam geometry is 52 mm in length and 0.3 mm in width. During the crystallization process dopant atoms from the doping layer distribute throughout the silicon [33].

In order to reduce stress in the glass, the samples are annealed at 950 °C for one minute in a rapid thermal annealing oven. The capping layer as well as around 300 nm of the crystallized silicon are removed with hydrofluoric acid (HF) and a solution based on HF, nitric acid (HNO_3), phosphoric acid (H_3PO_4) and acetic acid (CH_3COOH) (called poly-silicon etch), respectively. The samples receive a hydrogen plasma treatment as described in section 2.2. Plasma damaged surface material is removed with the poly-silicon etch solution, followed by a standard RCA cleaning procedure. Due to the wet chemical treatments, the final absorber thickness is approximately 600 nm thinner as compared to the as-grown absorber thickness.

To summarize the steps to prepare thin silicon layers on glass substrates using liquid-phase crystallization, figure 2.4 displays the steps schematically.

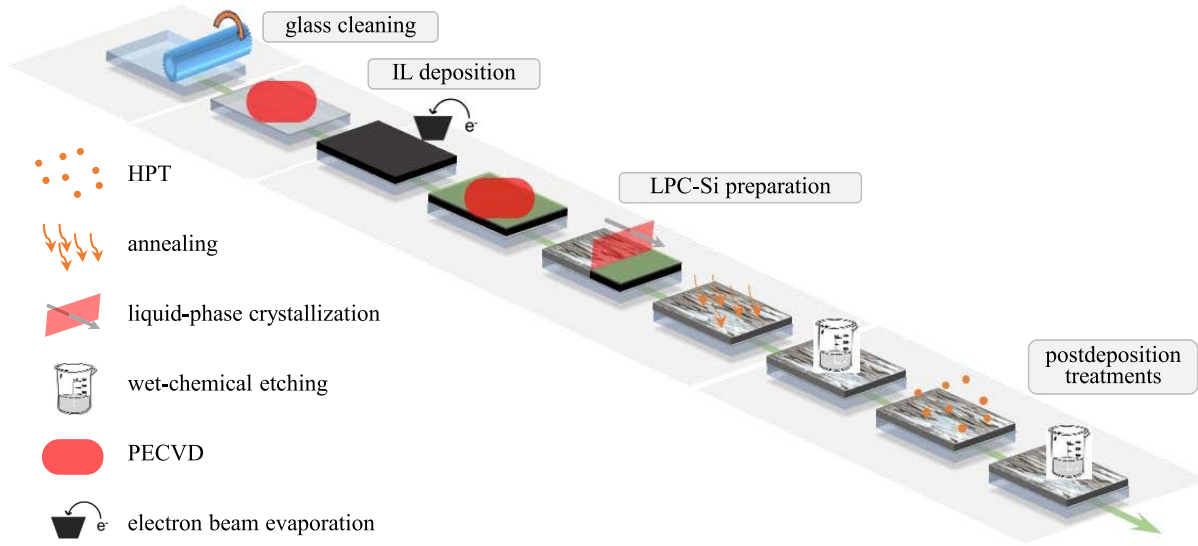


Figure 2.4: Sketch of process steps for the preparation of LPC-Si films on glass substrates. Adapted from [46].

The RCA-cleaned LPC-Si sample is coated with a hetero-junction emitter, this is, a double layer stack of intrinsic amorphous hydrogenated silicon ((i) a -Si:H) and p-doped amorphous hydrogenated silicon ((p) a -Si:H) with the PECVD method. The (i) a -Si:H layer is around 4 to 10 nm while the (p) a -Si:H layer is between 6 to 20 nm. Subsequently, 70 nm of indium-tin-oxide (ITO) are sputtered on top of the emitter. The cell areas are subsequently defined by sticking self-adhesive Kapton® dots with a diameter of 8 mm on top of the ITO. The absorber is exposed by etching the ITO and emitter layers in HF for 10 to 40 s and in poly etch solution for 1 min, respectively. The chemicals also etch the layers below the edges of the Kapton® dots. Afterwards, 30 nm of titanium (Ti) and 1 μ m of aluminium (Al) is evaporated. The direct contact between the majority and minority charge carrier contact is prohibited through the under-etching of the Kapton® dots. However, the gap between the contacts is not well-defined. Using optical microscopy a typical distance around 10 μ m or more is estimated. Finished cells are annealed below 200 °C to cure sputter damage and improve the electric contact.

Fabricated cells are test structures, so called quasi-cells or test cells, which are reliable and fast to fabricate and allow the determination of the open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), the quantum efficiency and optical losses. However, the conducting paths are long due to the simplicity of the fabrication process. In combination with the high silicon

absorber sheet resistance of typically 200 to 2000 Ω [19], the fill factor (FF) of test cells is lower as compared to more sophisticated contacting methods such as IBC cells.

The IBC cells discussed in this work are fabricated by Dr. Paul Sonntag and Dr. Cham Thi-Trinh following the procedure described in detail in [34,37,53]. For IBC cells, LPC-Si films are prepared in the same manner as for test cells (figure 2.4). Accordingly, prior to the IBC contact formation, the samples are RCA-cleaned and the hetero-emitter is deposited. Photolithography (resist: Microchemicals AZ 4533, mask aligner: MA6 SÜSS MicroTec, developer: 2.5 % metalion-free tetramethylammonium hydroxide (TMAH)) and an aqueous solution consisting of HF, HNO₃, and H₃PO₄ is used to structure the emitter. Subsequently, the samples are again RCA-cleaned and a 10 nm thin highly-doped (n^+)*a*-Si:H layer is deposited serving as back surface field (BSF). The BSF is structured using photolithography and the TMAH solution is used for developing and etching. The BSF overlaps the hetero-emitter by around 8 μm due to over-etching after patterning. 120 nm of ITO and 1 μm of silver (Ag) are sputtered on top of the samples. A third photolithography step is used to pattern the ITO/Ag and BSF layers. The silver is etch with a diluted mixture of ammonia solution (NH₄OH) and hydrogen peroxide (H₂O₂). Hydrochloric acid (HCl) (20 %) is used to remove ITO.

Final IBC structures have a total area of 0.7 cm² and an active area of 0.6 cm². The back surface field width (W_{BSF}) is 120 μm .

Figures 2.5 (a) and (b) display sketches of the cross sections of a test cell and an IBC cell, respectively. In figures (c) and (d), photographs of multiple finished test cells and IBC cells on 5 cm $\times$ 5 cm samples, respectively, are shown. The insets in both figures show one cell enlarged in top view.

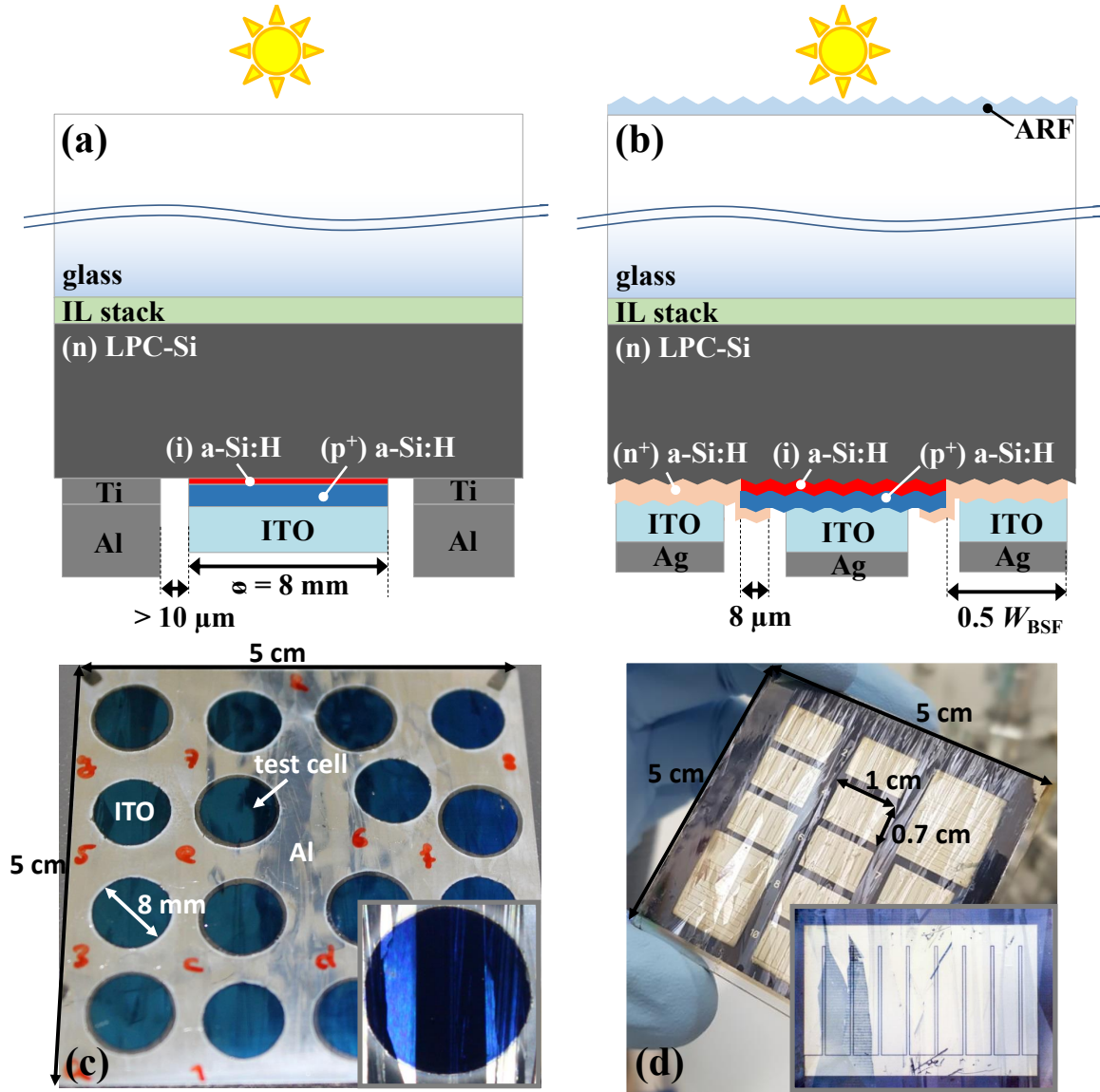


Figure 2.5: (a) and (b): Cross sections of a typical test cell and IBC cell in superstrate configuration, respectively. In (b), the anti-reflection foil (ARF) is shown which is attached to the glass side facing the light source during measurements of J - V curves. The foil reduces reflections at the air/glass interface. (c) and (d) depict corresponding photographs.

The majority of samples discussed in this thesis is fabricated following the process steps described above. A few samples are processed following a slightly different route. For these samples, borosilicate glass from SCHOTT AG (Schott Borofloat 33) with a thickness of 3.3 mm is used as substrate. The interlayer stack as well as the silicon layer are deposited with PECVD at 400 °C heater temperature and without vacuum break between interlayer and absorber deposition. The depositions are done in a AKT1600 PECVD cluster tool.

In order to effuse hydrogen from the glass/IL/LPC-Si stack, the samples are heated in nitrogen atmosphere using the following sequence: 8 hours at 450 °C - 8 hours at 550 °C - 8 hours at 650 °C.

Next, the silicon is crystallized in ambient atmosphere by sweeping a line-shaped continuous wave infrared diode laser (808 nm, Lissotschenko Mikrooptik, LIMO GmbH) with 10 mm/s across the silicon surface. Test cells are fabricated in a similar manner as described above.

2.4 Development of MIS structures based on LPC-Si on glass

For the direct analysis of the passivation quality at the IL/LPC-Si interface, the interface defect state density (D_{it}) and the effective interlayer charge density ($Q_{IL,eff}$) are crucial parameters. In order to quantify D_{it} and $Q_{IL,eff}$ of IL/LPC-Si stacks, MIS structures based on LPC-Si on glass are developed, which are compatible to $C-V$ measurements. The latter are then used to determine D_{it} and $Q_{IL,eff}$.

The MIS structure is developed with respect to three requirements: (a) the gate metal has to allow adhesion of the layers during the crystallization process, (b) the contact between the LPC-Si material and the metal serving as back contact needs to be ohmic, and (c) the area of the MIS structure needs to be well-defined.

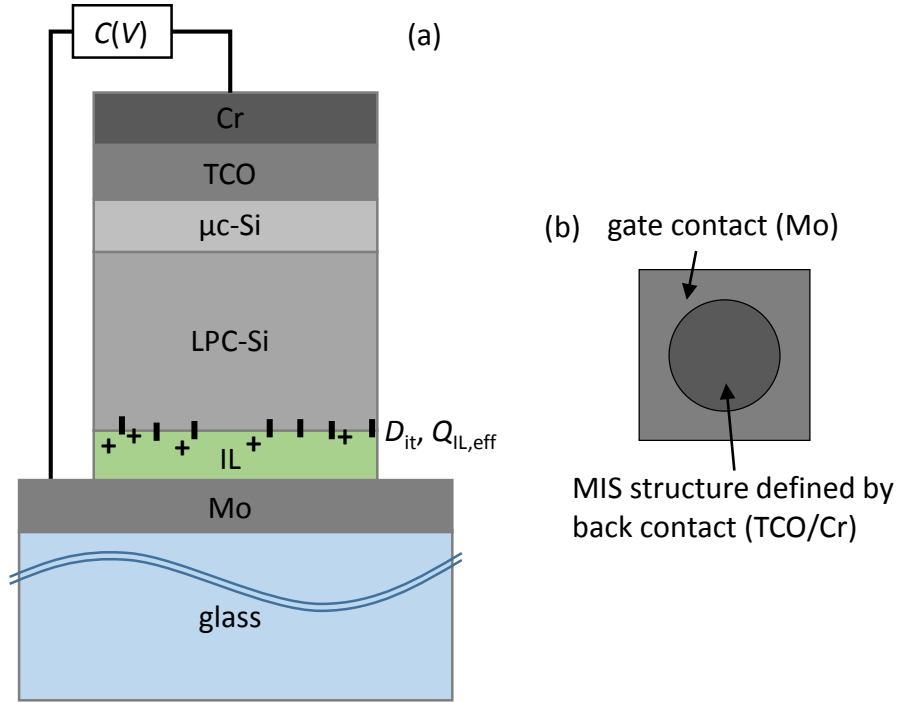


Figure 2.6: Sketch of one MIS structure based on LPC-Si on glass that allows the investigation of the passivation quality in terms of the interface defect state density (D_{it}) and the effective interlayer charge density ($Q_{IL,eff}$) at the buried interface between the interlayer (IL) stack and LPC-Si: (a) cross section and (b) top view. The electrodes for the capacitance-voltage (C-V) measurements are indicated.

Molybdenum is chosen as gate metal because it has a similar coefficient of expansion to that of both silicon and glass. The layer is deposited using magnetron sputtering. Different deposition conditions (5 μbar , 4 kW and 13 μbar , 1 kW) and molybdenum thicknesses (200 nm, 400 nm, 800 nm) are tested. The molybdenum film deposited with 13 μbar and 1 kW is less dense, the adhesion to the glass is enhanced and it is less conductive as compared to the molybdenum layer deposited at 5 μbar and 4 kW. Figure 2.7 displays photographs of the samples after crystallization, taken from the glass and the silicon side, respectively.

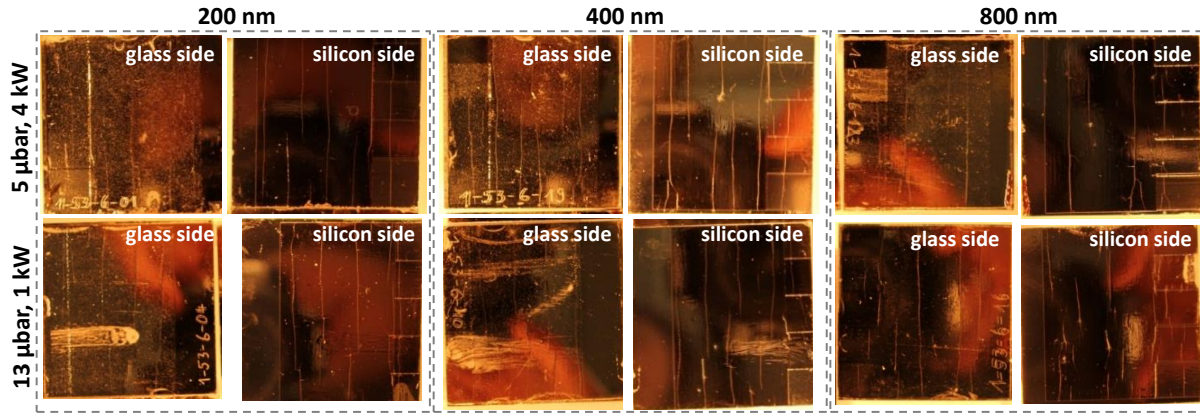


Figure 2.7: Photographs of 5 cm × 5 cm samples with different molybdenum layers, taken after crystallization from the glass and the layer side.

As demonstrated in figure 2.7, the laser-crystallization of the silicon is successful on all molybdenum films. In the final MIS structure, the 800 nm thin molybdenum layer sputtered with 5 μbar and 4 kW is used. On top of the molybdenum layer, the interlayer stack and the silicon is deposited as described in section 2.3.

As back contact, chromium (Cr) is used for p- and n-doped LPC-Si absorbers, because it is an effective etch stop for the subsequent selective etching process discussed below [67,68]. However, as evident from the current-voltage (J - V) curves shown in figures 2.8 (a) and (b), the contact does not show an ohmic behaviour for the n- and p-doped LPC-Si absorbers with a doping concentration of around $5 \times 10^{16} \text{ cm}^{-3}$ (blue dotted curves). AFORS-HET is used to simulate the band diagram at the metal/semiconductor interface [69]. In the simulated structure, the metal/semiconductor contact is selected and the work function of the metal is taken from literature as denoted in the caption of figure 2.8.

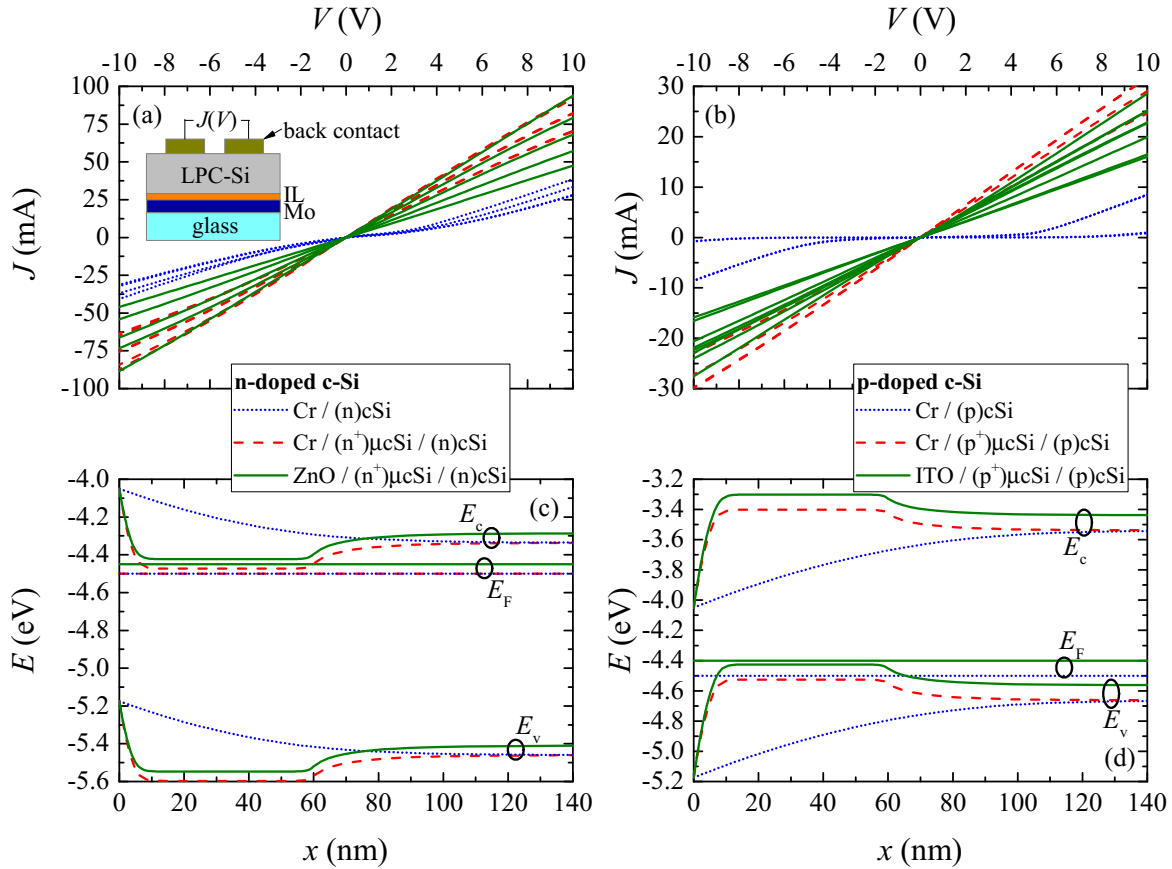


Figure 2.8: Ohmic back contact for MIS structure: (a) and (b) show multiple measured current-voltage (J - V) curves for n- and p-doped LPC-Si, respectively. The inset in (a) depicts the configuration for the measurement. (c) and (d) show simulated band structures of the back contact/LPC-Si region for n- and p-doped LPC-Si, respectively. Simulations are performed using AFORS-HET [69]. The energy E is depicted with respect to the vacuum level. Assumptions: c-Si doping = $5 \times 10^{16} \text{ cm}^{-3}$, $\mu\text{c-Si:H}$ doping = $1 \times 10^{19} \text{ cm}^{-3}$, $\mu\text{c-Si:H}$ material parameters the same as for c-Si. $\phi_{\text{Cr}} = 4.5 \text{ V}$ [70, p. 251], $\phi_{\text{ITO}} = 4.0 \text{ V}$ [71], $\phi_{\text{ZnO}} = 4.45 \text{ V}$ [72].

As can be seen in figures 2.8 (c) and (d), the energy barriers at the Cr/silicon interfaces (blue dotted curves) are about 100 nm wide and the simulated Schottky barrier heights (energy difference between the conduction and valence band edge (E_c and E_v , respectively) and the Fermi energy level (E_F)) are 0.45 eV and 0.67 eV with n-doped and p-doped silicon, respectively. Measured Schottky barrier heights at room temperature are 0.61 V and 0.50 V on n-doped and p-doped silicon, respectively [70, p. 291]. The difference between simulated and measured Schottky barrier heights could be attributed to the fact, that the simulation does not take into account Fermi-level pinning. Nonetheless, it can be concluded that the energy barrier prohibits current flow.

High doping of the silicon at the interface reduces the thickness of the barrier [70, p. 306]. The simulated band diagrams shown in figures 2.8 (c) and (d) reflect such a behaviour (green and red curves). The reduced barrier thicknesses allow the charge carriers to pass the barrier, either by thermionic field emission or by direct tunneling [70, p. 306]. As can be seen, measured J - V curves are also linear, demonstrating an ohmic contact.

In the final MIS structure, a triple stack composed of 60 nm highly-doped $\mu\text{c-Si:H}$, 70 nm transparent conducting oxide (TCO) and 150 nm Cr is used as back contact. As TCO, ITO and ZnO are used for p-doped and n-doped LPC-Si samples, respectively. The stack is deposited through a mask with 500, 700 and 900 μm circular openings.

According to the MIS structure (figure 2.6), the gate metal needs to be selectively exposed for contacting. Wet-chemical etching as well as dry-chemical etching is tested to remove the silicon and the interlayer selectively to expose the molybdenum layer.

Wet-chemical etching is performed with 25 % potassium hydroxide (KOH) and buffered oxide etch (BOE) to remove the LPC-Si and the interlayer, respectively. A double stack of 300 nm SiO_x deposited with PECVD and photo resist (AZ 4533) serves as etch mask. It is found that the SiO_x is essential for adhesion of the etch mask during the etch process. In the first test, the metal layer is omitted (LPC-Si/ SiO_x /resist). As can be seen in figure 2.9 (a), the side walls of the resulting mesa are nearly vertical and thus, the etch process seems promising, because the area of MIS structures is well defined. However, with aluminium (Al) sandwiched between the LPC-Si and the SiO_x , the etch mask does not withstand the etch process (figure 2.9 (b)). Another metal could be tested. However, it takes very long to expose the molybdenum, especially due to the ≈ 2 hours-long photolithography process, and therefore, wet-chemical etching is omitted for the fabrication of the MIS structure.

Next, dry-chemical etching is tested employing different gas mixtures based on fluorine. During the etch process, the feed gas is dissociated in the plasma by electron impact and fluorine atoms react with silicon atoms forming volatile molecules such as SiF_x [68].

It is observed, that a remote NF_3 plasma removes the silicon, the interlayer as well as the molybdenum layer within 400 s. The etch mask, this is, 1.5 μm aluminium withstands the etch process as can be seen in figure 2.9 (c). It is concluded, that this process can be used to etch the LPC-Si and the interlayer quickly. However, due to the high etch rate (around 13 nm/sec), careful optimization is required to not remove the molybdenum layer.

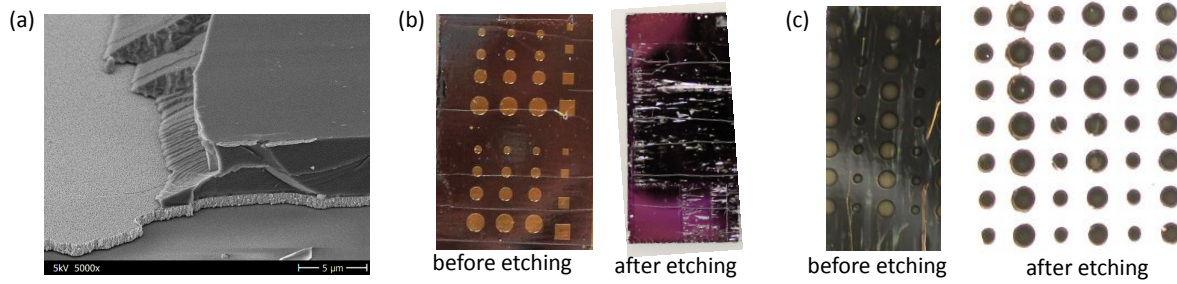


Figure 2.9: Failures observed during the development of the etch processes to expose the gate metal. Wet-chemical etching: (a) scanning electron microscopy (SEM) image of the etched border of a MIS structure without back contact (tilted view). (b) Photographs of one sample before and after etching, whereby the etch mask made of aluminium did not withstand the etch process. Dry-chemical etching: (c) Photographs of one sample before and after exposure to a NF₃ plasma. The etch mask withstood the 400 s-long etch process, but the molybdenum layer is gone.

Another dry-chemical etch method to anisotropically etch silicon with well-controllable patterns is reactive ion etching (RIE) based on SF₆ [68].

RIE is performed using a PLASMALAB 80plus RIE system from Oxford Instruments. The pressure during the process (13.3 Pa) is automatically controlled with a throttle valve. The sample rests on a silicon wafer, which is surrounded by a ring-shaped graphite plate. Prior to the etch step, a cleaning step is performed for 1 min with O₂ at 13.3 Pa. Two different gas mixtures, 14 sccm SF₆/35 sccm CHF₃ and 60 sccm SF₆/20 sccm O₂, are tested. It is found that the etch process is successful with both processes, this is, the molybdenum layer is exposed and the side walls of the mesa are almost vertical. With SF₆/CHF₃ feed gas mixture, the overall etch rate is lower (around 300 nm/min) as compared to the SF₆/O₂ gas mixture (around 200 nm/min). Therefore, in the final MIS structure, the latter process is employed to expose the gate contact. Further optimization of the mesa shape could be obtained using SF₆/CHF₃/O₂ as feed gas mixture [68].

Figure 2.10 (a) shows a photograph of a sample in top view with several MIS structures and after different etch times. In the lower part of the picture, the interlayer (IL) stack is not removed yet, while in the upper part of the picture the gate metal is exposed. SEM images of the developed MIS structure are shown in figures 2.10 (b) cross section, (c) top view tilted and (d) top view tilted with the border of one structure enlarged. In most cases, the resulting mesa sizes are around 100 μm larger than the holes in the sputter mask due to a non-vertical sputter deposition as well as etching.

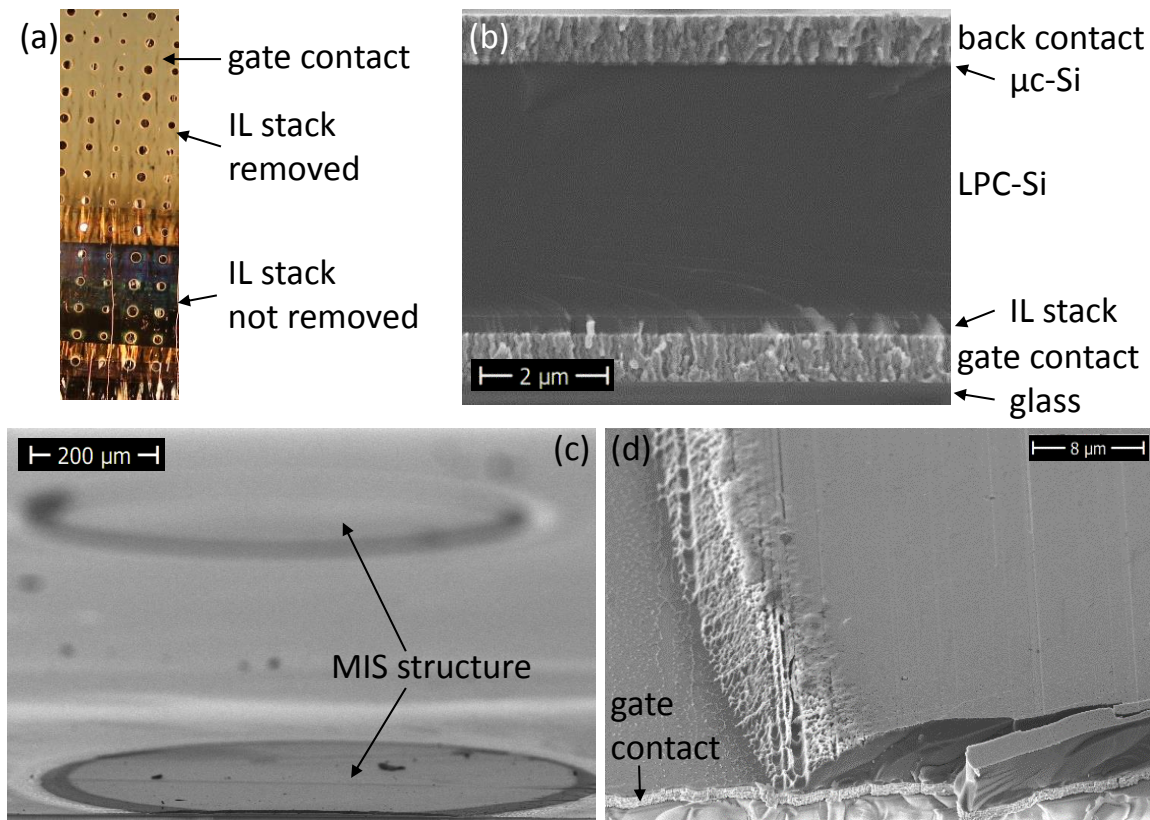


Figure 2.10: Developed MIS structure for C-V measurements: (a) Photograph of sample's surface to illustrate appearance of sample after different etch times. SEM images of (b) the cross section and (c) and (d) top view tilted.

The employed process steps to manufacture MIS structures are successfully used for samples with 15 μm absorber as well as with 5 μm absorber.

CHAPTER 3

Sample Characterization

In this chapter, all methods that are employed in the framework of this thesis to characterize LPC-Si-on-glass samples (section 3.1) and single dielectric layers on silicon wafers (section 3.2) are summarized and described. In section 3.3, the simulation package ASPIN3 is introduced, which is used to model optical properties (section 5.3) as well as solar cell parameters (sections 6.3.2 and 6.6).

3.1 Characterization of LPC-Si samples

LPC-Si material is studied macroscopically. The electrical quality is determined from solar cell parameters using commonly applied measurement techniques such as the sun simulator. The doping concentration is determined from sheet resistance measurements. The photoluminescence (PL) technique is used to study macroscopically the structural properties of LPC-Si on glass. The interface between the interlayer and the LPC-Si absorber is studied microscopically using transmission electron microscopy. In addition, the interface is studied with regard to its electrical properties using the capacitance-voltage (C-V) technique. All methods are described below.

3.1.1 SunsVoc and current-voltage (J - V) curves

The open-circuit voltage (V_{oc}) and pseudo fill factor (pFF) of fabricated solar cells is determined from SunsVoc measurements using a SunsVoc set-up from Sinton Instruments. Measurements are performed in substrate configuration.

The current-voltage (J - V) curves are measured with a sun simulator with AAA characteristic at 1000 W/m^2 under AM1.5 spectrum [73]. A chuck is used which allows for the illumination of the cells in substrate (illumination from the silicon side) and superstrate (illumination from the glass side) configuration. However, the temperature of the solar cells is not monitored. Selected IBC cells are measured with an ARF attached to the glass surface facing the light source in order to reduce reflection at the air/glass interface. The foil is provided by DSM Advances Surfaces [74].

3.1.2 UV-Vis transmission and reflection

Transmission ($T(\lambda)$) and reflection ($R(\lambda)$) spectra of LPC-Si solar cells are measured with a PerkinElmer LAMBDA 1050 spectrometer with an integrated sphere. $1 \text{ mm} \times 2 \text{ mm}$ of the cell area is illuminated. If not stated otherwise, the cell is illuminated in superstrate configuration. From $T(\lambda)$ and $R(\lambda)$, the short-circuit current density potential ($J_{\text{sc,max}}$) is calculated using equation (3.1).

$$J_{\text{sc,max}} = \int_{300 \text{ nm}}^{1100 \text{ nm}} \text{AM1.5}(\lambda) \times (1 - R(\lambda) - T(\lambda)) d\lambda \quad (3.1)$$

3.1.3 Quantum efficiency (QE) from spectral response (SR)

The spectral response (SR), this is, the ratio of output current of a solar cell under short circuit conditions (I_{sc}) and the power of incident monochromatic light, is measured for wavelengths between 300 and 1100 nm using a self-built set-up with a monochromator. Around $2 \text{ mm} \times 4 \text{ mm}$ of the cell area is illuminated. If not stated otherwise, the cell is illuminated in superstrate configuration. Based on SR, the external quantum efficiency (EQE) is obtained

$$\text{EQE}(\lambda) = \frac{h c}{q} \times \frac{\text{SR}(\lambda)}{\lambda}. \quad (3.2)$$

where h is the Planck constant, c is the speed of light and q is the elementary charge.

The EQE includes optical losses, this is, reflection and transmission losses. By definition, the internal quantum efficiency (IQE) represents the QE when optical losses are subtracted, this is, considering only photons that are absorbed by the solar cell:

$$\text{IQE}(\lambda) = \frac{\text{EQE}(\lambda)}{1 - R(\lambda) - T(\lambda)} \quad (3.3)$$

3.1.4 Doping density (N) from sheet resistance (R_s)

The doping density (N), the donor doping density (N_D) or acceptor doping density (N_A), of LPC-Si is determined from measured sheet resistance (R_s) results. R_s is determined with a combined constant current source and digital voltmeter (Jandel RM3-AR) using the four point method. Measurements are performed on at least 6 different spots on the bare LPC-Si surface. From the averaged R_s results ($\overline{R_s}$), N is calculated according to equations (3.4).

$$N = \frac{1}{q \times C \times \mu \times \overline{R_s} \times d_{\text{LPC-Si}}} \quad (3.4)$$

$$\mu = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(\frac{N}{N_0}\right)^\gamma}$$

$\mu_{\min}$, $\mu_{\max}$, N_0 and γ are constants empirically determined for n-doped and p-doped crystalline silicon [75]. The charge carrier mobility (μ) in n-doped LPC-Si is reduced to $C = 80$ % of the mobility in mono-crystalline silicon, respectively, which was found to be appropriate for LPC-Si material [46].

3.1.5 Photoluminescence (PL)

Generated electron-hole pairs in a semiconductor return to equilibrium conditions by recombination. Without defects in the band gap, the recombination is upon the emission of photons. The energy of the photon corresponds to the band gap of the semiconductor. The emission of light by the semiconductor is called luminescence. Recombination via defect state located in the band gap is non-radiative. Measuring the luminescence with a camera gives insight into the spatial distribution of defects (dark areas in the image). The excitation of electron-hole pairs can be realized with photons (PL) or with electrons (electro-luminescence (EL)). The resolution of the obtained image depends on the optical lens array and the choice of the detector.

The employed PL set-up used in this work is equipped with light emitting diodes emitting light with 650 nm and a charge-coupled device (CCD) silicon camera. The sample under test is excited with an illumination intensity of one sun. The luminescence signal is filtered with a double side polished gallium arsenide wafer coated with a SiN_x film for anti-reflection. All images are acquired in superstrate configuration.

3.1.6 Morphology and elemental distribution from electron microscopy

The morphology, the thickness of ultra-thin layers as well as the nitrogen and oxygen distribution at the IL/LPC-Si interface are determined with transmission electron microscopy (TEM) and scanning transmission electron microscopy and electron energy loss spectroscopy (STEM-EELS).

To this end, cross-sectional specimens are prepared by face-to-face gluing of the corresponding solar cell or thin-film stacks. The resulting cross-sections are polished mechanically and using an Ar-ion ion beam until a hole formed. At the fringes of the hole, the specimens are electron-transparent.

For TEM investigations, a Philips CM12/STEM set-up operating at 120 kV accelerating voltage is employed. A lanthanum hexaboride (LaB_6) cathode is used. A super TWIN lense is used for high resolution, i.e. 0.3 nm dot resolution and 0.14 nm line resolution. The camera is a $2k \times 2k$ CCD camera from Gatan (Orius SC 830). Sample preparation and TEM image acquisition are performed by Ulrike Bloeck at the Helmholtz Zentrum Berlin in the CoreLab CCMS.

At the Humboldt University in Berlin in the department of physics, STEM-EELS investigations are performed with Dr. Holm Kirmse. A JEOL JEM2200FS set-up is used. The instrument is operated at 200 kV and it is equipped with an in-column filter. For achieving high spatial resolution and high enough EELS signal, the size of the STEM probe is set to 0.5 nm.

An electron beam passes the sample. Some electrons in the beam scatter inelastically with electrons in the material and they loose energy. The spectrum, that is recorded, depicts the intensity of the measured signal as a function of the energy lost by the electrons in the beam.

Exemplary, figure 3.1 shows measured spectra obtained on three different spots, namely in the SiO_x , the SiN_x and the LPC-Si region.

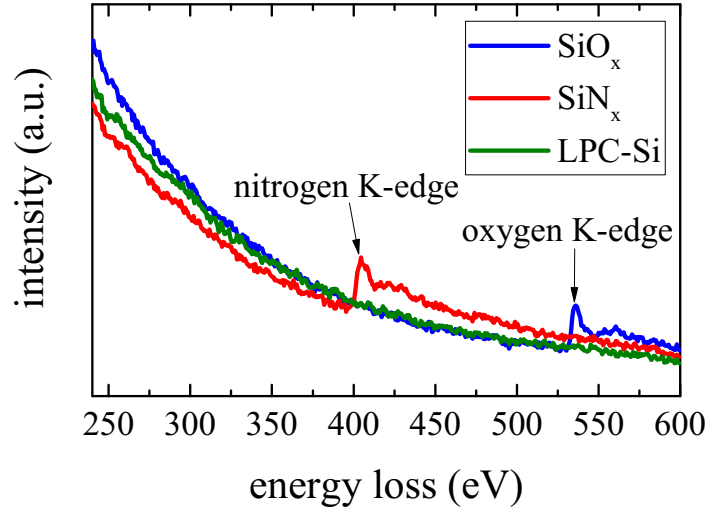


Figure 3.1: Measured STEM-EELS line scans detected in the SiO_x , the SiN_x and the LPC-Si region close to the IL/LPC-Si interface.

The spectra show the characteristic ionization edges (K-edges) for nitrogen and oxygen in the SiO_x and SiN_x region, respectively. The Si-K ionization edge is located at around 1840 eV, so it is not visible in the spectrum.

STEM-EELS line scans are performed, i.e. the spectra displayed in figure 3.1 are measured for several spots in a line. From the STEM-EELS line scans, jump-ratio profiles are derived to signify the distribution of nitrogen and oxygen. For this, the three window technique is applied [76] since the background modelling for the oxygen K edge at 532 eV is complicated by the post-edge intensity of the nitrogen K edge at 401 eV. For calculating the jump-ratio intensity of each recorded spectrum, two energy intervals of 20 eV are defined. The pre-edge intensity is collected at 20 eV below the edge energy and the post-edge intensity at 10 eV above the edge energy. Thus, for nitrogen the pre-edge interval for integration ranges from 470 eV to 490 eV whereas the post-edge interval ranges from 400 eV to 420 eV. The jump-ratio is calculated by dividing the integrated post-edge intensity by the integrated pre-edge intensity. Finally, the normalized jump-ratio values are given as line profiles for signifying the elemental distribution. Adequately to the nitrogen K edge, the oxygen K edge is treated. The pre-edge interval ranges from 500 eV to 520 eV and the post-edge interval from 530 to 550 eV.

Please note that a quantitative description of the elemental composition is not possible upon the presented data. For a quantitative description, scattering cross sections that describe the possibility of interaction between the electrons from the beam and from the nitrogen and oxygen atoms need to be known.

3.1.7 Capacitance-voltage (C-V) curves

Capacitance-voltage (C-V) measurements are used to determine the interface defect state density (D_{it}) and the effective interlayer charge density ($Q_{IL,eff}$) at the interface between the interlayer and the LPC-Si. For this, the MIS structure shown in figure 2.6 is developed as described in section 2.4.

C-V curves are measured with a Keithley 590 CV analyzer by applying a direct current (DC) voltage (called gate voltage (V_g)) to the gate metal (molybdenum layer). The DC signal defines whether the MIS structure is in accumulation, depletion or inversion (section 4.3). The DC voltage is superimposed by a 1 MHz signal with an amplitude in the mV-range. Minority charge carriers, whose concentration in the inversion region increases exponentially with DC voltage, cannot follow the high-frequency signal due to their low generation and recombination rate. Therefore, their charge contribution to the overall high-frequency capacitance is not measured and, thus they cannot be measured and the high-frequency capacitance remains constant in the inversion region (figure 4.3).

C-V curves are measured in sweep mode as well as in relaxation mode. In case the relaxation mode is employed, the capacitance is measured as a function of time at a given gate voltage. Once the capacitance reaches a constant value for a time interval of 15 s, the measurement stops and the constant capacitance value is recorded for the C-V curve. This is repeated for all gate voltages of the C-V curve. In this manner, equilibrium capacitances of the MIS system are obtained. All C-V curves are measured in darkness to prevent parasitic charge generation.

Parasitic processes such as leakage currents, charge redistribution within the interlayer and charge carrier transfer across the IL/LPC-Si interface may hinder the reliable evaluation of measured C-V curves with respect to D_{it} and $Q_{IL,eff}$. For instance, it may happen that charge carriers penetrate through the interlayer when a voltage is applied across the MIS structure (called leakage currents). These currents prevent the formation of an accumulation or inversion layer in MIS systems. In measured C-V curves the effect of leakage currents is reflected as a drop of the capacitance in the inversion regime indicating the formation of a deep depletion region.

Charge carrier injected from the silicon or from the gate into the interlayer may also occur as well as a redistribution of mobile charges that may exist in the interlayer in addition to fixed charges. Redistribution of mobile charges affects the deduced fixed charge density. In measured C-V curves a hysteresis is observed when charges are injected from the silicon or from the gate into the interlayer or when mobile charges within the interlayer redistribute. The orientation of the hysteresis gives insights into the responsible parasitic process. For instance, charge injection from the silicon into the interlayer would lead to a clockwise hysteresis on

n-doped silicon: If the C - V measurement is started in accumulation, this is, at a positive gate voltage in case of n-doped silicon, majority charge carriers (electrons) are injected from the silicon into trap levels located in the interlayer close to the interface. This increases the negative component of $Q_{IL,eff}$ which shifts the C - V curve towards more positive voltages. When starting in inversion, this is, at a negative gate voltage, minority charge carriers (holes) are injected from the silicon into the interlayer. Hence, the positive component of $Q_{IL,eff}$ increases shifting the C - V curve towards more negative voltages. If the orientation of the hysteresis is inverted, i.e. counter-clockwise with n-doped silicon, other charge mechanisms dominate. One option is that electrons are injected from the gate into traps in the interlayer stack. However, charging of traps near the metal/IL interface has little effect on $Q_{IL,eff}$.

In order to examine such parasitic processes at the IL/LPC-Si interface in the developed MIS structures, high-frequency C - V curves are measured in relaxation mode as described above. Two C - V curves are recorded per mesa structure, one scans from the accumulation to the inversion region and the other one in the opposite direction. Figure 3.2 (a) shows two corresponding C - V curves. The typical S-shape of the curves is obtained whereby the highest capacitances are measured in the accumulation regime.

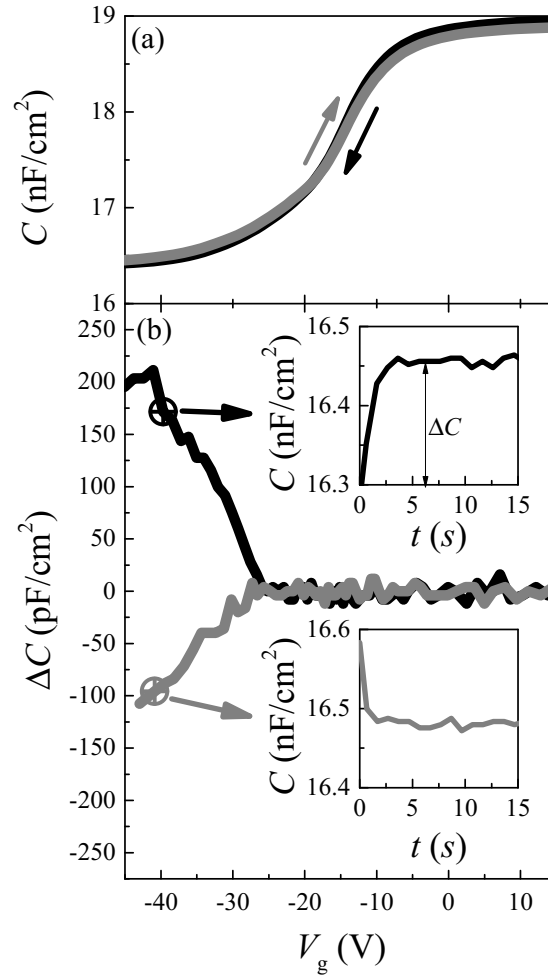


Figure 3.2: Analysis of parasitic processes with N/O/ON/(n)-doped LPC-Si sequence. (a) High-frequency C - V curves measured in relaxation mode. Arrows depict the scanning direction of the gate voltage. (b) ΔC - V_g curves. Exemplary, capacitance-time (C - t) curves are shown for two gate voltages in the inversion region.

As described in section 3.1.7, when C - V curves are measured in relaxation mode, the capacitance is measured as a function of time for each applied gate voltage. As can be seen in the insets in figure 3.2 (b), for gate voltages below -25 V the capacitance is not stable for the first few seconds. The capacitance stabilizes after approximately 15 s. The difference between stabilized capacitance and initial capacitance is denoted as ΔC . When the gate voltage is swept from accumulation to inversion, the initial capacitance is lower as compared to the stabilized capacitance ($\Delta C > 0$) due to the slow generation rate of minority charge carriers. The opposite effect ($\Delta C < 0$) is observed when the gate voltage is swept from the inversion region to the accumulation region because of the slow recombination rate of minority charge carriers. For

gate voltages between -25 V and 15 V, this is, in the depletion and accumulation regions, the capacitance is time-independent and thus, $\Delta C = 0$ pF/cm². Stabilized capacitances are used in the C-V curve. The observed stabilization of the capacitance in the inversion region indicates the formation of an inversion region and thus, no leakage currents are present. This indicates that the developed MIS structure is suitable for measuring true capacitances via the C-V technique.

3.2 Characterization of dielectric layers on silicon wafers

Single dielectric layers on silicon wafers are studied with respect to their refractive index, their extinction coefficient and their stoichiometry using spectral ellipsometry as well as fourier transform infrared spectroscopy (FTIR). Furthermore, the residual stress of the layers is determined.

The film characteristics depend on the substrate on which they are deposited. Thus, the film properties that are obtained by using the listed characterization methods for single layers on silicon wafers might differ from the properties of the films when they are incorporated into LPC-Si solar cells. Furthermore, when used in LPC-Si solar cells, the films experience the crystallization process, which might impact the film, for example by densification. Nevertheless, it is assumed that relative trends remain.

3.2.1 Refractive index (n), extinction coefficient (k) and stoichiometry (x)

A spectral ellipsometer (SENTECH SE850) is used to determine the thickness (d), the refractive index spectrum ($n(\lambda)$) as well as the extinction coefficient spectrum ($k(\lambda)$) of dielectric films.

Monochromatic, polarized light hits the sample's surface and interacts with the material. The wavelength of the incident light is varied between 220 and 850 nm and the angle of incidence is 50 °, 60 ° and 70 °. The change in polarisation upon reflection at the film's surface quantified by an amplitude (Ψ) and a phase difference (δ) is detected. In order to determine the desired parameters from Ψ and δ , the Tauc-Lorentz oscillator model [77,78] is used for all dielectric layers. On top of the SiN_x films, a SiO_x film is simulated as Cauchy-layer to account for an oxidized surface. In all cases, the SiO_x layer is < 5 nm. Based on the obtained refractive index at 632.8 nm ($n_{632.8 \text{ nm}}$), the stoichiometry (x) of the SiN_x is determined using equation (3.5) [79–81] with $n_{632.8 \text{ nm}}(a\text{-Si:H}) = 3.3$ and $n_{632.8 \text{ nm}}(\text{Si}_3\text{N}_4) = 1.9$. Hydrogen bonding is neglected.

$$x = \frac{[\text{N}]}{[\text{Si}]} = \frac{4}{3} \times \frac{3.3 - n_{632.8 \text{ nm}}}{n_{632.8 \text{ nm}} - 0.5} \quad (3.5)$$

3.2.2 N-H and Si-H bond densities from mid-infrared transmission

The chemical composition of dielectric layers is investigated with fourier transform infrared spectroscopy (FTIR).

A Bruker Tensor 27 FTIR spectrometer is employed to measure the transmission spectra ($T(\omega)$) for wave numbers in the mid-infrared ($400 - 4000 \text{ cm}^{-1}$) of the silicon wafer/dielectric layer stacks. The spectra are corrected for atmospheric influence using the OPUS 7 software [82].

In order to derive the absorption spectra ($\alpha(\omega)$) of the dielectric layers, the SCOUT software [83] is used to fit the measured transmission spectra to the calculated spectra of a simulated stack composed of vacuum/dielectric layer/native SiO_x /silicon wafer/vacuum.

In order to determine the bond density ($[X-Y]$) of the X-Y bond, the corresponding peak located at the characteristic wave number is fitted to a Gaussian function using the Fityk software. Based on the fit parameters, the normalized absorption intensity ($I_{[X-Y],\text{norm}}$) is calculated as suggested by Bustarret *et al.* [80].

$$I_{[X-Y],\text{norm}} = \int \frac{\alpha(\omega) \times d\omega}{\omega} \quad (3.6)$$

$$[X-Y] = K_{[X-Y]} \times I_{[X-Y],\text{norm}}$$

$K_{[X-Y]}$ is the oscillator strength factor. For the bonds of interest in this thesis ([Si-H] and [N-H] stretching bonds located at around 2180 cm^{-1} and around 3337 cm^{-1} , respectively) $K_{[\text{Si-H}]} = 4 \times 10^{20} \text{ cm}^{-2}$ and $K_{[\text{N-H}]} = 1.2 \times 10^{20} \text{ cm}^{-2}$ [80].

The density of bonded hydrogen is calculated as the sum of [Si-H] and [N-H] bond densities [80]:

$$[\text{H}] = [\text{Si-H}] + [\text{N-H}] \quad (3.7)$$

3.2.3 Residual film stress (σ_f) from sample curvature

The residual stress (σ_f) in dielectric films is composed of two components, on the one hand the intrinsic stress (σ_i), which is determined by the film structure and by the deposition conditions, and on the other hand the thermal stress (σ_{th}). The latter is equal to the difference of the coefficient of thermal expansion (CTE) of film and substrate, respectively, the difference of the

temperature (T) during the deposition and during the investigation of σ_f , respectively, and the biaxial modulus of the film (B_f) [84]: $\sigma_{th}(T) = (CTE_{\text{substrate}} - CTE_{\text{film}}) B_f (T - T_{\text{deposition}})$.

The residual stress of the dielectric layers is estimated using the curvature method. In principle, the curvature of a wafer is measured before and after the deposition of the dielectric layer under investigation. Stoney's equation (3.8) is then used to calculate the residual stress [85].

$$\sigma_f(T) = \sigma_i + \sigma_{th} = \frac{E_s \cdot d_s^2}{6 \cdot (1 - \nu_s) \cdot d_f} \cdot \left(\frac{1}{R_{\text{post}}} - \frac{1}{R_{\text{pre}}} \right) \quad (3.8)$$

$E_s = 130$ GPa and $\nu_s = 0.28$ are the Young's modulus and the Poisson's ratio of the silicon substrate, respectively [86]. The thicknesses of the substrate (circular silicon wafer) and of the film are $d_s = 100$ to 350 nm and $d_f = 300$ to 350 μm , respectively. R_{pre} and R_{post} are the radii of the curved substrate before and after the film deposition, respectively. R is calculated using equation (3.9).

$$R = \frac{(0.5 \times L)^2}{2 \times h} \quad (3.9)$$

The height of the curvature (h) is measured with a Dektak XT Bruker profilometer by scanning a distance ($L = 5$ cm) across the sample's surface, whereby the centre of the wafer is passed.

Films under compression try to expand, and if the substrate is thin, the film bows the substrate with the film being on the convex side as seen from the film side (figure 3.3 (a)) [87]. R_{post} and thus, σ_f , are positive in this case. If the film has tensile stress, the film tries to contract bowing the substrate so the film is on the concave side (figure 3.3 (b)). R_{post} and σ_f are negative in this case. Exemplary, figure 3.3 depicts profilometer line scans before and after the deposition of two different SiN_x films with (a) tensile and (b) compressive stress.

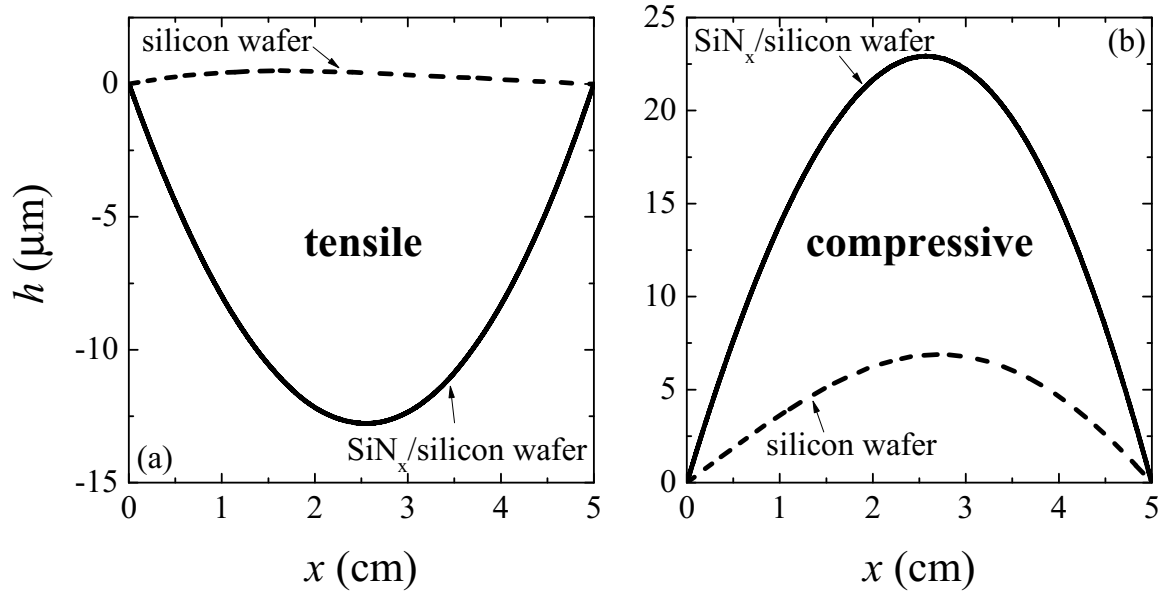


Figure 3.3: Profilometer line scans across the surface of a silicon wafer before (dashed line) and after the SiN_x film was deposited (solid line).

As can be seen in figure 3.3 (b), the bare wafer is bent by 5 μm before the deposition of the SiN_x film. Such bending is observed for several wafers. However, the initial bending radius is taken into account in the Stoney's equation and thus, σ_f represents the stress in the film only.

3.3 Simulations with ASPIN3

ASPIN3 is a two-dimensional (2D) simulation software package developed at the University of Ljubljana [88]. In the framework of this thesis, ASPIN3 is used to simulate two things. On the one hand, ASPIN3 is used to simulate reflection and transmission losses for the glass/IL/LPC-Si/(i) a -Si:H/(p) a -Si:H/ITO sequence based on various interlayer stacks (section 5.3). Doing this by simulations instead of by experiment, saves time and costs. Selected layer combinations are compared to experimental results. On the other hand, ASPIN3 is used to model measured solar cell parameters. In section 6.3.2, the effective front-side surface recombination velocities that are obtained for the IL/LPC-Si interface are fed together with the bulk lifetime into the software to model measured external quantum efficiency (EQE) curves. From the best fit, the effective minority charge carrier diffusion length is calculated and compared to literature results. In section 6.6, the open-circuit voltage and the short-circuit current density are simulated as a function of the effective front-side surface recombination

velocity for two different bulk lifetimes. It is evaluated, which of the two parameters limits the performance of LPC-Si solar cells on the developed interlayer stacks.

In this section, the software is described roughly. Further details are found in [89, p. 29-35]. The code is adapted from the code developed by Dr. Paul Sonntag [89].

ASPIN3 simulates the electrical part and the optical part of a structure separately. For the optical part, the thicknesses of the implemented layers as well as their optical parameters (refractive index and extinction coefficient spectra) are taken into account. Based on these data, the generation film is calculated by ASPIN3. ASPIN3 can only treat planar layers which is sufficient for all samples that are simulated in this work. For all simulations a sequence of glass/IL/LPC-Si/(i) *a*-Si:H/ (p) *a*-Si:H/ITO is simulated, which is in accordance with a typical test cell (figure 2.5). The glass is 1.1 mm and the (i) *a*-Si:H/(p) *a*-Si:H/ITO layers have a thickness of 6 nm/20 nm/90 nm. The refractive index and extinction coefficient spectra of ITO [90], silicon [91] and glass [92] are taken from literature. The $n(\lambda)$ and $k(\lambda)$ data of the SiO_x and SiN_x films as well as of the *a*-Si:H emitter layers are obtained from ellipsometry measurements on corresponding single layers on silicon wafers.

For the electrical part, non-linear partial differential equations are solved based on the drift-diffusion model. In principle, ASPIN3 is capable of simulating intrinsic (Auger and radiative) and extrinsic (SRH) recombination mechanisms. For non-degenerately doped silicon, the Shockley-Read-Hall (SRH) process is generally dominant [93]. Thus, in the simulation of studied non-degenerately doped LPC-Si test cells ($N_D \approx 10^{17} \text{ cm}^{-3}$), only SRH recombination is considered. The SRH recombination rate is calculated from the majority and minority charge carrier SRH bulk lifetimes. The latter is used as input parameter while the SRH bulk lifetime of majority charge carriers is fixed at 10 μs for all simulations.

A 2 nm thin amorphous defect layer is simulated at the rear-side of the LPC-Si absorber to result in a good match between experimental and simulated open-circuit voltages as was also found in [34,47]. Gaussian-like defects located in the middle of the silicon band gap are introduced. The density of these defects is named N_{tr} . The mobility in the defect layer is set equal to the amorphous emitter layers.

The charge carrier mobilities are calculated using the Masetti model (equation (3.4)) [75] whereby the mobilities are reduced to 80 % of the mobility in crystalline silicon [46,53].

CHAPTER 4

Theoretical Background

The interlayer (IL) stack, which is developed in the framework of this thesis, is characterized with regards to its optical properties, this is, how much light is reflection from it and how much light is absorbed by it. Furthermore, the interlayer stack is characterized with respect to its passivation properties.

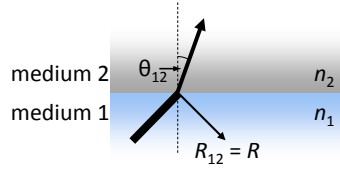
In this chapter, the theoretical background for reflection and absorption of dielectric multi-layer stacks (section 4.1) as well as fundamentals on the passivation of silicon surfaces (section 4.2) is addressed. In section 4.3 it is outlined how the interface passivation parameters (interface defect state density (D_{it}), fixed charge density (Q_f) and effective surface recombination velocity (S_{eff})) are determined from measured capacitance-voltage (C-V) curves and from using the extended Shockley-Read-Hall (SRH) formalism and the algorithm developed during this thesis based on section C and [94,95].

4.1 Reflection and absorption of dielectric multi-layer stacks

LPC-Si solar cells are generally illuminated from the glass side through the dielectric multi-layer stack (figure 1.4). In order to realize a high cell current it is a fundamental requirement to couple the light into the thin LPC-Si absorber. Therefore, the reflection at the glass/IL stack needs to be as low as possible and no light should be absorbed in the interlayer stack. In this section the fundamentals on reflection and absorption of dielectric multi-layer stacks are presented briefly.

Light that hits the interface between two media with different refractive indices ($n_1(\lambda)$ and $n_2(\lambda)$) is partly reflected and partly transmitted under a specific angle of refraction (θ_{12}) as can

be seen below. According to Fresnel equations, the reflection (R) for normally incident light is solely a function of $n_1(\lambda)$ and $n_2(\lambda)$.

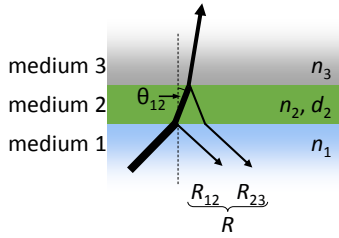


Normally incident light

$$R(\lambda, n_1, n_2) = \frac{(n_1(\lambda) - n_2(\lambda))^2}{(n_1(\lambda) + n_2(\lambda))^2}$$

When light with $\lambda = 632.8$ nm hits the interface between semi-infinite glass ($n_{\text{glass}}(632.8 \text{ nm}) \approx 1.5$ [96]) and semi-infinite silicon ($n_{\text{silicon}}(632.8 \text{ nm}) \approx 3.9$ [91]) under normal incidence around 20 % of the light is lost due to reflection. In order to reduce R , a layer (called anti-reflection coating (ARC)) with a specific thickness (d) can be inserted between glass and silicon as depicted in the sketch below. Due to interference between the light reflected from the interface between medium 1 and 2 and medium 2 and 3, reflection depends on the thickness and on the refractive index of the ARC [97, p. 162]. $\delta(\lambda, n_2, d_2)$ is called phase factor.

Normally incident light



$$R(\lambda, n_1, n_2, n_3, d_2) = \frac{r_1(\lambda)^2 + r_2(\lambda)^2 + 2r_1r_2 \cos \delta(\lambda)}{1 + r_1(\lambda)^2 r_2(\lambda)^2 + 2r_1(\lambda)r_2(\lambda) \cos \delta(\lambda)}$$

$$r_1(\lambda) = \frac{(n_1(\lambda) - n_2(\lambda))^2}{(n_1(\lambda) + n_2(\lambda))^2}$$

$$r_2(\lambda) = \frac{(n_2(\lambda) - n_3(\lambda))^2}{(n_2(\lambda) + n_3(\lambda))^2}$$

$$\delta(\lambda, n_2, d_2) = 4\pi \frac{n_2(\lambda) d_2}{\lambda}$$

In order to achieve zero reflection for a specific wavelength, the ARC layer needs to fulfil (a) $n_1 < n_2 < n_3$, $n_2^2 = n_1 n_3$ and $n_2 d_2 = \lambda/4$. Taking the example from above with glass and silicon as medium 1 and 3, respectively, and assuming incident light with 632.8 nm, zero reflection is obtained with $n_2 = 2.4$ and $d_2 = 65$ nm. For example, SiN_x films deposited by plasma-enhanced chemical vapor deposition can be tuned to fulfil these properties.

The extinction coefficient (k) is a measure for the absorption of dielectric layers, which should be minimized because it is parasitic. The extinction coefficient is directly proportional to the absorption coefficient (α), $k(\lambda) = \alpha(\lambda) \lambda / (4 \pi)$.

4.2 Passivation of silicon surfaces

In this thesis, the passivation quality at the interface between the interlayer stack and the LPC-Si absorber is investigated using capacitance-voltage (C-V) measurements. From measured C-V curves, the interface defect state density (D_{it}) and the effective interlayer charge density ($Q_{IL,eff}$) are determined as described in section 4.3. In this section both parameters are introduced.

A silicon crystal consists of an ordered structure of silicon atoms, which chemically bond to each other and form the energetic states within the material. At the free surface of the crystal the atoms lack neighbouring atoms resulting in dangling bonds that can capture and release charge carriers [98, 99]. The energy level of a dangling bond state depends on the kind of atom that is back-bonded to the silicon atom. In the ideal silicon lattice, the silicon atom is back-bonded to three silicon atoms. The $Si_3 \equiv Si \bullet$ defect (" $\equiv$ " stands for three connected bonds and " $\bullet$ " represents one dangling bond) lies energetically inside the silicon band gap and is a major recombination center [100]. In addition to the defect states originating from silicon dangling bonds, defect states are present that originate from stretched or compressed atomic bonds and bonding angles [100]. The defect density at the surface of a clean silicon crystal is almost as high as the density of surface atoms (10^{15} cm^{-2}) [70, p. 380].

A commonly applied method to reduce surface states is the deposition of dielectric layers on top of the silicon crystal. The atoms in the film bond to the dangling bonds at the surface and thus, the interface defect state density (D_{it}) is reduced (chemical passivation). Furthermore, fixed charges (Q_f) can be present in the dielectric film which provoke the separation of majority and minority charge carriers in space (field-effect passivation).

Fixed charges originate from silicon dangling bonds inside the dielectric films close to the interface to the silicon crystal. As mentioned above, the energetic position of a silicon dangling bond defect depends on the three atoms back-bonded to the silicon atom. If the back-bonded atoms are more electronegative than the silicon atom, the back-bonded atoms attract electrons to themselves [70, p. 276] and the energy of the defect level is in the upper half of the silicon band gap resulting in a positive fixed charge. If the silicon atom is more electronegative than the back-bonded atoms, the defect is negatively charged.

If the charges are located in the dielectric film at a specific distance (x) from the interface, the fixed charge density that is "seen" by the charge carriers in the silicon crystal is reduced by a factor of $(d_{\text{dielectric}} - x)/d_{\text{dielectric}}$, with $d_{\text{dielectric}}$ being the thickness of the dielectric layer. In many cases, an effective fixed charge density ($Q_{f,eff}$) is reported, as though the charges were located at the dielectric layer/silicon interface.

One distinguishes between accumulation-type passivation (majority charge carriers are attracted by the fixed charges) and depletion- or inversion-type passivation (minority charge carriers are attracted by the fixed charges). Accumulation-type passivation is often the preferred type of passivation, because the inversion-type passivation results in an enhanced recombination of charge carriers via defects located in the depletion region, i.e. between the inversion layer directly at the interface and the silicon bulk. Furthermore, enhanced recombination is observed when no inversion layer is formed, e.g. due to an insufficient fixed charge density.

Figure 4.1 displays typical materials used to passivate silicon wafer surfaces arranged according to typical defects state densities and fixed charge densities at the interface.

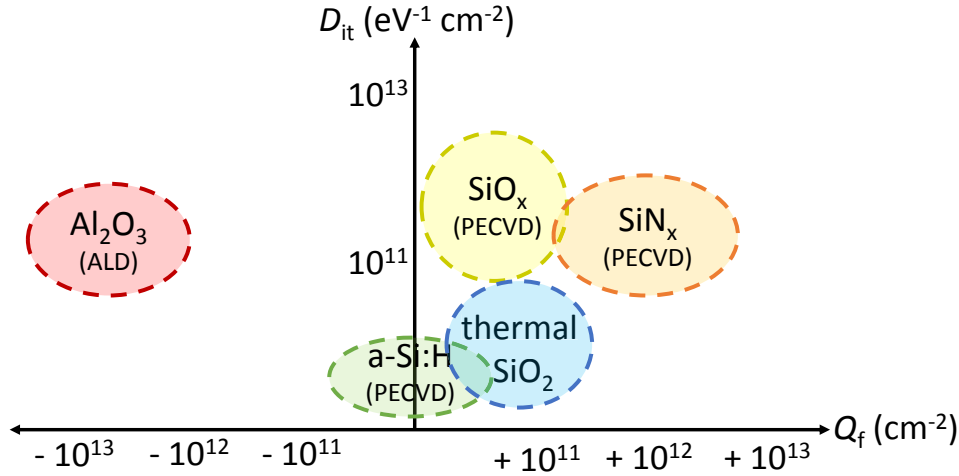


Figure 4.1: Overview of common passivation coatings on silicon wafers arranged quantitatively in terms of the interface defect state density (D_{it}) and the fixed charge density (Q_f). After [101]. Selected references: (i) a -Si:H: [102, 103], thermal SiO₂: [95, 104], PECVD SiO_x: [41, 105, 106], PECVD SiN_x: [104, 107, 108], Al₂O₃: [104, 109].

4.3 Determination of D_{it} , $Q_{IL,eff}$ and $S_{eff,front}$ from measured C-V curves

In this thesis, the passivation quality at the buried interface between the interlayer stack and the LPC-Si material is investigated in terms of D_{it} , $Q_{IL,eff}$ and effective front-side surface recombination velocity ($S_{eff,front}$). To this end, a MIS structure based on LPC-Si on glass is developed which enables the determination of the passivation parameters via capacitance-voltage (C-V) measurements. Further details on the MIS structure can be found in section 2.4.

In C-V measurements, the capacitance of the MIS structure is measured as a function of the DC voltage applied to the gate metal sandwiched between glass substrate and interlayer stack

(figure 2.6). The energy bands and charge carriers in the silicon respond to the applied gate voltage (V_g), which is discussed next.

Figure 4.2 shows MIS energy band diagrams and charge distributions in thermal equilibrium for four different voltage conditions. In figures 4.2 (a1)-(a4) the ideal MIS structure ($D_{it} = 0 \text{ eV}^{-1} \text{ cm}^{-2}$ and $Q_{IL,eff} = 0 \text{ cm}^{-2}$) is discussed while in figures 4.2 (b1)-(b4), defect states and fixed charges are present at the interface (real MIS structure). In the figures, the work function difference between metal and semiconductor is assumed to be zero.

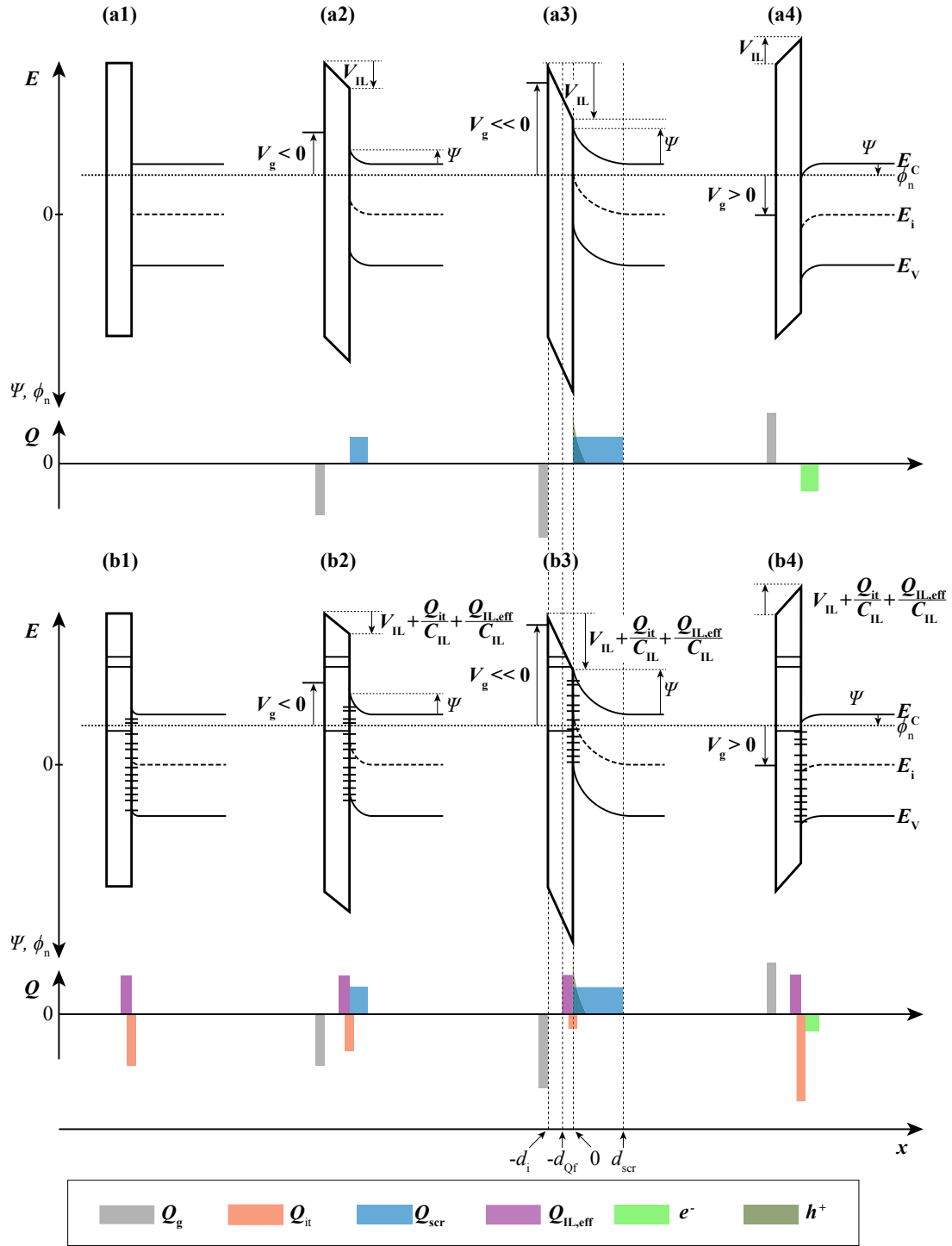


Figure 4.2: MIS energy band diagrams and charge distributions gate voltage (V_g) conditions, exemplary with n-doped semiconductor. The rectangle represents the insulator, metal is on the left and semiconductor is on the right. (a1)-(a4): ideal MIS structure ($D_{it} = 0 \text{ eV}^{-1} \text{ cm}^{-2}$, $Q_f = 0 \text{ cm}^{-2}$. The energy level of the K^+ defect ($\text{Si} \equiv \text{N}_3$) lies $\leq 0.1 \text{ eV}$ below conduction band edge (E_C) (black horizontal line in insulator) [110]. Energy levels of $\text{Si} \equiv \text{O}_3$, $\text{Si} \equiv \text{O}_2$, $\text{Si} \equiv \text{O}_2\text{N}$ are located at higher energy levels [110]. Work function difference between metal and semiconductor is ignored.

When $D_{it} = 0 \text{ eV}^{-1}\text{cm}^{-2}$ and $Q_{IL,eff} = 0 \text{ cm}^{-2}$ and no gate voltage is applied (figure 4.2 (a1)), the energy bands are flat (flat band conditions). Upon V_g , a charge is introduced in the metal (charge density in the gate metal (Q_g)). On the silicon side, an equal and opposite charge forms to maintain charge neutrality in the MIS system (charge density in the space charge region (Q_{scr})). As a consequence of the charge redistribution close to the interface, the energy bands in the silicon bend up- or downwards depending on the gate voltage.

When the gate voltage is positive, electrons are attracted towards the interface and accumulate there (figure 4.2 (a4), accumulation condition). As a consequence, the energy bands bend downwards.

When a negative voltage is applied to the gate metal, electrons are depleted from the interface (figure 4.2 (a2), depletion condition). Immobile, positively charged ions are left behind forming a space charge region. In order to accommodate the fixed charges, the energy bands in the silicon bend upwards near the interface. When the voltage is decreased further, the width of the space charge region widens to increase the number of positive ions. For a larger negative gate voltage, minority charge carriers (holes) appear at the interface (figure 4.2 (a3), inversion condition). With further increasing the negative voltage the hole concentration increases exponentially [111].

When the silicon is p-doped, the opposite situations as for n-doped silicon described above, occurs. A negative gate voltage causes accumulation and a positive gate voltage causes the interface to be depleted or inverted.

In the ideal MIS structure discussed above, the applied gate voltage drops partially across the interlayer (V_{IL}) and partially at the IL/LPC-Si interface on the silicon side. The latter voltage drop is called surface potential (ψ_s). Overall, $V_{g,ideal} = V_{IL} + \psi_s$. Using charge neutrality and Gauss' law for the ideal MIS structure

$$Q_g = \epsilon_0 \times \epsilon_{IL,r} \times F_{IL} = \epsilon_0 \times \epsilon_{IL,r} \times \frac{V_{IL}}{d_{IL}} = C_{IL} \times V_{IL} = -Q_{scr} \quad (4.1)$$

leads to equation (4.2). The voltage term dedicated to the work function difference between metal and silicon (V_{ms}) is also considered.

$$V_{g,ideal} = \psi_s - \frac{Q_{scr}}{C_{IL}} + V_{ms} \quad (4.2)$$

ϵ_0 is the vacuum permittivity and $\epsilon_{IL,r}$ is the relative permittivity of the interlayer. F_{IL} , d_{IL} and C_{IL} are the electric field, the thickness and the capacitance of the interlayer, respectively.

If fixed charges are present in the dielectric film (figures 4.2 (b1)-(b4)), they induce, in addition to Q_g , an opposite charge in the silicon. When $D_{it} \neq 0 \text{ eV}^{-1}\text{cm}^{-2}$, another charge contribution originates from charged interface defects with corresponding interface charge density (Q_{it}), because the defect states can exchange charges with the silicon in a short time [70, p. 379]. Q_{it} depends on the location of the defect states within the band gap and on the position of the Fermi level at the interface as indicated in figures 4.2 (b1)-(b4).

When taking $Q_{IL,eff}$ and Q_{it} into account, the voltage applied to the real MIS structure is composed of

$$V_g = \psi_s - \frac{Q_{scr}}{C_{IL}} + V_{ms} - \frac{Q_{IL,eff}}{C_{IL}} - \frac{Q_{it}}{C_{IL}} \quad (4.3)$$

Based on the derived expressions for the voltage drop across the ideal MIS structure (equation (4.2)) and across the real MIS structure (equation (4.3)), D_{it} and $Q_{IL,eff}$ can be extracted when the capacitance of the MIS structure is measured as a function of the applied gate voltage which is briefly described next. The employed algorithm was introduced by Dr. W. Füssel [112] and implemented in a LabView routine by T. Henckel [113] and details on the algorithm can be found therein.

Subtracting equation (4.2) from (4.3) results in an expression for Q_{it} :

$$Q_{it} = -C_{IL} \times (V_g - V_{g,ideal}) - Q_{IL,eff} \quad (4.4)$$

At mid gap (MG), charge contributions by acceptor- and donor-like interface defect states are minimized ($Q_{it,MG} = 0 \text{ cm}^{-2}$). Thus, equation (4.4) can be used to determine $Q_{IL,eff}$ at MG voltage conditions:

$$\boxed{Q_{IL,eff} = -C_{IL} \times (V_{g,MG} - V_{g,ideal,MG})} \quad (4.5)$$

As can be seen, $Q_{IL,eff}$ is proportional to the difference between $V_{g,ideal,MG}$ and $V_{g,MG}$. $Q_{IL,eff}$ shifts a measured C-V curve along the gate voltage axis compared to the ideal C-V curve. As can be seen in figure 4.3, positive fixed charges lead to a shift towards negative gate voltages.

Equation (4.4) can also be used to determine D_{it} [114, p. 195]:

$$\begin{aligned} D_{it} &= -\frac{1}{q_{el}} \times \frac{dQ_{it}}{d\psi_s} \\ &= \frac{C_{IL}}{q_{el}} \times \left(\frac{dV_g}{d\psi_s} - \frac{dV_{g,ideal}}{d\psi_s} \right) \end{aligned} \quad (4.6)$$

where q_{el} is the charge of an electron and

$$\begin{aligned} \frac{dV_g}{d\psi_s} &= \frac{dV_g}{dC} \times \frac{dC}{d\psi_s} = \frac{dV_g}{dC} \times \left(\frac{C_{IL}}{C_{IL} + C_{SCR}} \right)^2 \times \frac{dC_{scr}}{d\psi_s} \\ \frac{dV_{g,ideal}}{d\psi_s} &= 1 - \frac{dC_{SCR}}{d\psi_s} \times \frac{1}{C_{IL}} = 1 + C_{scr,lf} \times \frac{1}{C_{IL}} \end{aligned} \quad (4.7)$$

and hence

$$D_{it} = \frac{C_{IL}}{q_{el}} \times \left(\frac{C_{IL}}{C_{IL} + C_{SCR}} \right)^2 \times \frac{dC_{scr}}{d\psi_s} \left(\frac{dC}{dV_g} \right)^{-1} - \left(1 + \frac{C_{scr,lf}}{C_{IL}} \right) \quad (4.8)$$

$C_{scr,lf}$ is the capacitances of the silicon space charge region for low frequencies. dC/dV_g is the experimentally accessible slope of measured C-V curves. As can be seen in figure 4.3, the measured C-V curve has a gentler slope compared to the ideal C-V curve due to the amphoteric character of D_{it} .

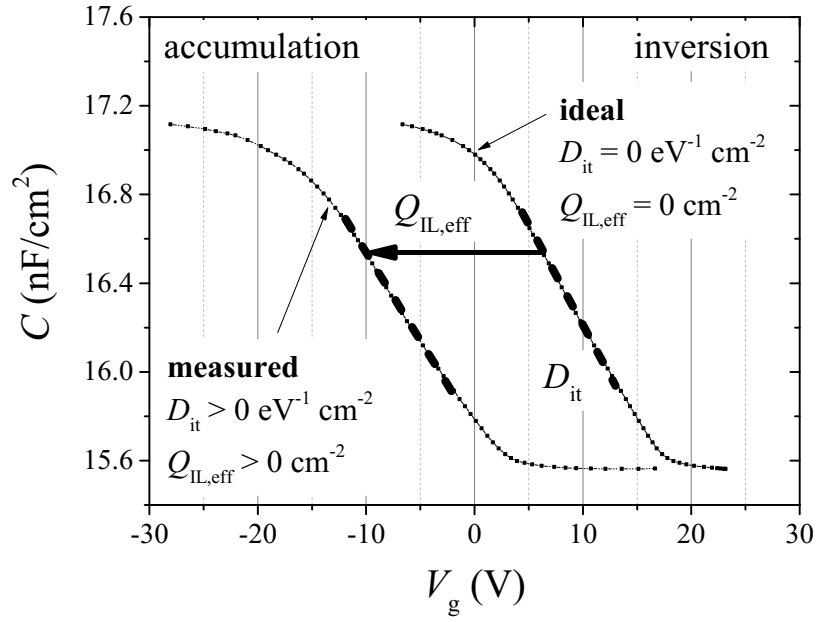


Figure 4.3: Measured high-frequency capacitance-voltage (C-V) curve of a MIS structure based on a SiN/SiO/SiON/p-doped LPC-Si stack. The calculated C-V curve of the corresponding ideal MIS structure is also shown. D_{it} at the IL/LPC-Si interface as well as $Q_{IL,eff}$ are deduced from the comparison of the two C-V curves.

Defect states located at the mid gap energy level are of special interest, since these defects exhibit the highest recombination rate for charge carriers [115, 116].

D_{it} and $Q_{IL,eff}$ determined from C-V measurements as described above are used to calculate the effective surface recombination velocity (S_{eff}). The Shockley-Read-Hall (SRH) theory [117] provides a mathematical expression to calculate S_{eff} by assuming recombination via defect states (equation (4.9)).

$$\begin{aligned}
 S_{eff} &= \frac{n_s \times p_s - n_i^2}{\Delta n} \int_{E_v}^{E_c} \frac{\nu_{th} \times D_{it}(E)}{\sigma_p^{-1}(E) \times (n_s + n_1(E)) + \sigma_n^{-1}(E) \times (p_s + p_1(E))} dE \\
 n_1(E) &= n_i \times \exp\left(\frac{E - E_i}{k_B \times T}\right) \\
 p_1(E) &= n_i \times \exp\left(-\frac{E - E_i}{k_B \times T}\right)
 \end{aligned} \tag{4.9}$$

n_s and p_s are the electron and hole density at the surface, respectively, which are in general not the same as the densities in the silicon bulk. n_i is the intrinsic charge carrier concentration ($n_i \approx 10^{10} \text{ cm}^{-3}$), ν_{th} is the thermal velocity of the charge carriers ($\nu_{th} \approx 2 \times 10^7 \text{ cm/s}$), k_B

is the Boltzmann constant and T the temperature. The electron capture and emission cross section (σ_n) and the hole capture and emission cross section (σ_p) are characteristic for a given defect and they are also energy-dependent. E is the energy, E_i is the intrinsic energy level which lies in the middle of the band gap and E_V and E_C are the energy levels of the valence and conduction band edge, respectively. The integration over the entire band gap accounts for the fact that the surface states are continuously distributed across the energy band gap.

As can be seen in equation (4.9), S_{eff} is directly proportional to D_{it} (reduction of D_{it} is chemical passivation) as well as to the product of surface electron density (n_s) and surface hole density (p_s) (reduction of either n_s or p_s is field-effect passivation).

In order to determine S_{eff} using equation (4.9), n_s and p_s need to be calculated which depend on the surface potential (ψ_s). To this end, the method introduced by Girisch *et al.* is used, whereby surface potential (ψ_s) is varied until the charges at the interface between the interlayer and the silicon (figure 4.2) balance to satisfy charge neutrality in the space-charge region [94]:

$$\boxed{Q_{\text{scr}}(\psi_s) + Q_{\text{it}}(\psi_s) + Q_g + Q_f = 0} \quad (4.10)$$

with the charge density in the space charge region ($Q_{\text{scr}}(\psi_s)$), the interface charge density ($Q_{\text{it}}(\psi_s)$) and the charge density in the gate metal (Q_g) which are calculated according to equations (4.11), (4.12) and (4.13), respectively. The fixed charge density (Q_f) is obtained from C-V measurements. The unit of all charges is cm^{-2} .

$$Q_{\text{scr}}(\psi_s) = -\text{sign}(\psi_s) \sqrt{2V_{\text{th}}\epsilon_r} \left[\exp\left(\frac{\phi_p(d) - \psi_s}{V_{\text{th}}}\right) - \exp\left(\frac{\phi_p(d)}{V_{\text{th}}}\right) + \exp\left(\frac{\psi_s - \psi_n(d)}{V_{\text{th}}}\right) - \exp\left(-\frac{\phi_n(d)}{V_{\text{th}}}\right) + \frac{\psi_s}{V_{\text{th}}} \frac{N_a - N_d}{n_i} \right]^{\frac{1}{2}} \quad (4.11)$$

$$Q_{\text{it}} = - \int_{E_V}^{E_C} D_{\text{it},a}(E) f_a(E) dE + \int_{E_V}^{E_C} D_{\text{it},d}(E) f_d(E) dE$$

$$f_a(E) = \frac{\sigma_n n_s + \sigma_p n_i \exp\left(\frac{-(E-E_i)}{k_B T}\right)}{\sigma_n \left[n_s + n_i \exp\left(\frac{(E-E_i)}{k_B T}\right) \right] + \sigma_p \left[p_s + n_i \exp\left(\frac{-(E-E_i)}{k_B T}\right) \right]} \quad (4.12)$$

$$f_d(E) = \frac{\sigma_p p_s + \sigma_n n_i \exp\left(\frac{(E-E_i)}{k_B T}\right)}{\sigma_n \left[n_s + n_i \exp\left(\frac{(E-E_i)}{k_B T}\right) \right] + \sigma_p \left[p_s + n_i \exp\left(\frac{-(E-E_i)}{k_B T}\right) \right]}$$

$f_a(E)$ and $f_d(E)$ are the occupation functions of the acceptor and donor traps. Per definition, donor traps are neutral when occupied by an electron and positively charged when unoccupied.

Acceptor traps are neutral, when unoccupied and negatively charged when occupied by an electron.

$$Q_g = -\frac{1}{d_{IL}} \left(\frac{Q_f \times d_{\text{fixed charges}}}{2} + \epsilon_0 \times \epsilon_{IL,r} \times (\psi_s - V_g) \right) \quad (4.13)$$

$d_{\text{fixed charges}}$ is the fixed charge layer thickness.

Figure 4.4 depicts a diagram of the numerical algorithm. More details including the MATLAB code can be found in section C.

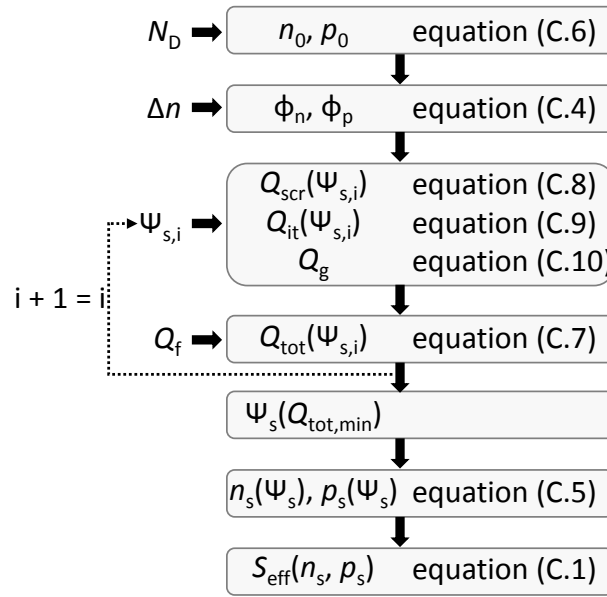


Figure 4.4: Schematic diagram of the numerical algorithm used for the calculation of the surface recombination velocity with input parameters.

CHAPTER 5

Interlayer Stack for Adhesion and Light Coupling into Absorber

5.1 Introduction

Adhesion of the silicon layer on the interlayer stack and of the interlayer stack on the glass substrate is the foundation for the fabrication and characterization of LPC-Si solar cells. The most critical process step for adhesion is the crystallization process whereby the interlayer stack plays a crucial role.

In order to illustrate the importance of the interlayer stack for adhesion during the crystallization process, three samples with glass/IL/silicon structure are prepared. The samples differ in the interlayer stack only and the employed crystallization parameters are the same (heater temperature, crystallization speed, laser power). Thus, adhesion properties can be correlated to the properties of the interlayer stack. Figure 5.1 displays photographs of the three samples.

This chapter is based on

1. N. Preissler, D. Amkreutz, P. Sonntag, M. Trahms, R. Schlatmann, and B. Rech (2017). *Interface Engineering for Liquid-Phase Crystallized Silicon Solar Cells on Glass*. Sol. RRL, 1(3-4):1700015 / DOI 10.1002/solr.201700015

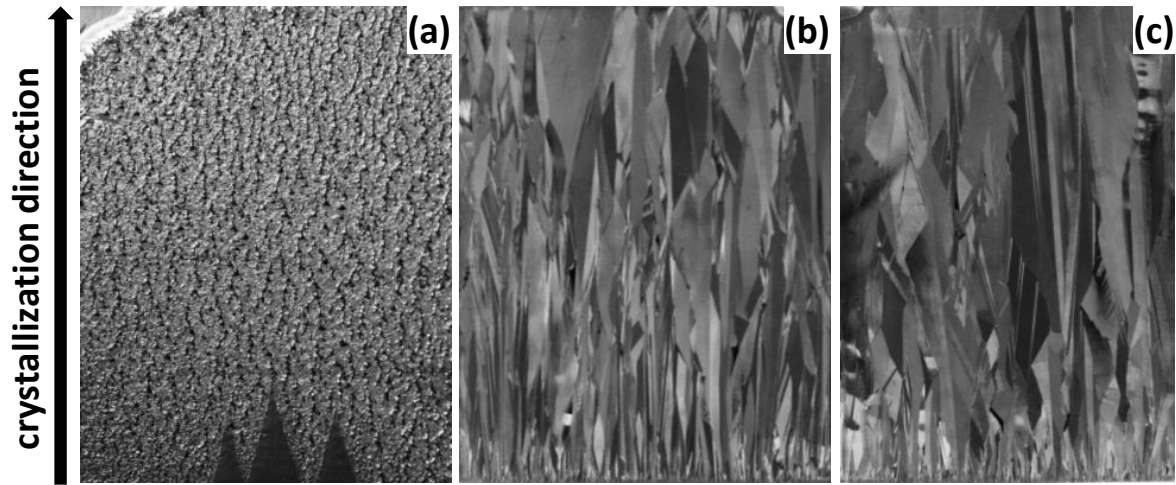


Figure 5.1: Photographs in top view of glass/IL/silicon structures after crystallization. The samples are based on three different interlayer (IL) stacks: (a) and (b) O/N/O with different SiN_x layers and (c) O/N with the same SiN_x as in (b). The SiO_x layer is the same for all three interlayer stacks. In (a), the silicon delaminated during the crystallization process. In (b) and (c), adhesion is observed. Further details are discussed in section 5.2. To increase visibility of grains, the crystallized silicon layers are textured using a potassium hydroxide (KOH)-based solution with Alkatex free+ additive at 80 °C for 3 min, resulting in pyramid sizes of 2-3 μm on the initial [100] surface. The displayed sample area is 4 cm $\times$ 5 cm.

In figure 5.1 (a), the silicon film partly delaminated resulting in a rough surface. Figures 5.1 (b) and (c) depict samples for which adhesion is observed and large laterally grown grains of several centimetres in scanning direction and a few millimetres in width are seen. The size of the grains is similar for the two samples, that are based on different interlayer stacks, indicating that the interlayer stack does not influence the grain size. The layers of the two samples depicted in figures 5.1 (b) and (c) adhere during all subsequent process steps up to finished LPC-Si solar cells.

Interlayer stacks, that are deposited by plasma-enhanced chemical vapor deposition (PECVD), contain hydrogen due to the use of process gases such as monosilane (SiH_4). It was reported, that the amount of hydrogen present in the interlayer stack is of major importance for adhesion, because incorporated hydrogen can rapidly effuse during crystallization which would result in blistering of the silicon [39,40,46]. Therefore, samples based on interlayer stacks deposited by PECVD were annealed for up to 24 h prior to the crystallization process to reduce the hydrogen content in the layers [39,40,46]. However, this step is unwanted, because it increases manufacturing time.

In section 5.2 the question is addressed which properties of the interlayer stack are important to achieve adhesion during the crystallization process. On the one hand glass/IL/silicon stacks are prepared based on different interlayer stacks. It is tested if the layers adhere to the substrate during the crystallization process or if they delaminate. Different forms of dewetting are not distinguished. On the other hand the layers used in the interlayer stacks are deposited as single layers on silicon wafers. These layers are characterized with respect to the stoichiometry and the residual stress, the density of Si-H and N-H bonds, the amount of chemically bonded hydrogen as well as the bonding configuration of hydrogen. Then, the interlayer properties are correlated to the adhesion properties observed for the stacks. The aim is to develop an interlayer stack deposited with PECVD that enables adhesion without the extended annealing step.

The coupling of light into the thin LPC-Si layers is crucial for achieving a maximum number of photons which can be converted into electrons in the silicon material and thus, contribute to a maximum energy conversion efficiency. LPC-Si solar cells are generally illuminated from the glass/interlayer side (superstrate configuration), Thus, the interlayer stack needs to be transparent and non-absorbing for wavelengths between 250 nm (below, the glass is opaque [96]) and 1200 nm (above, silicon, with a band gap of 1.12 eV, does not absorb photons). The optical properties of the dielectric layers developed for adhesion are addressed in section 5.3.

5.2 Interlayer stack for adhesion

The interlayer stack strongly influences the adhesion properties during the crystallization process as demonstrated in figure 5.1 exemplary on basis of three samples. The two samples for which adhesion is observed are based on the same SiN_x layer, while the sample for which delamination is observed is based on another SiN_x layer. The SiO_x layers are the same in all three stacks. This demonstrates the critical role of the SiN_x layer for the wetting characteristics. The two samples with the same SiN_x layer differ such, that one is deposited on an O/N stack while the other is deposited on an O/N/O stack. This demonstrates, that a thin layer sandwiched between the SiN_x and the silicon does not hinder adhesion during the crystallization process. Photographs of more crystallized samples on a broader variety of interlayer stacks can be found in chapter B.

Due to the critical role of the SiN_x layer for adhesion, the properties of this layer are studied in this section. SiN_x layers are grouped into "group A SiN_x ", for which adhesion is observed, and "group B SiN_x ", for which delamination is observed. Throughout this section, group A SiN_x films are coloured in green, while group B SiN_x films are coloured in red.

Figure 5.2 gives an overview on all studied SiN_x layers, sorted according to their refractive index at 632.8 nm ($n_{632.8 \text{ nm}}$) and the corresponding stoichiometry (x). The linear relationship is a consequence of equation (3.5), which is used to translate $n_{632.8 \text{ nm}}$ into x (section 3.2.1).

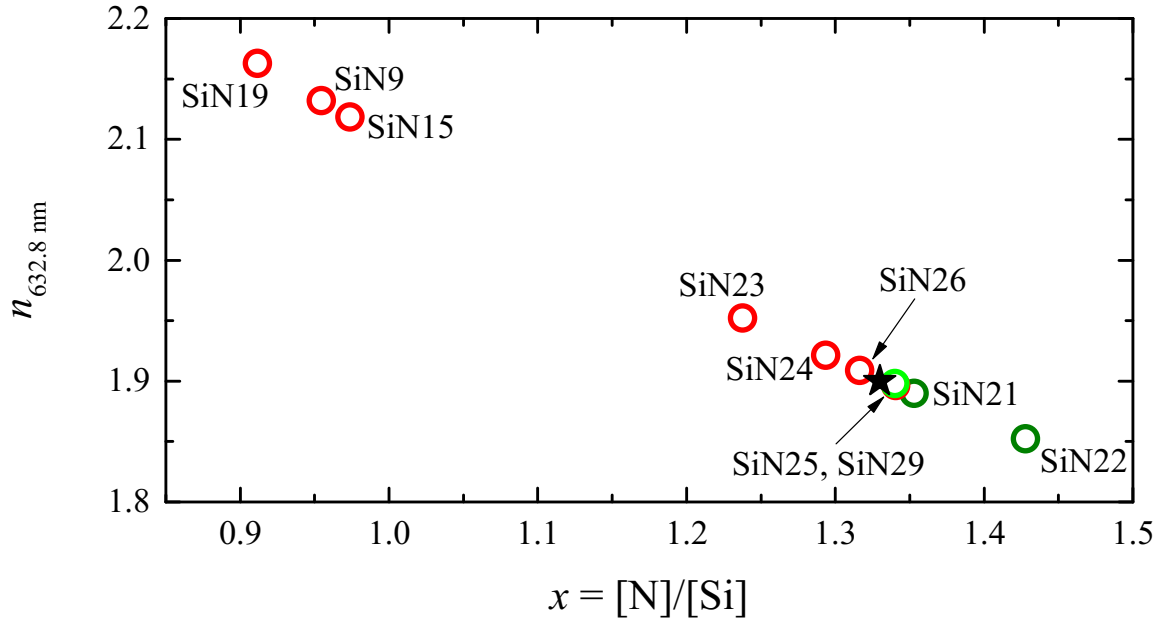


Figure 5.2: Overview on studied SiN_x films in terms of the refractive index at 632.8 nm ($n_{632.8 \text{ nm}}$) and the stoichiometry (x). The layers are distinguished by the assigned nomenclature, for example "SiN15" or "SiN21". Corresponding process conditions are listed in table A.1. The light green circle corresponds to the SiN_x layer called "SiN29", which is not tested for adhesion properties. The black star represents stoichiometric Si_3N_4 [118].

As can be seen in figure 5.2, $n_{632.8 \text{ nm}}$ of the SiN_x films under investigation spans from 1.85 to 2.16. Type A SiN_x films exhibit the lowest $n_{632.8 \text{ nm}}$ and correspondingly, the highest x . Layers with $x < 1.33$ are called silicon-rich and layers with $x > 1.33$ are called nitrogen-rich in the following. Except of the "SiN25" film, all type B SiN_x films are silicon-rich.

The chemical composition of type A and type B SiN_x films is studied using the fourier transform infrared spectroscopy method (section 3.2.2). Figure 5.3 (a) displays the absorption spectra ($\alpha(\omega)$). The focus is on the two peaks dedicated to stretching vibrations of the N-H and Si-H bonds and thus, the spectra are displayed for wave numbers between 3600 cm^{-1} and 1750 cm^{-1} . The N-H and Si-H bonds are used to determine the amount of bonded hydrogen in SiN_x films [80]. Figures 5.3 (b) and (c) show data that are extracted from the spectra in figure 5.3 (a). In (b), the position of peaks representing Si-H and N-H stretching vibrations is depicted. In (c),

the calculated densities of Si-H and N-H bonds as well as of chemically bonded hydrogen are shown.

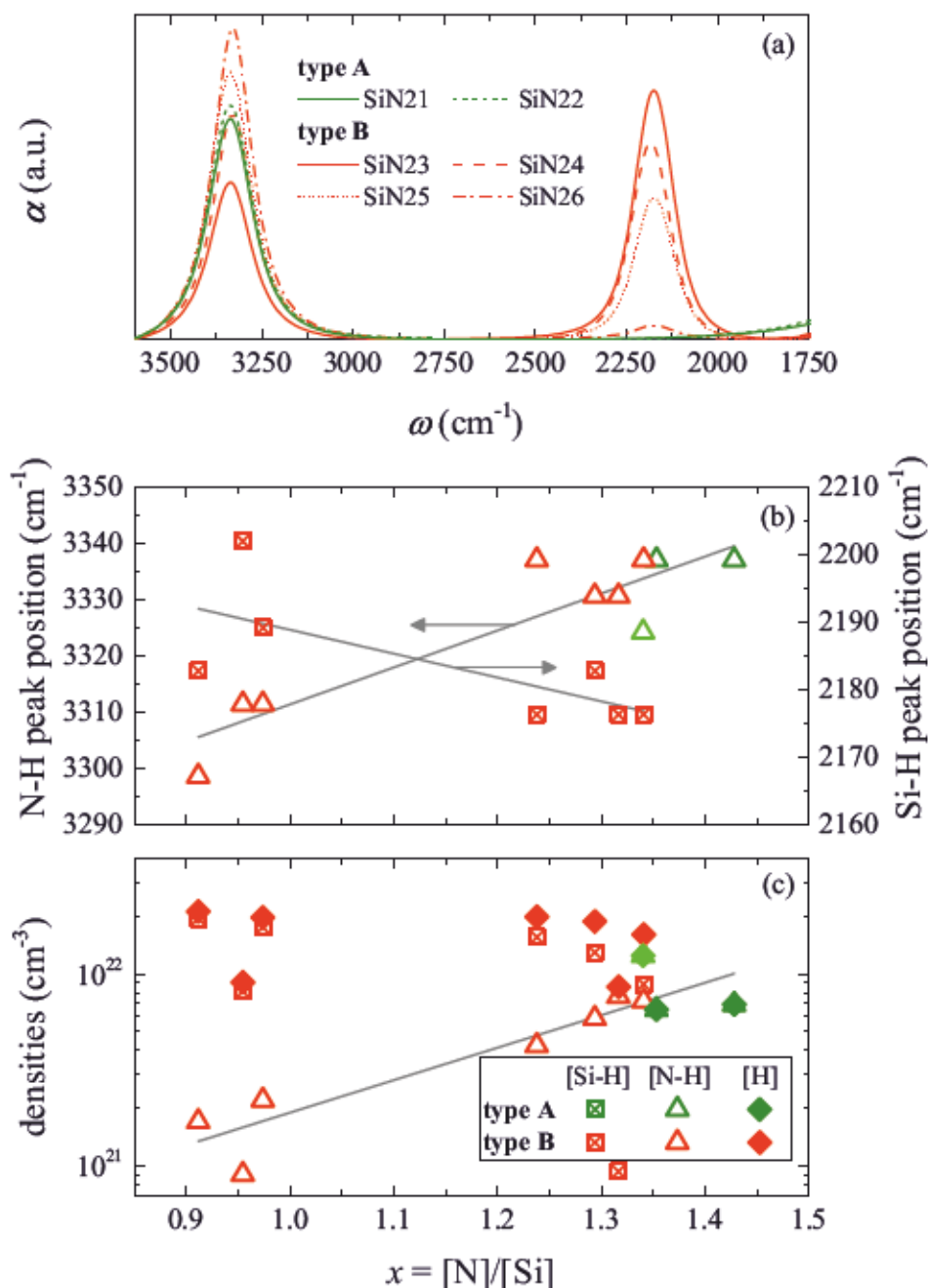


Figure 5.3: Characterization of various type A and type B SiN_x films using the FTIR method. In (a), selected mid-infrared absorption spectra are shown. The selection is done to maintain clarity. In (b), the spectral positions of the N-H and Si-H peaks is depicted. In (c), the calculated densities of the Si-H and N-H bonds as well as of bonded hydrogen is shown. The layers are distinguished by the assigned nomenclature, for example "SiN15" or "SiN21". Corresponding process conditions are listed in table A.1. The light green symbols in (b) and (c) correspond to the SiN_x layer called "SiN29", which is not tested for adhesion properties. Light grey lines represent linear fits to the results to guide the eye.

As can be seen in figure 5.3 (a), the spectrum of all SiN_x films shows a peak between 3600 cm^{-1} to 3000 cm^{-1} corresponding to vibrations of N-H bonds. Type B SiN_x layers (red curves) exhibit an additional peak between 2500 cm^{-1} and 1875 cm^{-1} dedicated to Si-H bonds. The presence of Si-H bonds indicates a silicon-rich nature of the SiN_x films while the absence of the peak in the type A SiN_x spectra indicates nitrogen-rich films [80,119,120] which is in line with the refractive index of the layers (figure 5.2).

As can be seen in figure 5.3 (b), absorption peaks dedicated to stretching vibrations of N-H bonds are centered between 3340 and 3300 cm^{-1} while peaks caused by stretching vibrations of Si-H bonds are centred between 2200 and 2175 cm^{-1} . Data points corresponding to the Si-H peak position of type A SiN_x films and the "SiN29" film cannot be seen because these bonds are not present in these films. The position of the peak related to N-H vibrations shifts towards higher wave numbers with increasing x , as was also observed in literature [79,80] underlining the nitrogen-rich nature of type A SiN_x films as well as the silicon-rich nature of the majority of type B SiN_x films. The position of the peak related to Si-H bonds shifts towards lower wave numbers with increasing x which is also observed in literature [79].

Figure 5.3 (c) shows the densities of Si-H and N-H bonds as well as the density of chemically bonded hydrogen. With increasing x , the N-H bond density increases. The same trend was observed for other SiN_x films deposited with the PECVD method [87]. The Si-H bond density does not show a clear trend with the stoichiometry. Except of one point, the density of Si-H bonds scatters between $8 \times 10^{21}\text{ cm}^{-3}$ and $2 \times 10^{22}\text{ cm}^{-3}$. The outlier represents the Si-H peak of the film "SiN26" and it can be seen in figure 5.3 (a) that the peak area is very small.

As proposed in [80,121], the density of chemically bonded hydrogen is the sum of the Si-H and N-H stretching bond densities. It follows, that the total amount of bonded hydrogen in type A SiN_x films ($\approx 7 \times 10^{21}\text{ cm}^{-3}$) is slightly lower as compared to type B SiN_x films ($\approx 9 - 20 \times 10^{21}\text{ cm}^{-3}$). However, due to the rather small difference in [H] between type A and B films, it is proposed that the total amount of bonded hydrogen is not crucial for adhesion.

It is known from literature that plasma-deposited nitrogen-rich SiN_x films are thermally more stable upon annealing as compared to silicon-rich films which was related to a more flexible molecular network in nitrogen-rich SiN_x [120]. Furthermore, it was demonstrated that silicon-rich films release a higher hydrogen concentration beginning at $400\text{ }^\circ\text{C}$ much faster as compared to nitrogen-rich films [122,123]. The enhanced desorption of hydrogen from silicon-rich layers is partially related to the lower Si-H binding energy (3.3 eV [124]) as compared to the N-H binding energy (4.0 eV [124]) [123]. Considering these observations in combination with the results presented above it is concluded that the less flexible structure as well as enhanced hydrogen desorption from the silicon-rich type B SiN_x films as compared to type A SiN_x films seems, at least partly, responsible for the observed delamination during crystallization. Due to

the small difference in the density of incorporated hydrogen of type A and type B films it is proposed that the amount of bonded hydrogen is not as critical for adhesion.

It was shown in literature, that the residual stress (σ_f) in SiN_x films on top of silicon wafers can lead to buckeling or delamination of the SiN_x [125, 126]. Thus, the residual stress in type A and type B SiN_x films might also influence adhesion properties during the crystallization process. In the following, the SiN_x films are characterized and compared with respect to the residual stress. As a reference, the stress of a silicon nitride layer is measured that is used in an O/N/O interlayer stack deposited with reactive RF-sputtering. This interlayer stack allows for adhesion of glass/O/N/O/LPC-Si stacks during crystallization [19, 47]. The sputtered silicon nitride layer is characterized by a compressive residual stress of around 140 MPa.

Figure 5.4 displays the residual stress (σ_f) of the SiN_x layers as a function of the stoichiometry (x).

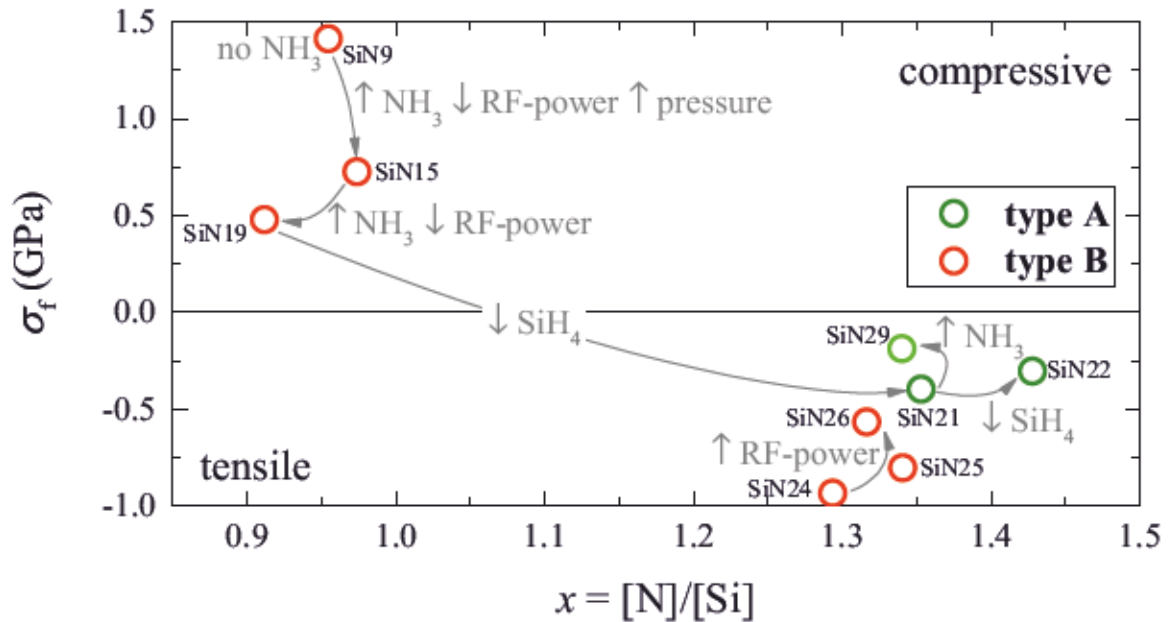


Figure 5.4: Characterization of various type A and type B SiN_x films in terms of the residual stress (σ_f). Nomenclatures of the SiN_x films is indicated. Corresponding process conditions are listed in table A.1. The light green symbol corresponds to the SiN_x layer called "SiN29", which is not tested for adhesion properties. Light grey arrows indicate variations of specific PECVD process conditions, while the other process parameters remained unchanged.

The layer named "SiN9" was the first layer investigated in terms of the residual stress in the framework of this thesis. The residual stress of this layer is high (1.4 GPa, compressive).

The residual stress in the reference layer is almost one order of magnitude lower. Thus, it is likely that the residual stress in the "SiN9" film is at least partly responsible for the observed delamination of the silicon film during the crystallization process (figure B.1).

It is known from literature that the residual stress of SiN_x films can be tuned over a wide range by changing the PECVD deposition parameters [87, 126, 127]. This is also evident from the presented results in figure 5.4, in which the variation of selected PECVD process conditions is highlighted.

The "SiN9" layer is deposited without NH_3 in the process gas mixture. The nitrogen in the layer originates from nitrogen (N_2) process gas molecules. It is found that by adding NH_3 to the process gas mixture and reducing the RF-power, the residual stress is reduced from 1.4 GPa (compressive) to around 500 MPa (compressive) ("SiN19"). Despite the reduction of the film stress the "SiN15" and "SiN19" layers lead to delamination of the silicon during the crystallization process (figure B.1). For the "SiN19" film parasitic absorption is also observed as discussed in section 5.3 (figure 5.7). Overall, "SiN15" and "SiN19" are not suitable for the interlayer stack in LPC-Si solar cells.

Reducing the SiH_4 flow rate of the "SiN19" film (4 sccm) to 3 sccm ("SiN21") or 2 sccm ("SiN22") results in SiN_x layers with tensile residual stress below 400 MPa. For these films, adhesion is observed (figures 5.1 (b) and (c)).

The strong influence of the RF-power on the residual stress is highlighted by the films "SiN24", "SiN25" and "SiN26". By increasing the RF-power from 70 W ("SiN24") to 160 W ("SiN26") the tensile residual stress decreases from 940 MPa ("SiN24") to 570 MPa ("SiN26"). This can be explained as follows. A higher RF-power leads to a higher dissociation of gases, which leads to more N^+ species in the plasma and therefore, an increased incorporation of nitrogen in the film. As evident from figure 5.3 (c), with increasing RF-power, an increasing N-H bond density is observed. A higher amount of nitrogen results in the expansion of the film's matrix and an increase in the compressive stress [126, 128, 129]. The higher compressive stress compensates the tensile stress in the SiN_x film and leads to an overall lower tensile stress, which is in line with the results obtained for the films "SiN24", "SiN25" or "SiN26" (figure 5.4).

The crystallization is not successful when the "SiN24", "SiN25" or "SiN26" layers are used in O/N/O interlayers in glass/IL/LPC-Si stacks. However, wetting properties are better when the "SiN26" film with reduced residual stress and lower Si-H bond density is used than the "SiN24" film as can be seen in figure 5.5.

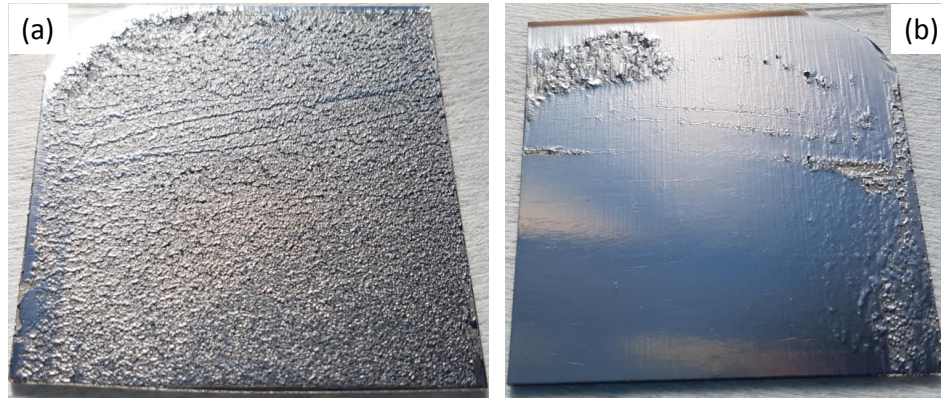


Figure 5.5: Photographs in top view of glass/IL/silicon structures. The samples are based on O/N/O interlayer (IL) stacks which differ only in the SiN_x film: (a) "SiN24" and (b) "SiN26". The displayed sample area is $5 \text{ cm} \times 5 \text{ cm}$.

By further increasing the RF-power of the "SiN26" film it might be possible to obtain another type A SiN_x layer.

As discussed above, incorporation of nitrogen increases the compressive residual stress in SiN_x films and that the RF-power can be used to increase the amount of incorporated nitrogen. Another option to increase the amount of incorporated nitrogen while maintaining zero Si-H bonds is to increase the NH_3 flow rate from 3.5 sccm ("SiN21") layer to 10 sccm ("SiN29") as evident from figure 5.3 (c). Accordingly, it is found that the increase in NH_3 flow rate decreases the residual stress to 189 MPa (tensile) (figure 5.4). The data corresponding to the "SiN29" film are coloured in light green because this layer is not tested for adhesion properties in glass/IL/LPC-Si stacks. The "SiN29" is a promising candidate for a type A film.

Please note, that the residual stress in the SiN_x films might be different when the layers are deposited on glass instead of a silicon wafer, because the coefficient of thermal expansion (CTE) in SiN_x films ($2.8 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$ [126]) is less than in glass ($3.76 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$) but higher than in the silicon wafer ($2.6 \times 10^{-6} \text{ }^\circ\text{C}^{-1}$) [84]. This difference affects the thermal stress (σ_{th}) and with that the residual stress (section 3.2.3). Nonetheless, the presented results can be used to develop SiN_x films on silicon wafers and then incorporate them in glass/IL/LPC-Si stacks.

The development of the SiN_x layer with respect to adhesion properties results in the selection of one SiN_x film ("SiN21"). This layer, in combination with the "SiO19" film, enables adhesion without extended annealing treatments prior to the crystallization process.

Adhesion is examined also on a microscopic scale using transmission electron microscopy. Glass/IL/LPC-Si samples with O/N and O/N/O interlayer stacks based on the "SiN21" and

"SiO19" films are prepared as described in section 3.1.6. Figure 5.6 shows corresponding images of the region between the interlayer stack and the LPC-Si absorber.

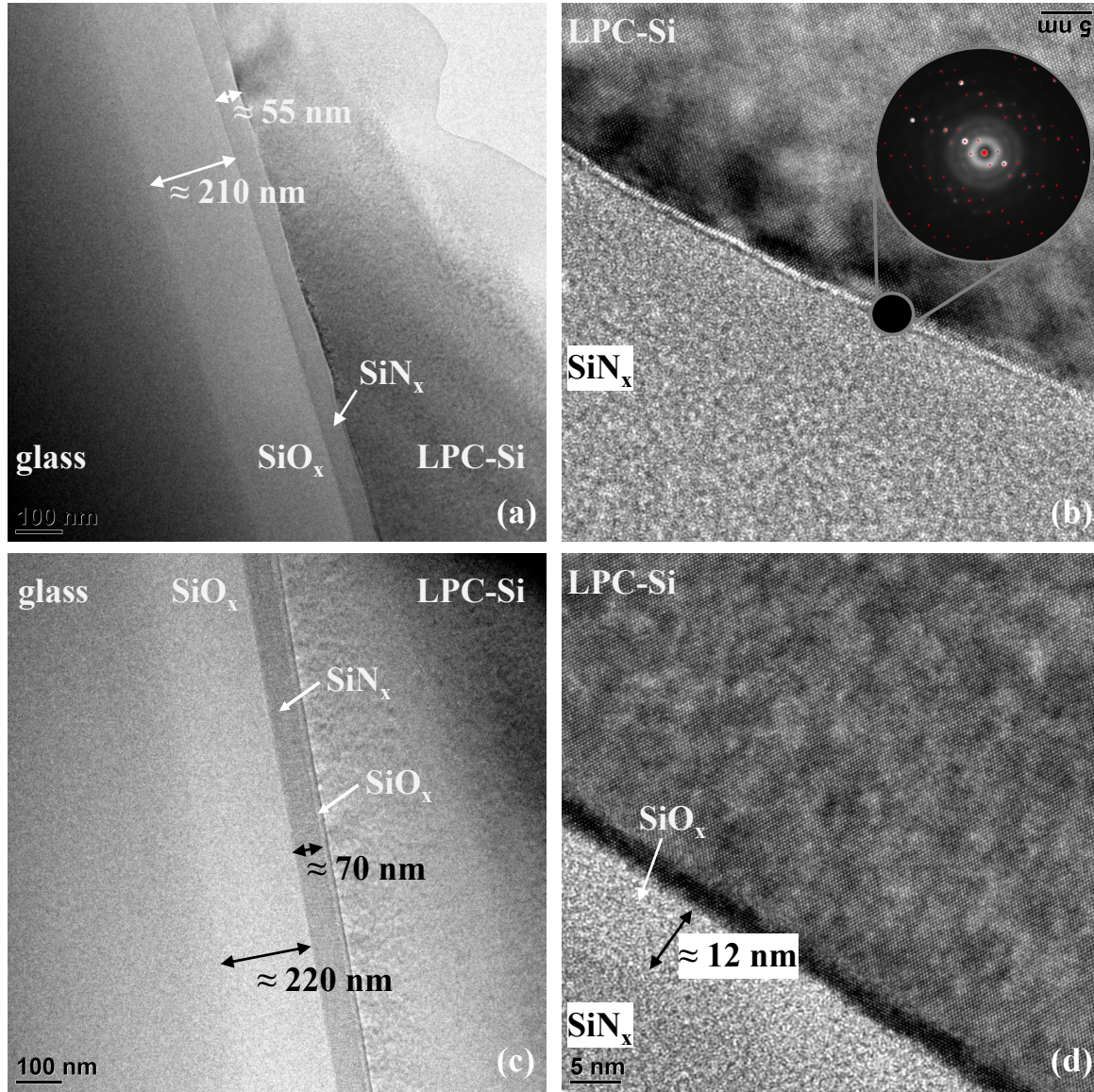


Figure 5.6: Transmission electron microscopy images of the interface region between the interlayer stack and LPC-Si for the microscopic analysis of adhesion properties with developed SiN_x film ("SiN21") and SiO_x film ("SiO19"). The inset in (b) depicts a measured electron diffraction pattern overlaid with a simulated diffraction pattern for crystalline silicon (red features).

As can be seen, the layers are well defined and the interfaces are smooth. The silicon adheres on top of the interlayer stack. The silicon is crystallized up to the interlayer as demonstrated by

the excellent overlap of the measured and simulated diffraction pattern. Smeared out circles are attributed to the amorphous interlayer.

5.3 Interlayer stack for light coupling into absorber

The SiN_x and SiO_x layers that are selected in the previous section 5.2 due to their suitable properties with respect to adhesion are now examined with respect to their optical properties.

Figures 5.7 (a) and (b) display the refractive index (n) and the extinction coefficient (k) of the SiN_x ("SiN21") and SiO_x ("SiO19") films as a function of the wavelength, respectively. The results of a SiO_xN_y film deposited with PECVD are included as well to serve as an example for an SiO_xN_y layer because in figure 6.5 it is shown that a SiO_x film deposited on top of the SiN_x film has a SiO_xN_y -like character. This is related to nitrogen diffusion from the SiN_x into the SiO_x during the deposition process at elevated temperatures.

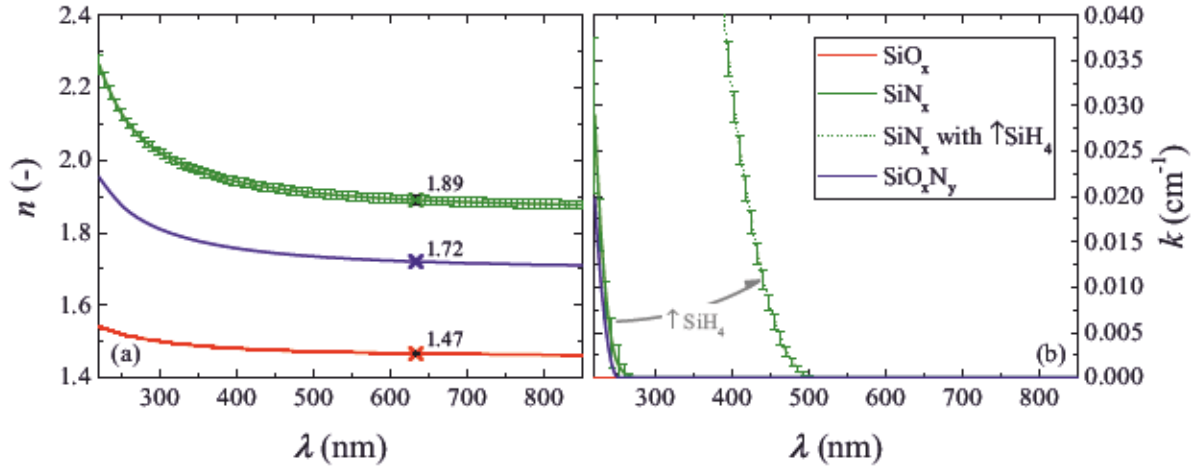


Figure 5.7: Spectra of (a) the refractive index (n) with $n_{632.8\text{ nm}}$ highlighted and (b) the extinction coefficient (k) of SiN_x and SiO_x films developed for the interlayer in LPC-Si solar cells. The curves of a SiO_xN_y film are included as well as the $k(\lambda)$ spectra of a SiN_x deposited with increased SiH_4 flow rate (dashed line). Error bars represent the standard deviation of five sample pieces of one deposition run, except the SiO_xN_y film which represents only one sample piece.

The films exhibit normal dispersion, this is, an increase of the refractive index towards shorter wavelengths. As can be seen, the refractive index of the SiO_x film varies between 1.46 and 1.54, and it varies between 1.88 and 2.28 in case of the SiN_x film. The refractive index of the SiO_xN_y film is in between the one of the SiO_x and the SiN_x .

At 632.8 nm, the refractive index of the SiO_x , the SiO_xN_y and the SiN_x layer is 1.47, 1.72 and 1.89, respectively. The SiO_x film is optically indistinguishable from the glass (at 632.8 nm, $n_{\text{glass}} \approx 1.5$ [96]). Thus, if the SiO_x layer is deposited on top of the glass substrate its thickness is not critical to achieve a suitable optical performance. In order to have a sufficient diffusion barrier for impurities from the glass substrate, the thickness of the SiO_x adjacent to the glass is set to around 210 nm (figure 5.6). The SiN_x films serves the purpose of an anti-reflection coating, because its refractive index can be tuned for optimum anti-reflection properties ($n_{632.8 \text{ nm}} = 2.4$ for zero reflection at 632.8 nm as discussed in section 4.1). Thus, the refractive index of the developed SiN_x layer is too low. However, the nitrogen-rich character of the layer is important to achieve adhesion without annealing the sample prior to crystallization as discussed in section 5.2.

The extinction coefficient of the SiO_x film is zero for wavelengths between 220 nm and 850 nm. This is also observed for the SiN_x film, except that the extinction coefficient increases for wavelengths below 260 nm. The absorption of the SiN_x film is significantly increased when the SiH_4 flow rate is increased from 3 sccm ("SiN21") to 4 sccm ("SiN19") as can be seen in figure 5.7 (b). The "SiN19" film appears yellow when deposited on a glass substrate.

Next, the optical properties of the developed SiO_x and SiN_x layers are investigated, when the films are incorporated as O/N/O interlayer stack in LPC-Si solar cells.

First, reflection and transmission losses of a structure composed of glass/ SiO_x / SiN_x / SiO_x /LPC-Si/(i) a -Si:H/(p) a -Si:H/ITO are simulated using ASPIN3 [88]. The layers are planar and the absorber has a thickness of 14.7 μm . Illumination is from the glass side. Please refer to section 3.3 for further details. Figure 5.8 displays simulated results, whereby the thickness of one of the layers (except the emitter layers) is varied while the others are kept constant.

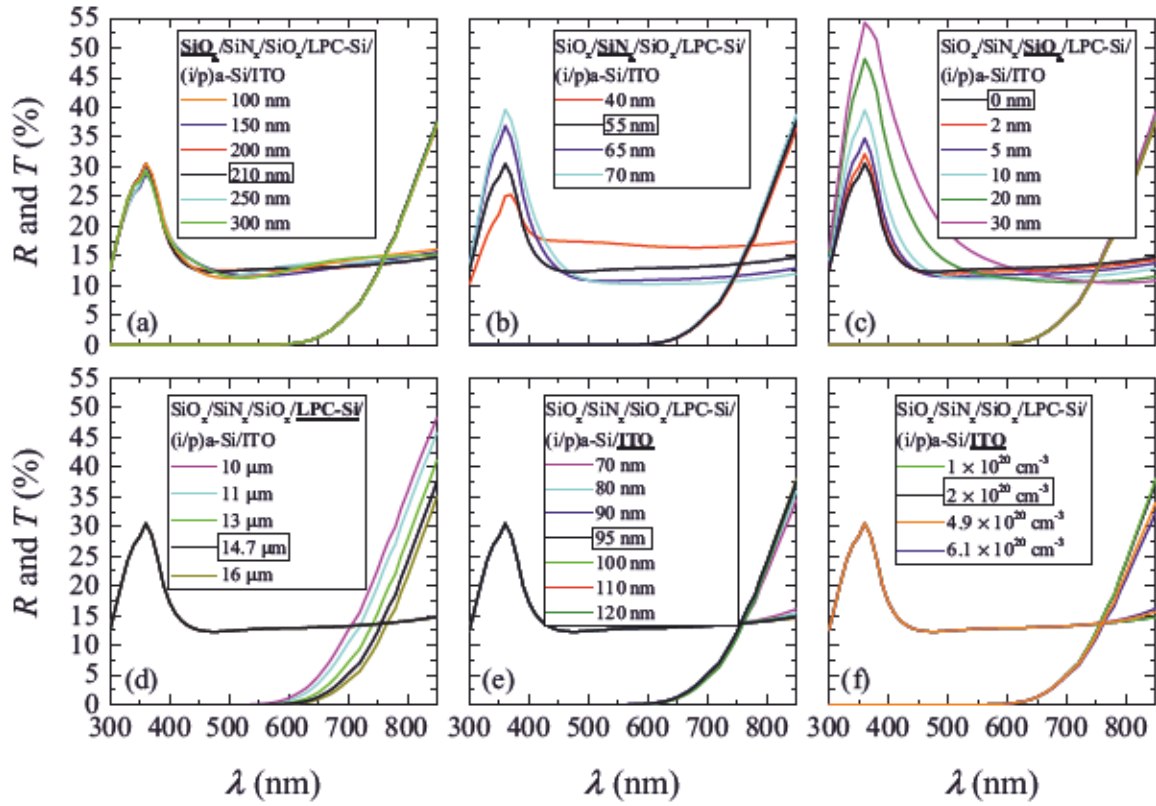


Figure 5.8: Simulated reflection and transmission losses of a structure composed of $\text{SiO}_x/\text{SiN}_x/\text{SiO}_x/\text{LPC-Si}/(\text{i})\text{a-Si:H}/(\text{p})\text{a-Si:H}/\text{ITO}$ as a function of the wavelength. Layer thicknesses are varied: (a) SiO_x adjacent to the glass substrate, (b) SiN_x , (c) SiO_x adjacent to the silicon, (d) LPC-Si, (e) ITO. In (f), the doping concentration of the indium-tin-oxide (ITO) layer is varied, whereby $n(\lambda)$ and $k(\lambda)$ data are taken from [90]. The parameters used for the base case are framed. ASPIN3 is employed for the simulations (section 3.3).

The influence of the thickness of the SiO_x layer adjacent to the glass substrate on reflection is negligible as expected from the $n(\lambda)$ and $k(\lambda)$ data in figure 5.7. With increasing SiN_x thickness, reflection losses at short wavelengths below around 500 nm increase, while at longer wavelengths the losses decrease. The strongest influence on reflection in the short-wavelength range is observed for the SiO_x film adjacent to the LPC-Si absorber. By varying the thickness from 0 to 30 nm, reflection increases from around 30 % to above 50 % at 360 nm.

Transmission losses become relevant for wavelengths greater than 600 nm and are not influenced by the thicknesses of the layers in the interlayer stack. These losses are attributed to the decreasing absorption coefficient of the silicon absorber layer for longer wavelengths [91]. Accordingly, transmission losses are significantly influenced by the thickness of the absorber as

can be seen in figure 5.8 (d). The properties of the ITO layer at the rear side of the cell have a small influence on the transmission losses as evident from figures 5.8 (e) and (f).

Finally, LPC-Si solar cells are fabricated based on the developed SiN_x and SiO_x layers and reflection and transmission is measured in superstrate configuration. Figure 5.9 (a) displays corresponding transmission and reflection spectra.

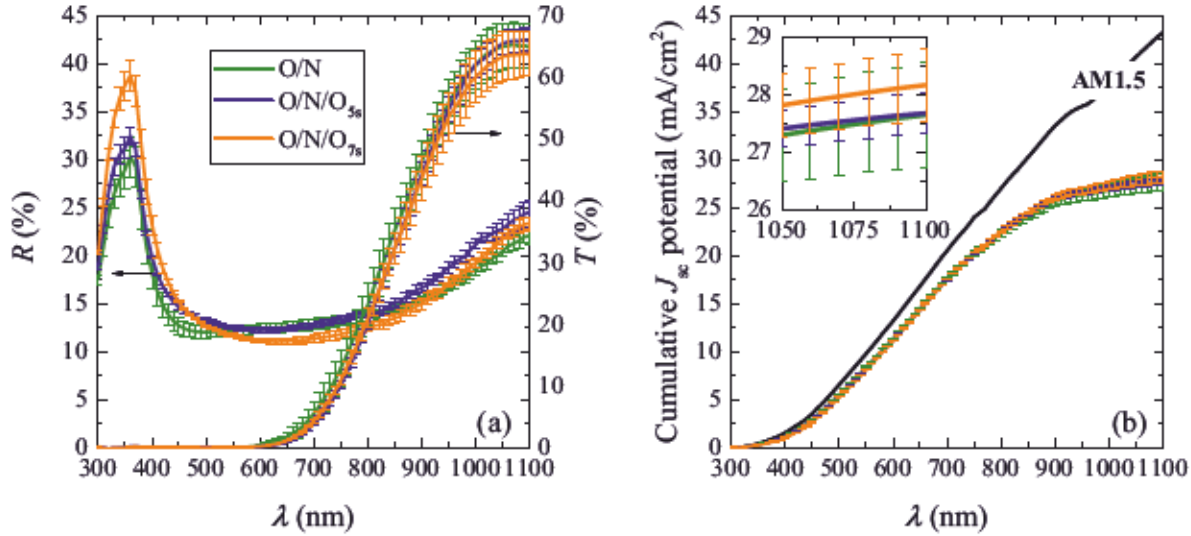


Figure 5.9: Measured (a) transmission and reflection spectra as well as (b) the calculated cumulative J_{sc} potential as a function of the wavelength. The layers are planar. The index in the legend depicts the deposition time used for the SiO_x layer adjacent to the silicon. Error bars stem from measurements of at least ten solar cells positioned randomly on each of the three $5\text{ cm} \times 5\text{ cm}$ samples.

As can be seen, measured curves (figure 5.9) follow the same trends as simulated curves (figure 5.8). In the short-wavelength region ($< \approx 550\text{ nm}$), reflection losses are strongly affected by the interlayer stack whereby losses can be reduced when the thickness of the SiO_x adjacent to the LPC-Si is reduced. Exemplary, at 360 nm , for the cell with the O/N/O_{7s} stack almost 40 % is lost upon reflection while the cell with the O/N stack results in 30 % reflection losses. However, for wavelengths between 550 nm and 850 nm , reflection losses are slightly lower when the thickness of the SiO_x layer adjacent to the silicon is increased.

At 1100 nm , up to 70 % of the incident light is lost due to transmission. These optical losses can be reduced when a reflector, for example a silver layer, is deposited at the rear-side of the cell. Furthermore, the rear-side of the absorber can be textured to increase reflection of light back into the absorber. Both these features are used in IBC cells as described in section 2.3.

Based on the transmission and reflection properties, the cumulative short-circuit current density (J_{sc}) potential is calculated, which would result if only optical losses are considered, i.e.

if losses due to recombination in the LPC-Si material and parasitic absorption in other layers than the absorber are neglected (figure 5.9 (c)). These current values are the maximum possible short-circuit current density with these types of interlayer stacks and without any features to enhance light coupling into the absorber.

As can be seen, the AM1.5 spectrum delivers in total around 43 mA/cm² in the wavelength range between 300 nm and 1100 nm. The studied LPC-Si samples can harvest between 27.5 mA/cm² to 28.1 mA/cm², i.e. between 64 to 65 %. The J_{sc} potential is marginal higher with the O/N/O_{7s} as compared to the other two stacks, despite the higher reflection losses at short wavelengths. This is due to the low photon flux at short wavelengths in the AM1.5 spectrum.

5.4 Conclusions

Glass/IL/silicon structures with different interlayer stacks are tested for adhesion during the crystallization process and the crucial role of the interlayer stack, in particular of the SiN_x layer, is demonstrated. It is observed that studied interlayer stacks, that enable adhesion, do not influence the grain size of crystallized silicon films.

Due to its important role, the focus of the interlayer development is put on the SiN_x film.

The SiN_x films, that enable adhesion of the silicon during the crystallization process, are nitrogen-rich, while most of the films that result in delamination are silicon-rich. This is demonstrated based on refractive indices obtained from ellipsometry measurements and the analysis of mid-infrared absorption spectra.

The total amount of bonded hydrogen is only slightly lower ($\approx 7 \times 10^{21} \text{ cm}^{-3}$) in films that enable adhesion as compared to films, that result in delamination ($\approx 9 - 20 \times 10^{21} \text{ cm}^{-3}$). Due to the rather similar values the amount of bonded hydrogen does not seem to be critical for adhesion.

The most critical parameter for adhesion is the bonding configuration of hydrogen in the layers. If hydrogen is bonded to nitrogen only, adhesion is observed. If hydrogen is also bonded to silicon atoms, then the layers delaminate.

The residual stress in the SiN_x films might also play a role for adhesion. Films that exhibit a high residual stress (more than 500 MPa compressive or tensile) lead to delamination. Films that result in adhesion, are characterized by a residual stress below 400 MPa (tensile).

Overall it is found that in order to obtain adhesion, SiN_x layers on silicon wafers should exhibit a residual stress below 400 MPa and no Si-H bonds.

Reflection losses depend on the thickness of the SiO_x layer adjacent to the LPC-Si absorber. The layer should be as thin as possible to reduce losses in the short-wavelength regime, while a thicker layer leads to reduced losses in the longer wavelength regime. The overall impact on the maximum extractable current by the cell is found to be very little for the investigated layer thicknesses. Therefore, the thickness of the layer adjacent to the silicon can be adjusted to maximize the passivation quality at the buried absorber surface which has a stronger influence on cell performance as discussed in the next chapter 6.

CHAPTER 6

IL/LPC-Si Interface Passivation and LPC-Si Solar Cell Performance

6.1 Introduction

In this chapter, the electrical properties of LPC-Si samples on glass are addressed. The focus is on the passivation quality at the interface between the interlayer stack and the LPC-Si layer. Results are correlated to the electrical performance of corresponding fully functional LPC-Si solar cells.

The passivation quality at the interface between a dielectric layer and a silicon wafer was extensively investigated in the past and widespread literature is available. For example, it was found that SiN_x films exhibit in general a high fixed charge density and passivate silicon surfaces by the separation of majority and minority charge carriers while SiO_x films passivate interface defect states effectively as described in section 4.2. In LPC-Si samples on glass, the dielectric layers used for the passivation of the buried LPC-Si surface are sandwiched between glass and silicon and during the crystallization process, the films face molten silicon with temperatures above 1400 °C. Therefore, it is not clear whether the observations made for the

This chapter is based on

1. [N. Preissler](#), J. A. Töfflinger, I. Shutsko, O. Gabriel, S. Calnan, B. Stannowski, B. Rech, and R. Schlatmann (2016). *Interface Passivation of Liquid-Phase Crystallized Silicon on Glass Studied with High-Frequency Capacitance-Voltage Measurements*. Phys. Status Solidi A, 213(7):1697-1704 / DOI 10.1002/pssa.201532957
2. [N. Preissler](#), J. A. Töfflinger, O. Gabriel, P. Sonntag, D. Amkreutz, B. Stannowski, B. Rech and R. Schlatmann (2017). *Passivation at the interface between liquid-phase crystallized silicon and silicon oxinitride in thin film solar cells*. Prog. Photovolt: Res. Appl., 25(7):515-524 / DOI 10.1002/pip.2852
3. [N. Preissler](#), C. Thi Trinh, M. Trahms, P. Sonntag, D. Abou-Ras, H. Kirmse, R. Schlatmann, B. Rech, and D. Amkreutz. *Impact of Dielectric Layers on Liquid-Phase Crystallized Silicon Solar Cells*. Accepted for publication in IEEE Journal of Photovoltaics

dielectric layer/silicon wafer interface apply for the interface between the interlayer stack and LPC-Si as well.

The passivation quality is quantified in terms of the effective surface recombination velocity (S_{eff}). For silicon wafers, S_{eff} can be determined via the bulk lifetime (τ_b) which can be measured using for example the QSSPC technique [41, 55, 56]. The mathematical expressions for the conversion of τ_b into S_{eff} are supplied in, for example, [57].

In thin crystalline silicon films on glass it is difficult to determine τ_b and S_{eff} by experimental means. For example, the QSSPC method cannot be applied, because of a low signal-to-noise ratio due to the small amount of material, due to depletion region modulation effects [58, 59] and due to a high number of bulk defects [60]. On top of that, the interface between the interlayer stack and the LPC-Si absorber is difficult to access, because one side of the interface is blocked by the glass substrate.

The effective surface recombination velocity at the IL/LPC-Si interface (named effective front-side surface recombination velocity ($S_{\text{eff,front}}$) in this thesis) is commonly estimated using simulation packages such as AFORS-HET, ASPIN3 and TCAD SentaurusTM to model measured solar cell results [19, 34, 46, 53, 61, 62]. An insight into specific passivation mechanisms was not achieved with these methods. For example, the defect state density at the interface was not known. Among others, it was demonstrated, that the post-deposition hydrogen plasma treatment enhances the effective front-side surface recombination velocity at the IL/LPC-Si interface [46, 61]. However, the underlying mechanism was unclear in the past.

In this thesis, the passivation quality at the buried IL/LPC-Si interface is studied in terms of the interface defect state density (D_{it}) and the effective interlayer charge density ($Q_{\text{IL,eff}}$). To this end, MIS structures are prepared as described in section 2.4 and measured capacitance-voltage curves are evaluated as demonstrated in section 4.3. Based on D_{it} and $Q_{\text{IL,eff}}$, $S_{\text{eff,front}}$ can be calculated based on the extended Shockley-Read-Hall (SRH) formalism.

In section 6.2, the post-deposition hydrogen treatments at elevated temperatures are addressed. It is studied, how such treatments influence on the one hand D_{it} and $Q_{\text{IL,eff}}$ at the buried interface and on the other hand the open-circuit voltage of LPC-Si test cells. The solar cell performance is correlated to the interface passivation.

In section 6.3, the SiO_x and SiN_x layers that resulted from the development with respect to adhesion and optics (chapter 5) are tested as passivation layers in O/N and O/N/O interlayer stacks. In the first part of the section, the focus is on the interface passivation, whereby the influence of the thickness of the SiO_x adjacent to the absorber is highlighted. The effective front-side surface recombination velocity provided by the O/N and O/N/O interlayer stack is calculated and compared to published results for LPC-Si solar cells on glass as well as

silicon wafers. In the second part of the section, the O/N and O/N/O interlayer stacks are implemented in LPC-Si test cells and the cell performance is compared. Measured EQE curves on the two stacks are modelled using ASPIN3, whereby the effective front-side surface recombination velocity, that is obtained from the investigation of the interfaces by means of the C-V technique, is used as input parameter. The second input parameter, namely the SRH bulk lifetime (τ_b) of minority charge carriers, is adjusted to fit measured curves. Based on $S_{\text{eff,front}}$ and τ_b , the effective minority charge carrier diffusion length is calculated and compared to literature results. At the end of section 6.3, the O/N and O/N/O interlayer stacks are critically evaluated taking into account the obtained results.

In section 6.4, the interlayer stack based on the developed SiO_x and SiN_x layers is further developed by considering the determined passivation mechanism as well as technological aspects. The developed stack is tested in LPC-Si test cells.

The performance of IBC LPC-Si solar cells on the developed stacks is compared among each other as well as in the context of cell results presented in literature.

Finally, it is evaluated, which factor - the front-side interface quality, the LPC-Si bulk quality or the rear-side interface quality - limits the performance of LPC-Si solar cells based on the developed interlayer stack. To this end, the open-circuit voltage and the short-circuit current density are simulated as a function of $S_{\text{eff,front}}$ covering a perfect front-side passivation quality (1 cm/s) up to a miserable front-side passivation quality (10^5 cm/s). The bulk lifetime is varied as well.

6.2 Post-deposition hydrogen treatments at elevated temperatures

From literature it is known that a post-deposition hydrogen plasma treatment at 400 °C for 30 min improves the passivation quality at the IL/LPC-Si interface. In this section, this aspect is investigated in more detail.

Two types of samples are fabricated. MIS structures are prepared as described in section 2.4 and LPC-Si test cells are prepared as described in section 2.3. All samples are based on a glass/Mo/IL/LPC-Si sequence with N/O/ON (20/100/80 nm) interlayer stack. As reference, test cells without molybdenum layer are prepared. These have a slightly different interlayer stack (N/O/N/ON (10/200/60/20 nm)) as compared to the cells with molybdenum layer. All samples have an absorber deposited with the PECVD method. The as-deposited absorber thickness is 5 μm which is reduced to 4.3 μm due to wet-chemical treatments. The absorber is n-doped with a doping concentration of $N_D \approx 1.1 \times 10^{17} \text{ cm}^{-3}$ for the samples with molybdenum layer and $N_D \approx 1.8 \times 10^{17} \text{ cm}^{-3}$ for the samples without molybdenum layer.

The samples are subjected to the following post-deposition treatments (table 6.1): One sample is subjected to a 30 min-long hydrogen plasma treatment with a plateau substrate temperature of 400 °C (Hpla30). Another sample experiences the same treatment except for a shorter process duration of 15 min (Hpla15). A third sample is annealed in hydrogen atmosphere only, this is, the plasma is not ignited (H30) and a fourth sample remains untreated.

Table 6.1: Different post-deposition hydrogen treatments at elevated temperatures. The plateau heater temperature, the process duration and the nomenclature is shown.

treatment	nomenclature
none	untreated
400 °C, 30 min	H30
400 °C, 15 min and hydrogen plasma	Hpla15
400 °C, 30 min and hydrogen plasma	Hpla30

6.2.1 IL/LPC-Si interface passivation

High-frequency capacitance-voltage (C - V) curves are recorded in relaxation mode on several MIS structures on one sample and analysed with respect to parasitic processes as described in section 3.1.7. For the determination of the interface defect state density and the effective interlayer charge density, C - V curves are selected for which no parasitic processes are observed.

Figures 6.1 (a) and (b) display the interface defect state density at mid gap energy ($D_{it, MG}$) and the effective interlayer charge density ($Q_{IL, eff}$) at the IL/LPC-Si interface, respectively, for the different post-deposition treatments listed in table 6.1.

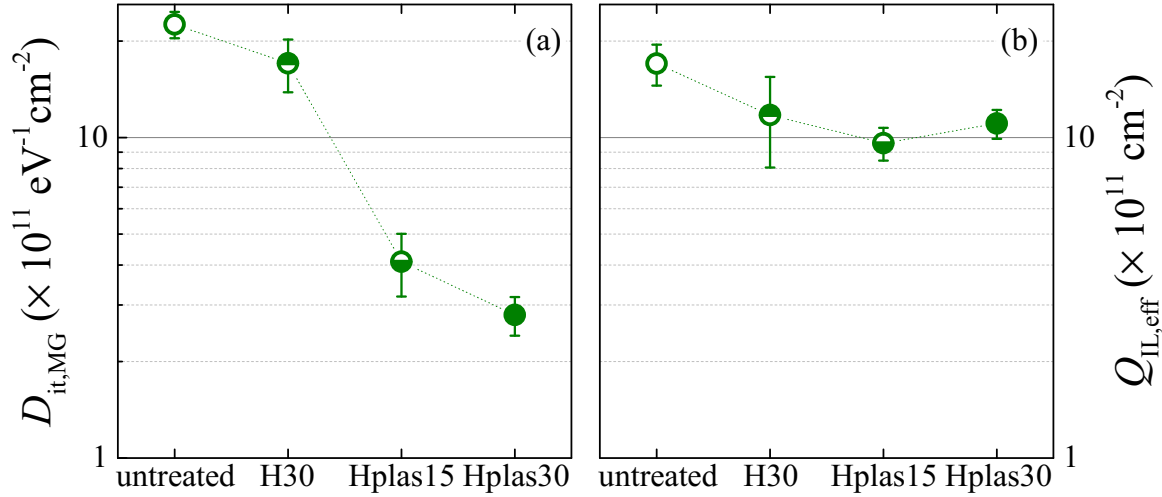


Figure 6.1: (a) $D_{it,MG}$ and (b) $Q_{IL,eff}$ of MIS samples with N/O/ON interlayer stack and around $4.3 \mu\text{m}$ thin, n-doped LPC-Si layers. The effect of different post-deposition treatments is studied (table 6.1): without treatment (untreated); 400°C , 30 min in hydrogen atmosphere (H30); 400°C , 15 min, hydrogen plasma (Hpla15); 400°C , 30 min, hydrogen plasma (Hpla30). Error bars represent multiple C-V curves measured on at least two different mesas on each sample.

As can be seen in figure 6.1, studied post-deposition treatments significantly influence the buried IL/LPC-Si interface. Without treatment, $D_{it,MG} \approx 22.5 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$. When a hydrogen plasma is used at 400°C for 30 min, the defect state density is reduced by one order of magnitude to $D_{it,MG} \approx 2.5 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$. When the process time is reduced to 15 min, only a slight increase of $D_{it,MG}$ is observed with respect to the 30 min-long process. Annealing the sample in hydrogen atmosphere without igniting the plasma results in $D_{it,MG} \approx 17 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$. It is concluded that the employment of a plasma is crucial for achieving a significant reduction of $D_{it,MG}$.

Similarly to $D_{it,MG}$, $Q_{IL,eff}$ is reduced by the post-deposition treatments which is unwanted in terms of the passivation quality. Without post-deposition treatment, $Q_{IL,eff} \approx 17 \times 10^{11} \text{ cm}^{-2}$ and with the treatments, $Q_{IL,eff} \approx 10 \times 10^{11} \text{ cm}^{-2}$ to $12 \times 10^{11} \text{ cm}^{-2}$ on average.

In order to obtain a comprehensive assessment of the influence of the post-deposition treatments on the IL/LPC-Si interface passivation quality, the interface to p-doped LPC-Si is also studied [50]. When the N/O/ON interlayer stack is adjacent to p-doped LPC-Si ($N_A \approx 7.7 \times 10^{16} \text{ cm}^{-3}$) it is observed that $D_{it,MG}$ results are very similar to the results with n-doped LPC-Si, while $Q_{IL,eff}$ is slightly higher when the LPC-Si is p-doped. The high amount of positive fixed charges adjacent to p-doped LPC-Si results in an inversion layer at the IL/LPC-Si interface [130]. In the following, the focus is on n-doped LPC-Si.

6.2.2 LPC-Si solar cell performance

The open-circuit voltages of LPC-Si test cells that experienced the post-deposition treatments listed in table 6.1 are measured with the sun simulator. Cells with molybdenum layer are measured in substrate configuration, while cells without molybdenum layer are measured in superstrate configuration. Figure 6.2 displays the results.

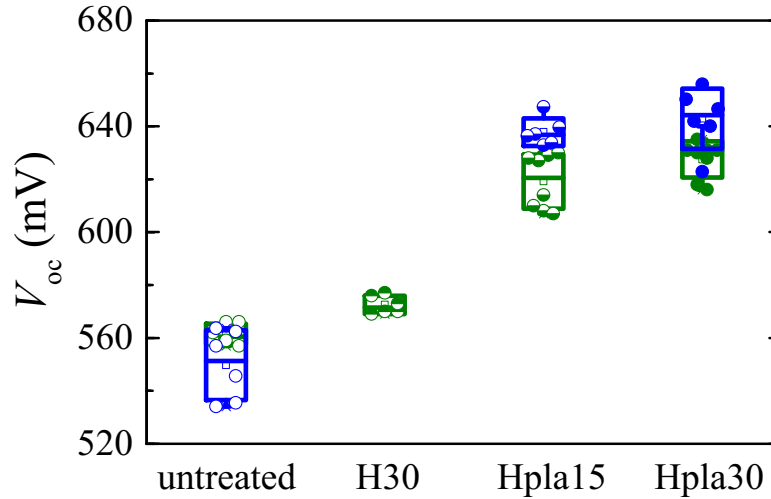


Figure 6.2: Open-circuit voltages of test cells based on the glass/Mo/IL/LPC-Si sequence with N/O/ON (20/100/80 nm) interlayer (green). Corresponding current-voltage curves are measured in substrate configuration. As reference, open-circuit voltages of test cells without molybdenum layer and with N/O/N/ON (10/200/60/20 nm) interlayer stack are displayed (blue). Corresponding current-voltage curves are measured in superstrate configuration.

The open-circuit voltage of cells with molybdenum layer is around 560 mV without any treatment (untreated). Elevated temperatures of 400 °C for 30 min lead to only slight improvements of V_{oc} to around 570 to 580 mV (H30). A significant improvement of V_{oc} to 620 to 640 mV is observed with the hydrogen plasma treatment at 400 °C for 15 and 30 min.

Usually, solar cells based on LPC-Si do not contain a molybdenum layer. The V_{oc} results of cells with a very similar device structure but without molybdenum layer (blue symbols in figure 6.2) are very similar to the open-circuit voltages of the cells with molybdenum layer. This indicates, that the molybdenum layer does not affect the LPC-Si material quality which indicates that the interlayer stack is an effective diffusion barrier for molybdenum.

6.2.3 Discussion

The post-deposition hydrogen plasma treatments at elevated temperatures improve the interface passivation quality, which is in line with literature results [46, 61]. The presented data demonstrate, that the improvement is dedicated to a reduction of the interface defect state density at mid gap energy. It is proposed, that the reduction of $D_{it, MG}$ is due to hydrogen atoms from the hydrogen-rich interlayer as well as due to hydrogen atoms from the plasma which diffuse through the roughly 4.3 μm thin absorber during the hydrogen plasma treatment.

The out-diffusion of hydrogen from dielectric layers such as SiN_x is frequently applied for chemical passivation of silicon surfaces [122, 131–133]. For example, Zhuo *et al.* investigated the interface properties of SiO_xN_y layers on Cz-Si wafers prepared by atmospheric-pressure plasma oxidation-nitridation [133]. After annealing in forming gas for 30 min at 400 °C, they found a decrease in $D_{it, MG}$ from $2.3 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$ to $6.1 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$. Lelièvre *et al.* observed a strong reduction of $D_{it, MG}$ (from $\approx 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$ to $\approx 10^{10} \text{ eV}^{-1}\text{cm}^{-2}$) at the SiN_x /silicon wafer interface after annealing at around 800 °C for 1 s and attributed this effect to the passivation of silicon dangling bond defects by hydrogen [122].

The diffusion of hydrogen from the plasma towards the buried IL/LPC-Si interface is quite complex, because hydrogen diffusion depends on e.g. the absorber doping concentration, defects in the absorber and the charge state of the hydrogen atoms [134–137]. Further investigations, e.g. with the secondary ion mass spectroscopy (SIMS) technique, could be employed to study hydrogen (or deuterium for better identification) diffusion in the material.

$Q_{IL, eff}$ is related to silicon dangling bonds located in the dielectric film close to the interface to the silicon. If the silicon atom is back-bonded to three nitrogen atoms (called K^+ -centre), the energy level is located around 0.1 eV or less below the conduction band edge in silicon [110]. The lower $Q_{IL, eff}$ values observed for n-doped silicon as compared to p-doped silicon could be explained by the neutralization of the K^+ -centres by electrons originating from the conduction band in silicon. The slight decrease of $Q_{IL, eff}$, which is observed when any of the post-deposition treatments is applied, could originate from hydrogen atoms that bond to the K^+ centres [79, 138, 139].

The increase of the open-circuit voltage when the hydrogen plasma treatments are applied can be explained in two ways. The increase could be related to the improved passivation quality at the buried interface. However, the positive fixed charge density is 10^{12} cm^{-2} or more, which results in a strong accumulation-type field-effect passivation. Assuming that the IL/LPC-Si interface is sufficiently passivated by the fixed charges, the improved cell performance is related to an increased LPC-Si bulk quality upon the post-deposition treatments. This is supported by literature. It was reported that hydrogen effectively passivates defects in n-doped silicon [137].

Furthermore, the improvement of the material quality of intrinsic poly-crystalline silicon upon a hydrogen plasma treatment thin films was related to the reduction of bulk defects located at grain boundaries and in grains [140].

In the following sections, all samples receive a post-deposition hydrogen plasma treatment.

6.3 O/N and O/N/O interlayer stacks

6.3.1 IL/LPC-Si interface passivation

From literature it is known that the passivation mechanism of SiO_x (chemical passivation) and SiN_x (field-effect passivation) films deposited on silicon wafers differs significantly. In this section, this aspect is investigated in detail for the IL/LPC-Si interface. In the first part, the charge stability at the two interfaces is examined. Next, the $D_{it, \text{MG}}$ and $Q_{\text{IL}, \text{eff}}$ provided by the O/N and O/N/O interlayer stacks are studied and the passivation mechanism is evaluated. Then, the influence of the SiO_x layer thickness on $D_{it, \text{MG}}$ and $Q_{\text{IL}, \text{eff}}$ is highlighted and discussed. For the O/N and O/N/O interlayer stack, the effective front-side surface recombination velocity is calculated based on the extended Shockley-Read-Hall formalism.

MIS structures are prepared as described in section 2.4. The as-deposited silicon thickness is 15 μm which is reduced to 14.3 μm by wet chemical treatments. All LPC-Si layers are n-doped and receive the same post-deposition hydrogen plasma treatment at 600 °C for 15 min. These conditions are different (higher heater temperature, shorter process time) from the conditions examined in section 6.2. As shown in section 2.2, as long as the heater temperature exceeds 300 °C, hydrogen plasma treatments at different conditions increase the open-circuit voltage in a similar manner. However, the hydrogen plasma treatment is not topic of this section.

Charge stability

The focus is on the charge stability at the interface between O/N and O/N/O interlayer stack and LPC-Si layer. High-frequency capacitance-voltage (C - V) curves are measured in sweep mode on several MIS structures on the two samples (figure 6.3 (a)). The voltage is swept from inversion to accumulation and vice versa. In order to obtain the full C - V curve covering the inversion and accumulation region it is necessary to vary the voltage between -90 V and 0 V and between -30 V and +10 V in case of the O/N and the O/N/O stack, respectively. For one mesa on each of the two samples, C - V curves in sweep mode are recorded five times consecutively and $Q_{\text{IL}, \text{eff}}$ is recorded under mid gap voltage conditions (figure 6.3 (b)).

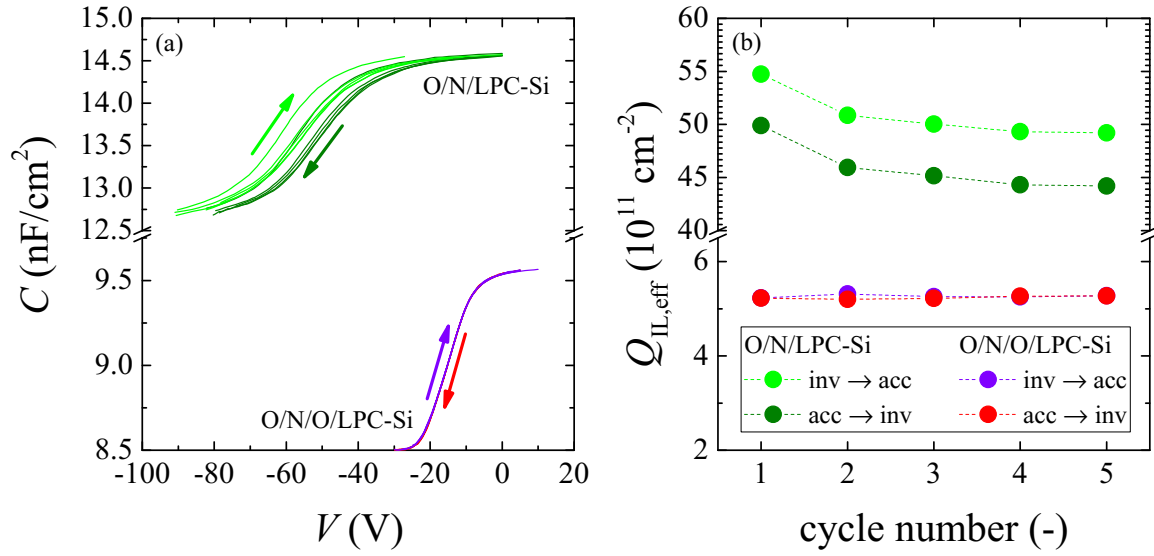


Figure 6.3: (a) Multiple C - V curves measured in sweep mode on several mesa on a sample based on the O/N interlayer stack and another sample based on the O/N/O interlayer stack. (b) $Q_{IL,eff}$ determined under mid gap voltage conditions from a sequence of C - V curves measured in sweep mode on the same mesa.

As can be seen in figure 6.3 (a), C - V curves with the O/N/LPC-Si structure are shifted towards higher negative voltages as compared to C - V curves based on the O/N/O/LPC-Si structure. This shift is an indication for a higher fixed charge density in the O/N interlayer stack as compared to the O/N/O interlayer stack. Furthermore, the slope of the C - V curves is less steep with O/N interlayer stack than with O/N/O interlayer stack implying that the O/N/LPC-Si interface has a higher defect state density than the O/N/O/LPC-Si interface. Corresponding $D_{it, MG}$ and $Q_{IL, eff}$ results obtained from C - V curves measured in relaxation mode are discussed below.

With the O/N interlayer stack a hysteresis is observed. The orientation of the hysteresis gives evidence of trap states in the interlayer which are charged through charge carrier injection from the LPC-Si into the interlayer upon applied gate voltage as explained in section 3.1.7. Accordingly, it can be seen in figure 6.3 (b), that $Q_{IL, eff}$ is slightly lower when it is determined from the C - V curve measured from accumulation to inversion than from inversion to accumulation.

The initially obtained $Q_{IL, eff}$ decreases slightly during the subsequent C - V sweep measurements on the same mesa when the O/N interlayer stack is used. This indicates a discharge of the average positive charge density in the O/N interlayer stack, which stabilizes after four measurements. However, the clockwise hysteresis remains, indicating a consistent charge carrier transfer between the O/N interlayer stack and the LPC-Si. In contrast, $Q_{IL, eff}$ at the

interface between O/N/O interlayer stack and LPC-Si remains stable for all five measurements and no hysteresis is observed.

In literature it was reported that SiN_x layers adjacent to silicon wafers may show a hysteresis effect when a voltage is applied across the $\text{SiN}_x/c\text{-Si}$ interface [100]. This effect was related to trapping of charges from the silicon by silicon dangling bonds in the Si_3N_4 network (K^+ -centres) [100].

Defect state density and fixed charge density with O/N and O/N/O interlayer

The interface passivation quality with O/N and O/N/O interlayer stack is evaluated in terms of $D_{\text{it,MG}}$ and $Q_{\text{IL,eff}}$. High-frequency C - V curves are recorded in relaxation mode and evaluated with respect to parasitic processes as described in section 3.1.7. For the determination of $D_{\text{it,MG}}$ and $Q_{\text{IL,eff}}$, C - V curves are selected for which relaxation capacitances are recorded in the inversion region and no charge instabilities are seen that might introduce artefacts in the calculated interface defect state density. Table 6.2 displays $D_{\text{it,MG}}$ and $Q_{\text{IL,eff}}$.

Table 6.2: $D_{\text{it,MG}}$ and $Q_{\text{IL,eff}}$ at the interface between O/N and O/N/O interlayer (IL) stacks and LPC-Si.

IL stack	$D_{\text{it,MG}} (\times 10^{11} \text{ eV}^{-1}\text{cm}^{-2})$	$Q_{\text{IL,eff}} (\times 10^{11} \text{ cm}^{-2})$
O/N	17.8 ± 4.6	45.0 ± 4.8
O/N/O	1.0 ± 0.4	4.3 ± 0.9

At both interfaces, fixed charges are positive which results in an accumulation-type passivation in case of n-doped silicon. Both, the effective interlayer charge density and the interface defect state density at mid gap energy, are around one order of magnitude higher with O/N interlayer stack than with O/N/O interlayer stack.

In SiN_x films, the fixed charge density is related to silicon dangling bonds back-bonded to three nitrogen atoms (K^+ -centres) located close to the $\text{SiN}_x/\text{LPC-Si}$ interface [100,141]. The developed SiN_x is nitrogen-rich and thus, contains a high number of nitrogen atoms that can contribute to K^+ -centres. This explains the high fixed charge density observed with the O/N interlayer stack. Similar results with $Q_{\text{IL,eff}} > 10^{12} \text{ cm}^{-2}$ were observed for the interface between SiN_x and a silicon wafer [105,142].

The high defect density in the bulk results in a high amount of defect states at the interface [100]. The reduction of interface states is often accomplished with hydrogen that is driven out from dielectric films at elevated temperatures. Hydrogen is more easily freed from a silicon atom

(binding energy 3.3 eV [122]) than from a nitrogen atom (binding energy 4.0 eV [122]). The developed SiN_x layer does not contain Si-H bonds in order to enable adhesion of the silicon film during the crystallization process (section 5.2). The high amount of fixed charges in combination with missing Si-H bonds in the developed nitrogen-rich SiN_x film explains the obtained $D_{\text{it,MG}}$ above $10^{12} \text{ eV}^{-1}\text{cm}^{-2}$. As expected, the density of interface defects is reduced when the SiO_x passivation layer is used ($D_{\text{it,MG}} \approx 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$).

In literature, a defect state density at mid gap of $7 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$ was reported at the interface between a silicon wafer and a SiO_x film deposited with the PECVD method after annealing the sample in forming gas [109]. The lower $D_{\text{it,MG}}$ observed with the SiO_x used in this work may be influenced by the SiN_x acting as hydrogen source to some extent [41, 105, 106, 109]. In addition, the MIS structures with 15 μm thin absorbers received a post-deposition hydrogen plasma treatment at 600 °C for 15 min. In section 6.2 it was demonstrated for 4.3 μm thin absorbers, that such a treatment at 400 °C for 30 min reduces $D_{\text{it,MG}}$ by around one order of magnitude. Therefore it is probable that this treatment is also responsible for the lower $D_{\text{it,MG}}$.

Defect state density and fixed charge density for different SiO_x thicknesses

As evident from table 6.2, the around 20 nm thin SiO_x layer between SiN_x and LPC-Si absorber has a strong effect on $D_{\text{it,MG}}$ and $Q_{\text{IL,eff}}$. The effect of the thickness of the SiO_x layer adjacent to the LPC-Si film on the passivation quality is examined in more detail.

MIS structures on the O/N/O interlayer stack with varying thickness of the SiO_x layer adjacent to the absorber are prepared. In order to better control the thickness of the SiO_x film, the deposition rate of the SiO_x is reduced by decreasing the SiH_4 flow rate from 8 sccm to 2 sccm (named "SiO20", table A.1). Three samples with different SiO_x layer thicknesses are prepared. PECVD deposition times of 41 s, 81 s and 163 s are used, respectively. The thickness of the SiO_x layer deposited with the shortest (41 s) PECVD process is $(12 \pm 2) \text{ nm}$ (figure 5.6). When a linear growth rate is assumed, the other two layers have a thickness of 24 nm and 48 nm, respectively.

Figure 6.4 displays $D_{\text{it,MG}}$ and $Q_{\text{IL,eff}}$ obtained for the interface between the O/N/O interlayer stack with varying SiO_x passivation layer thickness and LPC-Si.

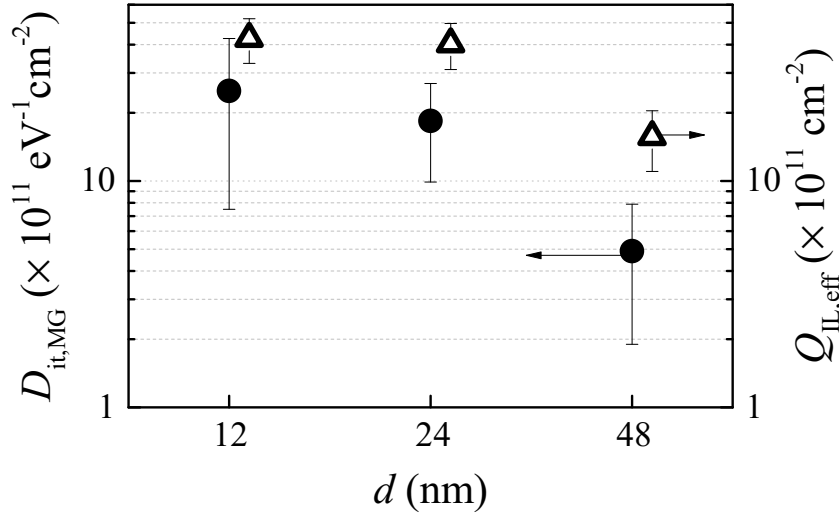


Figure 6.4: Interface passivation in terms of $D_{it, MG}$ and $Q_{IL, eff}$ with O/N/O interlayer stack, whereby the thickness (d) of the SiO_x adjacent to the LPC-Si absorber is varied. The layer with a thickness of (12 ± 2) nm is deposited in a 41 s PECVD process (figure 5.6). The layer thicknesses of the other two layers are calculated assuming a linear growth rate.

As can be seen, with increasing SiO_x thickness from 12 nm to roughly 24 nm, the fixed charge density is the same (on average around $42 \times 10^{11} \text{ cm}^{-2}$). With the thickest SiO_x film, $Q_{IL, eff}$ is reduced to $15 \times 10^{11} \text{ cm}^{-2}$. $D_{it, MG}$ is reduced from $25 \times 10^{11} \text{ cm}^{-2}$ to $5 \times 10^{11} \text{ cm}^{-2}$ with increasing SiO_x thickness.

Nitrogen plays a crucial role for the passivation quality, because it contributes to silicon dangling bonds in the dielectric film, for example in form of K^+ centres. Therefore, the STEM-EELS technique is employed to study the nitrogen and oxygen distribution in the interface region as described in section 3.1.6.

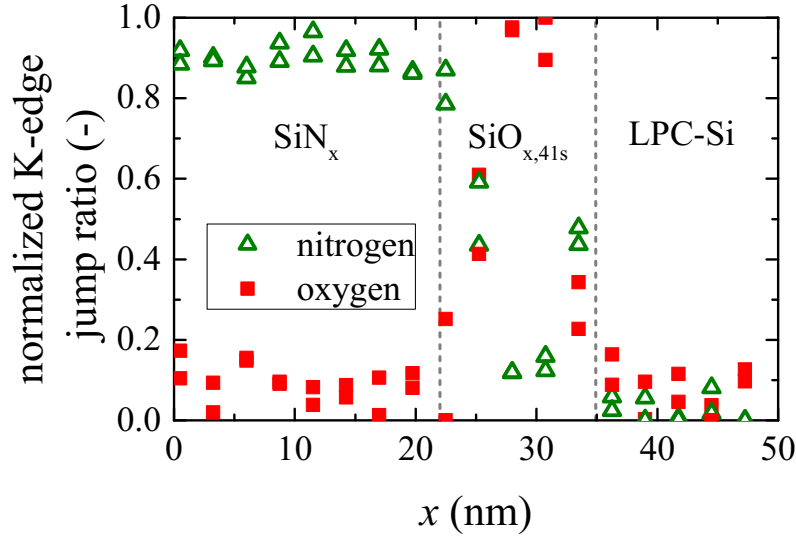


Figure 6.5: Distribution of oxygen and nitrogen in the interface region between O/N/O interlayer stack and LPC-Si. The SiO_x film adjacent to the LPC-Si layer is deposited in a 41 s PECVD process. This interface is investigated with the C-V technique (figure 6.4).

As can be seen in figure 6.5, the SiO_x layer adjacent to the LPC-Si absorber contains nitrogen. It is assumed, that nitrogen diffuses from the SiN_x film into the SiO_x film during the deposition process at 600 °C heater temperature and reach the SiO_x /LPC-Si interface when the 12 and 24 nm thin SiO_x layers are used. At the interface the atoms may back-bond to silicon dangling bonds. This would explain the high fixed charge densities assuming that most of the nitrogen atoms form K^+ centres. The drop of $Q_{\text{IL,eff}}$ observed for the roughly 48 nm thin layer indicates that less nitrogen atoms are present at the interface as compared to the thinner SiO_x films. In this case, it is assumed that more oxygen-correlated dangling bond defects ($\text{Si}\equiv\text{O}_3$, $\text{Si}\equiv\text{O}_2$, $\text{Si}\equiv\text{O}_2\text{N}$) form similar to the $c\text{-Si}/\text{SiO}_x$ interface.

Dingemans *et al.* demonstrated that the fixed charge density of more than 10^{12} cm^{-2} at the interface between a silicon wafer and SiN_x deposited with the PECVD method is reduced when a 50 nm thin SiO_x film is sandwiched between crystalline silicon ($c\text{-Si}$) and SiN_x [105]. This observation is in line with the ones presented above for the IL/LPC-Si interface. Mack *et al.* examined $c\text{-Si}/\text{thermal SiO}_2/\text{SiN}_x$ stacks with varying SiO_2 thickness. They observed an exponential decay of the fixed charge density from 5 to $1.3 \times 10^{12} \text{ cm}^{-2}$ with increasing thickness of the thermal oxide from around 4 to 14 nm [143]. The SiN_x film used in [143] has a comparable refractive index (1.90) to the SiN_x film developed in this work, however, the deposition temperature used by Mack *et al.* is lower (heater temperature of 400 °C instead of 600 °C used in this work). Furthermore, the thermal oxide might be more compact as

compared to the developed SiO_x film deposited with the PECVD method. Thus, it is assumed that nitrogen does not influence the passivation properties at the interface studied in [143].

It is concluded that the SiO_x thickness significantly influences the amount of fixed charges at the interface to the LPC-Si and thus, the thickness can be used to tune the band bending at the IL/LPC-Si interface. Overall, the $D_{it, \text{MG}}$ and $Q_{\text{IL, eff}}$ values determined for the IL/LPC-Si interface are in a similar range as published results for the interface between SiO_x and SiN_x and a silicon wafer, despite the different preparation processes and the different treatments that the passivation layers experience.

Surface recombination velocity with O/N and O/N/O interlayer

The interface defect state density and effective interlayer charge density obtained with MIS structures on the O/N and O/N/O interlayer stacks (table 6.2) are used to estimate the effective front-side surface recombination velocity ($S_{\text{eff, front}}$) using the extended Shockley-Read-Hall (SRH) formalism and the algorithm developed during this thesis based on section C and [94, 95].

Input parameters are - aside from the doping concentration (N), the excess charge carrier density (Δn) and the effective interlayer charge density ($Q_{\text{IL, eff}}$) as depicted in figure 4.4 - the energy-dependent interface defect state density ($D_{it}(E)$) and the energy-dependent capture cross sections of electrons and holes for a given defect ($\sigma_n(E)$ and $\sigma_p(E)$, respectively).

Schmidt *et al.* investigated the $\text{SiN}_x/c\text{-Si}$ interface using small pulse deep-level transient spectroscopy (DLTS) [144]. They suggest that the fundamental defects at the $\text{SiN}_x/c\text{-Si}$ interface are silicon dangling bonds as in the case of the thermal $\text{SiO}_2/c\text{-Si}$ interface when the 13.56 MHz PECVD method is used to deposit the SiN_x [110]. When the low-frequency (100 kHz) PECVD method is used a defect corresponding to surface damage dominates the interface defect structure [110]. Dangling bond defects at the thermal $\text{SiO}_2/c\text{-Si}$ interface are characterized by $\sigma_n = 10^{-14} \text{ cm}^2$ and $\sigma_p = 10^{-16} \text{ cm}^2$ at mid gap energy, respectively [95, 100].

In this work, the high-frequency PECVD method is employed to deposit the SiO_x and SiN_x films. Considering the results from [95, 100, 110, 144] it is assumed that the interface defect structure with these films is the same as with thermally grown SiO_2 . Thus, $\sigma_n = 10^{-14} \text{ cm}^2$ and $\sigma_p = 10^{-16} \text{ cm}^2$ are chosen for the simulations. It is further assumed that σ_n and σ_p are energy-independent. For the simulations, the excess charge carrier density (Δn) is fixed at 10^{14} cm^{-3} . This value is not critical because Δn does not impact $S_{\text{eff, front}}$ when it is smaller than 10^{16} cm^{-3} (details are depicted in figure C.1). The implemented doping density ($N_D = 1 \times 10^{17} \text{ cm}^{-3}$) is in accordance with the prepared MIS structures on the O/N and O/N/O interlayer stacks.

Figure 6.6 (a) displays $S_{\text{eff,front}}$ as a function of $Q_{\text{IL,eff}}$. The curves are based on defect state densities obtained from the integration of $D_{\text{it}}(E)$ curves between -0.2 and 0.2 eV as well as -0.4 and 0.4 eV. The green and red stars highlight $Q_{\text{IL,eff}}$ values obtained for the interface between LPC-Si and O/N and O/N/O interlayer stack, respectively (table 6.2).

As can be seen in figure 6.6 (b), the $D_{\text{it}}(E)$ curves follow an U-shape symmetrical around mid gap in the studied energy interval of -0.4 V to 0.4 V. This is similar to what is found for the interface between a silicon wafer and silicon oxide prepared by thermal annealing or plasma-oxidation [95, 145].

One can observe from figure 6.6 (a) that the effective front-side surface recombination velocity decreases with an increasing effective interlayer charge density which is dedicated to a stronger field-effect passivation. The $S_{\text{eff,front}}(Q_{\text{IL,eff}})$ curves can be described with $S_{\text{eff,front}} \sim 1/Q_{\text{IL,eff}}^2$ for sufficiently high amounts of fixed charges. $S_{\text{eff,front}} \sim 1/Q_{\text{IL,eff}}^2$ applies if $Q_{\text{IL,eff}}$ is the only charge present at the interface and if $Q_{\text{IL,eff}}$ is high enough to provide accumulation conditions at the interface to n-doped silicon [146]. With O/N/O interlayer stack (red curve) this region is reached for $Q_{\text{IL,eff}} \gtrsim 9 \times 10^{11} \text{ cm}^{-2}$. With O/N interlayer stack (green curve) a higher fixed charge density is needed to compensate the higher interface defect state density and thus, the onset for the inverse square-root dependence is at $Q_{\text{IL,eff}} \gtrsim 40 \times 10^{11} \text{ cm}^{-2}$. With both interlayer stacks, the obtained $Q_{\text{IL,eff}}$ values are sufficiently high to provide a strong field-effect passivation with accumulation conditions at the interface which relaxes the requirements for the interface defect state density [107, 147].

Taking into account defects located within ± 0.2 eV around the mid gap energy and assuming that these defects are well represented by $\sigma_p = 10^{-16} \text{ cm}^{-2}$ and $\sigma_n = 10^{-14} \text{ cm}^{-2}$, the calculated effective front-side surface recombination velocity (stars in figure 6.6) is slightly lower at the interface between LPC-Si and O/N interlayer stack ($\approx 3 \text{ cm/s}$) than at the interface between LPC-Si and O/N/O interlayer stack ($\approx 10 \text{ cm/s}$). These results demonstrate an excellent front-side passivation of the LPC-Si layer by the developed SiO_x and SiN_x films.

A larger integration interval of ± 0.4 eV considers a higher number of interface defect states and thus, $S_{\text{eff,front}}$ is increased (13 cm/s and 53 cm/s at the O/N/LPC-Si and O/N/O/LPC-Si interface, respectively). These results are based on the assumption that the capture cross sections are energy-independent. In reality, $\sigma_p(E)$ and $\sigma_n(E)$ of defects at SiO_2/Si and SiN_x/Si interfaces decrease strongly towards the band edges meaning that defects that are located farther away from the middle of the bandgap are less recombination active. Thus, 13 cm/s and 53 cm/s should be considered as an upper limit for the surface recombination velocity at the O/N/LPC-Si and the O/N/O/LPC-Si interface, respectively.

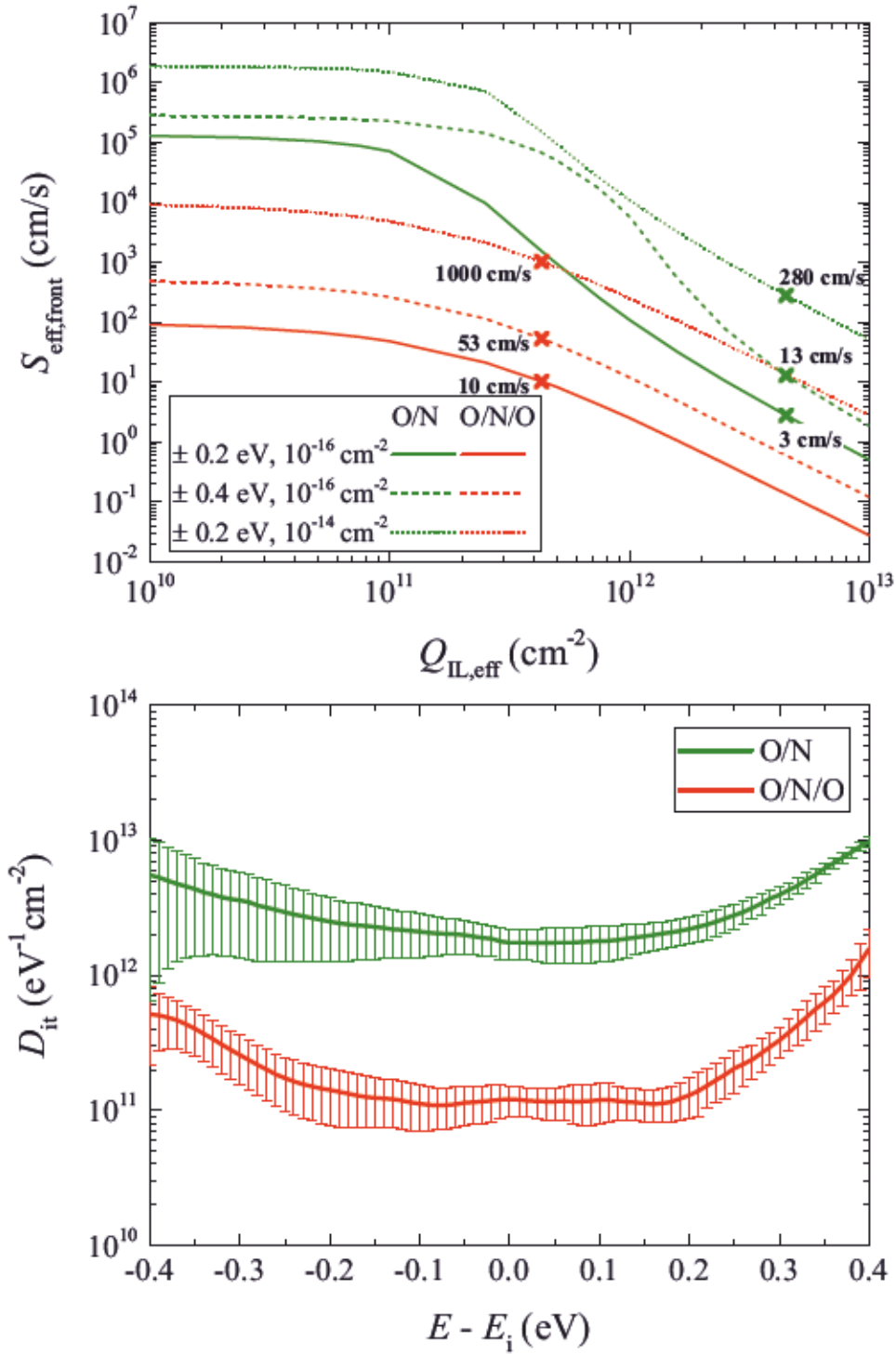


Figure 6.6: Passivation quality at the IL/LPC-Si interface with O/N and O/N/O interlayer stack: (a) Simulated effective front-side surface recombination velocity ($S_{\text{eff,front}}$) as a function of the effective interlayer charge density ($Q_{\text{IL,eff}}$). $\sigma_n = 10^{-14} \text{ cm}^2$ and $\sigma_p = 10^{-16} \text{ cm}^2$ (solid and dashed lines) and a higher σ_p of 10^{-14} cm^2 (dotted curves) is employed. $D_{\text{it}}(E)$ curves are integrated between $\pm 0.2 \text{ eV}$ (solid and dotted curves) and $\pm 0.4 \text{ eV}$ (dashed curves). Simulations are based on the extended SRH formalism and the algorithm developed during this thesis and [94,95]. $Q_g = 0 \text{ cm}^{-2}$ (no gate electrode). (b) Measured interface defect state density (D_{it}) as a function of the energy with respect to the intrinsic energy level (E_i). Error bars represent results on multiple MIS structures on one sample. $D_{\text{it}}(E)$ curves are determined from C - V curves measured in relaxation mode.

$S_{\text{eff,front}}$ is also sensitive to the capture cross section of minority charge carriers (σ_p) as illustrated exemplary for $\sigma_p = 10^{-14} \text{ cm}^{-2}$ in figure 6.6 (dotted curves). However, as discussed above it is assumed that $\sigma_p = 10^{-16} \text{ cm}^{-2}$ represents both interfaces well.

It can be seen that $S_{\text{eff,front}}$ is very sensitive to a reduction in $Q_{\text{IL,eff}}$, in particular with O/N interlayer stack due to the high interface defect state density. A reduction of $Q_{\text{IL,eff}}$ could be caused by injection of charge carriers from the silicon into the interlayer stack. As shown in figure 6.3, such a charge transfer is possible with the employed nitrogen-rich SiN_x film when a gate voltage is applied across the MIS structure. Charge carrier injection might also be observed when the sample is illuminated [95, 110].

Surface recombination velocity in context of literature

The results obtained for the effective surface recombination velocity at the IL/LPC-Si interface with developed O/N and O/N/O interlayer stacks are discussed in the context of published results (table 6.3).

The methods that are used to determine $S_{\text{eff,front}}$ at the front-side interface in LPC-Si samples are indicated in the footnotes.

Table 6.3: Effective surface recombination velocity at the interface between SiO_x and SiN_x layers and LPC-Si or silicon wafers. The last layer in the listed stacks is the layer adjacent to silicon. In case of the wafers, S_{eff} is extracted at $\Delta n \approx 1$ to $5 \times 10^{14} \text{ cm}^{-3}$. PVD refers to reactive RF-magnetron sputtering.

passivation layer	deposition method	doping type	S_{eff} (cm/s)	reference
passivation layer on silicon wafer				
SiO_2	thermal	p	30	[95]
SiO_2	thermal	n	0.46	[148]
SiO_x	PECVD	n	130	[109]
SiN_x	PECVD	p	4 - 6	[79]
SiN_x	PECVD	p	10	[110]
N/ON	PECVD	n	0.3 - 26	[100]
N/O	PECVD	n	< 6 - 27	[105]
N/O	PECVD	p	40 - 700	[41]
O/N/O	PECVD	p	20 - 200	[41]
N/O	PECVD / thermal	p	10 - 30	[143]
passivation layer	deposition method	doping type	$S_{\text{eff,front}}$ (cm/s)	reference
passivation layer sandwiched between glass substrate and LPC-Si				
SiC_x	PVD	p	$10^5 - 10^7$	[62] ⁽¹⁾
SiO_x	PVD	p	10^4	[61] ⁽¹⁾
N/O/ON	PECVD	p	1500 - 5500	[46] ⁽²⁾
N/O/ON	PECVD	n	1200 - 4000	[46] ⁽²⁾
O/N/O	PVD	n	< 500	[19] ⁽²⁾
O/N/O	PECVD	n	200	[53] ⁽³⁾
O/N/ON	PECVD with plasma-oxidation	n	100	[34] ⁽⁴⁾
O/N/O	PECVD	n	10	this work ⁽⁵⁾
O/N	PECVD	n	3	this work ⁽⁵⁾

¹ modelling QE curves with AFORS-HET

² modelling collection efficiency curves [149]

³ modelling QE curves with ASPIN3, interlayer stack developed in this thesis

⁴ modelling cell parameters with TCAD SentaurusTM, interlayer stack developed in this thesis

⁵ C-V measurements and SRH model [117] (section 6.3.1), interlayer stack developed in this thesis

When SiO_x and SiN_x films are adjacent to silicon fixed charges are positive which leads to accumulation conditions at the interface with n-doped silicon and to depletion or inversion conditions at the interface with p-doped silicon. In combination with the inequality of the capture cross section of electrons and of holes ($\sigma_n/\sigma_p = 100$) the effective front-side surface

recombination velocity is usually much lower for n-doped silicon interfaces than for p-doped silicon interfaces [95,110]. This is reflected by most of the results depicted in table 6.3.

As can be seen in table 6.3, the surface of silicon wafers can be passivated very well with SiN_x and thermally grown SiO_2 layers and effective surface recombination velocities below 10 cm/s were achieved. In general, these low values are found after annealing treatments, which bring hydrogen to defect sites to satisfy dangling bonds. 10 cm/s or below allows for high-efficiency solar cells that are limited by the bulk quality rather than by the surface [41,150]. It can be also seen that multi-layer stacks such as the N/O stack deposited with the PECVD method result in low surface recombination velocities which, in the case of the N/O stack, is explained by hydrogenation of the interface due to the SiN_x capping layer acting as source for hydrogen [104,143].

At the front-side of LPC-Si solar cells on glass, reported effective front-side surface recombination velocities are obtained from the analysis of finished solar cells as indicated in the footnotes in table 6.3. The $S_{\text{eff,front}}$ values estimated for single layers are higher than the ones determined for multi-layer stacks composed of silicon nitride, silicon oxide and silicon oxinitride. This is probably caused by an increased impurity concentration at the buried interface because single layers are likely an insufficient diffusion barrier. It is assumed that the lack of high amounts of fixed charges due to the absence of nitrogen reduces the passivation quality when single SiO_x and SiC_x films are employed as interlayer material. The effective front-side surface recombination velocity results obtained in this thesis are lower (11 cm/s) as compared to published results (200 cm/s) for the same O/N/O interlayer stack. This has several reasons. First, C-V measurements are performed on MIS structures with diameters of 900 μm or less. These small structures fit easily in one crystal grain, which is several centimetres in length and millimetres in width (figure 5.1). Thus, the results are not affected by structural defects such as grain boundaries. Solar cells cover a much larger area than the MIS structures and thus, the cell performance is influenced by these defects. This might explain the estimation of larger surface recombination velocities. In addition, cell parameters are obtained under illumination. It might be possible that charges are injected from the silicon into the interlayer stack upon illumination, which could neutralize K^+ centres. A reduction in $Q_{\text{IL,eff}}$ results in an increase of $S_{\text{eff,front}}$ (figure 6.6).

6.3.2 LPC-Si solar cell performance

In this section, the performance of LPC-Si solar cells based on the O/N and O/N/O interlayer stacks is studied. Test cells as well as IBC cells are evaluated. SunsVoc results are measured in substrate configuration while the current-voltage (J - V) curves as well as the external quantum efficiency (EQE) curves are obtained in superstrate configuration. Measured EQE curves are

modelled with ASPIN3 using the effective front-side surface recombination velocity ($S_{\text{eff,front}}$) and the SRH minority charge carrier bulk lifetime (τ_b) as input parameters. From the best fits, an effective minority charge carrier diffusion length is estimated.

Figure 6.7 displays the open-circuit voltage measured with the SunsVoc method in substrate configuration for test cells based on the O/N and O/N/O interlayer stacks.

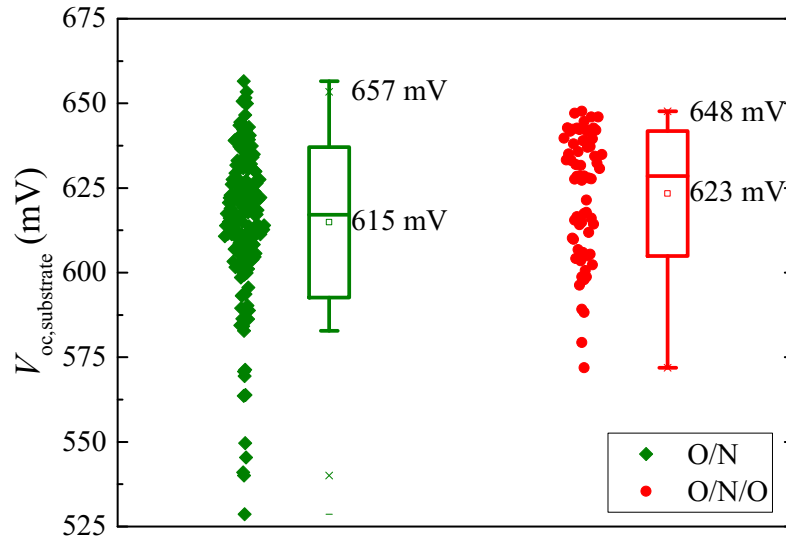


Figure 6.7: The open-circuit voltage (left) and corresponding box plots (right) of test cells with O/N and O/N/O interlayer stacks measured with the SunsVoc method in substrate configuration. At least 65 test cells on different samples for each interlayer stack are measured. All data with a pseudo fill factor below 0.7 are ignored.

The maximum V_{oc} of 657 mV is obtained with the O/N stack. The maximum V_{oc} with the O/N/O stack is 648 mV. However, the large scattering of the values motivates to compare the average values. The average open-circuit voltage with the O/N stack is 615 mV and with the O/N/O interlayer stack it is 7 mV higher. With O/N/O interlayer stack the median is also higher than for the O/N interlayer stack indicating that on the O/N/O interlayer stack a higher number of cells has a higher V_{oc} than on the O/N interlayer stack. The lowest V_{oc} results down to 526 mV are obtained on the O/N interlayer stack.

The lower V_{oc} values on the O/N interlayer stack might be caused by thermal instabilities of the SiN_x in direct contact with the silicon. Unpublished X-ray photoelectron spectroscopy (XPS) results of the air/LPC-Si interface obtained by Martina Trahms give evidence for nitrogen at the LPC-Si surface when the developed O/N interlayer stack is used. A further indication of such instabilities is that it takes much longer (around 30 min) to remove the around 100 nm thin capping layer by means of hydrofluoric acid from the silicon surface (indicated by surface

hydrophobicity) when the O/N interlayer stack is used instead of the O/N/O interlayer stack (around 5 min). If nitrogen diffuses to the LPC-Si surface during the crystallization process, it forms a SiO_xN_y layer in conjunction with oxygen from the capping layer which is more difficult to remove by hydrofluoric acid. Furthermore, for a variety of O/N samples the surface appearance is a lighter shade of grey after etching in contrast to samples based on the O/N/O interlayer stacks attributed to increased roughness. Finally, test cells fabricated on the O/N interlayer stack were frequently shunted. However, the investigation of the interface region between the developed O/N interlayer stack and the LPC-Si layer with transmission electron microscopy (figure 5.6), does not show thermal instabilities of the SiN_x film. Instead, the layers appear compact and well-defined. However, only around 500 nm of the interface is displayed.

In literature thermal instabilities of SiN_x films in direct contact to LPC-Si were detected. X-ray photoelectron spectroscopy (XPS) investigations from the LPC-Si/air side revealed a nitrogen peak at the surface of the LPC-Si material when a single physical vapor deposition (PVD) SiN_x layer is used as interlayer stack [151]. With such an interlayer a nitrogen concentration of 10^{20} cm^{-3} was measured in the LPC-Si bulk employing SIMS measurements [152]. A TEM investigation of a sputtered O/N layer showed void formation through the O/N stack giving rise to impurity diffusion from the glass substrate [52]. Impurities, that diffuse from the glass through voids in the interlayer stack into the LPC-Si absorber, as well as precipitations of nitrogen or oxygen are defects in the silicon bulk and thus, are additional recombination centres for charge carriers. This could explain the reduced open-circuit voltages observed for some cells with O/N interlayer stack. Overall, the O/N stack is somewhat less robust than the O/N/O interlayer which can result in good cells but also in bad cells.

Next, the quantum efficiency curves as well as the optical losses of test cells on the O/N and O/N/O interlayer stacks are compared. Figure 6.8 shows corresponding (a) EQE curves, $1 - R(\lambda) - T(\lambda)$ spectra and (b) IQE curves. The curves represent the average of 18 (19) test cells on three (four) $5 \text{ cm} \times 5 \text{ cm}$ samples based on the developed O/N/O (O/N) interlayer stack.

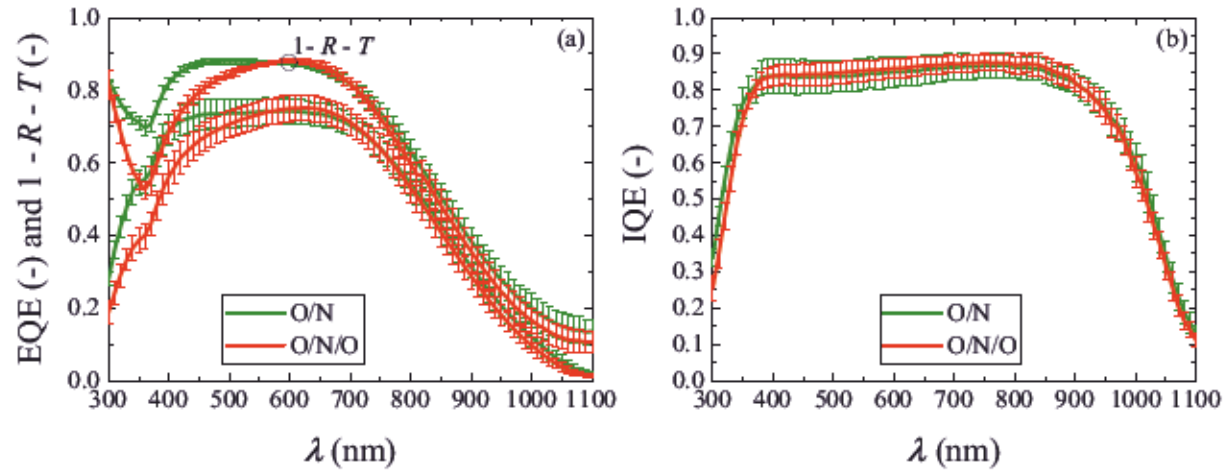


Figure 6.8: Comparison of LPC-Si test cells with O/N and O/N/O interlayer stack in terms of (a) EQE curves and $1 - R(\lambda) - T(\lambda)$ spectra and (b) IQE curves. Cells are illuminated in superstrate configuration. Error bars represent the average of 18 (19) test cells on three (four) $5 \text{ cm} \times 5 \text{ cm}$ samples based on the developed O/N/O (O/N) interlayer stack.

As expected from discussions in section 5.3, in the short-wavelength regime optical losses are higher with the O/N/O stack as compared to the O/N stack. The gap is largest at 360 nm where 30 % is lost with the O/N interlayer stack and almost 50 % is lost with the O/N/O interlayer stack. The difference translates in differences of EQE curves, i.e. at 360 nm, $\text{EQE} = 55 \%$ and $\text{EQE} = 43 \%$ with O/N and O/N/O interlayer stack, respectively. IQE curves reflect the quantum efficiency when reflection and transmission losses are ignored and thus, from these curves the electrical quality of the LPC-Si bulk and at the interfaces can be compared. As can be seen from the data presented in figure 6.8 (b) both IQE curves are almost the same. The spread of curves obtained on the O/N interlayer stack is slightly larger as compared to the curves obtained on the O/N/O interlayer stack, which is in line with the V_{∞} results.

Modelling measured EQE curves based on surface recombination velocity and bulk lifetime

Measured EQE curves of one test cell batch on O/N and O/N/O interlayer stack are modelled with ASPIN3. In general, modelling of EQE curves cannot distinguish between the interface passivation quality and the bulk quality. In this section the $S_{\text{eff,front}}$ results that are determined from measured C-V curves are used for the simulations while the SRH bulk lifetime serves as variable input parameter. Based on $S_{\text{eff,front}}$ and τ_b combinations that represent the measured EQE curves the effective minority charge carrier diffusion length ($L_{\text{diff,eff}}$) is calculated and discussed in the context of literature results.

$L_{\text{diff,eff}}$ is calculated by assuming that the interface at the rear side of the silicon absorber is ideal ($S_{\text{eff,rear}} = 0$ cm/s). With this, $S_{\text{eff,front}}$ is converted into an effective front-side interface lifetime ($\tau_{\text{eff,front}}$) using $\tau_{\text{eff,front}} = d_{\text{LPC-Si}}/S_{\text{eff,front}} + 4/D(d_{\text{LPC-Si}}/\pi)^2$, whereby $d_{\text{LPC-Si}}$ is the absorber thickness and D is the diffusivity. The latter is obtained using $D = V_{\text{th}} \mu_{\text{minority}}$. V_{th} is the thermal voltage and μ_{minority} is the mobility of minority charge carriers which is reduced to 80 % of the mobility in crystalline silicon [46, 53, 75]. Finally, $L_{\text{diff,eff}} = (D \times (\tau_{\text{front}}^{-1} + \tau_{\text{b}}^{-1})^{-1})^{0.5}$. Calculated $L_{\text{diff,eff}}$ for each of the $S_{\text{eff,front}}/\tau_{\text{b}}$ combinations are shown in table 6.4.

The implemented structure is in accordance to the fabricated test cells. The absorber thickness is 11.5 to 12 μm and the absorber doping is $N_{\text{D}} = 1 \times 10^{17} \text{ cm}^{-3}$. Further details are described in section 3.3. Figure 6.9 displays the measured and simulated EQE curves for structures based on the O/N and the O/N/O interlayer stack. Table 6.4 lists the combinations of input parameters that are used to fit the measured EQE curves.

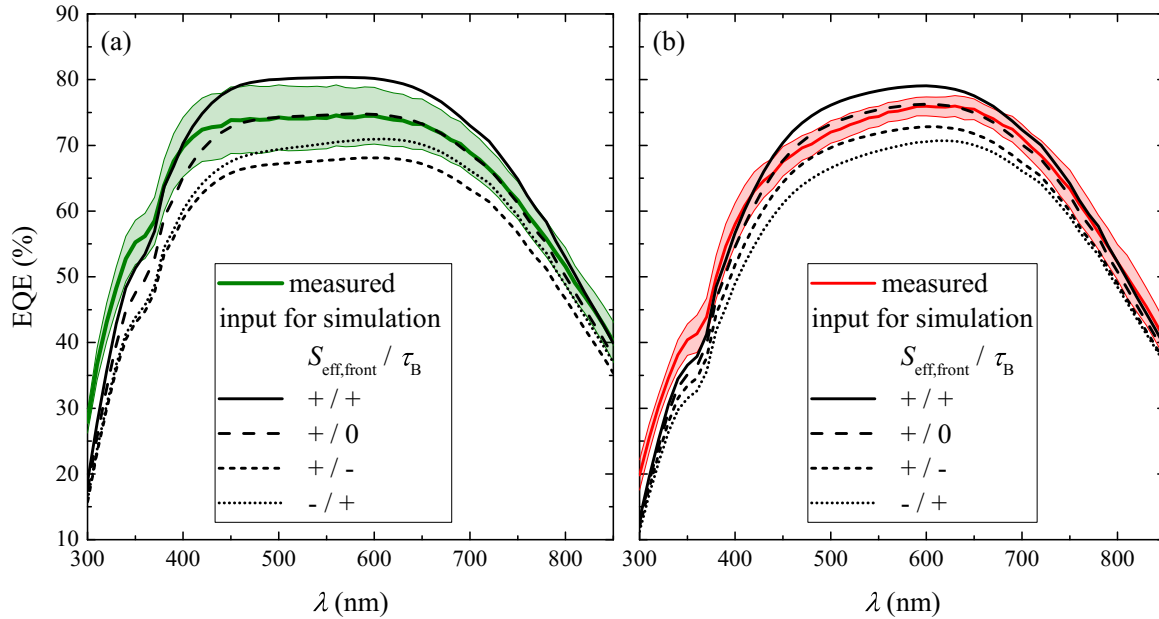


Figure 6.9: Measured and simulated EQE spectra of LPC-Si test cells based on (a) the O/N and (b) the O/N/O interlayer stack, respectively. For the simulations, ASPIN3 is employed. Errors represent four different solar cells. Table 6.4 lists the $S_{\text{eff,front}}/\tau_{\text{b}}$ combinations that are used to fit the measured EQE curves.

Table 6.4: Combinations of $S_{\text{eff,front}}$ and τ_b used as input parameters for the modelling of the measured EQE curves using ASPIN3. The samples are based on the O/N and O/N/O interlayer stack developed in the framework of this thesis. Nomenclatures of input combinations are given.

IL stack	$S_{\text{eff,front}}$ (cm/s)	τ_b (μs)	nomenclature	$L_{\text{diff,eff}}$ (μm)
O/N	4	0.4	+ / -	16.6
O/N	4	0.7	+ / 0	21.9
O/N	4	1.5	+ / +	32.1
O/N	1000	1.5	- / +	23.1
O/N/O	11	0.5	+ / -	18.5
O/N/O	11	0.7	+ / 0	21.9
O/N/O	11	1.0	+ / +	26.1
O/N/O	1000	1.0	- / +	20.6

As can be seen in figures 6.9 (a) and (b) and in table 6.4, the EQE curves on O/N and O/N/O interlayer stack can be described with the effective front-side surface recombination velocity data obtained from C-V measurements (4 and 11 cm/s, respectively), when the bulk lifetime is around 0.4 to 1.5 μs and 0.5 to 1.0 μs , respectively, whereby the averaged curves are best described with 0.7 μs for both interlayer stacks. Corresponding effective minority charge carrier diffusion length range between 16.6 to 32.1 μm and 18.5 to 26.1 μm for the O/N and O/N/O interlayer stack, respectively.

Taking the bulk lifetime that describes the upper limit of measured EQE curves and assuming a low front-side passivation quality of $S_{\text{eff,front}} = 10^3$ cm/s it can be seen that the slope of the EQE curve is not represented well in case of the O/N interlayer stack. This indicates that $S_{\text{eff,front}}$ is smaller than 1000 cm/s. In case of the O/N/O interlayer stack simulated results with the combination "- / +" are too low to describe the measured curves.

In literature, effective minority charge carrier diffusion lengths of 11 μm and 14 μm were obtained from the analysis of IQE curves as well as from transient photo-luminescence (PL) records on LPC-Si solar cells [46, 153]. The effective minority charge carrier diffusion length ($L_{\text{diff,eff}}$) was also determined from investigations with the light-beam induced current technique on certain spots on LPC-Si samples based on the developed O/N/O interlayer stack [53, 154, 155]. It was found that τ_b and $L_{\text{diff,eff}}$ are reduced with increasing absorber doping [155]. For $N_D = 1.7 \times 10^{17} \text{ cm}^{-3}$, which is similar to the doping of cells studied in this section, a SRH bulk lifetime of $(17 \pm 1) \mu\text{s}$ and an effective minority charge carrier diffusion length of $(0.5 \pm 0.1) \mu\text{s}$ was obtained. This is in line with the presented results in table 6.4.

It is concluded that the $S_{\text{eff,front}}$ results that are determined from C-V measurements as described in section 6.3.1 can be used to describe measured EQE curves and that resulting effective minority charge carrier diffusion length are comparable to results obtained by other methods.

6.3.3 Discussion

As shown above, test cells on O/N and O/N/O interlayer stack yield similar results. However, cell results on the O/N interlayer stack scatter more than on the O/N/O interlayer stack which is probably related to thermal instabilities of the SiN_x layer in direct contact to the silicon.

In order to justify a correlation between the performance of cells on O/N and O/N/O interlayer stack and the front-side passivation quality determined in section 6.3.1 the interlayer stacks should not influence the LPC-Si bulk quality. For example, the interlayer stack should not influence the grain size because the grain size affects the open-circuit voltage if the grain size is smaller than the absorber thickness [18,19]. Figures 5.1 (b) and (c) show glass/IL/LPC-Si samples after crystallization and texturing on the O/N and the O/N/O interlayer stack, respectively. Large laterally grown grains of several centimetres in scanning direction and a few millimetres in width (which is larger than the absorber thickness) are seen which are typically observed after liquid-phase crystallization of the thin silicon films on the glass substrates. No difference in the grain size is observed and thus, the similar performance of test cells on O/N and O/N/O interlayer stack is related to the similar passivation quality at the front-side of the test cells.

With O/N interlayer stack high amounts of fixed charges are measured in the interface region between the interlayer stack and LPC-Si. This increases the passivation quality due to the strong electric field that separates minority from majority charge carriers. However, due to the high interface defect state density, the effective front-side surface recombination velocity is sensitive to a reduction of the effective interlayer charge density. For example, a reduction of $Q_{\text{IL,eff}}$ by one order of magnitude results in an increase of $S_{\text{eff,front}}$ from 4 cm/s to approximately 10^5 cm/s (figure 6.6). Such a strong dependence of $S_{\text{eff,front}}$ on $Q_{\text{IL,eff}}$ is not desirable.

The O/N/O interlayer stack results in a low defect state density at the front-side interface making the passivation not as sensitive to variations in the fixed charge density as observed for the O/N interlayer stack. The around 20 nm thin SiO_x adjacent to the LPC-Si absorber is deposited in a short (17 s) PECVD process, which involves the risk for unstable process conditions. Furthermore, such very short process times increase the risk for inhomogeneities in the thickness of the thin SiO_x film which affects the passivation quality in terms of $Q_{\text{IL,eff}}$ and $D_{\text{it,MG}}$ as shown in figure 6.4.

These considerations motivate the realization of an oxygen capping layer for the O/N interlayer stack which prevents nitrogen diffusion through the absorber during the crystallization process, which provides a high fixed charge density, which is homogeneous and for which the thickness is well-controllable.

6.4 O/N/ON interlayer stack formed by plasma-oxidation

It is known that SiO_xN_y films can be realized by plasma-oxidation of SiN_x films prepared with PECVD whereby the SiN_x film is gradually converted into the SiO_xN_y [156, 157]. Similarly, SiO_x films can be formed upon plasma-oxidation of silicon [145]. During the oxidation process silicon is consumed by contrast to layer deposition, thereby replicating the thermal oxidation process. The advantage of an oxidation process with a plasma is that process temperatures are lower ($< 600^\circ\text{C}$) than temperatures used for thermal oxidation (1100°C).

Plasma-oxidized SiN_x layers were demonstrated in literature with similar passivation properties as compared to thermally grown oxides, this is a defect state density below $10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ and a fixed charge density of around 10^{11} cm^{-2} [156]. Kennedy *et al.* highlighted, that defects located close to the middle of the silicon band gap are reduced upon plasma-oxidation of SiN_x films [157]. Another benefit which is exploited by using plasma-oxidation is the homogeneity of the resulting film [157]. An oxide growth rate of 0.038 nm/s was found when an oxygen plasma is used to plasma-anodize a Si_3N_4 film [157]. The mechanism of oxide growth is described as a replacement of nitrogen by oxygen atoms caused by bonding instability of nitrogen at the surface of the SiN_x layer [157]. Nitrogen exits into the plasma in form of molecular nitrogen [157]. When a SiO_x is formed upon plasma-oxidation of silicon the growth kinetics are linear only for around 10 to 20 min [145]. At longer oxidation times the growth kinetics follow a parabolic shape [145].

Overall, plasma-oxidation is a promising alternative to the PECVD technique to fabricate the desired capping layer for the O/N interlayer stack which is motivated in the previous section. LPC-Si samples are prepared to test plasma-oxidation of the O/N interlayer stack. A glass substrate coated with the O/N stack is prepared. Then, an N_2O plasma is ignited with a N_2O flow rate of 100 sccm , a RF-power of 160 W , 0.5 mbar pressure, a heater temperature of 600°C corresponding to a samples temperature of about 450°C (figure A.1) and a distance between the two electrodes of 18 mm . The duration of the oxidation treatment is set to 10 min .

The oxidation of the SiN_x layer upon the plasma treatment is verified with the STEM-EELS method. Figure 6.10 (a) depicts the normalized K-edge jump ratios of oxygen and nitrogen obtained from 120 nm -long line scans taken normal to the interface as described in section 3.1.6.

In figures 6.10 (b) and (c), the interface morphology is depicted which is obtained with the transmission electron microscopy (TEM) method.

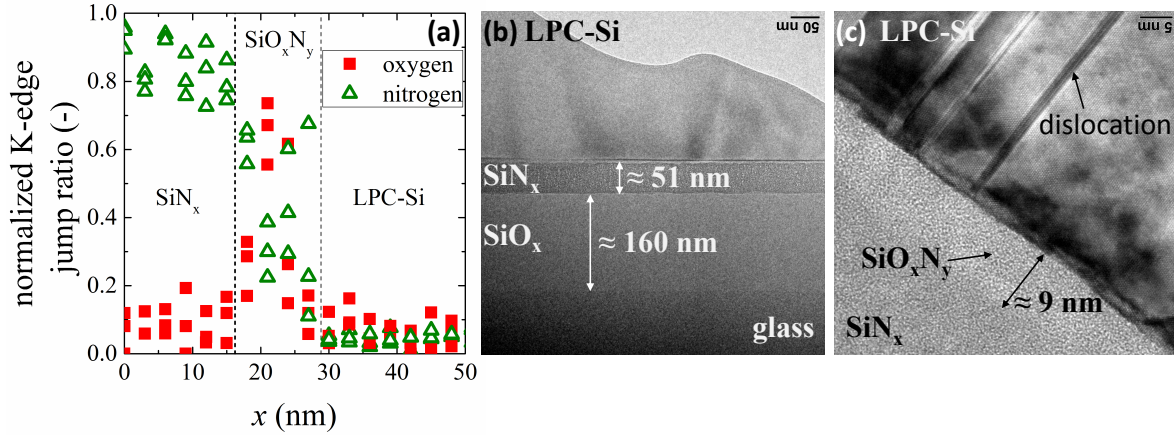


Figure 6.10: Detailed investigation of the effect of plasma-oxidation of the SiN_x film on (a) the distribution of oxygen and nitrogen and (b), (c) on the morphology at the interface between the interlayer stack and LPC-Si. (b) and (c) display the interface region on a different scale.

As can be seen, the interface is smooth, layers are well-defined and compact. The smooth interface is attributed to the developed nitrogen-rich SiN_x layer in which hydrogen is bonded to nitrogen only (no Si-H bonds present) making the layer more stable upon annealing as discussed in section 5.2. In figure 6.10 (c), dislocations are visible, which are frequently observed in LPC-Si material.

The 10 min-long N₂O plasma treatment transformed around 9 nm of the top surface of the SiN_x layer into a SiO_xN_y layer which is indicated by the light grey surface region in figure 6.10 (c) as well as in figure 6.10 (a). Thus, the effective oxidation growth rate is 0.013 nm/s. The quantification of oxygen and nitrogen is not possible upon the presented data because scattering cross sections that describe the possibility of the interaction between the electrons from the beam and from the nitrogen and oxygen atoms are not known.

The developed O/N/ON interlayer stack is tested in test cells. The absorber thickness is approximately 14.7 μm. The planar absorber is n-doped with $N_D \approx (11 \pm 3) \times 10^{16} \text{ cm}^{-3}$. Figure 6.11 (a) displays open-circuit voltage (V_{oc}) results measured in substrate configuration with the SunsVoc method. The y-axis is the same as in figure 6.7 for better comparability. In figure 6.11 (b), $1 - R(\lambda) - T(\lambda)$, EQE curves and IQE curves obtained in superstrate configuration are shown.

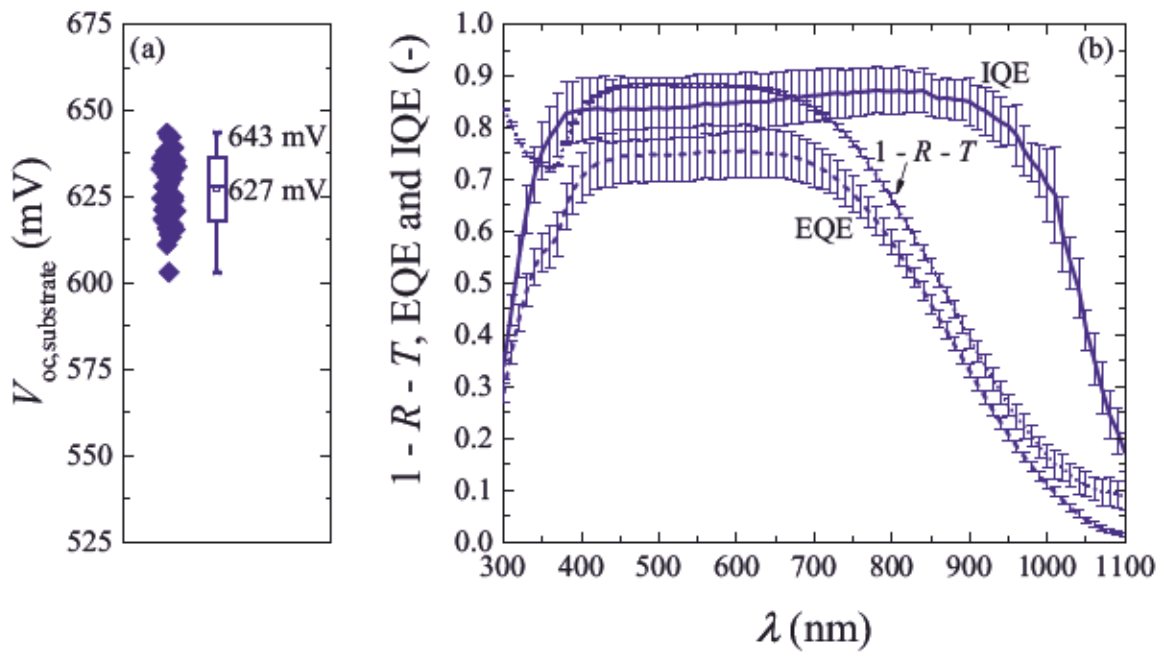


Figure 6.11: Test cells on the developed O/N/ON interlayer stack: (a) V_{oc} (left) and corresponding box plots (right) of test cells measured in substrate configuration with the SunsVoc method. All data with a pseudo fill factor below 0.7 are ignored. (b) $1 - R(\lambda) - T(\lambda)$, EQE curves and IQE curves obtained in superstrate configuration. Error bars in (b) represent curves of seven test cells on one $5\text{ cm} \times 5\text{ cm}$ sample.

As can be seen, the maximum V_{oc} is 643 mV and the average V_{oc} is 627 mV. The results are similar to results obtained on the O/N and the O/N/O interlayer stack. However, the spread of the data is lower with the O/N/ON interlayer than for the other two interlayer stacks. The EQE results scatter slightly more than with O/N and O/N/O interlayer. For example, at 600 nm the EQE is $(75.4 \pm 5.0)\%$ with the O/N/ON interlayer stack while it is $(74.2 \pm 3.5)\%$ and $(75.0 \pm 3.5)\%$ with the O/N and O/N/O interlayer stack, respectively.

It is experienced that LPC-Si samples based on the O/N/ON interlayer stack behave similar to samples on the O/N/O interlayer stack in terms of removal of the capping layer (fast) and appearance of the surface (not grey). Accordingly, unpublished X-ray photoelectron spectroscopy (XPS) results of the air/LPC-Si interface with the developed O/N/ON interlayer stack obtained by Martina Trahms do not give evidence for nitrogen at the LPC-Si surface. This indicates that the SiO_xN_y film formed upon plasma-oxidation of the SiN_x layer is thermally stable, also when in direct contact to the silicon.

It is likely that the incorporation of oxygen reduced $Q_{IL,eff}$ to some extent. However, it is speculated that the amount of fixed charges originating from the nitrogen-rich SiN_x layer is

still sufficiently high to provide a strong field-effect passivation. It might be that D_{it} is reduced due to the presence of oxygen at the interface which is also reported in [157].

6.5 IBC cell results on developed interlayer stacks

In this section, the developed interlayer stacks, namely O/N, O/N/O and O/N/ON, are implemented in IBC LPC-Si solar cells and compared with respect to the open-circuit voltage, short-circuit current density, fill factor and energy conversion efficiency. Figure 6.12 shows the current-voltage (J - V) curves of the best cells. Table 6.5 lists corresponding V_{oc} , J_{sc} , FF and η data.

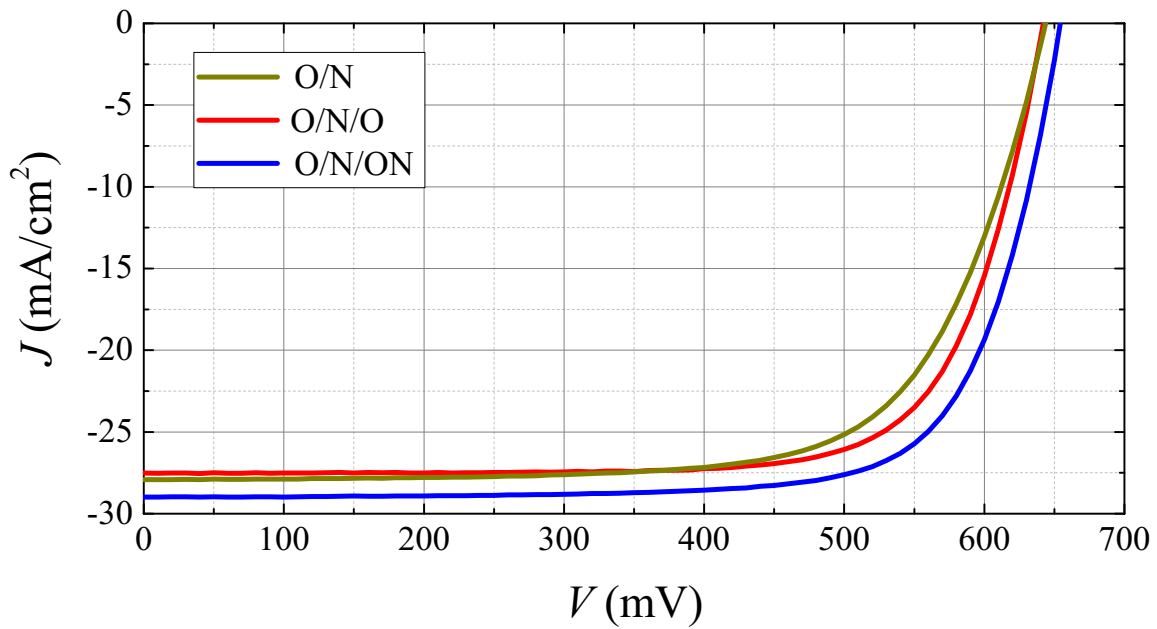


Figure 6.12: Current-voltage (J - V) curves of the best IBC LPC-Si solar cells based on the O/N, O/N/O [53] and O/N/ON [34] interlayer stacks developed in the framework of this thesis. All curves are measured with an anti-reflection foil (ARF).

Table 6.5: Parameters of LPC-Si solar cells based on different interlayer (IL) stacks. The cells are contacted with sophisticated methods, this is, interdigitated back-contact (IBC), FrontEra and point contacts (PC). PVD refers to reactive RF-magnetron sputtering.

IL stack	IL deposition method	cell type	doping type/density $\times 10^{16} \text{ cm}^{-3}$	V_{oc} mV	J_{sc} mA/cm^2	FF %	η %	reference
O/N	PECVD	IBC	n / 9	644	27.9	70	12.6	this thesis
O/N/O	PECVD	IBC	n / 12	642	27.5	75	13.2	[53], this thesis
O/N/ON	PECVD	IBC	n / 8	654	29.0	75	14.2	[34], this thesis
O/N/O	PVD	FrontERA	n / 4	632	27.8	67	11.8	[47]
O/N/O	PVD	FrontERA	n / 3.9	629	27.5	66	11.5	[19]
N/O/ON	PECVD	FrontERA	n / 9	649	27.3	68	12.1	[48]
N/O/N/ON	PECVD	PC	p / 0.8	619	28.3	66	11.5	[36]
O/N/O	PVD	PC	p / 4	585	27.6	72	11.7	[51]

The IBC cells deposited on the developed interlayer stack exhibit an open-circuit voltage above 642 mV which reveals the high quality of the LPC-Si material. The highest open-circuit voltage of 654 mV is found on the cell with the O/N/ON interlayer stack realized upon plasma-oxidation [34]. Another cell from this batch even showed 661 mV [34]. The high open-circuit voltage of cells on the O/N/ON interlayer stack are remarkable because the doping concentration is lower in comparison to the cell based on the O/N/O stack which exhibits 642 mV [53].

The short-circuit current density of the IBC cells on the developed O/N/ON interlayer stack is about $1.5 \text{ mA}/\text{cm}^2$ higher ($29 \text{ mA}/\text{cm}^2$) as compared to the cells on the O/N and O/N/O interlayer stacks. Currently, the cause for the observed high short-circuit current density is being investigated, for example by means of the light-beam induced current (LBIC) method. This technique allows the determine of the locally dissolved recombination activity at structural defects such as grain boundaries located in the LPC-Si bulk.

The fill factor (FF) is lowest (70 %) when the developed O/N interlayer stack is used. This might be related to the thermally unstable SiN_x layer when in direct contact to the silicon. In [34] it is demonstrated that the fill factor is influenced by the back surface field width (figure 2.5). However, all three IBC cells displayed in figure 6.12 have the same back surface field width of $120 \mu\text{m}$.

The IBC silicon hetero-junction cell based on the O/N/ON interlayer stack exhibits an efficiency of 14.2 % which is a record for LPC-Si solar cells on glass [34]. The high open-circuit voltage of 661 mV shows the potential of LPC-Si thin film solar cells.

6.6 Limitations of LPC-Si solar cell performance

At the end of this chapter it is estimated to what extent the performance of LPC-Si solar cells on the developed interlayer stacks is limited by the front-side interface.

In order to do so the open-circuit voltage and the short-circuit current density are simulated as a function of $S_{\text{eff,front}}$ for two different SRH bulk lifetimes. One bulk lifetime represents a well passivated bulk ($1.5 \mu\text{s}$) and the other a poorly passivated bulk ($0.5 \mu\text{s}$). For the simulations ASPIN3 is employed. The implemented structure is in accordance to a typical test cell with a planar $15 \mu\text{m}$ -thin absorber with $N_D = 1 \times 10^{17} \text{ cm}^{-3}$. Figure 6.13 displays the results.

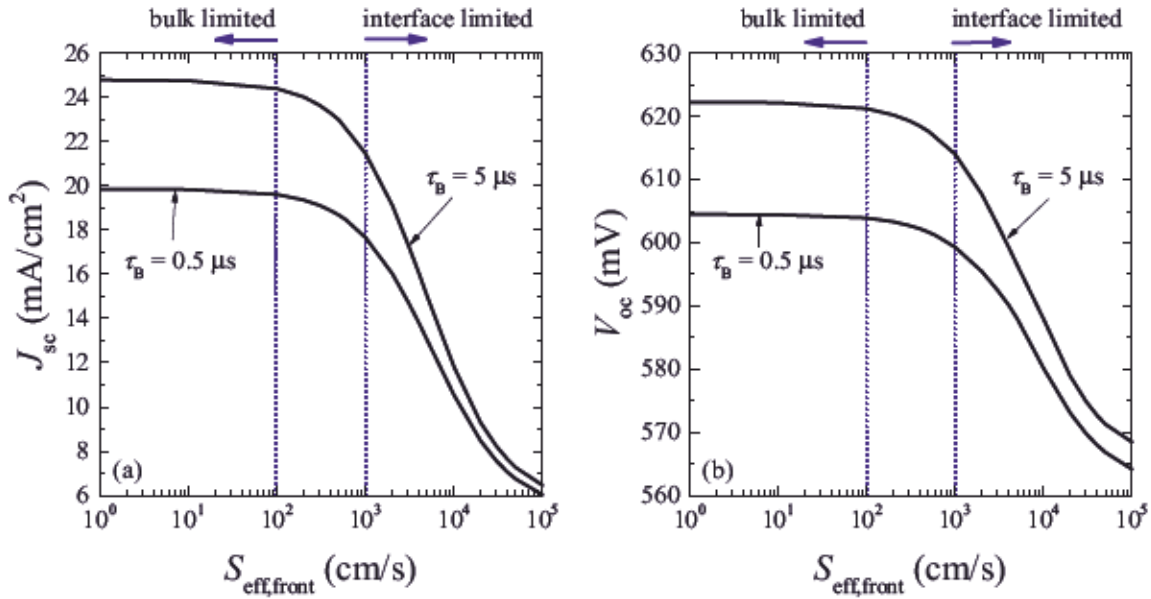


Figure 6.13: Simulated (a) short-circuit current density (J_{sc}) and (b) open-circuit voltage (V_{oc}) as a function of $S_{\text{eff,front}}$ and τ_b using ASPIN3 [88]. The defect density in the 2 nm thin defect layer at the rear side of the simulated structure is set to $N_{\text{tr}} = 1.3 \times 10^{15} \text{ cm}^{-3}$. Horizontal dotted lines split the graph into three regions: bulk limited for $S_{\text{eff,front}} \lesssim 100 \text{ cm/s}$ or below, interface limited for $S_{\text{eff,front}} \gtrsim 1000 \text{ cm/s}$ and an intermediate range where both, the bulk and the interface quality influence V_{oc} and J_{sc} .

As can be seen in figure 6.13 for $S_{\text{eff,front}} \lesssim 100 \text{ cm/s}$ $S_{\text{eff,front}}$ does not affect V_{oc} and J_{sc} and simulated J_{sc} and V_{oc} are limited by the bulk quality. For $S_{\text{eff,front}} \gtrsim 1000 \text{ cm/s}$, V_{oc} and J_{sc} strongly drop with increasing $S_{\text{eff,front}}$ and thus, the front-side interface quality limits J_{sc} and V_{oc} .

The V_{oc} depends strongly on the defect trap density in the defect layer at the rear side. Without defects ($N_{tr} = 0 \text{ cm}^{-3}$) the simulated V_{oc} is 688 mV for 5 μs and 1 cm/s. In figure 6.13 $N_{tr} = 1.3 \times 10^{15} \text{ cm}^{-3}$ to demonstrate the influence of N_{tr} . N_{tr} does not affect simulated J_{sc} results. Interface defects at the rear-side of the absorber were also implemented in [34,47] to achieve a good fit between simulated and measured open-circuit voltages.

In section 6.3 it is demonstrated that the surface recombination velocity with O/N and O/N/O interlayer stack is 4 cm/s and 11 cm/s, respectively. These values are derived under the assumption of certain energy-independent capture cross sections for electrons and holes and stable fixed charges in the interlayer stack. With these parameters it is possible to model EQE curves measured on test cells based on the O/N and O/N/O interlayer stacks. Calculated effective minority charge carrier diffusion lengths are in the range of published results on the same interlayers. In literature, $S_{eff,front}$ values between 100 cm/s and 200 cm/s were estimated on LPC-Si cells based on the interlayer stacks developed in this thesis [34,53]. Overall, it is concluded that the interlayer stacks developed in the framework of this thesis provide a front-side passivation quality between 4 cm/s and 200 cm/s. As can be seen in figure 6.13 in this regime of $S_{eff,front}$, the bulk limits J_{sc} and V_{oc} .

To enhance the efficiency of LPC-Si solar cells, the bulk quality needs to be enhanced, as well as the quality at the rear-side. Furthermore, effective light trapping and coupling techniques need to be introduced to increase J_{sc} to values exceeding 32 mA/cm².

6.7 Conclusions

The passivation quality at the front-side interface between the developed interlayer stack and the LPC-Si absorber is difficult to analyse because common methods applied for silicon wafers are not applicable for thin film silicon solar cells. Therefore, a suitable MIS structure is developed in the framework of this thesis that enables the characterization of the passivation quality using the C-V method.

Using this method, it is demonstrated, that the post-deposition hydrogen treatment at elevated temperatures influences the buried interface between interlayer stack and LPC-Si absorber, mainly by decreasing the defect state density. The increase is more pronounced when a hydrogen plasma is used instead of solely annealing the sample in hydrogen atmosphere. A high positive fixed charge density above 10^{12} cm^{-3} is measured, which results in an accumulation-type passivation at the interface to the n-doped absorber. The open-circuit voltage of test cells, that experienced the same post-deposition treatments as the MIS structures, increases upon the treatments and is highest when the hydrogen plasma is used. It is proposed that this increase is

mainly due to an improved bulk quality, because it is assumed that the front-side is sufficiently passivated by the fixed charges. The results underline the importance of the post-deposition hydrogen plasma treatment and all other samples studied in this thesis receive such a process.

It is found, that the O/N interlayer stack results in a high fixed charge density of $Q_{IL,eff} = (45.0 \pm 4.8) \times 10^{11} \text{ cm}^{-2}$ which is related to the nitrogen-rich character of the developed SiN_x film. The interface defect state density at mid gap with O/N interlayer stack is $D_{it,MG} = (17.8 \pm 4.6) \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$. It is concluded, that the crystallization process and the glass/IL/LPC-Si sequence do not hinder the formation of fixed charges. Instead, the presented results are in line with reported results for the interface between a SiN_x and a silicon wafer. Based on $D_{it,MG}$ and $Q_{IL,eff}$, an effective front-side surface recombination velocity of 3 cm/s is calculated employing the SRH formalism. It is found, that the effective front-side surface recombination velocity is dominated by field-effect passivation provided by the positive fixed charges.

When a thin SiO_x layer is sandwiched between the SiN_x and the LPC-Si material, i.e. when an O/N/O interlayer stack is used, the amount of fixed charges as well as the interface defect state density is reduced by one order of magnitude, which is again in line with results obtained on silicon wafers. Transmission electron microscopy results give evidence for nitrogen in the SiO_x film deposited on the SiN_x layer. It is assumed that nitrogen diffuses from the SiN_x layer into the SiO_x during the deposition process at elevated temperature. If the SiO_x layer is sufficiently thin, nitrogen atoms reach the IL/LPC-Si interface and contribute to $Q_{IL,eff}$. The effective front-side surface recombination velocity at the interface between O/N/O interlayer stack and LPC-Si absorber is calculated to be 10 cm/s.

Solar cells on O/N and O/N/O interlayer stack perform very similar. However, the spread of measured data is slightly higher with O/N interlayer stack as compared to the O/N/O interlayer stack which might be related to thermal instabilities of the SiN_x layer in direct contact with the silicon. By modelling measured EQE curves with ASPIN3 and by using the obtained $S_{eff,front}$ values as input parameters, a diffusion length between 16.6 to 31.0 μm and 18.5 to 23.4 μm is obtained for cells with O/N and the O/N/O interlayer stack, respectively. These results are similar to values published for other LPC-Si samples.

The interlayer stack is developed further by using plasma-oxidation to realize a thin, homogeneous oxygen containing capping layer for the SiN_x layer. It is demonstrated that the employed 10 min-long N_2O plasma is suitable to transform around 9 nm of the SiN_x layer into a SiO_xN_y layer with an effective oxidation growth rate of about 0.013 nm/s. Due to the slow oxidation rate, the thickness of the oxidized layer can be controlled easily. The layers in the interface region appear compact and well-defined and no structural damage upon the plasma treatment is observed by transmission electron microscopy. The layer is thermally stable in direct contact

to the silicon. It is scope of future work to determine $D_{it,MG}$ and $Q_{IL,eff}$ using MIS structures and $C-V$ measurements.

Finally, it is demonstrated using simulations of the short-circuit current density and open-circuit voltage as a function of the effective front-side surface recombination velocity for two different bulk lifetime, that LPC-Si solar cells on the developed interlayer stacks are not limited by the front-side passivation quality, but by the bulk quality as well as by the rear-side passivation quality.

In the next chapter 7 approaches are discussed that potentially increase the bulk quality of LPC-Si solar cells.

CHAPTER 7

Towards an Improved LPC-Si Bulk Quality

7.1 Introduction

As described in chapter 6, the current state of the interlayer development makes the bulk and the rear interface quality the focal point for further improvements of the solar cell devices. This chapter is about approaches to minimize the detrimental effect of bulk defects, either by passivation with hydrogen or by removing them from sites where they are harmful.

A large variety of defects is present in multi-crystalline silicon (mc-Si) material that act as recombination centres for minority charge carriers. The performance of solar cells, that are minority-carrier devices, depends critically on the amount of these defects. The defects are structural defects like grain boundaries, stacking faults, dislocations and intra-grain defects as well as impurities and clusters of impurities. Grain boundaries can host dangling bond defects and they may be decorated with impurities.

Common impurities include transition metals such as chromium (Cr), iron (Fe), aluminium (Al) and nickel (Ni) [158–160]. They originate from the melt, the crucible, handling, chemicals or the process chamber. Impurity concentrations can be measured with techniques such as neutron activation analysis [158, 159], inductively-coupled plasma mass spectrometry [160], secondary ion mass spectroscopy [21, 33, 65, 161, 162], fourier transform infrared spectroscopy [163] Typical impurity concentrations are around 10^{12} to 10^{18} cm⁻³ as depicted in figure 7.1 (a).

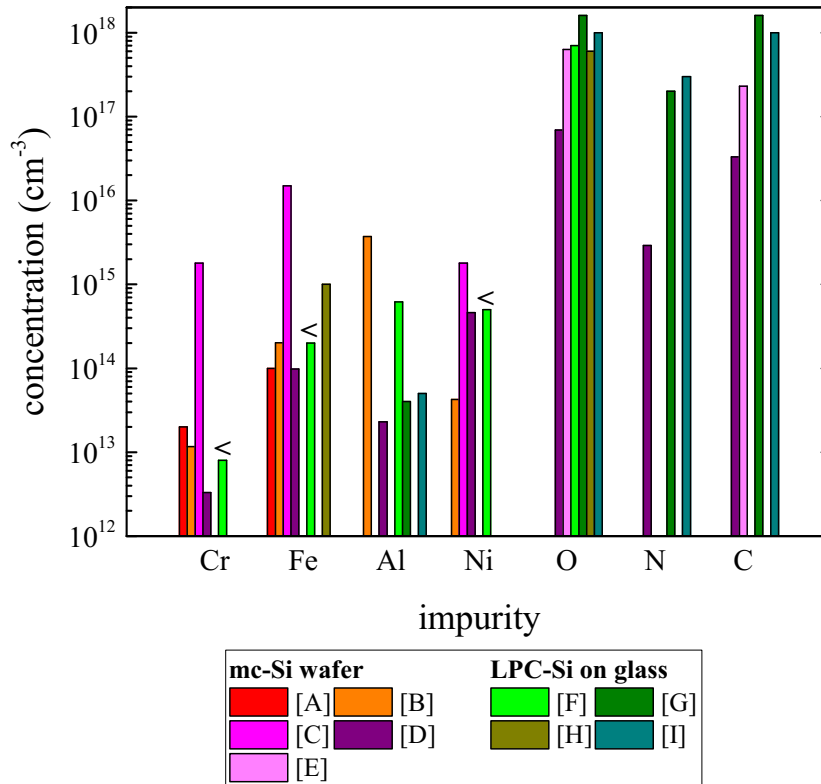


Figure 7.1: Concentrations of selected impurities present in multi-crystalline silicon (mc-Si) silicon wafers and LPC-Si on glass. [A]: [158], [B]: [160], [C]: [159], [D]: [162], [E]: [163] [F]: [21], [G]: [65], [H]: [33] [I]: [161]. Please note, that some impurity concentrations are below the detection limit of the measurement equipment and thus, the displayed values are upper limits (indicated by "<").

Impurities are present in mc-Si material in various forms: as interstitial or substitutional ions or in precipitates of oxides, silicates or silicides [158]. Some impurities such as Fe and Cr are most harmful when present as interstitials [164, 165], others (e.g. Cu [166] and oxygen) appear to have a greater impact when precipitated.

Hydrogen has been shown to be capable of passivating many different types of defects in silicon, such as chemical impurities as well as crystallographic defects [137]. Hydrogen may be introduced using plasma exposure or it may be released in its atomic form from a dielectric layer such as silicon nitride. The SiN_x film of choice should be silicon-rich because it releases hydrogen much faster and in much higher quantities as compared to nitrogen-rich SiN_x films [122, 123].

A hydrogen plasma can also be used as source for hydrogen atoms. When these atoms enter the silicon material, they are present as interstitial hydrogen, before they bond to a defect.

Interstitial hydrogen may exist in three charge states in silicon. It can be positively charged (H^+), neutral (H^0) or negatively (H^-) charged. Illumination may be used to manipulate the charge state of hydrogen. This could be beneficial, because certain defects can only be passivated by a certain charge state of hydrogen. For example, in p-doped silicon, most metallic impurities favour the positive charge state [137]. Therefore, hydrogen should be negatively charged, which can be achieved when illumination is provided during the hydrogen plasma treatment [137, 167].

Gettering is a very effective method to reduce the concentration of interstitial impurities from sites where they are harmful [168–174]. During the getter process, interstitial impurities diffuse to a getter site where they precipitate out. The diffusion process is usually supported by high temperatures between 800 and 900 °C [175]. Getter sites can be either intrinsic, such as grain boundaries, dislocations or oxygen precipitates, or extrinsic, such as highly doped layers at the surface of the silicon. In case of p-doped silicon, diffused emitters provide such a highly phosphorous doped extrinsic getter site and the getter process (known as phosphorous diffusion gettering) can be easily incorporated into the manufacturing process of p-doped silicon solar cells. Since solar cells use nearly the entire bulk, it is more attractive to use external gettering techniques to clean up the silicon bulk, instead of intrinsic gettering sites. When impurities are successfully gettered, the silicon should not be exposed to high temperatures any more since gettered impurities might be released from intrinsic getter sites again.

Plenty of literature exists for gettering of iron. For example, it was found, that 3 to 9 % of the initially dissolved iron concentration remains in the bulk of mc-Si after the high temperature gettering step [176]. Adding a low temperature anneal at 650 °C reduces the initial iron concentration further to around 0.1 % of the initial value due to the greater ratio of solubility limits between the gettering layer and the bulk at lower temperatures.

Impurities and structural defects are also present in LPC-Si material. In LPC-Si, oxygen, nitrogen and carbon are present in high concentrations (figure 7.1). The interlayer stacks composed of SiO_x , SiN_x and SiC_x are potential sources [21, 33, 39, 65]. Figure 7.2 depicts structural defects, i.e. grain boundaries, stacking faults and intra-grain defects, in LPC-Si material detected with the photo-luminescence (PL) technique. The images are recorded from the glass side at an excitation wavelength of 650 nm.

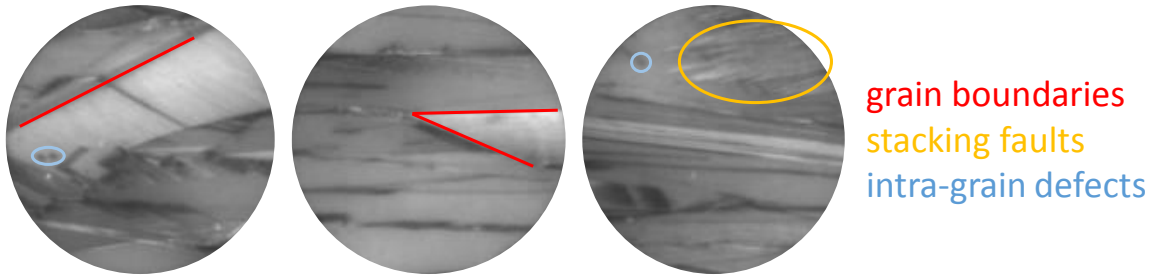


Figure 7.2: PL images of three LPC-Si test cells with a diameter of 8 mm on the developed O/N/ON interlayer stack to illustrate structural defects in the LPC-Si bulk.

It was estimated that grain boundaries and dislocation-rich areas account for 11 to 14 % of current loss in LPC-Si solar cells on glass [53]. Therefore, methods are needed to minimize losses in the LPC-Si bulk. In section 7.2, a hydrogen plasma treatment under illumination is tested and the influence on the open-circuit voltage of LPC-Si test cells is analysed. In section 7.3, a post-deposition gettering treatment is tested on LPC-Si samples on glass. A highly phosphorous-doped (n^+) a -Si:H layer is used and samples are annealed following typical temperature ramps employed for silicon wafers. The affect of the treatments is studied by PL as well as using the sun simulator to measured V_{oc} .

7.2 Hydrogen plasma treatment under illumination

The passivation of defects with a hydrogen plasma as described in section 2.2 is one process step usually performed for the fabrication of LPC-Si solar cells.

During the process, the samples are heated by halogen lamps. The idea is to modify the sample holder such, that the samples face the illumination from the halogen lamps during the hydrogen plasma treatment. Another beneficial effect of such a configuration would be, that plasma damage is avoided. Figure 7.3 (a) depicts the reactor configuration with the advanced sample holder. It is made of stainless steel. Figure 7.3 (b) shows the open-circuit voltage of LPC-Si test cells measured in superstrate configuration using the sun simulator. The samples are n-doped and have an absorber thickness of 8.5 μm .

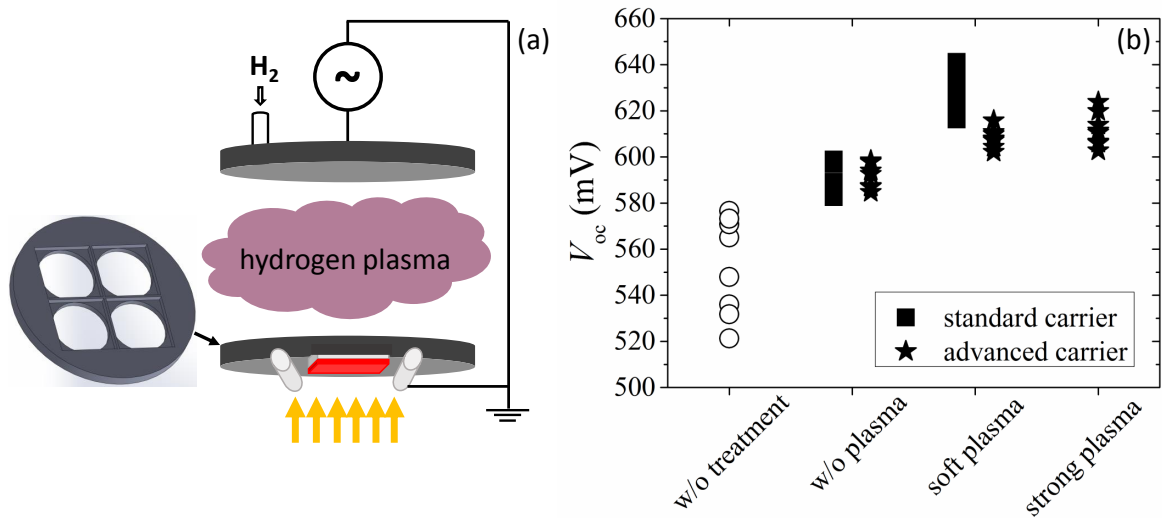


Figure 7.3: Hydrogen plasma treatment under illumination: (a) Sketch of reactor configuration with advanced sample holder and (b) measured V_{oc} results in superstrate configuration of LPC-Si test cells on N/O/ON IL stack. Process conditions: 400 °C, 30 min. Soft plasma: 50 W at 2.5 mbar, strong plasma: 250 W at 0.6 mbar.

It can be seen that annealing in hydrogen atmosphere increases V_{oc} similarly on the standard carrier as well as the advanced carrier, which is, at least partly, related to an improved front-side passivation as demonstrated in section 6.2. When the hydrogen plasma is used, V_{oc} increases, whereby the increase is stronger when the standard carrier is used instead of the advanced samples holder, that allows for a hydrogen plasma treatment under illumination.

One reason might be, that the photon intensity supplied by the halogen lamp is too low. In literature, the influence of the illumination intensity on the efficiency of the hydrogenation process is evaluated [177]. It might also be that metallic impurities from the advanced sample holder diffuse into the silicon absorber during the hydrogen plasma treatment under illumination. It is also probable, that hydrogen atoms from the plasma do not reach the LPC-Si absorber in sufficient quantities, because the sample does not face the plasma.

It is concluded, that this simple modification of the sample holder used for the hydrogen plasma treatment does not result in an increase of the open-circuit voltage of LPC-Si test cells.

7.3 Gettering

Gettering is tested for LPC-Si samples on glass. To this end, LPC-Si samples on the O/N interlayer stack are prepared. The samples have an as-deposited absorber thickness of 15.8 μm . Two different doping concentrations are tested, $N_D = 2 \times 10^{16} \text{ cm}^{-3}$ and $N_D = 6 \times 10^{16} \text{ cm}^{-3}$. After the crystallization process, the samples were annealed at 950 $^{\circ}\text{C}$ for 1 min and the SiO_x capping layer was removed as described in section 2.3.

Then, the 5 cm $\times$ 5 cm samples are split in halve. One half serves as reference and is fabricated to test cells following the standard process steps as described in section 2.3. The other half receives a specific treatment as listed in table 7.1.

Table 7.1: Overview on studied samples for gettering experiments. PH_3 refers to the phosphine flow rate during the deposition of the *a*-Si:H layer. The 650 $^{\circ}\text{C}$ process was performed directly after the 800 $^{\circ}\text{C}$ process. "-" denotes no layer or no annealing.

$N_D \text{ (cm}^{-3}\text{)}$	$\text{PH}_3 \text{ (sccm)}$	annealing time (min)		nomenclature
		800 $^{\circ}\text{C}$	650 $^{\circ}\text{C}$	
6×10^{16}	2	-	-	A
6×10^{16}	0	59	-	B
6×10^{16}	2	15	-	C
6×10^{16}	2	59	-	D
6×10^{16}	-	15	59	E
6×10^{16}	0	15	59	F
6×10^{16}	2	15	59	G
2×10^{16}	-	15	59	H
2×10^{16}	0	15	59	I
2×10^{16}	2	15	59	J

Except for two samples, all samples are capped with an around 50 to 100 nm thin *a*-Si:H layer deposited with the PECVD method at 400 $^{\circ}\text{C}$ heater temperature. The phosphine (PH_3) flow rate during the *a*-Si:H deposition is either 0 sccm, i.e. intrinsic *a*-Si:H(i) layer, to test the influence of hydrogen from the layer on the LPC-Si material quality, or 2 sccm to test the influence of phosphorous. With 2 sccm, the doping concentration of the *a*-Si:H layer is $N_D \approx 1.7 \times 10^{19} \text{ cm}^{-3}$. The two samples that are not capped with an *a*-Si:H layer are used to study the impact of the annealing treatment itself on the LPC-Si material.

Next, a 100 nm thin SiO_x layer is deposited on top of the samples. The idea is to prevent out-diffusion of phosphorus to the ambient during the annealing process, which follows next.

Different annealing treatments are tested as shown in table 7.1. Two samples with an $a\text{-Si:H(n}^+)$ layer, experience 800 °C for 15 and 59 min, respectively. Another sample with $a\text{-Si:H(i)}$ layer is annealed at 800 °C for 59 min. Six other samples are first annealed at 800 °C for 15 min and then at 650 °C for 59 min. The studied annealing treatments are similar to treatments performed in [176]. Before the samples can be removed from the oven, the oven temperature needs to reach 100 °C. Using the highest possible nitrogen flow rate of 10 sccm to enhance the cooling rate, the temperature of the samples drops from 650 °C to below 100 °C within around 15 min. During this rather long cooling process impurities might re-distribute. At 100 °C, the samples are removed from the furnace.

Next, the SiO_x capping layer is removed with hydrofluoric acid (HF). The $a\text{-Si:H(n}^+)$ and around 500 nm of the LPC-Si absorber is removed using the poly-silicon etch solution. The treated samples are combined with the reference samples and all samples experience a hydrogen plasma treatment at 600 °C for 15 min. All subsequent process steps are according to the standard process steps as described in section 2.3.

The effect of the gettering treatments is studied with the photo-luminescence (PL) method. PL images are taken from the glass side using an excitation wavelength of 650 nm. Histograms are extracted from the PL images. The histograms represent a sample area of around 5 cm² and they are normalized with respect to the maximum PL counts.

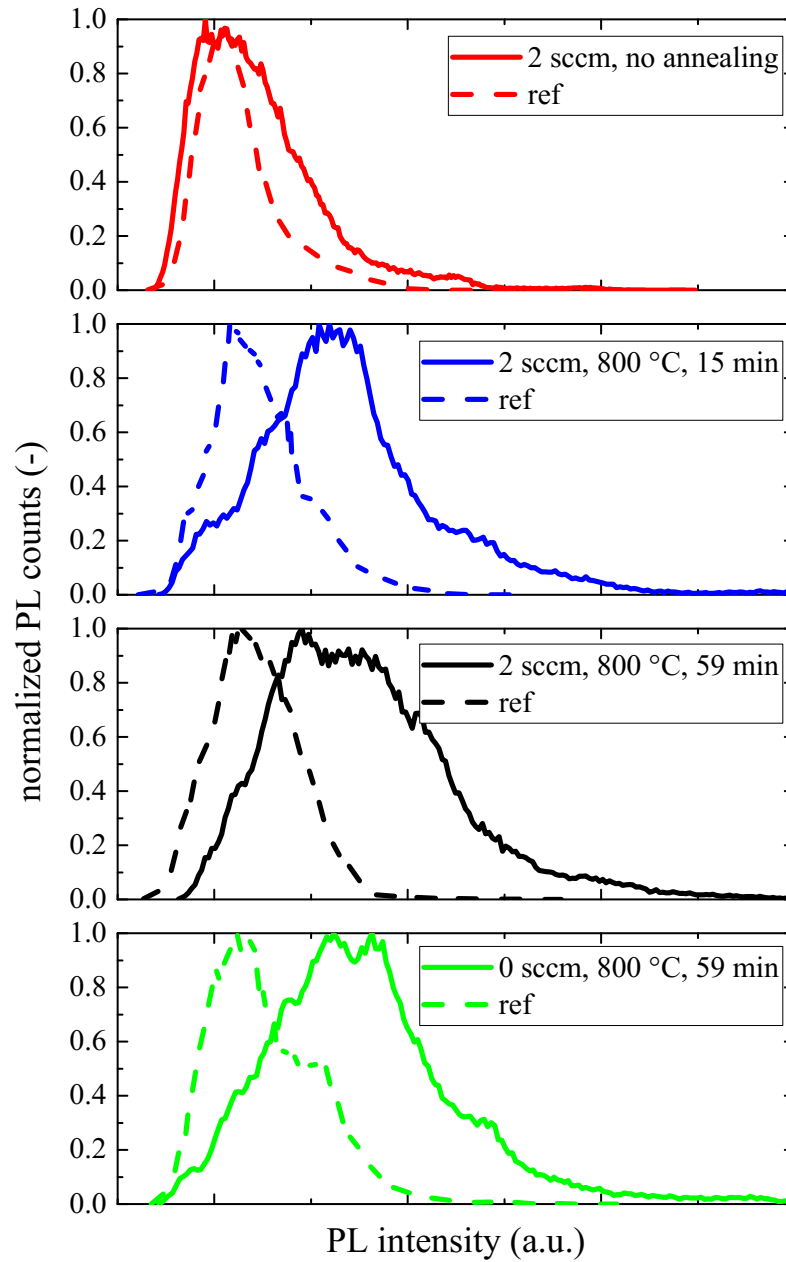


Figure 7.4: PL histograms of treated samples (top to bottom: A, B, C and D in table 7.1) as well as corresponding reference samples.

As can be seen, PL histograms are shifted towards higher PL intensities for all samples that experienced the gettering treatment as compared to the reference samples. This demonstrates that non-radiative recombination processes reduced upon the gettering treatments. The peak widths are broader for treated samples. This can be explained as follows. Grain boundaries are not improved upon the gettering treatments as they act as intrinsic gettering sites. They

remain defect-rich and are responsible for the PL counts at low PL intensities. On the other hand, the PL signals at higher PL intensities demonstrate, that the material quality within the grains increased, because impurities diffuse to getter sites where they reside. These results demonstrate the positive effect of getter treatments on the LPC-Si material quality.

It is evident that annealing is essential to improve the material quality, since the broadening and shift in the PL histogram is significantly reduced without annealing. The role of phosphorus seems not crucial, since the PL histograms representing the samples which were treated with $a\text{-Si:H(i)}$ and $a\text{-Si:H(n}^+)$ layers, appear similar. In addition, from the presented data, it seems as if the duration of the annealing process (15 min or 59 min) is not crucial.

Figure 7.5 displays V_{oc} results measured with the SunsVoc method of the treated samples (closed symbols) as well as of corresponding reference samples (open symbols). All samples are annealed at 800 °C for 15 min followed by 650 °C for 59 min. The samples have two different doping concentrations, this is, $6 \times 10^{16} \text{ cm}^{-3}$ and $2 \times 10^{16} \text{ cm}^{-3}$.

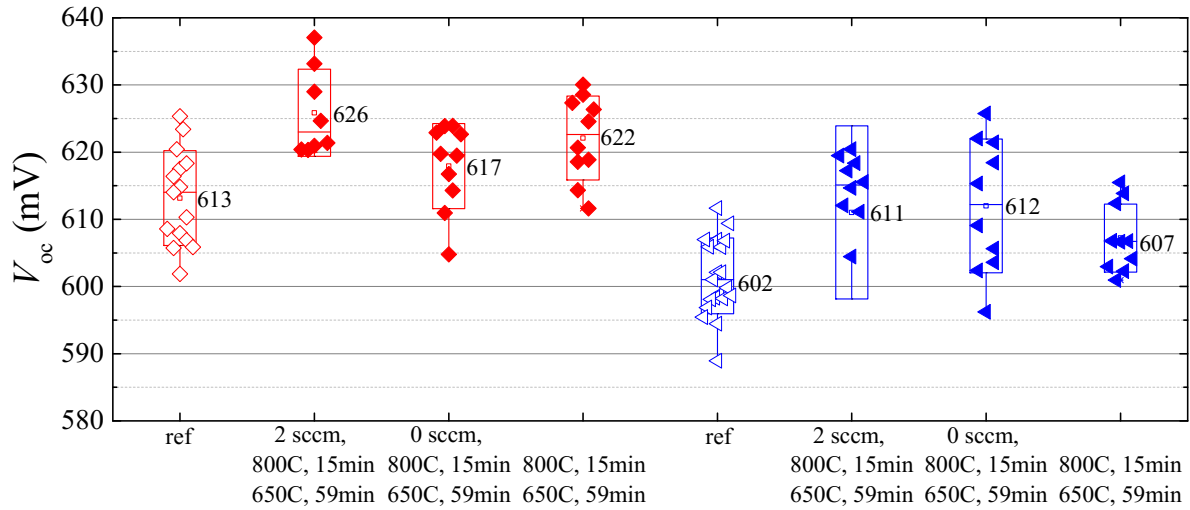


Figure 7.5: V_{oc} results of treated samples (closed symbols) as well as of corresponding reference samples (open symbols). Samples are treated according to processes E, F, G, H, I, and J in table 7.1. For the reference samples, V_{oc} results of each individual half are combined. Absorber doping is $N_D = 6 \times 10^{16} \text{ cm}^{-3}$ (red symbols) and $2 \times 10^{16} \text{ cm}^{-3}$ (blue symbols).

As can be seen, the V_{oc} of the reference samples is on average lower as compared to the treated samples, while V_{oc} results are slightly higher for the samples that have a higher doping concentration. The highest V_{oc} is found for the higher-doped sample which received the $a\text{-Si:H(n}^+)$ layer. However, this treatment does not lead to a higher V_{oc} in case of the lower

doped samples. Overall, the presented data allow the conclusion that annealing leads to an increase in V_{oc} . The influence of hydrogen and phosphorous is not clear.

Iron (Fe) is the most prominent impurity that is gettered and diffusion coefficients of Fe (D_{Fe}) in crystalline silicon are well known. According to Istratov *et al.*, $D_{Fe} = 2.2 \times 10^{-7} \text{ cm}^2/\text{s}$ at 800 °C. By using $L_{diff} = \sqrt{D \times t}$, the distance can be estimated (L_{diff}) that Fe diffuses in a specific time t . In 15 min, Fe diffuses 272 μm which is 18 times more than the thickness of the LPC-Si absorber. Therefore, the results should not be diffusion limited.

7.4 Conclusions

Bulk defects such as impurities (figure 7.1) and grain boundaries (figure 7.2) are present in LPC-Si material and limit the device performance. In this chapter, two approaches were described to improve the LPC-Si bulk quality.

Although the positive effect of a hydrogen plasma treatment under illumination is observed in literature, the simple modification of the sample holder to allow a hydrogen plasma treatment under illumination does not lead to improved LPC-Si quality quantified by the open-circuit voltage. This may be related to a too low illumination intensity. Furthermore, with the advanced sample holder, the sample does not face the hydrogen plasma and it is assumed that hydrogen atoms do not reach the absorber. It might be more promising to use the crystallization laser in hydrogen atmosphere to achieve hydrogenation under illumination as in [177].

Gettering of impurities is seen as a promising method to increase the LPC-Si bulk quality. Preliminary results obtained on LPC-Si samples reveal an increase in the material quality, when samples experience a high-temperature annealing step. PL results indicate the improvement of the material quality inside the grains. Based on the presented data, the influence of phosphorous is not clear.

It is suggested to continue the experiments on getter treatments. Sample should be deposited on the O/N/ON interlayer stack to avoid shunt problems. Shunted test cells were frequently observed for the samples on the O/N interlayer stack which is related to the interaction between the O/N interlayer stack and the LPC-Si/air surface as discussed in section 6.3.3. The impact of gettering should be studied in more detail using LBIC measurements. It is expected, that a line scan across a grain boundary reveals a higher recombination activity when the LPC-Si sample experienced the getter treatment as compared to a reference sample. In addition, a map of the iron distribution in samples with and without gettering treatment would be interesting. For these investigations, the SIMS method could be used.

CHAPTER 8

Summary and Conclusions

Liquid-phase crystallized silicon (LPC-Si) solar cells on glass are based on silicon absorber layers with thicknesses below 40 μm and grain sizes comparable to multi-crystalline silicon wafers. First cells were fabricated in 2011 and exhibited an efficiency of almost 5 % [33]. As depicted in figure 8.1, since then, strong efficiency improvements were achieved through careful developments, in particular of the doping type, the contact system as well as the interlayer stack sandwiched between the glass substrate and the silicon absorber.

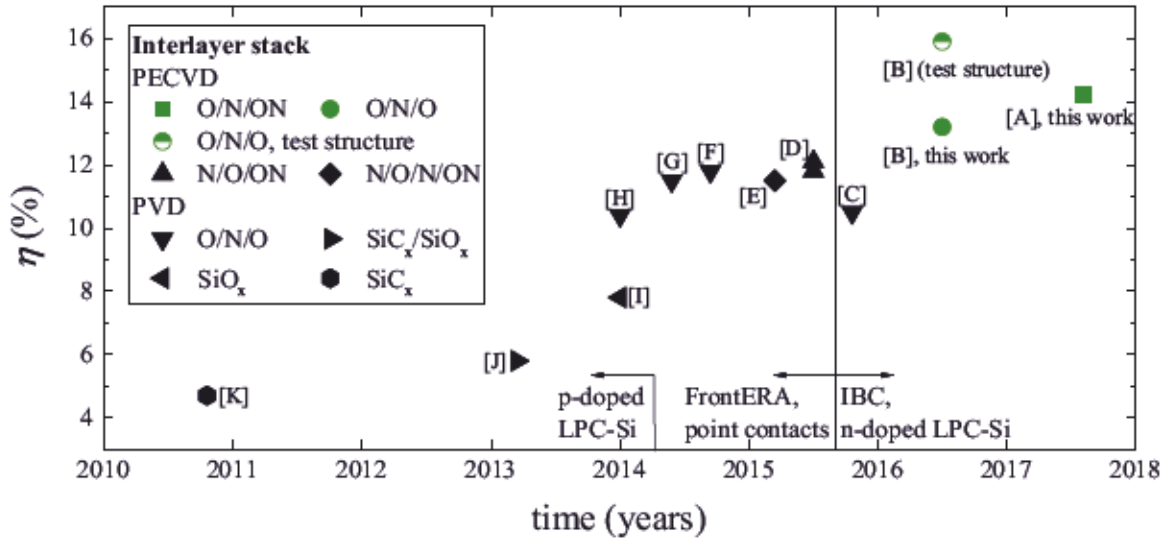


Figure 8.1: Efficiency improvement of solar cells with liquid-phase crystallized silicon absorbers on glass substrates. The improvement is achieved through the use of n-doped instead of p-doped absorber layers, and a careful development of the contact system and the interlayer stack. [A]: [34], [B]: [53], [C]: [37], [D]: [48], [E]: [47], [F]: [19], [G]: [36], [H]: [51], [I]: [61], [J]: [35], [K]: [33]. Green symbols highlight interlayer stacks developed in the framework of this thesis.

The presented thesis, which started in October 2014, focuses on the development and characterization of the interlayer stack. As indicated by figure 8.1, different stacks are used whereby stacks based on silicon carbide were soon replaced by stacks based on amorphous hydrogenated silicon oxide (SiO_x), amorphous hydrogenated silicon nitride (SiN_x) and amorphous hydrogenated silicon oxynitride (SiO_xN_y) due to insufficient passivation and carbon contamination of the absorber. Although plenty of interlayer options were tested and successfully used, detailed investigations of the dielectric layers were not available that would help to understand and explain observed adhesion and passivation properties.

The plasma-enhanced chemical vapor deposition (PECVD) technique is chosen for the interlayer development and characterization in order to profit from the flexibility of process conditions. Sample based on interlayer stacks deposited with PECVD received extended annealing treatments prior to crystallization to reduce the amount of incorporated hydrogen in order to avoid hydrogen effusion and blistering during the crystallization process [39, 40, 46]. This step is unwanted, because it increases manufacturing time. Thus, the first step of the interlayer development addressed the investigation of adhesion properties to develop an interlayer that enables crystallization without the extended annealing procedure.

It is found that SiN_x plays a crucial role for adhesion (figure 5.1). Therefore, the development and characterization focusses on the SiN_x . The refractive indices at 632.8 nm of studied SiN_x films vary from 2.16 (silicon-rich) to 1.85 (nitrogen-rich) and the residual stress is either highly compressive (almost 1.5 GPa) or tensile (up to 1 GPa). The total amount of chemically bonded hydrogen is between $\approx 7 \times 10^{21} \text{ cm}^{-3}$ to $\approx 20 \times 10^{21} \text{ cm}^{-3}$.

Results reveal, that in SiN_x films that enable adhesion during crystallization, hydrogen is only bonded to nitrogen, whereas hydrogen is also bonded to silicon in films that lead to delamination. The bonding configuration of hydrogen seems to be the most crucial parameter to achieve adhesion during crystallization. The total amount of chemically bonded hydrogen seems not to be as crucial for adhesion. In addition, if the residual stress is approaching 1 GPa either compressive or tensile it is assumed that it is also partly responsible for delamination of the films during crystallization. The SiN_x films that enable adhesion are characterized by a tensile stress below 400 MPa (figure 5.4).

Developed SiN_x and SiO_x films are suitable as interlayer stack in terms of their optical properties. On the one hand, they are transparent between 260 nm and 1100 nm (figure 5.7). The SiO_x film has a similar refractive index to the glass substrate and thus, its thickness can be increased to provide a sufficient diffusion barrier for impurities from the glass substrate. The refractive index of the SiN_x is slightly too low to serve as ideal anti-reflection coating. However, all SiN_x films with a higher refractive index delaminated during the crystallization process. The thickness of the SiO_x layer adjacent to the silicon absorber influences reflection losses (figure 5.8). In the short-wavelength regime, reflection is significantly increased with increasing SiO_x thickness. However, the potential short-circuit current density that can be extracted from the cell is not significantly influenced due to the low photon flux in the AM1.5 spectrum (figure 5.9). Therefore, the SiO_x layer thickness adjacent to the silicon absorber can be chosen to optimize the passivation quality, which is summarized next.

The investigation of the passivation quality at the buried interface between the interlayer stack and the LPC-Si absorber is not straightforward, since the interface is not easily accessible with electrical measurement techniques and common methods to determine the minority charge carrier lifetime are not applicable for thin crystalline silicon absorbers. In the framework of this thesis a metal-insulator-semiconductor (MIS) structure based on LPC-Si on glass is developed that is compatible to capacitance-voltage ($C-V$) measurements. This technique is used to determine the interface defect state density (D_{it}) as well as the effective interlayer charge density ($Q_{IL,eff}$) at the buried interface of LPC-Si samples on glass.

Using this method, it is proven that annealing at elevated temperatures reduces the defect states density at the interface between the interlayer stack and the LPC-Si absorber. The reduction is significantly increased when a hydrogen plasma is ignited (figure 6.1). These results contribute

significantly to the understanding of the commonly applied postdeposition treatments used to increase the material quality of crystallized thin silicon absorbers.

The developed nitrogen-rich SiN_x layer is characterized by a high amount of fixed charges ($> 10^{12} \text{ cm}^{-2}$) while the SiO_x layer offers a reduced defect state density ($10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ at mid gap) (table 6.2). Therefore, the passivation mechanism is similar as to SiO_x and SiN_x layers that are deposited on a silicon wafer as reported in literature (table 6.3). Using the extended Shockley-Read-Hall (SRH) model, an effective front-side surface recombination velocity of 4 and 11 cm/s is calculated for the passivation quality with O/N and O/N/O interlayer stack, respectively. Both interfaces are dominated by field-effect passivation supplied by the high amount of fixed charges.

It is found that LPC-Si solar cells on the O/N and O/N/O interlayer stack perform similar (figures 6.7 and 6.8). By modelling measured EQE curves (figure 6.9), an effective minority charge carrier diffusion length between 16.6 to 31.0 μm and 18.5 to 23.4 μm is calculated for samples on the O/N and O/N/O interlayer stack, respectively, which is in the range of published results.

The use of the O/N interlayer layer has drawbacks. First, the SiN_x film in direct contact to the silicon might not be stable, leading to nitrogen contaminations in the LPC-Si bulk and at the LPC-Si/air interface. Furthermore, a slight reduction of the density of fixed charges in the SiN_x film, for example due to charge carrier transfer across the interface, results in a strong increase of the effective front-side surface recombination velocity, because the high amount of defect states start to take part in recombination processes. In the O/N/O interlayer stack, the challenge is the deposition of a homogeneous, thin SiO_x film with the PECVD method, since the passivation quality is sensitive to its thickness (figure 6.4).

Therefore, plasma-oxidation of the SiN_x layer is tested as alternative to the PECVD method. Detailed investigations of the interface region with transmission electron microscopy demonstrate, that a 10 min-long N_2O plasma transforms around 9 nm of the SiN_x film into a SiO_xN_y film while layers are well-defined and no plasma-damage is observed. The effective oxidation rate is low (0.013 nm/s) and thus, the thickness of the SiO_xN_y film is well controllable.

Results of an LPC-Si solar cell with interdigitated back-contacts based on the developed O/N/ON interlayer exhibits a record efficiency of 14.2 % (table 6.5).

Using simulated solar cell parameters it is demonstrated that in the current state of interlayer development, the performance of LPC-Si solar cells is limited by the bulk quality and rear-side passivation rather than by the front-side passivation quality (figure 6.13).

In order to further increase the efficiency of LPC-Si solar cells, implementation of adapted light trapping schemes at the front-side of the absorber is needed to raise J_{sc} above 32 mA/cm² [178, 179]. One promising way to increase the bulk quality is to use the gettering method which would reduce the amount of impurities inside grains. Preliminary experiments in the framework of this thesis demonstrate the improvement of the bulk quality upon the treatments using the photo-luminescence technique and open-circuit voltages. Up to now, annealing seems to be a crucial improvement factor. However, further research is necessary to understand in detail the factors that lead to the improved bulk quality and to optimize the treatment conditions.

APPENDIX A

Overview PECVD Deposition Parameters of Dielectric Layers

For the development of the interlayer stack the plasma-enhanced chemical vapor deposition (PECVD) method is chosen because layer properties can be tuned of a wide range due to multi-fold process conditions. Table A.1 lists the process conditions used for the dielectric layers discussed in this thesis.

Figure A.1 depicts the temperature on top of a 0.7 mm thin glass substrate as a function of the heater temperature in the PECVD chamber "PC1" in the Von Ardenne CS400PS cluster tool.

Table A.1: Overview of all PECVD process conditions used for dielectric layers studied in this thesis. d is the distance between the electrodes. The deposition rate r as well as $n_{632.8\text{ nm}}$ were determined from ellipsometry measurements on corresponding single layer/silicon wafer stacks. Layers are differentiated with consecutive letters.

nomenclature	SiH ₄ (scm)	N ₂ O (scm)	NH ₃ (scm)	CO ₂ (scm)	N ₂ (scm)	H ₂ (scm)	power (P) (W)	pressure (p) (mbar)	d (mm)	T (°C)	r (nm/s)	$n_{632.8\text{ nm}}$
Von Ardenne CS400PS cluster tool, "PCI" chamber												
SiO10	4	80	0	0	0	100	50	0.5	13	400	0.57	1.55
SiO13	8	100	0	100	0	0	100	0.5	13	400	0.14	1.47
SiO14	8	100	0	100	0	0	100	0.5	13	600	1.10	1.51
SiO19	8	100	0	100	0	0	160	0.5	13	600	1.10	1.47
SiO20	2	100	0	100	0	0	160	1.0	13	600	0.10	1.46
SiN5	2	0	0	0	100	0	76	1.3	13	400	0.20	1.95
SiN9	4	0	0	0	100	0	220	0.7	13	600	0.41	2.13
SiN15	4	0	3	0	100	0	170	0.8	13	600	0.47	2.12
SiN19	4	0	3.5	0	100	0	130	0.8	13	600	0.49	2.16
SiN21	3	0	3.5	0	100	0	130	0.8	13	600	0.29	1.89
SiN22	2	0	3.5	0	100	0	130	0.8	13	600	0.20	1.85
SiN23	6	0	48	0	0	0	40	1.3	13	600	0.96	1.95
SiN24	6	0	48	0	0	0	70	1.3	13	600	0.79	1.92
SiN25	6	0	48	0	0	0	120	1.3	13	600	0.82	1.90
SiN26	6	0	48	0	0	0	160	1.3	13	600	0.61	1.91
SiN29	3	0	10	0	100	0	130	0.8	13	600	0.28	1.90
SiON5	2	0	0	4	100	0	60	1.3	13	400	0.25	1.70
AKT1600 PECVD cluster tool, "ChB" chamber												
SiN _x	20	0	0	0	1200	0	250	2.0	1200	400	0.34	2.06
SiO _x	4	0	0	100	0	200	600	1.3	650	400	0.24	1.44
SiO _x N _y	10	0	0	20	500	0	600	1.3	650	400	0.49	1.77

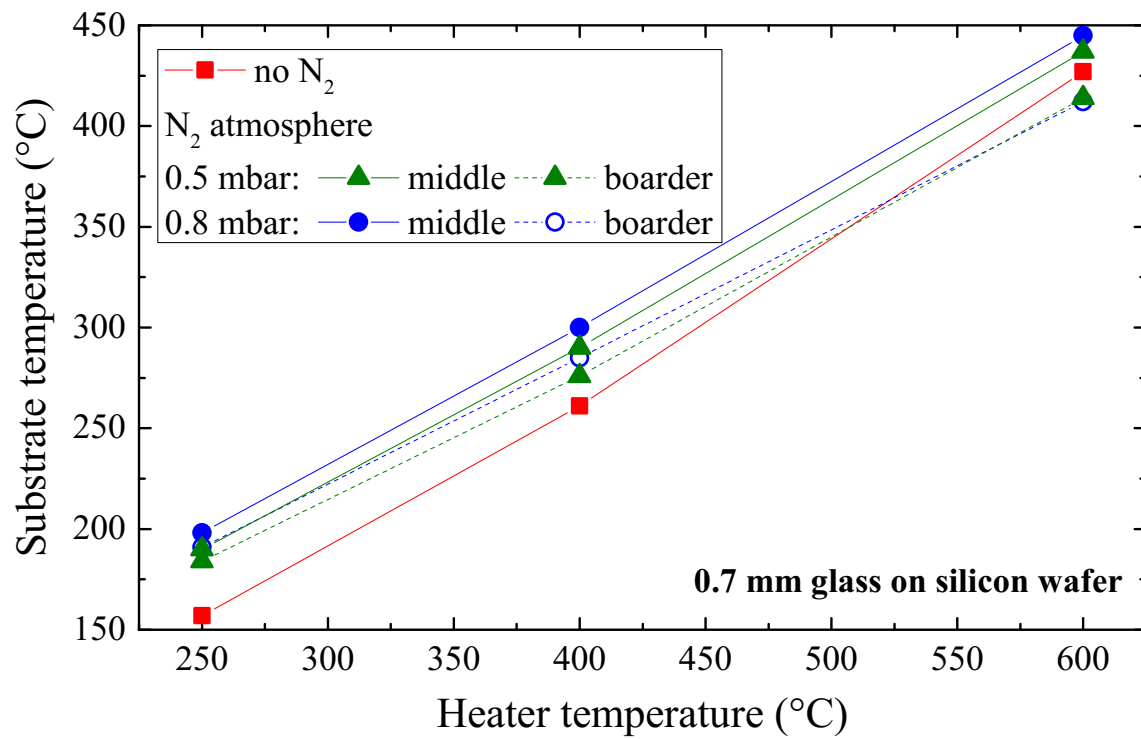


Figure A.1: Temperature calibration for PECVD chamber "PC1" in the Von Ardenne CS400PS cluster tool.

APPENDIX B

Adhesion Properties for Variety of Samples

A variety of glass/IL/LPC-Si samples on different interlayer stacks is tested for adhesion during crystallization which is presented in this chapter B. The crystallization parameters are the same for all crystallization processes. Different forms of delamination are not distinguished.

Figure B.1 shows photographs of the samples after the crystallization process. Details on corresponding interlayer stacks including the information if adhesion is observed are supplied in table B.1.

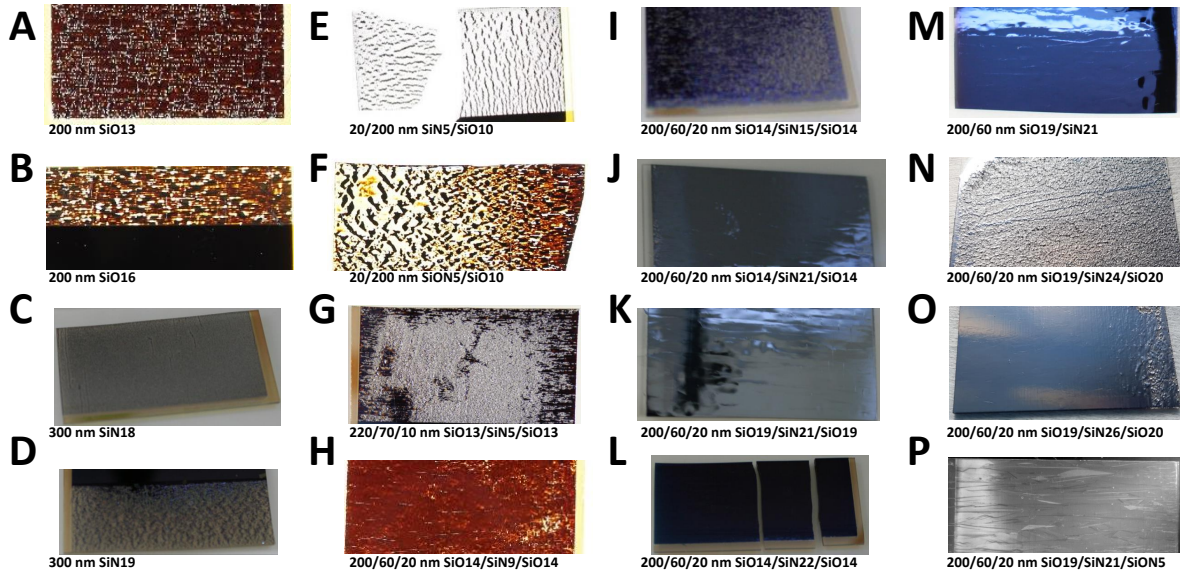


Figure B.1: Photographs of silicon absorbers after crystallization based on different interlayer stacks. Process conditions of individual layers are listed in table A.1. Displayed sample area is $\approx 2.5 \text{ cm} \times 5 \text{ cm}$.

Table B.1: Various interlayer (IL) stacks tested for adhesion during the crystallization process. The layers are distinguished by the assigned nomenclature, for example SiN15 or SiN21. Corresponding process conditions are listed in table A.1. Layer thicknesses are obtained from ellipsometry measurements on corresponding single layer/silicon wafer stacks.

sample number	IL stack	IL thickness (nm)	adhesion during crystallization
A	SiO13	200	✗
B	SiO16	200	✗
C	SiN18	300	✗
D	SiN19	300	✗
E	SiN5/SiO13	20/200	✗
F	SiON5/SiO10	20/200	✗
G	SiO13/SiN5/SiO13	220/70/10	✗
H	SiO14/SiN9/SiO14	200/60/20	✗
I	SiO14/SiN15/SiO14	200/60/20	✗
J	SiO14/SiN24/SiO20	200/60/20	✗
K	SiO19/SiN26/SiO20	200/60/20	✗
L	SiO14/SiN21/SiO14	200/60/20	✓
M	SiO19/SiN21/SiO19	200/60/20	✓
N	SiO14/SiN22/SiO14	200/60/20	✓
O	SiO19/SiN21/SiON5	200/60/20	✓
P	SiO19/SiN21	200/60	✓

Wetting is observed for all stacks with SiN21 and SiN22 (named "group A SiN_x"). The variation of the thin (< 30 nm) layer between the SiN21 and the silicon does not affect adhesion. Furthermore, the SiO_x film between glass and SiN21 is varied (SiO14 and SiO19) without affecting adhesion. When other SiN_x layers are used (SiN9, SiN15, SiN19, SiN23, SiN26), dewetting occurred (named "group B SiN_x").

None of the samples is annealed prior to the crystallization process. It is observed that crystallization is successful for all samples when they are annealed at 950 °C for 1 min prior to crystallization, except for the sample with a single SiN19 as interlayer.

APPENDIX C

Calculation of Surface Recombination Velocity Based on SRH Theory

C.1 Mathematical background

The aim is to calculate the surface recombination velocity (S_{eff}) at the interface between a dielectric layer and silicon based on the SRH theory (equation (4.9)) [117]. In order to determine S_{eff} , the charge carrier densities at the interface (n_s and p_s) need to be known. In the following the procedure to calculate n_s and p_s is described. Relevant parameters are illustrated in figure 4.2.

The charge carrier densities (n and p) are represented by a term describing thermal equilibrium (electron density at thermal equilibrium (n_0) and hole density at thermal equilibrium (p_0)), i.e. no illumination and/or applied voltage. In case of excitation, a term describing the excess charge carrier densities (Δn and Δp) is added. $\Delta n(x) = \Delta p(x)$ applies for a quasi-neutral bulk. x is the distance from the interface towards the silicon bulk perpendicular to the interface.

$$\begin{aligned} n(x) &= n_0 + \Delta n(x) \\ p(x) &= p_0 + \Delta p(x) = p_0 + \Delta n(x) \end{aligned} \tag{C.1}$$

The concentration of charge carriers is directly linked to the electron quasi-Fermi level (ϕ_n) and the hole quasi-Fermi level (ϕ_p) [70, p. 85]

$$\begin{aligned}\phi_n(x) &= \psi(x) - V_{th} \times \ln \left(\frac{n(x)}{n_i} \right) \leftrightarrow n(x) = n_i \times \exp \left(-\frac{\phi_n(x)}{V_{th}} \right) \exp \left(\frac{\psi(x)}{V_{th}} \right) \\ \phi_p(x) &= \psi(x) + V_{th} \times \ln \left(\frac{p(x)}{n_i} \right) \leftrightarrow p(x) = n_i \times \exp \left(\frac{\phi_p(x)}{V_{th}} \right) \exp \left(-\frac{\psi(x)}{V_{th}} \right)\end{aligned}\quad (C.2)$$

with the potential (ψ) and the thermal voltage (V_{th}). As a side note, under thermal equilibrium conditions, ϕ_n and ϕ_p coincide with the Fermi energy (E_F). At the edge of the space-charge region located at $x = d$, $\psi(d) = 0$ V (figure 4.2) and it follows

$$\begin{aligned}\phi_n(d) &= -V_{th} \times \ln \left(\overbrace{\frac{n_0 + \Delta n(d)}{n_i}}^{n(d)} \right) \leftrightarrow n(d) = n_i \times \exp \left(-\frac{\phi_n(d)}{V_{th}} \right) \\ \phi_p(d) &= V_{th} \times \ln \left(\overbrace{\frac{p_0 + \Delta n(d)}{n_i}}^{p(d)} \right) \leftrightarrow p(d) = n_i \times \exp \left(\frac{\phi_p(d)}{V_{th}} \right)\end{aligned}\quad (C.3)$$

In order to determine n_s and p_s it is assumed that ϕ_n and ϕ_p are constant throughout the space-charge region, thus $\phi_n(0) = \phi_n(d)$ and accordingly for holes. By merging equations (C.2) and (C.3) for the condition $x = 0$, the expressions for n_s and p_s are derived:

$$\boxed{\begin{aligned}n_s &= (n_0 + \Delta n(d)) \times \exp \left(\frac{\psi_s}{V_{th}} \right) \\ p_s &= (p_0 + \Delta n(d)) \times \exp \left(-\frac{\psi_s}{V_{th}} \right)\end{aligned}}\quad (C.4)$$

n_0 and p_0 are calculated based on the mass action law ($n_0 \times p_0 = n_i^2$, with the *intrinsic electron density* (n_i)) and the assumption that all doping atoms are ionized:

$$\begin{aligned}n_0 &= N_D \quad \text{and} \quad p_0 = \frac{n_i}{N_D} \quad \text{for n-doped silicon} \\ p_0 &= N_A \quad \text{and} \quad n_0 = \frac{n_i}{N_A} \quad \text{for p-doped silicon}\end{aligned}\quad (C.5)$$

As shown in equations (C.4), n_s and p_s depend exponentially on ψ_s . ψ_s is determined by satisfying charge neutrality in the space-charge region as suggested by Girisch *et al.* [94]:

$$\boxed{Q_{\text{scr}}(\psi_s) + Q_{\text{it}}(\psi_s) + Q_g + Q_f = \delta} \quad (\text{C.6})$$

with $Q_{\text{scr}}(\psi_s)$, $Q_{\text{it}}(\psi_s)$ and Q_g calculated according to equations (C.7), (C.8) and (C.9), respectively. Ideally, δ should be zero. In the simulations performed in the framework of this thesis, $\delta \approx 10^7 \text{ cm}^{-3}$. Q_f is obtained from C-V measurements.

$$Q_{\text{scr}}(\psi_s) = -\text{sign}(\psi_s) \sqrt{2V_{\text{th}}\epsilon_r} \left[\exp\left(\frac{\phi_p(d) - \psi_s}{V_{\text{th}}}\right) - \exp\left(\frac{\phi_p(d)}{V_{\text{th}}}\right) + \exp\left(\frac{\psi_s - \psi_n(d)}{V_{\text{th}}}\right) - \exp\left(-\frac{\phi_n(d)}{V_{\text{th}}}\right) + \frac{\psi_s}{V_{\text{th}}} \frac{N_a - N_d}{n_i} \right]^{\frac{1}{2}} \quad (\text{C.7})$$

$$Q_{\text{it}} = - \int_{E_v}^{E_c} D_{\text{it},a}(E) f_a(E) dE + \int_{E_v}^{E_c} D_{\text{it},d}(E) f_d(E) dE$$

$$f_a(E) = \frac{\sigma_n n_s + \sigma_p n_i \exp\left(\frac{-(E-E_i)}{k_B T}\right)}{\sigma_n [n_s + n_i \exp\left(\frac{(E-E_i)}{k_B T}\right)] + \sigma_p [p_s + n_i \exp\left(\frac{-(E-E_i)}{k_B T}\right)]} \quad (\text{C.8})$$

$$f_d(E) = \frac{\sigma_p p_s + \sigma_n n_i \exp\left(\frac{(E-E_i)}{k_B T}\right)}{\sigma_n [n_s + n_i \exp\left(\frac{(E-E_i)}{k_B T}\right)] + \sigma_p [p_s + n_i \exp\left(\frac{-(E-E_i)}{k_B T}\right)]}$$

$f_a(E)$ and $f_d(E)$ are the occupation functions of the acceptor and donor traps, respectively. Per definition, donor traps are neutral when occupied by an electron and positively charged when unoccupied. Acceptor traps are neutral, when unoccupied and negatively charged when occupied by an electron.

$$Q_g = -\frac{1}{d_{\text{IL}}} \left(\frac{Q_f \times d_{\text{fixed charges}}}{2} + \epsilon_0 \times \epsilon_{\text{IL},r} \times (\psi_s - V_g) \right) \quad (\text{C.9})$$

$d_{\text{fixed charges}}$ is the fixed charge layer thickness.

C.2 Sensitivity analysis

Input parameters for the code are, aside from the doping concentration (N), the excess charge carrier density (Δn) and the fixed charge density ($Q_{\text{IL,eff}}$) (figure 4.4), the energy dependent interface defect state density ($D_{\text{it}}(E)$) and the capture cross sections of electrons and holes for a given defect (σ_n and σ_p , respectively). Figure C.1 illustrates the dependence of the effective

front-side surface recombination velocity ($S_{\text{eff,front}}$) on the excess charge carrier density (Δn). As can be seen, $S_{\text{eff,front}}$ does not depend on Δn , if $\Delta n < 10^{16} \text{ cm}^{-3}$.

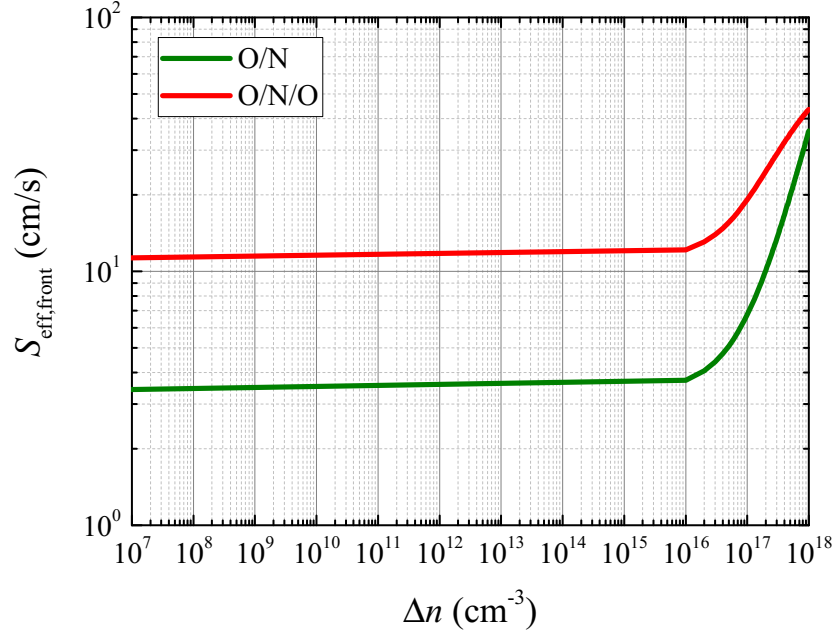


Figure C.1: Simulated effective front-side surface recombination velocity ($S_{\text{eff,front}}$) as a function of excess charge carrier density (Δn). Simulations are based on the extended SRH formalism. No gate electrode, thus, the Q_g is set to zero.

C.3 MATLAB code

Seff_final_Dita_Ditd_import.m

```

1 clear all;
2 clc;
3 close all;
4
5 prompt = 'Please enter 1 = n-doped; 2 = p-doped: ';
6 selection = input(prompt);
7 prompt = 'Lower energy cut-off for integration of Dit [eV] (e.g. -0.3): ';
8 min_value_t = input(prompt);
9 prompt = 'Upper energy cut-off for integration of Dit [eV] (e.g. 0.3): ';
10 max_value_t = input(prompt);
11 prompt = 'Step size for integration of Dit [eV] (e.g. 0.01): ';
12 step_size_t = input(prompt);
13 prompt = 'Starting value for surface potential [eV] (e.g. -0.7): ';
14 min_value_p = input(prompt);
15 prompt = 'Stop value for surface potential [eV] (e.g. 0.7): ';
16 max_value_p = input(prompt);
17 prompt = 'Iteration step size for surface potential [eV] (e.g. 0.00001): ';
18 step_size_p = input(prompt);
19
20 input_parameters;
21 input_constants;
22
23 Dita_import = importdata('Dita_average_interpoliert_68a_ON_02eV.txt');
24 % import Dita (acceptor-like traps, upper half band gap ≥ 0 eV) data in same ...
    amount as t
25 Ditd_import = importdata('Ditd_average_interpoliert_68a_ON_02eV.txt');
26 % import Ditd (donor-like traps, lower half band gap < 0 eV) data in same ...
    amount as t
27
28 for q=1:length(Qf)
29     % variable q: variation of Qf
30
31     %initialization before for loop
32     Qtotfinal=zeros(length(Dn),1);
33     psisfinal=zeros(length(Dn),1);
34     nsfinal=zeros(length(Dn),1);
35     psfinal=zeros(length(Dn),1);
36     Us=zeros(length(Dn),1);
37     d=1;
38

```



```

39     for d=1:length(Dn)
40         % variable d: variation of Dn
41         [Qtotfinal(d),psisfinal(d),nsfinal(d),psfinal(d)] = ...
            nsfinal_psisfinal_Dita_Ditd_import(Dn(d), Qf(q), ...
            Dita_import, Ditd_import, min_value_t, max_value_t, step_size_t, ...
            min_value_p, max_value_p, step_size_p, sigmap0, sigman0, Vth, n0, ...
            ni, p0, epsilonsi, e, k, T, ddielectric, epsilondielectric);
42
43         Qtotfinal(d)
44         % display vector values in workspace
45
46         nsfinal(d) = (n0+Dn(d))*exp(psisfinal(d)/Vth);
47         % surface electron density as a function of psis
48         psfinal(d) = (p0+Dn(d))*exp(-psisfinal(d)/Vth);
49         % surface hole density as a function of psis
50
51         % Dit = Nitintegration of Dit dE to obtain Nit [cm-2] for Us
52
53         % energy steps [eV]
54         b=1;
55         % control variable
56         Us(d)=0;
57         % setting at beginning: Us(b=1)=0; will be overwritten with result from ...
            loop with variable t
58
59         %initialization before for loop
60         number_of_iterations_t = ...
            intl6(((((-1)*min_value_t)+max_value_t)/step_size_t) + 1);
61         Et=zeros(number_of_iterations_t,1);
62         n1=zeros(number_of_iterations_t,1);
63         p1=zeros(number_of_iterations_t,1);
64         Sp0=zeros(number_of_iterations_t,1);
65         Sn0=zeros(number_of_iterations_t,1);
66
67         for t = min_value_t:step_size_t:max_value_t
68             % variable t: variation of trap energy; assumption: Dit constant ...
                for -0.2 eV < Ei < 0.2 eV
69                 Et(b) = t + dE/2;
70                 % trap energy [eV]
71                 Ei = 0;
72                 % intrinsic energy level; energy axis chosen such, that Ei=0eV [eV]
73
74                 n1(b) = ni*exp((Et(b) - Ei)/(8.617e-5*T));
75                 % statistical factor [Aberle1992] [cm-3]
76                 p1(b) = ni*exp(-(Et(b) - Ei)/(8.617e-5*T));
77                 % statistical factor [Aberle1992] [cm-3]
78

```

```

79         Sp0(d) = vthp * sigmap0 * Dit_import(b) * dE;
80         % interface recombination velocity parameter of holes [cm/s]
81         Sn0(d) = vthn * sigman0 * Dit_import(b) * dE;
82         % interface recombination velocity parameter of electrons [cm/s]
83
84
85         Us(d) = (nsfinal(d)*psfinal(d)-ni^2) / ((nsfinal(d)+n1(b))/Sp0(d) ...
86             + (psfinal(d)+p1(b))/Sn0(d)) + Us(d);
87         % SRH interface recombination rate [cm-2s-1]; calculated Us(q) is ...
88         % used as new input above
89
90         b=b+1;
91     end
92
93     Seff(d) = Us(d)/Dn(d);
94     % interface recombination velocity [cm*s]
95
96     Seff_matrix(d,q) = Us(d)/Dn(d);
97     %Seff_matrix for plot
98     d= d+1;
99 end
100
101 %%% PLOT RESULTS
102 %%% uncomment for plot if Dn variation
103 % plot(Dn, Seff, 'color', cl(q))
104 % hold on
105 % set(gca, 'xscale','log');
106 % set(gca, 'yscale','log');
107 % set(gca,'YTick',[0.1 1 10 100 1000 10000 100000 1000000 10000000])
108 % xlim([1e6 1e18])
109 % ylim([10e-2 1e7])
110
111 % SAVE RESULTS INTO EXCEL FILE
112
113 filename = 'Seff_Dn_Qf_Dit.xlsx';
114 col_header = {'Excess charge carrier density Dn [cm-3]', 'Surface ...
115             recombination velocity [cm/s]', 'Fixed charge density [cm-2]'};
116 sheet = q;
117 xlRange = 'A1';
118 xlswrite(filename,col_header,sheet,xlRange)
119
120 for w=1:length(Dn)
121     qtrans(w,1)=Qf(q);
122     % write fixed charges into column vector
123 end
124
125 % transpose

```

```

123     Dntrans = Dn';
124     Sefftrans = Seff';
125
126     filename = 'Seff_Dn_Qf_Dit.xlsx';
127     B = [Dntrans, Sefftrans, qtrans];
128     sheet = q;
129     xlRange = 'A2';
130     xlswrite(filename,B,sheet,xlRange)
131 end
132
133 %PLOT RESULTS QF, Seff, comment if DN variation
134 figure
135 for asd=1:1:size(Seff_matrix,1);
136     plot(Qf, Seff_matrix(asd,:))
137     xlabel('Qf')
138     ylabel('Seff')
139     hold on
140     set(gca, 'xscale','log');
141     set(gca, 'yscale','log');
142     set(gca,'YTick',[0.1 1 10 100 1000 10000 100000 1000000 10000000])
143     xlim([1e6 1e18])
144     ylim([10e-2 1e7])
145 end;

```

nsfinal_psisfinal_psisfinal_Dita_Ditd_import.m

```

1 function [Qtotfinal,psisfinal,nsfinal,psfinal] = ...
    nsfinal_psisfinal_psisfinal_Dita_Ditd_import(Dn, Qf, Dita_import, ...
    Ditd_import, min_value_t, max_value_t, step_size_t, min_value_p, ...
    max_value_p, step_size_p,sigmap0, sigman0, Vth, n0, ni, p0, epsilonsi, e, ...
    k, T, ddielectric, epsilondielectric)
2
3     phin = - Vth*log((n0+Dn)/ni);
4     % quasi-Fermi level for electrons at edge of interface space-charge ...
        region; assumption: constant in SCR [eV]
5     phip = + Vth*log((p0+Dn)/ni);
6     % quasi-Fermi level for holes at edge of interface space-charge region; ...
        assumption: constant in SCR [eV]
7
8     % VARIAION OF psis TO SATISFY CHARGE NEUTRALITY: Qtot = Qf + Qg + Qsi + ...
        Qit < Δ
9     % INTPUT: Qf, Dn (taken from file Seff_final_Dit_import.m), OUTPUT: psis ...
        (which satisfies Qtot < Δ), ns, ps
10

```

```

11     a=1;
12     % control variable
13
14     %initialization before for loop
15     iteration_number_of_iterations=int16(((((-1) * iteration_min_value) + ...
16         iteration_max_value) / iteration_step_size) + 1);
17     psis=zeros(iteration_number_of_iterations,1);
18     ns=zeros(iteration_number_of_iterations,1);
19     ps=zeros(iteration_number_of_iterations,1);
20     fa=zeros(iteration_number_of_iterations,1);
21     fd=zeros(iteration_number_of_iterations,1);
22     Qg=zeros(iteration_number_of_iterations,1);
23     B=zeros(iteration_number_of_iterations,1);
24     Qsi=zeros(iteration_number_of_iterations,1);
25     Qit=zeros(iteration_number_of_iterations,1);
26
27     for p = min_value_p:step_size_p:max_value_p
28         % variable p: variation of psis
29
30         psis(a) = p;
31
32         ns(a) = (n0+Dn)*exp(psis(a)/Vth);
33         % surface electron density as a function of psis
34         ps(a) = (p0+Dn)*exp(-psis(a)/Vth);
35         % surface hole density as a function of psis
36
37         % CHARGES
38         % Qg [C*cm-2]: charge density in gate metal
39         % Vg = 0;
40         % gate voltage [V]
41         % Qg(a) = -1/ddielectric*(Qf*dQf/2 + epsilondielectric*(psis(a)-Vg));
42         Qg(a) = 0;
43
44         % Qsi [C*cm-2]: charge density accumulated in silicon
45         A = 2*Vth*ni*epsilonsi;
46         B(a) = exp((phip-psis(a))/Vth) - exp(phip/Vth) + ...
47             exp((psis(a)-phin)/Vth) - exp(-phin/Vth) + psis(a)/Vth*(p0-n0)/ni;
48         Qsi(a) = -sign(psis(a))*(A*B(a))^(1/2);
49
50         % Qit [C*cm-2]: charge density trapped in defect states
51         % integration of Dit dE to obtain Nit [cm-2] for Qit
52         b=1;
53         % control variable
54         Qit(a)=0;
55         % setting at beginning: Qit(a,b=1)=0; will be overwritten with result ...
56         from loop with variable t

```

```

55
56     %initialization before for loop
57     integration_number_of_iterations = int16(((((-1) * min_value_p) + ...
58         max_value_p) / step_size_p) + 1);
59     Et=zeros(integration_number_of_iterations,1);
60     n1=zeros(integration_number_of_iterations,1);
61     p1=zeros(integration_number_of_iterations,1);
62
63     for t = min_value_t : step_size_t : max_value_p
64         % variable t: variation of trap energy; assumption: Dit constant ...
65         % for -0.2 eV < Ei < 0.2 eV
66
67         Et(b) = t + step_size_t/2;
68         % trap energy [eV]
69         Ei = 0;
70         % intrinsic energy level; energy axis chosen such, that Ei=0eV [eV]
71
72         n1(b) = ni*exp((Et(b) - Ei)/(8.617e-5*T));
73         % statistical factor [Aberle1992] [cm-3]
74         p1(b) = ni*exp(-(Et(b) - Ei)/(8.617e-5*T));
75         % statistical factor [Aberle1992] [cm-3]
76
77         fa(a) = (sigman0*ns(a)+sigmap0*p1(b))/(sigman0*(ns(a)+n1(b)) + ...
78             sigmap0*(ps(a)+p1(b)));
79         % occupation function of acceptor trap [-]
80         fd(a) = (sigman0*n1(b)+sigmap0*ps(a))/(sigman0*(ns(a)+n1(b)) + ...
81             sigmap0*(ps(a)+p1(b)));
82         % occupation function of donor trap [-]
83
84         Qit(a)= step_size_t*e*(fd(a)*Dita_import(b) - ...
85             fa(a)*Ditd_import(b)) + Qit(a);
86
87     b=b+1;
88     end
89
90     Qtot(a) = abs(Qf *e + Qit(a) + Qsi(a) + Qg(a));
91     % magnitude of charge density total [C*cm-2]
92     a=a+1;
93     end
94
95     % find minimum of vector Qtot(a) -> = Qtot
96     Qtotfinal=Qtot(1);
97     % assumption: Qtot(a=1) = minimum
98
99     for c=2:length(Qtot)
100         % length(Qtot) given by variation window of variable p
101         difQtot(c)=Qtot(c)-Qtotfinal;

```

```

97         % difference
98         if difQtot(c)<0
99             % satisfaction of Qtot = 0
100            Qtotfinal=Qtot(c);
101            % if difference (ci+1 - ci) < 0 -> Qtotfinal from above is ...
              replaced with Qtot(ci)
102            psisfinal=psis(c);
103            nsfinal=ns(c);
104            psfinal=ps(c);
105        end
106        c=c+1;
107    end
108 end

```

input_parameters.m

```

1  epsilon_rdielectric = 3.7;
2  % relative permittivity of dielectric layer [-]
3  ddielectric = 250e-7;
4  % thickness of dielectric layer [cm]
5
6  dQf = 3e-7;
7  % fixed oxide charge layer thickness [cm]
8
9  sigmap0 = 1e-16;
10 % hole capture cross section of neutral state [cm2]
11 sigman0 = 1e-14;
12 % electron capture cross section of neutral state [cm2]
13
14 % ELECTRON AND HOLE CONCENTRATION AT THERMAL EQUILIBRIUM
15 ni = 1e10;
16 % instrinsic carrier concentration in silicon at 300 K [cm-3]
17 NA = 1e16;
18 % acceptor concentration [cm-3]; note: NA = p0
19 ND = 1e17;
20 % donor concentration [cm-3]; note: ND = n0
21
22 if selection == 1
23     n0 = ND;
24     % hole density at thermal equilibrium [cm-3]
25     p0 = ni^2/ND;
26     % electron density at thermal equilibrium [cm-3]
27 elseif selection == 2
28     p0 = NA;

```

```

29     % hole density at thermal equilibrium [cm-3]
30     n0 = ni^2/NA;
31     % electron density at thermal equilibrium [cm-3]
32 else
33     disp('Please correct your input.')
34 end;
35
36 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
37 % Dn [cm-3]: excess charge carrier density at edge of space charge region
38     % Dn = [1e6 1e7 1e8 1e9 1e10 1e11 1e12 1e13 1e14 1e15 1e16 1e17 1e18];
39     % Dn = [1e12 2.5e12 5e12 7.5e12 1e13 2.5e13 5e13 7.5e13 1e14 2.5e14 5e14 ...
40             7.5e14 1e15 2.5e15 5e15 7.5e15 1e16 2.5e16 5e16 7.5e16 1e17 2.5e17 ...
41             5e17 7.5e17 1e18 2.5e18 5e18 7.5e18 1e19];
42     % excess carrier concentration at edge of interface space-charge region ...
43     [cm-3]
44     % Dn = [1e14 1e15 1e16];
45     Dn = 1e14;
46     % Dn = input('Enter excess carrier concentration in cm-3 = ');
47
48 % Qf [cm-2]: fixed charge density in interlayer
49     % Qf = 1e10;
50     % fixed charge density in insulator [cm-2]
51     % cl = 'b';
52     % define colors for each Of
53     %Qf = [1e10 1e11 1e12 1e13];
54     %cl = ['b' 'k' 'r' 'g'];
55     Qf = [1e10 2.5e10 5e10 7.5e10 1e11 2.5e11 4.3e11 5e11 7.5e11 1e12 1.57e12 ...
56           2.5e12 4.03e12 4.26e12 4.5e12 5e12 7.5e12 1e13];
57     cl = ['b' 'k' 'r' 'g' 'b' 'k' 'r' 'g' 'b' 'k' 'r' 'g' 'b' 'k' 'r' 'g' 'b' ...
58           'k'];
59     %Qf = input('Enter fixed insulator charge density in cm-2 = ');
60
61 % Dit [eV-1cm-2]: interface defect state density
62     % Dit = 1e11;
63     % interface defect state density [eV-1cm-2]
64     % Dit = input('Enter interface defect state density in cm-2 = ');

```

input_constants.m

```

1 % CONSTANTS
2
3 e = 1.602e-19;
4 % elementary charge [C]
5 k = 1.381e-23;

```

```
6 % Boltzmann constant [J/K]
7 T = 300;
8 % temperature [K]
9 Vth = k*T/e;
10 % thermal voltage [V]
11
12 % MATERIAL PROPERTIES
13
14 mo = 9.1e-31;
15 % free electron rest mass [kg]
16 mthp = 0.41*mo;
17 % thermal velocity effective mass of holes [kg] [Green1990]
18 mthn = 0.28*mo;
19 % thermal velocity effective mass of electrons [kg] [Green1990]
20
21 vthp = sqrt(8*k*T/(mthp*pi))*100;
22 % hole thermal velocity [cm/s]
23 vthn = sqrt(8*k*T/(mthn*pi))*100;
24 % electron thermal velocity [cm/s]
25 sprintf('thermal velocity of holes in cm/s = %d', vthp)
26 sprintf('thermal velocity of electrons in cm/s = %d', vthn)
27
28 epsilon0 = 8.854e-14;
29 % permittivity of vaccum [C/(V*cm)]
30 epsiloninsi = 11.9;
31 % relative permittivity of silicon [-]
32 epsiloninsi = epsiloninsi*epsilon0;
33 % permittivity of silicon [C/(V*cm)]
34 epsilonindielectric = epsiloninsidielectric*epsilon0;
35 % permittivity of dielectric layer [C/(V*cm)]
```


APPENDIX D

Publications, Presentations and Patent

D.1 Publications

As lead author

1. N. Preissler, J. A. Töfflinger, I. Shutsko, O. Gabriel, S. Calnan, B. Stannowski, B. Rech, and R. Schlatmann (2016). *Interface Passivation of Liquid-Phase Crystallized Silicon on Glass Studied with High-Frequency Capacitance-Voltage Measurements*. Phys. Status Solidi A, 213(7):1697-1704 / DOI 10.1002/pssa.201532957
2. N. Preissler, J. A. Töfflinger, O. Gabriel, P. Sonntag, D. Amkreutz, B. Stannowski, B. Rech and R. Schlatmann (2017). *Passivation at the interface between liquid-phase crystallized silicon and silicon oxinitride in thin film solar cells*. Prog. Photovolt: Res. Appl., 25(7):515-524 / DOI 10.1002/pip.2852
3. N. Preissler, D. Amkreutz, P. Sonntag, M. Trahms, R. Schlatmann, and B. Rech (2017). *Interface Engineering for Liquid-Phase Crystallized Silicon Solar Cells on Glass*. Sol. RRL, 1(3-4):1700015 / DOI 10.1002/solr.201700015
4. N. Preissler, C. Thi Trinh, M. Trahms, P. Sonntag, D. Abou-Ras, H. Kirmse, R. Schlatmann, B. Rech, and D. Amkreutz. *Impact of Dielectric Layers on Liquid-Phase Crystallized Silicon Solar Cells*. Accepted for publication in IEEE Journal of Photovoltaics

As co author

1. D. Amkreutz, N. Preissler, C. Trinh, M. Trahms, P. Sonntag, R. Schlatmann, B. Rech (2017). *Influence of the precursor layer composition and deposition processes on the electronic quality of liquid phase crystallized silicon absorbers*. Accepted for publication in Prog. Photovolt: Res. Appl.
2. C. Thi Trinh, N. Preissler, P. Sonntag, M. Muske, K. Jäger, M. Trahms, R. Schlatmann, B. Rech, D. Amkreutz (2017). *Potential of Interdigitated Back-Contact Silicon Heterojunction Solar Cells for Liquid-Phase Crystallized Silicon on Glass with efficiency above 14 %*. Solar Energy Materials & Solar Cells, 174:187-195 / DOI 10.1016/j.solmat.2017.08.042
3. P. Sonntag, M. Bokalic, N. Preissler, D. Amkreutz, B. Rech, M. Topic (2017). *Liquid Phase Crystallized Silicon - A Holistic Absorber Quality Assessment*. Article in press in Solar Energy Materials & Solar Cells / DOI 10.1016/j.solmat.2017.08.019
4. P. Sonntag, N. Preissler, M. Bokalič, M. Trahms, J. Haschke, R. Schlatmann, M. Topič, B. Rech, D. Amkreutz (2017). *Silicon solar cells on glass with power conversion efficiency above 13 % at thickness below 15 micrometer*. Scientific reports, 7(1):873 / DOI 10.1038/s41598-017-00988-x
5. T. Frijnts, N. Preissler, S. Gall, S. Neubert, B. Rech, R. Schlatmann (2017). *Influence of the frontside charge inversion layer on the minority carrier collection in backside contacted liquid-phase crystallized silicon on glass solar cells*. Sol. RRL, 1(9):1700100 / DOI 10.1002/solr.201700100
6. O. Gabriel, T. Frijnts, N. Preissler, D. Amkreutz, S. Calnan, S. Ring, B. Stannowski, B. Rech, R. Schlatmann (2015). *Crystalline silicon on glass - interface passivation and absorber material quality*. Prog. Photovolt: Res. Appl., 24(12):1499-1512 / DOI 10.1002/pip.2707

D.2 Oral presentations

1. N. Preissler, J. A. Töfflinger, I. Shutsko, O. Gabriel, S. Calnan, D. Amkreutz, B. Stannowski, B. Rech, R. Schlatmann. Date: 17.09.2015. *On Defects and Interface Passivation of Thin Crystallized Silicon Absorbers for Next Generation Solar Cells on Glass*. ICANS26, Aachen
2. N. Preissler, J. A. Töfflinger, O. Gabriel, P. Sonntag, D. Amkreutz, B. Rech, R. Schlatmann. Date: 22.06.2016. *Passivation at the Interface between Liquid-Phase Crystallized Silicon and Silicon Oxynitride in Thin Film Solar Cells*. 32nd EU PVSEC, Munich

3. N. Preissler, C. Trinh, M. Trahms, P. Sonntag, D. Abou-Ras, H. Kirmse, R. Schlatmann, B. Rech, D. Amkreutz. Date: 27.06.2017. *Impact of Dielectric Layers on Liquid-Phase Crystallized Silicon Solar Cells*. 44th IEEE PVSC, Washington D.C.

D.3 Poster presentations

1. I. Shutsko, N. Preissler, J. A. Töfflinger, O. Gabriel, R. Schlatmann. Date: 24.09.2015. *On Defects and Interface Passivation of Thin Crystallized Silicon Absorbers for Next Generation Solar Cells on Glass*. Summer school, Berlin

D.4 Patent application

1. B. Stannowski, O. Gabriel, N. Preissler, R. Schlatmann, Halbleiter-Bauelement mit vorder- und rückseitiger Elektrode und Verfahren zu dessen Herstellung, DE 102016110965 7

APPENDIX E

List of Symbols and Acronyms

Symbol	Description	Unit
k_B	Boltzmann constant	J/K
q	elementary charge	C
α	absorption coefficient	cm^{-1}
E_c	conduction band edge	eV
E_v	valence band edge	eV
E_i	intrinsic energy level	eV
E_F	Fermi energy	eV
ϕ_n	quasi-Fermi level of electrons	eV
ϕ_p	quasi-Fermi level of holes	eV
Δn	excess charge carrier density	cm^{-3}
n_i	intrinsic electron density	cm^{-3}
n_s	surface electron density	cm^{-3}
p_s	surface hole density	cm^{-3}
n_0	electron density at thermal equilibrium	cm^{-3}
p_0	hole density at thermal equilibrium	cm^{-3}
N_A	acceptor doping density	cm^{-3}
N_D	donor doping density	cm^{-3}
v_{th}	thermal velocity of electrons and holes	cm/s
μ	charge carrier mobility	cm^2/Vs
τ_b	bulk lifetime	μs
$L_{\text{diff,eff}}$	effective minority charge carrier diffusion length	μm
$Q_{\text{IL,eff}}$	effective interlayer charge density	cm^{-2}
Q_f	fixed charge density	cm^{-2}

Symbol	Description	Unit
Q_{scr}	charge density in space charge region	cm^{-2}
Q_{it}	interface charge density	cm^{-2}
Q_g	charge density in gate metal	cm^{-2}
D_{it}	interface defect state density	$\text{cm}^{-2}\text{eV}^{-1}$
$D_{it,MG}$	interface defect state density at mid gap energy	$\text{cm}^{-2}\text{eV}^{-1}$
$S_{eff,rear}$	effective rear-side surface recombination velocity	cm/s
$S_{eff,front}$	effective front-side surface recombination velocity	cm/s
σ_n	capture and emission cross section of electrons	cm^2
σ_p	capture and emission cross section of holes	cm^2
V_g	gate voltage	V
V_{scr}	voltage across space charge region	V
V_{ms}	work function difference between metal and semiconductor	V
V_{oc}	open-circuit voltage	V
V_{th}	thermal voltage	V
ψ_s	surface potential	V
C_{IL}	capacitance of interlayer	$\frac{s^2 \times C^2}{m^2 \times kg}$
C_{SCR}	capacitance of space charge region	$\frac{s^2 \times C^2}{m^2 \times kg}$
R_s	sheet resistance	Ω
J_{sc}	short-circuit current density	A/cm^2
$J_{sc,max}$	short-circuit current density potential	A/cm^2
R	reflection	%
η	energy conversion efficiency	%
EQE	external quantum efficiency	%
IQE	internal quantum efficiency	%
FF	fill factor	%
pFF	pseudo fill factor	%
σ_f	residual stress	Pa
ω	wave number	cm^{-1}
k	extinction coefficient	cm^{-1}
x	stoichiometry	
n	refractive index	
C-V	capacitance-voltage	
J-V	current-voltage	
<i>a</i> -Si:H	amorphous hydrogenated silicon	
(i) <i>a</i> -Si:H	intrinsic amorphous hydrogenated silicon	
(n) <i>a</i> -Si:H	n-type amorphous hydrogenated silicon	

Symbol	Description	Unit
(p) <i>a</i> -Si:H	p-type amorphous hydrogenated silicon	
μ c-Si:H	micro-crystalline hydrogenated silicon	
mc-Si	multi-crystalline silicon	
<i>c</i> -Si	crystalline silicon	
Al	aluminium	
AlO _x	amorphous aluminium oxide	
ARC	anti-reflection coating	
ARF	anti-reflection foil	
BSF	back surface field	
CO ₂	carbon dioxide	
CVD	chemical vapour deposition	
CTE	coefficient of thermal expansion	
Cr	chromium	
Cz-Si	Czochralski silicon	
FTIR	fourier transform infrared spectroscopy	
H ₂	hydrogen	
HPT	hydrogen plasma treatment	
IBC	interdigitated back-contact	
IL	intermediate layer	
IQE	internal quantum efficiency	
ITO	indium-tin-oxide	
KOH	potassium hydroxide	
LPC	liquid phase crystallization	
LPC-Si	liquid phase crystallized silicon	
LBIC	light-beam induced current	
MILC	metal induced layer exchange	
MIS	metal-insulator-semiconductor	
MG	mid gap	
N ₂	nitrogen	
N ₂ O	nitrous oxide	
NH ₃	ammonia	
PECVD	plasma-enhanced chemical vapor deposition	
PL	photo-luminescence	
PV	photovoltaics	
PVD	physical vapour deposition	
QSSPC	quasi-steady state photoconductivity	

Symbol	Description	Unit
RIE	reactive ion etching	
SEM	scanning electron microscopy	
SHJ	silicon hetero-junction	
SIMS	secondary ion mass spectroscopy	
SiN _x	amorphous silicon nitride	
Si ₃ N ₄	stoichiometric silicon nitride	
SiO ₂	stoichiometric silicon oxide	
SiO _x	amorphous silicon oxide	
SiO _x N _y	amorphous silicon oxinitride	
SiC _x	amorphous silicon carbide	
SiH ₄	monosilane	
SPC	solid-phase crystallization	
SR	spectral response	
SRH	Shockley-Read-Hall	
STEM-EELS	scanning transmission electron microscopy and electron energy loss spectroscopy	
Ti	titanium	
TEM	transmission electron microscopy	
TCO	transparent conducting oxide	
XPS	X-ray photoelectron spectroscopy	
ZnO	zinc-oxide	
ZMR	zone-melting recrystallization	

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APPENDIX I

Statement of Authorship

I, Natalie Preissler, declare on oath that I completed the present work on my own and that information which has been directly or indirectly taken from other sources has been noted as such.

Berlin, October 2017