GaN-HEMT Power Amplifiers and Smart Transmitters for *Ku*-Band Satellite Communication

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Abstract

Daniel Maaßen

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Smart Transmitters for Ku-Band
Satellite Communication

Within this contribution the design, implementation, and experimental results of a satellite communication (SatCom) power amplifier (PA), block upconverter (BUC) as well as an evaluation within the satellite link are described. Three *Ku*-band GaN-HEMT PAs are presented.

A two stage design approach with two 250 nm bare-die devices has been chosen to achieve a considerably high saturated gain of 15 dB over the whole extended *Ku*-band (13.75 - 14.5 GHz). The circuit is realised in a hybrid microwave integrated circuit (MIC) technology on an alumina substrate. The PA shows a measured performance of more than 50 W output power for a continuous wave (CW) signal with a power added efficiency (PAE) higher than 23%. Modulated measurements (QPSK) demonstrate an average output power of more than 30 W (70 W peak) and 21% PAE, while holding the Eutelsat linearity requirements.

The design procedures used were extended to a second PA in a lower frequency range of 12.75 - 13.25 GHz achieving more than 80 W output power for pulsed RF signals with 34% PAE. This thesis proposes a third PA design which covers both up-link frequency bands (12.75 - 14.5 GHz) and achieves more than 55 W output power with 20% PAE. This achieved 14% fractional bandwidth (FBW) design is equal to the theoretical limit of a broadband matching at $f_0 = 13.25$ GHz for the chosen bare-dies.

The developed BUC is supposed to work within a very small aperture terminal (VSAT). Here an integration of either a developed 10 W or a 50 W amplifier within this BUC is shown that comes along with a small size and low weight, paired with a low amount of dissipated power. Additionally, the BUC is equipped with a linearisation technique that automatically improves the spectral regrowth for common modulation schemes (QPSK, 8PSK), as well as for future higher order modulation like 16APSK, 32APSK (DVB-S2X).

Finally, the BUC is tested with a VSAT in a satellite link and demonstrates its function with data rates of up to 1 Mbit/s.

Zusammenfassung

Daniel Maaßen

GaN-HEMT Power Amplifiers and Smart Transmitters for Ku-Band Satellite Communication

Diese Arbeit beschäftigt sich mit der Entwicklung, dem Aufbau sowie der messtechnischen Evaluierung von Leistungsverstärkern (PA) und einem Block Up-Converter (BUC) für die Satellitenkommunikation. Im Verlauf der Arbeit werden drei verschiedene GaN-HEMT PA's im Detail aufgeführt.

Ein zwei-stufiges Verstärkerdesign, welches zwei gleich große 250 nm bare-dies GaN-HEMTs verwendet, wurde ausgewählt, um einen akzeptable Verstärkung von 15 dB im extended *Ku*-band (13.75 - 14.5 GHz) zu erreichen. Die Schaltung wurde als microwave integrated circuit (MIC) auf einem Aluminiumoxid Trägerkeramik entwickelt. Mit diesem Verstärkerkonzept wurden mehr als 50 W Ausgangsleistung, mit einer power added efficiency (PAE) von mehr als 23%, für eine continuous wave (CW) Anregung erreicht. Auch modulierte Signale (z.B. QPSK) wurden verwendet, wodurch eine Ausgangsleistung von 30 W (70 W peak) und 21% PAE erreicht wurden, während die Linearitätsbestimmungen der Eutelsat Regulierung erfüllt wurden.

Die beschriebenen Entwicklungstechniken wurden des Weiteren dafür verwendet, einen zweiten Leistungsverstärker für den Frequenzbereich von 12.75 -13.25 GHz aufzubauen. Dieser zeigt mehr als 80 W Ausgangsleistung bei einer PAE $\geq 34\%$ für gepulste Signale. Eine dritte Entwicklung zielte darauf ab, einen einzigen Verstärker in beiden Frequenzbereichen verwenden zu können (12.75 -14.5 GHz). Dieser definiert mit 14% fractional bandwidth (FBW) die theoretisch maximale Bandbreite bei $f_0 = 13.25$ GHz und erreicht eine Ausgangsleistung von 55 W bei einer reduzierten PAE von 20%.

Zur Verwendung der PA's in einem very small aperture terminal (VSAT) wurde ein BUC entwickelt, der durch eine geringe Größe, ein geringes Gewicht und eine niedrige Leistungsaufnahme besticht. Außerdem konnte eine aktive Linearisierung implementiert werden, die eine signifikante Verbesserung von Schulterabständen erreicht. Diese Technik wurde sowohl für aktuelle Modulationsarten (QPSK, 8PSK) als auch für künftige mit höherer Ordnung wie 16APSK, 32APSK (DVB-S2X) evaluiert.

Abschließend wurde der BUC in Kombination mit einem VSAT im Satelliten Link getestet und zeigt Sende-Datenraten von bis zu 1 Mbit/s.

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List of Abbreviations

2DEG	Two Dimensional Electron Gas
2D	Two Dimensional
3D	Three Dimensional
3G	3rd Generation mobile communication
5G	5th Generation mobile communication
ACLR	Adjacent chanel leakage ratio
ACPR	Adjacent chanel power ratio
AM	Amplitude Modulation
AM/AM	Amplitude to Amplitude Modulation
AM/PM	Amplitude to Phase Modulation
BB	Base Band frequency
BER	Bit Error Rate
BUC	Block up-converter
BP	Band Pass
CAD	Computer-aided design
CAE	Computer-aided engeneering
T-CAD	Technology-Computer-aided design
CW	Continous Wave
DPD	Digital predistortion
DUT	Device under Test
DVB-S	Digital Video Broadcasting-Satellite
DVB-S2	Digital Video Broadcasting-Satellite 2nd Generation
DVB-S2x	Digital Video Broadcasting-Satellite 2x future Generation
EIRP	Effective Isotropic Radiated Power
ESR	Equivalent Series Resistance
EVM	Error Vector Magnitude
EM	Electro Magnetic
ET	Envelope Tracking
FBW	Fractional Bandwidth
FDTD	Finite-Difference Time-Domain Method
FEC	Forward Error Correction
FEM	Finite Element Method
FET	Field Effect Transistor
FP	Field Plate
FSS	Fixed Satellite Services
FWL	Forward Link
GaN	Gallium Nitride
GaAs	Gallium Arsenide
GEO	Geosynchronous Earth Orbit
GND	Ground Potential
GSG	Ground Signal Ground
GSOLT	General Short Open Load Thru calibration
HEMT	High Electron Mobility Transistor
HP	High Pass
HTS	High throughput Satellite
IBO	Input back off
IF	Intermediate Frequency
IL	Insertion Loss
IMD	Inter modulation distortion
IMD3	3rd order Inter modulation distortion
IMD5	5th order Inter modulation distortion
IMN	Input Matching Network
ISISTAR	Integrated Satellite Terminal for stationary Networks

ISMN	**I**nter **S**tage **M**atching **N**etwork
ISV	**I**ndividual **S**ource **V**ia
LDMOS	**L**aterally **D**iffused **M**etal **O**xide **S**emiconductor
LEO	**L**ow **E**arth **O**rbit
LNB	**L**ow **N**oise **B**lock converter
LO	**L**ocal **O**scillator
LP	**L**ow **P**ass
LVDS	**L**ow **V**oltage **D**ifferential **S**ignal
MIC	**M**icrowave **I**ntegrated **C**ircuit
MMIC	**M**onolithic **M**icrowave **I**ntegrated **C**ircuit
MS	**M**icro-**S**trip
MuFLoC	**Mu**lti **F**requency **Lo**ad-pull **C**ontours
OBO	**O**utput **b**ack **o**ff
OMN	**O**utput **m**atching **n**etwork
OMT	**O**rthogonal **m**ode **t**ransducer
PA	**P**ower **A**mplifier
PAE	**P**ower-**a**dded **E**fficiency
PDE	**P**artial**D**ifferential **E**quations
PCB	**P**rinted **c**ircuit **b**oard
PAPR	**P**eak-to-**a**verage **p**ower **r**atio
PLL	**P**hase **L**ocked **L**oop
PLO	**P**hase **L**ocked **O**scillator
PM	**P**hase **M**odulation
PSD	**P**ower **s**pectral **d**ensity
PSK	**P**hase **s**hift **k**eying
QAM	**Q**uadrature **A**mplitude **M**odulation
RL	**R**eturn **L**oss
RTL	**R**e**t**urn **L**ink
RF	**R**adio **F**requency
RFPAL	**R**adio **F**requency **P**ower **A**mplifier **L**inearisation
RFPD	**R**adio **F**requency **P**re **D**istortion
RHP	**R**ight **H**alf **P**lane
RX	**R**eceive
SIW	**S**ubstrate **I**ntegrated **W**ave-guide
SNR	**S**ignal **N**oise **R**atio
SPICE	**S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis
SRF	**S**elf **R**esonant **F**requency
SSB	**S**ingle **S**ide **B**and
SSPA	**S**olid **S**tate **P**ower **A**mplifier
TCP	**T**ransmission **C**ontrol **P**rotocol
TDR	**T**ime **D**omain **R**eflection
TCAD	**T**echnology **C**omputer **A**ided **D**esign
TDMA	**T**ime **D**ivision **M**ultiple **A**ccess
TL	**T**ransmission **L**ine
TOI	**T**hird **O**rder **I**ntercept
TRL	**T**hru **R**eflect **L**ine calibration
TX	**T**ransmit
TWTA	**T**ravelling **W**ave **T**ube **A**mplifier
UHDTV	**U**ltra **H**igh **D**evinition **T**ele **V**ision
VCO	**V**oltage **c**ontrolled **O**scillator
VCXO	**V**oltage **c**ontrolled **C**rystal **O**scillator
VGA	**V**ariable **G**ain **A**mplifier
VNA	**V**ector **N**etwork **A**nalyzer
VoD	**V**ideo **o**n **D**emand
VSAT	**V**ery **S**mall **A**perture **T**erminal
VSWR	**V**oltage **S**tanding **W**ave **R**atio

List of Symbols and Nomenclature

a, c	lattice constant	$\mathring{A}$
α	roll-off factor	
α_c	conductive attenuation constant	dB/cm
α_d	dielectric attenuation constant	dB/cm
α_i	forward travelling wave quantity	Np
α_r	radiated attenuation constant	dB/cm
α_t	total attenuation constant	dB/cm
Att_{atm}	atmospheric attenuation	dB
Att_{mis}	mispointing attenuation	dB
Att_{rain}	rain attenuation	dB
Att_{phys}	sum of physical link attenuation	dB
B	bandwidth	Hz
β_e	even mode image impedance	Ω
β_o	odd mode image impedance	Ω
β_i	reflected travelling wave quantity	Np
C	carrier power	dBm
C_{ds}	intrinsic output capacitance	F
C_{gd}	intrinsic feedback capacitance	F
C_{gs}	intrinsic input capacitance	F
C_{DS}	device output capacitance	F
C_{GD}	device feedback capacitance	F
C_{GS}	device input capacitance	F
C/N	Carrier to Noise distance	dB
C/N (th)	Carrier to thermal Noise distance	dB
C/(N+I)	Carrier to Noise distance including intermodulation Noise	dB
δ	skin-depth	μm
D_{die}	distance between pad centre to edge of die	μm
D_{gap}	distance between die and substrate	μm
D_{pad}	distance between gap and pad on substrate	μm
D_{total}	total distance pad to pad	μm
E_b	energy per bit	J
E_s	energy per symbol	J
E_B	break down field	V/cm
E_G	bandgap	eV
ε_r	dielectric constant	
ε_{re}	effective dielectric constant	
η	efficiency	%
η_c	combiner efficiency	%
f	frequency	Hz
f_0	fundamental centre frequency	Hz
$n \cdot f_0$	$n^{t}h$ harmonic centre frequency	Hz
f_{KNEE}	knee frequency (k $\geq$ 1)	Hz
f_{T}	transit frequency	Hz
f_{MAX}	maximum oscillation frequency	Hz
F	in band frequency range	Hz
F_{up}	upper in band frequency range	Hz
F_{low}	lower in band frequency range	Hz
F_{ext}	extended in band frequency range	Hz
Γ	reflection coefficient	
Γ_{in}	input reflection coefficient of DUT	
Γ_{output}	output reflection coefficient of DUT	
gm	transconductance	S

gm_n	nth derivative of transconductance	S
gd	conductance	S
$G_{\text{A,TX}}$	antenna gain TX	dBi
$G_{\text{A,RX}}$	antenna gain RX	dBi
G_{SS}	small-signal gain	dB
G/T	Gain to Noise Temperature	dB/K
h	height of substrate	μm
I_0	additive noise	
I_{d}	drain current	A
$i_{D,f0}$	fundamental output current	A
$i_{D,IMD3}$	3rd intermodulation products output current	A
I_{dc}	direct current	A
I_{DS}	drain-source current	A
$I_{\text{D,max}}$	maximum drain-source current	A
$I_{\text{D,sat}}$	saturated drain-source current	A
I_{DQ}	quiescent current	A
λ_0	free space wavelength	m
L_{bond}	bond inductance	H
L_{G}	parasitic drain inductance	H
l_{g}	gate length	μm
L_{G}	parasitic gate inductance	H
L_{pad}	pad inductance	H
L_{space}	free-space attenuation	dB
L_{S}	parasitic source inductance	H
μ	electron mobility	cm^2/Vs
N	thermal noise power	W
N_0	equivalent thermal noise power	
N_f	number of fingers	
N_{ft}	total number of fingers	
$\left[\text{PAE}_{f_1}\right]$	PAE contour depending on f_1, Z_L	%
$\left[\text{PAE}_{F}\right]$	PAE contour depending on F, Z_L	%
$P_{\text{diss,max}}$	max. dissipated power	W
P_{dc}	dc power consumption	W
P_{in}	input power	dBm
$P_{\text{in,1dB}}$	input 1 dB compression point	dBm
$P_{\text{in,avg}}$	average input power	dBm
$P_{\text{in,pk}}$	peak input power	dBm
$P_{\text{in, unc}}$	mismatch related measurement uncertainty	dB
P_{out}	output power	W or dBm
$P_{\text{out,1dB}}$	output 1 dB compression point	W or dBm
$P_{\text{out,avg}}$	average output power	W or dBm
$P_{\text{out,pk}}$	peak output power	W or dBm
$P_{\text{out,sat}}$	saturated output power	W or dBm
$P_{\text{out, unc}}$	mismatch related measurement uncertainty	dB
$\left[\text{P}_{\text{out, }f_1}\right]$	output power contour depending on f_1, Z_L	dBm
$\left[\text{P}_{\text{out, }F}\right]$	output power contour depending on F, Z_L	dBm
Φ	electrical length of transmission line	$^\circ$
PN	single side-band phase-noise	dBc/Hz
Q	quality factor	
Q_c	conductive quality factor (MS)	
Q_C	Charge	eV
Q_d	dielectric quality factor (MS)	
Q_r	radiation quality factor (MS)	
Q_t	total quality factor (MS)	
$R_{\Delta \text{ max, JC}}$	max. temperature difference junction to case	K/W
Ra	Roughness	μm
R_c	code rate	
R_{gs}	Schottky gate source resistance	Ω
R_{gd}	Schottky gate drain resistance	Ω
R_G	ohmic gate resistance	Ω
R_D	ohmic drain resistance	Ω
R_{ds}	drain source channel resistance	Ω
R_{on}	on resistance	Ω

R_S	sheet resistance (MS) / ohmic source resistance	Ω
R_{TH}	thermal conductivity	W/mK
R_m	modulation rate	Bd or S/s
ρ	electrical resistivity	Ω/m
$\begin{bmatrix} S_{tot} \end{bmatrix}$	measured S-Parameter Matrix	
$\begin{bmatrix} T_{tot} \end{bmatrix}$	measured T-Parameter Matrix	
t	thickness of metallisation	μm
$\tan \delta$	loss angle	
T	Temperature	K
$T_{A,RX}$	antenna noise temperature	K
T_R	effective noise temperature	K
T_{RX}	noise temperature of receiver	K
Θ	conduction angle	$^\circ$
$v_{sat,n}$	electron saturation velocity	cm/s
V_{cc}	common collector voltage	V
$V_{gs,trap}$	gate source voltage traps gate-lag	V
V_{GS}	static gate source voltage	V
$V_{ds,trap}$	drain source voltage traps drain-lag	V
V_{DS}	static drain source voltage	V
V_{FIX}	fix supply voltage	V
V_{knee}	knee voltage	V
V_{MOD}	modulated supply voltage	V
$V_{p\text{-off}}$	pinch off voltage	V
V_{TH}	threshold voltage	V
ω	angular frequency	rad
w	width of MS line	μm
W	gate width	mm
W_t	total gate width	mm
Z_0	characteristic impedance	Ω
$Z_{0,e}$	characteristic even-mode impedance of MS	Ω
$Z_{0,en}$	characteristic even-mode impedance of coupled MS	Ω
$Z_{0,o}$	characteristic odd-mode impedance of MS	Ω
$Z_{0,on}$	characteristic odd-mode impedance of coupled MS	Ω
$Z_{L,opt}$	optimum load impedance	Ω
$Z_{S,opt}$	optimum input impedance	Ω
Z_{TL}	characteristic impedance of transmission line	Ω

1 Introduction

Motivation and Objectives

In the early 1930s space researchers found a circular orbit above the equator following the earth's rotation. Within this ≈ 35786 km distance to the ground, objects seem to be motionless above ground, hence the name Geosynchronous Earth Orbit (GEO). A signal directed to this position may be reflected and directed back to earth, achieving a huge coverage on earth, as C. Clarke stated in 1945 [Kra84]. Due to the high distance to the ground, signals directed to this orbit are attenuated by the free-space loss. It is for this very reason why a signal has to be amplified and extraterrestrially relayed within a satellite [Cla45]. This relaying was first carried out by Syncom3, a GEO-satellite in 1964. Its aim was to broadcast television coverage across the Pacific for the Olympic games.

Nowadays, satellite services are widely used for broadcasting as well as time-sensitive and critical communication. Apart from *new space* satellite constellations in the low earth orbit (LEO), traditional *Ku*-band satellite communication (SatCom) in the geostationary orbit (GEO) remains interesting. The very small aperture terminals (VSATs) are a particularly growing market due to the increasing number of satellite launches and resulting reduced capacity costs. With the usage of these VSATs, it is possible to provide network or internet connection to remote regions. Nevertheless, VSATs are limited to a certain equivalent isotropically radiated power (EIRP) either in terms of the antenna gain or the output power of the block up-converter (BUC). By increasing the antenna gain, which comes along with increasing the size of a dish or planar antenna, the VSAT gets bulky and impractical [Mar03]. Increasing the power of the BUC normally leads to a very heavy housing with a higher power consumption and a rapid growth of costs.

GaN-HEMT technology can play a major role in
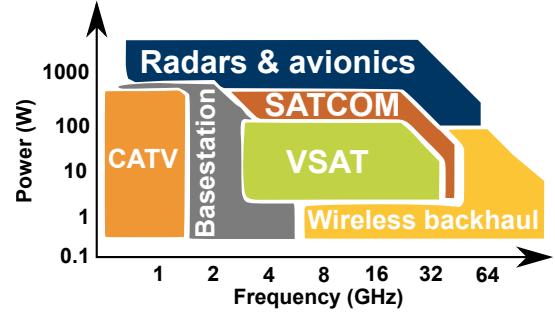
FIGURE 1.1: Available market for GaN related products.

lowering the costs of BUCs within VSAT, building a bridge between low power GaAs p-HEMT devices and high power travelling wave tube amplifiers (TWTA). The available market for GaN related products shown in Fig. 1.1 clearly depicts the VSAT as a major part in the SatCom market [Dev16]. However, the SatCom market can serve as a technological bridge between the already focussed mobile communication (Basestation) market in the lower frequency range and the technically sophisticated wireless backhaul market.

Within the GEO satellite market the *Ku*-band frequency range is becoming more and more attractive for VSAT applications. It can take advantage of low capacity costs due to an increasing number of transponders. In comparison to *Ka*-band or even *V*-band applications it benefits from a moderate rain-margin.

Research Gap

With the upcoming device technology of GaN-HEMT, a significant amount of effort was put into developing power amplifiers for the mobile communication market [Pen+12]. The trend of manufacturing GaN-HEMT on SiC and the advantages considering the thermal conditions as well as the lowered parasitics has led to great achievements

in efficiency enhanced power amplifiers in the mobile communication market. This is particularly the case with the popular 400 nm GaN-HEMT device technology, nowadays manufactured by several foundries, boosting power amplifiers to higher efficiencies in their saturation as well as their back-off operation. Nevertheless, the technologies are limited to a certain usage of up to $\approx 6\,$GHz due to their parasitics.

Newer manufacturing technologies like 250 nm (quarter micron) further increase the usable frequency range with transit frequencies of up to 40 GHz. However, not only is the usable frequency limited by the transistor's intrinsic parasitics but the mounting and bonding of the transistor to a matching circuit are a hindrance as well. To accommodate the demand towards higher frequencies there are three common approaches within research:

Firstly: The tolerances can be prevented by designing monolithic microwave integrated circuits (MMIC) with the matching circuits directly realised on the GaN/SiC substrates. This way, low parasitic interconnections between the transistor cells and its matching can be realised. However, the development of a MMIC is extremely expensive due to the costs of masks for the lithographic manufacturing steps. Furthermore, the losses of the SiC carrier substrate are a dominant part of the MMIC losses, as can be seen in Sec. 2.1. Nevertheless, power levels up to $P_{out} \approx 25\,$W are realised by the usage of 250 nm GaN-HEMT technology [Kan+14], [Creb].

Secondly: With an increase in output power the amplifiers are realised with high dielectric matching circuits, mounting the bare-die in between [Kaz+11], [Ima+14]. These microwave integrated circuits (MIC) lower the costs of a process run down to the bare-die size. Thanks to this MIC techniques power levels up to $P_{out} \approx 80\,$W were obtained. While comparing the device sizes of this second approach (MIC) to the first (MMIC), one will recognize that the total gate-width which is necessary for achieving an equal output power level, is far higher for a MIC compared to a MMIC.

This can be explained by the higher losses of the high dielectric matching circuits resulting in a lower efficiency (Sec. 2.1).

Thirdly: The mounting/assembling tolerances, and therefore the manufacturing tolerances, can be reduced based on flip-chip mounting technologies. This method eases an integration into hybrid substrate environments. However, packaging always significantly reduces the performance of the devices. The thermal connection between the device and a sink is extremely reduced by the package. Furthermore, the package reduces the upper frequency limit of the device due to parasitic package capacitances. Nowadays, only low-power devices are matched in the X-band with power levels up to $P_{out} \approx 5\,$W [Pav+15].

Approach

Within this thesis high power amplifiers have been developed that rely on a hybrid matching approach (MIC). Commercially available bare-dies were used with far less expense compared to MMICs. With an increased size of the bare-die the optimum impedances of the devices lowers. Special matching circuit techniques have therefore been developed which are capable of providing low impedance levels to the bare-die while reducing the transformation losses, when compared to the high k substrates described in the **second** approach.

A key-component of these matching circuits is a Bus Bar, first described by Marsh, for use with MMIC technologies [Mar+99]. Within this present work, the technique is enhanced by the use of multiple parallel microstrip (MS) lines for an even-mode propagation, and applied within a MIC design. A matching network with optimal load impedances less than $1\,\Omega$ is achieved by these parallelization (MS) lines.

All mounting and fabrication related parasitics, as well as tolerances, were analysed through the use of a 3-D EM-simulation. With regards to these constraints, the theoretical bandwidth limitations
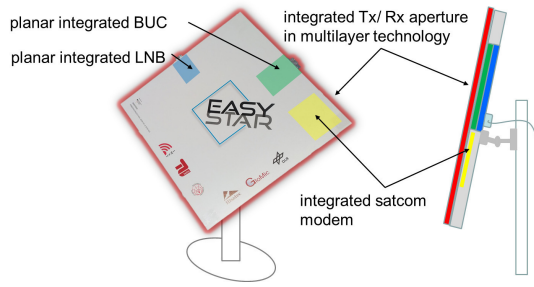
FIGURE 1.2: View of the realised low-profile *Ku*-band VSAT called EASYSTAR.

of the bare-dies have been analysed in detail by the techniques of Bode and Fano [Fan50]. These ideal matching limits are proven by the usage of Load-Pull simulations. This work enhances the classical Load-Pull techniques to a definition of Multi Frequency Load Pull Contours (MuFloC). Furthermore, the manufacturing as well as device constraints were taken into account for the design of matching circuits.

As an outcome of this applied technique, power levels of up to $P_{out} = 70$ W were achieved for three different designs in the *Ku*-band.

Furthermore, these MICs have been implemented into a hybrid planar BUC taking advantage of a low power consumption. The implementation of all parts of the BUC, namely the high power MICs, the frequency generation as well as the dc/dc conversion into one housing, eases the handling for a user. Despite the lower power consumption of the BUC, a GaN-HEMT typical soft compression was cancelled by the usage of a change in the biasing as well as an active RF-predistortion in real-time.

Finally, the BUC is connected to a planar TX-RX aperture shown in Fig. 1.2 building a lightweight thin VSAT. The VSAT is an outcome of the project ISISTAR which combines all the components of a VSAT, namely antenna, LNB, BUC and modem, to one system. During SatCom link measurements, the performance of the VSAT was evaluated.

Thesis Structure

This thesis is structured as follows. Each section is divided into subsections which are introduced in detail at the beginning of the section. These subsections are summarized at the end, while a discussion compares the developments of each section with state of the art results.

Starting with the Fundamentals (Sec. 2), a basic insight is given to all themes that are related to microwave technology for the use in SatCom.

The main Sec. 3 focuses on the development of MIC PAs where three designs are compared and evaluated. At the end, the back-off efficiency of the designs is enhanced, which finally leads to a discussion.

Sec. 4 describes the design and measurements of a block-up-converter.

Within, Sec. 5 all individually developed components are proven towards their combined functionality in a satellite link.

Finally, the achievements are summed up in the conclusion in Sec. 6.

2 Fundamentals

This chapter will provide insight into the fundamentals which have been applied to this work. Each subsection will provide a basic understanding of general knowledge related to power amplifier design with its application on the devices and frequencies used in the circuits developed later on. For a more detailed understanding, references to the given literature are provided. In order to reduce the number of fundamentals required, there are a number of descriptions located in the Appendix of this work. The definition of commonly known equations is mainly given for nomenclature purposes like for S-Parameters in Appx. A.1.

To determine the limitations of hybrid matching circuits the substrate parasitics are introduced in Sec. 2.1. In relation to these calculations, the necessary equations are given in Appx. A.2.

Fundamental aspects of the semiconductors and especially GaN-HEMTs used in this work are given in Sec. 2.2.

Sec. 2.3 introduces the Power Amplifier Fundamentals necessary for an understanding of the work. Amplifier related nomenclature is given in Appx. A.3. An introduction to simulation techniques is given in Appx. A.4 for circuit as well as electromagnetic-simulation.

An introduction to the commonly used SatCom signals and the necessary requirements for a system design are given in Sec. 2.4.

Sec. 2.5 describes a basic understanding of HF measurement techniques used within this thesis. The uncertainties related to the small and large signal measurements used in this work are explained in Appx. A.5.

2.1   Substrates

Substrates are key-components for all HF circuits. Their main application is for routing signals between active devices. By increasing the frequency of the signals, the parasitics of these interconnections, namely their equivalent capacitance and inductance, increase as well. It can therefore no longer be assumed that these connections are ideal.

The common line-type for HF transmissions is the microstrip (MS) line with its quasi-TEM behaviour. For designing MS transmission-lines several parameters need to be determined. The characteristic impedance Z_0 can be calculated based on the equations of Wheeler [Whe78]. They are related to the permittivity of the substrate ε_r and to its effective permittivity ε_{re}. Additional dispersion effects are described by Kobayashi [Kob88]. Hammerstad et. al. defined three factors that lead to losses within a HF line [Ham+80]:

1. The losses related to the conductivity of the metallisation are called α_c. These metal losses are in proportion to the square root of frequency and different for various line-types due to the different sheet resistances in MS, coax or wave-guide. In addition, the skin effect in combination with the roughness Ra of the metallisation, increases a_c.

2. α_d considers the dielectric losses within the substrate. Additional dispersion can further increase this loss factor. It is in proportion to frequency and constant over various line-types.

3. The radiation losses α_r increase with frequency and are mainly relevant to open-ended structures.

TABLE 2.1: Properties of dielectric materials at 10 GHz

	ε_r	$\tan \delta$	Ra (μm)	R_{TH} (W/mK)	h (μm)
Al_2O_3	9.9	0.0001	0.1	37	127
4H-SiC[1]	9.66	0.003	0.1	350	100
DLI CD	38	0.004	≤5	1.59	254
RO4003c	3.38	0.0027	5[2]	0.71	220
FR4	4.7	0.014[3]	2-6	0.25	254

[1] 4H-SiC is a semiconductor
[2] Lo Profile
[3] at 10 MHz.

TABLE 2.2: Properties of conductor materials

	ρ (Ω m)	R_{TH} (W/mK)	t (μm)	δ^1 (μm)
Cu	1.67e-8	393	35	0.54
CuMoCu	2.4e-8	295	1500	0.65
Au	2.4e-8	297	10	0.65
Au-20% Sn	1.6e-7	57	20	1.67
Ti	5.5e-7	22	0.06	3.01
Pd	1.06e-7	70	0.2	1.35
NiCr	1.1e-6	74	0.06	2.18

[1] skin depth for 14 GHz.

Dielectric Materials

A preliminary analysis of the substrates used in this work should introduce parasitics and losses within the *Ku*-band. Different types of dielectric materials and their properties are shown in Tab. 2.1 with the substrate height h used in this work.

FR4 is a representative for a product in the low frequency consumer market, whereas Al_2O_3 are ceramic or RO4003c are hydrocarbon-glass based HF substrates. 4H-SiC is described because it is the common choice for all GaN-HEMT related MMICs that are grown on SiC substrates. Within this table there is a representative of a high k substrate (DLI CD) with a $\varepsilon_r = 38$ which is used in single layer capacitors or for a hybrid pre-matching next to a bare-die.

As a first comparison related to the suitability in high frequency applications, their $\tan \delta$, which represents the dielectric losses, needs to be considered. Additionally, the selection of the substrate is always related to the impedance-levels that are needed and the losses that can be tolerated. For example, to match extremely low ohmic impedances a high permittivity substrate can be helpful, whereas a low height of the substrates h always corresponds to a small width w of the MS-line and as a result a high sheet resistance R_S. Furthermore, the roughness of the dielectric materials (Al_2O_3, DLI CD) is a consequence of the manufacturing process. The ceramic based materials can be polished before the metallisation gets sputtered. Hence the Ra of the dielectric material is directly related to the metal sputtered on top of it.

For hydrocarbon-glass or PTFE based substrates the Ra is related to the copper foil that is applied to the substrate. Within this work, only rolled instead of electro-deposited copper is used which is suitable for HF-application. For the RO4003c substrate, chosen in here, a special LoPro copper foil of Rogers is used that should further lower the Ra. These foils have a thickness of 35 μm and its conductivity can be observed from Tab. 2.2.

Conductor Materials

Due to manufacturing limitations on top of a ceramic based dielectric, some adhesive layers need to be applied underneath the real conductor. For the used Al_2O_3, this metallisation stack contains different layers (NiCr, Ti, Pd, Au) that are necessary for realising NiCr resistors on the substrate (Fig. 2.1 (a)). Different conductivities and thicknesses of these materials lead to a layer dependent analysis of skin depth in the metallisation stack, shown on the right of Fig. 2.1 (c). This way it can be determined that the thickness of the additional layers is low compared to Au. However, the conductivity (σ) of these additional layers is low, which induces the skin depth to a fraction of the wavelength. Equation 2.1 shows the accurate calculation of the skin depth, where the second part of the formula (in rectangle brackets) can be neglected for frequencies below $\omega \ll \frac{1}{\rho \varepsilon_r}$.

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \left[\sqrt{\sqrt{1 + (\rho\omega\varepsilon_r)^2} + \rho\omega\varepsilon_r} \right] \qquad (2.1)$$

The skin depth δ is calculated for each conductor at 14 GHz and given in Tab. 2.2. It can be calculated
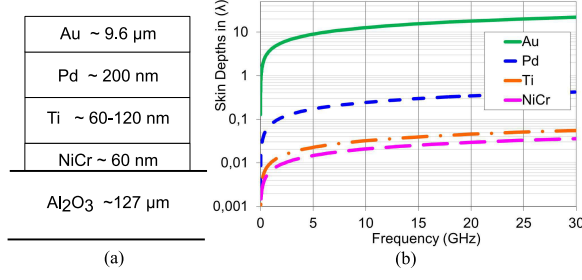
FIGURE 2.1: Layer stack of the Al_2O_3 substrate (a) with the equivalent skin depths per metal layer (c).

per layer depending on the layer thickness from Fig. 2.1 (a) and the resistivity from Tab. 2.2. With these values shown in Fig. 2.1 (c) an equivalent conductivity of the composite layer stack can be calculated to $\sigma_{comp} = 1.97e6\,S/m$ at 14 GHz. This lowered conductivity is later lowered again by taking the roughness of the dielectrics into account using a Hammerstad approximation. The described approximation is especially useful for easing a multilayer field-simulation, which is incapable of solving a thin thickness and rough width of the mesh simultaneous.

Loss Analysis

Based on the dielectric as well as metallic parameters, the losses of a MS-line can be calculated, as described in detail in [Bah03, 429 ff.] and Appx. A.2. The given parameters, namely the height of the substrate h and the thickness of the conductor t lead to a calculated width w of the MS-line to satisfy $Z_{TL} = 50\,\Omega$. Then the α_d dielectric (Fig. 2.2(a)) α_c conductive (Fig. 2.2(b)) as well as the α_t total losses (Fig. 2.2(c)) for a MS-line over various frequencies can be calculated. Within these total losses the dispersive character of the dielectric material, the roughness and therefore its lowered sheet resistance is taken into account.

The α_d dielectric losses are low for the dielectrics with the lowest $\tan\delta$ that is the Al_2O_3 (Fig. 2.2(a)). The dielectric losses for FR4 are in the order of 10^{-2} (dB/cm) higher compared to Al_2O_3. By considering the α_c conductive losses, one must realise that the FR4 metallisation represents the lowest losses due to its high width w of the MS-line (Fig. 2.2(b))

(a) α_d

(b) α_c
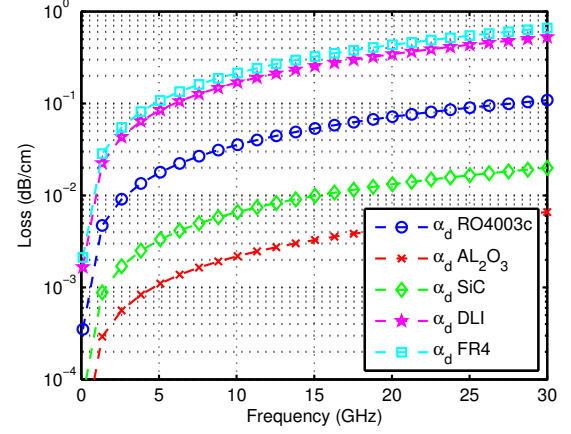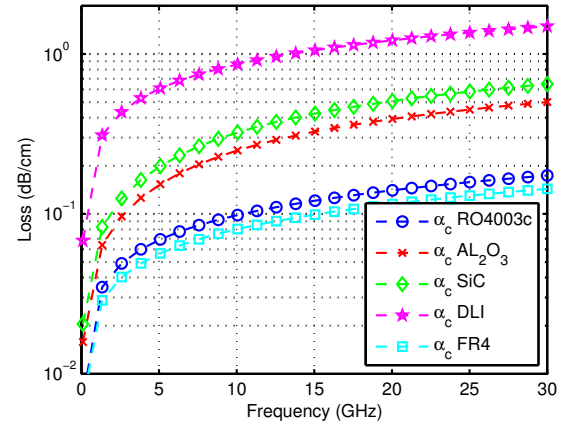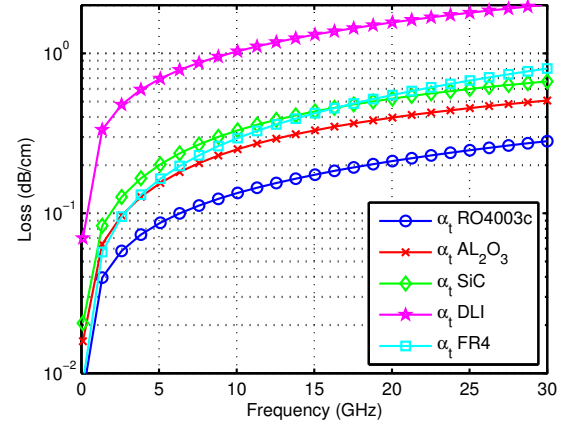
(c) α_t

FIGURE 2.2: Substrate losses divided into (a) the α_d dielectric, (b) α_c conductive as well as (c) the α_t total losses for a MS-line (50 Ω) over various frequencies.

related to the low Ra. Hence the smallest w of all substrates being the one of the DLI high ε_r substrate with its moderate Ra, resulting in conductive losses in the order of 10^{-1} (dB/cm) higher than the FR4 metallisation. The α_t total losses
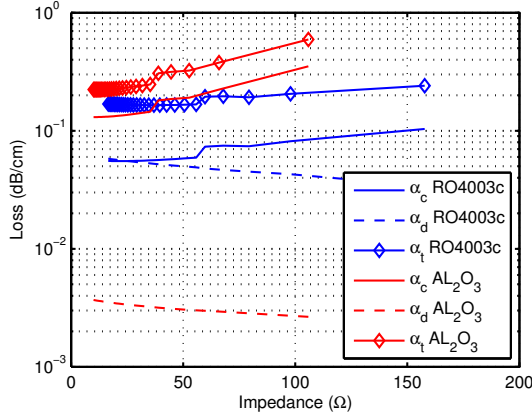
FIGURE 2.3: Conductive α_c, dielectric α_d as well as the total losses α_t for a MS line with various impedances for 14 GHz.

are the sum of both. The DLI high ε_r substrate clearly produces the highest losses in the order of 1.5 dB/cm at 14 GHz (Fig. 2.2(c)). Furthermore, the high conductive losses for the FR4 as well as the SIC determines the total losses in the range of 0.4 dB/cm at 14 GHz. This analytical result indicates that the RO4003c is the best choice when it comes to losses related to the $Z_{TL} = 50\,\Omega$ line impedance with 0.2 dB/cm at 14 GHz.

By lowering the Z_{TL} the w increases and as a result the sheet-resistance of a MS-line decreases. This way the low impedance levels benefit from lowered conductive losses (α_c) as shown in (Fig. 2.3) for 14 GHz. Approximately half of the energy is dissipated in the conductor for a $Z_{TL} = 10\,\Omega$ line impedance compared to the $Z_{TL} = 50\,\Omega$ line impedance.

Quality Factor Analysis

An open-ended MS-line is a resonator with its quality factor Q summing up the losses related to it. The Q describes the ability of a combination (substrate and metallisation) to be used for a HF filter or matching applications. In addition to the already defined losses α_c, α_d the radiation plays a major role for open-ended structures and is defined as α_r.
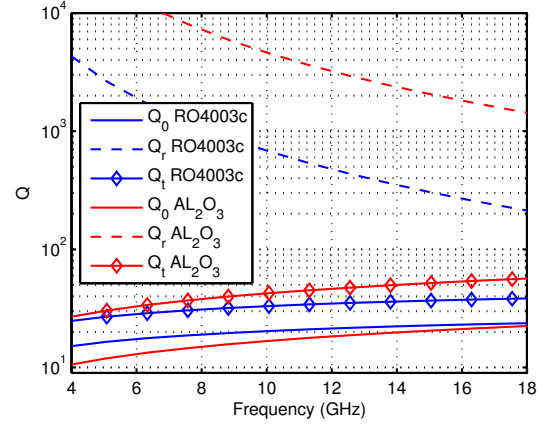
(a)
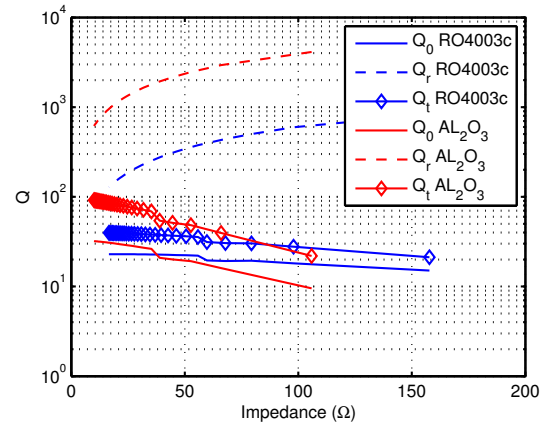
(b)

FIGURE 2.4: (a) shows the Q_r radiated, Q_0 conductive and dielectric as well as Q_t total quality factor for an open-ended $\lambda/4$ MS line (50 Ω) over various frequencies, and (b) various impedances for 14 GHz.

The relating quality factors [Bah03, 436 ff.] can be defined with:

$$\frac{1}{Q_0} = \frac{1}{Q_c} + \frac{1}{Q_d} = \frac{\lambda_0(\alpha_c + \alpha_d)}{\pi\sqrt{\varepsilon_{re}(f)}} \qquad (2.2)$$

$$\frac{1}{Q_t} = \frac{1}{Q_0} + \frac{1}{Q_r} \qquad (2.3)$$

The minor losses for an open-ended $\lambda/4$ MS line on the Al$_2$O$_3$ as well as the RO4003c substrates are clearly the α_r radiation losses, which is why the related quality factor Q_r is high, decreasing towards higher frequencies (Fig. 2.4(a)). Furthermore, the line width w of the RO4003c substrate is higher, resulting in a lowered Q_r compared to the Al$_2$O$_3$. Only the Q_t determines the unloaded Q of the resonator and identifies the Al$_2$O$_3$ substrate as the better choice for 14 GHz applications (Q_t=45).

Although both substrates only represent moderate quality factors the analysis can be extended by lowering the Z_{TL} line impedance as shown in (Fig. 2.4(b)). The Al_2O_3 substrate shows an increased Q_t of up to 100. Paired with its high manufacturing accuracy, it is the preferred choice for a realisation of matching and filter structures. The lowest losses were achieved by the RO4003c substrate, additional shielding would also improve the high radiation losses.

2.2 Semiconductors

Semiconductor materials

Semiconductor materials are the opposite of isolators. Inserting additional impurity atoms into the semiconductor lowers its specific resistance. Nowadays only extrinsic semiconductors with IV valent atoms inserted in an n-channel are used for HF applications. The most significant properties of semiconductors are shown in Tab. 2.3. The electron mobility μ especially limits the upper transit frequency, whereas a wide bandgap E_G is suitable for high power applications. The breakdown-field E_B limits the maximum operation field in the semiconductor. A combination of the electron mobility μ and the breakdown-field E_B, called the saturation velocity ($v_{sat,n}=\mu \cdot \vec{E}$) limits the semiconductor towards its high power and high frequency applications. Thus GaN clearly outperforms GaAs, enabling far higher current densities.

The compound semiconductors SiC, GaAs and GaN are nowadays grown by a molecular beam epitaxy (MBE) on a foreign substrate [Aae+11, p. 23]. The foreign substrate needs to represent as little lattice mismatch to the compound semiconductor as possible while its lattice constant is described via a, c[1]. The combination of GaN on Si compromises between costs and power, whereas GaN on SiC is a great fit for all high-power applications. The thermal conductivity R_{TH} of SiC

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[1]The hexagonal Wurtzide crystal structure needs to be represented by the lattice constant a and c.

TABLE 2.3: Properties of (compound) semiconductor materials

	Si	4H-SiC	GaAs	GaN
bandgap E_G (eV)	1.12	3.2	1.42	3.4
breakdownfield E_B (10^6 V/cm)	0.3	3.5	0.4	2
mobility μ (cm^2/Vs)	1300	260	5000	1500
sat. velocity $v_{sat,n}$ (10^7 cm/s)	1	2	0.72	2
th. conductivity R_{TH} (W/mK)	130	350	46	170
diel. const. ε_r	11.9	9.66	12.5	9.5
lattice const. a ($\AA$) c ($\AA$)	5.4 D[1] -	3.1 H[2] 10.1	5.6 C[3] -	3.2 H[2] 5.7

[1] Diamond [2] Wurtzide (hexagonal) [3] Zinc blende (cubic)

is nearly in the range of metal – hence why this foreign substrate is an almost perfect heat splay.

FET

Within a field-effect transistor (FET) a current flows along a semiconducting path described as the *channel*, connecting the electrodes called *drain* and *source*. The current along the channel is modulated via a biasing voltage at the *gate* electrode. The FET can be either driven by an insolated *gate* electrode (e.g. a *pn* junction) or a Schottky junction, where the last one represents a MesFET. In addition, FETs are separated by being operated in depletion (normally ON) or enhancement mode (normally OFF).

GaN-HEMT

A high-electron-mobility transistor (HEMT) operates like any other MesFET. However, within an HEMT there are at least two semiconductor layers with different bandgaps grown on each other, building the epilayers which represent a heterojunction.

Vertical Transistor

The vertical architecture of an HEMT consists of layers with different materials, chosen to build a channel in which the electrons are physically separated from their parent donors [Rob+01]. The free electrons provided by the *n*-type dopant are located in between an undoped space layer and the channel layer close to the heterojunction, building an almost two-dimensional section [Mar06]. This two-dimensional electron gas (2DEG) is located away from the lattice atoms, so it will not collude, lowering the impurity scattering and therefore giving the free electrons higher mobility. Less collusion within the channel decreases the noise figure of HEMTs compared to MesFETs.

The current flows, within the HEMT, from the ohmic contacts of the source to the ohmic contacts of the drain via the high mobility channel, as can be seen in the cross sectional view of Fig. 2.5 taken from [Pen+12]. This current is determined by the sheet electron concentration underneath the Schottky gate contact. The concentration can be modulated by the bias and in consequence the Schottky contact. The heterojunction underneath the gate represents a capacitor with its gate metal and 2DEG building the plates. In between, the spacer, donor, barrier and Cap layers form the dielectrics of this capacitor. The Barrier layer should isolate the channel from the gate and is typically made of AlN. The aluminium concentration controls the charge capacity of the channel. The resulting capacitance remains almost constant while changing the bias, as the dielectric separation is fixed by the thickness of these top epilayers. In conclusion, the current modulation in this HEMT is controlled by adding or removing charge Q_C of the 2DEG in response to the variations in voltage V at the Schottky contact using a simple capacitor equation $Q_C = C \cdot V$.

For high power applications the electrical field between the drain and the source is limited by the breakdown-field E_B. Nevertheless, the same electrical field is applied towards the gate through the epilayers which may lead to a gate breakdown. Consequently, the gate is located with a higher
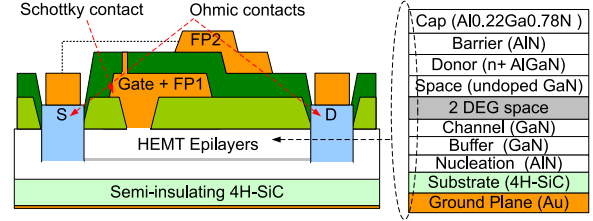
FIGURE 2.5: Cross sectional view of the GaN-HEMT with additional field plate technique.

offset to the drain than to the source, which further decreases the source resistance. The strongest electric field is located at the drain edge of the gate where the gate can provide free electrons to fill surface states. This enhancement of the gate behaves as a *virtual gate* which results in an extended depletion region and gate-source voltage variations (gate-lag) [Vet+01]. Furthermore, these field related states may be improved by a passivation layer (SiN) on top of the epilayers as well as a special design of the tee gate using field-plates (FP). They are designed to lower the field peaks towards the gate but, as a result, introduce a higher capacity, which lowers the f_{MAX} of the HEMT. To lower the effect of an increased gate capacity, a second field plate (FP2) can be connected to the source potential which is called double field plate technology. By introducing the second field plate, the drain-source capacity is increased, which is only a fraction of the gate capacity.

Underneath the channel, a buffer layer is added as a barrier to restrict the movement of the electrons. This is made of GaN doped with carbon or iron. Given the high electric fields between drain and source, the electrons moving in the 2DEG channel could be injected into the buffer. Hence the extension of the electric field from the channel towards the substrate, results in a leakage current called *traps* [Flo12, p. 20]. These injections represent extremely long trapping time constants, because these electrons are no longer part of the conduction for the HF signal. Moreover, the trapped electrons produce a negative charge which also depletes the 2DEG and in consequence reduces the channel current that finally results in a current collapse.

To reduce this trapping, an improved lattice matching is realised by a nucleation layer (AlN) that
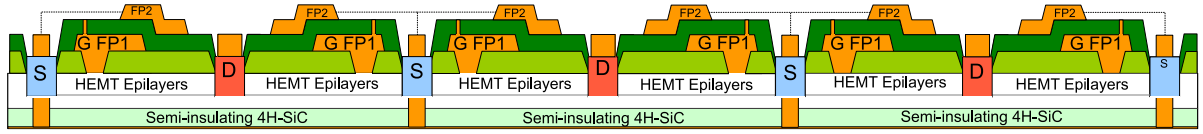
FIGURE 2.6: Cross sectional view of the N_f=6 gate finger GaN-HEMT of Wolfspeed (CGHV1J006D).

should reduce the piezoelectric field in between the buffer and the substrate. Trapping effects based on the buffer substrate are commonly known as *Drain lag* because they are mainly influencing the output conductance. In addition, these buffer traps can result in a *gate lag* which can be obtained as a delay between the start of a rising voltage slope at the gate and the current slope at the Drain. This extends the gate area by the virtual gate to an increased gate-Drain region leading to a decreased 2DEG density defined by an increase of the access resistance.

The semi-insulating substrate is used as mechanical and thermal support. A thickness of ≈ 4 mil is historically related to older GaAs processes. The different crystal lattice of the 4H-SiC to the GaN creates dislocations that lead to long time constant traps. As a result, both the buffer as well as the substrate technology used by the manufacturer determine the linearity of the GaN-HEMTs.

Horizontal Device

Among the vertical semiconductor structure already described, the device itself becomes horizontal with the use of multiple parallel fingers [2]. One gate finger refers to a single vertical structure, as shown in Fig. 2.5. The gate length l_g depends on the resolution of the manufacturing process and limits the f_{MAX} of the device (Fig. 2.7). With an increased width of the gate, the dc and RF current of the device increases until the width becomes a fraction of the wavelength, resulting in gate modulation effects. To further increase the output power of a GaN-HEMT, the vertical structure can be parallelized to N_f x the intrinsic GaN-HEMTs as shown in Fig. 2.6 and Fig. 2.7 with N_f=6 gate fingers. The

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[2]As an alternative, the vertical device can be scaled by the so-called fishbone layout which is typically not used in RF-design due to the necessary air-bridges.
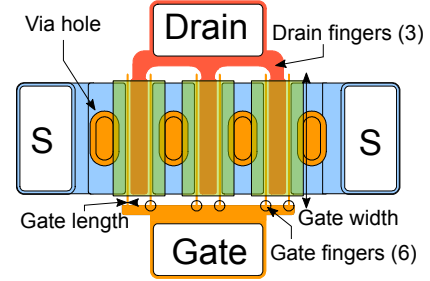
FIGURE 2.7: Top view of the 6 gate finger GaN-HEMT.

total gate width W_t represents the sum of all individual gate finger widths. For example, the gate width of one finger shown in Fig. 2.7 is 200 μm, resulting in a total gate width of W_t=1.2 mm. In total, any device has at least two gate fingers feeding one drain finger.

The gate periphery represents the total size of the device. The device's parameter can be scaled with the gate periphery as shown in Tab. 2.4. The gate fingers are interconnected to the pad via the gate bus bar. The drain bus bar serves as an interconnection for the drain fingers, while the interconnection length needs to stay a fraction of the wavelength, like with the gate width. Fig. 2.7 also visualizes individual source vias (ISVs) which provide very low inductance source interconnection to the backside of the device. A special oval shape of the via reduces the necessary source contact pad size and therefore decreases the size of one intrinsic HEMT. In addition, ISVs are used to improve the heat spray of the device.

GaN-HEMT model

The described vertical structure of a GaN-HEMT can be analysed by the manufacturers based on technology CAD tools (T-CAD[3]) where the field densities can be obtained and improved. Design aspects like the gate capacitance can be optimized

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[3]Technology CAD Tools, e.g. ISE^{TM}or Silvaco^{TM}
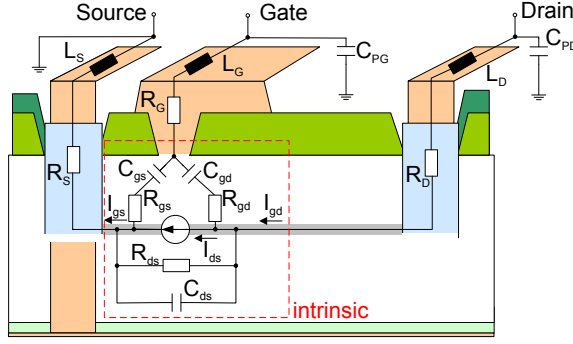
FIGURE 2.8: Cross sectional view of the GaN-HEMT with equivalent circuit elements.

through the structure of the gate (e.g. tee-gate with field plate). Furthermore, charge currents and therefore channel resistances can be calculated. These models solve the non-linear partial differential equations (PDE) for the 2D vertical structure. They can be extended to, for example, the width of the gate to represent a horizontal device, resulting in physical based compact models based on time-consuming simulations. Nevertheless, the complexity of the models means they are not usable by circuit designers.

For this reason, compact models are used for the purpose of circuit design and are summed up in [Rud+11]. Within the following summary only a short description of one compact model extraction technique is given, described in [Gas12]:

Linear model extraction through S-parameters

The behaviour of a device is measured based on S-Parameters and extracted to a small-signal model as in [Kon86]. A small-signal equivalent circuit of a GaN-HEMT is shown in Fig. 2.8 and corresponds to the vertical structure of the device. First of all, the extrinsic components that represent pad or interconnection inductances (L_G, L_S, L_D), as well as series resistance of the ohmic contacts (R_G, R_S, R_D) or pad capacitances (C_{PG}, C_{PD}), are determined because they are independent to biasing conditions. Subsequently, the S-Parameter measurements can be de-embedded to the intrinsic reference plane and transformed into Y-Parameter. Based on the given equations in [Aae+11, 207ff.]

the drain current (I_d), conductance (gd) as well as transconductance (gm) are determined depending on the parasitic capacitances (C_{gs}, C_{gd}, C_{ds}), the Schottky resistances (R_{gs}, R_{gd}) and the channel resistance (R_{ds}). The intrinsic components represent the voltage controlled current source of the channel and all intrinsic elements are optimized to fit to the measurements. Nevertheless, this approximation only represents valuable data for the device's state of the initial S-Parameter measurements.

Non-linear model extraction with pulsed IV

The model needs to be extended by large-signal measurements. Pulses are the favoured method for characterising a power device while maintaining a constant thermal state. Based on short pulses, the thermal resistance of a device can be determined while avoiding self-heating. During longer pulses a current decrease occurs in the device which can be used to determine its thermal capacitance. Both influence the equivalent transistor junction temperature (T) and result in a non-linear current ($I_{ds} = f(V_{ds}, V_{gs}, T)$) a non-linear conductance as well as transconductance ($\partial gs = f(V_{gs}, T)$, $\partial gd = f(V_{gd}, T)$). The thermal analysis can be extended by IR-thermography of the device's top side in comparison to its T-CAD model.

Non-linear model extraction with pulsed IV/RF

The parasitic capacitances of a GaN-HEMT depend on its terminal voltages, which itself depends on the timing as well as the thermal state of the device. Moreover, a non-linear gate voltage behaviour of the GaN-HEMT affects the feedback capacitance, which is why it needs to be modelled for synchronised voltage currents and RF states ($C_{gs} = f(V_{gs})$, $C_{gd} = f(V_{gd})$). In contrast to common lateral FETs, the dependency of C_{ds} to V_{ds} is negligible for the on-state. Various pulse-widths are used to represent various time constants of the trapping effects. A separation between surface trapping (*gate-lag*) and buffer trapping (*drain-lag*) can be done by a series of measurements while influencing

TABLE 2.4: Parameters of GaN-HEMT scaling

parameter	No. finger N_f	gate width W
g_m	N_f	W
C_{GS}, C_{DS}	N_f	W
f_{MAX}	-	$1/W$
f_{T}	-	-
$Z_{\text{L,opt}}$	$1/N_f$	$1/W$
$R_{\text{D}}, R_{\text{S}}$	$1/N_f$	
R_{G}	$R_{\text{G}}(\frac{W_t}{W})(\frac{N_{ft}}{N_f})^2$	

$V_{gs,trap}$ or $V_{ds,trap}$ resulting in a non-linear current ($I_{ds} = f(V_{ds,trap}, V_{gs,trap}, T)$).

Load-Pull for Model Validation

Load-Pull measurements of the device can be used to validate its model beyond the ideal $50\,\Omega$ loads. Nowadays, active Load-Pull measurements are applied during pulsed power conditions with vector receivers. Therefore, the already obtained compact model can be used to determine the optimal input impedance of the DUT, always resulting in true power gain conditions. This is important because of the non-linear input impedance with dependency to the input power level. Nevertheless, Load-Pull measurements are limited to frequency or the device-size, as described in detail in Sec. 2.5. Consequently, a model validation based on Load-Pull measurements can only be applied towards a certain size of the device.

Scaling

For power devices that exceed the number of fingers by a huge parallelisation, modelling is done by scaling smaller devices [Aae+11, 203ff.]. To be more precise: – a compact behavioural model, based on the described techniques, needs to be up-scaled to the real device size with the gate periphery. All parasitic elements of one transistor are in parallel, resulting in the total parasitic elements. Tab. 2.4 sums up the scaling rules for direct or indirect dependencies of the gate width or the number of fingers.

GaN-HEMT losses

The *conduction losses* of the GaN-HEMT are mainly determined by the R_{on} characteristics. In addition to these frequency independent losses, several losses need to be summed up to represent the so-called *switching losses*. First, the device parameters influence the high frequency switching ability that are the gate length (l_g) and the channel mobility (μ), where the last one depends on the temperature. That said, not only the device parameters but also the gate drive current, the stray inductances and especially the non-linear device parasitic capacitances leads to a high frequency limitation. With an increased frequency the gain decreases up to the frequency where unilateral stability is achieved (f_{KNEE}).

To further improve the efficiency of devices one has to eliminate the surface traps (either in passivation or epitaxial), the bulk traps (growth condition tuning) and of course decrease possible leakage (low dislocation density). With an increased gate-periphery the PAE decreases by:

- the voltage drop along the gate width

- phase differences between the gate fingers

- thermal coupling between devices increases its temperature which results in a negative slope of dc-characteristics

2.3 Power Amplifier Theory

For the application of solid state power amplifiers (SSPA) in the microwave field only n-channel devices are used, based on their higher electron mobility. All used FET devices of this work are biased in a common-source topology taking advantage of the high power ability. Within these transconductance amplifiers the input voltage modulates the amount of current flowing through the FET. For a direct current operation the output current (I_{dc}) can be set in relation to the input bias (V_{GS}) by the knowledge of the transconductance (mutual gain)

gm_{dc}:

$$I_{dc} = gm_{dc} \cdot V_{GS} \qquad gm_{dc} = \frac{\partial I_{dc}}{\partial V_{GS}}\bigg|_{V_{DS}=const.}$$
(2.4)

For an alternating current the same applies for the dependence of the output current i_D to the input voltage v_{GS} for a fixed drain voltage.

$$gm = \frac{\partial i_D}{\partial v_{GS}}\bigg|_{V_{DS}=const.}$$
(2.5)

Amplifier Biasing Class

By using a commonly known **Class-A** amplifier, 100% of the input signal passes through the amplifier which continues to conduct. The amount of output current to the input voltage can be set in relation to the period of a sinusoidal input signal (0 - 360°). The conduction angle Θ is 360° while the output current is an exact representative of the input voltage. As a drawback, the amplifier needs to be biased to half the input voltage swing to remain conductive for the negative half of the sinusoidal signal. In conclusion, a permanent current occurs which limits the theoretical efficiency of the amplifier to $\eta = 50\%$.

By lowering the conduction angle the waveform of the output current is cut by its lower half in relation to the conduction angle ($\Theta < 360°$) and the efficiency increases. With $\Theta = 180°$ the amplifier is said to be in **Class-B** only conducting half of the applied signal. The range in between is defined as a **Class-AB** amplifier ($180° < \Theta < 360°$). By conducting less than half of the applied signal ($\Theta < 180°$) the amplifier is said to be working in **Class-C** mode.

In the literature, most of the definitions regarding these amplifier classes are related to its devices turn-on behaviour located at $\Theta = 180°$, whereas the ideal threshold voltage V_{TH} defines the beginning of the conducting region [Bow+07, 150 ff.]. V_{TH} is highly related to the V_{DS} (Eq. 2.5) and, in addition, to the saturation or the previous state of the device. Especially for the highly scaled GaN-HEMT transistor, the V_{TH} cannot be easily determined based on its extrinsic control voltage due to short-channel effects and therefore varies with temperature.

Nowadays, there is a huge variety of additional classes of operation that are worth mentioning in detail. Their intention is to reduce the overlap of the current and voltage-swing at the devices intrinsic current plane. In conclusion, the amount of dissipated power is reduced and the efficiency increases, which is shown in detail in [Cri06].

Small-Signal approximated Amplifiers

The non-linearity of the output current can, according to [Col+09, 358 ff.], be defined by a 3rd order power series of:

$$i_D = I_{dc} + gm \cdot v_{GS} + gm_2 \cdot v_{GS}^2 + gm_3 \cdot v_{GS}^3$$
(2.6)

with the small-signal definitions of the higher order partial derivatives:

$$gm_2 = \frac{\partial^2 i_D}{\partial v_{GS}^2}\bigg|_{V_{DS}=const.}$$
(2.7)

$$gm_3 = \frac{\partial^3 i_D}{\partial v_{GS}^3}\bigg|_{V_{DS}=const.}$$
(2.8)

Taking advantage of the addition theorem this equation can be changed to:

$$dc: \quad i_D = I_{dc}+ \tag{2.9}$$
$$f_0: \quad gm \cdot v_{GS} \cdot cos(\omega t)+ \tag{2.10}$$
$$2 \cdot f_0: \quad gm_2 \cdot v_{GS}^2 \cdot cos^2(\omega t)+ \tag{2.11}$$
$$3 \cdot f_0: \quad gm_3 \cdot v_{GS}^3 \cdot cos^3(\omega t) \tag{2.12}$$

The frequency dependency of the higher order derivatives can clearly be observed. According to this separation, Cabal et al. defines the beginning of the conduction ($\Theta = 180°$) by the zero of the third order derivative gm_3 (Eq. 2.8) [Cab+04]. This definition of cut-off voltage clarifies the uncertainty of the previously defined varying V_{TH} and can be obtained in Fig. 2.9 for a simulated GaN-HEMT.

By inserting a fundamental wave into this non-linear circuit a number of harmonics are generated (2 for this example). With an increased saturation of this amplifier, the compression increases and
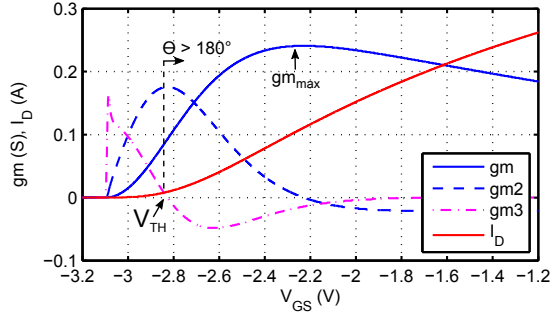
FIGURE 2.9: Simulated example of ac gm behaviour as a function of V_{GS} for a 250 nm GaN-HEMT (CGHV1J006D; $V_{DS} = 40$ V; 1 GHz).

therefore the amount as well as the power of the harmonics increases.

Large-Signal approximated Amplifiers

Nevertheless, this approach relies on a small-signal assumption of the gm which cannot sufficiently represent the large-signal (saturated) conditions of the gate of an GaN-HEMT. According to Pedro et al. the compression behaviour of the transistor cannot be modelled by the small-signal expansion of Eq. 2.6 because this memoryless assumption relies on an isolated FET [Ped+03, 340 ff.]. For an increasing high v_{GS} the non-linear boundary effects increase which is why a *self-biasing* effect occurs. The i_D is no longer only a function of the static V_{GS} (dc), but rather than the amount of the varying ac v_{GS} which is indirectly declared in P_{in}.

$$v_{in}(t) = V_{GS} + v_{GS}(t) \qquad (2.13)$$

The Taylor series expansion can be increased to a higher order:

$$i_D[v_{in}(t)] = I_{dc} + gm \cdot v_{GS}(t) + gm_2 \cdot v_{GS}(t)^2$$
$$+ gm_3 \cdot v_{GS}(t)^3 + gm_4 \cdot v_{GS}(t)^4 + gm_5 \cdot v_{GS}(t)^5$$
$$(2.14)$$

as well as the coefficients:

$$gm_n = \frac{1}{n!} \frac{\partial^n i_D[v_{in}]}{\partial v_{in}^n} \bigg|_{v_{in} = V_{GS}; V_{DS} = const.}$$
$$(2.15)$$

Self-biasing effects are especially critical for a GaN-HEMT driven into saturation. The gate-collapse increases the self-biasing for high input power ratios.

By considering a large-signal compact modelled GaN-HEMT the large-signal transconductance can be calculated as defined in Eq. 2.15 for various input power levels. The device is therefore biased with various V_{GS} in a stable power match condition at a rather low operation frequency of 1 GHz – not producing parasitic resonances. The static dc output current of this simulation driven at 1 GHz can be seen in Fig. 2.10(a). The input power value of P_{in} = -30 dBm represents a small-signal condition equal to the Fig. 2.9. By applying an increased input power level the device starts self-biasing. An input power level of P_{in} = 15 dBm represents the saturation of the device (P_{out} = 6 W). It can be obtained that the V_{TH} lowers extremely down to -6 V with an increase of input power.

According to the previously analysed amplifier classes of operation, the beginning of a **Class-B** operation located at $\Theta = 180°$ changes during the modulation. As a consequence, the class of operation cannot be determined for the used amplifier because it depends on the input power modulation rather than only the static bias.

In addition, the gm changes drastically with a decrease, while the output power achieves its maximum $P_{out,f1}$. The influence of the static gate bias to the output power level of the second harmonic is displayed in Fig. 2.10(e) indicating only a 20 dBc distance to $P_{out,f1}$ for the saturation case.

The previously stated definition of a correct V_{TH} located at the zero of gm_3 still works for the increased driving level, while in Fig. 2.10(f) this zero can no longer be obtained because of a huge decrease in gm_3. It can be noted that also the amount of third harmonics (Fig. 2.10(g)) only varies in a range of ± 5 dBc for the saturation case – mainly independent of the static biasing conditions - while for less input power its level significantly changes.

Large-Signal IMD in Amplifiers

Nowadays, multi-tone excitation is the common operation mode for a power amplifier within the data-communication segment. The spacing in between the carriers depends on the signal type. Two

(a)

(b) gm_1

(c) $P_{out,f1}$

(d) gm_2

(e) $P_{out,f2}$

(f) gm_3

(g) $P_{out,f3}$
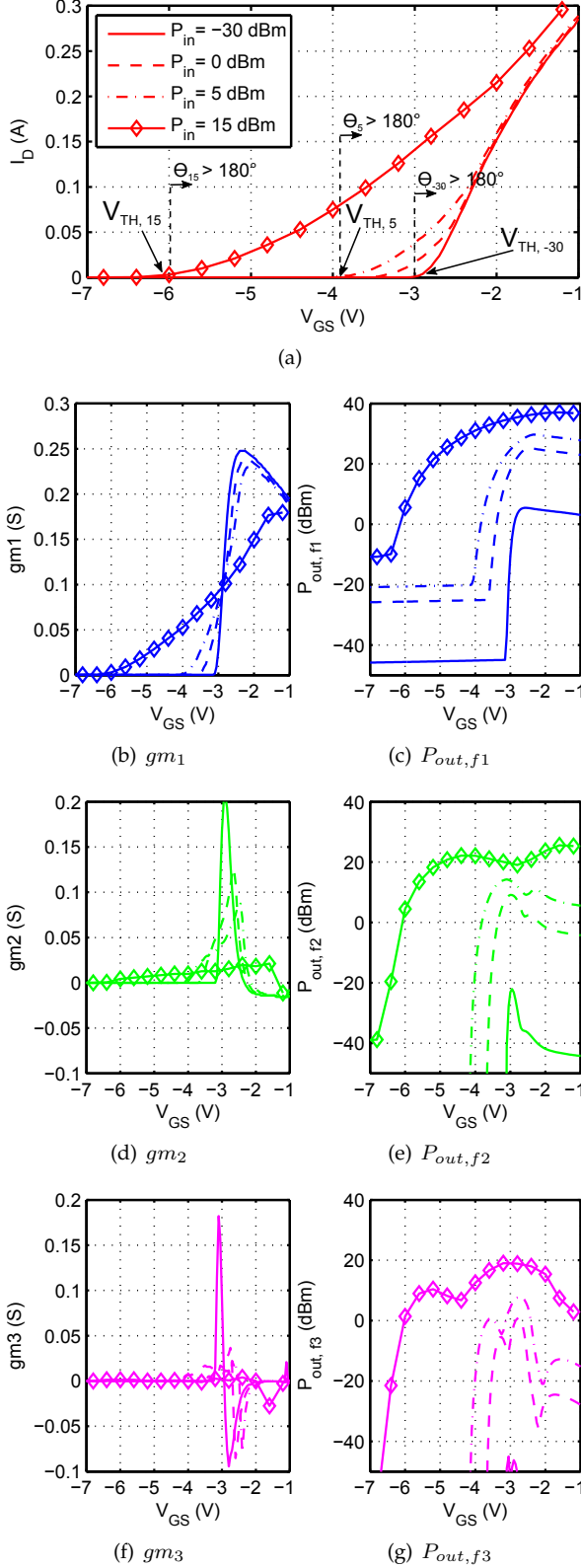
FIGURE 2.10: Simulated example of ac large-signal gm behaviour as a function of V_{GS} and P_{in} for a 250 nm GaN-HEMT (CGHV1J006D; $V_{DS} = 40$ V; 1 GHz).

carriers with its power (A_1, A_1) can be defined as

follows:

$$v_{GS}(t) = A1 \cdot \left[cos(\omega_1 t) + cos(\omega_2 t) \right]$$
$$+ A2 \cdot \left[cos(2 \cdot \omega_1 t) + cos(2 \cdot \omega_2 t) \right] \quad (2.16)$$

By the excitation of multiple generated frequencies into the non-linear circuit, like in Eq. 2.9, the number of harmonics as well as their mixing products increase. This is called intermodulation. The mixing order defines the order of intermodulation distortion, for example, IMD3 or IMD5. Unlike harmonics, the IMD products cannot be filtered because they are located too close to the carrier. The power of the IMD3 and IMD5 products is highly related to the higher order transconductances. The fundamental output current can be defined by:

$$i_{D,f0} = cos(\omega_1) \cdot \left\{ gm \cdot A_1 + gm_2 \cdot A_1 A_2 + \right.$$
$$\left. gm_3 \cdot \left[\frac{9}{4} A_1{}^3 + 3 A_1 A_2{}^2 \right] \right\} \quad (2.17)$$

By skipping the amount of harmonics the important IMD3 products can be defined as:

$$i_{D,IMD3} = cos(2\omega_2 - \omega_1) \cdot \left\{ gm_2 \cdot A_1 A_2 + \right.$$
$$\left. gm_3 \cdot \left[\frac{3}{4} A_1{}^3 + \frac{3}{2} A_1 A_2{}^2 \right] \right\} \quad (2.18)$$

By observing that $gm3$ strongly depends on the chosen bias point, we can reduce the amount of IMD3 by choosing the right bias conditions. The minimum of IMD3 is referred as a *sweet spot* condition [Car+99]. This *sweet spot*, or the beginning of a **Class-B** operation, can be assumed to determine the biasing conditions with the lowest amount of IMD3 products. Note that this assumption varies with the change of V_{DS} as well as the temperature conditions of the device. In addition, it depends on the input power conditions as already shown in Fig. 2.10(a).

The distance between one of the two-tone carriers to its IMD3 product is the intermodulation distortion IMD3. It can be analysed by the previously used large-signal simulation of the 250 nm GaN-HEMT device with two carriers separated with 1 MHz spacing around 1 GHz.

(a)

(b)

(c)

(d)
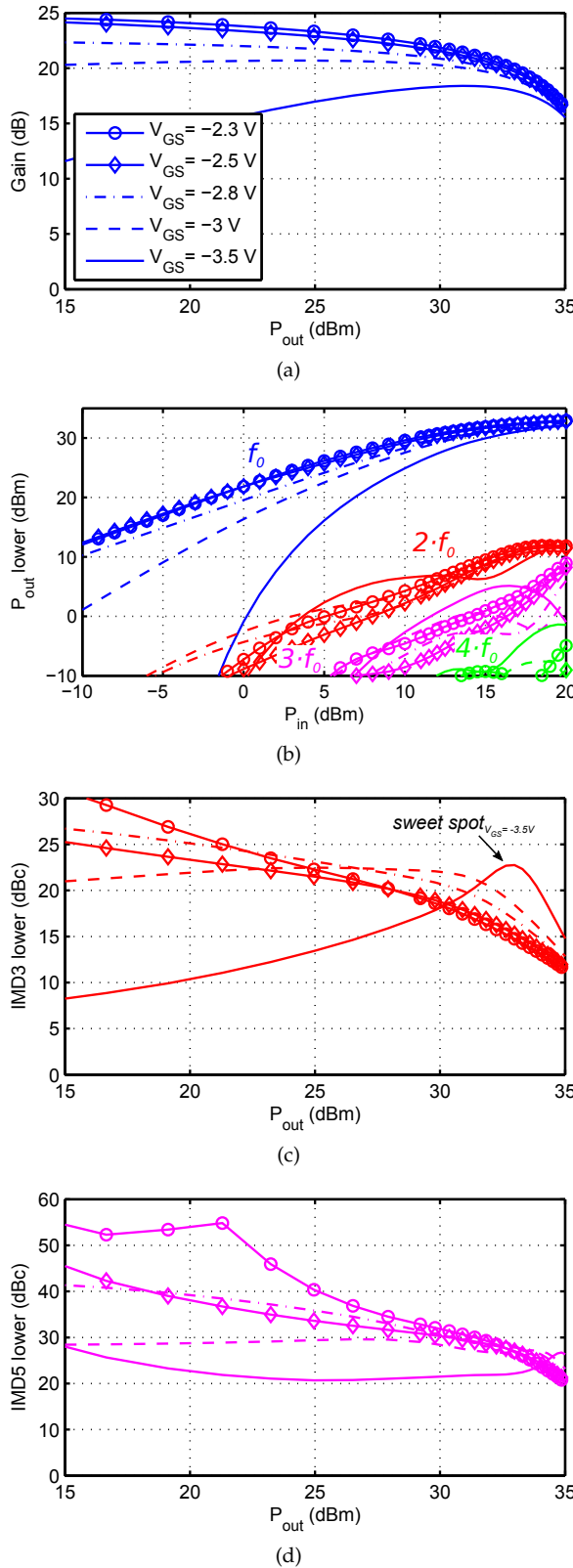
FIGURE 2.11: Simulated example of (a) two-tone gain (b) harmonics (c) IMD3 (d) IMD5 for a 250 nm GaN-HEMT (CGHV1J006D; V_{DS} = 40 V; 1 GHz; 1 MHz spacing).

The operation point with a max. gm for small-signal conditions can be determined with V_{GS} = -2.3 V which is equal to 100 mA quiescent current.

This operation condition is the one most equal to a **Class-A** operation representing the highest gain (Fig. 2.11(a)) and a low amount of IMD3 (Fig. 2.11(c)), particularly for lower output power levels. By decreasing the biasing V_{GS} = -3 V, the gain decreases in the back-off with the positive effect of lowering the soft-compression. In addition, the IMD3 increases for the back-off, but decreases towards saturation. This *sweet spot* behaviour can be clearly observed for a V_{GS} = -3.5 V in Fig. 2.11(c) while for its gain an expansion can be observed. By considering higher order intermodulation products the IMD5 is shown in Fig. 2.11(d). The biasing conditions of V_{GS} = 3 V display a compromise of a constant 30 dBc distance to its carriers.

The appearance of IMD3 or IMD5 related *sweet spots* depends furthermore on the tone spacing, the harmonic match as well as the selected baseband impedance. For use with modulated signals, special care must be taken so that the chosen *sweet spot* of the IMD3 doesn't produce a sensitivity of the IMD5 that results in an unwanted increase of those side-band products.

In theory, the extrapolated increase of the IMD3 products results in the third order intercept point (OIP3), crossing the linear extrapolation of the power increase. This assumption can be done for small-signal gm analysis. However, the assumption that the slope of this IMD3 increase is constant cannot be observed in Fig. 2.11 for large-signal observations. In conclusion, an OIP3 or OIP5 analysis is not useful for power-amplifiers operating towards the **Class-C** biasing conditions.

Additional calculations and nomenclature regarding amplifiers are provided in Appx. A.3.

2.4 SatCom Signals

SatCom signals rely on an amplitude and/or phase-shift keying technique. From the beginning of SatCom a simple QPSK modulation was used. For use within broadcasting applications, DVB-S1 defines the common modulation schemes to be BPSK, QPSK, OQPSK and 8PSK with various forward

TABLE 2.5: PAPR (dB) of different modulation schemes

α	DVB-S2				
	DVB-S1				
	BPSK	QPSK	8PSK	16APSK	32APSK
0.35	4.1	3.9	3.8	4.8	6.2
0.25	5.1	4.9	4.7	5.7	6.8

error corrections (FEC). Beginning with the DVB-S2 definitions, optional modulation schemes of 16APSK with up to 32APSK can be used, while a backward compatibility is granted [ETS09]. In addition, the necessary SNR of the signals decreases within DVB-S2 due to the improved coding. The roll-off factor can also be reduced down to $\alpha = 0.2$ to improve further the spectral efficiency. The increased PAPR is displayed in Tab. 2.5.
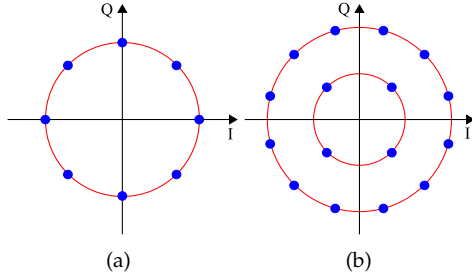
FIGURE 2.12: Constellation Diagram of modulation schemes for DVB-S2 transmission (a) 8PSK (b) 16APSK.

An example for the constellation diagram of an 8PSK and a 16APSK is given in Fig. 2.12. Note that in comparison to QAM a lower number of possible amplitude levels is achieved. It is therefore known to be more robust.

DVB-S2x is planned to be described within the newer ETSI definitions. It will extend the previous DVB-S2 regulation by the usage of up to a 256APSK with smaller roll-off factors down to $\alpha = 0.05$ for streaming UHDTV. The choice of modulation scheme is related to the signal to noise ratio (SNR), which is achieved at the satellite receiver. With the usage of DVB-S2 signals, various modulation schemes can be analysed regarding their necessary SNR. Depending on the bit error rate (BER), the SNR is shown in Fig. 2.13(a) with an FEC of 5/6. With the knowledge of the PAPR (given in Tab. 2.5), the error vector magnitude (EVM) can be calculated (Fig. 2.13(b)). It can be obtained that the

robust QPSK tolerates a high EVM $\geq 50\%$ while higher order modulation schemes degrade fast.
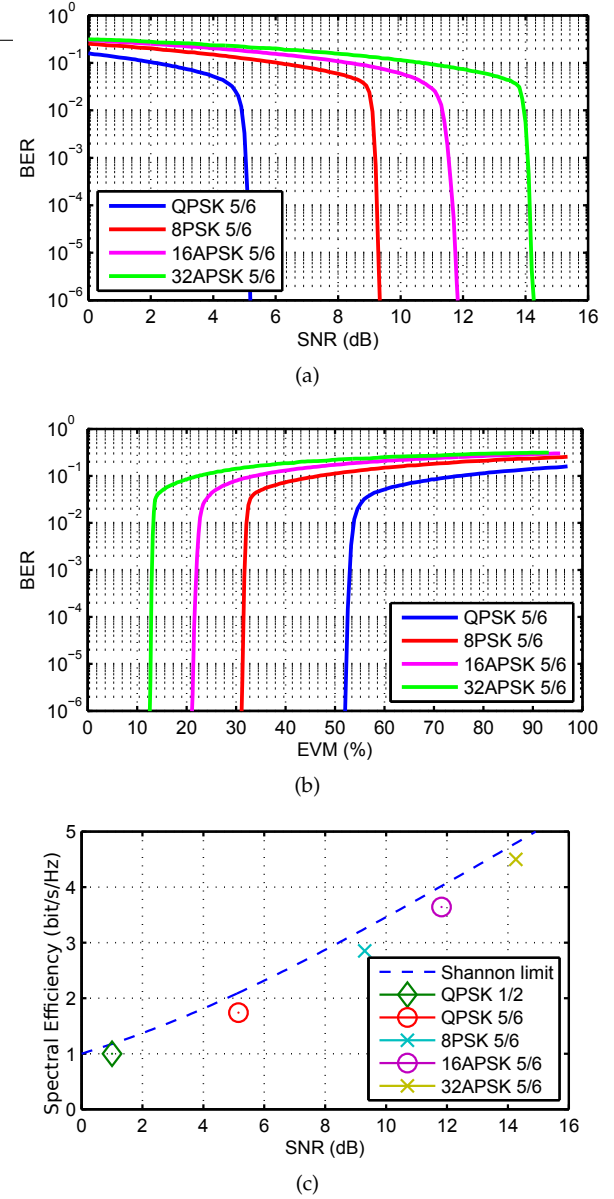
FIGURE 2.13: Theoretical analysis of (a) BER vs. SNR (b) BER vs. EVM for various modulation scheme (DVB-S2; $\alpha = 0.25$) (c) Spectral Efficiency vs. SNR (DVB-S2; $B = 6\,\text{MHz}$; $\alpha = 0.25$; BER $= 10^{-6}$).

For an equivalent thermal noise power of $N_0 = $ -174 dBm/Hz the various modulation schemes can be obtained close to the Shannon-limit in Fig. 2.13(c) at BER $= 10^{-6}$.

2.5 Measurement Techniques

Microwave measurements are distinguished into small-signal and large-signal measurements. A detailed description of all measurement techniques can be observed in [Dun12] while in the following subsections only a brief introduction to the used techniques is given.

FIGURE 2.14: Definition of the reference planes used within a probed measurement setup.

Small-Signal Measurements

Small-signal measurements represent the situation where all measured components are situated far away from their saturation. Vector Network Analyser (VNA) are commonly used to proceed this by measuring the forward (a_i) and reflected (b_i) wave quantities (Appx. A.6). Depending on the VNA the number of measurement ports (i) varies while the transmission and reflection from each port to each other port can be displayed through the use of the S-Parameters (Appx. A.13).

The analysis of the wave-quantities relies on the detected voltage that itself depends on the reference plane where this voltage takes place. On account of these reference plane dependent wave quantities, calibration techniques are used, to shift the reference plane along the measurement setup. The General Short Open Load Thru-procedure (GSOLT) is probably the most common calibration technique relying on well-defined calibration standards [Heu03]. After measuring these standards, its parasitic (known) behaviour is subtracted from the measurement results. With the knowledge of all measured standards and the measured device under test (DUT) the S-Parameters of the DUT at the defined reference planes (e.g. connector) can be extracted.

An additional second tier calibration can shift the reference plane along the measurement setup directly on the DUT substrate. Hence calibration standards can be manufactured directly on the substrate through the use of the Thru Reflect Line-procedure (TRL) [Eng+79]. This technique can take advantage of using no resistive match, which

comes along with parasitics, but a TL with its defined characteristic impedance. This technique is especially useful for probed measurements, where ground signal ground (GSG) probes are necessary. The outer contact (ground) of the probe connects to the substrate ground via the GSG pad. The inner contact (signal) serves as connection to the TL located on the substrate.

Fig. 2.14 visualizes the separation of the various calibration techniques related to a probed measurement setup. The increased number of connections from the port of the VNA to the DUT raises the sources of error considering a loose connection, phase instabilities or mismatch reflection. In view of the fact that these sources of error are difficult to obtain, a second-tier calibration TRL (e.g. on the DUT substrate) after an already proceeded GSOLT (e.g. On-Wafer calibration) makes sense. By contrast, each calibration technique can be used standalone as well. A detailed analysis of the frequency dependent uncertainties, caused by this measurement setup, is given in Appx. A.5 and is related to the Metas VNA-Tools™ uncertainty calculation [Wol+12].

De-embedding

A de-embedding of a connector or a probe-pad can be realised by a TRL calibration directly within the VNA or in MATLAB™. The combination of the measured Thru, a Reflection and a Line is sufficient for obtaining the feeding structure of the probe-pad. A transformation from the derived S-Parameter Matrixes (S_{tot}) into a T-Parameter structure $[T_{tot}]$ (Appx. A.12) displays a sequence of multiplications, representing the series setup

(Pad - DUT - Pad).

$$[S_{tot}] \Rightarrow [T_{tot}] = [T_{Pad}] \cdot [T_{DUT}] \cdot [T_{Pad}]^{-1} \quad (2.19)$$

According to the techniques defined in [Eng+79] any pad structure can be de-embedded with the remaining T_{DUT} that can be converted to the S_{DUT}. This principle is applied throughout this work. It is especially useful for shifting the reference plane from a coaxial to a WG reference plane.

Large-Signal Measurements

By considering large-signal conditions, in which measured components are situated towards their compression, the voltage level needed to be detected increases. Particularly with the use of PAs, a high amount of voltage and current swing needs to be detected. Hence power detectors measure the incoming and outgoing scalar power of the DUT. A power measurement needs to be distinguished into true RMS measurements related to the usage of thermocouple or thermistor detectors and the use of peak power meters, detecting the voltage. For the case of distortion free CW signals, both types of power meters deliver an equivalent value.

Since the diode voltage detectors are calibrated by using the known relationship between RMS and peak voltage (PAPR), they cannot be used for AM and SSB (two tone) signals. Furthermore, harmonic distortion will cause unpredictable results, while a distance of ≥ 50 dBc can be tolerated. During a calibration of the power-head, the power reference is certified with an uncertainty $P_{REF,unc} = \pm 0.6\%$, while the instrument itself adds up to $P_{REF,inst} = \pm 0.5\%$. The main cause of measurement errors in power measurements is still the uncertainty of the power meter, while an attached source is connected within mismatch conditions here defined as $P_{PM,unc}$.

To achieve an appropriate power level at the power head, the input as well as output power of a DUT is extracted from the measurement setup via directional couplers (dc, shown in Fig. 2.15). By considering the various matching levels at all the
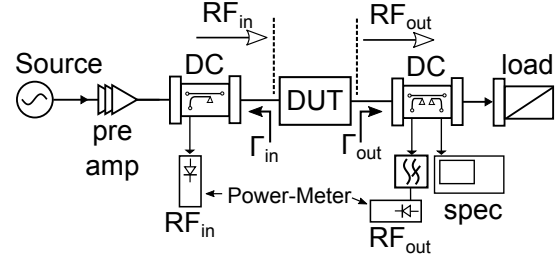
FIGURE 2.15: Schematic view of the large-signal measurement setup.

reference planes within the large-signal measurement setup, the total measurement uncertainty can be calculated. The RL, IL and directivity of the coupler needs to be considered for a measurement setup regarding a low measurement uncertainty. For the use of a DUT with a low amount of matching, the isolation of the coupler becomes the most relevant value. To prevent failures related to the mismatch uncertainty, the power that was measured for the PAs of this work was obtained through high directivity WG-couplers at the input and output, respectively.

By the knowledge of the coupling (in: 30 dB, out: 40 dB), matching (20 dB) and isolation (60 dB) of the couplers, the measurement uncertainty of this net-power can be calculated as in [Che+05]. By assuming that all interconnections are matched to ≥ 20 dB with a random phase, the only mismatch is inserted by the DUT at the input (Γ_{in}) as well as the output side (Γ_{out}). The obtained standard deviations ($P_{in, unc}$, $P_{out, unc}$) is shown in Tab. 2.6 for both measurement positions (RF$_{in}$, RF$_{out}$). With a decrease of the RL down to only 10 dB the deviation increases up to $P_{in, unc} = 0.23$ dB at the input and up to $P_{out, unc} = 0.34$ dB. Its statistical distributions are visualized in Appx. A.5.

TABLE 2.6: Power measurement uncertainty related to mismatch conditions

VSWR	1	1.05	1.1	1.22	1.5	1.92
RL (dB)	∞	30	25	20	14	10
$P_{PM,unc}$ (%)	0	0.1	0.25	1	4	10
$P_{in, unc}$ (dB)	0.01	0.02	0.05	0.07	0.14	0.23
$P_{out, unc}$ (dB)	0.01	0.02	0.05	0.12	0.31	0.34

Load-Pull Measurements

Load-Pull is originally a technique that is able to measure performance values of a transistor while constantly changing source and load impedances. The DUT is therefore located within a test-bench that ideally does not provide any matching to the transistor, only the biasing. This test-bench needs to provide as low losses as possible to realise a high reflection coefficient on the transistors in and output plane (Γ_{in}^*, Γ_{out}^*). Load-Pull tuners are realised based on low loss coaxial airlines, equipped with two motorized sliding open stubs. The open stubs and the airline in between both build a π-network. Due to well-chosen electrical lengths of the stubs as well as the airlines, this Load-Pull tuner is able to realise any arbitrary impedance among the Smith Chart at the coaxial reference plane. During a calibration a certain amount of arbitrary impedances can be positioned and measured with a VNA. By each of these, the frequency dependent insertion loss as well as return-loss is now saved within a software that can later compute the forward and reflected power to the DUT.

The outer area of the Smith Chart, which represents the highest reflection coefficient Γ, can only be reached by extremely low loss Load-Pull tuners due to the limited quality factor of the open stubs. In addition, the amount of power that a Load-Pull tuner is able to withstand is limited by its inherent losses. This is why it changes its electrical behaviour within high power applications, which increases the measurement uncertainty while measuring. The larger the transistor representing the DUT, the lower its optimal impedances are. For this reason it is increasingly difficult to provide the high reflection coefficients to the transistors reference plane. Additionally, the already limited
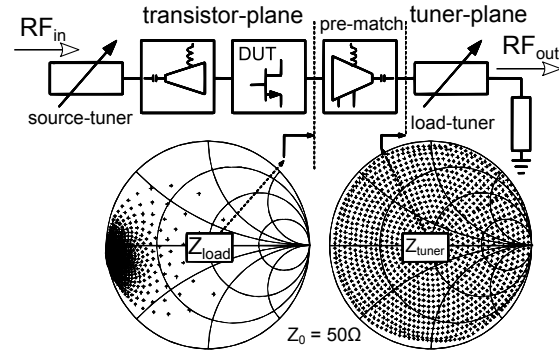
FIGURE 2.16: Illustration of the pre-transformed Load-Pull setup.

amount of Γ that is realised on the coaxial reference plane is further reduced by the pre-transformation and the losses of the test-bench. By choosing a well-known transformation network (pre-match) within the test-bench, it is possible to transform the discrete amount of Γ at the coaxial tuner plane to an area located more at the edge of the Smith Chart boundaries for the transistor-plane which is shown in [Maa+13] (Fig. 2.16). The technique used was able to improve the low-ohmic impedance accuracy for a packaged 50 W GaN-HEMT transistor at 2.45 GHz.

With an increased frequency towards the *Ku*-band, the inherent losses of the tuner as well as the test-bench will increase extremely. Hence the possible amount of Γ that can be provided to the transistors plane decreases further. Additionally, mounting and bonding tolerances increase to the biggest amount of uncertainty within the Load-Pull setup. Consequently, higher frequencies transistors were directly measured on its wafer with a probed Load-Pull setup that is either active or passive. However, the size of the transistors are limited by the pitch of the probes and its power capability, while a higher pitch of a (GSG)-probe lowers its upper frequency limit, as shown in Appx. A.1.

3 Power Amplifier

This chapter will describe the design, analysis and characterization of *Ku*-band power amplifiers. Initially, a commercially available GaAs MMIC PA was combined to achieve matching as well as a sufficiently high output power described in Sec. 3.1. It relied on a simple branch-line combining and was used as a measurement amplifier as well as for preliminary tests. The design had been previously published in combination with a linearisation setup in [Maa+15a].

In the following sections a design procedure for GaN-HEMT MIC PAs is given following the flow chart of Fig. 3.1, which starts with a detailed process description. The transistor technology and its model are analysed in Sec. 3.2. Optimum input-output-impedances are found based on Load-Pull simulations as well as theoretical assumptions. These classical Load-Pull simulations are extended to a new multi-frequency Load-Pull analysis technique.

The manufacturing of matching circuits leads to certain parasitics that are analysed in correlation with the device in Sec. 3.2.1. Taking into account the bandwidth, power and efficiency, ideal matching limits are addressed as well. Finally, Load-Pull related aspects concerning the linearity as well as harmonic matching are analysed.

The first GaN-HEMT PA design is described in Sec. 3.3 which will fulfil the recommendations of SatCom uplink PAs in the frequency range between 13.75 - 14.5 GHz (F_{up}) while it is already
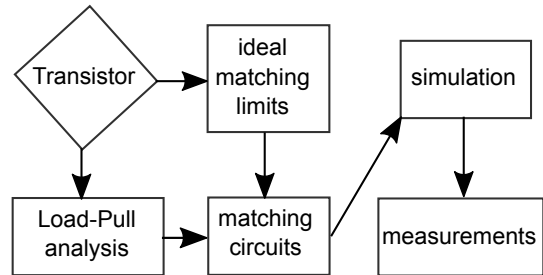
FIGURE 3.1: Flow chart of the PA design procedure.

published in parts [Maa+17a]. The explanation includes the design steps of the matching circuits, the simulation approach as well as the necessary measurement techniques.

To prove the methodology another design was proposed which should fulfil a lowered frequency range from 12.5 - 13.5 GHz (F_{low}) with a slightly higher FBW and is described in Sec. 3.4.

In addition one design was developed to provide a sufficient uplink power within both frequency ranges extending the previous designs to 12.75 - 14.5 GHz (F_{ext}) (Sec. 3.5).

Finally, these amplifiers are analysed on their potential to further improve its efficiency based on efficiency enhancement techniques, like envelope tracking or Doherty, in Sec. 3.6.

A discussion compares the developed amplifiers to previous state of the art work that can be either a MMIC or a MIC (Sec. 3.7).

3.1 Combined MMIC PA

Within this design a high gain $0.25\,\mu m$ gate GaAs p-HEMT technology was chosen to focus on a measurement pre-amplifier. The small signal gain of one packaged chip is approx. 25 dB and lowers to less than 20 dB in saturation. The PAE of one chip in the 1 dB compression is $\approx$18 %.

To increase the output power of this commercially available packaged amplifier, and therefore get enough drive level for our own developments, a two stage branch-line combining on a $228\,\mu m$ RO4003c substrate with an ε_r=3.55 was chosen. The losses in these high frequencies cause the branch-line combiner not to be flat over the upper *Ku*-band bandwidth (13.75-14.5 GHz). The combiner is therefore capacitively loaded at the $50\,\Omega$ port side with a high Q and high SRF Capacitance (ACCUP 0.1 pF). This technique compensates for the losses to higher frequencies (Fig. 3.2).

The bias point needs to be chosen in a **Class-A** range to overcome poor gain as well as low linearity in the *Ku*-band. This of course results in a low PAE and a higher power consumption. An expansion in the modulation standard with an increased PAPR drives the amplifier even more in the back-off operation.

The final small signal gain of the two stage design is higher than 22 dB from 13.5 GHz to 16.2 GHz for a supply voltage of V_{DS}=8.5 V and I_{DQ}=4 A quiescent current. The PA has an output power of $P_{out,1dB}$=9 W with a moderate PAE of 16% around 14 GHz. The PAE drops to approx. 12 % when

FIGURE 3.3: Picture of the PA with two packaged GaAs p-HEMT transistor combined via capacitive loaded branch-line combiner.
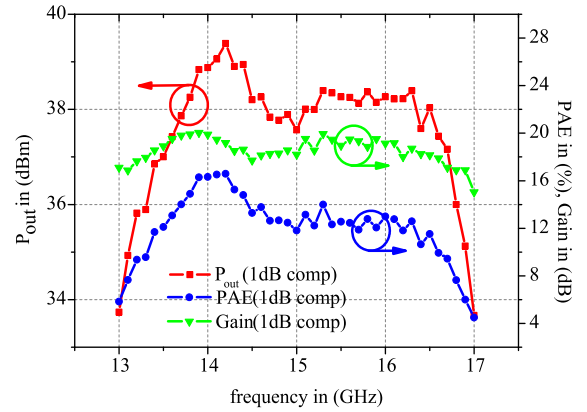
FIGURE 3.4: Large-signal measured output power, PAE and gain at different frequencies within the band for the 1 dB compression point; V_{DS}=8.5 V; I_{dq}=4 A.

taking the complete frequency range into consideration (Fig.3.4).

This low PAE results from both the combining losses and the **Class-A** biasing as well (Fig. 3.4). Nevertheless, the sufficiently high gain paired with the high drive level makes this amplifier an attractive low-cost laboratory amplifier. The use of the branch-line combining makes it withstand possible mismatch conditions based on a fault measurement setup or a DUT that is used behind this pre-amplifier.

FIGURE 3.2: PA schematic with two packaged GaAs p-HEMT transistors combined via capacitive loaded branch-line combiner.

3.2 250 nm GaN-HEMT Analysis

Based on the Wolfspeed 250 nm GaN-HEMT process, there are several bare die sizes available. The smallest represents a bare die, as shown in Fig. 2.7, with N_{ft}=6 gate fingers giving a total gate width W_t=1.2 mm (CGHV1J006D) that should hereby be defined as one *transistor cell*. In addition, another bare die with N_{ft}=4x6 fingers resulting in a total gate width W_t=4.8 mm (CGHV1J025D) is available. Its layout represents exactly 4 times the CGHV1J006D (one *transistor cell*) with a simple interconnection of the drain bus bar while still keeping individual drain pads. To suppress odd-mode instabilities, each *transistor cell* is separated at the gate bus bar with R_{odd}=200 Ω gate stability resistors (Fig. 3.5). The bare die CGHV1J070D with a further increased N_{ft}=12x6 number of fingers ends up with W_t=14.4 mm total gate width (12x *transistor cell*) and is shown in Fig. 3.6.

The specifications resulting for the different bare die sizes are summed up in Tab. 3.1 while the saturated power represents a typical value of 5 W/mm gate width for a modern 250 nm GaN-HEMT process.

Based on the double field plate technique the break-down voltage of the device is very high, defined with $V_{BD} \geq 100$ V. A pinch off with $V_{p\text{-off}}$ = -3.1 V demonstrates the normally-on characteristics of GaN-HEMTs. The max. ac - transconductance is gm ≈ 580 mS/mm for V_{GS} = -2.65 V at 14 GHz. The parasitic capacitances are C_{GS} = 1.6 pF, C_{DS} = 0.29 pF and C_{GD} = 0.41 pF per mm gate width [Wol12].

To obtain a high output power of $P_{out} \approx 50$ W the largest device CGHV1J070D was chosen. It is specified with a $P_{out,sat}$ = 70 W and an $I_{D,max}$ = 7 A for a size of 4.8 mm x 0.8 mm. Especially the high total in- and output capacitances of C_{GS} = 24 pF and C_{DS} = 4.2 pF make the matching towards high frequencies very challenging. Note that based on the diel. parameters given in Tab. 2.1 the electrical length is $\frac{\lambda}{4}$=2.3 mm at 14 GHz on the SiC substrate. Therefore, the width of the SiC semiconducting area (Mesa) of this large bare die exceeds
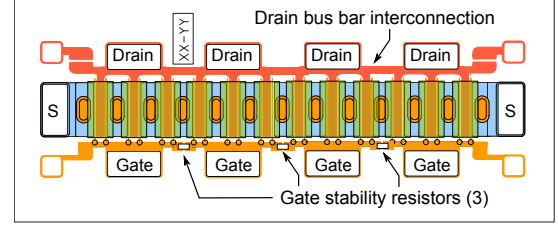
FIGURE 3.5: Top view of the N_{ft}=4x6 gate finger GaN-HEMT of Wolfspeed (CGHV1J025D) representing 4 *transistor cells*.

TABLE 3.1: Specifications of the 250 nm GaN-HEMTs process at 10 GHz.

W_t	N_{ft}=6 1.2 mm	N_{ft}=4x6 4.8 mm	N_{ft}=12x6 14.4 mm
$P_{out,sat}$ (V_{DD}=40 V)	6 W	25 W	70 W
$I_{D,sat}$ (V_{DS}=6 V)	1.1 A	4.3 A	13 A
η_{max} (I_{DQ}=5% $I_{D,sat}$)	60%	60%	60%
G_{SS} (I_{DQ}=5% $I_{D,sat}$)	17 dB	17 dB	17 dB
C_{GS} (V_{GS}= -8 V)	2 pF	8 pF	24 pF
C_{DS} (V_{DS}= 40 V)	0.35 pF	1.4 pF	4.2 pF
C_{GD} (f=1 MHz)	0.5 pF	0.2 pF	0.6 pF
V_{BD} (V_{GS}=-8 V)	100 V	100 V	100 V
$I_{G,max}$ (V_{GS}=2 V)	2.1 mA	4.8 mA	14.4 mA
$R_{\Delta\,max,\,JC}$	25 K/W	3.6 K/W	1.1 K/W

a $\frac{\lambda}{4}$ dimension for 14 GHz (Fig. 3.6). Given that the second harmonic frequency is located at 28 GHz, the die itself already has a width $\geq \frac{3}{4}\lambda_{2\cdot f_0}$. The $R_{\Delta\,max,\,JC}$ defines the maximum thermal resistance of the bare die bottom to the case, not exceeding the thermal limitations of the channel which drops towards the largest bare die.

3.2.1 Manufacturing Limitations

Mounting

The source contact of the bare die acts as interconnection to the GND potential of a matching circuit. Furthermore, it is the connection to the heat sink. The mounting of the bare die therefore needs to be low ohmic for matching requirements and of a minimum thermal resistance. In this work an eutectic die-attach compromises between a thin AuSn preform (20 μm) and a low amount of trapped air in the die-attach. In order to allow a controlled thermal expansion, the bare die was mounted on
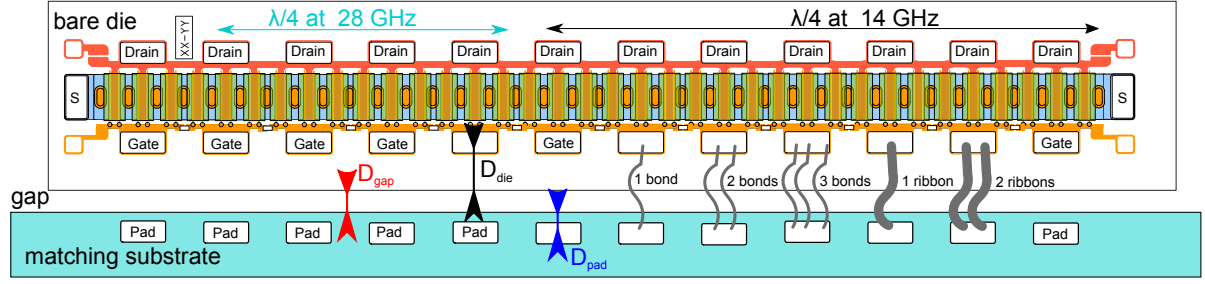
FIGURE 3.6: Top view of the N_{ft}=12x6 gate finger GaN-HEMT of Wolfspeed (CGHV1J070D) representing 12 *transistor cells*.

(a)

(b)
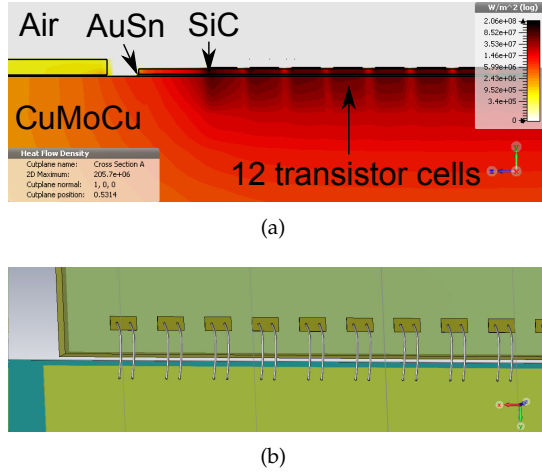
FIGURE 3.7: (a) Sideview of FEM simulated mounting heat flow density of 100 W dissipated power (b) Top view of the 3-D EM simulation with 24 bond wires.

a 1.5 mm thick CuMoCu flange. Thermal simulations are based on the assumptions of [Pre+09] and show that the resulting thermal resistance of the junction to case is $R_{\Delta JC} = 1.6°K/W$. The thermal conductivity was adaptively varied for GaN in relation to an increased channel temperature. By considering a PAE of 45%, a significant amount of dissipated power needs to be removed via the cooling system. In reality, the PAE will be even lower due to impedance mismatches and losses of the load transformation networks. X-Ray pictures of the mounting are finally taken to count the amount of trapped air within the soldering. The channel temperature of the device can be monitored with the model and needs to stay below $320°$ C, while a higher temperature will cause the device to fail. The theoretical possible cooling therefore limits the dissipated power to $P_{diss,max} \approx 86.4$ W. This possible cooling will be further degraded via a thermal coupling of other heat dissipating components.

Bonding

Twelve gate and twelve drain pads needed to be interconnected to the matching circuit. Thus, an array of 24 bond wires was 3-D modelled and applied at the input and output respectively with two parallel wires per pad. The resulting total equivalent inductance is L_{Bond} =12.5 pH including the mutual coupling. This value is of certain tolerance considering the bondheight, loop and distance. To increase the height and loop accuracy, automatic bonding is useful. It can achieve impressive results even for the aim of coupling between bond wires [CC+11].

However, the bond distance is mainly dependent on the mounting accuracy D_{gap}=60 ± 30 μm as can be seen in Fig. 3.6. D_{die} is initially 177μm with the size tolerances of the bare die itself ($-50\,\mu m$), set in relation to the total size of the die ($800\,\mu m$), the tolerances are going to be defined as ($-12\,\mu m$). In addition, the distance from the metallisation of the

TABLE 3.2: Bonding tolerances

distance	value (μm)	tol. (μm)	max; min (μm)
D_{die}	177	-12	177; 165
D_{gap}	60	±30	90; 30
D_{pad}	40	±30	70; 10
D_{total}	277	+60; -72	340; 203
inductance	(pH)	(pH)	(pH)
L_{2bonds}	139	+30; -36	169; 103
$L_{24bonds}$	11.6	+2.5; -3	8.6; 14.1
L_{3bonds}	92	+20; -24	68; 112
$L_{36bonds}$	7.6	+1.6; -2	9.2; 5.6
inductance EM	(pH)	(pH)	(pH)
L_{2bonds}	150	+50; -50.4	200; 99.6
$L_{24bonds}$	12.5	+4.1; -4.2	8.3; 16.6

matching substrate to the gap needs to be considered with D_{pad}=40 ± 30 μm. These tolerances can be summed up to a total distance between the pad on the die and the pad on the matching substrate as shown in Tab. 3.2. With a simple approach of choosing 2 bond wires per pad and the rule of thumb that 100 μm bond wire results in 100 pH inductance, we get the values of L_{2bonds} for one pad interconnection. All 12 pad interconnection reduce the inductance to $L_{24bonds} \approx 11.6 \pm 60$ pH.

The EM-simulations have shown that the variability of the total equivalent inductance is in the range of $L_{Bond} = \{8.3\,\text{pH}...16.6\,\text{pH}\}$ for the worst case scenario. In reality, the tolerances can be reduced by measuring the alignment accuracy and therefore calculating the optimal bond wire distance and loop respectively. This would reduce a possible frequency shift of the matching circuits that is related to the inductive pre-transformation.

3.2.2 Optimum Impedances

The optimum load-line resistance that represents the intrinsic current source (for Class A) can be calculated [Cri06] as:

$$R_{dc} \,\hat{=}\, Z_{o\,int} = \frac{V_{DS,OP} - V_{knee}}{0.5 \cdot I_{max}} = \frac{37\,V}{3.5\,A} = 10.5\,\Omega \tag{3.1}$$

The additional intrinsic capacitance C_{DS} as well as the pad and interconnection inductance transform the real $Z_{o\,int}$ to the optimum load impedances $Z_{o\,ext}$. By considering a power match condition, the impedances looking into the matching circuit need to be $Z^*_{o\,ext}$ (Fig. 3.8). This simple approach represents a very good approximation to the simulated optimum source and load impedances that are discussed later on and stated in Tab. 3.3.

3.2.3 Ideal Matching Limits

The impedances of the bare die itself can be analysed based on the Bode Fano limits [Fan50]. By using the simple transistor-schematic from Fig. 3.8, an equivalent impedance $Z'_1(s)$ of the L, C, R for the input as well as for the output can be stated and
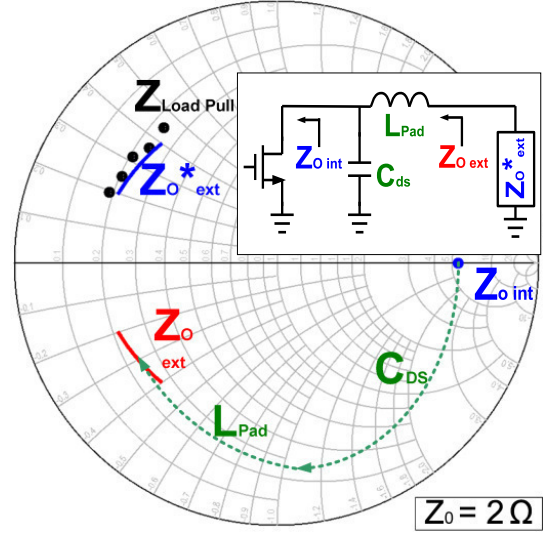
FIGURE 3.8: De-embedding from the intrinsic dc impedance to the optimum load impedance.

analysed towards a maximum achievable bandwidth as in [Pre+13].

$$Z'_1(s) = \frac{sL + r}{s^2 LC + srC + R} \tag{3.2}$$

A possible ideal matching circuit can be approximated by a Taylor series in the following form:

$$F(s) = ln\frac{1}{\rho} = jA_0 + \frac{A_1}{s} + \frac{A_3}{s^3} + \cdots \tag{3.3}$$

$$\text{with} \quad s = \sigma + j\omega \tag{3.4}$$

Transforming the impedance to an admittance, building the logarithm and negation, leads to:

$$ln\frac{1}{\rho} = ln\left[-\frac{\dfrac{1}{s^2}(R+r) + \dfrac{1}{s}(L+rC) + LC}{\dfrac{1}{s^2}(R-r) - \dfrac{1}{s}(L-rC) + LC} \right] \tag{3.5}$$

For $\frac{1}{s} = 0$ follows:

$$jA_0 = j\pi, \tag{3.6}$$

$$A_1 = \frac{2}{C} \quad \text{and} \tag{3.7}$$

$$A_3 = \frac{2(L-3C)}{3LC^3} \tag{3.8}$$

After Fano et al. [Fan50] an equivalent circuit with two zeros has to fulfil the following two integrals

at $s = \infty$:

$$\int_0^\infty ln\frac{1}{\rho}d\omega = \frac{\pi}{2}\left(A_1 - 2\sum\lambda_{ri}\right) \qquad (3.9)$$

$$\int_0^\infty \omega^2 ln\frac{1}{\rho}d\omega = -\frac{\pi}{2}\left(A_3 - \frac{2}{3}\sum\lambda_{ri}^3\right) \qquad (3.10)$$

Defining $K = \frac{2}{\pi}ln\frac{1}{\rho}$, a centre frequency ω_0, and the bandwidth b a substitution of:

$$\omega_1 = \omega_0(1 - \frac{b}{2}) \qquad (3.11)$$

$$\omega_2 = \omega_0(1 + \frac{b}{2}) \qquad (3.12)$$

leads to the expression

$$K\left(\omega_2^3 - \omega_1^3\right) + 3A_3 - \frac{1}{4}[A_1 - K\left(\omega_2 - \omega_1\right)]^3 = 0. \qquad (3.13)$$

An insertion of A_1 and A_3 from the Taylor series of (3.13) and replacing $\omega_0 L$ with X_L and $\omega_0 C$ with B_C leads to the equation:

$$K^3 - \frac{6}{b_C}K^2 + [\frac{12}{b^2}\left(1 + \frac{1}{B_c^2}\right)]K - \frac{24}{b^3 X_L B_C^2} = 0 \qquad (3.14)$$

This equation can be analysed in *Matlab^{TM}* for the input $Z_{in}\{R_{in}; C_{GS}; L_{pad}\}$ as well as the output $Z_{out}\{R_{dc}; C_{DS}; L_{pad}\}$ of the device. As a result, the theoretically relative matching, which is a function of the bandwidth, was obtained. The parasitic inductances become dominant for higher frequencies. The possible FBW, which can be theoretically matched, therefore depends on the operation frequency. Given that a moderate bond wire distance results in $L_{Bond} = \{12.5\,pH\}$ the dependency of relative matching to the achievable FBW can be seen in Fig. 3.9(a) for various centre frequencies.

Given that a relative matching of 10 dB will be sufficient, the analysed device can be easily matched to a FBW of 80 % for a centre frequency of 2 GHz for the input (Fig. 3.9(a) (top)). The output at 2 GHz is far easier to match to a FBW $\geq$ 150 % because of its lower parasitic capacitance C_{DS} compared to the input capacitance C_{GS}. Furthermore, the Fig. 3.9(a) shows that for an operation frequency of 5 GHz only 20 % FBW can be achieved on the input-side. Therefore, the input capacitance of $C_{GS} = 24\,pF$ is
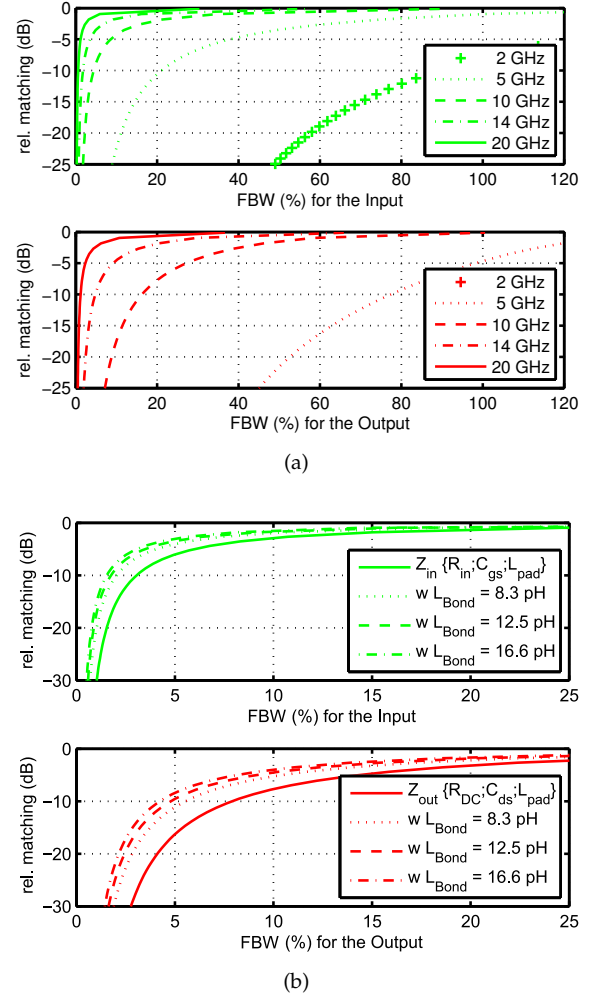
FIGURE 3.9: Analysed theoretical matching limit (Bode Fano) of the complex $Z_{in}\{R_{in}; C_{GS}; L_{pad}\}$ (top) and $Z_{out}\{R_{dc}; C_{DS}; L_{pad}\}$ (bottom) impedances for (a) various centre frequencies (b) for f_0 at 14 GHz.

clearly the limiting factor towards higher frequencies.

The theoretically possible relative matching can be seen in Fig. 3.9(b) on the bare die reference plane itself, as well as with possible L_{Bond} inductances for a centre frequency of 14 GHz. The values of $L_{Bond} = \{8.3\,pH; 12.5\,pH; 16.6\,pH\}$ therefore correspond to the variability of bond wires defined in section 3.3.2. Even by considering a relatively poor matching of only 10 dB, the input achieves less than 2.5% FBW around f_0. This is mainly due to the extremely low $R_{in} = 0.2\,\Omega$ with the high C_{GS}=24 pF.

This relative matching only represents the transformation from the optimum source impedance to
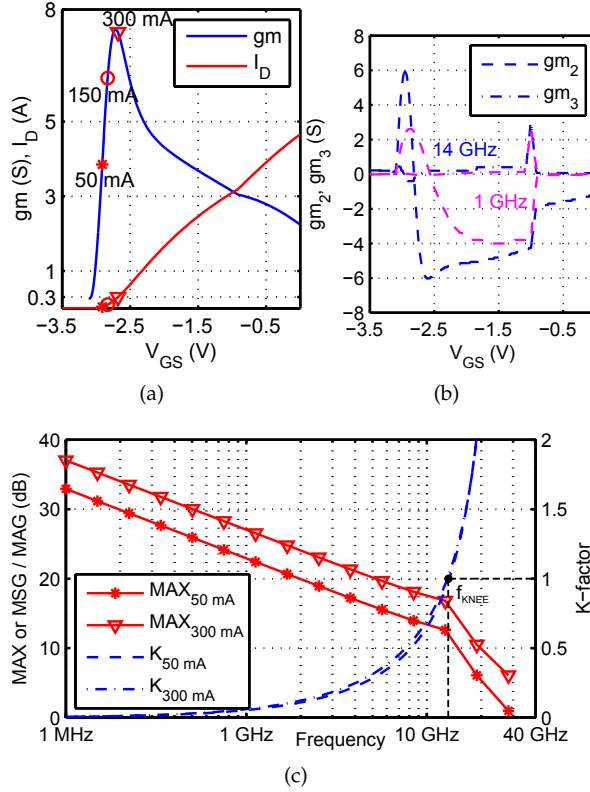
FIGURE 3.10: Simulated (a) ac transconductance gm, I_D (b) 2nd and 3rd derivative of conductance for 14 GHz and (c) MAG/MSG of the device for 40 V operation.

FIGURE 3.11: Simulated parasitic capacitances of the Die for (V_{GS} = -8 V) and (a) 1 MHz (b) 10 GHz.

3.2.4 Device Model

A large-signal device model has been supplied by the manufacturer including non-linear behaviour as well as self-heating. A detailed description of the modelling techniques used by the manufacturer is given in [Pen+12]. The device shows an extremely non-linear ac transconductance behaviour at 14 GHz (Fig. 3.10(a)). The strong decrease of gm after its maximum is related to the high operation frequency and maybe the outcome of the HEMTs so-called parasitic MESFET effect [Gol91]. In addition, the second and third derivatives of the conductance visualize the switching behaviour over V_{GS} (Fig. 3.10(b)). Small-signal analysis shows that the device gets unconditionally stable above 12.5 GHz (Fig. 3.10(c)). Therefore, the possible gain at an operation frequency of 14 GHz is already decreased to 9 dB and degrades further with 20 dB/decade beginning from the knee frequency (f_{KNEE} at K=1). For the drain current of a maximum gm (Fig. 3.10(a)) the extrinsic transit frequency is f_T = 40 GHz with a maximum oscillation frequency of f_{MAX} = 48 GHz.

The parasitic capacitances of the transistor can be analysed and they visualize a low V_{DS} dependency of C_{DS} in Fig. 3.11(a). In addition, it clarifies the dominance of the input capacitance C_{GS} with a non-linear feedback capacitance C_{GD}. For higher frequencies than 1 MHz the de-embedding of the parasitic capacitances does not represent only the capacitances but also the resonances of the complex parallel structure (Fig. 3.11(b)). It can be noted

50 Ω. However, the Source-Pull contours, based on the Source-Pull simulation, shows that a deviation from these optimum values can be tolerated. The output is, considering its higher values of R_{dc} = 10.5 Ω with the high C_{DS} = 4.2 pF, easier to match to at least 8 % FBW w/o the bond inductances. Within this analysis neither the feedback capacitance C_{GD} nor a possible housing or package capacitance C_{pack} is included. A housing capacitance would further increase the C_{GS} or C_{DS} because it is parallel. This means the package capacitance always lowers the theoretically possible relative matching. By contrast, C_{GD} acts as series capacitance in between C_{GS} and C_{DS}. Its parasitic character therefore mainly resonates with the parasitic inductances of L_{pad} and L_{bond}. This feedback results in a lowered gain of the device - which corresponds to a higher R_{dc}. In addition to the already used equivalent circuit, the C_{GD} can be taken into account, which will result in a lowered achievable bandwidth for frequencies up to unconditional stability (f_{KNEE}).

TABLE 3.3: Simulated optimum source and load impe-
dances ($V_{DS} = 40\,\text{V}$; $I_{Dq} = 0.3\,\text{A}$)

f (GHz)	P_{out} (dBm)	PAE (%)	$Z_{S,opt}$ (Ω)	$Z_{L,opt}$ (Ω)
13.0	48.34	48.1	0.25 - j0.08	0.47 + j1.91
13.5	48.39	47.4	0.16 - j0.09	0.48 + j1.82
14.0	48.21	46.0	0.15 - j0.19	0.42 + j1.73
14.5	48.21	44.8	0.15 - j0.21	0.41 + j1.64
15.0	47.94	43.6	0.14 - j0.26	0.38 + j1.57

here that the input as well as feedback capacitance increases, while the drain-source capacitance is almost equal to its pendant at $1\,\text{MHz}$.

The model of the $70\,\text{W}$ device with $W_t = 14.4\,\text{mm}$ total gate width (CGHV1J070D) behaves exactly like twelve times a $W_t = 1.2\,\text{mm}$ model in parallel (CGHV1J006D). That leads to the assumption that the model itself is up-scaled. Vice versa twelve times, a $1.2\,\text{mm}$ model can be seen as twelve times a *transistor cell* and can be used for further analysis to gain deeper insight into cell temperature, current, voltage or the resulting loadline.

Classical Load-Pull

The Load-Pull results of the used transistor were already obtained by the manufacturer and included in its model. Within this chapter, the model is used to perform a Load-Pull analysis only within the simulation software. First the optimization goals of the Load-Pull analysis needs to be defined. The common approach to optimize towards a maximum output power in parallel to a maximum PAE was used. The derived impedances are stated in Tab. 3.3. It can be noted that the optimum load impedances are extremely low ($\approx 0.4\,\Omega$) with little dependence over the frequency range 13 to $15\,\text{GHz}$. By analysing 12 *transistor cells* in parallel (12 x CGHV1J006D), exactly the same impedances can be obtained as shown in Tab. 3.3, which is in accordance to the scaling rules given in Sec. 2.2. However, as shown in Fig. 3.12, a small change in impedance results in a huge difference with respect to P_{out} and PAE. The impedances are shown in the Z-domain, as it is more valuable than the Smith Chart for displaying a "short". All Load-Pull analysis were carried out with an increased

flange temperature of the simulation model of $T_{flange} = 80°\,\text{C}$. This is necessary based on the mounting limitations that have already been obtained in Sec. 3.2.1.

Multi Frequency Load-Pull

The analysed impedances represent optimum values for a certain frequency. To realise a matching over the specified frequency range F_{up}, which is $\{13.75 - 14.5\,\text{GHz}\}$, one would be interested in, for example, the P_{out} dependence vs. F. Classical Source- and Load-Pull contours are only valuable for one frequency. By using the centre point of these contours for each point in F_{up} as optimum impedances, the result would be a huge restriction for the design.

Single frequency contours are summarized with their least intersection (for power or PAE level, respectively) to the newly defined multi-frequency Source- and Load-Pull contours (MuFLoC). A Load-Pull matrix $\left[P_{out,\,f_1}\right]$ that represents all P_{out} values over a certain complex range of $\left[Z_{Load}\right]$, can be defined for fixed biasing (V_{DS}, V_{GS}), a certain input impedance ($Z_{S,opt f_1}$) and the input power conditions (P_{in}) of f_1:

$$f_1 : \left[P_{out,\,f_1}\right] \quad \left(\left[Z_{Load}\right], P_{in}, V_{DS}, Z_{S,opt f_1}\right) \quad (3.15)$$

These matrices can be generated over all in-band frequencies $f_1, f_2...f_n$:

$$f_2 : \left[P_{out,\,f_2}\right] \quad \left(\left[Z_{Load}\right], P_{in}, V_{DS}, Z_{S,opt f_2}\right) \quad (3.16)$$

$$f_n : \left[P_{out,\,f_n}\right] \quad \left(\left[Z_{Load}\right], P_{in}, V_{DS}, Z_{S,opt f_n}\right) \quad (3.17)$$

Now it is possible to calculate the lowest P_{out} value matrix $\left[P_{out,\,F_{up}}\right]$ over all in-band frequencies F_{up}:

$$\left[P_{out,\,F_{up}}\right] = \left[P_{out,\,f_1}\right] \cap \left[P_{out,\,f_2}\right] \cap ... \cap \left[P_{out,\,f_n}\right]$$
$$(3.18)$$

In other words, the $P_{out} = 47\,\text{dBm}$ contour depicted in Fig. 3.12 represents the impedance area where an output power of at least $47\,\text{dBm}$ from 13.75 to $14.5\,\text{GHz}$ (F_{up}) can be expected. In contradiction to that, the individual max. output power contours ($P_{out,max} = 48\,\text{dBm}$) are shown frequency
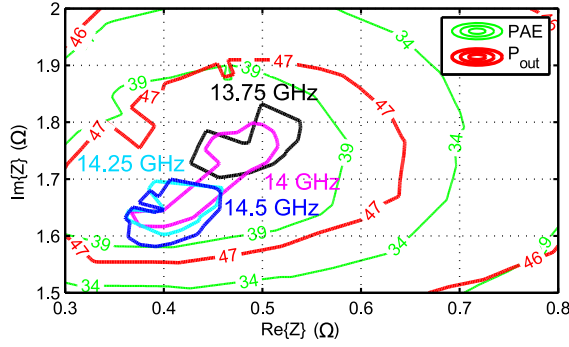
FIGURE 3.12: Simulated optimum Load-Pull impedances Z_{Load} for $P_{out,max} = 48\,dBm$ within $13.75; 14; 14.25; 14.5\,GHz$. Furthermore, multi-frequency Load-Pull contours (MuFLoC) are shown for P_{out} and PAE that represent the least-intersection within F_{up} ($V_{DS} = 40\,V$; $I_{Dq} = \{300\}\,mA$; $P_{in} = 39\,dBm$).

dependent for $f_1 = 13.75\,GHz, ... f_n = 14.5\,GHz$. The same principle applies for PAE with a frequency dependent $[PAE_{out, f_1}]$:

$$f_1 : \quad [PAE_{f_1}] \quad ([Z_{Load}], P_{in}, V_{DS}, Z_{S,opt f_1}) \quad (3.19)$$

and the least intersection over all in-band frequencies F_{up}:

$$[PAE_{F_{up}}] = [PAE_{f_1}] \cap [PAE_{f_2}] \cap ... \cap [PAE_{f_n}] \quad (3.20)$$

During the design procedure of matching circuits these MuFloCs help to observe whether all realised impedances fit within a certain contour or not, whereas using only the optimum impedances means you can just observe a distance between the optimum and realised impedances without any relation to the consequences.

Linearity Load-Pull

By suggesting that a solution for the frequency dependency of the Load-Pull contours was found by the MuFloCs, the influence of the optimum loads regarding linearity cannot be ignored. Ghannouchi et al. state that with a two-tone signal in compression, the resulting intermodulation distortion (IMD) can be used as a sufficient measure of linearity during the Load-Pull analysis [Gha+13, S.197 ff.]. However, this analysis depends on the type of the signal used (e.g. two-tone or a QPSK, 8PSK) as well as on the chosen

operation point. For choosing a two-tone signal with a rather high 10 MHz spacing, Load-Pull contours can be observed with regards to the IMD3, as in Fig. 3.13(a). The dependency of the IMD3 is shown in relation to the chosen quiescent current ($I_{Dq} = \{50; 150; 300\}\,mA$) for a back-off operation ($P_{in} = 30\,dBm$). The spot with the lowest intermodulation is mainly located at a short. The obtained optimum impedances related to P_{out} and PAE are displayed by the crosses $Z_{L,opt}$. One would notice that the low IMD3 located at the short are mainly related to the low output power at this impedance level in contradiction to the so-called *sweet spots* of the biasing.

The same approach can be used for analysing the IMD5 related products as can be seen in Fig. 3.13(b). With an increasing quiescent current the spot moves from the short towards $0.7+j*1\,\Omega$.

Taking a change in the input power level into consideration, we see a totally different behaviour in Fig. 3.14(a). It can be noted that this spot moves towards a purely resistive higher ohmic load ($1+j*0.5\,\Omega$) for this increased compression. The value of the IMD3 degrades with input level due to the increased harmonics. By considering the IMD5 related products, as can be seen in Fig. 3.14(b), the spot area with the lowest intermodulation is located at a point with a higher susceptance ($1+j*1.5\,\Omega$) for these increased input power levels.

By choosing different baseband impedances we
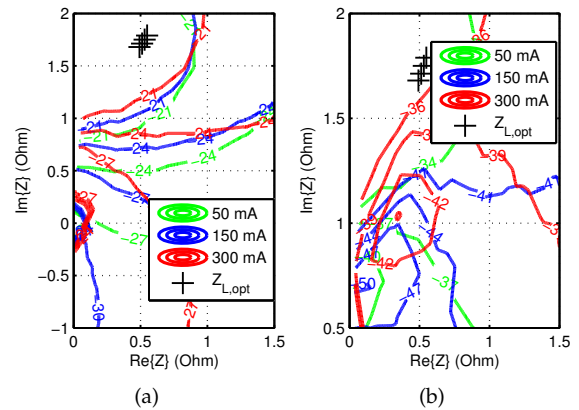
FIGURE 3.13: Simulated (a) IMD3 and (b) IMD5 related load impedances for various quiescent currents ($V_{DS} = 40\,V$; $I_{Dq} = \{50; 150; 300\}\,mA$; $P_{in} = 30\,dBm$).
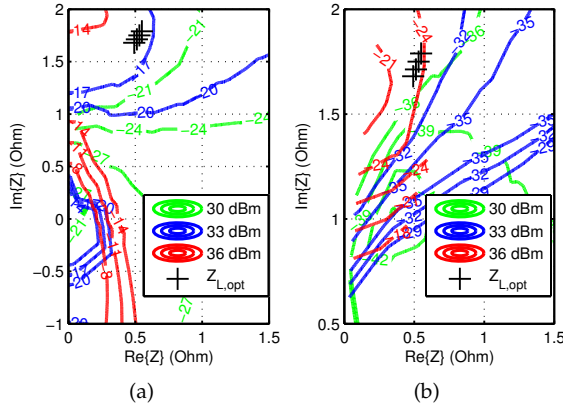
FIGURE 3.14: Simulated (a) IMD3 and (b) IMD5 related load impedances for various power levels ($V_{DS} = 40\,V$; $I_{Dq} = 300\,mA$; $P_{in} = \{30; 33; 36\}\,dBm$).

FIGURE 3.15: Simulated (a) IMD3 and (b) IMD5 related load impedances for various baseband impedances ($V_{DS} = 40\,V$; $I_{Dq} = 300\,mA$; $P_{in} = 30\,dBm$).

see different locations of the IMD spots again. Fig. 3.15(a) displays the dependency of IMD3 related products to a baseband open, short or an inductive load while the previous observations were related to a baseband open. On account of the static increase of the susceptance by the previous analysis it can be noted that an inductive load shows the lowest IMD3s at an impedance of $(1.5+j*1.5\,\Omega)$, while an open leads to a lower susceptance part of $(1+j*0.5\,\Omega)$The IMD5 dependency on the baseband impedance is mainly the same, as the IMD3 dependency and can be seen in Fig. 3.15(b).

What all these spots have in common is that their location is far away from the already obtained optimum impedances related to P_{out} and PAE. Consequently, the influence of IMD related products cannot be taken into consideration for realising matching circuits. However, a change in the quiescent current as well as the baseband impedance during the measurements can result in an improved performance.

Harmonic Load-Pull

Finally, the optimal impedances located at the harmonics will now be considered. The generated harmonics of the device itself can be reflected in a certain manner of phase in order to improve the overall efficiency of the device within saturation (e.g. switch mode amplifier). Rather than simply applying an open at the second and third harmonics, this

reflection ($\Gamma=0.95$) is changed in phase during the next analysis to see the influence on the device's total efficiency.

Fig. 3.16(a) displays the PAE (left axis) as well as P_{out} (right axis) of the device while sweeping the phase angle of the second harmonic ($2 \cdot f_0 = 28\,GHz$) as well as the third harmonic ($3 \cdot f_0 = 42\,GHz$). It can be observed that neither the second nor the third harmonic influences the P_{out}, and as a result the PAE, significantly. Only a drop of 0.25 dB regarding P_{out} as well as 2.5% PAE can be observed by the phase angle of 180°. The influence of the third harmonic to the PAE, is negligible, due to the low transit frequency of $f_T = 40\,GHz$.

The small influence with regard to the phase of the second harmonic can be explained by the size of the horizontal device of this bare-die. As can be seen in Fig. 3.6 the horizontal dimensions of this bare-die is $\geq \frac{3}{4}\lambda_{2 \cdot f_0}$ for the second harmonics. The second harmonics are already reflected towards the intrinsic cells within different phase angles over the n times *transistor cells*. In consequence, an additional reflection during this extrinsic Load-Pull simulation has a minor influence.

(a) CGHV1J070D

(b) CGHV1J006D
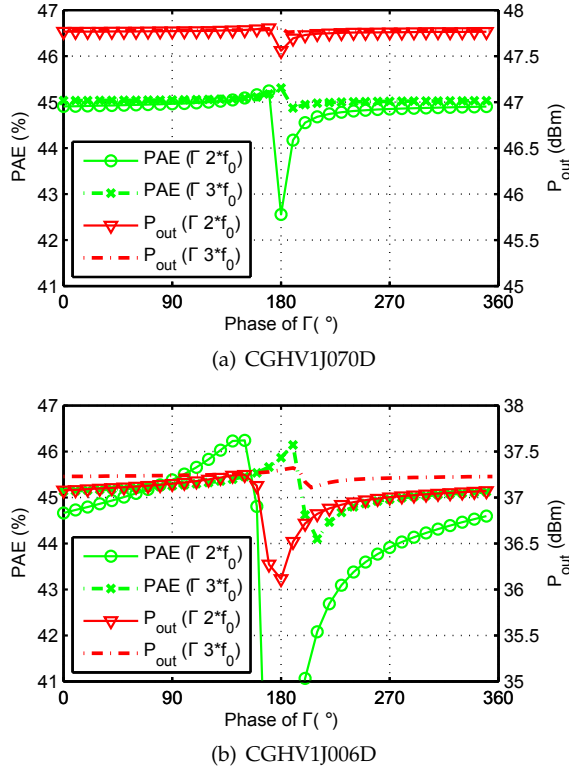
FIGURE 3.16: Simulated phase dependency of second ($2 \cdot f_0 = 28\,\text{GHz}$) and third ($3 \cdot f_0 = 42\,\text{GHz}$) harmonic reflection coefficient $\Gamma=0.95$ on PAE, P_{out} at $f_0=14\,\text{GHz}$ (a) 70 W device (b) 6 W device ($V_{DS} = 40\,\text{V}$; $I_{Dq} = 2\%\ I_{max}$).

This theory is proven by analysing the smaller device CGHV1J006D which represents, through the scaling rules, one *transistor cells*. Its $f_T = 46\,\text{GHz}$ is

only slightly higher but the horizontal dimensions are significantly less than $\frac{\lambda}{4}$ for the second harmonics. The harmonic phase-angle swept Load-Pull analysis can be seen in Fig. 3.16(b). A typical decrease of PAE down to 38% can be observed for the phase angle of 180°. It comes along with a drop in output power of 1 dB. In addition, an influence of the third harmonic phase angle can be observed within the 2% PAE range. One would define a safe phase angle area within 0-150° and 300-360°.

Efficiency Limitations

The described achievements concerning the optimum impedances in relation to frequency represent valuable data only for the port reference plane of the device. Additional losses of the interconnection as well as the matching will further decrease the efficiency of the amplifier. Moreover, this analysis is only representative for the bare-die itself. Packaging the bare-die will lead to an additional package capacitance which decreases f_T as well as f_{MAX} of the transistor. On account of the fact that, the device already barely works at 14 GHz, additional packaging limitations cannot be tolerated, which is why only a shielding of the whole MIC is considered within this work.

3.3 Upper *Ku*-band MIC PA

3.3.1 PA Design Approach

The very low optimum source and load impedances lead to a high impedance transformation ratio of the network of $\frac{50\,\Omega}{0.4\,\Omega} = 125$ at the output. Contrary to that is the need for achieving this transformation ratio over 5% fractional bandwidth (FBW). The previously analysed low power gain of $\approx 6.5\,$dB results in a multi-stage matching approach that can increase the gain to an acceptable level (Fig. 3.17(a)). The necessary driving level of the pre-amplifier (Q1) has been calculated to be $P_{out,drv} \approx 15\,$W. Preliminary analysis has shown that the smaller device with 4.8 mm gate width can hardly reach that level. Additional mismatch constraints, which are unavoidable when matching the output of this smaller device to the input of Q2, will further decrease its level. A previous design realisation showed that a continuous power level of $\geq 12\,$W can be reached in a deep compression [Maa+16a].

Therefore, the same device was chosen for the Q2 as well as Q1 while taking into account the total PAE, like in [Saa+14]. The resulting PAE of the two stages can be calculated with:

$$total\,PAE = \frac{Gain\,Q2 - \frac{1}{Gain\,Q1}}{\left(\frac{Gain\,Q2}{\eta\,Q2}\right) + \left(\frac{1}{\eta\,Q1}\right)} \qquad (3.21)$$

while the derivation is given in Appx.A.79. As can be seen in Fig. 3.17(b), the gain of Q2 needs to stay high in order to achieve a sufficient total PAE of $\geq 30\%$, whereas the drain efficiency of Q1 needs to exceed $\eta\,Q1 \geq 20\%$ (assuming $\eta\,Q2 = 40\%$). The premature power/gain compression of the HEMT device when operated at the high input power levels of Q2 causes additional AM-AM non-linearity [Qua08]. This compression is mainly caused by the gm curve progression. At the analysed frequencies, already exceeding f_{KNEE} ($k \geq 1$), the gm curve is asymmetric with a strong increase from turn-on to gm_{max} (Fig. 3.10(a)). The slow decrease towards $gm = 0\,$S is the reason for a constant compression over P_{in}. The simulations show that

(a)

(b)
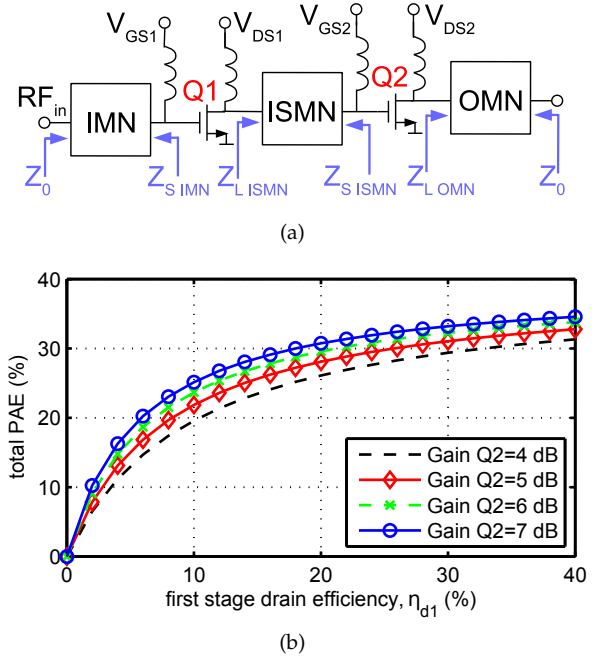
FIGURE 3.17: Proposed (a) two stage PA topology with (b) theoretical total PAE considerations.

this difficult time-dependent AM-AM compression can be compensated by a lower quiescent current of Q2 (Sec. 2.3) and by the type of applied input signal [Ped+14]. On the other hand, the increased AM-PM non-linearity can be compensated via a pre-distortion for modulated signals. Thus, for the design of matching networks, the optimum load impedances for Q2 ($Z_{L\,OMN}$) are chosen within saturation conditions. The load impedances for Q1 ($Z_{L\,ISMN}$) represent the maximum gain with respect to the lower output power level. The input impedances of both transistors Q1, Q2 ($Z_{S\,IMN}, Z_{S\,ISMN}$) should accomplish a flat gain over frequency. A mismatch of the input impedance of Q2 ($Z_{S\,ISMN}$) from the optimum conjugate complex match can help to lower AM-PM non-linearities as shown in [Gio+16].

3.3.2 Design of Matching Networks

The substrate chosen for the matching circuit compromises between low losses and a high ε_r to realise low transmission line impedances, small sizes as well as low radiation losses. Within this design, an intentionally one substrate approach has been used due to manufacturing constraints.

Multiple substrates with different ε_r values are widely used [Kaz+11], [Not+12], [Ima+14] while producing high losses as well as high radiation on account of interconnections, as already shown in Fig. 2.2. The height of the substrate should ideally be close to the bare-die height in order to ease the bonding. For this reason, a thin alumina substrate (Al_2O_3) with a height of $127\,\mu m$ and an $\varepsilon_r = 9.9$ has been chosen as it can take advantage of its extremely low $\tan\delta$. With a layer stack including a resistive $NiCr$-layer, it is possible to produce highly accurate thin film resistors on the substrate. To handle high currents the Au metallization has been grown to a thickness of $10\,\mu m$. All the sub elements have been individually analysed in a schematic as well as a 2.5 D *Momentum*^{TM} simulation to fulfil their specification. Parametrized EM-models of the components have also been created within *Keysight ADS*^{TM}. These models benefit from considering all parasitics while maintaining the ability to change their characteristic parameters, such as their length or width. All sub elements were evaluated based on 3 D *CST*^{TM} simulations taking possible radiation losses into account[1].

Matching

The matching of devices with very low impedances is challenging. By taking their additional trajectories over frequency into account, a broadband matching for the input matching network (IMN) as well as the output matching network (OMN) is almost impossible. Particularly in the interstage matching network (ISMN), the two consecutive stages need to be matched to one another. The required transformation ratio is considerably low but a complex to complex transformation needs to be done with different directions of the imaginary trajectories. Notwithstanding the previous difficulties, a reactively matched design approach has been chosen to compensate the dominant parasitics.

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[1]A more detailed description of the simulation techniques is given in Appx. A.4
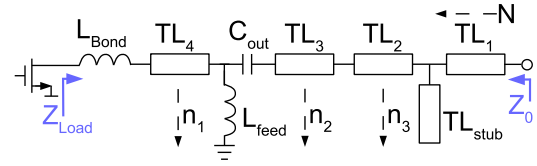
FIGURE 3.18: Schematic of the initial output matching circuit.

Distributed Matching

A matching circuit was developed based on the mechanical and electrical constraints. Taking these constraints into account, an ideal matching network can be designed. The additional parasitic limitations would decrease the obtained results from the ideal matching network towards a real matching network. For this reason, a matching circuit was developed based on lumped elements, taking their Q into consideration. They are connected via transmission line elements (analysed in Sec. 2.1) within a mixed schematic (Fig. 3.18). The drain-source capacitance C_{DS} at the output is resonated out with a shunt inductance L_{feed}. An additional series capacitance has been used to compensate L_{bond}, for further transformation as well as for the ability to block the dc. Ideally, the transistors internal current source can now be seen as a purely resistive impedance. The series line elements (TL_1...TL_4) behave like a stepped impedance transformer starting with a low characteristic impedance from the transistor. An additional open stub (TL_{stub}) has been used in between the last two transforming elements to flatten the filter response. The bandwidth of a stepped impedance transformer is limited by the number of elements (N). The transformation ratio is limited by the values ($Z_{1..N}$). Furthermore, both issues are limited to the lowest possible insertion loss ($N \to 0$) and the lowest realisable line impedance ($Z_{min...N}$). The schematic approach is divided into the following sub elements:

- dc-feed

- Parallel Lines

- Bus Bar

- Interdigital-Capacitor
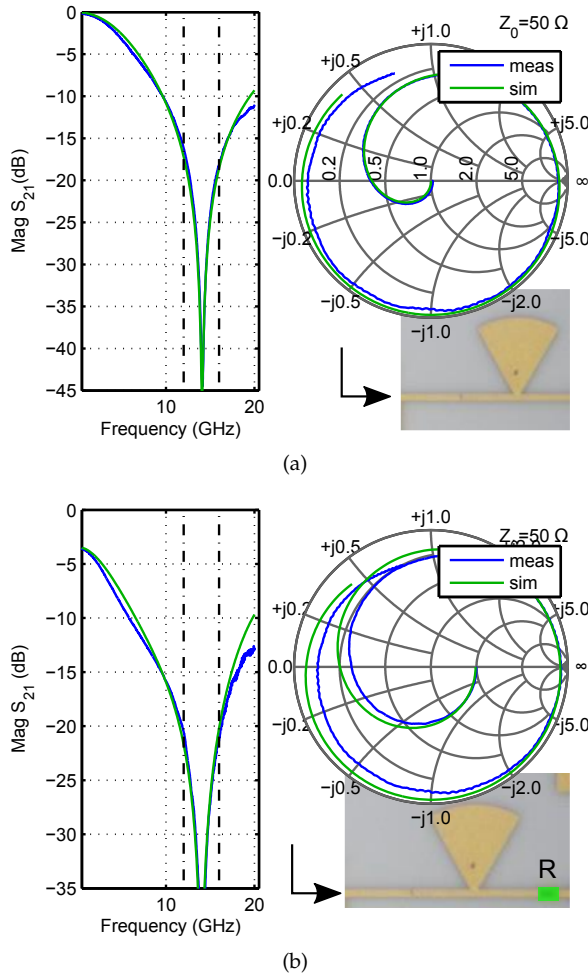
FIGURE 3.19: (a) Measured and simulated radial stub with $\lambda/4$-line line and (b) additional gate resistor.

that need to fulfil the requirements of the subsections.

dc-feed Requirements

For realising a dc-feed, a $\lambda/4$-line with an additional radial stub was designed. As a compromise, the characteristic impedance of the $\lambda/4$-line needs to be low (high width) to be able to transmit the high current at the drain, but preferably high, to realise a high Q of the transformed open over the bandwidth. This dc-feed was designed for both gate and drain supplies. It was produced separately within a test structure, including GSG probe-pads at the RF/dc reference planes. A comparison between probed measured and field-simulated

analysis is shown in Fig. 3.19(a) for the transmission as well as the reflection. The comparison visualizes the high accuracy of the thin film manufacturing process with a sharp rejection at the centre frequency. To ensure stability at the gate-side of the transistor the dc-feed was extended with an additional series resistor $R_{Gate} = 50\,\Omega$ based on the NiCr resistive layer. Thus, the comparison between measurement and simulation in the Smith Chart shows its origin at $100\,\Omega$ with a great match according to the simulation.

Parallel-Lines Requirements

Trying to realise a transmission line with an extremely low characteristic impedance tends to become a parallel plate in microstrip. The width of the microstrip line (w) gets multiple times the height (h) of the substrate which violates Wheelers axiom of microstrip definition. As a result, the current distribution can no longer be approximated by a quasi-TEM microstrip mode. The high width of the bare-die (4.8 mm) leads to a minimum strip width w of the same value. However, this w is more than $\lambda/2$ on the chosen substrate (Fig. 3.6) and may result in a multi-mode propagation. The power distribution over the width of such a wide microstrip line shows different magnitude and phase orientations which disturbs an even-mode propagation. In addition, the resulting characteristic impedance $Z_{min} = 6.5\,\Omega$ is at least 16 times less than the required transformation ratio.

Parallelizing one transmission line to n transmission lines can help to lower the total characteristic impedance. Given that an even-mode occurs at the transmission line, the field distribution of a microstrip line is $\approx n$ times the single one. The resulting distributed transmission lines have to be combined to a one ended line at the $Z_0 = 50\,\Omega$ output over the number of sections N, as can be seen in Fig. 3.21(a). The distance of the twelve parallel pads at the bare-die side is $360\,\mu m$, which results in a centred distance of all twelve parallel microstrip lines to be $360\,\mu m$. Furthermore, the minimum distance of two metallized structures is $50\,\mu m$ according to the substrate design rules. As a result,
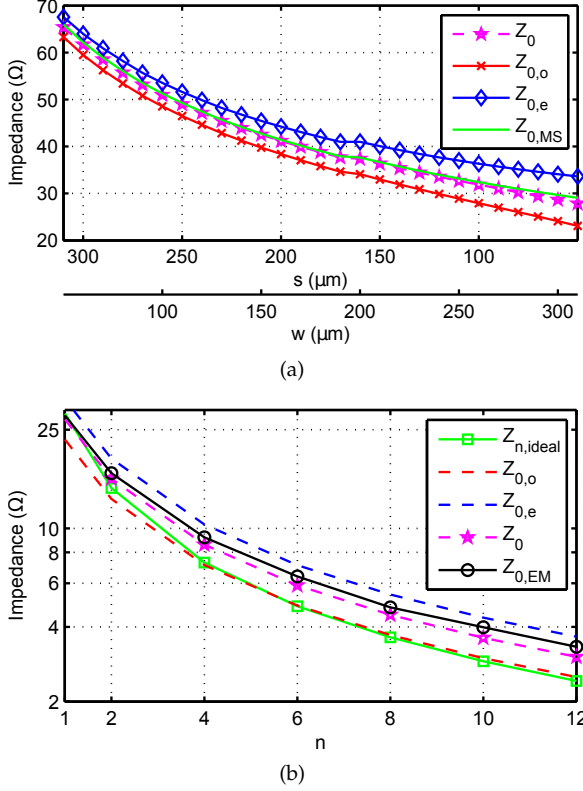
FIGURE 3.20: (a) Calculation of characteristic impedance from two coupled MS lines (b) Calculation of characteristic impedance from n coupled MS lines (each with w=310 μm), both for a Al_2O_3 substrate with 5mil thickness at 14 GHz.

the possible width of one MS line is $\{50 - 310\}\mu m$. Thus, the characteristic impedance of a MS line ($Z_{0,MS}$) can therefore be calculated, as described in Sec. 2.1 and given in Appx. A.38.

The result is that parallel MS lines could not be considered to behave like a single MS line. According to Kirchning [Kir+84], the coupling between two MS lines can be calculated by the definition of an effective dielectric constant of the even-mode propagation ($\varepsilon_{r,eff,e}$), as well as the odd-mode propagation ($\varepsilon_{r,eff,o}$). This analytical calculation is carried out for the width limitations of the MS lines in question and is shown in Fig. 3.20(a) (Appx. A.47). Here $Z_{0,o}$ denotes the odd-mode, $Z_{0,e}$ the even-mode as well as Z_0 the characteristic sum of both. Towards an increased line-width w the distance between both lines s has to decrease to be able to arrange all MS-lines within the $360\,\mu m$ grid. However, the MS based impedance calculation achieves a slightly higher value than the coupled MS lines

calculation due to the coupling (For $w=310\,\mu m$: $Z_{0,MS}$=29.5 Ω; Z_0=27.6 Ω).

Due to the twelve *transistor cells*, parallel lines sections with $n = \{1;\ 3;\ 6;\ 12\}$ over $N = 4$ were chosen. A first approximation of the transmission line (TL) parameter can be done by simply dividing the characteristic impedance by the number of parallel lines.

$$Z_{n,ideal} = \frac{Z_{n,distri}}{n}; \qquad \Phi_{n,ideal} = \Phi_{n,distri} \qquad (3.22)$$

Nevertheless, the coupling in between all MS lines cannot be neglected, so the parallel structure was analysed based on EM-simulations. The comparison is shown in Fig. 3.20(a) and visualizes that n parallel lines lowered the equivalent Impedance both in the EM-simulation ($Z_{0,EM}$), as well as in the simple approach ($Z_{n,ideal}$), but towards an increased n the values differ up to a factor of 2. Up to now no analytical solution to this problem has been found in the literature. Consequently, the quasi static analytical calculations of [Kir+84] for two parallel lines are:

$$Z_{0,e} = Z_0 \sqrt{\frac{\varepsilon_{r,eff}}{\varepsilon_{r,eff,e}}} \frac{1}{(1 - (Z_0/377)(\varepsilon_{r,eff})^{0.5}\,Q_4)} \tag{3.23}$$

$$Z_{0,o} = Z_0 \sqrt{\frac{\varepsilon_{r,eff}}{\varepsilon_{r,eff,o}}} \frac{1}{(1 - (Z_0/377)(\varepsilon_{r,eff})^{0.5}\,Q_{10})} \tag{3.24}$$

and they were extended to n parallel lines with the assumption that the effect of the coupling decreases with an increase of n by a simple quadratic polynom:

$$n_{fit} = -8.919e^{-4}n^2 + 0.804\,n + 0.2174 \qquad (3.25)$$

to result in:

$$Z_{0,en} = Z_{0,e}\,n_{fit}^{-1} \qquad (3.26)$$

$$Z_{0,on} = Z_{0,o}\,n_{fit}^{-1} \qquad (3.27)$$

The complete analytical calculation is given in Appx. A.47. This polynomial correction is stated on extensive 2.5-D as well as 3-D field simulations
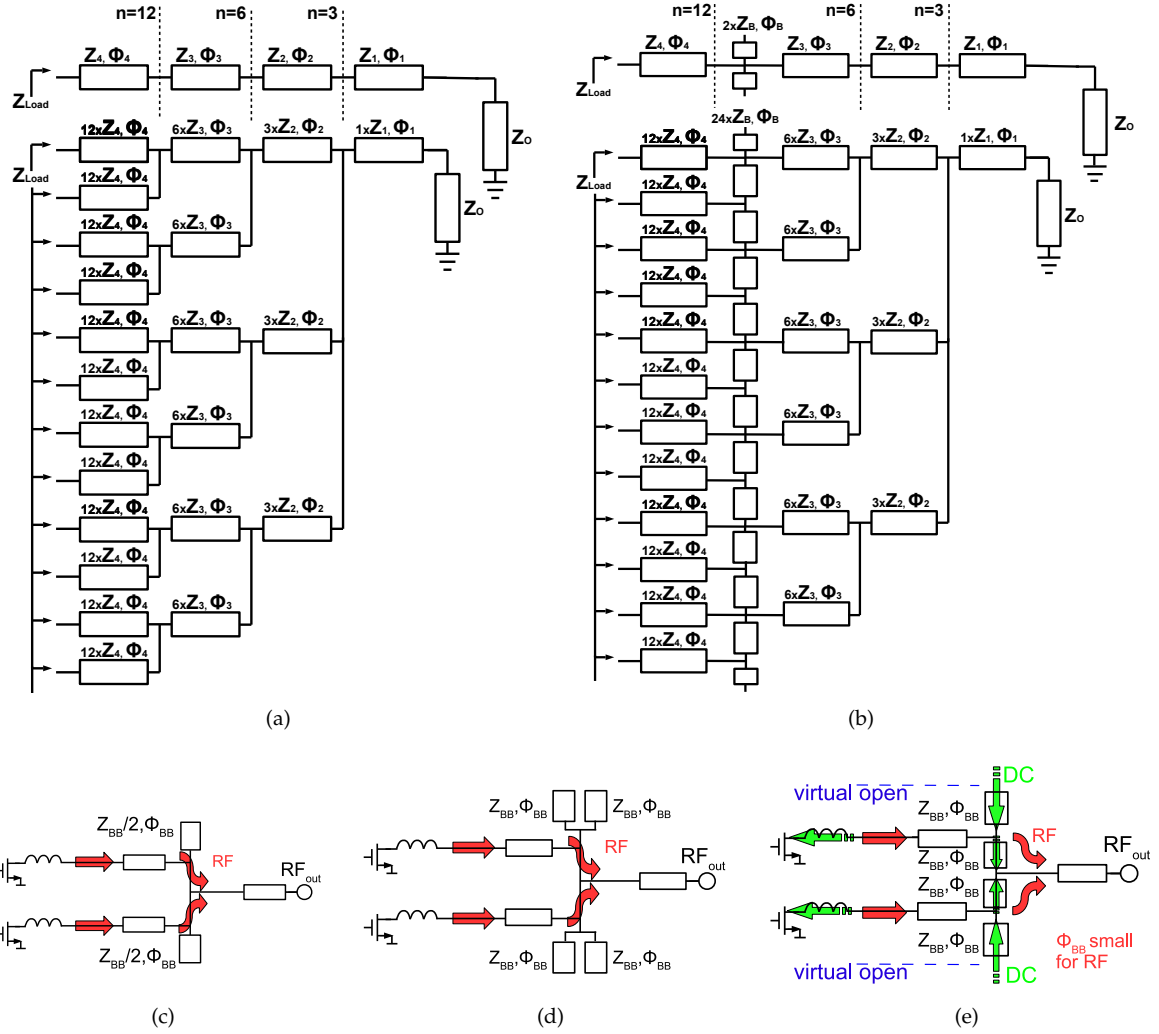
FIGURE 3.21: (a) Schematic visualisation of the parallel MS-line concept with (b) added a Bus Bar in between. Step by step visualisation of the *virtual open* in a Bus Bar. Starting with an open stub (c), double open stub (d) resulting in interconnected symmetrical stubs (e).

and is shown in Fig. 3.20(b) as well. A comparison of the measurements cannot be given here because n parallel lines cannot be easily measured within an even-mode propagation. The new analytical approximation Z_0 fits very well with the EM simulated structure ($Z_{0,EM}$) and denotes that equivalent characteristic impedance values of down to $Z_0 = 3\,\Omega$ are realisable. The calculation of the characteristic impedances of the sections $n = \{1;\ 3;\ 6\}$ is simpler due to the higher distance s of the MS lines and in consequence a weaker coupling (Fig. 3.21(a)).

Bus Bar Requirements

For providing an equal dc distribution to all transistor cells, while not destroying the even-mode propagation over the distributed transmission-line combiner, the Bus Bar principle was introduced by Marsh [Mar97]. In Fig. 3.21(c), a T-junction shows a proper RF isolation between two branches while working in an even-mode. It is self evident, that the RF propagation stays the same when splitting the two open stubs into four, keeping their sum of impedances constant (Fig. 3.21(d)). While maintaining a symmetrical network like in Fig. 3.21(e), it is possible to connect two of the open stubs at their end, as long as their electrical length (Φ_{BB}) is much

less than $\lambda/4$. As a result, a bar is built which alternately provides a virtual open and a combining sink. This concept enables the provision of a dc current to all transistor cells via a wide bar while maintaining RF isolation in between them by the resulting *virtual open*. Consequently, the bar is added to the combining circuit of Fig. 3.21(a), resulting in an eased combining in Fig. 3.21(b) due to the inserted odd-mode sink along the Bus Bar. This principle is limited to a FBW of $\approx 15\%$ [Mar+99]. For an increased FBW the virtual open combining planes can be capacitively loaded to ensure a higher isolation.

Interdigital-Capacitor Requirements

Within this design, all capacitors (C_{imn}, C_{ismn}, C_{omn}) were realised by Interdigital capacitors on the substrate. By using $n = 6$ Interdigital capacitors in parallel, the total series capacitance was increased. The finger width and spacing are set to $50\,\mu m$ according to manufacturing constraints. Lumped element models have been developed and verified by electro magnetic (EM) simulations. Fig. 3.22(a) depicts a comparison between the simulated and measured results for one single input capacitor ($\frac{C_{imn}}{n}$) as well as the behaviour of the equivalent model (Fig. 3.22(b)). The values for the equivalent model are $C_s = 0.06\,\mathrm{pF}$, $C_p = 0.11\,\mathrm{pF}$ and $L_s = 0.14\,\mathrm{nH}$ for the finger length $L_f = 0.2\,\mathrm{mm}$ and width $W_f = 50\,\mu m$ as well as a distance $W_{gap} = 50\,\mu m$ in between this structure. Even though, the parallel capacitance (C_p) is about twice as high as series one (C_s), the capacitors are utilized as complex matching elements. The SRF is kept high, in this case above $20\,\mathrm{GHz}$, to achieve an almost constant effective capacitance within the desired frequency range (Fig. 3.22(a)). As a result, possible deviations between simulation and realisation due to manufacturing tolerances can be minimized. Nevertheless, their $Q \approx 40$ is rather low, further decreasing with frequency. The Interdigital capacitors with their RF series resistance build a high-pass filter which reduces possible low frequency oscillations at the input side of the transistor.
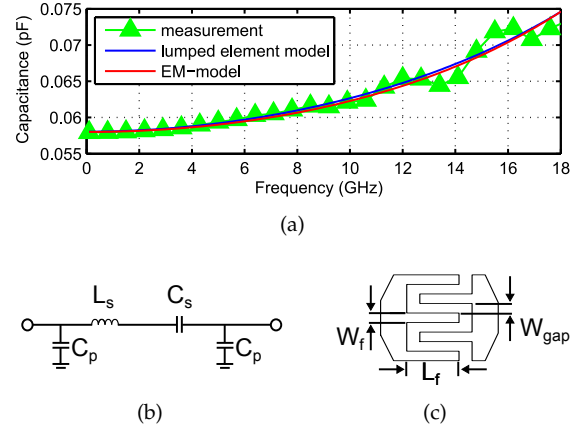
FIGURE 3.22: Measured and simulated capacitance (a) lumped equivalent model (b) and layout (c) of Interdigital capacitor.

3.3.3 Simulation Approach

Small-Signal Analysis

The matching networks were developed based on parametrized EM-models of the previously described sub-elements. Its objective was to realise the required optimum source- and load-impedances that were previously identified by the Source- and Load-Pull-simulations. During the small-signal simulation of the matching networks the ports were loaded with the conjugate optimum Load-Pull impedances, representing a large-signal match. The resulting schematic is given in Fig. 3.23(a) with its characteristic values of the elements shown in Tab. 3.4. The EM-based simulated impedances from 13.75-14.5 GHz for the input ($Z_{S\,IMN,realised}$, $Z_{S\,ISMN,realised}$) are shown in Fig. 3.23(b). For the output side of the transistor the impedances ($Z_{L\,ISMN,realised}$, $Z_{L\,OMN,realised}$) are shown in Fig. 3.23(c). Furthermore, multi frequency Source- and Load-Pull contours (MuFLoC) are plotted considering the output power as well as the PAE. The contours represent the minimum values of all frequency-dependent data in between 13.75-14.5 GHz - and so represent valuable in-band performance data, as described in section 3.2.2. It can be seen that the input of the first stage (IMN Q1) as well as the second stage (ISMN Q2) are well-matched to the optimum impedances
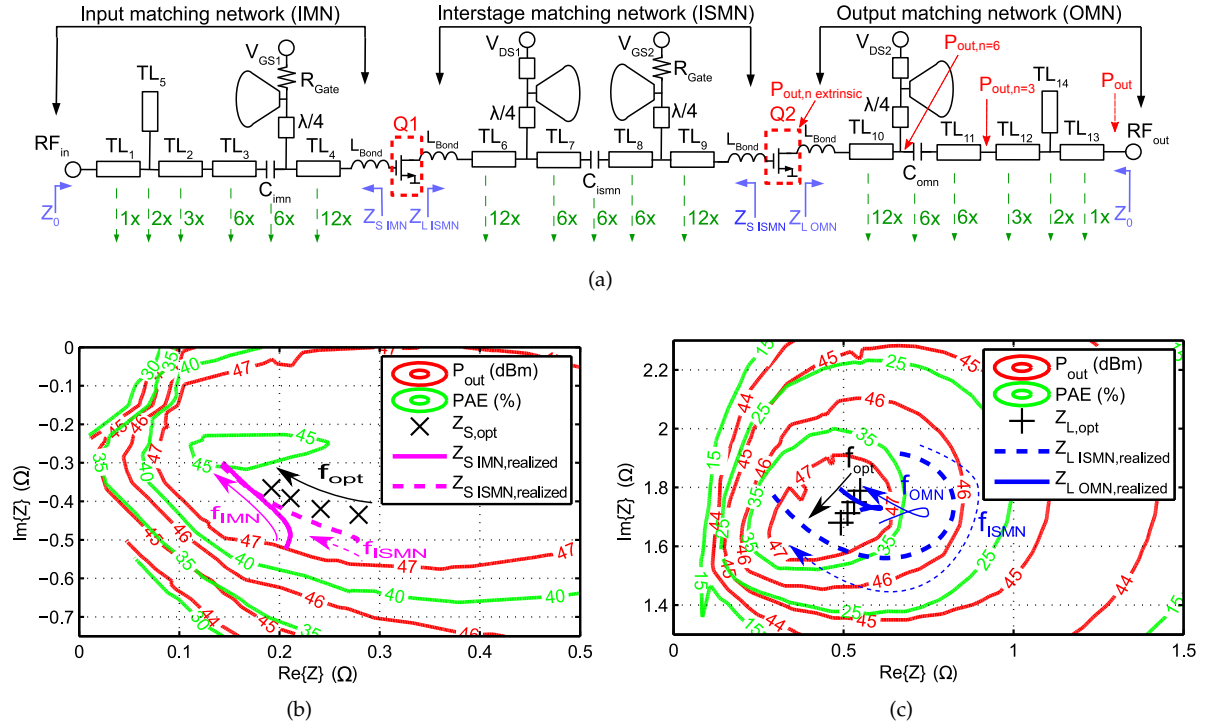
FIGURE 3.23: (a) Schematic of the proposed two-stage amplifier divided into three matching circuits (IMN, ISMN, OMN). Each transmission line (TL) is parallelised by n-times written underneath in green. Simulated EM-based impedances realised by the matching circuits within F_{up} for the input sides of Q1 (IMN) and Q2 (ISMN) (b) and for the output sides of Q1 (ISMN) and Q2 (OMN) (c). The plotted multi-frequency Load- and Source-pull contours (MuFLoC) represent the minimum value over the desired frequency range F_{up}.

($Z_{S,opt}$). The direction of the imaginary part is particularly the same. For the output side, much more attention was paid to achieve a high Q transformation for the output of (Q2). Consequently, the realised impedances are inside the $P_{out} = 47\,$dBm contour. The high PAE sensitivity should be noted, changing from $\geq 35\%$ for the inner circle within 10% down to 25% only by changing the load-impedance $0.5\,\Omega$. Within the ISMN the trajectories of the load and generator impedances travel in opposite directions over frequency, which is why the realised matching is a compromise. All three matching circuits are able to provide a matching $\geq 15\,$dB towards their opposite impedance.

An additional Monte-Carlo analysis takes the tolerances of Tab. 3.2 into account. Here a small-signal transmission of up to 23 dB for F_{up} can be seen in (Fig. 3.24(a)). The additional bond tolerances influence both stages, including the IMN, twice the ISMN as well as the OMN. Therefore, the S-Parameter changes in Fig. 3.24(a) need to be tolerated. The IMN, ISMN as well as OMN were

TABLE 3.4: Schematic values of the proposed two-stage amplifier for $f_0 = 14\,$GHz

IMN $\parallel$	TL$_1$	TL$_2$	TL$_3$	TL$_4$	TL$_5$
Φ	106°	111°	29°	41°	31°
Z_{TL}	50 Ω	14 Ω	3.6 Ω	2.3 Ω	25 Ω
Z_{TL} x n	50 Ω	42 Ω	21.6 Ω	27.6 Ω	50 Ω
$C_{imn} = 0.4\,$pF		$R_{Gate} = 50\,\Omega$		$L_{Bond} = 12.5\,$pH	

ISMN $\parallel$	TL$_6$	TL$_7$	TL$_8$	TL$_9$	
Φ	45°	5°	7°	37°	
Z_{TL}	2.9 Ω	6 Ω	6.6 Ω	2.25 Ω	
Z_{TL} x n	34.8 Ω	36 Ω	39.6 Ω	27 Ω	
$C_{ismn} = 0.282\,$pF		$R_{Gate} = 50\,\Omega$		$L_{Bond} = 12.5\,$pH	

OMN $\parallel$	TL$_{10}$	TL$_{11}$	TL$_{12}$	TL$_{13}$	TL$_{14}$
Φ	35°	25°	113°	104°	22°
Z_{TL}	2.25 Ω	4.6 Ω	13.3 Ω	50 Ω	25 Ω
Z_{TL} x n	26.4 Ω	27.6 Ω	26.6 Ω	50 Ω	50 Ω
$C_{omn} = 0.498\,$pF		$L_{Bond} = 12.5\,$pH			

analysed as combining circuits (1 to n) as well. The theoretical insertion loss of a real to real 1 to n combiner can be defined as follows:

$$IL = 10 \cdot log\frac{1}{n} \qquad (3.28)$$

(a)

(b)
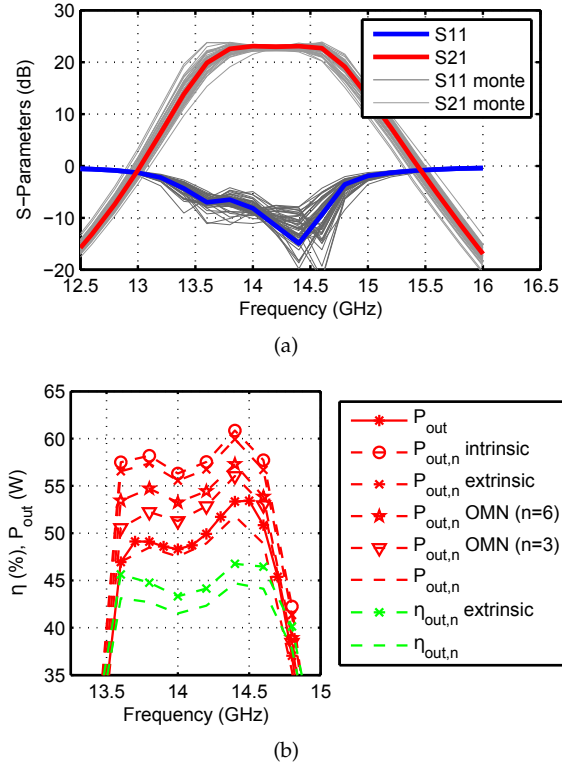
FIGURE 3.24: (a) Simulated small-signal (b) large-signal behaviour of the amplifier ($V_{DS1,2} = 40$ V; $I_{Dq1,2} = 300$ mA).

for $n = 12$ which represents the IMN as well as the OMN combiner the losses are:

$$IL = 10 \cdot log \frac{1}{12} = 10.79 \, dB \qquad (3.29)$$

Within the EM-simulation the IL of all n sections was -11.5 dB with ± 0.5 dB amplitude imbalance. The isolation of the Bus Bar can be depicted to be in the range of 7 dB. This way the phase difference between all branches is $\pm 3°$ with an increase towards higher frequencies, as can be seen further on in Fig. 3.25.

Large-Signal Analysis

During a large-signal analysis, power as well as frequency is swept using a *Harmonic Balance* Analysis. Special attention was given to the temperature of the junction so as not to exceed the theoretical cooling constraints during the simulation. The sensitive gate current was also monitored. The simulated output power of the amplifier (P_{out}) is shown in Fig. 3.24(b) using the normal large-signal

model of the device. Here, an output power level ≥ 50 W can be obtained over F_{up}. Each n *transistor cells* was modelled separately and de-embedded to its intrinsic current source. It was therefore possible to simulate the output power of all n intrinsic current sources described as ($P_{out,n}$ intrinsic). It can be obtained that the intrinsic power level is ≈ 10 W higher than the output power level of the amplifier (P_{out}). To determine the dependency of these losses, simulations were carried out at various positions within the OMN (compare Fig. 3.23(a)) where ($P_{out,n}$ extrinsic) is the extrinsic output reference plane of the device, ($P_{out,n}$ OMN (n=6)) is the reference plane where $n = 6$ lines are in parallel and ($P_{out,n}$ OMN (n=3)) is the reference plane where $n = 3$ lines are in parallel. According to these simulations (Fig. 3.24(b)), the losses of the OMN increases towards the output of the amplifier. The total losses of the OMN ($\alpha_c, \alpha_d, \alpha_r$) are in the range of 5 W according to the difference of ($P_{out,n}$ extrinsic) to ($P_{out,n}$). Based on this analysis the drain efficiency of this second stage ($Q2$) can be compared between the extrinsic reference plane ($\eta_{out,n}$ extrinsic) and the output of the amplifier ($\eta_{out,n}$) with a difference of only 3%. The achieved extrinsic efficiency ($\eta_{out,n}$ extrinsic) is nearly the maximum available drain-efficiency simulated within the Load-Pull analysis (Tab. 3.3) which indicates a great matching.

The magnitude and phase imbalance of all *transistor cells* can be analysed and are shown in Fig. 3.25. A phase-imbalance of the combiner can be observed that may be improved by changing the inner bond-wires. This can also be seen within the sum of all intrinsic powers within Fig. 3.24(b), where the distributed simulation approach degrades in power ($P_{out,n}$) towards higher frequencies, while the power (P_{out}) of the one transistor approach increases.

In addition, intrinsic load-line simulations of each *transistor cell* (Q2.1...Q2.12) were carried out, visualising a saturated amplifier (Fig. 3.26(a)). The load-lines indicate a typical **Class-AB** response with an oval shape towards a line - spanning a lower amount of area than a **Class-A** curve which
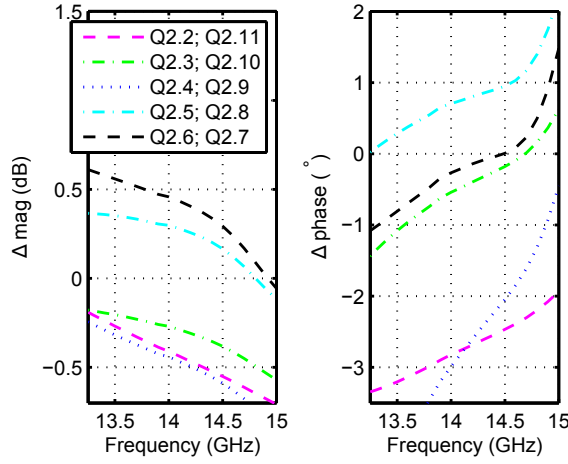
FIGURE 3.25: Simulated (left) magnitude imbalance (right) phase imbalance of the *transistor cells* referenced to (Q2.1...Q2.12).

improves efficiency. The power distribution between the *transistor cells* as well as leakage currents were analysed. From Fig. 3.26(b) a good distribution between the twelve cells can be noticed. The outer ones (Q2.1; Q2.12) provide the most RF-power to the matching circuit, due to their lower baseplate temperature and the reduced combining parasitics. Nevertheless, a slightly earlier degradation of the power towards higher frequencies can be observed for the inner transistor cells (Q2.5...Q2.8). The combiner efficiency (η_c) can be calculated to be $\geq 83\%$ for the relation between the output power (P_{out}) and the sum of all distributed extrinsic *transistor cells* [Gup92]:

$$P_{out} = \eta_c \sum_{i=1}^{n} P_{out, Q2.n} \, \text{extrinsic} \qquad (3.30)$$

Large-Signal Stability

Given that the designed amplifier is a multi - stage circuit, the stability calculations could not be done using classical K-factor analysis [Rol62]. Stability has therefore been proven in a large-signal analysis by the *STAN^{TM}-Tool* [Del+12]. By applying this approach, additional odd - mode signals were injected to all gates, drains and dc - connections of the 24 *transistor cells*. By calculating the large-signal transfer function of the amplifier, a pole zero analysis was performed. In Fig. 3.27(a) a stable operation can be seen as an example for an

inserted odd mode excitation at one certain port over various power levels within the ISMN. Unstable poles (in red arrows) can be determined, located at the same point as right-half-plane (RHP) zeros for the maximum injected power. After additional analysis they can be ignored as physical quasi-cancellation occurring from the low sensitivity in the interstage matching circuit [Del+12]. The same technique is applied for injecting power in the OMN (Fig. 3.27(b)). This means the injected power must be increased regarding the higher power level of Q2. Despite this, no oscillation was obtained.

Analysis with modulated Signals

The large signal simulation of the two stage amplifier can be used to prove its linearity within a *ADS/System Vue^{TM}* co-simulation. A QPSK-signal with 4 MSym/s at 14 GHz is generated. The signal is applied to the two-stage amplifier considering the different baseband impedances of the dc-feed while holding the output power constant at $P_{out, avg} = 30$ W. As can be seen in Fig. 3.28(a), a short slightly improves the shoulders of the output spectrum that are related to the IMD3 products[2]. Apart from that, the quiescent current of the stages {Q1/Q2} is varied to prevent IMDs that are related to AM/AM or AM/PM compression products. According to Fig. 3.28(b) the quiescent current of Q2 can be decreased to 50 mA while holding the current of Q1 at 300 mA with the best ACPR performance (cyan).

3.3.4 Realisation

The bare-dies and substrates were aligned and mounted on a thick CuMoCu-flange (Fig. 3.29(a)). All wedge-wedge bond-wire interconnections were automatically placed. A top view of the mounted MIC can be seen in (Fig. 3.29(b)). The die-attach was analysed via X-Ray microscopy (Fig. 3.29(c), 3.29(d)). The few bright dots are tiny air-inclusions.

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[2]The Bandwidth of the baseband termination is larger than the modulation bandwidth

(a)

(b)
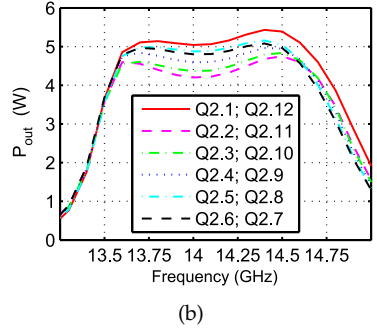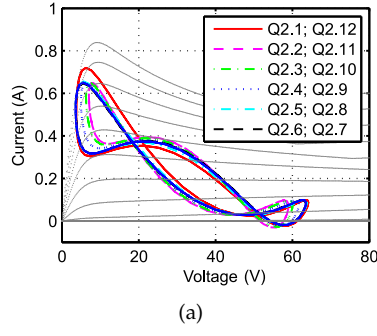
FIGURE 3.26: Simulated intrinsic load-lines (a) and power distribution over power bar (b).
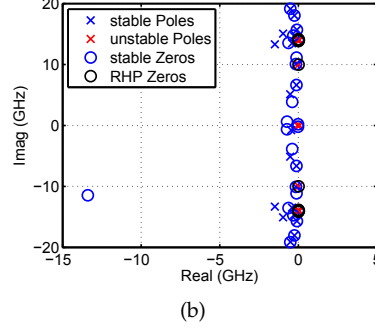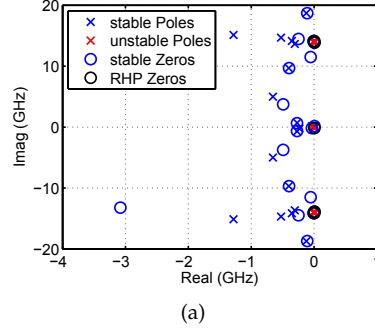
FIGURE 3.27: Example of an analysed amplifier large-signal transfer function by the *STAN^{TM}-Tool* for an odd mode injection in the (a) ISMN, (b) OMN.
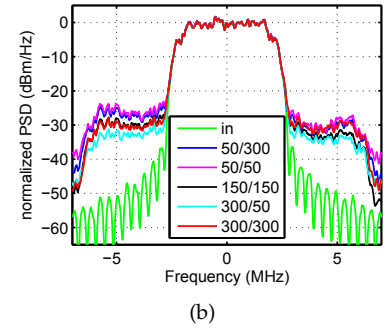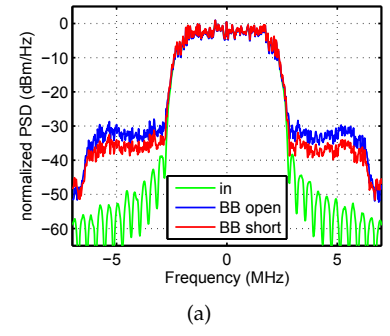
FIGURE 3.28: Simulated output spectrum with different (a) baseband impedance (b) biasing conditions (QPSK 4 MSyms; 14 GHz; $P_{out,avg} = 30$ W).

This pallet was later on positioned in a surrounding aluminium water cooled fixture. On top of this a $203\,\mu m$ thick bolted RO4003c substrate supplies all dc-potentials as well as the RF_{in}, RF_{out} signals to SMA-connectors (Fig. 3.31). Within this fixture the pallet can be measured on a alumina reference plane (Ref_{GSG}) via GSG-probes as well as at the SMA reference plane (Ref_{SMA}).

3.3.5 Measurement Results

Small-Signal Measurements

Probed small-signal measurements were carried out with $500\,\mu m$ pitch probes (|Z|-Probe^{TM}) on the alumina reference-plane (Ref_{GSG}) using a network analyser (N5230A). An additional 2nd tier thru-reflect-line calibration (TRL) de-embeds the ground-signal-ground-pads (GSG). In Fig. 3.30 (top) a very good agreement between simulation and measurement can be seen. Only a slight frequency shift occurs as a result of the bond-wire

tolerances. Six samples (#1 ... #6) were manufactured and compared within small-signal conditions in Fig. 3.30 (bottom). All show a slightly different behaviour with respect to the frequency, as well as the amplitude. Nevertheless, the aim to produce working samples within the specified frequency range of F_{up} {13.75 - 14.5 GHz} has been achieved.

Large-Signal Measurements

Large-signal measurements in the *Ku*-band suffer from high losses and in consequence high measurement uncertainties. To lower the losses and enhance the accuracy, a measurement setup based on high directivity WR75 waveguide-couplers (ATM) was used. The CW input is generated with a microwave synthesized source (E8254A) and boosted with a first pre-amplifier (ZVE-3W-183+) as well as a second one (previously developed [Maa+16a]) (Fig. 3.31) to be able to put the DUT in saturation. The input and output power levels of the DUT were measured with a power meter (E4412). A

(a)

(b)
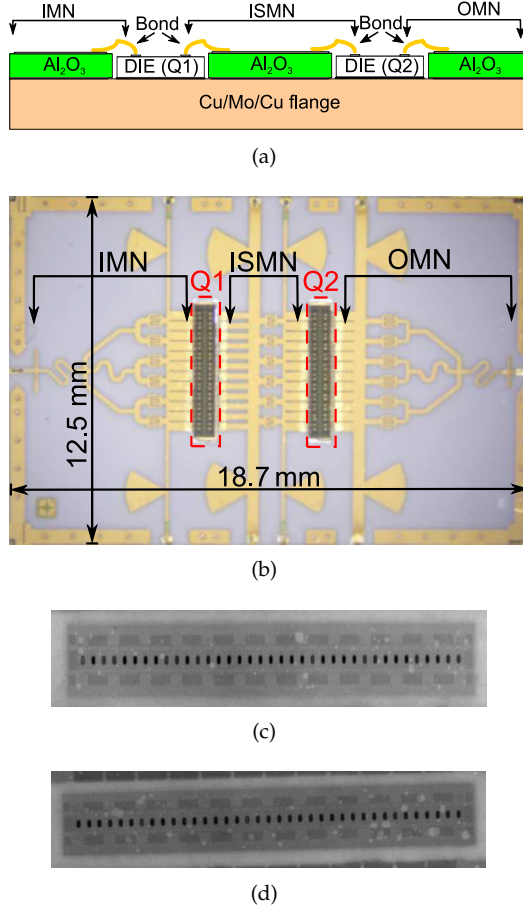
FIGURE 3.29: Realisation of the amplifier. Side-view illustration of the MIC (a). Top view of the MIC (b). X-Ray pictures of the bare-die Q1 (c), Q2 (d).

(a)

(b)

FIGURE 3.30: Comparison between measured (sample #1) and simulated small-signal behaviour of the amplifier ($V_{DS1,2} = 40$ V; $I_{Dq1,2} = 300$ mA) (a). Comparison between six measured amplifiers within small-signal condition ($V_{DS1,2} = 40$ V; $I_{Dq1,2} = 300$ mA) (b).
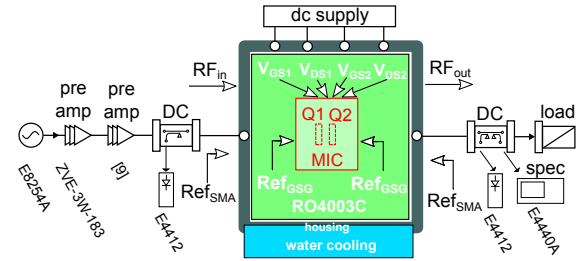
FIGURE 3.31: Large-Signal measurement setup.

non flat pre-amplification is compensated by a *Matlab*^{TM} controlled measurement system to hold the DUT in a reproducible thermal compression. Both gate currents were monitored separately to indicate the compression level. Automatic short intermissions were used in the measurement setup to lower thermal self heating. The setup was calibrated to the SMA reference plane Ref$_{SMA}$. Afterwards, the results were de-embedded to Ref$_{GSG}$ based on the known offset from the small signal measurements (Section 3.3.5).

The PA is characterised versus input power for all frequencies between 13.5-14.6 GHz within a dynamic range of 24 dB. From Fig. 3.32 it can be observed that the compression behaviour of the measurement is equal to the simulation for 14.2 GHz. A constant decrease in gain for the **Class-AB** behaviour needs to be stated. With a **Class-C** biasing the gain could have been lowered down to 15 dB

in the back-off while afterwards remaining constant up to P$_{sat}$. The output power reaches 47 dBm about 1 dB later than in simulation. The gain is compressed to 14 dB in the saturation, like in the simulation. The PAE of the two stages is 5% less than simulated but reaches up to 25%. This dependency can be explained by the device's self heating, which is higher than initially simulated.

By either increasing the R$_{th}$ of the model, or the base temperature, the higher self heating in the measurement can be explained. Moreover, this is proven by thermal images shown in Sec. 3.3.5. The six manufactured amplifiers were measured in their large-signal behaviour. They all demonstrate an equal peak output power with respect to the frequency shift seen in Fig. 3.30 (bottom). In Fig. 3.33 a reasonable agreement between simulation and
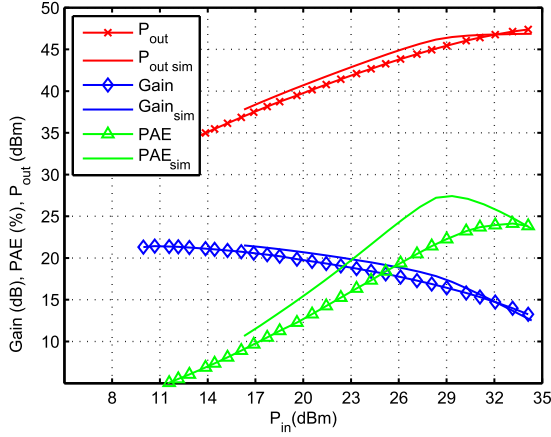
FIGURE 3.32: Comparison between measured and simulated large-signal behaviour of the two-stage amplifier. Power-sweep at 14.2 GHz ($V_{DS1,2} = 40$ V; $I_{Dq1,2} = 300$ mA).
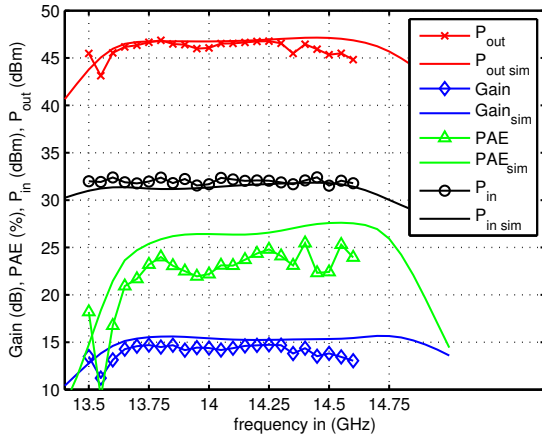
FIGURE 3.33: Comparison between measured and simulated large-signal behaviour over frequency ($V_{DS1,2} = 40$ V; $I_{Dq1,2} = 300$ mA).

measurement can be noted over frequency. The ripple in the frequency range of interest is ± 0.6 dB.

Thermal Analysis

A thermal imaging of the fixture was taken during a CW-measurement in the dark to monitor the surface temperature of the bare-die. The surface reflection coefficients (ε_{IR}) for IR light vary over the different materials. With a constant temperature of a heated up fixture, the bare-die coefficient on top of the passivation was analysed to be $\varepsilon_{IR(Die)} = 0.34$ and the flange $\varepsilon_{IR(flange)} = 0.5$. The thermal difference between the surface of the Si passivation and the channel itself is $\Delta_{T,pCH}(V) \approx 40\text{-}60$ K.

(a)   (b)
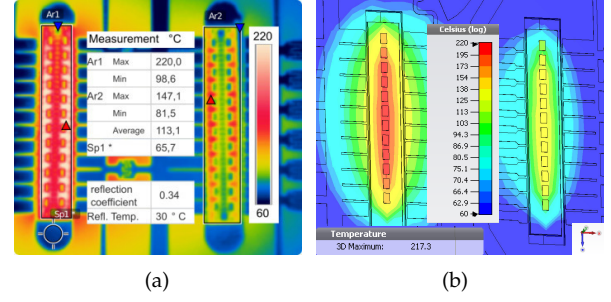
FIGURE 3.34: Comparison between measured (a) and simulated (b) thermal behaviour ($V_{DS1,2} = 40$ V; $I_{Dq1,2} = 300$ mA; $P_{out,avg} = 40$ W).

From Fig. 3.34 the channel temperature can be calculated for $P_{out} = 40$ W to $T_{CH,avg} \approx 228°$C with $T_{CH,peak} \approx 280°$C. The total thermal resistance of the junction to the sink can be calculated to:

$$R_{\Delta JS} = \frac{T_{CH} - T_{flange}}{P_{dc} - P_{RF}} = \frac{228°\text{C} - 24°\text{C}}{176\,\text{W} - 40\,\text{W}} = 1.5\,\frac{\text{K}}{\text{W}}$$
(3.31)

The thermal measurement is in a good agreement with the finite element method (FEM) thermal simulation based on CST^{TM} from Fig. 3.34(b). Nevertheless, the thermal conductivity of the mounting is too low for higher output power levels. For $P_{diss} \geq 80$ W a self heating occurs within the CW measurement. To achieve lower thermal resistances, modern mounting technologies with plated diamond [Han+15] as well as silver sintering [Baj+15] can be used in future work.

Modulated Measurements

The parameters previously analysed in CW excitation, like P_{sat} or P_{1dB}, are insufficient for describing the non-linear behaviour of an amplifier for operations in multi-carrier modes. This is why, AM-AM as well as AM-PM conversion, were chosen as the first set of valuable performance data. Compared to TWTAs, the premature gain compression of the GaN-HEMT is a highly non-linear behaviour (compare Fig.3.32). Within this work, effort has been made to compensate this compression simply through the biasing. For applying a gate voltage to the power amplifier Q2 in deep **Class-AB** $I_{Dq2} = 50$ mA instead of $I_{Dq2} = 300$ mA while holding the pre-amplifier Q1 in the biasing conditions
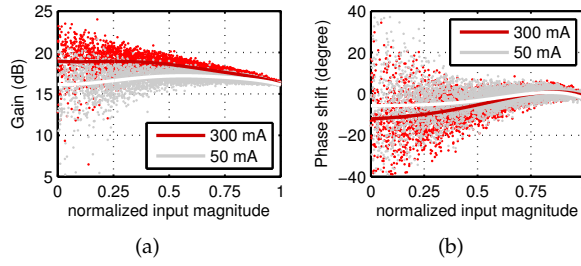
FIGURE 3.35: Measured gain compression (a) and AM-PM conversion (b) with a 32APSK modulation ($\alpha = 0.25$; 16 MSym/s) at an un-linearised amplifier for 14.25 GHz. ($V_{DS1,2} = 40$ V; $I_{Dq1} = 300$ mA; $I_{Dq2} = \{300; 50\}$ mA).
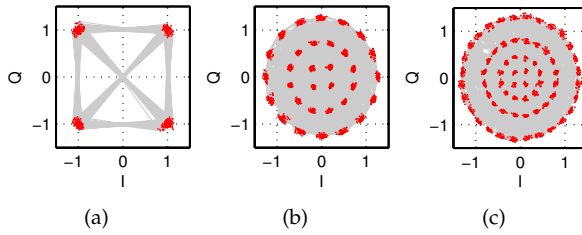
FIGURE 3.36: Measured modulation schemes of common SatCom signals for $P_{out,peak}$-PAPR, 14.25 GHz. (a) QPSK ($\alpha = 0.35$; 16 MSym/s; DVB-S1) (b) 32APSK ($\alpha = 0.25$; 16 MSym/s; DVB-S2) (c) 64APSK ($\alpha = 0.05$; 16 MSym/s; DVB-S2X).

of max gm ($I_{Dq1} = 300$ mA) results in a lowered small-signal gain (Fig. 3.35(a)). This AM-AM and AM-PM analysis were carried out with modulated signals to lower errors of a thermal self-heating. In Fig. 3.35(b) it can be noticed that this biasing also linearises the AM-PM conversion to a lower phase variation, the maximum can be depicted with 1.6° / dB. Additionally to AM-AM and AM-PM conversion the spectrum regrowth, measured by the adjacent channel power ratio (ACPR), is an important indicator of a linear amplifier operation. Furthermore, the error vector magnitude (EVM) is a comprehensive measure of the quality of the transmitter. A QPSK modulation with a peak to average power ratio (PAPR) of 3.9 dB and a roll-off factor $\alpha = 0.35$ was chosen to represent the classical DVB-S signal (Fig.3.36(a)). The increasing demand of data leads to higher order modulation schemes (up to 32APSK) that were defined in the DVB-S2 standard (Fig.3.36(b) PAPR = 5.6). Additionally, the roll-off factor was lowered to $\alpha = 0.25$ to enhance the spectral efficiency. The newly defined DVB-S2X standard allows modulation schemes
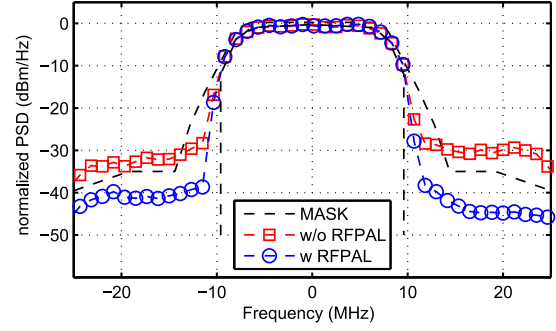
FIGURE 3.37: Output spectrum of the PA for $P_{out,avg} = 30$ W and a QPSK signal with 16 MSym/s; $\alpha = 0.35$ (w) and (w/o) a RFPAL at 14.375 GHz ($V_{DS1,2} = 40$ V; $I_{Dq1} = 300$ mA; $I_{Dq2} = 50$ mA; RBW = 200 kHz; RMS; VBW = 10 MHz; 300 ms sweep; 100 MHz span).

up to 256APSK with a sharp roll-off factor down to $\alpha = 0.05$. The decreased α particularly leads to high PAPR of up to 6.42 dB for a 64APSK with $\alpha = 0.05$ (Fig.3.36(c)). The spectral mask depends on the signal bandwidth and is defined in the ETSI standard [Eut]. Linearisation was performed with a digital pre-distortion (DPD) that was able to reduce the out-of-band energy and enhances the efficiency by compensating non-linearities like AM-AM, AM-PM as well as memory effects. As an alternative an IF pre-distortion directly in the block up-converter (BUC) path was used by the method described in [Maa+15a] called RF PA linearisation (RFPAL) that is explained later on in Sec. 4.3. Both techniques show equal performance levels and can be used either in the BUC (RFPAL) or in the modulator (DPD).

In Fig. 3.37 the resulting output spectrum of the
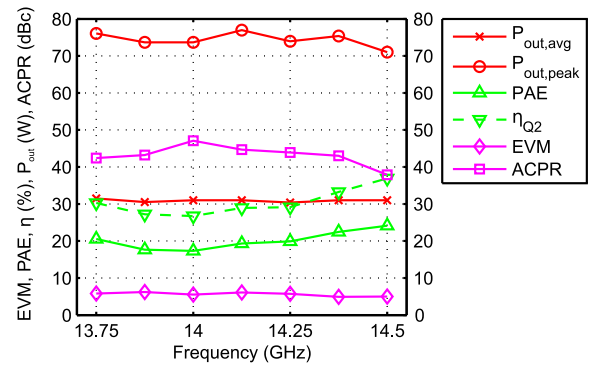
FIGURE 3.38: Measurement results for a QPSK signal with 16 MSym/s; $\alpha = 0.35$ and a RFPAL at ($V_{DS1,2} = 40$ V; $I_{Dq1} = 300$ mA; $I_{Dq2} = 50$ mA).

TABLE 3.5: Linearity measurements for various modulation schemes

MOD	f_0 (GHz)	$P_{out,avg}$ (W)	$P_{out,pk}$ (W)	PAPR (dB)	PAE (%)	η (%)	ACPR (dBc) w/o	w	EVM w (%)
QPSK	13.75	30	73.5	3.9	23	31	31	42	3.2
$\alpha = 0.35$	14.00	30	73.8	3.9	21	29	35	48	3.5
	14.25	30	74	3.9	23	31	32	44	3.6
DVB-S	14.50	30	70.5	3.7	22	30	30	39	3.8
32APSK	13.75	20	62	4.9	23.8	31	21	39	2.8
$\alpha = 0.25$	14.00	20	64	5	22.3	28	25	41	3.5
	14.25	20	65	5.1	22.4	30.2	27	41	3.2
DVB-S2	14.50	20	64.7	5.1	21.7	29.8	26	40	3.3
64APSK	13.75	16	68.3	6.3	22.7	30.2	22	31	6.5
$\alpha = 0.05$	14.00	16	64	6.0	20.3	28.9	26	37	4.5
	14.25	16	68.3	6.2	20.3	28.9	26	35	6.3
DVB-S2X	14.50	16	68	6.3	19.7	28	23	34	6.5

PA for a QPSK and an average output power $P_{out,avg} = 30$ W at 14.375 GHz can be seen. It can be noted that the amplifier can hardly reach the specifications in band as well as the required shoulder distance without (w/o) pre-distortion. The sidelobes cross the mask restrictions. However, the spectrum mask is easily fulfilled with (w) the RF-PAL.

Modulated measurements over frequency are visualized in Fig. 3.38 which takes advantage of the RFPAL for fulfilling the mask. Depending on the measured output crest factor the peak output power ($P_{out,peak}$) can be calculated. It can be noted that $P_{out,peak} \geq 70$ W is much higher than $P_{out,avg}$ during the CW measurements. The lower average power does not produce that much dissipated power and results in lower thermal stress for the devices. Consequently, self heating, that limits the output power, is lowered. The high output power results in an acceptable PAE of $\approx 20\%$ over the *Ku*-band. The calculated drain efficiency is with $\eta_{Q2} \approx 30\%$ as high as intended in the simulation, while the EVM is lower than 6%. Tab. 3.5 shows the linearity measurements for various modulation schemes, all with constant 16 MSym/s. It can be noted that with a higher order modulation scheme and a decreased α the $P_{out,\,avg}$ needs to be decreased as well to fulfil the mask. Nevertheless, high PAE can be achieved even in the deep back-off of the higher order modulation schemes (32APSK, 64APSK). This depicts the possibilities

for high-data rate transmission in VSATs.

3.3.6 Summary

In this section, an extensive design procedure for an efficient two-stage GaN-HEMT PA in the Ku-band has been presented. A Load/Source-Pull methodology has been used with a systematic design approach to develop the matching circuits. Effort was spent for EM-modelling of the matching circuits to reduce the effects of manufacturing constraints. The procedure has later been validated by implementing the two stage PA based on two 70 W bare-die GaN-HEMT devices.

Simulated and measured results of this PA show a very good agreement. Large-signal measurements (CW) show more than 50 W output power in the desired frequency range of interest with more than 23% PAE. These results were achieved while maintaining a high gain of ≥ 15 dB. Linearised modulated measurements using a 16 MSym/s QPSK (DVB-S) signal demonstrate an average PAE of 21% by more than 30 W output power (70 W peak) while holding the linearity requirements. Moreover, higher order modulation schemes 32APSK (DVB-S2), 64APSK (DVB-S2X) were tested and state 20 and 16 W output power with a PAE of $\geq 21\%$. Different manufactured amplifiers show only a small variation in their performance data.

3.4 Lower *Ku*-band MIC PA

To further prove the methodology used in the previous chapters the design has been changed to a working adaptation that should provide an equal output power in the frequency range of 12.75 - 13.25 GHz (F_{low}) and is going to be published in [Maa+op]. This range can also be used for broadcast uplink but not all transponders support its range. Its intended in several countries for providing advanced broadcasting services like UHDTV. Within, higher order APSK modulations are used to increase the data-rate of up to 100 MBit/s per transponder.

3.4.1 PA Design Approach

The design needs to fulfil the same mechanical dimensions (18.7 x 12.5 mm) as the previously mentioned upper *Ku*-band amplifiers to ease an integration within the test-setup. A lowered centre frequency of 1 GHz extends the mechanical length of a $\lambda/4$ 50 Ω MS-line within 0.17 mm ($\lambda/4$ at 14 GHz = 2.12 mm; $\lambda/4$ at 13 GHz = 2.28 mm). By fulfilling the limitations of mechanical dimensions the electrical lengths of the matching circuits needs to stay constant. In addition, the lowered operation frequency should exceed the previously achieved efficiency values based on:

- higher simulated PAE (Tab. 3.3)

- higher optimum impedances and therefore more easy matching circuits

- lowered electrical losses ($\alpha_c, \alpha_d, \alpha_r$)

Nevertheless, the low gain of the devices around 13 GHz needs to maintain the two-stage design with both equal devices as described in Sec. 3.3.1.

3.4.2 Design of Matching Networks

As a first approach the meandering of the 3 to 1 combiner section has been changed, which as a result shrinks its mechanical dimensions. Secondly, the coupling capacitors at all IMN, ISMN as well as OMN were increased, which increases

a pre-transformation. Based on layout constraints, the number of fingers cannot be scaled. As a result, only the finger lengths were enlarged. An increased capacitance results in a lowered SRF, which may affect the tolerance dependency of the whole circuit. As a validation of not exceeding the SRF of the Interdigital capacitors, its quality factor can be utilised. To lower the dependency of bond-wire tolerances the number of bond-wires were increased to three per pad. This does not lower the inductance by a factor of 2/3 - EM simulations showed a total resulting inductance of $L_{Bond} = 11$ pH due to the higher mutual coupling of the wires. The total schematic of the two-stage amplifier is given in Fig. 3.39(a) showing only minor changes to the previous design. The open stubs at the IMN and OMN were changed in position towards the 50 Ω MS-line position. Furthermore, the length of the pre-transformation line (TL$_3$) behind the capacitor C$_{imn}$ at the input side is exceeded.

3.4.3 Simulation Approach

Small-Signal Analysis

The matching networks are simulated like in the previous section using parametrized EM-models of all sub-circuits. The simulated S-Parameters of the matching networks are shown in Fig. 3.39 (b-d). The ports of the simulation are loaded with the optimum impedances that were analysed within the preliminary Load-Pull analysis. For instance, the simulation of the IMN consists of a 50 Ω port (Z_0) that represents the RF$_{in}$ with a reflection coefficient (S_{11}) shown in Fig. 3.39(b). The opposite facing term is the gate-side of the transistor with its optimum source impedances loaded to the port ($Z_{S\,IMN}$) resulting in a reflection coefficient (S_{22}).

The transmission parameter (S_{21}) represents a transmission ratio of the real to complex transformation network IMN. A low reflection coefficient paired with low IL can now be applied to the simulation tool as a design goal. These S-Parameters are shown for all three networks (IMN, ISMN, OMN) where a reflection coefficient of $\leq$-10 dB can be obtained for all networks. Furthermore, the

(a)

(b) IMN   (c) ISMN   (d) OMN

FIGURE 3.39: (a) Schematic of the proposed two-stage amplifier divided into three matching circuits (IMN, ISMN, OMN). Each transmission line (TL) is parallelised by n-times written underneath in green. Simulated EM-based s-parameters while the ports are loaded with the conjugate optimum impedances for (b) IMN (c) ISMN (d) OMN.

transmission losses are $\leq 1\,\mathrm{dB}$ which consists of a mismatch as well as electric losses ($\alpha_c, \alpha_d, \alpha_r$). It can be obtained that the extremely low ohmic input impedances are hard to match, resulting in a lower matching compared to the output side that achieves a RL of up to $20\,\mathrm{dB}$ (Fig. 3.39(d)). The designed circuits were later analysed towards their phase and amplitude imbalance considering the transistors as *transistor cells*. The values of all schematic elements are shown in Tab. 3.6. The

FIGURE 3.40: Simulated EM-based impedances realised by the matching circuits from 12.5 - 13.5 GHz (F_{low}) for the output sides of Q1 (ISMN) and Q2 (OMN). The plotted MuFLoCs represent the minimum value over the desired frequency range F_{low}.

TABLE 3.6: Schematic values of the proposed two-stage amplifier for $f_0 = 13\,\mathrm{GHz}$

IMN	TL_1	TL_2	TL_3	TL_4	TL_5
Φ	96°	108°	66°	74°	31°
Z_{TL}	47 Ω	12.5 Ω	5.6 Ω	3.3 Ω	25 Ω
Z_{TL} x n	47 Ω	37 Ω	53.1 Ω	28 Ω	50 Ω
$C_{imn} = 0.39\,\mathrm{pF}$		$Q_{Cimn} = 39$		$L_{Bond} = 11\,\mathrm{pH}$	

ISMN	TL_6	TL_7	TL_8	TL_9
Φ	84°	59°	52°	77°
Z_{TL}	5.3 Ω	6.5 Ω	6.6 Ω	3.4 Ω
Z_{TL} x n	35.6 Ω	33.7 Ω	37.6 Ω	28.6 Ω
$C_{ismn} = 0.33\,\mathrm{pF}$	$Q_{Cismn} = 38.7$		$L_{Bond} = 11\,\mathrm{pH}$

OMN	TL_{10}	TL_{11}	TL_{12}	TL_{13}	TL_{14}
Φ	82°	21°	105°	96°	22°
Z_{TL}	3.3 Ω	9.1 Ω	13 Ω	47.5 Ω	25 Ω
Z_{TL} x n	27.6 Ω	53.1 Ω	28 Ω	47.5 Ω	50 Ω
$C_{omn} = 0.83\,\mathrm{pF}$		$Q_{Comn} = 38$		$L_{Bond} = 11\,\mathrm{pH}$	

realised impedances of the output networks are optimized towards the MuFLoCs within the frequency range F_{low}. Fig. 3.40 shows the realised impedances for the OMN ($Z_{L\,OMN}$) that are located within the $P_{out} = 47\,\mathrm{dBm}$ contour. Moreover, the OMN impedances fit into the PAE = 39% contour. In contrast the load of the ISMN ($Z_{L\,ISMN}$) is realised with a far wider spread cutting the

FIGURE 3.41: Simulated pulsed RF-behaviour of the amplifier for 10% duty cycle with 1 μs period at 13 GHz.

PAE = 29% contour. The results demonstrate a compromise due to the different directions of the imaginary trajectories of both facing impedances ($Z_{L\,ISMN}$, $Z_{S\,ISMN}$).

Large-Signal Analysis

The Large-Signal analysis is performed with CW as well as pulsed RF-signals. The pulse signals are used to analyse the thermal compression of the devices and lower the self-heating. Fig. 3.41 shows the simulated RF response at 13 GHz with a slight overshoot at the beginning of the pulse. The high output power of up to $P_{out} = 75$ W demonstrates the good output matching. The structure is analysed within large-signal conditions and shows an almost equal output power within F_{low}. During large-signal simulations it turns out that the inherent AM/AM soft-compression of the GaN-HEMT can be easily compensated by lowering the quiescent current of $Q1$ towards a **Class-B** operation. This can be explained by the highly non-linear ac-transconductance of the device with its maximum at $I_{Dq} = 300$ mA at this high frequency operation. This lowering of the quiescent current of $Q1$ down to 100 mA comes along with a further increased mismatch in the ISMN that flattens the overall AM/PM as well as explained in detail in [Qua+14].

3.4.4 Realisation

The bare-dies and substrates were aligned and mounted on a thick CuMoCu-flange (Fig. 3.42(a)). The wedge-wedge bond-wire interconnections
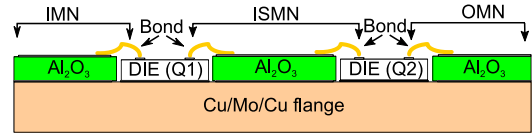
(a)
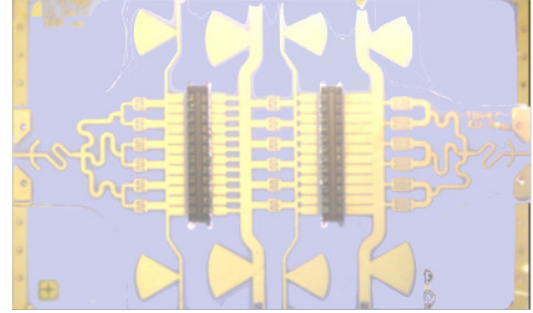
(b)
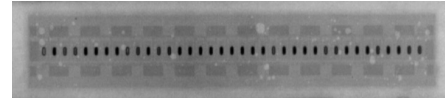
(c)
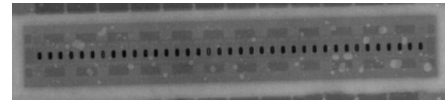
(d)

FIGURE 3.42: Realisation of the amplifier. Side-view illustration of the MIC (a). Top view of the MIC (b). X-Ray pictures of the bare-die Q1 (c), Q2 (d).

were designed to be three in parallel to lower the tolerances of the resulting inductance. A top view of the mounted MIC can be seen in (Fig. 3.42(b)). The die-attach was again analysed via X-Ray microscopy (Fig. 3.42(c), 3.42(d)) to circumvent thermal problems. A grinding pattern of the mounted bare-die was done and shows a thickness of the mounting of 18 μm.

3.4.5 Measurement Results

Small-Signal Measurements

Probed small-signal measurements were performed with 500 μm pitch probes (|Z|-Probe^{TM}) on the alumina substrate using a network analyser (N5230A). In Fig. 3.43(a) a comparison between simulation and measurements of the amplifier can be seen. The probe alignment was checked by changing the position of the probes several times.

This only affects the transmission phase of the measured small-signal measurements within $\pm 6\,°$. The measurement shows a slightly different transmission compared to the simulation resulting in a narrower band-pass behaviour. The gain can be determined to be 21 dB at the centre frequency of 13 GHz and within the in-band frequency range F_{low}. By applying the Monte-Carlo tolerance analysis of Tab. 3.2 the bond-wire tolerances clearly indicate the small deviations between simulation and measurement. To further clarify the dependency of the amplifier over various biasing conditions Fig. 3.43(b) shows the S-Parameters for $I_{Dq1,2} = \{10/10; 50/50; 150/150; 300/300\}$ mA biasing of both amplifier stages $Q1/Q2$.

It can be seen that the biasing conditions of $I_{Dq1,2} = \{150/150\}$ mA nearly achieves the 20 dB small signal gain while $I_{Dq1,2} = \{50/50\}$ mA only results in 10 dB gain. Fig. 3.43(c) visualizes the dependency to the supply voltage varying from $V_{DS1,2} = \{25; 30; 35; 40; 45\}$ V. A huge decrease in gain as well as in matching can be observed by lowering the supply voltage to $V_{DS1,2} = \{25\}$ V.

Large-Signal Measurements

The CW measurement setup of the last section (Fig. 3.31) has certain drawbacks:

- Firstly, the interconnection between the MIC and the surrounding RO4003c substrate was realised via a wide ribbon bond. The height and distance of the ribbon interconnection influence the input as well as output matching of the MIC and therefore cause additional mismatch losses. A de-embedding of this structure is only possible by measuring a suitable reference structure and de-embedding its losses from the measured DUT.

- Secondly, the measurement of the DUT within the CW state is difficult due to self-heating. This affects not only the DUT but also the pre-amplifier stages that are driven into compression due to the high losses of the surrounding RO4003c substrate.
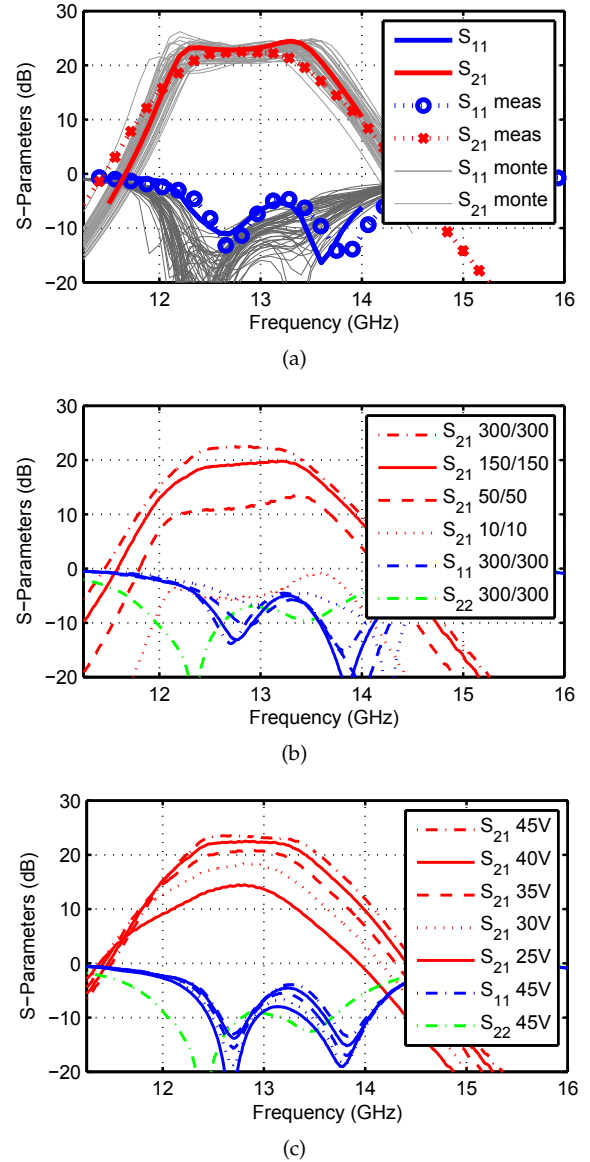
FIGURE 3.43: (a) Comparison between measured and simulated small-signal behaviour over frequency ($V_{DS1,2} = 40$ V; $I_{Dq1,2} = 300$ mA) with additional Monte-Carlo analysis (b) Measured small-signal behaviour in dependency to $I_{Dq1,2}$ ($V_{DS1,2} = 40$ V) (c) Measured small-signal behaviour in dependency to $V_{DS1,2}$ ($I_{Dq1,2} = 300$ mA).

To prevent an unwanted pre-matching of the surrounding substrate, GSG-probes can be used, as already done in the small-signal measurements. A special series of GSG-probes were used that are able to withstand up to 25 W average output power (GSG-500 |Z|-Probe™Power at 10 GHz). To lower interconnection losses the probes were directly connected to the WR75 directional couplers with low loss semi-rigid cables. The measurement setup can be seen in Fig. 3.44 while the MIC is still
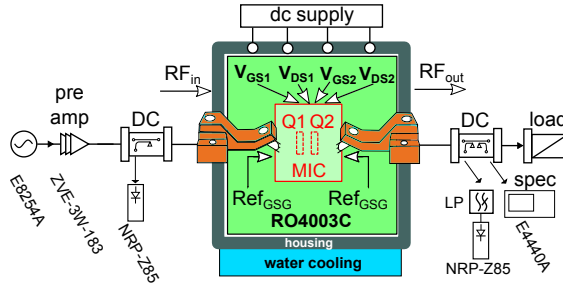
FIGURE 3.44: Probed Large-Signal measurement setup.

(a)

(b)

FIGURE 3.45: Comparison between measured and simulated pulsed RF-behaviour (a) over the input power level at 13 GHz and (b) over frequency ($V_{DS1,2} = 40$ V; $I_{Dq1,2} = 300$ mA).

located within the test-bench for feeding dc and water cooling.

To lower the self-heating of all devices the DUT is measured within pulsed RF conditions. The signal generator (Keysight^{TM}E8254A) can be driven to duty cycles of as low as 10% which means that the full amount of input power is only given during 10% of a period of $1\,\mu s$. The pulsed RF power is measured at the input as well as the output of the DUT via the WR75 directional couplers by peak power meters (R&S^{TM}NRP-Z85). At the output side, an additional low pass filter is located in between the coupled port of the directional coupler and the power meter. This is due to the fact that a wave-guide reacts as a high-pass filter beginning from its cut-off and not, as often suggested, as a bandpass filter. The coupling port is going to overestimate the amount of power by the 2nd harmonics within 11 dB (-29 dB coupling) to the fundamental (-40 dB coupling). Due to the lowered interconnection as well as input losses of this measurement setup, compared to the previous one, an additional pre-amplification after the pre amp is no longer necessary.

Firstly, the probed power measurement setup is calibrated by probing a TL while inserting a pulsed power sweep over frequency. The output power is compared with the input power and fulfils the conditions of equality considering the losses of the TL. The measured average output power $P_{out,avg}$ represents the integrated RF power during the period. Moreover, peak output power $P_{out,pk}$ represents the peak value of power that is only present during the, for example, 10% duty cycle of the period. For this reason, it has to be mentioned that the peak value is not equivalent to eventual positive

or negative overshoots. They are filtered during a timing offset. The peak output power $P_{out,pk}$ is consequently equivalent to the *pulse top power*.

The measured large-signal behaviour of the MIC is shown in Fig. 3.45(a) for a power-sweep at 13 GHz. Secondly, the duty cycle is defined with 10% for $1\,\mu s$ period. The measurement shows a slightly later compression than the simulation and exceeds the power level of the simulation at 13 GHz. The PAE shows a discrepancy in the back-off of the measurement to that of the simulation. In addition, the output power is slightly less than simulated in the back-off which results in a lowered gain and a lower PAE.

The saturated output power demonstrates a great fit to the simulation shown in Fig. 3.45(b). The measured frequency response has a more narrow bandwidth compared to the simulation, still performing within F_{low}. An extremely high peak output power of up to 82 W with $\geq 30\%$ PAE demonstrates the great achievements. The pulsed power

(a)

(b)

(c)
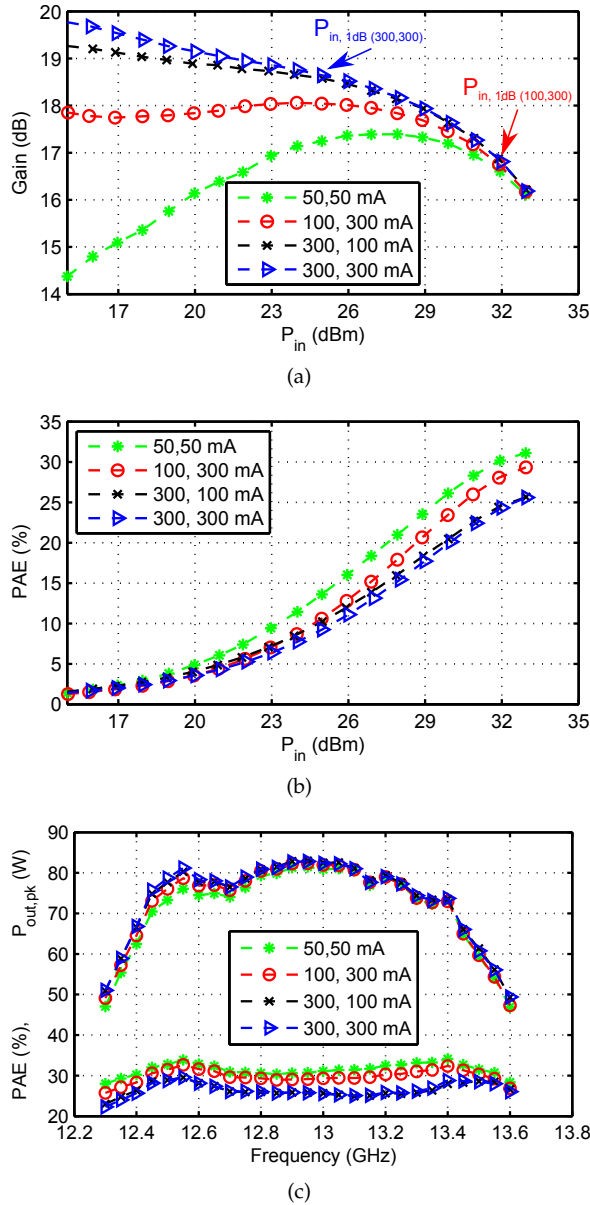
FIGURE 3.46: Measured pulsed RF-behaviour at 13 GHz (a) gain (b) PAE (c) saturated output power and PAE for various biasing conditions of (Q1,Q2) (10% duty cycle $V_{DS1,2} = 40$ V).

measurements makes it possible to get a deeper insight of the typical GaN-HEMT soft compression, which can be observed in Fig. 3.46(a). The

pulsed RF-signal lowers the thermal compression of the devices – the compression behaviour shown is therefore mainly related to the current collapse.

The pre-amplifier (Q1) is realised via a device which is far too large feeding the amplifier (Q2). However, the quiescent current of this stage (Q1) can be lowered while still achieving enough drive level for the PA (Q2). As a result, an almost flat gain compression can be realised with the quiescent current conditions of (100, 300 mA). This technique can be easily applied resulting in a 1 dB compression point of $P_{in\,1dB} = 32$ dBm with $P_{out\,1dB} = 70$ W at 13 GHz. The lowered quiescent current improves the PAE of the amplifier as can be observed in Fig. 3.46(b) with up to 10% towards 30%. The effects of this quiescent current correction over frequency are demonstrated in Fig. 3.46(c) showing that the saturated output power is less influenced while the PAE exceeds the 30% over frequency.

3.4.6 Summary

In this section the design procedures of the previous amplifier were once again applied, while the frequency range was lowered within 1 GHz. The resulting two stage PA was manufactured and its performance shows a great agreement to the simulation. It was possible to improve the measurement setup to a probed pulsed power setup which exceeds the measurement accuracy and lowers the thermal compression of the DUT. The PA shows a high gain of 17 dB with a $P_{out\,1dB} = 70$ W and up to 80 W output power. An increased PAE of $\geq 30\%$ was obtained through this.

3.5 Extended *Ku*-band MIC PA

To further clarify the bandwidth limitations of the transistor, a design should exceed the frequency range of both previously designed amplifiers to 12.75 -14.5 GHz (F_{ext}), which is 14% FBW. This design can be used within all *Ku*-band uplink channels fulfilling the lower F_{low} as well as the upper F_{up} frequency range and is published in [Maa+18].

3.5.1 PA Design Approach

During the design process of the previously mentioned amplifiers two factors limits the bandwidth and as a result the power-match of the amplifiers:

1. The analysed limitations towards a broadband impedance match are mainly related to the extremely low matching impedances. To lower these restrictions the load resistance can be increased by simply increasing the supply voltage (compare Eq. 3.1). The intrinsic breakdown voltage ($V_{BD} \geq 100\,\text{V}$) is the boundary that could not be exceeded. An increase of the supply voltage comes along with a lowered efficiency, which needs to be taken into account during the design.

2. The first pre-transformation of the matching networks is always caused by an inductance that represents the bond-wires. This inductance transforms the optimum load impedance, mainly a capacitive load, crossing the quality-factor circles within the Smith Chart. As already shown in Fig. 3.9(b) a low inductance interconnection to the matching circuit clearly eases the FBW of the matching. The inductance of this bond-wires can be lowered due to paralelizations down to a number of three in parallel. Afterwards, the mutual coupling of the bond-wires no longer decreases its inductances. To accommodate these limitations, ribbon-bond-wire interconnections might be a solution.

Consequently, the theoretical bandwidth limitations related to the Bode Fano equations (Sec. 3.2.3)
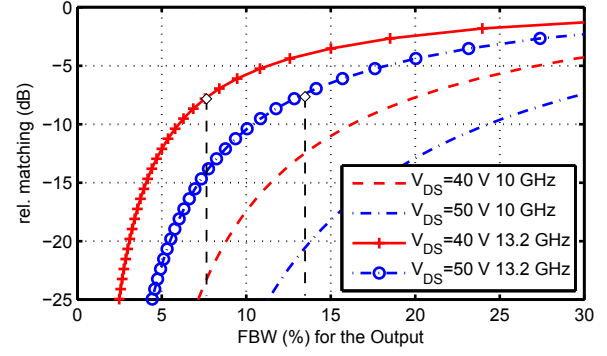
FIGURE 3.47: Analysed theoretical matching limit (Bode Fano) of the complex $Z_{out}\{R_{dc}; C_{DS}; L_{pad}\}$ (bottom) impedances for various supply voltages at $f_0 = 13.2\,\text{GHz}$.

are analysed again for an increased R_{dc} that is related to the $V_{DS} = 50\,\text{V}$ supply and a lowered $L_{bond} = 9\,\text{pH}$ by the usage of ribbon-bond-wires. Fig. 3.47 displays the increased theoretical FBW to 14% for a rel. matching of 8 dB at the new $f_0 = 13.2\,\text{GHz}$.

3.5.2 Design of Matching Networks

The load-pull analysis given in Sec. 3.2.4 has been extended to an increased supply voltage of $V_{DS} = 50\,\text{V}$, as well. Furthermore, the quiescent current was lowered to $I_{Dq} = 100\,\text{mA}$ to improve the efficiency performance as well as flattening the premature compression of GaN-HEMTs. Based on the techniques to build the least-intersection over various load-pull contours given in Sec. 3.2.4 it was also applied for the changed biasing conditions at this extended frequency range (F_{ext}).

3.5.3 Simulation Approach

Small-Signal Analysis

The techniques for designing the matching networks are already described in the previous sections. The same schematic as for the Ku_{low} MIC has been used here again (Fig. 3.39(a)). The bond-wire interconnection of the Q2-OMN has been analysed to be as low inductive as possible. Therefore two parallel ribbon bond-wires per pad were chosen, both with 100 μm width. The structure
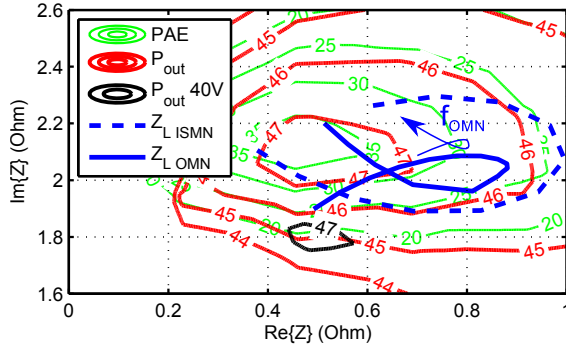
FIGURE 3.48: Simulated EM-based impedances realised by the matching circuits from 12.5 - 14.5 GHz (F_{ext}) for the output sides of $Q1$ (ISMN) and $Q2$ (OMN). The plotted MuFLoC represent the minimum value over the desired frequency range F_{ext} at $V_{DS1,2} = 50$ V.

was analysed within full 3D-EM simulations resulting in a extremely low equivalent inductance of only $L_{Bond} = 9$ pH for 24 parallel ribbon. Based on this value, the OMN was developed to fulfil the requirements of the MuFloC within F_{ext}.

The dc-feed circuits were changed to the new operation frequency by changing the $\lambda/4$ to its equivalent at f_0. As can be seen in Tab. 3.7 the matching Interdigital capacitors C_{omn} are like in the Ku_{low} design while the length and impedances of the TL are corrected to the extended bandwidth F_{ext} and the lowered inductance of L_{Bond}. The realised impedances of the developed OMN are shown in Fig. 3.48 in comparison to the $V_{DS} = 50$ V MuFLoCs. In addition, one MuFloC power contour is displayed, representing the optimum impedance area for the $V_{DS} = 40$ V operation. It can be noted that the area is much smaller and less inductive in comparison to the $V_{DS} = 50$ V operation contours for $P_{out} = 47$ dBm. It was not possible to develop the OMN with such a high transformation ratio to achieve all realised impedances ($Z_{L,OMN}$) within the $P_{out} = 47$ dBm contour. Nevertheless, they fit within the $P_{out} = 46$ dBm contour holding $\approx 25\%$ PAE. The output side of the ISMN ($Z_{L,ISMN}$) is even worth fitting within the $P_{out} = 46$ dBm contour representing a compromise to the input match of the ISMN $Z_{S,ISMN}$. All transmission and reflection coefficients of the matching circuits can be seen in Fig. 3.49. Within this simulation, all ports were once again loaded with the optimum impedances for a power match based on the new Load-Pull

analysis considering the $V_{DS} = 50$ V operation. The transmission parameter (S_{21}) of the IMN shows almost doubled losses in comparison to the previously developed Ku_{low} MIC. Moreover, the real to complex match can only be clarified to a RL ≈ 8 dB. In addition, the matching decreases towards the higher frequency edge of F_{ext} which explains the increased losses. The ISMN shows slightly increased losses in comparison to the Ku_{low} MIC with a tolerable match of up to RL ≈ 10 dB. The OMN can take advantage of its lowered bond inductance and achieves a good power match of up to ≈ 12 dB with a small resonance in the transmission losses at 14.2 GHz.

The extended FBW of F_{ext} leads to an increased asymmetry of the bus bar. To prevent a phase imbalance within the n-times sections of the ISMN the Interdigital coupling capacitors were designed with an unsymmetrical number of fingers across the positions, as can be seen in the picture of the realised MIC (Fig. 3.51(a)). This means that both outer and inner capacitors of the n=6 section were realised with only 3 fingers resulting in $C_{ismn1} = 0.038$ pF. Two different capacitors with 5 fingers ($C_{ismn2} = 0.074$ pF) flatten the phase imbalance of all cells (Q2.1-Q2.12) to $\pm 6\,°$. The resulting total capacitance is $C_{ismn} = 0.3$ pF (Tab. 3.7).

TABLE 3.7: Schematic values of the proposed two-stage amplifier for $f_0 = 13.25$ GHz

IMN ‖	TL$_1$	TL$_2$	TL$_3$	TL$_4$	TL$_5$
Φ	96°	108°	68°	75°	31°
Z_{TL}	47 Ω	12.5 Ω	6.9 Ω	4.2 Ω	25 Ω
Z_{TL} x n	47 Ω	37 Ω	39.8 Ω	27 Ω	50 Ω

$C_{imn} = 0.33$ pF		$Q_{Cimn} = 49$		$L_{Bond} = 11$ pH

ISMN ‖	TL$_6$	TL$_7$	TL$_8$	TL$_9$
Φ	81°	55°	24°	81°
Z_{TL}	4.2 Ω	7.9 Ω	6.5 Ω	3.4 Ω
Z_{TL} x n	35.5 Ω	45 Ω	37.5 Ω	28.3 Ω

$C_{ismn1} = 0.038$ pF	$Q_{Cismn1} = 21$	$L_{Bond} = 11$ pH
$C_{ismn2} = 0.074$ pF	$Q_{Cismn2} = 48$	
$C_{ismn} = (2xC_{ismn2}) \| (4xC_{ismn1}) = 0.3$ pF		$Q_{Cismn} = 30$

OMN ‖	TL$_{10}$	TL$_{11}$	TL$_{12}$	TL$_{13}$	TL$_{14}$
Φ	81°	46°	105°	83°	22°
Z_{TL}	3.3 Ω	6.2 Ω	13 Ω	40.9 Ω	25 Ω
Z_{TL} x n	27.6 Ω	35.6 Ω	28 Ω	40.9 Ω	50 Ω

$C_{omn} = 0.82$ pF		$Q_{Comn} = 39$		$L_{Bond} = 9$ pH

(a) IMN   (b) ISMN   (c) OMN
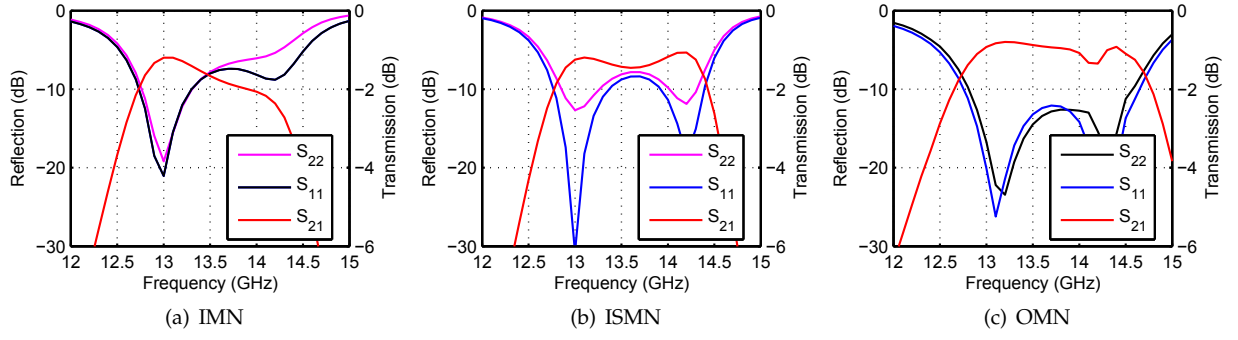
FIGURE 3.49: Simulated EM-based S-Parameters while the ports are loaded with the conjugate optimum impedances for (b) IMN (c) ISMN (d) OMN.

Large-Signal Analysis

The amplifier was analysed towards pulsed RF-operation as mentioned during the previous designs. Nevertheless, CW analysis was used to ensure a proper function of the amplifier by an increased thermal heating. Given the increased supply voltage, special care must be taken not to exceed the breakdown limitations of the device ($V_{BD} = 100\,$V). This breakdown voltage needs to be interpreted as the breakdown voltage of the intrinsic current source. Therefore, once again, the large-signal analysis approach of the twelve parallel *transistor cells* is employed to provide insight within the cells (Q2.1-Q2.12). Nevertheless, this extrinsic *transistor cells* needs to be de-embedded to the intrinsic current source by compensating the output capacitance C_{DS} as well as pad inductances L_{pad}. The voltage swing of all *transistor cells* can be monitored (intrinsic) during a power and frequency sweep of the pulsed RF-simulation and is shown in Fig. 3.50(a). It was obtained that the intrinsic voltage swing is up to 10 V higher than the extrinsic one. It can be seen that some frequency points at some intrinsic *transistor cells* are about to reach the V_{BD} for a high drive level of $P_{in} = 34\,$dBm. The model itself features a port that indicates the channel temperature of the devices so all temperatures of the *transistor cells* can be shown in Fig. 3.50(b) for saturation over frequency. The manufacturer limits the mounting temperature to 320°C for not exceeding the maximum channel temperature. The simulation shows only values

(a)

(b)
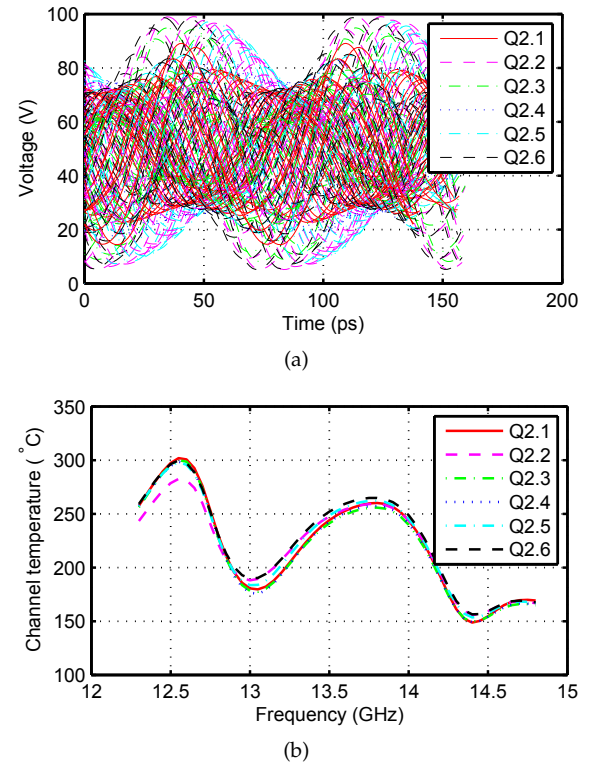
FIGURE 3.50: CW simulated (a) intrinsic voltage-swing (b) channel temperature for saturation operation ($V_{DS1,2} = 50\,$V; $I_{Dq1,2} = 100\,$mA; $P_{in} = 34\,$dBm).

up to 300°C for the high CW saturation. An almost equal heat spread over the *transistor cells* can be observed, indicating a good phase as well as amplitude over the wide bare-die. Large-signal stability was once-again ensured by the use of the *STAN^{TM}-Tool*.
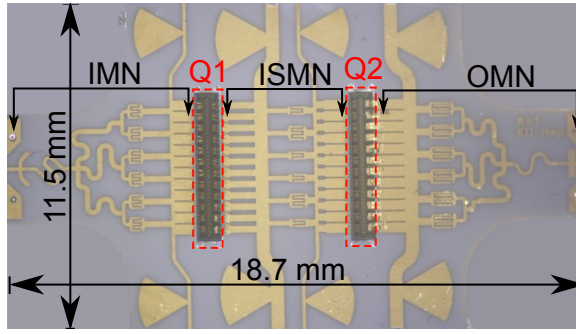
(a)
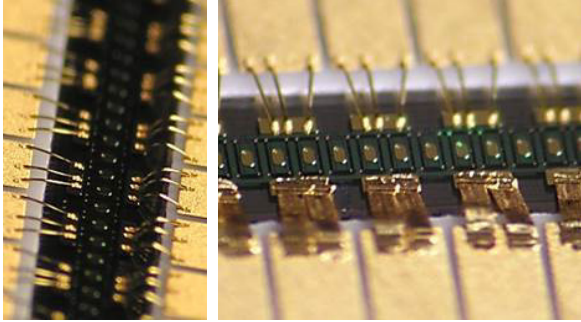
(b) (c)

FIGURE 3.51: (a) Top view of the extended *Ku*-band MIC (b) wedge-wedge bond-wire interconnection for $Q1$ (c) bond and ribbon interconnection for $Q2$.

3.5.4 Realisation

The bare-dies and substrates were aligned and mounted on a thick CuMoCu-flange, as for the previously mentioned amplifiers (Fig. 3.51(a)). Special care was taken for the bond-wire interconnections between the matching networks and the bare-die. The realised mounting distances were measured to calculate the best loop-height (that influences the bond-inductance) of the wedge-wedge bond-wires for the three interconnections (IMN-$Q1$, $Q1$-ISMN, ISMN-$Q2$). Fig. 3.51(b) displays a different shape of the connection IMN-$Q1$ (left) to the $Q1$-ISMN (right). Taking into consideration, the closed positioning between $Q1$ and $Q2$ with this bond-arrays, one may argue that a huge coupling between these different stages will occur. However, the extremely low impedance level at the input and output of the devices paired with the flat bond-wires makes the radiation negligible.

The output interconnection $Q2$-OMN is the most critical for the increased bandwidth of F_{ext} which is why it was realised with $100\,\mu m$ wide ribbon
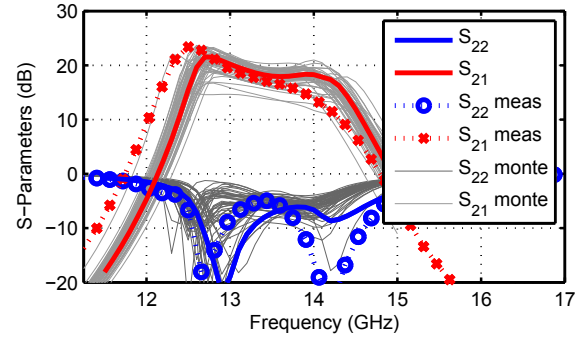
FIGURE 3.52: Comparison between measured and simulated small-signal behaviour over frequency ($V_{DS1,2} = 50\,V$; $I_{Dq1,2} = 100\,mA$) with additional Monte-Carlo analysis.

wires, as can be seen in Fig. 4.21. These ribbon interconnections were realised by the development of a special deep access ribbon wedge that is able to feed a $100\,\mu m$ wide ribbon into a sink while not cracking the surrounding substrates. To be able to melt this ribbon to the pads, the ultrasonic power of a bonder (K&S 4526) needed to be further amplified. The resulting ribbons from Fig. 3.51(c) visualises an extremely wide and low resistance interconnection to the bare-die. Within this manual bonding the risk of a bonding besides the pads is high, due to the enlarged size of the wedge. Nevertheless, no damage to the pads or the channel was observed.

Small-Signal Measurements

Fig. 3.52 shows a comparison between the simulation and the measurements of the amplifier. The increased supply voltage and the reduced quiescent current lead to almost the same small-signal gain in the simulation like for the previous MICs. The measurements indicate a frequency shift towards lower frequencies within 200 MHz. This leads to a non-flat amplification behaviour with up to 22 dB gain for the lowest operation frequency while only achieving a gain of 12 dB for 14.1 GHz. By considering the tolerances of the bond-wire inductance during a Monte-Carlo analysis, the measurements can hardly be explained only based on this bond-wire tolerances. Analysing the output reflection coefficient (S_{22}) the measurement indicates a far higher match than simulated for its poles but not

(a)

(b)
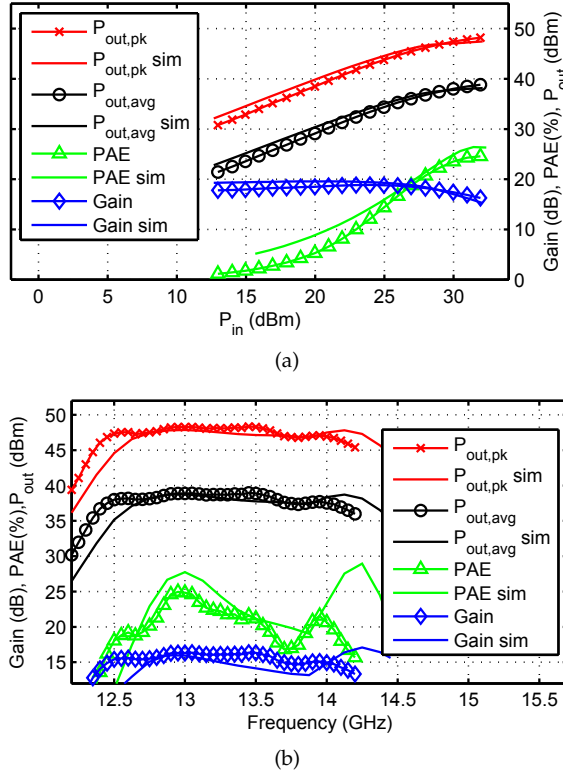
FIGURE 3.53: Comparison between measured and simulated large-signal behaviour (a) over the input power level at 13 GHz and (b) over frequency ($V_{DS1,2} = 50$ V; $I_{Dq1,2} = 100$ mA).

FIGURE 3.54: Measured saturated pulsed output power and PAE for various supply voltages (10% duty cycle $I_{Dq1,2} = 100$ mA, $P_{in} = 34$ dBm).

in the central area of f_0. A detailed optical measurement of the Interdigital fingers located in the OMN (C_{omn}) indicated that the finger distance (W_{gap}) was $\approx 5\,\mu m$ less than simulated. This can be explained by a layout failure resulting in an increased finger width (W_f). An increased capacitance can explain the frequency shift as well as the asymmetry. Nevertheless, the bandwidth of the measured amplifier is equal to its simulation.

Large-Signal Measurements

Large-signal measurements were carried out in the probed-pulsed power setup shown in Fig. 3.31. The measured behaviour of the MIC is shown in Fig. 3.53(a) for a power-sweep at 13 GHz. A good agreement can be observed with a slightly lowered gain of the measurement in the deep input back-off operation (deeper **Class-AB**), which leads to a reduced PAE. The duty cycle is defined with 10% for a $1\,\mu s$ period. The saturated output power is shown in accordance with the simulation in

Fig. 3.53(b). The already observed frequency shift of the small-signal measurements can be seen in these large-signal measurements again. Apart from that, the gain and, as a result, the output power drops ≈ 1 dB starting from 13.7 GHz. Despite the fact that a peak output power ≥ 55 W can be observed in between 14% FBW. The dependency to the supply voltage is displayed in detail in Fig. 3.54. The saturated output power significantly drops for a lowered supply voltage, due to the lower power-match. The PAE stays somehow constant around 20% in between 12.4-14.1 GHz even for the high voltage biasing conditions, due to the improved power-match.

3.5.5 Summary

In this section, the design procedures of the previous section were once again applied. The frequency range was extended to fit both the lower (F_{low}) as well as the upper (F_{up}) frequency range. To ease the matching, the optimum load impedances were enlarged by increasing the supply voltage. Furthermore, the bond-wire interconnections were improved by ribbon bond-wires. The resulting two stage PA was manufactured and its performance shows a good match according to the simulation with 200 MHz frequency shift. The PA shows a saturated gain of 15 dB with a $P_{out} \geq 55$ W, while a PAE of $\geq 20\%$ was obtained. The FBW of this design enlarged the previous ones to 14%, which is nearly the theoretically assumed 15% limitation of a working busbar, as stated by [Mar+99].

3.6 Efficiency Enhancement

To further improve the efficiency of power amplifiers within the *Ku*-band, the efficiency restrictions needed to be determined:

1. The **saturation efficiency** is limited by the transistor losses, as described in Sec. 2.2. The saturation efficiency of an amplifier can be enhanced by compensating its parasitics to shape the overlap between the current and voltage waveform at the intrinsic transistor. This *waveform* engineering is realised by *switch-mode* amplifiers which take advantage of special reflection coefficients at the harmonics of the amplifier. These techniques are nowadays popular within the mobile communication market [Cri06]. As previously described in Sec. 3.2.4, a harmonic Load-Pull analysis has shown that the scaling of the huge transistor bar is too wide to see an influence of harmonic matching at the intrinsic waveforms. The only solution for increasing the saturated efficiency of the amplifiers would be to realise a pre-matching located more closely to the intrinsic transistor. In addition, future design technologies like 150 nm GaN-HEMTs can take advantage from a lowered on-resistance and therefore lower losses at higher frequencies. None of these techniques can be applied to the developed MIC's.

2. The **back-off efficiency** of an amplifier is limited by its matching. It can be enhanced by increasing the optimum load-impedances during the output back-off (OBO) conditions while maintaining a low load-impedance during saturation, known as load-modulation. There are two common approaches for changing the load impedance. It can be realised by either changing the supply voltage, which is called *envelope tracking* [Kah52], or by modulating the sink and therefore the current which is defined as a *Doherty amplifier* [Doh36].

Modern DVB-S2x modulation standards have a PAPR of up to 6 dB, which means a PA is often driven in back-off operation. Furthermore, the amplifier working in a satellite link needs to be driven in an even lower output power, to gain for extra power during a rain-margin. Common amplifier architectures like **Class-C** and **Class-AB** suffer from a much lower efficiency here than in saturation. The techniques of enhancing the back-off efficiency should be evaluated within this section on the developed amplifiers.

3.6.1 Envelope Tracking

A way to change the load impedance of the transistor while working in the back-off is to change its supply voltage as can be seen in Fig. 3.48. This way, the optimum load impedance of the transistor decreases and saturation is achieved earlier. With an increased signal magnitude, the supply-voltage needs to increase as well to enhance the saturation again [Kah52]. Hence, the so-called envelope follows the momentary amplitude of the RF signal, which is called *envelope tracking* (ET).

Dynamic Envelope Tracking

To realise a working ET system, one has to control the supply voltage based on the actual RF-waveform in real-time. Therefore, an ET-system has been developed and published in [Maa+16b] for the ultra high frequency range (470 - 803 MHz). The block diagram is shown in Fig. 3.55(a) with a R&S SMU200a signal generation feeding the RF-signal as well as the envelope. The envelope is connected to the supply modulator via a low voltage differential signal connection (LVDS), ensuring signal integrity. The supply modulator (Emerson P5) used can take advantage of its extremely high dc/dc conversion efficiency by up to 95% with up to 80 MHz modulation bandwidth, which is multiple times the signal bandwidth required in [Wan14]. Overall, the supply modulator is able to switch 15 V (V_{MOD}) with multi-levels in 12 bit resolution. An additional supply voltage (V_{FIX}) is used to increase the supply voltage to 30 V ($V_{FIX}+V_{MOD}$).

(a)

(b)
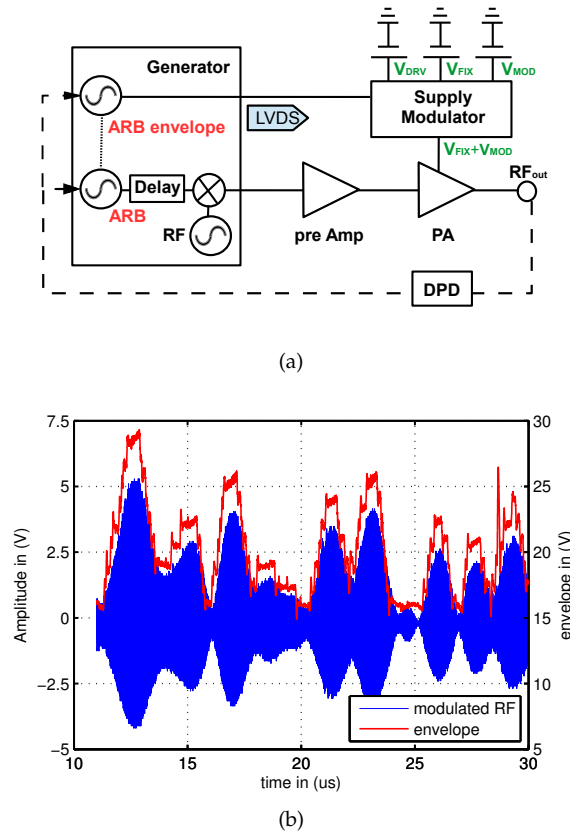
FIGURE 3.55: (a) Block diagram of the proposed ET system (b) Measured modulated RF and corresponding envelope for a 470 MHz DVB-T signal with 8.6 MHz bandwidth measured at the drain.

A programmable RF-delay within the signal generator ensures a synchronisation of the RF and the modulated supply at the drain of the PA. A measurement of this alignment was carried out with an Oscilloscope and is shown in Fig. 3.55(b). Although the envelope is not a constant adoption of the amplitude but rather a discretised function, due to the high number of steps, one would not call this static or a **Class-G** amplifier.

These analyses were made for laterally diffused metal oxide semiconductor (LDMOS) amplifiers working between 470 to 803 MHz for application in terrestrial broadcasting. The use of ET for this amplifier results in an overall efficiency improvement of 14% for modulated signals over the entire frequency range. The signals used are 8 MHz DVB-T signals (COFDM64 QAM) with a PAPR = 9 dB. Although the signals differ from its pendants in the satellite communication market the system used

can be easily adopted to an application within the *Ku*-band by replacing the pre-amplifier and the PA with a complete *Ku*-band BUC. Nevertheless, this technique represents an adoption with access to the baseband signal and therefore the baseband modulator, which cannot be granted within most SatCom applications.

Static Envelope Tracking

Static measurements were carried out to analyse the possible influence of a dynamic ET on the PAE of a *Ku*-band PA. This means that the supply voltage of the PA is constantly changing with discrete voltage levels during a power-sweep to achieve the maximum PAE for different output power states of the PA. This static change in supply voltage can be defined as a **Class-G** amplifier widely used for non time-sensitive applications.

The lower *Ku*-band PA, described in Section 3.4, was tested in its pulsed RF probe measurement setup. It should be mentioned that a reduction in the supply voltage results in a huge reduction of the amplifiers gain, as shown in Fig. 3.43(c) during small-signal measurements. An ET is intentionally used to increase the load in the back-off, which works for ideal transistors as well as for low frequency applications. As the gain shows a significant dependency on small variations in the supply voltage, the load-modulation is reduced. It is therefore not the drain efficiency which has to be improved by this static ET but rather the PAE, taking the lowered gain into account.

By using a simple algorithm which compares the achieved PAE for all supply voltages ($V_{DS1,2}$ = {20-45}V) during a power sweep, an improvement can be obtained from Fig. 3.56(a). This way, the power sweep is shown over the peak output power ($P_{out,pk}$) of a pulsed signal. While considering an output power back-off (OBO) of 4 dB, 11% PAE is reached for a supply voltage of $V_{DS1,2}$ = 45 V. By reducing the supply voltage to 35 V an improvement to 16% PAE can be obtained while the saturated output power is reduced. The static variation of supply voltage down to $V_{DS1,2}$ = 20 V improves
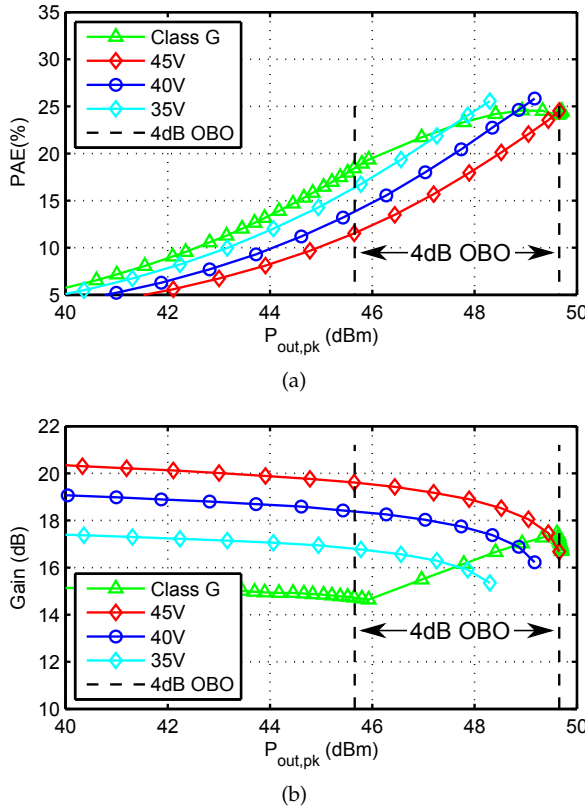
FIGURE 3.56: Measured (a) PAE (b) gain of the **Class-G** PA at 13 GHz (10% duty cycle, $I_{Dq1,2} = 300$ mA).
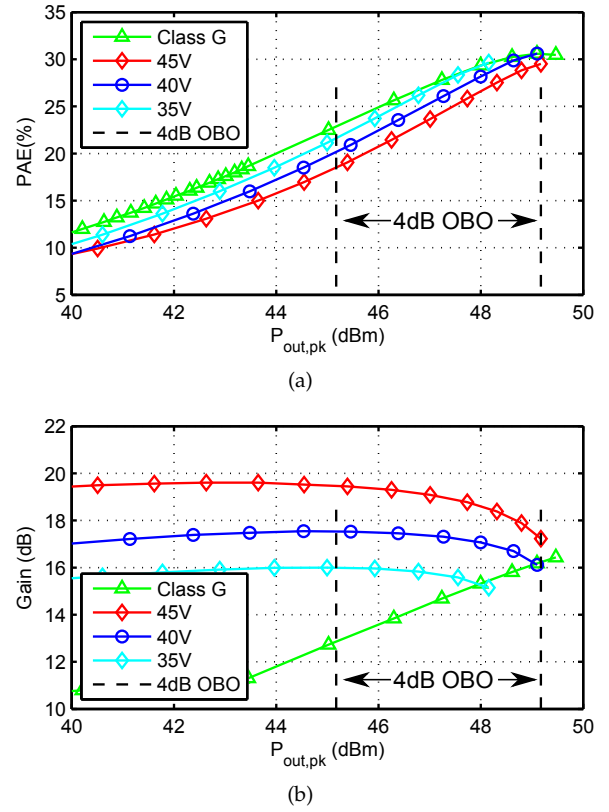
FIGURE 3.57: Measured (a) PAE (b) gain of the **Class-G** PA at 13 GHz (10% duty cycle, $I_{Dq1,2} = 50$ mA).

the OBO PAE up to 19%. With an increased output power level the **Class-G** statical increases the supply voltage to achieve the same high saturated output power as the constant supply voltage of $V_{DS1,2} = 45$ V. This algorithm leads to a non-linear gain over the output power level which is shown in Fig. 3.56. One should notice that the minor PAE improvement of 8% does not justify this impractical large-signal gain. By changing the algorithm to maintain a constant gain over the output power, only minor efficiency improvements of up to 4% were obtainable.

The impact of reducing the quiescent current towards deep **Class-B** biasing has a much higher influence on improving the PAE than the reduced voltage, as can be seen in Fig. 3.57(a). Yet, the lowered large signal gain of this biasing with $I_{Dq1,2} = 50$ mA shows a much more linear behaviour than the **Class-G** amplifier (Fig. 3.57(b)). The PAE of the $V_{DS1,2} = 40$ V measurement is improved in the saturation from 25% to 30%. In the 4 dB OBO the improvement is 6% while maintaining an almost

flat gain of 17 dB during the power sweep. In theory, the optimum impedance is increased by lowering the supply voltage. In fact, for all FET a lowering of the supply voltage furthermore reacts in an increase of the drain-source capacitance C_{DS}, which furthermore increases the complex optimum impedance. By applying this technique to a GaN-HEMT the drain-source capacitance C_{DS} only shows a small dependency on the supply voltage ($C_{DS} \neq f(V_{DS})$ Fig. 3.11(b)), whereas the feedback capacitance C_{DG} shows a huge dependency ($C_{DG} = f(V_{DS})$). Additionally, an increase in the input capacitance C_{GS} can be obtained for a high frequency operation (Fig. 3.11(b)). Note that this is not directly related to the standalone extrinsic capacitance: it is a dependency of the total die parasitics obtained for an increasing high feedback capacitance.

The dominance of the feedback capacitance clearly

reduces the effect of ET for GaN-HEMT's operating at frequencies above the frequency of unconditional stability. Furthermore, the gain of the transistor suffers a lot from reducing the supply voltage which results in a lowered effect of ET applied to GaN-HEMT amplifiers at high operation frequencies.

3.6.2 Doherty Amplifier

An active load-modulation can be achieved by changing the load of the main amplifier with an additional peaking amplifier in the back-off. During saturation, a combined working of both amplifiers is maintained. For the usage of this Doherty technique a few restrictions need to be considered:

1. The combining of two amplifiers, even with the use of ideal power-splitters and combiners, reduces the power gain of the amplifier.

2. With the use of non-ideal working transistors the load-modulation has to consider the non-linear parasitics. One solution is to increase the peaking-amplifier in size compared to the main-amplifier.

3. The working bandwidth of a Doherty amplifier is practically restricted. There is ongoing work to enhance this FBW to $\geq 50\%$ with the use of extremely low-ohmic transformation circuits in UHF [Qur+14]. Towards higher frequencies non equal devices help to increase the FBW to $\geq 42\%$ with additional non $50\,\Omega$ transformation circuits [Bat+11].

4. The improved OBO with an increased back-off efficiency depends on the design. For the realisation of high OBO like $10\,\text{dB}$ the usage of multiple peaking amplifiers is useful to achieve multiple peaks in the OBO efficiency [Ngh+14].

To use a Doherty amplifier in the *Ku*-band one has to consider the extremely non-linear parasitics paired with a low gain of the devices. The first stated argument of a decreased gain can be lowered by using the two-stage amplifier MIC of Ku_{up}. The already decreased gain of this MIC is partially

(a)

(b)   (c)
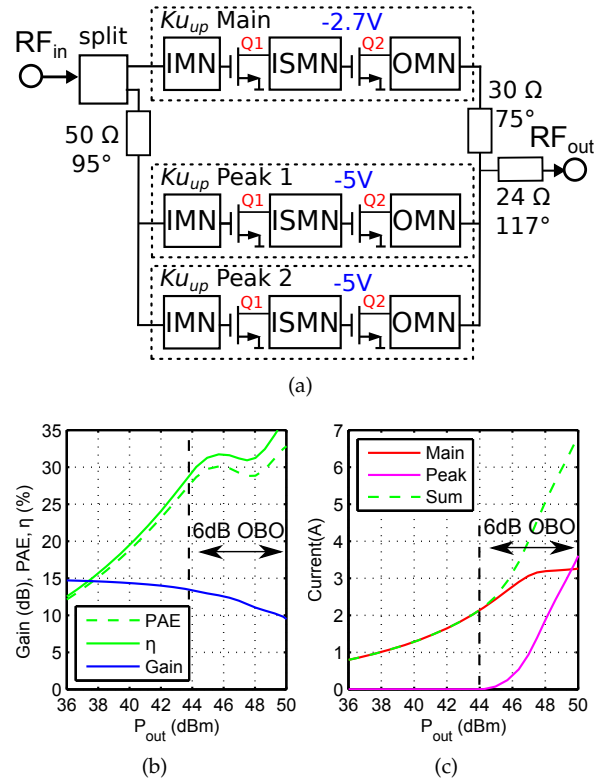
FIGURE 3.58: (a) Schematic view of the 2-Way unequal Doherty using three Ku_{up} MIC (b) simulation of the RF compression (c) simulation of the current distribution between the main and peaking amplifier ($14\,\text{GHz}$; CW, $I_{\text{Main}} = 500\,\text{mA}$, $V_{\text{GS,Peak}} = \text{-5 V}$).

related to its huge non-linear Miller capacitance. Multiple peaking amplifiers are therefore necessary to achieve a load-modulation of the main amplifier. However, bandwidth is not a restriction within the SatCom uplink because the FBW is only in the range of 6%. In addition, the OBO only needs to be improved within 4 - 6 dB considering the future DVB-S2x modulation schemes.

3.6.2.1 Simulation Approach

Within a simulation the Ku_{up} amplifier was analysed in an unequal 2-Way Doherty setup as shown in Fig. 3.58(a). The load of the Ku_{up} main amplifier can be modulated by using two parallel Ku_{up} peaking amplifiers. This unequal device technique is able to compensate for the strongly non-linear transconductance (Fig. 3.10(a)) as well as the non-linear Miller capacitance. The calculations of the load transforming networks were carried out as described in [Bat+11]. Fig. 3.58(b) visualizes the

simulation results of the proper working Doherty amplifier. The PAE and η can be held $\geq 30\%$ for the 6 dB OBO simulation at 14 GHz. Furthermore, Fig. 3.58(c) depicts the equal current split of the main and peaking amplifier with only a slight amount of leakage current.

The obtained simulated results work for the whole F_{up} frequency range. Nevertheless, they are obtained by using MS-line models. For a realisation, the distance between two Ku_{up} MIC is restricted by its mechanical size (18x12.5 mm). Within the first approach, it was intended to design low-loss SIW transformation structures to achieve a high mechanical distance with lower electrical losses compared to MS-lines.

So splitting and combining structures based on Riblet Short-Slot SIW structures were designed and published. The work [Kon+16] describes such an wideband SIW coupler (Fig. 3.59(a)). While a lot of effort was spend on improving the MS to SIW transitions used in this coupler (IL ≤ 0.7 dB), the losses of SIW related structures are by far too high (≥ 4 dB Fig. 3.59(b)) for use with a combining or splitting network. A future design methodology can rely on thicker SIW structures or air-filled SIW to lower the losses.

According to the simulation results, the improved back-off efficiency of a few percent, does not justify the usage of six bare-dies while the total gain remains at 10 dB for saturation.

To face this problem a scaling of the main and peaking device needs to be further investigated and the transforming as well as splitting structures needs to be realised directly on a MMIC, as already done in [Qua+17].

(a)

(b)
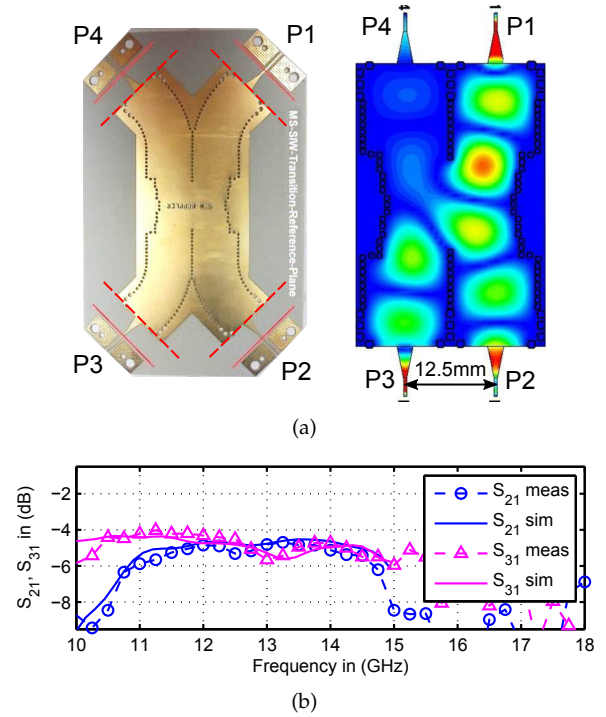
FIGURE 3.59: (a) Layoutview of the developed SIW coupler (b) de-embedded comparison between measurement and simulation of the coupling [Kon+16].

3.6.3 Summary

Within this section efficiency enhancement methods are analysed regarding their usability towards *Ku*-band SatCom PAs. The saturation efficiency of the developed PAs cannot be improved, due to the low dependency of the transistor itself regarding a harmonic match.

To enhance the back-off efficiency, static envelope tracking measurements were carried out for the developed Ku_{low} MIC and show a PAE improvement of up to 10% for the 4 dB OBO. The resulting varying gain reduces the usability of this technique.

The Ku_{up} MIC was analysed towards an improvement of the back-off efficiency by using a Doherty technique. The simulations proved, that during the 6 dB OBO the PAE can maintain $\geq 30\%$. Nevertheless, the large-signal gain decreased to only 10 dB using six bare-dies, therefore the design has not being further pursued.

3.7 Discussion

The results of the developed amplifiers are shown in comparison to previously reported packaged PAs in Tab. 3.8. The first two entries represent MMICs that have a comparable gain to the first described MIC (Ku_{up}) while suffering from a lower output power and PAE. The published MIC [Kaz+11] shows excellent PAE but under pulsed power conditions. Bandwidth and gain are considerably lower than in this work. However, the reported MICs [Not+12], [Ima+14] determine the max. output power reported suffering from a low power gain. A pre-matched MMIC resulting in a MIC reported in [Yua+16] demonstrates high bandwidth with high efficiency. These obtained results are implausible considering their design and measurement techniques and the FBW in particular exceeds the theoretical limitations. The first reported work [Maa+16a] shows a high power density over 6% FBW by using the smaller 25 W device.

Within the MIC Ku_{up} [Maa+17a] the low power gain is extended to 15 dB by keeping the PAE at $\geq 21\%$. Furthermore, an higher output power was achieved due to the increased gate-periphery.

The lower part in this table (Tab. 3.8) denotes the achievements within the lower *Ku*-band. The first entry represents a MMIC (Die) of Wolfspeed [Crea] using the same transistor technology as this work, but with a significant higher total gate width (W_t). With this higher gate periphery, it achieves 20 W less output power than the developed MIC Ku_{low} with significant less PAE and a lower FBW. The second entry [Nag+16] can take advantage of its lower gate length (150 nm) and moreover the increased PAE of 34%. Nevertheless, this MMIC has an almost doubled amount of W_t compared to Ku_{low} with an extremely low gain of only 6 dB.

The last entry represents the developed MIC Ku_{ext} which almost doubles the reported FBW to 14%, so the PAE is lower but still at 20%.

The excellent results obtained indicate that a hybrid two stage design approach has significant advantages towards system design while achieving a state-of-the-art efficiency.

TABLE 3.8: Comparison of state of the art PA in the *Ku*-band

	design	f_c (GHz)	FBW (%)	P_{out} (W)	Gain (dB)	PAE (%)	size (mm^2)	l_g (μm)	W_t [3] (mm)
[Kan+14]	MMIC	14.1	5	20 (CW)	10	16	226	0.25	9.6
[Creb]	MMIC	14.1	5	25 (CW)	20	18	232	0.25	16
[Kaz+11]	MIC	15.0	3.3	56 (pulse)	8	44	90	0.25	20
[Not+12]	MIC	14.0	-	100 (pulse)	-	-	-	0.25	38.4
[Ima+14]	MIC	14.1	5	80 (CW)	4.5	22	217	0.25	57.6
[Yua+16]	MIC	15	22.5	30 (pulse)	20	38	24	0.25	7.2
[Maa+16a]	MIC	14.0	6	12 (CW)	6	23	90	0.25	4.8
Ku_{up}	MIC	14.0	6	30 (QPSK)[1]	15	21	234	0.25	14.4
[Maa+17a]		14.0	6	70 (QPSK)[2]	15	21	234	0.25	14.4
		14.0	6	50 (CW)	15	23	234	0.25	14.4
[Crea]	MMIC (Die)	12.97	4	60 (pulse)	17.5	27	32.3	0.25	18
[Nag+16]	MIC	11.45	4	100 (CW)	6	35	217	0.15	28.8
Ku_{low}	MIC	12.9	7	80 (pulse)	17	34	215	0.25	14.4
Ku_{ext}	MIC	13.25	14	$\geq$55 (pulse)	15	20	215	0.25	14.4

[1] average power for QPSK.   [2] peak power for QPSK.   [3] Only PA stage.

4 Block Up-Converter

A block up-converter (BUC) is a part of the transmitting chain within a satellite uplink base-station. The signal processing of this base-station relies on a double up-conversion technique. First the modem generates a baseband signal and converts it to the intermediate frequency (IF 950-750 MHz). Afterwards, the BUC converts this IF to the radio frequency (RF).

Within this chapter the design and measurements of a BUC with packaged integrated circuits that are part of a hybrid design is described. The up-conversion from the IF (950-1750 MHz) towards the radio frequency (13.75-14.5 GHz) was conducted by mixing the IF with a phased locked local oscillator (PLO) of 12.8 GHz, which is described in detail in Sec. 4.1 (Fig. 4.1).

Unwanted mixing products had to be filtered by the TX-filter introduced in Sec. 4.2. A pre-amplifier is necessary for boosting the signal to a higher power level to feed the final PA (Sec. 4.3). In addition, the developed BUC was equipped with a pre-distortion technique that compares the output of the PA with the IF input (Sec. 4.3).

The MS output of the BUC was converted into a WR75 waveguide which is implemented in the housing (Sec. 4.5).

The complete conversion chain was analysed in a

system simulation as well as evaluating measurements which where carried out and described in Sec. 4.6.

A discussion section states the developed two BUCs in comparison to commercially available BUCs in Sec. 4.8.

The results of this realised BUC are partially published in [Maa+17c] and [Rau+17b].

Circuit Board

Within modern electronic mass-production all sub-elements of the circuit should be housed separately to ease the manufacturing. Most of these IC packages use a $500\,\mu m$ pitch between their pins. This value becomes important when the high frequencies which should be routed on the BUC circuit board are taken into consideration. As a design goal the lead-width of a package pad should represent a $50\,\Omega$ characteristic line impedance for an MS or coplanar line. Consequently, the height of the substrate with its ε_r can be calculated based on the lead-width. Within this design a RO4003c substrate with an $\varepsilon_r = 3.5$ and a thickness of $221\,\mu m$ was chosen, resulting in a line-width of $0.46\,mm$ for $Z_L = 50\,\Omega$ ($\Phi_{90} = 4.5\,mm$; $\varepsilon_{r,eff} = 2.7$). To lower the losses within the substrate, a special LoPro foil was chosen which lowers the roughness of
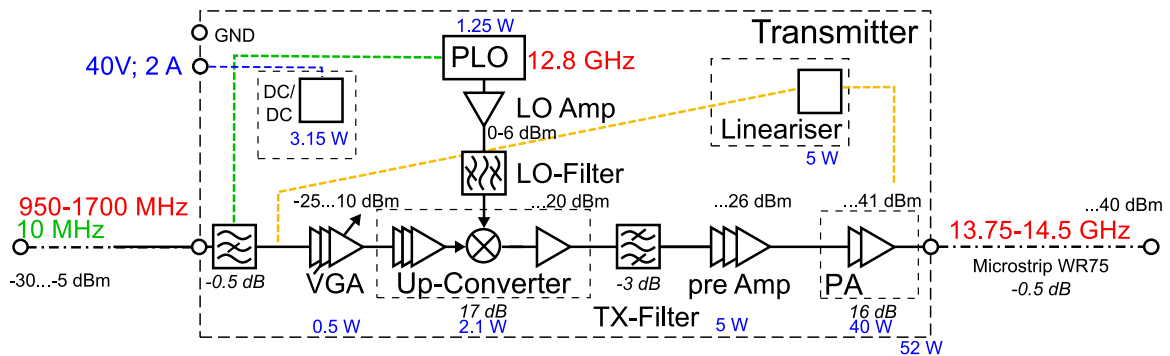
FIGURE 4.1: Schematic of the BUC including the predicted power levels and the power consumption.
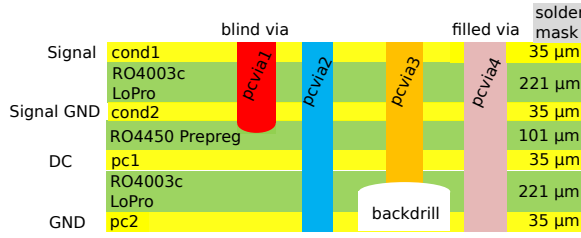
FIGURE 4.2: Layerstack of the HF circuit board.

the metallisation (as discussed in Section 2.1). Due to the high number of different potentials, a four layer stack provides two layers with 221 μm of thickness and one 101 μm prepreg (RO4450) in between to ease routing (Fig. 4.2). Furthermore, thermal vias (filled vias) are realised underneath the ICs as well as blind vias and via-walls for the high frequency isolation. In addition, vias can get back-drilled and plugged to provide spacing to a housing underneath and therefore, dc-isolation. Unlike a layer-stack with RO4350b, on top of a conventional FR4 core, this layer-stack is symmetric and does not bend during the lamination process.

4.1 Frequency Generation

Local Oscillator

SatCom relies on several timing protocols. For example, time division multiplexing (TDMA) is used within the modem to synchronize TX and RX data for different users. This means the modem provides a 10 MHz output signal (REF) to the BUC. The LO of the BUC is realised as a phased locked oscillator (PLO) referenced to the (REF) input. This REF is provided by an external modem but its phase noise depends on the crystal technology used within the modem. The REF signal is fed into the BUC in combination with the IF signal. At the input chain of the BUC both signals are extracted from each other via a triplexer filter that was realised via SMD components.

The output frequency of the LO should be 12.8 GHz, which is why the conversion ratio from 10 MHz is x1280. This leads to a high amount

(a)

(b)
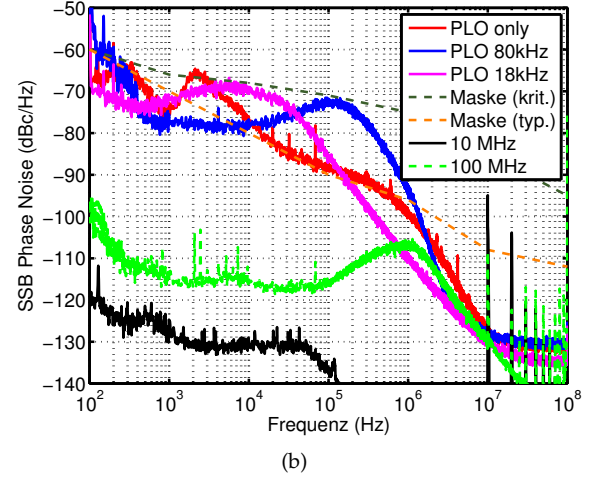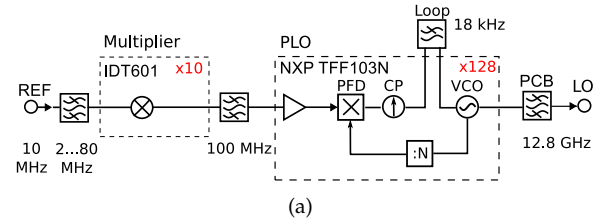
FIGURE 4.3: (a) Schematic of the multiplied PLO with its (b) measured SSB phase noise.

of theoretically converted phase noise (PN_{conv}):

$$PN_{\text{conv}} = 20 \cdot log(1280) = 62.2\,dB. \qquad (4.1)$$

Multiplied PLO

Within the first approach, the REF is directly multiplied by a factor of x10 via a simple multiplier. An integrated clock synthesizer should provide a low phase noise and consists of a sub-micron CMOS process (Fig. 4.3(a)). As a second step, this 100 MHz signal is converted with a phase locked oscillator (PLO) by a factor of x128 resulting in the 12.8 GHz LO. The given PN_{multi} = -132 dBc/Hz (@ 10 kHz) of the multiplier at 100 MHz is going to result in a theoretically converted phase noise of PN_{conv} = -90 dBc/Hz (@ 10 kHz) for the 12.8 GHz signal. This is going to fulfil the requirements of the critical phase noise mask within the Eutelsat standard [Eut].

The circuit based on this schematic was designed while realising different external loop filters (18 kHz, 80 kHz) of the second PLO. Thus, the

(a)

(b)
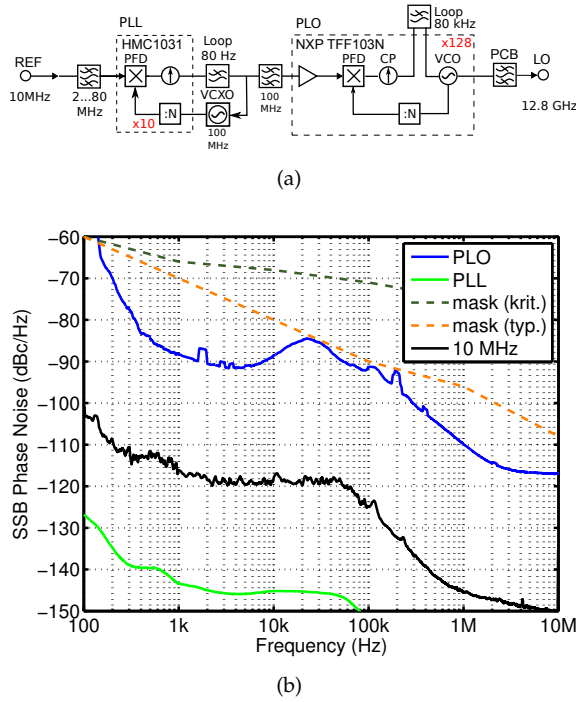
FIGURE 4.4: (a) Schematic of the two-stage PLO with its (b) measured SSB phase noise.

circuit was measured and is shown with its single sideband (SSB) phase noise in Fig. 4.3(b). It can be observed that the phase noise of the REF is PN_{REF} = -130 dBc/Hz (@ 10 kHz). The multiplied phase noise (in green) results in PN_{multi} = -118 dBc/Hz (@ 10 kHz) which is related to the theoretical assumptions. Furthermore, some spikes occur that rely on a non proper biasing of the circuit. The internal loop-bandwidth of the multiplier can be observed at 1 MHz due to an overshoot. This overshoot is further converted during the second stage PLO circuit, to an increased phase noise in the range between 10 kHz and 1 MHz – clearly breaking the mask. The measurements indicate that the phase frequency detector (PFD) of the PLO suffers from a high residual phase noise at 12.8 GHz. Increasing its loop bandwidth results in a decrease of the low frequency SSB. An increase of the loop bandwidth towards higher frequencies is not possible due to the overshoot of the first multiplier at 1 MHz.

Two-stage PLO

Within a second topology (Fig. 4.4(a)) the first multiplier is replaced with a conventional PLL. It consists of a PFD including a fixed division ratio of x10 and an external voltage controlled crystal oscillator (VCXO). It is possible to circumvent a high phase noise coming from the REF input. Furthermore, the loop bandwidth of this PLL can be set to extremely low values (80 Hz) based on low charge currents of the PFD. Now the loop bandwidth of the second PLO can be set to high values (80 kHz) to lower its effect of the PFD residual phase noise. The resulting total phase noise is shown in Fig. 4.4(b) and fulfils the typical and critical Eutelsat mask [Eut]. It should be mentioned that these measurements were taken with an even worth REF that only achieves PN_{REF} = -120 dBc/Hz (@ 10 kHz). Nevertheless, the first PLL is able to lower this input to PN_{PLL} = -145 dBc/Hz (@ 10 kHz) for the 100 MHz signal by using its own VCXO. The resulting phase noise at 12.8 GHz based on the PLO now clearly fulfils the mask while the internal loop bandwidth of 18 kHz shows a little overshoot.

PLO Amplifier

The differential output power level of the PLO is in the range of -6 dBm at V_{cc} = 3.3 V. To achieve an appropriate driving level for a mixer, the LO is boosted via a narrowband p-HEMT amplifier (BFU730) that is already packaged and gets matched on the RO4003c substrate. The amplifier has a 10 dB gain with a P_{1dB}=16 dBm. In addition to the narrowband character of the driving amplifier, this LO is filtered with a coupled short stub filter to further lower possible side-band products within the LO signal as can be seen in Fig. 4.5(a). It compromises between losses and side-band attenuation. Therefore, only one section was used with short ended stubs to increase the unloaded Q of the pole.

Up-Conversion

The up-conversion is carried out via a double balanced IC mixer (TGC2510) based on a GaAs p-HEMT process. It includes a buffer amplifier as well as an image rejection based on a fully differential IF input. The output TOI is $33\,dBm$ with a conversion gain of $17\,dB$. The p-HEMT process allows a biasing of up to $V_D = 5\,V$, even though all parts of the circuit need separate biasing (e.g. LO buffer, RF output, control voltage as well as a voltage reference). In addition, an LO-nulling technique was applied via the biasing of the differential IQ IF inputs. As described in [Bal+02], high precision mV supplies were designed based on operational amplifiers that were capable of providing $\pm 0.01V$ individually for the I and Q input of the mixer. Thus, the LO reduction at the RF output port was minimized to $\geq 40\,dBc$ within F_{Ku} for various output power levels.

4.2   Hybrid Filter

The filter in the uplink path must be able to eliminate the crosstalk between the TX-band (13.75 - 14.5 GHz) and the close RX-band (10.95 -12.75 GHz). Despite effort being spent on reducing the LO, in between the TX and the RX bands the f_{LO} = 12.8 GHz needs to be suppressed as well (Fig. 4.6). A proper working filter design results in a high spectral purity of the whole BUC. Filter design in a BUC for a *Ku*-band uplink path are traditionally made by coupled wave-guide cavities. However, they are rather big and difficult to implement in the PCB design. Coupled line filters have been widely used to achieve narrow FBW because of their relatively weak coupling. A good repetition of these filters is achievable with an easy synthesis procedure [Poz05]. A low loss behaviour is possible by choosing low $\tan\delta$ as well as a high electrical conductivity (σ) in combination with a low roughness (Ra) for the substrate. Nevertheless, hybrid filter design at these frequencies compromises the better rejection, leading to a high number of resonators and a low insertion loss.
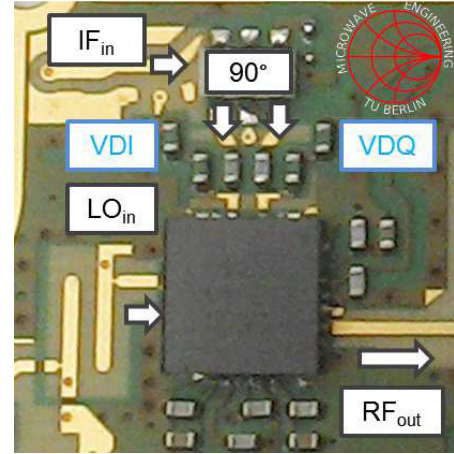
(a)
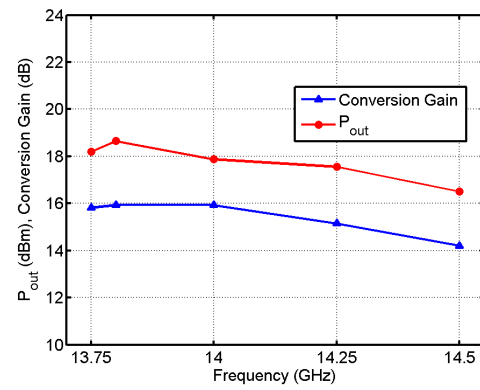
(b)

FIGURE 4.5: (a) Layout of the up-conversion with its (b) measured conversion gain.

Furthermore, the group delay needs to stay constant within the pass-band and should not exceed a value of $\approx 1\,ns\,pp$. Often edge-coupled filters produce the longest delay in a complete uplink path and the value increases even more with the filter order. Those tough requirements can be extended by the need for a harmonic suppression at two times the centre frequency ($2 \cdot f_0$).

Al_2O_3 TX Filter

The results of the substrate analysis in section 2.1 show that there are several limitations on the unloaded Q of a $\frac{\lambda_0}{4}$ resonator. The highest Q was obtained by a rather thin Al_2O_3 alumina substrate with $h = 127\,\mu m$ and an $\varepsilon_r = 9.9$. Therefore, the TX filter design starts on this substrate and was partially published in [Maa+16c].
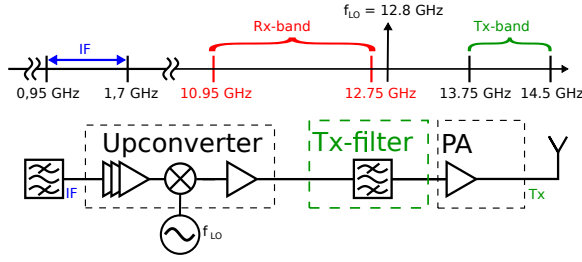
FIGURE 4.6: Transmission spectrum of the proposed transceiver in the *Ku*-band and block diagram of the up-conversion path.

FIGURE 4.7: Comparison between measurement and simulation of the proposed hairpin filter.

A band-pass filter (BPF), with the 5% FBW specifications located at 14.125 GHz, can be realised by either combining a low-pass (LP) and a high-pass (HP) or using resonant structures like quarter-wave coupled lines. Resonant structures are preferable in the case of size and PCB manufacturing issues and are then connected either capacitively or inductively. All filters are designed based on the commonly known equations depicted by Matthaei [Mat+85]. Thus, an appropriate schematic design is realised in *CST Design Studio ^{TM}* including common parasitic behaviour of edges, coupled lines and open end effects. The design is afterwards optimized and transformed to a layout, which is analysed via a full 3-D time domain EM-solver. Within the following subsections four topologies of filter were selected and later on designed. Different numbers of the coupled line sections were used while their FBW remains constant.

Coupled Line Filter

A coupled line filter (CLF) (Fig. 4.8 (b)) is an easy filter type of combined resonators. The length of one coupled line (CL) is $\frac{\lambda_0}{4}$ and within this work combined to three resonators to realise a moderate 3rd order filter with low insertion loss. The outer CLs are strongly coupled and the inner ones weakly coupled. It is intended to have a high FBW just around f_0 to get a flat as possible group delay.

Hairpin Filter

Within the hairpin filter (Fig. 4.8 (a)) the CL pairs are connected with uncoupled lines to realise the

folding. As a consequence, this results in a self-coupling of the resonator that decreases the filter bandwidth and increases the losses. The open-circuit resonators reduce the free-space radiation by the phase cancellation at its end. At high frequencies the bend discontinuities become dominant. What is more, it is the effect of folding the resonator which does not decrease the size (weak-coupling) [Mal04]. The spurious mode occurs at twice the pass-band frequency and can only be lowered by equalizing the even- and odd-mode phase constant (β_e, β_o) of the coupled resonators or changing the length of the input/output lines to $\frac{\lambda_0}{8}$ [Mal04]. To achieve a harmonic suppression the coupled lines are over-coupled to an electrical length of 130°. The pass-band response is not effected by this, since the derivative of the coupling response is zero at f_0. This over-coupling extends the phase length of the odd-mode like in [Rid88], [Kuo+03] and results in a suppression of ≥ 20 dB for the second harmonics. It is also well known that increasing the Image impedance of coupled lines equalizes β_e, β_o as well. The high ε_r of the used substrate in combination with the low thickness will result in thinner lines that exceed the manufacturing tolerances and are therefore not used. Both input and output lines are tapped to improve the matching.
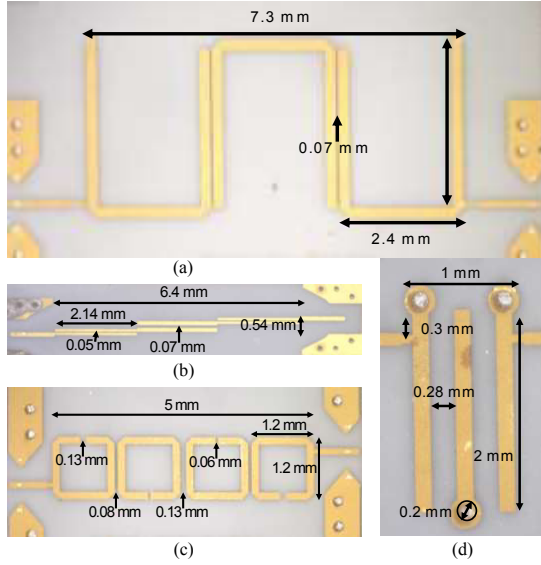
FIGURE 4.8: Pictures of the realised filter on alumina substrate (a) hairpin (b) CLF (c) ringresonator (d) interdigital.

Ringresonator Filter

The ringresonator, or open-loop resonator, can be seen as four resonators (1-4) that are directly coupled like in Fig. 4.9(a) (Realisation in (Fig. 4.8 (c))). It's behaviour is like the hairpin filter whereas the self coupling is increased due to the closer ring. The additional capacitive coupling of the open-ended lines result in a flatter response. Due to the high self coupling, of the ring, the CL cannot be over-coupled without changing the pass-band frequency. A harmonic suppression can therefore only be realised by equalizing the even- and odd-mode impedances (Z_e, Z_o). However, this approach cannot be realised due to the manufacturing constraints. A combination of open-loop resonators that are inductively, capacitively or mixed coupled can also lead to a harmonic suppression [Poz05].

Interdigital Filter

Interdigital filters (Fig. 4.8 (d)) are known to have multiple-order poles of attenuation at the fundamental and second harmonic. The lines operate as impedance transformer and are therefore coupled transformers and not coupled resonators. This filter does not have any even harmonic spurious

transmissions. Furthermore, the bandwidth can be as narrow as 1%. The difficulties regarding an interdigital filter rely on the manufacturing and the ground inductance of interconnection, which is necessary at the end of the stub. The ground inductance of a via is therefore studied with a full 3-D EM-simulation. Afterwards, a model is inserted in the schematic at the beginning of the optimization process.

Experimental Results

All filters are measured via $500 \, \mu m$ pitch probes with a HP8510c. A GSOLT-calibration defines the reference plane to the probe-pads. With an additional second tier TRL calibration on the Al_2O_3 substrate the reference plane is shifted to the $50 \, \Omega$ input of the filter. Fig. 4.7 shows, as an example, the comparison between the measured and simulated hairpin filter. It can be seen that simulation and measurement fit each other well. The FBW of the measurement is slightly higher than simulated. The centre frequency is equal. The IL (S_{21} in dB) and RL (S_{11} in dB) are both as simulated. The harmonic suppression at $2 \cdot f_0$ is a bit less than simulated but still ≥ 20 dB.

As shown in Fig. 4.9(b) all designed filters work in the frequency range of interest. The critical parameters are also compared in Tab. 4.1. The CLF has a low IL and a low suppression of the f_{RX} as well as the f_{LO}. The three other filters all derive benefits from their higher Q which helps to fulfil the specifications (dotted line) from Fig. 4.6. All filters have an IL ≤ 2.2 dB. Only the RL of the hairpin as well as the ringresonator filter is good with ≥ 17 dB. The interdigital filter has the weakest matching of only ≈ 10 dB due to its shortened stubs. A harmonic suppression can only be seen, as designed, for the hairpin filter of ≥ 20 dB and the interdigital filter of ≥ 42 dB. For the others, additional low-pass filters could be added.

The CLF has the lowest as well as the flattest group delay with 0.2 ± 0.03 ns (refer to Fig. 4.9(d)). The interdigital filter has a surprisingly flat group delay of 0.48 ± 0.03 ns in the frequency range of interest,
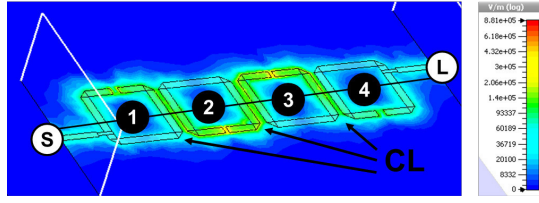
(a)
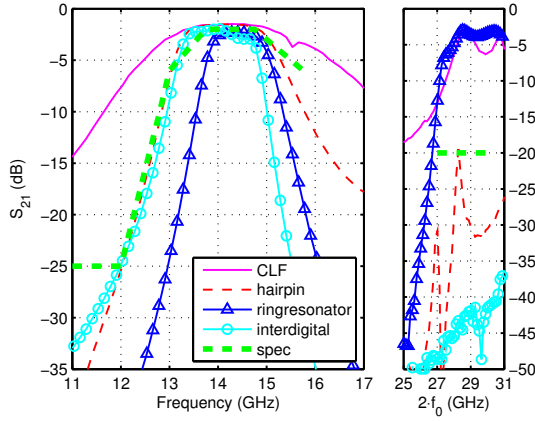
(b)
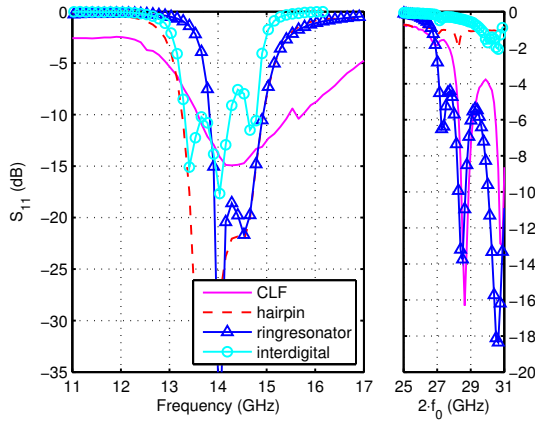
(c)
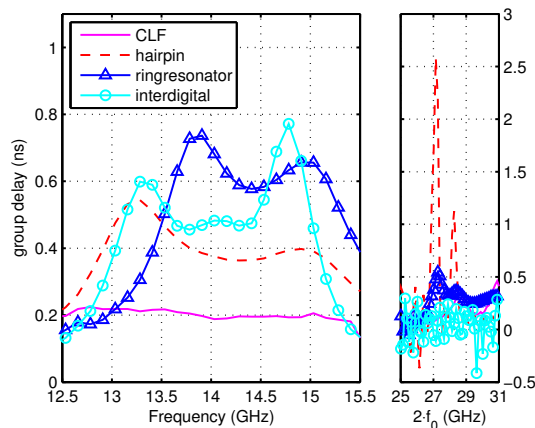
(d)

FIGURE 4.9: (a) 3D view of the ringresonator filter in CST with the appropriate coupling structure of the four resonators, source and load. (b) Measured transmission and (c) reflection, as well as (d) group delay results for the designed filters.

while the hairpin filter has $0.38 \pm 0.04\,\text{ns}$ around $14\,\text{GHz}$. In spite of the highest group delay with the biggest variance, the ringresonator filter has to be declared with $0.64 \pm 0.06\,\text{ns}$.

RO4003c TX Filter

The realised TX filter on AL_2O_3 works well for the defined requirements. However, interconnection losses between the components of the transceiver and the filter will be dominant in the case of choosing a second substrate only for the filters.

Ringresonator Filter

Based on this preliminary analysis a combination of a ringresonator and an interdigital filter is designed and realised directly on the lower unloaded Q RO4003c LoPro substrate (Fig. 2.4(a)) and is shown in Fig. 4.10(a). The shortened stub behaves as a feeding resonator with a higher Q than the normal open-stub of a hairpin. Special care was taken to determine exactly the ground inductance of the via holes by a full 3D EM simulation. In addition, two MS rings build a 4 pole section. So the increased self coupling of the rings interact with the feeding resonator. The harmonic suppression is realised by the construction of the poles.

SIW Filter

By far the best quality factors can be achieved by using coupled wave-guide cavities. Substrate integrated wave-guides (SIW) can be used to ease the integration of these cavities and to lower the dimension. Therefore, a SIW-filter containing five cavities is realised in [Rau+16b] and shown in Fig. 4.10 (b). Especially the high Q of the SIW cavities are a great example for lowering the LO frequency within the TX output spectrum as shown in Fig. 4.10 (c). This figure displays a comparison of both realised filters which were designed to perform with an almost equal FBW. It needs to be pointed out that the compared IL describes the reference plane related to the MS line not to the SIW plain, which would be far less. Effort was spent

TABLE 4.1: Comparison of realised *Ku*-band filters

	f_L 3 dB (GHz)	f_U 3 dB (GHz)	FBW 3 dB (%)	Q 3 dB	IL (dB)	RL (dB)	f_{RX} att. (dB)	f_{LO} att. (dB)	$2 \cdot f_0$ att. (dB)	group delay (ns)	Size (mm^2)
[Riu+05]	13.25		11.3	2.1	8.8	12	35*				29
[Li+08]	16.57		17.7		5.6	14.5					77.7
[Shi+10]	13.97		20	1.7	4.9	17		4.5			54
[Man+09]	12.5		18	4.6	5.4		40*				190
Al_2O_3											
CLF	12.5	16.16	28.6	3.8	1.5	13	7	2.7	3	0.2	18
hairpin	13.1	15.2	14.8	6.7	1.5	20	25	11	20	0.38	16
ringresonator	13.7	15.1	9.7	10.2	2.2	17	40	27	3	0.64	17.5
interdigital	13.2	14.78	11.2	8.85	1.9	10	20	14	42	0.48	9
RO4003c											
ringresonator	13.7	14.5	5.6	9	4.5	10	32	23		0.36	36
SIW [Rau+16b]	13.4	14.75	7.5	13.3	4.5	17	≥ 40	30		1±0.03	776

*This filter has a different centre frequency so the distance to f_{RX} is referenced and used

on optimizing the high impedance MS line transition to the low impedance SIW and up to 20 dB RL was achieved in [Kon+16]. Nevertheless, the transition losses from MS to SIW are that high that they significantly affect the total IL.

Furthermore, the IL of both filters are highly related to the $\tan \delta$ of 0.0027 of the substrate and the conductive losses based on the roughness. In the ringresonator only the top roughness of the substrate is important, whereas in the SIW the roughness of the metallized vias as well as the MS to SIW transition is significant. In addition, the low thickness h of the substrate increases the conductive losses of the SIW as well as the ringresonator.

Summary

Four different coupled line filter topologies are designed and measured on a Al_2O_3 substrate. All designs show a good agreement between simulations and measurements and are suitable for their application as a TX-filter in the up-conversion path of a *Ku*-band BUC. Compared to the published work (Tab. 4.1) the commonly used topology is a hairpin filter. The results of this work are like [Riu+05], [Li+08] and [Man+09] but with a lower IL and a harmonic suppression. [Shi+10] uses split-ring resonators in combination with a low-pass to realise a bandpass characteristic. Its low IL of 1.7 dB with

the higher FBW can therefore not be reached by the ringresonator filter of this work. The interdigital filter has a low FBW as well as low IL in combination with the highest harmonic suppression and the smallest size. Its the preferred choice of filter in between amplifier stages, where its low RL is not a hindrance. A developed SIW filter shows excellent filter parameters but due to its large size a realisation was impractical. A combination of the interdigital filter and the ringresonator was finally realised on a RO4003c substrate fulfilling all requirements of LO, RX suppression as well as the bandwidth, which is why it is used further on.

4.3 Amplifier

Dual Directional Coupler

A dual directional coupler was developed to determine the forward and reflected power level within different stages of the BUC. Realised on a RO4003c, it compromises between losses and bandwidths as already described during the previous filter analysis. The coupler should be located among different positions of the BUC, being so small as not to occupy more space than a necessary TL would take. As a result, only a weak coupling can be realised to lower the influence of the coupling path to the

(a)

(b)

(c)
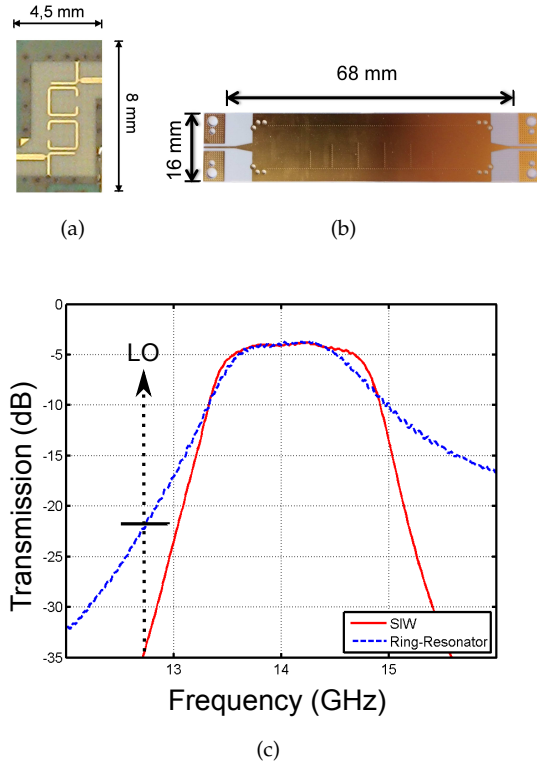
FIGURE 4.10: (a) Layoutview of the ring resonator, the (b) SIW Filter as well as (c) the measurement results obtained.

(a)

(b)

FIGURE 4.11: (a) Layoutview of the realised dual directional coupler (b) measurement results.

main line. A common dual directional coupler consists of a main line with two coupled lines along it. The length of the coupling lines determine the frequency range while the distance to the main-line influences the coupling.

For a centre frequency of 14 GHz the length should be $\frac{\lambda_0}{4}$ which is 4.5 mm. It can be shown that equalizing the electrical length of the even and odd mode for this coupler needs to be done to improve the directivity of the coupler [Mar82]. In [Zha+15] this technique is applied by using interdigital fingers at the edges of the coupled line, which locally introduce capacitance. Interdigital fingers are not only used at the edges of the coupling lines but also in between. The coupler is shown in Fig. 4.11(a) with additional coaxial connectors to ease a separate measurement. One coupled path ends at a coupler while the other one feeds a Wilkinson splitter. This splitting is necessary for the output side of the BUC to simultaneously use the forward power (FWD) for a down-conversion as well as a continuous power measurement with a power detector.

The reverse power (REV) is later on connected to another power detector.

From Fig. 4.11 the measured S-Parameters can be obtained, while the connectors are de-embedded. An IL of 0.45 dB is measured for the 4 mm structure with additional 1 mm 50 Ω MS lines (right Y-axis). The RL for the input as well as output is equal and ≥ 20 dB for F_{up} (left Y-axis). At the coupling port an FWD = -40 dB and a REV = -66 dB coupling can be determined. The REV can be seen as isolation – leading to a calculated directivity of ≥ 20 dB for F_{up} (right Y-axis). One may conclude that the directivity limits the detectable VSWR to 1:1.22 but a higher selectivity would lead to an even higher IL by the cost of output power.

Pre-Amplifier

A multi-stage 20 V GaN-HEMT pre-amplifier IC (TGA2958SM) is used to increase the P_{out} from the up-conversion to 32 dBm to be able to saturate the PA. The pre amp achieves a PAE of 25% that results in a $P_{diss} = 5$ W which needs to be cooled at the bottom of a 4x4 mm QFN package. The pre-amplifier
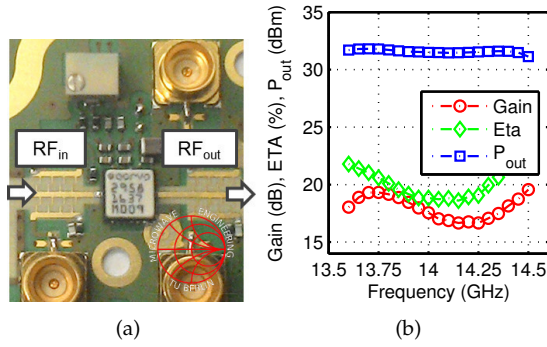
FIGURE 4.12: (a) Layoutview of the realised pre-amplifier with hybrid dual directional couplers and (b) measurement results with de-embedded connectors.

was measured with on-board dual directional couplers as can be seen in Fig. 4.12(a). CW measurements of Fig. 4.12(b) visualize the achieved output power of $P_{out} \geq 31$ dBm for the target frequency range F_{up}.

Power-Amplifier

To implement the designed MIC PA Ku_{up} from Sec. 3.3 into the BUC, a cavity was left with the mechanical dimensions of the PA. The PA is positioned in the cavity as a drop-in circuit. A side-view of the stack can be seen in Fig. 4.13. This way, the interconnection between the top metallisation on the RO4003c (cond1) and the metallisation on the AL_2O_3 is realised via $100\,\mu m$ wide gold ribbons. The gap in between both substrates leads to an inductive connection for the ribbon as well as the GND interconnection. So, this inductive ribbon needs to be compensated via a capacitive post or open-stub at the RO4003c side of the substrate. This compensation network is measured separately by a drop-in circuit that only consists of a $50\,\Omega$ ML and states 20 dB RL within F_{up}. By de-embedding the losses of the MS line the IL is determined to be 0.3 dB which depends on the positioning accuracy of the drop-in circuit. In addition, GND ribbons between both substrates were added. Besides this RF_{in}, RF_{out} feeds the biasing is realised via silver ribbons that can be easily attached by soldering. The CuMoCu flange is connected to the Al-housing
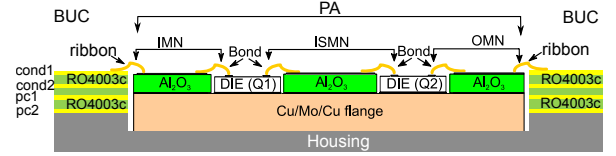
FIGURE 4.13: Integration of the designed MIC PA into the hybrid stack.

via screws to provide the best thermal connectivity where simulation indicates an $R_{TH} \leq 0.3$ K/W. The MIC PA can be scaled in output power between $P_{out, peak} = 25$ W [Maa+16a] using the smaller bare-die (CGHV1J025D) or $P_{out, peak} = 70$ W from Sec. 3.3 [Maa+17a] because both MICs are designed for the same mechanical dimensions and the same positions of the pads.

Linearisation

This section extends the results already published in [Maa+15a] by a complete implementation of a RF-linearisation within a BUC. Linearisation is nowadays a standard technique to compensate for the non-linearity of either an amplifier or a complete conversion chain for base-station applications (terrestrial broadcast, 3G telecommunication). A common method for compensating the compression behaviour of a PA is the usage of a digital pre-distortion (DPD) that can be included in the baseband digital modulation path and builds a gain expansion to achieve a linear output power behaviour [Fra+06]. For a DPD the processing power increases with the signal bandwidth. Unfortunately, the signal bandwidth of SatCom signals is rather high with up to 36 MHz[1] compared to, for example WCDMA or LTE signals with only a few MHz bandwidth. Apart from that, there is a lack of interconnection between the output of a BUC and the output of a modem as they are, based on the double up-conversion technique, located in different frequency ranges.

To overcome this problem, a so-called RF pre-distortion (RFPD), which filters the non-linearity as well as compensates for the memory dependants directly within the RF domain, can be a solution as

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[1]36 MHz represents one transponder of a *Ku*-band satellite.
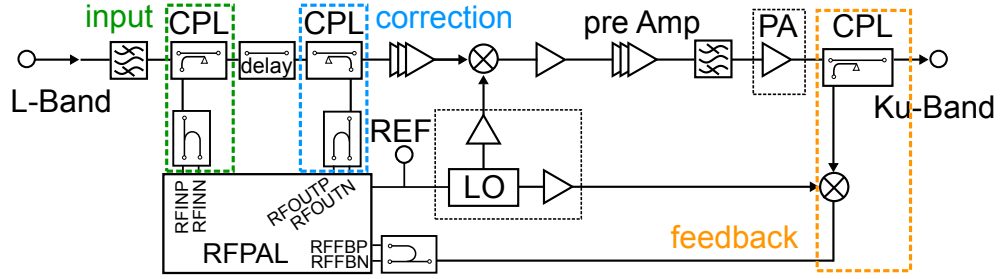
FIGURE 4.14: Schematic of the IF linearisation.

shown in [Kat+10], [Kat14]. RF linearisation techniques are already applied for TWTAs but only through the use of simple diode networks that expand the compression behaviour [Jie+15], [Vil+12]. Within this work, a RF pre-distortion is applied in the IF range (950-2150 MHz), instead of the RF path, as it was shown in [Ban+01] for OFDM signals.

The IF pre-distortion is realised with a RF PA linearisation (RFPAL-system) of Maxim Integrated™ (formerly Scintera™). Inside this IC an analogue linearisation takes place by dynamically enabling- or disabling filter coefficients [Rog13]. An input signal is compared to a feedback signal (from the PA output) in real-time and correction coefficients are applied towards optimized distortion.

Fig. 4.14 shows the schematic of the IF pre-distortion in which the input and correction coupler is placed in between the IF input and the IF up-conversion. A delay is necessary to compensate the processing time of the RFPAL IC that is fed back into the circuit via the coupler. At the output side of the PA the signal is coupled and converted back into the IF via a mixer. This way, the LO of the up-conversion as well as the down-conversion needs to be in phase.

The advantages of implementing this technique in the IF over the *Ku*-band are the lower losses and the commercially available RF-pre-distortion techniques from the telecommunication market. Moreover, the distortion of the up-conversion as well as the pre-amplifier, so the whole chain, is compensated. Additional distortion caused by the down-conversion mixer is negligible due to the low power level the mixer is operating. The

system is able to reduce the out-of-band energy by compensating non-linearities like AM/AM and AM/PM distortion as well as memory effects [Rog11]. The detection whether a signal is in-band or out-of-band relies on a live sampling of the signal and analysing its 10 dB slope. Furthermore, it automatically detects the IF as well as the bandwidth of the signal. The modulation type is not relevant for the RFPAL system. What is more, also multi-carrier signals can be applied. However, higher order modulation schemes will increase the error vector and side-band products, which makes an improvement more challenging.

Preliminary Tests

To get adequate measurement results, the linearity of the system with the combined hybrid GaAs PA from Sec. 3.1 was proven with (w) and without (w/o) the RFPAL-system based on measurements of the error vector magnitude (EVM), the resulting constellation diagram, and the spectral regrowth of the output signal. The output signal was therefore measured in the *Ku*-band to eliminate measurement failures that rely on a down-conversion. A signal with a 8PSK modulation and symbol rates from 10 MSym/s to 30 MSym/s (13-36 MHz) with a PAPR of 3.7 dB was chosen.

The output power spectrum of the BUC is shown in Fig. 4.15. It can be seen that a massive improvement of the shoulder distance can be realised by the pre-distortion for a constant output power of 37.5 dBm. This improvement was equal over all measured frequencies within Ku_{up}.
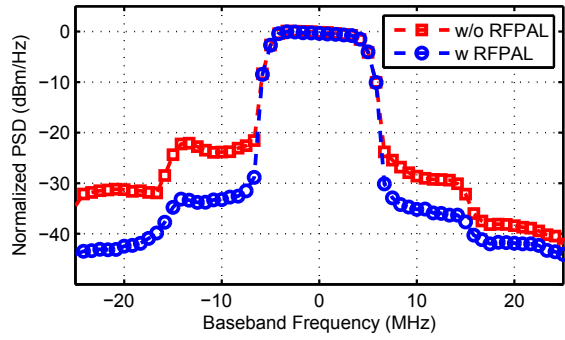
FIGURE 4.15: Normalised output power spectrum of the BUC at 14.35 GHz centre frequency with P_{out}=37.5 dBm. A 10 MSym/s 8PSK signal with 3.7 dB PAPR is used and measured with RBW=300 kHz; RMS; VBW=3 MHz; 2 s sweep; 100 MHz span.

FIGURE 4.16: Measured output constellation diagram for a 10 MSym/s 8PSK signal with 3.7 dB PAPR at P_{out}=36.7 dBm with a running RFPAL.

On the left shoulder the RFPAL-system improves the ACPR within 9.8 dBc, whereas the improvement on the right shoulder is only 7.7 dBc. The spectral regrowth is asymmetric over the channel frequency band, which indicates a group delay problem of the up-conversion as well as the feedback channel. Moreover, a base-band problem can cause this asymmetric response. Nevertheless, an improvement of the spectral regrowth can be noted almost independently from the symbol rate (Tab. 4.2). Due to the good results, the failure of the feedback path, caused by the down-conversion distortion, seems to be negligible. The output constellation diagram shows a good EVM improvement of at least 3 % over different symbol rates. A screen shot of the constellation diagram is shown in Fig. 4.16.

TABLE 4.2: Measured average output power, EVM and minimum ACPR level ($BW + 0.5\,MHz$), without (w/o) and with (w) RFPAL at 14.35 GHz for 8PSK modulation

	P_{out} (dBm)	EVM (%)		right ACPR (dBc)	
		w/o	w	w/o	w
10 MSym/s	36.7	6.1	3.1	-25.4	-37.6
10 MSym/s	37.5	6.9	4.1	-23.3	-31.0
20 MSym/s	37.5	12.0	9.1	-25.6	-33.1
30 MSym/s	37.5	21.4	18.2	-26.9	-30.3

Implementation

To implement this technique within the BUC a few constraints needed to be faced. Firstly, all the differential IF inputs of the RFPAL IC are originally used narrowband (e.g. 1400-1800 MHz), while internally the IC is able to work between 225-3800 MHz. To be able to use the whole IF range (950-2150 MHz) without changing the layout, new coupling as well as balancing circuits needed to be investigated. Secondly, a high directivity of the couplers must be granted as well as a flat IL over the whole system. For this extended bandwidth wire wound coupled air coils as SMD components are used (TCD-9-1WX+). The increasing losses towards the higher IF are compensated using a low slope high-pass circuit, as can be seen in front of the coupler in Fig. 4.17(a). Baluns were realised with LTCC multilayer circuits offering a good phase equality over the IF. The differential IF inputs are not strictly 100 Ω rather than a complex varying load that needed to be matched to the opposite facing term of the balun as well as the couplers. As an example, the matching between the differential in- and outputs of the IC to the balun is visualized for the IC output side in Fig. 4.17(a). An additional dc-feed is necessary to bias the CMOS output drivers and supplied via the cold-point of the balun. By applying this technique the RFPAL is easily matched to the required bandwidth.

To equalize towards an optimal SNR at the inputs of the RFPAL IC, additional variable gain amplifiers (VGA) were used to either boost or decrease

(a)

(a)

(b)
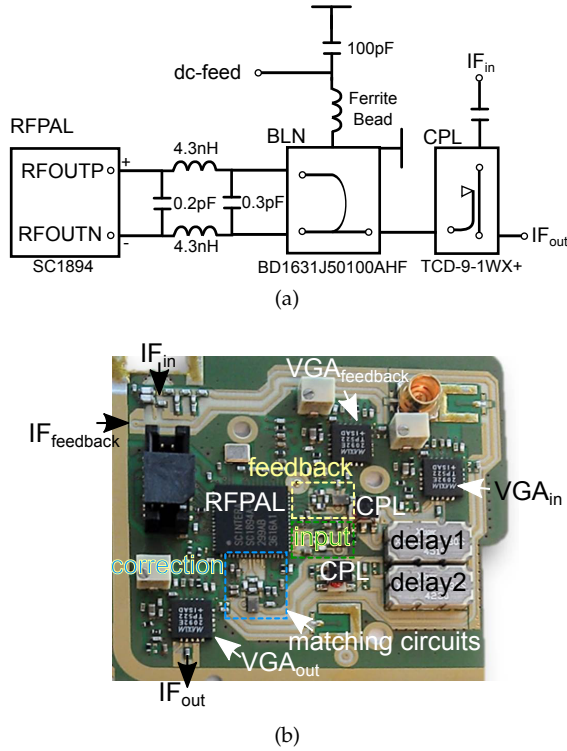
FIGURE 4.17: (a) Schematic of the linearisation matching circuits (b) Layoutview of the realised IF linearisation implemented in the BUC.

(b)

FIGURE 4.18: (a) Schematic view of the realised dc/dc conversion with (b) a layoutview.

the input power as well as the feedback power. In addition, one VGA is used at the output side of the RFPAL IC to match the level to the input of the up-conversion. The layout-view of the IF linearisation can be seen in Fig. 4.17(b).

4.4 dc/dc Conversion

Within the BUC there are in total 29 different potentials that need to be supplied to the different circuits. A range of different voltages and currents need to be biased while only the drain-supply of the PA is fed, directly coming from the connector dc-in via a switching FET (Fig. 4.18(a)). Coming from the connector, a first integrated step-down converter (LTC3649) switches the voltage to 20 V, which is the drain-supply for the pre-amplifier. An additional converter (LT8601) aligns the 20 V to 5 V, 3.3 V as well as 1.8 V, which are necessary for driving the up-conversion, the LO generation as well as the linearisation circuit. During the start-up sequence only the 3.3 V are biased to detect whether

a 10 MHz REF is connected or not. The power consumption of this stand-by mode is therefore only 1.5 W.

By applying the REF, the first PLL of the PLO is able to lock and therefore the LCKDET signal gets high. This LCKDET signal starts a sequence by first switching the 1.8 V, followed by the 5 V (Fig. 4.19(a)). Within a charge-pump the positive 5 V supply is afterwards converted to a -5 V supply that is used with operational amplifiers to realise the negative gate supply for all *normally on* devices (up-converter, pre-amplifier, PA). To prevent the self-destruction of these devices their drain-supply is switched off during the start-up sequence by a p-MOS switch (Si3127) triggered by NEGDET (Fig. 4.19(b)).

Baseband Impedance

The previous analysis regarding linearity of the GaN-HEMT process, in Sec. 3.2.4, showed that the influence of a well-chosen baseband impedance on the intermodulation distortion cannot be neglected, while the influence at the drain-side dominates the gate-side due to the effects of a stability
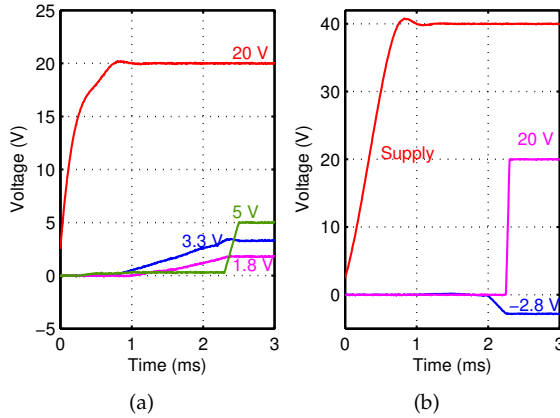
FIGURE 4.19: Measured starting sequence for the dc/dc conversion with (a) the connector injection and (b) the PA bias.

FIGURE 4.20: Measured reactance of four parallel dc-feeds.

resistor. In general, the dc-feed of an amplifier should provide an open circuit for the frequency range of usage. Within this work, this is realised by $\frac{\lambda_0}{4}$ lines located on the MIC substrate in combination with a radial stub. This enables a sufficient RF/dc isolation within the bandwidth of operation. The interconnection from this ended structure to the surrounding substrate is realised via gold ribbons that introduce an additional inductance to the path. Beginning on this surrounding structure, the RF blocking is extended by additional capacitors that typically increase with size within decades (e.g. $1 \, \text{pF}$, $10 \, \text{pF}$, $100 \, \text{pF}$, $0.1 \, \mu\text{F}$ ...). The failure of this *classical approach* is located within the resonances of this structure. The increasing distance between the capacitor (and therefore the inductance) introduce resonances in the overall blocking structure. Furthermore, modern multilayer SMD capacitors are pursuing for higher quality factors that sharpen these resonances. They are titled low equivalent series resistance (ESR) which defines the inner resistance and therefore the amount of dissipated power. By eliminating these resonances within the baseband frequency range as well as its harmonics, the IMD can be improved [Sri+08].

The new design approach of the biasing circuits is defined as follows:

- $\frac{\lambda_0}{4}$ lines with radial stub provide RF/dc isolation in band

- a small SMD capacitance with a low ESR

compensates for an inductive ribbon as well as feeding circuit next to the MIC

- one large SMD capacitance should provide enough decoupling for the IF range while its SRF is located away from operating frequency ranges

- the BB impedance response is not influenced by the previous capacitors and can take advantage of a non resonating large electrolyte capacitor as close as possible to the drain

However, it turns out that designing biasing circuits for a specific baseband impedance becomes difficult by the lack of measurement data for the blocking components. Therefore, measurements were carried out to enhance the S-Parameters provided by the manufacturer towards lower frequencies. In addition, these measurements were approximated by a discrete model to ease the simulations. Fig. 4.20 denotes the simulation of the complete dc-feeding circuit for a symmetrical bias of four drains in parallel. It can be seen that the first resonance of these bias networks is located at $\approx 300 \, \text{kHz}$ which is related to the resonance of a $470 \, \text{pF}$ electrolyte capacitor.

Later, the frequency range up to $36 \, \text{MHz}$ can be declared as the fundamental baseband frequency range. In here, no resonances should occur which tend to ring within intermodulation products. The denoted *classical approach* with the constantly increasing capacitance values shows at least two additional resonances located at 0.7 and $1.4 \, \text{MHz}$. The next resonance is located at $500 \, \text{MHz}$ which is

due to the high Q of a 100 pF capacitor used in the *classical approach*, while the *new approach* displays the same resonance but can take advantage of a low Q capacitor. Within the *Ku*-band the impedance is dominated by a $\frac{\lambda_0}{4}$ MS line with a radial stub that is equal for both approaches. The overall performance of the *new approach* is more flat without any disturbance. While applying this technique to the linearity measurements, which are described later on, an IMD3 improvement of up to 10 dBc was achieved. In particular, asymmetrical IMD products are highly related to resonances in the baseband impedances.

4.5   Realisation

Waveguide

With an increased operation frequency the common output connectors for BUCs are waveguides. For the *Ku*-band the WR75 rectangular waveguide dominates the VSAT market and enables low-loss interconnection from the BUC to the antenna feed. Two possible approaches of feeding a waveguide from a coaxial or MS line can be determined:

- A right angle (or orthogonal) transition interconnects the waveguide with a simple feed within the E-field maximum. A so-called *back-short* is positioned $\frac{\lambda_0}{4}$ away from the feed reflecting electromagnetic energy back to it. This results in a TE01 mode excitation orthogonal to the MS or coaxial feed. The transition represents an open circuit with the possibility of a low insertion loss interconnection.

- As an alternative, the in-line transition is realised by feeding the coaxial or MS line by a short circuit to the walls of the waveguide. The transition results in a slightly higher insertion loss caused by a field disturbance within the *back-short*.

The planar realisation of the BUC has to fulfil the mechanical constraints of feeding the antenna in an orthogonal way. In contrast, commercially available BUCs take advantage of the high power handling capability of an in-line transition, while in consequence, the waveguide connection is not located at the heat-sink side of the BUC. Within this developed VSAT the antenna should be considered as a possible heat-sink for the BUC. Therefore, the bottom of the BUC faces the back of the antenna, which both should provide the waveguide interconnection. Hence, the orthogonal transition is adopted via a hybrid MS feeding structure as described by Rautschke et al. in [Rau+17b]. Fig. 4.21(a) displays the top view of the rectangular WR75 waveguide. Within Fig. 4.21(b) the feeding structure of a MS circuit is obtainable and realisable as a drop-in circuit. The waveguide feed is a simple radial stub that reacts as a capacitive patch located at the E-plane of the waveguide. The cover of this transition can be depicted from Fig. 4.21(c) reacting as the *back-short*. An additional screw centred in the back-short is used to tune its distance to the feed.

Two of these transitions were interconnected at the MS reference plane and measured back-to-back feeding from the WR75 connection. The measurement is de-embedded via a second tier TRL calibration to the WR75 reference plane. By splitting the obtained T-Parameter, the S-Parameter results of Fig. 4.21(d) represent only one MS to WG transition. It can be obtained, that the IL = 0.65 dB is somehow constant over the frequency range of 10-15 GHz with a RL $\geq$ 20 dB. The IL is mainly related to the conductive losses of the long MS feeding line (Fig. 4.21(b)), which was necessary for positioning the mounting screws of the WR75 outside the housing of the BUC. Finally, the BUC can be either equipped with a SMA-connector[2] or this MS to waveguide transition, taking advantage of the same mechanical dimensions. The feed can also be realised for supplying to a lower height WG as described in [Oh+10] or by taking advantage of a SIW feeding structure as in [Can+15].

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[2]Rosenberger 32K242-40ML5

(a)   (b)   (c)

(d)
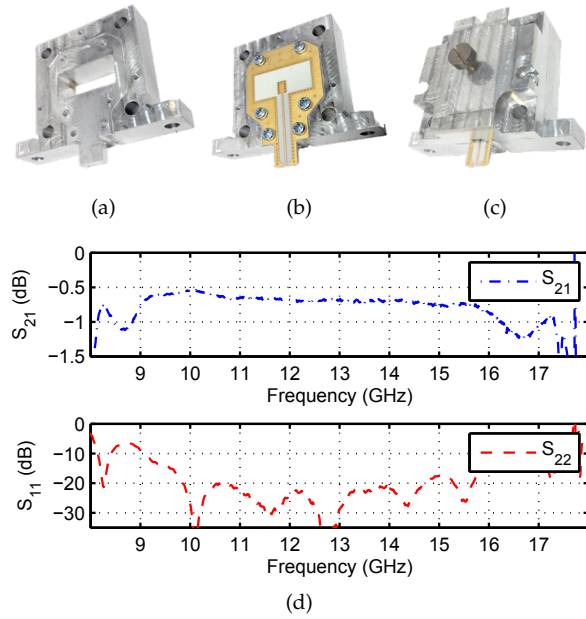
FIGURE 4.21: Top view of the MS to WR75 transition (a) housing (b) with substrate (c) including the back short (d) deembedded S-Parameter measurements of a transition.

Housing

By mounting the BUC on the backside of a planar antenna, one has to consider the weight the BUC adds to the antenna, changing its centre of gravity. Consequently, the pointing agility is lowered. The housing of the BUC compromises between cooling capacity and size/weight with a limitation of 1 kg. With a simple convection cooling, the thickness of the cooling-plate is calculated to 13 mm, giving the ability to spread the dissipated power to the side where additional heat sinks are located. Nevertheless, only a limited amount of dissipated power can be cooled with this thin housing, displayed in Fig. 4.22(b). For a dissipated power exceeding $P_{\mathrm{diss,max}} \approx 80 \, \mathrm{W}$ self heating will occur.

Fig. 4.22(a) shows the layout view of the BUC including the dc/dc conversion (A), a RF linearisation (B) and the up-conversion (C). In between the different sections a shielding wall is realised by a milled cover attached to via-walls in the substrate. The height of this shielding chambers is different for each chamber. Within the areas (A) and (B) the height of mounted components determines the minimum height of the chamber. Thus, the area (C)

(a)

(b)
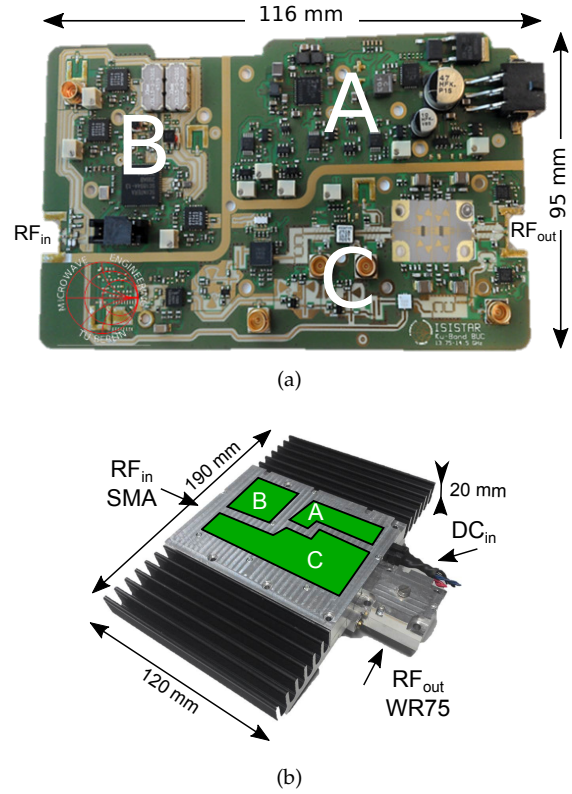
FIGURE 4.22: (a) Layout view of hybrid integrated BUC (b) with housing.

is the main high-frequency section including parts of the LO, the up-conversion as well as the PA. The height of this section is limited to the cut-off frequency of the highest *Ku*-band operation frequency. Eigen-mode calculations of this housing were carried out to prevent resonances caused by this shielding. The RF-interconnections between the sections (A, B, C) were realised in a lower layer (cond2). The MS line of layer "cond1" ends in a blinded via connecting to "cond2". Underneath the shielding a coplanar line with a reference GND on
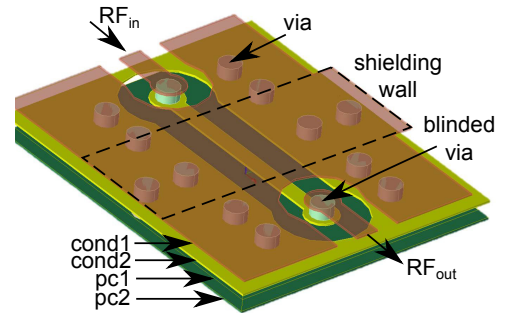
FIGURE 4.23: Layoutview of RF-interconnection underneath the shielding walls.
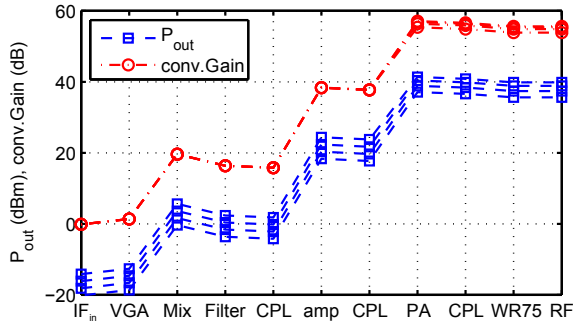
FIGURE 4.24: System simulation of the BUC for a varying input power level at the IF.

(a)

(b)

FIGURE 4.25: CW measurements of the BUC (a) in saturation with dependency to the frequency and (b) to the input power P_{in}.

top as well as on bottom is used (Fig. 4.23). Behind the shielding another blinded via returns the signal to the top layer (cond1). The diameter of the via ring metallisation was tuned as a capacitive post to resonate the via inductance. This RF interconnection was designed based on a time domain reflection (TDR) analysis and shows a measured RL ≥ 20 dB up to 4 GHz which is sufficient for the IF and REF interconnections. In a first approach, an RF-interconnection was designed using the same principles but up to the *Ku*-band frequencies which would enable a separate shielding of the up-conversion, LO as well as the PA section. Nevertheless, the uncertainty of the milling depth of the blind-via, which is $\approx 50 \, \mu m$, is degrading the RL of the interconnection for $f_0 \geq 6$ GHz, therefore this idea could not be realised.

The total size of the BUC including the housing is 190x120x20 mm with a weight of 950 g. Within the picture, the BUC is equipped with the 25 W PA. At the input and output of the layout-view the SMA connectors are missing because they were not part of the Reflow mounting process.

4.6 Simulation / Evaluation

The whole transmission chain of the BUC was analysed within ADS as a budget simulation. All components were adopted with characteristic equivalent values to ease the simulation. For example, the complex large-signal simulation of the PA can be replaced by a simple model that consists of the S-Parameters, the saturation power, and the gain

compression. Furthermore, the frequency generation can be replaced by an ideal source with a limited phase-noise and a mixer with an ideal conversion gain paired with second and third order intercept point definitions. A budget of the signal chain can thus be evaluated like for the output power and the conversion gain as shown in Fig. 4.24. All lossy networks, like the filters or couplers, result in a decrease of power level or a reduction in gain. Overall, a conversion gain of up to 55 dB can be obtained from this simulation. It can be seen that an increased IF input power to - 14 dBm is going to saturate the PA which results in a decreased conversion gain. Nevertheless, an output power level of up to 42 dBm for the 25 W PA was achieved during simulation.

For increased accuracy within system simulation, the complete transmission chain could be analysed within *ADS System-View*[TM] but therefore all sub-elements needed to be characterized non-linear on their own, which exceeded the time-frame of this development.
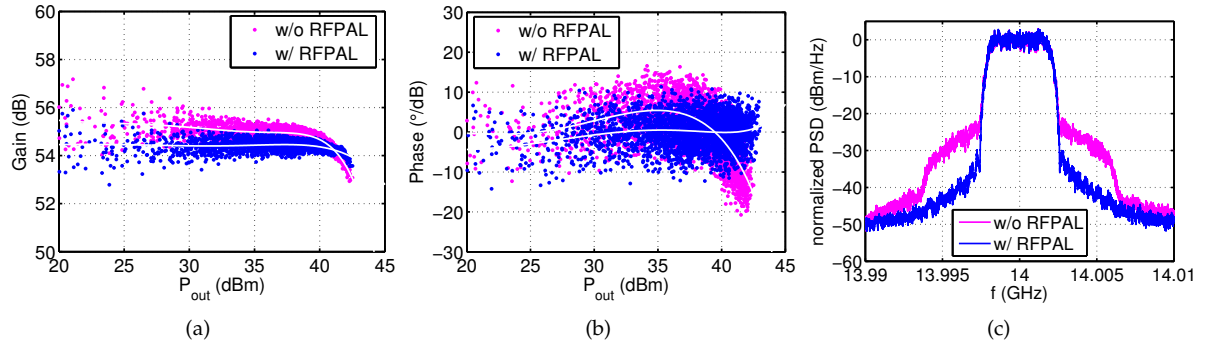
FIGURE 4.26: Measured output of the BUC (w) and (w/o) linearisation for (a) gain compression (b) AM/PM (c) spectrum for $P_{out,\,avg}$=39 dBm, 32APSK 4 MSym/s.

BUC with 25 W PA

As previously described, the BUC can either be equipped with a 25 W or a 70 W PA. So the evaluation and measurement is split into two parts. The BUC performance is analysed based on continuous wave (CW) measurements in Fig. 4.25(a). A very flat conversion gain of 55 ± 0.3 dB between 13.8 to 14.5 GHz can be seen with an output power higher than 39 dBm. The total efficiency exhibits 15%. The power consumption in saturation is only 52 W due to the implementation of high efficiency dc/dc step down converters.

Fig. 4.25(b) shows a constant power compression starting from P_{in} = -24 dBm to P_{in} = -17 dBm, resulting in a gain decrease from 60 to 55 dBm, which is typical for GaN technology (soft compression). It has to be mentioned that the PA can be operated in the deep compression of $P_{out,\,peak}$ = 39 dBm even though it is the 5 dB compression of the BUC, with a rather low increase of IMD products compared to GaAs or TWTAs.

Nevertheless, based on Eutelsat regulations, a BUC's operation has to be limited to its 1 dB compression by the fear of increased IMDs. The normal procedure of levelling a VSAT is that the satellite operation control increases the input power of the BUC within 1 dB steps upon the point where the measured output power (in the link) no longer increases in 1 dB steps. Even though a BUC is able to deliver **linear** higher output power levels, the control centre will not allow it through this obsolete procedure.

Compression

Biasing the PA in the **Class-AB** operation leads to an increased soft compression. By biasing the PA with a lower quiescent current its compression decreases as already shown in Sec. 3.3.5.

The compression behaviour is shown in detail in Fig. 4.26(a) for a 32APSK modulation (PAPR=6.4 dB) with a deep Class-AB to Class-C biasing. The gain compression is already flattened compared to the CW measurement (Fig.4.25(b)). The higher PAPR of the modulation limits the thermal compression of the PA that can additionally lead to a behaviour that is misunderstood as soft-compression. By enabling the linearisation system, the trendline of the gain compression is further reduced (Fig. 4.26(a) (w) RFPAL). The deeper Class-C biasing results in a slight overshoot of the AM/PM behaviour for the plot (w/o) RFPAL in Fig. 4.26(b), while (w) RFPAL the phase can be flattened.

By comparing this AM/PM plot with the one originally obtained for the stand-alone PA it needs to be mentioned that the spread of the phase points is wider in here. This can be explained by the higher amount of phase noise within the BUC compared to a laboratory signal generator. The output spectrum plot in Fig. 4.27 clearly shows the improvement of the out-of band energy (w) RFPAL enabled.

As can be seen in Fig. 4.27(a) the implemented RFPAL is able to reduce the ACPR of a 1.5 MSym/s QPSK within 5 dBc to 35 dBc for $P_{out,\,avg}$ = 39 dBm. While the BUC w/o RFPAL is already able to fulfil
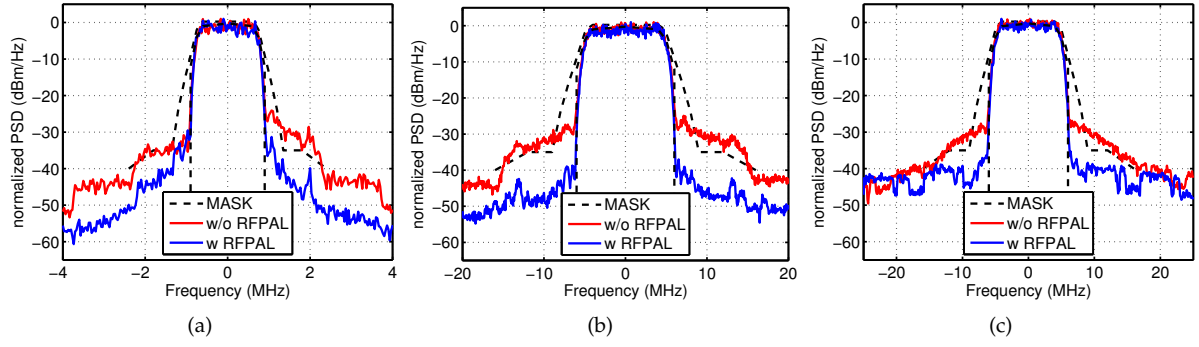
FIGURE 4.27: Normalized measured power spectral density of the BUC (w) and (w/o) linearisation for (a) QPSK 1,5 MSym/s (b) QPSK 10 MSym/s (c) 16APSK 10MSym/s for $P_{\text{out, avg}} = 39$ dBm.

the mask at saturated output power, the BUC (w) RFPAL is able to hold the more stringent military restrictions. The improvement for a 10 MSym/s QPSK is far better resulting in 10 dBc towards 42 dBc ACPR (Fig. 4.27(b)). This is related to the internal bandwidth of the RFPAL system, which starts with 1 MHz.

Particularly higher order modulation schemes like 16APSK can benefit from this technique. As can be seen in Fig. 4.27(c) a 16APSK output spectrum is improved with more than 10 dBc, now holding the mask. It has to be pointed out that this 16APSK has a 1 dB higher PAPR compared to QPSK. Therefore, using the BUC with the same average output power for a QPSK or a 16APSK results in a 1 dB higher **linear** peak power. Towards the trend of lowering the $\alpha \leq 0.35$ used within DVB-S2 or DVB-S2X, the more stringent requirements of linearity can be fulfilled with this linearisation technique without decreasing the output-power level of the BUC.

BUC with 70 W PA

The BUC is further analysed with the 70 W Ku_{up} PA described in Sec. 3.3. The improvements regarding linearity for various output signals are already stated in Sec. 3.3.5. The limitation of using this medium power amplifier within the small housing of this BUC is the amount of dissipated power. Tab. 4.3 states the input as well as output power of the BUC equipped with the 25 W as well as the 70 W PA. The usage of a QPSK signal with

TABLE 4.3: Comparison of both PAs in the BUC

	f_0 (GHz)	P_{dc} (W)	$P_{out,pk}$ (W)	PAPR (dB)	PAE (%)
25 W PA	13.75	51	19	3.9	13
$\alpha = 0.35$	14.00	52	19.4	3.9	14.3
4 MSym/s	14.25	50.9	20	3.9	14.5
QPSK	14.50	52	19.6	3.7	14.7
70 W PA	13.75	128	40.7	3	16.3
$\alpha = 0.35$	14.00	122	40.8	3.1	16.2
4 MSym/s	14.25	119	42.5	3.4	17
QPSK	14.50	117	40.9	3.1	17
70 W PA	13.75	93	37	4.4	13.9
$\alpha = 0.05$	14.00	93.8	39	4.8	14.4
4 MSym/s	14.25	86.9	38	5.1	15.5
32APSK	14.50	92	38	4.5	14.9

the 70 W PA is described in the second row, with an extremely high power consumption of ≥ 117 W. Here the PA is driven to a high compression reducing the PAPR from initially 3.9 dB to only 3 dB. This leads to a high self-heating which itself limits the output power to $P_{out,avg} = 20$ W. The resulting PAE_{sys} depends on the $P_{out,avg}$ in relation to the system power consumption (Appx. A.85).

The 70 W PA should only be seen as an extension for the use with signals towards higher modulation schemes for this small size BUC. By applying a 32APSK ($\alpha = 0.05$) the measurements indicate a $P_{out,avg} = 14$ W with up to $P_{out,pk} = 39$ W while holding the Eutelsat mask. The power consumption is, due to the increased PAPR, lowered to ≥ 86 W resulting in an excellent PAE_{sys} of up to 17%.

In comparison to the modulated measurements of the PA only (Sec. 3.3.5) the considerably high losses

of the output coupler as well as the MS to WG transition lowers the output power. Furthermore, the imperfect heat-sink of the BUC adds self-heating to the PA, while in the stand-alone measurement an almost perfect water cooling was attached.

Environmental Tests

The previous measurements state a proper behaviour of the BUC within laboratory conditions. Nevertheless, the described functions needed to be proven under bad thermal conditions as well. So environmental measurements were carried out within a thermal chamber. The temperature of the chamber was changed within a time-frame of four hours between 0 °C and 45 °C room-temperature over the course of a week. The resulting output power of the BUC, its power consumption as well as the resulting output power spectrum was monitored.

Fig. 4.28 visualizes the temperature behaviour of the chamber and the housing of the BUC during eight hours. No additional cooling was applied to the housing of the BUC. It can be obtained that extremely high temperature values of up to 68 °C for the housing were measured at 45 °C room temperature of the chamber. Over the course of the week a change in output power of ± 0.4 dB was observed. In addition, the IMD5 products rise with an increased temperature, but are still compensated by the linearisation to fulfil the mask.

This environmental analysis does not represent typical EN60068 analysis but indicates a proper working for additional outdoor usage.

4.7 BUC Summary

Within this chapter, a design procedure of a hybrid *Ku*-band BUC has been presented. Beginning with
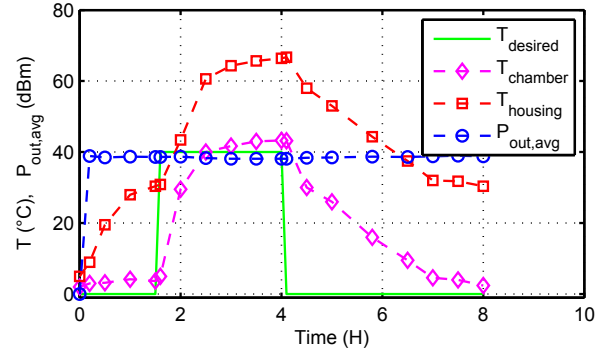
FIGURE 4.28: Measured temperature behaviour within climate chamber of the BUC equipped with the 25 W PA for a QPSK signal with $P_{out,avg}$ =39 dBm.

a design description, all components of a BUC, namely the LO generation, up-conversion, filtering as well as the amplifier and power amplifiers are described. All parts were evaluated individually as well as in the system. The BUC can be equipped with a P_{out} =25 W amplifier resulting in an output power up to 39 dBm with PAE_{sys} = 15% for a CW excitation. Through using QPSK signals, the peak output power increases to $P_{out,pk}$ =20 W due to the lowered self-heating.

With the aim of using higher order modulations and therefore an increased PAPR the larger Ku_{up} amplifier (P_{out} =70 W) can be located in the BUC. Measurements with a 32APSK modulation indicate $P_{out,pk}$ =40 W with up to PAE_{sys} = 17%.

The BUC is equipped with an IF-pre-distortion that is able to improve the ACLR for QPSK modulated measurements within 10 dBc. Real time centre frequency and signal bandwidth detection is realised without access to the baseband signal. This work has shown that a linearisation of the PA in a BUC can be done within the IF-range. An IF pre-distortion delivers good results for decreasing the spectral regrowth as well as minimizing the EVM of modulated SatCom signals. The technique is easy to implement directly within the BUC and can extend the throughput of the uplink as well as its efficiency.

4.8 BUC Discussion

The realised BUC cannot be directly compared to the state-of-the-art results due to the lack of published BUCs. The results are thus compared to commercially available BUCs. It can be noted, that commercially BUCs are nowadays made of GaAs up to a power level of $\approx$ 25 W. GaN is starting to build the bridge with medium power BUCs towards high power TWTA based BUCs, which are mainly used for broadcasting and the military. A comparison is stated in Tab. 4.4.

Starting with $P_{out,1dB}$ =39 dBm there are three near identical BUCs based on GaAs technology given in [Agi16a], [Nor15a], [NJR17a]. The output power is defined with up to 8 W resulting in a low PAE_{sys} of only up to 10%. In comparison, the developed low power BUC_{25W} shows a lower $P_{out,1dB}$ = 38 dBm due to the typical GaN *soft-compression*. Nevertheless, the output power is with up to 20 W, far higher – also the included linearisation enhances the output power level to linear values higher than $P_{out,1dB}$, but only for modulated signals. The BUC can furthermore take advantage of the higher drain efficiency resulting in a PAE_{sys} of 14.5%.

The PAE_{sys} for the medium power BUCs are calculated considering the 3 dB back-off power consumption in relation to the 3 dB back-off output power (Appx. A.85). In consequence, the PAE_{sys} is related to a realistic operation with a compressed QPSK signal. It should be mentioned that the first two entries do not state the technology used [Agi16b], [Nor15b]. However, based on their high power consumption, a combined GaAs technology can be assumed. In addition, they can take advantage of a high $P_{out,1dB}$ through the use of GaAs. The third mentioned BUC uses a GaN MMIC and is able to increase its PAE_{sys} of up to 11.4% [NJR17b]. Nevertheless, it does not state its $P_{out,1dB}$ due to the assumed *soft compression* of GaN. Furthermore, no linearisation technique is included in this BUC which is why, it is assumed that the BUC needs to be operated in a high back-off to fulfil $P_{out,1dB}$ compression requirements.

In comparison to this commercially available BUC, the developed BUC_{70W} can achieve an equal $P_{out,pk}$ while producing significantly less dissipated power. It can take advantage of the already improved PAE_{sys} with regard to the PA itself (Tab. 3.8) and does not lose power in an output combining like [Agi16b], [Nor15b].

TABLE 4.4: Comparison to commercial BUC in the extended *Ku*-band (13.75-14.5 GHz)

low power:	tech	$P_{out,1dB}$ (dBm)	$P_{out,pk}$ (W)	P_{dc} (W)	Gain (dB)	PAE_{sys} (%)	PN @1 kHz (dBc/Hz)	Dimensions L x W x H (cm)
Agilis ALB [Agi16a]	GaAs	39	8	85	64-72	9.4	-73	28x14x10
Norsat 1081XRTS [Nor15a]	GaAs	39	8	80	56-66	10	-70	28x13x13
NJT8318 [NJR17a]	GaAs	39	8	80	59-65	10	-70	18x13x8
BUC_{25W}	GaN	38	20[1]	52	55-60	14.5	-80	19x12x2
medium power:								
ALB128 slim [Agi16b]	?		46	350[3]	70	5.7	-75	34x35x4
MEDIBKU040 [Nor15b]	?		44	270[3]	65	9	-73	20x13x12
NJT8371 [NJR17b]	GaN		40	220[3]	68-74	11.4	-70	23x15x10
BUC_{70W}	GaN	43	40[1]	130[3]	65-71	17	-80	19x12x2
BUC_{70W}	GaN	42	40[2]	92[4]	65-71	16	-80	19x12x2

[1] QPSK   [3] 3dB back-off   [4] for 32APSK 4.5dB back-off

[2] 32APSK

5 Satellite Link

Within this section, the developed hardware, namely the PA and the BUC, are going to be evaluated in a Satellite Link.

A detailed description of the Link Scenario is given in Sec. 5.

The characteristic budgets of the Link are calculated in Sec. 5.1 while the necessary analysis and nomenclature is given in Appx. A.6.

The evaluating Link Test is described in Sec. 5.2, taking a Video-on-Demand (VoD) scenario into consideration. Finally, the results are summarised in Sec. 5.3.

Data Link

Television satellite services are widely realised with a single uplink, casting to any number of receivers back on earth (broadcast Fig. 5.1(a)). Nowadays, fixed satellite services (FSS) are widely used for classical telecommunications, television as well as back-haul solutions for data communications. In contrast to a classical broadcasting SatCom, a data connection via satellite needs to be directed within two directions. One is called the forward link (FWL), which directs to the satellite and is relayed back to earth. The receiving terminal on earth needs to reply to the transmission terminal with an acknowledgement (Ack) within the return link (RTL) via satellite (Fig. 5.1(b)). Several topologies can be realised, for example, a single cast uplink between a HUB and a VSAT results in a point-to-point connection. By increasing the number of VSATs a Star-Network is created enabling the typical application of several back offices communicating with one main office. An interconnection from one VSAT to another has to be relayed through the HUB, which reduces frequency allocation and lowers the necessary EIRP of a VSAT.
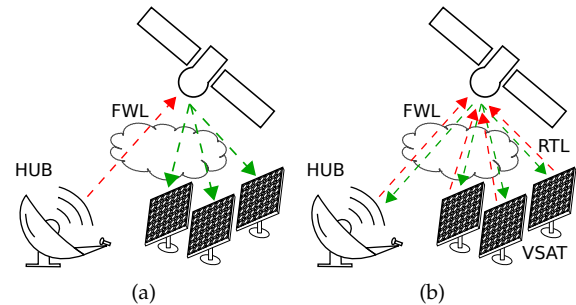
FIGURE 5.1: (a) classical SatCom with broadcast FWL (b) data link via HUB and VSAT with additional RTL (Star- or Mesh-Network).

Within a Mesh-Network all VSATs can generate interconnections to each other as well as the HUB. This is by far the most expensive network with a maximum amount of frequency allocation as well as a high EIRP of each VSAT. The amount of allocated frequencies can be reduced by time division protocols synchronizing several forward and return links. The needs for satellite interconnections increase, as a backup solution for time sensitive and critical markets. What these markets have in common is high investment as well as the operating costs to maintain the satellite link, which can be paid off quickly, during a breakdown of the conventional data communication system (e.g. mobile communication, telephone service).

Among these classical services, modern satellites provide an increased number of transponders to their precursor. A new launched satellite is therefore able to provide more data links than its pendant of the past. In particularly, the total number of *Ku*-band transponders has increased within the past few years, as can be seen in Fig. 5.2. Furthermore, new techniques like high throughput satellites (HTS) use spot beams and therefore frequency re-usage within a satellite to increase the possible data rate via satellites [Uni11]. This progress lowers the costs-per-bit of a satellite link for its user.

Apart from that, new markets can grow by the
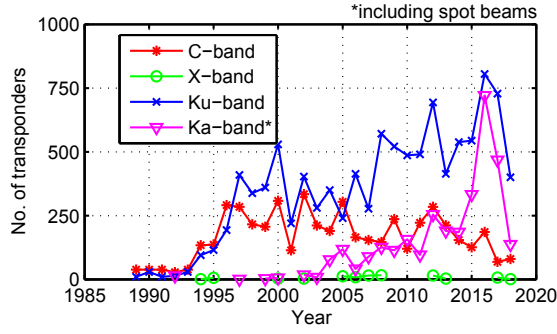
FIGURE 5.2: Launched transponders per year (data taken from [Sat]).

FIGURE 5.3: Various typical EIRP levels are calculated based on antenna gain versus PA output power.

increasing demand in selectable video content, in contradiction to the classical broadcasting television industry. VoD services can be realised via HTS through the use of a bidirectional VSAT for the end user. The request is sent from the VSAT in a rather small FWL with mainly signalling data. A HUB can reply within the RTL with the video content. An additional content provider needs to supply either selected or all content via a terrestrial network to the HUB. The increased number of spot-beams located on this HTS can, in combination with a transponder sharing increase the possible number of users per coverage.

To achieve a data connection in remote regions a terminal interconnection to a hub station via satellite can be the only solution among mobile communication realised by VSATs.

Link Scenario

Within the used satellite link there are two earth terminals that both react as transceivers. The satellite itself simply converts an incoming signal in frequency and amplitude and returns it to earth within its transponder. The larger terminal on earth can be defined as HUB and the other as VSAT. It needs to be mentioned that normally all directed interconnections (FWL up, FWL down, RTL up, RTL down) are defined with different frequency allocations. Thus, FWL as well as RTL are continuous in a two-way interconnection. Both earth terminals are equipped with a satellite modem that modulates/ demodulates Ethernet signals to an IF. While choosing a data link, the link budget has

to be calculated for the FWL as well as the RTL separately. The size of the dish (and therefore the antenna gain) influences the transmitting as well as the receiving signal strength. In conclusion, the HUB terminal has to compensate for the lower antenna gain of the VSAT by an increased size of its own dish to improve the carrier to noise (C/N) distance.

Nevertheless, VSATs are limited to a certain equivalent isotropically radiated power (EIRP) either in terms of the antenna gain or the output power of the block up-converter (BUC) as can be obtained from Fig. 5.3.

Typical EIRP levels of $\{41, 46, 49, 52\}$ dBW for commercially available VSATs are displayed regarding their BUC power level vs. their antenna gain. For example, by assuming an antenna gain of 40 dBi and a BUC output power of 10 W an EIRP of 49 dBW can be obtained while mispointing and interconnection losses are assumed as described in [Mar03].

By increasing the antenna gain, which comes along with increasing the size of a dish or planar antenna, the VSAT gets bulky and impractical. Increasing the power of the BUC normally leads to a very heavy housing with a higher power consumption and a rapid growth of its costs. The utilized techniques given in Sec. 3 for the PA and in Sec. 4 for the BUC lead to a lightweight solution with a high output power that is affordable. A functional test of this BUC, a LNB as well as a planar antenna is described within the following subsections.
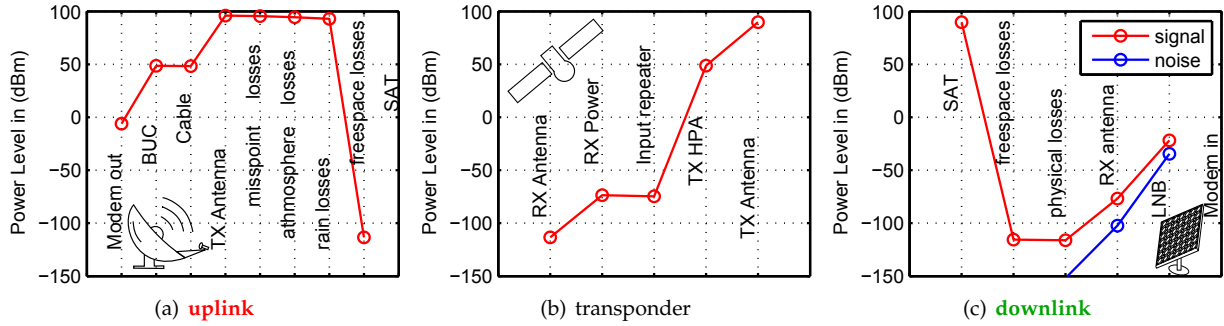
FIGURE 5.4: Link budget analysis calculating the equivalent power level (red) as well as the equivalent noise level (blue) for a 4 MHz QPSK signal displaying (a) the uplink (b) the transponder (c) the downlink.

5.1 Link Budget

All gains and losses of an interconnection from the base station transmitter to the opposite receiver are accounted for in a link budget. It therefore indicates the signal strength to the noise of the signal within a link. A so-called margin can be defined by taking into account the transmitted power, the free space loss and the noise. Only a positive margin indicates a proper working link. An example calculation is done to clarify the power levels within the different subsystems of the link. The related equations are given in [Rod01, 305ff] and defined in the Appx. A.6.

One-Way Link Budget

With regard to the **uplink** the calculation starts with the output power of the modem (-6 dBm in red) located in the IF (Fig. 5.4(a)). Afterwards, the conversion of the BUC to the TX frequency (13.81 GHz) results in an output power level of 48 dBm (60 W) at the WR75 reference plane. Interconnection losses to the antenna lower the power level within 0.5 dB. With a ∅ 2.4 m dish the signal is non isotropically radiated which gains within 48 dB to the total EIRP (96 dBm = 66 dBW) of the transmitting ground station. This antenna cannot be ideally pointed to the satellite, which is why mispoint losses (0.5 to 1 dB) occur. Moreover, the radiated signal passes through rain (1.5-6 dB) and the atmosphere (≈ 1 dB) which further decreases the power level. The main degradation of power occurs within the free space losses

(≈ 35786 km ≙ 210 dB) resulting in a power level of only -113 dBm at the GEO position of the satellite.

The budget of the satellite transponder is visualized in Fig. 5.4(b), starting with -113 dBm, as previously described, which increases with the RX antenna. The internal LNAs as well as the conversion, changing the TX frequency to the RX frequency, levels the signal before the high power amplifier (HPA[1]) amplifies the level up to the transponder TX power level. At the end, the TX antenna of the satellite increases the power level to 89 dBm = 59 dBW. Spot beams or conventional dishes are used depending on the type of satellite. It can be noted that the TX power level of the satellite is normally less than the TX power used from the earth station terminal. Special care must be taken not to overdrive the transponder with a high output power coming from the uplink base station. The transponder works in a FDMA converting multiple signals coming in to multiple frequencies going out. Therefore, each and every user has to maintain a certain power level from its base station, not to exceed the saturation flux density of the HPA located on the satellite.

Up to now, the noise (in blue) is not calculated for the uplink as well as the transponder. The receiving thermal noise of the transponder is highly related to the orbital position and the position of the HUB. Within the transponder the C/N is located in the range of 20 to 30 dB. For a 4 MHz QPSK signal $\alpha = 0.25$ the noise-density can be calculated to a representing power level, which therefore determines

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[1]conventionally a TWTA

TABLE 5.1: (a) Uplink calculation within the **FWL**; (b) Downlink calculation within the **FWL**; (c) resulting total link margin within the **FWL** (Berlin to AM44; 14.0722 GHz (H) up; 11.5222 GHz (V) down; 0.5 MSym/s; QPSK; FEC 3/4; $\alpha = 0.35$; $P_{out} = 10$ W; 99.5% availability ITU-R)

(a)

uplink	clear sky	rain up	
uplink EIRP	53	53	dBW
transponder IBO	7.85	7.85	dB
IBO/carrier	28.29	29.95	dB
antenna mispoint	0.3	0.3	dB
free space loss	207.23	207.23	dB
total attenuation	0.18	1.86	dB
C/N (th)	21.98	20.3	dB
C/(N+I)	21.96	20.28	dB
$E_b/(N_0+I_0)$	20.55	18.87	dB

(b)

downlink	clear sky	rain down	
sat EIRP	50.5	50.5	dBW
transponder OBO	5.18	5.18	dB
OBO/carrier	25.62	25.62	dB
antenna mispoint	0.3	0.3	dB
free space loss	205.5	205.5	dB
total attenuation	0.14	1.16	dB
total system noise	127.75	180.62	K
G/T	17.44	15.93	dB/K
C/N (th)	8.28	5.76	dB
$E_b/(N_0+I_0)$	6.82	4.32	dB

(c)

totals per carrier (end to end)	clear sky	rain up	rain down	dual fade	
C/N (th)	8.1	6.42	5.564	3.97	dB
C/(N+I) = [$E_s/(N_0+I_0)$]	8.05	6.38	5.62	3.95	dB
system margin	1	1	1	1	dB
net $E_s/(N_0+I_0)$	7.05	5.38	4.62	2.95	dB
required $E_s/(N_0+I_0)$ (for QPSK)	3.1	3.1	3.1	3.1	dB
excess margin	3.95	2.28	1.52	-0.15	dB

the distance to the signal level.

The **downlink** path (Fig. 5.4(c)) can take advantage of less free-space losses (≈ 205 dB) than the uplink, due to the slightly lowered frequency (11.012 GHz). In addition, the atmospheric and rain losses are summed up to the physical losses (3 dB). An antenna size of $\varnothing 1.2$ m will result in a gain of 41 dB boosting the signal level to -78 dBm. As can be obtained from Fig. 5.4(c), the signal-to-noise ratio (SNR) degrades extremely at the budged position of the RX antenna (only $\varnothing 1.2$ m). The next significant decrease of SNR is related to the Noise-Figure of the LNA located in the receiving earth station. The receiving antenna on earth cannot take advantage of a cold surrounding, which is why in combination with the LNA a gain to noise temperature (G/T) of 16 dB/K limits the signal quality. A total system SNR of 12 dB is visualized, which is sufficient for a demodulation. It has to be pointed out, that an increased absorptive rain attenuation directly reduces the earth station G/T which is why the receiving antenna diameter has to be increased, preventing an increase of rain attenuation in the downlink.

The complexity of the used signal determines the

requirements regarding the normalized SNR. During a link period of high SNR the modulation can be increased by maintaining the same signal bandwidth. In consequence, the data rate increases as well. During a period of rain fade the SNR is decreased which makes a decrease of the modulation or an increase of the forward error correction (FEC) necessary. However, the link budget is calculated for one modulation that requires a certain $E_s/(N_0+I_0)$. In addition, losses due to rain in the uplink, downlink or both are added to the calculation.

Apart from these simple calculations additional uplink intermodulation needs to be considered.

Two-Way Link Budget

The link budget as well as the transmission plan is normally calculated by the satellite provider for the end-user. Nevertheless, to prove a proper working link between VSAT and VSAT or VSAT and HUB the margin is calculated for an interconnection between Berlin (52°31′51″ N) and a satellite called Express-AM44 (11° W). The resulting angle for the VSAT is 209.63° azimuth, with 25.83° elevation. The previous shown link budget

TABLE 5.2: (a) Uplink calculation within the **RTL**; (b) Downlink calculation within the **RTL**; (c) resulting total link margin within the **RTL** (Berlin to AM44; 14.0737 GHz (H) up; 11.5237 GHz (V) down; 0.3 MSym/s; QPSK; FEC 3/4; $\alpha = 0.35$; $P_{out} = 10$ W; 99.5% availability ITU-R)

(a)

uplink	clear sky	rain up	
uplink EIRP	48	48	dBW
transponder IBO	7.85	7.85	dB
IBO/carrier	33.38	35.07	dB
antenna mispoint	0.3	0.3	dB
free space loss	207.23	207.23	dB
total attenuation	0.18	1.87	dB
C/N (th)	19.12	17.43	dB
C/(N+I)	19.09	17.41	dB
$E_b/(N_0 + I_0)$	17.68	16	dB

(b)

downlink	clear sky	rain down	
sat EIRP	50.5	50.5	dBW
transponder OBO	5.18	5.18	dB
OBO/carrier	30.71	30.71	dB
antenna mispoint	0.3	0.3	dB
free space loss	205.5	205.5	dB
total attenuation	0.14	1.16	dB
total system noise	137.54	190.42	K
G/T	19.97	18.5	dB/K
C/N (th)	7.64	5.21	dB
$E_b/(N_0 + I_0)$	6.19	3.78	dB

(c)

totals per carrier (end to end)	clear sky	rain up	rain down	dual fade	
C/N (th)	7.35	5.66	5.04	3.35	dB
C/(N+I) = [$E_s/(N_0 + I_0)$]	7.3	5.6	5.1	3.33	dB
system margin	1	1	1	1	dB
net $E_s/(N_0 + I_0)$	6.3	4.63	4.01	2.33	dB
required $E_s/(N_0 + I_0)$ (for QPSK)	3.1	3.1	3.1	3.1	dB
excess margin	3.2	1.53	0.91	-0.77	dB

is proven by the software Satmaster Pro [Arr99] with an extension of the RTL and a more detailed intermodulation analysis[2].

FWL Budget

The FWL is calculated based on a VSAT with a dish of $\varnothing$ 1.2 m diameter that results in an antenna gain of 43 dBi. Equipped with a 10 W BUC (BUC_{25W}) an EIRP = 53 dBW can be achieved. As can be seen in table 5.1 (a) based on the uplink EIRP and the knowledge of the transponder the normalized SNR ($E_b/(N_0 + I_0)$) can be calculated. I, as well as I_0 denotes, that a carrier intermodulation is being considered. Furthermore, the same calculation can be done for the downlink in table 5.1 (b). Here the dish size of the receiver terminal and its G/T becomes significant. In addition, the calculation is divided into one situation with *clear sky* that represents the free space losses, and one called *rain* that adds losses due to rain-fade. Note that the influence of rain, clouds or snow can impact the

[2]The intermodulation within a link is clarified in appendix A.119 and should not be mixed-up with the IMD that is related to the saturation of a PA

uplink, the downlink or both. Tab. 5.1 (c) summarizes the margin that is influenced by the uplink and the downlink as well. A required normalized SNR in form of $E_s/(N_0 + I_0)$ is defined with 3.1 dB that represents the dynamic range necessary, for demodulating a QPSK (FEC 2/3) [ETS09, 34 ff.]. It can be seen that a link works for the situation *clear sky* as well as *rain up* due to its positive excess margin. Only for the condition of a *dual rain-fade* no link can be achieved.

RTL Budget

The counterpart of the interconnection starts with the VSAT, its planar antenna (38 dBi) and the developed BUC_{25W} resulting in 45 dBW EIRP (Tab. 5.2). The lower EIRP compared to the previously reported HUB results in a reduced IBO per carrier at the satellite (Tab. 5.2 (a)). Hence, the OBO per carrier of the transponder is reduced as well, which increases the G/T within the downlink (Tab. 5.2 (a)). It can be noted that only a positive excess margin can be achieved during the situation *clear sky*, and *rain up* while an additional *rain down* suffers from the higher OBO of the transponder. Only

for the condition of a *dual rain-fade* no link can be achieved.

5.2   Link Test

The HUB is realised via a classical satellite terminal consisting of a dish mounted on a fixed or steerable support. A feed-horn is located within the focal point of the dish. This feed-horn is formed as a circular wave-guide towards the dish. An orthogonal mode transducer (OMT) afterwards splits the TX from the RX frequency range and ends in rectangular wave-guides. The OMT is able to achieve TX to RX isolation of up to 80 dB. The BUC as well as the LNB gets screwed to this wave-guides. By twisting this feed around the beam axis in the focal point a vertical or horizontal polarisation can be achieved.

The VSAT called EASYSTAR, that is an outcome of the project ISISTAR [Rau+17b], features an integrated planar LNB as well as the BUC_{25W} on the backside of a three layer passive planar antenna [Gei+17] (Fig. 1.2). The three layer antenna consists of an antenna array supported by two feeding networks each for the TX as well as the RX frequency range. It is intentionally designed to provide a 90° phase shift between TX and RX to increase the isolation. It can therefore be used without a separate OMT. All electric components are assembled on the back-side of the antenna. EASYSTAR can be easily pointed to the satellite by its spherical head in the mechanical centre of the backside plate. By twisting the planar antenna perpendicular to the beam axis its polarisation is tuned.

HUB to VSAT (Star-Network)

The first measured scenario displays the usage of a Star-Network with one HUB station located in Munich directing to a VSAT in Berlin. The analysed link can be divided into two different measurement scenarios separating the FWL from the RTL. A detailed Link-Budget analysis is given in the Appx. A.6.
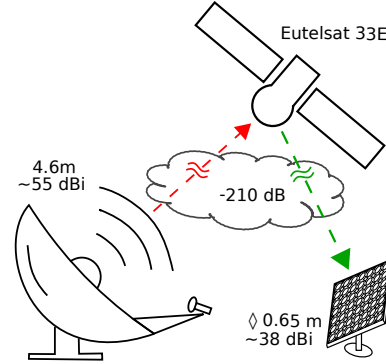
FIGURE 5.5: FWL HUB to VSAT.

TABLE 5.3: Measured data-rate HUB to VSAT in FWL.

TX	RX	RX
13930.87 MHz	11135.37 MHz	
5 MSym/s[1]	(C/N 9.8 dB)	(theor. limit)
FEC 1/2	4.5 MBit/s	5 MBit/s
FEC 2/3	5.2 MBit/s	6.6 MBit/s
FEC 3/4	5.9 MBit/s	7.5 MBit/s
FEC 5/6	6.9 MBit/s	8.3 MBit/s

[1] 6 MHz

FWL (HUB to VSAT)

Fig. 5.5 shows the FWL directing from the HUB to the VSAT. The HUB is realised with a ⌀ 4.6 m dish (ND SatCom) that provides a 5 MSym/s (≈ 6 MHz) QPSK uplink (DVB-S1). The TX antenna gain is 55 dBi which is powered by a BUC delivering $P_{out} = 10$ W resulting in up to 65 dBW EIRP.

The downlink ends up at EASYSTAR with a measured sufficient high C/N of 9.8 dB. Using a forward error correction (FEC) of 1/2 up to 4.5 MBit/s throughput is achieved (Tab. 5.5). Note that the TCP overhead lowers the measured data-rate in comparison to the theoretically 5 MBit/s. By reducing the FEC the data-rate increases over 5.2 MBit/s and 5.9 MBit/s of up to 6.9 MBit/s for FEC 5/6 which represents a spectral efficiency of 1.65.

The modem used (Romantis UHP 1000) was only able to realise a QPSK modulation, by firmware restrictions, which is why no higher order modulation schemes could be selected. The measured C/N of 9.8 dB is theoretically high enough for the usage of a 8PSK with FEC 5/6 with a spectral efficiency of 2.5 [ETS09, 34 ff.]. This would further increase the data-rate of up to 10.5 MBit/s. With

FIGURE 5.6: RTL VSAT to HUB.
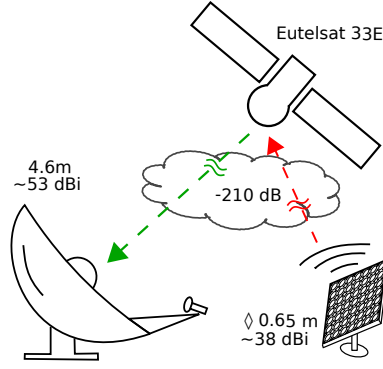
FIGURE 5.7: FWL VSAT to VSAT.

TABLE 5.4: Measured data-rate HUB to VSAT in RTL.

RX 11130.87 MHz (C/N 9.7 dB)	RX (theor. limit)	TX 13935.37 MHz 0.5 MSym/s[1]
0.4 MBit/s	0.5 MBit/s	FEC 1/2
RX (C/N 9.4 dB)	RX (theor. limit)	TX 1.2 MSym/s[2]
1 MBit/s	1.2 MBit/s	FEC 1/2

[1] 0.6 MHz [2] 1.3 MHz

TABLE 5.5: Measured data-rate VSAT to VSAT in FWL.

TX 14072.2 MHz 0.5 MSym/s[1]	RX 11522.2 MHz (C/N 6.4 dB)	RX (theor. limit)
FEC 1/2	0.4 MBit/s	0.5 MBit/s
1.2 MSym/s[2]	(C/N 6.4 dB)	(theor. limit)
FEC 5/6	1 MBit/s	1.2 MBit/s

[1] 0.6 MHz [2] 1.3 MHz

an increased C/N future DVB-S2 compatible modulation schemes, like 16APSK or 32APSK, have the ability to significantly increase this data rate.

RTL (HUB to VSAT)

Fig. 5.6 shows the RTL directing from the VSAT to the HUB. The TX antenna gain is 38 dBi equipped with the developed BUC_{25W}, which is able to deliver $P_{out} = 10$ W for a DVB-S1 QPSK signal. The resulting EIRP is 48 dBW for the RTL. Due to the lower EIRP of the RTL in comparison to the FWL, the signal bandwidth is lowered to 0.5 MSym/s pursuing a higher spectral density at the receiver of the HUB. The receiving antenna gain at the HUB is reduced to 53 dBi by the lowered RX frequency. The measured C/N of 9.7 is sufficiently high for demodulating the signal at the receiver with a data-rate of 0.4 MBit/s (Tab. 5.4). By increasing the signal bandwidth to 1.2 MSym/s up to 1 MBit/s was achieved for the RTL while the C/N was reduced to 9.4 dB.

VSAT to VSAT (Mesh-Network)

The second scenario represents a link connection between two VSATs which is more difficult either in terms of a lowered TX EIRP as well as due to the lowered RX antenna gain. One VSAT was realised with a smaller dish of only ∅ 1.2 m and a 10 W BUC, while the other VSAT is the already known EASYSTAR. The satellite AM44 was used on transponder D3. This scenario is equal to the previously calculated link-budget of Sec. 5.1.

FWL (VSAT to VSAT)

The FWL is directed from the dish based VSAT to EASYSTAR (Fig. 5.7). With the use of 43 dBi TX antenna gain the EIRP is 53 dBW. With a 0.5 MSym/s bandwidth a C/N of 6.4 dB was achieved during excessive rain. This results in 0.4 MBit/s data-rate for FEC of 1/2 with up to 1 MBit/s for FEC of 5/6 (Tab. 5.5).
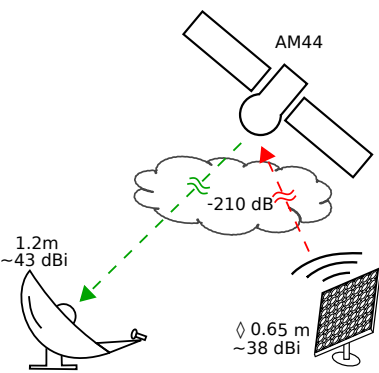
FIGURE 5.8: RTL VSAT to VSAT.

RTL (VSAT to VSAT)

The RTL from the VSAT to the dish based VSAT (Fig. 5.8) was also realised with 0.5 MSym/s, resulting in a measured C/N = 6.1 dB (Tab. 5.6). An equal data-rate of 0.4 MBit/s was achieved for the RTL, as with the FWL. One application of this VSAT to VSAT interconnection could be to provide two-way (internet) into remote regions. The achieved data-rate was sufficient for surfing with the restriction of the additional round trip time delay. In spite of the rather low data-rate the link was even sufficient for starting video streams.

TABLE 5.6: Measured data-rate VSAT to VSAT in RTL.

RX 11523.7 MHz (C/N 6.1 dB)	RX (theor. limit)	TX 14073.7 MHz 0.5 MSym/s[1]
0.4 MBit/s	0.5 MBit/s	FEC 1/2

[1] 0.6 MHz

5.3 Summary

Within this chapter, the designed BUC equipped with the previously designed PA was attached to a planar VSAT. The VSAT was tested in a data satellite link connected to a HUB station. The link shows a sufficient C/N level of 9.4 dB and up to 1 MBit/s throughput in the RTL directed from VSAT to HUB. A VoD application was used for the satellite link. A video request was sent via the RTL with a low amount of data. The FWL can take advantage of its high data-rate for providing up to Full-HD video content (1920x1080 H.264 4-8 MBit/s). The latency of the link is not important for VoD content. Starting from 0.5 MBit/s data-rate a common VoD stream can be commenced. By using higher order modulation schemes, the data-rate could easily fulfil the requirements of 4K content (3840x2160 H.265/HEVC 16-25 MBit/s).

In addition, a Mesh-Network topology was adapted realising a VSAT to VSAT interconnection with up to 0.5 MBit/s data-rate. The intention of realising a two-way (internet) connection was achieved.

The small mechanical dimension of the BUC as well as great performance data indicate the good perspectives of GaN-HEMT for future VSAT related SatCom applications.

6 Conclusion

In this thesis, an extensive design procedure for efficient two-stage GaN-HEMT PAs in the *Ku*-band has been presented. Starting with an ideal transistor approximation, the design constraints were theoretically analysed. A Load/Source-Pull methodology has been used with a systematic design approach to develop the matching circuits. The classical Load/Source-Pull has been extended to a Multi frequency Load/Source-Pull methodology to gather for a more optimum design. Effort was spent for the EM-modelling of all parasitics and the matching circuits to reduce the effects of manufacturing constraints.

The procedure was later validated by implementing the two stage PA based on two 70 W bare-die GaN-HEMT devices. Simulated and measured results of this PA showed a very good agreement. Large-signal measurements (CW) depicted more than 50 W output power in the desired frequency range of interest with more than 23% PAE. These results were achieved while maintaining a high saturated gain of $\geq 15\,\text{dB}$. Linearised modulated measurements using a 16 MSym/s QPSK (DVB-S) signal demonstrate an average PAE of 21% by more than 30 W output power (70 W peak) while holding the linearity requirements.

The derived design methodologies have been used to build a working adoption of the MIC PA in a lower (12.75-13.5 GHz) as well as extended frequency range (12.75-14.5 GHz). Both designs have shown a good agreement between measurement and simulation. While the first one enhances the achieved output power to more than 80 W with more than 34% PAE, the more broadband second approach suffers from a lower PAE of 20% achieving 50 W output power.

Different manufactured amplifiers have shown only a small variation in their performance data.

The excellent results obtained indicate that a hybrid two stage design approach has significant advantages towards system design while achieving a state-of-the-art efficiency.

In addition, a design procedure of a hybrid *Ku*-band BUC has been presented. Starting with a design description, all components of a BUC, namely the LO generation, up-conversion, filtering as well as the amplifier and power amplifiers were described. All parts were evaluated individually as well as in the system. CW measurements of the BUC show an output power up to 39 dBm with $\eta = 15\%$. Furthermore, higher order modulation schemes 32APSK(DVB-S2), 64APSK(DVB-S2X) were tested and denote 20 W and 16 W output power respectively with a PAE of $\geq 21\%$ by using a larger PA.

The BUC has been equipped with an RF-predistortion capable of improving the ACLR for QPSK modulated measurements within 10 dBc. Real time centre frequency and signal bandwidth detection has been realised without access to the baseband signal, in the IF-range. An IF predistortion delivered good results for decreasing the spectral regrowth as well as minimizing the EVM of modulated SatCom signals. The technique has been easily implemented directly in the BUC and extends the throughput of the basestation as well as its efficiency.

Particularly very small aperture terminals (VSATs) in a mesh topology can benefit from an enhanced output linearity with equal output power. Furthermore, this technique opens up new possibilities for transistor technologies with strong non-linearities or long term memory effects like GaN-HEMTs in higher frequency ranges.

The developed BUC exceeds the commercially available BUCs regarding their system efficiency with up to 5% for the low power (20 W) and up to 7% for the high power (40 W) version considering

the 3 dB back-off operation. Furthermore, the developed BUCs are extremely thin and lightweight compared to other products, which eases the pointing of a VSAT.

Finally a planar VSAT has been equipped with the BUC and tested in a satellite link to a Hub. The link has shown sufficient C/N level and up to 1 Mbit/s in the return link. The small dimension of the BUC as well as great performance data indicate the high perspectives of GaN for future SatCom applications.

The results of this thesis were summed up in a workshop for EUMW2017 [Maa+17d]. The derived technologies for matching low impedance devices can be used for the development of MMICs as well. SatCom related developments for the *Ka*-band can be carried out, with the use of 140 nm GaN-HEMT technologies in future work. *Ka*-band terminals are particularly suitable for implementing a linearisation technique in the IF like described in this work, due to the equal IF like in the *Ku*-band.

A Appendix

A.1 S-Parameter

Within the Microwave theory the behaviour of linear elements can be explained by the use of S-Parameters. One term of a port linear circuit can be defined by a complex voltage V_i and a complex current I_i where (i=1,2). These voltages and currents can be divided into forward (V_{fi}) and reflected (V_{ri}) propagation with the reference Impedance Z_L.

$$V_1 = V_{f1} + V_{r1}; \quad I_1 = \frac{V_{f1}}{Z_L} - \frac{V_{r1}}{Z_L} \quad (A.1)$$

$$V_2 = V_{f2} + V_{r2}; \quad I_2 = \frac{V_{f2}}{Z_L} - \frac{V_{r2}}{Z_L} \quad (A.2)$$

So the voltages and currents can be changed to wave quantities that are either propagating (a_i) or reflected (b_i).

$$a_i = \frac{V_{fi}}{\sqrt{Re\{Z_{Li}\}}} = \frac{V_i + Z_{Li} \cdot I_i}{2\sqrt{Re\{Z_{Li}\}}} \quad (A.3)$$

$$b_i = \frac{V_{ri}}{\sqrt{Re\{Z_{Li}\}}} = \frac{V_i - Z_{Li} \cdot I_i}{2\sqrt{Re\{Z_{Li}\}}} \quad (A.4)$$

$$V_i = \frac{Z_{Li} \cdot a_i + Z_{Li} \cdot b_i}{\sqrt{Re\{Z_{Li}\}}} \quad (A.5)$$

$$I_i = \frac{a_i - b_i}{\sqrt{Re\{Z_{Li}\}}} \quad (A.6)$$

The unit of this wave quantities is $\sqrt{W}$ based on the definition of the incoming (P_{wa}) and outgoing effective power (P_{wb}):

$$P_{wa} = \frac{1}{2} a\, a^* = \frac{V_f V_f^*}{2Z_L} \quad (A.7)$$

$$P_{wb} = \frac{1}{2} b\, b^* = \frac{V_r V_r^*}{2Z_L} \quad (A.8)$$

These incoming a_i and outgoing quantities b_i can be put in relation via the scattering matrix and linear equations:

$$b_1 = S_{11} a_1 + S_{12} a_2 \quad (A.9)$$

$$b_2 = S_{21} a_1 + S_{22} a_2 \quad (A.10)$$

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \quad (A.11)$$

In addition the wave quantities can be defined in the T-matrix:

$$\begin{pmatrix} a_1 \\ b_1 \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} \begin{pmatrix} b_2 \\ a_2 \end{pmatrix} \quad (A.12)$$

Among a two port these S-Parameter can be used as well for n-ports.

$$\begin{pmatrix} b_1 \\ ... \\ b_n \end{pmatrix} = \begin{pmatrix} S_{11} & ... & S_{1n} \\ ... & & \\ S_{n1} & & S_{nn} \end{pmatrix} \begin{pmatrix} a_1 \\ ... \\ a_n \end{pmatrix} \quad (A.13)$$

The scattering parameters S_{ij} that can be calculated based on the derivatives of the wave quantities are defined as follows for a two port:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \quad \text{input reflection} \quad (A.14)$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \quad \text{output reflection} \quad (A.15)$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \quad \text{feedback transm.} \quad (A.16)$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \quad \text{forward transm.} \quad (A.17)$$

They can also be calculated based on the Impedance quantities:

$$S_{ii} = \frac{Z_{Ei} - Z_{Li}}{Z_{Ei} + Z_{Li}} \quad (A.18)$$

$$Z_{Ei} = Z_{Li} \frac{1 + S_{ii}}{1 - S_{ii}} \quad (A.19)$$

$$S_{ji} = \frac{2V_j}{V_{0i}} \sqrt{\frac{Z_{Li}}{Z_{Lj}}} \quad (A.20)$$

By the use of these S-Parameters complex systems can be easily analysed.

Furthermore, based on this S-Parameters common

factors of microwave engineering are defined. Beginning with the definition of stability of an amplifier. Rollet defined a k-factor which needs to be positive ≥ 1 over the entire frequency range:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11} \cdot S_{22} - S_{12} \cdot S_{21}|^2}{2 \cdot |S_{12} \cdot S_{21}|} \quad (A.21)$$

In addition stability circles are used to determine weather the variation of source- and load-impedances ($|det\,S|$) is located outside the smith-chart.

$$D = |det\,S| = |S_{11} \cdot S_{22} - S_{21} \cdot S_{12}| < 1 \quad (A.22)$$

The available gain (G_{MAX} or MAG) of an amplifier can be analysed for a two port circuit independent to its source- and load-impedances:

$$G_{MAX} = \frac{|S_{21}|}{|S_{12}|} \cdot (k - \sqrt{k^2 - 1}) \quad for\, k \geq 1 \quad (A.23)$$

The available gain is undefined when k is less than one because then $\sqrt{k^2 - 1}$ gets imaginary. Therefore, for frequencies lower than $k = 1$ the maximum stable gain (MSG) is the limit of amplification:

$$MSG = \frac{mag|S_{21}|}{mag|S_{12}|} \quad (A.24)$$

Stability can be furthermore proven by the factor $B1$ which should be greater than zero.

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |det\,S|^2 \quad (A.25)$$

A.2 Transmission line Theory

Here, the MS definitions are cited by [Bah03] using the same nomenclature. Where possible, the complicated functions are eased through the use of symbolic functions. The formulas are given here for an easier recalculation of the well known transmission line theory. Wheeler defined the wave impedance of a microstrip to be [Whe78]:

$$Z_{TL} = \frac{Z_0}{2\pi\sqrt{2(1 + \varepsilon_r)}} \ln(1 + \frac{4h}{\omega_{eff}} \cdot T_{Lx}) \text{ with} \quad (A.26)$$

$$T_{Lx} = \frac{14 + \frac{8}{\varepsilon_r}}{11} \frac{4h}{\omega_{eff}} + \sqrt{(\frac{14 + \frac{8}{\varepsilon_r}}{11} \frac{4h}{\omega_{eff}})^2 + \pi^2 \frac{1 + \frac{1}{\varepsilon_r}}{2}}, \quad (A.27)$$

with ω_{eff} being the width of the microstrip taking account of the thickness of the metallisation.

$$\omega_{eff} = \omega + t\frac{1 + \frac{1}{\varepsilon_r}}{2\pi} \ln\left(\frac{4e}{\sqrt{(\frac{t}{h})^2 + (\frac{1}{\pi}\frac{1}{\frac{\omega}{t} + \frac{11}{10}})^2}}\right) \quad (A.28)$$

$$\eta = 120 \cdot \pi \quad (A.29)$$

if $\frac{W}{h} \leq \frac{\pi}{2}$

$$W_{e,h} = \frac{W}{h} + \frac{5\,t\,\left(\log\!\left(\frac{4\pi W}{t}\right) + 1\right)}{4\,\pi\,h} \quad (A.30)$$

else if $\frac{\pi}{2} \leq \frac{W}{h}$

$$W_{e,h} = \frac{W}{h} + \frac{5\,t\,\left(\log\!\left(\frac{2h}{t}\right) + 1\right)}{4\,\pi\,h} \quad (A.31)$$

if $\frac{W}{h} \leq 1$

$$F_{W,h} = \left(\frac{W}{h} - 1\right)\left(\frac{41\,W}{1000\,h} - \frac{41}{1000}\right) + \frac{1}{\sqrt{\frac{12\,h}{W} + 1}} \quad (A.32)$$

$$\varepsilon_{re} = \frac{\varepsilon_r}{2} - C + F_{W,h}\left(\frac{\varepsilon_r}{2} - \frac{1}{2}\right) + \frac{1}{2} \quad (A.33)$$

$$Z_0 = \frac{\eta \log\!\left(\frac{W_{e,h}}{4} + \frac{8}{W_{e,h}}\right)}{2\,\pi\,\sqrt{\frac{\varepsilon_r}{2} - C + \frac{\frac{\varepsilon_r}{2} - \frac{1}{2}}{\sqrt{\frac{12\,h}{W} + 1}} + \frac{1}{2}}} \quad (A.34)$$

else if $1 < \frac{W}{h}$

$$F_{W,h} = \frac{1}{\sqrt{\frac{12\,h}{W} + 1}} \quad (A.35)$$

$$\varepsilon_{r,eff} = \frac{\varepsilon_r}{2} - C + \frac{\frac{\varepsilon_r}{2} - \frac{1}{2}}{\sqrt{\frac{12\,h}{W} + 1}} + \frac{1}{2} \quad (A.36)$$

$$Z_0 = \frac{\eta}{\sqrt{\varepsilon_{r,eff}}\left(W_{e,h} + \frac{667\log\!\left(W_{e,h} + \frac{361}{250}\right)}{1000} + \frac{1393}{1000}\right)} \quad (A.37)$$

In addition, we can take the skin effect into account:

$$skin = \frac{\sqrt{\frac{\rho_c}{f\,\mu_0}}}{\sqrt{\pi}} \tag{A.38}$$

$$f_{k,TM0} = \frac{c0\,\arctan\left(\varepsilon_r\,\sqrt{\frac{\varepsilon_{r,eff}-1}{\varepsilon_r-\varepsilon_{re}}}\right)}{2\,\pi\,h\,\sqrt{\varepsilon_r-\varepsilon_{r,eff}}} \tag{A.39}$$

$$f_{50} = -\frac{f_{k,TM0}}{\frac{W\left(\frac{83}{250\,\varepsilon_r\,\frac{173}{100}}-\frac{3}{4}\right)}{h}-\frac{3}{4}} \tag{A.40}$$

if $\frac{W}{h} \leq 0.7$

$$mc = 1 - \frac{7\left(\frac{23\,\mathrm{e}^{-\frac{9\,f}{20\,f_{50}}}}{100}-\frac{3}{20}\right)}{5\left(\frac{W}{h}+1\right)} \tag{A.41}$$

else $mc = 1$

$$m_0 = \frac{1}{\sqrt{\frac{W}{h}+1}} + \frac{8}{25\left(\sqrt{\frac{W}{h}}+1\right)^3} + 1 \tag{A.42}$$

$$m = m_0 \cdot mc \tag{A.43}$$

$$\varepsilon_{r,eff,f} = \varepsilon_r - \frac{\varepsilon_r-\varepsilon_{r,eff}}{\left(\frac{f}{f_{50}}\right)^{m0\,mc}+1} \tag{A.44}$$

$$Z_{0,f} = \frac{\eta\,\sqrt{\frac{\varepsilon_{r,eff}}{\varepsilon_{r,eff,f}}}\,(\varepsilon_{r,eff,f}-1)}{\sqrt{\varepsilon_{r,eff}}\,(\varepsilon_{r,eff}-1)\,\Xi} \tag{A.45}$$

$$\Xi = \left(W_{e,h}+\frac{667\log\left(W_{e,h}+\frac{361}{250}\right)}{1000}+\frac{1393}{1000}\right) \tag{A.46}$$

The microstrip losses can be calculated dividing into conductive and dielectric losses:

$$u = \frac{W}{h} \qquad g = \frac{s}{h} \qquad v = g\,\mathrm{e}^{-g} + \frac{u\,(g^2+20)}{g^2+10} \tag{A.47}$$

$$a_e = \frac{10\log\left(\frac{1000\,v^3}{5929741}+1\right)}{187} + \frac{\log\left(\frac{v^4+\frac{v^2}{2704}}{v^4+\frac{54}{125}}\right)}{49} + 1 \tag{A.48}$$

$$b_e = \frac{141\left(\frac{\varepsilon_r-\frac{9}{10}}{\varepsilon_r+3}\right)^{\frac{53}{1000}}}{250} \tag{A.49}$$

$$\varepsilon_{r,eff,e} = \frac{\varepsilon_r}{2} + \frac{\frac{\varepsilon_r}{2}-\frac{1}{2}}{\left(\frac{10}{v}+1\right)^{ae\,be}} + \frac{1}{2} \tag{A.50}$$

$$a_0 = \left(\mathrm{e}^{-\frac{179\,u}{1000}}-1\right)\left(\frac{7287\,\varepsilon_r}{2e^5}-\frac{7287\,\varepsilon_{r,eff,f}}{1e^5}+\frac{7287}{2e^5}\right) \tag{A.51}$$

$$b_0 = \frac{747\,\varepsilon_r}{1000\left(\varepsilon_r+\frac{3}{20}\right)} \tag{A.52}$$

$$c_0 = b_0 - \mathrm{e}^{-\frac{207\,u}{500}}\left(b_0-\frac{207}{1000}\right) \tag{A.53}$$

$$d_0 = \frac{347\,\mathrm{e}^{-\frac{281\,u}{500}}}{500} + \frac{593}{1000} \tag{A.54}$$

$$\varepsilon_{r,eff,o} = \varepsilon_{r,eff,f} + \mathrm{e}^{-co\,g^{d_0}}\left(a_0+\frac{\varepsilon_r}{2}-\varepsilon_{r,eff,f}+\frac{1}{2}\right) \tag{A.55}$$

Considering coupled MS lines additional parameters need to be defined:

$$Q_1 = \frac{1739\,u^{\frac{97}{500}}}{2000} \tag{A.56}$$

$$Q_2 = \frac{7519\,g}{10000} + \frac{189\,g^{\frac{231}{100}}}{1000} + 1 \tag{A.57}$$

$$Q_3 = \frac{\log\left(\frac{g^{10}}{\frac{9.76e^6\,g^{10}}{2.015e12}+1}\right)}{241} + \frac{1}{\left(\frac{5.48e^9}{15625\,g^6}+\frac{83}{5}\right)^{\frac{387}{1000}}} + \frac{79}{400} \tag{A.58}$$

$$Q_4 = -\frac{2\,Q_1}{Q_2\left(\frac{\mathrm{e}^{-g}-2}{u^{Q_3}}-u^{Q_3}\,\mathrm{e}^{-g}\right)} \tag{A.59}$$

$$Z_{0,e} = -\frac{Z_{0f}\,\sqrt{\frac{\varepsilon_{r,eff,f}}{\varepsilon_{r,eff,e}}}}{\frac{Q_4\,\sqrt{\varepsilon_{r,eff,f}}\,\eta}{377\,\sqrt{\varepsilon_{r,eff}}\left(W_{e,h}+\frac{667\log\left(W_{e,h}+\frac{361}{250}\right)}{1000}+\frac{1393}{1000}\right)}-1} \tag{A.60}$$

$$Q_5 = \frac{57\log\left(\frac{319}{500\left(g+\frac{517\,g^{\frac{243}{100}}}{1000}\right)}+1\right)}{50} + \frac{897}{500} \tag{A.61}$$

$$Q_6 = \frac{10\log\left(\frac{g^{10}}{\frac{9.7e^6\,g^{10}}{4.20e^{15}}+1}\right)}{2813} + \frac{10\log\left(\frac{299\,g^{\frac{577}{500}}}{500}+1\right)}{51} + \frac{461}{2000}$$
(A.62)

$$Q_7 = \frac{190\,g^2 + 10}{\frac{823\,g^3}{10}+1}$$
(A.63)

$$Q_8 = e^{-\frac{19\log(g)}{20} - \frac{3.2e^6\,g^5}{243} - \frac{13}{2}}$$
(A.64)

$$Q_9 = \log(Q_7)\left(Q_8 + \frac{2}{33}\right)$$
(A.65)

$$Q_{10} = \frac{Q_2\,Q_4 - Q_5\,e^{\frac{Q_6\,\log(u)}{u^{\log(Q_7)}\left(Q_8+\frac{2}{33}\right)}}}{Q_2}$$
(A.66)

The nominal characteristic line impedance can be defined with:

$$Z_{0,o} = -\frac{Z_{0f}\sqrt{\frac{\varepsilon_{r,eff,f}}{\varepsilon_{r,eff,o}}}}{\frac{Q_{10}\sqrt{\varepsilon_{r,eff,f}}\,\eta}{377\sqrt{\varepsilon_{r,eff}}\left(W_{e,h}+\frac{667\log\left(W_{e,h}+\frac{361}{250}\right)}{1000}+\frac{1393}{1000}\right)}-1}$$
(A.67)

resulting in the even mode and odd mode line impedance:

$$Z_{0,e} = Z_0\sqrt{\frac{\varepsilon_{r,eff}}{\varepsilon_{r,eff,e}}}\frac{1}{(1-(Z_0/377)(\varepsilon_{r,eff})^{0.5}\,Q_4)}$$
(A.68)

$$Z_{0,o} = Z_0\sqrt{\frac{\varepsilon_{r,eff}}{\varepsilon_{r,eff,o}}}\frac{1}{(1-(Z_0/377)(\varepsilon_{r,eff})^{0.5}\,Q_{10})}$$
(A.69)

was extended to n parallel lines by the assumption that the effect of the coupling decreases with an increase of n by a simple quadratic polynom:

$$n_{fit} = -8.919e^{-4}n^2 + 0.804\,n + 0.2174$$
(A.70)

to result in:

$$Z_{0,en} = Z_{0,e}\,n_{fit}{}^{-1} \qquad Z_{0,on} = Z_{0,o}\,n_{fit}{}^{-1}$$
(A.71)

A.3 Amplifier Nomenclature

The dc power consumption of an amplifier is the sum of the drain and gate power:

$$P_{dc} = \{V_{GS} \cdot I_{gate}\} + \{V_{DS} \cdot I_{drain}\}$$
(A.72)

The input as well as output power of an amplifier depends on the definition of the reference-plane, the frequency as well as the reference impedance. For an amplifier the typical reference plane is the input and output connector

$$P_{in} = P_{in}(f) = \frac{1}{2}Re\{V_{in} \cdot I_{in}^*\}$$
(A.73)

$$P_{out} = P_{out}(f) = \frac{1}{2}Re\{V_{out} \cdot I_{out}^*\}$$
(A.74)

The gain of the amplifier is simply:

$$gain = \frac{P_{out}(f)}{P_{in}(f)}$$
(A.75)

To calculate the efficiency only the output power is set in relation to the dc power consumption:

$$\eta = \frac{P_{out}(f)}{P_{dc}} \cdot 100\,\%$$
(A.76)

By considering the gain instead of only the output power the power added efficiency is defined:

$$PAE = \frac{P_{out}(f) - P_{in}(f)}{P_{dc}} \cdot 100\,\% = \eta \cdot \left(1 - \frac{1}{gain}\right)$$
(A.77)

The difference between output power and dc power consumption represents the dissipated power, while the input power P_{in} can often be neglected for high gain amplifiers:

$$P_{diss} = P_{dc} - P_{out}$$
(A.78)

Given a two-stage amplifier the total gain can be derived into the gain of the first stage (gain Q1) and the second stage (gain Q2). The same can be done for their drain efficiencies.

$$gain\,Q1 = \frac{P_{Q1}}{P_{in}} \qquad \eta\,Q1 = \frac{P_1}{P_{dc,Q1}} \cdot 100\,\%$$
(A.79)

$$gain\,Q2 = \frac{P_{out}}{P_{Q1}} \qquad \eta\,Q2 = \frac{P_{out}}{P_{dc,Q2}} \cdot 100\,\%$$
(A.80)

As a result, the total drain efficiency is:

$$\frac{\eta}{100\,\%} = \frac{P_{out}}{P_{dc,Q1} + P_{dc,Q2}} = \frac{P_{out}}{\frac{P_{Q1}}{P_{dc,Q1}} + \frac{P_{out}}{P_{dc,Q2}}}$$

$$= \frac{1}{\frac{1}{gain\,Q2 \cdot \eta\,Q1} + \frac{1}{\eta\,Q2}} = \frac{\eta\,Q1 \cdot \eta\,Q2}{\eta\,Q1 + \frac{\eta\,Q2}{gain\,Q2}} \quad (A.81)$$

In consequence, the PAE is:

$$PAE = \frac{G\,Q2 - \frac{1}{G\,Q1}}{(\frac{G\,Q2}{\eta\,Q2}) + (\frac{1}{\eta\,Q1})} \quad (A.82)$$

An increase in $\eta\,Q1$ affects $G\,Q1$ therefore, it is more convenient to analyse the PAE by defining a reduction of PAE

$$\Delta PAE = PAE_{Q2} - PAE \quad (A.83)$$

due to the addition of the driver stage $PAE_{Q1}=$

$$\frac{(PAE_{Q2} - \Delta PAE)(G\,Q1 - 1) \cdot PAE_{Q2}}{[\Delta PAE \cdot (G\,Q2 - 1) + PAE_{Q2}] \cdot G\,Q1 - PAE_{Q2}}.$$
$$(A.84)$$

For modulated signals the PAE needs to be calculated based on the average power level as well as the average gain:

$$PAE_{\text{MOD}} = \frac{P_{\text{out,avg}} - P_{\text{in,avg}}}{P_{dc}} \cdot 100\,\%$$

$$= \eta \cdot (1 - \frac{1}{G}) \quad (A.85)$$

A.4 Simulation Techniques

Circuit Simulation

Nowadays, circuit simulation is widely used for hardware design within low- and of-course high-frequency applications. Microwave circuit simulation solves widely known techniques in its design environment. The CAE simulation tools ADS[1] or MWO[2] are the most common candidates in the market.

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[1]Advanced Design System (Keysight)
[2]Microwave Office (AWR)

The knowledge of the implemented Algorithm is nevertheless necessary to get a basic understanding. Especially during system faults a deeper understanding eases the debugging.

DC Simulation

A DC-simulation is carried out before any frequency analysis of a circuit within the CAE tools. The DC-simulation mainly solves Kirchhoff's equation for all notes of the circuit. Initially, all sources were set to an equal constant value ($\frac{dv}{dt}, \frac{di}{dt} = 0$). A capacitor represent an open, while an inductor is represented via a short. In conclusion the solution of this analysis depends on biasing within this *equilibrium analysis* and represents one possible solution. This solution does not necessarily needs to be the only possible solution.

Nearly all CAE tools rely on a SPICE method which relies on the use of a netlist to connect the components and the nodes. This Nodal Admittance Matrix is solved iteratively. Afterwards, a linearisation technique takes place that flattens all the step depended dc solutions by the usage of a Taylor series expansion [Kun95].

AC Simulation

Non constant signals are normally analysed through the use of an AC–simulation. Most analysis regarding AC–, XF–, or S-Parameter–Analysis rely on the so-called Phasor-Analysis. The small-signal reaction of a circuit is analysed for a certain number of frequencies. Amplitude as well as the phase response of this circuit are defined for its fundamental wave. The circuit's response always relies on the implementation of only one frequency, which is why no transient behaviour can be covered.

Transient Simulation

For circuits with non converging operation points the Transient-Analysis takes place. This time-domain analysis solves the partial differential

equations of the circuit stepwise of numeric approximations. The analysis of highly non-linear circuits, therefore leads to a high settling time which leads to a high simulation time. To compromise for the simulation time, some pseudo transient-analysis tools limits all used capacitors to 1 F, reducing the amount of various differential equations and in conclusion achieving the settling time faster.

Harmonic–Balance Simulation

For analysing non-linear high-frequency circuits, almost exclusively Harmonic–Balance (HB) simulations were used. The technique is particularly good for the analysis of large-signal simulations. All components of the circuit were analysed individually in the frequency-domain. The components are therefore per definition stable and their settling time is achieved. The whole circuit is afterwards divided into parts that can easily be explained linearly and those who parts which need a non-linear representation. The linear part of the circuit can be solved by using the time-domain techniques to evaluate the operation points.

Subsequently, different solving techniques were used for various large-signal input signals. A single, multi-tone or a pulsed-tone excitation needs different large-signal HB solving algorithms. For example, a Volterra-Series algorithm can be used to solve weak non-linear systems. For components with a high quality factor the HB analysis can find a solution faster than any other analysis that needs to rely on a steady state situation.

In comparison to the Transient simulation the HB simulation is not generalised for various signal types.

Electro–Magnetic Simulation

Very simple geometrical structures can be explained analytically. Yet even for a simple capacitor that mainly relies on two parallel plates, the fringing at the edges is difficult to approximate analytically. Therefore numerical solutions of the Maxwell

Equations, or a special adaption of its, are used to solve these structures.

Maxwell described solutions for macroscopic structures by the definition of an electro ($\vec{E}$) as well as a magnetic ($\vec{H}$) field. By using differential equations they can be summed up to:

$$rot\,\vec{E} \;=\; -\frac{\partial}{\partial t}\vec{B} \tag{A.86}$$

$$rot\,\vec{H} \;=\; \frac{\partial}{\partial t}\vec{D}+\vec{J} \tag{A.87}$$

$$div\,\vec{D} \;=\; \varrho \tag{A.88}$$

$$div\,\vec{B} \;=\; 0 \tag{A.89}$$

$$\oint_{\partial A}\vec{E}\cdot d\vec{s} \;=\; -\frac{d}{dt}\int_{A}\vec{B}\cdot d\vec{A} \tag{A.90}$$

$$\oint_{\partial A}\vec{H}\cdot d\vec{s} \;=\; \int_{A}(\frac{\partial\vec{D}}{\partial t}+\vec{J})\cdot d\vec{A} \tag{A.91}$$

$$\oint_{\partial V}\vec{D}\cdot d\vec{A} \;=\; \int_{V}\varrho\,dV \tag{A.92}$$

$$\oint_{\partial V}\vec{B}\cdot d\vec{A} \;=\; 0 \tag{A.93}$$

To build a bridge between the electric field $\vec{E}$ and its potential $\vec{D}$ as well as between the magnetic field $\vec{H}$ and the current density $\vec{J}$ the material equations were stated:

$$\vec{D} \;=\; \varepsilon\vec{E} = \varepsilon_0\varepsilon_r\vec{E} \tag{A.94}$$

$$\vec{B} \;=\; \mu\vec{H} = \mu_0\mu_r\vec{H} \tag{A.95}$$

$$\vec{J} \;=\; \kappa\vec{E} + \vec{J}_e \tag{A.96}$$

For solving geometrical structures with these equations they need to be discretisized within substructures. For each substructure the EM fields can be locally solved. The substructures are filled by the definitions according to the material equation, being either conductive or isolators. By the definition of special boundary conditions [3] all the substructures sum up to the previously defined geometrical structure.

The time-domain approximation can be transformed into the frequency-domain. Each spectral represent is defined by an amplitude and phasor.

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[3]For an equal electrical potential on the Dirichlet- boundary, an equal magnetical potential is called Neumann-boundary while neither of both represent an Open-boundary

Finite Difference Method (FDM)

Finite difference methods use numerical techniques to approximate the differential equations (E.g. Maxwell) with difference equations. FDM can therefore be stated as an discretization method. Eq. A.97 states a discretization with $f'(x_i)$ being the numerical approximation of f. The sum of all derivatives form a Taylor series which is the total approximation of the differential equation.
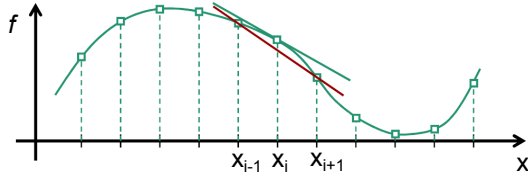
$$f'(x_i) = \frac{f(x_i + \Delta) - f(x_i - \Delta)}{2\Delta} + \Theta(\Delta)^2 \quad \text{(A.97)}$$

The number of used steps (i) or the distance in between determines the accuracy of the approximation. Yee defined a finite differences method for the time-domain (FDTD) which is especially useful for its application in the microwave engineering. The differnziation takes place, for the spatial orientation as well as for the time derivative. Both derivatives build a grid along their discretization step width. By definition both grids are allocated to each other, which lowers the access time. One drawback of this technique is that the whole structure needs to be solved for each excitation port separately. By using a high amount of excitation ports the amount of time increases.

Finite Integration Method (FIT)

The finite integration method (FIT) is a relative of FDTD. It is especially designed for the use with Maxwell's Equations and it is possible to achieve near lossless discretization. The original partial differential equations can be interpreted within two differently allocated grids of the FIT. Within these grid related Maxwell equations (Eq. A.98-A.105) the electrical $\widehat{e_n}$ and magnetical $\widehat{h_n}$ boundary potentials are defined exactly on the gridline. The electrical- and $\widehat{\widehat{d_n}}$ magnetical-flux $\widehat{\widehat{b_n}}$ enforce the surface which is surrounded by this discretisized gridlines. Muliple Source- (S) and Curl-Matrix (C)

span the grid. This primary grid (Matrix S, C) remains perpendicular to a secondary grid (Matrix $\tilde{S}, \tilde{C}$) which eases the operations in between both Matrixes ($C = \tilde{C}^T$).

$$\oint_{\partial A} \vec{E} \cdot d\vec{s} = -\frac{d}{dt} \int_A \vec{B} \cdot d\vec{A} \quad \text{(A.98)}$$

$$\Rightarrow C\widehat{e} = -\frac{d}{dt}\widehat{\widehat{b}} \quad \text{(A.99)}$$

$$\oint_{\partial A} \vec{H} \cdot d\vec{s} = \int_A (\frac{\partial \vec{D}}{\partial t} + \vec{J}) \cdot d\vec{A} \quad \text{(A.100)}$$

$$\Rightarrow \tilde{C}\widehat{h} = \frac{d}{dt}\widehat{\widehat{d}} + \widehat{j} \quad \text{(A.101)}$$

$$\oint_{\partial V} \vec{D} \cdot d\vec{A} = \int_V \varrho \, dV \quad \text{(A.102)}$$

$$\Rightarrow \tilde{S}\widehat{\widehat{d}} = q \quad \text{(A.103)}$$

$$\oint_{\partial V} \vec{B} \cdot d\vec{A} = 0 \quad \text{(A.104)}$$

$$\Rightarrow S\widehat{\widehat{b}} = 0 \quad \text{(A.105)}$$

The only approximation of this anaylsis relies in the approximation of the material definitions. For example, the permmitivity and conductivity is averaged along the surface of the grid. While the permeability is approximated along the gridlines.

$$\widehat{\widehat{d}} = M_\varepsilon \widehat{e} \quad \text{(A.106)}$$

$$\widehat{\widehat{b}} = M_\mu \widehat{h} \quad \text{(A.107)}$$

$$\widehat{\widehat{j}} = M_\kappa \widehat{e} \quad \text{(A.108)}$$

The FIT method is suitable for use within the frequency, as well as for transient fields in the time-domain. It is one of the most stable and fastest real 3-D EM-Solver commercially implemented in CST[4].

Finite Element Method (FEM)

The finite element method discretises the geometrical object into differently sized frameworks. The different sizes of the framework can be more easily solved on its own as this would be the case if all frameworks represent the same size. The boundary between all frameworks is constant as already described for the FDTD boundary conditions. This

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[4]Computer Simulation Technology (Dassault Systemes 3DS)

technique is applied in a real 3-D EM-Solver commercially implemented into HFSS[5] or EM-Pro [6].

Moment Method (MoM)

The method of moments only discretisizes the conductive parts of the geometrical structure. The planar dielectricel part is seperately approximated for one unit-cell (Substrate Matrix). One additional advantage of this technique is, that only one Matrix is defined for the whole structure. Therefore, an increased number of excitation ports does not increase the calculation time. The solving algorithm relies on the Green's equation. It is one of the commonly used techniques to solve planar (2.5-D) structures of printed circuit board application.

A.5 Measurement Uncertainty

Small-Signal Uncertainties

The measurement uncertainty of a probed test circuit is going to be visualized in Fig. A.1. The GSOLT calibration setup of Fig. 2.14 is used with a HP8510c[TM], two 1000 μm Z-Probes[TM] and a 5 mm long RO4003c MS line. Fig. A.1(a) shows that the whole measurement setup has an un-calibrated IL of up to 8 dB (25 GHz), while the un-calibrated RL is ≈ 25 dB due to the good matching of the VNA and the high residual losses caused by the IL of the cable and the probes.

Furthermore, the calibrated version of this measurement is displayed located at the reference-plane (GSOLT On-Wafer Cal.) through using a GSOLT Cal-Kit (Cascade CSR-15[TM]). The uncertainty of this measurement is caused by different types of errors. Taking advantage of the detailed uncertainty analysis of the METAS VNA-Tool different errors can be analysed separately [Wol+12]. By using a VNA with an excellent Drift the magnitude error is rather low (0.05 dB) for the transmission-case increasing towards higher frequencies Fig. A.1(c). The VNA Noise (-90 dBm/Hz

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[5]High Frequency Structure Simulator (Ansys)
[6]EM-Pro by ADS (Keysight)
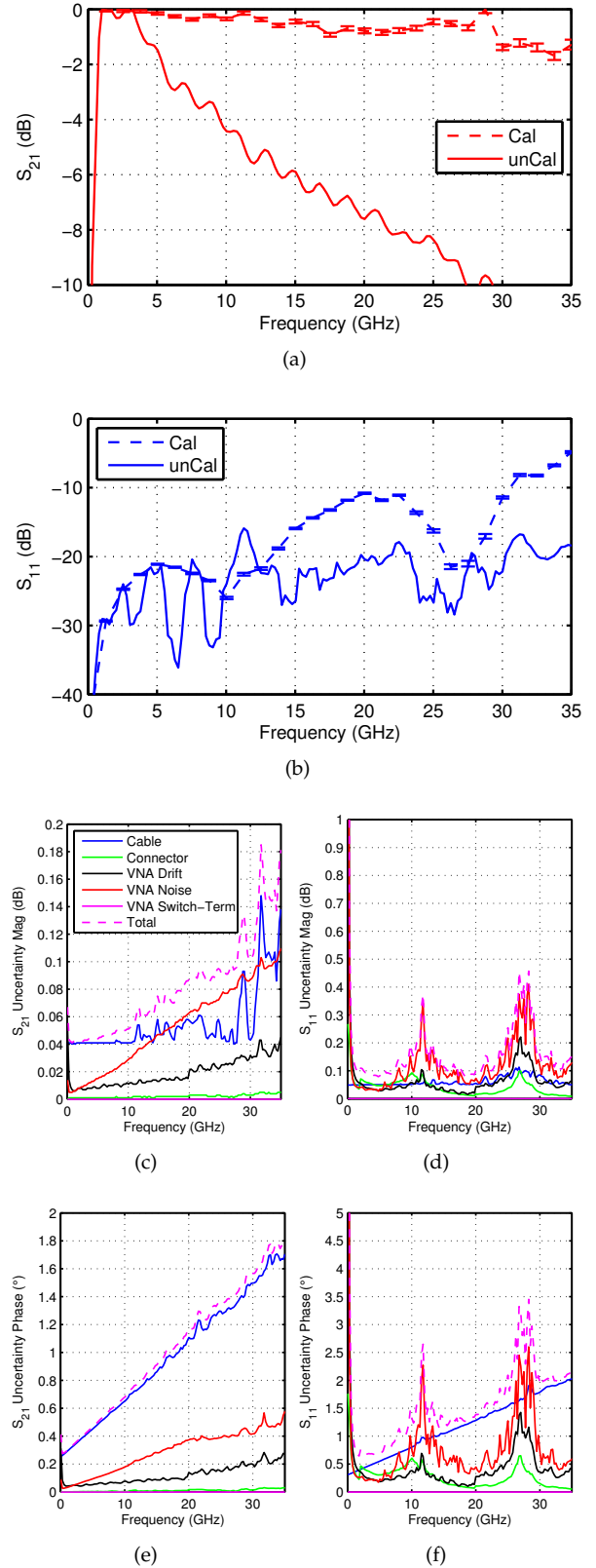
FIGURE A.1: Uncertainty analysis of probed TL (a) S_{21} (b) S_{11} (c) S_{21} unc. (d) S_{11} unc. (e) S_{21} phase unc. (f) S_{11} phase unc.

at 30 GHz) causes the largest uncertainty of up to (0.1 dB), while the isolation and directivity of the switch-terms the lowest. A high connectivity repeatability was assumed causing only a low uncertainty. In addition, possible cable movement can be approximated by the phase and magnitude variances described by the manufacturer. The total magnitude uncertainty can be explained with 0.15 dB for the magnitude (at 30 GHz) in the transmission path. While the reflection uncertainty sums up to 0.4 dB for the magnitude (at 30 GHz). The total phase uncertainty sums up to 1.5° for the transmission and up to 3° for the reflection.

This analysis lacks of the knowledge related to the calibration standard repeatability. Moreover, the low RL of the Z-Probe^{TM}($\leq$ 20 dB at 30 GHz) was only taken into account for the calibration. Its residual errors were not stated separately as a phase or magnitude uncertainty while it will probably causes the highest error of all. Cascade limits the upper operation frequency of their probes in relation to the pitch between the fingers. For GSG-Probes the upper operation frequency can be calculated regarding the pitch and the error as shown in Tab. A.1. For the use of 500 μm pitch probes at 14 GHz a measurement error of 2% can be assumed.

TABLE A.1: Measurement uncertainty of 500 and 1000 μm pitch GSG Z-Probes^{TM}

	error (%)	GSG 500	GSG 1000
max. f (GHz)	1	9.5	4.8
max. f (GHz)	3	19.1	9.5
max. f (GHz)	5	38.1	19.1

Large-Signal Uncertainties

The Large-Signal related uncertainties of the measurement setup given in Fig. 2.15 can be visualized by its statistical distribution. This way, 10000 samples were generated with varying phasors changing the Γ_{in} and Γ_{out} for a fixed RL of 14 and 20 dB. The statistical distribution is given in Fig. A.2. For the input-side a Kurtosis of 1.91 was obtained while the output-side shows a Kurtosis of 2.95 indicating a nearly normal distribution. It can be

obtained that introducing a higher mismatch at the DUT related plane significantly increases the measurement uncertainty. Taking the RL of 14 dB at the input coupler into consideration the measurement uncertainty increases up to $P_{in, unc} = 0.14$ dB as a mean value. For the output coupler the $P_{out, unc}$ arises up to 0.31 dB mean.

(a) $P_{in, unc}$ (b) $P_{in, unc}$

(c) $P_{out, unc}$ (d) $P_{out, unc}$
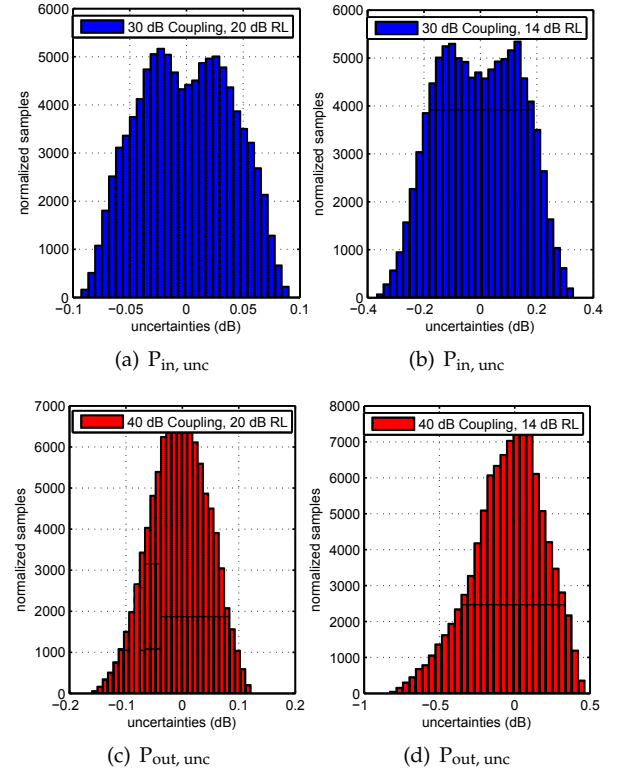
FIGURE A.2: Statistical distribution for a RL = 20 dB and a RL = 14 dB for (a),(b) input (c),(d) output coupler.

A.6   Link Nomenclature

Link calculation

The transmit power directed from a station towards the satellite is defined as the Effective Isotropic Radiated Power (EIRP). It is calculated based on the output power of the BUC (P_{out}) and the effective TX antenna gain $G_{A,TX}$. Losses in between the BUC and the antenna (IL$_{cable}$) degrade the EIRP which can be defined:

$$EIRP_{up} = P_{out} - IL_{cable} + G_{A,TX}. \qquad (A.109)$$

Additional mis-point losses (Att_{mis} = 0.3 to 1 dB) degrade the transmitted power. Rain losses (Att_{rain} = 0.3 to 6 dB) occur depending on the global position of the earth-station. ITU-R rain fade calculations can be done, which can be scaled depending on the overall year availability (like 99.5%). Att_{atm} depicts the atmospheric absorption. These physical losses can be summed up to (Att_{phys}):

$$\text{Att}_{\text{phys}} = \text{Att}_{\text{mis}} + \text{Att}_{\text{rain}} + \text{Att}_{\text{atm}} \quad (A.110)$$

The main losses of a satellite link are related to the free-space attenuation (L_{space}) which depends on the used frequency (f) and the distance to ground ($d \approx 35786$ km):

$$\text{L}_{\text{space}} = \left(\frac{4\pi \cdot d \cdot f}{c_0} \right)^2 \quad (A.111)$$

with c_0=299.710 km/s. The receiving carrier power at the satellite can be simply calculated by:

$$C = EIRP_{up} - \text{Att}_{\text{phys}} - \text{L}_{\text{space}} + G_{\text{A,RX}} \quad (A.112)$$

To determine the noise within a system the equivalent noise power (N) can be calculated based on the used bandwidth (B) the temperature of the receiving system (T_{RX}) and the Boltzmann constant (k=1.38e^{-23} W/Hz K).

$$N = k \cdot T_{RX} \cdot B \quad (A.113)$$

The receiving system noise temperature (T_{RX}) is given by the sum of the antenna noise temperature ($T_{A,RX}$) and the effective noise temperature of the receiver (T_R).

$$T_{RX} = T_{A,RX} + T_R \quad (A.114)$$

Considering the losses of a feeder (IL_{feed}) and a LNA (T_{LNA}) the equation has to be extended to:

$$T_{RX} = \frac{T_{A,RX}}{IL_{feed}} + \frac{IL_{feed} - 1}{IL_{feed}} \cdot T_0 + T_{LNA} \quad (A.115)$$

for the ambient temperature T_0=290 K. As a figure of merit the sensitivity of the receiver can be depicted by the term $\frac{G_{\text{A,RX}}}{T_{RX}}$ which is G/T. Thus, the uplink carrier power can be linear set into relation to the satellite receiving noise by:

$$\text{C/N}_{up}(\text{th}) = EIRP_{down} \cdot \frac{1}{\text{Att}_{\text{phys}}} \cdot \frac{1}{\text{L}_{\text{space}}} \cdot \frac{G_{\text{A,RX}}}{N} \quad (A.116)$$

This C/N is only related to a thermal noise and can be therefore named C/N (th). The calculation can also be applied for the downlink:

$$\text{C/N}_{down}(\text{th}) = EIRP_{down} \cdot \frac{1}{\text{L}_{\text{space}}} \cdot \frac{1}{\text{Att}_{\text{phys}}} \cdot \frac{G_{\text{A,RX}}}{N} \quad (A.117)$$

The same budget can be calculated for the downlink pointing from the satellite to the receiving earth-station. Important is the knowledge, that both C/N of the uplink (C/N_{up}) as well as the downlink (C/N_{down}) needs to be taken into account to determine the total C/N. While normally, the uplink C/N_{up} is significantly higher than the downlink C/N_{down} and often negligible.

$$\text{total C/N(th)} = \left((\text{C/N}_{up})^{-1} + (\text{C/N}_{down})^{-1} \right)^{-1} \quad (A.118)$$

Intermodulation distortion can occur in between satellites based on the sum of all side-lobes directed from the earth to the satellite. The uplink interference I is the sum of all interfering sources ($I = \sum I_i$). If the interfering uplinks are known they can be calculated based on the their orbital separation. Otherwise an adjacent satellite interference value can be assumed, considering the orbital location of the satellite pointing to ($C_{sat}/ASI_0 = \approx 132$ dB/Hz). This intermodulation distortions have the character of an additive thermal noise - which is why it can be easily added to the previous C/N calculations:

$$\text{total C/(N+I)} = \text{total C/N(th)} \| \text{C/I})^{-1} \quad (A.119)$$

For analysing the budget based on digital systems we can define the Energy per modulated symbol (E_s) with the code rate (R_c FEC) and the modulation rate (R_m). The Energy per bit (E_b) can be calculated for BPSK with M=2 or QPSK:M=4... :

$$E_s = R_m \cdot R_c \cdot E_b \quad \text{with} \quad R_m = log_2 \cdot M \quad (A.120)$$

With the knowledge of the bit rate (br) and the bandwidth (B):

$$C/N = E_b/N_0 \cdot \frac{br}{B} \qquad (A.121)$$

the C/N can be converted into the measure of signal to noise ratio for digital communication systems (E_b/N_0). The Energy per bit (E_b) is related to the spectral noise density (N_0) defined as E_b/N_0. By the usage of forward error correction the ideal E_s/N_0 can be taken as the reference for a C/N distance with the knowledge of the bandwidth (B) and the datarate (dr).

$$E_s/N_0 = C/N \cdot \frac{B}{dr} \qquad (A.122)$$

The definition of E_b/N_0 can be extended by additional intermodulation, as already shown for the C/N, by $E_b/(N_0+I_0)$, or $E_s/(N_0+I_0)$ for a certain modulation.

HUB to VSAT Link-Budget

A $\varnothing$ 4.6 m dish (ND SatCom) provides a 5 MSym/s QPSK uplink (DVB-S1) as HUB station. The TX antenna gain is 55 dBi which is powered by a BUC delivering $P_{out} = 10$ W resulting in up to 65 dBW EIRP. The Link-Budget is described in Tab. A.2. The RTL fom Easystar to the HUB is calculated based on a 1.2 MSym/s QPSK uplinkas follows in Tab. A.3.

TABLE A.2: (a) Uplink calculation within the **FWL**; (b) Downlink calculation within the **FWL**; (c) resulting total link margin within the **FWL** (Munich to Eutelsat 33E; 13.939087 GHz (H) up; 11.13537 GHz (V) down; 5 MSym/s; QPSK; FEC 5/6; $\alpha = 0.35$; $P_{out} = 10$ W; 99.5% availability ITU-R)

(a)

uplink	clear sky	rain up	
uplink EIRP	63.97	63.97	dBW
transponder IBO	7.85	7.85	dB
IBO/carrier	17.41	19.09	dB
antenna mispoint	0.3	0.3	dB
free space loss	207.15	207.15	dB
total attenuation	0.17	1.82	dB
C/N (th)	22.87	21.23	dB
C/(N+I)	22.84	21.2	dB
$E_b/(N_0 + I_0)$	20.98	19.34	dB

(b)

downlink	clear sky	rain down	
sat EIRP	50.5	50.5	dBW
transponder OBO	5.18	5.18	dB
OBO/carrier	14.82	14.82	dB
antenna mispoint	0.3	0.3	dB
free space loss	205.2	205.2	dB
total attenuation	0.14	1.08	dB
total system noise	122.6	171.6	K
G/T	17.6	16.15	dB/K
C/N (th)	9.56	7.16	dB
$E_b/(N_0 + I_0)$	7.62	5.25	dB

(c)

totals per carrier (end to end)	clear sky	rain up	rain down	dual fade	
C/N (th)	9.36	7.72	7.04	5.4	dB
C/(N+I) = $[E_s/(N_0 + I_0)]$	9.29	7.67	7	5.37	dB
system margin	1	1	1	1	dB
net $E_s/(N_0 + I_0)$	8.29	6.67	6	4.37	dB
required $E_s/(N_0 + I_0)$ (for QPSK)	5.18	5.18	5.18	5.18	dB
excess margin	3.11	1.49	0.82	-0.81	dB

TABLE A.3: (a) Uplink calculation within the **RTL**; (b) Downlink calculation within the **RTL**; (c) resulting total link margin within the **RTL** (Berlin to AM44; 13.93537 GHz (H) up; 11.113087 GHz (V) down; 1.2 MSym/s; QPSK; FEC 2/3; $\alpha = 0.35$; $P_{out} = 10$ W; 99.5% availability ITU-R)

(a)

uplink	clear sky	rain up	
uplink EIRP	48	48	dBW
transponder IBO	7.85	7.85	dB
IBO/carrier	33.18	34.83	dB
antenna mispoint	0.3	0.3	dB
free space loss	207.23	207.23	dB
total attenuation	0.18	1.83	dB
C/N (th)	13.38	11.73	dB
C/(N+I)	13.36	11.71	dB
$E_b/(N_0 + I_0)$	13.71	12.06	dB

(b)

downlink	clear sky	rain down	
sat EIRP	50.5	50.5	dBW
transponder OBO	5.18	5.18	dB
OBO/carrier	30.51	30.51	dB
antenna mispoint	0.3	0.3	dB
free space loss	205.18	205.18	dB
total attenuation	0.14	1.06	dB
total system noise	200.29	245.76	K
G/T	28.6	27.7	dB/K
C/N (th)	10.78	8.96	dB
$E_b/(N_0 + I_0)$	11.03	9.41	dB

(c)

totals per carrier (end to end)	clear sky	rain up	rain down	dual fade	
C/N (th)	8.88	7.23	7.62	5.97	dB
C/(N+I) = $[E_s/(N_0 + I_0)]$	8.8	7.17	7.57	5.93	dB
system margin	1	1	1	1	dB
net $E_s/(N_0 + I_0)$	7.8	6.17	6.57	4.93	dB
required $E_s/(N_0 + I_0)$ (for QPSK)	3.1	3.1	3.1	3.1	dB
excess margin	4.7	3.07	3.47	1.83	dB

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