Technische Universität Berlin

60- and 122-GHz SiGe BiCMOS Transceivers for FMCW Radar Applications

vorgelegt von

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von der Fakultät IV – Elektrotechnik und Informatik
der Technischen Universität Berlin
zur Erlangung des akademischen Grades
Doktor der Ingenieurwissenschaften (Dr.-Ing.)
genehmigte Dissertation

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Tag der wissenschaftlichen Aussprache: 30.04.2020

Berlin 2020

Abstract

The continuous need for high-performance transceivers with demanding parameters for huge industries targeting important radar applications are driving researchers to search for ways to improve the fabrication technologies, circuit topologies and system architectures. A considerable care should be exercised to achieve compact wideband chips at high frequencies with high output power and low power consumption built using low-cost technologies so that important radar metrics such as the detection range, resolution and accuracy could be further enhanced. As much as the core circuit, the overall performance is also determined by the designed package, antenna and baseband signal processing system. Therefore the whole process in designing a high-end complete product available in large volumes requires a combination of many factors, and in hierarchy, transceiver designs should be optimized based on the system requirements and the available packaging technology.

In this dissertation, the design steps, simulation and measurement results of fabricated transceiver chips to be utilized in FMCW radar applications are described. These MMICs which are built using 130 nm SiGe BiCMOS technology include single-channel monostatic, double-receive-channel and multi-channel transceiver versions operating within the ISM bands allocated around 60- and 122-GHz. With these compact chips, high detection range and resolution could be provided, thanks to their high EIRP and operation bandwidth. For the initial tests, the chips are wirebonded to high frequency substrates including wirebond compensation networks and on-board antennas. On the other hand, various package solutions for high frequency integration are developed and the measurement results of the manufactured samples are shared. Finally using the designed radar evaluation boards, real-time FMCW radar tests are conducted and successful target range detection measurements are achieved. Based on these results, it proves the suitability of the designed transceiver modules in FMCW radar applications requiring high radar range, resolution and accuracy.

Zusammenfassung

Der ständig steigende Bedarf an Transceivern mit anspruchsvollen Leistungs-Parametern für wichtige Industriezweige, die auf Radaranwendungen abzielen, motiviert Forscher, nach Wegen zu suchen, um Herstellungstechnologien, Schaltungs-Topologien und Systemarchitekturen zu verbessern. Es muss großer Aufwand darauf gerichtet werden, kompakte Breitbandchips mit hohen Frequenzen und hoher Ausgangsleistung sowie geringem Stromverbrauch zu entwickeln, die unter Verwendung kostengünstiger Technologien hergestellt werden, damit wichtige Radar-Parameter wie Erfassungsbereich, Auflösung und Genauigkeit weiter verbessert werden können. Genau wie der HF- Kern Leistungsfähigkeit wird auch die Gesamtleistung durch das verwendete Package, die Antenne und das Basisbandsignalverarbeitungssystem bestimmt. Daher erfordert der gesamte Prozess zum Entwickeln eines High-End-Komplettprodukts, das in großen Stückzahlen produziert werden soll, eine Kombination vieler Faktoren. In der Hierarchie sollten die Transceiver-Designs auf der Grundlage der Systemanforderungen und der verfügbaren Packaging-Technologie optimiert werden.

In dieser Dissertation werden die Entwurfsschritte sowie die Simulations- und Messergebnisse der hergestellten Transceiver-Chips für FMCW-Radaranwendungen beschrieben. Diese MMICs, die mit der 130-nm-SiGe-BiCMOS-Technologie hergestellt werden, umfassen einkanalige monostatische, zweikanalige und mehrkanalige Transceiver-Versionen, die innerhalb der ISM-Bänder mit 60 und 122 GHz arbeiten. Mit diesen kompakten Chips können dank ihrer hohen EIRP und Operationsbandbreite ein hoher Erfassungsbereich und eine hohe Auflösung erreicht werden. In den ersten Tests werden die Chips mit Hochfrequenzsubstraten, einschließlich Wirebond-Kompensationsnetzwerken und On-Board-Antennen, verkabelt. Zum anderen werden verschiedene Paketlösungen für die Hochfrequenzintegration entwickelt und die Messergebnisse der gefertigten Proben ausgetauscht. Schließlich werden unter Verwendung der entworfenen Radar Evaluation Boards Echtzeit-FMCW-Radartests durchgeführt und erfolgreiche Zielbereichserkennungs- Messungen erzielt. Basierend auf diesen Ergebnissen wird die Eignung der entworfenen Transceiver-Module für FMCW-Radaranwendungen unter Beweis gestellt, die eine hohe Radarreichweite, Auflösung und Genauigkeit erfordern.

Acknowledgements

First, I would like to express my gratitude to my supervisors, Dr. Wolfgang Winkler and Dr. Wojciech Debski in Silicon Radar GmbH for their continuous support and supervision. This thesis would not exist without the help of my supervisors and all my colleagues in Silicon Radar, where since the beginning I have gained a lot of experience and learned many things and still continuing to do so.

I would also like to especially thank my academic supervisor Prof. Dr.-Ing. habil. Dietmar Kissinger for his valuable advices and guidance throughout my entire PhD time. He gave me a lot of help and support which led me complete the thesis. Furthermore I am also grateful to Prof. Dr.-Ing. Friedel Gerfers and Prof. Dr.-Ing. Wolfgang Heinrich for evaluating this work and providing rewarding feedbacks.

I owe many thanks to my former supervisors, Prof. Ibrahim Tekin, Prof. Yaşar Gürbüz, Prof. Meriç Özcan in Sabanci University and Dr. Mehmet Kaynak in IHP for being the guiding figures through my entire education life and encouraging me in orienting to this very special filed in electronics.

During my doctoral studies, I received motivational support from many colleagues. Thus I would like to acknowledge especially Berk Yilmaz and many others for their help in the realization of this work.

Last but not least, the most significant contribution to my life and studies was and will always be from my family. Therefore I would like to thank my parents, Zülal and Bener, and my sister Ece. And my uttermost gratitude goes to my beloved wife, Ezgi, for always being there for me. Without her support, motivation and continuous encouragement, I would not have finished this thesis and made it this far.

Contents

Abstract iv
Zusammenfassung v
Acknowledgements vii
Contents x
1 Introduction 1
1.1 Motivation 1
1.2 Thesis Outline 4
2 Radar Fundamentals 7
2.1 FMCW Radar Theory 7
2.2 Important Radar Metrics 10
2.3 Link Budget Calculation and Specification Extraction 12
2.4 Transceiver Architectures 13
2.4.1 Single-Channel Monostatic Transceiver 14
2.4.2 Double-Receive-Channel Transceiver 16
2.4.3 MIMO Transceiver 17
3 Design and Implementation of Radar Transceivers 21
3.1 Fabrication Technology Overview 21
3.2 General-Use Circuits Design 23
3.2.1 ESD Protection Structures 23
3.2.2 Bias Circuit Design 24
3.2.3 CMOS Inverter 25
3.3 Receiver Channel Design 25
3.4 Transmitter Channel Design 40
3.5 LO Signal Generation and Distribution Network 47
3.5.1 VCO Design 47
3.5.2 Frequency Divider Design 52
3.5.3 Multiplexer / LO Switch Design 56
3.5.4 Frequency Tripler Design 57
3.5.5 20-GHz PA Design 62
3.5.6 Power Divider Design 64
3.5.7 Complete MIMO LO Chain Simulation 68
3.6 Summary of the Designs 71
4 IC Measurement Results 73
4.1 Measurements of 60-GHz Double-Receive-Channel TRx 74
4.2 Measurements of 122-GHz Double-Receive-Channel TRx 78
4.3 Measurements of 60-GHz Monostatic TRx 82

4.4 Measurements of 122-GHz Monostatic TRx 86
4.5 Measurements of 60-GHz MIMO TRx 89
4.6 Summary of the Measurement Results 94
5 Antenna Design, IC Packaging and Interconnect Concepts 97
5.1 PCB-Based Antenna Concept of 60- and 122-GHz ICs 98
5.2 Silicon Package Concept of 60- and 122-GHz TRM ICs 108
5.3 BSA Package and Antenna Concept of 60-GHz TRM IC 115
5.4 LGA Package and Antenna Concept of 60-GHz ICs 117
5.5 EWLB Package and Antenna Concept of 60-GHz MIMO IC 126
5.6 Interposer packaging of 60-GHz TR2 IC 131
5.7 Summary of the Adopted Packaging and Antenna Solutions 132
6 FMCW Radar Measurements 135
6.1 FMCW Radar Evaluation Board 135
6.2 Real-time FMCW Radar Measurements 137
6.3 Summary of the FMCW Radar Measurement Results 142
7 Conclusion and Future Works 145
Bibliography xiii
List of Figures xxii
List of Tables xxxiii
List of Abbreviations xxxiv
List of Publications xxxvi

1 Introduction

1.1 Motivation

The increasing industrial demand for better transceiver designs orients researchers to develop innovative concepts in radar, imaging and communication systems where the application fields might vary from avionics and robotics to automotive and military. Specifically with the radars, various applications could be realized with being most widely exploited in automotive industry for autonomous driving, park assist, collision avoidance, blind-spot detection, lane-change assist systems [1] – [7]. Aside from the simple speed and distance measurements, high accuracy tank gauging, material thickness and life-sign detection measurements could be conducted as well [8] – [13]. Keeping these massive industries and the required specifications in mind, the designers should put a considerable effort in developing high-end modules advanced in power consumption, range, resolution, accuracy and data-rate performances. At this point such high volumes should as well be fabricated with low-cost and cutting-edge technologies, which reduces the number of available and suitable technologies to quite few. Furthermore this whole complicated process in the way of designing a complete product includes high performance chip and antennas, a well-defined packaging process with high yield and a very precise package interconnect scheme. The quality of baseband system would also affect the final benchmark of system. Therefore limitations in the total performance might arise from any of these which would even lead to application-wise failure.

Compared to many of the existing fabrication technologies, the low-cost SiGe technology has boosted its popularity thanks to the continuous advancements in process which has already been supported with various highly-integrated reliable industrial products especially at higher frequency bands targeting the ISM (Industrial-Scientific-Medical) bands at 24, 60, 122 GHz and even higher [13] – [33]. Other than the SiGe products at these frequencies, 77 GHz with 5 GHz bandwidth is specifically allocated for automotive applications coinciding with the 10 GHz bandwidth (75 – 85 GHz, [1] – [7], [34] – [38]) of industrial fluid level sensing systems while the imaging applications are aimed at 35, 94, 140 and 220 GHz where the attenuation is lower due to atmospheric windows (see Figure 1.1) [39] – [46]. On the other hand, many researches are conducted to move the communication application bands at 28 GHz to upper frequencies at 60, 140 and 240 GHz to benefit the high bandwidths allowing high data-rate transmission links in short range [47] – [53]. Even

though the current literature proves the maturity and suitability of SiGe process in obtaining high-end radar product that is attractive enough for these industries, it is still open for further advancements both in technology and transceiver design.

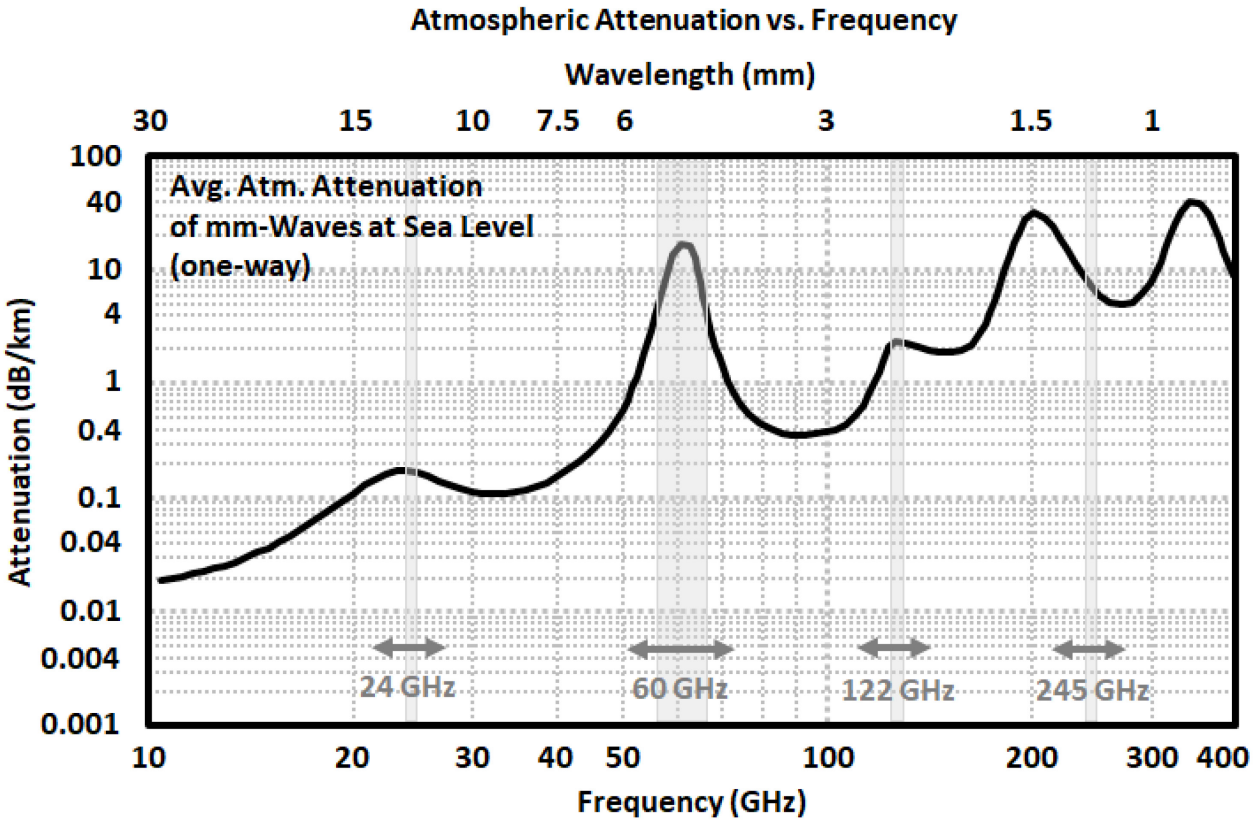

Figure 1.1: One-way average atmospheric attenuation of mm-Wave frequencies at sea level highlighting the common ISM bands.

Such high operation frequencies at ISM bands are of main focus while designing transceivers for radar applications. Because it naturally comes with antennas having low-form factor and MMICs consuming less die area, which help reducing the fabrication costs and designing compact modules. The requirement of achieving high accuracy benefits short wavelengths and, thanks to the allowed wide bandwidth operation, radar range resolution is increased at the same time. Especially for the 60-GHz band, the common allowed bandwidth reaches 7 GHz between 57 – 64 GHz (9 GHz bandwidth between 57 – 66 GHz in Europe) with a 55 dBmi equivalent isotropic radiated power (EIRP) level according to the European Telecommunication Standards Institute (ETSI) and a limitation of 10 dBm maximum generated output power. On the other hand, 1 GHz bandwidth (122 – 123 GHz) is allowed around the 122-GHz ISM band. Since the occupied area is much less, angular resolution would be boosted within couple folds lower area by employing multi-channel systems [1] – [3], [19], [37] – [40], [47] – [57]. However a disadvantage is that the detectable range of radar is limited by the gain and transmitted output power compared to their counterparts targeting

lower bands, which the fabrications processes extracts better performances at low frequencies. Path loss increases drastically at such high frequencies, thus gain boosting techniques on the antenna side should be utilized. Moreover the circuits could well be further upgraded to reach the most performance out of them to obtain the demanding radar requirements. Additionally, in case indoor applications are targeted where the field of usage is similar to in-tank or closed surrounding applications, such regulations of ETSI do not apply. Then larger operation bandwidths are naturally much easier to achieve compared to the designs operating at lower carrier frequencies and could be employed to improve the range resolution.

As important as the core circuit, performance of the selected package plays a crucial role for the end product. Its cost, reliability, effects on the performance parameters of transceiver core and availability for high volumes would be the most important criteria while choosing a suitable package. The packaged radar module would be somehow routed to antenna, in case of chips with off-chip antennas, to be employed in radar applications which puts stress in package development. Due to high operation frequencies, connection between chip and package fan-outs are practically limited to interconnects providing smaller inductances not to decrease the available bandwidth and output power. Even though wirebonds might still work at high frequencies around 122 GHz, they require compensation networks which further reduce the chip performance, yet provide a cheap solution [11], [12], [15] – [18], [30], [39], [41], [55] – [61]. On the other hand, technologies benefiting solder-balls in different forms and names generally offer an expensive solution and have different requirements with the currently available packaging options [1], [2], [20], [23], [24], [27], [28], [40], [51], [53], [62] – [67]. However they provide excellent high frequency performance regardless of the heat removal issue especially in power-hungry circuits which could be solved with additional manufacturing processes [68], [69]. In case of on-chip integrated antennas, such expensive interconnects, hence packages are not required since the high frequency sections are internally connected. But this time, the effect of package mold on antenna performance should be carefully investigated since it leads to surface wave excitation which would deteriorate the antenna performance [27], [58], [59], [66], [70], [71].

High performance antenna design is another aspect to be dealt with while designing a transceiver system. It possesses certain performance-defining metrics which in the end contribute to overall system performance in terms of improved link budget. Whether or not the antenna is integrated on chip or in package [12], [62], [63], [65], [66], [70] – [76], the trade-offs between cost, performance, integration difficulty and package suitability does exist. As the module operation frequencies get higher in order to benefit the available bandwidth, aperture sizes shrink so that the antennas could even fit inside the silicon substrate on which the chip is built [25], [36] – [39], [42], [44] – [46], [57], however a degraded performance must be awaited unless a huge silicon area is reserved for the antenna integration. Even in this case, the antenna performance is quite limited which is also a result of the lossy substrate decreasing the efficiency, yet the literature provides innovative solutions for increased on-chip antenna performance as well. PCB level designs offer high antenna directivity and flexibility [1], [3], [11], [16] – [18], [49] – [54], [56], but comes with the trade-off

between selected interconnect and overall system size and cost. However, especially for the transceiver units composed of high number of channels, such antenna designs on high frequency materials have various advantages, and also are almost impossible to place on chip. In other respects, performance boosting techniques for the radiating elements are applied by using 3D printed structures. In this case dielectric lenses (and other forms) are utilized to boost the antenna gain and increase the signal-to-noise ratio [13], [15] – [18], [25], [28], [43], [44], [46], [60], [73], [77], [78]. Adopting such methods on top of a high-performance antenna would improve the achievable range for both radar sensors and communication links. So depending on the requirements and knowing these trade-offs, researchers have developed various high quality antenna systems for the intended applications in the form of on-chip, in-package, on-package and on-PCB antenna solutions.

In this thesis work, transceiver ICs operating at 60- and 122-GHz ISM bands for FMCW radar applications are designed [15] – [19]. The technology is selected as low-cost 130 nm SiGe BiCMOS with f_t / f_{max} of 250 / 340 GHz. The very compact chips include single-channel monostatic transceivers aiming high detection range and double-receive-channel and MIMO transceivers aiming high angular resolution. In order to test the functionality of chips, evaluation boards with antennas having wirebond compensation networks are designed for the initial phase, and many of these are tested. Furthermore various packaging solutions, which are suitable for high frequency, are offered and the measurement results of the fabricated ones are shared. Since the remaining are still in fabrication process, only their simulation results are discussed. Nevertheless, high performance complete radar units are developed, fabricated, packaged and tested. Having achieved successful real-time radar measurements, it could be deducted that the proposed chips would perfectly fit in many applications targeting high performance FMCW radar operation.

1.2 Thesis Outline

The following chapters are organized as follows:

Chapter 2 discusses the basic concepts of FMCW radar theory and covers a ground on the important metrics of a radar system such as range, resolution, accuracy etc. and how they are measured. Then different radar architectures that are implemented in the scope of this work are studied and the advantages of each concept are reported. They include monostatic, double-receive-channel and MIMO transceivers around 60- and 122-GHz ISM bands. For the purpose of attaining high-performances out of these chips, certain metrics should be extracted and the final transceiver must comply with a defined link budget, which is calculated as well. These would determine the steps in defining system- and chip-level specifications.

Chapter 3 gives an insight into the fabrication technology and how the available active library components required for the transceiver design perform at the frequency bands of interest. This chapter presents the background theory of implemented circuits. In this context, receiver and transmitter channels and LO signal distribution network in all of the fabricated chips at 60- and

122-GHz are highlighted in detail with a great emphasis on design steps, important metrics of each sub-block and simulation results.

Chapter 4 brings the measurement results of the fabricated chips forward together with the measurement procedure. Measured performances of each chip are summarized in the end.

Chapter 5 mentions the other crucial components in order to realize a radar transceiver to be used in FMCW systems which could be classified as antenna, interconnects and packaging designs. Each of these concepts are investigated and implemented to achieve a high-performance complete transceiver product, and the important findings are shared.

Chapter 6 introduces the very basic radar signal processing procedure and the required board components to conduct such calculations. In the end, real-time FMCW measurements of radar evaluation boards, which contain these fabricated chips, are made. Target distance measurements are carried out and the results are displayed.

Chapter 7 gives an overall view of what have been realized in the context of this thesis work to obtain a high-performance transceiver module. Finally the thesis is concluded with possible future works that could further boost the performance of each unit.

2 Radar Fundamentals

This chapter aims to discuss the fundamentals of frequency-modulated continuous-wave (FMCW) radar and its system level implementation on the proposed transceiver ICs. Therefore modulation schemes, important metrics of radar and how they are derived are discussed. Based on such requirements, system concept is defined, link budget calculations are performed and chip-level specifications are extracted to apply in receiver and transmitter sub-blocks in order to achieve certain radar performance. Since different radar architectures improve these radar metrics differently, single- and multi-channel transceiver structures are implemented in the scope of this thesis. Additionally fundamental advantages of each with an emphasis on circuit block level arrangements are explained.

2.1 FMCW Radar Theory

Continuous-Wave (CW) radars are employed to detect the target velocity by measuring the Doppler shift of the received echo signal. Yet they lack in detecting the target range due to absence of the required time delay coming from its unmodulated nature. To overcome such issue, frequency modulation could be adopted as in FMCW radar systems in which an EM signal whose frequency is changing over time within a defined bandwidth is continuously transmitted.

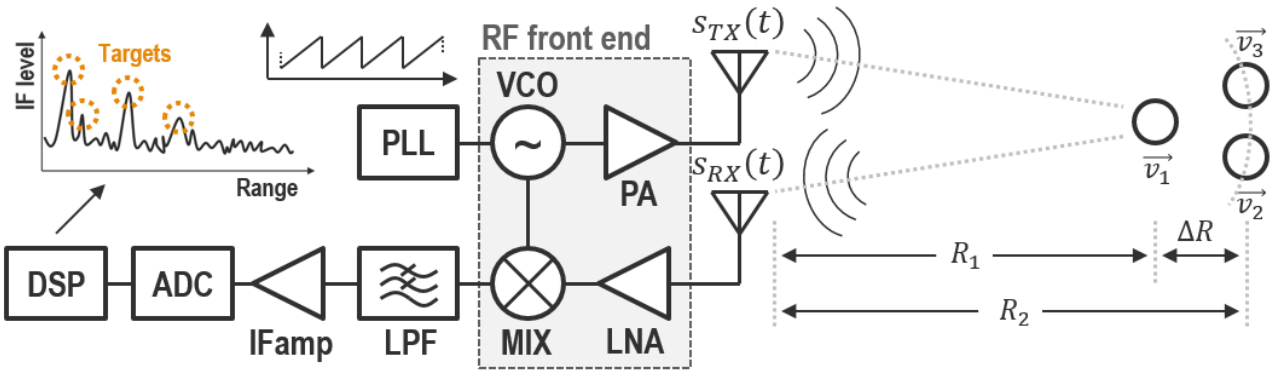

Figure 2.1: Block diagram of a typical target detecting radar system.

In a typical radar system shown in Figure 2.1, this operation is realized by a voltage-controlled-oscillator (VCO) whose frequency output could be adjusted generally in a linear fashion by a phase-locked-loop (PLL). A saw-tooth type ramp / chirp signal is used to control the generated frequency linearly between frequencies f_1 and f_2 (a start frequency of f_c with a bandwidth of BW) within the modulation period T_M by applying a varied voltage to the frequency tuning mechanism of VCO. This signal is then divided into two where one is amplified by a power amplifier (PA) and then transmitted through the antenna. This signal is reflected from the target and then captured by the receiver antenna with a propagation delay of Δt to be amplified by a low-noise amplifier (LNA) and down-converted to its intermediate-frequency (IF) – or its beat frequency, f_b – with the other mixing component being the second half of generated local oscillator (LO) signal. Owing to this delay, target range could be measured after analog-to-digital-converter (ADC) digitization and Fast-Fourier-Transform (FFT) signal processing. This is illustrated in Figure 2.2. In case of multiple target readings, multiples of the transmitted chirp signal would be received, each with its own f_b which are proportional to their distance from the radar, R. The detection of targets include peak identification in frequency domain whose power levels exceed a predefined threshold level above the noise floor. Moreover in case the object exhibits a relative velocity, its echo will carry a Doppler frequency shift of f_d. Since employing a single chirp would make the Doppler and range components of resulting IF spectra overlap and not separable, a frame of consecutive chirps (chirp train) is generated continuously. Then the velocity information is distinguished by taking a second FFT across the ramps within frame and figuring the phase shift between these ramps. The resulting process after successive FFTs is basically mapping the targets in a two-dimensional grid – so called range-doppler map – whose axes are range and velocity composed of many bins depending on the FFT procedure.

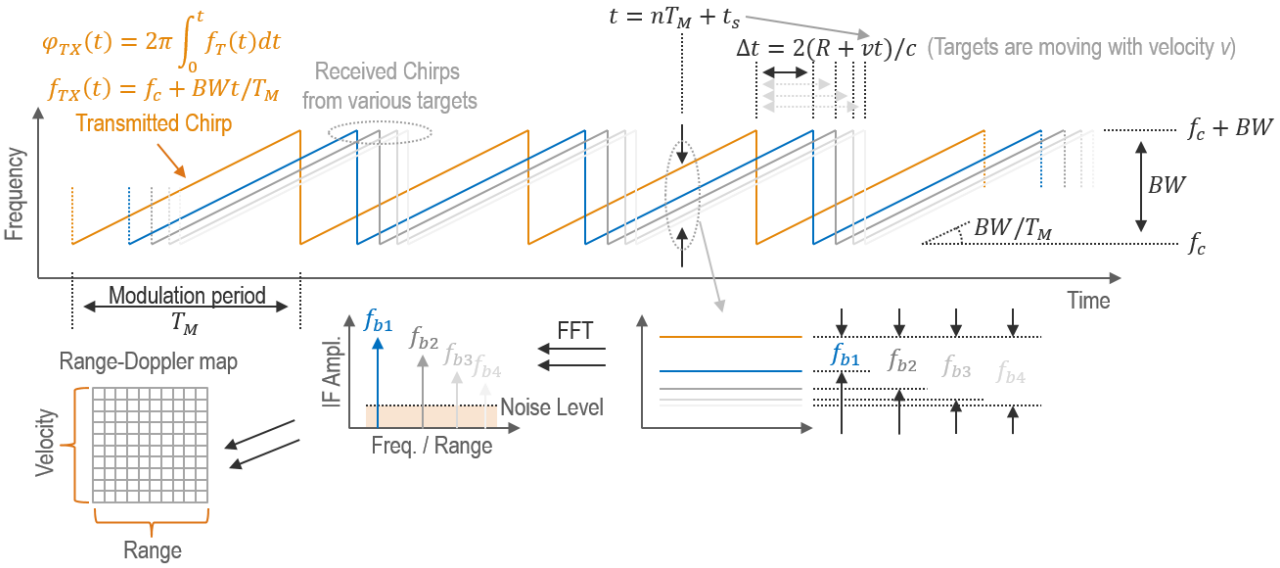

Figure 2.2: FMCW system illustration showing chirp modulation and beat frequency spectrum of the detected targets.

The generated and transmitted signal at starting frequency of f_c with a bandwidth of BW within modulation period of T_M, and its received echo from a moving target with a velocity of v from distance R after a time delay of Δt could be expressed as:

$$s_{TX}(t) = A_{TX}\cos(\varphi_{TX}(t)), \quad s_{RX}(t) = A_{RX}\cos(\varphi_{TX}(t-\Delta t)) \tag{2.1}$$

$$\varphi_{TX}(t) = 2\pi\int_0^t f_{TX}(t)\,dt, \text{ where } f_{TX}(t) = f_c + BW\cdot t/T_m \tag{2.2}$$

Using Eqn. (2.2) and substituting the terms in Eqn. (2.1) results in transmitted signal $s_{TX}(t)$ and received signal $s_{RX}(t)$:

$$s_{TX}(t) = A_{TX}\cos(2\pi\big(f_c(nT_M + t_s) + BW\cdot t_s^2/(2T_M)\big)) \tag{2.3}$$

$$s_{RX}(t) = A_{RX}\cos(2\pi\big(f_c(nT_M + t_s - \Delta t) + BW(t_s-\Delta t)^2/(2T_M)\big)) \tag{2.4}$$

The signal amplitudes, A_{TX} and A_{RX}, are based on the transmitted output power and received input power determined using the generic Friis radar equation, which takes the target radar cross section into account as well. Then their mixing products at the down-converter output defined by Eqn. (2.5), in its simplest form excluding the other mixing components due to leakage and harmonics, would become (in the case higher end sum-frequency component is filtered out):

$$s_{IF}(t) = s_{TX}(t)s_{RX}(t) \tag{2.5}$$

$$s_{IF}(t) = 0.5A_{TX}A_{RX}\cos(2\pi\big(f_c\Delta t + BWt_s\Delta t/T_M - BW\Delta t^2(2T_M)\big)) \tag{2.6}$$

The derivation of the target range is quite straightforward after this point when the delay term, Δt, is replaced as shown on Figure 2.2 with $2(R + v\cdot(n\cdot T_M + t_s))/c$. Neglecting the resulting small IF output components in the cosine function would result in an IF signal of:

$$s_{IF}(t) = 0.5A_{TX}A_{RX}\cos(2\pi(2BWt_sR/(c\cdot T_M) + 2vf_cnT_M/c) + 4\pi Rf_c/c) \tag{2.7}$$

From the above Eqn. (2.7) highlighting $s_{IF}(t)$, the IF signal frequency spectrum includes a fundamental frequency component of $BW\cdot 2R/(c\cdot T_M)$ as the first term which is named as the beat frequency, f_b which could be found after implementing an FFT on the IF signal over a signal period, and then translated into computation of target range, $R = f_b\cdot c\cdot T_M/(2BW)$. On the other hand, the second term gives a changing phase from the beat frequency with respect to number of sweeps due to the shift of Doppler frequency, $f_d = 2f_c\cdot v/c$, emanating from the target velocity. By rearranging the terms target velocity could be found by solving $v = f_d\cdot c/(2f_c)$. A second FFT is taken over n ramp periods on the top of the first FFT to map the velocity component in two-dimensional range-Doppler grid. Finally the third term in the IF signal cosine function gives the phase component that depends on target range.

In case multiple targets fall into the same range and doppler bin, such unambiguity could only be dealt with estimating the angular information of these targets. Angle of arrival could be extracted in case of multiple receive channels where each antenna receives the reflected signals with

certain phase shift depending on the distance between these radiating elements. In this case a fourth term is added inside the IF signal, being $k \cdot d \cdot sin(\theta)$ where d is the antenna separation, k is the k^{th} element in the receive channel array length of $k+1$ elements, which are generally spaced half wavelength apart, and θ is the angle of arrival with respect to the surface normal. To access such information, a third FFT could be applied on the down-converted signals from each antenna and comparing the phases.

2.2 Important Radar Metrics

There exist couple important metrics that defines the quality of a radar which could be classified on system level under maximum detectable range and velocity, range and velocity accuracy, range, velocity and angular resolution, and detection probability together with the false-alarm rate. Applying a certain chirp modulation allows formulating and determining the theoretical specifications base-line. On the other hand, chip level performances (such as output power, receiver conversion gain, receiver linearity, noise figure and so on) would be determined in accordance with these requirements. They could be derived using theories of minimum detectable signal and radar range equations.

The radar range, R_{max}, is defined as the maximum distance at which the radar can allocate the existing targets. It primarily depends on chip-level parameters such as transmitted signal strength, antenna gain, receiver channel noise figure and signal-to-noise ratio (SNR), which generally contradicts for the operation in high frequencies where system noise greatly increases while transmitted output power is limited due to the fabrication technology at such high frequencies. Maximum unambiguous range of a radar become $R_{max} = f_S \cdot c \cdot T_M/(4BW)$ where f_b is limited by the ADC sampling frequency, f_S, in a way that Nyquist criteria ($2f_b \leq f_S$) must be fulfilled as in a generic real ADC implementation (not complex quadrature). The maximum resolvable velocity is bounded up to quarter wavelength of phase change in between the consecutive chirps and could be determined by $v_{max} = \lambda/(4T_M)$. This means that shorter chirps increases maximum measurable velocity whereas decreases maximum measurable range.

Another important metric of a radar is its range resolution, ΔR, which measures how well the two targets in close proximity could be distinguished by the radar, such that targets staying within this ΔR would be completely resolved in distance. Range bins are determined in this way at the same time where the maximum and minimum detectable ranges are divided into M range bins with ΔR steps. From the notation, it is obvious that operation bandwidth, BW, should be increased in order to achieve higher resolution. That explains why ISM bands at higher frequencies are preferable for such applications such as 60-GHz ISM band with 9-GHz bandwidth, 122-GHz ISM band 1-GHz bandwidth or the automotive frequency band around 80-GHz. Range resolution could be derived from the above range equation depending on the beat frequency. Assuming the change in beat frequency, Δf_b, is limited by the modulation frequency $1/T_M$, then the minimum resolvable

range becomes $\Delta R = c/(2BW)$ to assign two targets to different range bins. The range resolution has also a factor in the range $[1 < a < 2]$ representing the degradation due to system errors and signal processing techniques like windowing operation [79].

Similar approach could be applied to velocity resolution, Δv, where this time frequency resolution limits the Doppler frequency change within n number of ramps in the frame, hence $\Delta v = \lambda/(2nT_M)$. For instance keeping the total active frame time constant ($T_F = nT_M$, idle frame time is not considered) and increasing the chirp modulation time would result in decreased v_{max} and improved R_{max} while achieving the same Δv and ΔR.

While a single-channel radar could resolve the targets within certain range, multiple channels might be required to increase the resolution of multiple targets at the same distance to transceiver, but distinct in lateral distance. This notion of angular resolution could be realized with the same radar with limited target detection capabilities. This parameter is extracted using the target range and the 3-dB beamwidth of antenna such that side lobes have comparably low power. Higher frequencies benefit better angular resolution for the same antenna form factor, because of the increased directivity. However the radar field-of-view degrades greatly due to sharper and focused beams. Therefore phased array and MIMO radar solutions, possessing multiple channels and multiple antenna beams, are offered to achieve the angular information. The angular resolution could be mathematically represented as $\Delta\theta = \lambda/(Kdcos(\theta))$ where K is the length of array and d is the spacing between consecutive antenna elements and θ is the angle of arrival. This term could be simplified as $\Delta\theta = 2/K$ since often the calculations are realized using $d = \lambda/2$ and $\theta = 0°$.

The accuracy, on the other hand, changes as well depending on the target distance, which tends to decrease for increasing distance, while increases as the operation frequency range goes higher. The RMS accuracy depends greatly on the SNR and could be formulated as $\sigma_R = c/(2 \cdot BW \cdot \sqrt{2 \cdot SNR})$ for the range accuracy, whereas $\sigma_v = \lambda/(2 \cdot n \cdot T_M \cdot \sqrt{2 \cdot SNR})$ for the velocity accuracy, which compose a small fraction of the range and velocity resolutions that are degrading with the SNR performance of system [80]. With the inclusion of other system level parameters, the accuracy would decrease and these resulting expressions should include dedicated coefficients signifying the degradation.

In addition to these, detection probability and false-alarm-rate (FAR) of a radar are the two other important metrics. While the prior corresponds to detection in the presence of a real target, the latter is related to a target declaration in the absence of a real target. These issues might be alleviated because of system noise, clutter or other interferences in a way that the previously set detection threshold level is exceeded. To be able to detect the target clearly in spectrum, its level should be above the noise floor by certain amount, which is called SNR. But SNR requirement could not be made too low since it would trigger increased FAR, or made too high which allows lower detection probabilities of real targets either being too far or having less power. System level algorithms should be implemented to prevent these, whereas the noise contribution of the designed transceiver should be minimized as possible.

2.3 Link Budget Calculation and Specification Extraction

Before designing the transceiver chip, system level parameters have to be determined since the block-level requirements would be defined accordingly. Regarding the modulation characteristics of 122-GHz version, the TRx operation bandwidth extends approximately from 119 – 126 GHz with a 7 GHz bandwidth, which automatically translates into a theoretical range resolution of 2.14 cm. Even though the ramp sweep time could be adjusted, it is accepted as 1 ms covering the full 7 GHz bandwidth, hence the sweep rate is found as 7 MHz/µs. Using an ADC with a sampling rate of 10 MSa/s gives a maximum detectable beat frequency of 5 MHz at the limit considering the Nyquist theorem and then maximum detectable range becomes 107.14 m using the above radar equations. In order to increase the maximum detection range, either an ADC with higher sampling frequency could be employed or chirp modulation time could be increased leading to slower measurement times. So per meter change corresponds to a beat frequency of 46.55 kHz/m. Maximum time delay of the reflected signal coming from the target located at this distance is then calculated as 714.3 ns. Maximum unambiguous velocity that the radar could detect is ± 0.615 m/s with a resolution of 0.077 m/s by keeping the total number of ramps as 16. Increasing number of ramps would result in better velocity resolution at the expense of boosted integration time. Similar metrics could be calculated for 60-GHz with the expected bandwidth of around 9 GHz which increases the range resolution at the first glance.

The minimum detectable signal (MDS) by the Rx channel is determined by the noise power, $S_n = kTBWF$, and the required SNR level. Here the BW specifies the system bandwidth which is generally limited by the ADC sampling rate (f_S), F specifies the receiver noise factor, k is the Boltzmann constant and T is the temperature. Therefore MDS is found to be $MDS = 10\log(S_n) + SNR$. Considering the total frame time of 16 ms (nT_M), system bandwidth becomes limited to 62.5 Hz. Thus the system noise floor would be measured as -156 dBm. Employing less number of chirps would be beneficial in terms of faster operation since the total measurement time is reduced, but at the expense of increased noise floor as well as the degraded velocity resolution. Since many transceiver chips at 60- and 122-GHz are designed and the circuit blocks do not change, common values to be reached in all transceivers are considered. Therefore the 122-GHz monostatic versions which will be discussed later in this chapter is taken as a basis of calculation due to having the highest noise figure and lowest transmitted power after integration of front isolation coupler. With the addition of 12 dB of receiver noise figure and the required 10 dB SNR to be able to identify the targets clearly, MDS specifying the receiver sensitivity rises to -134 dBm which is actually not quite hard to satisfy even with basic circuit implementations. In order to calculate the expected received power, Friis radar equation should be referred, which is expressed as below:

$$P_{RX} = \frac{P_{TX} G_{TX} G_{RX} \sigma \lambda^2}{(4\pi)^3 R^4 L_S} \tag{2.8}$$

The equation relates the received signal power, P_{RX}, to transmitted power, P_{TX}, antenna gains, G_{TX} and G_{RX}, operation wavelength, λ, radar cross section (RCS) of the detected target, σ, target distance, R, and a combined system loss of L_S. Considering a low transmitted power of 3 dBm, the antenna gain has to be boosted to compensate for the free space path loss which is around -114.77 dB at the specified maximum radar range of 107.14 m. Therefore the antenna gain should be selected around 22 dBi (including on-PCB antenna and Lens) so that the received power could reach -67.77 dBm excluding the target radar cross section (RCS) and system losses (L_s). The effect of these is not quite trivial since the RCS could easily change between -20 dBsm to 20 dBsm for different targets (100 m^2 for automobile and $1m^2$ for man) and system losses could emerge from quite a broad range of sources, each causing couple dB reduction, and in total could rise up to more than 20 dB. However even with 40 dB of total additional loss, such received power level is almost enough to produce a clear signal above the specified receiver sensitivity at the IF output spectrum taking the SNR level of 10 dB into account. Beyond this point, the receiver gain could be boosted with the help of LNA, down-converter mixer and IF amplifier gains, while the total system noise temperature is already set by the LNA.

Because the structure is of monostatic type where the system shares a single antenna for signal transmission and reception, the integrated coupler introduces a greater coupling compared to the classical bistatic radars with two separate antennas for each operation. This might result in transmitter leakage, thus requiring an input referred receiver linearity of certain level. Assuming the transmitter output power before the coupler as 9 dBm and the isolation between output ports of coupler as 27 dB would lead to a linearity specification of -18 dBm in order not to saturate the receiver channel. With a neat coupler design targeting around 35 dB isolation, the receiver linearity requirement could be relaxed. The required transmitted power could be generated through a non-demanding VCO having an output power around 4 dBm. Such power would be divided into two to feed the receiver and transmitter channels with a reduction by 4 dB. Therefore the mixers have enough LO power to switch the transistor pairs on. As mentioned, monostatic architecture is the most demanding one, thus other multi-channel configurations have more flexibility in these requirements.

2.4 Transceiver Architectures

The transceiver architectures designed within the scope of this thesis are composed of single- and multi-channel configurations at 60- and 122-GHz ISM bands. The multi-channel TRx include double-receive channel TRx of 2 Rx and 1 Tx (namely TR2) and MIMO TRx of 4 Rx and 4 Tx. On the other hand, the single-channel is of monostatic type (namely TRM) with on-PCB and on-chip integrated antenna solutions. The TR2 is measured with only one Rx channel active, therefore could be considered as a single-channel bistatic radar IC as well. Although heterodyne architectures

offer many advantages like improved isolation, homodyne receiver architecture is selected because of its simple implementation requiring less number of sub-blocks and a single-stage IF down-conversion. In the following sections, the fabricated TRx structures are detailed, and to avoid repetitiveness, just the 60-GHz versions are pictured even the 122-GHz version are identical.

2.4.1 Single-Channel Monostatic Transceiver

The classical bistatic approach shows its strength in its simple implementation, which two distinct antennas are placed for Tx and Rx channels and the outputs of these are directly connected to antennas. They might introduce some issues such as the inevitable coupling between Tx and Rx antennas. The leakage from Tx channel could easily cause saturation of the Rx if not designed carefully. However this puts itself as a generic issue in any radar architecture where simultaneous Tx and Rx operation take place. Nevertheless the classical approach still offers nice metrics when combined with a high performance chip. Yet the absence of a single focal point of this architecture could also limit the maximum achievable range and resolution, since at some distance, the antenna parameters and its frequency dependent matching network would aggravate beam squint issue and reduce the overall bandwidth. Depending on the target cross section affecting the reflection plane and the angle of arrival to Rx, this situation could result in a reduction in the maximum radar range further.

In order to overcome such issues, the monostatic approach, in which the Tx and Rx channels are combined (i.e. with a passive power combiner) to operate on the same antenna, could be brought forward. By this way, not only the single focal point is promoted, but also the coupling through the antenna section is eliminated. In the context of final system, by proper antenna center aligning according to the lens center, a higher directivity becomes also possible in terms of focal point matching. However it adversely affects the system owing to the introduced direct leakage path from Tx to Rx. In case of a design error either due to the fabrication process variations or faulty electromagnetic modeling, the channel isolation might be much worse and degrade the radar performance. Additionally, the integration of a power combining structure at the very front inserts an additional noise element on the Rx side and results in a reduced conversion gain at the same time. On the Tx section, the transmitted output power is reduced by the amount of insertion loss of this power combiner, which has a direct impact on the maximum radar range. But it possesses the advantage of allowing a flexible antenna design, where it is possible to either shrink the chip and package size (especially if the antennas are integrated on chip) and lower the fabrication costs as well, or to attain higher antenna gain by integrating a larger antenna on the same amount of area. Furthermore the antenna radiation pattern could be adjusted more easily depending on the application requirements. That is why the monostatic architecture is chosen for the single-channel transceiver.

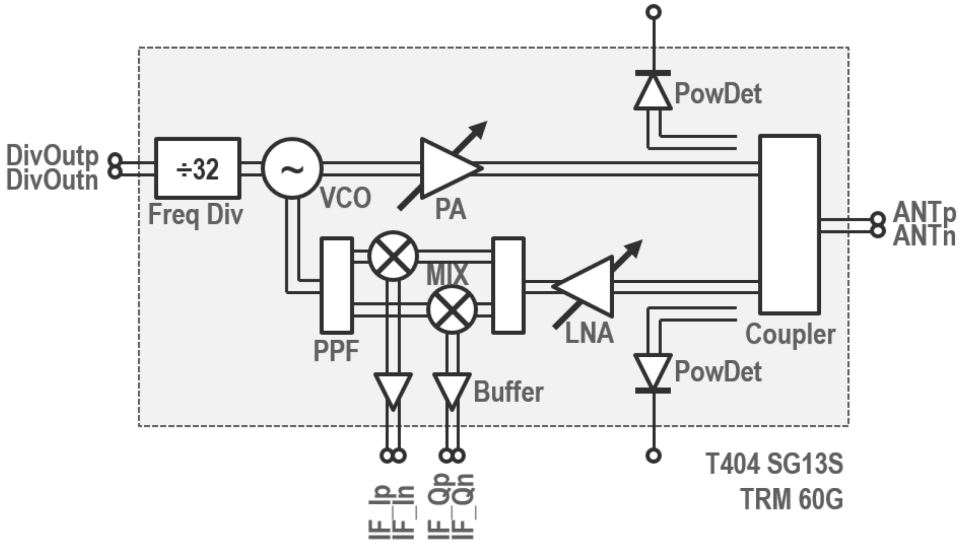

Figure 2.3: Block diagram of the single-channel monostatic 60-GHz TRx.

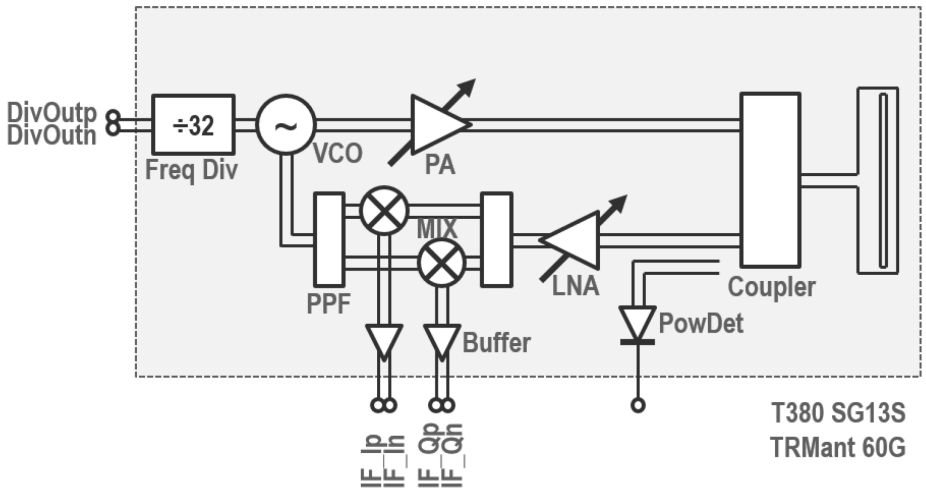

Figure 2.4: Block diagram of the single-channel monostatic 60-GHz TRx with integrated dipole antenna.

Figure 2.3 shows the block diagram of fabricated 60-GHz TRM IC whereas the other multi-channel versions are derived from this single-channel structure [16], [18]. The Tx channel is composed of a power amplifier to boost the transmitted power, power detectors to monitor the transmitted and reflected powers, and finally a push-push type VCO with 30-GHz fundamental frequency and 3-bit frequency tuning capability which is integrated to a frequency divider with a division ratio of 32 for external PLL operations. On the other hand, a direct-conversion receiver is designed on the Rx side, which incorporates a low-noise amplifier, a power divider, an I/Q signal generator to produce in-phase and quadrature LO signals, and two I/Q mixers with buffer circuits.

Then the differential I/Q IF outputs are directly processed outside on board by passing through low-pass filters, amplifiers and ADCs respectively. All the circuit blocks are designed differentially. Since the structure is of monostatic type and requires single antenna input for Rx and Tx channels, a coupler is designed for the input section which guarantees a high isolation between channels to prevent leakage. Furthermore the antenna including a wirebond compensation network is designed on a high-frequency substrate on which the fabricated TRx is wire bonded.

In order to evaluate different packaging options, versions with integrated dipole antennas for both 60- and 122-GHz are fabricated at the same time and are shown in Figure 2.4. The antennas are optimized to radiate backside through the silicon substrate and benefit from silicon lens stacked directly to the chip to focus the main antenna beam on a single side. Many antenna configurations exist in the literature, yet the occupied silicon area is quite effective in the selected antenna topology. The details of antenna and lens design is further mentioned in Section 5.2.

2.4.2 Double-Receive-Channel Transceiver

Besides of these single-channel TRxs, a double-receive-channel (TR2) version is designed so that the target directions could be tracked up to some point with the help of different angle of arrival information and the resultant delays on each Rx antenna [17]. This simple configuration provides a poor angular resolution due to provided number of Rx channels, yet it already supports couple industrial applications.

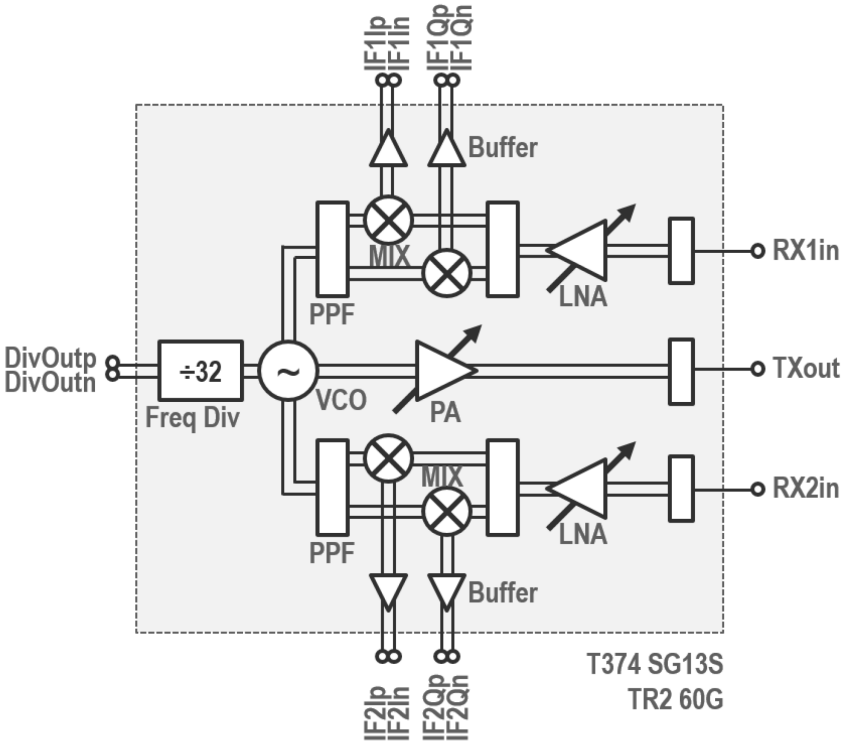

Figure 2.5: Block diagram of the double-receive-channel 60-GHz TRx.

In Figure 2.5, the block diagram of fabricated 60 GHz TR2 chip is highlighted. Although the main circuit blocks are same except individual performance improvements, main optimizations are carried on the VCO power division section to feed the down-converters and power amplifier. The two-way power divider is replaced with the three-way version to support three channels in total. Since the insertion loss of this block is higher, the receiver linearity and transmitter output power measures are optimized. Isolation between channels are further improved with the integrated via wall between each channel. In the end, an evaluation board including on-board high-frequency baluns converting the differential outputs with low phase and amplitude imbalance are designed to fully characterize the wirebonded chip. However the radar range measurements are realized using just one of the Rx channels due to measurement capabilities.

2.4.3 MIMO Transceiver

The TR2 topology helps figuring out the object positions to some extent due to the limited angular resolution gathered from just two antennas. In case of higher resolution requirement, the system should be developed to include more radiating elements which translates into a need for highly integrated MIMO TRx IC composed of multiple Tx and multiple Rx channels, or even a massive MIMO system formed by chaining these individual MIMO TRxs. Then the main challenge lies on the radar signal processing section together with transmitter multiplexing rather than the circuit design. Even though the chip and package area and the power consumption increases drastically – so does the overall costs, the applications requiring high angular resolution and wide coverage still has to adopt such topology.

Another solution to this requirement would be the classical phased-array radars where the individual antenna elements are followed by phase shifters to steer the resulting beam in an analogue way to achieve area coverage with certain resolution (even a higher resolution is possible with the use of gain-varying active phase shifters and increase in the number of channels) [81] – [83]. The phased-array version also provides much higher gain thanks to combined antenna operation, leading to improved detection while knowing the fact that the area coverage is only bounded to 120°. In order to achieve clear beam shifts without much distortion in the main beam due to rising side lobe levels, the number of required elements increases greatly which narrows down the beam. Yet for certain system specifications that could be achieved with phased-array cannot be compared to what MIMO could provide considering the number of radiating elements required. Because in contrast to phased-array topology where the resolution is determined with the number of physical channels integrated in the system, the MIMO topology aims to create a kind of virtual channel series whose length equals to the multiplication of Tx and Rx channel numbers, hence allowing for a better resolution for the same number of channels. The flexibility of choosing the individual beam patterns and waveforms for each Tx channel is another advantageous point of MIMO systems as well. In this case since the antennas are apart by certain distance, each subsequent Rx

channel would receive the reflected signal with certain delay which creates phase shifts. By sampling these signals across all channels and applying FFT, phase shifts could be computed. Number of channels should be increased to be able to detect the targets with higher resolution since it is possible that the targets cannot be differentiated in case of lower number of antennas. However higher number of channels comes with its benefits at the expense of increased baseband complexity since each Rx channel should be processed separately, in the end requiring multiple ADCs and FFT operations.

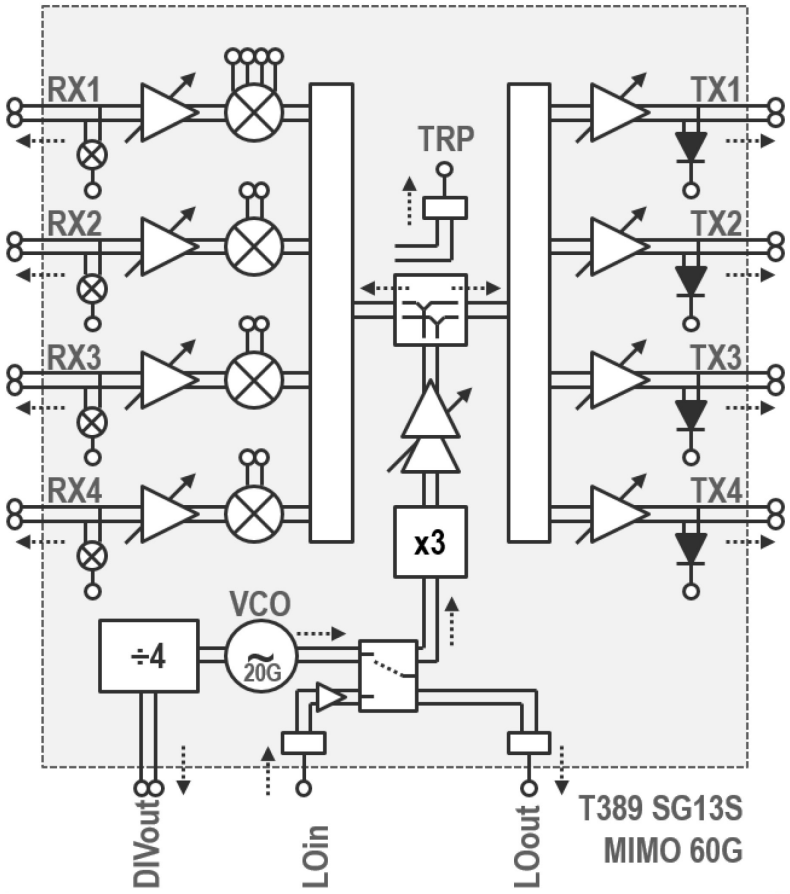

Figure 2.6: Block diagram of the 60-GHz MIMO TRx with 4-Tx and 4-Rx channels [19].

In Figure 2.6, the block diagram of fabricated 60-GHz MIMO IC which is of four switchable Tx and Rx channels is illustrated [19]. Using the same blocks from previous TRxs, but optimized for this application, would result in a MIMO array of 16 virtual channels at the end. This would mean an angular resolution measure of 7.5°. Three of the Rx channels gives a single IF output whereas one of them is designed to provide an I/Q IF output. BIST circuitries as power detectors and up-converters are located right before the Tx and Rx pads respectively, which each of these calibration blocks could be switched off during the main radar operation. At the end, these channels are connected by 1-to-4 and 1-to-2 passive power combiners consecutively to be fed by the main LO signal.

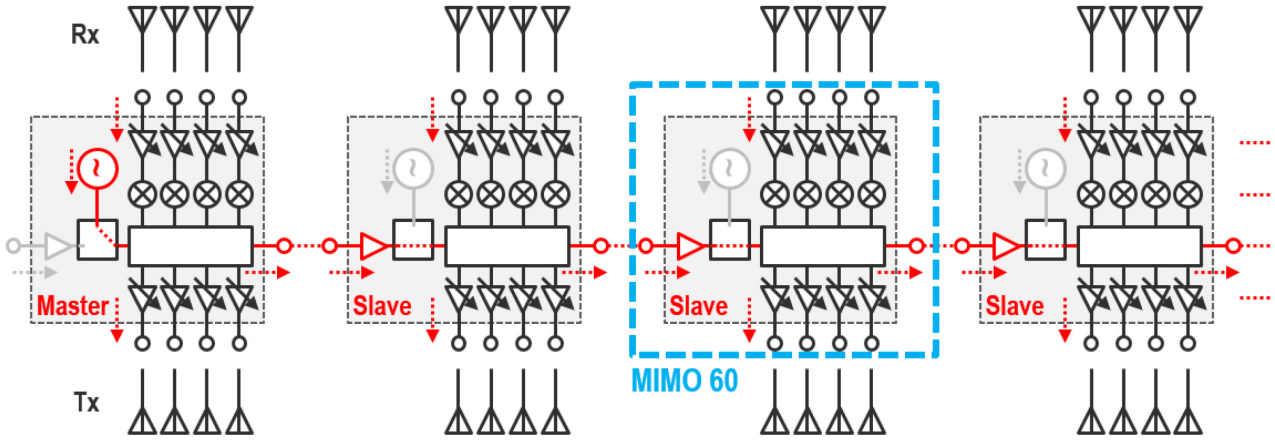

Figure 2.7: Block diagram of the massive MIMO chain composed of multiple scalable MIMO TRxs [19].

On the other hand, the LO signal could be generated by either an internal or an external VCO (by *LOin* pin) which is controlled by an integrated multiplexer whose additional output is directed outside (from *LOout* pin). This type of VCO configuration would enable massive MIMO systems through chaining of these single MIMO ICs (see Figure 2.7) by defining one as the '*master*' in which the internal VCO is operational and the others as the '*slave*' in which the internal VCOs are disabled and *LOin* pins are receiving the LO signal, thus synchronization of multiple ICs is satisfied. Since the routing of 60-GHz signal on board would be challenging, the fundamental frequency is decided to be kept at 20-GHz, and then internally multiplied by the frequency tripler to achieve the FMCW operation at 60-GHz. This means, the fundamental frequency of internal VCO is 20 GHz as well. At the *LOin* input, a 20-GHz power amplifier is designed to guarantee high enough output power entering in the multiplexer. The frequency tripler output could also be observed from the control pad directly coupled at the output of 1-to-2 power divider. In order to compensate for the losses emanating from the 1-to-4 bulky power combiners, additional amplifiers are attached to tripler. The VCO with three analogue frequency tuning inputs is also coupled to a divide-by-4 frequency divider for external PLL operations around 5-GHz. Finally the differential antenna design is again conducted on high frequency substrate including wire bond compensation networks. Couple packaging solutions are offered as well.

3 Design and Implementation of Radar Transceivers

In this chapter, the design methodology, implementation and simulation results of transceiver circuits to be utilized in FMCW radars functioning within the allocated ISM bands are highlighted. The fabricated transceivers in the context of this thesis include 60- and 122-GHz versions built using single-channel monostatic with and without on-chip antenna, double-receive-channel and multi-channel architectures. Since the 122-GHz version shares almost the same system topology and design methodology as its 60-GHz counterpart (with minor modifications in individual blocks to achieve better performance parameters and matching networks in terms of updating the operation frequency), only the design steps belonging to 60-GHz chips are highlighted throughout the thesis. Nevertheless the simulation and measurement results of both frequency versions are presented. An overview of what is available and achievable in selected fabrication process is discussed as well. This includes the technology layer stack-up, passive components and transistor specifications such as maximum operation frequency, gain, noise figure and so on, which all are quite crucial to achieve the targeted link budget. In the following chapters, the system level measurements of these chips with different antenna configurations are explained and different packaging solutions with a great emphasis on interconnects are proposed.

3.1 Fabrication Technology Overview

The designs are fabricated using 0.13 µm SiGe BiCMOS process with 250 GHz of f_t (transit frequency) and 340 GHz of f_{max} (maximum oscillation frequency) [84]. As shown in Figure 3.1, the technology includes 7 metal layers with top 2 being thick Aluminum layers (with 2 µm *TopMetal1* and 3 µm *TopMetal2*), which are quite suitable to create inductors with high quality factor (more than $Q > 15$) and high current density, and a very thin metal layer designated just for process-specific MIM (Metal-Insulator-Metal) capacitors. This MIM layer gives a capacitance density value of 1.5 fF/µm². The foundry additionally provides polysilicon resistors and variable capacitors that is especially good for VCO design. The dielectric used in back-end-of-line is Silicon Dioxide (SiO_2) with relative dielectric permittivity (ε_r) of 4.1, which is built on a Silicon (Si) substrate with 50 Ωcm resistivity with ε_r of 11.9. The silicon backside could be etched using a special technology

called Local-Backside-Etching in order to create passive structures with high quality factor and on-chip antennas with high efficiency. For the chips including integrated antennas or the ones where wirebond interconnect lengths play crucial role in overall performance, substrate thickness is selected accordingly and simulated carefully.

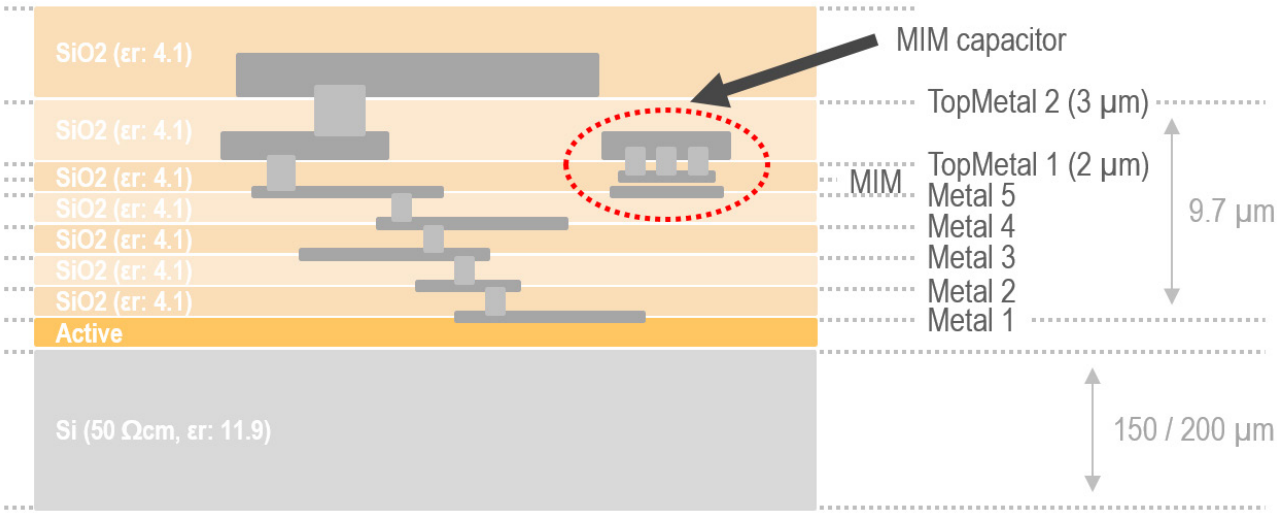

Figure 3.1: Cross section of the 7-layer SiGe BiCMOS technology.

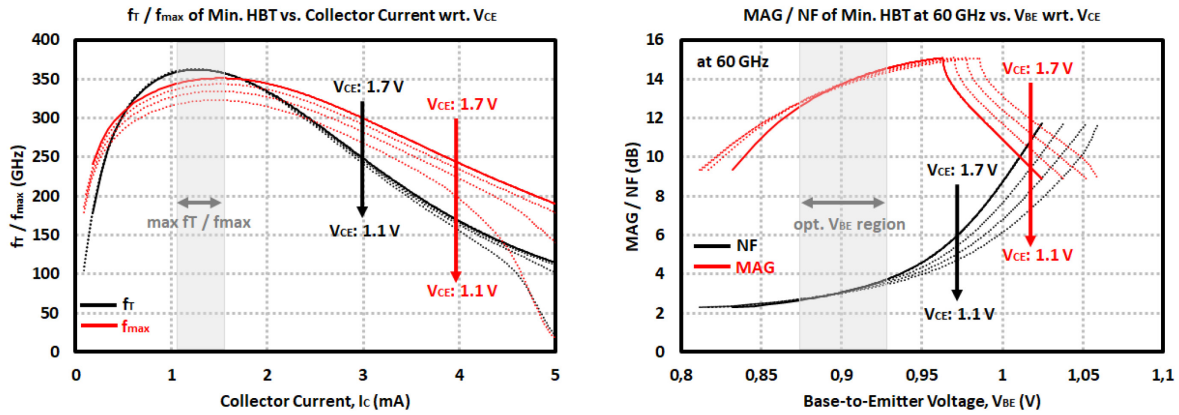

Figure 3.2: (*Left*) Minimum-length HBT transistor fT / fmax and (*right*) corresponding maximum available gain and noise figure with respect to base-to-emitter voltage at 60-GHz.

The technology also offers NPN transistors with current gain (β) of around 900 and BV_{CEO} (collector-emitter breakdown voltage) of 1.7 V. The transit frequency (f_T) and maximum oscillation frequency (f_{max}) are affected by how the transistors are biased. From Figure 3.2, the simulated f_T and f_{max} of the minimal HBT device (0.12 x 0.48 µm^2) are shown which exceeds 300 GHz for a collector current of around 1.5 mA biased at BV_{CEO}. Biasing around 900 mV allows device to operate with optimal maximum available gain (MAG) and minimum noise figure (NF_{min}) at 60-GHz where the simulations point out a MAG of 12.5 dB with NF_{min} of 3 dB. Not shown in the

figure, using the device at 122-GHz would provide MAG and NF_{min} of 7.3 dB and 5.3 dB respectively. By dragging the V_{BE} bias point to around 850 mV, NF_{min} could be decreased to 4.3 dB at the expense of reduced MAG of 6.2 dB, which is to be decided in the design process.

3.2 General-Use Circuits Design

All of the circuit blocks include some small structures which are quite important in the realization of reliable circuits. These include ESD diodes and clamp circuits, bias networks to control the current drain by each circuit and the CMOS inverter block. In order to avoid repetitiveness within the next sections, these circuit block are shared under this section.

3.2.1 ESD Protection Structures

During the board assembly and chip handling process, if not protected properly – the introduced electrostatic discharge (ESD) might damage the chip itself so that the manufacturing yield would drop drastically [85] – [87]. In order to prevent such cases, the internal circuitry should withstand excessive discharging emanating from different sources, such that they should include dedicated ESD protection structures right at the input pads. In order to test the ICs for ESD failures, various pre-defined models are considered such as human-body, machine and charged-device models measuring the ESD issues that might be caused by human handling and assembly process. Only the ICs satisfying some industrial standards defined for each of these models could be employed as a final product.

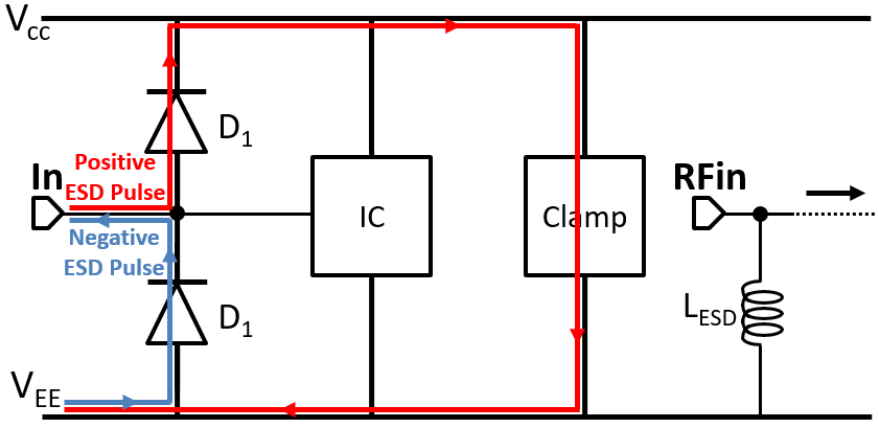

Figure 3.3: Concept of ESD protection at low- and high-frequency pads.

The ESD protection units are composed of two distinct circuitries designed for the main supply voltage pin and the control pins (i.e. gain, enable / disable) together with the relatively low frequency outputs (i.e. IF and frequency divider outputs) whose overall performances are not affected

by the integration of these units. Such circuit is composed of back to back diodes where the pad is fed in the middle of these two diodes and the other ends are connected to main supply and ground pins (see Figure 3.3). The foundry provided ESD structures are able to withstand up to 4 kV attacks which corresponds to Class-2 in industrial standards.

As critical as these pins, the high frequency inputs should be protected against ESD strikes. Since the introduced ESD units degrade the RF performance, they are realized in the form of shunt inductors connected to ground. The width and thickness of these inductors are selected to increase the current handling capability of the metal structure and withstand the high current drain, while the length determining the inductance value is important for proper RF matching. Such inductors are detailed in the following sections.

3.2.2 Bias Circuit Design

In Figure 3.4 a general current mirror circuit biasing almost all of the internal blocks is shown. Although there are minor differences for some bias circuits, the general architecture and operating principles are similar. The gain and enable pins are integrated through pMOS transistors attached to resistors to adjust the bias current. Each control pad is accompanied by a pull-down resistor such that all pMOS transistors would be turned on and the bias current would be maximized due to minimized collector load (R_5 // R_6 // R_7) when nothing applied to these pads.

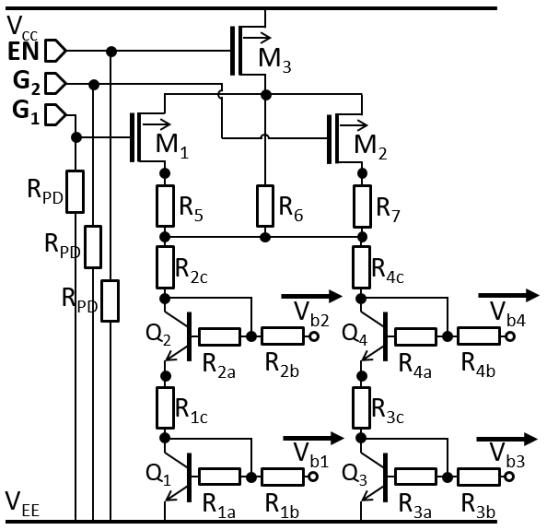

Figure 3.4: Schematic of a general use bias circuit based on current mirror topology.

3.2.3 CMOS Inverter

The CMOS inverter circuit together with its simulation result shown in Figure 3.5 is utilized generally in the gain / enable pins in all the TRxs providing various control options to internal blocks such as gain / output power setting and enabling / disabling channels for reducing power consumption and for software implementation of required application. In some of the circuits, low voltage transistor models are used that necessitates a lower gate voltage of about 1.3 V so that the inverters include simple resistive voltage dividers (2 kΩ / (2 kΩ + 3 kΩ)) as highlighted on the same figure. Finally input sections are connected to ground or supply via pull-down or pull-up resistors of 100 kΩ in order to set a default operation mode in case of an open-node which consumes negligible current.

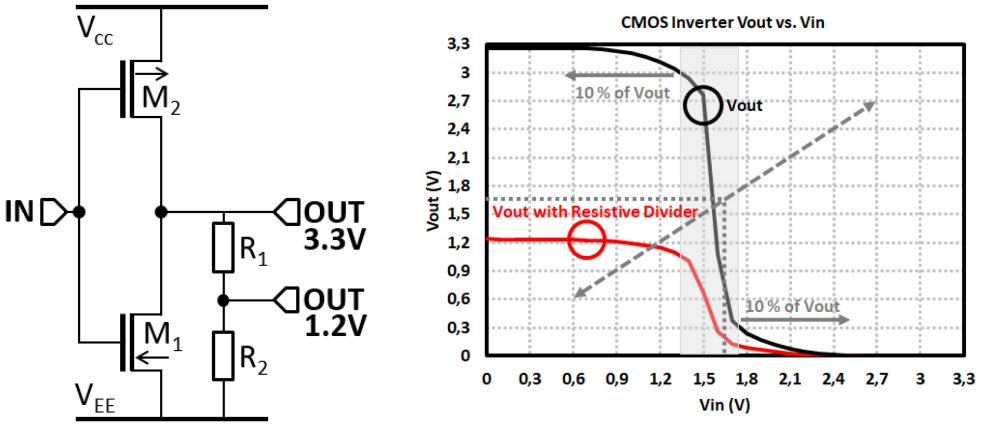

Figure 3.5: Schematic and simulation results of a CMOS inverter.

3.3 Receiver Channel Design

In both the 60- and 120-GHz versions, the quadrature Rx channels are employed, which comprises of an LNA, a Wilkinson power divider, two Gilbert-cell based mixers, an I/Q signal generator and IF buffers adjacent to the mixers. Each of these internal blocks are designed differentially and as symmetrical as possible to preserve the differential signal characteristics. The differential nature of circuits provides robustness against wirebonds, suppresses the even-order harmonics and eliminates the common mode noise. In order not to degrade the noise figure and gain performance of the Rx channel, balun circuits are not integrated at the inputs of 60-GHz TRxs since the antenna and package concepts still could be well realized without much of an issue whereas this is more critical in the TRxs at 122-GHz band where interconnects play a crucial role in the overall system performance. Therefore 122-GHz Rx channels benefit the balun so that the inputs are single-ended terminated and matched to 50 Ω impedance.

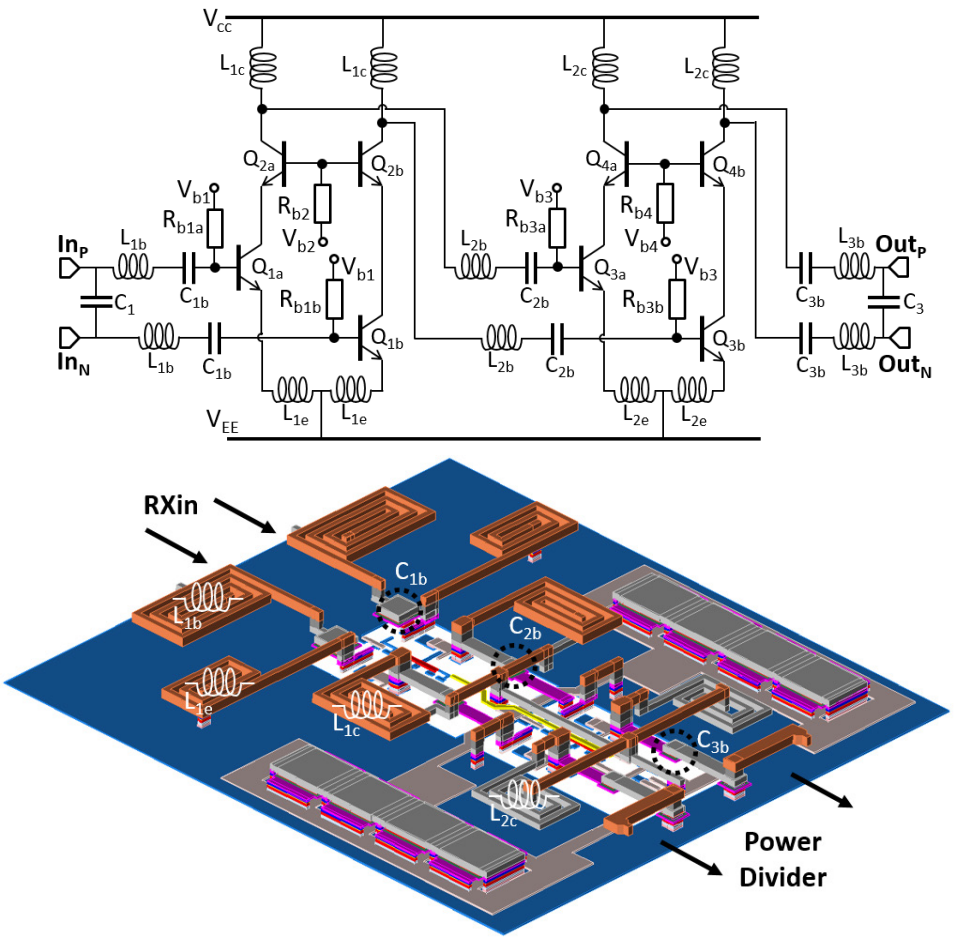

Figure 3.6: Schematic and layout of 60 GHz differential two-stage cascode LNA circuit.

As shown in Figure 3.6, the two-stage cascode topology is chosen for the LNA design which could deliver a high gain and a low noise figure. The circuit is biased through differently optimized current mirrors for each stage such that lower noise figure with a moderate gain is extracted from the first stage whereas the second stage is biased in a way to obtain higher gain while maintaining adequate linearity as well. Simple LC type transmission networks guarantee the input, inter-stage and output impedance matchings for maximum power transfer and optimum noise performance. In this respect, the initial simulations are realized with the lumped inductor and capacitor models together with the foundry provided HBT transistors. Then these inductors, together with the transistor connections through vias, are simultaneously simulated to take the coupling effect and interconnect parasitic into account for accurate modelling. The inductive loads (L_{1c}, L_{2c}) improve the bandwidth and high frequency gain while the degeneration section (L_{1e}, L_{2e}) provides a series-feedback and proper matching by controlling the real part of input impedance to compensate for the transistor parasitic capacitor (intrinsic base-to-emitter capacitance, C_{be} in combination with the reduced collector-to-base Miller capacitance, C_{cb}) and improves the stability at the expense of reduced gain. Such cascode topology is also useful in increasing the isolation. In order to eliminate the effect of substrate parasitic, the bottommost metal layer is utilized as a ground shield. Instead

of bulky microstrip transmission lines, inductors with moderate Q-factors, due to the ground shield beneath, are designed and bended as spirals to reduce the block size as much as possible, which the LNA fits only in 200 µm x 200 µm area at the end as could be viewed in Figure 3.6.

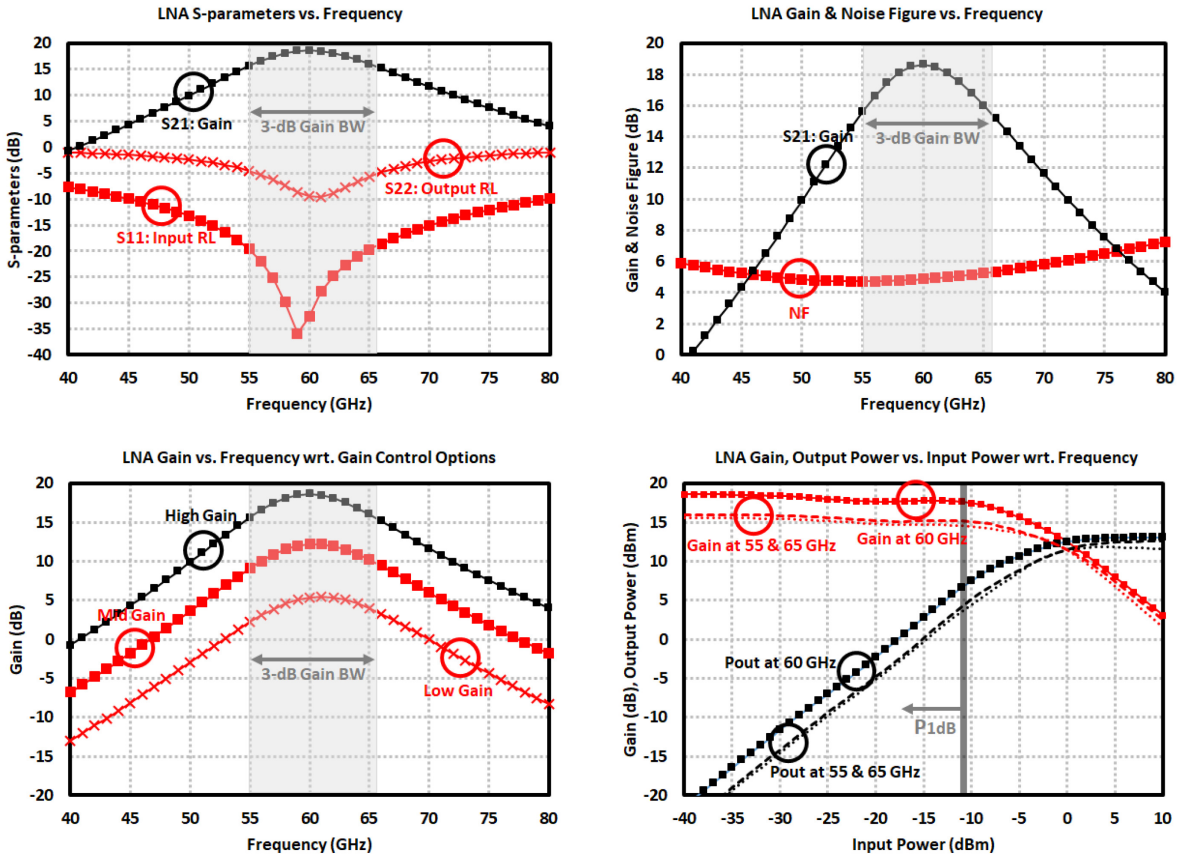

Figure 3.7: Simulation results of 60 GHz LNA: (*top left*) S-parameters, (*top right*) gain and noise figure, (*bottom left*) gain with respect to control options, (*bottom right*) gain and output power with respect to frequency.

To prevent any transmission line breakdown, the thickest topmost aluminum metal layer is employed allowing for higher current densities and on the lower thin metal layers where the conductivity is lower, the line widths together with via sizes are adjusted accordingly especially at the HBT inputs. Various control options are implemented basically to be able to have a control on the block gain and linearity by steering the currents drawn in bias circuitry. Finally the circuit stability is proven during the simulation phase with full electro-magnetic models.

According to the simulation results depicted in Figure 3.7, the LNA could achieve 18.6 dB of gain with 4.9 dB of noise figure at 60 GHz and a 3-dB bandwidth of 10.5 GHz between 55 – 65.5 GHz. Input is properly matched to differential 100 Ω while the output matching is brought to a point which could be easily matched to the latter power divider stage. The IP_{1dB} is simulated as -11 dBm and the corresponding output power is found as 6.6 dBm around 60 GHz. The total power consumption of this block is 25.8 mW when supplied at 3.3 V with maximum gain mode enabled.

Lower gain modes are introduced through the biasing scheme which result in about 5 dB of successive gain drop in the block with a minimum of 8.6 dB. Not shown in the figures, the LNA could be completely switched off through the enable-pin for applications using multi-channel operation. Finally a maximum of 2.5 dB gain reduction is observed for operation at 125 °C temperature.

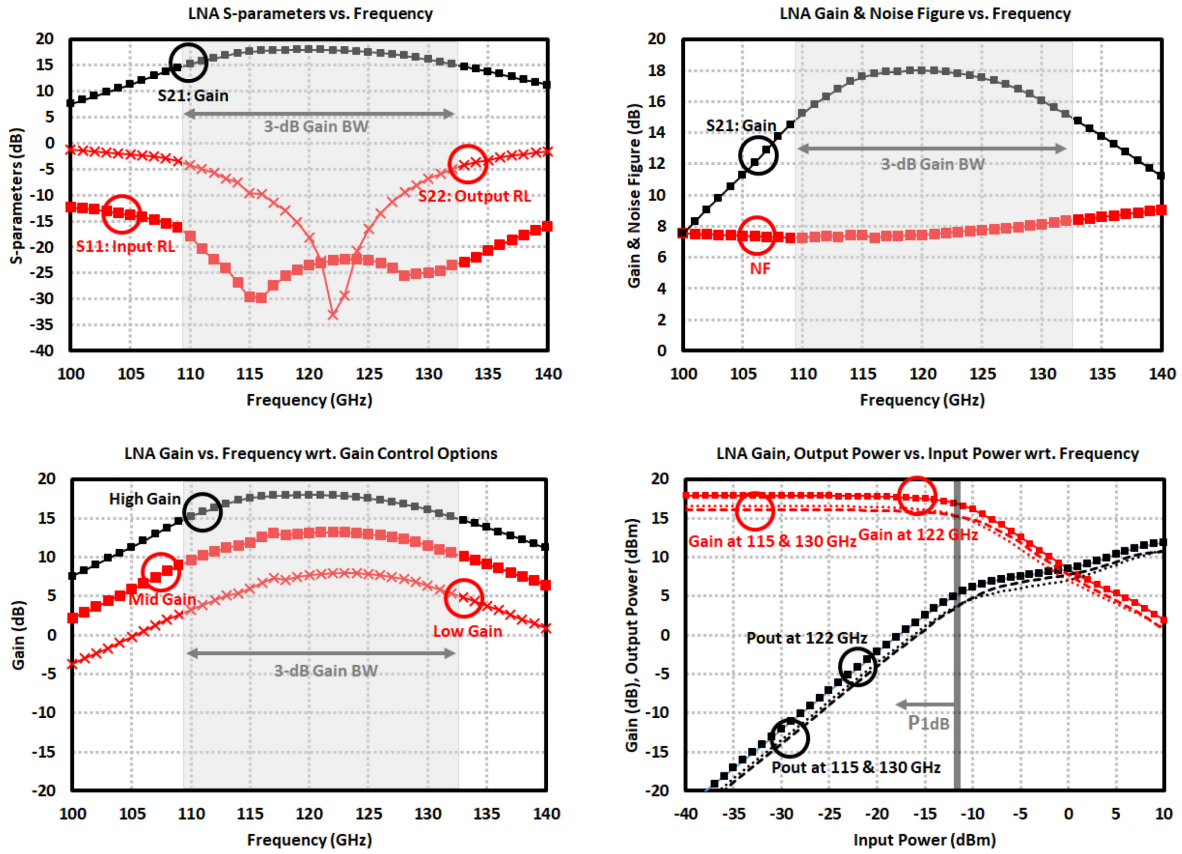

Figure 3.8: Simulation results of 122 GHz LNA: (*top left*) S-parameters, (*top right*) gain and noise figure, (*bottom left*) gain with respect to control options, (*bottom right*) gain and output power with respect to frequency.

On the other hand, as shown in Figure 3.8, its 122-GHz counterpart shows gain and noise figure performances about 18 dB and 7.4 dB respectively. The 3-dB bandwidth is 23 GHz between 109.5 – 132.5 GHz with a simulated IP_{1dB} of -12 dBm resulting in OP_{1dB} of 5 dBm. It consumes 24.4 mA of current from 3.3 V. With the help of control options, the gain and current consumption could be reduced to 8 dB and 9.6 mA.

Quadrature down-conversion is preferred for Rx channel thanks to its significant features such as image cancellation, allowing to acquire phase information and gain boosting out of the two IF channel operation, hence SNR improvement. For that purpose, the differential LNA should be directed to quadrature mixers, requiring differential power divider on the RF side and I/Q signal generator on the LO side.

The classical Wilkinson power dividers incorporate transmission lines having 70.71 Ω characteristic impedance with length of quarter-wavelength on the power dividing section that is terminated

with 100 Ω resistance regarding to generic even- and odd-mode analysis. Since the long transmission lines would eliminate the compactness, the RF signal after LNA is divided by passing through an LC-type Wilkinson power divider (see Figure 3.9). Compared to the structures adopting transmission line, the operation bandwidth could be much narrower. However this is not the case for a design targeting such limited ISM bandwidths. The important metrics to be reached in this block is the output phase and gain imbalances within the frequency band of interest as well as its average insertion loss, return losses and output port isolation to guarantee an equal power split. The equally divided LNA signals after this passive component is fed into the transconductance pairs of mixers.

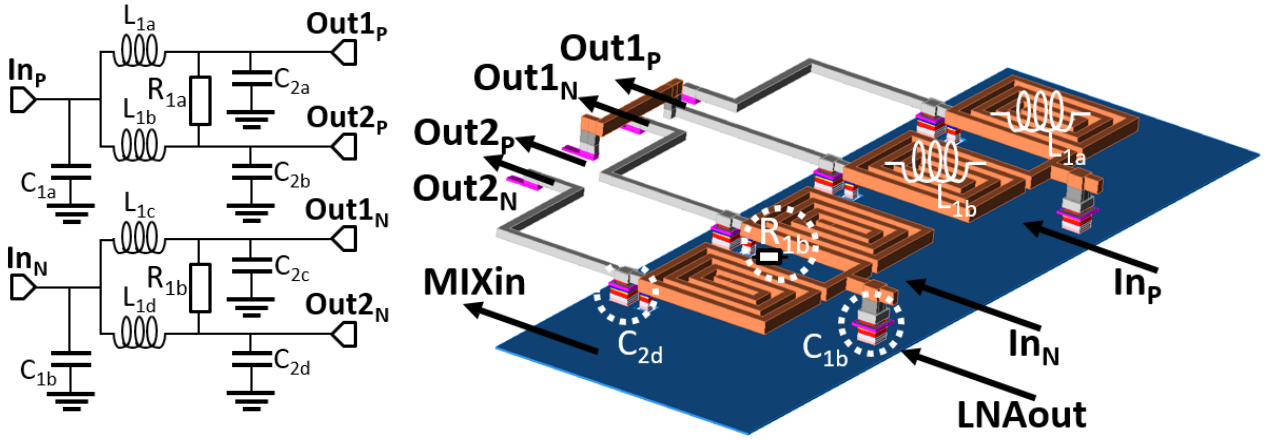

Figure 3.9: Schematic and layout of 60 GHz differential LC Wilkinson Power Divider.

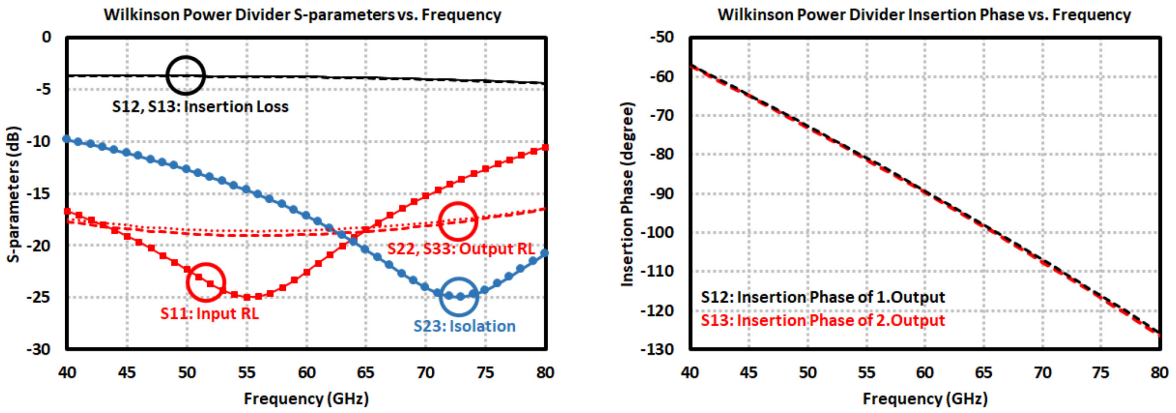

Figure 3.10: Simulation results of 60 GHz differential LC Wilkinson Power Divider: (*left*) S-parameters, (*right*) insertion phase at the divider outputs.

According to simulation results shown in Figure 3.10, the average insertion loss is found as 3.8 dB at 60 GHz with input and output matched to differential 100 Ω within a quite wide band. Moreover the phase and amplitude imbalances at the output ports are 0.7° and 0.06 dB respectively thanks to a full symmetric design. Similar power divider structure is employed in 122-GHz TRx and reaches almost the same performance metrics.

A good way to obtain in-phase and quadrature signals required for the mixers is to implement hybrid couplers based on impedance controlled transmission lines. Although there are methods to decrease the overall size it occupies by adjusting the line lengths and characteristic impedances, architectures based on lumped elements offer the same performance in a smaller area. Thus in-phase and quadrature signals are generated by two parallel quarter wavelength transmission line based couplers as shown in Figure 3.11 which same design metrics as the power divider are of importance. These transmission lines are again designed as inductors for compactness. While the in-phase output is obtained directly from the VCO signal, the quadrature output is achieved by its coupled reference terminated with 50 Ω impedance. Because the outputs are fed into the switching quads of mixers (cascode pairs), series capacitors are placed at these nodes, not to disturb the biasing of switching transistor pair.

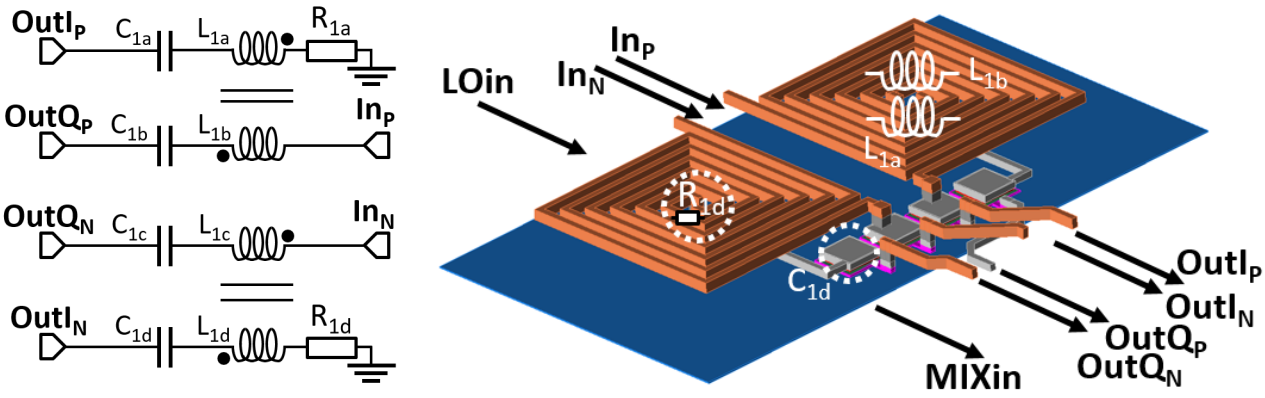

Figure 3.11: Schematic and layout of 60 GHz differential I/Q signal generator.

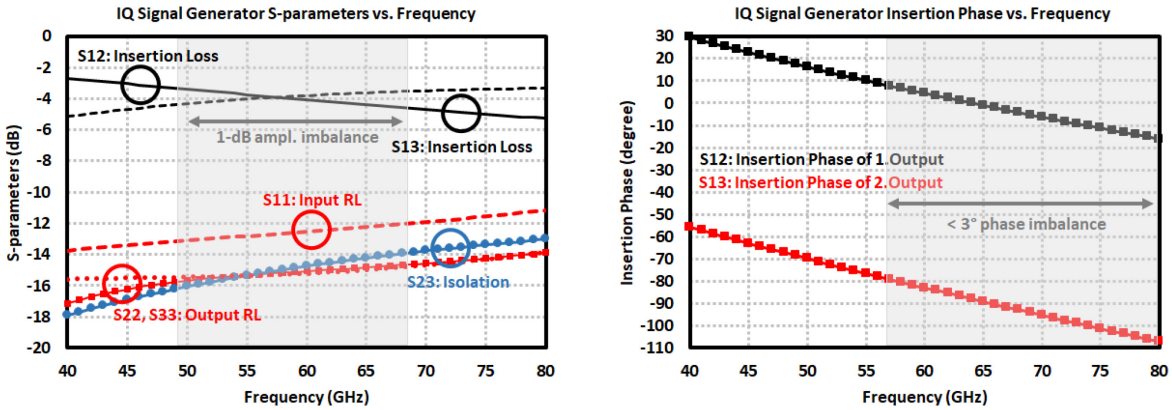

Figure 3.12: Simulation results of 60 GHz differential I/Q signal generator: (*left*) S-parameters, (*right*) insertion phase at the divider outputs.

The simulation results in Figure 3.12 highlight an average insertion loss around 4 dB having input and output return losses below 10 dB in the entire band. Within the band of interest, the

phase and amplitude imbalances are found as 2° and below 1 dB respectively. The quadrature Rx in 122-GHz TRx uses the same architecture achieving 4 dB insertion loss as well.

The mixer specifications are mainly determined depending on the linearity requirements rather than the noise figure and conversion gain metrics. Because the total Rx gain could be compensated by off-the-shelf baseband amplifiers placed on board as long as the excessive noise figure coming from the mixer could be suppressed by the LNA gain, thus not requiring a strict gain metric from the mixer side at the end, which also relaxes the mixer noise performance requirements at the same time. Nonetheless the Rx linearity is of a bigger concern when designing the mixer since the amplified LNA output power should not cause mixer to saturate and lower the overall Rx linearity in case of excessive received power at the antenna input or the internal Tx signal leakage.

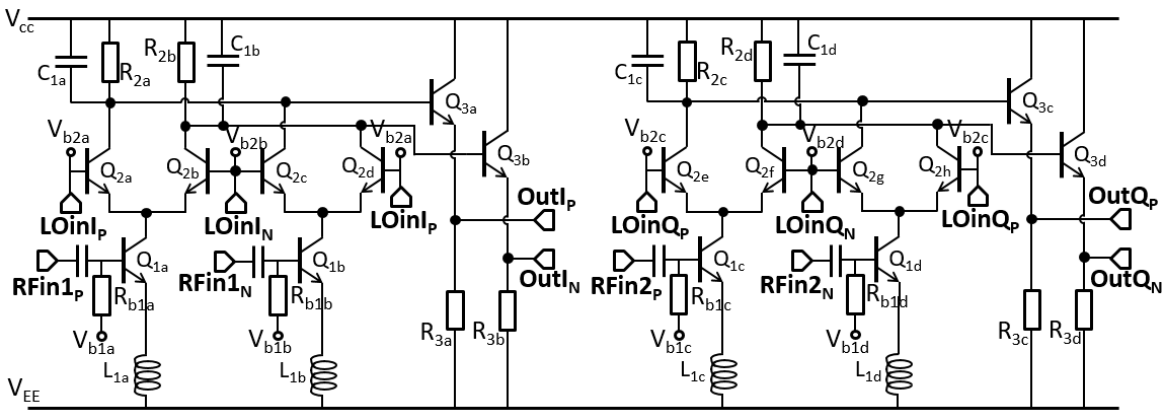

Figure 3.13: Schematic of 60 GHz double-balanced Gilbert-cell based quadrature mixer.

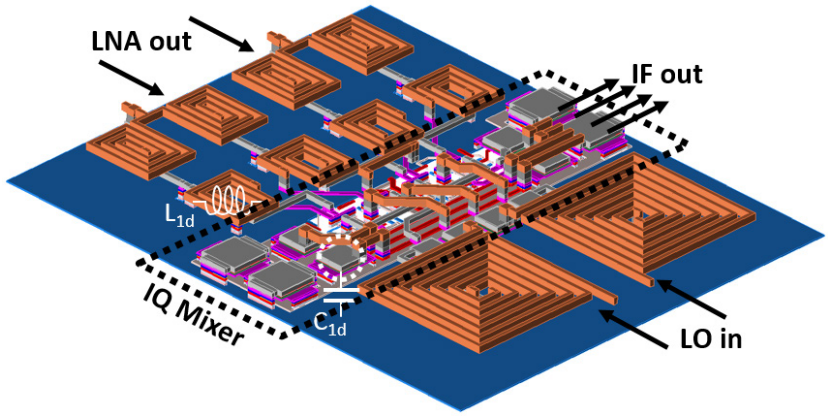

Figure 3.14: Layout of 60 GHz double-balanced Gilbert-cell based quadrature mixer.

The overall requirements from the Rx channel are already defined by the system level design parameters as mentioned previously. In this context, the total 18.6 dB of LNA gain, which is further reduced by the insertion loss of power divider, could support the high noise figure of quadrature mixers. So an active topology based on double-balanced Gilbert-cell architecture with the main design emphasis on linearity is implemented. This configuration is known to exhibit a

high conversion gain and spurious product suppression. Moreover linearity, even order distortion and LO-RF / LO-IF isolation are improved while only moderate LO power on the cascode transistors is required for appropriate switching.

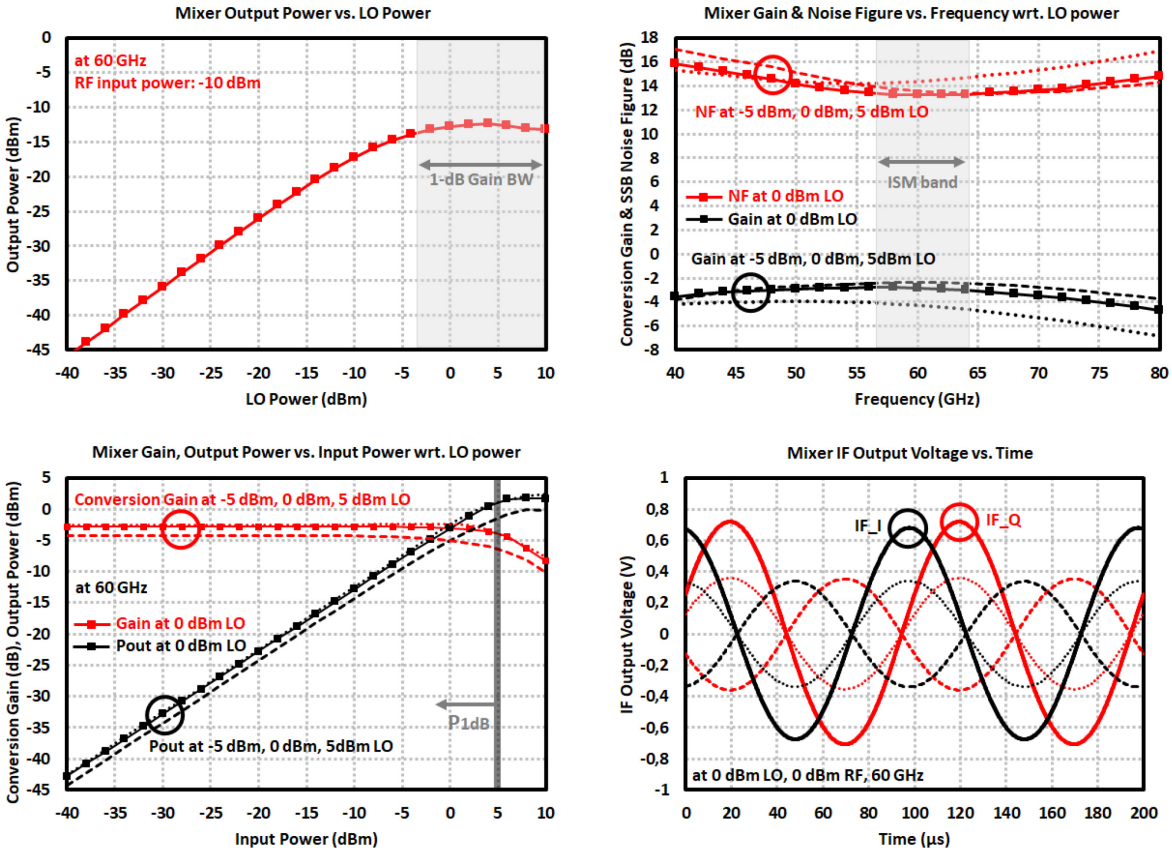

Figure 3.15: Simulation results of 60 GHz Mixer chain: (*top left*) output power vs. LO power, (*top right*) conversion gain and noise figure with respect to LO power, (*bottom left*) conversion gain and output power with respect to LO power, (*bottom right*) IF output voltages in time domain.

The circuit schematic and layout are seen in Figure 3.13 and Figure 3.14 respectively. It is composed of a differential transconductance pair (Q_1), where optimizations are completed to extract a decent gain with improved compression point, and switching / current commutating transistors (Q_2) which are sized to maintain this linearity and minimize the LO loading. Same current mirrors are utilized to bias the mixers. The degeneration inductors (L_1) placed at the emitter terminals not only acts as a current path, but also provides a wideband matching for the mixer inputs when combined with the intrinsic base-emitter capacitor (C_{be}) seen at this node and improves the linearity by reducing the effect of this impedance term created by C_{be} at the expense of reduced conversion gain. Since the switching pairs are differential, the LO waveform carries no DC term highlighting that RF feedthrough is suppressed. Furthermore the current at the IF output stays constant with respect to changing applied LO power which translates into LO feedthrough improvement. However the mixer architecture itself cannot be completely symmetric by nature

which might create DC offsets at the IF nodes and the fabrication tolerances especially in these switching stages would also result in LO signal leakage. Nevertheless for the current system application, it would not create much issue since the RF / LO and targeted IF tones are quite apart. But the DC offset due to LO self-mixing limits the dynamic range causes dead zones in radar systems which has to be taken care of. Since the received signal levels are quite low in the radar systems, generally additional amplifiers are accommodated at the IF outputs which might become saturated due to magnified offset levels as well.

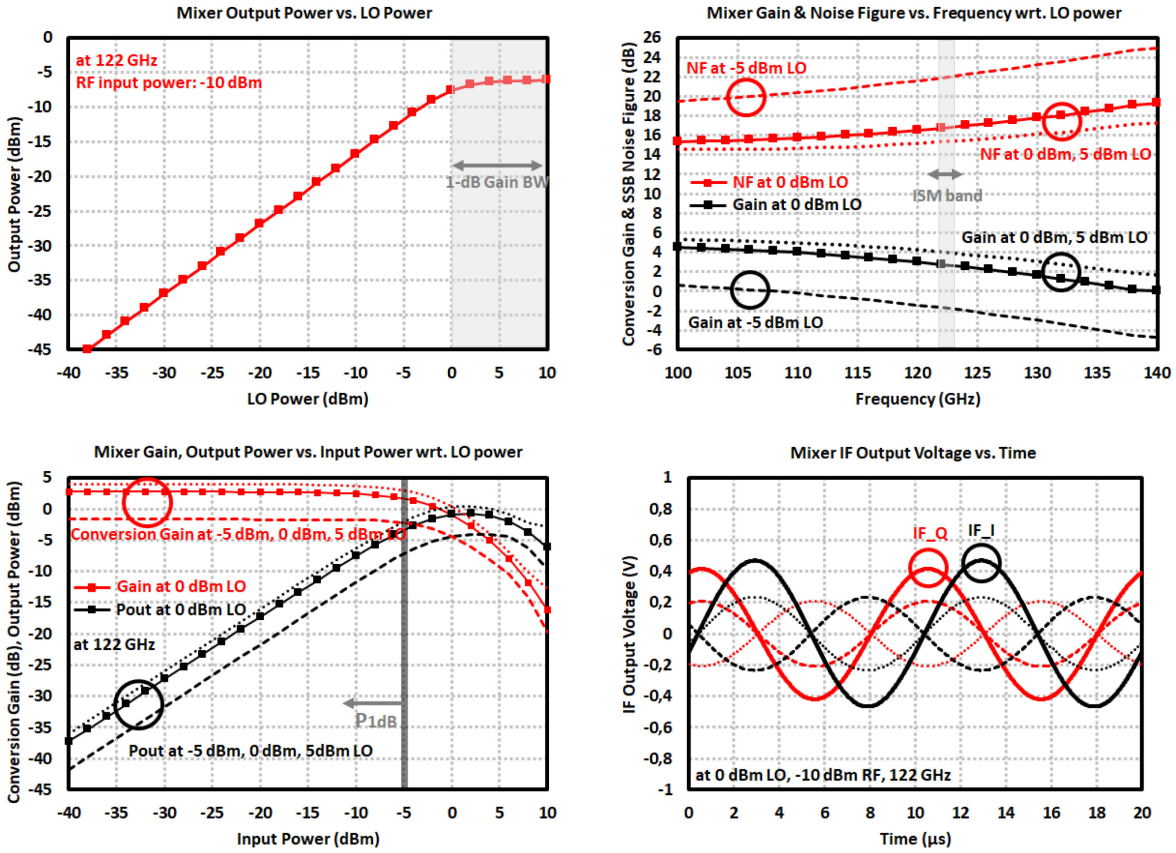

Figure 3.16: Simulation results of 122 GHz Mixer chain: (*top left*) output power vs. LO power, (*top right*) conversion gain and noise figure with respect to LO power, (*bottom left*) conversion gain and output power with respect to LO power, (*bottom right*) IF output voltages in time domain.

Because the noise contribution from each transistor is independent, in the case of switched-on common-base pairs (i.e. Q_{2a} & Q_{2b}) at each LO cycle, this section behaves as a differential amplifier and contribute to noise performance, thus large enough LO power is useful to shrink this transition time. On the other hand, the switching pairs have resistive loads forming low-pass-filters (R_2 & C_1) at the low frequency IF outputs. Finally buffers as single-stage emitter-followers (Q_3) are accommodated at the IF outputs to provide a low impedance output, help increase the isolation and reduce the overloading on the successive amplification stage.

Figure 3.15 shows the simulation results of the corresponding mixer chain combined with power divider, quadrature signal generator and IF buffers. For the optimum operation point to reach maximum IF output power, LO power is swept where above -3 dBm LO already turns on the switching pairs completely. With 0 dBm applied LO, the mixers achieve -2.8 dB of conversion gain in total with SSB noise figure of 13.2 dB at 60 GHz. The IP_{1dB} is found as 5 dBm with a OP_{1dB} of 1.2 dBm before saturation. The phase and amplitude imbalances of the quadrature IF channels are 12° and 0.3 dB due to the uneven connections between quadrature signal generator and mixers. Finally the power consumption of this chain occupying 250 µm x 200 µm area is 47.1 mW at 3.3V.

Since the transmitter output power is much lower compared to the one in 60-GHz TRx, the internal leakage on Rx channel would be less as well. Thus a higher conversion gain could be obtained from the 122-GHz mixer. This is achieved by using the same topology in Figure 3.13 and modifying the biasing scheme to ensure higher current drain through larger transconductance transistors along with the common-emitter scheme. The inductive degeneration is removed at the same time to further help increase the gain at the expense of reduced linearity. The simulation results of fabricated mixer could be viewed from Figure 3.16. Conversion gain of this chain is simulated to be 2.7 dB with 16.5 dB noise figure at 122 GHz. The IP_{1dB} and the resulting OP_{1dB} become -5 dBm and -1.7 dBm. It consumes 32.9 mA of current from 3.3 V.

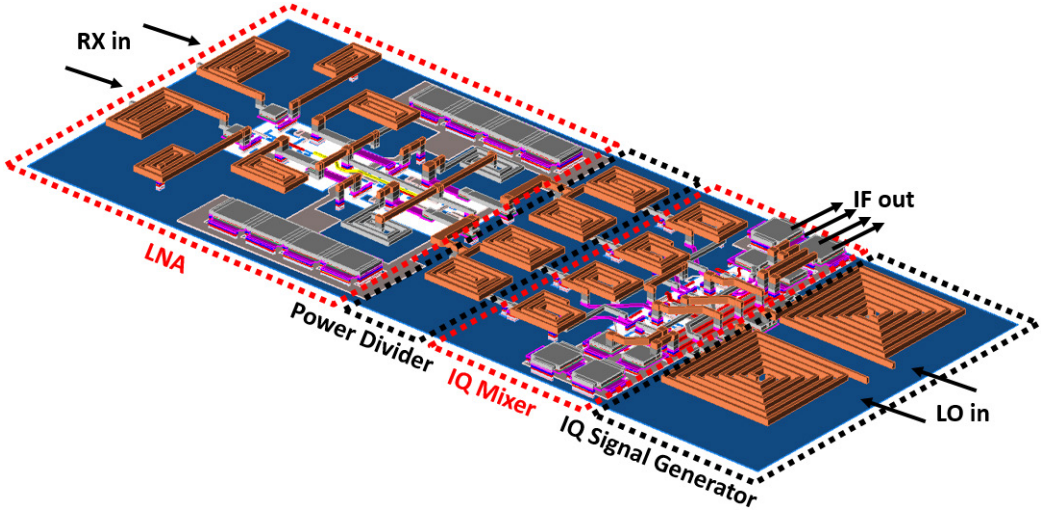

Figure 3.17: Layout of 60 GHz Rx channel highlighting the sub-blocks (450 µm x 250 µm).

Considering all these design steps, the 60-GHz version of Rx channel (see Figure 3.17) occupies only an area of 0.45 x 0.25 mm^2 with a power consumption of 74.6 mW at 3.3 V of single supply. After full EM simulations of all the blocks included which takes the mismatches and cross-talk into account (see Figure 3.18), 15.6 dB of conversion gain and 8.1 dB of SSB (Single-Side-Band) noise figure is expected. The IP_{1dB} is around -16 dBm at 60 GHz with 0 dBm LO applied. The quadrature IF outputs have 12.3° of phase and 0.3 dB of amplitude imbalances. Within the industrial temperature range (-40°C to +85°C), the circuit is operational and the conversion gain varies by about ±4 dB whereas the current consumption changes by only 2 mA.

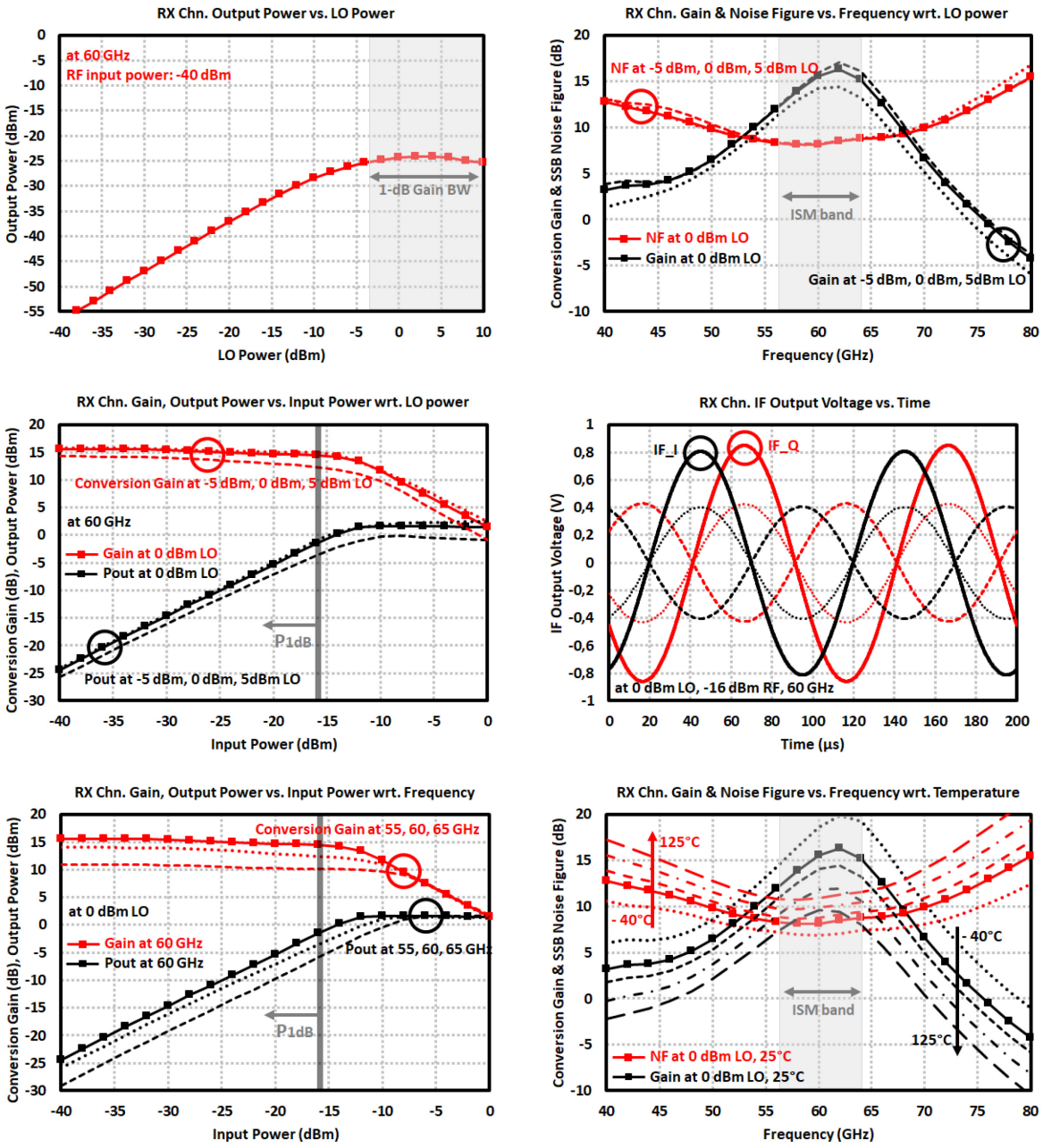

Figure 3.18: Simulation results of 60 GHz Rx channel: (*top left*) output power vs. LO power, (*top right*) conversion gain and noise figure with respect to LO power, (*middle left*) conversion gain and output power with respect to LO power, (*middle right*) IF output voltages in time domain, (*bottom left*) conversion gain and output power with respect to frequency, (*bottom right*) conversion gain and noise figure with respect to temperature.

The 122-GHz version, in other respects, has 20.5 dB conversion gain, 10.9 dB noise figure and -21 dBm IP_{1dB}. With the adjusted gain options, linearity could be further improved if required depending on the application. These results are highlighted in Figure 3.19. The current consumption of this channel occupying 0.44 x 0.20 mm^2 of area is 57.3 mA at 3.3 V single supply. Within the industrial temperature range, the gain drops to 14.6 dB and noise figure rises to 13.5 dB at

85°C. The I- and Q- outputs phases are better aligned compared to 60-GHz Rx channel with amplitude errors are a bit amplified. The main reason comes from the non-symmetric mixer LO feeding sections which is inevitable due to the circuit nature.

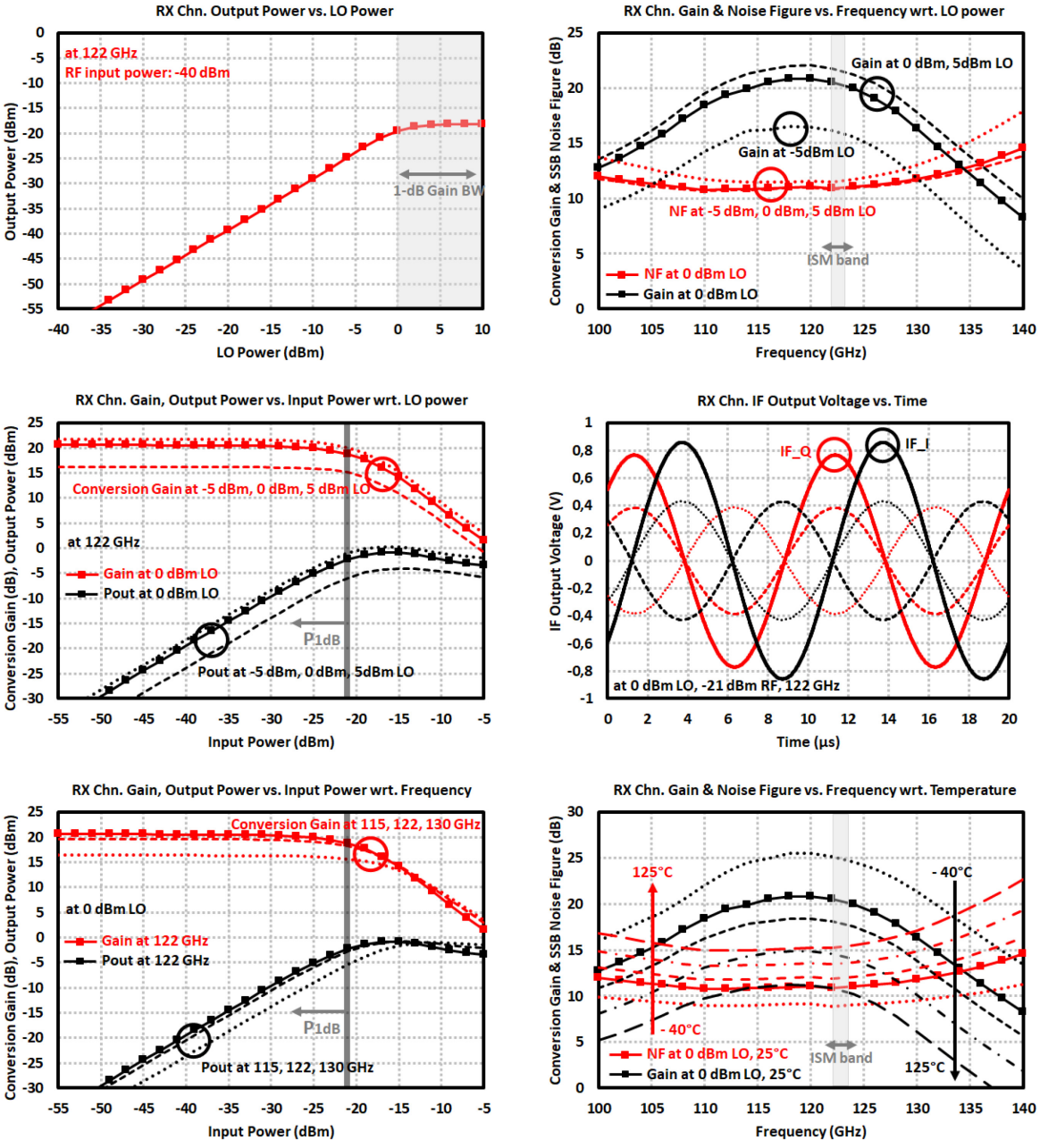

Figure 3.19: Simulation results of 122 GHz Rx channel: (*top left*) output power vs. LO power, (*top right*) conversion gain and noise figure with respect to LO power, (*middle left*) conversion gain and output power with respect to LO power, (*middle right*) IF output voltages in time domain, (*bottom left*) conversion gain and output power with respect to frequency, (*bottom right*) conversion gain and noise figure with respect to temperature.

In the 122 GHz TR2 TRx, a balun is integrated at the front to convert to single-ended for easy on-board handling and antenna matching including interconnect effects. A wideband Marchand structure having an insertion loss of 1.6 dB and acceptable input and output return losses is designed. The layout and simulation results are depicted in Figure 3.20 and Figure 3.21. The out-of-phase outputs of differential port are also phase- and amplitude-matched for proper signal delivery into the LNA. The design includes coupled transmission lines with optimized widths, spacing and lengths respectively for correct impedance match, coupling strength and operation band. Since transmission lines are utilized, a wider bandwidth could be achieved. Obtaining equal phases at the 100 Ω nodes is again crucial for appropriate signal combining for the LNA input. Therefore a necessary performance degradation in Rx channel due to the balun is expected. Because the matching is not satisfied perfectly, the expected loss increases and is verified by simulations having Rx channel and balun integrated. Same applies to Tx (see Section 3.4), with an output power degradation of around 2.5 dB.

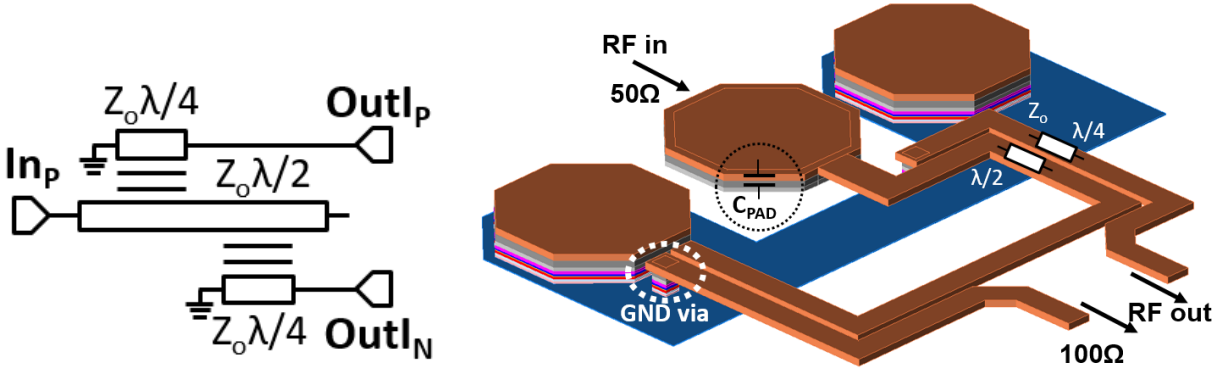

Figure 3.20: Schematic and layout of 122 GHz Marchand Balun.

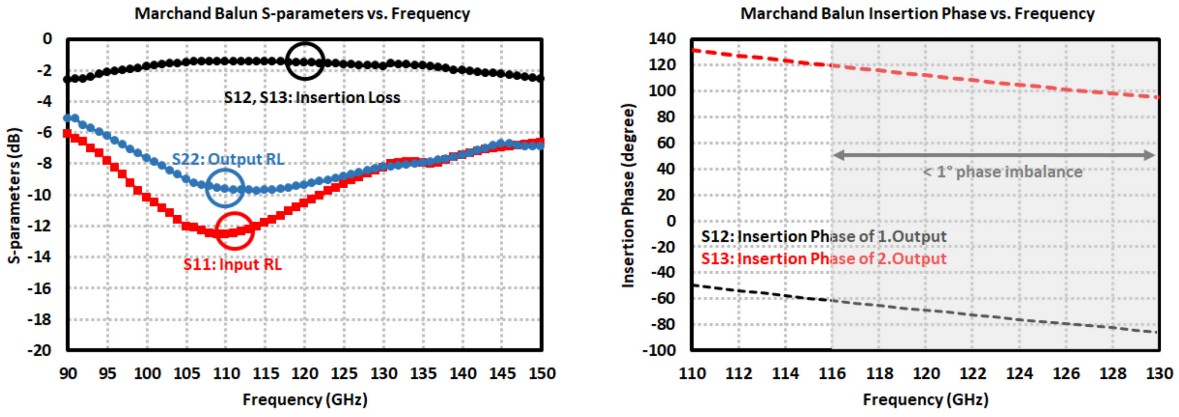

Figure 3.21: Simulation results of 122 GHz Marchand balun.

In the TRM versions of chips in both frequency bands, tunable high isolation couplers are integrated at the inputs, hence combining Tx and Rx channels to create a single antenna input so

that both channels could simultaneously operate and utilize the same radiating element as opposed to heavily used switched channel topology [52], [67]. The same Wilkinson power combiner architecture is employed which the corresponding schematic and 3D model are visualized in Figure 3.22 respectively. It is possible to observe frequency shifts in some IC blocks after the fabrication process owing to many reasons such as wrong transistor modeling, process variations and imperfections and unconsidered electromagnetic effects in layout. These could lead to problems like bandwidth and gain degradation, reduced linearity and so on. Therefore enough isolation at the correct frequency band should be guaranteed to minimize the inevitable Tx output signal leakage. In case of a frequency shift in the resonance peaking frequency of this coupler, the targeted isolation level of 30 dB could not be reached, and might even lead to Rx channel saturation and obscure the detection of targets arriving with very low power. To hinder this issue, a tuning mechanism at the differential RF input pads through variable capacitors is introduced such that the minimum possible leakage is achieved with the adjusted voltage. Then this voltage level could be fixed on board through resistive dividers.

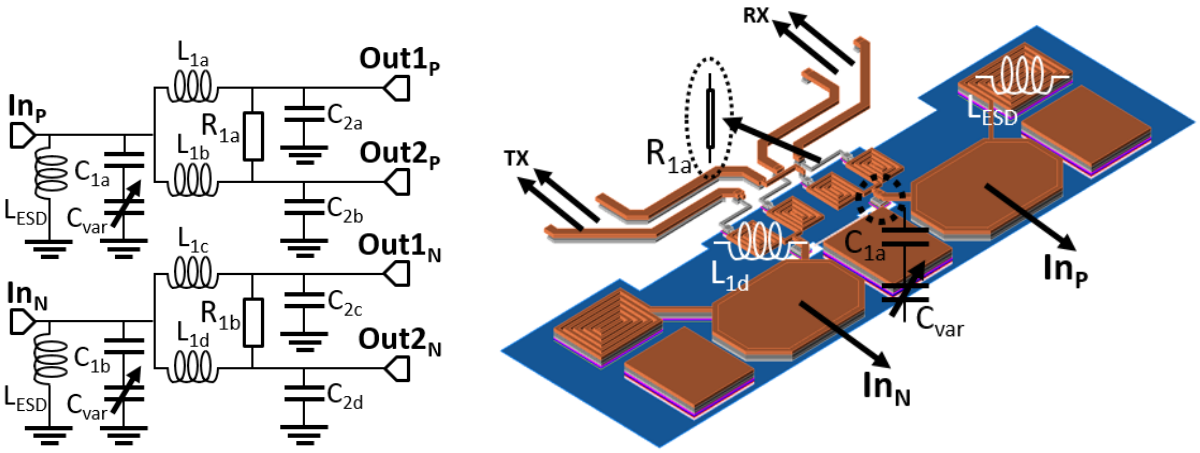

Figure 3.22: Schematic and layout of 60 GHz high isolation coupler.

The full electromagnetic simulations are performed including the input pads and shunt inductor used as an effective ESD structure, where the final layouts are optimized to get better isolation performance with good enough return losses. The simulation results shown in Figure 3.23 and Figure 3.24 demonstrate the S-parameters with respect to changing tuning voltages between 0 - 3.3 V. Based on these results, the average insertion loss is around 5.78 dB at 60 GHz and 5.88 dB at 122 GHz with full ISM band coverage of output port isolation. As a result better than 30 dB isolation would be attained. Furthermore the input and output return losses are kept better than -10 dB within the ISM bands. However the coupler poses disadvantage in Rx channel by increasing the noise figure and decreasing the conversion gain while reducing the transmitted output power in the Tx channel at the same time. Yet such effects could not be avoided considering a design with single antenna input.

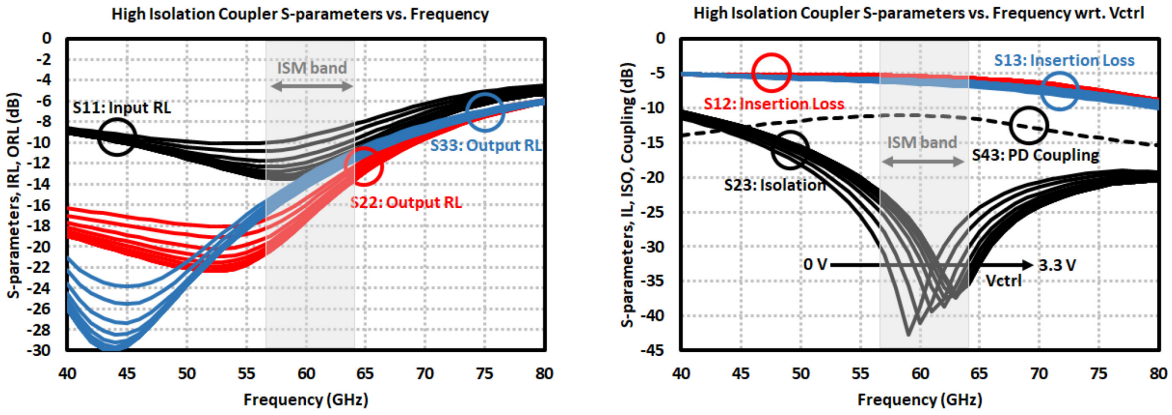

Figure 3.23: Simulation results of 60 GHz high isolation coupler: (*left*) input and output return losses, (*right*) insertion loss, isolation and coupling loss to power detector with respect to tuning voltage.

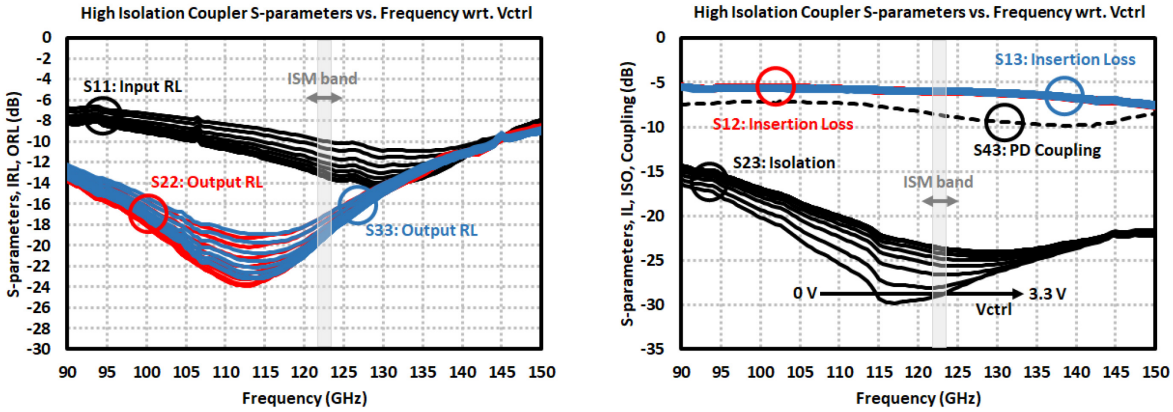

Figure 3.24: Simulation results of 122 GHz high isolation coupler: (*left*) input and output return losses, (*right*) insertion loss, isolation and coupling loss to power detector with respect to tuning voltage.

Since a separate coupler test block is not fabricated, such tuning mechanism could not be measured directly, but its effect on the IF outputs are checked on oscilloscope by observing if phase and amplitude distortions emerge due to the leakage from Tx channel. While the Tx is set to its maximum output power mode, no significant changes are observed with respect to different tuning voltages – even in the case when Tx is completely switched off – but minor improvements for some voltage levels. Furthermore on the FMCW radar test board, the coupler tuning pin is made accessible for adjustments during real-time operation which, at the end, is found to be not visibly changing the target amplitudes except couple-dBs improvement of blind spot region due to DC offset. As a result, it is found out that the coupler isolation level is already high enough not to be affected by any tuning voltage since such pin is inserted just in case if the electromagnetic simulations does not match the measured results.

3.4 Transmitter Channel Design

The main element in the transmitter channel is power amplifier which is, depending on the transceiver architecture, accompanied by either a power detector, some passive transmission network to couple out the signal for this power detector, a balun or the front isolation-coupler aforementioned.

In the fabricated chips for both 60- and 122-GHz TRxs, two-stage cascode topology is chosen for the power amplifier whose fundamental metrics mainly include output power, power gain and efficiency. Depending on the efficiency requirements, class of operation could be selected as well. However main optimizations took place in maximizing the output power in all the fabricated ICs, thus an optimized version of LNA circuit is developed instead of designing it from scratch. Since the biasing is not greatly changed for the cascode structure, the operation mode stays at class-A mode and provide high linearity and speed. This mode is known to ensure 360° of conduction angle, meaning that the circuit conducts the whole period of sinusoidal input signal, as illustrated in Figure 3.25. Since the conduction takes place even in case of no signal applied, efficiency is much lower compared to other classes which are optimized at operation points close to transistor pinch-off, hence conducting above certain input level. In contrast to conventional class-A, AB, B and C modes where the active device acts as a voltage-controlled current source, less straightforward class-D, E and F amplifiers benefit switching behavior of transistors with proper biasing, thus achieving higher-efficiency. So main disadvantage of class-A is high power consumption which contribute to chip heating considering that PA is the most power consuming block in full system. Especially in multichannel transceivers requiring multiple PAs, such heat dissipation issue might even cause chip failure. However with a neat design process, such issues could be prevented and then its high linear nature would be of great use.

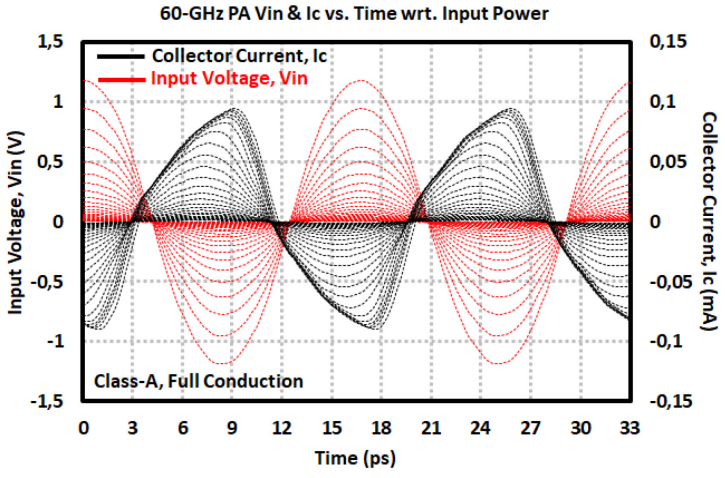

Figure 3.25: Class-A PA collector current and input voltage for swept input power levels for the fabricated 60-GHz PA.

Although the circuit schematic is quite similar to the LNAs shown in Figure 3.6, there exist distinct design steps to achieve a high performance PA in the end. The fundamental difference is the parallel transistors at each cascode stage which ensure higher current handling capability, as a result, increasing the transmitted output power by boosted current swing. The circuit is operating close to its saturation point to achieve the highest possible power added efficiency (PAE). This is guaranteed by the delivered VCO output power which will be discussed in Section 3.5.1 in detail. Employing larger sized transistors offers higher delivered power while optimum input impedance and output load resistance are lowered. The matching networks could be further facilitated with the increased transistor size, but up to a point where these networks become complicated. This would eventually necessitate either networks with higher quality factor, that is generally not possible due to the technology, or higher order filter design with multi-stage / distributed architecture, that introduces additional losses. As a result, compared to LNA, input and output return losses in PA are expected to perform with much higher bandwidths. The load inductors, that help voltage swing above the supply, are drawn with much wider widths to hinder transmission line breakdown due to excessive current. Finally the layout of the designed PA could be viewed in Figure 3.26.

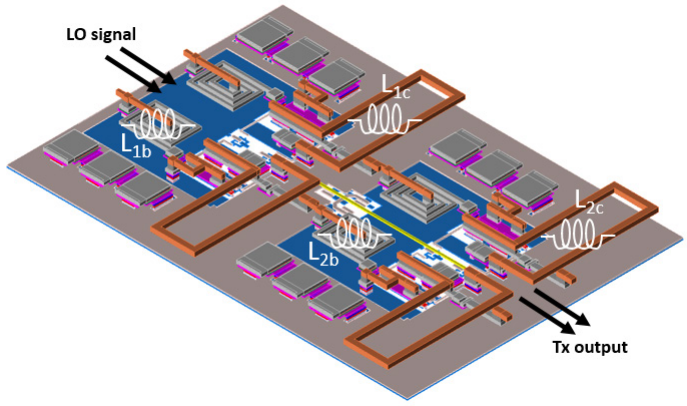

Figure 3.26: Layout of 60 GHz differential two-stage cascode PA circuit.

According to simulation results of the 60-GHz PA shown in Figure 3.27 and Figure 3.28, high gain around 20 dB is achieved over a bandwidth of 17.5 GHz – fully covering the ISM band while consuming 72.8 mA of current from 3.3 V supply. Moreover as expected, input and output return losses are improved compared to LNA and stay above 10 dB over a quite wide band. The integrated gain control pins could be used to adjust the gain to minimum 5.5 dB at 60 GHz with available mid gain values as well. An enable control voltage could be applied to bias circuitry to set the operation status of PA, which this is especially crucial in MIMO TRx to switch between multiple Tx channels in TDM operation. Furthermore the IP_{1dB} is around -5 dBm with a saturated output power (P_{sat}) of 17 dBm and a maximum PAE of % 17 at 4 dBm input power at 60 GHz. With respect to temperature changes, the gain varies between 16 dB and 21.5 dB at 60 GHz for -40°C and 125°C. Such increasing temperature adversely affects the output power, but just about 2 dB degradation is observed when 0 dBm of input power exists at the input of PA. With the integration of front isolation coupler in TRM version, the transmitted output power is expected to decrease

to 10 dBm. Overall high output power could be achieved, which the final FMCW radar greatly benefit by increasing the maximum detectable range.

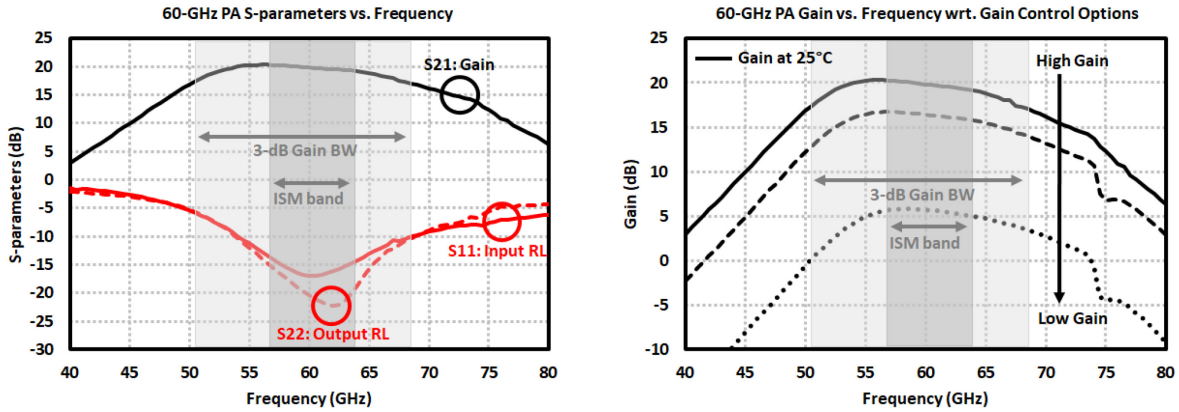

Figure 3.27: Simulation results of 60-GHz PA: (*left*) S-parameters, (*right*) gain with respect to gain control options.

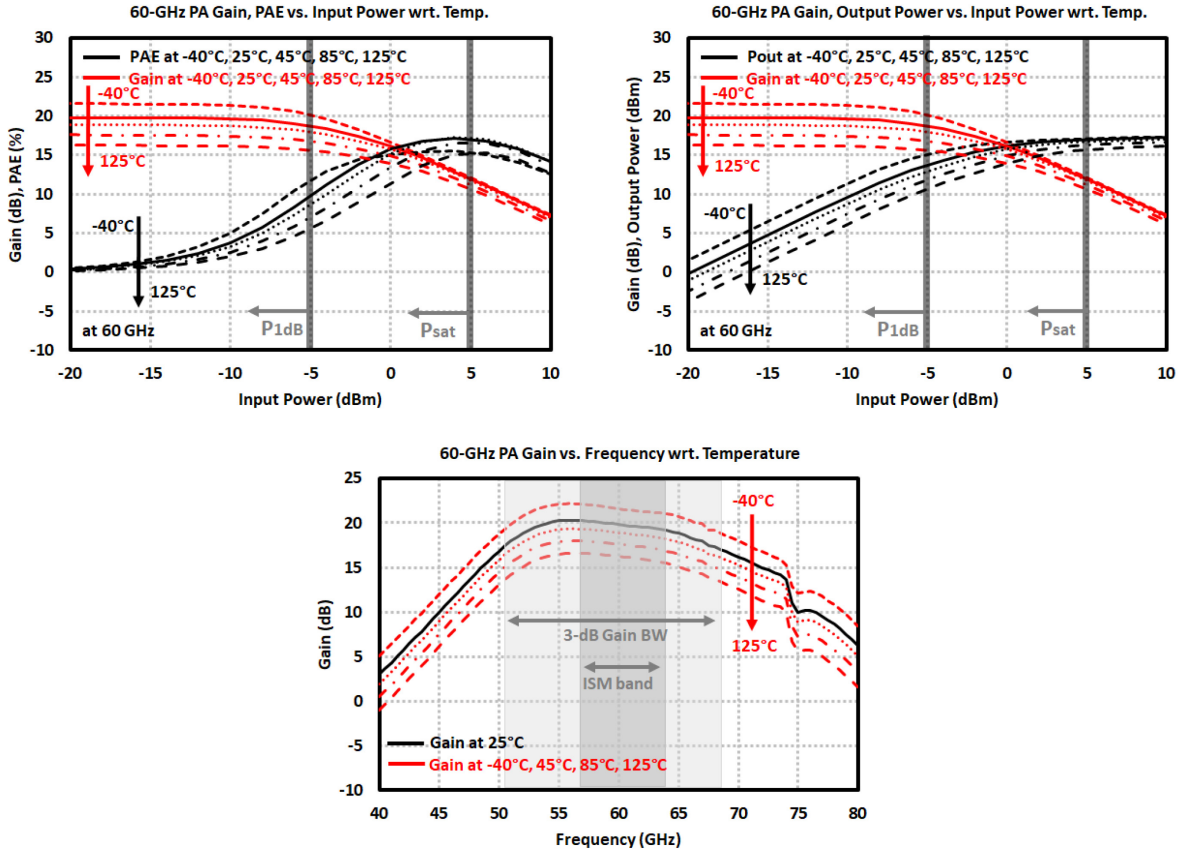

Figure 3.28: Simulation results of 60-GHz PA: (*top left*) gain and PAE at 60 GHz with respect to temperature, (*top right*) gain and output power at 60 GHz with respect to temperature, (*bottom*) gain with respect to temperature.

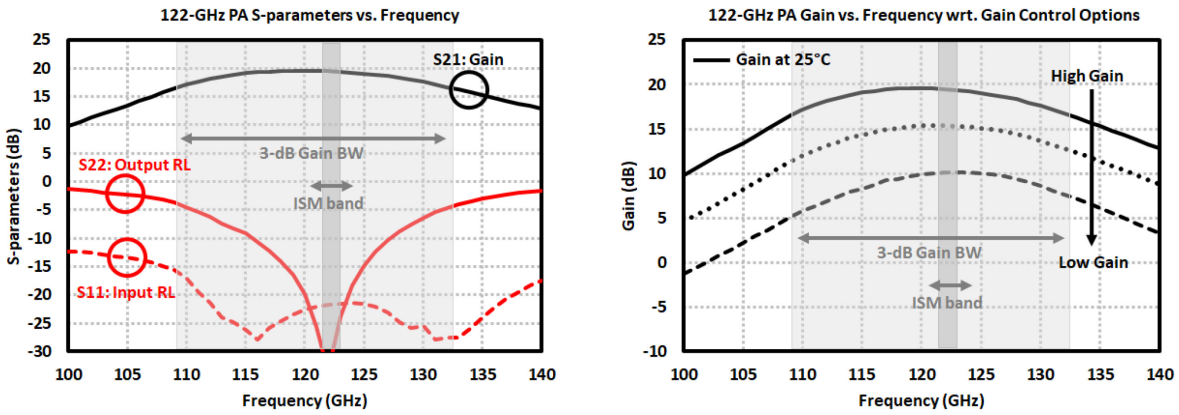

Figure 3.29: Simulation results of 122-GHz PA: (*left*) S-parameters, (*right*) gain with respect to gain control options.

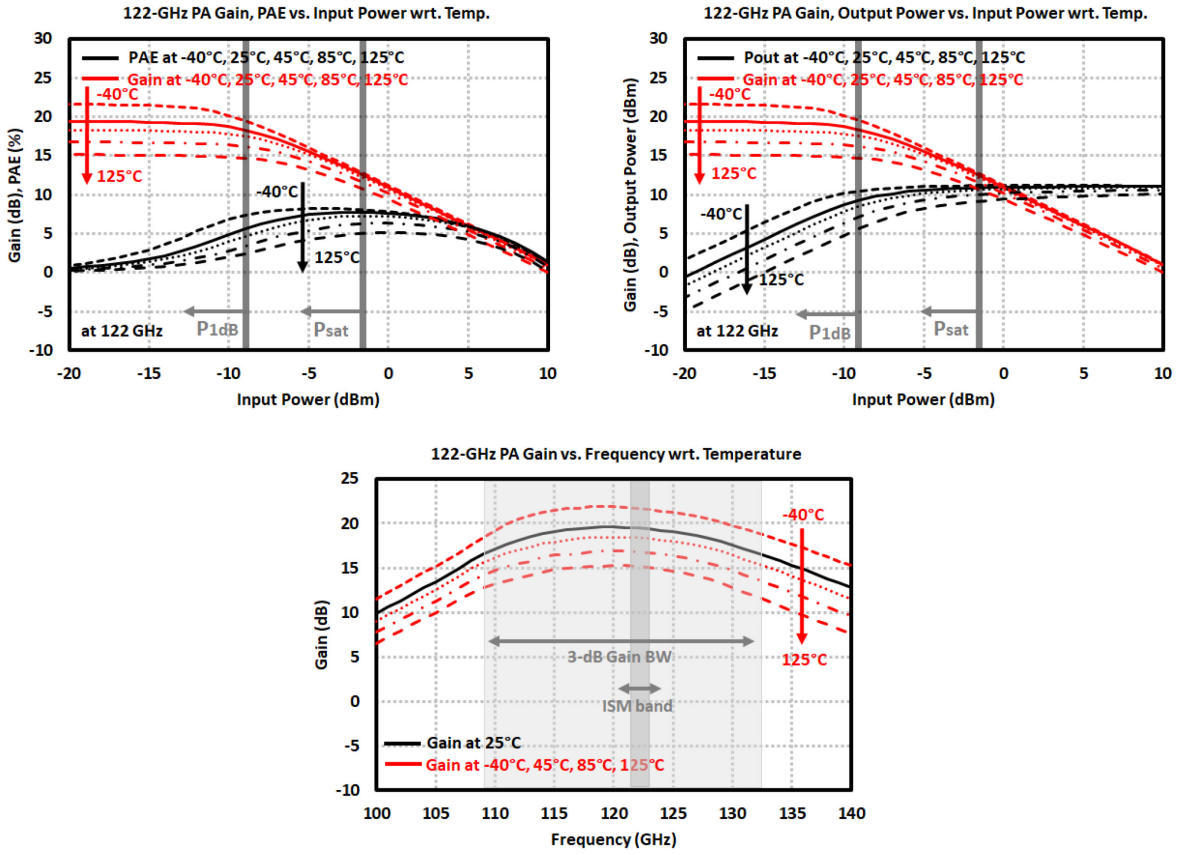

Figure 3.30: Simulation results of 122-GHz PA: (*top left*) gain and PAE at 122 GHz with respect to temperature, (*top right*) gain and output power at 122 GHz with respect to temperature, (*bottom*) gain with respect to temperature.

On the other hand, from the full EM simulations depicted in Figure 3.29 and Figure 3.30, its 122-GHz counterpart achieves around 20 dB of gain with a 3-dB bandwidth of 23.5 GHz (between

109 GHz and 132.5 GHz) and a maximum current consumption of 64 mA at 3.3 V supply. Return losses stay above 10 dB over the VCO operation bandwidth discussed in Section 3.5.1. Gain could be tuned with the same mechanism adopted in bias circuitry and could be decreased to 10 dB in case of lower power consumption requirement. Output power could reach 10.5 dBm, having an IP_{1dB} of -9 dBm while reaching its P_{sat} at -2 dBm of input power at 60 GHz. PAE is found as % 8 which is, with respect to increasing temperature, degraded as output power and gain.

In the TR2 version, balun decreases the output power by about 2.5 dB due to poor inter-stage matching. Assuming that the VCO could provide around 0 dBm input power to the PA (considering the loss from power divider), around 6.5 dBm of output power is expected at the Tx output of 122-GHz TR2 chip. On the other hand, the TRM version benefits front isolation coupler which reduces the transmitted output power again. In full EM simulations, 4.7 dBm output power is achieved from this 122-GHz TRM chip with 0 dBm LO power applied.

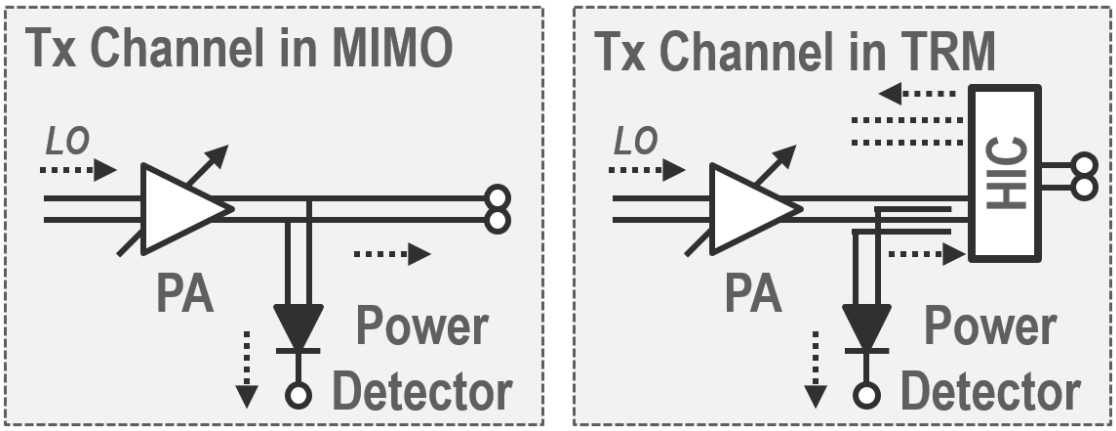

Figure 3.31: BIST circuits and coupling mechanisms including power detectors in Tx channels of, (*left*) 60-GHz MIMO TRx, (*right*) 60- / 122-GHz TRM.

After designing the PAs, output signal is coupled out to power detectors in order to monitor the transmitted power in a voltage scale. Such structures shown in Figure 3.31 are called BIST (Built-In-Self-Test) circuits since they could provide a functionality test capability without requiring any external measurement equipment. In the Tx case, in order not to reduce the transmitted power, a coupling mechanism with low insertion loss on the main path should be placed, therefore providing high coupling loss. This loss of coupling, together with the PA output power, should be considered in designing the accepted input power levels to be monitored by the power detector, to stay within its dynamic range.

The coupling mechanism is either integrated to the front isolation coupler as in TRM 60- / 122-GHz TRx with / without antenna, or designed separately as a directional coupler at the PA output right before the pads as in 60-GHz MIMO TRx (see Figure 3.32). In both cases, the Tx combining branch of coupler has the identical branch on lower metal layer (TopMetal1) to couple out certain

portion of the signal. Generic microstrip-line directional couplers has coupled transmission line lengths matched to $\lambda/4$. While the opposite end of the coupled port is isolated normally considering the coupled section has the correct length, neither the length is optimized nor the isolated port is terminated properly, since it is not the target to divide the signal almost equally between *through* and *coupled* outputs. Such weak coupling provides not only a lower insertion loss on the *through* path, but also increases the loss on the *coupled* path, thus requiring a power detector having sensitivity between -23 dBm to 5 dBm which could be easily achieved.

The S-parameter simulation results of the 60-GHz versions seen in Figure 3.32 points out an insertion loss of 5.78 / 0.53 dB in average and coupled output has a signal level reduction of 10.85 / 21.57 dB (Tx output referred) within the ISM band respectively for front coupler / pad integrated mechanisms. The 122-GHz counterparts achieve similar performances as well.

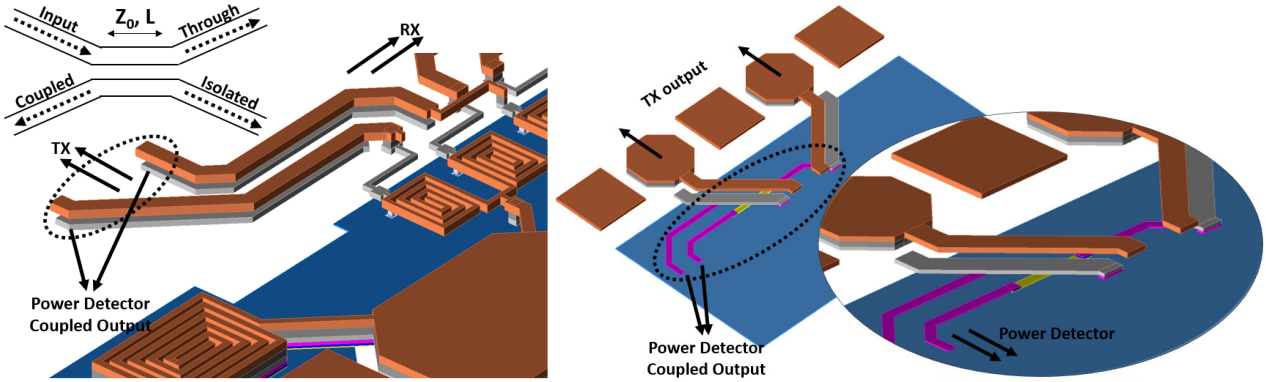

Figure 3.32: Layout of power detector coupler mechanism integrated to (*left*) high isolation coupler in monostatic TRxs and (*right*) Tx output pads in 60-GHz MIMO TRx.

Power detector schematic and simulation results are shown in Figure 3.33. The differential coupled inputs are applied from AC coupling capacitors of 200 fF (C_1) which is connected to the outputs shown in Figure 3.32, and then are combined at the collector terminals of the transistor pair Q_1 where the input power is converted to voltage. In high frequency power detectors, the input section should normally contain a 50 Ω matched LC section to better optimize for responsivity, however such matching network is not designed not to increase the die area since only its dynamic range is of concern. The output is then followed by a pMOS load transistor (M_1) and a diode-connected HBT transistor (Q_2). The second stage includes single-transistor amplifier as a DC level shifter attached to a low-pass filter composed of 500 fF capacitor (C_2) to filter out the RF signal and its harmonics. The bias network (connecting to V_{b1}) is formed by a current mirror where the DC point at the base is carefully set to adjust the observable range. Since the circuitry does not contain a reference block to be subtracted from the main detector path to cancel out the offsets caused by various mechanisms, at least the temperature stabilization is realized by employing p-doped gate polysilicon resistors having low temperature coefficients when combined with

HBT transistors. For the other coupling mechanism in Figure 3.32 (coupling from Tx output pads), power detector range is optimized accordingly.

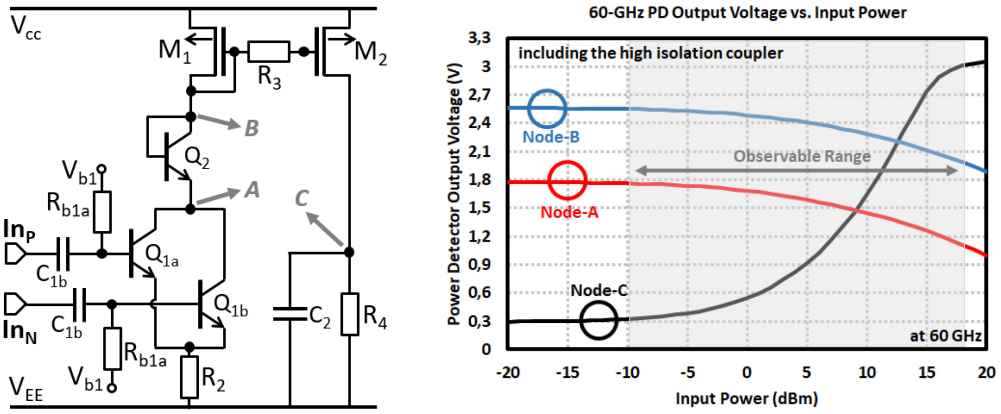

Figure 3.33: Schematic and simulation results of power detector together with high isolation coupler in 60-GHz TRM.

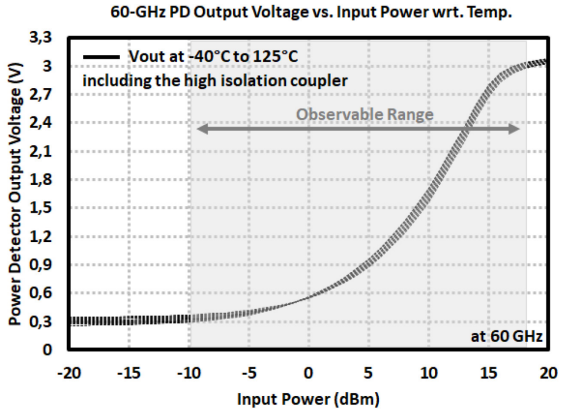

Figure 3.34: Power detector output voltage with respect to temperature.

The simulations in Figure 3.33 are done with power detectors attached to front coupler in 60-GHz TRM transceivers as an example, taking the coupling and insertion losses into account. According to results, input power ranging from -10 dBm to 18 dBm, which is generated after the PA (for the structure with HIC in Figure 3.31), could be observed corresponding to a voltage change between 360 mV to 3.02 V at *node-C*. Since 60-GHz PA has a simulated saturated output power around 17 dBm and the gain options could help reducing the output power further, such sensitivity range already meets the requirements. With respect to temperature (see Figure 3.34), it maintains a constant output curve between -40°C to 125°C. Finally the circuit consumes only 310 µA at 3.3 V supply. Similar performances are expected in 122-GHz power detectors.

3.5 LO Signal Generation and Distribution Network

The fundamental elements of LO chain are surely VCO and frequency divider. These signal generators (20-GHz VCO in MIMO chip, 60-GHz and 122-GHz VCOs in single- / double-channel TRxs) and various frequency dividers had already been designed and proven to be functioning previously such that they are not designed from scratch. In context of this thesis work, some modifications on these ready blocks were carried out in order to improve the performance and better optimize them for the intended TRx designs, which forms the scope of this section. As seen from the block diagrams in Figure 3.35, the updated VCO and frequency dividers are accompanied by various active and passive circuit components which are detailed in the following sections.

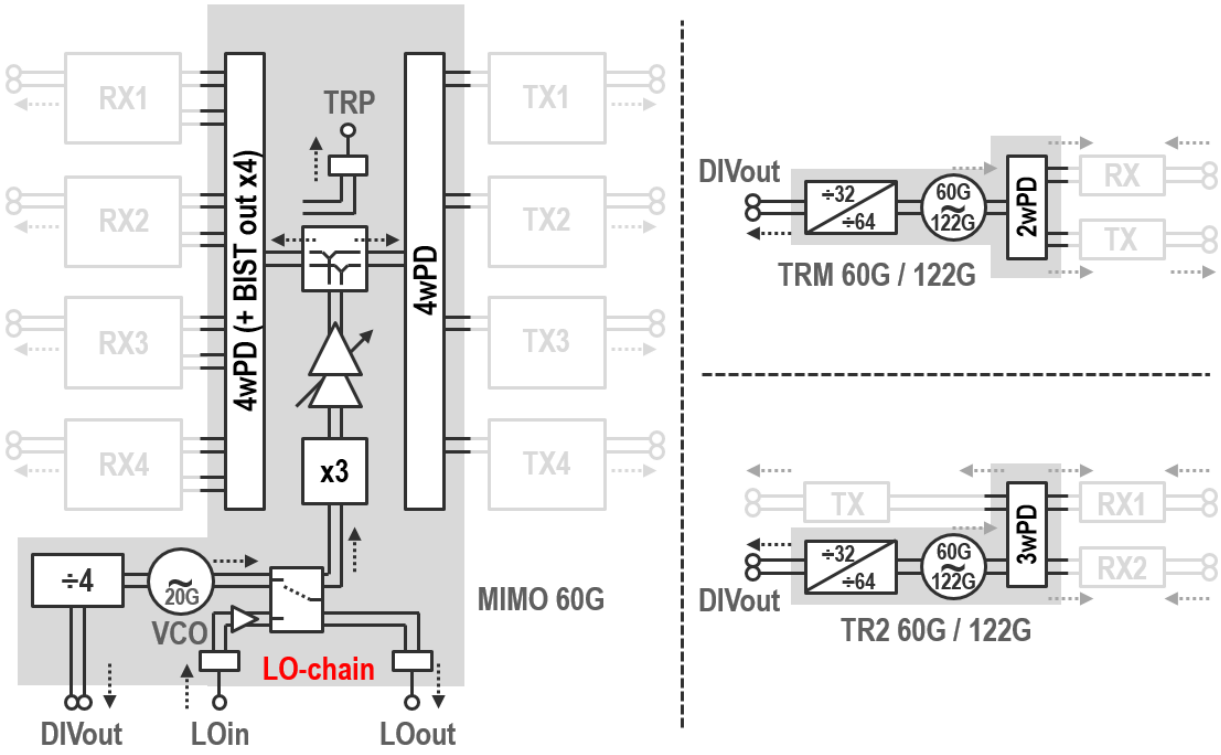

Figure 3.35: LO signal distribution networks for different chips including monostatic, double-receive, MIMO TRx.

3.5.1 VCO Design

In TRM and TR2 transceivers, LO signal generation is carried out by a VCO which is integrated to a frequency divider and an amplifier. In this context, the required LO signal for 60 GHz chip is generated through a push-push type tunable Colpitts oscillator as shown in Figure 3.36. The core center frequency is set to 30 GHz, namely f_o, with the help of a differential LC-tank circuit which

is of L_1, C_1 including transistor parasitics of Q_1 pair and C_2 in combination with varactors. The output spectrum at *node-A* of this tank circuit is highlighted on the same figure together with its harmonics as well. Then the 60 GHz signal is achieved from the second harmonic benefitting from the high non-linearity of Q_1 transistor pair.

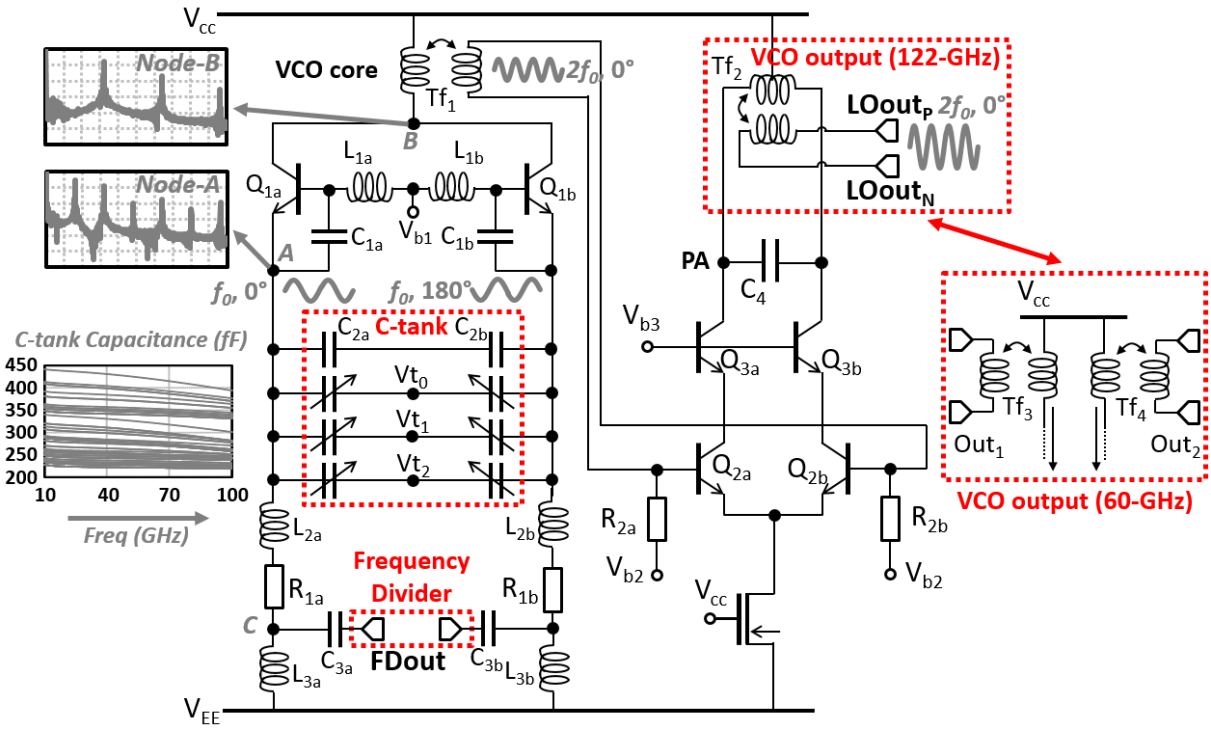

Figure 3.36: Schematic of 60 GHz VCO integrated to a PA and a Frequency Divider.

Such topology is quite advantageous compared to a classical VCO operating exactly at the desired frequency since it allows obtaining much lower phase noise and easy implementation at lower frequency. The signals with f_o frequency at transistor base terminals are added at the common-mode *node-B*. As a result, while the odd-order harmonics are cancelled out in theory thanks to being complementary in phase (or suppressed greatly in practice due to unavoidable non-symmetry in layout), the even-order harmonics are added together, hence generating the desired $2f_o$ signal. The frequency tuning mechanism in 60-GHz TRx is introduced through three variable capacitors (four variable capacitors implemented in 122-GHz) whose capacitance values could be adjusted in an analogue manner separately (in the range of 220 fF to 420 fF at 60 GHz) with the applied voltages in the 0 V – 3.3 V range so that the frequency resonance of LC-tank circuit is changing. Different sizing of these capacitors lead to different frequency tuning slopes. The push-push structure is single-ended by nature, thus transformer Tf_1 is integrated to provide an inductive load increasing the gain and to attain differential signal from the coupled inductor at the same time. The degeneration inductors L_2 and L_3 placed at the emitter terminals of Q_1 transistor pair are for noise reduction at f_o and $2f_o$ while maintaining the matching at point where the differential frequency divider is coupled out through series capacitors C_3. To reach lower phase noise, it is very

important to implement high-Q inductors in the tank circuit, so wider transmission lines are utilized with a proper layout to minimize the parasitic capacitances as well (see Figure 3.37).

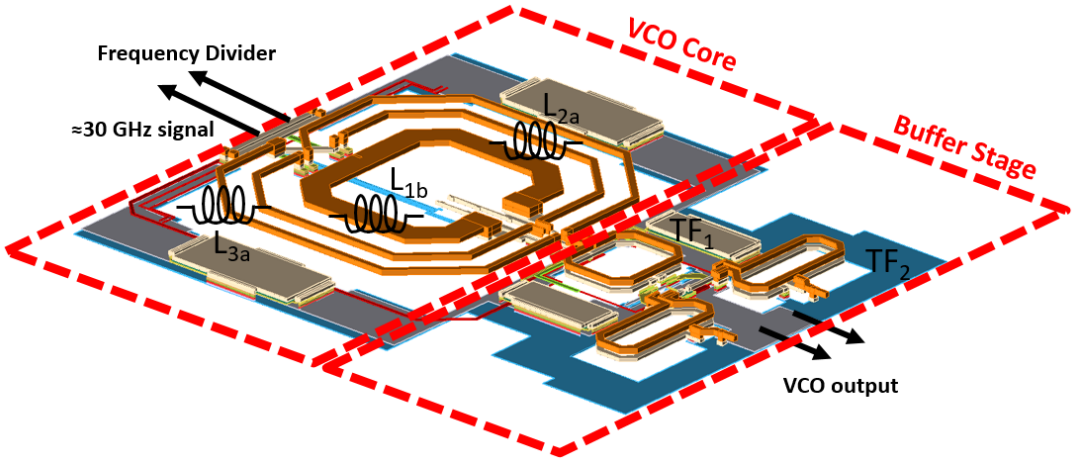

Figure 3.37: Layout of 60 GHz VCO integrated to the single-stage buffer PA.

The second harmonic is then amplified with the help of a PA which is acting as a filter for all the other harmonics at the same time. The PA is a single-stage cascode amplifier with an inductive load as seen in Figure 3.36. For wider operation bandwidth, the output is obtained after a transformer, Tf_2. In 122-GHz TRx versions, only one differential LO output is gathered whereas the 60-GHz TRM employs two transformers, Tf_3 and Tf_4, to achieve two differential outputs for further internal use based on the desired TRx architecture. This amplifier also serves as a buffer and guarantee high isolation with the latter stages. In 60-GHz TR2 TRx, these outputs are changed to provide a single output by reducing one of the transformers which is directed into a three-way Wilkinson power divider discussed in Section 3.3 to feed all the three channels.

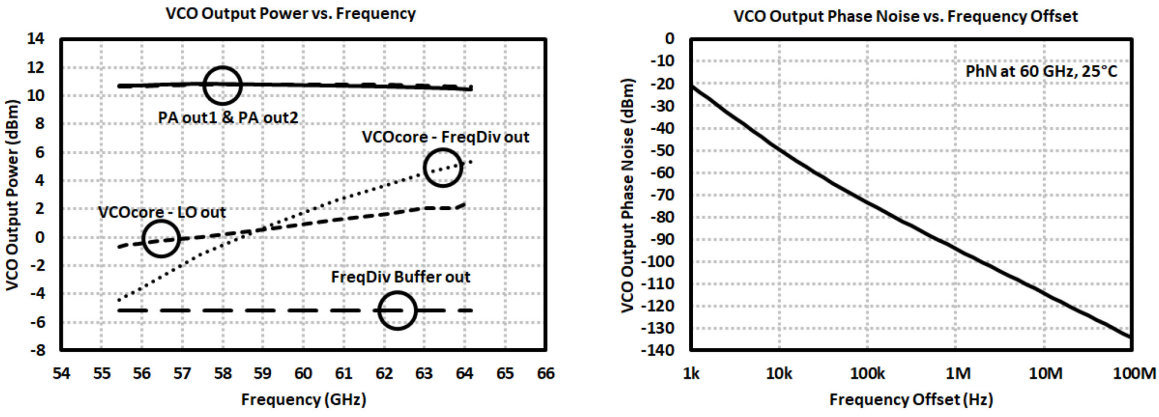

Figure 3.38: 60 GHz VCO, (*Left*) power levels: PA out1 / out2 output power, frequency divider and PA input power delivered from VCO core, frequency divider buffer output power, (*Right*) phase noise at 60 GHz.

The VCO core consumes only about 9.3 mA current at 3.3 V while the frequency divider and the single-stage PA to boost the delivered output power drain 18.8 mA and 35.7 mA respectively,

where the simulation results are illustrated in Figure 3.38 and Figure 3.39. The tuned nature of PA with inductive load also helps suppressing the higher-order harmonics. The core generates 1 dBm of average output power within the operation frequency of 55.44 – 64.15 GHz which is defined by the tuned control voltages of capacitor tank network and results in an operation bandwidth of 8.71 GHz in simulations. The PA has a P_{sat} of 10.7 dBm with an IP_{1dB} of -6 dBm at 60 GHz. Thus the expected LO output power from each of the two matched output ports becomes 10.7 dBm with a full differential voltage swing of about 3 V_{pp}. Such output power is simulated at the inputs of PA and quadrature signal generator of Rx channel including the connecting transmission lines. At the frequency divider input, the VCO could generate 30 GHz fundamental signal with an average 1 dBm power. The simulated phase noise of the VCO core is -73.5 / -94.2 / -114.3 dBc/Hz at 0.1 / 1 / 10 MHz offset respectively. The input power to the frequency divider is in average 1 dBm which is already much higher than its sensitivity. Moreover the phase noise at the output of frequency divider is by nature -118.2 dBc/Hz at 1 MHz offset, which is 6 dB less than the phase noise of VCO core for each division stage (four divide-by-2 circuits cascaded, which translates into 24 dB phase noise improvement). The output voltage spectrum with respect to swept frequency tuning voltages at *node-A* of VCO core and *LOout* of PA including the harmonics are shown in Figure 3.39, which emphasize the suppression of odd-order harmonics at the common mode node and after respectively.

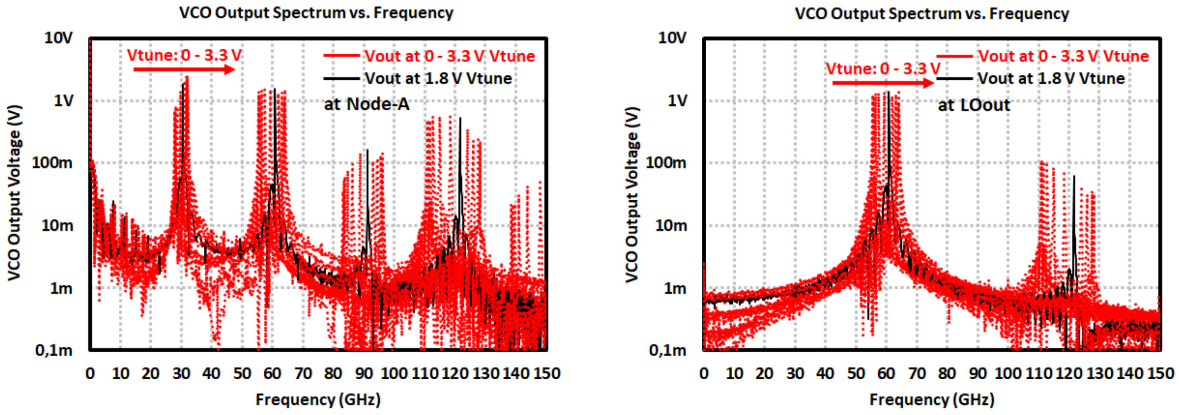

Figure 3.39: 60 GHz VCO output voltage spectrum, (*Left*) at node-A, emitter terminal, (*Right*) at *LOout* of PA.

On the other hand, the 122-GHz version that is designed with the same steps, but minor modifications in matching networks, achieves similar performance metrics with a total current consumption of 77.4 mA at 3.3 V (including VCO core, PA and divide-by-32 frequency divider). Its single differential output could provide an average LO signal around 9.05 dBm over the frequency range of 127.7 – 136.9 GHz with a simulated phase noise of -95.5 dBc/Hz at 1 MHz offset. It is worth to mention that both of the simulated frequency responses belonging to 60- and 122-GHz VCOs are optimized through analyzing various measurement results of successive chip fabrications due to either wrong modelling of devices or neglected layout segments. Thus, especially for the

122-GHz VCO, the higher operation band in simulations is actually observed to be functioning in the 10 GHz lower frequency band, hence covering the targeted ISM band, which is mentioned in Section 4.4 and Section 4.2 in detail. In 122-GHz TRM, the single LO output is directed to PA and Rx through a two-way power divider whereas the TR2 TRx having three channels incorporates a three-way power divider as in its 60-GHz counterpart.

The 60-GHz MIMO chip employs 20 GHz Colpitts oscillator (without the push-push architecture, not to enlarge the chip area further due to large LC-tank inductor size that should have been realized at 10 GHz otherwise) integrating a divide-by-4 frequency divider and a PA. So the 20 GHz core output signal is divided into two to feed both the PA and the frequency divider with a simple current combining technique. By this way, emitter terminals of the Q1 transistors (*node-C* in Figure 3.36) provide the VCO core output, where the common-mode *node-B* is directly dragged to supply. It achieves quite similar results in terms of output power and phase noise which is about -88.6 dBc/Hz at 1 MHz offset. At the frequency divider output after two consecutive divide-by-2 blocks, the phase noise would be -96.6 dBc/Hz at 1 MHz offset. The 60 GHz signal is later reached with the help of a frequency tripler which is discussed in Section 3.5.4. The output power after a single-stage PA going in multiplexer, and then tripler, is 12.1 – 13.22 dBm in the operation range of 21.11 – 24.37 GHz at room temperature with a total current consumption of 61.4 mA at 3.3 V (including VCO core, PA, divide-by-4 frequency divider). As mentioned previously, the operation frequency is intentionally kept higher in simulations while expecting lower operation frequencies from the fabricated chip.

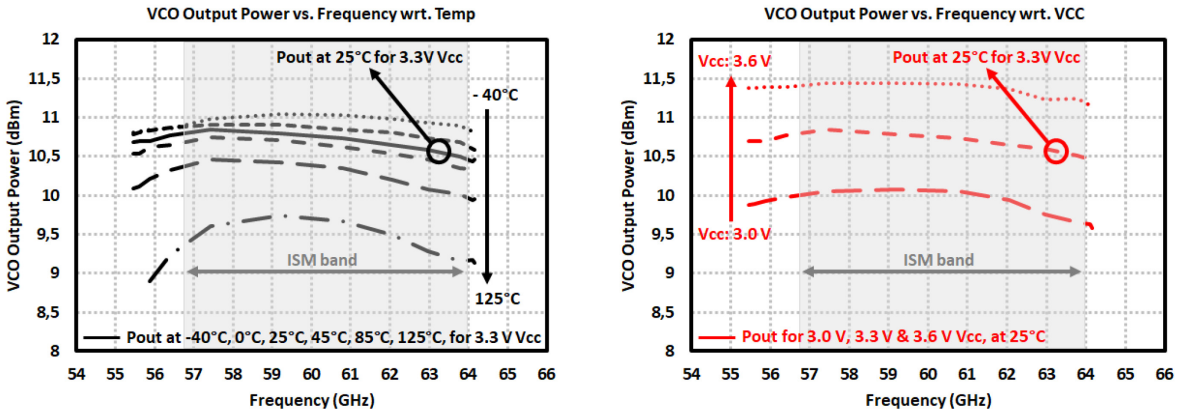

Figure 3.40: 60 GHz VCO output power with respect to swept tuning voltages for different (*Left*) operation temperature and (*Right*) supply pushing / pulling.

The complete VCO should as well withstand the changes in output power and corresponding frequency behavior with respect to temperature. In case of a reduced output power, the mixers in down-converter might not function whereas the transmitted output power to the antenna would drop drastically. On the other hand, the frequency divider might not be driven with such low level of coupled output power, hence not enabling the frequency division properly. The Tx frequency could be shifted as well which results in either reduced bandwidth or a complete out-of-band

operation considering the allowed ISM bands. Therefore a careful simulation flow is considered to characterize the circuit performance with respect to temperature changes. With the same logic, the circuit should also maintain its overall performance with voltage pulling / pushing cases. Because if the supply voltage is applied different than the specified 3.3 V (i.e. a voltage drop on board at this supply node), the VCO biasing scheme is affected which would definitely result in previously mentioned failures.

Such simulations are also performed and the results are shown in Figure 3.40 and Figure 3.41. According to simulated results, the VCO output frequency shifts about ±400 MHz for operation temperature change within -40°C to 85°C at the tuning edges (not in the middle tuning range). Additionally the delivered output power varies less than ±0.4 dB in order for 60-GHz while it is a bit higher for 122-GHz VCOs which is about ±2.1 dB. Phase noise performance at the center frequencies is degraded with respect to increasing temperature while the current consumption changes just by around ±2.4 mA at high temperatures for both versions. Finally under 300 mV voltage pulling / pushing conditions, the frequency shift and gain variation stays in ±40 MHz and ±0.8 dB respectively, which is negligible.

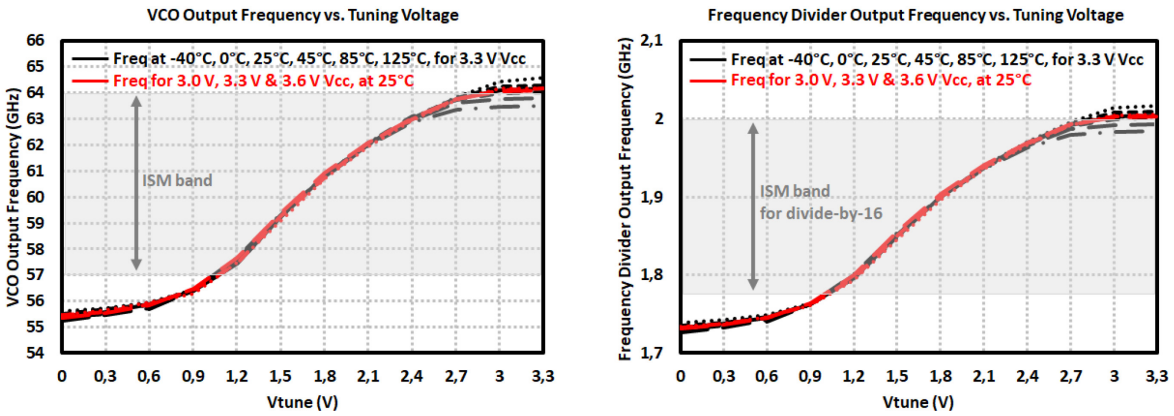

Figure 3.41: 60 GHz VCO with respect to swept tuning voltages for different operation temperature and supply pushing / pulling, (*Left*) LO output frequency, (*Right*) frequency divider output frequency.

3.5.2 Frequency Divider Design

A frequency divider with a division ratio of 16 is integrated at the 60 GHz VCO core (divide-by-32 and divide-by-4 blocks are used respectively in 122 GHz and 20 GHz VCOs) using another transformer coupler. As displayed in Figure 3.42, each division block is of a static divide-by-2 frequency divider which are based on differential D-Flip-Flop (DFF) emitter-coupled-logic (ECL) circuits and are formed by two current steering D-latches in master / slave configuration through a negative feedback loop, and a buffer to the next division stage. The clock inputs in DFFs (or VCO differential coupled output) are inversely inserted into each master and slave DFF. When

the clock input is set high, the transistor pairs Q_{2a} and Q_{2b} senses this input by allowing the current to flow through Q_{1a} within half the clock cycle. In the second half cycle, the output stores it along the Q_{2c}, Q_{2d} and Q_{1b} path and then inverts for the next clock period, as a result halving the clock frequency in the buffer outputs (Out_P, Out_N) for each divide-by-2 DFF. By cascading four as seen in the block diagram in Figure 3.43, the divider output could be adjusted to VCO operation frequency divided by 16, thus external PLL referenced to the divider output frequency is employed to stabilize the free-running VCO through controlling its frequency tuning inputs attached to VCO core varactors.

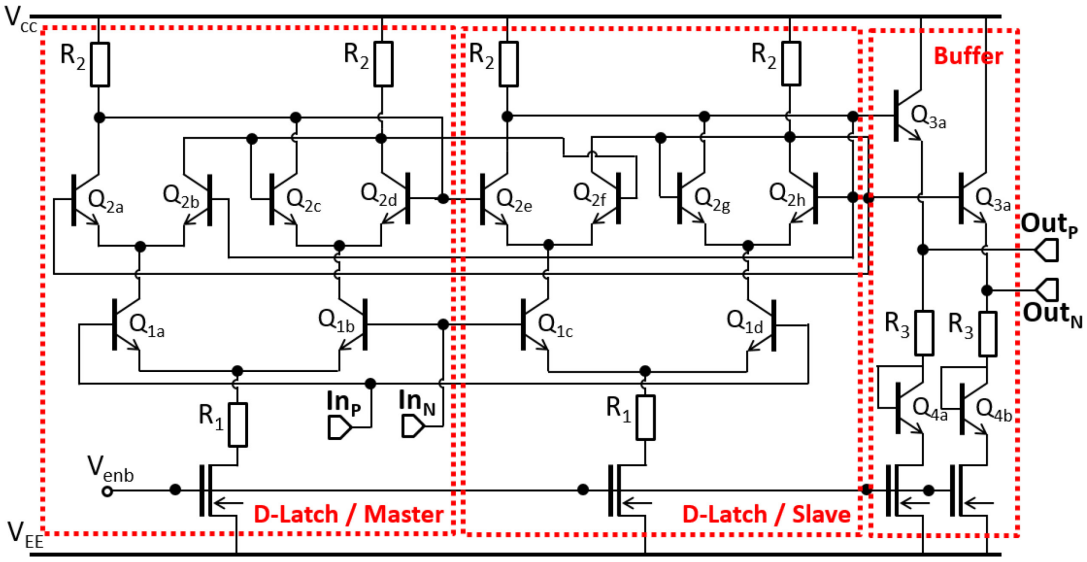

Figure 3.42: Schematic of Divide-by-2 circuit composed of two D-latches and a buffer.

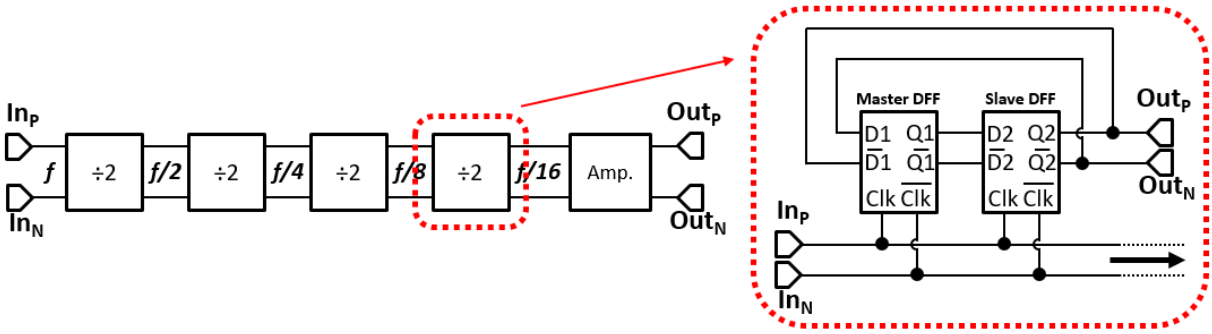

Figure 3.43: Block diagram of the divide-by-16 frequency divider and its divide-by-2 master / slave DFF sub-block.

The operation frequency of each block is controlled by adjusting the resistors, where rest of the circuitry is identical with the succeeding stages. To guarantee high speed operation, the transistors with minimum sizes are employed hence lower power consumption is maintained. At the output of final frequency divider, an additional single-stage resistive-load differential amplifier is placed

to increase the isolation level, reduce the loading on divider core, set the DC offset and provide a low impedance at the output to ease PLL driving.

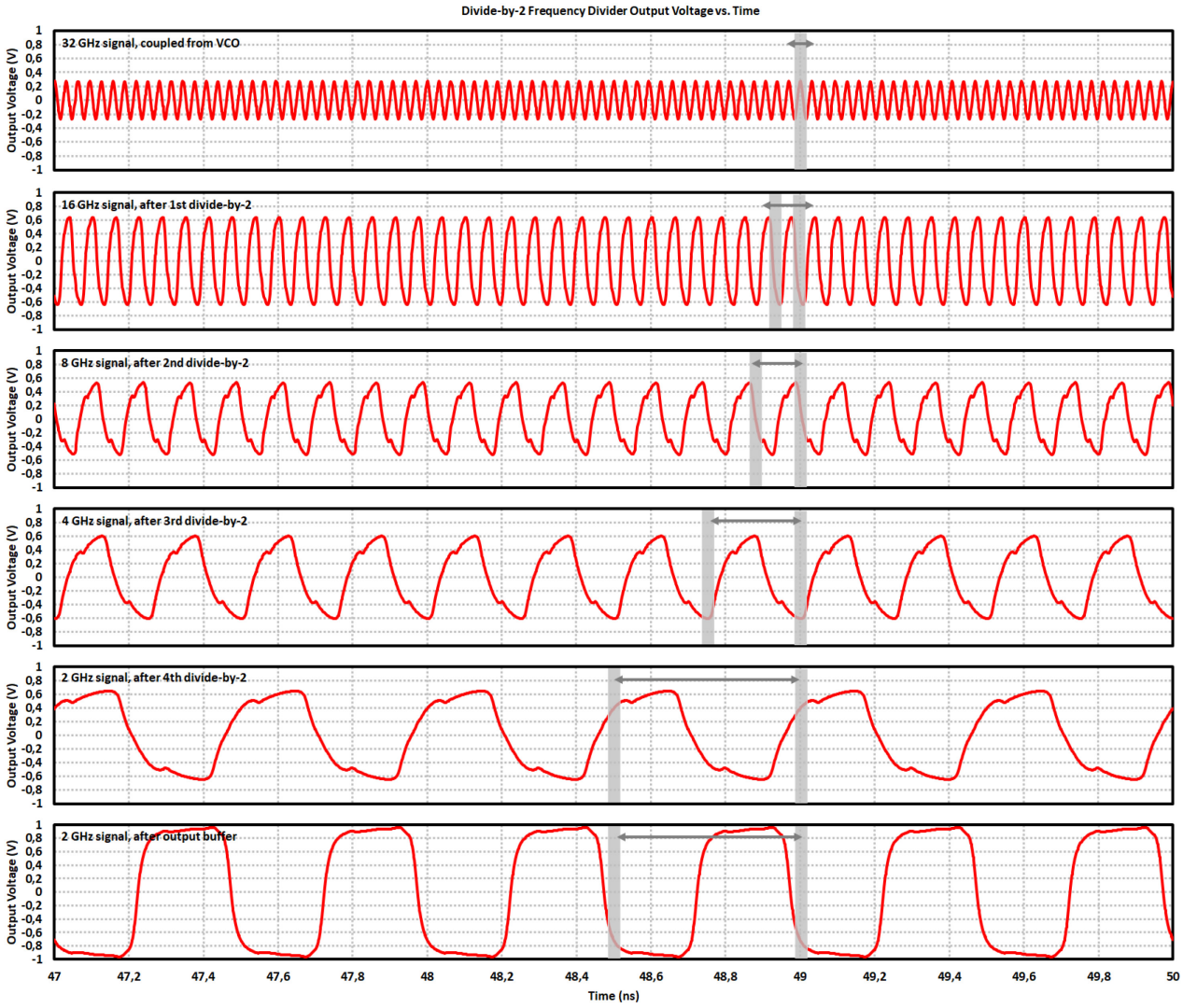

Figure 3.44: Divide-by-16 frequency divider output voltage at each divide-by-2 output node.

The maximum operation frequency of each DFF is determined by the parasitic capacitances of transistors, interconnects between these and the resistor values, which contribute to total time constant in the end such that the DFF speed is reduced. Therefore careful layout work is carried out to minimize interconnects and reduce the propagation delay while keeping the differential circuit symmetry as much as possible. For each successive division stage, the transistor sizes are kept smallest in available technology, so does the parasitic capacitances, which requires peak sensitivity adjustment by increasing the RC time constant through larger load resistors. The simulations are realized by just using lumped elements excluding interconnects, which would surely result in more optimistic performance compared to the ones after final layout and fabrication process. In this context, a detailed simulation explaining the frequency division at each divide-by-2 stage

starting with a random input power at 32 GHz until the input of last stage buffer is stated in Figure 3.44.

The most important point to be considered in such frequency dividers is to guarantee enough voltage swing at the clock inputs (In_P, In_N), such that the divider is injection-locked to the VCO core frequency rather than its self-oscillation frequency which exists due to its ring-oscillator nature. Therefore sensitivity curves shown in Figure 3.45 should be plotted to check the maximum operation frequency with respect to applied input power. Moreover the frequency divider has a self-oscillation frequency of around 2.23 GHz at room temperature, so if the coupled output power from the VCO core could not generate the required power level to turn on the switching transistor pairs (Q_1 transistors) of each divider block, then the divider is locked to this self-oscillation frequency rather than the desired output frequency. This would easily make the full TRx fail functioning since the FMCW operation could not be realized due to the unstable frequency response of a free-running VCO which has to be fixed with the help of a PLL. Considering all of these, the divider should also withstand the supply voltage pulling / pushing and industrial temperature conditions to take the reduced output power fashion of VCO in such cases into account.

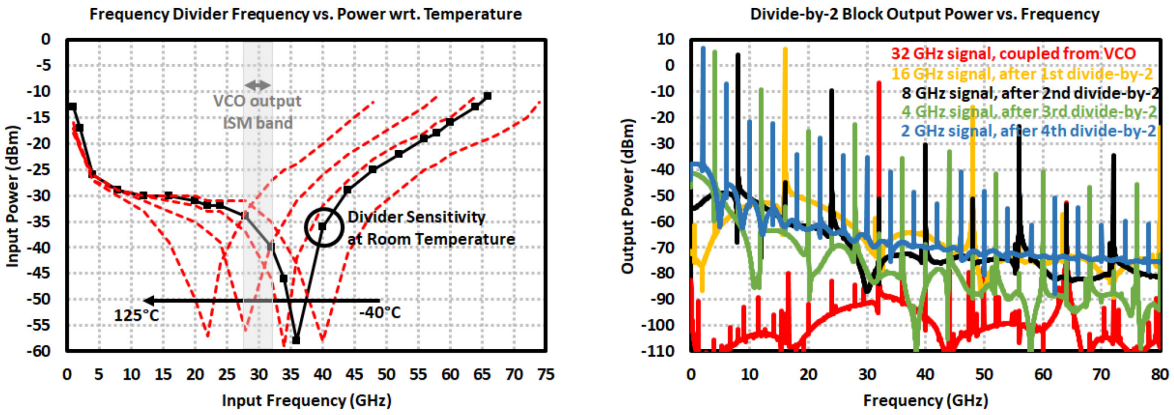

Figure 3.45: (*Left*) Divide-by-16 frequency divider sensitivity measure with respect to temperature, (*Right*) Divide-by-2 frequency divider block output power spectrum at each division stage.

According to simulation results, the frequency divider would provide a differential output signal within 1.75 – 2.03 GHz band. The simulated sensitivity is kept below -30 dBm between 12 – 43 GHz with the peak observed at 36 GHz at room temperature. As the temperature increases, the sensitivity curve starts drifting apart from the designed center frequency which could not create a crucial issue thanks to high sensitivity. As discussed previously, the addition of parasitic components and interconnects would change the sensitivity behavior, yet resulting in a safe operation. Finally the power consumption of the frequency divider chain is 62 mW at 3.3 V single supply. Similar performance metrics except power consumption are expected naturally in all the frequency dividers of 20-, 60-, 122-GHz circuits since the blocks are completely the same.

3.5.3 Multiplexer / LO Switch Design

Multiplexer is only used right after the PA output of 20-GHz VCO in 60-GHz MIMO TRx where the aim is to switch between this internal VCO and external LO signals to use *master / slave* configurations for cascading multiple chips. The switched signal is then sent to both frequency tripler and LO output pin for other *slave* chips. The circuit schematic and layout are visualized in Figure 3.46.

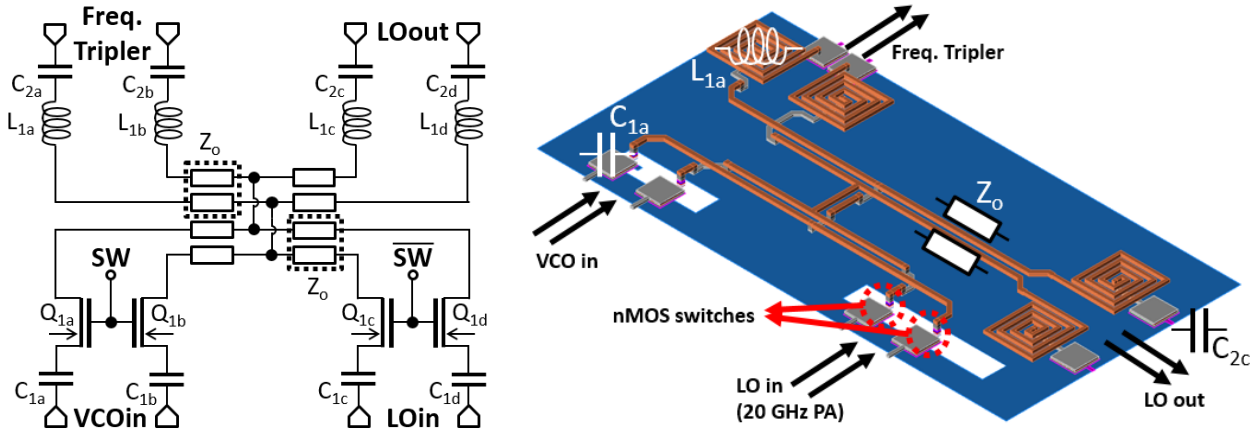

Figure 3.46: Schematic and layout of 20-GHz differential multiplexer.

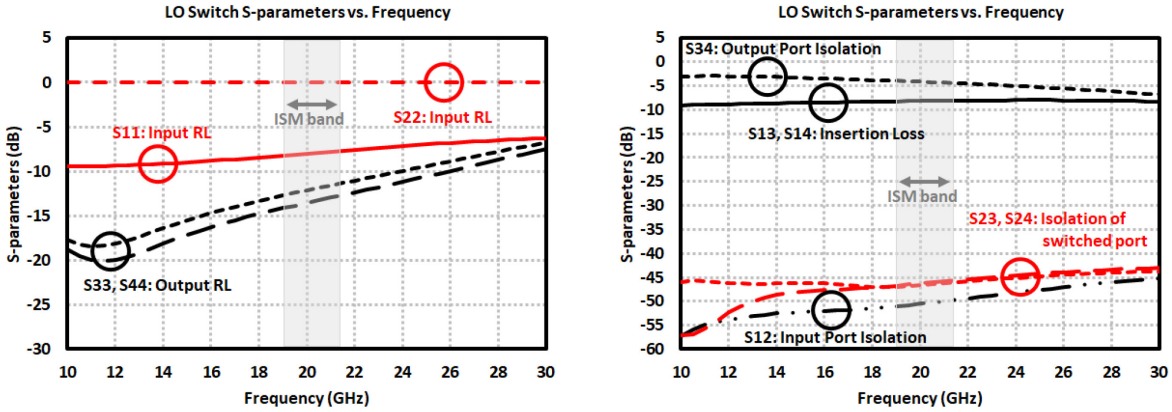

Figure 3.47: Simulation results of 20-GHz differential multiplexer.

This differential multiplexer consists of nMOS transistors as switches whose gate terminals are controlled by CMOS inverters to guarantee *on* or *off* operation for each branch when logic high or low is applied. By default internal VCO path is turned *on* where the external signal path is set to *off* mode combining both the relative MOS switch transistor and 20-GHz PA at this LO input pin. Other than that, the structure acts as an input-switched back-to-back passive power divider. As shown in the layout, area conserving spiral inductors of 375 pH with series capacitors of 1 pF to block the DC at the outputs are used to match to 100 Ω differential impedance. Since the structure

is of a power divider, upon its theoretical loss of 3 dB, losses of transmission lines which are held shorter compared to classical $\lambda/4$ length lines not to increase the area (105 Ω lines with 22° electrical length), matching inductors and the switch transistors are accumulated, which increase the overall insertion loss, hence reducing the delivered power going in both the frequency tripler and *LOout* pad. This power loss is already compensated by latter amplification stages after the frequency tripler, yet the design could well be improved with the main focus on reduction of the switch insertion loss.

The simulation results are shared in Figure 3.47. According to these, outputs are well matched to differential 100 Ω with input return loss of about -8 dB and an average insertion loss of 8.2 dB within 18 – 30 GHz frequency band. The complete isolation of the *off*-path is guaranteed not only by the above 45 dB insertion loss / isolation of this second input in *off*-mode, but also by the switched off 20-GHz input PA which is already not functioning at the same time. In the other case where the LO path is *off*, the generated signal is attenuated by the same level, however the VCO also integrates a separate supply pin which is disabled in this *slave* mode, hence not only improving the isolation, but also lowering to the power consumption as well.

3.5.4 Frequency Tripler Design

The MIMO chip requires a fundamental 20-GHz VCO for cascading multiples of it in order to realize massive MIMO chains, as illustrated in Figure 2.7, which the targeted operation band is around 60 GHz frequency. Therefore a frequency tripler circuit is implemented such that the structure consists of a tripler core and a single-stage power amplifier which is then followed by an additional two-stage PA, as mentioned in Section 3.4, to boost the delivered output power that is to be lost in bulky power division networks.

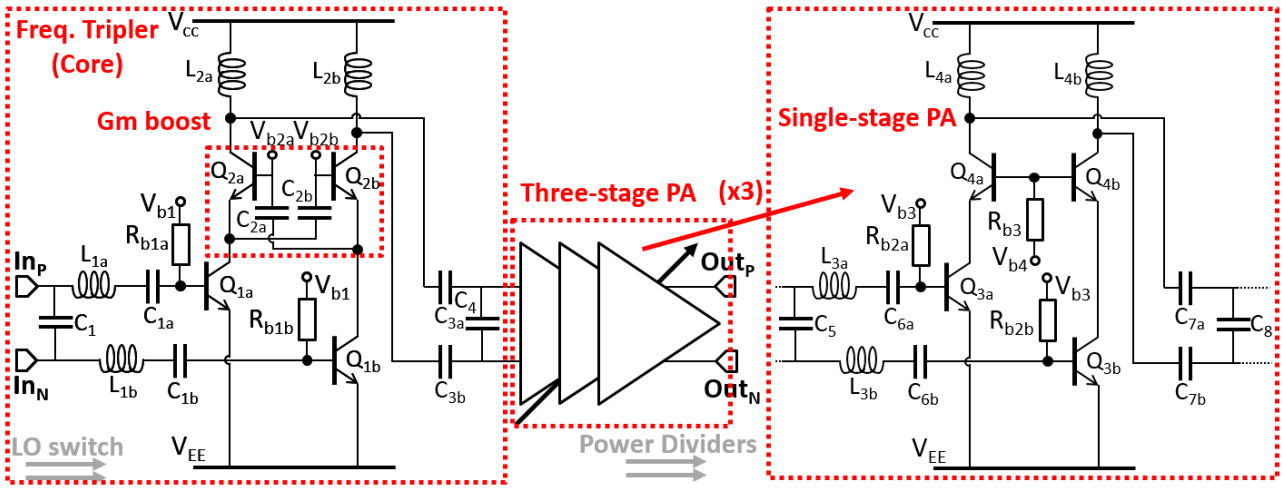

Figure 3.48: Schematic of 60-GHz frequency tripler.

The differential tripler is based on a harmonic generating transistor core in which the 20 GHz signal and its harmonics are amplified through regular transconductance pairs biased at class-A mode. While even-order harmonics are already suppressed greatly by the circuit nature even considering the non-fully-symmetrical layout, the odd-order harmonics are suppressed by the succeeding 60 GHz amplifier which acts as a filter to 20 GHz fundamental frequency (f_0) and other higher order harmonics which clears the output spectrum by leaving just the 60-GHz component.

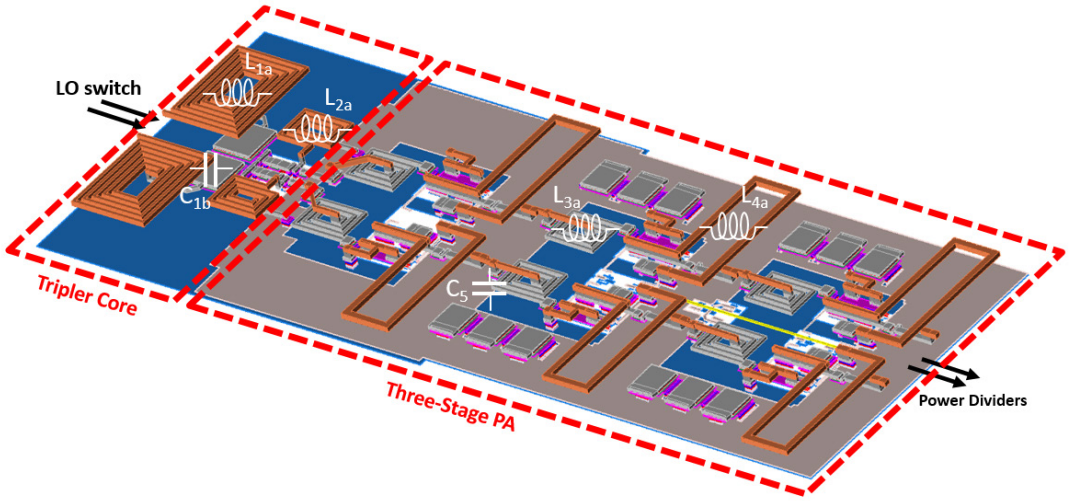

Figure 3.49: Layout of 60-GHz frequency tripler.

The circuit schematic and layout are shown in Figure 3.48 and Figure 3.49 respectively. Input stage is matched at 20 GHz using a spiral inductor of 1.1 nH (L_1), a parallel 100 fF capacitor (C_1) and a DC blocking 1 pF capacitor (C_2). At the collector terminals of Q_1 pair, all the harmonics of f_0 exist thanks to non-linear behavior of transistors with proper biasing. The following capacitive-cross-coupled common-base Q_2 transistor pair are placed to benefit the Gm-boosting technique to further amplify the harmonics. In this case, the input signal after Q_1 pair is amplified by the factor of $(1 + C_3 / (C_3 + C_{be}))$ which approaches to 2 since $C_1 >> C_{be}$, where the second capacitive ratio term is called inverting amplification ratio. Normally at the collector terminals of Q_1 pair, some notch filter structures based on $\lambda/4$ transmission lines are placed to filter out the fundamental f_0 signal. However in this design, such area consuming matching network structure is not adopted because of the already required multi-stage PA acting as a filter to other harmonics as well. The inter-stage matching between the tripler core and amplifier is of a regular LC-type network matched at 60 GHz using 167 pH of L_2, 30 fF of C_4 and 110 fF of C_5 with tuned inductive peaking method such that f_0 and higher order components are already suppressed before the main amplification stage. The output is then differentially obtained after series capacitors (C_4) right at the collector nodes of Q_2 pair.

A 60 GHz single-stage cascode amplifier further improves the delivered output power while maintaining high linearity. This element has 17 dBm P_{sat} with 5 dBm IP_{1dB} and a PAE of 18.9 %. It drains 50.1 mA at 3.3 V in the high gain mode, has a gain of 10.6 dB in its linear region and

possesses a 3-dB gain bandwidth of 27.5 GHz in the range of 46 – 73.5 GHz. Having full LO chain simulations completed, it is observed that the output power might not be enough due to the excessive damping in power division network. For that reason, the main two-stage cascode PA in Tx section is also integrated before this power division stage, which a detailed analysis regarding to PA design is already presented in Section 3.4. Gain control and enable pins are implemented on the bias section by cascaded pMOS transistor bank each attached to different resistors at their drain terminals, which provide four bit gain tuning mechanism mainly by controlling the current in the amplification stage by switching between these. Hence depending on the end-application requirements, the output power could be adjusted and total power consumption is reduced, which relaxes the package heat dissipation issue.

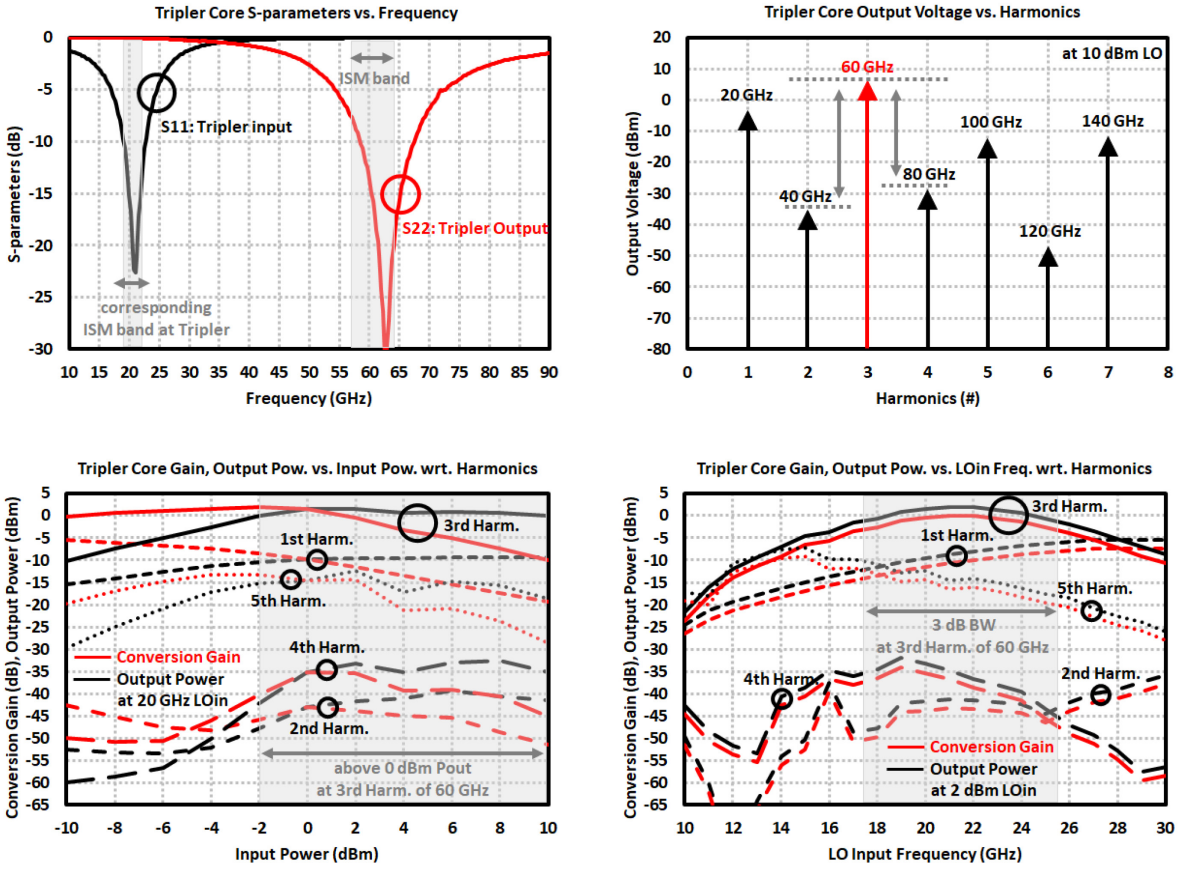

Figure 3.50: Simulation results of frequency tripler core. (*top left*) S-parameters, (*top right*) harmonics at 10 dBm LO input at 20 GHz, (*bottom left*) conversion gain and output power with respect to input power for harmonics of 20 GHz LO input, (*bottom right*) conversion gain and output power with respect to LO input frequency for harmonics of 2 dBm 20 GHz LO input.

Simulation results of the tripler core is shown in Figure 3.50. Input and output return losses are quite well matched at the frequency band of interest. The tripler core gives an output power of 1.5 dBm at the 3rd harmonic of 60 GHz with 2 dBm of 20 GHz LO input signal. At this input power level, it achieves its maximum output power, however supplies with more than 0 dBm

output power beyond -2 dBm input power. The 3-dB operation bandwidth is found to be 7.8 GHz in the range of 17.5 – 25.3 GHz. Such range well covers the internal VCO operation band and expands beyond to enhance the TRx bandwidth from external LO, which results in a total bandwidth of 23.4 GHz between 52.5 – 75.9 GHz at its 3rd harmonic. Within the 3-dB bandwidth, maximum conversion gain is found as almost 0 dB at 21.5 GHz. As seen from the figures, the even-order harmonics are suppressed well below -30 dBm whereas the output inductive load degrades the 1st and 5th harmonics more than 10 dB as well. The odd-order harmonic suppression is further improved with the single-stage PA. Current consumption of this block is only 8.2 mA at 3.3 V. Finally, with respect to temperature variations considering the industrial operation range, it becomes more robust with 0 dBm to 6 dBm of LO input power at 20 GHz such that the output power change is only about 1 dB (see Figure 3.53).

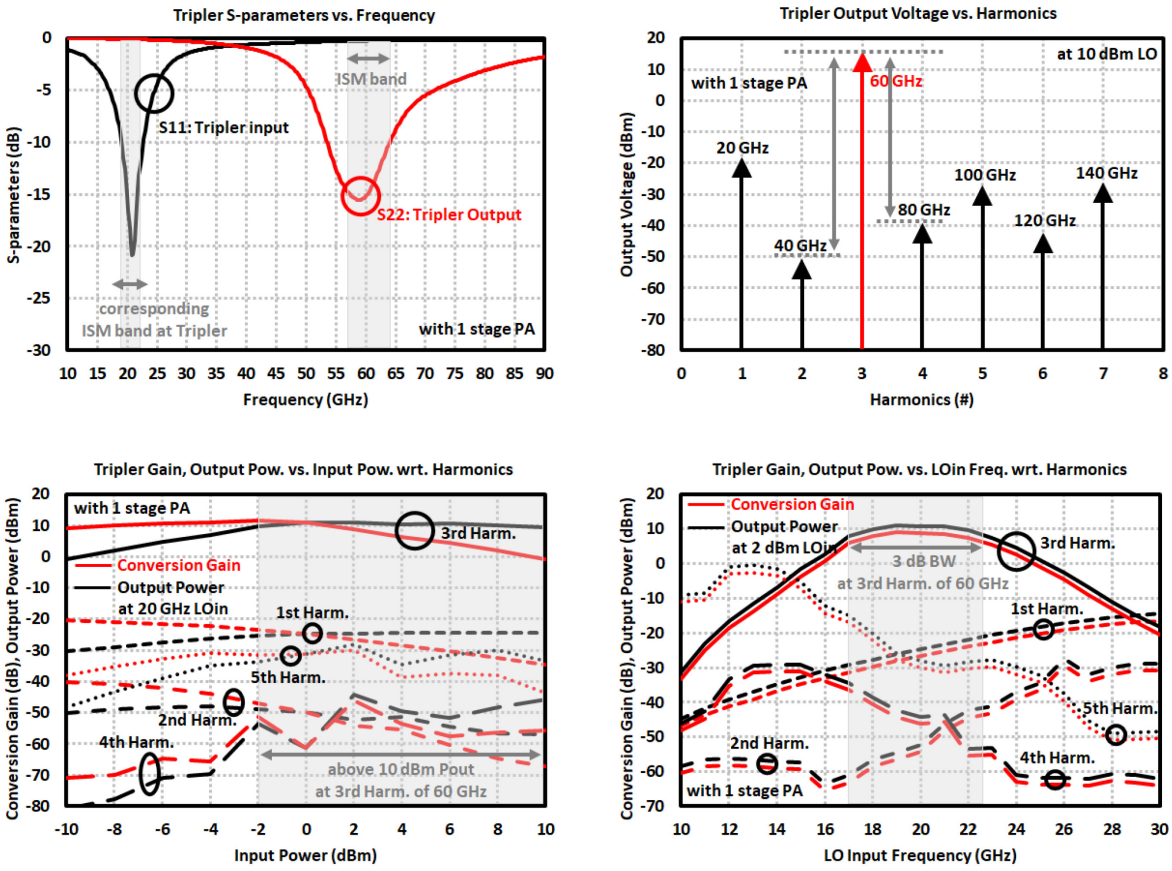

Figure 3.51: Simulation results of frequency tripler including a single-stage PA. (*top left*) S-parameters, (*top right*) harmonics at 10 dBm LO input at 20 GHz, (*bottom left*) conversion gain and output power with respect to input power for harmonics of 20 GHz LO input, (*bottom right*) conversion gain and output power with respect to LO input frequency for harmonics of 2 dBm 20 GHz LO input.

After single-stage amplification whose results are shown in Figure 3.51, the delivered output power becomes 10.8 dBm at 2 dBm of LO. The 3-dB bandwidth is simulated as 5.5 GHz between 17 – 22.5 GHz which translates into an operation at the 3rd order harmonic between 51 – 67.5

GHz. On the other hand conversion gain is around 8.8 dB with maximum observed at 19 GHz. The harmonics are further suppressed, since it acts as a tuned amplifier at the center frequency of 60 GHz. Even-order harmonics level are below -45 dBm while the odd-order harmonics are suppressed below -25 dBm within the specified frequency band.

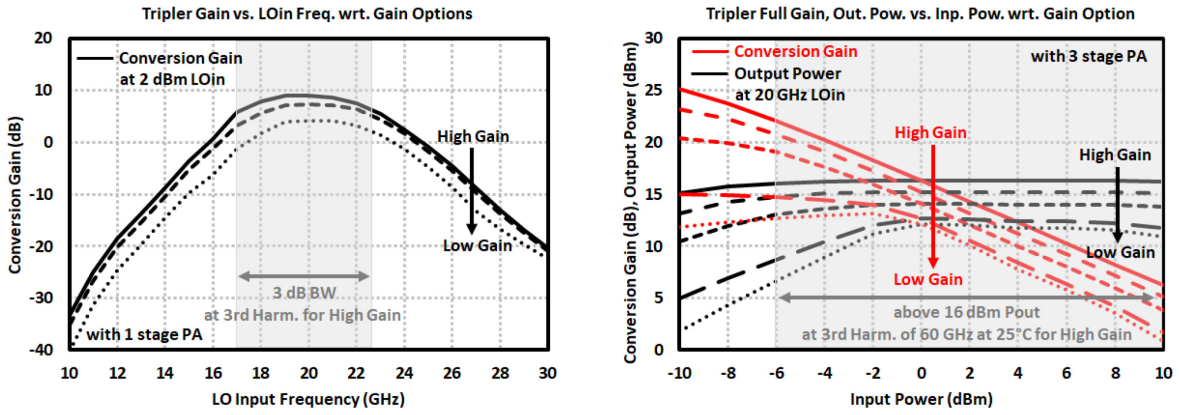

Figure 3.52: Simulation results of frequency tripler including a single-stage PA. Conversion gain and output power with respect to input power for the 3rd harmonic of 20 GHz LO input at different temperatures.

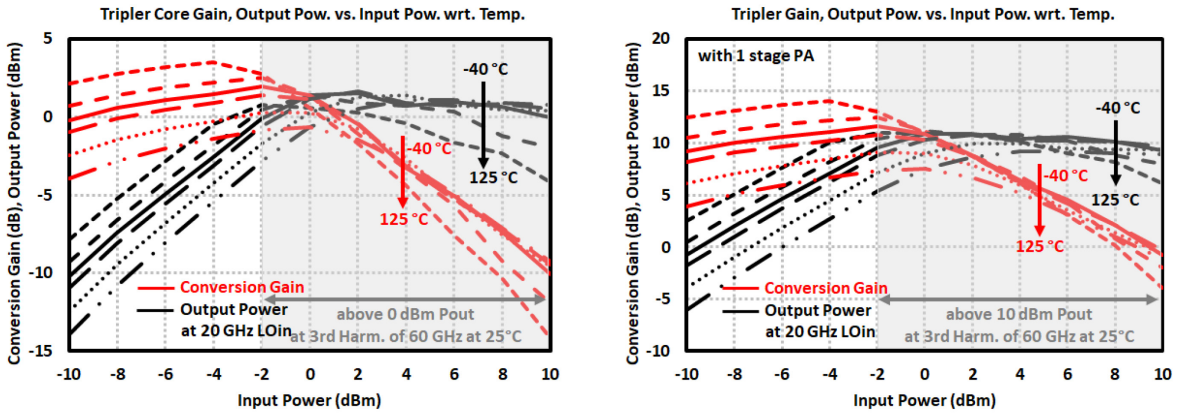

Figure 3.53: Conversion gain and output power with respect to input power for the 3rd harmonic of 20 GHz LO input at different temperatures for (*left*) tripler core, (*right*) tripler with single-stage PA.

In Figure 3.52 and Figure 3.53, the effect of temperature and different gain options on conversion gain and output power are depicted. According to these, same behavior of tripler core for temperature is observed. Additionally, there are three gain options which could be used to adjust the conversion gain and output power by about 5 dB depending on the application requirements such that the current consumption might be reduced to 15.4 mA in low gain mode from 55.2 mA in high gain mode.

Furthermore with the integration of latter two-stage PA coming with its two separate gain control pins, which is discussed in Section 3.4, 16.2 dBm at 60 GHz is obtained at the expense of

a current consumption of 122 mA at 3.3 V with all the gain options set to maximum gain mode (see Figure 3.54). Such high output power is achievable in simulations for LO input power more than -4 dBm. With the tuning options adjusted to lower gain modes, 15.2 / 14.1 / 12.6 dBm output power are achievable at 60 GHz with current consumption of 80.7 / 56 / 32.7 mA. The 3-dB bandwidth improves to 7.9 GHz within 16.2 – 24.1 GHz.

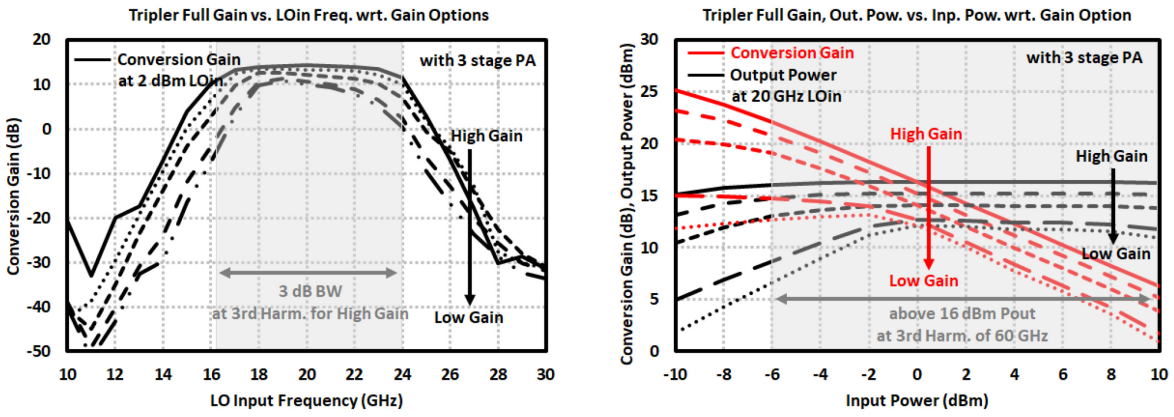

Figure 3.54: Simulation results of frequency tripler including the three-stage PA. Conversion gain and output power with respect to input power for the 3rd harmonic of 20 GHz LO input at different temperatures.

3.5.5 20-GHz PA Design

A 20-GHz single-stage differential PA is also implemented at the LO input stage before the other end of multiplexer for external LO operation (see Figure 3.55). Although the detailed study of PAs is given in Section 3.4, the simulation results of this block are provided here for complete LO chain simulations of the 60-GHz MIMO TRx. The same PA in tripler block is tuned to achieve around 20 GHz operation with main modifications focused at designs of input stage and load inductors of 570 pH (L_1) and 340 pH (L_2) in series with 1pF (C_1) and 150 fF (C_2) capacitors. According to simulation results shared in Figure 3.56, it achieves 17.1 dB gain at 20 GHz with a maximum gain of 17.6 dB centered at 18 GHz and has a 3-dB bandwidth of 9.5 GHz (14 – 23.5 GHz). With respect to temperature changes, gain varies by ±1.5 dB in its most active region. Input and output return losses are below -10 dB for the full band and P_{sat} is around 17 dBm with an IP_{1dB} of -5 dBm. The efficiency is simulated maximum 26 % at 3 dBm P_{in} with a drop down to 20 % after its saturation point at 10 dBm. However it could be deducted that the linear region (or the region where harmonics do not appear significantly) extends to LO input power around 1 dBm when only about 2 dB input compression is observed. The current consumption is simulated as 19.6 mA at 3.3 V supply. Finally, the output is controlled by an enable pin through the bias network which is connected to the multiplexer switch controls such that this block is disabled when not used.

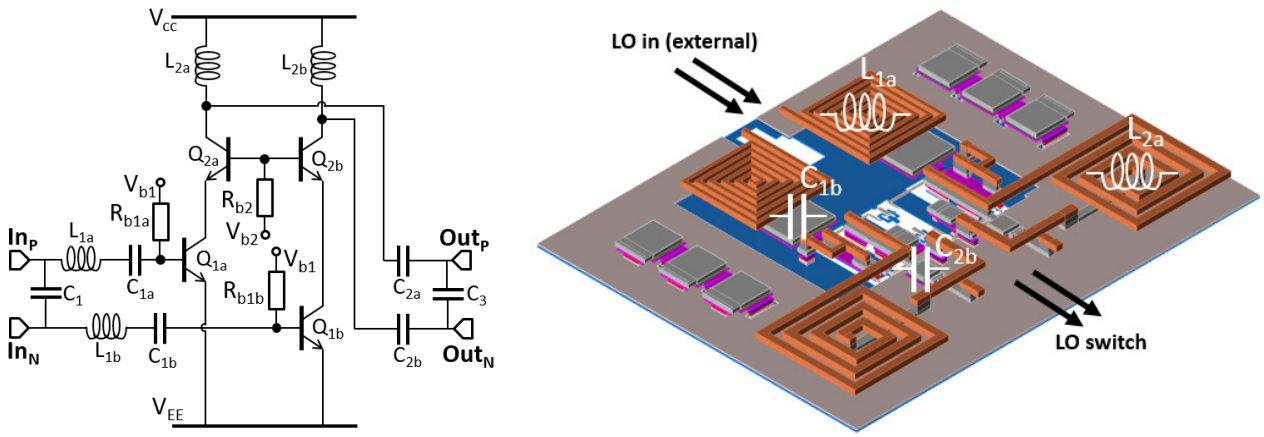

Figure 3.55: Schematic and layout of 20-GHz single-stage cascode PA.

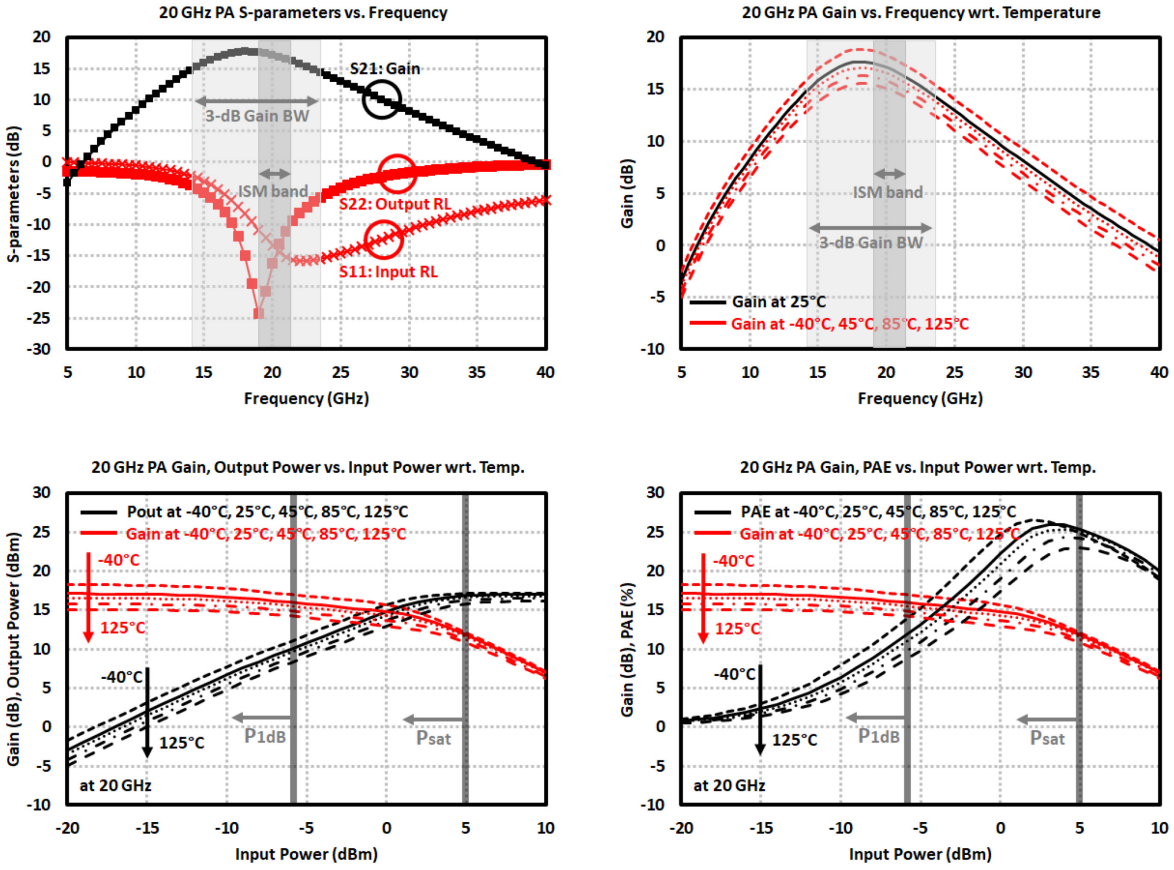

Figure 3.56: Simulation results of 20 GHz PA: (*top left*) S-parameters, (*top right*) gain with respect to temperature, (*bottom left*) gain and output power with respect to temperature, (*bottom right*) gain and PAE with respect to temperature.

3.5.6 Power Divider Design

The designed VCO is then followed by a two-way and a three-way Wilkinson power divider respectively in TRM and TR2 transceivers to feed the Rx and Tx. In addition to these, four-way power dividers attached to the outputs of a two-way power divider are employed after the frequency tripler stage in MIMO TRx in order to separate the LO signal into eight channels in total. Such passive LO signal distribution network has already been illustrated in Figure 3.35.

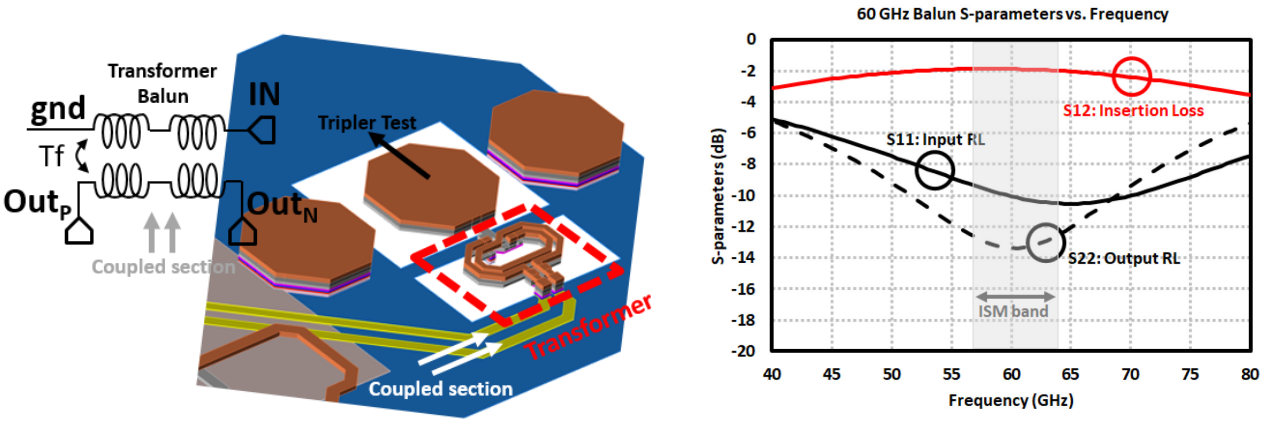

Figure 3.57: Layout and simulation results of 60-GHz balun in two-way power for frequency tripler.

The design of two-way version is already discussed previously in Section 3.3, where only minor modifications are realized on top to guarantee the required specifications in monostatic TRx. But one distinct feature integrated in the power division network after MIMO LO chain is the tripler output could be directly measured under probe setup with the realization of a coupled output at the two-way power divider which connects to a 60-GHz transformer coupled balun as well. The differential structure and corresponding simulation results together with the input pads are illustrated in Figure 3.57. According to results, the compact balun has an average insertion loss of 1.9 dB within ISM band where the return losses are better than -10 dB. Because of the main aim of just monitoring the tripler output with respect to LO frequency, achieving a high output power level is not important. Henceforth, rather than a three-way power divider which would increase the losses on all channels including the PA input power on the Tx path, a branch line coupler with a coupling loss of 23 dB is integrated on the Rx path so that power delivered to Tx is not affected while only 4.3 dB of loss in the power going in Rx channel is simulated at the center frequency of 60 GHz. In Figure 3.58 and Figure 3.59, the structure and simulation results of such power division network just before the four-way power dividers are shown. The frequency tripler output power measurement port has an insertion loss of 25.75 dB along the ISM band. Output port isolation is 16.8 dB with input and output return losses below -10 dB for the whole frequency band.

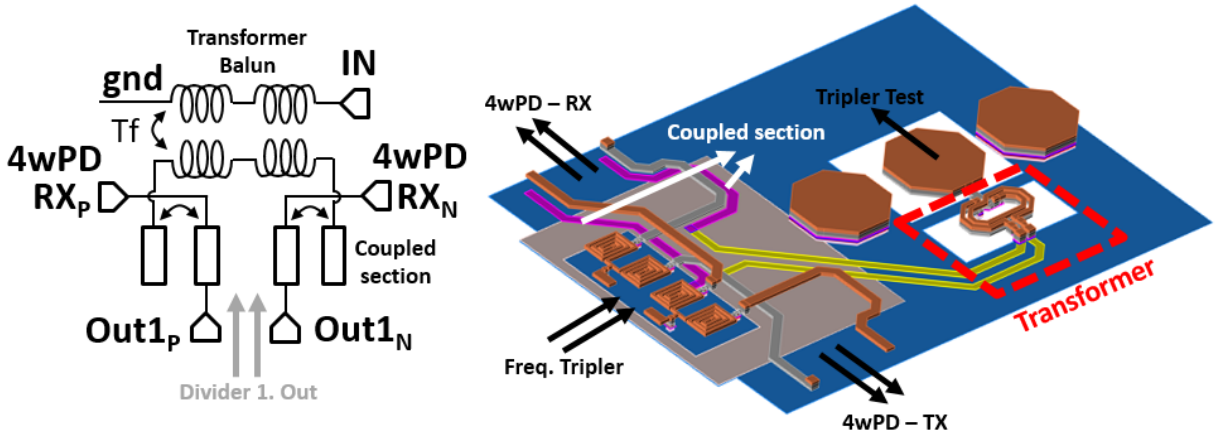

Figure 3.58: Schematic and layout of 60-GHz two-way power divider with a coupled output for frequency tripler.

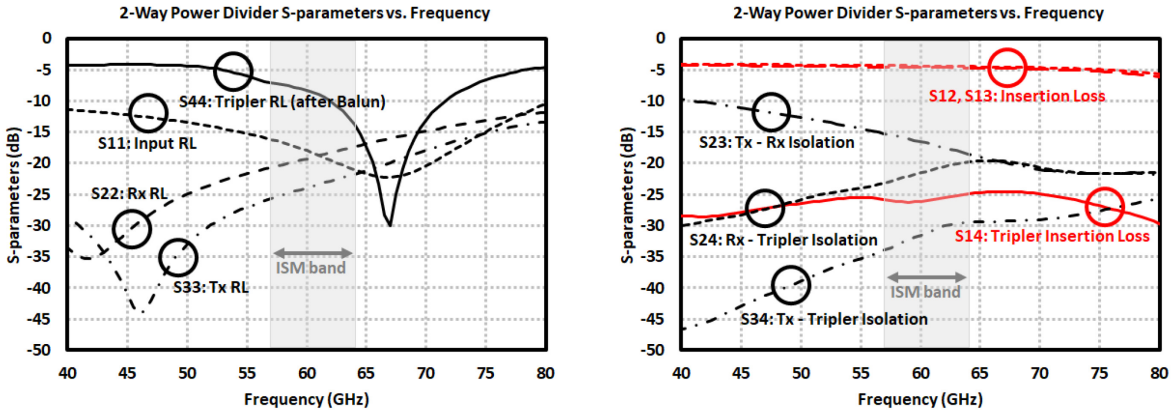

Figure 3.59: Simulation results of 60-GHz two-way power divider with a coupled output for frequency tripler.

The differential three-way power divider schematic and layout is shown in Figure 3.60. It is designed with the same Wilkinson power divider logic with transmission lines are matched to different characteristic impedances as required by the topology. While the input ports of three-way power divider are connected to a single stage PA after VCO in TR2, the two symmetric outputs connect to Rx channels and the other to Tx channel on the same side of chip with VCO. Such positioning of channels also facilitates the antenna design on board. As shown in Figure 3.61, the three-way architecture has an average insertion loss of 6.3 dB in the ISM band with all ports are matched to differential 100 Ω. In order to keep the structure compact, the transmission lines are meandered as a result it occupies only 300 µm x 500 µm area. The 122 GHz version, having same architecture and consuming much less die area, performs an insertion loss of 6.6 dB at 122 GHz with return losses above 10dB guaranteed in a frequency bandwidth of 50 GHz between 90 – 140 GHz (see Figure 3.62). The core power division network is designed with line widths of 2 µm, the thinnest allowed by technology, whereas the length is 540 µm satisfying $\lambda/4$ rule at 60 GHz.

The connecting transmission lines placed at the input and output ports have much lower impedances by using wider widths about 10 µm to facilitate the matching process. Additionally ports are well isolated with levels below -25 dB within the ISM band and beyond.

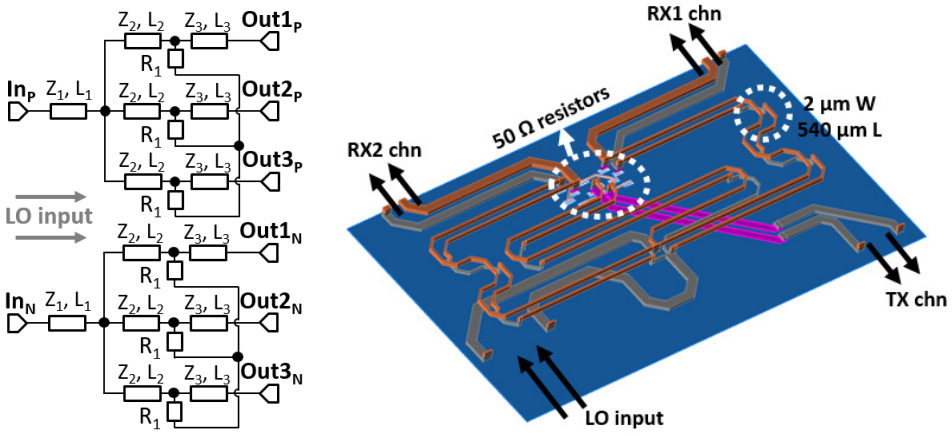

Figure 3.60: Schematic and layout of 60-GHz three-way power divider.

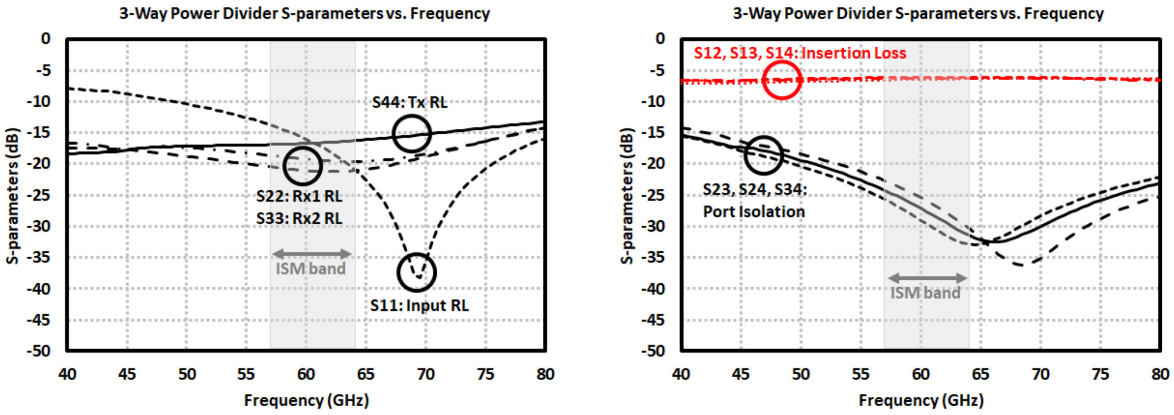

Figure 3.61: Simulation results of 60-GHz three-way power divider.

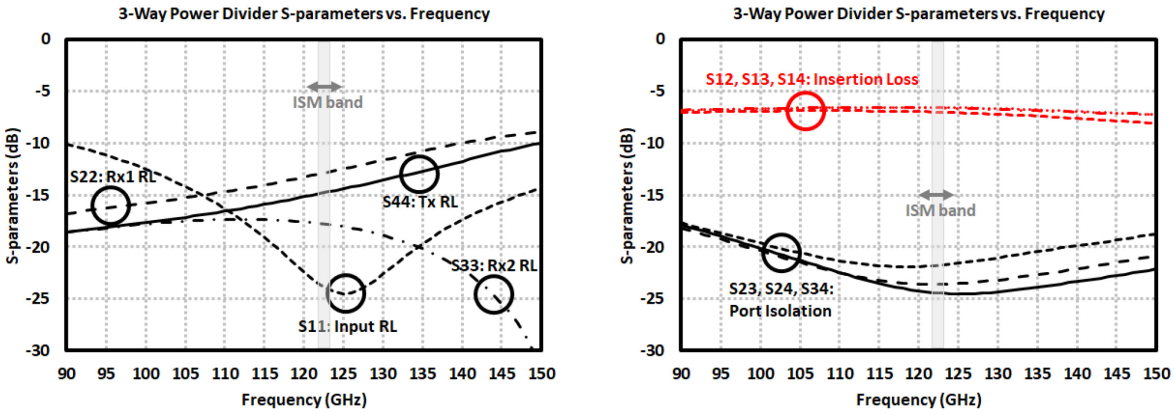

Figure 3.62: Simulation results of 122-GHz three-way power divider.

On the other hand, its four-way counterpart and simulation results are shared in Figure 3.63 and Figure 3.64. It is basically composed of successive 2 two-way power dividers. Since BIST circuitries are implemented in MIMO design, separate LO signal distribution is required for each Rx and BIST channels on the same power divider. Since the chip area is quite limited and not to degrade the signal level going into the Rx mixers, instead of an eight-way power divider on the Rx side, same coupling scheme of frequency tripler output in two-way power divider is adopted. This is realized by placing transmission lines with certain lengths to couple out additional outputs carrying enough amount of delivered power, which results in a practical eight-way power divider while not increasing the loss on main Rx path at the expense of high coupling loss on BIST path. However careful optimizations are not performed since these blocks would be enabled only to check the Rx functionality during just the initial phases of radar operation. Based on the simulation results, 9.1 dB average insertion loss is achieved with input / output matching conditions satisfied. Such high insertion loss is inevitable due to long transmission lines that are necessary because of the Rx / Tx channel positioning inside the chip, while keeping in mind the theoretical minimum loss of 6 dB from an ideal four-way power divider. Coupled outputs have insertion loss of 21.5 dB which is still enough for mixer sections of BIST channels to operate properly thanks to the following amplification stage. For the first BIST channel belonging the only quadrature Rx channel of the chip, coupling loss reaches almost 35 dB, which is still acceptable thanks to the increased output power after the frequency tripler and the additional PA inserted in BIST channel. The return loss performance of these BIST inputs is therefore quite poor. Finally, shown in Figure 3.63, the same architecture excluding additional coupled outputs is utilized on Tx side which would result in comparatively reduced insertion loss which is found to be 8.7 dB in average.

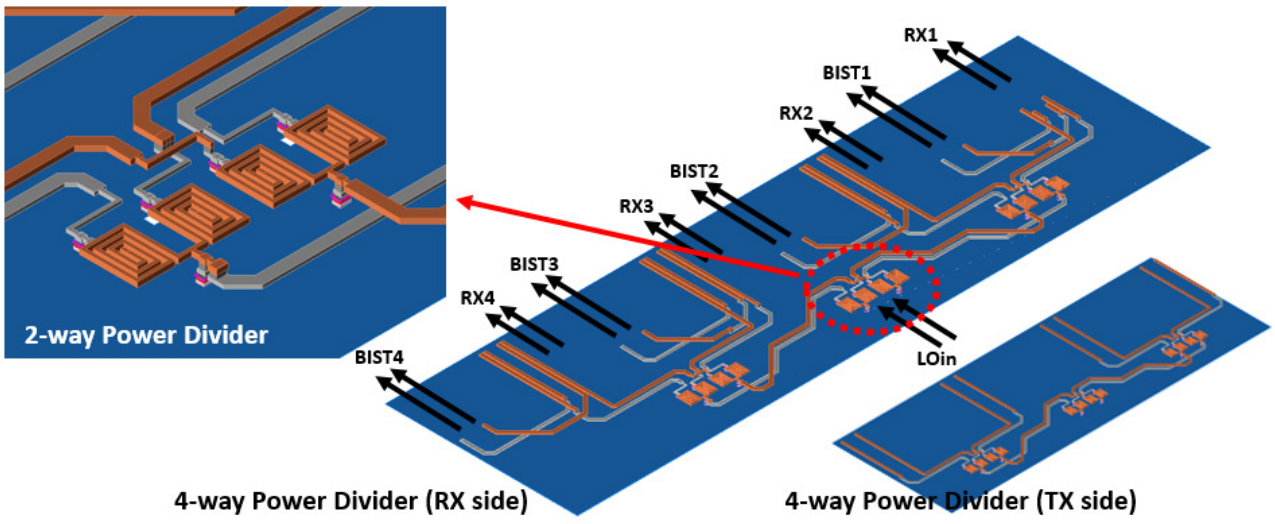

Figure 3.63: Layout of 60-GHz four-way power divider.

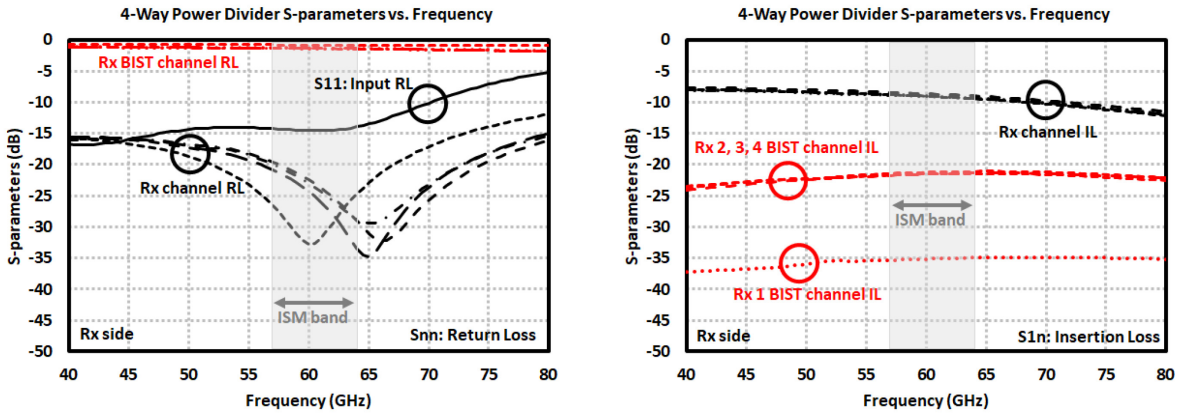

Figure 3.64: Simulation results of 60-GHz four-way power divider on Rx side.

Combining all these passive structures, the performance of total power division stage is simulated and the expected results are stated as in Figure 3.65. Based on the data provided in figures, return losses of Rx and Tx channels stay above 10 dB for almost the whole band. Moreover the average insertion loss within the ISM-band for all the Rx and Tx channels are found to be 13.2 dB whereas the tripler output and BIST channels perform with much higher loss, around 25 dB, as was discussed previously.

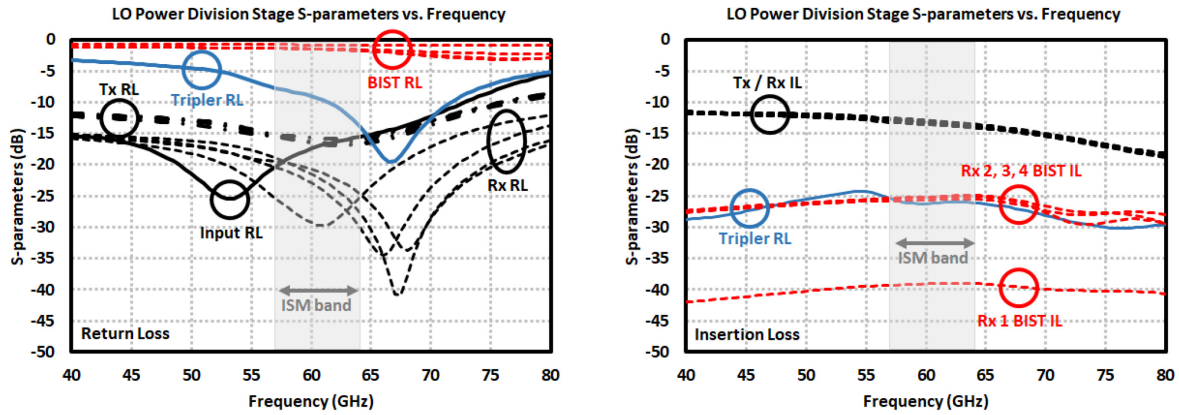

Figure 3.65: Simulation results of 60-GHz combined LO power division stage.

3.5.7 Complete MIMO LO Chain Simulation

Considering all of these design steps, simulation and optimization of the LO chain in 60-GHz MIMO TRx (shown in Figure 3.66) are completed and the results are illustrated in Figure 3.67. The fully simulated LO signal distribution network consists of 20-GHz PA, LO switch, frequency tripler, two-stage PA, 1-to-8 power divider (excluding coupled tripler and BIST channel outputs)

and additional passive structures like transmission lines and balun at 20 GHz for the *LOin* and *LOout* pads.

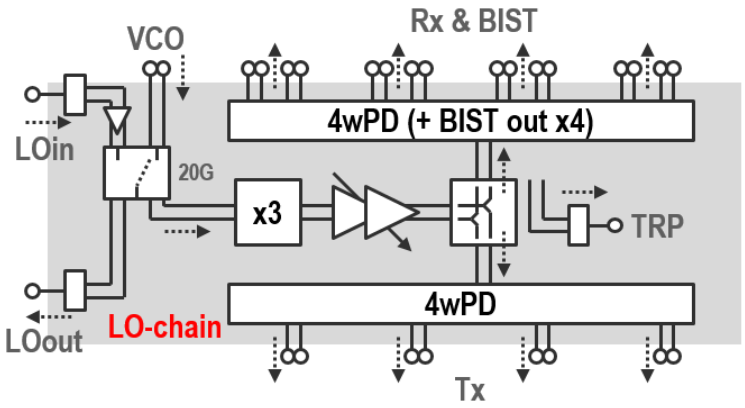

Figure 3.66: Schematic of the complete LO chain in 60-GHz MIMO TRx.

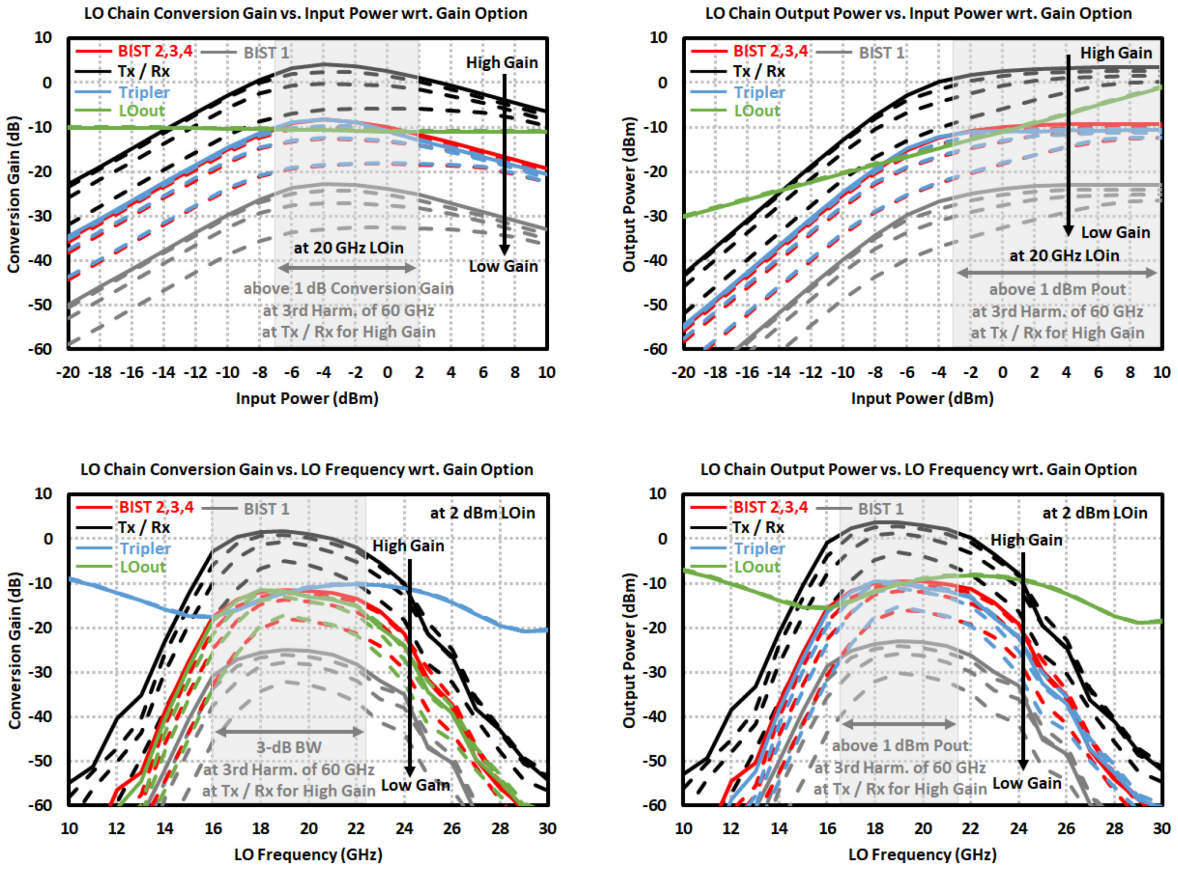

Figure 3.67: Simulation results of the complete LO chain in 60-GHz MIMO TRx with respect to different gain options in *master* mode: (*top left*) conversion gain vs. input power at 20 GHz internal VCO input, (*top right*) output power vs. input power at 20 GHz internal VCO input, (*bottom left*) conversion gain vs. LO input frequency at 2 dBm internal VCO input, (*bottom right*) output power vs. LO input frequency at 2 dBm internal VCO input.

With high gain option enabled, current consumption is found as 122 mA at 3.3 V which could be reduced at the expense of lower transmitted output power, depending on the application. As shown in the same figures, the conversion gain could be reduced from 1.7 dB to -5.1 dB with 2 dBm input power applied (where the output power saturation has already started) within 8 GHz of bandwidth centered at 19 GHz. The output power at Tx and Rx channel inputs are found as 3.6 dBm at 60 GHz whereas the BIST channels and Tripler test output have much less, around -9.5 dBm (the first BIST channel reaches an output power of -23 dBm), as expected. With lower gain options selected, 31.7 mA current (by applying 2.6 V to set the gain) could be saved. In measurements, gain setting pin is adjusted to 2.3 V which corresponds to 2.8 dBm output power in simulations which is quite enough to produce more than 15 dBm of total transmitted output power at the Tx output as was explained in Section 3.4. On the other hand, the *LOout* pin is directed right after the 100 Ω characteristic impedance differential transmission line which is integrated to a balun. This passive section (see Figure 3.68) including the pad parasitic capacitance has a total insertion loss of 1.35 dB with input and output matched, thus the chip output power at *LOout* pad becomes average -9 dBm which is to be directed to the successive *slave* MIMO chip. Including the 20-GHz signal generation circuit current drain of 61.4 mA at 3.3 V (VCO + Frequency Divider + single-stage PA), the total LO signal generation circuitry has itself 605 mW of power consumption at high gain mode.

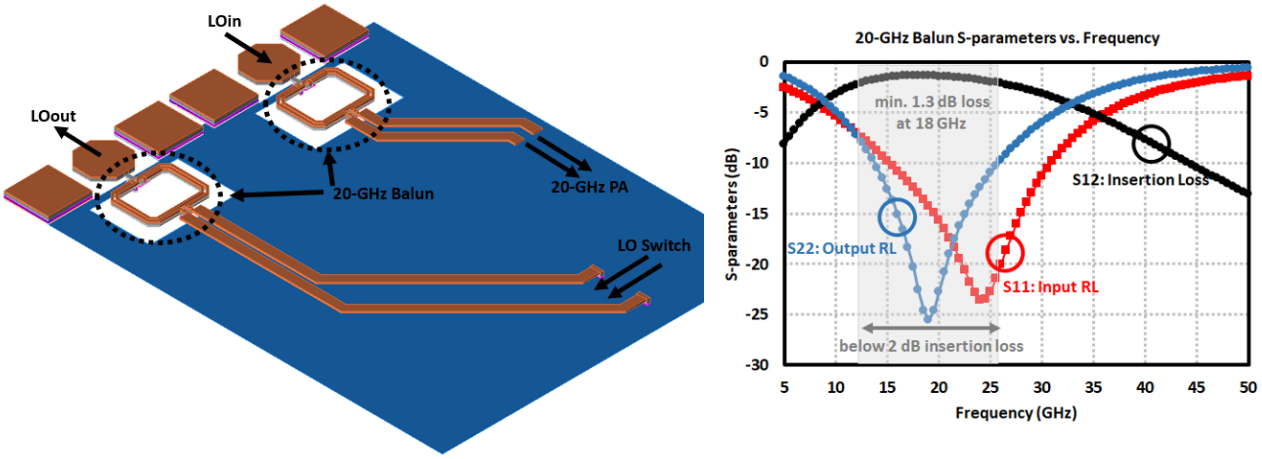

Figure 3.68: Layout and simulation results of 20-GHz balun at *LOin* and *LOout* pads in 60-GHz MIMO LO chain.

Assuming that the chip operates at *slave* mode such that the VCO is turned off, LO switch is set accordingly and the 20-GHz PA is in operation, then the maximum current consumption reaches 140 mA with the maximum output power on channels being saturated with 3.2 dBm at 60 GHz (see Figure 3.69). The conversion gain is 18.9 dB at low input power levels with a bandwidth of 6 GHz. The IP_{1dB} is -15 dBm so that the accepted input power from *LOin* pad is in the range of -15 dBm to 5 dBm at 16.5 – 22.5 GHz. Having high input power at the *LOin* pad lets the circuit go into saturation and degrades the conversion gain greatly, however it only provides an

LO signal that does not carry an important information as in communication systems, thus making it safe to utilize such high input levels. In order to benefit the high operation bandwidth to achieve better range resolution, all the chained MIMO chips could be employed in *slave* mode and fed from an external signal generator because of the limited internal VCO bandwidth (see Figure 2.7).

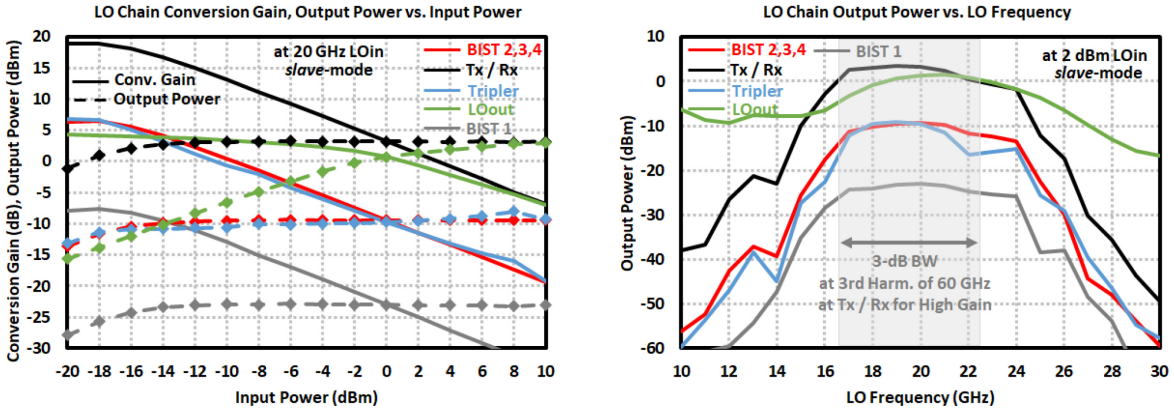

Figure 3.69: Simulation results of the complete LO chain in 60-GHz MIMO TRx in *slave* mode where internal VCO is disabled: (*left*) conversion gain and output power vs. input power at 20 GHz external LO input, (*right*) output power vs. LO input frequency at 2 dBm external LO input.

3.6 Summary of the Designs

Within this chapter, a summary of the design procedure and simulation results of each building block to be placed in the specified five different TRx versions operating around 60- and 122-GHz is discussed. A 130 nm SiGe BiCMOS process with 250 / 340 GHz of f_T / f_{max} is chosen as the fabrication technology. The implemented blocks within the scope of this thesis work include Rx / Tx channels and LO distribution networks except VCO and frequency divider designs (yet many optimizations on these blocks are realized as well). Especially for the TR2 versions, higher performances are expected since the Rx inputs and Tx output are directly connected to pads without additional front isolation coupler. The full EM simulations points out that the designed 60- / 122-GHz PA reaches 17 dBm / 10 dBm saturated output power whereas the 60- / 122-GHz Rx chain, which is composed of LNA, power divider, quadrature mixers and I/Q signal generator, gives a conversion gain of 15.6 dB / 20.5 dB with SSB noise figure of 8.1 dB / 10.9 dB and IP_{1dB} of -16 dBm / -21 dBm in total. Even considering the losses from front isolation couplers in TRM versions, additional connecting lines, baluns and pads in TR2 and MIMO versions, modeling errors and fabrication tolerances, the chipsets are expected to operate with high performance. With these loss-adding sub-components inserted in the simulations, the expected transmitter output powers at the RF pads of 60-GHz TRM and TR2 / MIMO become 10 dBm and 16 dBm whereas its 122-GHz counterparts are expected to achieve 4.7 dBm and 6.5 dBm respectively. Even though the

saturated output power of PA is simulated as 10 dBm, much lower LO power is expected from the VCO especially in TR2 chip having lossy three-way power divider, which would result in decreased transmitted power. According to these results of the compact sub-circuits, high operation bandwidths covering the desired ISM bands with high output power could be achieved overall with these chips which at the end would be suitable candidates for FMCW radar applications.

4 IC Measurement Results

Using the simulation results of all these blocks, different TRx chips are designed and fabricated using 130 nm SiGe BiCMOS process. These chips include 60- / 122-GHz TRM with and without integrated antenna, 60- / 122-GHz TR2 and 60-GHz MIMO TRx. Therefore this section is dedicated to the measurement results of ICs which are already published in [15] – [19].

Since separate test blocks for any of the sub-circuits are not fabricated, full transceivers are directly characterized. For chip measurement purposes, simple FR4 test boards are designed where the RF sections are directly fed with GSG (Ground-Signal-Ground) probes best optimized at the frequency of interest. Many of the circuits have differential output requiring GSGSG type probes that were not available by the time of measurements that is why only a single pad is excited in such circuits and the other is left open. Then the calibration of this is conducted by careful comparison with the simulations by creating the same measurement environment in simulations. For the Rx measurements, an external signal generator is utilized to apply RF power at swept frequencies with swept powers to extract the conversion gain and linearity measures at the IF outputs which are observed through the oscilloscope. The LO inputs of mixers are already powered with integrated VCOs thus additional signal source is not required. For the Tx measurements, first a spectrum analyzer is utilized to observe the Tx output spectrum with respect to adjusted VCO tuning voltages and the IC operation bandwidth is identified. To correctly characterize the transmitted power, a power detector operating at the specific frequency band is utilized and the losses until the chip pads are de-embedded. At this point the effects of all the gain tuning options are tested. Frequency divider output is directly connected to frequency counter so that frequency and output power information are attained. Such information is necessary for proper design of external PLL network to be used in the final FMCW radar. 122-GHz chip measurements are realized with a harmonic mixer and directional coupler connecting to spectrum analyzer for the Tx measurements whereas frequency extender is added at the output of signal generator to achieve a D-band measurement setup for Rx channel measurements.

Considering these measurement steps, all the transceiver chips are characterized and their performances are summarized in the following sections which are dedicated to a different chip version.

4.1 Measurements of 60-GHz Double-Receive-Channel TRx

Figure 4.1 shows the photo of fabricated 60-GHz TR2 chip which has a silicon area of 1.55 mm^2. Current consumption of this chip is 183 mA at 3.3 V single supply. To increase the output power, a supply voltage of 3.9 V could be applied which causes a current drain of 245 mA. From Figure 4.2, the Tx operation frequency is found as 55.5 – 65.1 GHz with a resultant bandwidth of 9.6 GHz. Such bandwidth difference between the 60-GHz TRM chip emanates from different tapeouts in which the TRM version is enhanced with increased bandwidth. On the other hand, the frequency divider operates between 1.73 – 2.03 GHz. The effect of 3-bit VCO tuning controls are shown as well.

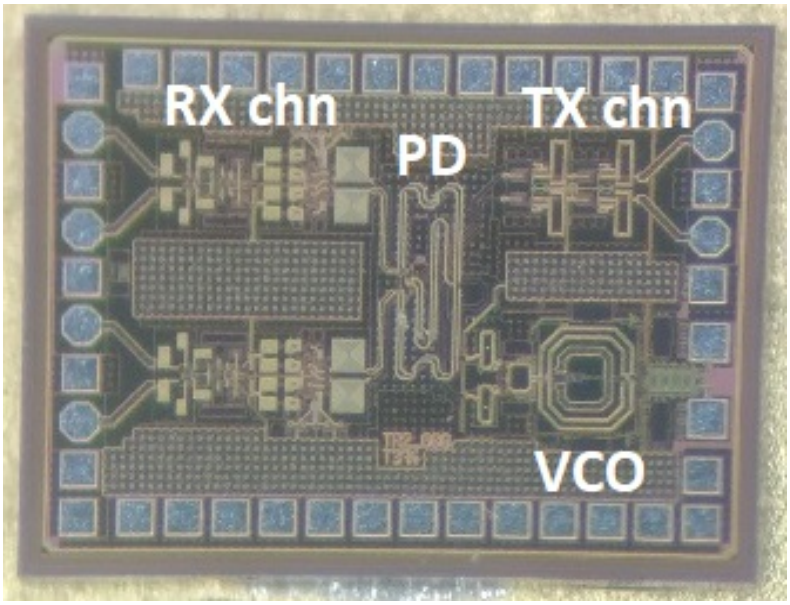

Figure 4.1: Photo of the fabricated 60-GHz TR2 transceiver chip occupying 1.46 mm x 1.06 mm area.

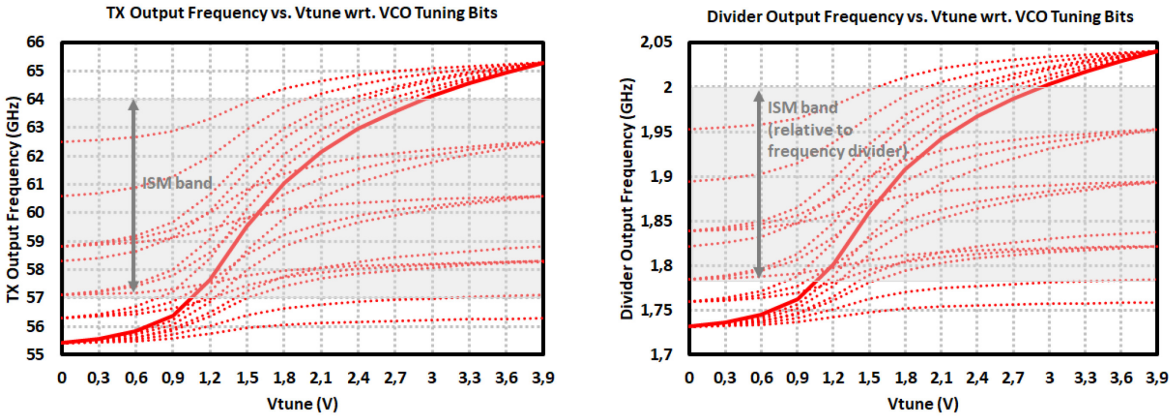

Figure 4.2: Measurement results of the 60-GHz TR2 TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to VCO tuning bits.

With respect to applied voltages, the changes in Tx and frequency divider output frequencies, together with Tx and frequency divider output powers are stated in Figure 4.3 and Figure 4.4 respectively. According to results, a voltage change up to 3.9 V corresponds to 600 MHz of frequency shift in Tx output which is a similar to what is found in 60-GHz TRM VCO. Since this version does not include the high isolation coupler, output power is much higher in contrast to TRM chip. Using Figure 4.4, it is concluded that, with 3.3 V supply, output power could reach maximum 14.5 dBm centered at 62 GHz while possessing a 3-dB bandwidth of more than 10 GHz starting from 55.5 GHz and extending beyond 65.5 GHz which could not be measured due to required measurement equipment. With higher supply voltages, 15.5 dBm output power could be attained whereas around 13.7 dBm output power is accessible even with 3.0 V supply which is quite beneficial to reduce the current consumption to 158 mA. Frequency divider reaches an average output power of -10 dBm at 3.3 V while 2.5 dB increase is possible at higher supply as well.

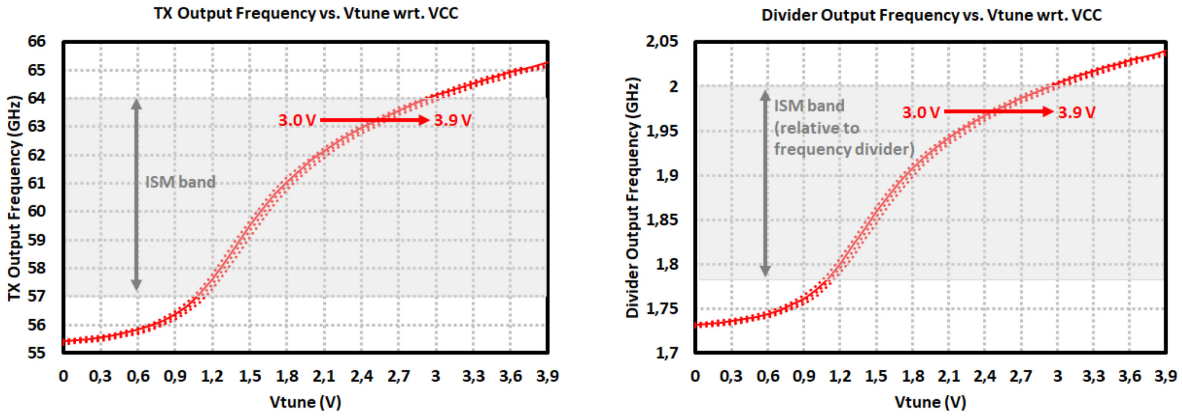

Figure 4.3: Measurement results of the 60-GHz TR2 TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V.

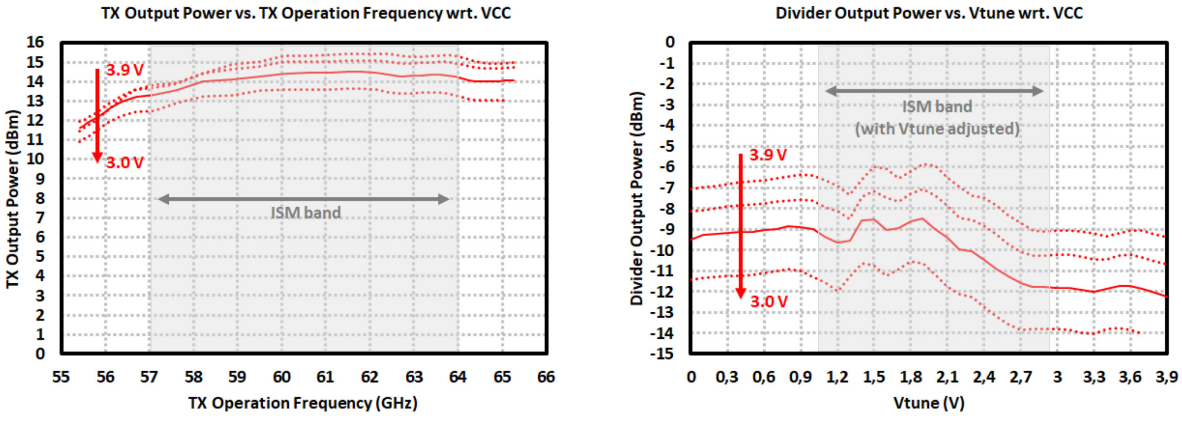

Figure 4.4: Measurement results of the 60-GHz TR2 TRx: (*left*) Tx output power vs. frequency, and (*right*) Frequency Divider output power vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V.

In Figure 4.5 and Figure 4.6, the effect of temperature increase on Tx output power and Tx and frequency divider output frequencies are illustrated. Based on these graphs, the Tx output power decreases by 4.5 dB at 125°C in its less active region starting from 59 GHz. The current consumption drops to 173 mA at the same time. The VCO operation frequency changes by 600 MHz in the lower and upper frequency ranges whereas this change is less effective within the ISM band with about 300 MHz frequency shift.

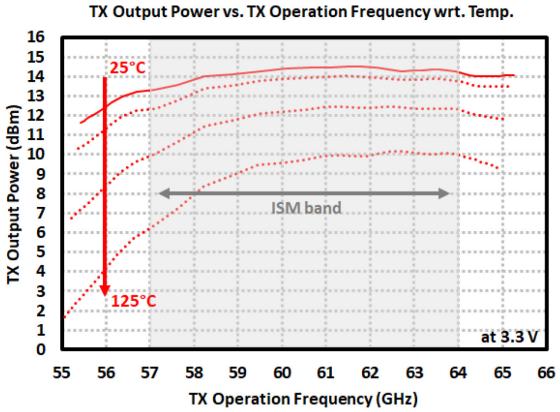

Figure 4.5: Measurement results of the 60-GHz TR2 TRx: Tx output power vs. frequency with respect to temperature.

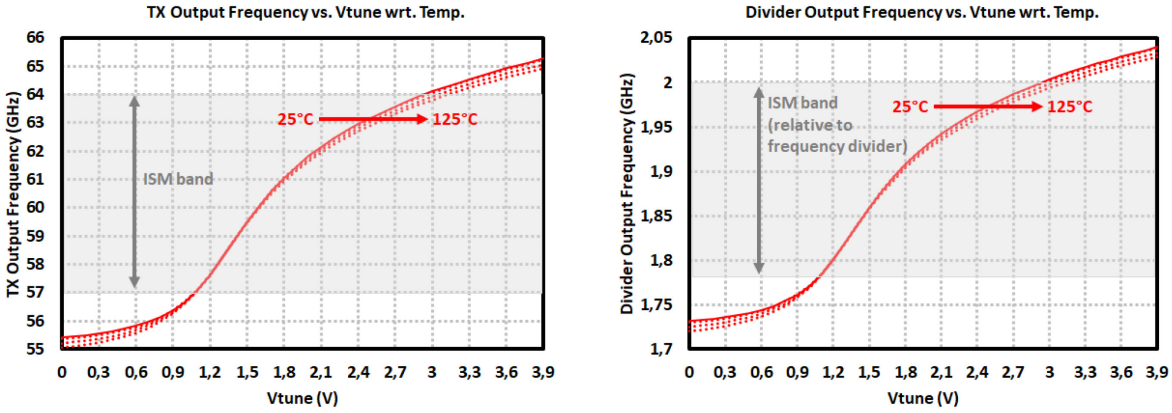

Figure 4.6: Measurement results of the 60-GHz TR2 TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to temperature.

In Figure 4.7, Tx output power with respect to Tx gain options and the phase noise measured at the differential frequency divider outputs are plotted. Adjusting the gain controlling pads, Tx output power, hence the power consumption, could be set. With the lowest gain option enabled, around 2 dBm output power is obtained. Using the adjacent graph, divider output phase noise is found as maximum -124.3 dBc/Hz at 1 MHz offset (-100 dBc/Hz at 100 kHz and -137 dBc/Hz at 10 MHz) which translates into a VCO phase noise of -100.3 dBc/Hz at 1 MHz offset.

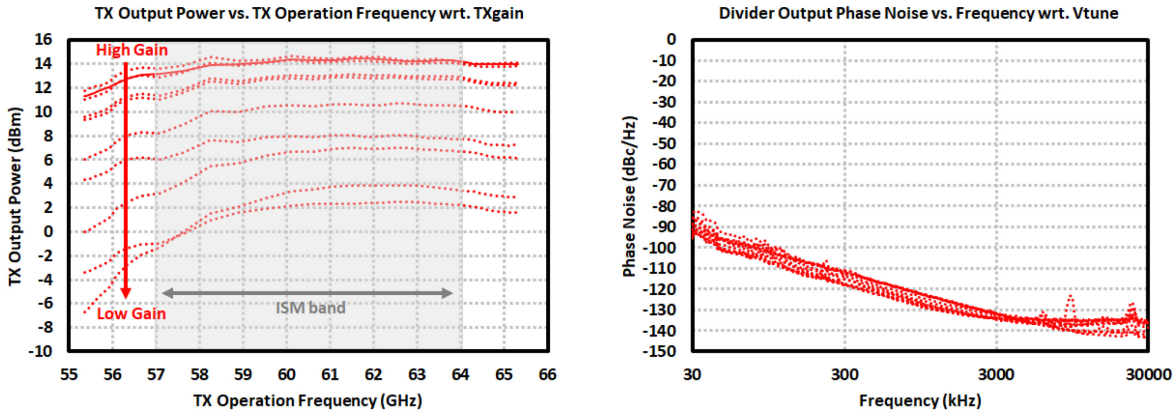

Figure 4.7: Measurement results of the 60-GHz TR2 TRx: (*left*) Tx output power vs. frequency with respect to Tx gain control voltages 0 V – 3.3 V, (*right*) Frequency Divider phase noise with respect to VCO tuning voltages.

Finally Rx measurements are conducted and the results are shared in Figure 4.8 and Figure 4.9. The conversion gain is measured in both channels and 21 dB in average is attained while it reaches a quite flat operation. Between the differential I/Q IF outputs, maximum amplitude and phase imbalances are found below 0.5 dB and 10° (from quadrature outputs). Not shown in the figures, isolation between Rx channels is above 20 dB which is measured by applying power to Rx channel 2 and comparing the IF channel 1 output levels. The linearity measures for different Rx gain control options are conducted as well and plotted in Figure 4.9. These gain control pins could set the gain down to 8 dB by 6 dB steps. Input referred 1 dB compression point at 64.5 GHz is -14 dBm at high gain mode enabled whereas this could be improved to -2 dBm with the low gain mode which provides quite linear behavior. Since the conversion gain curve is almost flat, same response is achieved almost for the whole frequency band.

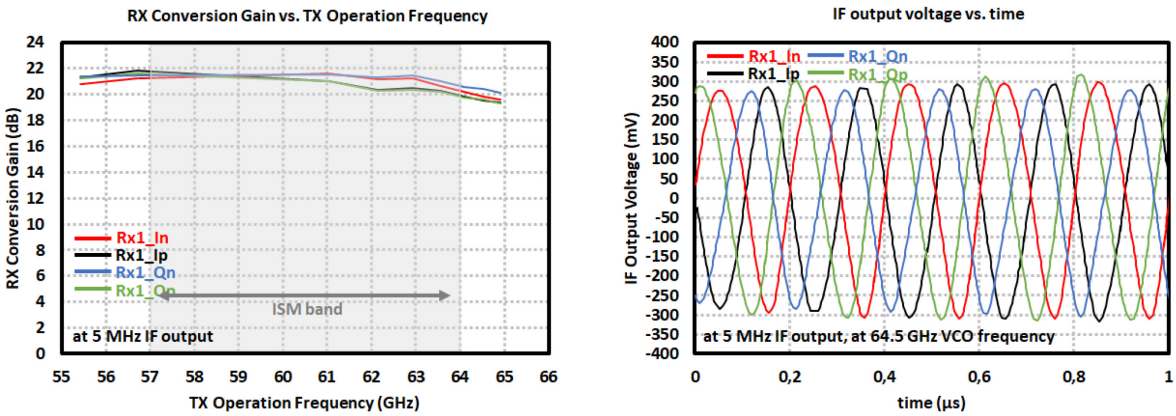

Figure 4.8: Measurement results of the 60-GHz TR2 TRx: (*left*) Rx channel 1 conversion gain vs. frequency, (*right*) 5-MHz IF output voltages at 64.5 GHz.

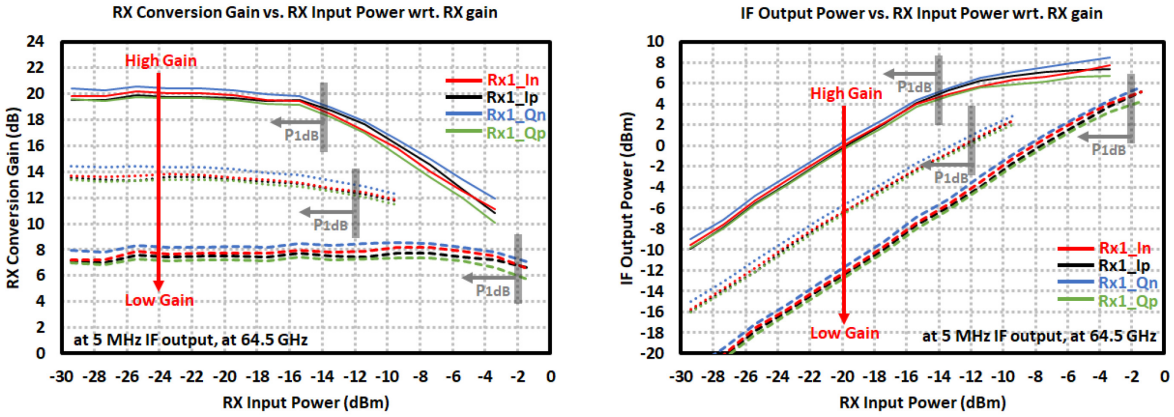

Figure 4.9: Measurement results of the 60-GHz TR2 TRx: (*left*) Rx channel 1 conversion gain, and (*right*) IF channel 1 output power vs. Rx input power at 64.5 GHz with respect to Rx gain control voltages.

4.2 Measurements of 122-GHz Double-Receive-Channel TRx

The 122-GHz counterpart of TR2 architecture is shown in Figure 4.10. It has a total chip area of 1.42 mm^2 which is quite compact as the other versions. The chip drains 282 mA from 3.3 V of single supply. This high current consumption is necessary to achieve high output power.

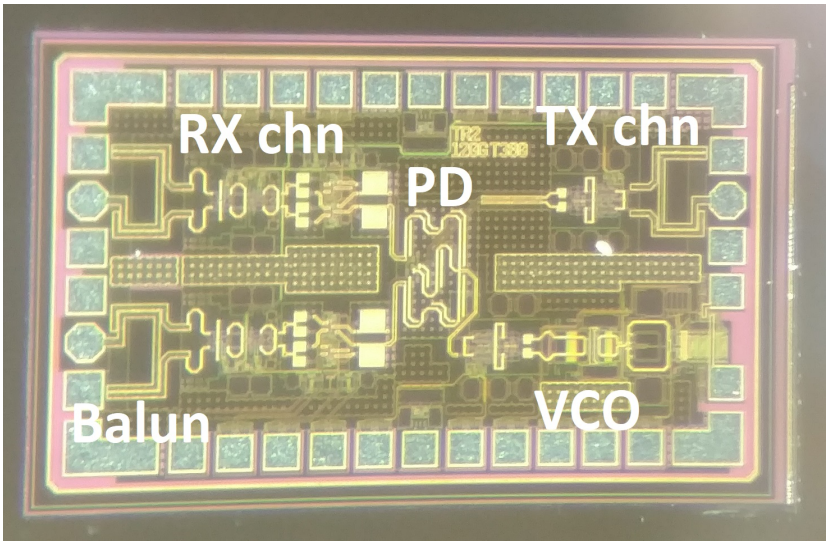

Figure 4.10: Photo of the fabricated 122-GHz TR2 transceiver chip occupying 1.54 mm x 0.92 mm area.

The Tx operation bandwidth is found as 7.4 GHz in the range of 118.9 – 126.3 GHz whereas the corresponding power detector output operates in the between 1.86 – 1.97 GHz for external PLL (see Figure 4.11). In this version the internal VCO has 2-bit frequency tuning mechanism as seen from the same curves.

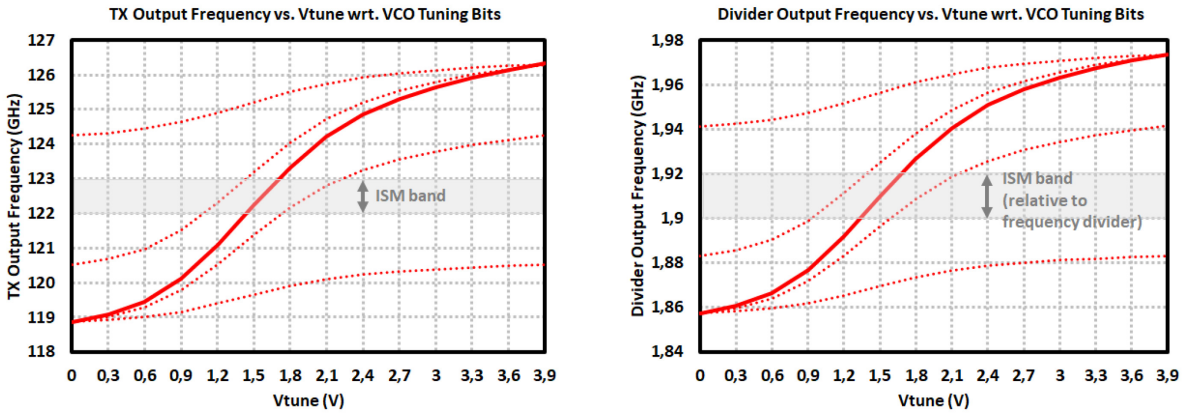

Figure 4.11: Measurement results of the 122-GHz TR2 TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to VCO tuning bits.

In the following Figure 4.12 and Figure 4.13, effect of supply voltage change by 300 mV up to 3.9 V on Tx and frequency divider output frequencies and output powers are mentioned. Based on the measured data provided, VCO operation frequency experiences a constant downward frequency shift of 300 MHz as the VCC is changed from 3.0 V to 3.9 V. For the frequency divider, such shift means only 5 MHz decrease in total. The Tx output power is measured to be 2 dBm in average across the specified operation bandwidth with maximum of 2.5 dBm at 119 GHz when fed with 3.3 V supply. In case this supply voltage is increased to 3.9 V, the circuit consumes 373 mA of current while only delivering 2.5 dBm average power. Naturally the lower power consumption is preferred over such low power increase. Having observed the change in maximum output power with respect to frequency compared to the simulations, it could be interpreted that there exists a frequency shift in the operation range towards 118 GHz. Yet the output power is much lower compared to the simulated results. On the other hand, frequency divider has -8 dBm output power.

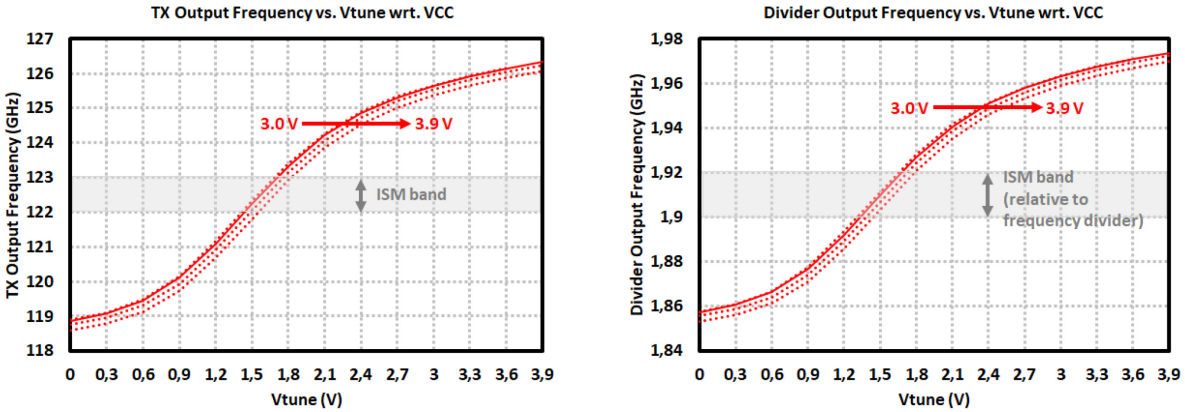

Figure 4.12: Measurement results of the 122-GHz TR2 TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V.

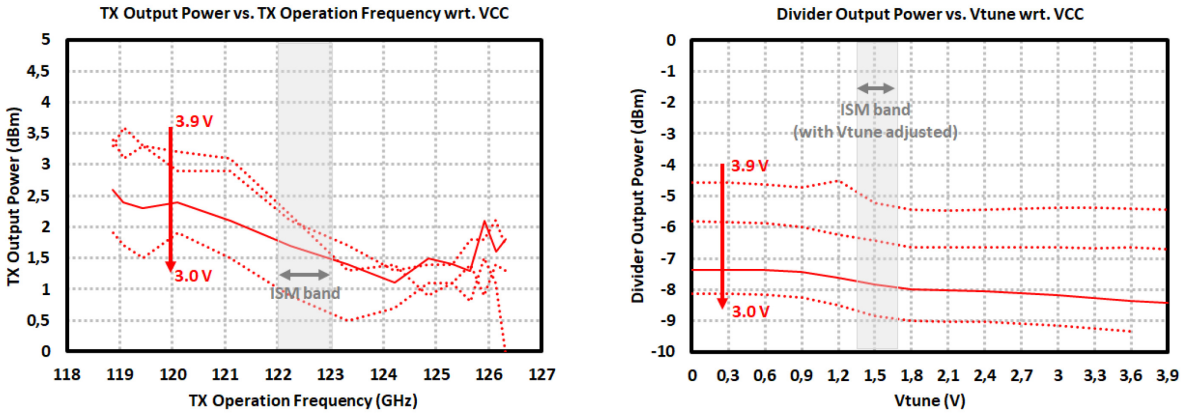

Figure 4.13: Measurement results of the 122-GHz TR2 TRx: (*left*) Tx output power vs. frequency, and (*right*) Frequency Divider output power vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V.

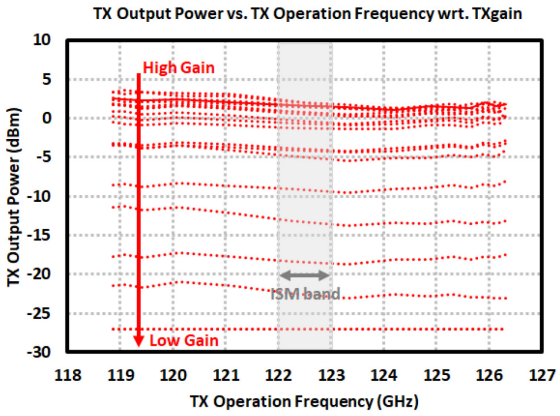

Figure 4.14: Measurement results of the 122-GHz TR2 TRx: Tx output power vs. frequency with respect to Tx gain control voltages 0 V – 3.3 V.

With the help of gain tuning pins, the output power could be controlled in analogue way and made completely turned off. Such operation is illustrated in Figure 4.14 where the minimum level around -28 dBm is due to the limit in minimum observable range of external D-band power detector. From the behaviors of curves, it is evident that a flat power response is attained. Figure 4.15 shows the relation between temperature change and Tx output frequency and output power. According to results, with the operation temperature rising to 125°C, the output power significantly decreases below -8 dBm within the ISM band. Moreover the frequency shift is much greater compared to previous TRx versions which varies about 1.5 GHz. Yet within the industrial temperature standards the power drops to -2 dBm at 85°C (considering the ISM band between 122 – 123 GHz) which allows range measurements with 900 MHz downward frequency shift. Current consumption at this temperature becomes 273 mA at 3.3 V.

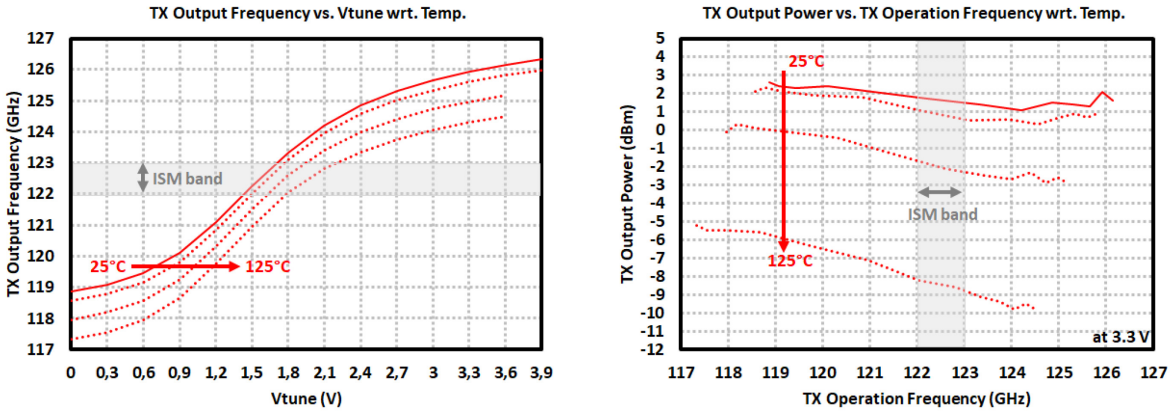

Figure 4.15: Measurement results of the 122-GHz TR2 TRx: (*left*) Tx output frequency vs. VCO tuning voltages, and (*right*) Tx output power vs. frequency with respect to temperature.

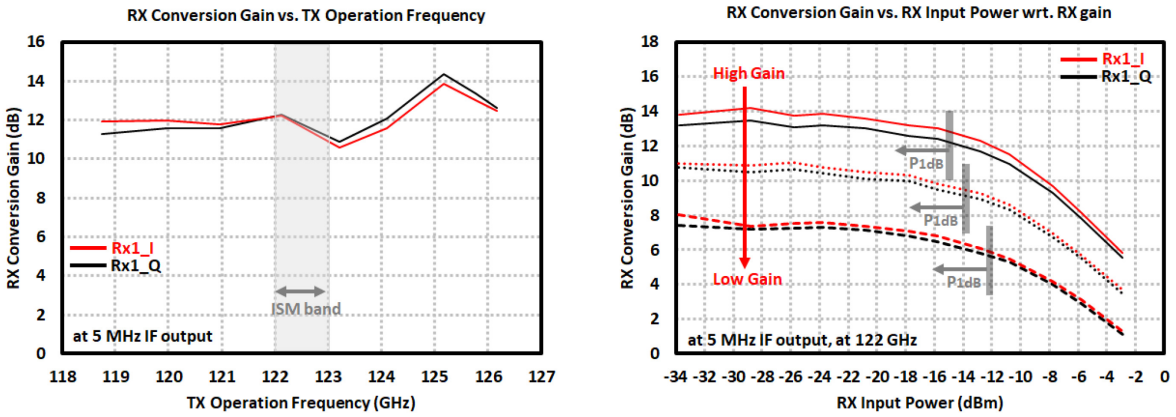

Figure 4.16: Measurement results of the 122-GHz TR2 TRx: Rx channel 1 conversion gain (*left*) vs. frequency, and (*right*) vs. Rx input power with respect to Rx gain control voltages at 122 GHz.

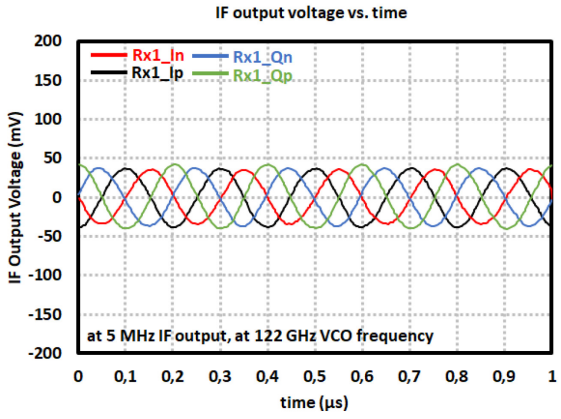

Figure 4.17: Measurement results of the 122-GHz TR2 TRx: 5-MHz IF output voltages at 122 GHz.

The Rx channel measurements are depicted in Figure 4.16 and Figure 4.17. The conversion gain is around 12 dB in average and whole the operation band is within the 3-dB bandwidth of Rx channel. The gain and I/Q phase imbalances are less than 0.5 dB and 7°. The gain tuning options could be applied to decrease the gain by 6 dB in total with 3 dB gain steps and to improve the linearity. With the Rx enable option, the channels could be separately turned off. The IP_{1dB} is measured as -15 dBm at high gain mode which could be further improved to -12 dBm in low gain mode while decreasing the current consumption to 260 mA.

4.3 Measurements of 60-GHz Monostatic TRx

The photo of fabricated TRM and TRMant (version with monostatic TRx with integrated dipole antenna) chips occupying 1.2 mm^2 and 1.4 mm^2 die area are shown in Figure 4.18 with all the measurement results depicted between Figure 4.19 and Figure 4.25. The circuit blocks are highlighted on the figures with the HIC being the high isolation coupler inserted for monostatic configuration. In the TRMant version, the dipole antenna is placed at the chip edge considering the expected beam tilt to be later corrected with the adjusted lens position.

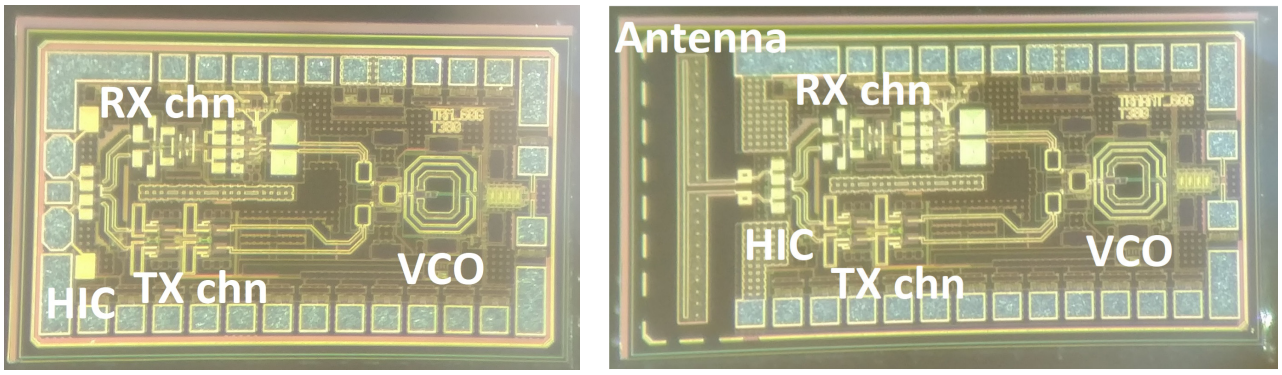

Figure 4.18: Photo of the fabricated 60-GHz TRM and TRMant transceiver chips occupying 1.42 mm x 0.84 mm and 1.64 mm x 0.84 mm area.

The total power consumption of these chips are measured as 171 mA at 3.3V single supply (184 mA / 198 mA at 3.6 V / 3.9 V supply). As seen in Figure 4.19, the operation bandwidth is found to be 10 GHz between 55.6 – 65.6 GHz when 3-bit VCO tuning voltages of 0 V – 3.9 V is applied. Since the frequency divider has a division ratio of 16, the operation frequency which is to be directed to external PLL for frequency stabilization is measured as 1.74 – 2.05 GHz considering the 30-GHz fundamental frequency of push-push VCO.

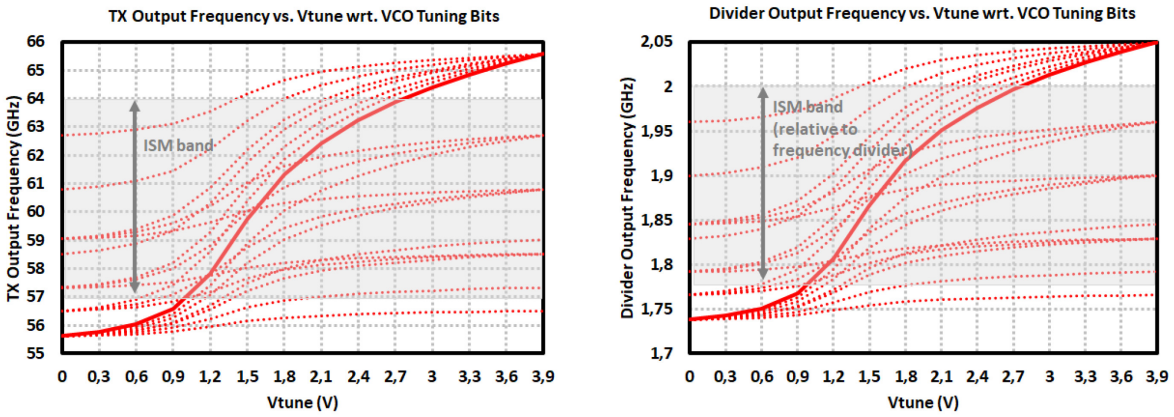

Figure 4.19: Measurement results of the 60-GHz TRM TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to VCO tuning bits.

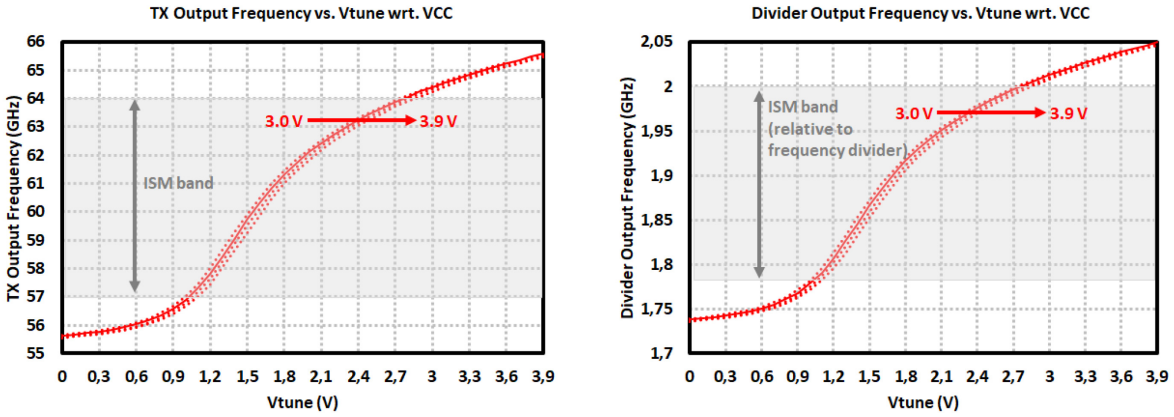

Figure 4.20: Measurement results of the 60-GHz TRM TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V.

The graphs in Figure 4.21 highlight the Tx channel and frequency divider output powers with respect to supply voltage change by 300 mV. The Tx output power at 3.3 V is found as 8.5 dBm in average within the defined ISM band (57 – 64 GHz) with 9.2 dBm maximum output power observed at 57.5 GHz. Using the same graphs, the 3-dB bandwidth of Tx channel (excluding the internal VCO bandwidth limitation) extends beyond 10 GHz. When 3.9 V is applied, at the expense of increased power consumption, the transmitter output power could be enhanced by 1 dB and 9.5 dBm output power could be extracted. On the other hand, the frequency divider output power is around -12.5 dBm at 3.3 V supply which is improved by 3 dB with 3.9 V. Such low output power is still enough for the frequency synthesizer network.

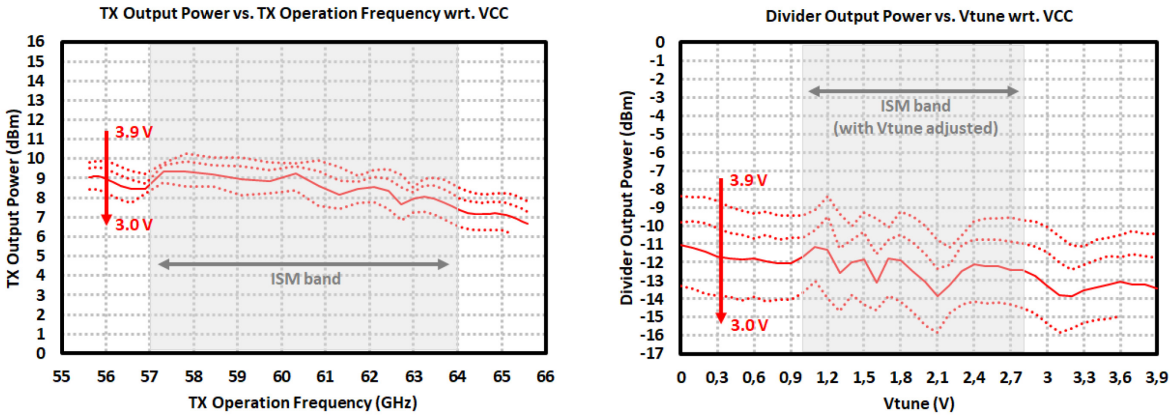

Figure 4.21: Measurement results of the 60-GHz TRM TRx: (*left*) Tx output power vs. frequency, and (*right*) Frequency Divider output power vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V.

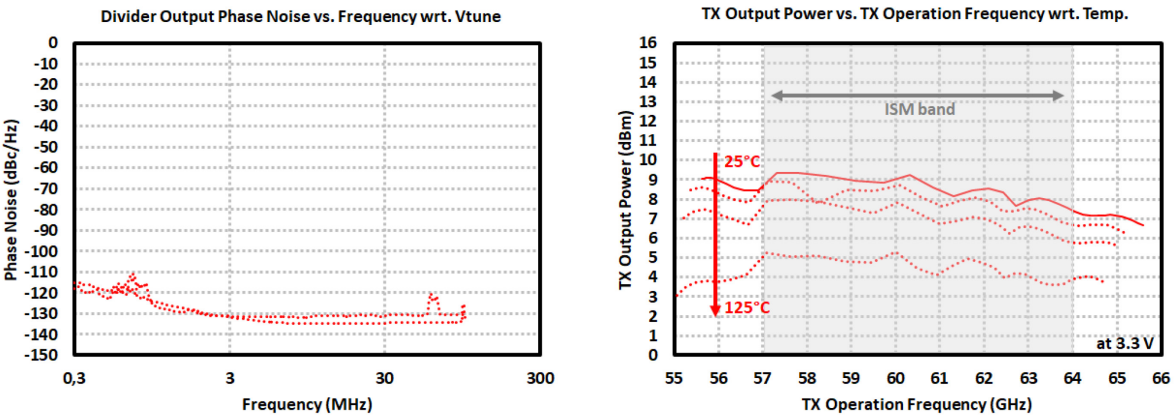

Figure 4.22: Measurement results of the 60-GHz TRM TRx: (*left*) Frequency Divider phase noise at 1.74 GHz and 2.05 (corresponding to Tx operation frequencies of 55.6 GHz and 65.6 GHz), (*right*) Tx output power vs. frequency with respect to temperature.

Using the graph in Figure 4.22, divider output phase noise is measured as maximum -124.5 dBc/Hz at 1 MHz offset (-115 dBc/Hz at 300 kHz and -134.6 dBc/Hz at 10 MHz) which corresponds to a VCO phase noise of -100.5 dBc/Hz at 1 MHz offset. On the same figure and in Figure 4.23, Tx output power, Tx output frequency and frequency divider output frequency with respect to changing operation temperatures are highlighted. To achieve these results, a simple measurement is realized where the chuck temperature of probe setup is varied up to 125°C. Based on the results, VCO operation frequency changes to 55.1 – 64.9 GHz with a downward frequency shift of about 600 MHz at 3.3 V supply. The current consumption decreases to 148 mA at 125°C which translates into the output power drop approximately by 4 dB (4.5 dBm). Within the ISM band, the frequency shift in Tx is less than 300 MHz which corresponds to below 10 MHz shift in frequency divider output. The Tx output power could be changed with the integrated gain control

pins. This is visualized in Figure 4.24 on which the analogue gain tuning could provide a gain range about 20 dB when adjusted between 0.8 V and 3.3 V. On the same figure, the effect of some of the gain options on Tx output power with respect to Tx operation frequency is plotted where clear gain drop across frequency is observed. The integrated power detector operation is drawn as well. Using the same graph, the power detector achieves a dynamic range of more than 20 dB by mapping Tx output power range between -12 dBm and 9.5 dBm to a linear voltage output range between 120 mV and 1 V, which could be easily measured using a multimeter without any amplification.

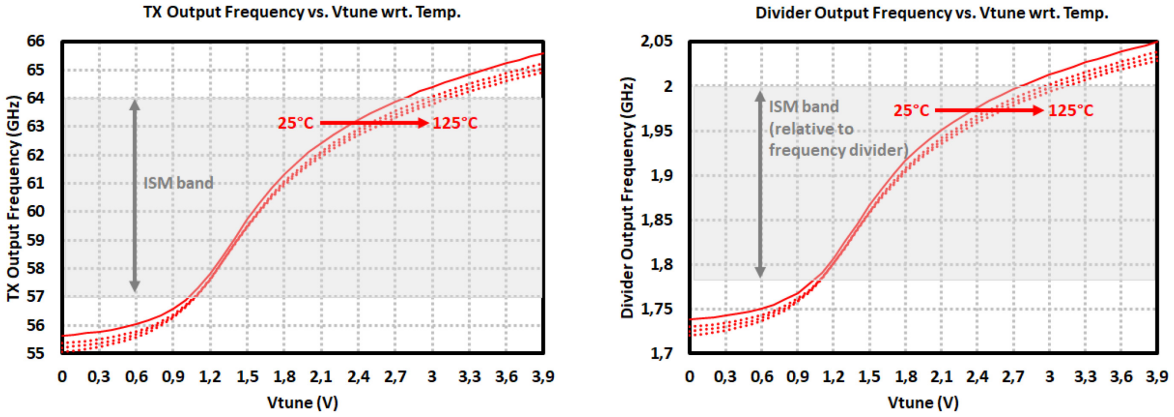

Figure 4.23: Measurement results of the 60-GHz TRM TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to temperature.

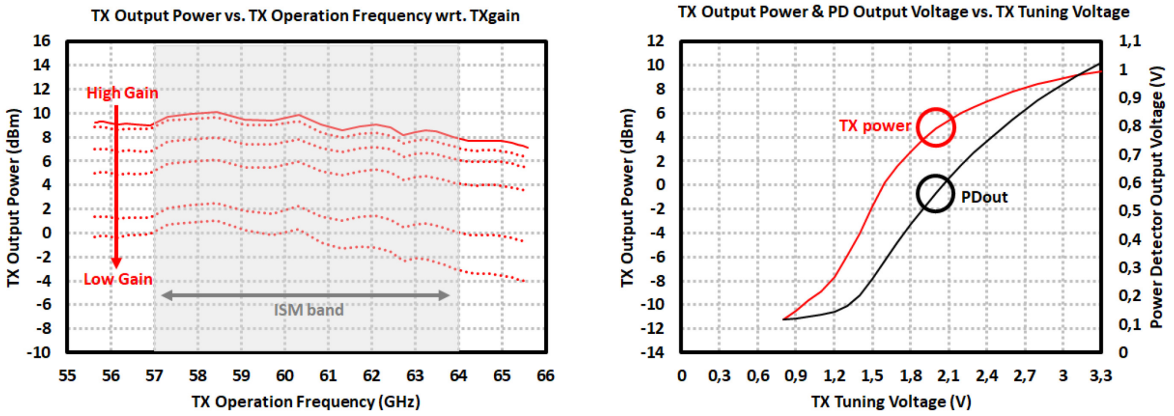

Figure 4.24: Measurement results of the 60-GHz TRM TRx: (*left*) Tx output power vs. frequency with respect to Tx gain control voltages 0 V – 3.3 V, (*right*) Tx output power and Power Detector voltage vs. Tx gain tuning voltages.

In Figure 4.25, the Rx channel measurements are shown where conversion gain plot is extracted with respect to digitally controlled Rx gain options. The results of first Rx channel point out maximum conversion gain of 14 dB (averaged for differential I/Q IF outputs) at 62 GHz with a 3-dB bandwidth of 7 GHz between 58 – 65 GHz. With the control options, the gain could be

reduced by almost 16 dB in 8 dB steps. The gain imbalance between IF outputs are found as ±1 dB with phases are almost correctly aligned for the differential outputs. However I/Q phase imbalance is measured as 10° which the main reason is from the non-symmetric connection between I/Q signal generator and differential mixer. On the same figure, IF outputs achieved at 5 MHz is highlighted as well.

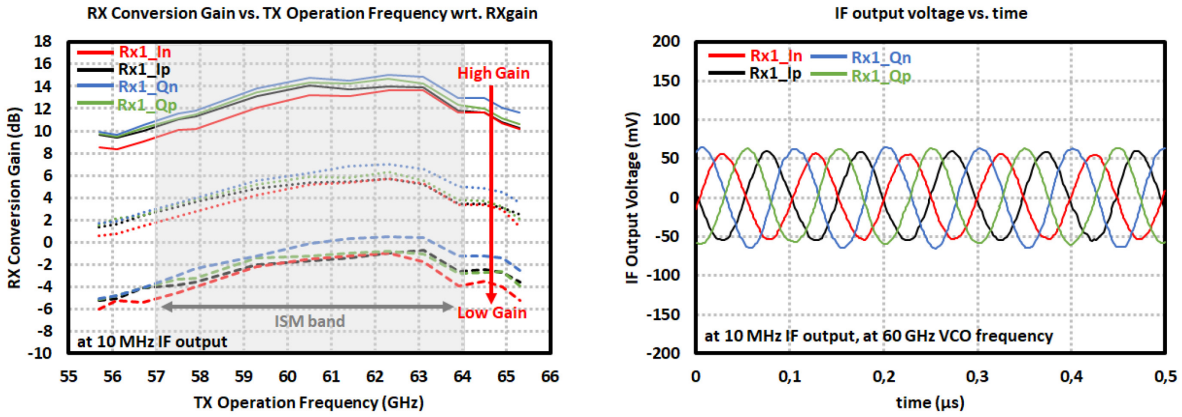

Figure 4.25: Measurement results of the 60-GHz TRM TRx: (*left*) Rx channel conversion gain vs. frequency with respect to Rx gain control voltages, (*right*) 10-MHz IF output voltages at 60 GHz.

4.4 Measurements of 122-GHz Monostatic TRx

In Figure 4.26, photos of the fabricated 122-GHz TRM and TRMant versions could be viewed with the block names highlighted. They occupy 1 mm^2 and 1.1 mm^2 respectively.

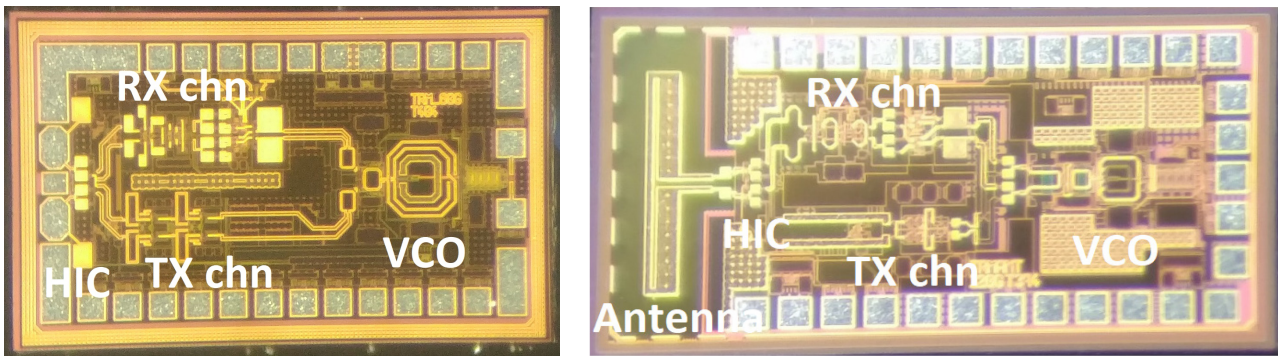

Figure 4.26: Photo of the fabricated 122-GHz TRM and TRMant transceiver chips occupying 1.35 mm x 0.76 mm and 1.49 mm x 0.73 mm area.

The maximum current consumption of these TRM circuits defined by the enabled maximum gain mode are measured as 152 mA at 3.3 V of single supply. In the measurements shown in Figure 4.27, the VCO bandwidth is found to be 7.4 GHz starting from 119.2 GHz and extending up to

126.6 GHz whereas the power detector output frequency is changing between 1.86 – 1.98 GHz to be stabilized with PLL later on. Since the VCO block is completely the same as in the prior bistatic TR2 version, the chip would naturally operate in the same frequency region. Minor differences in their frequency responses come from different fabrication processes with changing transistor and capacitor tolerances occurring especially in the VCO core, however it is quite negligible when compared.

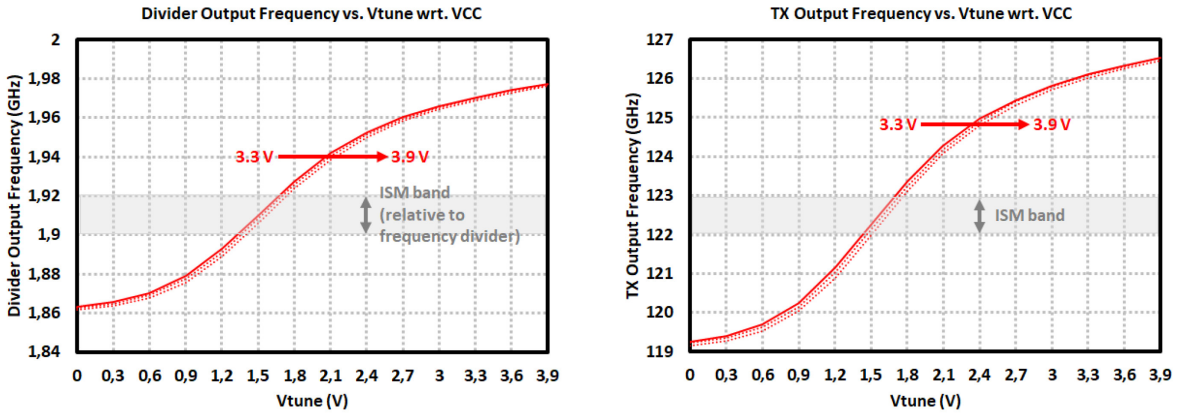

Figure 4.27: Measurement results of the 122-GHz TRM TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to changing supply voltages between 3.3 V – 3.9 V.

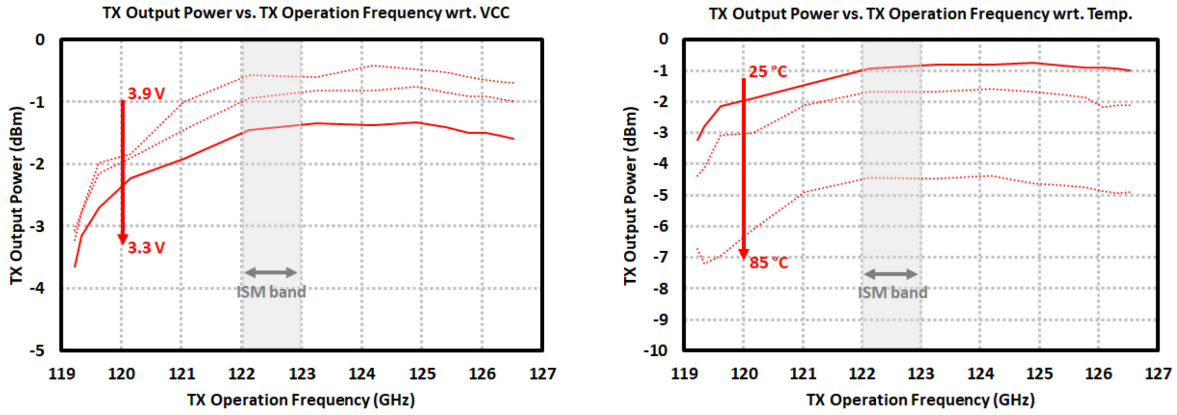

Figure 4.28: Measurement results of the 122-GHz TRM TRx: (*left*) Tx output power vs. frequency with respect to changing supply voltages between 3.3 V – 3.9 V, (*right*) Tx output power vs. frequency with respect to temperature.

In Figure 4.28, transmitter and frequency divider output powers with respect to different operation voltages within the full VCO bandwidth are highlighted. According to measurements, maximum transmitted output power is found to be -1.3 dBm between 122 – 125 GHz when fed from 3.3 V single supply. At the lower operation frequencies, the output power decreases to -3 dBm. Such decreased power levels compared to TR2 version are due to the integration of front coupler

for conversion to single RF input. With higher supply voltages the output power could be increased up to -0.5 dBm with a current consumption of 185.3 mA at 3.9 V and to -0.8 dBm with 170 mA current drain from 3.6 V supply. On the other hand, the frequency divider has an output power around -8 dBm within the full operation range and could be further increased at higher supplies. Tx output power behavior with respect to different temperatures is plotted in Figure 4.28 as well. When the temperature rises to 85 °C, output power reduces to -4.5 dBm (at 3.6 V supply) while the IC is still operational.

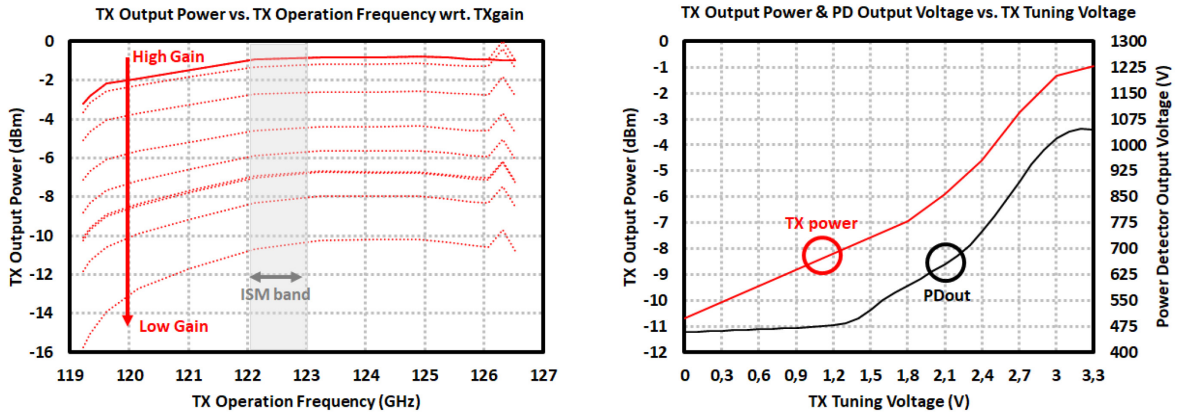

Figure 4.29: Measurement results of the 122-GHz TRM TRx: (*left*) Tx output power vs. frequency with respect to Tx gain control voltages, (*right*) Tx output power and Power Detector output voltage vs. Tx gain tuning voltages.

The chip incorporates Tx channel gain modes which is controlled by a combination of dedicated gain tuning pins. By this way the output power is adjusted in almost 10 dB range and the power consumption could be set depending on the application requirements. This scheme is illustrated in Figure 4.29 where the power detector maps this range to an output voltage profile changing between 450 mV and 1.05 V at the center frequency.

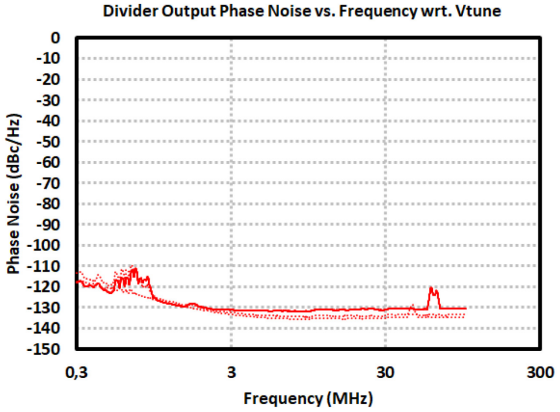

Figure 4.30: Measurement results of the 122-GHz TRM TRx: Frequency Divider phase noise at 1.86 GHz, 1.91 GHz and 1.97 (corresponding to Tx operation frequencies of 119.1 GHz, 122.2 GHz and 126.1 GHz).

The frequency divider phase noise is plotted in Figure 4.30, which is measured as -125.5 dBc/Hz at 1 MHz offset (-113.1 dBc/Hz at 300 kHz and -131.4 dBc/Hz at 10 MHz). This translates into a VCO phase noise of -95.5 dBc/Hz at 1 MHz offset.

Rx measurements are not performed for this version. However the internal blocks are kept the same as the TR2 version (see Section 4.2) with almost the only change being the integrated front isolation coupler except the matching sections between blocks. Therefore similar operation curves are expected with reduced conversion gain, average around 7 dB, and noise figure performances and a bit improved linearity, around -9 dBm, compared to what is achieved in TR2 in Figure 4.16.

4.5 Measurements of 60-GHz MIMO TRx

The chip photo of fabricated 60-GHz MIMO IC occupying 5.2 mm^2 area is shown in Figure 4.31, [19]. The current consumption is measured when TDM operation is considered for which only one Tx channel would be turned on at each time slot, which results in 353 mA in *master* mode at 3.3 V single supply with all the Rx channels are turned on at the same time. Increasing the supply voltage to 3.9 V would bring the total current consumption to 527 mA just for about 1 dB of output power raise which is not practical and not considered for the end product.

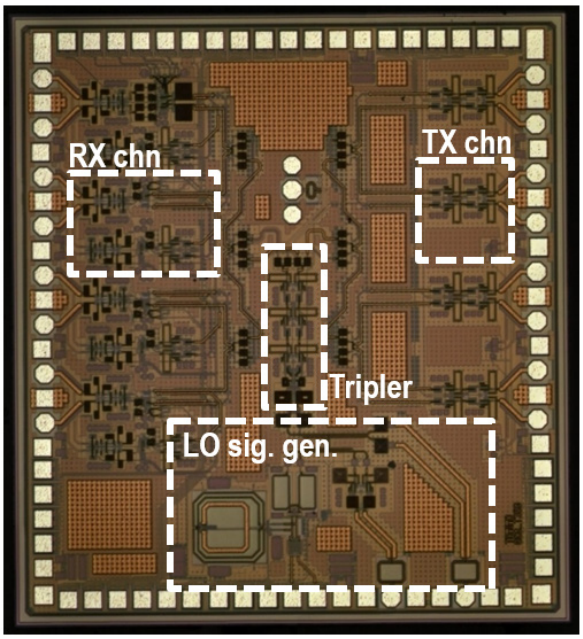

Figure 4.31: Photo of the fabricated 60-GHz MIMO transceiver chip occupying 2.16 mm x 2.39 mm area) [19].

Tx and frequency divider output frequencies with respect to different supply voltages are plotted in Figure 4.32. The TRx operation frequency band extends between 55.4 – 64.8 GHz with a bandwidth of 9.4 GHz considering the internal VCO in *master* mode. The frequency divider has an

output frequency between 4.6 GHz and 5.4 GHz with a total division ratio of 12. Not shown on the figures, the divider output power in this range is found in average -4.7 dBm at 3.3 V which increases by almost 1 dB per 0.3 V increase in supply voltage. The frequency shift due to supply voltage change to 3.9 V is only 100 MHz which is less than 10 MHz at frequency divider outputs. Thus the circuit would perfectly withstand against supply pulling and pushing effects.

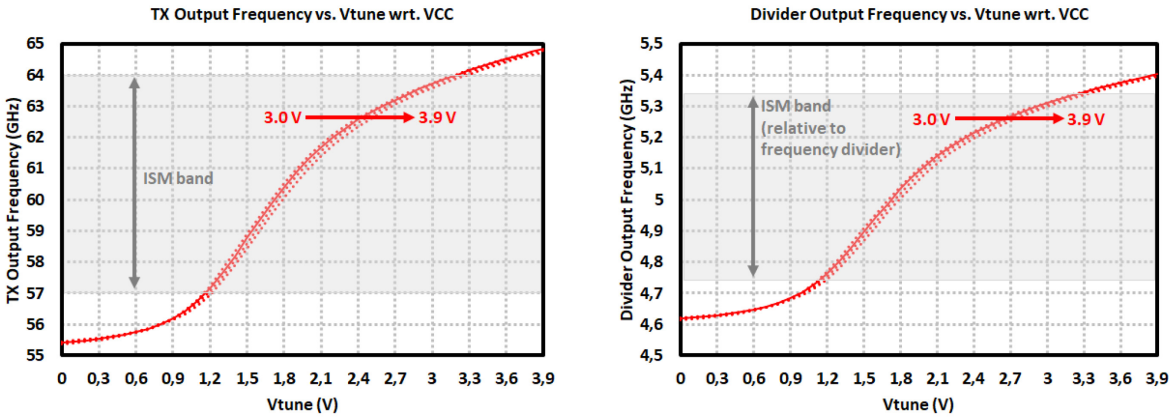

Figure 4.32: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V.

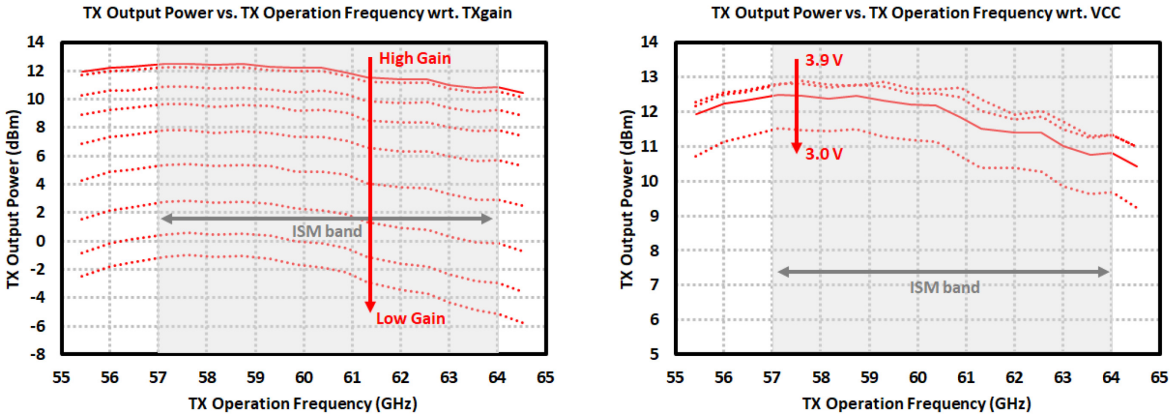

Figure 4.33: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: Tx output power vs. frequency with respect to (*left*) Tx gain control voltages 0 V – 3.3 V and (*right*) changing supply voltages between 3.0 V – 3.9 V.

The graphs in Figure 4.33 draws the Tx output power with respect to many Tx gain options and different supply voltages. According to results, average 12 dBm of output power is achieved at the high gain mode where, with one of the gain tuning mechanisms, the output power could be lowered down to -2 dBm in average across the whole ISM band. The Tx channels could be completely turned off with the help of dedicated enable pins for each channel. For the normal use case where the supply voltage is set to 3.3 V at high gain mode with only one Tx is operational at a

time, the output power curve is quite flat over the whole bandwidth and has an actual bandwidth starting from 52 GHz and extending beyond the measurable range of 66 GHz as seen in Figure 4.39. Such measurement is available thanks to *slave* mode where the internal VCO is off and external LO around 20 GHz is applied from *LOin* pads. The power detectors could observe the Tx output power levels depicted in Figure 4.33 and map them between 1.0 V and 2.4 V within the ISM band (see Figure 4.34). The chip has *LOout* output power of -4 dBm in average. The lower edge of this *LOout* output power curve is observed to be decreasing due to the designed *master* / *slave* switch. However the output levels are already enough to feed the successive *slave* MIMO chips thanks to integrated 20-GHz PAs. Additionally LOout has operation range between 18.5 – 21.6 GHz.

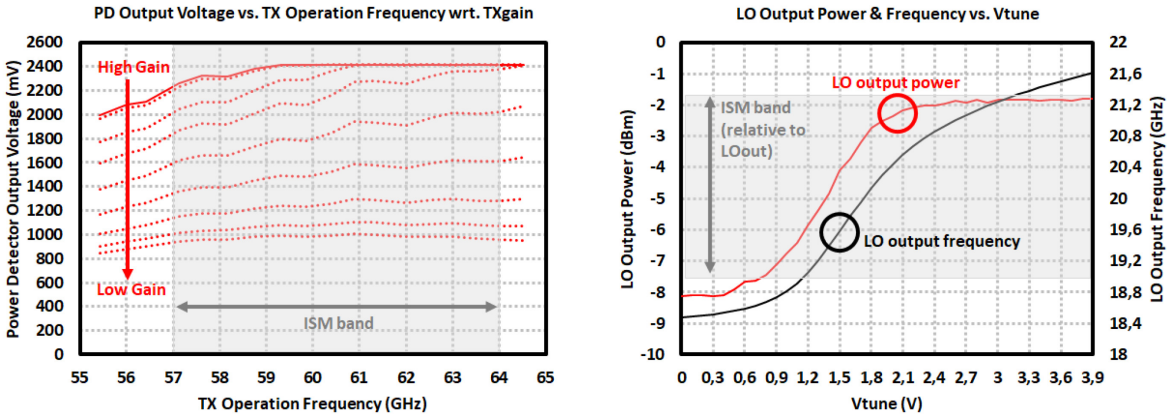

Figure 4.34: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: (*left*) Power Detector output voltage vs. frequency with respect to Tx gain control voltages 0 V – 3.3 V, (*right*) *LOout* output power and frequency vs. VCO tuning voltages.

The Rx channel provides a conversion gain of around 18.5 dB within the ISM Band which is covered as well by its wide 3-dB bandwidth of 9 GHz between 56 – 65 GHz, as shown in Figure 4.35. The quadrature Rx channel has the highest gain while the remaining single-channel Rx sections have 18 dB of average conversion gain. It is seen that whereas the quadrature channel is correctly centered at 60 GHz, the single-ended channels are shifted upper in frequency of about 4 GHz with maximum of 18.5 dB at 64 GHz. They possess much wider bandwidths more than 14 GHz by interpolating the curves for the upper range which is not measurable. With respect to Rx gain control options, the gain could be lowered by maximum 6 dB. The IP_{1dB} measured at I/Q Rx outputs is found to be -15 dBm which is improved to -10 dBm with the operation at low gain mode (see Figure 4.36). If outputs are also characterized for each channel which could be viewed in Figure 4.37. Using these results, the amplitude and phase imbalances in quadrature outputs of Rx channel 1 are found again around 0.7 dB and 10° whereas the differential outputs are aligned correctly. The single-channel differential outputs, on the other hand, experience equal phase and amplitudes.

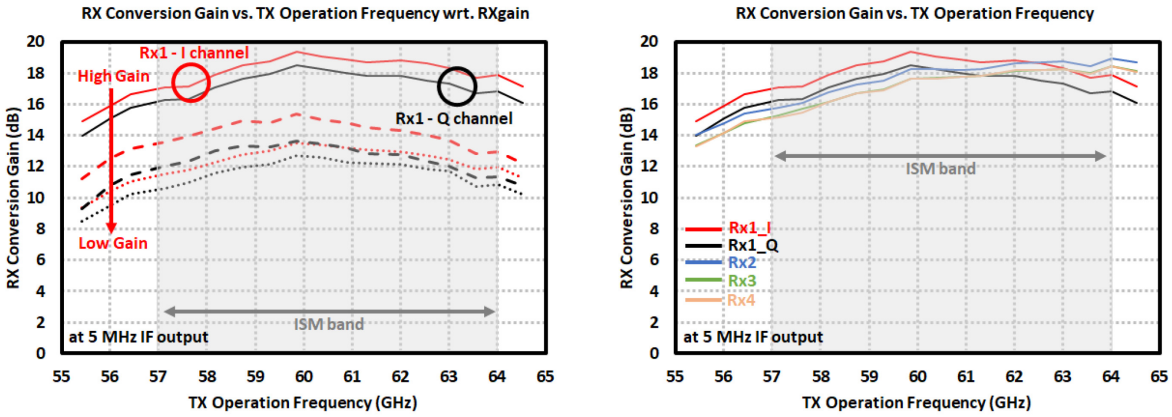

Figure 4.35: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: (*left*) Rx channel 1 conv. gain vs. freq. with respect to Rx gain control voltages, and (*right*) Rx channel conv. gain vs. freq.

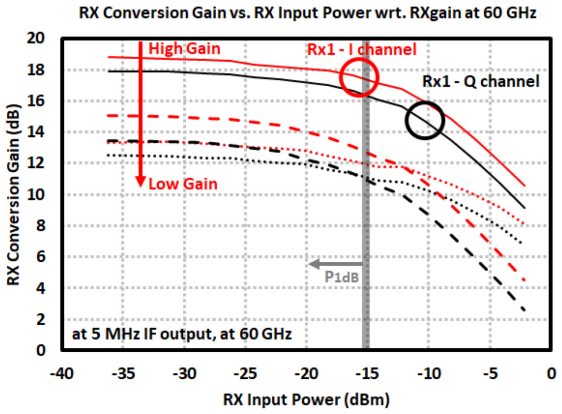

Figure 4.36: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: Rx channel 1 conversion gain vs. Rx input power with respect to Rx gain control voltages.

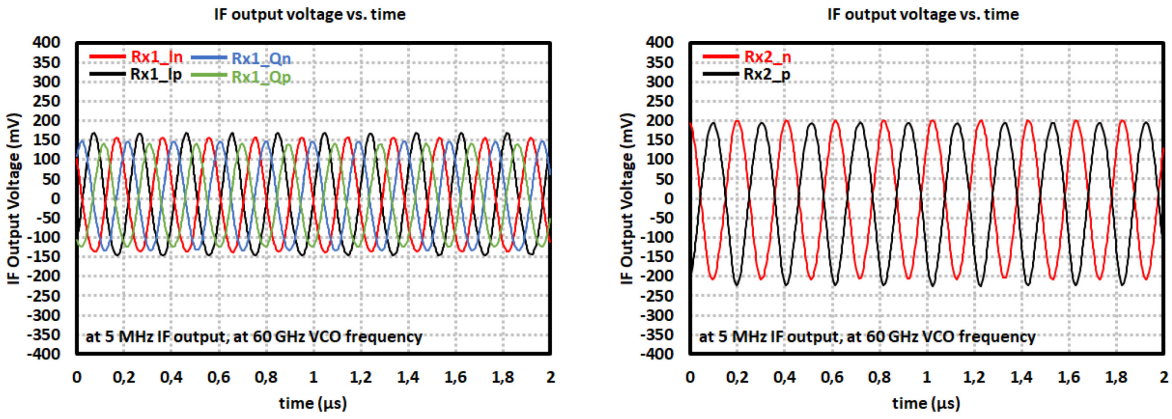

Figure 4.37: Measurement results of the 60-GHz MIMO TRx: 5-MHz IF output voltages at 60 GHz (*left*) from quadrature Rx channel 1, and (right) Rx channel 2.

Measurements are conducted in the case of enabled *slave* mode as well (internal VCO consuming around 62 mA current is switched off). These are illustrated in Figure 4.38 and Figure 4.39 for the Rx and Tx channels. First the required LO input power from *LOin* pad in order to reach the maximum conversion gain is determined which is measured with powers above -13 dBm (only 2 dB less than the maximum). At -3 dBm and above the conversion gain becomes already fixed and maximized at 18.5 dB and gradually decreases from this level to 0 dB gain with inserted power around -23 dBm. With the applied -3 dBm input power at 20 GHz from *LOin*, the gain curves with respect to frequency and applied Rx input power are plotted for different Rx gain control options which have the same characteristic as in the *master* mode.

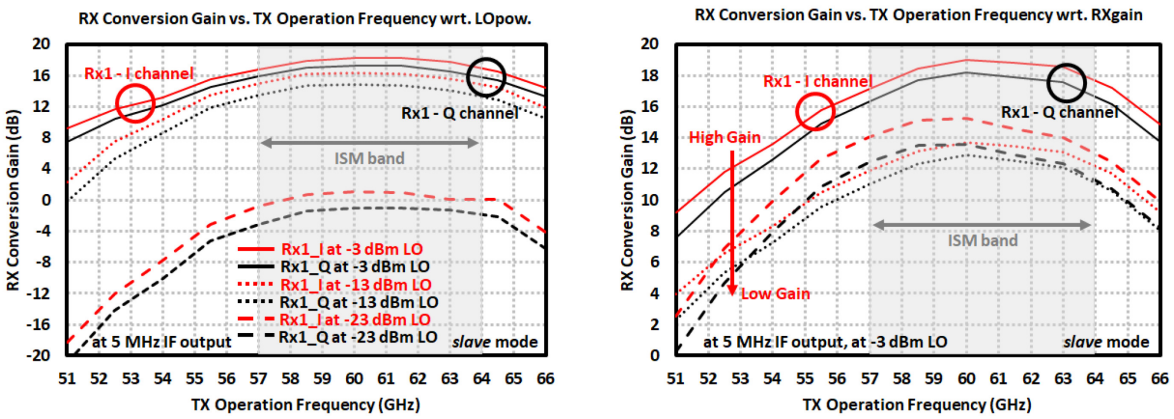

Figure 4.38: Measurement results of the 60-GHz MIMO TRx in *slave* mode where external LO is applied: (*left*) Rx channel 1 conversion gain vs. frequency with respect to applied LO power from *LOin* pad, and (*right*) Rx channel 1 conversion gain vs. frequency with respect to Rx gain control voltages at -3 dBm LO input power.

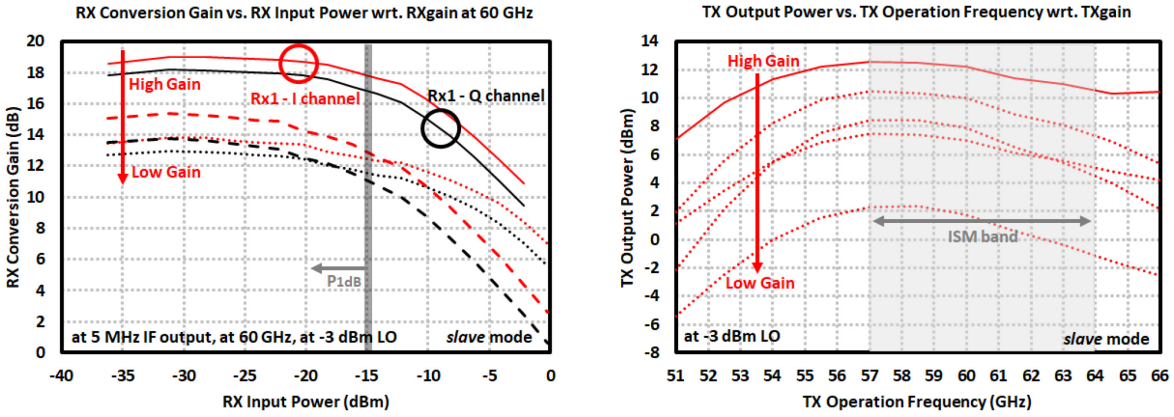

Figure 4.39: Measurement results of the 60-GHz MIMO TRx in *slave* mode where external LO is applied: (*left*) Rx channel 1 conversion gain vs. Rx input power with respect to Rx gain control voltages at -3 dBm LO input power, (*right*) Tx output power vs. frequency with respect to Tx gain control voltages at -3 dBm LO input power.

Finally the Tx output power is maximized around 12.5 dBm at 57.5 GHz with an average output power of 12 dBm over the ISM band. As mentioned previously, the Tx channel has a 3-dB bandwidth of more than 14 GHz starting from 52 GHz and extending beyond 66 GHz. In Figure 4.40, the phase noise characteristic of 5-GHz frequency divider could be seen which is around -108.3 dBc/Hz at 1 MHz offset (-89.8 dBc/Hz at 100 kHz and -131.8 dBc/Hz at 10 MHz) which translates into a VCO phase noise of -96.3 dBc/Hz at 1 MHz offset.

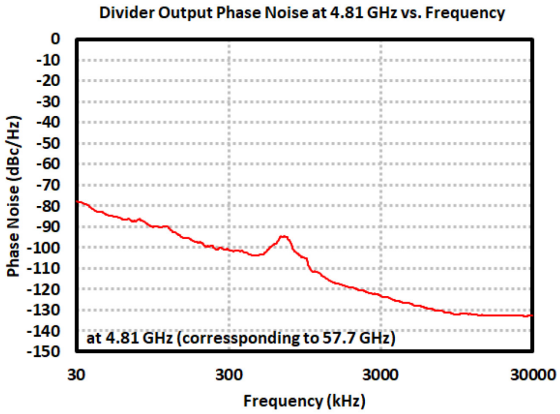

Figure 4.40: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: Frequency Divider phase noise at 4.81 GHz (corresponding to Tx operation frequency of 57.7 GHz).

4.6 Summary of the Measurement Results

A summary of the measurement results belonging to important parameters of each TRx is shared in the below Table 1. As highlighted in the measurement results, it could be deducted that high performances are obtained from each chipset with high output power and high operation range which they cover a range more than the defined ISM bands. This would allow improved detection range and range resolution while the integration of multiple channels, especially in MIMO version, greatly benefit the angular resolution.

Compared to simulation results discussed in Section 3.6, the expected transmitted output powers from the Tx parts of 60-GHz TRM and TR2 are recorded around 10 dBm / 16 dBm which are measured quite close to these levels performing around 8.5 dBm / 14.5 dBm. The MIMO version has around 4 dB less output power compared to simulations and reached 12 dBm. Such reduction in the MIMO chip could be due to a decrease in the expected tripler output power which immediately affects the arrived power at the PAs in Tx after the bulky LO signal distribution network. On the other hand, the output powers in 122-GHz chips decrease greatly by more than 5 dB. This emanates from weaker VCO signal arriving at the PA, general modeling errors of transistors at such high frequencies and mismatches between sub-blocks. Yet the achieved output levels are still

acceptable for many applications, and as will be discussed in the later sections, high performance FMCW measurements are successfully realized with these chips.

Table 1: Summary of the measurement results of fabricated TRxs

Fabricated Chipsets	TR2 60	TR2 122	TRM 60	TRM 122	MIMO 60
Number of Tx / Rx channels	1 / 1	1 / 1	1 / 2	1 / 2	4 / 4
Supply voltage, VCC (V)	3.3	3.3	3.3	3.3	3.3
Current Cons. (mA) at 3.3 V	183	282	171	152	353 (TDM)
VCO operation frequency (GHz)	55.5 – 65.1	118.9 – 126.3	55.6 – 65.6	119.2 – 126.6	55.4 – 64.8
VCO freq. tuning bits (#)	3	2	3	4	3
VCO phase noise at 1 MHz (dBc/Hz)	-100.3	-95.5	-100.5	-95.5	-96.3
VCO tuning sensitivity (GHz/V)	2.462	1.897	2.564	1.897	2.410
VCO pushing in ± 0.3 V (MHz)	± 100	± 300	± 100	± 90	± 100
Freq. divider frequency (GHz)	1.73 – 2.03	1.87 – 1.97	1.74 – 2.05	1.86 – 1.98	4.62 – 5.40
Freq. divider division ratio	32	64	32	64	12
Freq. divider output power (dBm)	-10	-8	-12.5	-8	-4.7
Tx output power at VCC, avg. (dBm)	14.5	2	8.5	-1.3	12
Tx adjustable output power Power range (dBm) – (dBm)	✓ 14.5 – 2	✓ 2 – (OFF)	✓ 8.5 – (-11.5)	✓ (-1.3) – (-11.3)	✓ 12 – (OFF)
Tx 3-dB bandwidth (GHz) Bandwidth range (GHz) – (GHz)	> 10 57.5 – (> 65.5)	> 7.4 (> 118.9) – (> 126.3)	> 10 (< 55.6) – (> 65.6)	> 7.6 119 – (> 126.6)	> 14 52 – (> 66)
Rx conversion gain, avg. (dB)	21	12	14	7	18
Rx adjustable gain Gain range (dB) – (dB)	✓ 21 – 8	✓ 12 – 6	✓ 14 – (-2)	✓ 7 – 1	✓ 18 – 12
Rx 3-dB bandwidth (GHz)	> 10 55.5 – (> 65.1)	> 7.4 (> 118.9) – (> 126.3)	7 58 - 65	> 7.6 119 – (> 126.6)	9 56 – 65
Rx SSB noise figure, simulated (dB)	8.6	10.5	14.4	16.3	8.6
Rx IP_{1dB} (dBm)	-14	-15	-8	-9	-15
IF frequency range (MHz)	10	10	10	10	10
IF I/Q amplitude imbalance (dB)	±1	±1	±1	±1	±1
IF I/Q phase imbalance	±10°	±10°	±10°	±10°	±10°
Die area (mm^2)	1.46 x 1.06	1.54 x 0.92	1.42 x 0.84	1.35 x 0.76	2.16 x 2.39

5 Antenna Design, IC Packaging and Interconnect Concepts

In this chapter, different antenna and package designs, which are developed for the tests of fabricated chips, are discussed. In this context, antennas for different applications are designed on high frequency substrates as a cheap and high performance solution rather than on-chip integrated antennas which would boost the fabrication costs and reduce the total directivity due to this limited area. On the other hand, Lens structures with different sizes are designed and implemented on top of these on-board antennas to attain higher gain and more focused radiation pattern. Only quite few versions include integrated on-chip antenna, however their gain and beamwidth performances are increased with stacked lenses. For many of the transceiver versions, between the chip and antenna, wirebond interconnects are utilized necessitating compensation networks whereas, for the rest, solder-bump interconnects are implemented. Especially for the ones including wirebonds, a careful optimization process is required considering the wirebond and PCB trace width tolerances and its effect on the radiation pattern and reflection losses.

Furthermore in order to realize complete products, package solutions should be implemented in the end as well. Having the structures operating at high frequencies, the degraded performances resulted from interconnects prevent the usage of simple QFN types. Solder bump method offers a good solution in getting lower interconnect inductance and not decreasing the operation bandwidth, yet it requires much larger chip area due to wider pad requirements and might be applicable especially for chips having lower power consumption owing to heat dissipation problem. Since the silicon back side is exposed, compared to the classical wirebonding technique where the chip substrate sits on a ground plane, heat dissipation inside the package may cause the IC fail operating. However it provides many advantages in high frequency sections. Instead of these, PCB based package designs are adopted where the wirebond compensation networks are integrated inside the package. Such concerns are detailed in this chapter, and together with different antenna and package designs, complete product candidates especially for 60-GHz transceivers are proposed.

5.1 PCB-Based Antenna Concept of 60- and 122-GHz ICs

For the initial FMCW radar tests with 60- and 122-GHz monostatic TRx chips, simple on-board 2 x 2 differential microstrip patch antennas shown in Figure 5.1 and Figure 5.2 are designed. Complex structures are avoided because of the manufacturing tolerances which could degrade the overall radiation characteristics anyways.

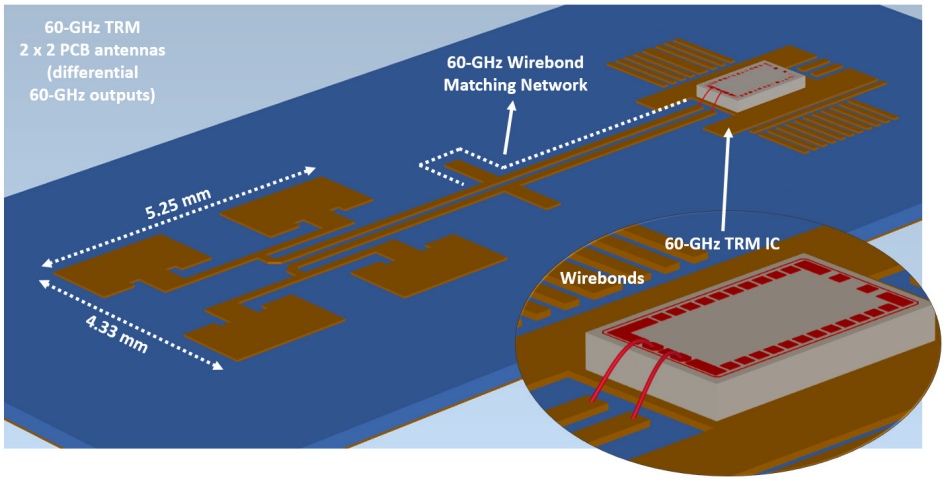

Figure 5.1: PCB antenna concepts of 60-GHz TRM chips including wirebond compensation network.

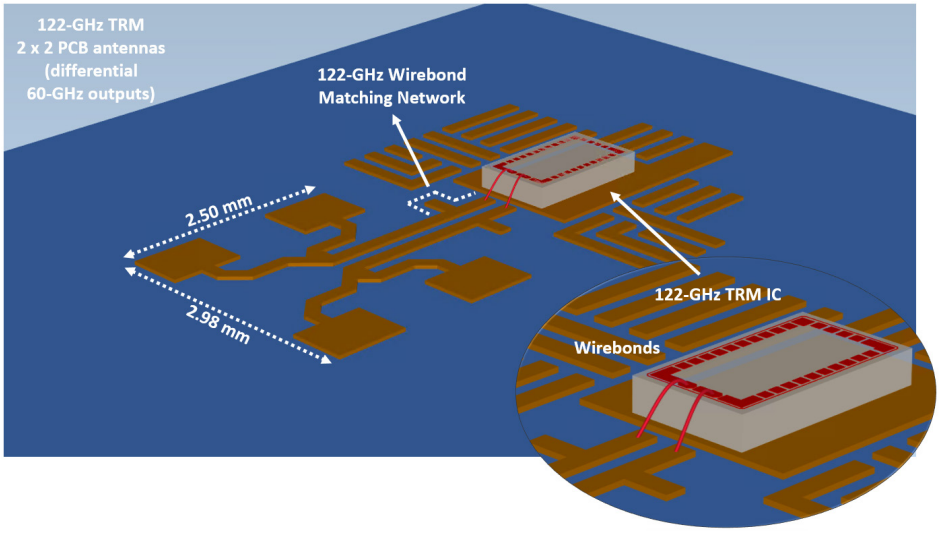

Figure 5.2: PCB antenna concepts of 122-GHz TRM chips including wirebond compensation network.

The structure is limited by 4 antenna elements in order to get the best compromise between antenna directivity and beamwidth due to higher number of antenna elements would mean sharper beams which could cause measurement difficulty. Since the antennas are of patch type which have a close ground plane beneath, quite narrow band that is tried to be centered around the frequency band of interest is achieved. Although there exists patch antennas or other kinds with wider

bandwidth which are obtained by removing or shaping the bottom reflector, such ground plane is as well necessary since the final evaluation board would be stacked on top of the radar baseband board in the end that might include such a ground plane quite apart from the radiating patch and hence ruin the radiation pattern. The antennas are realized on Astra MT77 material having a measured dielectric constant (ε_r) of 3 and a tangent loss ($tanD$) of 0.0017. The 60-GHz version is built on 254 µm thick board whereas the 122-GHz antenna uses 127 µm thickness, which are then stacked on 1 mm-thick FR4 board for mechanical robustness. Boards with different thicknesses guarantee better radiation efficiency at the specified frequency ranges hence decreasing the losses in substrate.

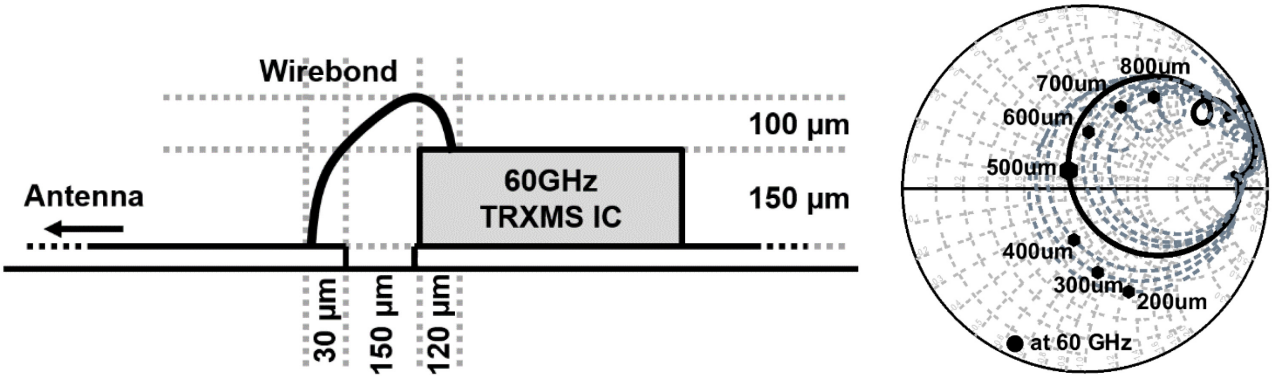

Figure 5.3: Wirebond drawing and effect of wirebond length on return loss [18].

On the other hand the ICs are connected by wirebonds bringing additional inductances of 350 pH – 450 pH depending on the chip thickness and distance between the RF pads and the antenna connecting part. Thus couple ways to eliminate the effect of wirebonds on return loss are investigated and methods like stub matching [16] – [18], [56] and L-C-L type matching [11], [61] (chip – wirebond – small patch on board – wirebond – antenna) networks are brought forward. Quarter-wavelength matching [58] is neglected since insertion loss increases dramatically to compensate for such high inductances which require relatively long successive matching sections. Moreover CPW matching is not a preferred solution as well due to trace width / spacing limitations and tolerances such that the matching cannot be guaranteed while the board complexity increases. In other respects, in spite of the narrow band nature, mainly the stub matching is selected thanks to less number of wirebonds required (compared to L-C-L type [11], [61]) while considering the fact that antennas are only necessary for FMCW radar functionality, hence high performance is not expected. On PCB side, the minimum possible trace / spacing width is limited to 100 µm which comes with tolerances about % 20. Such width already limits the transmission line impedances to 90 Ω and 120 Ω, respectively for substrates with 127 µm and 254 µm thicknesses, thus raising difficulties in antenna matching networks. Specifically for L-C-L type matching, the capacitive pad on board, whose sizes are generally quite close to this limit, might be over-etched and degrade the matching characteristics. Therefore such tolerances should be kept in mind while designing the

antenna and compensation networks. This compensation network could be designed inside the chip, solving such issues, however chip measurement process gets complicated this time.

As in the PCB manufacturing process, interconnects have tolerances as well especially considering the hand-made wirebonds. However the wirebonds are made as short as possible by placing the chip quite close to the antenna, which these tolerances could be eliminated up to some point. In Figure 5.3, such drawing of the wirebond is viewed which is implemented in simulation environment and verified by the 3D EM simulations as well [18]. Taking these tolerances into account, wirebond effect together with antenna and a dedicated compensation network for certain wirebond length is simulated with respect to changing lengths / inductances. Looking at the same figure, it could be implied that the return loss becomes acceptable for wirebonds having lengths between 450 – 600 µm (giving proportional inductance values) at 60 GHz. At 122 GHz, wirebonds become more problematic, hence higher accuracy should be provided.

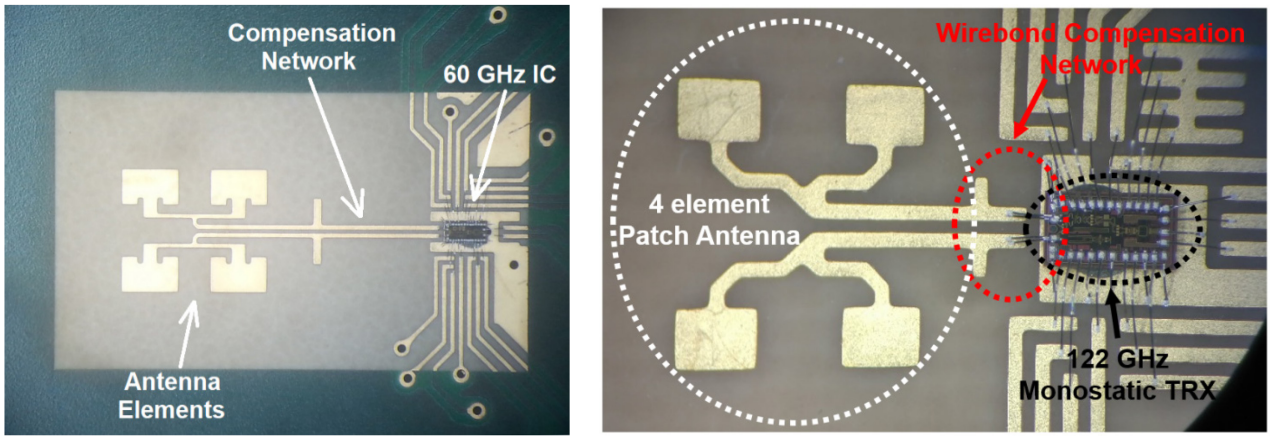

Figure 5.4: Manufactured evaluation boards with 60- / 122-GHz TRM chips and PCB antennas [15], [18].

Since the chips have differential RF outputs, differential antenna structures are adopted as seen in Figure 5.1 and Figure 5.2. The 60-GHz antenna version is composed of inset-fed elements to better optimize the matching, whereas the feeding is at the edge for 122-GHz antenna as shown in Figure 5.4 [15], [18]. The single element design is based on generic rules for antenna width / length where the length is almost matched to have radiation centered at 60- / 122-GHz while the width is used to tune the antenna impedance. This single patch could perform with approximately 8 dBi gain which would theoretically increase by 6 dB with the addition of three more patches, hence 14 dBi of gain is achievable (in case of perfectly matched structure). Considering the losses from connecting lines, power divider, compensation network and the mismatch, a reduced gain about 12 dBi would be obtained. According to simulation results of these 2 x 2 patches, the antenna has a maximum directivity of 13.5 / 12.9 dBi centered at 60 / 126 GHz respectively for 60- and 122-GHz versions. The 3-dB beamwidth and radiation efficiency are found as ±19.5° / ±18° and % 92 / % 95. The input impedance seen by these antennas should be matched to differential 100 Ω by utilizing the dedicated wirebond compensation networks composed of open-stub sections. These sections are matched at the frequencies of interest, thus behave as dipole antennas at the same

time, which might result in distortion in radiation pattern if not carefully designed. Together with these compensation networks, results are updated as shown in Figure 5.5 / Figure 5.6 where the total directivity is simulated to be 13 / 12.4 dBi at 60- / 122-GHz.

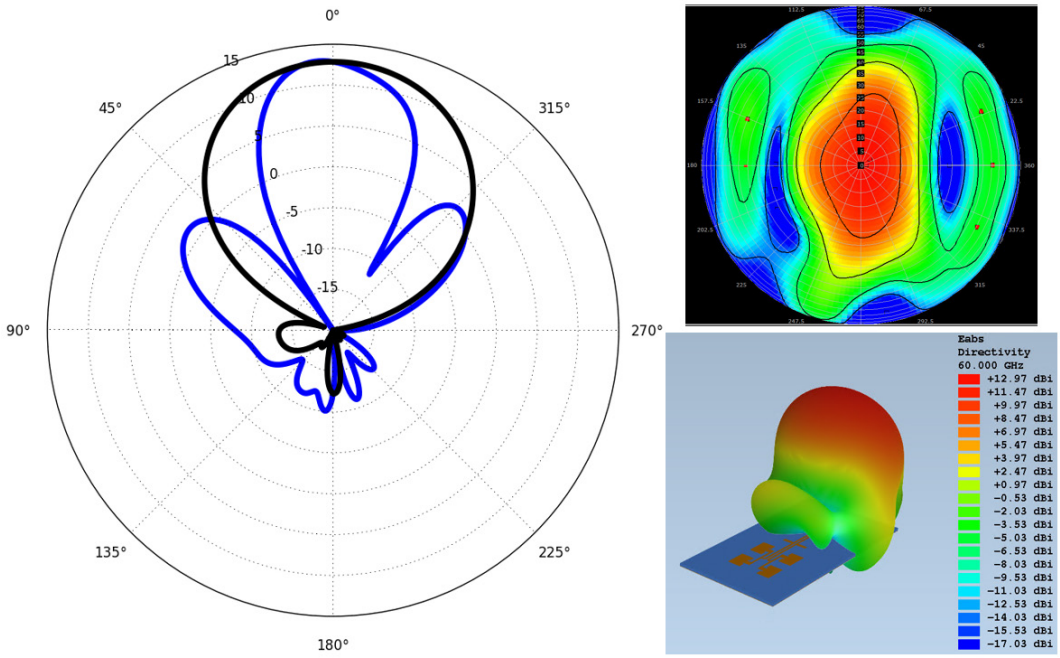

Figure 5.5: Simulation results of PCB antenna of 60-GHz TRM chip including wirebond compensation network.

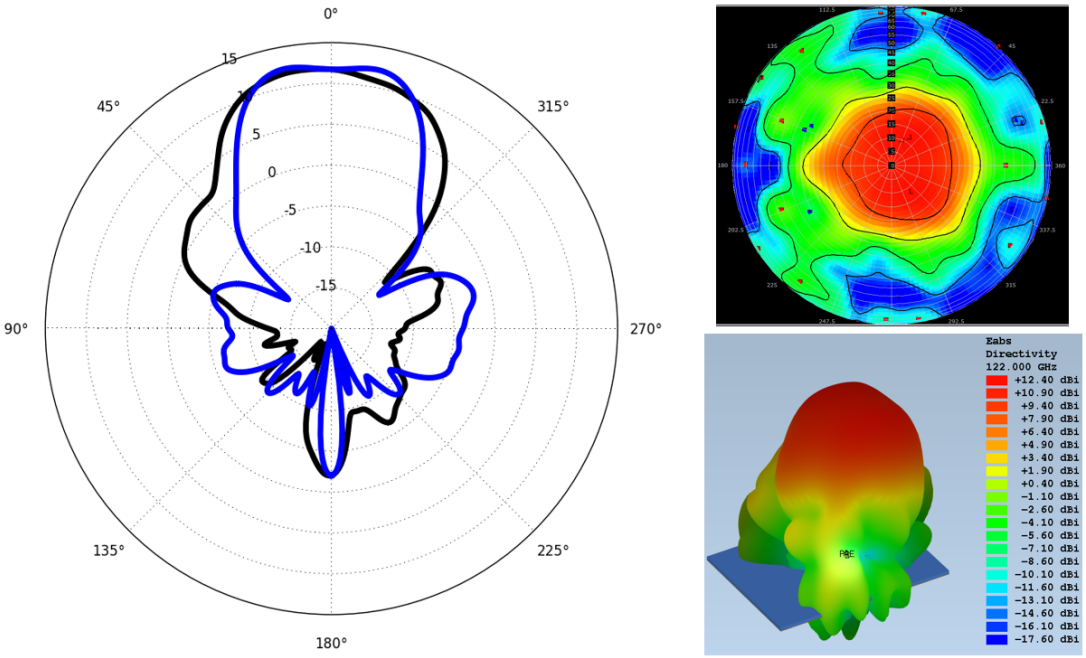

Figure 5.6: Simulation results of PCB antenna of 122-GHz TRM chip including wirebond compensation network.

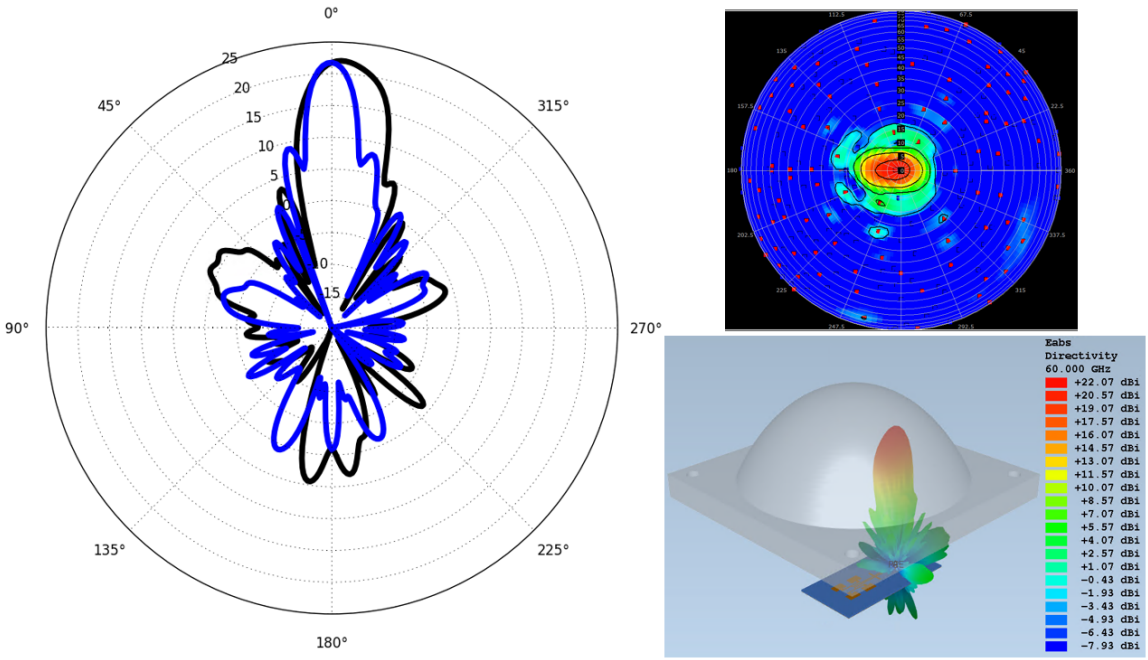

Figure 5.7: Simulation results of PCB antenna of 60-GHz TRM chip including HDPE plastic lens at 1.5 cm.

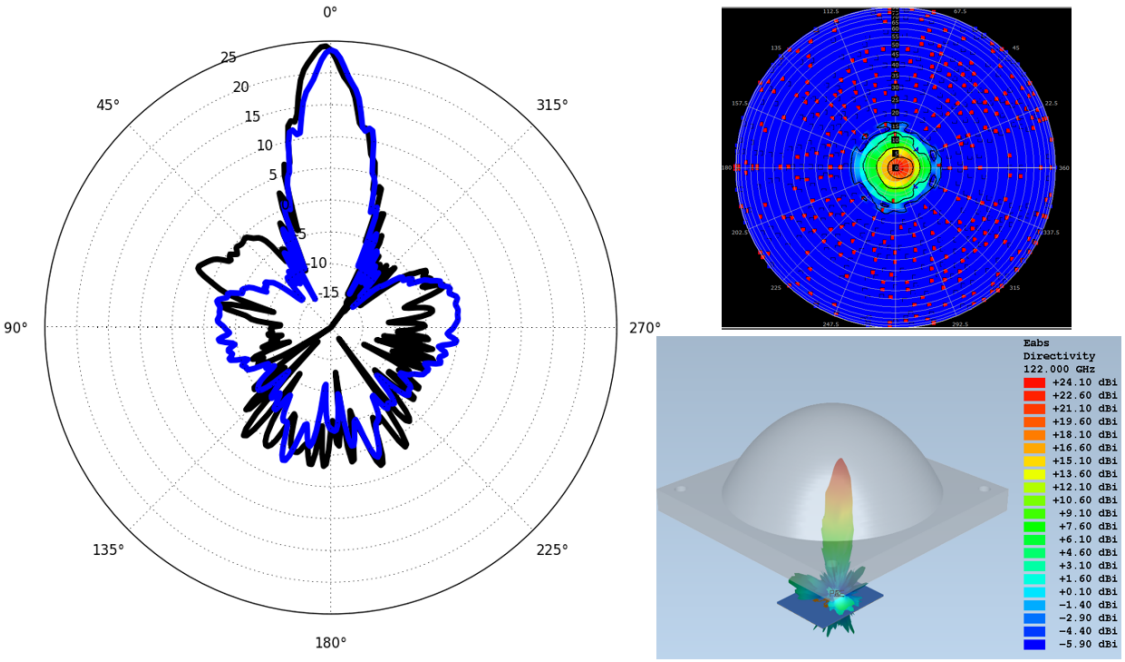

Figure 5.8: Simulation results of PCB antenna of 122-GHz TRM chip including HDPE plastic lens at 1.5 cm.

In order to detect obstacles at much farther distances, the antenna gain should be significantly increased which is generally realized by a lens on top of the antenna [12], [15] – [18], [25], [28], [44], [60], [78]. Even though much larger lens structures are normally utilized, the real-time tests of both 60- and 122-GHz radars are conducted with 3 cm x 3 cm printed plastic HDPE (High-Density Polyethylene) lens with ε_r of 2.75 and focal point of 1.5 cm at 60- / 122-GHz. Full simulations

including the antenna and lens are completed and the results are depicted in Figure 5.7 and Figure 5.8 for 60-GHz and 122-GHz Lens integration respectively.

Based on the simulated data, lens helped decreasing the beamwidth to 8° (±4°) while increasing the directivity to 22 / 24 dBi. This gain improvement theoretically means of an increase in detectable range by 3.5 / 4 folds considering the 44 / 48 dBi total antenna gain in Friis equation respectively for 60- / 122-GHz versions (radiated signal travels two times the distance), even if all the other parameters are fixed. Furthermore the side lobes, especially caused by the open-stub is eliminated since the energy is collected and directed by the lens.

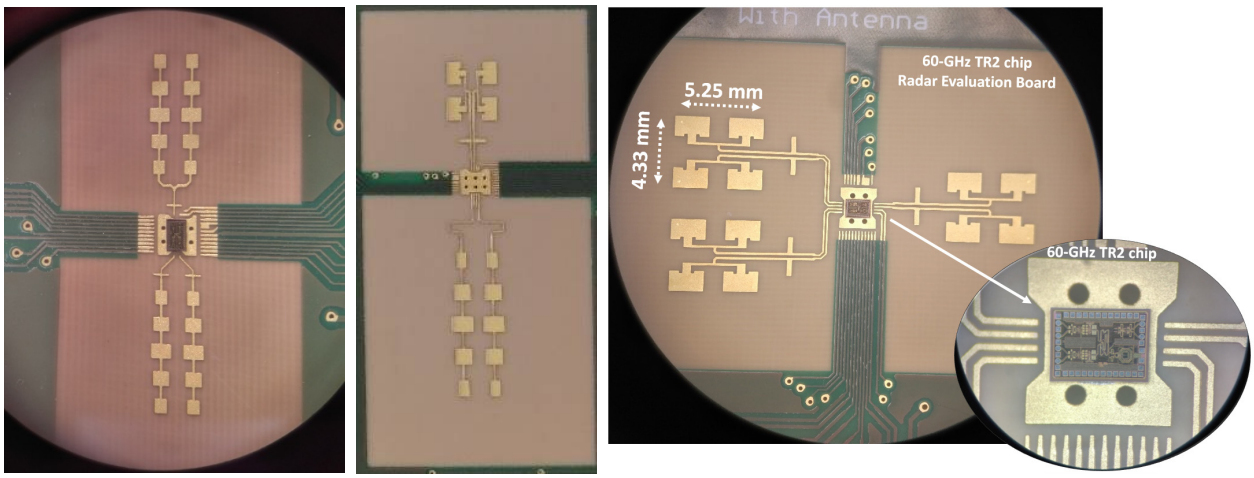

Figure 5.9: Manufactured evaluation boards and PCB antennas with (*left*) 122-GHz TR2 (1 x 5 patch array), (*middle*) 60-GHz TR2 (1 x 5 patch array), (*right*) 60-GHz TR2 (2 x 2 patch array).

For the multichannel chips, the stack-up remains the same but the antenna structures are changed to adapt the new functionalities. The simplest version, TR2, has two Rx antennas separated by $\lambda/2$ in order to be able to utilize the final demonstrator as a smaller MIMO kit. Therefore 1 x 5 series fed patch array (see Figure 5.9) is built so that the required spacing is conserved. Such certain distance requirement comes from the MIMO theory suggesting that the positioning of Tx and Rx antennas on board should conform the convolution of single element radiation patterns such that the created virtual array would have $\lambda/2$ spacing as well [88]. This distance could be varied depending on the application, however side lobes emerge in the virtual array in a regular MIMO operation. Wirebond compensation network is implemented as well. In simulations, as shown in Figure 5.10, the 1 x 5 series fed antenna achieves 11.5 dBi of directivity with 3-dB beamwidth of 17° in azimuth plane. The simulated radiation efficiency is around % 65. Same architecture is adopted for the 122-GHz version and similar results are obtained. On the other hand, another evaluation board version which adopts the same Tx antenna on Rx channel as well is designed (see Figure 5.10). Using the simulations in Figure 5.11, the 2 x 2 patch array antenna achieves 13.6 dBi directivity at 60 GHz.

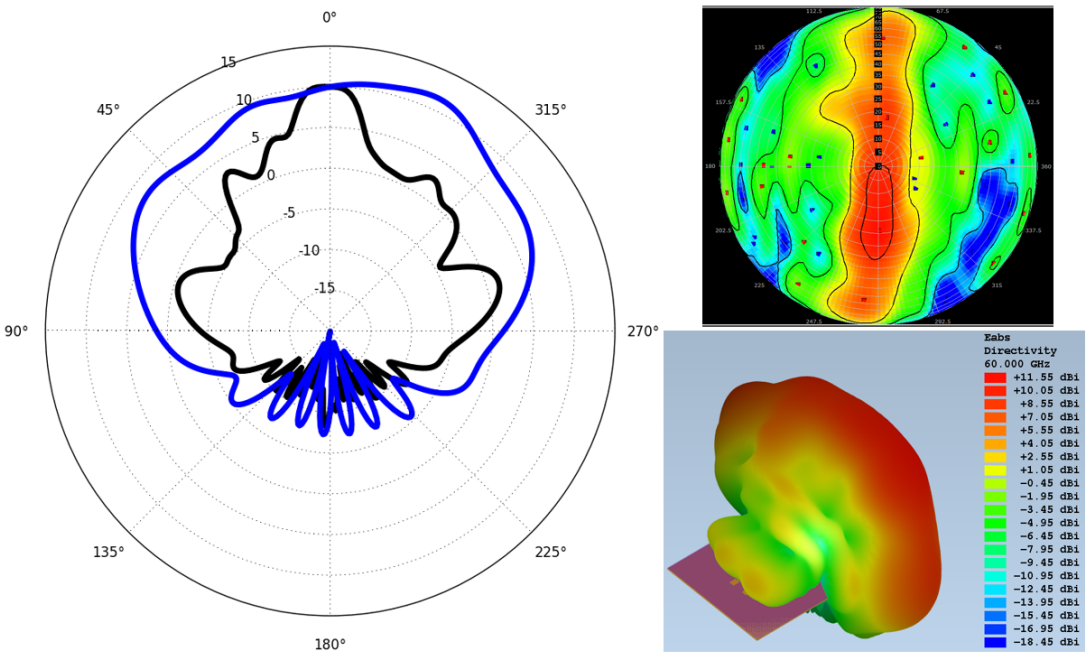

Figure 5.10: Simulation results of PCB antenna (1 x 5 patch array) of 60-GHz TR2 chip.

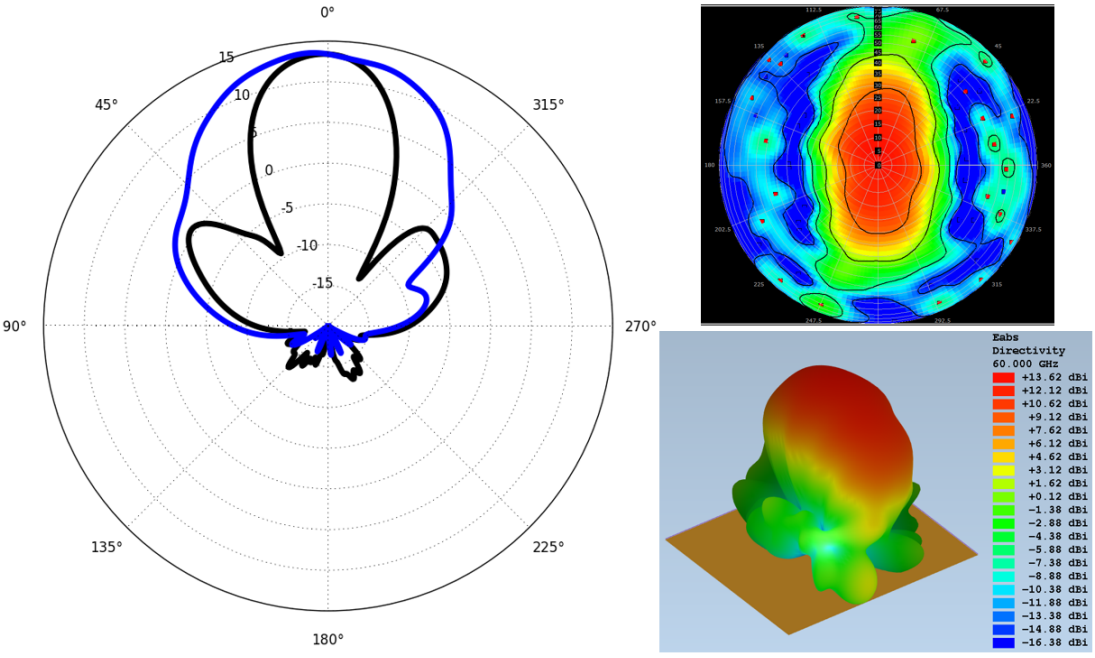

Figure 5.11: Simulation results of PCB antenna (2 x 2 patch array) of 60-GHz TR2 chip.

60-GHz MIMO antenna is designed in the same way with the 1 x 5 series fed patch array. The antenna spacing between each Rx channel is kept at $\lambda/2$ whereas the Tx channels are separated by 2λ. This notion of one-dimensional virtual antenna array is illustrated in Figure 5.12. Having 4 Rx and 4 Tx channels would result in a total virtual array length of 16 elements. The antennas could be arranged as in Figure 5.13 and two-dimensional virtual arrays could be achieved which

enables scanning in the other dimension as well. Depending on the application requirements, antenna placement and the resulting angular resolution could be altered [3], [38], [88].

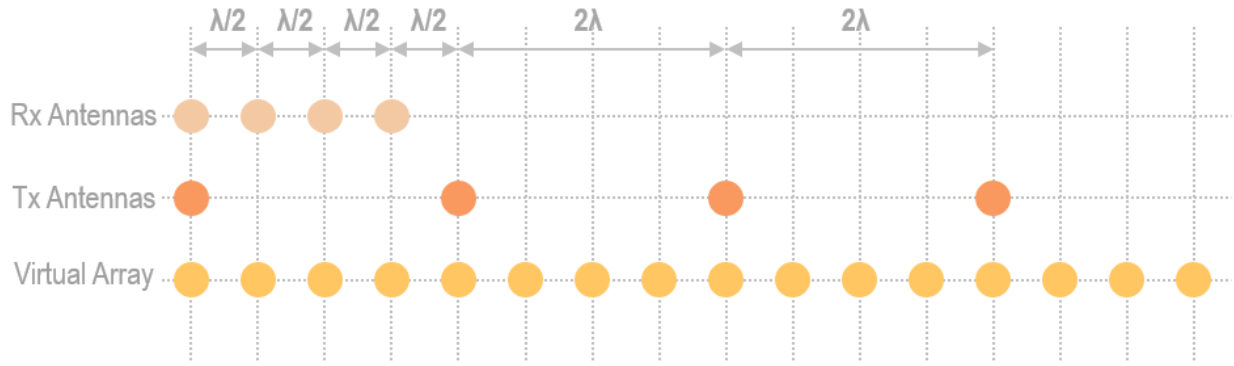

Figure 5.12: Illustration of one-dimensional 1 x 16 MIMO virtual array formation.

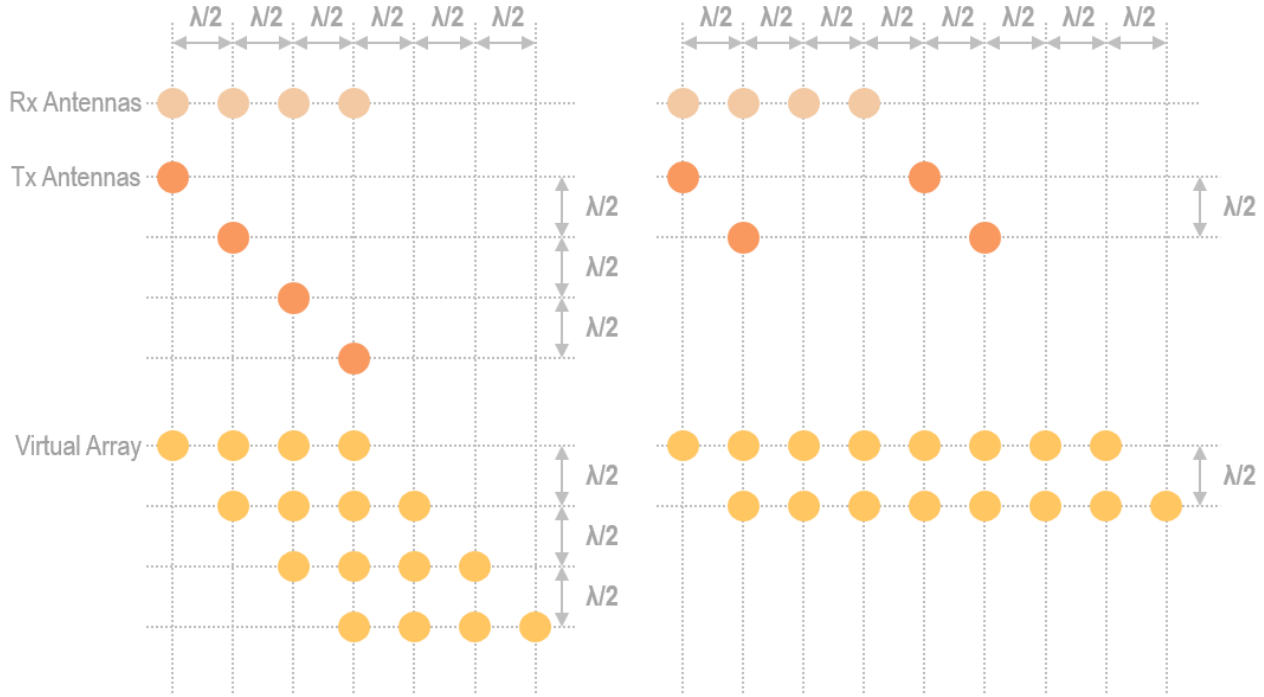

Figure 5.13: Illustration of two-dimensional 4 x 4 and 2 x 8 MIMO virtual array formations.

All these configurations are implemented on the same Astra material (254 µm thickness) with antennas kept same but the matching networks are optimized accordingly to excite the antennas with same phases. The radar boards including antenna arrays are visible in Figure 5.15. In order to protect the chip and wirebonds, a molding material with the process named as GlobTop is deposited on top of the chips. According to simulation results of the MIMO channel having 1 x 16 virtual array, Rx and Tx antennas together with the matching networks have directivities of 12.7 dBi and 12.8 dBi at 60-GHz. The 3-dB beamwidth is simulated as 17° in the E-plane.

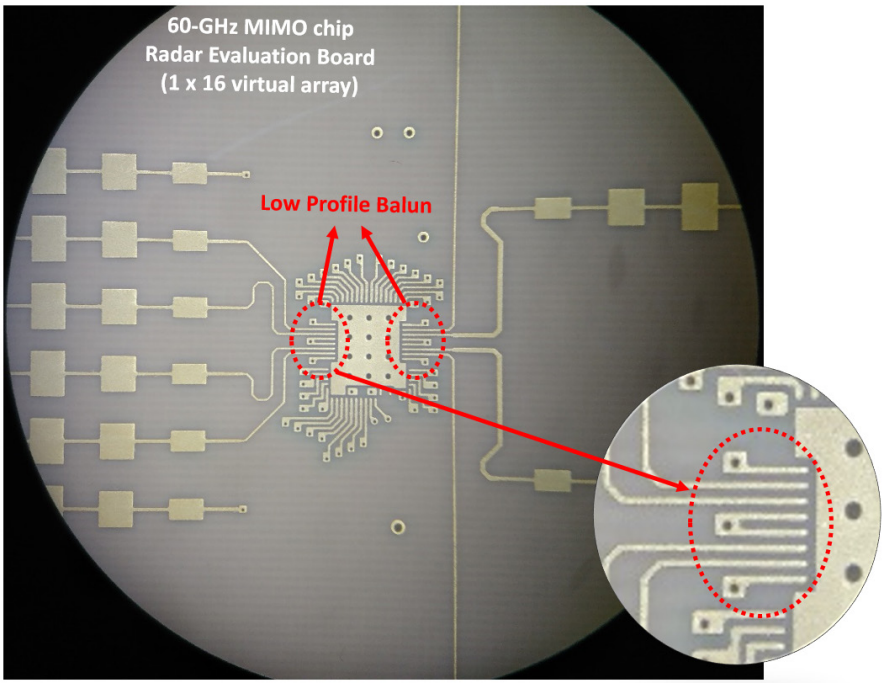

Figure 5.14: 60-GHz MIMO radar evaluation boards highlighting the PCB-based balun.

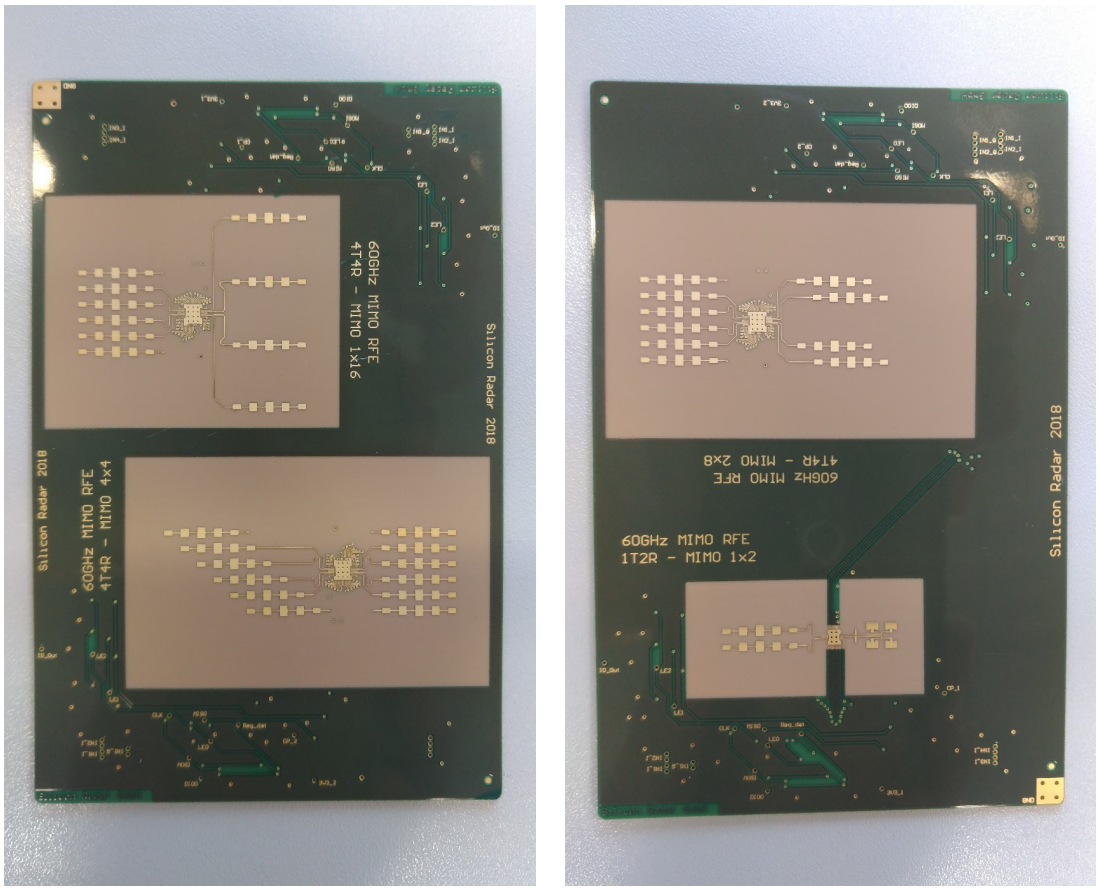

Figure 5.15: 60-GHz MIMO radar evaluation boards including antenna arrays for different virtual arrays.

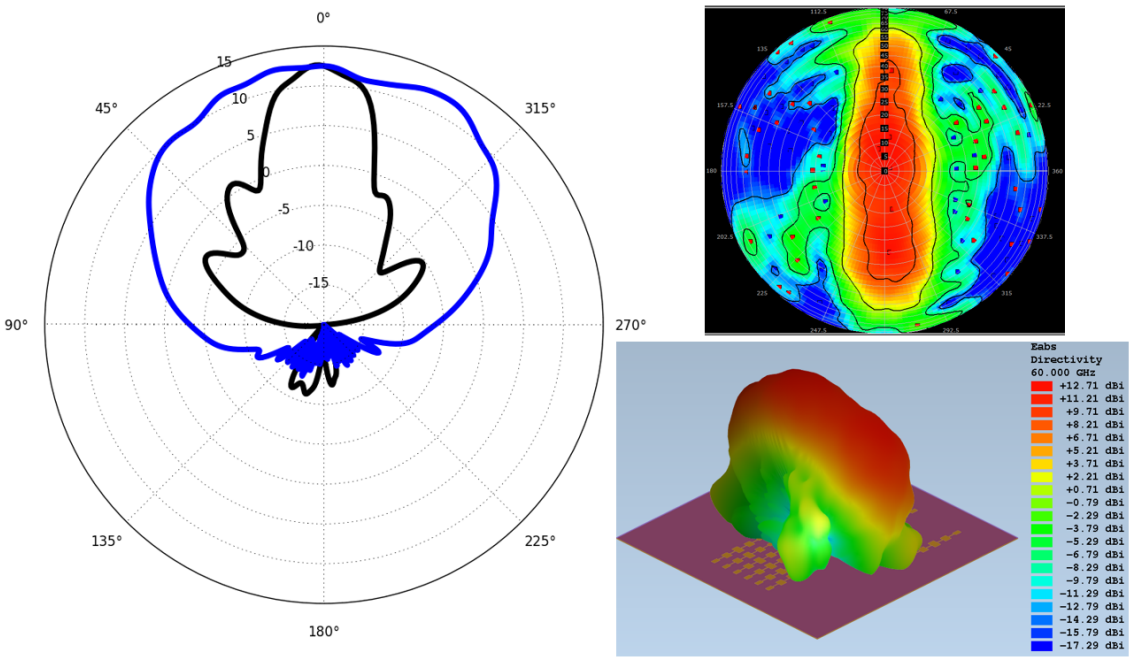

Figure 5.16: Simulation results of PCB antenna (1 x 5 patch array) of 60-GHz MIMO chip (Rx1 is excited).

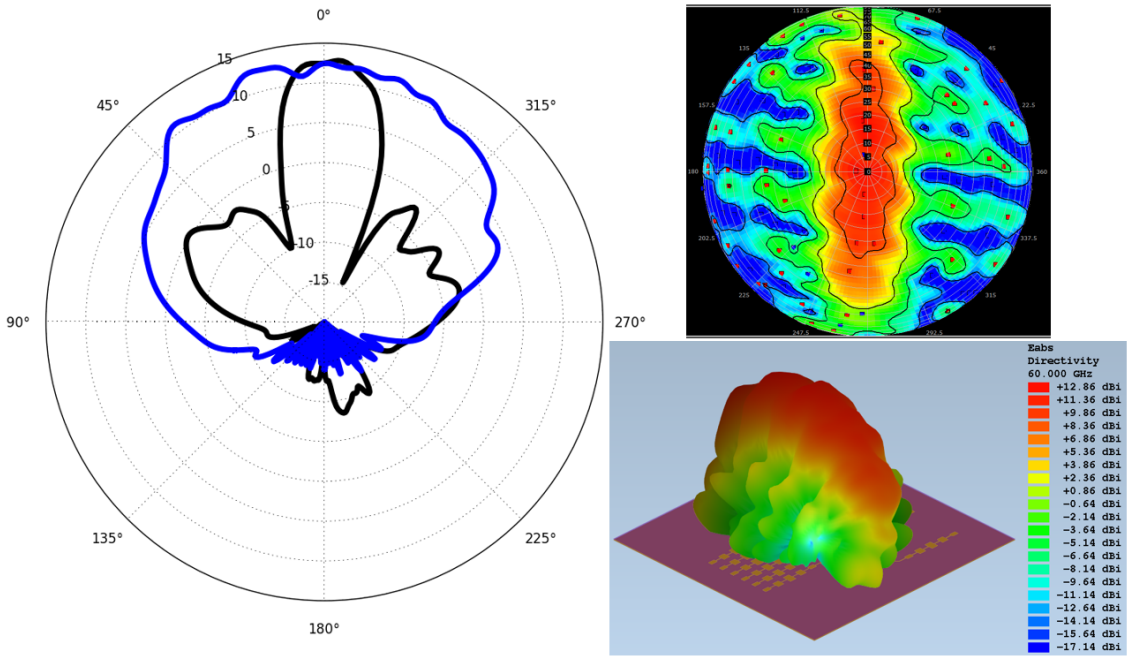

Figure 5.17: Simulation results of PCB antenna (1 x 5 patch array) of 60-GHz MIMO chip (Tx1 is excited).

Another important measure of MIMO antennas is the isolation between antennas which is generally calculated by evaluating envelope correlation coefficient (ECC) between each antenna element. This measure tells how correlated each antenna are. In case of exactly the same radiation patterns with same polarizations, this coefficient becomes 1 which states that the antennas are correlated. A rule of thumb for good MIMO antenna construction is said to be resulting in ECC

of below 0.3. Having observed from the simulation results shown in Figure 5.18, on which the isolation between each 4 Tx and 4 Rx antenna are highlighted, all the coefficients are found below 0.25 within the ISM band. On the other hand the simple S-parameters would reflect the same results as well. Yet the main coupling between Tx and Rx channels would result from the antennas.

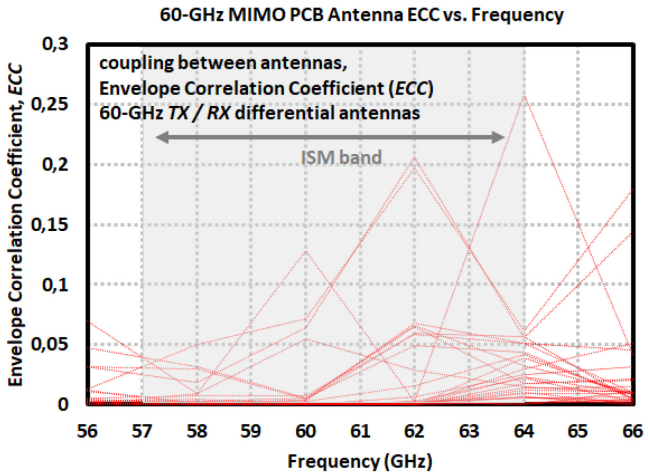

Figure 5.18: Simulation results of PCB antenna (1 x 5 patch array) of 60-GHz MIMO chip showing MIMO Envelope Correlation Coefficients (*ECC*) between each antenna.

5.2 Silicon Package Concept of 60- and 122-GHz TRM ICs

A different packaging solution is implemented as well which requires on-chip integrated antenna and a stacked lens for the TRM transceivers. To realize such configuration, antennas are designed to radiate from the back side of silicon, not as usual as having a ground plane beneath as a reflector. Then the chip could be glued on a silicon-lens having the same dielectric properties of the chip substrate material so that not much loss is expected compared to the case in wave travelling inside different dielectrics. Additionally, because the integrated antenna greatly experiences substrate loss and the silicon area is quite limited, the antenna efficiency and directivity are much lower compared to on-board antenna. Therefore silicon-lens would boost the gain and provide many advantages in radar systems [46], [73].

Antenna integration on chip could be quite costly due to large area usage. In order to reduce the chip area, dipole structures are designed both in 60- and 122-GHz versions and placed at the edge of chip without any additional spacing from the substrate edge. Such placement could normally cause a beam tilt in certain direction due to insufficient substrate area beneath the antenna, however the correct placement of silicon-lens would eliminate such effect. The radiation center of antenna is adjusted on the silicon-lens, so the lens center is a bit shifted to achieve an aligned radiation pattern.

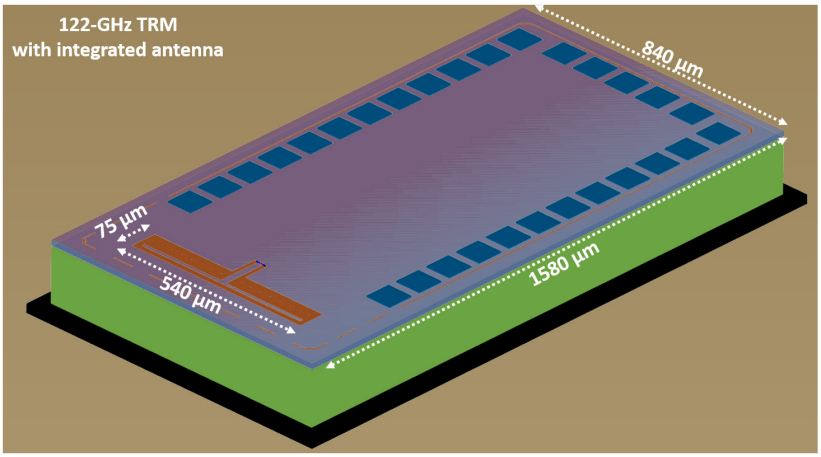

Figure 5.19: 122-GHz TRMant chip.

These folded dipole structures, as shown in Figure 5.19, have lengths of 740 / 540 µm at 60- / 122-GHz frequencies. They reach simulated directivity of 7.1 dBi gain (see Figure 5.20) which is quite insufficient compared to what is achievable from on-board antenna. A lens integration would boost the gain and radar measurement range could be improved. Since the backside of chip is exposed and heat conduction would be poor, the lens mounted on board and the chip mounted on this lens are stacked with high heat conductivity glue (electrically low conductive) so that the heat could be transferred directly on board through the lens without being trapped inside the lens and chip up to some point. Yet such low power consumption attained from the chip would not cause thermal issues.

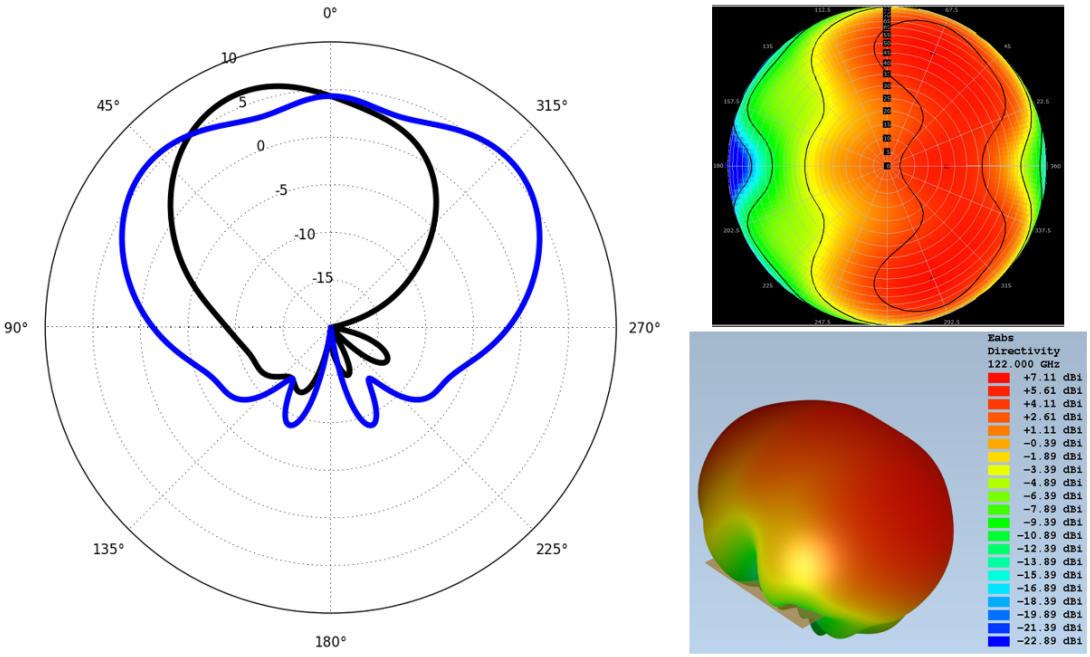

Figure 5.20: Simulation results of 122-GHz TRMant chips.

Many simulations with respect to different lens sizes are performed and optimum lens structure for each frequency band is achieved. The general structure of lens is illustrated in Figure 5.21. It consists of a hemispherical volume with certain radius at the top to direct the main beam with high gain and a cylindrical volume at the bottom with certain height to match to certain focal point. The dielectric constant of silicon-lens is considered as ε_r of 11.9 in simulations as of the chip substrate which is 200 / 150 µm thick for 60- / 122-GHz transceivers respectively. The substrate thicknesses do not play an important role in such configuration with silicon-lens, however it provides a proper matching and better antenna performance as a simple TRx with integrated antenna in the case of a reflective ground plane on which the chip substrate is placed and no lens is used for these purposes. Combining the chip incorporating antenna and the silicon-lens (optimum reached with radius of 5.5 mm and additional lens height of 2.0 mm), simulations are completed using full 3D EM software and the results are depicted in Figure 5.21. Integrating a bigger lens would result in higher directivity, but at the expense of increased structure size which might not be very practical depending on the desired application. The beamwidth is ±6° with a maximum directivity of 22.6 dBi centered at 122 GHz, where the manufactured board is shown in Figure 5.22. Non-optimized lens dimensions would result in reduced gain and emerging side-lobes. Using a lens with same radius, but different height for better optimized performance, similar results are achieved for the 60-GHz version as well.

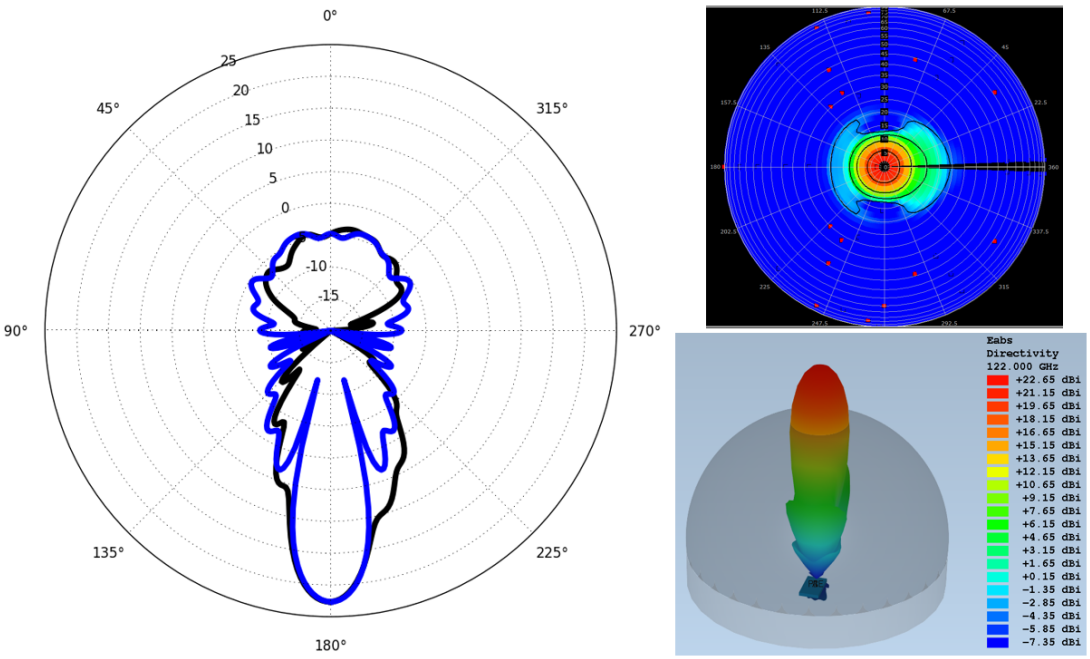

Figure 5.21: Simulation results of 122-GHz TRMant chip with Silicon-lens of 2.0 mm additional height and 5.5 mm radius.

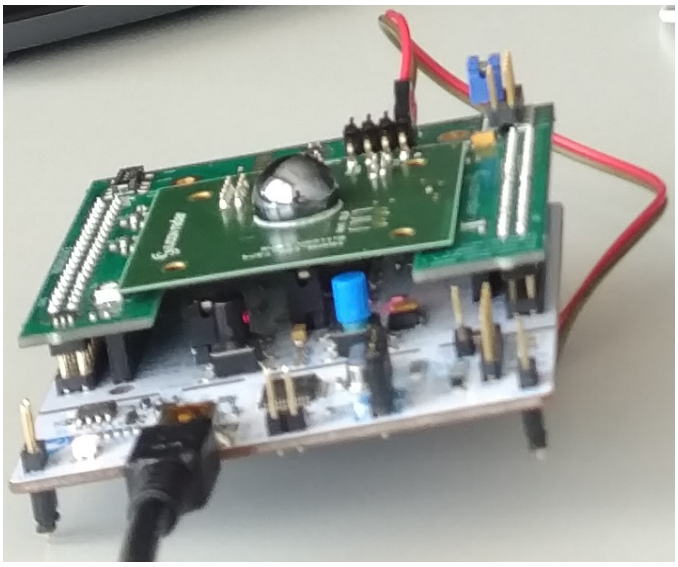

Figure 5.22: Radar evaluation board of 122-GHz TRMant chip with Silicon-lens of 2.0 mm height and 5.5 mm radius.

A different packaging solution is offered using the idea of silicon-lens integration and combining with a custom QFN-like package where the stack-up and corresponding 3D simulated structure are illustrated in Figure 5.23 and Figure 5.24. The compact 5 mm x 5 mm package applied to 122-GHz version includes a 500 µm thick silicon plate which is found to be the optimum height of cylindrical plate when such small lens diameter of 4.5 mm is considered in terms of radiation characteristics. On top of this silicon plate, the chip is mounted and wirebonded to the bottom lead-frame and the final package is molded. Afterwards the silicon-lens is glued on the silicon plate. Wirebonds are realized on the bottom package plate and, since the package would be flipped in normal use case, the lead frame extends to the top package.

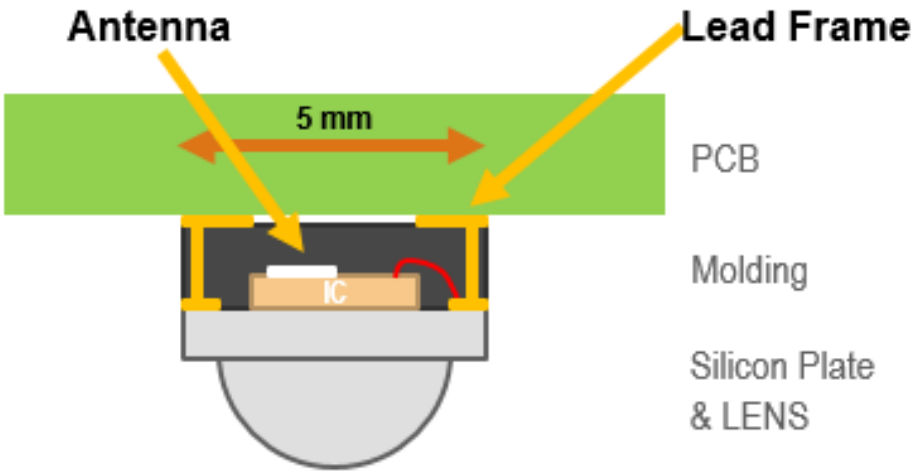

Figure 5.23: 60-GHz TRMant Silicon package with integrated Silicon-lens stack-up.

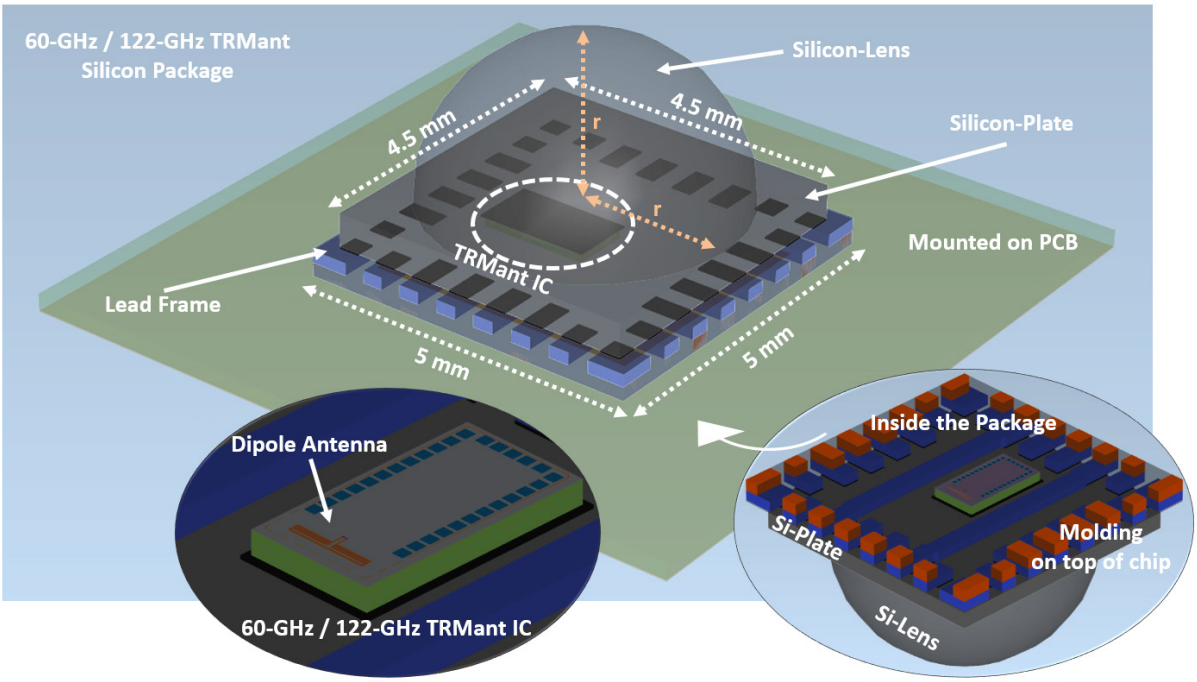

Figure 5.24: 60- / 122-GHz TRMant, 5 x 5 mm^2 Silicon package and antenna.

The simulation results shown in Figure 5.25 point out directivity of 16 dBi and beamwidth of ±14° (including a 5° beam tilt due to alignment error) at 122 GHz even with a small lens size. The complete package is soldered on a cheap PCB material (where no RF connections needed) and the effect of a possible reflector plane beneath is considered in these simulations as well.

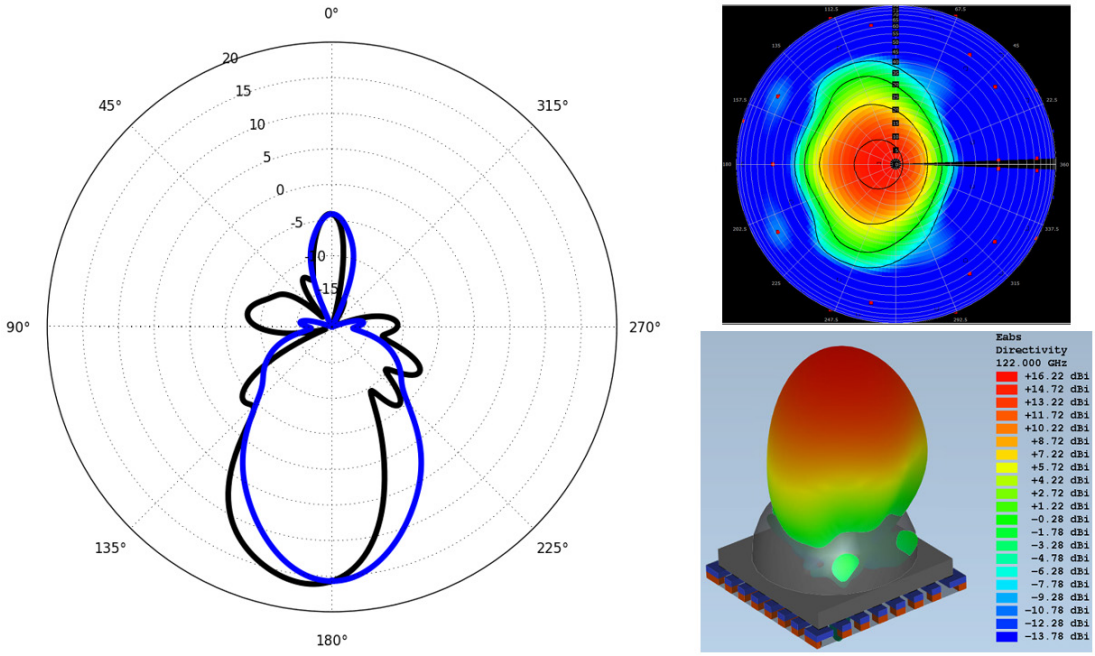

Figure 5.25: 122-GHz TRMant Silicon package antenna simulation results.

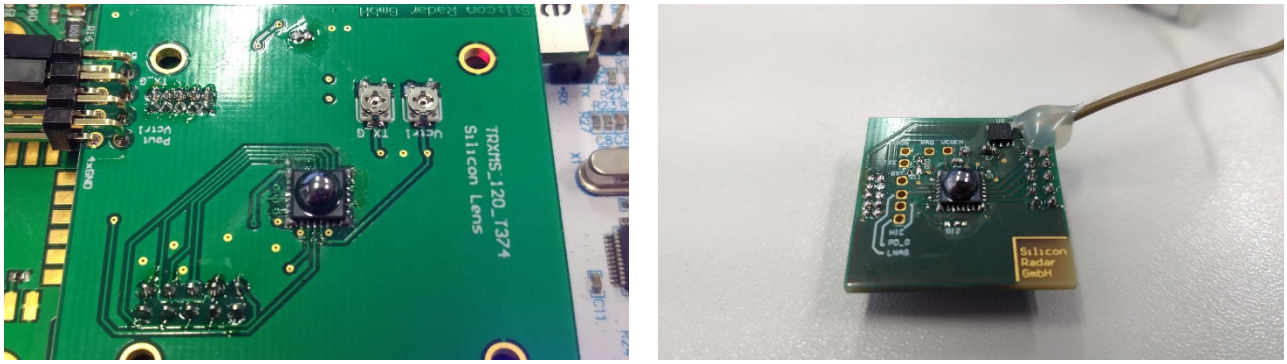

Figure 5.26: Manufactured radar evaluation boards including (*left*) 122-GHz TRMant and (*right*) 60-GHz TRMant Silicon package.

Same package concept is applied to 60-GHz TRM with integrated dipole antenna. Since the package has already been fixed, further optimizations to improve the performance at 60-GHz (such as silicon plate thickness) could not be carried out. Thus reduced performance compared to 122-GHz module is extracted from this version, yet it achieves 9.3 dBi directivity. However the beam focusing as in Figure 5.25 disappears. The manufactured radar evaluation boards for both of the chipsets including the silicon package and silicon lens could be seen in Figure 5.26.

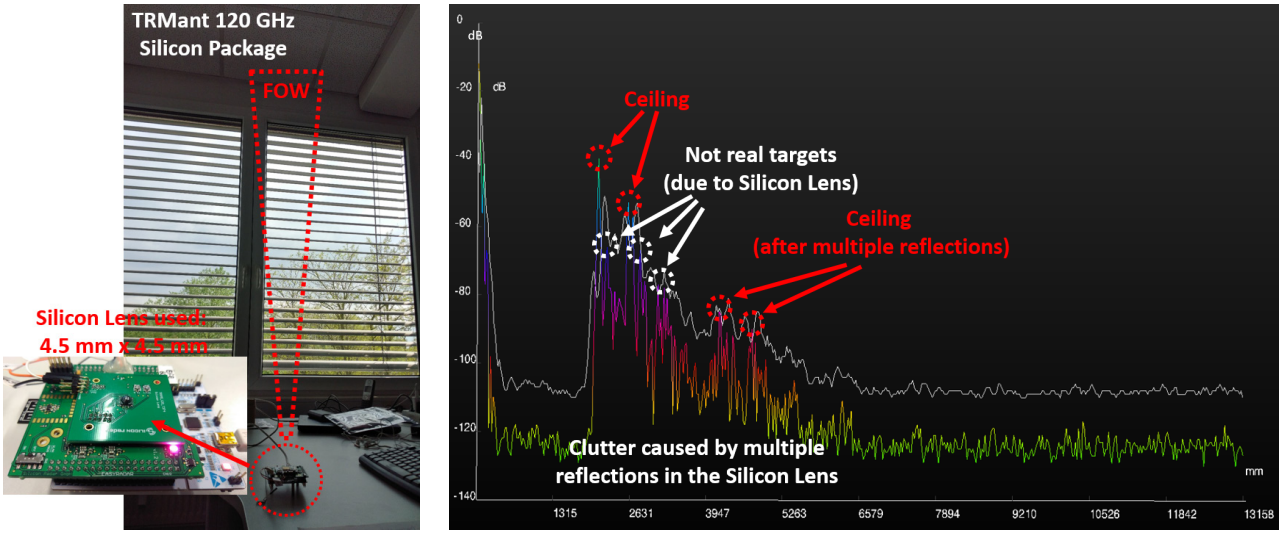

Figure 5.27: Simple indoor measurement using the radar board of 122-GHz TRMant Silicon package including the hemispherical Silicon lens having 4.5 mm diameter directed towards the office ceiling.

Although the real time FMCW radar measurements are detailed in Section 6.2, measurement results of the 122-GHz TRM silicon package is mentioned here for discussion convenience (results of 60-GHz version are not provided to avoid repetitiveness). The first setup includes the package with optimized Silicon lens which is hemispherical in shape having 4.5 mm diameter and the measurement environment as shown in Figure 5.27. The target around 2 m is clearly detected.

However due to multiple reflections within the lens, there are unreal targets appearing in the spectrum having lower SNR levels. Furthermore, a clutter region is formed due to same reason and increased leakage between the channels. In the following Figure 5.28, additional 3 cm x 3 cm plastic lens is inserted on top of the package including the same hemispherical lens so that the signal amplitudes are boosted with the increased antenna directivity.

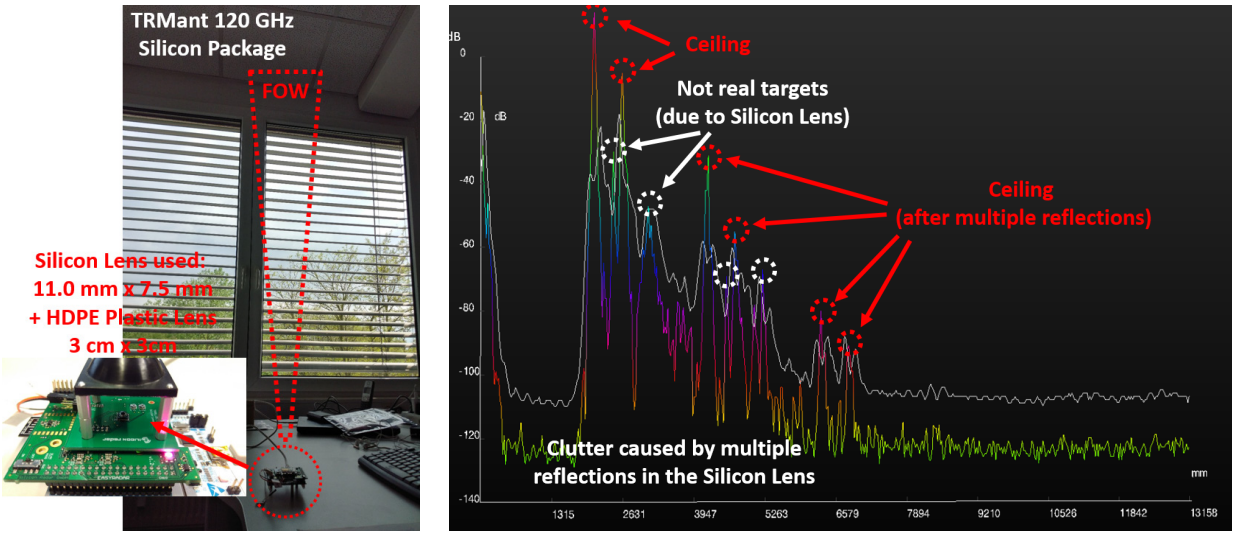

Figure 5.28: Simple indoor measurement using the radar board of 122-GHz TRMant Silicon package including the hemispherical Silicon lens having 4.5 mm diameter and additional 3 cm x 3 cm HDPE lens on top directed towards the office ceiling.

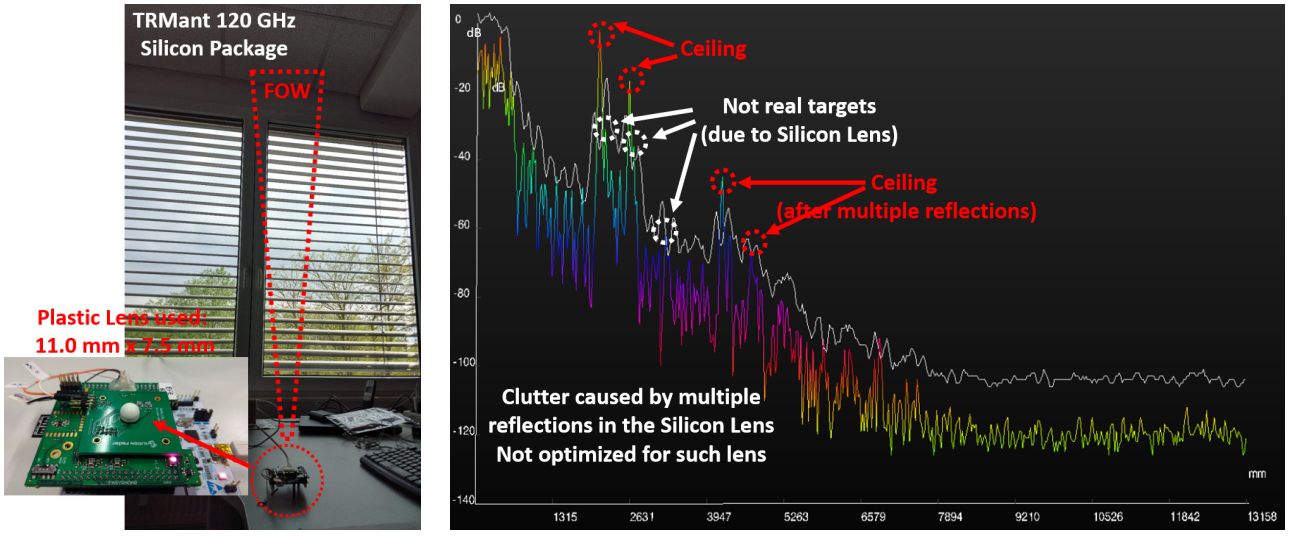

Figure 5.29: Simple indoor measurement using the radar board of 122-GHz TRMant Silicon package including the Plastic lens having 11.0 mm x 7.5 mm size directed towards the office ceiling.

The behavior is also tested with a larger Plastic lens having close dielectric properties to Silicon lens and a size of 11.0 mm x 7.5 mm to see the effect of antenna-lens matching and target SNR

levels (see Figure 5.29). According to measurements the signal amplitudes of the detected targets are improved as expected, but a large clutter region exists as mentioned due to poor matching and non-optimized lens design as a result of multiple reflections, even including the signal trapped inside the lens.

In terms of mass production, silicon-lenses are quite costly that is why lenses with different dielectrics should be designed and compared in terms of their performances. It is found out that cost-effective plastic-lenses with almost similar dielectric properties could offer almost the same performance as was carried out in other measurements. At the same time, additional matching layer with a medium dielectric constant material on top of the lens could be provided to increase the radiation characteristics at the expense of simulation, system and realization complexity.

5.3 BSA Package and Antenna Concept of 60-GHz TRM IC

For the 60-GHz TRM transceiver, another QFN-like packaging solution – called BSA (Back-Side Antenna) – is proposed requiring an antenna built on the back-side of high-frequency material while the chip is connected through via on the front-side. Although the RF performance of via is not clearly known, the overall concept is still expected to achieve high gain with a directing radiation pattern positioned at the antenna center without tilting. PCB stack-up and the corresponding antenna architecture are shown in Figure 5.30 and Figure 5.31 where 4 x 4 differential patch antenna is designed on the top side (*Layer 4*) of Astra material having 254 µm thickness. The antenna array utilizes a reflector plane beneath (*Layer 3*).Then, in order to route the DC connections and provide mechanical robustness, an FR4 section is stacked to the bottom with a cavity reaching an opening such that it creates enough room for chip placement and facilitates the wirebonding process. DC connections on the inner layer (*Layer 2*) are routed to the bottom of package through vias, which composes a lead frame on the bottom layer (*Layer 1*). Finally molding, that covers the cavity / opening is realized to protect the chip and wirebonding sections.

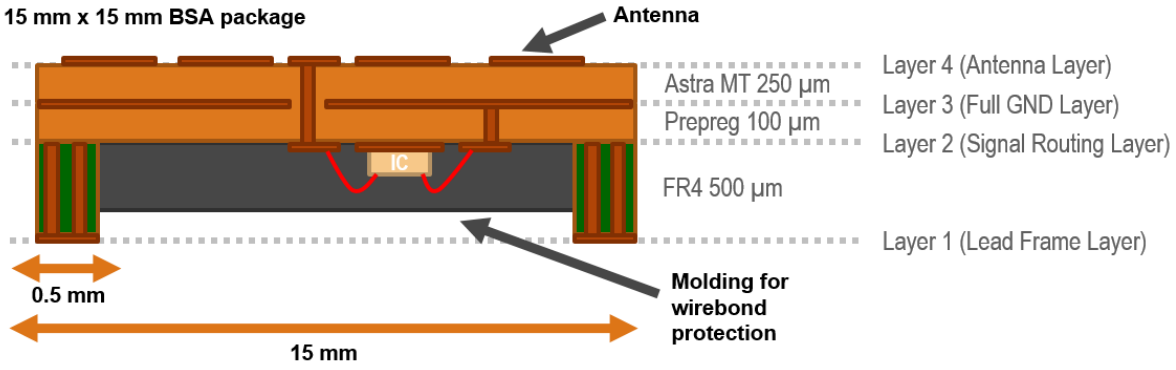

Figure 5.30: 60-GHz TRM BSA package PCB stack-up.

Same antenna topology in Figure 5.2 is employed and the gain is enhanced by a theoretical 6 dB on top of the expected 13 dBi from 2 x 2 patch. Such high directivity is naturally accompanied by narrow beamwidth as well. The antenna matching is realized with wirebond compensation network which is actually composed of wirebond connecting matched transmission lines with 600 µm length, a via and surrounding via patch and power divider sections. The core of a single-ended section is composed of a small series-fed-patch array of two elements. The gain is increased by the four row elements in total, which are connected by three on-board power dividers and finally routed to the center via part. Its mirrored differential half adds another 3 dB of gain within a total package area of compact 15 mm x 15 mm. The photos of the manufactured packages are shared in Figure 5.32 with its soldered version on radar evaluation board.

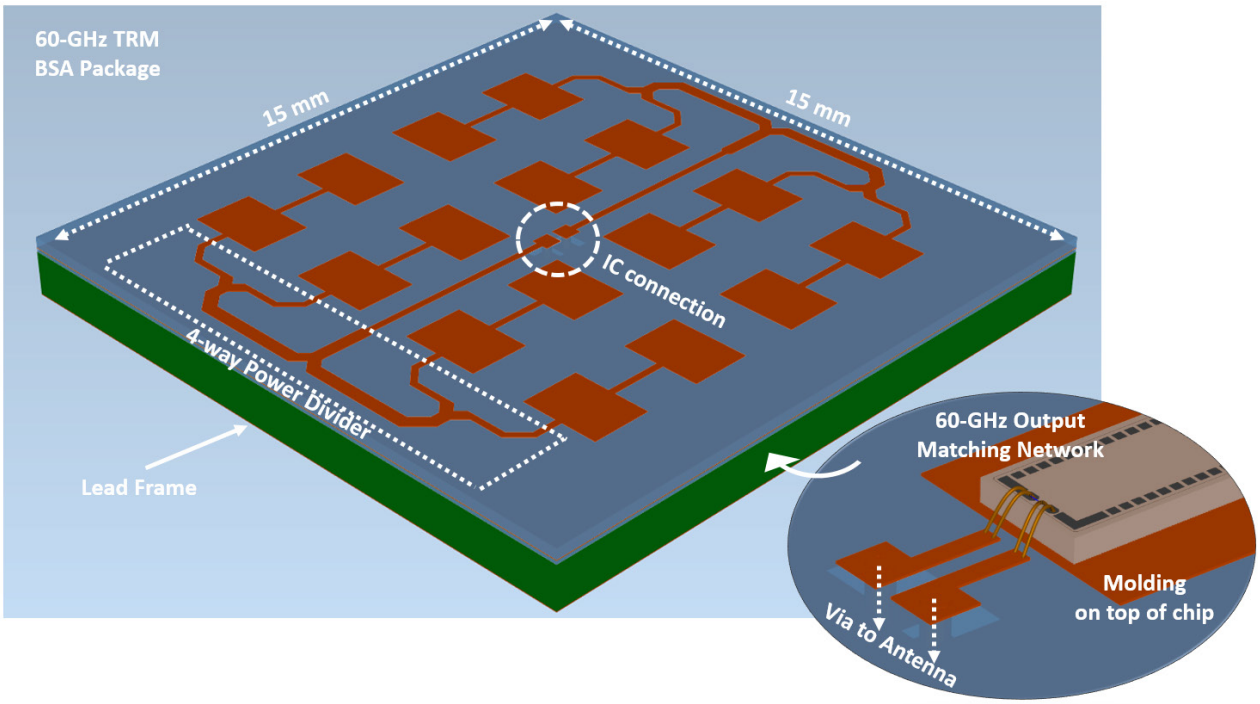

Figure 5.31: 60-GHz TRM 15 x 15 mm^2 BSA package and antenna.

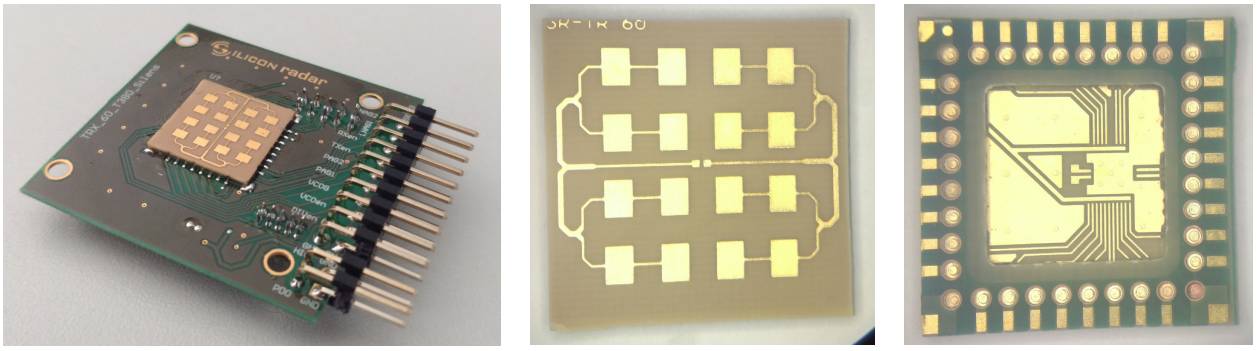

Figure 5.32: Photo of fabricated 60-GHz TRM BSA package and its view in radar evaluation board.

The results of full antenna and package simulation of the manufactured design could be viewed in Figure 5.33 and Figure 5.34. According to results, a directivity of 18.5 dBi is expected at 60 GHz. To downgrade the effect of wirebond inductance, double wirebonds are utilized on the RF sections which the chip has relatively larger pads to ease the process. Side-lobe levels are around 4 dBi. Finally the total beamwidth at 60 GHz is 16° and the 3-dB operation bandwidth covers the full ISM band.

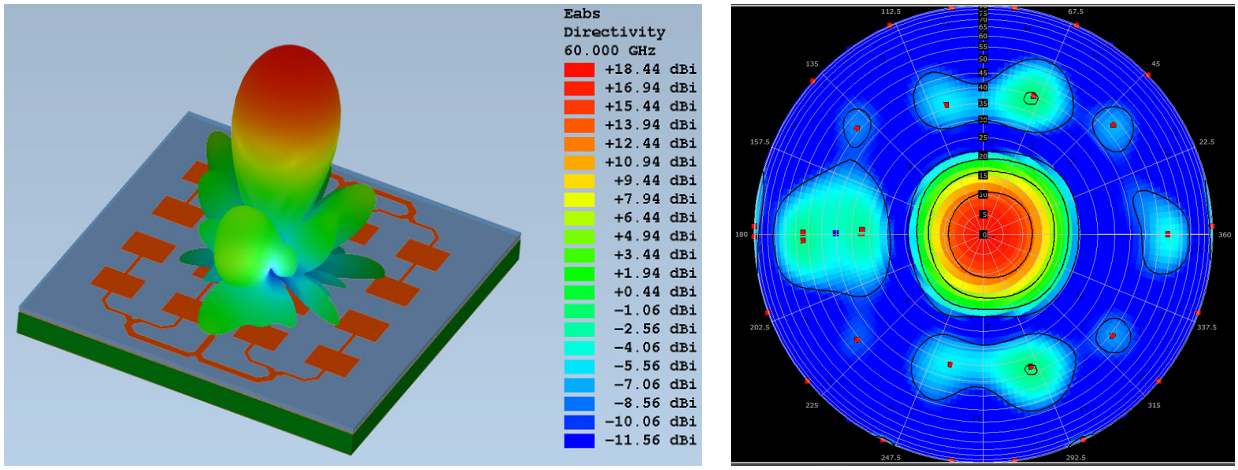

Figure 5.33: 60-GHz TRM BSA antenna simulation results (3D radiation pattern at 60 GHz).

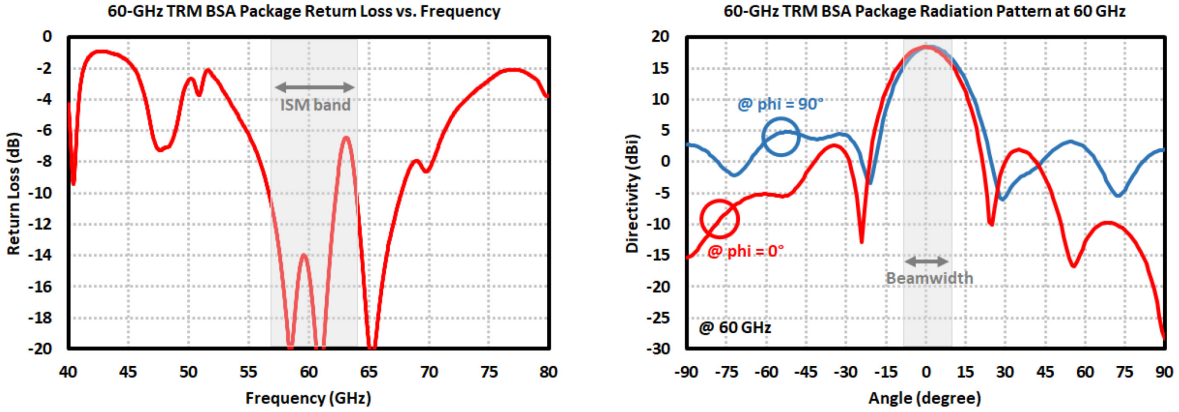

Figure 5.34: 60-GHz TRM BSA antenna simulation results (radiation pattern at 60 GHz and return loss).

5.4 LGA Package and Antenna Concept of 60-GHz ICs

BGA (Ball-Grid-Array) packaging option [2], [28], [40], [64] was considered and simulated at first. However, considering the number of required pads and routing of these on the PCB on which these packages would be mounted, it would have complicated the PCB design and might result in

higher insertion losses. Therefore another package idea called LGA (Land-Grid-Array), suitable for high frequency, is employed especially for 60-GHz chips. The package is composed of four layer Astra MT77 substrate where two 127 µm thick core Astra substrates are stacked with its 120 µm thick Prepreg (see Figure 5.35 for the board stack-up). These QFN-like packages have sizes of 6 x 6 / 6 x 6 / 10 x 10 mm^2 respectively for TRM / TR2 / MIMO transceivers. The bottom layer (*Layer 1*) is designed in a way to conform the generic QFN layout including the die-attach-pad. The two inner layers (*Layer 2* and *Layer 3*) are used as RF ground planes so that microstrip transmission lines could be laid out on the top layer (*Layer 4*). This top layer includes the DC connecting lines as well which are then connected to lead frame through vias. The *Layer 3* and *Layer 4* have cavities for chip placement which help reducing wirebond lengths, hence the inductance, so offer a better impedance matching option. In the end, the chips sit on the much thicker copper plane in *Layer 2* that is connected to die-attach-pad through via arrays for proper heat dissipation. The extra grounding and via-wall between RF transmission lines and DC lines are implemented on *Layer 4* to offer shielding to some extent. Finally the chip, wirebonds and the transmission lines are protected by a molding material.

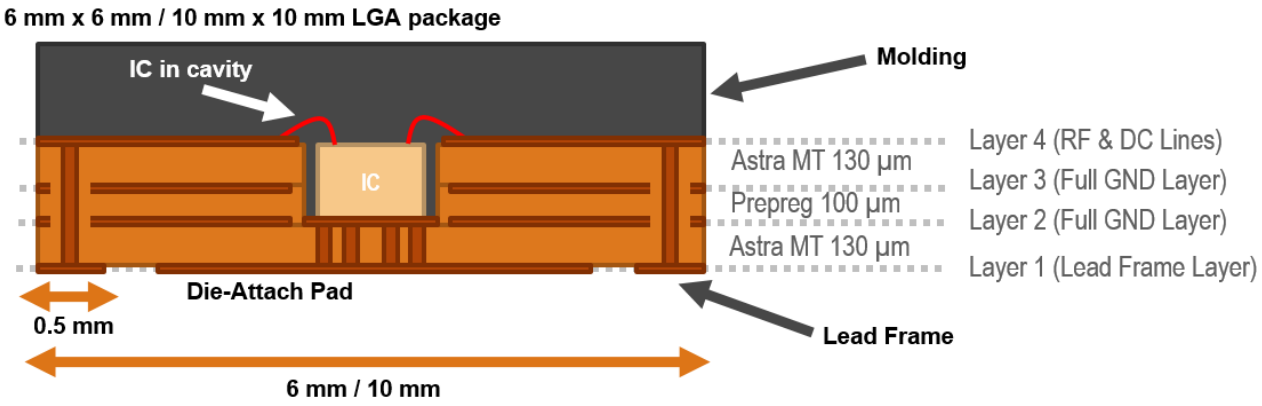

Figure 5.35: 60-GHz LGA package PCB stack-up.

The manufactured PCBs containing these packages are shared in Figure 5.36, Figure 5.37 and Figure 5.38. The TRM and TR2 packages have differential Tx / Rx signal outputs since there are enough leads to fan out from the package. Therefore the simulations are also quite straightforward and the impedance matching is much simpler. However the MIMO chip has many control pins which leads to a necessary removal of the differential RF connections, thus low-profile balun structures are implemented on *Layer 4* in order to convert them to single-ended outputs. The other reasons include the limited space on the top layer and much higher simulated insertion losses caused by the differential output routing.

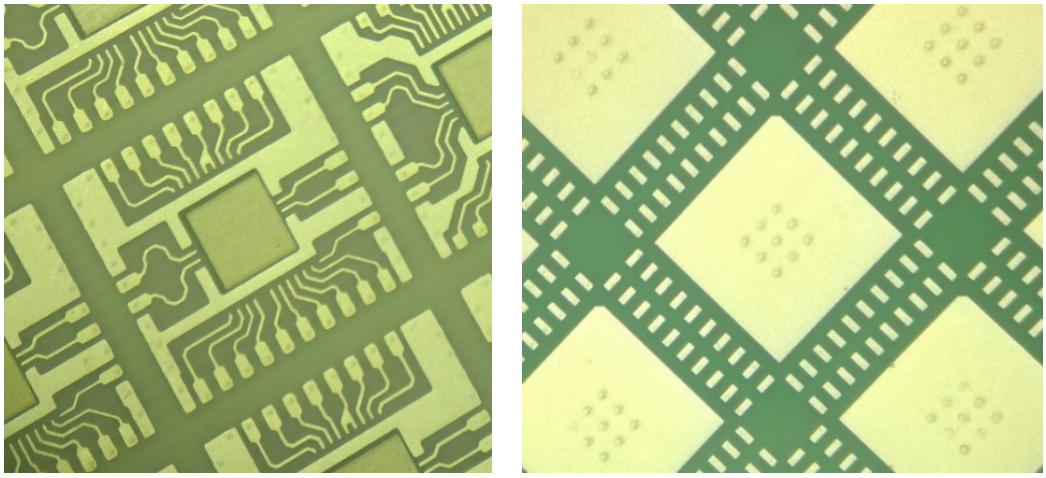

Figure 5.36: 60-GHz TRM 6 x 6 mm^2 LGA package, top (RF and DC connections) and bottom (lead frame).

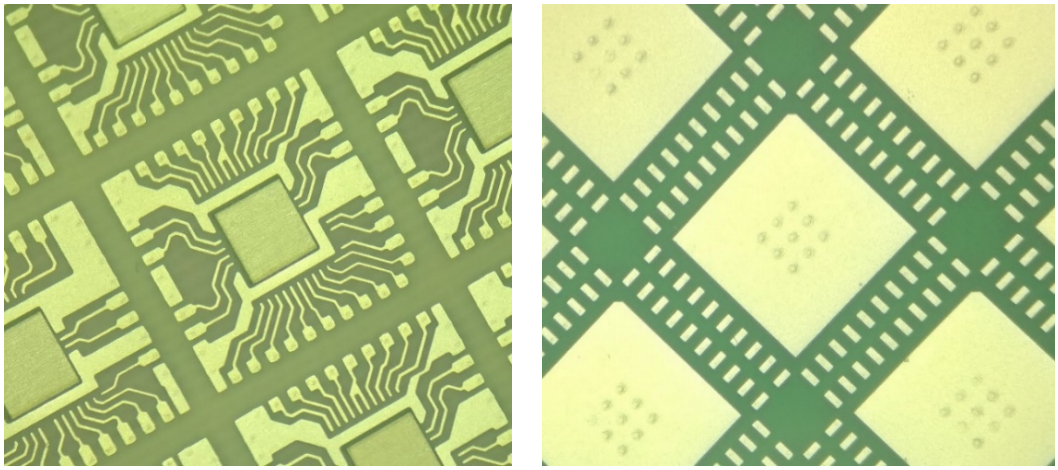

Figure 5.37: 60-GHz TR2 6 x 6 mm^2 LGA package, top (RF and DC connections) and bottom (lead frame).

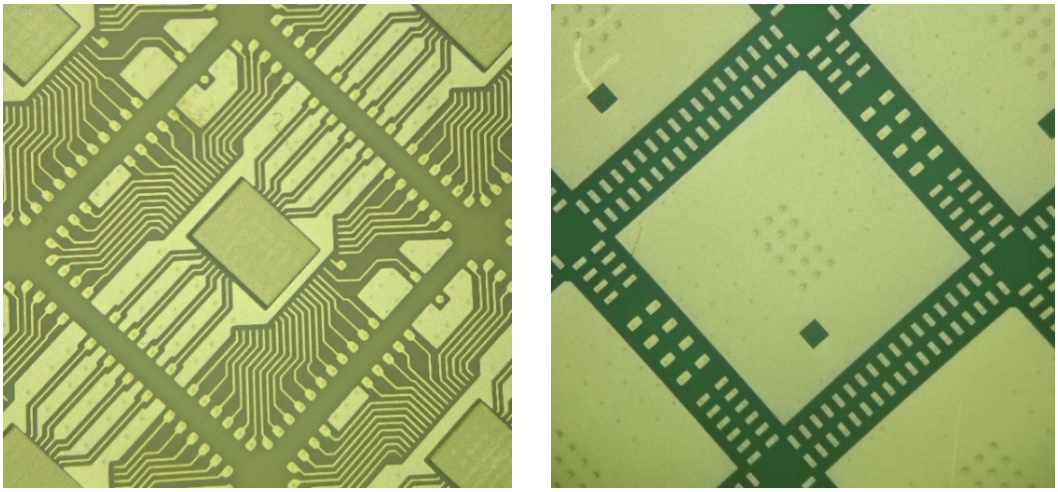

Figure 5.38: 60-GHz MIMO 10 x 10 mm^2 LGA package, top (RF and DC connections) and bottom (lead frame).

In TRM version, the matching sections are formed successively by wirebonds, impedance-matched transmission lines, via and capacitive via-surrounding pads both on *Layer 1* and *Layer 4*, as shown in Figure 5.39. The simulation results of these are highlighted in Figure 5.40, where TRM has 2.5 dB of insertion loss in average on the RF path within the defined ISM band. The return losses are also at acceptable levels even though 100 Ω differential matching is not satisfied.

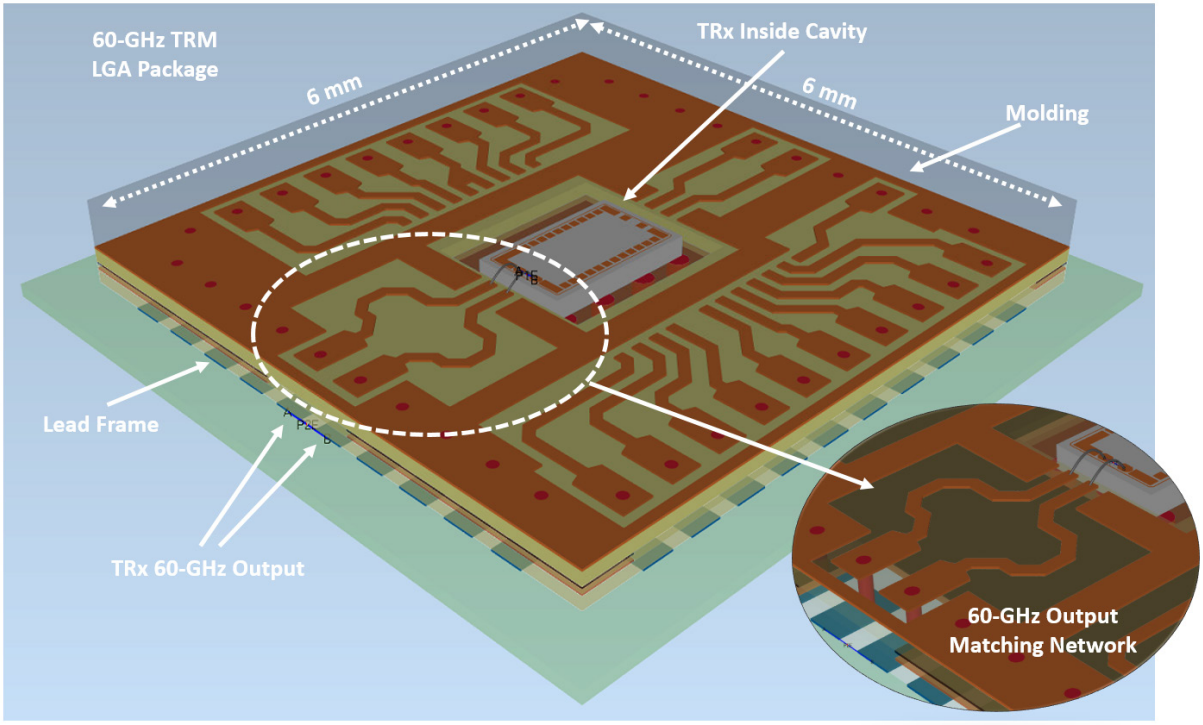

Figure 5.39: Simulated 60-GHz TRM 6 x 6 mm^2 LGA package structure.

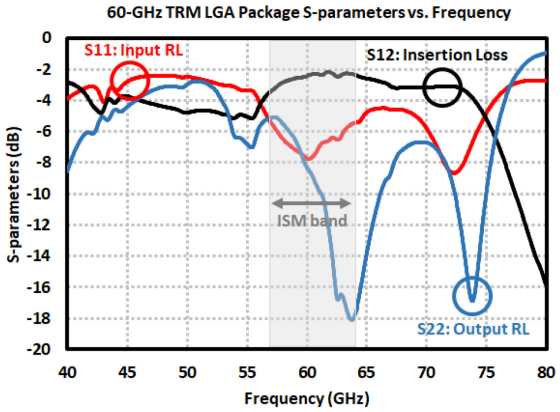

Figure 5.40: Return loss and insertion loss of 60-GHz TRM LGA package.

On the other hand, similar performance is achieved from the TR2 chip in terms of return loss and insertion loss for each Tx and Rx ports. The simulated structure and its results are shown in Figure 5.41 and Figure 5.42 respectively. The package performs 2.5 dB insertion loss in average

with return losses are still acceptable and isolation between ports are below -20 dB (maximum at isolation between Rx channels) within the ISM band.

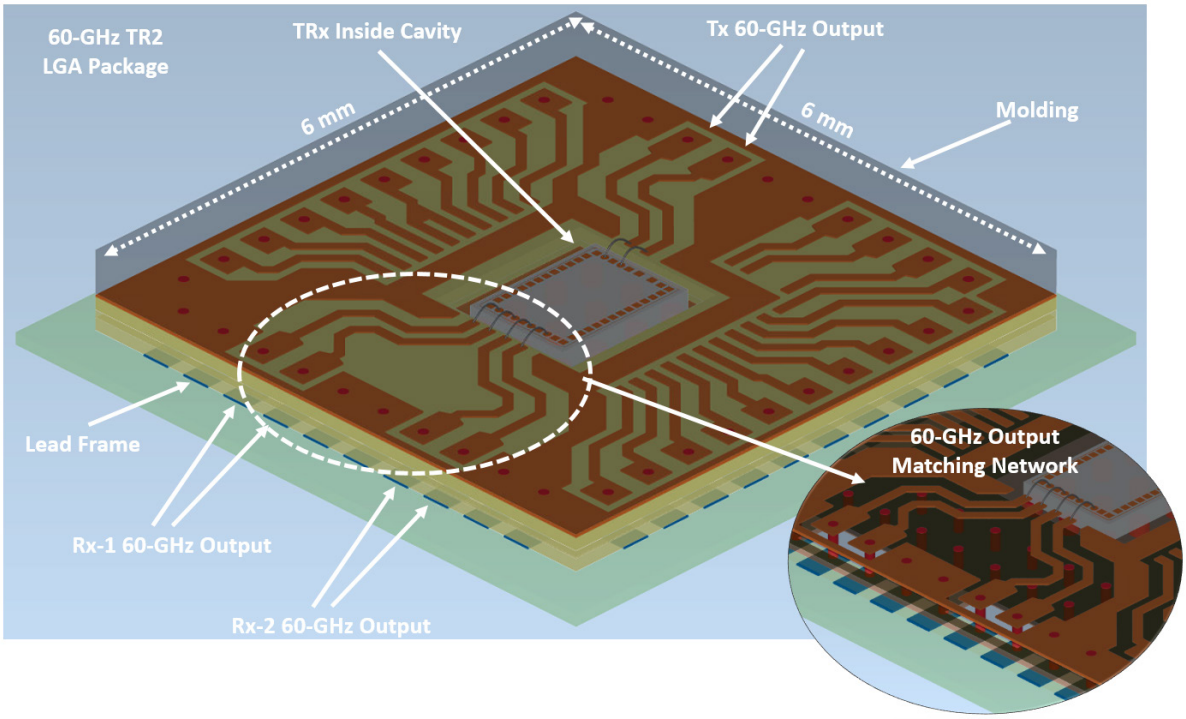

Figure 5.41: Simulated 60-GHz TR2 6 x 6 mm² LGA package structure.

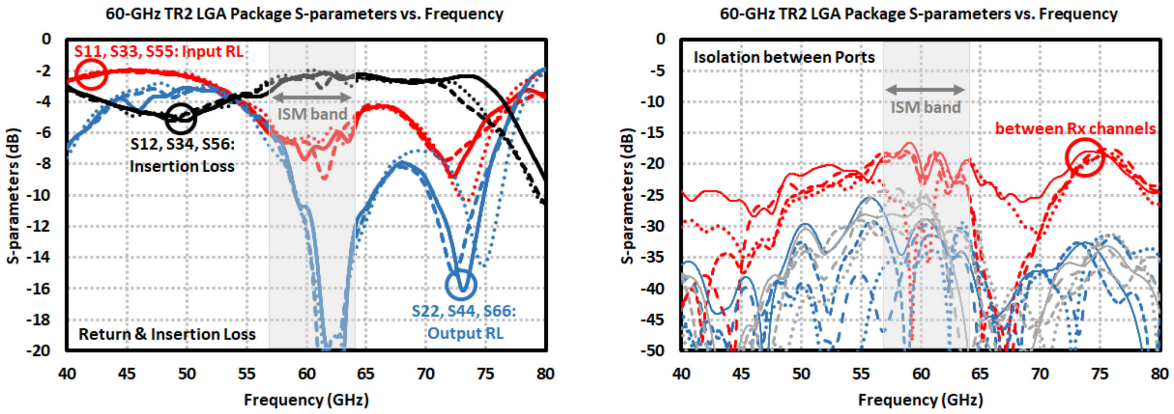

Figure 5.42: Return loss, insertion loss and port isolation of 60-GHz TR2 LGA package.

Finally, MIMO chip simulations are performed based on the package model shown in Figure 5.43. 60-GHz MIMO chip contains 5-GHz frequency divider and 20-GHz *LOin* and *LOout* outputs, as well as the 60-GHz Tx and Rx channel outputs, hence multiple high frequency transmission lines are routed inside the package. Due to limited area provided, *LOout* pin has a longer connection having a length of almost 10 mm, which brought additional loss compared to *LOin* pin whose corresponding pad on chip and output on package are placed on the same side, hence lowering the

insertion loss. Since the package has limited number of lead frames (package size is not increased just to get higher number of pads), 60-GHz outputs are converted to single-ended using a very simple balun structure by dragging one of the differential inputs to ground while the conjugate is connected to output pad.

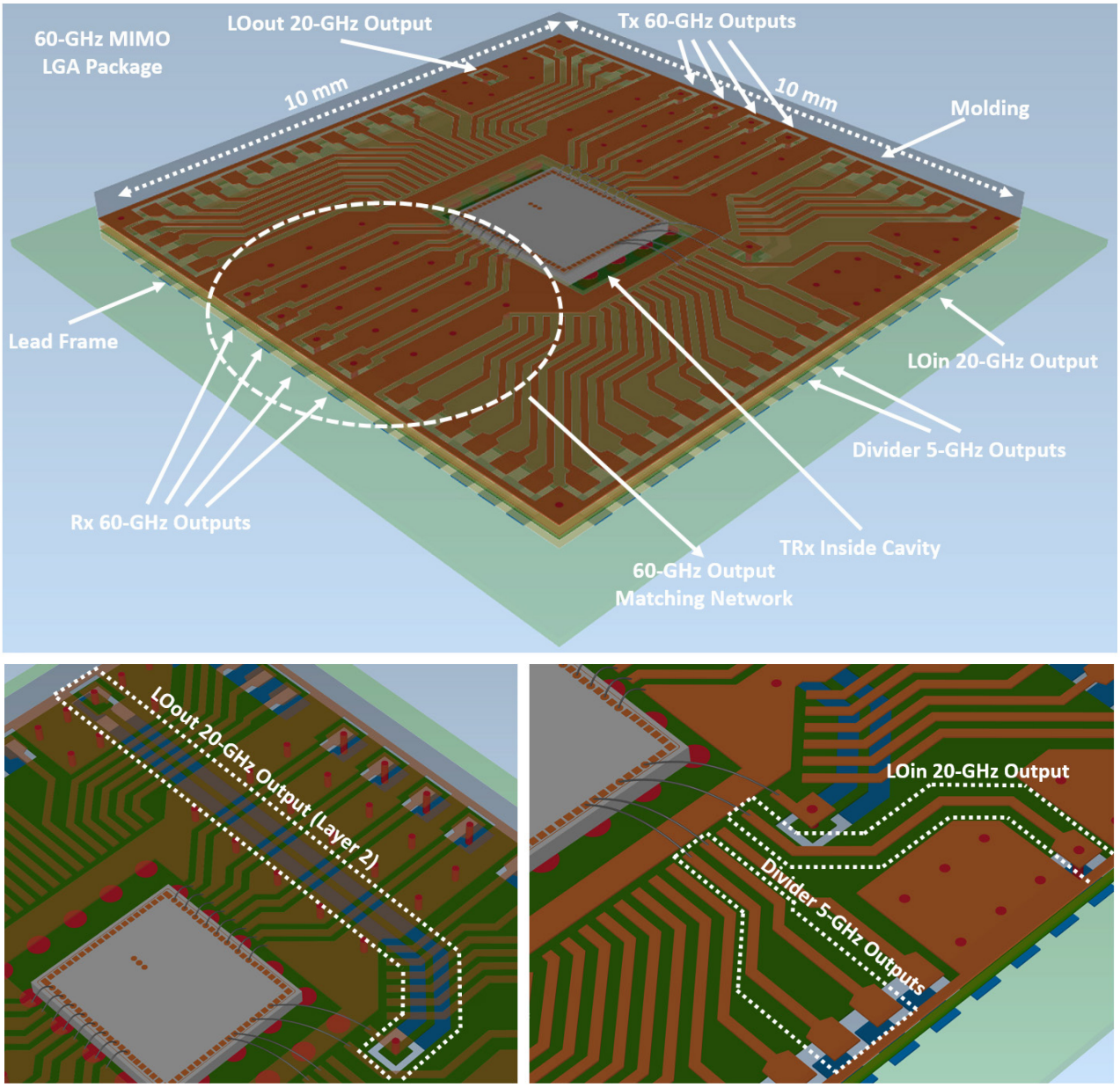

Figure 5.43: Simulated 60-GHz MIMO 10 x 10 mm^2 LGA package structure.

Simulation results of all the high frequency sections are highlighted in Figure 5.44 to Figure 5.47. According to results, the 5-GHz differential frequency divider outputs have an insertion loss of 1.1 dB with acceptable input and return losses just below 10 dB within the ISM band proportional to the frequency range (4.75 – 5.33 GHz) of this divider (see Figure 5.44).

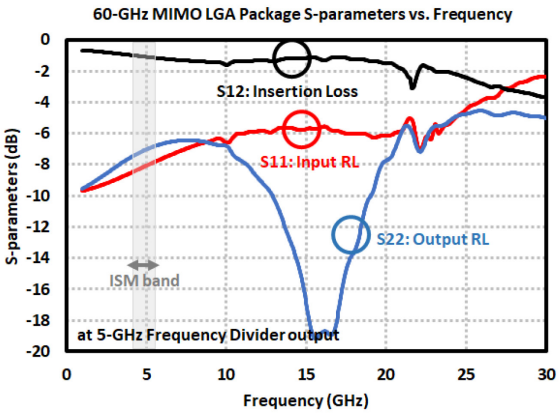

Figure 5.44: Return loss and insertion loss of 5-GHz frequency divider outputs of 60-GHz MIMO LGA package.

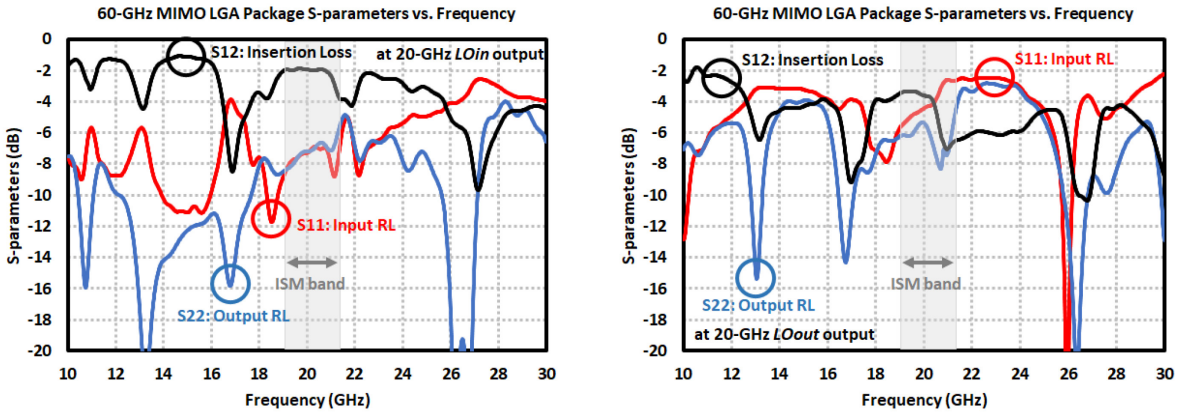

Figure 5.45: Return loss and insertion loss of 20-GHz *LOin* and *LOout* outputs of 60-GHz MIMO LGA package.

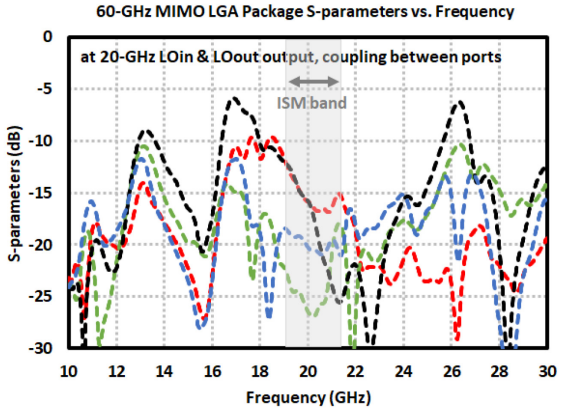

Figure 5.46: Coupling between 20-GHz *LOin* and *LOout* outputs of 60-GHz MIMO LGA package.

On the other hand, as shown in Figure 5.45, single-ended 20-GHz *LOin* and *LOout* sections have insertion losses of 2.1 dB / 4.6 dB respectively. Whereas the input and output return losses of

LOin section is acceptable, poor return losses for *LOout* are achieved within the proportional ISM band (19 – 21.33 GHz). Yet the MIMO chip provides an output power around -4.5 dBm in average (see Figure 4.34) from the *LOout* pad for the next *slave* chip which is already enough to obtain the maximum Tx output power (required *LOin* powers are compared in Figure 4.38). Therefore LOout section would guarantee an output power around -9 dBm together with the chip which is right in the range of required input power for the latter *slave* chip in massive MIMO chain in Figure 2.7. From Figure 5.46, it is observed that the coupling loss between the 20-GHz input and output ports are above 15 dB within the ISM band range. It is worthy to mention that the glitches in simulation results are both due to decreased mesh sizes in order to shorten the total simulation time as well as the simulator convergence errors.

In Figure 5.47, simulation results show return losses almost above 10 dB for the Tx and Rx channels. Insertion losses are found to be around 7 dB in average within the ISM band for these 60-GHz single-ended Tx and Rx sections, which is much higher compared to TRM and TR2 packages due to low-profile balun (one of the differential signals are wirebonded to ground while the other is routed as signal input) and around 3 mm transmission line in combination with via and via-rings. Moreover isolation between ports stay above 15 dB, which might reduce the chip performance.

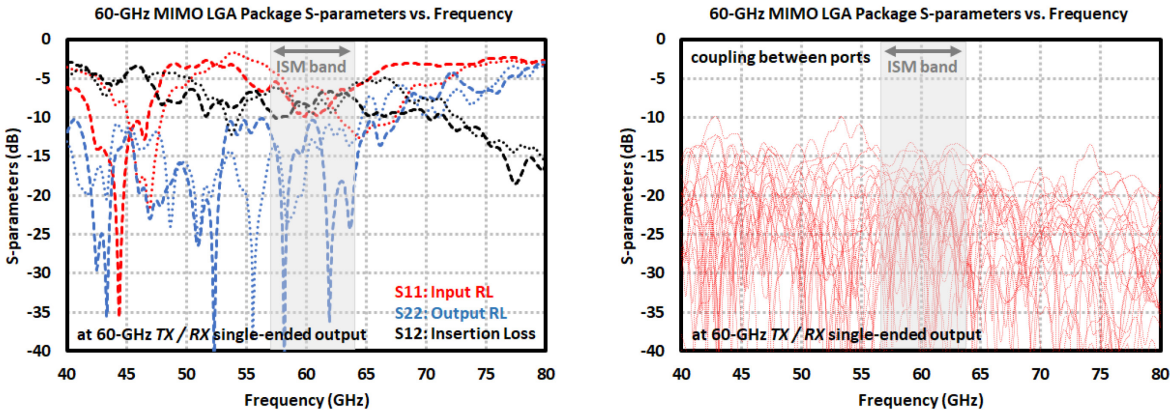

Figure 5.47: Return loss, insertion loss and port coupling of 60-GHz Tx / Rx outputs of 60-GHz MIMO LGA package.

The clear disadvantage of such package is that they are prone to manufacturing tolerances during both the interconnect process and in-package composition (i.e. transmission lines, vias, chip cavity size and high frequency substrate thicknesses) which limit the performance by reducing bandwidth and increasing insertion loss on the Tx and Rx paths. Therefore a correct guess of package effect using simulation tools becomes quite hard. Yet the package losses could be observed after straightforward output power measurements by comparing the chip results. These packages for TRM, TR2 and MIMO chips are already manufactured and shown in Figure 5.48, Figure 5.49 and Figure 5.50 respectively. They are mounted on evaluation boards prepared using the same high frequency Isola Astra MT77 substrate. For the correct evaluation of TRM and TR2 chips,

low-profile balun structures are designed on the 60-GHz paths and the lines are matched to 50 Ω until high-frequency connectors having 1.5 dB average insertion loss. The transmitted output power is measured through a power sensor and the additional losses are de-embedded. Since the package and board have the same output connections on the Rx side as well, similar performance degradation would apply to Rx metrics so that Rx measurements are not carried out.

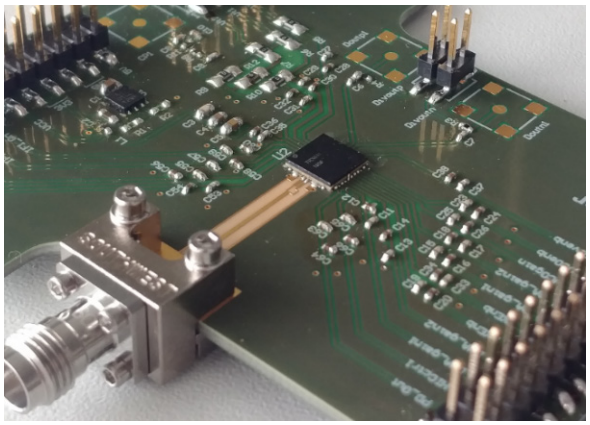

Figure 5.48: 60-GHz TRM 6 x 6 mm^2 LGA package mounted on the designed evaluation board.

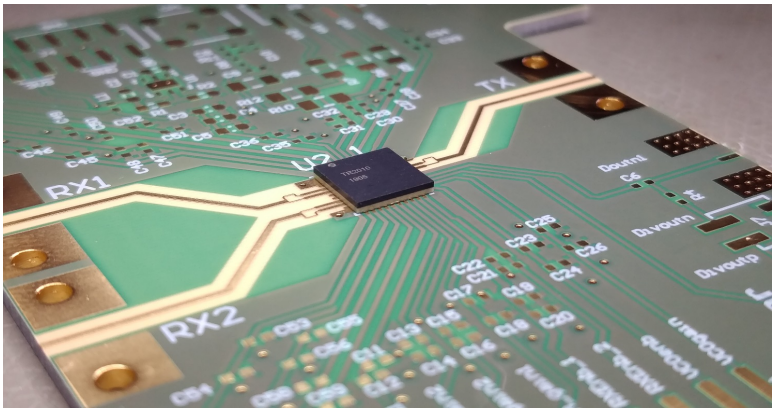

Figure 5.49: 60-GHz TR2 6 x 6 mm^2 LGA package mounted on the designed evaluation board.

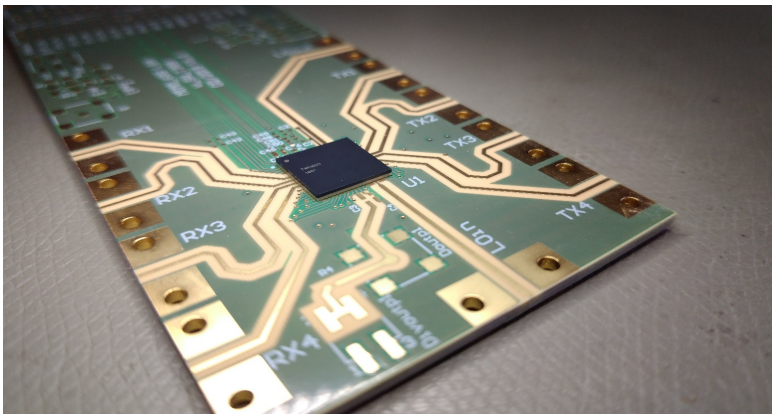

Figure 5.50: 60-GHz MIMO 10 x 10 mm^2 LGA package mounted on the designed evaluation board.

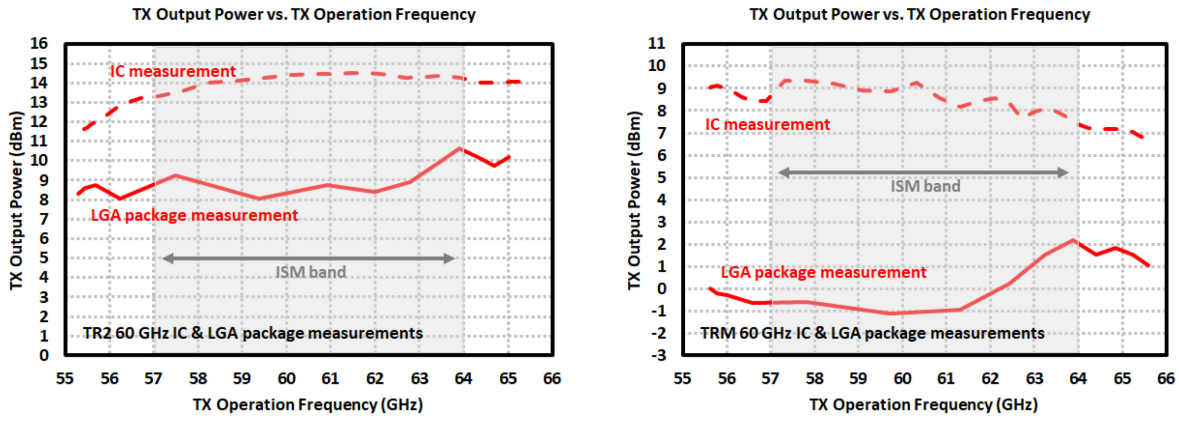

Figure 5.51: Measurement results of Tx output power in LGA packages of (*left*) 60-GHz TR2 and (*right*) 60-GHz TRM chips in comparison to their bare-die performances.

The measurement results of 60-GHz TR2 and TRM LGA packages are plotted in Figure 5.51 which are compared as well to their bare-die performances as summarized in Section 4.1 and Section 4.3. According to results, the packaged TR2 / TRM chips have transmitted output power in average around 8.5 dBm / -0.5 dBm within the ISM band. The on-board balun, transmission line and connector losses are correctly de-embedded for both cases since they have separate test structures. In conclusion, these results point out an increased insertion loss from the package interconnects from the simulations and a great deviation especially for the TRM version owing to the before mentioned reasons. Such response would also reveal itself in the worsened Rx channel noise figure metric and SNR – in combination with the reduced output power. Even though the IC performances are greatly suppressed due to package, successful FMCW measurements are still carried out. Yet the package has to be re-designed and simplified to eliminate the parts which might be affected by the introduced tolerances. Finally the measurements of MIMO version are not completed yet, however as observed such losses would further downgrade its performance due to much complicated design.

5.5 EWLB Package and Antenna Concept of 60-GHz MIMO IC

EWLB (Embedded-Wafer-Level-Ball-Grid-Array) packaging has many advantages over the above designs requiring wirebonds for RF connections [20], [23], [24], [27], [62], [63], [66]. Such interconnects are realized with solder balls placed on chip pads where the chip is flipped, then stacked on the metal layers defined in substrate, and finally molded for protection. These solder balls / copper pillars / vias have low inductances – maximum around 50 pH to 70 pH depending on the distance between chip and the metal layer – thus simplifying the matching networks and allowing high performance matching networks and antenna designs. The fabrication stack-up utilized in the scope of this thesis is shown in Figure 5.52. Technology offers two redistribution layers

for all the DC and RF connections which are mainly separated as the layer where such connections and high frequency transmission lines are designed, and the layer which is dedicated to a ground plane for correct realization of microstrip transmission lines. The distance between two metal layers are only 3.5 µm, hence it allows for transmission lines with a broad range of characteristic impedances together with minimum trace width / spacing of 10 / 12 µm. These limitations provide almost the same flexibility as in a chip fabrication process in contrast to 100 µm limitation of track width / spacing in the case of previous PCB-based designs. Additionally, final solder bump heights play an important role in the total performance of RF connections (especially 60-GHz Tx / Rx outputs) so that they are considered in design with changing heights of 150 µm to 250 µm where the BGA has 500 µm standard pitch. In this respect, two package versions for 60-GHz the MIMO chip (with differential and single-ended 60-GHz Tx / Rx outputs) having 8 mm x 8 mm sizes in total are designed. Even though the manufacturing of these has not been realized yet, simulations and final layouts are completed, and the two packages are in production.

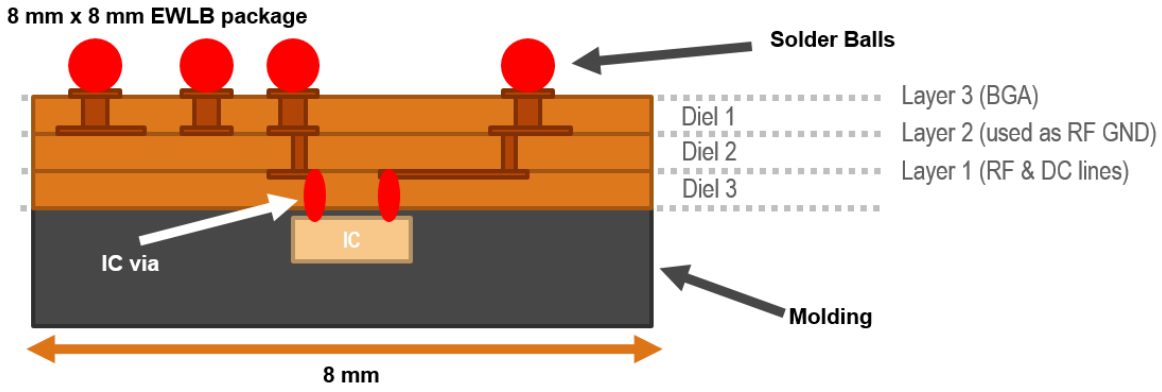

Figure 5.52: 60-GHz MIMO EWLB package stack-up.

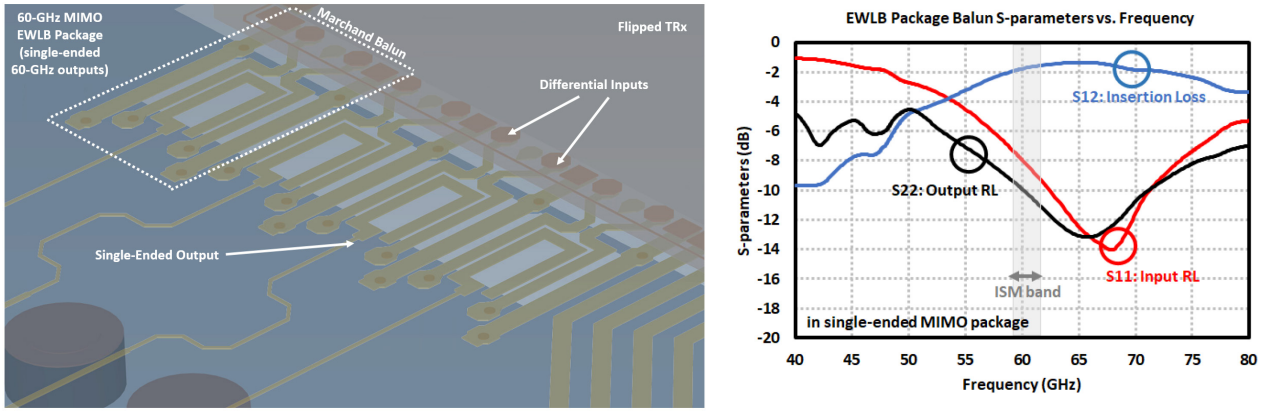

Figure 5.53: Return loss and insertion loss of Marchand balun in 60-GHz MIMO EWLB package.

On the first layer, a Marchand balun is implemented for single-ended package version where the differential-ends are grounded to bottom layer through 30 µm thick vias. The line lengths, widths

and spacing are carefully optimized at 60 GHz as explained in Figure 3.20 and the simulation results are highlighted in Figure 5.53. According to simulation results, an average insertion loss of 1.3 dB is extracted from the balun while the output phases are balanced with input / output perfectly matched within the specified ISM band.

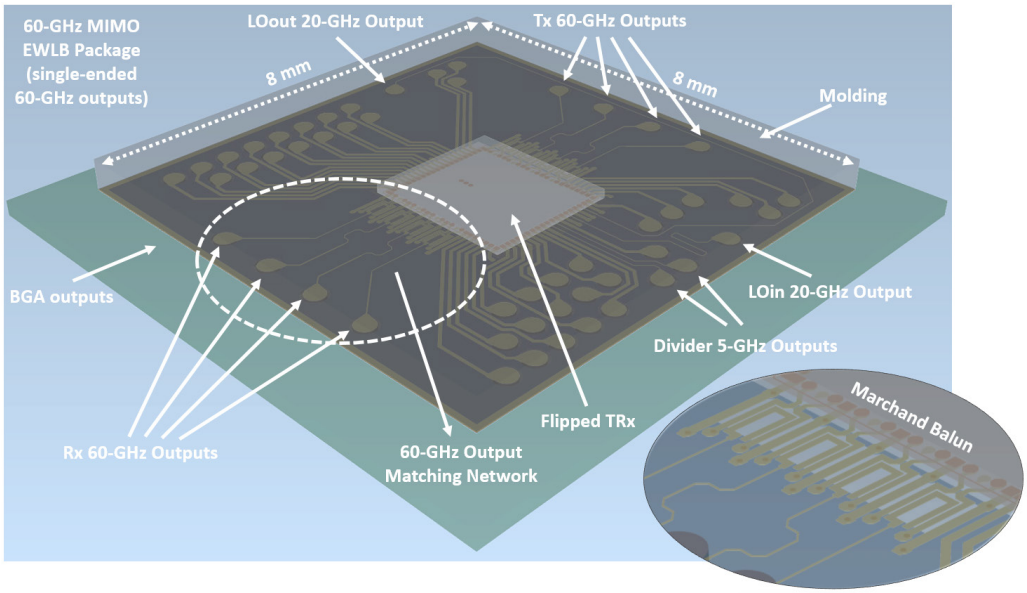

Figure 5.54: Simulated 60-GHz MIMO 8 x 8 mm^2 EWLB package structure with single-ended 60-GHz outputs.

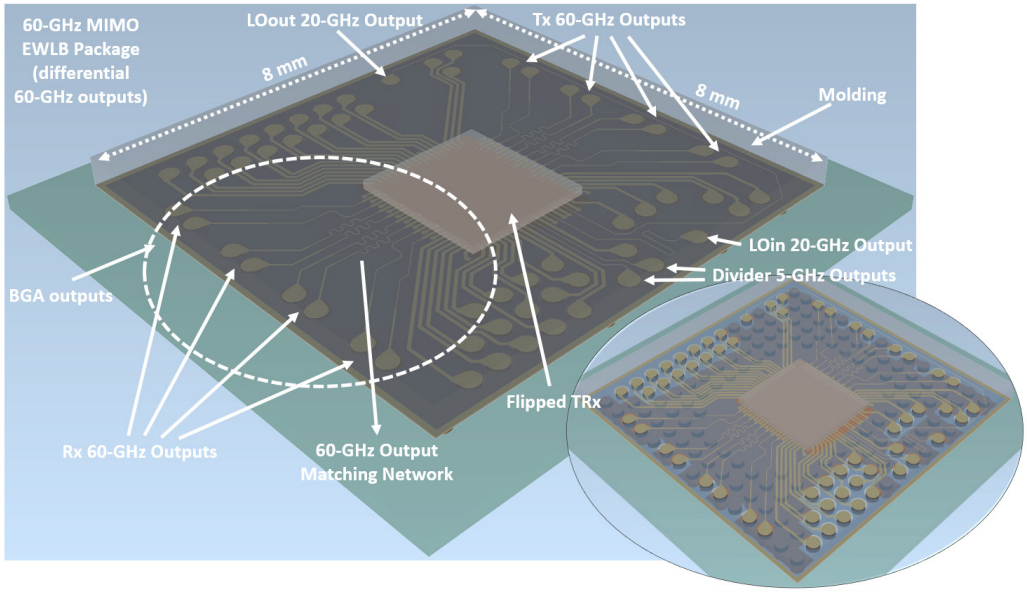

Figure 5.55: Simulated 60-GHz MIMO 8 x 8 mm^2 EWLB package structure with differential 60-GHz outputs.

The layouts and S-parameter results of simulated single-ended and differential packages are shown between Figure 5.54 to Figure 5.60. It is observed that all the 5-GHz differential frequency divider outputs, 20-GHz single-ended *LOin* / *LOout* outputs and single-ended / differential 60-GHz Tx / Rx connections are matched properly while possessing 0.25 dB, 2.0 / 4.5 dB and 3.1 /

2.9 dB of average insertion losses within the defined ISM band (or proportional ISM band corresponding to each output at different frequencies) respectively. Furthermore, not shown in the figures, coupling loss between these outputs stay below -25 dB.

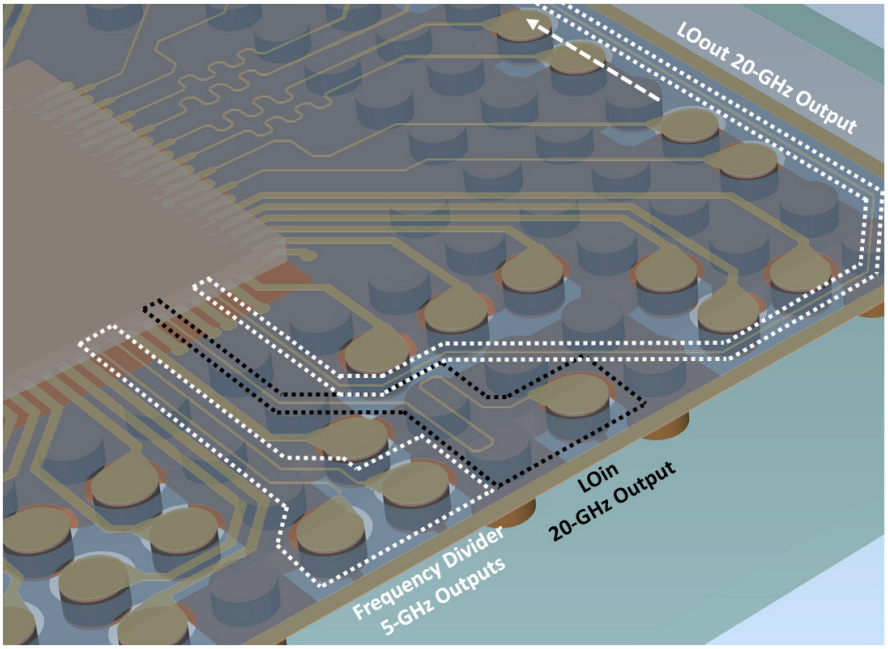

Figure 5.56: Simulated 5-GHz divider and 20-GHz *LOin* / *LOout* outputs in EWLB package structure.

As visible in Figure 5.56, *LOin* and *LOout* pads are brought to the same position in different package edges to simplify the routing in a massive MIMO chain highlighted in Figure 2.7. This could be fixed in chip level as well. Such long routing within the package increased the insertion loss, which could be still negligible in terms of the final performance of radar chip. All these RF outputs at different frequency ranges are accompanied by adjacent GND pads to increase the isolation between each on board level.

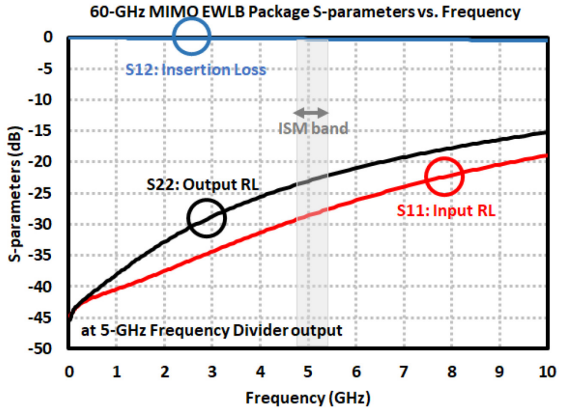

Figure 5.57: S-parameter simulation results of differential 5-GHz frequency divider outputs in EWLB package.

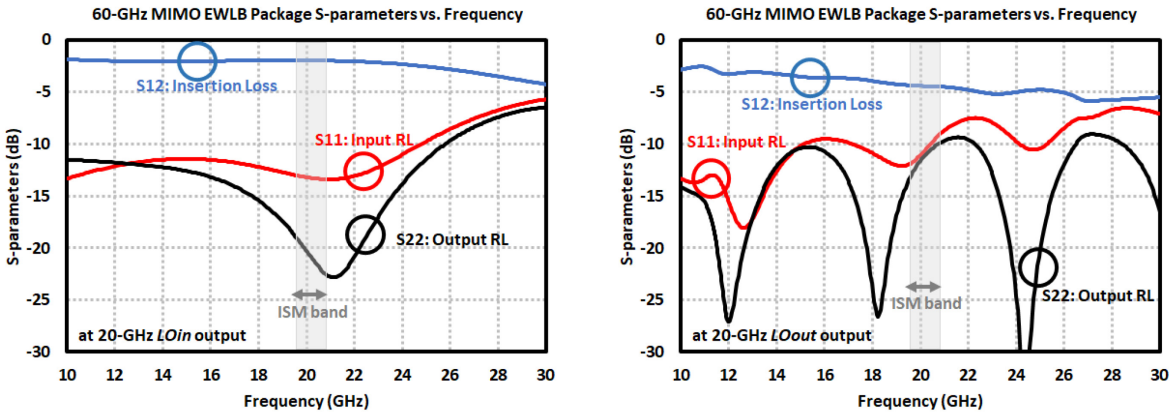

Figure 5.58: S-parameter results of single-ended 20-GHz (*left*) *LOin* and (*right*) *LOout* outputs in EWLB package.

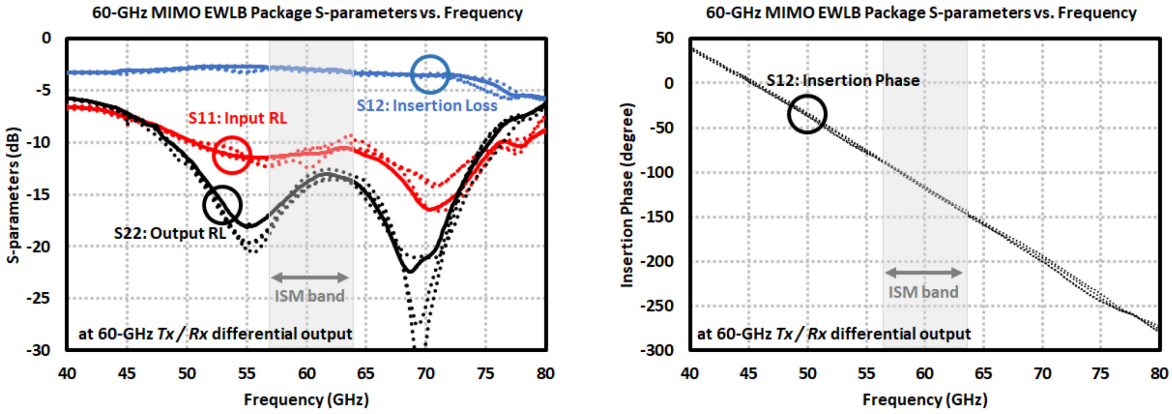

Figure 5.59: S-parameter results of differential 60-GHz Tx / Rx outputs in EWLB package.

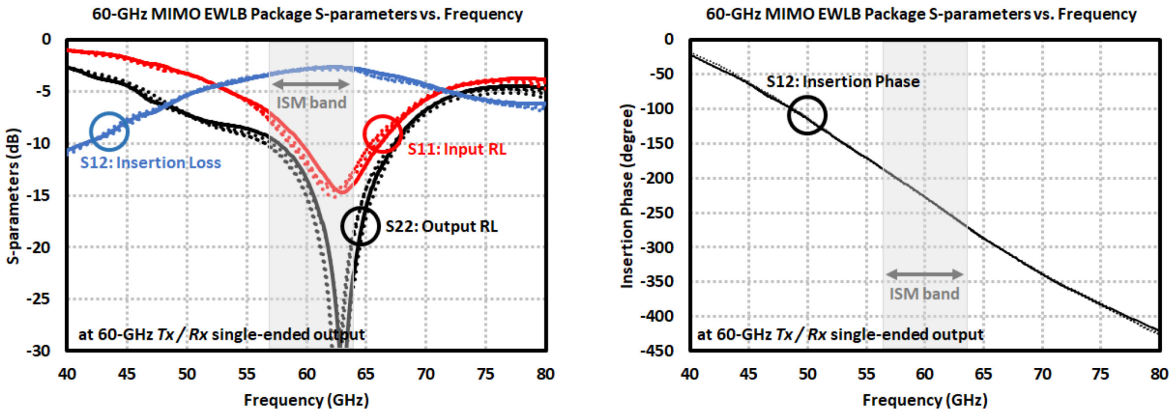

Figure 5.60: S-parameter results of single-ended 60-GHz Tx / Rx outputs in EWLB package.

5.6 Interposer packaging of 60-GHz TR2 IC

Another packaging type utilized for 60-GHz TR2 chip is named as interposer packaging (IPR). The known disadvantage of EWLB packaging concept comes from its poor heat dissipation feature, which puts the performance, or even the functionality, of high power consuming chips into question. The IPR concept addressing such issue is quite similar to generic EWLB package where copper pillars are grown on the pads and then the chip is flipped. The technology offers two redistribution layers with fine-line technology and high resolution as in EWLB process which are grown on a special dielectric material stacked to either a high resistive Silicon or a glass interposer substrate. Similarly the bottom layer is passivated with the exceeding dielectric and additional via and metallization are grown on top for solder ball placement having heights of 250 – 300 µm. Due to signal routing and ball placement, it is similar in structure with BGA packages. Thanks to low inductance at the RF outputs, the impedance matching networks are simpler and less lossy. The package concept is still in manufacturing period, thus only the simulation results are available.

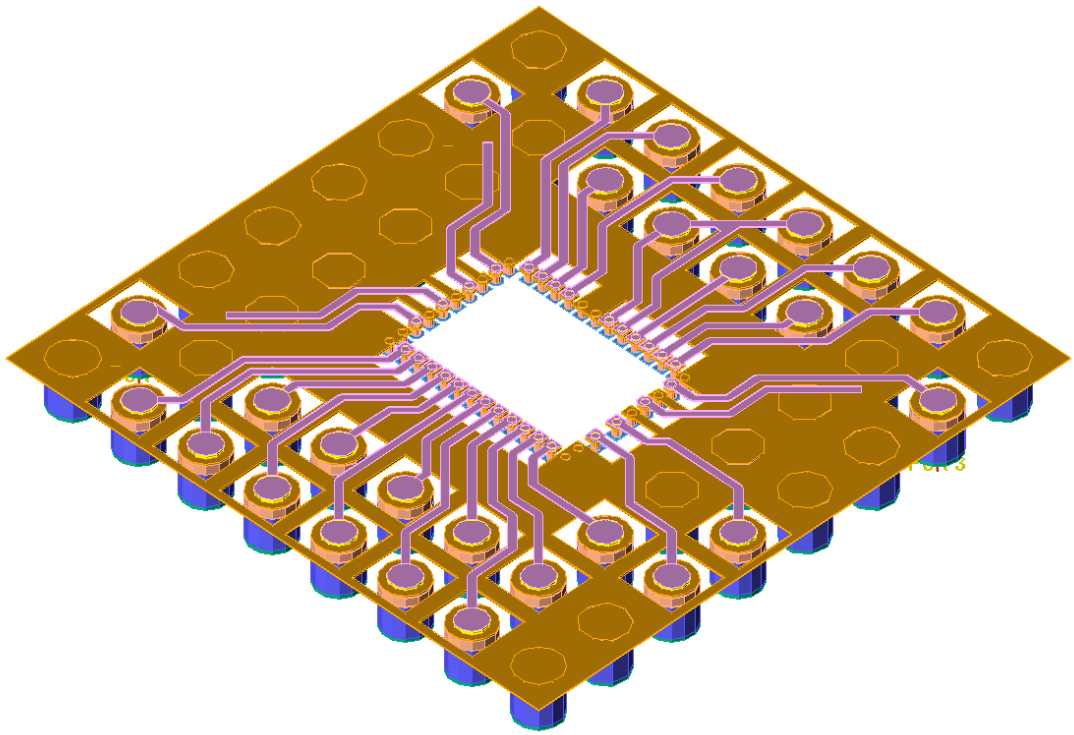

Figure 5.61: Simulated 60-GHz TR2 4 x 4 mm^2 IPR package structure with single-ended 60-GHz outputs.

Two packages with single-ended and differential 60-GHz outputs are designed and the packages have a total area of 4 x 4 mm^2 which is quite comparable to actual chip area as shown in Figure 5.61 (only single-ended version is highlighted). The 60-GHz outputs are again converted to single-ended through a similar balun mechanism where the top layer is employed as a ground plane for microstrip transmission line realization. BGA has a pitch of 500 µm for simplified evaluation board

design. Simulation results are shared in Figure 5.62 which states an insertion loss of 1.5 / 1.8 dB (differential / single-ended packages) around 60-GHz ISM band with input and outputs are matched nicely. Finally the port isolation stays below -25 dB as well.

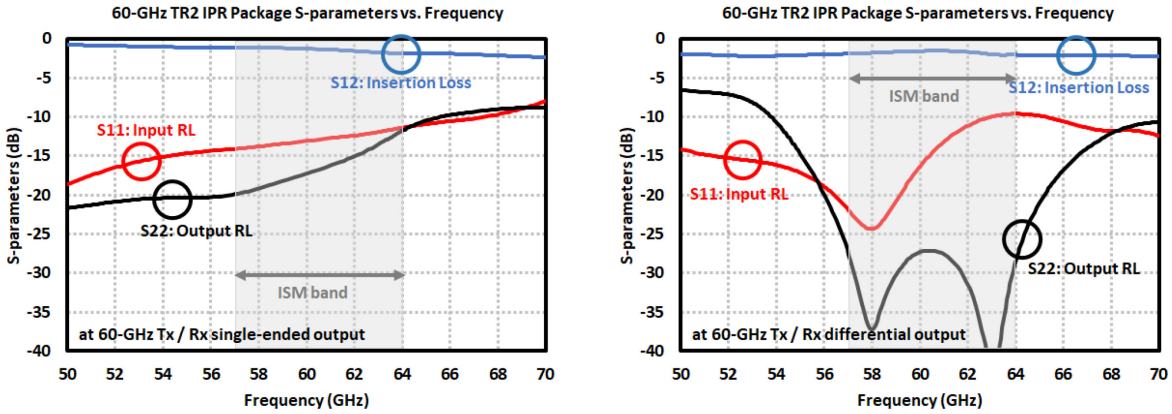

Figure 5.62: S-parameter results of 60-GHz outputs in (*left*) single-ended and (*right*) differential IPR package versions.

5.7 Summary of the Adopted Packaging and Antenna Solutions

Especially for the chips operating at 60-GHz, where wirebond interconnects could still show acceptable performances, various package models are developed. These include silicon package with integrated lens, BSA and LGA packages for the TRM chip. For the TR2 chip same LGA package is modified and EWLB-like IPR package is developed on high resistive interposer substrate. Finally the MIMO IC is packaged using an advanced technology like EWLB and another custom package of LGA. Amongst these LGA was expected to offer the cheapest packaging especially for TRM and TR2 chips since simulation-wise it allows for low insertion losses about 2.5 dB with input / output return losses are acceptable. However measurements are conducted on the fabricated packages and it is observed that the manufacturing tolerances play a great role in the overall performance of chips and greatly reduced performances are obtained especially for the TRM chip. From the TR2 version around 8.5 dBm of output power is achieved and would still lead to a successful product. The cost-effective LGA packaging is applied to MIMO chip as well and poor S-parameter results are attained. This is expected to further decrease the performance of MIMO LGA considering the previous measurements on LGA packages which makes the end-product hard to be utilized in radar applications unless a package re-design is carried out. On the other hand, EWLB package offers a high-performance, yet expensive solution where almost 3 dB insertion loss is achieved for the 60-GHz outputs in differential and single-ended package version.

Even though couple packaging options with wirebonds are available as products operating around 122-GHz, the frequency does not allow for low-cost packaging solutions. Hence antenna

integration on chip is realized and lens integrated silicon package is used where the radiation from the chip back side is benefitted. Since the package is optimized for 122-GHz chip, it allows 16 dBi of directivity, however its 60-GHz counterpart experience performance loss because of not optimized lens structure. With the help of real time FMCW measurements, the importance of lens and antenna matching is revealed with an emphasis of clutter region formation in the desired frequency spectrum.

Due to limited silicon area for antenna integration, PCB-based antennas are implemented for the FMCW radar tests. Even a simple 2 x 2 patch antenna at both targeted frequencies could easily achieve more than 12 dBi gain with high efficiency in spite of the reduced performance after integration of wirebond compensation networks. For all the fabricated radar chips a high-frequency material with proper thickness for the selected frequency bands is utilized and stacked on a mechanically stable thick substrate. Depending on the application either for single- or multi-channel chip integration, various patch antenna architectures are implemented. Finally a compact plastic lens is employed to increase the directivity, so that the detectable radar range improves.

6 FMCW Radar Measurements

In this chapter, a summary of the radar baseband system is explained. The system block diagram with the functions of each component and how the signal processing and target detection are realized are the main goals of this chapter. Finally FMCW measurements are conducted for each chipset and the resulting measurements of couple of these are shared.

6.1 FMCW Radar Evaluation Board

The block diagram of the radar evaluation board is shown in Figure 6.1. The ICs are wirebonded on these boards including a fractional-N PLL, which offers high resolution modulation and helps stabilizing the VCO frequency, filters and amplifiers for IF outputs of chips and a microcontroller for the main signal processing [18].

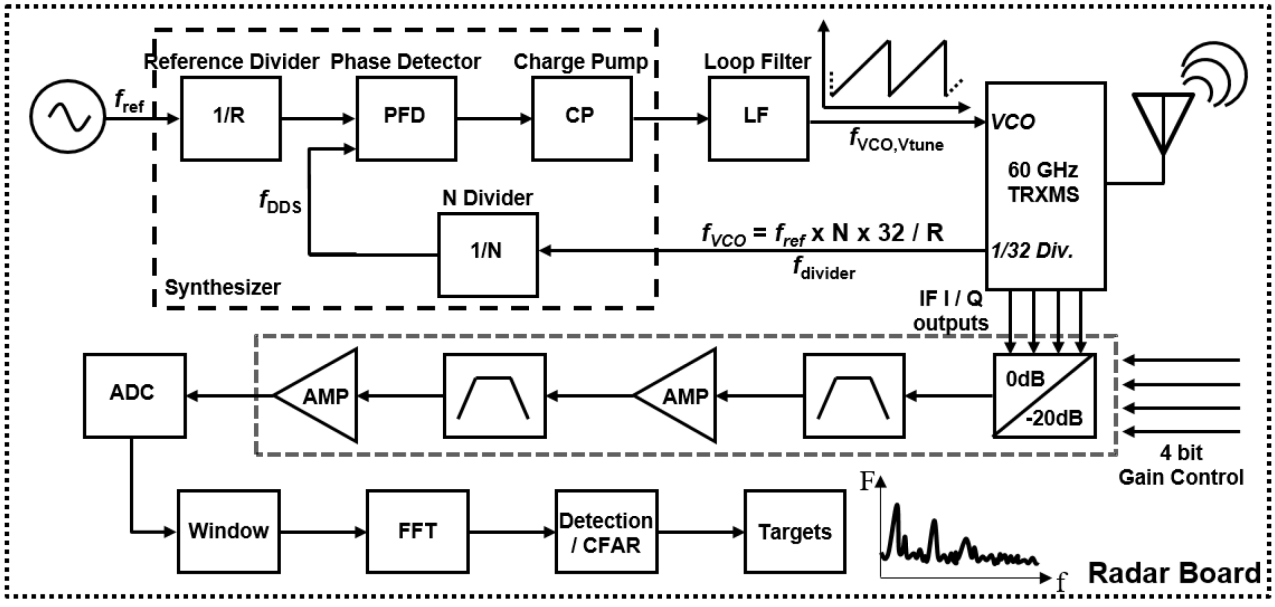

Figure 6.1: Block diagram of radar signal processing evaluation board [18].

The ADF4159 fractional-N frequency synthesizer is employed to generate the required saw-tooth chirp train using an external 80-MHz reference. An example of such modulation is illustrated in Figure 6.2 which belongs to a scheme with 5 GHz operation bandwidth in a 1.3 ms chirp time realized where the total number of ramps is 16 (with additional 2 at the beginning and end of series). Delays between successive chirps are intentional for proper VCO and baseband amplifier operation. The input to this synthesizer is the frequency divider output around 2 GHz from the TRx circuits. At the charge pump output, a loop filter on evaluation board is implemented to control the frequency tuning inputs of VCO. Having the chirp sent by the Tx and then received by the Rx antenna with a propagation delay, different IF frequencies appear at the differential quadrature IF outputs depending on the target distances. In order to evaluate the range profile of targets, frequency spectrum of the resulting IF signals should be extracted through FFT signal processing after digitization. The IF signals are first filtered and amplified where the variable gain of these amplification stages is automatically controlled internally and IF saturation is prevented. The signal processing is then carried out through STM32F303xE microcontroller including analog-to-digital conversion, window function application and FFT and target detection operations. The resulting range profile of targets is then visualized in a GUI environment allowing flexible FMCW operation such as controlling bandwidth, number of FFT samples, FFT size and number of ramps.

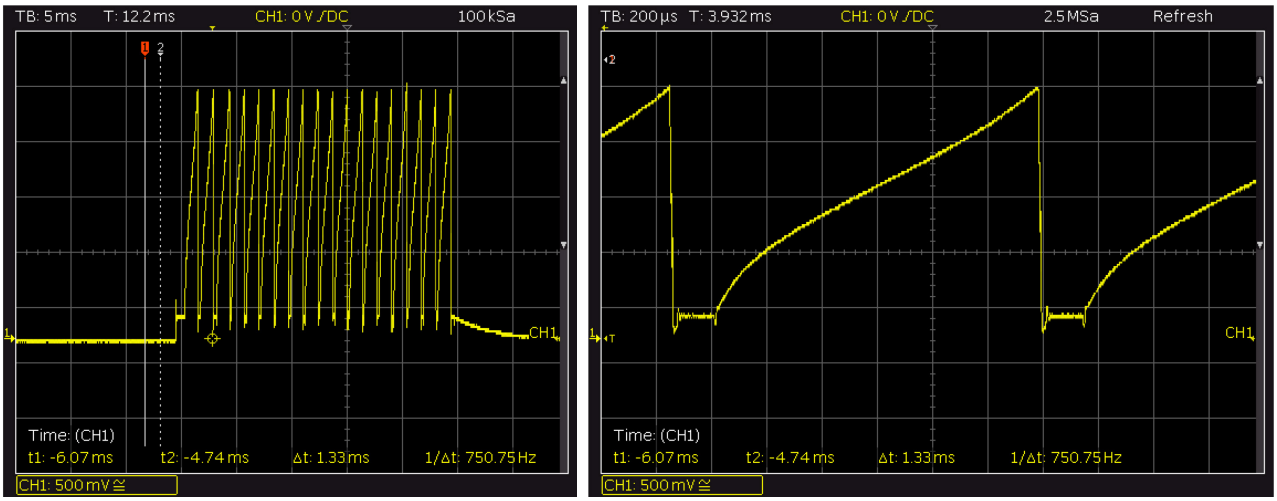

Figure 6.2: Saw-tooth chirp train generated by PLL to be sent through the Tx for 5 GHz modulation bandwidth.

In Figure 6.3, the radar evaluation board including the 60 GHz TRM chip is shown [18]. The chip is wirebonded to a 2 x 2 antenna as explained in previous chapters and a compact 3 cm x 3cm HDPE plastic lens is mounted on the high-frequency board to increase the detection range. The second layer, so called “Silicon Radar – EASYRADAR”, mainly contains the frequency synthesizer and baseband amplifiers whereas the third stack is the STM microcontroller evaluation board. For each of the product under development, dedicated evaluation boards with antennas are designed and tested. However only the results belonging to TRM versions are highlighted in the below section.

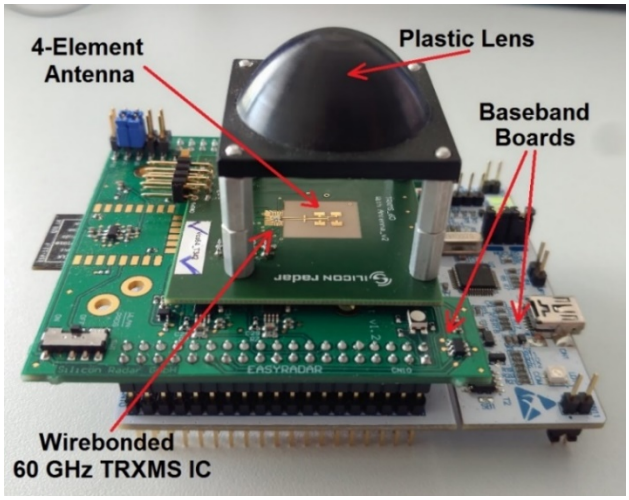

Figure 6.3: FMCW radar evaluation board demonstrated using 60-GHz TRM IC with the simulated 3 cm x 3 cm Lens [18].

6.2 Real-time FMCW Radar Measurements

With some of the designed transceivers, some including the packages as well, real-time FMCW radar measurements are conducted for characterization of their suitability in such applications. Mainly simple range measurements are carried out and the results are shared in the following figures which are already published in [15] – [19].

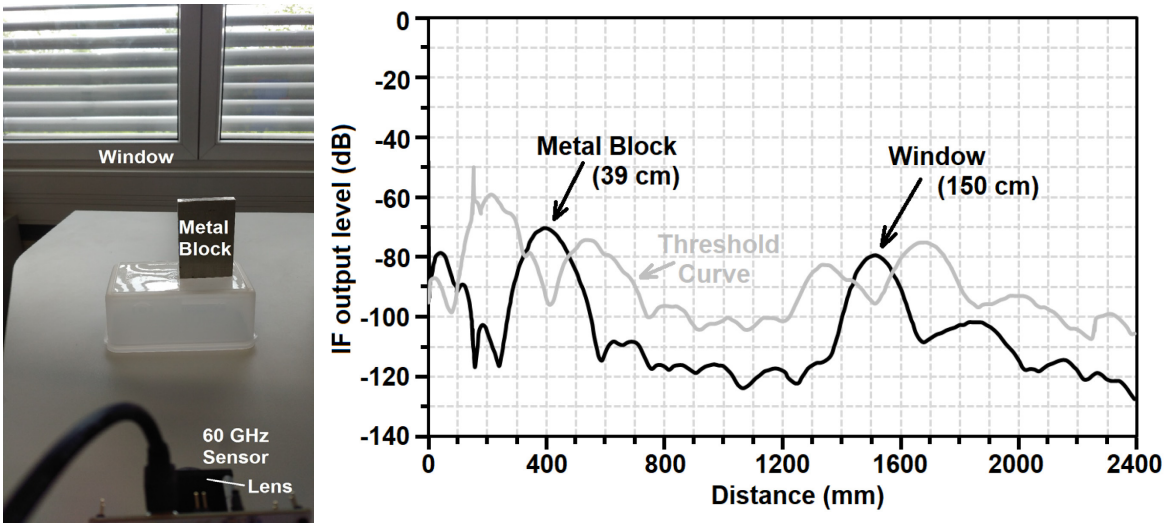

Figure 6.4: Simple indoor measurement using the radar board of 60-GHz TRM including the lens [18].

Considering a very simple indoor environment having two available targets (see Figure 6.4), these objects located very close to radar utilizing the 60 GHz TRM IC are clearly captured. On the same graph aside from the main detection curve, another curve is plotted as well which shows

an automatically set threshold helping differentiating the fake targets. Such false alarms could emanate from either internal leakage and reflections or noise from the environment and components on the baseband system. The objects with detected levels staying below this curve are treated as fake targets. However the threshold level could be adjusted through the GUI so that the IF levels of real targets still staying below this threshold could be put above in case of low level of reflection from the target due to many reasons. Besides using the same graph, the blind spot or the dead zone of radar at close ranges is visible as well.

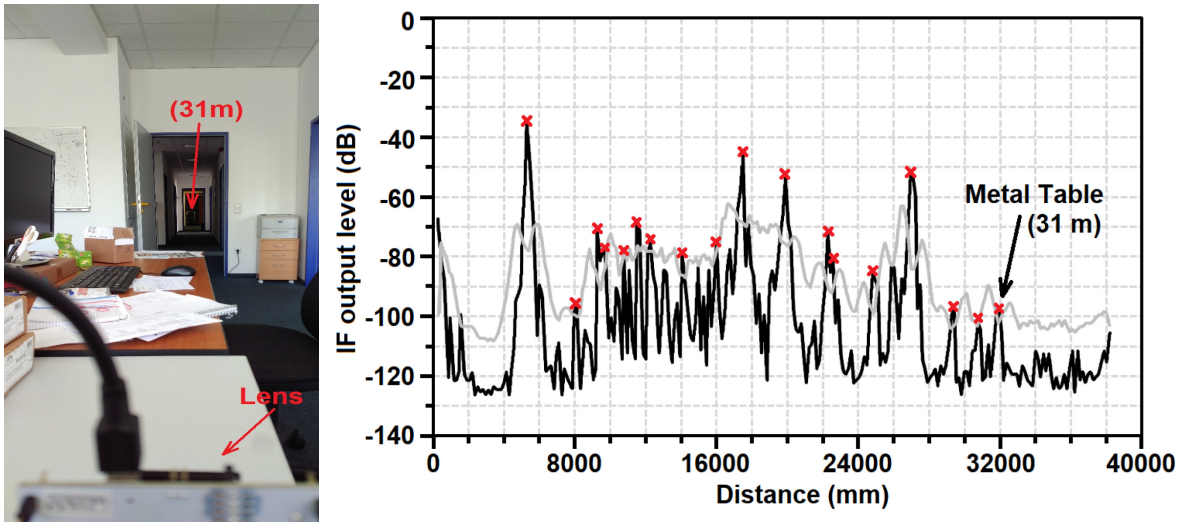

Figure 6.5: Complex indoor measurement using the radar board of 60-GHz TRM including the lens with the farthest available target being the metallic table at 31 m [18].

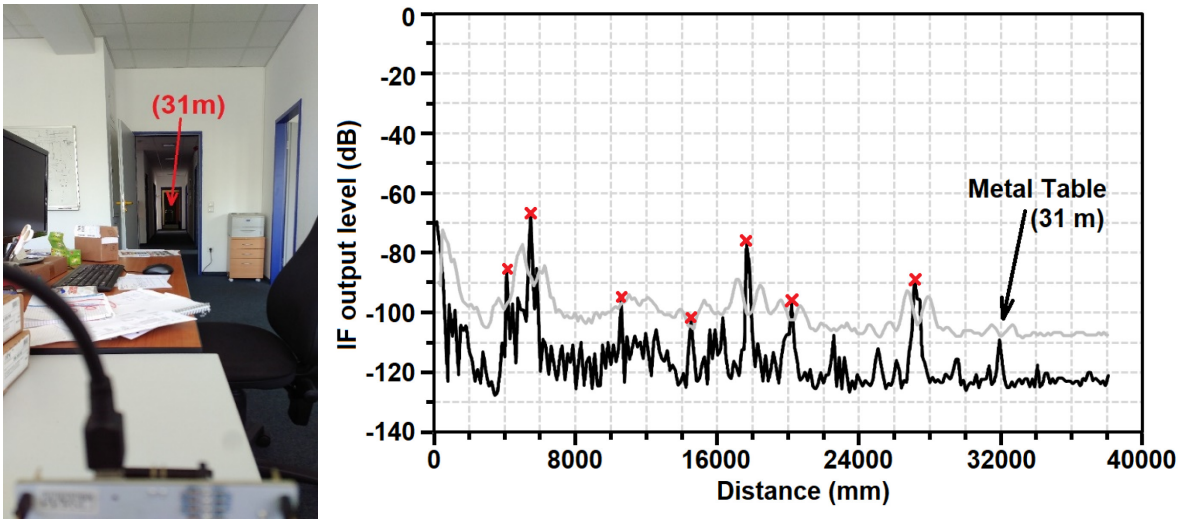

Figure 6.6: Complex indoor measurement using the radar board of 60-GHz TRM excluding the lens with the farthest available target being the metallic table at 31 m (below the detection threshold, needs threshold adjustment) [18].

Another indoor measurement with the same chip is conducted with and without the lens to see the effect of increased directivity on the antenna side (see Figure 6.5 and Figure 6.6 respectively). The farthest target in this scenario is the metal table located at the end of hallway which is around 31 m, and it is detectable by the radar. Yet in the second scenario where the lens is excluded, the IF level stays below the threshold curve, hence it is not recognized as a real target which is to be adjusted depending on the application requirements. With the integration of lens quite many of the objects in environment are detected, however a clutter region is observed as well which results from multiple reflections. The disappearing targets in the no-lens case are due to the orientation mismatch of the radar while dismantling of the lens.

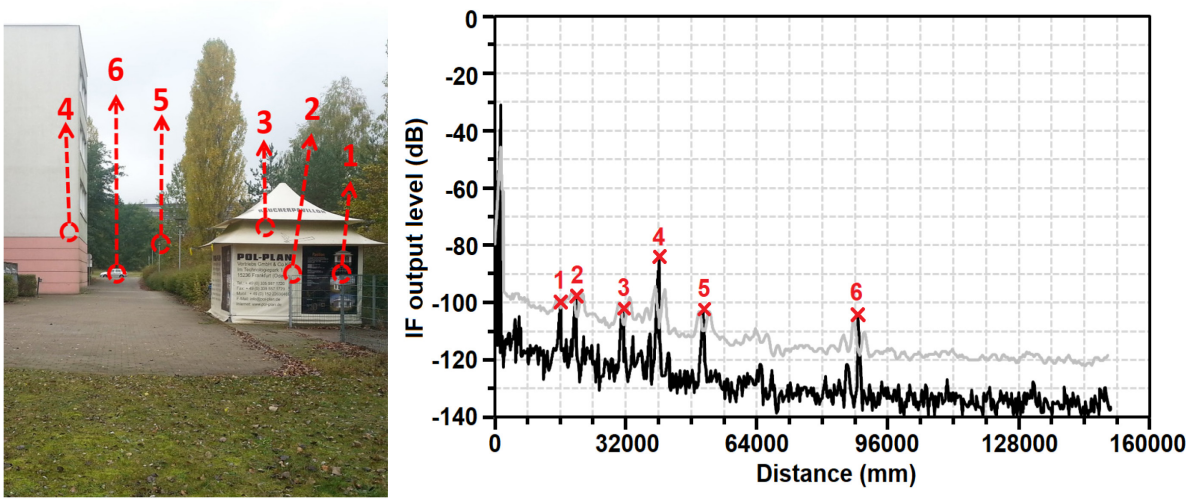

Figure 6.7: Outdoor measurement using the radar board of 60-GHz TRM including the lens with the farthest available target being the mid-sized vehicle at 90 m [18].

Using the environment in Figure 6.7, maximum detection range is tried to be extracted. Since the measurement area is limited, the farthest target being a mid-sized vehicle at 90 m is detected with all the other objects highlighted as well. Because the increased directivity causes a pointing beam, it is quite hard to mechanically stabilize the system and attain steady results that is why the closer targets have less or comparable output power with the farthest target, yet this could be corrected with a more robust system. On the other hand, the SNR level is still quite high, more than 30 dB at such distance, thus it is assumed that the maximum detectable range could be extended beyond 120 m even with such a small lens having a size of 3 cm x 3cm. The range could be further increased with a bigger lens or antenna and a lower required SNR level for the detection.

The BSA package in Section 5.3 is also characterized for FMCW functionality as well. Using the same environment in Figure 6.11 chosen for 122-GHz TRM chip performance evaluation, the measurement results in Figure 6.8 are achieved. The lens is omitted in this case to have a comparison with the antenna performances, where the maximum detectable range of radar benefits the increased element size of 16 patches. It is obvious that the metallic door frames are revealed by the radar with quite high SNR levels together with the target at 97 m away defining already the

boundary of measurement place. Having the lens in front would significantly boost the SNR and would allow for much clearer target detection. The minor differences between two measurements with 60- and 122-GHz chipsets come from the positioning of evaluation boards and field of view which could be corrected with a neat alignment to match both results.

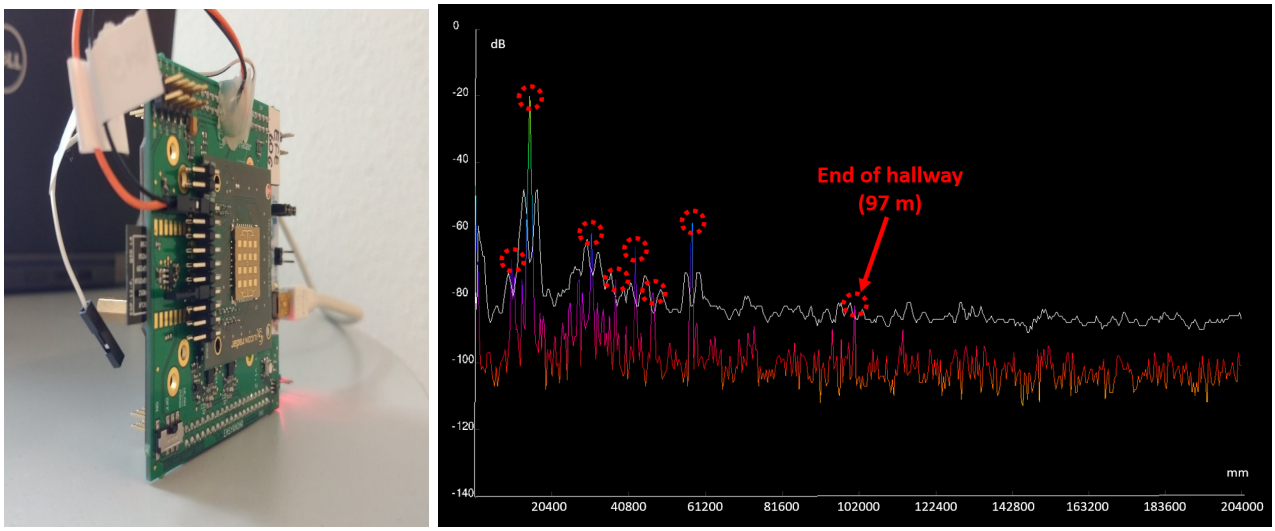

Figure 6.8: Complex indoor measurement using the radar board of 60-GHz TRM in the BSA package (having 4 x 4 antennas and excluding the lens) with the farthest available target being the metallic door at 97 m.

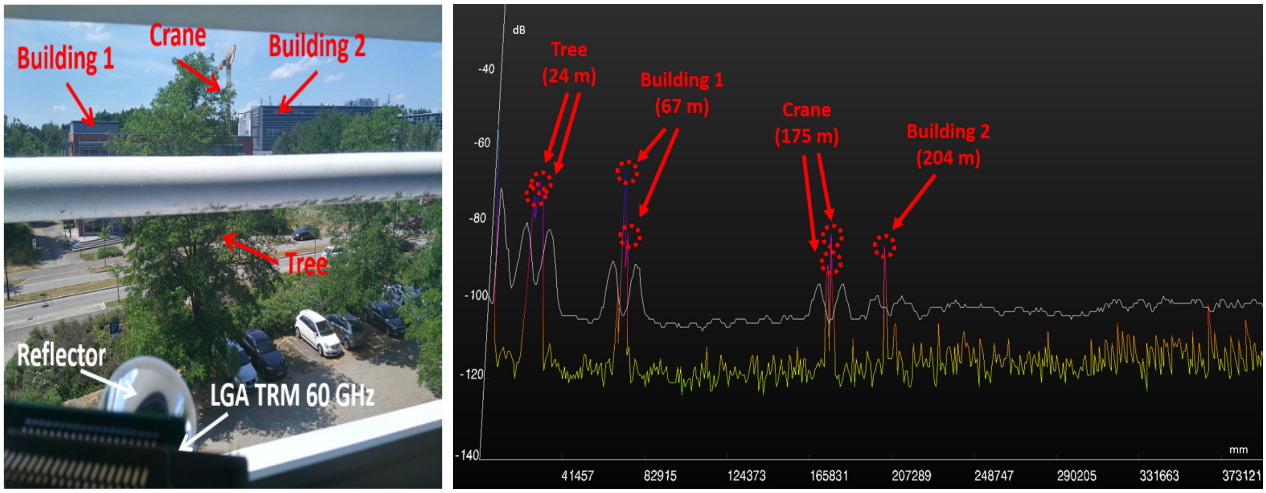

Figure 6.9: Outdoor measurement using the radar board of 60-GHz TRM in the LGA package (having 4 x 4 antennas and a reflector with 40 dB gain) with the farthest available target being the building at 204 m.

As shown in Figure 6.9, integrating a 40 dB reflector on top of the 2 x 2 antenna in 60-GHz TRM LGA package version yields a maximum detection range of 204 m (due to limited measurement environment) with high SNR even considering the reduced transmitted output power as a result of package tolerances which brings the noise floor to much higher levels compared to other versions.

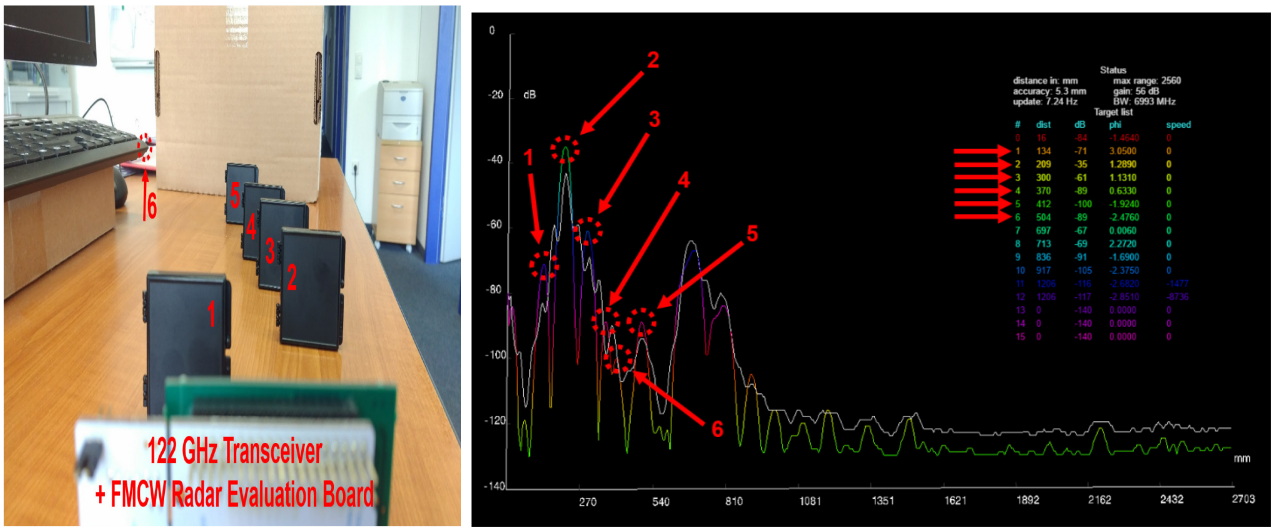

Figure 6.10: Simple indoor measurement using the radar board of 122-GHz TRM including the lens to detect closely spaced targets [15].

Same measurements are carried out for 122-GHz TRM IC as well. In Figure 6.10, target detection of closely spaced objects is illustrated. To be able to distinguish between these targets, available bandwidth is increased to 7 GHz allowing for a theoretical range resolution of 20 mm without considering the coefficients of baseband windowing functions affecting the achievable resolution. In measurements close results are achieved where the minimum separation is set to 40 mm while the remaining change between 50 mm to 100 mm. In results, all the targets are mapped successfully in the GUI environment.

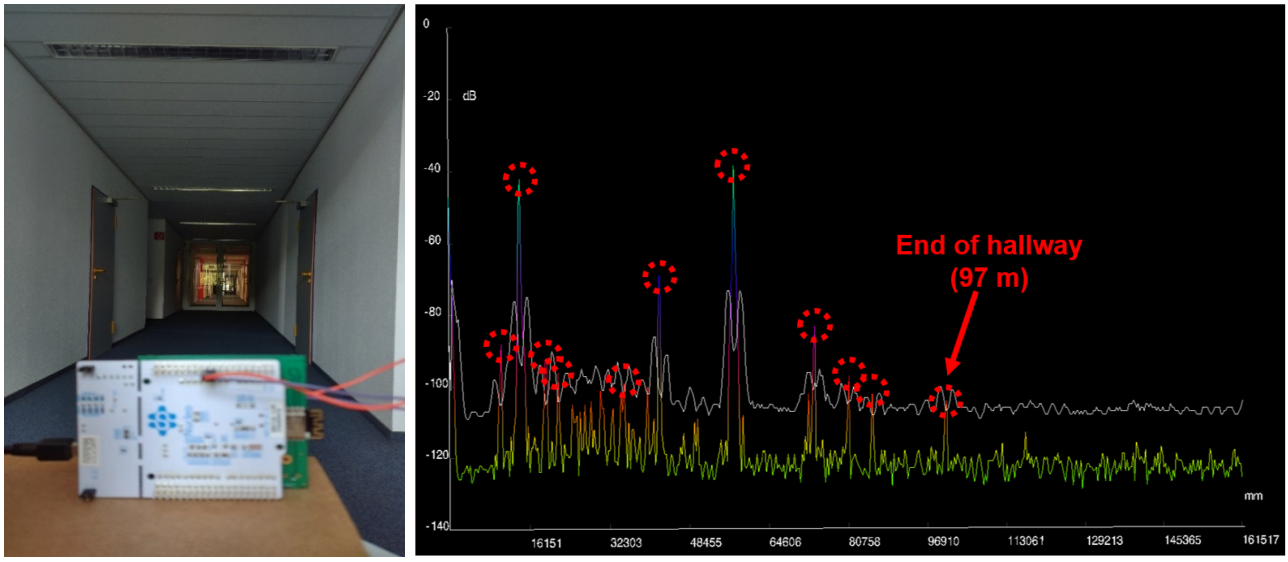

Figure 6.11: Complex indoor measurement using the radar board of 122-GHz TRM including the lens with the farthest available target being the metallic door at 97 m [16].

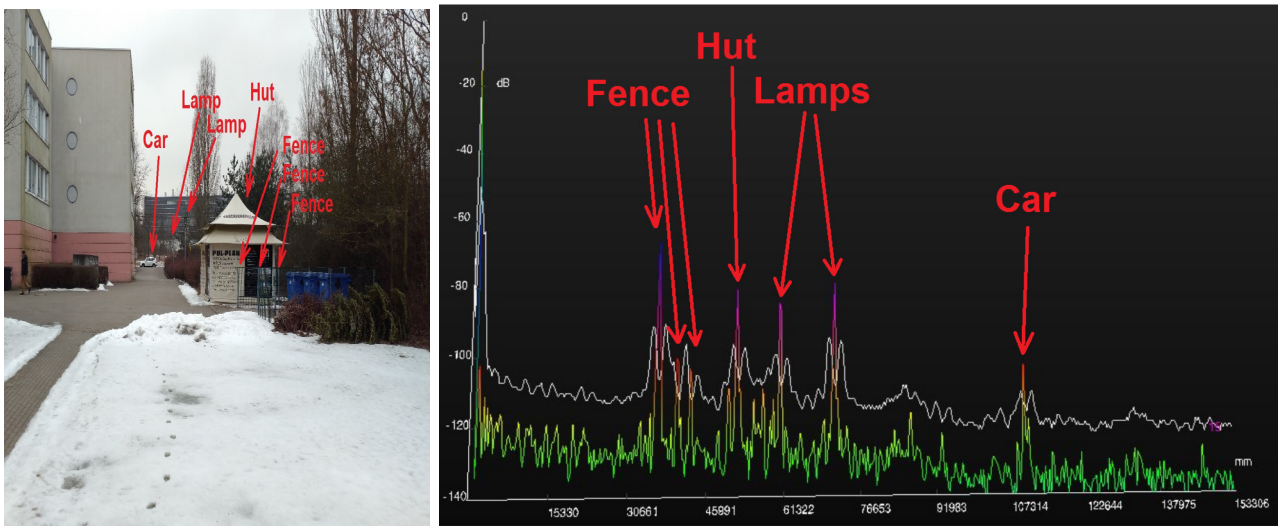

Figure 6.12: Outdoor measurement using the radar board of 122-GHz TRM including the lens with the farthest available target being the mid-sized vehicle at 107 m [16].

In order to detect much farther objects, the FFT size, number of samples and operation bandwidth is set accordingly. As shown in Figure 6.11, the metallic door frame at the very end of hallway around 97 m is captured by the radar using the same lens while performing a high SNR of around 25 dB. The closer door frames achieve higher IF levels thanks to high baseband amplifier gain. Finally the same measurement environment for the evaluation of 60-GHz TRM radar is used again to see the maximum detection range (see Figure 6.12). According to results the car at 107 m is captured by the radar with all the other closer targets appearing on the GUI as well. IF level at such ranges is observed to be quite high and the radar is assumed to be able to measure much farther distances at the expense of reduced accuracy.

6.3 Summary of the FMCW Radar Measurement Results

In summary, all the designed TRM and TR2 transceivers are measured using FMCW radar evaluation boards, and the results of TRM versions are share in this chapter (the others are skipped to avoid repetitiveness). Since the measurements did not take place in an anechoic chamber or with ideal setup, resolution and accuracy measurements are not conducted, but theoretical numbers for these are provided. With the TRM 60- and 122-GHz chips, objects at distances more than 100 m are clearly captured by the radar with high SNR levels. From this, it could be concluded that the proposed chips suit well to targeted FMCW radar applications. The comparison of these results with the state-of-the-art works presented in literature [18], which the TRx functionalities are proven with their demonstrators, are shared in Table 2 below. With the presented results in [17] – [19] in the context of this thesis using the previous versions of each chipset, the radar

performances would be further boosted considering the increased output power and wider bandwidth with the new generation of chips stated in Table 1.

Table 2: Comparison of the Demonstrated SiGe BiCMOS Radar Transceivers in Literature [18]

Ref. [#]	Freq (GHz)	Topology	BW (GHz)	Pout (dBm)	PDC (W)	Chip Area (mm²)	Demonstrator Purpose (Reported)
[29]	20.5 – 28.5	M / 1R / 1T	8	-1	0.245	1.51	FMCW radar for high accuracy (± 250 µm at 3 m)
[31]	23.5 – 25.5	B / 2R / 1T	2	1	0.400	1.54	FMCW Radar
[32]	23.2 – 26.2	B / 1R / 1T	3	0	0.240	2.04	FMCW Radar
[23]	54 – 64	M / 1R / 1T B / 1R / 1T	10	6 10	0.924 0.924	6.72 6.72	FMCW radar for high accuracy (< 0.23 mm at 3 m) (using 2 GHz BW)
[57]	55.8 – 65.8	B / 1R / 1T	5	11.5	0.594	3.72 (ext. LO)	FMCW radar for high accuracy (< 6.1 µm at 1 m)
[17]*	58.3 – 63.9	B / 2R / 1T	5.6	10	0.759	1.73	FMCW radar for high range (> 70 m)
[18]*	58.3 – 63.9	M / 1R / 1T	5.6	6.4	0.520	1.03	FMCW radar for high range (> 90 m)
[26]	59 – 64	B / 1R / 1T	5	-	-	-	FMCW radar for high range (> 78 m)
[4]	68 – 93.6	M / 1R / 1T	25.6	-2	0.488	3.04	FMCW radar for high resolution (< 7.12 mm at 2.1 m) and accuracy (< 0.36 µm)
[3]	75 – 77	M / 4R / 4T	2	2	-	-	FMCW radar for high angular resolution
[38]	76 – 78	B / 4R / 3T	2	-	-	-	FMCW radar for high angular resolution (2.4°) (using 5 TRx)
[36]	76.5 – 80.75	B / 1R / 1T	4.25	6.2	1.2	5.40	PRN radar for high accuracy (< 1.02 cm) and resolution (< 3.50 cm)
[39]	91 – 97	M / 1R / 1T	6	6.5	0.610	1.10 (ext. LO)	FMCW radar for high range and angular resolution (using 4 TRx)
[14]	115 – 125	B / 2R / 2T	10	5	1.182	10.14 (int. antenna)	FMCW radar for high accuracy (< 15.06 µm at 2 m)
[57]	116.6 – 126.6	B / 1R / 1T	10	5	0.627	3.72 (ext. LO)	FMCW radar for high resolution (< 3 cm at 2.5 m)
[24]	121 – 124	B / 1R / 1T	3	6	0.636	-	FMCW Radar (using 1 GHz BW)
[12]	121 – 127	B / 1R / 1T	6	-4	-	1.26	FMCW radar for high accuracy (< 5 µm at 35 mm)
[16]*	120.8 – 128.1	M / 1R / 1T	7.3	2	0.891	0.97	FMCW radar for high range (> 107 m)
[66]	120 – 130	B / 1R / 1T	10	0	0.560	3.60 (ext. LO)	FMCW radar for high resolution (< 3.9 cm at 2.45 m)
[42]	104.4 – 161.2	B / 1R / 1T (separate ICs)	56.8	-	1	2.1 Rx / 2.1 Tx (int. antenna, ext. LO)	FMCW radar for high resolution (< 5 mm at 26 cm)
[8]	122 – 170	M / 1R / 1T	48	-1 to -7	0.650	3.86	FMCW radar for high accuracy (< 1 µm at 65 cm) and resolution (< 5.88 mm)
[41]	136 – 150	B / 1R / 1T	14	4	0.724	1.16	FMCW radar
[77]	152 – 172	B / 1R / 1T	20	2	0.855	1.40 (ext. LO)	FMCW radar for high accuracy (< 24 µm at 2.54 m)
[46]	210 – 270	M / 1R / 1T	60	5	-	3.19 (ext. LO)	FMCW radar for high resolution (< 2.57 mm)
[45]	210 – 252	B / 1R / 1T	42	-	-	2.85 (int. antenna)	FMCW radar for high resolution (< 4.93 mm), SAR imaging

* Represents the works presented in publications ([17], [18], [19]) based on the thesis study. The demonstrators are realized with the previous versions of each chipset, thus the performances of each have already been improved.

** M-B / nR /nT: Monostatic-Bistatic topology with n number of Rx and m number of Tx channels

7 Conclusion and Future Works

Within the scope of this thesis, various single- and multi-channel compact TRx chips operating in the ISM bands around 60- and 122-GHz are designed using high-performance and low-cost SiGe BiCMOS technology with 250 / 340 GHz of f_T / f_{max}. These chips include monostatic TRx with and without integrated antenna implemented for basic FMCW functionality, double-receive-channel TRx for extraction of angle-of-arrival in the simplest way, and finally, four-receive four-transmit MIMO TRx which aim for higher angular resolution.

All the internal circuit blocks of transceivers are designed adopting differential architectures. The simulations are completed using full electro-magnetic models including all the inductors, transmission lines, capacitors, input / output pads with ESD structures and via connections until the transistor inputs where only the foundry models of transistors and resistors are integrated on schematic level. In this way coupling and all the interference between each block are taken into account which allows for re-optimization of each circuitry as well. Even though the TRxs are intended for different use cases, internal blocks are almost the same with minor optimizations to satisfy the matching between each. The main differences mainly come from either the LO signal distribution network, which necessitates updates in power division section and VCO fundamental frequency and multiplication chain, or the interface between Tx / Rx channels and input / output pads so that balun and isolation couplers in front are designed. Since the Tx and Rx channels are almost the same, similar measured performances are achieved except the differences emanating from integration of these balun and coupler structures. These additional blocks reduce the Tx output power and Rx conversion gain while increasing the Rx noise figure, however such results are unavoidable due to requirements depending on the application which decides on the required TRx architecture. Based on the measurement results, a general performance table could be drawn as in the following way where 14.5 / 2 dBm of output power is obtained from Tx for 60- / 122-GHz TR2 versions, whereas the conversion gain is around 21 / 12 dB in general with an IP_{1dB} of -14 / -15 dBm. The operation bandwidths of VCOs, on the other hand, are 9.6 / 7.4 GHz in the ranges of 55.5 – 65.1 / 118.9 – 126.3 GHz. However the 3-dB gain bandwidths extend much beyond these TRx operation ranges. The TRM chips utilize almost the same building block so that the measurement results pointed out a reduced performance by the level of front coupler insertion loss. The most advanced chipset is the 60-GHz MIMO TRx allowing for cascading multiple MIMO TRxs to be chained using their 20-GHz LO signal inputs and outputs. Increasing the number of

active channels would eventually provide higher angular resolution for the targeted FMCW applications.

In order to create a high-performance complete product which could support large volumes, antenna integration and package and interconnect implementations play crucial roles in this process. Therefore investigation of these are realized in the thesis as well and different packaging solutions addressing these issues are offered. The packages utilize wirebond and solder ball interconnects which require a know-how about the effects of wirebonds on matching networks connecting the antenna. By this way the necessity of shorter wirebonds or even replacement of these with the available flip-chip type technologies employing solder balls on chip pads would be interpreted. The packages including wirebonds are applied to 60-GHz version since the effect of these on high-frequency networks could still be eliminated by proper compensation networks as opposed to 122-GHz versions. In this context, LGA packaging with the idea of using standard PCB technology within the size of a regular QFN package while having a regular lead frame is implemented for 60-GHz TRM, TR2 and MIMO chips. To shorten the wirebonds, cavity openings are applied and the chips are buried inside. Matching networks are implemented considering the wirebonds and in-package-vias connecting to the outer pad in lead frame. From the TR2 chip using this package, high performances are obtained since the matching structures are not complicated and the package is quite compact, which allows shorter RF signal routing, due to number of control pads required for the chips. However its TRM counterpart experiences much higher losses even though it has much simplified package interconnect model. This proves the adverse outcomes of manufacturing tolerances yielding lower performances. Specifically for MIMO chips, high-resolution EWLB packaging is adopted which benefits two additional redistribution layers for signal routing where one of the layers is used as a ground plane for microstrip transmission lines required for high-frequency outputs. The interconnects are made of solder balls having diameters around 50 µm forming a very low inductance, hence not affecting the overall performance. The final package would be flipped and mounted on board from its quite standard BGA with 500 µm pitch. Compared to the LGA package designed for the MIMO chip as well, EWLB performs much better in terms of S-parameter results. For the TR2 chip, interposer packaging technology (IPR) is applied where the structure is quite similar to EWLB with additional routing layers where the main aim is to address for the heat dissipation issue in EWLB concept. Instead of the molding structure in EWLB, the chip is stacked on a high-resistivity interposer substrate on which a dielectric material and the metallization layers are grown. The package gives BGA outputs for both the DC and RF connections. Yet considering the cost issues, LGA package for TR2 offers a better performance. Another package option, namely BSA, is developed for 60-GHz TRM chip where it is stacked on the back side inside of a high-frequency substrate cavity. The wirebonded chip has connections on the same side to vias connecting to the top side of package where 4 x 4 differential antenna is placed. The package DC connections are located on the bottommost metal layer on cavity substrate. On the other hand, TRM with integrated antenna chips are packaged inside a modified QFN package where the exposed chip bottom is glued on a silicon plate of 5 x 5 mm^2 on which the lead frame is printed

and the DC connections are wirebonded. In order to focus the main radiation on the back side, a silicon lens of 4.5 x 4.5 mm^2 which boost the antenna directivity is utilized. This custom package is adopted by both 60- and 122-GHz chips and compared to 60-GHz chip, high performance could be achieved from the 122-GHz chip since the package and lens is optimized for it. Among these packages, BSA and Silicon package models are already measured meaning that 60-GHz TRM chips including on-chip integrated antenna could be promoted as product. On the other hand, LGA, EWLB and IPR package manufacturing for 60-GHz MIMO, TR2 and TRM chips are still on-going. However they are expected to work with quite high performance since both the TRxs have already achieved nice metrics proven with the measurement results and the packages include low loss transmission sections for the high frequency outputs. The LGA concept for MIMO is expected to achieve a poor, yet acceptable performance due to higher package losses. On the contrary, its TR2 and TRM counterparts would exert high performance thanks to smaller package, hence shorter RF signal routing.

In order to test the FMCW radar functionality of chips, various antennas centered at 60- and 122-GHz are developed on high-frequency PCB substrates. Since wirebond compensation networks for the bare dies could be realized, PCB antenna designs offer low-cost and high performance solutions. Simple patch antennas are employed and modified in structure to adapt to different radar applications. Especially for TRM based sensors, a compact plastic lens with 3 cm x 3 cm in size increased the detectable range. Other TRx configurations could benefit the high gain of such lens, yet a performance degradation might occur due to distinct focal points of Tx and Rx antennas. This issue disappears with the monostatic architecture employing a single antenna for both transmission and reception. The TRM chips employ 2 x 2 patch antennas giving more than 12 dBi of directivity which is enhanced further with the addition of this plastic lens by around 12 dB. By this way, two way antenna gain improves by 24 dB which directly translates into higher detection range and SNR. The produced pencil beam having a 3-dB beamwidth of 8° could be beneficial for many other applications as well. On the other hand, all the Tx / Rx channel outputs of TR2 and MIMO chips are wirebonded on 1 x 5 series fed patch antennas resulting in 12 dBi of directivity with 17° of beamwidth in the E-plane. Compensation networks are implemented in a very limited area, and low-profile baluns are designed and placed at the inputs due to complexity of on-board routing of such high number of channels in differential configuration on a PCB technology which already has quite high trace / spacing widths limiting the quality of impedance matching parts. Specifically for the MIMO version, correlation between antennas indicating the measure of how good the antennas are designed is simulated in the end which guarantees a high performance MIMO operation.

Considering these design steps and measured chip performances, real time FMCW measurements are conducted using a commercial radar evaluation board on which the manufactured boards including the radar chips and antennas are directly connected. This evaluation board integrates a PLL to control the tuning range of each TRx within a predefined saw-tooth chirp sweep time. Having the transmitted signals from TRx reflected back from the target, IF beat frequency with

respect to the distance of target appearing at the Rx outputs are directed to filter and baseband amplifier stages before digitization successively. Then this data is further processed with multiple FFT and detection algorithms through microcontroller to map the distances and velocities of various targets. In the end using a GUI environment integrated in the radar evaluation board, the measurements are realized. According to these, the TRM chips could achieve more than 100 m of measurement distance, thanks to their high output power, when equipped with a compact lens with only a size of 3 cm x 3cm. With larger lens sizes, higher target detection ranges would be attained. The theoretical range resolution of these 60- and 122-GHz TRM versions are 15 mm and 21 mm which are reduced further with windowing functions. Similar measurements are conducted for TR2 chips with two different boards. Using one of them which includes the same antennas in TRM chips, the maximum detection range is found around 75 m with the same lens. This decrease is due to the tilt in focal point between Tx and Rx antennas which worsens as the distance gets higher. Due to limited measurement capabilities, range resolution and accuracy measurements could not be conducted.

In order to achieve products with higher performance, couple improvements could be realized both on the chip and package designs. The main optimizations should be applied to 122-GHz transceiver versions, because the measurement results pointed out much lower transmitted output power than what is achievable even the possible reductions due to fabrication tolerances and modelling errors are counted. An updated version would help improving the detection range in FMCW radar applications. Another point to note is that although wirebonds on RF path provide easy and quick solution for radar functionality tests, it reduces the overall product performance in operational bandwidth, transmitted power and conversion gain in terms of the packaging. Unless low-cost solutions are avoided, it is quite fragile to fabrication tolerances and the overall performance becomes even more limited by the PCB process tolerances in combination with the employed wirebonds. Therefore solutions including solder bumps and flip-chip under different names depending on the utilized technology should be adopted. This comes with higher costs considering the solutions offered for heat dissipation issue, however provides higher performances and reliability which facilitates the RF board manufacturing at the same time. As previously explained, many of the package concepts are still in manufacturing process. Therefore measurements of these – both on chip level and system level – will be completed in the next phases. Using a proper measurement setup will also help revealing significant radar measures such as range resolution and accuracy, which will be carried out as well. On the other hand, angular resolution metrics for TR2 and especially MIMO chips will be extracted using dedicated radar boards benefiting antennas with certain element separations appropriate for MIMO applications.

In conclusion, 60- and 122-GHz radar chipsets with high emphasis on their design steps, simulation and chip-level measurement results and real-time FMCW measurement results together with the designed package and antenna concepts are presented in this thesis. Looking at the successful measurement results, it proves the suitability of each TRx chip in FMCW radar systems for various radar applications.

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List of Figures

Figure 1.1: One-way average atmospheric attenuation of mm-Wave frequencies at sea level highlighting the common ISM bands. 2
Figure 2.1: Block diagram of a typical target detecting radar system. 7
Figure 2.2: FMCW system illustration showing chirp modulation and beat frequency spectrum of the detected targets. 8
Figure 2.3: Block diagram of the single-channel monostatic 60-GHz TRx. 15
Figure 2.4: Block diagram of the single-channel monostatic 60-GHz TRx with integrated dipole antenna. 15
Figure 2.5: Block diagram of the double-receive-channel 60-GHz TRx. 16
Figure 2.6: Block diagram of the 60-GHz MIMO TRx with 4-Tx and 4-Rx channels [19]. 18
Figure 2.7: Block diagram of the massive MIMO chain composed of multiple scalable MIMO TRxs [19] 19
Figure 3.1: Cross section of the 7-layer SiGe BiCMOS technology. 22
Figure 3.2: (*Left*) Minimum-length HBT transistor fT / fmax and (*right*) corresponding maximum available gain and noise figure with respect to base-to-emitter voltage at 60-GHz. 22
Figure 3.3: Concept of ESD protection at low- and high-frequency pads. 23
Figure 3.4: Schematic of a general use bias circuit based on current mirror topology. 24
Figure 3.5: Schematic and simulation results of a CMOS inverter. 25
Figure 3.6: Schematic and layout of 60 GHz differential two-stage cascode LNA circuit. 26
Figure 3.7: Simulation results of 60 GHz LNA: (*top left*) S-parameters, (*top right*) gain and noise figure, (*bottom left*) gain with respect to control options, (*bottom right*) gain and output power with respect to frequency. 27
Figure 3.8: Simulation results of 122 GHz LNA: (*top left*) S-parameters, (*top right*) gain and noise figure, (*bottom left*) gain with respect to control options, (*bottom right*) gain and output power with respect to frequency. 28
Figure 3.9: Schematic and layout of 60 GHz differential LC Wilkinson Power Divider. 29
Figure 3.10: Simulation results of 60 GHz differential LC Wilkinson Power Divider: (*left*) S-parameters, (*right*) insertion phase at the divider outputs. 29
Figure 3.11: Schematic and layout of 60 GHz differential I/Q signal generator. 30
Figure 3.12: Simulation results of 60 GHz differential I/Q signal generator: (*left*) S-parameters, (*right*) insertion phase at the divider outputs. 30
Figure 3.13: Schematic of 60 GHz double-balanced Gilbert-cell based quadrature mixer. 31
Figure 3.14: Layout of 60 GHz double-balanced Gilbert-cell based quadrature mixer. 31
Figure 3.15: Simulation results of 60 GHz Mixer chain: (*top left*) output power vs. LO power, (*top right*) conversion gain and noise figure with respect to LO power, (*bottom left*) conversion

gain and output power with respect to LO power, (*bottom right*) IF output voltages in time domain. 32

Figure 3.16: Simulation results of 122 GHz Mixer chain: (*top left*) output power vs. LO power, (*top right*) conversion gain and noise figure with respect to LO power, (*bottom left*) conversion gain and output power with respect to LO power, (*bottom right*) IF output voltages in time domain. 33

Figure 3.17: Layout of 60 GHz Rx channel highlighting the sub-blocks (450 µm x 250 µm)... 34

Figure 3.18: Simulation results of 60 GHz Rx channel: (*top left*) output power vs. LO power, (*top right*) conversion gain and noise figure with respect to LO power, (*middle left*) conversion gain and output power with respect to LO power, (*middle right*) IF output voltages in time domain, (*bottom left*) conversion gain and output power with respect to frequency, (*bottom right*) conversion gain and noise figure with respect to temperature. 35

Figure 3.19: Simulation results of 122 GHz Rx channel: (*top left*) output power vs. LO power, (*top right*) conversion gain and noise figure with respect to LO power, (*middle left*) conversion gain and output power with respect to LO power, (*middle right*) IF output voltages in time domain, (*bottom left*) conversion gain and output power with respect to frequency, (*bottom right*) conversion gain and noise figure with respect to temperature. 36

Figure 3.20: Schematic and layout of 122 GHz Marchand Balun..... 37

Figure 3.21: Simulation results of 122 GHz Marchand balun. 37

Figure 3.22: Schematic and layout of 60 GHz high isolation coupler. 38

Figure 3.23: Simulation results of 60 GHz high isolation coupler: (*left*) input and output return losses, (*right*) insertion loss, isolation and coupling loss to power detector with respect to tuning voltage. 39

Figure 3.24: Simulation results of 122 GHz high isolation coupler: (*left*) input and output return losses, (*right*) insertion loss, isolation and coupling loss to power detector with respect to tuning voltage. 39

Figure 3.25: Class-A PA collector current and input voltage for swept input power levels for the fabricated 60-GHz PA. 40

Figure 3.26: Layout of 60 GHz differential two-stage cascode PA circuit. 41

Figure 3.27: Simulation results of 60-GHz PA: (*left*) S-parameters, (*right*) gain with respect to gain control options. 42

Figure 3.28: Simulation results of 60-GHz PA: (*top left*) gain and PAE at 60 GHz with respect to temperature, (*top right*) gain and output power at 60 GHz with respect to temperature, (*bottom*) gain with respect to temperature. 42

Figure 3.29: Simulation results of 122-GHz PA: (*left*) S-parameters, (*right*) gain with respect to gain control options. 43

Figure 3.30: Simulation results of 122-GHz PA: (*top left*) gain and PAE at 122 GHz with respect to temperature, (*top right*) gain and output power at 122 GHz with respect to temperature, (*bottom*) gain with respect to temperature. 43

Figure 3.31: BIST circuits and coupling mechanisms including power detectors in Tx channels of, (*left*) 60-GHz MIMO TRx, (*right*) 60- / 122-GHz TRM.....44
Figure 3.32: Layout of power detector coupler mechanism integrated to (*left*) high isolation coupler in monostatic TRxs and (*right*) Tx output pads in 60-GHz MIMO TRx. 45
Figure 3.33: Schematic and simulation results of power detector together with high isolation coupler in 60-GHz TRM. 46
Figure 3.34: Power detector output voltage with respect to temperature.....46
Figure 3.35: LO signal distribution networks for different chips including monostatic, double-receive, MIMO TRx. 47
Figure 3.36: Schematic of 60 GHz VCO integrated to a PA and a Frequency Divider. 48
Figure 3.37: Layout of 60 GHz VCO integrated to the single-stage buffer PA.....49
Figure 3.38: 60 GHz VCO, (*Left*) power levels: PA out1 / out2 output power, frequency divider and PA input power delivered from VCO core, frequency divider buffer output power, (*Right*) phase noise at 60 GHz.....49
Figure 3.39: 60 GHz VCO output voltage spectrum, (*Left*) at node-A, emitter terminal, (*Right*) at *LOout* of PA. 50
Figure 3.40: 60 GHz VCO output power with respect to swept tuning voltages for different (*Left*) operation temperature and (*Right*) supply pushing / pulling. 51
Figure 3.41: 60 GHz VCO with respect to swept tuning voltages for different operation temperature and supply pushing / pulling, (*Left*) LO output frequency, (*Right*) frequency divider output frequency. 52
Figure 3.42: Schematic of Divide-by-2 circuit composed of two D-latches and a buffer. 53
Figure 3.43: Block diagram of the divide-by-16 frequency divider and its divide-by-2 master / slave DFF sub-block. 53
Figure 3.44: Divide-by-16 frequency divider output voltage at each divide-by-2 output node. 54
Figure 3.45: (*Left*) Divide-by-16 frequency divider sensitivity measure with respect to temperature, (*Right*) Divide-by-2 frequency divider block output power spectrum at each division stage. 55
Figure 3.46: Schematic and layout of 20-GHz differential multiplexer.....56
Figure 3.47: Simulation results of 20-GHz differential multiplexer. 56
Figure 3.48: Schematic of 60-GHz frequency tripler. 57
Figure 3.49: Layout of 60-GHz frequency tripler.....58
Figure 3.50: Simulation results of frequency tripler core. (*top left*) S-parameters, (*top right*) harmonics at 10 dBm LO input at 20 GHz, (*bottom left*) conversion gain and output power with respect to input power for harmonics of 20 GHz LO input, (*bottom right*) conversion gain and output power with respect to LO input frequency for harmonics of 2 dBm 20 GHz LO input. ...59
Figure 3.51: Simulation results of frequency tripler including a single-stage PA. (*top left*) S-parameters, (*top right*) harmonics at 10 dBm LO input at 20 GHz, (*bottom left*) conversion gain and output power with respect to input power for harmonics of 20 GHz LO input, (*bottom right*)

conversion gain and output power with respect to LO input frequency for harmonics of 2 dBm 20 GHz LO input. 60

Figure 3.52: Simulation results of frequency tripler including a single-stage PA. Conversion gain and output power with respect to input power for the 3rd harmonic of 20 GHz LO input at different temperatures. 61

Figure 3.53: Conversion gain and output power with respect to input power for the 3rd harmonic of 20 GHz LO input at different temperatures for (*left*) tripler core, (*right*) tripler with single-stage PA. 61

Figure 3.54: Simulation results of frequency tripler including the three-stage PA. Conversion gain and output power with respect to input power for the 3rd harmonic of 20 GHz LO input at different temperatures. 62

Figure 3.55: Schematic and layout of 20-GHz single-stage cascode PA. 63

Figure 3.56: Simulation results of 20 GHz PA: (*top left*) S-parameters, (*top right*) gain with respect to temperature, (*bottom left*) gain and output power with respect to temperature, (*bottom right*) gain and PAE with respect to temperature. 63

Figure 3.57: Layout and simulation results of 60-GHz balun in two-way power for frequency tripler. 64

Figure 3.58: Schematic and layout of 60-GHz two-way power divider with a coupled output for frequency tripler. 65

Figure 3.59: Simulation results of 60-GHz two-way power divider with a coupled output for frequency tripler. 65

Figure 3.60: Schematic and layout of 60-GHz three-way power divider. 66

Figure 3.61: Simulation results of 60-GHz three-way power divider. 66

Figure 3.62: Simulation results of 122-GHz three-way power divider. 66

Figure 3.63: Layout of 60-GHz four-way power divider. 67

Figure 3.64: Simulation results of 60-GHz four-way power divider on Rx side. 68

Figure 3.65: Simulation results of 60-GHz combined LO power division stage. 68

Figure 3.66: Schematic of the complete LO chain in 60-GHz MIMO TRx. 69

Figure 3.67: Simulation results of the complete LO chain in 60-GHz MIMO TRx with respect to different gain options in *master* mode: (*top left*) conversion gain vs. input power at 20 GHz internal VCO input, (*top right*) output power vs. input power at 20 GHz internal VCO input, (*bottom left*) conversion gain vs. LO input frequency at 2 dBm internal VCO input, (*bottom right*) output power vs. LO input frequency at 2 dBm internal VCO input. 69

Figure 3.68: Layout and simulation results of 20-GHz balun at *LOin* and *LOout* pads in 60-GHz MIMO LO chain. 70

Figure 3.69: Simulation results of the complete LO chain in 60-GHz MIMO TRx in *slave* mode where internal VCO is disabled: (*left*) conversion gain and output power vs. input power at 20 GHz external LO input, (*right*) output power vs. LO input frequency at 2 dBm external LO input. 71

Figure 4.1: Photo of the fabricated 60-GHz TR2 transceiver chip occupying 1.46 mm x 1.06 mm area. 74
Figure 4.2: Measurement results of the 60-GHz TR2 TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to VCO tuning bits. 74
Figure 4.3: Measurement results of the 60-GHz TR2 TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V. 75
Figure 4.4: Measurement results of the 60-GHz TR2 TRx: (*left*) Tx output power vs. frequency, and (*right*) Frequency Divider output power vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V. 75
Figure 4.5: Measurement results of the 60-GHz TR2 TRx: Tx output power vs. frequency with respect to temperature. 76
Figure 4.6: Measurement results of the 60-GHz TR2 TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to temperature. 76
Figure 4.7: Measurement results of the 60-GHz TR2 TRx: (*left*) Tx output power vs. frequency with respect to Tx gain control voltages 0 V – 3.3 V, (*right*) Frequency Divider phase noise with respect to VCO tuning voltages. 77
Figure 4.8: Measurement results of the 60-GHz TR2 TRx: (*left*) Rx channel 1 conversion gain vs. frequency, (*right*) 5-MHz IF output voltages at 64.5 GHz. 77
Figure 4.9: Measurement results of the 60-GHz TR2 TRx: (*left*) Rx channel 1 conversion gain, and (*right*) IF channel 1 output power vs. Rx input power at 64.5 GHz with respect to Rx gain control voltages. 78
Figure 4.10: Photo of the fabricated 122-GHz TR2 transceiver chip occupying 1.54 mm x 0.92 mm area. 78
Figure 4.11: Measurement results of the 122-GHz TR2 TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to VCO tuning bits. 79
Figure 4.12: Measurement results of the 122-GHz TR2 TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V. 79
Figure 4.13: Measurement results of the 122-GHz TR2 TRx: (*left*) Tx output power vs. frequency, and (*right*) Frequency Divider output power vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V. 80
Figure 4.14: Measurement results of the 122-GHz TR2 TRx: Tx output power vs. frequency with respect to Tx gain control voltages 0 V – 3.3 V. 80
Figure 4.15: Measurement results of the 122-GHz TR2 TRx: (*left*) Tx output frequency vs. VCO tuning voltages, and (*right*) Tx output power vs. frequency with respect to temperature. 81

Figure 4.16: Measurement results of the 122-GHz TR2 TRx: Rx channel 1 conversion gain (*left*) vs. frequency, and (*right*) vs. Rx input power with respect to Rx gain control voltages at 122 GHz. 81
Figure 4.17: Measurement results of the 122-GHz TR2 TRx: 5-MHz IF output voltages at 122 GHz. 81
Figure 4.18: Photo of the fabricated 60-GHz TRM and TRMant transceiver chips occupying 1.42 mm x 0.84 mm and 1.64 mm x 0.84 mm area. 82
Figure 4.19: Measurement results of the 60-GHz TRM TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to VCO tuning bits. 83
Figure 4.20: Measurement results of the 60-GHz TRM TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V. 83
Figure 4.21: Measurement results of the 60-GHz TRM TRx: (*left*) Tx output power vs. frequency, and (*right*) Frequency Divider output power vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V. 84
Figure 4.22: Measurement results of the 60-GHz TRM TRx: (*left*) Frequency Divider phase noise at 1.74 GHz and 2.05 (corresponding to Tx operation frequencies of 55.6 GHz and 65.6 GHz), (*right*) Tx output power vs. frequency with respect to temperature. 84
Figure 4.23: Measurement results of the 60-GHz TRM TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to temperature. 85
Figure 4.24: Measurement results of the 60-GHz TRM TRx: (*left*) Tx output power vs. frequency with respect to Tx gain control voltages 0 V – 3.3 V, (*right*) Tx output power and Power Detector voltage vs. Tx gain tuning voltages. 85
Figure 4.25: Measurement results of the 60-GHz TRM TRx: (*left*) Rx channel conversion gain vs. frequency with respect to Rx gain control voltages, (*right*) 10-MHz IF output voltages at 60 GHz. 86
Figure 4.26: Photo of the fabricated 122-GHz TRM and TRMant transceiver chips occupying 1.35 mm x 0.76 mm and 1.49 mm x 0.73 mm area. 86
Figure 4.27: Measurement results of the 122-GHz TRM TRx: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to changing supply voltages between 3.3 V – 3.9 V. 87
Figure 4.28: Measurement results of the 122-GHz TRM TRx: (*left*) Tx output power vs. frequency with respect to changing supply voltages between 3.3 V – 3.9 V, (*right*) Tx output power vs. frequency with respect to temperature. 87
Figure 4.29: Measurement results of the 122-GHz TRM TRx: (*left*) Tx output power vs. frequency with respect to Tx gain control voltages, (*right*) Tx output power and Power Detector output voltage vs. Tx gain tuning voltages. 88

Figure 4.30: Measurement results of the 122-GHz TRM TRx: Frequency Divider phase noise at 1.86 GHz, 1.91 GHz and 1.97 (corresponding to Tx operation frequencies of 119.1 GHz, 122.2 GHz and 126.1 GHz). 88
Figure 4.31: Photo of the fabricated 60-GHz MIMO transceiver chip occupying 2.16 mm x 2.39 mm area) [19]. 89
Figure 4.32: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: (*left*) Tx output frequency and (*right*) Frequency Divider output frequency vs. VCO tuning voltages with respect to changing supply voltages between 3.0 V – 3.9 V. 90
Figure 4.33: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: Tx output power vs. frequency with respect to (*left*) Tx gain control voltages 0 V – 3.3 V and (*right*) changing supply voltages between 3.0 V – 3.9 V. 90
Figure 4.34: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: (*left*) Power Detector output voltage vs. frequency with respect to Tx gain control voltages 0 V – 3.3 V, (*right*) *LOout* output power and frequency vs. VCO tuning voltages. 91
Figure 4.35: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: (*left*) Rx channel 1 conv. gain vs. freq. with respect to Rx gain control voltages, and (*right*) Rx channel conv. gain vs. freq. 92
Figure 4.36: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: Rx channel 1 conversion gain vs. Rx input power with respect to Rx gain control voltages. 92
Figure 4.37: Measurement results of the 60-GHz MIMO TRx: 5-MHz IF output voltages at 60 GHz (*left*) from quadrature Rx channel 1, and (right) Rx channel 2. 92
Figure 4.38: Measurement results of the 60-GHz MIMO TRx in *slave* mode where external LO is applied: (*left*) Rx channel 1 conversion gain vs. frequency with respect to applied LO power from *LOin* pad, and (*right*) Rx channel 1 conversion gain vs. frequency with respect to Rx gain control voltages at -3 dBm LO input power. 93
Figure 4.39: Measurement results of the 60-GHz MIMO TRx in *slave* mode where external LO is applied: (*left*) Rx channel 1 conversion gain vs. Rx input power with respect to Rx gain control voltages at -3 dBm LO input power, (*right*) Tx output power vs. frequency with respect to Tx gain control voltages at -3 dBm LO input power. 93
Figure 4.40: Measurement results of the 60-GHz MIMO TRx in *master* mode where internal VCO is enabled: Frequency Divider phase noise at 4.81 GHz (corresponding to Tx operation frequency of 57.7 GHz). 94
Figure 5.1: PCB antenna concepts of 60-GHz TRM chips including wirebond compensation network. 98
Figure 5.2: PCB antenna concepts of 122-GHz TRM chips including wirebond compensation network. 98
Figure 5.3: Wirebond drawing and effect of wirebond length on return loss [18]. 99
Figure 5.4: Manufactured evaluation boards with 60- / 122-GHz TRM chips and PCB antennas [15], [18]. 100

Figure 5.5: Simulation results of PCB antenna of 60-GHz TRM chip including wirebond compensation network. 101
Figure 5.6: Simulation results of PCB antenna of 122-GHz TRM chip including wirebond compensation network. 101
Figure 5.7: Simulation results of PCB antenna of 60-GHz TRM chip including HDPE plastic lens at 1.5 cm. 102
Figure 5.8: Simulation results of PCB antenna of 122-GHz TRM chip including HDPE plastic lens at 1.5 cm. 102
Figure 5.9: Manufactured evaluation boards and PCB antennas with (*left*) 122-GHz TR2 (1 x 5 patch array), (*middle*) 60-GHz TR2 (1 x 5 patch array), (*right*) 60-GHz TR2 (2 x 2 patch array). 103
Figure 5.10: Simulation results of PCB antenna (1 x 5 patch array) of 60-GHz TR2 chip....104
Figure 5.11: Simulation results of PCB antenna (2 x 2 patch array) of 60-GHz TR2 chip....104
Figure 5.12: Illustration of one-dimensional 1 x 16 MIMO virtual array formation. 105
Figure 5.13: Illustration of two-dimensional 4 x 4 and 2 x 8 MIMO virtual array formations. 105
Figure 5.14: 60-GHz MIMO radar evaluation boards highlighting the PCB-based balun. 106
Figure 5.15: 60-GHz MIMO radar evaluation boards including antenna arrays for different virtual arrays. 106
Figure 5.16: Simulation results of PCB antenna (1 x 5 patch array) of 60-GHz MIMO chip (Rx1 is excited). 107
Figure 5.17: Simulation results of PCB antenna (1 x 5 patch array) of 60-GHz MIMO chip (Tx1 is excited). 107
Figure 5.18: Simulation results of PCB antenna (1 x 5 patch array) of 60-GHz MIMO chip showing MIMO Envelope Correlation Coefficients (*ECC*) between each antenna. 108
Figure 5.19: 122-GHz TRMant chip. 109
Figure 5.20: Simulation results of 122-GHz TRMant chips. 109
Figure 5.21: Simulation results of 122-GHz TRMant chip with Silicon-lens of 2.0 mm additional height and 5.5 mm radius. 110
Figure 5.22: Radar evaluation board of 122-GHz TRMant chip with Silicon-lens of 2.0 mm height and 5.5 mm radius. 111
Figure 5.23: 60-GHz TRMant Silicon package with integrated Silicon-lens stack-up. 111
Figure 5.24: 60- / 122-GHz TRMant, 5 x 5 mm^2 Silicon package and antenna. 112
Figure 5.25: 122-GHz TRMant Silicon package antenna simulation results. 112
Figure 5.26: Manufactured radar evaluation boards including (*left*) 122-GHz TRMant and (*right*) 60-GHz TRMant Silicon package. 113
Figure 5.27: Simple indoor measurement using the radar board of 122-GHz TRMant Silicon package including the hemispherical Silicon lens having 4.5 mm diameter directed towards the office ceiling. 113

Figure 5.28: Simple indoor measurement using the radar board of 122-GHz TRMant Silicon package including the hemispherical Silicon lens having 4.5 mm diameter and additional 3 cm x 3 cm HDPE lens on top directed towards the office ceiling. 114
Figure 5.29: Simple indoor measurement using the radar board of 122-GHz TRMant Silicon package including the Plastic lens having 11.0 mm x 7.5 mm size directed towards the office ceiling. 114
Figure 5.30: 60-GHz TRM BSA package PCB stack-up. 115
Figure 5.31: 60-GHz TRM 15 x 15 mm^2 BSA package and antenna 116
Figure 5.32: Photo of fabricated 60-GHz TRM BSA package and its view in radar evaluation board. 116
Figure 5.33: 60-GHz TRM BSA antenna simulation results (3D radiation pattern at 60 GHz). 117
Figure 5.34: 60-GHz TRM BSA antenna simulation results (radiation pattern at 60 GHz and return loss). 117
Figure 5.35: 60-GHz LGA package PCB stack-up. 118
Figure 5.36: 60-GHz TRM 6 x 6 mm^2 LGA package, top (RF and DC connections) and bottom (lead frame) 119
Figure 5.37: 60-GHz TR2 6 x 6 mm^2 LGA package, top (RF and DC connections) and bottom (lead frame) 119
Figure 5.38: 60-GHz MIMO 10 x 10 mm^2 LGA package, top (RF and DC connections) and bottom (lead frame). 119
Figure 5.39: Simulated 60-GHz TRM 6 x 6 mm^2 LGA package structure. 120
Figure 5.40: Return loss and insertion loss of 60-GHz TRM LGA package. 120
Figure 5.41: Simulated 60-GHz TR2 6 x 6 mm^2 LGA package structure 121
Figure 5.42: Return loss, insertion loss and port isolation of 60-GHz TR2 LGA package. 121
Figure 5.43: Simulated 60-GHz MIMO 10 x 10 mm^2 LGA package structure. 122
Figure 5.44: Return loss and insertion loss of 5-GHz frequency divider outputs of 60-GHz MIMO LGA package. 123
Figure 5.45: Return loss and insertion loss of 20-GHz *LOin* and *LOout* outputs of 60-GHz MIMO LGA package. 123
Figure 5.46: Coupling between 20-GHz *LOin* and *LOout* outputs of 60-GHz MIMO LGA package. 123
Figure 5.47: Return loss, insertion loss and port coupling of 60-GHz Tx / Rx outputs of 60-GHz MIMO LGA package 124
Figure 5.48: 60-GHz TRM 6 x 6 mm^2 LGA package mounted on the designed evaluation board. 125
Figure 5.49: 60-GHz TR2 6 x 6 mm^2 LGA package mounted on the designed evaluation board. 125
Figure 5.50: 60-GHz MIMO 10 x 10 mm^2 LGA package mounted on the designed evaluation board. 125

Figure 5.51: Measurement results of Tx output power in LGA packages of (*left*) 60-GHz TR2 and (*right*) 60-GHz TRM chips in comparison to their bare-die performances. 126
Figure 5.52: 60-GHz MIMO EWLB package stack-up. 127
Figure 5.53: Return loss and insertion loss of Marchand balun in 60-GHz MIMO EWLB package. 127
Figure 5.54: Simulated 60-GHz MIMO 8 x 8 mm^2 EWLB package structure with single-ended 60-GHz outputs. 128
Figure 5.55: Simulated 60-GHz MIMO 8 x 8 mm^2 EWLB package structure with differential 60-GHz outputs. 128
Figure 5.56: Simulated 5-GHz divider and 20-GHz *LOin* / *LOout* outputs in EWLB package structure. 129
Figure 5.57: S-parameter simulation results of differential 5-GHz frequency divider outputs in EWLB package. 129
Figure 5.58: S-parameter results of single-ended 20-GHz (*left*) *LOin* and (*right*) *LOout* outputs in EWLB package. 130
Figure 5.59: S-parameter results of differential 60-GHz Tx / Rx outputs in EWLB package. 130
Figure 5.60: S-parameter results of single-ended 60-GHz Tx / Rx outputs in EWLB package. 130
Figure 5.61: Simulated 60-GHz TR2 4 x 4 mm^2 IPR package structure with single-ended 60-GHz outputs. 131
Figure 5.62: S-parameter results of 60-GHz outputs in (*left*) single-ended and (*right*) differential IPR package versions. 132
Figure 6.1: Block diagram of radar signal processing evaluation board [18]. 135
Figure 6.2: Saw-tooth chirp train generated by PLL to be sent through the Tx for 5 GHz modulation bandwidth. 136
Figure 6.3: FMCW radar evaluation board demonstrated using 60-GHz TRM IC with the simulated 3 cm x 3 cm Lens [18]. 137
Figure 6.4: Simple indoor measurement using the radar board of 60-GHz TRM including the lens [18]. 137
Figure 6.5: Complex indoor measurement using the radar board of 60-GHz TRM including the lens with the farthest available target being the metallic table at 31 m [18]. 138
Figure 6.6: Complex indoor measurement using the radar board of 60-GHz TRM excluding the lens with the farthest available target being the metallic table at 31 m (below the detection threshold, needs threshold adjustment) [18]. 138
Figure 6.7: Outdoor measurement using the radar board of 60-GHz TRM including the lens with the farthest available target being the mid-sized vehicle at 90 m [18]. 139
Figure 6.8: Complex indoor measurement using the radar board of 60-GHz TRM in the BSA package (having 4 x 4 antennas and excluding the lens) with the farthest available target being the metallic door at 97 m. 140

Figure 6.9: Outdoor measurement using the radar board of 60-GHz TRM in the LGA package (having 4 x 4 antennas and a reflector with 40 dB gain) with the farthest available target being the building at 204 m.....140

Figure 6.10: Simple indoor measurement using the radar board of 122-GHz TRM including the lens to detect closely spaced targets [15].....141

Figure 6.11: Complex indoor measurement using the radar board of 122-GHz TRM including the lens with the farthest available target being the metallic door at 97 m [16]. 141

Figure 6.12: Outdoor measurement using the radar board of 122-GHz TRM including the lens with the farthest available target being the mid-sized vehicle at 107 m [16].....142

List of Tables

Table 1: Summary of the measurement results of fabricated TRxs..... 95
Table 2: Comparison of the Demonstrated SiGe BiCMOS Radar Transceivers in Literature [18] 143

List of Abbreviations

ADC	Analog-to-Digital Converter
BGA	Ball-Grid-Array
BIST	Built-In-Self-Test
BSA	Back-Side-Antenna package
DFF	D Flip-Flop
ECC	Envelope Correlation Coefficient
ECL	Emitter-Coupled-Logic
EIRP	Equivalent Isotropic Radiated Power
EM	Electro-Magnetic
ESD	Electrosatic Discharge
EWLB	Embedded-Wafer-Level Ball-Grid-Array
FAR	False Alarm Rate
FFT	Fast Fourier Transform
f_{max}	Maximum oscillation frequency
FMCW	Frequency-Modulated Continuous-Wave
f_T	Transit frequency
GUI	Graphical User Interface
HBT	Heterojunction Bipolar Transistor
HDPE	High-Density-Polyethylene
I / Q	In-phase / Quadrature
IC	Integrated Circuit
IF	Intermediate Frequency
IP_{1dB} / OP_{1dB}	Input / Output referred 1dB compression point
IPR	Interposer package
ISM	Industrial-Scientific-Medical
LC	Inductor-Capacitor
LGA	Land-Grid-Array
LNA	Low-Noise Amplifier
LO	Local Oscillator
MIM	Metal-Insulator-Metal
MIMO	Multiple-In Multiple-Out
MMIC	Monolithic Microwave Integrated Circuit
NF	Noise Figure
PA	Power Amplifier
PAE	Power-Added Efficiency
PCB	Printer Circuit Board

PLL	Phase-Locked Loop
Q	Quality Factor
QFN	Quad Flat No-Lead package
RCS	Radar Cross Section
RF	Radio Frequency
Rx	Receiver
SiGe BiCMOS	Silicon-Germanium Bipolar Complementary Metal-Oxide-Semiconductor
SNR	Signal-to-Noise Ratio
SSB	Single-Sideband
TDM	Time Division Multiplexing
TR2	Double-Receive Channel Transceiver
TRM	Monostatic Transceiver
TRMant	Monostatic Transceiver with integrated antenna
TRx	Transceiver
Tx	Transmitter
VCO	Voltage-Controlled Oscillator

List of Publications

Parts of the thesis have already been published in peer-reviewed journals and conferences:

- **E. Öztürk**, U. Yodprasit, D. Kissinger, W. Winkler and W. Debski, "A Master/Slave 55.5 – 64.8 GHz 4x4 FMCW Radar Transceiver in 130 nm SiGe BiCMOS for Massive MIMO Applications," *in IEEE MTT-S Int. Microw. Symp. Dig.,* pp. 683-686, Jun 2019.
- M. SeyyedEsfahlan, **E. Öztürk**, M. Kaynak, I. Tekin and A. K. Skrivervik, "Two-Element Antenna-Active Phase Shifter Packaging at 77 GHz," *in Proc. 13th Eur. Antennas Propag. Conf. (EuCAP),* pp. 1-4, Apr. 2019.
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