Reliability Study of Stud Bump Bonding Flip Chip Assemblies on Molded Interconnect Devices

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So eine Arbeit wird eigentlich nie fertig,
man muß sie für fertig erklären,
wenn man nach Zeit und Umständen
das mögliche getan hat.

Johann Wolfgang von Goethe
Italienische Reise, 1787

Summary

The Stud Bump Bonding (SBB) flip chip technology on Molded Interconnect Devices (MID) is a highly promising solution to the increasing demand for reliable interconnection technology at high temperatures, a miniaturized assembly and a reduction of costs and parts.

The reliability and potential failure mechanism of the flip chip technology on organic boards, such as FR4, invoking the solder bump technology is widely studied, whereas the failure mechanism and therefore the criteria to optimize a SBB flip chip interconnection on MID was still largely unknown.

Carrying out thermal cycling, this work shows for the first time that the SBB flip chip technology used in combination with Printed Wiring Boards based on the MID technology is a highly reliable packaging technology. Using requirements set by the automotive industry, such as exposing the assembled flip chip interconnections to thermal cycles between 150 °C and -40 °C, no single electrical failure is detected; it was tested until 3000 thermal cycles.

In order to consider a greater technology variety, two different kinds of SBB flip chip technologies were studied: isotropic conductive adhesive (ICA) in combination with capillary underfill (UF), as well as no-flow underfill such as non-conductive adhesive (NCA). Moreover, for both technologies, two different underfill respectively NCA materials were used, which further support the analysis. Additionally, two different chip sizes and board thicknesses were used. The influence of oxygen plasma treatment of the surface of the LCP board was investigated, which strongly influences the wetting angle between substrate and underfill.

This work proves that in thermal cycling of this kind of packaging technology, two failure mechanisms are dominant. A systematic and detailed investigation of potential failure mechanism by means of a complete literature study followed by Finite Element (FE) Analysis of the interconnection were performed. Two potential failure mechanisms were initially theoretically proposed: bulk fillet cracking and delamination between board and underfill. Then, experimental reliability analysis of the SBB flip chip technology on MID boards was carried out and univocally verified the theoretically proposed failure mechanisms, proving that the failure mechanisms can occur simultaneously. Failure originating from the bump area was not detected.

For investigating the delamination risk, a highly innovative enhancement, suitable for industrial use, of the button-shear-test for measuring the interfacial toughness of an underfill/substrate interface was developed. Since adhesion depends strongly on the ratio between shearing and tension loading of the interface, it is necessary to measure the toughness at different phase angles. With the enhanced button-shear-test, which is based on correlation of FE analysis and experimental testing, the phase angle can be widely varied using a single test specimen and different shearing heights. The obtained dependence conforms with values from

the literature, which are mostly obtained from cumbersome testing on various test setups. The failure for the tested structure appeared in the upper layer of the thermoplastic board material LCP. Therefore, plasma treatment of the LCP did not show great improvement of the adhesion.

The proposed failure mechanisms were used to create a guideline to optimize SBB flip chip interconnections. The general conclusion can be drawn that the two failure mechanisms were strongly influenced by local parameters. Parameters which influence the global behavior of the flip chip interconnection such as the chip size and the thickness of the board show negligible influences on the failure mechanisms. A higher impact was observed via the CTE value and Young's modulus of the adhesive. The lower the CTE value and Young's modulus, the lower the risk of bulk fillet cracking. An increase of the adhesive CTE value by 25 %, as well as the wetting angle between underfill and substrate, increase the risk of delamination by almost 75 %.

Comparing the impact of the used adhesives on the risk of fillet cracking and delamination, the unfilled adhesive NCA1 shows the highest risk for both failure mechanisms. This is due to the higher CTE value of NCA1 compared to the other utilized adhesives. Even more, the measured critical stress intensity factor K_{Ic} for that adhesive is much lower. Since the fillet formation is different for every adhesive, and the formation shows a very high impact on fillet cracking, the impact of the adhesive properties can not be experimentally verified using flip chip assemblies.

Based on the results of the present work, optimization of SBB flip chip interconnections on MID boards is based on the present work already possible in the design phase. There are only two failure mechanisms for this kind of interconnection technology when exposed to thermal cycling. Failure at the bump is not a failure mechanism for the studied packaging technology. The proposed guidelines support the selection of the appropriate underfill, board material and geometry such as thickness and chip size. Additionally, the results of this work clearly indicate the use of oxygen plasma treatment on the LCP board prior to flip chip assembly.

Zusammenfassung

Die Stud Bump Bonding (SBB) Flip-Chip Technologie auf MID Substraten ist eine vielversprechende Lösung für die wachsende Nachfrage nach zuverlässigen Aufbau- und Verbindungstechnologien bei gleichzeitiger Miniaturisierung und Reduktion von Kosten und Komponenten.

Potentielle Fehlermechanismen und deren Einflüsse auf die Zuverlässigkeit von gelöteten Flip-Chip Verbindungen auf organischen Substraten wurden bereits in zahlreichen Studien untersucht. Hingegen waren im Vorfeld dieser Arbeit die Fehlermechanismen sowie die Einflussfaktoren auf die Zuverlässigkeit von SBB Flip-Chip Verbindungen auf thermoplastischen MID Substraten weitgehenst noch unbekannt.

Diese Arbeit zeigt, dass die SBB Flip-Chip Technologie in Kombination mit der MID Substrat-Technologie eine höchst zuverlässige Aufbau- und Verbindungstechnik (AVT) darstellt. Basierend auf Automotive Anforderungen konnte gezeigt werden, dass diese AVT Technologie Temperaturwechsel-Lagerungen zwischen 150 °C und -40 °C ohne jegliche elektrische Ausfälle widersteht. Die Untersuchungen wurden bis 3000 Zyklen durchgeführt.

Es kamen zwei unterschiedliche SBB Technologien zum Einsatz. Zum einen wurde ein isotrop leitfähiger Klebstoff (ICA) zusammen mit einem Underfiller (UF) verwendet um eine elektrische und mechanische Verbindung zwischen Silizium-Chip und MID Substrat aufzubauen. Zum anderen wurde die SBB Flip-Chip Technologie mit einem nicht elektrisch leitfähigen Klebstoff (NCA) zum Verbindungsaufbau zwischen Chip und Substrat verwendet. Für beide Technologien wurden jeweils zwei Underfiller bzw. zwei NCAs untersucht. Um experimentell noch weitere Einflussparameter auf die Zuverlässigkeit beurteilen zu können, wurden zusätzlich zwei unterschiedliche Chipgrößen und Substratdicken zur Herstellung der SBB Flip-Chip Verbindungen eingesetzt. Darüber hinaus wurde der Einfluss der Oberflächenbehandlung mit Sauerstoffplasma untersucht welche den Benetzungswinkel und Meniskusform stark beeinflusst.

Eine systematische und detaillierte Zusammenstellung von potentiellen Ausfallmechanismen für SBB Flip-Chip Anwendungen basierend auf einer Literaturübersicht wurde durchgeführt. Es konnten zwei potentielle Fehlermechanismen identifiziert werden. Eine Finite Elemente Analyse der Spannungen und Dehnungen im Klebstoff-Meniskus unterstützt diese Zusammenstellung weiter. Zum einen ist dies eine Rissentstehung im oberen Teil des Meniskus. Zum anderen wird eine Delamination-Entstehung zwischen dem Substrat und der Unterfüllung bzw. Klebstoff als Ausfall vorhergesagt.

In den Zuverlässigkeitsuntersuchungen konnten die beiden theoretisch vorhergesagten Ausfallmechanismen bei SBB Verbindungen experimentell nachgewiesen werden. Es konnte gezeigt werden, dass die beiden Mechanismen auch gleichzeitig auftreten können. Eine Aus-

fallinitiierung bzw. Versagen in der Nähe der Stud Bumps wurde, wie theoretisch ebenfalls vorhergesagt, nicht detektiert.

Der standardisierte Haftkegel-Test wird verwendet um einfach und kostengünstig die Haftung zwischen unterschiedlichen Substraten zu bestimmen. In dieser Arbeit wurde dieser Test erweitert um das Delaminationsrisiko zwischen dem MID Substrat und den Klebstoffen zu charakterisieren. Die Adhäsion hängt stark von dem Verhältnis aus Scher- und Zugspannung im Bereich einer Delamination ab, dem so genannten Phasenwinkel. Daher ist es entscheidend, die Haftfestigkeit bei unterschiedlichen Phasenwinkeln zu bestimmen. Mit Hilfe des in dieser Arbeit erweiterten Haftkegeltests kann eine weite Variation des Phasenwinkels mit nur einem einzigen Testaufbau realisiert werden. Hierbei wird eine Korrelation zwischen Finite-Elemente Analyse und experimentellen Schertests bei unterschiedlichen Scherhöhen verwendet. Die Abhängigkeit der Haftfestigkeit von dem Phasenwinkel ist im Einklang mit Arbeiten aus aufwendigen Tests an unterschiedlichsten Probengeometrien. Das Versagen bei der Untersuchung der Haftfestigkeit trat in der obersten, äußerst dünnen Spritzgusshaut des LCPs ein. Daher konnte mit der untersuchten Oberflächenbehandlung mit Sauerstoff-Plasma kaum eine Haftfestigkeitssteigerung erreicht werden.

Die theoretisch vorhergesagten Ausfallmechanismen dienten als Basis um einen Auslegungs-Leitfaden für die Optimierung von SBB Flip-Chip Verbindungen auf MID Substraten zu erstellen. Grundsätzlich kann ausgesagt werden, dass die beiden Ausfallmechanismen sehr stark von lokalen Geometrien und Materialeigenschaften in der Umgebung der kritischen Bereiche abhängen. Größen, die das globale Verhalten der Verbindung beeinflussen, haben einen zu vernachlässigen Einfluss auf die Ausfallmechanismen. Dies sind die Chipgröße, die Substratdicke sowie die Substrateigenschaften.

Eine große Auswirkung auf die betrachteten Vergleichsgrößen haben der thermische Ausdehnungskoeffizient (CTE) und das E-Modul des Klebstoffs. Je niedriger der Ausdehnungskoeffizient und das E-Modul, desto geringer ist das Risiko einer Rissentstehung im oberen Teil des Meniskus. Eine Erhöhung des CTE-Werts um 25% erhöht das Risiko eines Ausfalls um fast das Dreifache. Ebenso kann das Delaminationsrisiko zwischen Klebstoff und Substrat reduziert werden, wenn der Benetzungswinkel so klein wie möglich gehalten wird. Eine Erhöhung des Winkels um 25 % zieht eine Erhöhung des Delaminationsrisikos um mehr als 75 % nach sich.

Vergleicht man den Einfluss der eingesetzten Klebstoffe auf das Risiko für eine Riss-Initiierung im Underfill Meniskus und Delamination, zeigt NCA1 zeigt das höchste Risiko hinsichtlich beider Ausfallmechanismen. Dies kann auf den höheren Ausdehnungskoeffizienten des NCA1 im Vergleich zu den anderen eingesetzten Klebstoffen zurückgeführt werden. Darüber hinaus zeigt NCA1 auch den niedrigsten kritischen Spannungsintensitätsfaktor K_{Ic} der verwendeten Klebstoffe. Da jedoch die Meniskusausbildung sehr stark vom eingeset-

zten Klebstoff abhängt, und die Meniskusausbildung einen sehr großen Einfluss auf die untersuchten Ausfallmechanismen besitzt, kann der Einfluss der Material-Eigenschaften des Klebstoffes nicht anhand der Ergebnisse der Zuverlässigkeitsuntersuchungen der Flip Chip-Verbindungen experimentell verifiziert werden.

Mit Hilfe der Ergebnisse der hier vorliegenden Arbeit kann eine Optimierung und daher Zuverlässigkeitssteigerung einer SBB Flip-Chip Verbindung auf MID Substraten bereits in der Auslegungsphase durchgeführt werden. Der Leitfaden hilft bei der Auswahl der geeigneten Klebstoffe, Substratmaterialien und Geometriegrößen wie Substratdicke und Chipgröße. Als Ergebnis dieser Arbeit ist zudem festzuhalten, dass die Oberflächenbehandlung mit Sauerstoffplasma einen unabdingbaren Prozessschritt darstellt um die Zuverlässigkeit von SBB Flip-Chip Verbindungen auf MID Substraten zu erhöhen.

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Contents

Part I

Introduction

Chapter 1

Introduction

The Moore´s law has been the proven dictum in semiconductor development for many years now and this will continue to be for the foreseeable future. However, the progress in the semiconductor industry alone will not be able to meet the performance, functionality, miniaturization and cost efficiency requirements of today's microelectronic systems [90]. The packaging technology plays a key role to meet the required miniaturization, increased functionality and reducing costs [89]. In order to achieve these goals, new technologies and materials have to be developed. *Reichl et al.* adds that a rapid market introduction of such new concepts is to be achieved by using state-of-the-art technologies and existing infrastructure, as well as the integration of latest technologies [90].

This is especially true for the development of new packaging concepts for automotive applications, while a rapid introduction of new technologies is important in order to guarantee market leadership, the combination of state-of-the-art technologies with the latest invention reduces the risk when introducing new concepts. One example of such an automotive application is a rotational sensor, Fig. 1.1, which combines the widely-used flip chip technology with the latest substrate technology Molded Interconnect Devices (MID).

MID is capable of realization of new functions which the planar Printed Circuit Board (PCB) technology cannot yet fulfill [17]. The MID technology allows the combination of conductor parts and the housing into a single piece. Thus, it is possible to use three-dimensional injected molded thermoplastic parts as conductor paths, a screening layer and an antenna function. Moreover, the MID parts can be utilized as a carrier for electronic components, as well as for the integration of mechanical elements.

Besides the challenges of the manufacturing and assembly processes, the identification of the failure mechanisms and reliability affecting parameters play a key role in the acceptance of a new packaging concept, particulary for automotive applications.

(a) MID substrate

(b) Flip chip assembled

Fig. 1.1: Example of a sensor for automotive application; using the MID technology as a three dimensional PCB and the flip chip technology to interconnect the chip with the PCB [8, 40]

The packaging concept Stud Bump Bonding (SBB) flip chip on MID is already used for consumer products such as hearing aids [106, 129] and lens holders for cameras [39]. The reliability studies are limited to prove feasibility, rather than identification of failure mechanisms and understanding the impact of certain parameters on reliability. Until now, the packaging technology has not found an entry in automotive applications, particularly because of the exposure occurring to these applications such as thermal cycling and humidity storage.

Failure mechanisms can, among others, be distinguished in overstress and wearout failure mechanisms [114]. Overstress failure mechanisms are defined as an exceeding of the strength or capacity of a component or material within a single event. On the other hand, wearout failure mechanisms take place, when a component is loaded at a much lower level but continuously. Failure mechanisms are fatigue damage, creep, wear, stress-driven voiding and interfacial delamination, etc. Fatigue mechanisms are either fully or partially responsible for 90 % of all structural and electrical failure [114]. In order to ensure that electronic components do not fail by these wearout mechanisms within their required lifetime, different standardized test conditions are set up. For electronic components and systems for Automotive applications, the Automotive Electronics Counsils (AEC) defined qualification tests which are shown in Tab. 1.1. These qualification tests are similar to the MIL standards [1, 2, 3, 124].

Flip chip interconnections are widely studied under the testing conditions listed in Tab. 1.1. Among these conditions, the temperature cycling and humidity biasing are considered to be the tests which are most challenging. In this work, the focus lies on the thermal cycling of SBB flip chip interconnection on LCP substrates. Compared to standard PCB material, like FR4, the substrate material LCP has a different Young's modulus and Coefficient of thermal expansion. This leads primarily to a different CTE mismatches between chip and substrate compared to flip chip interconnections with FR4. Therefore, the focus lies on the reliability performance when exposed to thermal cycling. Moreover, LCP shows a very low humidity

Tab. 1.1: Stress test qualification according to AEC Q100 in order to approve a principal suitability of devices; Electrical, environmental, and mechanical tests similar to MIL STD750, MIL STD202, etc. [1, 2, 3, 124]

Test	**Conditions**	**Failure allowed**
Temperature Storage	1000 hours at $T_{\max}$	0 from 77 ... 120
Temperature Humidity Bias	1000 hours 85 °C / 85 % RH $V_{\max}$	0 from 120 ... 231
Temperature Cycling	1000 cycles -40 °C to $T_{\max}$	0 from 120
Power Temperature Cycling	-40 °C to 125 °C for 1000 cycles	0 from 231
Vibration	4 minutes at 40 g and 20 Hz to 2000 Hz	0 from 231

absorption in contrast to FR4 or PCB made of flex materials [1].

The scope of the present work is in the identification of the failure mechanisms of the SBB flip chip interconnection on MID boards. Two different kinds of SBB flip chip technologies are used: the ICA (isotropic-conductive adhesive, plus capillary underfill) and NCA (non-conductive adhesive) technology. The Laser-Direct-Structuring (LDS) is utilized as MID technology. The assembled interconnections are tested under automotive thermal cycling conditions (+150 °C/-40 °C). In order to extend the lifetime of the SBB flip chip interconnections on MID boards, the failure mechanisms are used to create a design guideline. The guideline contains the influence of the chip size, board thickness and surface treatment, utilized SBB technology, as well as the fillet shape.

[1] FR4 has an absorption of humidity of about 0.9 % [77], where LCP shows an absorption between 0.005 and 0.03% [110]

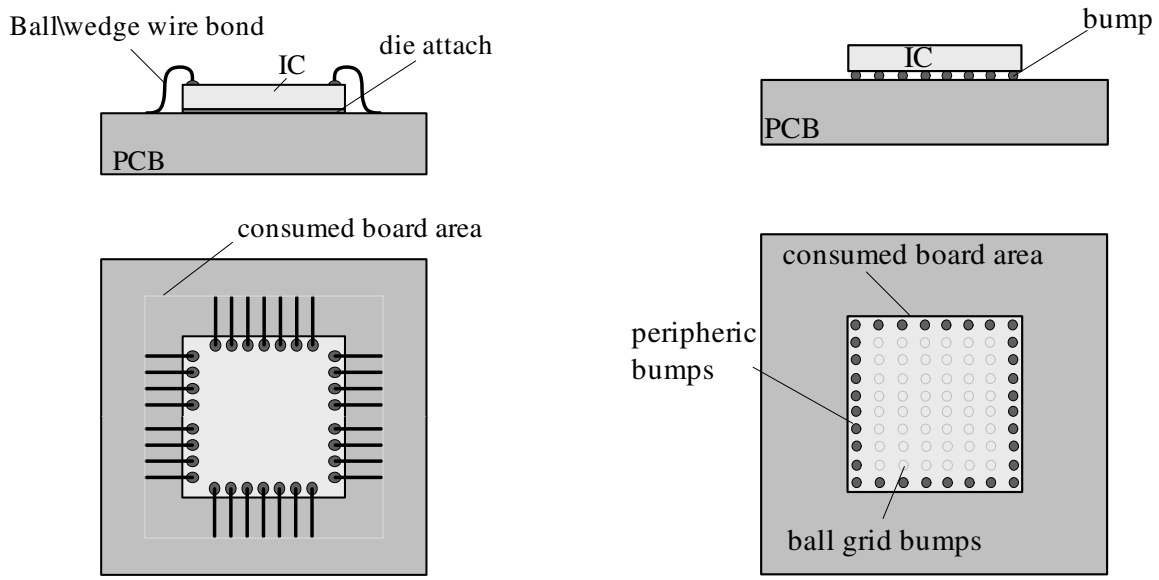
Chapter 2

Technological Description of SBB Process and MID

A Stud Bump Bonding (SBB) flip chip interconnection belongs to the class of chip scale packages (CSP). A CSP is defined as an IC package which occupies a footprint area of no more than 50 % greater than the area of the chip it packages [114]. Several varieties of CSP designs are in use today. The main types of CSP are the wirebonding and the flip chip technology, either on flexible or rigid PCB boards [43, 78, 81, 114]. The two technologies are displayed in Fig. 2.1.

In wirebonding, the chip is mounted face up and it's rear surface is directly bonded to the substrate. The interconnection consumes the chip area plus the area needed for the wirebonds. On the contrary, the flip chip assembly requires the lowest footprint area on the substrate and allows additional significant reduction in package height [81]. The mechanical and electrical connections between IC and substrates are established by bumps, mainly made of metals. The flip chip process was first introduced for ceramic substrates by IBM in 1962 as the so-called C4 technology - Controlled Collapse Chip Connection [114].

The flip chip technology can basically be categorized into two different kinds: flip chip assemblies using solder bump technology and flip chip assemblies using adhesives, conductive or non-conductive [80]. For solder bumped flip chip interconnections, the bumps are deposited on solder wettable metal terminals on the active surface of the IC. The pads on the IC matches wettable pads on the PCB [114]. The solder bumps are aligned to the PCB and then reflowed at high temperatures to form simultaneously electrical and mechanical connections. The advantages of the solder bump flip chip technology definitely lies in the high ampacity and the parallel formation of the bumps and the inexpensive bump material. The high reflow temperatures, especially when it comes to leadfree solder materials, play a limiting factor concerning the use of polymer-based PCB material. Moreover, the necessity



(a) Wire bonded chip interconnection

(b) Flip chip interconnection

Fig. 2.1: Overview of the chip scale packages (CSP) wire bonding and flip chip technology; (a): Chip placement on the board using die attach material (solder, adhesives) to establish mechanical and thermal connection; wire bonds using ball/wedge bonding for electrical interconnection; (b): balls made of solder, by gold stud bumping or electroless procedures are used to give mechanical, electrical and thermal connection between IC and substrate; the wire bond assembly consumes board area of the size of the die plus the wire bond loops, whereas the flip chip interconnection does not need more area than the chip itself; comparing the number of I/Os, the flip chip technology is capable of having bumps not only located peripherally along the chip edges but distributed over the whole chip [43, 81, 112, 114]

of applying flux during assembly process limits the reliability of solder joint flip chip interconnections. The flux is used to clean the pads, prevent re-oxidation and increase the heat flow during solder process [32]. The failure mechanisms of solder bumped flip chips assembly and their relevance for SBB flip chip interconnections are discussed below. Alternatively, flip chip assemblies using adhesive bonding are available. The bumps on the pads of the IC are formed mainly by electroplating, electroless plating, or manufacturing of gold stud bumps by using a modified wire bonder [81]. After bump formation, the connection between the IC and the substrate is established using conductive or non-conductive adhesives. The adhesives are cured at elevated temperatures. The main advantages of this kind of flip chip technology are the lower process temperatures during flip chip assembly, as well as that no flux is needed.

In the present work, the Stud Bumping technology is invoked to form the bumps on the aluminum pads on the IC. It is similar to the ball/wedge wire bonding process. But after creating the ball and placing it on the chip pad, the wire is broken off [81]. This controlled breaking off above the heel is forced by doping the gold wire with 1 to 2 percent palladium [66]. The process is sketched in Fig. 2.2.

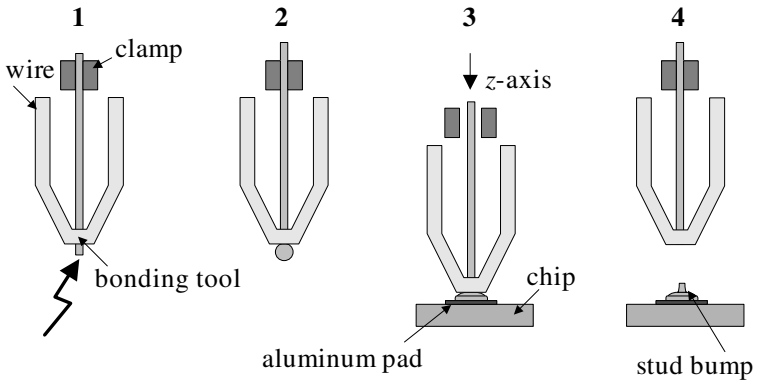


Fig. 2.2: Schematic flowchart of gold stud bumping; in the first step: (1) Passing the gold wire through the capillary tube like for conventional wire bonding process, (2) formation of a ball by applying an electrical discharge, (3) placing the ball on the die pad and building up an interconnection of ball and pad by thermocompression and ultrasonic energy, (4) the capillary tube clamping the wire is withdrawn and the wire is cut [39, 66, 81, 112, 129].

Modern wire bonders are capable of placing up to fifteen bumps per second [66, 129].

The flip chip technology Stud Bump Bonding (SBB) Process is a relatively rarely used technology compared to solder bump flip chip technology. Nevertheless, consumer applications such as hearing aids [106, 129], lens holders for cameras and ASIC packaging on flexible printed wiring board [39] are already realized using the SBB process.

There are different kinds of SBB flip chip technologies. The main difference between the methods lays in the way the chip and the substrate are electrically connected [33, 66]. In that study, two methods are used: (1) Using an isotropic-conductive adhesive (ICA) for the electrical connection, together with a capillary underfill (UF) which establishes a stable mechanical connection; (2) the electrical connection of the chip and the substrate is realized via a direct contact of the stud bump to the metallization of the substrate; through its cure shrinkage, a non-conductive adhesive (NCA) secures constant mechanical and therefore electrical contact between the bump and the substrate [127].

The process flow of the ICA SBB technology is displayed in Fig. 2.4.

The Stud Bump Bonding Process, which utilizes a non-conductive adhesive, requires less process steps than the ICA SBB process, Fig. 2.3.

The process steps can also be combined or performed in a slightly different sequence. The advantages of the SBB process compared to solder flip chip technology are [66, 91]

- the SBB process is suitable for MEMS and ICs without passivation on the electrical structures

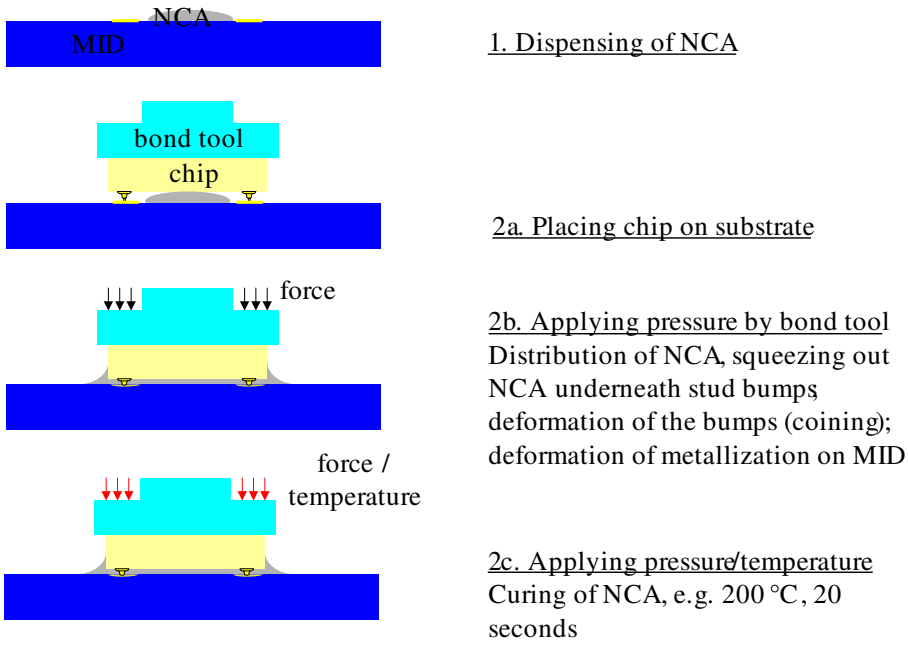


Fig. 2.3: Process Flow: Stud Bump Bonding (SBB) Process using non conductive adhesive (NCA) [66, 87, 127]

- Bumping can be performed on the already diced chip, which makes it especially interesting for small volume applications or prototypes
- It is based on the well-controlled thermosonic wire bonding
- It has the following advantages over the solder bump technology
  - no use of lead based materials as well as flux
  - lower curing temperatures of the isotropic-conductive adhesive and underfills; very short curing time for the NCA SBB technology
  - higher resistance concerning high temperature storage

where the disadvantages are

- Concerning the ICA technology, the handling of the adhesive bonded but yet not underfilled chips can be critical due to the low adhesive bonding of the bumps and the pad on the IC
- Risk of short circuits caused by broken wire tails during coining process
- Stud Bumping is a sequential process which is therefore not cost efficient for high I/O counts.

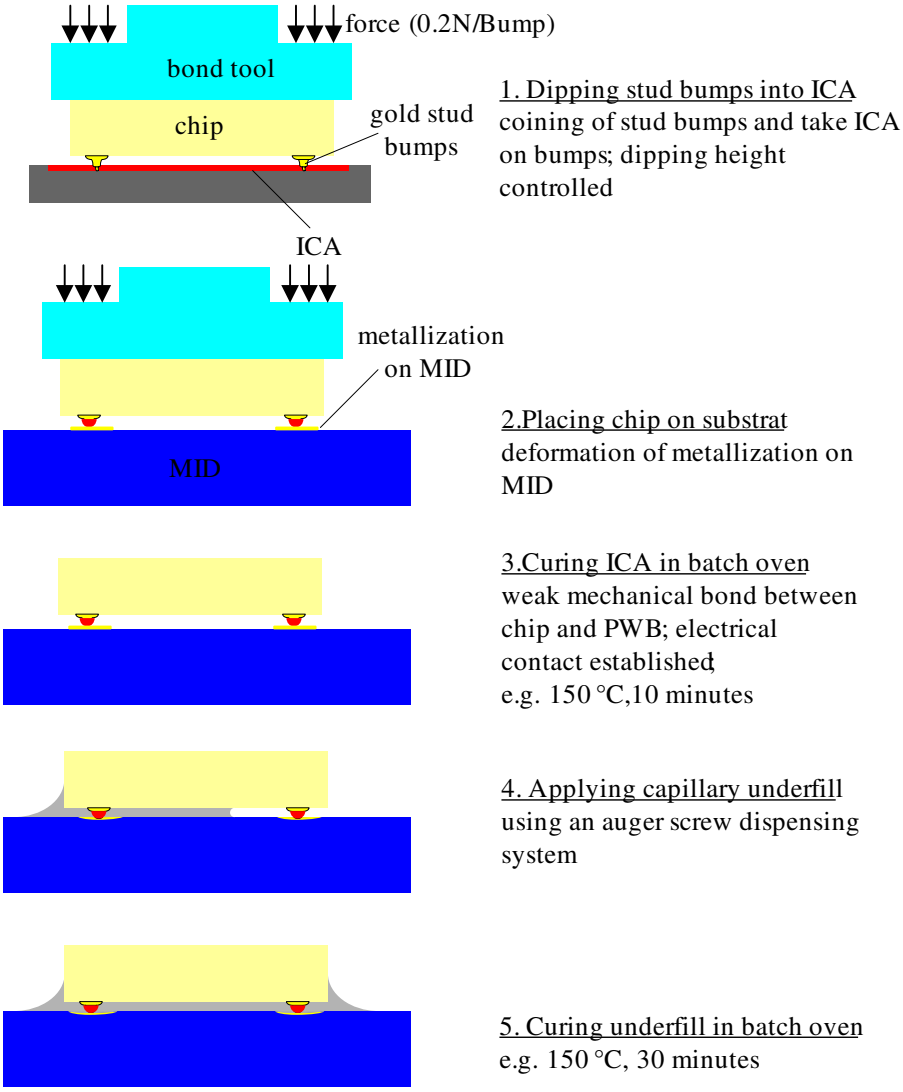


Fig. 2.4: Process Flow: Stud Bump Bonding (SBB) Process using isotropic conductive adhesive (ICA) together with capillary underfill (UF) [66, 87]

As already mentioned, comparing the manufacturing time of the bumps on the silicon wafer, the solder ball technology shows a significant advantages in contrast to the Stud Bump technology when it comes to high I/O counts. An example of a commercial solder bumping process for deposition on evaporation and plating can be found in [77, 79, 114]. The process can consist of about seven steps on the wafer level: (1) Evaporation of Under Bump Metallization (UBM) and the solder dam, (2) pattern plating and template resist, (3) etching of solder dam, (4) electroplating of the solder, (5) stripping of the photoresist, (6) reflow process to build solder balls and finally (7) etching of the solder dam and UBM. The masks created, especially for a certain chip design, can be used several times for deposition and edging. Performing also the bump creation on the wafer level by the Stud bump technology, the needed time is much higher for high I/O counts. Nevertheless, the creation of the mask is not needed for the Stud bumping process.

The assembly of solder ball flip chips consists of dipping of the diced chips with the solder balls in a flux film to transfer flux to the balls. The flux is needed to clean the balls and pads on the substrate from oxides and contaminations. After placing the chip on the substrate, the solder balls are again melted in the reflow process to produce a mechanical and electrical contact between the chip and the substrate through the balls. These steps are performed sequentially for each flip chip and therefore quite similar to the SBB ICA assembly process. The following underfill process is for both technologies, solder ball and SBB ICA flip chip technology, the same, Fig. 2.4.

The Stud Bump Bonding flip chip technology obeying the NCA process reduces the number of process step significantly since only the placing of the chip and curing of the NCA is required, Fig. 2.3. The curing has to be performed directly in the chip placer, which lowers the throughput of the chip placer compared to the solder bump and SBB ICA technology where the melting or curing are performed in a reflow or batch oven, respectively.

The idea of creating electric interconnections based on thermoplastic materials, produced by injection molding, goes back to the 1960s [18]. The MID technology has the advantage through combining electrical and mechanical functionality. The biggest advantage of the MID technology lies in the realization of three dimensional conductor paths whereas boards based on ceramic or fiber reinforced thermoset materials (e.g. FR4) are mainly limited to two dimensions. An overview of the different MID-technologies can be found in [18, 20, 36, 41, 74]. In the presented work, the MID substrates are fabricated using the Laser Direct Structuring (LDS) technology [50, 61, 62, 97]. The process steps are shown in Fig. 2.5.

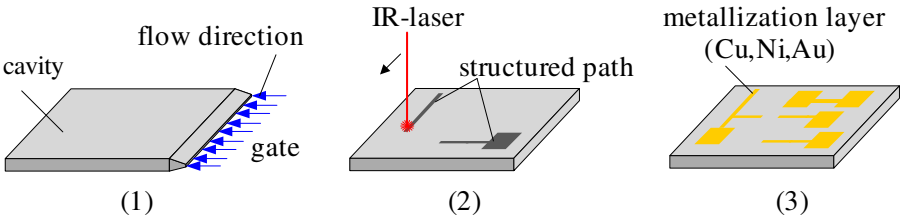


Fig. 2.5: Process flow of LPKF-Direct Laser Structuring (LDS) of a thermoplastic substrate [50, 61, 62]; (1) injection molding of a Liquid Crystal Polymer (LCP); it is modified to be capable of laser activation; the gate is designed as a film gate; (2) LPKF laser structuring of the LCP by an IR laser; (3) deposition of Cu,Ni,Au-layers by chemical deposition

Part II

Theoretical Assessments, Models and Assemblies

Chapter 3

Identification of Potential Failure Mechanism of SBB Flip Chip Interconnections

The SBB process is, in comparison to solder bumped flip chip interconnections, a rarely studied technology. The published studies concentrate on the feasibility of the assembly process. No reports are available concerning reliability for SBB flip chip interconnections. As mentioned, the solder bumped flip chip interconnections are the focus of many studies. Therefore, the concepts and failure mechanism used to study the reliability of solder bumped flip chip interconnections with relevance for SBB assemblies are shown and discussed.

Many mechanical and thermo-mechanical systems are described by simple analytical models. Many attempts to cover the behavior of a flip chip interconnection by a simplified system can be found in literature. Flip chip interconnections are simplified by tri- or bi-material-layered system where the fillet and the bumps are neglected: for two-layered systems in [93, 103, 128] and for three-layered systems by [9, 104, 121].

The thermo-mechanical behavior is described by differential equations based on the theory of elasticity. The equations are solved by applying boundary condition, as well as transition conditions between the two or three layers [120]. The solutions are the tensile σ_{yy} and peel stress τ_{xy} between the layers as function of the coordinate x. Additionally, the warpage $\delta(x)$ can be determined.

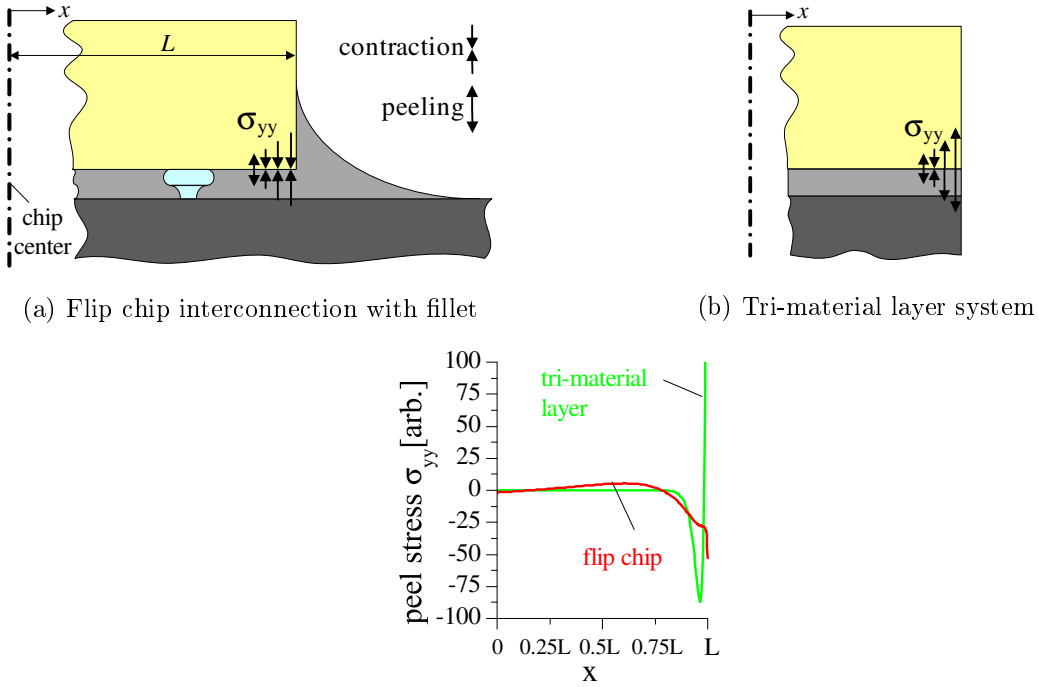
The advantage of the analytical solutions lies in the simple representation of dependencies of the stresses and warpage on the load and material properties [93, 103]

$$\sigma_{yy}, \tau_{xy} \quad \sim \quad \Delta\alpha\Delta T, E \tag{3.1}$$

$$\delta \quad \sim \quad \Delta\alpha\Delta T, \frac{1}{E}. \tag{3.2}$$

The warpage δ increases with the distance x from the center and reaches its maximum at $x = L$. The shear stresses τ_{xy} between the layers are zero at $x = L$. This is due to the fact that no lateral forces are present at that position [103]. The peeling stress σ_{yy} decays rapidly when x approaches the center of the composite $x \to 0$.

Fig. 3.1 reveals that an approximation of a flip chip interconnection by a tri-material layer does not correctly represent the stresses at $x = L$. Parameters and geometries which mostly act locally cannot be represented by these solutions.



(a) Flip chip interconnection with fillet

(b) Tri-material layer system

(c) Peel stresses

Fig. 3.1: Comparison of tensile stresses in the interface of a flip chip interconnection and a tri-material layer; (a) due to the fillet, the interface chip/underfill experiences a contraction for $x \to L$; (b) for a tri-material layer, due to the singularity at $x = L$, the tensile stresses are showing a peeling character; analytical solutions are available [9, 104, 120, 121, 128]; (c) it reveals that a tri-material layer approximation of a flip chip interconnections is not capable of displaying the stresses correctly

Therefore, the analytical representation cannot be used to study the reliability of a flip chip interconnection. The Finite Element Analysis can overcome that problem. Therefore, the interconnection is studied using Finite Element Analysis because it is capable of truly representing the geometry of the interconnection, as well as accounting for complex material behavior as visco-elasticity and plasticity.

In order to study the reliability of the flip chip interconnection, it is essential to know the mechanisms which lead to failure. This approach is generally known as the physics-of-failure approach and has been used for many years now. Physics of failure analysis is a term for identifying and understanding the physical processes and mechanisms of failure. It led to

improvements concerning the reliability of systems, even as the complexity of the systems increased. Due to more powerful computers, numerical simulations of the failure mechanisms which are mainly based on physical and chemical principles are used more and more. The feasibility of computer-based physics-of-failure analysis grew even more due to the availability of complex material models. Using computer-based physics-of-failure, it is even possible to combine different failure mechanisms in the reliability study [115].

The flip chip technology is a widely-studied application in which the physics-of-failure approach is applied. Fig. 3.2 gives an overview of the reported failure locations and mechanisms. The failure mechanism are mainly detected for solder bumped flip chip interconnections. The reported mechanisms are now described and their applicability to stud bump bonding flip chip interconnections discussed.

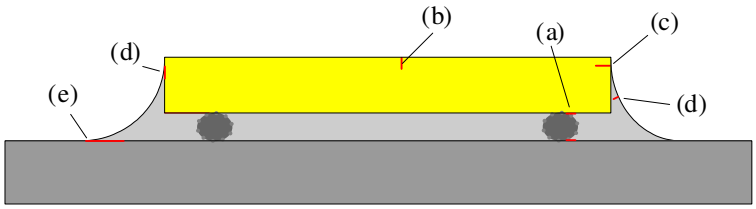


Fig. 3.2: Reported location of failure of solder bumped flip chip interconnections: (a) solder fatigue followed by delamination of passivation and underfill or visversa; (b) horizontal chip cracking [116]; (c) vertical chip cracking [30, 58, 59]; (d) bulk and interfacial cracking in the upper part of the fillet [6, 23, 63, 64]; (e) interfacial cracking between underfill and substrate [5, 27, 46, 64, 70, 71, 73, 108]

The lifetime of solder bumped flip chip interconnections is limited by the solder fatigue of the bumps when exposed to thermal cycling storage. Cyclical plastic deformation change the structure, weaken the solder and can lead to fatigue. A frequently relation to estimate the number of cycles until fatigue fracture occurs is based on the Coffin-Manson relation

$$N_\mathrm{f} = C\,\varepsilon_\mathrm{creep}^{-n}, \tag{3.3}$$

with the creep strain per cycle $\varepsilon_\mathrm{creep}$ [45, 77, 114, 125]. C and n are material constants. An important technology to dramatically increase the fatigue lifetime is to underfill the chip. The filled epoxy encapsulant matches the CTE of the bumps, minimizes the stresses on the solder joints and increases the fatigue life [82]. It could be shown that significant improvements in fatigue life can be achieved [21]. Depending on the size of the flip chip and bump, the use of underfills yields an increase of lifetime by 8 up to 80 times compared to flip chip interconnections without underfill. However, restraining the movement of the chip relative to the substrate can produce a significant shear stress as well as tensile stress of the underfill layer giving rise to a new failure mode: underfill delamination and rupture. Especially in presence of flux contamination originating from the assembly process, delamination between the chip passivation and underfill can occur and again reduce the lifetime [25, 45, 83, 84, 85,

125]. The delamination leads to much higher creep strain $\varepsilon_{\text{creep}}$ in the bump and therefore to a shorter lifetime, even with underfill [32]. To summarize, creep strain in the bump made of solder leads to failure in the bump region of solder bumped flip chip interconnections. Using underfill, the creep strain can be significantly reduced. Whereas contamination from the flip chip process may lead to delamination of the bump/underfill respectively underfill/chip and again to higher creep strain in the bump.

In the present work, the gold stud bump technology is used to form the bumps. Therefore, no plastic creep strain is expected to occur in the bump. Since underfill material is used, the stresses and strains in the bump can be decreased compared to flip chip assemblies without underfill [21, 83, 84]. Nevertheless, the stress and strain level within the gold bump depends also on the chosen underfill or NCA. The SBB process does not require the use of flux, therefore, no contamination around the bumps is expected [66]. This supports the assumption that bump failure is not a potential failure mode for SBB flip chip interconnections. Nevertheless, scanning acoustic microscopy (SAM) and the measurement of the electrical resistance are performed during and after reliability testing to experimentally verify the assumption of no risk of bump failure.

Another reported failure mechanism of flip chip interconnections is bulk cracking of the silicon die. For integrated circuits dies, defects are caused by etching, sawing, device processing and handling. Hereby, two different kinds of cracking are reported: in Fig. 3.2b vertical die cracking on the top surface of the chip due to scratches [116]; and in Fig. 3.2c cracking on the vertical chip edge caused by flaws produced by dicing process [30, 58, 59].

For brittle materials, the maximum tensile stress is not a unique material property, because it is dependent on the specimen preparation. A more definite criterion is available in fracture mechanics, where the critical stress σ_c is given as a function of the initial defect [116]. For surface flaws with a size of $2a$, the critical tensile stress is a function of the critical stress intensity factor K_{Ic}

$$\sigma_{\text{c}} = m\frac{K_{\text{Ic}}}{\sqrt{\pi a}} \tag{3.4}$$

where m represents a form factor of the defect which equals $m = 1.2$ for a semi-elliptical shape [59, 116]. The critical stress intensity factor of silicon lies between 0.82 and 1.1 MPa$\sqrt{\text{m}}$ [15, 58, 59, 101, 116].

Vertical chip cracking can be avoided by polishing the flip chip surface. Since the backside of the chips in the present work are polished, and the chip bending is expected to be low [1], vertical die cracking is not a concern but is experimentally monitored. Defect on the vertical edge of the die is mainly caused by the sawing process. In some studies, the die cracking

[1] The chip warpage and therefore the vertical chip cracking is strongly influenced by the CTE-mismatch and the ratio of the inertia of bending of the substrate and chip

is investigated due to possible catastrophical failure already at cool down after underfill process [59]. Other publications concentrate on die cracking due to thermal cycling [58]. For the present work, the flaw size of the flip chips after dicing process are in the range of 1 to 2 μm, Fig. 3.3.

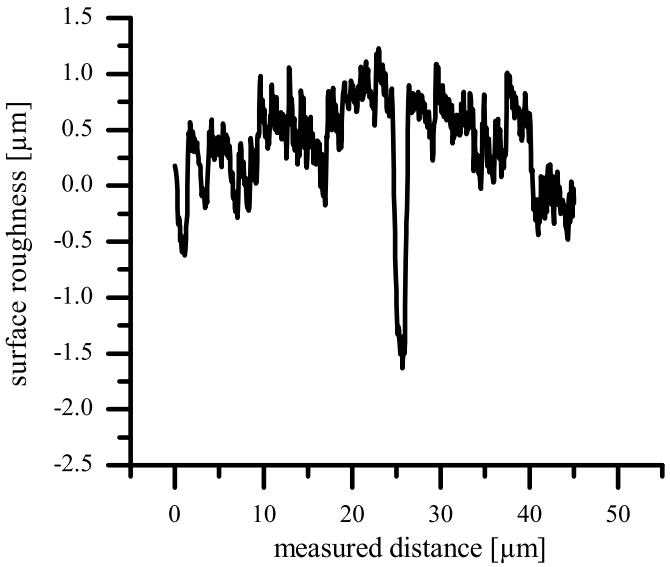


Fig. 3.3: Surface roughness of used flip chip along the sawing edge measured by a profilometer; the maximum flaw size is around 2μm

Using Eq. (3.4), the critical stress equates to 526 MPa. The stress along the vertical chip edge of the flip chip for the studied assemblies lies around 30MPa for cooling down from 150 °C to -40 °C. Therefore, die cracking is not taken into account as failure criteria for the studied SBB flip chip interconnections.

The underfill fillet plays a key role in horizontal chip/underfill delamination. This is due the fact that the fillet converts tensile stresses at the chip edge to compressive stress [6]. Nevertheless, as seen in Fig. 3.1, maximum stresses are present in the fillet. The stresses in the fillet can lead to crack initiation at different locations of the fillet [6, 23, 63, 64]. In [6], the influence of crack initiation and propagation of solder bump flip chip is studied. The focus lies on the experimental observation of fillet cracking due to thermal cycling and moisture. The fillet cracks start in the chip corners and lead to delamination between vertical chip edge and underfill. Consequently, the delamination reaches the lower chip corner and is followed by chip passivation/underfill interfacial cracking. [64, 70] studies additional crack initiation at the chip edges. The fillet is analyzed applying a two dimensional fracture mechanics approach. Despite this, crack initiation starts in the bulk material; additional, [64, 70] models a delamination between the vertical chip edge and the underfill.

Additional to fillet cracking, delamination between the substrate and the underfill at the

lower part of the fillet is reported [5, 27, 46, 64, 70, 71, 73, 108]. The delamination initiation is due to singular stresses in that region. This kind of failure can lead to bump failure once the delamination has reached the bump [70].

It can be assumed that fillet cracking - at vertical chip edge or between substrate and underfill - is independent of the bumping technology used. Therefore, it is considered as a possible failure mechanism for SBB flip chip interconnections.

Cracking in bulk material is caused by fatigue of the material due to cyclic loading, e.g. thermal cycling. Fatigue is described by the domain of micro mechanics or damage mechanics [117, 123]. Once a micro crack extended to a macro crack, the method of fracture mechanics can be applied. Since damage concepts are not well established respectively not very practical to apply on whole structures, the numerical modeling for a more complicated structure like a flip chip interconnection is not well established. Damage models are available for test specimens and RVEs (representative volume element) [13, 29]. However, no damage models are commercially available for interfaces. The concept of fracture mechanics is well studied for bulk and interfacial cracks. Due to the fracture mechanics approach of the crack tip field, the critical values of test specimens can be compared with more complicated structures. Widely-used test specimen for obtained critical bulk properties are the CT-test (Mode-I) and CTS-probe (mixture of Mode-I,-II). Investigations in using smaller test specimens are performed [117]. For interfacial cracking, several different types of test specimens are available. Therefore, the fracture mechanics approach is used to study the SBB flip chip interconnection.

Crack propagation can be distinguished in subcritical and critical crack propagation. Fig. 3.4 shows the crack propagation per cycle as function of the stress intensity factor.

The stress intensity factor K is a quantity used in fracture mechanics and related to the stress at the crack. Cyclic loading is assumed as well as pure tensile loading. The crack propagation depends on the existing stress intensity factor. In region I, the applied load is below a threshold value $K_{\mathrm{th.}}$, where no crack propagation is detected. Increasing the load, the crack propagation speed is linear proportional to the applied load. Increasing the load further, the crack propagation is instable followed by a complete failure. This value of the stress intensity factor is defined as the fracture toughness K_{c} of the material. For most engineering problems, crack propagation occurs in region II. This also applies for the studied flip chip interconnections, where thermal cycling leads to failure after a certain number of cycles.

Characterization of bulk material in region II is time-consuming and involves extensive testing. Moreover, only few publications exist in which the constant crack propagation due to thermal loading is studied. The focus of the present work lies in developing a method, which allows a quick design of and material choice for SBB flip chip interconnections. Therefore,

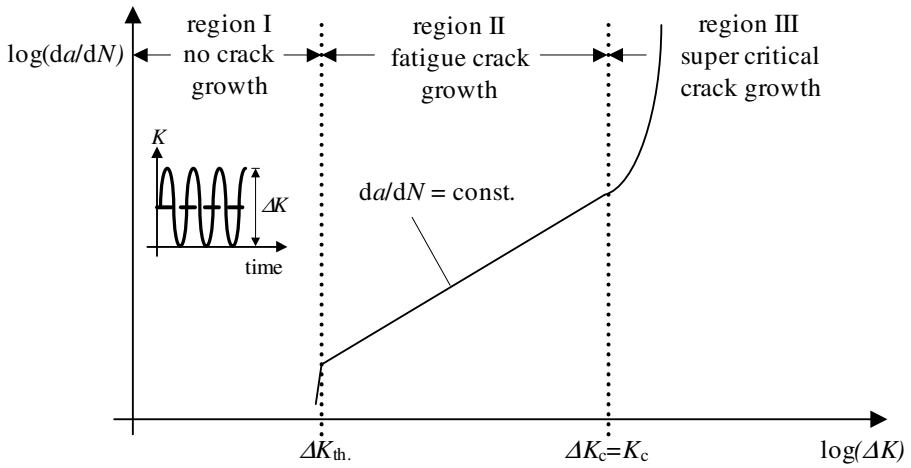


Fig. 3.4: The crack growth rate $\log(\mathrm{d}a/\mathrm{d}N)$ depends on the applied external load; the higher the load, the faster the crack propagation; the different crack growth regions depend on the applied stress intensity factor ΔK; in region I, no crack propagation can detected due to the fact that the external load is too small; where as at region II and III crack propagation occurs; in region II, crack growth occurs, the crack propagation rate is linear dependent on the external load ΔK; supercritical crack characterizes region III, the crack propagates with a high velocity

the underfills and NCAs used are characterized by their mechanical properties, as well as by their fracture toughness K_c. For cracking of substrate/underfill interface, no test is available which is fast and has small consumption of material. Therefore, a method has to be developed which includes these requirements.

Chapter 4

Theory of Bulk and Interfacial Fracture Mechanics

4.1 Linear Elastic Fracture Mechanics (LEFM)

The fracture mechanics approach is used to describe the proposed failure mechanism - bulk cracking in the fillet as well as interfacial cracking between the substrate and the underfill.

Cyclic loading causes fatigue cracking in bulk material. Fatigue is described by methods like micro or damage mechanics [117, 123]. Fatigue damage concepts are widely studied. The most studies are performed on cyclic fatigue of metals [10, 11, 49, 57], while only few studies are focused on damage of polymers. The mechanisms are strongly influenced by the matrix and filler particles [13, 117, 123]. These damage concepts have not yet reached a level where they are verified. Moreover these concepts are time- and cost-effective. Another reason why damage concepts are beyond the focus of the present work lies in the lack of damage concepts for interfaces.

The fracture mechanics approach is formulated for bulk and interfacial cracks. Due to the nature of the approach using a crack tip field method, the critical values of test specimens can be compared with more complex structures. Widely-used test specimens for critical bulk properties are the CT-test (Mode-I) and CTS-probe (mixture of Mode-I,II). For interfacial cracking, several different types of test specimens are available. Therefore, the fracture mechanics approach is used to study the SBB flip chip interconnection.

For the description of a crack, it is assumed that the zone, where microscopic affects are the dominating regime, is limited to a certain area P, which is defined in Fig. 4.1. Around that area, the behavior of the cracked body can be described by the linear elastic field. This field is divided into the near field K and far field E. In the near field, the singular stress

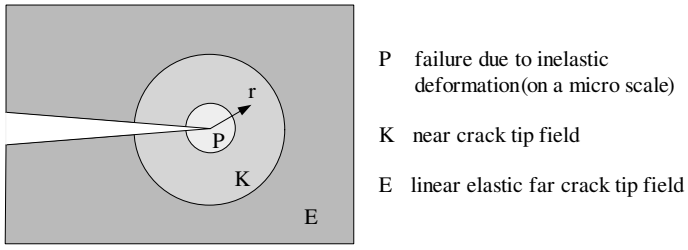


Fig. 4.1: Process zone of linear elastic fracture mechanics (LEFM); the plastic zone P describes the area where microcracking takes place which are mostly inelastic; the cracking occurs in the matrix or for filled materials between the filler particles and the surrounding matrix material; around that lies the near crack tip field K in which the stress intensity factor concept is valid: it is assumed that the stresses are a linear function of the stress intensity factor K, Eq.(4.6); around the K-field, the linear dependence of the stresses and stress intensity factor are no longer valid anymore).

field dominates and higher order terms can be neglected. The singularity leads to an infinite increase of the stresses for $r \to 0$. The type of singularity at the crack tip depends on the boundary conditions at the crack flanks. For linear-elastic materials, the singularity is of the type $r^{-1/2}$, whereas for perfect linear-plastic materials, the singularity shows a r^{-1} shape [24]. Moreover, the singularity of an interfacial crack is even more complex. The singularity shows an oscillating behavior very close to the crack tip.

The size of the different zones is strongly dependent on the plastic deformation of the body before new crack surface is built. Crack propagation in brittle material is rarely accompanied by plastic deformation. Epoxy resins show for temperatures below glass transition a brittle behavior [48, 122]. Therefore, the theory of linear-elastic fracture mechanics (LEFM) is sufficient to describe cracks within epoxy based polymers.

Cracks in two-dimensional load cases can be divided into different kinds of crack modes depending on the stress distribution σ_{yy}, σ_{xy}. Mode-I associates to a symmetric opening referring to the x-axis, Fig. 4.2. The antisymmetric displacement of the crack flanks in x-direction symbolizes the shearing mode (Mode-II).

Different concepts are available for LEFM and described in detail in [24]. In the presented work, the concept of the energy release rate (ERR) is used to describe the load on an existing crack. This method is capable of quantifying cracks in homogeneous materials, as well as cracks lying in the interface of a material combination [102]. Moreover, the method has the advantage that a regular Finite Element mesh is sufficient for numerical calculation of ERR [37, 38, 94]. Therefore, the method stands out in comparison to concepts which require a mesh with collapsed elements. These kinds of elements are required for obtaining accurate results in case of K-concept and J-integral [38, 102].

For LEFM, the energy release rate is related to the K-concept. It describes the singular stress field around a crack. The understanding of the concept is an essential requirement for

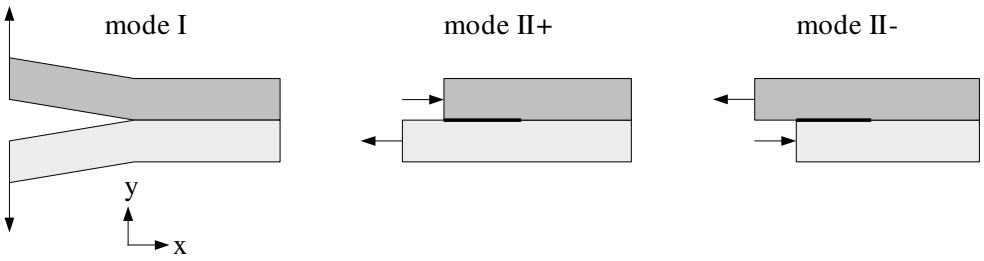


Fig. 4.2: Depending on the external load and geometry, cracks can be divided in different modes; Mode-I is opening mode ($\Delta y > 0$) where no sliding of the flanks is present ; Mode-II represents the sliding of the flanks along the x-axis; hereby, two different cases can be distinguished: Mode-II+: shearing mode ($\Delta x > 0$) and Mode-II-: shearing mode with ($\Delta x < 0$); in the most cases, both modes occur simultaneously;

the application of ERR to interfacial LEFM. Specifically, the definition of the singularity of an interfacial crack is a prerequisite.

4.2 Stress Field at Crack Tip

4.2.1 Bulk Crack

The stress and displacement field in an elastic, homogeneous body can be described by using complex stress functions [24]. For plane stress and strain conditions, the stress field is completely described by two complex functions $\Psi(z), \Phi(z)$ with the complex variable $z = r^{i\phi}$, with its respective conjugated variable $\bar{z} = r^{-i\phi}$. This approach originates from Muskhelishvili [60]. The solution for the stress and displacement field in terms of the complex functions are the formulas by Kolosov

$$\sigma_{\mathrm{x}} + \sigma_{\mathrm{y}} = 2\left[\Phi'(z) + \overline{\Phi'}(z)\right] \tag{4.1}$$

$$\sigma_{\mathrm{y}} - \sigma_{\mathrm{x}} + 2i\tau_{xy} = 2\left[\overline{z}\Phi''(z) + \Psi'(z)\right] \tag{4.2}$$

$$2G(u + iv) = \kappa\Phi(z) - z\overline{\Phi'}(z) - \overline{\Psi}(z) \tag{4.3}$$

with $\kappa = 3 - 4\nu$ for plane strain.

To describe the crack tip field, it is assumed that the complex functions are of the form of

$$\Phi(z) = A\, z^{\lambda} \quad \Psi(z) = B\, z^{\lambda} \tag{4.4}$$

where λ is restricted to be real and positive. A and B are constants which are determined from boundary conditions. Using Eq.(4.4), a linear system of equations is obtained. Assuming that the crack flanks are traction free – zero tensile and shear stress at the crack faces ($\psi = \pi$) –

the equation of the eigenvalues of the linear system of equations is obtained. For $r \to 0$ (K region in Fig. 4.1), the eigenvalue $\lambda = 1/2$ dominates and higher order eigenvalues can be neglected

$$\lambda = 1/2 \quad \text{for} \quad r \to 0. \tag{4.5}$$

It is convenient to split the solution into symmetric and asymmetric parts with respect to the x-axis. The symmetric stress and displacement fields are defined as the crack Mode-I

$$\sigma_{ij} = \left[\frac{1}{\sqrt{2\pi r}}\right] K_{\mathrm{I}}\, \mathrm{f}_{1,ij}(\varphi) \tag{4.6}$$

$$u, v = \left[\sqrt{\frac{r}{2\pi}}\right] \frac{K_{\mathrm{I}}}{\sqrt{2G}}\, \mathrm{f}_{u,v}(\varphi) \tag{4.7}$$

with the functions f, which depend only on the angle φ [24, 48, 123]. Crack Mode-II is represented by the asymmetric part of the solution. The expressions for Mode-II stress and displacement field can be found in [24, 48]. K_{I} and K_{II} are stress intensity factors and are a quantity to describe strength of the crack tip field.

The ratio of shear to tensile stress in a crack tip is defined as mode-mix, often also referred to as mode-mixity. For a crack in a homogeneous body, K_{I} accounts independently from the distance r to the crack tip for the tensile stress. So does K_{II} for the shear stress. Therefore, the mode-mixity can be expressed as

$$\psi = \arctan\left(\frac{\tau_{xy}(r,0)}{\sigma_{yy}(r,0)}\right) = \arctan\left(\frac{K_{\mathrm{II}}}{K_{\mathrm{I}}}\right) \neq f(r) \tag{4.8}$$

with ψ as the phase angle.

Recalling Eq.(4.6), the stress field shows a $r^{-1/2}$ singularity. This is characteristic for a crack in a linear elastic material with traction-free crack flanks. The displacement field shows a $r^{1/2}$ singularity, Eq.(4.7). Therefore, the displacement of the crack surfaces $\varphi = \pm\pi$ has a parabolic shape, Fig. 4.3,

$$\Delta v = v^{+} - v^{-} = \frac{K_{\mathrm{I}}}{\sqrt{2G}}\,(\kappa + 1)\,\left[\sqrt{\frac{r}{2\pi}}\right]. \tag{4.9}$$

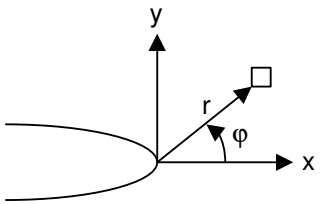


Fig. 4.3: Used coordinate system of crack tip field; due to the eigenvalue $\lambda = 1/2$, the displacement field at the crack tip shows a parabolic shape, Eq.(4.9)

The type of the singularity changes depending on the geometry of the crack tip (i.e. a v-notch), linear-elastic plastic crack tips, as well as other boundary conditions other than traction-free crack flanks (e.g. contact of the crack flanks).

K_i is obtained by calculating the stresses or displacements for $r \to 0$ from Eq. (4.6). For frequently-used geometries and loads (i.e. compact tension (CT) test), analytical solutions of the stress fields are listed in [24, 48]. For a CT specimen, K as function of the force P, the geometry parameters B,W and the crack length a are given by

$$K = \frac{P}{B\sqrt{W}}\, f(t) \quad \text{with} \quad f = \frac{2+t}{(1-t)^{3/2}} \sum_{\mathrm{i}=0}^{4} C_\mathrm{i}\, t_\mathrm{i} \tag{4.10}$$

with $t = a/W$ and the constants C_i. For more complex geometries and loads, the stress field has to be solved numerically. Finite Element packages mostly utilize the displacements at the crack flanks to calculate the stress intensity factors, compare Eq.(4.9) [4].

4.2.2 Interfacial Crack

The stress field of an interfacial crack can also be described by the equations of Kolosov Eq.(4.3). Because the crack lies between materials with different elastic properties, Fig. 4.4, the complex functions Eq.(4.4) are applied to each layer separately

$$\Phi_1(z) = A_1\, z^\lambda \quad \Psi_1(z) = B_1\, z^\lambda \quad \Phi_2(z) = A_2\, z^\lambda \quad \Psi_2(z) = B_2\, z^\lambda \tag{4.11}$$

where the subscript 1 and 2 denote the layer 1 and 2, respectively [14, 24].

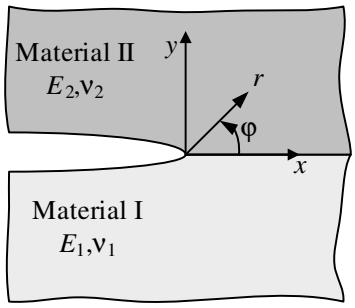


Fig. 4.4: A crack between two dissimilar materials

Applying the boundary conditions, (1) stress free crack surfaces at $\varphi = \pm\pi$ and (2) transition conditions between the two materials at $\varphi = 0$, lead to a system of linear equations[1]. The

[1] For different boundary conditions other than traction-free crack flanks, the eigenvalue and therefore the kind of singularity changes. The eigenvalue of flanks which are in contact leads to a solely real eigenvalue which is dependent on the coefficient of friction [14, 102].

solution of the system (higher order terms are neglected) is an eigenvalue which is similar to the one for the homogeneous case Eq.(4.5)

$$\lambda = 1/2 + \mathrm{i}\,\varepsilon. \tag{4.12}$$

ε is the bimaterial constant and describes the influence of the ratio of the two materials. In plane strain condition, ε is obtained by

$$\varepsilon = \frac{1}{2\pi} \ln\left(\frac{\mu_2\,\kappa_1 + \mu_1}{\mu_1\,\kappa_2 + \mu_2}\right) = \frac{1}{2\pi} \ln\left(\frac{1+\beta}{1-\beta}\right) \tag{4.13}$$

with $\kappa_i = 3 - 4\nu_i$ and μ_i as the bulk shear modulus for materials 1 and 2.

A more frequently used interpretation of the mismatch of the elastic properties are the Dundurs' parameters α and β [29]. They separate the influences of the plane tensile and shear modulus across the interface. α gives a relation of the Young's modulus of the both materials. Whereas β reveals the mismatch due to the difference of the in-plane bulk modulus. For plane strain with $E^* = \frac{E}{1-\nu^2}$, they are given as

$$\alpha = \frac{E_1^* - E_2^*}{E_1^* + E_2^*} \qquad \beta = \frac{1}{2}\,\frac{\mu_1\,(1-2\nu_2) - \mu_2\,(1-2\nu_1)}{\mu_1\,(1-\nu_2) + \mu_2\,(1-\nu_1)}. \tag{4.14}$$

For the homogeneous case $E_1 = E_2$ and $\nu_1 = \nu_2$ where the material mismatch vanishes, the Dundurs' parameters α, β, as well as the bimaterial constant ε, are zero.

The solution of the stress field $\sigma(r, \varphi)$ is obtained applying the eigenvalue to Eq.(4.11). The solution can be found in [14, 29]. The stress field in the ligament between the two materials, $\varphi = 0$, is given by

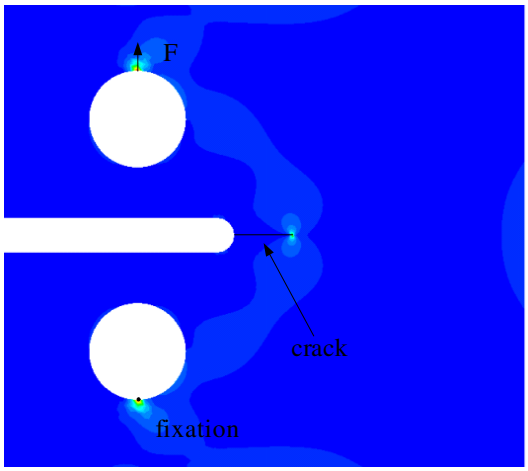
$$\sigma_{yy}(r, \varphi = 0) + i\sigma_{xy}(r, \varphi = 0) = \left[\frac{r^{\mathrm{i}\varepsilon}}{\sqrt{2\pi r}}\right] K. \tag{4.15}$$

K represents the complex interface stress intensity factor

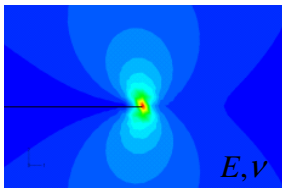
$$K = K_1 + \mathrm{i}K_2 = |K|\, r^{i\varepsilon}. \tag{4.16}$$

Because of the asymmetry of the material properties, K_1 and K_2 do not represent the crack opening mode (Mode-I) and shearing mode (Mode-II), respectively [24].

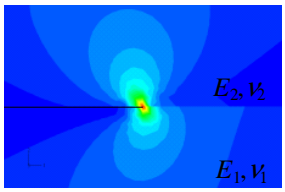
The asymmetry of the stress field due to the difference in material properties can be seen in Fig. 4.5. A compact tension (CT) specimen is symmetrically loaded by a force F, Fig. 4.5a. The symmetric test configuration for a crack in a bulk material (E, ν) leads to a symmetric stress field, shown in Fig. 4.5b. Therefore, Mode-II equals $K_{\mathrm{II}} = 0$. For a bimaterial specimen with a pre-crack lying between two different materials $((E_1, \nu_1), (E_2, \nu_2))$, the stress field is asymmetric, Fig. 4.5c, which leads to $K_{\mathrm{II}} \neq 0$.



(a) FE analysis of CT specimen with fixation and symmetric loading by force F



(b) Bulk: $K_{\mathrm{II}} = 0$



(c) Interface: $K_{\mathrm{II}} \neq 0$

Fig. 4.5: Comparison stress field (σ_{yy}) for a bulk and interfacial crack at symmetric loading; (b) symmetric stress field hence homogeneous material; (c) asymmetric stress field hence bimaterial crack

In order to calculate the stress intensity factors which represent the real Mode-I and Mode-II of the interface, *Hutchinson* suggests using the formula ψ [29]

$$\psi = \arctan\left[\frac{\Delta u}{c\Delta v}\right] + \arctan(2\varepsilon) + \varepsilon \ln(r/L) \tag{4.17}$$

with

$$c = \sqrt{\frac{2(\mu_1 + \mu_2)}{\mu_1 \frac{1-2\nu_2}{1-\nu_2} + \mu_2 \frac{1-2\nu_1}{1-\nu_1}}}, \tag{4.18}$$

where L as a characteristic length is introduced.

The first term in Eq.(4.17) gives the ratio of sliding and opening of the crack flanks, modified by the factor c which counts for the difference in elastic properties of both layers. In the case of a crack in a homogenous material, c becomes zero - so do the other two terms - and the phase angle is solely calculated by the relative displacements of the flanks. The second and third term are due to the difference of the elastic properties.

The influence of the characteristic length can also be understood as a rotation around the angle consisting of the first and second term in Eq.(4.17). The rotation depends on the selection of the characteristic length L as well as on the bimaterial constant ε. This is shown in Fig. 4.6.

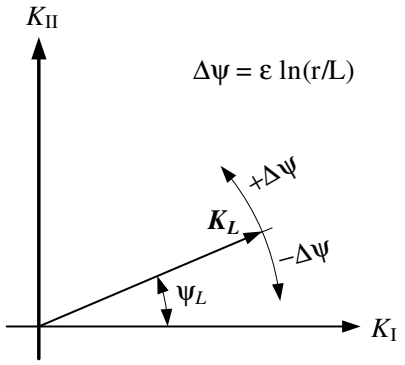


Fig. 4.6: $K_{\mathrm{I}}, K_{\mathrm{II}}$-space; complex stress intensity factor K_L at $r = L$; rotation of K by $\Delta\psi = \varepsilon \ln(r/L)$ caused by oscillating singularity; $|\Delta\psi| \leq 4°$ for epoxy/LCP interface ($\varepsilon_{\mathrm{epoxy/LCP}} \approx 0.03$)

The tension and shear stresses in the ligament are obtained at $r = L$. In the presented work, the element size of the Finite Element mesh L is used as the characteristic length. A element size of about 0.5 μm is chosen. This leads to a simplification of Eq.(4.17)

$$\psi = \arctan\left[\frac{\Delta u}{c\Delta v}\right] + \arctan(2\varepsilon). \tag{4.19}$$

The influence of the third term can be estimated when $r = \Delta r + L$ is chosen, with $\Delta r = 0.1L$. The rotation contributed by the third is around 0.16°, which can therefore be neglected.

With $\varepsilon_{\mathrm{epoxy/LCP}} \approx 0.03$, the rotation due to the oscillating singularity is $|\Delta\psi_{\max}| = 4°$.

4.3 Energy Release Rate

4.3.1 Concept

The energy release rate (ERR) is based on the theorem of energy conservation. Once a crack propagates from a to $a + \Delta a$, the internal energy of the body degrades. This energy can be related to the energy needed to produce new crack surface. This leads to the definition of the energy release rate which simplifies for plane strain to

$$G = -\frac{\mathrm{d}\Pi}{\mathrm{d}a}. \tag{4.20}$$

G is of the unit $[force/length]$. A more figurative definition of the ERR is the contention by *Irwin* [31]. It is proposed that if the crack extends by a small amount Δa, the energy absorbed in the process is equal to the work required to close the crack to its original length. Applying this statement, the ERR can also be used to characterize the crack Mode-I, -II by

$$G_{\mathrm{I}} = \lim_{\Delta a \to 0} \int_0^{\Delta a} \sigma_{yy}(\Delta a - r, 0)\, \Delta v(\Delta a - r, \pm\pi)\, \mathrm{d}r \tag{4.21}$$

$$G_{\mathrm{II}} = \lim_{\Delta a \to 0} \int_0^{\Delta a} \tau_{xy}(\Delta a - r, 0)\, \Delta u(\Delta a - r, \pm\pi)\, \mathrm{d}r \tag{4.22}$$

with the stresses at the near crack tip $\sigma_{yy}(r, \varphi)$, and $\tau_{xy}(r, \varphi)$, $\Delta v(r, \varphi)$ the crack opening displacement and $\Delta u(r, \varphi)$ the sliding of the crack flanks [38, 76, 94, 123]. Moreover, the components G_{I} and G_{II} are linearly added to the complete energy release rate[2]

$$G = G_{\mathrm{I}} + G_{\mathrm{II}}. \tag{4.23}$$

This interpretation of the ERR is utilized by the Virtual Crack Closure Technique (VCCT) which is used to numerically obtain G. VCCT was first introduced by *Rybicki* and *Kanninen* [94]. A detailed adaption to Finite Element formulation can be found in [38]. This implementation into FE analysis utilizes the displacements u, v and the forces X, Y at the nodes to calculate G. The forces represent the cohesion of the corresponding nodes against separation. Therefore, the Eqs.(4.21),(4.22) are translated for a plane strain to

$$G_{\mathrm{I}} = -\frac{1}{2\Delta a} \left[Y_{\mathrm{i}} \left(u_{\mathrm{l}}^{u} - u_{\mathrm{l}}^{\mathrm{l}} \right) + Y_{\mathrm{j}} \left(u_{\mathrm{m}}^{u} - u_{\mathrm{m}}^{\mathrm{l}} \right) \right] \tag{4.24}$$

$$G_{\mathrm{II}} = -\frac{1}{2\Delta a} \left[X_{\mathrm{i}} \left(v_{\mathrm{l}}^{u} - v_{\mathrm{l}}^{\mathrm{l}} \right) + X_{\mathrm{j}} \left(v_{\mathrm{m}}^{u} - v_{\mathrm{m}}^{\mathrm{l}} \right) \right] \tag{4.25}$$

where the notation for the displacements and forces are shown in Fig. 4.7.

A requirement for adapting VCCT to Finite Element analysis is the accessibility to the forces X, Y at the nodes i, j. For the used Finite Element package *ABAQUS*, these forces are not directly available. Therefore, the forces are obtained by a work-around, by adding connector elements in the crack tip [86].

For a crack in a homogeneous body, ERR can be expressed in terms of the stress intensity factors [24]. Because ERR describes the energy change caused by crack propagation in an elastic body, it refers to both crack modes

$$G = \frac{1}{E^*} \left(K_{\mathrm{I}}^2 + K_{\mathrm{II}}^2 \right) \tag{4.26}$$

with $E^* = \frac{E}{1-\nu^2}$ for plane strain. Invoking Eqs.(4.21),(4.22), the stress intensity factors belonging to the single modes can be calculated by [94]

$$K_{\mathrm{I}} = \sqrt{E^*\, G_{\mathrm{I}}} \quad K_{\mathrm{II}} = \sqrt{E^*\, G_{\mathrm{II}}}. \tag{4.27}$$

[2]Where the stress intensity factor K symbolizes a vectorized value, ERR is scalar and can be added as performed in Eq.(4.23)

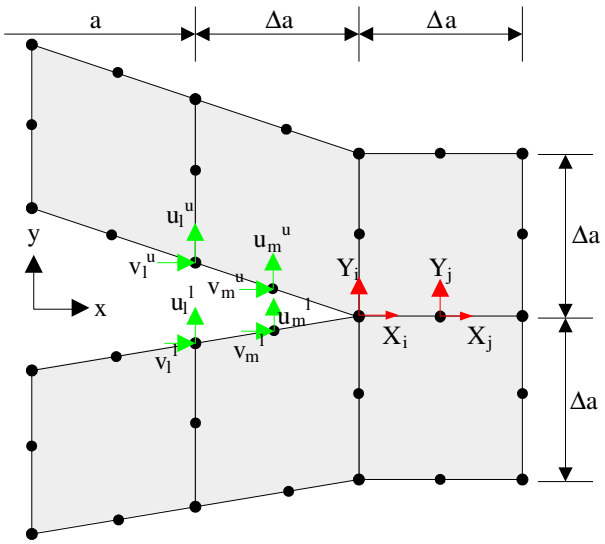


Fig. 4.7: Virtual Crack Closure Technique (VCCT) for implementation of ERR into Finite Element analysis; using displacements and forces at nodes; adaption into FE package *ABAQUS* by using connector elements [86]

4.3.2 ERR for Interfacial Fracture Mechanics

The ERR accounts for the energy set free during tensile as well as shear loading of a crack Eq.(4.27). This relation is also valid for an interfacial crack and modifies to

$$G = \frac{1}{\overline{E}\cosh^2(\pi\varepsilon)}\left(K_1^2 + K_2^2\right) = \frac{1}{\overline{E}\cosh^2(\pi\varepsilon)}|K|, \tag{4.28}$$

because of the change of the elastic properties of the material combination, with $\overline{E}$

$$\frac{1}{\overline{E}} = \frac{1}{2}\left(\frac{1}{E_1} + \frac{1}{E_2}\right). \tag{4.29}$$

The overall energy release rate for an interfacial crack, gathered from VCCT Eqs.(4.21),(4.22), is an adaption of Eq.(4.23)

$$G = G_1 + G_2. \tag{4.30}$$

G_1 and G_2 do not represent the Mode-I and -II of the interfacial crack. In order to perform mode separation, the mode-mixity angle ψ from Eq.(4.17) and the total ERR G are used.

In the present work, the mode-mixity ψ and the total ERR G are used to describe the crack load of an interfacial crack.

Chapter 5

Material Characterization

5.1 Relevant Material Properties

To describe the thermo-mechanical behavior of a flip chip interconnection which is exposed to thermal cycling, the Young‘s modulus E, Poisson‘s ratio ν and the Coefficient of thermal expansion α are the relevant material properties. These factors determine the warpage, stresses and strain caused by temperature change.

The underfills and the non-conductive adhesives (NCA) are epoxy-based polymers. Three of the four studied materials are filled with SiO_2 particles. Cure shrinkage of the underfills and NCAs already leads at curing temperature to residual stresses. Therefore, the volume change caused by curing is measured. The curing is also accompanied by a change of the Young's modulus. The Young's modulus, depending of the rate on conversion, is not determined due to lack of reliable measurement methods. Epoxy-based polymers show visco-elastic behavior in the cured state. Therefore, the time- as well as temperature-dependent Young's modulus is obtained.

Liquid Crystal Polymer (LCP) is used as board material. The plates for the MID boards are manufactured using injection molding. This process leads to orthotropic thermo-mechanical material properties depending to the flow direction of the LCP in the molding tool. The time- and temperature-dependent material properties are also studied for LCP.

In addition to the underfill and board material, gold stud bumps, as well as a silicon die, are modeled for studying the performance of the flip chip interconnection. These materials are assumed to have a linear-elastic time and temperature independent material behavior. The values are taken from literature.

At the beginning of this section, the structure and specific properties of the epoxy-based underfills and NCAs are discussed, followed by detailed description of LCP. The determina-

tion of the thermo-mechanical properties such as Young's modulus and coefficient of thermal expansion (CTE), are displayed for the underfills, NCAs and LCP together. Tab. 5.1 gives a preliminary overview of the material models for the materials used.

Tab. 5.1: Table of materials used and applied material models

Material	**Behavior**	**Constitutive Law**	**Domain**	**Component**
epoxy resin	visco-elastic	time-temperature-shift	isotropic	UF, NCA
LCP	elastic, temperature-dependent	linear	orthotropic, thickness-dependent	MID board
gold	elastic	linear	isotropic	stud bump
silicon	elastic	linear	isotropic	chip

5.2 Used Materials

5.2.1 Underfills and NCAs

The underfills and the NCAs are unfilled and filled epoxy-based polymers. The materials differ in matrix, hardener type, and filler grade, as well as in size and distribution of particles of the filler. Additionally, special ingredients are used to optimize flow, cure and adhesion properties of the underfills and NCAs [19, 32, 43, 44, 45, 77, 119, 126].

Two different underfills are used – UF1 and UF2. Both have a bisphenol matrix and an anhydride hardener. The underfills are filled with SiO_2 particles. Tab. 5.2 shows the cure shrinkage and the filler of the underfills used. The measurement of the cure shrinkage is determined by volume dilatometry. The non-conductive adhesives used are also epoxy-based polymers. The NCA ensures steady electrical and mechanical contact between the stud bump and the metallization of the board. NCAs are usually less filled which results in different material properties in comparison to capillary underfills. The hardeners for commercially available NCAs are quite different. Fast-curing NCAs use amine as a hardener, whereas for slow-curing NCAs anhydride hardener is used. In the present work, two different kinds of NCAs are used: NCA1, a non-filled epoxy with an amine hardener and NCA2, a filled epoxy with an anhydride hardener, refer to Tab. 5.3.

Tab. 5.2: Cure shrinkage and filler content of underfills UF1 and UF2; particle size standardized to average particle size of UF1

	UF1	**UF2**
cure shrinkage [%]	1.8	0.4
filler	SiO_2	SiO_2
filler content [Vol-%]	14	23
particle size standardized, [average $^{\text{min}}_{\text{max}}$]	$1\,^{0.6}_{1.7}$	$2.2\,^{0.5}_{5}$

Tab. 5.3: NCAs used – NCA1 and NCA2 – filler content and cure shrinkage; particle size standardized to average particle size of UF1

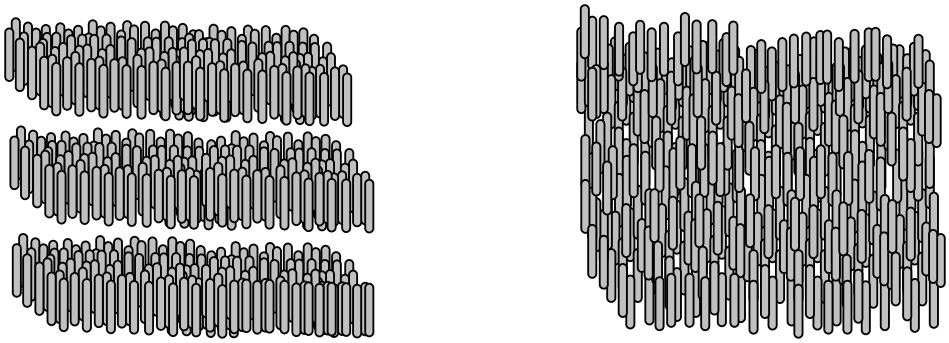
	NCA1	**NCA2**
cure shrinkage [%]	1.8	0.3
filler	-	SiO_2
filler content [Vol-%]	0	23
particle size standardized, [average $^{\text{min}}_{\text{max}}$]	n.a.	$1\,^{0.6}_{1.6}$

5.2.2 Liquid Crystal Polymer (LCP)

Liquid Crystal Polymer (LCP) builds a structure, which is between an isotropic liquid and a solid crystal state [34, 95]. It is defined as a fourth state of aggregation. Already in the liquid state the molecules of LCP build a crystal-like orientation. This is due the fact that the molecules have a high chain rigidity. Additionally, the ratio of length and diameter is very high. Therefore, the highest package density is achieved for parallelly orientated molecules. The molecules consist of rigid anisotropic units, which are called mesogens [34]. These units are able to form either rodlike molecules, main chain LCPs, or branches, the so-called side chain LCPs. Chemicals used to build mesogentic groups are 4-hydroxybenzoic acid (HBA), hydroquinone (HQ), terephthalic acid (TA) and 2-hydroxy-6-naphthoic acid (HNA) [34].

LCP shows different spacious structures: cholesteric, smectic and nematic [95], the two latter are schematically sketched in Fig. 5.1. The molecules are orientated parallel without building entanglement, like other thermoplast materials.

The liquid crystalline structure explains the anisotropy of the material properties in a macroscopic perspective. The dependency on direction of the orientation results in the magnetic, optical, electrical, thermal, as well as the mechanical material properties. Especially the thermo-mechanical properties are strongly influenced by the orientation. The liquid crystalline structure leads to low temperature dependency of the LCP in comparison to other



(a) Smectic (b) Nematic

Fig. 5.1: Types of phases of Liquid Crystal Polymer [95]; parallel organization of polmyer molecules leads to anisotropic macro behavior even without any filler, e.g. thermo-mechanical properties

thermoplastics [96].

Injection molding is used to manufacture the substrates for the MIDs. Caused by the crystalline structure and the flow during injection molding, LCP plates show distinct skin and core morphology [68]. The molten polymer injected into the molding cavity reaches the flow front and experiences an advancing flow. This leads to a strong orientation of the molecules at the wall. The portions at the center are injected late and are related to shear flow [67].

Fig. 5.2 shows the layered structure of a neat LCP depending on the flow direction. Four

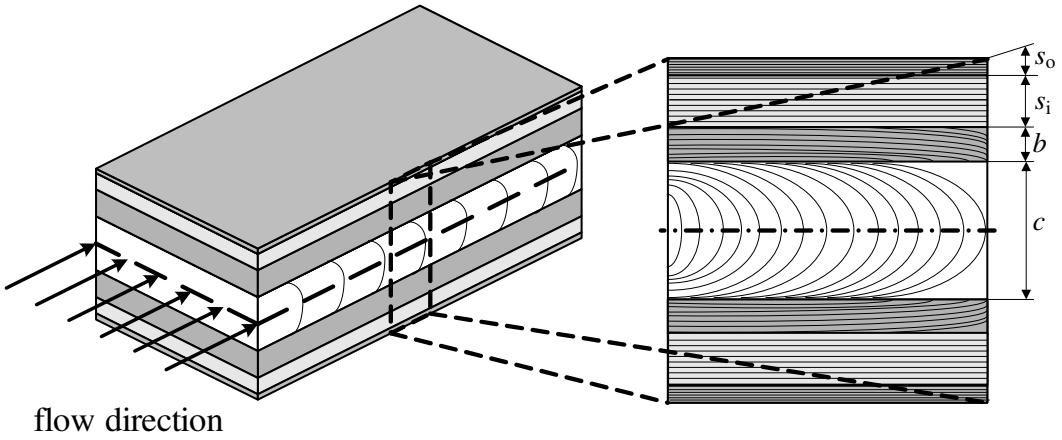


Fig. 5.2: Layer structure of neat LCP corresponding to flow direction; outer skin $s_o \approx 2$ %, inner skin $s_i \approx 11$ %, boundary layer $b \approx 8$ %, core layer $c \approx 58$ %; outer and inner skin layer s_o, s_i are completely aligned in flow direction; boundary b layer shows quenched crystalline appearance (changing orientation from s_i to c); core layer c is perpendicular-orientated to flow direction [95]

different layers can be distinguished: outer skin layer s_o, inner skin layer s_i, a boundary layer b as well as core layer c [95].

The change in orientation along the thickness of an injection molded LCP can be clearly seen in Fig. 5.3.

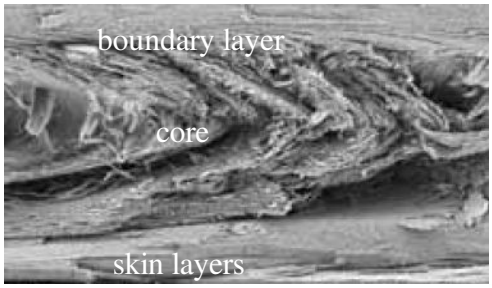


Fig. 5.3: SEM picture of cross section of a LCP plate [109]

Some studies point out that the outer and inner skin layer are not clearly distinguished [96]. Nevertheless, the skin layer respectively skin layers are highly orientated and show therefore strong differences in material properties in comparison to the core. The thickness of the skin layers are almost independent from the overall plate [96]. Therefore, the thicker the plate, the higher the portion of the core and less dominant the highly orientated skin. Nevertheless, the macroscopic material properties are built in an integral way over both layers, which leads to thickness-dependent material properties.

The influence of layer thickness and flow direction on the material properties like Young's modulus and CTE are discussed in the corresponding sections.

5.3 Modeling of Visco-Elastic Material Behavior

Epoxy-based polymers show a time-dependent material behavior. The theory of linear visco-elasticity describes the deformation behavior of polymers restricted to small strains [98]. The time dependent stress-strain relation is defined as [22, 98, 123, 125]

$$\sigma(t) = \int_{-\infty}^{t} E(t-\xi) d\varepsilon(\xi) = \int_{-\infty}^{t} E(t-\xi) d\dot{\varepsilon}(\xi) d\xi. \tag{5.1}$$

The solution of the integral Eq.(5.1) can be found by solving a differential equation based on generalized Maxwell elements. The solution of the differential equation is Eq.(5.2)

$$\frac{\sigma(t)}{\varepsilon(t)} = E(t) = \sum_{i=1}^{N} E_i \, e^{-\frac{E_i}{\eta_i}(t-t_0)} + E_\infty. \tag{5.2}$$

The visco-elastic material behavior of polymers can be measured by Dynamic Mechanical Analysis (DMA), among others. The specimen is exposed to a forced sinusoidal oscillation

in tension. Because of visco-elasticity, the strain is phase-shifted to the stress by angle δ. Therefore, a complex approach must be used to connect strain and stress

$$\varepsilon^* = \varepsilon_0 \, e^{(i\omega t)} \quad \text{and} \quad \sigma^* = \sigma_0 \, e^{i(\omega t + \delta)} \tag{5.3}$$

with ε_0 and σ_0 as the magnitude of the complex strain and stress, respectively. The complex dynamic module is then defined as

$$E^*(\omega) = E^{'}(\omega) + iE^{''}(\omega) = \frac{\sigma^*}{\varepsilon^*} \tag{5.4}$$

where $E^{'}$ represents the storage modulus and $E^{''}$ the lost modulus. Both $E^{'}$ and $E^{''}$ are obtained from DMA measurements for different frequencies and temperatures. The specimens made of the adhesives for the DMA measurements have a size of $50 \times 10 \times 1$ mm^3. The curing temperature of the specimens are the same as for assembly of the flip chip interconnections. The storage and lost modulus are determined for temperature from -50 °C to 220 °C and for frequencies from 0.5 Hz to 63 Hz. Fig. 5.4 shows the storage modulus from DMA measurements for UF1.

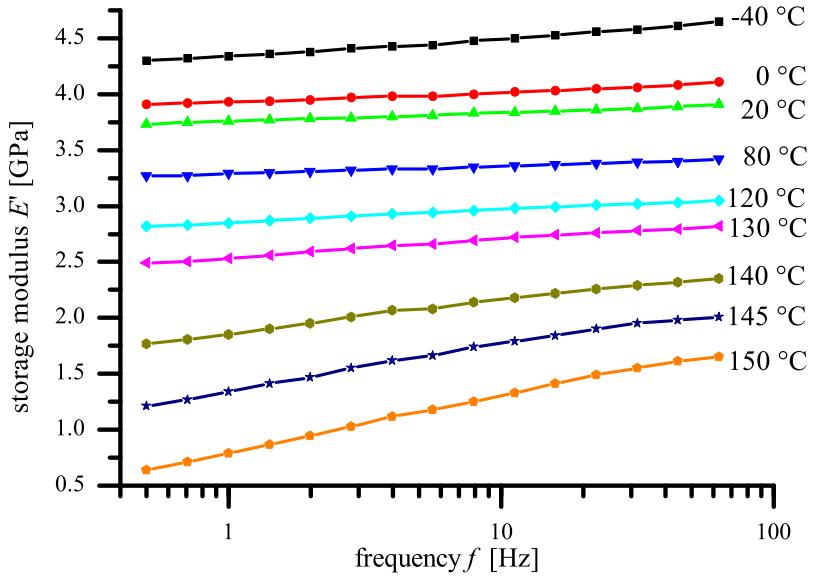


Fig. 5.4: Storage modulus for UF1 gathered from DMA measurements for different frequencies and temperatures; it reveals the frequency respectively time dependencies of the storage modulus, especially for temperatures around the glass transition region.

For many polymer-based materials, it is shown that the material behavior at elevated temperatures is similar to the behavior at lower temperatures with slower loading times. Figuratively increasing the temperature T equals a compression of the time scale of the reference temperature T_{ref} [123]. Or applied to the frequency scale, elevating the temperature leads to stretching of the frequency scale. This time/frequency-temperature-superposition

is especially useful for obtaining the long-term behavior of a polymer based on short-time measurements [52]. The superposition and therefore the change in frequency scale can be described as

$$\log \omega = \log a(T) + \log \omega_{\text{eff}}, \tag{5.5}$$

where ω_{eff} stands for the frequency at reference temperature. Therefore, the material behavior $E(\omega_{\text{eff}}, T_{\text{ref}})$ can be translated to the current frequency ω and temperature T by applying the shift function $a(T)$

$$E(\omega, T) = E(\omega_{\text{eff}}, T_{\text{ref}}). \tag{5.6}$$

Depending on the material, time and temperature range, there are different methods for describing the time-temperature-shift. One of the most studied and used methods is the so-called WLF function which was developed by *William*, *Landel* and *Ferry*. Due to the assumption of the WLF function, it is strictly only valid 50 K above and below reference temperature [52]. The reference temperature is the glass transition temperature of the polymer. The glass transition temperature of the materials used is approximately 120 °C to 150 °C. The application temperature is between 150 °C and -40 °C, therefore the WLF function is not applicable. Instead, to describe the time-temperature-shift, the shift function as function of temperature is given as table in the form of $a(T)$.

Applying the frequency-temperature-shift, mastercurves of the frequency dependent modulus can be obtained. These mastercurves for the glass transition temperature are shown in Fig. 5.5.

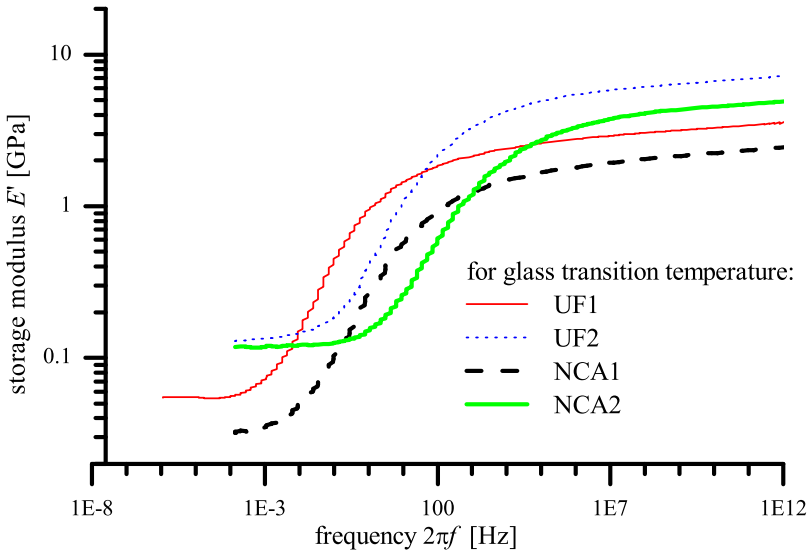


Fig. 5.5: Mastercurves for the storage modulus for underfills and NCAs based on frequency-temperature shift; measurements performed in the frequency domain using Dynamic Mechanical Analysis (DMA)

The frequency range for the mastercurves lies between 10^{-6} Hz and 10^{12} Hz where the measurement cover only one decade (0.5 Hz to 63 Hz). Converting the frequency range into the time regime, the DMA measurement covers times between 10^{-12} seconds and 277 hours. The time for a thermal cycle is about 8 to 12 minutes. This shows that measurement of the time behavior of a polymer using the frequency method (DMA) can only be used to give qualitatively results and to be used to compare different polymers, which is the focus of the presented work. A more relevant test method for the characterization of the viscoelastic behavior is the relaxation experiment where the time range is more suitable to describe the behavior at thermal cycling [125]. Nevertheless, relaxation experiments are much more time consuming.

The frequency-temperature shift for the materials used is displayed in Fig. 5.6. The rising shift factors for temperatures approaching -40 °C leads to a shift of the mastercurve to higher frequencies and therefore higher storage modulus.

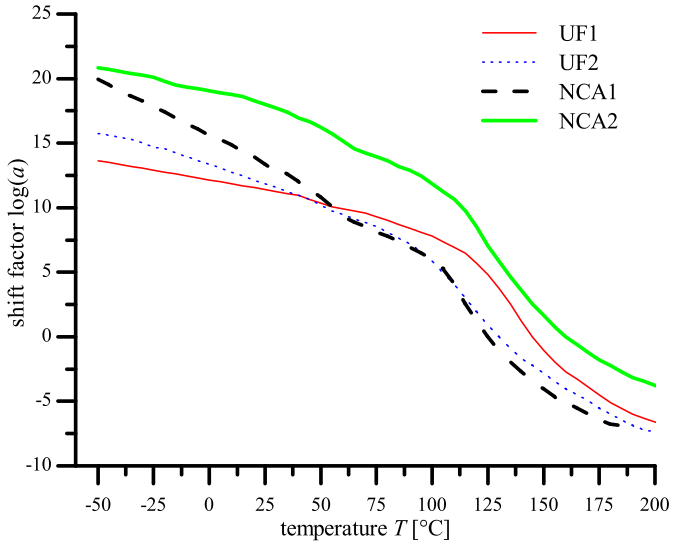


Fig. 5.6: Shift factor a(T) based on frequency-temperature obtained from Fig. 5.5

An approach widely used to describe the storage and loss modulus is the Prony series, here in the frequency regime [22],

$$E'(\omega) = E_0 \left[1 - \sum_{i=1}^{N} e_i\right] + E_0 \sum_{i=1}^{N} \frac{e_i \tau_i^2 \omega^2}{1 + \tau_i^2 \omega^2} \tag{5.7}$$

$$E''(\omega) = E_0 \sum_{i=1}^{N} \frac{e_i \tau_i \omega}{1 + \tau_i^2 \omega^2} \tag{5.8}$$

where e_i and τ_i define the Prony coefficients and times, respectively. E_0 states the instanta-

neous Young's modulus, which refers to the long-term Young's modulus E_∞ by

$$E_\infty = E_0 \left[1 - \sum_{i=1}^{N} e_i\right]. \tag{5.9}$$

The storage and loss modulus described by the Prony series, the instantaneous or long-term storage modulus, as well as the frequency-temperature-shift $a(T)$ are sufficient to describe the visco-elastic material behavior of the epoxy-based underfills and NCAs.

The specimens for the DMA measurements of LCP have a size of 50×10 mm^2 $\times$ thickness. They are taken out of an injection molded plate with the size 80×80 mm^2, Fig. 5.7.

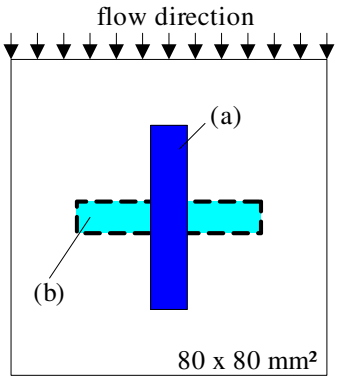


Fig. 5.7: Schematic representation of injection molded LCP plate and the specimen preparation for DMA measurements; specimen (a) in flow direction and (b) transversal flow direction

Fig. 5.8 displays the DMA measurements of LCP as function of frequency at different temperatures. It reveals that LCP has an almost linear-elastic material behavior. Therefore, the

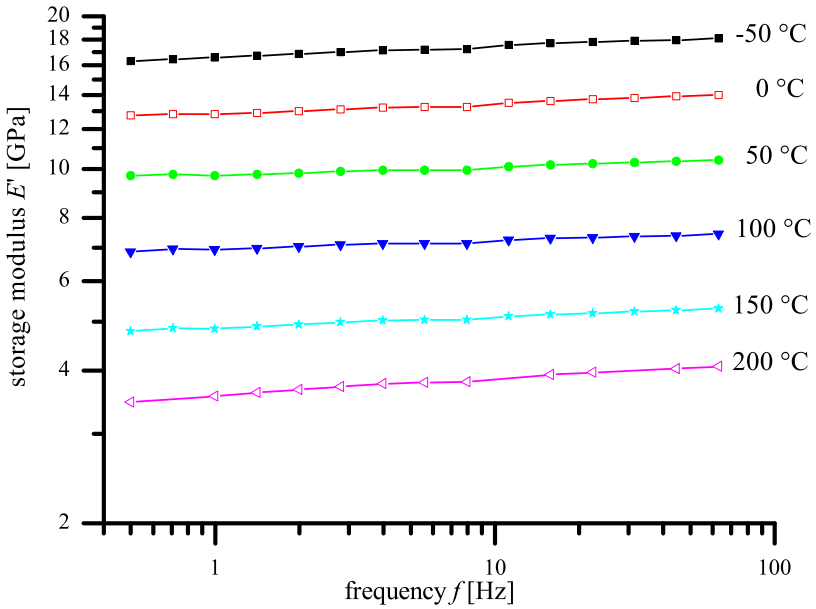


Fig. 5.8: Storage modulus E' for LCP as function of frequency; LCP shows a linear-elastic behavior

material properties for LCP are taken as linear-elastic, but temperature dependent.

The material properties of LCP are dependent on the substrate thickness, as well as on the orientation throughout injection molding. Fig. 5.9 presents the Young's modulus of LCP for 1 mm and 2 mm plates, as well as for material orientation along flow direction and transversal to flow direction. The dependency on the material thickness is only dominant for

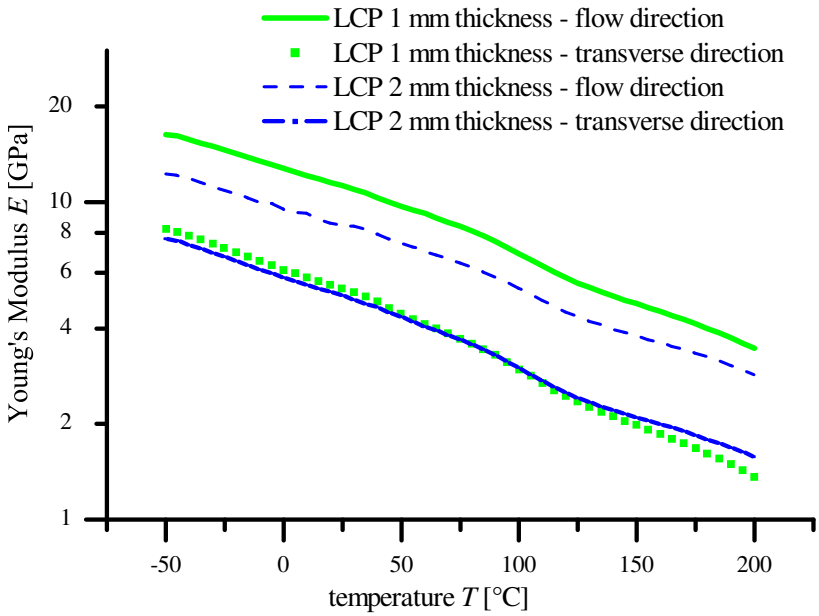


Fig. 5.9: Storage modulus E' of LCP for orientation along flow direction and transversal

material orientation along flow direction. This is caused by the fact that the highly orientated injection skin influences the material behavior.

5.4 Coefficient of Thermal Expansion (CTE)

The coefficient of thermal expansion (CTE) is determined by using Thermo-Mechanical-Analysis (TMA). The test specimens have a size of 5×5 mm^2 $\times$ thickness. The thickness of the underfills and NCAs are 5 mm, whereas the thickness of the LCPs is defined by the substrate thickness. The epoxy specimens are cured corresponding to the temperature profile used for the flip chip assembly process. The underfills UF1 and UF2 are cured at 150 °C, whereas the NCAs are cured at 180 °C. The CTE of adhesives based on epoxy resins are different below and above glass transition temperature T_g. α_1 and α_2 are the CTE below and above T_g, respectively.

The CTE is extracted from TMA measurements taking the slope of the curve. The CTEs as function of temperature of the underfills and NCAs are shown in Fig. 5.10.

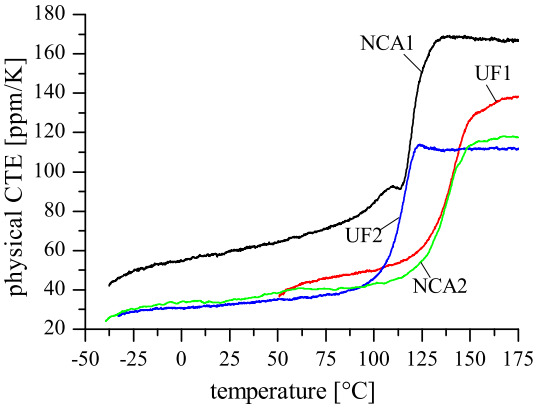


Fig. 5.10: Coefficient of thermal expansion of used underfills and NCAs as function of temperature

Tab. 5.4 summarizes the values of the coefficient of thermal expansion below and above T_g as well as glass transition temperatures taken from TMA measurements. Additionally, an averaged CTE value is calculated based on α_1, α_2 and T_g which simplifies the comparison between the underfills and NCAs used. The calculation is performed by using

$$\overline{\alpha} = \alpha_2 \frac{T_\mathrm{g} - T_\mathrm{low}}{T_\mathrm{high} - T_\mathrm{low}} + \alpha_1 \frac{T_\mathrm{high} - T_\mathrm{g}}{T_\mathrm{high} - T_\mathrm{low}} \tag{5.10}$$

where T_high and T_low represent the upper and lower temperature of the thermal cycles, i.e. 150 °C and -40 °C. Nevertheless, for the FE analysis, the temperature dependent CTE values are used.

As for the Young's modulus of LCP, the CTE is also dependent on the thickness of the substrate and molecule orientation corresponding to injection molding process. The size of the TMA specimens are 5×5×1 mm^3 and 5×5×2 mm^3 for 1 mm and 2 mm substrates, respectively.

Tab. 5.4: CTE and glass transition temperature T_g of underfills and NCAs obtained from TMA measurements; averaged CTE value $\overline{\alpha}$ based on a cooling from 150 °C to -40 °C is only calculated to give a more convenient value to compare the materials used; for the FE simulation, the temperature dependent CTE value, as measured using the TMA method, is used, Eq.(5.10).

Adhesive	**NCA1**	**NCA2**	**UF1**	**UF2**
α_1 / α_2 [ppm/K]	65/160	36/117	42/132	32/110
T_g [°C]	117	137	145	120
$\overline{\alpha}$ [ppm/K]	82	42	44	44

Fig. 5.11 shows TMA measurements for LCP. It reveals that the CTE value of LCP, in the temperature range considered, is independent of the temperature. Similar to the Young's

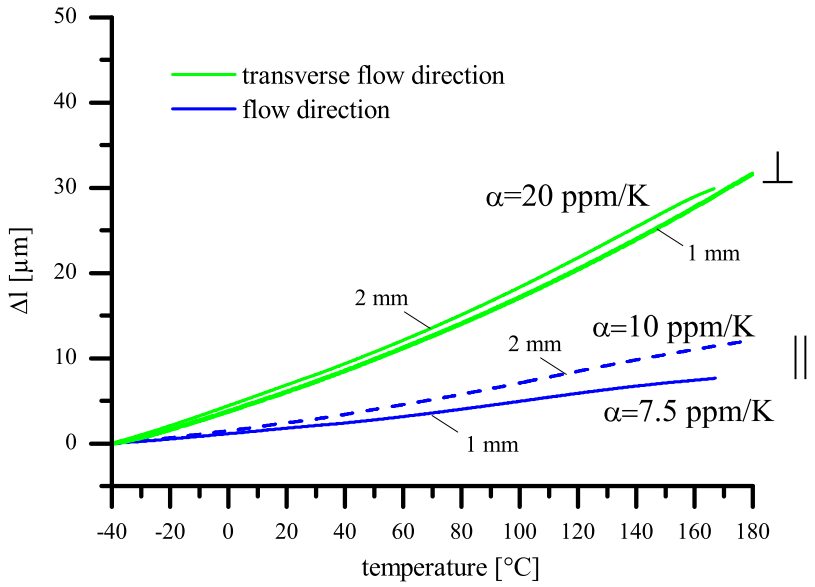


Fig. 5.11: Thermal expansion of LCP; CTE depends on thickness as well as on orientation with respect to flow direction during injection molding.

modulus, the ratio between the CTE longitudinal and transversal gets closer to the isotropic case for a thicker plate.

5.5 Calculation of Properties for Interface Adhesive/LCP

The interfacial fracture approach requires the calculation of the bimaterial constant ε, Eq.(4.13). The Poisson ratio and the Young's modulus of both materials at -40 °C are taken to calculate the bimaterial constant. The FE software ABAQUS used does not allow to combine temperature dependency of the Poisson's ratio and visco-elastic material behavior. Therefore, a constant Poisson's of 0.3 is used for all materials.

The values for the various interfaces are listed in Tab. 5.5.

Tab. 5.5: Bimaterial constant ε for interface adhesive/LCP and adhesive/silicon at -40 °C; calculated for plane strain condition from Eq.(4.13); indexing for upper and lower material from Fig. 4.4

Adhesive	**NCA1**	**NCA2**	**UF1**	**UF2**
LCP 1 mm $\parallel$	-0.0431	-0.0211	-0.0328	-0.0328
LCP 1 mm $\perp$	-0.0215	0.0063	-0.0078	-0.0078
LCP 2 mm $\parallel$	-0.0352	-0.0104	-0.0233	-0.0233
LCP 2 mm $\perp$	-0.0192	0.0089	-0.0053	-0.0053
silicon	-0.0698	-0.0649	-0.0677	-0.0659

Chapter 6

Critical Bulk and Interfacial Fracture Toughness

6.1 Crack Initiation and Propagation in Homogenous Media

The physical mechanism of crack initiation and crack propagation varies depending on the material. For highly-filled polymers, crack mechanisms are described in [117, 122, 123]. Crack initiation is caused by brittle fatigue of the media. The prevailing mechanisms for epoxy-based polymers are the formation of micro cracks [13]. Especially for highly-filled epoxy resins, maximum stresses and strains act between the filler particle and the epoxy matrix. For fracture of brittle homogenous materials, the fracture path is assumed to have a Mode-I dominant crack-tip stress field [58, 122]. Fracture will occur when the existing stress intensity factor respectively energy release rate exceeds the critical stress intensity factor K_{Ic} respectively ERR G_{c}

$$G_{\mathrm{I}} > G_{\mathrm{Ic}} \quad \text{resp.} \quad K_{\mathrm{I}} > K_{\mathrm{Ic}}. \tag{6.1}$$

The critical stress intensity factor K_{Ic} is a material-related fracture parameter and is defined as fracture toughness. It is used to compare the fracture behavior of different materials. Because of the local character of the K-concept, the K_{Ic} obtained for different types of test specimens, but the same material can be compared [102]. The comparability is only guaranteed for the same test conditions, which are primarily test speed and temperature as well as process conditions. Typical values of K_{Ic} for steel are in the range of 30..100 $\mathrm{MPa}\sqrt{\mathrm{m}}$, for ceramics 3..10 $\mathrm{MPa}\sqrt{\mathrm{m}}$ [24] and 0.5..2 $\mathrm{MPa}\sqrt{\mathrm{m}}$ for epoxy-based polymers [48, 92, 117, 122].

The critical stress intensity factor respectively energy release rate is determined using com-

pact tension (CT) specimens [24, 48, 117, 122, 123]. The test is standardized for metals in ASTM 399 and for polymers in ASTM D5045-99. The size of the specimens are selected with respect to the latter-mentioned standard. The width W of the specimen is 20 mm and the thickness B is 4 mm. The critical stress intensity factor for the CT specimen is calculated according to

$$K_{\mathrm{Ic}} = \frac{F_{\mathrm{c}}}{B\sqrt{W}}\,\mathrm{f}(a/W) \tag{6.2}$$

where F_{c} defines the force at crack propagation, B the thickness of the specimen, W the width and a the crack length at crack propagation. The function $\mathrm{f}(a/W)$ can be found in [122]. The CT test is performed on a *Zwick* testing machine. A small v-shaped notch as pre-crack is introduced using a razor blade. For monitoring the crack length at propagation, an optical crack tracer is used [48]. The maximum stress in the flip chip interconnection is present at -40 °C. Therefore, the critical stress intensity factor for the underfills is determined at this temperature.

Because of the brittleness of the epoxy-based underfills, especially at -40 °C, reaching the critical force F_{c} leads to a catastrophical break of the CT specimen. Therefore, the optical crack tracer system is only used to determine the length of the pre-crack a.

The values for the fracture toughness of the materials used are listed in Tab. 6.1. UF2 shows the highest K_{Ic} in comparison to the other underfills. This is primarily explained by the high filling grade of UF2 [63, 92]. This consequently also applies to the low K_{Ic} of the unfilled epoxy NCA1.

Tab. 6.1: Critical stress intensity factors K_{Ic} for the underfills and NCAs at -40 °C, determined using standardized CT specimens; the critical ERR G_{Ic} is calculated using Eq.(4.27).

	UF1	UF2	NCA1	NCA2
K_{Ic} [MPa$\sqrt{\mathrm{m}}$]	1.13 ± 0.05	1.48 ± 0.18	0.8 ± 0.08	1.01 ± 0.09
G_{Ic} [N/m]	255 ± 0.5	346 ± 5	185 ± 2	144 ± 1

The relation of filler grade and fracture toughness for an epoxy system is shown in Fig. 6.1. The calculation is based on the rule of mixture, which is explained in detail in [63, 92]. Since the underfills and NCAs studied here have different epoxy matrices and particle size distributions, the results from Tab. 6.1 and Fig. 6.1 can only compared qualitatively.

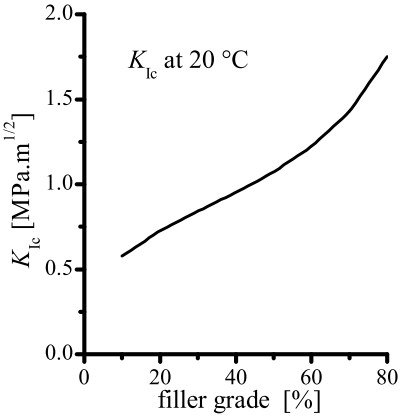


Fig. 6.1: Bulk fracture toughness as function of volume fraction of SiO_2 particles based on an empirical approach [63]; it can be seen that the higher the filler grade, the higher the fracture toughness; this explains the difference of the fracture toughness of the materials used in Tab. 6.1; the filler grade is shown in Tab. 5.2 and Tab. 5.3

6.2 Fracture Toughness of Interfacial Cracks

6.2.1 Overview of Interfacial Fracture Toughness

For a crack lying between two dissimilar materials with symmetric loading, asymmetry of the stress field arises due to the mismatch of the elastic material properties. Therefore, it is essential to study the interfacial toughness under mode-mixity conditions.

[118] studied the interfacial fracture toughness of a plexiglass/epoxy interface performed on a Brazil Nut specimen. The specimen enables toughness tests under different mixes of loading from pure Mode-I to pure Mode-II, by varying the orientation of the specimen, Fig. 6.2. The interfacial fracture toughness is a strong function of the mode-mixity: the higher the portion of tensile loading, the lower the interface toughness. For the test specimen used in Fig. 6.2, the critical ERR G_c for pure shear loading ($\psi = 90°$) is about four times higher than for pure tensile loading ($\psi = 0°$).

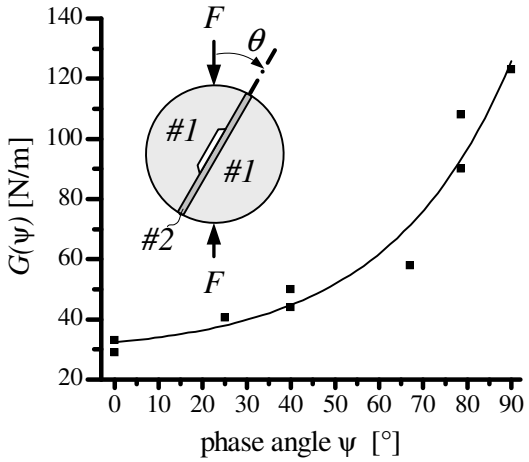


Fig. 6.2: Interface toughness function G_c for a plexiglass/epoxy interface obtained from a Brazil-nut-sandwich specimen [118]; phase angle ψ gives the ratio between Mode-II and Mode-I; $\psi = 0°$ for pure Mode-I and $\psi = 90°$ for pure Mode-II; rotation of specimen to negative values of angle ϕ result in negative values for the fracture toughness; the calculation of the mode-mixity ψ from the loading angle ϕ is performed numerically in [118]

In addition to the Brazil-nut-sandwich specimen, several types of specimens and loading conditions are studied [5, 14, 48, 53, 71], which came to the same dependency of the mode-mixity and the interfacial fracture toughness. Therefore, these results are essential for establishing design rules for SBB flip chip interconnections.

However, these tests have the disadvantage that the consumption of material for specimen preparation is high. Materials used for electronic packaging are costly and mostly available

only in small portions. Therefore, a method has to be developed which is cost-effective (low consumption of expensive underfill or NCA), fast to prepare and implement and also suitable for various interface topographies. Additionally, the test has to be suitable for characterization of environmental effects on the interface properties such as moisture and temperature.

The standardized button shear test fulfills the requirements above-stated. It is widely used for characterization of mold compounds on leadframes [105] or flip chip packages [99]. As can be deduced from the name of the method, it is used to obtain the interfacial shear adhesive strength of an interface. In actual assemblies, the interface experiences shear as well as tensile loading. The ratio of shear and tensile loading depends on the geometry, load condition and material combinations used. Therefore, the standard button shear test is extended in order to characterize the interface completely (shear and tensile loading). This can be achieved by varying the height of the shear tool. The greater the shearing height, the more the interface is loaded by Mode-I.

The failure of the button has to occur in the interface of the underfill and substrate. In order to force an interfacial crack, a pre-crack is fabricated [88, 107]. On one hand, the advantage is that the crack is constrained to occur in the interface. On the other hand, by having a pre-crack, the test can be studied by means of fracture mechanics. The advantages of using fracture mechanics approach lie in the FE-mesh independency and the translation of the obtained interface characterization on other geometries, but with the same material combinations. The load of the interface during the test is characterized by ERR and mode-mixity represented by the phase angle ψ. ERR and ψ are adequate to completely describe the interface strength for a given combination of underfill and substrate.

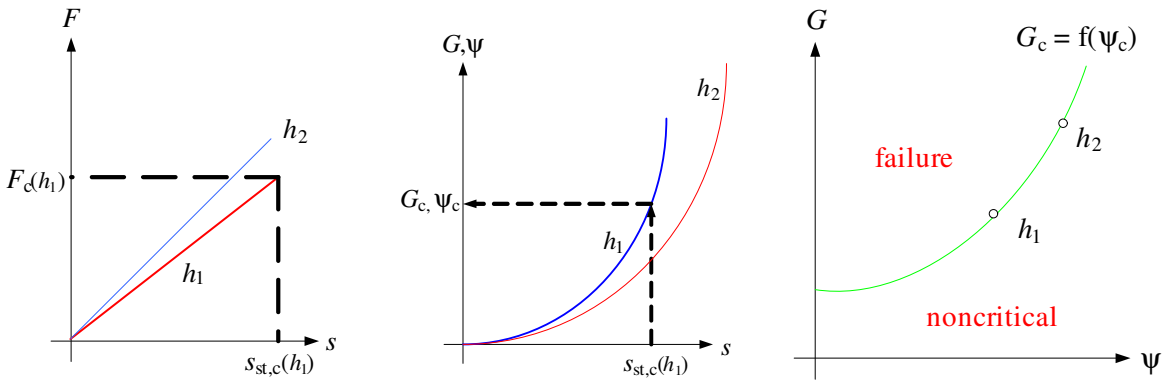
The objective of the study is to characterize the interface between LCP and the underfills and NCAs used. As stated earlier, the oxygen plasma treatment of the LCP influences the behavior of the surface. The plasma treatment cleans the surface from contamination, as well as building additional oxygen groups into the surface, which improves the adhesive strength. Therefore, the influence of the plasma treatment of the LCP on the ERR and ψ is also studied.

6.2.2 Work Flow of the Button Shear Test

The goal of obtaining the critical ERR as a function of ψ for the underfill/LCP interface is achieved by correlating the FE analysis with the experimentally-obtained results from the shear test:

1. Measurement of the critical force F_c and critical movement of the shear tool $s_{st,c}$ for the shearing height of h_1 (start of interfacial cracking), Fig. 6.3a
2. Performing a FE analysis of the test for the specific shearing height h_1 to establish the relation of the movement of the shear tool and the ERR and mode-mixity: $G = f(s_{st})$ and $\psi = f(s_{st})$
3. Correlation of experimentally and numerically obtained data: gathering G_c, ψ_c at $s_{st,c}$, Fig. 6.3b
4. Repetition for the next shearing heights h_2.., Fig. 6.3c, to obtain the complete interfacial fracture toughness

The critical load F_c, which leads to an interfacial crack, is measured experimentally with the button test. The present ERR G_c and phase angle ψ_c at interfacial cracking is obtained by FE analysis. By varying the shearing height, different ERRs and mode-mixities are achieved. This procedure is summarized in Fig. 6.3.



(a) Experiment: values F_c and s_c at failure of button on substrate

(b) FE analysis: G, ψ as function of s_{st}; taking $s_{st,c}$ from Fig. (a), G_c and corresponding ψ_c for h_1 are obtained

(c) Repeating step (a) and (b) for different shearing heights and plotting G_c over ψ_c

Fig. 6.3: Process flow for characterization interface toughness G_c of a material combination as function of phase angles ψ using a correlation of FE analysis and experimental results.

6.2.3 Experimental Setup and Testing

Sample Preparation of Button Test

As stated, the size of the button should be suitably small, in order to minimize the volume of underfill used. Standard buttons have a round cross-section, with a diameter of 4-12 mm [16, 99, 100, 105]. In order to ease demolding, the buttons are conically shaped [105, 88]. Studying the interfacial cracking of a cylindrically or conically shaped button using a fracture mechanics approach is quite complicated. This is due the fact that the width of the crack front changes during testing. As a result, the FE analysis must be performed three dimensionally. Additionally, modeling the outer part of the buttons is more cumbersome because of the round shape. To avoid these drawbacks and increase the efficiency of FE analysis, the button is set to be cuboidal. Fig. 6.4 shows a sketch of the sample for the button test. The PTFE strip with canvas is used to apply a pre-crack. The strip is self-adhesive on one side and not adherent on the other. The thickness of the PTFE strip is 80 μm.

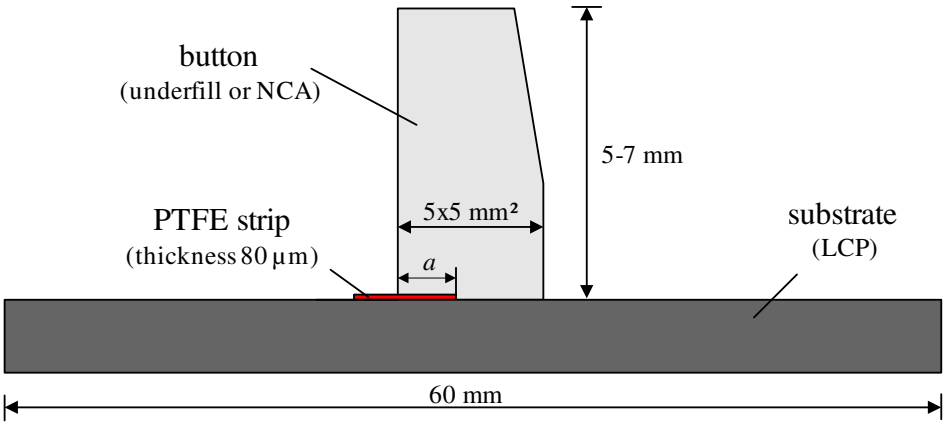
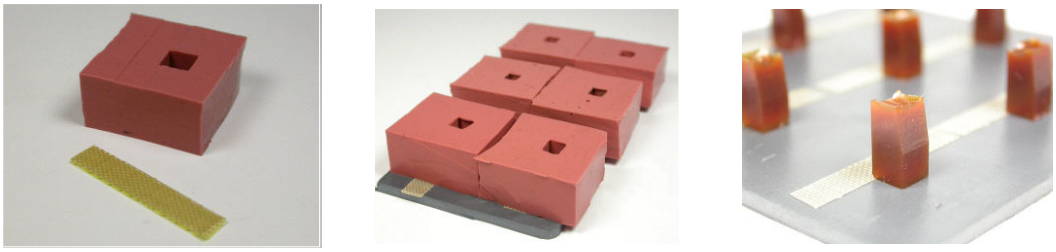


Fig. 6.4: Sketch of button composed of underfill or NCA on LCP substrate; PTFE strip with canvas is adhesive bonded to the substrate; upper side of strip is not adherent to adhesive; a is the length of pre-crack.

The steps in order to fabricate a button on LCP are displayed in Fig. 6.5. A molding form made out of silicone with a cut-out for the PTFE strip is shown in Fig. 6.5a. The cavity in the silicone form is $5 \times 5 \times 10$ mm^3. The cut-out has a thickness of 80 μm. The molding form is placed on the substrate, Fig. 6.5b. In order to increase efficiency of the manufacturing process, several forms are placed on a single substrate. Using a volume-controlled dispensing system, the cavities are filled with underfill or NCA. Because of the stickiness of the silicone, the underfill is restricted just to fill the cavity, so as not to lead to bleed-out. The curing of the adhesives is performed in an oven at the corresponding curing temperature. Fig. 6.5c shows the buttons after removal from the mold.



(a) Silicone mold form with out-cut for PTFE strip

(b) mold forms on LCP substrate ready for dispensing underfill

(c) buttons after curing of underfill/NCA

Fig. 6.5: Sample preparation of buttons made of underfill or NCA on LCP substrate; using PTFE strip as pre-crack

Fig. 6.6 shows a cross-section of the button after preparation. Due to the stickiness of the silicone, the flash is quite small. The cure shrinkage of the NCA leads to a reduction in volume.

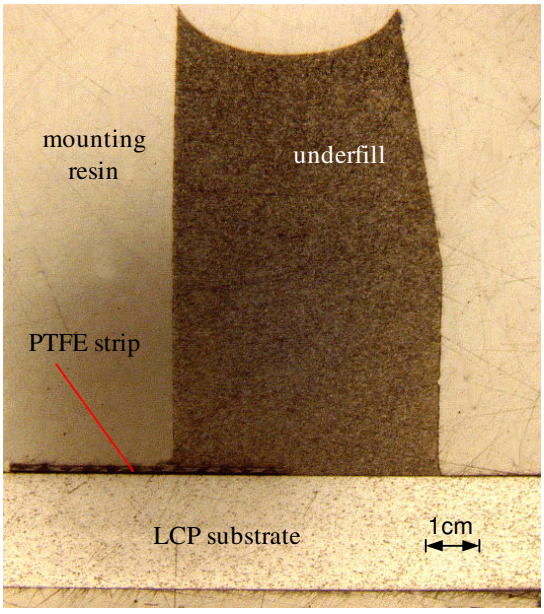


Fig. 6.6: Cross section of a button on LCP substrate; realization of pre-delamination by using a PTFE strip; no flash of NCA on LCP substrate

Procedure of Measurement of Adhesive Strength

The adhesive strength of the button on the LCP substrate is measured with the shear tester DAGE 4000. The LCP substrate is fixed with a bench vise at the outer part of the plate. Therefore, the substrate is free to bend in the area of the interface to the button. The buttons are placed directly in the middle of the substrate. The material and geometry properties of

the LCP substrate - thickness and flow direction during injection molding - influence the bending. This can be utilized to achieve different load cases of the crack.

In order to avoid torsional stress, a circular shear tool is used with a diameter of 6 mm.

Fig. 6.7 shows the applied force over movement of the shear tool s_{st}. The force and the movement are recorded once an initial force of 1 N is measured by the load cell. This ensures that only the movement which is based on the movement of the load cell is taken into account. It is worth noting that there is also a movement of the shear tool itself. This is due the fact that the shear tool is twisted in its' shaft. This movement is measured and subtracted. The measurement of a specific material combination is repeated at least five times.

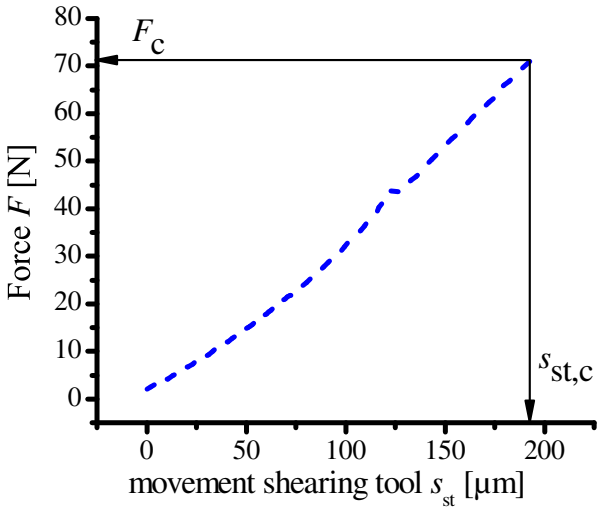
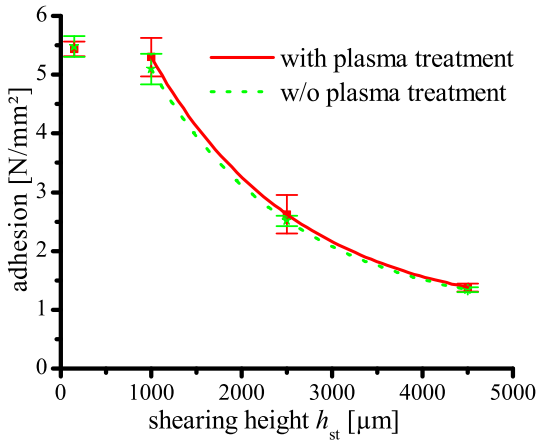


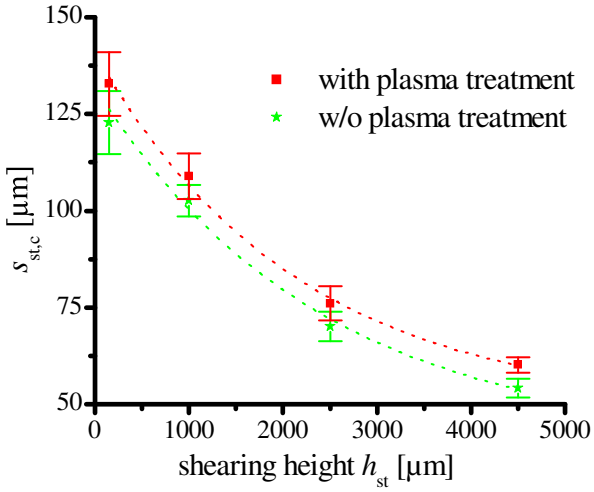
Fig. 6.7: Shear test: force F as function of movement of shear tool s_{st}; F_{c} and $s_{\mathrm{st,c}}$ mark the values at interfacial cracking

6.2.4 Measurements of Adhesive Strength NCA on LCP

Using the procedure described above, the adhesion strength for different shearing heights h_{st} can be obtained. Hereby, the critical force F_{c} is divided by the area of the button, Fig. 6.8a. The adhesion strength decays with increasing shearing height. It can be stated that the plasma treatment of the LCP surface only has minimal effect on the adhesion strength. For correlation of the experimentally obtained data to the numerically obtained energy release rate, the movement of the shear tool at fracture $s_{\mathrm{st,c}}$ is utilized. Plotting $s_{\mathrm{st,c}}$ as function of the shearing height h_{st}, Fig. 6.8b is obtained. For the adhesion, a decaying of $s_{\mathrm{st,c}}$ for increasing shearing heights is observed.



(a) Adhesion at fracture for different shearing heights h_{st}



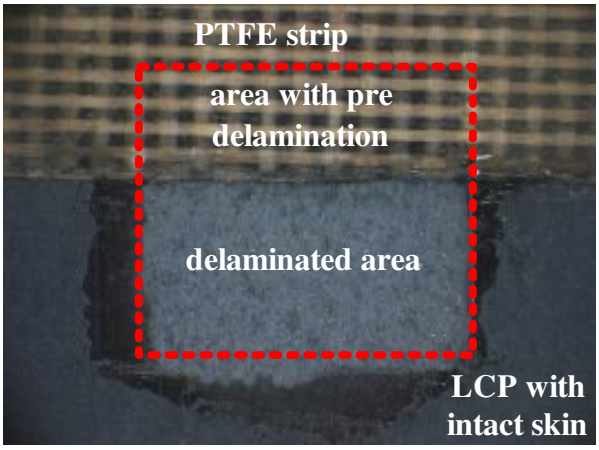
(b) Movement of shear tool $s_{st,c}$ at fracture for different shearing heights h_{st}

Fig. 6.8: Experimentally obtained movement of shear tool and adhesion for different shearing heights h_{st}; LCP with and without plasma treatment; plasma treatment shows negligible influence on adhesion.

Analyzing the fractured area of the substrate and the button, it can be stated that fracture does not occur directly in the interface between NCA and LCP. Fig. 6.9a shows the LCP substrate after button shear test. The fracture occurs in the skin of the LCP substrate, as can be seen by the difference in the color of the fractured area and the intact area. This can additionally be seen on the button, where on the delaminated area remainders of the skin are present, Fig. 6.9b. The fracture occurs independent of the surface treatment and underfill or NCA. Therefore, the correlation of experiment and numerical data in order to obtain energy release rate curves for different mode-mixities is only performed for NCA2.

Fig. 6.10a, and 6.10b sketch the fracture occurring in the interface respectively in the outer skin of the LCP. The cracking between the several layers in the LCP can also be seen as an interfacial cracking since it occurs between materials with two different properties. Since the outer layer is quite thin, with a thickness approximately 20 to 40 μm, and the outer layer sticks to the adhesive, interfacial fracture mechanics approach between the adhesive and the LCP[1] is assumed.

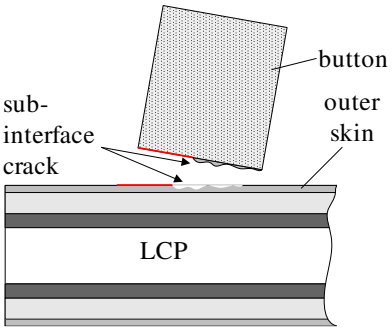
[1]Although LCP consists of several layers, refer to Fig. 5.2, the material is modeled as a homogenous material



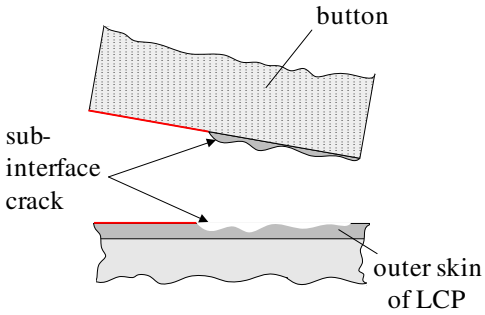
(a) LCP substrate; PTFE strip on substrate; delaminated area with partially removed skin of LCP

(b) Button with rests of skin of LCP substrated on delaminated area

Fig. 6.9: Fractured area from button shear test; fracture occurs partially within skin of LCP substrate, refer to structure of LCP in Fig. 5.2; fracture occurs in LCP skin independent of plasma treatment and used underfill or NCA



(a) Overview: LCP consists of several different layers, Fig. 5.2



(b) Detail: fracture occurs interfacial as well as in the skin of LCP

Fig. 6.10: Sketch of sub-interfacial fracture LCP/NCA; cracking occurs interfacial as well as in the LCP skin. The cracking between the several layers in the LCP can also be seen as an interfacial cracking since it occurs between materials with two different properties. Since the outer layer is quite thin, with a thickness approximately 20 to 40 μm, and the outer layer sticks to the adhesive after the shearing test, interfacial fracture mechanics approach between the adhesive and the LCP is assumed.

6.2.5 FE-Analysis to Calculate ERR and Mode-Mixity

FE-Implementation of Button Shear Test

From experimental analysis of the button shear test, the movement of the shear tool at fracture $s_{\mathrm{st,c}}$ for different shearing heights h_{st} is obtained. The Finite Element Analysis is used to link $s_{\mathrm{st,c}} = \mathrm{f}(h_{\mathrm{st}})$ with the critical energy release rate G_{c} and the present mode-mixity ψ.

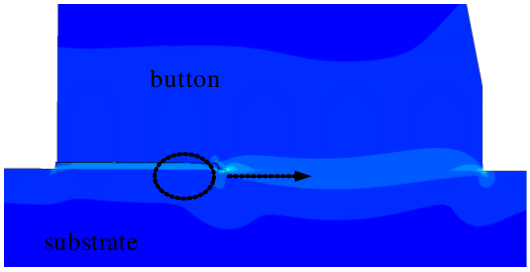
Because of the cuboided shape of the button, two-dimensional modeling is sufficient to describe the system. The geometry displayed in Fig. 6.4 is modeled in *ABAQUS*. As elements for meshing, generalized plane strain (CPEG) elements are used. The pre-crack is applied between the PTFE strip and the underfill. Applying the fracture mechanics approach, the crack is extended into the interface underfill and LCP substrate. Penetration is avoided using contact elements between the PTFE and the underfill.

In order to count for the residual stresses due to the assembly process, the cooling down from curing to room temperature is analyzed. For the sample preparation, the cured underfill button on LCP is cooled down to room temperature by natural convection. The ramp and time for cooling down influences the residual stresses. Therefore, the temperature field during cooling down is simulated in a temperature transient FE analysis. The simulation is compared with experimentally measured temperature data in the button. The heat-transfer coefficient h_{ht} is determined to be 15 $\frac{\mathrm{W}}{\mathrm{m^2 \cdot K}}$ which correlates with [42]. The temperature transient analysis is used as input for a stress analysis to calculate the residual stresses.

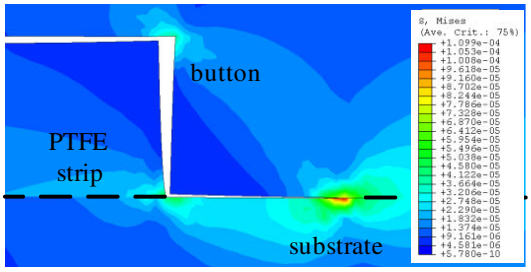
The material properties of LCP are used as described in the Chapter 5. For the simulation of the button test, linear-elastic material properties are used for the NCA. This is due the fact that the actual test is performed at room temperature where the relaxation is relatively slow. The material properties of the PTFE strip are regarded as from bulk PTFE. The shear tool is modeled as a non-deformable body. The movement of the shear tool is given as a boundary condition.

Influence of residual stresses from sample preparation

The buttons made of NCA2 are cured at 150 °C. Because of the thermal mismatch of the substrate, PTFE strip and adhesive, the interface already experiences stresses when cooling down from curing to room temperature. When modeling an additional delamination (other than the pre-delamination caused by the PTFE strip), and cooling down from curing temperature, that leads to a crack opening as shown in Fig. 6.11. Due to the higher CTE value of the PTFE strip, no contact between the underfill and the PTFE is reported.



(a) Sliding of underfill on the PTFE strip due to the thermal mismatch; avoiding penetration by using contact elements



(b) crack opening and stress concentration around crack tip; stresses are in 10^6 MPa

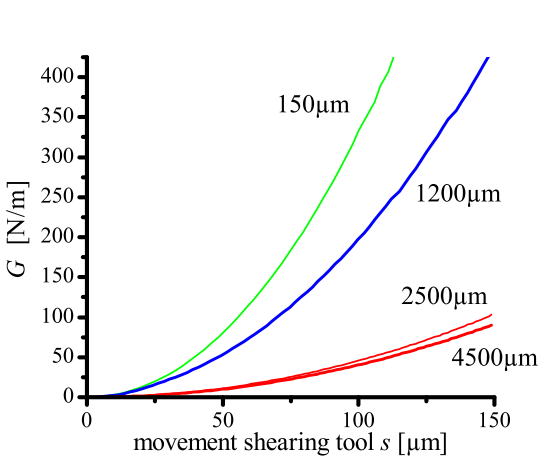
Fig. 6.11: Cooling down from curing to room temperature leads to crack opening and residual stresses; it can be seen that the residual stresses have to be taken into account when developing a test to quantify the adhesion strength; nevertheless, in the present work, for calculating the energy release rate and the mode-mixity, the residual stresses are not considered.

For the modeled button-shear specimen in Fig. 6.11, it is assumed that the pre-delamination occurred already at curing temperature. But for the actual performed button-shear-test, no pre-delamination other than the PTFE-strip is present. Therefore, no crack opening occurs when cooling down from curing temperature to room temperature. The actual delamination propagation only occurs when the shear-test is performed. Therefore, the residual stresses are not considered.

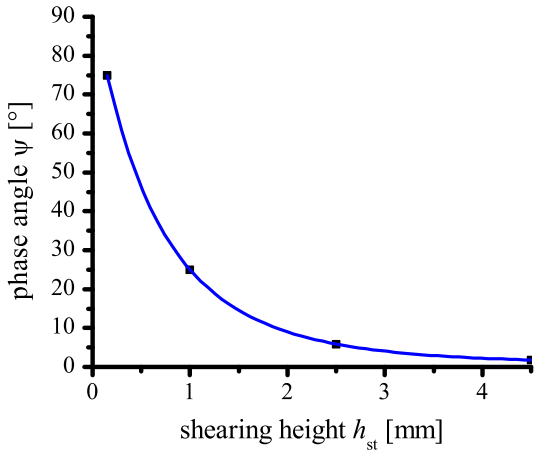
FE-Analysis of Button Shear Test

The button shear test is performed at room temperature. The modeling and the assumptions used are explained above. From the FE analysis, ERR G and phase angle ψ are determined as function of the movement of the shear tool s_{st}. The critical $s_{\mathrm{st,c}}$ is gathered experimentally.

Four different shearing heights h_{st} are used: 150, 1500, 2500 and 4500 μm. Fig. 6.12a shows the ERR as function of the movement of the shear tool s_{st} for the different shearing heights where 6.12b displays the phase angle ψ. It can be deduced that the shearing height has a significant influence on ERR and the mode-mixity. The lower the shearing height, the higher the ERR for the same movement of the tool. The influence of the shearing heights on ERR and ψ for heights higher than 2500 μm decreases significantly. Varying the shearing height between 150 and 4500 μm, the mode-mixity can be varied between 2° and 75°. It is possible to vary ψ almost in the same range as for the much more complex Brazil-Nut-sandwich specimen proposed by *Wang* and *Suo* [118].



(a) ERR G as function of movement of the shear tool s_{st} for different shearing heights h_{st}



(b) Phase angle ψ for different shearing heights; Mode-Mixity independent of s_{st} (not displayed))

Fig. 6.12: Finite Element Analysis of button shear test; calculation of ERR G and phase angle ψ for different shearing heights; the lower the shearing height, the bigger the phase angle and therefore the higher the portion of tension in the interface; it has to be noted that the residual stress due to the curing and cooling down from curing temperature to room temperature are not considered

6.2.6 Correlation to Obtain Interfacial Fracture Toughness

From the experimental button shear test, the critical movement of the shear tool $s_{\mathrm{st,c}}$ for different shearing heights h_{st} is obtained. On the other side, the Finite Element Analysis of the test is used to gather the energy release rate as well as the phase angle as a function of

the shearing height. By correlating the experimentally-obtained data with the FE analysis, the interfacial toughness of the interface NCA/LCP substrate can be described. The fracture occurs close to the interface of the NCA/LCP, but is not solely an interfacial crack.

From experimental testing, the adhesion of NCA on LCP is determined at four different shearing heights h_{st} =150, 1200, 2500 and 4500 μm. At these heights, $s_{st,c}$ is used to determine the critical energy release rate G_c from Fig. 6.12a. As stated, the phase angle ψ is constant over the movement of the shear tool, but it is a function of the shearing height as shown in Fig. 6.12b. Using these correlations, the interfacial toughness curve can be drawn, Fig. 6.13. As stated for the adhesion strength in Fig. 6.8a, the plasma treatment of the LCP surface has little influence on the interfacial fracture toughness. This is due to the fact that the fracture occurs within the skin of the LCP.

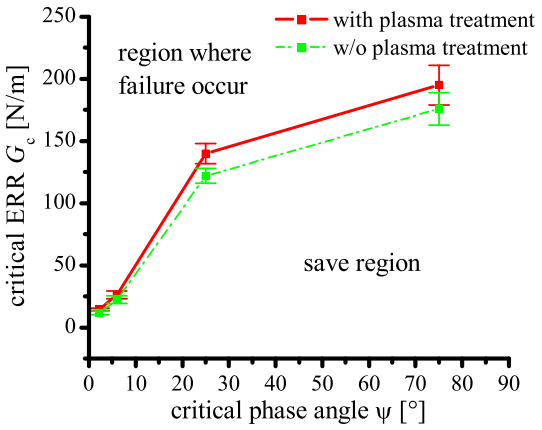


Fig. 6.13: Interfacial fracture toughness for NCA on LCP for different loadings; fracture occurs within LCP skin and therefore expected curve is not applicable; interfacial fracture toughness curves state that shear loading leads to much higher critical energy release rates than pure tension loading.

Chapter 7

FE-Modeling, Stress Analysis and Establishing Failure Criteria

7.1 FE-modeling of Flip Chip Interconnection

7.1.1 Parameterized FE-Modeling

The FE model of a stud bump bonding flip chip interconnection is parameterized in Finite-Element-Method (FEM) software *ABAQUS*. This has the advantage that geometry changes can be performed quickly. Moreover, the parameterized model can be used for automatic optimization of the geometry if connected with an optimization tool. The geometric parameters are displayed in Fig. 7.1. The stud bumps are not modeled because they have negligible affect on the stresses in the fillet region. The affect is discussed later.

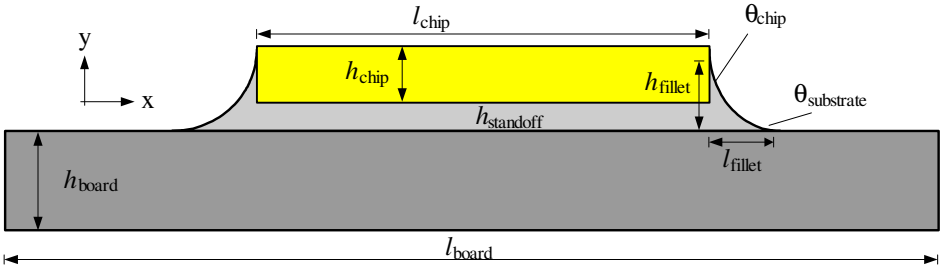


Fig. 7.1: Parameterized FE model of flip chip interconnection; invoking *Python* scripting for *ABAQUS*, the geometry parameters, displayed, can be varied.

Methods are available to calculate the fillet shape by measuring the contact angle of the underfill on the substrate and chip edge, as well the surface tension. These methods lead to a formulation of the angles in the uncured state of the underfill. Because cure shrinkage leads to

a different shape, physically-based modeling of the cured underfill fillet is difficult. Therefore, a mathematical approach is used to model the fillet shape. The method to implement fracture mechanics into Finite Element modeling, the Virtual Crack Closure Technique, requires a mesh with quadratic elements around the crack tip. Therefore, it is not possible to use spline representation of the outer line to the fillet. The line has to be built up using straight lines. In order to give a smooth shape to the fillet, more than 50 single lines are used to model the fillet. The mathematical formulation for the fillet is based on an exponential approach in the form of

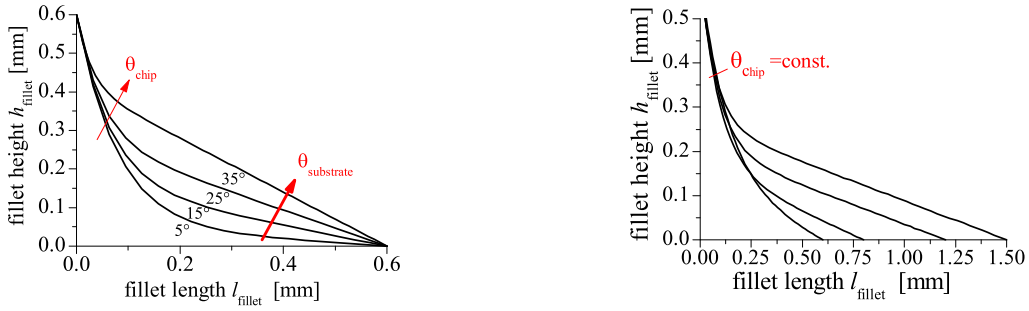
$$y(x) = A_1\, e^{-A_2 x} + A_3 x + A_4 \tag{7.1}$$

with four constants. x and y are the coordinates of the starting and ending points of the several lines. The coordinate system is shown in Fig. 7.1. The four constants A_1 to A_4 are determined by applying the following boundary conditions

$$y(0) = h_{\text{fillet}} \qquad y(l_{\text{fillet}}) = 0 \qquad y'(0) = \tan\theta_{\text{substrate}} \qquad y'(0) = \tan\theta_{\text{chip}} \tag{7.2}$$

where θ_{chip} and $\theta_{\text{substrate}}$ are the wetting angle of the cured underfill with respect to the chip and substrate, respectively. h_{fillet} and l_{fillet} are the height and length of fillet as show in Fig. 7.1. The four parameters are obtained in compliance with Newton's method.

Fig. 7.2 shows different fillet shapes calculated on the described method in Eq.(7.1).

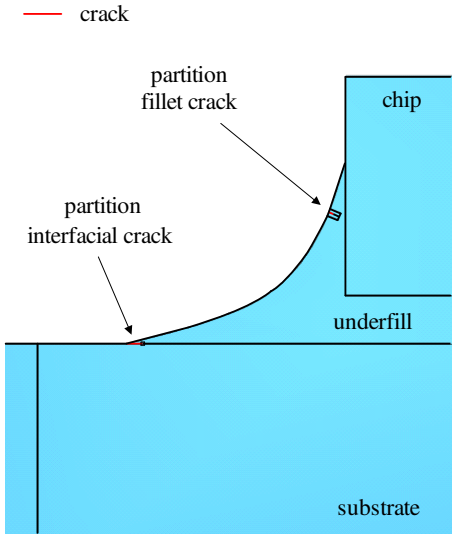


(a) $h_{\text{fillet}}, l_{\text{fillet}} = \text{const.}$ (b) $\theta_{\text{chip}} = \text{const.}$

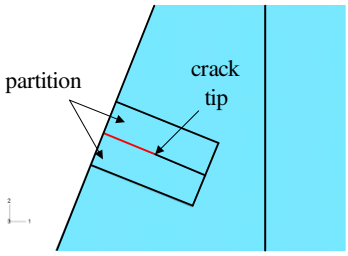
Fig. 7.2: Parameterized modeling of fillet by single lines using exponential mathematical approach; fillet height and length as well as wetting angles underfill and chip respectively substrate can be almost independently changed.

7.1.2 VCCT Implementation and Calculation of Energy Release Rate

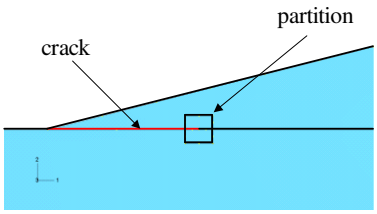
The Virtual Crack Closure Technique (VCCT) is utilized to apply fracture mechanics to FE. Using VCCT, the energy release rate ERR for an existing crack can be calculated. Hereby, the method is capable of determining ERR for a crack lying in bulk material, as well as a crack between two materials. The calculation procedure is explained in Section 4.3. VCCT requires quadratic first or second order elements [38, 94]. The capability of triangular elements to fill arbitrary shapes, e.g. the fillet, is their advantage. Therefore, hybrid meshing of the flip chip interconnection is used. Partitions around the crack tip are placed to apply quadratic elements Fig. 7.3a-c.



(a) FE modeling of fillet; partitions are placed at the fillet and interface LCP/underfill



(b) bulk crack in fillet



(c) interfacial crack

Fig. 7.3: FE implementation of the Virtual Crack Closure Technique (VCCT) by creating partitions; the VCCT is used to obtain the stress intensity factor K_{I} for a bulk crack and the Energy Release Rate G as well as the mode-mixity ψ for an interfacial crack.

The crack in the regularly structured mesh in a partition is applied by doubling the corresponding nodes [38, 94]. The crack opening after loading can be seen in Fig. 7.4.

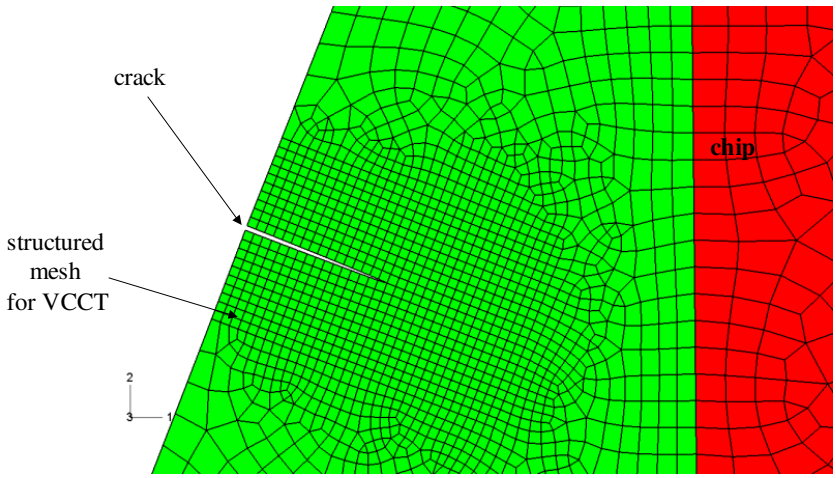
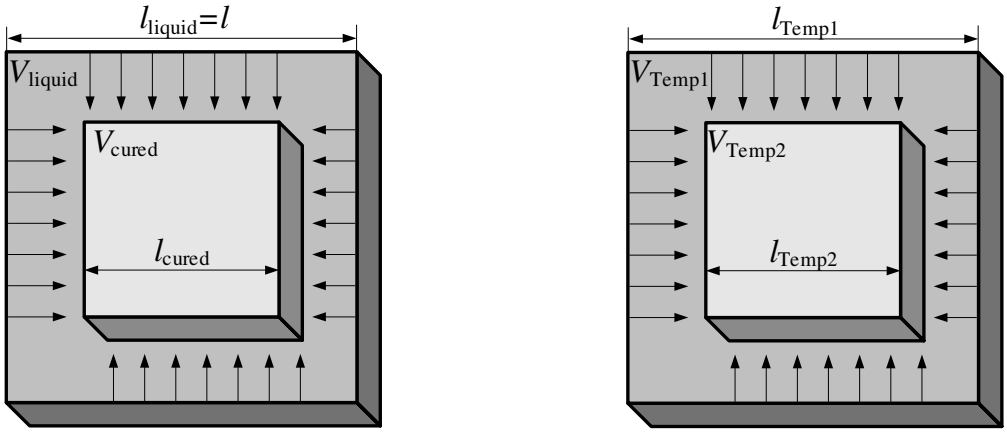


Fig. 7.4: Finite Element mesh chosen to be appropriate for the implementation of VCCT; quadratic elements around the crack tip within a geometric partition are required; hybrid meshing around partition to also be able to create a mesh for non-rectangular structures; crack implementation by doubling the corresponding nodes; here shown for a crack in the fillet

7.1.3 Assessment of Curing Shrinkage

The curing of the underfills and NCAs are performed at an elevated temperature, e.g. 150 °C for UF1. The shrinkage caused by chemical conversion already leads to residual stresses at curing temperature. The volume change during curing of the adhesives is measured by volume dilatometry and listed in Tab. 5.2 and Tab. 5.3.

The volume shrinkage $\varepsilon_{\text{curing}}$ can, among others methods, be implemented by using the analogy of chemical curing shrinkage and compression induced by an artificial temperature change ΔT of the polymer [1], Fig. 7.5. During curing process, the density increases, therefore the volume decreases. Since the underfills and NCAs used are filled with spherical fillers, the cure shrinkage is isotropic.



(a) Volume reduction from V_{liquid} to V_{cured} during curing process; isotropic shrinkage assumed

(b) Volume reduction caused by temperature change ΔT with $T_1 > T_2$ and $\alpha > 0$

Fig. 7.5: Invoking the analogy to model the curing process: the cure shrinkage leads to a volume reduction, and so does a cooling from T_1 to T_2 [7]

Using the analogy, cooling the polymer also results in a decreasing volume [7]. The volume shrinkage S_{volume} can be related to an one-dimensional compression by

$$\begin{aligned} S_{\text{volume}} &= \frac{V_{\text{liquid}} - V_{\text{cured}}}{V_{\text{liquid}}} = 1 - \frac{V_{\text{cured}}}{V_{\text{liquid}}} = 1 - \frac{V_{\text{liquid}} - \Delta V}{V_{\text{liquid}}} = 1 - \frac{(l-\Delta l)^3}{l^3} \\ &\approx 1 - \frac{l^3 - 3l^2\Delta l}{l^3} = 3\frac{\Delta l}{l} \quad \text{with} \quad \Delta l^2, \Delta l^3 \approx 0 \end{aligned} \tag{7.3}$$

where $V_{\text{liquid}} = l^3$ is the volume of a cube in the uncured state, $V_{\text{cured}} = V_{\text{liquid}} - \Delta V$ the volume in the cured state. Higher order components are neglected.

[1] This method can be similar used to estimate the influence of swelling caused by humidity absorption [55].

The linear compression induced by a temperature change is defined by

$$\Delta l = l\,\Delta T\,\alpha \rightarrow \Delta T = \frac{\Delta l}{l}\,\frac{1}{\alpha} \tag{7.4}$$

with α as the CTE value of the cured material at curing temperature. Using the analogy curing shrinkage / thermal compression and replacing the expression $\Delta l/l$ in Eq.(7.4) by Eq.(7.3), the artificial temperature change needed to account for the cure shrinkage can be obtained

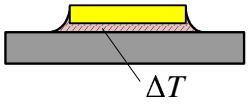
$$\Delta T = \frac{\Delta l}{l}\,\frac{1}{\alpha} = \frac{S_{\text{volume}}}{3}\,\frac{1}{\alpha}. \tag{7.5}$$

Applying this method to model cure shrinkage of underfill UF2, which has a cure shrinkage S_{volume} of 0.4 % and a coefficient of thermal expansion of 110 pmm/K at curing temperature, the artificial temperature change is around $\Delta T = 12.1$ °C. The initial temperatures for the other UFs and NCA are shown in Tab. 7.1.

Tab. 7.1: Implementation of cure shrinkage in the FE analysis; temperature changes ΔT used for the UFs and NCAs based on Eq.(7.5); the values of the cure shrinkage are taken from Tab. 5.2 and Tab. 5.3

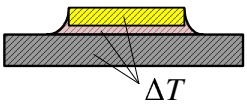
Adhesive	**NCA1**	**NCA2**	**UF1**	**UF2**
ΔT [°C]	37.5	8.5	45.5	12.1
cure shrinkage S_{volume}[%]	1.8	0.3	1.8	0.4

Fig. 7.6 shows the implementation of the cure shrinkage in the FE analysis. The initial temperature for the reactive material is defined as $T = T_{\text{cure}} + \Delta T$, where the non-reactive material has T_{cure}. During Step 1 - calculation of impact due to curing process - the UF or NCA is cooled down to T_{cure}. No cure-dependent Young's modulus for the polymers is used. The corresponding Young's modulus at curing temperature is used for the reactive materials. In the next steps, the flip chip interconnection is cooled to the upper dwell temperature $T = T_{\text{high}} = 150$ °C and afterwards to the lower dwell temperature of -40 °C.



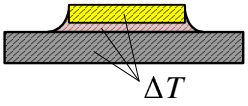
	Initial condition	Step 1: cured state
Reactive material (NCA, UF)	$T=T_{\text{cure}} + \Delta T$	$T=T_{\text{cure}}$
Non-reactive material (IC, board)	$T=T_{\text{cure}}$	$T=T_{\text{cure}}$

(a) Initial condition → Step 1: Cooling down the reactive material (UF, NCA) from artifical temperature $T = T_{\text{cure}} + \Delta T$ to T_{cure}; keeping the other materials at curing temperature



	Step 1: cured state	Step 2: T_{high}
Reactive material (NCA, UF)	$T=T_{\text{cure}}$	$T=T_{\text{high}} = 150$ °C
Non-reactive material (IC, board)	$T=T_{\text{cure}}$	$T=T_{\text{high}} = 150$ °C

(b) Step 1 → Step 2: Cooling down from T_{cure} to $T_{\text{low}} = 150$ °C



	Step 2: T_{high}	Step 3: T_{low}
Reactive material (NCA, UF)	$T=T_{\text{high}} = 150$ °C	$T=T_{\text{low}} = -40$ °C
Non-reactive material (IC, board)	$T=T_{\text{high}} = 150$ °C	$T=T_{\text{low}} = -40$ °C

(c) Step 2 → Step 3: Cooling down from $T_{\text{high}} = 150$ °C to $T_{\text{low}} = -40$ °C

Fig. 7.6: Process flow to implement cure shrinkage estimation in the FE analysis; using different initial conditions for the reactive material and non-reactive material

In order to assess the influence of the cure shrinkage, the warpage of a flip chip interconnection is calculated. For this simulation, it is essential to also include the stud bumps in the FE model. At the same time, the warpage caused by cooling down from curing temperature to room temperature is considered. Hereby, stress, and therefore warpage-free condition, is

assumed to be at curing temperature. As shown in Fig. 7.7, the contribution of the curing process leads to concave warpage of the chip. This can be explained by the restricted contraction due the stud bumps. Nevertheless, the value of the warpage is negligible in comparison to the warpage caused by the CTE-mismatch in the cured state. Moreover, the warpage due to curing is overestimated, because of the assumption that during curing process the Young's modulus is conversion independent. It is assumed that the Young's modulus already has its full value at the uncured state. Therefore, the influence of the curing can be neglected.

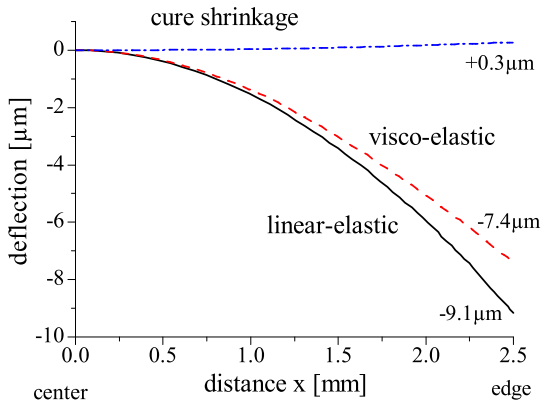


Fig. 7.7: Assessment of cure shrinkage shown for warpage of flip chip interconnection; comparison of deflection caused by cure shrinkage and cooling down from curing to room temperature; for the latter, stress free condition assumed at curing temperature; influence of cure shrinkage on warpage is negligible and therefore neglected

7.1.4 Material Models and Applied Load

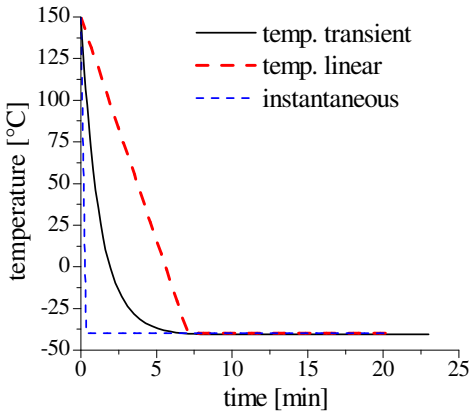
A list of the material models used is shown in Tab. 5.1. As stated, the underfill and NCAs are modeled with a visco-elastic material behavior.

In the experimental reliability testing of the flip chip interconnections, a thermal-cyclic loading is applied. The cooling time depends on the performance of the thermal-cycling chamber, as well as on the thermal mass of the specimens and oven itself.

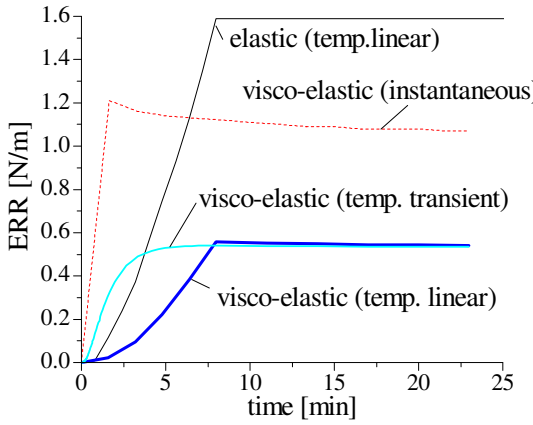
In this work, the cooling process from curing temperature to -40 °C is performed. The curing temperature of the assemblies using underfills is 150 °C. Whereas for the NCA assemblies, the curing temperature and therefore the stress free condition is at 180 °C.

The transient temperature profile used in the simulation is obtained based on the measured temperature profile in the actual thermal-cycling chamber. For the simulation of the temperature field, the flip chip interconnection is modeled three dimensionally. The coefficient of heat transfer from the materials to air is obtained by iterative adjustment of the transient simulation to the experimental data of the temperature profile.

The heat transfer coefficient of 60 $\frac{W}{m^2K}$ is found to provide the best results. For forced heat transfer the value lies within the range given by [42]. The transient temperature profile is shown in Fig. 7.8a. For the simulation, the temperature change from 150 °C to -40 °C is additionally linearly incremented by using the time for cooling from transient simulation. The third curve gives the temperature profile for an instantaneously applied temperature.



(a) Temperature profile for different assumptions; to obtain transient temperature profile, a thermal analysis is performed before stress analysis



(b) ERR for a fillet crack for different temperature profiles and material behavior of underfill; significant influence of assumed material behavior (linear elastic, visco-elastic)

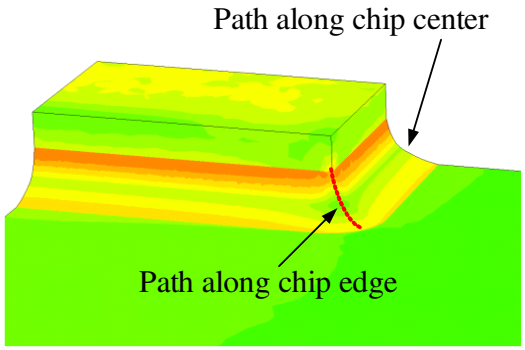
Fig. 7.8: Impact of temperature application and material behavior for the calculation of a fillet crack; instantaneous application for linear-elastic and visco-elastic leads to an overestimation of ERR in the crack; ERR for transient and linearly applied temperature change leads to same ERR; therefore, it is sufficient to model the cooling down linearly, although it shows an exponentially decreasing function; modeling the temperature change linearly reduces the number of required simulations and and therefore the computational effort.

The impact of the temperature profile used on an arbitrary fillet crack is displayed in Fig. 7.8b. The temperature profiles from Fig. 7.8a are used. Additionally, the impact of the material behavior of the underfill is shown. It can be clearly seen that for modeling the underfill with a linear-elastic material behavior, the ERR is overestimated (Fig. 7.8b "elastic (temp.linear)"). Moreover, the utilization of visco-elastic material behavior in combination with an instantaneous temperature application also leads to an overestimation ("visco-elastic (instantaneous)"). The results for a linear and transient application of the temperature in combination with visco-elastic material behavior lead to the same result ("visco-elastic (temp.transient)" and "visco-elastic (temp.linear)"). Therefore, it is sufficient to use linear instrumentation of the temperature.

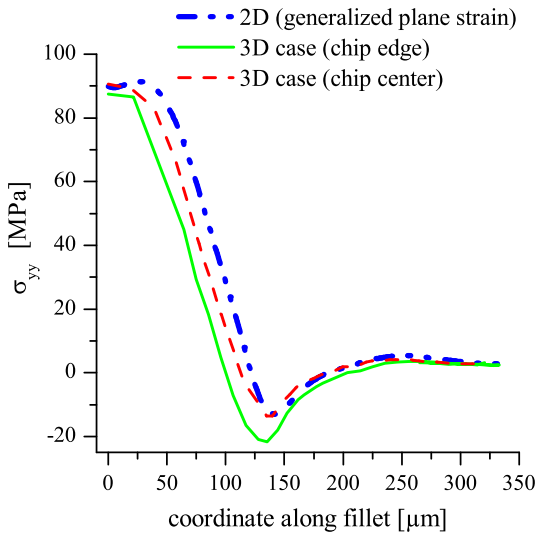
7.2 Stress Analysis of SBB Flip Chip Interconnection

7.2.1 Stress Analysis Without Crack

A stress analysis of the fillet is performed to identify the critical locations for crack initiation. Simplifying the flip chip interconnection to a two-dimensional model (2D) reduces modeling effort and computation time significantly. This is especially needed when the influence of multiple parameters has to be considered. Nevertheless, a simplification is only valid when the stress distributions are similar for the two-dimensional and three-dimensional (3D) model. The distribution of the stress component σ_{yy} along the fillet for a two- and three-dimensional model are displayed in Fig. 7.9b. The stresses along the fillet at the chip corner and chip center are obtained for the three-dimensional model as well as for the two-dimensional model. It can be stated that the distribution, as well as the absolute values are in the same range for the 2D and 3D model. Therefore, the flip chip assembly is represented by a 2D Finite Element model.



(a) 3D quarter model of the flip chip interconnection; the stresses along the fillet at the chip edge and center are extracted



(b) Obtaining the stress component σ_{yy} along the fillet using a 2D and 3D Finite Element Analysis

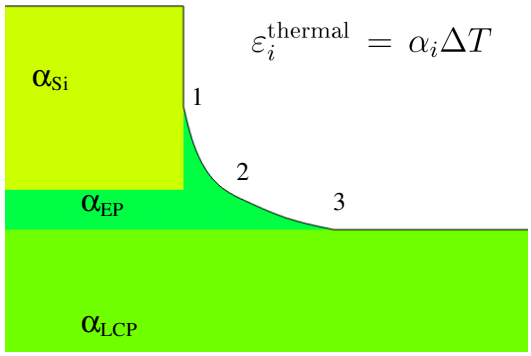
Fig. 7.9: Comparison two- and three-dimensional Finite Element stress analysis of the fillet; 2D FE analysis leads to a similar stress distribution along the fillet; the critical regions – lower and upper part of the fillet – are also displayed in the simplified 2D case; since the computational effort for the three-dimensional is much higher and not feasible for parametric studies, only two-dimensional Finite Element analysis is performed

In order to identify the critical locations along the fillet, and to explain the distinct distribution of the stress in the fillet, a stress and strain analysis of the fillet is performed.

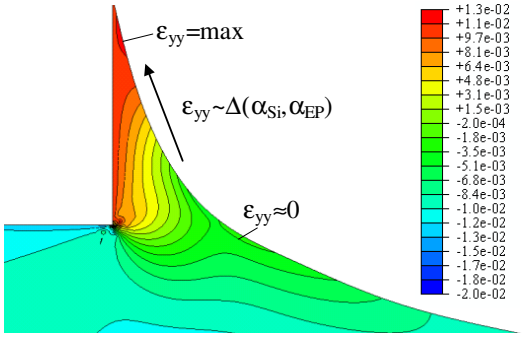
The overall strain $\varepsilon^{\text{total}}$ is decomposed into a thermal $\varepsilon^{\text{thermal}}$ and an elastic part $\varepsilon^{\text{elastic}}$. The thermal strain accounts for the thermal expansion (or contraction) due to temperature change

$$\varepsilon_i^{\text{thermal}} = \alpha_i \Delta T \quad \text{with } i = \text{Si,LCP,epoxy.} \tag{7.6}$$

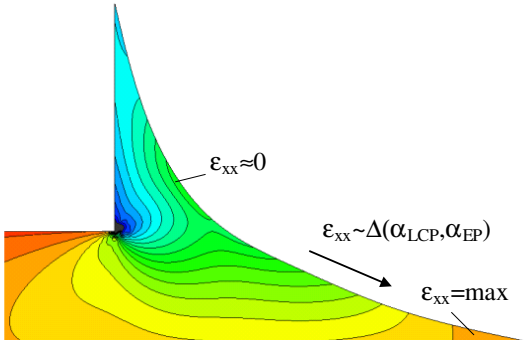
The thermal strain $\varepsilon^{\text{thermal}}$ on the different components is shown in Fig. 7.10a.



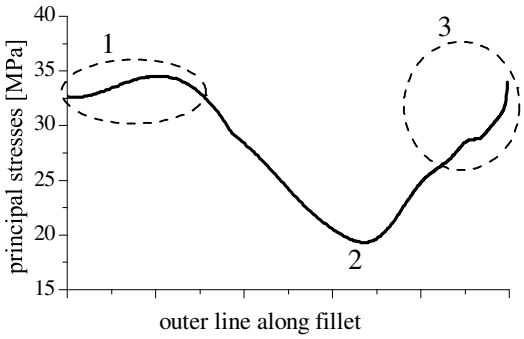
(a) $\varepsilon_x^{\text{thermal}}$: is dependent only on $\Delta T \alpha_i$, represents the free contraction ($\Delta T < 0, \alpha_i > 0$)



(b) $\varepsilon_{yy}^{\text{elastic}}$: dominated by CTE-mismatch of Si/epoxy; legend is valid for Fig. 7.10a-c



(c) $\varepsilon_{xx}^{\text{elastic}}$: dominated by CTE-mismatch of LCP/epoxy; also by CTE-mismatch passivation/EP



(d) First principal stresses σ^1 along the fillet: high stresses at location 1,3; vanishing stresses at point 2

Fig. 7.10: Strain, stress analysis of fillet when exposed to cooling down ($\Delta T < 0$); high strains in fillet in region of interface chip/underfill and substrate/underfill; vanishing strain where thermal contraction is not restricted; using principal stresses σ^1 to account for the maximum stresses, regardless of element orientation

The elastic strain results from restriction of the free thermal expansion. The restriction is mainly caused by boundary conditions like fixation or material interfaces. For a flip chip interconnection, these are the interface chip/underfill and substrate/underfill. The mismatch in CTE of silicon die and the epoxy-based underfill dominates the elastic strain in y-direction $\varepsilon_{yy}^{\text{elastic}}$, Fig. 7.10b. Whereas the difference in the CTE of the substrate and the underfill contributes to $\varepsilon_{xx}^{\text{elastic}}$ which is displayed in Fig. 7.10c. It is worth mentioning that the interface passivation/underfill with its mismatch also leads to high strains in x-direction. Since no imperfections are present, this mismatch is not considered to be critical. In the part of the

fillet where both interfaces are separated by a certain distance, the epoxy is almost free to contract. Therefore, the elastic strain decreases rapidly[2]. The total strain is therefore calculated as

$$\varepsilon^{\text{total}} = \varepsilon^{\text{thermal}} + \varepsilon^{\text{elastic}}. \tag{7.7}$$

The stress is calculated by invoking Hooke's Law

$$\sigma = E\,\varepsilon^{\text{elastic}}. \tag{7.8}$$

The critical stress components which lead to crack initialization in brittle material are the first principle stresses σ_1 [13]. Therefore, the first principle stresses are used to identify critical locations along the fillet. This is shown in Fig. 7.10d. The principle stresses show two locations with high stress concentration: the area at the upper part of the fillet (Fig. 7.10d "Pos.1") and the lower end of the fillet ("Pos.3"). As stated above, these two locations also show high strain components, refer to Fig. 7.10b and c. Since the strain at ("Pos.2") is very small, only very low stress is present at this position. Therefore, it is less likely that a crack initiates at this position.

7.2.2 Assessment of Stress Concentration at Upper Part of Fillet

At ("Pos.1") in Fig. 7.10d high stresses are present. The occurrence of high stresses is due to the bi-material face between the underfill and vertical chip edge. The exact position of the maximum stress is dependent on the fillet shape. In Fig. 7.11 the influence of the wetting angle θ_{chip} is studied. It shows that the maximum of the stresses shift closer to the vertical chip edge when the wetting angle is increased.

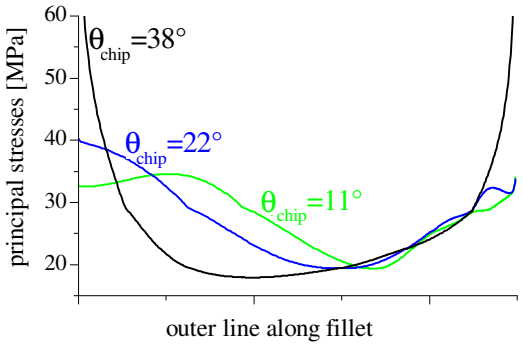
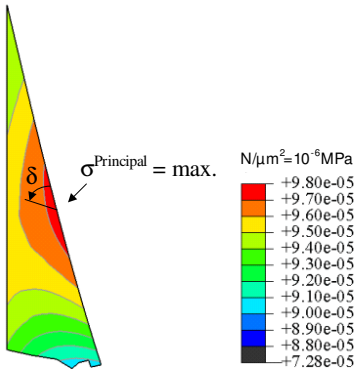


Fig. 7.11: Influence of wetting angle θ_{chip} on the position of the maximum principal stress σ_1 in the upper part of the fillet; the higher the angle, the closer the maximum stresses to the vertical chip edge

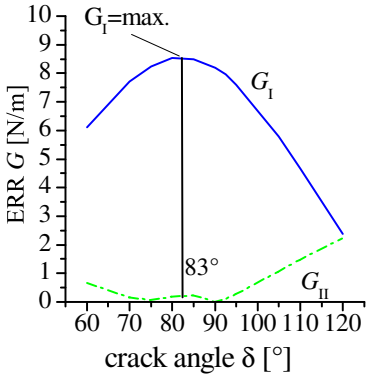
[2] e.g.: for a bar which is fixed on both sides and exposed to temperature change, the total axial strain is zero. Therefore, the magnitude of the elastic strain equals the thermal strain. The stresses resulting from the restricted expansion are calculated by the Young's modulus and the elastic strain (Hooke's Law).

To apply the physics-of-failure approach, the failure mechanism must be known. For the upper part of the fillet, it can be either a bulk crack in the underfill or a delamination between the vertical chip edge and the underfill. Moreover, the critical value for both kinds of failure mechanism for all the materials respectively combinations have to be known. The interfacial toughness between the underfill and the vertical chip edge is not known. But it can be assumed that in the absence of media influence, for example humidity, the interfacial fracture toughness is fairly high. Therefore, it is assumed that the crack initialization occurs in the underfill.

For brittle material such as epoxy, fatigue and resulting crack initiation occur at position of maximum principle stresses σ_1. Crack initiation is caused by damage mechanisms in the epoxy respectively in the interface between the filler particles and epoxy. Due to the lack of damage models for the materials used, as well as missing experimental data, the crack initiation process is not taken into account. For the simulation, it is assumed that thermal cycling already led to crack initiation. The location of crack occurrence is identified using the position of maximum tensile stress σ_1 along the fillet, Fig. 7.12a.



(a) $\sigma^{\text{principal}}$ at fillet; modeling crack with δ to the outer line



(b) crack criterion $G_{\text{I}} = \max.$ is used $\rightarrow \delta = 83°$; since $G_{\text{I}} \ll G_{\text{Ic}}$ (G_{Ic}=144 .. 346N/m for the used underfills and NCAs), only undercritical crack propagation is possible

Fig. 7.12: Determination of σ_1 by thermo-mechanical analysis without crack; crack modeling at this point; crack modeling perpendicular to the outer line of the fillet

A crack with an initial size of 5 μm is modeled. The angle of the pre-crack is obtained by calculation of the energy release rate. The ERR for Mode-I G_{I} and Mode-II G_{II} are calculated. The Mode-II components for angles δ between 70° and 95° are smaller than 3 % of $G_{\text{I,max}}$. G_{I} shows a clear maximum at 83°. Therefore, the pre-crack is modeled with an angle of 83°, Fig. 7.12b.

The existing crack in the fillet is exposed to further thermal cycling. The overcritical stress intensity factor K_{Ic} and overcritical ERR G_{Ic} for the underfills used are listed in Tab. 6.1. These values are obtained applying a mechanical force until crack propagation occurs. The test is performed at -40 °C. The values lie between 0.8 and 1.48 MPa$\sqrt{\mathrm{m}}$ for K_{Ic} and 144 and 346 N/m for G_{Ic}. Comparing the overcritical values with the existing values from the FE analysis, displayed in Fig. 7.12b, it can be stated that crack propagation is not overcritical in the fillet, i.e. one thermal cycle does not lead to instable crack propagation. Crack propagation can only be undercritical since

$$K_{\mathrm{I}} \ll K_{\mathrm{Ic}} \quad G_{\mathrm{I}} \ll G_{\mathrm{Ic}}. \tag{7.9}$$

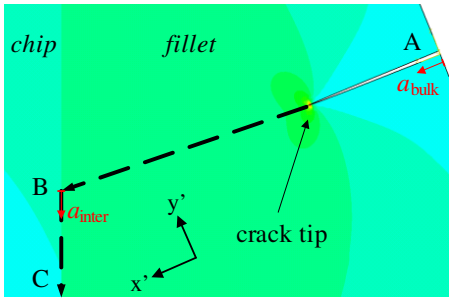
The undercritical crack growth, also defined as fatigue crack growth, Fig. 3.4, can be described by the Paris Erdogan relation

$$\frac{\mathrm{d}a}{\mathrm{d}N} \sim (\Delta G)^n \tag{7.10}$$

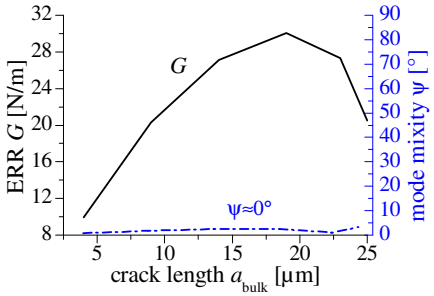
where a is the crack length, N number of cycles and n the Paris exponent [72]. Since no experimental values are available for the polymers used, fatigue crack growth is not studied.

Fig. 7.13a shows a modeled bulk crack with a length a_{bulk}, points "A" to "B". The external loading remains constant for an increasing number of thermal cycles. But the energy release rate G_{I} increases with increasing crack length a_{bulk}, Fig. 7.13b. This leads to an accelerated crack propagation. The crack propagation slows for crack lengths $a_{\mathrm{bulk}} > 20$ μm. This is due to the fact that the crack approaches the vertical chip edge. Nevertheless, it can be assumed that the crack propagates until the edge is reached.

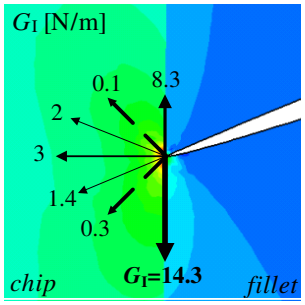
At the vertical chip edge, point "B" in Fig. 7.13a, the crack can either be deflected and lead to an interfacial cracking between underfill and vertical chip edge or the bulk crack in the fillet can lead to horizontal die cracking. Therefore, the energy release rate for different paths of crack propagation is calculated, Fig. 7.13c. Hereby, the critical energy release rates for bulk cracking in silicon have to be compared to the present ERR at point "C". From the critical stress intensity factor for Mode-I $K_{\mathrm{I,c}} = 0.83$ MPa$\sqrt{\mathrm{m}}$ of silicon, the critical energy release rate is calculated to be $G_{\mathrm{I,c}} = 5.4$ N/m [30, 58, 101, 116]. The critical energy release rate is almost twice as high as the present value of about $G = 3$ N/m, Fig. 7.13c. Additionally, the interfacial fracture toughness of underfill on the silicon edge has to be taken into account. The interfacial toughness depends on various parameters, like roughness of the silicon, load case etc. No values are available. Therefore, no estimation about crack propagation – bulk cracking of the silicon die or delamination propagation along the interface silicon and underfill – can be done based on critical values from measurements. Nevertheless, since fatigue crack initiation and propagation of silicon is less likely in case of $G < G_{\mathrm{Ic}}$, it can be assumed that the crack continues along the interface between silicon and epoxy.



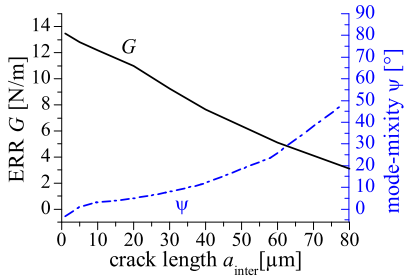
(a) Phases of cracking in fillet; A: bulk crack; B: deflection; C: delamination along die edge



(b) A → B - bulk crack; ERR G as function of crack length; propagation is Mode-I dominated



(c) B: highest ERR G for a crack along vertical die edge; die cracking not likely



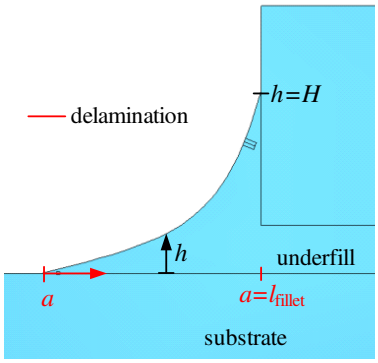
(d) B → C; decreasing ERR G, and increasing Mode-II with crack length

Fig. 7.13: Phases of crack propagation of a bulk crack in the fillet; accelerated crack propagation in underfill until vertical die edge; deflection at vertical die edge; decreasing delamination because Mode-II increases

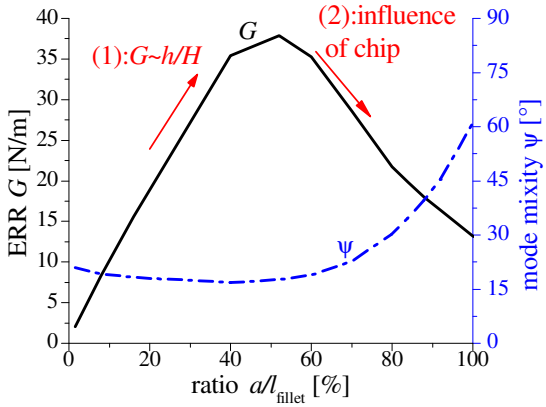
From Fig. 7.13c, it can be deduced that in case of interfacial crack propagation, the crack continues along the highest existing ERR which is towards the LCP board. The existing ERR in that direction is $G_I = 14.3$ N/m, and towards the upper chip surface only $G_I = 8.3$ N/m. Moreover, considering the mode-mixity for interfacial cracking in Fig. 7.13d, the phase angle is close to zero, which implies a high portion of tension loading. As stated for the interfacial toughness for NCA/LCP, the lower the mode-mixity angle, the lower the fracture toughness. Therefore, it is likely that the crack propagates along the vertical die edge to point "C".

7.2.3 Assessment of Delamination Adhesive/Board

Location "3" in Fig. 7.10, the interface between the underfill fillet and the substrate, also shows a maximum of principle stresses. In order to study the interfacial crack propagation, a FE analysis is performed. A delamination as in Fig. 7.3c is modeled. The delamination length is varied and ERR and the phase angle ψ are calculated. Fig. 7.14b shows G and ψ as functions of the ratio crack length a to the fillet length l_{fillet}. The function ERR as well as the mode-mixity can be separated into two regimes. Regime (1) $G \sim h/H$ dominates up to a ratio $\frac{a}{l_{\text{fillet}}}$ of about 50 %. Regime (2) dominates when the delamination reaches the chip edge.



(a) Definition of crack length $a = 0..l_{\text{fillet}}$ and fillet height $h = 0..H$



(b) Energy Release Rate G and mode-mixity ϕ as function of delaminated length a/h_{fillet} between underfill and board

Fig. 7.14: Analysis of delamination between underfill and LCP board; two effects are interacting; (1) for small a, the geometry can be approximated by a two-layer system with thicknesses h, H, Fig. 7.15; ERR G is proportional to the ratio h/H; (2) chip restricts crack opening and leads to an increasing shearing portion when a approaches l_{fillet}

Regime (1) can be approximated by a two-layered system consisting of underfill and substrate, as sketched in Fig. 7.15. It is also exposed to a temperature change. The thickness ratio h, H, and the difference in material properties lead to a loading of a pre-existing delamination. Fig. 7.15 shows the ERR and phase angle for different ratios of h, H. It is seen that for an increasing ratio, the ERR increases as well. This is due the fact that rigidity of the upper layer rises. The mode-mixity is almost independent of the ratio. Applied to the studied flip chip interconnection, this characteristic is also seen for Regime (1).

Approaching the edge of the chip, the influence of the restricted bending due to the rigidity of the chip dominates the characteristic of ERR and the phase angle, Regime (2). The delamination faces an increasing part of shearing portion which results in a rising phase

angle ψ. Increasing phase angle ψ and decreasing total energy release rate G lead to a lowered risk of delamination propagation.

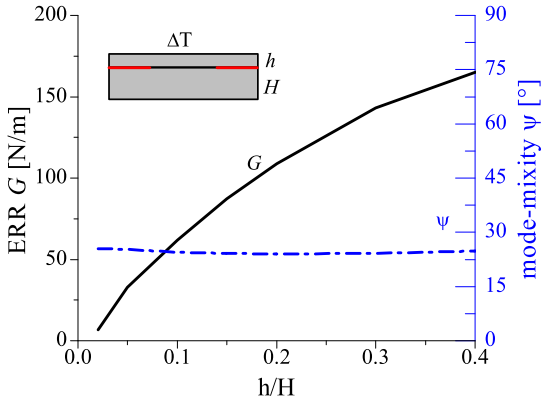


Fig. 7.15: Two-layered system as simplification of model in Fig. 7.14a, to explain the delamination behavior of the flip chip fillet for a/l_{fillet} between 0 % and 50 %; h and H are the thicknesses of the layered system; increasing ERR for increasing ratio of h, H; phase angle ψ is almost independent of the ratio [28, 29, 56]

Chapter 8

Characterization of Flip Chip Assemblies

8.1 Layout and Characterization of MID substrates

8.1.1 Layout of the MID substrates

In order to study the proposed failure mechanisms, the experimentally assembled flip chip interconnections are characterized since the used SBB technologies, materials, substrate thicknesses and fillet shapes have to be known to study the impact of these parameters. The Printed Circuit Board (PCB) is manufactured using the Molded Interconnect Devices (MID) technology. Hereby, a thermoplastic plate is produced using injection molding. As board material, Liquid Crystal Polymer (LCP) is used. The plates have a size of 80×80 mm^2 and a thickness of 1 and 2 mm. The material properties are described in Chapter 5.

The LPKF-Laser-Direct-Structuring (LDS) technology is invoked to deposit a conductive pattern on the LCP board [50, 61, 62, 97]. The metallization is established using an electroless chemical deposition of copper, nickel and gold with a thickness of about 6-8 μm, 2-3 μm and 0.1 μm respectively.

The layout of the conductor paths for the MID substrate for 5×5 mm^2 is shown in Fig. 8.1. Different layouts are designed for the different peripheric bumped chips. Depending on the chip size, different numbers of chips are fit onto the MID board.

The layout is designed to enable checking of functionality of all bumps. Additionally, Kelvin measurements of nearly each bump on the chip are possible. Moreover, the resistance of some MID conductor paths can be monitored.

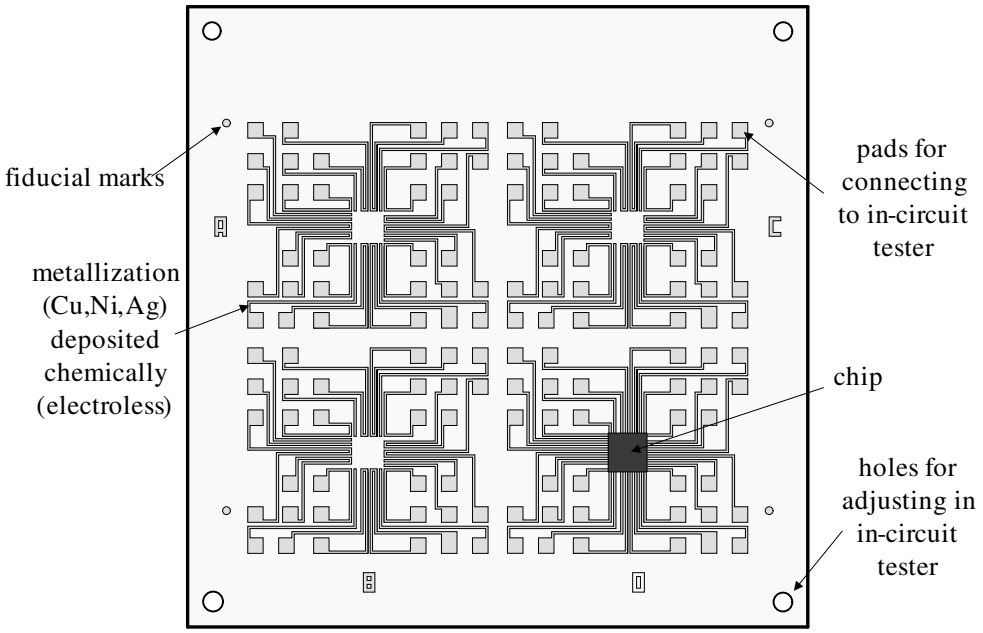
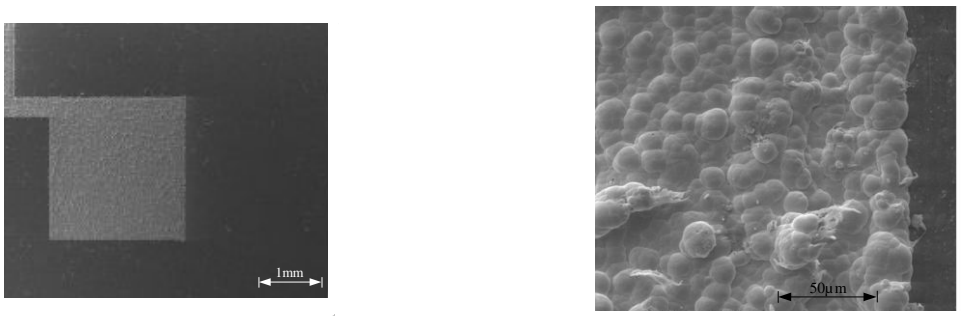


Fig. 8.1: Layout of MID substrate for 5×5 mm^2 chips; depending on the chip size, different number of chips are placed on the board; the layout includes fiducial marks for the assembly process as well as pads for needle probing for electrical transition resistance measurements of the flip chips; the holes are used for adjustment in the in-circuit tester

8.1.2 Metallization Process and Characterization of MID Substrates

The electroless chemical metallization process results in a relatively rough surface. The surface structure is qualitatively seen in Fig. 8.2a and Fig. 8.2b.



(a) Pad for probing

(b) detail

Fig. 8.2: SEM of MID substrate; rough metallization surface due to electroless chemical deposition process

The average thickness of the metallization is about 12 μm. The difference of maximum and minimum thickness within a single conductor path is up to 8 μm, refer to Fig. 8.3.

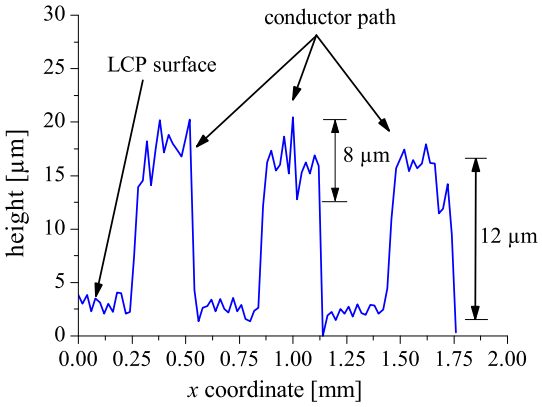


Fig. 8.3: Line scan of conductor path on MID substrate; overall averaged thickness of metallization is about 12 μm; the difference between maximum and minimum metallization thickness of a single conductor path is about 8 μm

8.1.3 Surface Properties of LCP Substrate

For capillary underfill, the surface tension strongly influences the wetting of the printed wiring board [32]. It is desirable to increase the surface tension for optimized wetting of the substrate. Plasma treatment is a method to clean surfaces of contaminations and improve the adhesion. The increased adhesion is based on various effects such as mechanical interlocking, interdiffusion, interpenetration of the network, and chemical bonding theories [100, 111]. The effect of plasma treatment on the the surface tension is shown in Fig. 8.4.

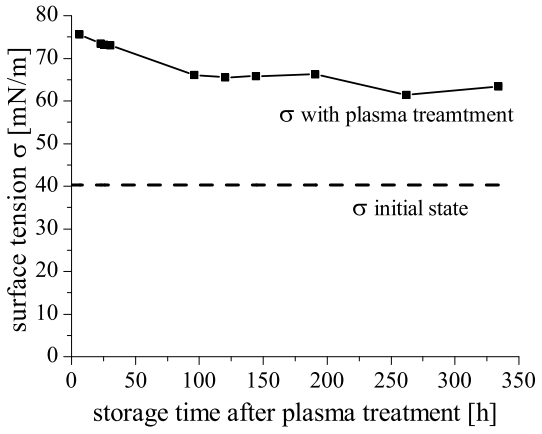
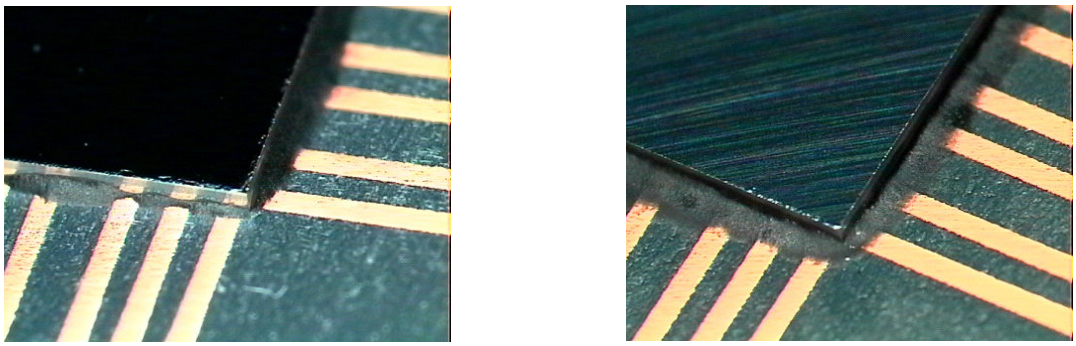


Fig. 8.4: Surface tension of LCP with and without oxygen plasma treatment

The LCP substrates are exposed to low pressure (0.1 bar) oxygen plasma treatment for three minutes. The surface tension is obtained from contact angle measurements [32, 77, 100]. Glycerin, water and methyleniodid are used as test liquids to measure the surface energy. The method according to *Owens*, *Wendt*, *Rabel* and *Kaelble* is applied to calculate the surface tension [69, 75]. The surface tension of a LCP substrate after metallization process lies at 40 mN/m. Directly after plasma treatment it increases to 76 mN/m. The flip chip assembly process, and therefore the underfill process, is performed within one day after plasma treatment where the surface tension only dropped by 4 %. The surface tension of FR4 printed wiring boards with soldermask lies between 50 to 60 mN/m [32, 77].

The low surface tension of the LCP substrate without plasma treatment leads to weak wetting of the capillary underfill. Moreover, without plasma treatment, the SBB flip chip process utilizing capillary underfill leads to inhomogeneous fillet formation, Fig. 8.5a. Therefore, all MID-substrates used for capillary underfilling are plasma treated, Fig. 8.5b.



(a) without plasma treatment (b) with plasma treatment

Fig. 8.5: Impact of plasma treatment on fillet formation for capillary underfill process; LCP substrate without plasma treatment leads to inhomogeneous fillet formation; therefore only plasma treated LCP plates for SBB process with capillary underfill are used

8.2 Flip Chip and Stud Bump Bonding Process

8.2.1 Process Description of Stud Bumping

Two different chip sizes are used to investigate the impact of chip size on the reliability of a SBB flip chip interconnection: 5×5 and 10×10 mm^2. The thickness is the same for all chips: 300 μm. The layout of the 5×5 mm^2 flip chip is shown in Fig. 8.6. The pitch of the bumps is 600 μm. The layout of the 10×10 mm^2 is similar.

The bumps are manufactured by a stud bumping process which utilizes a modified ball bonding process [39, 51, 66, 91, 129]. The gold wire for the stud bumping has a thickness of

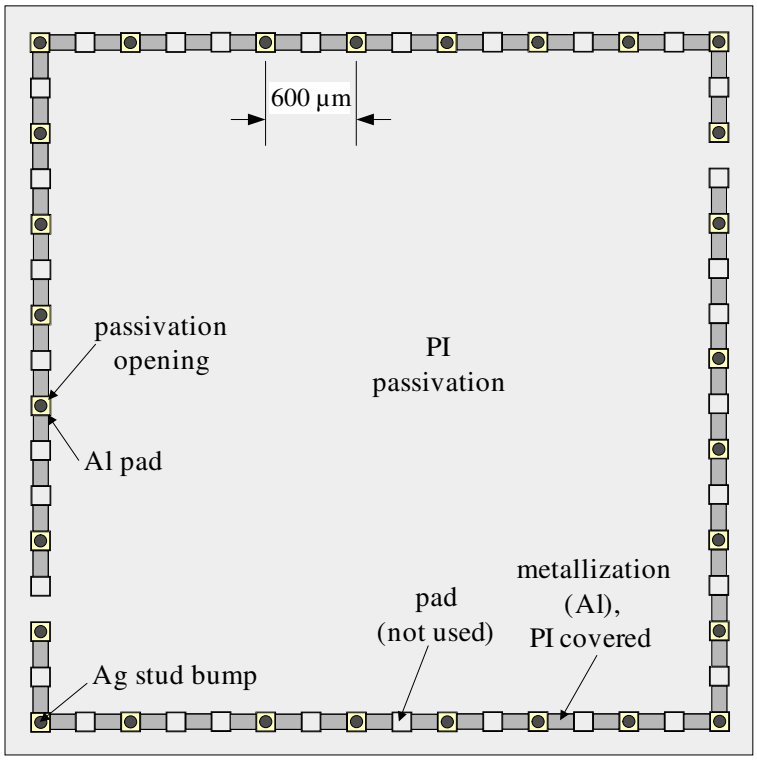
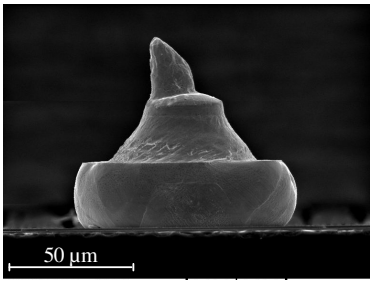


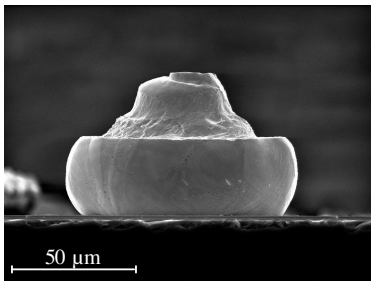
Fig. 8.6: Layout Flip Chip 5×5 mm^2 with 28 bumps and a pitch of 600 μm; additional, chips with size of 10×10 mm^2 are designed with 64 bumps

33 μm. The stud bumps after the bumping process have a diameter of about 110 μm. The height without the tail lies around 100 μm, Fig. 8.7a. The tail is defined as the left-over of the wire before the wire is towed away.

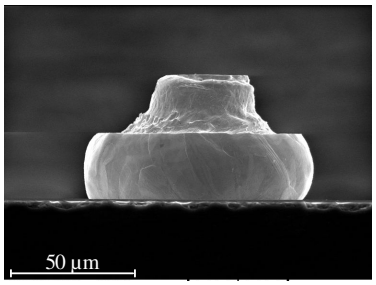
The coining process, which is used to equalize the height of all bumps of a single chip, can either be performed before or during assembly process [66]. The latter-mentioned procedure has the advantage of less process steps. The influence of coining force is investigated by using different values, 0.2 to 0.6 N/bump. For forces greater than 0.4 N/bump, no significant change in height is observed, Fig. 8.7.



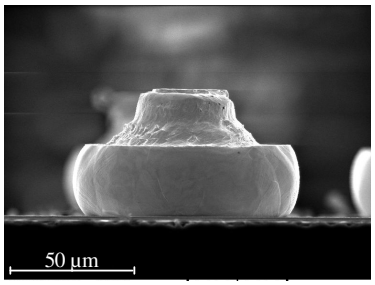
(a) After stud bumping process



(b) Coining force 0.2 N/Bump



(c) Coining force 0.4 N/Bump



(d) Coining force 0.6 N/Bump

Fig. 8.7: SEM pictures of stud bumps after stud bumping and subsequent coining

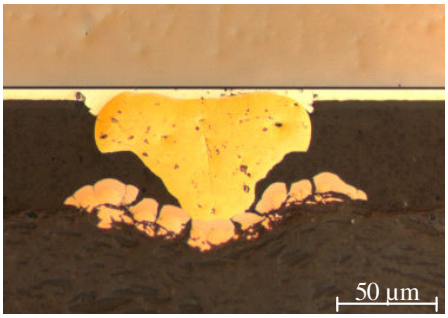
8.2.2 Stud Bump Bonding Process

Assembly Process

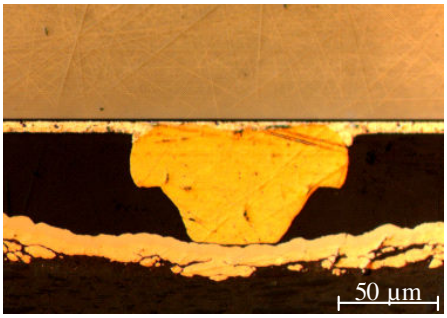
The appropriate force for placing the flip chip on the MID board is dependent on the deformation of the bump, as well as on the rigidity of the conductor path of the MID substrate. Because of its fragile structure, an assembly force of 0.6 N/bump leads to cracks in the metallization of the substrate, Fig. 8.8a. This can lead to electrical failure. By performing the coining and flip chip assembly on the MID board in two separate steps, cracking in the substrate metallization can be avoided. Hereby, the coining is performed on a rigid flat plate with a force of 0.6 N/bump. Whereas for the flip chip assembly process a reduced force of 0.2 N/bump is used, which is shown in Fig. 8.8b. This procedure is followed for SBB flip chip interconnections using ICA/capillary underfill, as well as for NCA interconnections.

ICA/Capillary Underfill Process

The ICA process is performed as described in Fig 2.4. A conductive adhesive which is specially made for the SBB technology is applied. The ICA is cured for 10 minutes at 150 °C. The adhesive shows a high flexibility, which is essential for the first cooling down to room temperature. The capillary underfill is applied at 60 °C in order to improve the filling process. The underfills UF1 and UF2 are cured in a batch oven for 30 minutes at 150 °C .



(a) Coining and assembly in a single step: force 0.6 N/bump



(b) Coining with 0.6 N/bump, assembly with 0.2 N/bump

Fig. 8.8: Influence sequence at SBB process (here displayed for NCA process, also valid for ICA process); assembly with a force of 0.6 N/bump leads to cracks in the MID metallization; coining and assembly with different forces advisable

NCA Process

The NCAs are dispensed on the MID-substrate. Two different NCAs are used: NCA1 and NCA2. The chip with its stud bumps is coined on a separate plate with 0.6 N/bump. Afterwards, the chip is placed on the MID-substrate with 0.2 N/bump. The curing of the NCA is performed by heating the picking tool to 180 °C. The manufacturer of the adhesives suggests a curing time of 10 seconds at that elevated temperature. In order to ensure complete curing, the flip chip interconnections are placed in a batch oven at 210 °C for 120 seconds.

8.2.3 Studied Flip Chip Assemblies

The objective of the investigation is to determine the factors which influence reliability. The potential factors can be divided into geometric and material properties of the underfills respectively NCAs. As geometric parameters the chip size, thickness of the LCP board, as well as the fillet shape are studied, Fig. 8.9. Two different chip sizes are utilized. Two different substrate thicknesses are used to produce the MID-boards. The fillet shape is indirectly varied by application of oxygen plasma treatment on the surface. The fillet shape is characterized in Section 8.3.

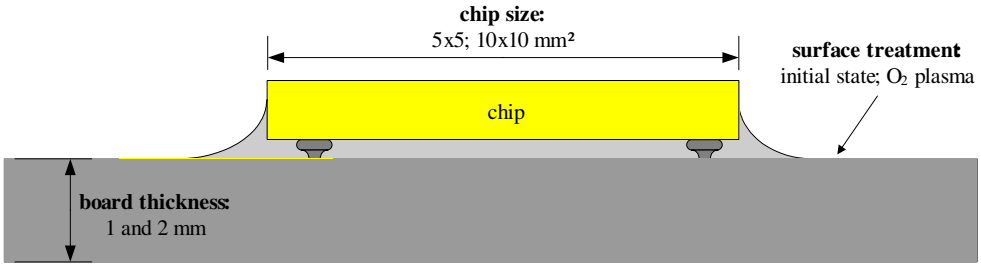


Fig. 8.9: experimental investigated geometric parameters: chip size, substrate thickness and fillet shape due to application of plasma treatment

The two different SBB technologies are used to assemble the flip chip interconnections: ICA/capillary underfill and NCA technology.

As mentioned previously, the SBB technology with capillary underfill requires plasma treatment of the LCP substrates. Therefore, only plasma-treated MID boards are used to assemble. This does not apply for the NCA technology. During the assembly step, the NCA is squeezed by pressing the chip into the adhesive. Therefore, LCP plates with and without oxygen plasma treatment are used for reliability testing. Tab. 8.1 gives an overview of all assembled flip chip interconnections and their characteristics.

Tab. 8.1: List of all assembled and tested flip chip interconnections

Adhesive	**Board Thickness**	**Surface Condition LCP**	**Chip Size** [mm^2]	**Internal No.**
UF1	1 mm	O_2 plasma	10×10	A
UF1	2 mm	O_2 plasma	10×10	B
UF1	1 mm	O_2 plasma	5×5	11
UF2	1 mm	O_2 plasma	10×10	C
UF2	2 mm	O_2 plasma	10×10	D
UF2	1 mm	O_2 plasma	5×5	12
UF2	2 mm	O_2 plasma	5×5	6
NCA1	1 mm	initial condition	5×5	7
NCA1	2 mm	initial condition	5×5	2
NCA1	1 mm	O_2 plasma	5×5	8
NCA1	2 mm	O_2 plasma	5×5	4
NCA2	1 mm	initial condition	5×5	10
NCA2	2 mm	initial condition	5×5	3
NCA2	1 mm	O_2 plasma	5×5	9
NCA2	2 mm	O_2 plasma	5×5	1

8.3 Characterization of Flip Chip Assembly

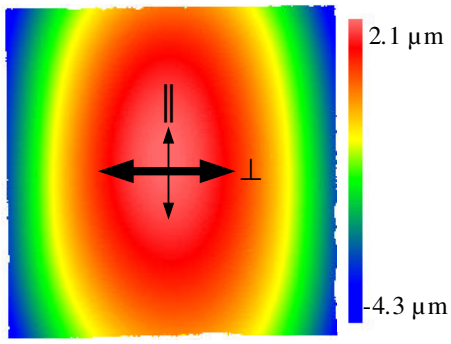
8.3.1 Warpage Measurements

Considerations and Measurement Procedure

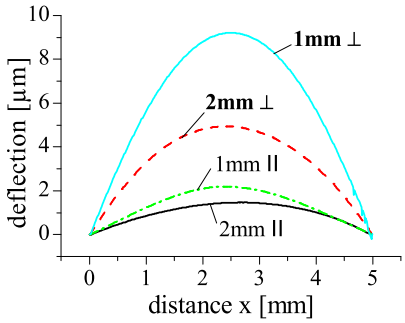
The warpage of the flip chip package is mainly caused by the CTE-mismatch of the silicon and board when exposed to temperature change. Additional warpage is contributed by the cure shrinkage of the adhesive. In many studies, it is assumed that a stress-free, and therefore warpage-free condition, is present at curing temperature. The cure shrinkage is neglected. This is supported by the FE analysis performed on the SBB flip chip interconnection, shown in Fig. 7.7. The warpage of the assembled flip chip interconnections is measured using the interferometer method and is determined at room temperature.

Warpage of ICA/Capillary Underfill Flip Chip Interconnections

The underfills UF1,UF2 of the SBB flip chip assemblies utilizing ICA/capillary underfill are cured at 150 °C. The cooling down to room temperature causes convex bending of the interconnection due to the CTE-mismatch. The CTE values of LCP are thickness-dependent, as well as dependent on the flow direction of the injection molding process. The thinner the plate, the smaller the CTE value for LCP. Moreover, the CTE value along flow direction is smaller than transversal to flow direction. At the same time, the warpage is also restricted by the rigidity of the board. The thicker the board, the higher the section module. These two considerations explain the results of the warpage measurements for Fig. 8.10a. Although the CTE of 1 mm plates is smaller, the warpage is bigger than that of the 2 mm plates, which have a higher CTE value. This is due the higher section modulus of the 2 mm boards.



(a) Fine arrow shows flow direction of LCP (α=7.5 ppm/K), wide arrow transversal direction (α=20 ppm/K)

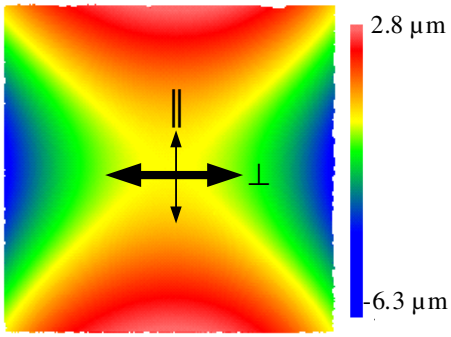


(b) path of maximum warpage along and perpendicular to flow direction from Fig. 8.10a

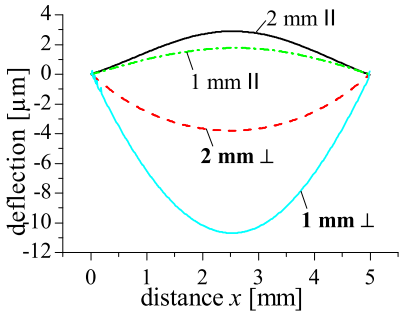
Fig. 8.10: Warpage measurements of ICA/capillary underfill flip chip interconnections (chip size 5×5 mm^2, chip thickness 300 μm) performed at room temperature, obtained from interferometer method; convex warpage for all combinations; higher warpage for path along transversal flow direction and thinner boards

Warpage of NCA Flip Chip Interconnections

The steps of the NCA process are described in Section 8.2.2. In contrast to the ICA/capillary underfill interconnections, the chips show a convex and concave warpage depending on the orientation of the LCP substrate. Along the flow direction of the substrate the path shows a concave deflection, while on the same chip, there is a convex bending perpendicular to flow direction. This is observed for 1 mm and 2 mm LCP plates. As stated, the warpage caused by curing can be neglected.



(a) convex warpage along flow direction, concave in transversal flow direction



(b) path of maximum warpage along and perpendicular to flow direction from Fig. a

Fig. 8.11: Warpage measurements of NCA flip chip interconnections (chip size 5×5 mm^2, chip thickness 300 μm) performed at room temperature; the concave warpage can be explained by the annealing of the LCP board during post-curing process at 210 °C; the plain LCP board also shows concave bending when exposed to the elevated temperature (without flip chip assembly); the annealing process requires a certain temperature; the curing temperature of the ICA flip chip assemblies, T=150 °C, is too low to lead to annealing in the LCP

In Tab. 8.2, the deflection radius of the plain LCP substrates are listed. The deflection measurements are performed using the interferometer method.

Tab. 8.2: Deflection radius of LCP plate after manufacturing (without flip chip), storage at 150 °C for 24 hours and 210 °C for two minutes; the radius is measured longitudinally and transversally to flow direction at both board thicknesses of 1 and 2 mm; results reveal that the radius decreases when exposed to temperature storage which equals an increasing warpage; this effect is much more distinct for the transversal direction in which the radius changes signs, explaining, the warpage of the flip chip interconnections in Fig. 8.11

Board Thickness	1 mm		2 mm	
Orientation	longitudinal	transversal	longitudinal	transversal
25 °C	19644 mm	285473 mm	238006 mm	35605 mm
150 °C	15937 mm	10066 mm	109801 mm	26478 mm
210 °C	1972 mm	-2529 mm	14913 mm	-17315 mm

The measurement of the radius is carried out directly after the molding process and again after temperature storages at different temperatures. The curing of the ICA flip chip interconnections are done at 150 °C where the NCA interconnections faced post-curing. The post-curing is carried out in a batch oven for two minutes at 210 °C. These temperatures are chosen to study the influence of the board deflection on the flip chip warpage. The deflection radius of the plain LCP boards show a large value for the initial condition as well as for the boards after temperature storage at 150 °C. This translates to a very low bending of the boards. The radius longitudinal and transversal to the molding direction shows a significant difference already at these temperatures. Moreover, the deflection radius for the 1 and 2 mm boards are different. Exposing the LCP to 210 °C storage – to simulate the post curing of the NCA – the radius changes even more. For the transversal direction, the sign of the deflection changes. Annealing of LCP at leveled temperatures leads to a reduction of the residual stresses [26]. These stresses are caused by inhomogeneous cooling during and after demolding. The annealing has a certain threshold temperature and is strongly dependent on the orientation with respect to the molding gate. Based on these results, it can be stated that the concave bending of the NCA flip chip interconnections, Fig. 8.11, is due to annealing processes when exposed to 210 °C storage, and not to the CTE-mismatch chip/board.

8.3.2 Fillet Formation

Finite Element analysis reveals that the maximum stresses are present in the fillet. It can be assumed that the fillet shape has an influence on the stress. Therefore, the fillet shapes of all assembled flip chip interconnection are recorded. The fillet is dependent on the applied volume of capillary underfill respective to the NCA volume dispensed. Moreover, the surface tension of the MID board is a key factor concerning the wetting angle $\theta_{\text{substrate}}$. The influence of the surface tension of LCP is shown; plasma treatment leads to a spreading of a liquid on the surface. This changes the wetting angle. Therefore, the wetting angle in the cured state is essential when studying the behavior of a crack located in the fillet. In order to characterize the fillet shape, the fillet width and length, as well as the wetting angles $\theta_{\text{substrate}}$ and θ_{chip} are used, Fig. 8.12.

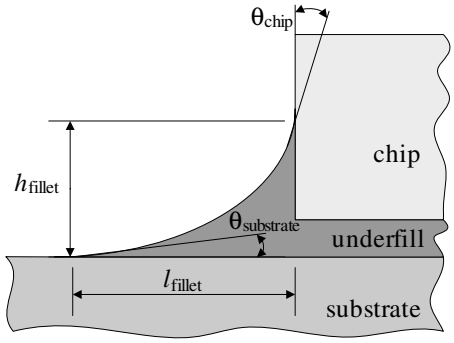
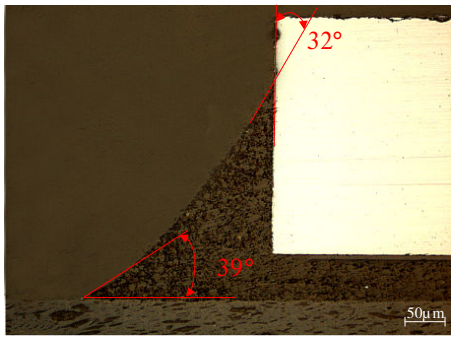
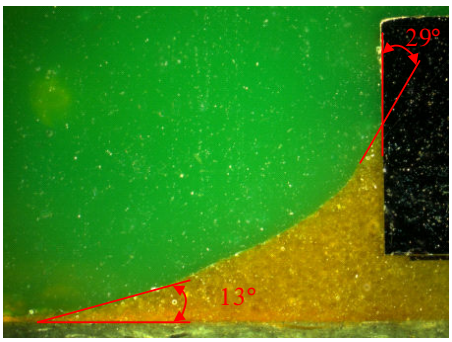


Fig. 8.12: Definition of wetting angles and fillet height and length

Fig. 8.13 shows the procedure for measuring the wetting angles. Fig. 8.13a shows the cross-section of a flip chip interconnection where NCA2 is used. The LCP surface is not plasma-activated. On the other side, Fig. 8.13b shows the influence of plasma treatment for a flip chip interconnection where UF2 is used.



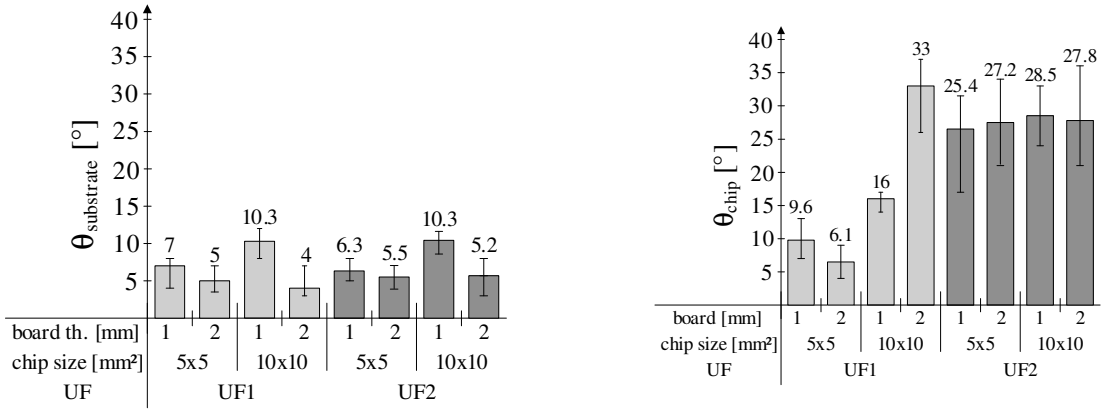
(a) NCA2; MID substrate without plasma treatment



(b) UF2: MID substrate with plasma treated surface

Fig. 8.13: Wetting angles of fillet

For all ICA SBB flip chip interconnections, the LCP is plasma treated before flip chip assembly. Two different chip sizes are used. The wetting angles $\theta_{\text{substrate}}$ and θ_{chip} are displayed in Fig. 8.14. It can be seen that the variation of the fillet angles is high for some combinations.



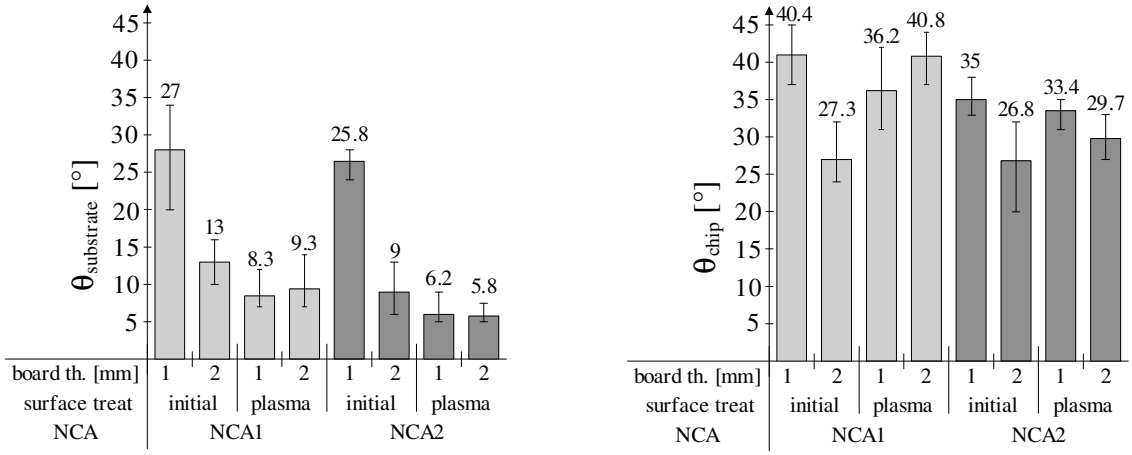
(a) Wetting Angle UF/LCP $\theta_{\text{substrate}}$

(b) Wetting Angle UF/chip θ_{chip}

Fig. 8.14: Wetting angle for flip chip interconnections where UF1 and UF2 is used

This is similar for the flip chip interconnections where the NCA technology is invoked. Flip chip interconnections on LCP boards, without plasma treatment of the surface, show different wetting angles for the 1 mm and 2 mm plates. The metallization process of the 1 mm and 2 mm boards is the same, but these were produced from different metallization batches. The cause is not further studied. Nevertheless, the resulting wetting angles are important and therefore recorded.

The same effect, a difference in the wetting angles for 1 mm and 2 mm LCP boards, is seen for flip chip interconnections where NCA2 is used, Fig. 8.15.



(a) $\theta_{\text{substrate}}$

(b) θ_{chip}

Fig. 8.15: Wetting angles for the NCA technology with NCA1 and NCA2

Part III

Reliability Studies

Chapter 9

Design-Study by Application of Theoretical Failure Criteria

9.1 Considerations Concerning Impact of Parameters

9.1.1 Failure Criteria Used for Design-Studies

The parameters of a flip chip interconnection, which are displayed in Fig. 7.1, can be classified by the size of impact on a theoretical failure criterion. Some parameters have less impact on a certain criterion, but an enormous impact on the other. In the present study, two criteria are used to study the impact of the geometric and material properties of the board and underfill respectively NCA. In the first, the stress intensity factor K_{I} for an existing bulk crack in the fillet is taken as a failure criterion. In order to take the critical stress intensity factors K_{Ic} for the studied underfills/NCAs into account, a normalized, dimensionless stress intensity factor $\overline{K_{\mathrm{I}}}$ with

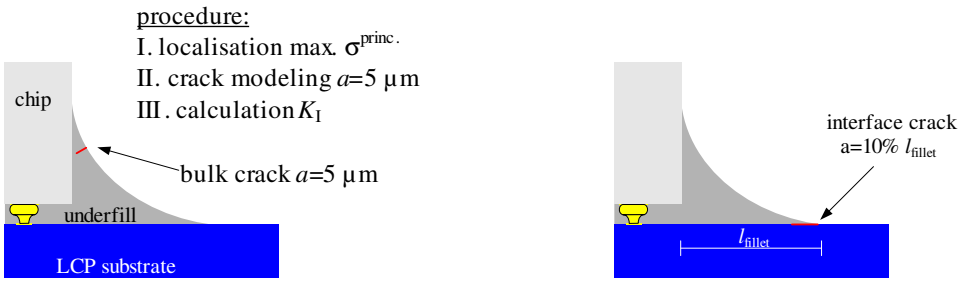
$$\overline{K_{\mathrm{I}}} = \frac{K_{\mathrm{I}}}{K_{\mathrm{Ic}}} \tag{9.1}$$

is defined for the different underfills and NCAs. The higher the value, the higher the load of an existing crack caused by one thermal cycle.

Fig. 9.1a shows the procedure which is applied to model a bulk crack in the fillet. The location of maximum stress along the fillet is identified and a crack of 5 μm is modeled. 5 μm is the maximum particle size for the underfills used, Tab. 5.2 and Tab. 5.3.

In the second, a modeled delamination between the substrate and the underfill is used as criterion, where the energy release rate ERR G as well as the phase angle ψ are considered, Fig. 9.1b. The difficulty for the latter-mentioned criterion lies in a two-parameter failure

criterion. The ERR and phase angle can not be discussed independently as shown in Fig. 6.13. The critical values for interfacial fracture toughness between LCP and the underfill are much higher than the calculated load for the studied flip chip interconnection when exposed to one thermal cycle. Nevertheless, cycling exposure to temperature change leads to fatigue delamination initiation and propagation.

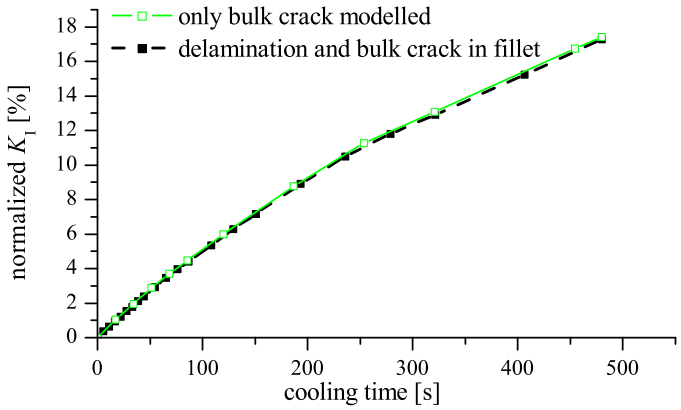


(a) Criterion I: bulk cracking in the underfill/NCA fillet; crack length of $a = 5\ \mu$m is used from averaged particle size

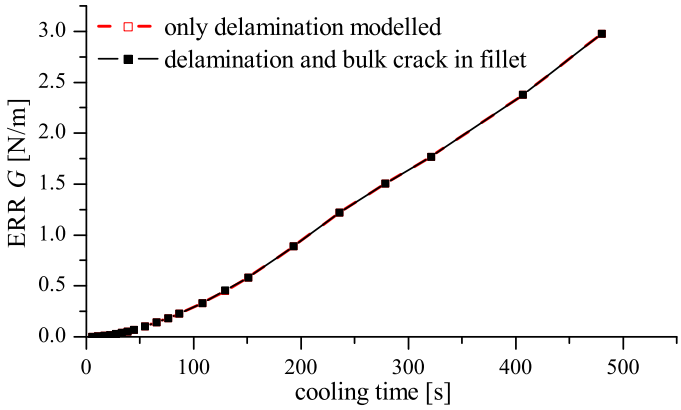
(b) Criterion II: interfacial cracking; crack length a is chosen to be 10 % of the fillet length l_{fillet}

Fig. 9.1: Failure criteria used to study impact of geometry and material properties of the flip chip interconnection

When considering the impact of the two failure mechanisms, it is essential to know if both of these failure mechanisms interact. Therefore, a model is set up which shows both failures: a fillet crack and a delamination between the adhesive and the substrate. Additionally, $\overline{K}_{\text{I}}$ and G are calculated for models which show only the fillet crack or delamination. Fig. 9.2a compares the normalized stress intensity factor $\overline{K}_{\text{I}}$ for a model with both failures to a model with only a fillet crack. It can be stated that the risk of failure in the fillet is independent of the delamination between board and adhesive. The same negligible effect is detected when modeling the delamination between the adhesive and substrate, Fig. 9.2b. This can be explained by the small size of the defects. Based on this result, it can be stated that for a single flip chip interconnection, both failure mechanisms can occur simultaneously.



(a) Criterion I: Calculation of the stress intensity factor $\overline{K}_{\mathrm{Ic}}$ for a model with only a fillet crack and another with both studied failure modes



(b) Criterion II: comparison of ERR G for a model which shows both failure modes and a model with only a delamination

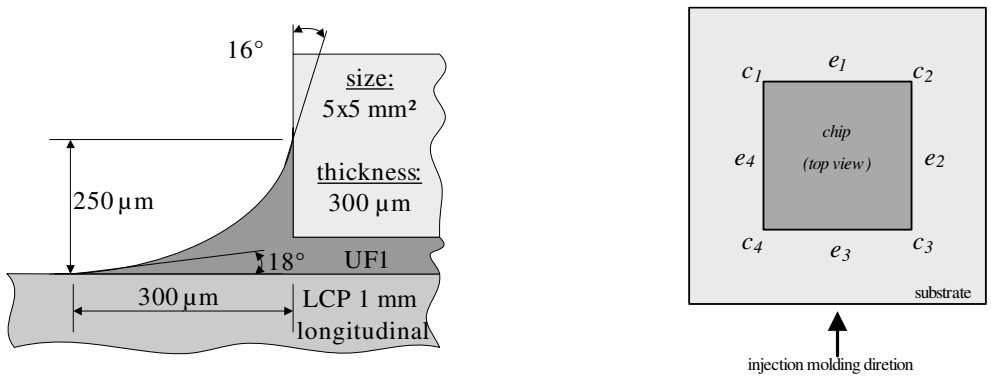
Fig. 9.2: Interaction of the two studied failure modes; it reveals that there is no interaction between the two failure modes, e.g. for a single flip chip interconnection, both failure modes can lead to failure simultaneously; this can be explained by the local character of the failures

9.1.2 Investigated Design Parameters

The relevant design parameters are various geometric features and the material properties. The impact of these parameters on the described failure criteria is investigated in order to deduce design rules for flip chip interconnections. The impact of the geometric features chip size, board thickness and fillet shape are studied, as well as the influence of the board and underfill material on the described failure criteria.

The study of these parameters is sequentially performed, first as a general study and determination of the influence. It is then applied to the actually assembled flip chip interconnection.

The parameters are firstly studied independently of one other. Therefore, a representative flip chip interconnection is created as sketched in Fig. 9.3a.



(a) Representative flip chip interconnection; study of impact of certain parameters (variation of one parameter at the time)

(b) Numbering of edges and corners of the adhesive fillet with respect to direction of molding process of the board

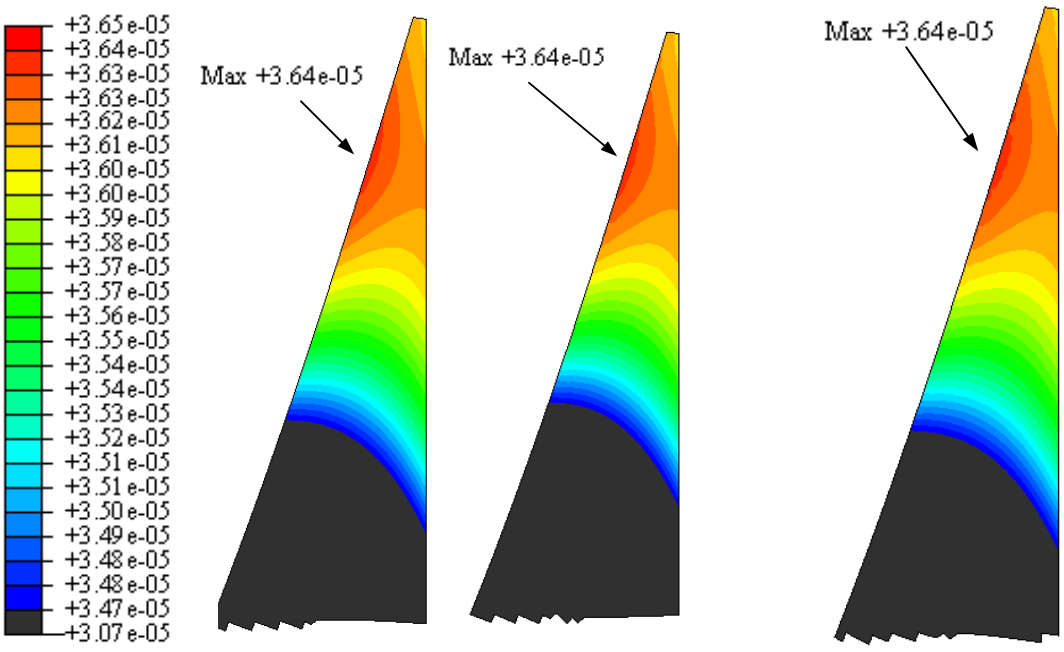
Fig. 9.3: Representative flip chip interconnection and numbering of edges and corners

The single edges and corners of the fillet are numbered as shown in Fig. 9.3b. The edges e_2 and e_4 lie along the injection molding direction, perpendicular to the edges e_1 and e_3.

9.2 Impact of Specific Geometric Parameters and Material Properties

9.2.1 Size of Flip Chip

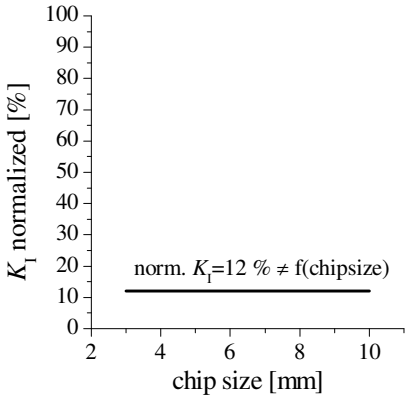
In order to study the impact of the chip size, three different chip sizes are theoretically compared: 3×3, 5×5 and 10×10 mm^2. The other parameters are kept constant as described in Fig. 9.3. A stress analysis without any defects in the fillet is performed. Fig. 9.4 shows the stress field in the fillet for the different chip sizes, but with the same fillet shape, board thickness and material parameters. It can be clearly seen that the location of maximum principle stress $\sigma_{\text{max.}}^{\text{princ.}}$, as well as the value of $\sigma_{\text{max.}}^{\text{princ.}}$ are independent of the chip size. This can be explained by the fact that the stress field at the outer line is mainly determined by the local geometry and material properties. Therefore, the failure criteria I and II are also not influenced by the chip size, Fig. 9.5. But it is worth mentioning that once the crack reached a significant length, the global behavior of the flip chip interconnection is influenced by the crack and therefore by the chip size.



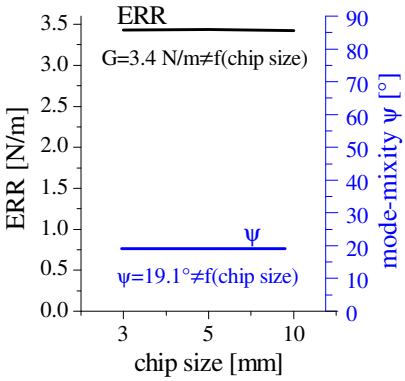
(a) Size: 3×3 mm^2 (b) Size: 5×5 mm^2 (c) Size: 10×10 mm^2

Fig. 9.4: Maximum principle stresses $\sigma_{\text{max.}}^{\text{princ.}}$ for different chip sizes for a flip chip interconnection without crack; range and position of maximum stresses $\sigma_{\text{max.}}^{\text{princ.}}$ independent of chip size; the key holds for Fig. 9.4a-c; units of the maximum principle stresses are in N/μm^2 $= 1 \cdot 10^6$ N/mm^2

Based on these results, the study of the other parameters of the global behavior as well of both failure criteria are performed for a chip size of 5×5 mm^2.



(a) Failure Criterion I: bulk crack in the fillet



(b) Failure Criterion II: interfacial crack between adhesive and LCP

Fig. 9.5: Influence of chip size on the failure criteria; chip size influences the global behavior, but not the local behavior in the region where the cracks occur

9.2.2 Board Thickness

The board material in the present study is made of the thermoplastic Liquid Crystal Polymer (LCP). The plates are made by injection molding and have a thickness of 1 and 2 mm. The thermo-mechanical behavior is assumed to be linear-elastic, but temperature-dependent. Additionally, LCP has the characteristic that the material properties are dependent on the orientation with respect to the flow direction of the injection molding process. Moreover, the properties are thickness-dependent. A rough estimation of the dependency of the warpage d of the board thickness can be performed based on the inertia of bending. The warpage is inversely related to the substrate thickness to the third power. The influence of the board

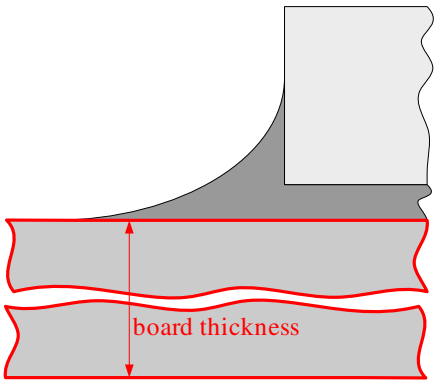


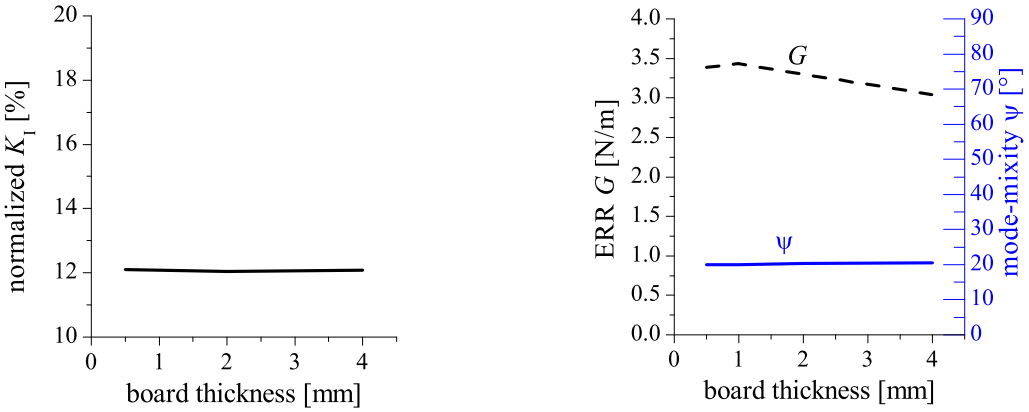
Fig. 9.6: Variation of board thickness between 0.5 and 4 mm

thickness and material properties on the failure criteria are more complex. In order to obtain a general relation between the substrate parameters and the failure criteria, the properties

are altered in a wider range than in the actually assembled flip chip interconnections. The warpage of the chip is calculated for board thicknesses of 0.5, 1, 2 and 4 mm, Fig. 9.6. The Young's modulus is assumed to be independent of the thickness in order to be able to distinguish between the impact of thickness and Young's modulus.

Because of the inverse relation of the thickness of the board to the inertia of bending, the warpage of the flip chip interconnection due to thermal cycling decays for increasing board thicknesses.

Concerning the defined failure criteria, the board thickness shows diverse impacts. For failure criterion I, the board thickness does not have an impact on an existing crack in the upper part of the fillet, Fig. 9.7a. This can be explained by the local character of the failure mode. It can be expected that the board thickness has an influence on failure criterion II. This is due to the fact that delamination depends on the localized stress field around the delamination tip. The impact of board thickness on the ERR and mode-mixity is shown in Fig. 9.7b. The ERR experiences a small impact from the board thickness where ψ does not have any dependence on the board thickness (in the varied range).



(a) Failure criterion I

(b) Failure criterion II

Fig. 9.7: Impact of board thickness on failure criteria: the normalized stress intensity factor and the mode-mixity show no dependence on the board thickness; a very small impact is detected for the ERR; this can be explained by the local character of the failure mechanisms

9.2.3 Board Material Properties

The board material is LCP. Because the properties are dependent on the board thickness and orientation, a general analysis of the influence of the board material properties, CTE α and Young's modulus E, is performed, Fig. 9.8. E is varied between 2 and 80 GPa. The CTE values are altered from 2 to 40 ppm/K. The Poisson's ratio is kept at 0.3.

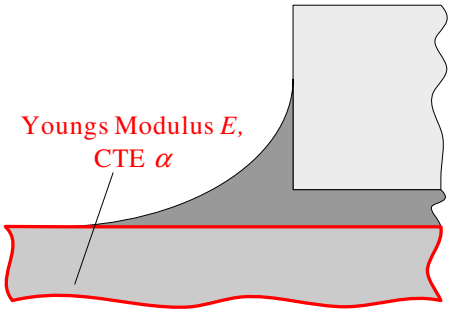
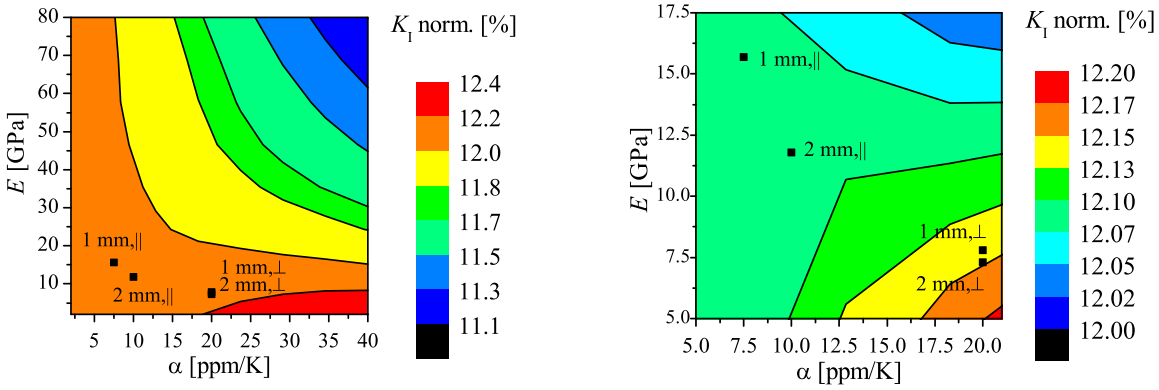


Fig. 9.8: Variation of Young's modulus E and CTE α of board

The stress intensity factor K for failure criterion I, calculated for the different board material properties, is displayed in Fig. 9.9. Additionally, the material properties of the boards used are shown.



(a) Stress Intensity Factor as a function of board material properties Young's modulus E and CTE α

(b) Detailed view on Fig. 9.9a; the range of $\overline{K}_I$ is small, but a tendency can be seen

Fig. 9.9: The influence of the board material used in the study on the normalized stress intensity factor $\overline{K}_I$ is quite small. Two tendencies are present: (1) increasing the rigidity of the board (higher Young's modulus) leads to decreasing stress intensity factors; this can be explained by a smaller bending of the board through its higher Young's modulus; (2) on the other side, a higher CTE value of the LCP board also reduces $\overline{K}_I$; increasing CTE leads to a smaller difference between the CTE value of the board and the adhesive, and therefore to a smaller load on an existing crack in the upper part of the fillet; but this is only valid for board Young's modulus higher than about 12.5 MPa; below that value, a higher CTE value of the board reduces the risk of bulk cracking in the fillet.

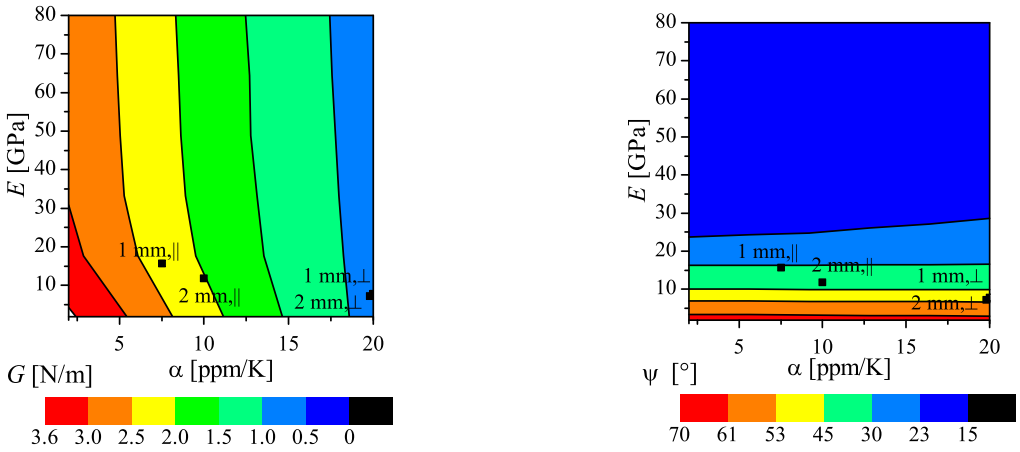
The impact on K shows a superposition of different effects. A higher Young's modulus of the board reduces the bending of the board when faced with temperature change. The higher the rigidity of the board, the smaller the bending of the board occurs. The bending is caused by the CTE-mismatch of board and die. Consequently, the adhesive underneath the die experiences much higher shear stresses, whereas the adhesive in the fillet is less stressed due to less bending of the board. This leads to a reduced stress intensity factor in the fillet.

On the other side, a reduction of CTE-mismatch between board and adhesive leads to less stresses in the fillet, which results in a smaller stress intensity factor. Nevertheless, this only can take place once a certain rigidity of the board is reached.

Another effect is seen in Fig. 9.9. Using a board with a smaller Young's modulus than the adhesive, as well as a CTE value close to the adhesive, higher stresses occur in the fillet. This is due the fact that the adhesive can contract freely.

In order to explain the relation of Young's modulus and CTE to the delamination between the LCP and the underfill, the flip chip interconnection is simplified by a two-layered beam: adhesive and board. Interfacial crack opening can only occur when the CTE value of the board is lower than the CTE of the adhesive; a higher rigidity of the board is assumed. The higher the CTE-mismatch between the adhesive and the board is, the higher the crack opening and therefore the ERR. This construct can explain the dependency of the ERR on the CTE of the board in Fig. 9.10.

Since the rigidity of the board is higher than the rigidity of the adhesive, the influence of the Young's modulus of the board on ERR is negligible. The Young's modulus of the board primarily determines the relation of tensile and shear stress in the interfacial crack which affects the mode-mixity. The higher the rigidity of the board, the less bending the board experiences. This leads to higher contraction of the adhesive in the fillet perpendicular to the board and therefore to higher tensile stresses in the crack.



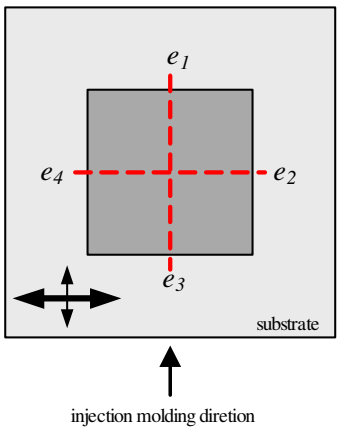
(a) Failure criterion II: ERR

(b) Failure criterion II: Phase angle

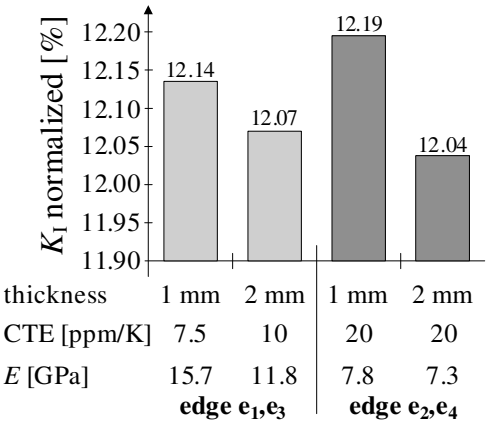
Fig. 9.10: ERR and mode-mixity for a delamination as function of board material properties Young's modulus E and CTE α; the ERR is almost not influenced by the Young's modulus of the board, but strongly influenced by the CTE value; since the CTE-mismatch of the board and the underfill leads to shearing stresses at an existing delamination, a higher CTE-mismatch results in a higher ERR; on the other side, the phase angle ψ is almost independent from the CTE-mismatch, due the fact that the mode-mixity is mostly influenced by the geometry of the fillet; but the mode separation method applied uses the difference in bulk properties of the underfill and LCP, the Young's modulus has a significant impact on the phase angle.

9.2.4 Orientation of Orthotropic Board Material

The orientation of the orthotropic board material influences the thermo-mechanical material properties. The CTE value for a LCP plate with 2 mm thickness is 10 ppm/K, where for 1 mm thickness α is determined to 7.5 ppm/K. The CTE for the transversal flow direction is 20 ppm/K for both plate thicknesses. Similar thickness and orientation dependency is present for the Young's modulus. The values are given in Fig. 9.11b.



(a) Board orientation; two board thickness are used: 1 and 2 mm



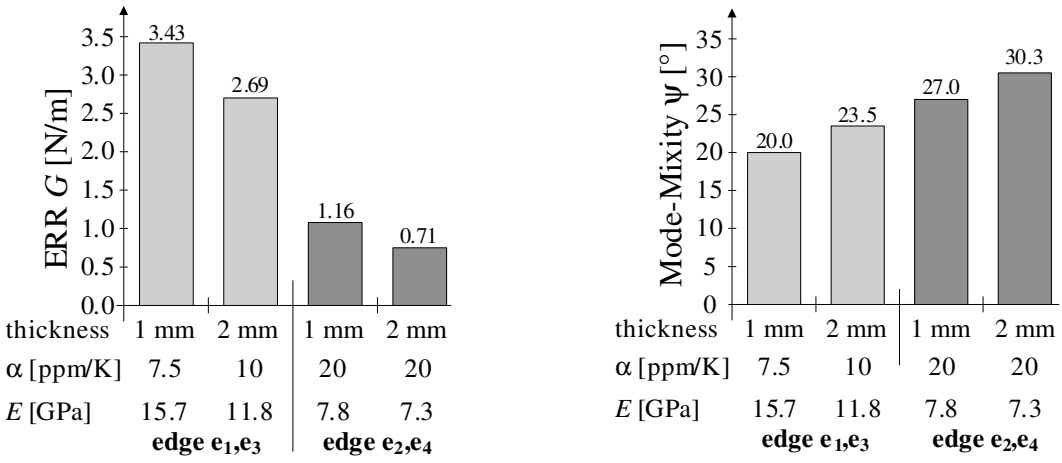
(b) Normalized stress intensity factor for different board orientations; and the material properties of the LCP board

Fig. 9.11: Influence of board orientation on fillet cracking; higher $\overline{K}_I$ for edges e_2 and e_4 and thinner boards; higher CTE of board in transversal direction leads to higher $\overline{K}_I$, as stated in Fig. 9.9, where increasing board thickness lowers the risk of fillet cracking, refer to Fig. 9.7; it can be concluded that the risk of bulk cracking along the edge e_2 and e_4 is higher

Fig. 9.11b shows the normalized stress intensity factor $\overline{K}_I$ for a bulk crack in the fillet for longitudinal and transversal board direction, as well as for two different board thicknesses. For a certain thickness, transversal and longitudinal board direction can be considered as two substrates with different material properties. Therefore, the results can be compared with the study of the impact of board material, refer to Fig. 9.9. The higher the CTE value and the smaller the Young's modulus of the board, the higher $\overline{K}_I$. This is the case for the transversal board direction compared to the longitudinal direction.

Applying these results to the assembled flip chip interconnections, the risk of bulk cracking at the edges e_2 and e_4 is higher than that at e_1 and e_3.

Concerning delamination risk between board and adhesive, the ERR and mode-mixity strongly depend on the CTE-mismatch, as shown in Fig. 9.12. The higher the CTE-mismatch, the higher the ERR and the lower the mode-mixity. This translates to a higher delamination risk at the edges e_1 and e_3. The mismatch in Young's modulus plays a minor role.



(a) Energy Release Rate G

(b) Mode-mixity ψ

Fig. 9.12: Delamination risk between adhesive and substrate as function of molding direction, Fig. 9.11a; higher risk of delamination for edges e_1 and e_3 because of the smaller CTE-mismatch for the transversal board orientation

9.2.5 Adhesive Material Properties

The adhesive in a flip chip interconnection converts shear stresses at the bumps to bending of the whole package. The amount of bending depends on the CTE-mismatch of the board and the silicon die. The adhesive transfers the stress and strain as an interlayer from the die to the board. The more rigid the adhesive layer, the better the coupling of the stresses and the strain. On the other hand, using quite flexible adhesives, e.g. silicone, the contraction/expansion of the board can be decoupled from the die.

In order to obtain a general statement concerning the impact of the material properties of the adhesive, the Young's modulus E and CTE α are changed independently, Fig. 9.13. Nevertheless, E and α are related for a polymer.

Although the material behavior of the underfills used is visco-elastic, linear-elastic material behavior is assumed for the general investigation of the impact. For a detailed comparison of the experimentally assembled flip chip interconnection, the visco-elasticity is taken into account. In the case of linear-elasticity, an averaged CTE $\overline{\alpha}$ over the temperature range of 150 °C to -40 °C is calculated. The values are listed in Tab. 5.4. An averaged CTE value $\overline{\alpha}$ has

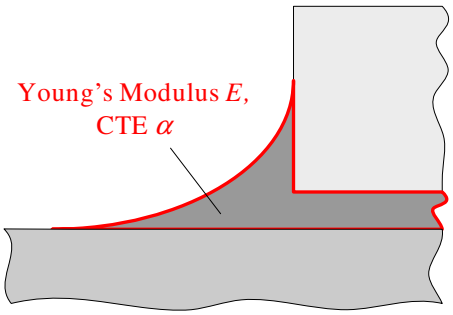


Fig. 9.13: Variation of E and α of the adhesive

the advantage that the different values of the α above/below glass transition temperature T_g as well as the T_g itself can be included.

Concerning failure criterion I, bulk cracking in the upper fillet, the location of the maximum principle stress does not change for different material properties of the adhesive. This leads to the assumption that the location is geometrically determined. The stress intensity factor for a bulk crack for different material properties of the adhesive is shown in Fig. 9.14.

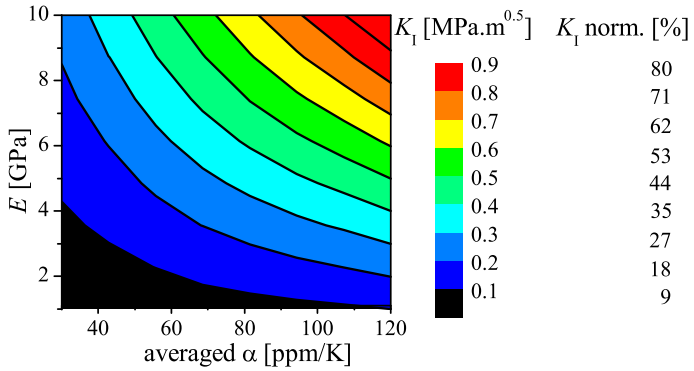


Fig. 9.14: Stress Intensity Factor as a function of adhesive properties Young's modulus E and averaged CTE $\overline{\alpha}$; since a general study of the impact of the adhesive material is performed, the absolute stress intensity factor K is calculated (left caption); nevertheless, in order to be able to judge the influence of the adhesive properties, the fracture toughness K_{Ic} of UF1 is used to calculate a normalized stress intensity factor $\overline{K}_I$ (right caption)

The lower the coefficient of thermal expansion and Young's modulus, the lower the stress intensity factor of a crack in the fillet. This is due to the fact that a higher CTE value leads to a higher contraction of the adhesive. On the other side, a higher Young's modulus of the adhesive leads to higher stresses and therefore higher stress intensity factors.

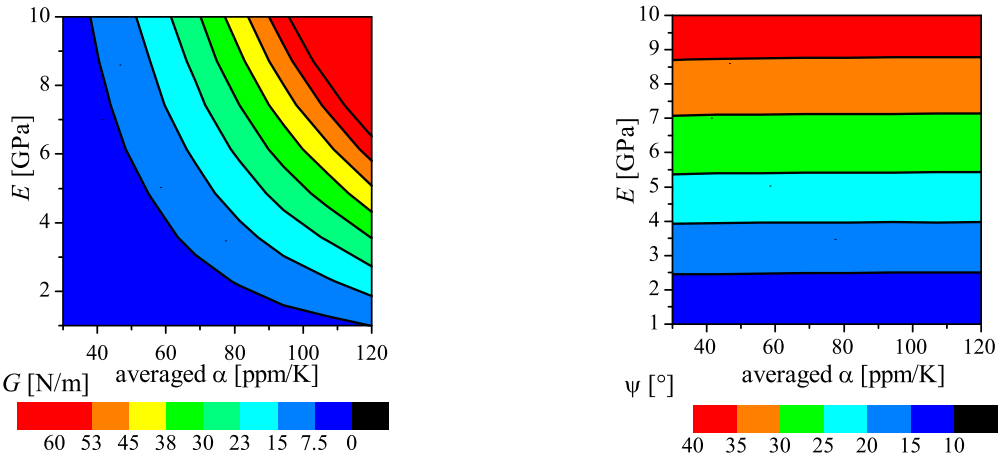
In order to give a ranking of the used underfills and NCAs, the stress intensity factor K_I is computed using Finite Element analysis, Tab. 9.1. Using the measured critical stress intensity factor K_{Ic}, Tab. 6.1, the normalized stress intensity factor $\overline{K}_I$ is obtained. It reveals, that

the NCA1 shows the highest K_{I} as well as the lowest K_{Ic} which leads to a high risk of bulk cracking compared to the other adhesives.

Tab. 9.1: Normalized stress intensity factor for the studied adhesives for the same geometry parameters and board properties; calculation of $\overline{K}_{\mathrm{I}}$ based on the stress intensity factor from the FE analysis K_{I} divided by the measured critical stress intensity factor K_{Ic} from Tab. 6.1

Adhesive	**UF1**	**UF2**	**NCA1**	**NCA2**
K_{I} from FE analysis [MPa$\sqrt{\mathrm{m}}$]	0.14	0.16	0.25	0.17
K_{Ic}, Tab. 6.1 [MPa$\sqrt{\mathrm{m}}$]	1.1	1.5	0.8	1.0
normalized $\overline{K}_{\mathrm{I}}$ [%]	12.5	10.5	31.6	17.2

Concerning the delamination between board and underfill, the higher the CTE and Young's modulus of the underfill, the higher the energy release rate, Fig. 9.15a.



(a) Energy Release Rate

(b) Mode-mixity

Fig. 9.15: Impact of material properties of the adhesive on the failure criterion II; for this general study, linear-elastic material property are assumed; detailed discussion about the actually assembled flip chip interconnection in Section 9.4; the substrate material used has a Young's modulus of about 15.7 GPa and CTE value lies around 7.5 ppm/K

ERR arises due to a CTE-mismatch between board material and underfill which overlies a difference in Young's modulus. Nevertheless, for an interfacial crack, the mode-mixity has to be taken into account when studying the impact of underfill material, Fig. 9.15b. The Young's modulus has a strong influence on the mode-mixity. The smaller the difference of Young's modulus of board and adhesive material, the higher the portion of shear stresses in the interfacial crack (the higher the mode-mixity).

For a flip chip interconnection with the same geometry parameters and substrate properties, the delamination risk is calculated for the used adhesives, Tab. 9.2. NCA1 shows the highest

ERR G whereas UF2 shows a small ERR. The mode-mixities of the used materials are in the similar range. Therefore, it can be stated that also for the risk of delamination, NCA1 shows the highest value.

Tab. 9.2: ERR and mode-mixity for the studied adhesives based for the same geometry parameters and board properties; NCA1 shows the highest risk of delamination; the mode-mixity of the used materials are in the same range

Adhesive	**UF1**	**UF2**	**NCA1**	**NCA2**
ERR G [N/m]	1.4	0.9	2.6	1.4
Mode-Mixity ψ [°]	16	15.7	16.3	15.6

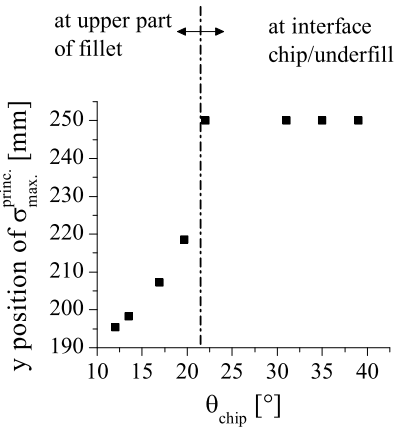
9.2.6 Wetting Angle

The fillet shape is influenced by the amount of applied adhesive for underfilling or dispensing process. Moreover, the surface tension of the LCP substrate plays a key role concerning the shape of the fillet: the higher the surface tension, the higher the spreading of the adhesive, the smaller the wetting angle $\theta_{\text{substrate}}$. The wetting angle at the chip θ_{chip} is more influenced by the flow properties of the adhesive itself.

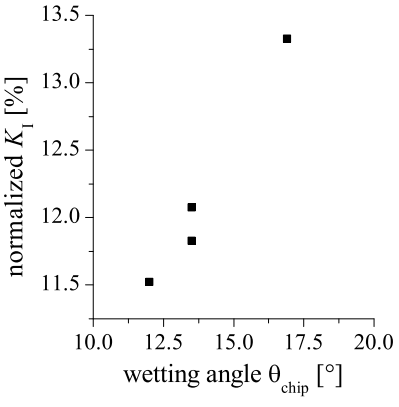
The wetting angle $\theta_{\text{substrate}}$ for the assembled flip chip interconnection lies between 5 and 40 degrees, while θ_{chip} is in the range of 10 and 40 degrees for the different adhesives and substrate surfaces.

In order to distinguish between the impact of different parameters, all parameters of the representative flip chip interconnection in Fig. 9.3 are used as described, except for the fillet shape. The fillet shape in the first investigation is changed only in wetting angles $\theta_{\text{substrate}}$ and θ_{chip}. Afterwards, the fillet length and height are altered. The warpage of the chip is mostly influenced by the thermal expansion and rigidity of the board. A small influence is observed for the properties of the adhesive. No impact of the fillet shape on the chip warpage is detected.

In order to determine the location of crack initiation in the fillet, the maximum principle stresses $\sigma_{\text{max.}}^{\text{princ.}}$ is calculated. The position of the maximum principle stresses as function of the fillet height is shown in Fig. 9.16a. The fillet height is 250 μm.



(a) y-position of $\sigma_{\text{max.}}^{\text{princ.}}$ for different wetting angles chip/underfill



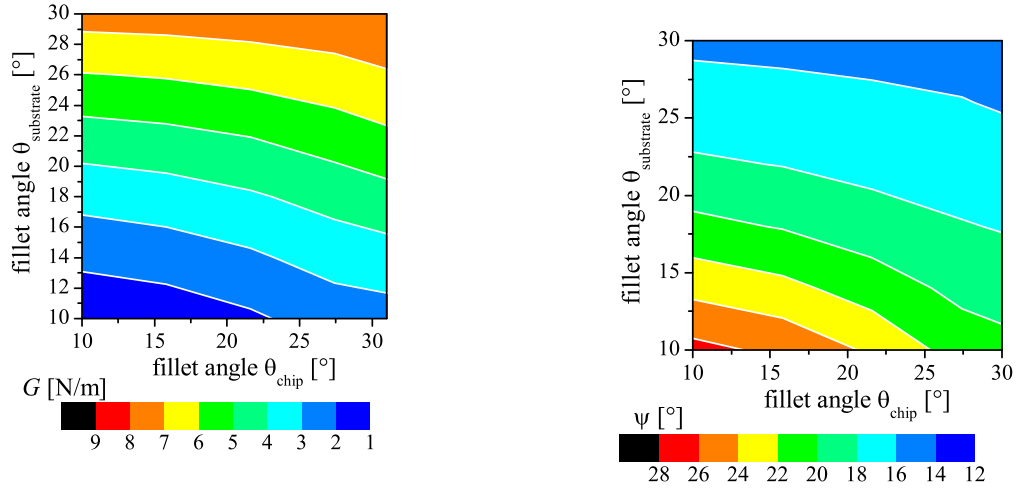
(b) Stress intensity factor as function of wetting angles θ_{chip} below 22°

Fig. 9.16: Influence of wetting angle θ_{chip} on the position of the maximum stresses $\sigma_{\text{max.}}^{\text{princ.}}$ and the resulting stress intensity factor for a crack modeled at that location; maximum stress moves along the fillet until it reaches the vertical chip edge; the maximum is located at the vertical chip edge for wetting angles higher than 22°, where no stress intensity factor can be calculated

The position of $\sigma_{\text{max.}}^{\text{princ.}}$ moves with increasing θ_{chip} towards the vertical chip edge. At an angle of approximately 22°, the maximum stress is located at the vertical chip edge - in the interface between the vertical chip edge and the underfill. Therefore, a bulk crack in the fillet can only be modeled until a wetting angle θ_{chip} of 22°.

Fig. 9.16 shows $\overline{K_{\text{I}}}$ as function of the wetting angle θ_{chip}. The greater the wetting angle, the higher the stress intensity factor, due to the greater influence of the chip edge when approaching the vertical chip edge.

The maximum principle stresses at the lower fillet end lies independent of the fillet shape in the interface between the substrate and underfill. For a modeled delamination, the Energy Release Rate as function of the wetting angle $\theta_{\text{substrate}}$ and θ_{chip} is shown in Fig. 9.17a. It can be stated that the ERR is strongly influenced by the wetting angle $\theta_{\text{substrate}}$, where θ_{chip} shows a minor influence. This originates from the local character of the delamination limited to the region at the lower part of the fillet. Taking $\theta_{\text{chip}} = 20°$ in Fig. 9.17, the strong dependency of ERR as well as the mode-mixity from the wetting angle between underfill and board becomes more visible, Fig. 9.18b.



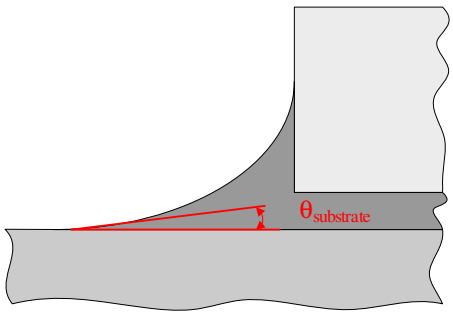
(a) Energy Release Rate strongly influenced by wetting angle $\theta_{\text{substrate}}$

(b) Mode-mixity

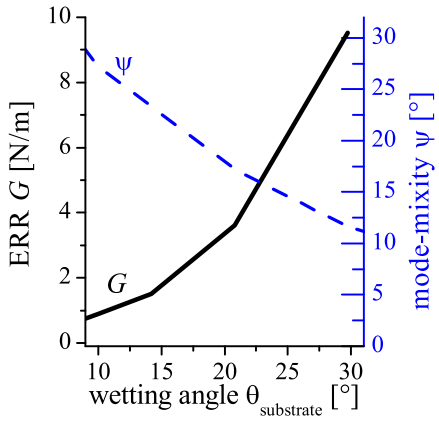
Fig. 9.17: Correlation stress intensity factor K_{I} and energy release rate G and wetting angles $\theta_{\text{substrate}}$ and θ_{chip}

ERR increases greatly for higher wetting angles where the mode-mixity decays. A smaller ψ can be equalized with a higher portion of tension stresses in comparison to shearing stresses in the interfacial crack. Moreover, the increasing G is due to the fact that for increasing wetting angles $\theta_{\text{substrate}}$ more underfill material is present. This phenomenon is equivalent to the two-layered beam in Fig. 7.15. Hereby, the two layers are a LCP substrate and an underfill, where G and ψ are calculated for an increasing underfill thickness. In summary, the

lower the wetting angle $\theta_{\text{substrate}}$, the lower the risk of delamination between the substrate and the underfill.



(a) Impact study of wetting angle between substrate and underfill $\theta_{\text{substrate}}$



(b) ERR and mode-mixity as function of wetting angle

Fig. 9.18: Energy Release Rate and mode-mixity as function of wetting angle $\theta_{\text{substrate}}$; wetting angle θ_{chip} is kept constant at 20°; this graph is extracted from Fig. 9.17; it shows clearly that the delamination risk can be reduced dramatically by lowering the wetting angle $\theta_{\text{substrate}}$

9.2.7 Fillet Height and Width

In addition to the wetting angle, the fillet height and width are design parameters influenced by the dispensing process, as well as of the surface treatment of the board, Fig. 9.19. In order to study the influence of the fillet dimensions, the wetting angles are kept constant.

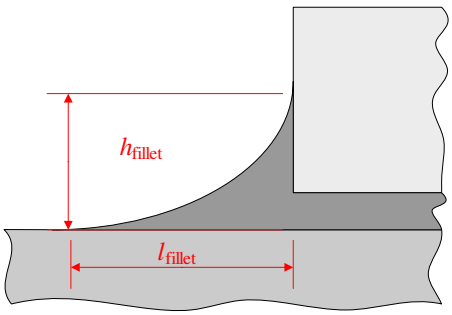
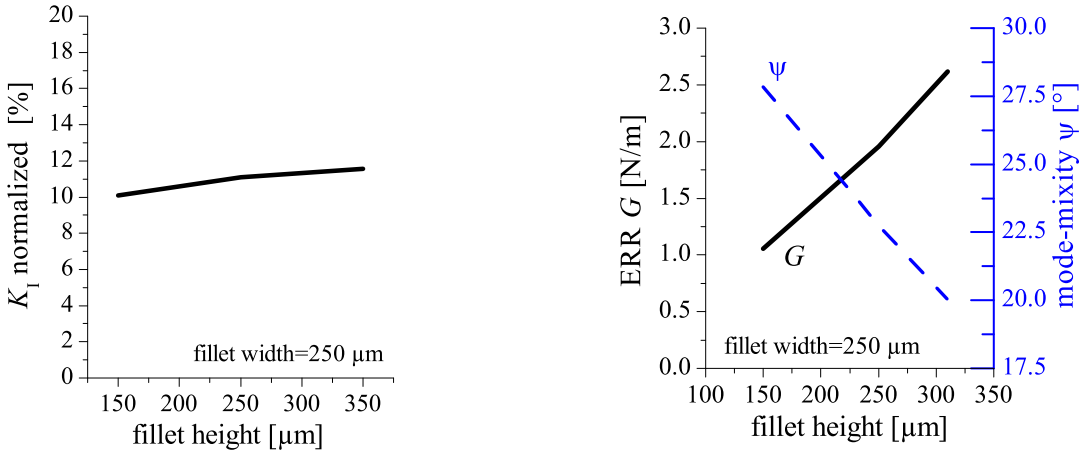


Fig. 9.19: Studying the impact of fillet height and width on the failure criteria

The fillet width is varied between 150 and 450 μm whereas the studied fillet heights are 150, 250 and 350 μm. Fig. 9.20a shows the impact of the fillet height on bulk cracking. The greater the fillet height, the higher the risk of bulk cracking in the fillet is. This can be explained by the increased coupling of chip and adhesive for greater fillet heights.



(a) Bulk Cracking

(b) Delamination

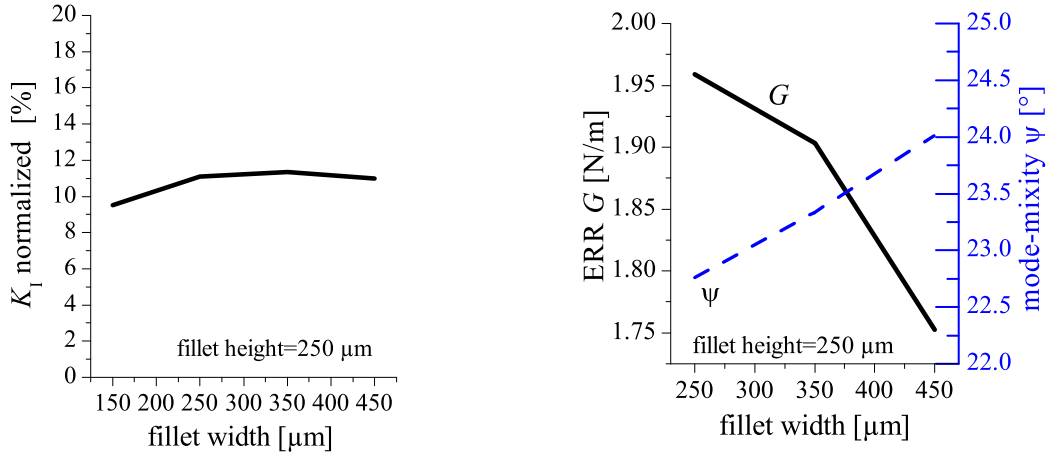
Fig. 9.20: Impact of fillet height on the risk of bulk cracking and delamination; the more the vertical chip edges are covered by the adhesive, the higher the risk of bulk cracking; moreover, the delamination risk is also higher for increasing fillet height

For a fillet height of 150 μm, the vertical chip edge is covered with only 85 μm adhesive, whereas for a fillet height of 350 μm, almost the complete vertical chip edge is covered with adhesive[1].

The delamination risk also increases for higher fillet heights, Fig. 9.20b. The higher the fillet, the more adhesive material in the fillet. This leads to higher contraction of the adhesive and also a higher portion of tensile stress in the interfacial crack.

[1]The stand-off between the chip and the substrate is 65 μm. The fillet height is measured from board surface.

The impact of the fillet width on K_I shows similar dependency on the fillet height. The more adhesive material in the fillet, the higher the stress intensity factor, Fig. 9.21a. On the other side, Fig. 9.21b shows that a greater fillet width leads to reduced delamination risk due to less adhesive directly above the delamination. This also explains the increasing mode-mixity for greater fillet widths.



(a) Bulk Cracking

(b) Delamination

Fig. 9.21: Influence of fillet width on the two failure criteria studied; the larger the fillet width, the lower the risk of delamination and bulk cracking in the fillet is.

9.3 Summary of Parameters Influencing Failure Criteria

In the previous sections, the impact of certain design parameters on the failure criteria are studied. Hereby, the parameters are varied in a wide range. In order to compare the impact of these parameters on the fillet cracking and delamination risk, each parameter is changed by +25 % in respect to the representative flip chip interconnection, displayed in Fig. 9.3. For example, the coefficient of thermal expansion of the adhesive is increased by +25 % from 44 ppm/K to 55 ppm/K. This leads, in the case of fillet cracking, to an increase of about the same value: +26.7 %. Whereas the impact of the adhesive CTE on delamination risk even increases by about 70 %. The change in mode-mixity has to interpreted differentially. Decreasing mode-mixity of a delamination equals a higher portion of tensile stress. As shown in Fig. 6.13, the bearable tensile stress is much lower than the bearable shear stress. Therefore, a decreasing mode-mixity leads to a higher risk of delamination.

In summary, it can be stated that the CTE value of the adhesive, the Young's Modulus, as well as the wetting angle θ_{chip} show significant impact on fillet cracking. Whereas the chip size, board properties and fillet shape (besides the already mentioned wetting angle θ_{chip}) have negligible influence on the risk of cracking in the fillet. Concerning delamination risk between the underfill and substrate, the board Young's Modulus, the properties of the adhesive, the wetting angles, as well as the fillet width have an impact on interfacial cracking.

It is essential to mention that for all studied parameters, an increase of the varied parameters leads for both failure criteria used to a higher risk. Therefore, a lower CTE value of the adhesive, a less rigid adhesive, as well as a fillet shape with small wetting angles θ_{chip}, $\theta_{\text{substrate}}$ and small fillet width can be used to achieve lower risk of failure.

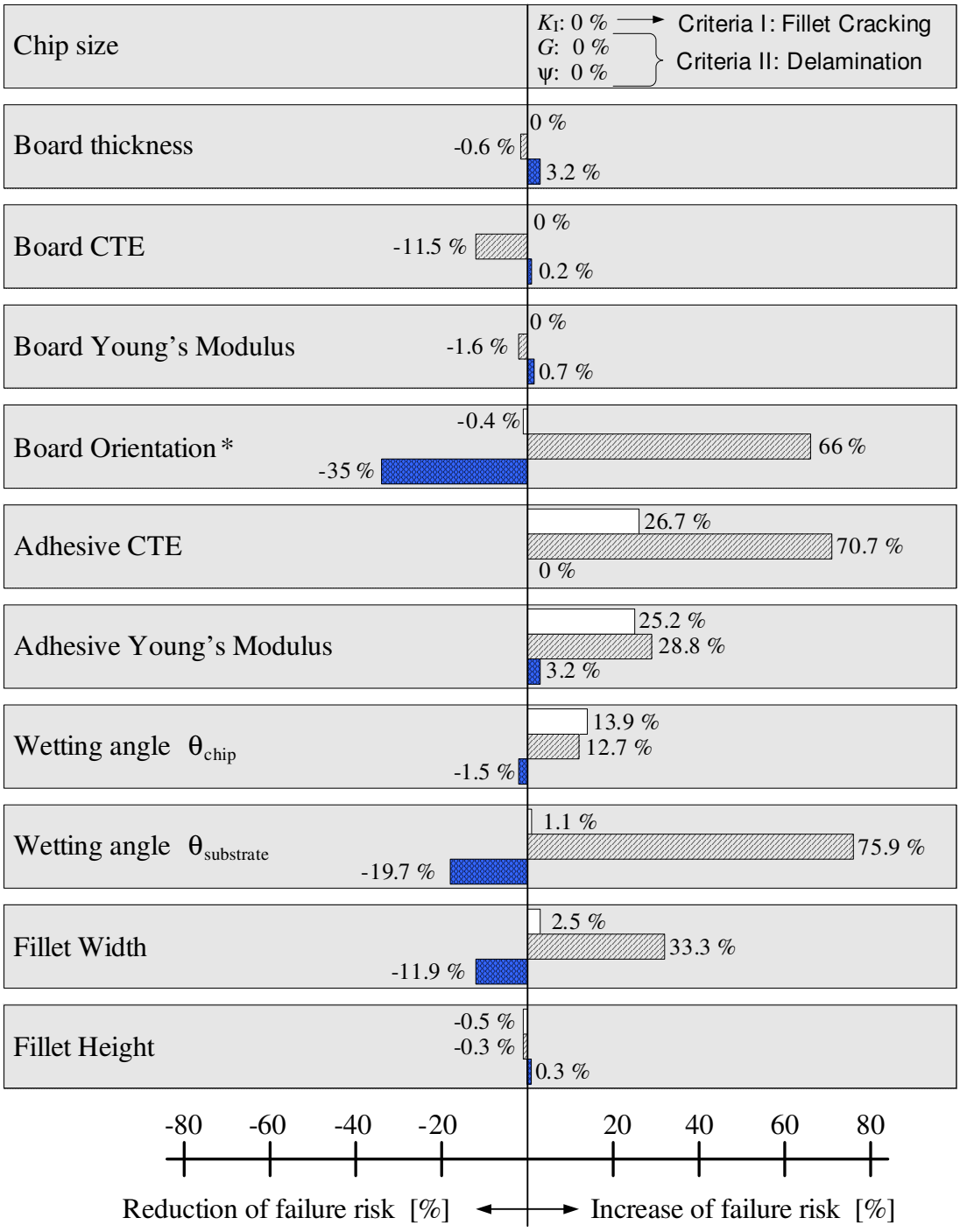


Fig. 9.22: Summarization of impact of geometric features and material properties on the two failure criteria: K_I and G, ψ; the impact is separated in reduction and increase of failure risk in respect to the representative flip chip assembly, displayed in Fig. 9.3; it is assumed that the parameters are varied by +25 %; for bulk cracking in the fillet, the material properties of the adhesive as well as the wetting angle θ_{chip} have the largest impact; concerning delamination risk, the adhesive CTE as well as the wetting angle $\theta_{\mathrm{substrate}}$ leads to a dramatically increase of delamination risk by over 70 %; therefore, it can be summarized that a reduction of the CTE of the adhesive has a positive effect on both failure criteria; $*$ change of board orientation by 90 degrees

9.4 Results for Experimentally Assembled Flip Chip Interconnections

In chapter 8, the flip chips, boards and adhesives used are listed and the assembly process is described. Depending on the surface treatment and the specific underfill, different fillet shapes are present for the various assemblies. As previously shown, the geometry and the material properties show certain influence on the failure criteria I and II. In order to provide a ranking of the assembled flip chip interconnections with respect to the failure criteria, the assembled interconnections are modeled. The normalized stress intensity factor, as well as the ERR and mode-mixity for the two failure mechanisms, are obtained.

The calculated stress intensity factors K_{I} are smaller than the critical stress intensity factor K_{Ic}. The underfills and NCAs have different K_{Ic} values as listed in Tab. 6.1. Therefore, the comparison based on failure criterion I is performed on the normalized $\overline{K_{\mathrm{I}}}$, Eq.(9.1).

The numerical studies of the failure modes show a great impact by the fillet formation. Due to manufacturing tolerances, the fillet shape is not constant within in one single batch, Fig. 8.14 and 8.15. This leads to a range of stress intensity factor K and ERR G within a single flip chip assembly.

Fig. 9.23 shows the average of the $\overline{K_{\mathrm{I}}}$ as well as the maximum and minimum value. The flip chip assemblies with NCA1 show the highest risk of fillet cracking.

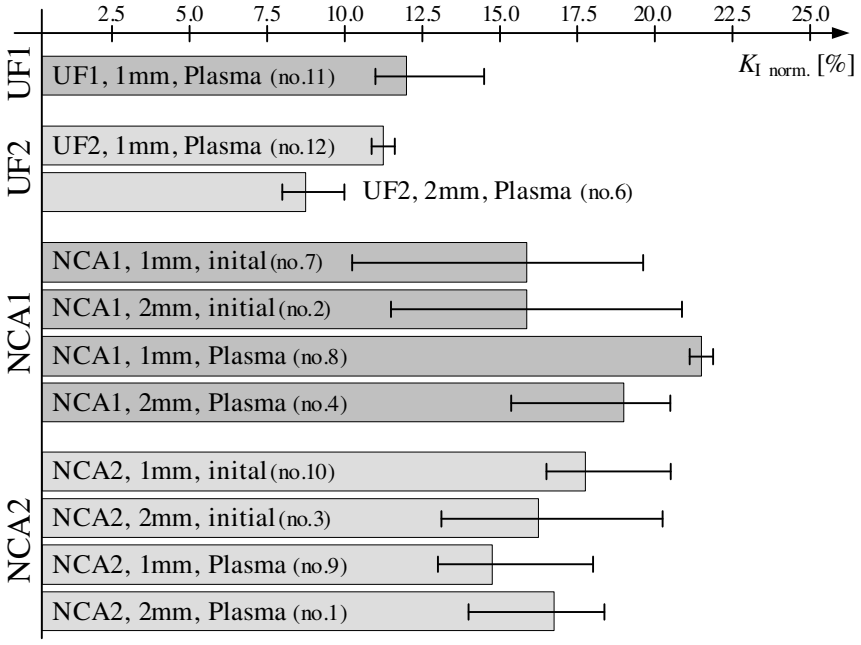


Fig. 9.23: Failure Criterion I: Crack in upper part of fillet; normalized stress intensity factor $\overline{K_{\mathrm{I}}}$ for the assembled flip chip interconnections

The risk of delamination between the substrate and the adhesive is described by failure criterion II. The energy release rate G and the phase angle ψ are used to quantify the delamination risk. Fig. 9.24 to Fig. 9.26 show G and ψ for the assembled flip chip interconnections. Hereby, each symbol represents a single flip chip interconnection. The mode-mixity of most flip chip interconnections are between 17° and 27°. Only the flip chips interconnections *no.2* show a much higher mode-mixity. The higher the phase angle ψ, the higher the critical ERR, the lower the delamination risk. The energy release rate varies between 0.05 N/m and 4.2 N/m. Based on the characterization of the interface LCP/adhesive, e.g. shown in Fig. 6.13, the lower the mode-mixity, the smaller the bearable energy release rate. Therefore, it can be stated that the flip chip interconnections of type *no.7* show a high risk of delamination, Fig. 9.25.

Whereas for the flip chip interconnections using capillary underfill, (*no.6,no.11,no.12*), the risk of delamination is small, Fig. 9.24.

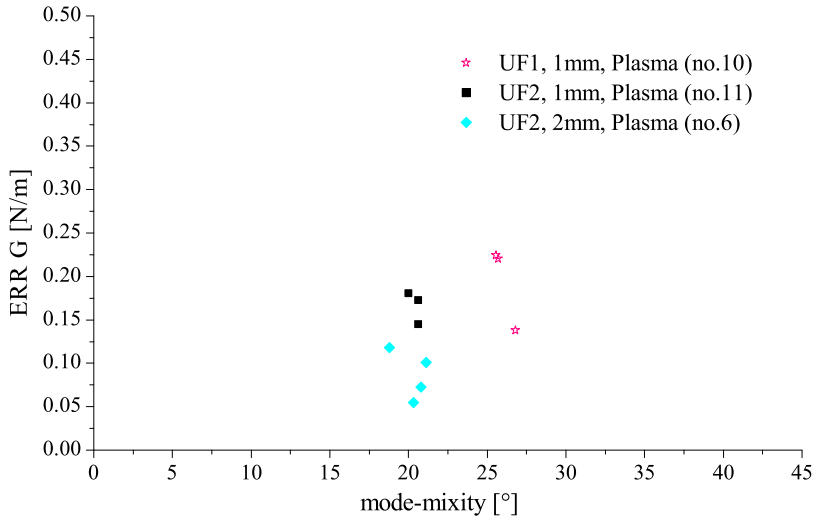


Fig. 9.24: Failure Criterion II: Delamination risk for flip chip interconnections using capillary underfill; each symbol represents a single flip chip interconnection; the delamination risk is quite small compared to some of the interconnection where NCAs are used; this can be explained by the small wetting angle between the underfill and substrate; the wetting angle is strongly influenced by the surface treatment: plasma treatment reduced dramatically the wetting angle; for all assembled interconnection with capillary underfill, plasma treatment is applied

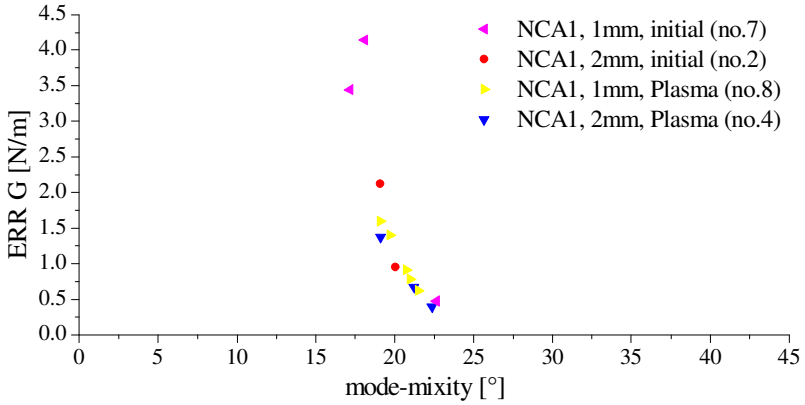


Fig. 9.25: Failure Criterion II: Delamination LCP substrate/NCA1; high risk for flip chip interconnection on 1 mm LCP board, without plasma treatment; this is due the fact that the wetting angle $\theta_{\text{substrate}}$ for these flip chip interconnections is much higher

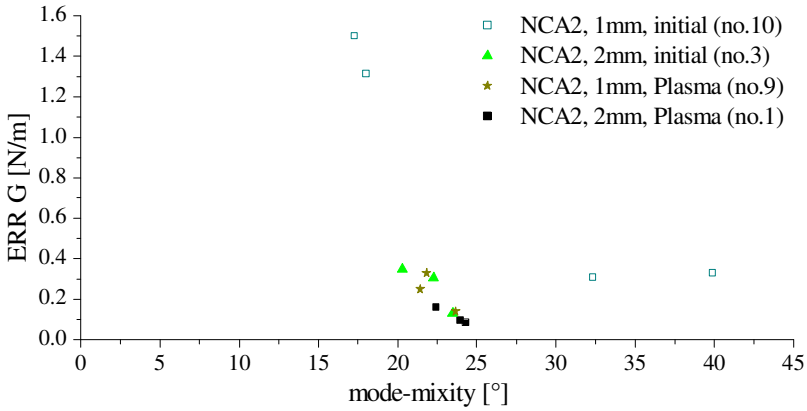


Fig. 9.26: Failure Criterion II: Delamination LCP substrate/NCA2; delamination risk is lower compared to interconnections using NCA1 which can be explained by the difference in fillet shape; it can be also seen that the variation within one batch is quite high, e.g. *no.10*

Chapter 10

Experimental Verification

10.1 Objective of Experimental Reliability Testing

Two different mechanisms are proposed to lead to failure of SBB flip chip interconnections when exposed to thermal cycling: in the previous chapter, Finite Element Analysis is carried out to identify these failure mechanisms.

In this chapter, these predicted failure mechanisms are verified experimentally. Fifteen variants of flip chip interconnections are assembled and tested where geometry and material properties are altered. The different variants are listed in Tab. 8.1.

10.2 Procedure of Reliability Testing and Failure Definition

10.2.1 Thermal Cycling

The flip chip interconnections are exposed to thermal cycling between 150 °C and -40 °C. The testing is performed in a three chamber thermal shock oven. The temperature profile is shown in Fig. 10.1. The dwell time at both temperatures is 15 minutes.

Every 250 thermal cycles, the flip chip interconnections are inspected outside the temperature chamber:

- measurements of electrical transition resistance of the Stud Bump interconnections as well as the conductor path of the MID substrate

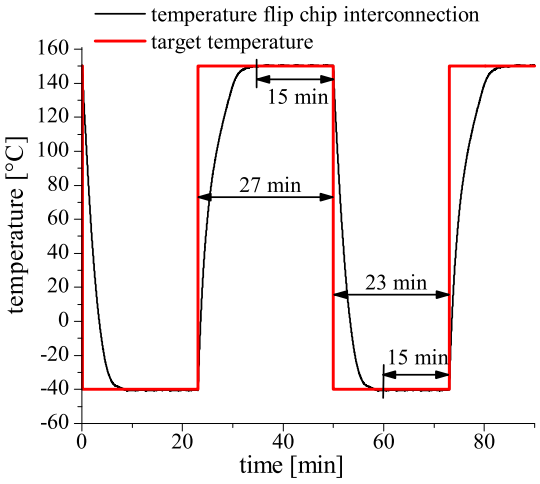


Fig. 10.1: Temperature profile of thermal shock testing of the flip chip interconnections; the temperature is measured between the chip and substrate by a thermocouple; the storage time is chosen in a way that the dwell time is 15 minutes for the upper and lower temperature; since the cooling down takes place in a shorter time, the thermal cycles for the lower and upper temperature are different

- Acoustic Microscopy Measurement (SAM) to account for delamination in interfaces substrate/underfill and underfill/chip passivation
- optical inspection of the fillet to observe fillet cracking and delamination

10.2.2 Failure Definition

Reliability testing is performed until all interconnections showed one kind of crack initiation in the fillet. Monitoring of electrical transition resistance of the bumps as well as SAM measurements are carried out to account for further failure mechanisms other than those proposed.

10.3 Experimental Verification of Failure Modes

10.3.1 Experimentally Observed Failure Mechanism

The reliability testing is carried out until 3000 cycles are reached where the most combinations showed crack initiation in the fillet. No electrical failure or delamination between substrate/adhesive and chip/adhesive originating at the bumps are detected.

Depending on the adhesives used, SBB technology and surface treatment of the LCP substrate, the tested flip chip interconnections showed the two proposed failure mechanisms at three different locations:

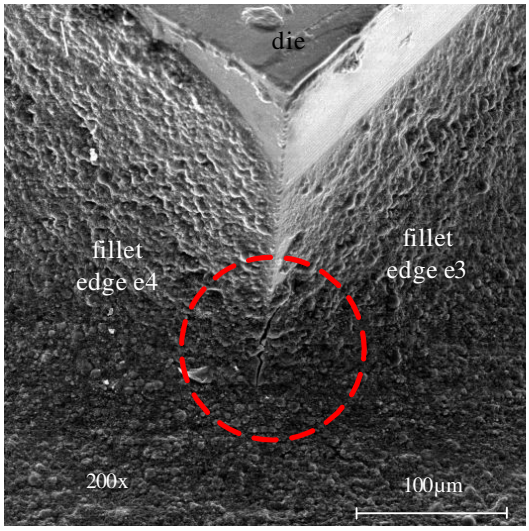
- Bulk cracking in upper part of the fillet, starting in the corners e_1, e_2, e_3 and e_4, compare Fig. 10.3
- Bulk cracking also in upper part of fillet, but starting point of cracking at center of chip edge e_2 and e_4, Fig. 10.5
- Delamination between LCP and adhesive, initiation at vertices e_1 and e_3, Fig. 10.9

Additional to the described failure mechanism horizontal chip cracking for flip chip interconnections on 1 mm LCP boards with 10×10 mm^2 chips and underfill UF1 are detected. The chip cracking occurred within in the first 100 cycles. These failures are considered to be early failures and are therefore not considered.

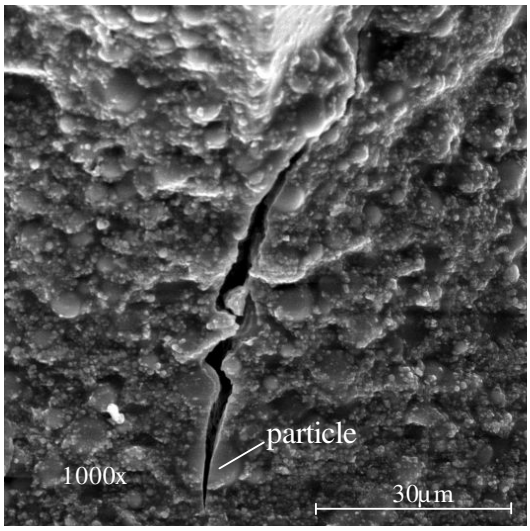
The detected failures are first generally described. Then, the failures are listed for all assembled flip chip interconnections.

10.3.2 Bulk Cracking, Initiating at Corner fillet

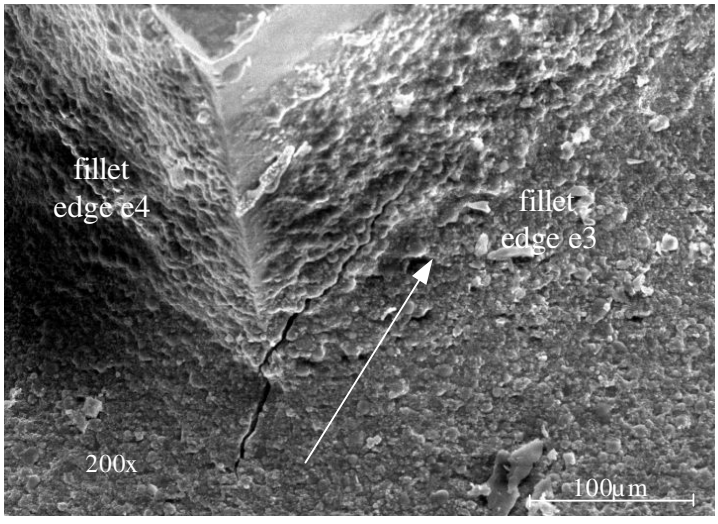
For certain combinations, bulk cracking originating at the die corner is detected, Fig. 10.2a-c. The cracks are detected firstly after 500 thermal cycles. They initiate along the fillet at the die corner, at an angle of about 45°. The crack goes through polymer matrix as well as filler particles, Fig. 10.2b. These locations show the highest stresses because the distance is $\sqrt{2}$ times higher than to the edges e_1 to e_4. After exposed to further cycles, the crack propagates in direction of edge e_1 or e_3.



(a) Vertical crack in fillet at die corner: 500 cycles (sample 1: UF2)



(b) Detail of a: cracks within particle (sample 1: UF2)



(c) Crack propagation along edge e_3: 1500 cycles (sample 2: UF2)

Fig. 10.2: Crack in fillet at die corner; cracking initiates vertically at chip corner; crack propagation along edge e_1 or e_3

In Fig. 10.3, the position of crack initiation is sketched as well as the path of crack propagation. The crack propagation, displayed in Fig. 10.2c, is caused by a three-dimensional loading of the crack. In the present study, a two-dimensional FE model is used to represent the flip chip interconnection, as shown in the sketch Fig. 10.3. Therefore, the model used is not capable to study that kind of crack propagation. The two-dimensional modeling is chosen in order to perform a parametric study of the flip chip assembly and study the crack initiation rather than the crack propagation. As mentioned, a flip chip assembly is considered to have failed once a crack or delamination is detected.

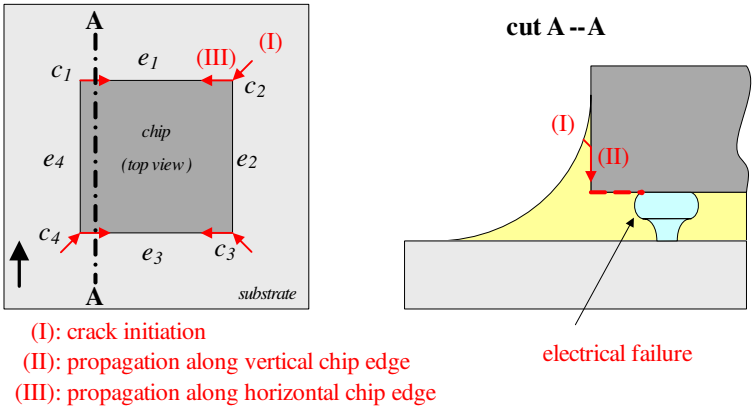
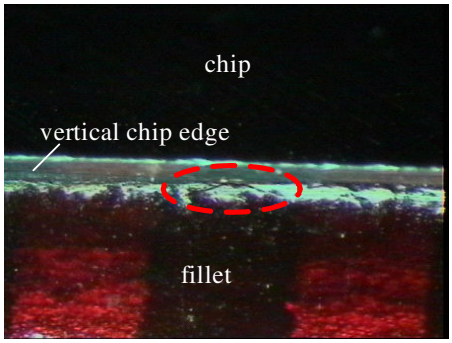


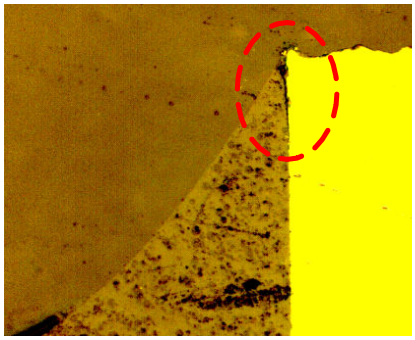
Fig. 10.3: Corner Crack in Fillet at corners c_1 to c_4, assumed propagating along edge e_1 and e_3; Fillet crack: initiation (I) and propagation (II,III) of a crack; propagation (III) along horizontal edge does not lead to electrical failure; it acts as a pre crack for crack propagation path (II); (II) leads to delamination of interface passivation/underfill and therefore to electrical failure of the interconnection; the electrical failure is not detected within the performed cycles

10.3.3 Bulk Cracking, Initiating at Center Fillet

In addition to the corner cracking, crack initiation in the upper part of the fillet is also detected at the middle of the chip edges e_2 and e_4, Fig. 10.4 and Fig. 10.5. The crack propagates within the adhesive, towards the substrate surface.



(a) Crack in fillet at vertical chip edge for flip chip assemblies using NCA1; crack initiation in the middle of edge



(b) Cross sectional cut: bulk cracking in NCA2, which leads to delamination vertical chip edge and NCA

Fig. 10.4: Crack in fillet at vertical chip edge (edges e_2 and e_4); detected for different NCAs

The experimentally detected location of crack initiation in the fillet correlates with the theoretically proposed location. Based on that location, failure criterion I - bulk cracking in the upper part of the fillet - is formulated. Moreover, in the present work, it is theoretically proposed that the risk of fillet cracking (center cracking) is higher along the edges e_2 and e_4, Fig. 9.11. The experimental results also verify this proposal.

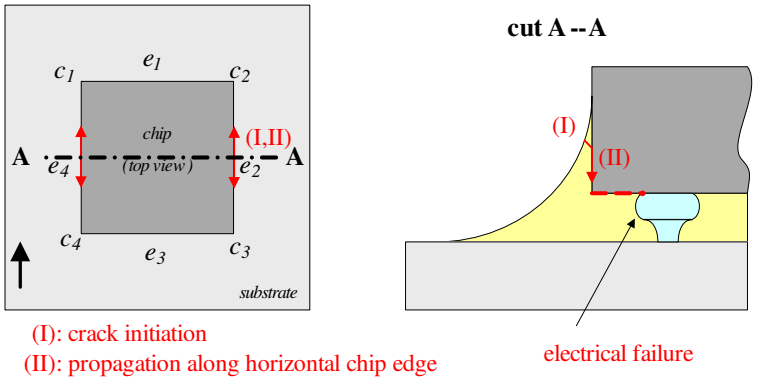
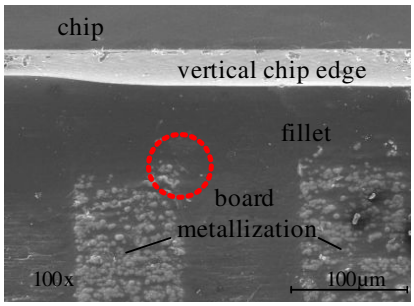


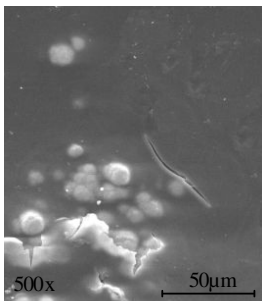
Fig. 10.5: Fillet Cracking originating from center of edge e_2 and e_4

10.3.4 Delamination Between Board and Adhesive

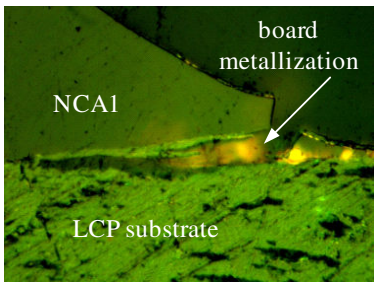
Delamination between the LCP board and underfills or NCAs are detected. Fig. 10.6a-b shows that the crack initiation in the adhesive occurs at the metallization of the MID board.



(a) SEM picture of crack initiation in the lower part of the fillet at metallization of MID board



(b) Detail of a: stress concentration at metallization

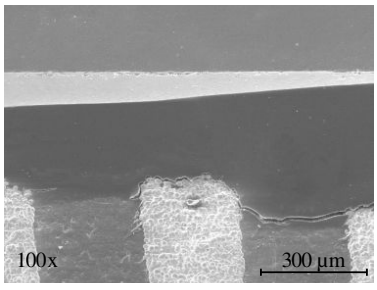


(c) Cross section of crack initiation at metallization of board; delamination within skin of LCP

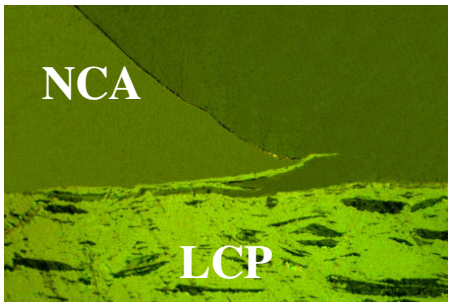
Fig. 10.6: Delamination between board and adhesive; initiation in adhesive at board metallization

The metallization acts as a stress concentration. The crack initiates in the lower part of the fillet, Fig. 10.6c. This initiation is only detected at the edges e_1 and e_3. This can be explained by the higher CTE-mismatch between the adhesive and the board in longitudinal direction, which is displayed previously in Fig. 9.12.

The bulk crack turns to a delamination between the board and the adhesive, Fig. 10.7a. As already seen in the button shear test, the delamination is within the very thin outer skin of LCP, Fig. 10.7b. Because of the weak cohesion of the skin to the layers underneath as well as due to the fact that the adhesion strength shows a strong mode-mixity dependency, the crack is considered to be an interfacial cracking between LCP and the adhesive.



(a) SEM image of delamination propagation after crack initiation, Fig. 10.6



(b) Cross section of delamination propagation; cracking lies within the LCP skin

Fig. 10.7: Delamination propagation

The delamination propagates along the edges e_1 and e_3 as well as towards the chip center, Fig. 10.8. The latter is critical because it can lead to electrical failure once the delamination

reaches the stud bumps. Delamination propagation along the edges e_1 and e_3 is less critical, because it does not lead to electrical failure.

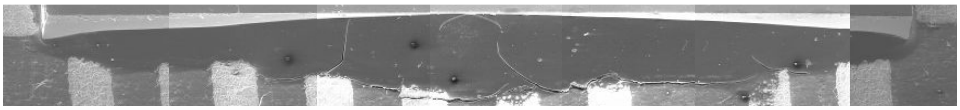


Fig. 10.8: Delamination propagation for an 5×5 mm^2 chip using NCA2; displayed edge: e_1; image consists of several single SEM images

Fig. 10.9 summarizes the crack initiation and delamination propagation for that kind of failure. Moreover, the theoretically proposed failure Mode-II is experimentally verified.

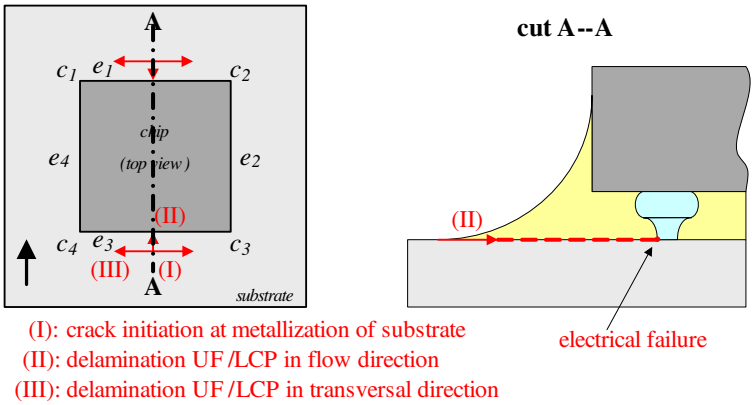


Fig. 10.9: Delamination between board and adhesive originating at edge e_1 and e_3; as for the bulk cracks, electrical failure is not detected within the 3000 cycles

10.4 Correlation of Predicted and Experimentally Detected Failure Mechanism

The predicted failure mechanisms based on two-dimensional Finite Element simulation are cracking in the upper part of fillet and delamination between the adhesive and the board.

The experimental reliability studies verify the proposed failure mechanisms. The bulk fillet crack initiation occurs in the center of the die edge as well as in the corner. The latter failure also leads after initiation to a center crack. In addition to the bulk crack in the upper part the fillet, the delamination between the board and adhesive is also experimentally detected.

In Tab. 10.1, the tested flip chip interconnections and the detected failure mechanisms after reliability testing are listed.

Tab. 10.1: List of flip chip interconnections and detected failure mechanism after reliability testing; due the local character of the failure mechanism, fillet cracking and delamination can be present simultaneously.

Adhesive	**Board Thickness**	**Surface**	**Chip Size** [mm^2]	**No.**	**Fillet Crack**		**Delamination**
					corner crack	center crack	delamination
UF1	1 mm	plasma	10×10	A	x		
UF1	2 mm	plasma	10×10	B	x		
UF1	1 mm	plasma	5×5	11	x		
UF2	1 mm	plasma	10×10	C	x		
UF2	2 mm	plasma	10×10	D	x		
UF2	1 mm	plasma	5×5	12	x		
UF2	2 mm	plasma	5×5	6	x		
NCA1	1 mm	initial	5×5	7			x
NCA1	2 mm	initial	5×5	2		x	x
NCA1	1 mm	plasma	5×5	8		x	x
NCA1	2 mm	plasma	5×5	4	x		
NCA2	1 mm	initial	5×5	10	x		x
NCA2	2 mm	initial	5×5	3	x		
NCA2	1 mm	plasma	5×5	9	x		
NCA2	2 mm	plasma	5×5	1	x		

For certain combinations, only one failure mechanism occurs whereas for others fillet cracking

and delamination lead to failure. Concerning fillet cracking, either corner cracking or center cracking is detected. As stated in Fig. 9.2 from a theoretical point of view, delamination and fillet cracking can be present simultaneously, which was then experimentally verified.

For combination *no.7* – NCA1, board thickness of 1 mm, no surface treatment – the only failure mechanism detected is delamination between substrate and adhesive. For all other combinations for which interfacial cracking occurred, a fillet crack is also present.

The occurrence of a failure depends on the existing stress intensity factor for a crack in the upper part of the fillet or the combination ERR,ψ for a delamination. Fig. 10.10 shows the normalized stress intensity factor $\overline{K_{\mathrm{I}}}$ and ERR for the assembled flip chip interconnections. The detected failure mechanisms are shown as different colored cells. For both failure modes, the values from FE analysis are divided into four ranks: *low*, *middle*, *high* and *very high*. The corresponding values for $\overline{K_{\mathrm{I}}}$ and ERR are shown in the lower left corner. For example, the ranking *low* indicates that the $\overline{K_{\mathrm{I}}}$ is between 0 and 5 % of the critical value, where for *very high* the values are above 15 %. For almost all flip chip interconnections, bulk cracking is detected. The $\overline{K_{\mathrm{I}}}$ from FE analysis are ranked as *middle* to *very high*. Therefore, bulk cracking in the upper part of the fillet occurs if the $\overline{K_{\mathrm{I}}}$ is equal or higher to 8 % of the critical value obtained from CT testing at -40 °C. The calculated $\overline{K_{\mathrm{I}}}$ values for the flip chip interconnections are shown in Fig. 9.23. Since only crack initiation is monitored, it is not possible to distinguished between the different ranks.

The delamination risk is characterized by the ERR. The ranks go from *low* to *very high*. Flip chip assemblies where the ERR is ranked *low* did not show delamination initiation. For the assemblies with an ERR higher than 1 N/m (rank *middle*, *high* and *very high*), delamination initiation is detected. Therefore, a flip chip assembly must designed to have an ERR not higher than 1 N/m.

The flip chip combinations where capillary underfill UF1 and UF2 is used, show only bulk cracking, initiating at the corner. The stress intensity factor lies around 8 to 12 % of the critical value. The energy release rate is quite small compared to the flip chip assemblies *no.2,no.7,no.8* with NCA1. This can be explained by the small wetting angle adhesive/substrate. This conclusion also holds for three of the four NCA2 combinations, as well as for combination *no.4* where NCA2 is utilized.

Nevertheless, for the combinations where NCA1 is used, the normalized stress intensity factor is higher compared to the assemblies with UF and NCA2, but no corner crack occurred. Even for one combination, no bulk cracking at all is detected within the first 3000 thermal cycles. This can be explained by the lower risk of crack initiation due to the absence of filler particle in NCA1 whereas UF1, UF2 and NCA2 are filled with spherical particles, refer to Tab. 5.2.

The higher the wetting angle, the higher the energy release rate, the higher the risk of

delamination between adhesive and substrate. This is clearly seen for combination *no.10* - NCA2, 1 mm board thickness and no surface treatment - and combination *no.7* - NCA1, 1 mm board thickness and no surface treatment.

$*$ to Fig. 10.10:
The Stress Intensity factor $\overline{K_{\mathrm{I}}}$ as well as the Energy Release Rate G are calculated and ranked as *low*, *middle*, *high* and *very high*; (1) bulk cracking: 10 of 11 assemblies show bulk cracks in the fillet; $\overline{K_{\mathrm{I}}}$ lies between 8 and 22 %; since almost all combinations show bulk cracking, it can be stated that $\overline{K_{\mathrm{I}}} > 8$ % leads to fillet cracking after 3000 thermal cycles; (2) delamination: the ERR G lies for the interconnections where no delamination is detected below $G = 0.5$ N/m; for the assemblies where delamination occurred, the calculated ERR is higher than $G = 1.1$ N/m; this suggests that in order to prevent delamination initiation, an ERR of $G = 0.5$ N/m should not be exceeded

Fig. 10.10: Correlation of FE-analysis and experimentally detected failures of the assembled flip chip interconnections *

10.5 Conclusion

In order to increase the acceptance of a new packaging technology, it is essential to understand the failure mechanisms and the influencing parameters, to extend the time before the failure takes place. In the presented work, the packaging technology flip chip on MID boards is studied when exposed to thermal cycling. Two different kinds of SBB flip chip technologies are used: ICA with capillary underfill and the NCA technology. Through the presented work, the failure mechanisms for flip chip interconnections on MID boards are identified: bulk cracking in the upper part of the underfill fillet and delamination between the underfill and the MID substrate. Moreover, the influence of certain geometric and material parameters on these failure mechanisms are obtained and experimentally verified. Based on the results of this work, a guideline to optimize a flip chip interconnection on LCP in order to extend the lifetime can be drawn.

- It was found that the SBB flip chip technology used in combination with MID board, made of LCP, is a highly reliable packaging technology. Using requirements set by the automotive industry, such as exposing the assembled flip chip interconnections to thermal cycles between 150 °C and -40 °C, no single electrical failure is detected; it was tested until 3000 cycles.
- The detected failure mechanisms are bulk cracking in the upper part of the fillet and delamination between the underfill and the LCP substrate. Failure originating from the bump area (fatigue of the bump material or delamination caused by contamination from assembly process as known with solder bumped flip chips) was not detected. This can be explained by the fluxless SBB flip process which does not lead to weak adhesion between the underfill and chip passivation. The delamination at the interface underfill/LCP occurred within the different layers of the LCP skin.
- The two failure mechanisms can occur simultaneously as theoretically proposed and experimentally verified.
- It is pointed out that the plasma treatment of the LCP surface plays a significant role for the capillary underfilling process. The surface tension of LCP can be doubled by plasma treatment. The better the surface tension, the better the wettability, the better the capillary underfill flow. Moreover, it could be shown that the increased surface tension by plasma treatment only drops by 4 % within 350 hours (storage at room temperature), which leads to a wide process window. All ICA/capillary underfill flip chip interconnections are assembled on plasma treated LCP boards.
- The fillet formation of the assembled flip chip interconnections are also strongly influenced by the plasma treatment. The interconnection where plasma treatment is per-

formed shows a much lower wetting angles than the interconnections where no plasma treatment was utilized.

- When comparing the different used adhesives, the unfilled system NCA1 shows the highest risk of fillet cracking. This is due to the higher CTE value of NCA1 when considering the calculated stress intensity factor K_{I}. Taking also the critical value K_{Ic} (obtained from isothermal overcritical testing using CT specimens) into account, the risk of fillet cracking for NCA1 is even more pointed out. NCA1 shows the smallest critical stress intensity factor K_{Ic} compared to the other used adhesives. This leads for the same geometry of the fillet and substrate material to a 20 to 30 % higher risk of fillet cracking of a flip chip interconnection where NCA1 is used. Since the fillet formation is different for every adhesive, and the formation shows a very high impact on fillet cracking, the impact of the adhesive properties can not be experimentally verified using flip chip assemblies.

- NCA1 shows also, same fillet formation and other geometric parameters assumed, the highest risk of delamination between the adhesive and LCP substrate when considering a flip chip interconnection. The calculated ERR G for a modeled interfacial crack using NCA1 shows a 40 to 50 % higher risk of delamination compared to the other utilized adhesives. This is can also be explained by the higher CTE value of NCA1.

- The experimentally detected failure mechanisms were initially theoretically proposed based on a detailed Finite Element stress analysis. It was clearly shown that the location of failure can be identified by using the maximum principle stress. Applying the physics-of-failure approach, it was possible to study the impact of certain geometric features and material properties, which are later summarized in a guideline.

- The button-shear-test is modified in order to obtain the adhesion between the underfill and LCP at various mode-mixities. The mode-mixity denotes the ratio of shearing and tensile stress at a crack tip. The test has the advantages that the consumption of expensive underfill material is low, no certain size and shape of the substrate material is required and the mode-mixity can be easily varied by changing the shearing height.

Design Guideline

The experimental testing showed that the assembled flip chip interconnections can withstand more than 3000 thermal cycles without any electrical failure. Nevertheless, the proposed and also experimentally verified failure mechanism will lead to electrical failure after continued testing. Therefore, it is essential to provide a guideline for further improvement of the SBB flip chip interconnection on MID boards.

No improvement of the reliability can be expected from

- changing the size of the flip chip,
- increasing or decreasing the thickness of the board,

A moderate enhancement of the flip chip interconnection and therefore an extension of lifetime can be forced by

- changing the height of the fillet.
- lowering the wetting angle between the underfill and vertical chip edge,
- lowering the fillet width,
- increasing the CTE and the stiffness of the board,
- using an adhesive (underfill or NCA) with a lower Young's modulus.

The highest impact on the failure mechanisms and therefore the reliability of the flip chip interconnection is detected by

- the CTE value of the adhesive; the lower the CTE value, the lower the risk of bulk and interfacial cracking
- the highest impact on delamination risk shows the wetting angle between the substrate and the adhesive. Reducing the wetting angle by 25 % reduces the risk of delamination by more than 75 %. The wetting angle, as stated previously, can be reduced using plasma treatment of the LCP board

10.6 Outlook

The use of the physics-of-failure approach allows also to study of the lifetime of a structure. In the presented work, overcritical testing were used to obtain the critical stress intensity factor and ERR for the bulk cracking and delamination, respectively. In order to provide a method to estimate the lifetime, critical bulk and interfacial toughness values have to obtained by fatigue testing of test specimens. These test methods are so far only available for cycling mechanical loading, but not yet for thermo-mechanical induced loading.

Chapter 11

Abbreviations

CTE	Coefficient of thermal expansion
DMA	Dynamic Mechanical Analysis
DSC	Differential Scanning Calorimetry
ERR	Energy release rate (ERR)
FEM	Finite Element Method
ICA	Isotropic Conductive Adhesive
LCP	Liquid Crystal Polymer
LEFM	Linear elastic fracture mechanics
LPKF	Company name
MID	Molded Interconnect Devices
NCA	Non-Conductive Adhesive
no.	Number
PI	Polyimid
PTFE	Polytetrafluoroethen (Teflon)
SAM	Scanning Acoustic Microscopy
SBB	Stud Bump Bonding
SEM	Scanning Electron Microscopy
TGA	Thermo Gravimetric Analysis
TMA	Thermo Mechanical Analysis
UF	Underfiller
VCCT	Virtual Crack Closure Technique

Chapter 12

Mathematical Notations

α	Coefficient of thermal expansion (CTE)
α_1	CTE below glass transition temperature T_g
α_2	CTE above glass transition temperature T_g
$\overline{\alpha}$	Averaged CTE with respect to α_1,α_2 and T_g
ε	Bimaterial constant
E	Young's Modulus
F_c	Critical shear force (button shear test)
θ_chip	Wetting angle between vertical chip edge and adhesive
$\theta_\mathrm{substrate}$	Wetting angle between substrate and adhesive
G	Energy release rate (ERR)
G_c	Critical energy release rate (ERR)
h	Shearing height (button shear test)
K	Stress intensity factor
K_I	Stress intensity factor Mode-I
K_Ic	Critical stress intensity factor Mode-I
K_II	Stress intensity factor mode II
$\overline{K_\mathrm{I}}$	Normalized stress intensity factor Mode-I
$N_\mathrm{init.}$	Number of cycles at crack initiation
ψ	Mode-mixity
$\sigma_\mathrm{max.}^\mathrm{princ.}$	Maximum principle stresses
s_st	Movement of shear tool (button shear test)
s_stc	Critical movement of shearing tool (button shear test)
T_g	Glass transition temperature

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