GaN-Based HEMTs for High Voltage Operation

Design, Technology and Characterization

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לרבקה ומוטי סמט, אתם נהדרים, תודה על הכל!

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Executive Summary

Gallium nitride (GaN)-based High Electron Mobility Transistors (HEMTs) for high voltage, high power switching and regulating for space applications are studied in this work. Efficient power switching is associated with operation in high OFF-state blocking voltage while keeping the ON-state resistance, the dynamic dispersion and leakage currents as low as possible. The potential of such devices to operate at high voltages is limited by a chain of factors such as subthreshold leakages and the device geometry. Blocking voltage enhancement is a complicated problem that requires parallel methods for solution; epitaxial layers design, device structural and geometry design, and suitable semiconductor manufacturing technique.

In this work physical-based device simulation as an engineering tool was developed. An overview on GaN-based HEMTs physical based device simulation using Silvaco-"ATLAS" is given. The simulation is utilized to analyze, give insight to the modes of operation of the device and for design and evaluation of innovative concepts. Physical-based models that describe the properties of the semiconductor material are introduced. A detailed description of the specific AlGaN/GaN HEMT structure definition and geometries are given along with the complex fine meshing requirements. Nitride-semiconductor specific material properties and their physical models are reviewed focusing on the energetic band structure, epitaxial strain tensor calculation in wurtzite materials and build-in polarization models. Special attention for thermal conductivity, carriers' mobility and Schottky-gate-reverse-bias-tunneling is paid. Empirical parameters matching and adjustment of models parameters to match the experimental device measured results are discussed.

An enhancement of breakdown voltage in $Al_xGa_{1-x}N$/GaN HEMT devices by increasing the electron confinement in the transistor channel using a low Al content $Al_yGa_{1-y}N$ back-barrier layer structure is systematically studied. It is shown that the reduced sub-threshold drain-leakage current through the buffer layer postpones the punch-through and therefore shifts the breakdown of the device to higher voltages. It is also shown that the punch-through voltage (V_{PT}) scales up with the device dimensions (gate to drain separation). An optimized electron confinement results both, in a scaling of breakdown voltage with device geometry and a significantly reduced sub-threshold drain and gate leakage currents. These beneficial properties are pronounced even further if gate recess technology is applied for device fabrication. For the systematic study a large variations of back-barrier epitaxial structures

were grown on sapphire, *n*-type 4H-SiC and semi-insulating 4H-SiC substrates. The devices with 5 µm gate-drain separation grown on *n*-SiC owning $Al_{0.05}Ga_{0.95}N$ and $Al_{0.10}Ga_{0.90}N$ back-barrier exhibit 304 V and 0.43 $m\Omega \times cm^2$ and 342 V and 0.41 $m\Omega \times cm^2$ respectively. To investigate the impact of $Al_yGa_{1-y}N$ back-barrier on the device properties the devices were characterized in DC along with microwave mode and robustness DC-step-stress test. Physical-based device simulations give insight in the respective electronic mechanisms and to the punch-through process that leads to device breakdown.

Systematic study of GaN-based HEMT devices with insulating carbon-doped GaN back-barrier for high voltage operation is also presented. Suppression of the OFF-state sub-threshold drain leakage-currents enables breakdown voltage enhancement over 1000 V with low ON-state resistance. The devices with 5 µm gate-drain separation on SI-SiC and 7 µm gate-drain separation on *n*-SiC exhibit 938 V and 0.39 $m\Omega \times cm^2$ and 942 V and 0.39 $m\Omega \times cm^2$ respectively. Power device figure of merit of ~2.3×10^9 $V^2/\Omega \cdot cm^2$ was calculated for these devices. The impacts of variations of carbon doping concentration, GaN channel thickness and substrates are evaluated. Trade-off considerations in ON-state resistance and of current collapse are addressed.

A novel GaN-based HEMTs with innovative planar Multiple-Grating-Field-Plates (MGFPs) for high voltage operation are described. A synergy effect with additional electron channel confinement by using a heterojunction AlGaN back-barrier is demonstrated. Suppression of the OFF-state sub-threshold gate and drain leakage-currents enables breakdown voltage enhancement over 700 V and low ON-state resistance of 0.68 $m\Omega \times cm^2$. Such devices have a minor trade-off in ON-state resistance, lag factor, maximum oscillation frequency and cut-off frequency. Systematic study of the MGFP design and the effect of Al composition in the back-barrier are described. Physics-based device simulation results give insight into electric field distribution and charge carrier concentration depending on field-plate design.

The GaN superior material breakdown strength properties are not always a guarantee for high voltage devices. In addition to superior epitaxial growth design and optimization for high voltage operation the device geometrical layout design and the device manufacturing process design and parameters optimization are important criteria for breakdown voltage enhancement. Smart layout prevent immature breakdown due to lateral proximity of highly biased interconnects. Optimization of inter device isolation designed for high voltage prevents substantial subthreshold leakage. An example for high voltage test device layout design and an example for critical inter-device insulation manufacturing process optimization are presented.

While major efforts are being made to improve the forward blocking performance, devices with reverse blocking capability are also desired in a number of applications. A novel GaN-based HEMT with reverse blocking capability for Class-S switch-mode amplifiers is introduced. The high voltage protection is achieved by introducing an integrated recessed Schottky contact as a drain electrode. Results from our Schottky-drain HEMT demonstrate an excellent reverse blocking with minor trade-off in the ON-state resistance for the complete device. The excellent quality of the forward diode characteristics indicates high robustness of the recess process. The reverse blocking capability of the diode is better than –110 V. Physical-based device simulations give insight in the respective electronic mechanisms.

Kurzfassung

In dieser Arbeit wurden Galliumnitrid (GaN)-basierte Hochspannungs-HEMTs (High Electron Mobility Transistor) für Hochleistungsschalt- und Regelanwendungen in der Raumfahrt untersucht. Effizientes Leistungsschalten erfordert einen Betrieb bei hohen Sperrspannungen gepaart mit niedrigem Einschaltwiderstand, geringer dynamischer Dispersion und minimalen Leckströmen. Dabei wird das aus dem Halbleitermaterial herrührende Potential für extrem spannungsfeste Transistoren aufgrund mehrerer Faktoren aus dem lateralen und dem vertikalen Bauelementedesign oft nicht erreicht. Physikalisch-basierte Simulationswerkzeuge für die Bauelemente wurden daher entwickelt. Die damit durchgeführte Analyse der unterschiedlichen Transistorbetriebszustände ermöglichte das Entwickeln innovativer Bauelementdesignkonzepte. Das Erhöhen der Bauelementsperrspannung erfordert parallele und ineinandergreifende Lösungsansätze für die Epitaxieschichten, das strukturelle und das geometrische Design und für die Prozessierungstechnologie. Neuartige Bauelementstrukturen mit einer rückseitigen Kanalbarriere (back-barrier) aus AlGaN oder Kohlenstoff-dotierem GaN in Kombination mit neuartigen geometrischen Strukturen wie den Mehrfachgitterfeldplatten (MGFP, Multiple-Grating-Field-Plate) wurden untersucht. Die elektrische Gleichspannungscharakterisierung zeigte dabei eine signifikante Verringerung der Leckströme im gesperrten Zustand. Dies resultierte bei nach wie vor sehr kleinem Einschaltwiderstand in einer Durchbruchspannungserhöhung um das etwa Zehnfache auf über 1000 V. Vorzeitige Spannungsüberschläge aufgrund von Feldstärkenspitzen an Verbindungsmetallisierungen werden durch ein geschickt gestaltetes Bauelementlayout verhindert. Eine Optimierung der Halbleiterisolierung zwischen den aktiven Strukturen führte auch im kV-Bereich zu vernachlässigbaren Leckströme. Während das Hauptaugenmerk der Arbeit auf der Erhöhung der Spannungsfestigkeit im Vorwärtsbetrieb des Transistors lag, ist für einige Anwendung auch ein rückwärtiges Sperren erwünscht. Für Schaltverstärker im S-Klassenbetrieb wurde ein neuartiger GaN-HEMT entwickelt, dessen rückwärtiges Sperrverhalten durch einen tiefgelegten Schottkykontakt als Drainelektrode hervorgerufen wird. Eine derartige Struktur ergab eine rückwärtige Spannungsfestigkeit von über 110 V.

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Chapter 1

Introduction

Unintentional coincidence had led to intercept the GaN-power electronics' destiny with my own. As a lithography process engineer in the Si industry I expended my horizons towards optoelectronic engineering. Thus, my initial intention in the Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH) was to conduct my PhD work in the optoelectronic department. This trivial course was interrupted as I was assigned to the GaN electronics business area to develop high breakdown voltage capabilities of GaN-based HEMTs for switching applications in satellites. The GaN electronics business area group in the FBH was assigned to carry out the Radiation-Hardness GaN-based HEMT for space applications project. The goal of this project is the development of GaN-based radiation hardened with high breakdown voltage switching transistors and regulators as an alternative to Si-based power MOSFETs for Electric Power Conditioner (EPC) in the next generation of Travelling Wave Tube Amplifiers (TWTA) in satellites.

GaN-based semiconductor electronics was foreign to me as the surface of the moon, but I was immediately charmed with its properties and merits. Although I must admit that in the beginning transistors with neither native oxide and polysilicon gates, nor *p*-*n* junctions and implanted ohmic contacts were miraculous to me. But most amazing for me was the existence of two-dimensional-electron-gas (2DEG) channel under the thin AlGaN barrier that is created by polarization differences between the two wide-bandgap materials. Throughout this time I recognized and prevailed enormous challenges in the GaN-based HEMTs through device simulations, device design, processing and characterization.

1.1. Radiation Hardness GaN-Based HEMTs' Project Specifications

GaN-based semiconductor holds particular promise for the space sector. It can reliably operate at much higher voltages and temperatures than widely-used semiconductors such as silicon (Si) or gallium arsenide (GaAs), and is also inherently radiation-hard [1]. When used to realize space-based microwave and power devices, GaN should enable reduction in the size and mass of cooling systems, an enhanced ability to survive the hard radiation environment of deep space with superior output power [2].One of the most attractive concepts is replacement high voltage power Si MOSFETs with GaN-based HEMTs in the satellite communications power systems. Key components for communications satellites are the power amplifiers in the telecommunications payload. Travelling Wave Tube Amplifier (TWTA) is a key element for a satellite transponder. The TWTA consists of the Travelling Wave Tube (TWT) mainly determining the RF performance and the Electronic Power Conditioner (EPC), designed and manufactured for power matching of the DC and bus interfaces.

The developed devices intended to replace existing Si based MOSFET power devices. Therefore they obliged to be compatible with their electrical specifications. Examples for commercial devices with comparable specifications are IRHNA57264SE for switching applications and IRHY7G30CMSE for regulation applications [3]. The radiation hardness GaN-Based HEMTs project explicitly defined the following specifications for the developed devices:

Tolerance to ionizing radiation, TID (gamma)	100-300 krad (Si)
Single Event Effect, (SEE), (heavy ion) with linear energy transfer, (LET):	14-82 MeV/(mg/cm^2), 150-460 MeV
Lifetime:	> 20 years
Devices for switching application:	250 V normally-off very low R_{ON} of 50 mΩ I_D of 150 A
Devices for regulation application:	1000 V normally-on and normally-off R_{ON} of 5000 mΩ I_D of 5 A
Flip chip assembly	

Table 1.1–1 General specifications for radiation hardness AlGaN/GaN HEMTs.

In the radiation hardness GaN-based HEMTs development project's work frame four major phases were defined:

Phase 1: Concepts and feasibility studies for breakdown voltage and for radiation hardness on test structures. Develop reliable of flip-chip technology.

Phase 2: Development of normally-on devices with $V_{BR\ OFF} > 550$ V and normally-off devices $V_{BR\ OFF} > 250$ V for switching application.

Phase 3: Development of normally-on and normally-off devices with $V_{BR\ OFF} > 1000$ V for regulation application.

Phase 4: Radiation hardness and reliability tests.

1.2. Problem Definition, Scope of Work and Success Criteria

Prior to this project, GaN-Based HEMT's in FBH were designed as microwave power amplifiers for high frequency operation with high output power and high power added efficiency. Such design focused on high current, high gain, low RF losses and low RF dispersion. In such design the OFF-state breakdown voltage has less importance. On the other hand the microwave design and process was a fertile ground for high voltage power switching devices due to its basic merits such as high carrier density, very low ohmic contact resistance and ON-state resistance. Therefore the task was to design GaN-based switching devices with enhanced OFF-state blocking capability while preserving as much as possible other device electrical properties.

The power devices' chart depicts, in Figure 1.2–1, the GaN, Si and SiC-based state-of-the-art power devices vs. typical microwave design test devices, $1\ \mu m \geq L_{GD} \geq 10\ \mu m$, from FBH at the starting point of this work. It could be seen that such devices have much lower ON-state resistance than the compared devices but suffers from lack of OFF-state blocking capability. At that time such devices were far from the GaN material limitation using its superior breakdown field.

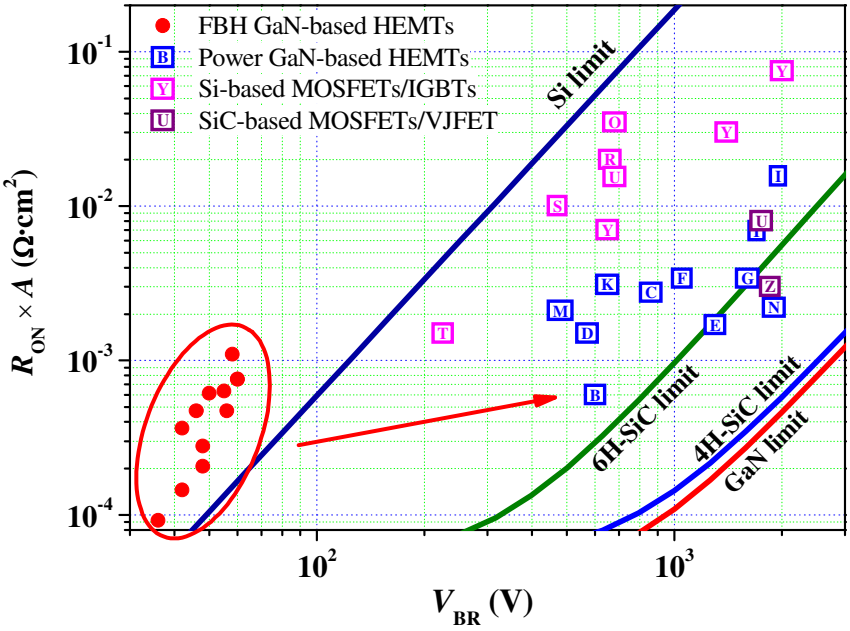


Figure 1.2–1 OFF-state breakdown voltage, $V_{BR\ OFF}$, vs. $R_{ON} \times A$ of the fabricated GaN-based HEMTs from FBH at the project starting point compared with those of the state-of-the-art Si, SiC and GaN-based devices. The theoretical limitations of different device families are taken from literature see section 2.4.2.

Points	Year	Group	Technology	$R_{ON} \times A$ ($\Omega \cdot cm^2$)	$V_{BR\ OFF}$ (V)
B	2005	Saito *et al.* [4]	GaN HEMT	0.0006	600
C	2004	Huili *et al.* [5]	GaN HEMT	0.0028	860
D	2000	Zhang *et al.* [6]	GaN HEMT	0.0015	570
E	2002	Zhang *et al.* [7]	GaN HEMT	0.0017	1300
F	2001	Zhang *et al.* [8]	GaN HEMT	0.0034	1050
G	2006	Tipirneni *et al.* [9]	GaN HEMT	0.0034	1600
I	2006	Yagi *et al.* [10]	GaN HEMT	0.0069	1700
K	2007	Morita *et al.* [11]	GaN HEMT	0.0031	650
M	2007	Saito *et al.* [12]	GaN HEMT	0.0021	480
N	2006	Dora *et al.* [13]	GaN HEMT	0.0022	1900
O	2000	Infineon CoolMOS™ [14]	Si MOSFET	0.035	680
R	2006	Fuji SJ-MOSFET [15]	Si MOSFET	0.02	658
S	2005	Philips RESERF MOSFET [16]	Si MOSFET	0.0098	473
T	2006	Denso/Toyota SJ-MOSFET [17]	Si MOSFET	0.0015	225
Y	Range	Range	Si IGBT	Range	Range
U	2008	Cree MOSFET [18]	SiC MOSFET	0.008	1750
Z	2008	Semisouth VJFET [18]	SiC VJFET	0.003	1850

Table 1.2–1 OFF-state breakdown voltage, $V_{BR\ OFF}$ vs. $R_{ON} \times A$ data.

1.2.1. Scope and Schedule of This Work

The scope of this work is a derivative of the complete radiation hardness GaN-based switching transistors project. In this part of the project, enhancement of the OFF-state blocking voltage to 1000 V while keeping the ON-state resistance as low as possible is desired. The development in this work should have followed the milestones in the project and therefore it was divided to 4 predefined working stages:

Stage 1: Seeking for concepts and feasibility studies for breakdown voltage using physically based simulation and electrical measurements analysis.

Stage 2: Develop normally-on devices with OFF-state blocking capability of $V_{BR\ OFF} > 550$ V and $V_{BR\ OFF} > 250$ V to create the foundations switching application.

Stage 3: Develop normally-on devices with OFF-state blocking capability $V_{BR\ OFF} > 1000$ V to create the foundations to regulation application.

Stage 4: Transfer the developed technology to power device with high voltage and large area.

Schedule	2006		2007				2008				2009			
	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Simulations of the device electrical properties and device characterization matching.					← Ongoing →									
Identification of tools and methods to enhance the device breakdown voltage							← Ongoing →							
Experimental verification of the device design performance and iterations.														
Transfer to power device with high voltage and scale-up.														

Table 1.2–2 This work principal schedule and milestones' Gantt-chart.

Principal schedule Gantt-chart for this work is shown in Table 1.2–2. Follow the development of the simulation tools for device design characterization and analysis it is desired to use it as an ongoing engineering tool in a feedback loop from the experimental results. The development of tools and methods for breakdown voltage enhancement in the

device is also an ongoing task along the experimental verification of the proposed devices, as described along this work.

Tasks in this work should be solved by the following means; Simulation and design of epitaxial layers structures optimized to extract the merits of the GaN material system. Design device geometry (field plates, layout etc.) to reduce critical electric fields and reduce the subthreshold leakages in the device. Process modifications and adjustments that may have influence on the high voltage characteristics of the devices should be considered. Last but not list, are the electrical measurements and analysis of the devices at high voltage.

In addition support to other projects such as the S-class switching amplifier was given. Here it was desired integrate a reverse high voltage bias protection diode into the GaN-based HEMT. Such diode should protect the microwave power HEMT that may experience a short negative pulse at the drain terminal as a result of a fly-back signal from the output filter.

1.2.2. The Flow of This Work

Chapter 2 covers the essential background on GaN-based HEMTs required for this work. GaN-based semiconductor material properties and merits are reviewed. GaN-based HEMT device principal operation is enlightened. Brief description of the device manufacturing process steps is provided. Description of operation as MW power amplifier and as power switching device is given. Theoretical breakdown voltage and ON-state resistance, power device theoretical limitations and premature breakdown mechanisms are discussed in details.

Chapter 3 gives overview on GaN-based HEMTs physical based device simulation as an engineering tool for design, analysis and evaluation of innovative concepts. Introduction to the physical-based models, structure definition and geometrical meshing is given. Nitride semiconductor material properties and their physical models are reviewed. Empirical parameters matching and adjustment of models parameters to match the experimental device measured results are discussed.

Chapter 4 presents systematic study of AlGaN/GaN/AlGaN DH-HEMTs as a possible solution for breakdown voltage enhancement. The physical-theory introduction to the DH-HEMTs is given along with simulation insight. Realization and fabrication of DH-HEMT devices on different substrates with parameters variation is demonstrated by multi-wafer experiments. Enhancement of the breakdown voltage by hundreds of volts with negligible influence on the ON-state resistance is shown. Comprehensive characterization in DC, robustness and reliability, and time and frequency domain is performed. Optimization of the DH-HEMT design parameters is discussed.

Chapter 5 demonstrates AlGaN/GaN/GaN:C back-barrier based HEMTs for state-of-the-art high breakdown voltage power switching devices. GaN carbon doping back-barrier concept is explained. Electrical DC characterization shows considerable reduction in the subthreshold leakage currents that result in breakdown voltage above 1000 V with very low ON-state resistance. Special attention is given to current-collapse phenomena in the manufactured devices.

Chapter 6 presents an innovative concept of Multiple Grating Field-Plates (MGFPs) integrated in DH-HEMTs. Physical insight to the mode of operation is given using physical based simulations. Electrical DC characterization discloses breakdown voltage enhancement of hundreds of volts. Minor tradeoff in current-collapse, time and frequency domain parameters is shown.

Chapter 7 introduces GaN-based HEMTs with reverse blocking capability for Class-S

switch mode amplifiers. The high voltage protection achieved by introducing recessed Schottky contact as a drain electrode. Such configuration provides protection of reverse bias over 110 V. Robust process integration is demonstrated. Devices are characterized in DC, large signal microwave power analysis, current collapse and switching test.

Chapter 8 introduces layout design and manufacturing technique examples for high voltage GaN-based HEMTs. Smart layout prevent immature breakdown due to lateral proximity of highly biased interconnects. Optimization of inter-device isolation designed for high voltage prevents substantial subthreshold leakage.

Chapter 9 concludes the results obtained in this work and summarizes results obtained. An outlook is given for future work towards optimization of GaN-based power switching electronic devices.

Chapter 2

Fundamentals of GaN-based HEMTs Device and Technology

Fundamental background on GaN-based HEMTs material system, devices and technology are introduced in this chapter. First, the basic material properties and parameters of Gallium Nitride (GaN)-based semiconductors and their merits as a power electronics material are reviewed. GaN-based High Electron Mobility Transistors (HEMTs) physical principal of operation is described. Polarization effects in GaN-based semiconductor particularly for $Al_xGa_{1-x}N$/GaN heterostructures are introduced. Brief review of $Al_xGa_{1-x}N$/GaN HEMTs as microwave power amplifier and power switching transistor is given. Theoretical background on device breakdown and ON-state resistance in semiconductor unilateral device is introduced and the theoretical limits are calculated. Finally, a summary of the most common premature breakdown mechanisms in GaN-based HEMTs are reviewed.

2.1. Introduction to GaN-Based Semiconductors and AlGaN/GaN HEMTs

Wide-bandgap semiconductor Gallium Nitride (GaN)-based material systems is standing in the center of attention of this work. Since its emergence in the early 1990s, GaN has attracted attention as highly promising material system for both optical and electronic applications. Over the last twenty years researchers from all over the world have made large efforts to transfer its potential into commercialization. GaN-based material systems are very interesting for electronic applications due to their wide-bandgap, excellent transport properties, high critical field and high thermal stability.

Fast development and performance demonstrations of GaN-based microwave and power devices in the last decade made it at present attractive alternative to Si-based power IGBTs and MOSFET high-end products. GaN-based transistors may bring about a revolution in power amplifier circuits for mobile phone base-stations, and power supply, motor drive and other circuits in fields including industrial equipment, white goods and automobiles. Compared to existing Si devices, they combine lower power losses with output up to ten times more, yielding circuits that are smaller and draw less power than ever. Though, it is far from perfection. Natural normally-on characteristics vs. normally-off requirements play a significant role for power switching.

GaN-based semiconductor devices offer five key characteristics: high dielectric strength, high operating temperature, high current density, high-speed switching and low ON-resistance, see Figure 2.1–1. These characteristics are due to the properties of GaN which include electrical breakdown characteristics ten times higher than that of Si, carrier mobility as good or better than that of Si, and a bandgap three times or more that of Si.

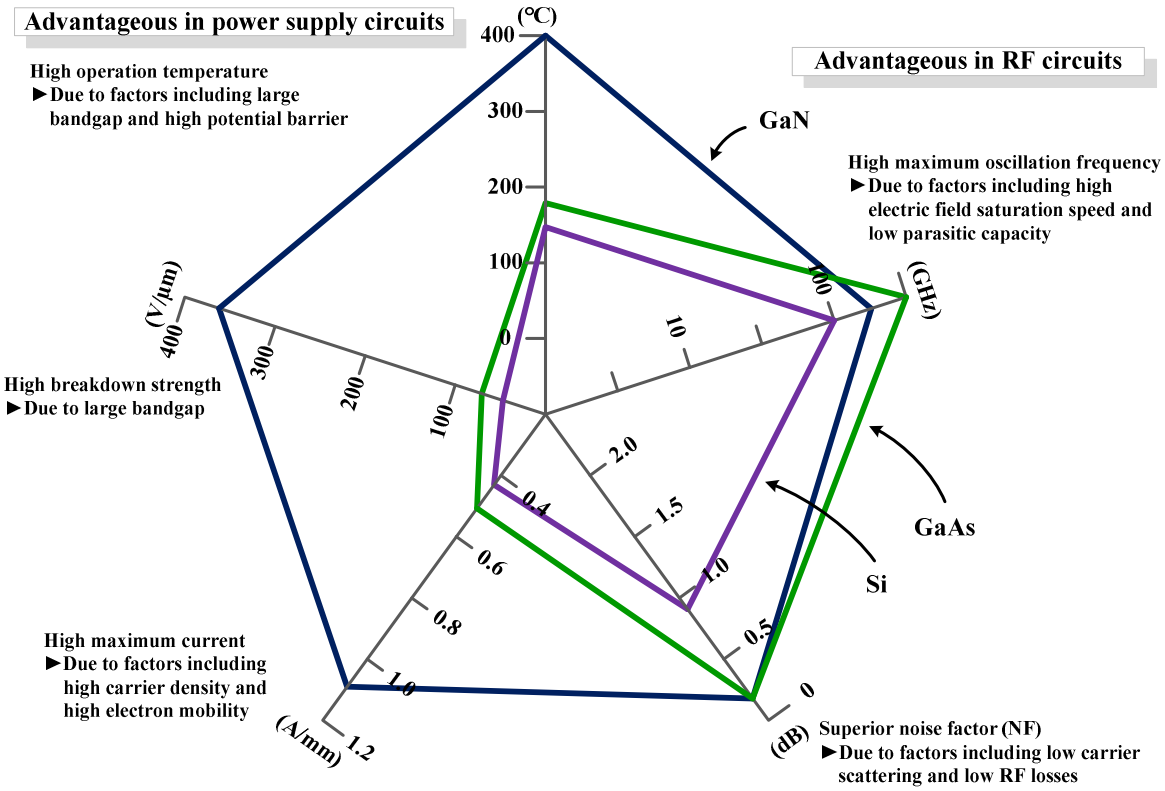


Figure 2.1–1 GaN material merits compared to Si and GaAs [19].

Generally, to achieve high currents and high frequency operation in a semiconductor device, high charge carrier mobility (μ) and high saturation velocity (v_{sat}) are desirable. The high value for electron mobility of GaAs (8500 $cm^2 V^{-1} s^{-1}$) is the main reason that field-effect transistors (FETs) fabricated from this material have such excellent high-frequency performance (see Figure 2.1–1). A primary disadvantage of fabricating transistors from bulk GaN is the relatively low values for the electron mobility, which are ~900 $cm^2 V^{-1} s^{-1}$. However, these values are sufficient for transistors specifically designed for high-power operation. In general, wide-bandgap semiconductors have relatively low mobility but very high values for the saturation velocity, which is reached at high electric fields that can easily be supported (see sections 2.1.3 and 2.1.4 below). The mobility and saturation velocity of the 2DEG at the $Al_xGa_{1-x}N$/GaN heterojunction is very suitable for high-power and high-frequency device applications. The room temperature mobility of the 2DEG, which is typically between 1200 $cm^2 V^{-1} s^{-1}$and 2000 $cm^2 V^{-1} s^{-1}$, is significantly better than that of bulk GaN. The 2DEG sheet charge density (n_s) of the $Al_xGa_{1-x}N$/GaN structure is very high (experimental values up to 1×10^{13} cm^{-2}) due to piezoelectric and spontaneous polarization induced effects.

2.1.1. Material Structure and Polarization Wurtzite GaN-Based Semiconductors

GaN-based and other group III-N based semiconductors exist under different crystal structures, Wurtzite, Zinkblende and Rock-salt [20], [21]. At ambient conditions Al/In/Ga-N alloys present a thermodynamically metastable Wurtzite structure (WZ or 2H). The absolute majority of AlGaN/GaN HEMTs being grown on the Wurtzite phase, only this crystal structure will be farther considered. The Wurtzite structure has a hexagonal unit cell and consists of two intercepting Hexagonal Closed Packed (HCP) sub-lattice. Hence it is defined by two lattice parameters, a_0 and c_0, in ideal ratio $c_0/a_0 = \sqrt{8/3} \approx 1.633$, as shown in Figure 2.1–2. Each sub-lattice is constituted by one type of atoms which are shifted with respect to each other along the c axis by the amount $u_0 = 3/8$ in fractional coordinates. Because of the different metal cations, the bond lengths and the resultant c_0/a_0 ratios of the common nitride compounds AlN, GaN, and InN and their alloys are different. As the lattice non-ideality increases, c_0/a_0 ratio moves away from 1.633 of the ideal lattice [22].

Wurtzite GaN-based semiconductors and other group III-N based semiconductors; have a polar axis resulting from a lack of inversion symmetry in the <0001> direction. Owning to the difference in electronegativity (here given in Pauling's scale) between the Gallium (1.81) and/or Aluminum (1.61) and/or Indium (1.78), atoms and the Nitrogen (3.04) atom, the group III-N's are characterized with high ionicity of the metal-nitrogen covalent bond. Due to this electronic charge redistribution inherent to the crystal structure the group III-N semiconductors exhibit exceptionally strong polarization. This polarization refers to spontaneous polarization, P_{sp}, [22]. Because of their Wurtzite structure, GaN-based and group III-N based semiconductors can have different polarities, resulting from uneven charge distribution between neighboring atoms in the lattice. The polarity of the crystal is related to the direction of the group III-N dipole along the <0001> direction. Figure 2.1–2 shows the two possible polarities, in cation-face, i.e. Ga-face (a), structures the polarization field points away from the surface to the substrate, while in anion-face, i.e. N-face (b), structures the direction of the polarization field is inverted.

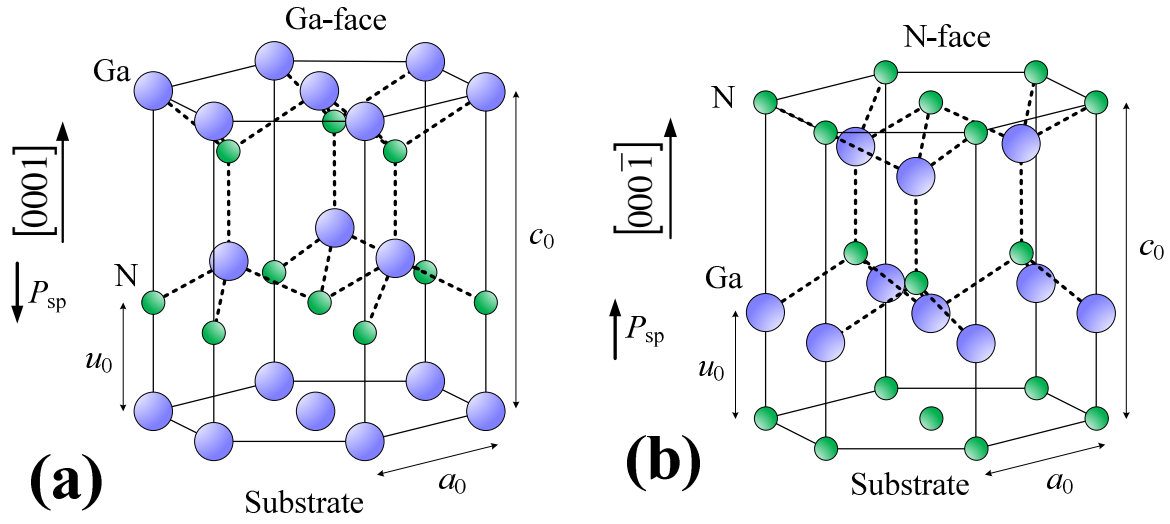


Figure 2.1–2 Illustration of (a) Gallium-face (b) Nitrogen-face ideal Wurtzite GaN lattice structure.

Due to this lack of inversion symmetry, when stress is applied along the <0001> direction to the group III-N semiconductors' lattice, the ideal lattice parameters c_0 and a_0 of the crystal structure will change to accommodate the stress. Therefore, the polarization strength will be changed. This additional polarization in strained group III-N crystals is called piezoelectric polarization, P_{pe} [22]. For example, if the nitride crystal is under biaxial compressive stress, the in-plane lattice constant a_0 will decrease and the vertical lattice constant c_0 will increase. Hence, the c_0/a_0 ratio will increase towards 1.633 of the ideal lattice and the total polarization strength of the crystal will decrease because the piezoelectric and spontaneous polarizations will act in the opposite directions. It is clear that if tensile stress is applied to the crystal, the total polarization will increase because the piezoelectric and spontaneous polarizations in that case act in the same direction. The piezoelectric polarization, P_{pe}, is simply expressed via the piezoelectric coefficients e_{33} and e_{13} as:

$$P_{pe} = e_{33}\varepsilon_3 + e_{13}(\varepsilon_1 + \varepsilon_2) \qquad 2\text{–}1$$

where a_0 and c_0 are the equilibrium values of the lattice parameters, $\varepsilon_3 = (c - c_0)/c_0$ is the strain along the c axis, and the in-plane strain $\varepsilon_1 = \varepsilon_2 = (a - a_0)/a_0$ is assumed to be isotropic. The different strains in the lattice are related as in:

$$\varepsilon_3 = -2 \cdot \frac{C_{13}}{C_{33}} \cdot \varepsilon_1 \qquad 2\text{–}2$$

where C_{13} and C_{33} are elastic constants. Eq. 2–1 and Eq. 2–2 can be combined to obtain the following equation:

$$P_{pe} = 2 \cdot \frac{a - a_0}{a_0} \cdot \left[e_{13} - e_{33} \frac{C_{13}}{C_{33}} \right] \qquad 2\text{–}3$$

Since in the wurtzite III-nitrides the piezoelectric coefficient e_{13} is always negative while e_{33}, C_{13}, and C_{33} are always positive, it turns out that $(e_{13} - e_{33} \cdot C_{13}/C_{33})$ will always be negative [20], [22]. As a consequence, the value of piezoelectric polarization (P_{pe}) in group III-N is always negative for layers under tensile stress ($a > a_0$) and positive for layers under compressive stress ($a < a_0$). As spontaneous polarization in group III-nitrides is always negative, it can be concluded that for layers under tensile stress, spontaneous and piezoelectric polarizations are parallel to each other (as shown in Figure 2.1–3(b)), and for layers under

compressive stress the two polarizations are anti-parallel (as shown in Figure 2.1–3(a)).

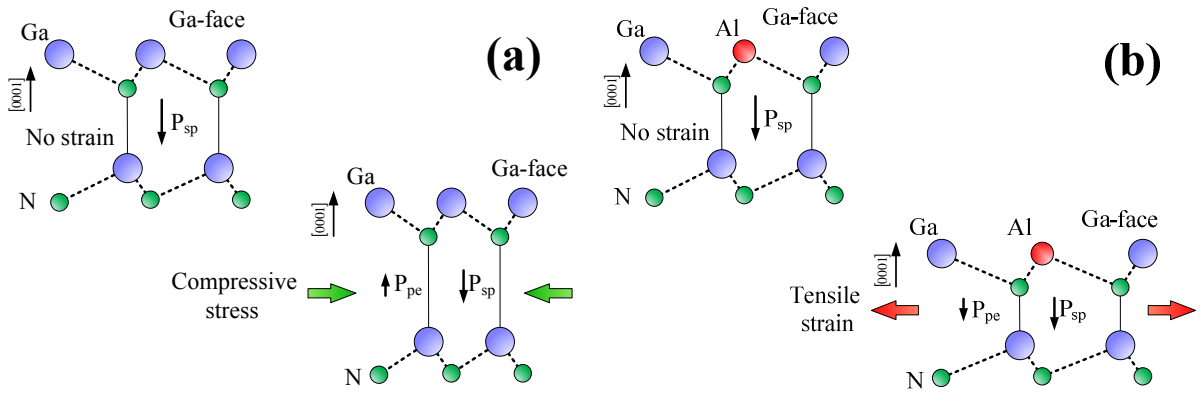


Figure 2.1–3 Illustration of (a) GaN Wurtzite Ga-face compressive stress. (b) AlGaN Wurtzite Ga-face tensile strain.

Polarization itself and gradients in polarization at interfaces and surfaces of AlGaN/GaN heterostructures induce fixed sheet charges, which in turn cause strong electric fields inside every heterostructure. In the nitrides the electric field can reach strength of 3×10^6 V/cm and therefore enhance electron or hole accumulation (depending on the polarity of the material) at AlGaN/GaN interfaces. This accumulation is known as polarization induced doping that is the source of the Two-Dimensional Electrons Gas (2DEG) that will be discussed in the following section.

2.1.2. $Al_xGa_{1-x}N$/GaN Heterostructures and 2DEG Formation

The most unique feature of the HEMT is channel formation from carriers (in our case electrons) accumulated along a heterojunction in a quantum well that are usually referred to as a Two-Dimensional Electrons Gas (2DEG) [23]. These electrons show enhanced mobility due to significantly reduced Coulomb scattering as they are separated from the top supply layer atoms from which they stem. In addition, mobility is further enhanced because of strongly reduced impurity scattering as the quantum well resides in the unintentionally doped, UID, material. Enhanced electron mobility is the key feature that differentiates HEMTs from ordinary FETs.

In early generation AlGaAs/GaAs-based HEMTs the origin of the carrier is a junction between a heavily doped high bandgap and a lightly doped low bandgap region. In GaN-HEMTs based structures, this carrier accumulation is mainly due to polarization charges developed along the heterojunction in the high bandgap AlGaN side. An $Al_xGa_{1-x}N$/GaN heterostructure is shown in Figure 2.1–4.

In Figure 2.1–4(a) the Fermi levels E_F of the two semiconductors do not coincide. At a real heterostructure in thermodynamic equilibrium, this will lead to a bending of the bands, until the structure will have just one common Fermi level (Figure 2.1–4(b)). The heterostructure results in the formation of a discontinuity in the conductance (E_C) and valence (E_V) band at the heterojunction. A triangular quantum well emerges, filled with electrons diffusing from semiconductor II and thus the strongly localized 2DEG develops. The term 2DEG refers to the condition in which electrons have quantized energy levels in one spatial direction but are free to move in the other two directions, parallel to the interface.

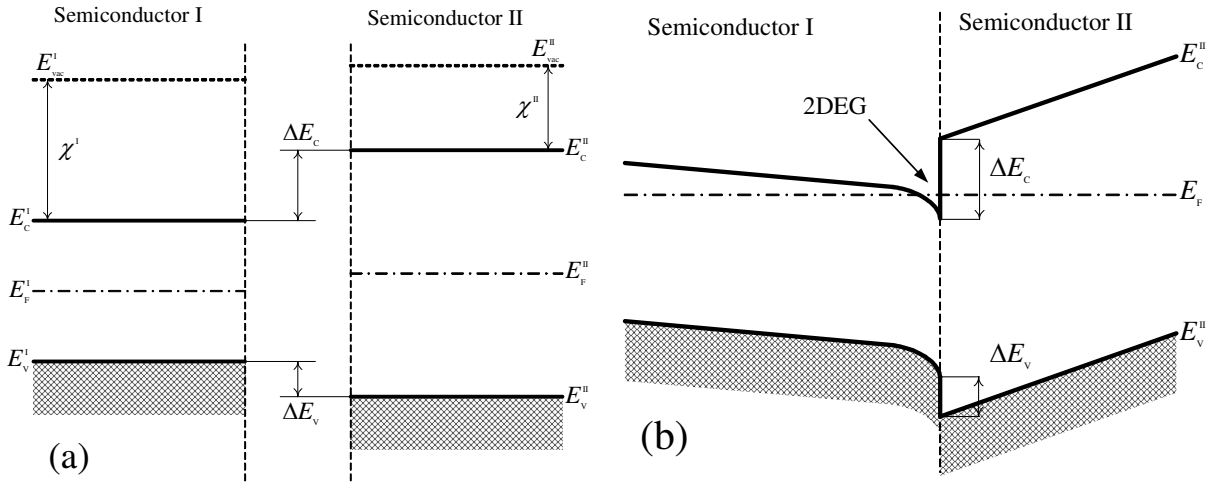


Figure 2.1–4 Band diagram of the heterostructure formed by polarized-piezoelectric narrow gap semiconductor I and polarized-piezoelectric wide gap semiconductor II, $a_I > a_{II}$ divided one from another (a) and together in thermo-dynamical equilibrium where semiconductor II is tensile strained (b).

It was shown that nitride epitaxial layers under stress exhibit both spontaneous and piezoelectric polarization fields. In general, if the polarization field ($\vec{P}$) changes in space, there will be a bound charge density (ρ) associated with it which is given by:

$$\rho = -\vec{\nabla} \cdot \vec{P} \qquad 2\text{–}4$$

For wurtzite III-nitrides polarization is always directed along the *c*-axis, perpendicular to the heterostructure interface. Hence, at the heterojunction, which is assumed to be planar and abrupt a bound sheet charge (σ) will be formed that is given by [24]:

$$\begin{aligned}\sigma &= \vec{P}_{(\text{top layer})} - \vec{P}_{(\text{bottom layer})} = \\ &= \left\{\vec{P}_{\text{sp}(\text{top layer})} + \vec{P}_{\text{pe}(\text{top layer})}\right\} - \left\{\vec{P}_{\text{sp}(\text{bottom layer})} + \vec{P}_{\text{pe}(\text{bottom layer})}\right\}\end{aligned} \qquad 2\text{–}5$$

This bound charge, which is induced by a change in polarization of the two layers, will attract compensating mobile charge at the interface. If the bound charge is positive it will cause a negative mobile sheet charge and vice versa. Baring this in mind we will focus on the calculation of bound charge and the corresponding 2DEG density in a Ga-face undoped AlGaN/GaN heterojunction as shown in Figure 2.1–5.

At the $Al_xGa_{1-x}N$/GaN interface, the difference in polarization between both materials leads to a polarization sheet charge:

$$\sigma = \vec{P}_{(\text{AlGaN})} - \vec{P}_{(\text{GaN})} \qquad 2\text{–}6$$

If this sheet charge density is positive, free electrons compensate this charge and form a two dimensional electron gas, 2DEG, assuming that the band structures of the materials at the interface allow this to happen. To calculate the amount of polarization induced sheet charge density at the interface between $Al_xGa_{1-x}N$ and GaN, material parameters for $Al_xGa_{1-x}N$ alloys can be calculated from the known Al mole fraction values of $0 \geq x \geq 1$ [25], [26]. The polarization induced sheet charge density is expressed as:

$$\sigma = \vec{P}_{\text{sp}(Al_xGa_{1-x}N)} + \vec{P}_{\text{pe}(Al_xGa_{1-x}N)} - \vec{P}_{\text{sp}(\text{GaN})} - \vec{P}_{\text{pe}(\text{GaN})} \qquad 2\text{–}7$$

The piezoelectric polarization for GaN $\vec{P}_{\text{pe}(\text{GaN})}$ is assumed to be zero since bulk GaN buffer layers are assumed none-strained and thus strain-free. Since $Al_xGa_{1-x}N$ grown on Ga-face GaN is always under tensile strain, both piezoelectric and spontaneous polarizations have the same

sign and add up.

The high positive polarization induced sheet charge density, formed at $Al_xGa_{1-x}N$/GaN interface for Ga-face layers, can be compensated by free electrons to form a two-dimensional electron gas (2DEG). It is not clear where the electrons come from: they can be attracted from the bulk GaN buffer layer or from donor-like surface states [27], or from carrier injection from the metal contacts [24]. The maximum sheet carrier concentration can be expressed as [25], [28]:

$$n_s(x)=\frac{\sigma}{q}-\frac{\varepsilon_0 E_F}{q^2}\left(\frac{\varepsilon_r(x)}{d(x)}+\frac{\varepsilon_{r(GaN)}}{d_{(GaN)}}\right)-\frac{\varepsilon_0\varepsilon_r(x)}{q^2 d(x)}\left[q\phi_b(x)+\Delta(x)-\Delta E_C(x)\right] \qquad 2\text{–}8$$

where $d(x)$ the thickness of the $Al_xGa_{1-x}N$ layer, E_F the position of the Fermi level with respect to the GaN conduction band at the GaN-substrate interface, $q\phi_b$ the Schottky barrier height of the gate contact on top of the $Al_xGa_{1-x}N$ layer, $\Delta(x)$ the position of the conduction band below the Fermi-level at the interface, and $\Delta E_C(x)$ the conduction band offset at the interface. This equation cannot be solved analytically. The middle term containing E_F is negligible if GaN buffers thicker than 1 µm are grown, and the expression reduces to that given in [24]. A schematic indication of the $Al_xGa_{1-x}N$ /GaN conduction band diagram is given in Figure 2.1–5.

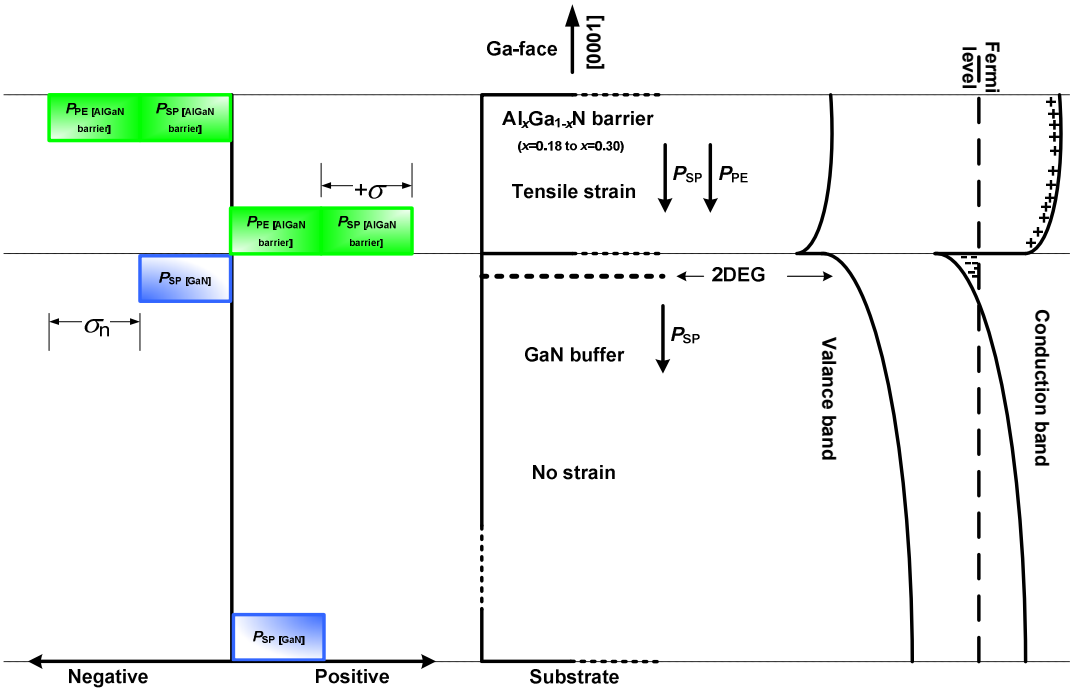


Figure 2.1–5 Polarization scheme and conduction band diagram of Ga-face $Al_xGa_{1-x}N$ /GaN-based HEMTs.

2.1.3. Carrier Mobility in $Al_xGa_{1-x}N$/GaN heterostructures' 2DEG

In power devices the resistance of the drift region can be drastically reduced by replacing narrow band gap semiconductor like silicon with wide band gap semiconductors like GaN-based semiconductors. The resistivity (ρ) of any semiconductor region is given by:

$$\rho=\frac{1}{q\mu N_n} \qquad 2\text{–}9$$

where μ by the mobility, which is a function of the carrier (electrons) concentration (N_n).

In any semiconductors, carriers are accelerated by the presence of an electric field and achieve an average velocity determined by the carrier scattering processes. As the free carriers are transported along the direction of the electric field, their velocity increases until they experience scattering. In the bulk semiconductor, the scattering can occur either by interaction with the lattice or at ionized donor and acceptor atoms. Consequently, the mobility is dependent upon the lattice temperature and the ionized impurity concentration. The low field mobility (μ) is defined as the proportionality constant relating the average carrier velocity (v_D) to the electric field (E):

$$v_D = \mu E \qquad 2\text{–}10$$

This expression is valid at low electric fields. However, in power devices the high electric field presents then the velocity is no longer found to increase in proportion to the electric field. In fact, the velocity approaches a constant value known as the saturated drift velocity. (See section 2.1.4 below)

As the carriers travel through a semiconductor, they undergo a variety of interactions with the host material. The electron mobility is the most popular and most important transport parameter used to characterize the microscopic quality of the semiconductor layers. Mobility is considered to be the figure of merit for materials used for electronic devices.

In addition to the high carrier concentration in the 2DEG created by the polarization induced doping at the AlGaN/GaN interface; carriers in the 2DEG have unique high mobility properties. GaN-based semiconductors' large bandgap, large dielectric breakdown field, good electron transport properties (an electron mobility possibly in excess of 2000 $cm^2\ V^{-1}\ s^{-1}$ and a predicted peak velocity approaching 3×10^7 cm s^{-1} at room temperature), and good thermal conductivity are merits for high-power/temperature electronic devices.

In AlGaN/GaN-based HEMTs, the carriers that form the 2DEG channel in the smaller bandgap material, UID GaN, are donated by the larger bandgap material, AlGaN. Because the mobile carriers and their parent donors are spatially separated, short-range ion scattering is nearly eliminated, which leads to mobilities that are characteristic of nearly pure semiconductors.

Electron mobility is a key parameter in the operation of GaN-based HEMT as it affects the access resistances as well as the rate with which the carrier velocity increases with electric field. Consequently, the low-field mobility in GaN is depending on various scattering events. The electron mobility is limited by the interaction of electrons with phonons and, in particular, with optical phonons. This holds for bulk mobility as well as that in AlGaN/GaN HEMTs' 2DEG.

Khan *et al*. showed in their early work, illustrated in Figure 2.1–6, mobility for the single GaN layer increases from 450 $cm^2\ V^{-1}\ s^{-1}$ at room temperature to 1200 $cm^2\ V^{-1}\ s^{-1}$ at 150 K. It then decreases for lower temperatures due to ionized impurity scattering. On the other hand, the electron mobilities of the heterojunction increases from 1500 $cm^2\ V^{-1}\ s^{-1}$ at room temperature to a value of 5000 $cm^2\ V^{-1}\ s^{-1}$ at 150 K and remains essentially constant for temperatures down to 80 K. This enhanced electron mobility is associated to the presence of 2DEG at the hetero-interfaces. The 2DEG mobility enhancement is caused by a much higher volume electron concentration (compared to the bulk *n*-GaN), which results in a larger Fermi energy and a more effective screening [29], [30].

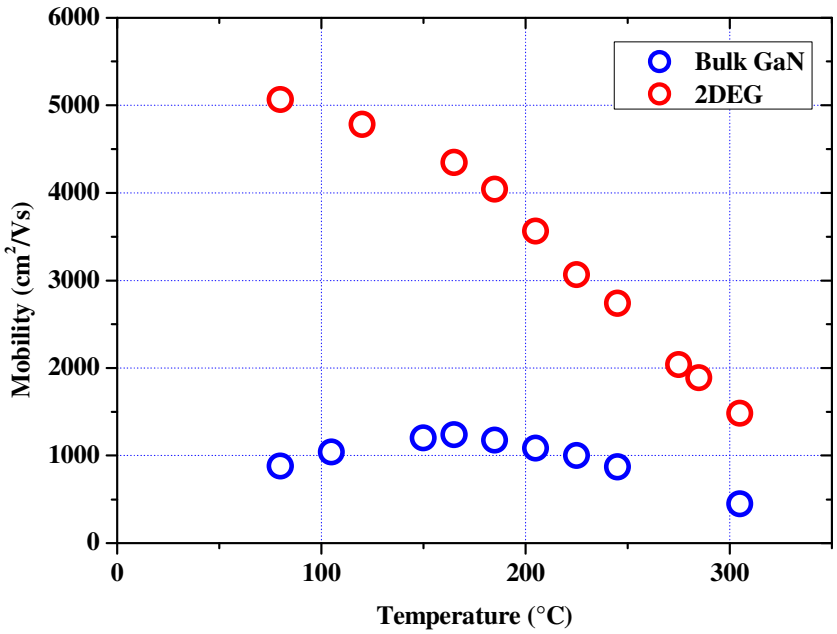


Figure 2.1–6 Experimental electron Hall mobility in GaN vs. temperature for $Al_{0.1}Ga_{0.9}N$/GaN two dimensional electron gas (2DEG) and bulk *n*-GaN $n = 1 \times 10^{17}$ cm^{-3}. (Results are taken from [29])

The 'traditional' scattering mechanisms in 2DEG and their effects on the carrier mobility have been studied for AlGaAs/GaAs and Si-MOSFET systems. They are important in AlGaN/GaN 2DEG transport as well. Electrons moving in the 2DEG experience interface-roughness scattering due to the non-abrupt interface between AlGaN and GaN. The 2DEG wave-function is mostly confined in GaN, but there is a finite part that penetrates the AlGaN barrier, leading to alloy-disorder scattering. Interface-roughness scattering and alloy scattering are short-range scattering sources [31]. Charged impurities are always present in the semiconductors samples, and constitute a form of long-range Coulombic scattering source. The lattice vibrates at finite temperatures and phonons form a potent scattering mechanism at high temperatures. An important form of Coulombic scattering in AlGaN/GaN 2DEGs is dislocation scattering, owing to the large density of dislocations in the material. The cores of threading edge dislocations have dangling bonds that introduce states in the gap of the semiconductor, causing a dislocation to become a line of charge. Such charged dislocations scatter conduction electrons. Dislocations also scatter from strain-fields that develop around them.

Due to the very high electric fields that result from the large polarization (~ 1 MV/cm), electrons in the 2DEG are electro-statically pushed close to the AlGaN/GaN interface, and the centroid of the wave function is brought closer to the hetero-interface. This directly leads to an increased sensitivity to alloy disorder and interface roughness scattering, which turn out to be the dominant scattering processes at low temperatures, and even at room temperature for very high density 2DEGs. In addition the microscopic disorder in an alloy layer, the dipole moment in each unit cell is no more periodic with the crystal lattice; therefore it leads to 'dipole-scattering'. This interesting novel scattering mechanism has no analogue in traditional non-polar and weakly-polar semiconductors.

For the design of GaN-based HEMTs structures specially for high power devices with high conductivity the following should be taken into consideration [32]; Mobility of low-density AlGaN/GaN 2DEGs ($n_{2DEG} \leq 10^{12}$ cm^{-2}) is limited by scattering from charged defects such as dislocations, dipoles, residual impurities. Mobility of high-density AlGaN/GaN 2DEGs is insensitive to scattering by various charged impurities. Alloy disorder scattering limits the mobility for AlGaN/GaN 2DEGs at low temperatures. At extremely high carrier densities,

alloy scattering is as severe as scattering from phonons, even at room temperature.

2.1.4. Carrier Velocity in GaN-Based Material Systems

The steady-state electron drift velocity versus electric field has been calculated for the nitride binaries and ternaries at different temperatures and for various doping concentrations [33]. As expected, Monte Carlo simulations [34], [35] confirm that electron velocity of GaN depends on doping concentration, electric field, and temperature. The variation of electron velocity with electric field always shows a peak.

Figure 2.1–7 shows the calculated electron steady-state drift velocity versus applied electric field, for GaN, $Al_{0.2}Ga_{0.8}N$, $Al_{0.5}Ga_{0.5}N$, $Al_{0.8}Ga_{0.2}N$, and AlN materials [33]. Much higher drift velocity is calculated for $Al_{0.2}Ga_{0.8}N$/GaN heterojunction's 2DEG with peak velocity of 1.5×10^8 cm·s^{-1} at 70 kV·s^{-1} [36].

The velocity-field characteristics can be described by (i) Ohmic in low field region; (ii) Nonlinear transport characterized by a hump in the velocity-field curve at fields of ~ 10 to 50 kV/cm; (iii) peak velocity region occurring at ~ 2×10^5 V/cm; (iv) negative resistance region followed by and (v) saturation and until breakdown.

The obtained velocity-field characteristics for GaN-based semiconductors suggest a rather high electron peak and saturation velocity together with high field. The combination of high-field and high electron velocity in GaN-based semiconductors confirms the potential to increase of output power densities, since high current densities and high voltages would be achieved at the same time. More theory on GaN-based semiconductors transport is discussed in section 3.3.2.5 below.

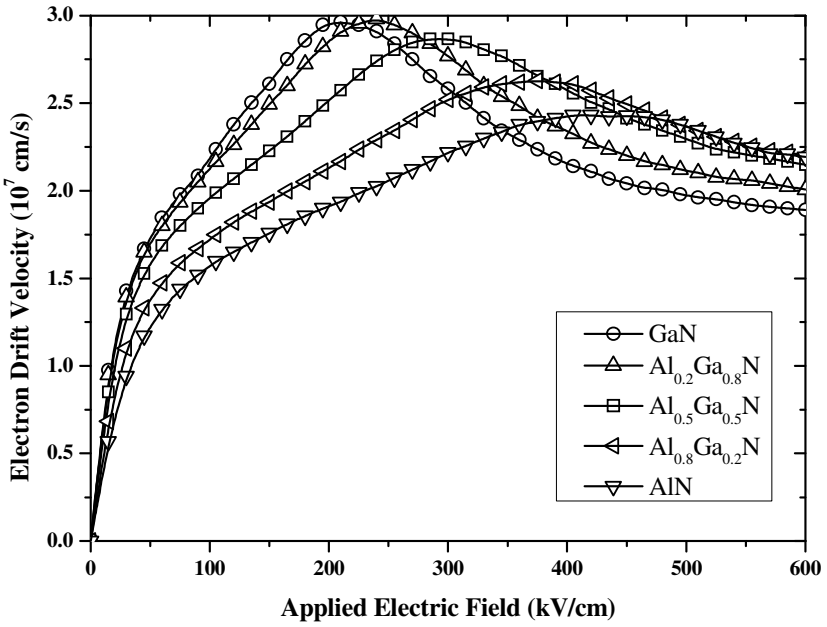


Figure 2.1–7 Monte Carlo simulations of electron drift velocity versus applied electric field for GaN, $Al_{0.2}Ga_{0.8}N$, $Al_{0.5}Ga_{0.5}N$, $Al_{0.8}Ga_{0.2}N$, and AlN. Lattice temperature is at 300 K, and electron concentration is equal to 10^{17} cm^{-3} (Results are taken from [33]).

Velocity–field curves have also been calculated for a temperature range of 77–1000 K [37]. The variation of electron velocity with electric field as a function of the temperature is shown in Figure 2.1–8. Calculated temperature dependence of electron mobility in GaN quantum wells was found to be higher than in the bulk GaN material, which is counterintuitive as carrier scattering into the barrier where the mass is higher and velocity is lower would lower the velocity instead. Unfortunately, many GaN parameters necessary for Monte Carlo

calculations are not yet precisely known. In view of this uncertainty, it may be unwise to draw any definitive conclusion regarding the calculated effect of compensation on the electron mobility.

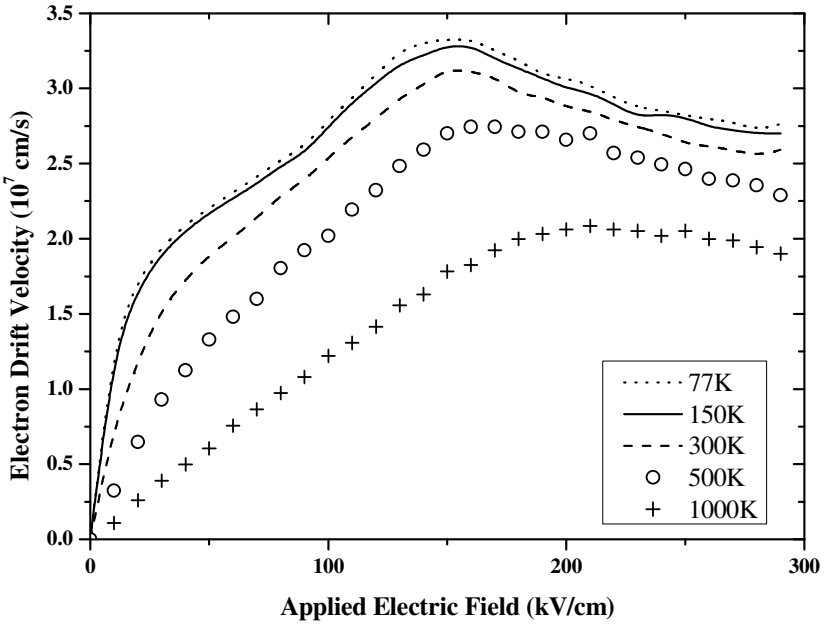


Figure 2.1–8 Monte Carlo simulations of temperature dependence of velocity field characteristics of GaN, $n = 10^{17}$ cm^{-3}. T = 77 K, 150 K, 300 K, 500 K and 1000 K (Results are taken from [37]].

2.2. AlGaN/GaN-Based HEMTs

The main feature of GaN-based power and high-frequency devices is the two-dimensional electron gas, 2DEG, at the AlGaN/GaN heterojunction. The first report on the fabrication and operation of AlGaN/GaN heterojunction FETs, also called HEMTs, was by Khan *et al*. in 1993 [38].

Figure 2.2–1 shows the cross-sectional diagram of an AlGaN/GaN HEMT and the energy band diagram under the gate electrode, respectively. A high carrier density is generated at the AlGaN/GaN hetero-interface due to spontaneous and piezoelectric polarization effects (section 2.1.2 above). The combination of the large carrier density and high breakdown voltage enables high power output operation.

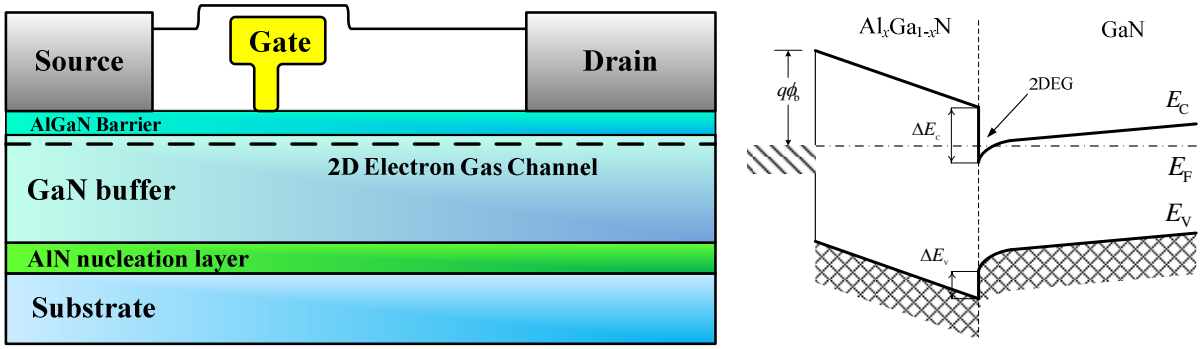


Figure 2.2–1 A planar gate AlGaN/GaN based HEMT structure and the energy band-diagram under the gate electrode.

A GaN-based HEMT transistor is a three terminal device in which the current flowing between the ohmic source and the drain contacts is modulated by the Schottky metal gate

contact. The majority carriers, electrons, are traveling through the highly conductive 2DEG channel formed at the AlGaN/GaN interface and their number is modulated by the electric field resulting from the gate bias. Such transistor is usually working in a depletion mode, i.e. at $V_{GS} = 0$ V gate conditions the device is normally in its "ON" state allowing current to flow through it. Such characteristics are big concern for switching applications for safe operation reasons. High current levels in the device may occur unintentionally when gate control is lost. Therefore, reliable normally-OFF devices are needed.

2.2.1. AlGaN/GaN HEMTs as Microwave Transistors

GaN-based HEMTs were first considered for microwave applications due to their superior properties. A good power device is that which allows to switch as large current as possible, on and off across as large a load resistance as possible, to obtain the maximum output power across this load resistance. Therefore maximize of the current available from the device and the voltage swing it can sustain is desired. In GaN-based HEMTs due to the large values of the access resistances, the maximum drain current is not velocity limited but field limited hence the $n_s \cdot \mu$ product is more important than the $n_s \cdot v_{sat}$ product. The 2DEG channel provides the high carrier density and high carrier mobility as a consequence of the strong polarization field present in the GaN system.

Schematic DC *I-V* characteristics of GaN-based HEMT are illustrated in Figure 2.2–2. In such devices both high current densities and high drain voltage are available and explain the large power capacity. The maximum output current $I_{DS\,max}$, the knee voltage V_{knee} and the breakdown voltage $V_{BR\,OFF}$ can be measured to estimate the maximum output power in class-A operation.

$$P_{max} = \frac{I_{DS\,max}\left(V_{BR\,OFF} - V_{knee}\right)}{8} \qquad 2\text{–}11$$

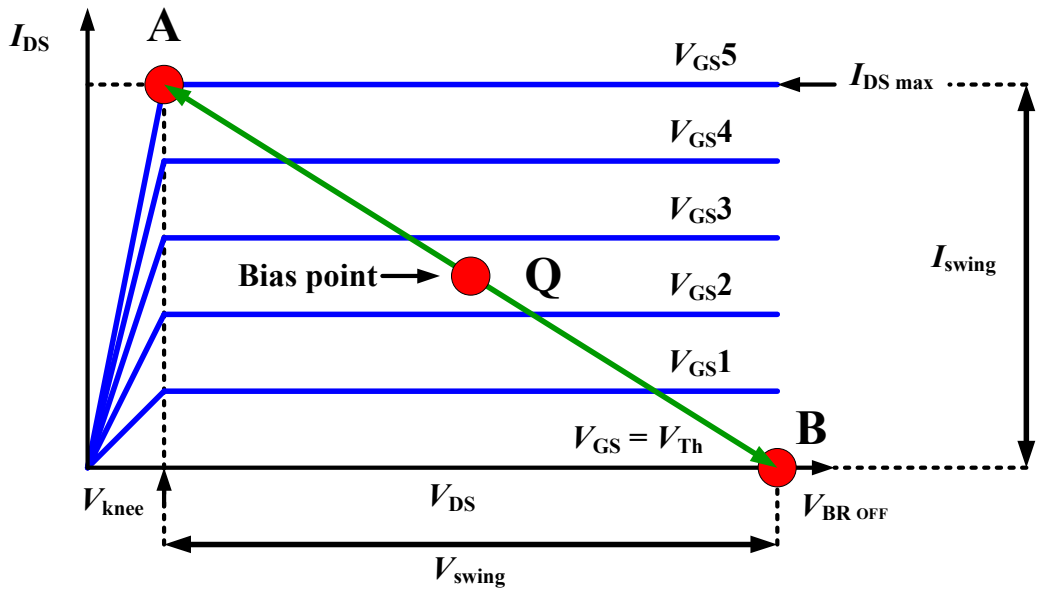


Figure 2.2–2 Illustration of operation points on *I-V* curves of microwave class-A power amplifier.

Threshold voltage, V_{Th}, is the gate-source voltage necessary to stop the current in the device by totally depleting the 2DEG channel from mobile carriers.

$$V_{Th} = V_{GS}\big|_{I_{DS}\to 0,\, V_{DS} >> V_{GS}} \qquad 2\text{–}12$$

The ability of the gate to modulate the current flow between the source and the drain is expressed by the transconductance, g_m, defined as:

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=\text{Const.}} \qquad 2\text{–}13$$

Additional figure of merits are commonly used to characterize the microwave power HEMTs in terms of high frequency performance [39]; the current-gain cut-off frequency, f_T, and the maximum oscillation frequency f_{max}. These parameters could be extracted from small signal measurements (*S*-parameters). The cut-off frequency, f_T, value is extracted from the $|h_{21}|^2$ parameter-curve where it equals gain of 0 dB. The maximum oscillation frequency, f_{max}, value is extracted from the maximum unilateral transducer-power gain, MUG, and maximum stable gain, MSG, parameters curves where it reaches gain of 0 dB.

Nevertheless f_T, and f_{max} just describe the small signal behavior of the device. In order to evaluate the RF power performance, the associated gain, G, the power added efficiency, %PAE, and the output power, P_{out}, are used.

$$\%\text{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} \cdot 100\% = \frac{P_{out}}{P_{DC}}\left(1 - \frac{1}{G}\right) \cdot 100\% \qquad 2\text{–}14$$

By definition %PAE is limited to 100%; however depending on the mode of operation the theoretical limits are set, for example to 50% in class-A and 78% in class-B. A measured %PAE close to the theoretical limit is an indication of a good quality of the device, low DC and RF dispersion and low dissipation.

Thermal management is important in a microwave device in order to reach a maximal output power. Self-heating effect that elevates the channel temperature reduces the low-field carrier mobility and their saturation velocity. The available drain current decreases at high drain voltage, thus the output power density is reduced.

2.2.2. AlGaN/GaN HEMTs as Power Switching Transistors

Silicon has long been the dominant semiconductor for high voltage power switching devices, most commonly making use of structures like the double-diffused metal-oxide-semiconductor (DMOS), UMOS etc, [40]. However, silicon power devices are rapidly approaching theoretical limits for performance (see section 2.4.2 below). There have been successful efforts to push beyond limits of Si by novel device structures like the Super Junction MOSFET [15], [17], CoolMOS™ [14] and RESERF MOSFET [16].

At the same time, wide bandgap materials, particularly GaN and SiC, have attracted much attention because they offer a number of potential advantages over silicon. These potential advantages arise from the fundamental physical properties of the material.

GaN-based High Electron Mobility Transistors (HEMTs) are considered to be excellent candidates for high-power switching applications such as highly efficient power switches in switched power-supplies or AC motor-drive systems, due to their high electron mobility ($\mu \sim 1500\ \text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$), high saturation velocity and high sheet-carrier density ($n_s \sim 1 \times 10^{13}\ \text{cm}^{-2}$) in the two dimensional electron gas (2DEG) channel. These in turn yield a high $n_s \cdot \mu$ product which contributes to a low ON-state resistance, R_{ON}. The high critical electric

field-strength (~ 3.5 MV/cm) allows high natural OFF-state blocking capability in smaller device regions thereby also reducing the R_{ON} [41], [42], [43]. The polarization induced doping results in low electron scattering. In addition to their good thermal conductivity the wide bandgap is suitable for high temperature operation up to 400 °C. In GaN-based HEMTs' structures the operating temperature is only limited by the extrinsic materials like the SiN_x passivation layer, Schottky metal stability etc.

Nevertheless, like any other semiconductor switch, the power GaN-based HEMT is not ideal. It blocks voltage in one direction only, in case of Schottky metal gate. It passes a low but finite value of leakage current when OFF and has a nonzero value of resistance when ON. The OFF-state blocking voltage and ON-state currents have limits, set respectively by the drain-source breakdown voltage and by the onset of the active region operation. The time taken to switch from one state to another is not zero.

2.2.2.1. Ideal Power Device Characteristics [44]

The I-*V* characteristics of a typical power switch and simplified resistive drain switching circuit are illustrated in Figure 2.2–3. Ideal transistor conducts current in the ON-state with zero voltage drop and blocks voltage in the OFF-state with zero leakage current. In addition, the ideal device can operate with a high current and voltage in the active region, with the saturated forward current in this mode controlled by the applied gate bias. The spacing between the characteristics in the active region is uniform for an ideal transistor indicating a gain that is independent of the forward current and voltage.

In reality the device exhibits a finite resistance when carrying current in the ON-state as well as a finite leakage current while operating in the OFF-state (not shown in the figure because its value is much lower than the ON-state current levels). The breakdown voltage of a typical transistor is also finite as indicated in the figure. The typical transistor can operate with a high current and voltage in the active region. This current is controlled by the gate voltage. The spacing between the characteristics in the active region is non-uniform for a typical transistor with a square-law behavior for devices operating with channel pinch-off in the current saturation mode.

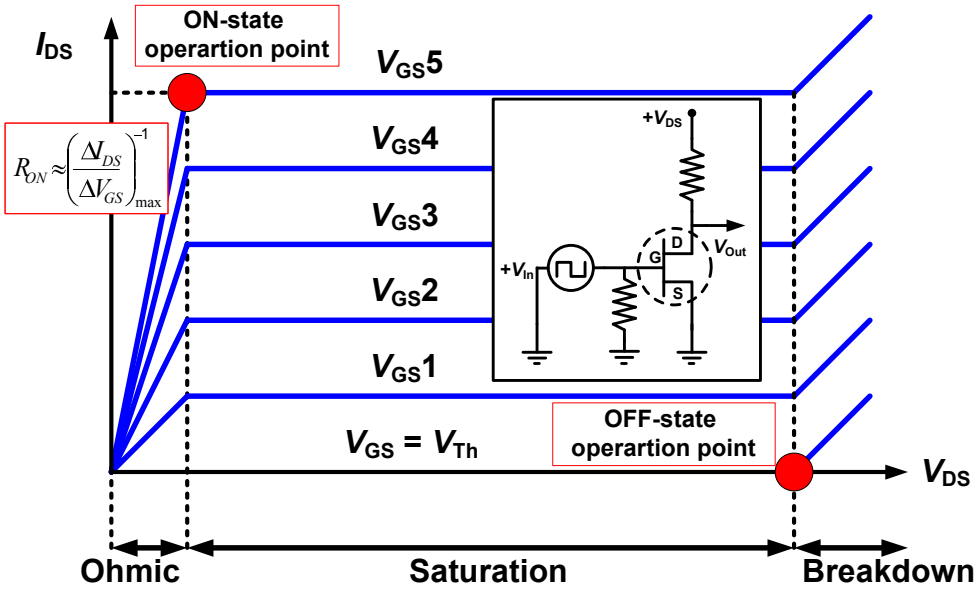


Figure 2.2–3 Illustration of operation points on *I-V* curves of switching transistor. Inset: example of simplified resistive drain switching circuit.

2.2.2.2. Power dissipation in power switching devices [45]

Switching transients always cause an increase in dissipation. During turn-on the energy

stored in parasitic capacitance has to be absorbed. During turn-off the energy in inductance is dissipated. Under steady-state conditions the power dissipation is $I_D^2 R_{DS(ON)}$. Additional energy dissipated during switching:

$$P = I_D^2 R_{DS(ON)} + \left(E_{ON} + E_{OFF}\right) f_s \qquad 2\text{–}15$$

where the additional energy during turn-on is E_{ON} and during turn-off is E_{OFF} and the switching frequency is f_s.

For resistive drain circuit, as shown in Figure 2.2–3 inset, with linear changes in the drain current,I_0, and drain-source voltage,V_0, with rise and fall times of τ_r and τ_f, respectively, the total switching energy is:

$$E_{ON} + E_{OFF} = \frac{1}{6} V_0 I_0 \left(\tau_r + \tau_f\right) \qquad 2\text{–}16$$

The total power dissipation, P_T, is the sum of the switching losses, P_S, conduction losses, internal gate losses, P_G, and leakage current losses, P_L. The power loss resulting from turn-ON and turn-OFF for resistive load is given by:

$$P_S = \frac{V_{DS(max)} I_{D(max)}}{6} t_s f_s \qquad 2\text{–}17$$

where t_s is the average switching time and f_s is the switching frequency.

A proportion of the gate drive power will be dissipated in the internal resistance of the gate. The internal gate losses are given by:

$$P_{G(int)} = V_{GS} Q_G f_s \frac{R_{G(int)}}{R_S + R_{G(int)}} \qquad 2\text{–}18$$

where Q_G is the gate charge transfer during switching, $R_{G(int)}$ is the internal gate resistance, and R_S is the external gate resistance.

The losses due to drain-source leakage current can usually be discounted even in high-voltage power devices. However the leakage current may not be insignificant when the OFF-state gate drive voltage approaches the threshold voltage. Losses due to leakage current are given by:

$$P_L = I_{DSS} V_{DS} \left(1 - \delta\right) \qquad 2\text{–}19$$

where δ is the ON-time duty cycle.

The conduction power loss is given by:

$$P_C = I_{D(rms)}^2 R_{DS(ON)} \qquad 2\text{–}20$$

The rms value of rectangular waveform is given by:

$$I_{rms} = I_D \sqrt{D} \qquad 2\text{–}21$$

where D is the ON-time duty cycle fraction.

$R_{DS(ON)}$ increases significantly with the temperature, thereby increasing the dissipation and the channel temperature. Therefore for efficient power switching it is important that wide band gap GaN-based HEMTs will own low ON-state resistance and will be able to operate in high temperatures with low thermal resistance.

The design of efficient GaN-based HEMTs switching devices should then take into considerations two main parameters The ON-state resistance and gate-channel capacitance. The gate-channel capacitance is the main contributor to the rise and fall times τ_r and τ_f, respectively. These time constants are depend on the gate geometry, gate width, L_G, AlGaN

barrier thickness, d_{AlGaN} and the $Al_xGa_{1-x}N$ barrier molar fraction, x. Since the AlGaN barrier thickness and the $Al_xGa_{1-x}N$ barrier molar fraction are relatively constants and are the control parameters to the carrier density in the 2DEG the main contributor to the gate capacitance is the gate length. Low ON-state resistance could be achieved by short drift region, i.e. short gate-drain separation, L_{GD}, short gate length L_G, for short depletion region and high 2DEG carrier sheet density, n_s.

2.3. AlGaN/GaN HEMTs Process Technology and Integration

GaN-based lateral heterostructure field effect transistors, (HFETs), or high electron mobility transistor, (HEMTs), planar manufacturing process in FBH is a successor of GaAs MESFET and InP HBT manufacturing processes. A detailed discussion on the fabrication process is the intellectual property of the FBH and therefore brought as an overview in this work. The basic manufacturing process of the device frontend steps are illustrated in Figure 2.3–1.

The process starts by growth of nitride based epitaxial layers by Metal Organic Vapor Phase Epitaxy (MOVPE) on single crystal substrate in FBH material technology laboratory. Typical substrates used for the epitaxial growth are sapphire, Semi-Isolating 4H-SiC and *n*-type 4H-SiC. The wafers diameters used as substrates are 3-inch and in some cases are 2-inch. During the epitaxial growth a two dimensional electron gas, (2DEG) is formed and will serve as the device high mobility conductive channel.

Field-effect transistors are fabricated in FBH process technology class 100 clean-room laboratories. For the development of high voltage test devices a frontend short process loop is used excluding the backend second passivation, interconnectors and air bridges.

The ohmic contacts are defined by image reversal optical lithography [46]. A Ti/Al/Mo/Au metal stack is then deposited by e-beam evaporation followed by a photo resist liftoff. The ohmic metal contacts are formed on the AlGaN barrier layer by rapid thermal annealing, (RTA), at 830°C. Inter-device insulation is made using photolithographic mask defined $^{14}N^{+}$ three-energy levels implantation (see Chapter 8 for details). The AlGaN barrier is passivated with 150 nm Plasma-Enhanced Chemical Vapor Deposition, (PECVD) SiN_x. A gate trench in the passivation is defined by i-line optical lithography and subsequently opened by Inductively Coupled Plasma, (ICP), Reactive Ion, (RIE), dry etching. Using the same photolithographic mask and etch process metal interconnection windows opening in the SiN_x passivation are patterned. Ir/Ti/Au contacts are then evaporated for the gate Schottky metal and the interconnections, followed by a metal liftoff. To improve the interconnections robustness a second Ti/Au metal stack is formed on top of the contacts.

The fabricated test devices are 2 × 125 µm and 2 × 50 µm wide (W_G) with a gate length of 0.7 µm and asymmetrical Γ-gate head of 1.5 µm with 0.2 µm extension towards the source and 0.6 µm extension towards the drain. The source-gate spacing L_{GS} was kept at 1 µm. Wide range of 2 × 125 µm devices with gate-drain spacing L_{GD} varied from 1 µm to 18 µm are tested to evaluate the device ability to scale up the OFF-state breakdown voltage with its gate to drain separation. Chapter 8 gives additional details regarding the devices layout and design.

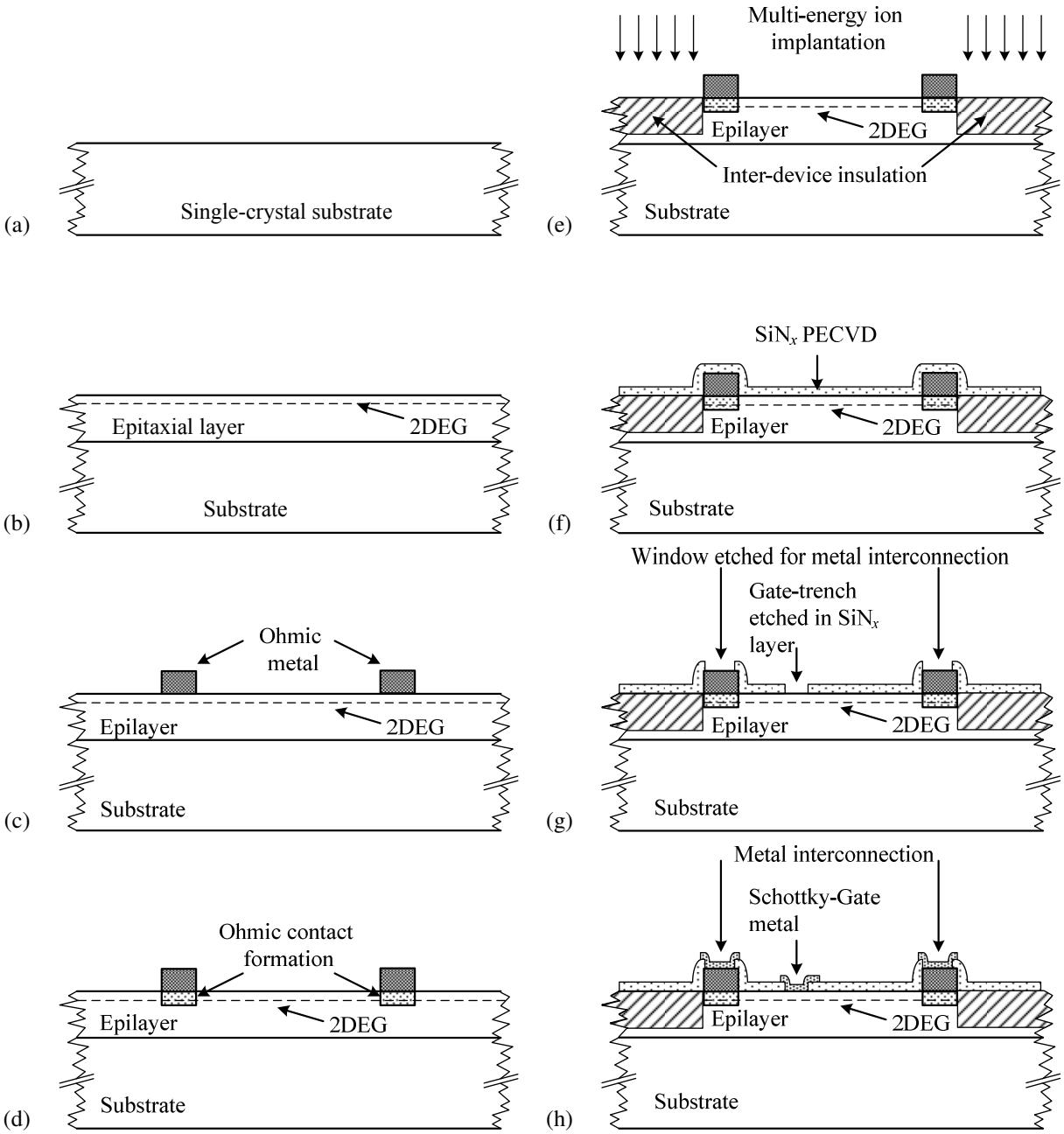


Figure 2.3–1 Illustration of planar GaN-based HEMTs technology process (a) single crystal substrate (b) growth of GaN-based HEMT epitaxial layers (c) lithography defined ohmic contacts metal deposition and liftoff (d) ohmic contacts formation by rapid thermal annealing (e) inter-device insulation using multi-energy ion implantation (f) PECVD SiN_x passivation formation (g) photolithographic gate trench and metal interconnection etching in the SiN_x passivation (h) lithography defined gate Schottky-metal and interconnections deposition and liftoff.

2.4. Theoretical Breakdown Voltage and ON-State Resistance in Power Devices [44]

On of the most unique feature of power semiconductor devices is their ability to withstand high voltages. The desire to control larger power levels has encouraged the development of power devices with larger breakdown voltages.

In a semiconductor, the ability to sustain high voltages without the onset of significant current flow is limited by the avalanche breakdown phenomenon, which is dependent on the electric field distribution within the structure. High electric fields can be created within the interior of power devices as well as at their edges. The design optimization of power devices must be performed to meet the breakdown voltage requirements for the application while minimizing the ON-state voltage drop, so that the power dissipation is reduced.

In this section the theory behind the avalanche and the punch-through breakdown limitations and the ideal specific ON-state resistance are discussed.

2.4.1. Theoretical Breakdown Voltage

Power devices are designed to sustain high voltages within a depletion region formed across either a *p*–*n* junction, a metal-semiconductor (Schottky-barrier) contact, or a metal-oxide-semiconductor (MOS) interface. Any charge carrier that enter the depletion layer either due to the space-charge generation phenomenon or by diffusion from neighboring regions - are swept out by the electric field produced in the region by the applied voltage. As the applied voltage is increased, the electric field in the depletion region increases, resulting in acceleration of the mobile carriers to higher velocities. With further increase in the electric field, the mobile carriers gain sufficient kinetic energy from the electric field, so that their interaction with the lattice atoms produces the excitation of electrons from the valence band into the conduction band. The generation of electron–hole pairs due to energy acquired from the electric field in the semiconductor is referred to as the impact-ionization. Since the electron–hole pairs created by impact-ionization also experience acceleration by the electric field in the depletion region, they participate in the creation of further pairs of electrons and holes. As a result, impact ionization is a multiplicative phenomenon, which produces a cascade of mobile carriers being transported through the depletion region leading to a significant current flow through it. Since the device is unable to sustain the application of higher voltages due to a rapid increase in the current, it is considered to undergo avalanche breakdown. Thus, avalanche breakdown limits the maximum operating voltage for power devices.

The initiation of the avalanche breakdown condition can be analyzed by assuming that the voltage is supported across only one side of the structure. This holds true for an abrupt (metal or *p*)-*n* junction with a very high carrier concentration on one side when compared with the other side. One-dimensional abrupt parallel-plane junction can be used to describe the drift region within power devices. The case of a (metal or p^+)/*n* junction is illustrated in Figure 2.4–1(a) where the p^+ side is assumed to be very highly doped or a metal, so that the electric field supported within it can be neglected. When this junction is reverse-biased by the application of a positive bias to the *n*-region, a depletion region is formed in the *n*-region together with the generation of a strong electric field within it that supports the voltage.

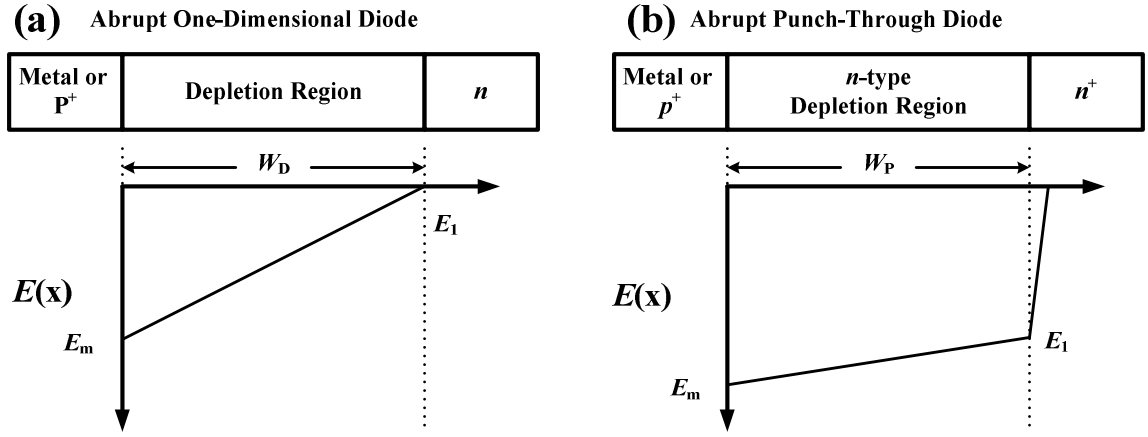


Figure 2.4–1 Electric field for (a) an abrupt parallel-plane (metal or p^+)/n junction and (b) punch-through design for a (metal or p)-i-n junction.

Analytical solution for the avalanche breakdown voltage in abrupt parallel-plane junctions, BV_{pp}, as a function of the donor concentration in the uniformly doped n-region, N_D, the can be derived for GaN [47]:

$$BV_{pp} = 2.87 \times 10^{15} N_D^{-\frac{3}{4}} \qquad 2\text{–}22$$

The avalanche breakdown voltages calculated using this solution is shown in Figure 2.4–2 for GaN material system.

The onset of the avalanche breakdown for an abrupt parallel-plane junction is accompanied by a maximum electric field at the junction referred to as the critical electric field for breakdown, E_C. The critical electric field for wurtzite GaN as a function of doping concentration is given by [47]:

$$E_C = 3.4 \times 10^4 N_D^{\frac{1}{8}} \qquad 2\text{–}23$$

In the case of some power devices designs the resistance of the drift region is greatly reduced during ON-state current flow by the injection of a large concentration of minority carriers. In these cases, the doping concentration of the drift region does not determine the resistance to the ON-state current flow. Consequently, it is preferable to use a thinner depletion region with a reduced doping concentration to support the voltage. This configuration for the drift region is called the punch-through design.

The electric field distribution for the punch-through design is shown in Figure 2.4–1(b). In comparison with the triangular electric field distribution shown in Figure 2.4–1(a), the electric field for the punch-through design takes a trapezoidal shape. The electric field varies more gradually through the drift region due to its lower carrier concentration and then very rapidly with distance within the n^+ end region due to its very high carrier concentration. The electric field at the interface between the drift region and the n^+ end region is given by:

$$E_1 = E_m - \frac{qN_D}{\varepsilon_S} W_P \qquad 2\text{–}24$$

Where E_m is the maximum electric field at the junction, N_D is the doping concentration in the drift region, and W_P is the width of the drift region. The voltage supported by the punch-through diode is given by:

$$V_{PT} = \left(\frac{E_m + E_1}{2} \right) W_P \qquad 2\text{–}25$$

If the small voltage supported within the n^+ end region is neglected. The punch-through

diode undergoes avalanche breakdown when the maximum electric field (E_m) becomes equal to the critical electric field (E_C) for breakdown. Using this condition in Eq. 2–25 together with the field distribution in Eq. 2–24, the breakdown voltage for the punch-through diode is given by:

$$BV_{PT} = E_C W_P - \frac{qN_D W_P^2}{2\varepsilon_S} \qquad 2–26$$

The punch-through breakdown voltages calculated using this relationship are shown in Figure 2.4–2 for GaN with various thicknesses for the drift region. In performing these calculations, the change in the critical electric field with doping concentration was taken into account. For any doping concentration for the drift region, the breakdown voltage for the punch-through diode is reduced due to the truncation of the electric field at the n^+ end region. The breakdown voltage becomes smaller as the thickness of the drift region is reduced.

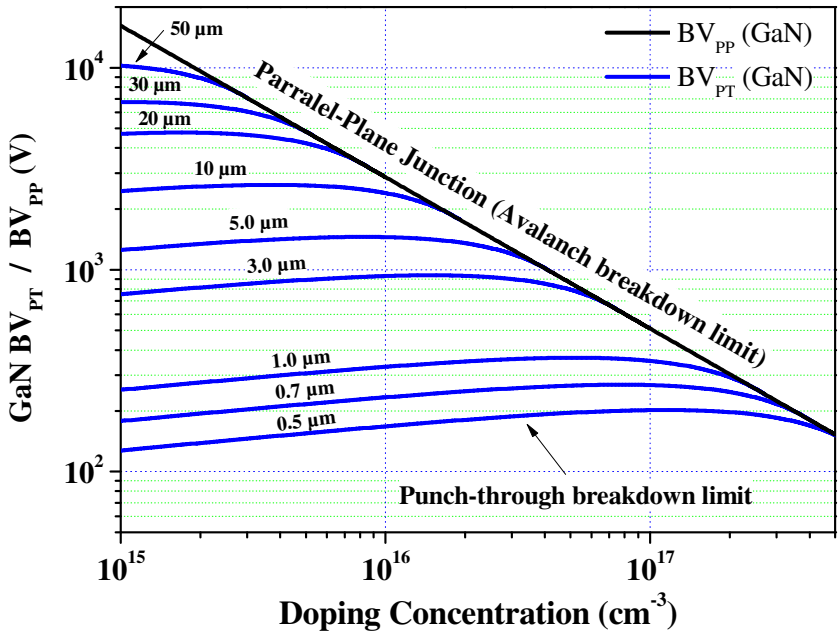


Figure 2.4–2 Breakdown Voltage as function of drift region doping level for GaN.

2.4.2. Power Device Limits Calculation

The semiconductor structures discussed above contain a drift region, which is designed to support the blocking voltage. The properties (doping concentration and thickness) of the ideal drift region can be analyzed by assuming an abrupt junction profile with high carrier concentration on one side and a low uniform carrier concentration on the other side, while neglecting any junction curvature effects by assuming a parallel-plane configuration. The resistance of the ideal drift region can then be related to the basic properties of the semiconductor material. Such semiconductor structure own a triangular electric field distribution, as shown in Figure 2.4–3, within a uniformly doped drift region with the slope of the field profile being determined by the doping concentration.

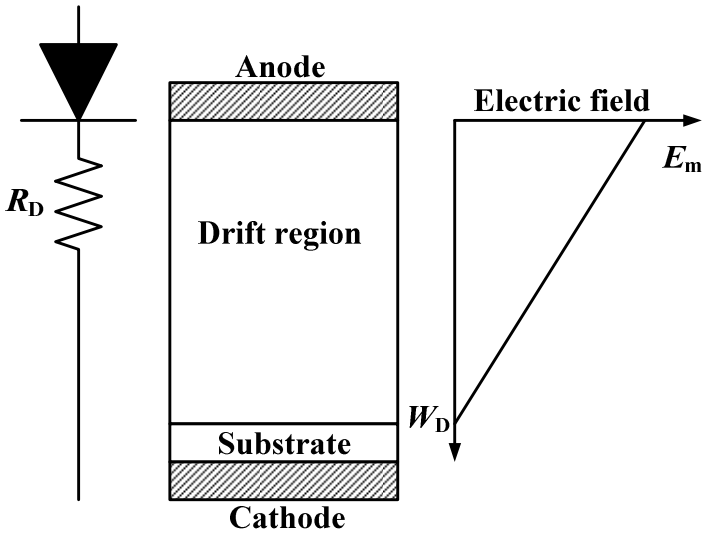


Figure 2.4–3 The ideal drift region and its electric field distribution.

The maximum voltage that can be supported by the drift region is determined by the maximum electric field (E_m) reaching the critical electric field (E_c) for breakdown for the semiconductor material. The critical electric field for breakdown and the doping concentration then determine the maximum depletion width (W_D). The resistance of ideal drift region of area, A, is given by:

$$R \cdot A = \int_0^{W_D} \rho(x)dx = \int_0^{W_D} \frac{dx}{q\mu_n N_D(x)} \qquad 2\text{–}27$$

The specific resistance (resistance per unit area) of the ideal uniformly doped drift region is therefore:

$$R_{on,sp} = \left(\frac{W_D}{q\mu_n N_D} \right) \qquad 2\text{–}28$$

The depletion width under breakdown conditions is given by:

$$W_D = \frac{2BV}{E_C} \qquad 2\text{–}29$$

where BV is the desired breakdown voltage. The doping concentration in the drift region required to obtain this BV is given by:

$$N_D = \frac{\varepsilon_S E_C^2}{2qBV} \qquad 2\text{–}30$$

Combining these relationships, the specific resistance of the ideal drift region is obtained:

$$R_{on-ideal} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3} \qquad 2\text{–}31$$

The denominator of this equation ($\varepsilon_S \mu_n E_C^3$) is commonly referred to as Baliga's figure of merit for power devices. It is an indicator of the impact of the semiconductor material properties on the resistance of the drift region.

Practical specific ON-resistance estimation is calculated using the following approximation [45]:

$$E_C \propto N_D^y \qquad 2\text{–}32$$

and

$$\mu_n \propto N_D^{-x} \qquad 2\text{–}33$$

than

$$R_{ON}\left(\Omega \cdot \mathrm{cm}^2\right) \propto BV^{\alpha} \qquad 2\text{–}34$$

where

$$\alpha = \frac{2-x-y}{1-2y} \qquad 2\text{–}35$$

For GaN [47]:

$$R_{ON}\left(\Omega \cdot \mathrm{cm}^2\right) = 2.4\times10^{-12}\,\mathrm{BV}^{2.5} \qquad 2\text{–}36$$

For 6H-SiC [47]:

$$R_{ON}\left(\Omega \cdot \mathrm{cm}^2\right) = 1.45\times10^{-11}\,\mathrm{BV}^{2.6} \qquad 2\text{–}37$$

For 4H-SiC [44]:

$$R_{ON}\left(\Omega \cdot \mathrm{cm}^2\right) = 2.97\times10^{-12}\,\mathrm{BV}^{2.5} \qquad 2\text{–}38$$

and for Si [44]:

$$R_{ON}\left(\Omega \cdot \mathrm{cm}^2\right) = 5.93\times10^{-9}\,\mathrm{BV}^{2.5} \qquad 2\text{–}39$$

An example of the theoretical, total specific ON-resistance with contributions of drift region (Eq. 2–36, 2–37, 2–38 and 2–39) and contact resistance is presented in Figure 2.4–4 for Si, GaN, 6H-SiC and 4H-SiC. The main advantage of the wide-bandgap materials GaN and SiC is clear: for the same breakdown voltage, they offer a significantly reduced ON-resistance and hence also reduced ON-state losses.

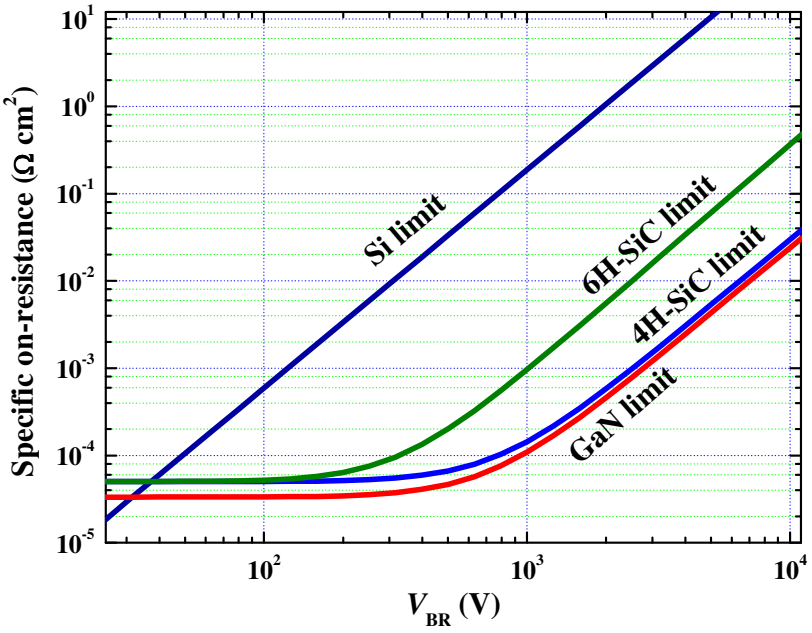


Figure 2.4–4 Sum of specific on resistance of the drift region and the ohmic contact resistance versus breakdown voltage for Si, 4H-SiC, 6H-SiC and GaN.

The theoretical total specific ON-resistance are used as theoretical limits along this work for benchmarking the results in this work with the state-of-the-art devices.

2.5. Breakdown Mechanisms of AlGaN/GaN Based HEMTs

In switching operation the transistors alternate between ON-state were the gate opens the channel and allow the carriers flow through the device and OFF-state were the gate closes the channel and blocks the current of carriers. At OFF-state the gate potential, V_{GS}, is lower than the device's threshold potential, V_{Th}, and considered as subthreshold conditions. For efficient switching the OFF-state operation point conditions should be at high positive drain voltage and negligible drain current therefore a strong gate blocking capability is required. At very high positive drain voltage condition the blocking capability of the device degrades and gives rise to subthreshold leakage, (STL), current. The subthreshold leakage current will increase and become significant then will reduce the efficiency of the switching. A significant leakage current is considered as three orders of magnitude lower than the device's maximal output current therefore a common used value is 1 mA/mm. At high voltages, currents that are higher than this value may initiate destructive processes in the device therefore it is considered to be the starting point of the device breakdown. Thus, the breakdown voltage is usually defined as the voltage at which the drain current exceeds the traditional value of 1 mA/mm in three terminal measurements.

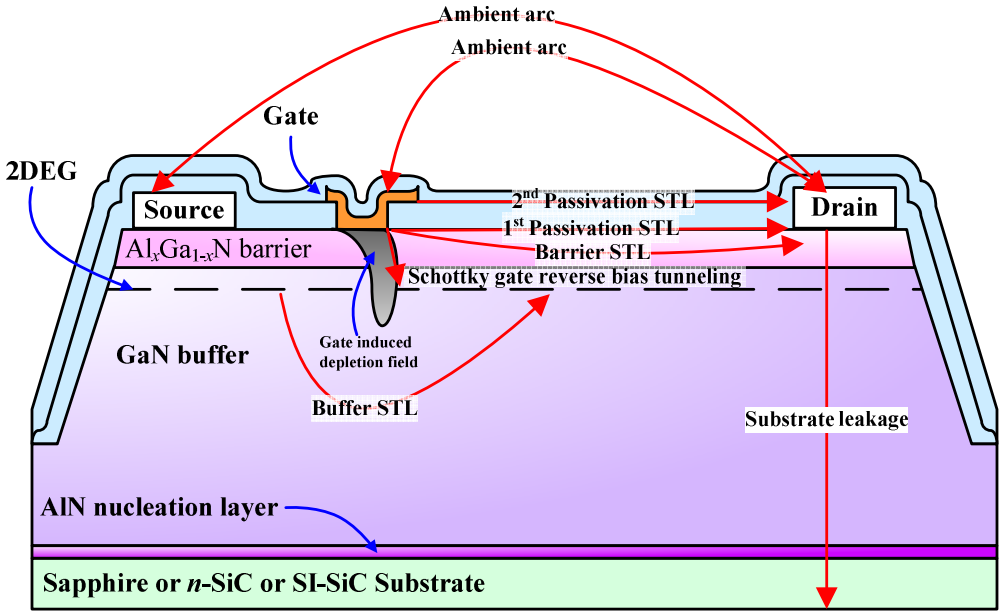


Figure 2.5–1 Illustration of vertical sub-threshold current leakages and breakdown paths in GaN-based HEMTs.

By increasing the potential difference at the drain terminal the charge carriers would drift by electrical forces to the lower potential through intermediate potential levels and states and will reach eventually to the drain terminal. The path of the charge carriers through these intermediate potential states is the device blocking weakness and it determines the mechanisms of the device breakdown. Figure 2.5–1 illustrates the subthreshold leakage paths and mechanisms in conventional AlGaN/GaN based HEMT that can lead to premature breakdown of the device. The paths can be lateral and located in a semiconductor layers, in an insulator layer, in an interfaces between layers, in the ambient or vertical through the substrate.

Enhancement of the device OFF-state breakdown voltage is not a strait-forward task. While

eliminating one source of subthreshold leakage current other weak path give rise to competitive leakage current that may lead to the device excess drain leakage current. Therefore the device's designer use different approaches to eliminate all subthreshold leakages.

Two dominant subthreshold leakage current mechanisms were identified in most of the cases as the cause for lack of OFF-state blocking capability and reaching premature breakdown conditions; the bulk subthreshold leakage current and the Schottky-gate reverse bias tunneling leakage current. Two other pronounced subthreshold current leakage paths are the lateral inter-device insulation, (Mesa insulation) leakage and the substrate vertical leakage in *n*-type SiC substrates.

The characterization on the OFF-state breakdown voltage is clouded by the use of many different measurement techniques. A two-terminal technique is used to measure the gate breakdown; here the Schottky diode is characterized at reverse bias conditions. A three-terminal technique is used to obtain the drain-source breakdown and also the gate-drain breakdown. A variety of criteria are used in extracting the breakdown values from these techniques. Breakdown voltages are extracted either from the shape and slope of the breakdown characteristics or at a given current criteria commonly but not always 1 mA/mm. In addition to the conventional three-terminal breakdown measurement a drain-current injection technique is widely used in throughout this work. Insight to this technique is given in section 2.5.5.

2.5.1. Bulk Subthreshold Leakage Breakdown Mechanism

The bulk subthreshold leakage current is initiated by electron current underneath the depletion region of the transistor gate through the insulating buffer layer and known as space charge inject of electrons into the GaN buffer layer [48], carrier spill-over [49] or buffer layer punch-through effect [50], [51]. The punch-through of the electrons into the buffer causes rapid increase of the sub-threshold drain leakage current and it is often interpreted as the device breakdown-voltage.

An example DC measurements characterization of a device exhibiting an OFF-state breakdown dominated by a subthreshold buffer layer punch-through is shown in Figure 2.5–2. Here, during a three-terminal-conventional breakdown voltage measurement, as shown in Figure 2.5–2(a), the drain current increases rapidly above certain drain bias while the gate current remains orders of magnitudes lower. Also, in a two-terminal Schottky gate diode reverse bias measurements the device exhibits very low reverse bias current, shown in Figure 2.5–2(b) that at a reverse bias of -20 V the leakage current is lower than ~$1e^{-7}$ A/mm. Supporting this assumption is the device drain current-injection three terminal breakdown measurement [52], shown in Figure 2.5–2(c); while forcing the drain current to constant level of 1 mA/mm and closing the gate with negative biasing the drain bias increases attempting to maintain drain current the gate current is monitored. It could be seen that with the increase of the drain voltage the gate diode does not leak and the current does not increase and feed the drain. The current that supply the drain is coming only from the source through the buffer.

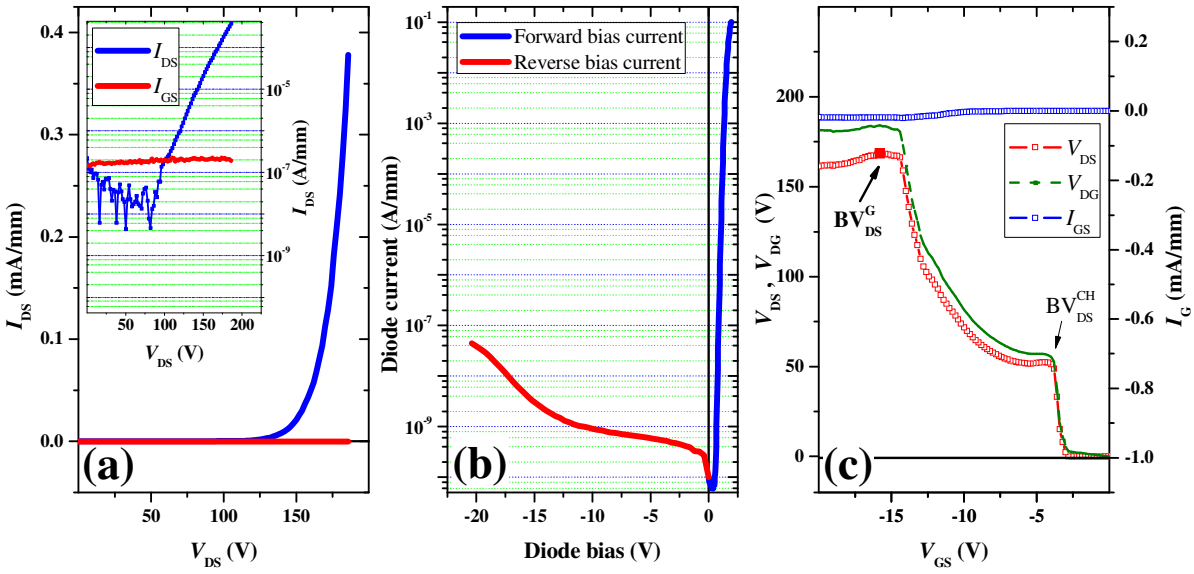


Figure 2.5–2 Example of $V_{BR\ OFF}$ measurement were the buffer leakage dominates the subthreshold leakage current (a) conventional three-terminal breakdown measurement, inset: in logarithmic scale (b) two-terminal Schottky gate diode measurement (c) drain current-injection breakdown measurement [52].

2.5.2. Schottky Gate Reverse Bias Tunneling Leakage Breakdown Mechanism

The Schottky-gate reverse bias tunneling leakage current [53], [54], [55], [56], is dependent on the temperature, the vertical electrical field at the gate edge and the strain of the top-barrier layer and have two dominant mechanisms. The first mechanism is field-emission tunneling from the metal into the semiconductor that becomes significant for large reverse-bias voltages. The second mechanism, is associated with dislocation-related leakage current paths, it is consistent with either one-dimensional variable-range-hopping conduction along the dislocation or trap-assisted tunneling [57].

An example for DC measurements characterization of a device exhibiting an OFF-state breakdown dominated by a Schottky drain reverse bias tunneling subthreshold current is shown in Figure 2.5–3. Here, during a three-terminal-conventional breakdown voltage measurement, as shown in Figure 2.5–3(a) and the inset, the gate and the drain leakage currents are equal with opposite sign and increases rapidly with the increase of the drain bias. The two-terminal Schottky gate diode reverse bias measurements shows that this device exhibits very high reverse bias current, shown in Figure 2.5–3(b) that at a reverse bias of -20 V the leakage current reaches a value of ~1e^{-4} A/mm.

The drain current-injection three-terminal breakdown measurement for this device gives solid indication to the gate leakage and is shown in Figure 2.5–3(c). As the gate bias become more negative and closes the channel a rapid increase in the gate current is seen and it reaches the value of 1 mA/mm, i.e. Schottky gate is strongly leaking and the entire drain current is supplied from the gate terminal.

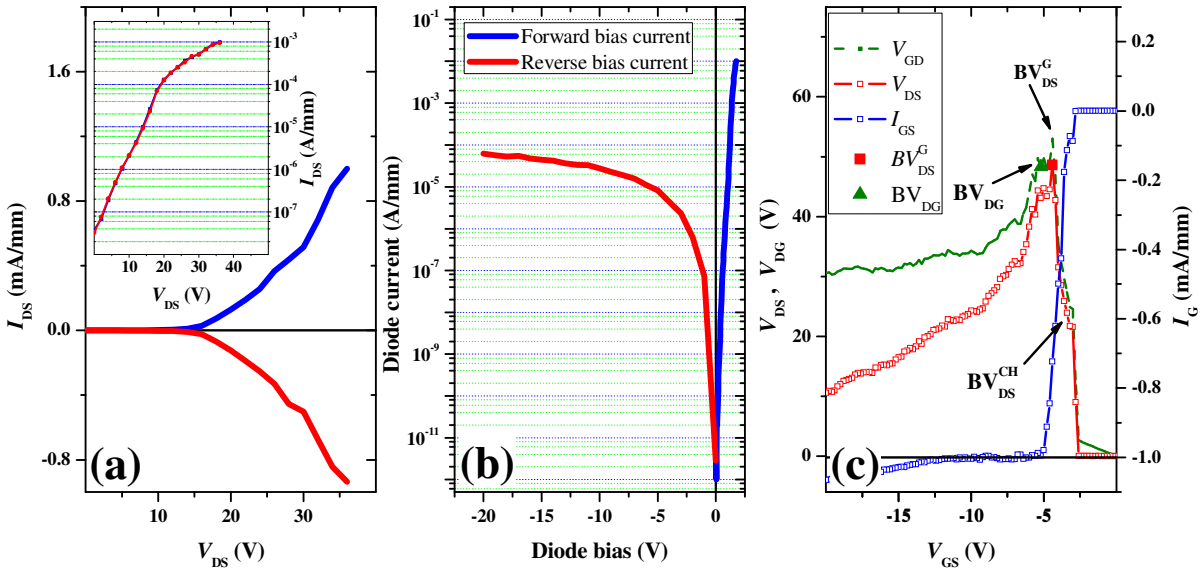


Figure 2.5–3 Example of $V_{BR\ OFF}$ measurement were the Schottky gate reverse bias tunneling leakage dominates the subthreshold leakage current (a) conventional three-terminal breakdown measurement, inset: in logarithmic scale (b) two-terminal Schottky gate diode measurement (c) drain current-injection breakdown measurement [52].

2.5.3. Inter-Device Insulation and Substrate Leakage Breakdown Mechanism

Inter-device (Mesa)-insulation hinders carrier currents not only between neighboring devices but also provide insulation at OFF-state conditions between the source and drain ohmic contact terminals within the device it self. Lack of inter-device insulation at high voltage OFF-state operation could be a weak link and provide the path for carriers to subthreshold leakage current. Inter-device insulation leakage and the substrate leakage are often difficult to distinguish and may have similar characteristics. Here given examples for both leakage currents and the method to distinguish between them.

The inter-device insulation leakage is dependent on the Mesa insulation type, Mesa recess using Cl_2/BCl_3 reactive ion etching and multi-energy implantation inter-device insulation. In the case of etched Mesa, conductive states created at the edge of the active area used as a path to carriers at high voltage conditions. In addition in this case the gate Schottky metal crosses a carrier reach zone, the 2DEG, and creates a gate leakage.

Inter-device insulation can also be made using $^{14}N^{+}$ multi-energy implantation. Here two leakage mechanisms can origin subthreshold leakage currents, to little implantation can leave the strain structure of the AlGaN top-barrier and remain of the 2DEG electron reach volumes, or excessive implantation can create conductive defects in the GaN buffer.

Figure 2.5–4(b) illustrates the path for inter-device (Mesa)-insulation leakage. At OFF-state high drain voltage conditions the carriers from the carrier-reach active area can laterally bypass the gate edge depletion region and give rise to substantial leakage. The inter-device insulation quality and its leakage measurement are carried out using a special meander test structure, illustrated in Figure 2.5–4(c), with minimum lateral spacing of 5 µm between two conductive ohmic contact stripes separated by inter-device insulation. Figure 2.5–4(a) compares example of two terminal inter-device insulation test measurements of device with etched mesa insulation and device with optimized multi-energy ion implantation inter-device insulation. Reduction of orders of magnitude of the leakage current and increase of hundred of volts of the structure breakdown is observed with the use of inter-device multi-energy implantation make it the favorable choice to be used in high voltage devices (see section 8.2).

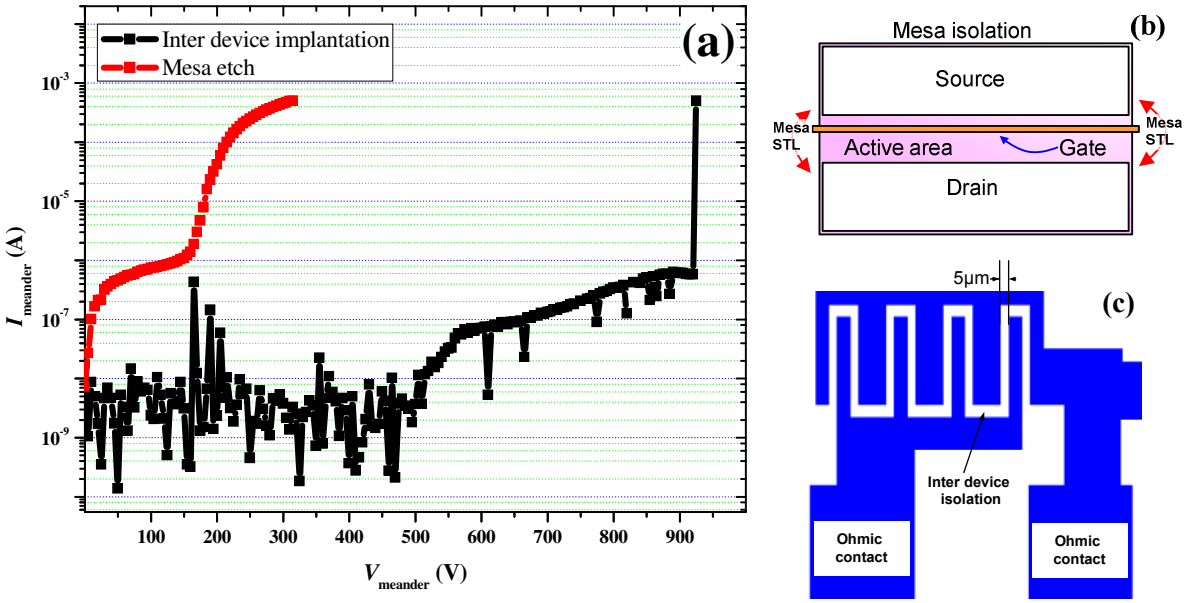


Figure 2.5–4 (a) Example of two-terminal $V_{BR\ OFF}$ measurement of test insulation meander structure on Sapphire wafer (b) Top-view illustration of lateral sub-threshold current leakages and breakdown paths in GaN-based HEMTs inter-device (Mesa)-insulation (c) Top-view illustration of meander inter-device (Mesa)-insulation test structure.

GaN–based HEMTs grown on *n*-SiC substrates often exhibit a substantial substrate leakage. This leakage current flows from one terminal vertically down to the substrate and back up to the other terminal. Figure 2.5–5 illustrates DC characterization measurements of device manufactured on *n*-SiC substrate that exhibit an excessive substrate leakage. Here, during a three-terminal-conventional OFF-state breakdown voltage measurement, as shown in Figure 2.5–5(a), the drain increases rapidly above a certain drain bias while the gate current remains lower. The two-terminal Schottky gate diode reverse bias measurements shows that the device exhibits very low reverse bias current, shown in Figure 2.5–5(b), at a reverse bias of -20 V the leakage current is lower than ~1e^{-7} A/mm.

The two terminal substrate and inter-device insulation breakdown voltage measurements are shown in Figure 2.5–5(c). A rapid increase in the substrate leakage is observes with the increase of the two terminal potential indicate that this vertical structure can not block voltage above 150 V. The inter-device insulation breakdown test show about twice higher breakdown voltage which is an indication that the carriers travel vertically through the buffer into the conductive substrate, bypassing the highly resistive inter-device insulation volume and drift back to the second terminal.

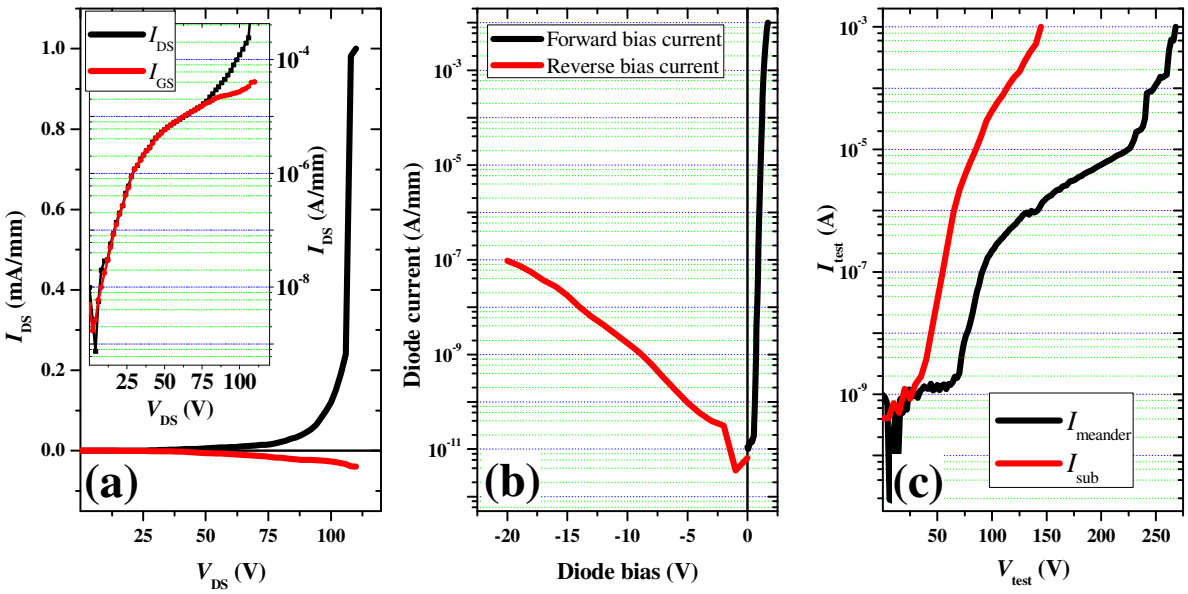


Figure 2.5–5 Example of $V_{BR\ OFF}$ measurement were the substrate leakage dominates the subthreshold leakage current (a) conventional three-terminal breakdown measurement, inset: in logarithmic scale (b) two-terminal Schottky gate diode measurement (c) two terminal lateral inter-device insulation and vertical substrate breakdown measurement.

Figure 2.5–6 compares three cases of epitaxial design with different level of substrate insulation. (a) and (b) depict structures grown on *n*-SiC substrate, with excessive substrate leakage and with enhances substrate insulation respectively. It could be seen that in comparison to epitaxial stack grown on SI-SiC wafer (c) they suffer from orders of magnitude more leakage current that could be the source of current for premature device breakdown.

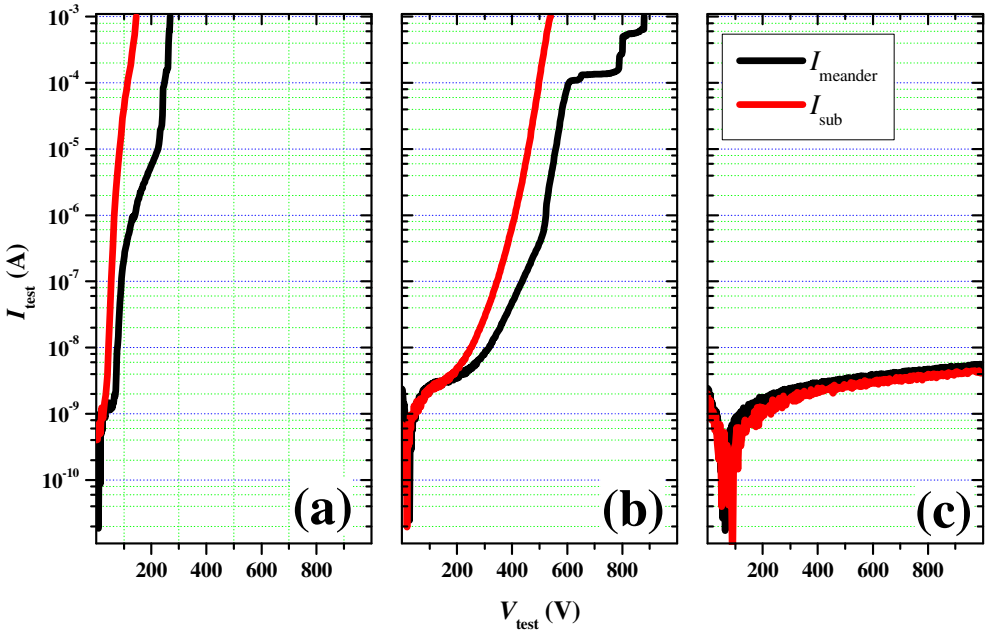


Figure 2.5–6 Example of two terminal lateral inter-device insulation and vertical substrate breakdown measurement with (a) strong vertical substrate leakage-current (on *n*-SiC substrate) (b) reduced vertical substrate leakage-current (on *n*-SiC substrate) (c) negligible substrate leakage-current (on SI-SiC substrate).

2.5.4. Other Subthreshold Leakage Sources and ruinous Breakdown Mechanisms

In addition to the major subthreshold leakage current mechanisms there are less pronounced possible leakage current paths in AlGaN/GaN based HEMTs believed to lead for a device breakdown and rapid ruinous failures that destroy the device: The path between the gate and the drain contacts through the AlGaN-SiN_x passivation interface and/or other SiN_x passivation interface, the path between the gate and the drain-electrode through the AlGaN barrier layer. A common destructive failure occurs at high voltages is arcing through the air, and the path between neighboring electrodes through the ambient (Arc). Section 8.1 describes geometrical layouts modifications to postponed arcing and other ruinous breakdown in the device.

2.5.5. Drain-Current Injection Technique for the Measurement of OFF-State Breakdown Voltage [52]

For many applications, the OFF-state drain-source breakdown voltage BV_{DS} is an important parameter. BV_{DS} is typically defined as the drain voltage of the turned-off device, where a sharp rise in I_D occurs on the output *I-V* characteristics. It does not necessarily imply that breakdown occurs in the channel; it could equally occur between drain and gate. BV_{DS} cannot be a precisely defined value because of the following two reasons. First is the difficulty in defining the threshold voltage V_{Th}, especially for short-channel devices. Second is the dependence of BV_{DS} on V_{GS}. There is, however, a particular value of BV_{DS} which is uniquely defined. This is the maximum drain-source voltage the device can attain for a given drain-current criteria. At this bias point V_{DS} is limited by gate breakdown. Therefore this point is labeled as BV_{DS}^{G}.

Bahl *et al*. presented a Drain-current Injection technique to unambiguously measure both BV_{DS} and BV_{DG}, which overcomes the above difficulties. The schematic of the technique is shown in Figure 2.5–7.

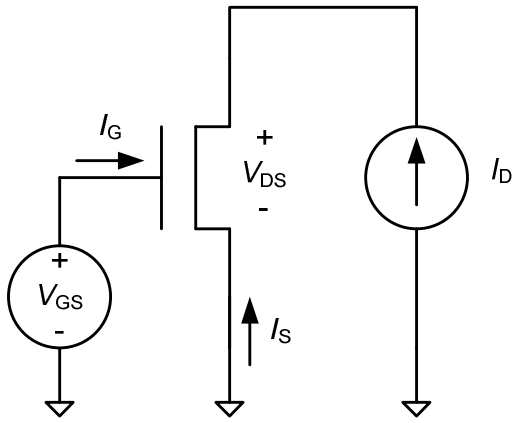


Figure 2.5–7 Schematic circuit diagram for drain-current injection technique.

To characterize breakdown, a fixed predefined current is injected into the drain, the gate-source voltage is ramped down from a strong forward bias to below threshold, and V_{DS} and I_G are monitored. The technique traces the locus of V_{DS}, V_{DG}, and I_G versus V_{GS} at fixed I_D on the output *I-V* characteristics. BV_{DS}^{G} is unambiguously defined as the maximum V_{DS} attained, irrespective of V_{GS}. BV_{DG} is defined at $I_D = -I_G$, i.e., $I_S = 0$. Additionally, the onset of channel breakdown can also be observed in some cases. This point is denoted as BV_{DS}^{Ch}.

Chapter 3

Physical Based Simulation Model for AlGaN/GaN HEMTs

This Chapter gives overview on GaN-based HEMTs physical based device simulation using Silvaco-"ATLAS". Physical based models that describe the properties of the semiconductor material are introduced. A detailed description of the specific AlGaN/GaN HEMT structure definition and geometries are given along with the complex fine meshing requirements. Nitride semiconductor specific material properties and their physical models are reviewed focusing on the energetic band structure, epitaxial strain tensor calculation in wurtzite materials and build-in polarization models. Special attention for thermal conductivity, carriers' mobility and Schottky gate reverse bias tunneling is paid. Empirical parameters matching and adjustment of models parameters to match the experimental device measured results are discussed. The simulation can then serve as a useful engineering tool for design, analysis and evaluation of innovative concepts.

3.1. Introduction to GaN-Based HEMT Physical Based Simulation

GaN-based devices and specially AlGaN/GaN HEMTs are relatively new type of semiconductor devices [58] and therefore the practical and experimental common knowledge of such devices, their physical characteristics and performance are unlike Si devices very limited. In many cases the developers of such devices are not willing to reveille their intellectual properties due to tight competition. On the other hand experimental results are very expensive and very time consuming. In order to get over these limitations the device designer need a reliable tool for prediction of the device performance in short time and low coast before device tape out, set of masks manufacturing, epitaxial growth on expansive wafers and very expansive clean room time. A common and useful tool for design and prediction semiconductor devices is the physically-based device simulation. Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a two or three dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, onto this grid it can simulate the transport of carriers through a structure. This means that the electrical performance of a device can now be modeled in DC, AC or transient modes of operation. Physically-based simulation is predictive; it provides insight to the device, it conveniently captures and visualizes theoretical knowledge. Physically-based simulation is different from empirical modeling. The goal of empirical modeling is to obtain analytic formulae that approximate existing data with good accuracy and minimum complexity. Empirical models provide efficient approximation and interpolation. They do not provide insight, or predictive capabilities, or encapsulation of theoretical knowledge. Physically-based simulation has become very important for two reasons. One, it is almost always much quicker and cheaper than performing experiments. Two, it provides information that is difficult or impossible to measure. The drawbacks of physically-based simulation are that all the relevant physics must be incorporated into a simulator. Also, numerical procedures must be implemented to solve the associated equations.

3.2. Basic Modeling of the Physically Based Simulator

Silvaco "ATLAS" [59], a physically-based simulator uses mathematical model to describe any semiconductor device. This model consists of a set of fundamental equations, which link together the electrostatic potential and the carrier densities, within some simulation domain. These equations, which are solved inside any general purpose device simulator, have been derived from Maxwell's laws and consist of Poisson's Equation, the continuity equations and the transport equations. Poisson's Equation relates variations in electrostatic potential to local charge densities. The continuity and the transport equations describe the way that the electron and hole densities evolve as a result of transport processes, generation processes, and recombination processes.

Poisson's Equation relates the electrostatic potential to the space charge density:

$$div\left(\varepsilon\nabla\psi\right)=-\rho \qquad 3\text{–}1$$

where ψ is the electrostatic potential, ε is the local permittivity, and ρ is the local space charge density. The local space charge density is the sum of contributions from all mobile and fixed charges, including electrons, holes, and ionized impurities. The electric field is obtained from the gradient of the potential.

$$\vec{E} = -\nabla \psi \qquad 3\text{–}2$$

The continuity equations for electrons and holes are defined by equations:

$$\frac{\partial n}{\partial t} = \frac{1}{q} div\vec{J}_n + G_n - R_n \qquad 3\text{–}3$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} div\vec{J}_p + G_p - R_p \qquad 3\text{–}4$$

where n and p are the electron and hole concentration, $\vec{J}_n$ and $\vec{J}_p$ are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rates for electrons and holes, and q is the magnitude of the charge on an electron.

Poisson's equation (Eq. 3–1) and the carrier continuity equations (Eq. 3–3 and Eq. 3–4) provide the general framework for device simulation. But further secondary equations are needed to specify particular physical models for: $\vec{J}_n$, $\vec{J}_p$, G_n, R_n, G_p and R_p.

The current density equations, or charge transport models, are usually obtained by applying approximations and simplifications to the Boltzmann Transport Equation. These assumptions can result in a number of different transport models such as the drift-diffusion model, the Energy Balance Transport Model or the hydrodynamic model. The choice of the charge transport model will then have a major influence on the choice of generation and recombination models.

The simplest model of charge transport that is useful is the drift-diffusion model. This model has the attractive feature that it does not introduce any independent variables in addition to ψ, n and p. Until recently, the drift-diffusion model was adequate for nearly all devices that were technologically feasible. The drift-diffusion approximation, however, becomes less accurate for smaller feature sizes. More advanced energy balance and hydrodynamic models are therefore becoming popular for simulating deep submicron devices. "ATLAS" supplies both drift-diffusion and advanced transport models.

Silvaco "ATLAS" uses an internal general purpose 2D device simulator, "BLAZE", for III-V, II-VI materials, and devices with position dependent band structure (e.g., heterojunctions). "BLAZE" accounts for the effects of positionally dependent band structure by modifications to the charge transport equations and Poisson's equation. "BLAZE" is applicable to a broad range of devices such as: HBTs, HEMTs, LEDs, lasers, heterojunction photodetectors (e.g., APDs, solar cells) and heterojunction diodes.

"GIGA", internal simulator, extends "ATLAS" to account for lattice heat flow and general thermal environments. "GIGA" implements Wachutka's thermodynamically rigorous model of lattice heating [60], which accounts for Joule heating, heating and cooling due to carrier generation and recombination, and the Peltier and Thomson effects. It accounts for the dependence of material and transport parameters on the lattice temperature. It also supports the specification of general thermal environments using a combination of realistic heat-sink structures, thermal impedances, and specified ambient temperatures. "GIGA" works with "BLAZE" and with both the drift-diffusion and energy balance transport models.

3.3. GaN-Based HEMTs Simulation Structures, Models and Parameters

The following section describes the methodology used in the physically based simulations of nitride based HEMTs devices. It is desired to match the simulation out put characteristics to the actual electrical and physical performance of a typical manufactured device. Here the

simulated device-structure is analyzed and matched to the standard device fabricated in FBH's clean room. The matching process starts with the definition of the simulated structure, its fraction to fine elements by adequate progressive meshing and the materials building blocks. The simulation manual recommends models for use and has a build in material parameters tables based on the latest research results. Unfortunately, as could be seen in the following sections, it is not sufficient; the recommendations are not specific and does not include many of the required models for accurate description of a GaN-based HEMTs and other field effect devices. Therefore, additional models along with empirical modification in the existing models and parameters are required in order to achieve a useful tool for the device designer and researcher as a first order approximation.

3.3.1. Structure and Mesh Definition for the Simulation

Exact definition of the structure for the simulation is one of the basic keys to match the simulations electrical calculations out put to the experimental electrical measurements of typical GaN-based HEMT. The structure should match the wafer substrate, the epitaxial layers growth, the device layers layout and the process capabilities.

For the device electrical matching the simulated structure is based on Semi-Insulating (SI) 4H-SiC substrate. The epitaxial growth layers are defined exactly as in the reference wafer; ~50 nm AlN wetting layer, 2.4 µm UID GaN buffer layer and 25 nm $Al_{0.25}Ga_{0.75}N$ barrier layer. Device structure geometry shown in Figure 3.3–1 having L_G =2 ×50µm = 100 µm, L_{SG} = 1.0 µm, L_{GD} = 2 µm matches the layout of FBH GaN technology standard monitoring transistors (2 × 50 µm A2). The gate structure matched to the T-gate process geometry with gate foot-print of 0.4 µm and 0.2 µm symmetrical gate "wings" and a uniformly deposit 300 nm Si_3N_4 serves as a device passivation.

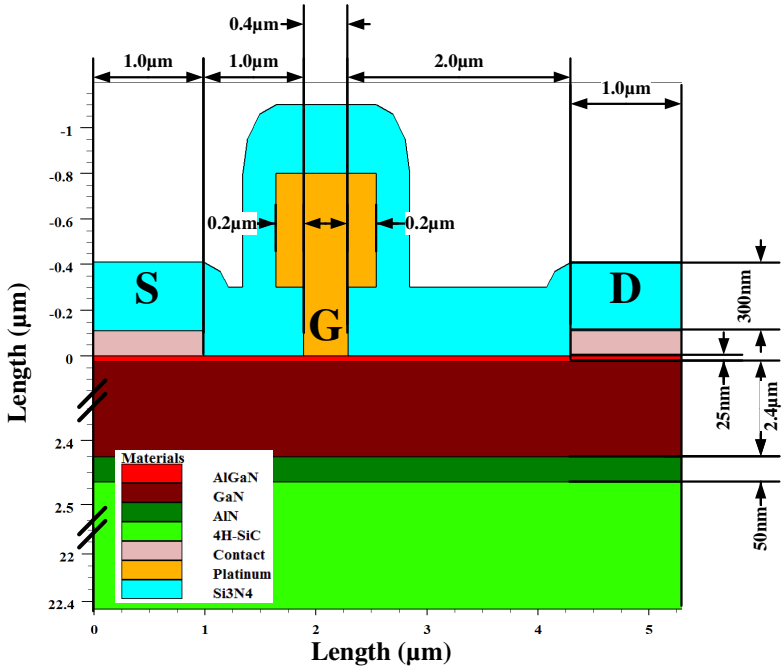


Figure 3.3–1 GaN base HEMT basic simulation structure.

Next step after the device structure creation is to generate an adequate mesh which could be used by Silvaco "ATLAS" simulator. Specifying a good grid is a crucial issue in device simulation. But, there is a trade-off between the requirements of accuracy and numerical efficiency. Accuracy requires a fine grid that resolves the structure in solutions. Numerical efficiency is greater when fewer grid points are used. The critical areas to resolve are difficult

to generalize because they depend on the technology and the transport phenomena. The only generalization possible is that most critical areas tend to coincide with reverse-biased metallurgical junctions. Typical critical areas in GaN-based HEMTs are: Around heterojunctions and interfaces, areas with high electric fields at the drain/channel junction and areas with transverse electric field beneath the Schottky gate. Figure 3.3–2 shows a GaN based HEMT structure with typical mesh. This mesh contains ~33,100 mesh points (nodes) and ~66,000 meshing triangles. The meshing points and triangles number increased rapidly with the introduction of complex epitaxial stacks and structural changes such as field-plates.

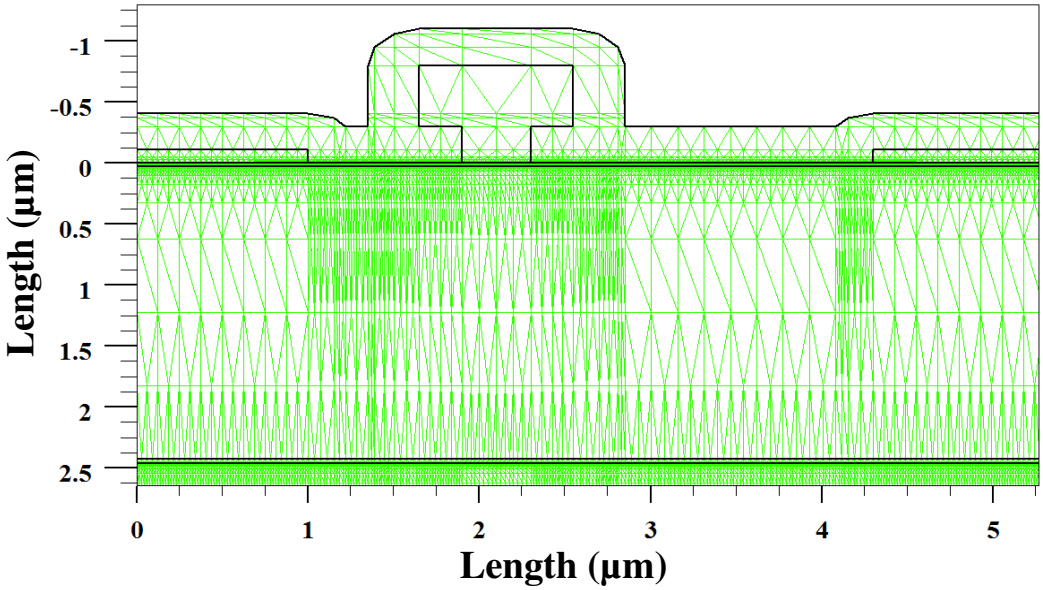


Figure 3.3–2 Mesh of GaN base HEMT basic simulation structure.

3.3.2. Material Parameters and Physical Models

The simulation of GaN-based HEMTs using Silvaco "ATLAS" requires specific definitions and use of physical models that describe the material properties of nitride compounds. Silvaco "ATLAS" contains many build-in physical models and material properties that can be used to simulate such devices. Here are the models used by the simulation to define the physical properties of the materials presented by the order in the simulation's scripts.

3.3.2.1. Nitride Material Properties: Bend gap, Electron Affinity, Permittivity and Density of States Masses

The following sections describe the relationship between mole fraction, *x*, and the material parameters and various physical models specific to the $Al_xGa_{1-x}N$ system. By default, the bandgap for the nitrides is calculated in a two step process. First, the bandgap(s) of the relevant binary compounds are computed as a function of temperature, *T*, using [61]:

$$E_g(\mathrm{GaN}) = 3.507 - \frac{0.909\times10^{-3}T^2}{T+830.0} \qquad 3\text{–}5$$

$$E_g(\mathrm{AlN}) = 1.994 - \frac{0.245\times10^{-3}T^2}{T-624} \qquad 3\text{–}6$$

Then, the dependence on composition fraction, *x*, is described [62]:

$$E_g(\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N}) = E_g(\mathrm{AlN})x + E_g(\mathrm{GaN})(1-x) - 1.3x(1-x) \qquad 3\text{–}7$$

The electron affinity is calculated such that the band edge offset ratio is given by [62]:

$$\frac{\Delta E_c}{\Delta E_v} = \frac{0.7}{0.3} \qquad 3\text{–}8$$

The permittivity of the nitrides as a function of composition fraction, x, is given by linear interpolations of the values for the binary compounds [63].

$$\varepsilon\left(\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N}\right) = -0.3x + 10.4 \qquad 3\text{–}9$$

The nitride density of states masses as a function of composition fraction, x, is given by linear interpolations of the values for the binary compounds [61]:

$$m_e\left(\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N}\right) = 0.314x + 0.2(1-x) \qquad 3\text{–}10$$

$$m_h\left(\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N}\right) = 0.417x + 1.0(1-x) \qquad 3\text{–}11$$

3.3.2.2. Epitaxial Strain Tensor Calculation in Wurtzite Materials and Build-in Polarization Models

The strain tensor in epitaxial layers is used to calculate piezoelectric polarization [22] and/or in gain modeling [64], [65], [66]. In epitaxial layers, the strain tensor can be represented by ε_{xx}, ε_{yy}, ε_{zz}, ε_{xy}, ε_{yz} and ε_{zx}. The relationships between the various components of the strain tensor are given by:

$$\varepsilon_{xx} = \varepsilon_{yy} = \frac{a_s - a_0}{a_0} \qquad 3\text{–}12$$

$$\varepsilon_{zz} = -2\frac{C_{13}}{C_{33}}\varepsilon_{xx} \qquad 3\text{–}13$$

$$\varepsilon_{xy} = \varepsilon_{yz} = \varepsilon_{zx} = 0 \qquad 3\text{–}14$$

where C_{13} and C_{33} are elastic constants. The parameter a_0 is the lattice constant in the "reference substrate"

Polarization in wurtzite materials, such as N-III based materials family, is characterized by two components, spontaneous polarization, P_{sp}, and piezoelectric polarization, P_{pi}. Therefore, the total polarization, P_{total}, is given by:

$$P_{\text{total}} = P_{sp} + P_{pi} \qquad 3\text{–}15$$

The piezoelectric polarization, P_{pi}, is given by:

$$P_{pi} = 2\frac{a_s - a_0}{a_0}\left(e_{31} - \frac{C_{13}}{C_{33}}e_{33}\right) \qquad 3\text{–}16$$

where e_{31} and e_{33} are piezoelectric constants, and C_{13} and C_{33} are elastic constants. The a_0 parameter is the lattice constant of the material layer in question. The a_s parameter is the average value of the lattice constants of the layers directly above and below the layer in question.

The polarization enters into the simulation as a positive and negative fixed charges appearing at the top and bottom of the layer in question. By default, the positive charge is added at the bottom and the negative charge is added at the top.

3.3.2.3. Chuang's Three Band Model for Gain and Radiative Recombination in Wurtzite Materials

Chuang's model [64], [65], [66] is derived from the $k \cdot p$ method for three valence bands in wurtzite crystalline structure. Given the assumptions of parabolic bands, no valence band mixing and momentum approaching zero, the following approach can be used. The matrix elements for a strained wurtzite semiconductor are:

$$\theta_\varepsilon = D_3\varepsilon_{zz} + D_4\left(\varepsilon_{xx} + \varepsilon_{yy}\right) \qquad 3\text{–}17$$

$$\lambda_\varepsilon = D_1\varepsilon_{zz} + D_2\left(\varepsilon_{xx} + \varepsilon_{yy}\right) \qquad 3\text{–}18$$

Here, D_1, D_2, D_3, and D_4 are shear deformation potentials and ε_{xx}, ε_{yy}, and ε_{zz}, are taken from the strain tensor calculations described in section 3.3.2.2. Next, the simulation calculates the valence band energies from:

$$E_{hh}^0 = E_v^0 + \Delta_1 + \Delta_2 + \theta_\varepsilon + \lambda_\varepsilon \qquad 3\text{–}19$$

$$E_{lh}^0 = E_v^0 + \frac{\Delta_1 - \Delta_2 + \theta_\varepsilon}{2} + \lambda_\varepsilon + \sqrt{\left(\frac{\Delta_1 - \Delta_2 + \theta_\varepsilon}{2}\right)^2 + 2\Delta_3^2} \qquad 3\text{–}20$$

$$E_{ch}^0 = E_v^0 + \frac{\Delta_1 - \Delta_2 + \theta_\varepsilon}{2} + \lambda_\varepsilon - \sqrt{\left(\frac{\Delta_1 - \Delta_2 + \theta_\varepsilon}{2}\right)^2 + 2\Delta_3^2} \qquad 3\text{–}21$$

Here, Δ_1, Δ_2 and Δ_3 are split energies and E_v^0 is the valence band reference level. Next, the simulation calculates the hydrostatic energy shift from:

$$P_{c\varepsilon}^0 = a_{cz}\varepsilon_{zz} + a_{ct}\left(\varepsilon_{xx} + \varepsilon_{yy}\right) \qquad 3\text{–}22$$

Here, a_{cz} and a_{ct} are hydrostatic deformation potentials. From which the simulation calculates the conduction band energy:

$$E_c^0 = E_v^0 + \Delta_1 + \Delta_2 + E_g + P_{c\varepsilon} \qquad 3\text{–}23$$

Here, E_g is the energy bandgap.

Next, the simulation calculates the effective masses in the various bands:

$$m_{hh}^z = -m_0\left(A_1 + A_3\right)^{-1} \qquad 3\text{–}24$$

$$m_{hh}^t = -m_0\left(A_2 + A_4\right)^{-1} \qquad 3\text{–}25$$

$$m_{lh}^z = -m_0\left[A_1 + \left(\frac{E_{lh}^0 - \lambda_\varepsilon}{E_{lh}^0 - E_{ch}^0}\right)A_3\right]^{-1} \qquad 3\text{–}26$$

$$m_{lh}^t = -m_0\left[A_2 + \left(\frac{E_{lh}^0 - \lambda_\varepsilon}{E_{lh}^0 - E_{ch}^0}\right)A_4\right]^{-1} \qquad 3\text{–}27$$

$$m_{ch}^z = -m_0\left[A_1 + \left(\frac{E_{ch}^0 - \lambda_\varepsilon}{E_{ch}^0 - E_{lh}^0}\right)A_3\right]^{-1} \qquad 3\text{–}28$$

$$m_{ch}^{t} = -m_0\left[A_2 + \left(\frac{E_{ch}^0 - \lambda_\varepsilon}{E_{ch}^0 - E_{lh}^0}\right)A_4\right]^{-1} \qquad 3\text{–}29$$

Here, m_0 is the free space mass of an electron, m_{hh}^{z}, m_{hh}^{t}, m_{lh}^{z}, m_{lh}^{t}, m_{ch}^{z} and m_{ch}^{z} are the effective masses for heavy holes, light holes and crystal split of holes in the axial and transverse directions and A_1, A_2, A_3 and A_4 are hole effective mass parameters.

The momentum matrix elements for the various transitions are calculated by the simulation using:

$$M_{hh}\,\|= 0 \qquad 3\text{–}30$$

$$M_{lh}\,\|= b^2\left(\frac{m_0}{2}E_{pz}\right) \qquad 3\text{–}31$$

$$M_{ch}\,\|= a^2\left(\frac{m_0}{2}E_{pz}\right) \qquad 3\text{–}32$$

$$M_{hh}\,\perp= \frac{m_0}{4}E_{px} \qquad 3\text{–}33$$

$$M_{lh}\,\perp= a^2\left(\frac{m_0}{4}\right)E_{px} \qquad 3\text{–}34$$

$$M_{ch}\,\perp= b^2\left(\frac{m_0}{4}\right)E_{px} \qquad 3\text{–}35$$

Here, E_{px} and E_{pz} P_1^2, P_2^2 a^2 and b^2 are given by:

$$E_{px} = \left(2m_0/\hbar^2\right)P_2^2 \qquad 3\text{–}36$$

$$E_{pz} = \left(2m_0/\hbar^2\right)P_1^2 \qquad 3\text{–}37$$

$$P_1^2 = \frac{\hbar^2}{2m_0}\left(\frac{m_0}{m_e^z} - 1\right)\frac{\left(E_g + \Delta_1 + \Delta_2\right)\left(E_g + 2\Delta_2\right) - 2\Delta_3^2}{\left(E_g + 2\Delta_2\right)} \qquad 3\text{–}38$$

$$P_2^2 = \frac{\hbar^2}{2m_0}\left(\frac{m_0}{m_e^t} - 1\right)\frac{E_g\left[\left(E_g + \Delta_1 + \Delta_2\right)\left(E_g + 2\Delta_2\right) - 2\Delta_3^2\right]}{\left(E_g + \Delta_1 + \Delta_2\right)\left(E_g + 2\Delta_2\right) - 2\Delta_3^2} \qquad 3\text{–}39$$

$$a^2 = \left(\frac{E_{lh}^0 - \lambda_\varepsilon}{E_{lh}^0 - E_{ch}^0}\right) \qquad 3\text{–}40$$

$$b^2 = \left(\frac{E_{ch}^0 - \lambda_\varepsilon}{E_{ch}^0 - E_{lh}^0}\right) \qquad 3\text{–}41$$

Note that $a^2 + b^2 = 1$. Here m_e^t and m_e^z are the transverse and axial conduction band effective masses. The simulation uses default values for the parameters of this model.

3.3.2.4. Thermal Conductivity Definition and Parameters

The simulation adds the heat flow equation to the primary equations that are solved by "ATLAS". The heat flow equation has the form:

$$C\frac{\partial T_L}{\partial t} = \nabla\left(\kappa\nabla T_L\right) + H \qquad 3\text{–}42$$

where C is the heat capacitance per unit volume, κ is the thermal conductivity, H is the heat generation and T_L is the local lattice temperature. The heat capacitance can be expressed as $C = \rho C_p$, where C_p is the specific heat and ρ is the density of the material. Because thermal conductivity is generally temperature dependent, the following form is used.

$$\kappa(T) = \frac{1}{\left(\mathrm{Tc_A} + \mathrm{Tc_B}T_L + \mathrm{Tc_C}T_L^2\right)} \qquad 3\text{–}43$$

The $\mathrm{Tc_A}$, $\mathrm{Tc_B}$ and $\mathrm{Tc_C}$ are material specific fitting parameters.

For transient calculations, specify heat capacities for every region in the structure. These are also functions of the lattice temperature and are modeled as:

$$C(T) = \mathrm{Hc_A} + \mathrm{Hc_B}T_L + \mathrm{Hc_C}T_L^2 + \frac{\mathrm{Hc_D}}{T_L^2} \qquad 3\text{–}44$$

The $\mathrm{Hc_A}$, $\mathrm{Hc_B}$, $\mathrm{Hc_C}$ and $\mathrm{Hc_D}$ are material specific fitting parameters.

When thermal calculation simulator is used, the electron and hole current densities are modified to account for spatially varying lattice temperatures:

$$\overrightarrow{J_n} = -q\mu_n n\left(\nabla\phi_n + P_n\nabla T_L\right) \qquad 3\text{–}45$$

$$\overrightarrow{J_p} = -q\mu_p p\left(\nabla\phi_p + P_p\nabla T_L\right) \qquad 3\text{–}46$$

where: P_n and P_p are the absolute thermoelectric powers for electrons and holes.

When carrier transport is handled in the drift-diffusion approximation the heat generation term, H, used in Eq. 3–42 has the form:

$$\begin{aligned} H = {} & \frac{\left|\overrightarrow{J_n}\right|^2}{q\mu_n n} + \frac{\left|\overrightarrow{J_p}\right|^2}{q\mu_p p} - T_L\left(\overrightarrow{J_n}\nabla P_n\right) - T_L\left(\overrightarrow{J_p}\nabla P_p\right) \\ & + q(R-G)\left[T_L\left(\frac{\partial\phi_n}{\partial T_{n,p}}\right) - \phi_n - T_L\left(\frac{\partial\phi_p}{\partial T_{n,p}}\right) + \phi_p\right] \\ & - T_L\left[\left(\frac{\partial\phi_n}{\partial T}\right)_{n,p} + P_n\right] divJ_n - T_L\left[\left(\frac{\partial\phi_p}{\partial T}\right)_{n,p} + P_p\right] divJ_p \end{aligned} \qquad 3\text{–}47$$

In the steady-state case, the current divergence can be replaced with the net recombination then the heat generation term simplifies to:

$$H = \left[\frac{\left|\overrightarrow{J_n}\right|^2}{q\mu_n n} + \frac{\left|\overrightarrow{J_p}\right|^2}{q\mu_p p}\right] + q(R-G)\left[\phi_p - \phi_n + T_L\left(P_p - P_n\right)\right] - T_L\left(\overrightarrow{J_n}\nabla P_n + \overrightarrow{J_p}\nabla P_p\right) \qquad 3\text{–}48$$

where:

$\left[\frac{\left|\overrightarrow{J_n}\right|^2}{q\mu_n n}+\frac{\left|\overrightarrow{J_p}\right|^2}{q\mu_p p}\right]$ is the Joule heating term,

$q(R-G)\left[\phi_p-\phi_n+T_L(P_p-P_n)\right]$ is the recombination and generation heating and cooling term, and $-T_L\left(\overrightarrow{J_n}\nabla P_n+\overrightarrow{J_p}\nabla P_p\right)$ accounts for the Peltier and Joule-Thomson effects.

If the general expression shown in Eq. 3–42 is used for the non-stationary case, the derivatives $\left(\frac{\partial\phi_n}{\partial T_L}\right)_{n,p}$ and $\left(\frac{\partial\phi_p}{\partial T_L}\right)_{n,p}$ are evaluated for the case of an idealized non-degenerate semiconductor and complete ionization. The heat generation term, *H*, is always set equal to 0 in insulators. For conductors $H=\frac{(\nabla \mathrm{V})^2}{\rho}$

At least one thermal boundary condition must be specified when the lattice heat flow equation is solved. The thermal boundary conditions used have the following general form:

$$\sigma\left(\vec{J}^{u}_{tot}\cdot\vec{s}\right)=\alpha(T_L-T_{ext}) \qquad 3\text{–}49$$

where σ is either 0 or 1, $\vec{J}^{u}_{tot}$ is the total energy flux and $\vec{s}$ is the unit external normal of the boundary. The projection of the energy flux onto *s* is:

$$\left(\overrightarrow{J^{u}_{tot}}\cdot\vec{s}\right)=-\kappa\frac{\partial T_L}{\partial n}+(T_L P_n+\phi_n)\vec{J}_n\cdot\vec{s}+(T_L P_p+\phi_p)\left(\vec{J}_p\cdot\vec{s}\right) \qquad 3\text{–}50$$

When $\sigma = 0$, Eq. 3–49 specifies a fixed temperature boundary condition:

$$T_L=T_{ext} \qquad 3\text{–}51$$

When $\sigma = 1$, Eq. 3–49 takes the form:

$$\left(\overrightarrow{J^{u}_{tot}}\cdot\vec{s}\right)=\alpha(T_L-T_{ext}) \qquad 3\text{–}52$$

3.3.2.5. Carrier Mobility Definitions

A composition and temperature dependent low-field model is used and defined as the mobility model for the nitride Wurtzite phase materials system. The model is specified for electrons as the majority carriers. The Farahmand Modified Caughey Thomas (FMCT) model [33] was the result of fitting a Caughey Thomas [67] like model to Monte Carlo data: low field mobility:

$$\mu_0(T,N)=\mu_{\min}\left(\frac{T}{300}\right)^{\beta_1}+\frac{(\mu_{\max}-\mu_{\min})\left(\frac{T}{300}\right)^{\beta_2}}{1+\left[N_{ref}\left(\frac{T}{300}\right)^{\beta_3}\right]^{\alpha(T/300)^{\beta_4}}} \qquad 3\text{–}53$$

Here, *T* is the temperature, N_{ref} is the total doping density, and α, β_1, β_2, β_3, β_4, $\mu_{\min}$ and $\mu_{\max}$ are parameters that are determined from Monte Carlo simulation [33].

A nitride specific field dependent mobility model for high field mobility could be specified using the following dependence (FMCT.N and GANSAT.N):

$$\mu_n(E) = \frac{\mu_0(T,N) + v_n^{sat}\dfrac{E^{n_1-1}}{E_c^{n_1}}}{1 + a\left(\dfrac{E}{E_c}\right)^{n_2} + \left(\dfrac{E}{E_c}\right)^{n_1}} \qquad 3\text{–}54$$

where $\mu_0(T, N)$ is the low field mobility as expressed in Eq. 3–53. The parameters in the model (v_n^{sat} , E_c, a, n_1 and n_2) are determined from Monte Carlo simulation.

Another alternative is to use the parallel electric field-dependent mobility (FMCT.N and FLDMOB). As carriers are accelerated in an electric field, velocity starts to saturate as the electric field magnitude reaches a significantly higher value. This effect has to be accounted for by a reduction of the effective mobility since the magnitude of the drift velocity is the product of the mobility and the electric field component in the direction of the current flow. The following Caughey and Thomas expression [67] is used to implement field-dependent mobility. This provides a smooth transition between low-field and high field behavior where:

$$\mu_n(E) = \mu_0(N,T)\left[\frac{1}{1 + \left(\dfrac{\mu_0(N,T)E}{v_n^{sat}}\right)^{\beta_n}}\right]^{1/\beta_n} \qquad 3\text{–}55$$

Here, E is the parallel electric field and $\mu_0(N,T)$ is the low-field electron mobility. The low-field mobility is calculated by the low-field mobility model (FMCT). The saturation velocity is calculated from the temperature-dependent models [68]:

$$v_n^{sat} = \frac{\alpha_n^E}{\theta_n^E \exp\left(\dfrac{T_L}{T_n^E}\right)} \qquad 3\text{–}56$$

The Canali model [69] has been implemented as an alternative to using fixed values of β_n in the Caughey-Thomes model. This uses the exponent β, which depends on lattice temperature (T_L), and will calculate the value of β_n as:

$$\beta_n = \beta_n^0 (T_L/300)^{\beta_n^1} \qquad 3\text{–}57$$

3.3.2.6. Schottky Gate Reverse Bias Tunneling Leakage Current Modeling

It has been found that the reverse *I-V* characteristics of some Gallium Nitride (GaN) diodes can best be explained by using a phonon-assisted electron tunneling model [55]. The electrons are assumed to be emitted from local levels in the metal-semiconductor interface and give a contribution to the current of:

$$J = eN_sW \qquad 3\text{–}58$$

where e is the electronic charge, N_s is the occupied state density near the interface, and W is the rate of phonon-assisted tunneling of electrons from localized states into the conduction band. The rate of phonon-assisted tunneling W, as function of temperature T and field strength E is:

$$W = \frac{eE}{\left(8m^{*}\varepsilon_T\right)}\left[\left(1+\gamma^2\right)^{1/2}-\gamma\right]^{1/2}\left[1+\gamma^2\right]^{-1/4} \times \exp\left\{-\frac{4}{3}\frac{\left(2m^{*}\right)^{1/2}}{eE\hbar}\varepsilon_T^{3/2}\left[\left(1+\gamma^2\right)^{1/2}-\gamma\right]^2 \times\left[\left(1+\gamma^2\right)^{1/2}-\frac{1}{2}\gamma\right]\right\} \quad 3\text{–}59$$

where

$$\gamma = \frac{\left(2m^{*}\right)^{1/2}\Gamma^2}{8e\hbar E\varepsilon_T^{1/2}} \quad 3\text{–}60$$

$$\Gamma^2 = \Gamma_0^2\left(2n+1\right) = 8a\left(\hbar\omega\right)^2\left(2n+1\right) \quad 3\text{–}61$$

$$n = \left[\exp\left(\frac{\hbar\omega}{k_B T}\right)-1\right]^{-1} \quad 3\text{–}62$$

where $\hbar\omega$ is the phonon energy, ε_T is the trap depth, m^{*} is the effective mass of electron and a is the electron-phonon interaction constant.

3.3.2.7. Electrons as the Majority Carriers (Single Carrier Solutions)

Frequently for MOSFETs simulation, it is recommended to simulate only the majority carrier. This will significantly speed up simulations where minority carrier effects can be neglected. This can be done by turning off the minority carrier in the continuity equations. In the case of GaN-based HEMTs it is possible to use electrons only as charge carriers due to their dominance in the device characteristics.

3.4. Empirical Matching to Measured Devices

In Silvaco-"ATLAS" there are build-in models and nitride-based semiconductors physical parameters are in many cases based on Monte Carlo simulations and fit to physical properties measurements and not based on experimental device electrical measurements. Therefore in many cases the initial results of the simulation are by far to fit and describe a GaN based HEMTs measured electrical performance. Here some adjustments of the physical models parameters described above are needed. In addition Silvaco "ATLAS" does not specifically define the models and methods required to simulate a device such as GaN based HEMT but gives general guidelines and multiple freedom of choice to the user. The task of tuning the simulation to match the experimental measurements results requires turning large number of the simulation "knobs" and require from the user large number of time consuming iterations of trial-and-error to reach his goals. In the following section a summarized description of the empirical adjustments made in the simulation to fit a FBH GaN technology standard monitoring transistors is given. Figure 3.4–1 shows the output (I_{DS}-V_{DS}), transfer (I_{DS}-V_{GS}) and transconductance (g_m) characteristics of the initial simulation with the simulation default parameters and models compared to median wafer-level measurements. The nonconformity of the fit is obvious in all electrical and physical levels.

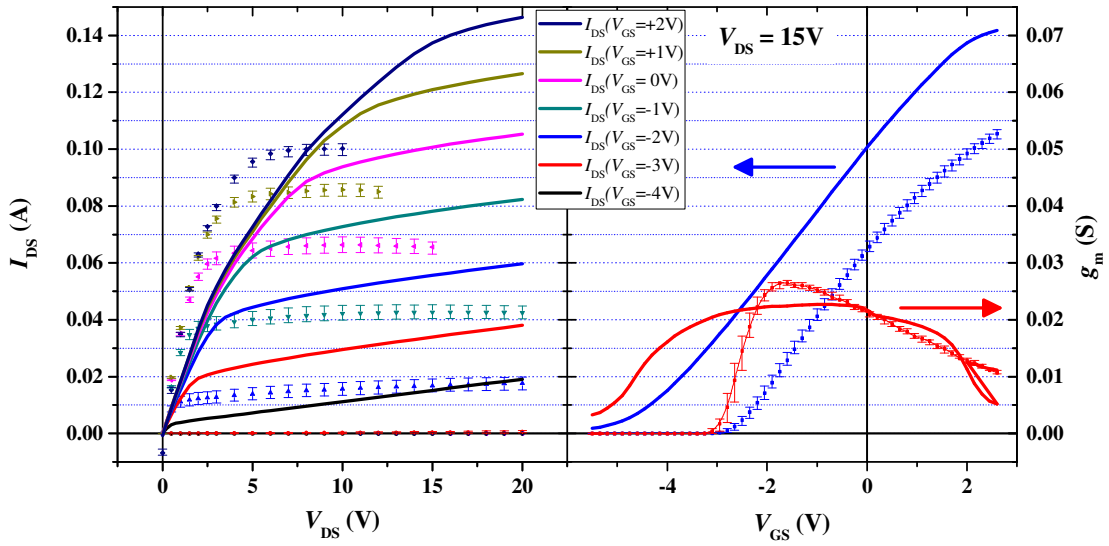


Figure 3.4–1 A GaN based HEMT *I-V* curves and transfer characteristics simulation vs. experimental results.

3.4.1. Simulation Models and Parameter Modifications for an Empirical Matching

The following models which were chosen and modified were considered in the simulation script: The basic Silvaco-"ATLAS" script that was used for the matching to the experimental results is shown in appendix A.

- A high field mobility was chosen (Eq. 3–55 FLDMOB) instead of the nitride specific field dependent mobility model (Eq. 3–54 GANSAT.N) for high field to fit better the experimental results. In addition to the low-field mobility model was incorporated (Eq. 3–53 FMCT.N) unfortunately the model could not predict the low R_{on} or the profile of the *I-V* curves or the transfer characteristics of GaN HEMTs and therefore the parameters of the FMCT model had to be modified for the GaN material. To improve the mobility temperature dependency the Canali model (Eq. 3–57 CANALI.N) with modified parameters was added as a correction to the mobility in the GaN material.
- Even though Silvaco "ATLAS" recommends **not** to use the polarization statements for GaN-based FET devices but to use fixed interface charges, the polarization model (as described in section 3.3.2.2) was successfully used with the corrections. The corrections included the scalar polarization magnitude of the AlGaN barrier and set the right reference electron affinity to the 4H-SiC substrate. The polarization scaling parameter adjusts the device maximum drain current and the gate threshold voltage. The simulation contains three polarization parameters sets [61], [62] and [65]. The parameters polarization set from [62] fits the best to the experimental measurements results.
- The simulation contains four parameters sets for $k \cdot p$ model taken from [61], [62], [64] and [70]. The $k \cdot p$ parameters set from [62] fits the best to the experimental measurements results.
- Since there is no default value for the Schottky gate work-function in Silvaco "ATLAS" the value was set and calibrated to fit the best sub-threshold drain current and threshold voltage.
- Geometrical considerations mesh vs. time and accuracy ultra fine mesh for gate leakage model (see Figure 3.4–6).
- Silvaco "ATLAS" neither recognize nor define the formation of ohmic contacts from geometrical point of view, i.e. depositing an ohmic metal on the AlGaN, therefore a

quasi-ohmic contact must be defined by using high *n*-type quasi-doping concentration with adequate meshing.

- Acceptor traps were added to fit the slope of the sub-threshold current characteristics of the GaN buffer.

As a result of the incorporation of the selected models and the empirical adjustments of the models' parameters the simulated results fit much better to the experimental electrical measurements. Figure 3.4–2 shows a cross-section of a calculated band structure of a GaN based HEMT. The generation of the Two-Dimensional-Electron-Gas (2DEG) and the electron concentration profile result from the simulation calculation could be seen.

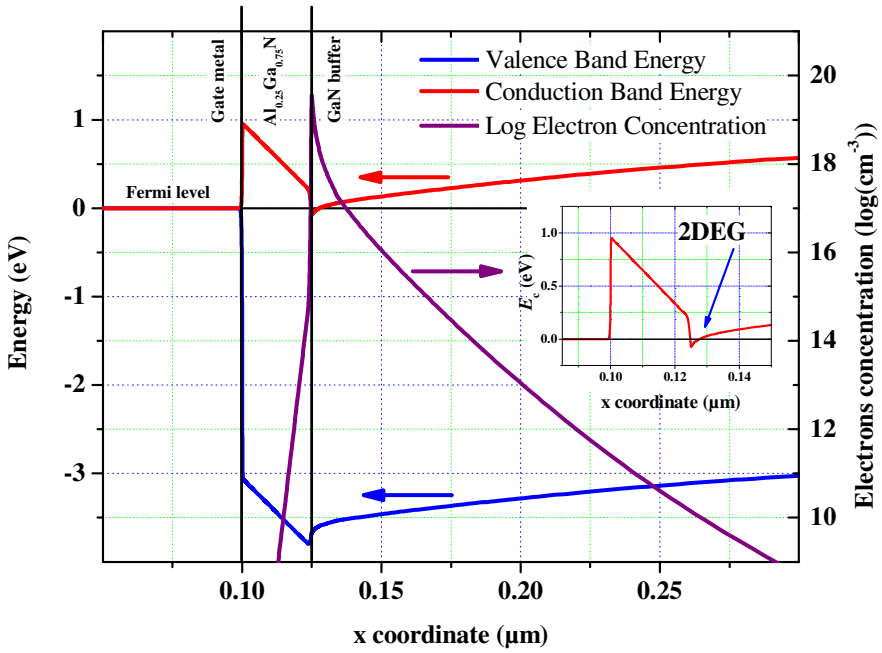


Figure 3.4–2 GaN based HEMT calculated band structure and calculated electrons concentration. Inset shows the potential pit and 2DEG location at the GaN/AlGaN interface.

The new resulting calculations of the electrical characteristics, which take into consideration the modifications in the models and models parameters as described above, compared to the experimental results (shown in Figure 3.4–3). It could be seen that very good correlation to the experimental measurements is obtained in the output I_{DS}-V_{DS}, the transfer (I_{DS}-V_{GS}) and the transconductance (g_m) characteristics. Example of the two dimensional physical and the electrical properties cross section is presented in Figure 3.4–4, logarithmic scale electron concentration distribution, and Figure 3.4–5, distribution of the magnitude of electric field. The figures compare the simulation results in ON-state and OFF-state conditions, default models and parameters and the modified models and parameters. Significant differences could be seen for all cases and properties. These differences would become critical when analyzing the device and when using it as a design tool.

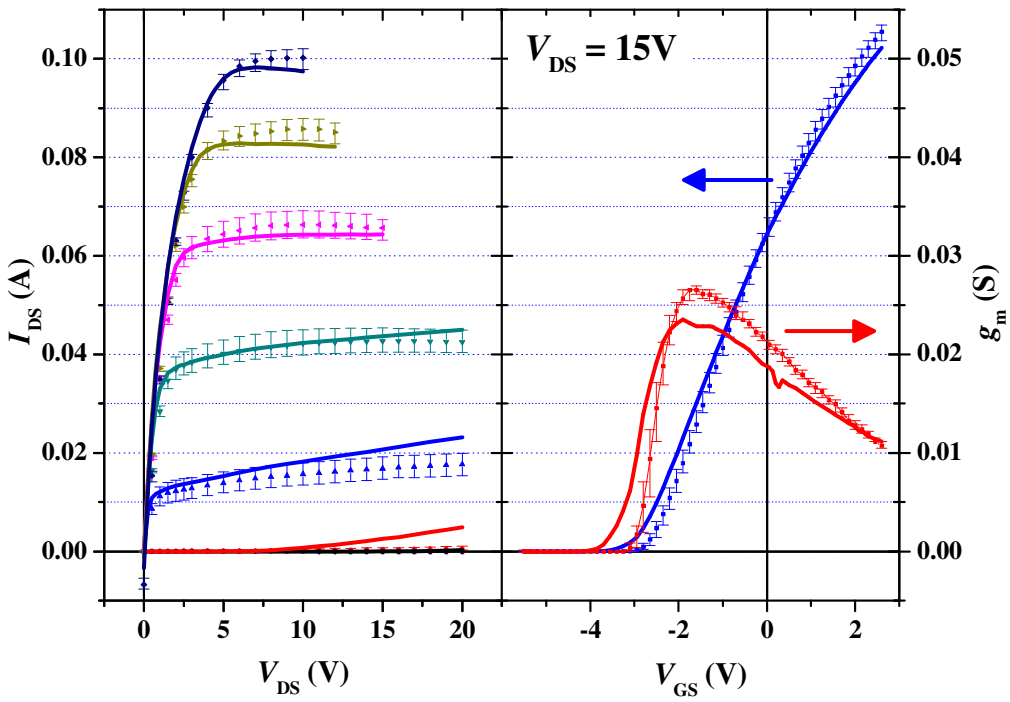


Figure 3.4–3 A GaN based HEMT *I-V* curves ($V_{GS\,max}$ = +2 V and ΔV_{GS} = 1 V), transfer characteristics and transconductance simulated calculations vs. experimental results.

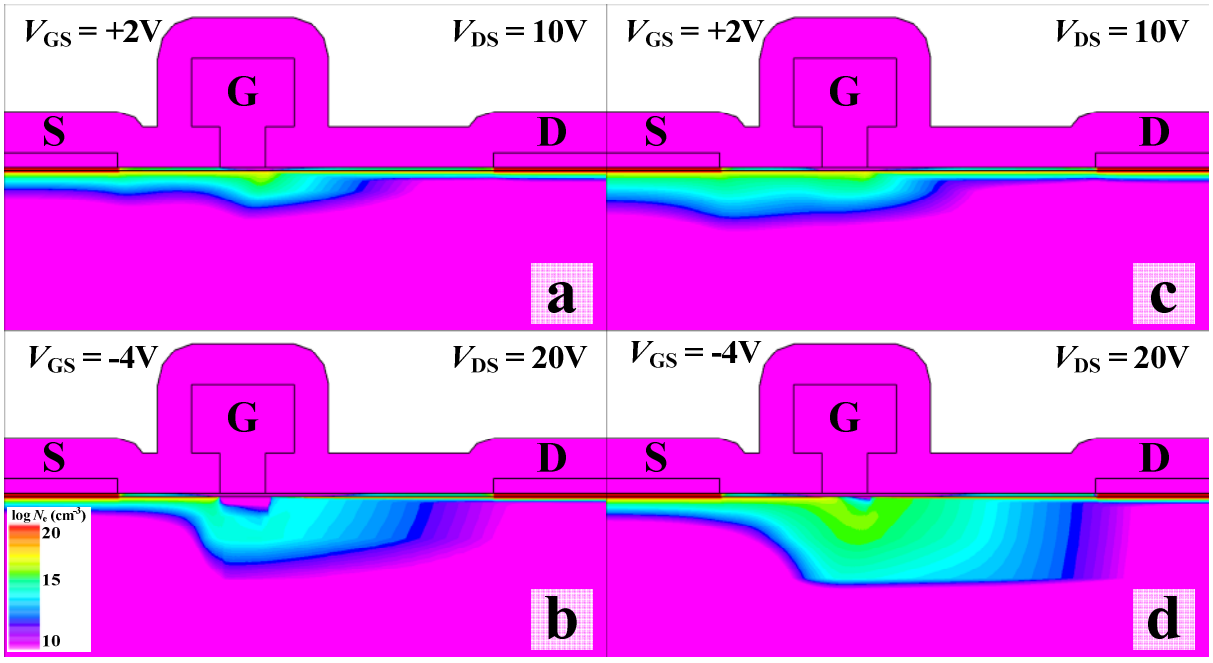


Figure 3.4–4 Electron concentration distribution cross section in a simulated GaN-based HEMT structure results (a) and (b) from modified simulation models (c) and (d) from default simulation models. (a) and (c) are ON-state conditions V_{GS} = +2 V, V_{DS} = 10 V and (b) and (d) are OFF-state conditions V_{GS} = -4 V, V_{DS} = 20 V.

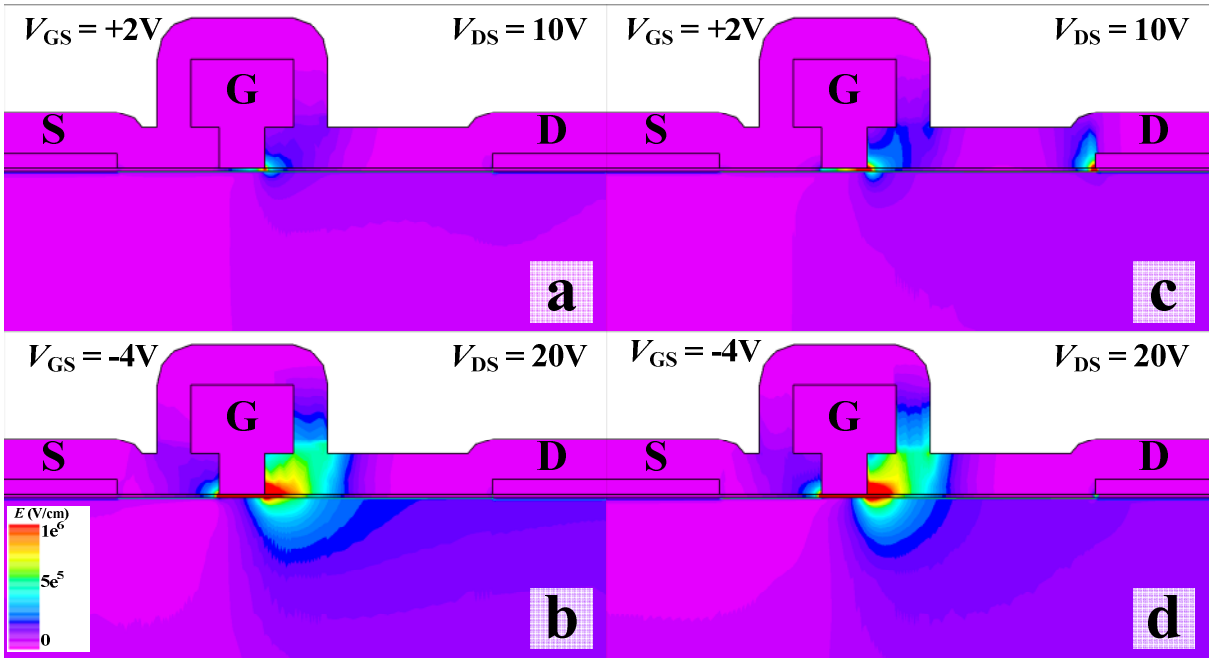


Figure 3.4–5 Electric field distribution cross section in a simulated GaN-based HEMT structure results (a) and (b) from modified simulation models (c) and (d) from default simulation models. (a) and (c) are ON-state conditions V_{GS} = +2 V, V_{DS} = 10 V and (b) and (d) are OFF-state conditions V_{GS} = -4 V, V_{DS} = 20 V.

Recently Silvaco "ATLAS" incorporated in the simulation GaN specific Schottky contact reverse bias leakage current mechanism explained by using a phonon-assisted electron tunneling model developed by Pipinys *et al.* [55] described in section 3.3.2.6. The electrical field dependent leakage mechanism requires an ultra fine, sub-nanometer, high resolution mesh.

Figure 3.4–6(a) show the mesh under the Schottky gate that was used in the simulated structure. The simulation default parameters were used except the density of charge states for the diode that is taken from the original paper $N_s = 1.2 \times 10^{13}$ cm^{-2}. For the empirical matching the control parameter of the effective mass of electrons was modified from 0.222 m_e to ~0.050 m_e to achieve the correct level of reverse bias leakage current of the Schottky gate diode. In addition the Canali model [69] was added to improve the fit of the temperature dependent mobility properties.

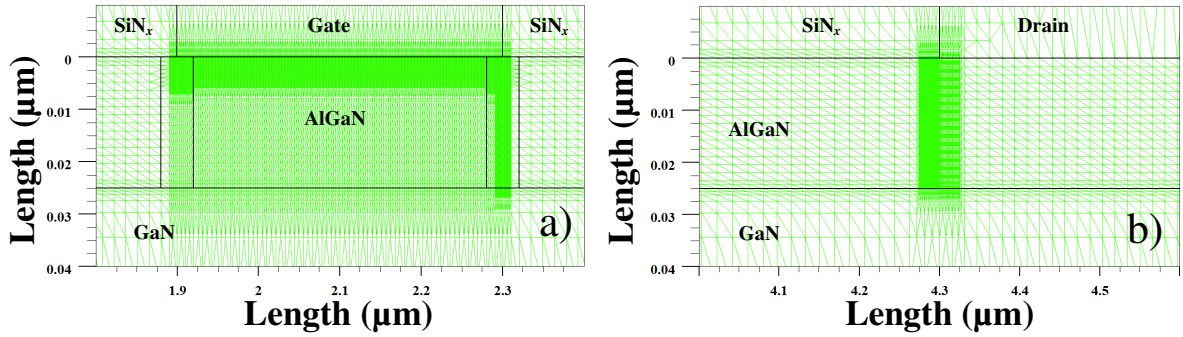


Figure 3.4–6 Ultra fine, sub-nanometer, high resolution mesh requirements for high electric field simulations (a) under the gate (b) under the drain.

Excellent fit of the simulation calculated *I-V* curves, transfer characteristics and the transconductance to the median measurements of a typical device is shown in Figure 3.4–7 and Figure 3.4–8. Accurate fit could be seen not only in the current level values but in the ON-state and in the OFF-state regimes. In the ON-state an accurate resistance is calculated and

in the OFF-state the accurate sub-threshold gate and drain leakage currents are calculated. The ability to predict the sub-threshold leakage currents is the key to analyze and design GaN-based devices operating in high voltages OFF-state conditions.

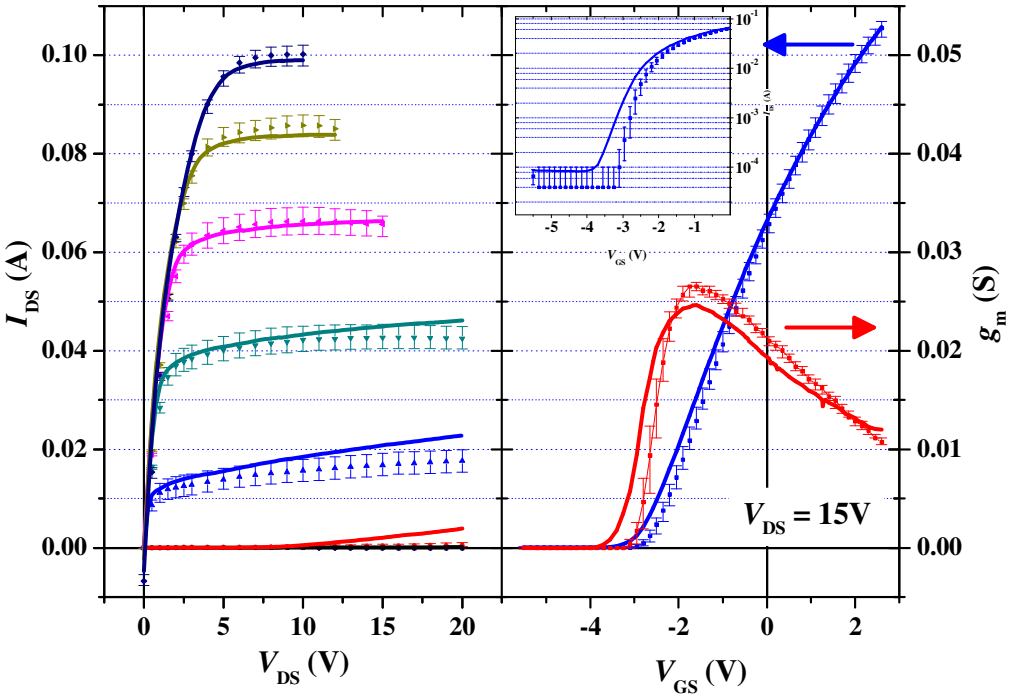


Figure 3.4–7 A GaN based HEMT *I-V* curves ($V_{GS\,max}$ = +2 V and ΔV_{GS} = 1 V), transfer characteristics and transconductance simulated calculations vs. experimental results (including the Pipinys [55] and the Canali [69] models). Inset: log scale of the sub-threshold regime.

Figure 3.4–8 demonstrates the influence of the introduction of a Schottky reverse bias tunneling leakage model [55]. Previous models neglected this very important and dominating leakage mechanism and the prediction of the reverse bias gate current was far-off the device performance. As the model introduced a very accurate prediction of the leakage current is calculated with the exception of the opening of the Schottky diode in forward bias, shifted in about +1 V, that still need calibration of the Schottky barrier and the metal work function.

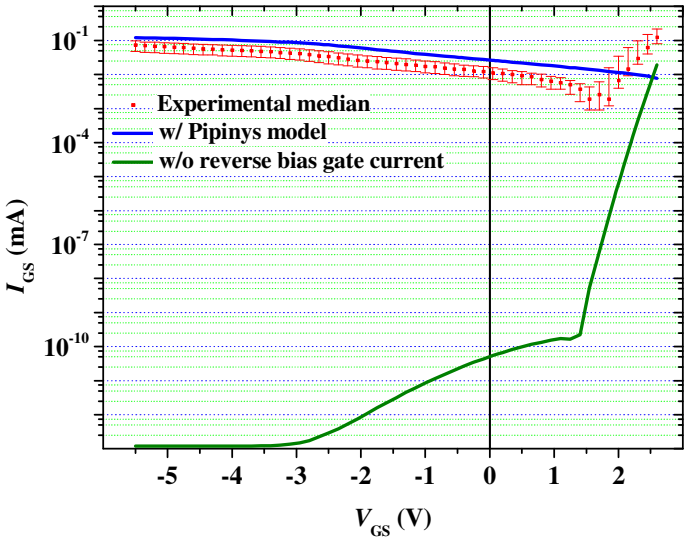


Figure 3.4–8 A GaN based HEMT gate current, I_{GS}, transfer characteristics simulated calculations vs. experimental results (including the Pipinys [55] and the Canali [69] models).

3.5. Conclusions

A systematic matching of GaN-based HEMTs experimental DC measurements to physically based Silvaco-"ATLAS" simulation program was developed. Suitable physical models were chosen for best representation of the GaN-based semiconductor material system. Empirical modifications of the models' parameters were essential for accurate match to experimental device measurements. Simulated device structure fine mashing definitions were one of the important parameters for accurate simulation, therefore attracted intensive attention during the matching process. Special attention was given to the accuracy of the simulation in subthreshold conditions for the analysis of the device leakage currents which are the limiting factor of the OFF-state blocking voltage capability. The GaN-based device simulation is now a useful tool for design and physical insight-analysis that is require for development of such devices.

Examples for device geometry design, epitaxial layers design and analysis of dynamic physical properties of GaN-based HEMTs during its operation using the physical based simulation is given through out this work and detailed in each of the chapters. Addition examples for GaN-based simulation and an engineering design and analysis tool made parallel to this work could be found elsewhere [71], [72], [73], [74], [75], [76], [77], [78].

Chapter 4

Systematic Study of AlGaN/GaN/AlGaN DH-HEMTs

An enhancement of breakdown voltage in $Al_xGa_{1-x}N$/GaN high electron mobility transistor devices by increasing the electron confinement in the transistor channel using a low Al content $Al_yGa_{1-y}N$ back-barrier layer structure is presented. It is shown that the reduced sub-threshold drain-leakage current through the buffer layer postpones the punch-through and therefore shifts the breakdown of the device to higher voltages. It is also shown that the punch-through voltage (V_{PT}) scales up with the device dimensions (gate to drain separation) and further improves for recess type device structures. An optimized electron confinement results both, in a scaling of breakdown voltage with device geometry and a significantly reduced sub-threshold drain and gate leakage currents. These beneficial properties are pronounced even further if gate recess technology is applied for device fabrication. For systematic study a large variations of back-barrier epitaxial structures were grown on sapphire, *n*-type 4H-SiC and semi-insulating 4H-SiC substrates. To investigate the impact of $Al_yGa_{1-y}N$ back-barrier on the device properties the devices were characterized in DC along with microwave mode and robustness DC-step-stress test. Physical-based device simulations give insight in the respective electronic mechanisms and to the punch-through process that leads to device breakdown [79], [80], [81], [82], [83].

4.1. Introduction to $Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N$ DH-HEMTs

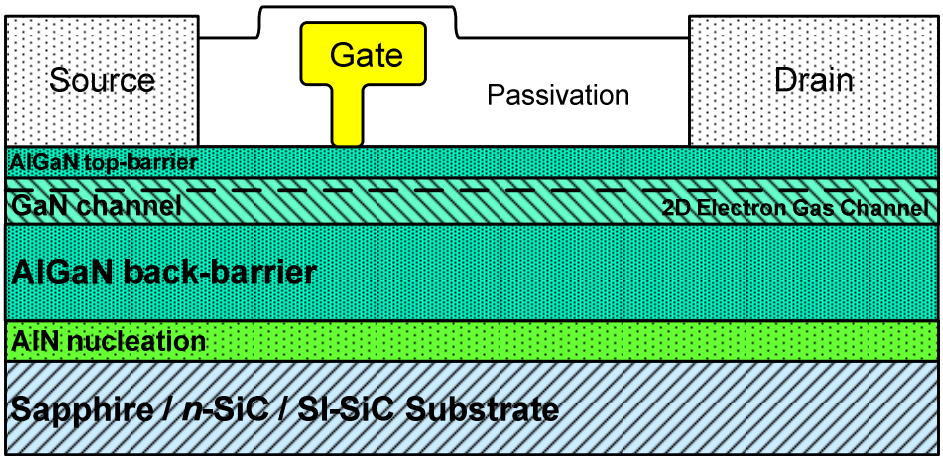


Figure 4.1–1 A planar gate GaN based DH-HEMT structure.

GaN-based High Electron Mobility Transistors (HEMTs) are considered to be excellent candidates for high-power switching applications such as highly efficient power switches in switched power-supplies or AC motor-drive systems, due to their high sheet-carrier density in the two dimensional electron gas (2DEG) channel and large breakdown field-strength (~ 3.5 MV/cm) [41], [42], [43]. The power-switch performance is limited by the conduction losses in the ON-state and by the OFF-state breakdown voltage ($V_{BR\ OFF}$). Enhancing $V_{BR\ OFF}$ while keeping the gate-drain distance short is therefore one of the most important challenges in current developments of GaN-based HEMT power switches. This paper shows that a good carrier confinement to the channel will increase $V_{BR\ OFF}$. Carrier confinement and insulating buffer layers have already shown good impact on the AC power performance of GaN based HEMTs [84], [85], [86]. Buffer layer leakage currents are much more significant than surface leakages in high-voltage operation [87]. Breakdown in GaN-based HEMTs and other field effect devices is, in many cases, initiated by electron current underneath the depletion region of the transistor gate through the insulating buffer layer and known as space charge inject of electrons into the GaN buffer layer [48], carrier spill-over [49] or buffer layer punch-through effect [50], [51]. The punch-through of the electrons into the buffer causes rapid increase of the sub-threshold drain leakage current and it is often interpreted as the device breakdown-voltage. In many cases it is only the initiator for a breakdown processes such as avalanche-breakdown. In standard epitaxial designs for GaN HEMTs electrons are well confined to the upper side of the channel by the AlGaN barrier layer. However in standard HEMTs with a GaN buffer layer there is an insufficient confinement to the bottom side which may give rise to punch-through effects even at low drain voltages and closed channel conditions. The punch-through effect may be prevented, by introducing a *p*-type doping to the GaN buffer layer [51], [85], by increasing the amount of acceptor type traps in the GaN buffer layer [50] or, as in our case, by using a heterostructure for confining the electrons in the channel layer. In the so called double heterojunction (DH)-HEMT, shown in Figure 4.1–1, the channel is separated from the buffer layer by a second heterojunction giving AlGaN/GaN/AlGaN and/or AlGaN/InGaN/AlGaN structures [49], [84], [88]. In addition, DH-HEMTs also show high mobility and high maximum electron concentration. However, the 2DEG sheet density is somewhat lower [89], [90].

Here we present an improved bottom confinement by introducing an AlGaN buffer layer with low Al content to the structure. A GaN interlayer between the AlGaN buffer and the barrier serves as channel for the 2DEG, i.e., we consider the system as an

$Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N$ DH-HEMT.

Figure 4.1–2 depicts the spontaneous polarization, (P_{SP}), piezoelectric polarization, (P_{PE}), bound interface charges, (σ), 2DEG, conduction and valance band edges scheme in $Al_yGa_{1-y}N/GaN/Al_xGa_{1-x}N$ DH-HEMT heterostructures with Ga-face polarity. The thick $Al_yGa_{1-y}N$ buffer is assumed to be free of strain and both the GaN channel and the $Al_xGa_{1-x}N$ top-barrier are grown pseudomorphicaly on the $Al_yGa_{1-y}N$ therefore the lattice constant, a, of the grown layers assume to be $a_{Al_xGa_{1-x}N} = a_{GaN\,Channel} = a_{Al_yGa_{1-y}N}$ [26].

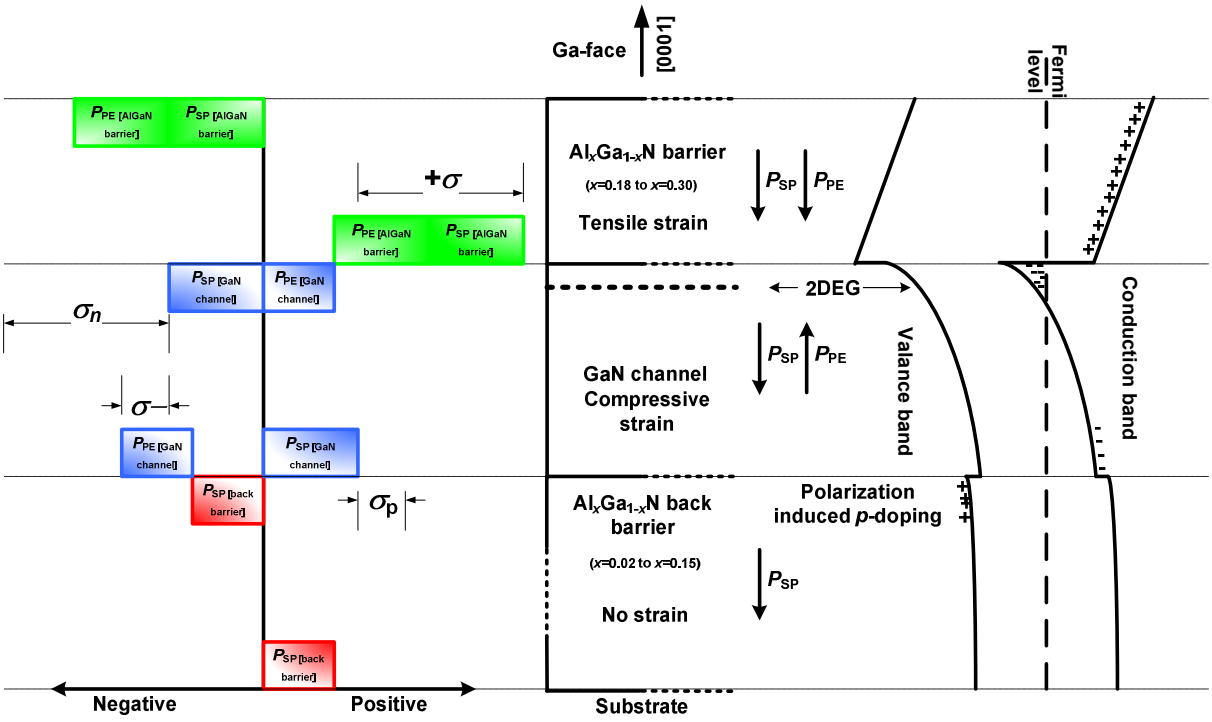


Figure 4.1–2 Spontaneous polarization, piezoelectric polarization, bound interface charges, 2DEG, conduction and valance band edges scheme in $Al_yGa_{1-y}N$ /GaN/ $Al_xGa_{1-x}N$ DH-HEMT heterostructures with Ga-face polarity.

The total polarization in the free of strain thick $Al_yGa_{1-y}N$ buffer is only the spontaneous polarization and the piezoelectric polarization equal to zero. On the other hand the GaN channel's lattice constant is now smaller due to the biaxial compressive stress which becomes larger with the increase of the Al mole fraction in the AlGaN back barrier film and therefore exhibit spontaneous polarization and piezoelectric polarization with opposite vector directions $[000\bar{1}]$ and $[0001]$ respectively. The $Al_xGa_{1-x}N$ top-barrier with the higher Al mole fraction has now a lattice constant which is larger than it is in strain free conditions due to the biaxial tensile strain and therefore exhibit spontaneous polarization and piezoelectric polarization with the same vector direction $[000\bar{1}]$. Charge densities at the $Al_yGa_{1-y}N/GaN$ interface $\sigma_{Al_yGa_{1-y}N/GaN}$ and the $GaN/Al_xGa_{1-x}N$ interface $\sigma_{GaN/Al_xGa_{1-x}N}$, are caused by the different polarization of the $Al_yGa_{1-y}N$ the GaN and the $Al_xGa_{1-x}N$. A negative difference in the $Al_yGa_{1-y}N/GaN$ interface generates an excess positive charge in the top of the $Al_yGa_{1-y}N$. This charge generates the back potential barrier or a polarization induces p-type doping. The positive difference in the GaN/ $Al_xGa_{1-x}N$ interface generates an excess negative charge in the top of the GaN channel. This charge generates the 2DEG.

The polarization generates a strong electric field inside the GaN layer:

$$E_{GaN} = -\frac{P_{SP(GaN)} + P_{PE(GaN)}}{\varepsilon_{Al_yGa_{1-y}N}\varepsilon_0} \qquad 4\text{–}1$$

Where $\varepsilon_{Al_yGa_{1-y}N}$ and ε_0 are the dielectric constants of the $Al_yGa_{1-y}N$ and vacuum. The band edges are strongly modified by the electric field in the GaN and shifts positive strongly the bands.

4.2. Simulation Insight into $Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N$ DH-HEMTs

Two dimensional physical-based device simulations (Silvaco - "ATLAS") [59] were done to get an insight to the punch-through effect in conventional AlGaN/GaN HEMTs and $Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N$ DH-HEMTs. The simulation followed the measurement sequence of the sub-threshold drain-leakage current and the punch-through voltage and the logarithmic electron concentration, n_e, was logged. Figure 4.2–1(a) compares the calculated conduction band energy of a DH-HEMT structure consisting of a $Al_{0.1}Ga_{0.9}N$ buffer layer and conventional GaN HEMT with GaN buffer layer in neutral bias conditions. Figure 4.2–1(b) shows the dramatic reduction, more than 10 orders of magnitude, of the electron concentration n_e in the $Al_{0.1}Ga_{0.9}N$ buffer layer, that prevents current flowing through it. The simulation shows consistence with the experimental finding. The reduction of the $I_{DS\ max}$ and the increase of the V_{Th} indicate a reduction in the sheet electron concentration in the 2DEG channel. This is due to the deeper and much narrower conduction band well that forms the transistor channel see Figure 4.2–1(a) [88] [89]. An electron distribution analysis was preformed at closed-gate conditions with V_{GS} = -6 V << V_{Th} in dependence on the drain bias until the punch-through was identified. As in experiment the simulation shows a reduction of the sub-threshold drain-leakage current and an increase of the punch-through voltage in the DH-HEMTs. This is due to the raised conduction band of the AlGaN (Figure 4.2–1(a)). The electron channel becomes a deep potential well that enables a good 2DEG confinement. Figure 4.2–2 shows cross-sections of the electron concentration distribution at V_{DS} = 30 V for devices with GaN buffer layer (a) and DH-HEMTs with AlGaN buffer layer that contains 0.05 (b) and 0.10 (c) mole fraction of Al. For the conventional GaN buffer layer the channel volume under the gate is totally depleted by the gate induced field. But the electrons bypass this field and travel through the buffer layer to the lower potential regions. In DH-HEMTs the energy barrier towards the buffer layer, created by the AlGaN/GaN heterojunction prevents the majority of the carriers from spilling over into the buffer layer. This reduces the sub-threshold drain-leakage current and postpones the punch-through of the buffer layer.

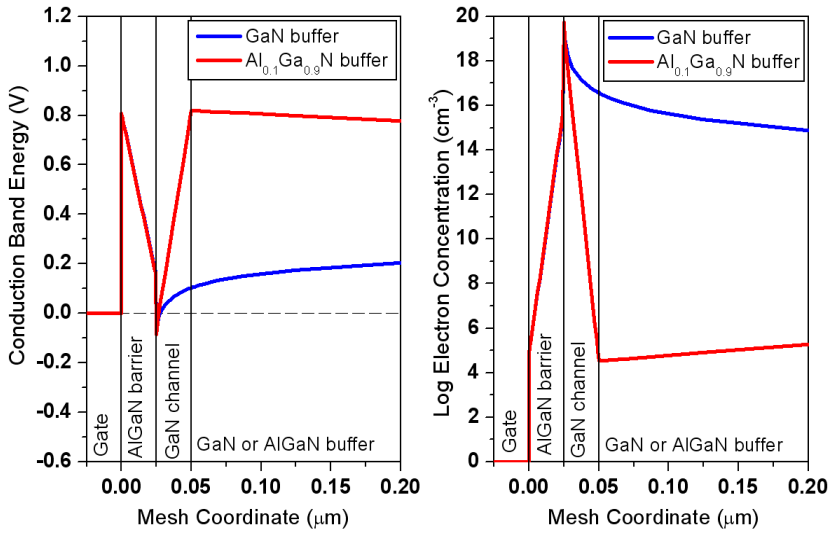


Figure 4.2–1 GaN based DH-HEMT device cross section with GaN buffer layer and $Al_{0.1}Ga_{0.9}N$ buffer layer (a) calculated conduction band energy. (b) calculated electron concentration, n_e.

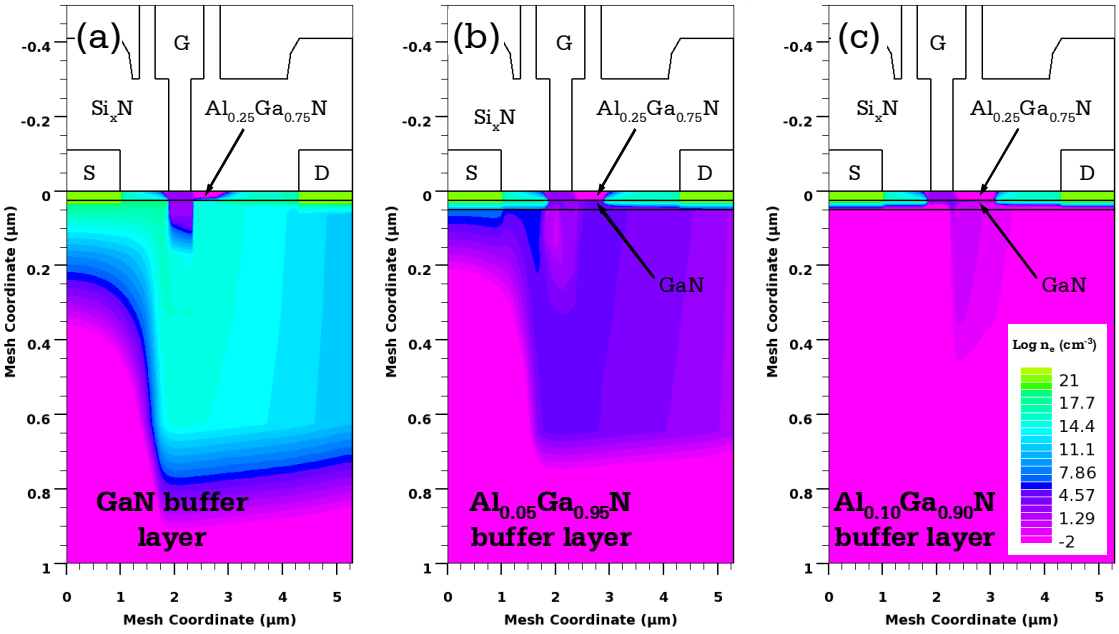


Figure 4.2–2 Electrons concentration, n_e, distribution in HEMT device (a) with GaN buffer layer (b) with $Al_{0.05}Ga_{0.95}N$ buffer layer (c) with $Al_{0.1}Ga_{0.9}N$ buffer layer, at V_{GS} = -6 V and V_{DS} = 30 V. n_e varies between 10^{-2} cm^{-3} and 10^{21} cm^{-3}.

Although it is shown that the introduction of AlGaN back-barrier increases the conduction band energy, reduces the electron concentration in the device buffer and postpones the device punch-through, it is desired to increase this barrier as much as possible to optimize the device OFF-state blocking capability. The UID GaN channel thickness, d_{Ch}, in the DH-HEMTs is one of the parameters that are relatively controllable and have a strong impact on the band structure. Modifying the UID GaN channel thickness, d_{Ch}, allows maintaining low Al mole fraction in the back-barrier while increasing the height of energy back-barrier.

Figure 4.2–3(a) compares the dependence of the calculated study-state energy bands structure in conventional GaN HEMT and in DH-HEMTs with different UID GaN channel thicknesses, d_{Ch}, while keeping the Al mole fraction $y = 0.05$ in the back-barrier constant. Figure 4.2–3(b) shows the resulting calculated electron concentration of the same structures. It shows that the conduction band level is steeply increased with the increase of the GaN

channel thickness with increase rate of ~0.031 eV/nm up to the saturation value of $E_{g\,AlGaN}$ above the Fermi-level. Farther increase of the GaN channel thickness results in reduction of the slope. An optimized GaN channel thickness could be assessed from the default model calculations as $d_{Ch,}$ ~225 nm, ~110 nm and ~60 nm for DH-HEMT with $Al_yGa_{1-y}N$ back-barrier were the Al mole fraction is 0.02, 0.05 and 0.10 respectively.

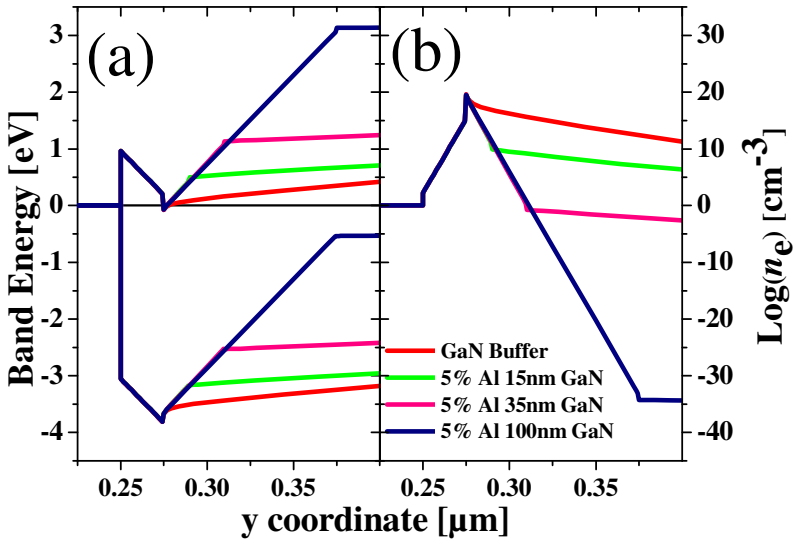


Figure 4.2–3 Cross section of calculated (a) conduction and valance band energy and (b) electrons concentration n_e in a DH-HEMT with $Al_{0.05}Ga_{0.95}N$ devices with GaN channel layer thickness, d_{Ch}, 15 nm, 35 nm and 100 nm compared with conventional GaN HEMT.

Recently the "Self-Consistent Coupled Schrödinger Poisson Model" [59] was used to calculate the band energy structure in DH-HEMTs. This model self-consistently solves Poisson's equation (for potential) and Schrodinger's equation (for bound state energies and carrier wave functions). The equation solution gives a quantized description of the density of states in the presence of quantum mechanical confining potential variations.

Figure 4.2–4 compares the dependence of the calculated steady-state energy bands structure in conventional GaN HEMT and in DH-HEMTs with different UID GaN channel thicknesses, d_{Ch}, and different Al mole fraction $y = 0.02$ to 0.10 in the back-barrier. Figure 4.2–5 shows the resulting calculated electron concentration of the same structures.

Here, as in the default energy band model, the conduction band energy barrier and its slope rises with the increase of the Al mole fraction for constant GaN channel thickness. The conduction band level is steeply increased with the increase of the GaN channel thickness up to the saturation value of $E_{g\,AlGaN}$ above the Fermi-level. In this calculation method the saturation is reached in much thinner GaN channel thicknesses. Farther increase of the GaN channel thickness results in reduction of the slope and broadening of the 2DEG channel. An optimized GaN channel thickness could be assessed from the Schrödinger-Poisson model calculations as $d_{Ch,}$ ~45 nm, ~30 nm and ~20 nm for DH-HEMT with $Al_yGa_{1-y}N$ back-barrier were the Al mole fraction is 0.02, 0.05 and 0.10 respectively.

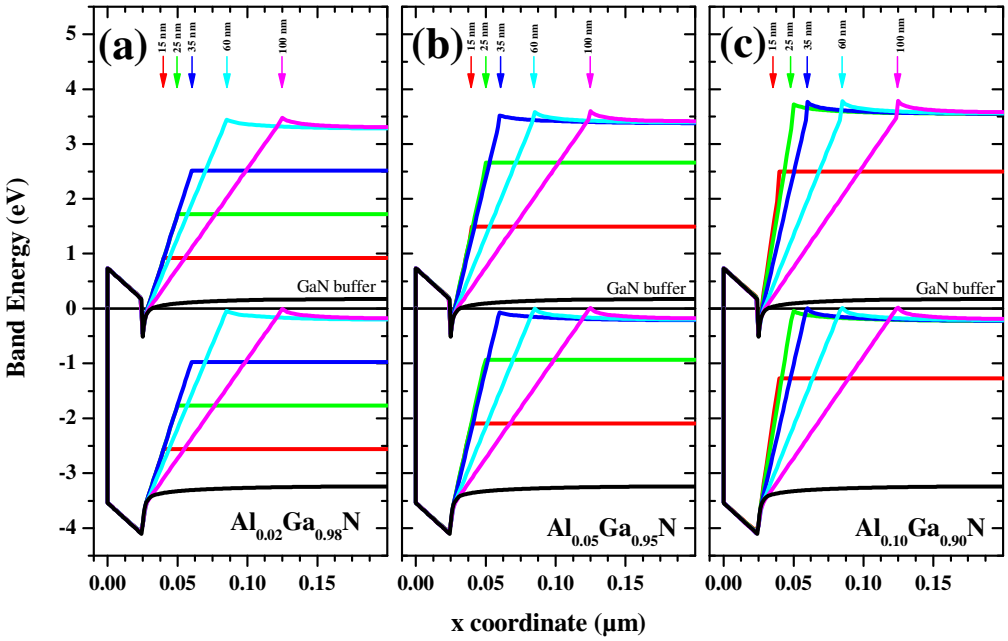


Figure 4.2–4 Cross section from the calculation of the self-consistent coupled Schrödinger Poisson model for conduction and valance bands energy in DH-HEMTs in steady-state conditions. (a) $Al_{0.02}Ga_{0.98}N$ back-barrier, (b) $Al_{0.05}Ga_{0.95}N$ back-barrier (c) $Al_{0.10}Ga_{0.90}N$ back-barrier. The devices owning GaN channel layer with thickness, d_{Ch}, of 15 nm, 25 nm, 35 nm, 60 nm and 100 nm are compared with conventional GaN HEMT.

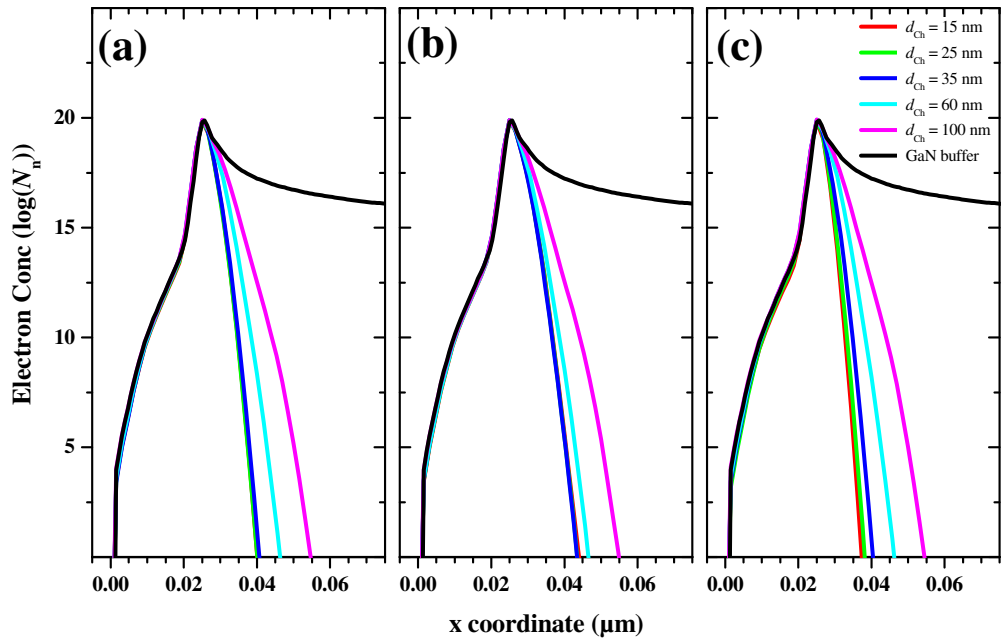


Figure 4.2–5 Cross section from the calculation of the self-consistent coupled Schrödinger Poisson model for electrons concentration n_e in DH-HEMTs in steady-state conditions. (a) $Al_{0.02}Ga_{0.98}N$ back-barrier, (b) $Al_{0.05}Ga_{0.95}N$ back-barrier (c) $Al_{0.10}Ga_{0.90}N$ back-barrier. The devices owning GaN channel layer with thickness, d_{Ch}, of 15 nm, 25 nm, 35 nm, 60 nm and 100 nm are compared with conventional GaN HEMT.

4.3. Fabrication and Measurements of $Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N$ DH-HEMTs

4.3.1. Fabrication and Measurements of DH-HEMTs on Sapphire Substrate

DH-HEMTs were realized in FBH for the first time on 2 inch sapphire substrates and detailed in the following section. For comparison, four types of samples were studied, a conventional AlGaN/GaN HEMT, wafer "A", and three variations of AlGaN double-heterojunction structure, wafers "B"-"D", (see summary in Table 4.3–1). The samples were grown by Metal Organic Vapor Phase Epitaxy (MOVPE) on sapphire substrates. All sample types have the same AlN nucleation layer followed by 1150 nm Unintentionally Doped (UID) GaN. For the GaN buffer structure (wafer "A") a 1.5 µm thick UID GaN was grown. For the AlGaN DH-buffer structure (wafers "B"-"D") a 2.0 to 2.3 µm thick UID linearly graded $Al_yGa_{1-y}N$ layer with Al maximum mole fraction (y) of 0.05, 0.07 and 0.10 at the interface to the GaN channel layer was grown. They are referred to later as DH-HEMTs with AlGaN buffer layer with y Al mole fraction. The grading was done over a thick layer in order to reduce polarization induced doping [91] and to avoid the generation of a secondary channel in the buffer layer. All samples had a 25 nm UID GaN channel layer followed by 25 nm $Al_{0.26}Ga_{0.74}N$ barrier layer.

Layer	Wafer "A"		Wafer "B"		Wafer "C"		Wafer "D"	
	x or y	d (nm)	x or y	d (nm)	x or y	d (nm)	x or y	d (nm)
Barrier $Al_xGa_{1-x}N$	0.26	25	0.26	25	0.26	25	0.26	25
Channel GAN	-	25	-	25	-	25	-	25
Buffer layer $Al_xGa_{1-x}N$	-	1500	0→0.05	~2000	0→0.07	~2300	0→0.10	~2200
Buffer GaN	-	1150	-	1150	-	1150	-	1150
Nucleation AlN	-	~250	-	~250	-	~250	-	~250
"d" refers to layer thickness and "x" and "y" refer to Al mole fraction.								

Table 4.3–1 Epitaxy Structure of compared wafers.

Field-effect transistors were fabricated on all wafer types. Ohmic contacts ware made by evaporating Ti/Al/Mo/Au and annealing at 830°C. Mesa insulation was formed using Cl_2/BCl_3 reactive ion etching. The AlGaN barrier was passivated with SiN_x. A mask defined by electron beam lithography and dry etching created the gate opening in the passivation. Pt/Ti/Au contacts were then evaporated for the gate Schottky metal, followed by a metal liftoff. The surface was again passivated with a second SiN_x layer. A second set of wafers of the same four types was gate recessed. In this case the AlGaN barrier layer is dry etched using a longer etching time in the gate definition process. The recess depth was ~10 nm, leaving an AlGaN layer of 15 nm under the gate. The fabricated devices were 2 × 125 µm wide with a gate length of 0.5 µm. The gate-drain spacing L_{GD} was varied from 1 µm to 10 µm for device scaling tests.

DC transfer characteristics for the DH-HEMTs with L_{GD} = 2 µm are shown for planar gate devices in Figure 4.3–1(a) and for 10 nm gate recess in Figure 4.3–1(b). For the GaN buffer layer and planar gate, the maximum drain current, $I_{DS\,max}$, measured at V_{GS} = +3 V was 750 mA/mm and the threshold voltage V_{Th} = -3.8 V. By increasing the Al concentration x in the buffer layer to y = 0.05, 0.07 and 0.10 the maximum drain current was reduced to 557 mA/mm, 537 mA/mm and 495 mA/mm, respectively and the threshold voltage (V_{Th}) was shifted towards the positive gate bias to V_{Th} = -2.8 V, -2.7 V and -2.2 V, respectively. For the

gate-recess DH-HEMTs for the same buffer layer Al mole fraction of $y = 0.05$, 0.07 and 0.10 $I_{DS\,max}$ = 633 mA/mm, 470 mA/mm, 432 mA/mm and 421 mA/mm, respectively. V_{Th} was shifted to V_{Th} = -1.8 V, -0.9 V, -0.8 V and -0.6 V, respectively. Figure 4.3–2(a) and Figure 4.3–2(b) compare the wafer level median *I-V* characteristics of conventional GaN based HEMT, wafer "A" with DH-HEMT wafer "D" respectively. The reduction of the $I_{DS\,max}$ and the increase of the V_{Th} for planar and recessed gate cases indicates a reduction in the sheet electron concentration in the 2DEG channel. These experimental results are in agreement with previous works [88], [89], [90] and are explained by the abrupt increase of the band gap energy at the interface between the GaN channel and the AlGaN buffer layer and of the negative polarization, confining the carriers in a smaller volume. For recessed devices a reduced positive spontaneous polarization charge at the 2DEG position results in an additional reduction of $I_{DS\,max}$ [24], [63].

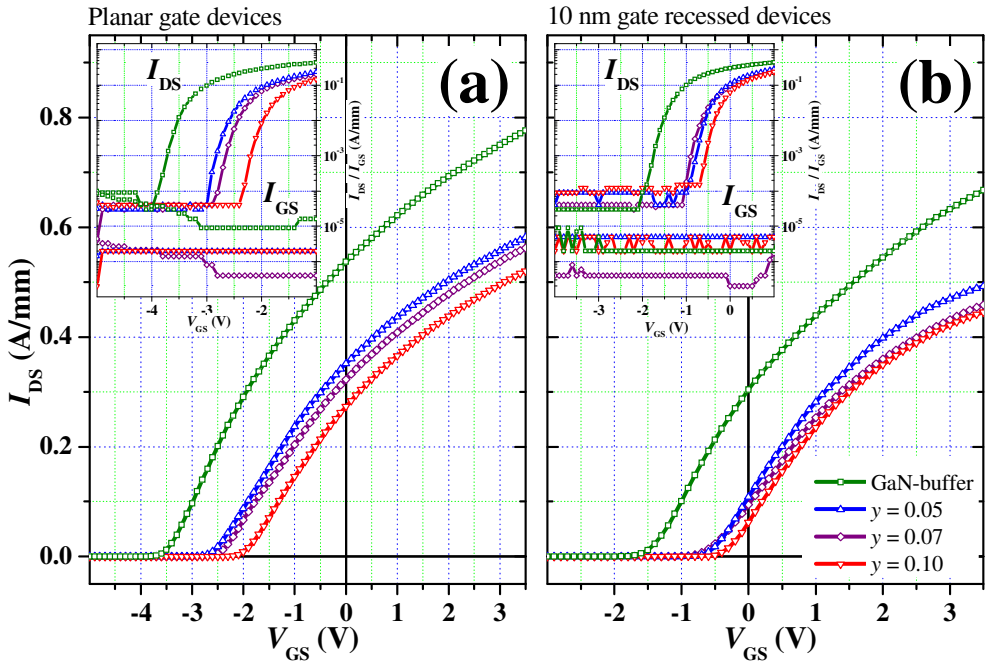


Figure 4.3–1 Wafer level median transfer characteristics of GaN HEMT cells with different Al mole fraction, y, in the $Al_yGa_{1-y}N$ buffer layer (a) for planar gate devices and (b) for 10 nm gate-recessed devices. Measured at V_{DS} = 15 V.

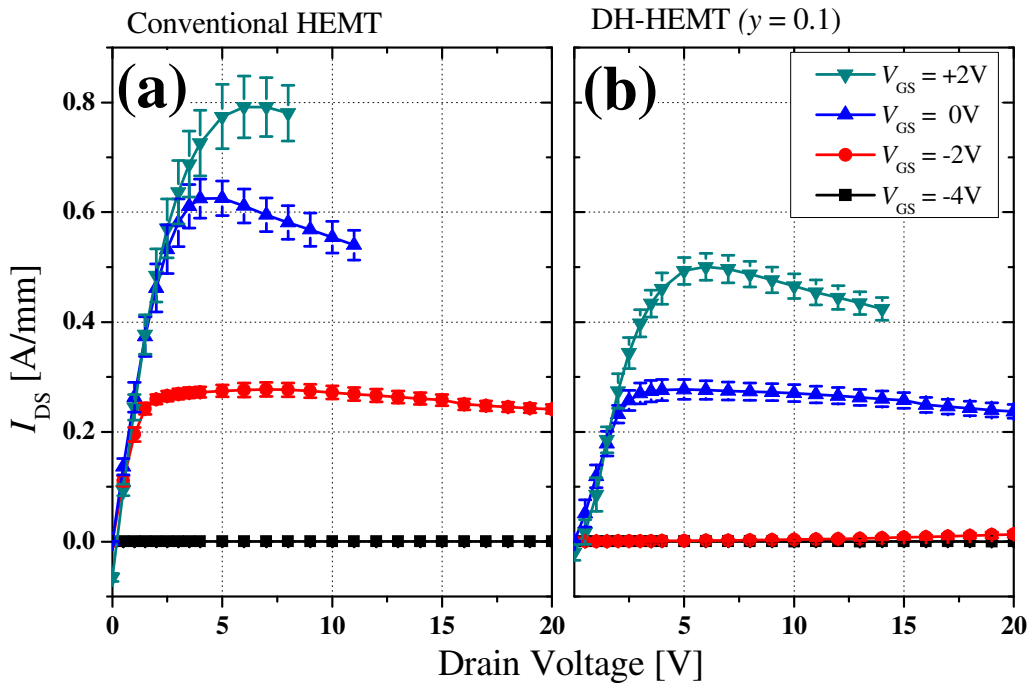


Figure 4.3–2 Wafer level median *I-V* characteristics of 2×50 µm planar gate devices with $L_{GD} = 2$ µm (a) GaN buffer, (b) $Al_{0.1}Ga_{0.9}N$ back-barrier. (Error bars are 25% and 75% percentiles).

The difference in confinement for the GaN-buffer layer and the AlGaN-buffer layer devices is demonstrated by the shift of V_{Th} with increasing drain voltage (V_{DS}). Figure 4.3–3 shows that V_{Th} gets shifted towards a more negative gate bias when V_{DS} is increased. This shift is much more pronounced for the GaN-buffer layer devices than it is for the AlGaN-buffer layer devices. For the GaN buffer layer, electrons can drift deeper into the buffer layer to bypass the gate depletion region at sufficiently high V_{DS}. The gate depletion region has therefore to be further extended to close the channel. On the other hand the electrons are hindered to move into the buffer layer for the DH-HEMTs. Then, V_{Th} is less sensitive to V_{DS}.

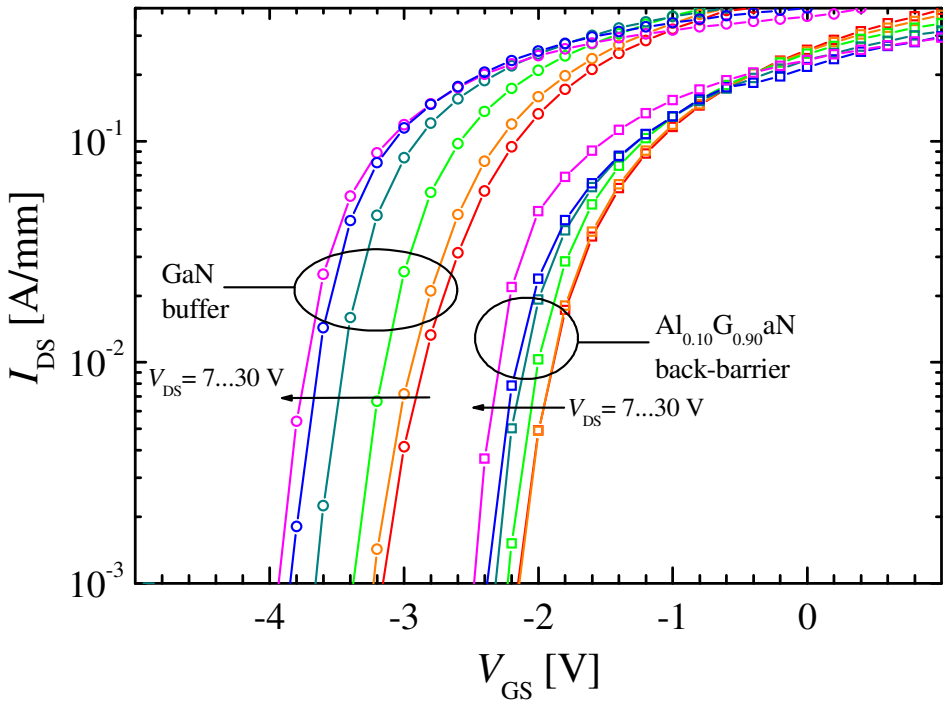


Figure 4.3–3 Transfer characteristics for devices with GaN buffer layer and with AlGaN buffer layer ($y = 0.1$). The drain voltage was varied with 7 V, 10 V, 15 V, 20 V, 25 V and 30 V. The resulting shift in V_{Th} is 0.9 V for the GaN buffer layer and 0.4 V for the AlGaN buffer layer.

The punch-through voltage V_{PT} of the devices was measured at closed gate conditions below a threshold bias $V_{Th} >> V_{GS} = -6$ V. The drain bias was increased and logged until punch-through was identified. The punch through voltage was defined as the voltage at which the drain current exceeds the value of 5 mA/mm or as the voltage at which the value of the drain current exceeds 20 % of the value of the preceding drain current measurement at V_{DS}-1 V, depending on which criterion is fulfilled first. Figure 4.3–4 shows examples of sub-threshold drain-leakage current measurements for conventional HEMTs with GaN buffer layer and DH-HEMTs with AlGaN buffer layer with Al content of $y = 0.10$, both with gate-recess. The results show a large reduction in the sub-threshold drain leakage current for the DH-HEMTs and a dramatic improvement in the device punch-through characteristic from an average of 50 V, for conventional HEMTs, to an average of 180 V with a maximum of 230 V for DH-HEMTs.

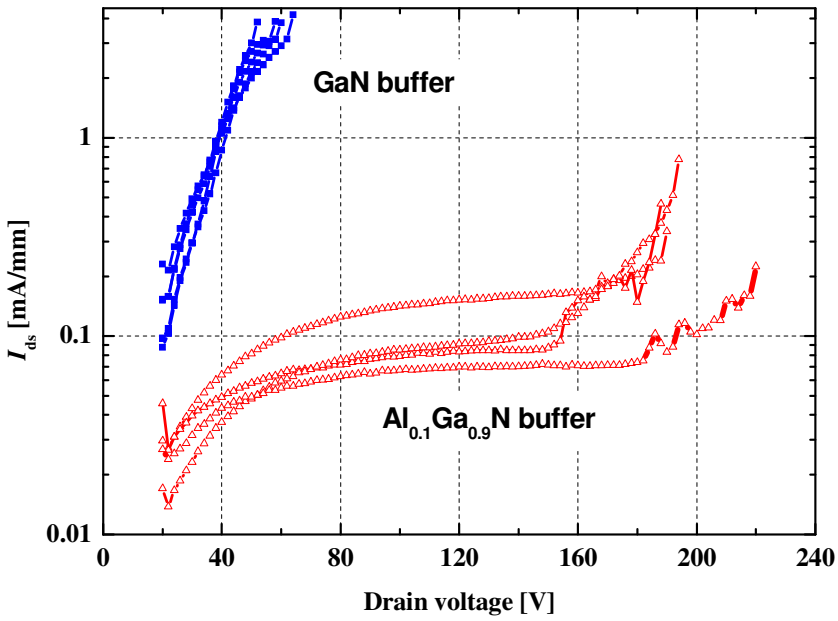


Figure 4.3–4 Drain current output during V_{PT} measurements for HEMT devices with GaN buffer and $Al_{0.1}Ga_{0.9}N$ buffer layer for 10 nm gate-recessed devices (L_{GD} = 5 µm).

High subthreshold drain leakage currents and low punch-through voltage characteristics in GaN buffer layer HEMTs are often observed and are related to the epitaxial properties of the GaN buffer layer. In high quality GaN buffer layers thicker than 2 µm, as in this experiment, the trap density formed by threading dislocations is reduced. Therefore, the electron mobility in the buffer is higher, leading to an overall higher electrical conductivity. Thus, a higher leakage current flows through the buffer resulting in punch-through and later a device breakdown [92]. Nitrogen vacancies and screw dislocations are also contributors to the buffer conductivity [93], [94]. The scaling of the punch-through voltage with increasing gate-drain distance from L_{GD} = 1 µm to 10 µm has shown dramatic improvement for the DH-HEMTs devices in comparison to GaN buffer layer devices. The tested GaN buffer layer devices practically show no scaling. This issue will be discussed later.

The average punch-through voltages for different gate-drain distances are shown in Figure 4.3–5(a) for planar gate devices and in Figure 4.3–5(b) for gate-recess devices. In both cases, V_{PT} (or $V_{BR\ OFF}$) is low and independent on the gate-drain distance for the GaN-buffer layer HEMTS. In contrast, the DH-HEMTs show a scale-up up to a limit of L_{GD} = 6 µm. For the gate-recess DH-HEMTs, the slope of the scaling as well as the maximum V_{PT} (or $V_{BR\ OFF}$) clearly increases with the Al concentration in the buffer layer. The planar-gate DH-HEMTs show both effects in tendency but the maximum V_{PT}'s are lower and there is even a slight reduction for y = 0.10.

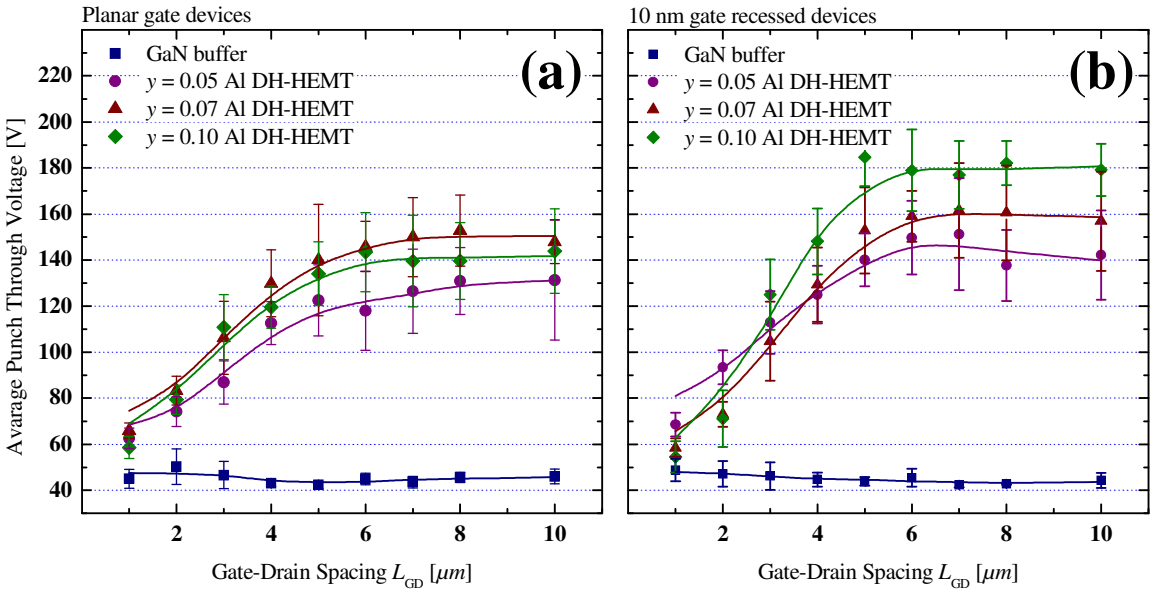


Figure 4.3–5 Average V_{PT} measurement for different Al mole fraction y and for different gate drain distances (L_{GD}) (a) for planar gate devices and (b) for 10 nm gate-recessed devices.

4.3.2. Fabrication and Measurements of DH-HEMTs on 4H-SiC Substrate

In this section, a systematic study of $Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N$ double-heterojunction high-electron-mobility-transistor (These wafers are referred to later as DH-HEMTs) devices and the dependent different epitaxial structures and properties such as the GaN channel layer thickness (d_{Ch}), the Al mole fraction in the back-barrier (y), the Al mole fraction in the top-barrier (x), and the substrates are examined. The samples were grown by Metal Organic Vapor Phase Epitaxy (MOVPE) on SiC substrates which have better thermal conductivity and better lattice mismatch than sapphire substrates. High resistive semi-insulating 4H-SiC (SI-SiC) substrates versus low-cost *n*-type 4H-SiC (*n*-SiC) substrates are compared. A device breakdown voltage enhancement was achieved by increasing the electron confinement in the transistor channel using an $Al_yGa_{1-y}N$ back-barrier-layer structure. An optimized electron confinement results in a scaling of breakdown voltage with device geometry, low ON-state resistance and a significantly reduced sub-threshold drain and gate leakage currents [82].

The comprehensive study includes eighteen 3 inch wafers, fifteen *n*-SiC wafers and three SI-SiC wafers. The wafers in the study can be divided into four experimental wafer-sets in which different epitaxial parameter and structures resulting in variation of the electrical properties of the examined devices.

Wafer-set-I examines the influence of the thickness of the UID GaN channel while the Al mole fraction in the back-barrier is held in $y = 0.05$ grown on *n*-SiC substrate (see Table 4.3–2). As a reference, wafer with conventional GaN buffer structure (wafer "A") with a 2.4 µm thick unintentionally doped (UID) GaN was grown. For this set of AlGaN DH back-barrier structures (wafers "B" – "F") a 1.60 µm to 1.84 µm thick UID AlGaN layer with Al mole fraction of $y = 0.05$ was grown. All sample types have AlN nucleation layer [95]. Here it is desired to keep the Al mole fraction as low as possible due to higher heat conductivity [96], higher $I_{DS\,max}$, and lower R_{ON}. The DH-HEMTs samples had a 15 nm to 110 nm UID GaN channel layer followed by 25 nm to 30 nm UID $Al_xGa_{1-x}N$ barrier layer with for Al mole fraction (x) between 0.23 to 0.25. The vertical substrate breakdown voltage, $V_{BR\,Sub}$, across the epitaxial layers and the substrates, has been between 840 V and 920 V.

Wafers-set-II compares DH-HEMTs with thick UID Al-rich $Al_yGa_{1-y}N$ back-barrier layer,

wafers "G" – "K" with reference wafer "A" (see Table 4.3–3). The AlN nucleation layer followed by a growth of 1.60 µm to 1.84 µm thick UID AlGaN layer with for Al mole fraction of y = 0.08 - 0.10. Here it is desired to keep the for Al mole fraction as high as possible due to the superior confinement properties of the lower heterojunction. The DH-HEMTs samples had a 15 nm to 75 nm UID GaN channel layer followed by 25 nm to 30 nm UID $Al_xGa_{1-x}N$ barrier layer with Al mole fraction between 0.23 to 0.25. The vertical substrate breakdown voltage, $V_{BR\ Sub}$, across the epitaxial layers and the substrates, has been between 860 V and 1060 V.

Wafers-set-III compares DH-HEMTs with thick UID AlGaN back-barrier layer with low Al concentration and different Al mole fraction in the top-barrier, x, Wafers "L" – "N" (see Table 4.3–4), were wafer "L" with 1.74 µm conventional UID GaN buffer is the wafers-set's reference. The AlN nucleation layer followed by a growth of 1.60 µm thick UID AlGaN layer with Al mole fraction of ~0.02 was grown. The DH-HEMTs samples had a 200 nm UID GaN channel layer followed by 27 nm UID $Al_xGa_{1-x}N$ barrier layer with Al mole fraction between 0.25 and 0.28.

Wafers-set-IV compares DH-HEMTs with thick UID AlGaN back-barrier layer grown on SI-SiC substrates, wafers "S" – "V", to DH-HEMTs with thick UID AlGaN layer grown on n-SiC, wafers "A", "Q" and "R" (see Table 4.3–5). As a reference structures wafers "A" and "V" with AlN nucleation layer followed by 2.4 µm and 1.65 µm UID GaN buffer on n-SiC and SI-SiC substrate respectively were grown. A ~1.7 µm thick UID AlGaN layer with Al mole fractions, y, of 0.05 and 0.10 was grown on wafers "Q" and "R" on n-SiC substrate and on wafers "S" and "T" on SI-SiC substrate respectively. The DH-HEMTs samples had a 35 nm UID GaN channel layer followed by 25 nm UID $Al_xGa_{1-x}N$ barrier layer with Al mole fraction of 0.25.

	Wafer "A"		Wafer "B"		Wafer "C"		Wafer "D"		Wafer "E"		Wafer "F"	
FBH wafer number	GNR02-01		GNR02-04		GNR02-05		GNR02-07		GNR02-12		GSL01-02	
Layer	x / y	d (nm)	x / y	d (nm)	x / y	d (nm)	x / y	d (nm)	x / y	d (nm)	x / y	d (nm)
Barrier $Al_xGa_{1-x}N$	0.23	30	0.23	30	0.23	30	0.25	27	0.25	27	0.24	0.25
Channel GaN	-	-	-	35	-	15	-	110	-	90	-	60
Buffer layer $Al_yGa_{1-y}N$	-	-	0.05	1840	0.05	1840	0.05	1600	0.05	1600	0.05	1670
Buffer GaN	-	2400	-	-	-	-	-	-	-	-	-	-
Nucleation AlN	-	~360	-	~360	-	~360	-	~360	-	~300	-	~100
Substrate	3" n-SiC		3" n-SiC		3" n-SiC		3" n-SiC		3" n-SiC		3" n-SiC	
Substrate V_{BR} (with epitaxy layers)	920 V		870 V		915 V		920 V		840 V		N/A	
"d" refers to layer thickness and "x" and "y" refer to Al mole fraction.												

Table 4.3–2 Epitaxy Structure of compared wafers-set-I.

	Wafer "A"		Wafer "G"		Wafer "H"		Wafer "J"		Wafer "K"	
FBH wafer number	GNR02-01		GNR02-03		GNR02-02		GSL01-03		GNR02-08	
Layer	*x* / *y*	*d* (nm)	*x* / *y*	*d* (nm)	*x* / *y*	*d* (nm)	*x* / *y*	*d* (nm)	*x* / *y*	*d* (nm)
Barrier $Al_xGa_{1-x}N$	0.23	30	0.23	30	0.23	30	0.24	25	0.25	27
Channel GaN	-	-	-	35	-	15	-	60	-	75
Buffer layer $Al_yGa_{1-y}N$	-	-	0.10	1840	0.10	1840	0.10	1670	0.08	1600
Buffer GaN	-	2400	-	-	-	-	-	-	-	-
Nucleation AlN	-	~360	-	~360	-	~360	-	~100	-	~300
Substrate	3" *n*-SiC		3" *n*-SiC		3" *n*-SiC		3" *n*-SiC		3" *n*-SiC	
Substrate V_{BR} (with epitaxy layers)	920 V		860 V		940 V		N/A		1060 V	
"*d*" refers to layer thickness and "*x*" and "*y*" refer to Al mole fraction.										

Table 4.3–3 Epitaxy Structure of compared wafers-set-II.

	Wafer "L"		Wafer "M"		Wafer "N"	
FBH wafer number	GNR02-10		GNR02-11		GNR02-13	
Layer	*x* / *y*	*d* (nm)	*x* / *y*	*d* (nm)	*x* / *y*	*d* (nm)
Barrier $Al_xGa_{1-x}N$	0.24	27	0.25	27	0.28	27
Channel GaN	-	-	-	200	-	200
Buffer layer $Al_yGa_{1-y}N$	-	-	~0.02	1600	~0.02	1600
Buffer GaN	-	1740	-	-	-	-
Nucleation AlN	-	~300	-	~300	-	~300
Substrate	3" *n*-SiC		3" *n*-SiC		3" *n*-SiC	
Substrate V_{BR} (with epitaxy layers)	N/A		N/A		N/A	
"*d*" refers to layer thickness and "*x*" and "*y*" refer to Al mole fraction.						

Table 4.3–4 Epitaxy Structure of compared wafers-set-III.

	Wafer "A"		Wafer "Q"		Wafer "R"		Wafer "S"		Wafer "T"		Wafer "V"	
FBH wafer number	GNR02-01		GSL01-01		GSL01-04		GSL01-06		GSL01-05		GSL01-07	
Layer	*x* / *y*	*d* (nm)	*x* / *y*	*d* (nm)	*x* / *y*	*d* (nm)	*x* / *y*	*d* (nm)	*x* / *y*	*d* (nm)	*x* / *y*	*d* (nm)
Barrier $Al_xGa_{1-x}N$	0.23	30	0.24	25	0.23	25	0.25	25	0.25	25	0.25	25
Channel GaN	-	-	-	35	-	35	-	35	-	35	-	-
Buffer layer $Al_yGa_{1-y}N$	-	-	0.05	1670	0.10	1670	0.05	~1700	0.10	~1700	-	-
Buffer GaN	-	2400	-	-	-	-	-	-	-	-	-	1650
Nucleation AlN	-	~360	-	~100	-	~100	-	~100	-	~100		~50
Substrate	3" *n*-SiC		3" *n*-SiC		3" *n*-SiC		3" SI-SiC		3" SI-SiC		3" SI-SiC	
Substrate V_{BR} (with epitaxy layers)	920 V		N/A		N/A		N/A		N/A		N/A	
"*d*" refers to layer thickness and "*x*" and "*y*" refer to Al mole fraction.												

Table 4.3–5 Epitaxy Structure of compared wafers-set-IV.

Field-effect transistors were fabricated on all wafer types. Ti/Al/Mo/Au based ohmic contacts were formed by e-beam evaporation and annealed at 830°C. Inter-device insulation was made using $^{14}N^+$ multi-energy implantation. The AlGaN barrier was passivated with 150 nm SiN_x. A gate trench in the passivation was defined by i-line optical lithography and subsequently opened by dry etching. Ir/Ti/Au contacts were then evaporated for the gate Schottky metal, followed by a metal liftoff.

The fabricated devices were 2 × 125 µm and 2 × 50 µm wide (W_G) with a gate length of 0.7 µm and asymmetrical Γ-gate head of 1.5 µm with 0.2 µm extension towards the source and 0.6 µm extension towards the drain. The source-gate spacing L_{GS} was kept at 1 µm. Wide

range of devices with gate-drain spacing L_{GD} varied from 1 µm to 18 µm were tested to evaluate the device ability to scale up the OFF-state breakdown voltage with its gate to drain separation.

4.3.2.1. DC Measurements Results of Wafer-Set-I

DC transfer characteristics for the conventional GaN HEMT and DH-HEMTs of wafer-set-I with L_{GD} = 2 µm, L_G = 0.7µm and W_G = 2 × 50 µm are shown in Figure 4.3–6. The devices' key DC measurements parameters are summarized in Table 4.3–6 .The reduction of the $I_{DS\,max}$ and the increase of the V_{Th} indicates a reduction in the sheet electron concentration in the 2DEG channel. These experimental results are in agreement with the results on sapphire wafers (presented in previous section) and are explained by the abrupt increase of the band gap energy at the interface between the GaN channel and the AlGaN back-barrier layer mainly due to the polarization effect induced by the AlGaN back-barrier layer. Thus electrons in the GaN channel are confined in a smaller volume if the AlGaN back-barrier is present.

Careful examination of the sub-threshold regime, in Figure 4.3–6 inset, reveals more; the sub-threshold drain and gate leakage currents at ~V_{Th}-1.0 V are about 3 orders of magnitude lower in wafers "B" and "C", with the AlGaN back-barrier, compared to wafer "A", GaN buffer. These currents are originated by the reverse bias Schottky contact of the gate [55] and in many cases is the cause of premature OFF-state breakdown of the device. A rapid increase of reverse bias Schottky leakage current is observed with the increase of UID GaN channel thickness.

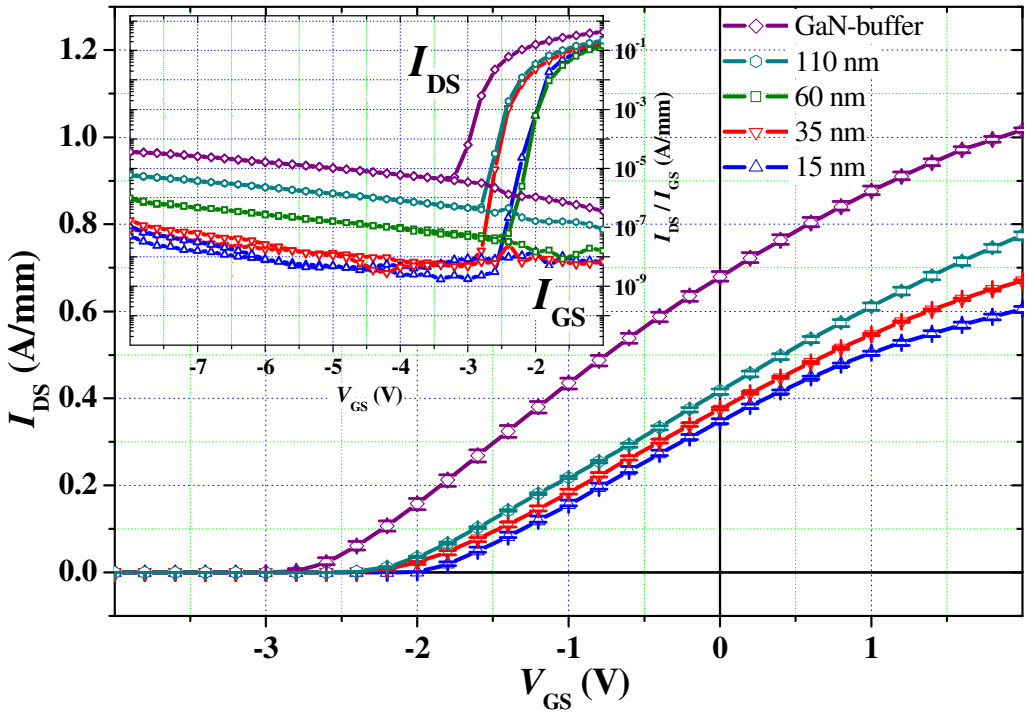


Figure 4.3–6 Wafer median transfer characteristics of conventional GaN HEMT cells and DH-HEMTs with Al mole fraction y = 0.05 and with different GaN channel thicknesses, d_{Ch}. (Error bars represent 25% and 75% quantiles of the measured population with in the wafer). Devices' gate drain spacing is L_{GD} = 2 µm, L_G = 0.7 µm and 2 × 50 µm length measured at V_{DS} = 10 V. Inset: log scale of the sub-threshold regime.

	Wafer "A"	Wafer "B"	Wafer "C"	Wafer "D"	Wafer "E"	Wafer "F"
FBH wafer number	GNR02-01	GNR02-04	GNR02-05	GNR02-07	GNR02-12	GSL01-02
UID GaN channel thickness d_{Ch}	GaN buffer	35 nm	15 nm	110 nm	90 nm	60 nm
V_{Th} (V)	-3.03	-2.37	-2.21	-2.28	-1.01	-1.98
$I_{DS\ max}$ (V_{GS} = +2V) (A/mm)	0.95	0.67	0.61	0.77	0.60	0.69
$V_{BR\ OFF}$ (2 ×50 µm, L_{GD} =2 µm) (V)	37(±5)	127(±3)	110(±7)	62(±5)	50(±18)	95(±6)
R_{ON} (Ω·mm)	2.63	3.22	3.53	2.41	2.44	2.92
$I_{GS\ leak}$ (V_{GS} = V_{Th}-1.0 V) (A/mm)	5.47×10^{-6}	5.35×10^{-9}	7.85×10^{-9}	5.10×10^{-7}	9.05×10^{-8}	4.83×10^{-8}
$I_{DS\ leak}$ (V_{GS} = V_{Th}-1.0 V) (A/mm)	5.59×10^{-6}	6.17×10^{-9}	2.32×10^{-9}	5.16×10^{-7}	1.01×10^{-7}	5.76×10^{-8}
$g_{m\ max}$ (mS/mm)	227	195	187	225	252	219

Table 4.3–6 DC measurements parameters summary of inline monitoring 2 × 50 µm A2 devices, L_{GD} = 2 µm and L_G = 0.7 µm for compared wafer-set-I (y = 0.05).

The dependencies of the ON-state resistance, R_{ON}, on the gate-drain separation, L_{GD}, for wafers with different thickness of the UID GaN channel, d_{Ch}, are presented in Figure 4.3–7. A rapid increase of the ON-state resistance with the narrowing of the GaN channel thickness is observed. For wafers with $d_{Ch} \leq 35$ nm showed larger increase of the R_{ON} for devices with $L_{GD} \geq 10$ µm. This increase could be explained by an increased influence of the carriers' channel narrowing between the gate and drain. The buffer resistivity was measured between two isolated ohmic contact pads at 100 V. Wafer median resistivity was 10.93 $\log_{10}(\Omega/\square)$, 11.17 $\log_{10}(\Omega/\square)$, 8.62 $\log_{10}(\Omega/\square)$, 12.05 $\log_{10}(\Omega/\square)$ and 11.88 $\log_{10}(\Omega/\square)$, for GaN Buffer, GaN channel thickness, d_{Ch}, of 110 nm, 60 nm, 35 nm and 15 nm, respectively. The wafer with 60 nm suffered from severe substrate leakage.

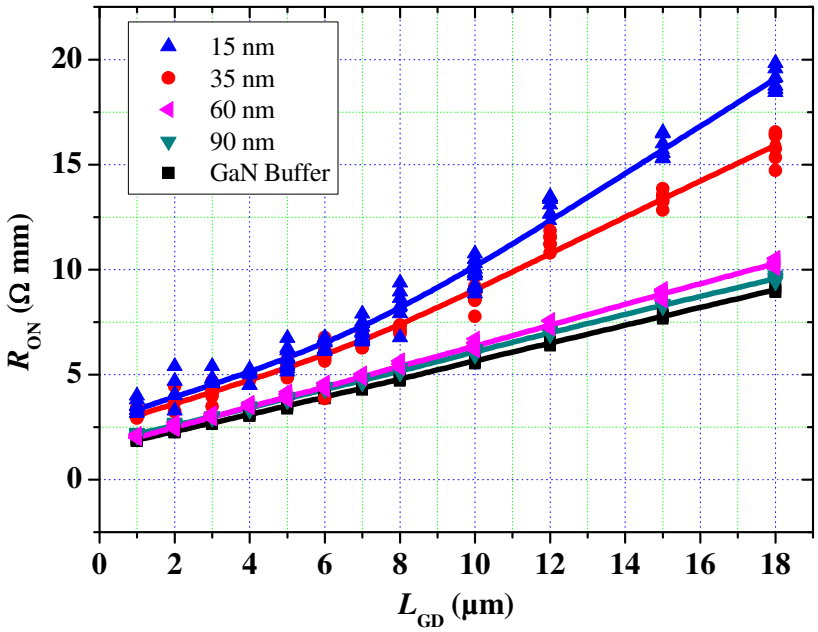


Figure 4.3–7 Wafer-set-I (y = 0.05): the dependence of the ON-state resistance in DH-HEMTs on the UID GaN channel thickness, d_{Ch}, for $W_G = 2 \times 125$ µm devices with, L_G = 0.7 µm and L_{GD} = 1 µm to 18 µm manufactured on n-SiC substrate.

The $V_{BR\ OFF}$ of the devices was measured at closed gate conditions below a threshold bias $V_{Th} >> V_{GS} = V_{Th}$ -2 V in air ambient. The drain bias was increased and logged until punch-through or breakdown was identified. The punch-through or $V_{BR\ OFF}$ were defined as the voltage at which the drain current exceeds the value of 10 mA/mm. Figure 4.3–8(a) shows examples of sub-threshold drain-leakage current measurements for L_{GD} = 7 µm transistors for

conventional HEMTs with GaN buffer layer and DH-HEMTs with different GaN channel thickness layer of d_{Ch} = 15 nm, 35 nm, 90 nm and 110 nm. The results show an orders of magnitude reduction in the sub-threshold drain leakage current for the DH-HEMTs and a dramatic improvement in the device punch-through characteristic from 50 V, for conventional GaN HEMTs, to 366 V for DH-HEMTs with 15 nm GaN channel. The scaling of the $V_{BR\ OFF}$ with increasing L_{GD} from L_{GD} = 1 µm to 10 µm has shown dramatic improvement for the DH-HEMTs devices in comparison to GaN buffer layer devices. The tested GaN buffer layer devices practically show no scaling. The V_{PT} or $V_{BR\ OFF}$ for different L_{GD} are shown in Figure 4.3–8(b). The $V_{BR\ OFF}$ is low and independent on the L_{GD} for the GaN-buffer layer HEMTS. In contrast, the DH-HEMTs show a scale-up up to a saturation of L_{GD} = 10 µm with $V_{BR\ OFF}$ above 400 V. For DH-HEMTs, the slope of the scaling as well as the maximum $V_{BR\ OFF}$ clearly increases with the reduction of the thickness of the GaN channel layer. The scale up reaches saturation at L_{GD} of 10 µm at ~400 V, 6 µm at ~260 V and 3 µm at ~125 V for GaN channel thickness of 15 nm and 35 nm, 90 nm and 110 nm respectively. The maximum scale up slope reaches ~50 V/µm, ~50 V/µm, ~42 V/µm and ~33 V/µm for GaN channel thickness, d_{Ch}, of 15 nm, 35 nm, 90 nm and 110 nm respectively.

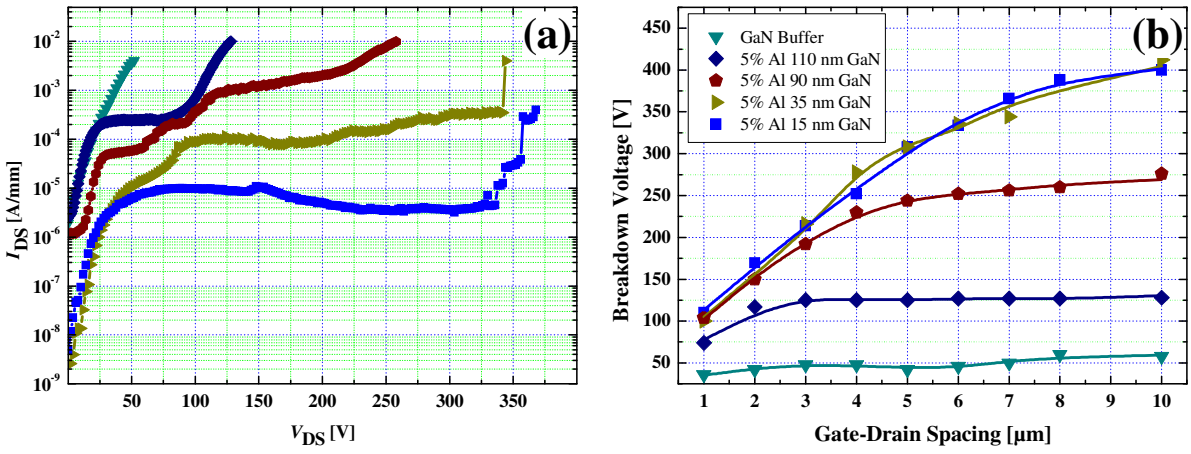


Figure 4.3–8 Wafer-set-I (y = 0.05) breakdown characteristics (a) Sub-threshold drain current monitor during breakdown voltage measurements for device with GaN buffer and DH-HEMTs devices with different GaN channel thickness. Devices' gate drain spacing is L_{GD} = 7 µm. (b) Devices' breakdown voltage dependence on gate drain spacing, L_{GD}, for DH-HEMT devices with different GaN channel thickness. W_G = 2 × 125 µm and L_G = 0.7 µm.

Figure 4.3–9 shows a wafer level comparison between the drain and the gate sub-threshold current during breakdown measurements. For a well confined UID GaN channel d_{Ch} = 15 nm the gate current is lower compared to the drain current. With the increase of the UID GaN channel thickness, d_{Ch} = 35 nm, the gate current looks more and more like the drain current and for devices with d_{Ch} = 90 nm the gate and drain currents are almost identical i.e. the source of the sub-threshold leakage current is entirely from the Schottky reverse biased gate.

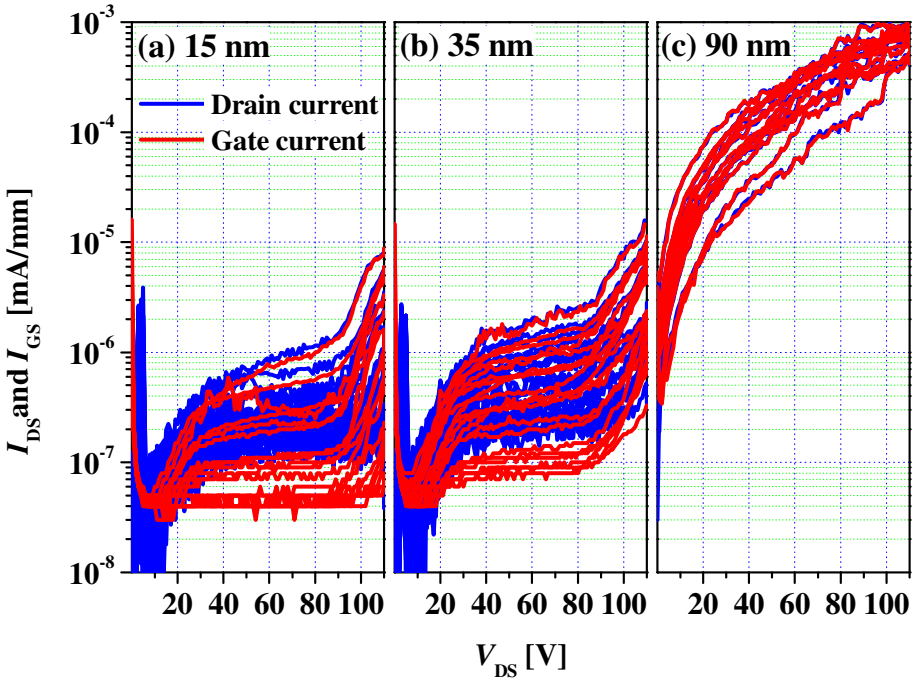


Figure 4.3–9 The sub-threshold drain and gate currents monitor during breakdown voltage measurements for device with GaN buffer and DH-HEMTs with $Al_{0.05}Ga_{0.95}N$ back-barrier devices with different GaN channel thickness of (a) 15 nm, (b) 35 nm and (c) 90 nm. Devices' gate drain spacing is $L_{GD} = 2$ µm, $L_G = 0.7$ µm and $W_G = 2 \times 125$ µm measured at $V_{GS} = -5$ V.

Typical three-terminal drain current injection OFF-state breakdown voltage measurements for devices from wafer-set-I are presented in Figure 4.3–10 [52]. The tested devices are 2×50 µm wide with $L_{GD} = 2$ µm and the injected drain current is $I_{DS} = 1$ mA/mm. For device with conventional GaN buffer on wafer "A" the precursor onset of the channel breakdown BV_{DS}^{Ch} could be easily observed prior to the gate-drain breakdown BV_{DS}^{G} and followed complete flow of the injected current only through the gate BV_{DG}. This property is an indication for a weak buffer confinement which also appears in GaAs MESFETs that are known for their poor channel confinement.

For DH-HEMTs with $Al_{0.05}Ga_{0.95}N$ back-barrier improvement in the channel confinement that leads for $V_{BR\ OFF}$ enhancement is observed. For DH-HEMT with $d_{Ch} = 15$ nm the measurement does not show a clear sharp channel breakdown BV_{DS}^{Ch} and the gate sluggishly leaks. With the increase of the UID GaN channel to $d_{Ch} = 35$ nm the characteristics are changed a slight channel breakdown BV_{DS}^{Ch} is observed and the gate starts to leak rapidly as the channel is closed. This property is an indication for a strong buffer confinement which also appears in Si JFETs that are known for their superior channel confinement.

For devices with $d_{Ch} = 90$ and 110 nm the gate leakage at reverse bias is dominating the drain injection current and the BV_{DS}^{G} and BV_{DG} merges. Here the gate leaks immediately as the gate closes the channel at V_{th} and the rapidity increase in the gate current leakage reduces the device $V_{BR\ OFF}$.

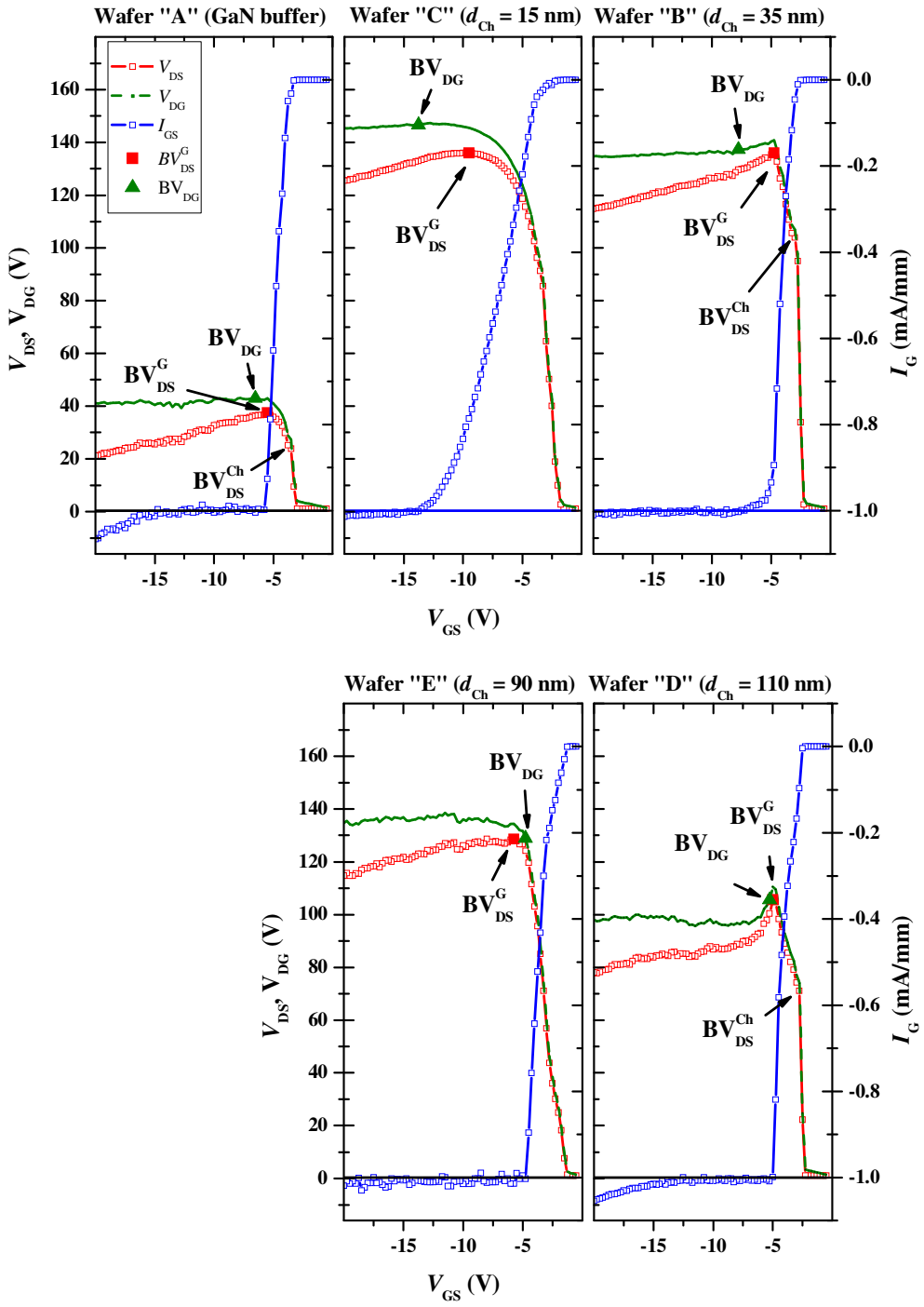


Figure 4.3–10 Three-terminal drain current injection-technique to measure $V_{BR\ OFF}$ for devices with $Al_{0.05}Ga_{0.95}N$ back-barrier devices with different GaN channel thickness of 15 to 110 nm. Devices' gate drain spacing is L_{GD} = 2 µm, L_G = 0.7 µm and W_G = 2 × 50 µm A2 measured at I_{DS} = 1 mA/mm injection current.

Figure 4.3–11 shows the comparison between the ON-state resistances multiplied by the transistors' active area (A) versus their breakdown voltage. Each point series represents a different epitaxy structure with different L_{GD} scaled transistors. It could be seen that while $R_{ON} \times A$ of the DH-HEMT transistors is comparable to the conventional GaN HEMT the $V_{BR\ OFF}$ increase is dramatic. Also, a trade-off between $R_{ON} \times A$ and the GaN channel thickness could be noticed, while the $R_{ON} \times A$ of the DH-HEMTs with the thick GaN channel, i.e. 90 nm and 110 nm, are lower than the one of the conventional GaN HEMT it is increased for the thinner GaN channel cases i.e. 15 nm and 35 nm.

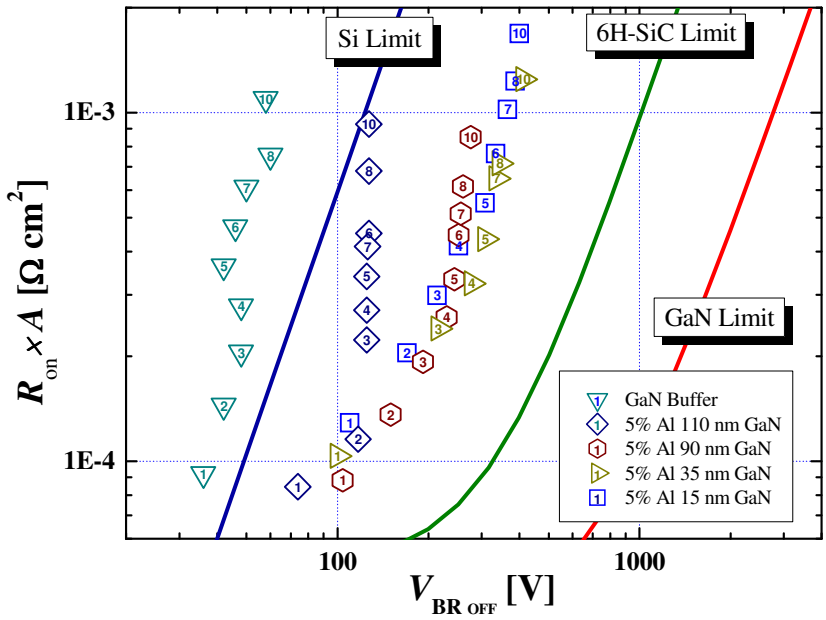


Figure 4.3–11 ON-state resistance times active area ($R_{ON} \times A$) vs. $V_{BR\ OFF}$ comparison between conventional GaN HEMT and DH-HEMTs with Al mole fraction of $y = 0.05$ and GaN channel thickness, d_{Ch}, variations on n-SiC substrate for different L_{GD} transistors (interior numbering are L_{GD} in µm). The theoretical limitations of different device families are taken from literature see section 2.4.2. $W_G = 2 \times 125$ µm and $L_G = 0.7$ µm.

4.3.2.2. DC Measurements Results of Wafer-Set-II

DC transfer characteristics for the conventional GaN HEMT and DH-HEMTs of wafer-set-II with $L_{GD} = 2$ µm, $L_G = 0.7$µm and $W_G = 2 \times 50$ µm are shown in Figure 4.3–12. The devices' key DC measurements parameters are summarized in Table 4.3–7. The reduction of the $I_{DS\ max}$ and the increase of the V_{Th} indicates a reduction in the sheet electron concentration in the 2DEG channel. In this case the electrons in the GaN channel are even more confined in a smaller volume if the AlGaN back-barrier is present.

The subthreshold regime, in Figure 4.3–12 inset, shows that the sub-threshold drain and gate leakage currents at ~V_{Th}-1.0 V are 3 orders of magnitude and more lower in wafers "G" and "H", with the AlGaN back-barrier, compared to wafer "A", GaN buffer. Here as well, an increase of reverse bias Schottky leakage current is observed with the increase of UID GaN channel thickness d_{Ch}.

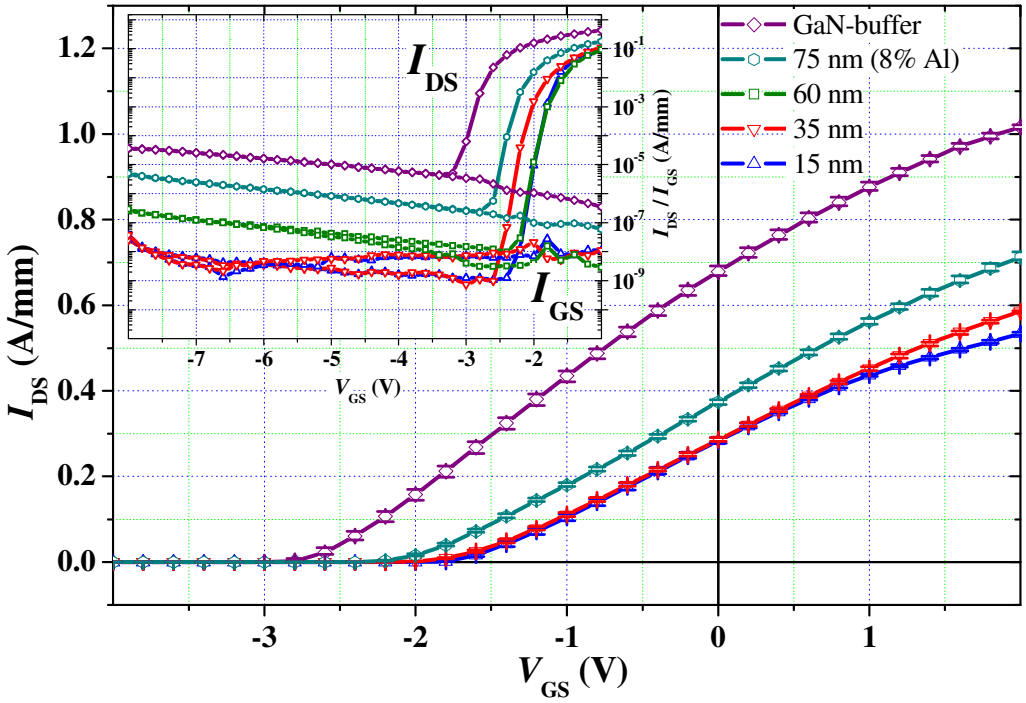


Figure 4.3–12 Wafer median transfer characteristics of conventional GaN HEMT cells and DH-HEMTs with Al mole fraction $y = 0.10$ and with different GaN channel thicknesses. (Error bars represent 25% and 75% quantiles of the measured population with in the wafer). Devices' gate drain spacing is $L_{GD} = 2$ µm, $L_G = 0.7$ µm and 2×50 µm length measured at $V_{DS} = 10$ V. Inset: log scale of the sub-threshold regime.

	Wafer "A"	Wafer "G"	Wafer "H"	Wafer "J"	Wafer "K"
FBH wafer number	GNR02-01	GNR02-03	GNR02-02	GSL01-03	GNR02-08
UID GaN channel thickness d_{Ch}	GaN buffer	35 nm	15 nm	60 nm	75 nm
V_{Th} (V)	-3.03	-2.01	-1.96	-1.80	-2.13
$I_{DS\,max}$ (V_{GS} = +2V) (A/mm)	0.95	0.59	0.53	0.60	0.71
$V_{BR\,OFF}$ (2 ×50 µm, L_{GD} =2 µm) (V)	37(±5)	137(±6)	130(±5)	115(±4)	84(±9)
R_{ON} (Ω·mm)	2.63	3.40	3.63	2.99	2.59
$I_{GS\,leak}$ ($V_{GS} = V_{Th}$-1.0 V) (A/mm)	5.47×10^{-6}	7.56×10^{-9}	6.90×10^{-9}	3.12×10^{-9}	2.54×10^{-7}
$I_{DS\,leak}$ ($V_{GS} = V_{Th}$-1.0 V) (A/mm)	5.59×10^{-6}	7.33×10^{-10}	1.26×10^{-9}	1.37×10^{-9}	2.63×10^{-7}
$g_{m\,max}$ (mS/mm)	227	180	181	196	213

Table 4.3–7 DC measurements parameters summary of inline monitoring 2×50 µm A2 devices, $L_{GD} = 2$ µm and $L_G = 0.7$ µm for compared wafer-set-II ($y = 0.08$ to 0.10).

The buffer resistivity was measured between two isolated ohmic contact pads at 100 V. Wafer median resistivity was 10.93 $\log_{10}(\Omega/\square)$, 11.40 $\log_{10}(\Omega/\square)$, 11.81 $\log_{10}(\Omega/\square)$, 9.06 $\log_{10}(\Omega/\square)$ and 11.14 $\log_{10}(\Omega/\square)$, for GaN Buffer, GaN channel thickness of 15 nm, 35 nm, 60 nm and 75 nm, respectively. The wafer with 60 nm suffered from severe substrate leakage.

The $V_{BR\,OFF}$ of the devices from wafer-set-II was measured at closed gate conditions below a threshold bias $V_{Th} >> V_{GS} = V_{Th}$ -2 V in air ambient. The drain bias was increased and logged until breakdown was identified. The $V_{BR\,OFF}$ were defined as the voltage at which the drain current exceeds the value of 10 mA/mm. Figure 4.3–13(a) shows examples of sub-threshold drain-leakage current measurements for $L_{GD} = 7$ µm transistors for conventional HEMTs with GaN buffer layer and DH-HEMTs with different GaN channel thickness layer of $d_{Ch} = 15$ nm, 35 nm, and 75 nm. As before the results show orders of magnitude reduction in

the sub-threshold drain leakage current for the DH-HEMTs and a dramatic improvement in the device $V_{BR\ OFF}$ characteristic from 50 V, for conventional GaN HEMTs, to 352 V and 390 V for DH-HEMTs with d_{Ch} = 15 nm and 35 nm respectively. The scaling of the $V_{BR\ OFF}$ with increasing L_{GD} from L_{GD} = 1 µm to 10 µm has shown dramatic improvement for the DH-HEMTs devices in comparison to GaN buffer layer devices. The $V_{BR\ OFF}$ for different L_{GD} are shown in Figure 4.3–13(b). As in wafer-set-I, the DH-HEMTs show a scale-up up to a saturation of L_{GD} = 10 µm with $V_{BR\ OFF}$ of ~440 V. For DH-HEMTs, the slope of the scaling as well as the maximum $V_{BR\ OFF}$ clearly increases with the reduction of the thickness of the GaN channel layer. The scale up reaches saturation at L_{GD} of 10 µm at ~448 V, 10 µm at ~436V and 3 µm at ~170 V for GaN channel thickness of 15 nm and 35 nm, and 75 nm respectively. The maximum scale up slope reaches ~55 V/µm, ~65 V/µm, and ~40 V/µm for GaN channel thickness, d_{Ch}, of 15 nm, 35 nm, and 75 nm respectively.

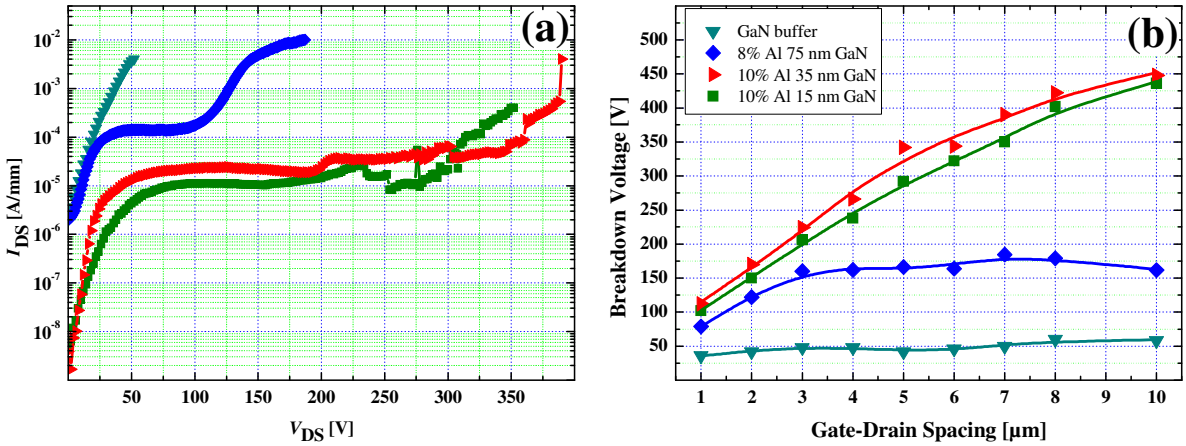


Figure 4.3–13 Wafer-set-II (y = 0.08 to 0.10) breakdown characteristics (a) Sub-threshold drain current monitor during breakdown voltage measurements for device with GaN buffer and DH-HEMTs devices with different GaN channel thickness. Devices' gate drain spacing is L_{GD} = 7 µm. (b) Devices' breakdown voltage dependence on gate drain spacing, L_{GD}, for DH-HEMT devices with different GaN channel thickness. W_G = 2 × 125 µm and L_G = 0.7 µm.

Figure 4.3–14 shows a wafer level comparison between the drain and the gate sub-threshold current during breakdown measurements. For a well confined UID GaN channel d_{Ch} = 15 nm the gate current is lower compared to the drain current. With the increase of the UID GaN channel thickness, d_{Ch} = 35 nm, the gate current looks more and more like the drain current and for devices with d_{Ch} = 75 nm the gate and drain currents are almost identical i.e. the source of the sub-threshold leakage current is entirely from the Schottky reverse biased gate.

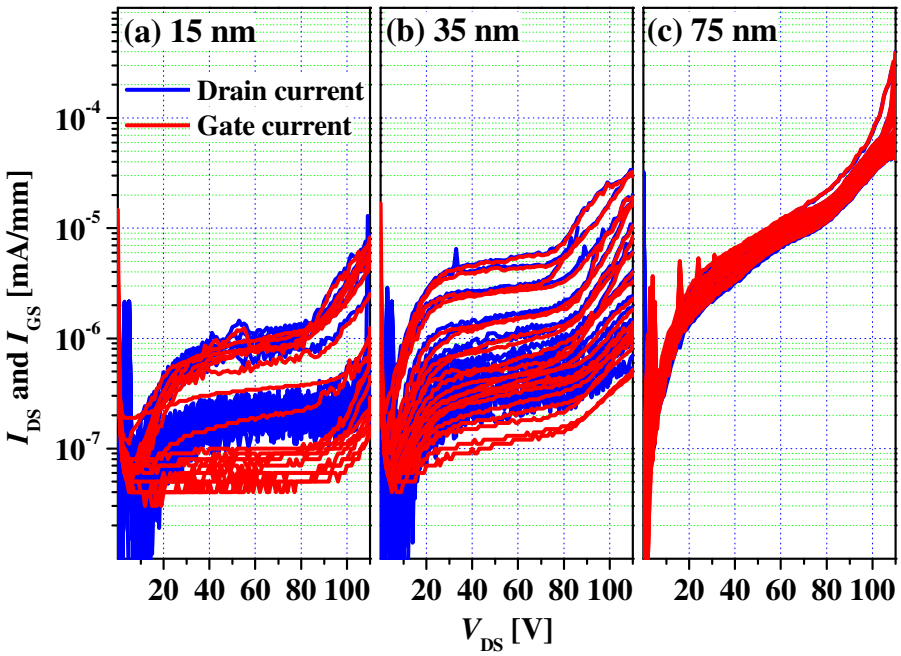


Figure 4.3–14 The sub-threshold drain and gate currents monitor during breakdown voltage measurements for device with GaN buffer and DH-HEMTs with $Al_{0.10}Ga_{0.90}N$ back-barrier devices with different GaN channel thickness of (a) 15 nm, (b) 35 nm and (c) 75 nm ($Al_{0.08}Ga_{0.92}N$ back-barrier). Devices' gate drain spacing is L_{GD} = 2 µm, L_G = 0.7 µm and W_G = 2 × 125 µm measured at V_{GS} = -5 V.

Typical three-terminal drain current injection OFF-state breakdown voltage measurements for devices from wafer-set-II are presented in Figure 4.3–15 [52]. The tested devices are 2 × 50 µm wide with L_{GD} = 2 µm and the injected drain current is I_{DS} = 1 mA/mm.

For DH-HEMTs with $Al_{0.10}Ga_{0.90}N$ back-barrier the characteristics show, as previously, superior buffer confinement, which also characterize Si JFET, that are known for their strong channel confinement. The superior improvement in the channel confinement that leads to $V_{BR\ OFF}$ enhancement is again clearly observed. When comparing DH-HEMT with d_{Ch} = 15 and 35 nm the measurement shows a clear increase of the channel breakdown BV_{DS}^{Ch} this may indicate the rapid increase of the conduction band energy as was predicted in the simulation. For devices with d_{Ch} = 60 and 75 nm the gate leakage at reverse bias is dominating the drain injection current and the BV_{DS}^{G} and BV_{DG} merges. Here the gate leaks immediately as the gate closes the channel at V_{Th} and the rapidity increase in the gate current leakage that depends on the GaN channel thickness d_{Ch} reduces the device $V_{BR\ OFF}$.

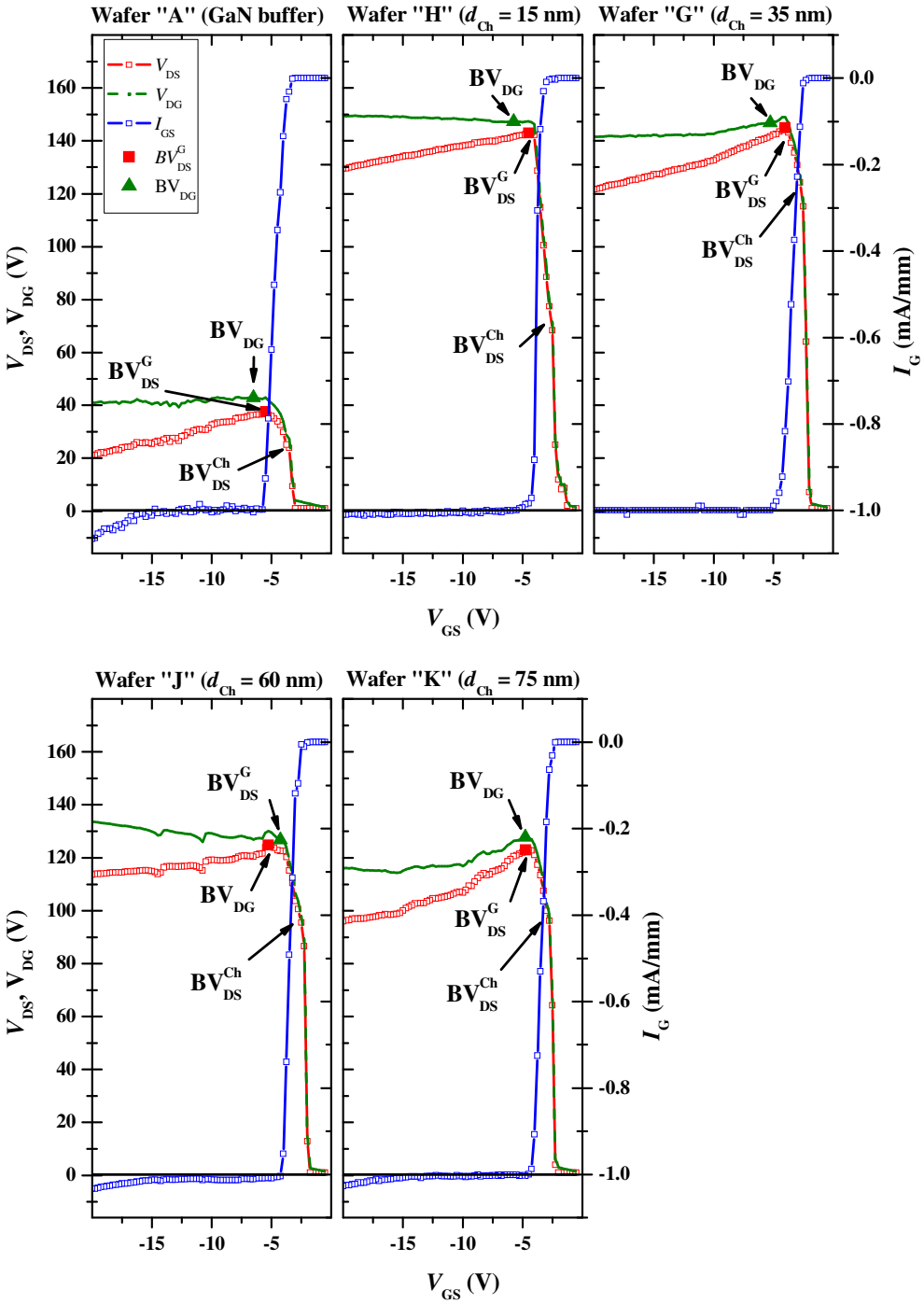


Figure 4.3–15 Three-terminal drain current injection-technique to measure $V_{BR\ OFF}$ for devices with $Al_{0.10}Ga_{0.90}N$ back-barrier devices with different GaN channel thickness of 15 to 75 nm. Devices' gate drain spacing is $L_{GD} = 2$ µm, $L_G = 0.7$ µm and $W_G = 2 \times 50$ µm A2 measured at $I_{DS} = 1$ mA/mm injection current.

Figure 4.3–16 shows the comparison between the ON-state resistances multiplied by the transistors' active area (A) versus their breakdown voltage in wafer-set-II. Each point series represents a different epitaxy structure with different L_{GD} scaled transistors. It could be seen that while $R_{ON} \times A$ of the DH-HEMT transistors is comparable to the conventional GaN HEMT the $V_{BR\ OFF}$ increase is dramatic. Also, a trade-off between $R_{ON} \times A$ and the GaN channel thickness could be noticed, while the $R_{ON} \times A$ of the DH-HEMTs with the thick GaN channel, i.e. 75 nm, are lower than the one of the conventional GaN HEMT it is increased for

the thinner GaN channel cases i.e. 15 nm and 35 nm.

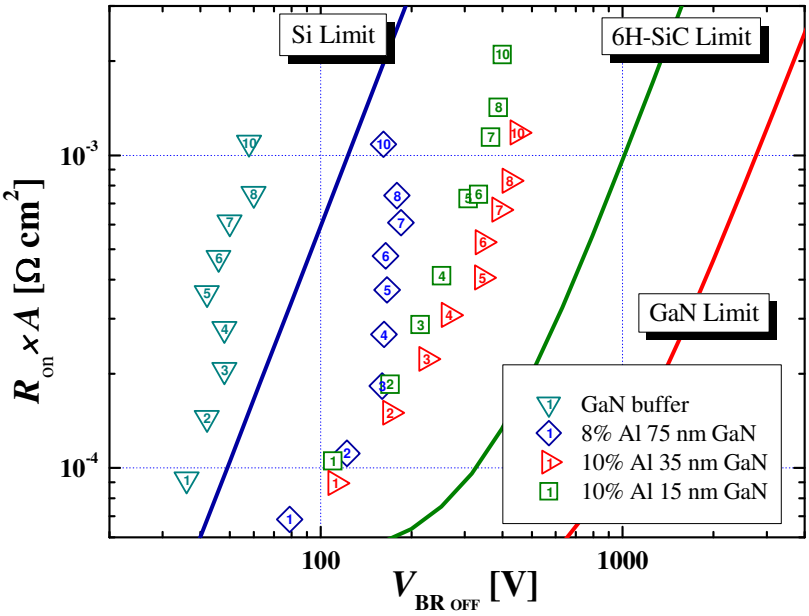


Figure 4.3–16 On resistance times active area ($R_{ON} \times A$) vs. $V_{BR\ OFF}$ comparison between conventional GaN HEMT and DH-HEMTs with Al mole fraction of 0.10 and GaN channel thickness variations on *n*-SiC substrate for different L_{GD} transistors (interior numbering are L_{GD} in µm). The theoretical limitations of different device families are taken from literature see section 2.4.2. $W_G = 2 \times 125$ µm and $L_G = 0.7$ µm.

4.3.2.3. DC Measurements Results of Wafer-Set-III

DC transfer characteristics for the conventional GaN HEMT and DH-HEMTs of wafer-set-III with $L_{GD} = 2$ µm, $L_G = 0.7$µm and $W_G = 2 \times 50$ µm are shown in Figure 4.3–17. The devices' key DC measurements parameters are summarized in Table 4.3–8. Wafer "M" with $Al_{0.02}Ga_{0.98}N$ back-barrier shows, as in previous back-barrier wafers, reduction of the $I_{DS\ max}$ and the increase of the V_{Th} when compared to reference conventional GaN buffer, wafer "L". The increase of the Al mole fraction, x, in the top-barrier in wafer "N" while keeping the $Al_{0.02}Ga_{0.98}N$ back-barrier, increase again the $I_{DS\ max}$ and shifts back the V_{Th}. In this case, increase of the lattice mismatch and therefore increase of the polarization charge in the top interface increases the 2DEG sheet carrier density. Even though that the lattice mismatch is larger in wafer "N" than in wafer "L" the polarization charge could not be fully recovered and the increase of the $I_{DS\ max}$ and the shift of the V_{Th} does not reach the original values. Thus the increase of the Al mole fraction in the top barrier does not compensate for the reduction in the sheet electron concentration in the 2DEG channel.

Comparison of the sub-threshold regime, in Figure 4.3–17 inset, shows that the sub-threshold drain and gate leakage currents at ~V_{Th}-1.0 V are somewhat lower in wafer "M" with the $Al_{0.02}Ga_{0.98}N$ back-barrier, compared to reference wafer "L", GaN buffer both owning the same Al mole fraction in the top-barrier. The increase of the Al mole fraction in the top barrier to $y = 0.28$ results in increase of the sub-threshold leakages to the values of wafer "L" with the conventional GaN buffer. Here an increase of reverse bias Schottky leakage current is observed with the increase of mole fraction in the top barrier to $y = 0.28$.

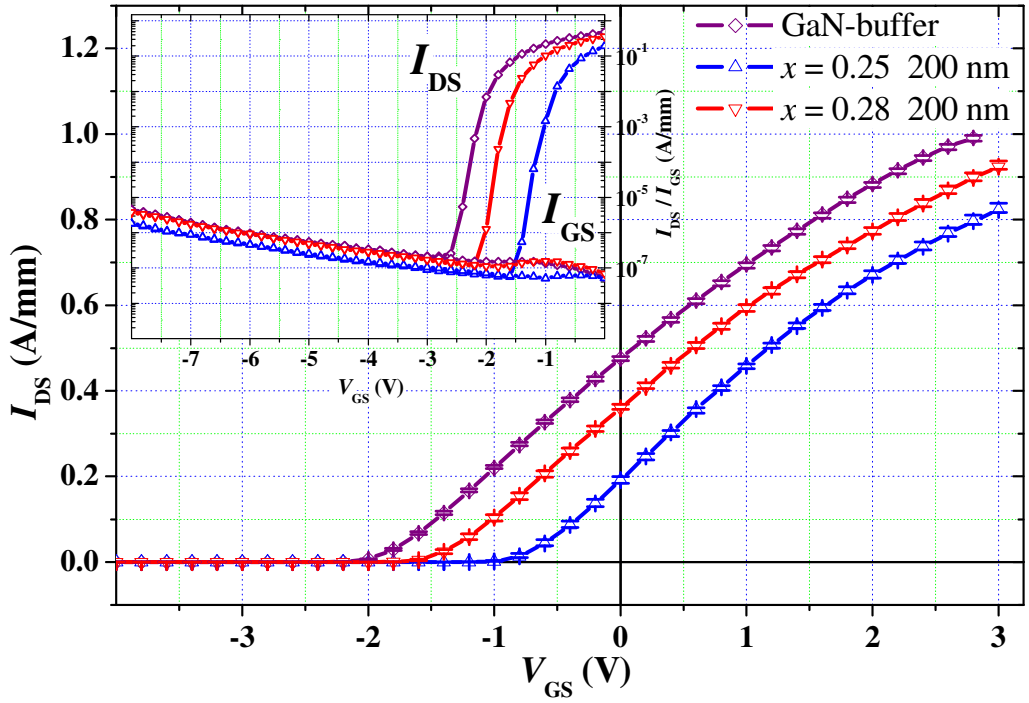


Figure 4.3–17 Wafer median transfer characteristics of conventional GaN HEMT cells and DH-HEMTs with Al mole fraction $y = 0.02$ and 200 nm GaN channel thicknesses with different AlGaN top-barrier composition.(Error bars represent 25% and 75% quantiles of the measured population with in the wafer). Devices' gate drain spacing is $L_{GD} = 2$ µm, $L_G = 0.7$µm and $W_G = 2 \times 50$ µm measured at $V_{DS} = 10$ V. Inset: log scale of the sub-threshold regime.

	Wafer "L"	Wafer "M"	Wafer "N"
FBH wafer number	GNR02-10	GNR02-11	GNR02-13
Top-barrier Al mole fraction x	GaN Buffer	0.25	0.28
V_{Th} (V)	-2.12	-1.13	-1.81
$I_{DS\ max}$ (V_{GS} = +2V) (A/mm)	0.89	0.67	0.77
$V_{BR\ OFF}$ (2 ×50 µm, L_{GD} =2 µm) (V)	44(±5)	55(±6))	38(±3)
R_{ON} (Ω·mm)	2.22	2.23	2.30
$I_{GS\ leak}$ ($V_{GS} = V_{Th}$-1.0 V) (A/mm)	2.30×10^{-7}	7.90×10^{-8}	1.56×10^{-7}
$I_{DS\ leak}$ ($V_{GS} = V_{Th}$-1.0 V) (A/mm)	2.27×10^{-7}	6.62×10^{-8}	1.46×10^{-7}
$g_{m\ max}$ (mS/mm)	271	277	266

Table 4.3–8 DC measurements parameters summary of inline monitoring 2 × 50 µm A2 devices, $L_{GD} = 2$ µm and $L_G = 0.7$ µm for compared wafer-set-III.

The dependencies of the ON-state resistance, R_{ON}, on the gate-drain separation, L_{GD}, for wafers with different top-barrier Al mole fraction, x, are presented in Figure 4.3–18. Insignificant change of the ON-state resistance with the increase of the top-barrier Al mole fraction with maximum difference of ~1.3 Ω·mm is observed.

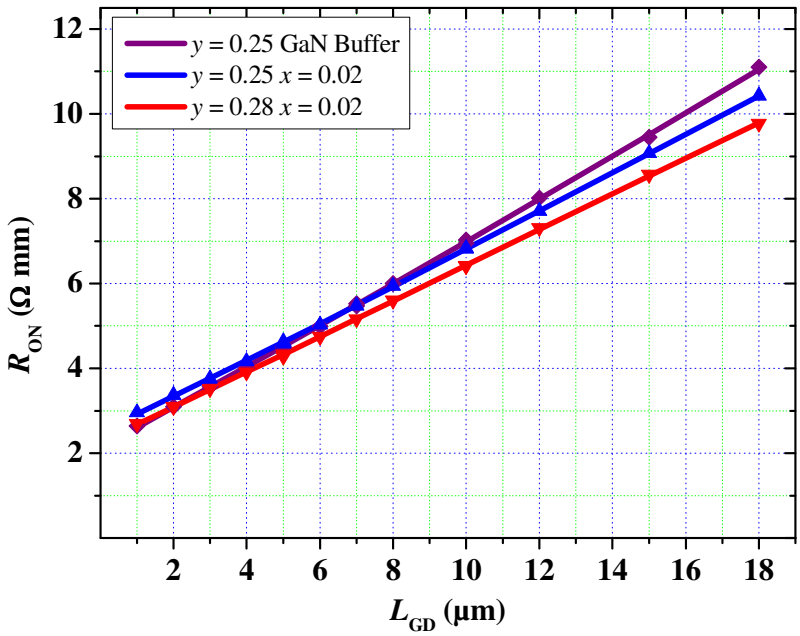


Figure 4.3–18 Wafer-set-III ($y = 0.02$): the dependence of the ON-state resistance in conventional GaN HEMT cells and DH-HEMTs with Al mole fraction $y = 0.02$ and 200 nm GaN channel thicknesses with different AlGaN top-barrier composition, for $W_G = 2 \times 125$ µm devices with $L_G = 0.7$ µm and $L_{GD} = 1$ µm to 18 µm manufactured on *n*-SiC substrate.

The $V_{BR\ OFF}$ of the devices from wafer-set-III was measured at closed gate conditions below a threshold bias $V_{Th} >> V_{GS} = V_{Th}$ -2 V in air ambient. The drain bias was increased and logged until breakdown was identified. The $V_{BR\ OFF}$ were defined as the voltage at which the drain current exceeds the value of 1.0 mA/mm. Figure 4.3–19(a) shows examples of sub-threshold drain-leakage current measurements for $L_{GD} = 7$ µm transistors for conventional HEMTs with GaN buffer layer and DH-HEMTs with different top-barrier Al mole fraction, $x = 0.25$ and 0.28.

Here the results show very little reduction in the sub-threshold drain leakage current for the DH-HEMTs and a limited in the device $V_{BR\ OFF}$ characteristic from 50 V, for conventional GaN HEMTs, to 95 V for DH-HEMTs with $Al_{0.02}Ga_{0.98}N$ back-barrier and $d_{Ch} = 200$ nm. Reduction of the device $V_{BR\ OFF}$ back to the baseline is observed when the Al mole fraction in the top-barrier increased from 0.25 to 0.28 due to the increase in the device reverse bias gate leakage.

The $V_{BR\ OFF}$ for different L_{GD} are shown in Figure 4.3–19(b). The scaling of the $V_{BR\ OFF}$ with increasing L_{GD} from $L_{GD} = 1$ µm to 10 µm has shown very small improvement for the DH-HEMTs with $Al_{0.02}Ga_{0.98}N$ back-barrier and $d_{Ch} = 200$ nm devices in comparison to GaN buffer layer devices. When the Al mole fraction in the top-barrier increased from 0.25 to 0.28 no scaling is observed and the devices' $V_{BR\ OFF}$ is limited again to less than 50 V.

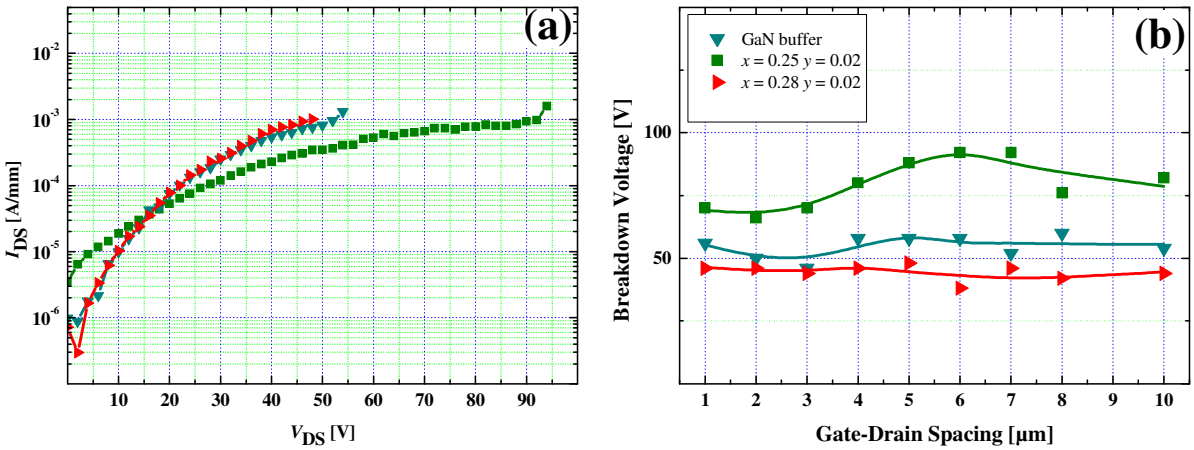


Figure 4.3–19 Wafer-set-III ($y = 0.02$) breakdown characteristics (a) Sub-threshold drain current monitor during breakdown voltage measurements for device with conventional GaN HEMT cells and DH-HEMTs with Al mole fraction $y = 0.02$ and 200 nm GaN channel thicknesses with different AlGaN top-barrier composition. Devices' gate drain spacing is $L_{GD} = 7$ µm. (b) Devices' breakdown voltage dependence on gate drain spacing, L_{GD}. $W_G = 2 \times 125$ µm and $L_G = 0.7$ µm.

Typical three-terminal drain current injection OFF-state breakdown voltage measurements for devices from wafer-set-III are presented in Figure 4.3–20 [52]. The tested devices are 2×50 µm wide with $L_{GD} = 2$ µm and the injected drain current is $I_{DS} = 1$ mA/mm.

Even a very low Al mole fraction, $y = 0.02$, in the AlGaN back-barrier and a thick UID GaN channel show an enhancement of the $V_{BR\ OFF}$ and the characterization it changes and show improvement in the buffer confinement. The gate reverse bias leakage starts as the channel closes at V_{Th}, and the values of BV_{DS}^{G} and BV_{DG} are close to each other and at the same gate bias value.

With the increase of the Al mole fraction in the top AlGaN barrier to $x = 0.28$ the breakdown voltage of the device reduces to the conventional GaN HEMT baseline values. While a comparable breakdown values achieved their characteristics are different. The DH-HEMT device with the top AlGaN barrier of $x = 0.28$ still show the same characteristics as the one with $x = 0.25$ but with much rapid increase of the gate leakage. It could be assumed that the gate aggravated leakage is a result of the high Al content in the barrier that result in increase of the strain in the AlGaN top-barrier layer and between the AlGaN top-barrier and the Schottky metal.

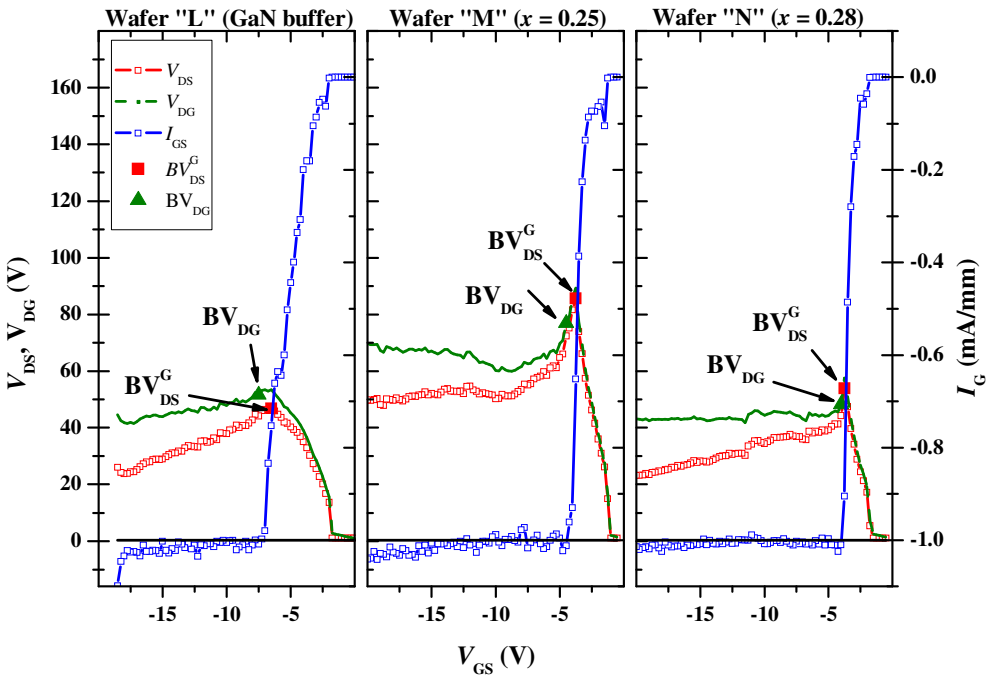


Figure 4.3–20 Three-terminal drain current injection-technique to measure $V_{BR\ OFF}$ for devices with conventional GaN HEMT cells and DH-HEMTs with Al mole fraction $y = 0.02$ and 200 nm GaN channel thicknesses with different AlGaN top-barrier composition. Devices' gate drain spacing is $L_{GD} = 2$ µm, $L_G = 0.7$ µm and $W_G = 2 \times 50$ µm A2 measured at $I_{DS} = 1$ mA/mm injection current.

4.3.2.4. DC Measurements Results of Wafer-Set-IV

DC transfer characteristics for the conventional GaN HEMT and DH-HEMTs of wafer-set-IV with $L_{GD} = 2$ µm, $L_G = 0.7$µm and $W_G = 2 \times 50$ µm are shown in Figure 4.3–21 and Figure 4.3–22. The devices' key DC measurements parameters are summarized in Table 4.3–9. DH-HEMTs grown on SI-SiC wafers exhibit, as on *n*-SiC substrate, reduction of the $I_{DS\ max}$ and the increase of the V_{Th} with the increase of the Al mole fraction, *y*, in the back-barrier due to the reduction in the sheet electron concentration in the 2DEG channel. As in previous measurements these experimental results are explained by the abrupt increase of the band gap energy at the interface between the GaN channel and the AlGaN back-barrier layer mainly due to the polarization effect induced by the AlGaN back-barrier layer. Thus electrons in the GaN channel are confined in a smaller volume if the AlGaN back-barrier is present.

From Figure 4.3–21 inset to the sub-threshold regime, it could be seen that the sub-threshold drain and gate leakage currents at ~V_{Th}-1.0 V are about 1.5 to 2 orders of magnitude lower in wafers "S" and "T", with the AlGaN back-barrier, compared to wafer "V", GaN buffer. It could be also observed that the subthreshold gate and drain leakage currents are in absolute value equal. These currents are originated by the reverse bias Schottky contact of the gate [55] and in many cases is the cause of premature OFF-state breakdown of the device. A decrease of reverse bias Schottky leakage current is observed with the increase of the Al mole fraction, *y*, in the back-barrier.

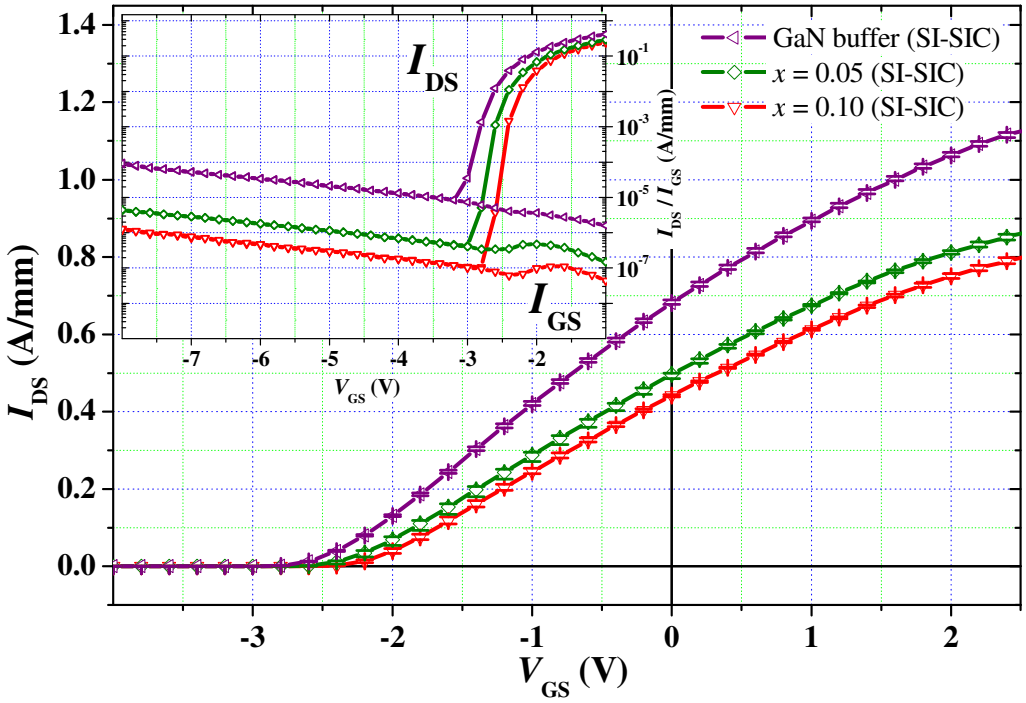


Figure 4.3–21 Wafer median transfer characteristics of conventional GaN HEMT and DH-HEMTs on SI-SiC substrate with Al mole fraction $y = 0.05$ and 0.10. The GaN channel thicknesses $d_{Ch} = 35$ nm. (Error bars represent 25% and 75% quantiles of the measured population with in the wafer). Devices' gate drain spacing is $L_{GD} = 2$ µm, $L_G = 0.7$ µm and 2×50 µm length measured at $V_{DS} = 10$ V. Inset: log scale of the sub-threshold regime.

Figure 4.3–22 compares the transfer characteristics of DH-HEMTs grown with the same epitaxial structure on different 4H-SiC substrate, SI-SiC versus *n*-SiC. The DH-HEMTs on SI-SiC exhibit higher $I_{DS\,max}$ and more negative V_{Th} in comparison to DH-HEMTs grown on *n*-SiC wafers. From Figure 4.3–22 inset to the sub-threshold regime, it could be seen that the sub-threshold drain and gate leakage currents at ~V_{Th}-1.0 V are about 1.5 to 2 orders of magnitude lower in wafers "Q" and "R", with the AlGaN back-barrier grown on *n*-SiC substrate, compared to wafers "S" and "T", with the AlGaN back-barrier grown on SI-SiC substrate. In contrast to DH-HEMTs grown on SI-SiC the subthreshold drain leakage currents measured in DH-HEMTs grown on *n*-SiC is lower in absolute value from the gate leakage current. This indicates a superior channel confinement in DH-HEMTs grown on *n*-SiC.

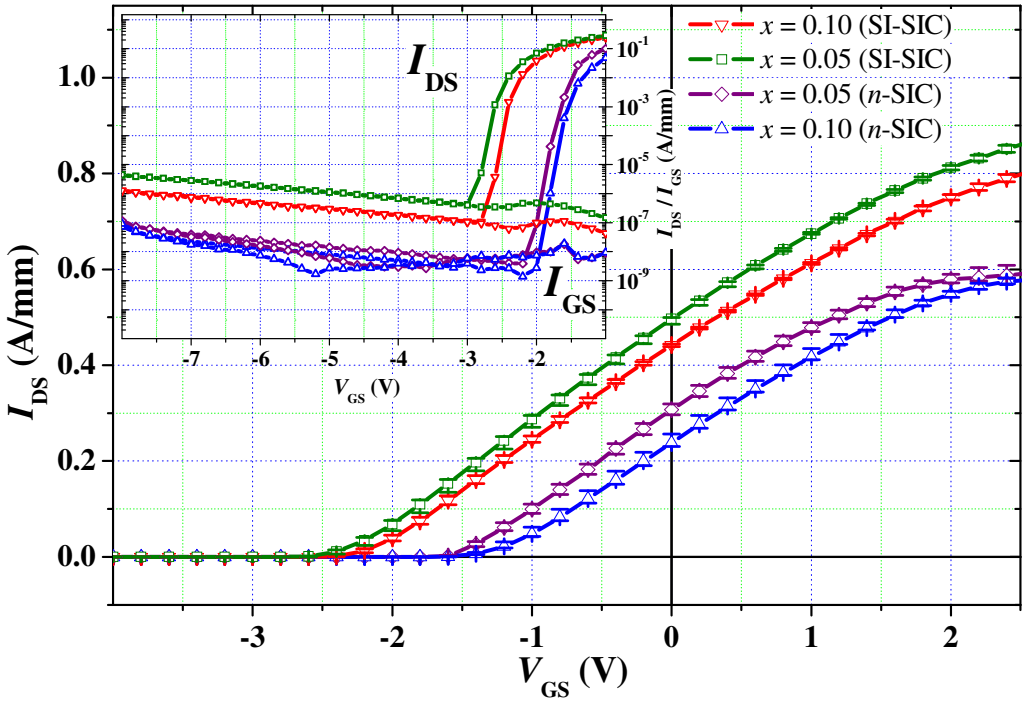


Figure 4.3–22 Wafer median transfer characteristics of DH-HEMTs on *n*-SiC and SI-SiC substrates with Al mole fraction $y = 0.05$ and 0.10. The GaN channel thicknesses $d_{Ch} = 35$ nm. (Error bars represent 25% and 75% quantiles of the measured population with in the wafer). Devices' gate drain spacing is $L_{GD} = 2$ µm, $L_G = 0.7$ µm and 2×50 µm length measured at $V_{DS} = 10$ V. Inset: log scale of the sub-threshold regime.

	Wafer "A"	Wafer "Q"	Wafer "R"	Wafer "S"	Wafer "T"	Wafer "V"
FBH wafer number	GNR02-01	GSL01-01	GSL01-04	GSL01-06	GSL01-05	GSL01-07
Back-barrier Al mole fraction *y*	GaN buffer	0.05	0.10	0.05	0.10	GaN buffer
V_{Th} (V)	-3.03	-1.84	-1.56	-2.61	-2.39	-2.91
$I_{DS\ max}$ (V_{GS} = +2V) (A/mm)	0.95	0.58	0.55	0.81	0.75	1.06
$V_{BR\ OFF}$ (2 ×50 µm, L_{GD} =2 µm) (V)	37(±5)	96(±5)	127(±3)	78(±19)	124(±10)	26(±4)
R_{ON} (Ω·mm)	2.63	3.18	3.20	2.31	2.31	2.08
$I_{GS\ leak}$ ($V_{GS} = V_{Th}$-1.0 V) (A/mm)	5.47×10^{-6}	6.11×10^{-9}	5.31×10^{-9}	5.54×10^{-7}	1.36×10^{-7}	1.30×10^{-5}
$I_{DS\ leak}$ ($V_{GS} = V_{Th}$-1.0 V) (A/mm)	5.59×10^{-6}	5.10×10^{-9}	2.78×10^{-9}	5.65×10^{-7}	1.36×10^{-7}	1.29×10^{-5}
$g_{m\ max}$ (mS/mm)	227	211	198	224	213	272
Substrate	*n*-SiC			SI-SiC		

Table 4.3–9 DC measurements parameters summary of inline monitoring 2×50 µm A2 devices, $L_{GD} = 2$ µm and $L_G = 0.7$ µm for compared wafer-set-IV.

The $V_{BR\ OFF}$ of the devices from wafer-set-IV was measured at closed gate conditions below a threshold bias $V_{Th} >> V_{GS} = V_{Th}$ -2 V in air ambient. The drain bias was increased and logged until breakdown was identified. The $V_{BR\ OFF}$ were defined as the voltage at which the drain current exceeds the value of 1 mA/mm. Figure 4.3–23(a) shows examples of sub-threshold drain-leakage current measurements for $L_{GD} = 7$ µm transistors for conventional HEMTs on SI-SiC substrate with GaN buffer layer and DH-HEMTs on SI-SiC and *n*-SiC substrates were an $Al_{0.10}Ga_{0.90}N$ serves as back-barrier with a GaN channel thickness layer of $d_{Ch} = 35$ nm.

It could be seen that the DH-HEMTs on SI-SiC exhibit limited suppression of the subthreshold leakage currents and enhancement of the $V_{BR\ OFF}$ from ~50 V to ~150 V is observed. Here, consistently with the transfer characteristics (Figure 4.3–22 inset), the results show reduction in the sub-threshold drain leakage current for the DH-HEMTs grown on SI-SiC compared with conventional GaN HEMTs. Figure 4.3–23(a) inset shows in linear

scale both drain and gate subthreshold leakage currents of the examined devices. Here, for the devices grown on SI-SiC substrate, the symmetry seen between the gate and drain currents, indicates the subthreshold leakage current originated from the Schottky gate contact. In the case of DH-HEMT grown on *n*-SiC substrate the gate leakage is lower than the buffer / drain leakage and therefore a significant enhancement of the breakdown voltage is exhibited.

The $V_{BR\ OFF}$ for different L_{GD} are shown in Figure 4.3–23(b). The scaling of the $V_{BR\ OFF}$ with increasing L_{GD} from $L_{GD} = 1\ \mu m$ to $10\ \mu m$ has shown dramatic improvement for the DH-HEMTs devices in comparison to GaN buffer layer devices. The DH-HEMTs grown on SI-SIC show very limited scale-up up to a saturation of $L_{GD} = 2\ \mu m$ with $V_{BR\ OFF}$ of ~125 V.

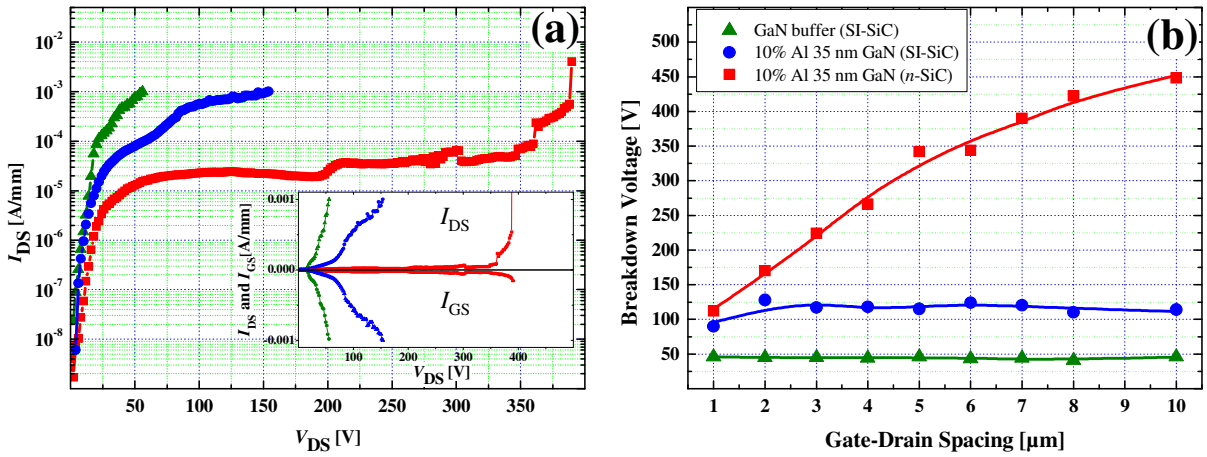


Figure 4.3–23 Wafer-set-IV breakdown characteristics (a) Sub-threshold drain current monitor during breakdown voltage measurements for device with GaN buffer on SI-SiC substrate and DH-HEMTs devices with $Al_{0.10}Ga_{0.90}N$ back barrier and GaN channel thickness of 35 nm grown on SI-SiC and *n*-SiC substrates. Devices' gate drain spacing is $L_{GD} = 7\ \mu m$. (b) Devices' breakdown voltage dependence on gate drain spacing, L_{GD}, for DH-HEMTs devices with $Al_{0.10}Ga_{0.90}N$ back barrier and GaN channel thickness of 35 nm grown on SI-SiC and *n*-SiC substrates. Inset in (a): linear scale of the sub-threshold drain current and gate current. $W_G = 2 \times 125\ \mu m$ and $L_G = 0.7\ \mu m$.

Typical three-terminal drain current injection OFF-state breakdown voltage measurements for devices from wafer-set-III are presented in Figure 4.3–24 [52]. The tested devices are $2 \times 50\ \mu m$ wide with $L_{GD} = 2\ \mu m$ and the injected drain current is $I_{DS} = 1$ mA/mm.

The comparison between conventional devices with GaN buffer grown on SI-SiC and *n*-SiC substrate a comparable characterization with similar $V_{BR\ OFF}$ values is observed. Both show a channel breakdown and buffer punch-through followed by rapid increase of the Schottky gate reverse bias tunneling leakage current but the device grown on SI-SiC show a steeper increase.

For both substrate types the introduction of AlGaN back-barrier increases the $V_{BR\ OFF}$. For devices grown on *n*-SiC substrate the increase of the Al mole fraction in the back-barrier shows increase in the channel breakdown value, BV_{DS}^{Ch}, but the gate-drain breakdown values, BV_{DS}^{G} and BV_{DG}, are similar. Here as in the device with conventional GaN buffer the gate leakage follows the channel breakdown; this is an indication for superior gate leakage prevention. On the other hand, devices that are grown on SI-SiC substrates show immediate increase of the gate current as the channel is closed an V_{Th}, therefore no channel breakdown, BV_{DS}^{Ch}, is observed and the gate-drain breakdown values, BV_{DS}^{G} and BV_{DG}, are very close. This indicates that the gate leakage prevention is weaker than the channel confinement and would create upper limitation for the OFF-state breakdown. Other indication for the good channel confinement in devices grown on SI-SiC substrates is the increase of the breakdown

voltage with the increase of the Al mole fraction from 0.05 to 0.10.

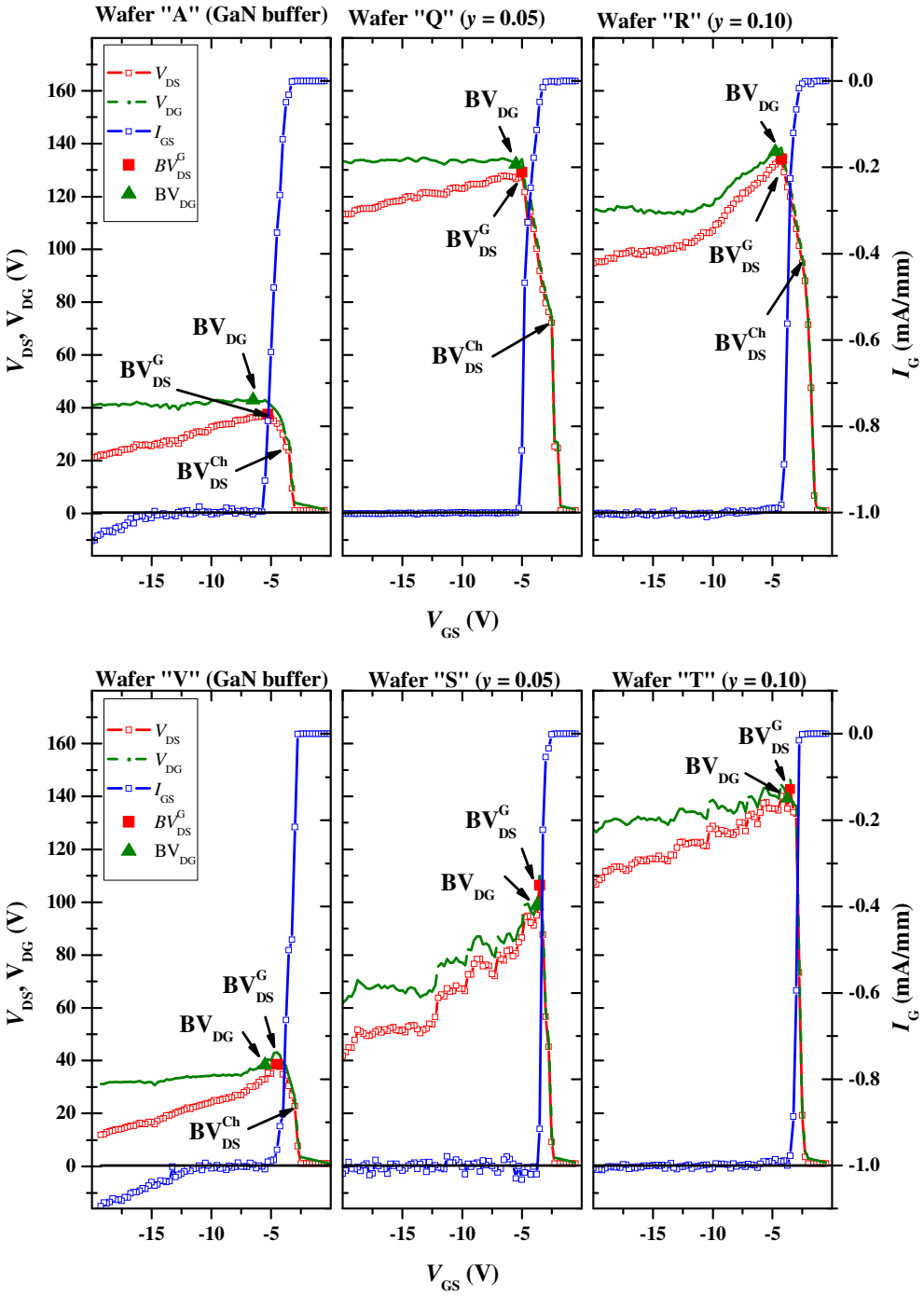


Figure 4.3–24 Drain Three-terminal drain current injection-technique to measure $V_{BR\ OFF}$ for devices with $Al_{0.05}Ga_{0.95}N$ and $Al_{0.10}Ga_{0.90}N$ back-barrier devices on *n*-SiC and SI-SiC substrates. Devices' gate drain spacing is $L_{GD} = 2$ µm, $L_G = 0.7$ µm and $W_G = 2 \times 50$ µm A2 measured at $I_{DS} = 1$ mA/mm injection current.

4.4. Robustness and Reliability

Reliability evaluation studies of AlGaN/GaN HFET devices are currently one of the most important undertakings to provide a rapid industrialization of this technology. Long and short term life tests under DC operation conditions have been performed on AlGaN/GaN HEMTs to provide reliability data at the one side and to develop techniques to predict potential reliability

problems within a short time frame. The latter aspect motivated the development of a short-term robustness test based on DC-Step-Stress testing [83], [97]. The intention of this test is to provide a rapid technique to study the robustness as processed devices in order to provide a rapid feed-back to device development and processing.

So far, the main failure modes identified during aging of GaN HFETs result in irreversible changes, for example the drain current I_{DS}, the sub-threshold drain current $I_{DS\,sub}$, the gate leakage current I_{GS}, the threshold voltage V_{Th}, the output power P_{out} or the ON-state resistance R_{ON}. In this test, the focus is on the change of the gate leakage current during on-wafer DC-Step-Stress testing as an indicator of degradation. This test is considered as a robustness test which, in comparison to long term aging, gives results in quite a short time. However it has still to be proven, whether there is a direct correlation with long term tests. It has been found that a threshold drain voltage is existing beyond which device starts to degrade. It is defined as the drain voltage where the gate leakage current starts to increase irreversibly. The onset of leakage current increase with time is considered as an indicator of a starting degradation in this case. Experimental data revealed that the threshold for degradation is more positive if the Al concentration in AlGaN top-barrier is reduced and/or if a GaN cap design is present [98]. In this chapter the performance of devices with and without AlGaN back-barrier has been compared. Different physical mechanisms such as thermionic emission, tunneling, surface or bulk hopping mechanisms and impact ionization holes currents may explain gate leakage current increase observed during stress testing. The first two mechanisms are related to the properties of the Schottky contact (gate) and its effective barrier on a given epitaxial layer sequence, the latter effects could explain gate leakage caused by surface or bulk defects and the channel confinement.

In order to investigate the influence of a AlGaN back-barrier grown on *n*-SiC wafers, a DC-Step-Stress tests were preformed on 2×125 µm and $L_{GD} = 6$ µm GaN-based HEMTs fabricated on *n*-SiC wafers; a conventional GaN buffer wafer (a) a DH-HEMT with $Al_{0.05}Ga_{0.95}N$ back barrier and 15 nm UID channel layer (b) and a DH-HEMT with $Al_{0.05}Ga_{0.95}N$ buffer and 35 nm UID cannel layer. The wafers epitaxial structures and properties are given in Table 4.3–2 and their DC measurement results are presented in section 4.3.2.

The DC-Step-Stress tests were conducted by increasing the drain-source voltage V_{DS} by 5 V every two hours. The devices were operated at OFF-state conditions at a gate voltage well below threshold voltage ($V_{Th} >> V_{GS} = -7$V). The critical voltage $V_{DS\,deg}$ for a starting degradation is defined as the voltage where the gate current starts to increase irreversibly during an individual step at a respective bias level.

Figure 4.4–1(a) shows a typical gate leakage current during Step-Stress-Test for an epitaxial design on conventional GaN-based HEMT with UID GaN buffer. Initially a recovery of the gate leakage current takes place after every increase of drain voltage. This might be due to the population of trap states in the vicinity of the gate. However, exceeding a certain threshold voltage, the gate leakage does not recover any more within one step period but starts to increase irreversibly. The onset of irreversible gate leakage degradation is marked in Figure 4.4–1. This point is referred as the threshold of degradation ($V_{DS\,deg}$). For device conventional GaN-based HEMT the gate leakage current starts to increase irreversibly at 20-30V V_{DS}. In contrast, for device having an AlGaN back-barrier grown on *n*-SiC wafers, neither increase of the gate leakage current I_{GS} nor the I_{DS} could be seen up to the maximum measurement-system drain-source voltage V_{DS} limitation of 120 V. Figure 4.4–1(b) and (c) show a typical leakage current during Step-Stress-Test for DH-HEMT devices with $Al_{0.05}Ga_{0.95}N$ back-barrier and UID GaN channel thickness of 15 nm or 35 nm respectively.

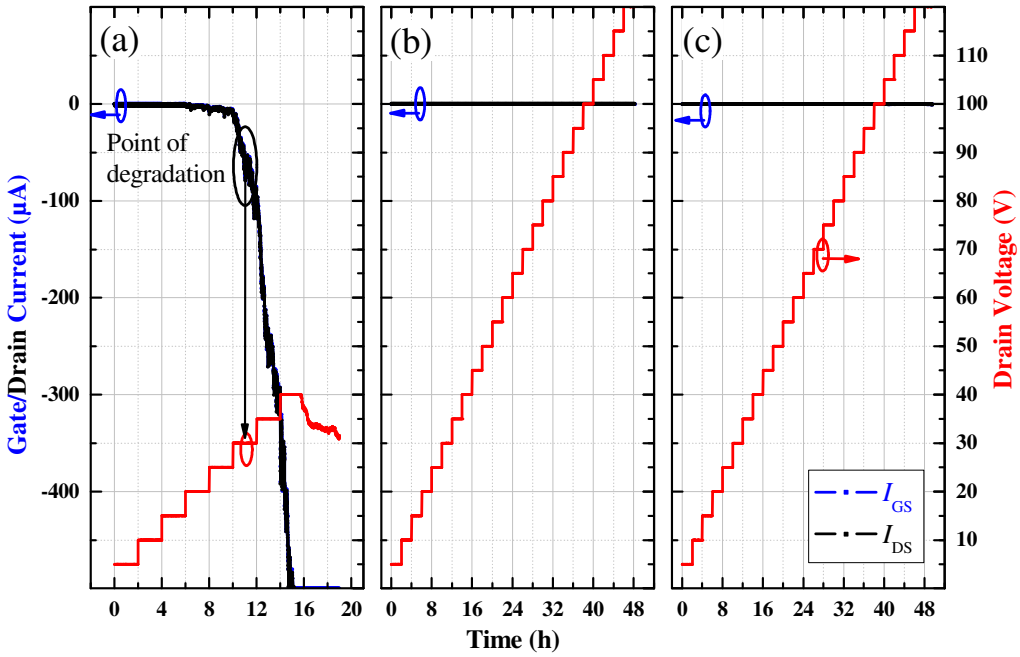


Figure 4.4–1 A typical step-stress-test of (a) GaN buffer layer (b) $Al_{0.05}Ga_{0.95}N$ buffer layer with 15 nm UID GaN channel and (c) $Al_{0.05}Ga_{0.95}N$ buffer layer with 35 nm UID GaN channel, grown on *n*-SiC wafers. Where V_{GS} = -7 V and L_{GD} = 6 µm, W_G = 2 × 125 µm and L_G = 0.7 µm.

The sub-threshold drain current of conventional GaN-based HEMT with UID GaN buffer starts to increase significantly if the drain voltage exceeds about 30 V. The subthreshold drain current and gate leakage increase simultaneously and showed exactly the same values. This effect is more pronounced as the drain voltage V_{DS} further increases. This suggests an electron current flow from the gate directly to the drain and it believed that this behavior is related to the poor buffer confinement at higher voltage [79]. Any further stepwise increase of the drain voltage provokes a corresponding increase of the sub-threshold current. Within one step the drain current decreases exponentially. This could be an indication of trap charging at these conditions. The higher the drain-voltage the higher the sub-threshold drain leakage current. Electrons that are injected into the GaN buffer can then start to occupy trap levels there and thus reduce the available carrier density in the channel. The occupation of slow traps results in the observed exponential decay of the sub-threshold drain leakage current during one step period.

On the other hand, by employing an AlGaN back-barrier in the devices both source-drain and gate drain sub-threshold leakage currents are restrained. The charge carriers are prevented from being trapped in the buffer traps level and/or in the upper AlGaN barrier. Therefore, no degradation was observed in the devices even after attaining maximum measured drain voltage much smaller than the devices OFF-state breakdown voltage.

This finding is supported by Electroluminescence (EL)-measurements in OFF-state conditions. In degraded samples from wafer with conventional GaN buffer bright spots appear between the gate and drain region at reverse biased conditions as shown in Figure 4.4–2. The increase of bright spots could relate to the defects created during the stress which may open a pathway for electrons to overcome the barrier. Chen [99] pointed out that extended defect complexes may be responsible for spotty behavior at OFF-state.

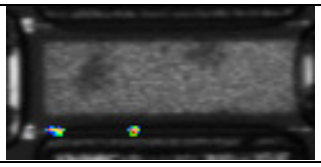
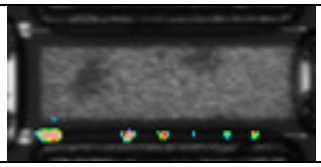
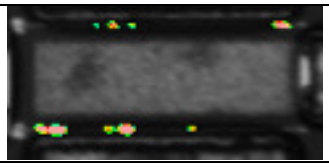
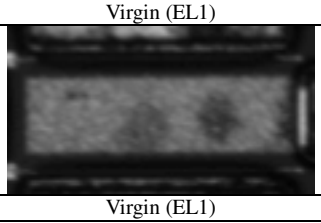
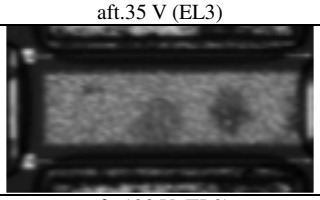
Wafer "A"			
	Virgin (EL1)	aft. 15 V(EL2)	aft.35 V (EL3)
Wafer "B"			
	Virgin (EL1)		aft. 120 V (EL2)

Figure 4.4–2 Evolution of EL spots at OFF-state (V_{GS} = -7 V, V_{DS} = 10 V, L_{GD} = 6 µm, W_G = 2 × 125 µm and L_G = 0.7 µm) during step stressing. Note: EL intensity is not yet normalized.

Physical device simulations indicate that the internal electrical fields at OFF-state conditions for wafers with AlGaN back barrier are significantly smaller as compared to conventional GaN buffer if calculated at the same biasing conditions. This is mainly due to the modified band structure in presence of an AlGaN back-barrier and, in open conditions, also due the lower electron density in the channel. Since we have strong indications that the observed degradation of device with conventional GaN buffer occurs in the high field region of the gate, the better device robustness for devices from wafers with AlGaN back barrier may in part be attributed to local electrical-field reduction in the gate vicinity. Additionally, the presence of a bulk AlGaN back-barrier reduces the tensile strain in the AlGaN top-barrier layer of DH-HEMTs as compared to wafer with conventional GaN buffer and thus shifts the relaxation limit of the AlGaN barrier to higher Al values. This means that higher fields would be necessary to provoke a material degradation due to the inverse piezoelectric effect as suggested by Joh *et al.* [100].

4.5. Time and Frequency Domain Characterization

4.5.1. Dynamic Pulsed *I-V* (DIVA) Measurements

A dynamic pulsed *I-V* measurement (DIVA) is an efficient tool to determine the device switching efficiency and in many cases it reveals severe problems of the device. Current collapse occurs when hot channel carriers are injected into the buffer under the drift region, where they are trapped at the deep defects sites [101], [102]. Representative example of 200 ns pulsed *I-V* measurements for AlGaN back-barrier DH-HEMT from wafer set-I and set-II and conventional GaN buffer devices on *n*-SiC wafers is shown in Figure 4.5–1 and Figure 4.5–2. Figure 4.5–1 shows the pulsed *I-V* measurements of DH-HEMT with $Al_{0.05}Ga_{0.95}N$ back-barrier with GaN channel thickness of 15 nm and 35 nm. Figure 4.5–2 shows the pulsed *I-V* measurements of DH-HEMT with $Al_{0.05}Ga_{0.95}N$ and $Al_{0.10}Ga_{0.90}N$ back-barrier with constant GaN channel thickness of 35 nm.

The pulsed measurements were done at two quiescent bias points; at [V_{GS} = 0 V, V_{DS} = 0 V], to minimize the effect of thermal heating and slow traps [103] and at sub-threshold closed channel conditions of [V_{GS} = -3 V, V_{DS} = 30 V] to emphasize the drain current lag originated at the drift region.

As demonstrated in Figure 4.5–1 and Figure 4.5–2 no gate lag or knee-walk-out could be seen when pulsing from quiescent bias point V_{GS} = 0 V, V_{DS} = 0 V. A minor increase in drain current lag could be observed when measuring the DH-HEMT devices from the demanding closed channel conditions quiescent bias point of [V_{GS} = -3 V, V_{DS} = 30 V] with slight

knee-walk-out.

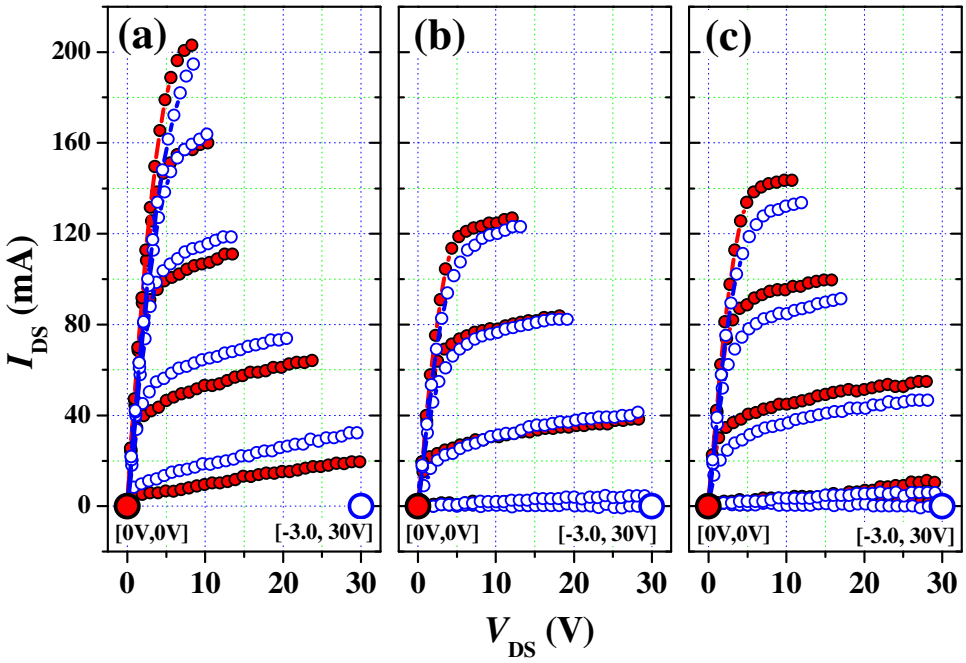


Figure 4.5–1 200 ns pulsed *I-V* (DIVA) measurements for devices with $L_{GD} = 6$ µm, $W_G = 2 \times 125$ µm and $L_G = 0.7$ µm (a) GaN buffer layer (b) $Al_{0.05}Ga_{0.95}N$ buffer layer with 15 nm UID GaN channel and (c) $Al_{0.05}Ga_{0.95}N$ buffer layer with 35 nm UID GaN channel. $V_{GS\ max} = +1$ V and $\Delta V_{GS} = 1$ V. DIVA quiescent points [$V_{GS} = 0$ V, $V_{DS} = 0$ V] (solid red dot) and [$V_{GS} = -3.0$ V, $V_{DS} = 30$ V] (empty blue dot).

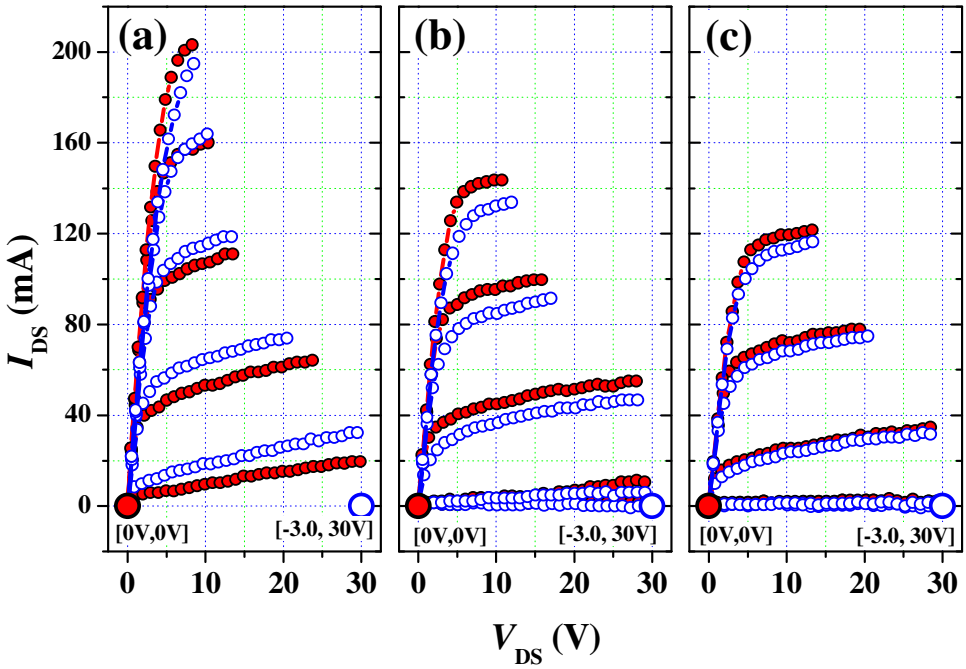


Figure 4.5–2 200 ns pulsed *I-V* (DIVA) measurements for devices with $L_{GD} = 6$ µm, $W_G = 2 \times 125$ µm and $L_G = 0.7$ µm (a) GaN buffer layer (b) $Al_{0.05}Ga_{0.95}N$ buffer layer with 35 nm UID GaN channel (c) $Al_{0.10}Ga_{0.90}N$ buffer layer with 35 nm UID GaN channel. $V_{GS\ max} = +1$ V and $\Delta V_{GS} = 1$ V. DIVA quiescent points [$V_{GS} = 0$ V, $V_{DS} = 0$ V] (solid red dot) and [$V_{GS} = -3.0$ V, $V_{DS} = 30$ V] (empty blue dot).

4.5.2. Small Signal Analysis (S-Parameters)

Small signal frequency dependent S-parameters for all types of devices with AlGaN back-barrier grown on *n*-SiC wafers were measured. The cut-off frequency, f_T, values were extracted from the $|h_{21}|^2$ parameter-curve where it equals gain of 0 dB. The maximum oscillation frequency, f_{max}, values were extracted from the maximum unilateral transducer-power gain, MUG, and maximum stable gain, MSG, parameters curves where it reaches gain of 0 dB. Typical S-parameters respond to small microwave signal for devices manufactured on wafers (a) GaN buffer layer (b) $Al_{0.05}Ga_{0.95}N$ buffer layer with 15 nm UID GaN channel and V_{GS} = -0.5 V and (c) $Al_{0.05}Ga_{0.95}N$ buffer layer with 35 nm UID GaN channel could be seen in Figure 4.5–3. Typical S-parameters respond to small microwave signal for devices manufactured on wafers (a) GaN buffer layer (b) $Al_{0.05}Ga_{0.95}N$ buffer layer with 35 nm UID GaN channel and V_{GS} = -0.5 V and (c) $Al_{0.10}Ga_{0.90}N$ buffer layer with 35 nm UID GaN channel could be seen in Figure 4.5–4. The evaluated typical f_T and f_{max} values for all types of devices are give in Table 4.5–1. It could be seen that the epitaxial design has minor effect on both f_T and f_{max}. The values are relatively low mainly due to the *n*-SiC substrate (see section 6.5.2 for evaluation of f_T and f_{max} for devices with AlGaN back-barrier manufactured on SI-SiC).

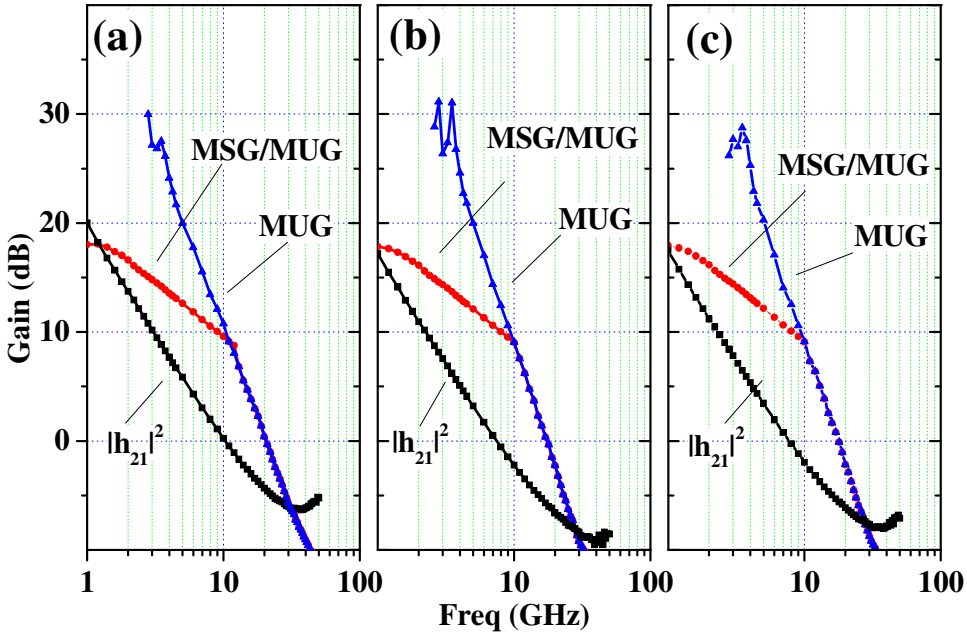


Figure 4.5–3 Frequency response small signal characteristics for devices with L_{GD} = 2 µm, W_G = 2 × 50 µm and L_G = 0.7 µm (a) GaN buffer layer measured at V_{DS} = 15 V and V_{GS} = -2.0 V (b) $Al_{0.05}Ga_{0.95}N$ buffer layer with 15 nm UID GaN channel measured at V_{DS} = 15 V and V_{GS} = -0.5 V and (c) $Al_{0.05}Ga_{0.95}N$ buffer layer with 35 nm UID GaN channel measured at V_{DS} = 15 V and V_{GS} = -0.5 V.

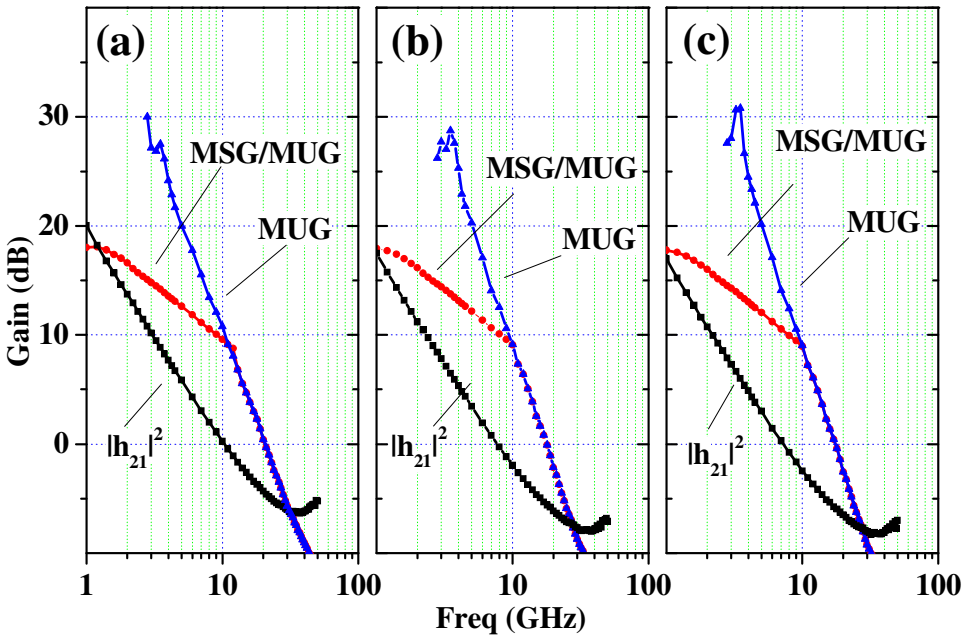


Figure 4.5–4 Frequency response small signal characteristics for devices with L_{GD} = 2 µm, W_G = 2 × 50 µm and L_G = 0.7 µm (a) GaN buffer layer measured at V_{DS} = 15 V and V_{GS} = -2.0 V (b) $Al_{0.05}Ga_{0.95}N$ buffer layer with 35 nm UID GaN channel measured at V_{DS} = 15 V and V_{GS} = -0.5 V and (c) $Al_{0.10}Ga_{0.90}N$ buffer layer with 35 nm UID GaN channel measured at V_{DS} = 15 V and V_{GS} = -0.5 V.

Layer	GaN buffer		$Al_{0.05}Ga_{0.95}N$		$Al_{0.10}Ga_{0.90}N$	
	f_T	f_{max}	f_T	f_{max}	f_T	f_{max}
GaN buffer	10.5	20.2	-	-	-	-
15 nm Channel GaN	-	-	7.4	17.8	7.2	17.6
35 nm Channel GaN	-	-	7.6	18.0	7.2	17.6
f_T and f_{max} are in GHz						

Table 4.5–1 Evaluated typical f_T and f_{max} values for DH-HEMTs devices and conventional GaN buffer devices grown on *n*-SiC substrates. Measured on inline monitoring 2 × 50 µm A2 devices, L_{GD} = 2 µm and L_G = 0.7 µm.

4.5.3. RF-Characterization from Load-Pull Measurements

Representative example of RF-characterization from load-pull measurements in class AB operation at 2 GHz for AlGaN back-barrier DH-HEMT from wafer set-I and set-II and conventional GaN buffer devices on *n*-SiC wafers is shown in Figure 4.5–5 and Figure 4.5–6. Figure 4.5–5 shows the load-pull measurements of DH-HEMT with $Al_{0.05}Ga_{0.95}N$ back-barrier with GaN channel thickness of 15 nm and 35 nm. Figure 4.5–6 shows the load-pull measurements of DH-HEMT with $Al_{0.05}Ga_{0.95}N$ and $Al_{0.10}Ga_{0.90}N$ back-barrier with constant GaN channel thickness of 35 nm.

Table 4.5–2 shows cross comparison for the tested devices of the saturated output power density with 28 V drain bias, power added efficiency (PAE), and gain. The introduction of all types of AlGaN back-barrier shows a reduction in the output power density, reduction in the power added efficiency both are associated with the reduction of the thermal conductivity with the increase of the Al mole fraction in the buffer [96]. The phenomenon is more pronounced with the increase of the device gate width. On the other hand an increase of the gain is observed. It is related to the superior channel confinement of DH-HEMT devices.

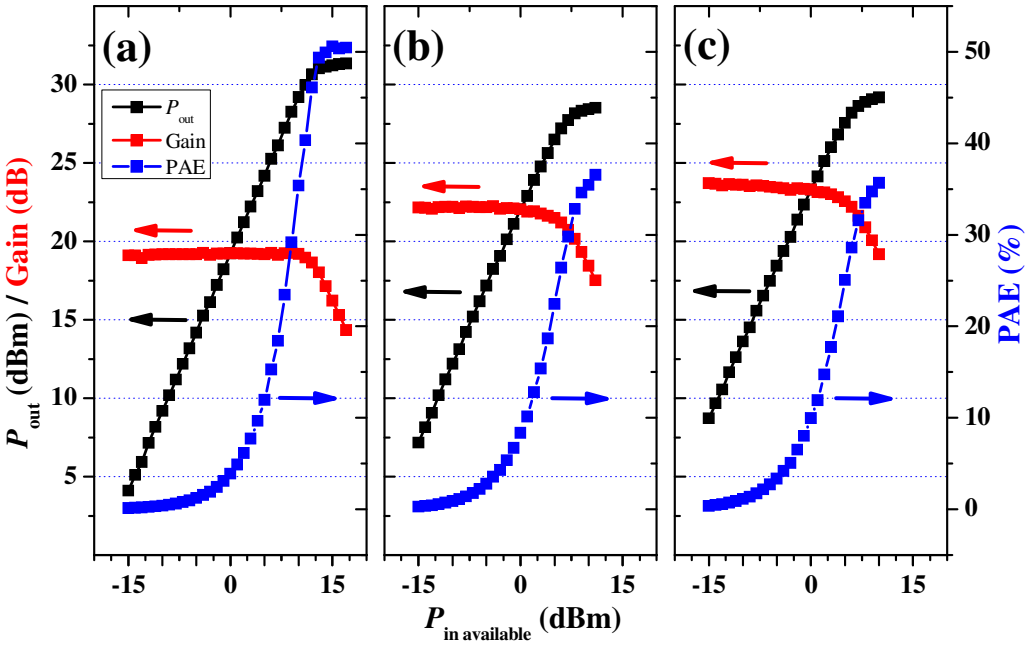


Figure 4.5–5 Load-pull measurements for class AB amplifier for devices with $L_{GD} = 6\ \mu m$, $W_G = 2 \times 125\ \mu m$ and $L_G = 0.7\ \mu m$ (a) GaN buffer layer (b) $Al_{0.05}Ga_{0.95}N$ buffer layer with 15 nm UID GaN channel and (c) $Al_{0.05}Ga_{0.95}N$ buffer layer with 35 nm UID GaN channel. Measured at 2 GHz, $V_{DS} = 28$ V and $I_{out} = 10$ mA.

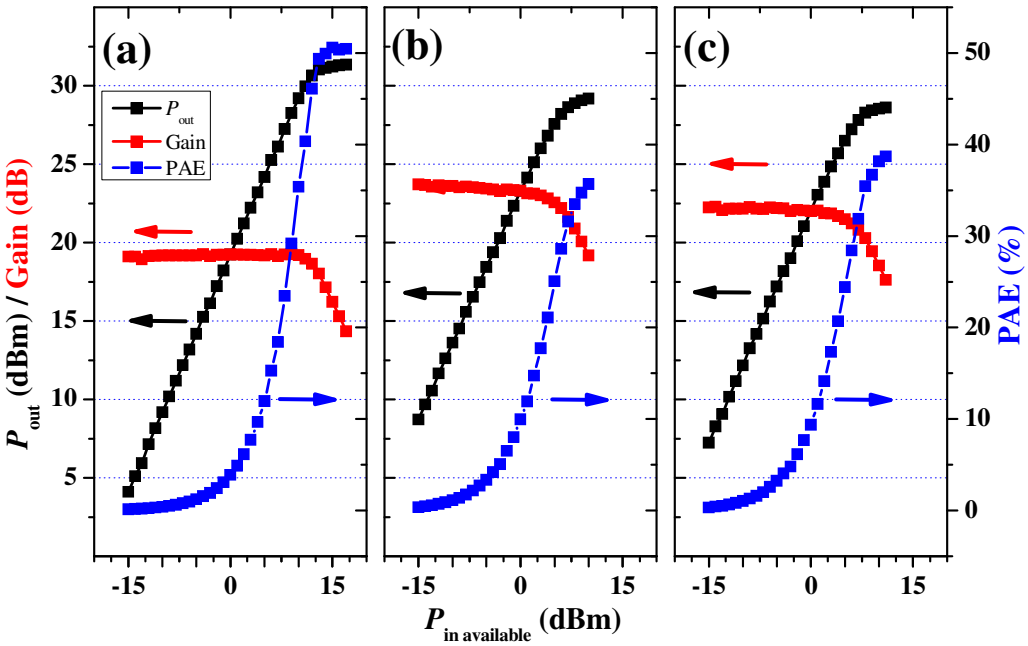


Figure 4.5–6 Load-pull measurements for class AB amplifier for devices with $L_{GD} = 6\ \mu m$, $W_G = 2 \times 125\ \mu m$ and $L_G = 0.7\ \mu m$ (a) GaN buffer layer (b) $Al_{0.05}Ga_{0.95}N$ buffer layer with 35 nm UID GaN channel and (c) $Al_{0.10}Ga_{0.90}N$ buffer layer with 35 nm UID GaN channel. Measured at 2 GHz, $V_{DS} = 28$ V and $I_{out} = 10$ mA.

Layer	GaN buffer			$Al_{0.05}Ga_{0.95}N$			$Al_{0.10}Ga_{0.90}N$		
	P_{out} [W/mm]	PAE [%]	Gain [dB]	P_{out} [W/mm]	PAE [%]	Gain [dB]	P_{out} [W/mm]	PAE [%]	Gain [dB]
GaN buffer	5.4	50.5	14.3	-	-	-	-	-	-
15 nm channel GaN	-	-	-	2.8	36.6	17.5	3.0	42.4	17.8
35 nm channel GaN	-	-	-	3.3	35.7	19.2	2.9	38.7	17.6

Table 4.5–2 Load-pull measured in class AB operation at 2 GHz and V_{GD} = 28 V for DH-HEMT devices (V_{GS} = -0.1 V, I_{DS} = 10 mA) and conventional GaN buffer (V_{GS} = -1.9 V, I_{DS} = 10 mA) devices grown on *n*-SiC substrate.

4.6. Discussion on DH-HEMTs' Experimental Results

The intention of the DH-HEMTs was to increase the device $V_{BR\ OFF}$ by reducing the sub-threshold drain leakage current by preventing the carrier punch-through of the device buffer layer. Simulations show that the sub-threshold drain-leakage current, is due to punch-through in the device buffer layer (Figure 4.2–2(a)). This leakage current is often interpreted as device breakdown since it may fulfill the standard conditions of breakdown measurements. By preventing punch-through in the device the sub-threshold drain leakage current will be reduced and therefore the breakdown of the device will be postponed.

The steep increase of the conduction-band causes a confinement of electrons in the GaN channel (Figure 4.2–1(a) and Figure 4.2–4). Thus the electrons are closer bound to the AlGaN/GaN channel interface and cannot penetrate into the buffer layer, even at higher drain potential (Figure 4.3–3). As a consequence of this a reduced punch-through into the buffer layer in high field conditions (Figure 4.2–2) can be seen, the sub-threshold drain leakage is reduced (examples are shown in Figure 4.3–4, Figure 4.3–8 and Figure 4.3–13) and $V_{BR\ OFF}$ is increased.

A good scaling of $V_{BR\ OFF}$ with the L_{GD} distance is observed in DH-HEMTS while it could not be seen in conventional devices with GaN buffer layer. In the case of the GaN buffer layer, the confinement of the electrons is weak and there is already no barrier towards the buffer layer for low $V_{DS,}$ see Figure 4.6–1(a). Especially if the material properties of the GaN buffer are good, e.g. the trap and defect density is low, any electrons being injected into the buffer layer experience quite a high mobility leading to a low conductive bypass of the space charge region and therefore to a pronounced sub-threshold leakage current. In this case the electron bypass is mainly dependent of buffer material properties, the influence of geometrical device variations such as gate-to-drain distance; L_{GD} is then negligible which results in the observed non-scaling with $L_{GD.}$ In the case of DH-HEMTs, a high potential barrier in the GaN-AlGaN buffer layer interface generated by the band gap difference and the accumulated negative polarization charge, see Figure 4.6–1(b) and Figure 4.6–1(c) prevents punch-through. For short L_{GD}, the influence of V_{DS} on the buffer layer potential barrier is strong, thus; giving a strong scaling between L_{GD} and V_{DS}. As the V_{DS} increases the buffer layer interface potential barrier reduces, as in Figure 4.6–1(b), and finally allows electron flow into the buffer layer resulting in punch-through.

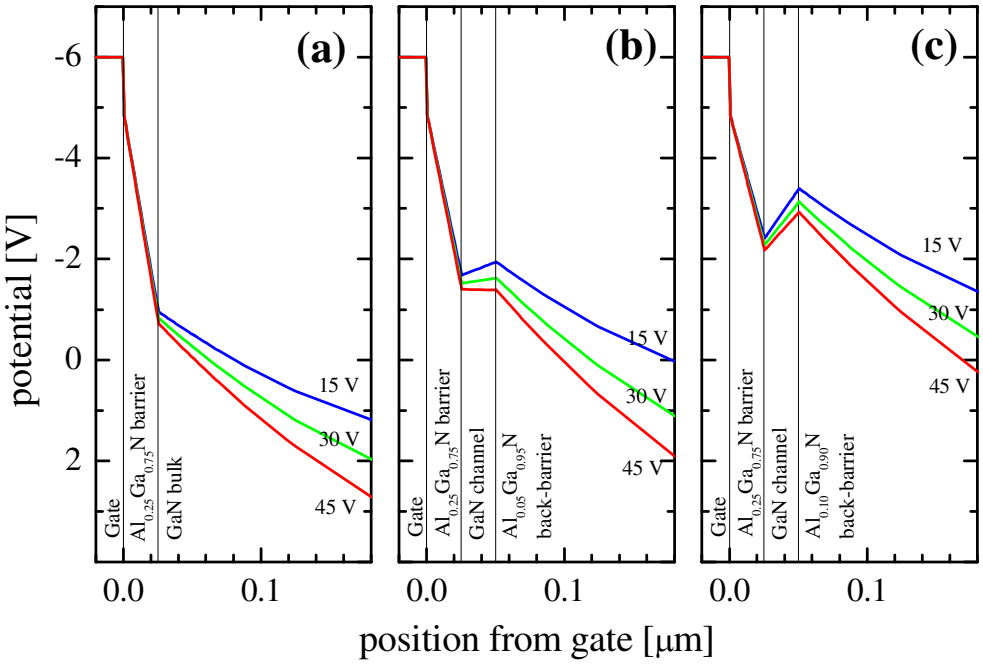


Figure 4.6–1 Potential in a HEMT device cross section of (a) GaN buffer layer (b) $Al_{0.05}Ga_{0.95}N$ buffer layer and (c) $Al_{0.1}Ga_{0.9}N$ buffer layer. Where L_{GD} = 2 µm, V_{GS} = -6 V and V_{DS} = 15 V, 30 V and 45 V.

For large L_{GD}, the impact of a varying V_{DS} on the potential situation at the gate area is smaller. The potential barrier is rather dominated by the gate potential. The scaling between L_{GD} and V_{DS} is then much weaker than in the case of short L_{GD} and eventually saturates for sufficient long L_{GD}. This saturation is confirmed experimentally and is displayed in Figure 4.3–5(a) and (b), Figure 4.3–8 and Figure 4.3–13.

Recess-gate DH-HEMTs (Figure 4.3–5(b)) show a stronger scaling than planar-gate DH-HEMTs (Figure 4.3–5(a)). In the case of gate-recess the influence of the gate fixed potential barrier is larger due to the proximity of the gate to the 2DEG channel and to the buffer layer potential barrier. The impact of V_{DS} on the channel-buffer layer potential-barrier is therefore less than for the un-recessed case. This has two impacts: For short L_{GD}, the scaling is stronger and for large L_{GD} saturation occurs at a higher $V_{BR\ OFF}$ than for planar device. In experiment, the scaling slope for the planar case is 14 V/µm and for the recessed case 22 V/µm according to Figure 4.3–5(a) and Figure 4.3–5(b). The saturated $V_{BR\ OFF}$ is increased by 20 % for the recessed case. For devices grown on *n*-SiC the scaling slope reaches ~60 V/µm according to Figure 4.3–8 and Figure 4.3–13. With the increase of the Al mole fraction *y* in the buffer layer the conduction band barrier towards the buffer layer is increased, thus, at OFF-state conditions the blocking of the sub-threshold drain current more efficient. This explains the experimentally observed increase in $V_{BR\ OFF}$ with the Al concentration in the buffer layer.

Follow the successful demonstration of GaN-based $Al_yGa_{1-y}N$ back-barrier DH-HEMTs on Sapphire substrate a systematic study on DH-HEMTs device grown on 4H-SiC substrates was conducted. 4H-SiC substrates have better thermal conductivity and better lattice mismatch than sapphire substrates. Two types of 4H-SiC substrates were examined, *n*-type 4H-SiC, (*n*-SiC), and Semi-Isolating (SI)-SiC. The *n*-SiC substrates are attractive low cost alternative for SI-SiC substrates for a large scale intensive research and development, although it has significant differences. Through this study the influence of the Al mole fraction, *y*, in the $Al_yGa_{1-y}N$ back-barrier, the UID GaN channel thickness, the Al mole fraction, *x*, in the $Al_xGa_{1-x}N$ top-barrier and the SiC substrate type were deeply investigated.

As in the previous experiment with DH-HEMTs grown sapphire substrates the DC

characteristics of the DH-HEMTs show the same trends when compared to conventional GaN-based HEMTS with UID GaN buffer. GaN-based DH-HEMTs grown on SiC substrates show reduction in $I_{DS\,max}$ and positive shift in V_{Th} and week influence on the R_{ON}. This change is related to the smaller lattice constant determined by the thick AlGaN back-barrier composition. It reduces the mismatch between the UID GaN-channel to the top-barrier and reduces the polarization charge and the 2DEG sheet density. On the other hand it has a strong influence on the confinement of the electrons in the UID GaN channel. The experimental results show that even DH-HEMTs' back barrier with very low Al mole fraction of $y = 0.02$ and very thick UID GaN channel $d_{Ch} = 200$ nm has a strong influence on the device DC performance such as $I_{DS\,max}$, V_{Th} and R_{ON} but low influence on the gate leakage reduction therefore low influence on the $V_{BR\,OFF}$.

As could be learned from the experimental results in addition to the source-drain leakage, also known as punch-through, the Schottky gate reverse bias tunneling-leakage play a significant role in dominating the leakage currents in the subthreshold regime of DH-HEMT devices (insets in Figure 4.3–6, Figure 4.3–12, Figure 4.3–17, Figure 4.3–21 and Figure 4.3–22). This phenomenon could be controlled in adequate design of back-barrier parameters and is well distinguished using the drain-current injection measurement method (as illustrated in Figure 4.3–10, Figure 4.3–15, Figure 4.3–20 and Figure 4.3–24).

A large part of this study was to determine the optimal combination between the Al mole fraction, y, in the $Al_yGa_{1-y}N$ back-barrier and the UID GaN channel thickness, d_{Ch}. From physical-based simulations it could be learned that the back-barrier potential height and its steepness are strongly dependent on both parameters (see example in Figure 4.2–4).

As a major design guideline, it is desired to keep the Al mole fraction, y, in the thick back-barrier as low as possible due to steep reduction in the thermal conductivity with the increase of the Al mole fraction in AlGaN thin films [96]. In addition DH-HEMT devices with lower back-barrier Al mole fraction have higher current density and lower ON-state resistance.

The increase of the channel thickness while holding the Al mole fraction constant increase the back-barrier potential height up to saturation where the conduction band reaches the value of the back-barrier band gap, E_G, farther increase of the channel thickness reduces the steepness of the potential barrier, the gate confinement is limited and the Schottky gate reverse bias tunneling leakage become dominant and lead to premature $V_{BR\,OFF}$ and low scaling ability. On the contrary, too thin UID GaN channel result in low potential barrier, lack of electron back-barrier confinement, decrease of the $I_{DS\,max}$ (see example in Figure 4.3–6) and increase of the ON-stare resistance (see example in Figure 4.3–7) but has a very strong reduction in the Schottky gate reverse bias tunneling leakage that result in breakdown voltage enhancement along with very good scaling ability (see example in Figure 4.3–8). This hypothesis is well confirmed when the devices are measured by the drain-current injection breakdown measurements (Figure 4.3–10 and Figure 4.3–15). It could be seen that the channel confinement increased up to $d_{Ch} \approx 35$ nm there the gate leakage take the domination and increase of the channel thickness show rapid gate leakage and reduction of the gate-drain breakdown voltage.

Similar dependence could be seen for increase of the Al mole fraction at a constant d_{Ch}. Increase of the Al mole fraction while keeping the UID GaN channel thickness constant increases the back-barrier potential height up to saturation where the conduction band reaches the value of the back-barrier band gap, E_G, farther increase of the Al mole fraction result in channel depletion, reduction of the $I_{DS\,max}$ and increase of the ON-stare resistance. But, too low Al content in the back-barrier will not achieve the desired back barrier confinement. Once more, this hypothesis could be well confirmed by drain-current injection breakdown measurements of the devices (Figure 4.3–10 (top) and Figure 4.3–15 (top)).

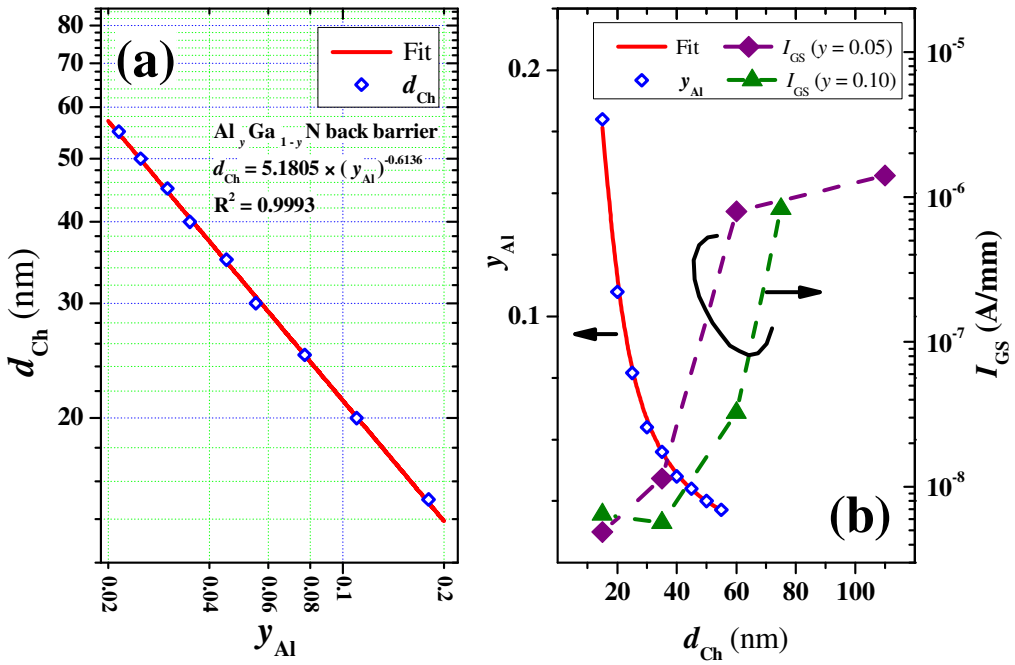


Figure 4.6–2 (a) Calculated (self-consistent coupled Schrödinger Poisson model) optimized UID GaN channel layer thickness as function of the Al mole fraction, y, in the back-barrier. (b) Compared to the Schottky gate reverse bias leakage current for devices with $y = 0.05$ and 0.10 where $L_{GD} = 2$ µm, $L_G = 0.7$ µm, $V_{GS} = -5$ V and $V_{DS} = 10$ V.

Figure 4.6–2(a) shows the optimal dependence of the UID GaN channel thickness, d_{Ch}, as a function on the Al mole fraction, y, in the AlGaN back-barrier. The values were extracted from self consistent coupled Schrödinger-Poisson model calculations of the DH-HEMTs' band structure diagrams (see example in Figure 4.2–4). The dependence is in a power function form $d_{Ch} = a \times y^b$ with correlation parameters a = 5.1805 nm and b = -0.6136 [-]. The optimal thickness was determined as the conduction band reached saturation and could not be increased any more with out reduction of the slope. Figure 4.6–2(b) shows the overlay of the calculated optimal back-barrier with the Schottky gate reverse bias leakage. It could be concluded that for DH-HEMT devices Al mole fraction of 0.05 and UID GaN channel of 35 nm is adequate to suppress the gate leakage and at the same time suppress the source-drain leakage with the high potential back-barrier.

Additional relationship between the Schottky gate reverse bias leakage and the epitaxial structure is the Al mole fraction, x, in the top-barrier. This relationship was not deeply investigated in this work but still has significant influence on the device performance.

The measurements of wafer set-III, shown in Figure 4.3–20, are good examples to distinguish between the two breakdown-mechanisms. For devices with similar breakdown voltage values, wafer "L" and "N", very different characteristics could be seen. The increase of the Al mole fraction, x, in the top-barrier result in increase of the gate leakage but the back-barrier confinement remains the same as in wafer "M", therefore regression in the $V_{BR\ OFF}$ is observed.

Even though SI-SiC and n-SiC substrates lattice properties are apparently very closed to each other and growth of thick buffer on top of them should strongly reduce these differences it is not this way. These differences are not easy to explain and are still under investigation. While conventional GaN-based HEMTs with UID GaN buffer grown on these two types of substrates show similar DC characteristics the DH-HEMTs grown on different types of 4H-SiC substrates show pronounced differences. In general DH-HEMTs grown on n-SiC substrates has lower $I_{DS\ max}$, more positive V_{Th}, higher R_{ON} but significantly lower Schottky gate reverse

bias leakage (see summary in Table 4.5–1, Figure 4.3–21 and Figure 4.3–22). DH-HEMTs grown on SI-SiC substrates also show reduction in the sub-threshold leakage currents but it is limited due to pronounced Schottky gate reverse bias leakage current.

The breakdown voltage measurements emphasize the difference between the two types of devices. While DH-HEMTs grown on *n*-SiC show large enhancement of the breakdown voltage along with the ability to scale it up with the gate drain separation the DH-HEMTs grown on SI-SIC show to certain extent some enhancement of the breakdown voltage but very poor, if at all, ability to scale it up with the gate-drain separation geometry. Drain injection technique support this finding and show very good source-drain confinement (no channel breakdown BV_{DS}^{Ch} could be observed) but a steep increase of the gate current as the channel is closed lead to premature breakdown conditions. One of the ways to overcome the excessive subthreshold leakage currents in DH-HEMTs grown on SI-SiC substrates is the use of field plates as presented in Chapter 6.

An important outcome of the superior confinement of DH-HEMTs is the reduction of the subthreshold currents, especially the Schottky gate reverse bias tunneling leakage, in highly stressed conditions therefore increases the device robustness. The degradation of GaN based HEMTs devices are tightly bonded to the reverse bias gate leakage. Therefore devices such as DH-HEMTs that are characterized with low gate leakage show extremely low degradation in robustness tests.

While the improvement in the device $V_{BR\ OFF}$ characteristics is significant, some price has to be paid: The ON-state resistance is negligibly increased by the presence of the back-barrier heterojunction. It is mainly influenced by the GaN channel thickness [81], [82].

DH-HEMTs on *n*-type SiC substrates biggest advantage is having comparable $R_{ON} \times A$ values to conventional GaN HEMTs while dramatically increasing the $V_{BR\ OFF}$. For thin GaN channel the $R_{ON} \times A$ is higher as compared to conventional GaN HEMTs. If the GaN channel layer thickness increases the $R_{ON} \times A$ get slightly lower.

A pulsed *I-V* measurement (DIVA) is an efficient tool to determine the device efficiency and in many cases it reveals severe problems of the device. Current collapse occurs when hot channel carriers are injected into the buffer under the drift region, where they are trapped at the deep defects sites [101], [102]. In our case, the pulsed measurement shows to some extent very small increase in dispersion and knee walkout for some of the DH-HEMTs devices compared with conventional GaN-based HEMTs that can be associated with immaturity of the AlGaN buffer growth.

The frequency-dependent small signal measurements show a minor dependence of f_T and f_{max} on the epitaxial design. For DH-HEMT devices grown on *n*-SiC substrates a reduction of f_T and f_{max} could be seen but modifications in the UID GaN channel thickness and the Al mole fraction in the back barrier have no influence. On the other hand for DH-HEMT devices grown on SI-SiC substrates no influence on the f_T and f_{max} was observed (see section 6.5.2).

Even though DH-HEMTs are not designed to serve as microwave power amplifiers the RF-characterization from load-pull measurements are taken for additional insight. The introduction of all types of AlGaN back-barrier shows a reduction in the output power density, reduction in the power added efficiency both are associated with the reduction of the thermal conductivity with the increase of the Al mole fraction in the buffer [96]. The phenomenon is more pronounced with the increase of the device gate width. On the other hand and increase of the gain is observed. It is related to the superior channel confinement of DH-HEMT devices.

4.7. Conclusions

A systematic study of GaN based DH-HEMTs with a wide band-gap AlGaN back-barrier layer replacing the traditional GaN buffer layer used in GaN based HEMTs on sapphire, *n*-type 4H-SiC and SI 4H-SiC substrates was conducted. The introduction of an AlGaN back-barrier layer leads to a better confinement of the electrons in the UID GaN channel, accompanied by a reduction in $I_{DS\,max}$ and a positive shift of V_{Th}. Due to large polarization charges in the heterostructures the bands energetic states are strongly dependent on the Al mole fraction in the AlGaN back-barrier and the UID GaN channel thickness. An optimized relationship between the two parameters is calculated and demonstrated experimentally. These parameters of the epitaxial stack strongly influence the electrical characteristics, such as the $I_{DS\,max}$, the V_{Th}, the R_{ON} and the leakage currents of the manufactured device. Already for low maximum Al mole fraction (0.02-0.05) in the back-barrier layer, DH-HEMTs prevent the buffer layer punch-through and reduce the sub-threshold drain-leakage and gate-leakage currents, thus significantly increase the device $V_{BR\,OFF}$. With the increase of the GaN channel thickness the subthreshold Schottky-gate reverse bias tunneling leakage current increases and dominates the sub-threshold leakage current, thus the device OFF-state breakdown voltage then decreases. Well designed DH-HEMTs enable much better scaling of the devices' $V_{BR\,OFF}$ with the gate-drain separation, L_{GD}, than conventional GaN based HEMTs. With the decrease of the GaN channel thickness the device $V_{BR\,OFF}$ scaling saturation appears at higher gate-drain spacing, the saturation voltage level as well as scaling slope increases. DH-HEMTs grown on SI-SiC substrates show inferior $V_{BR\,OFF}$ performance and scaling ability due to more intensive Schottky gate reverse bias tunneling leakage than those who were grown on *n*-SiC. Gate-recess and the use of low Al concentration AlGaN back-barrier layer show synergy in increasing $V_{BR\,OFF}$ and in scaling up.

Time and frequency domain measurements show that DH-HEMTs does not suffer from dispersion and knee-walkout, the epitaxial design has minor effect on both f_T and f_{max}, their microwave gain increase due to superior channel confinement but their power efficiency descend due to low heat dissipation.

GaN based DH-HEMTs are a promising concept for high-voltage device application due to their superior channel confinement, superior OFF-state blocking capability and low gate leakage.

Chapter 5

AlGaN/GaN/GaN:C Back-Barrier HFETs

Systematic study of GaN-based Heterostructures Field Effect Transistors (HFETs) with insulating carbon-doped GaN back-barrier for high voltage operation is presented. Suppression of the OFF-state sub-threshold drain leakage-currents enables breakdown voltage enhancement over 1000 V with low ON-state resistance. The devices with 5 µm gate-drain separation on SI-SiC and 7 µm gate-drain separation on *n*-SiC exhibit 938 V and 0.39 $m\Omega \times cm^2$ and 942 V and 0.39 $m\Omega \times cm^2$ respectively. Power device figure of merit of ~2.3×10^9 $V^2/\Omega \cdot cm^2$ was calculated for these devices. The impacts of variations of carbon doping concentration, GaN channel thickness and substrates are evaluated. Trade-off considerations in ON-state resistance and of current collapse are addressed [104], [105].

5.1. Introduction and Physical Concepts of Carbon Doped *i*-GaN Back-Barrier

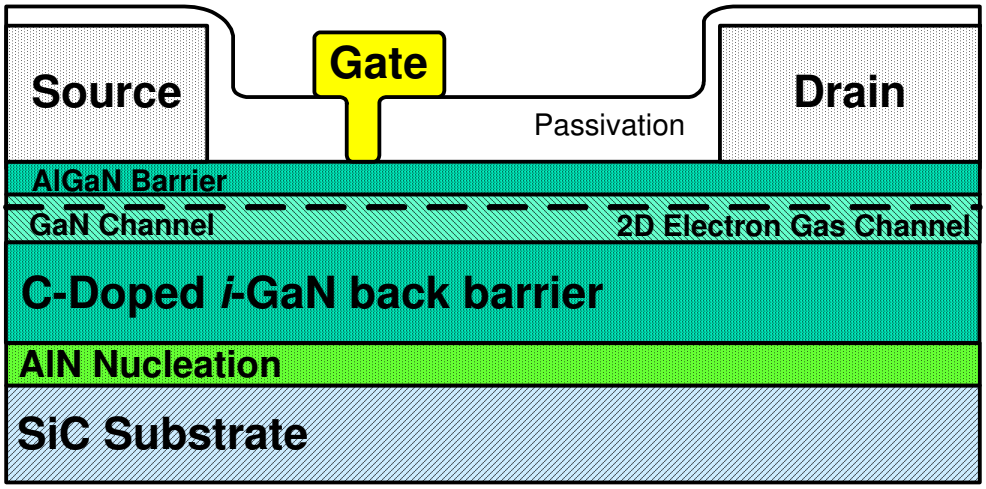


Figure 5.1–1 A planar gate GaN based HEMT structure with carbon-doped *i*-GaN back-barrier.

GaN-Based heterostructures field effect transistors (HFETs), owning properties of high sheet-carrier density and high mobility in the two dimensional electron gas (2DEG) channel and large breakdown field-strength, showed superior performance for high-power switching applications [106] ,[107]. Nevertheless, like other switching devices, the conduction losses in the ON-state resistance (R_{ON}), and the OFF-state breakdown voltage ($V_{BR\ OFF}$) are the main limitations of the power-switch performance of GaN-based HFET switches. Increasing $V_{BR\ OFF}$ while maintaining R_{ON} as low as possible by keeping the gate-drain distance short is, therefore, one of the most important challenges in current developments of GaN-based HFETs for power switching applications. Another important issue for high voltage switching devices is the dynamic ON-state resistance [108] which is related to the device dispersion. The addressed issues are main focus of this chapter.

In many cases, the OFF-state breakdown voltage of a GaN-based HFETs is determined by the sub-threshold drain current at which currents exceeds ~0.1% of $I_{DS\ max}$ or alternatively by the commonly used value of 1 mA/mm. The sub-threshold drain current is mostly dominated by two leakage currents; space charge injection of electrons into the GaN buffer layer i.e. the bulk punch-through [50] and the Schottky-gate reverse bias tunneling leakage current [53], [54]. Suppression of these sub-threshold leakage currents by using high quality insulating buffer layer is essential for realizing sharp current pinch-off, high ON-and OFF-state ratio and would enable enhancement of the device $V_{BR\ OFF}$.

GaN-based HFETs for high-power switching applications often utilize thick unintentionally doped (UID) GaN buffer as a highly-resistive blocking layer. It is desirable to use UID GaN buffer with low defect and low dislocation densities so that the mobility of electrons cannot be degraded by scattering. Low-level residual donors (like oxygen and silicon) [109] are compensated by intrinsic defect states originating from dislocations and point defects ensuring semi-insulating electrical properties.

However, to prevent punch-through currents at higher electric fields a dedicated charge trapping or current blocking in the buffer is mandatory. This can be achieved by either using a heterostructure buffer as demonstrated [79] or by introducing acceptor-like trap states with intentional dopants like iron or carbon [101], [110], [111], [112], [113].

AlGaN/GaN HFETs and GaN based MESFETs utilizing carbon rich GaN to obtain

semi-insulating (SI-) or insulating (*i*-) GaN as device buffer on different types of substrates and epitaxial growth systems were recently investigated by key-playing research groups for power-switching and microwaves applications [101], [110], [111], [112], [113]. Carbon acts as a deep acceptor state with an ionization energy of above 200 meV if incorporated on a substitutional lattice site (C_N) [114]. Carbon is a favorite acceptor-like compensation agent. Unlike iron and magnesium it shows no segregation or memory effects [115] in the growth system and in the device epitaxial stack itself and allows a sharp transition to an UID GaN channel [116]. Carbon-doping is thus one of the favorite choices to enhance $V_{BR\,OFF}$ of power-switching and microwave devices [112], [113], [117], [118].

It has been shown that carbon incorporation in the GaN buffer of HFETs and other field effect devices increases dispersion phenomena (current-collapse and knee-walkout) leading to reduction of the power-switching efficiency, maximum output power and power added efficiency [119] ,[120], [121]. Klein *et al*. showed that the current collapse in GaN based MESFETs and AlGaN/GaN HEMTs is attributed to traps located in the high-resistivity GaN buffer. The incorporated traps causing current collapse were linked to growth pressure in case of the metal organic vapor phase epitaxy (MOVPE) growth which changes the carbon incorporatation considerably.

Other drawbacks known are drastic increase of the device ON-state resistance and reduction of $I_{DS\,max}$ due to the reduction of the sheet carrier concentration as the carbon concentration, [C], in the GaN buffer increases [122]. These problems could be eliminated or at least suppressed by using UID-GaN channel layer and by increasing the vertical spacing between the carbon-rich *i*-GaN buffer and the 2DEG [110], [111], [117], [121].

Although carbon doped semi-insulating buffer layer become more and more in use, to the best of our knowledge, no systematic study on the influence of carbon incorporation in the buffer layer and of UID GaN channel thickness on the sub-threshold leakage effect in GaN HFETs was preformed.

Here, we present such studies considering the variations from wafer to wafer, the variations within wafer along with geometrical variations in the device. The experiments were carried out with GaN based HFETs utilizing carbon-doped *i*-GaN back-barrier grown by MOVPE on SiC substrates which have better thermal conductivity and better lattice mismatch than sapphire substrates. High resistive semi-insulating 4H-SiC (SI-SiC) substrates versus low-cost *n*-type 4H-SiC (*n*-SiC) substrates are compared.

It is shown that the sub-threshold drain-leakage currents are reduced and thus postpone the $V_{BR\,OFF}$ to higher voltages with neither the use of gate insulator nor field plates. The dependences of the device power switching performance and current collapse on the carbon concentration along with the UID GaN channel thickness and the type of substrate is examined. It is also shown that $V_{BR\,OFF}$ scales up sharply with device dimensions (gate to drain separation). To investigate the impact of carbon on current dispersion, the devices were characterized in pulsed along with DC operation mode.

5.2. Process Integration of AlGaN/GaN/GaN:C Back-Barrier HFETs

A cross-section of the fabricated AlGaN/GaN/GaN:C back-barrier devices is illustrated in Figure 5.1–1. For comparison, four types of samples were studied, a conventional AlGaN/GaN HEMT (wafer “A”), and three variations of carbon-doped GaN (GaN:C) back-barrier structures (wafers “B”-“D”), (see summary in Table 5.2–1). The samples were grown by MOVPE on 3-inch SI-SiC substrates, wafers “A”-“C”, and on *n*-SiC substrate, wafer “D”. The carbon doping of the GaN buffer is achieved without an additional carbon source. Details will be published elsewhere in the coming future. For the GaN buffer structure (wafer “A”), a 1.65 µm thick UID GaN was grown. For wafers “B”-“C” a 250 nm thick UID

GaN layer was followed by GaN:C buffer structure. Wafer "B" has GaN:C $1e^{18}$ cm^{-3} buffer and Wafer "C" has GaN:C $4e^{19}$ cm^{-3} buffer. Wafer "D" has 3 µm GaN:C $4e^{19}$ cm^{-3}. An UID GaN channel layer of 35 nm, for wafers "B"-"C", and 100 nm for wafer "D" was grown followed by 25 nm UID AlGaN barrier with Al molar fraction of $x \sim 0.25$.

Layer	Wafer "A"		Wafer "B"		Wafer "C"		Wafer "D"	
FBH wafer number	GSL01-07		GSL01-08		GSL01-09		GSL01-20	
	x	*d* (nm)	*x* / [C]	*d* (nm)	*x* / [C]	*d* (nm)	*x* / [C]	*d* (nm)
Barrier $Al_xGa_{1-x}N$	0.26 *	25	0.25 *	25	0.25 *	25	0.25 *	25
Channel GaN	-	1650	-	**35**	-	**35**	-	**100**
GaN:C Back barrier layer	-	-	**$1e^{18}$ cm^{-3} ****	1500	**$4e^{19}$ cm^{-3} ****	1500	**$4e^{19}$ cm^{-3} ****	3000
GaN Buffer	-	-	-	250	-	250		
Nucleation AlN	-	~50		~50		~50	-	~300
Substrate	SI-SiC		SI-SiC		SI-SiC		*n*-SiC	
Substrate Resistance	-		-		-		0.172 Ω×cm	

"*d* " refers to layer thickness , "*x* " refers to Al mole fraction, [C] refers to carbon concentration.
* Measured by HRXRD.
** Measured by SIMS.

Table 5.2–1 Epitaxy Structure of compared wafers.

Field-effect transistors were fabricated on all wafer types. Ti/Al/Mo/Au based ohmic contacts were formed by e-beam evaporation and annealed at 830°C. Inter-device insulation was made using $^{14}N^+$ multi-energy implantation. The AlGaN barrier was passivated with 150 nm SiN_x. A gate trench in the passivation was defined by i-line optical lithography and subsequently opened by dry etching. Ir/Ti/Au contacts were then evaporated for the gate Schottky metal, followed by a metal liftoff.

The fabricated devices were 2×125 µm and 2×50 µm wide (W_G) with a gate length of 0.7 µm and asymmetrical Γ-gate head of 1.5 µm with 0.2 µm extension towards the source and 0.6 µm extension towards the drain. The source-gate spacing L_{GS} was kept at 1 µm. Wide range of devices with gate-drain spacing L_{GD} varied from 1 µm to 18 µm were tested to evaluate the device ability to scale up the OFF-state breakdown voltage with its gate to drain separation.

5.3. DC Characterization and Measurements

Wafer-level statistical distributions of DC transfer characteristics were measured at $V_{DS} = 10$ V for devices fabricated on wafer "A"-"D" and the results are shown in Figure 5.3–1. The devices' key DC measurements parameters are summarized in Table 5.3–1. The reduction of the $I_{DS\,max}$ and positive shift of the threshold bias, V_{Th}, with the increase of the carbon concentration, carbon concentration, in the back-barrier is observed in wafers "A"-"C". While keeping the carbon concentration high in the GaN buffer ($4e^{19}$ cm^{-3}) and widening the UID GaN channel from 35 nm to 100 nm, the $I_{DS\,max}$ increases and the V_{Th} becomes more negative as can be seen in wafer "D". Careful look in the sub-threshold regime, in Figure 5.3–1 inset, reveals more; the sub-threshold drain leakage current at ~V_{Th}-0.5 V is more than 3 orders of magnitude lower in wafer "C, with the GaN:C back-barrier, compared to wafer "A", GaN buffer. This current is originated by the reverse bias Schottky contact of the gate [55] and in many cases is the cause of premature OFF-state breakdown of the device. The increase of reverse bias Schottky leakage current is observed with the reduction of the carbon concentration in the GaN:C back-barrier, wafer "B", and/or the increase of the

thickness of the UID GaN channel, wafer “D”.

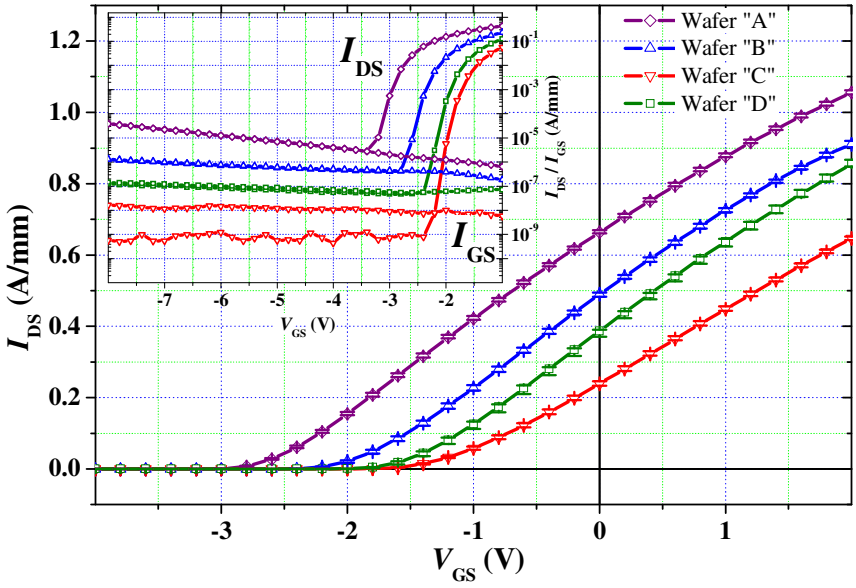


Figure 5.3–1 Wafer-level median transfer characteristics of $W_G = 2 \times 50$ µm $L_{GD} = 2$ µm devices with GaN buffer and GaN:C back-barrier devices measured at $V_{DS} = 10$ V. (Error bars are 25% and 75% percentiles). Inset: log scale of the sub-threshold regime.

	Wafer “A”	Wafer “B”	Wafer “C”	Wafer “D”
FBH wafer number	GSL01-07	GSL01-08	GSL01-09	GSL01-20
UID GaN channel thickness d_{Ch}	GaN buffer	35 nm	35 nm	100 nm
V_{Th} (V)	-2.91	-2.50	-1.96	-2.15
$I_{DS\,max}$ (V_{GS} = +2V) (A/mm)	1.06	0.91	0.65	0.86
$V_{BR\,OFF}$ (2 ×50 µm, L_{GD} =2 µm) (V)	26(±4)	56(±4)	349(±4)	251(±6)
R_{ON} (Ω·mm)	2.08	2.51	3.35	2.08
$I_{GS\,leak}$ ($V_{GS} = V_{Th}$-1.0 V) (A/mm)	1.30×10^{-5}	4.72×10^{-7}	8.82×10^{-9}	5.92×10^{-8}
$I_{DS\,leak}$ ($V_{GS} = V_{Th}$-1.0 V) (A/mm)	1.29×10^{-5}	4.45×10^{-7}	7.33×10^{-10}	4.77×10^{-8}
$g_{m\,max}$ (mS/mm)	272	264	211	265
Substrate	SI-SIC			*n*-SiC

Table 5.3–1 DC measurements parameters summary of inline monitoring 2 × 50 µm A2 devices, $L_{GD} = 2$ µm and $L_G = 0.7$ µm for compared wafers.

The breakdown voltage $V_{BR\,OFF}$ of the devices was measured at OFF-state conditions below the device threshold bias $V_{Th} >> V_{GS} = -5$ V. During the $V_{BR\,OFF}$ measurements, the devices were immersed in 3M™ Fluorinert™ Electronic Liquid FC-3283 [123] in order to avoid arcing through the air. The drain bias was increased in steps of 2 V and logged until breakdown was identified. The breakdown voltage was defined as the voltage at which the drain current exceeds the value of 1 mA/mm. The voltage limit of the measurement system is +/-1000 V. The wafers were placed on a floating stage during the measurement. Figure 5.3–2 shows the results of sub-threshold drain-leakage current measurements for wafer “C” with $L_{GD} = 1$ µm to 10 µm. The results show overall very low background sub-threshold drain leakage current, ~10^{-7} A/mm. Depending on the gate drain spacing, the current increases rapidly at different $V_{BR\,OFF}$. It could be seen that the profile of the current is very uniform and the breakdown voltage is dependent on nothing but the lateral spacing. It could also be seen that for devices with $L_{GD} \geq 6$ µm breakdown of the device could not be observed in the existing measurement system and lays above 1000 V.

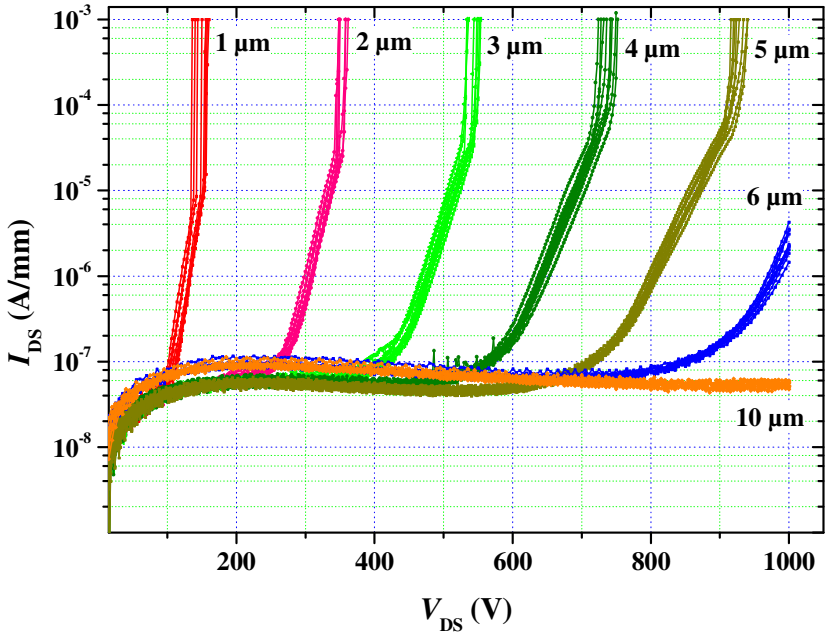


Figure 5.3–2 Drain current output during $V_{BR\ OFF}$ measurements for HFET devices on wafer "C" with GaN:C $4e^{19}$ cm^{-3} back-barrier on SI-SiC substrate with different gate drain spacing L_{GD} and $W_G = 2 \times 125$ µm. The measurement is limited by the current compliance of 1 mA/mm and drain bias V_{DS} = 1000 V measured at V_{GS} = -5 V.

Typical three-terminal drain current injection OFF-state breakdown voltage measurements for devices from all types of wafers are presented in Figure 5.3–3 [52]. The tested devices are 2 × 50 µm wide with L_{GD} = 2 µm and the injected drain current is I_{DS} = 1 mA/mm.

The introduction of carbon doped back-barrier to the devices show also in this measurement technique enhancement of the $V_{BR\ OFF}$ for wafers "B" to "D". Wafer "A" with low [C] in the back-barrier show a unique breakdown characteristics, here the channel break, BV_{DS}^{Ch}, in a relatively low bias follows by a sluggish increase of the gate current. The slow increase of the drain bias indicate that even though a improvement in the buffer confinement achieved with respect to conventional UID GaN buffer it is the dominant mechanism of the device breakdown, but a better prevention of the gate reverse bias leakage could be seen. As the [C] increases in wafers "C" and "D" the breakdown voltage of the devices increases. For devices with high [C] back barrier no channel breakdown, BV_{DS}^{Ch}, but only the gate-drain breakdown, BV_{DS}^{G} and BV_{DG}, could be observed. This property is an indication for a strong buffer confinement which also appears in Si JFETs that are known for their superior channel confinement. The increase of the UID GaN channel thickness d_{Ch}, is associated with reduction of the gate-drain breakdown values, BV_{DS}^{G} and BV_{DG}.

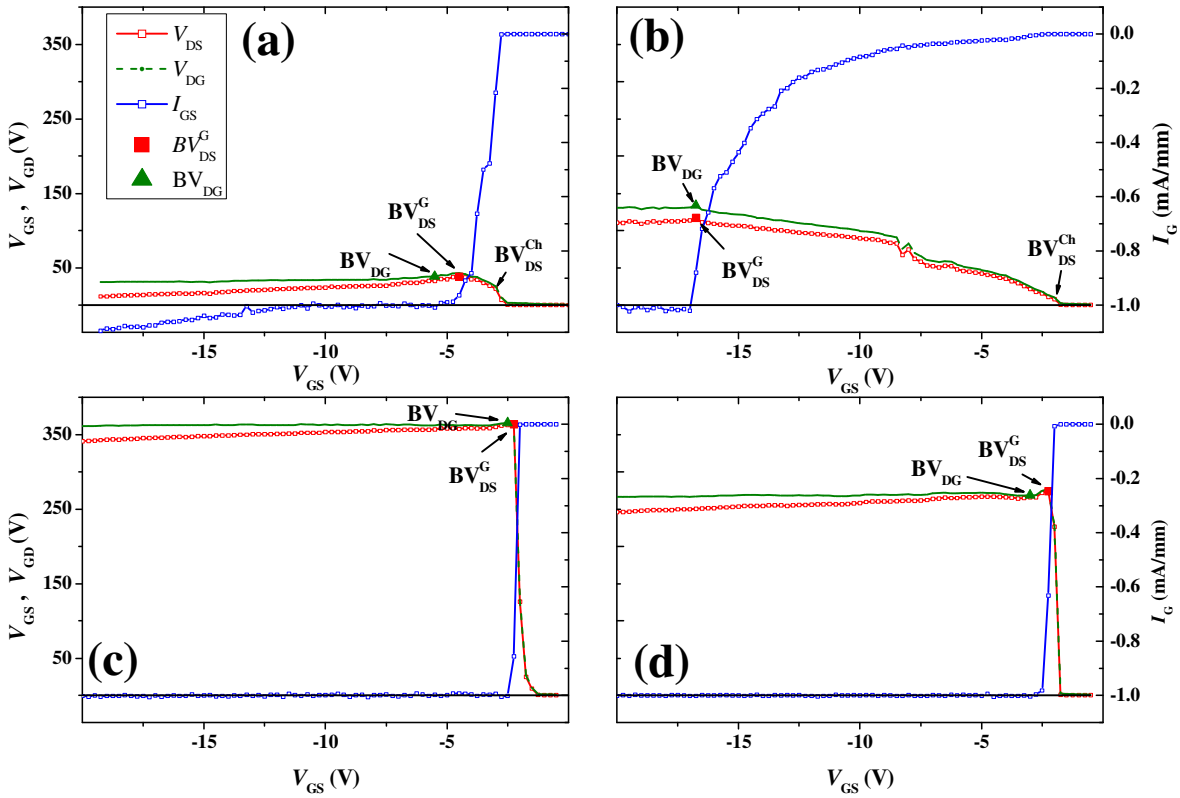


Figure 5.3–3 Drain Three-terminal drain current injection-technique to measure $V_{BR\ OFF}$ for devices on (a) wafer "A" with conventional GaN buffer, (b) wafer "B", (c) wafer "C" and (d) wafer "D" with GaN:C back-barrier devices on SI-SiC and *n*-SiC substrates. Devices' gate drain spacing is $L_{GD} = 2$ µm and 2×50 µm A2 measured at $I_{DS} = 1$ mA/mm injection current.

Wafer-level statistical analysis of the breakdown voltage measurements for increasing gate-drain spacing, L_{GD}, on all types of wafers is shown in Figure 5.3–4. For wafer "A" with the GaN buffer, a median of ~45 V was measured. Neither the median nor the distributions of the devices breakdown voltage are influenced by gate drain spacing. Wafer "B" with the low carbon concentration back-barrier show increase of the $V_{BR\ OFF}$ from median value of 52 V up to $L_{GD} = 3$ µm with slope of 30 V/µm and settles around ~110 V. Dramatic increase of the breakdown voltage in several hundreds of volts for devices on wafer "C" is observed with median $V_{BR\ OFF}$ of 930 V for device with $L_{GD} = 5$ µm and median slope of 194 V/µm.

Wafer "D", which was grown on *n*-SiC substrate with a 100 nm UID GaN cannel, also shows very good improvement in the $V_{BR\ OFF}$. For devices with $L_{GD} = 7$ µm a maximum value of $V_{BR\ OFF} = 942$ V was achieved. It could also be seen that for devices with $L_{GD} \geq 15$ µm breakdown of the device could not be achieved in the existing measurement system and lays above 1000 V. In contrast to wafer "C", the measured data scatter more widely for devices larger than 3 µm and two slopes are identified. The maximum increase of $V_{BR\ OFF}$ with gate drain spacing is 133 V/µm but the median slope is only 65 V/µm.

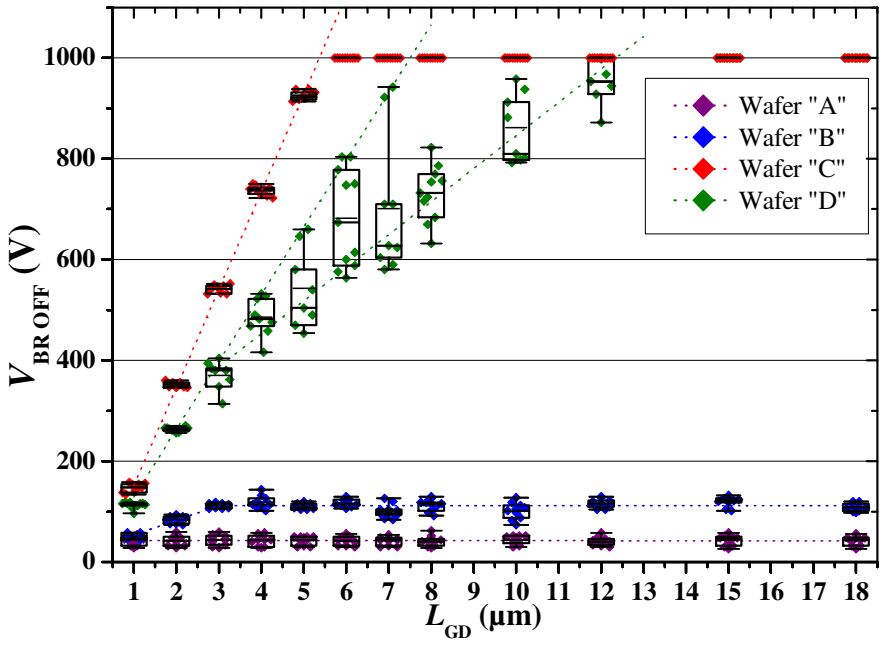


Figure 5.3–4 Wafer-level distribution of breakdown voltage for devices with gate-drain spacing of L_{GD} = 1 µm to L_{GD} = 18 µm and W_G = 2 × 125 µm. dotted line is a linear fit of the measurement median. The center line is the population median, box top/bottom lines are 25% and 75% percentiles and top/bottom lines are minimum and maximum.

While demonstrating a tremendous improvement in the breakdown voltage, the price in the specific ON-state resistance, $R_{ON} \times A$, is minimal. Here, the $R_{ON} \times A$ is defined as the reciprocal of the *I-V* curve's slope at V_{GS} = +2 V and I_{GS} compliance of 200 mA/mm at the steepest position multiplied by the device active area, *A*. The Active area for lateral structures defined $A = (L_{GS} + L_G + L_{GD}) \times W_G$. As shown in Figure 5.3–5, the introduction of carbon into the devices' buffer as back-barrier contributes very little to increase the ON-state resistance. For example: when comparing devices with L_{GD} = 5 µm; additional median resistance of ~ 0.08 mΩ × cm^2 and ~ 0.16 mΩ × cm^2 for wafers "B" and "C" is measured respectively. On the other hand wafer "D" owning high carbon concentration GaN:C back-barrier and 100 nm UID channel is equivalent in median and variance to wafer "A".

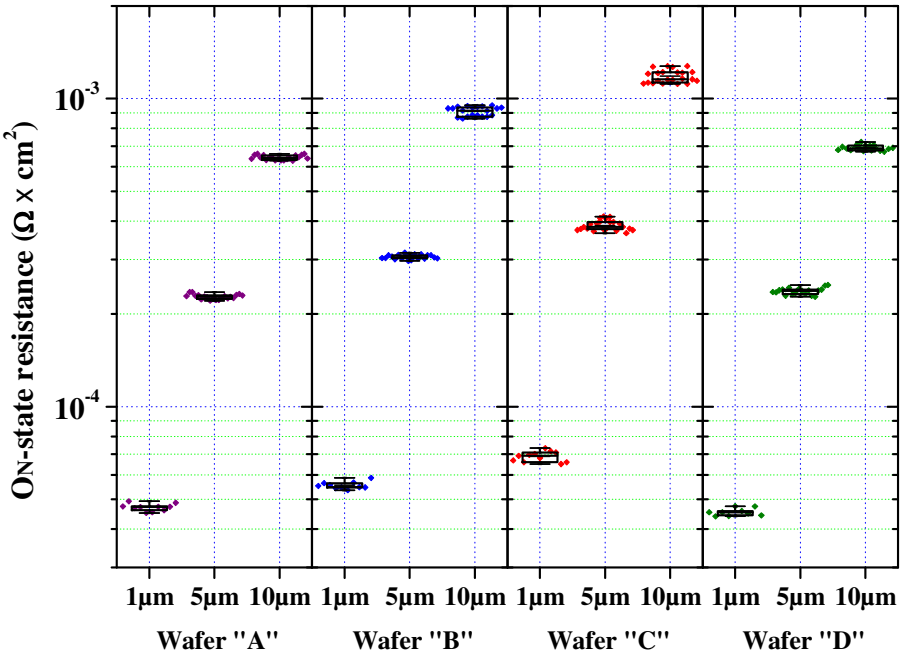


Figure 5.3–5 Wafer-level distribution of ON-state resistance ($R_{ON} \times A$) measured at V_{GS} = +2 V for devices with gate-drain spacing of L_{GD} = 1 µm, 5µm and 10 µm and W_G = 2 × 125 µm. The center line is the population median, box top/bottom lines are 25% and 75% percentiles and top/bottom lines are minimum and maximum.

In lateral devices, high OFF-state breakdown voltage requires a very good vertical electrical insulation. In addition to the device buffer confinement, the substrate insulation at high voltages plays an important role. Substrate breakdown of the described wafers was measured by biasing an 80 µm × 80 µm ohmic contact pad on the processed wafer surface while the bottom of the wafer substrate was electrically grounded. The voltage and current compliance are 1 mA and 1000 V, respectively. Figure 5.3–6 brings the results of wafer-level vertical measurement of the wafers' substrates breakdown characteristics. In contrast to the very low substrate leakage current of the SI-SiC wafers (wafer "C" does not exceed 10^{-8} A at 1000 V and wafer "A" does not exceed 10^{-7} A at 1000 V) the *n*-SiC wafer shows rapid and uniformly increase of the current and reaches the limit of 1 mA at ~550 V.

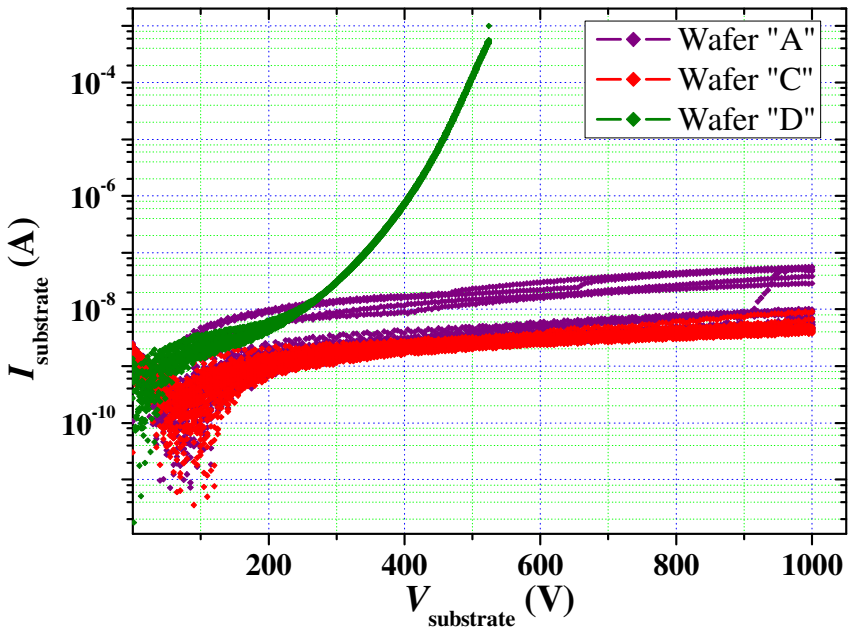


Figure 5.3–6 Wafer-level measurement of substrate breakdown voltage of different substrate types *n*-SiC and SI-SiC with epitaxy GaN:C $4e^{19}$ cm^{-3} back-barrier layer and UID GaN buffer. Measurements limited in current by 1 mA and in potential by 1000 V.

5.4. Dynamic Pulsed *I-V* (DIVA) Measurements

Representative example of 200 ns dynamic pulsed *I-V* (DIVA) measurements for devices on all wafers types is shown in Figure 5.4–1(a)-(d). DIVA pulsed measurement is a very good on-wafer dynamic method to evaluate the device current collapse without the use of complicated impedance-matching-circuits as used by Saito *et al.* [108], in addition it minimize the influence of burn-in degradation effect. The pulsed measurements were done at two quiescent bias points; [V_{GS} = 0 V, V_{DS} = 0 V], to minimize the effect of reduction of mobility due to low heat removal rates and the effect of slow traps [103] and at [V_{GS} |(I_{DS}= 10 mA), V_{DS} = 30 V] to emphasize the drain current lag at class AB operation conditions. V_{GS} |(I_{DS}= 10 mA) was -3.1 V, -1.9 V, -0.8 V and -1.25 V for devices on wafer "A", "B", "C", and "D" respectively.

As shown in Figure 5.4–1(a)-(d) no observable gate lag in any of the wafers could be seen when pulsing from quiescent bias point [V_{GS} = 0 V, V_{DS} = 0 V]. Some increase of the drain current lag and knee-walkout of the V_{GS} = +2 V branch could be observed in all types of wafers with GaN:C back-barrier at the demanding operation condition, quiescent bias point of [V_{GS} |(I_{DS}= 10 mA), V_{DS} = 30 V]. More significant drain current lag was observed with wafer "C" than others.

Figure 5.4–1(e) summarizes the current lag parameter for the different wafers with different GaN:C back-barrier devices. Here, the drain current lag, *L* (%), is defined by:

$$L(\%) = \frac{\Delta I_{\text{DS dyn}}}{I_{\text{DS dyn}}\big|_{(V_{GS}=0\text{V},V_{DS}=0\text{V})}} \times 100\% \Bigg|_{(V_{GS}=+1\text{V},V_{DS}=10\text{V})} \qquad 5\text{–}1$$

$$\Delta I_{\text{DS dyn}} = I_{\text{DS dyn}}\big|_{(V_{GS}=0\text{ V},V_{DS}=0\text{ V})} - I_{\text{DS dyn}}\Big|_{\left(V_{GS}\,|_{(I_{DS}=100\text{ mA / mm})},V_{DS}=30\text{ V}\right)} \qquad 5\text{–}2$$

where $I_{\text{DS dyn}}\big|_{(V_{GS}=0\text{V},V_{DS}=0\text{V})}$ is the drain current measured in dynamic pulsed conditions with

quiescent bias point $V_{GS} = 0$ V and $V_{DS} = 0$ V, $I_{DS\,dyn}\Big|_{\left((V_{GS}|_{(I_{DS}=10\,mA)}, V_{DS}=30\,V\right)}$ is the drain current measured by the pulsed measurements with quiescent bias point of V_{GS} that gives $I_{DS} = 10$ mA in DC and $V_{DS} = 30$ V, both measured when $V_{GS} = +1$ V and $V_{DS} = 10$ V.

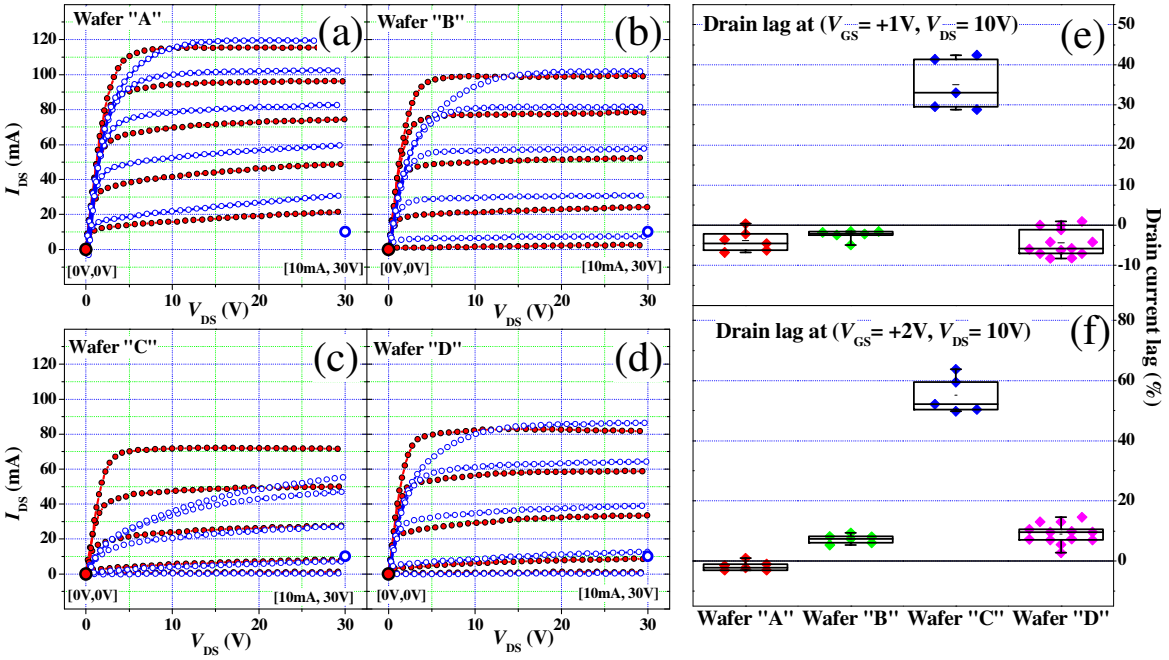


Figure 5.4–1 (a)-(d) 200 ns pulsed *I-V* (DIVA) measurements for the devices with 2 × 50 µm and gate-drain spacing of $L_{GD} = 2$ µm on wafer "A"-"D". $V_{GS\,max} = +2$ V and $\Delta V_{GS} = 1$ V. DIVA quiescent points $V_{GS} = 0$ V, $V_{DS} = 0$ V (solid red dot) and $I_{DS} = 10$ mA, $V_{DS} = 30$ V (empty blue dot). Wafer-level drain current lag parameter distribution for the different type of wafers. (e) Drain lag from $V_{GS} = +1$ V branch at $V_{DS} = 10$V, (f) Drain lag from $V_{GS} = +2$ V branch at $V_{DS} = 10$V.

For manufactured devices the median current lag is; on a wafer "A" –4%, on a wafer "B" –2%, on wafer "C" 33% and on wafer "D" –6%. There is no significant difference among wafers except wafer "C". To emphasize more the drain knee-walkout phenomena, Figure 5.4–1(f) summarizes the current lag parameter of the wafers for the $V_{GS} = +2$ V branch. For manufactured devices the median current lag is; on a wafer "A" –2%, on a wafer "B" 8%, on wafer "C" 52% and on wafer "D" 10%. From statistical point of view, wafers "B" and "D" show very similar behavior.

5.5. Discussion

In this work, several hundred volts of OFF-state breakdown voltage enhancement in GaN based HEMTs was obtained by employing GaN:C back-barrier. Sub-threshold drain and gate leakage currents suppression led to $V_{BR\,OFF}$ enhancement.

As mentioned previously, the sub-threshold drain leakage current composed mainly from two independent sources, the source leakage that appears as buffer punch-through and the Schottky-gate-reverse-bias tunneling leakage. Therefore, suppression of both punch-through leakage and gate-tunneling-leakage is essential to enhance the OFF-state breakdown voltage. The drain-source leakage is dominated by the magnitude of the punch-through effect and could be suppressed by the device's buffer modification such as using carbon doped GaN back-barrier. The Schottky-gate-tunneling-leakage is dominated by the electrical field under the drain side of the gate and could be suppressed by reduction and/or spreading of this field.

However, this work and our previous paper show that an introduction of a back-barrier in HEMTs can also enhance $V_{BR\ OFF}$, by reducing the electrical field under the drain-side of the gate [79].

Devices with GaN:C back-barrier in OFF-state conditions, where $V_{GS} << V_{Th}$, show reduction of the sub-threshold current. This indicates strong reduction in the gate reverse bias leakage which is a large contributor for limited $V_{BR\ OFF}$. This sub-threshold current is suppressed by several orders of magnitude by increasing the carbon concentration in the GaN:C back-carrier while keeping the UID GaN-channel thickness constant. The reverse bias leakage current depends on the thickness of UID GaN-channel. Slight increase of the reverse bias leakage current to almost 10^{-7} A/mm was observed as the UID GaN-channel becomes thicker, 100 nm, with constant carbon concentration.

The $V_{BR\ OFF}$ measurements *I-V* monitoring shows that the GaN:C back-barrier suppresses the sub-threshold leakage currents originated from both, gate and source. Suppression of the sub-threshold leakage currents below 10^{-7} A/mm in OFF-state conditions enhances the device breakdown voltage in hundreds of volts. The suppression of the sub-threshold leakage currents is dependent on the carbon concentration in the GaN:C back-barrier and the UID GaN channel thickness.

As carbon concentration in the GaN:C back-barrier increases while keeping the UID GaN channel thickness constant, a reduction of $I_{DS\ max}$ and a positive V_{Th} shift were observed. Both indicate that the electron-gas channel volume is narrowed. On the other hand, when the thickness of UID GaN channel thickness is increased while keeping the carbon concentration in the GaN:C back-barrier constant, the $I_{DS\ max}$ becomes higher and V_{Th} shifts to more negative bias, i.e. the volume of 2DEG increases.

Scaling the $V_{BR\ OFF}$ with the device dimensions is possible for devices with GaN:C back-barrier. The scaling slope depends on the carbon concentration in the GaN:C back-barrier and the UID GaN channel thickness.

The substrate vertical leakage in devices fabricated on *n*-SiC substrates become dominant in the device breakdown characteristics. While devices on *n*-SiC with low dimensions show good uniformity, devices on SI-SiC devices with $L_{GD} \geq 3$ µm show increasing variation in $V_{BR\ OFF}$. The $V_{BR\ OFF}$ populations of devices manufactured on *n*-SiC show two scaling trends: maximal increasing slope and nominal increasing slope. The variation in $V_{BR\ OFF}$ is originated from the vertical substrate leakage. Carbon doping in the GaN buffer can suppress and reduce substrate vertical leakage at high voltages although the substrate leakage still limits the $V_{BR\ OFF}$ for some devices with $L_{GD} \geq 3$ µm.

While the improvement in the device breakdown characteristics is significant, some price has to be paid: The specific ON-state resistances, $R_{ON} \times A$, increases with carbon concentration in the GaN:C back-barrier for devices with thin, $d = 35$ nm, UID GaN-channel. While keeping the carbon concentration in the GaN:C back-barrier high and increasing the UID GaN channel thickness to $d = 100$ nm the $R_{ON} \times A$ values return to be matched to $R_{ON} \times A$ in devices with conventional GaN buffer. A similar phenomenon was observed in devices owning an AlGaN back-barrier [81].

A pulsed *I-V* measurement (DIVA) is an efficient tool to determine the device efficiency and in many cases it reveals severe current collapse problems in the device. DIVA measurements show absence of gate lag for all devices from quiescent point [0, 0]. Drain-lag factor is used to quantify the current collapse phenomenon. Commonly the $V_{GS} = +1$ V branch is used for the calculation. In this branch, the drain lag factor is equivalent for wafers "A", "B" and "D". The drain lag knee walk-out is more visible with the increase of the carbon concentration in the GaN:C back barrier while keeping the thickness of the UID GaN cannel constant. (Comparing wafers "A", "B" and "C"). While keeping the carbon concentration in the GaN:C back-barrier high and constant and increasing the UID GaN channel thickness from 35 nm to 100 nm, the drain lag knee and walk-out decrease and the lag parameter is equivalent to the one in conventional GaN HFET with UID GaN buffer. More pronounced

drain lag knee walk-out could be seen for the V_{GS} = +2 V branch. For this *I-V* branch, the evaluated lag parameter is about 10 % higher for wafers "B" and "D" compared to wafer "A" with the conventional UID GaN buffer.

The specific ON-state resistances, $R_{ON} \times A$, versus the breakdown voltage, $V_{BR\ OFF}$, of the manufactured devices with GaN:C back barrier wafer "C" and wafer "D" are compared in Figure 5.5–1(a). Devices on both wafers exceed the 6H-SiC theoretical limit for devices with $L_{GD} \geq 5$ µm and $L_{GD} \geq 7$ µm respectively. These devices have a power figure of merit of ~2.3×10^9 V^2/Ω·cm^2. To the best of our knowledge these values are the highest reported value. For the low dimensions, the specific ON-state resistance is dominated by the ohmic contacts resistance. The $R_{ON} \times A$ versus the $V_{BR\ OFF}$, of the manufactured devices with GaN:C back-barrier wafer "C" are compared to the state-of-the-art GaN based devices in Figure 5.5–1(b). The devices are best in class with low $R_{ON} \times A$ values and exceed the 6H-SiC limit. The doted line is the correlation fit of the $V_{BR\ OFF}$ to the median $R_{ON} \times A$ measurements with the increase of the device dimensions:

$$R_{ON}\left(\Omega \cdot \mathrm{cm}^2\right) = 5.25 \times 10^{-5} + 4.34 \times 10^{-9}\, \mathrm{V}_{BR\ OFF}^{1.65} \qquad 5\text{–}3$$

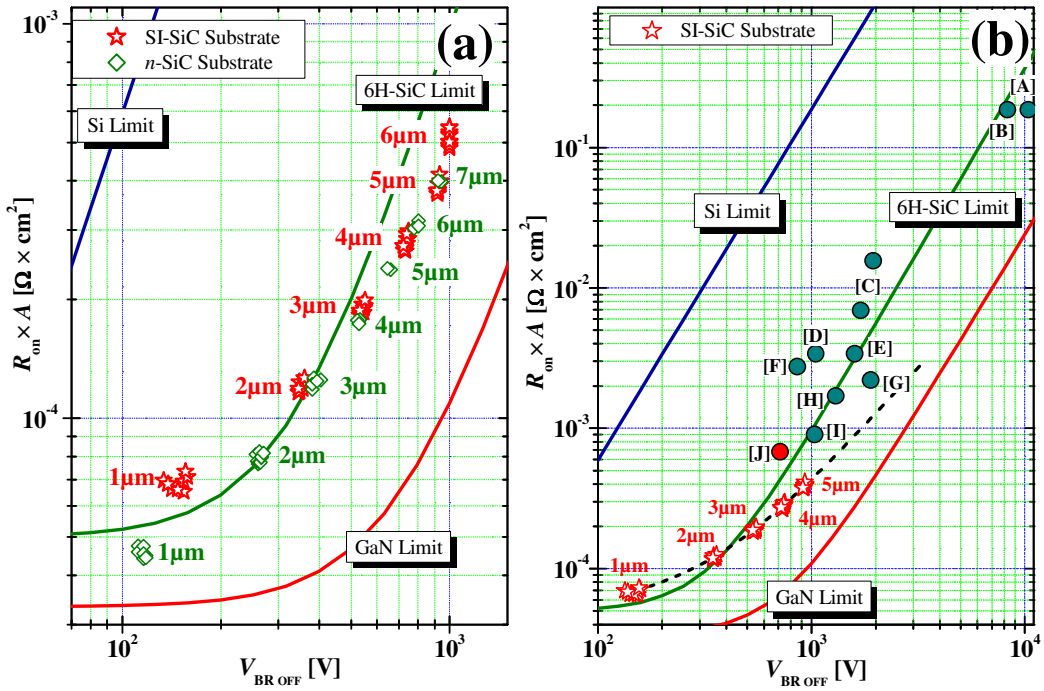


Figure 5.5–1 (a) Breakdown voltage vs. $R_{ON} \times A$ of the fabricated HEMTs with GaN:C on SI-SiC (wafer "C") and on *n*-SiC (wafer "D") substrates. The carbon concentration in both wafers is 4e^{19} cm^{-3}. (b) Breakdown voltage vs. $R_{ON} \times A$ of the fabricated DH-HEMTs with GaN:C 4e^{19} cm^{-3} back-barrier on SI-SiC (wafer "C") compared with those of the state-of-the-art GaN based devices. The doted line corresponds to Eq. 5–3.

Points	Year	Group	Technology	$R_{ON} \times A$ (Ω·cm^2)	$V_{BR\ OFF}$ (V)
A	2009	Uemoto *et al.* [124]	GaN HEMT	0.186	10400
B	2007	Uemoto *et al.* [125]	GaN HEMT	0.186	8300
C	2006	Yagi *et al.* [10]	GaN HEMT	0.0069	1700
D	2001	Zhang *et al.* [8]	GaN HEMT	0.0034	1050
E	2006	Tipirneni *et al.* [9]	GaN HEMT	0.0034	1600
F	2004	Huili *et al.* [5]	GaN HEMT	0.0028	860
G	2006	Dora *et al.* [13]	GaN HEMT	0.0022	1900
H	2002	Zhang *et al.* [7]	GaN HEMT	0.0017	1300
I	2009	Shi *et al.* [126]	GaN HEMT	0.0009	1035
J	2010	Bahat-Treidel *et al.* [127]	GaN HEMT	0.00068	714

Table 5.5–1 OFF-state breakdown voltage, $V_{BR\ OFF}$ vs. $R_{ON} \times A$ data.

5.6. Conclusions

A systematic study of AlGaN/GaN/GaN:C back-barrier HFETs on SI-SiC and *n*-SiC substrates was carried out. The introduction of a GaN:C back-barrier layer leads to a better confinement of the electrons in the GaN channel, although it accompanied by a reduction in $I_{DS\,max}$ and an increase of V_{Th}. The GaN:C back-barrier layer suppresses the sub-threshold drain currents, source-drain leakage and gate leakage, therefore enhances the device $V_{BR\,OFF}$ by hundreds of volts. The devices demonstrated excellent scaling of the $V_{BR\,OFF}$ with their geometry. Devices fabricated on *n*-SiC substrates suffered from pronounced vertical leakage that limited the device $V_{BR\,OFF}$ uniformity across the wafer. Trade-off in ON-state resistance, due to channel confinement was observed. The increase of lag factor was observed due to proximity of the GaN:C layer to the 2DEG. Both issues were improved with vertical separation of the GaN:C from the 2DEG by controlling the thickness of UID channel. The presented devices on both, SI-SiC and *n*-SiC substrates, own record high power figure of merit and exceed the 6H-SiC theoretical material power limit.

Chapter 6

Study and Analysis of Multiple Grating Field Plates (MGFP) in AlGaN/GaN HEMTs

GaN-based High Electron Mobility Transistors (HEMTs) with planar multiple grating field plates (MGFPs) for high voltage operation are described. A synergy effect with additional electron channel confinement by using a heterojunction AlGaN back-barrier is demonstrated. Suppression of the OFF-state sub-threshold gate and drain leakage-currents enables breakdown voltage enhancement over 700 V and low ON-state resistance of 0.68 $m\Omega \times cm^2$. Such devices have a minor trade-off in ON-state resistance, lag factor, maximum oscillation frequency and cut-off frequency. Systematic study of the MGFP design and the effect of Al composition in the back-barrier are described. Physics based device simulation results give insight into electric field distribution and charge carrier concentration depending on field plate design [127].

6.1. Introduction and Physical Concepts of MGFPs

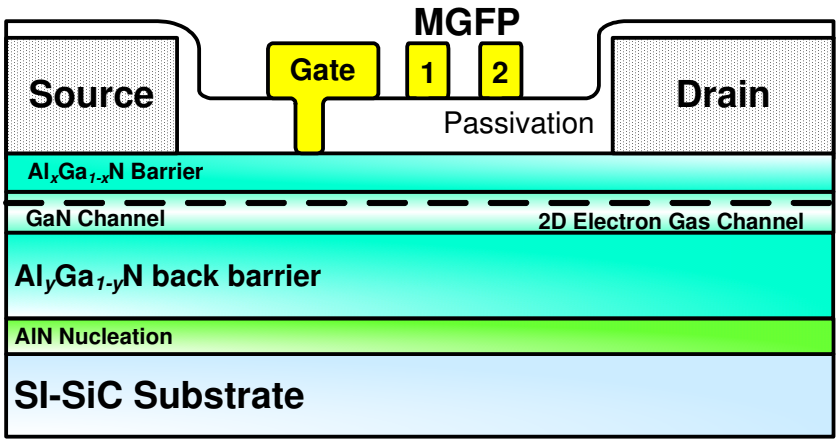


Figure 6.1–1 A planar gate GaN based DH HEMT structure with Multiple Grating Field Plates (MGFPs).

GaN-based High Electron Mobility Transistors (HEMTs) already show excellent performance for high-power switching applications due to their high sheet-carrier density in the two dimensional electron gas (2DEG) channel and large breakdown field-strength [106], [107]. However, the conduction losses in the ON-state resistance (R_{ON}), and the OFF-state breakdown voltage ($V_{BR\ OFF}$) are the main limitations of the power-switch performance. Enhancing $V_{BR\ OFF}$ while keeping the R_{ON} as low as possible is therefore one of the most important challenges in current developments of GaN-based HEMT for power switching applications. For high voltage switching devices the dynamic R_{ON} is an important issue. It is related to the device dispersion as examined in this chapter.

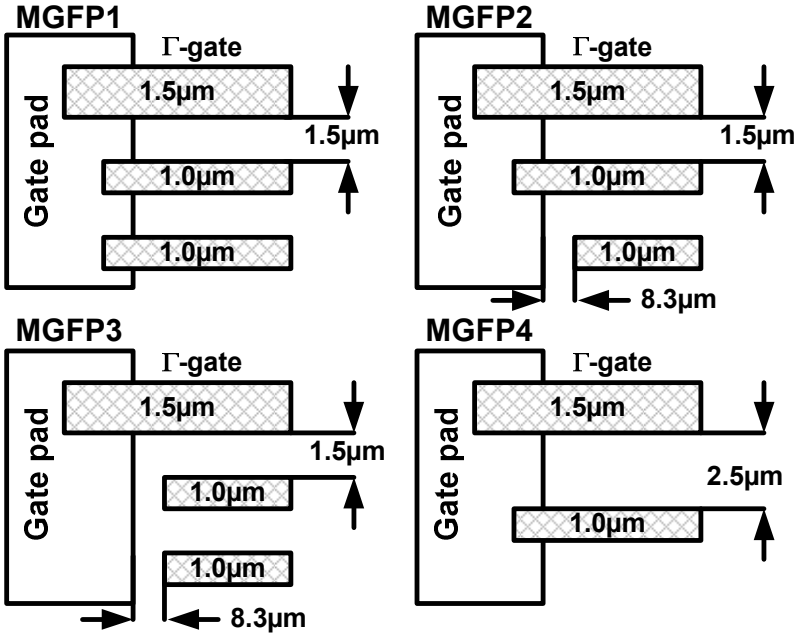


Figure 6.1–2 Top view schematic of Multiple Grating Field Plates (MGFP) configuration types.

In many cases the breakdown of a GaN-based HEMTs is determined by the sub-threshold drain current exceeding the commonly used value of 1 mA/mm. The sub-threshold drain

current is mostly dominated by two leakage currents; the bulk punch-through [50], [79] and the Schottky-gate reverse bias tunneling leakage current [53], [54]. Suppression of these sub-threshold leakage currents would enable enhancement of the device $V_{BR\ OFF}$. Double-Heterojunction (DH)-HEMTs have shown ability to suppress these sub-threshold current leakages , enhance the device $V_{BR\ OFF}$ and an ability to scale it up with the device dimensions [79], [81], But the gate sub-threshold leakage current remains the bottleneck. The Schottky-gate reverse-bias tunneling-leakage is driven by the magnitude and the volumetric-distribution of the electric field peak under the drain-side of the gate [128]. In HEMTs and other field effect devices $V_{BR\ OFF}$ enhancement using field plates (FPs) is a well known method [129], [130], [131]. The FPs distribute the electric field in the channel more equally. Thus, the peak value of the electric field in critical volumes such as under the gate's drain side and under the drain's gate side is reduced. The device performance is improved by a reduced gate leakage. A continuous FP generates one single electric field peak under its edge [129], [132], thus it limits its efficiency to equally distribute the electrical field in the critical volumes of the device. In order to enhance the field redistribution, multiple stacked FPs has been developed [5]. They improve the devices $V_{BR\ OFF}$ performance further but have major drawbacks: A dramatic increase of the device capacitance limits its high-frequency and switching performance. Besides, multi-layer processing requires more photolithographic cycles. Therefore we suggested single layer Multiple Grating Field Plates (MGFPs) as shown in Figure 6.1–1 [74], [133]. The top view of the MGFP types is illustrated in Figure 6.1–2. This design is implemented in the same mask as the gate, so no additional process cycles are required. Additional advantage of the MGFPs is the flexibility of connecting the grating "fingers" to different potential sources such as the gate, the drain, the source, an external potential, or floating fingers in order to reduce the device capacitance. In this experiment, an AlGaN back-barrier was considered along with MGFPs. It was predicted that combining FPs and vertical potential back-barriers would increase the $V_{BR\ OFF}$ of devices, for example applying a *p*-type doped buffer layer [134]. Here, we use the natural, scattering-free, polarization-induced depletion back-barrier [24] of $Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N$ DH-HEMT structures. A multi-wafer study with significant statistical device populations was carried out to investigate different MGFPs configurations. The MGFP fingers are gate-biased or floating. These different configurations were examined on different epitaxial layer structures comparing a conventional GaN buffer with an $Al_yGa_{1-y}N$ back-barrier with two different Al mole fractions, *y*. The devices were characterized in DC and small signal RF operation. Prior to device fabrication we demonstrated the advantages and gave insight to the mode of operation of the MGFPs on GaN based HEMTs devices using the two dimensional, 2-D, physical-based simulation, using Silvaco-"ATLAS" [59].

6.2. Simulation Insight into DH-HEMTs with MGFPs

Two dimensional physical-based device simulations (Silvaco-"ATLAS") [59] were carried out to get an insight into the MGFPs effect in conventional AlGaN/GaN HEMTs and $Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N$ DH-HEMTs. In our previous study, the simulation predicted the current experimental results [74]. The simulation followed the measurement sequence of the sub-threshold drain-leakage current during breakdown or punch-through voltage and logged the 2-D distribution of the devices' physical properties. The simulation was conducted at OFF-state conditions; the gate bias is $V_{GS} = V_{TH}$-1 V << V_{TH} and the drain bias, V_{DS}, was ramped up to V_{DS} = 300 V subsequently. The cross section of electron concentration and the electrical field distribution at V_{DS} = 300 V are presented in Figure 6.2–1 and Figure 6.2–2, respectively for four different devices (a) GaN buffer layer, (b) GaN buffer with MGFP2, (c) DH-HEMTs with $Al_{0.05}Ga_{0.95}N$ back-barrier and (d) DH-HEMTs with $Al_{0.05}Ga_{0.95}N$ back-barrier with MGFP2. The simulation reveals the impact of the FPs to the charge carrier

concentration in the device drift region. Their potential and accumulated electrical field depletes the AlGaN barrier and the channel from electrons as shown in Figure 6.2–1. The simulation for conventional GaN HEMT supports two sub-threshold leakage mechanisms, buffer punch-through [50], [79] and reverse bias tunneling current of the gate Schottky contact [53], [54], [55]. The tunneling current caused by the large magnitude of the electrical field accumulated at the drain-side of the gate, is initiated with the gate's turn-off and rises up with the increase of the drain bias. In parallel, the buffer punch-through current of carriers originated from the source-drain potential difference adds to the total leakage current. This contribution starts at higher drain potentials and in most of the cases dominates the leakage current at sufficiently high drain potential.

As in experiment the simulation result shows a reduction of the sub-threshold drain-leakage current and an increase of the $V_{\mathrm{BR\ OFF}}$ in the DH-HEMTs. This is due to the raised conduction band of the AlGaN-back-barrier. The electron channel becomes a deep potential well, which enables a good 2DEG confinement. In addition the electrical field under the drain side of the gate is reduced and limits the carriers tunneling from the gate-Schottky contact. If the tunneling phenomenon is strong the enhancement of the $V_{\mathrm{BR\ OFF}}$ using AlGaN-back-barrier is limited. The integration of MGFP2 with conventional GaN HEMT shows, as in experiment, no enhancement of the $V_{\mathrm{BR\ OFF}}$. Here both, the gate-drain current and the source-drain current can unhinder flow. The electrons are not confined in the channel layer and punch through it not only under the gate but also under the FPs in high field conditions as shown in Figure 6.2–1(c). Even though that the FPs reduce the fields under the drain side of the gate, it take place only in higher drain voltages, where the buffer punch-through of the device already occurred therefore they are not efficient to enhance the device $V_{\mathrm{BR\ OFF}}$. On the other hand, the inclusion of MGFP2 in DH-HEMTs yields the intended results. Both, the gate and source leakage currents get confined by the back-barrier. Thus, the depletion zones of the gate and the FPs can efficiently block the current path. In addition to the depletion zone of the gate that acts on the source leakage current, the depletion zones of the MGFPs additionally act on the gate leakage.

The MGFPs integrated on DH-HEMTs work in positive-feedback-loop mode. As the drain voltage increases and reaches high voltage operation range, the FPs accumulate more and more electrical field that increases the potential barrier and deepens the depletion of the channel. Consequently the flow of carriers is prevented and therefore enables further increase of the drain voltage. The device $V_{\mathrm{BR\ OFF}}$ is postponed. The magnitude of the remaining leakage current is limited by the back-barrier confinement.

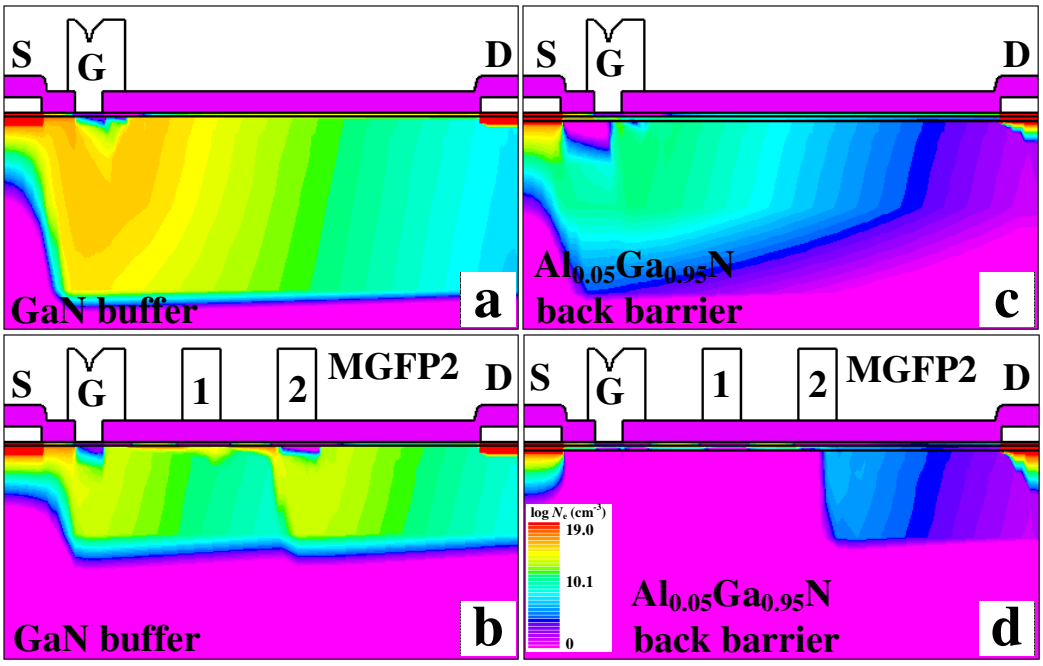


Figure 6.2–1 Logarithmic electron concentration, n_e, distribution calculation from physical based simulation for devices with L_{GD} = 10 µm at V_{DS} = 300 V and V_{GS} = V_{Th} - 1 V with (a) GaN buffer, (b) GaN Buffer w/MGFP2, (c) $Al_{0.05}Ga_{0.95}N$ back-barrier, and (d) $Al_{0.05}Ga_{0.95}N$ back-barrier w/MGFP2.

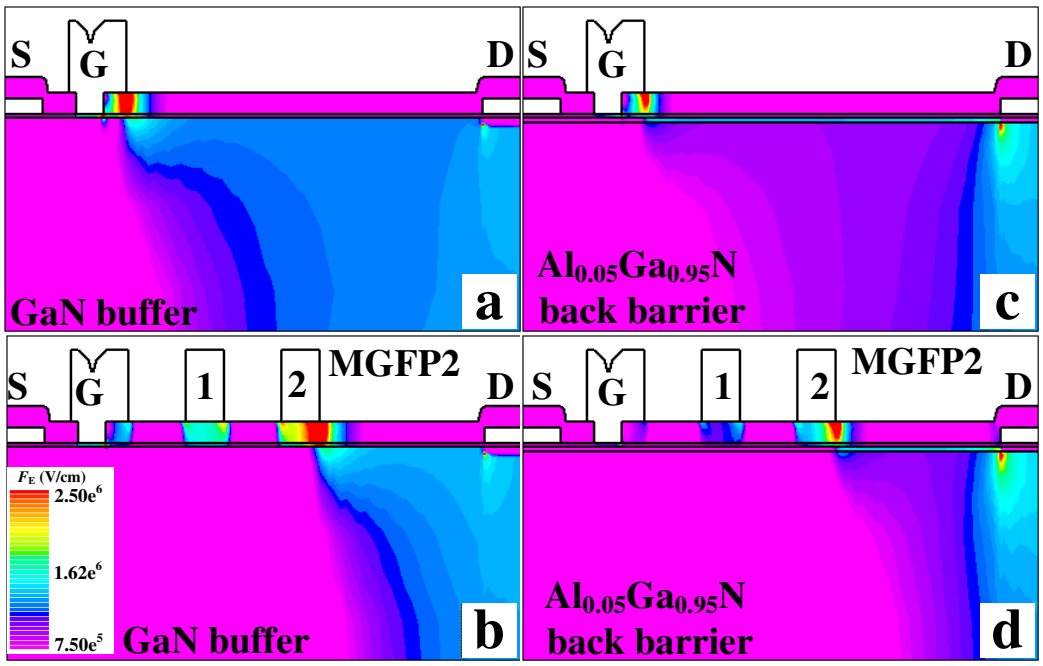


Figure 6.2–2 Electric field distribution calculation from physical based simulation for devices with L_{GD} = 10 µm at V_{DS} = 300 V and V_{GS} = V_{Th} - 1 V with (a) GaN buffer, (b) GaN Buffer w/MGFP2, (c) $Al_{0.05}Ga_{0.95}N$ back-barrier, and (d) $Al_{0.05}Ga_{0.95}N$ back-barrier w/MGFP2.

6.3. Process Integration of DH-HEMTs with MGFPs

For comparison, three types of samples were studied, a conventional AlGaN/GaN HEMT, wafer "A", and two variations of AlGaN double-heterojunction (DH) structure, wafers "B"-"C", (see summary in Table 6.3–1). The samples were grown by Metal Organic Vapor Phase Epitaxy (MOVPE) on semi-isolating (SI)-SiC substrates. All samples have an AlN

nucleation layer followed by Unintentionally Doped (UID) buffer layer. For the GaN buffer structure (wafer "A") a 1.65 µm thick UID GaN was grown. For the AlGaN DH-buffer structure (wafers "B"-"C") a 1.7 µm thick UID $Al_yGa_{1-y}N$ layer with Al mole fraction (y) of 0.05 and 0.10 was grown. They are referred to later as DH-HEMTs with $Al_yGa_{1-y}N$ buffer layer with y Al mole fraction. The DH-HEMTs samples had a 35 nm UID GaN channel layer. All samples had a 25 nm $Al_{0.25}Ga_{0.75}N$ barrier layer. Field-effect transistors were fabricated on all wafer types. Ti/Al/Mo/Au based ohmic contacts were formed by e-beam evaporation and annealed at 830°C. Inter-device insulation was made using $^{14}N^+$ multi-energy implantation. The AlGaN barrier was passivated with 150 nm SiN_x. A gate trench in the passivation was defined by i-line optical lithography and subsequently opened by dry etching. Ir/Ti/Au contacts were then evaporated for the gate Schottky metal, followed by a metal liftoff.

Layer	Wafer "A"		Wafer "B"		Wafer "C"	
	x	d (nm)	x / y	d (nm)	x / y	d (nm)
Barrier $Al_xGa_{1-x}N$	0.25	25	0.25	25	0.25	25
Channel GaN	-	1650	-	35	-	35
Back barrier layer $Al_yGa_{1-y}N$	-	-	0.05	~1700	0.10	~1700
Nucleation AlN	-	~50	-	~100	-	~100
"d " refers to layer thickness , "x " and "y " refer to Al mole fraction.						

Table 6.3–1 Epitaxy structure of the compared wafers.

The fabricated devices were 2×125 µm wide with a gate length of 0.7 µm and asymmetrical Γ-gate head of 1.5 µm with 0.2 µm extension towards the source and 0.6 µm extension towards the drain. The gate-drain spacing L_{GD} was 10 µm and the source gate spacing L_{GS} was 1 µm. Four types of MGFPs designs, constrained by lithography-liftoff process capability, were tested and compared with standard device having no FPs as an experiment control. The top view of the MGFP types is illustrated in Figure 6.1–2, MGFP1 has two 1.0 µm wide FPs with spacing of 1.5 µm; both MGFPs are connected to the gate electrode pad. MGFP2 has two 1.0 µm wide FPs with spacing of 1.5 µm; but only one FP is connected to the gate electrode pad and the second FP is floating (i.e. neither connected to any potential nor grounded). MGFP3 has two 1.0 µm wide FPs with spacing of 1.5 µm; both MGFPs are floating. MGFP4 has one 1.0 µm wide FP with spacing of 2.5 µm from the gate head, connected to the gate electrode pad. Figure 6.3–1 depicts a SEM micrograph of manufactured high voltage test device with MGFP2 configuration.

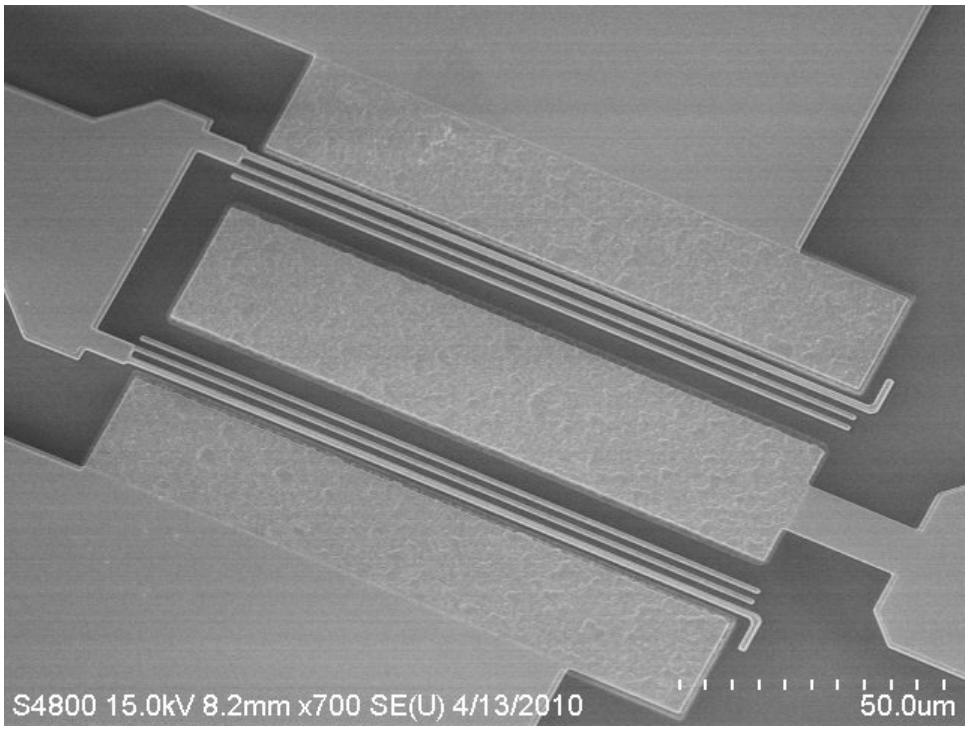


Figure 6.3–1 SEM micrograph of manufactured device 2 × 125 µm L_{GD} =10 µm L_G = 0.7 µm with MGFP2 configuration.

6.4. DC Characterization and Measurements

Wafer level distributions of DC transfer characteristics were measured at V_{DS} = 10 V for devices on wafer "A" and on wafer "C" with L_{GD} = 10 µm having either no FPs or MGFP2 are shown in Figure 6.4–1. The reduction of the $I_{DS\,max}$ with the increase of the Al mole fraction y in the back-barrier is in agreement with our previous work [79]. Any statistical difference in transfer characteristics could not be observed for any type of MGFPs. Figure 6.4–2 shows an example of comparison of wafer level distribution of *I-V* characteristics for devices with no FPs, and devices with MGFP2 configuration on wafer with $Al_{0.05}Ga_{0.95}N$ back-barrier. No statistical difference at this measurement level could be seen.

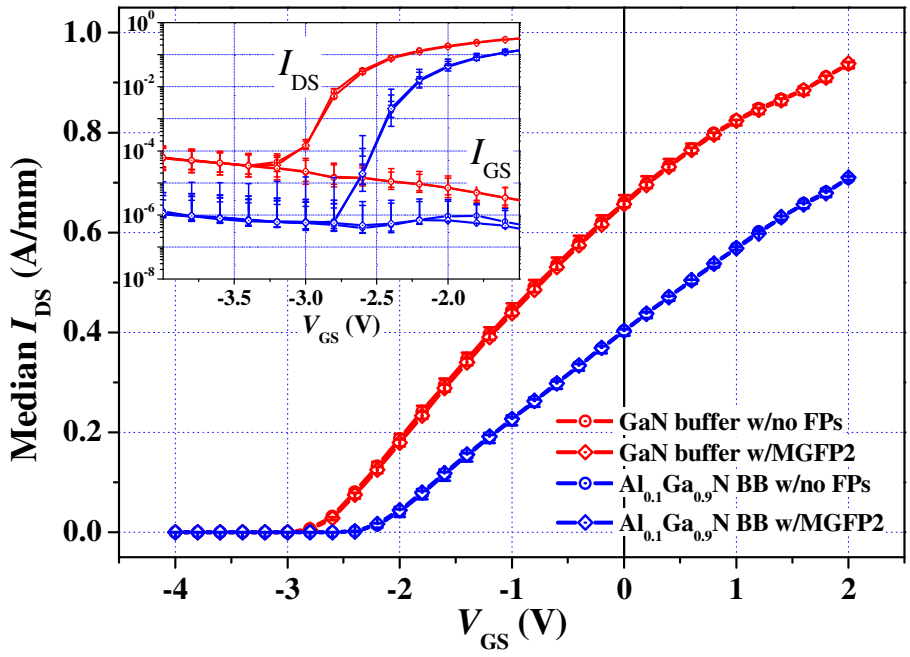


Figure 6.4–1 Wafer level median transfer characteristics of L_{GD} = 10 µm devices with GaN buffer, $Al_{0.1}Ga_{0.9}N$ back barrier with no field plates and with MGFP2 measured at V_{DS} = 10 V. (Error bars are 25% and 75% percentiles). Inset: log scale of the sub-threshold regime. The curves for devices with no FPs, and devices with MGFP did no show any statistical difference and in this graph visually lying on top of each other.

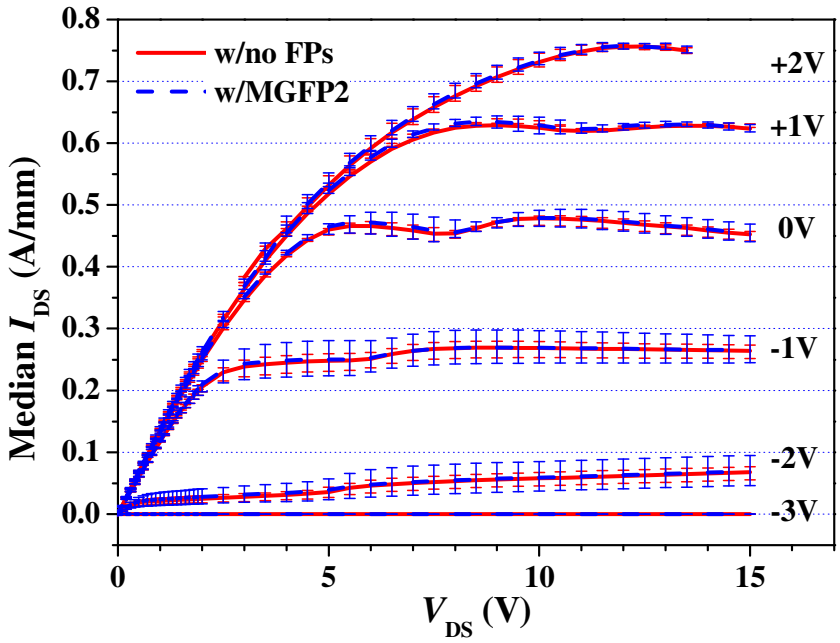


Figure 6.4–2 Wafer level median *I-V* characteristics of L_{GD} = 10 µm devices with GaN buffer, $Al_{0.05}Ga_{0.95}N$ back barrier with no field plates and with MGFP2. (Error bars are 25% and 75% percentiles).

The device's $V_{BR\ OFF}$ was measured at sub-threshold bias $V_{TH} >> V_{GS}$ = -7 V. During the $V_{BR\ OFF}$ measurements the devices were immersed in 3M™ Fluorinert™ Electronic Liquid FC-3283 [123] to avoid arcing through the air. The drain bias was increased in steps of 2 V and the currents were logged until breakdown was identified. The $V_{BR\ OFF}$ was defined as the voltage at which the drain current exceeds the value of 1 mA/mm. Figure 6.4–3 shows examples of sub-threshold leakage currents measurements for conventional HEMTs on wafer

"A", on wafer "C", on wafer "B" with MGFP2 and on wafer "C", with MGFP2. The results show a suppression of the sub-threshold drain leakage current for the DH-HEMTs and an improvement in the device $V_{BR\ OFF}$ characteristic. Drastic suppression of the sub-threshold drain leakage current was observed when a MGFP2 was integrated in the DH-HEMT devices. The sub-threshold drain-leakage current is suppressed and devices $V_{BR\ OFF}$ reach values of 648 V and 714 V for wafers "B" and "C" respectively.

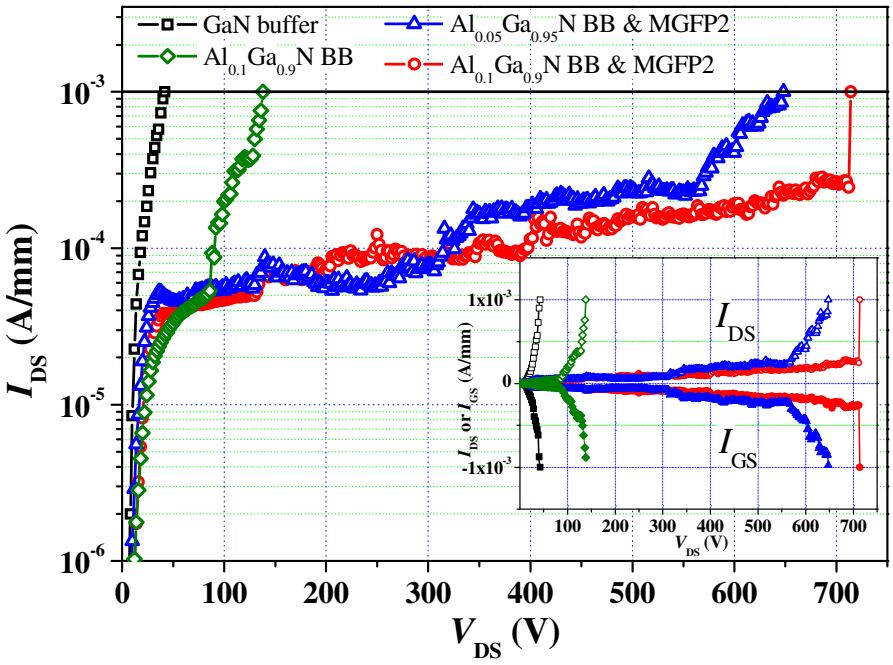


Figure 6.4–3 Drain current output during $V_{BR\ OFF}$ measurements for HEMT devices with GaN buffer, $Al_{0.1}Ga_{0.9}N$ back barrier layer, $Al_{0.05}Ga_{0.95}N$ back barrier layer with MGFP2 and $Al_{0.1}Ga_{0.9}N$ back barrier layer with MGFP2 devices measured at V_{GS} = -7 V. (L_{GD} = 10 µm). Inset: linear scale of the sub-threshold drain current and gate current.

Wafer-level statistical distribution analysis of the $V_{BR\ OFF}$ measurements for all wafers and different MGFPs designs is shown in Figure 6.4–4. For wafer "A" a median of 40 V was measured. Neither the median nor the distributions of the devices $V_{BR\ OFF}$ are influenced by any FPs configuration. DH-HEMT devices with no FPs show median of 122 V and 116 V for wafers "B" and "C" respectively, with similar statistical variation. Dramatic increase of the $V_{BR\ OFF}$ in several hundreds of volts for devices with MGFPs on both DH-HEMTs is shown. Wafers' level median $V_{BR\ OFF}$ values, shown in Figure 6.4–4, are 427 V, 490 V and 502 V for devices with MGFP1, MGFP2 and MGFP4 respectively on wafer "B", and Wafers' level median $V_{BR\ OFF}$ values are 466 V, 634 V and 542 V for devices with MGFP1, MGFP2 and MGFP4 respectively on wafer "C". In the case of the combination of both types of DH-HEMTs and MGFP3 configuration, with two floating MGFPs, the wafer's level median $V_{BR\ OFF}$ shows no discrepancy from the devices with no FPs, and the all four populations distributions match. In wafer "B" the wafer's level $V_{BR\ OFF}$ distribution for MGFP2 and MGFP4 statistically matches, but the MGFP1 configuration is somewhat lower, and in wafer "C" the wafer's level $V_{BR\ OFF}$ distributions for all types of MGFPs do not match, and clear segmentation is observed.

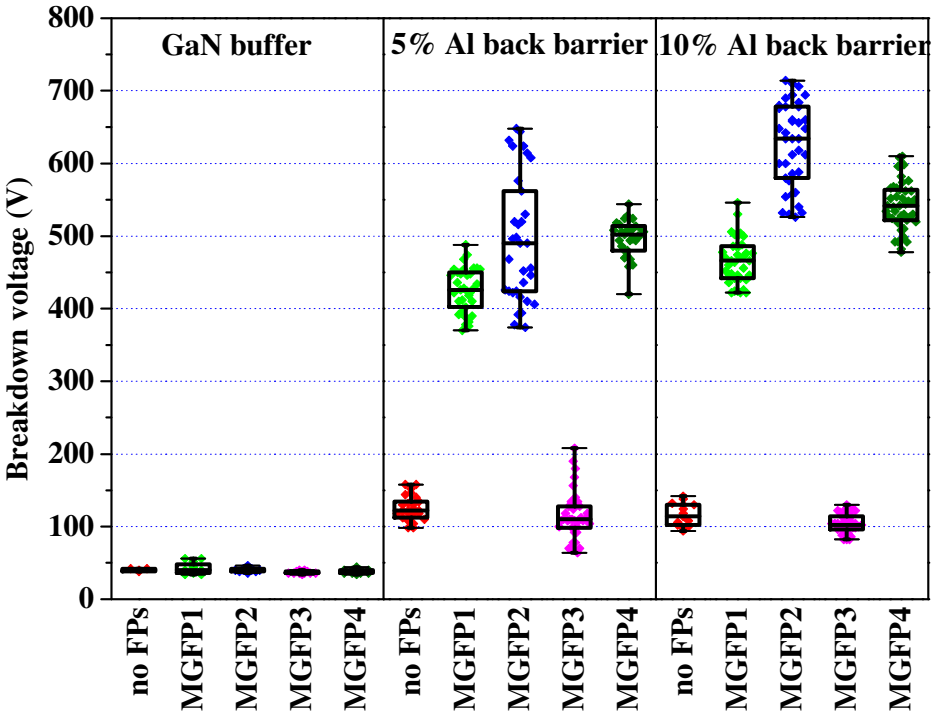


Figure 6.4–4 Wafers' distribution breakdown voltage for devices with L_{GD} = 10 µm with different MGFPs configuration. The center line is the population median, box top/bottom lines are 25% and 75% percentiles and top/bottom lines are minimum and maximum.

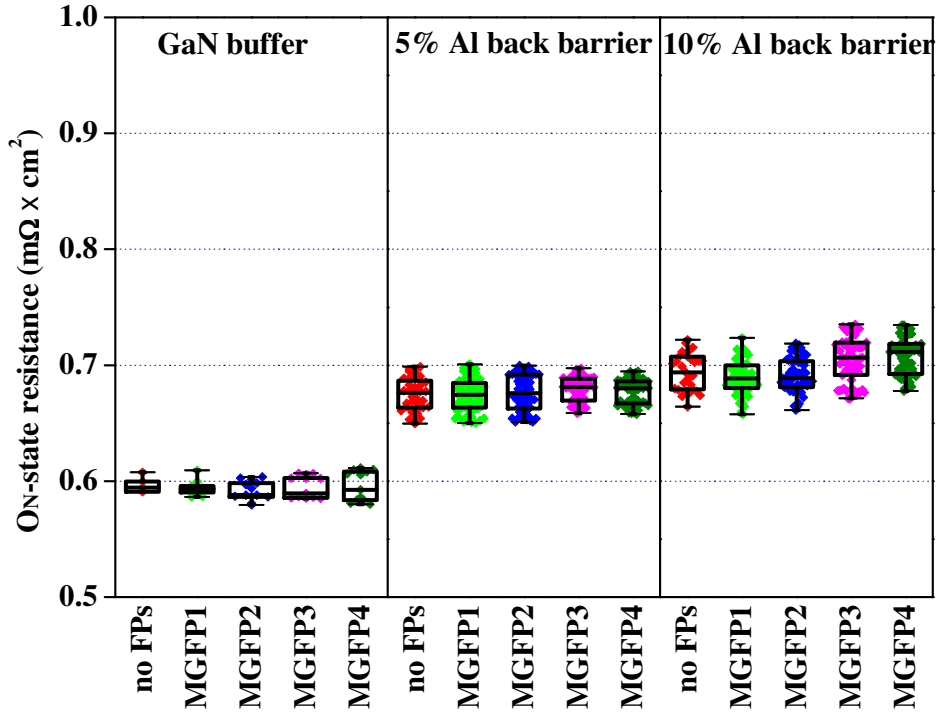


Figure 6.4–5 Wafers' distribution ON-state resistance ($R_{ON} \times A$) measured at V_{GS} = +2 V for devices with L_{GD} = 10 µm with different MGFPs configuration. The center line is the population median, box top/bottom lines are 25% and 75% percentiles and top/bottom lines are minimum and maximum.

While demonstrating an enormous improvement in the $V_{BR\ OFF}$, the price in the specific ON-state resistance, $R_{ON} \times A$, is minimal. Here, the $R_{ON} \times A$ is defined as the reciprocal of the *I-V* curve's at V_{GS} = +2 V slope at the steepest position multiple by the device active area, *A*.

As shown in Figure 6.4–5 the introduction of Al into the devices' buffer as back-barrier adds only a very small component to the $R_{ON} \times A$ of ~ 0.1 mΩ × cm^2. The integration of MGFP, in any configuration, has no effect on the $R_{ON} \times A$ on the individual wafers; they are equally distributed and belong to the same population.

6.5. Mw Characterization and Measurements

6.5.1. DIVA measurements

Representative example of 200 ns pulsed *I-V* (DIVA) measurements for devices on wafer "C" without FPs and with MGFP2 configuration is shown in Figure 6.5–1. The pulsed measurements were done at two quiescent bias points; at [V_{GS} = 0 V, V_{DS} = 0 V], The pulsed measurements were done at two quiescent bias points; at [V_{GS} = 0 V, V_{DS} = 0 V], to minimize the effect of thermal heating and slow traps [103] and at partially open channel conditions of [V_{GS} |(I_{DS}= 100 mA/mm), V_{DS} = 30 V] to emphasize the drain current lag originated at the drift region from the interaction of the MGFPs with the back-barrier; were V_{GS} |(I_{DS} = 100 mA/mm) = -2.3 V, -1.8 V and -1.7 V for devices on wafer "A", "B" and "C" respectively. As demonstrated in Figure 6.5–1 no observable difference between non field-plated device and the device owning MGFPs could be seen when pulsing from quiescent bias point [V_{GS} = 0 V, V_{DS} = 0 V].

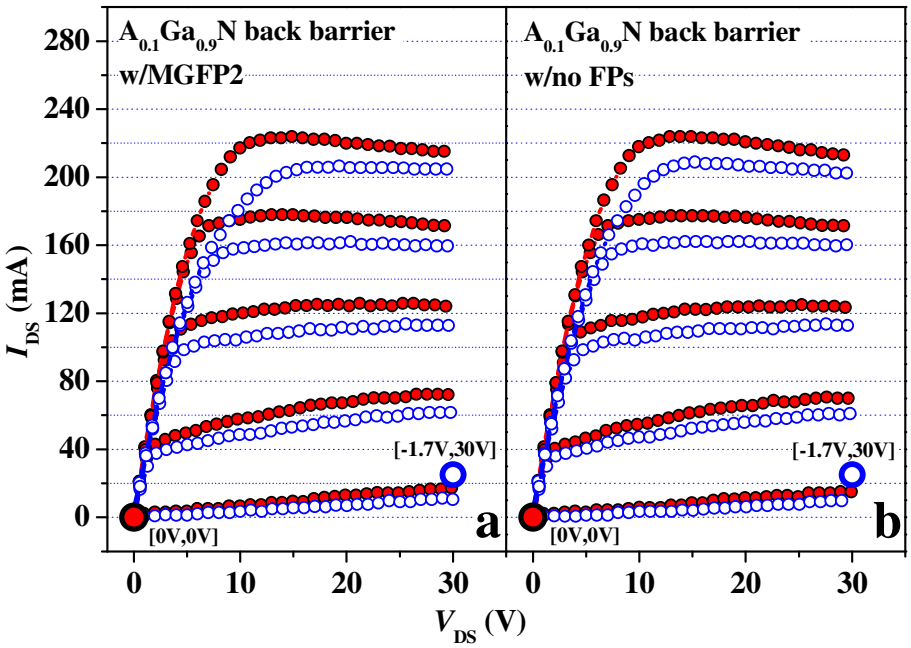


Figure 6.5–1 200 ns pulsed *I-V* (DIVA) measurements of 2 × 125-µm, L_{GD} = 10 µm DH-HEMT devices with $Al_{0.1}Ga_{0.9}N$ back-barrier (a) with MGFP2 and (b) with no FPs. $V_{GS\ max}$ = +2 V and ΔV_{GS} = 1 V. DIVA quiescent points [V_{GS} = 0 V, V_{DS} = 0 V] (solid red dot) and [V_{GS} = -1.7 V, V_{DS} = 30 V] (empty blue dot).

An increase in drain current lag could be observed when measuring the MGFPs devices from the demanding partially open channel conditions quiescent bias point of V_{GS} |(I_{DS}= 100 mA/mm), V_{DS} = 30 V. The drain current lag, *L* (%), is quantified by:

$$L(\%) = \frac{\Delta I_{\text{DS dyn}}}{I_{\text{DS dyn}}\big|_{(V_{\text{GS}}=0\text{V},V_{\text{DS}}=0\text{V})}} \times 100\% \Bigg|_{(V_{\text{GS}}=+1\text{V},V_{\text{DS}}=10\text{V})} \qquad 6\text{–}1$$

$$\Delta I_{\text{DS dyn}} = I_{\text{DS dyn}}\big|_{(V_{\text{GS}}=0\text{ V},V_{\text{DS}}=0\text{ V})} - I_{\text{DS dyn}}\Big|_{\left(V_{\text{GS}}\big|_{(I_{\text{DS}}=100\text{ mA / mm})},V_{\text{DS}}=30\text{ V}\right)} \qquad 6\text{–}2$$

Where $I_{\text{DS dyn}}\big|_{(V_{\text{GS}}=0\text{V},V_{\text{DS}}=0\text{V})}$ is the drain current measured in dynamic pulsed conditions from quiescent bias point of $V_{\text{GS}} = 0$ V and $V_{\text{DS}} = 0$ V, $I_{\text{DS dyn}}\big|_{(V_{\text{GS}}|(I_{\text{DS}}=100\text{mA/mm}),\,V_{\text{DS}}=30\text{V})}$ is the drain current measured by the pulsed measurements from quiescent bias point of V_{GS} that gives $I_{\text{DS}} = 100$ mA/mm in DC and $V_{\text{DS}} = 30$ V, both measured when $V_{\text{GS}} = +1$ V and $V_{\text{DS}} = 10$ V. Figure 6.5–2 summarizes the current lag parameter for the different MGFP configurations and different back-barrier devices. For devices manufactured on wafer "A" the current lag is dependent on the MGFP configuration; devices with at least one MGFP biased with gate potential show some lag increase. Devices without FPs and devices only floating FPs, have similar current lag. For devices on wafer "B" the current lag is increased for all type of devices. Similar to wafer "A" the drain current lag is dependent on the MGFP configuration. For devices on wafer "C" the current lag is dominated only by the back-barrier Al mole fraction. The devices' current lag on this wafer type is independent on the existence of any type of MGFPs and statistically matched for all types of MGFPs. Additional pulsed measurements were done from sub-threshold quiescent bias points at [$V_{\text{GS}} = V_{\text{th}}$-0.5 V, $V_{\text{DS}} = 30$ V]; were V_{GS} = -3.55 V, -3.10 V and -2.95 V resulting in lag parameter of L =4.8 %, 11.1 % and 9.1 % for devices on wafer "A", "B" and "C" respectively. The lag parameter for all MGFPs types in this case was equally distributed and belongs to the same wafer's population.

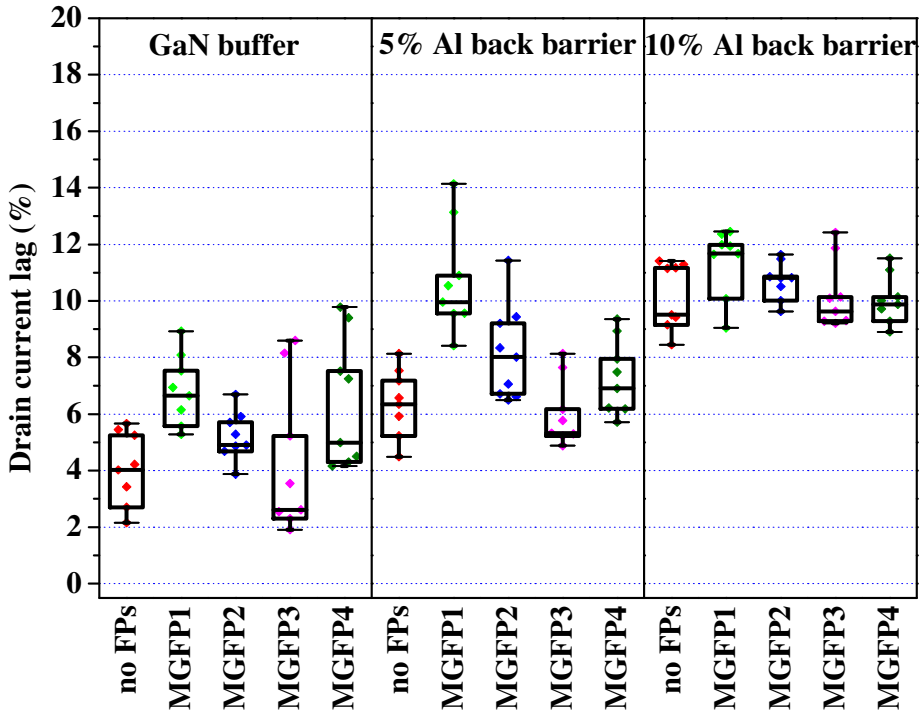


Figure 6.5–2 I_{DS} lag percentage distribution for different types back-barrier and different types of MGFPs

6.5.2. S-Parameter Measurements and f_t and f_{max} Extraction

Small signal frequency dependent S-parameters for all types of devices were measured. Typical S-parameters respond to small microwave signal for devices without FPs and with MGFP2 manufactured on wafer "B" could be seen in Figure 6.5–3. Cut-off frequency, f_T, values ware extracted from the extrapolation of the $|h_{21}|^2$ parameter where it's slope equals -20 dB / decade reaches gain of 0 dB. The maximum oscillation frequency, f_{max}, values were extracted from the extrapolation of the maximum unilateral transducer-power gain, MUG, and maximum stable gain, MSG, parameters where it's slope equals -20 dB / decade reaches gain of 0 dB.

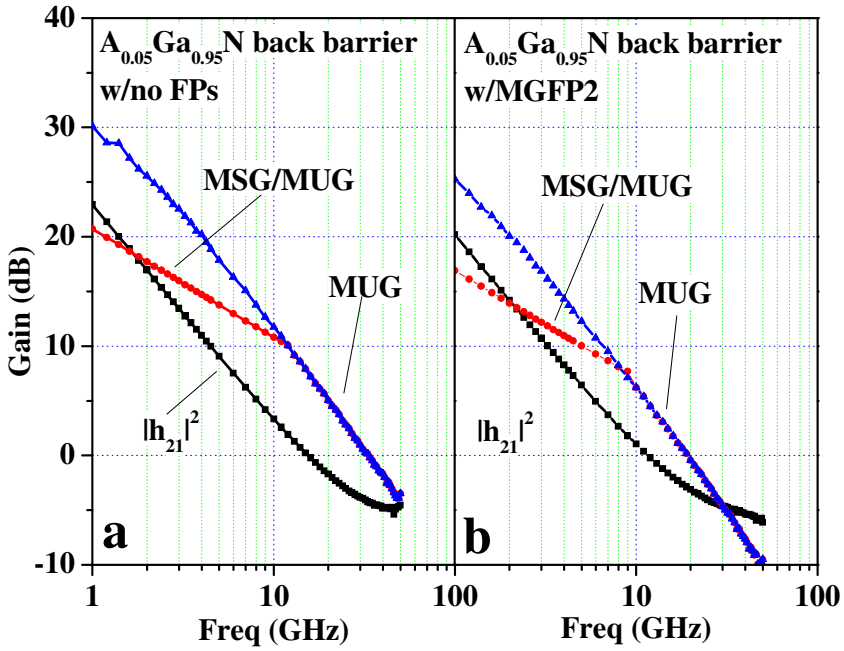


Figure 6.5–3 Frequency response characteristics of DH-HEMTs devices with $Al_{0.05}Ga_{0.95}N$ back-barrier having no FPs (a) and MGFP2 (b) measured at V_{DS} = 15 V and V_{GS} = -0.7 V.

Figure 6.5–4 compares the evaluated f_T and f_{max} for the all types of devices. The epitaxial design did not affect both f_T and f_{max}. However, the introduction of FPs with gate potential reduces the evaluated f_T and f_{max} values. Devices with MGFP1, with two FPs owning gate potential, show wafers' median f_T value of 8.2 GHz and wafers' median f_{max} value 14.3 GHz. Devices with MGFP2 and MGFP4, both with one FP owning gate potential, show wafers' median f_T values of 10.0 GHz and 10.1 GHz and wafers' median f_{max} values 21.3 GHz and 22.4 GHz respectively. Both populations are statistically matched. Devices with MGFP3, owning no gate potential FPs, and devices with no FPs, show wafers' median f_T values of 14.0 GHz and 14.1 GHz and wafers' median f_{max} values 38.7 GHz and 38.9 GHz respectively, both populations are statistically matching.

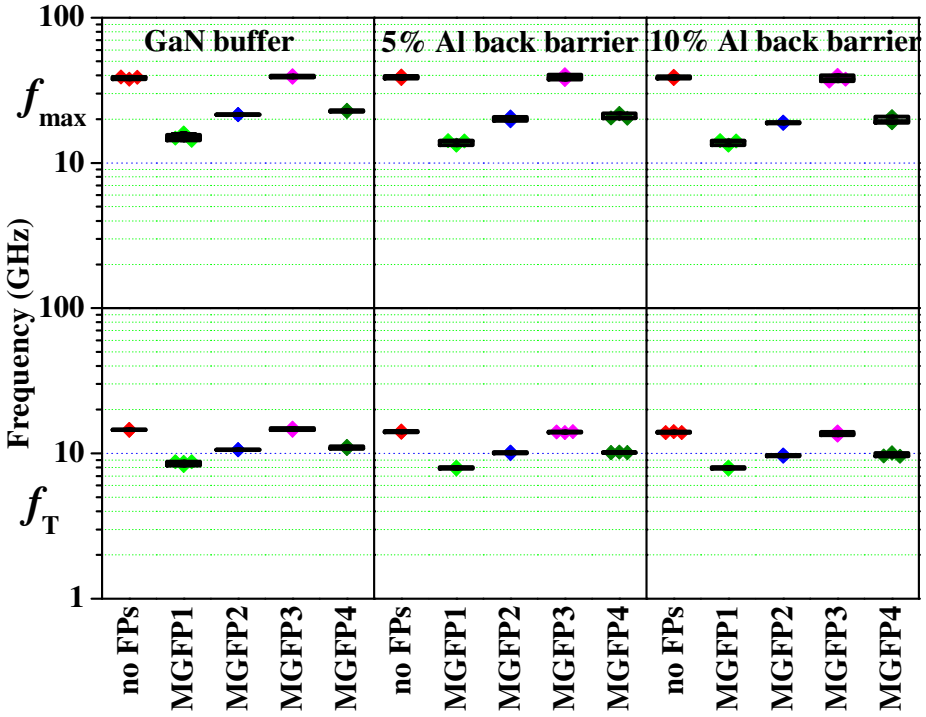


Figure 6.5–4 Wafers' level distribution comparison of f_T and f_{max} for devices with different MGFPs types.

6.6. Discussion

Several hundreds volts of $V_{BR\ OFF}$ enhancement in GaN based HEMTs were obtained. By employing combination of two complimentary methods, DH-HEMTs with $Al_yGa_{1-y}N$ back-barrier and MGFPs, the device sub-threshold drain leakage current was reduced, thus the $V_{BR\ OFF}$ was postponed to higher values.

The MGFPs with at least one gate biased FP behaves as secondary MOS gate. The DC mode of operation of the MGFPs could be learned from the physical-based two dimensional simulations. The combination of the MGFP and AlGaN-back-barrier takes action in two complimentary operation modes; redistribution of the electrical field at high voltages along the depletion region between the gate and the drain and by that reducing the electrical field peak under the drain side of the gate. By reducing this field the Schottky-gate reverse bias leakage is suppressed. Second, the MGFPs accumulate strong negative field that deeply depletes the depletion region between the gate and the drain and suppress any sub-threshold leakage current.

The integration of MGFPs in HEMTs with conventional GaN buffer layer could not enhance the devices $V_{BR\ OFF}$. This is due to the high sub-threshold gate and source leakage currents. The total leakage current exceeds the $V_{BR\ OFF}$ current limit of 1 mA/mm before the FPs accumulate enough electric field to prevent and block the gate leakage. It implies that the GaN buffer is inadequate to prevent the punch-through as also indicated by 2D simulation results. The enhancement of the $V_{BR\ OFF}$ in DH-HEMT is achieved by two effects. The improved channel confinement prevents efficiently the punch-through and the mitigated electrical field peak under the drain-side of the gate reduces the Schottky-gate-tunneling-leakage. However, if the sub-threshold leakage current is dominated by the gate-leakage the device will reach the $V_{BR\ OFF}$ current limit conditions early and the effect of the channel confinement for $V_{BR\ OFF}$ is therefore limited.

The independence of the $V_{BR\ OFF}$ on the Al mole fraction ($y = 0.05$ or $y = 0.10$) in AlGaN back-barrier, see Figure 6.4–4, suggests that the improvement of the device buffer

confinement solely is insufficient; therefore it is attributed to the fact that the dominant mechanism in DH-HEMTs of $V_{BR\ OFF}$ is gate-tunneling-leakage when no FPs are used.

On the other hand, remarkable $V_{BR\ OFF}$ enhancement is possible by combining the DH-HEMTs with MGFPs with the condition of at least one gate-connected FP. In this case, increasing the Al mole fraction, y, in the back-barrier from $y = 0.05$ to $y = 0.10$ leads into the further $V_{BR\ OFF}$ enhancement, see Figure 6.4–4. As shown in Figure 6.4–3, in the case of DH-HEMT without MGFPs the sub-threshold leakage current is suppressed up to relatively low drain voltages and increases exponentially as the gate-tunneling-leakage progresses with the increasing electrical field under the drain side of the gate. In contrast the integration of MGFPs suppresses the leakage current and does not allow the rapid increase of it. The sub-threshold current stays for both Al mole fraction DH-HEMTs on the same level but the one with the higher Al mole fraction prevents the later high voltage punch through up to higher drain voltages, thus gives a higher $V_{BR\ OFF}$.

As mentioned, the enhancement of the $V_{BR\ OFF}$ is possible if at least one of the FPs is biased with the gate potential. MGFP3 configuration with two floating FPs did not show improvement of the device's $V_{BR\ OFF}$. This suggests that the FP-function is a MOS-like second gate, as observed from the simulation.

When applying the gate potential on both FPs (MGFP1) a weakening of $V_{BR\ OFF}$ due to the larger field under this second FP was observed. The incorporation of a floating FP, MGFP2, buffers the high field of the drain and shows $V_{BR\ OFF}$ improvement. This is more pronounced in the case of high Al mole fraction back-barrier where the electrical field is better distributed along the cannel. In both cases the increase of the scatter in the measured $V_{BR\ OFF}$ values can be associated to the change in the distribution of the actual potential of the floating FP which can be related to local variations of the material properties.

While the improvement in the device $V_{BR\ OFF}$ characteristics is significant, some price has to be paid: The ON-state resistance is negligibly increased by the presence of the back-barrier heterojunction. It is mainly influenced by the GaN channel thickness [81], [82]. The presence of MGFPs does not affect the R_{ON}, which makes this technique very attractive for power devices.

A pulsed I-V measurement (DIVA) is an efficient tool to determine the device efficiency and in many cases it reveals severe problems of the device. Current collapse occurs when hot channel carriers are injected into the buffer under the drift region, where they are trapped at the deep defects sites [101], [102]. In our case, the pulsed measurement shows to some extent an increase in the lag parameter for devices with MGFPs. MGFP1, with two gate-connected FPs, shows a higher lag parameter than other MGFP designs, see Figure 6.5–2. MGFP3, with only floating FPs, shows the same lag parameter as no FPs. This could be explained by the larger potential swing below a gate connected FP compared to a floating FP. Thus, more localized states get filled and emptied below the gate connected FP. As the Al mole fraction in the back-barrier increases the lag parameter does not depend anymore on the MGFP design. This is due to the increased channel confinement. The higher lag parameters compared to the GaN-buffer case are only attributed to the lower absolute drain currents for the DH-HEMTs.

The frequency-dependent small signal measurements (see Figure 6.5–3 and Figure 6.5–4) disclose more about the nature of the MGFPs While there is no apparent dependence of f_T and f_{max} on the epitaxial design, f_T and f_{max} values strongly correlate with the number of gate-biased FPs. MGFP2 and MGFP4 which have one gate connected FP show the similar values of f_T and f_{max}. MGFP1 that has two gate connected FP has lower f_T and f_{max}, and MGFP3 with floating FPs has as high f_T and f_{max} values as devices with no FPs. The dependence in f_T and f_{max} for the gate-potential biased FPs also supports the assumption that these MGFPs act like additional MOS gates.

The specific ON-state resistances, $R_{ON} \times A$, versus the $V_{BR\ OFF}$, of the manufactured devices are compared to the state-of-the-art GaN based devices in Figure 6.6–1. It could be seen that

the integration of the MGFP, for the case of MGFP2, shifts the device power performance horizontally towards higher $V_{BR\ OFF}$, aligning it with other reported state-of-the-art low $R_{ON} \times A$ GaN technology. The synergy of DH-HEMTs and MGFPs enables devices that can be operated up to the material limits, thus taking full advantage of the superior material properties of the AlGaN/GaN system.

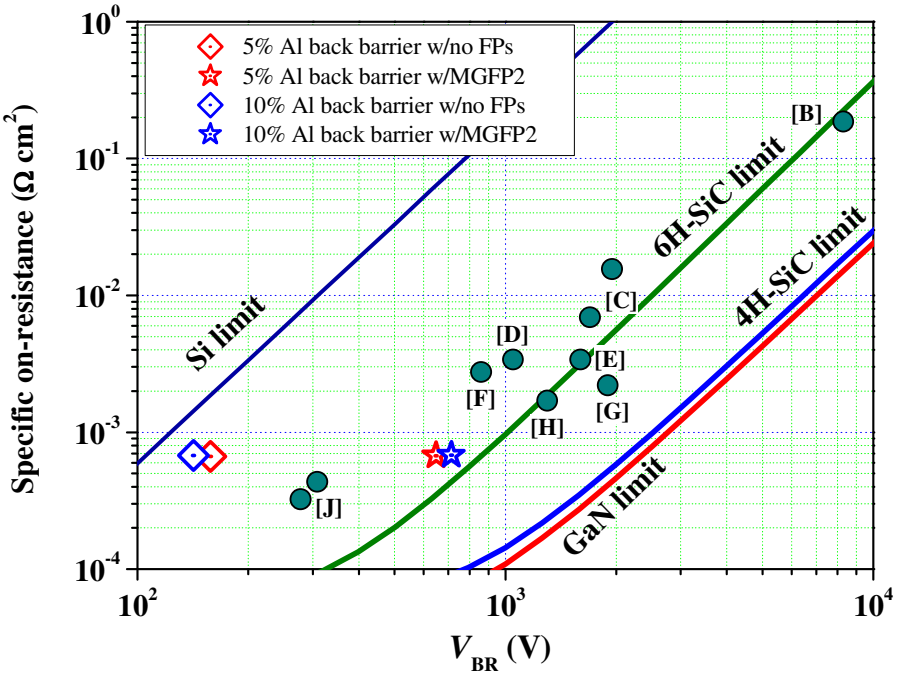


Figure 6.6–1 OFF-state breakdown voltage, $V_{BR\ OFF}$ vs. $R_{ON} \times A$ of the fabricated DH-HEMTs with no FPs and with MGFP2 compared with those of the state-of-the-art GaN based devices.

Points	Year	Group	Technology	$R_{ON} \times A$ (Ω·cm²)	$V_{BR\ OFF}$ (V)
B	2007	Uemoto *et al.* [125]	GaN HEMT	0.186	8300
C	2006	Yagi *et al.* [10]	GaN HEMT	0.0069	1700
D	2001	Zhang *et al.* [8]	GaN HEMT	0.0034	1050
E	2006	Tipirneni *et al.* [9]	GaN HEMT	0.0034	1600
F	2004	Huili *et al.* [5]	GaN HEMT	0.0028	860
G	2006	Dora *et al.* [13]	GaN HEMT	0.0022	1900
H	2002	Zhang *et al.* [7]	GaN HEMT	0.0017	1300
J	2010	Bahat-Treidel *et al.* [82]	GaN HEMT	0.00034	310

Table 6.6–1 OFF-state breakdown voltage, $V_{BR\ OFF}$ vs. $R_{ON} \times A$ data.

6.7. Conclusions

A systematic study of Multiple Grating Field Plates, MGFPs, in combination with a wide-bandgap AlGaN back-barrier was conducted in GaN based HEMTs on SI-SiC substrate. The introduction of an AlGaN buffer layer leads to a better confinement of the electrons in the GaN channel, accompanied by a reduction in $I_{DS\ max}$ and an increase of V_{Th}. Combining DH-HEMTs with gate biased MGFPs suppresses the sub-threshold drain currents, source-drain leakage and gate leakage, therefore enhances the device $V_{BR\ OFF}$ by hundreds of volts. Devices with one gate connected FP and one floating FP, integrated in DH-HEMT with $Al_{0.1}Ga_{0.9}N$-back-barrier showed the best $V_{BR\ OFF}$ performance. Negligible trade-off in ON-state resistance, due to channel confinement was observed. Minor lag factor increase and decrease in f_T and f_{max} were observed due to the additional gate-channel and gate-drain capacitance.

Chapter 7

AlGaN/GaN-HEMT with Integrated Recessed Schottky-Drain Protection Diode

An AlGaN/GaN high electron mobility transistor (HEMT) with integrated recessed protection diode on the drain side of the transistor channel is presented. Results from our Schottky-drain HEMT demonstrate an excellent reverse blocking with minor trade-off in the ON-state resistance for the complete device. The excellent quality of the forward diode characteristics indicates high robustness of the recess process. The reverse blocking capability of the diode is better than –110 V. Physical-based device simulations give insight in the respective electronic mechanisms. This is the first time that a recessed Schottky-drain diode integrated in a HEMT device is presented [135], [136].

7.1. Introduction, Concept and Physical Based Simulation

GaN based High Electron Mobility Transistors (HEMTs) already show excellent performance in microwave power amplifiers, including wireless base stations [137]. For high efficiency power amplifiers (PAs), efforts are presently focusing on the switch-mode type of amplifier architecture, as it allows highest power added efficiency. From the different types the Class-S concept, which uses band-pass delta sigma bit sequences at the input to switch the power transistor between ON and OFF-state, becomes more attractive also for microwave frequencies [138]. Class-S switch-mode amplifiers need a reconstruction filter at the output side that may lead to short negative pulses at the drain terminal of the power transistor. The negative pulses depending on circuitry may reach similar voltage level as in the positive range. For the purpose of high frequency switching in microwave switch-mode amplifiers it is therefore highly desirable to combine the advantages of the high speed switching transistor with a fast switching protection diode connected in series with the GaN-HEMT. The integration of a fast diode in the transistor protects the switching transistor from transients due to the external circuitry. Due to the minimized trade-off with respect to the ON-state resistance of the overall device it maximizes switching efficiency.

Recently, discrete protection diode has been combined with AlGaN/GaN HEMT on the same chip [139]. An AlGaN/GaN HEMT with integrated recessed Schottky protection diode is demonstrated for the first time. From simulation we propose the structure shown in Figure 7.1–1. The Schottky metal drain contact is connected to the HEMT's 2DEG by recessing the drain contact and complete removal of the AlGaN barrier layer so that the Schottky drain contact metal is connected directly to the GaN buffer. The recess reduces the forward voltage onset and can reduce the ON-state power loss in diodes for power applications [140]. The device takes advantage of the good electrical connection between the Schottky metal and the GaN buffer in forward bias that is introduced by the high mobility the electrons spilling into the buffer at the vicinity of the drain electrode during the high field condition [79]. This results in a high conductivity in forward direction of the Schottky-drain diode.

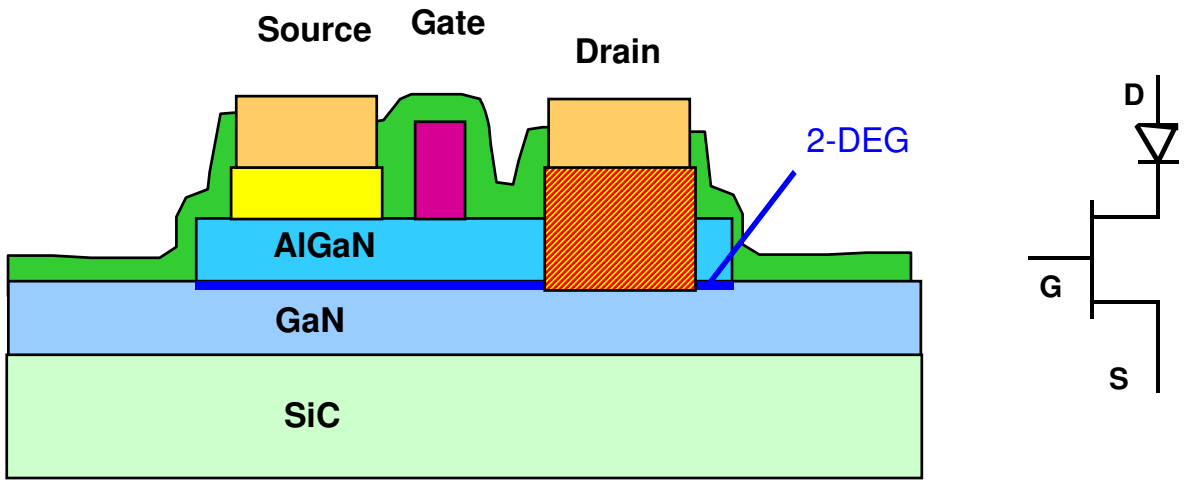


Figure 7.1–1 Schematic sketch of the AlGaN/GaN HEMT with fully recessed AlGaN in the area of the drain contact and the equivalent circuit.

7.1.1. Class-S GaN Switch-Mode Amplifiers

The efficiency of next generation microwave communication amplifiers can be

substantially increased by introducing switch-mode concepts [138]. A recent switch-mode variant in the microwave frequency range is the class-S concept: the analog input signal is converted to a digital signal using a band-pass delta-sigma modulator (BP-DSM). The digital signal is amplified using a high-efficiency power switch. Commonly, DSM is employed in A/D converters. As a part of the high-efficiency amplification chain here, it is rather used as a signal modulator. It transforms a given narrow-band signal into a two-state digital bit stream used as input signal for the power switching stages. An analog band-pass filter is applied at the output of these switching stages to reconstruct the analog signal. For such amplifiers, GaN is the most promising technology today [141] because it combines high breakdown voltage with high speed. Of course, efficiency of the switching stages is very important. In addition, the filter topology and the output network are key elements for the overall efficiency as they operate directly on the output signal.

Figure 7.1–2 presents the class-S concept. It follows a digital approach for power amplification: The analog input signal around f_0, which can be WCDMA, OFDM, etc. or a common harmonic sinusoidal signal is converted to a digital one by means of a band-pass delta sigma modulator (BPDSM). Its sampling frequency corresponds to the bit rate of the resulting digital signal. It is determined by the over-sampling ratio and is typically 4 times the signal frequency f_0. This bit sequence is then amplified by means of power switching stages and the analog signal is reconstructed by means of a filter at the out-put. In the present approach we use a current–mode class-S topology for the output stage; with the 2 transistors S_1 and S_2 operated in differential mode and a floating load (see Figure 7.1–3). The transistors are fed by DC current sources I_n. The filter must be of the parallel resonance type, with high impedance at f_0 and ideally zero impedance elsewhere. This causes the resulting voltage over the load to be narrowband and thus of sinusoidal shape. As the transistors ideally act merely as a switch, the dissipated power within the transistor remains zero and, for lossless filtering, the PAE can theoretically reach 100% independently of the output power level.

Advanced highly efficient amplifier architectures, for example class-S topologies, require fast switching power transistors in combination with appropriate protection diodes to shield the switching transistors from transients originating from external circuitry such as reconstruction filters. If high voltage negative pulses appear at the drain terminal, the switching transistor would be operated in the third quadrant for a short time which could either damage the device or cause additional dispersion effects which would slow down the transistor switching speed (see Figure 7.1–4). For Current Mode Class-S amplifiers (CMCS) fast protection diodes need to be connected in series to the switching transistors (see Figure 7.1–1). Such diodes have to be fast enough to prevent the transistors from operating in the third quadrant and, at the same time, provide only a minor contribution to the over all ON-state resistance of the switching transistors. A possible solution is the monolithic integration of switching transistor and Schottky diode according to Figure 7.1–1. In this case the drain electrode is replaced by a recessed Schottky contact which provides an optimum contact to the 2DEG region of the transistor in ON-set and results in effective blocking capability if the device is biased in OFF-state.

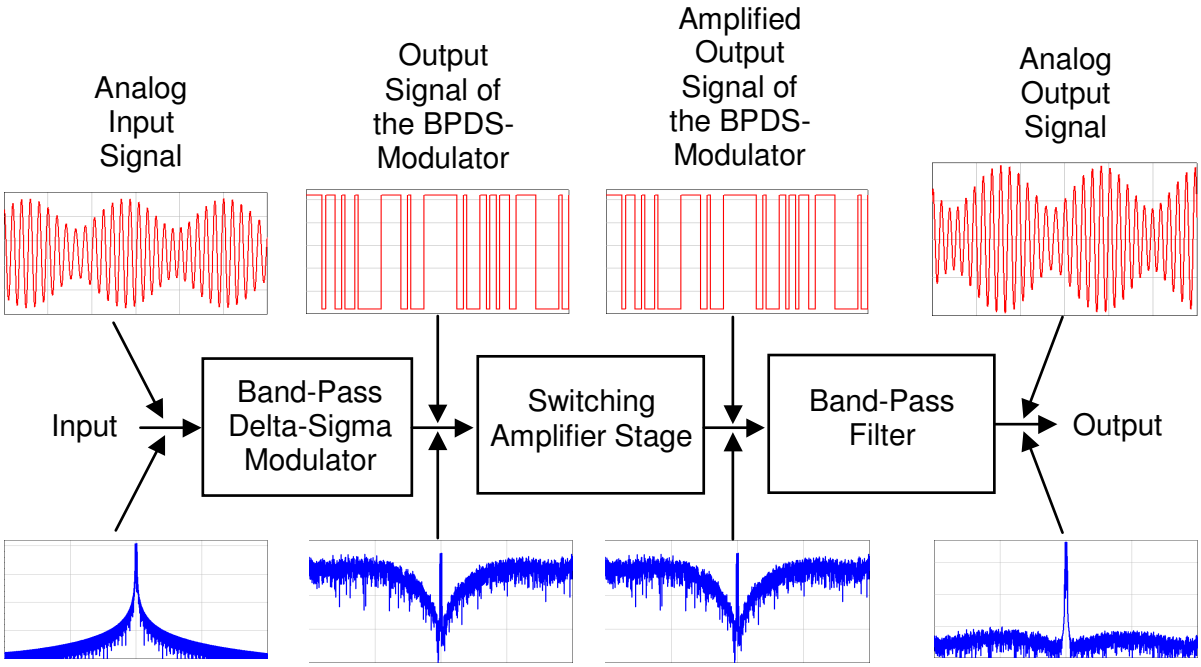


Figure 7.1–2 Class-S switching amplifier schematic operation.

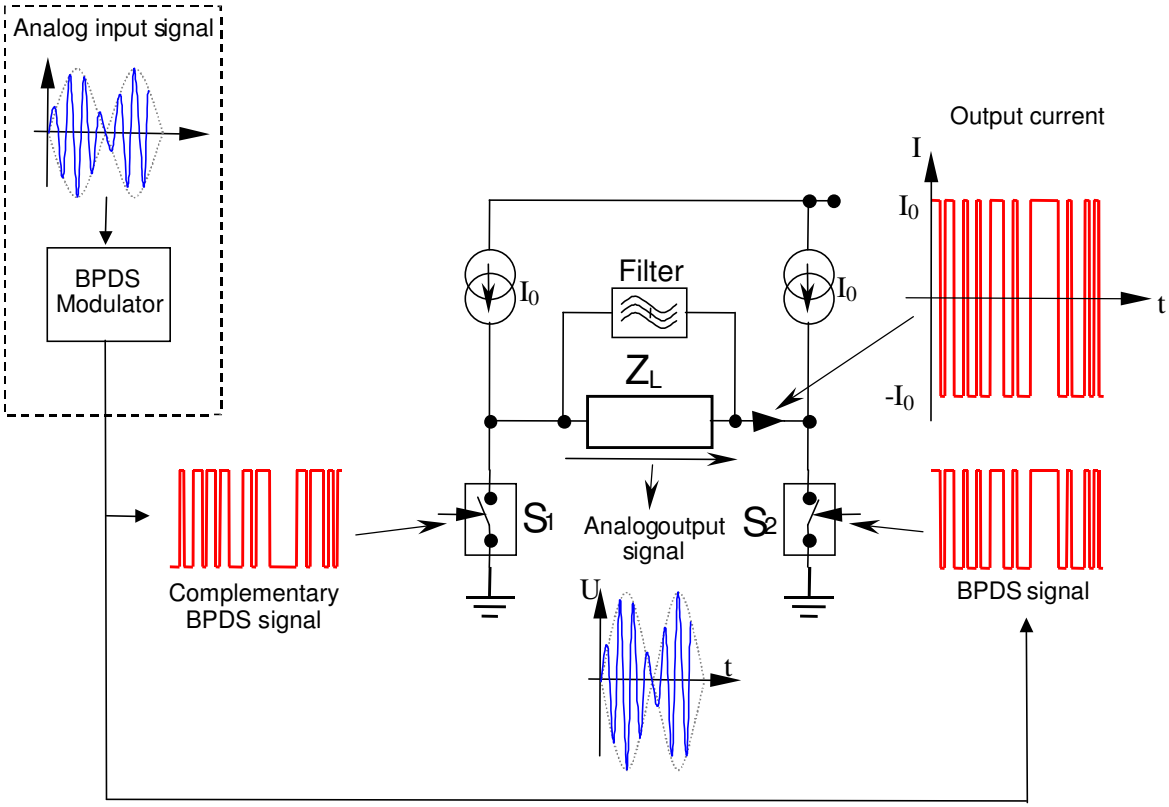


Figure 7.1–3 Output stage and main components of a class-S amplifier in current-mode configuration.

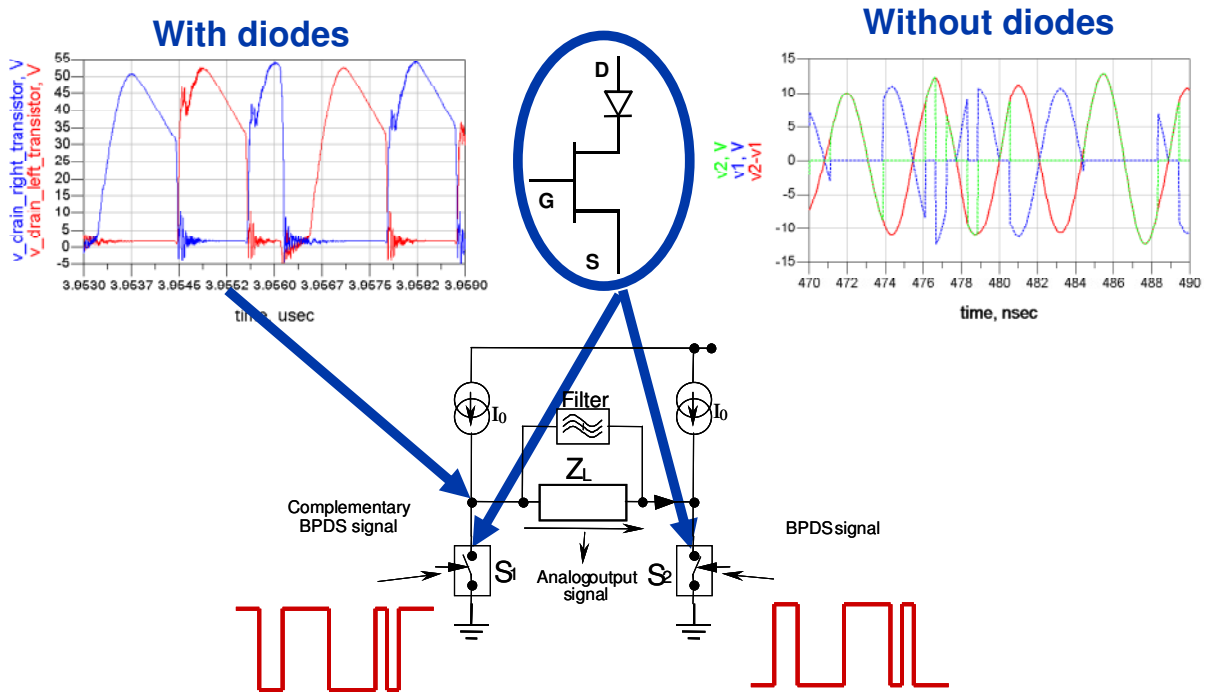


Figure 7.1–4 Output stage and main components of a class-S amplifier in current-mode configuration; Schottky diodes connected in series to the switching transistors, S_1 and S_2, prevent the transistors from operating in the third quadrant.

7.1.2. Integrated Recessed Schottky-Drain Electrode Concept and Simulation

Two dimensional physical-based device simulations (Silvaco-"ATLAS") [59] are performed to get an insight to the recessed Schottky drain contact HEMTs. The simulation follows the measurement sequence of the measurement for ON-state condition in forward and reverse bias. The simulated logarithmic electron concentration, n_e, in the device for the different conditions is logged. The simulation is consistent with the experimental findings. An onset current flow due to the Schottky-drain diode and the reverse blocking capability for the ON-state of the Schottky-drain HEMT is obtained. During forward bias (Figure 7.1–5(a) and Figure 7.1–6(a)) most of the electrons are travelling in the 2DEG region, however some of them are electrons are injected from the 2DEG into the GaN buffer due to the presence of high electric fields. Once injected into the buffer the electrons experience quite a high mobility. This means that in addition to direct contact of the Schottky drain electrode to the 2DEG the highly mobile electrons in the GaN volume are able to bypass a potential gap between 2DEG and Schottky metal by just being injected into the GaN buffer thus providing a drain connection with low ON-resistance. On the other hand during reverse drain bias (Figure 7.1–5(b) and Figure 7.1–6(b)), as in a protection diode mode, a strong depletion of electrons in the surroundings of the Schottky drain electrode can be seen, preventing reverse current and by that protecting the transistor.

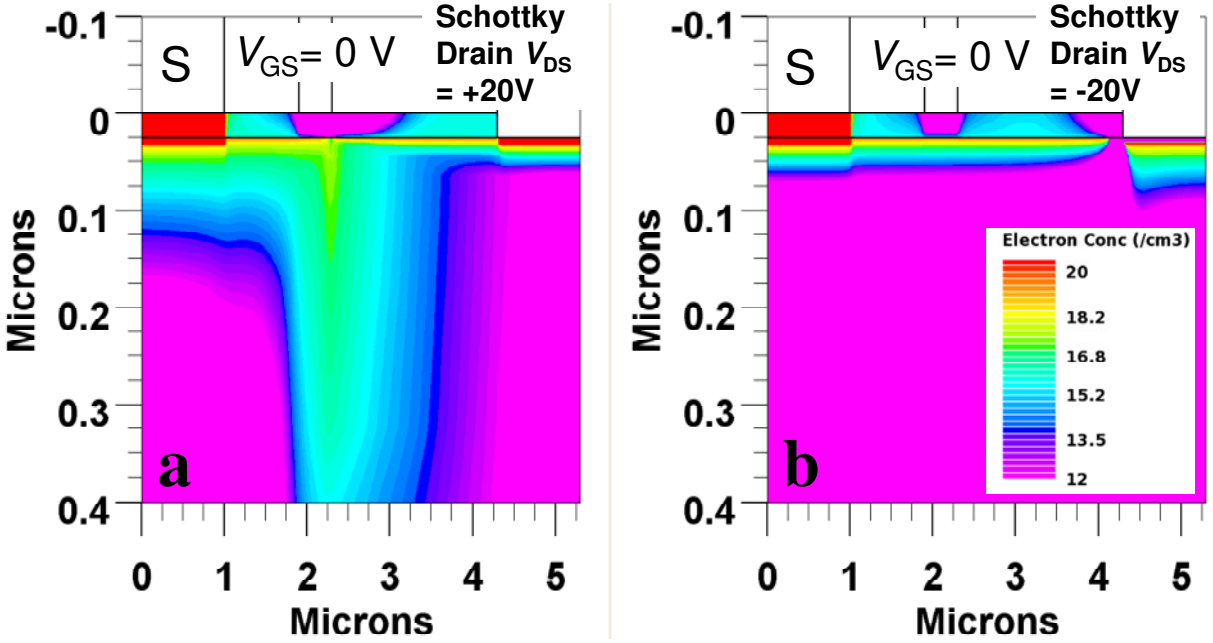


Figure 7.1–5 Electron distribution in simulated AlGaN/GaN HEMT with integrated recessed Schottky-drain electrode (a) in forward bias V_{DS} = +20 V condition (b) in reverse bias V_{DS} = -20 V condition.

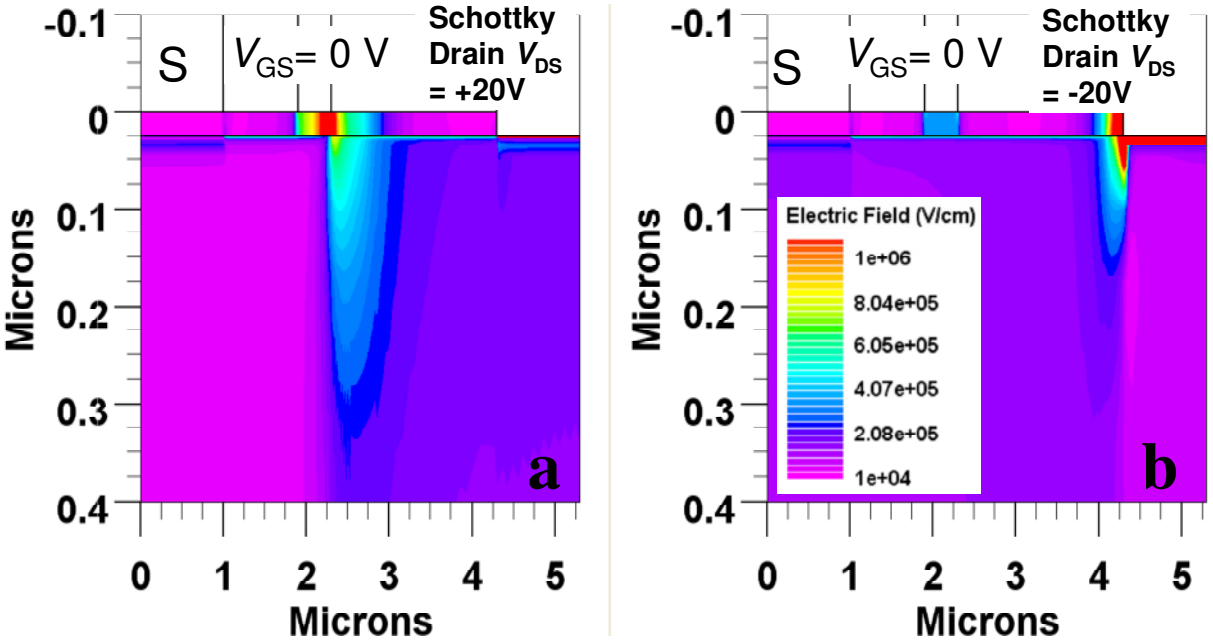


Figure 7.1–6 Electric field distribution in simulated AlGaN/GaN HEMT with integrated recessed Schottky-drain electrode ((a) in forward bias V_{DS} = +20 V condition (b) in reverse bias V_{DS} = -20 V condition.

7.2. Process Integration and Robustness of the Schottky Diode Formation

HEMT structures were grown by Metal Organic Vapor Phase Epitaxy (MOVPE) on semi-insulating SiC-substrates having AlN nucleation layer followed by 1400 nm unintentionally doped (UID) GaN-buffer layer and a 25 nm UID AlGaN barrier layer containing 0.24 Al mole fraction on top.

Field-effect transistors were fabricated on the wafer. Source-ohmic contacts ware made by evaporating Ti/Al/Ti/Au with a sputtered WSiN-layer on top to provide smooth pattern

delineation after RTP at 830°C. Mesa insulation was performed using Cl_2/BCl_3 reactive ion etching. Drain trenches for the Schottky contacts were defined by electron beam lithography and the AlGaN layer was recessed by using BCl_3 based reactive ion etching. Two etch durations were investigated which correspond to 26 nm and 32 nm etching depth, respectively. The Schottky contacts use Pt/Ti/Au stack metallization aligned to the etched trench. The T-shaped gate defined by electron beam lithography has a footprint of 0.4 µm using Pt/Ti/Au stack for the Schottky barrier metal. The Pt/Ti/Au stack that serves as a Schottky contact metal provides a barrier height of 0.65 eV. The HEMT structures were passivated with SiN_x from PECVD and finally connection and plating layers were fabricated.

7.3. DC Characterization and Measurements

DC-output characteristics of the ON-state (V_{GS} = 0 V) and threshold-state (V_{GS} = -4 V) of forward and reverse bias is shown in Figure 7.3–1 and Figure 7.3–2. The tested devices were 2 × 125 µm wide with gate-drain spacing L_{GD} = 6 µm and gate-source spacing L_{GS} = 1 µm. The reverse blocking capability for both on and threshold states of the Schottky-drain diode is higher than -110 V. The ON-state operation shows an ON-set, where I_{DS} = 1 mA/mm, of current flow due to the Schottky-drain diode at 1.0 V drain voltage. Characterization of the HEMT devices reveals an average saturation current of 1.2 A/mm and average maximum transconductance of 290 mS/mm (Figure 7.3–2). Comparable numbers are obtained for devices using customary ohmic drain contacts. The average device breakdown was measured at V_{GS} = -6 V was 40 V limited by a drain current of 1 mA/mm. The ON-state resistance (R_{ON}) defined as the reciprocal of the *I-V* curve's slope at the steepest position and the drain saturation current ($I_{DS\ max}$) of the two recess depths applied to the properties of the reference device are compared (Figure 7.3–3). The wafer average measured R_{on} are 3.97 ± 0.10 Ω·mm, 4.48 ± 0.08 Ω·mm and 3.21 ± 0.16 Ω·mm and the measured $I_{DS\ max}$ are 1.15 ± 0.22 A/mm, 1.16 ± 0.19 A/mm and 1.18 ± 0.18 A/mm which correspond to 26 nm, 32 nm recess depth and standard ohmic drain contact respectively. These values reflect the robustness of the contact recess process as will be discussed later.

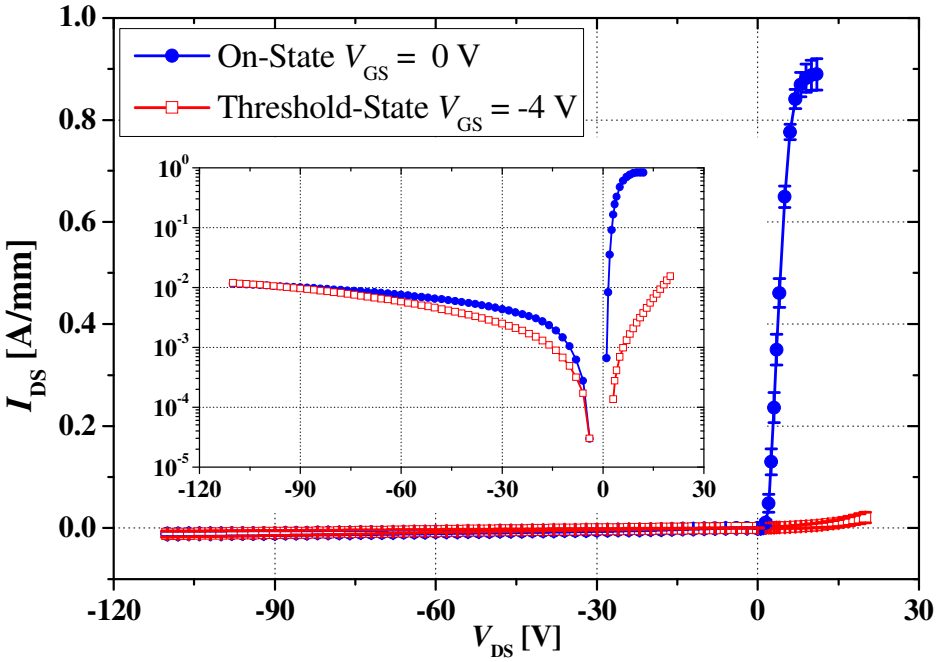


Figure 7.3–1 Output characteristics in ON-state (V_{GS} = 0 V) and threshold-state (V_{GS} = -4 V) showing reverse blocking due the integrated diode. Inset the same in logarithmic scale.

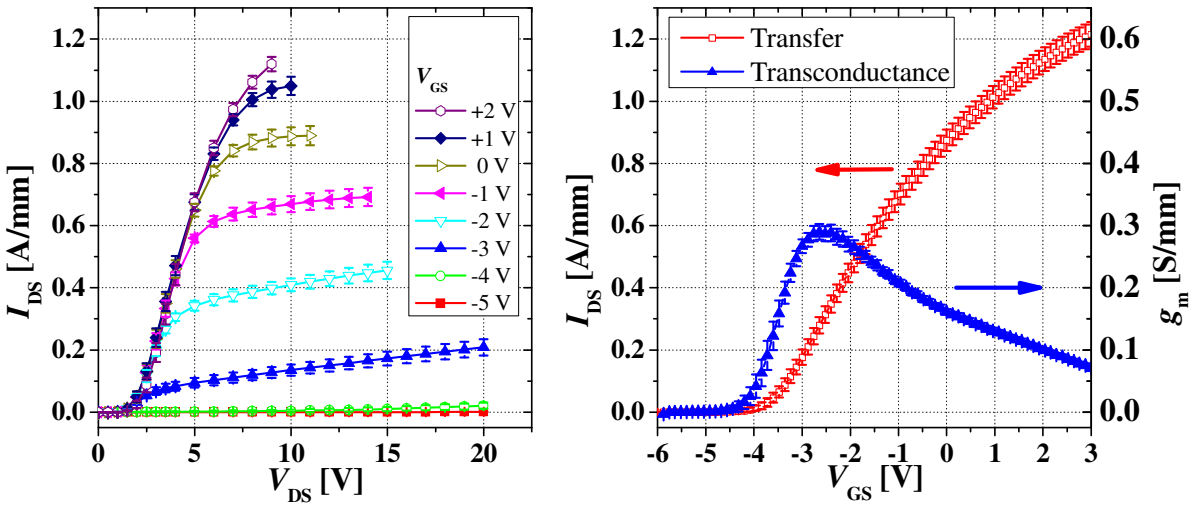


Figure 7.3–2 (on the left) Detail of wafer average output characteristics showing onset of drain current at $V_{DS} = 1.0$ V. (on the right) Wafer average transfer at $V_{DS} = 15$ V characteristics and transconductance of GaN HEMTs with recess Schottky drain. Error bars represent standard deviation of the measurements.

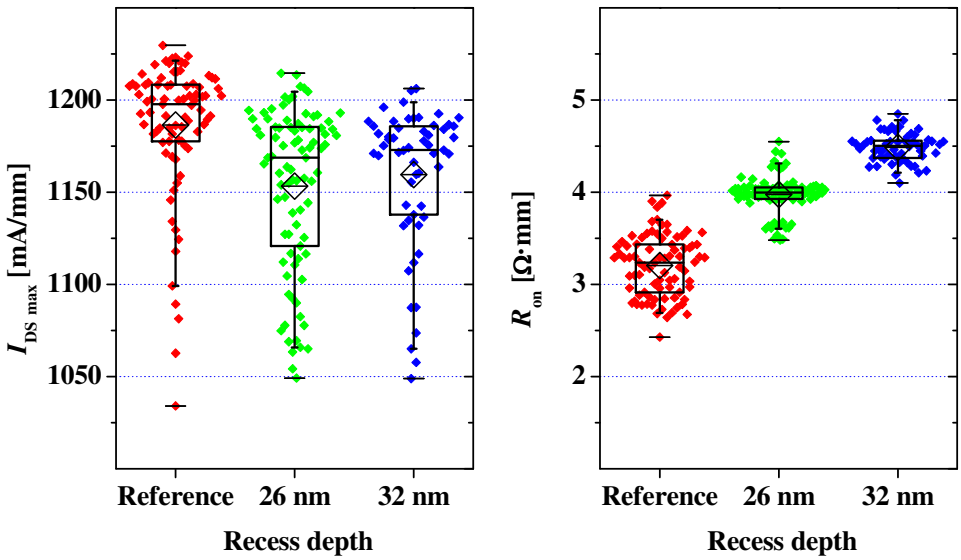


Figure 7.3–3 Comparison of ON-state resistance (R_{ON}) and drain saturation current $I_{DS\ max}$ between standard ohmic drain contact and recess Schottky drain contacts with 26 nm and 32 nm recess depth.

7.4. Test of Microwave and Switching Capabilities

RF-characterization from load-pull measurements in class AB operation at 2 GHz (shown in Figure 7.4–1) of GaN based HEMT with integrated recessed Schottky drain device , reveal a saturated output power density of 9.5 W/mm with 65 V drain bias (2 × 125 µm finger width, field plate 1 µm), power added efficiency, PAE, of 42% and 23 dB unilateral gain. The reference device with the same dimensions and measurement conditions leads to 9.9 W/mm, 46% PAE and 25 dB gain. By a drain bias of 28 V the saturated output power density of 4.5 W/mm with PAE of 41% and unilateral gain of 24 dB is measured. The reference device shows out put power of 4.9 W/mm, 53% PAE and gain of 24 dB.

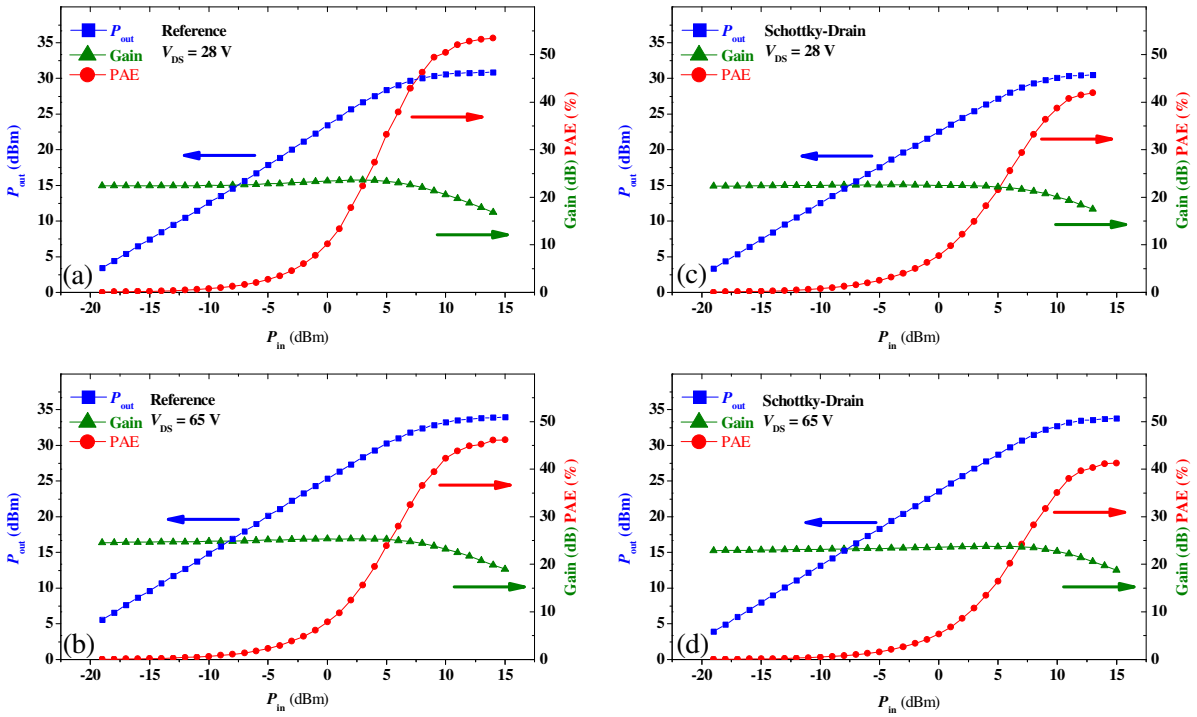


Figure 7.4–1 Output power measured in class AB operation by 2 GHz load-pull setup (2 × 125 µm finger width) of (a) a reference HEMT-device in V_{DS} = 28 V, (b) a reference HEMT-device in V_{DS} = 65 V, (c) a HEMT-device with integrated Schottky drain-diode in V_{DS} = 28 V and (d) a HEMT-device with integrated Schottky drain-diode in V_{DS} = 65 V.

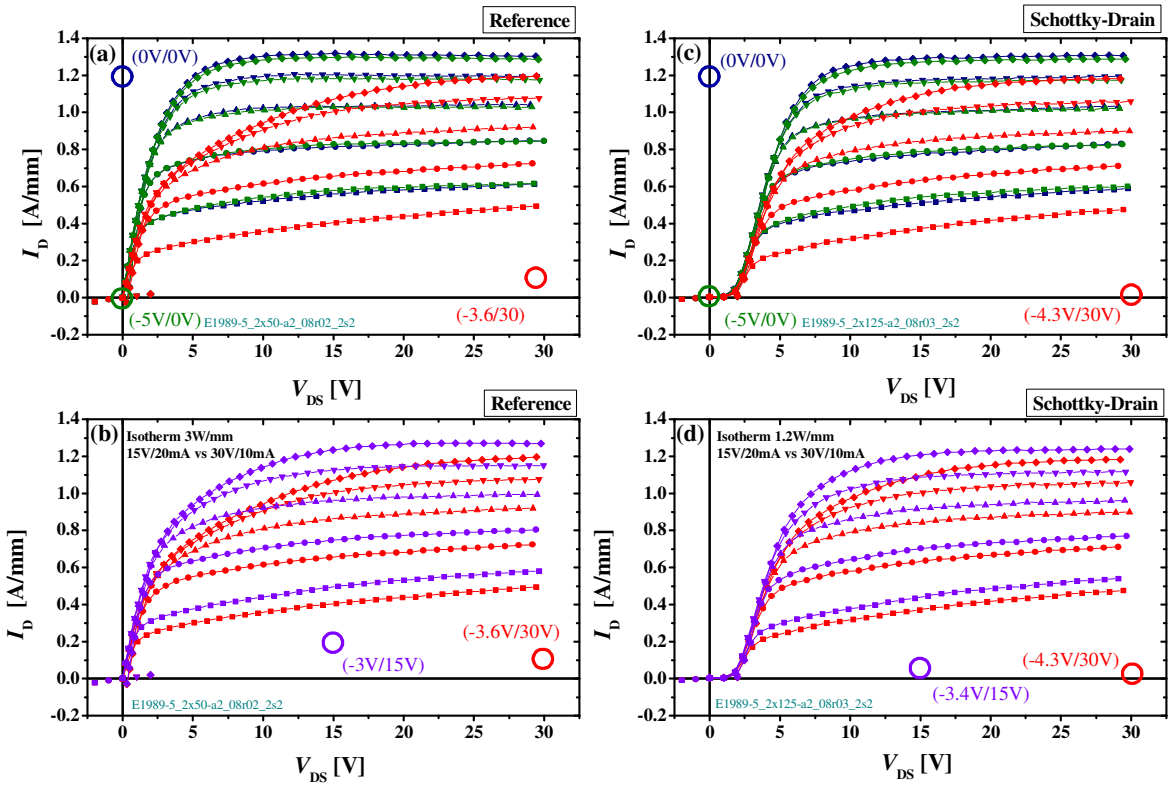


Figure 7.4–2 200 ns pulsed *I-V* (DIVA) measurements of ((a) and (b)) 2×50 µm, L_{GD} = 2 µm reference device and ((c) and (d)) 2×125 µm, L_{GD} = 2 µm with integrated Schottky drain-diode device. $V_{GS\,max}$ = +2 V and ΔV_{GS} = 1 V. DIVA quiescent points V_{GS} = 0 V, V_{DS} = 0 V (blue dot), V_{GS} = -5 V, V_{DS} = 0 V (green dot), V_{GS} (I_{DS} = 10 mA), V_{DS} = 15 V (lilac dot), and V_{GS} (I_{DS} = 20 mA), V_{DS} = 30 V (blue dot).

Representative example of 200 ns pulsed *I-V* (DIVA) measurements for devices with integrated recessed Schottky drain configuration and reference device is shown in Figure 7.4–1. The pulsed measurements were done with four quiescent bias points; at [V_{GS} = 0 V, V_{DS} = 0 V], at [V_{GS} = -5 V, V_{DS} = 0 V], at [V_{GS} (I_{DS}= 20 mA), V_{DS} = 15 V] and at [V_{GS} (I_{DS}= 10 mA), V_{DS} = 30 V] to emphasize the drain and gate current lag at operation conditions; as demonstrated no significant difference, excluding the drain onset, between reference device and the device owning integrated recessed Schottky drain could be seen.

In order to evaluate the switching capabilities, the Schottky-drain HEMT is tested under operating conditions comparable to those in a class-S amplifier, or in another comparable switch-mode amplifier (such as class-D for example) using an appropriate sequence of bit pattern. In class S amplifiers the input signal is supplied from a Band Pass Delta Sigma (BPDS) modulator. A switching power stage amplifies this signal, which is finally converted back by a reconstruction filter. For actual device testing, the BPDS signal has been provided by a bit pattern generator. According to Figure 7.4–3 the BPDS signal has been fed into the drain terminal of the Schottky drain transistor. This configuration emulates pulses coming back from the reconstruction network in real class-S amplifier environment. The BPDS signal applied at the drain forces a current flowing from the drain to the source. Its magnitude depends on the blocking capability of the Schottky drain diode. The ohmic resistance of the transistor channel probes the diode current. Therefore, the gate electrode acts as a voltage divider, where the RF diode current can be measured in time domain. The gate DC-supply V_{GS} is set to keep the gate diode in fully open condition (V_{GS} = +2 V). During measurement the drain potential V_{DS} is ramped form negative values (-10 V) to positive values (+10 V). At negative drain voltage the Schottky drain is operated in OFF-state at positive drain voltage in ON-state conditions. At OFF-state the BPDS pulses should be effectively blocked by the diode and thus not be visible at the gate probing terminal. The tests have been performed at a BPDS data rate of 2 Gbps and monitored by time domain measurements as displayed in Figure 7.4–4. At diode ON-state conditions the wave form of the bit pattern is not affected by the introduction of the Schottky-drain diode. At OFF-state conditions the clipping of negative pulses for a BPDS bit pattern up to 2 Gbps is clearly observed.

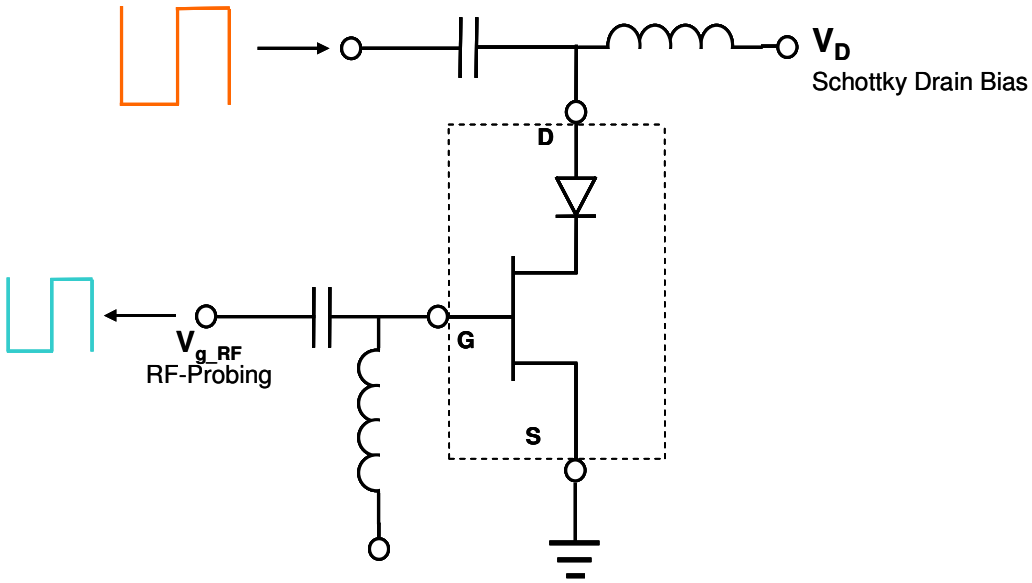


Figure 7.4–3 Measurement set-up for the verification of the clipping performance of the Schottky-drain diode: Microwave signal and DC-bias V_{DS} are feed into the Schottky-drain. The resistivity of the transistor channel probes the diode current. This corresponds to the drain to source current with the gate acting as a voltage divider. The gate DC-supply V_{GS} is set to keep the gate diode in fully open condition and thus the gate-source resistance probes a voltage proportional to the drain current.

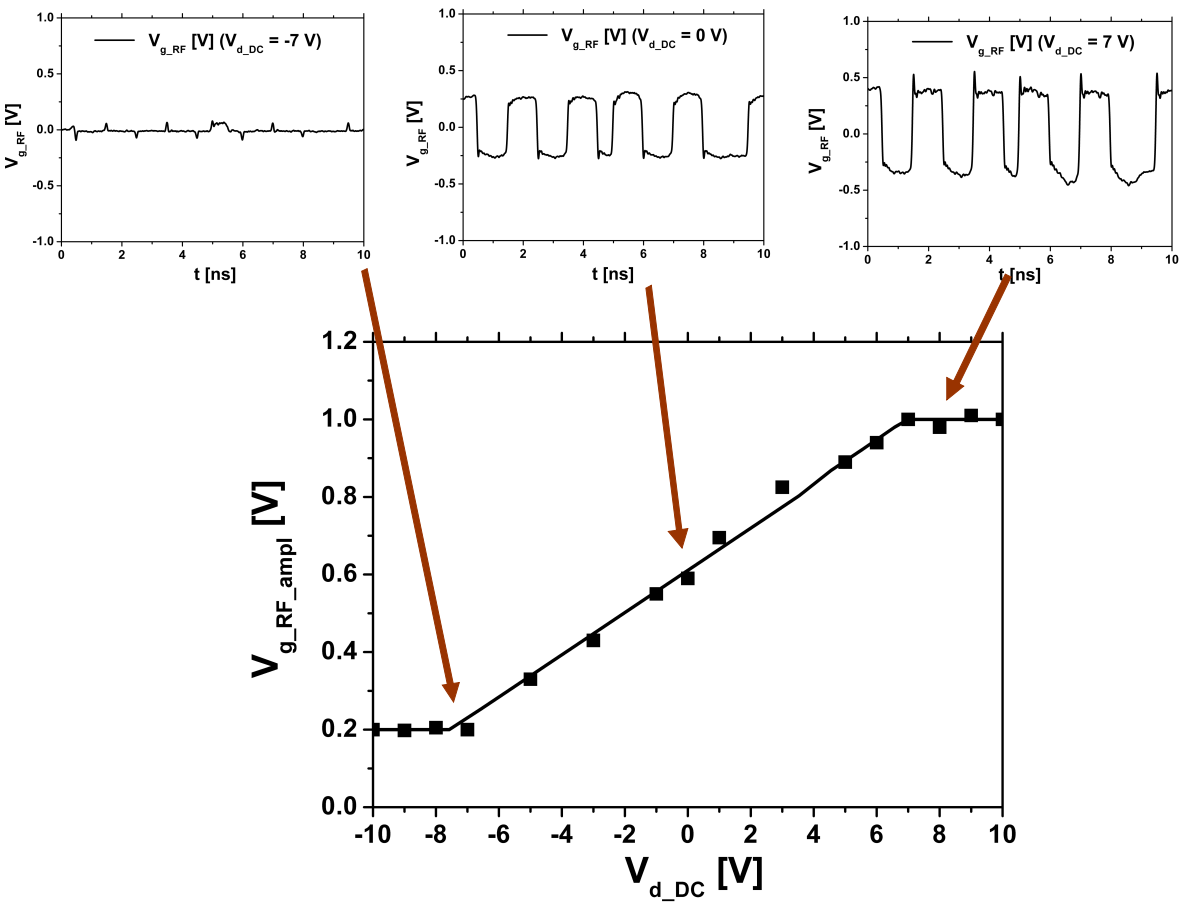


Figure 7.4–4 Verification of complete waveform clipping of the negative current by the drain diode shown with a BPDS pattern at 2 Gbps. The input square signal amplitude is set to a voltage swing of 14 V_{PP}. The bias voltage on the drain shifts the square signal forcing the diode to clip the negative portion. Squares represent measurements; the line is intended to guide the eye.

7.5. Discussion and Conclusions

The intention of the AlGaN/GaN HEMTs with protection diode is to prevent a current flow in the transistor during reverse bias conditions in switching devices. Replacing the planar drain ohmic contact by a Schottky metal without recess will show the desired reverse blocking but with the disadvantages of very high ON-resistance and often poor blocking in reverse bias. The realization of a good Schottky diode is possible when the AlGaN barrier underneath the metal is completely removed and a contact of the Schottky metal to the 2DEG and/or GaN semiconductor buffer layer is achieved. Simulations and measurements have shown that in addition to direct contact the 2DEG from the side of the Schottky drain electrode, electrons are injected to the GaN buffer under the Schottky metal and contact it. Due to high field assisted electron injection into the buffer it is also possible to slightly etch through the 2DEG region without too much penalty in the ON-state resistance. This provides quite a safe process window for device fabrication. At forward drain bias conditions a deep potential drop creates a high field condition in the vicinity of the drain electrode. This field allows the electrons to spill over in to the high resistive GaN buffer where they have such a high mobility that allows them to flow towards the drain electrode. In reverse drain bias the Schottky potential barrier depletes the GaN buffer close to the drain and the electrons cannot get injected into the buffer. Any further increase of the reverse potential increases the

depletion depth and the drain diode blocking is improved.

In addition there is a big advantage in process robustness of the recessed drain Schottky electrode. Simulation shows that the current flow into the Schottky drain is distributed across some nanometers of depth and extends the thickness of the 2DEG. The complete etching of the AlGaN barrier has therefore not necessarily to be stopped exactly at the AlGaN/GaN interface. Some over-etching is acceptable with only low penalty in the device performance. This gives the concept of the recessed Schottky drain diode pronounced process robustness.

A demonstration of AlGaN/GaN HEMT with integrated protection Schottky diode is presented. The results of the innovative Schottky-drain HEMT demonstrated an excellent reverse blocking with minor trade-off in the ON-state resistance for the complete device. A reverse blocking capability of the diode was better than –110 V demonstrated with excellent quality of the forward diode characteristics. The demonstrated recess process showed high robustness and low influence on the electrical DC characteristics.

Chapter 8

Process Development for High Voltage Operation Devices

The GaN superior material breakdown strength properties are not always a guarantee for high voltage devices. In addition to superior epitaxial growth design and optimization for high voltage, (HV), operation the device geometrical layout design and the device manufacturing process design and parameters optimization are important criteria for breakdown voltage enhancement. In this chapter an example for HV test device layout design and example for critical inter-device insulation manufacturing process optimization are presented.

8.1. Layout Design of GaN-Based HEMTs for High Voltage OFF-State Operation

GaN-based power switching devices are successors to advanced GaN based microwave, (MW), power amplifiers devices. For continuity and bench marking, in many cases, the same devices layout and manufacturing process were useful for the development of the HV power switching devices. However, with the enhancement of the device OFF-state blocking voltage the limitations and week points of the MW test device were emphasized. As a result much lower breakdown voltage than the designed was achieved therefore a new design inevitable. In this section the new layout design for the HV test devices is presented. The new strict design criteria that prevent undesired catastrophically premature breakdown are demonstrated experimentally.

8.1.1. Geometrical Layout Modifications for High Voltage Devices

High voltage test devices require a strict design rules for maximal separation of the high and low voltage conduction metal lines. In addition, avoiding creation of conductor metal with sharp corners is crucial. These corners accumulate extremely high electric field that would be the source of breakdown initiation process.

One of the pronounced premature failures was electrical arcing between the high voltage biased metal pads, drain, and other metal pads, gate and source. In order to avoid such arcing the source contact pads were shorten and the drain pad is left laterally isolated. This is the most visible modification of the HV test device. Figure 8.1–1(a) and (b) depicts the top view of the MW and the HV test devices and Figure 8.1–1(c) and (d) depicts SEM micrographs of same manufactured devices, here the large scale changes in the pads are observed.

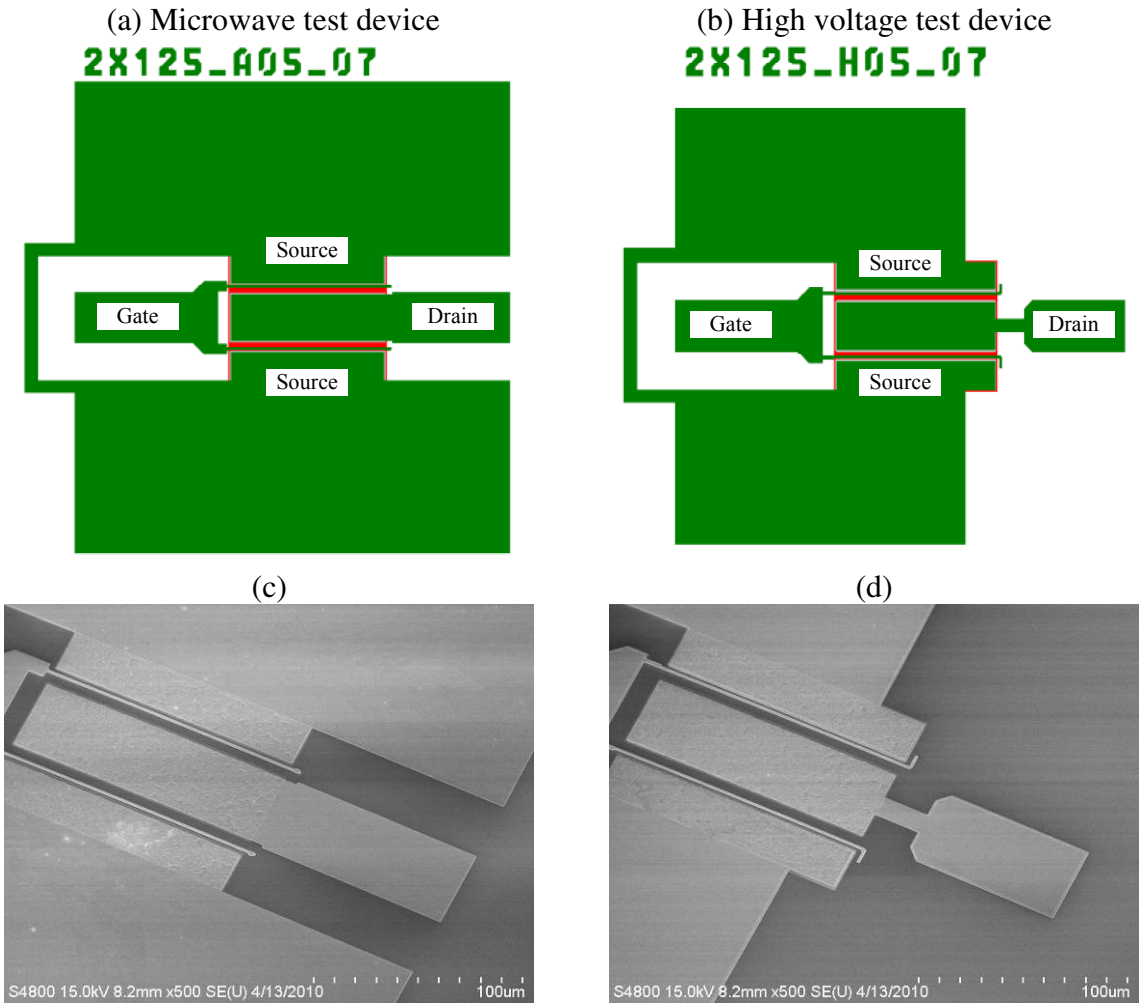


Figure 8.1–1 Layout design and SEM micrographs of manufactured devices with 2 × 125 µm gate width and $L_{DG} = 5$ µm GaN based HEMT for (a), (c) microwave test device (b), (d) high voltage test device.

The modification of the drain ohmic metal contact on the active area is illustrated in Figure 8.1–2. here the four corners in the layout of pad were trimmed. Such trim in the layout will be translated after the lithography and liftoff process into an approximately rounded figure. The resulting processed rounding of the drain ohmic metal contact could be observed in the SEM micrograph in Figure 8.1–3(d).

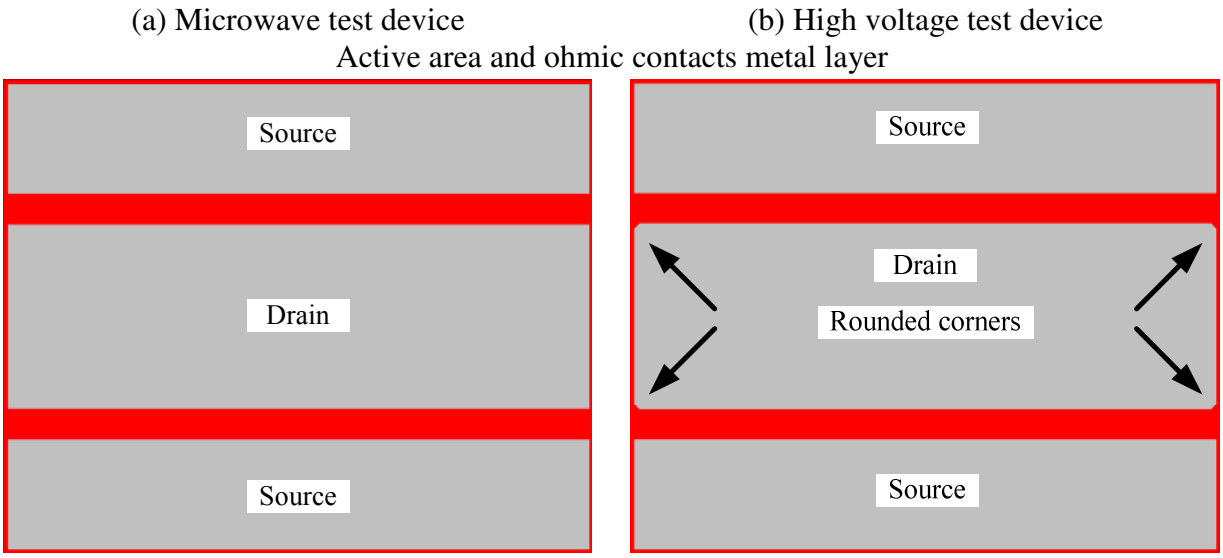


Figure 8.1–2 Active area (red) and ohmic contacts (gray) layout design of devices with 2×125 µm gate width and $L_{DG} = 5$ µm GaN based HEMT for (a) microwave test device (b) high voltage test device with rounded corners.

The layout design of the gate side pads of the test devices is illustrated in Figure 8.1–3(a) and (b) for the MW and the HV test devices respectively. Figure 8.1–3(c) and (d) depicts SEM micrographs of resulting same manufactured devices. Here the gate pad is laterally separated from the drain ohmic contact metal. The gate fingers are connected continuously to the gate metal pad any sharp corners removed.

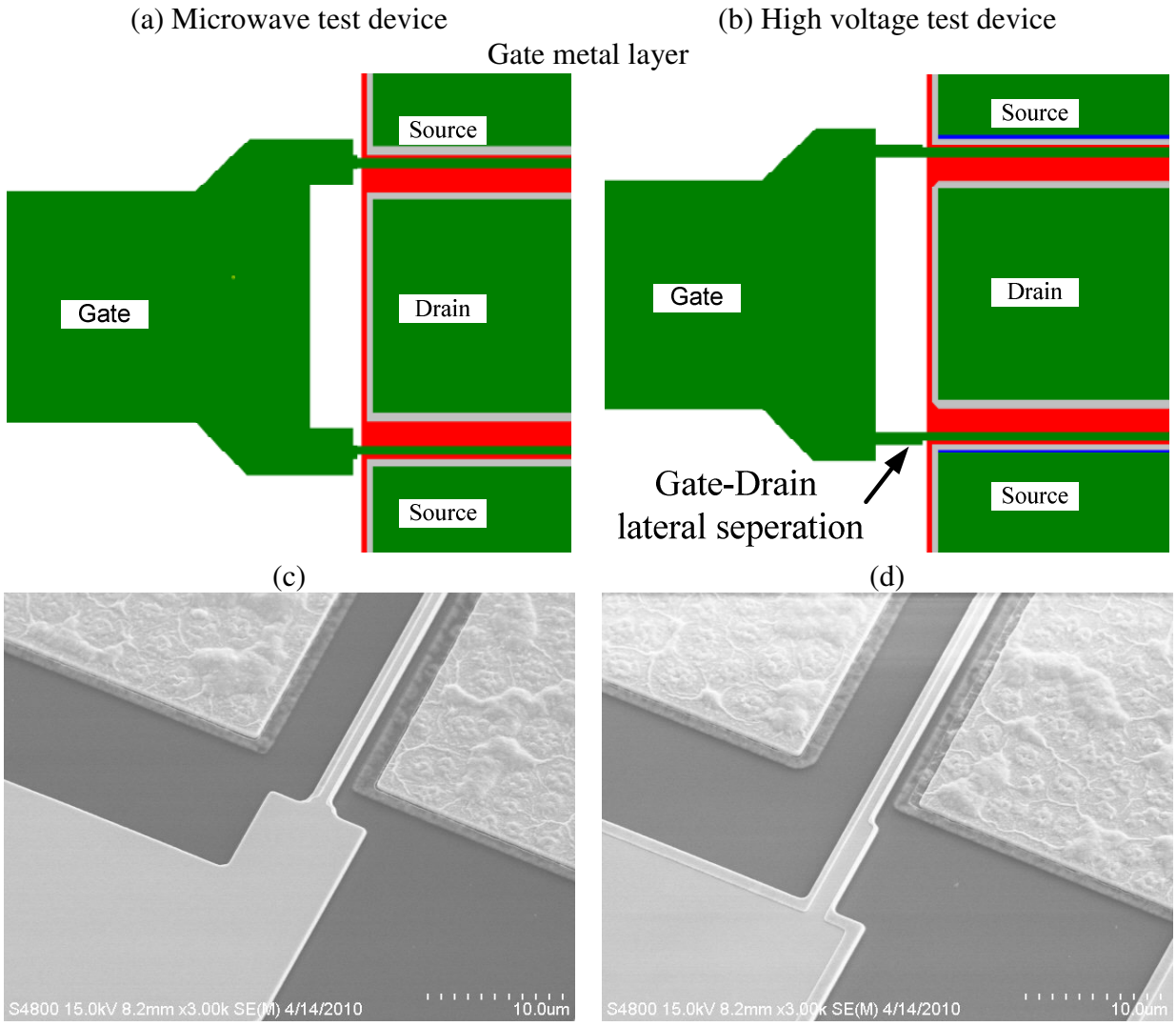


Figure 8.1–3 Gate pad and gate metal connections layout design and SEM micrographs of manufactured devices with 2×125 µm gate width and $L_{DG} = 5$ µm GaN based HEMT for (a), (c) microwave test device (b), (d) high voltage test device.

The layout design of the drain side pads of the test devices is illustrated in Figure 8.1–3(a) and (b) for the MW and the HV test devices respectively. Figure 8.1–3(c) and (d) depicts SEM micrographs of resulting same manufactured devices. Here the drain pad was redesigned for high voltage operation. The connection between the pad and the drain ohmic contact is narrowed and the corners of the pad are also trimmed to achieve maximal separation from the gate extensions. The gate extension was designed as a guard ring to separate and protect the source ohmic contact from the drain pad. This guarding extension should generate a additional depletion above the inter-device insulation and prevent such leakage from the source to the drain.

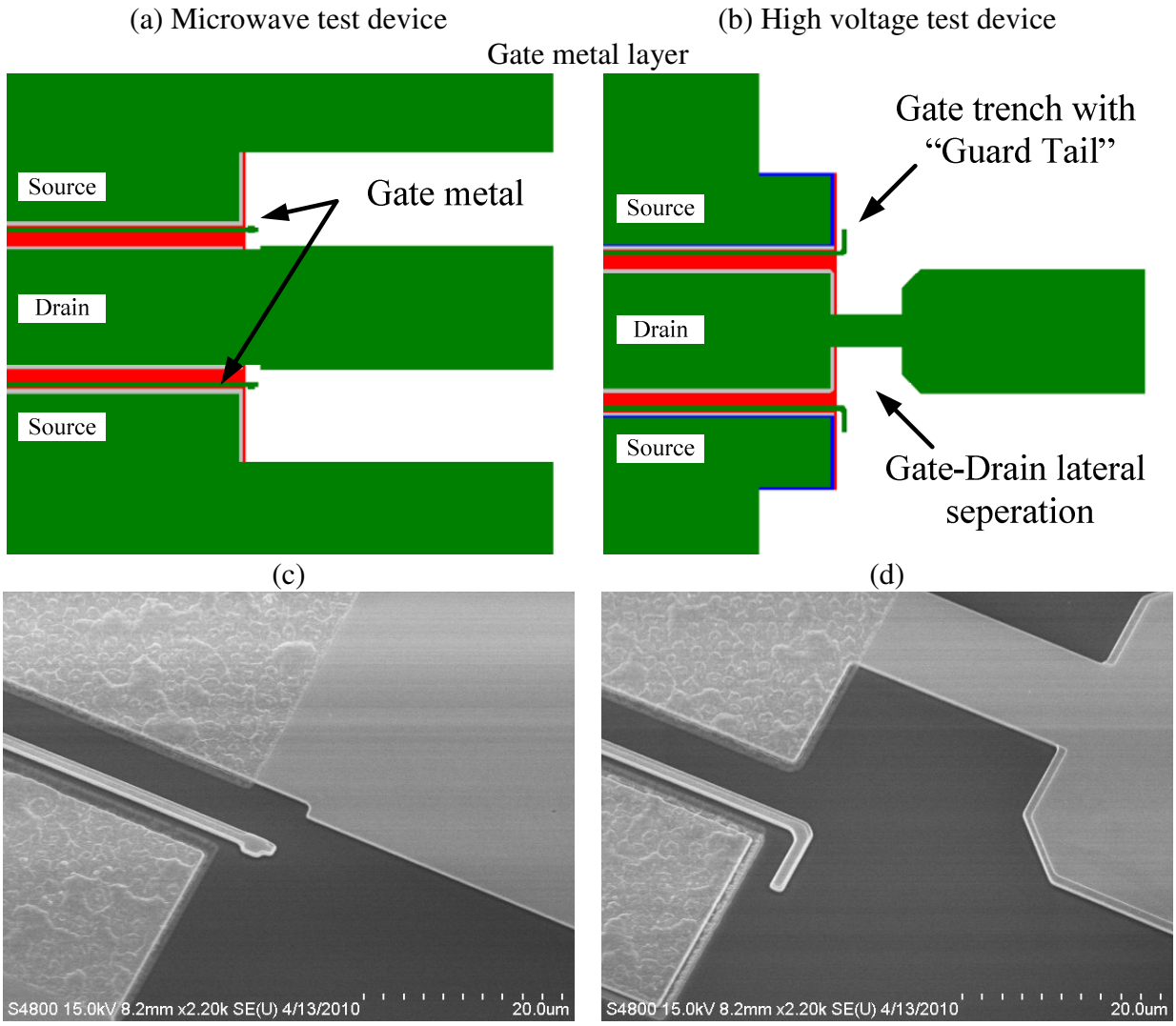


Figure 8.1–4 Drain pad layout design and SEM micrographs of manufactured devices with of 2 × 125 µm gate width and L_{DG} = 5 µm GaN based HEMT for (a), (c) microwave test device (b), (d) high voltage test device.

8.1.2. Experimental DC and OFF-State Breakdown Measurements Results

Low voltage DC characterization measurements show statistical identity in all measured parameters, such as V_{Th}, $I_{DS\ max}$, R_{ON} etc., for the two types of layout designs. On the other hand significant difference in $V_{BR\ OFF}$ is observed and strongly dependent on the test device geometry.

The breakdown voltage $V_{BR\ OFF}$ of the devices was measured at OFF-state conditions below the device threshold bias $V_{Th} >> V_{GS}$ = -5 V. During the $V_{BR\ OFF}$ measurements, the devices were immersed in 3M^{TM} Fluorinert^{TM} Electronic Liquid FC-3283 [123] in order to avoid arcing through the air. The drain bias was increased in steps of 2 V and logged until breakdown was identified. The breakdown voltage was defined as the voltage at which the drain current exceeds the value of 1 mA/mm. The voltage limit of the measurement system is +/-1000 V. The wafers were placed on a grounded stage during the measurement. Figure 8.1–5(a) shows the results of sub-threshold drain-leakage and gate-leakage currents measurements for microwave, (MW) test devices and high voltage, (HV), manufactured on wafer "C" in Chapter 5 with L_{GD} = 5 µm. The samples were chosen from this wafer due to its high $V_{BR\ OFF}$ therefore the limitations of the layout design are clearly emphasized. The results show overall very low background sub-threshold drain leakage current, ~10^{-7} A/mm and even lower gate leakage current. For the MW test devices the gate leakage current increase rapidly above

500 V and for the HV test device it increases less rapidly at about 800 V resulting a breakdown voltage of 610 V and 930 V respectively.

Wafer-level statistical analysis of the breakdown voltage measurements for increasing gate-drain spacing, L_{GD}, on all types of wafers is shown in Figure 8.1–5(b). Constant increase of the breakdown voltage in several hundreds of volts for HV test devices is observed with median $V_{BR\ OFF}$ of 930 V for device with L_{GD} = 5 µm and median slope of 194 V/µm. As for the MW test devices and the same increase is observed for devices owning L_{GD} = 1 and 2 µm (in this case the higher $V_{BR\ OFF}$ compared to the HV test devices is a result of 0.1 µm larger L_{GD} in this design). For devices with 7 µm ≥ L_{GD} ≥ 3 µm a reduction in $V_{BR\ OFF}$ is observed with lower increasing rate and for devices with L_{GD} ≥ 8 µm the $V_{BR\ OFF}$ saturates at 920 V and is independent of the gate-drain spacing.

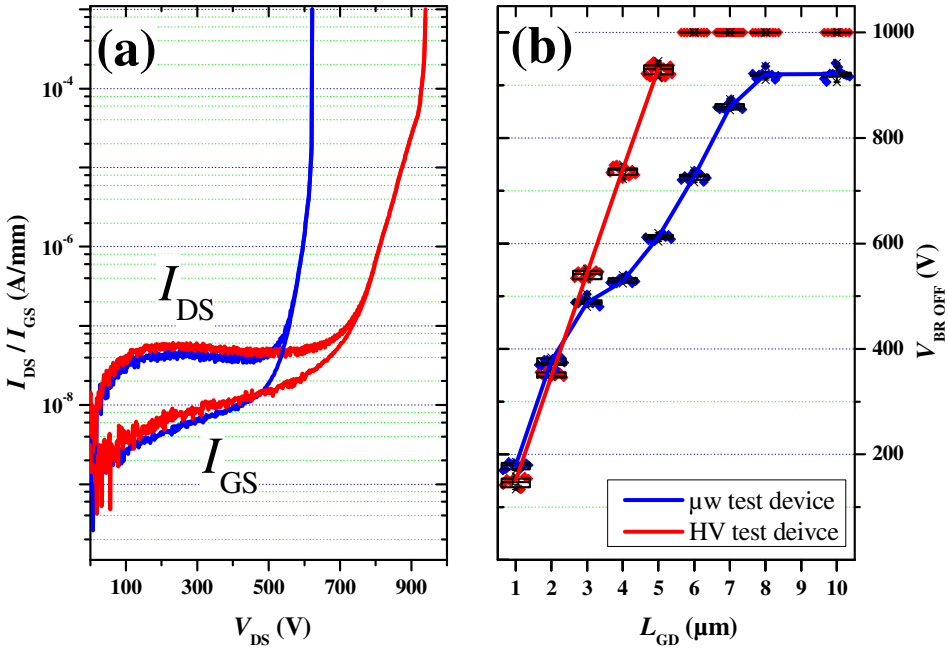


Figure 8.1–5 Example of breakdown voltage measurements of HFET devices with GaN:C $4e^{19}$ cm^{-3} back-barrier on SI-SiC substrate for test device with microwave layout design and test device with high voltage, HV, layout design. (a) Subthreshold currents output during $V_{BR\ OFF}$ measurements for devices with L_{GD} = 5 µm and W_G = 2 × 125 µm. (b) Wafer-level distribution of breakdown voltage for devices with gate-drain spacing of L_{GD} = 1 µm to L_{GD} = 10 µm. The measurement is limited by the current compliance of 1 mA/mm and drain bias V_{DS} = 1000 V measured at V_{GS} = -5 V.

8.1.3. Discussion and Conclusions on Geometrical Layout Design

Figure 8.1–6 depicts typical SEM micrographs of devices from both types of layout design with gate-drain separation of L_{GD} = 2 µm, 5 µm, 8 µm and 10 µm that exhibited destructive three-terminal OFF-state breakdown measurement. Here the destruction breakdown point is clearly observed. For devices of both types of layout design with gate-drain separation of L_{GD} = 2 µm the breakdown point is located in the active area of the device between the highly biased drain and the gate. Therefore for these devices equivalent breakdown voltage is achieved. As the gate-drain separation increases with 7 µm ≥ L_{GD} ≥ 3 µm the breakdown point of the MW test devices is located between the gate pad extension and the drain ohmic contact. This distance is shorter than the gate-drain spacing and it increases proportionally to it, therefore an increase of the device breakdown is observed but with lower slope. On the other hand for HV test devices the gate pads extensions were removed and the minimum distance of the gate-drain separation is kept and the breakdown occurs in the active area only.

For MW test devices with L_{GD} ≥ 8 µm the breakdown occurs between the gate and the highly biased drain pad. Here it is the minimal separation distance between the gate and the drain and it is constant with the increase of the gate-drain separation and therefore no additional increase of the breakdown voltage is possible and it reaches $V_{BR\ OFF}$ ≈ 920 V.

HV test devices with L_{GD} ≥ 6 µm did not reach their breakdown in this measurement setup due to it's +/- 1000 V limitation. This is an indication that the suggested HV layout that increases the separation between the high voltage conductors and the gate is essential for premature breakdown prevention.

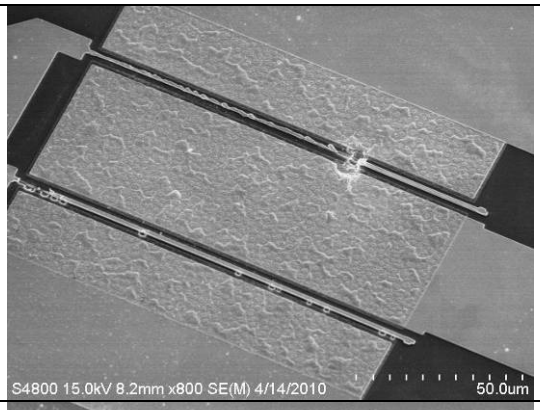
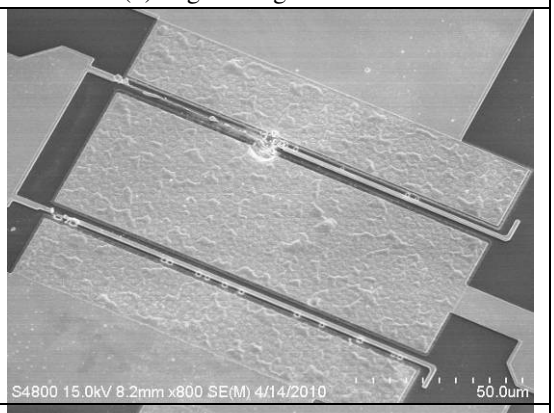
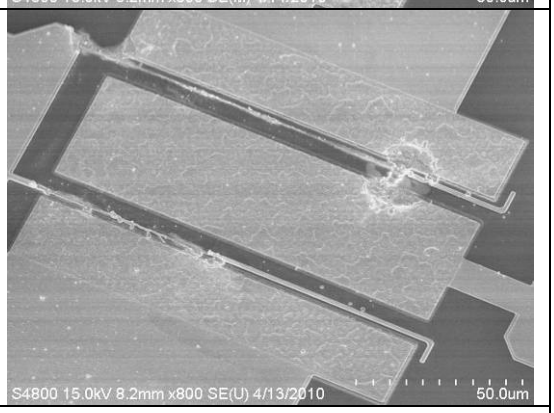
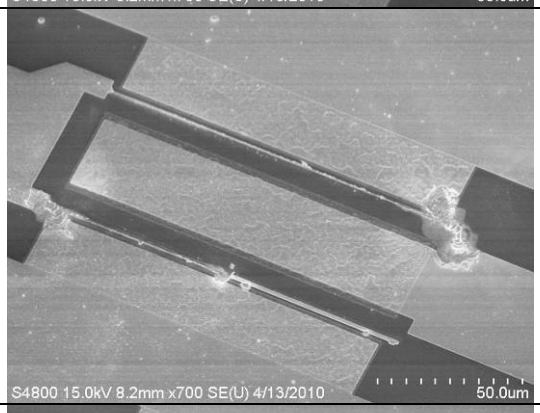
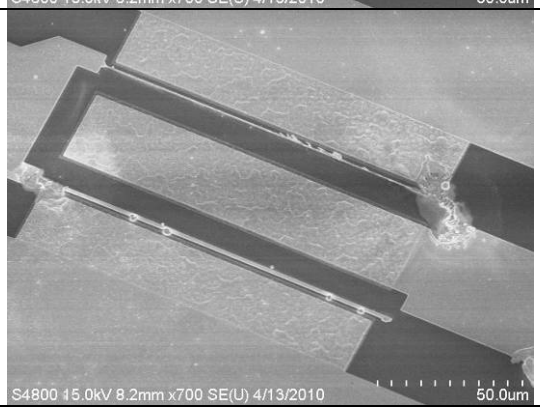
	(a) Microwave test device	(b) High voltage test device
L_{GD} = 2 µm		
L_{GD} = 5 µm		
L_{GD} = 8 µm		No destructive breakdown
L_{GD} = 10 µm		No destructive breakdown

Figure 8.1–6 SEM micrograph for analysis of breakdown failure of 2×125 µm, L_{GD} = 2, 5, 8 and 10 µm GaN-based HEMT for (a) microwave test device (b) high voltage test device.

8.2. Optimization of the Inter-Device Insulation

Defining the semiconductor electronic device active-area inter device insulation prevents

not only crosstalk between neighboring devices but also insulation between the different bias charged functionality areas within the device. In GaN-based HEMTs the main function of the inter-device insulation is segregation of the highly conductive active area. Nevertheless, at high voltage OFF-state operation a leakage current from the source through the inter-device insulation to the drain may be a limitation.

Traditionally in GaN-based HEMTs for microwave devices a mesa topology is used. The surroundings of the active area is recessed by etch process deep into the GaN buffer removing any remaining of the conductive 2DEG. Recently a multi-energy ion implantation is used to paralyze the existence of the 2DEG in the active areas surroundings [142]. This method is preferred for high voltage operation due to its superior insulation, planar topology with improved gate diode characteristics and process simplicity. The initial development of multi-energy ion implantation used in the GaN-based HEMTs process used very high ion doses that had inferior insulation properties and suffered from high leakage at high voltages.

Here a systematic study to optimize the inter-device insulation for high voltage operation is presented. The traditional mesa insulation is enhanced with additional shallow and low dose ion implantation. The planar inter-device insulation process is developed and optimized with low dose deep multi-energy ion implantation.

8.2.1. Devices Process and Experimental Setup

For comparison, eight types of samples with conventional AlGaN/GaN HEMT structure grown by MOVPE on sapphire substrate were studied, a mesa etch inter-device insulation (sample "A"), three variations of shallow ion implantation in addition to the mesa etch structures (samples "B"-"D"), and four variations of planar devices with multi-energy ion implantation (samples "E"-"H") [142]. The ion implantation doses and energy for each sample are summarized in Table 8.2–1.

Mesa etch								
	Sample "A"		Sample "B"		Sample "C"		Sample "D"	
Ion	No implantation		$^{132}Xe^{+}$		$^{14}N^{+}$		$^{14}N^{+}$	
	Energy (KeV)	Dose (cm^{-2})	Energy (KeV)	Dose (cm^{-2})	Energy (KeV)	Dose (cm^{-2})	Energy (KeV)	Dose (cm^{-2})
Additional ion implantation	-	-	25	$5e^{+12}$	25	$5e^{+12}$	25	$2e^{+12}$

Multi-energy ion implantation								
	Sample "E"		Sample "F"		Sample "G"		Sample "H"	
Ion	$^{14}N^{+}$		$^{14}N^{+}$		$^{14}N^{+}$		$^{14}N^{+}$	
	Energy (KeV)	Dose (cm^{-2})	Energy (KeV)	Dose (cm^{-2})	Energy (KeV)	Dose (cm^{-2})	Energy (KeV)	Dose (cm^{-2})
Energy level I	25	$8.0e^{+12}$	30	$8.0e^{+12}$	25	$1.6e^{+12}$	25	$8.0e^{+12}$
Energy level II	50	$1.0e^{+13}$	160	$2.3e^{+13}$	50	$2.0e^{+13}$	50	$1.0e^{+13}$
Energy level III	75	$2.0e^{+13}$	360	$3.0e^{+13}$	75	$4.0e^{+13}$	75	$2.0e^{+13}$
Energy level IV	160	$2.3e^{+13}$	-	-	-	-	-	-
Energy level V	360	$3.0e^{+13}$	-	-	-	-	-	-

Table 8.2–1 Inter-device insulation method and recipe of compared samples.

Field-effect transistors were fabricated on all samples types. Ti/Al/Mo/Au based ohmic contacts were formed by e-beam evaporation and annealed at 830°C. For samples "A"-"D" mesa insulation was preformed using Cl_2/BCl_3 reactive ion etching and for samples "B"-"D" additional single energy shallow ion implantation was made. For samples "E"-"H" planar inter-device insulation was made using $^{14}N^{+}$ multi-energy ion implantation. The AlGaN

barrier was passivated with 200 nm SiN_x. A gate trench in the passivation was defined by i-line optical lithography and subsequently opened by dry etching. Ir/Ti/Au contacts were then evaporated for the gate Schottky metal, followed by a metal liftoff.

8.2.2. Experimental DC and OFF-State Breakdown Measurements Results

Low voltage DC characterization measurements show statistical identity in all measured parameters, such as V_{Th}, $I_{DS\,max}$, R_{ON} etc., for the two types of inter-device insulation processes, nevertheless difference in the diode characteristics are observed. Figure 8.2–1 and Figure 8.2–2 depict the Schottky gate diode potential barrier height, ϕ_B, and the Schottky gate diode reverse bias tunneling leakage measured at V_{diode} = -10 V for all samples respectively. The planar multi-energy ion implantation shows in overall higher Schottky gate diode potential barrier height, ϕ_B, than the mesa inter-device insulation. The lower potential barrier is associated with the gate Schottky metal crossover the mesa surface [143], [144]. Samples "F" and "G" are statistically equal and have the highest potential barrier height, and samples "E" and "H" are statistically equal but own somewhat lower ϕ_B. The mesa inter-device insulation samples "A" and "B" are statistically equal but a reduction in ϕ_B observed for the combination with shallow $^{14}N^+$ ion implantation.

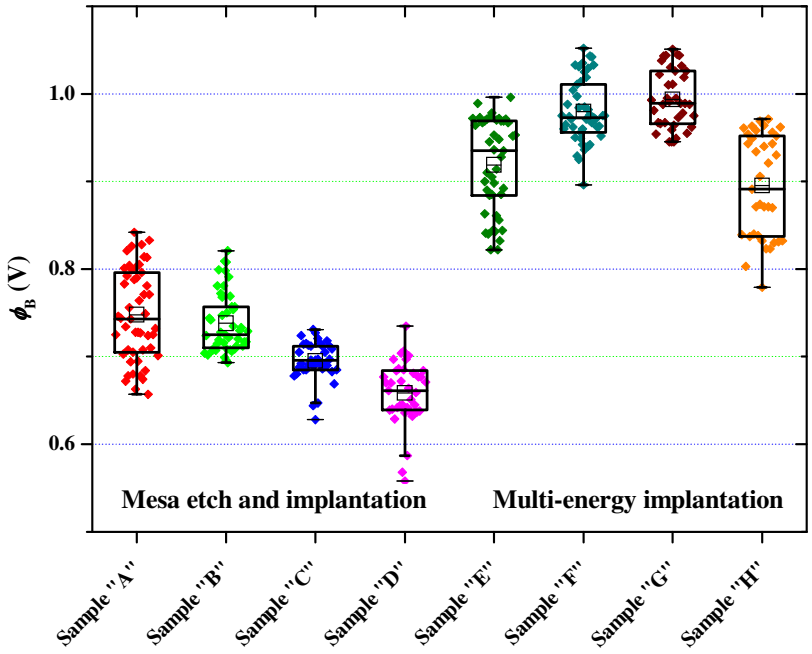


Figure 8.2–1 Samples' distribution of inline monitoring of the Schottky barrier potential height, ϕ_B. Devices' gate drain spacing is L_{GD} = 2 µm and 2 × 50 µm length. The center line is the population median, box top/bottom lines are 25% and 75% percentiles and top/bottom lines are minimum and maximum.

The Schottky diode reverse bias tunneling leakage measurements shows a lower and statistically equal leakage for samples "B", "C", "F" and "G". On the other hand samples "A", "D", "E" and "H" show much higher leakage, samples "A" and "D" and samples "E" and "H" are statistically equal respectively. Both cases are characterized with low implantation ion dose in the upper volume of the semiconductor which may lead to insufficient gate insulation over the inter-device insulation.

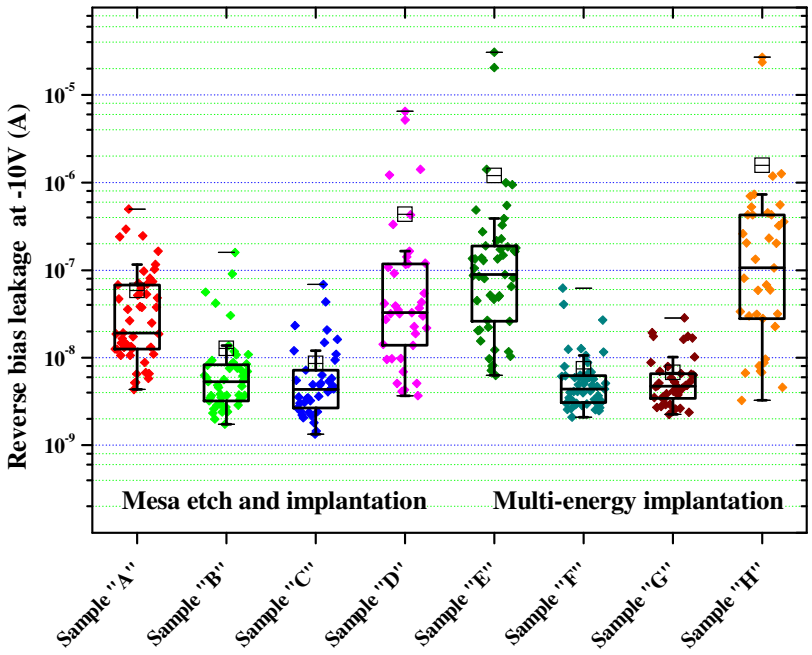


Figure 8.2–2 Samples' distribution of inline monitoring of Schottky gate reverse bias leakage measured at -10 V. Devices' gate drain spacing is L_{GD} = 2 µm and 2 × 50 µm length. The center line is the population median, box top/bottom lines are 25% and 75% percentiles and top/bottom lines are minimum and maximum.

For the electrical analysis and characterization of the inter-device insulation the inline meander electrical-test structures was measured (see Figure 2.5–4(c)). The meander structure is constructed from two ohmic conductive stripes separated by minimal spacing of 5 µm inter device insulation. The meander test structure logarithmic resistance measured at 100 V for all samples is shown in Figure 8.2–3. Mesa etch inter-device insulation solely shows the lowest resistance that assumed to be originated from remaining of the conductive charges on the surface of the mesa [143]. The additional shallow ion implantation shows increase of the resistance with the $^{14}N^{+}$ ion dose in samples "C" and "D". The additional implantation of the large isotopic mass $^{132}Xe^{+}$ ions shows the most significant improvement of the insulation resistance and is an indication to the suppression of upper surface leakage. The planar multi-energy inter-device insulation samples "E"-"H" show superior resistance and statistically equal to each other and to sample "B".

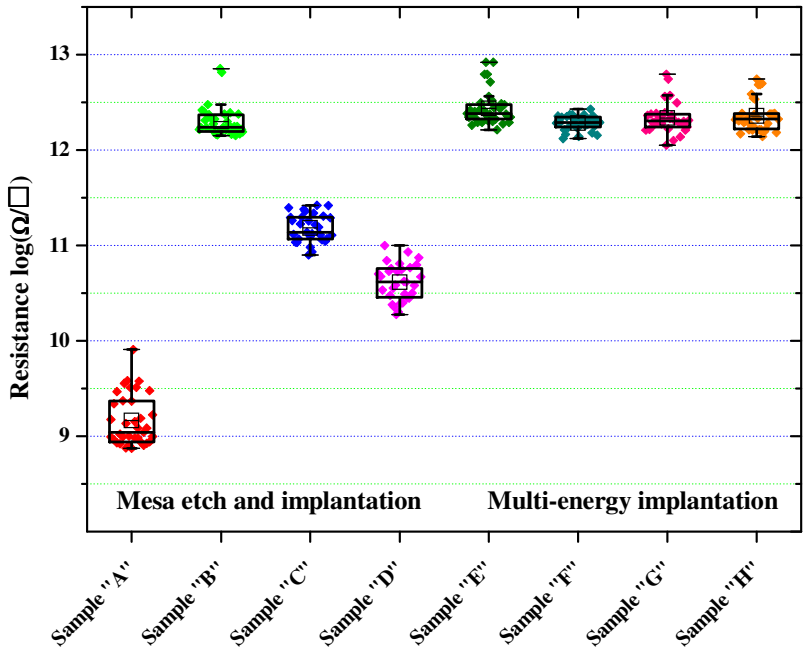


Figure 8.2–3 Samples' distribution of inline monitoring of meander inter-device insulation test structure's, $L = 5$ µm, logarithmic resistance measured at 100 V. The center line is the population median, box top/bottom lines are 25% and 75% percentiles and top/bottom lines are minimum and maximum.

In additional to the traditional inter-device insulation meander test structure resistance measurements two terminal breakdown measurements were performed. The meander breakdown characteristics are depicted in Figure 8.2–4 and Figure 8.2–5 for samples "A"-"D" and samples "E"-"H" respectively. Figure 8.2–6 shows the meander breakdown voltage, $V_{\text{BR meander}}$, distribution for all types of samples. During the measurements one probe is grounded and the other is positively biased and the current flowing through the meander is logged. The breakdown is determined at a current level of 0.5 mA that are equivalent to 1 mA/mm in the test device. The measurements were taken in ambient air with out the use of electronic liquids therefore most of the meander structures were eventually distracted by arching.

The reduction of the leakage current and increase of the breakdown voltage, $V_{\text{BR meander}}$, in the mesa inter-device insulation with any additional shallow single ion implantation is observed in Figure 8.2–4. Sample "A" with mesa etch only have a median breakdown voltage $V_{\text{BR meander}} = 332$ V only. Sample "C" with the higher $^{14}N^{+}$ dose show lower leakage than in sample "D" nevertheless a statistically equal median breakdown of $V_{\text{BR meander}} = 630$ V and 655 V respectively. The sample with the additional $^{132}Xe^{+}$ ion implantation shows the lowest leakage current with the highest breakdown voltage $V_{\text{BR meander}} = 695$ V comparing to other mesa inter-device insulations.

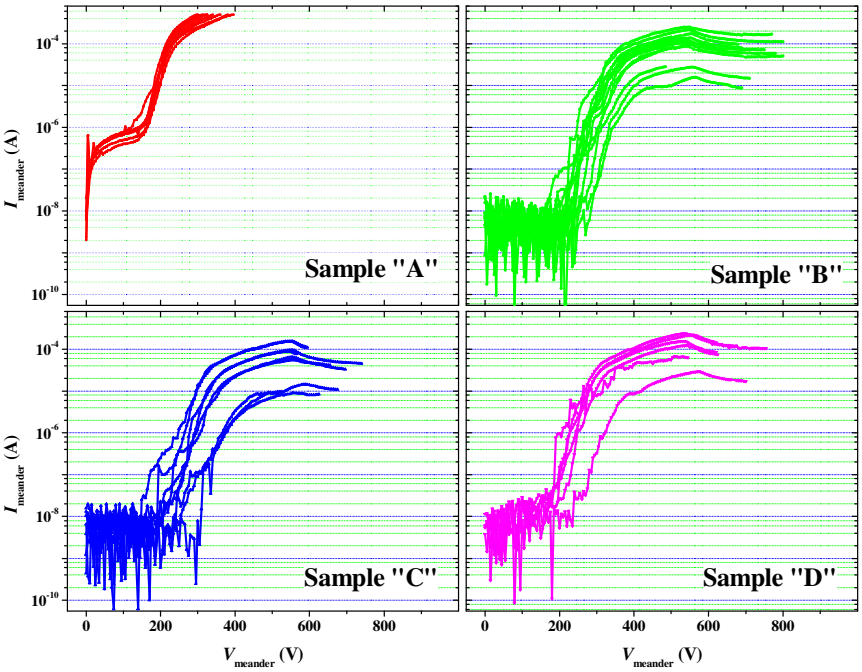


Figure 8.2–4 Inter-device insulation current output during V_{BR} measurements for meander test structure with spacing of $L = 5$ µm for samples with Mesa etch insulation combined with ion implantation (samples "A" – "D") on sapphire substrate. The measurement is limited by the current compliance of 0.5 mA.

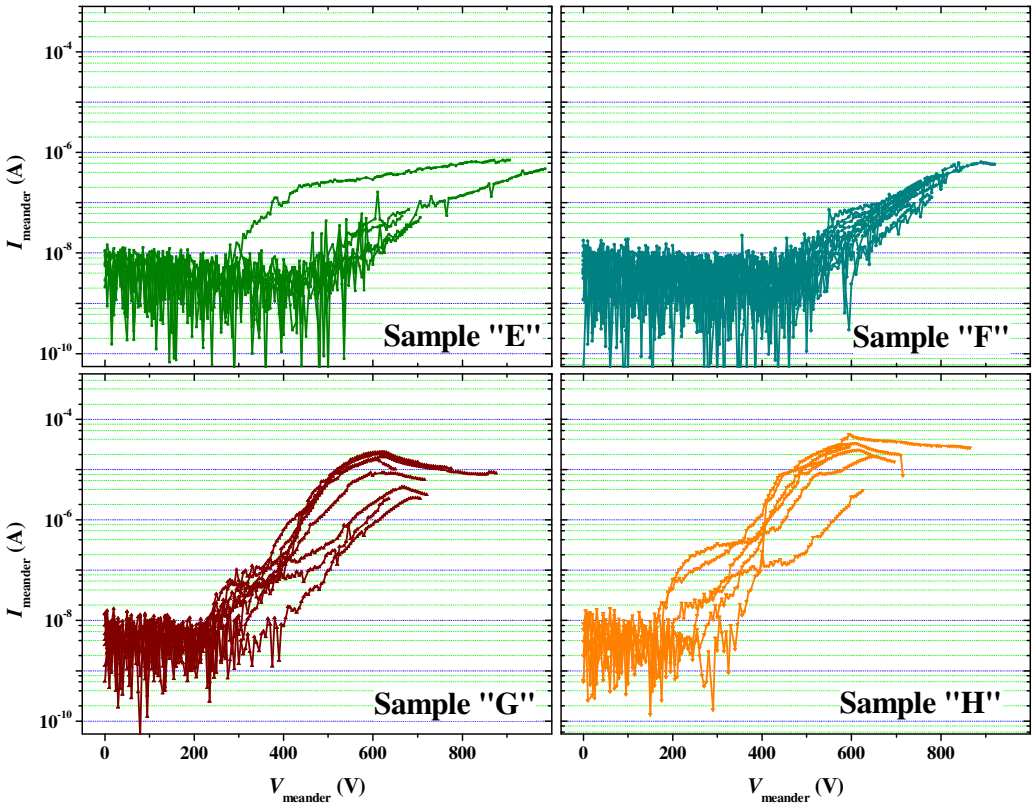


Figure 8.2–5 Inter-device insulation current output during V_{BR} measurements for meander test structure with spacing of $L = 5$ µm for samples with multi-energy $^{14}N^{+}$ ion implantation (samples "E" – "H") on sapphire substrate. The measurement is limited by the current compliance of 0.5 mA.

Planar multi-energy ion implantation shows superior inter-device insulation over the mesa insulation variations. Samples "E"-"H" have a lower leakage current and higher breakdown voltage values of $V_{BR\ meander}$ = 690 V and 775 V 715 V and 675 V respectively samples "E", "G" and "H" show statistical equality. The lower leakage above 200 V in samples "E" and "F" in comparison to samples "G" and "H" can be associated to the high energy deep implantation [142]. The lower median breakdown voltage of sample "E" compared to sample "F" can be associated to the smaller sample size and the measurement in the ambient air.

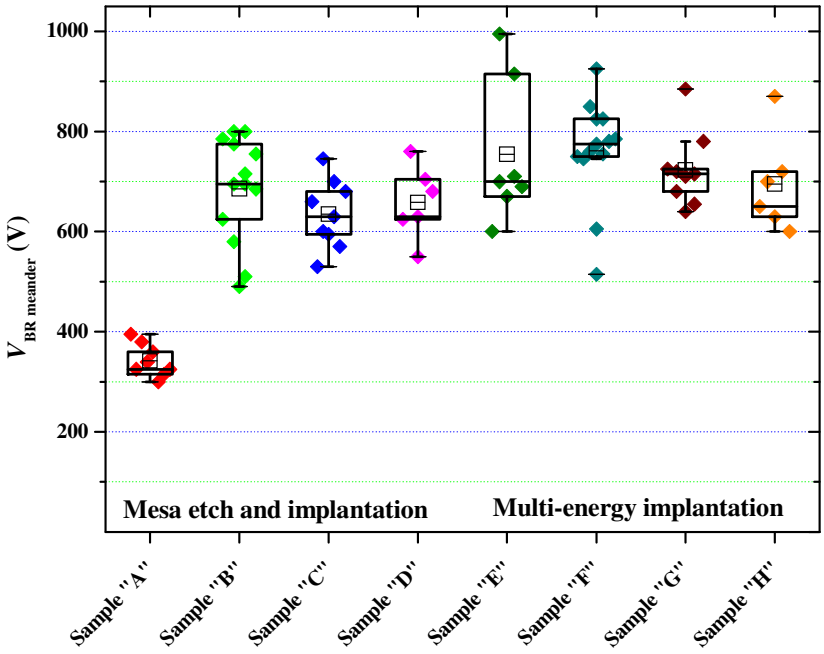


Figure 8.2–6 Samples' distribution of meander inter-device insulation test structure's, $L = 5$ µm, two pole breakdown measurement. The center line is the population median, box top/bottom lines are 25% and 75% percentiles and top/bottom lines are minimum and maximum.

8.2.3. Discussion and Conclusions on Inter-Device Insulation Process

Strong inter-device Insulation is a critical property for high voltage devices that prevent a lateral leakage during OFF-state operation (see section 2.5.3). Two principal methods for inter-device insulation were presented, a mesa type with optional additional shallow ion implantation and planar multi-energy ion implantation.

For high voltage OFF-state operation traditional mesa inter-device insulation is insufficient due to its surface leakages therefore an alternative and improvement to this method is desired. The surface leakage can be reduced with shallow ion implantation and the leakage was correlated to the $^{14}N^{+}$ implanted ion dose (samples "C" and "D") and the isotopic mass of the implanted ion (samples "C" and "B"). $^{132}Xe^{+}$ ion is an excellent choice to passivate the surface due to its large isotopic mass that does not allow it to penetrate into the semiconductor bulk. The added implantation of $^{132}Xe^{+}$ ion improved dramatically the insulation resistance, reduced the insulation leakage current and improved its breakdown voltage. This type of implantation did not affect the gate diode potential barrier height but reduced the reveres bias leakage.

Planar multi-energy ion implantation is relatively simpler process compared to mesa Cl_2/BCl_3 reactive ion etching. This planar topology show higher Schottky diode potential

barrier than mesa insulation topology although it has equivalent diode reverse bias leakage current. The multi-energy ion implantation samples have higher insulation resistance and much lower leakage current resulting in higher insulation breakdown. High energy deep ion implantation, samples “E” and “F”, is essential for suppression the insulation leakage at high voltages above 700 V.

For the high voltage switching devices the three-level energy ion implantation that was demonstrated in sample “F” was chosen due to its low insulation leakage current and superior insulation breakdown voltage. In addition it has a high Schottky potential barrier.

Chapter 9

Conclusions

During this work a large scale multi-wafer experimental systematic studies were conducted to extract the most of the GaN-based material systems potential for use in high voltage operation devices. High voltage blocking capabilities enhancement in forward and reverse drain bias were the focus of investigation in this work. The pursue toward high voltage operation considered many levels of development. It mainly focused on development of reliable simulation tools, design and development of the epitaxial grown stack. Within the same level of importance improvement of manufacturing process technologies, designs of topology and devices layout were considered. Along with device formation a sincere effort was done to characterize the large number of device variations with in the different delivered experiments

A systematic matching of GaN-based HEMTs experimental DC measurements to physically based Silvaco-"ATLAS" simulation program was developed. The GaN-based device simulation was a useful tool for design and insight-analysis that is require for development of such devices. The simulation tool was efficiently used throughout the entire work for device geometry design, epitaxial layers design and analysis of dynamic physical properties of GaN-based HEMTs during their operation.

The simulations results along with intensive analysis of measurements from manufactured devices revealed the nature of the device's breakdown and paved the way for understanding the lack of blocking capability in GaN-based HEMTs. In addition the simulation gave good indication to practice innovative concepts such as the DH-HEMTs, field-plates configurations and the nature of Schottky drain recessed contact.

The OFF-state blocking voltage capability of the investigated devices was found to be dependent on two main subthreshold leakages. The simulation results pointed out the source-drain leakage current also known as punch through. In addition many experimental measurements indicated a Schottky gate reverse bias leakage as dominant leakage mechanism. On the other hand no evidence to SiN_x passivation layer surface leakage was found [7].

From the first steps in this work it was qualitatively understood that suppression of the subthreshold leakage currents by carrier confinement in the channel will enhance the high voltage blocking capabilities of the device. Furthermore, alleviate the high electric fields accumulated in the device is essential during high voltage operation. But the problem is not to be lightheaded approached. Suppression of one or more subthreshold leakage current source will give rise to additional vulnerable hidden leakage sources path. Additionally, deterioration

of the device electrical characteristics must me avoided. In switching devices in many cases increase of the blocking voltage capability is associated with the increase of the ON-state resistance which significantly reduces the device switching efficiency. It also leads to reduction in sheet carrier density and the maximal current density and can have a harmful effect by increasing dispersion.

For microwave-design devices in addition to the mentioned above special care should be considered to the large signal power added efficiency, gain and output power , the small signal cut-off frequency and maximum oscillation frequency, and device linearity. Therefore incremental progress approach that requires many iterations is needed suppressing all week points with the increase of the blocking voltage.

One of the comprehensive approaches that was considered and in many means is the core of this work for blocking voltage enhancement is GaN based DH-HEMTs with a wide band-gap AlGaN back-barrier layer replacing the traditional GaN buffer layer used in GaN based HEMTs.

GaN based DH-HEMTs are found to be a promising concept for high-voltage device application due to their superior channel confinement and superior OFF-state blocking capability without the use of gate insulation.

From the study of GaN based DH-HEMTs grown on sapphire, *n*-type 4H-SiC and SI 4H-SiC substrates the following is concluded.

The introduction of an AlGaN back-barrier layer creates polarization induced potential barrier below the channel. Due to large polarization charges in the heterostructures the bands energetic states are strongly dependent on the Al mole fraction in the AlGaN back-barrier and the UID GaN channel thickness. An optimized relationship between the two parameters is calculated and demonstrated experimentally. The emerged back-barrier leads to a better confinement of the electrons in the UID GaN channel, is accompanied by a reduction in $I_{DS\,max}$ and a positive shift of V_{Th}. The epitaxial stack configuration, determined by the Al composition and UID GaN channel thickness, is strongly influence the electrical characteristics, such as the $I_{DS\,max}$, the V_{Th}, the R_{ON} and the leakage currents. Already for low Al mole fraction (0.02-0.05) in the back-barrier layer, DH-HEMTs prevent the buffer layer punch-through and reduce the sub-threshold drain-leakage and gate-leakage currents, thus significantly increase the device $V_{BR\,OFF}$. With the increase of the GaN channel thickness the subthreshold Schottky-gate reverse bias tunneling leakage current increases and dominates the sub-threshold leakage current, thus the device OFF-state breakdown voltage then decreases. Well designed DH-HEMTs enable much better scaling of the devices' $V_{BR\,OFF}$ with the gate-drain separation, L_{GD}, than conventional GaN based HEMTs. With the decrease of the GaN channel thickness the device $V_{BR\,OFF}$ scaling saturation appears at higher gate-drain spacing, the saturation voltage level as well as scaling slope increases. DH-HEMTs grown on SI-SiC substrates show inferior $V_{BR\,OFF}$ performance and scaling ability due to more intensive Schottky gate reverse bias tunneling leakage than those who were grown on *n*-SiC. Gate-recess and the use of low Al concentration AlGaN back-barrier layer show synergy in increasing $V_{BR\,OFF}$ and in scaling up.

Time and frequency domain measurements show that DH-HEMTs does not suffer from dispersion and knee-walkout, the epitaxial design has minor effect on both f_T and f_{max}, their microwave gain increase due to superior channel confinement but their power efficiency descend due to low heat dissipation.

Additional approach was considered for high electrical field management improvement within the device. Field plates technology is used in GaN-based HEMTs to tranquil the electrical field peak at the drain side of the gate. This field is believed to be driving force to the Schottky gate reverse bias leakage. Innovative multiple grating field plates, MGFPs, configuration was then used along with DH-HEMTs grown on SI-SiC wafers with inferior gate leakage.

As already demonstrated the introduction of an AlGaN back-barrier layer leads to a better

confinement of the electrons in the GaN channel. Combining DH-HEMTs with gate biased MGFPs suppresses the sub-threshold drain currents, source-drain leakage and gate leakage, therefore enhances the device $V_{BR\ OFF}$ by hundreds of volts. Devices with one gate connected FP and one floating FP, integrated in DH-HEMT with $Al_{0.1}Ga_{0.9}N$-back-barrier showed the best $V_{BR\ OFF}$ performance.

Negligible trade-off in ON-state resistance, due to channel confinement was observed. Minor lag factor increase and decrease in f_T and f_{max} were observed due to the additional gate-channel and gate-drain capacitance.

Even though a substantial improvement in DH-HEMTs of the blocking voltage in OFF-state was achieved farther efforts were required to satisfy the requirement of $V_{BR\ OFF} \geq 1000$ V for DC voltage regulators. This goal was achieved by the use of AlGaN/GaN/GaN:C back-barrier HFETs on SI-SiC and *n*-SiC substrates. The introduction of a GaN:C back-barrier layer leads to a better confinement of the electrons in the GaN channel, although it accompanied by a reduction in $I_{DS\ max}$ and an increase of V_{Th}. The GaN:C back-barrier layer suppresses the sub-threshold drain currents, source-drain leakage and gate leakage with out the use of gate insulation layer. A pronounced enhancement of the device $V_{BR\ OFF}$ by hundreds of volts was achieved. The devices demonstrated excellent scaling of the $V_{BR\ OFF}$ with their geometry. Devices fabricated on *n*-SiC substrates suffered from pronounced vertical leakage that limited the device $V_{BR\ OFF}$ uniformity across the wafer.

Trade-off in ON-state resistance, due to channel confinement was observed. The increase of lag factor was observed due to proximity of the GaN:C layer to the 2DEG. Both issues were improved with vertical separation of the GaN:C from the 2DEG by controlling the thickness of UID channel.

The presented devices on both, SI-SiC and *n*-SiC substrates, own record high power figure of merit and exceed the 6H-SiC theoretical material power limit.

The described achievements are not solely independent and strongly dependent of peripheral effects such as substrate leakage, inter-device insulation and high voltage lateral separation. These undesired effects were prevented by adequate device layout and topology design and improved process technologies such as multi-energy ion implantation for inter-device insulation.

The improved high-voltage device design mainly focused on lateral separation of the high-voltage drain module from the delicate gate module. In addition sharp corners that believed to accumulate high electric field were eliminated.

Strong inter-device Insulation is a critical property for high voltage devices that prevent a lateral leakage during OFF-state operation. Two principal methods for inter-device insulation were presented, a mesa type with optional additional shallow ion implantation and planar multi-energy ion implantation.

For high voltage OFF-state operation traditional mesa inter-device insulation is insufficient due to its surface leakages therefore an alternative and improvement to this method was demonstrated. For the high voltage switching devices the three-level energy ion implantation was chosen due to its low insulation leakage current and superior insulation breakdown voltage. In addition it has a high Schottky potential barrier.

While major efforts were made throughout this work to improve the forward blocking performance, GaN-based HEMTs with reverse blocking capability are also desired in a number of applications. In a recently demonstrated AlGaN/GaN Class-S amplifier, the power HEMT may experience a short negative pulse at the drain terminal as a result of a fly-back signal from the output filter. The intention of the AlGaN/GaN HEMTs with protection diode is to prevent a current flow in the transistor during reverse bias conditions in switching devices. Replacing the planar drain ohmic contact by a recessed Schottky metal will show the desired reverse blocking bias. The realization of a good Schottky diode is possible when a contact of the Schottky metal to the 2DEG and/or GaN semiconductor buffer layer is achieved.

A demonstration of AlGaN/GaN HEMT with integrated protection Schottky diode is

presented. The results of the innovative Schottky-drain HEMT demonstrated an excellent reverse blocking with minor trade-off in the ON-state resistance for the complete device. A reverse blocking capability of the diode was better than -110 V demonstrated with excellent quality of the forward diode characteristics. The demonstrated recess process showed high robustness and low influence on the electrical DC characteristics.

The goals defined for this work (section 1.2) were completely achieved. Deep understanding of the premature breakdown mechanisms led to design and development of concepts for breakdown voltage enhancement in GaN-based HEMTs for power switching and regulation application. Such deep knowledge and insight is a result of development of mature physically based device simulation tools. Development and manufacturing of large area normally-off 250 V 50 A devices achieved (see section 9.1) [78]. The design and development of 1000 V normally-on and normally-off regulators is in advanced progress in the time of writing these lines. In addition substantial progress in analysis the GaN-based device robustness and reliability achieved [98], [145]. Long term reliability test results are expected in the very near future.

9.1. Vision

Throughout this work many achievements were demonstrated but there are still tasks yet to be accomplished. Recently a large area normally-off GaN-based HEMTs prototypes for radiation hardened power switching application with enhanced breakdown voltage using the methods developed in this work were introduced by FBH (see Figure 9.1–1 and Figure 9.1–2). To maintain the low-cost and price compatibility with Si-based MOSFETs of such product these prototypes were grown on low cost *n*-SiC substrates and their OFF-state blocking voltage was limited by the substrate subthreshold leakage. The demonstrators design is based on flip-chip bumps assembly. These demonstrators were successfully tested for radiation hardness at the customer's laboratories.

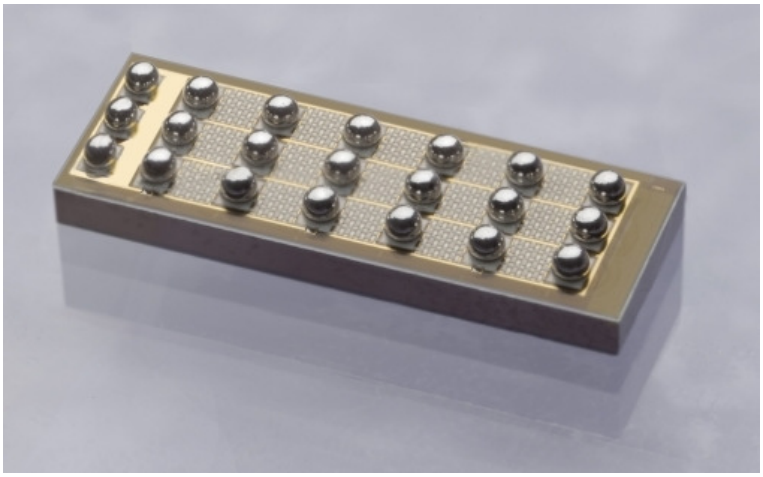


Figure 9.1–1 FBH demonstrated radiation hardened normally-off GaN-Based HEMT cellular flip-chip bumps assembly design for switching applications. With W_g = 110 mm, $V_{BR\ OFF}$ > 250 V, R_{DS} (ON) = 0.067 Ω at I_D = 5 A and R_{DS} (ON) = 0.104 Ω at I_D = 50 A.

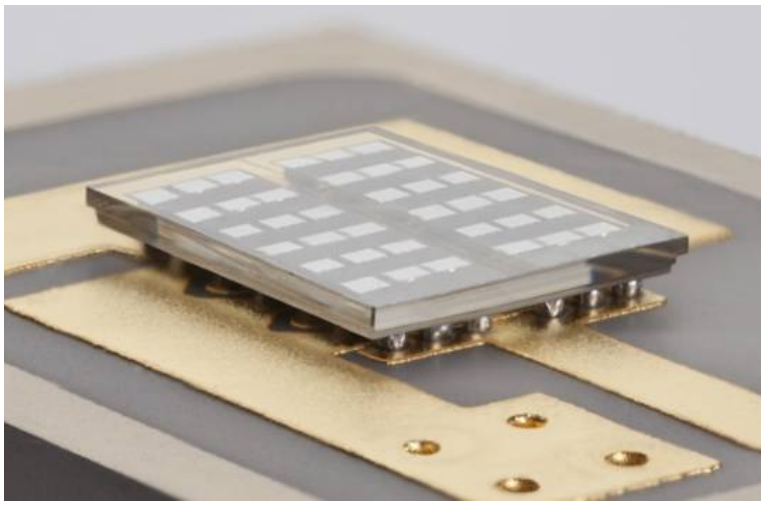


Figure 9.1–2 FBH demonstrated radiation hardened normally-off GaN-Based HEMT mounted cellular flip-chip bumps assembly design for switching applications. With W_g = 110 mm, $V_{BR\ OFF}$ > 200 V, R_{DS} (ON) = 0.067 Ω at I_D = 50 A.

For farther OFF-state blocking capability additional development and standardization of the epitaxial structures are required. Such epitaxial structures should be well design to serve *p*-GaN normally-off devices [78]. As such, an optimization between the sheet carrier density in the 2DEG and threshold voltage in close proximity to zero is desired. Integration of highly resistive GaN:C back-barrier into DH-HEMTs is an obvious step for breakdown voltage enhancement along with GaN:C associated dispersion prevention while maintaining low ON-state resistance. Special considerations should be taken for prevention of the substrate subthreshold leakage associated with the *n*-SiC substrate.

Epitaxial growth of GaN-based structures of foreign substrate is accompanied by high strain due large difference of thermal expansion between the substrate and the epitaxial layers. Therefore reckless growth results it highly none-flat or bowed wafers. Such wafers are extremely difficult to process due to lack of uniform focal plane that required for lithographic patterning. Therefore, such epitaxial growth should calculate the exact bow of these wafers in addition to their material design.

The development of GaN-based HEMTs for switching applications is a successor of the microwave design. There it was required to use highly isolated material with excellent thermal conductivity for high microwave power performance. For compatibility of the epitaxial growth along with maintaining low-cost the device manufactured by FBH were grown on *n*-SiC. But in order to be competed Si-base power technology GaN on Si substrates should be used.

Normally-on GaN-base devices use Schottky metal as a gate electrode. As shown along this work the Schottky gate reverse bias tunneling leakage is one of the dominant subthreshold leakages that prohibit high off-state blocking voltage. In addition to the methods developed and demonstrated in this work additional techniques are needed to be developed such as slanted gate technology, the use of gate dielectrics and reliable short gate technology.

Dispersion in GaN-based HEMTs cased by charge trapping create a problem in power switching applications transistors due to limits of figures of merit such as the ON-resistance and therefore increases conduction losses. Reduction of the device dispersion by appropriate growth process is essential to improve device characteristics at high drain voltages up to the kV range, suitable for switching applications. The high resistivity buffer is compensated by defects, e.g. deep acceptors such as carbon (as presented in section 5.4) or also gallium vacancies, but also threading dislocations. Therefore, their influence on device characteristics has to be studied by electrical as well as physical characterization techniques such as photoluminescence and deep-level trap spectroscopy

Time domain power switching measurements are the next step in the device performance evaluation. Such on-wafer measurements were unavailable due to complexity of the impedance matching circuitry. Such power switches measurements illustrate the frequency dependent switching waveforms observed resulting in power dissipation during the ON-state, OFF-state, as well as during the switching transients.

Farther investigation on device robustness along long term reliability is essential especially for space applications that require lifetime of over 20 years. The proposed DH-HEMTs devices already have shown superior robustness due to strong reduction in the drain and gate leakage currents. Nevertheless, robustness test is just the first step prior to long term reliability test at elevated temperatures and high voltages. Such tests require dicing and packaging of selected devices and will be conducted in the near future for the manufactured devices. Finally all device types should be certified as radiation hardness for space applications.

Reference

[1] A. Ionascut-Nedelcescu, C. Carlone, A. Houdayer, H. J. von Bardeleben, J. L. Cantin, and S. Raymond, "Radiation hardness of gallium nitride," *Nuclear Science, IEEE Transactions on*, vol. 49, no. 6, pp. 2733-2738, Dec.2002.

[2] in *http://www.esa.int*.

[3] in *http://www.irf.com*.

[4] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Design optimization of high breakdown voltage AlGaN-GaN power HEMT on an insulating substrate for R_{ON}A-V_B tradeoff characteristics," *Electron Devices, IEEE Transactions on*, vol. 52, no. 1, pp. 106-111, 2005.

[5] X. Huili, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, "High breakdown voltage AlGaN-GaN HEMTs achieved by multiple field plates," *Electron Device Letters, IEEE*, vol. 25, no. 4, pp. 161-163, 2004.

[6] N.-Q. Zhang, S. Keller, G. Parish, S. Heikman, S. P. DenBaars, and U. K. Mishra, "High breakdown GaN HEMT with overlapping gate structure," *Electron Device Letters, IEEE*, vol. 21, no. 9, pp. 421-423, 2000.

[7] N.-Q. Zhang, "High voltage GaN HEMTs with low on-resistance for switching applications." *PhD Thesis* University of California, Santa Barbara, USA, 2002.

[8] N.-Q. Zhang, B. Moran, S. DenBaars, U. K. Mishra, X. W. Wang, and T. P. Ma, "Kilovolt AlGaN/GaN HEMTs as Switching Devices," *physica status solidi (a)*, vol. 188, no. 1, pp. 213-217, July2001.

[9] N. Tipirneni, A. Koudymov, V. Adivarahan, J. Yang, G. Simin, and M. A. Khan, "The 1.6-kV AlGaN/GaN HFETs," *Electron Device Letters, IEEE*, vol. 27, no. 9, pp. 716-718, 2006.

[10] S. Yagi, M. Shimizu, M. Inada, Y. Yamamoto, G. Piao, H. Okumura, Y. Yano, N. Akutsu, and H. Ohashi, "High breakdown voltage AlGaN/GaN MIS-HEMT with SiN and TiO2 gate insulator," *Solid-State Electronics*, vol. 50, no. 6, pp. 1057-1061, June2006.

[11] T. Morita, M. Yanagihara, H. Ishida, M. Hikita, K. Kaibara, H. Matsuo, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "650V 3.1mΩcm GaN-based Monolithic Bidirectional Switch Using Normally-off Gate Injection Transistor," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International* 2007, pp. 865-868.

[12] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, Y. Saito, I. Omura, and M. Yamaguchi, "Current Collapseless High-Voltage GaN-HEMT and its 50-W Boost Converter Operation," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International* 2007, pp. 869-872.

[13] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. DenBaars, and U. K. Mishra, "High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates," *IEEE Electron Device Letters*, vol. 27, no. 9, pp. 713-715, Sept.2006.

[14] J. M. Hancock and I. Zverev, "Introduction to Avalanche Considerations for

CoolMOS S5 and C2, SMPS Applications," Infineon CoolMOS Application Note, 2000.

[15] K. Takahashi, H. Kuribayashi, T. Kawashima, S. Wakimoto, K. Mochizuki, and H. Nakazawa, "20 mΩ·cm^2 660 V Super Junction MOSFETs Fabricated by Deep Trench Etching and Epitaxial Growth," in *Power Semiconductor Devices and IC's, 2006. ISPSD 2006. IEEE International Symposium on* 2006, pp. 1-4.

[16] C. Rochefort and R. van Dalen, "A scalable trench etch based process for high voltage vertical RESURF MOSFETs," in *Power Semiconductor Devices and ICs, 2005. Proceedings. ISPSD '05. The 17th International Symposium on* 2005, pp. 35-38.

[17] S. Yamauchi, T. Shibata, S. Nogami, T. Yamaoka, Y. Hattori, and H. Yamaguchi, "200 V Super Junction MOSFET Fabricated by High Aspect Ratio Trench Filling," in *Power Semiconductor Devices and IC's, 2006. ISPSD 2006. IEEE International Symposium on* 2006, pp. 1-4.

[18] J. Casady, "SemiSouth's transistors boost photovoltaic system efficiencies," *Compound Semiconductor*, vol. 15, no. 1, pp. 18-20, Feb.2009.

[19] in http://techon.nikkeibp.co.jp/.

[20] A. Trampert, O. Brandt, and Ploog.K.H., "Crystal Structure of Group III Nitrides," in *Gallium Nitride (GaN) I, Vol. 50*. J. I. Pankove and T. D. Moustakas, Eds. San Diego, CA: Academic press, 1998, pp. 167-192.

[21] H. Morkoç, *Handbook of Nitride Semiconductors and Devices, Vol. 1: Materials Properties, Physics and Growth*. Weinheim, Germany: Wiley-VCH Verlag GmbH & Co. KGaA, 2008.

[22] F. Bernardini, V. Fiorentini, and D. Vanderbilt, "Spontaneous polarization and piezoelectric constants of III-V nitrides," *Phys. Rev. B*, vol. 56, no. 16, p. R10024, Oct.1997.

[23] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3ed. Hoboken, New Jersey: John Wiley & Sons, Inc., 2007.

[24] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 85, no. 6, pp. 3222-3233, Mar.1999.

[25] O. Ambacher, J. Majewski, C. Miskys, A. Link, M. Hermann, M. Eickhoff, M. Stutzmann, F. Bernardini, V. Fiorentini, V. Tilak, B. Schaff, and L. F. Eastman, "Pyroelectric properties of Al(In)GaN/GaN hetero- and quantum well structures," *Journal of Physics: Condensed Matter*, vol. 14, no. 13, p. 3399, 2002.

[26] O. Ambacher, "Growth and applications of Group III-nitrides," *Journal of Physics D: Applied Physics*, vol. 31, no. 20, pp. 2653-2710, 1998.

[27] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Applied Physics Letters*, vol. 77, no. 2, pp. 250-252, July2000.

[28] B. K. Ridley, O. Ambacher, and L. F. Eastman, "The polarization-induced electron gas in a heterostructure," *Semiconductor Science and Technology*, vol. 15, no. 3,

p. 270, 2000.

[29] M. A. Khan, Q. Chen, C. J. Sun, M. Shur, and B. Gelmont, "Two-dimensional electron gas in GaN-AlGaN heterostructures deposited using trimethylamine-alane as the aluminum source in low pressure metalorganic chemical vapor deposition," *Applied Physics Letters*, vol. 67, no. 10, pp. 1429-1431, Sept.1995.

[30] M.Shur, B.Gelmont, and K. Asif, "Electron mobility in two-dimensional electron gas in AlGaN/GaN heterostructures and in bulk GaN," *J. Electron. Mater.*, vol. 25, no. 5, pp. 777-785, 1996.

[31] W. Walukiewicz, H. E. Ruda, J. Lagowski, and H. C. Gatos, "Electron mobility in modulation-doped heterostructures," *Phys. Rev. B*, vol. 30, no. 8, p. 4571, Oct.1984.

[32] C. Wood and D. Jena, *Polarization Effects in Semiconductors From Ab InitioTheory to Device Applications*. New York, NY: Springer, 2008.

[33] M. Farahmand, C. Garetto, E. Bellotti, K. F. Brennan, M. Goano, E. Ghillino, G. Ghione, J. D. Albrecht, and P. P. Ruden, "Monte Carlo simulation of electron transport in the III-nitride wurtzite phase materials system: binaries and ternaries," *Electron Devices, IEEE Transactions on*, vol. 48, no. 3, pp. 535-542, 2001.

[34] M. A. Littlejohn, J. R. Hauser, and T. H. Glisson, "Monte Carlo calculation of the velocity-field relationship for gallium nitride," *Applied Physics Letters*, vol. 26, no. 11, pp. 625-627, June1975.

[35] B. Gelmont, K. Kim, and M. Shur, "Monte Carlo simulation of electron transport in gallium nitride," *Journal of Applied Physics*, vol. 74, no. 3, pp. 1818-1821, Aug.1993.

[36] M. S. Krishnan, N. Goldsman, and A. Christou, "Transport simulation of bulk $Al_xGa_{1-x}N$ and the two-dimensional electron gas at the $Al_xGa_{1-x}N$/GaN interface," *Journal of Applied Physics*, vol. 83, no. 11, pp. 5896-5903, June1998.

[37] U. V. Bhapkar and M. S. Shur, "Monte Carlo calculation of velocity-field characteristics of wurtzite GaN," *Journal of Applied Physics*, vol. 82, no. 4, pp. 1649-1655, Aug.1997.

[38] M. A. Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, "High electron mobility transistor based on a GaN-$Al_xGa_{1-x}N$ heterojunction," *Applied Physics Letters*, vol. 63, no. 9, pp. 1214-1215, Aug.1993.

[39] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2ed. Upper Saddle River, New Jersey: Prentice Hall, 1997.

[40] B. J. Baliga, "Trends in power semiconductor devices," *Electron Devices, IEEE Transactions on*, vol. 43, no. 10, pp. 1717-1731, 1996.

[41] T. P. Chow and R. Tyagi, "Wide Bandgap Compound Semiconductors for Superior High-Voltage Unipolar Power Devices," *Electron Devices, IEEE Transactions on*, vol. 41, no. 8, pp. 1481-1483, Aug.1994.

[42] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, and H. Ohashi, "High breakdown voltage AlGaN-GaN power-HEMT design and high current density switching behavior," *Electron Devices, IEEE Transactions on*, vol. 50, no. 12, pp. 2528-2531, 2003.

[43] S. Yoshida, J. Li, T. Wada, and H. Takehara, "High-power AlGaN/GaN HFET with a lower on-state resistance and a higher switching time for an inverter

circuit," *Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on*, pp. 58-61, 2003.

[44] B. J. Baliga, *Fundamentals of Power Semiconductor Devices* Springer US, 2008.

[45] D. A. Grant and J. Guwar, *Power MOSFETs: Theory and Applications*, First ed Wiley-Interscience, 1989.

[46] in *http://www.microchemicals.com/*.

[47] S. J. Pearton, C. R. Abernathy, and F. Ren, *Gallium Nitride Processing for Electronics, Sensors and Spintronics*. London: Springer London, 2006.

[48] M. Micovic, P. Hashimoto, H. Ming, I. Milosavljevic, J. Duvall, P. J. Willadsen, W. S. Wong, A. M. Conway, A. Kurdoghlian, P. W. Deelman, Jeong-S Moon, A. Schmitz, and M. J. Delaney, "GaN double heterojunction field effect transistor for microwave and millimeterwave power applications," in *Electron Devices Meeting, 2004.IEDM Technical Digest.IEEE International* 2004, pp. 807-810.

[49] G. Simin, X. Hu, A. Tarakji, J. Zhang, A. Koudymov, S. Saygi, J. Yang, K. Asif, M. Shur, and R. Gaska, "AlGaN/InGaN/GaN Double Heterostructure Field-Effect Transistor," *Jpn. J. Appl. Phys.*, vol. 40(2), no. 11A, p. L1142-L1144, Jan.2001.

[50] M. J. Uren, K. J. Nash, R. S. Balmer, T. Martin, E. Morvan, N. Caillas, S. L. Delage, D. Ducatteau, B. Grimbert, and J. C. De Jaeger, "Punch-through in short-channel AlGaN/GaN HFETs," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 395-398, Feb.2006.

[51] S. Kato, Y. Satoh, H. Sasaki, I. Masayuki, and S. Yoshida, "C-doped GaN buffer layers with high breakdown voltages for high-power operation AlGaN/GaN HFETs on 4-in Si substrates by MOVPE," *Journal of Crystal Growth*, vol. 298, pp. 831-834, Jan.2007.

[52] S. R. Bahl and J. A. del Alamo, "A new drain-current injection technique for the measurement of off-state breakdown voltage in FETs," *Electron Devices, IEEE Transactions on*, vol. 40, no. 8, pp. 1558-1560, 1993.

[53] P. Ellrodt, W. Brockerhoff, and F. J. Tegude, "Investigation of leakage current behaviour of Schottky gates on InAlAs/InGaAs/InP HFET structures by a 1D model," *Solid-State Electronics*, vol. 38, no. 10, pp. 1775-1780, Oct.1995.

[54] S. Takamiya, M. Harayama, T. Sugimura, T. Tsuzuku, T. Taya, K. Iiyama, and S. Hashimoto, "Reverse currents of Schottky gates of III-V MESFET/HEMTS: field emission and tunnel currents," *Solid-State Electronics*, vol. 42, no. 3, pp. 447-451, Mar.1998.

[55] P. Pipinys and V. Lapeika, "Temperature dependence of reverse-bias leakage current in GaN Schottky diodes as a consequence of phonon-assisted tunneling," *Journal of Applied Physics*, vol. 99, no. 9, pp. 093709-3, May2006.

[56] E. J. Miller, X. Z. Dang, and E. T. Yu, "Gate leakage current mechanisms in AlGaN/GaN heterostructure field-effect transistors," *Journal of Applied Physics*, vol. 88, no. 10, pp. 5951-5958, Nov.2000.

[57] E. J. Miller, E. T. Yu, P. Waltereit, and J. S. Speck, "Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular-beam epitaxy," *Applied Physics Letters*, vol. 84, no. 4, pp. 535-537, Jan.2004.

[58] M. A. Khan, J. N. Kuznia, J. M. Van Hove, N. Pan, and J. Carter, "Observation of a two-dimensional electron gas in low pressure metalorganic chemical vapor

deposited GaN-$Al_xGa_{1-x}N$ heterojunctions," *Applied Physics Letters*, vol. 60, no. 24, pp. 3027-3029, June1992.

[59] "ATLAS User's Manual, Device Simulation Software", 2010 ed Santa Clara, CA.: SILVACO International, 2010.

[60] G. K. Wachutka, "Rigorous thermodynamic treatment of heat generation and conduction in semiconductor device modeling," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 9, no. 11, pp. 1141-1149, 1990.

[61] I.Vurgaftman, J.R.Meyer, and M. Ram, "Band parameters for III-V compound semiconductors and their alloys," *Journal of Applied Physics*, vol. 89, no. 11, pp. 5815-5875, 2001.

[62] J. Piprek, "Electron energy bands," in *Semiconductor Optoelectronic Devices: Introduction to Physics and Simulation* UCSB: Academic Press, 2003, pp. 13-48.

[63] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, A. J. Sierakowski, W. J. Schaff, L. F. Eastman, R. Dimitrov, A. Mitchell, and M. Stutzmann, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 87, no. 1, pp. 334-344, Jan.2000.

[64] S. L. Chuang, "Optical gain of strained wurtzite GaN quantum-well lasers," *Quantum Electronics, IEEE Journal of*, vol. 32, no. 10, pp. 1791-1800, 1996.

[65] S. L. Chuang and C. S. Chang, "k*p method for strained wurtzite semiconductors," *Phys. Rev. B*, vol. 54, no. 4, p. 2491, July1996.

[66] M. Kumagai, S. L. Chuang, and H. Ando, "Analytical solutions of the block-diagonalized Hamiltonian for strained wurtzite semiconductors," *Phys. Rev. B*, vol. 57, no. 24, p. 15303, June1998.

[67] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proceedings of the IEEE*, vol. 55, no. 12, pp. 2192-2193, June1967.

[68] S. A. Schwarz and S. E. Russek, "Semi-empirical equations for electron velocity in silicon: Part II—MOS inversion layer," *Electron Devices, IEEE Transactions on*, vol. 30, no. 12, pp. 1634-1639, Dec.1983.

[69] C. Canali, G. Majni, R. Minder, and G. Otteviani, "Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature," *Electron Devices, IEEE Transactions on*, vol. 22, no. 11, pp. 1045-1047, Nov.1975.

[70] S. L. Chuang and C. S. Chang, "A band-structure model of strained quantum-well wurtzite semiconductors," *Semiconductor Science and Technology*, vol. 12, no. 3, pp. 252-263, 1997.

[71] C.-Y. Lu, E. Bahat-Treidel, O. Hilt, R. Lossy, N. Chaturverdi, E. Y. Chang, J. Würfl, and G. Tränkle, "Influence of the device geometry on the Schottky gate characteristics of AlGaN/GaN HEMTs," *Semiconductor Science and Technology*, vol. 25, no. 7, p. 075005, June2010.

[72] I. Khalil, E. Bahat-Treidel, F. Schnieder, and J. Wurfl, "Improving the Linearity of GaN HEMTs by Optimizing Epitaxial Structure," *Electron Devices, IEEE Transactions on*, vol. 56, no. 3, pp. 361-364, 2009.

[73] E. Bahat-Treidel, J. Würfl, and G. Trankle, "Breakdown voltage simulation of AlGaN/GaN HEMTs on 4H-SiC," in *The 31st Workshop on Compound Semiconductor Device and Integrated Circuits*. G. Meneghesso, Ed. Venice, Italy: 2007, pp. 303-305.

[74] E. Bahat-Treidel, V. Sidorov, J. Würfl, and G. Trankle, "Simulation of AlGaN/GaN HEMTs' breakdown voltage enhancement using grating field plates," in *Simulation of Semiconductor Processes and Devices 2007,* 12 ed. T. Grasser and S. Selbererr, Eds. Vienna: Springer Vienna, 2007, pp. 277-279.

[75] E. Bahat-Treidel, I. Khalil, O. Hilt, J. Würfl, and G. Trankle, "Engineered linearity of GaN-based HEMTs power devices by tailoring transfer characteristics," in *35th International Symposium on Compound Semiconductors, abstract book*. O. Ambacher, Ed. Rust, Germany: 2008, p. P27.

[76] Eldad Bahat-Treidel, Ibrahim Khalil, Oliver Hilt, Joachim Würfl, and Günther Tränkle, "Engineered linearity of GaN-based HEMTs power devices by tailoring transfer characteristics," *physica status solidi (c)*, vol. 6, no. 6, pp. 1378-1381, 2009.

[77] O. Hilt, E. Bahat-Treidel, V. Sidorov, and J. Würfl, "Gate-Length Dependent on-state 2DEG Constriction in AlGaN/GaN HEMTs," in *The 32nd Workshop on Compound Semiconductor Devices and Integrated Circuits, abstract book*. M. Germain, Ed. 2008, pp. 29-30.

[78] O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel, and H.-J. Würfl, "Normally-off AlGaN/GaN HFET with p-type GaN Gate and AlGaN Buffer," *Power Semiconductor Devices & IC's (ISPSD), 2010 22nd International Symposium on* , vol., no., pp.347-350, 6-10 June 2010.

[79] E. Bahat-Treidel, O. Hilt, F. Brunner, J. Wurfl, and G. Trankle, "Punchthrough-Voltage Enhancement of AlGaN/GaN HEMTs Using AlGaN Double-Heterojunction Confinement," *Electron Devices, IEEE Transactions on*, vol. 55, no. 12, pp. 3354-3359, 2008.

[80] E. Bahat-Treidel, O. Hilt, F. Brunner, J. Würfl, and G. Tränkle, "Punch-through voltage enhancement scaling of AlGaN/GaN HEMTs using AlGaN double heterojunction confinement," *physica status solidi (c)*, vol. 6, no. 6, pp. 1373-1377, 2009.

[81] E. Bahat-Treidel, O. Hilt, F. Brunner, J. Würfl, and G. Tränkle, "AlGaN/GaN/AlGaN Double Heterojunction HEMTs on *n*-type SiC Substrates," in *The 36th International Symposium on Compound Semiconductors*. U.K.Mishra, Ed. 2009, pp. 369-370.

[82] E. Bahat-Treidel, O. Hilt, F. Brunner, H.-J. Würfl, and G. Tränkle, "AlGaN/GaN/AlGaN Double Heterojunction HEMTs on *n*-type SiC Substrates," *physica status solidi (c)*, Vol. 7, No. 10, pp. 2407-2411, 2010.

[83] P. Ivo, A. Glowacki, E. Bahat-Treidel, R. Lossy, H.-J. Würfl, C. Boit, and G. Tränkle, "Comparative study of AlGaN/GaN HEMTs robustness versus buffer design variations by applying electroluminescence and electrical measurements," in *Reliability Of Compound Semiconductors Workshop*. Peter Ersland, Ed. 2010.

[84] N. Maeda, T. Saitoh, K. Tsubaki, T. Nishida, and N. Kobayashi, "Enhanced Electron Mobility in AlGaN/InGaN/AlGaN Double-Heterostructures by Piezoelectric Effect," *Jpn. J. Appl. Phys.*, vol. 38, Part 2, no. 7B, p. L799-L801, July1999.

[85] Y. C. Choi, M. Pophristic, B. Peres, H-Y. Cha, M. G. Spencer, and L. F. Eastman, "High breakdown voltage C-doped GaN-on-sapphire HFETs with a low specific on-resistance," *Semiconductor Science and Technology*, vol. 22, pp. 517-521, Mar.2007.

[86] T. Inoue, T. Inoue, T. Nakayama, Y. Ando , M. Kosaki, H. Miwa , K. Hirata , T. Uemura , and H. Miyamoto, "Polarization Engineering on Buffer Layer in GaN-Based Heterojunction FETs," *Electron Devices, IEEE Transactions on*, vol. 55, no. 2, pp. 483-488, 2008.

[87] W. S. Tan, M. J. Uren, P. A. Houston, R. T. Green, R. S. Balmer, and T. Martin, "Surface leakage currents in SiN_x passivated AlGaN/GaN HFETs," *Electron Device Letters, IEEE*, vol. 27, no. 1, pp. 1-3, 2006.

[88] C. Q. Chen, J. P. Zhang, V. Adivarahan, A. Koudymov, H. Fatima, G. Simin, J. Yang, and M. A. Khan, "AlGaN/GaN/AlGaN double heterostructure for high-power III-N field-effect transistors," *Applied Physics Letters*, vol. 82, no. 25, pp. 4593-4595, June2003.

[89] N. Maeda, T. Saitoh, K. Tsubaki, T. Nishida, and N. Kobayashi, "Enhanced effect of polarization on electron transport properties in AlGaN/GaN double-heterostructure field-effect transistors," *Applied Physics Letters*, vol. 76, no. 21, pp. 3118-3120, May2000.

[90] N. Maeda, T. Saitoh, K. Tsubaki, T. Nishida, and N. Kobayashi, "Two-dimensional electron gas transport properties in AlGaN/GaN single- and double-heterostructure field effect transistors," *Materials Science and Engineering B*, vol. 82, no. 1-3, pp. 232-237, May2001.

[91] D. Jena, S. Heikman, D. Green, D. Buttari, R. Coffie, H. Xing, S. Keller, S. DenBaars, J. S. Speck, U. K. Mishra, and I. Smorchkova, "Realization of wide electron slabs by polarization bulk doping in graded III-V nitride semiconductor alloys," *Applied Physics Letters*, vol. 81, no. 23, pp. 4395-4397, Dec.2002.

[92] A. Hinoki, J. Kikawa, T. Yamada, T. Yamada, S. Kamiya, M. Kurouchi, K. Kosaka, T. Araki, A. Suzuki, and Y. Nanishi, "Effects of Traps Formed by Threading Dislocations on Off-State Breakdown Characteristics in GaN Buffer Layer in AlGaN/GaN Heterostructure Field-Effect Transistors," *Appl. Phys. Express*, vol. 1, pp. 011103-1-011103-3, 2008.

[93] J.Neugebauer and C.G.Van de Walle, "Atomic geometry and electronic structure of native defects in GaN," *Phys. Rev. B*, vol. 50, no. 11, pp. 8067-8070, Sept.1994.

[94] J. E. Northrup, "Screw dislocations in GaN: The Ga-filled core model," *Applied Physics Letters*, vol. 78, no. 16, pp. 2288-2290, Apr.2001.

[95] F. Brunner, O. Reentilä, J. Würfl, and M. Weyers, "Strain engineering of AlGaN-GaN HFETs grown on 3 inch 4H-SiC," *physica status solidi (c)*, vol. 6, no. S2, p. S1065-S1068, 2009.

[96] W. Liu and A. A. Balandin, "Thermal conduction in $Al_xGa_{1-x}N$ alloys and thin films," *Journal of Applied Physics*, vol. 97, no. 7, pp. 073710-073716, Apr.2005.

[97] P. Ivo, A. Glowacki, R. Pazirandeh, E. Bahat-Treidel, R. Lossy, J. Wurfl, C. Boit, and G. Trankle, "Influence of GaN cap on robustness of AlGaN/GaN HEMTs," in *Reliability Physics Symposium, 2009 IEEE International* 2009, pp. 71-75.

[98] P. Ivo, R. Pazirandeh, E. Bahat-Treidel, O. Hilt, R. Lossy, J. Würfl, and G. Trankle, "GaN HEMT Critical Voltage Determination by DC-Step-Stress Tests,"

in *The 32nd Workshop on Compound Semiconductor Devices and Integrated Circuits, abstract book*. M. Germain, Ed. Leuven, Belgium: 2008, pp. 129-130.

[99] H. Chen, Z. Lai, S. C. Kung, R. M. Penner, Y. C. Chou, R. Lai, M. Wojtowicz, and G. P. Li, "Observing Electroluminescence from Yellow Luminescence-Like Defects in GaN High Electron Mobility Transistors," *Jpn. J. Appl. Phys.*, vol. 47, no. 5, p. 3336, May2008.

[100] J. Joh, L. Xia, and J. A. del Alamo, "Gate Current Degradation Mechanisms of GaN High Electron Mobility Transistors," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International* 2007, pp. 385-388.

[101] P. B. Klein, J. Freitas, S. C. Binari, and A. E. Wickenden, "Observation of deep traps responsible for current collapse in GaN metal-semiconductor field-effect transistors," *Applied Physics Letters*, vol. 75, no. 25, pp. 4016-4018, Dec.1999.

[102] P. B. Klein, S. C. Binari, K. Ikossi-Anastasiou, A. E. Wickenden, D. D. Koleske, R. L. Henry, and D. S. Katzer, "Investigation of traps producing current collapse in AlGaN/GaN high electron mobility transistors," *Electronics Letters*, vol. 37, no. 10, pp. 661-662, 2001.

[103] G. Meneghesso, F. Zanon, M. J. Uren, and E. Zanoni, "Anomalous Kink Effect in GaN High Electron Mobility Transistors," *Electron Device Letters, IEEE*, vol. 30, no. 2, pp. 100-102, 2009.

[104] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, H.-J. Würfl, and G. Tränkle, "AlGaN/GaN/GaN:C back-barrier HFETs with breakdown voltage of over 1kV and low $R_{on}{\times}A$," *Electron Devices, IEEE Transactions on*, vol.57, no.11, pp.3050-3058, November 2010.

[105] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, H.-J. Würfl, and G. Tränkle, "GaN-Based HEMTs With Insulating-GaN Back-Barrier For Breakdown Voltage Over 1 kV And Low ON-State Resistance," in *The 34ed Workshop on Compound Semiconductor Device and Integrated Circuits, Extended Abstracts Book*. Dimitris Pavlidis, Ed. 2010, pp. 93-94.

[106] N. Q. Zhang, B. Moran, S. P. DenBaars, U. K. Mishra, X. W. Wang, and T. P. Ma, "Effects of surface traps on breakdown voltage and switching speed of GaN power switching HEMTs," in *Electron Devices Meeting, 2001.IEDM Technical Digest.International* 2001, p. 25.

[107] W. Saito, I. Omura, T. Ogura, and H. Ohashi, "Theoretical limit estimation of lateral wide band-gap semiconductor power-switching device," *Solid-State Electronics*, vol. 48, no. 9, pp. 1555-1562, Sept.2004.

[108] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "On-Resistance Modulation of High Voltage GaN HEMT on Sapphire Substrate Under High Applied Voltage," *Electron Device Letters, IEEE*, vol. 28, no. 8, pp. 676-678, 2007.

[109] J. Neugebauer and C. Van de Walle, "Native defects and impurities in GaN," in *Festkörper Probleme Advances in Solid State Physics,* 35ed. Reinhard Helbig, Ed. Springer Berlin / Heidelberg, 1995, pp. 25-44.

[110] J. B. Webb, H. Tang, S. Rolfe, and J. A. Bardwell, "Semi-insulating C-doped GaN and high-mobility AlGaN/GaN heterostructures grown by ammonia molecular beam epitaxy," *Applied Physics Letters*, vol. 75, no. 7, pp. 953-955, Aug.1999.

[111] S. Keller, Y.-F Wu, G. Parish, N.-Q. Zhang, J. J. Xu, B. P. Keller, S. P. DenBaars,

and U. K. Mishra, "Gallium nitride based high power heterojunction field effect transistors: process development and present status at UCSB," *Electron Devices, IEEE Transactions on*, vol. 48, no. 3, pp. 552-559, 2001.

[112] N. Ikeda, L. Jiang, and S. Yoshida, "Normally-off operation power AlGaN/GaN HFET," in *Power Semiconductor Devices and ICs, 2004. Proceedings. ISPSD '04. The 16th International Symposium on* 2004, pp. 369-372.

[113] Y. C. Choi, M. Pophristic, B. Peres, M. G. Spencer, and L. F. Eastman, "Fabrication and characterization of high breakdown voltage AlGaN/GaN heterojunction field effect transistors on sapphire substrates," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 24, no. 6, pp. 2601-2605, 2006.

[114] O. Lopatiuk, L. Chernyak, Y. Feldman, and K. Gartsman, "Studies of electron trapping in GaN doped with carbon," *Thin Solid Films*, vol. 515, no. 10, pp. 4365-4368, Mar.2007.

[115] Y. Niiyama, S. Kato, Y. Sato, M. Iwami, J. Li, H. Takehara, H. Kambayashi, N. Ikeda, and S. Yoshida, "Fabrication of AlGaN/GaN HFET with a High Breakdown Voltage on 4-inch Si (111) Substrate by MOVPE," *Mater. Res. Soc. Symp. Proc.*, vol. 955, p. 0955-I16-06, 2007.

[116] H. Tang, J. B. Webb, J. A. Bardwell, S. Raymond, J. Salzman, and C. Uzan-Saguy, "Properties of carbon-doped GaN," *Applied Physics Letters*, vol. 78, no. 6, pp. 757-759, Feb.2001.

[117] C. Poblenz, P. Waltereit, S. Rajan, S. Heikman, U. K. Mishra, and J. S. Speck, "Effect of carbon doping on buffer leakage in AlGaN/GaN high electron mobility transistors," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 22, no. 3, pp. 1145-1149, May2004.

[118] Z. Chen, Y. Pei, S. Newman, R. Chu, D. Brown, R. Chung, S. Keller, S. P. DenBaars, S. Nakamura, and U. K. Mishra, "Growth of AlGaN/GaN heterojunction field effect transistors on semi-insulating GaN using an AlGaN interlayer," *Applied Physics Letters*, vol. 94, no. 11, pp. 112108-3, Mar.2009.

[119] P. B. Klein, S. C. Binari, K. Ikossi, A. E. Wickenden, D. D. Koleske, and R. L. Henry, "Current collapse and the role of carbon in AlGaN/GaN high electron mobility transistors grown by metalorganic vapor-phase epitaxy," *Applied Physics Letters*, vol. 79, no. 21, pp. 3527-3529, Nov.2001.

[120] S. Rajan, A. Chakraborty, U. K. Mishra, C. Poblenz, P. Waltereit, and J. S. Speck, "MBE-grown AlGaN/GaN HEMTs on SiC," in *High Performance Devices, 2004. Proceedings. IEEE Lester Eastman Conference on* 2004, pp. 108-113.

[121] N. Ikeda, J. Li, K. Kato, S. Kaya, T. Kazama, T. Kokawa, Y. Sato, M. Iwami, T. Nomura, M. Masuda, and S. Kato, "High-Power GaN HFETs on Si Substrate," *Furukawa Review*, vol. 34, pp. 17-23, 2008.

[122] J. Selvaraj, S. L. Selvaraj, and T. Egawa, "Effect of GaN Buffer Layer Growth Pressure on the Device Characteristics of AlGaN/GaN High-Electron-Mobility Transistors on Si," *Jpn. J. Appl. Phys.*, vol. 48, pp. 121002-1-121002-4, Dec.2009.

[123] in *http://www.3m.com/*.

[124] Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "Recent advances of high voltage AlGaN/GaN power HFETs," in *Proc. SPIE, Gallium Nitride Materials and Devices IV,* 7216 ed. H. Morkoc, C. W. Litton, J. I. Chyi, Y. Nanishi, J. Piprek, and

E. Yoon, Eds. San Jose, CA, USA: SPIE, 2009, pp. 721606-721611.

[125] Y. Uemoto, D. Shibata, M. Yanagihara, H. Ishida, H. Matsuo, S. Nagai, N. Batta, L. Ming, T. Ueda, T. Tanaka, and D. Ueda, "8300V Blocking Voltage AlGaN/GaN Power HFET with Thick Poly-AlN Passivation," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International* 2007, pp. 861-864.

[126] J. Shi, L. F. Eastman, X. Xin, and M. Pophristic, "High performance AlGaN/GaN power switch with HfO_2 insulation," *Applied Physics Letters*, vol. 95, no. 4, p. 042103, July2009.

[127] E. Bahat-Treidel, O. Hilt, F. Brunner, V. Sidorov, J. Würfl, and G. Trankle, "AlGaN/GaN/AlGaN DH-HEMTs breakdown voltage enhancement using Multiple Grating Field Plates (MGFPs)," *Electron Devices, IEEE Transactions on*, vol. 57, no. 6, pp. 1208-1216, June2010.

[128] D. M. Sathaiya and S. Karmalkar, "Edge Effects on Gate Tunneling Current in HEMTs," *Electron Devices, IEEE Transactions on*, vol. 54, no. 10, pp. 2614-2622, 2007.

[129] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate," *Electron Devices, IEEE Transactions on*, vol. 48, no. 8, pp. 1515-1521, 2001.

[130] A. Chini, D. Buttari, R. Coffie, S. Heikman, S. Keller, and U. K. Mishra, "12 W/mm power density AlGaN/GaN HEMTs on sapphire substrate," *Electronics Letters*, vol. 40, no. 1, pp. 73-74, 2004.

[131] Y. Okamoto, Y. Ando, T. Nakayama, K. Hataya, H. Miyamoto, T. Inoue, M. Senda, K. Hirata, M. Kosaki, N. Shibata, and M. Kuzuhara, "High-power recessed-gate AlGaN-GaN HFET with a field-modulating plate," *Electron Devices, IEEE Transactions on*, vol. 51, no. 12, pp. 2217-2222, 2004.

[132] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Influence of surface defect charge at AlGaN-GaN-HEMT upon Schottky gate leakage current and breakdown voltage," *IEEE Transactions on Electron Devices*, vol. 52, no. 2, pp. 159-164, Feb.2005.

[133] E. Bahat-Treidel, V. Sidorov, and J. Würfl, "Semiconductor Component and Method for Producing the Same,"WIPO Patent Application Patent WO/2008/101989, Aug.28, 2008.

[134] S. Karmalkar, D. Jianyu, and M. S. Shur, "RESURF AlGaN/GaN HEMT for high voltage power switching," *Electron Device Letters, IEEE*, vol. 22, no. 8, pp. 373-375, 2001.

[135] E. Bahat-Treidel, R. Lossy, J. Wurfl, and G. Trankle, "AlGaN/GaN HEMT With Integrated Recessed Schottky-Drain Protection Diode," *Electron Device Letters, IEEE*, vol. 30, no. 9, pp. 901-903, 2009.

[136] J. Würfl, R. Lossy, E. Bahat-Treidel, A. Wentzel, C. Meliani, and G. Trankle, "Fast Switching AlGaN/GaN-HEMT with Integrated Recessed Schottky-Drain Protection Diode for Class-S Microwave Amplifiers," in *The 33^{ed} Workshop on Compound Semiconductor Device and Integrated Circuits, Extended Abstracts Book*. F. Calle, Ed. Málaga, Spain: 2009, pp. 18-19.

[137] H. Shigematsu, Y. Inoue, S. Masuda, M. Yamada, M. Kanamura, T. Ohki, K. Makiyama, N. Okamoto, K. Imanishi, T. Kikkawa, K. Joshin, and N. Hara, "C-Band GaN-HEMT Power Amplifier with Over 300-W Output Power and Over 50-

% Efficiency," in *Compound Semiconductor Integrated Circuits Symposium, 2008. CSICS '08. IEEE* 2008, pp. 1-4.

[138] C. Meliani, J. Flucke, A. Wentzel, J. Wurfl, W. Heinrich, and G. Trankle, "Switch-mode amplifier ICs with over 90% efficiency for Class-S PAs using GaAs-HBTs and GaN-HEMTs," in *Microwave Symposium Digest, 2008 IEEE MTT-S International* 2008, pp. 751-754.

[139] W. Chen, K.-Y. Wong, and K. J. Chen, "Monolithic Integration of Lateral Field-Effect Rectifier with Normally-off HEMT for GaN-on-Si Switch-mode Power Supply Converters," in *Electron Devices Meeting, 2008.IEDM Technical Digest.IEEE International* 2009.

[140] Hidetoshi Ishida, Daisuke Shibata, Hisayoshi Matsuo, Manabu Yanagihara, Yasuhiro Uemoto, Tetsuzo Ueda, Tsuyoshi Tanaka, and Daisuke Ueda, "GaN-based Natural Super Junction Diodes with Multi-channel Structures," in *Electron Devices Meeting, 2008.IEDM Technical Digest.IEEE International* 2008.

[141] S. Gao, H. Xu, S. Heikman, U. Mishra, and R. A. York, "Microwave class-E GaN power amplifiers," in *Microwave Conference Proceedings, 2005. APMC 2005. Asia-Pacific Conference Proceedings,* 2 ed 2005, p. 4.

[142] J. W. Johnson, J. Gao, K. Lucht, J. Williamson, C. Strautin, J. Riddle, R. Therrien, P. Rajagopal, J. C. Roberts, A. Vescan, J. D. Brown, A. Hanson, S. Singhal, R. Borges, E. L. Piner, and K. J. Linthicum, "Material, Process, and Device Development of GaN-based HFETs on Silicon Substrates," *Electrochemical Society Proceedings*, vol. 2004, no. 06, pp. 405-419, 2004.

[143] X. Chuan, W. Jinyan, C. Hongwei, X. Fujun, D. Zhihua, H. Yilong, and P. Cheng Wen, "The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaN/GaN Heterostructure," *Electron Device Letters, IEEE*, vol. 28, no. 11, pp. 942-944, 2007.

[144] C. Young-Hwan, L. Jiyong, J. In-Hwan, C. Kyu-Heon, K. Young-Shil, and H. Min-Koo, "AlGaN/GaN HEMT without Schottky contact on the dry-etched region for high breakdown voltage," in *Semiconductor Device Research Symposium, 2007 International* 2007, pp. 1-2.

[145] A. Glowacki, P. Laskowski, C. Boit, P. Ivo, E. Bahat-Treidel, R. Pazirandeh, R. Lossy, J. Würfl, and G. Tränkle, "Characterization of stress degradation effects and thermal properties of AlGaN/GaN HEMTs with photon emission spectral signatures," *Microelectronics Reliability*, vol. 49, no. 9-11, pp. 1211-1215, Sept.2009.

Appendix A: Silvaco-“ATLAS“ Command Scripts

Silvaco “ATLAS” Basic Command Script for GaN-Based HEMT

```
########################################
####  Bench Mark FBH 2X50A2 device     #####
####  Created by: Eldad Bahat-Treidel  #####
####  All rights received               #####
####  Ver. 260207                      #####
########################################

go atlas

###### Set test case labels ###################

mesh  infile = filename.str width=100

##### Region and polarization statments modifications ######################

region modify number=4 material = 4H-SiC     insulator
region modify number=3 material = AlN        substrate                    polarization calc.strain polar.scale = -1.0
region modify number=2 material = GaN                                     polarization calc.strain polar.scale = -1.0
region modify number=1 material = AlGaN      x.comp=0.25 grad.34=0.0      polarization calc.strain polar.scale = -0.795

################### Ohmic Contacts doping ##################################

doping uniform x.min=0.0 x.max=1.0 y.min=0.00 y.max=0.03 n.type conc=5.0e20
doping uniform x.min=4.3 x.max=5.3 y.min=0.00 y.max=0.03 n.type conc=5.0e20

################### Material statments modifications ######################

material number=1 TC.A=0.666 TC.B=0 TC.C=0 HC.A=1.97  HC.B=0.00036 HC.C=0 HC.D=-3.7e+4 tcon.polyn hc.std
material number=1 name=AlGaN align=0.65 pip.omega=0.07 pip.acc=2 pip.et=1 pip.nt=1.2e13
material number=2 tcon.polyn
material number=3 tcon.polyn
material number=4 affinity=4.422 tcon.polyn

######################### Interface and traps ##############################

trap e.level=0.70 acceptor density=5.5e15 degen=1 taun0=1e-12 taup0=2e-11 region=2

#############################################################################

material number=1          pol.set1          kp.set1
material number=2          pol.set1          kp.set1
material number=3          pol.set1          kp.set1

############## Models ######################################################

models material=AlN        k.p Chuang fldmob print lat.temp  HEAT.FULL
models material=GaN        k.p Chuang fldmob print lat.temp  HEAT.FULL
models material=AlGaN      k.p Chuang fldmob print lat.temp  HEAT.FULL

################ Mobility Modeling #########################################

mobility material=AlN      fmct.n print
mobility material=AlGaN    fmct.n print
mobility material=GaN      fmct.n mu1n.fmct=3500.0 mu2n.fmct=4665 alphan.fmct=0.66 betan.fmct=-3.02 deltan.fmct=-
3.84
                           gamman.fmct=3.02 epsn.fmct=0.81 ncritn.fmct=1e17       print
mobility material=GaN      n.canali n.beta0=0.635 n.betaexp=0.30
```

```
########## Contact definitions ##############################################

contact name=gate           workfunction=4.892 pipinys thermionic surf.rec me.tunnel=0.050 barrier
contact name=source         resist=250
contact name=drain          resist=250
thermcontact num=1          x.min=0.0 x.max=5.3 y.min=2.465 y.max=22.465 temp=300 ^boundary alpha=1.7

########## Culculation method ################################################

method gumits=300 autonr block nblockit=50 carr=1 electrons min.temp=300 stack=10 itlimit=20

###############################################################################
```

Silvaco “ATLAS” Schrödinger Equation Solver Command Script for GaN HEMT

```
# Created by: Melanie Cho #

go atlas

mesh infile = SCH-GaN_buffer-200nm.str

region modify num = 1 material = AlGaN x.comp = 0.25 calc.strain polarization polar.scale = -0.7
region modify num = 2 material = GaN                                polarization polar.scale = -0.7

material numbe r= 1 align = 0.75

doping uniform x.min = 0.0 x.max = 1.0 y.min = 0.0 y.max = 0.03 n.type conc = 5e18
doping uniform x.min = 4.3 x.max = 5.3 y.min = 0.0 y.max = 0.03 n.type conc = 5e18

spx.mesh loc = 0          spac = 0.01
spx.mesh loc = 5.3        spac = 0.01
spy.mesh loc = 0          spac = 0.001
spy.mesh loc = 0.01       spac = 0.0001
spy.mesh loc = 0.135      spac = 0.001
spy.mesh loc = 0.2        spac = 0.001

models k.p schro fixed.fermi srh sp.geom = 1dy qmincon = 1e-9 npred.negf = 10 num.direct = 1 sp.dir = 0

output con.band val.band band.param polar.charge eigens = 3 qss x.com
method gummel newton carriers = 0 maxtrap = 4

contact name = gate workfunc = 4.4
contact name = source surf.rec
contact name = drain surf.rec

solve init
solve vgate=0
```

Author's List of Publications

Reviewed Journal Publications

E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, H.-J. Würfl, and G. Tränkle, "AlGaN/GaN/GaN:C back-barrier HFETs with breakdown voltage of over 1kV and low R_{ON}×A," *Electron Devices, IEEE Transactions on*, vol.57, no.11, pp.3050-3058, November 2010.

E. Bahat-Treidel, O. Hilt, F. Brunner, V. Sidorov, J. Würfl, and G. Trankle, "AlGaN/GaN/AlGaN DH HEMTs breakdown voltage enhancement using Multiple Grating Field Plates (MGFPs)," *Electron Devices, IEEE Transactions on*, vol. 57, no. 6, pp. 1208-1216, June2010.

C.-Y. Lu, **E. Bahat-Treidel**, O. Hilt, R. Lossy, N. Chaturverdi, E. Y. Chang, J. Würfl, and G. Tränkle, "Influence of the device geometry on the Schottky gate characteristics of AlGaN/GaN HEMTs," *Semiconductor Science and Technology*, vol. 25, no. 7, p. 075005, June2010.

E. Bahat-Treidel, O. Hilt, F. Brunner, H.-J. Würfl, and G. Tränkle, "AlGaN/GaN/AlGaN Double Heterojunction HEMTs on *n*-type SiC Substrates," *physica status solidi (c)*, Vol. 7, No. 10, pp. 2407-2411, 2010.

I. Khalil, **E. Bahat-Treidel**, F. Schnieder, and J. Wurfl, "Improving the Linearity of GaN HEMTs by Optimizing Epitaxial Structure," *Electron Devices, IEEE Transactions on*, vol. 56, no. 3, pp. 361-364, Mars 2009.

Eldad Bahat-Treidel, Ibrahim Khalil, Oliver Hilt, Joachim Würfl, and Günther Tränkle, "Engineered linearity of GaN-based HEMTs power devices by tailoring transfer characteristics," *physica status solidi (c)*, vol. 6, no. 6, pp. 1378-1381, 2009.

Eldad Bahat-Treidel, Oliver Hilt, Frank Brunner, Joachim Würfl, and Günther Tränkle, "Punch-through voltage enhancement scaling of AlGaN/GaN HEMTs using AlGaN double heterojunction confinement," *physica status solidi (c)*, vol. 6, no. 6, pp. 1373-1377, 2009.

E. Bahat-Treidel, R. Lossy, J. Wurfl, and G. Trankle, "AlGaN/GaN HEMT With Integrated Recessed Schottky-Drain Protection Diode," *Electron Device Letters, IEEE*, vol. 30, no. 9, pp. 901-903, 2009.

A. Glowacki, P. Laskowski, C. Boit, P. Ivo, **E. Bahat-Treidel**, R. Pazirandeh, R. Lossy, J. Würfl, and G. Tränkle, "Characterization of stress degradation effects and thermal properties of AlGaN/GaN HEMTs with photon emission spectral signatures," *Microelectronics Reliability*, vol. 49, no. 9-11, pp. 1211-1215, Sept.2009.

E. Bahat-Treidel, O. Hilt, F. Brunner, J. Wurfl, and G. Trankle, "Punchthrough-Voltage Enhancement of AlGaN/GaN HEMTs Using AlGaN Double-Heterojunction Confinement," *Electron Devices, IEEE Transactions on*, vol. 55, no. 12, pp. 3354-3359, 2008.

B. Apter, **E. Bahat-Treidel**, and U. Efron, "Continuously controllable, wide-angle liquid crystal beam deflector based on the transversal field effect in a three-electrode cell," *Optical Engineering*, vol. 44, no. 5, pp. 054001-054007, May2005.

U. Efron, B. Apter, and **E. Bahat-Treidel**, "Studies of fringing field effects in liquid crystal beam-steering devices," *Proc. SPIE, Liquid Crystals IX*, vol. 5936, no. 1, pp. 59360P-593612, Aug.2005.

B. Apter, **E. Bahat-Treidel**, and U. Efron, "Electro-optical wide-angle beam deflection based on transversal-field-induced refractive inhomogeneity in a liquid crystal layer," *Proc. SPIE, Free-Space Laser Communications V*, vol. 5892, no. 1, p. 58921B, Aug.2005.

E. Bahat-Treidel, B. Apter, and U. Efron, "Experimental study of phase-step broadening by fringing fields in a three-electrode liquid-crystal cell," *Appl. Opt.*, vol. 44, no. 15, pp. 2989-2995, May2005.

E. Bahat-Treidel, B. Apter, and U. Efron, "Simple method for controlled variation of liquid crystal cell thickness," *Optical Engineering*, vol. 43, no. 12, pp. 3021-3025, Dec.2004.

U. Efron, B. Apter, and **E. Bahat-Treidel**, "Fringing-field effect in liquid-crystal beam-steering devices: an approximate analytical model," *J. Opt. Soc. Am. A*, vol. 21, no. 10, pp. 1996-2008, Oct.2004.

B. Apter, U. Efron, and **E. Bahat-Treidel**, "On the Fringing-Field Effect in Liquid-Crystal Beam-Steering Devices," *Appl. Opt.*, vol. 43, no. 1, pp. 11-19, Jan.2004.

Patents

I. Khalil, **E. Bahat-Treidel**, J. Würfl, and O. Hilt, "Electrical devices having improved transfer characteristics and method for tailoring the transfer characteristics of such an electrical device," European Patent Office Patent EP2040299 (A1), Mar.25, 2009.

E. Bahat-Treidel, V. Sidorov, and J. Würfl, "Semiconductor Component and Method for Producing the Same,"WIPO Patent Application Patent WO/2008/101989, Aug.28, 2008.

J. Würfl and **E. Bahat-Treidel**, "Shottky Drain Transistoren," Germany Application Patent 10 2008 045 241.6, Aug.28, 2008.

Conference Proceedings

E. Bahat-Treidel, O. Hilt, F. Brunner, V. Sidorov, H.-J. Würfl, and G. Tränkle, "GaN-Based Double Heterojunction HEMTs' Breakdown Voltage Enhancement Using Multiple Grating Field Plates," in *The 34ed Workshop on Compound Semiconductor Device and Integrated Circuits*, Extended Abstracts Book. Dimitris Pavlidis, Ed. 2010, pp. 21-22.

E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, H.-J. Würfl, and G. Tränkle, "GaN-Based

HEMTs With Insulating-GaN Back-Barrier For Breakdown Voltage Over 1 kV And Low ON-State Resistance," in *The 34ed Workshop on Compound Semiconductor Device and Integrated Circuits*, Extended Abstracts Book. Dimitris Pavlidis, Ed. 2010, pp. 93-94.

S. A. Chevtchenko, O. Bengtsson, F. Brunner, **E. Bahat-Treidel**, and H.-J. Würfl, "Two-Tone Intermodulation Distortion Characterization Of AlGaN/GaN HFETs Fabricated On Different Epitaxial Structures," in *The 34ed Workshop on Compound Semiconductor Device and Integrated Circuits*, Extended Abstracts Book. Dimitris Pavlidis, Ed. 2010, pp. 27-28.

P. Ivo, A. Glowacki, **E. Bahat-Treidel**, R. Lossy, H.-J. Würfl, C. Boit, and G. Tränkle, "Comparative study of AlGaN/GaN HEMTs robustness versus buffer design variations by applying electroluminescence and electrical measurements," in *Reliability Of Compound Semiconductors Workshop*. Peter Ersland, Ed. 2010.

O. Hilt, A. Knauer, F. Brunner, **E. Bahat-Treidel**, and H.-J. Würfl, "Normally-off AlGaN/GaN HFET with *p*-type GaN Gate and AlGaN Buffer," *Power Semiconductor Devices & IC's (ISPSD), 2010 22nd International Symposium on* , vol., no., pp.347-350, 6-10 June 2010.

O. Hilt, A. Knauer, F. Brunner, **E. Bahat-Treidel**, and H.-J. Würfl, "Normally-off AlGaN/GaN HFET with *p*-type GaN Gate and AlGaN Buffer," in *6th International Conference on Integrated Power Electronic Systems*. J.Daan van Wyk and Leo Lorenz, Eds. 2010, pp. 185-188.

J. Würfl, R. Lossy, **E. Bahat-Treidel**, A. Wentzel, C. Meliani, and G. Tränkle, "Fast Switching AlGaN/GaN-HEMT with Integrated Recessed Schottky-Drain Protection Diode for Class-S Microwave Amplifiers," in *The 33ed Workshop on Compound Semiconductor Device and Integrated Circuits*, Extended Abstracts Book. F. Calle, Ed. Málaga, Spain: 2009, pp. 18-19.

E. Bahat-Treidel, O. Hilt, F. Brunner, J. Würfl, and G. Tränkle, "AlGaN/GaN/AlGaN Double Heterojunction HEMTs on *n*-type SiC Substrates," in *The 36th International Symposium on Compound Semiconductors*. U. K. Mishra, Ed. 2009, pp. 369-370.

P. Ivo, A. Glowacki, R. Pazirandeh, **E. Bahat-Treidel**, R. Lossy, J. Würfl, C. Boit, and G. Tränkle, "Influence of GaN cap on robustness of AlGaN/GaN HEMTs," in *Reliability Physics Symposium*, 2009 IEEE International 2009, pp. 71-75.

F. Brunner, **E. Bahat-Treidel**, O. Hilt, J. Würfl, and M. Weyers, "Growth and Characterization of AlGaN-GaN HFETs on 3 inch 4H-SiC designed for High-Voltage Operation," in *8th International Conference on Nitride Semiconductors* ICC Jeju, Korea: 2009, p. TP142.

E. Bahat-Treidel, O. Hilt, F. Brunner, J. Würfl, and G. Tränkle, "AlGaN/GaN HEMTs Breakdown Voltage Enhancement using AlGaN Double Heterojunction Buffer Confinement," in *The 32nd Workshop on Compound Semiconductor Devices and Integrated Circuits*, abstract book. M. Germain, Ed. Leuven, Belgium: 2008, pp. 23-24.

O. Hilt, **E. Bahat-Treidel**, V. Sidorov, and J. Würfl, "Gate-Length Dependent on-state 2DEG Constriction in AlGaN/GaN HEMTs," in *The 32nd Workshop on Compound Semiconductor Devices and Integrated Circuits*, abstract book. M. Germain, Ed. Leuven, Belgium: 2008, pp. 29-30.

M. J. Uren, S. W. Smith, **E. Bahat-Treidel**, I. Khalil, J. Würfl, V. Krozer, K. Hirche, and A. R. Barnes, "Intermodulation Distortion in GaN HEMTs," in *The 32nd Workshop on Compound Semiconductor Devices and Integrated Circuits*, abstract book. M. Germain, Ed. Leuven, Belgium: 2008, pp. 103-104.

P. Ivo, R. Pazirandeh, **E. Bahat-Treidel**, O. Hilt, R. Lossy, J. Würfl, and G. Tränkle, "GaN HEMT Critical Voltage Determination by DC-Step-Stress Tests," in *The 32nd Workshop on Compound Semiconductor Devices and Integrated Circuits*, abstract book. M. Germain, Ed. Leuven, Belgium: 2008, pp. 129-130.

E. Bahat-Treidel, O. Hilt, F. Brunner, J. Würfl, and G. Tränkle, "Punch-through voltage enhancement scaling of AlGaN/GaN HEMTs using AlGaN double heterojunction confinement," in *35th International Symposium on Compound Semiconductors*, abstract book. O. Ambacher, Ed. Rust, Germany: 2008, p. Tu 2.4.

E. Bahat-Treidel, I. Khalil, O. Hilt, J. Würfl, and G. Tränkle, "Engineered linearity of GaN-based HEMTs power devices by tailoring transfer characteristics," in *35th International Symposium on Compound Semiconductors*, abstract book. O. Ambacher, Ed. Rust, Germany: 2008, p. P27.

E. Bahat-Treidel, J. Würfl, and G. Tränkle, "Breakdown voltage simulation of AlGaN/GaN HEMTs on 4H-SiC," in The 31st *Workshop on Compound Semiconductor Device and Integrated Circuits*. G. Meneghesso, Ed. Venice, Italy: 2007, pp. 303-305.

E. Bahat-Treidel, V. Sidorov, J. Würfl, and G. Tränkle, "Simulation of AlGaN/GaN HEMTs' breakdown voltage enhancement using grating field plates," in *Simulation of Semiconductor Processes and Devices 2007*, 12 ed. T. Grasser and S. Selbererr, Eds. Vienna: Springer Vienna, 2007, pp. 277-279.

B. Apter, **E. Bahat-Treidel**, and U. Efron, "Electrooptical wide-angle beam deflector based on fringing-field-induced refractive inhomogeneity in a liquid crystal layer," *Electrical and Electronics Engineers in Israel, 2004. Proceedings*. 2004 23rd IEEE Convention of, pp. 240-243, 2004.

תקציר

טרנזיסטורי תוצא-השדה המבוססים על מערכות המוליכים למחצה מסוג גליום-ניטריד עבור מערכות מיתוג חשמליות במתח והספק גבוהים לשימושי חלל נלמדו בעבודה זו. יעילות המיתוג במערכות הספק גבה קשורה לגובה הממתח במצב סגור כאשר ההתנגדות במצב פתוח, פיזור הזרם הדינמי וזרמי הזליגה קטנים ככל שניתן. יכולת ההתקן לפעול בממתח גבה תלויה בשרשרת של גורמים מגבילים כגון זרמי זליגה מתחת לסף הרחש ותצורה גאומטרית. בעבודה זו נעשה שימוש בכלי סימולציה המבוססים על מודלים פיזקלים ככלי הנדסי שפותח לניתוח אופן הפעולה, הבנה ותכנון רעיונות מתקדמים. שיפור יכולת החסימה במתחים גבוהים היא משימה מורכבת הדורשת פיתרון מקבילי במספר דרכים; תכנון גידול השכבות האפיטקסיאליות, תכנון גאומטרית ומבנה ההתקן, והתאמת תהליכי יצור מתאימים. התקנים ייחודים בעלי מחסום תחתי העשוי חומר רחב רווח אסור אלומיניום-גליום-ניטריד או גליום-נטריד מסומם בפחמן וכן שילוב גאומטריה ייחודית של לוחות שדה. אפיון ההתקנים במתח ישר הראה דיכוי משמעותי של זרמי הזליגה וכתוצאה מכך העלאה של הממתח ללמעלה מ-1000 V כאשר ההתנגדות במצב פתוח נשארה נמוכה מאוד. תכנון ייחודי של מערך ההתקן מנע התמוטטות מוקדמת של ההתקן הנובעת מקרבה צידת שבין מוליכים בעלי מתח גבוה. מיטוב ותכנון הבידוד הבין-התקני למתח גבוה מנע הצורה ניכרת זרמי זליגה. בעוד שמירב המאמצים נעשים לשיפור יכולת החסימה של ההתקן בממתח קדמי, התקנים בעלי יכולת חסימה בממתח אחורי נדרשים למספר יישומים. התקן מקורי בעל יכולת חסימה בממתח אחורי עבור מגברי מיתוג מסוג-S הוצג לראשונה. ההגנה ממתח גבוה בממתח אחורי הושגה על מגע מסוג שוטקי בגומחה במוליך למחצה. התקן זה מספק הגנה במתח של יותר מ-110 V.

דף זיכרון – יזכור

לזכרם של בני משפחתי שנרצחו בידי הגרמנים הנאצים מפלצות הצוררים ימ"ש ועזריהם ימ"ש בשואת יהודי אירופה.

יוהנה (אנה) טריידל ז"ל
לבית בנדר מהעיר קובלנץ, נולדה ברביעי לאפריל 1844 ונרצחה בתשע עשר לפברואר 1943 בטרזנשטט.

מקסמיליאן (מקס) טריידל ז"ל
מהעיר קובלנץ, נולד בתשע עשר ליוני 1873 ונרצח בתאריך לא ידוע בטרזנשטט.

קמילה (מילי) טריידל ז"ל
לבית שויער מהעיר קובלנץ, נולדה בשלושים למאי 1883 ונרצחה בתאריך לא ידוע באושוויץ.

הינריך שטראוס ז"ל
מהעיר לודוויגסהפן על הריין, נולד בעשרים ואחד לינואר 1876 ונרצח בתשעי לפברואר 1942 בגורס.

טרזה שטראוס ז"ל
לבית גרן לודוויגסהפן על הריין, נולדה בתשע עשר לפברואר 1890 ונרצחה בתאריך לא ידוע באושוויץ.

יהי זכרם ברוך

Yizkor – Memorial Prayer

In memory of those members of my family that were murdered by the Nazis and their supporters in the Holocaust:

Johanna (Anna) Treidel née Bender
From Koblenz, born in Briedel on April 4, 1844, murdered on February 19, 1943 in Theresienstadt.

Maximilian (Max) Treidel
From Koblenz, born in Mayen on June 19, 1873, murdered in Theresienstadt.

Kamilla (Milli) Treidel née Scheuer
From Koblenz, born in Trier on May 30, 1883, murdered in Auschwitz.

Heinrich Strauss
From Ludwigshafen am Rhein, born in Kindenheim on January 21, 1876, murdered on February 9, 1942 in Gurs.

Therese Strauss née Gern
From Ludwigshafen am Rhein, born in Ludwigshafen am Rhein on February 19, 1890, murdered in Auschwitz.

Yizkor – Gedenkstättengebet

Zum Andenken an diejenigen Mitglieder meiner Familie, die während des Holocaust von den Nationalsozialisten und deren Anhängern ermordet wurden:

Johanna (Anna) Treidel geb. Bender
Aus Koblenz, geboren in Briedel am 4 April 1844, ermordet am 19 Februar 1943 in Theresienstadt.

Maximilian (Max) Treidel
Aus Koblenz, geboren in Mayen am 19 Juni 1873, ermordet in Theresienstadt.

Kamilla (Milli) Treidel geb. Scheuer
Aus Koblenz, geboren in Trier am 30 Mai 1883, ermordet in Auschwitz.

Heinrich Strauss
Aus Ludwigshafen am Rhein, geboren in Kindenheim am 21 Januar 1876, ermordet am 9 Februar 1942 in Gurs.

Therese Strauss geb. Gern
Aus Ludwigshafen am Rhein, geboren in Ludwigshafen am Rhein am 19 Februar 1890, ermordet in Auschwitz.