

TUTORIAL AND REVIEW PAPER

Design and layout strategies for integrated frequency synthesizers with high spectral purity

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Design guidelines for fractional-N phase-locked loops with a high spectral purity of the output signal are presented. Various causes for phase noise and spurious tones (spurs) in integer-N and fractional-N phase-locked loops (PLLs) are briefly described. These mechanisms include device noise, quantization noise folding, and noise coupling from charge pump (CP) and reference input buffer to the voltage-controlled oscillator (VCO) and vice versa through substrate and bondwires. Remedies are derived to mitigate the problems by using proper PLL parameters and a careful chip layout. They include a large CP current, sufficiently large transistors in the reference input buffer, linearization of the phase detector, a high speed of the programmable frequency divider, and minimization of the cross-coupling between the VCO and the other building blocks. Examples are given based on experimental PLLs in SiGe BiCMOS technologies for space communication and wireless base stations.

Keywords: Noise analysis, RF front-ends, Frequency synthesizer

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1. INTRODUCTION

Integrated fractional-N phase-locked loops (PLL) are important building blocks in many communication systems, both in CMOS technology [1, 2] and SiGe BiCMOS [3, 4]. One advantage of SiGe BiCMOS technology is the fact that SiGe HBTs are inherently radiation-hard with respect to gamma-rays, neutrons, and protons [5], which makes this technology a good candidate for space applications.

Figure 1 shows an exemplary charge-pump PLL schematic, both for integer-N and fractional-N operation. In both cases, the voltage-controlled oscillator (VCO) is followed by a pre-scaler with a fixed division ratio of $M = 2^m$, where m is the number of cascaded divide-by-two circuits (DTCs). This pre-scaler is followed by a programmable frequency divider. Its output signal is compared with the PLL input frequency fed through a reference buffer (REF-BUF) in a phase-frequency detector (PFD). The two PFD outputs control a charge pump (CP) connected to a low-pass filter (LPF), which controls the VCO in a feedback loop. The principles of PLLs and their noise properties are described in many textbooks, e.g., in [6]. In modern communication systems CP PLLs (type-II PLLs) are of special interest. Their infinite open-loop gain at DC results in a static phase error of zero between the two inputs to the PFD. Moreover, the PLL frequency tuning

range is only limited by the VCO, that is, there is no difference between hold range and capture range as in traditional mixer-based type-I PLLs. The main disadvantage of integer-N PLLs as depicted in Fig. 1(a) is their limited loop bandwidth resulting from the limited input frequency f_{REF} . For a given channel spacing Δf at the VCO output, the input frequency obeys $f_{REF} \leq \Delta f / M$. The low loop bandwidth limits the PLL settling time and prevents the VCO phase noise from efficient high-pass filtering. The solution to this problem is the fractional-N PLL, where channel spacing and loop bandwidth are decoupled. Here, the division ratio N is not constant, but is dithered around a fractional number. This can formally be described by a perfect fractional-N divider superimposed by quantization noise. The basic idea for obtaining a high spectral purity is to shape this noise such that it has most of its energy at large frequency offsets, where it can be filtered by the LPF. This can be achieved by using a $\Delta\Sigma$ modulator (DSM) [7–9]. In [4] and [10], the value of the fractional number was controlled by a serial-peripheral interface as indicated in Fig. 1(b). Fractional-N PLLs have the potential to reduce the phase noise significantly by using a high input frequency. However, they create a number of new problems such as fractional spurs related to the quantization noise in the DSM and quantization noise folding due to nonlinearities of the PFD/CP phase detector (PD) [8–11]. Moreover, the noise coupling within a silicon chip can result in near-integer boundary spurs. They are not related to the quantization noise in the DSM, but result simply from the fact that the VCO output signal and the reference input signal may have a long common period [12]. Coupling of the high-frequency VCO signal to the reference input buffer through the common

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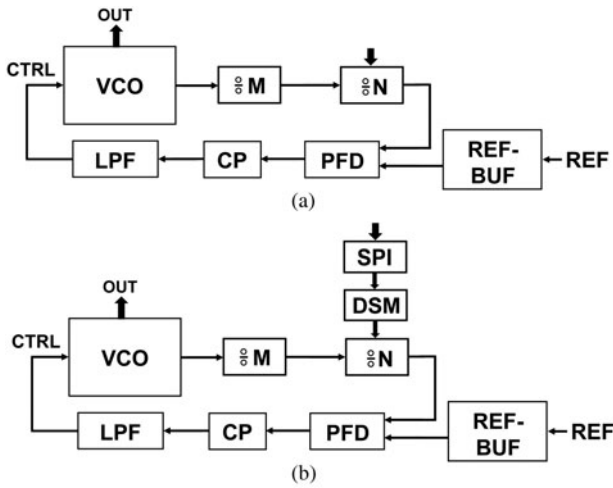


Fig. 1. Synthesizer architecture using a charge pump PLL. (a) Integer-N PLL architecture; (b) fractional-N PLL architecture.

silicon substrate or through bondwires causes a VCO modulation, which may result in large in-band spurs. Mitigation of these problems is mandatory for making fractional-N PLLs with integrated VCOs a possible candidate for flexible payloads in future satellite communication systems [10].

The rest of the paper is organized as follows. Section II describes the main causes for phase noise and spurs in integer-N and fractional-N PLLs. Here, in addition to the classical topics such as device noise and quantization noise in the DSM, problems associated with signal integrity are addressed. Section III briefly outlines methods of noise reduction for each of these noise causes, and Section IV concludes this paper.

II. ORIGIN OF PHASE NOISE AND SPURS

A) Device noise

Each building block of the PLL introduces phase noise. By adding their output noise power spectral densities (PSD) weighted with their noise transfer functions results in the total PLL output phase noise spectrum [6, 13]. The main contributors are typically the reference phase noise at low frequency offsets, noise in reference input buffer and CP at medium offset, and VCO noise at large offsets.

The CP activity in a fractional-N PLL is higher than for the integer-N counterpart. This is due to the higher CP duty cycle $\alpha_{CP} = T_{ON}/T_{REF}$, where T_{ON} is the CP activation time and T_{REF} is the reference period. The PSD of the CP output current due to thermal noise and shot noise is proportional to α_{CP} , whereas $1/f$ noise is proportional to α_{CP}^2 [6]. Adding the two noise contributions, we obtain for the PSD of the CP output current [13]:

$$S_{CP}(f) = S_{CP}^{white} \alpha_{CP} \left(1 + \frac{\alpha_{CP} f_c}{f} \right), \quad (1)$$

where f_c is the $1/f$ noise corner frequency of the transistor. The parameter S_{CP}^{white} corresponds to the CP current noise PSD due to white noise sources at 100% CP duty cycle. Since in a binary weighted CP S_{CP}^{white} is proportional to the CP peak current I_{CP} , we can introduce a figure of merit γ_{CP} for the CP architecture

by $S_{CP}^{white} = \gamma_{CP} I_{CP}$. Transforming the noise current PSD to the PFD input and neglecting $1/f$ noise, we obtain for input-referred phase PSD

$$S_{CP}^{in} = \frac{(2\pi)^2}{I_{CP}} \gamma_{CP} \alpha_{CP}. \quad (2)$$

Next, we consider the reference input buffer. We assume a CMOS inverter chain as input buffer driven by a sinusoidal signal of peak amplitude V_o . The contribution of the first CMOS inverter to the input-referred phase noise can be approximately described by [13]:

$$S_{BUF}^{in} \propto \frac{1}{g_m V_o^2} \quad (3)$$

where g_m is the transconductance. The proportionality constant can be obtained by circuit simulation or by PLL phase noise measurements using small input amplitudes, where this noise contribution is maximized. The expressions (2) and (3) will be helpful for phase noise optimization.

B) Quantization noise

The quantization noise generated by the DSM is folded in the nonlinear PD composed of PFD and CP before it is filtered by the LPF. This effect results in an increased in-band noise floor. The PD linearity can be improved significantly by adding a DC offset current I_{OS} between the CP output and VSS or VDD [14]. In this case, either only the UP current or only the DOWN current of the CP varies in the steady state, and a good matching of UP and DOWN currents is not required. With such a static phase offset, the PD characteristic can be approximated by a second-order polynomial [13]

$$I = K_{PD} \left(\phi + \frac{\beta}{2} \phi^2 \right), \quad (4)$$

where

$$K_{PD} = dI/d\phi = I_{CP}/(2\pi), \quad (5)$$

is the PD gain and

$$\beta = (d^2 I / d\phi^2) / K_{PD}, \quad (6)$$

is the normalized curvature of the PD characteristic at the bias point. The two-sided PD output current PSD reads for Gaussian quantization noise [13]

$$S_{i,QNF} = \frac{K_{PD}^2 \beta^2 \sigma_{\phi,in}^4}{2f_{REF}}, \quad (7)$$

where $\sigma_{\phi,in}$ is the standard deviation of the phase error at the PD input. Transforming $S_{i,QNF}$ to the PD input and from there to the PLL output, we obtain the corresponding PLL phase noise contribution given by

$$S_{\phi,QNF}(f) = \frac{\beta^2 \sigma_{\phi,in}^4}{2f_{REF}} |H(f)|^2, \quad (8)$$

where $|H(f)|^2 \approx (MN)^2$ below the loop bandwidth. This expression has been verified by time-domain simulation in

[15]. The predicted dependencies on β and $\sigma_{\phi, \text{in}}$ were also confirmed, both for phase noise and for fractional spurs.

C) Coupling spurs in fractional-N PLLs

If in a PLL the VCO is integrated, its spectral purity may be affected by coupling between different circuit blocks through bondwires and the common silicon substrate. This may cause spurs at frequency offsets equal to twice the reference frequency. Moreover, in the case of a fractional-N PLL large in-band spurs are observed resulting from modulations of the PD input by VCO leakage.

Let us consider a reference input buffer composed of a cascade of CMOS inverters. This buffer produces a current through the bondwires for ground and supply with twice the input frequency, since the inverters draw current both at the rising edge and the falling edge of the digital signal. The currents in these bondwires may couple to the VCO bondwires through the mutual inductances between REF-BUF and VCO. As a result, the VCO frequency will be modulated with $2f_{\text{REF}}$. A similar effect is observed in the CP, if the CP currents are very large. Here, the coupling spurs occur at an offset equal to $\pm f_{\text{REF}}$. Unlike the classical reference spurs they cannot be reduced by the LPF.

As shown in [12] and [4] the role of noise aggressor and noise victim may be reversed in a fractional-N PLL. The high-frequency VCO output signal may propagate to the reference input buffer and cause modulation spurs. Here, the VCO leakage can propagate through neighboring bondwires of different PLL blocks or through the common silicon substrate. The position of the largest spurs is determined by the distance of $M\alpha$ from the nearest integer number, where α is the fractional part of the division ratio N . For example, for $M = 4$ and $\alpha < 1$ the classical fractional spurs occur at $\pm \alpha f_{\text{REF}}$, but the modulation spurs occur at $\pm 4\alpha f_{\text{REF}}$. This makes it easy to distinguish between spurs related to quantization noise and the modulation spurs, provided that the feedback divider contains a prescaler, i.e., $M > 1$.

Substrate noise is especially troublesome in CMOS technology. As described in [16], a noisy VCO substrate voltage modulates the transistor capacitances in the VCO. Moreover, the transistor transconductances are modulated through the body effect. The sensitivity of the VCO frequency with respect to the substrate noise can be quantified by an according VCO gain $K_{\text{sub}} = df_o/dV_{\text{sub}}$ in hertz per volt. Let $S_{V, \text{sub}}(f)$ be the one-sided substrate voltage PSD. Since the phase represents the integrated frequency, we obtain for the corresponding phase noise spectrum

$$S_{\phi, \text{sub}}(f) = \frac{1}{2} S_{V, \text{sub}}(f) \left(\frac{K_{\text{sub}}}{f} \right)^2. \quad (9)$$

The factor $1/2$ results from the fact that the phase noise spectrum is defined as a two-sided PSD.

III. MITIGATION OF PHASE NOISE AND SPURS

In this section, we will briefly describe the methods of reducing phase noise and spurs based on the results from Section II.

A) Device noise

A high quality factor of the resonator in the VCO is essential for a low phase noise. Moreover, the intrinsic voltage amplitude should be maximized. By using a binary weighted array of switchable capacitors the analog VCO tuning range can be reduced, which also improves the phase noise [4]. For more details the reader is referred to the extensive literature available, such as the books [6, 17] and the references therein.

Next, we turn to the minimization of the in-band phase noise plateau. According to [13], the main contributors to the phase noise plateau are typically the white noise sources in the CP (thermal noise, shot noise), the reference input buffer noise and, in the case of fractional-N PLLs, the quantization noise folded in the nonlinear phase detector. As evident from (2), a high CP current minimizes the phase noise contribution of the devices in the CP. This has been verified in a 10 GHz CMOS PLL [18]. Figure 2 shows the phase noise spectrum of the 10.5 GHz PLL for different CP currents. As predicted by (2), the lowest phase noise is obtained for the highest CP current of 8 mA. This does not necessarily mean that the CP must have a very high power consumption, since the duty cycle α_{CP} is usually on the order of 10% in fractional-N PLLs and much smaller in integer-N PLLs.

Another main phase noise contributor may be the reference input power. When realized as a CMOS inverter chain, the first inverter should have a large g_m as evident from (3). Based on extensive investigations in the context of [18], [10], and [4], we recommend an aspect ratio W/L on the order of 100 for the MOSFETs in the input inverter. The following inverters may use smaller transistors, since they are less sensitive to additive noise due to the large signal slopes at their inputs.

B) Quantization noise f_{REF}

The minimization of quantization-noise-related phase noise and spurs is based on (8). In the following, we will discuss the effect of the reference frequency, the PD nonlinearity parameter β and the PD input rms phase error $\sigma_{\phi, \text{in}}$ on the levels of folded quantization noise and in-band spurs.

Since the total division ratio MN is proportional to $1/f_{\text{REF}}$ for a given output frequency, we conclude from (8) that

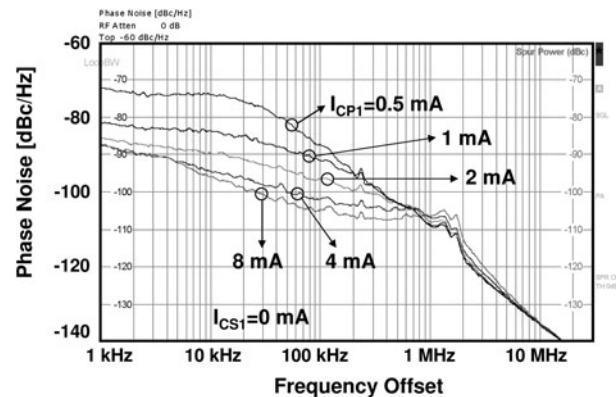


Fig. 2. Measured PLL phase noise at 10.5 GHz for different CP currents [18]. DC offset current at the CP output is disabled.

doubling f_{REF} reduces this type of phase noise by 9 dB. The input frequency is usually limited by the speed of the CMOS DSM to 100–200 MHz, depending on the technology node. Moreover, the availability of crystal oscillators may limit the reference frequency for low-cost applications. A CMOS frequency doubler or quadrupler may be useful here [19].

Figure 3 shows the simulated curvature β for a typical PLL as a function of the static phase error ϕ at the PFD input. This curve was obtained as follows: we performed an open-loop simulation for a cascade of PFD, CP and LPF driven by two CMOS signals with a time delay t_d between them. The CP output current $I(t)$ was averaged over one reference period T_{REF} to obtain the mean CP current I , which depends on the input delay t_d . A parametric simulation with respect to t_d was performed to calculate the function $I(t_d)$ with a high accuracy. Finally, we have numerically calculated the second derivative of $I(t_d)$ to obtain the curvature parameter β from (6) as a function of the PFD input phase error $\phi = 2\pi(t_d/T_{REF})$. As evident from Fig. 3, the linearity depends on the value of the bypass capacitor C_2 placed between CP output and chip ground. This shows that a codesign of CP and LPF is important for a good PLL phase noise performance. The optimum choice of the DC phase offset at the PD input results from a trade-off between PD linearity and CP device noise. For our example, the optimum phase offset is around 36° , corresponding to a CP duty cycle of $\alpha_{CP} = 10\%$. A detailed comparison of different CPs in a 130 nm SiGe BiCMOS technology was presented in [20]. It was shown that with a sufficient DC offset at the CP output only one type of transistors is switching in the steady state. This can be a pMOSFET, an nMOSFET or a SiGe-HBT. The basic idea to maximize the PD linearity is to use the fastest available transistor for steady-state switching. In a CMOS technology this would be an nMOSFET, and in a SiGe-BiCMOS technology it would be a SiGe-HBT. In either case, a DC UP current at the CP output to VDD is preferable over a DOWN current to ground to achieve this desired behavior.

A reduction of the rms phase error $\sigma_{\phi, in}$ at the PFD input by a factor of two reduces the folded quantization noise by 12 dB according to (8). Remember that this result requires a DC phase offset between the two PFD input signals.

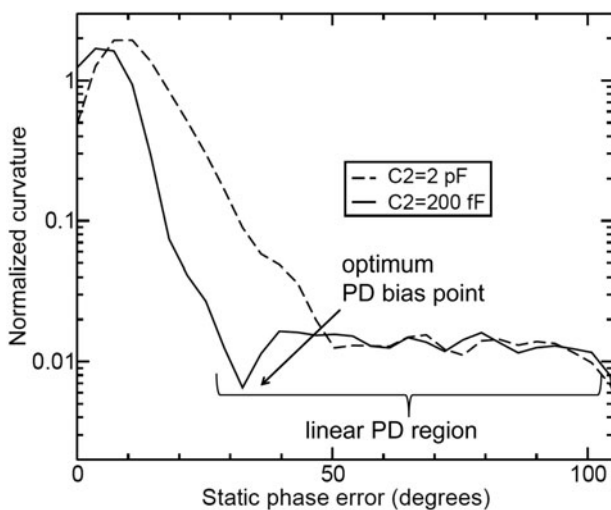


Fig. 3. Simulated PD nonlinearity parameter β according to (6) for two different values of the loop filter bypass capacitor C_2 .

Moreover, the curvature β should be relatively constant as obtained in Fig. 3 for large phase offsets to make the parabolic approximation (4) a reasonable assumption.

The minimization of $\sigma_{\phi, in}$ requires small phase excursions of the divided VCO signal. As shown in [9], single-loop DSMs have lower phase excursions than multi-stage noise shaping (MASH) DSMs, resulting in a lower in-band phase noise. Another method to minimize this type of phase noise is the maximization of the programmable divider speed. For a given total division ratio M/N , a high N implies a low M . Note that the elimination of one DTC in the prescaler reduces $\sigma_{\phi, in}$ by a factor of two. As a result, both phase noise and fractional spurs due to quantization noise folding are reduced by 12 dB [21].

C) Coupling spurs in fractional-N PLLs

The mutual inductances between bondwires may influence the spectral purity of the PLL output signal, both in a negative and in a positive way. Figure 4 shows two examples of a PLL layout. In Fig. 4(a) the VCO is located relatively close to the CP and the reference input buffer. The bondwires of VCO, CP, and REF-BUF are in parallel, resulting in large mutual inductances between them. By contrast, in Fig. 4(b) VCO and CP are better separated from each other. Moreover, the VCO bondwires are orthogonal to the other bondwires, which minimizes the mutual inductances between them. Note that the pads for supply and ground for each block are next to each other, which maximizes the mutual inductance between them. Since they are carrying the opposite current, the total bondwire inductance for each building block is minimized. To obtain an intuitive understanding, assume that the bondwires for supply and ground are merged into one wire. In this case, the net current in this wire is zero and no voltage modulations are induced on the chip.

In Fig. 4(b) several layout aspects for reducing the on-chip coupling are illustrated. They are based on a long experience in developing fractional-N PLLs for mobile base stations [4] and for space communication [10]. First of all, the VCO

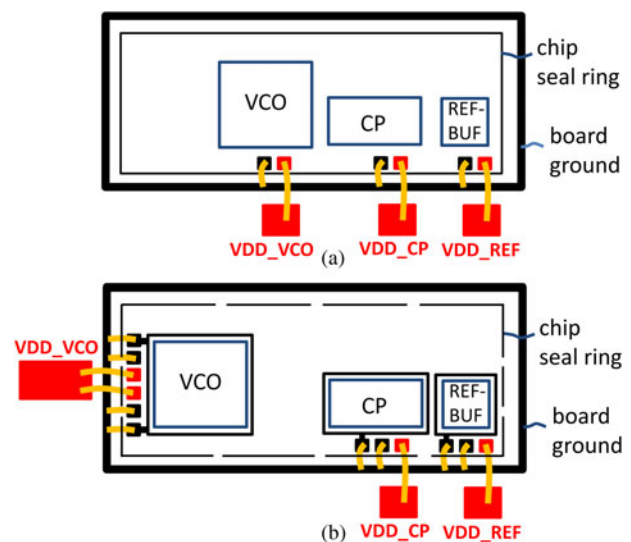


Fig. 4. Possible locations of PLL building blocks. (a) Example with strong noise coupling; (b) example with reduced noise coupling.

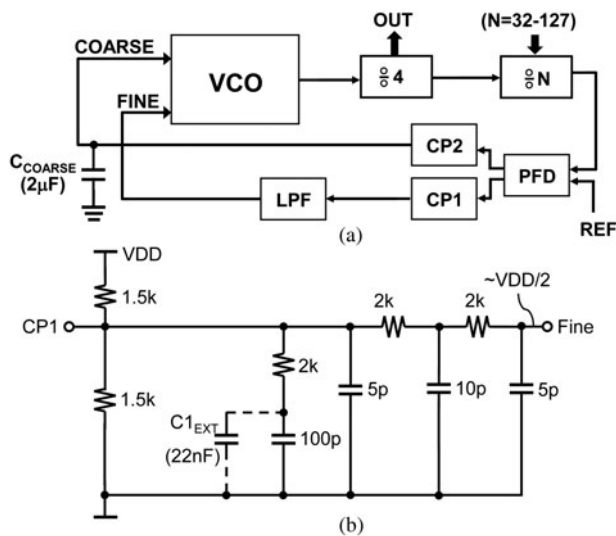


Fig. 5. Schematic of (a) programmable integer-N PLL using two parallel charge pumps for VCO control and (b) the LPF used in this PLL.

must have a separate supply and a separate ground on the chip. Moreover, on a low-doped silicon substrate as used for low-noise PLLs the spatial separation of the VCO from CP, reference input buffer and other digital circuitry reduces the coupling. Usually, a chip is surrounded by a seal ring, which is contacted to the substrate. If this seal ring is completely closed, the substrates of VCO and noisy building blocks are shorted, and the effect of spatial separation is partially compensated. To avoid such a ‘noise highway’, the seal ring should be broken as indicated in Fig. 4(b). Guard bands may be realized as p + doped substrate taps connected to ground. Their bondpads must not be on-chip connected to any active ground. The admittance from the noise aggressor (or victim) to the board ground through the guard band should be low. At high frequencies this implies a low bond inductance. Therefore, several bondwires for the VCO guard band may be helpful.

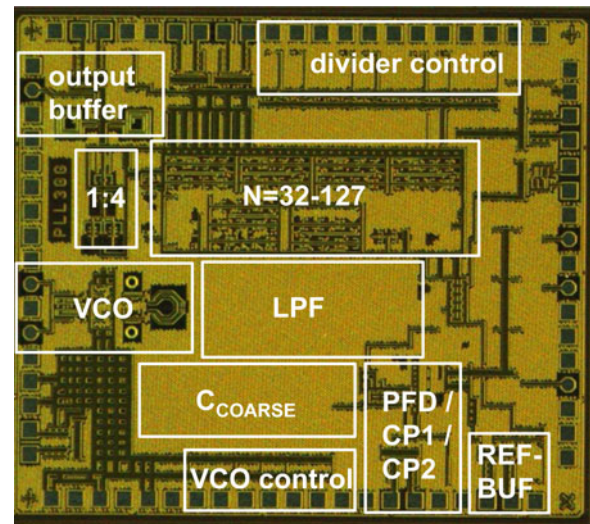


Fig. 6. Chip photograph of integer-N PLL.

Figure 5 shows the schematic of a 30 GHz integer-N PLL with 5 GHz tuning range designed in a 130 nm SiGe BiCMOS technology [22]. The PLL uses a slow coarse tuning loop and a fast fine tuning loop, see also [18]. Any noise on the fine tuning VCO input has a small effect on the VCO output frequency due to the small tuning gain. By contrast, the coarse tuning input is highly sensitive to any noise due to the high VCO gain, but it is loaded only with a metal-insulator-metal (MIM) capacitor to chip ground in parallel to an external 2 μF capacitor to board ground. The resistive voltage divider at the LPF input keeps the VCO fine tuning voltage, the corresponding VCO gain and the loop bandwidth fairly constant over the PLL tuning range. Figure 6 shows a photograph of the PLL. Due to the large distance between VCO and CMOS blocks (PFD, CP, reference buffer), the substrate noise produced in the CMOS circuitry is strongly attenuated before it reaches the VCO. The VCO is biased from left, whereas the other blocks are bias from bottom or top to

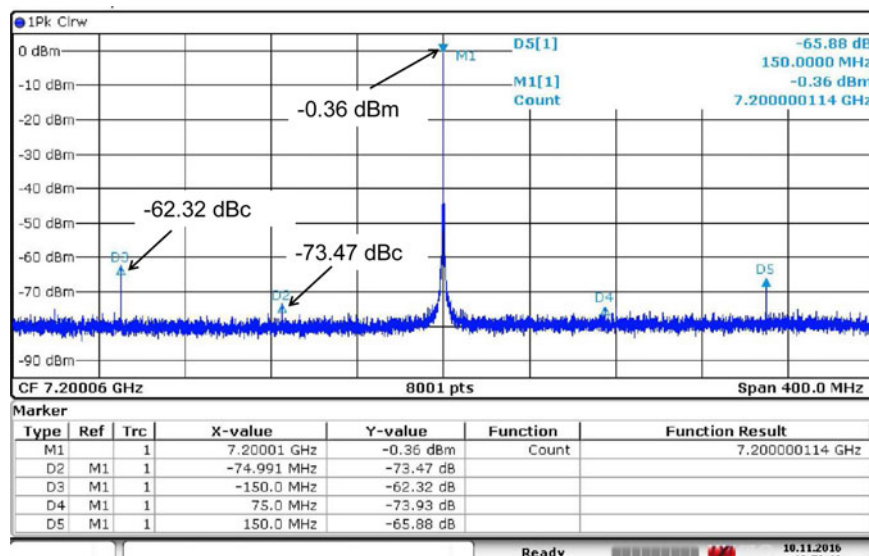


Fig. 7. Measured output spectrum of 28.8 GHz PLL at 1:4 prescaler output.

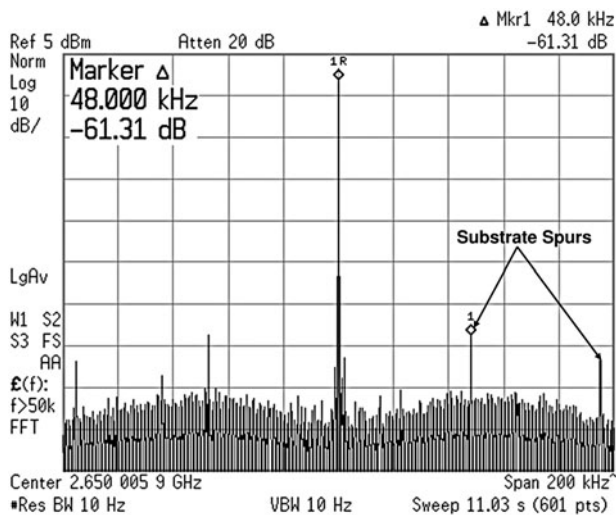


Fig. 8. Measured output spectrum of a 21.2 GHz fractional-N PLL at 1:8 divider output [4].

minimize the mutual inductances between the bondwires. Figure 7 shows the spectrum for an output frequency of 28.8 GHz measured at the 1:4 prescaler output, where the reference frequency is 75 MHz. The reference spurs at ± 75 MHz offset are below -73 dBc. At ± 150 MHz we observe spurs due to the substrate coupling from the input buffer to the VCO as discussed in Section 2.2.3. Their level is below -62 dBc.

Near-integer boundary spurs are observed in fractional-N PLLs. Their name is due to the fact that they occur if the total division ratio M/N is close to an integer number. In this case, the spurs are located at frequency offsets below the loop bandwidth, where they are hardly filtered by the PLL. Figure 8 shows the spectrum of a 21.2 GHz fractional-N PLL measured at the 1:8 divider output [4]. Here, the reference frequency was 80 MHz, and the division ratios were $M = 4$ and $N = 66.25015$. According to (2) in [4] we expect the largest modulation spurs at a frequency offset of $\pm(4 \times 0.25015 - 1) \times 80$ MHz = ± 48 kHz. This is exactly the measured position as evident from Fig. 8. The power level of this spur is as low as -61 dBc due to a careful layout. The measurement showed that the power of this spur is independent of the PD nonlinearity, but responds to changes in the VCO output power. This verifies that the coupling from the VCO output to the PD input is the cause for this spur.

IV. CONCLUSION

We have discussed various mechanisms affecting the spectral purity of phase-locked loops. Emphasis was placed on fractional-N PLLs, where the VCO frequency and the reference frequency are not harmonically related. The effect of quantization noise folding in the nonlinear PD was described and methods for minimizing this effect were proposed. They include a DC offset current at the CP output for linearizing the phase detector, the use of single-loop DSMs and the maximization of the programmable divider speed. It was outlined how the high-frequency VCO output signal can affect the

spectral purity of the PLL through substrate coupling and electromagnetic coupling between the bondwires. Remedies were presented to minimize these effects by a proper layout.

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he has been working on the design of silicon ICs for RF communications. His main research interests are design and optimization of high-performance frequency synthesizers for space applications and radar sensors.



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