SiGe BiCMOS Integrated Circuits for Optical Communication Transmitters

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der Technischen Universität Berlin
zur Erlangung des akademischen Grades

Doktor der Ingenieurwissenschaften
-Dr.-Ing.-

genehmigte Dissertation

Promotionsausschuss:

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Tag der wissenschaftlichen Aussprache: 11.04.2019

Berlin 2019

Zusammenfassung

Telekommunikation spielt in unserem alltäglichen Leben eine sehr wichtige Rolle und dies nicht nur wegen der Interaktion, sondern auch durch die rasante Entwicklung der Inter-Maschinen Kommunikation - dem so genannten Internet der Dinge (IdD). Diese immer schnellere Daten Kommunikation zwischen den Geräten erfordert auch einen Ausbau der Netzinfrastruktur. Deshalb gibt es den Trend zu komplexeren Modulationsformaten die eine höhere spektrale Effizienz besitzen was eine schnellere Datenübertragung ermöglicht. Der Fokus dieser Arbeit liegt an der Entwicklung von neuen Schaltungstopologien um die Effizienz von elektro-optischen Transmitter zu erhöhen. Dies wird mit Hilfe von fortgeschrittene Silizium-Germanium BiCMOS Technologie ermöglicht.

Der erste Teil dieser Arbeit beschreibt die Möglichkeiten sowie die Eigenschaften der Silizium-Photonik Plattform für die Integration des Treibers und Mach-Zehnder Modulators (MZM). Diese Plattform ermöglicht die Entwicklung eines voll-integriert elektro-optischen Transmitter basierend auf segmentierter Topologie. Diese segmentierte Topologie ermöglicht eine sehr effektive Verteilung der Treiberspannung über die gesamte Länge des Modulators. Durch die Anpassung der Geschwindigkeit von optischen und elektrischen Signalwellen wurde die Limitierung der Bandbreite kompensiert. Mit diesem Ansatz wurde die Datenübertragung über 60 km Glasfaser bei 112 Gb/s Datenrate demonstriert.

In zweiten Teil der Arbeit lag der Fokus auf verschiedenen MZM Treiber Varianten, die unterschiedliche Schaltungstechniken für die integrierten Schaltungen (IC) untersuchten. Als erstes wurde eine 25 Ω Impedanz 40 Gb/s MZM Treiber Topologie präsentiert, welches die zusätzliche Verlustleistung des 25 Ω MZM kompensierte. Als zweites wurde ein Treiber Design in einer komplementären BiCMOS Technologie implementiert, mit der eine Datenrate von 28 Gb/s dabei wurde eine Effizienz von 6.4% erreicht. Dies ist der beste Wert, der zu der Zeit publizierten wurde. Zum Schluss wurde eine Implementierung von einer 100 Gb/s MZM Treiber Variante, mit einem 2-bit RF Digital-Analog (DA) Wandler gezeigt, durch die kein externer DA Wandler mehr benötigt wurde und dadurch konnte auch eine niedrigere Gesamtverlustleistung ermöglicht werden.

Der letzte Teil meiner Arbeit beschäftigt sich, mit Lösungen die Datenraten über 100 Gb/s ermöglichen. Dabei wurden unterschiedliche Treiber Varianten analysiert, die mit verteilten Verstärkern eine Bandbreite von mehr als 90 GHz erreichten. Um die unterschiedlichen Varianten des elektro-optischen Module leichter im Labor zu charakterisieren. Wurde das Design eines Pseudo-Random Bit Sequenz (PRBS) Generators präsentiert. Diese PRBS Generator Implementierung unterstützt ein PRBS7 Format und eine Datenrate von 115 Gb/s. Dabei konnte ein Bewertungsfaktor (Figure-of-Merit) von 0.87 pJ/b erreicht werden – was dem neuesten Stand der Technik entspricht.

Abstract

Telecommunications play a crucial role in our daily lives, not only because of their significance in allowing interaction between all of us, but also due to the forthcoming expansion of connection and exchange of data between machines, the so-called Internet of Things (IoT), which will result in a massive network of thousands of millions of devices around the world. Such growth of the internet calls for simultaneous development of the underlying network, as it needs to support faster speeds in current devices. Consequently, metro areas tend to experience much of this throughput concentration, demanding electro-optical transceivers with types of modulation featuring higher spectral efficiency. This thesis focuses on the development of new designs to improve the performance of electro-optical transmitters by making use of advanced manufacturing processes in SiGe BiCMOS technology.

In the first part, the capability of a silicon photonics platform for the implementation of driver and Mach-Zehnder modulator (MZM) is investigated. With the aim to implement a high-speed solution using this platform, a segmented topology is used for the investigation. With this scheme the driving voltage can be effectively applied along the whole modulator length and velocity matching between optical and electrical waves can be achieved, overcoming the bandwidth impairments. With the implemented module, transmission over 60 km of fiber at up to 112 Gb/s data rate is demonstrated.

In the second part of the thesis, stand-alone MZM driver implementations are presented which serve to explore different techniques in the electrical design of this integrated circuit (IC). First, the design of a 40-Gb/s driver compatible with a modulator with a custom impedance of 25 Ω is presented, which investigates a topology to overcome the additional power dissipation due to the lower load impedance. Secondly, a low-power solution driver implemented in a complementary BiCMOS technology is demonstrated, achieving 28 Gb/s and an efficiency of 6.4%, the highest in the literature. Finally, the implementation of a 100-Gb/s driver is investigated which includes a 2-bit RF digital-to-analog converter (DAC), eliminating the need for external DAC and therefore reducing power dissipation and footprint.

The last part of the thesis deals with solutions targeting data rates higher than 100 Gb/s. A high-speed driver using a distributed amplifier topology in a differential manner is presented, achieving a record bandwidth of 90 GHz. Test equipment must also be able to cope with the increasing data rates in optical transmissions; in this context a pseudo-random bit sequence (PRBS) generator to ease measurements of the electro-optical devices is also designed, with eye-diagram measurements showing a PRBS7 of 115 Gb/s and demonstrating a state-of-the-art figure-of-merit (FoM) value of 0.87 pJ/b.

"People are mistaken when they think that technology just automatically improves.
It does not automatically improve.
It only improves if a lot of people work very hard to make it better,
and actually it will, I think, by itself degrade, actually."

Elon Musk at TED, Vancouver, Canada, 28th April 2017

Acknowledgements

The making of this work would not be possible without the collaboration and support of many people. First, I would like to thank my advisor Prof. Dr.-Ing. habil. Dietmar Kissinger for providing me this research opportunity, general guidance and working environment.

I would also like to thank my two group leaders, Dr. Daniel Micusik and Prof. Dr.-Ing. Ahmet Cagri Ulusoy. With the support from Daniel, I was able to learn so much about circuit design and BiCMOS technology. Without his initial guidance, persistence and attention to detail to maximize performance, the work here developed wouldn't have the same quality. The contribution of Cagri was equally important, to give a direction to the work and publications advice. Moreover, I would like to thank Dr.-Ing. Ahmed Awny and Dr. Minsu Ko for the guidance of our team towards the end of my work in IHP.

A so important acknowledge to (also from now on Dr.-Ing.) Iria García López for working so closely with me in all the designs we develop in IHP. I believe without this common support and without the environment we created from the beginning to learn and share so much, I couldn't get to this point. I'm really proud of our collaboration. I'm very grateful as well to have you, Dr.-Ing. Subhajit Guha, Carlos Benito Sánchez and Rahul Yadav sharing this time together with me. This was a very important period of my life and you contributed to my evolution as a person.

I would like to thank all the colleagues from the Circuit Design department which also contributed to the enrichment of my technical knowledge. Also essential to the development of the electro-optical chips of this work, the collaboration with the photonics group of the Technology department (led by Prof. Dr.-Ing. Lars Zimmermann) and project partners.

A special message to my friends back to Portugal, the moments we spent together and relationships we still maintain with physical distance. Important connections that continue to contribute so positively to my life.

To my girlfriend Rita Ferreira, I thank you so much for your presence in my life, your love, support, help, power, care, and your influence on my day-to-day life. With you, I could accomplish my career goals with more easiness and motivation. As always, we are on this together, this accomplishment is another victory for both of us.

Finally, to my family, my tremendous gratitude for the education and attention you have given me, essential foundations for my dreams and goals so far realized.

Thank you! Dankeschön! Obrigado!

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Acronyms

AWG arbitrary waveform generator

BER bit error rate
BJT bipolar junction transistor
BPG bit pattern generator

CD chromatic dispersion
CM common-mode
CML current-mode logic
CMRR common-mode rejection ratio
CW continuous wave

DAC digital-to-analog converter
DCF dispersion compensating fiber
DSP digital signal processor
DWDM dense wavelength division multiplexing

EAM electroabsorption modulator
ECL emitter-coupled logic
EDFA erbium-doped fiber amplifier
EF emitter-follower
EM electromagnetic
EPIC electronic-photonic integrated circuit
ER extinction ratio

FFE feed-forward equalization
FoM figure-of-merit

HBT heterojunction bipolar transistor

IC integrated circuit
IEEE Institute of Electrical and Electronics Engineers
ISI intersymbol interference

LCA lightwave component analyzer
LDO low-dropout

MIM metal-insulator-metal
MMI Multimode interference
MQW multiple quantum well
MZM Mach-Zehnder modulator

NF noise figure
NRZ non-return-to-zero

OIF Optical Internetworking Forum
OOK on-off keying
OpAmp operational amplifier
OSNR optical signal-to-noise ratio

PAM pulse amplitude modulation
PDM polarization-division-multiplexing
PIC photonic integrated circuit
PRBS pseudo-random bit sequence

QAM quadrature amplitude modulation
QPSK quadrature phase shift keying

SE-MZM segmented Mach-Zehnder modulator
SFDR spurious-free dynamic range
SNR signal-to-noise ratio
SSMF standard single mode fiber

TDCM tunable dispersion compensating module
THD total harmonic distortion
TIA transimpedance amplifier
TWE-MZM travelling-wave electrode Mach-Zehnder modulator

VNA Vector Network Analyzer
VOA variable optical attenuator

WDM wavelength division multiplexing

1 Introduction

1.1 Scope and Motivation

Over the recent years, the network traffic on a global scale has grown rapidly, together with a constant evolution of new sophisticated services and more connected devices. Not only the internet is connecting more and more people, but also the communication between machines is becoming much more relevant. This evolution results in the interconnection of thousands of millions of devices around the world. This massive growth of the internet imposes a constant evolution of the telecommunications industry as the throughput continues to increase, hence challenging the limits of the capacity of the global network. Consequently, metro areas tend to experience much of this concentration, demanding systems with types of modulation featuring higher spectral efficiency. Fig. 1.1 represents a prediction of the data-rate growth until 2020, where optical modules will be required to have a throughput up to 1 Tbps. This exponential growth is mainly attributed to the increased access to video streaming and cloud computing.

During the recent years, organizations as the Institute of Electrical and Electronics Engineers (IEEE) and the Optical Internetworking Forum (OIF) have been working in defining the next generation standards for optical communications for data centers and core networks, 200G and 400G networks. For data center applications, recently IEEE approved the IEEE 802.3bs standard, allowing commercial deployment. The standard defines different specifications in the wavelength range of 1300 nm (O-band), with for example distances ranging from 100 m to 10 km, modulation format of non-return-to-zero (NRZ) and pulse amplitude modulation (PAM) with four symbols (PAM-4), all with a constant symbol rate per lane of 26.5625 GBd [1]. For core networks, OIF shares technology options for short haul, metro and long-haul communications. Here the modulation format can vary from quadrature phase shift keying (QPSK) to quadrature amplitude modulation (QAM) with 64 symbols (QAM-64) and the maximum reach from 10 km to more than 2000 km. The symbol rate is higher than in data center applications, since the recommendation is to achieve up to 64 Gbaud [2]. Polarization-division-multiplexing (PDM) is used to allow transmission in up to 8 lanes in the wavelength band of 1550 nm (C-band).

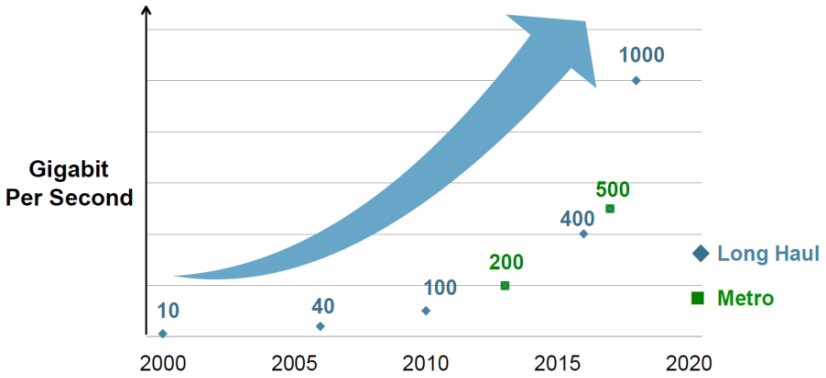


Figure 1.1: Global data throughput growth [5].

The new standards enforce new developments in the core components of the optical transceivers regarding power consumption, bandwidth and linearity [3]. Miniaturization is another requirement as with the increase of the baseband speeds, short-distance interconnections between the components are of great relevance. Regarding the latter, developments in the technology have been done in two main directions: the integration of photonics components (photonic integrated circuits (PICs)) in silicon technologies and the combination of different technologies (III-V with SiGe for example) in hybrid approaches utilizing for instance wafer bonding [4].

In order to make the electro-optical subsystem practical, integration and co-packaging of driver and modulator is an important issue. Moreover, with the increasing number of transceivers, lowering the cost of optical communications is another matter of importance, in particular for data centers. For these reasons, electro-optical solutions based on silicon photonics technology platforms are a promising candidate. Silicon photonics have the additional advantage of being thermally insensitive [6].

In this thesis, integrated circuits (ICs) for optical transmitters are investigated, described and tested. The two approaches of integration are considered, monolithic and hybrid. In the case of monolithic integration, the electronic-photonic integrated circuit (EPIC) platform of IHP is used to implement and demonstrate the complete eletro-optical transmitter. When a hybrid integration is proposed, drivers for general purpose optical modulators are designed, focusing the work mainly in the electric part. The motivation is to present different approaches and techniques for future development of optical transmitters that can comply with the new standards, hence fitting in the upcoming demand of network throughput growth.

1.2 Optical Transmitters

Two distinct ways to generate modulated optical signals are presented in Fig. 1.2. In the first method, known as direct modulation, the electrical signal carrying the data information turns on and off the laser, modulating its current. In the second method, the laser is always turned on, producing a continuous wave (CW) optical signal. In this configuration, a separated modulator is added, and depending on the type of modulator, the electrical signal modulates the optical signal in amplitude or phase. This method is known as external modulation. The two methods are usually used in different applications. Whereas the direct modulation

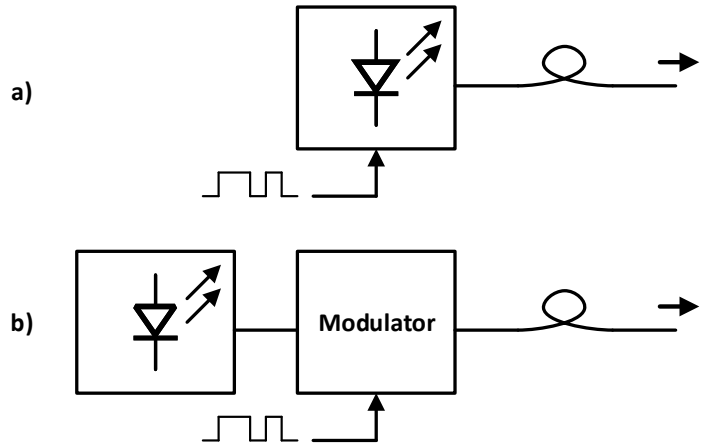


Figure 1.2: Types of optical transmitters. a) Direct modulation b) External modulation.

configuration is simple, compact and efficient, fitting the requirements of, for instance, data centers, the external modulation format can produce higher quality optical signals, reaching higher data-rates and higher orders of modulation formats. In external modulation, the modulated signal features narrower spectral linewidth and higher extinction ratio, however, this comes at the expense of a more complex and costly system mainly used in metro and long-haul networks. The main focus of this thesis is on the external modulation method.

1.2.1 Optical Modulators

There are two types of optical modulators which are commonly used in optical transmitters:

Electroabsorption modulator (EAM): The EAM comprises an active semiconductor region inserted between a p-doped and n-doped layer, creating a p-n junction. The EAM operates on the principle called *Franz-Keldysh* effect, where the effective bandgap of a semiconductor decreases with the rise of the electric field. With no bias voltage applied to the p-n junction, the bandgap of the active region is simply too wide to be transparent at the wavelength of the light from the source. Contrary, applying large enough reverse bias across the junction, the effective bandgap is reduced and the absorption effect starts, thus becoming opaque. In practical EAMs, the active region normally is structured as a multiple quantum well (MQW), resulting in a stronger field-dependent absorption effect. The relationship between the optical output power, P_{out}, and the applied reverse voltage, V_M, is described by a switching curve. The operation voltage for switching the modulator from the on state to the off state is the switching voltage V_{SW}. Typically, V_{SW} is in the range of 1.5 to 4 V, and the dynamic extinction ratio (ER) typically is in the range of 11 to 13 dB [7].

Mach-Zehnder modulator (MZM): The MZM enables the optical transmitter to modulate in phase and intensity as response to the applied voltage signal. The electrical field of the incoming optical carrier can be modulated in phase in each phase shifter arm, as the refractive index of the material varies with the applied voltage, and thus

the refractive index of the waveguide. Assuming the change of the refracted index is linear to the applied external voltage $u(t)$, a driving voltage necessary to obtain a phase shift of π in the optical signal, is denoted by V_π. The expression that lists the incoming optical carrier, $E_{in}(t)$, and the outgoing phase modulated optical field, $E_{out}(t)$, is given by [8, 9]:

$$E_{out}(t) = E_{in}(t)e^{j\frac{u(t)}{V_\pi}\pi} \tag{1.1}$$

The relative phase shift results in interference that can vary between constructive and destructive. This type of modulator is described in more detail in section 2.3.

1.2.2 Limits in Optical Transmitters

A set of limits which affect the optical communications systems is briefly presented. Although the main focus of this thesis is not in the overall performance of the optical link, it is still essential to understand from where the weaknesses of the transmission are coming, in order to define specific characteristics for the transmitters. Three main limitations are fiber attenuation, chromatic dispersion and polarization-mode dispersion.

Fiber attenuation: The fiber attenuation is characterized by α, which is the attenuation measured in dB/km. To find the attenuation limit, the following expression is used, given a transmitted power P_T and the power intensity at the receiver P_R, both in dBm, to calculate the maximum distance in km [7]:

$$L \leq \frac{P_R - P_T}{\alpha} \tag{1.2}$$

Chromatic dispersion: The chromatic dispersion originates from having different wavelengths (or colors) traveling at different velocities through the fiber. Assuming a transmitter which comprises a dual-drive MZM, the maximum distance of fiber limited by the chromatic dispersion can be approximated to the following equation [7]:

$$L \leq \frac{c}{2|D|\,\lambda^2\,B^2} \tag{1.3}$$

where c is the speed of light in vacuum, D the dispersion parameter of the fiber, λ is the wavelength and B is the transmitted bit rate.

Polarization-mode dispersion: Polarization-mode dispersion happens due to different polarization modes traveling at different speeds. The maximum distance for the transmission due to the limitation caused by the polarization-mode dispersion is given by [7]:

$$L \leq \frac{(0.1)^2}{D_{PMD}^2\,B^2} \tag{1.4}$$

with D_{PMD}^2 defined as the polarization-mode dispersion parameter.

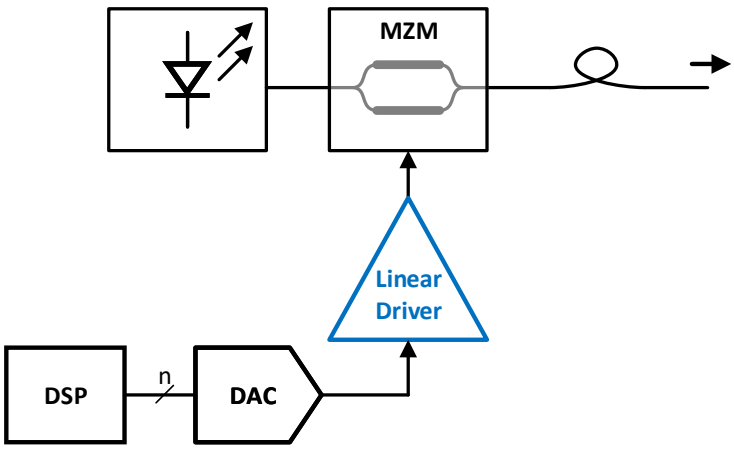


Figure 1.3: An electrical driver in an optical transmitter.

These different factors will determine the maximum transmission distance that can be achieved in an optical communication system. For different applications, a set of specifications is also defined to guarantee a minimum bit error rate (BER) in the receiver end point. Essential specifications in a optical transmitter are bandwidth, output power, modulation format, ER and optical signal-to-noise ratio (OSNR). For the calculation of the achievable output power, the selection of the laser maximum power is critical, plus the attenuation in the modulator due to static and modulation-induced optical losses and the selection of optical amplifiers.

1.3 Electrical Driver for Mach-Zehnder Modulators

A simplified scheme of an electro-optical transmitter is depicted in Fig. 1.3. The digital signals produced by the digital signal processor (DSP) are transferred through a digital bus to the DAC where the signal is transformed into an analog waveform. The voltage amplitude of this signal is amplified and delivered to the MZM by the driver. Large input voltage (defined as V_π) is required for this type of modulators, ranging from 2 V to more than 10 V, depending upon MZM design and length [10, 11]. The driver is not only required to provide the amplification necessary to drive such high voltage amplitudes, but also has to match the modulator input impedance. The equivalent load of the modulator seen by the driver output might be resistive or capacitive, depending on the MZM driving approach, analyzed in subsection 2.3.1. For simple modulation formats as NRZ or QPSK, as the data signal is in an on-off keying (OOK) format, the DAC is not required and the driver is implemented as a limiting amplifier. For the application shown in the block diagram, the driver integrates linear amplifiers, and linearity is an important specification in the design of the circuit. Thus, this case is applied to the transmissions with high-order modulation formats.

The power dissipation of a modulator driver is quite large when compared with other transceiver blocks. The driver must deliver large voltage swings into a load resistance that typically is around 25 to 50 Ω. Moreover, for capacitive modulator driving approaches, the high switching speed necessary for Gb/s drivers also requires substantial currents to charge and discharge the load capacitance. A low power dissipation is desirable because it reduces the

heat generation in the driver IC and in the system. Excessive heating may require an expensive package, and excessive heating in the system may degrade the transmitter performance or require a large power-consuming thermoelectric cooler to remove the heat. Furthermore, a low power dissipation also reduces the cost of the power supply.

The main focus of this thesis is to implement driver designs for different modulator driving approaches and for different transmitter specifications. Each design tries to adopt the best topology to comply with the described targets, in terms of bandwidth, data-rate, input and output matching, linearity and power dissipation. Finally, all designs are characterized and compared to state-of-the-art implementations.

1.4 Thesis Outline

In addition to this introductory chapter, this thesis is organized in more five chapters:

Chapter 2 - Broadband Circuit and Optical Modulator Fundamentals starts with an essential investigation to the output stage of broadband circuits implemented in HBTs technologies, where the specification of linearity of the driver is analyzed. Thereafter, the MZM is described in different driving techniques and an electro-optical co-simulation platform is shown.

Chapter 3 - Monolithically Integrated Modulator Drivers presents two variants of the monolithic electro-optical transmitted developed in the EPIC SiGe:C BiCMOS platform of IHP. The design is described, the techniques used in the electrical design are detailed and the results are shown and compared to state-of-the-art implementations.

Chapter 4 - Travelling-Wave Electrode Modulator Drivers depicts three drivers implemented for generic 25-Ω and 50-Ω travelling-wave electrode Mach-Zehnder modulators (TWE-MZMs) with the aim to explore different approaches to achieve high-speed transmissions and low power dissipation of the electrical ICs. For the different implementations, the designs are described and the results are presented and compared to other published work.

Chapter 5 - Above 100 Gb/s Optical Transmitter Circuits describes two different devices: a high-bandwidth driver and a state-of-the-art PRBS generator to enable testing of optical transmitters with bit rate of more than 100 Gb/s. For the two designs, the topologies are described and the results are presented and compared to other works.

Chapter 6 - Summary and Outlook summarizes the content of the thesis and concludes the work developed for electro-optical transmitters.

2

Broadband Circuit and Optical Modulator Fundamentals

This chapter begins with a summary of the electronics technology platform used in this work and reviews the small-signal model of the heterojunction bipolar transistor (HBT) transistor. After that, a linearity analysis of the differential pair amplifier is performed. Furthermore, different optical transmission driving approaches are presented and discussed to understand the advantages and limitations of each one. Finally, a co-simulation integrating electronics and photonics in a platform is described.

2.1 Technology and Small-Signal Modelling

2.1.1 Heterojunction Bipolar Transistors

An HBT is a transistor with a pn heterojunction, a junction made of two different materials, whereas a bipolar junction transistor (BJT) is a homojunction bipolar transistor. In a homojunction bipolar transistor, the emitter doping is chosen to be much greater than the base doping. However, one limitation of the f_T in bipolar devices is the time required for minority carriers to cross the base. One way to increase f_T is reducing the base width, but it will lead to the increase of the base resistance. In the same way, the base resistance will limit speed, due to the pole formed with the capacitance at the base node [12]. To overcome this tradeoff, germanium is added to the base of the bipolar transistor, forming an HBT. The two different materials, Si and Ge, on the two sides of the pn junction have different band gaps, with the band gap of Si being greater than the Ge one. Forming a SiGe compound in the base reduces the band gap there [12]. Therefore, the emitter doping can be decreased and the base doping can be increased in an HBT in comparison to a BJT. With higher doping at the base, the base resistance remains constant when the base width is reduced to increase f_T. Moreover, this change reduces the width of the base-collector depletion region in the base with the transistor operating in the forward active region which will increase the Early voltage V_A [12]. HBTs characteristics are described by the same equations as those employed for Si

BJTs. Another point of the HBTs is the possibility to be included as the bipolar transistors in BiCMOS processes.

The HBT is an ideal candidate to be used in the broadband amplifier. It offers high breakdown voltages and high f_T values (up to 300 GHz in IHP technologies). The performance of the HBT varies depending on the technology variant used. In this thesis, several technology variants are utilized, as the choice is adjusted to the particular requirements of the planned solution: desired speed, monolithic integration of photonic devices, and specific devices from the available technology modules, for instance, pnp HBTs.

2.1.2 SiGe:C BiCMOS Technology

In this thesis, the electronics are implemented in SiGe:C BiCMOS technologies of IHP. BiCMOS technologies offer suitable characteristics for broadband applications, required for the development of optical communications. The most important device offered is the HBT transistor. IHP process provides high-frequency HBTs devices without deep trenches and with low-resistance collectors formed by a high-dose implant after shallow trench formation [13]. This approach permits the development of top bipolar performance with minimum cost on the process and minimizes the impact of the HBT thermal processing on the CMOS devices [13]. The MOS transistors made available in the BiCMOS technologies are mostly used in this work for the implementation of dc or low-frequency circuitries required to support the RF core of the design. For instance, both NMOS and PMOS are utilized to implement operational amplifiers (OpAmps), low-dropout (LDO) voltage regulators and current-mirrors, and additionally, they are part of the bandgap circuitry too.

2.1.3 HBT Small-Signal Model

Fig. 2.1 presents the equivalent small-signal models of the HBT. The hybrid-π model is shown in Fig. 2.1b). This model represents the HBT as a voltage-controlled current source and explicitly includes the input resistance looking into the base, r_π. Defining β as the transistor current gain, g_m and r_π are given by:

$$g_m = \frac{I_C}{V_T} \tag{2.1}$$

$$r_\pi = \frac{\beta}{g_m} \tag{2.2}$$

with I_C defined as the transistor collector current and V_T the thermal voltage, approximately 25 mV at 25 °C.

Although the hybrid-π model can be used to analyze most of the small-signal conditions of the circuit, there are situations in which an alternative model, shown in Fig. 2.1c), is much more convenient. This model is called the T model and represents the HBT as a current-controlled current source. This model explicitly shows the emitter resistance r_e rather than the base resistance r_π featured in the previous model:

$$r_e = \frac{V_T}{I_E} \tag{2.3}$$

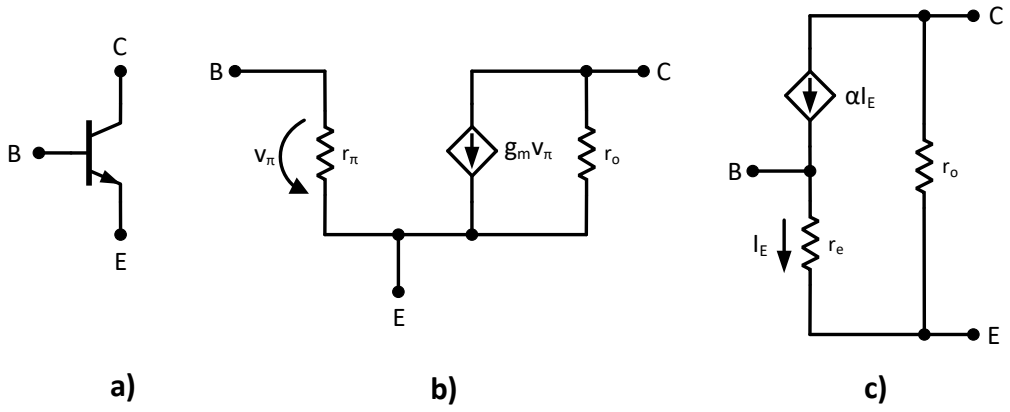


Figure 2.1: Small signal model of the HBT. a) HBT symbol with 3 terminals b) the hybrid-π model and c) the T model

with I_E defined as the transistor emitter current.

The currents in the transistor are related by the following equations:

$$I_E = I_C + I_B \tag{2.4}$$

$$I_C = \beta I_B = \alpha I_E \tag{2.5}$$

with I_B defined as the transistor base current and $\alpha = \beta/(\beta + 1)$.

The T model is the preferred model used in the analysis of the HBT amplifiers which will be presented in the following.

2.1.4 Common-Emitter Amplifier with Emitter Resistance

Throughout this thesis, most of the drivers which were designed for optical modulators follow a linear amplifier topology. In all the output stages of the linear amplifiers, the amplifier configuration chosen is the common-emitter amplifier with emitter resistance, also called common-emitter amplifier with emitter degeneration. In contrast to a regular common-emitter amplifier, including a resistance in the emitter leads to significant changes in the amplifier characteristics. To simplify the analysis, a single-ended is used in the representation. The schematic of this amplifier is shown in Fig. 2.2a). When the HBT is replaced by the T model presented previously, the equivalent circuit can be represented as shown in Fig. 2.2b).

The voltage gain of this circuit can be expressed as [14]:

$$\frac{V_{out}}{V_{in}} = -\alpha \frac{R_c}{r_e + R_e} = -\frac{g_m R_c}{1 + R_e/r_e} \tag{2.6}$$

Alternatively the voltage gain of the common-emitter amplifier with emitter resistance can be approximated to:

$$\frac{V_{out}}{V_{in}} \approx -\frac{g_m R_c}{1 + g_m R_e} \tag{2.7}$$

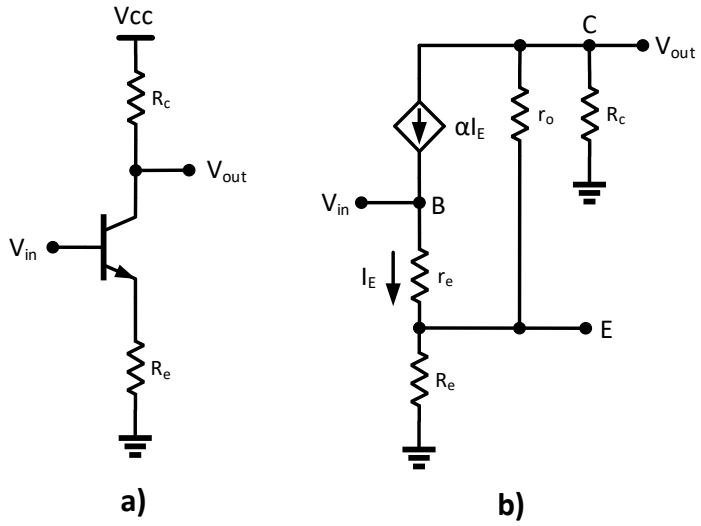


Figure 2.2: a) Schematic of a single-ended common-emitter amplifier with emitter resistance. b) HBT replaced by the T model in the amplifier schematic.

In conclusion, including an emitter resistor in the common-emitter amplifier results in the following characteristics [14]:

- The input resistance of the amplifier is increased by a factor of $1 + g_m R_e$.
- The voltage gain of the amplifier is controlled by R_c and R_e, as the gain is reduced approximately by the factor $1 + g_m R_e$ in comparison to a conventional common-emitter amplifier. The gain curve is more linear and less dependent on the value of β.
- The emitter resistance degenerates the input signal, allowing the input amplitude to increase by the factor $1 + g_m R_e$.
- Not considering the effect of the load resistance R_c, the output resistance is increased, multiplying r_o by the factor $1 + g_m R_e$.

2.2 Distortion Analysis

2.2.1 Total Harmonic Distortion

Total harmonic distortion (THD) is a common index for representing the linearity characteristics of analog circuits [15]. The THD calculation tells how much of the distortion of a voltage is due to harmonics in the signal. THD is an important aspect in broadband circuits for optical communications and it should typically be as low as possible. The definition of THD is as follows. Applying an input signal $V_{in}(t)$ to an amplifier:

$$V_{in}(t) = a_0 + a_1 \, cos(\omega t) \tag{2.8}$$

And obtaining the output $V_{out}(t)$ in the following form [15]:

$$V_{out}(t) = b_0 + b_1\, cos(\omega t) + b_2\, cos(2\omega t) + b_3\, cos(3\omega t) + b_4\, cos(4\omega t) + ... \tag{2.9}$$

where ω is the fundamental angular frequency of the desired signal. The THD, in dB, is then defined as [15]:

$$\text{THD} = 10\, log \frac{b_1^2}{b_2^2 + b_3^2 + b_4^2 + ...} \tag{2.10}$$

In optical communications the specification of THD is usually given in percentage and it is calculated as:

$$\text{THD} = \frac{\sqrt{b_2^2 + b_3^2 + b_4^2 + ...}}{b_1^2} \times 100 \tag{2.11}$$

Thus, by definition, the THD of a signal is the ratio between the sum of all the spurious components and the fundamental harmonic. The spurious components appear as result of the non-linearities of the amplifier.

2.2.2 Differential Pair Amplifier with Emitter Degeneration

A driver for an optical transmitter is an amplifier which operates mainly with large signals. This is due to the fact that typically, from the first stage, the input signal is already greater than $10 \times V_T$. With such range of amplitudes, the amplifier has to be properly designed to support linear characteristics. As referred previously, a preferred candidate for an amplifier with linear response is the common-emitter amplifier with emitter resistance. The schematic of this amplifier is depicted in Fig. 2.3. The gain response of this amplifier is correspondent to the single-ended counterpart analyzed previously in the subsection 2.1.4.

The emitter-degeneration resistors included in series with the emitters of the transistors increase the range of V_{in} over which the differential pair behaves approximately as a linear amplifier. The effect of the resistors may be understood intuitively from the examples plotted in Fig. 2.4. For large values of emitter-degeneration resistors, the linear range of operation is extended by an amount approximately equal to $R_e I_{\text{tail}}$. This result stems from the observation that all of I_{tail} flows in one of the degeneration resistors when one transistor turns off. Therefore, the voltage drop is $R_e I_{\text{tail}}$ on one resistor and zero on the other, and the value of V_{in} required to turn one transistor off is changed by the difference of the voltage drops on these resistors [12].

2.2.3 Biasing Techniques

Typically in optical communications, the required low cutoff frequency is in the order of tens of kHz, bounding the options for the design of the amplifiers. The broadband response has to start down from dc, requiring the usage of resistive matching, in contrast to RF matching techniques which can be used for specific frequency bands. Furthermore, linear drivers cannot use topologies based on limiting amplifiers, which could be used for OOK applications. Therefore, linear drivers for optical communications are power hungry and any

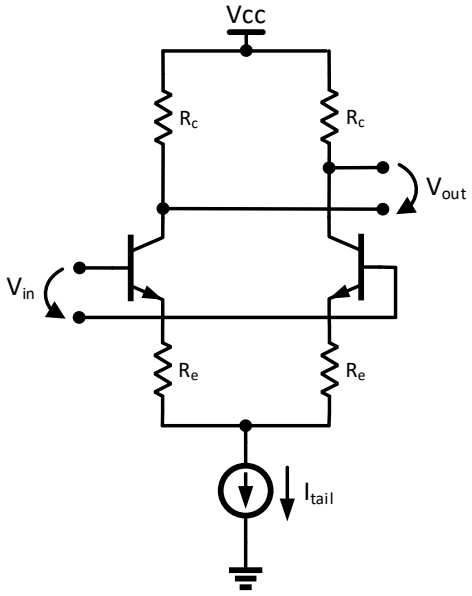


Figure 2.3: Schematic of a differential pair amplifier with emitter degeneration.

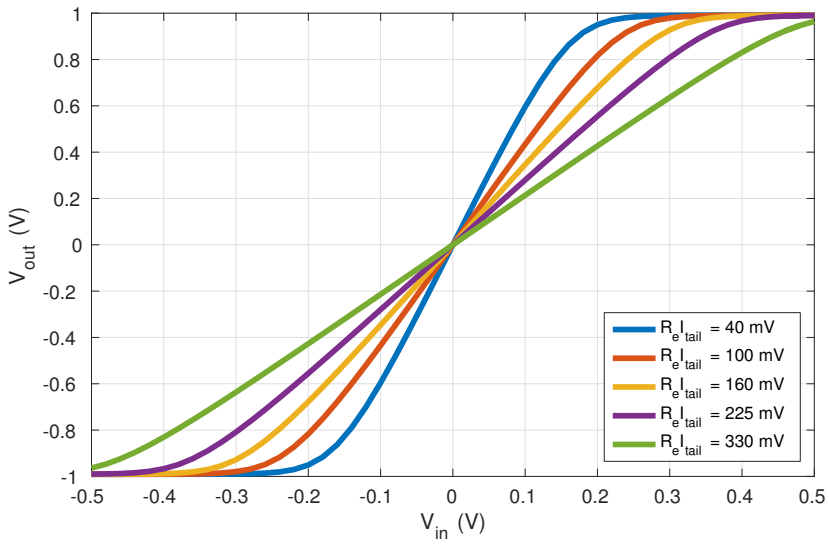


Figure 2.4: Output amplitude versus input amplitude for different values of emitter resistance.

saving in power dissipation improves significantly the overall power budget of the optical transceiver.

Two implementation options for the current source represented in Fig. 2.3 are presented in Fig. 2.5. The first option shown in Fig. 2.5a) is the most common implementation, a current mirror. It provides the biasing of the HBTs of the stage by current and leaves some margin for the dc voltage of the HBTs base. Most importantly the current mirror will provide high impedance at the common node (V_1), resulting in high common-mode rejection ratio (CMRR), especially if the current mirror incorporates emitter degeneration as well. However, in some cases with multi-stage topologies, the CMRR specification at the output stage may be relaxed, and the current mirror might be replaced by a simple resistor as current source. In this case, the headroom required for the current source, V_1, is reduced (typically is kept at around

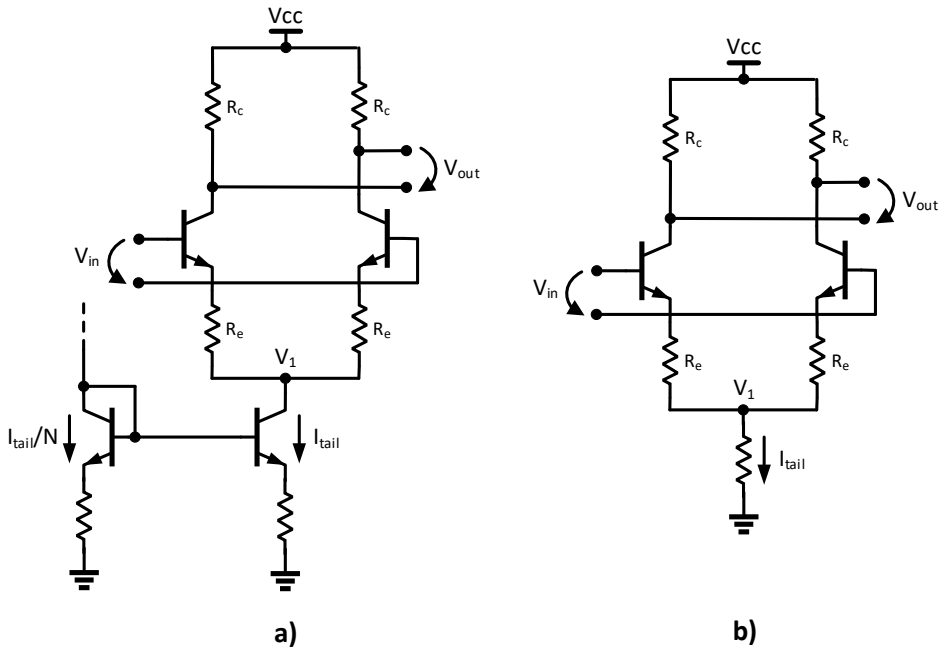


Figure 2.5: a) Differential pair amplifier with current mirror and b) with resistive current source.

$10 \times V_T$). However, the biasing of the stage is now controlled by the base voltage of the HBTs, the common-mode voltage of V_{in}. In order to set the biasing current of the differential pair properly, an LDO is required in one of the previous stages. The LDO implementation is analyzed in more detail in the next chapters where the designs of the drivers are presented.

Furthermore, the voltage headroom required in the collector resistor R_c is also important to determine the required power consumption of the stage. The minimum voltage drop across the resistor terminals can be calculated as:

$$V_{cc} - V_{out_{cm}} = V_{out_p} = R_c \frac{I_{tail}}{2} \tag{2.12}$$

with $V_{out_{cm}}$ defined as the common-voltage and V_{out_p} the single-ended peak amplitude of the output signal.

While I_{tail} and R_c can be calculated for the minimum voltage headroom and thus, the supply voltage of the amplifier, Vcc, can be finally determined, few considerations have to be taken:

- Typically the first pole in the frequency response of the differential pair amplifier is at the output. This is due to the physical size of R_c required to support high current flow which increases the capacitive parasitics in this node. In order to maximize the bandwidth of the amplifier, R_c should be as low as possible, increasing the required I_{tail} and thus, the power dissipation.
- For resistive loads, the R_c value should be in the range of the output impedance, for matching purposes ($50\,\Omega$, for instance).
- As analyzed in 2.1.4, the gain of the stage is dependent on the value of R_c.

- For low values of R_c, in order to maintain the required gain, R_e might reach a value too small, limiting the input amplitude range in which the amplifier behaves linearly (Fig. 2.4).

2.2.4 Amplifier Characteristics and Linearity

In general, it has been understood in the previous subsections how the determination of different values for the differential pair amplifier components, influences the power dissipation, gain and linearity. However, the relation between the values of the components and the required percentage of THD is yet to be shown. In order to understand better this tradeoff, simulations were performed of the simplified differential pair amplifier depicted in Fig. 2.3 for a set of different component values.

All the following items are common in the upcoming simulations:

- Frequency of the fundamental harmonic of the input signal: 1 GHz;
- Simulation analysis: harmonic balance at 27 °C;
- BiCMOS technology: IHP SG13G2 HBTs with f_T/f_{max} = 300/500 GHz;
- Ideal resistors and current source;
- Ideal voltage source for the input signal;
- No modulator load;
- The output amplitude is kept constant at 2 Vppd when sweeping R_c and R_e.

The aim of this analysis is to characterize the linearity of a differential pair amplifier, neglecting the impact on bandwidth and the effect of having output load. Obviously, for the final design of the amplifier, the high cutoff frequency impact has to be considered for the determination of the values of the components. Although, for that purpose, different techniques are also considered to compensate the performance of the stage at high-frequencies. These techniques are analyzed in the different driver designs in the following chapters.

The first set of simulations aims to investigate the g_m dependency on the linearity. The input amplitude is fixed at 0.5 Vppd for a required gain of 12 dB. In order to sweep the g_m value, the differential pair is biased with different values of I_{tail}. For each case, the HBTs are dimensioned to keep the same current density per finger, 1.5 mA. The results are presented in Fig. 2.6. It can be observed that the variation of THD for different $R_e I_{tail}$ values is consistent for different conditions of g_m. It can also be concluded that for a gain of 12 dB the required $R_e I_{tail}$ product to achieve 1 % of THD is approximately 150 mV and for a THD of 5 %, 50 mV would be enough. However, the drawback to achieve low values of THD is the required R_c value to obtain the gain of 12 dB and the output amplitude of 2 Vppd. Fig. 2.7 demonstrates the rise of voltage drop in R_c to accommodate the lower values of THD, increasing significantly the supply voltage and thus the power dissipation. Once again, the results are similar for different values of I_{tail} (g_m).

To explore ways of reducing the voltage drop across R_c for the more linear conditions, a second set of simulations was performed. In this case, the value I_{tail} was maintained and

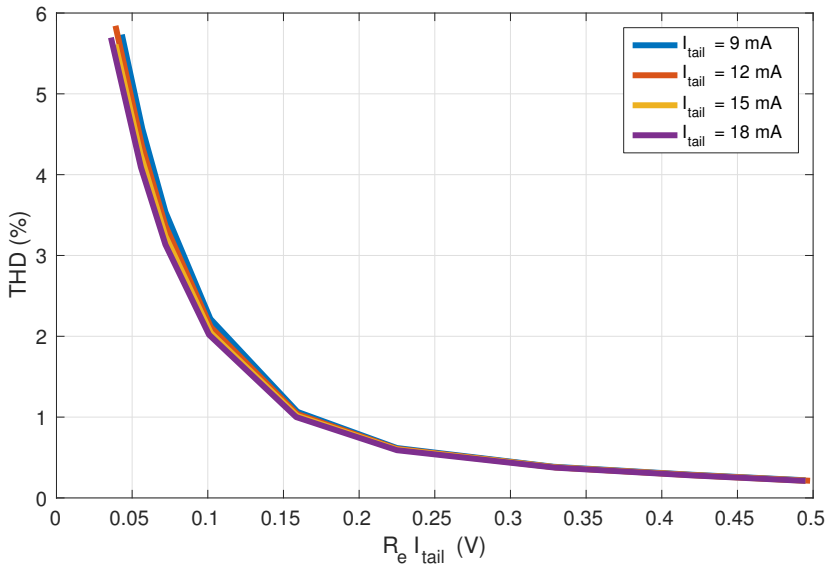


Figure 2.6: THD versus $R_e\,I_{tail}$ for different I_{tail} values (g_m change).

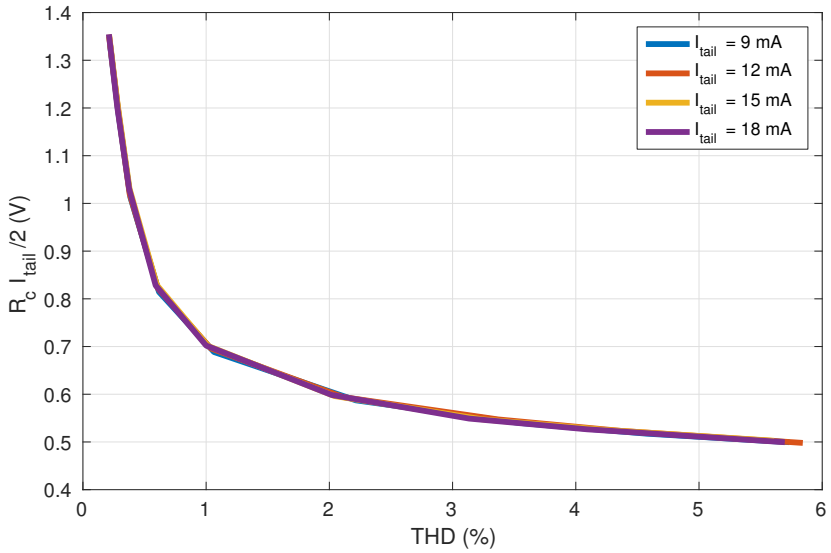


Figure 2.7: Voltage headroom ($R_c\,I_{tail}/2$) over THD values for different I_{tail} values (g_m change).

the transistor was modified to three different sizes, testing different current density levels per finger. The simulation results are displayed in Fig. 2.8. It can be observed that higher $R_e\,I_{tail}$ product is required for lower current densities to maintain the same THD. However, when the results are plotted in terms of voltage drop in R_c over the THD values (Fig. 2.9), it can be seen that the results are comparable. Therefore, the same voltage headroom in R_c is required for a given THD for different HBT sizes. Thus, using smaller HBTs could only be beneficial in power dissipation due to the saving of voltage drop across R_e.

Finally, the last analysis is performed keeping the same current I_{tail} and size of the transistors. In this set of simulations, the input amplitude is swept and the values of R_c and R_e are again chosen to achieve different THD for the same output amplitude of 2 Vppd. The input amplitude varies from 0.5 to 1 Vppd, therefore the gain changes between 6 dB and 12 dB. With lower gain values (using higher input amplitudes), the required R_c is also lower, according to the equation 2.7. However, as seen if Fig. 2.4, higher input amplitude will require higher

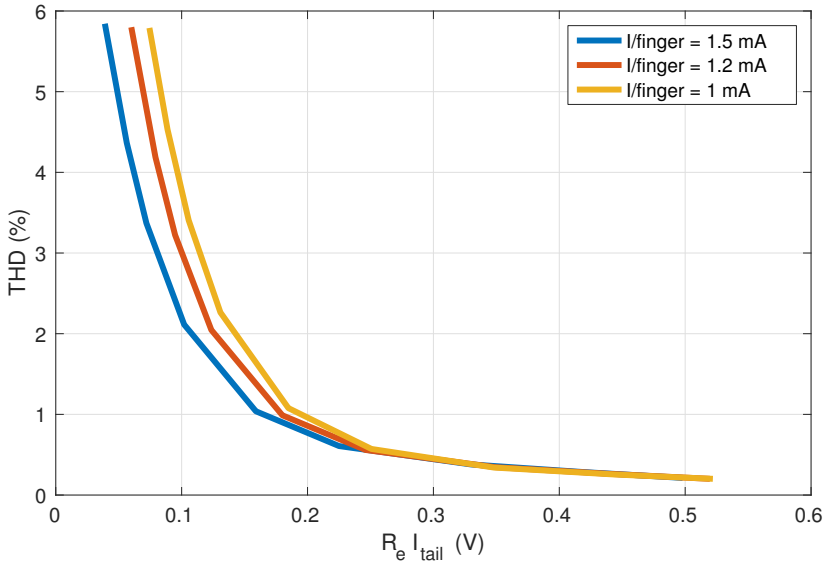


Figure 2.8: THD versus $R_e\,I_{tail}$ for different current densities per HBT finger.

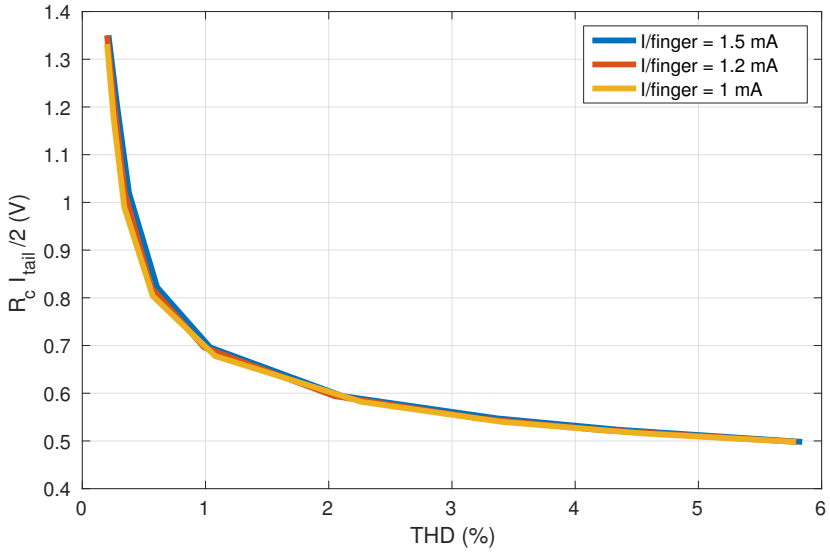


Figure 2.9: Voltage headroom ($R_c\,I_{tail}/2$) over THD values for different current densities per HBT finger.

$R_e\,I_{tail}$ product. Therefore, the goal of this simulation is to understand if decreasing the gain will somehow help reducing the amount of voltage drop in R_c to achieve low values of THD. Fig. 2.10 shows the results for the required voltage headroom for different input amplitudes. As predicted, in order to achieve low values of THD, less voltage drop across R_c is required. In contrast though, as observed in Fig. 2.11, the amount of voltage which drops in R_e is also increased to keep the linearity. Fig. 2.11 is now plotted in a similar way as Fig. 2.10, calculating the voltage drop in R_e and using the x-axis for the THD sweep. In this way, the graphs can be directly compared for different values of THD where the voltage drop is increasing the most, in R_e or R_c.

To make it even clearer, in Fig. 2.12 plots the sum of the voltage drop in the two resistors. Having this comparison, it will help the designer to determine the best strategy to find the most adequate gain value for the stage, depending on the THD requirement. For example, for a THD of 1 %, it can be observed that the power dissipation is quite constant for different input

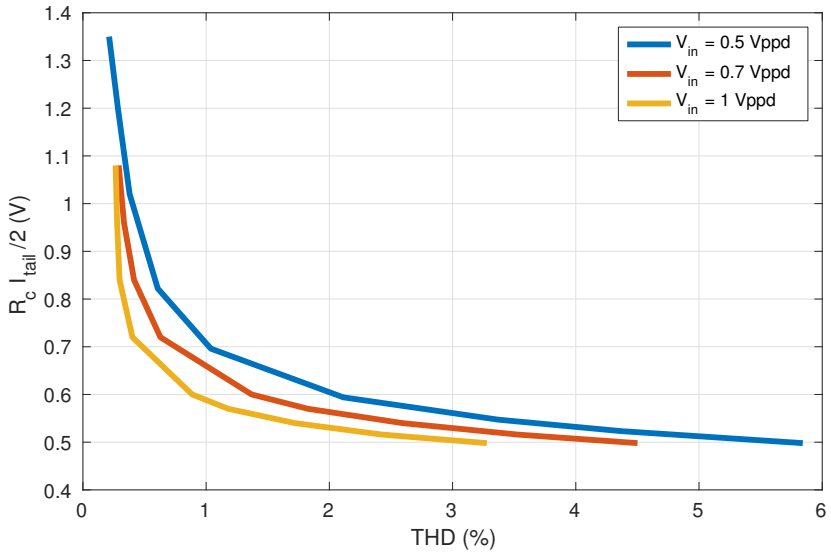


Figure 2.10: Voltage headroom ($R_c\, I_{tail}/2$) over THD values for different input amplitudes.

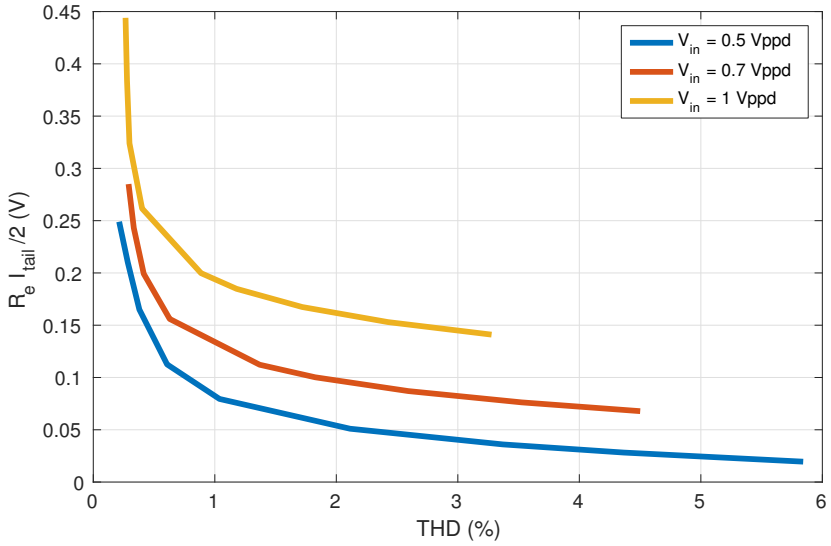


Figure 2.11: Voltage drop in R_e ($R_e\, I_{tail}/2$) over THD values for different input amplitudes.

amplitudes. However, for a THD of 3 %, the difference is more obvious and it is concluded that designing the stage for higher gain could benefit the power dissipation as the total voltage drop is less. Finally, it is also observed that for higher THD values, as for instance 5 %, the amplifier with lower gain cannot achieve such THD values. Thus, for a relaxed specification of linearity, using greater gain in this stage will be beneficial.

Typically, the drivers developed in this thesis have linearity requirements for a THD between 3 % and 5 %. Thus, it will be observed throughout the different designs that the strategy of confining most of the amplification at the output stage was followed, in-line with the conclusions of this analysis.

2.3 Mach-Zehnder Modulator

The Mach-Zehnder modulator (MZM) is a type of modulator used in the external modulation type of optical transmitters which modulates in phase and intensity as a response to an input

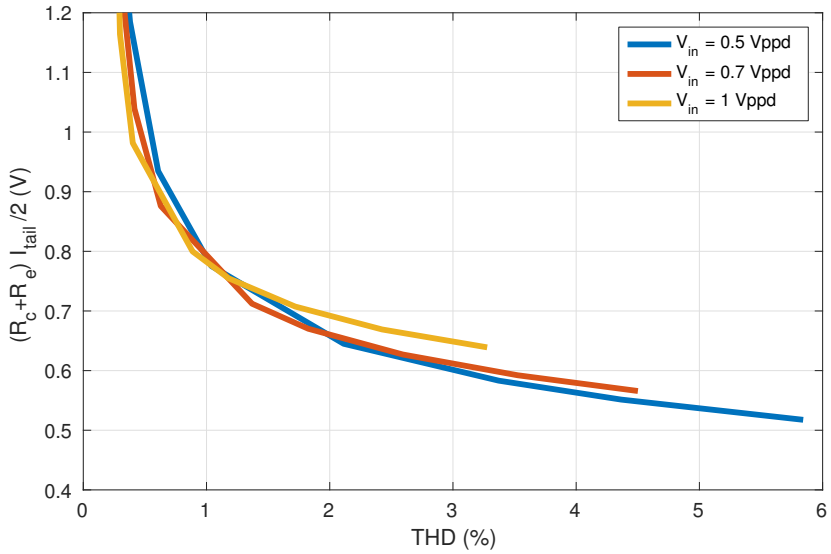


Figure 2.12: Sum of voltage drop in R_c and R_e over THD values for different input amplitudes.

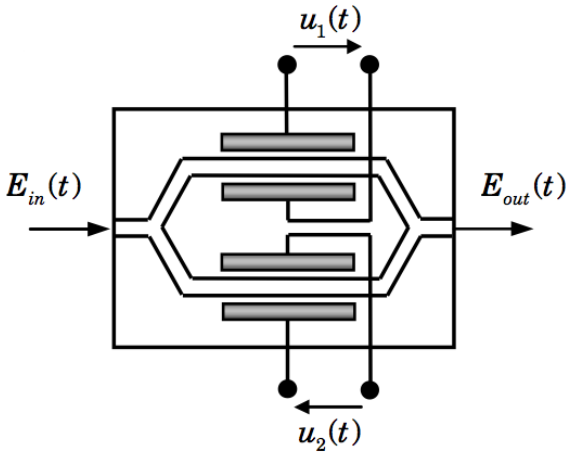


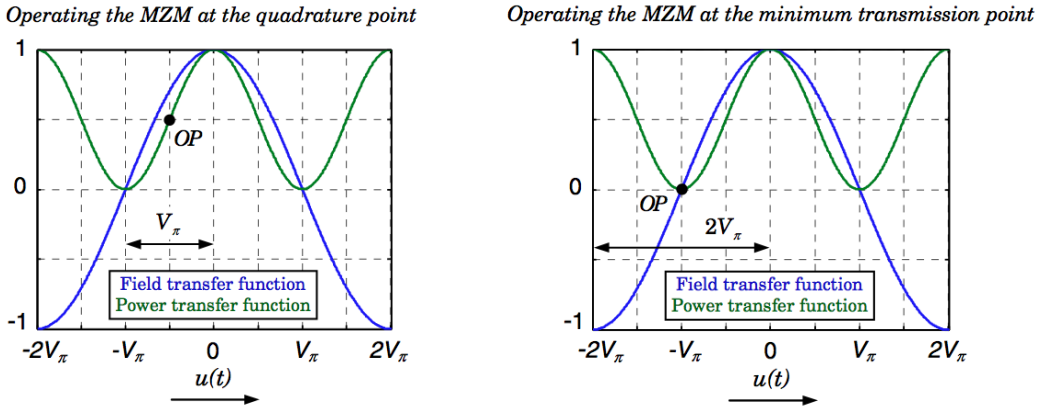
Figure 2.13: Integrated optical Mach-Zehnder modulador (dual-drive) [8].

voltage signal. A scheme of the MZM is depicted in Fig. 2.13. The modulator comprises two phase shifters driven by $u_1(t)$ and $u_2(t)$. A driving voltage necessary to obtain a phase shift of π, is denoted by V_π. The expression that lists the incoming optical carrier and the outgoing phase modulated optical field in each phase shifter was presented in chapter 1 in equation 1.1.

To cause intensity modulation of the optical lightwave, the principle of interference is a result of the process of phase modulation in the phase shifters, in a configuration known as dual-drive MZM. The incoming light is split into two paths, and by accumulating phase differences relative to each other, then the optical fields are recombined. The relative phase shift results in interference that can vary between constructive and destructive.

A Multimode interference (MMI) coupler is utilized to split the light at the input, redirecting each half of the power into the phase modulators of each arm. The drive voltage of each arm is specified by [8]:

$$u_i(t) = V_{bias\ i} + V_{RF\ i}\ ,\ \ i = 1, 2 \tag{2.13}$$



(a) MZM Operation in the quadrature point.

(b) MZM Operation in the minimum transmission point.

Figure 2.14: MZM Operation in the quadrature point and the minimum transmission point [8].

The MZM can operate in two modes: the push-push mode and the push-pull mode. In the push-push mode it is applied the same phase shift in both arms, it means that $u_1(t) = u_2(t)$. In the push-pull mode, $u_1(t) = -u_2(t)$, the phase is symmetric in both arms and a chirp-free amplitude modulation is obtained, decreasing the effect of the dispersion in the fiber. The expression of the output field can then be written as [8]:

$$E_{out}(t) = \cos\left(\frac{u(t)}{2V_\pi}\pi\right) E_{in}(t) \tag{2.14}$$

From the previous expression, it is possible to conclude that the MZM in push-pull operation is periodic with a period of $2V_\pi$.

The MZM can be biased in two points of the operation curvature: quadrature point and minimum transmission point. In Fig. 2.14 is presented these two modes. When the MZM is operating at the quadrature point, the bias voltage, V_{bias} is half of V_π. In this mode, the total voltage swing will be equal to V_π. With the MZM biased at the minimum transmission point, the driving voltage will vary a total of $2V_\pi$ with the operating point corresponding to the position in which the optical power is practically nonexistent [8].

Operating the MZM in push-pull mode leads to the possibility of building an IQ modulator. This type of modulator is shown in Fig. 2.15. With an IQ modulator is possible to modulate signals with high-order modulation formats, due to the usage of two child MZMs: the in-phase (I) and the quadrature (Q). To the quadrature part, a phase shift of $\frac{\pi}{2}$ is added, so then it is created the needed difference of phase between the two modulators. The two child MZMs have the operation point at the minimum transmission point, in order to provide the full constellation.

The amplitude modulation and phase modulation are given by the following expressions [8]:

$$a_{IQM}(t) = \left|\frac{E_{out}(t)}{E_{in}(t)}\right| = \frac{1}{2}\sqrt{\cos^2\left(\frac{u_1(t)}{2V_\pi}\pi\right) + \cos^2\left(\frac{u_Q(t)}{2V_\pi}\pi\right)} \tag{2.15}$$

$$\phi_{IQM}(t) = arg\left[\cos\left(\frac{u_1(t)}{2V_\pi}\pi\right) + \cos\left(\frac{u_Q(t)}{2V_\pi}\pi\right)\right] \tag{2.16}$$

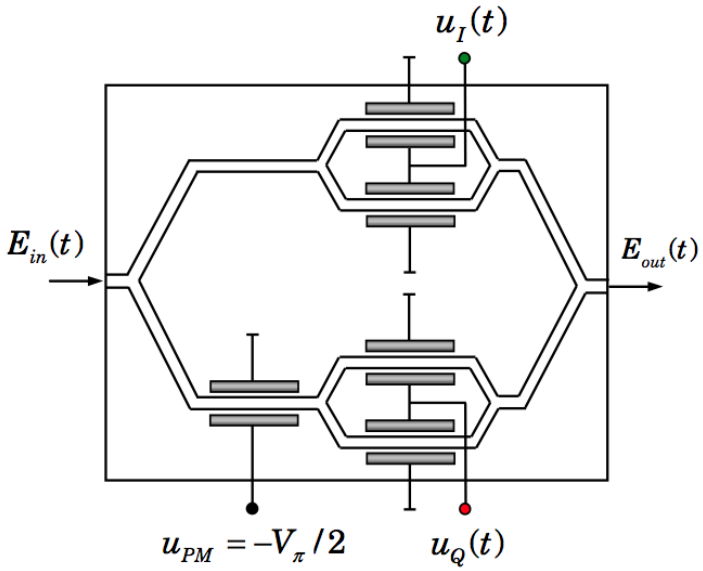


Figure 2.15: Optical IQ Modulator [8].

2.3.1 MZM Driving Approaches

A key metric in MZMs is the electro-optical modulation efficiency. It is technology-dependent and for depletion-mode silicon MZMs is considered as a weakness due to the fact that the overlap between optical mode and depletion region is relatively small [16]. The electro-optical conversion efficiency is determined by the normalized product $V_\pi L$ typically given in Vcm, where V_π, as described earlier, is the required voltage to induce π phase shift and L the phase shifter length. A key parameter for the quality of the transmitted digital optical signal is the extinction ratio (ER) defined by the ratio between the optical power levels corresponding to 0 and 1. To improve the ER either high driving voltages are needed or else the MZMs length needs to be increased, reducing the required voltage. Several driving schemes have been utilized to drive MZMs and they can be described in three categories: driving the modulator as a lumped element, as it is the typical case for short MZMs or resonant ring modulators [17]; driving of travelling-wave electrode Mach-Zehnder modulators (TWE-MZMs) and driving of segmented Mach-Zehnder modulators (SE-MZMs).

The lumped element topology (Fig. 2.16) requires the modulator to be relatively short in comparison to the operating electrical wavelengths in order to comply with the lumped condition up to reasonable frequencies. A total length for the modulator of $\lambda/10$ is accepted as the maximum dimension to this consideration, with λ the wavelength corresponding to the maximum targeted operating frequency of the data signal. For short MZMs though, very high driving voltages are required, which are difficult to achieve in Si high-speed drivers. Moreover, the driver is directly exposed to the total capacitance of the modulator, thus limiting high operation speeds. These points summarize the challenges to obtaining high ERs in optical transmitters using this approach.

The second approach is sketched in Fig. 2.17. It is commonly used in III-V modulators and results as an evolution from the lumped devices. In this configuration, instead of a large lumped capacitance, the capacitive load is distributed in transmission lines, designed to propagate the voltage along the modulator. This transforms the capacitive behavior of the modulator into

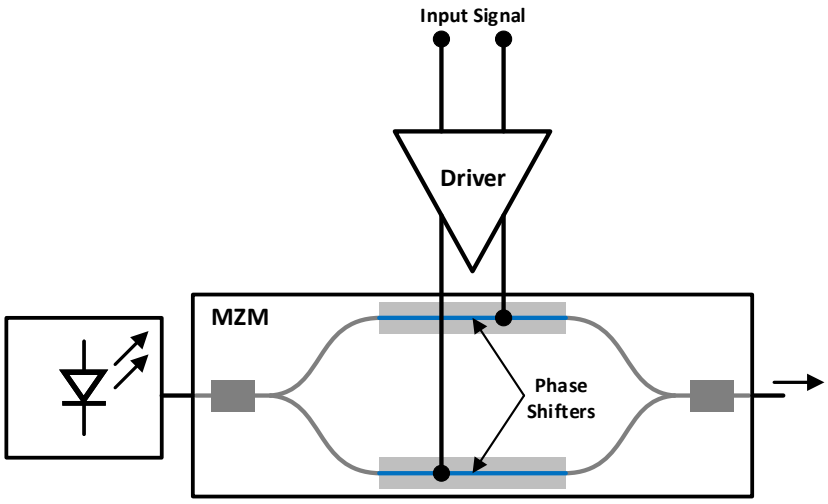


Figure 2.16: Lumped Electrode MZM driving scheme.

RF lines with characteristic impedance Z_0 and with differential termination of $2\,Z_L$. However, to maintain the electro-optical bandwidth, TWE-MZMs with high lengths are unfeasible. This occurs as, after a certain phase shifter length, the electrical losses are predominant, with no improvement in the efficiency [6]. Another critical issue for long modulators with high target electro-optical bandwidth is the mismatch between the velocities of electrical and optical waves. The electrical signal must propagate in the same direction and at precisely the same speed as the optical wave, permitting the phase modulation to accumulate monotonically irrespective of frequency. For the TWE-MZM approach, with increasing frequency and modulator length, velocity mismatch may cause anti-phase modulation between the two arms resulting in the cancellation of initial modulation. This behavior is critical at high frequencies, where the electrical signals are not considered as lumped compatible, and so it ultimately reduces bandwidth (demonstrated in subsection 2.4.3). To overcome the velocity mismatches between the two waves and to better control the characteristic impedance of the electrical transmission lines, a variant of the TWE-MZM, the segmented TWE-MZM, has been widely used, firstly studied and analyzed in [18]. In this approach, the modulator is divided into lumped segments, where the electrical transmission line is occasionally contacted. Hence, more flexibility to control the properties of the propagation of the electrical wave is obtained. However, the device still suffers from electrical losses that limit the total length that can be targeted.

To overcome mainly the electrical losses issue, the third type of driving, the SE-MZM is shown in Fig. 2.18, was introduced in [19] and already implemented in [20, 21, 22, 23]. By using this segmentation of the driver, the amplifiers are placed between the transmission line and the modulator, instead of having a single driver at the input of the modulator, detaching the electrical wave from the modulator parasitics. Using this topology, it is possible to keep the voltage constant for longer lengths, thus opening the possibility of targeting high-efficiency high-speed optical transmitters. Ideally, with this scheme, the same voltage can be effectively applied along the whole modulator length. Having the delay under control on the driver side, velocity matching between optical and electrical waves can be achieved, increasing the total performance of the modulator. Using the segmentation of the driver and modulator, schemes

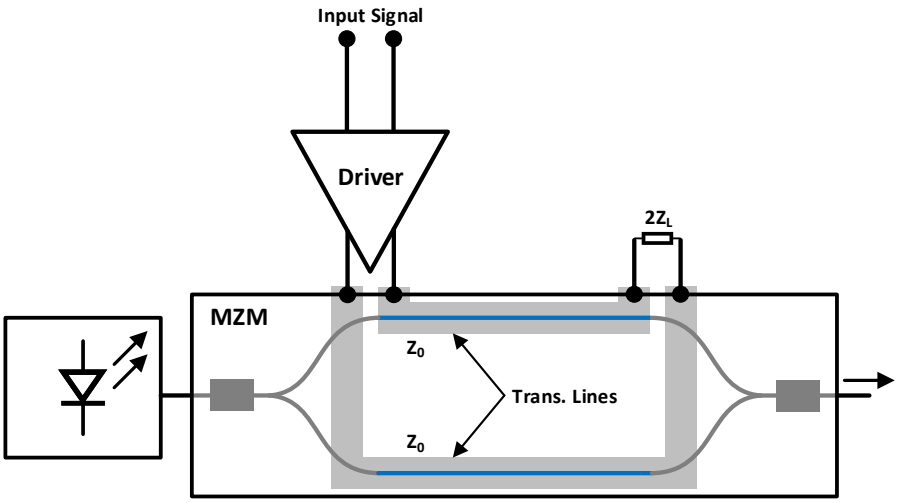


Figure 2.17: TWE-MZM driving scheme.

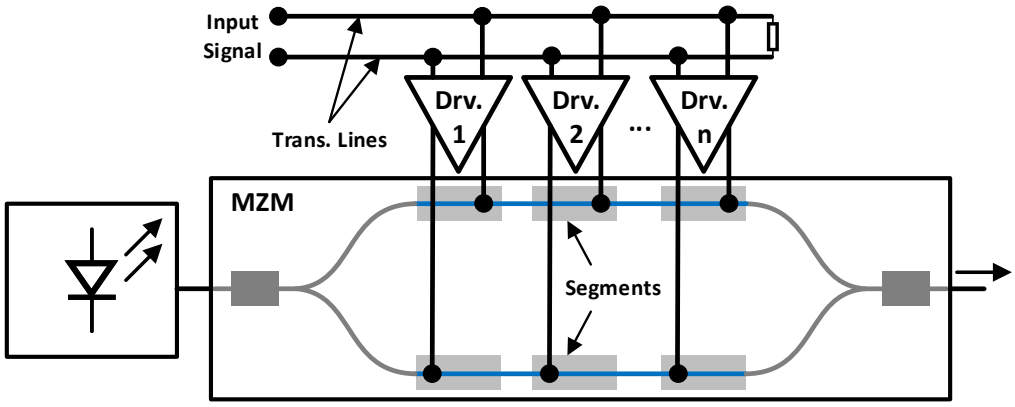


Figure 2.18: Segmented MZM driving scheme.

that integrate the DAC in the sub-system have been proposed [24, 25, 26], eliminating the need for an external DAC and offering power efficient topologies. However, a key drawback of such topology is the limitation regarding the number of digital inputs available, resulting in a reduced effective number of bits for the transmitter, required for pre-distortion techniques to compensate MZMs nonlinear transfer function (Fig. 2.14), when close to or fully-driven. For this reason, MZMs driven by linear drivers featuring external high-speed DACs are an essential matter of research [27, 28, 29] to produce a highly flexible optical transmitter for coherent communications using high-order modulation formats.

2.4 Electro-Optical Co-simulation

In order to design the segmented driving approach, due to the high integration level of electronics and photonics, the development of an electro-optical co-simulation methodology is of great interest. This simulation aims to incorporate electrical and optical domains together in one platform. Two main properties are modeled and reproduced in the simulation: the

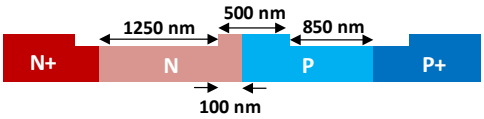


Figure 2.19: Cross-section of the MZM phase-shifter PN juction.

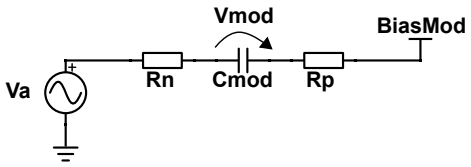


Figure 2.20: Electrical lumped model of the MZM phase shifter segment.

electrical model of the modulator and the electro-optical conversion. The electrical model is essential to determine the overall bandwidth of the transmitter, as the modulator is the driver load. The modeling of the electro-optical conversion has the aim of providing a simulation test-bench where it is possible to have an optical output to analyze the full transmitter performance and produce comparisons to electro-optical measurements.

2.4.1 Modulator Electrical Model

Fig. 2.19 depicts the cross-section of the PN junction of the MZM phase shifter implemented in the silicon photonics platform of IHP. The parameters chosen for this structure result from a trade-off between electro-optical conversion efficiency and optical losses. A detailed analysis can be found in [30]. When this PN junction is reverse biased and an RF signal is applied to its terminals, Va, the electrical model of the structure can be approximated to the circuit shown in Fig. 2.20. Cmod is the parasitic depletion capacitance and together with the series resistance of the phase shifter (Rn + Rp) results in the major bandwidth limitation on the system. Resistor Rp, resulting from the junction p-side, is the main contributor for the series resistance because of its lower doping. The dc voltage BiasMod is the reverse bias voltage applied to the junction. Finally, the amplitude voltage at the Cmod terminals is the voltage delivered to the phase shifter, represented as Vmod.

2.4.2 Electro-Optical Conversion Model

To prepare a full simulation of the transmitter, with a test-bench comprising an electrical input and an optical output, optical components have to be integrated in the simulator. These optical components are represented in a generic block diagram of a MZM in Fig. 2.21.

2.4.2.1 Phase-shifter

The optical depletion-type phase shifter ($\Delta\phi_{\mathrm{PS}}$) is modeled by using device simulation tools described previously in [30]. Effective index change behavior in the waveguide (Δn_{eff}) is a

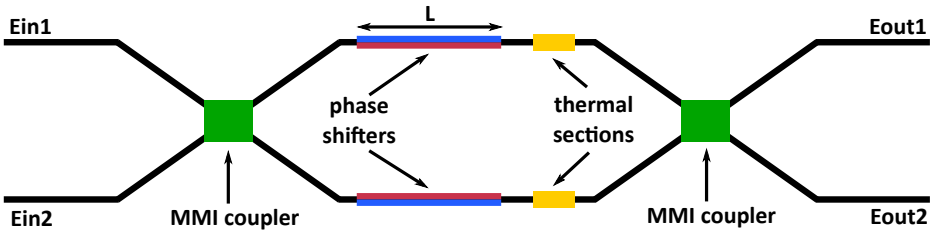


Figure 2.21: Block diagram of the MZM optical components implemented in the co-simulation.

function of the applied voltage on the phase-shifter (Vmod). The phase shift produced in this component is given by:

$$\Delta\phi_{\mathrm{PS}} = \frac{2\pi\ \Delta n_{\mathrm{eff}}(V\mathrm{mod})\ L}{\lambda} \tag{2.17}$$

where L is the phase shifter length and λ is the optical wavelength, 1550 nm.

The optical losses inside the phase shifter due to free carriers [30] are also dependent on Vmod and are calculated by:

$$Loss = L\ \alpha(V\mathrm{mod}) \tag{2.18}$$

where α is the absorption coefficient.

2.4.2.2 Optical propagation delay

The propagation delay of the lightwave is a key factor for long phase shifters due to the mismatch of the velocities of electrical and optical waves. The predicted refractive group index of the optical waveguide in the silicon photonics technology of IHP is $n_g = 3.6$ and the propagation delay (Δt) is calculated as follows:

$$\Delta t = L\ \frac{n_g}{c} \tag{2.19}$$

where c is the speed of light and L the length of the waveguide.

2.4.2.3 MMI coupler

This component is used twice in the MZM, at the input and at the output. At the input, it splits the signal into two arms for the differential modulation. At the output, it combines the modulated optical signals in phase, creating amplitude modulation. The MMIs used are 2×2 type (2 inputs and 2 outputs). The MMI at the input receives the CW laser light only from one input Ein1. At the output, only one of the outputs of Eout1 and Eout2 is used. The transfer function of a MMI coupler is described by the following calculation [30]:

$$\begin{bmatrix} \mathrm{MMI}_{\mathrm{out1}} \\ \mathrm{MMI}_{\mathrm{out2}} \end{bmatrix} = \begin{bmatrix} \sqrt{1-s} & j\sqrt{s} \\ j\sqrt{s} & \sqrt{1-s} \end{bmatrix} \begin{bmatrix} \mathrm{MMI}_{\mathrm{in1}} \\ \mathrm{MMI}_{\mathrm{in2}} \end{bmatrix} \tag{2.20}$$

where $\mathrm{MMI}_{\mathrm{in1}}$ and $\mathrm{MMI}_{\mathrm{in2}}$ are the inputs for each MMI coupler, $\mathrm{MMI}_{\mathrm{out1}}$ and $\mathrm{MMI}_{\mathrm{out2}}$ the outputs and s the splitting ratio which is set to 0.5 in this work.

2.4.2.4 MZM operating point

The operating point of the MZM is set by a thermal tuning section. This is a heating element present at the end of both arms of the modulator which can also be used for small adjustments to address unwanted asymmetries in the device. Temperature tuning is achieved by applying dc voltage on a metal layer on top of the waveguide, changing the optical effective index altering the signal phase. In the simulation, this effect is reproduced as a simple phase shift:

$$\phi_{\text{out}} = \phi_{\text{in}} + \Delta\phi_{\text{TS}} \tag{2.21}$$

where ϕ_{in} is the optical phase before the section, ϕ_{out} after the section and $\Delta\phi_{\text{TS}}$ the difference set by the heating effect.

For IQ modulations, no phase offset is necessary to be applied, as the modulator is biased in the minimum point. As the scope of the work developed in this thesis is to use amplitude modulations, the MZM is set in the quadrature point. In this case, the thermal section is set to provide a phase difference of $^{\pi}/_{2}$. The described two points of operation may be recalled in Fig. 2.14.

2.4.2.5 Simulation platform

The models of the described optical components are incorporated together with the electrical design environment used in this work, *Cadence® Virtuoso®*. Equations are directly translated into *VerilogA* instances [31], making it compatible with *Cadence® spectre®* simulation engine. The resulting integration provides the possibility to analyze the optical output of the full transmitter directly in one simulation where the segmented driver and modulator are designed.

2.4.3 Electrical and Optical Waves Velocity Mismatch Analysis

In subsection 2.3.1, it has been introduced one of the motivations for the MZM to be driven in a segmented manner. The electrical and optical waves are detached and the propagation delays of the waves can be better matched. Using the electro-optical co-simulation developed in this work, it is possible to analyze the impact on the modulator performance when velocity mismatch exists between the two waves, and how much accurate has to be the delay matching between them.

A testbench was prepared with the model of the Si MZM described before, with the phase-shifters divided into 16 segments. From the electrical side, an ideal model of a 50-Ω transmission line was used with adjustable group delay. The connections from the electrical transmission lines to the MZM include ideal drivers in-between to drive the RC load of the phase shifters in each segment. The total length considered for the MZM was 6.4 mm. The propagation delay of the optical wave is kept constant in the model of the MZM and the electrical delay is swept from zero to 20% of mismatch. A normalized magnitude of the optical output of the MZM is plotted over frequency to observe the impact of the mismatch on the electro-optical bandwidth of the transmitter. For an RC load in each segment of C_{mod}=150 fF and R_{n}+R_{p}=25 Ω, the expected bandwidth is approximately 42 GHz.

The results of the simulation are plotted in Fig. 2.22. It can be observed that for the curve with no mismatch the 3-dB bandwidth value is close to the expected 42 GHz. However,

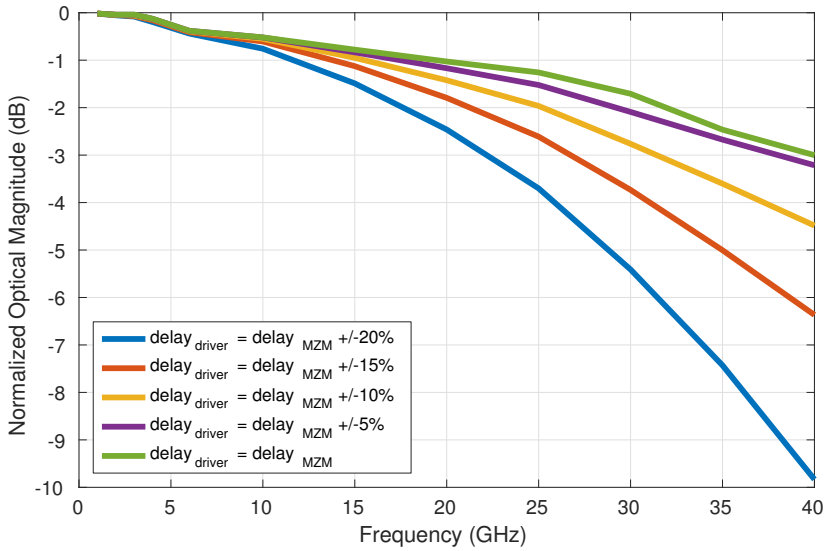


Figure 2.22: Impact on the MZM bandwidth of the velocity mismatch between electrical and optical waves in the segmented driving approach.

as the mismatch of the propagation delay between electrical and optical waves increases, the bandwidth value drops to 22 GHz for the case of 20% of mismatch. The results of this simulation highlight the importance of matching the velocity of electrical and optical waves for long MZMs.

3

Monolithically Integrated Modulator Drivers

An increased challenge for symbol rates above 50 Gbaud is the required bandwidth of the electro-optic components while still offering a cost-effective, low power, small form factor solution. Integrated silicon photonics has emerged as an attractive technology platform to provide such high-performance transceivers. It holds the promise of low manufacturing cost, high yield and a high degree of integration, by incorporating the electronic driver and the modulator on the same chip. Solutions based on EPICs offer reduced interconnection parasitics between the electrical and photonics parts, omitting the usage of bondwires and bondpads, enabling high bandwidth and high electro-optic modulation efficiency. Monolithic co-integration of silicon photonics with RF driving electronics and digital logic based on high-performance BiCMOS permits extremely compact solutions with reduced off-chip control overhead. This combination allows for cost-effective sub-systems of improved manufacturability.

Results have been published in [32, 33, 34], demonstrating the feasibility of 112 Gb/s PAM-4 transmission over 80 km, but have been achieved with a bulky and expensive $LiNbO_3$ MZM and external drivers. The motivation of the work described in this chapter is to achieve up to 112 Gb/s data-rate PAM-4 transmissions using segmented depletion-type MZM with linear driver amplifiers monolithically integrated in an EPIC BiCMOS technology. Designs are explained and measurements are performed to demonstrate the performance of the transmitter prototypes. Two implementations of the electro-optical transmitter are described, integrating linear driver and modulator. The first design targets an electro-optical 3-dB bandwidth close to 20 GHz, using a first-generation Si depletion-type MZM with simple implantation, and a first generation driver with a common-emitter amplifier topology. A second version is thereafter designed where the modulator is improved with additional implants (n^{++}, p^{++}) easing the electrical load for the driver, and the output stage of the driver is also improved with the usage of a cascode stage which increases the amplifier gain-bandwidth product. This version shows a much improved 6-dB bandwidth up to 40 GHz.

3.1 A 50-Gb/s Segmented Linear Driver and Modulator

The electro-optical transmitter described in this section is the first optical transmitter comprising linear driver and segmented depletion-type MZM in a single chip, making usage of the EPIC 0.25 µm SiGe:C BiCMOS technology platform from IHP [35, 36]. First of all, implementing the driver in this technology uses an important advantage of BiCMOS in comparison with other CMOS approaches, as it features high break-down voltage HBTs for comparable high f_T values. For instance, the 65nm-CMOS process of STMicroelectronics has a transit frequency (f_T) of 170 GHz and maximum oscillation frequency (f_{max}) of 240 GHz for a core voltage of 1.2 V [37]. In comparison, the IHP process here used (SG25H4EPIC) with similar f_T=f_{max}=190 GHz, the HBT transistors have $BV_{CEO} = 1.9$ V and $BV_{CBO} = 4.5$ V, featuring high break-down voltage suitable for power applications. Additionally, the possibility of monolithic integration incorporating the driver and the modulator in the same chip offers great flexibility in the positioning of the devices and leads to the reduction of interconnection parasitics between devices [38]. Hence, such integration can enable numerous possibilities for performance enhancement in terms of bandwidth [26] and electro-optical efficiency of the complete transmitter.

This work is firstly introduced in [39] where preliminary results are shown, demonstrating OOK transmission at 28 Gb/s with 13 dB of ER. In [40, 41] electro-optical bandwidth is measured in addition to new time-domain measurements with OOK modulation format, presenting data transmission up to 32 Gb/s with 11 dB of ER. In [42], as in this thesis, the transmitter implementation is fully described and a demonstration of the linearity performance of the driver through detailed characterization is also presented, showing detailed results of the linear driver and electro-optical measurements with PAM-4 modulation format, where data-rates up to 50 Gb/s are demonstrated.

This electro-optical transmitter follows a segmented topology already introduced in chapter 2 in the description of the electro-optical co-simulation, section 2.4. A block diagram of the implemented design is shown in Fig. 3.1. The modulator is divided into 16 segments, each segment acting as phase shifter that can be approximated as the RC lumped element, also described in chapter 2. The driver amplifier part integrates two stages. The input stage is matched at the input to 50 Ω and drives a differential signal to two single-ended transmission lines. The second stage of the driver is distributed laterally to the MZM segments. Each driver segment senses the differential voltage from the lines, amplifies it and applies the required amplitude to each section of the modulator. The differential outputs of the driver segments are connected to the n-side of the two MZM arms. An external dc voltage is applied to the p-side of both arms, setting the reverse bias voltage for the phase shifters. The modulator load represents the dominant pole, determining the overall bandwidth of the transmitter. The driver is strategically positioned between the MZM arms, providing optimal symmetry in the layout level. As described before, using the segmented driver approach, the electrical transmission lines for the differential signal are detached from the modulator, opening the possibility of optimization in terms of loss reduction and delay matching. The optical part is also represented in Fig. 3.1. The optical interface is located on the left side. At the input, a CW optical signal from the laser is injected. This signal is then split into two arms of the

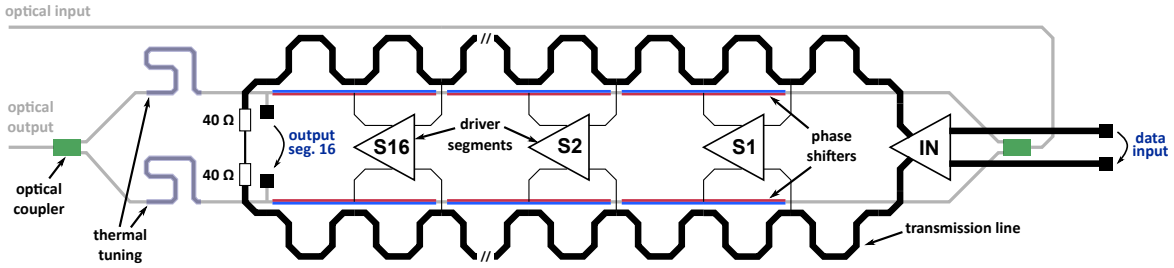


Figure 3.1: Block diagram of the monolithically integrated segmented driver and MZM.

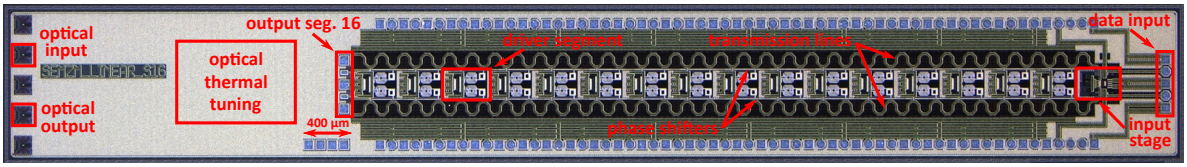


Figure 3.2: Chip microphotograph of the optical transmitter.

MZM using one MMI coupler. The two phase shifters modulate the optical signal according to the applied voltage. Finally, the two arms are combined using another MMI coupler, where the optical signal is modulated in amplitude due to the constructive and destructive interference created by the phase difference between the two arms. The block diagram can be compared to the chip microphotograph presented in Fig. 3.2. The monolithically integrated linear driver and modulator occupy an area of 12.7 mm^2 (9.8 mm × 1.3 mm).

3.1.1 Transmitter Design

3.1.1.1 Mach-Zehnder Modulator

In this design, the MZM has an efficiency of 2.9 Vcm. A length of 6.08 mm was chosen to the designed MZM. The determination of the length was based on the maximum voltage amplitude that the driver could apply. Due to the common-emitter configuration of the output stage, the maximum amplitude is limited by the collector-emitter breakdown of 1.9 V (BV_{CEO}). For the chosen length, the required V_π is 4.75 V. For amplitude modulation, the operating point of the modulator is set in the quadrature point and consequently to achieve nearly the maximum ER, the driver delivers a differential amplitude up to 4 V. The 16 segments of the phase-shifters in each arm have a length of 378 µm each, using 2 µm of separation. The segment length was chosen to support data transmission up to 38 GHz, when approximated by a lumped equivalent circuit model. This is determined assuming as lumped element a structure with maximum dimension of $\lambda/10$. As presented in Fig. 2.20 the electrical equivalent model is a series resistance and a load capacitance with the values of 50 Ω and 150 fF respectively, for a reserve bias of 1.5 V.

3.1.1.2 Driver input stage

In Fig. 3.3 the schematic of the input stage is presented. First, there are two 50 Ω resistors for input matching. Next, emitter-followers (EFs), with HBTs Q1 and Q2 smaller than Q3 and Q4, are used to decrease the capacitance seen by the input signal, hence lowering the impact

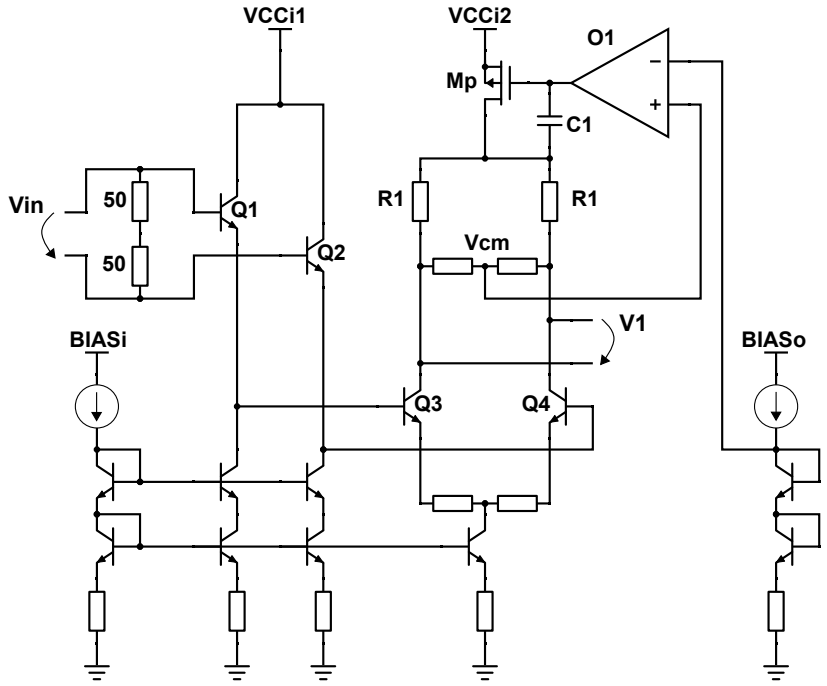


Figure 3.3: Driver input stage schematic.

on the bandwidth. The differential pair (Q3, Q4) amplifies the signal, with a gain of 1 dB. This gain can be adjusted with the bias current through "BIASi". Resistors R1 are matched to the characteristic impedance of the transmission lines. This differential pair, apart from acting as a buffer between the input and the transmission lines, also sets the operating point of the following stages, the driver segments, using a LDO voltage regulator at the supply node. The LDO has as reference two diode connected transistors that set a voltage amplitude equal to $2V_{\mathrm{BE}}$. This voltage is equivalent to the dc voltage drop that the signal will encounter in the driver segment stage. The PMOS Mp together with the OpAmp O1 constitute a negative feedback loop where capacitor C1 is used to compensate the loop. The loop operates as follows. When the bias current is increased, adjusting "BIASo", the value of $2V_{\mathrm{BE}}$ will slightly increase. The OpAmp O1 reacts and decreases V_{SD} of the PMOS. This will equalize "Vcm" to the new $2V_{\mathrm{BE}}$ value, which increases the current in the driver segments. In this way, the bias can control the gain of all driver segments, removing the need of current-mirrors in those stages, making use of the connected HBTs bases through the transmission lines.

3.1.1.3 Driver segments

The schematic for this stage is depicted in Fig. 3.4. EFs are utilized to minimize the influence of the segment in the characteristic impedance of the transmission line due to their high input impedance. Transistors Q5 and Q6 are also sized to minimize the impact of the input capacitance in the transmission line. Thus, the EFs act as buffers between the sensed signal from the transmission line (V2) and the gain stage. This gain stage consists of a differential pair (Q7, Q8) providing 12 dB of gain. This stage is loaded with the correspondent modulator section. In order to improve the linearity and the stability [43] of the amplifier, degeneration resistors were included in the differential pair (Re1, Re2). Moreover, to compensate the transmission line loss that occurs especially towards the last segments, Re1 resistors are

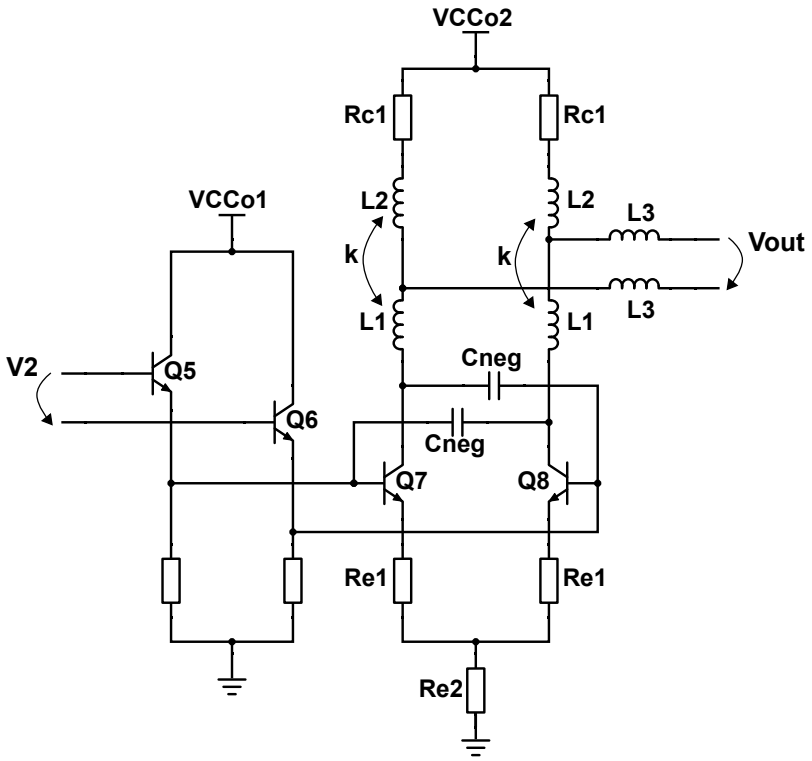


Figure 3.4: Driver segment schematic.

sequentially reduced to adjust the gain on those sections. Thus, the applied voltage to the modulator is maintained constant throughout the whole length of the modulator. With the reduction of Re1, Re2 resistors (stage's current-source) are increased, maintaining the current and the power dissipation. Resistor Re2 is also used to enhance the CMRR. Each driver segment dissipates 120 mW when the maximum gain is set by "BIASo". In order to improve the bandwidth of the differential pair, negative Miller capacitance and T-coil inductive peaking techniques were utilized.

Negative Miller capacitance technique As observed in Fig. 3.4, cross-coupled capacitors were connected between the differential pair inputs and outputs. This creates an effect named negative Miller capacitance that neutralizes the input capacitance of the stage [44, 45]. As referred before, the sizes of the EFs are kept small so as not to load the transmission line. This, however, reduces their driving capabilities. Fig. 3.5 displays a set of simulations for different values of Cneg in order to find the best value to recover the bandwidth of the EF. It can be observed that for high values, the curve presents high peaking that could translate into an unstable stage. This happens when the overall input capacitance of the differential pair turns to negative, becoming an inductive load for the EF, resulting in instability [46]. The value chosen for the cross-coupled capacitor Cneg was 30 fF.

T-coil technique This technique was used to enhance the bandwidth of the amplifier, which is limited by the modulator load. The T-coil is an inductive peaking technique which is more effective in comparison to conventional shunt-peaking inductor, as it can increase the cut-off frequency by 3 times [47]. The T-coil consists in 2 inductors (L1 and L2) with

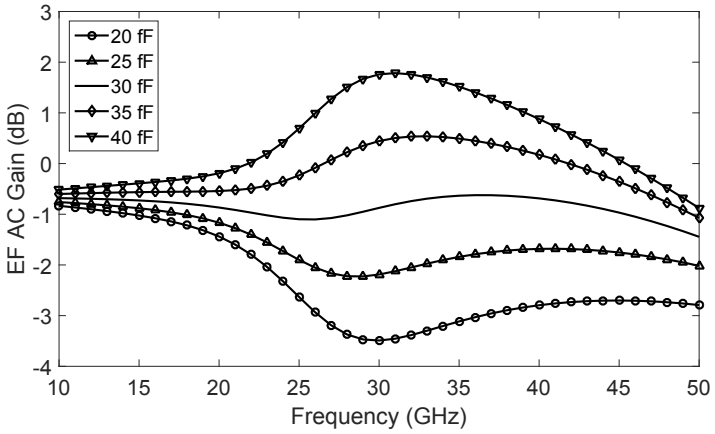


Figure 3.5: Simulation of different values of Cneg to determine the negative Miller capacitance value.

similar values of inductance coupled by a k factor. This combination results in 3 effective inductances, two of them in-place of L1 and L2 and a third in series to the amplifier load. To find the best value of L1 and L2, an initial value is taken from the calculation R^2C [47] where R is the collector resistance and C the capacitance that the amplifier has as load. The value is optimized after several electromagnetic (EM) simulations, to take into account the parasitic resistance and capacitance added to the stage. The k factor can be negative or positive. In this design, positive k factor was chosen, as the load capacitance is much higher when compared to the self parasitic capacitance of the amplifier [48]. The final coupling factor value is established after a few iterations in the simulation. Fig. 3.6 analyzes different coupling factors without changing the inductance values. The coupling impacts the performance in the range of frequencies from 10 to 20 GHz. This can observed by the fact that the gain curve becomes more flat when the k factor value is increased. As seen in section 2.4 (Fig. 2.20), the load has a series resistance. To overcome the damping effect of this resistance towards higher frequencies, a third inductor L3 was added to the amplifier. The presence of this inductor creates additional peaking in the range of 30 GHz, approximately the cut-off frequency value of the RC load. In order to find adequate inductance value, simulations with different values of L3 were performed. Fig. 3.7 displays simulation results for the various peaking structures. The value of 350 pH was selected as a compromise between flatness and achievable bandwidth.

3.1.1.4 Transmission line

In the SG25H4EPIC process there are five metal layers available, two thick top metals and three lower layers. The two top layers support high current density, having thickness of 2 µm and 3 µm. They are also suitable for RF passive components design (inductors and transmission lines) due to the low sheet resistance. Therefore, the transmission lines were designed in the most top thick layer and the ground shield was implemented in one of the bottom thin layers, following a microstrip design.

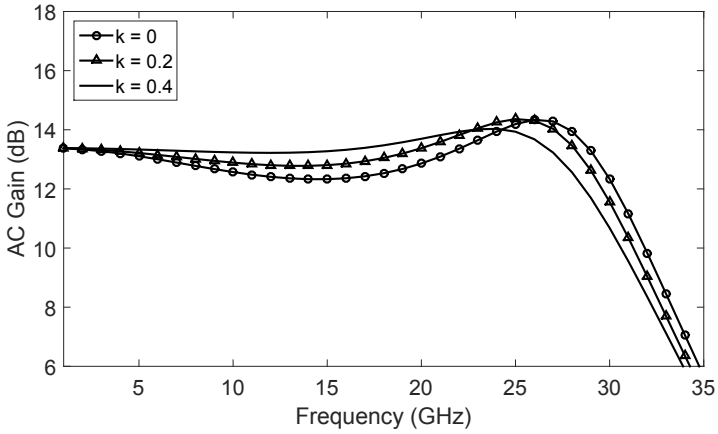


Figure 3.6: Simulation of the effect of coupling in the T-coil design.

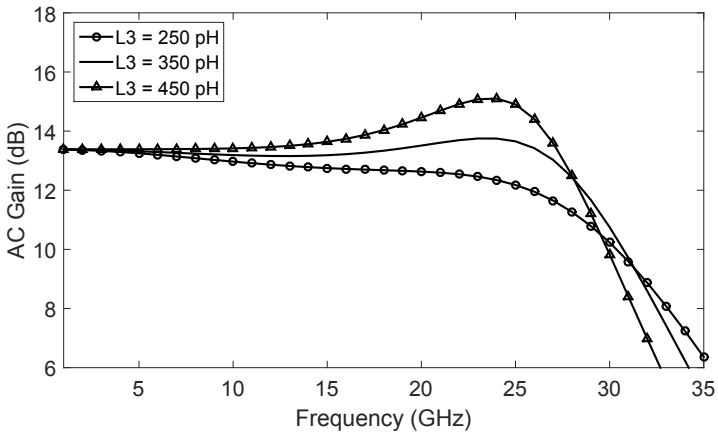


Figure 3.7: Simulation of the contribution of the inductor L3 to the driver frequency response.

The differential signal propagates through the transmission lines from the first to the last segment. The electrical effective refractive index is 2.1, based on EM simulations. The total length of the line is 5.7 mm (15 × 380 µm). For the best electro-optical response, due to different propagation speeds of electrical and optical waves, the electrical transmission lines were folded to create an additional artificial delay. Using this technique, the timing difference between both waves was reduced, achieving the required delay value. This optical propagation delay is 4.6 ps, per segment, according to equation 2.19. Moreover, in order to minimize the electrical loss within the transmission line, its characteristic impedance was designed to be 40 Ω. With this impedance alteration, the lines are wider (18 µm) than conventional 50-Ω lines, reducing the loss along the line. The lines are terminated with resistors making use of the virtual ground arising from differential excitation.

3.1.1.5 Single-segment variant

An additional IC was designed to ease electrical characterization of the driver. The block diagram of this IC is shown in Fig. 3.8. It comprises the same input stage as in the full driver but only one driver segment. From the driver segment, an electrical output is taken, allowing electric measurements. Due to the 50-Ω environment, the driver does not provide nominal gain and the output swing is reduced to approximately half. This happens because the driver

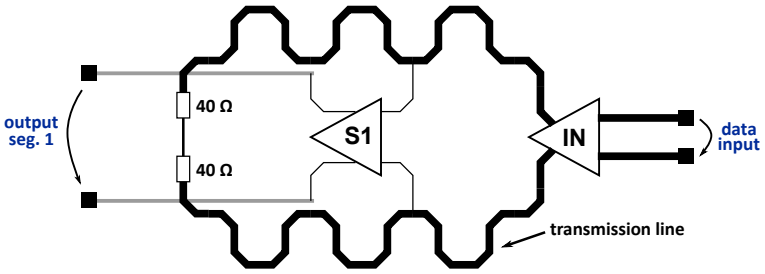


Figure 3.8: Block diagram of the single-segment variant.

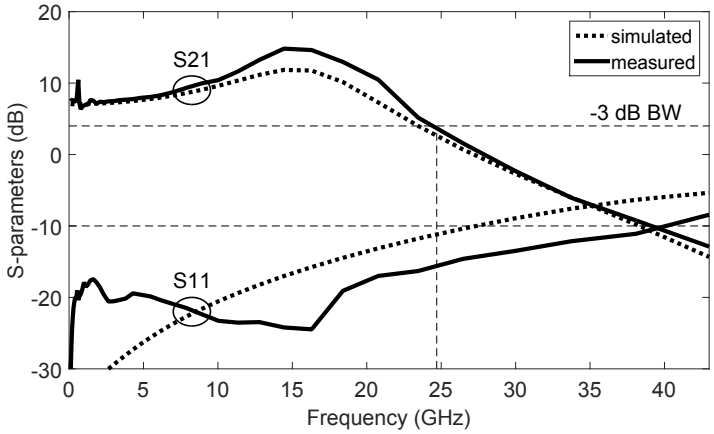


Figure 3.9: Driver S-parameters results. Comparison between post-layout simulation and measurements.

segment has a collector resistor (Rc1) of 70 Ω, which in parallel with 50-Ω load results in 27 Ω. However, characterization of this variant was valuable in order to compare with the simulation results.

3.1.2 Measurement Results

The measurements of the transmitter were performed in two parts. Firstly, the driver was independently characterized using mainly the single-segment variant, described in subsection 3.1.1.5. Thereafter, electro-optical measurements were executed to demonstrate the full transmitter operation.

3.1.2.1 Electrical characterization

True differential S-parameter measurements were performed on-wafer using a Rhode & Schwarz ZVA67 Vector Network Analyzer. The comparison between simulated and measured S-parameters is plotted in Fig. 3.9. During S-parameter measurements, as the driver is not loaded with the targeted impedance (MZM segments), the gain falls from the expected 14.5 dB to 7 dB. The 3-dB bandwidth of the driver is found to be 25 GHz. The input return loss is also presented in Fig. 3.9. The driver shows good input matching, with S11 being less than -10 dB up to 40 GHz.

Additionally, to demonstrate the linearity of the driver, THD was measured for a set of frequencies. The setup to perform these measurements is described as follows: the signal at

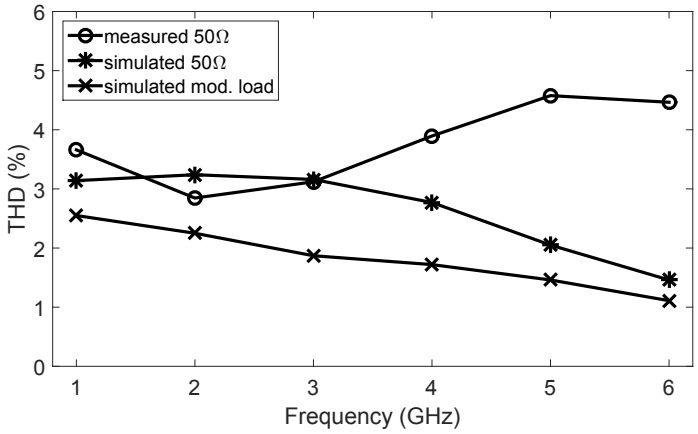


Figure 3.10: THD results. Comparison between measurements and simulation.

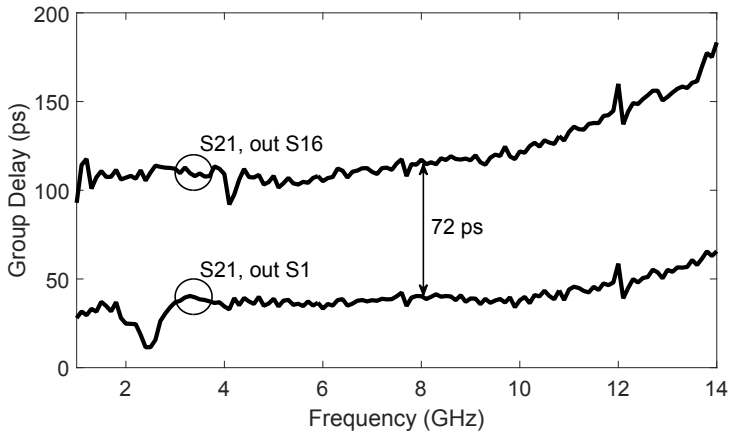


Figure 3.11: Group delay from the input to the output of the 1st segment and from the input to the output of the 16th segment of the driver.

the input is generated using Keysight PSG Analog Signal Generator E8257D (up to 20 GHz); the signal is converted to a differential signal using a balun, that works from 1 to 12 GHz, and connected to the chip; at the output another balun, this one with bandwidth up to 18 GHz, combines the differential signal into a single-ended signal that is connected to a Rhode & Schwarz FSUP Signal Source Analyzer (up to 26.5 GHz). Frequency tones from 1 to 6 GHz with 1 GHz step were generated at the input and the output spectrum data was collected through the Signal Analyzer. After accounting for the losses of the setup (cables and baluns) at the input and at the output, the data was processed and THD values were calculated. Due to the limited frequency response of the baluns, THD was only measured until 6 GHz, so that up to the third harmonic of the signal could be included (18 GHz). As observed in Fig. 3.9, the measured curve gain has higher peaking than in the simulation. As this peaking occurs at 18 GHz, worse measured THD in comparison to the simulated is expected in the range of 5 to 6 GHz. Nevertheless, the measured THD is still found to be below 5% for the nominal differential input amplitude of 800 mVpp, demonstrating the linear capability of the driver. Moreover, as the measurements were performed in a 50-Ω environment, and as described before in subsection 3.1.1.5, the gain and the headroom for the signal is limited at the output. To

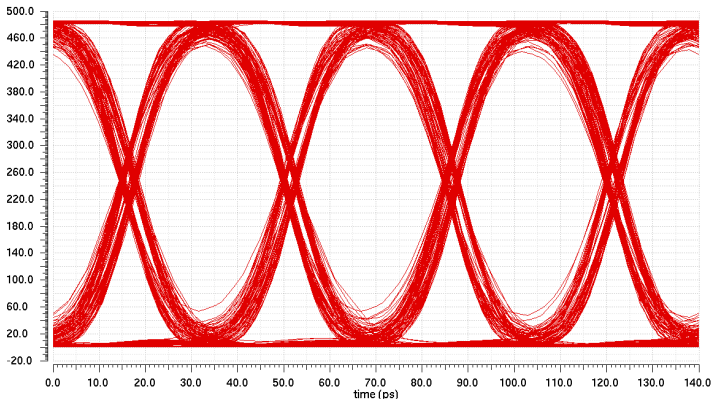


Figure 3.12: Simulated optical output eye-diagram transmitting OOK signal at 28 Gb/s, using the co-simulation.

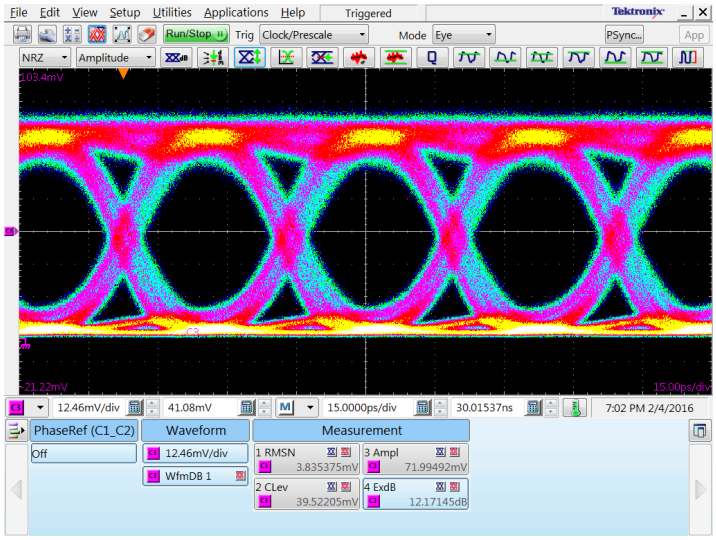


Figure 3.13: Measured optical output eye-diagram transmitting OOK signal at 28 Gb/s using 2^{31}-1 PRBS without pre-emphasis.

show that the driver would perform better when loaded by the modulator, the simulated THD with the nominal load is plotted in Fig. 3.10.

Finally, in order to validate the propagation delay of the electric wave in the driver transmission lines another test was performed. As seen in the block diagram of the full transmitter in Fig. 3.1, an electrical connection at the last segment was made available through extra pads. Measuring the S-parameters of the complete transmitter, having as port 2 the output of the last segment, it was possible to analyze the group delay from the input to the output of the sixteenth segment. Similarly, the group delay was extracted from the S-parameters measurement of the single-segment variant, having then the delay from the input to the output of the first segment. With this data, calculating the difference between the two group delays, results in the difference of time between the first and the sixteenth segment, correspondent to the propagation delay in the transmission line. However, it has to be taken into account, that in the case of the measurement of the full transmitter, the modulator RC load is also present, in addition to the 50-Ω load of the setup. This results in discrepancies for higher frequencies, as the gain response will change due to the different location of the peaking, affecting the group delay response as well, which is the reason this test is only meaningful

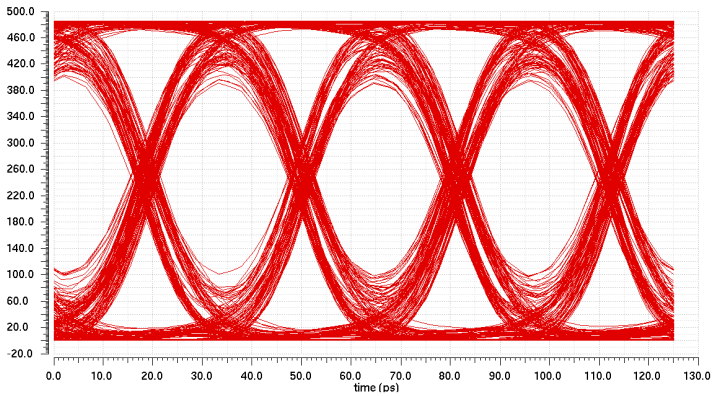


Figure 3.14: Simulated optical output eye-diagram transmitting OOK signal at 32 Gb/s, using the co-simulation.

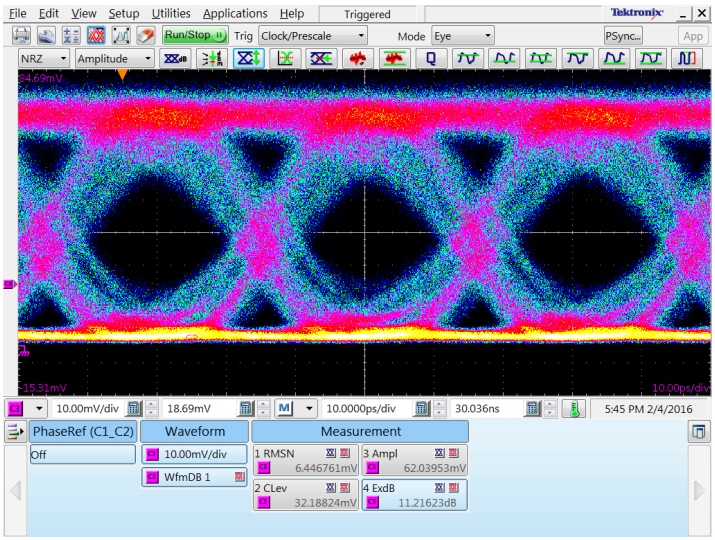


Figure 3.15: Measured optical output eye-diagram transmitting OOK signal at 32 Gb/s using 2^{31}-1 PRBS without pre-emphasis.

at the lower frequencies. Fig. 3.11 presents the comparison between the two group delays, showing a difference of approximately 72 ps, which is very close to the targeted propagation delay of 15 × 4.6 ps (69 ps).

3.1.2.2 Electro-optical measurements

Firstly, OOK time-domain electro-optical measurements of the full implementation were performed. To demodulate the optical signal, a photodiode was utilized connected to a sampling oscilloscope. An electrical signal with a bit pattern of PRBS31 was connected to the transmitter input. The differential input voltage amplitude was 700 mVpp. Fig. 3.12 presents the transmitter simulated optical eye-diagram at 28 Gb/s and Fig. 3.13 the measured one, featuring an ER of 12 dB [41]. The transmitter was also measured at 32 Gb/s, and Fig. 3.14 and Fig. 3.15 show the results at this data-rate, featuring an ER of more than 11 dB [41]. The measured and simulated eye-diagrams show good agreement.

The next test, electro-optical characterization of the whole transmitter in frequency domain, was performed with a lightwave component analyzer (LCA) Keysight N4373D with 2 electrical ports, to create the differential input, and 1 optical port, which receives the modulated signal.

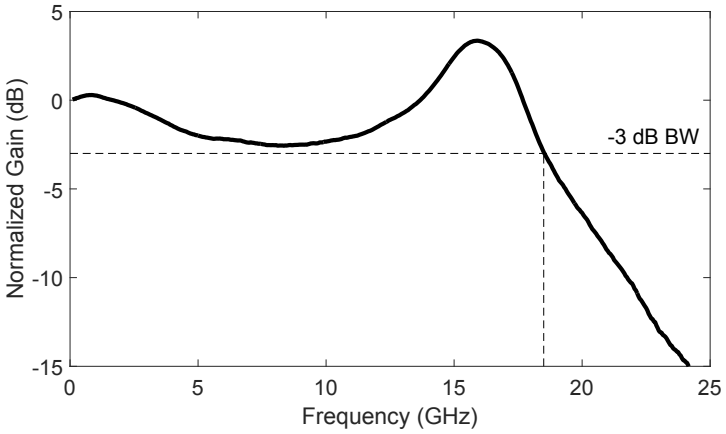


Figure 3.16: Electro-optical bandwidth measurement with normalized gain with reverse bias of 1.5 V applied to the MZM.

Fig. 3.16 shows the normalized curve obtained, where the electro-optical bandwidth is shown to be 18 GHz. As expected the electro-optical bandwidth is lower than the reported electrical bandwidth in 50-Ω measurements since in these conditions the driver has the RC of the modulator as load. The reported bandwidth curve is obtained with a reverse bias of 1.5 V, the same conditions used in the time-domain measurements in [39]. Electro-optical bandwidth was reported previously in [41], where higher peaking was observed. The measurements here performed were obtained from a new version of the chip with improved decoupling of the supplies through better distribution of the on-chip capacitors.

To demonstrate the linearity of the driver, new time-domain electro-optical measurements were performed using a higher order modulation format (PAM-4). The setup is shown in Fig. 3.23. A Keysight arbitrary waveform generator (AWG) M8195A was used at the input to generate a PAM-4 signal with PRBS7 without pre-emphasis, and a CW laser light with a wavelength of 1550 nm was injected at the optical input of the device. The fiber-to-fiber optical loss at this wavelength is 18 dB. In order to recover the signal, an erbium-doped fiber amplifier (EDFA) is utilized at the output of the transmitter, providing an optical gain of 20 dB. The optical signal is converted by a photodiode, with 50 GHz of bandwidth, connected to a sampling oscilloscope (Textronix DSA8300). It is also shown in Fig. 3.23 how the transmitter is probed on-wafer. To the input is connected a 67-GHz differential RF probe, the supplies are connected from the sides using 20-needle dc probes and a fiber-array couples the light at the optical interface, providing the CW light signal from the laser and receiving the modulated signal from the chip. Two additional single needles are used to contact the pads related to the thermal section to control the operating point of the modulator. Measuring on-wafer is an important advantage of integrating monolithically driver and modulator in a single chip, easing the testing of the electro-optical transmitter without the need of bonding and packaging.

The differential input voltage amplitude from the AWG was 600 mVpp. To operate the modulator in a linear region to deliver a modulated signal with levels equally spaced, the gain of the driver was reduced, not providing the full V_π. Hence, the ER is expected to be lower in comparison to previous measurements with OOK modulation format reported in [39, 41]. Consequently the dc power dissipation of the driver is lower (1.5 W). Fig. 3.18 presents the output optical eye-diagram at 20 Gbaud (40 Gb/s) and Fig. 3.21 at 25 Gbaud (50 Gb/s). The

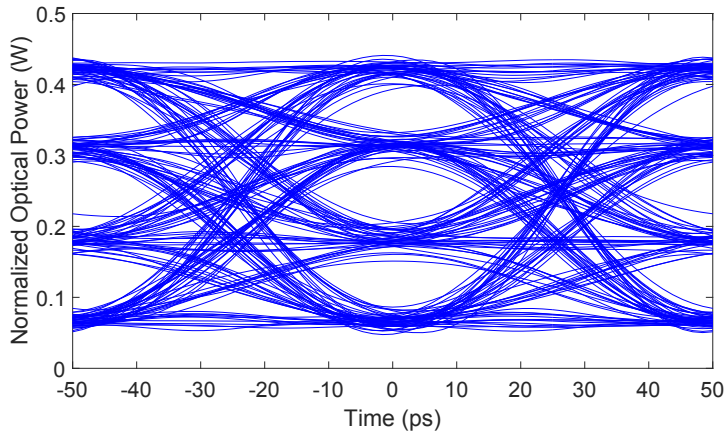


Figure 3.17: Simulated optical output eye-diagram transmitting PAM-4 signal at 20 Gbaud (40 Gb/s), using the co-simulation.

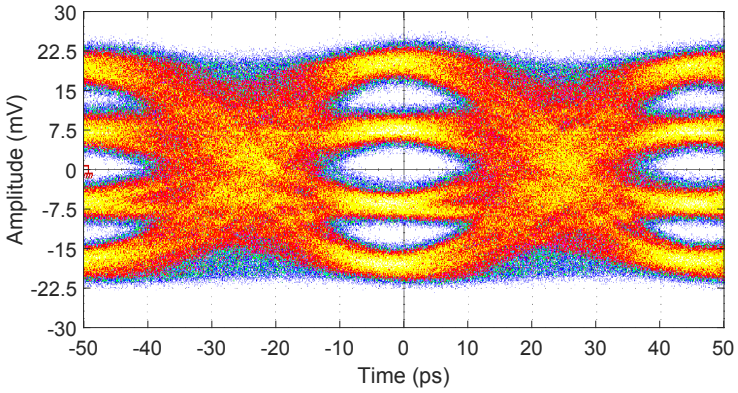


Figure 3.18: Measured optical output eye-diagram transmitting PAM-4 signal at 20 Gbaud (40 Gb/s) using 2^7-1 PRBS without pre-emphasis.

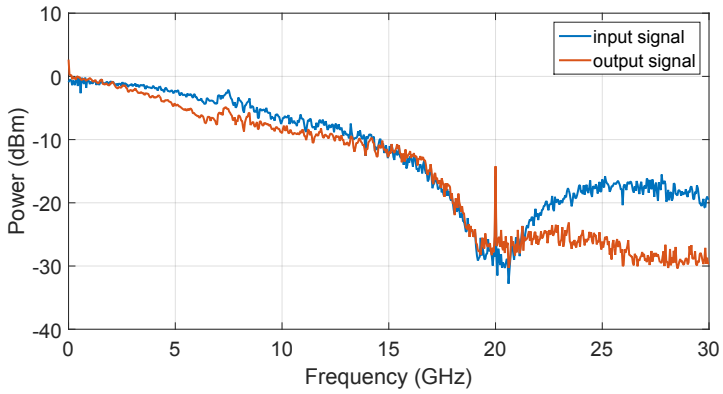


Figure 3.19: Spectrum of the optical output in a PAM-4 transmission (2^7-1 PRBS) at 20 Gbaud (40 Gb/s). The spectrum of the input signal is also plotted.

correspondent simulated eye-diagrams of the optical output using the co-simulation are plotted in Fig. 3.17 and Fig. 3.20. The measured and simulated eye-diagrams are in good agreement, proving the effectiveness of the co-simulation methodology outlined in section 2.4. With a dc power dissipation of 1.5 W for the driver, the energy per bit is 30 pJ/bit at 50 Gb/s.

In addition, the output of the photodetector was connected to a signal analyzer (Rohde & Schwarz FSV 10 Hz-30 GHz) and the spectrum of the demodulated optical signal was saved.

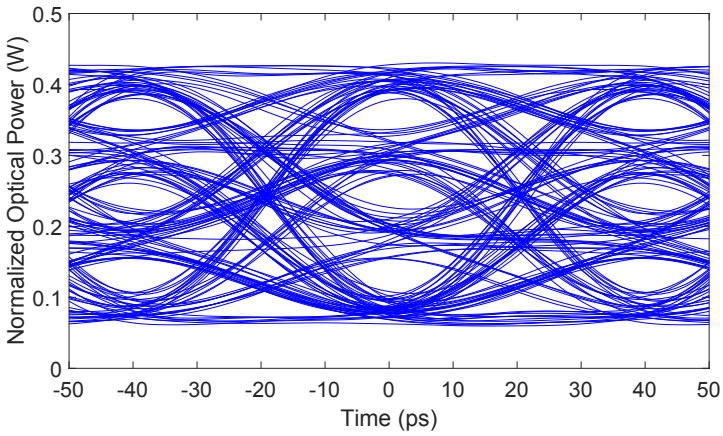


Figure 3.20: Simulated optical output eye-diagram transmitting PAM-4 signal at 25 Gbaud (50 Gb/s), using the co-simulation.

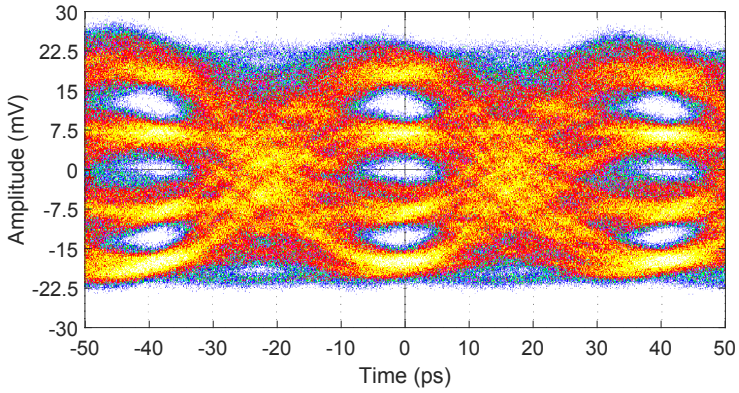


Figure 3.21: Measured optical output eye-diagram transmitting PAM-4 signal at 25 Gbaud (50 Gb/s) using 2^7-1 PRBS without pre-emphasis.

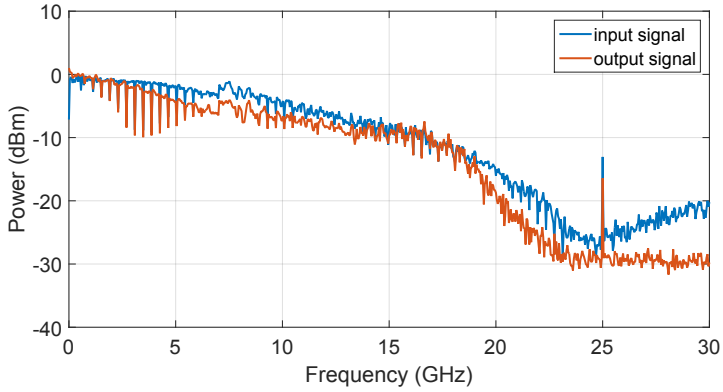


Figure 3.22: Spectrum of the optical output in a PAM-4 transmission (2^7-1 PRBS) at 25 Gbaud (50 Gb/s). The spectrum of the input signal is also plotted.

Fig. 3.19 and Fig. 3.22 present the results of these measurements at 20 Gbaud and 25 Gbaud. The spectrum of the input signal from the AWG was also saved using the signal analyzer. The input signals are plotted in the same figures and all power values are normalized for comparison. As expected, due to the non-flat response of the transmitter (Fig. 3.16), the signal is slightly degraded. The peaking observed in the electro-optical bandwidth measurement at 16 GHz helps recovering the signal power around this frequency. On the contrary, due to the

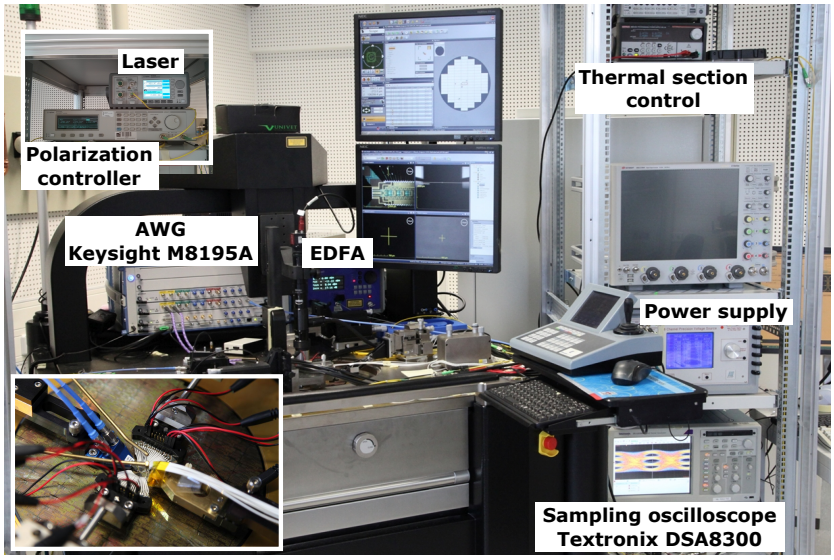


Figure 3.23: Experimental electro-optical setup for on-wafer PAM measurements using an AWG at the input. A magnified picture of the probing is also shown in the bottom-left corner.

reported less gain between 5 and 12 GHz, it can be observed in the spectra that the power of the output signal drops in comparison to the input signal. Overall the output signal is not significantly distorted due to the non-flat response of the transmitter.

A spurious-free dynamic range (SFDR) experiment was also performed. A 1 GHz sine was generated by the AWG and connected to the input of the transmitter. The output of the photodetector was connected to the signal analyzer used in the previous spectrum measurement. A difference of 33 dB between the fundamental and the second harmonic was observed, resulting in a SFDR value of 33 dBc. The overall linearity of the transmitter is affected by the nonlinear curve of the MZM. This is the main motivation for the inclusion of a linear driver in the subsystem, enabling compatibility with an external DAC to apply pre-emphasis and post-correction in a real application.

Electro-optical measurements were carried out at room temperature. Si modulators are considered more robust in temperature drifts when compared to other technologies; therefore an accurate control of the device temperature was not required in the setup.

3.1.3 Performance Comparison

As reported in [39], the proposed transmitter shows the highest extinction ratio (13 dB) at 28 Gb/s when compared to other state-of-the-art silicon solutions [49, 26, 50]. The key feature enabling this result is the usage of a segmented driver with a long MZM concept, which unfortunately comes at the expense of increased power dissipation. Table 3.1 summarizes the state-of-the-art comparison in Si optical transmitters. In terms of the data-rate, with the here demonstrated PAM-4 measurements, the proposed monolithic transmitter is in-line to the state-of-the-art [26, 25, 50], achieving data-rate up to 50 Gb/s. The different cited works make use of different implementation approaches. In [50], the modulator features a similar efficiency value than the one reported here, but shorter length is used, demonstrating high-speed OOK transmission at low value of ER. In [25], a different MZM is used (SISCAP) which has state-of-the-art efficiency which allows for a reduction of the phase-shifters length,

Table 3.1: Comparison of State-of-the-art Si Optical Transmitters

Ref.	[49]	[26]	[50]	[25]	**This work**
Technology	90 nm CMOS	90 nm CMOS	0.13 µm BiCMOS	40 nm CMOS	**0.25 µm BiCMOS**
Driver Topology	Limiting	Integrated 2-bit	Limiting	Integrated 2-bit DAC	**Linear segmented**
Integration / MZM type	Monolithic / depletion	Monolithic / depletion	Hybrid / depletion	Hybrid / SISCAP	**Monolithic / depletion**
MZM $V_\pi L$ (Vcm)	1.67	1.47	4.3	0.2	**2.9**
MZM length (mm)	3	3	3.36	1	**6.08**
Wavelength (µm)	1.3	1.3	1.3	1.55	**1.55**
Driver output (Vppd)	3.4	2.2	4	1	**4***
Power dissipation (W)	0.278	0.27	0.43	0.5	**1.5**
Max. ER (dB)	10.4	6.5	2.7	-	**13***
Data-rate OOK (Gb/s)	16	25	56	-	**28***
Data-rate PAM-4 (Gb/s)	-	56	-	56	**50**

*featuring 2 W power dissipation[39].

optimizing the subsystem in terms of power dissipation. The module here presented, with a monolithically integration of the driver and modulator, has as main asset the inclusion of linear amplifiers on the driver, which enables compatibility with an external DAC to perform pre-emphasis to compensate the nonlinear transfer function of the MZM. This opens the possibility to achieve high ER with higher order modulation formats.

3.1.4 Summary

A monolithically integrated segmented linear driver and modulator in EPIC 0.25 µm SiGe:C BiCMOS technology has been reported. The chip occupies an area of 12.7 mm^2 with dimensions of 9.8 mm × 1.3 mm. Electrical measurements to demonstrate the linearity of the driver were performed, showing THD below 5%. The electrical characterization also shows gain (13 dB) and bandwidth (25 GHz) in line with the expected values from post-layout simulations. The linearity of the driver is also demonstrated performing electro-optical measurements of PAM-4 modulation format at 20 Gbaud (40 Gb/s) and 25 Gbaud (50 Gb/s). The transmitter also shows the highest extinction ratio (13 dB) at 28 Gb/s. To deliver these results in a depletion-type Si MZM, the implemented transmitter incorporates a long modulator and a segmented driver topology to apply constant voltage amplitude. The total power dissipation of the driver is 1.5 W, resulting in an energy per bit of 30 pJ/bit at 50 Gb/s. The reported optical transmitter demonstrates for the first time an implementation of a linear driver integrated with a MZM in

Figure 3.24: Cross-section PN junction.

a Si monolithic process. The next iteration of the optical transmitter aims to deliver higher electro-optical bandwidth in order to show higher data-rates.

3.2 A 112-Gb/s Segmented Linear Driver and Modulator

In this section, an improved version of the monolithically integrated optical transmitter comprising a linear driver and a MZM is described. The aim of this new design is to use new techniques to improve the performance of both driver and modulator. Reducing the equivalent electrical load of the modulator segments and using a new topology for the driver, a higher speed performance can be achieved. The second generation of the electro-optical transmitter is therefore implemented in the same EPIC 0.25 µm SiGe:C BiCMOS.

The modulator parameters are the following. The phase shifters have efficiency of 2.9 Vcm as in the previous design. The cross section of the updated design of the phase shifter is depicted in Fig.3.24. Two additional implants are now fabricated in the edges of the diode (n^{++} and p^{++}) which are more doped, resulting in a less series resistance value in the contact to the depletion region. The layers are strategically located in a distance far enough to minimize the impact on the static optical insertion loss. The reduction in the series resistance is 50% (25 Ω instead of 50 Ω per segment) and the insertion loss is increased by only 20%. Similarly to the first generation, the implemented modulator in this design has the same 6.08 mm of length, resulting in the same requirement for the delivery voltage, a minimum V_π of 4 V. This amplitude is the maximum achievable output amplitude for an ac signal in this technology due to the limitation in the biasing conditions to not surpass the breakdown voltage of the high-speed HBTs. For this length, the total capacitance for each arm of the MZM is 2.4 pF, 150 fF for each segment. The segmented configuration is followed in-line with the previous design. The improved design of the segmented driver is presented in the following.

3.2.1 Transmitter Design

A block diagram of the transmitter is shown in Fig. 3.25. The phase-shifters of the modulator are divided into 16 segments with 380 µm of length. The separation between segments is 20 µm, sufficient to create electrical isolation. To the n-side of each phase shifter segment in both arms is connected the differential output of the correspondent driver segment. A dc voltage potential is applied to the p-side of both arms, through a separated pin, setting the reverse bias voltage of the modulator together with the common-mode of the driver output. The electric equivalent of each portion of the phase shifter represents the load for the driver segments, and it is the dominant pole, determining the overall bandwidth of the transmitter. In contrast to the previous implementation, the input stage with the objective to drive the

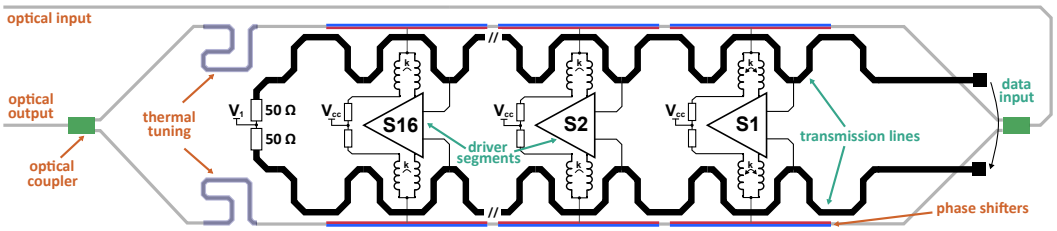


Figure 3.25: Block diagram of the second generation monolithically integrated segmented driver and MZM.

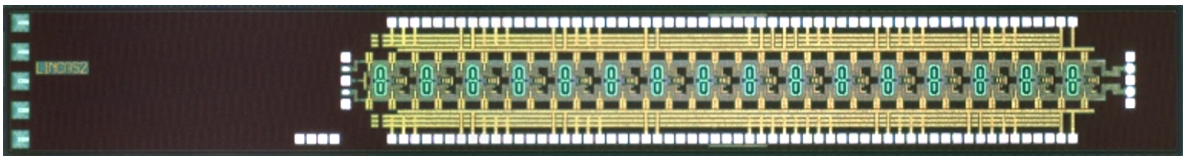


Figure 3.26: Chip microphotograph of the second generation optical transmitter.

transmission lines was not included, as an additional effort to reduce the power dissipation. Thus, the input is connected directly to the transmission lines, forcing the 50-Ω characteristic impedance. The design of the transmission lines follow a distributed amplifier topology to maximize input matching. The lines comprise a ladder network of T-sections which embed the capacitive elements from the driver segments with series inductance, terminated by 50-Ω resistors. Additionally, the designed lines also have capacitance which needs to be considered, leading to an iterative design procedure. The result is an artificial transmission line matched to the required impedance, easing the transfer of the signal power throughout the segments.

The schematic of each segment of the driver is depicted in Fig. 3.27. The differential pair follows a similar approach to the first generation, with a common-emitter amplifier with degeneration resistor and resistive current source instead of a current-mirror, allowing for a reduced supply voltage. The common-emitter differential pair though contains common-base HBTs Q5 and Q6 forming a cascode stage, to enhance the gain-bandwidth product. The collector resistor Rc has a value of 64 Ω to keep the headroom for the output swing. The T-coil comprises the inductors L1 and L2 with values of inductance of 300 pH each. The coupling factor k between the inductors is 0.3. L3 represents the series connection to each phase shifter segment, modelled by a value of 50 pH. The emitter-followers driving the output stage serve the same purpose as in the first generation of the driver, in isolating the large transistors of the output stage from the transmission lines. With the required higher supply voltage to accommodate the cascode amplifier, omitting the input stage from the first version of the design, allows to keep the power dissipation similar.

Finally, the block diagram can be compared to the chip microphotograph presented in Fig. 3.26. The monolithically integrated linear driver and modulator occupy an area of 13.5 mm^2 (10.23 mm × 1.32 mm).

3.2.2 Measurement Results

Firstly, the driver was independently characterized using the single-segment variant, taped-out separately for electrical characterization means. True differential S-parameter measurements were performed on-wafer using a Rhode & Schwarz ZVA67 Vector Network Analyzer (VNA).

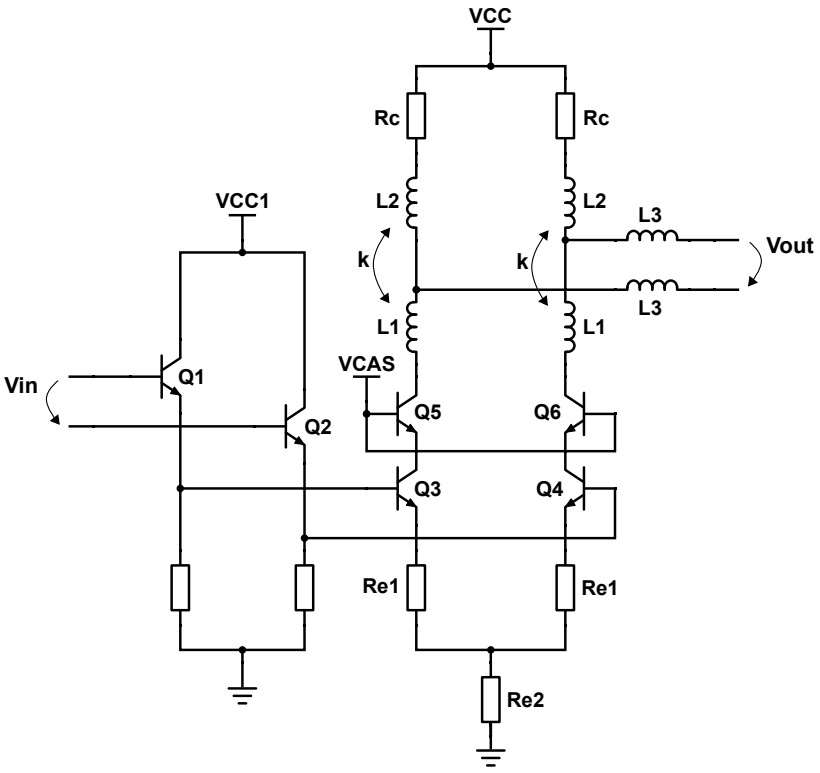


Figure 3.27: Segment schematic of the driver.

The comparison between simulated and measured S-parameters is plotted in Fig. 3.28. As expected, since the driver is not loaded with the targeted impedance (MZM segments) during S-parameter measurements, the gain falls to 6 dB. The measured 3-dB bandwidth of the driver is found to be 51 GHz, approximately doubling the speed from the previous version.

3.2.2.1 PAM-4 performance analysis with pre-distorted input

The next test, electro-optical characterization of the whole transmitter in frequency domain, was performed with a LCA Keysight N4373D with 2 electrical ports, to create the differential input, and 1 optical port, which receives the modulated signal. Fig. 3.29 shows the normalized curve obtained, where the electro-optical 3-dB bandwidth is shown to be more than 12 GHz, depending on the reverse bias change. This value is slightly lower when compared to version one, in consequence of the new T-coil implementation having less peaking in the frequency-domain. However, this design shows much better roll-off of the bandwidth curve, with a 6-dB bandwidth value being much higher, achieving more than 40 GHz. This improvement is in-line with the improvement shown in the electrical measurements. With a much smoother response, especially without the peaking at 17 GHz, the transmitter fits better with pre-distortion techniques often applied with the DAC placed at the input, to improve the output data rate of the modulated signal.

To demonstrate the speed improvement, time-domain electro-optical measurements were performed using pre-emphasis. A Keysight AWG M8195A was used at the input to generate OOK and PAM-4 signals with PRBS7. In order to recover the signal, an EDFA is utilized at the output of the transmitter, providing an optical gain of 20 dB. The optical signal is converted by a photodiode, with 50 GHz of bandwidth, connected to a sampling oscilloscope

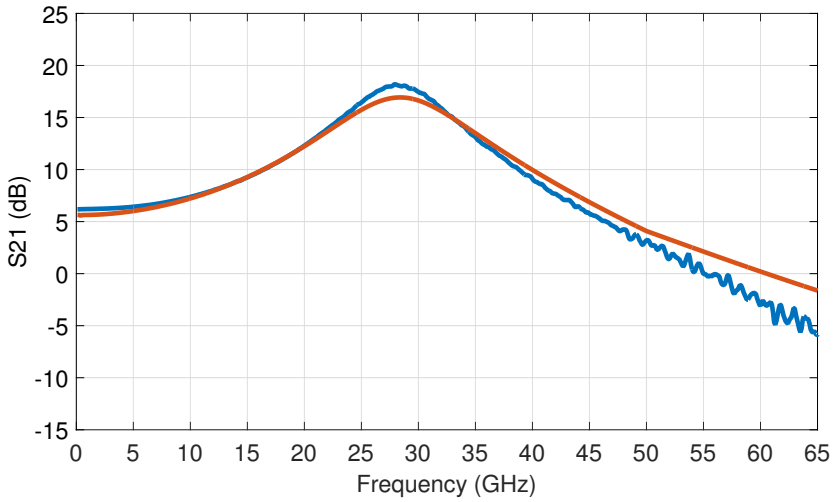


Figure 3.28: Comparison of simulated (red) and measured (blue) S21 of the driver with one segment.

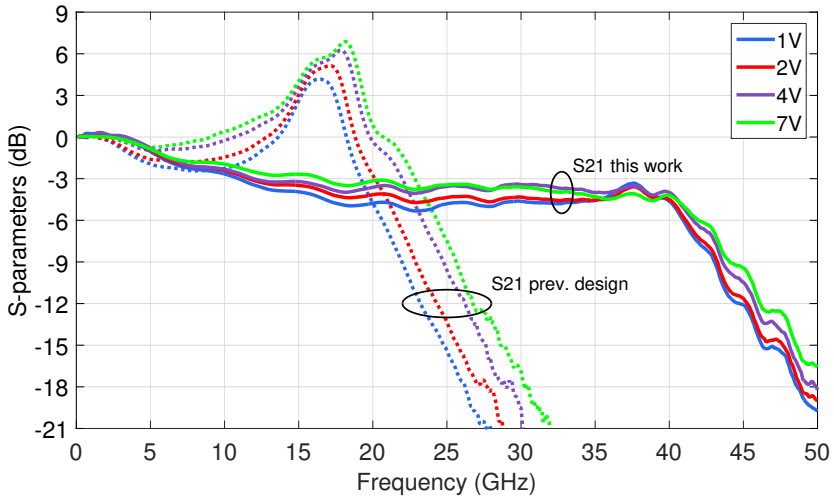


Figure 3.29: Electro-optical S-parameters measurements with normalized gain with reverse bias applied to the MZM from 1 V to 7 V.

(Textronix DSA8300). At the input a 67 GHz differential RF probe is connected, the supplies are connected from the sides using 5-needle dc probes and a fiber-array couples the light at the optical interface, providing the CW light signal from the laser with a wavelength of 1550 nm. Two additional single needles are used to contact the pads related to the thermal section to control the operating point of the modulator.

In Fig. 3.30 is depicted the results for the maximum achieved transmission with a OOK signal, 34 Gb/s. The distorted input signal created by the AWG is shown in the top-left corner. This was the maximum speed that could be measured with the available AWG, as the maximum sampling of frequency of the device is 65 Gsamples. To create the input signal the following conditions were applied: Tap #-1 2 dB, Tap #-2 1 dB, Tap #+1 -4 dB and Tap #+2 -1 dB. The minimum reverse bias is used (1 V) for maximum ER. However, the ER of the shown results is 6 dB, significantly less in comparison to the results of the first version of the driver. This is due to the limited amplitude provided by the AWG when the pre-emphasis techniques are applied. Fig. 3.31 shows the results when a PAM-4 signal is applied to the input of the transmitter. A maximum baud rate of 30 Gbaud was obtained with the distorted input signal

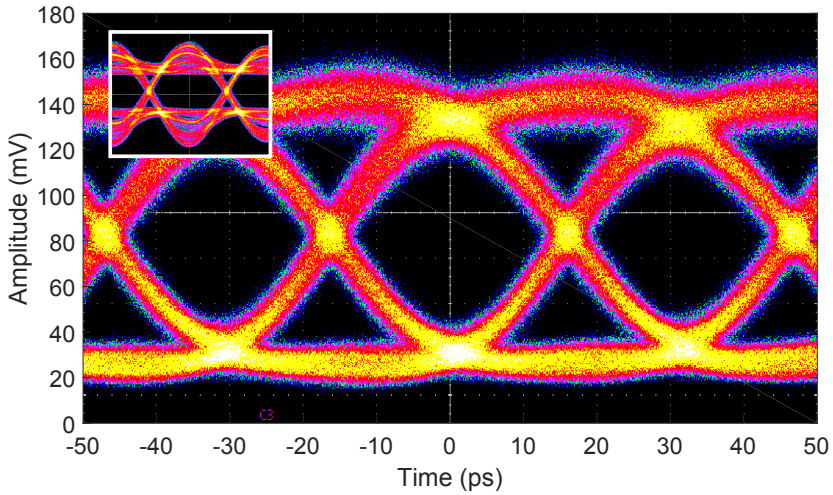


Figure 3.30: Electro-optical eye-diagram OOK 34 Gb/s. The inset shows the input eye-diagram.

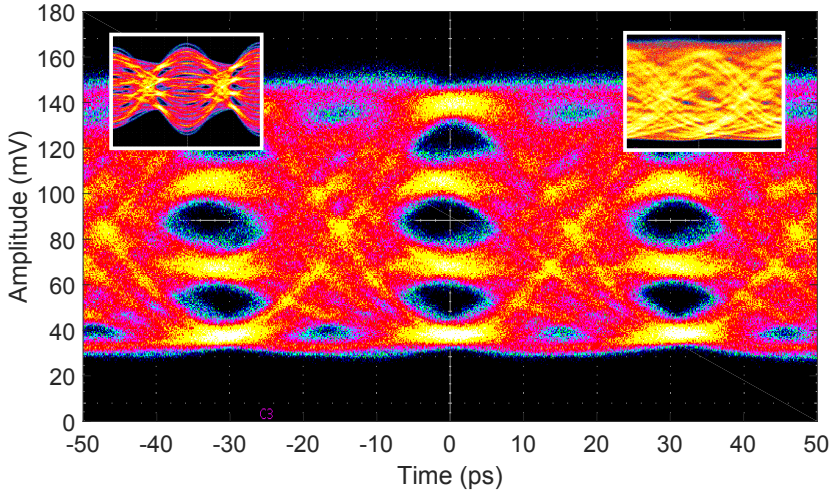


Figure 3.31: Electro-optical eye-diagram PAM-4 30 Gbaud (60 Gb/s). The top-left inset shows the input eye-diagram and the top-right inset shows the output eye-diagram without pre-emphasis.

shown at the top-left corner in the same figure. The same tap configuration as used in the OOK measurements was set in the AWG. These results are a significant improvement when compared to the results of the first version, due to the new possibility to apply pre-distortion techniques. In the first version of the transmitter this was much more difficult to achieve due to the peaking response and abrupt drop of gain after the 3-dB bandwidth.

3.2.2.2 PAM-4 performance analysis with clock recovery and feed-forward equalization (FFE)

A PAM-4 setup was prepared with a Keysight M8196A AWG with improved 32-GHz bandwidth and sampling rate of 84 GS/s, producing an 56 Gbaud (112 Gb/s) input signal with a swing set to 600 mVpp [51]. The transmitted signal was based on a gray-mapped 4-ary de-Bruijn sequence of order eight, which was resampled to 1.5 samples per symbol with raised-cosine frequency shaping (roll-off of 0.3). Subsequently, pre-emphasis was applied to compensate for the imperfections of the AWG and the connecting electrical cables. Only the electrical transmitter chain is compensated to investigate in a first step the performance of the modulator,

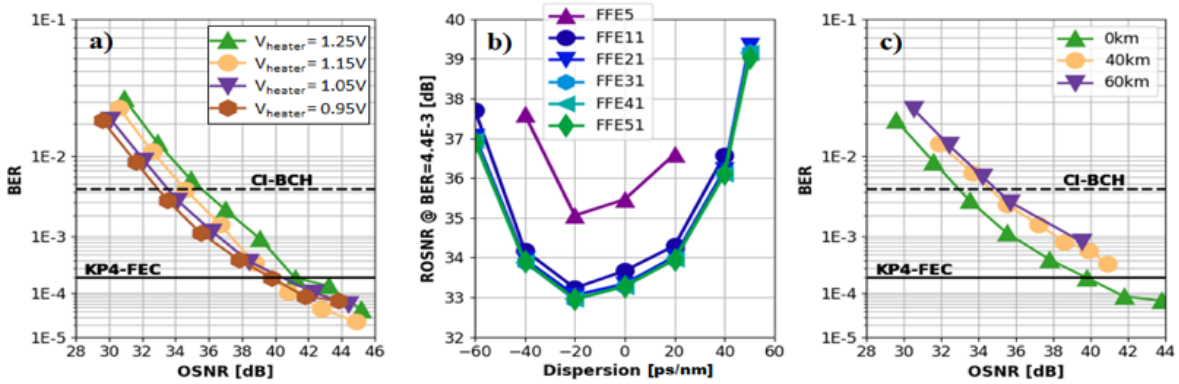


Figure 3.32: a) OSNR performance for optical b2b, b) dispersion tolerance and c) OSNR performance at different transmission distances.[51]

without manipulating its behavior using DSP. Three different optical transmission scenarios were evaluated. The first scenario included a variable optical attenuator (VOA) and an EDFA for noise loading to establish the back-to-back (b2b) OSNR tolerance. In the second scenario, a tunable dispersion compensating module (TDCM) with 100-GHz operating bandwidth was added to measure the chromatic dispersion (CD) impact on the signal. The third scenario comprised a single span of 40 km or 60 km standard single mode fiber (SSMF), a matched dispersion compensating fiber (DCF), and booster and receiver EDFAs. In all three scenarios, a MUX and a DEMUX were included at the transmitter and at the receiver with a 3-dB bandwidth of approximately 78 GHz in order to emulate the bandwidth limitations of a 100-GHz-grid dense wavelength division multiplexing (DWDM) systems. At the receiver, the optical signal power was set by a VOA to -2 dBm, and the signal was detected with a 35-GHz photodetector/transimpedance amplifier (TIA) pair. Data were captured with a 200-GS/s real-time oscilloscope (Tektronix, 40 GHz BW) and stored for offline processing. Afterwards, in the DSP, the signal was first resampled, timing recovery by means of the Gardner algorithm was applied, followed by a blind 21-tap symbol-spaced FFE based on the least mean square algorithm.

Fig. 3.32a) shows BER versus OSNR for optical b2b using different heater voltages of the modulator. The heater voltage of 1.25 V corresponds to biasing the MZM in the quadrature point. Lower voltages increase the ER at the expense of slightly asymmetric signal. With higher ER though the BER is improved for lower OSNR values. The lower heater voltage (0.95 V) is used for the next measurements. In Fig. 3.32b) is depicted the dispersion tolerance in terms of required OSNR, ROSNR, for a BER of $4.4\text{x}10^{-3}$ versus CD for different numbers of FFE taps. Using 21 filter taps (FFE21), the OSNR penalty is below 2 dB for dispersion values ranging from -45 ps/nm to 30 ps/nm. Finally, Fig. 3.32c) shows the BER vs OSNR for the distances of 40 and 60 km. For the fiber transmission cases, the optimum fiber launch power was set to 5 dBm, trading off achievable OSNR and fiber non-linearities. A successful transmission over up to 60 km with BERs below 10^{-3} and a 1.5-dB penalty between optical b2b and fiber transmission was achievable.

3.2.3 Summary

An improved monolithically integrated segmented linear driver and modulator in EPIC 0.25 µm SiGe:C BiCMOS technology has been reported in this section. This version of the transmitter occupies an area of 13.5 mm^2. Electrical measurements to demonstrate the increased bandwidth of the driver are in-line with expected values from post-layout simulations. Electro-optical measurements demonstrate an improved speed and smoother frequency response, with a combined 6-dB bandwidth of 35 GHz. The linearity of the driver is also demonstrated performing electro-optical time-domain measurements of PAM-4 modulation format up to 30 Gbaud (60 Gb/s). Moreover, a transmission over 60 km of SSMF up to 112-Gb/s and BER measured below 10^{-3} with a simple FFE-based DSP equalizer was achieved. To deliver these results in a depletion-type Si MZM, the implemented transmitter incorporates a long modulator with a segmented driver topology in which a cascode amplifier topology is included for this version. The input stage of the driver is omitted and transmission lines are designed as artificial transmission lines incorporating the parasitic capacitances of the driver segments, following a distributed amplifier manner. The total power dissipation of the driver is 2.3 W for the maximum ER.

4

Travelling-Wave Electrode Modulator Drivers

Different driving approaches have been considered for the MZM in section 2.3.1. As presented in the previous chapter, the aim to develop silicon photonics is the tight integration with electronics, low cost and packaging simplification. However, at the time of writing, silicon photonics performance is not comparable to III-V technologies yet. Additionally, the lack of optical active devices (laser, optical amplifiers, etc.) in the silicon photonics PICs limits the possibility of having a single PIC with all the components, hence the final solution has to rely on III-V chips to complete the design. Therefore, the development of drivers in SiGe for III-V modulators has very high potential, since the electronics can take advantage of the SiGe technologies and, in the photonics end, more advanced photonics technologies may be used. In this chapter, different drivers are investigated for this hybrid integration approach.

4.1 Driver for 25 Ω TWE Mach-Zehnder Modulators

The first driver implementation is a custom design for low-impedance-type MZM [52]. TWE-MZMs typically employ integrated transmission lines with characteristic impedance and termination loads. The termination is normally compatible with 50 Ω-environment, which translates to a differential 100 Ω-load seen by the driver. However, for high-speed MZMs, a key-limiting factor is the electrical insertion loss, as the length of such modulators is typically in the range of several millimeters in order to achieve a V_π low enough to be derivable by the driver. Consequently, MZMs based on 25-Ω transmission lines have been considered [53]. Lower transmission line characteristic impedance leads to wider lines, consequently with lower skin-effect losses, improving the electro-optical bandwidth of the MZM.

The design of the driver, however, has to be adapted to the new input impedance, requiring more driving current capability and therefore dissipating more power, in comparison to conventional 50-Ω designs, to deliver the same output swing. The purpose of this work is to present a low-power solution capable of driving 25-Ω TWE TWE-MZMs up to 40 Gb/s data

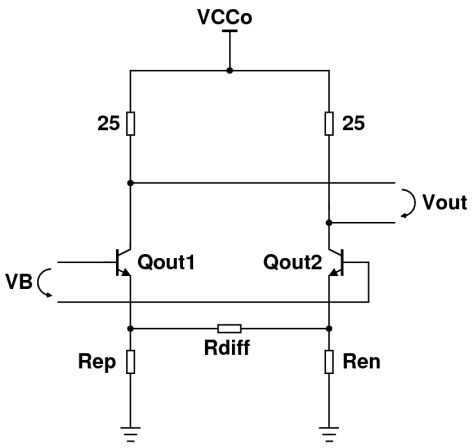


Figure 4.1: Detailed schematic of the driver output stage.

rate. The driver is implemented in the 0.13 µm SiGe:C BiCMOS technology of IHP, SG13S, with f_T / f_{max} = 250/340 GHz.

4.1.1 Modulator Driver Implementation

The circuit integrates two stages. The input stage is matched at the input to 50 Ω and it drives the output stage as well as incorporates an automatic control for the biasing of the output stage. The output stage is the main stage for signal amplification and its output is matched to 25 Ω.

4.1.1.1 Output stage

The schematic for this stage is given in Fig. 4.1. It consists of a differential pair with 12 dB of gain. For broadband matching at the output, 25-Ω collector resistors are utilized. For the desired output differential amplitude of 4 Vpp, the peak amplitude is 1 V in each arm and, for ac, the load resistance seen by the amplifier is 12.5 Ω. Therefore, the minimum necessary dc current for the signal excursion for each arm is in the range of 80 mA.

Such high dc current leads to higher dc power consumption when compared to 50-Ω designs. The fact of having the current and resistors fixed, respectively for voltage swing and output matching, the reduction of the supply voltage is the only way to overcome the increased additional power consumption.

Based on the value of the dc current deduced before, the output common-mode (CM) will be approximately 2 V down from VCC. Including additionally 1 V for the lower peak of the signal, the minimum collector voltage in operation will be in the range of $VCC - 3V$. This is also the value defined for the HBTs (Qout1,2) base voltage. Down from the transistor base, no current-mirrors were incorporated. In this way, it was possible to further shrink the supply voltage. To preserve differential operation, a resistor between the two arms was added (Rdiff). The CMRR of this stage was aggravated, however a differential pair incorporated in the input stage improves the total CMRR of the circuit.

Degeneration resistors (Rep,n) were maintained to fix the gain at 12 dB, with a small voltage drop across them of 250 mV. These resistors also improve the linearity of the driver. Since the current source was eliminated, another method for the biasing of this stage was

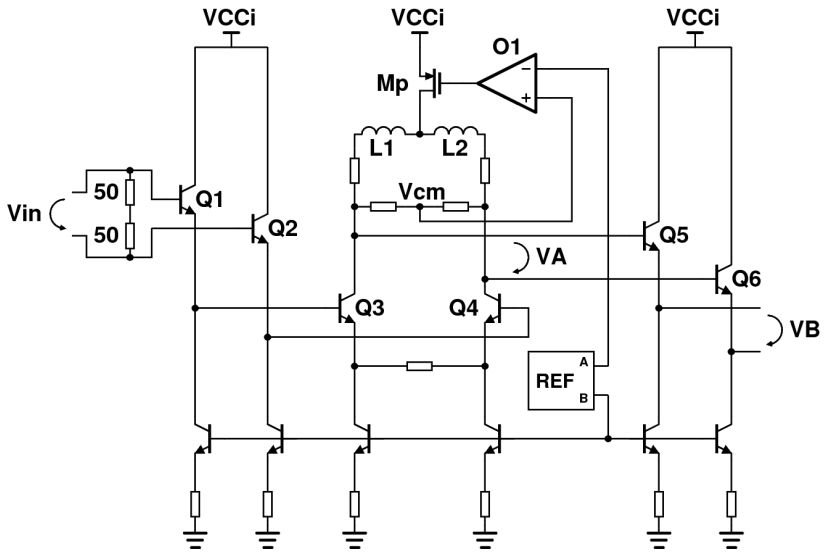


Figure 4.2: Detailed schematic of the driver input stage.

required. By placing resistors in the differential pair emitters, the bias current is now hardly dependent on the dc voltage of the HBTs base. The control of this voltage is automatically done through a low frequency feedback loop incorporated in the input stage.

4.1.1.2 Input stage

In Fig. 4.2 the schematic of this stage is presented. First, the input signal encounters two 50-Ω resistors for input matching. To drive the signal to a differential pair, the circuit begins with a small buffer (emitter-followers Q1 and Q2). In this way, the parasitic capacitance seen by the input signal is lower, and the input pole is shifted to high frequency, having less impact on the bandwidth.

The differential pair (Q3,4) has two main functions. First, it provides adequate CMRR for the input differential signal. Second, the output common-mode voltage of the differential pair (Vcm) is isolated from its input common-mode. This is an advantage for using Vcm to control the required biasing of the output stage.

To regulate the biasing of the output stage, it was defined that the CM voltage value (VB) of the output stage transistors base (Qout1,2) has the same value of the base voltage of the current-mirrors of the input stage (reference voltage B). In this way, the bias current for the output stage will be a scaled value (according to the size of the transistors) from the reference positioned in the input stage.

With an emitter-follower (Q5,6) in between the input differential pair and the output stage, Vcm is given by:

$$Vcm = V_{Rep,n} + Vbe_{Qout1,2} + Vbe_{Q5,6} \tag{4.1}$$

To fix such voltage at that point, a LDO voltage regulator was utilized. An OpAmp senses the Vcm of the differential pair, compares with a reference that produces the desired voltage deduced in 4.1 (reference voltage A) and, through negative feedback, forces the PMOS (Mp) to supply the required current to balance both OpAmp inputs.

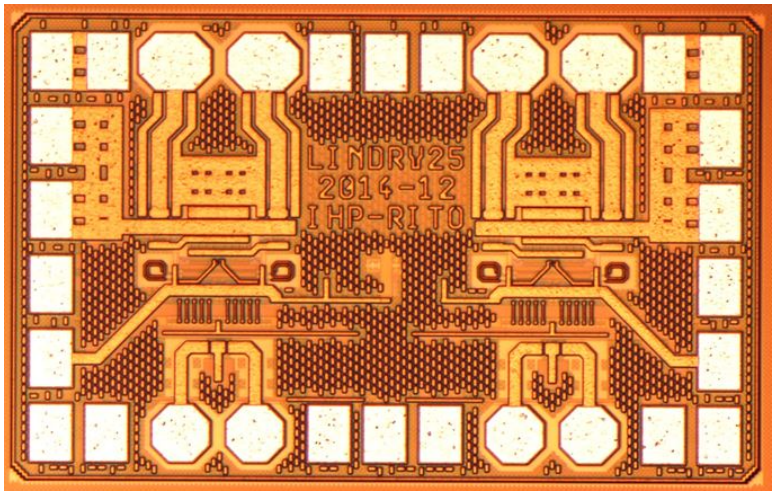


Figure 4.3: Microphotograph of the chip.

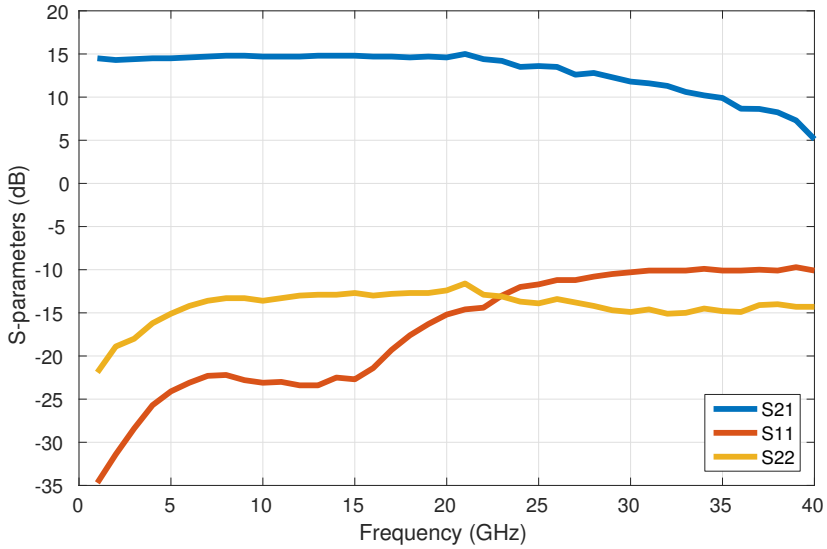


Figure 4.4: S-parameter measurements of the linear driver for 25-Ω MZMs.

The size of all transistors was chosen in such a way that as we move from the beginning of the circuit to the end, the size of the transistors increases by a factor between 2 and 3, so that the bandwidth at any point of the circuit is not lower than the specification. Still, at the output of the differential pair, due to the large size of the PMOS (Mp), inductive peaking was required in order to enhance the bandwidth (L1 and L2).

4.1.2 Measurement Results

The chip microphotograph is presented in Fig. 4.3. The entire IQ modulator driver occupies an area of 0.54 mm^2. The IC here characterized is an improved version of the one published in [52]. The circuit has two different supply voltages, VCCi is 2.7 V and VCCo is 4.7 V. The total power consumption is 2.2 W, 1.1 W per channel. The measured S-parameters (S21, S11 and S22 converted to 25-Ω environment) are plotted in Fig. 4.4. True-differential S-parameter measurements were performed on-wafer using a Rhode & Schwarz ZVA67 VNA. The measured 3-dB bandwidth was found to be 30 GHz. The measured output return loss is more than 10 dB

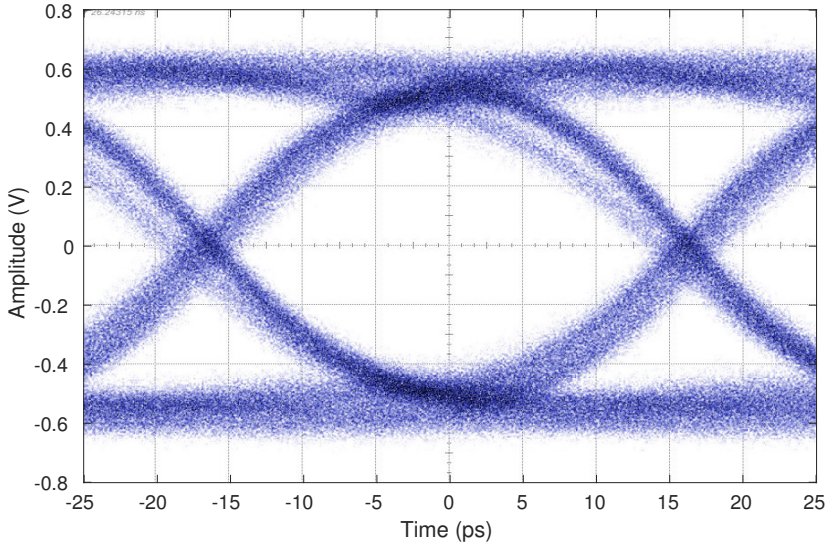


Figure 4.5: Differential output eye-diagram at 32 Gb/s. Signal is attenuated by 10 dB at the input of the oscilloscope. Input amplitude is limited to 1.2 Vppd.

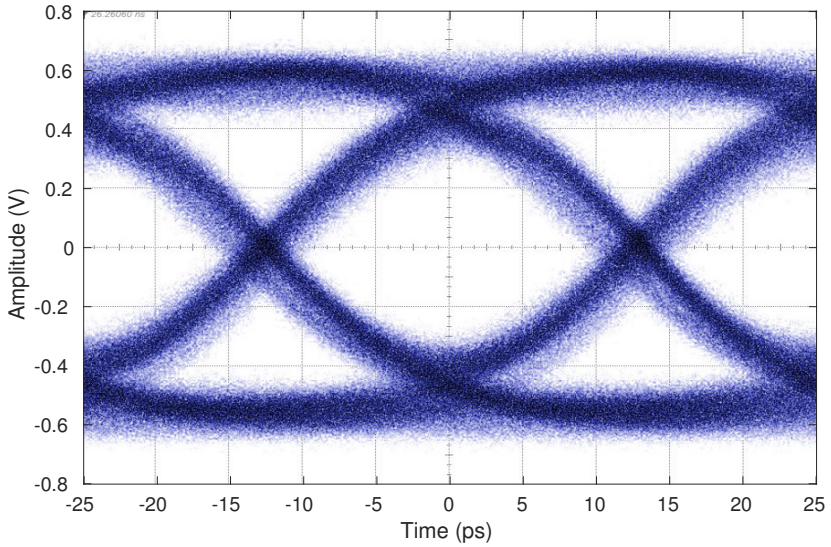


Figure 4.6: Differential output eye-diagram at 40 Gb/s. Signal is attenuated by 10 dB at the input of the oscilloscope. Input amplitude is limited to 1.2 Vppd.

in the frequencies of interest, providing a good matching between the driver and the 25-Ω modulator. Magnitude of S11 shows an input return loss better than 10 dB up to 40 GHz.

Fig. 4.5 shows the eye-diagram measurements of one of the differential outputs of the IC at 32 Gb/s. Due to equipment limitation, only 1.2 Vpp of differential amplitude at the input was used. The output signal is attenuated by 10 dB into the oscilloscope connection. Fig. 4.6 demonstrates the output eye-diagram at maximum speed of 40 Gb/s. The time-domain measurements are performed in a 50-Ω environment setup.

Table 4.1 compares the implemented design in this work to other published modulator drivers for 40 Gb/s. The power efficiency of the driver was used as a figure of merit, calculated as the ratio between the delivered output power and the dc power dissipation. Compared to the state-of-the-art, the presented MZM driver shows an improved efficiency.

Table 4.1: Comparison of State-of-the-art SiGe High-voltage 40 Gb/s Modulator Drivers

Ref.	Technology	AC Gain (dB)	f_{-3dB} (GHz)	Diff Output swing (Vpp)	DC Power consumption (W)	Load (Ω)	Output power / DC power ratio
[54]	80-GHz HBT	13.6	32.2	3	1.13	50	1%
[55]	0.18 µm BiCMOS HV-HBT	36	22	7.2	3.6	75	1.2%
[43]	0.25 µm 180-GHz BiCMOS	13	33.7	6	1.33	50	3.4%
This work	**0.13 µm SiGe BiCMOS**	**14.5**	**30**	**4**	**1.1**	**25**	**3.6%**

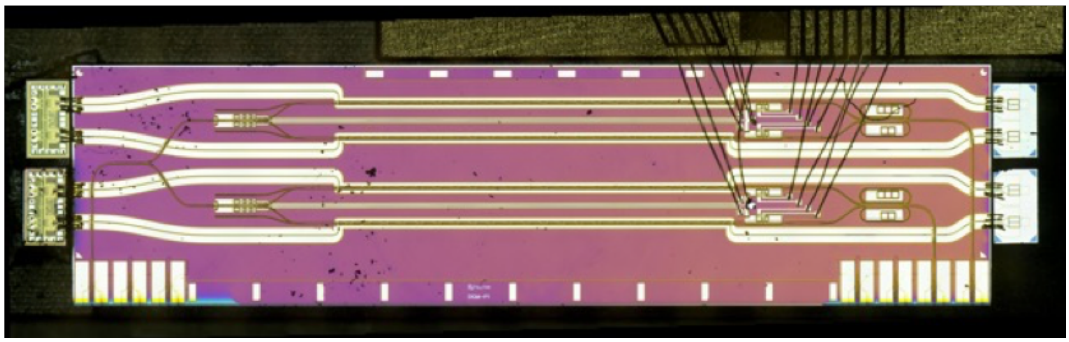


Figure 4.7: Electro-optical module comprising two 25-Ω IQ drivers and a dual-IQ optical modulator.

4.1.3 Electro-Optical Module

Thereafter, a module was assembled to demonstrate a test case of an electro-optical transmitter using the design of this driver in a 25-Ω environment. The final configuration is a dual-IQ modulator, requiring two 25-Ω IQ drivers. Fig. 4.7 displays the final assembly of the dual-IQ transmitter module. On the left part, two drivers are located which are wire-bonded to the PIC and on the right side two additional chips are also attached to provide the resistive terminations for the modulators.

Electro-optical measurements in time-domain were performed to demonstrate the performance of the assembly. Fig 4.8 shows an eye-diagram of the optical magnitude at the output of one of the IQ modulator arms. The generated signal is a QPSK signal at 25 Gbaud.

4.1.4 Summary

A high-voltage modulator driver in 0.13 µm SiGe:C BiCMOS technology has been described. The proposed design is a custom solution suitable for 25-Ω TWE-MZMs. In order to overcome the additional power dissipation due to the lower load impedance, keeping a linear topology, a strategy that can reduce the supply voltage was described. The total power dissipation is

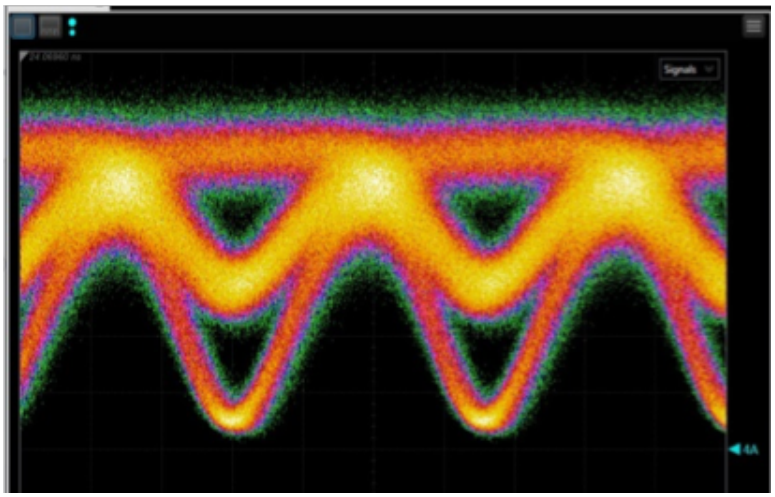


Figure 4.8: Optical magnitude at the output of one of the IQ modulator arms of the generated QPSK signal at 25 Gbaud.

1.1 W per channel, resulting in superior power efficiency in comparison with other 40 Gb/s modulator drivers. The results show 30 GHz of bandwidth in small-signal frequency-domain measurements and an operation up to 40 Gb/s in large-signal time-domain measurements. The integration of the two channels in the same chip occupies a area of 0.54 mm^2 including pads.

4.2 Driver with High Efficiency in a Complementary SiGe:C BiCMOS Technology

As observed in the other implementations of drivers in this thesis, these ICs for optical modulators dissipate a considerable high amount of power, due to the required high voltages to be delivered. Furthermore, the circuit must be designed with broadband techniques such as resistive matching, dissipating large amounts of power, reducing the power efficiency values of the complete transmitter. Technology platforms with bipolar transistors are highly desirable for the implementation of such modulator drivers due to the good tradeoff between high breakdown voltages and achievable speeds. However, BiCMOS technologies do not typically provide a pnp HBT that would make possible to implement more efficient switching amplifiers topologies similar to the ones used in CMOS in topologies of limiting amplifiers. Thus, the availability of a high-speed complementary bipolar technology with pnp and npn HBTs with matched performance offers new opportunities in power consumption optimization [56]. An example of usage of a complementary BiCMOS technology was reported in [57] where a power amplifier for 7.5 GHz signals was demonstrated.

The purpose of this investigation is to design a highly efficient driver making use of the npn together with pnp transistors, with the output stage designed according to an H-bridge switching amplifier topology. The driver implemented in the 0.25 µm SiGe:C complementary BiCMOS technology of IHP, SG25H3P, with f_T/f_{max} of 110/180GHz for the npn and 95/140 GHz for the pnp transistor is described in the following.

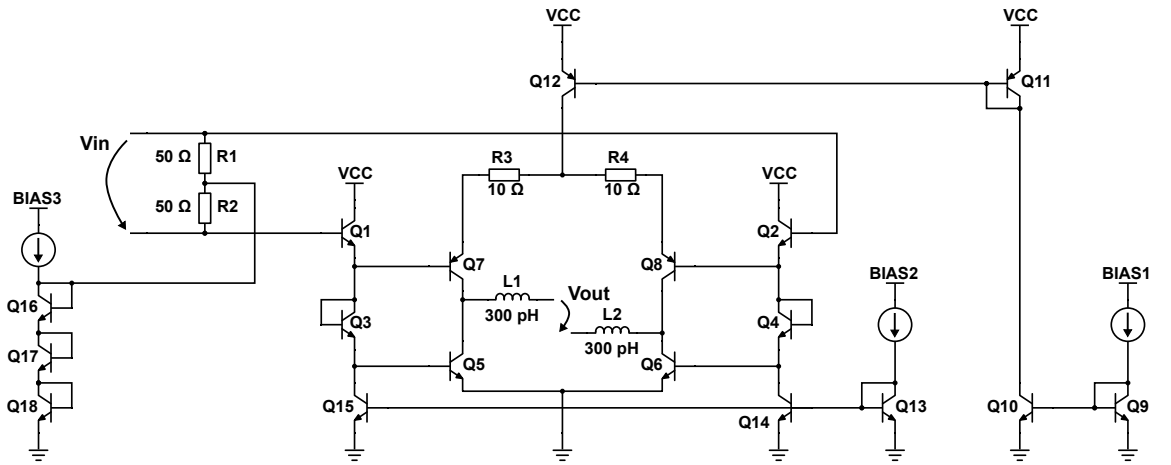


Figure 4.9: Circuit schematic.

4.2.1 Circuit Design

The circuit schematic of the differential driver is depicted in Fig.4.9 [58]. The circuit comprises two stages: an input buffer and an output stage. Additionally, the driver includes circuitry for biasing purposes.

Firstly, there are two 50-Ω resistors (R1, R2) for input matching. Between these resistors, the common-voltage for the input signal is applied. This voltage is produced as the result of the three diode connected npn transistors (Q16-Q18) in series, which have a comparable drop voltage of the subsequent stages (3Vbe). This voltage can be slightly tuned by "BIAS3" pin. The emitter-followers with npn HBTs (Q1, Q2) drive the signal to the output stage. These transistors are sized in order to provide enough driving capability for the pnp (Q7, Q8) and npn (Q5, Q6) transistors of the output stage. Due to this requirement, the power dissipation of the emitter-followers is however 60% of the total power dissipation of the driver, which makes it an important stage to optimize the design tradeoff in terms of speed and power efficiency. Diode-connected transistors (Q3, Q4) are placed in series between the output of the emitter follower and the npn transistors of the output stage, to provide different dc voltage for the transistors of different type at the output stage, in order to leave enough headroom for the targeted output amplitude of 3 Vppd.

The output stage comprises two npn (Q5, Q6) and two pnp (Q7, Q8) transistors. Only one pair of an npn and a pnp is conducting at a time. For instance, when the input signal is positive at Q2 and negative at Q1, Q5 and Q8 are in cut off and Q6 and Q7 are in saturation. In this case, the current from the current mirror Q12 flows through Q7, Q6 and the load, resulting in a drop of 1.5 V on the load. This results in a differential voltage swing of 3 Vpp. This topology is usually referred to as an H-bridge driver. It is the first time that such topology is designed for a high speed driver for optical modulators. This topology can provide better power efficiencies than CMOS drivers, as HBTs have higher transconductance, making them more suitable for such amplifiers. Few challenges in the design limit the circuit of achieving even higher power efficiencies. Firstly, as referred before, emitter followers at the input are required, dissipating a considerable amount of current needed to drive the output stage. Secondly, in order to properly bias the npn and pnp transistors independently at the output stage, a current mirror

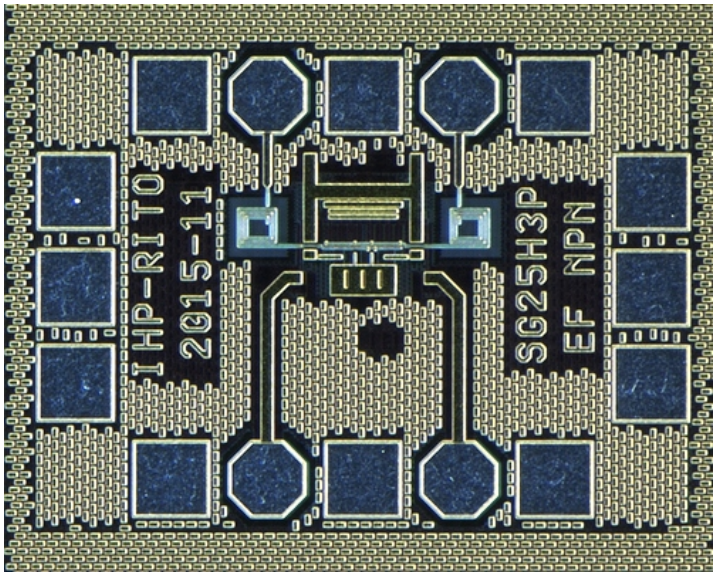


Figure 4.10: Chip microphotograph.

(Q12) had to be implemented. This increases the supply voltage, also worsening the efficiency. This current mirror is used to set the bias current of both types of transistors. In the case of the npn HBTs, the operating point is also dependent on the applied voltage through the input common-mode and the bias current of the emitter follower. Thus, small adjustment can be done to guarantee the best performance of the driver in terms of eye diagram symmetry and achievable speeds. In summary, the external voltage pins that are used to control the output stage bias point are the following: "BIAS" controls the output stage current; "BIAS2" the current of the emitter-followers; and "BIAS3" the common-mode voltage at the input. Degeneration resistors (R3, R4) were used at the emitter of the pnp HBTs to better equalize the eye diagram quality in terms of symmetry. Inductors (L1, L2) in series to the output, with inductance of 300 pH, were included to enhance the driver speed performance.

The chip microphotograph is presented in Fig. 4.10 occupying an area of 0.35 mm^2. The total power dissipation of the IC when driving a data rate of 28 Gb/s is 175 mW with a supply of 3.5 V. The output stage only dissipates 70 mW.

4.2.2 Measurement Results

To demonstrate the performance of the driver, time domain measurements were performed. A bit pattern generator (BPG) was used at the input to generate a PRBS31 signal. The differential input voltage amplitude was 600 mVpp. At the output, the signal was attenuated by 9 dB and connected to a sampling oscilloscope (Keysight DCA X 86100D) with the capability of measuring differential eye diagrams using skew calibration. Fig. 4.11 presents the output signal at 25 Gb/s and Fig. 4.12 at 28 Gb/s. The output amplitude is found to be 3 Vppd, representing an output power to power dissipation ratio of 6.4%.

Table 4.2 shows a comparison of this implementation with other recently published drivers. When compared to prior bipolar implementations, this work outperforms in terms of efficiency, having almost the double output power to power dissipation ratio. However, it has lower data rate, due to the limitation on f_T. Even when comparing with other state of the-art drivers

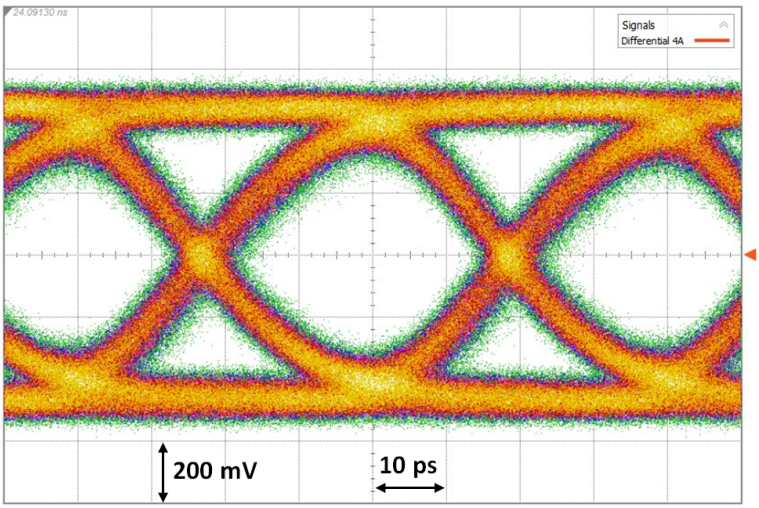


Figure 4.11: Measured differential eye-diagram at 25 Gb/s.

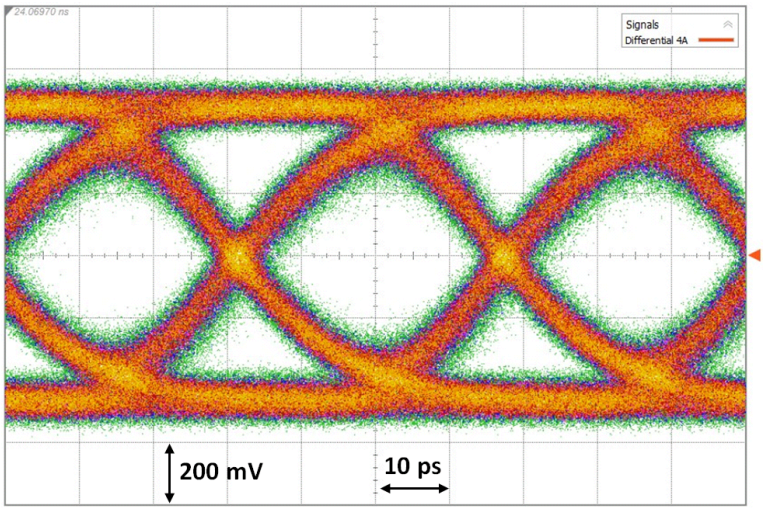


Figure 4.12: Measured differential eye-diagram at 28 Gb/s.

in CMOS technologies, the presented H-bridge driver has also higher efficiency, and has the highest data rate, except for [59], which uses a more advanced SOI CMOS technology.

4.2.3 Summary

A high-voltage modulator driver fabricated in the 0.25-µm SiGe:C complementary BiCMOS technology of IHP has been described in this section. The total power dissipation of the IC is 175 mW. At the time of writing, the proposed design has the highest ratio of output power to power dissipation in comparison to other state-of-the-art driver implementations at comparable data rates. Such high power efficiency has been achieved by implementing an H-bridge topology taking advantage of the availability of the pnp HBTs in the technology used in this design. Time-domain measurements were performed to demonstrate operation up to 28 Gb/s and output amplitude of 3 Vppd. The chip occupies an area of 0.35 mm^2 including pads. The proposed BiCMOS IC is suitable to drive optical modulators compatible with 50-Ω, requiring power efficient drivers, such as the case of the TWE-MZMs for two-level amplitude transmissions as OOK or QPSK.

Table 4.2: Comparison of State-of-the-art Low-power Optical Drivers

Ref.	Technology	f_T (GHz)	Data-rate (Gb/s)	Diff Output Amp. (Vpp)	Power (W)	Output power / power dissipation ratio
[43]	0.25 µm BiCMOS	180	40	6	1.35	3.3%
[52]	0.13 µm BiCMOS	250	40	4*	1.1	3.6%
[60]	130 nm CMOS	-	20	3.4	0.312	4.6%
[26]	90 nm CMOS	-	25	2.2	0.135	4.5%
[59]	45 nm CMOS	-	40	4.5	0.437	5.7%
This work	**0.25 µm comp. BiCMOS**	**110 (npn) 95 (pnp)**	**28**	**3**	**0.175**	**6.4%**

*driving a 25-Ω load.

4.3 PAM-4 Driver for Optical Modulators

One possible way of increasing the transmission capacity is to add more lanes in parallel in the transmitter, using wavelength division multiplexing (WDM) [61]. However, available physical area which can dissipate the heat is one of the fundamental limitations in such subsystems. Therefore, the development of transmitters with higher baseband data rate performance becomes essential. Moreover, with the progress in advanced DSP algorithms, the implementation of multilevel coded transmissions at higher speeds is becoming possible [62]. The usage of multilevel signaling can reduce intersymbol interference (ISI) and crosstalk in comparison to NRZ systems which require challenging increase of bandwidth to achieve similar data rates [63]. For the next generation 400-Gb/s transmissions, the usage of signals encoded with four amplitude levels has been proposed [3], such as PAM-4.

One configuration to create PAM signals is to have the driver preceded by a DAC which generates the encoded signal. In this configuration however the overall speed of the system is reduced by the DAC, as its bandwidth is compromised by having available a large number of bits, suitable to apply pre-emphasis compensation. Another constraint of the DAC is the power dissipation which can be in the range of 2 W [64].

An alternative configuration is a custom design with the incorporation of the DAC into the driver, resulting in a single device featuring digital inputs and capable of driving large voltage amplitudes. The number of bits are selected according to the number of levels needed for the PAM encoding. Thus, linear amplification is no longer required, reducing the complexity of the driver. Moreover, at over 50 Gbaud, data retiming becomes more stringent, increasing dramatically the complexity of synchronous devices [65]. Hence, designing a less complex electrical front-end between DSP and MZM without data retiming and minimizing the number of stages turns out to be an interesting topology to achieve such high speeds without increasing power dissipation, resulting in a highly-efficient subsystem.

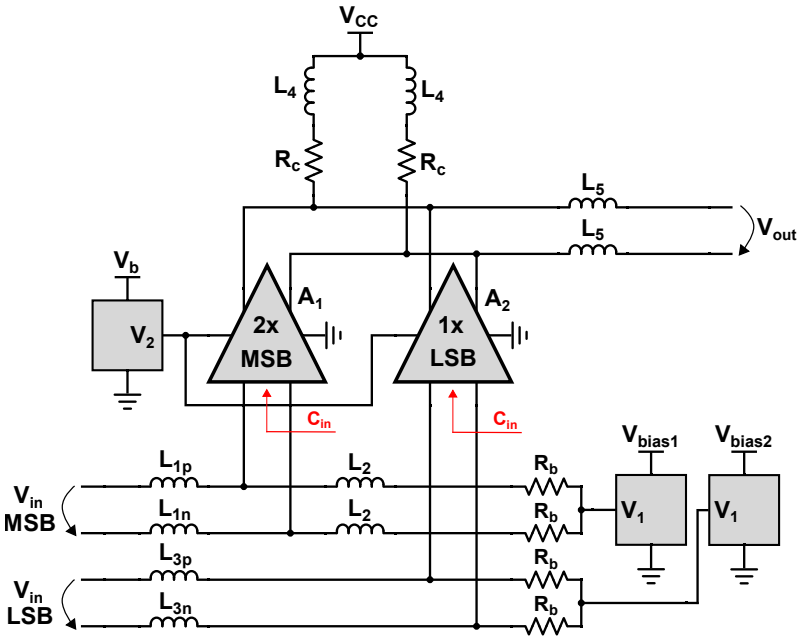


Figure 4.13: Schematic of the PAM-4 driver.

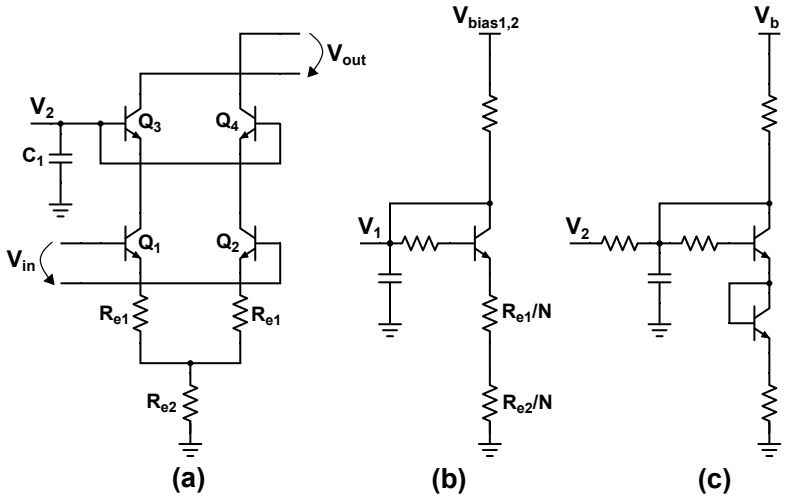


Figure 4.14: Stages schematics. a) amplifier b) input base bias and c) cascode base bias.

In this section, a driver integrating a 2-bit DAC to generate PAM-4 signals is investigated. The IC is fabricated in the fastest 0.13 µm SiGe:C BiCMOS technology of IHP, SG13G2, with f_T/f_{max} of 300/500 GHz, $BV_{CEO} = 1.7\,V$ and $BV_{CBO} = 4.8\,V$.

4.3.1 Circuit Design

The circuit schematic is depicted in Fig. 4.13 [66]. The driver consists of a current mode 2-bit DAC topology, with two gain cells in parallel. The gain cells have independent inputs correspondent to the required 2 bits (LSB and MSB) and the outputs are connected together, driving the resulting current to the collector resistors R_c. In order to reduce power dissipation, R_c and R_b have values of 60 Ω instead of 50 Ω to decrease the required collector current for the targeted output amplitude. This discrepancy does not produce significant matching deviation, as it affects only the lower frequency range. At the output, R_c in parallel with the 50-Ω

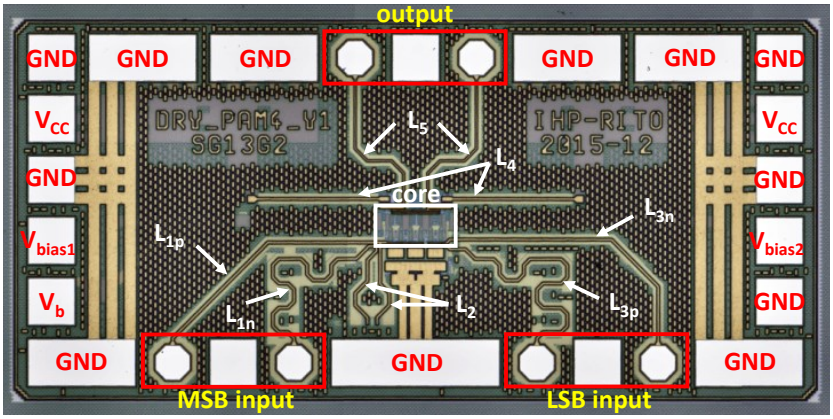


Figure 4.15: Chip microphotograph.

Table 4.3: PAM-4 Driver Circuit Design Parameters

Component	Value	Length	Group delay
L_{1p}, L_{1n}	190 pH	390 µm	3 ps
L_2	75 pH	150 µm	-
L_{3p}, L_{3n}	220 pH	470 µm	3 ps
L_4	100 pH	200 µm	-
L_5	140 pH	275 µm	2 ps
A_1	-	-	8 ps
A_2	-	-	8 ps
R_b	60 Ω	-	-
R_c	60 Ω	-	-

equivalent load, translates into a collector resistance of 27.3 Ω, seen from both amplifier cells. To guarantee enough headroom in the equivalent output resistance for an output voltage swing of 4 Vppd (1 V peak single-ended), the circuit is biased with 37.5-mA collector current in each R_c, which results in a total current consumption of 75 mA. To produce a 4-level output signal, the gain cells are weighted in a ratio of 1:2 between the LSB gain cell and the MSB gain cell, therefore corresponding to 25 mA and 50 mA of current for each amplifier.

A cascode topology was chosen for the implementation of the two gain cells. The schematic of the amplifier is presented in Fig. 4.14. The cascode architecture increases the gain-bandwidth product and the isolation between input and output in comparison to a common-emitter amplifier. Another advantage is the possibility for higher swing voltages, since it is BV_{CBO} limited and not by BV_{CEO}. Finally, the input capacitance (C_{in}) is smaller due to the unitary common-emitter gain in Q_1 and Q_2, reducing the Miller-effect. The latest point has high relevance in the design of this driver, since the design target was to keep the driver with only one stage to have the signal travelling through the minimum number of stages. Higher RF complexity would lead to the requirement of signal retiming with flip-flops and clock distribution, increasing even more the complexity of the circuit and the power consumption. For a flat gain curve response, degeneration resistors (R_{e1}) are included. Resistor R_{e2} is the current-source of the amplifier and enhances the CMRR. Resistors R_{e1} determine the gain value of each gain cell, consequently R_{e1} in the LSB cell has double value (half gain) in comparison

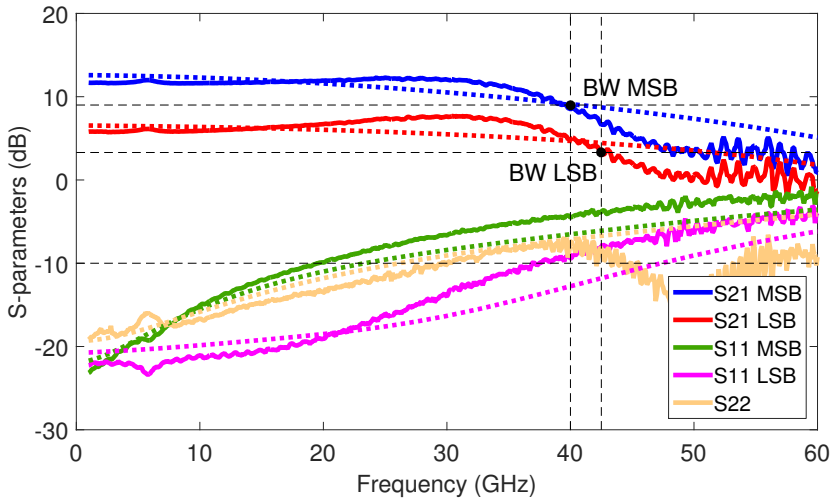


Figure 4.16: S-parameters results (gain and return loss). Comparison between post-layout simulation (dashed) and measurements (solid).

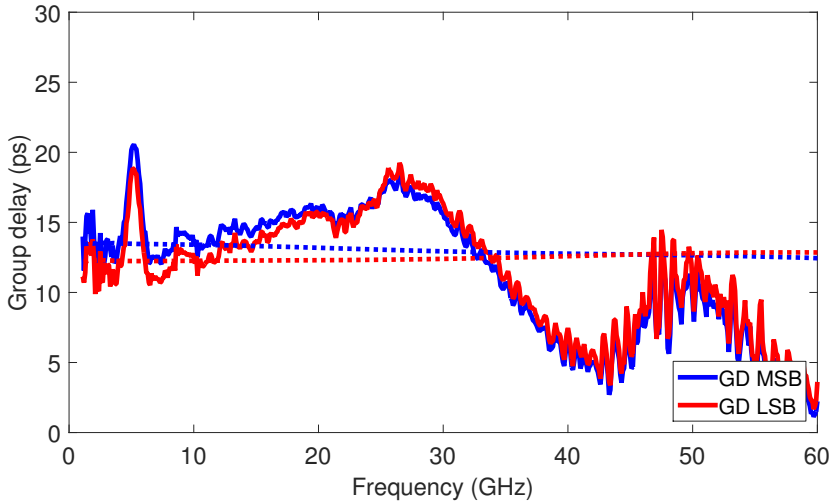


Figure 4.17: S-parameters results (group delay). Comparison between post-layout simulation (dashed) and measurements (solid).

to the MSB cell. The capacitor C_1, located at the base of the cascode transistor (Q_3, Q_4), ensures an AC-ground for the high-frequencies.

Even though the cascode amplifier relaxes the input capacitance C_{in}, the high collector currents require large transistors which create significant parasitic capacitance due to the base-emitter capacitance (C_π). This produces a limiting pole at the input that is overcome by series inductive peaking. To achieve the best values for L_1, L_2 and L_3, EM simulations were performed. For the MSB input, the preferred combination was an inductor placed before the amplifier (L_1) and another one (L_2) between the amplifier and the resistor (R_b), which results in a pi network L-C-L optimized for input matching and bandwidth response. For the LSB, as the input capacitance is half, only one inductor (L_3) was required to produce similar frequency response, resulting in an L-C structure. Due to the lack of retiming, the propagation of both signals are required to have same group delay, so the inductance values of L_1 and L_3 were chosen with similar values. The values are detailed in Table 4.3. As seen in Fig. 4.15, the positive and negative inductor lines have to result in different layout design due to the location of the four input pads. A scheme where the inner lines are bended was followed in order to

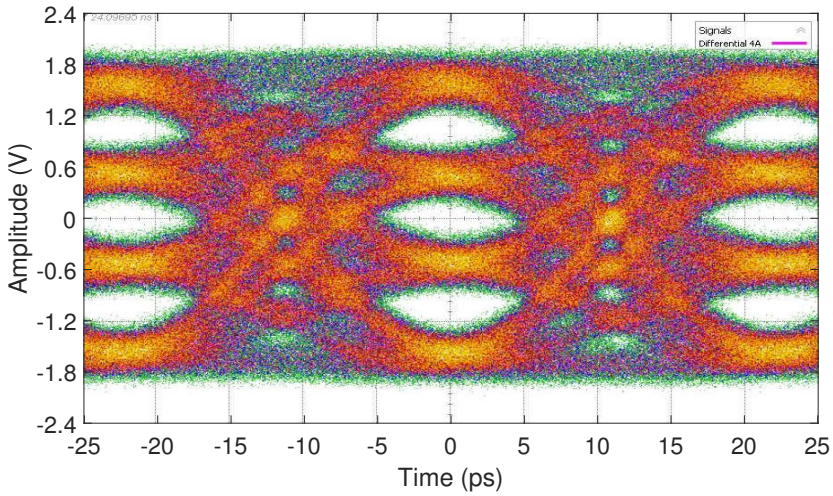


Figure 4.18: Measured PAM-4 differential eye-diagram of the driver output at 45 Gbaud (90 Gb/s) using PRBS31 at the input.

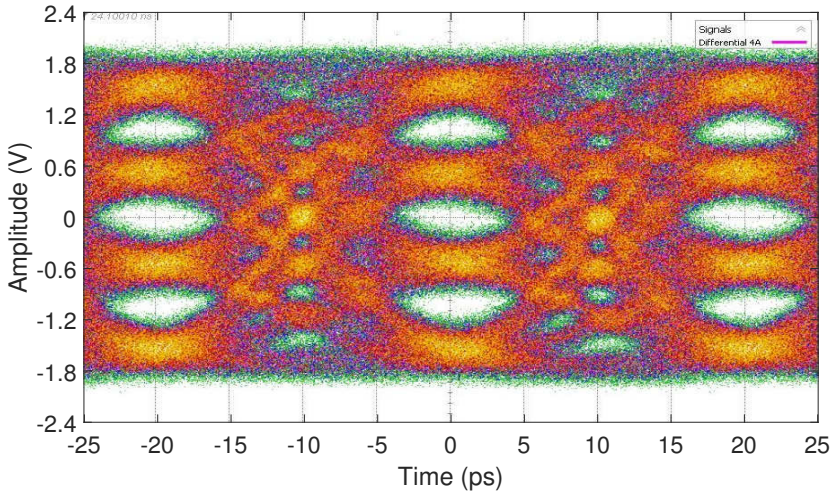


Figure 4.19: Measured PAM-4 differential eye-diagram of the driver output at 50 Gbaud (100 Gb/s) using PRBS31 at the input.

maintain the same physical length and inductance value between the inductors of the positive and negative lines for both inputs. To further enhance the bandwidth of the circuit, a network of inductors was designed at the output as well. Shunt inductive compensation was used at the supply node with the inductor L_4. This technique creates peaking at higher frequencies, increasing the bandwidth value by 15%. This comes however at the expense of inducing group delay variance across the frequency domain, so the value was carefully chosen to maintain a flat group delay response. Finally, inductor L_5 is placed in series to the output, improving output matching at the higher frequencies. The group delay values of each component encountered by the signal from the input to the output (inductors and amplifiers) are presented in Table 4.3. The total group delay of the circuit is 13 ps.

The circuitry to bias the base of transistors Q_1 and Q_2 is presented in Fig. 4.14. This circuit is placed twice in the driver to provide bias for both inputs. Having the pins V_{bias1} and V_{bias2}, the bias conditions of the amplifiers can be fine-tuned during the circuit operation, with the objective to equalize the four levels of the PAM signal. The third circuit shown in Fig. 4.14 is the reference used to bias the base of the cascode transistor of the gain cells.

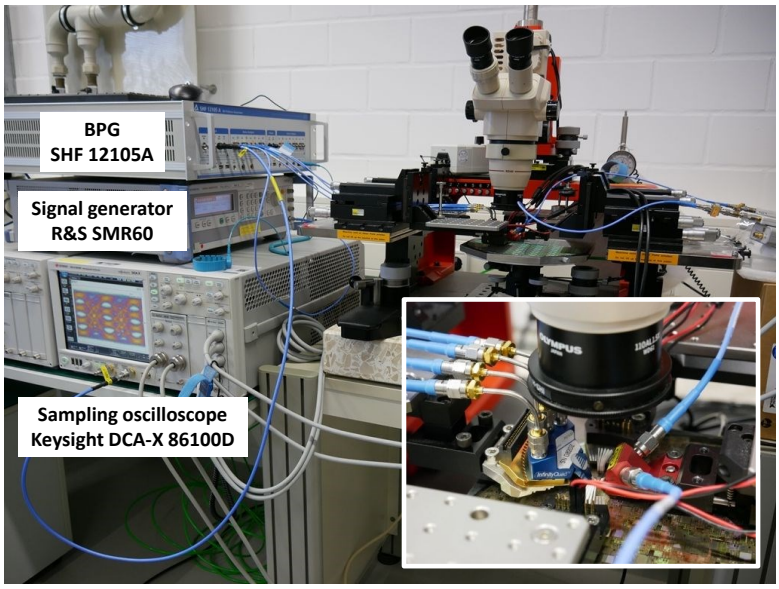


Figure 4.20: Experimental setup for on-wafer PAM measurements. The inset shows the magnified picture of the probing setup.

The chip microphotograph of the PAM-4 driver is presented in Fig. 3. The layout of the circuit occupies an area of 0.9 mm^2 (1.35 mm × 0.65 mm). With a supply (V_{CC}) of 5 V, the total power dissipation is 390 mW.

4.3.2 Measurement Results

True-differential S-parameters characterization of the driver was performed on-wafer using a 4-port VNA Rohde & Schwarz ZVA67 with a channel base power of -10 dBm. Two measurements were performed. First, the four ports were connected to the differential MSB input and the differential output, and after to the LSB input and the output. The measured gain (S21) of the two signal paths are presented in Fig. 4.16 together with the simulation results. The MSB amplifier has a bandwidth of 40 GHz and the LSB amplifier 43 GHz. Input return loss is better in the LSB input (10 dB up to 40 GHz) due to the larger input capacitance in the MSB input (which has input return loss better than 10 dB up to 20 GHz). Output return loss is better than 10 dB up to 30 GHz. The results show good agreement between measurements and simulation. Group delay data was extracted from these measurements and it is depicted in Fig. 4.17. The average group delay value of the measurements equals to the expected value of 13 ps. The measurements also demonstrate negligible difference between the delays of the MSB and LSB paths.

Time-domain measurements were also performed to demonstrate the PAM-4 encoded signal and the large-signal capability of the driver. Two differential 900-mVpp PRBS31 signals generated by a BPG SHF 12105A were applied to the MSB and LSB inputs of the driver. At the output of the driver, the differential signal was AC-coupled using two DC blocks, attenuated by 10 dB and connected to a sampling oscilloscope Keysight DCA-X 86100D with 60-GHz sampling probes. A picture of this setup is shown in Fig. 4.20. The differential output

Table 4.4: Comparison of State-of-the-art PAM-4 Drivers

Ref.	Technology	f_T (GHz)	Topology	Data rate (Gb/s)	Diff. output amp. (Vpp)	Power (W)	Output power / power dissipation ratio
[67]	0.18 µm BiCMOS	-	4-half-rate inputs with 2:1 mux	112	2.2	2.31	0.26%
[68]	0.5 µm InP HBT	290	built-in mechanism to adjust levels	56	2.24	0.956	0.66%
[69]	28 nm CMOS FDSOI	-	with 4 FFE taps and PLL	64	1.2	0.145	1.24%
This work	**0.13 µm BiCMOS**	**300**	**retiming not required**	**100**	**4**	**0.39**	**5.13%**

signal at 45 Gbaud (90 Gb/s) is presented in Fig. 4.18 and at 50 Gbaud (100 Gb/s) in Fig. 4.19, showing peak-to-peak amplitude of 4 V and verifying the PAM-4 generation by the driver.

Table 4.4 summarizes the state-of-the-art in PAM-4 drivers. It has to be noted that the described design sacrifices functionality in favor of targeting large output amplitude and high efficiency, in contrast to other implementations which have additional blocks for signal retiming, levels adjustment [68] and emphasis [69], increasing the total power dissipation. Therefore, the driver here reported achieves the highest output voltage and the highest output power to power dissipation ratio. These results demonstrate the potential of the implemented driver to deliver high-voltage PAM-4 signals to optical modulators for future optical communications standards.

4.3.3 Summary

A PAM-4 driver for optical modulators in 0.13 µm SiGe:C BiCMOS technology has been proposed. A topology of a single stage amplifier together with reactive components was followed to achieve high speed at low power consumption. S-parameter measurements were performed to characterize the driver in small-signal for LSB and MSB signal paths, demonstrating 3-dB bandwidth of 40 GHz. Time-domain measurements up to 50 Gbaud (100 Gb/s) were also performed to verify the PAM-4 signal generation and the large-signal capabilities of the driver. An output differential signal of 4 Vpp was demonstrated. The chip occupies an area of 0.9 mm^2. The total power dissipation of the IC is 390 mW. At the time of writing, this is the first PAM-4 driver in SiGe achieving such efficiency, data rate and output voltage, suitable for future 400-Gb/s optical transmitters.

5

Above 100 Gb/s Optical Transmitter Circuits

For the next generation standards, as 400G systems, specifications are converging towards the use of four amplitude level encoded data signals such as pulse amplitude modulation (PAM) and QAM [3], requiring ICs featuring analog bandwidths of above 50 GHz [70]. Beyond 400G, more complex modulation formats will be used, as such optical transmitters with large bandwidth and very high linear capabilities will be essential. In this chapter, two ICs are developed with the aim of being compatible with such high-speed standards. The first circuit is a linear driver using a distributed amplifier topology, capable of achieving very wide bandwidth from dc up to 90 GHz. The second circuit proposes a very efficient test chip for high-speed drivers, a bit pattern generator (BPG) capable of generating OOK signals up to 115 Gb/s, suitable to test optical front-ends in custom ICs for minimal losses.

5.1 A DC-90-GHz 4-Vpp Modulator Driver

In the same way which was described in previous chapters, typical configurations of optical transmitters make use of external modulation, utilizing MZMs. The integration of a linear driver in an optical transmitter scheme has the aim to amplify the complex analog signals coming from a DAC which were previously processed by a DSP. High bandwidth and linearity of the driver are essential to enable high-order modulation formats at high data-rates [71]. To meet the linearity requirements, limiting amplifier topologies cannot be used, and instead, emitter degeneration resistors and large collector currents which allow for enough headroom at the output of the amplifier are necessary. Additionally, since the modulators operate from dc, the circuit must provide broadband-matching which is accomplished by making use of resistive matching techniques, translating into low power-efficiency values. To increase the bandwidth, the use of typical millimiter-wave structures becomes also essential, since the operating frequency of the transistor is not anymore the main limiting factor, but the bandwidth is now mainly limited by the layout parasitics due to the size of the components.

Moreover, the electrical wavelength becomes comparable to the physical dimensions of the on-chip signal distribution. A circuit topology candidate to comply with these bandwidth requirements is the distributed amplifier. This type of amplifiers however, is limited by the typical requirement of off-chip ac coupling realization to reduce the low cutoff frequency, not compatible with the interface between the driver and the optical modulator. This problem can be solved by designing the distributed amplifier in a fully differential configuration, such that the ac ground will emerge intrinsically, solving the previously described constraints and allowing for gain down to dc [72, 73, 74, 75, 76]. Having a differential output is also a typical requirement by the optical modulator which operates in a push-pull manner.

This section investigates the implementation of a differential linear driver using a distributed amplifier topology. The design is targeted to achieve very wide bandwidth from dc, suitable to transmit multilevel high data rate baseband signals for 400-Gb/s optical communications standards. To increase the driver efficiency, the amplifier comprises only one stage, reducing the total current consumption. However, it must be noted that this approach might limit the total gain value and therefore, an additional pre-driver may be required in certain applications. The driver is implemented using a SiGe BiCMOS technology. The high break-down voltage of the HBTs in this process is an important advantage to the driver design in comparison with other technologies which are within the same range of f_T values, as for example 28 nm RF-CMOS processes [77].

Inital description of this circuit is done in [78] where preliminary results were shown, demonstrating on-off keying (OOK) transmission at 50 Gb/s with output of $4\,V_{ppd}$ and PAM-4 at 30 Gbaud, and in [79] where the driver implementation is fully described and the high-speed capability for high-speed operation is proven through additional time-domain measurements at higher speed, achieving 120 Gb/s OOK and 45 Gbaud PAM-4 (90 Gb/s), and power measurements to characterize compression, linearity and noise.

5.1.1 Circuit Design

The driver is implemented in a 0.13 µm SiGe:C BiCMOS process with transit frequency (f_T) of 300 GHz and maximum oscillation frequency (f_{max}) of 500 GHz. The process is offered by IHP as SG13G2. There are seven metal layers available, two thick top metals and and five lower layers. The two top layers support high current density, having thickness of 2 µm and 3 µm. They are also suitable for RF passive components design (inductors and transmission lines) due to the low sheet resistance. Ground shield was designed in the third thin metal to leave available two layers for interconnections, isolating them from the RF design. Moreover, the process offers polysilicon resistors and metal-insulator-metal (MIM) capacitors. The MIM capacitors are placed between the fifth thin layer and the first top metal layer. Finally, the HBT transistors have $BV_{CEO} = 1.7\,V$ and $BV_{CBO} = 4.8\,V$, featuring high break-down voltage suitable for power applications [80].

5.1.1.1 Distributed amplifier

A typical driver configuration is depicted in Fig. 5.1a), with a cascode amplifier topology. The value of R_c is 50 Ω for output matching. At the output, R_c in parallel with the 50-Ω equivalent load, translates into a collector resistance of 25 Ω, seen from the amplifier side. To guarantee

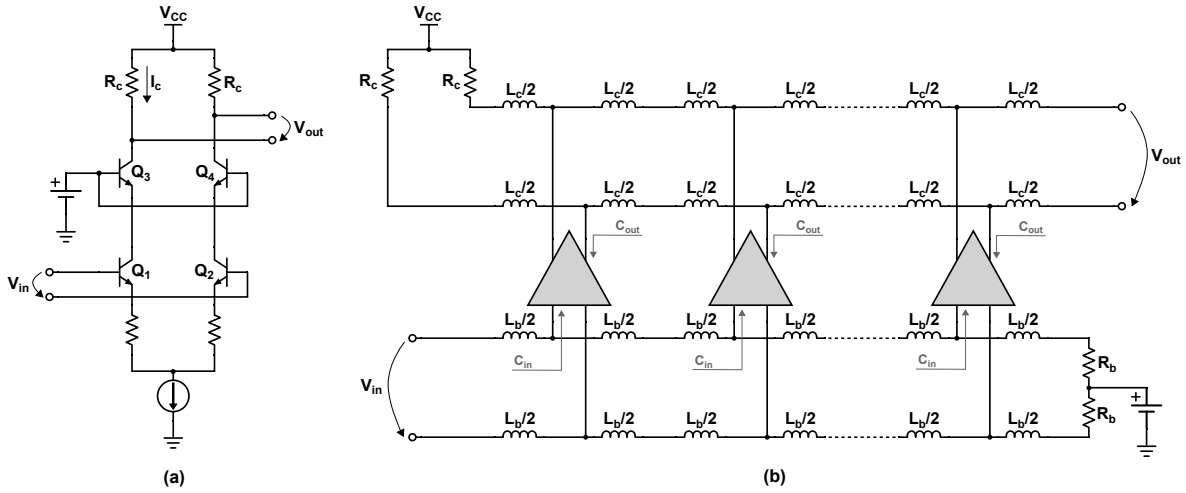


Figure 5.1: a) Typical driver schematic. b) Differential distributed amplifier topology.

enough headroom in the equivalent output resistance, for an output voltage swing of $4\,\mathrm{V_{ppd}}$ ($1\,\mathrm{V}$ peak single-ended at each output) plus some additional headroom to ensure proper bias, the circuit is biased with a collector current of $50\,\mathrm{mA}$ ($\mathrm{I_c}$), which results in a total current consumption of $100\,\mathrm{mA}$ for the differential amplifier. With such amount of current, circuit components are required to be considerably large and the parasitic capacitances coming from the layout interconnections become too large, limiting the circuit performance. Moreover, a number of pre-stages with buffer amplifiers would be required to drive such transistors, increasing the total power dissipation. Buffers would also be necessary to reduce the input capacitance in order to place 50-Ω resistors for input matching without limiting the overall bandwidth. It is here where the benefits of a distributed topology arise. A general schematic of such topology is shown in Fig. 5.1b). It consists in n gain cells embedded between two artificial transmission lines, one for the input signal and the other to guide the output signal. The gain cells add individual $\mathrm{g_m}$'s of the HBTs without adding their input and output capacitances [81]. This configuration is then doubled to turn the amplifier into a differential topology as observed in Fig. 5.1b).

5.1.1.2 Transmission lines

The input and output transmission lines comprise a ladder network of T-sections which embeds the capacitive elements from the amplifier with series inductance [82]. Additionally, the designed lines also have capacitance which needs to be considered, leading to an iterative design procedure.

The characteristic impedances of the input (Z_b) and output (Z_c) lines are designed to match 50 Ω and can be approximated as [83, 81]:

$$Z_\mathrm{b} = \sqrt{\frac{L'_\mathrm{b}}{C'_\mathrm{b} + \frac{C_\mathrm{in}}{l}}} \tag{5.1}$$

$$Z_\mathrm{c} = \sqrt{\frac{L'_\mathrm{c}}{C'_\mathrm{c} + \frac{C_\mathrm{out}}{l}}} \tag{5.2}$$

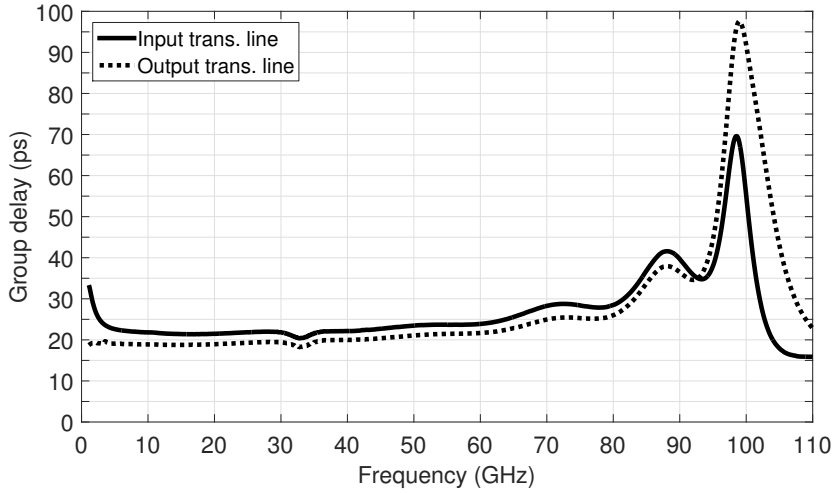


Figure 5.2: Simulation of the group delay of input and output transmission lines.

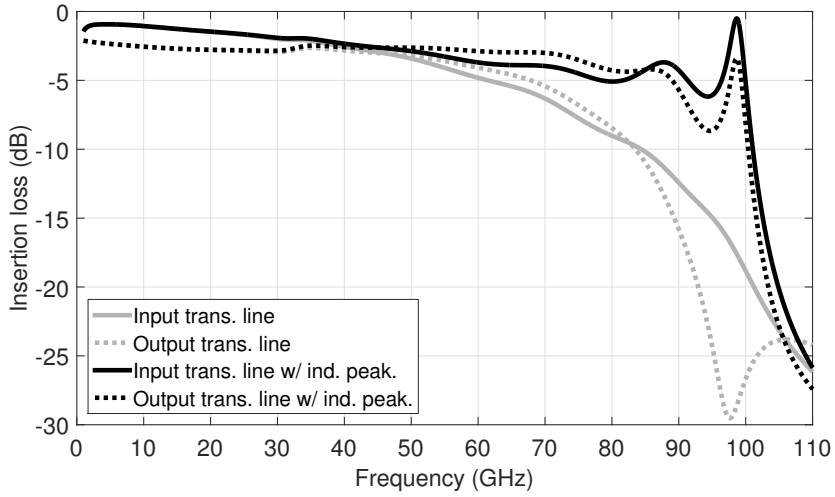


Figure 5.3: Simulation of the insertion loss of input and output transmission lines.

where L'_b, C'_b and L'_c, C'_c are the inductance and the capacitance per unit of length of the input and output transmission lines segments, respectively and l is the length of the line between gain cells. C_{in} is the input capacitance of the gain cell, where the base-emitter capacitance ($C_\pi = 67\,\text{fF}$) of the common-emitter transistor is the main contributor. C_{out} is the output capacitance of the gain cell, largely represented by the collector-substrate capacitance ($C_{cs} = 9\,\text{fF}$) and the equivalent capacitance from the collector-base capacitance ($C_\mu = 21\,\text{fF}$) of the common-base transistor.

For a constructive gain behavior in the distributed amplifier, the currents at the output of each gain cell should be added in phase along the propagation of the signal in the output transmission line. To comply with this requirement, the group delay of the input and output transmission lines must match, according to the follow relation [84]:

$$\sqrt{L'_b l(C'_b l + C_{in})} = \sqrt{L'_c l(C'_c l + C_{out})} \tag{5.3}$$

The group delay results extracted from the simulation of the implemented input and output transmission lines are presented in Fig. 5.2. The difference of time across a broad range of frequencies is approximately 2 ps, representing a maximum of 10% of mismatch.

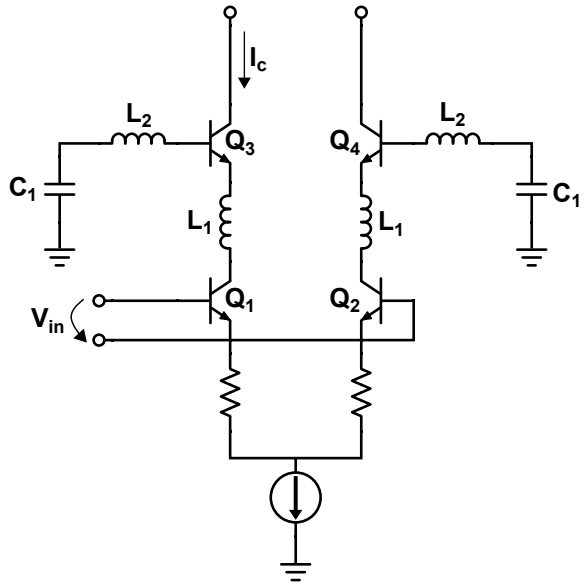


Figure 5.4: Simplified schematic of the gain cell.

Ideally, the bandwidth of the distributed amplifier is dominated by the input and output cutoff frequencies which are expressed as [83, 84]:

$$f_{c,\mathrm{in}} = \frac{1}{\pi\sqrt{L'_{\mathrm{b}} l (C'_{\mathrm{b}} l + C_{\mathrm{in}})}} \tag{5.4}$$

$$f_{c,\mathrm{out}} = \frac{1}{\pi\sqrt{L'_{\mathrm{c}} l (C'_{\mathrm{c}} l + C_{\mathrm{out}})}} \tag{5.5}$$

However, the losses of the transmission lines have to be taken into account. The losses are originated by two main factors: the sheet resistance of the metal and the input resistance of the HBT. To overcome these losses at high frequencies, a topology using a common-source MOSFET together with a common-base HBT (BiCMOS cascode) [76, 84] or a scheme using cascode with HBTs preceded by an emitter-follower [72, 85] have been proposed. A BiCMOS cascode amplifier is desirable but could not be considered in this design due to the limited bandwidth of the MOSFETs in this technology. The emitter-follower solution was also not used in this design to minimize the power dissipation, reducing the number of stages. Moreover, the usage of the emitter-follower, technique also known as common-collector cascode, transforms the capacitance seen between the emitter-follower and the cascode stage into a negative resistance, and is prone to cause stability issues [86].

In previous implementations of distributed amplifiers, with slower technologies, it is seen how, in order to comply with (5.3), the output line needs to be longer [87]. Additionally, to maintain $Z_{\mathrm{b}} = Z_{\mathrm{c}} = 50\,\Omega$, the output line is wider to reduce the inductance. However, when the capacitance of the transistors, $\mathrm{C_{in}}$ and $\mathrm{C_{out}}$ and parasitics of the layout routing start to be in the range of the lines capacitance ($\mathrm{C_b}$, $\mathrm{C_c}$), it becomes more practical to have input and output transmission lines with similar physical structure. In this design the lines have same length value (l_b, l_c) of 308 µm for each metal strip per stage. The lines are bended to reduce the chip footprint. The width of the artificial lines is much narrow than conventional 50-Ω lines in this technology (4 µm of width instead of 15 µm), behaving as inductors, and together

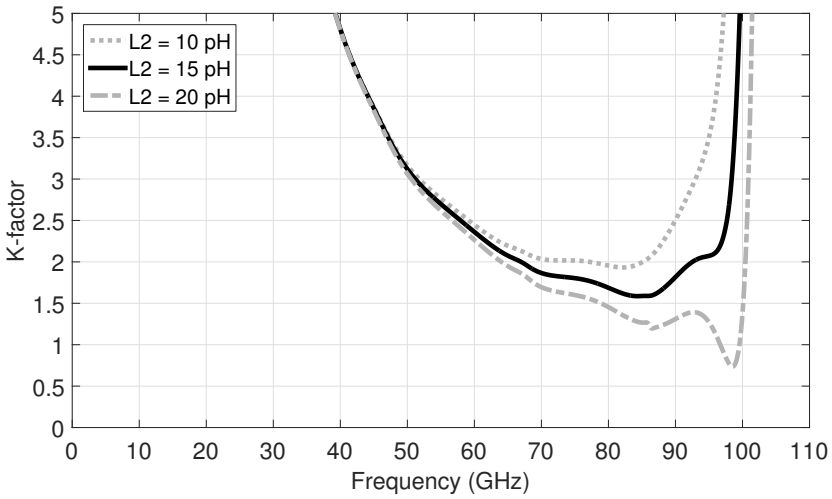


Figure 5.5: K-factor simulation for different values of L_2.

with $C_{b,c}$ and $C_{in,out}$ the artificial transmission lines of 50 Ω are created. C_{in} is still higher than C_{out}, originating a slight difference of group delay which is observed in Fig. 5.2. Due to the narrow width of the lines, high losses at high frequencies are expected, due to the sheet resistance of the metal. The simulated insertion loss of the input and output transmission lines used in the design of the driver is depicted in Fig. 5.3 (in gray). As this is the main limiting factor of the bandwidth, these losses are then compensated through the frequency behavior of the gain cell.

5.1.1.3 Gain cell topology

A simplified schematic of the gain cell used in this work is depicted in Fig. 5.4. It is a differential cascode amplifier with inductive peaking technique. The cascode stage is the most suitable for the distributed amplifier topology, as it demonstrates the highest gain-bandwidth product [84]. It also has the highest output resistance, beneficial to the performance of the output transmission line [88]. Another advantage is the smaller input capacitance (C_{in}) due to the reduced Miller-effect in Q_1 and Q_2. Finally, it features high isolation between input and output signals. Inductive peaking is introduced in the gain cell using the interconnection between the common-emitter transistor ($Q_{1,2}$) and the common-base transistor ($Q_{3,4}$). The inductance value (L_1) is relatively small (approximately 15 pH) and the connection is designed in a low metal layer to avoid the usage of long vias which would increase the inductive effect. Furthermore, the connection to the ac ground coupling capacitor (C_1) at the base of the HBTs $Q_{3,4}$ also introduces inductive peaking. As referred before, the MIM capacitor in this technology is placed in upper metals in the layer stack, thus the interconnection of the transistors to the capacitors have to be considered, adding inductance value L_2 of approximately 15 pH. The values of inductors L_1 and L_2 are estimated using electromagnetic simulation in Keysight Momentum. These inductors create a resonance frequency seen from the input and output of the gain cell. The result of the resonance is observed in Fig. 5.3, where a simulation of the insertion loss of the lines is plotted with the inductive peaking effect of the gain cell. This behavior partially compensates the losses of the lines, bringing a higher bandwidth value to the driver [84]. In order to analyze the impact of L_2 on the stability of the driver, K-factor

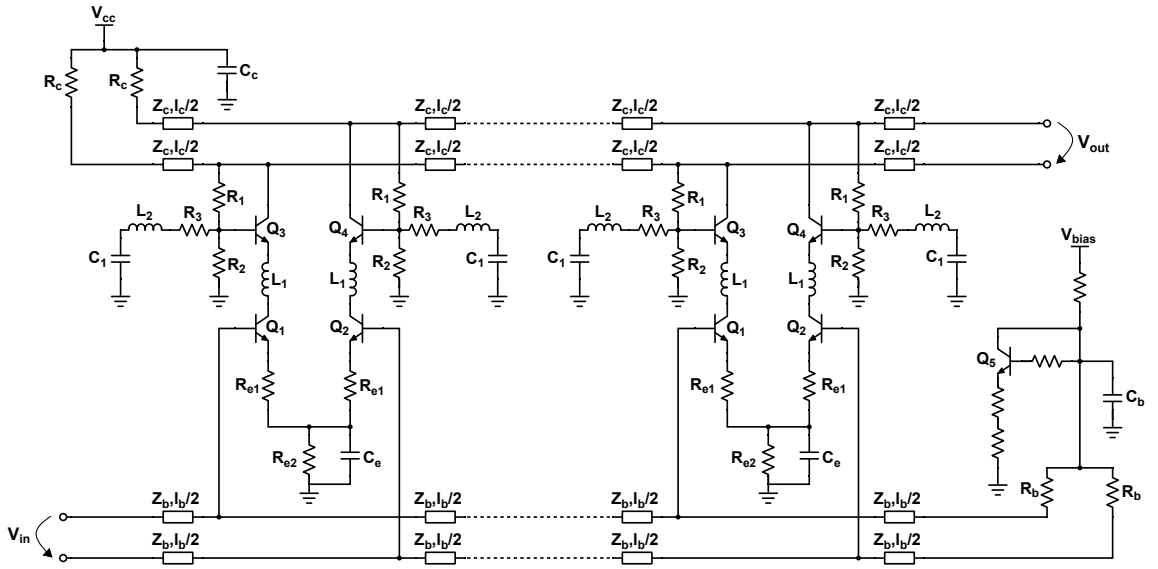


Figure 5.6: Full circuit schematic.

values over frequency were extracted from the differential S-parameters simulation for different values of the inductance. These results are depicted in Fig. 5.5. For the predicted value of 15 pH the K-factor is over 1, ensuring the stability of the amplifier. However, for a value of 20 pH, the K-factor becomes lower than 1 (close to the frequency of 100 GHz), reflecting how critical is to limit the value of L_2 in the design procedure.

5.1.1.4 Full driver schematic

The full circuit schematic is depicted in Fig. 5.6. The driver consists of six gain cells spaced by 250 µm which together result in the required number of transistors to drive the targeted output voltage amplitude. The value of R_c and R_b is 50 Ω for input and output matching. As presented before, a cascode amplifier scheme was chosen for the implementation of the differential pairs. It has to be noted that the cascode amplifier is also preferred in driver implementations for higher swing voltages, since it is BV_{CBO} limited and not by BV_{CEO} [89]. For the linearity requirements, degeneration resistors (R_{e1}) are included. Resistor R_{e2} is the current-source of the amplifier and enhances the CMRR. To enhance the stability of the amplifier, mainly due to the resonance created by L_2, feedback resistors (R_1) were added between the collector and the base of the cascode transistors (Q_3, Q_4), at the expense of slightly decreasing the overall gain. Moreover, with this scheme, the bias voltage of the base of Q_3 and Q_4 is not manually adjustable, and is dynamically tied to V_{cc}. The values of the resistor-divider composed by R_1 and R_2 determine the ratio between V_{cc} and the base voltage of the cascode transistor. Low-impedance resistor R_3 is also included to enhance the stability of the stage and C_1 ensures an ac ground at the base of the cascode transistor for the high-frequencies.

The chip microphotograph is presented in Fig. 5.7. The implementation of the differential arrangement of the distributed amplifier was done as follows. The transmission lines located in the middle are connected to the input pads (as seen in Fig. 5.7) and the output transmission lines are the outer ones, connected to the left part of the chip. Since the separation between transmission lines is critical, a stack of metals connected to ground was included in the

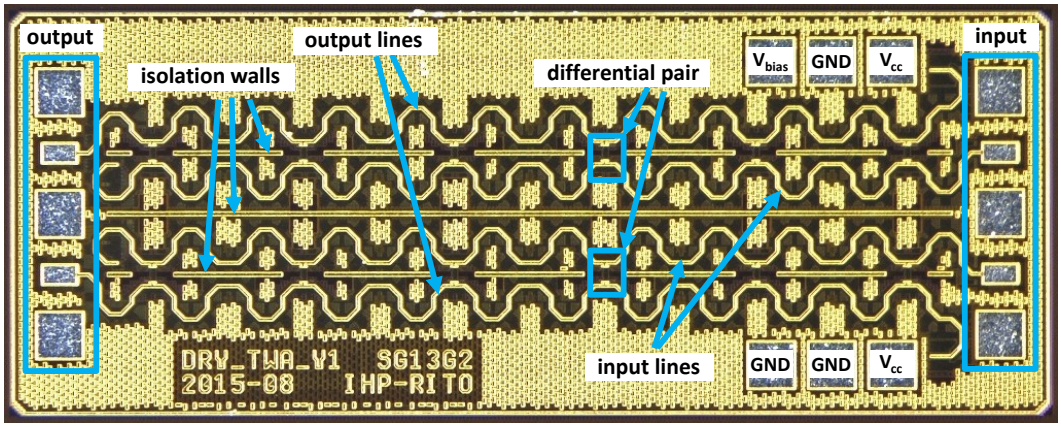


Figure 5.7: Chip microphotograph with pins description and identification of circuit parts.

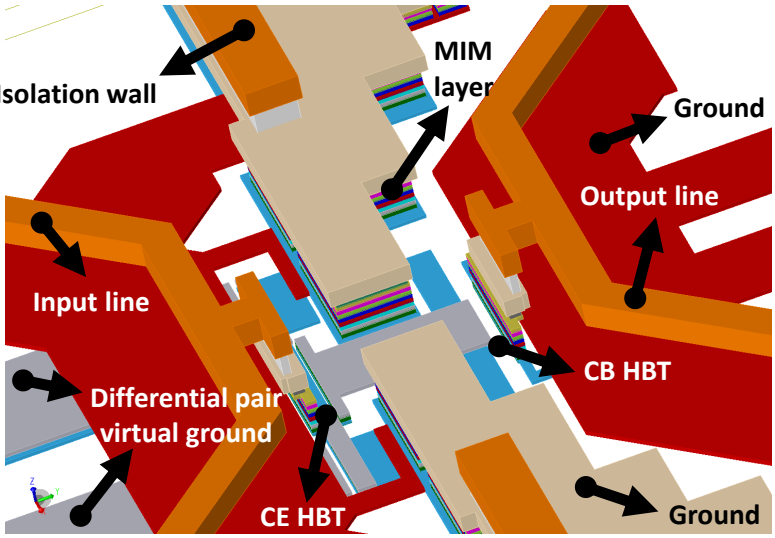


Figure 5.8: Layout 3D view (without resistors and transistors). Layout structure used in electromagnetic simulation in Keysight Momentum.

separation space between the lines, creating an isolation wall. Fig. 5.8 displays a 3D view of the layout of a single arm of the differential pair. The isolation wall is identified and it can be seen how it goes up to the RF layer (top metal). The other arm of the differential pair is placed between the other pair of input and output transmission lines, thus the active components of each arm are physically separated. The connection of the virtual ground below the degeneration resistors (R_{e1}) is carefully designed to not have any impact on the input characteristic impedance due to the crossing of the lines. This can also be observed in Fig. 5.8, where the virtual ground is placed below the ground shield. Electromagnetic simulations of this layout structure were performed in Keysight Momentum.

To be able to characterize the circuit for high-frequencies in a single-ended manner, some capacitors were included. The space between the two arms in each gain cell is filled with a capacitor (C_e) connected to the ground, creating an ac ground for high-frequencies. Additionally, capacitors were also included between the differential 50-Ω resistors on the termination of the lines (C_b and C_c), for the same purpose. The circuitry which includes Q_5,

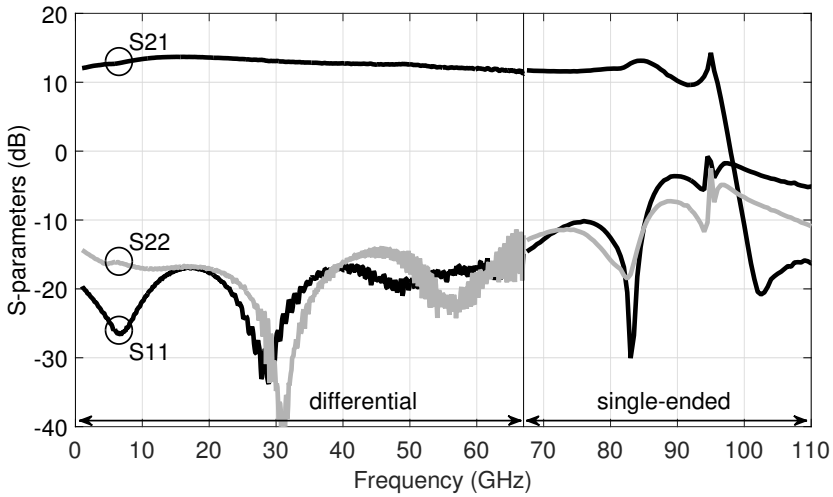


Figure 5.9: S-parameters measurement results (gain and return loss).

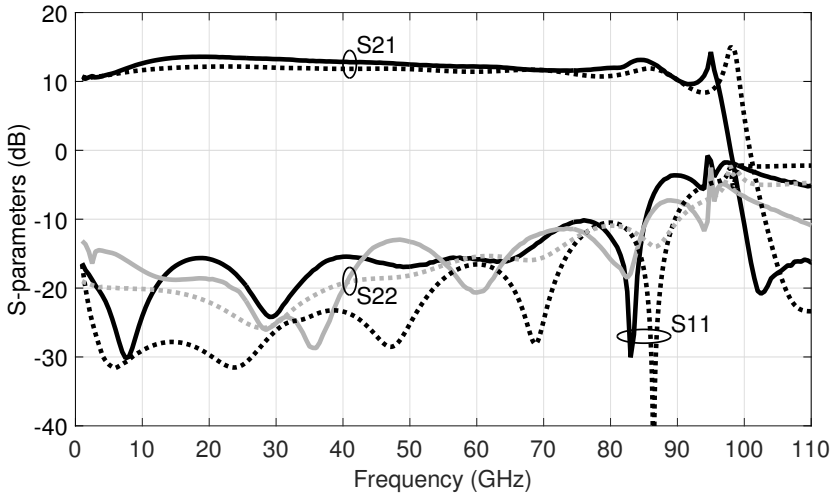


Figure 5.10: Single-ended S-parameters results (gain and return loss). Comparison between post-layout simulation (dashed) and measurements (solid).

several resistors and the external contact V_{bias} is the reference to set the bias point of the circuit. The control over V_{bias} is used to tune the overall current of the driver.

The differential linear driver occupies an area of $1.2\,mm^2$ ($1.75\,mm \times 0.68\,mm$). With a supply (V_{cc}) of 5.5 V, the total power dissipation is 550 mW.

5.1.2 Measurement Results

The measurements of the driver were performed in three parts. First, small-signal characterization in frequency-domain was performed. Thereafter, power measurements were executed to demonstrate the linearity of the driver and the maximum output power which is capable of delivering. Finally, time-domain measurements were performed to evaluate the high-speed behavior in terms of data rate and to demonstrate multi-level signals as well.

5.1.2.1 S-parameters measurements

S-parameters characterization of the driver was performed through two different frequency-domain measurement setups. With a 4-port VNA Rohde & Schwarz ZVA67, true-differential

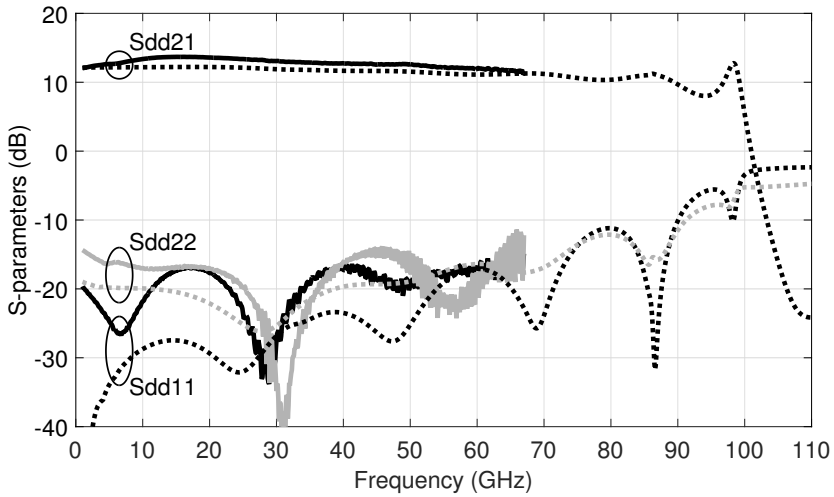


Figure 5.11: Differential S-parameters results (gain and return loss). Comparison between post-layout simulation (dashed) and measurements (solid).

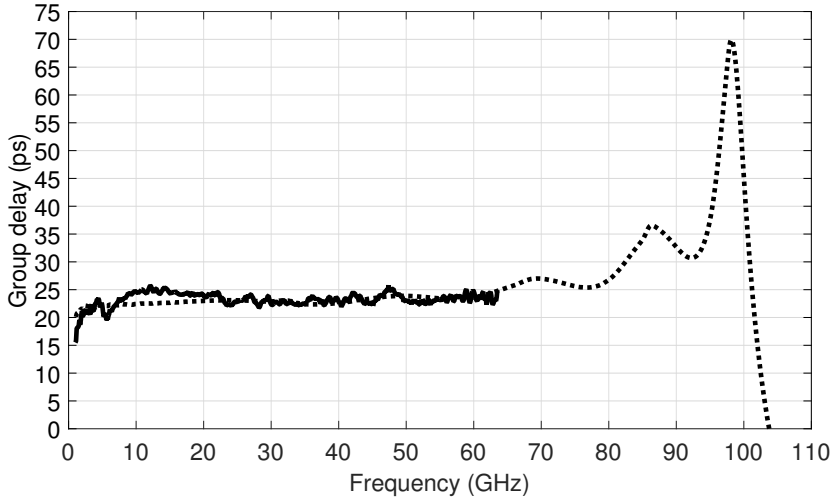


Figure 5.12: Differential S-parameters group delay results. Comparison between post-layout simulation (dashed) and measurements (solid).

S-parameters measurements were performed, fully characterizing the amplifier up to 67 GHz. To measure more than 67 GHz, a VNA Keysight 8510C with test heads E7352 (110 GHz) was used, with a 2-port configuration, therefore performing a single-ended test up to 110 GHz. In this way, it was possible to find the 3-dB bandwidth point. A plot with the two measurement results together is depicted in Fig. 5.9. The driver has small-signal gain of 12.5 dB and 3-dB bandwidth of 90 GHz. The input and output return losses are better than 10 dB up to 83 GHz. The circuit is dc coupled, so the reported gain is expected down to dc, required for optical communications and uncommon in distributed amplifiers, which either feature low cutoff frequencies in the order of 1 GHz or require bulky off-chip components for the ac coupling.

In Fig. 5.10, the single-ended measurements results are plotted with the single-ended post-layout simulation results. Through this comparison it is possible to observe that the peaking after the 3-dB bandwidth point is presented in the simulation results as well. As described in the subsection 5.1.1.3, the small inductors which are part of the layout parasitics create a resonance, improving the bandwidth of the driver. As a consequence of this, a peaking in S11 and S22 curves is also observed at approximately 95 GHz with values close to 0 dB, which might

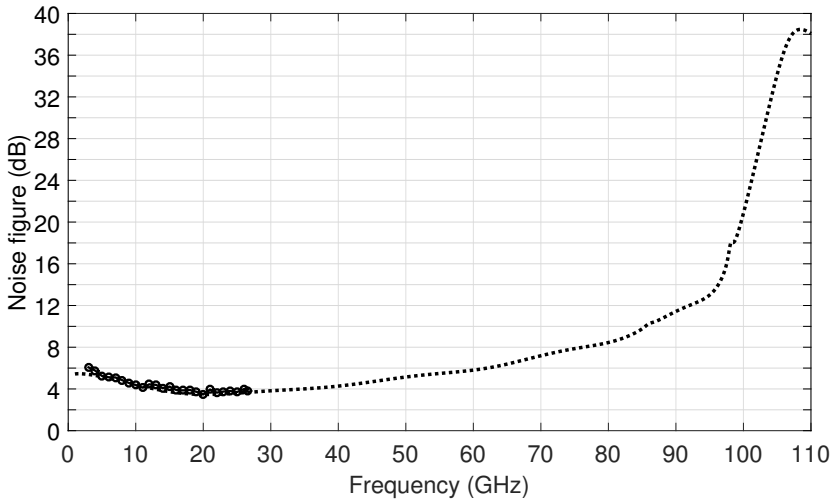


Figure 5.13: Single-ended noise figure results. Comparison between post-layout simulation (dashed) and measurements (marked with circles).

be an indicator for stability concerns. In Fig. 5.11, the differential post-layout simulations are plotted. It can be seen that the Sdd21 behavior is very similar to the single-ended S21 curve. However, Sdd11 and Sdd22 curves at the frequency of the peaking show an opposite behavior, as the values don't approximate to 0 dB. This difference can be explained by the fact that having differential excitation improves the ac ground coupling at the base of the common-base transistors, mitigating the peaking.

Group delay values were derived from the phase of the forward transmission coefficient of the differential S-parameters measurements Sdd21. The measurements were performed with a frequency step of 100 MHz and the curve was plotted using an aperture value of 5. The group delay curve is shown in Fig. 5.12 in comparison to the simulated values. It can be observed that the group delay response of the driver is very flat across the measured frequency range, with a variation of less than 5 ps.

5.1.2.2 Power measurements

Firstly, noise figure (NF) measurements were performed in a single-ended manner from 3 GHz to 26.5 GHz with an Agilent NFA N4002A (noise source N40002A). The results are presented together with the post-layout simulation results in Fig. 5.13. In the measured frequency range the two curves are very closely matched. The minimum NF is less than 4 dB at 20 GHz with a maximum of almost 12 dB at 90 GHz.

Thereafter, to demonstrate the linearity of the driver, total harmonic distortion (THD) was measured for a set of frequencies as a function of the input signal amplitude. The setup to perform these measurements is described as follows. The signal at the input is generated using Rohde & Schwarz SMR60 signal generator. The signal is converted to a differential signal using a broadband balun Marki microwave BAL0067 with balanced phase up to 67 GHz, and connected to the chip; at the output another balun, with same characteristics, combines the differential signal into a single-ended signal that is connected to a Keysight E4448A Spectrum Analyzer (limited to 50 GHz). Frequency tones of 1, 8 and 14 GHz were generated at the input, and the output spectrum data was collected through the signal analyzer. After accounting

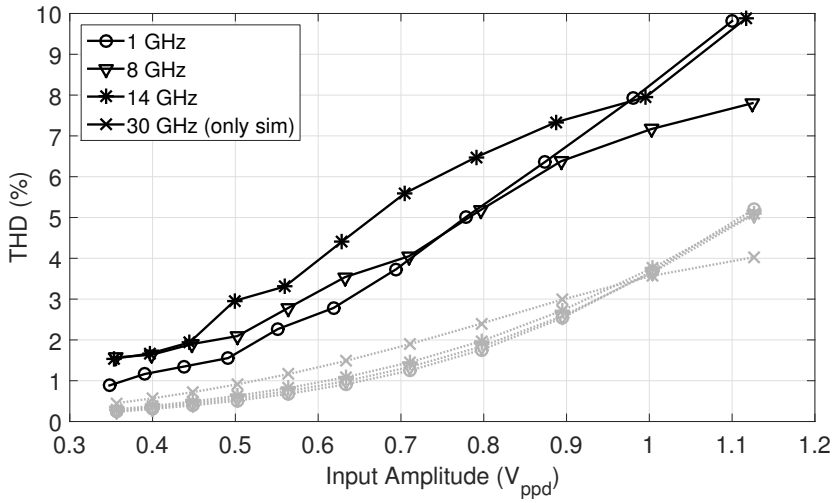


Figure 5.14: THD results over input amplitude for different frequency values. Comparison between post-layout simulation (gray) and measurements (black).

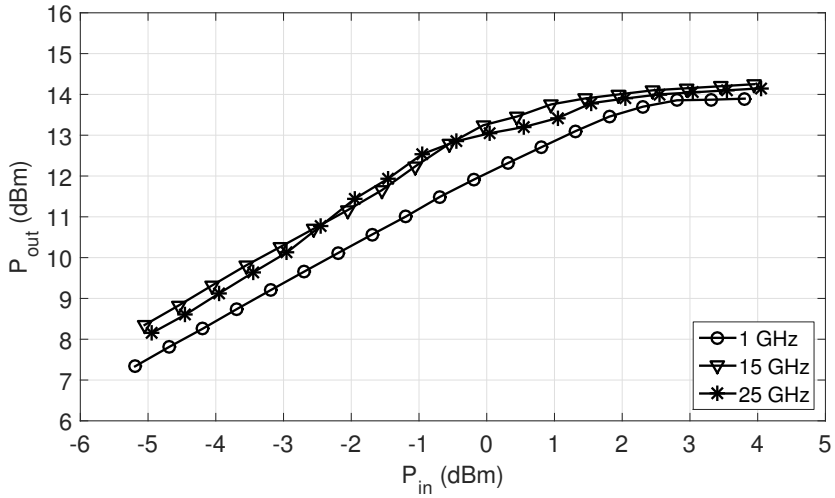


Figure 5.15: Measured output power (P_{out}) over input power (P_{in}) for different frequency values.

for the losses of the setup (cables and baluns) at the input and at the output, the data was processed and THD values were calculated for a input voltage amplitude range from 0.3 V_{ppd} to almost 1.2 V_{ppd}. The THD was only measured until 14 GHz, due to the limited frequency of the setup, so that three or more harmonics of the signal could be included. The results are depicted in Fig. 5.14. THD is below 5 % up to an input amplitude of 800 mV_{ppd} at 1 and 8 GHz and up to almost 700 mV_{ppd} at 14 GHz. In this range of amplitude a good linearity of the driver is expectable (equivalent to an output amplitude of 3 V_{ppd}). A comparison to the simulation results is also depicted in Fig. 5.14, where simulated THD values show better linearity, which can be attributed to few imperfections in the measurement setup, such as delay mismatch in the differential signals.

Finally, using the same differential power setup of the THD measurements, power characterization was also conducted to find the compression point of the driver. In Fig. 5.15 three curves are presented of the output power over input power for 1, 15 and 25 GHz. The small-signal gain is correspondent to the S-parameters measurements and input P1dB is found at approximately 2 dBm.

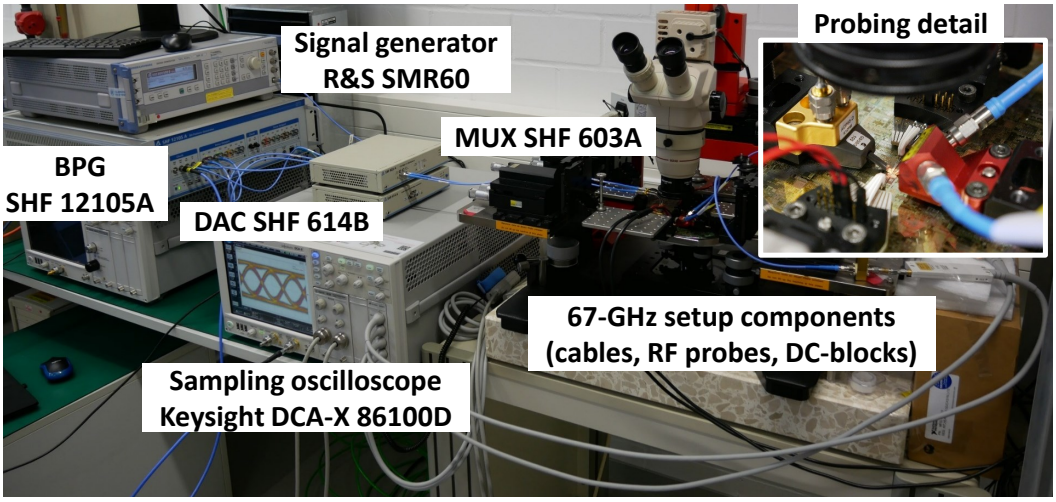


Figure 5.16: Experimental setup for on-wafer time-domain measurements. The inset shows the magnified picture of the probing setup.

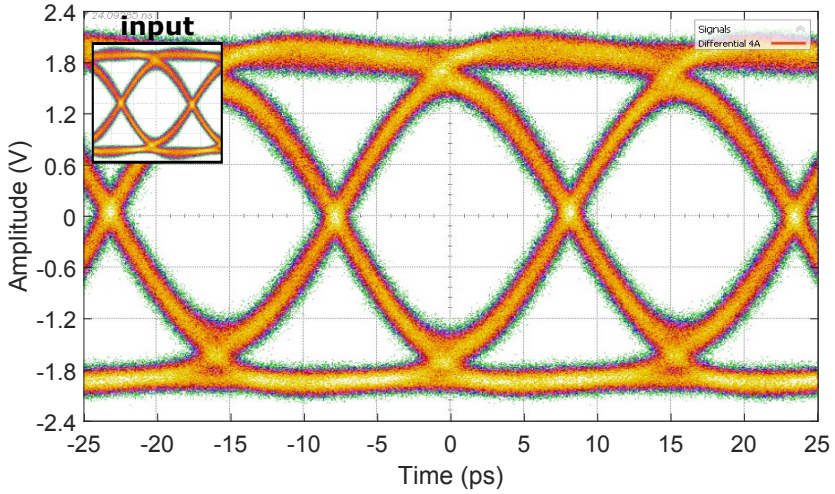


Figure 5.17: Differential output eye-diagram OOK 64 Gb/s with $4\,V_{ppd}$ (input $1.2\,V_{ppd}$). Measured eye amplitude is 3.3 V, jitter peak-to-peak is 3.6 ps and jitter rms is 507 fs. The inset shows the input eye-diagram.

5.1.2.3 Time-domain measurements

Time-domain measurements were performed on-wafer to demonstrate the large-signal operation of the driver using a BPG SHF 12105A of 8 channels up to 64 Gb/s. One of the channels of the BPG, generating a PRBS31 differential signal up to $1.2\,V_{pp}$, was connected to the input of the driver. At the output, the signal was attenuated by 10 dB and connected to a sampling oscilloscope (Keysight DCA-X 86100D) with the attenuation value included. The OOK differential output eye-diagram at 64 Gb/s is presented in Fig. 5.17, showing the maximum amplitude of $4\,V_{ppd}$, thus having a large signal gain of 10.5 dB.

Secondly, a multiplexer (MUX) SHF 603A was added to the setup. The MUX doubles the OOK data rate up to 120 Gb/s using two channels of the BPG. This configuration is shown in a picture of the setup in Fig. 5.16. Two RF cables phase-matched with length of 0.5 m were used to guide the differential signal between the MUX and the input RF probe. Moreover, two similar RF cables were used between the output and the attenuators placed before the oscilloscope sampling heads (N1045A with 60 GHz of bandwidth). DC-blocks were

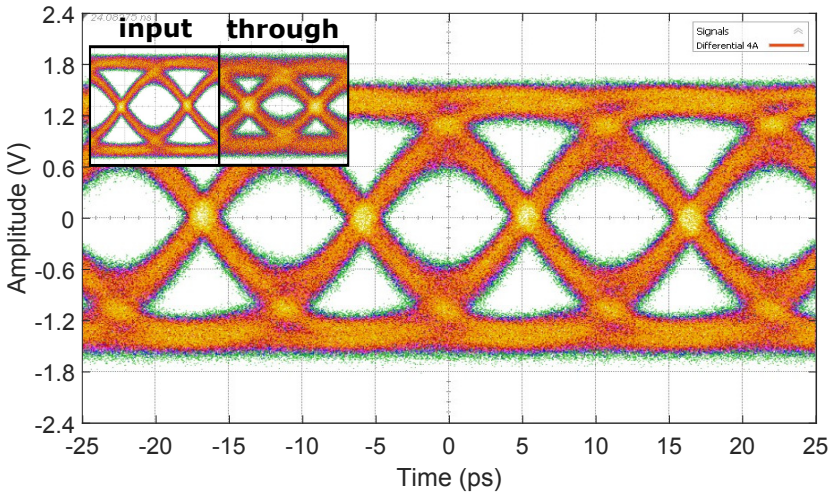


Figure 5.18: Differential output eye-diagram OOK 90 Gb/s with $3\,V_{ppd}$ (input $0.9\,V_{ppd}$). Measured eye amplitude is 2.123 V, jitter peak-to-peak is 3.4 ps and jitter rms is 609.5 fs. The insets show the input eye-diagram and the measured eye-diagram with a through structure.

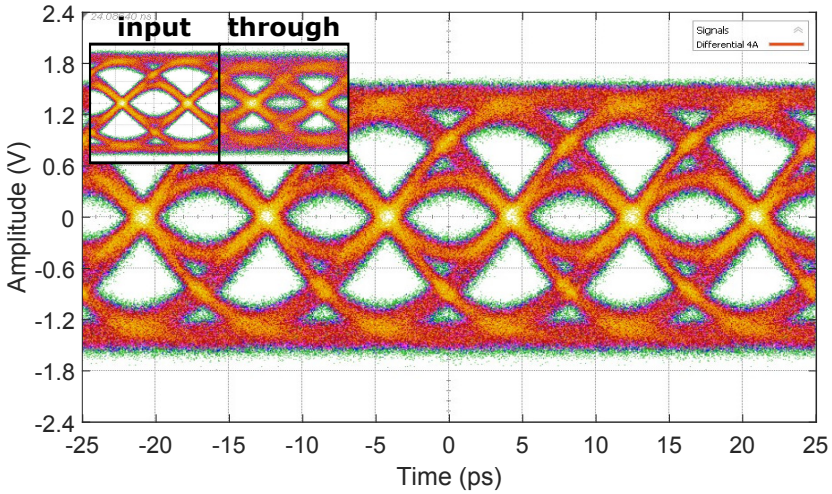


Figure 5.19: Differential output eye-diagram OOK 120 Gb/s with $3\,V_{ppd}$ (input $0.9\,V_{ppd}$). Measured eye amplitude is 1.775 V, jitter peak-to-peak is 4.0665 ps and jitter rms is 571.5 fs. The insets show the input eye-diagram and the measured eye-diagram with a through structure.

also required at the input and at the output. All these components have specification for 67 GHz. The maximum output voltage of the MUX was $900\,mV_{ppd}$, thus not sufficient to achieve the maximum output voltage swing of the driver. The differential output eye-diagram of the driver acquired at 90 Gb/s is presented in Fig. 5.18 and at 120 Gb/s in Fig. 5.19, both with an amplitude of $3\,V_{ppd}$. The input signal applied to the driver is depicted in the inset of the figures, where it is possible to observe that the quality of eye-diagram is already degraded at the input by the setup components, in particular at 120 Gb/s. The eye-diagram is also worsened by the components located in the connection from the driver output to the oscilloscope. This effect is observed in the included inset "through", where the driver was replaced between the two RF probes with a differential transmission line of 2 ps (available in the calibration substrate of the probes) to measure the eye-diagrams including all the setup losses.

Finally, to observe the linear behavior of the driver, PAM-4 measurements were conducted. Using the same setup described before, the MUX was replaced with a 6-bit DAC SHF 614B, using six channels of the BPG. The maximum performance of the DAC is 60 Gbaud, however

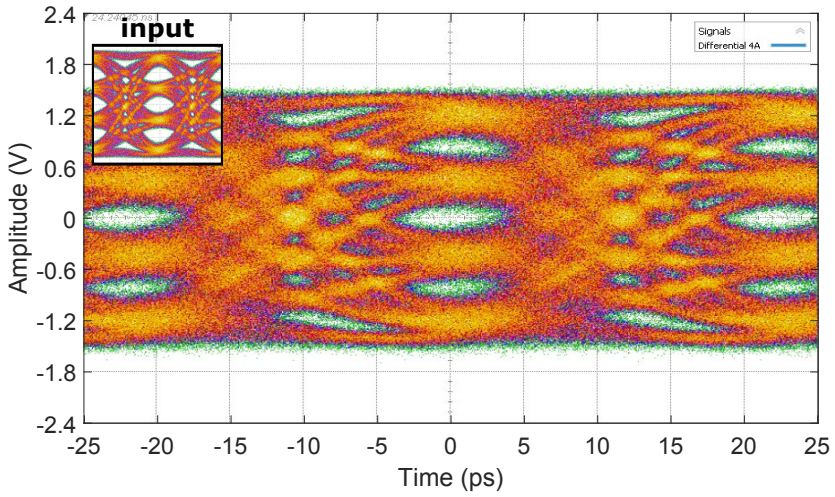


Figure 5.20: Differential output eye-diagram PAM-4 45 Gbaud (90 Gb/s) with 3 V_{ppd} (input 0.9 V_{ppd}), without pre-emphasis. The inset shows the input eye-diagram.

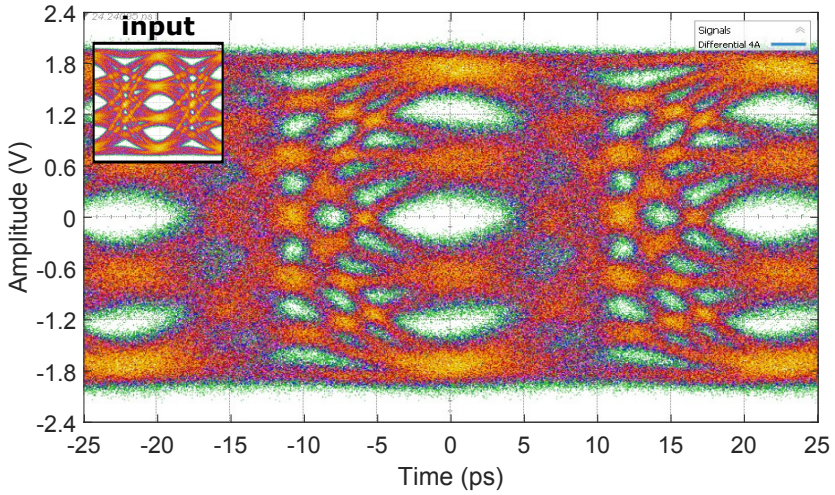


Figure 5.21: Differential output eye-diagram PAM-4 45 Gbaud (90 Gb/s) with 4 V_{ppd} (input 1.2 V_{ppd}), without pre-emphasis. The inset shows the input eye-diagram.

due to the bandwidth limitation coming from the components used on the setup, eye-diagrams were only measured up to 45 Gbaud. Differential output eye-diagrams with PAM-4 modulation are shown in Fig. 5.20 and Fig. 5.21. In Fig. 5.20, an input amplitude of 0.9 V was applied to the driver, achieving an output swing of 3 V_{pp}. In this region of operation the driver is operating in the linear region, hence equal eye-openings are observed in the output signal. The PAM-4 signal was also measured with an input amplitude of 1.2 V_{pp}, shown in Fig. 5.21. Here the maximum output of 4 V_{pp} is achieved. However, in this condition the driver is already in the saturation region, therefore the compression is observed in the eye-diagram, where the first and third eyes are relatively closed compared to the second eye. The input eye-diagram is shown in the figures for comparison. No pre-emphasis techniques were applied to compensate the setup losses or the compression of the driver.

5.1.2.4 Performance comparison

Table 5.1 summarizes the state-of-the-art implementations of drivers for optical modulators in different technologies. The driver presented in [43] uses a double breakdown topology,

Table 5.1: Comparison of State-of-the-art High-speed Drivers for Optical Modulators

Ref.	[43]	[27]	[73]	[90]	[70]	[76]	**This work**
Technology	0.25-µm SiGe BiCMOS	0.25-µm InP DHBT	0.25-µm InP DHBT	55-nm SiGe BiCMOS	55-nm SiGe BiCMOS	55-nm SiGe BiCMOS	**0.13-µm SiGe BiCMOS**
Driver Topology	double breakdown, limiting	linear	dist. amp with VGA, linear	limiting	push-pull MOS-HBT, linear	dist. amp, linear	**dist. amp, linear**
Bandwidth (GHz)	33.7	37.8	>67	-	57.5	>70	**90**
Gain (dB)	13	16.2	10.7	-	18.8	20	**12.5**
Data-rate OOK (Gb/s)	40	28	100	56	-	120	**120**
Data-rate PAM-4 (Gbaud)	-	28	-	-	64	64	**45***
Diff. Output Swing (V_{pp})	6	3	2	1.6	4.8	4.8	**4**
P_{DC} (mW)	1350	730	840	300	820	1100	**550**
P_{out} / P_{DC} ratio	3.3 %	1.5 %	0.6 %	1.1 %	3.5 %	2.6 %	**3.6 %**

*no pre-emphasis applied.

achieving high output voltage swing of 6 V and high efficiency of 3.3 %. However, as it uses the slowest technology of the comparison, it is limited by bandwidth, making it not suitable for the upcoming optical transmission standards. The drivers [27] and [73] are linear and implemented in InP DHBT technology. [27] has the highest output swing and power efficiency in InP DHBT processes. [73] uses a distributed amplifier topology as well, achieving high bandwidth (more than 67 GHz) and high data rate (100 Gb/s in OOK), similar to the driver presented in this work, however with less output voltage swing and power efficiency. [90] presents an implementation of a hybrid configuration of a MZM and a low-power limiting driver, not compatible for multi-level signals. [70] shows a linear driver using a push-pull MOS-HBT topology to achieve good efficiency and high output swing, reporting PAM-4 at 64 Gbaud with 4.8 V_{ppd}. Finally, [76] reports a distributed amplifier with 20 dB of gain, implementing the driver with higher number of stages (therefore having less power efficiency), achieving OOK up to 120 Gb/s. The driver implemented in this work has lower gain in comparison with [76] and [70], but it achieves the highest bandwidth reported in linear drivers, achieving OOK data rates in line with [73] and [76], combined with good power efficiency as in [70]. The reported performance in PAM-4 measurements is limited by the setup and by the fact that pre-emphasis was not applied. If a pre-driver had been integrated in the proposed design, higher power

dissipation would be expectable, and linearity could also be degraded. The driver is a good candidate for wide bandwidth applications, such as optical transmitters, where amplitudes around 1 V can be applied to the input of the driver.

5.1.3 Summary

A linear driver for optical modulators in a 0.13 µm SiGe:C BiCMOS technology has been described. The chip occupies an area of 1.2 mm^2. High bandwidth has been achieved by implementing a distributed amplifier topology in a differential manner, adapting the design to the requirements of optical transmitters. Differential and single-ended S-parameters measurements were performed to characterize the driver in small-signal, demonstrating 3-dB bandwidth of 90 GHz. To demonstrate the large signal capabilities of the driver, time-domain measurements were performed with OOK signals up to 64 Gb/s with output amplitude of 4 V_{ppd} and up to 120 Gb/s with output amplitude of 3 V_{ppd}. Furthermore, measurements with PAM-4 signals were also performed up to 45 Gbaud (90 Gb/s). The total power dissipation of the IC is 550 mW. At the time of writing, the proposed design has the largest small-signal bandwidth and the best efficiency for such high data-rates in high-voltage linear drivers.

5.2 A 0.87-pJ/b 115-Gb/s 2^7-1 PRBS Generator

In this section, a 115-Gb/s 2^7-1 PRBS generator is demonstrated with the lowest power consumption relative to the bit rate and sequence length [91]. To achieve this performance, the circuit is based on a half-rate topology, which was modified enabling the achievement of higher speed than the state-of-the-art without compromising on low power dissipation. The circuit is fabricated in the fastest 0.13 µm SiGe:C BiCMOS technology of IHP, SG13G2, with f_T/f_{max} of 300/500 GHz.

5.2.1 Introduction

PRBS generators are important blocks used for testing systems in time-domain measurements. The generated bit pattern is a wideband signal which can be applied to the input of broadband circuits, mostly used in communication transceivers. Fiber-optics transmission links demand ever-increasing data rates, requiring advancements in the measurement setups to fulfill such high-speeds. ICs designed for the front-end of optoelectronic solutions are currently achieving above 67-GHz bandwidths [79] which surpass the performance of most of the available equipment in the market. In addition, optical transmission formats, such as polarization-division-multiplexing QPSK and QAM, have been demonstrated at 107 Gbaud [92]. Moreover, in a transmission link experiment, cables, adaptors and DC-blocks tend to become the main speed limiting factors [79] and therefore the development of high-speed low-power PRBS generators which can be monolithically integrated in a communication chip is of special interest. Several implementations of such PRBS generators can be found in the literature, mainly based on SiGe and InP technologies, for high-speed operation. Reference [93] demonstrates a broadband transmitter which includes a 2^{11}-1 PRBS implemented in SiGe capable of achieving 80 Gb/s, with a power dissipation of 1 W. Similarly, [94] reports speed up to 80 Gb/s, with a longer

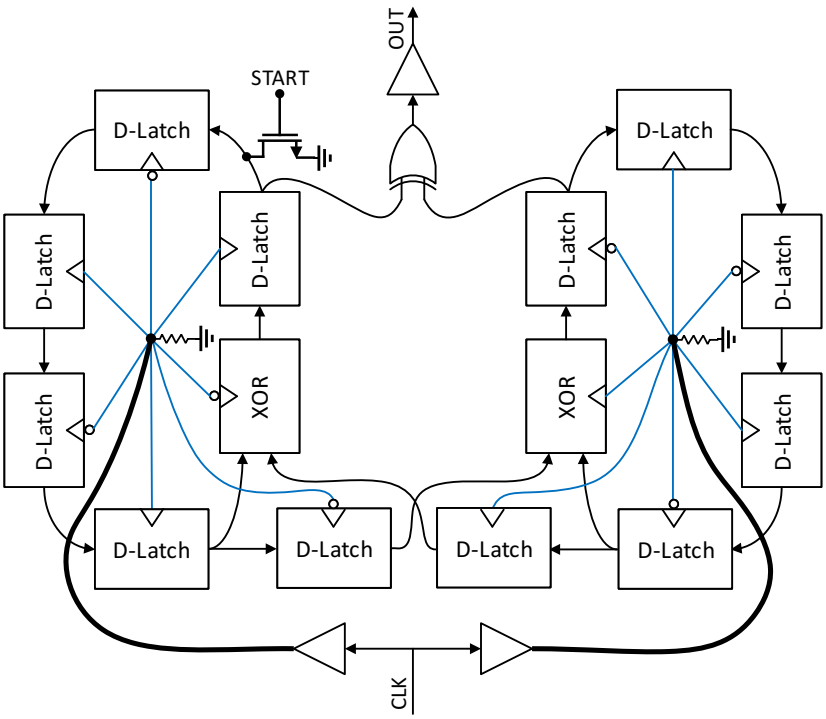


Figure 5.22: Block diagram of the implemented PRBS generator.

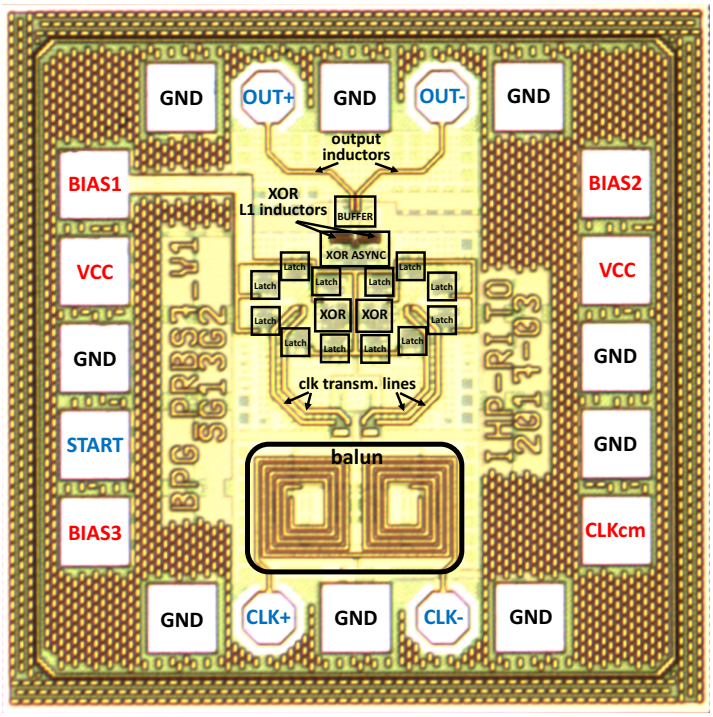


Figure 5.23: Chip microphotograph of the fabricated PRBS generator.

pattern of 2^{15}-1, hence dissipating a power of 1.7 W. A faster speed of 100 Gbs/s was achieved in [95], using an InP technology.

5.2.2 Architecture

The conventional architecture of a PRBS generator (pattern length 2^{N}-1), with N=7, requires seven flip-flops (or fourteen latches) of D-type and one XOR gate to produce the polynomial

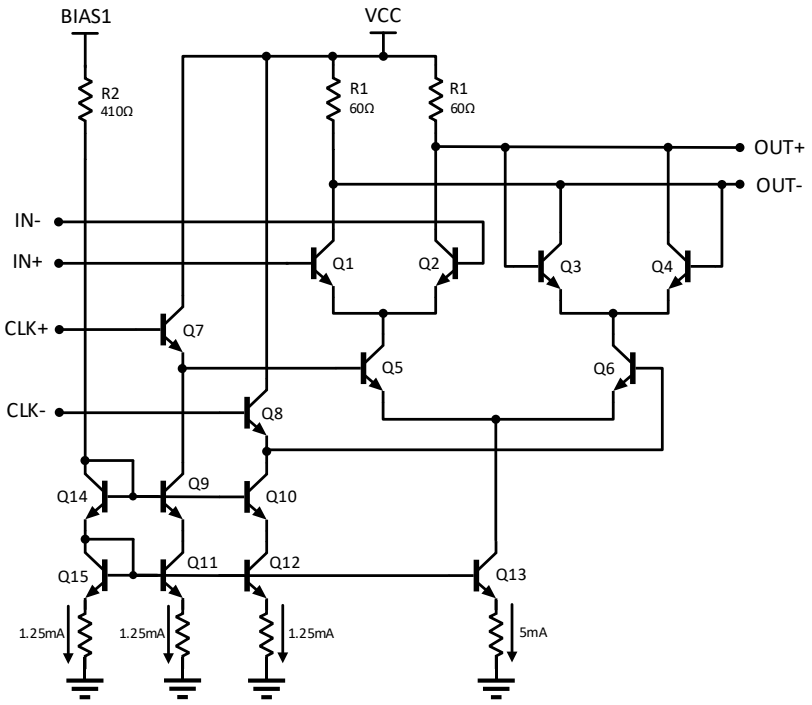


Figure 5.24: Schematic of the standard latch.

$x^7 + x^6 + 1$[96]. In this case every block has to operate at full-rate, limiting the maximum achievable speed. Alternatively, a half-rate topology makes use of two parallel loops which operate at half clock frequency, each one having seven latches and one XOR [96]. The generated signals by the two loops are asynchronously combined to produce the desired high-speed pattern. However, the need for these XOR gates adds unwanted delay to the signal path, degrading the synchronization between the clock and data signals. To alleviate this issue, [95] introduced a modified architecture requiring only one XOR gate, shared by both branches. However, the XOR gate is asynchronous and as it is part of both loops, delays the signal, still limiting the maximum speed. In [93] and [94] desynchronization is partially compensated in the design of the layout of the clock distribution, using transmission lines where the propagation delay of the clock is equivalent to the delay created in the data path. However, desynchronization will occur when closing the loop, in the connection between the last and the first latch, with which the limiting factor persists.

To overcome the above mentioned issues, here a modified half-rate topology is presented. The block diagram of the PRBS generator here implemented is presented in Fig. 5.22. The circuit operates with differential signals in all stages, although for simplification all nets are drawn as single-ended paths. The clock was distributed in a star manner, equalizing the propagation delay of the clock signal between a common point (transmission line termination) and all latches. Additionally, to improve the clock-signal synchronization, asynchronous gates inside the loop have been avoided, modifying the XOR gates inside the loops to be synchronous, replacing one of the seven latches per branch with an XOR gate [97]. Finally, outside the loops, the combination of the generated half-rate signals is realized with an asynchronous XOR gate

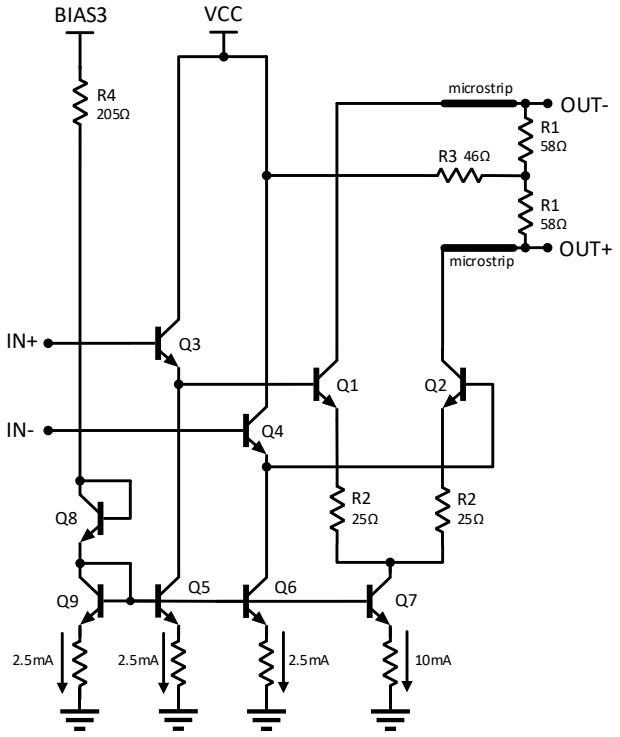


Figure 5.25: Schematic of the clock buffer.

which operates at a full-rate. The output signal is then amplified by a buffer stage to drive a differential 100-Ω load.

The chip microphotograph is shown in Fig. 5.23. Due to the difficulty to generate externally the differential clock signal with enough power amplitude, a balun is integrated in the chip, converting a single-ended continuous wave signal to a differential one. The balun can operate at clock frequencies from 20 to 60 GHz, which is the range where the phase difference between outputs is close to 180 degrees, the insertion loss varies from 4.7 dB to 6.3 dB and the input return loss is better than 7 dB, based on simulation results. The circuit includes the pin "START" to apply a trigger signal which pulls the output of one of the branches using an NMOS (as represented in Fig. 5.22), forcing the startup. "CLKcm" is the dc voltage which defines the common-mode voltage of the differential clock signal at the output of the balun. The bias pads are voltage references to the current mirrors of different types of stages which can be tuned during measurements. "VCC" is the main supply voltage (3.3 V). The layout of the circuit occupies an area of 0.64 mm^2 (0.8 mm × 0.8 mm).

5.2.3 Circuit Design

The schematic of the standard latch is depicted in Fig. 5.24. The D-type latches are implemented using a current-mode logic (CML) topology. Typically to enhance speed, feedback emitter followers are included as the last stage in latches [98]. In this implementation, as the latches are only present in the half-rate data paths (sampling up to 57.5 GS/s), and due to the high-speed response of the HBTs, they were found to not be required, which aids the power dissipation

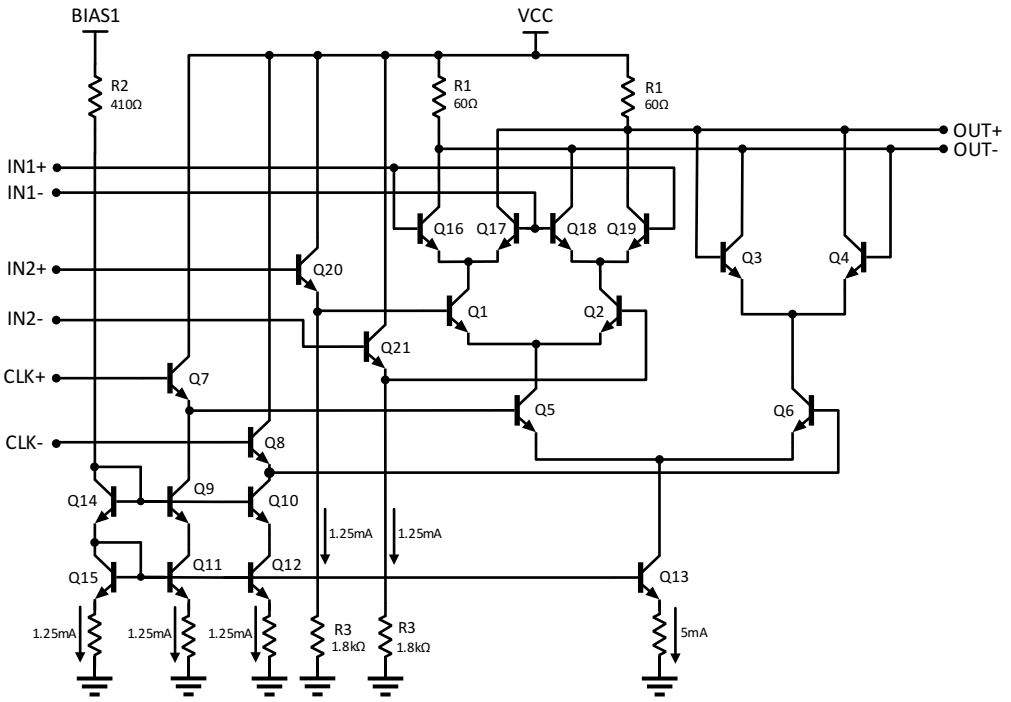


Figure 5.26: Schematic of the latch with XOR function (synchronous).

reduction. Emitter followers (Q7, Q8) are, however, needed to buffer the clock signal in each latch to increase input impedance, enhancing isolation for better clock distribution. All latches share the same voltage reference "BIAS1", with the current reference implemented in each latch through resistor R2. The value of resistors R1 is chosen as a trade-off between the required maximum speed of the latch and the sufficient current value to achieve a differential amplitude of 300 mVpp. The schematic of the latch with the synchronous XOR function is presented in Fig. 5.26. It is based on the schematic of the standard latch, which also excludes an output stage with emitter followers. In order to create the XOR operation, an additional differential input is created with the HBTs Q16-Q19. As both inputs reach this stage with the same common-mode, IN2 requires additional emitter followers (Q20, Q21) for dc-level shifting. To maintain the same behavior across all latches inside the loop, the current densities are kept the same in Q1-Q4 as in the standard latch. The total current consumption of this latch is only increased due to the inclusion of the emitter followers Q20, Q21. Furthermore, the current sources of these emitter followers are implemented with resistors R3 to keep the layout structure as close as possible to the D-type latch and to minimize parasitics in the signal path. The power dissipation of the two branches comprising all latches is 68% of the total power dissipation.

The asynchronous XOR gate uses a fully symmetrical circuit composed by two parallel Gilbert cells with inverted inputs [99]. The schematic is depicted in Fig. 5.27. Keeping full symmetry in this stage is critical, since it is not synchronous with the clock, and as it operates at full-rate speed, any skew episode might increase jitter in the output signal. The current mirrors of the two halves of the circuit do not share the same reference due to symmetry considerations in the design of the layout. Shunt inductive compensation was used at the supply node with the inductors L1, creating peaking at higher frequencies, increasing the bandwidth of the stage. This stage utilizes 8% of the total power dissipation.

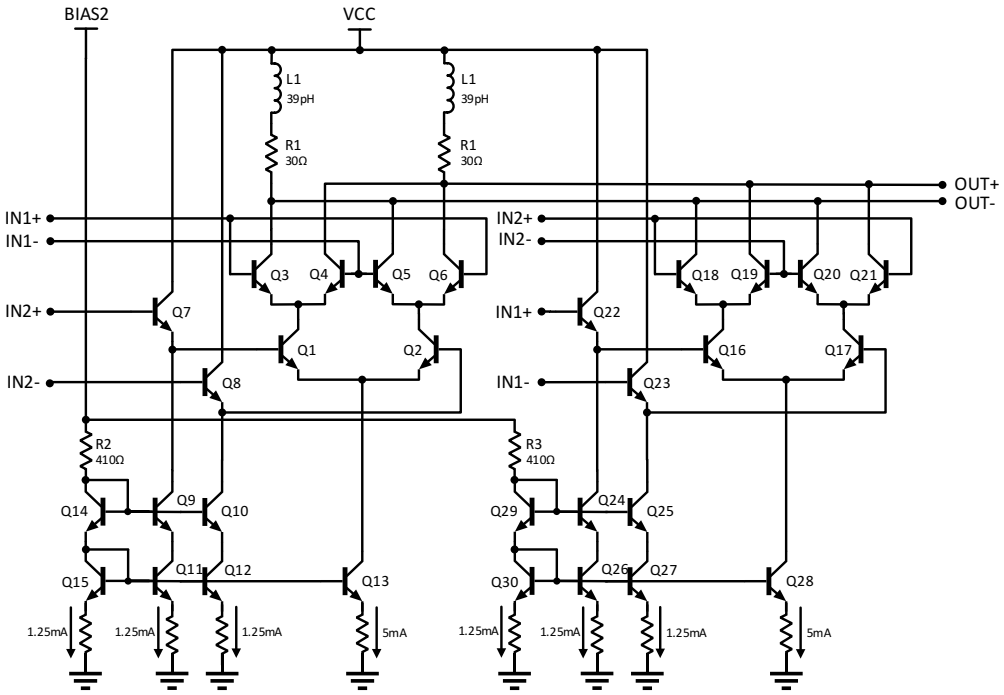


Figure 5.27: Schematic of the full-rate XOR gate (asynchronous).

The design of the remaining stages are described as follows. The clock buffers (schematic depicted in Fig. 5.25) use a conventional open-collector differential pair topology, as the load resistors are placed at the termination of the transmission lines in the star node (as sketched in Fig. 5.22). The voltage reference utilized to the current mirrors of both clock buffers is "BIAS3". The clock buffers absorb 16% of the total power dissipation of the circuit. The buffer stage, represented as the last stage in the signal path in the block diagram, is implemented as two-stage amplifier comprised by an emitter follower and a typical emitter-coupled logics (ECLs) differential pair with collector resistors carefully chosen for broadband output matching. This stage utilizes 8% of the total power dissipation. Inductors with a value of 75 pH were added in series to the output pads to improve output matching at high-frequencies (as seen in Fig. 5.23).

5.2.4 Measurement Results

Characterization of the PRBS7 generator was performed through on-wafer measurements. Firstly, time-domain measurements were performed to demonstrate the maximum data rate of the PRBS7 generator and the eye-diagram quality of the output signal. A VNA Rohde & Schwarz ZVA67 was configured to generate two continuous-wave signals, one at half-rate and the other at one fourth of the data rate. The first, with a signal power of 4 dBm, was used as the required single-ended clock, which is then converted to a differential clock with the internal balun included in the chip. The second port was set as the reference of the sampling oscilloscope Keysight DCA-X 86100D, used to characterize the output signal. The two oscilloscope sampling heads have bandwidth up to 60 GHz. They are also connected directly to the differential RF-probe to avoid the usage of RF cables, minimizing signal degradation. Fig. 5.28 presents the eye-diagram when generating a PRBS7 at 100 Gb/s. The differential output voltage is approximately 600 mVpp. In this condition, a 50-GHz clock is provided to

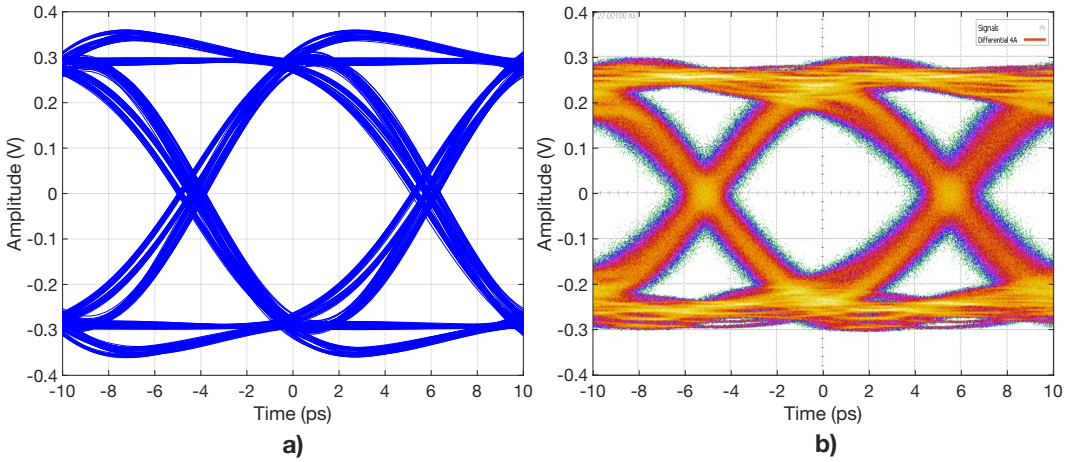


Figure 5.28: a) Simulated differential output eye-diagram at 100 Gb/s. b) Measured differential output eye-diagram at 100 Gb/s. The SNR has a value of 7.94 dB, the eye width is 7.63 ps, the eye height is 289 mV and the jitter rms value is 501.6 fs. The acquisition count number is 505.

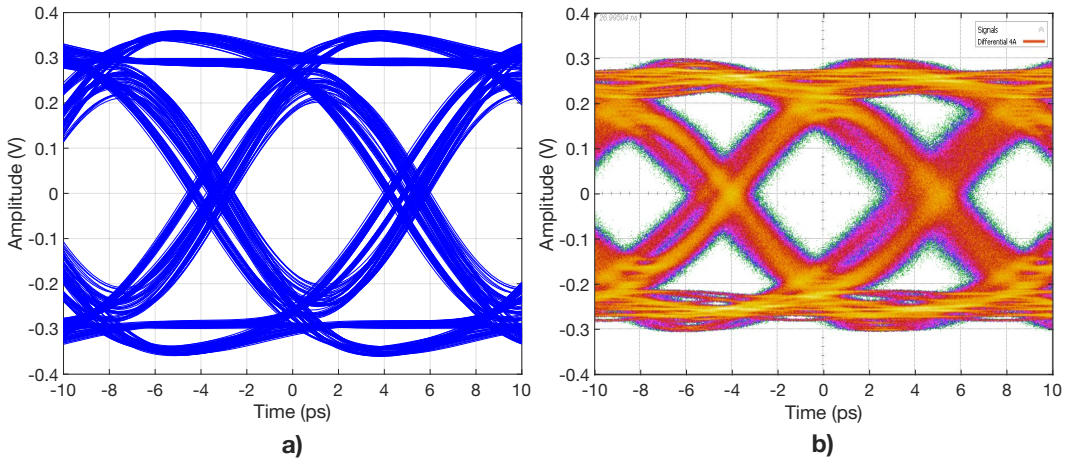


Figure 5.29: a) Simulated differential output eye-diagram at 115 Gb/s. b) Measured differential output eye-diagram at 115 Gb/s. The SNR has a value of 5.58 dB, the eye width is 4.97 ps, the eye height is 197 mV and the jitter rms value is 677.6 fs. The acquisition count number is 560.

the chip and the precision time-base reference frequency of the oscilloscope is 25 GHz. The maximum data rate generated by the circuit is 115 Gb/s. The corresponding eye-diagram is shown in Fig. 5.29. In the VNA, the ports were set to 57.5 GHz for the clock frequency and 28.75 GHz to the precision time-base reference of the oscilloscope. For comparison, the simulation results are also depicted in the same figures. In order to approximate the simulation test bench to the measurement setup, a third-order Butterworth filter with cut-off frequency of 60 GHz was applied to the simulated output signal. The measured and simulated eye-diagrams are in good agreement.

Thereafter, the frequency of the signal provided to the oscilloscope was changed to 900 MHz and connected to the trigger input. The clock frequency for the IC was set to a value 127 times higher (114.3 GHz). In this way, the repetition in the oscilloscope would occur for the complete PRBS length, thus displaying the complete pattern instead of the eye-diagram. This measurement result is shown in Fig. 5.30. A complete pattern of 127 bits is marked in the figure. To further validate the generation of a PRBS7, one of the sampling probes of the oscilloscope was disconnected and replaced by the connection to a spectrum analyzer Rohde

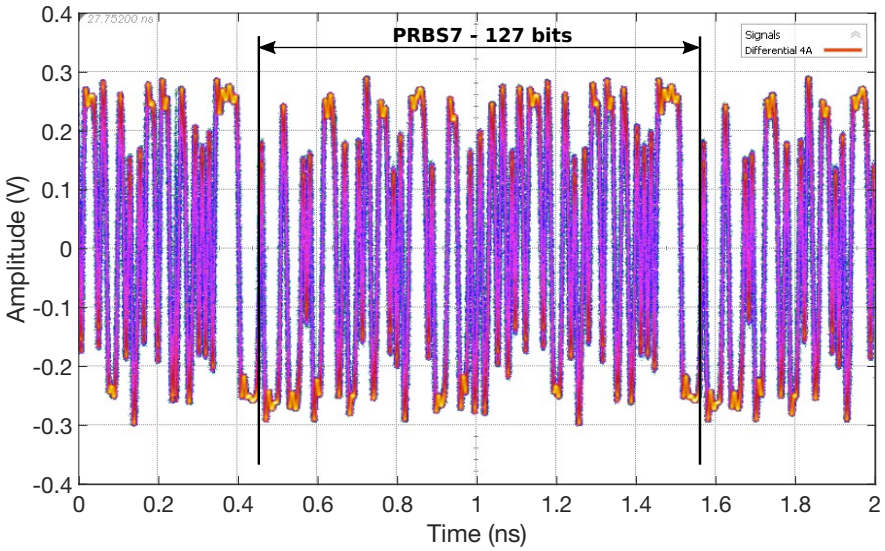


Figure 5.30: Measured differential output signal, showing the data pattern of the generated PRBS at 114.3 Gb/s.

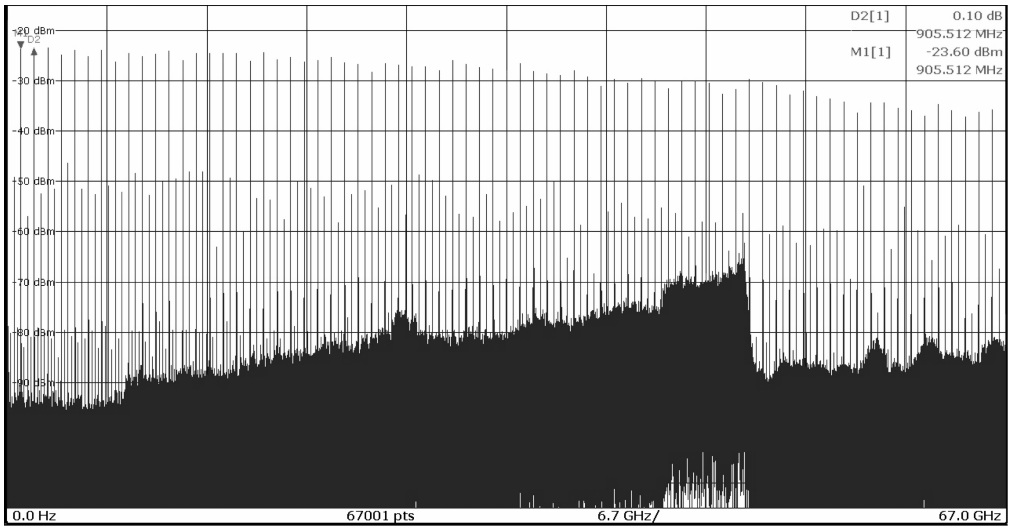


Figure 5.31: Measured spectrum of the output pattern at 115 Gb/s with tone spacing of 905.512 MHz.

& Schwarz FSW67 to perform frequency-domain measurements. The measured spectrum when the circuit is operating at 115 Gb/s is shown in Fig. 5.31. The spectrum is displayed up to 67 GHz, which is the maximum available span of the spectrum analyzer. The difference between frequency tones is measured and displayed in the figure. As expected, with a sequence length of 127 bits and a data rate of 115 Gb/s, the tone separation is 905.512 MHz.

Performance comparison with state-of-the-art designs is summarized in Table 5.2. The circuit here presented achieves the highest data rate (115 Gb/s) with the lowest power dissipation of 0.7 W. It is also the generator with the fastest data rate and lowest power dissipation among the generators with a pattern length of 2^7-1. Moreover, to compare the power dissipation with other works that provide longer patterns, a figure-of-merit (FoM) is calculated by dividing the power dissipation by the binary logarithm of the sequence length (N), divided by the maximum bit rate. The presented generator achieves a record efficiency of 0.87 pJ/b.

Table 5.2: Comparison of State-of-the-art PRBS Generators

Ref.	Technology	f_T (GHz)	Length	Data rate (Gb/s)	Power (W)	FoM (pJ/b)
[98]	0.13 µm SiGe BiCMOS	150	2^{31}-1	80	9.8	3.95
[100]	0.35 µm SiGe BiCMOS	200	2^7-1	100	1.5	2.15
[94]	0.13 µm SiGe BiCMOS	300	2^{15}-1	80	1.7	1.42
[95]	InP HBT	290	2^7-1	100	0.955	1.36
[93]	0.35 µm SiGe BiCMOS	200	2^{11}-1	80	1	1.14
This work	**0.13 µm SiGe BiCMOS**	**300**	2^7-1	**115**	**0.7**	**0.87**

5.2.5 Summary

A 2^7-1 PRBS generator fabricated in a 0.13 µm SiGe:C BiCMOS has been proposed. A modified half-rate topology was followed to achieve high-speed at low power consumption. Time-domain measurements at 100 Gb/s and 115 Gb/s were performed to validate the maximum bit rate of the circuit and to evaluate the quality of the output eye-diagram. Frequency-domain measurements were also carried out to verify the generated sequence length of 2^7-1 bits. The chip occupies an area of 0.64 mm^2. The total power dissipation of the IC is 700 mW with a record FoM value of 0.87 pJ/b.

6

Summary and Outlook

In this thesis, new designs to improve the performance of electro-optical transmitters by making use of advanced manufacturing processes in SiGe BiCMOS technology have been presented. An essential element in the transmitter is the driver, since it delivers and amplifies the voltage amplitude required by the Mach-Zehnder modulator (MZM). Various transmitter scenarios have been considered, in which different driver designs were investigated in order to comply with the described targets, regarding bandwidth, data-rate, linearity, power dissipation, input and output matching. All designs have been characterized and compared to state-of-the-art implementations.

Firstly, the linearity of the differential pair amplifier was investigated, more specifically the THD performance in the amplifier for different gain settings and biasing conditions. THD is an important aspect in broadband circuits for optical communications. Thus, the design considerations needed to improve linearity while keeping power dissipation as low as possible were studied. An overview of different driving topologies for MZMs was also provided. While focusing more specifically on the segmented topology, a co-simulation environment was implemented to enable a full simulation of the electro-optical transmitter.

A monolithically integrated segmented linear driver and modulator in EPIC 0.25 µm SiGe:C BiCMOS technology was presented, which is the first described in the literature. In order to drive the available depletion-type Si MZM at high speed, the transmitter module incorporated a long modulator and a segmented driver topology to apply constant voltage amplitude. Electrical measurements to demonstrate the linearity of the driver were performed, showing THD below 5%. The linearity of the transmitter was also demonstrated performing electro-optical measurements of PAM-4 modulation format at 20 Gbaud (40 Gb/s) and 25 Gbaud (50 Gb/s). A second generation of this transmitter module was reported as well. Frequency-domain measurements demonstrated the increased bandwidth of the driver, approximately doubling the 6-dB bandwidth value to 40 GHz due to the cascode amplifier topology and the improvement in the MZM with two additional implants. Electro-optical measurements of PAM-4 modulation format up to 30 Gbaud (60 Gb/s) were performed, demonstrating a speed improvement in the new version, and transmission over 60 km of SSMF up to 112-Gb/s was achieved with a BER measured below 10^{-3} with a simple FFE-based DSP equalizer.

Thereafter, a 4-Vppd driver design in 0.13 µm SiGe:C BiCMOS technology was presented, suitable to 25-Ω TWE-MZMs. To overcome the increased current consumption due to the lower load impedance, a topology that could reduce the supply voltage was proposed. A bandwidth of 30 GHz enabling data-rate operation up to 40 Gb/s were demonstrated. The total power dissipation was 1.1 W per channel, resulting in superior power efficiency in comparison with other modulator drivers with comparable data rates. Subsequently, another modulator driver, fabricated in a 0.25-µm SiGe:C complementary BiCMOS technology, was implemented. This design features the highest ratio of output power to power dissipation in comparison to other state-of-the-art driver implementations at comparable data rates, with an efficiency of 6.4%. Such high power efficiency has been achieved by making use of an H-bridge topology taking advantage of the availability of the pnp HBTs which were utilized at the output stage. Operation at up to 28 Gb/s with output amplitude of 3 Vppd was demonstrated. Finally, using the fastest 0.13 µm SiGe:C BiCMOS technology, a PAM-4 driver for TWE-MZMs was designed. A topology of a single stage amplifier together with reactive components was selected to achieve high-speed 4 Vppd output voltage. S-parameters measurements were performed to characterize the driver in small-signal for LSB and MSB signal paths, demonstrating 3-dB bandwidth of 40 GHz. Time-domain measurements up to 50 Gbaud (100 Gb/s) were also performed to verify the PAM-4 signal generation.

Finally, a linear driver for optical modulators compatible with data-rates above 100 Gb/s was implemented in a 0.13 µm SiGe:C BiCMOS technology. High-bandwidth has been achieved by implementing a distributed amplifier topology in a differential manner. Differential and single-ended S-parameters measurements were performed to characterize the driver in small-signal, demonstrating 3-dB bandwidth of 90 GHz. To demonstrate the large signal capability of the driver, time-domain measurements were performed with OOK signals up to 64 Gb/s with output amplitude of $4\,V_{ppd}$ and up to 120 Gb/s with output amplitude of $3\,V_{ppd}$. Furthermore, measurements with PAM-4 signals were also performed up to 45 Gbaud (90 Gb/s). The total power dissipation of the IC is 550 mW. Additionally, a 2^7-1 PRBS generator fabricated in the same technology has been described. A modified half-rate topology was selected in order to achieve high-speed at low power consumption. Time-domain measurements at 100 Gb/s and 115 Gb/s were performed to validate the maximum bit rate of the circuit and to evaluate the quality of the output eye-diagram. Frequency-domain measurements were also carried out to verify the generated sequence length of 2^7-1 bits. The total power dissipation of the IC is 700 mW with a record FoM value of 0.87 pJ/b.

The ICs for optical transmitters here presented show different techniques suitable for the development of future products in optical communications which will allow the transmission of higher data rates in a power efficient manner. Although the presented solutions are in the context of circuit-level techniques on the driver side, new technological advancements are expected, enabling better integration of electronics and photonics. Furthermore, new system-level solutions applied to the modulation formats and to the signal recovery are expected to improve too, allowing more efficient bandwidth utilization in the transmission channel.

List of Publications

First Author

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