Intermodulation Distortion in GaN HEMT

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আমার ভাইয়ের রক্তে রাঙানো একুশে ফেব্রুয়ারী, আমি কি তা ভুলিতে পারি ?

Being inspired by submitting the thesis on Bengali new year eve (1st Baishakh 1416 - 14th Apr. 2009), I dedicate this work to the martyrs of the language movement day – 21 Feb 1952, Dhaka, Bangladesh.*

**21st February – UNESCO international mother tongue day.*

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Abstract

This work treats intermodulation distortion performance of GaN-HEMT high-power transistors. A detailed study on the physical parameters influencing third-order intermodulation distortions is carried out, based on the large-signal model and on physical device simulation. Devices are characterized in terms of linearity by setting up a sophisticated measurement system. Among others, an electronic fuse is used at the drain side to avoid catastrophic failure during measurement. The bias-dependent transconductance characteristic is identified as the dominating source for intermodulation distortion in GaN HEMTs, while drain-source capacitance and access resistances have only minor influence. The corresponding physical parameters governing the transconductance behavior are determined and optimized structures for high linearity are proposed. Besides characterization and analysis of conventional designs, a novel device architecture for very high linearity is presented. Finally, performance of GaN HEMTs within a hybrid amplifier configuration is shown and the combination of high power, high linearity, and low-noise characteristics is highlighted.

Kurzfassung

Diese Arbeit behandelt das Verhalten von GaN-HEMT-Hochleistungs-Transistoren in bezug auf Intermodulations-verzerrungen. Die Grundlage bildet eine detaillierte Untersuchung des Einflusses der verschiedenen physikalischen Parameter auf die Intermodulationsprodukte 3. Ordnung, die auf dem Großsignalmodell und auf physikalischen Bauelementesimulationen beruht. Zur Charakterisierung der Linearität der Transistoren wurde ein komplexes Messsystem aufgebaut, bei dem u.a. an der drainseitigen Versorgungsquelle eine elektronische Sicherung implementiert ist, die die Zerstörung des Messobjekts bei kritischen Betriebszuständen verhindert. Als dominierende Ursache der Intermodulations-verzerrungen in GaN-HEMTs wurde die arbeitspunktabhängige Charakteristik der Steilheit identifiziert, währenddessen Drain-Source-Kapazität und Kontaktwiderstände nur geringen Einfluss haben. Die physikalischen Parameter, die das Steilheitsverhalten bestimmen, werden ermittelt und optimierte Strukturen for hohe Linearität vorgeschlagen. Neben der Charakterisierung und der Analyse von konventionellen Designs wird eine neuartige Baulelementearchitektur für sehr hohe Linearität vorgestellt. Abschließend wird das Potential von GaN-HEMTs in einer hybriden Verstärkerstruktur gezeigt und die resultierende Kombination aus hoher Leistung, hoher Linearität und niedriger Rauschzahl demonstriert.

Contents

1 Introduction

Modern wireless communication systems are improving day-by-day and offering new services such as video telephony, internet access, high quality audio, video transfer etc. All these applications require high-speed data transfer. To provide services to the increasing numbers of customers and to meet the demand of high-speed transmission, mobile industry keeps on migrating one generation to other. Transferring high data rate means high frequency carrier, higher transmission bandwidth, and complex modulation techniques.

This increasing service quality demands low cost, compact, wideband, and efficient and linear power amplifiers. In addition to mobile phone services there are many other applications where a linear amplifier is required. Some of these applications are satellite communication, navigation system, anti-collision radar, wi-fi and many other wireless data communication modules.

In table 1, frequency allocation and approximated power range of commonly used wireless devices are shown.

In first-generation cellular standards such as advanced mobile phone system (AMPS), an analogue modulation scheme was used. As this modulation had constant envelope, no significant linearity requirements were necessary for handset PA. The efficiency of the system was very low as well. However, for base-station, still there were some linearity requirements. In second-generation systems i.e, the global system for mobile communications (GSM), cell capacity was increased to a great extent by using digital modulation technique and sophisticated digital signal processing (DSP). There were two types of

multiple access techniques implemented namely time division multiple access (TDMA) and code division multiple access (CDMA). The TDMA-based system has become the most widely used mobile system. A constant envelope signal was still used, but, some linearity requirements were needed due to power ramping for a transmitter time slot. This reduced the efficiency slightly, but since the PA is on for only 1/8 of the time, the importance of PA efficiency over the total operating time was reduced to a significant degree and very good operating times were achieved in GSM handsets. However, this does not hold for base stations.

In third-generation systems such as wideband code-division multiple access (WCDMA) or universal mobile telephone

TABLE 1.1
STANDARDS & ALLOCATED RF FREQUENCY BANDS

Standard	Freq. Band (GHz)	Average Transmitted Power
GSM-900/1800 (DL)	0.935 - 0.960 1.805 - 1.880	10-20 Watts
UMTS (DL)	2.110 - 2.170	5-10 Watts
WLAN 802.11a	5.725 - 5.850	50-250 mW
Wi-Fi	2.400 - 2.484	1 Watt
Bluetooth	2.40 - 2.484	0-20 dBm
UWB	3.10 - 10.60	-40dBm/MHz
Satellite	8 - 10	-
Automotive Radar	76-77	6-20 dBm

Transmitted power are typical values, which may differ from application to application.

system (UMTS), operating times comparable to those available in second-generation systems present a serious challenge, and current applications are not capable of achieving these. From a PA point of view, the difficulties in modern telecommunications systems arise from spectral efficiency.

With rapidly increasing numbers of users and their demand of higher data transmission rate, the available frequency spectrum is heavily crowded. To cut the cost in expensive frequency spectrum, one must transmit the maximum amount of data using the minimum bandwidth. This can be achieved using complex and sophisticated modulation techniques. For example, UMTS utilizes a bandwidth-efficient modulation, usually Quadrature Phase Shift Keying (QPSK), and therefore is capable of providing higher bit rates per unit bandwidth. Typically UMTS systems are expected to deliver peak data rates of up to 2.4 Mbps with average data rates of 300 kbps. Unfortunately these kind of modulation schemes lead to wide, dynamic signals that require highly linear amplification. As a result, signal distortion must be minimized in order not to interfere neighboring channels and to use the frequency spectrum efficiently. Therefore, linearity of RF power amplifiers becomes one of the most and probably the most important parameter to be considered for modern communication.

PA linearity is normally achieved with high back-off or external linearizer circuits. High back-off means less efficiency and oversized amplifiers, which results in high production cost and environmental disaster in long run due to lower efficiency. External linearizer means extra effort and complex circuits, which are costly and cumbersome. Moreover, increasing the modulation scheme complexity and

bandwidth to enable fast data transfer often renders linearization schemes ineffective.

On the other hand, increasing demand from wireless industry made the semiconductor industry to improve the technology and find new materials. The first amplifying transistor based on semiconductor was invented by the team of William B. Schockley in 1947 at Bell Lab and later shared his Nobel Prize with his team members John Bardeen and Walter H. Brattain [1][2]. The invention of the first transistor based on germanium became the basis for the electronic age. Since then, semiconductor industry kept on growing. Silicon based devices were very successful and mostly used in past decades. Silicon has low electron mobility therefore it was not easy to make high frequency devices with this technology. GaAs (Gallium Arsenide) came with a great hope for high frequency application as it has high electron mobility. InP (Indium Phosphide) technology was also introduced for very high frequency applications. These materials are often called compound (III-V) semiconductor as they are compound of two material from 3rd and 5th column of periodic table. GaN (Gallium Nitride) is a new material in this III-V community. It has potential to become the most important semiconductor material since silicon. Although GaN was first introduced as a material for blue laser, recently high frequency and high power RF applications found GaN to be a very promising material. It has large band-gap, very high sheet carrier density and high mobility. Taking advantage of these combinations GaN offers high breakdown voltage, high current density and robustness. Besides its problems with defects and traps it has been proven by this time one of the best material capable of delivering highest density of power up to mm-wave [3][4]. This technology has a growing interest in RF community.

At the Ferdinand-Braun-Institut, power HEMTs and MMICs are developed based on GaN technology. As a new material, this technology is undergoing its evolution era. The technology is not yet commercialized in mass scale. As modern broadband communication concerned, it is very important to characterize the linearity of these amplifying devices. The purpose of this thesis was to characterize these devices in terms of linearity, specifically intermodulation distortion. In more detail, it covers the following aspects.

- Development of a reliable measurement system to characterize high power GaN HEMTs in terms of linearity.
- A thorough investigation to identify the causes of intermodulation distortions in GaN HEMTs. This includes simulation, systematic comparison and analysis of measurement data.
- To propose methods for linearity improvement at the device level.
- Linear amplifier design with GaN HEMT technology.

1.1 Organization of the thesis

This thesis consists of seven chapters and conclusions. It is comprised of three main parts. The first part is the introductory part that includes general understanding of distortion phenomenon and characterization methods. It also includes a general description of GaN HEMT technology. The second and core part is about the systematic analysis of devices and improvement of device architecture in terms of linearity. The concluding part presents performance of GaN HEMT device within an amplifier. In the following the organization of the chapters is given.

Chapter 1 – *Introduction*, starts with the motivation and the goal of this thesis along with some general information to understand the necessity of this thesis. General information includes different wireless standards and an introductory overview on different semiconductor technologies to realize wireless communication circuitry. A comprehensive guideline and understanding the organization of the thesis is the main focus of this chapter.

Chapter 2, *Nonlinear Distortions*, revises the basics of distortion mechanism in active amplifying devices. Nonlinear characterization methods and commonly used figure of merits in terms of linearity are presented here.

In **Chapter 3,** *GaN HEMT*, we have briefly introduced the AlGaN/GaN HEMT technology. This technology is a relatively new technology in semiconductor industry. Ferdinand-Braun-Institut (FBH) has its own process line to fabricate GaN HEMTs and MMIC based on this technology.

Chapter 4, Measurement *and Characterization*, presents the measurement system for GaN HEMT characterization used for this work. As the characterized GaN devices are high power devices, it was necessary to develop a reliable measurement system which is capable of handling such high power and perform accurate measurements.

In **Chapter 5,** IMD *Sources in GaN HEMT*, we examine device level distortion sources in GaN HEMTs. Analysis based on large-signal model and measurement data are presented in this chapter. A model-based analysis captures the mechanism of nonlinear distortions in GaN HEMT. This chapter also includes a measurement based analysis where a number of devices with changed physical parameters were compared.

Chapter 6 – *Enhancing Device Level Linearity* addresses the physical parameter optimization and innovative methods to improve GaN HEMT linearity at the device level. It was shown that optimized physical parameter and operating condition is the key of linearity enhancement. This chapter also presents an innovative device architecture for highly linear devices.

Performance of GaN HEMTs within an amplifier is presented in **Chapter 7** – *GaN HEMT as Linear Amplifier*. This chapter also includes some concepts and considerations for designing practical linear amplifiers based on GaN HEMT.

Finally, – **Conclusion,** concludes the thesis with a comprehensive summary and outlook.

2 Nonlinear distortions

In a perfect world, communication would be transfer of information across a given medium without any loss or interference to other users. In reality, the communication channels add unwanted signals to the desired information. These signals include random noise and distortion. Random noise is not correlated with the information, whereas distortion generation is a strong function of the information carrying signal [5]. Distortion can be generated from any part of the communication subsystem e.g., circuit components or from the medium. These subsystems include antennas, amplifiers, mixers, digital-to-analog and analog-to-digital converters. The amplifying device is the heart of electrical communication system. These active devices or amplifiers are usually quasi nonlinear to strongly nonlinear. Distortion generated as a result of the nonlinear characteristics of active devices is the scope of this chapter.

This chapter reviews the relevant results and theories related to the distortions in amplifying devices, especially HEMTs, which were important in the development of this thesis.

2.1 Linearity figure of merit for active devices

Usually the following terms are commonly used as figure of merit for linearity of amplifiers or amplifying devices.

- Gain compression/$P_{-1\ dB}$ point
- Harmonic distortion
- Phase distortion
- Intermodulation distortion

- IP3 /TOI (Third Order Intercept Point).
- ACPR (Adjacent Channel Power Ratio)/ Spectral regrowth.
- EVM (Error Vector Magnitude).

Actually, they are related to each other and will be clarified in the following sections.

2.2 Distortions in amplifying devices

Active devices such as transistors are usually used to amplify electrical signal. In a perfect linear system these devices would amplify the signal with a constant gain up to infinite input power. In reality these devices have a transfer characteristic as shown in fig. 2.1 in comparison to perfect linear amplifier.

As pointed in the figure, gain drops after a certain input or output power. When the gain is 1 dB less than the linear gain the corresponding output power is called P_{-1dB}. In ideal case the output power is considered only at one frequency which is the input signal frequency. Due to the nonlinearity, the amplifier generates additional frequency components at the multiples of this signal frequency are called harmonic distortion.

The input vs. output curve can be expressed by Taylor series as shown in eq. 2.1.

$$V_{out} = a_0 + a_1.V_{in} + a_2.V_{in}^{\ 2} + a_3.V_{in}^{\ 3} + ...a_n.V_{in}^{\ n} + ... \quad (2.1)$$

Let us consider an RF amplifier amplifying a pure sine wave ($x = A\sin\omega_1 t$). The output signal consists of the amplified signal and higher harmonics. The nearest harmonic product occurs at the double of the signal frequency and thus can be filtered out easily.

Figure 2.1 Input vs. output curve of a typical non-linear device and corresponding frequency spectrum for monochromatic input signal.

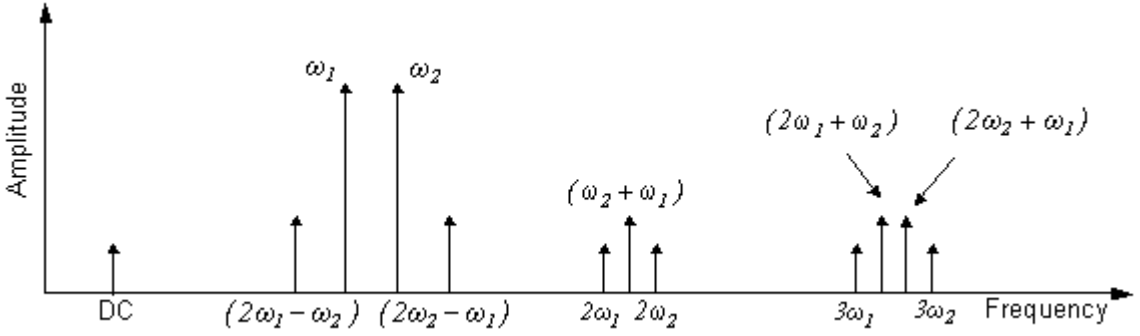


Figure 2.2 The output spectrum of a device excited with a two-tone signal (up to third order mixed products i.e., n≤3).

TABLE 2.1

LIST OF THE OUTPUT FREQUENCY COMPONENTS OF A NONLINEAR SYSTEM EXCITED BY A TWO-TONE SIGNAL (N≤3)

Frequency Components	Magnitude	Phase
dc	$a_0 + a_1 \ .A^2$	…
ω_1 , ω_2	$a_1 A + \frac{9}{4} a_3 \ .A^3$	*Sin*
$2\omega_1 , 2\omega_2$	$\frac{1}{2} a_2 \ .A^2$	*-Cos*
$3\omega_1 , 3\omega_2$	$\frac{1}{4} a_3 \ .A^3$	*-Sin*
$(\omega_1 + \omega_2) , (\omega_2 - \omega_1)$	$a_2 \ .A^2$	*-Cos, Cos*
$(2\omega_1 + \omega_2) , (2\omega_2 + \omega_1)$	$\frac{3}{4} a_3 \ .A^3$	*-Sin*
$(2\omega_1 - \omega_2)$	$\frac{3}{4} a_3 \ .A^3$	*"Sin"* if , $\omega_1 > \omega_2$ Otherwise *"–Sin"*
$(\omega_1 + 2\omega_2) , (\omega_1 - 2\omega_2)$	$\frac{3}{4} a_3 \ .A^3$	*"Sin"* if, $\omega_2 > \omega_1$ Otherwise *"–Sin"*

** The phase of a term is defined by its behavior at t=0.*

For a modulated signal, however, this does not work anymore because mixing products are generated which fall in the signal band and it is impossible to filter them out. These mixing products are called intermodulation distortion products. The simplest modulated signal is a two-tone signal ($x = A_1 \sin\omega_1 t + A_2 \sin\omega_2 t$), where ω_1 and ω_2 correspond to two closely spaced frequency components, which is similar to an amplitude-modulated signal.

A two-tone signal consists of two closely spaced sine waves. A simple two-tone signal having the same amplitude A can be written as: $x = A(\sin\omega_1 t + \sin\omega_2 t)$

The next step is to replace V_{in} in eq. (2.1) by the two-tone signal and to do some mathematical calculations to have a spectral representation. Fig. 2.2 shows the resulting frequency components considering the terms up to third order in eq. (2.1), table 2.1 adds details on the respective spectral lines.

However, as distortion products are concerned, power devices have more than one nonlinearity mechanism and the components generated from different mechanism interact [6]. The third order distortion components at $(2\omega_1 - \omega_2), (2\omega_2 - \omega_1)$ are of special interest because they fall inside the signal band. They are commonly referred to as third-order intermodulation products (IM3). $(2\omega_1 - \omega_2)$ is called "IM3L" and $(2\omega_2 - \omega_1)$ is called "IM3U" where "L" and "U" stand for Lower and Upper sideband. If the input signal is increased by a factor x then IM3 products would increase by x^3. That means in a flat gain operation, if the input and output fundamental signal amplitude is increased by 1 dB, the third-order components grow by 3 dB. If we imagine that we could increase the input signal amplitude further and further while maintaining this slope, at some point the IM3 will meet the Pout curve. This point is defined as third-order intercept point, often abbreviated as IP3 or TOI. This point is a point derived by extrapolation. A real amplifier will reach saturation far below this power level. The IP3 has been the most widely used measure for defining device linearity. Intercept points of any order can be calculated by a single RF measurement when applying the following formulas:

$$IP_n\ [\text{dBm}] = Pout_{(fund.)}\ [\text{dBm}] + \frac{(Suppression)_n}{(n-1)}\ [\text{dB}] \tag{2.2}$$

where,

$$(Suppression)_n\ [\text{dB}] = Pout_{(fund.)}\ [\text{dBm}] - Pout_{(IM_n)}\ [\text{dBm}]$$

For IP3, one obtains the specific result

$$IP_3\ [\text{dBm}] = Pout_{(fund.)}\ [\text{dBm}] + \frac{Pout_{(fund.)} - Pout_{(IM3)}}{2}[\text{dB}] \tag{2.3}$$

This calculation is valid only if the measurement is performed carefully within the linear operation regime ensuring that the distortion products are well above the noise level. However, the amplifiers or devices do not behave the same for each input power level and therefore IP3 is often debated to be the linearity figure of merit. If one measures the output powers and the IM3 powers of the tones for the complete operating power range of a device then the real nonlinear behavior of the device of full operating range can be estimated. The real difference between the output power of the fundamental tone and IM3 tone is called carrier to intermodulation (C/I) ratio. Thus the IP3 for a single power level is usually redefined as TOI (Third order intercept) by the following relation derived from eq 2.4.

$$TOI\ [\text{dBm}] = Pout_{(fundamental)}\ [\text{dBm}] + \frac{1}{2}\cdot\left(C/I\right)[\text{dB}]$$
$$\text{where,}\left(C/I\right)[\text{dB}] = Pout_{(fundamental)}\ [\text{dBm}] - Pout_{(IM3)}\ [\text{dBm}] \tag{2.4}$$

2.3 IMD characterization of the devices

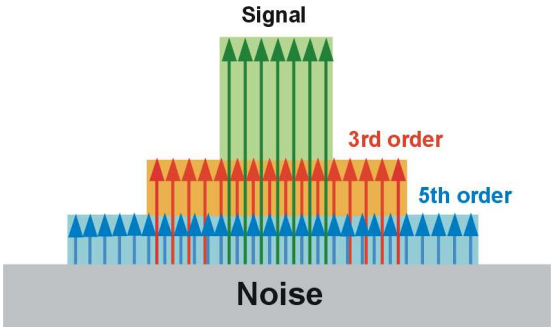
There are various ways of intermodulation distortion characterization. The most common and classical one is to measure

the intermodulation distortion products by exciting the device with a two-tone signal as explained in section 2.1. Two-tone signal is amplitude modulated like signal with suppressed carrier. As mentioned earlier, today's mobile communication usually use a wideband digitally modulated signal. Such a signal can be imagined as densely spaced multiple tones. If the device is excited with a multitone signal then a broad spectrum of the distortion product can be seen. This gives a more clear idea how a device would behave under wide-band excitation. However, a more realistic test can be done if a real world wide-band signal. The amplifier can be excited according to users wish (i.e. the modulation scheme, number of channel etc.) and the output spectrum can be observed. Fig. 2.3(b), shows a typical output spectrum of an amplifier, amplifying wideband modulated signal and fig. 2.3(a) shows the mechanism of growing sidebands from multitone point of view. If the channels are defined, then one can measure the ratio of total power in the signal and the power in the side band. This measurement is called adjacent channel power ratio (ACPR).

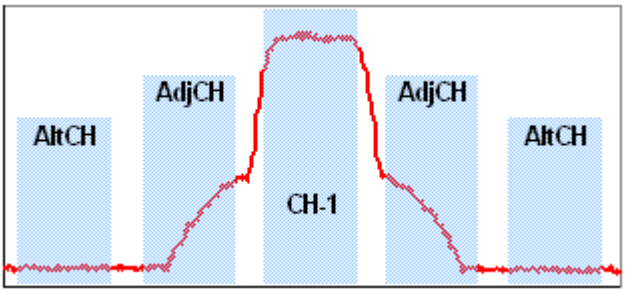
2.3.1 Demodulated signal characterization

If the analyzer is equipped with a digital demodulator and synchronized with the signal generator, then one can demodulate the signal at the output of the amplifier and analyze the amplified signal quality. Constellation diagram, error vector magnitude (EVM), Bit Error Ratio (BER), code domain analysis etc. are some examples of more advanced and signal specific figures of merit. A constellation diagram is a representation of a signal modulated by a digital modulation scheme such as quadrature amplitude modulation or phase-shift keying. It displays the signal as a two-dimensional scatter diagram in the complex plane at symbol sampling instants. In a more abstract sense, it represents the possible symbols that may be selected

by a given modulation scheme as points in the complex plane. Measured constellation diagrams can be used to recognize the type of interference and distortion in a signal.



(a)



(b)

Figure 2.3: The output spectrum of a device excited with (a) multitone signal (b) wide band signal where the abscissa and ordinate correspond to frequency and power accordingly.

A signal sent by an ideal transmitter or received by a receiver would have all constellation points precisely at the ideal locations. Due to distortion of the signal, the actual constellation points deviate from the ideal location. An error vector is a vector in the I-Q plane between

the ideal constellation point and the point received by the receiver. Its average length (or magnitude), defined as the Euclidean distance between the two points, is the EVM.

The error vector magnitude is equal to the ratio of the power of the error vector to the root mean square (RMS) power of the reference. It is defined in dB as:

$$EVM\,(\mathrm{dB}) = 10\log_{10}\left(\frac{P_{error}}{P_{reference}}\right) \tag{2.5}$$

where P_{error} is the RMS power of the error vector, and Preference is the RMS power of ideal transmitted signal.

EVM is defined as a percentage in a compatible way with the same definitions:

$$EVM\,(\%) = \sqrt{\frac{P_{error}}{P_{reference}}} \times 100\,\% \tag{2.6}$$

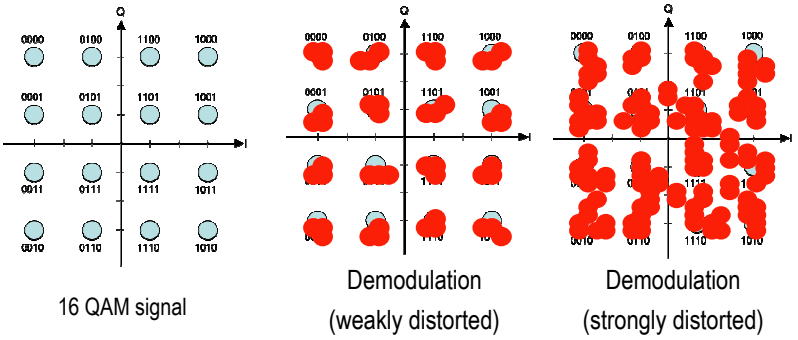


Figure 2.4: Constellation diagram (Defined and received signal shown in I-Q plane)

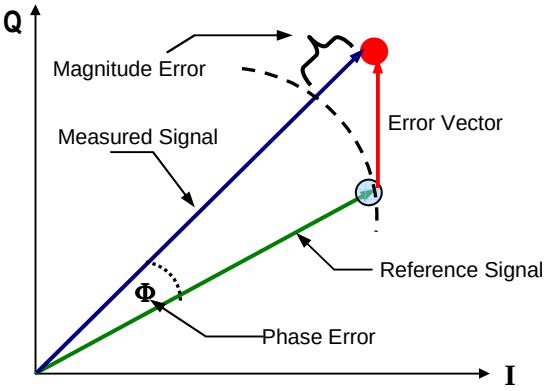


Figure 2.5: Vector components defining error vector magnitude (EVM)

Bit error ratio is the ratio of the number of bits incorrectly received to the total number of bits sent during a specified time interval.

2.4 Comparison of devices in terms of linearity

As one of the main goal of this work is to minimize the intermodulation distortion at the device level, it is very important to compare the intermodulation distortion of devices in a reliable way. The absolute linearity of a device is very difficult to determine and hence to compare. This is because the linearity of device depends on many factors such as bias, termination impedance etc. One of the most simple and classic figures of merit is to compare IP3. However IP3 is not able to show the complete picture as most of the practical

application consider large signal operation of active device. A complete power sweep of two-tone measurement can show the linearity behavior over whole power spectrum. In this case it is enough to compare only C/I ratio. Some publication compare C/I ratio over the input power which does not show a real comparison if the devices have difference in gain. Therefore C/I must be compared as a function absolute output power.

Devices with different architecture may have different pinch-off voltage and transconductance profile. Therefore, it is important to fix the bias point properly. Sometimes the comparisons are done at constant V_g and V_d which is valid if both the transistor have similar pinch-off condition and transconductance profile. This is not usually the case for different epitaxial design. A better way is to compare them at the same drain current.

Termination impedance is another factor to consider. As long as the transistors have the same periphery and technology we assume similar mismatch at 50 Ω. It is safe to measure the devices in the well defined 50 Ω environment. To be consistent, in this work we have compared linearity of the devices with equal periphery at defined drain bias (voltage and current) in a 50 Ω environment.

3 GaN HEMT

GaN is the youngest and one of the most promising materials in III-V semiconductor industry. GaN was introduced as the first material to produce blue laser. Later it was also successfully adapted to produce devices for RF applications. As a III-V material system the GaN and AlGaN pair has the same advantage as other III-V materials to create a heterojunction. The GaN/AlGaN system is often referred to have similarity with GaAs/AlGaAs. However, recent findings show that the 2 DEG (two dimensional electron gas) formation process is quite different in these two technologies.

Therefore, it is important to understand the mechanism of GaN HEMT operation, in particular, the 2DEG formation in AlGaN/GaN heterostructures. In this chapter, the basic HEMT and specially GaN HEMT operation are sketched, together with a short description on the FBH process. This is important to understand the mechanism of intermodulation distortion in GaN HEMTs.

3.1 Basic HEMT operation

The HEMT operation relies on using high mobility electrons generated from the hetero junction of with a highly doped n-type AlGaAs layer and an undoped GaAs layer. The electrons generated in the n-type AlGaAs drop completely into the neighboring GaAs, because the hetero-junction created by different band-gap material forms a steep canyon in the GaAs side where the electrons can move quickly without colliding with their donor atoms.

However, the GaN HEMT 2DEG formation is different from that in GaAs. Due to the presence of a strong polarization field across the AlGaN/GaN heterojunction, a 2DEG with sheet carrier density up to 10^{13} per square centimeter is achieved without any doping [7]. Ibbetson *et al.* [8] found that surface states act as a source of electrons in 2DEG. The built-in static electric field in the AlGaN layer induced by spontaneous and piezoelectric polarization leads to an altered band diagram and the electron distribution of the AlGaN/GaN heterostructure. Basic GaN HEMT structure and band diagrams are shown in fig. 3.1.

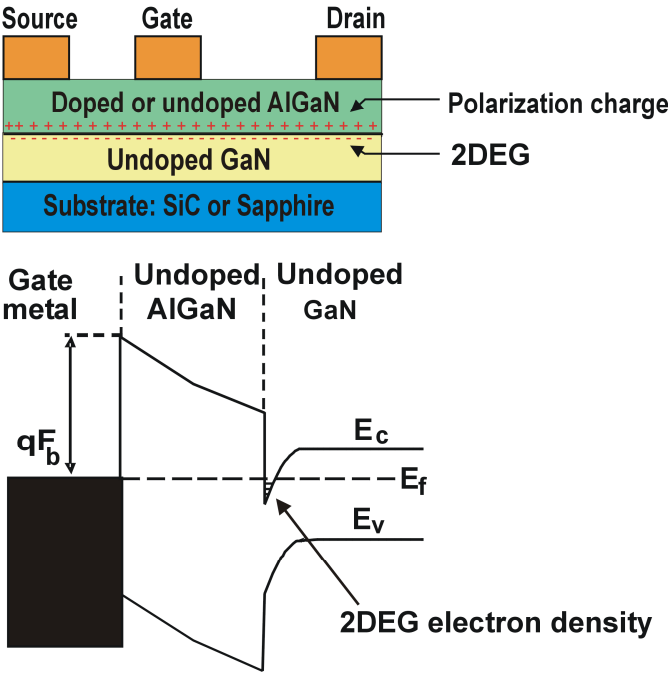


Figure 3.1: Basic structure and its band diagram AlGaN/ GaN HEMT .

3.2 GaN material properties

The material properties of GaN, makes it a very attractive material to produce high power microwave devices in comparison to other available semiconductor materials.

Wide band-gap and high breakdown electric field allows high terminal voltage operation of the transistor based on GaN technology. High electron mobility ($\mu = 1200$ to 1500 cm^2/Vs in 2DEG) and saturation velocity determine its high frequency characteristics. The high sheet carrier density (ns $\approx$ $1x10^{13}$ cm^{-2}) of two-dimensional electron gas (2DEG) in AlGaN/GaN HEMT maintains high current densities. The high voltage operation with high current density makes GaN devices the best high power devices so far. GaN grown on SiC has a very good thermal conductivity which is very important for

TABLE 3.1

SEMICONDUCTOR MATERIAL PROPERTIES

Material properties	Si	GaAs	6H-SiC	4H-SiC	GaN
Band gap (eV)	Indirect	Direct	Indirect	Indirect	Direct
	1.1	1.4	3.0	3.2	3.4
Electron mobility (cm^2/V-s)	1500	8500	250	700	800
Breakdown voltage (MV/cm)	0.3	0.4	2.4	2.0	3.3
Saturation velocity ($x10^7$ cm /s)	1.0	2.0	2.0	2.0	2.7
Thermal conductivity (W/cm-K)	1.5	0.5	4.5	4.5	1.3
Operating temperature (℃)	300	300	> 500	> 500	750
Melting temperature (K)	1690	1510	> 2100	> 2100	>1700
Johnson figure of merit (α V_{br}^2 x V_{sat}^2)	1	11	260	180	760

power transistors to be reliable and durable due to increased channel temperature at high power operation. Experiments showed that a GaN transistor can work at high ambient temperature such as 300°C while silicon transistors stop working at about 140°C [19].

3.3 GaN Device fabrication

At FBH, a complete GaN HEMTs process line is available covering the entire spectrum from epitaxy to packaging. GaN layers are grown on SiC wafers. A detailed discussion on the fabrication process is out of the scope of this thesis. However, a brief review is given in the following based on [10], which clarifies the basics of the devices investigate during this work.

3.3.1 Substrate

The choice of the suitable substrate is a key issue for GaN HEMTs. GaN is so far not commercially available as substrate crystal. The first successful epitaxial layers of GaN were grown on Sapphire. Sapphire is cost effective but has low thermal conductivity. Therefore, SiC gained recently more popularity with improved technology to grow defect free GaN layer. SiC has very good thermal properties, which is nearly 10 times more than that of the sapphire. Also, the reduced lattice mismatch between SiC substrate and GaN improves the epitaxial quality and reduces dislocations densities. As SiC is still expensive, other thermal management techniques such as flip-chip mounting technology have been used to make AlGaN/GaN HEMTs on sapphire competitive. GaN HEMTs have also been produced using freestanding GaN substrates [9]. However, this is very expensive, have lower thermal conductivity and till now limited to laboratory. Recently, GaN on Si substrate has also been commercialized. Si wafer is 100 time cheaper than SiC and allows to use larger wafer size.

3.3.2 Basic GaN Process technology at FBH

The $Al_{0.25}Ga_{0.75}N$/GaN HFET structures used for this work were grown by MOCVD on 2″ SiC wafers. The epitaxy growth sequence started with the deposition of a 500 nm thick AlGaN layer followed by a 2.7 µm thick highly insulating GaN buffer layer, 3 nm $Al_{0.25}Ga_{0.75}N$ spacer, 12 nm Si-doped $Al_{0.25}Ga_{0.75}N$ supply layer, 10 nm $Al_{0.25}Ga_{0.75}N$ barrier. A 25 nm thick AlGaN layer on the top of the GaN buffer forms a two-dimensional electron gas (2 DEG) at the AlGaN/GaN interface.

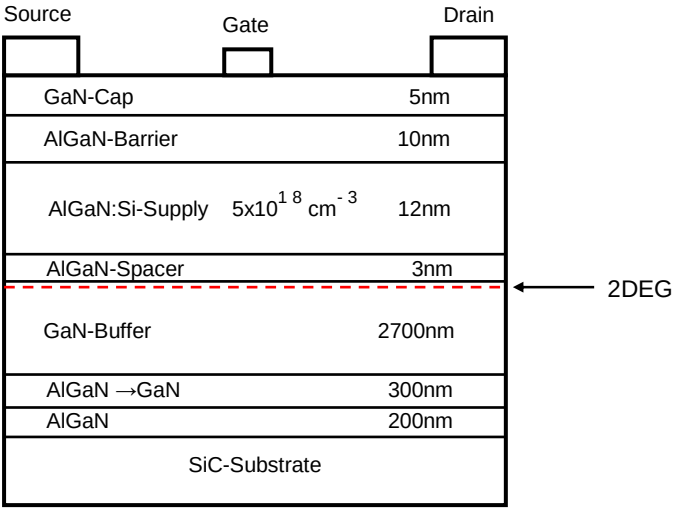


Figure 3.2: Basic FBH epitaxial layer structure for GaN HEMT

The $Al_{0.25}Ga_{0.75}N$/GaN HEMT device fabrication was accomplished in eight lithography steps shown in fig. 3.3. It starts with the deposition of backside and front side Ti reflector layers (Z-layer) on

transparent wafers for ease of handling, recognition and exposure using wafer stepper layer and a 5 nm thick GaN cap layer.

The front side Ti layer is structured and alignment marks are defined by stepper lithography. A sophisticated Ti/Al/Ti/Au/$WSiN_x$ metallization scheme is employed for the fabrication of ohmic contacts (B-layer). The reflector is then removed (Y-layer) and wafers are annealed in N_2 ambient to achieve low contact resistance. Gate contacts (C-layer) are made in using Pt/Ti/Au metallization. A gate length of 0.5 μm is defined with stepper lithography.

The mesa isolation is done (A-layer) by reactive ion etching RIE ($BCl_3/Cl_2/Ar$). Gate fingers and drain fingers are interconnected (D-layer) using Ti/Au. Source pads are connected using Au air bridges in two steps. First the plating base (F1-layer) is defined using Ti/Au/Ti metal and then the air bridges are realized using Au galvanic electroplating (F2-layer).

To improve the device performance, several modification have been introduced in FBH process technology in the last years. Some important modifications are the implementation of SiN_x passivation layer. to protect the device surface from surface contamination and possible damage during device processing, an improved metallization system and implementation of fieldplate etc. Besides this, many other special modifications have been taken place for application specific devices such as low noise, high linearity, high frequency applications etc. [10].

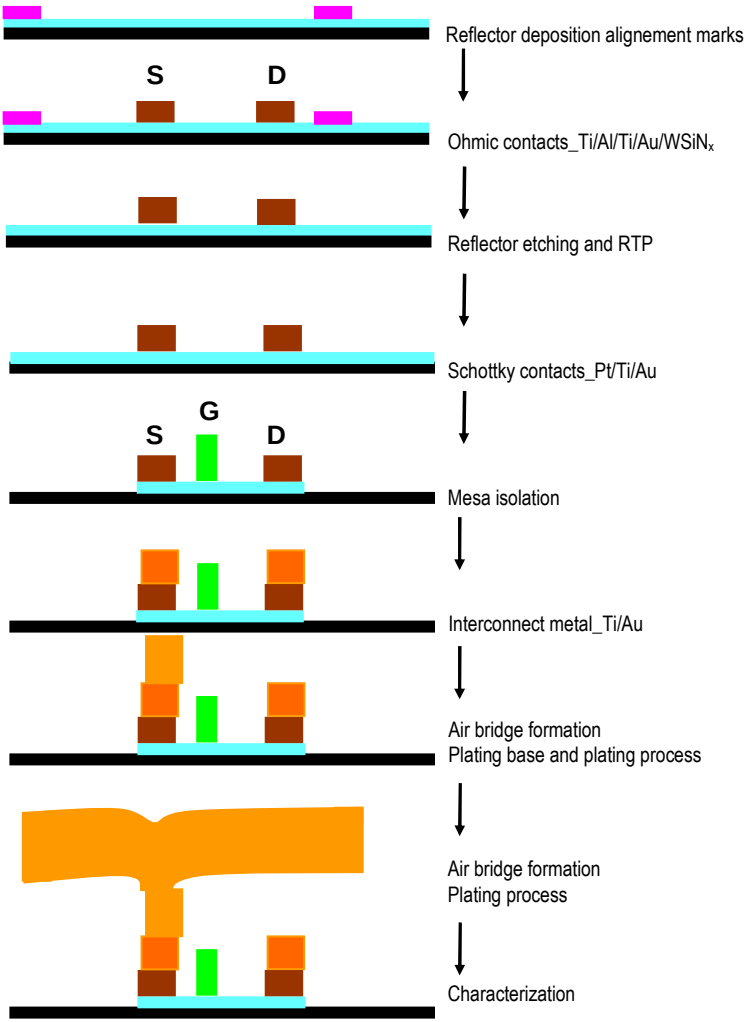
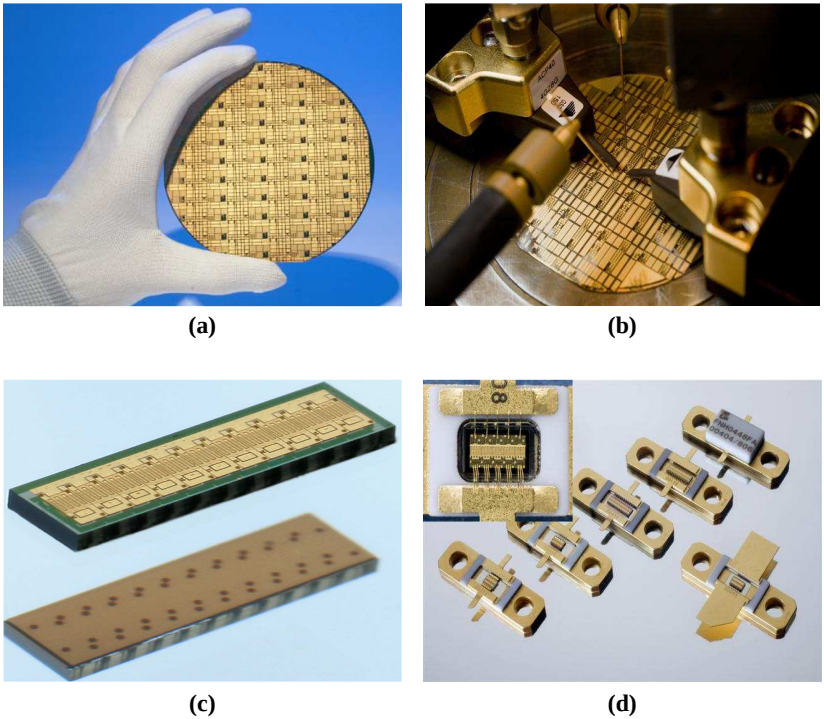


Figure 3.3: The AlGaN/GaN HEMT device fabrication steps [10].

3.4 Packaging

After fabrication and characterization on wafer, the transistors are diced and packaged in convenient metal packages. Usually the base plate (often called flange) of the package is made of gold plated copper-tungsten-alloy which shows high thermal and electric conductivity. Above the flange a rectangular Aluminium oxide (Al_2O_3) frame is placed. On the top of this layer, T-shaped metal fins are placed at the input and output side which serve as leads and as bonding area.



(a) **(b)**

(c) **(d)**

Figure 3.4 GaN HEMT packaging steps: (a) A Processed wafer , (b) On-wafer test (c) Diced device, (d) Device bonded in package

The diced chip is normally soldered at the middle of the package and bonded at the gate and drain side of the device. Source connected to the flange either by via holes or by bonding. After bonding the device into a package, it is sealed by a ceramic lid. In fig. 3.4, different steps from wafer till packaging is shown.

4 Measurement and characterization

Measurement and characterization of devices is the most fundamental part of this work. Although nonlinear measurements, in particular two-tone measurements were the most important characterizations in terms of linearity, other standard measurements like s-parameter, load-pull and noise figure measurements have been performed as well. Devices were characterized on-wafer and in packaged form. Packaged devices were characterized in special test fixtures. As high power devices are concerned, the commercial non-linear measurement systems were not capable of handling the required measurements. Therefore, a customized and dedicated measurement system had to be built for nonlinear characterization using commercial equipment. The measurement system was completely automated, The control software was realized using LabView[1].

In this chapter, we will mainly present the non-linear measurement system of FBH along with the difficulties and innovative solutions for reliable characterization of high power GaN devices. In addition to that, some critical failures during measurements and the corresponding counter actions are described.

4.1 Intermodulation test setup

Usually, a two-tone test signal is generated combining the output signals of two signal-generators. This method has a few drawbacks and difficulties:

[1] LabView is a trade mark of National Instruments.

- It is very difficult to maintain equal amplitude of both tones due to the individual control of each tone. Especially, if the signals are amplified using individual external amplifiers to obtain higher driving power, problems arise due to gain differences in these amplifiers. Moreover, there might be isolation problem.
- In order to achieve stable and reproducible results, the phases of the two signals must be controlled, which is maintained only if phase-locking of the two generators is realized.
- If the signal is first combined and then amplified by a single amplifier this amplifier itself generates distortion products, which result in an incorrect measurement. In this case, the amplifier must be operated at a large power back-off, which leads often to a very expensive solution and sometimes may be even impossible.

To avoid these difficulties, modern multi-tone generators have a built-in wide-band I-Q modulator. Controlling quadrature I-Q signals at the base-band, it is possible to generate arbitrary multi-tone signals. If the two-tone signal is generated with this kind of generator, the signal is available from a single channel, which eliminates the first two problems mentioned above. However, the output power of the generator is not very high and therefore we encounter the same problem as before in amplifying the signal without distortion. As we can control the base-band I-Q signal there is a possibility to compensate the distortion of the amplifier by a proper pre-distortion of the I-Q modulation. This, of course, requires an option at the generator to control the I-Q signal externally.

Therefore, it is necessary to set up a combined system with a connection between the analyzer and the generator. One first has to measure the distortion products of the amplifier and, then based on this information, generate a pre-distorted base-band signal at the input of this amplifier so that the resulting distortion components at the output vanish. This process can be called linearization. In our case, we use an Agilent PSG (Performance Signal Generator) and PSA (Performance Spectrum Analyzer)[2] connected by GPIB to a computer.

Concept diagram of the measurement system using a multi-tone generator is shown in fig. 4.1. A two-tone signal is generated using a PSG. Next to the generator, there is an amplifier followed by an automatic attenuator. Such an automatic attenuator, also remotely controlled by the computer, is required to realize the power sweep. This is necessary because the distortion of the input amplifier is suppressed by pre-distortion as stated earlier. But this linearization holds only at a particular power level. If the power level is swept at the generator, the linearization does not remain valid for the entire sweep and it would have been necessary to perform linearization for each power value, which is impractical because of several reasons: First, linearization is very sensitive and not well reproducible. Thus, when using predetermined I-Q data from a look-up table, this may not yield the desired low distortion levels at the amplifier output. This is because the linearization depends on many factors like amplifier gain, phase, temperature etc. Second, the correction is achieved by an adaptive optimization algorithm and therefore time consuming. Moreover, the DUT (Device Under Test) must be replaced by a through at the time of new calibration.

[2] PSA (Performance Signal Analyzer) and PSG (Performance Signal Generator) are the trademarks of Agilent Technologies.

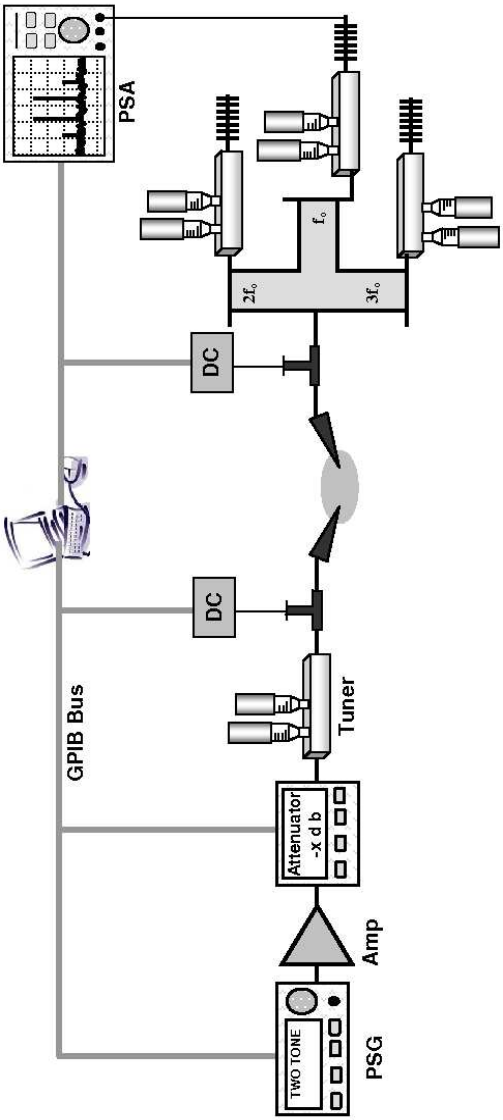


Figure 4.1 Measurement setup for intermodulation distortion characterizations.

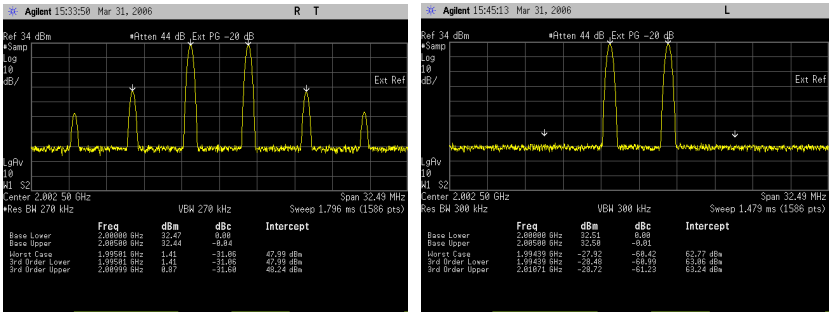


Figure 4.2 Test signal before and after linearization. Signal tone spacing 5 MHz and linearization done on 25 MHz bandwidth

Therefore, the best idea is to perform the correction of the input amplifier at the highest possible output power and realizing the power sweep by using a step attenuator.

In fig 4.2, the test signal is shown before and after linearization. As can be seen, linearization is very effective. To do the linearization a computer algorithm is used. The software gets the distortion data from the PSA and calculates an approximate distortion parameter according to the gain of the path (PSG output to PSA input) and rotates the I-Q offset at the generator. Then the output is measured again, compared to the previous setting and an error factor is calculated. In this way, a continuous iteration is done to find the optimum pre-distortion parameters. However, one must take care of selecting the appropriate amplifier and bias-Ts.

4.1.1 The input driving amplifier

If the amplifier produces too much distortion then the software may not find a solution to linearize (and it might even be impossible on principle because the linearization concepts are limited in terms of

the distortion level they can compensate). One should use an amplifier having high dynamic range with suitable output power, reasonably low-noise properties, high-IP3 and broadband characteristics. If the amplifier is narrow-band (as, e.g., LDMOS amplifiers) it may be very difficult or even impossible to linearize them according to the aforementioned technique. In our case, we use GaAs-HBT and GaN-HEMT amplifiers. We tried *Si* LDMOS and TWT amplifiers as well but were not able to achieve satisfactory linearization even after a number of iterations.

Also, it is always better to have a single amplifier with sufficiently high output power and gain margin. If more than one amplifier are connected in series to achieve higher gain and power, it becomes difficult to linearize them due to interstage distortions.

The test signals before and after linearization are shown in fig. 4.2 for a commercial amplifier. Here the tones have 5 MHz spacing and a linearization is done on a bandwidth of 25 MHz to suppress 3^{rd} and 5^{th} order distortion components.

4.1.2 Bias-T

It is very important to select proper bias-Ts for an IP3 measurement. The bias-T must cover also the frequency range of the envelope, i.e. the tone spacing Δf. If the bias T does not pass this frequency component properly the envelope will be distorted and the measurement can be incorrect. This shows up as asymmetry between the lower (IM3L) and upper (IM3U) distortion products, which may be misinterpreted as memory effect of the device.

We have also added tuners at the input and output for device characterization at different source and load impedances. A very high quality triplexer is used at the output to separate higher harmonics

and tune them independently so that higher harmonic effects on linearity can be studied.

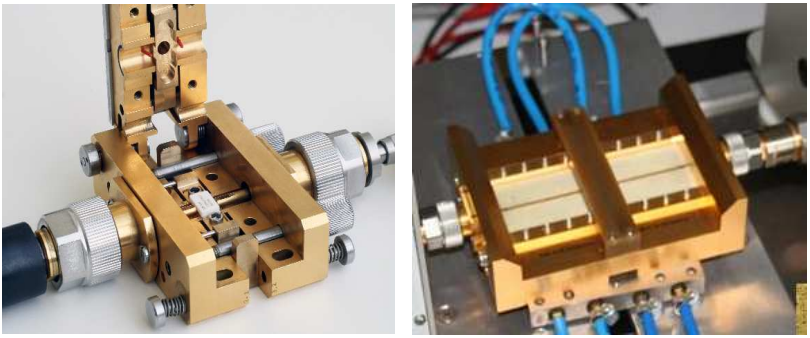
4.2 Power calibration

A power calibration is necessary to perform accurate measurements. Loss at the output network must be determined using a network analyzer or a power meter. For this purpose, output and input are connected by a thru and a power sweep is done using the attenuator. For each position of the attenuator, the power is measured taking into account the losses in the output network i.e., in the probes, the connectors, and the cable, and, if applicable, any attenuator at the input of the spectrum analyzer. The measured power is later used as the input power at the DUT for different attenuator positions.

4.3 Fixture

GaN devices fabricated on wafer are usually diced and packaged in industry standard packages. As this package adds parasitics, it is important to characterize these devices in packaged form. We have used two kind of commercial fixtures as shown in fig. 4.3 (a) and (b) for small signal and large signal characterization accordingly. We will call them *Robotron* and *ICM* fixture according to their manufacturer name. The *Robotron* fixture can be calibrated precisely at the device reference plane for small signal measurement. The device is clamped directly at the coaxial interface. The drawback of this fixture is that it cannot handle very high power. In the ICM fixture the transistor is connected to a microstrip interface and the fixture is mounted on a water cooled heat sink. This fixture is very robust and can handle more than 100 Watt CW power. Another advantage of this fixture is

that the 50 Ω microstrip lines can be replaced by arbitrary boards. It is important to measure power accurately. The low impedance presents a tuning problem for the load and source-pull measurement due to the fact that the impedances are either outside the range of the tuner, or where the tuner accuracy degrades [11]. The tuner losses increase with the increasing reflection coefficient seen from the input and output of the transistor towards the tuners. As a result, it is difficult to estimate the accurate power delivered from the device. It was observed that after measuring the whole packaged device in a standard commercial test fixture, expected power was not available. To estimate the impedance, s-parameter of the device was measured in a 50 Ω environment. Quarter wavelength transformers were designed as pre-matching networks. This means that a lower impedance transmission line directly at the device which matches input or output impedance of the transistor to 50 Ω. Having a transmission line which is much closer to the impedance level of the transistor, the amount of loss decreases and the tuner is relaxed considerably to tune the device further more accurately.



(a) **(b)**

Fig 4.3 (a) *"Robotron"* fixture and (b) *"ICM"* fixture.

4.4 Measurements

The PSA provides a third order intercept point (TOI) measurement option, which is based on the suppression formula stated earlier in eq. 2.3. This measurement has the following disadvantages:

- The whole bandwidth from $(2\omega_1 - \omega_2)$ to $(2\omega_2 - \omega_1)$ must be selected at once. Therefore, the noise level of the analyzer increases and dynamic range is decreased.

- Without performing a power sweep, one does not know whether the measurements are reliable. If the device is operated at low input power, the distortion components may not be high enough compared to system noise (i.e., close to or lower than MDS, the Minimum Detectable Signal). In this case, the analyzer takes the noise level as distortion component amplitude, which provides a totally wrong result. On the other hand, if the device is driven to the saturation region, there will be huge distortions and the single-point measurement would not satisfy the IP3 definition. In fig. 4.4, these two phenomenon can be observed at low and high input levels.

- Under some special conditions, i.e., at some particular bias-point and RF level, the device may operate in an extremely linear way, which is called sweet spot. One may take advantage of such conditions but they cannot be used as the IP3 of the device. These points are very sensitive to all parameters and sometimes even not reproducible. Therefore, performing a single-point measurement one may incidentally meet this condition, which leads to a drastically overestimation of the device linearity.

In our case, the measurement system is completely automated and computer controlled by in-house software developed using LabView. The frequency components of interest are measured individually with a very narrow bandwidth. Therefore, it is possible to detect also very low amplitudes. There is the possibility of hardware averaging and peak search to avoid possible uncertainties. DC-Sweep, RF-sweep and security measures are implemented in the program as well.

In the following we show an example of a measurement (see fig. 4.4). The DUT is a packaged high-power GaN transistor.

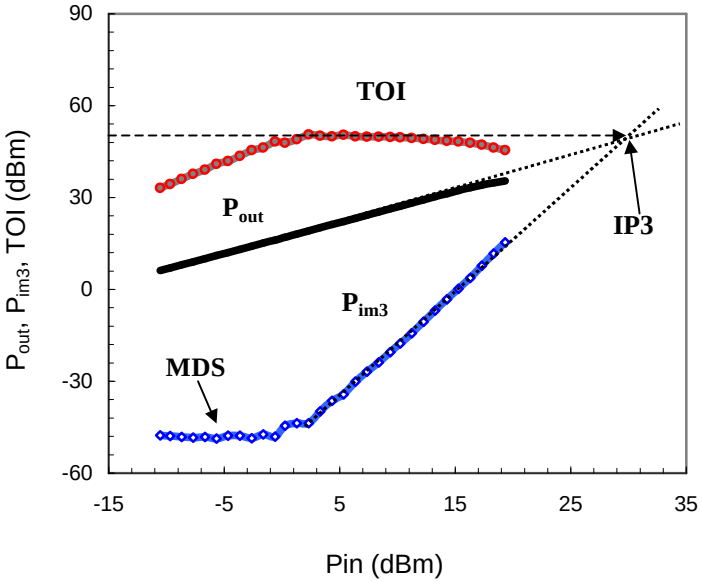


Figure 4.4 Output power, 3rd-order intermodulation power and the corresponding 3rd-order intercept point as a function of input power. The device is a packaged GaN-HEMT.

This device reaches an IP3 of about 50 dBm. To achieve good accuracy, one needs an adequate amount of linear input power. Therefore, an external amplifier was used to amplify the test signal and its distortion was suppressed as described above in order to obtain a distortion-free two-tone signal. Please notice that up to an input power of about 4 dBm the distortion components are below the MDS (Minimum Detectable Signal). This illustrates that accurate measurement of such big devices needs enough driving power. If the power of third-order distortion components does not grow according to a 3rd order rule, either there is no distortion by transfer mechanisms (this is the case for ideal linear devices such as a passive component, for instance) or the distortion components are out of measurement sensitivity. If the 3rd order distortion components show a 1st order characteristics, i.e., the curve is parallel to the fundamental power, this can be interpreted as input distortion, which might origin from the input amplifier or attenuator and is only amplified by the DUT.

4.5 Measurement safety

As very high power devices concerned, critical failure during measurements results in a catastrophic penalty. Common problems during measurements are:

- Maximum electric field within the device exceeds the breakdown field and the drain is burnt or explodes.
- Forward turn-on of the gate diode exceeds the burnout limit [58].
- Unwanted oscillation due to bad tuning or impedance matching.

Using following safety measures these critical failures can be avoided in many cases.

4.5.1 Drain safety using e-fuse

GaN Power devices are operated at very high drain voltage and they deliver high current. During large power device measurement typical DC voltage at the drain exceeds 50 V and current goes up to 10 A. Huge DC power supplies are required, with a high amount of stored energy. Therefore, quite often the current limits adjusted by the bias compliance settings reacts too slow. As a consequence, the transistors are destroyed during critical measurements and, even worse, destroys neighboring devices and other parts of the system, e.g. the probe tips. Using an e-fuse the damage can be minimized in such situations, thus protecting wafer probes, bias tees, connectors, and, as far as possible, the transistors themselves.

The DUT (device under test) is usually on-wafer device and contacted by suitable probe tips. In the following, the device is assumed to be of HEMT type.

During the measurements, current or voltage may exceed their maximum values or a failure in the transistor or at its periphery may occur due to RF and thermal stress. This will usually result in an excessive DC current into the drain which heats up the devices, burning the drain or even causing explosion in the worst cases. The proposed drain current e-fuse can avoid these types of accidents in many cases. This inexpensive solution may save a great deal of time and money and avoid loss of invaluable measurement data. DUTs and probe tips are safe from the transient DC peaks of the power supplies usually generated due to the high-energy emission of output capacitors of the power supply. Moreover, in cases of device failure, the fast

switch-off process of the e-fuse restricts the damage to its origin. Hence, the defective part can be located, which helps in detecting the sources of failure and is very important for device development.

A. E-fuse working principle:

As discussed above, the main reason of damage is a high drain current. Thus, if the drain bias is switched off very fast, the damage can be avoided in many cases. For this purpose, we need to do two things, firstly to follow the instantaneous drain current continuously and, second, to switch it off very fast and efficiently, i.e., without any parasitic DC pulse or overshooting. Fig. 4.5 presents a schematic diagram of the circuit realizing these functions. The e-fuse circuit works as follows:

The voltage across the resistor R_{m} is proportional to the drain current. This voltage is monitored and compared with a variable reference voltage V_{ref}. If the voltage drops at R_{m} is higher than V_{ref}, the flip-flop will be turned off. Then, the transistor Q_1 driven by the flip-flop will cut the drain supply of the DUT very fast. The flip-flop can be turned on or off via the front panel. After a break action, the flip-flop must be reset or switched on for further measurements. The essential feature of the e-fuse is its switching characteristic that should be fast and free from parasitic pulses and peaks. Fig. 4.6 presents the respective data, a screenshot from the oscilloscope. The current is drawn as a function of time. Switching off 10 A of continuous current takes about 150 ns. One observes that the switching is very clean in terms of unwanted pulses or peaks.

B. Measurement Examples with and without e-fuse:

In this section we will present some measurements performed with and without the e-fuse connected to the drain. The output capacitance

of common laboratory power supplies which is shown as C_{source} in fig. 4.7, is in the range of 1.000 µF to 10.000 µF. If we assume a drain voltage of 28 V, the stored energy in the power supplies reaches 0.4 to 4 W. If an e-fuse is connected, C_{source} is isolated from the DUT. Therefore, only the stored energy in the bias Tee, i.e., the energy in C_{bias} and an additional contribution generated due to the switching action are effective and can damage the DUT. A typical bias Tee has a capacitance of 10 nF to 100 nF, hence the energy stored is about 40 µW to 400 µW.

Assuming a total short resistance of 1 Ω and a total switching time of 1 µs, there is an additional switch-off energy of about 400 µWs. Therefore, depending on the actual conditions of the devices used, applying an e-fuse drastically reduces the stored energy, in the example above by a factor of 500 to 10,000.

Fig. 4.8 presents photos of a GaN HEMT measured without e-fuse before and after a catastrophic failure, which led to excessive drain current causing explosion of the transistor. As can be seen the drain side is completely burnt. Even worse, this damaged the probe tips as well. The center finger of the probe tip was simply melted and partially evaporated. This can be avoided by using the e-fuse. In the following, we will show an example.

Figs. 4.9 (a) and (b) refer to the case without e-fuse. It can be seen that the drain side of the multi-finger device is burnt completely and the damage extends till the probes causing a tip damage. In contrast, figs. 4.9 (c) and (d) present the results for a similar kind of problem when using the e-fuse. Only a minimum burn-out has taken place where only a single finger is damaged and the drain contact remains intact leaving the tip unaffected. This is important not only in order to save cost on measurement equipment but also due to the

fact that it allows better localization of the origin of the failure in within the transistor. Overall, the benefits of the quick drain fusing are obvious.

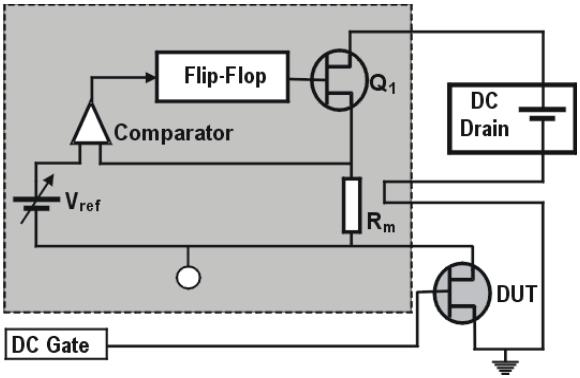


Figure 4.5 Schematic diagram of the e-fuse circuit (shaded part is the e-fuse)

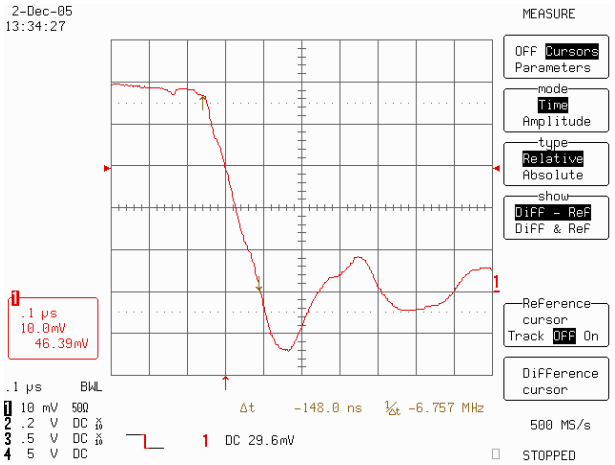


Figure 4.6 Screen shot of a switching action. Abscissa corresponds to time and ordinate corresponds to current, 50 ns and 2 A per div. respectively.

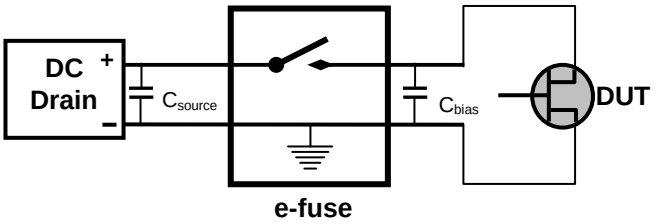


Figure 4.7 A typical RF measurement system connected with an e-fuse.

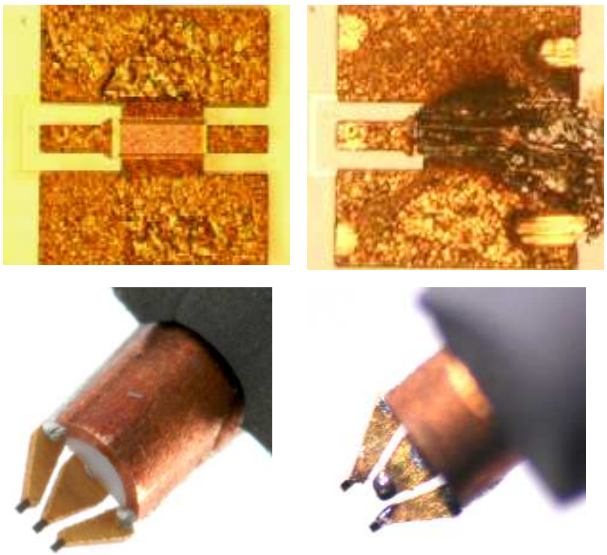


Figure 4.8 A GaN HEMT and probe tip damaged during measurement without e-fuse (right).

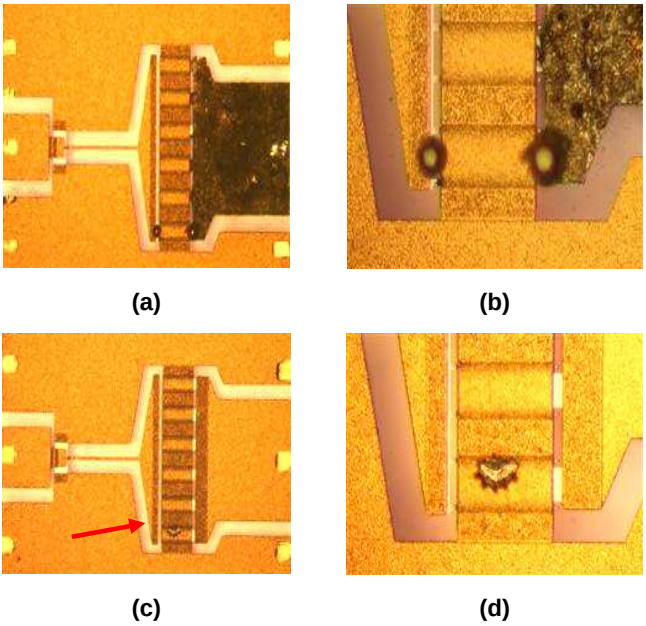


Figure 4.9 Transistor after failure during RF power measurements: without e-fuse (a) and (b); using e-fuse (c) and (d).

4.5.2 Self pinching bias-T to avoid gate turn-on and spurious oscillation[3]

This section deals with the forward turn-on and unwanted oscillation problems. We propose a simple gate bias-T for GaN HEMT measurement and circuits based on this kind of devices. This bias includes a simple series diode in the DC path that blocks any positive current from gate, in other words it restricts the gate diode of the device to operate in forward bias which is often called as forward turn-on. The new bias circuit assures a safe operating condition of

[3] Patent pending: Nr.- 08164363.7-1233

FET/HEMT transistor during forward turn-on and do not hamper or degrade normal operating performance.

The presented bias T includes a normal p-n diode in the DC path of the gate bias. This diode does not have any effect during normal operation but pinches off the device automatically during forward turn-on. We have presented different RF measurements where this gate turn-on and gate-burn occurs. Measurements with the proposed bias-T clearly show that these condition can be easily avoided and thus the device survivability can be increased.

It is important to notice that, "gate-diode" refers to the schottky diode at the gate of the device which is the internal diode of the device or the part of the device itself. The "bias T-diode" refers to the external p-n diode that is introduced at the gate DC path which is not a part of the device rather a part of bias circuitry.

A. Principle of operation:

The proposed DC bias circuit is similar to a commercial bias T that includes a simple diode restricting forward bias current at GaN FET/HEMT gate. At Normal operating conditions gate of FET/HEMT (Normally on) devices is kept at a negative voltage at a desired bias condition. At this condition a very small negative current flow towards the gate that means the gate-diode is in reverse bias. The DC source at gate which is kept at negative voltage delivers a negative current. We have observed during measurement that, with increasing RF drive at the gate, the device enters into a self biasing condition and this negative current starts increasing towards zero. When the RF drive at the gate becomes very high then the gate current tries to shift towards positive. In this operating condition the gate-diode operates in forward bias. The device cannot stand this condition and can be easily damaged.

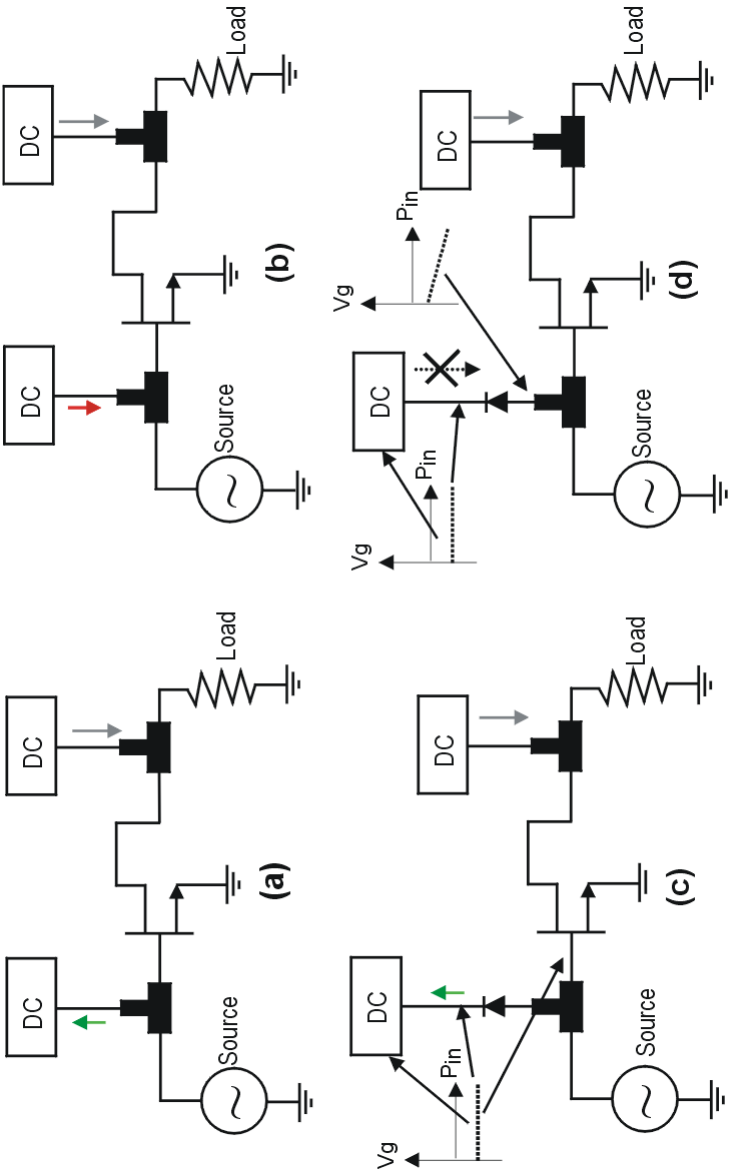


Figure 4.10 HEMT Operation in (a) and (c) normal operating condition with commercial bias and with new bias scheme; (b) and (d) under overdrive with commercial and new bias respectively.

A statistical study of our measurements shows that the most of the device damaged during RF measurement had a positive gate current. To avoid this situation we have added a simple p-n diode in the gate path. A series diode as shown in fig. 4.10 can restrict this positive current. Restricting this positive current the FET/HEMT device can be operated in a safe mode. If the diode is deployed at the gate DC path then maximum current which is allowed to flow from the DC source is zero. To fulfill this condition the voltage at gate automatically shifts towards negative (pinch-off) voltage. The principle of operation is shown in fig 4.10.

To investigate further we have tested the effectiveness of this bias scheme under very high pulsed input drive. As can be seen in fig. 4.11 (a), the voltage at the gate of the device drops according to input power and hence protect the device.

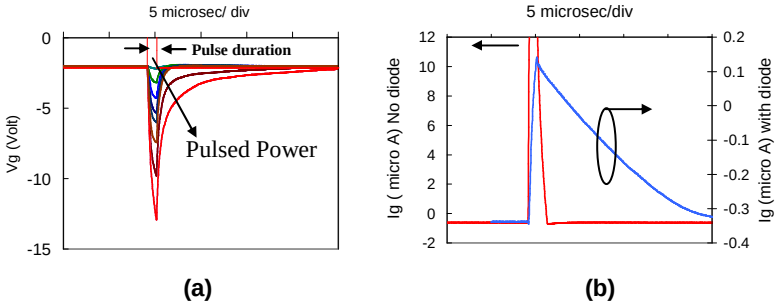


Figure 4.11 (a) Voltage at the gate of a 2x125 µm device under pulsed overdrive (Pulsed RF power applied up-to 16 Watts. (b) Gate current measured at 16 Watt with diode and at 5 Watt without diode at gate path. The device did not survive in the second case.

The voltage at the gate dropped upto –13V for an 1 μs long RF pulse of 16 Watts at the input of a small 2x125 μm device. The negative gate voltage at gate is not critical at GaN device. It is shown in [12], that GaN device survives more than –50 Volt.

B. Load Pull Measurement:

During characterization, it is necessary to operate these devices at many variations, sometimes extreme conditions (i.e. at different bias conditions and input/output impedance terminations). An inappropriate operating condition often ruins these devices unexpectedly during characterization. Specially during load/source pull measurement where load and source impedance is varied to get the optimum RF operating condition (i.e., maximum power, highest linearity, high PAE etc.), tuners scan through different complex impedances over the smith chart. Some of the tuner positions may present a critical complex impedance to the device and lead to unwanted oscillation, usually but not restricted, at very low frequency where the device has very high gain. This can be observed by a spectrum analyzer but in many cases it is too late to save the device. The proposed bias circuit can automatically pinch off the device and thus saves it.

We have compared the load pull measurement of high power GaN HEMT devices with and without diode configuration. The implementation of the diode does not degrade the performance or measurement quality in terms of power and efficiency below normal driving condition (i.e. below P_{-1} dB). However, it does affect the measurement results at saturated power. In fig. 4.11, a comparison of load-pull power sweep is shown. As stated earlier, another major problem during load-pull measurement is to meet oscillating condition which can kill the device.

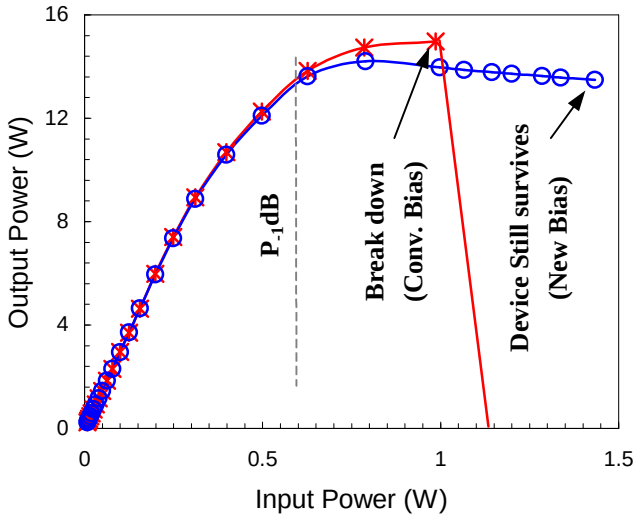


Figure 4.11 A 5x8x250 device measured at 2 GHz; V_d=24 Volt and I_d=1A.

Fig. 4.12 (a) and (b) shows such unwanted situations during harmonic load-pull where critical input/output harmonic impedances are presented to the device and thus oscillates at lower and higher frequencies accordingly without any RF drive. We have identified such impedances and reproduced them to show the effect of new bias configuration. Fig. 4.12 (c) shows the same measurement condition with the new gate bias scheme where there is no oscillation. This oscillation stopping process is an automatic self-sustaining process which is an interesting and very useful phenomenon.

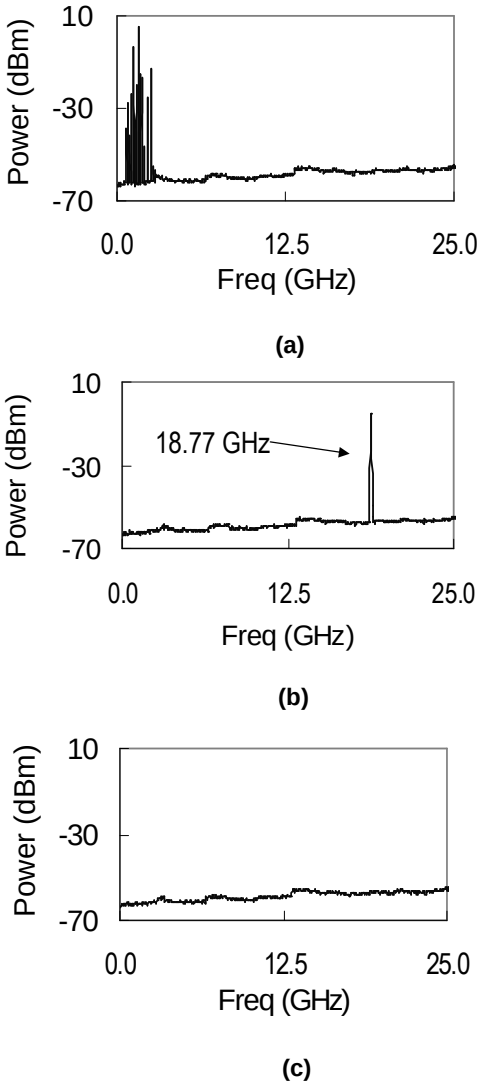


Figure 4.12 Spectrum at no RF drive (a) and (b) Unwanted oscillation condition at low and high frequencies with common bias T and unwanted termination impedance respectively, (c) shows the same measurement conditions with new bias T. No oscillation is observed. DC bias provided V_g=–2V and V_d=20V; Voltage at gate falls automatically to –7V and –4.3V for case (a) and (b) when new bias scheme is used.

As soon as the transistor meets the oscillating condition the transistor tries to draw positive current at gate. Due to the diode this is restricted and therefore the gate voltage automatically shifts towards negative values because the peak of the gate current becomes positive, i.e., current starting to flow into the gate. In this condition there is no more positive current and the gate voltage tries to recover to its original value but at the same instant the device tends to go to forward turn-on this process falls in a loop and sustain. We ran the device for several hours under this process and observed that this does not damage or degrade the transistor at least for the tested time span.

C. Linearity Measurement:

The linearity measurement system is a harmonic loadpull system which is similar to a usual load pull system. The main difference is that we use a spectrum analyzer with digital IF to measure power precisely at multiple frequency in frequency domain.

In linearity measurement the device is excited with two-tone, multitone or wideband signals. This signal has high crest factor, therefore the danger of overdrive is increased and the importance of the new bias-T is increased in this case. In fig. 4.13, a typical C/I ratio measurement is shown both with standard and new bias-T side by side. The measurements shows the pinching off effect at forward turn-on with new bias. Interestingly, as the device is operated with the new bias, at overdrive condition, C/I ratio becomes higher. This should not be misunderstood as a lineralization as the output power also falls. However, the distortion level in neighboring band remains favorable. The figure also shows the gate voltage when the pinching off process is in action. It can be seen that under normal operating condition the gate bias voltage remains constant and shifts to the negative as

overdrive takes place. The good about this behavior is that, it restricts the device to interfere neighboring channels under overdrive, for example in presence of a jammer signal at LNA.

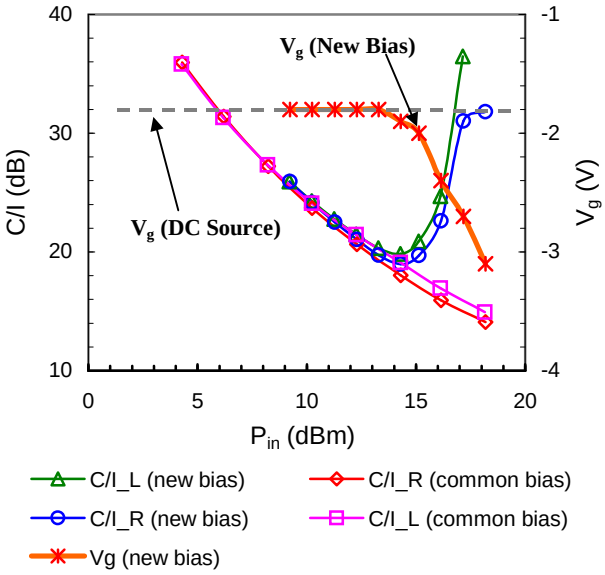


Figure 4.13: C/I ratio over input driving power measured at 2 GHz, tone spacing 10 MHz , V_d=28V,and V_g =-1.8 V (at DC source), which remains constant for common bias and changes at high drive as plotted.

5 IMD sources in GaN HEMT

In this chapter, we will present a detailed analysis evaluating the physical parameters of GaN HEMTs on the intermodulation distortion at the device level. Initially, we have performed a model-based sensitivity analysis. The purpose of this analysis was to relate IM3 characteristics to GaN HEMT device properties and to sort out the predominant effects. This was done by studying the large-signal model of a GaN-HEMT, varying the different parameters in a realistic range and quantifying the resulting changes in IM3 performance. This investigation, in contrast to experimentally based approaches, allows a systematic analysis. It was very useful to understand the mechanisms of distortion. However, not all parameters of the large-signal description can be directly related to a single physical dimension and/or physical parameter of the device. This needs additional investigations.

The second part of the analysis was measurement-based analysis. A number of devices with different architecture were measured and the measurement data were compared systematically. This comparative analysis based on the sensitivity analysis, gave an insight which device parameters can be optimized in reality.

The third-order intercept point (TOI) is used as figure of merit to compare linearity. TOI is calculated by the following formula, with $Pout_{(fund)}$ denoting output power of the fundamental tone and $Pout_{(IM3)}$ the power of the third order distortion product at output.

$$TOI\,[\mathrm{dBm}] = Pout_{(fund)}\,[\mathrm{dBm}] + \frac{Pout_{(fund)} - Pout_{(IM3)}}{2}\,[\mathrm{dB}] \qquad (5.1)$$

5.1 Sensitivity analysis based on large-signal model

The analysis is based on the Chalmers (Angelov) transistor model [13][14], modified for the application to AlGaN/GaN HEMTs on SiC developed at FBH [15]. Fig. 5.1 shows the equivalent circuit of the GaN HEMT.

The drain-current source, the gate-source and gate-drain capacitances together with the gate-source and gate-drain diodes establish the nonlinear part of the transistor model. The equations describing the transfer characteristics allow precise modeling of the tranconductance maximum, typical for HEMT behavior. The thermal part of the model is controlled by the power loss within the device and the thermal resistance. The resulting device temperature influences the values of several current and capacitance parameters. Frequency dispersion of the output conductance is included by an RF branch at the drain terminal, signal delay in the transistor by a transit-time parameter.

This behavior is translated into a set of equations and constant variables. The equations are given in Table 5.1. The parameters are determined by measurements. As the model is a physics-based model, each variable or equation can be correlated with a physical characteristic of the device. It is obvious that the parameters changes when modifying the device.

To quantify the influence of different parameters on linearity, TOI according to eq. (5.1) is calculated by sweeping each variable within a reasonable range keeping all other variables constant, at their values extracted from measurements. For this purpose, a harmonic balance simulation is performed in ADS using the above-described model in a 50 Ω environment. The initial value for the swept variable was the

realistic extracted value and the sweep was performed in a range of ±100%. (This sweeping range is considered to be the maximum range of variation that might be tuned. A large variation in the order of 10 times shows sensitivity on other parameters which is not useful from the practical point of view.) If any variable reacts strongly on TOI, this indicates that the physical parameter related to that should be a potential parameter to be optimized in order to improve the linearity. A GaN-HEMT with a gate width of 2x250 µm is considered in the following. The extracted values for this device are listed in Appendix-I. Measured distortion products in "class-A" operation were in very good agreement with simulations. Therefore, this model should give reliable information on the basic characteristics we are interested in here. At the first step of our sensitivity analysis is restricted to the large signal model level, we observed quite clear results.

Fig. 5.2 shows a statistics of the simulation results for swept variables where the vertical bar represents the deviation of TOI during sweep from the TOI of the original structure. This means: the larger the bar is, the more sensitive the variable. As can be seen, all the variables, except P1, P2, P3, showed almost no reaction on TOI. The simulation result of these interesting variables is shown in fig. 5.2 (b). On the abscissa, 0% is the extracted initial value of the variable where +100% and –100% means the same amount is added or deducted accordingly. The ordinate represents normalized TOI.

TABLE 5.1
MODEL EQUATION

Drain Current (I_{ds}) Equations	
Ids= Ipk0T(1+tanp)*tanh(alpha*Vds)*(1+lambda*Vds)*	*alpha=alphar+alphas*(1+tanp)*
X1=P1T(Vgs-Vpkm)+P2*(Vgs-Vpkm)* ^{2} *+P3*(Vgs-Vpkm)*^{3}	*Vpkm=Vpks-DVpks +DVpks*tanh(alphas*Vds)*
tanp=tanh(x)	*P1m=P1(1+B1/((e*$^{-30}$*)+cosh(B2*Vds))*^{2}*)*
Gate Current Equation	
Igs=Ij(exp(Pg*tanh((_v3-Vjg)))-exp(-Pg*Vjg))*	*Igd=Ij*(exp(Pg*tanh((_v2-Vjg))) -exp(-Pg*Vjg))*
Capacitance Equations	
*Cgs=Cgs0*th1*th2+Cgspi*	*th1=(1+tanh(P10+P11*Vgsc))*
*Cgs1=Cgs0*th11*th2+Cgspi*	*th2=(1+tanh(P20+P21*Vdsc))*
Cgd=Cgd0(th3*th4)+Cgdpi*	*th3(1+tanh(P30-P31*Vdsc))*
Cgd1=Cgd0(th3*th41)+Cgdpi*	*th4=(1+tanh(P40+P41*Vgdc))*
Th41=(1+Vgdc+P40)/((P41+(Vgdc-P40)^2*))*$^{0.5}$	*Th11=(1+(Vgsc+P10)/((P11*(1+(Vgsc-P10)*^{2}*))*$^{0.5}$
Thermal Equations	
TrefK = TambK	*Ipk0T=Ipk0*(1+Tclpk0*abs(_v5))*
TambK = Tamb + 273	*P1T=P1m*(1+TcP1* abs(_v5))*
Vtherm=abs(_v5)	*Cgs0T=Cgs0*
*Ptot=Ids*Vds*	*Cgd0T=Cgd0*
ih=_i5	*Ctherm1=Ctherm+0.0001*
TchanK = TambK + Vtherm	
Dispersion Equation	
Rc1=Rcmin+Rc/0.000001+(1+tanh((Vgs-Vpks))))	

[*] *P1* is the only co-efficient defining transconductance, *P2* makes transconductance curve asymmetrical and *P3* is responsible for the pinch-off characteristic. These constants have no effect on transconductance at V_{pk}. *P2* negative means the maximum transconductance occurs at current less than half of the saturated current. C_{gs0} and *Cgspi* will change *Cgs* . *Cgs* is addition of *Cgspi* and thermal constant multiply C_{gs0}. *P10, P11*, *P20* and *P21* affect constants th1, th11 and th2 which changes C_{gs} and similarly *P30, P31, P40, P41* decides *Cgd.*

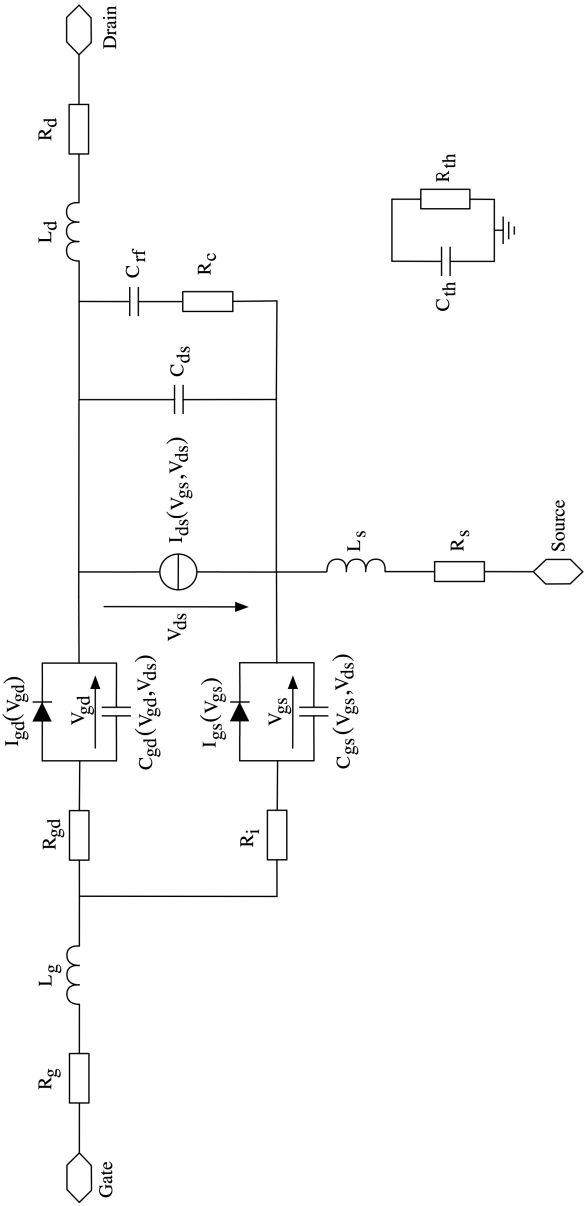


Figure 5.1 Schematic diagram of the large signal GaN HEMT model used.

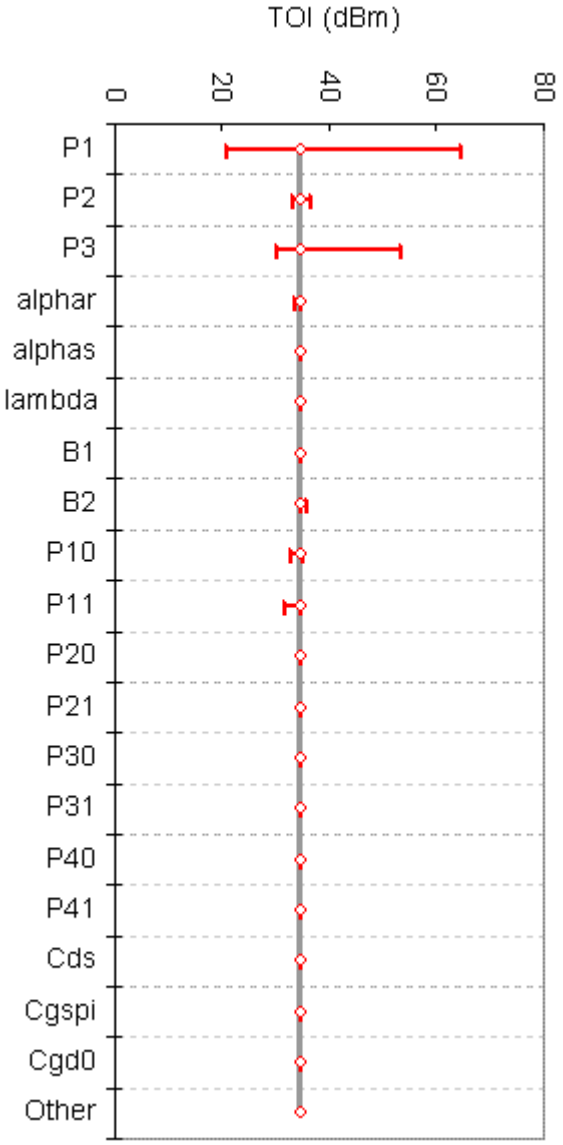


Figure 5.2 (a) TOI calculated sweeping individual variable in the range of ±100% of the extracted value. The vertical error bar shows the maximum deviation from the measured TOI.

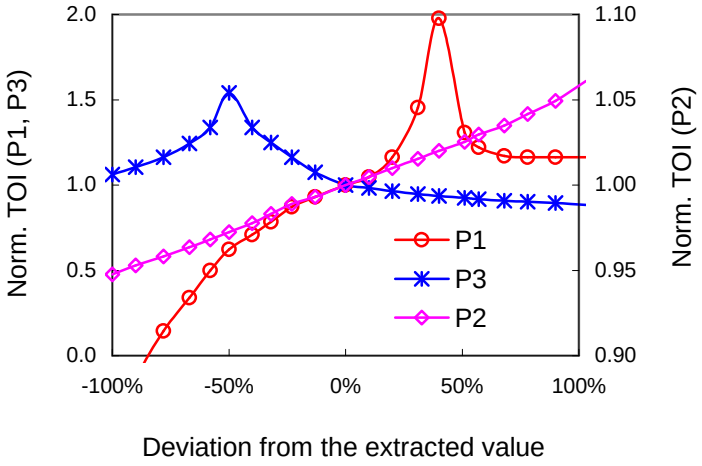


Figure 5.2 (b) Normalized TOI calculated by sweeping the transconductance related model parameters P1, P2 and P3.

The results show that the function of the drain-source current I_{ds} has the strongest influence where I_{ds} is given as:

$$I_{ds} = I_{pk}[1+\tanh(\psi)](1+\lambda V_{ds})\tanh(\alpha V_{ds}) \tag{5.2}$$

where,

$$\psi = \mathrm{P1}\times(V_{gs}-V_{pk}) + \mathrm{P2}\times(V_{gs}-V_{pk})^2 + \mathrm{P3}\times(V_{gs}-V_{pk})^3 + \ldots$$

This describes the dependence of I_{ds} on both the gate and the drain voltage. I_{pk} denotes the current and V_{pk} the gate voltage for peak transconductance at saturated drain voltages. ψ is a power series function centered at V_{pk} with variable V_{gs}. α and λ are the parameters related to the drain part. P1 is the coefficient defining transconductance, P2 makes transconductance curve asymmetrical and P3 is responsible for the pinch-off characteristics [14].

All the variables P1, P2 and P3 show strong effect on TOI. This indicates that not only the absolute value but also the shape of the I_{ds} curve as a function of V_{gs} governs linearity of the device. Compared to these variables, all other variables had almost no or very small effect on TOI.

Therefore, we will study now the behavior of I_{ds} as a function of V_{gs} in more detail. Concentrating on this dependence, eq. (5.2) reduces to eq. (5.3) (the drain voltage V_{ds} is constant and its influence is incorporated into I'_{pk}):

$$I_{ds} = I'_{pk} + I'_{pk} . \tanh\left[P1 \cdot \left(V_{gs} - V_{pk}\right) + P2 \cdot \left(V_{gs} - V_{pk}\right)^2 + P3 \cdot \left(V_{gs} - V_{pk}\right)^3 + ... \right] \quad (5.3)$$

The representation of eq. 5.2 is still strongly motivated by the modeling equations and not by the terminal behavior. Alternatively, I_{ds} can be expressed in terms of the transconductance as shown in eq. 5.4 where the drain current I_{d0} and the gate bias voltage V_{g0} are introduced. This is equivalent to small signal case.

$$\begin{aligned} I_{ds} - I_{d0} = & \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{Vg0} (V_{gs} - V_{g0}) + \left.\frac{\partial^2 I_{ds}}{\partial V_{gs}^{\ 2}}\right|_{V_{g0}} (V_{gs} - V_{g0})^2 \\ & + \left.\frac{\partial^3 I_{ds}}{\partial V_{gs}^{\ 3}}\right|_{V_{g0}} (V_{gs} - V_{g0})^3 + ... \quad .... \end{aligned} \quad (5.4)$$

This eliminates the artificial model parameters P1, P2, and P3 together with the *tanh* term and replaces them by more device-oriented quantities: The partial derivatives in eq. 5.4 can be identified as terms closely related to gm: the first order derivative of I_{ds} is the transconductance g_m, the second-order and third-order derivatives of I_{ds} are g_{m2} and g_{m3}, respectively, (see eq.5.5).

$$\left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{pk}} = g_m; \qquad \left.\frac{\partial^2 I_{ds}}{\partial V_{gs}^{\,2}}\right|_{V_{pk}} = g_{m2}; \qquad and \ \left.\frac{\partial^3 I_{ds}}{\partial V_{gs}^{\,3}}\right|_{V_{pk}} = g_{m3} \tag{5.5}$$

Since IM3 products are caused by the 3rd-order term in the transfer characteristics, g_{m3} should be the key parameter controlling IM3 and thus TOI. In order to prove this, we studied the same transistor (i.e. 2x250 µm transistor used for model based analysis) in more detail, sweeping the gate voltage while keeping the drain voltage constant and calculating the output power spectrum by HB simulation. g_m is extracted from small signal s-parameter simulations at the respective gate voltage and is differentiated to derive the higher order g_m terms. In this way we obtain TOI as well as the corresponding g_{m3} behavior for the complete range of gate voltages. This is plotted in Fig. 5.3. One clearly recognizes that the maximum TOI (and thus lowest IM3) occurs at the gate voltages where g_{m3} is near zero (note that g_{m3} denotes the third order derivative of I_{ds} with regard to V_{gs}). This means that in order to minimize IM3, we have to keep the magnitude of the third order derivative of I_{ds} as small as possible.

According to the previous findings it is clear that the second order derivative of transconductance (or, in other words, the inflection of g_m) should be as small as possible to achieve best IM3 performance. Fig. 5.3 presents a typical transconductance curve of a GaN HEMT as a function of gate voltage V_{gs}. With increasing V_{gs}, one observes a maximum behavior with two inflection points around –3 V and near -1 V. On the other hand, of course, one has to take care of the g_m level and thus output power. If transconductance or output power is too low, then TOI may be very high but the device is of no practical use.

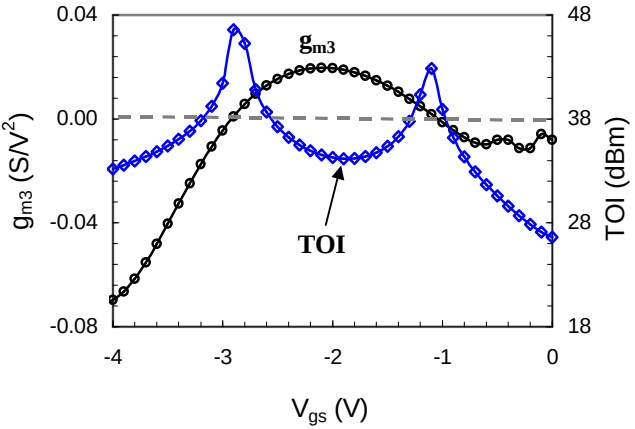


Figure 5.3 Third order transconductance g_{m3} and third order intercept TOI as a function of gate bias voltage (simulated data for typical GaN- HEMT)

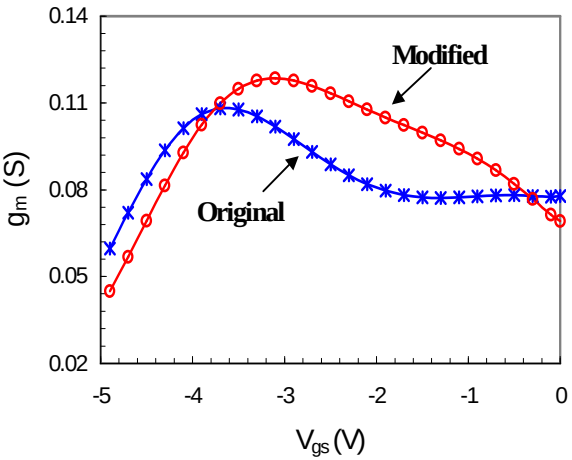


Figure 5.4 Transconductance g_m as a function of gate-source voltage V_{gs} for the original structure (see fig. 5.3) and a modified one.

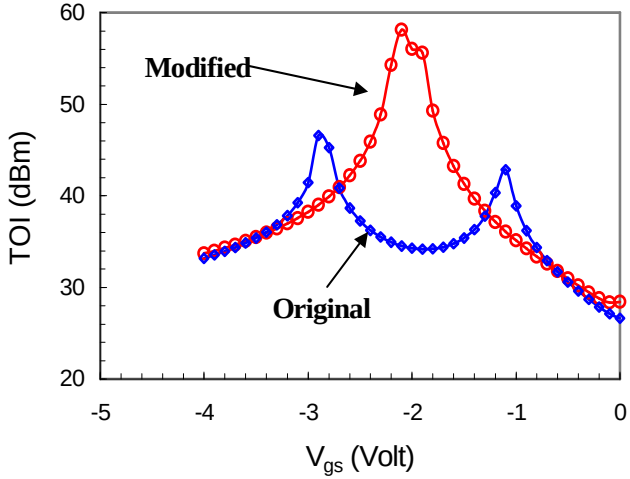


Figure 5.5 Improvement of TOI by modifying g_m : TOI vs. gate-source voltage for the two g_m corresponding to fig. 5.4.

Now, in order to tailor g_m for improving the device in terms of linearity, we optimized the three variables P1, P2, P3 at a particular gate voltage of –2 V. The g_m curve of the modified transistor is plotted in fig. 5.4 and compared with the original one. The resulting TOI is plotted in fig. 5.5 together with the original data. The peak in TOI at the target voltage of –2 V can be seen clearly, the resulting TOI exceeds that of the non-optimized structure by more than 10 dB. The respective inflection points in the g_m curve around –3V and near -1V translate into TOI maxima near –2V as expected.

In order to provide a more complete picture, fig. 5.6 presents the results of a power sweep comparing the two devices, with equal output powers

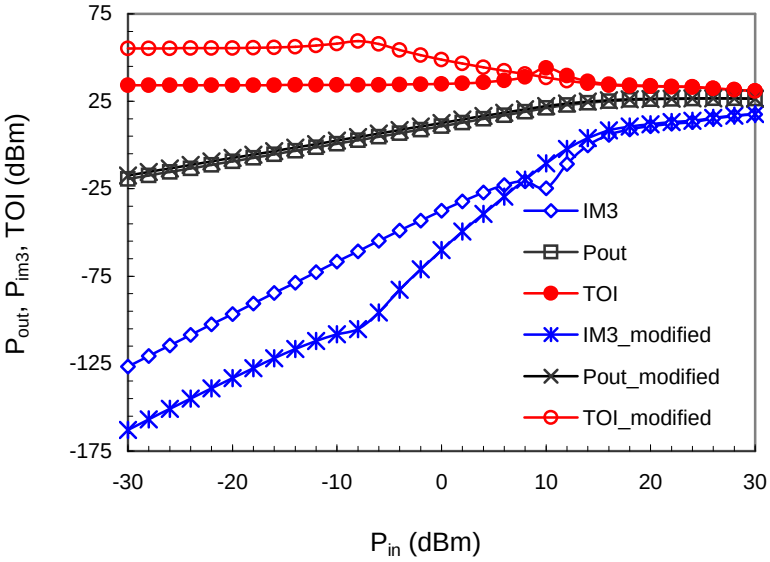


Figure 5.6 Output power P_{out}, IM3 and TOI against input power ; comparison between original and the modified device

As one can see, the modified device generates lower distortion products over a large power range which is clearly more than a sweet-spot phenomenon. On the other hand, the advantages are most pronounced for the low power range and disappear near to the saturation regime. This is because we optimized P1, P2 and P3 in a restricted range for V_{gs}. In the case of large signal input, the bias point will be shifted. Therefore, if the g_m curve is not flat in a range of appropriate size there can be a strong effect on linearity with increasing RF amplitudes.

Thus, the gate voltage range included in the optimization needs to be large enough. One should try to keep g_m constant ($g_{m3} = 0$) over a V_{gs} range as broad as possible in order to have better linearity also in case of large output powers. It should be noted that in reality P1, P2 and P3 or the corresponding g_m terms cannot be treated separately because they together form the variables determining the shape of the I_{ds} and hence the g_m curve. There is no physical tuning parameter controlling these variables independently. So designing a linear device remains tricky and one must consider aspects from epitaxial growth till layout design. But achieving a flat g_m curve remains the most important criterion for designing a linear GaN HEMT.

5.2 Measurement based analysis

We have measured and compared different devices in terms of linearity with epitaxy and architectural variation. Some layout parameters were changed in order to vary physical parameters that reflect model terms. It was observed that the measurement results confirm model-based analysis. Measurement based analysis is mainly done among two or more devices which have same physical parameters and dimensions except the investigated parameter. Comparisons were made among the devices, which were processed in the same batch in order to avoid process uncertainty.

5.2.1 SiN undoped cap

Epitaxial layer structures of the compared wafers (GAB 01-01 and GAB 01-02) are given in table-5.2. These wafers are compared to investigate the effect of an undoped cap layer.

TABLE 5.2

EPITAXY STRUCTURE OF WAFTERS WITH AND WITHOUT SiN CAP

Physical Parameters		GAB01-01	GAB01-02
Cap*	**SiN**	**NONE**	**~3**
Spacer**	$Al_xGa_{1-x}N$	18	18
bulk	AlN	~0.5	~0.5
bulk	GaN	2210	2240
buffer	AlN	~ 30	~ 30

All thickness given in nm.

**SiN Cap is undoped , **x (Al content)=26 %*

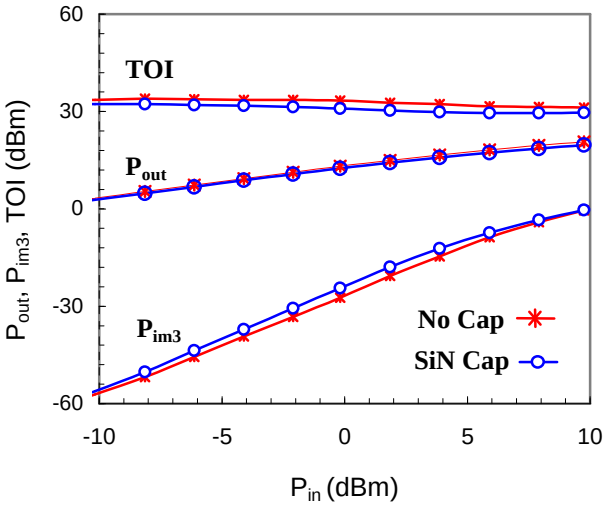


Figure 5.7 Linearity comparison of two devices with and without SiN cap layer: Measured P_{out} , TOI and IM3 vs. input power for the two epitaxial structures according to table 5.2.

In fig. 5.7, the measured data are shown. It can be noticed that the devices having undoped SiN layer have slightly lower performance in power and linearity. On the other hand, it also does not degrade device linearity drastically.

5.2.2 GaN cap doped with silicon (*Si*)

In the second step, unlike SiN undoped cap, the effect of doped GaN cap is investigated. The GaN cap layer protects the AlGaN barrier layer from oxidation. The GaN cap can be doped or undoped. FBH adopts n-doped GaN cap due to its proven performance in literature. This is a 5 nm n-doped GaN layer at the top of the AlGaN barrier layer. Introducing this layer over AlGaN/GaN, a virtual gate formation can be prevented. Fujitsu Lab in Japan has demonstrated 174 W @ 2 GHz high efficiency HEMT using this technique to reduce the current collapse [16]. The n-doped cap layer flattens the valence band and reduces the conduction band edge as shown in fig. 5.8. This reduces current collapse by fading the electric field between gate and drain region.

We have compared the wafers GMX04-02 and GMX04-04. The epitaxial data are given in table-5.3. A doped GaN cap is implemented in wafer GMX04-04 where GMX04-02 is processed without GaN cap.

Measurement results on two types of devices shows that the GaN cap indeed improves the linearity. However, further investigations show that the improvement of linearity may not be linked to the current collapse issue. This is further discussed in section 6.2.

TABLE 5.3

EPITAXY STRUCTURE OF WAFTERS WITH AND WITHOUT GAN CAP

Physical Parameters		GMX04-02	GMX04-04
Cap*	**GaN**	**NONE**	**~5**
Spacer**	$Al_xGa_{1-x}N$	18	18
bulk	AlN	~0.7	~0.7
bulk	GaN	2270	2400
buffer	AlN	~ 50	~ 50

** All thickness given in nm.*

***GaN Cap is doped with Si (n/p = ~7E18 cm^{-3}) , **x (Al content)=25 %*

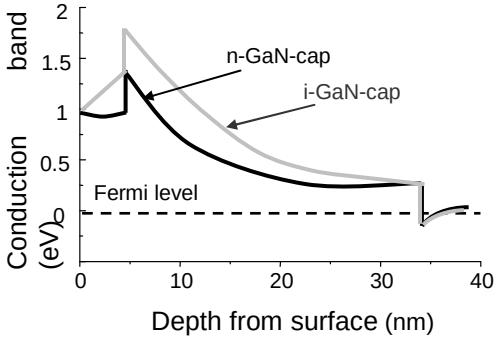


Figure 5.8 Band diagram comparison for doped and udoped GaN cap.

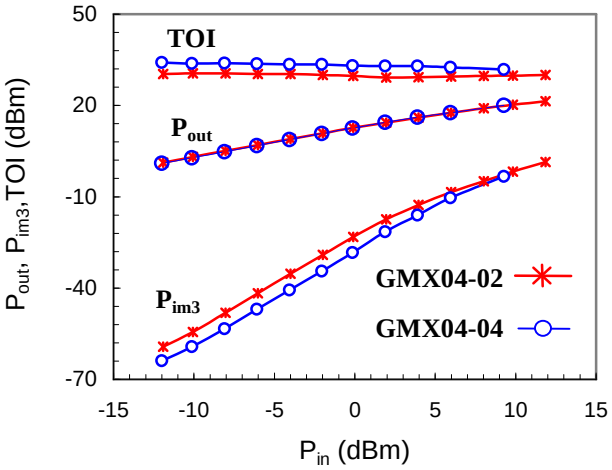


Figure 5.9 Two tone measurement of devices with and without GaN cap: P_{out}, TOI and IM3 vs. input power for the two epitaxial structures according to table 5.3.

5.2.3 AlGaN barrier height

AlGaN barrier height plays an important role in the linearity of GaN HEMT. This subject is discussed more in detail in 6.2 as it is directly related to improvement of device linearity.

5.2.4 T-gate and embedded gate

Implementing embedded gate technology is an effective way to solve the problem of current collapse. Embedded gate coming over the nitride layer acts as a field plate, which helps in reducing the current collapse. PECVD SiN_x was used due to the ease of SiN_x etching process.

TABLE 5.4

EPITAXY STRUCTURE OF WAFTERS WITH DIFFERENT GATE TYPES

Physical Parameters		GBT02-07	GBT02-08
Gate type	-	**Embedded Gate**	**T-Gate**
Cap*	GaN	~5	~5
Spacer**	$Al_xGa_{1-x}N$	25	25
bulk	AlN	~0.5	~0.5
bulk	GaN	2240	2240
buffer	AlN	~ 30	~ 30

All thickness given in nm.

**GaN Cap is doped with Si (n/p = ~7E18 cm^{-3}) , **x (Al content)=26 %*

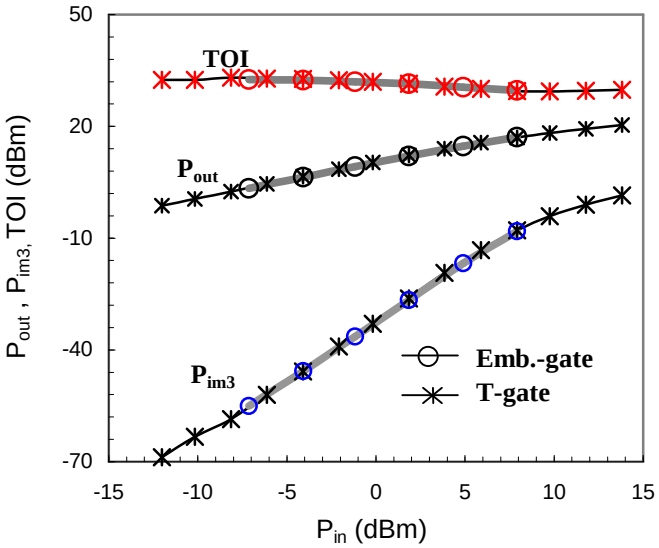


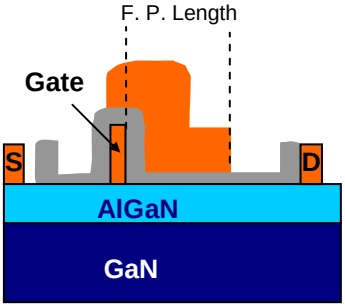
Figure 5.10 Linearity comparison of devices which T-gate and Embedded gate: P_{out}, TOI and P_{im3} vs. input power for the two epitaxial structures according table 5.4.

On the other hand, for T-gate technology, no dry etching is required and therefore problems with damage from impinging ions are avoided. Damage can introduce deep traps that lower performance in RF-operation. In the table 5.4, epitaxy data of two processed wafers (GBT02-07 and GBT02-08) are given which are identical as the wafers were processed in the same batch. The difference between them is the gate structure, the devices of the wafer GBT02-07 have embedded gate technology and the devices on GBT02-08 have T-Gate structure. Fig. 5.10 presents measured linearity characteristics. The clear outcome is that, in terms of power and linearity, virtually there is no difference.

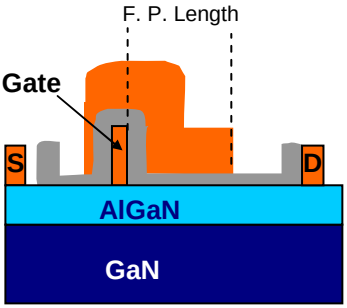
5.2.5 Field plate variation

A field plate changes the distribution of electric field near the edge of the gate electrode on the drain side thus can reduce its peak value, which helps in increasing the breakdown voltage. Three different types (type-I, type-II and type-III) of field plate structures with different lengths illustrated in fig. 5.11 were implemented. The field plate metal is evaporated as a second gate on top of the SiN_x passivation layer.

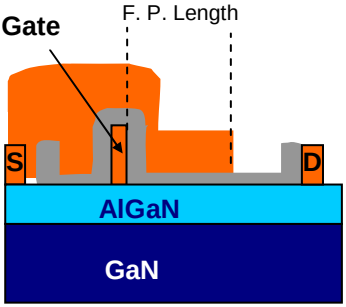
Type-I is a gate-overlapped field plate structure. The field plate extends only on the drain side and connected to the gate through the common path of the gate feeder and pads in the extrinsic device region. The field plate according to type-II also covers the gate-source region, but only partly while the type-III structure does it fully and is connected to the source. In all three cases, the field plate length parameter is defined as the length between the drain-side edge of the gate to the drain-side end of the field plate. HEMT structures with and without these three types of field plates fabricated on the same wafer were compared.



Type-I
Field-plate connected to gate



Type-II
Field-plate covering gate



Type-III
Field-plate connected to source

Figure 5.11 Different types of field plate realized and investigated.

In fig. 5.12, average TOI at a moderate input power (P_{in}=5 dBm) are plotted. The abscissa corresponds to the field-plate types. Data point is an average of measured TOI of the device with field-plate lengths 0.0 µm, 0.5 µm, 1 µm and 1.5 µm of each type and the vertical bar around the data point represents the deviation of measurement data. The deviation is below 0.5 dB which suggests the types and lengths of field-plates investigated, do not influence the linearity of the device significantly. It is worthwhile to mention here that the field-plates also changes input and output capacitances C_{gs} and C_{ds} accordingly.

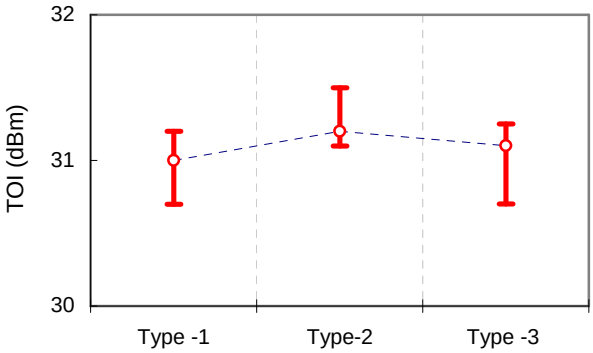


Figure 5.12 Measured TOI at 5 dBm input power for the devices with different field plate lengths of each types. Data point is an average of 20 measurements (5 devices of each length) and the error bar shows the maximum and minimum value.

5.2.6 Drain-source capacitance (C_{ds}) variation

Nonlinear drain source capacitance is often suspected as a source of device nonlinearity. However, the sensitivity analysis given in the previous section did not show any significant influence on linearity for a realistic variation of C_{ds}. Due to the fact that other types of devices

in literature exhibit this effect, we have checked this issue for our devices experimentally. A series of devices with different drain source distance L_{ds} was fabricated. This is the simplest way of varying drain source capacitance, as the area is directly proportional to the capacitance.

It is shown in fig. 5.13 that these devices tagged as A2, A3, A5, A6, A8 and A10 who have the L_{ds}=2, 3, 5, 6, 8 and 10 µm respectively, have virtually no difference in terms of output power and linearity. This supports the result of the model analysis that the variation of C_{ds} in a realistic (realizable by available technology) do not have any significant effect on linearity for class-AB operation.

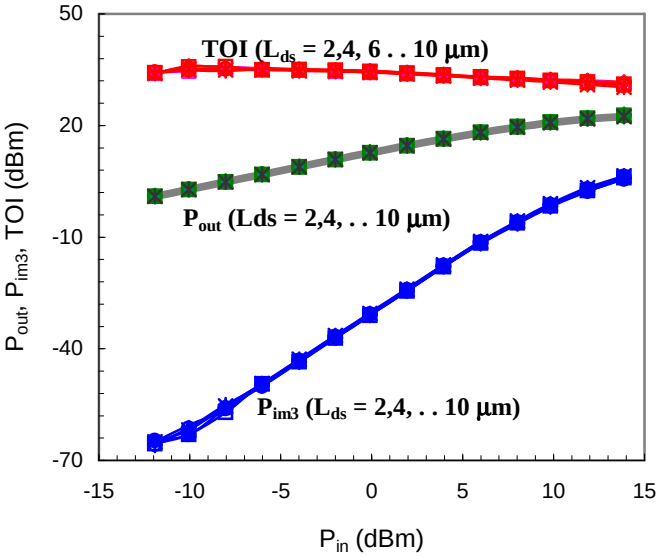


Figure 5.13 Linearity comparison of devices with different drain source distance and therefore different C_{ds}.

5.3 Access resistance related nonlinearity in high power devices

Bias dependent access resistances, has been claimed as the main source of device nonlinearity of AlGaN/GaN HEMTs in some recent publications [17][19][20]. Accordingly, in [17][20], device architectures were suggested to improve the access resistance dependent linearity.

In order to clarify this effect, we have investigated the bias dependence of R_d and R_s parameters in order to approximate their effect on linearity. It is worthwhile to mention that these devices are passivated, as the access resistance dependency on bias is crucial for non passivated AlGaN/GaN HEMTs due to current collapse [19]. On the other hand, DC modulation of access resistances of passivated devices are also considered to be significant in [17][20].

The investigated power transistor consists of five sub-cells, each with 8 gate fingers of 250 µm gate width. These are connected in parallel and bonded into an industry-standard ceramic package. Fig. 5.14 shows a close-up of a typical HEMT power-bar inside the package. The packaged devices were measured in a well-defined test fixture (*Robotron* fixture, see fig. 4.3(a)). Measured s-parameter data was then deembeded to extract the s-parameter at the device reference level. The source is connected through vias on the chip and backside metallization. The GaN HEMT devices were characterized at 2 GHz. Fig. 5.15 shows the small signal equivalent-circuit model of a GaN HEMT including the package. Our intention was to characterize the device with the package, therefore in the de-embedding process we only de-embed the fixture. Bias dependent parasitic resistances R_d and R_s were then directly extracted from the S-parameter measurements of this device at the package reference, which is similar to the method presented in [21].

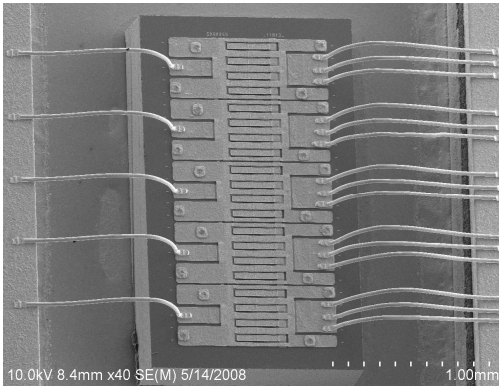


Figure 5.14 SEM picture of a GaN-HEMT power transistor bonded into a ceramic package.

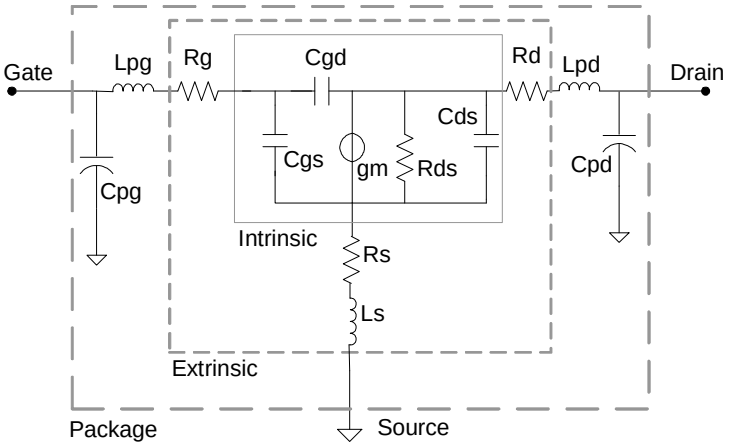


Figure 5.15 GaN HEMT small signal model, R_g , R_s, R_d are the extrinsic parasitic resistances. L_{pg} and L_{pd} are the bond wire inductance where C_{pg} and C_{pd} are the package capacitances.

After converting S to Z and Y parameters, the bias dependent parasitics are extracted from the following linear relationship:

$$\mathrm{Re}(Z_{12}) = \left\{ \frac{C_{\mathrm{gd}}}{g_{\mathrm{m0}}} X + R_{\mathrm{s}} \right\}$$

where,

$$X = \omega\left\{\cos(\omega\tau)\left[\mathrm{Im}(Z_{21}) - \mathrm{Im}(Z_{12})\right] - \sin(\omega\tau)\left[\mathrm{Re}(Z_{12}) - \mathrm{Re}(Z_{21})\right]\right\}$$

and, $g_{\mathrm{m0}} = g_{\mathrm{m}} e^{-j\omega\tau}$

R_{S} is found from the intercept of $\mathrm{Re}(Z_{12})$ versus X. Once R_{S} is subtracted from the Z-parameters, the hot value of R_{d} is determined as:

$$R_{\mathrm{d}} = \left\{ \frac{\mathrm{Im}(Z_{12})\,\mathrm{Im}(D) + \mathrm{Re}(Z_{12})\,\mathrm{Re}(D)}{\mathrm{Im}(Z_{12})\,\mathrm{Im}(Z_{21}) + \mathrm{Re}(Z_{12})\,\mathrm{Re}(Z_{21})} \right\}$$

where, $D = Z_{11}Z_{22} - Z_{21}Z_{12}$

Other equivalent circuit elements such as R_{ds}, C_{gs}, C_{gd}, C_{ds} were also physically extracted. The "HotFET" extracted values of R_{d} and R_{s} are extremely low (R_{d} = 0.5 Ω and R_{s} = 0.1 Ω) and show a constant behavior over a usable bias range. We would not refer to these numbers as accurate values as they are extremely small and at the limit of measurement and extraction sensitivity. However, what we want to stress is that these values are pretty small and have almost no bias modulation effect. Interestingly, R_{ds} of the intrinsic transistor, which is parallel to the nonlinear current source, exhibits certain nonlinearity. This is related to the non-linearity of the current source. The measured g_{m}, I_{d} and extracted R_{ds} are plotted in fig. 5.16. The measured g_{m} is very flat over common operating gate bias range. We have also extracted drain bias dependent R_{ds} and C_{gd} keeping constant gate bias (I_{d} = approximately 1 A). As it can be seen in

fig 5.17, both quantities depend on drain voltage, the influence of which is stronger than that of the gate voltage.

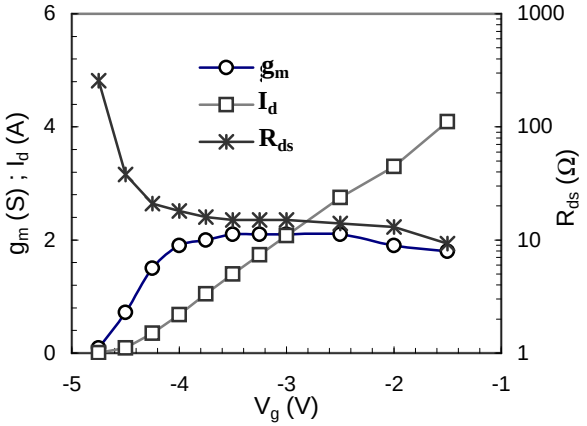


Figure 5.16 Drain current I_d, tranconductance g_m and R_{ds} at different gate bias and constant V_{ds}=10V.

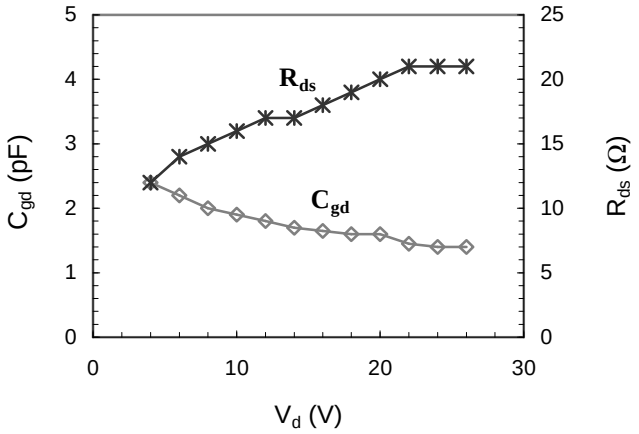


Figure 5.17 Drain Bias dependency of Cgd and R_{ds} ; I_d=1A.

Due to the fact that for some parameters we were at the limit of measurement and extraction accuracy and did not observe any bias dependency for such large device, we wanted to verify our extraction procedure. Hence, we decided to bond only a single cell in the same package (i.e, forming a 1x8x250 μm device instead of a 5x8x250 μm one) and extracted R_d. Fig. 5.18 presents the results. This shows a very slight but not pronounced variation in common bias range. The "Hot FET" R_d is about 2 Ω for a single cell which reasonably fits to the previous result for the large transistor.

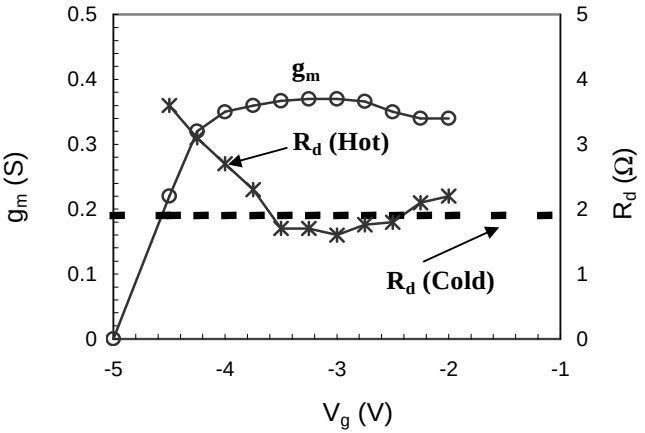


Figure 5.18 Transconductance g_m and access resistance R_d of a single cell bonded in a package. V_d=25V , I_d=1A.

To double-check the extraction procedure we applied an alternative method to verify the accuracy of extracted R_d and R_s. If the transistor chip is bonded in a package, the measured S-parameters exhibit a resonance around 6 GHz (for this particular package). The resonance frequency depends on the value of L_{pg} and C_{pg} of the package. The width of this resonance curve is very sensitive to R_d and

R_s that allows to check the accuracy of these parameters. We have simulated the small signal equivalent circuit with a set of R_d and R_s values. Simulated resonance curve does not fit well with the measured curve for any other value of R_d and R_s instead of the extracted ones.

5.3.1 Influence of gate-source spacing L_{gs}

In [20], reduced gate-source distance L_{gs} was proposed in order to improve the linearity by reducing access resistance R_s based on the results published in [17][19]. However, no practical results were presented. We have verified this topology for our devices. Our standard power devices have a source gate distance L_{gs} of 1 µm. To study the effect of L_{gs} we have fabricated and studied linearity performance for transistors with different extreme gate-source spacing (L_{gs}), 0.5 µm and 2.0 µm, with constant gate-drain distance of 2.3 µm. The transfer characteristics were measured at a drain bias V_d = 15 V and in the range from below pinch-off to +3 V of gate bias. The g_m profile was obtained from transfer characteristics and compared for two types of transistors as shown in fig. 5.19.

Two-tone measurements were performed similar to the condition of previous measurements i.e., at 2 GHz with a tone spacing of 10 MHz. Drain voltage was kept +15 V with quiescent current of approximately 80 mA. The measurement result is shown in fig. 5.20. It clearly shows that the device with smaller gate-source spacing reveals no improvement in linearity rather, surprisingly the linearity performance deteriorates. As can be seen that the shorter L_{gs} reveals higher current and gain, a further study to find the optimum L_{gs} is necessary. On the other hand, devices with shorter L_{gs} is difficult to fabricate in terms of technology and therefore have lower yield. However, it at least shows that the R_s optimization to enhance linearity is not effective for this devices.

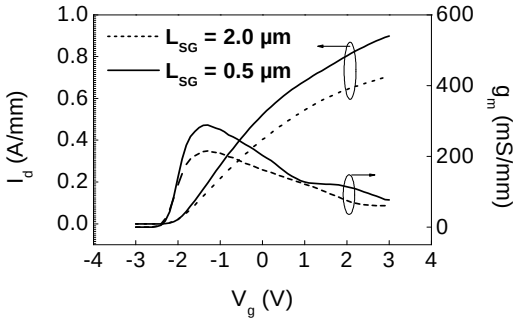


Figure 5.19 Comparison of transfer characteristics and transconductance profiles measured for transistors with L_{gs} 2.0 µm and 0.5 µm, gate length 0.3 µm and gate width 125 µm. Drain bias is 15 V.

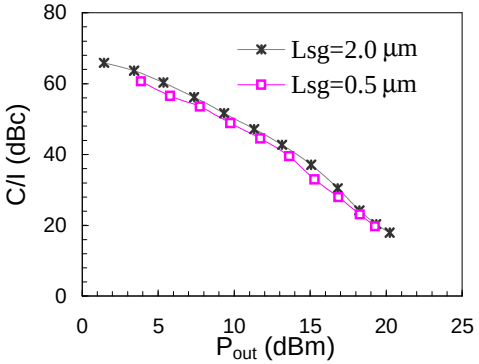


Figure 5.20 Carrier to intermodulation ratio (C/I) of transistors with L_{gs} 2.0 µm and 0.5 µm. V_d= 15 V and I_g =80 mA. Two-tone measurements are done in 50 Ω environment with tone spacing of 10 MHz where the first tone was fixed at 2 GHz.

Summarizing, we can state that both R_s and R_d were found to be very small with a negligible bias dependence. Hence their influence on nonlinearity is not significant for state-of-the-art GaN HEMT device.

6 Device level linearity of GaN HEMT

In recent years, regarding linearity of RF devices and amplifiers, research has been mainly focused on characterizing the devices in terms of linearity and external linearization of power amplifiers (PAs). However, only very few initiatives have been taken so far to analyze or to improve the linearity at the device level [22][23].

According to the previous findings it is clear that the second order transconductance (or, in other words, the inflection of g_{m}) should be as small as possible to achieve best IM3 performance. In this chapter, methods of improving GaN HEMT linearity are presented based on the aforementioned findings.

We have shown that certain physical parameters have significant influence on device linearity, which can be optimized in order to improve device level linearity. A novel idea to make an ultra-linear device by super-positioning the characteristics of multiple devices is also presented.

6.1 Linking systematic and sensitivity analyses to physical device simulation

It was concluded from the analyses of chapter-5, that one should have a flat transconductance profile in order to minimize the third-order distortion components. Physical device simulators usually calculate only DC characteristics. Therefore, to optimize devices by physical device simulator needs special treatment (i.e., fitting of the DC curves and extracting higher order transconductances) which is briefly explained in the following.

The physical device simulation used is *Silvaco Atlas-Blaze,* with self-heating effects enabled, and a thermal resistance, which was calculated using a separate 3D thermal simulation of the device [24]. Self-heating is required to give good agreement between model and experiment over the full IV plane, including the knee region. A key issue in gaining good agreement between the DC current and voltage characteristics, especially in forward bias, is the choice of the surface state energy level, which pins the Fermi-level in the ungated access regions. Good agreement was only found by pinning the Fermi-level at 0.5 eV below the AlGaN conduction band edge.

The electron transport is modelled using a constant mobility and velocity saturation using a Caughey-Thomas function with a saturated velocity of 1.9×10^7cm/s. As this physical device simulator does not support harmonic balance or time domain simulation. Therefore, an alternative method was used to calculate TOI from the simulated transconductance profile. Intermodulation distortion was evaluated by using a Volterra-series approach [26].

The gate transfer curve was fitted locally using a polynomial expansion:

$$V_D(V_G) = k_0 + k_1 V_G + k_2 V_G^2 + k_3 V_G^3 + ... \quad (6.1)$$

The third-order intercept was then extracted using:

$$P_{TOI} = 10\log\left[4\frac{Y_{21}^{\ 3}}{Y_{21}^{''}} R_L .10^3 \right] = 10\log\left[\frac{2k_1^{\ 3}}{3k_3} \times \frac{10^3}{R_L} \right] \quad (6.2)$$

where, Y'' is the second derivative of Y matrix with respect to V_G

Using Atlas to calculate a gate transfer characteristic allows us to calculate P_{TOI} over a range of gate bias. This was done using a MATLAB script, which fits a third and first order polynomial to a $\pm$ 0.7 V range of gate bias, extracts the values of k_1 and k_3 and calculates P_{TOI}. According to our findings in Chapter 5, we have to look for a device architecture that has the largest k_1 and lowest k_3, which can be done by a computer optimization algorithm.

In fig. 6.1, the base device structure with the investigated dimensions is shown. In addition to these dimensions, varying Aluminum concentration was also studied. After a strenuous computer calculation by sweeping all these parameters, some parameters have been found to have a particular influence. A detailed discussion on the physical simulation results is out of the scope of this thesis. However, the following observations are of special importance:

- Buffer doping has insignificant effect on linearity.
- Field-plates at drain side have no major effect on TOI but do result in a significant reduction in electric fields.
- Changes to the epitaxial layer structure that reduce carrier concentration, will increase operating voltage but degrade linearity. (i.e, lower *Al* concentration results in lower linearity).

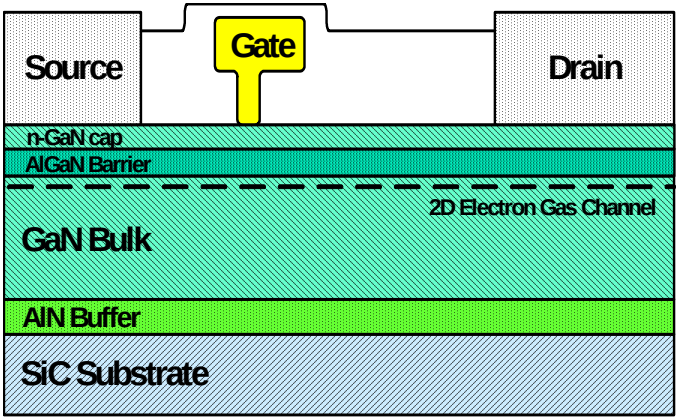


Figure 6.1(a) GaN HEMT epitaxial structure.

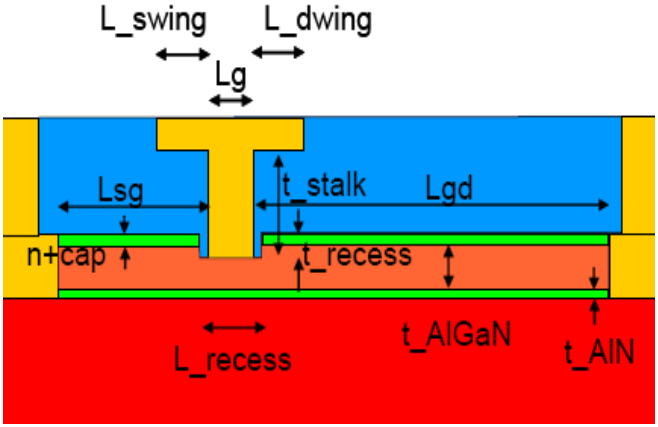


Figure 6.1(b) Investigated physical dimensions of a GaN HEMT using the physical device simulator.

To verify the method, simulated results are compared with measurements. We have selected the case of devices with different barrier thickness where we observed a clear effect on linearity of the device. In fig. 6.2, the normalized measured ACPR is plotted in comparison to simulated normalized integrated third order intercept point in the range of a operating gate voltage which is denoted as (IPTOI).

The integrated quantity IPTOI is calculated to get a reliable figure of merit due to the fact that the physical simulator returns a noisy TOI over the V_g of class-A bias range. TOI is noisy because it is calculated at every discrete gate voltage. The comparison shows a good agreement between simulation and measured linearity figures of merit.

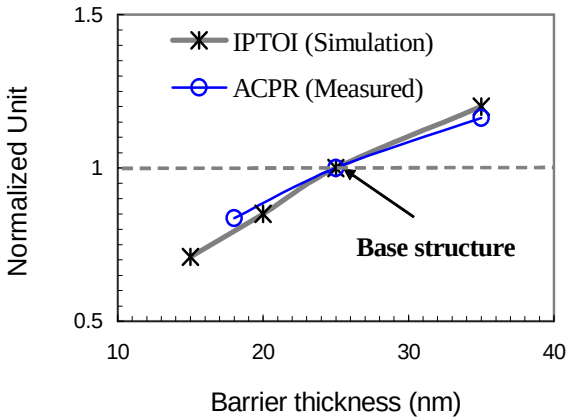


Figure 6.2 Normalized IPTOI (simulation) and measured ACPR (normalized) against different AlGaN barrier thickness. (Linearity of base structure with 25 nm barrier thickness [=t_AlGaN in fig 6.1(b)] corresponds to unity at ordinate for both the cases).

6.2 Influence of barrier thickness

Experimental data analysis on devices with different barrier thickness and doped cap showed a significant influence on transconductance and linearity. Therefore, it is clear that this physical parameter should be considered when optimizing device linearity. Accordingly, HEMT devices with different epitaxial structures were simulated, fabricated, and measured. Third-order intermodulation distortion IMD3 and ACPR measurements were performed in order to compare linearity experimentally. A significant linearity improvement is observed for an optimized architecture.

6.2.1 Theory and simulation

As mentioned earlier, the first-order parameters determining nonlinearity of III-V HEMTs are the higher-order transconductances (derivatives of the transfer characteristics). We use a physical device simulator as mentioned in section 6.1, to analyze the IV characteristics of our GaN HEMT structures with different barrier thickness. The third derivative of the transfer characteristic g_{m3} (that means the second derivative of the transconductance) for devices with different barrier thickness with/without doped cap was calculated, in order to compare the third order distortion components quantity. A lower absolute g_{m3} means a lower third order intermodulation distortion.

The simulated and manufactured structure of the AlGaN/GaN HEMT is shown in fig. 6.1 The AlGaN layer forms the barrier for electron transport. Its thickness with/without the doped cap layer, which is equivalent to the total distance between the gate and the two-dimensional electron gas (2DEG), turns out to be a key parameter for linearity. In fig. 6.3 (a) and (b), simulated transconductance g_m

and third order transconductance g_{m3} are plotted, respectively, for HEMT devices with 250 µm total gate width and the epitaxial profile as listed in table-1. It can be seen that the device with higher barrier thickness has a flatter gm curve, which leads to a small absolute g_{m3} over a wide range of gate voltage and, therefore, lower third-order distortion components.

It should be outlined that the g_{m3} for the device with 35 nm thickness has an overall lower magnitude $|g_{m3}|$, and not just a single zero crossing point. Such a single zero crossing point is often called a sweet spot in literature. A sweet spot is a particular bias point where g_{m3} crosses the zero line and the device shows a linearity peak (theoretically infinite). Unfortunately, these points are not easy to reproduce in reality, as the bias point shifts continuously under real world operating conditions. On the other hand, with increasing AlGaN layer thickness, the device losses on the absolute value of g_m due to reduced driving capability of the gate. This may affect microwave gain. Therefore, one must be careful to select the optimum thickness to obtain the best possible tradeoff between gain and linearity.

We studied an alternative solution for increasing the effective barrier height, by introducing a thin doped cap layer. This also shows a significant improvement in terms of linearity compared to the conventional thin barrier layer design. The additional doped cap layer increases the distance between the 2 DEG and the Schottky metal, which results in a flatter g_m profile, being similar to a device with thicker AlGaN layer. Due to the fact that both types of devices (thin AlGaN barrier with doped cap layer and thick AlGaN layer of total similar thickness) show similar linearity behavior, it seems that only the absolute distance between 2DEG and Schottky gate is decisive with respect to linearity.

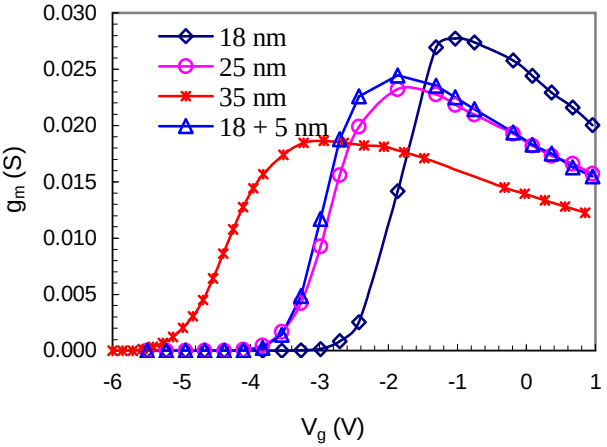


Figure 6.3 (a) Simulated g_m of GaN HEMT cells with different barrier thickness and with/without cap as a function of gate source voltage.

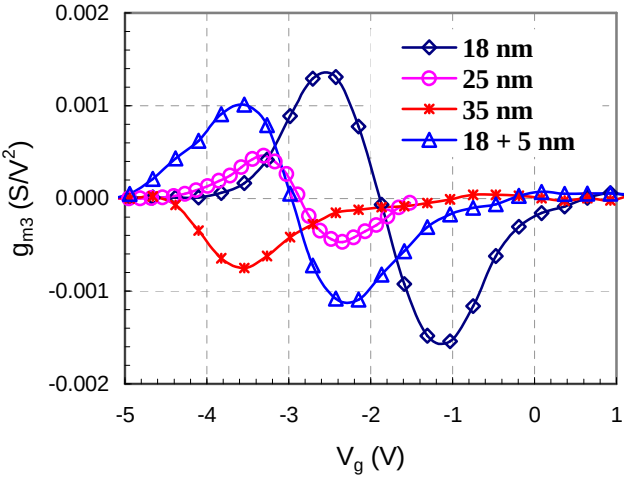


Figure 6.3 (b) Simulated g_{m3} of GaN HEMT cells with different barrier thickness and with/without cap as a function of gate source voltage.

6.2.2 Fabrication, measurements and discussion

In order to verify the effect of barrier thickness and doped GaN cap, we fabricated devices on two pairs of wafers as listed in table-1. The *Al*-concentration in the AlGaN barrier has been kept constant at 23% in all the cases. In the first pair, the thickness of the AlGaN layer was 25 nm and 35 nm, respectively, with none of them having a GaN cap. The second pair had a different epitaxial structure using a thinner AlGaN layer of 18 nm thickness and, for one of the wafers, an additional 5 nm GaN doped cap layer. The AlGaN thickness was precisely controlled during the epitaxial growth and measured afterwards using high-resolution x-ray diffraction (HRXRD). Table-1 shows the epi-structures of the four wafers that were compared. All other dimensions except the distance between gate Schottky metal and the 2DEG were kept the same. Fabricated and measured devices are GaN HEMTs with a total gate width of 250 μm (2x125 μm device geometry). The linearity measurements of these transistors are presented in the following [27].

A. Two-tone measurements

The third-order distortion components (IM3) were characterized by two-tone measurements (for measurement set-up see 4.1). The DC drain source voltage V_d and drain source current I_d were kept constant for all devices in order to allow a reasonable comparison. V_d was set to 20 V and gate-source voltage V_g was selected carefully to have an I_d of approximately 80 mA in all cases. Output power was swept in order to obtain a complete picture and to avoid any sweet point phenomenon. (Note that absolute output power is relative low because of the mismatch between Γ_{opt} and 50 Ω.) The first tone was kept at 2 GHz and the tone spacing was 10 MHz.

TABLE 6.1
EPITAXY STRUCTURE OF COMPARED WAFERS WITH DIFFERENT BARRIER THICKNESS

Layer	Wafer "A"		Wafer "B"	
	x	d (nm)	x	d (nm)
$Al_xG_{1-x}N$	0.23	18	0.23	25
Buffer GaN	-	~2330	-	~2330
AlN	-	~40	-	~40

Layer	Wafer "C"		Wafer "D"	
	x	d (nm)	x	d (nm)
GaN Cap		0		5
$Al_xG_{1-x}N$	0.23	35	0.23	18
Buffer GaN	-	~2310	-	~2310
AlN	-	~40	-	~40

**The thickness of AlGaN layer was measured by HRXRD measurement*

Since g_m drops for a thicker barrier, the gain will be different for different epitaxial structures. Hence, one must compare the measurement data for the same output power and not at the same input level. Only if one device has less IM3 at a given output power it can be concluded that it is inherently more linear than another device. Fig. 6.4 presents the measured data on carrier-to-intermodulation ratio C/I at different output powers. It can be seen that the device with 35 nm barrier thickness shows a C/I ratio almost 4 dB better than

that of the device with 18 nm thickness over a broad range of output powers. The device with 25 nm AlGaN thickness without cap and the device with 18 nm AlGaN plus 5 nm cap performs almost equal which is slightly worse than the 35 nm design and better than the 18 nm (without cap) design.

B. ACPR measurements

For wireless communication applications, adjacent channel power ratio (ACPR) provides a linearity figure of merit, which is more realistic than third order intercept point (TOI) or IP3. Measurements were performed using an arbitrary WCDMA standard downlink signal with test-model-1 (64 DPCH). In fig 6.5, the output spectrums of all 4 device types are compared at the same output power. The device with

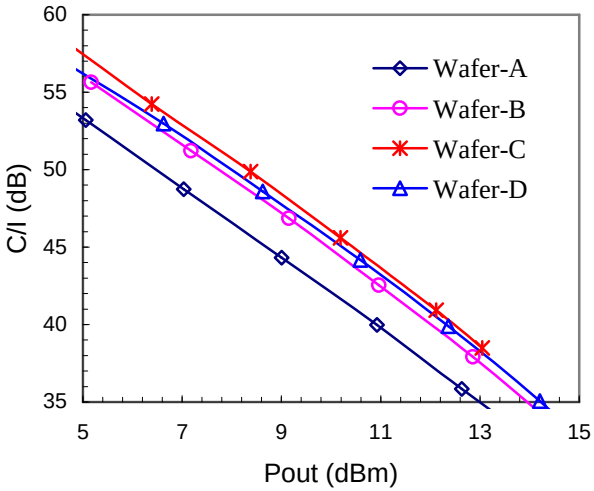


Figure 6.4 Comparison of C/I ratio of 2x125 GaN HEMTs with different AlGaN thickness (see table 6.1) at $V_d = 20$ V and $I_d = 80$ mA.

35 nm barrier thickness shows an ACPR performance at least 7 dB better than that of the transistor with 18 nm barrier thickness (without cap), which is in line with the IM3 data. In fig. 6.6, ACPR is plotted as a function of I_d. Drain voltage V_d was kept constant at 20 V and the gate voltage V_g was adjusted accordingly. It can be seen that the device with 35 nm barrier thickness maintains its superiority with regard to linearity also when varying the drain current. As for the data in figs. 6.4 and 6.5, the device with 18 nm AlGaN thickness combined with a 5 nm cap layer performs almost similar to the device with 25 nm AlGaN thickness.

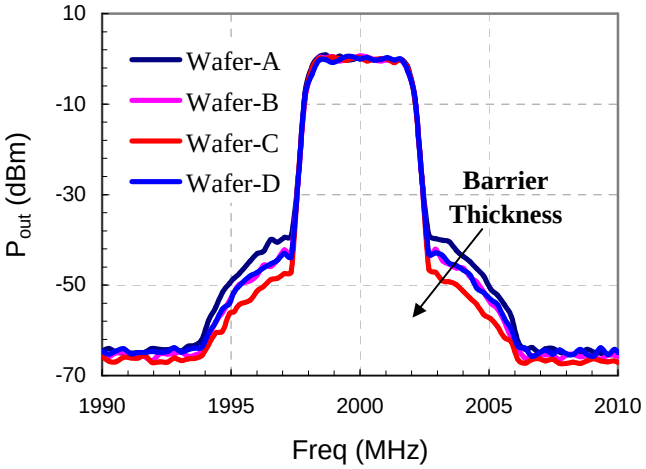


Figure 6.5: ACPR measured under standard WCDMA signal (Test-model-1, 64 DPCH) for different devices with different epitaxy (see fig. 4 and table-1) at a bias point V_d=20V and I_d=96 mA at equal output band power 15 dBm (other data as in fig. 6.4).

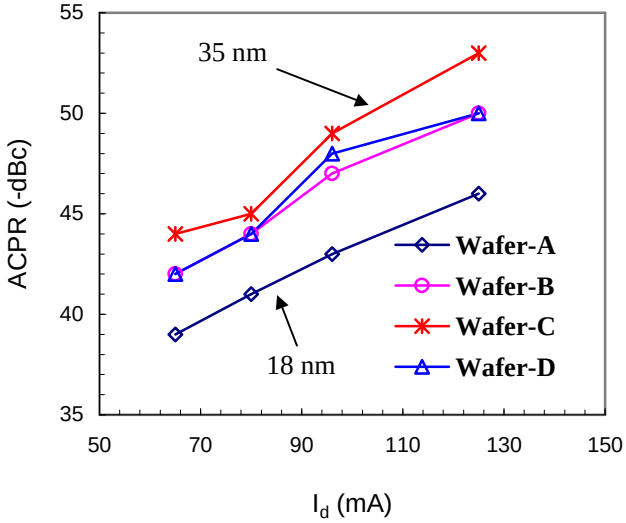


Figure 6.6 ACPR measured at different drain currents (V_d=20V and V_g set according to the drain current), other data as in fig. 6.4.

6.3 Enhancing linearity of a large device by optimizing individual device units

In this section we are presenting a novel technique for the improvement of overall device linearity. The basic idea is to parallel HEMT cells having slightly different transfer characteristics in order to equalize overall g_m curve. This can be realized within a single device or at a power bar level. In case of a single device this method is applicable only if the device contains several fingers or consists of more than one unit. In the case of power bars, each unit cell may have variation in transconductance characteristic. Controlling this variation precisely, it is possible to tailor the overall transconductance in a way such that the intermodulation distortion due to higher order transconductance is minimized. The idea comes from the fact that the

main source of nonlinearity in a typical transistor at weakly linear operating condition is the nonlinearity of transconductance. In a multi-unit transistor or power bar when bonding them in parallel, usually all the units are identical and therefore the shape of the transconductance curve does not change. If every unit is designed a bit different to have more linear overall transconductance shape then the overall linearity performance will improve. Fig. 6.7 shows the mechanism graphically. This can be realized in different ways. For example:

- Recess Technology: By recessing the gate of a HEMT, the transconductance can be precisely controlled. Controlling the recess depth, the pinch-off voltage can be shifted and the shape of the transconductance curve can be optimized. Shifting the pinch off voltage, optimizing the shape and scaling the gate width, it is possible to achieve a great flexibility to engineer the transconductance curve.
- Gate position: By changing the gate lengths and gate position it is also possible to change the shape of the transconductance curve.

As an example we present here simulation results of a multi-cell HEMT Powerbar optimized for high linearity. To vary the transconductance shape of each individual cell, recess technology is used. If the gate is recessed with different depths, the transfer characteristic changes. In case of recessing, the depth of “t_recess” in fig. 6.1(b) will be varied. In fig. 6.8, simulated transconductance g_m is shown at different recess depths. It can be seen that there is a shift in pinch off voltage and a change in slope at each cell.

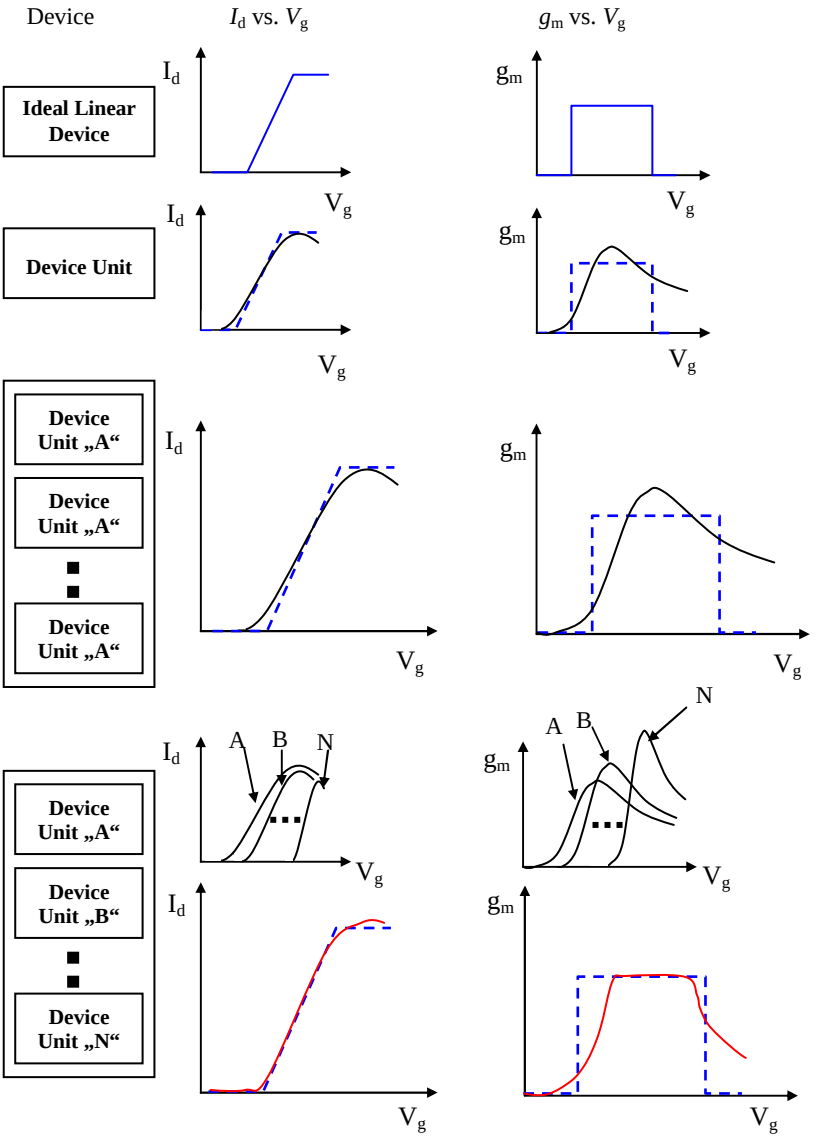


Figure 6.7 Graphical representation of the linearity enhancement by optimizing each individual units of a multi-unit device [28].

To enhance the overall linearity of the device, higher order g_m have to be minimized and therefore the resulting g_m curve has to be flat. We took a few numbers of recessed cells with different recess depths (labeled in fig. 6.8 as R_{xx}; here "xx" is the recess depth) and thus varying transconductance characteristics and combined them. The recess depth and the gate area of the individual cells were precisely optimized such a way so that the resulting transconductance curve lead to a flat form hence resulting in a minimum nonlinearity[1]. The gate length of the particular recessed cell is normalized and represented as scaling factor.

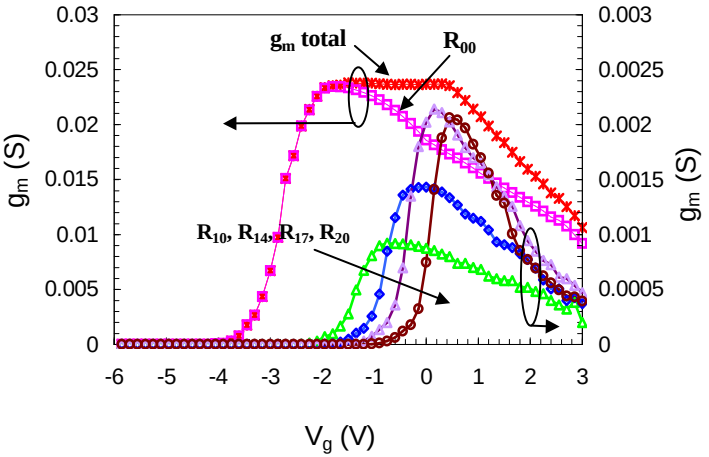


Figure 6.8 Simulated transconductance vs. V_g of six individual device units and of the complete device. R_{00}, R_{10}, R_{14}, R_{17}, R_{20} are the unit devices having scaling factor n = 1, 0.03, 0.04, 0.05, 0.04 accordingly (Scaling factor is normalized gate length).

[1] Patent pending Patent Nr. 071106253.1-2203

6.4 Enhancing linearity at low back-off regime

Wideband digital modulated signals usually have very high peak to average ratio. Therefore, amplifiers are operated at high back-off to meet the linearity specification at peak power. Therefore linearity near saturation is a very important issue to operate PA efficient. On the other hand, astonishingly, modern mobile phone base stations have an overall efficiency of 5-10% that is very bad in terms of energy cost and environment. Unfortunately, linearity and efficiency are contradictory parameters for a RF circuit designer.

Class-A amplifiers are known to be very linear but inefficient as the amplifier is always on and consumes DC power even when there is no RF signal at the input. Higher efficiency classes usually bias the device near or below pinch-off so that no DC power is consumed during idle time. Linearity of these classes is usually bad due to clipping effect. It has been shown that, class-B can be linear if the gate closes sharply during pinch-off and the device can be precisely biased [29]. In this section we have analyzed this fact at the device level with a physical simulator and improved the gate-closing profile for high-efficiency linear operation. Physical level simulation shows that the reason for the "dogleg" like I_d vs. V_g profile occurs due to gate punch-through during pinching off. An easy solution to stop or decrease this punch-through current is to use a longer gate. However, longer gate will decrease gain and hence f_T which is not desirable for high-frequency operation. Therefore, a design compromise must be made according to application. There can be many other effective solutions (e.g., back-barrier) to stop punch-through current keeping the gate reasonably shorter. Our intension is to show that the linearity enhancement for higher efficiency classes (i.e., class-AB, class-B etc.) operation needs considering punch-through current.

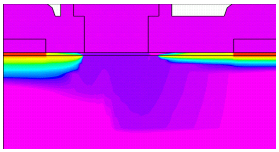
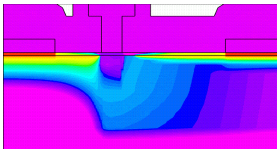
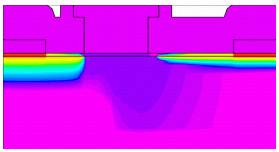
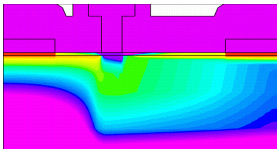
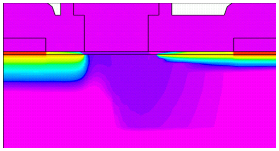
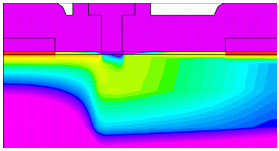
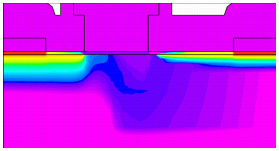
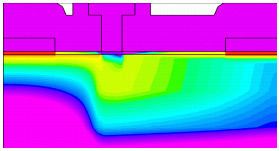
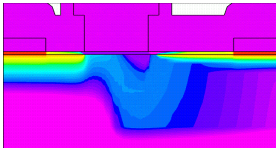
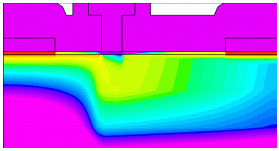
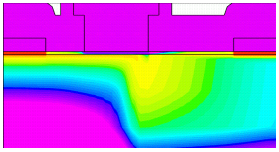
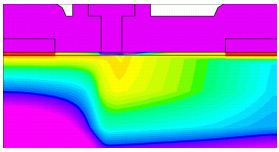
6.4.1 Simulation and analysis:

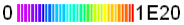
A longer gate shows a very good on-off characteristic, which is appropriate for higher efficiency class operation. In Table 6.1, simulated electron concentration in GaN HEMT with different gate length, at different gate bias are shown. It is noticeable that even with very high negative bias there is a small current flowing in the channel of the short gate device, which is called punch through current. The current slowly increase till the channel is totally open. On the contrary, for the device with the longer gate, there is almost no current above a certain negative gate bias, which is reasonable. It should be noticed that the turn-on gate voltage is quite sharp as compared to the shorter gate device.

In fig 6.9 (a), simulated and measured drain current is plotted as a function of gate voltage for the devices with different gate lengths. This picture clearly shows the "dogleg" profile of the I_{d} vs. V_{g} curve. The device with the longer gate having a narrow turn-on region, that suggests a very fast closing and opening of the gate. This improves the linearity at saturation region. This is simply because of clean clipping effect when bias near or below pinch-off and at higher drive of class-AB. After the fabrication of the devices, they were measured. Fig. 6.9 (b) shows the DC measurements. The plotted data is an average of 45 device measurements. The simulation captures the bending intensity of the "dogleg" shape. The long gate devices have a sharper turn-on region.

C/I ratio of the devices with gate lengths of 0.25 μm and 1 μm was measured. The devices with longer gate showed higher C/I ratio at high drive. If biased near pinch off, the devices with the longer gate ensures high linearity at peak power, which is very interesting.

TABLE 6.1
ELECTRON CONCETRATION IN THE CHANNEL

V_g	Long Gate (Device-A)	Short Gate (Device-B)
-6 V		
-4.5V		
-3.6 V		
-3.4 V		
-3.3 V		
-1.9 V		



Color intensity corresponds to the electron concentration /cm^3

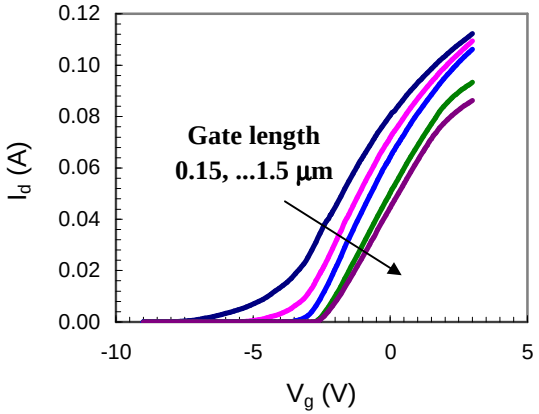


Figure 6.9 (a) Simulated drain current I_d as a function of gate voltage V_g of the devices with gate length of 0.15 µm, 0.25 µm, 0.40 µm, 1.0 µm and 1.5 µm accordingly.

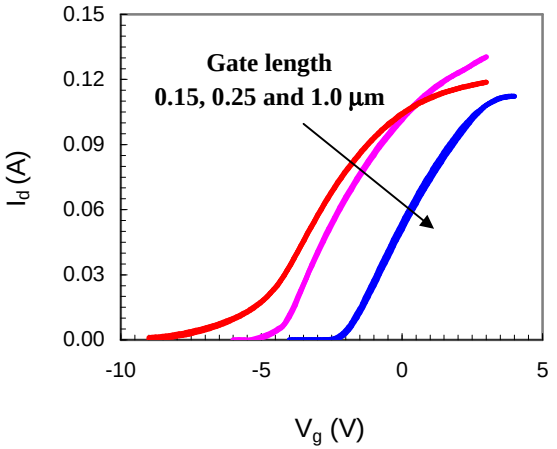


Figure 6.9 (b) Measured drain current I_d as a function of gate voltage V_g for devices with different gate length.

In fig. 6.10, the C/I measurements of two devices are compared. The C/I ratio plotted for the device with short gate is its best performance near class-A bias where the device with the long gate is biased near pinch-off. We have also measured devices of the same type at different positions on the wafer which shows an excellent reproducibility at the same bias voltages. It is to be mentioned that the devices with the narrow gate do not show a comparable linearity peak when biased near pinch-off.

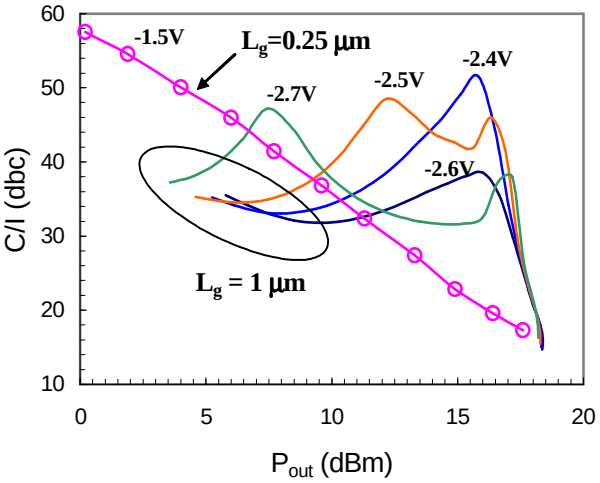


Figure 6.10 Measured C/I ratio vs. output power. Long gate-length (L_g= 1.0µm) device measured at gate voltage from –2.4 V to –2.7 V which is near pinch off and compared with the best performance of short-length gate(L_g= 0.25 µm) device biased at Class-A (Vg=-1.5V). V_d is 24 V for all measurements.

7 GaN HEMT as linear amplifier

The previous chapters focused on the linearity of GaN HEMTs. It was analyzed in detail in order to understand the mechanism of distortion product formation in these devices. Based on this analysis, methods of improvement of linearity were suggested.

In this chapter, we will present the performance of GaN HEMTs within an amplifier following the class-AB concept.

7.1 Class-A, B and AB

A detailed discussion on different amplifier classes is beyond the scope of this thesis and can be found in most of the textbooks related to RF amplifiers [29][30][31].

Class-A amplifier is the most simple linear amplifier. The bias point is kept in the center of the I-V curve and the conduction angle is 360°. The conduction angle is defined as the part of a period during which the transistor is carrying current. This means that the amplifier conducts full 360° of the input signal. This amplifier class is the most linear one unless extra linearization technique is used, but it also has the disadvantage of being the lowest efficient one. Theoretical maximum efficiency of this class is 50%.

For class-B, the bias voltage equals the pinch-off voltage, resulting in a conduction angle of half the period and a half sine wave for the output current. A perfect class-B cannot be achieved due to the limitation of amplifying devices. Class B amplifiers are usually built in

a push-pull configuration of two transistors In contrast to class A mode, the theoretical efficiency is 78.5%.

Class-AB represents a compromise between class-A and class-B. This class has a conduction angle between 50 % and 100 %. It is the mode used for most practical power amplifier implementations with high linearity requirement.

7.2 GaN HEMT based linear PA design: Concept and consideration

The basic advantage of designing PA based on GaN HEMTs is that the high output impedance level makes it easier to design the matching networks. However, due to immaturities of the technology, the accuracy of the large-signal model is not always satisfying. Therefore, the safest method to design a power amplifier is load-pull measurement based design. In fig. 7.1, the measured load-pull contour of a small GaN HEMT of 2x125 micrometer periphery is shown. The load-pull was done with a WCDMA (test-model-1, 64 DPCH) test signal tracking channel powers and tuning load impedance over the entire smith chart. WCDMA signal is a wide band modulated signal and therefore having much higher crest factor compare to that of the single tone or two-tone signal. The real value of crest factor usually varies from 4.5 dB to 11 dB depending on the number of code channels varying from 1 to 128 accordingly. Such load-pull measurement emulates realistic operating condition.

As it can be seen from the load-pull measurements there is a clear tradeoff between the optimum impedances for the best output power and lowest adjacent channel power ratio (ACPR). Designer must choose the optimum impedance carefully according to the design goal.

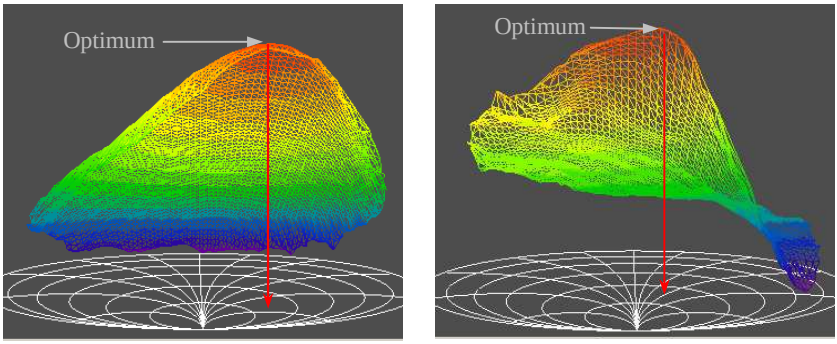


Figure 7.1 (a) Output power **(b):** adjacent channel power ratio (ACPR in absolute value vs. load reflection factor for WCDMA test signal (Test Model-1).

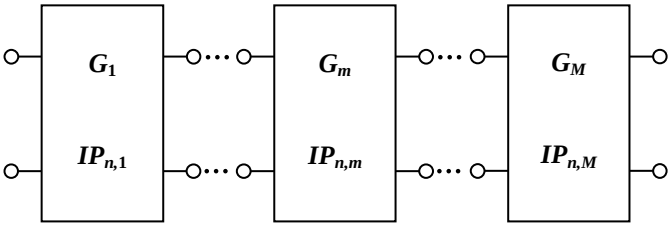


Figure 7.2 Chain of amplifying blocks with given distortion and gain.

The choice of impedance becomes tricky in the case of multistage amplifier design. Considering a design having "M" amplifying blocks as shown in fig. 7.2, eq. 7.1 represents the n^{th} order distortion power under assumption that the various blocks are matched, do not interact and the mixing of lower order distortion products generating n^{th} order components is negligible [32].

$$P_{IMD_n} = G_1^n \ldots G_M^n \, IP_n^{(1-n)} P_i^n \tag{7.1}$$

The resulting amplitude is a vector addition of the distortion power generated by the block itself and the amplified distortion power of the previous block. The worst case will be an in-phase addition and the best case will be total cancellation which is extremely rare if not designed with special technique (e.g., feed-forward).

To simplify the case, let us consider a two-stage amplifier. One important conclusion is that, to design a high dynamic range amplifier, the driving stage should be optimized for high gain and low distortion. It is better to over-dimension the driving stage in order not to generate high distortion components at the input of the power stage. The interstage match network must be carefully designed so that the output impedance of the driving stage is a compromise between power and linearity. At the same time, it should also provide good source match for the power stage.

7.3 Performance of GaN HEMT

To quantify the performance of GaN HEMT within an amplifier, we are presenting here a large packaged device characterized in a demo board (see fig 7.3). The device size is 5x8x250 µm, which means five unit cell devices bonded in parallel where each unit cell has 8 gate fingers of 250 µm length. The demo-board provides input and output matching networks with integrated DC supply. The demo-boards match the device to 50 Ω at 2 GHz based on the quarter-wavelength transformer concept. The network was simulated in ADS and realized in microstrip technology. The demo boards were then mounted on a heat sink. Characterization of the device was done with this demo

boards in a 50 Ω environment. Noise figure (NF) was measured using a commercial NF measurement system HP 8970. Linearity was determined by means of an in-house linearity measurement system.

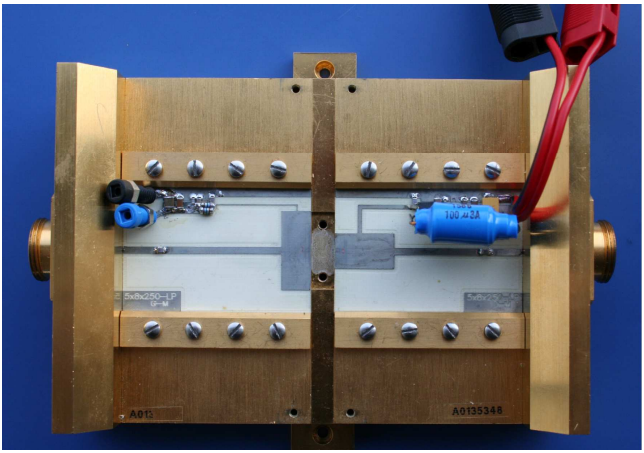


Figure 7.3 Designed demo-board with integrated bias supply mounted in the ICM test fixture.

Load-pull measurements were performed in order to check further improvement in output power. However, load-pulling yielded only negligible improvement over 50 Ω measurements, which proves that matching is already provided by the demo-boards.

The following sections present the measurement results.

7.3.1 Power performance

Power measurement was performed at 2 GHz with V_d = 28 V and V_g= -3.1 V. Results are plotted in fig. 7.4. A maximum power of 30 W is reached, with 18 dB small-signal gain and 50% PAE. P_{-1} dB is

about 44 dBm. The drain current I_d, increases due to self biasing from its quiescent value (864 mA at 10 dBm input power) to 2.43 A at 44 dBm. The resulting power density is about 3 Watt/mm.

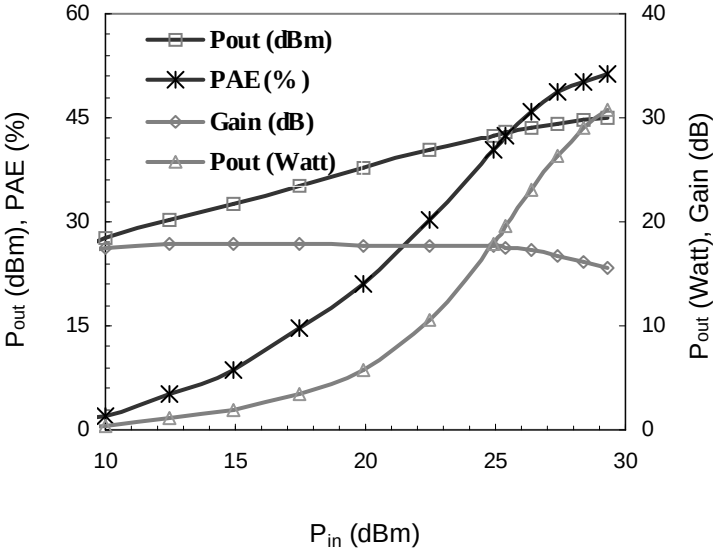


Figure 7.4 Power measurements at 2 GHz, V_d = 28 V (drain current I_d= 864 mA at P_{in} =10 dBm, it increases to I_d = 2.43 A due to self biasing).

7.3.2 Noise performance

The device is usable not only as power transistor but also exhibits attractive low noise characteristics. Fig. 7.5 shows noise figure and gain at different drain currents measured at a drain voltage of 25 V. It can be seen that the noise figure is clearly below 2 dB if operated at a drain current from 150 mA to 500 mA.

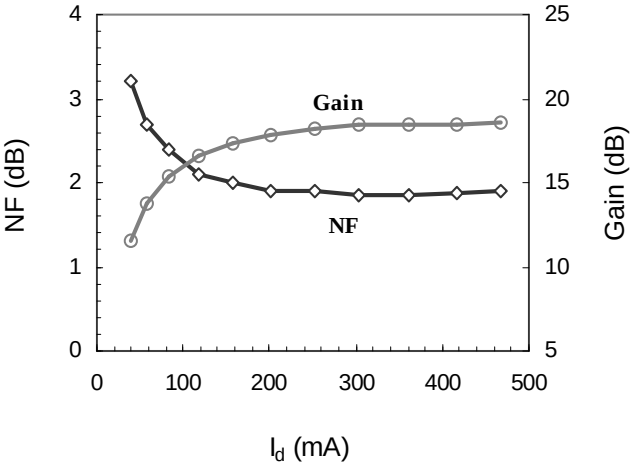


Figure 7.5 Noise figure NF and associated gain G at $V_d = 25$ V, f = 2 GHz, as a function of drain bias current I_d.

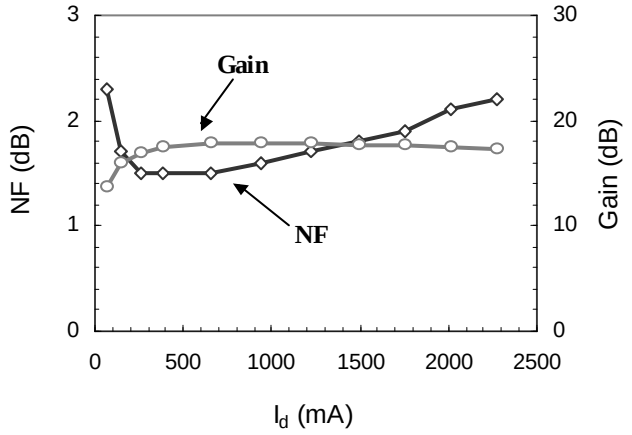


Figure 7.6 Noise figure NF and associated gain at $V_d = 15$ V, $f = 1.9$ GHz, as a function of drain current I_d.

For higher currents, NF is expected to increase further. However, for a drain voltage of 25 V, noise measurements at high drain currents are a problem due to the high dissipated DC power (e.g., 25 Watt at a current of 1 Ampere). Therefore, we characterized a transistor at a reduced drain bias of V_d =15 V in order to study the full current range. Fig. 7.6 presents the corresponding results, which exhibit the well-known FET behavior with an NF minimum around a bias current of 10% of the maximum I_d. (note that the lower drain bias causes a slight decrease of NF in general).

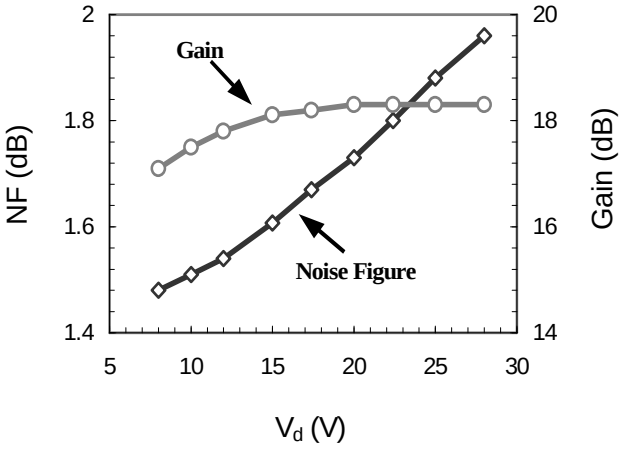


Figure 7.7 Noise figure NF and associated gain at I_d = 300 mA, f = 2 GHz, as a function of drain voltage.

To complete the data, fig. 7.7 shows noise figure if drain voltage is swept at a constant drain current of 300 mA. Generally, noise figure increases with drain voltage. Extrapolating the data of figs. 7.5..7.7, for 28V drain bias and high drain bias currents, one can expect NF to

increase from values around 2 dB for currents in the 0.2…1 A range to a level slightly below 2.5 dB for currents up to 2.5 A.

7.3.3 Linearity performance

IP3 measurements were performed with a tone spacing of 10 MHz where the first tone was fixed at 2 GHz. The bias point during the IP3 measurement was kept the same as in the power measurement (see fig. 7.4). Excellent linear characteristics are obtained as can be seen from fig. 7.8. OIP3 is more than 54 dBm. It is worthwhile to mention that the power in both of the side bands, i.e., upper and lower sideband, is almost equal which indicates no or very low memory effect and envelope distortion. We have also measured adjacent channel power ratio (ACPR) under a WCDMA standard signal (test-model-1) at approximately 10 dB power back-off from P_{-1}dB. ACPR measurements also show a good linear behavior as plotted in fig 7.9. Symmetric sideband power suggests memory-effect-free characteristics. Measured ACPR reaches -43 dBc at channel power 33 dBm which almost meets the specification for 3G standard without any linearization and/or optimized matching. (Specification for 3G base station ACPR 45 dBc and AltCPR 50 dBc [33].)

It is to be mentioned here that we have also performed a tone sweep from 50 KHz to 25 MHz and did not observe any sideband imbalance for this sweeping range. We had to restrict the tone spacing in this range due to the limited bandwidth of bias-T (45 kHz to 18 GHz) and internal modulator (40 MHz) of the vector signal generator. A tone amplitude equalization of the test signal was not possible for larger tone spacing.

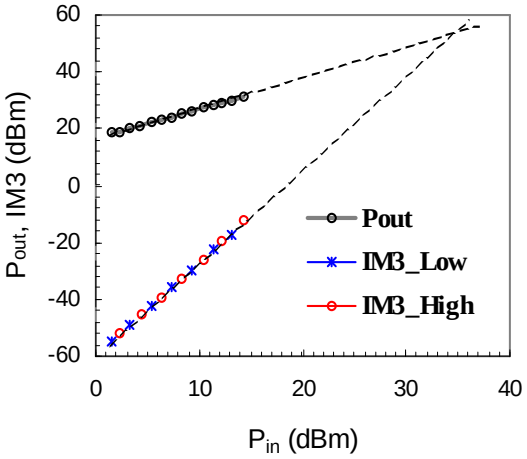
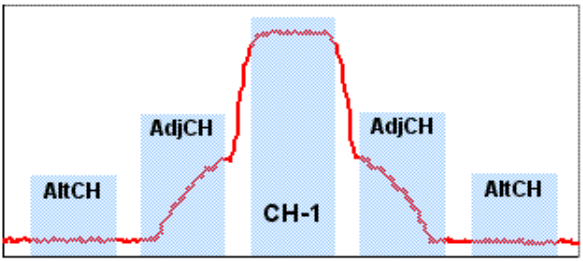


Figure 7.8: OIP3 measurement at 2 GHz bias (other data as in fig. 7.4). Measured powers correspond to single tone. For total power 3 dB should be added.



Channel BW =3.84 M Hz; Center Freq = 2 GHz;
WCDMA Test Model 1 (64 DPCH)

Device	Ch.Pwr	ACPR	AltCPR
5X8X250	33 dBm	-43 dBc	-56 dBc

Figure 7.9 ACPR measurement with a WCDMA signal (test-model-1) at 10 dB power back-off from P_{-1} dB (other data as in fig. 7.4).

Conclusions

Recent progress in AlGaN/GaN HEMT technology opened new possibilities and applications of these devices in communication circuits. Due to large band-gap and other excellent material properties, this material system is emerging as one of the main prominent players in the area of RF power devices. Due to its ruggedness and high breakdown voltage in combination with high electron transport property, among the competing technologies, AlGaN/GaN devices offer so far the highest power density up to mm waves.

In the present development phase, it is very important to characterize and analyze the device properties and performance systematically. As GaN HEMTs are targeted to be employed in the wireless communication circuits, linearity performance is one of the most important issues. In particular, in-band intermodulation distortions of wideband signals, which cannot be eliminated by using filters, must be characterized and minimized. This is the area this work contributes to.

In the field of device linearity, most of the previous work had been focused on understanding the device response under non-linear operation and external linearization. In contrast, this work considers a detailed investigation on device level nonlinearity of AlGaN/GaN HEMT. GaN technology will benefit from this work regarding device optimization, in order to improve device level linearity.

A systematic treatment starting with a model-based sensitivity analysis gives an insight regarding the influence of physical parameters on intermodulation distortions. For this purpose, a large signal model

has been used, quantifying the sensitivity of intermodulation distortion to the model parameters. This allows one to identify distortion prone physical model parameters and to sort out predominant effects. However, these model variables do not directly correlate to physical parameters. This is because the model variables are usually part of complex equation systems describing electrical behavior. Thus, one has to establish the interdependence between model and physical parameters additionally.

This analysis yields an important understanding of distortion mechanism in GaN HEMT. The transconductance (g_m) behavior, particularly the third order transconductance g_{m3}, is clearly the most important parameter responsible for third order distortion. In order to have a device with high linearity, one first has to address this point and the ideal transconductance curve would be a flat and inclination free curve over operating gate voltage range. This important understanding was used then to set the goal of a physical device simulator for optimizing the device architecture in order to minimize intermodulation distortion which is a device having high drain current $I_{d,}$ and very low absolute g_{m3} at the same time. g_{m3} can be calculated by differentiating I_d (in practice, step by step fitting and smoothing is needed).

The most important results revealed from the physical simulation are:

- The separation between the 2DEG channel and gate contact has a clear effect on linearity.
- There is a trade off between the breakdown voltage and high linearity. Higher Aluminum (Al) concentration can improve linearly at the cost of breakdown voltage.

In order to validate these findings, a number of devices with different epitaxial structures were processed, characterized and compared in terms of linearity. The effect of some special arrangements like field plate, T-gate, embedded gate was evaluated experimentally.

We explicitly investigated the effect of dynamic access resistances on linearity as this was claimed to be the main source of nonlinearity for some devices. "Hot-FET" dynamic access resistances were extracted from measured S-parameter. For our devices, dynamic access resistances showed negligible effect on linearity.

In order to achieve reliable and precise characterization results, a dedicated measurement system had to be developed based on state-of-the-art vector signal generator and spectrum analyzer with digital IF. The generator is capable of producing accurate multi-tone or wideband modulated signal whereas the spectrum analyzer taking the advantage of digital IF is capable of measuring precisely spectrum power also of very weak signals in presence of strong spectral components. However, the generator cannot deliver enough power to drive high power devices. Therefore, an external amplifier was used to amplify signal power. This driving amplifier does have intermodulation distortion and hence causes inaccuracies in the measurement results. Therefore, we have linearized this amplifier prior to measurements by taking advantage of the connectivity between signal generator and spectrum analyzer. An automatic attenuator was used for power sweep. In this way, it was possible to have a very accurate linearity measurement. The main measurement used in this work was the two-tone measurement.

A device level intermodulation distortion minimization was achieved by optimizing AlGaN layer thickness. A novel concept was

introduced to enhance the linearity of a multi-section device. As the device linearity or more specifically the higher order intermodulation distortion products are directly related to the shape of the transconductance profile, a device with high linearity can be achieved combining a number of device units having different transconductance profile. Simulation results indicate that a perfect transconductance profiles can be achieved by superposing the transconductance of precisely controlled recessed structures.

Finally, performance of a large packaged GaN HEMT is presented. This single device delivers saturated output power of 30 Watts with an small signal gain of 18 dB and IP3 is about 54 dBm. Adjacent channel power ratio ACPR measurement under a WCDMA signal shows high linearity (-43 dBc at 10 dB back-off) with symmetric sideband spectrum. Symmetry in sideband suggests that there is no device level memory effect. At the same time it has a very good noise behavior and high linearity. Noise figure is below 2 dB.

A single device, combining high performance in power, gain, noise and linearity proves the potential of GaN devices in manifold use in modern communication circuits. It opens new possibilities to design highly linear amplifiers with high dynamic range. In transceivers, low noise amplifiers (LNA) usually cannot be designed for high input power capability. Instead, in order to avoid interference from large transmitted power from the transmitter block, LNAs are equipped with filters. However, these filters are useless for in-band interferers. In telecommunication systems, in-band interferes can arise from other services sharing the same physical transmission channel, unintentional or intentional perturbation (like man made jamming signal), or even due to leakage from the same transceiver in case of full-duplex transmission [32]. In the presence of such interferer with high power,

LNAs can be easily overloaded and desensitized. High dynamic range LNAs using GaN HEMTs can help in mitigating this problem.

A further extension of this work may basically cover two aspects: first, regarding measurements and characterization and second, further investigation on realizable technological aspects to enhance linearity.

A reliable measurement system to perform tone sweep up to very wide tone spacing is one of the most useful characterization. An accurate real time phase detection of the distortion products is another very interesting subject. By detecting the phase, it will be possible to measure distortion products precisely providing accurate calibration even with a distorted input signal. This will eliminate the linearization procedure used in our measurement system. On the other hand, measuring the phase, one has information about real and complex part of the distortion products, which can be very useful to optimize devices. Linearity investigation and optimization of devices for different amplifier classes, is also a very interesting field of research. A detailed investigation on base-band and harmonic termination impedances influencing linearity should not be ignored.

From technology side, realization of the highly linear devices based on superposition concept using precise recess technique is a challenge. The method of optimizing device architecture opens a door to explore many other concepts (e.g., optimized complementary channel, delta doping, back barrier technique etc.) to enhance linearity at the device level.

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List of Acronyms

2DEG	Two Dimensional Electron Gas
AMPS	Advance Mobile Phone System
ACPR	Adjacent Channel Power Ratio
AltCPR	Alternate Channel Power Ratio
AlGaN	Aluminium Gallium Nitride
BER	Bit Error Rate
C/I	Carrier to Intermodulation Ratio
DC	Direct Current
DL	Down Link
DPCH	Downlink Dedicated Physical Channel
DUT	Device Under Test
E-Fuse	Electronic Fuse
EVM	Error Vector Magnitude
FBH	Ferdinand-Braun-Institut für Höchstfrequenztechnik
FET	Field Effect Transistor
FP	Field Plate
f_T	Transit Frequency
g_m	First order transconductance
g_{m3}	Third order transconductance
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GPIB	General Purpose Interface Bus
GSM	Global System for Mobile Communication. (originally from : Groupe Spécial Mobile)
HEMT	High Electron Mobility Transistor
HRXRD	High Resolution X-Ray Diffraction
IM3	Third Order Intermodulation Product
IP3	Third Order Intercept Point
IPTOI	Integrated Third Order Intercept Power

LDMOS	Laterally Diffused Metal Oxide Semiconductor
Mbps	Megabit per second
MDS	Minimum Detectable Signal
MOCVD	Metal-Organic Chemical Vapour Deposition
NF	Noise Figure
PA	Power Amplifier
PSA	Performance Specrum Analyzer
PSG	Performance Signal Generator
QAM	Quadrature Amplitdre Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SEM	Scanning Electron Microscope
SiN	Silicon Nitride
SiC	Silicon Carbide
TOI	Third Order Intercept
TWT	Travelling Wave Tube
UMTS	Universal Mobile Telecommunications System
UWB	Ultra Wide Band
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

Appendix-I

Extracted model parameters for a 2x250 μm GaN HEMT

Idsmod=1

Ipk0=0.281812 A

Vpks=-2.10402 V

Dvpks=0.105965 V

P1=0.331237

P2=-0.0349138

P3=0.0229953

Alphar=0.392279

Alphas=4.39322e-005

Lambda=0.00310349

B1=0.837033

B2=2.63834

Lsb0=0.0

Vtr=60 V

Vsb2=0 V

Cds= 1320 fF

Cgspi=350 fF

Cgs0 = 115.759 fF

Cgdpi = 135 fG

Cgd0 = 99.3006 fF

Cgdpe = 0 fF

P10 = 9.34539

P11 = 1.96804

P20 = 1.22132

P21= 0.677367

P30 = 0.729832

P31 = 0.00483836

P40 = 2.20453

P111 = 0

Ctherm= 0.001 F

Tclpk0= -0.000979363

TcP1=-0.00104375

TcCgs0=0.00

TcCgd0=0.00

TcLsb0=0.0

Tamb=25

Lj=0.0079A

Pg=2.71183

Vjg=0.5755 V

Pi= 2.5 Ω

Rgd=14 Ohm

Rcmin=580.895 Ω

Rc=5.69436 Ω

Crf= 10 μ f

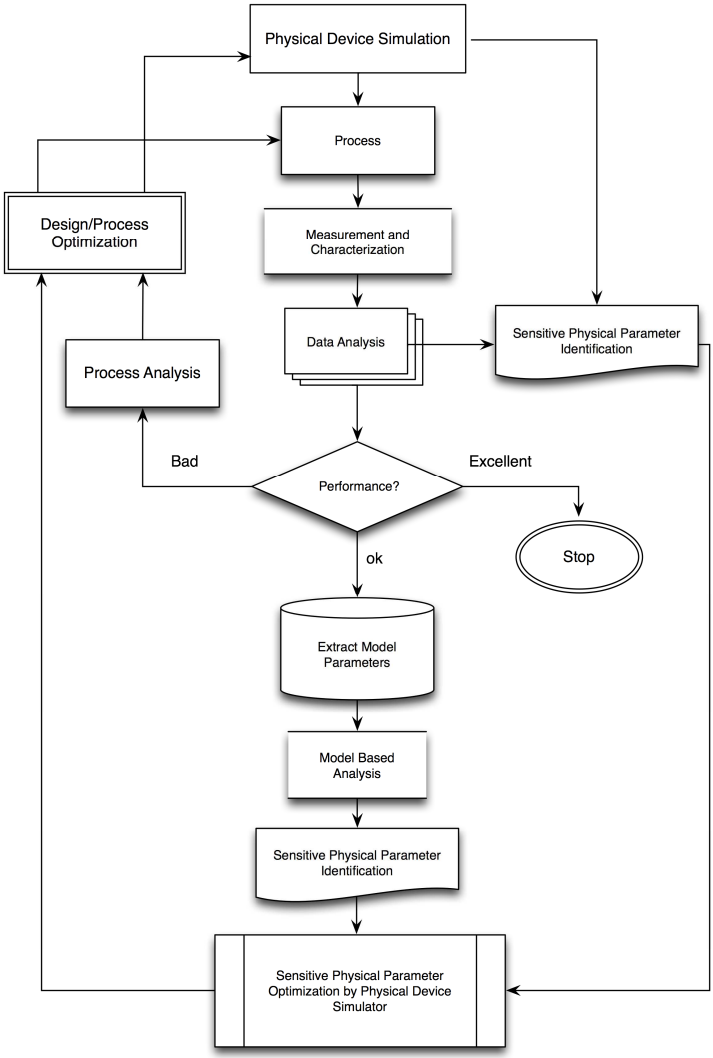
Rcin=100 k Ω

Crfin = 10 fF

Tau = 2.8 psec

Appendix-II

Flowchart of the device optimization procedure



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