Experimental Investigation of GaN Power Devices

Dynamic Performance, Robustness and Degradation

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بِسْمِ اللَّهِ الرَّحْمَٰنِ الرَّحِيمِ

وَقُلِ اعْمَلُوا فَسَيَرَى اللَّهُ عَمَلَكُمْ وَرَسُولُهُ وَالْمُؤْمِنُونَ

صدق الله العظيم

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Nasser

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Abstract

Over the next decade, the power electronics will require a new generation of semiconductor devices that are smaller, cheaper and more efficient. Technology changes will radically influence the power electronics business in different industries, including the automotive, renewable energy, motion and rail industry. The key features of highly efficient power converters comprise high switching performance and low on-state resistance at high power and high frequency. In comparison with silicon (Si), Gallium Nitride (GaN) semiconductors boast excellent features when compared to silicon (Si), particularly for power electronics applications. The development of power semiconductor devices has always been a driving force for power electronics systems. For a long time, silicon-based power devices have dominated both power electronics as well as power system applications. As the requirements for electric energy continue to grow, silicon (Si) devices are beginning to face some fundamental limits in performance due to the inherent limitations of Si material properties, which make them incompetent for future demands, especially in high-voltage, high-efficiency, and high-power-density applications. By applying GaN-based rather than state-of-the-art Si-based power devices, power converter efficiency can be significantly increased. In this dissertation thesis, the current collapse phenomena in Gallium Nitride (GaN)-based High Electron Mobility Transistors (HEMTs) are investigated. GaN HEMT has traditionally suffered from the so-called *trapping effect*, which leads to substantial degradation and instability of the on-state resistance. Dynamic impacts such as a high switching frequency at high-power transients are playing a major role by the degradation of the on-state resistance. It is evident that the number of switching transients substantially influences the increase of the R_{DSON}, suggesting that this increase is attributable to a current collapse in GaN HEMTs. Thermal effect is also a reason for the increase of on-state resistance on account of the increase of the junction temperature at high currents. To distinguish between thermal and trapping effects in GaN HEMT, different dynamic tests were carried out and possible interpretations have been made. A new measurement method to extract the dynamic on-state resistance R_{DSON} of GaN HEMTs is also proposed. Such a method is an essential condition to conduct any R_{DSON} measurement test. It permits an accurate measurement of R_{DSON} from 200 ns after turn-on to any arbitrary time and is feasible for operation at high switching frequencies up to 1MHz. Applying this measurement method, different normally-off and normally-on GaN HEMTs grown on Si and SiC substrate are experientially investigated at different blocking voltages, switching currents, switching frequencies and switching speeds. The results are compared to the commercial state-of-the-art super-junction Silicon (Si) MOSFET operating under hard-switching conditions. Robustness and reliability of GaN HEMT is an essential issue. A short-circuit event is a serious and potentially destructive operation condition for a power transistor and needs to be turned-off quickly and safely. To define strategies for how to improve the reliability of a power device, it is necessary to understand the failure dynamics during a short circuit. A comprehensive experimental study

focusing on the short-circuit capability of different types of 600V power transistors based on Si, SiC and GaN is provided. Failure mechanisms during short-circuit conditions of the investigated power transistors are analyzed and a possible theoretical explanation is given. The investigation of GaN-based Schottky diode feasible for high frequency operation and rated at 600V/20A represents another topic presented in this thesis. Static and dynamic characteristics of the diode are experimentally evaluated at varying temperatures and compared to commercially available Silicon Carbide (SiC) Schottky diodes. Lastly, an Interleaved Buck Converter (IBC) based on the investigated 600V normally-off GaN HEMT is used and tested in CCM, whereas the degradation and instability of the on-state resistance is assessed and compared with the results achieved during the double pulse experiments.

Kurzfassung

Im nächsten Jahrzehnt wird die Leistungselektronik eine neue Generation von Halbleiterbauelementen, die kleiner, preiswerter und effizienter sind, benötigen. Technologieänderungen werden den Leistungselektronikmarkt in verschiedenen Branchen, einschließlich der Automobil-, erneuerbare Energien und Bahnindustrie, sehr stark beeinflussen. Die Hauptmerkmale hocheffizienter Stromrichter sind eine hohe Schaltleistung und ein geringer Leitwiderstand bei hoher Leistung und hoher Frequenz. Im Vergleich zu Silizium (Si) zeichnen sich Galliumnitrid (GaN) Halbleiter, insbesondere für Leistungselektronikanwendungen, durch hervorragende Eigenschaften aus. Die Entwicklung von Leistungshalbleiterbauelementen war schon immer eine treibende Kraft für Leistungselektroniksysteme. Seit langer Zeit dominieren Silizium basierte Bauelemente die Leistungselektronik, wie auch deren Anwendungen. Da die Anforderungen im Bereich der Energieübertragung und -wandlung stetig weiter wachsen, stößt Silizium an seine physikalischen Grenzen, auf Grund seiner Materialeigenschaften, die es für zukünftige Anforderungen ungeeignet macht, vor allem bei Hochspannungsanwendungen mit hoher Leistungsdichte. Durch die Anwendung von GaN-basierten anstelle von hochmodernen Si-basierten Leistungsbauelementen kann der Wirkungsgrad des Leistungssystems deutlich erhöht werden. In dieser Dissertation wird das Phänomen des so genannten „Stromkollapses“ in GaN-basierten High Electron Mobility Transistors (HEMTs) untersucht. Der GaN HEMT hat traditionell unter dem sogenannten „Trapping-Effekt“ gelitten, was zu einer erheblichen Verschlechterung und Instabilität des Einschaltwiderstands (on-state resistance) führt. Dynamische Effekte, wie eine hohe Schaltfrequenz bei schnellen Schaltvorgängen spielen eine wesentliche Rolle bei der Verschlechterung des on-state Widerstandes. Es ist offensichtlich, dass die Anzahl der Schaltvorgänge die Zunahme des R_{DSON} wesentlich beeinflusst, was darauf hindeutet, dass diese Zunahme auf einen Stromzusammenbruch in GaN HEMTs zurückzuführen ist. Der thermische Effekt hat auch Einfluss auf die Erhöhung des on-state Widerstands bei hohen Strömen. Zur Unterscheidung zwischen den thermischen und den Trapping-Effekten in GaN HEMTs, wurden verschiedene dynamische Tests durchgeführt. Eine neue Messmethode zur Extraktion des dynamischen On-State Resistance R_{DSON} von GaN HEMTs wird ebenfalls vorgeschlagen. Ein solches Verfahren ist eine wesentliche Voraussetzung für die Durchführung eines R_{DSON}-Messversuchs. Es ermöglicht eine genaue Messung des $R_{DSON,}$ ab 200ns nach dem Einschalten, und ist für den Betrieb bei hohen Schaltfrequenzen bis zu 1 MHz möglich. Bei der Nutzung dieses Messverfahrens werden verschiedene Anreicherung- und Verarmungstypen-GaN HEMTs (normally-on, normally-off) basieren auf Si und SiC-Substrat bei verschiedenen Sperrspannungen, Schaltströmen, Schaltfrequenzen und Schaltgeschwindigkeiten experimentell untersucht. Die Ergebnisse werden mit einem aktuellen (Stand der Technik) Super-Junction-Silizium-MOSFET unter hartschaltenden funktionalen Bedingungen verglichen. Robustheit und Zuverlässigkeit von GaN HEMTs ist ein wesentliches Thema. Ein Kurzschlussereignis ist eine ernsthafte und potenziell zerstörerische

Betriebsbedingung für einen Leistungstransistor und muss schnell und sicher abgeschaltet werden. Um Strategien für die Verbesserung der Zuverlässigkeit eines Leistungshalbleiters zu definieren, ist es notwendig, die Ausfalldynamik während eines Kurzschlusses zu verstehen. Diese Arbeit enthält eine umfassende experimentelle Studie, die sich auf die Kurzschlussfähigkeit verschiedener Typen von 600V-Leistungstransistoren auf der Basis von Si, SiC und GaN konzentrierte. Ausfallmechanismen bei Kurzschlussbedingungen der untersuchten Leistungstransistoren werden analysiert und eine mögliche theoretische Erläuterung gegeben. Die Untersuchung einer GaN-basierten Schottky-Diode (600V, 20A), die für den Hochfrequenz-betrieb geeignet ist, stellt ein weiteres Kapitel dieser Arbeit dar. Die statischen und dynamischen Eigenschaften der Diode werden bei unterschiedlichen Temperaturen experimentell ausgewertet und mit einem Stand der Technik Silicon Carbide Schottky-Dioden verglichen. Schließlich wird ein Interleaved Buck Converter (IBC) basierend auf dem untersuchten 600V normal-off GaN HEMT verwendet und im Dauerbetrieb getestet. Die Instabilität des Einschaltwiderstands wird bewertet und mit den Ergebnissen verglichen, die während der Doppelpulsexperimente erzielt wurden.

Table of Contents

1 Introduction

The Gallium nitride (GaN) High-Electron-Mobility Transistor (HEMT) has rapidly developed in recent years. Research and development focused on GaN power semiconductors began several years ago. Since the early 1990s, gallium nitride has been regarded as a very promising semiconductor material for highly efficient power conversion [1]-[12]. Modern power converters have to be characterized by high reliability and high efficiency at high power density and high ambient temperature. The high-performance power transistor is the essential requirement of such innovation of power conversion technology. The number of GaN-based devices being manufactured continues to grow, covering applications ranging from low-power voltage regulators to high-power systems. In comparison with state-of-the-art silicon MOSFET, GaN High-Electron-Mobility Transistor (HEMT) boasts a much better figure of merit and demonstrates potential for high-power, high-frequency applications. Applying GaN-based power devices rather than state-of-the-art Si-based variants results in substantially increased power converter efficiency and power density. In order to redeem the high potential of GaN power semiconductors, academics, research institutions and industries around the world have worked intensively over the past 25 years. The result is that, since 2013, various enhancement modes, depletion mode and cascade-configured GaN power transistors up to 650V have become commercially available. This chapter begins by stating the objectives and problem definition of the research work. Following that, an introduction is given concerning the current benefits and advantages of GaN power semiconductors in comparison with Si and other wide-bandgap (WBG) materials. Next, an overview is presented of the application areas and the state-of-the-art of GaN-based high-power electronics. Lastly, the outline of the thesis is provided along with the thesis structure and its content.

1.1 Research Objective and Motivation

Gallium nitride high-electron-mobility transistor (GaN HEMT) has become a promising device for high-frequency [1], high-density power converters [2]-[12]. Efficiency and power density are becoming more and more a major concern in the power electronics industry, since the demand for efficient and compact power converters has increased substantially [13]-[16]. Different industries such as automotive and solar technology require smaller, faster, cheaper and more efficient power semiconductor devices. Also to consider is that the silicon-based power transistors such as Si MOSFET and Si IGBT are reaching their limits. Thus, the first question one should ask in this context is whether Si-based power transistors are on their way out. It is well known that GaN and silicon carbide (SiC) boast excellent features and properties in comparison with silicon and are expected to grow faster over the next decade than Si-based power semiconductors. Fig. 1.1 shows the specific on-resistance versus breakdown voltage for Si, GaN and SiC and compares the GaN HEMT with state-of-the-art silicon power FETs. Obviously, the specific on-resistance limit of GaN is quite distant from that of silicon and SiC [2]. The GaN HEMT demonstrates a superior relationship between on-state resistance and breakdown voltage; this is attributed to the high electron mobility and the electrical field strength in the channel. A small on-resistance at high breakdown voltage results in a reduction of the size of the device, which leads to a power density increase.

Two state-of-the-art Si-based power device solutions are commonly used in the power electronics area: the super-junction power MOSFET (used in applications from 300V to 900V) and the IGBT (up to 6.5kV applications). In contrast, current GaN HEMT solutions with their various technologies (depletion mode, enhancement mode or cascode-configuration HEMTs) are available for applications up to 600V. Can GaN power HEMTs at some point displace the Si-based power devices from the 600V applications (900V-applications in the best case)? The answer to this question is not a simple one. Tradeoffs exist between the technologies on account of different aspects, including the cost and size of semiconductor wafers, cost of manufacturing the device and also what industrial customers are prepared to pay for a device. On the other hand, super-junction MOSFET performance has also been enhanced, with the on-state resistance and switching speed close to that of the GaN power HEMT.

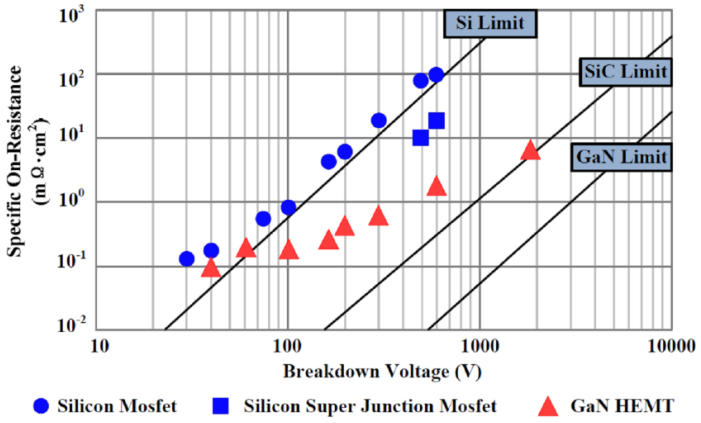


Fig. 1.1 Specific on-resistance versus breakdown voltage for GaN, SiC, Si [17].

One must also consider that GaN HEMT is not the perfect power device. It is hampered by a lattice mismatch, not to mention the so-called trapping effects. Robustness and reliability issues as well as low thermal conductivity represent additional weak points. Although 600V e-mode, depletion mode and cascode-configured GaN power transistors are commercially available, it is not clear whether the Si-based 600V-application market will be largely displaced by GaN in the near future. Nevertheless, GaN and SiC semiconductor technologies are undoubtedly making an impact on the power electronics market and industry. Despite the commercial availability of GaN HEMTs for 600V-applications, as noted above the robustness, reliability and stability of the power device remain problematic issues. In this work, the basic topics such as the degradation of dynamic on-state resistance at different dynamic impacts and the robustness of GaN HEMT in short-circuit mode are studied and analyzed. Additionally, the testing and characterising of high-frequency power semiconductors requires specific measurement and driving techniques that need to be carefully selected.

1.2 State-of-the-Art

In recent years and right up to 2017, several industries and research institutions have been focused on GaN research and development, recently working on GaN-EpiWafer and GaN-based power devices, with many cutting-edge results. The Table 1.1 below lists the currently developed GaN-based devices and epiGaN wafer platform from companies and academic institutions around the world:

Industry & Academy	Country	GaN Epiwafer/Power Devices (CR: Currently Research, CA: Commercially Available)
FBH Berlin	Germany	CR: 600V/2…20A/150… 65mΩ normally-on and normally-off GaN HEMT. 600V/2…10A/128…85mΩ, GaN Schottky Diode
GaN System	Canada	CA: 650V/7…60A/200…25mΩ normally-off GaN HEMT. 100V/45…90A/15…7mΩ normally-off GaN HEMT. CR: 900V-based Normally-off GaN HEMT
Transphorm Inc	USA	CA: 650V/31A/35mΩ cascode configured GaN HEMT, 600V/25A/52mΩ cascode configured GaN HEMT. CR: 900V-based Normally-off and cascode GaN HEMT
Panasonic	Japan	CA: 600V/15A/65mΩ normally-off GaN HEMT. CR: 850V-based Normally-off.
International Rectifier	USA	CR: 600V GaN HFET and GaN Schottky diode.
EPC	USA	CA: 300V/6A/120mΩ normally-off GaN HEMT.
MicroGaN	Germany	CA: 600V 3D-GaN HFET Normally-off Ron: 5mΩ/cm² (Si-MOSFET+GaN).
Dowa Electronics Materials	Japan	CA: 3", 4" and 6" inches EpiWafer. AlGaN/GaN-On-Si HEMT. HV resistance (1000V)
AZZURRO	Germany	CA: 6" inches (150 mm) EpiWafer AlGaN/GaN-On-Si HEMT. Crack-free.
EpiGaN	Belgium	CA: 6" inches EpiWafer ALGaN/GaN-on-silicon. 150mm and 200mm Crack-free.
NTTAT	Japan	CA: 6" inches EpiWafer AlGaN/GaN-On-Si Crack-free.
Powdec	Japan	CA: 4" inches EpiWafer AlGaN/GaN-On-Si and AlGaN/GaN-On-SiC.
Texas Instument	USA	CA: 600V Normally-off GaN HEMT. Integrated solution: transistor and gate driver

Table 1.1 Achievement of devices and epi-wafer platform for GaN power semiconductor at the end of 2017.

1.3 Dissertation Contents

This thesis is organized as follows:

Chapter 1: The first chapter introduces the benefits of Gallium Nitride (GaN) power semiconductors. Also presented are the fundamentals of the gallium nitride semiconductors, the corresponding research background, the motivation, and finally the outline of the thesis along with the thesis structure and its content.

Chapter 2: The experimental equipment and driving techniques used during the work are presented in this chapter, which is divided into three parts. The first part shows the experimental laboratory setup including all measurement tools and sensors. The second part introduces the high-speed gate drive circuitry in order to drive the high and low sides normally-off and normally-on GaN HEMTs. Conventional and resonant gate drivers are implemented. The third task presented in this chapter is the design of an FPGA-based control system used for experimental investigation purposes.

Chapter 3: This chapter discusses the static and switching characteristics of the investigated 400V and 600V normally-on (depletion mode) and normally-off (enhancement mode) GaN HEMTs that are being developed at the Ferdinand Braun Institute (FBH Berlin).

Chapter 4: In this chapter, a systematic study is presented of the dynamic on-state resistance of GaN HEMT at high voltage operation. The so-called trapping effects play the major role in the degradation of R_{DSON} of the GaN HEMTs. This degradation and the related phenomena are investigated. Also, a new measurement method to extract the dynamic on-state resistance R_{DSON} of GaN HEMTs is proposed. The proposed method allows an accurate measurement of R_{DSON} from 200 ns after turn-on to any arbitrary time and is feasible for operation at high switching frequencies up to 1MHz. Applying this measurement method, different GaN HEMTs grown on Si and SiC substrate are investigated at different blocking voltages, switching currents, switching frequencies and switching speeds.

Chapter 5: This chapter discusses the static and switching characteristics of two 600V/2A and 600V/8A GaN Schottky diodes. The results are compared to state-of-the-art SiC Schottky diodes and soft recovery p-n Si diodes. All devices are tested varying the junction temperature

Chapter 6: In this chapter, a comprehensive experimental study is presented focusing on the short-circuit capability of different types of 600V power transistors based on Si, SiC and GaN. Failure mechanisms during short-circuit conditions of the investigated power transistors are analyzed and a possible theoretical explanation is provided.

Chapter 7: The implementation and analysis of an interleaved buck converter IBC based on normally-off GaN HEMT operated at high-switching frequency in CCM are presented. The converter is tested also with other Si, SiC and GaN power transistors and the efficiency results are compared.

Chapter 8: The last chapter concludes and summarizes the results obtained during this work.

1.4 Scientific Publications Related to this Dissertation

Parallel to each stage of this work, scientific paper have been published in an IEEE conference or journal between 2012 and 2016.

Paper I, [18] "High Speed Gate Driver Design for Testing and Characterizing WBG Power Transistors".
N. Badawi, P. Knieling and S. Dieckerhoff. IEEE conference. EPE-PEMC 2012, Novi Sad, Serbia.

Paper II, [19] "Switching Characteristics of 200V Normally-off GaN HEMTs",
N. Badawi, O. Hilt, S. Dieckerhoff, E. Bahat-Treidel and J. Würfl. PCIM Europe 2013, Nürnberg, Germany.

Paper III, [20] "Switching Performance of 400V Normally-on and Normally-off GaN HEMTs"
N. Badawi, O. Hilt, S. Dieckerhoff, E. Bahat-Treidel, and J. Würfl. WOCSDICE 2013, Germany.

Paper IV, [21] "Evaluation of 600V GaN and SiC Schottky-Diodes at Different Temperatures"
N. Badawi, E. Bahat-Treidel, S. Dieckerhoff, O. Hilt, and J. Würfl. IEEE conference. EPE-ECCE 2013 Lile, France.

Paper V, [22] "A new Method for Dynamic Ron Extraction of GaN Power HEMTs"
N. Badawi, S. Dieckerhoff. PCIM 2015, Nürnberg, Germany.

Paper VI, [23] "Investigation of the Dynamic On-State Resistance of 600V Normally-off and Normally-on GaN HEMTs".
N. Badawi, O. Hilt, E. Bahat-Treidel, J. Böckler, J. Würfl and S. Dieckerhoff, IEEE conference. ECCE 2015, Montreal, Canada.

Paper VI, [24] "Investigation of the Dynamic On-State Resistance of 600V Normally-off and Normally-on GaN HEMTs"
N. Badawi, O. Hilt, E. Bahat-Treidel, J. Böckler, J. Würfl and S. Dieckerhoff. IEEE Transactions on Industry Applications, 2016. Vol 52, pp. 4955 – 4964.

Paper VIII, [25] "Robustness in Short-Circuit Mode: Benchmarking of 600V GaN HEMTs with Power Si and SiC MOSFETs"
N. Badawi, A. E. Awwad, S. Dieckerhoff. IEEE conference. ECCE 2016, Milwaukee, USA.

1.5 Dissertation Structure

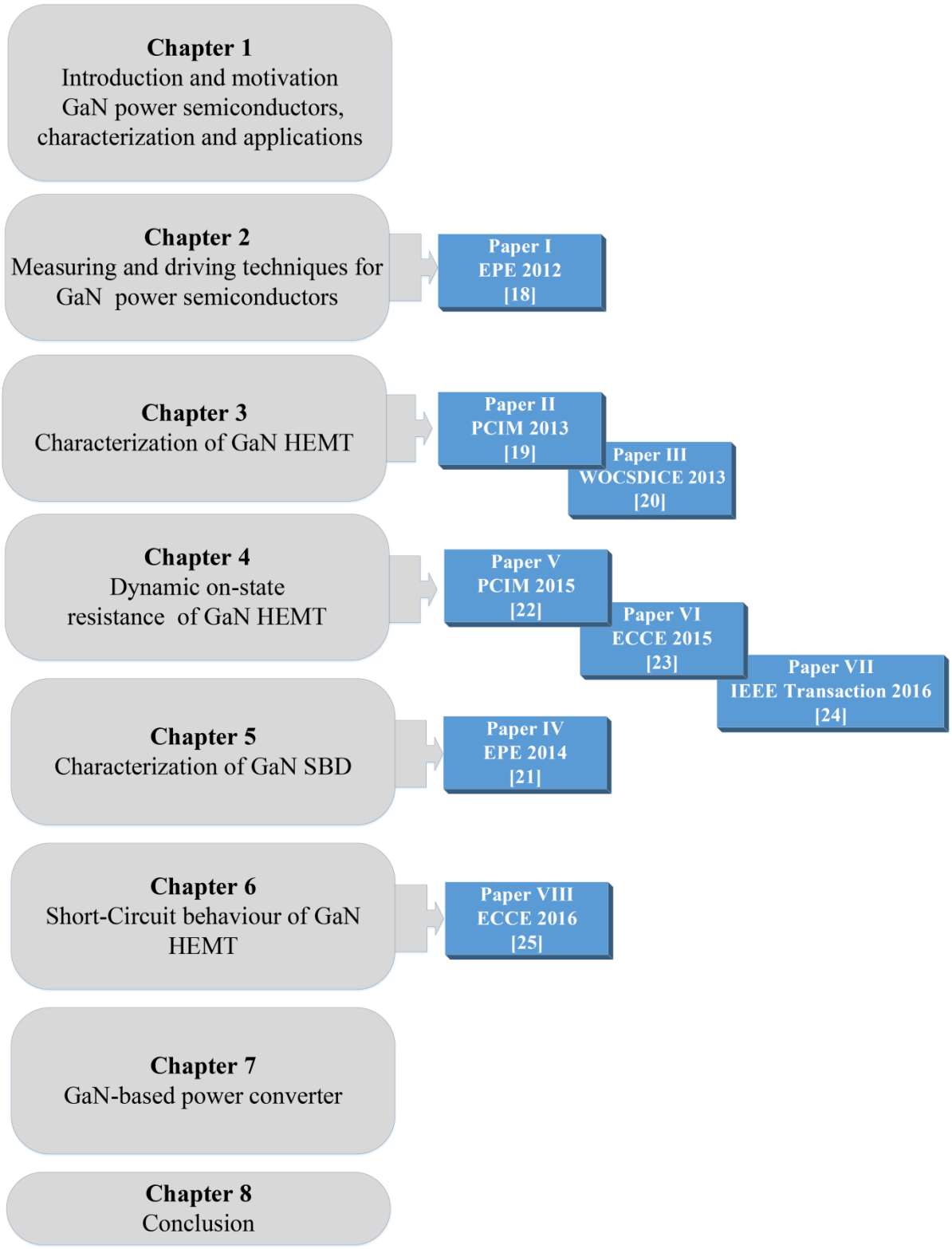


Fig. 1.2 Dissertation structure

2 Measurement and Driving Technique for GaN HEMT

Special measuring and driving techniques are necessary for experimental work dealing with high-frequency power semiconductors such as gallium nitride (GaN) and silicon carbide (SiC). The experimental environment (e.g., sensors, gate drivers and test stand equipment) has to be carefully and precisely designed in order to obtain accurate experimental results. A construction of an experimental test stand was essentially necessary for investigating high-voltage high-frequency power devices. Only single and double pulse signals could be generated with this test stand, however. Thus, a new control platform needed to be designed that could be employed for the driving purposes of GaN power HEMTs in continuous operation, where different functions could be utilized like precisely setting a few nanosecond dead-time between two PWM signals, or to generate an exact number of pulses for the characterization of the dynamic on-state resistance of GaN HEMT. For this purpose, an optimal design choice was the FPGA-based control system. The third part of this chapter describes the design of the gate driver for GaN power HEMTs. The implemented gate driver is used for providing a solution for GaN-based high voltage applications up to 600 V. It is based on the conventional MOSFET driver which is capable to switch on and off the GaN devices in less than 20 nanoseconds.

2.1 Test Environment

2.1.1 Experimental Setup

Dynamic device characteristics are typically evaluated in a buck converter, both in double pulse tests as well as in continuous switching operation. Fig. 2.1 depicts the overall test set-up schematic. Fig. 2.2 shows the standard double pulse test (DPT) circuit employed to characterize the power switches. It consists of the buck converter with inductive load, the gate driver and measurement equipment. Since the parasitic inductance in a high-voltage high-frequency power converter is substantially impactful on the turn-on and turn-off transients, special care was needed to minimize the effect of the parasitics by using a very low inductive power loop. The test bench is controlled using the PC-based software "Labview." The pulse blaster card TDS100 from National Instruments generates outgoing pulse signals, which are transmitted over fiber-optic cable to the test circuit. The test set-up measurement signals are obtained using two digital storage oscilloscopes (DSO) with 400 MHz bandwidth and four measuring channels each. The dc link voltage of the test circuit is provided by the capacitor charging device HCK 800M. Based on the required current and voltage measuring points the values of the clamped inductive load L and the DC capacitance C_{DC} have been calculated. These values are 740 µH and 120 µF. Fig. 2.4 depicts the typical inductive double-pulse switching waveforms, the gate source voltage V_{GS}, drain source voltage V_{DS} and drain current I_D. As seen from the figure, at the end of the first pulse and beginning of the second pulse the device's switching transients can be captured under the pre-set drain-source voltage and drain current conditions. The investigated diodes are also tested under typical hard switching conditions applying the dynamic test circuit given in Fig. 2.3. For the measurement of a high-speed switching signal (exceeding 5ns), which is to be transmitted over a 100 cm coaxial cable, all oscilloscopes and probes should have at least a bandwidth of 200 MHz. Power devices based on GaN or SiC can switch on and off in a few nanoseconds. Such switching speed re-

quires sufficient bandwidth of the measurement tools in order to capture the fast rising and falling edges of the transient.

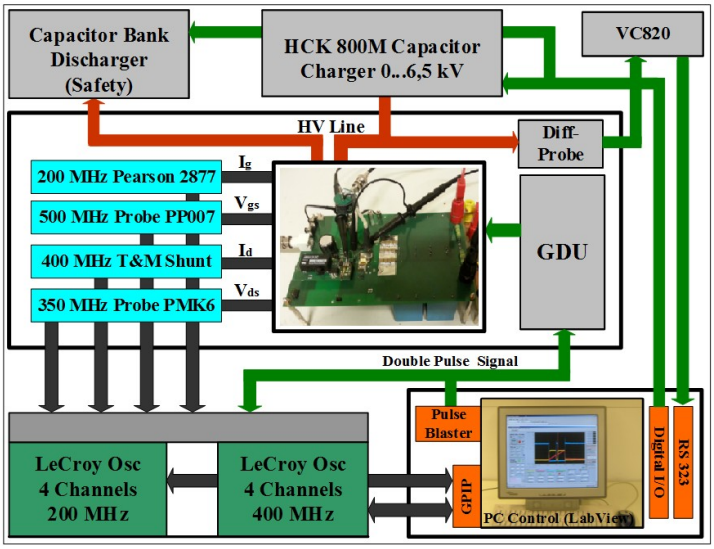


Fig. 2.1 Structure of the test set-up, the test bench is controlled with the PC-based software “Labview.”

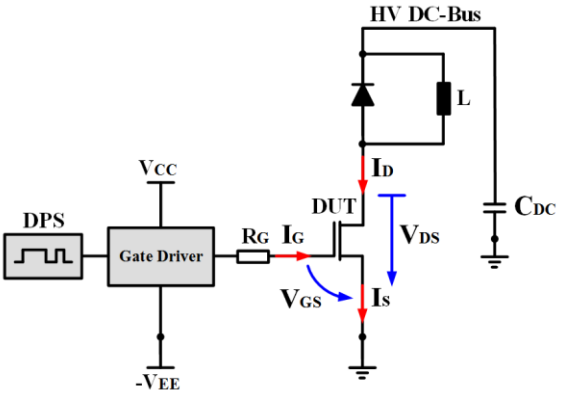


Fig. 2.2 Dynamic circuit for transistor characterization

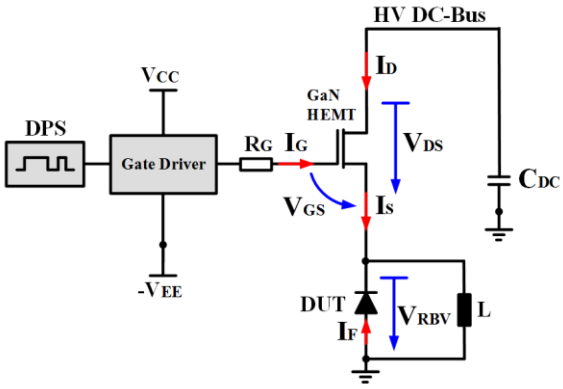


Fig. 2.3 Dynamic circuit for diode characterization.

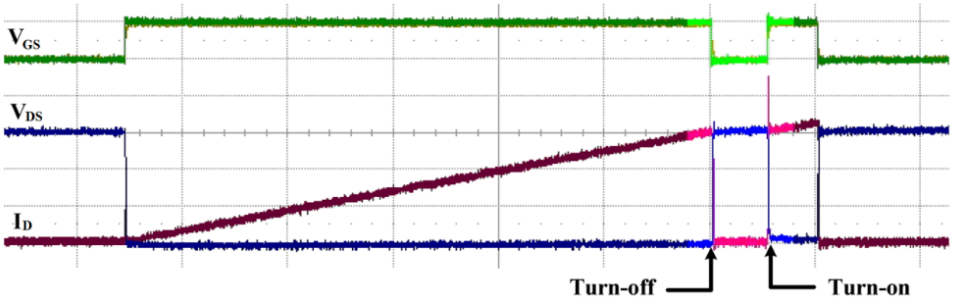


Fig. 2.4 Typical double-pulse switching waveforms.

The rising time t_r of the drain source voltage V_{DS} can reach 10 ns at 600 V, and the drain current I_d can rise even faster with 5 ns at rated current. To provide suitable measurement tools for capturing V_{DS}, I_D and the gate voltage V_{GS}, the required effective bandwidths of the switching transients of the measured signals are calculated. The effective bandwidth of the signal slope can be calculated using the following rule [51]. It is important to leave at least four times margin in order to capture the high-speed ringing of the measured signal.

$$F_{Bandwidth} = \frac{0.35}{t_r} \tag{2.1}$$

Fig. 2.5 presents the sensors currently being used at wide range currents and frequencies. The measurement requirements and equipment of the test set-up are summarized in Table 2.1. All of the cable bandwidths have to be sufficient for the application while also being matched to the DSO input channels. The bandwidth of voltage probes employed in the test is 500 MHz. This is sufficient for our fast voltage transients (7 ns – 9 ns). The high-speed current transients of GaN HEMTs are typically measured either by using a high bandwidth shunt (T&M shunt BW_{max} = 400 MHz) or a Person Sensor (BW_{max} = 200 MHz).

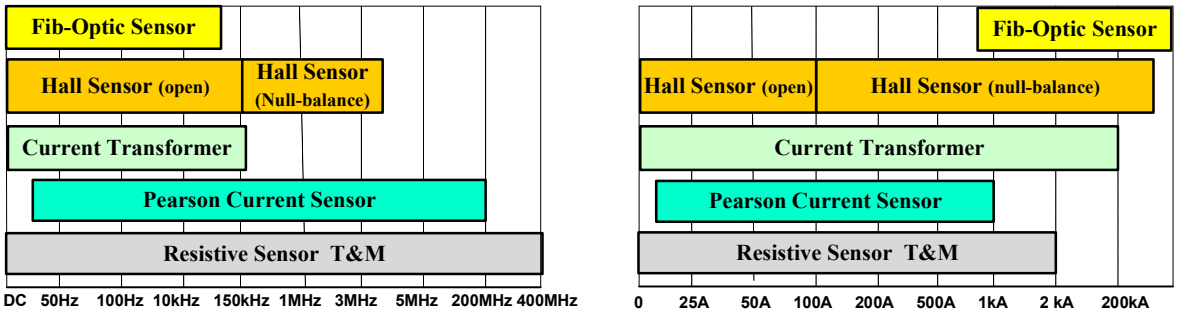


Fig. 2.5 Different current sensors with different measuring capabilities [51].

Signal	Rise/Fall Time	Measurement Equipment
V_{DS_GND}, V_{GS_GND}	< 10ns	500 MHz DSO, Probe PP007
V_{DS_Differ}	< 10ns	400 MHz PMK PS-02, Diff-Probe
I_D, I_S, I_G	< 5ns	200 MHz Pearson 2877

Table 2.1 Measurement equipment.

The incorporation of the 400 MHz T&M shunt in the setup led to further disturbance in the power loop, while the ringing was substantial in the measured signal. Thus, it was decided that the Pearson sensor with 200 MHz would be employed. Last, one must also consider that different types of probes feature different propagation delays. If the propagation delays are not compensated, they will prompt serious timing misalignment for transients and this will result in wrong conclusions when evaluating power losses [51].

2.2 Gate Drivers for GaN HEMT

A gate driver used to drive a power transistor is basically a power amplifier that takes a low power control signal from the processor unit circuit at specific switching frequency and amplifies it in order to drive the power transistor. In this section, two different gate driver concepts for GaN HEMT are discussed. The first driver is a conventional gate driver, which is based on a single complementary IC driver that is normally used to drive a power MOSFET. The second gate driver is based on the resonant topology that is introduced in [52][53]. Fig. 2.6 shows the power and gate currents during the turn-on and turn-off processes. The central component of the conventional gate driver is the commercially available IC devices which are provided by different manufacturers (Figure A 1.1). These components are a high frequency driver ICs that can drive GaN HFETs and SiC MOSFET up to several MHz while having a relatively high peak current capability. A comparison of the corresponding manufacturing details of these drivers is summarized in Appendix A 1.

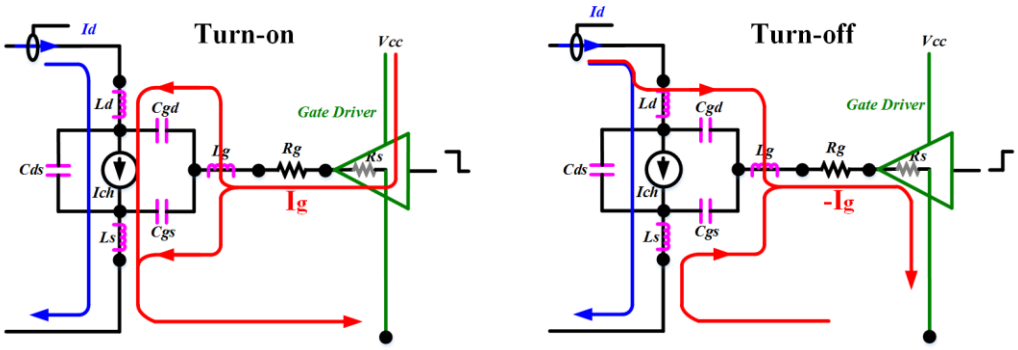


Fig. 2.6 Power and gate current during turn-on and turn-off processes.

As shown in Fig. 2.6, by applying the gate voltage V_{GS}, the input capacitance C_{iss} of the GaN HEMT becomes charged during the turn-on process, while it is discharged during the turn-off process. To determine the existing power consumption for separate gate drivers when switching a normally-off GaN HEMT, the total gate charge Q_g was considered specified at -3V/+5 V gate voltage. As given in [54]-[56], the power dissipated in the gate driver is comprised of three parts. The first is because of the total gate charge as defined in (2.2)

$$P_{gate} = Q_g \cdot V_{gate} \cdot f_{sw} \tag{2.2}$$

where Q_g is the total gate charge at specific gate voltage V_{gate} and f_{sw} is the switching frequency.

The other two parts consist of the *quiescent power loss* and *transient power loss*. The losses that correspond to the quiescent power ($P_{quiescent}$) and the transient power ($P_{transient}$) are slight in comparison with the loss related to the charging and discharging of the gate capacitance (P_{gate}) [57], and thus one can ignore these losses. The normally-off GaN HEMT is regarded as a capacitive load with 100 pF. One measures the total charge Q_g by integrating the gate current I_g. The power consumption for -3/+5 V gate voltage (considering normally-off GaN HEMTs) is measured at different switching frequencies, varying from 100 kHz to 2 MHz. Figure A 1.2 (Appendix A 1) shows the dissipated power for the selected MOSFET drivers at 100 pF capacitive load.

Other gate drive topologies can be seen as a second option for driving of GaN HEMTs. One of them is the resonant concept. Fig. 2.7 shows the schematic of the implemented resonant gate driver which is based on the resonant topology introduced in [52][53]. A resonant gate circuit allows recovering the driving energy and therefore offers the possibility to reduce power losses in the gate circuit [58][59]. Since the driver power is proportional to the switching frequency, this is an interesting option for very HF operation of GaN and SiC semiconductors. As described in Fig. 2.7, the main components of the resonant gate driver are the discrete pMOS and nMOS HF transistors in a "totem-pole" configuration. For the supplementary drive and the recovery path, two Schottky diodes D_1 and D_2) are chosen. In general, the resonant gate driver is very attractive for high frequency power applications up to 50 MHz, e.g., for HF low power dc/dc converters. Since for most high voltage applications > 600 V, the switching frequency is typically between 20 kHz and 500 kHz, for these applications it is more efficient to use the conventional gate driver.

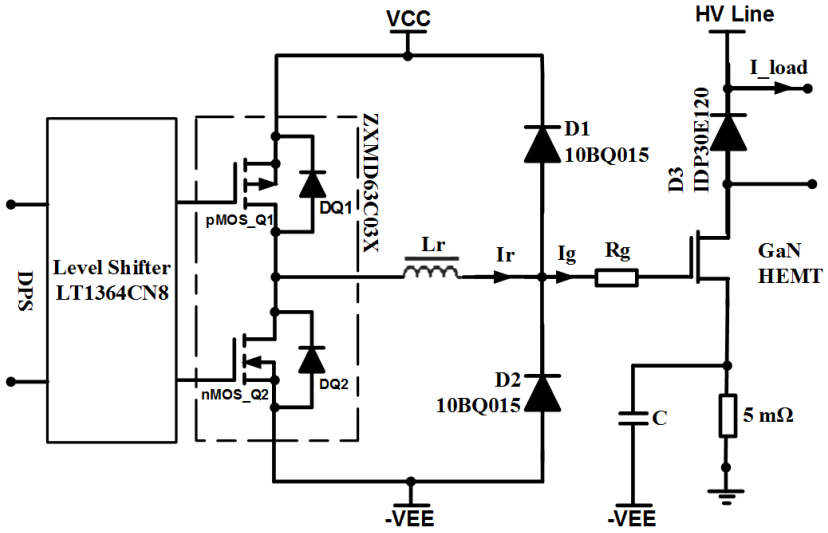


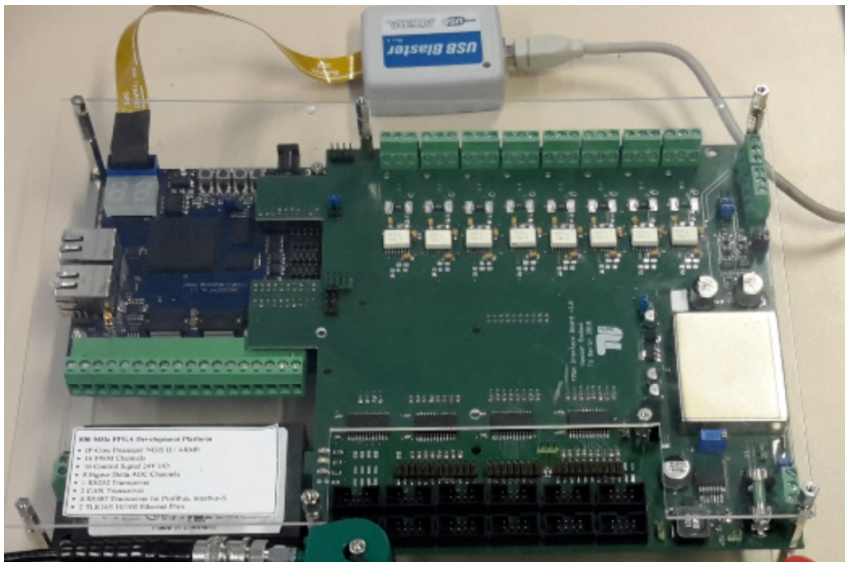
Fig. 2.7 First implementation of the resonant gate driver with energy recovery as proposed in [52][53].

2.3 FPGA-based Control System for Investigation Purposes

Several driving functions and tasks were necessary to conduct investigations of the GaN power devices. Investigating the dynamic on-state resistance of GaN HEMT at a specific and an exact number of transients is one of the tasks discussed in chapter 4. . For such test requirements different VHDL-blocks have been created as the PWM generator which is used to drive a full-bridge configuration, in which a precise setting of the dead-time between the drive signals in a few nanoseconds is necessary. For such utilities and purposes, promising solution is represented by FPGA-based technology. This subsection presents an FPGA-based control system for investigating different power devices. The implemented FPGA-based hardware is given in Fig. 2.8a. The main purpose of the design is to identify the best approach to exploit FPGA technology in power converter control specifically for power converters based on GaN and SiC power devices. Fig. 2.8b displays the completely developed FPGA-based system. The top-level design is implemented in a Quartus II schematic design file. The system

can be divided into three parts. The first is the Nios® II processor, which is responsible for establishing the connection to the Labview program and initializing the external memory. It is also responsible for writing the incoming data to the memory and sharing the data with the VHDL components. Values written to memory constitute the parameters for the modulation algorithms. Control signals for the interface controller are applied from the C program through input/output ports PIOs.

(a)



(b)

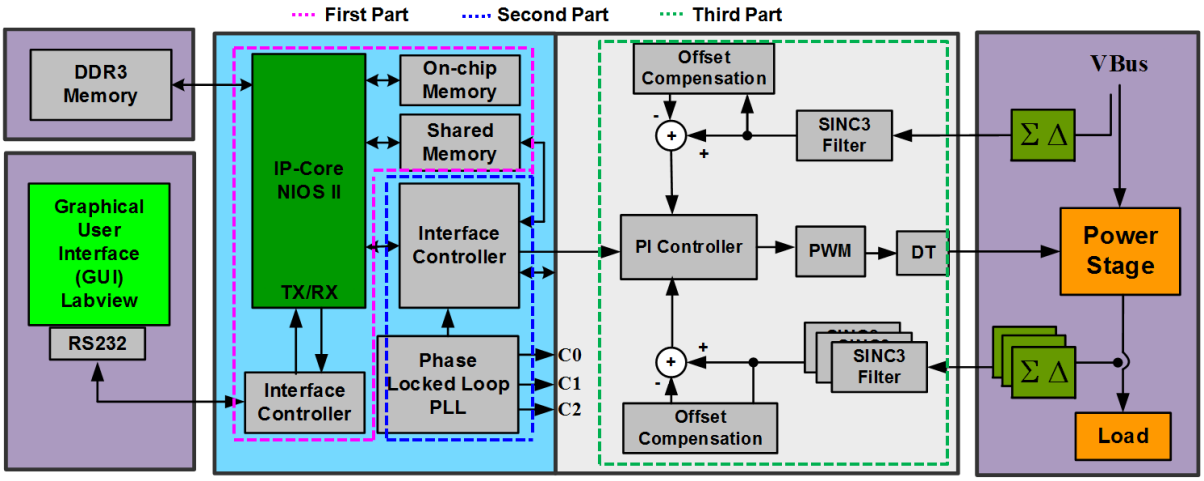


Fig. 2.8 (a) FPGA hardware design. (b) FPGA system overview.

3 Characterization of GaN HEMTs

High Voltage GaN-devices can operate at very high switching frequencies and therefore enable electric power converter systems operating in the MHz range. Such advantages push the development of new GaN-devices and their introduction into applications. This chapter discusses the static and switching characteristics of new 400 V and 600 V normally-on (depletion mode) and normally-off (enhancement mode) GaN HEMTs. These devices are developed recently at Ferdinand Braun Institute (FBH Berlin). This chapter also presents an introduction for the next chapter, where the degradation of the dynamic on-state resistance and the trapping effect phenomena are investigated.

3.1 Fundamentals of GaN Power Semiconductors

3.1.1 Overview of Gallium Nitride

Juza and Hahn first synthesized GaN in the 1930s by passing ammonia (NH_3) over liquid gallium (Ga) at high temperatures [26][28]. Maruska and Tietjen first attempted in 1968 the Hydride Vapor Phase Epitaxy (HVPE) approach to grow GaN layer on sapphire substrates [27][28]. The first idea of the Heterostructure Field-Effect Transistor (HFET) was announced by Takashi Mimura in 1979 at the Japanese Fujitsu Laboratories [32]. Bell Laboratories presented the first enhanced mobility effect validated in AlGaNAs/GaAs heterojunctions in 1979. The latter was applied to demonstrate an HFET in 1980 by Mimura and Delagebeaudeuf [32][33]. The enhanced electron mobility along the heterojunction of an Al_xGa_xN/GaN HEMT revealed an excellent potential for microwave electronics and was presented in 1994 by Khan [34]. GaN has attracted attention as highly promising material system for both optical and electronic applications since its emergence in the early 1990s [29].

3.1.2 Advantages and Disadvantages of Gallium Nitride

The first relevant question to be considered when selecting a new semiconductor material for use in power systems is what the advantages of this material are that make it more attractive than existing materials. In this section, the advantages and disadvantages of Gallium Niride (GaN) compared to the other existing materials (Silicon Si and Silicon Carbide SiC) are presented. Table 3.1 compares the key parameters of Silicon (Si), Silicon Carbide (SiC) and Gallium Nitride (GaN) [28][35][36][37].

Parameters	Si	GaAs	SiC	GaN
Bandgap Energy E_g [eV]	1.1	1.34	3.3	3.4
Saturation velocity v_{sat} [x10^7cm/s]	1.0	1.0	2.0	2.5
Electron mobility μ_n [cm^2/Vs]	1500	5800	1000	1200
Breakdown field intensity E_{BR} [MV/cm]	0.3	0.4	3.0	3.0
Thermal conductivity λ [W/cmK]	1.5	0.5	3.37 – 4.5	1.3 – 2.1
Dielectric constant ε_r	11.9	12.8	10	9.5

Table 3.1 Material properties of Si, SiC and GaN.

Bandgap Energy (E_g): The bandgap is the difference between the valence and conduction bands of the semiconductors. Large bandgap energy results in a high internal breakdown electric field, which allows for the application of high voltages. Applying a large voltage across the drain source terminals of the transistor always requires a high breakdown electrical field. The electric breakdown fields for WBG materials are typically one order of magnitude larger than those of conventional semiconductors [28].

Electron mobility μ_n: To physically reach high current and high frequency operation, high electron (carrier) mobility (μ) and high saturation velocity (v_{sat}) are needed, these parameters reveal how fast the electrons move in the transistor channel. Carrier mobility is the first parameter and is defined as the slope of the electron velocity versus the electric field (*v-E)* characteristics (at low e-field). Fig. 3.1a and Fig. 3.1b depict the linear and logarithmic representation of the electron velocity versus the E-field. As seen in Fig. 3.1a, by applying an electric field to the semiconductor, which is relatively low (less than 5kV/cm), one can see how well the electrons respond to the fast changing of the E-field. Concerning these physical characteristics, a figure of merit (FOM) is evaluated, that is called the "*carrier mobility"*. In Fig. 3.1a, the carrier mobility of the semiconductors appears to be similar. This is because the slopes of these curves are obviously quite similar. In contrast to the logarithmic representation, the different graph with the linear scale in Fig. 3.1b clearly demonstrates that gallium arsenide GaAs has much higher carrier mobility than gallium nitride GaN or silicon carbide SiC. It is obvious that the electrons respond extremely well to the rapid changes of the electric field when the strength of the electric field is relatively low. There is a high value for electron mobility of gallium arsenide GaAs (8500 cm^2/Vs). This is the chief reason why field-effect transistors (FETs) made from this material have such excellent high-frequency performance [28], and it is exactly what makes GaAs an excellent material for low noise amplifier.

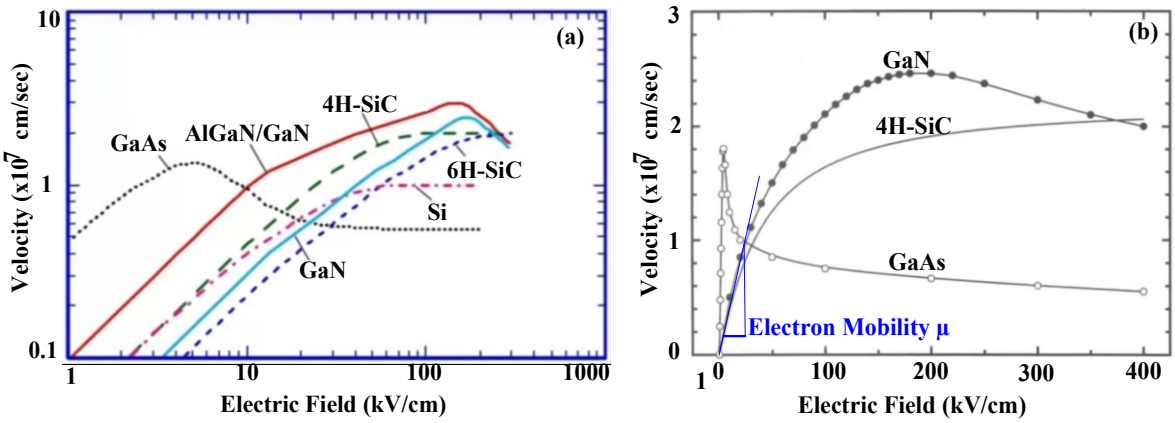


Fig. 3.1 Linear and logarithmic representation of the electron velocity versus the e-field[31][129].

Saturation Velocity v_{sat}: The current is defined as movement of charges and is expressed as the product between charge density and transport velocity [31]. To reach a high current, both charge density and transport velocity have to be high. The saturated velocity is the maximum velocity of the charge carrier (generally an electron) in a semiconductor attains in the presence of very high electric fields. Fig. 3.1a shows that the saturation velocity of silicon carbide SiC is clearly higher than silicon Si and gallium arsenide (GaAs), while the Gallium nitride (GaN) as depicted in the graph with the linear scale (Fig. 3.1b) is still better than in silicon carbide SiC.

Dielectric Constant ε_r: Another good quality of semiconductor material is the low dielectric constant. Semiconductor materials with a low dielectric constant possess lower capacitance loading. Capacitance remains proportional to dielectric constant, however, and to the overall area of the semiconductor. Because of a lower dielectric constant, the semiconductor device area can be increased, while the impedance constant is kept constant. As summarized in Table 3.1, the semiconductor materials that have a large bandgap difference between the top of the valence band and the bottom of the conduction band such as SiC and GaN have essentially a lower dielectric constant. This allows for having considerable advantages at high frequencies.

Thermal Conductivity λ: A semiconductor material possessing good thermal conductivity can efficiently and effectively extract heat from the device. Poor thermal conductivity results in degraded device operation when temperatures are elevated. Silicon carbide and diamond both exhibit excellent thermal conductivity. In comparison with silicon carbide, the thermal conductivity of gallium nitride is obviously lower; moreover, it is comparable to silicon. This is the reason why, in the last few years GaN transistors are manufactured on silicon carbide substrate, which is attributable to silicon carbide's excellent thermal properties. Nevertheless, most of the new GaN/AlGaN HEMTs are developed based on silicon substrate.

3.1.3 Original GaN HEMT and the Heterojunction Interface

GaN-based high electronic mobility transistors (HEMTs) are majority carrier devices based on n-type semiconductor material. The distinctive feature of GaN HEMT is found in the channel formation from the enhanced mobility of electrons accumulated in parallel along the so-called heterojunction between GaN and AlGaN layers. This is the so-called Two-Dimensional Electrons Gas (2DEG) [38]. Principally, the first configured heterojunction (heterostructure) has been achieved using the material combination of GaAs with Al-GaAs. For microwave applications, the using of GaAs was once the automatic choice of semiconductor material because of the good high-frequency performance. Fig. 3.2 depicts the structure of the original Al-GaAs/GaAs HFET and the corresponding energy band diagram, announced by Takashi Mimura in 1979 at the Japanese Fujitsu Laboratories, as discussed in [32]. In contrast, GaN have recently attracted more attention due to their high-power performance. Specifically for high voltage applications, most of the developed HEMTs at present are based on GaN/AlGaN heterojunction interface. This type of structure (a *heterostructure*) boasts several advantages. A heterostructure consists of at least two or more layers of different semiconductor materials, while the *heterojunction* (or a *heterointerface*) is the interface between these layers.

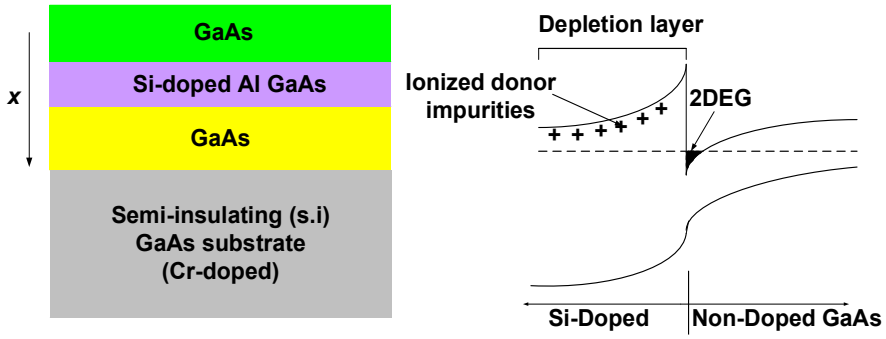


Fig. 3.2 Schematic cross-sectional of the original Al-GaAs/GaAs HFET and the corresponding energy band [32].

This kind of structure enables so-called "*modulation doping*". Modulation doping provides a substantial advantage in device engineering by offering a mechanism allowing the free carrier concentration within the semiconductor layer to increase significantly without introducing any doping impurities. The conventional doping technique is able to substantially increase free carrier concentrations. However, it results in an increase of ionized impurity scattering and hence a reduction in carrier mobility. Modulation doping, in contrast, enables free carriers to be increased substantially while not compromising mobility. A heterojunction is required for modulation doping. To achieve this, a wide bandgap semiconductor material wafer such as Aluminium Gallium Nitride (AlGaN) is grown on top of another material wafer with a lower bandgap like Gallium Nitride (GaN). While the conduction band is energetically higher in the AlGaN side than it is on the GaN side, the electrons start to occupy the lowest allowed energy state. They begin to move from the AlGaN side to the GaN side. This mechanism causes electron concentration to increase in the GaN material without reducing any of the donor's impurities. This results in reduced impurity scattering of the transfer electrons, while higher electrons mobility is achieved [31].

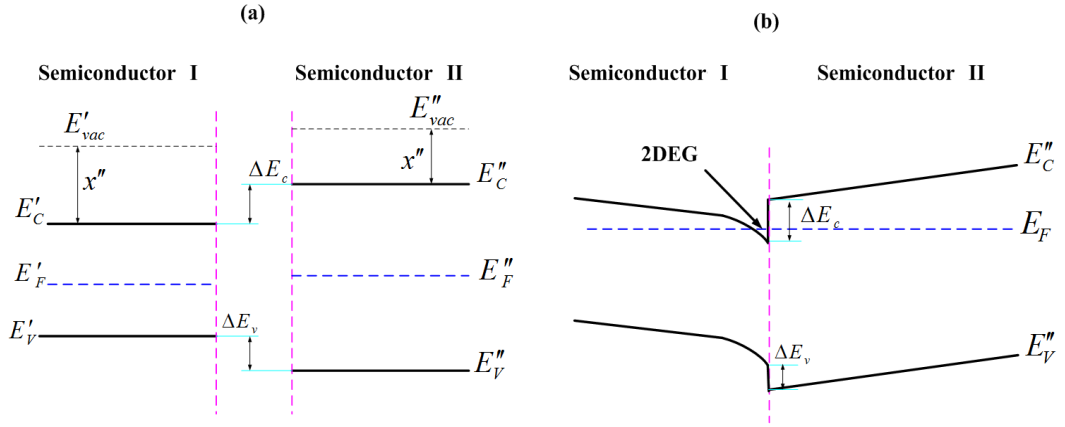


Fig. 3.3 Band diagram of the heterostructure formed between wide gap semiconductor II and narrow band gap semiconductor I. (a) Before the equilibrium, while the Fermi levels of the two semiconductors I and II are not coinciding (b) After the equilibrium where the lattice of the semiconductor II is comprised and strained [29].

In early generation AlGaAs/GaAs-based HEMTs, the origin of the carriers (electrons) is located in a junction between a heavily doped high bandgap and a lightly doped low bandgap region. In AlGaN/GaN-HEMT-based structures, this carrier accumulation is chiefly attributable to polarization charges along the heterojunction in the high bandgap AlGaN side [29]. Fig. 3.3b demonstrates the hetrostructure of two different semiconductors after bending of the bands, where the formation of a discontinuity occurs in the conductance (EC) and valence (EV) band at the heterojunction, and one common Fermi level is established.

3.2 Device and Technology

Many developments of GaN power HEMT based-on SiC and Si substrate have been made in recent years at Ferdinand Braun Institute (FBH Berlin) [61]-[64]. The GaN devices presented are designed and implemented as normally-on and normally-off types based on different gate technologies. Basically, GaN HEMTs are normally-on devices; they can be switched off by applying a negative gate source

voltage V_{GS}. Currently, more attention is paid to normally-off GaN transistors because of their inherent safety [2]. Several attempts have been carried out in recent years to convert normally-on into normally-off using gate recess, fluorine incorporation and p-GaN gate technology. The p-type gate already blocks the transistor channel at 0 V gate bias; the gate threshold voltage is shifted from negative to positive, which results in a normally-off device. The breakdown strength properties of GaN material are not always a guarantee for high voltage devices, while the geometrical layout design, device manufacturing process and parameters optimization are important issues for breakdown voltage enhancement [100]. Fig. 3.4 and Fig. 3.5 below present the epitaxial structure of normally-on and normally-off GaN HEMTs [31]. Fig. 3.6 depicts the investigated GaN device mounted in A0191 microwave packages. The normally-off GaN power transistor is obtained by using p-type GaN gate [2].

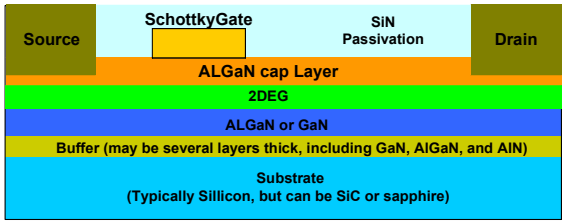


Fig. 3.4 Structure of the normally-on GaN HEMT

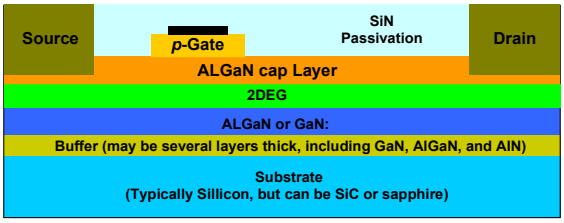


Fig. 3.5 Structure of the normally-off GaN HEMT

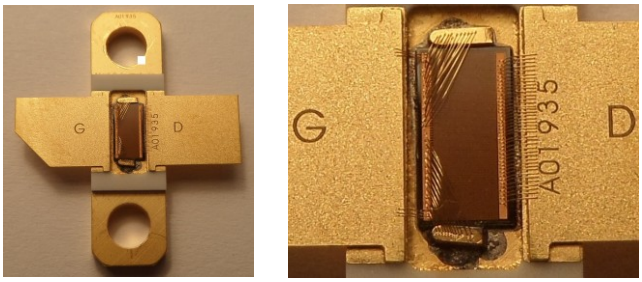


Fig. 3.6 GaN device mounted in A0191 microwave packages

In 2010, the first normally-off GaN transistor made at FBH Berlin for power applications using p-type GaN gate technology with a modified epitaxial concept was presented. This device was processed on 3" SiC wafers and the p-GaN gate was metallized with a Ni/Au ohmic contact, while the p-GaN Epi layer was selectively plasma-etched [61]. When the threshold voltage goes over 1 V; the on-state resistance can be kept low at high breakdown voltage strength. As shown in Fig. 3.7, the top performance occurs with $R_{ON}.A = 3.52\ m\Omega.cm^2$ at voltage breakdown (V_{BR}) of 870 V. The normally-off GaN devices from FBH with different gate drain distances L_{GD} = 6, 8, 10, 12, 15 and 18µm are benchmarked in [61] concerning the on-state resistance R_{ON} versus the breakdown voltage (V_{BR}) against other reported normally-off GaN. The design choice between the high breakdown voltage (V_{BR}) and low on-state resistance R_{ON} is a trade-off and depends on different geometric parameters. Thus, the achievement of a high breakdown voltage for low gate-drain spacing with optimum "R_{ON} x V_{BR}" ratio establishes the investigated devices as among the best normally-off GaN devices. Nevertheless, several degradations could be observed during dynamic testing of this device. The increase of the dynamic on-state resistance R_{DSON} at high power transients (high off-state voltage and high drain current) at high frequency represents one of the most problematic degradations observed.

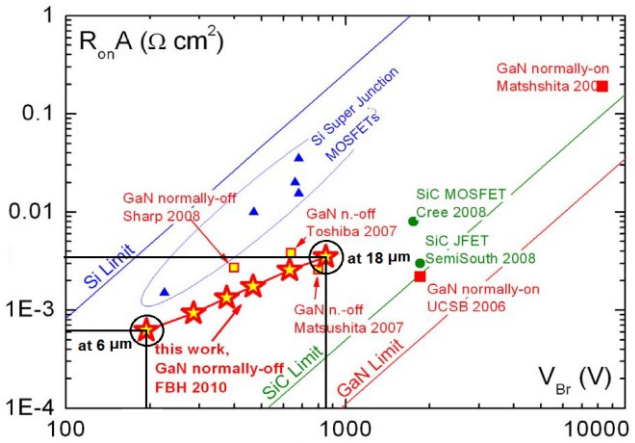


Fig. 3.7 Specific on-state resistance R_{ON} vs. V_{BR} blocking voltage for normally-off GaN devices with gate lengths of 6 to 18 µm benchmarked with Si- and SiC-based devices from other manufactures [61]

The experimental results with this device are presented in section 4.2. Furthermore, the results in Fig. 3.7 show that the proposed normally-off GaN HEMT with pGaN and $Al_{0.05}Ga_{0.95}N$ buffer [61] is comparable to GaN devices developed by other manufactures (Sharp, Toshiba and Matsushita). Following that, new versions of the GaN HEMTs for both normally-off with p-GaN gate and normally-on with Schottky-type metal gate types rated at 400V/12A were sequentially developed at FBH with different GaN buffer compositions. This has a direct impact on the dynamic on-state resistance. Some of these devices employ a carbon-doped GaN buffer rather than the $Al_{0.05}Ga_{0.95}N$ buffer. As stated in [62], the selected buffer concepts are targeted to improve the high-voltage capability of the devices, while the dynamic on-state resistance (R_{DSON}) is kept as low as possible. Fig. 3.8 shows a comparison of the normalized on-state resistance as function of off-state bias for p-GaN and Schottky gate devices using different buffer technologies. By comparing the investigated GaN devices with different buffer types, one observes a considerable increase of the dynamic on-state resistance (R_{DSON}) for the normally-off device with $Al_{0.05}Ga_{0.95}N$ buffer. Furthermore, the results at 65V off-state $V_{DS\text{-}Bias}$ reveal that the dynamic on-state resistance (R_{DSON}) of the p-GaN device with GaN:C buffer are obviously less than with Schottky-gate technology.

Table 3.2 Parameters of the FBH's first generation normally-off GaN HEMT using pGaN technology

Parameter	870V GaN HEMT [61]
Buffer	2 µm $Al_{0.05}Ga_{0.95}N$
GaN channel	35 nm
AlGaN barrier	15 µm $Al_{0.23}Ga_{0.77}N$
Gate technology	110 nm Mg-doped p-GaN
Effective doping	3e17 cm^{-3}
Gate width	3.8 mm
Gate drain distance	6 µm
Gate source distance	1 µm
Gate length	6 to 18 µm
Substrate	SiC

Typical device degradation in GaN HEMT is the gate reverse-bias tunneling leakage, which is driven by the magnitude and the volumetric distribution of the electric field peak under the drain side of the gate [66]. A common method uses field plates (FPs) to provide equal distribution of the electric field in the GaN channel [46][67]-[70]. The result is that the electric field under the gate-drain and source-gate is reduced and the device performance is improved with regard to the dynamic R_{DSON}. In general,

the use of such field plates seeks to reduce trapping effects in the buffer layer. This is proposed to be the main reason for the dynamic R_{DSON} increase. This trapping phenomenon will be discussed later in chapter 4.

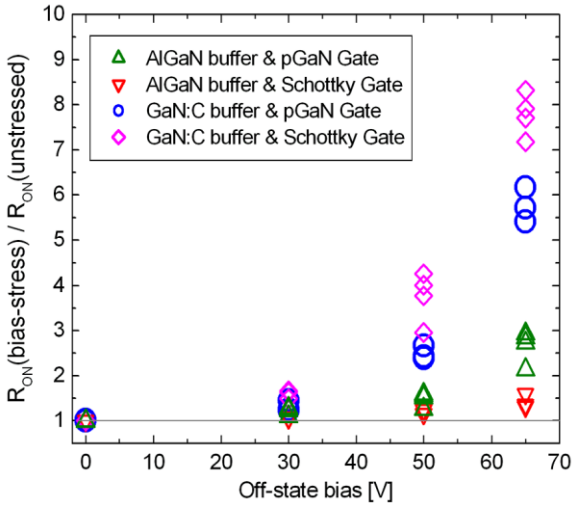


Fig. 3.8 Increase in the normalized dynamic on-state resistance as function of off-state bias. Normally-off and normally-on technologies with doped GaN:C and $Al_{0.05}Ga_{0.95}N$ buffers are compared [62].

The 400V normally-off and normally-on devices with carbon-doped GaN that are investigated use a type of gate-connected field plate. These field plates are constructed between 1.5 µm and 2.5 µm from the drain-side gate edge and placed on top of the 150 nm thick SiN_x passivation [62]. Another type of field plate is the source-connected field plate, which is considered to be more effective and to offer further reduction in dynamic R_{DSON} [62]. The field plate structures, *"gate-connected"* and *"source-connected"* have been used in the proposed GaN HEMTs. In the dynamic tests conducted in this thesis, it is observed that both 400 V devices are still characterized by a high dynamic on-state resistance R_{DSON} at high off-state voltage despite the use of field plates and different buffer technologies. More information and an in-depth discussion about the physics of the device can be found in [61][62].

Parameter	400V Schottky-gate device	400V pGaN-gate device
R_{ON}	85 m Ω	85 m Ω
Buffer	2-3 µm GaN:C	2-3 µm GaN:C
GaN channel	40-100 nm	40-100 nm
AlGaN barrier	25 nm $Al_{0.25}Ga_{0.75}N$	15 nm $Al_{0.23}Ga_{0.77}N$
Gate technology	Schottky-gate	110 nm Mg-doped p-GaN
Gate width	22 mm	22 mm
Gate drain distance	1 to 18 µm	1 to 18 µm
Gate source distance	1 µm	1 µm
Substrate	n-SiC	n-SiC

Table 3.3 Parameters of the investigated 400V normally-on and normally-off GaN HEMT

The final version of GaN transistors tested in this thesis consists of the 600 V normally-off and normally-on GaN HEMTs. Table 3.4 summarizes the parameters and features of the investigated 600 V GaN HEMTs in both Schottky-gate and pGaN-gate types. Both of the GaN devices contain the planar Multiple-Grating-Field-Plates (MGFPs). These significantly influence the electric field distribution in the transistor [63][65][104]. Differences between the two devices are linked either to the different gate type or to the different GaN buffer composition.

Parameter	600V Schottky-gate device	600V pGaN-gate device
R_{ON}	150 m Ω	70 m Ω
Buffer type	GaN:C AlGaN	GaN:Fe
GaN channel	40-100 nm	40-100 nm
AlGaN barrier	25 nm $Al_{0.25}Ga_{0.75}N$	15 nm $Al_{0.23}Ga_{0.77}N$
Gate technology	Schottky-gate	110 nm Mg-doped p-GaN
Gate width	134 mm	214 mm
Gate drain distance	15 µm	15 µm
Gate source distance	1 µm	1 µm
Gate lenght	0.7 µm	1.3 µm
Substrate	n-SiC	Si
Total chip area	2.8 x 2.3 mm^2	4.4 x 2.3 mm^2

Table 3.4 Parameters of the investigated 600V normally-on and normally-off GaN HEMT

Experimentally, the results of the static and dynamic tests of the 400 V devices are discussed briefly in the sections 3.3.1 and 3.4.1, while the focus of this work is placed on the 600 V power devices as given in chapters 4, 6 and 7. In conducting the initial tests, the GaN devices were mounted in A0191 microwave packages, as shown in Fig. 3.6, while the comparable state-of-the-art super-junction MOSFETs employed in further tests use the standard TO220 packages.

DUT Type	V_{rated} (V)	I_{max} (A)	V_{th} (V)	R_{on} (mΩ)	Q_g (nC)
Normally-on GaN HEMT [61] [62]	400	12	-4.2	85	not measured
Normally-off GaN HEMT [61] [62]	400	12	1.0	85	not measured
Normally-on GaN HEMT [62]	600	12	-3.7	150	9.2
Normally-off GaN HEMT [63]	600	16	1.1	70	15

Table 3.5 GaN power HEMTs developed at FBH Berlin.

3.3 Static Characteristics

Static characteristics are the most basic evaluations of the power device. In this section, the DC characteristics for the investigated 400V and 600V GaN HEMTs are presented. It consists of the forward and transfer characteristics. The static on-resistance R_{ON} is also measured at different base plate temperatures varying from 25 °C to 150 °C. The static test circuit used for DC characterization is shown in [3.9]. As described in the circuit, the gate signal at the low-side is always high and the GaN device is constantly turned-on. At the high-side, a single-pulse of 1 µs is applied and the load current flows through the MOSFET. Subsequently, the drain current I_D and drain-source voltage V_{DS} of the GaN HEMT will be measured at different gate voltages V_{GS}. The static on-state resistance R_{ON} can be read directly from the output characteristic curves under varying temperature from 25 °C to 150 °C. R_{ON} was measured under V_{GS} = 5V and V_{GS} = 1V and the output characteristic for gate voltage ranges V_{GS} -2 to 5V and -5 to 1V for the normally-off and normally-on devices respectively. The measured transfer characteristic, instead, was evaluated under 10V drain source V_{DS} while varying the gate source voltage V_{GS}.

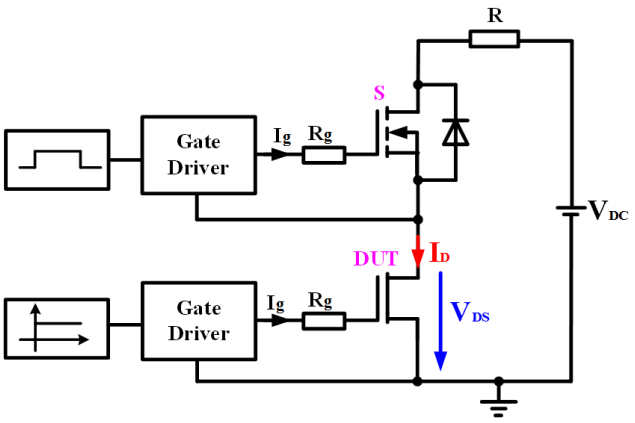


Fig. 3.9 Static test circuit used for the characterization of the GaN HEMTs (DUT).

3.3.1 Static Characteristics of the 400 V GaN HEMTs

In Fig. 3.10a and Fig. 3.11a, the forward characteristics measurements of the investigated 400V normall-on and normally-off devices are demonstrated and compared. Furthermore, the thermal impacts on the static R_{ON} resistance have been considered. From the results in Fig. 3.10a and Fig. 3.11a it can be seen that the investigated GaN devices provide saturated drain currents of 33 A and 29 A at gate bias of 1 V and 5 V for normally-on and normally-off, respectively. For power applications, threshold voltage ranges above +1 V are desirable to ensure safe operation. The threshold voltage V_{TH} of the different devices can be read from the transfer characteristics in Fig. 3.10b and Fig. 3.11b. The measured V_{TH} value (0.9V … 1V) shows that the pGaN gate needs to be improved in order to provide an acceptable operation safety margin. Based on the measured forward characteristics, R_{ON} resistances of both devices are calculated. Fig. 3.12a and Fig. 3.12b show the measured R_{ON} resistance vs. drain current I_D for normally-on and normally-off GaN HEMTs, respectively. Both devices characterize quite similar R_{ON} resistance at maximum gate bias (+1 V and +5 V) in the linear region. This mainly refers to the similarity in physical and geometrical (chip area) properties of the devices. However, normally-on device characterize a higher saturated current than the normally-off. This is possibly due to the use of different gate technologies which affect the electron concentration in the GaN channel. Essentially, the threshold voltage of p-GaN gate transistors is adjusted by the p-GaN doping concentration and by the AlGaN barrier thickness. On the other hand, there is a trade-off for the 2DEG-channel electron concentration, since both V_{TH} and the on-state resistance vary with the electron concentration [69]. Fig. 3.13a shows the increase of the static R_{ON} for both normally-off and normally-on devices as a function of temperature. The normalized temperature-dependent $R_{ON\text{-}Norm}$ ($R_{ON\text{-}T°}/R_{ON\text{-}25°}$) of both GaN transistors is in the same range, which is summarized in Fig. 3.13b. As seen, the temperature has a significant impact on the static R_{ON}. The increase of the static R_{ON} resistance with higher temperature can be attributed to the reduction of the electron mobility and electron saturation velocity in the channel [129].

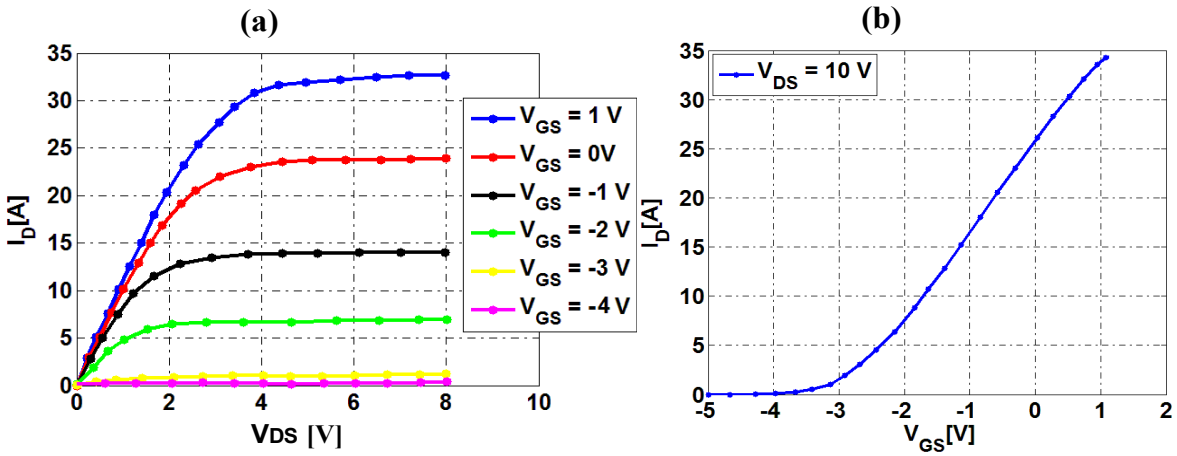


Fig. 3.10 Measured I-V forward and transfer characteristics for normally-on GaN transistor with R_{ON} = 85 mΩ.

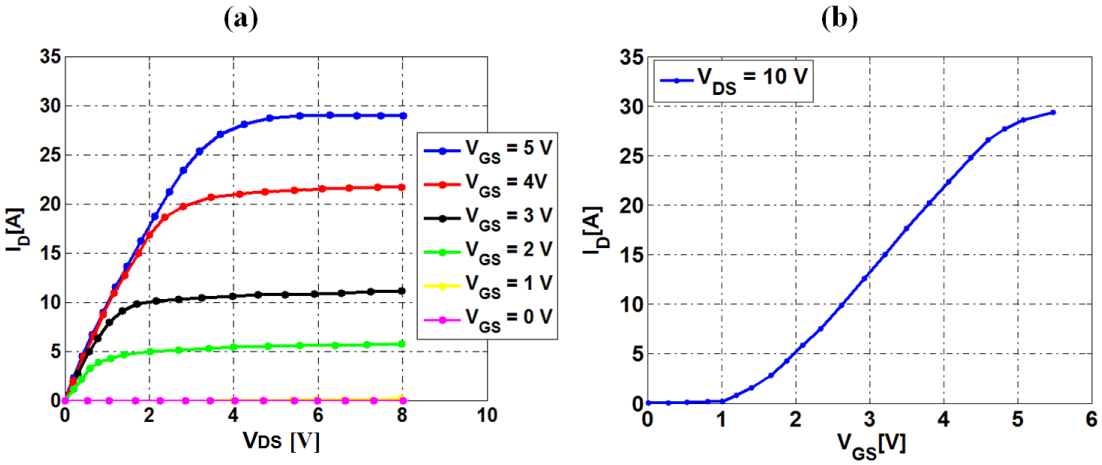


Fig. 3.11 Measured I-V forward and transfer characteristics for normally-off GaN transistor with R_{ON} = 85 mΩ.

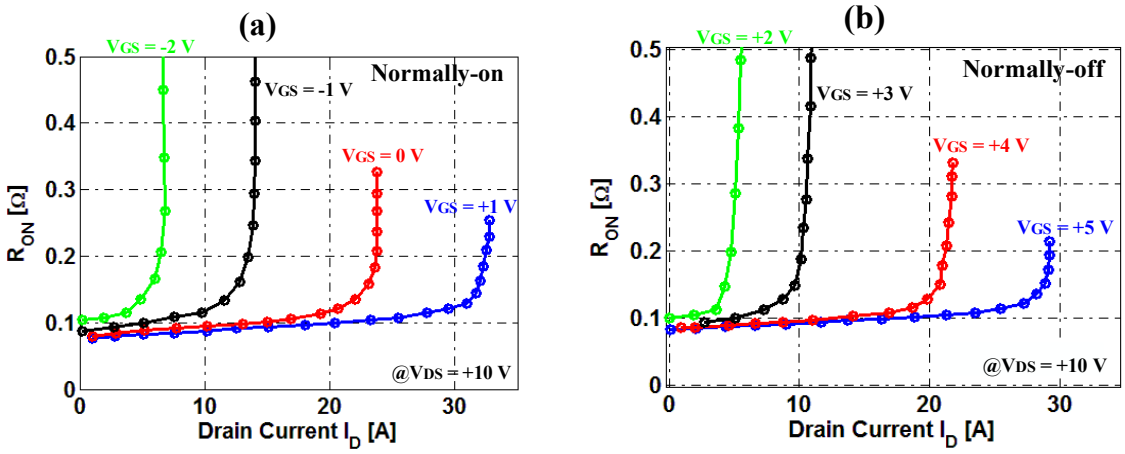


Fig. 3.12 Measured R_{ON} resistance vs. drain current I_D for normally-on and normally-off GaN HEMTs.

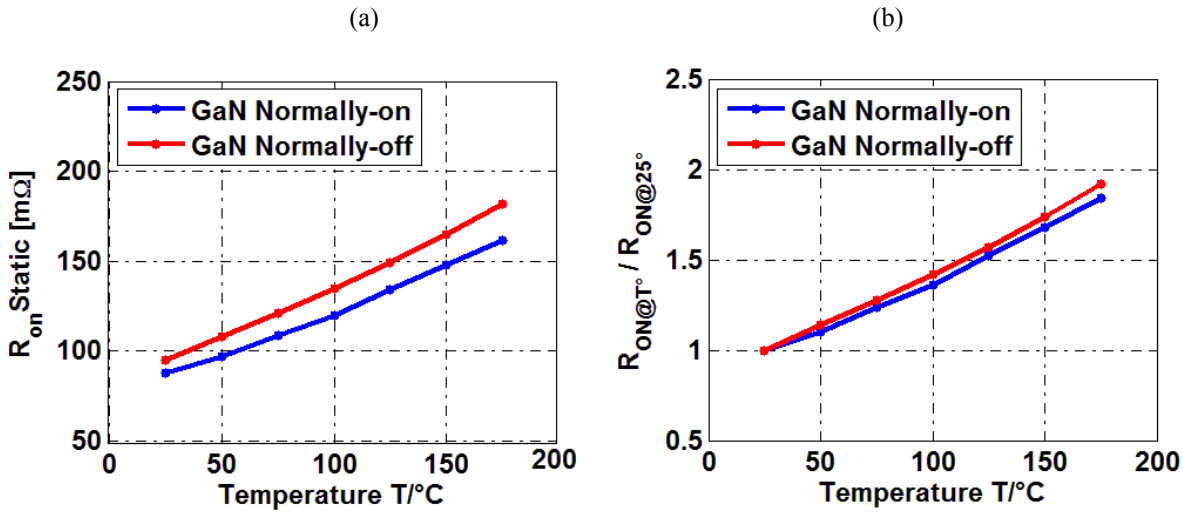


Fig. 3.13 (a) Measured R_{ON} at different tempertures. (b) Normalized R_{ON} (T°), V_{GS} = 5V.

3.3.2 Static Characteristics of the 600 V GaN HEMTs

In contrast to the investigated 400V GaN power devices, the 600V normally-on and normally-off HEMTs are considerably improved. The characterization of a reliable power device is essentially important to provide a reasonable comparison to its silicon counterparts. For benchmarking, the static and dynamic tests are conducted with the state-of-the-art 600V super-junction MOSFET 'IPP25R125C7' from Infineon [47], which has the standard TO-220 package. The forward characteristics measurements in Fig. 3.14a, Fig. 3.15a and Fig. 3.16a demonstrate the maximum drain currents of 30A, 90A and 70A at gate bias of +1V, +5V and +15V for normally-on and normally-off GaN HEMTs and the Si MOSFET respectively. The threshold voltage V_{TH} of the different devices can be read from the transfer characteristics shown in Fig. 3.14b, Fig. 3.15b and Fig. 3.16b. From the results, the V_{TH} values of GaN devices are identical with the 400V devices. This is mainly due to the use of the same gate technologies for both devices as described in Table 3.3.

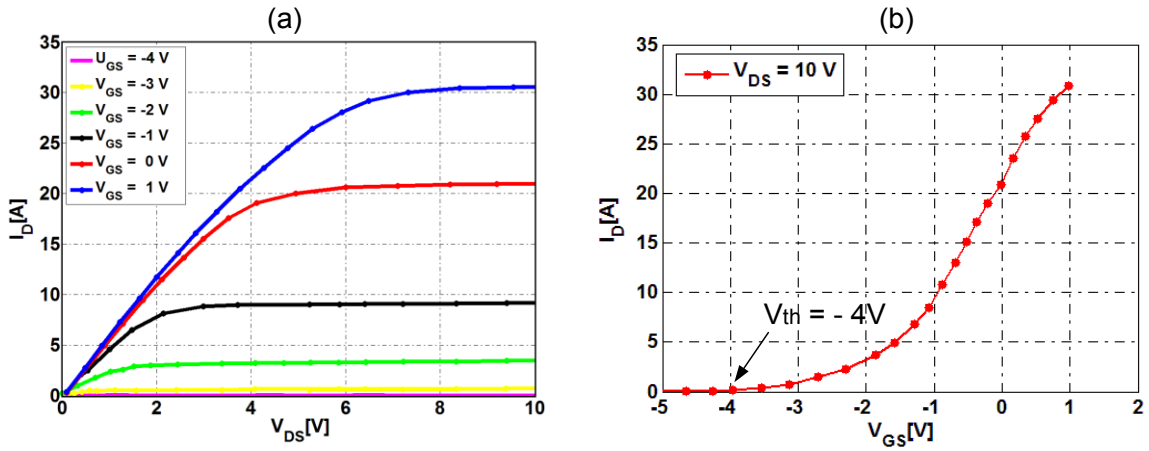


Fig. 3.14 Measured I-V forward and transfer characteristics for normally-on GaN HEMT. Pulse time = 1 µs.

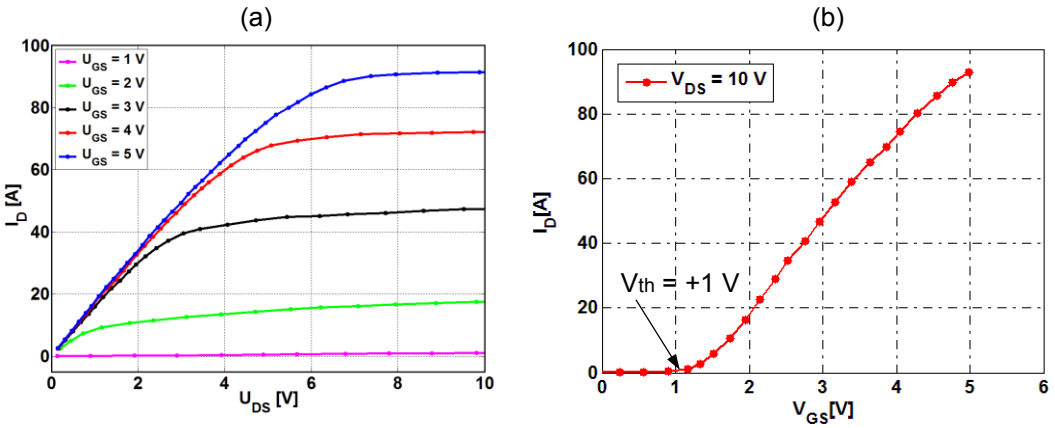


Fig. 3.15 Measured I-V forward and transfer characteristics for normally-off GaN HEMT. Pulse time =1 µs.

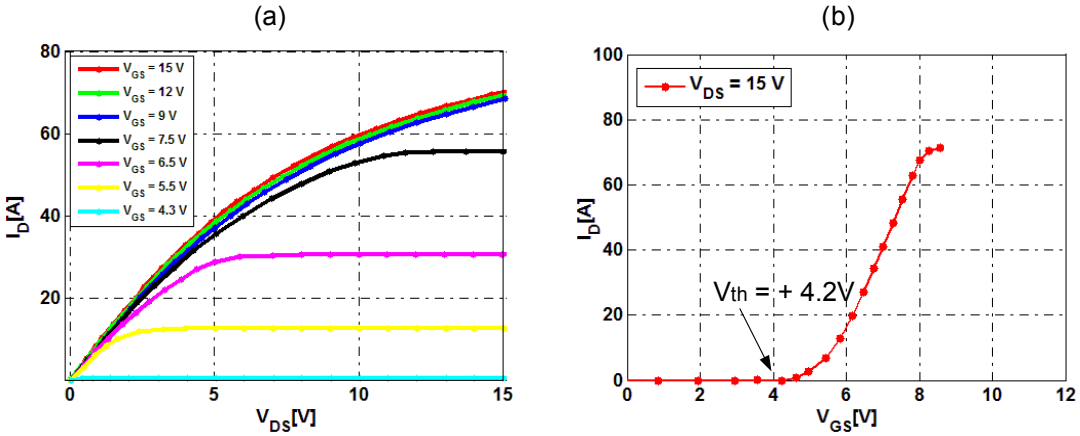


Fig. 3.16 Measured I-V forward and transfer characteristics for SJ- MOSFET. Pulse time = 1 µs.

Based on the measured forward charachteristic of the three devices the R_{ON} resistance is calculated. Fig. 3.17a, Fig. 3.17b and Fig. 3.17c show the R_{ON} rasistance versus the dain current I_D. Analogous to the forward characteristics of the 400V devices, the drain currents of GaN devices reach the maximum values in the saturation region at the maximum gate bias (+1V and +5V). However, it seems different for the investigated SJ-MOSFET. By comparing the measured R_{ON} characteristics in Fig. 3.17c with the results in Fig. 3.17a and Fig. 3.17b, the SJ-MOSFET characterizes unsaturated current of more than 70A at the maximum gate bias of 12V (as shown also in Fig. 3.16a).

In general, to compare the impact of different parameters on the R_{ON} of different power devices, it is important to use power devices that have equal chip area. Unfortunately, the available GaN devices used in this work do not have the same chip area. For the 65 mΩ normally-off GaN-on-Si HEMT the chip area was arranged on 4.4 × 2.3 mm^2, while the only available normally-on GaN device was arranged on 2.8 × 2.3 mm^2. Although specific information about the chip area of the investigated super-junction MOSFET was not available, the static tests can provide some information which is required to distinguish between different effects in the device during the dynamic tests. One of these static tests is the forward characteristics at different temperatures which is needed to distinguish between the thermal and trapping effects in GaN devices. This will be discussed in the next chapter.

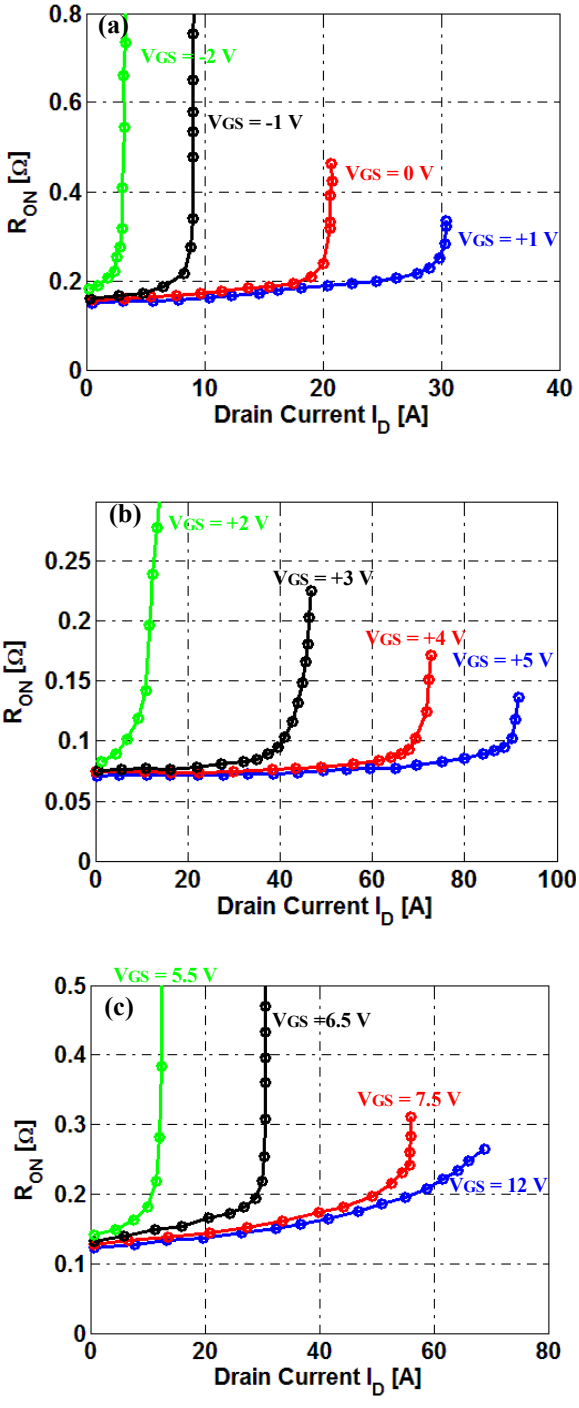


Fig. 3.17 Measured on-state resistance of the investigated transistors vs. drain current. Temperatures = 25°C
(a) Normally-on GaN HEMT.
(b) Normally-off GaN HEMT.
(c) Super-junction MOSFET.

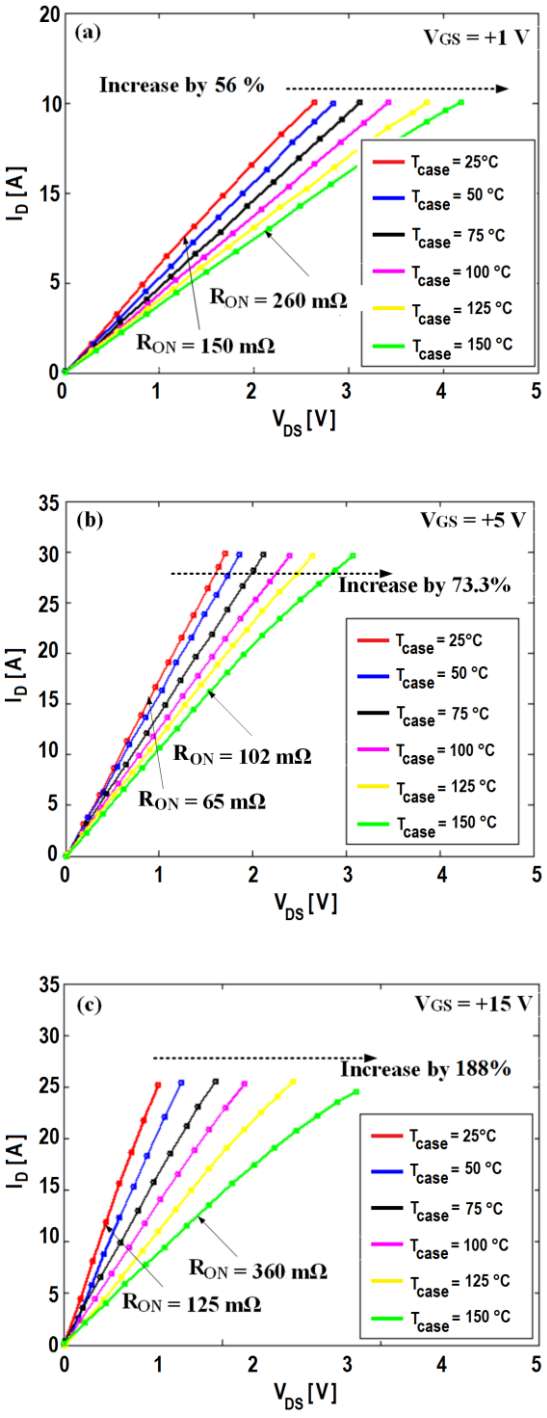


Fig. 3.18 Linear forward characteristics of the investigated transistors at different temperatures varying from 25°C to 150°C.
(a) Normally-on GaN HEMT, V_{GS} = +1V.
(b) Normally-off GaN HEMT, V_{GS} = +5V.
(c) Super-junction MOSFET, V_{GS} = +15V.

Essentially, the investigation of the dynamic R_{DSON} degradation in GaN HEMT represents one of the main goals of this work. Such degradation refers to the increase of the junction temperature (thermal effect) or to the so-called trapping effects. In order to differentiate between these effects, the linear forward characteristics of the investigated 600 V power transistors are obtained at different temperatures varying from 25° C to 150° C. These characteristics will be used as a reference for the measurements of the dynamic R_{DSON}. Fig. 3.18 summarizes the linear forward characteristics at different temperatures. The temperature-dependent R_{ON} for GaN devices is relatively low compared to the SJ-MOFET. R_{ON} increases from 25° C to 150° C by 56% and 73% for normally-on and normally-off transistors, respectively, while an increase of 188% is measured for the super-junction MOSFET. Lastly, the increase of the R_{ON} resistance of both normally-off and normally-on devices as a function of the temperature from 25°C to 150°C is demonstrated in Fig. 3.19a. Both GaN transistors characterize approximately the same normalized temperature-dependent $R_{ON\text{-}Norm}$ ($R_{ON\text{-}T°}/R_{ON\text{-}25°}$) up to 100°C, while the SJ-MOSFET as expected illustrates stronger temperature-dependence (Fig. 3.19b).

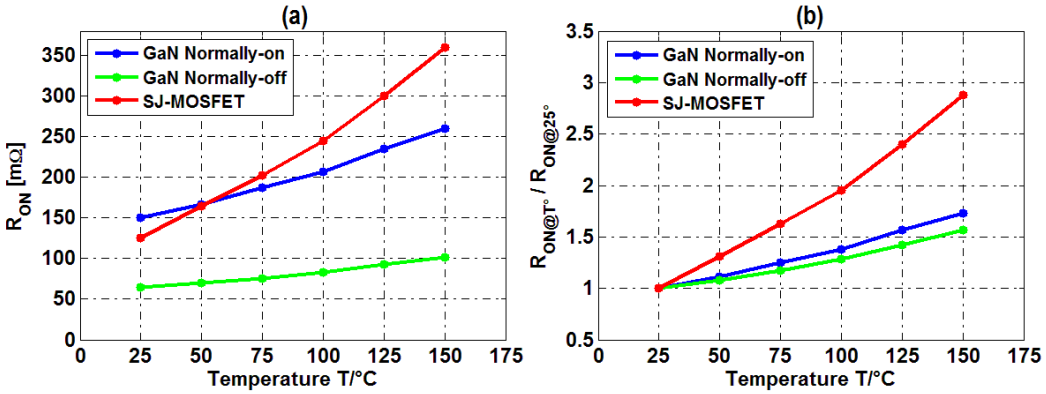


Fig. 3.19 (a) Measured Ron and (b) normalized R_{ON} (T°) at different temperatures.

3.4 Switching Characteristics

In this section, the switching performance of the investigated normally-off and normally-on GaN HEMTs is presented. Commonly, the switching characteristic is evaluated in double pulse tests using a buck converter. Test circuit and measurement requirements have been discussed in section 2.1.1. Since no matching GaN diode was available, the switching results were obtained applying a 650V SiC Schottky freewheeling diode from CREE [71]. Both transistors are switched with -3V/+5V and -5V/+2V gate voltages V_{GS}. Figure 3.20 depicts exemplary switching transients of the investigated 400V normally-off GaN HEMT. Fig. 3.20 shows different observations. The first part "obs1" is the V_{DS} overshoot during the turn-off. This is mainly due to the energy stored in the parasitic inductances in the power loop. As a result, this high voltage overshoot will constrain the DC input voltage and consequencelly limit the power density of the power system. Therefore, the commutation loop has to be designed as short as possible in order to improve the system performance. The second part "obs2" is the voltage notch of the V_{DS} during turn-on. At $V_{GS} = V_{TH}$, the GaN transistor gets ready to conduct the drain current I_D and starts to increase linearly. As the drain current increases during the transient from zero to I_L with *di/dt*, the voltage drop across the parasitc inductances and inductive load will reshape the drain-source voltage V_{DS} forming a voltage notch as seen at "obs2" where the $V_{DS-Notch} = U_L = L \cdot di/dt$.

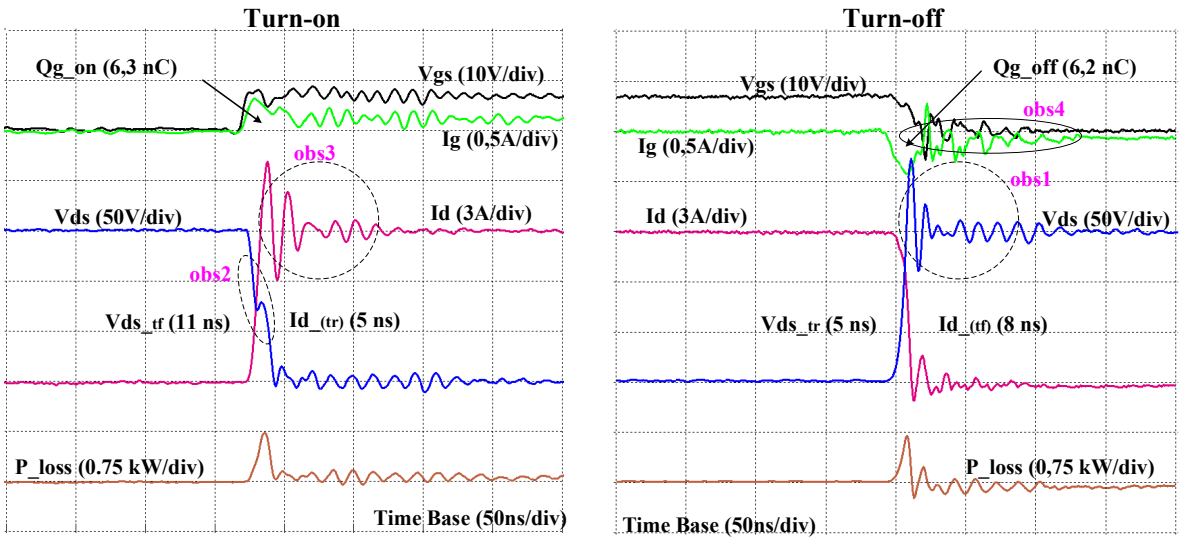


Fig. 3.20 Measured turn-on and turn-off waveforms of 400V normally-off GaN HEMT in double pulse test (V_{DS}=100V and I_D=12 A, R_G=10Ω). The test results are obtained applying a 600V SiC Schottky freewheeling diode from CREE (C2D10120A [71]).

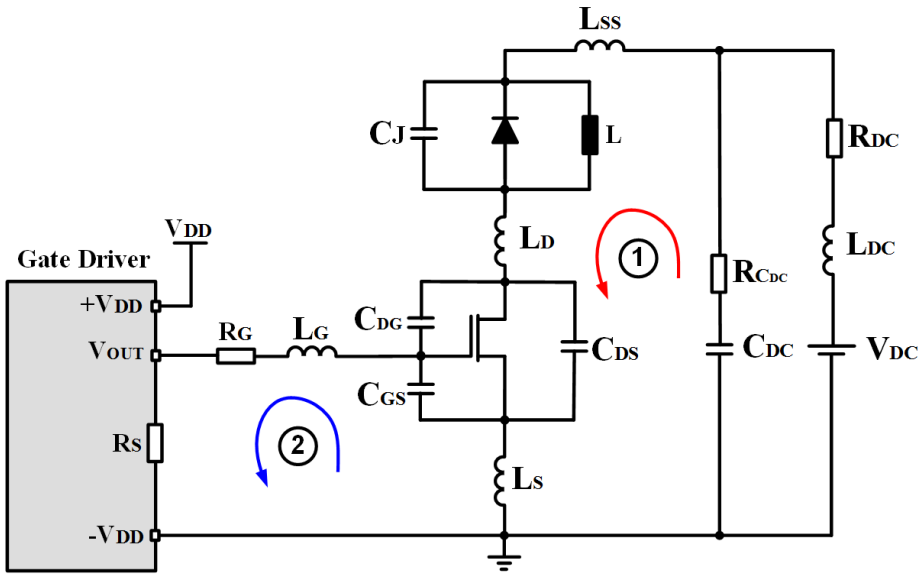


Fig. 3.21 Schematic test circuit including the parasitic elements in the power (1) and gate (2) current loops.

The third part “obs3” is the drain current peak and ringing. While the drain current ringing refers to the parasitic inductances in correlation with high *di/dt*, the current peak is essentially affected by the high *dv/dt*. The last observation “obs4” is the ringing of the gate current I_G and gate-source voltage V_{GS} during turn-on and turn-off. This ringing refers to the parasitic inductance L_g in series with the gate-source capacitance C_{GS} in the gate loop. Fig. 3.21 shows the dynamic circuit including all capacitive and inductive parasitics. Fig. 3.22 explains the switching transients during Turn-on and Turn-off. While a low on-state resistance R_{ON} is the key parameter to limit the conduction losses, the total gate charge Q_g is a major factor for the switching losses. The product of the gate charge and the on-state

resistance Q_g x R_{ON} is denoted as a Figure of merit (FOM) of the power switching device. This product is often used as FOM for switching efficiency. In order to achieve a high performance, the R_{ON} x Q_g of the power device has to be as small as possible. The gate charge Q_g is calculated by integrating the gate current I_G over time. Exemplary inductive switching transients during turn-on and turn-off of a power super-junction MOSFET is given in Fig. 3.22. Compared to the results in Fig. 3.20, the idealized curves show no oscillatory behavior, which leads to additional circuit losses. In general, there are two major reasons for the ringing during the transients. The first one is related to the parasitic inductance in the circuit loops and the other one is related to the high *dv/dt* rate [159].

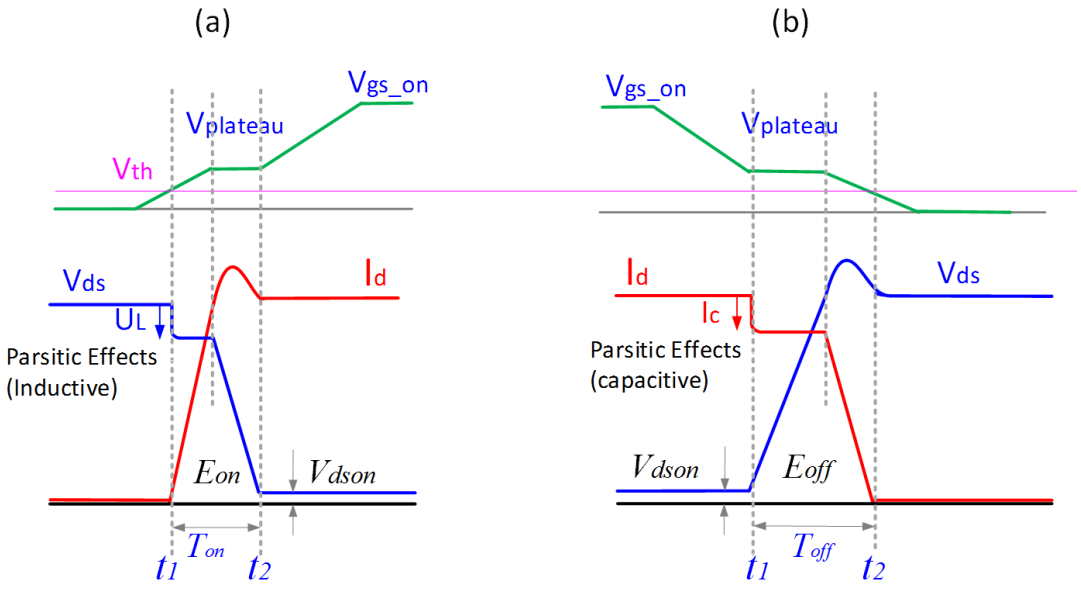


Fig. 3.22 Exemplary inductive switching transients during turn-on and turn-off.

3.4.1 Switching Test of 400V Normally-on and Normally-off GaN HEMTs

Normally-on and normally-off transistors are tested using a double pulse at different switching speeds. Fig. 3.23 shows a comparison between the measured waveforms of the 400 V normally-off GaN HEMT during turn-on and turn-off at different gate resistances R_G = 5, 15, 30 and 45Ω. The switching test is conducted at 25°C. In the figure, the switching power losses can be substantially reduced by increasing the switching speed (fast switching transients, i.e., high di/dt). The measured waveforms are obtained at V_{DS} = 100V and I_D = 12A load condition. Obviously, with increasing switching speed, a significant reduction of power losses is achievable at the cost of higher ringing, higher current overshot at turn-on and voltage overshot at turn-off. For comparison purposes, the measured V_{GS}, V_{DS} and I_D waveforms are aligned in time. The rise time t_r is the time required for I_D or V_{DS} to rise from 10% to 90% of its steady-state. Similarly, the fall time t_f is the time taken to fall from 90% to 10% of the steady-state value. Based on this difination, the turn-off time t_{OFF} is defined as a time between V_{DC} rising to 10% of the dc bus voltage to I_D falling to 10% of the load current. Whereas, the turn-on time t_{ON} is the time interval between I_D rising to 10% of the load current to V_{DC} falling to 10% of the dc bus voltage.

Depending on the t_{ON} and t_{OFF} definition the switching time calculations are made and summarized in Table 3.6 and Table 3.7. The turn-on switching energy Eon and turn-off energy E_{OFF} are integrals of the product of V_{DS} and I_D over t_{ON} and t_{OFF}, respectively. Fig. 3.25 shows the switching energies E_{ON} and E_{OFF} vs. the drain current I_D for different switching speeds. Both E_{ON} and E_{OFF} increases approximately linearly versus the I_D with gate resistance R_G = 5 and 15Ω, and nonlinearly with R_G = 30 and 45Ω. Moreover, the investigated normally-off GaN HEMT characterizes a higher increase of E_{ON} compared to E_{OFF}. This is mainly due to the shorter turn-off interval time t_{OFF}, compared to t_{ON}. From the results, different points can be concluded: 1) GaN HEMT has the capability to switch on and off very fast in a few nanoseconds. 2) As reported in [8], GaN HEMT behavs quite similar to Si-MOSFET. 3) Controlling the *dv/dt* can be achieved by increasing or decreasing the gate resistance R_G. 4) The commercial MOSFET gate driver used in the test shows suitability to drive GaN HEMT; this gives more evidence that GaN HEMT and Si-MOSFET have many things in common. As with the normally-off device, the switching performance of the 400 V normally-on GaN HEMTs is also investigated at different switching speeds, as shown in Fig. 3.24. The device reveals a very similar performance compared to the normally-off type.

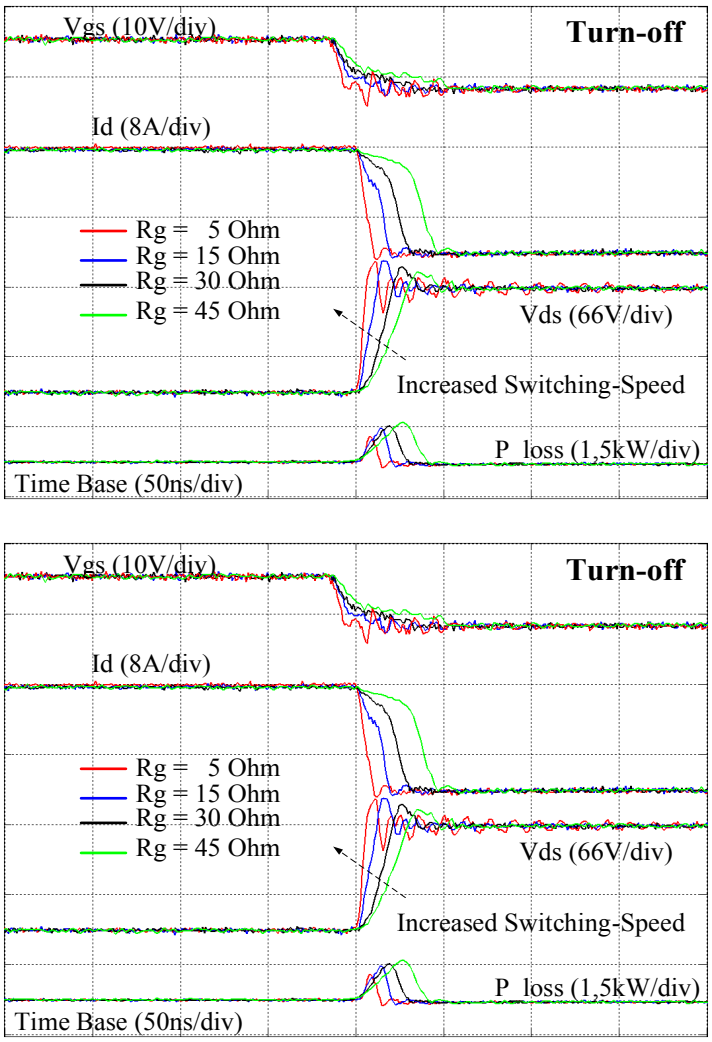


Fig. 3.23 Measured turn-off and turn-on waveforms of the 400V normally-off GaN HEMT at different switching speed. V_{DS}=100V and I_D =12 A. Gate resistance R_G = 5, 15, 30 and 45Ω.

	Turn-on			Turn-off		
	V_{DS}, t_f (ns)	I_D, t_r (ns)	t_{ON} (ns)	V_{DS}, t_r (ns)	I_D, t_f (ns)	t_{OFF} (ns)
R_G = 5 Ω	6.5	4	12	4	4	9
R_G = 15 Ω	7.5	6	15	6.5	4.5	12
R_G = 30 Ω	13	8.5	23	12	6	19
R_G = 45 Ω	22	11	35	19	10.5	31

Table 3.6 Switching times of the normally-off HEMT at V_{DS}=100V, I_D =12 A and R_G= 5, 15, 30 and 45Ω.

The measured switching times of the V_{DS} and I_D versus the gate resistances at 100V/12A are presented in summary in Table 3.7. Fig. 3.26 shows the switching energy E_{ON} and E_{OFF} of the investigated normally-on device. In contrast to normally-off device, the E_{ON} and E_{OFF} results of the normally-on device consistently show a nonlinear increase with increase of the I_D at different switching speeds. Only with R_G = 10Ω and 15Ω the E_{OFF} illustrates a linear increase at high switching speeds. The resulting quantities Q_g x R_{ON} of the HEMTs are compared in Table 3.8 to a commercially available Si-MOSFET and the EPC 200V/12A GaN transistor.

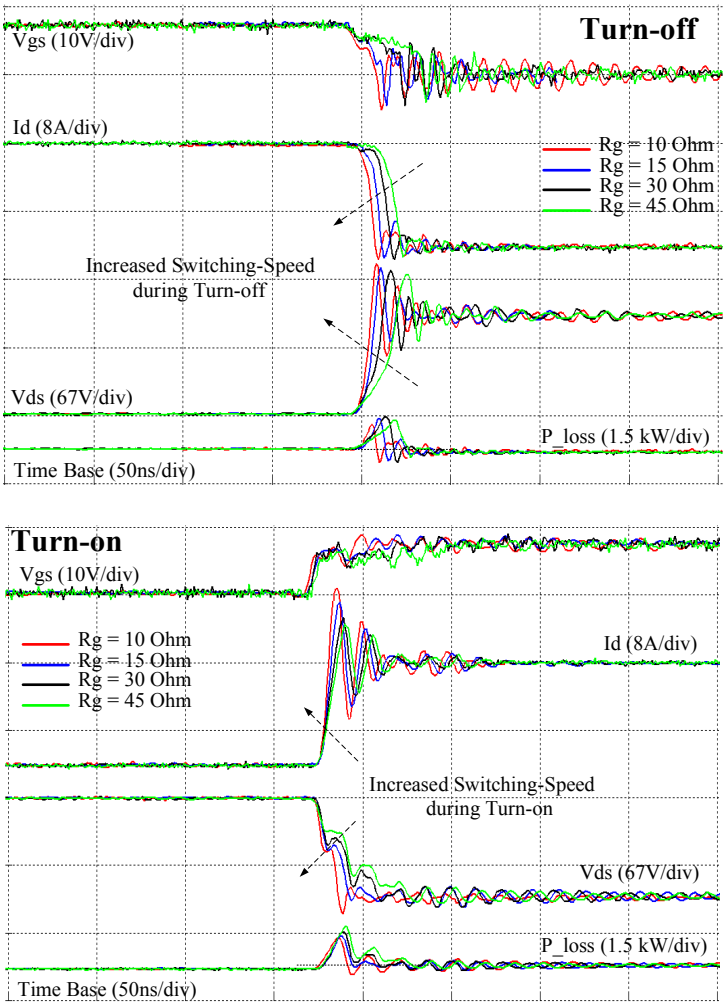


Fig. 3.24 Measured turn-off and turn-on waveforms of the 400V normally-on GaN HEMT at different switching speed (V_{DS}=100V and I_D =12 A. Gate resistance R_G = 5, 15, 30 and 45Ω).

The results show that the quantities Q_g x R_{ON} for the three GaN devices is significantly improved in comparison to the exemplary Si-MOSFET. Even though the gate charge is very much similar, the switching performance of the normally-on devices is better, which is indicated in the evaluation of switching energies in Fig. 3.26. Both of the proposed GaN transistors obviously demonstrate good switching speeds and low static on-state voltage. Nevertheless, the high dynamic on-state resistance in both transistors, to be discussed in the next chapter, remains a fundamental challenge.

	Turn-on			Turn-off		
Resistance	**V_{DS}, t_f (ns)**	**I_D, t_r (ns)**	**t_{ON} (ns)**	**V_{DS}, t_r (ns)**	**I_D, t_f (ns)**	**t_{OFF} (ns)**
R_G = 10 Ω	4	2	6.5	3	3	6.5
R_G = 15 Ω	5.5	3	9.5	4	5	10
R_G = 30 Ω	11	4	16	6	8	17
R_G = 45 Ω	15	6.5	25	7.5	12	21

Table 3.7 Switching times of the normally-on HEMT at V_{DS}=100V, I_D =12 A and R_G= 5, 15, 30 and 45Ω.

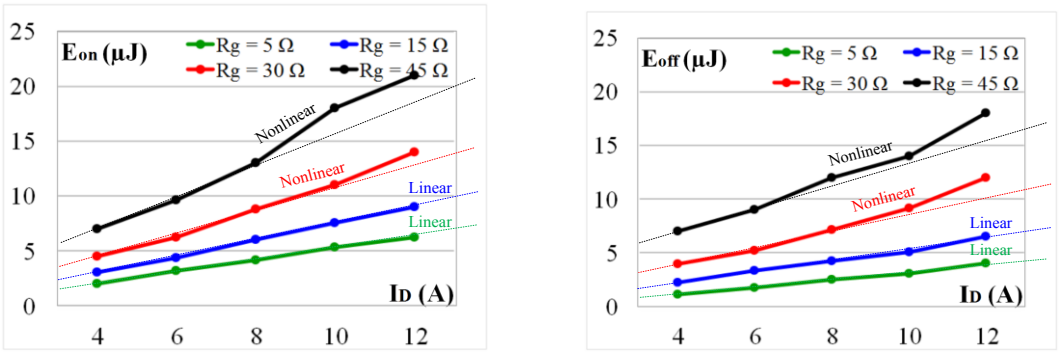


Fig. 3.25 Switching energies E_{ON} (a) and E_{OFF} (b) versus the drain current I_D for the normally-off GaN HEMT at different switching speed (V_{DS}=100V and I_D =12 A. Gate resistance R_G = 5, 15, 30, 45Ω.

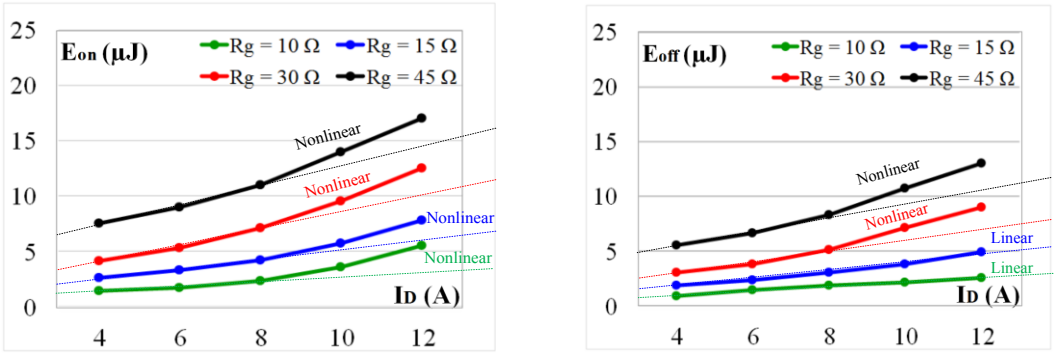


Fig. 3.26 Switching energies E_{ON} (a) and E_{ON} (b) versus the drain current I_D for the normally-on GaN HEMT at different switching speed (V_{DS}=100V and I_D =12 A. Gate resistance R_G = 5, 15, 30Ω.

Switch	V_{DS} / $I_{D\,(rated)}$	Q_g (nC)	$R_{ON(rated)}$ (mΩ)	Q_g x R_{ON}.(Ω x nC)	Package
IRF740	400/10	43	480	20	TO220
EPC2010*	200/12	5	25	0.125	TO220
Normally-on HEMT	400/12	6,2	80	0.52	A0191
Normally-off HEMT	400/12	5,5	85	0.47	A0191

Table 3.8 Comparison of gate charge at the test condition V_{DS} = 100V, I_D = 12A, T_j = 25° C.
*Since a 400V/12A GaN HEMT was commercially not available, a 200V/12A transistor has been selected for this comparsion.

3.4.2 Switching Characteristics of the Investigated 600 V GaN HEMTs

In this section, 600V normally-off GaN HEMTs based on p-GaN gate technology are investigated and compared (i) to a normally-on GaN HEMT with Schottky-type gate and (ii) to the high voltage super-junction MOSFET from Infineon's latest C7 CoolMOS generation (CoolMOS™ C7 "IPP65R125C7") [47]. Fig. 3.27 depicts the measured switching transients of the investigated transistors for 300 V and 10 A. A 10 □ gate resistor was used for these measurements at room temperature. The test results are obtained applying a new 600 V GaN Schottky freewheeling diode developed at FBH [21][109]. As seen in the results, a significant current and voltage oscillation is observed during the transients. The parasitic inductances (L_{SS}, L_D and L_S) and source inductance (L_{DC}) as given in Fig. 3.20 have the major impact on the switching transients. Also, the parasitic capacitances C_{DG}, C_{GS} and C_{DS} influence the transient significantly. While the drain gate capacitance C_{GD} regulates the *dv/dt* of GaN transistor, the gate-source capacitance C_{GS} determines the *di/dt*. Further, the charging and discharging current of the drain-source capacitance C_{DS} are forming the drain current peak during turn-on and turn-off. Because of the high switching speed of the GaN HEMT parasitic elements become a serious problem during the transients. For that reason, the large power and gate loops in the PCB layout can be a limiting factor in the dynamic performance of GaN transistors. Therefore, an identical PCB with very short power and gate loops is developed and used for the three investigated transistors. However, it is obvious that the investigated transistors behave differently during the transients.

As seen in Fig. 3.27 the normally-on device characterizes higher current and voltage oscillations during the transients compare to the normally-off and super-junction MOSFET devices. This probably refers to the small parasitic capacitances of the normally-on device compared to other devices. To guarantee a safe operation of GaN devices during the transients, a realistic compromise between the maximum switching performance and a larger gate resistance to decrease the signal overshot and oscillation has to be considered. In conclusion, Table 3.9. summarizes the electrical characteristics including the evaluated FOM (R_{ON} x Q_g). Obviously, the normally-off GaN HEMT achieves a better FOM than the normally-on device and of course than the super-junction MOSFET. It seems that the normally-off device has a further physical improvement over the normally-on. This is obvious regarding to the high current capability of the normally-off device, which also results in a lower R_{ON} (65 mΩ), approximately the half of the value in the normally-on device (R_{ON} = 125 mΩ). On the other hand, increase of the total input capacitance C_{GS} results in a total gate charge of 15nC; this is a factor of 1.63 higher than the normally-off. Lastly, the larger chip size and the technological enhancement are probably the reason for the improvement of the dynamic bahaviour in the normally-off device.

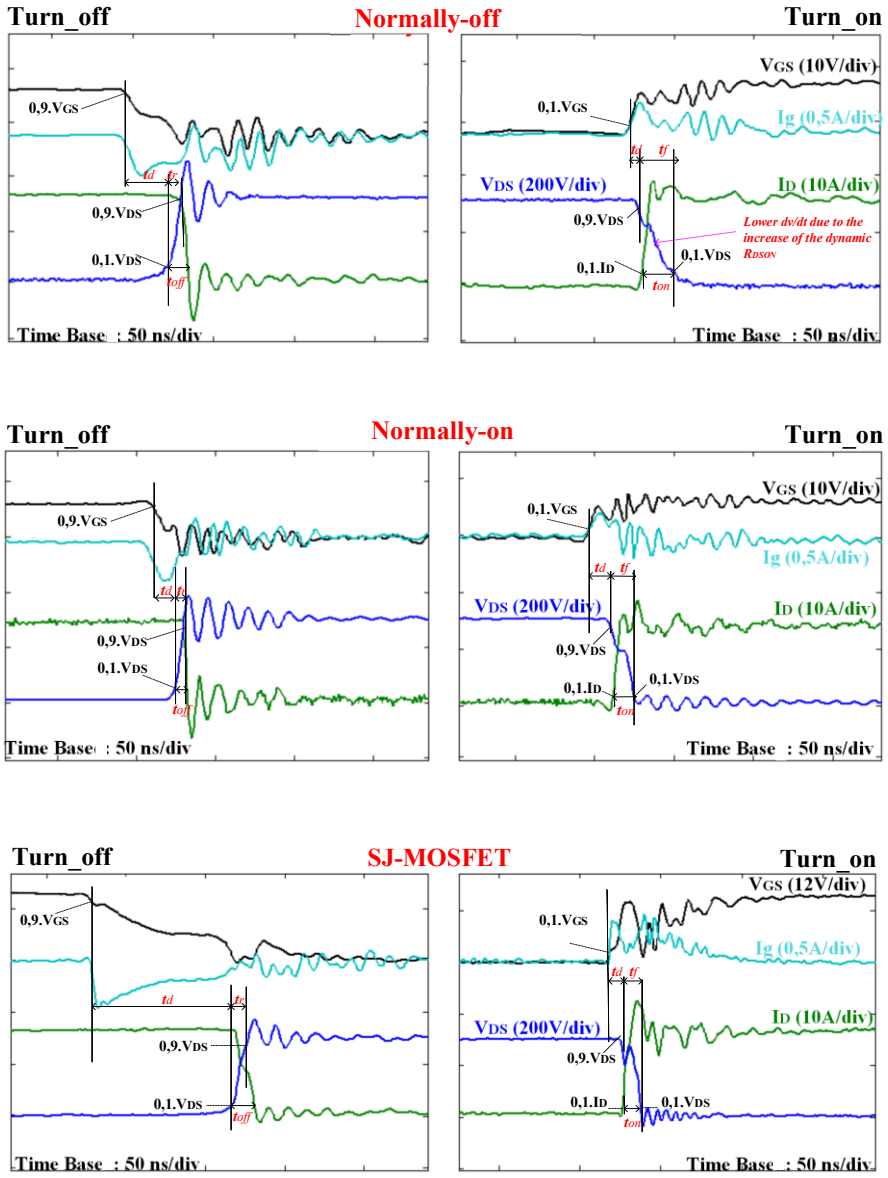


Fig. 3.27 Measured switching transients of the investigated normally-on and normally-off GaN HEMTs and super-junction MOSFET in the double pulse test. V_{DS} = 300 V, I_D = 10A and R_G =10 Ω. T= 25°C.

Parameters	Investigated GaN HEMTs and Si MOSFET (V_{DS} =300V, I_D = 10A, Rg =10 Ω, T= 25°C)		
	Normally-on HEMT	Normally-off HEMT	SJ-MOSFET C7
$V_{DS,max}$ (V)	600	600	650
Turn-on: t_d, t_f, t_{on} (ns)	7, 14, 21	10, 18, 28	25, 19, 35
Turn-off: t_d, t_r, t_{off} (ns)	19, 4, 15	27, 6, 33	78, 7, 84
R_{ON} (mΩ)	150	65	125
Q_g (nC)	9.2	15	38
R_{ON} (Ω) x Q_g (nC)	1.4	0.98	4.7

Table 3.9 Electrical characteristics of the investigated transistors

4 On-state Resistance of GaN HEMT

A key parameter for a highly efficient power system is a low on-state resistance at high power, high temperature and high switching frequency. Generally, the evolution of the power devices begins with the enhancements at the semiconductor-manufacturing level. The increase of the dynamic on-state resistance, however, caused by different impacts like the longtime stress of the off-state, high blocking voltage and high switching frequency still remains a basic challenge in GaN development and technology. To gain a deep insight into this important area, a systematic study is presented of the dynamic on-state resistance of Gallium Nitride High-Electron-Mobility Transistors (GaN HEMTs) at high voltage operation. The related experimental results that were achieved for this topic have been published in [22]-[24].

4.1 Physical Background

In recent years, a large number of studies are focusing on the design of GaN-based power devices. Some physical problems persist related to the fabrication processes that limit the device performance and reliability. One typical problem in GaN HEMT is *"current collapse*" [75]. This refers to a reduction of the drain current in the GaN channel lower than what is expected. This phenomenon is also referred to as "*current dispersion*" or "*current compression*" [86]. Different studies make a distinction between the device's degradation and current collapse. The breakdown failure mechanisms in AlGaN/GaN HEMTs have been studied and reviewed in [81]-[83], while device degradation was addressed in [84][85] and the current collapse covered in [86]-[89]. These failure mechanisms in the device lead to a temporary or permanent reduction of the drain current: a) Permanent reduction of the current is attributable to current collapse. b) Temporary reduction of the current is attributable to the device degradation after long-life tests.

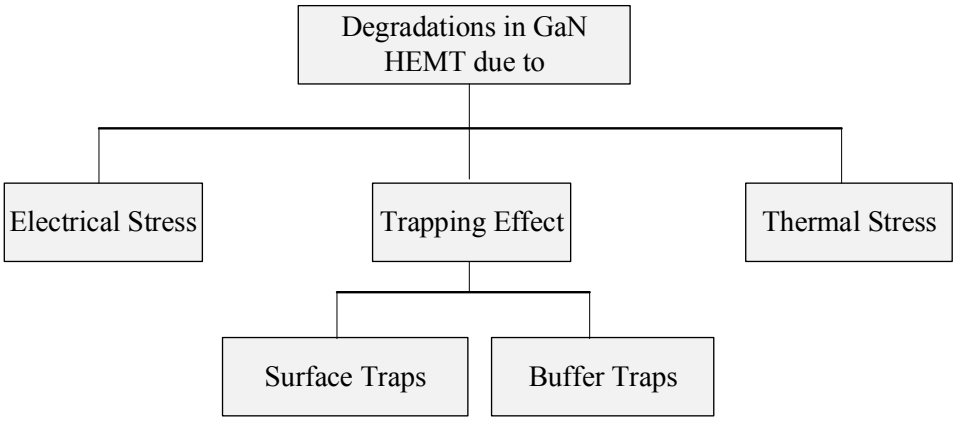


Fig. 4.1 Degradations in GaN device caused by the presence of different effects.

Both device degradation and current collapse in GaN HEMT are, related to the trapping effects. As discussed in [32], device degradation refers to trapped electrons in newly created traps, while current collapse refers to trapped electrons in already existing traps.

4.1.1 Electrical Stress

Degradation on account of the electrical stress in GaN HEMT is discussed in [79][80]. For both enhancement and depletion mode GaN devices (normally-on and normally-off) the electrical degradation is described as the increase of the gate leakage current and reduction of the drain current. This degradation is caused by a built-in "*tensile electrical stress*" that causes considerable defects or crack density in AlGaN layer, limiting the performance of GaN device [79] as described in Fig. 4.2.

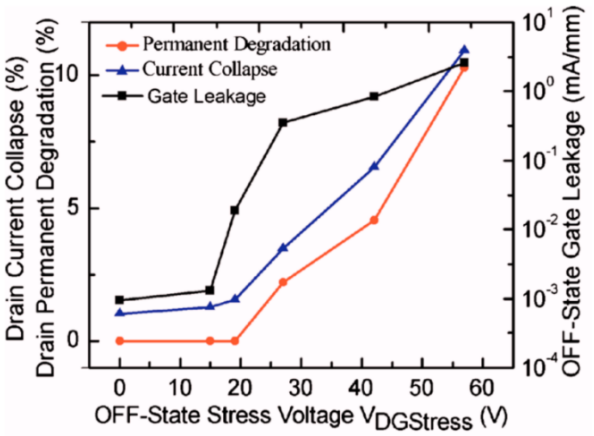


Fig. 4.2 Current degradation after applying electrical stress [79].

4.1.2 Thermal Stress

Even though GaN HEMTs can operate at high temperatures, the thermal stress can substantially degrade and limit the performance of the device. As the experiments and discussion in [79] show, if the GaN device is stressed for long time under high off-state DC voltage, a thermal storage builds up an additional interfacial layer formed between the gate and AlGaN surface. This results in a resistance increase of the ohmic contact along with an increase in surface roughness. This device degradation through the change of Schottky barrier height and increase in ohmic contact resistance because of the thermal stress results in a shift of the threshold voltage and collapse at the drain current in GaN HEMT [79].

4.1.3 Traps

During the fabrication process of AlGaN/GaN HEMT some defects in the AlGaN and GaN materials occur [90]. Thus, undesirable imperfections often referred to as "*traps*" are found in the GaN or AlGaN layers or in the surface by applying the fabrication technique. The traps cause a serious unwanted effect in GaN HEMT, which is claimed to be the main reason for the current dispersion in GaN HEMT. The transient time constants of the trapped electrons depend basically on the energy level of the traps [91]. As experimentally observed in [92][93] traps with long time constants can be in the order of hundreds of milliseconds or even of seconds and therefore the trapped electrons cannot follow the high frequency signal during operation. Subsequent to an immediate change of the gate voltage, the trapped electrons will need time to be released and the channel remains partially depleted. It is

quite difficult technically to control the traps' density in the material during the fabrication process of GaN devices. A chief result of the trapping phenomenon in GaN HEMT is the substantial increase in dynamic on-state resistance (R_{DSON}) during continuous operation. In recent years, several research groups [94]-[98] have examined the degradation of on-state resistance at high off-state voltage and high-frequency operation. Such degradation mainly results when a part of the electrons, moving in the Two Dimensional Electrons Gas (2DEG), are trapped in the GaN buffer or at the AlGaN layer under different stress conditions. Khan et al. [99] was the first to present the expected trapping locations in AlGaN/GaN HEMT. As they reported, traps can be present at different places: 1) the semi-insulating substrate in the case of growth on SiC, 2) at the interface between GaN and the substrate in the case of sapphire or SiC, 3) in the high-resistivity GaN buffer, 4) at the AlGaN/GaN interface (at both sides of the heterojunction), or 5) in the AlGaN barrier layer.

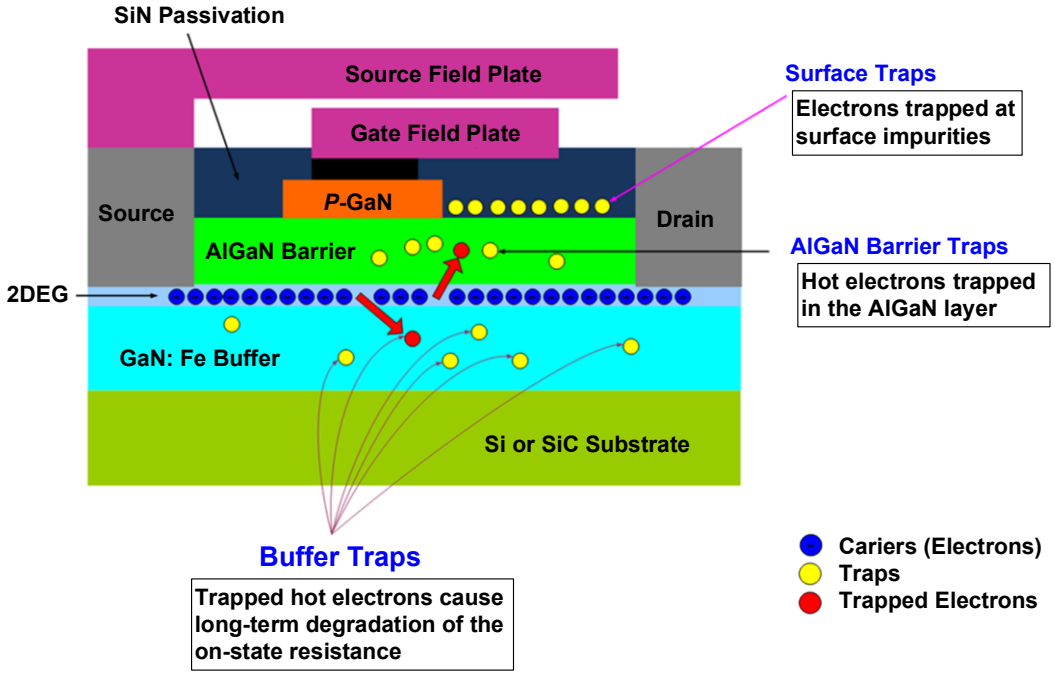


Fig. 4.3 Basic normally-off GaN HEMT structure with p-GaN including the possible trapping locations.

The origin of traps in the device remains a topic of debate [79]. In current devices, one can find them in different locations as described by [99], in the bulk and at the surface. Fig. 4.3 reveals the fundamental structure of the normally-off GaN HEMT using p-GaN gate showing the possible locations of traps. SiN passivation and field plates positioned on the surface represent new technologies to reduce trapping effects on the surface of the GaN HEMT.

4.1.3.1 Surface Traps (Surface States)

Traps present on the surface of the GaN/AlGaN HEMT are called *surface states* or *surface traps* [39][40][41][99]. Vetury et al. [100] first reported on the impact of surface states. This type of trapping is associated with polarization during the growth process of the AlGaN barrier on the top of GaN

layer. Different technologies have been used in recent years in order to reduce the effects of the surface states in GaN HEMTs. As depicted in Fig. 4.4, two gates are present on the surface, between the source and drain and are connected in series [31][40]. The potential on the second gate *"virtual gate"* is mainly controlled by the total amount of trapped charges in the gate drain access region. As several scientific studies have shown, the use of silicon nitride SiN passivation on the surface of the AlGaN considerably decreases the effect of the surface states on the electrons being trapped on the surface. Other technologies have been made by different research groups in order to reduce the trapping effect. One of these technologies is to add multiple field plates on the top of the device. These field plates help to reduce the electric field at the gate edge, which, as a result, reduces the trapping effects in the AlGaN/GaN HEMT. Vetury et al. [100] suggest that SiN passivation interrupts the positively charged surface donors and renders them inaccessible to electrons leaking from the metal gate. Some solutions, including single [42]-[44] or multiple field plates [45], have been proposed to avoid the creation of a virtual gate. Using SiN passivation at the surface or using field plates does not, however, have an impact on the traps created in the buffer layer.

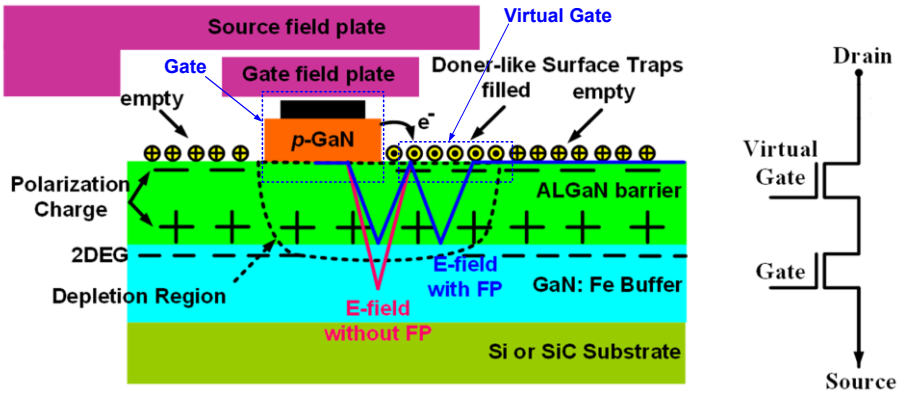


Fig. 4.4 GaN HEMT Structure with p-GaN including a description of the empty and filled surface traps which acts as a virtual gate, depletion region, polarization charges and distribution of the electric field with and without the field plates [31][40].

To understand how trapped electrons on the surface can impact the drain current flowing through the GaN channel, it is important to understand the formation of the 2DEG at the AlGaN/GaN heterojunction and polarization effect during the AlGaN/GaN growth process. In principle, when a semiconductor material such as Aluminum Gallium Nitride (AlGaN) grows on top of another such as Gallium Nitride (GaN), the result is a complex band structure in which the crystal lattice of upper material (AlGaN) becomes compressed and strained. The problem is that AlGaN and GaN semiconductor materials have different lattice constants, that is to say different physical dimensions of unit cells in lattice crystals. By attempting to grow AlGaN on the top of GaN layer, one is thus trying in effect to match a wide lattice to narrow lattice (see Fig. 4.5). As a result, the strained lattice will have charges where the electrons sheets are not the same as they were previously and a sub-electric field is created due to charges in those positions. Basically, two types of polarization build up in the AlGAN/GaN structure: spontaneous and piezoelectric polarizations. Spontaneous polarization corresponds to the polarization field in an unstrained crystal. By contrast, the piezoelectric polarization results from

crystal lattice distortion, where the charges create an electric field in the strained layer. Some device degradations in the AlGaN/GaN HEMT are caused by stress-induced defect generation via the converse piezoelectric effect [29]. The sum of both spontaneous and piezoelectric polarizations contributes to forming the two-dimensional electron gas (2DEG) that contains a sheet with very high electron density.

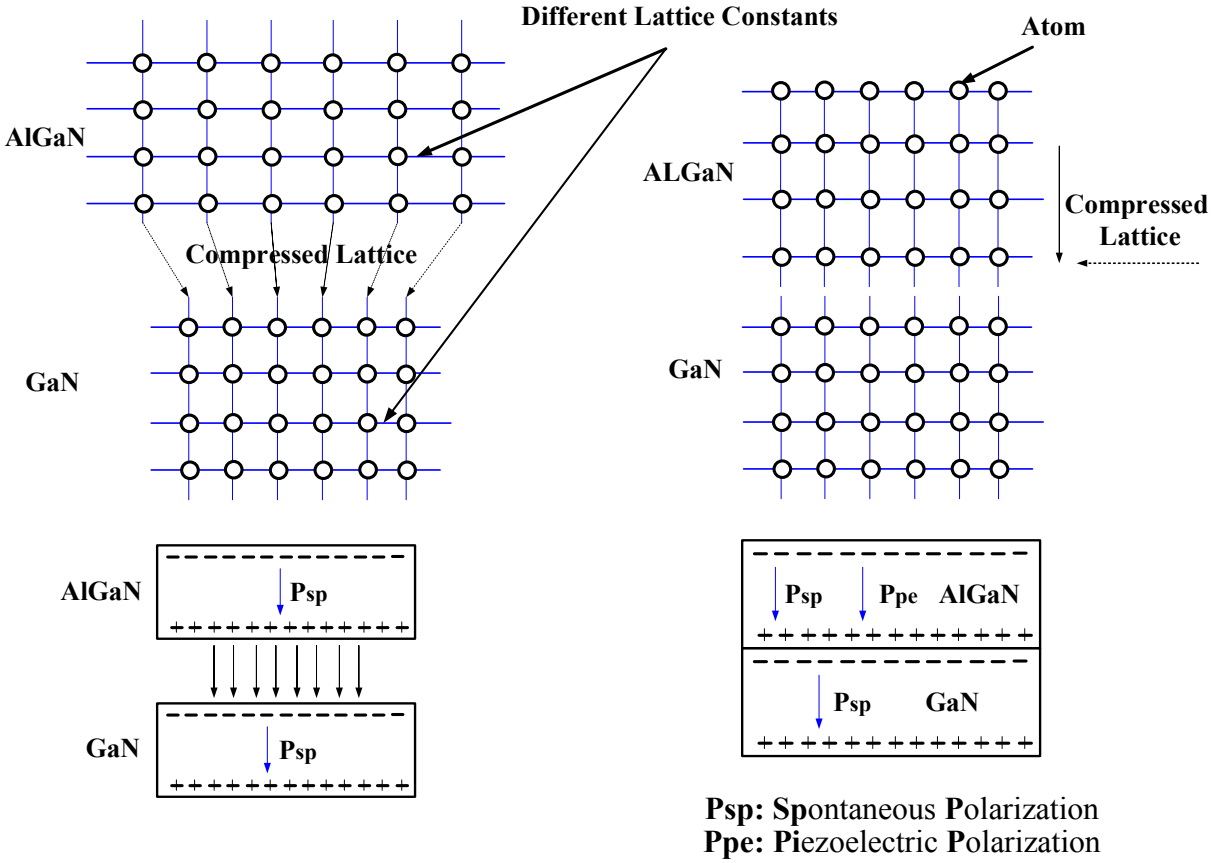


Fig. 4.5 Creation of the piezoelectric polarization in the AlGaN layer at the expense of lattice distortion during the growth process, where the lattice of AlGaN has been strained to match the lattice of GaN [31].

The polarization field represents the dominant controlling factor for the charge and electric field distribution in GaN HEMTs [119]. The only materials demonstrating spontaneous polarization are the III-V nitrides. This represents a major advantage compared to other materials when high electron mobility is sought [119]. Furthermore, charge polarization can affect the carrier confinement at the heterointerface between GaN and AlGaN layers. Both AlGaN and GaN will have their spontaneous polarization. Only the AlGaN layer, however, will have the piezoelectric polarization because of the strain and distortion of the lattice during the growth process on GaN layer, which is depicted in Figure 4.5. Because the layer thickness of the AlGaN layer increases during the growth process on the GaN buffer, the internal electric field that is created due to the piezoelectric polarization becomes high enough to ionize the donor states at the surface. When the AlGaN barrier achieves a critical thickness, the trap level reaches the Fermi level and the traps begin to empty, becoming positively charged. Because of the strong electric field, the electrons move down into the channel [66]. Thus, the existence of the polarization in the AlGaN barrier layer alone is not sufficient for a 2DEG to form the potential

well at the AlGaN/GaN interface. A positive sheet charge therefore must exist at the AlGaN surface in order to form the 2DEG in the heterojunction [31].

4.1.3.2 Buffer Traps

As shown in Fig. 4.3, the buffer layer also represents a possible location for trapping in the AlGaN/GaN HEMT. By the application of the high voltage between the drain-source terminals, a high electric field is created and the electrical stress in the GaN channel also becomes high. As a result, the electrons moving in the 2DEG channel may become captured into the buffer traps. Buffer traps in GaN transistors may have time constants (de-trapping time) of milliseconds, but some may require 10's or 100's of seconds, which is considerably longer than observed in GaAs [70]. Because of the longer trapping time constant, the trapped electrons cannot follow the high frequency signal. Thus, they are not available for conduction [70]. These trapped electrons also create a negative charge and this again acts to deplete the 2DEG, further reducing the channel current. Employing the gate field-plate to spread out the electric field near the gate edge of the drain side represents a conventional approach for improving device performance [79].

4.1.4 Hot Electron Effect

Binari [94] was the first to report the correlation between the "*current collapse*" and the "*hot electron*" by deep traps in the buffer layer. Contrary to the trapped electrons in GaN HEMT under static or dynamic stress, hot electrons arise and are trapped only under high dynamic electrical stress conditions. When the GaN HEMT is switching high power transients (high current, high voltage) at high switching frequency, the electrons in the channel are accelerated by the produced high electric field. They possess a large amount of kinetic energy ("hot electron") and thus may have enough energy to induce traps either in the channel, in the barrier or at the interface [17][79]. Hot electrons may also tunnel to the gate or the AlGaN surface and become injected in the traps there. With respect to the current collapse caused by the presence of trapped electrons in general, and particularly with regard to the hot election injection, dynamic tests are performed under static, low dynamic and high dynamic stress conditions to differentiate between the observed degradations and effects occurring in GaN HEMT during different operation modes.

4.2 Device under Test

With respect to the dynamic on-state resistance R_{DSON}, the 600V GaN HEMTs and the super-junction MOSFET presented in chapter 3 are systematically investigated by means of different dynamic tests. The results are presented and discussed in the section 4.4. The brief experimental results, however, of early-stage 870V/1.5A and 400V/12A GaN devices are presented here. These suffer from very high dynamic R_{DSON} increase at high off-state voltage and are therefore well-suited to highlight the degradation and limitation of R_{DSON} in GaN HEMT. In contrast to these devices, significant improvements in the switching performance and R_{DSON} have been achieved with the aforementioned 600V GaN HEMTs. The switching characteristics are evaluated using double pulse tests. The circuit used in the test is the commonly used buck converter (the test circuit is shown in section 2.1.1). Fig. 4.6 presents the measured waveforms of the investigated 870V normally-off GaN HEMT at off-state voltage

V_{DS} 375V. The drain current I_D reaches 0.7A and 0.9A during the first and second pulse, respectively. The applied gate source voltage V_{GS} was +2V/-5V. As seen, a high R_{DSON} of the investigated device is observed and the measured on-state voltage V_{DSON} reaches 200V at 0.75 A. Fig. 4.7 demonstrates that the measured off-state voltages of the 870V normally-off GaN HEMT varied from 50 V to 375 V at constant drain current. As can be seen, at higher off-state voltage, the on-state voltage V_{DSON} will increase significantly. When the current increases in the second pulse, the on-state voltage will also increase and reaches 325V of the applied 375V off-state voltage at t = 7.75µs. This is about 86% of the off-state voltage, while the measured drain current reaches 0.9 A. At t_2, the peak current reaches 2A; this probably refers to the junction capacitance Cj of the freewheeling diode. As discussed above, AlGaN/GaN HEMTs are hampered by the undesirable electron trapping effect phenomena. As seen, the measurement shows an enormously high value of dynamic R_{DSON}. This possibly indicates that the trapping effects at the early stage of GaN development are particularly high.

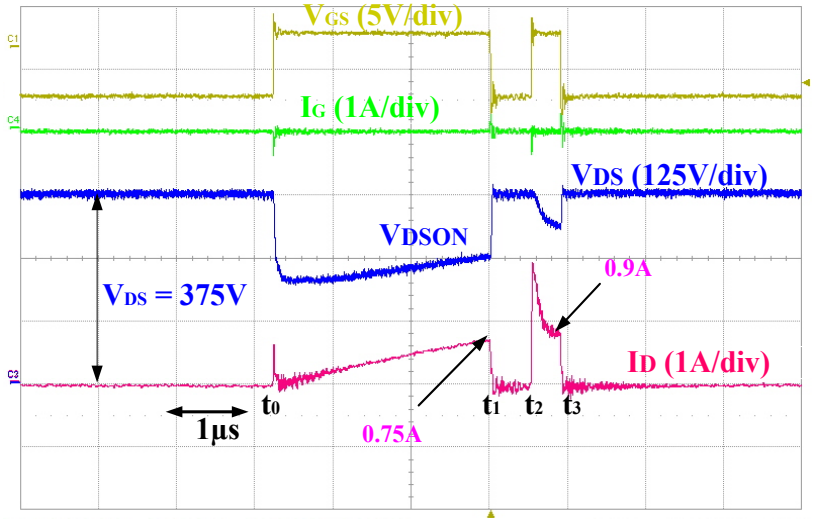


Fig. 4.6 Measured double pulse waveforms of the investigated normally-on GaN HEMT at V_{DS} = 375V and I_D = 0.75A at t_1, T=25°C..

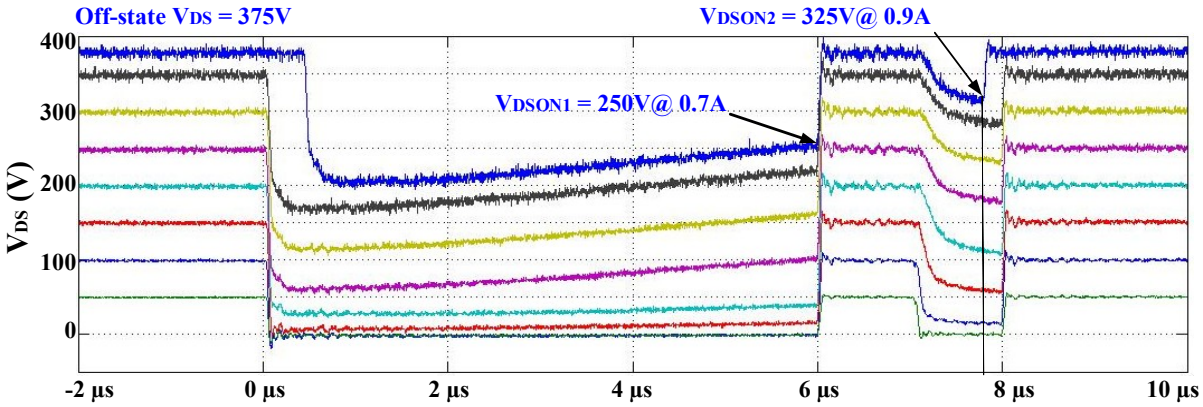


Fig. 4.7 Measured off-state voltages of the investigated (870V/1.5A) normally-off GaN HEMT. V_{DS} is varying from 50V to 375V and I_D increases from 0.7A to 0.95A during the 2nd pulse. T=25° C.

Fig. 4.8 presents the measured V_{DS} transients of the 400V/12A (2nd development) normally-off GaN HEMT at different off-state voltages V_{DS} = 50V…200V and constant currents I_D = 12A. The switching test is conducted at 25° C. Test results were obtained by applying a fast SiC Schottky freewheeling diode C2D10120 [71]. From a technology view, some design adjustments and changes were carried out compared to the first normally-off device development. Since the transistor is manufactured based on SiC substrate, it represents a combination of an AlGaN back barrier with the carbon-doped buffer to avoid the quick off-state punch-through [102].

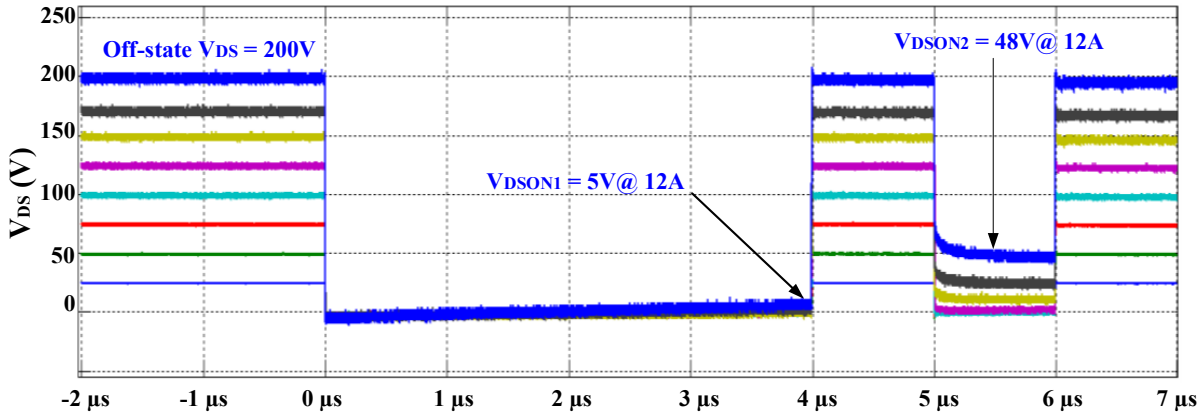


Fig. 4.8 Measured off-state voltages of the investigated (400V/12A) normally-off GaN HEMT. V_{DS} is varying from 25 V to 200 V and I_D increases from 11A to 12A during the 2nd pulse. T=25°C.

In comparison with the previous measurements of the 870V/1.5A device, a clear improvement in terms of the dynamic R_{DSON} has been achieved. Nevertheless, the measured value of the dynamic R_{DSON} remains high with regard to the static R_{ON}. Fig. 4.9 and Fig. 4.10a summarize the measured V_{DSON} and the evaluated R_{DSON} of the (2nd development) normally-off GaN HEMT at different drain current varying from 3A to 12A. Depending on the results, it is thus evident that the increase in the off-state voltage and switching a higher drain current will substantially influence the value of the R_{DSON}. The noticeably high increase in the R_{DSON} may refer to a high number of trapped electrons in the buffer layer or at the surface of the transistor.

Since the measured values of the R_{DSON} of the 1st and 2nd developments of GaN HEMTs (870V/1.5A and 400V/12A) were quite high, there was no need to employ any specific technique to measure the V_{DSON}. The ratio between the measured on-state and off-state voltages for the 1st and 2nd developments of GaN HEMTs were 1:8 at 9A and 1:1.5 at 0.7A, respectively. As the new 600 V normally-on and normally-off GaN HEMTs (3rd development) using p-GaN continues to be developed, a considerable improvement in the technology has been achieved regarding the dynamic R_{DSON} and trapping effect phenomena. In the next section, a new measurement method used to extract the dynamic R_{DSON} of GaN devices will be presented. Thereafter, a systematic investigation of the dynamic R_{DSON} will be carried out using this method.

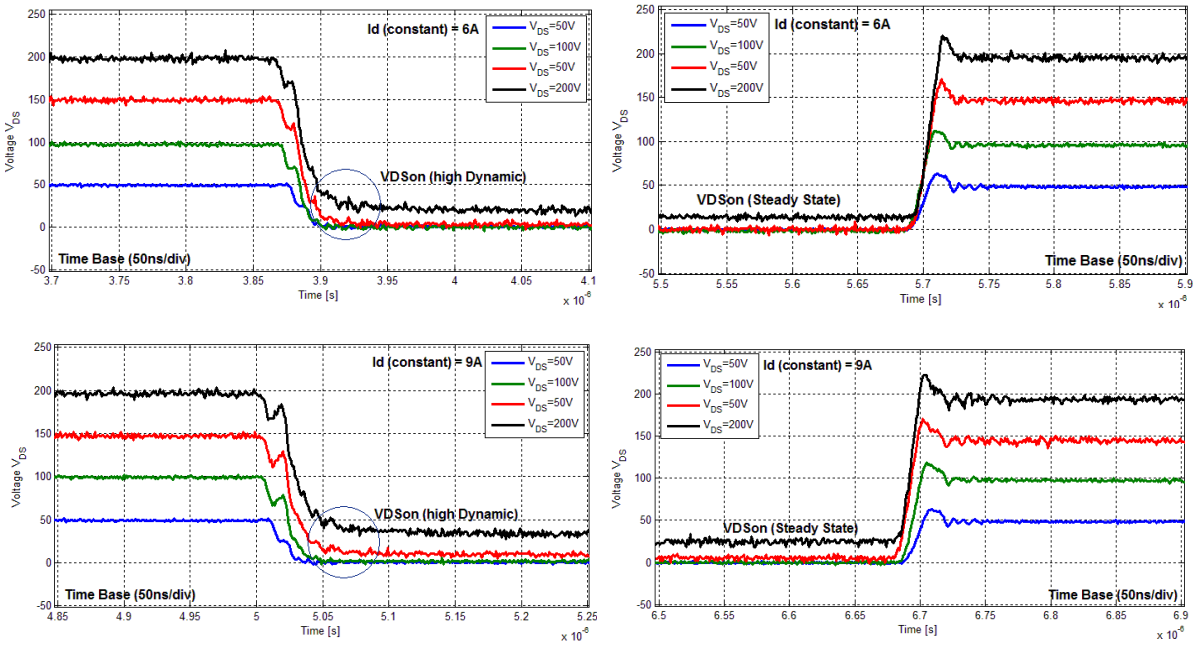


Fig. 4.9 Measured normally-off GaN HFET drain source voltage V_{DS} waveforms at different off-state voltages V_{DS} = 50V…200V and different switching drain current I_D of 6A and 9A. R_G = 15 Ω and T= 25°C. These results were taken from the master's thesis [157].

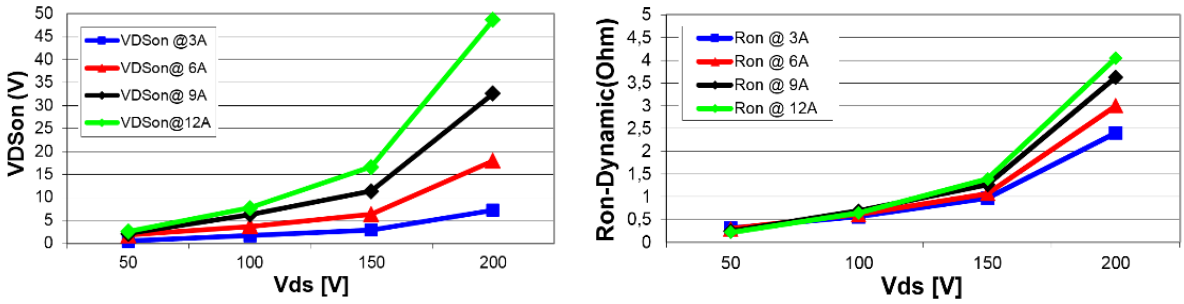


Fig. 4.10 Measured dynamic on-state voltage V_{DSON} (left) and the calculated on-state resistance R_{DSON} (right) for the investigated normally-off GaN HEMT at different off-state voltages V_{DS} = 50V…200V and different switching drain current I_D = 3A…12A. T= 25°C.

4.3 Extraction of the Dynamic On-state Resistance of GaN Power HEMTs

4.3.1 State-of-the-Art

Since the drain source voltage of the GaN device changes between hundreds of volts in the off-state and a few millivolts in the on-state, an accurate determination of the on-state voltage V_{DSON} is not achievable with standard measurement equipment due to the saturation of the DSO's input channel. In order to measure and display the dynamic R_{DSON}, the measurement equipment must be able to capture and observe the on-state voltage V_{DSON} immediately after the transients in the nanoseconds range.

Principally, the instantaneous dynamic value of R_{DSON} can be extracted from the measured V_{DSON} divided by the measured drain current I_D during on-state. In this section, a new measurement method used to extract the dynamic R_{DSON} of GaN HEMTs is proposed. This method is based on a high-voltage, fast-switching zero recovery SiC Schottky diode as a main component of a clamping circuit. The proposed method allows an accurate measurement of R_{DSON} from 200 ns after turn-on to any arbitrary time and is feasible for operation at high switching frequencies up to 1MHz. Applying this measurement method, the 600V normally-off and normally-on GaN HEMTs grown on Si and SiC substrates are experientially investigated at different blocking voltages, switching currents, frequencies and speeds. The results are compared to the commercial state-of-the-art super-junction silicon MOSFET operating under hard-switching conditions. In the last years, few references [50][76][77][103] have discussed how to measure the dynamic on-state resistance of fast-switching power devices. Clamping measurement approaches have been demonstrated in [78][101][154].

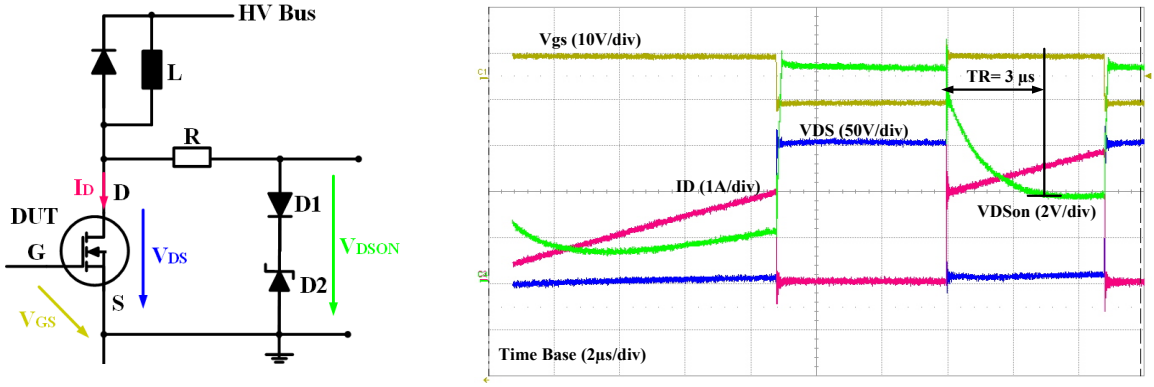


Fig. 4.11 Measured double pulse waveforms (right) of the investigated 400V normally-off GaN HEMT at V_{DS} = 150V and I_D = 2A using a simple clamping circuit based on Zener diode for R_{DSON} measurement (left).

A summary of published voltage clamping circuits used to measure the dynamic on-state voltage V_{DSON} is given in Fig. 4.12. The first clamping circuit in Fig. 4.12a consists of a Zener diode and a high ohmic resistor. The input terminals are connected directly to the drain and source of the investigated transistor, and the output voltage is equal to the rated Zener diode voltage V_Z during the off-state and to the DUT's V_{DSON} during the on-state. The advantage of this circuit is its simplicity: no external voltage source and no differential measurement are needed. The long-time reaction (RC-delay) of V_{DSON} caused by the resistor R in series with the Zener diode capacitance is the main disadvantage of this method. Fig. 4.11 shows this clamping circuit (passive clamping circuit) connected to the drain-source terminals of the active switch of the buck converter (left). As seen from the measured waveforms (right), the time reaction of V_{DSON} reaches 3 µs. Due to this long time reaction, value and behavior of the R_{DSON} at the high dynamic area are not observable. Using this simple method, as seen in Fig. 4.11, only the measured steady-state of V_{DSON} after 3 µs can be considered. However, it is necessary to measure the on-state voltage as close as possible to the voltage transient to observe the high dynamic region, which is usually less than 500 nanoseconds. In circuit II (Fig. 4.12b), the RC-delay is significantly reduced by using a p-channel MOSFET (RC-delay < 300ns) [78]. Circuit III (Fig. 4.12c) is a combination of circuits I and II, which has the advantages of both methods [101]. Circuit IV (Fig. 4.12d) is the last presented clamping circuit [154].

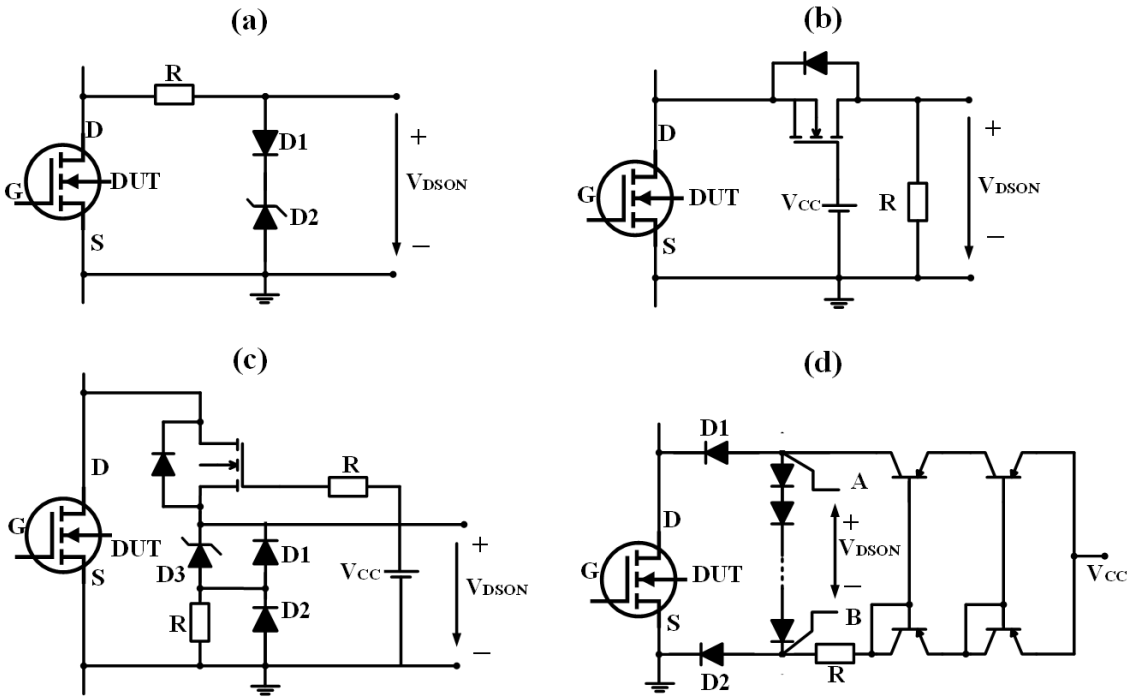


Fig. 4.12 Voltage clamping circuits for dynamic R_{on}. (a) Clamping circuit I based on Zener diode. (b) Clamping circuit II based on p-channel MOSFET [78]. (c) Clamping circuit III is a combination of I and II [101]**.** (d) State-of-the-art clamping circuit IV [101][154].

	Circuit I	**Circuit II**	**Circuit III**	**Circuit IV**	**Circuit V (proposed)**
Based on	Zener Diode	MOSFET	MOSFET	p-n Diode	SiC-SBD
RC Delay	> 3000 ns	< 300 ns	< 300 ns	< 100 ns	< 100 ns
Clamped Voltage	No Limit	600V	600V	300V	600V
External Source Voltage	Passive	8 V	8 V	5 V	Self-feeding
V_{DSON} Measurement	⊥ GND	⊥ GND	⊥ GND	Differential	⊥ GND
Voltage Offset	Subtracted	Subtracted	Subtracted	Not introduced	Subtracted

Table 4.1 Comparison between the voltage clamping circuits

Compared to the conventional clamping circuits, this method allows higher measurement accuracy due to the use of an extremely fast-switching diode with very small parasitic capacitance ($C_{Parasitic} \approx 2$ pF) and the employment of the current mirror technique. On the other hand, this approach requires the use of a differential probe. The input amplifier of the differential probe cannot completely reject the common mode signal during the measurement. Consequently, a small amount of the common-mode voltage will appear in the output and add an additional erroneous value to the measured signal [156]. Nevertheless, this method ensures a high measurement accuracy of R_{DSON} and a small RC-delay compared to the conventional circuits. In the next section, an alternative clamping circuit is proposed which is based on a high-voltage zero recovery SiC Schottky diode (600V/1A). The features of all described clamping circuits compared to the proposed circuit are summarized in Table 4.1.

4.3.2 Proposed SBD-based Clamping Circuit

The proposed measurement method is discussed in this section. Fig. 4.13 shows the proposed voltage clamping circuit. This method is based on a quite simple circuit with the SiC Schottky diodes D_1 and D_2 (CSD01060) representing the main components. As depicted in Fig. 4.14a, during the off-state the GaN HEMT will turn off and a charging current will flow through the SiC Schottky diode D_1 and charge the 450µF capacitor C. The voltage drop across the capacitor C is clamped to the rated voltage V_Z of the Zener diodes D_3 and D_4 and used during the on-state to supply the rest of the circuit. R_2 and R_3 keep the currents I_{ZD4} and I_{ZD3} through the zener-diode equal. When the DUT is switched on (Fig. 4.14b) the capacitor C starts to discharge, the discharging current will flow through the GaN HEMT via D_2.

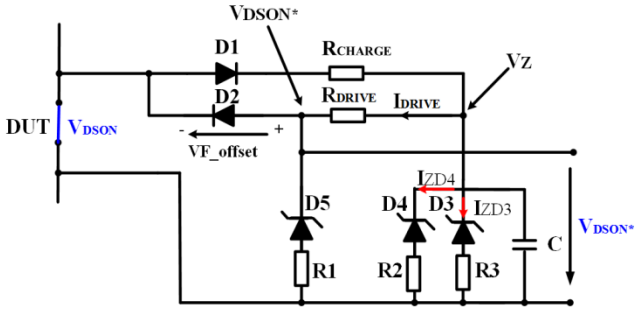


Fig. 4.13 Dynamic circuit including the proposed clamping circuit.

As a result, the measured voltage drops V_{DSON}* at the D_2-Anode terminal represents the on-state voltage V_{DSON} of the GaN HEMT plus the forward voltage V_F of the Schottky diode D_2. The measured value needs to be corrected by this voltage offset to get the actual V_{DSON}. Since the selected series resistor R_{DRIVE} is 100Ω, the forward current I_F through D_2 will reach a few milliamps. Hence, the measured forward voltage V_F of D_2 is kept nearly unchanged, with a very low tolerance between 830 mV and 840 mV due to the small change of the diode forward current I_F. Fig. 4.15 depicts the measured forward characteristics of the SiC Schottky diode at 25°C and 75°C case temperature. Since the maximum forward current in D_2 will not be higher than 30 mA in any case, an increase of the junction temperature during the measurement is not expected. The provided current I_{DRIVE} is adjusted by the selected Zener voltage V_Z and the resistor $R_{DRIVE.}$ The measured on-state voltages V_{DSON} of the investigated 600V normally-off GaN HEMT with and without the proposed clamping circuit are compared in Fig. 4.16. The transistor based on Si-substrate has 70 mΩ and uses pGaN gate technology [63]. All measurements were performed using a 400 MHz oscilloscope, 500 MHz voltage probe, and a 200 MHz Pearson Current Sensor. It can be seen that after the decay of transient effects, an accurate V_{DSON} is obtained using the clamping circuit. The peaks on the clamped voltage V_{DSON} are caused by the parasitic capacitance of diode D_2. Therefore, the capacitance is minimized by using a small SiC Schottky diode. Fig. 4.17a depicts exemplary measured waveforms of the investigated normally-off GaN HEMT during turn-on in the double pulse test. The off-state voltage V_{DS} is 200 V and the switched drain current is 5A at an ambient temperature of 25° C. The evaluated R_{DSON} in Fig. 4.17 is measured for different off-state voltages, varying from 50 V to 200 V at a constant drain current I_D = 5A. In Fig. 4.18 a, drain currents are varied from 3 A to 7 A at a constant drain source voltage V_{DS} = 200 V, and in Fig. 4.18b, the drain source voltage V_{DS} is varied from 50 V to 200 V with a constant drain current

I_D of 5A. In each figure, the stress point, i.e., the time that has passed since the occurrence of the switching event is included as a further parameter. The results show that switching from a high blocking voltage (V_{DS}) as well as switching higher drain currents significantly contribute to the increase of the dynamic R_{ON}, indicating that this increase is due to a current collapse in GaN HEMT.

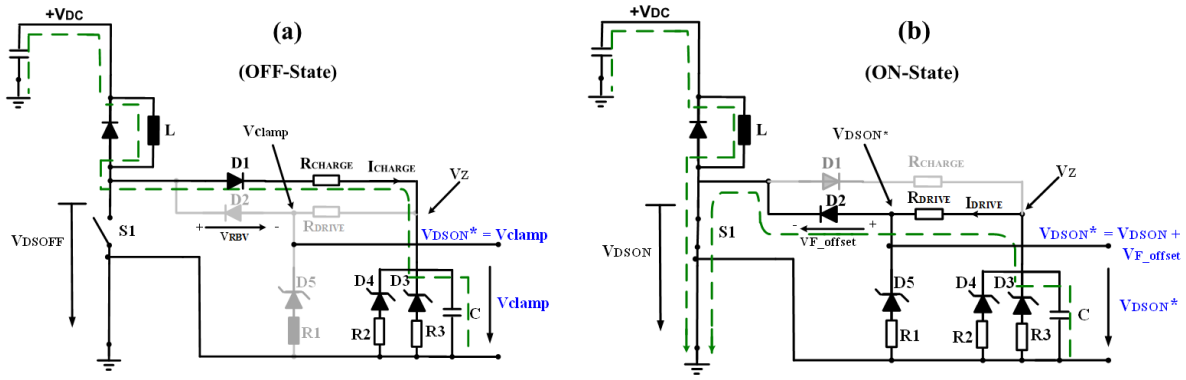


Fig. 4.14 Clamping circuit during (a) off-state and (b) on-state.

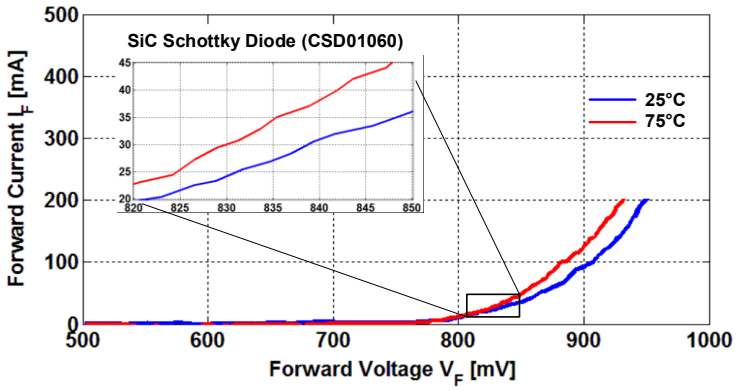


Fig. 4.15 Measured forward characteristics of the SiC Schottky diode (CSD01060) at 25° C and 75°

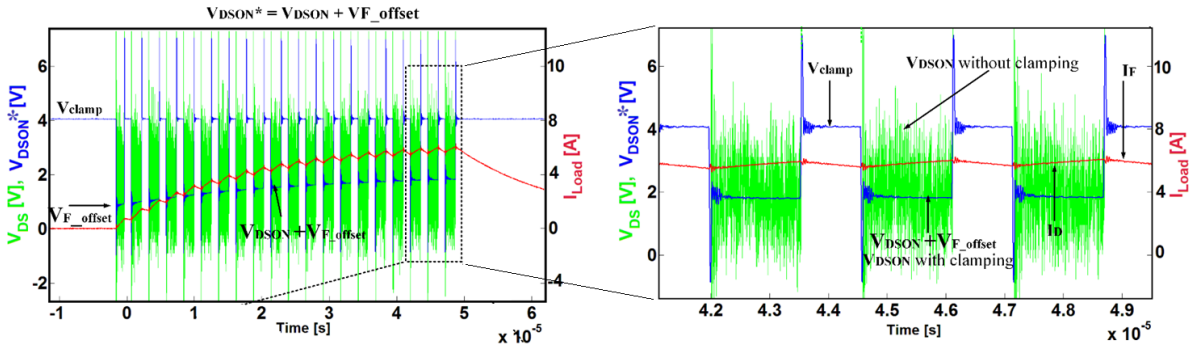


Fig. 4.16 Measured waveforms of the investigated normally-off GaN HEMT [63] with and without clamping circuit. V_{DS} = 150 V and I_D = 6 A, switching frequency 400 kHz, T=25°C.

As a final point, the results of the R_{DSON} in Fig. 4.16, Fig. 4.17 and Fig. 4.18 have been only obtained in order to validate and describe the advantages of the proposed method, while the extensive measurement and analysis of the dynamic R_{DSON} and the correlated trapping effect phenomena of the investigated 600V GaN HEMTs will be corresponding in the next section.

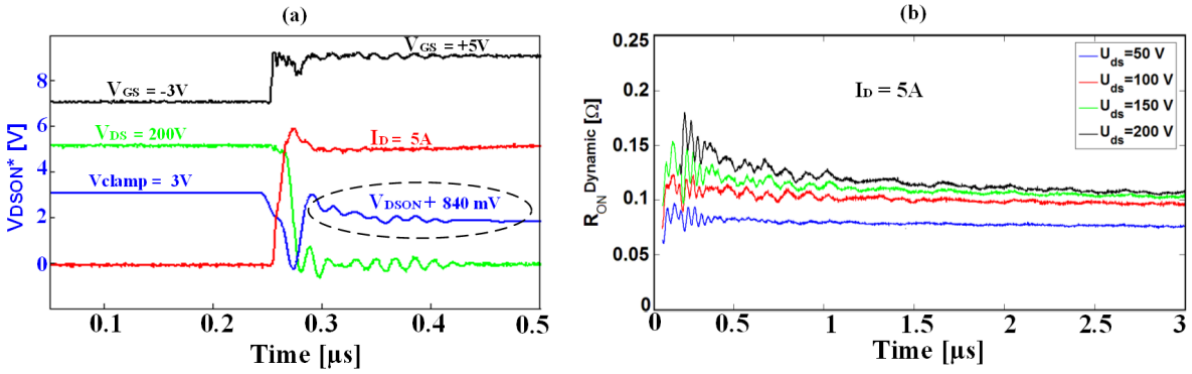


Fig. 4.17 Measured transients including V_{DSON} of GaN HEMT [63] using the proposed clamping circuit at V_{DS} = 200 V and drain current I_D = 5 A. (b) Measured dynamic R_{DSON} directly after the switching at different drain source voltages V_{DS} varying from 50 V to 200 V and 5 A drain current I_D. The test is carried out at 25° C

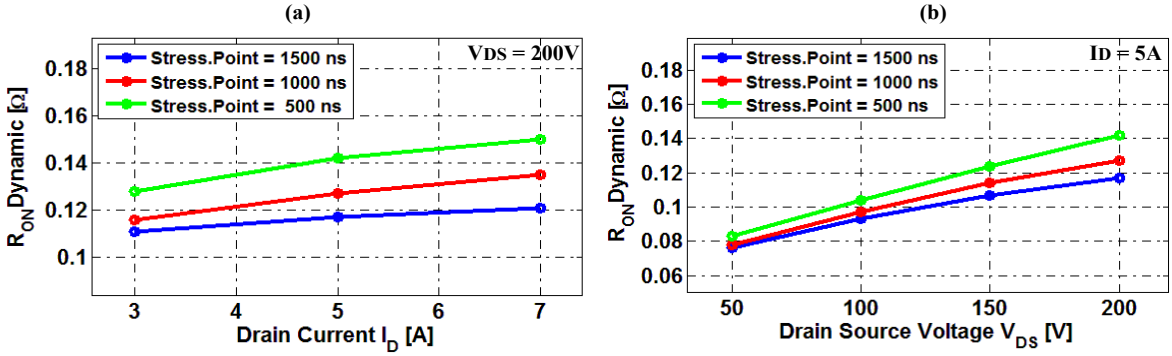


Fig. 4.18 Measured dynamic on-state resistance R_{DSON} of GaN HEMT [63] for (a) different drain currents I_D varying from 3 A to 7 A with constant drain source voltage V_{DS} = 200 V and (b) different drain source voltage V_{DS} varying from 50 V to 200 V with a constant drain current I_D of 5A. The test is carried out at 25° C.

4.4 Dynamic On-state Resistance of GaN HEMT

Regarding the dynamic R_{DSON} degradation of GaN HEMTs, a systematic investigation is performed. While the switching tests of the investigated GaN HEMTs and super-junction MOSFET were presented in the previous chapter, only the R_{DSON} degradation and the related trapping phenomenon effects are investigated in this section. The R_{DSON} of the 600V normally-off GaN HEMT with pGaN gate [63] is extracted by means of the proposed clamping circuit and then compared to a normally-on GaN HEMT with Schottky-type gate and to the high voltage super-junction (SJ) MOSFET from Infineon CoolMOS™ C7 "IPP65R125C7" [47]. Usually the high off-state voltage is considered the primary cause for the increase in the trapping in GaN transistor. Other electrical quantities also show similar impacts, however, and lead to a similar increase in R_{DSON}. Experimentally, the investigation is split up into five different tests.

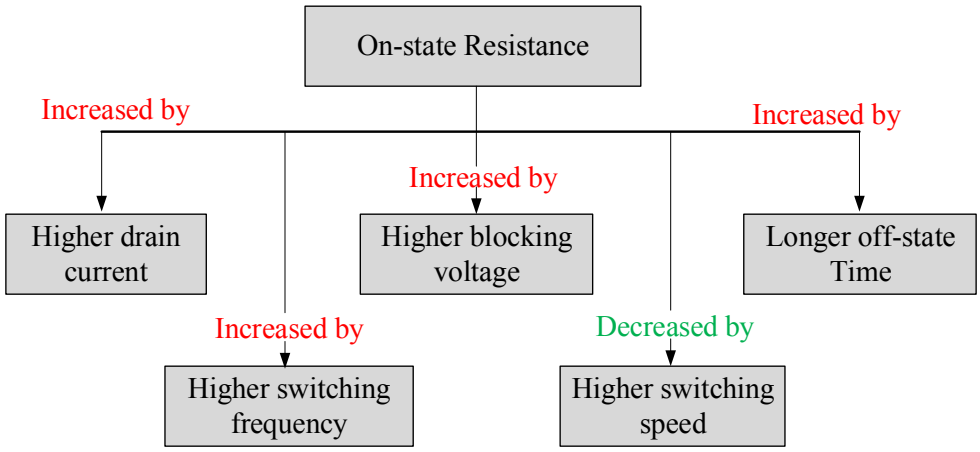


Fig. 4.19 Dynamic test conditions and their impacts on the degradation of R_{DSON} in GaN HEMT

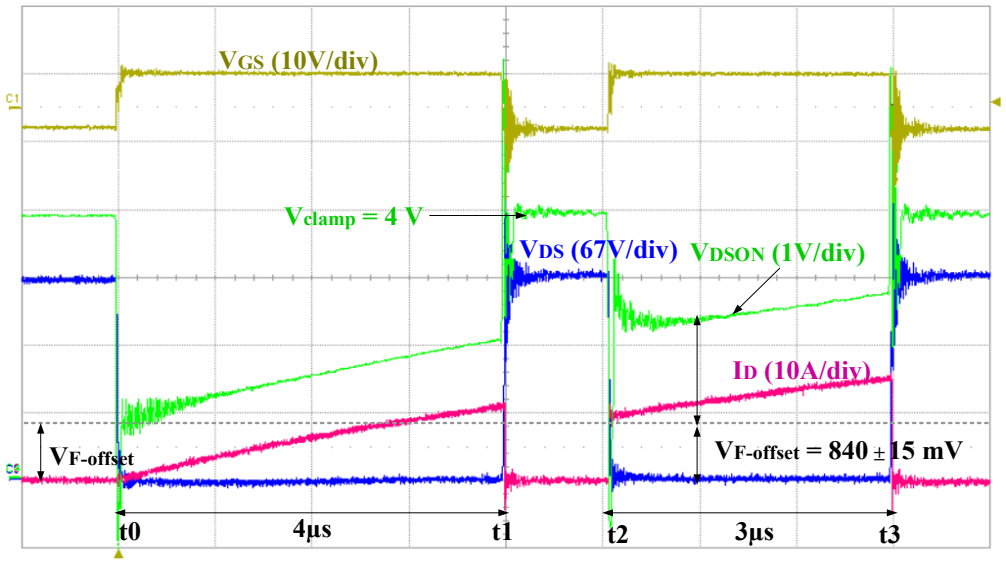


Fig. 4.20 Measured waveforms of the normally-off GaN HEMT in the double pulse test switching from off-state drain voltage V_{DS} = 200 V. I_D increases from 10 A to 14 A in 3µs. Test temperature = 25° C.

The test circuit schematic including the proposed diode-based clamping circuit is shown in Fig. 4.14. The FPGA-based platform presented in Appendix A2 is used to allow for a precise generation of pulses and their durations to drive and control the selected transistors. A gate double pulse signal was applied and the measured waveforms are depicted in Fig. 4.20. It shows sample measurement of the drain current, the drain-source voltage and the clamped voltage with R_{DSON} of the normally-off GaN HEMT. In order to limit the increase of the junction temperature (self-heating), the DUT is turned on for a short time (4 µs) during a first pulse (t_0 - t_1), where the drain current reaches the nominal value at t_1, and the DUT will be switched off for 1 µs between t_1 and t_2. The second (3 µs) pulse is then used for R_{DSON} determination. Table 4.2 summarizes the electrical and physical parameters for different dynamic tests.

Test	Impact on R_{DSON} by variation of	Blocking Voltage V_{DS}(V)	Drain current I_D (A) at Turn-on	Temperature T (°C)	Switching frequency f_{SW}
Test_1a	Off-state stress time	200	10	25	Double pulse
Test_1b	Off-state relax time	200	10	25	Double pulse
Test_2	Blocking voltage	100, 200, 300	10	25 and 150	Double pulse
Test_3	Drain current	300	5, 10, 15	25 and 150	Double pulse
Test_4	Switching frequency	200	2.15	25	50 - 400 kHz
Test_5	Switching speed	200	6	25	200 kHz

Table 4.2 Electrical and physical parameters for different dynamic tests

4.4.1 Electrical Stress

Depending on the different static and dynamic impacts on the GaN channel, the electrical and thermal stress was divided into two main parts. These are defined as static stress and dynamic stress:

- Static stress occurs after applying a high off-state voltage with specific off-state time before switching the transistor on.
- Dynamic stress occurs after switching the transistor on and is divided into three parts: high dynamic area, low dynamic area and steady state area.

The definition of these areas depends on the on-state time between the measuring point and the on-state transient. The high dynamic area refers to the on-state area directly after the voltage transient and it can take a few hundreds of nanoseconds (typically <500 ns). In this region, the trapping effect is maximal. As the on-state time increases, the R_{DSON} decreases. The steady state area refers to the area where the transistor is relaxed and the dynamic R_{DSON} shows the lowest value on account of the de-trapping mechanism (typically > 3µs). The area between the high dynamic and the steady state is defined as the low dynamic region, in which the R_{DSON} continually decreases during the on-state time. One should note that the trapping effect correlated with the hot electron injection in GaN buffer or AlGaN barrier is attributed to the defined high dynamic area under high electrical stress conditions such as high power transients at high switching frequency and low switching speed.

4.4.2 Impact of Different Off-state Times (Test_1a)

The first dynamic test is made up of two parts. The first part investigates the impact of the applied time of the off-state voltage before switching on the device at t_0. Fig. 4.21 shows the test timing conditions including the signal timing description used to investigate the impact of different off-state time (t_0 - t_1). As seen in Fig. 4.22b, the R_{DSON} of the normally-off GaN HEMT is significantly higher than the static value shortly after switching from the off-state and relaxes to a constant value after a few minutes. This is most likely because of de-trapping mechanisms in both GaN HEMTs [102]. Contrary to both GaN HEMTs, the SJ-MOSFET demonstrates a constant R_{DSON} with no more than 5% deviation from its nominal R_{DSON} value. In this experiment, the dynamic R_{DSON} of the normally-off device at 0.5 µs after switching from 200 V off-state is 170 mΩ after a blocking time of 1 second, 192 mΩ after a blocking time of 3 minutes and 200 mΩ after a blocking time of 60 minutes (Fig. 4.24).

Fig. 4.22a shows the corresponding R_{DSON} of the normally-on GaN HEMT increases, which is similar to the normally-off transistor. The dynamic R_{DSON} decreases within the on-state intervals. Table 4.3 summarizes the measured values of R_{DSON} drawn by varying the off-state time intervals.

The second part of the test is shown in Fig. 4.23. Contrary to the first part, the steps of this test were conducted in reverse order. At t_0, the negative gate source (V_{GS} = -3V) and while the gate source voltage remains unchanged at V_{GS} = -3V in the case of normally-off GaN HEMT. From t_1 to t_2 the device is relaxed for a specific relax time. The dc voltage will then be connected again at t_2, (V_{DS} = 200V), and the double pulse signal is applied immediately.

	R_{DSON} after 1 s	R_{DSON} after 3 min	R_{DSON} after 60 min	off-state V_{DS} (V)
Normally-off HEMT	170 Ωm	192 Ωm	200 Ωm	200
Normally-on HEMT	238 Ωm	252 Ωm	265 Ωm	200
SJ-MOSFET	129 Ωm	129 Ωm	130 Ωm	200

Table 4.3 Dynamic R_{DSON} of the investigated transistors at different off-state times.

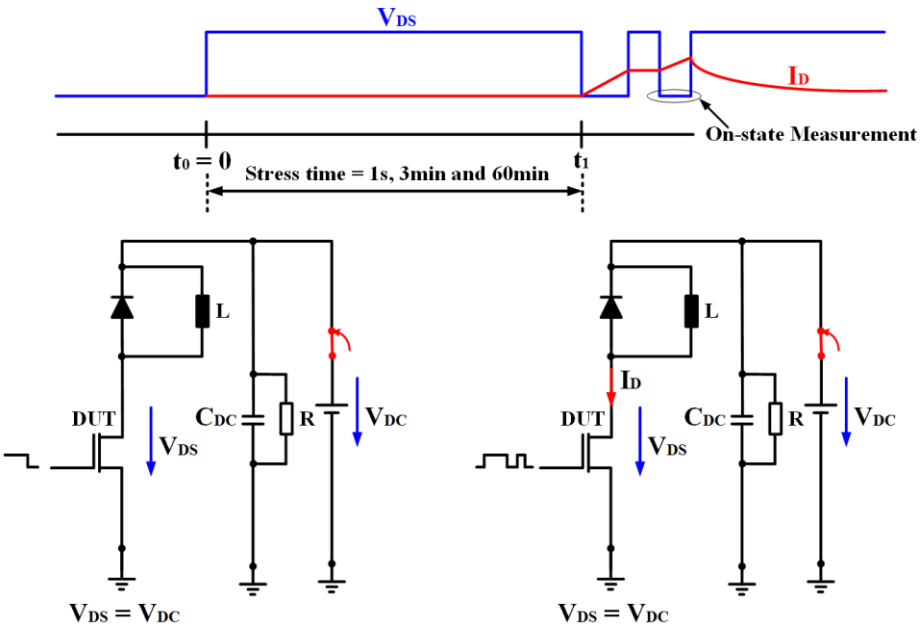


Fig. 4.21 Description of the first dynamic test to investigate the impact of different applied off-state time in the interval (t_0 - t_1) before switching on the device at t_1.

As a last step of the test, the dynamic on-state resistance R_{DSON} will be measured. The test steps will be repeated with changing the relax time for each new measurement from 3 seconds to 15 minutes. Fig. 4.24 and 4.25 present the results of the the first and second parts of the test. As is shown in Fig. 4.24a, R_{DSON} of the normally-off and normally-on GaN HEMTs is considerably higher than the static value and also increases as a function of the off-state stress up to 10 minutes. After that, the R_{DSON} seems to be saturated and reaches a constant value under the specified dynamic test conditions (I_D and V_{DS} transients). This constant value probably refers to the maximum number of the existing traps in the buffer and AlGaN layers or only to the maximum number of the electrons that can be captured at 200V off-state voltage. Mostly, the number of the existing traps is reasonably higher than the number of the

trapped electrons. However, the numbers of the existing traps and the captured electrons can be also equal under extreme thermal and electrical stress.

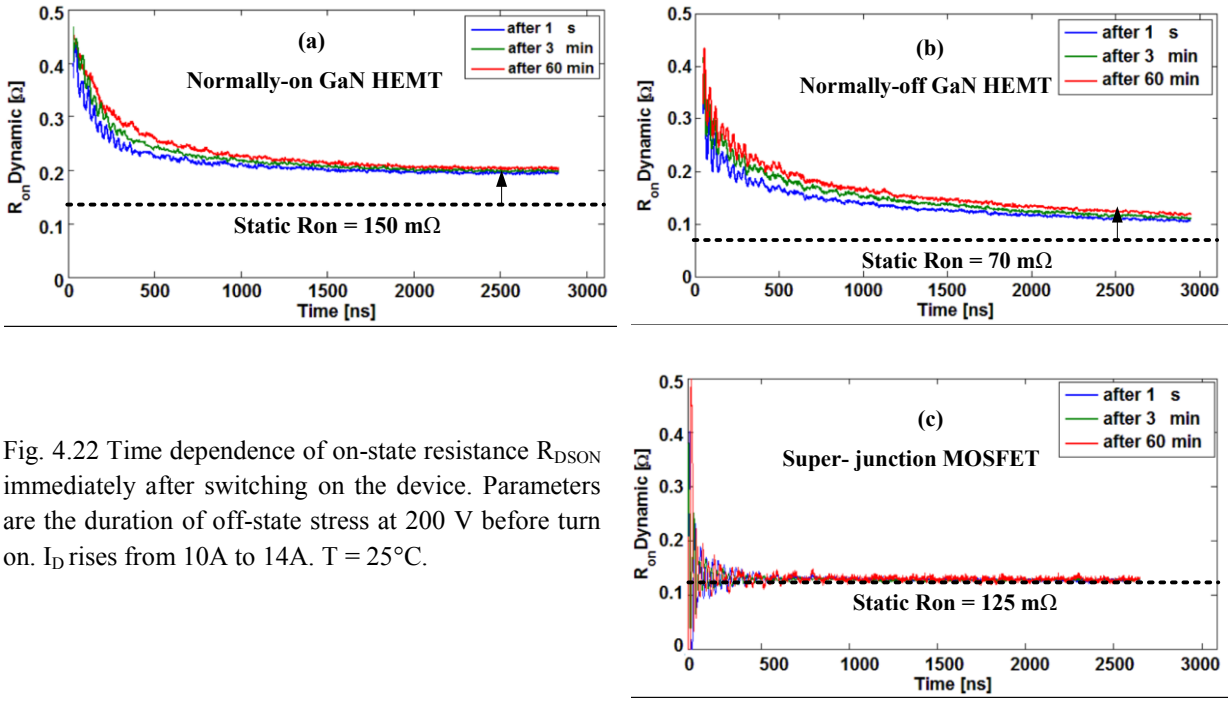


Fig. 4.22 Time dependence of on-state resistance R_{DSON} immediately after switching on the device. Parameters are the duration of off-state stress at 200 V before turn on. I_D rises from 10A to 14A. T = 25°C.

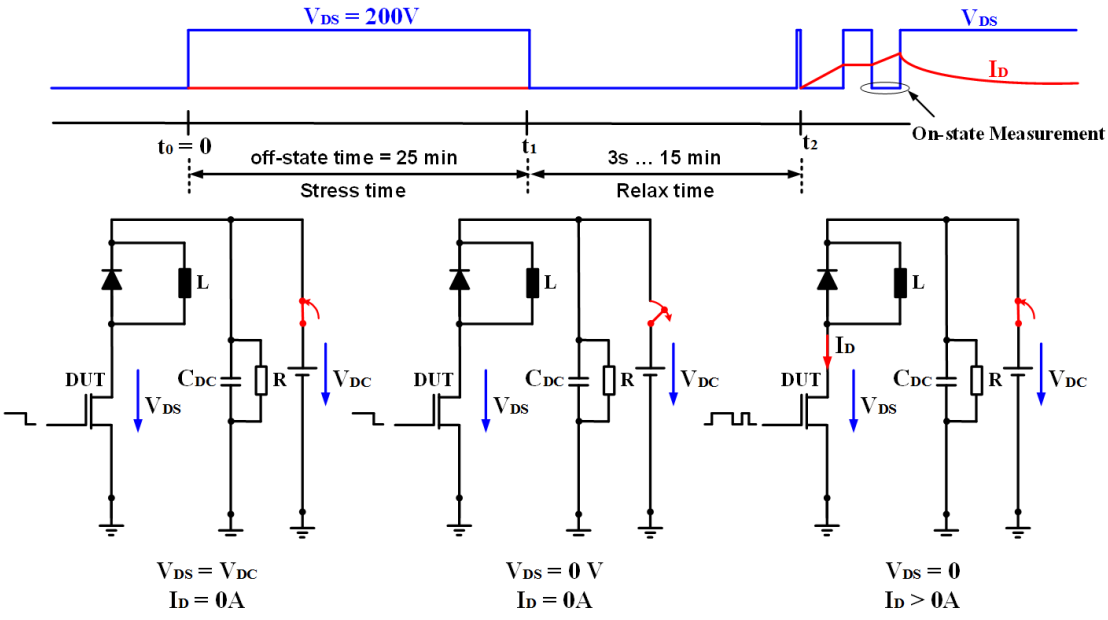


Fig. 4.23 Description of the second dynamic test to investigate the impact of applied off-state stress time (interval t_0 - t_1) with a relax time (interval t_1 - t_2) and before switching on the device at t_2.

In the second part of the test as shown in Fig. 4.24b, the maximum value of R_{DSON} is measured at the shortest relax time (1…3 seconds), and then starts to decrease by increasing the relax time. This is possibly caused by de-trapping mechanisms in both GaN HEMTs, in which more trapped electrons are increasingly released from the traps by increasing the relax time. After a relax time of approximately 7 minutes for the normally-off and 11 min for normally-on device, the R_{DSON} retains a constant value. Probably, most of the trapped electrons at the surface and bulk are released from the traps and become available again for conduction. The results achieved in both parts of the test show that the trapping phenomenon effect increases when the GaN HEMT is biased longer in the off-state at large drain voltage, whereas the de-trapping happens when the static stress conditions are eliminated and the device channel is relaxed. Finally, the normalized R_{DSON} has been evaluated and shown in Fig. 4.25. Following the electrical stress definition in 4.4.1, the stress produced in the GaN channel due to long-time off-state voltage contributed to the static stress, while the dynamic stress is caused by the high power transients during the double pulse test. Relating to the trapping effect, it can be acknowledged that the current collapse manifested in this test is not attributed to hot electron effect.

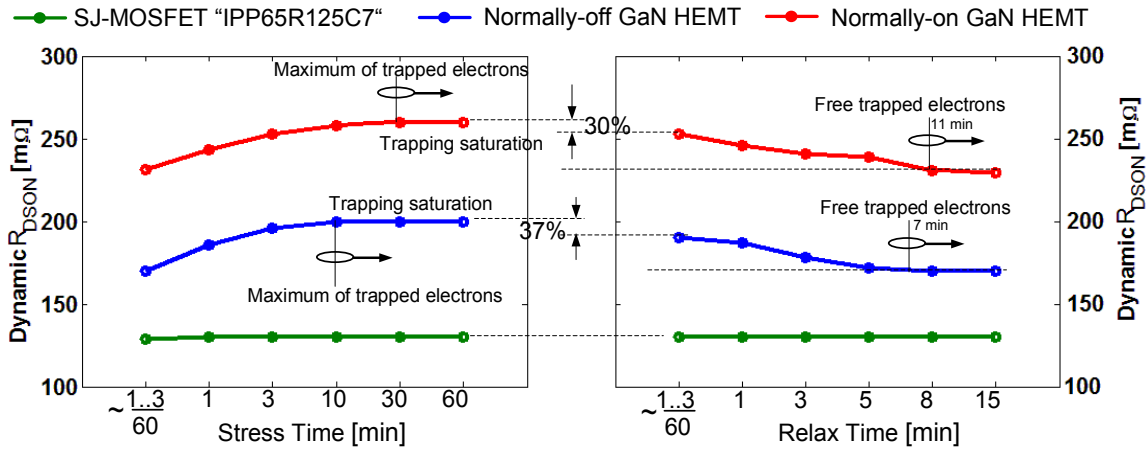


Fig. 4.24 Time dependence of on-state resistance R_{DSON} after switching on.

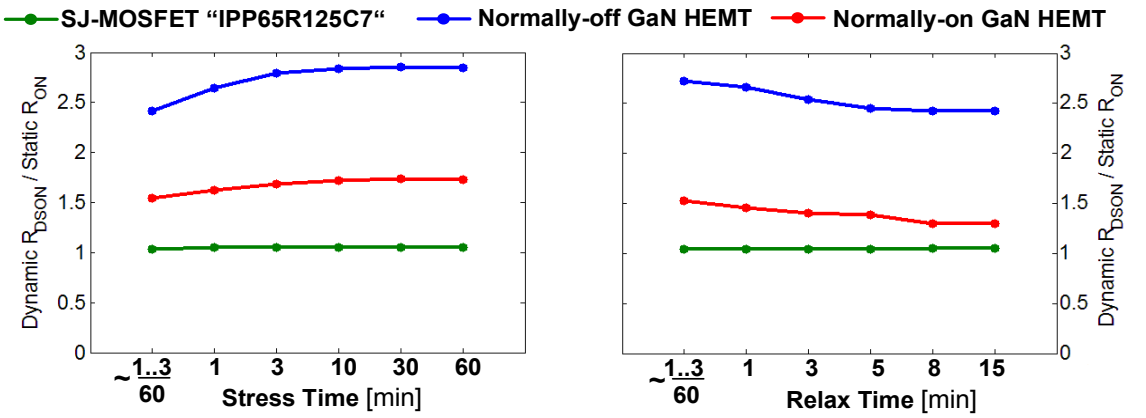


Fig. 4.25 Normalized R_{DSON} vs. stress and relax times after switching on.

4.4.3 Impact of Off-state Voltage at different Temperatures

In this experiment, the dynamic R_{DSON} transient is measured after applying different off-state drain voltages between 50 V and 300 V at 25° C and 150° C base-plate temperature. Fig. 4.26 shows exemplary transients for the normally-off GaN HEMT. For all analyzed time instants up to 3 µs, the dynamic R_{DSON} increases with off-state drain bias. Fig. 4.27 summarizes the dynamic R_{DSON} for all three investigated transistors at 500 ns and 2500 ns after switching. The increase of the dynamic R_{DSON} of the normally-off GaN HEMT is similar to the normally-on GaN HEMT. In contrast, the dynamic R_{DSON} of the SJ-MOSFET is independent of the off-state voltage. The small variations of less than 3% may correlate with the increase of the junction temperature. As in the first part of the dynamic test in section 4.4.2 and following the electrical stress definitions in 4.4.1, also in this test, the produced electrical stress on the GaN channel refers to the static stress that is caused by the high off-state voltage. However, the current collapse observed in this test also cannot be attributed to the hot-electron effect.

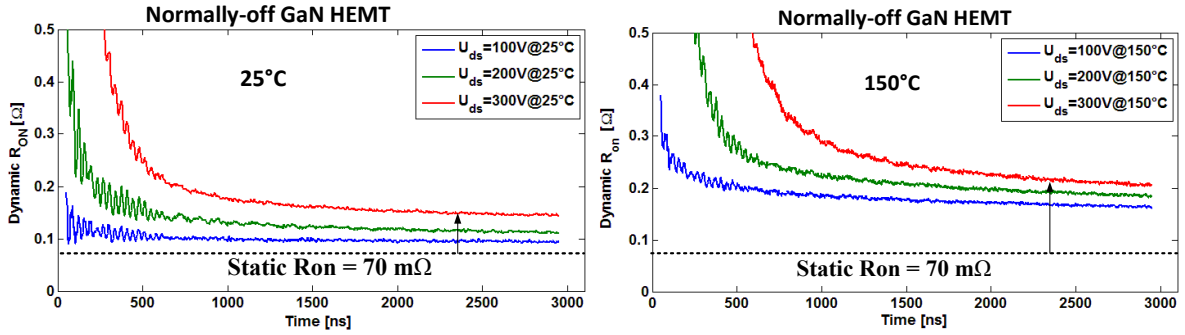


Fig. 4.26 Measured dynamic R_{DSON} transients of the investigated normally-off GaN HEMT directly after switching from different off-state drain voltages V_{DS} = 100 … 300 V. I_D increases from 10 A to 14 A in 3µs. Test temperature = 25° C and 150° C.

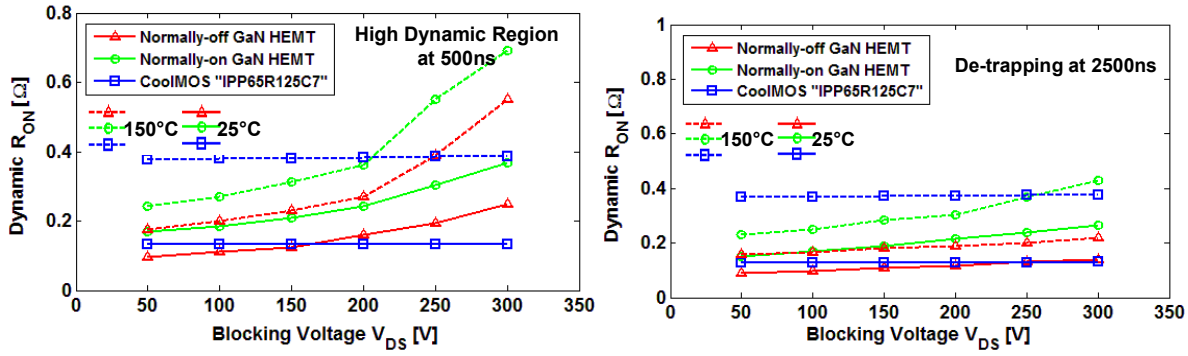


Fig. 4.27 Comparison of dynamic R_{DSON} of the investigated transistors: 0.5 µs and 2.5 µs after switching for different off-state drain voltages V_{DS} = 50 … 300 V. I_D increases from 10 A to 14 A in 3 µs. Test temperatures 25° C and 150° C

4.4.4 Impact of Drain Current at different Temperatures

In this test, the dynamic R_{DSON} transient is measured after applying different on-state drain currents between 5 A and 15 A after 300 V off-state bias and for 25° C and 150° C base-plate temperature. Fig. 4.28 shows some of the normally-off GaN HEMT transients. For all analyzed times up to 3 µs, the dynamic R_{DSON} increases with the drain current. Fig. 4.29 summarizes the dynamic R_{DSON} for all three investigated transistors at 500 ns and 2500 ns after switching. The increase of the dynamic R_{DSON} of the normally-off GaN HEMT is qualitatively similar to the normally-on GaN HEMT. For the normally-on device, however, the tests were performed on a relatively higher current level with respect to the maximum pulse current (Fig. 3.10). From the presented results in Fig. 4.29, it is easy to understand how far the trapping phenomenon is affecting the device performance. It is observable that the increase of the drain current is also playing a signifcant role in the R_{DSON} degradation at constant off-state voltage. In general, the reason for R_{DSON} degradation and the trapping effects observed in the dynamic test with double pulse or small number of pulses contributes to the low dynamic stress. However, it is difficult in this test to clearly consider what type of trapping is the chief cause of the degradation of the R_{DSON}. This is due to the applied test conditions. The test was conducted for double pulse. That means the number of the transient is only two. This is typically enough reason for the large number of the electrons to become trapped. The high off-state voltage in parallel with the high drain current in the GaN channel can constitute a crucial reason for the emergence of the hot electron injection phenomena during the transient and at high dynamic stress area.

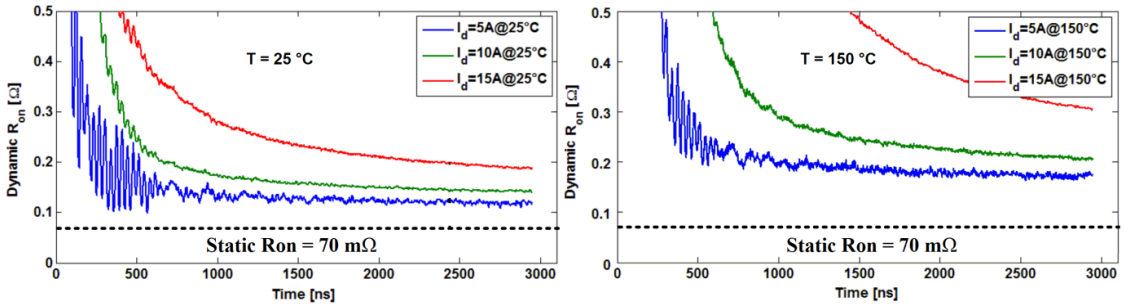


Fig. 4.28 Measured dynamic R_{DSON} transients of the investigated normally-off GaN HEMT directly after switching at constant V_{DS} = 300 V for different I_D = 5 A to 15 A in 3 µs. Test temperature = 25° C and 150° C.

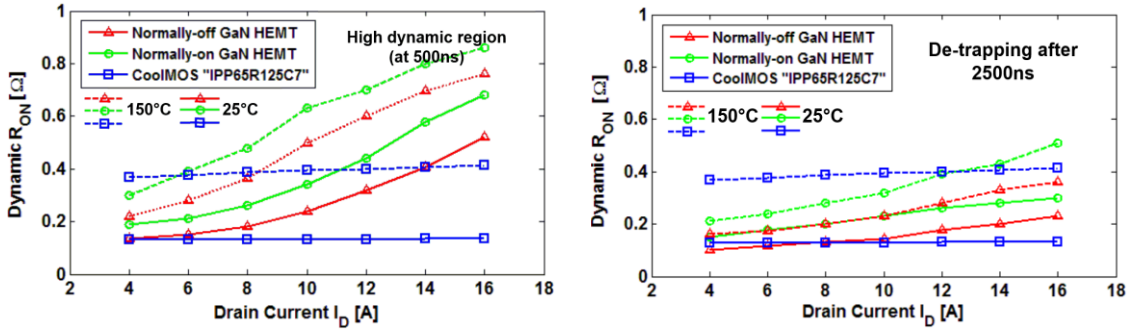


Fig. 4.29 Comparison of dynamic R_{DSON} of the investigated transistors, at 500ns (a) and 2500ns (b) after the switching-off (t_2). Off-state voltage is constant V_{DS} = 300 V for different drain currents I_D = 4A …16A. Case temperature T = 25°C and 150°C.

4.4.5 Impact of Different Switching Frequencies

To investigate the current collapse phenomena in GaN HEMTs, all devices are switched by applying a pulsed gate signal for 1 ms at different switching frequencies varying from 50 kHz to 400 kHz. The gate pulse signal has a 50% duty cycle. Fig. 4.30 shows the measured waveforms at V_{DS} = 200 V and I_D = 2.15 A for the normally-off GaN HEMT, indicating the measured variables. Two values for the on-state voltage V_{DSON} are defined, the first one is $V_{DSON,initial}$ which is measured at the beginning of the signal, when the drain current reaches 2.15 A. The second value is $V_{DSON,stress}$, which is equal to the on-state voltage after 1 ms signal duration.

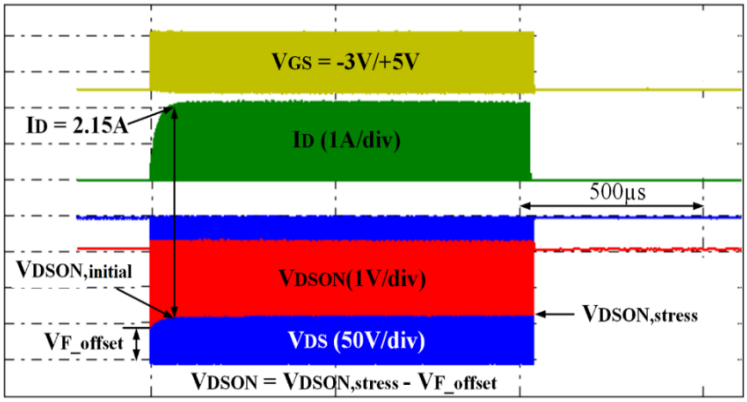


Fig. 4.30 Voltage and current for 200V/2.15A switching operation of the normally-off GaN HEMT at 400 kHz and 1 ms duration.

Fig. 4.31 depicts the measured on-state voltage V_{DSON} for the 600V normally-off GaN HEMT. The measured values of $V_{DSON,initial}$ and $V_{DSON,stress}$ at different switching frequencies varying from 50kHz to 400kHz are summarized in Table 4.4. It is easy to observe, that the increase of the switching frequency provokes an increase of on-state resistance, which is probably related to the increase of the trapped electrons.

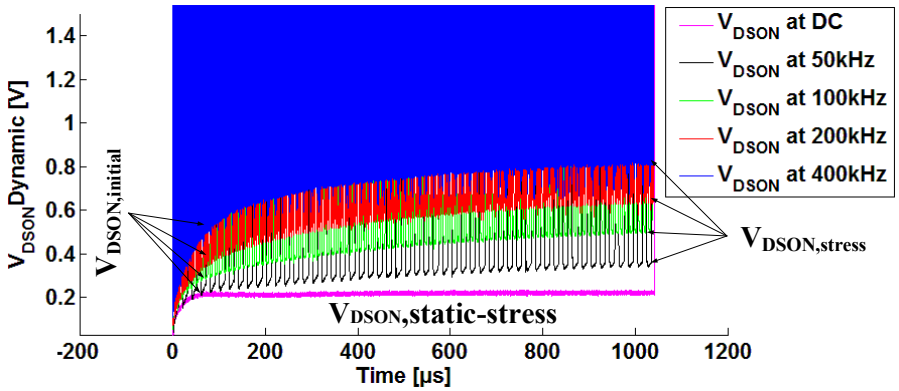


Fig. 4.31Comparison of the dynamic on-state resistance of 600V normally-off and GaN HEMT measured at drain source voltage V_{DS} = 200 V and drain current I_D = 2.15 A. Switching frequency is varying from 50 kHz to 400 kHz.

In these experiments, two time constants related to the trapping and de-trapping mechanism are defined. These are the trapping and de-trapping time constants (T_{trap} and $T_{de\text{-}trap}$). The exact timing of the trapping and de-trapping mechanisms remains unknown and can be overlapped between different trapped electrons. It is expected, however, that most of the hot electrons are trapped at high dynamic stress as depicted in Fig. 4.32.

Switching Frequency	50 kHz	100 kHz	200 kHz	400 kHz
$V_{DSON,initial}$	240 mV	310 mV	400 mV	550 mV
$V_{DSON,stress}$	335 mV	405 mV	590 mV	760 mV

Table 4.4 Measured $V_{DSON,initial}$ and $V_{DSON,stress}$ of the 600V normally-off GaN HEMT (1st development) at different switching frequencies varying from 50kHz to 400 kHz.

This is exactly what occurs during and after the turn-on transient, where the free electrons moving in 2DEG will be kidnapped in GaN buffer and AlGaN barrier. This interval begins from the interacted current and voltage transients, in which the trapping effect is maximum, until 100s of nanoseconds and it may be different between one trapped electron and another. Following that, the dynamic stress begins to decrease, where the de-trapping mechanism starts in parallel to the device relaxation. The time from the point where the hot electron is trapped until it is released is referred to as the *de-trapping* time or the *emission* time. Essentially, trapped electrons bear a different de-trapping time constant. This is due to the energy difference between the traps.

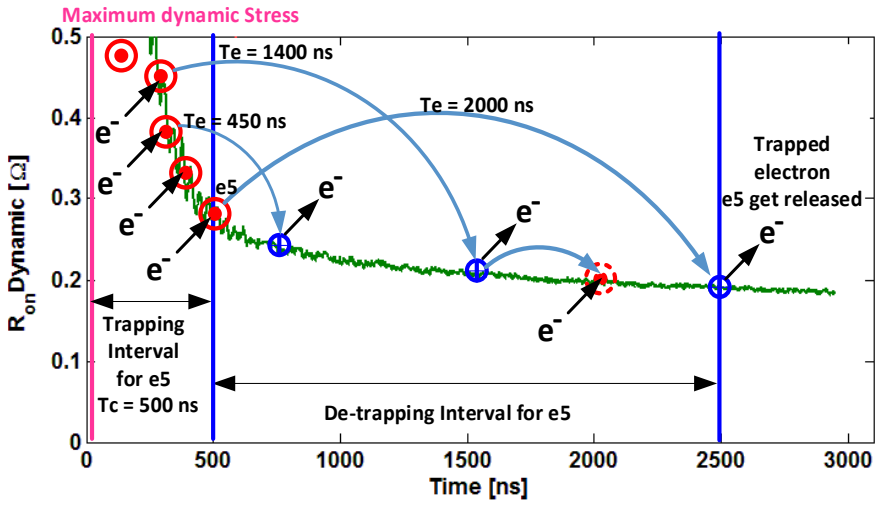


Fig. 4.32 Interpretation of the trapping mechanism at high dynamic stress

A specific point or interval between the trapping and de-trapping mechanisms is unknown and floating depending on the number of traps and the energy of the traps in GaN HEMT. Also, it is important to distinguish between the de-trapping mechanism and the device relaxation term. Since the de-trapping mechanism depends on the long-time constant of the trap which can be 10s, 100s of micro or milliseconds, the trapped electrons remain in the traps and cannot follow the high frequency signal until the

time constant expires, and then the electrons can break free from traps. The de-trapping mechanism is continually happening in the interval between the turn-on transient and the low dynamic stress area, even at the high dynamic stress area, this essentially depend on the long-time constant of the trap. Whereas the device relaxation basically describes the status of device after removing the source of the electrical stress until the steady state is reached. This typically happens after the device operation when the applied off-state voltage V_{DS} is removed. However, even during the operation if the on-state time is long enough, which is usually the case at low switching frequency. As mentioned above, the energy of each trap (defect) is the main factor that decides how long the electron will remain in the trap. Following the first turn-on transient, the number of electrons that become trapped at 50 kHz and 400 kHz should be equal. The number of pulses at 400 kHz is 8 times higher than at 50 kHz, however. Thus, the expected number of the trapped electrons should be higher after each additional pulse. The hot electrons probably fill the traps until most of the existing empty traps are filled and the GaN channel gets a kind of trapping saturation. After the turn-on transients, the dynamic stress on GaN channel begins to decrease and most of the trapped electrons with short time constant are released from the traps. At the high frequency signal as in the case of 400 kHz, however, the on-state time is almost 2.5 µs, while it is 20 µs at 50 kHz. The trapped electrons with a long-time constant will obviously remain in the traps longer, while the relaxation of the device is not long enough at 400 kHz compared to 50 kHz. As a consequence, the trapped electrons at 400 kHz are accumulated after each turn-on transient. This the main reason for the observable increase of the on-state resistance R_{DSON}.

Switching Frequency	50 kHz	100 kHz	200 kHz	400 kHz
$V_{DSON,initial}$	225 mV	236 mV	250 mV	280 mV
$V_{DSON,stress}$	247 mV	280 mV	302 mV	335 mV

Table 4.5 Measured $V_{DSON,initial}$ and $V_{DSON,stress}$ of the 600V normally-off GaN HEMT (2nd development) at different switching frequencies varying from 50kHz to 400 kHz.

Fig. 4.33 shows the measured on-state voltage V_{DSON} for the investigated power transistors. The measured $V_{DSON,initial}$ and $V_{DSON,stress}$ (Fig. 4.33a) of an improved development of the 600V normally-off transistor at different switching frequency varying from 50kHz to 400 kHz are summarized in Table 4.5. The $V_{DSON,DC\text{-}stress}$ is the static on-state voltage encountered during switching-on the transistor continuously with a drain current $I_D = 2.15A$ after applying an off-state drain voltage of $V_{DS} = 200V$. A higher switching frequency and a longer pulse-duration will result in an increase of the on-state resistance. After 1 ms switching at 400kHz, R_{DSON} is 30-40% higher as compared to switching at 50kHz for both GaN devices (Fig. 4.34). It is already known from double-pulse experiments with pulses in the microsecond-regime that GaN-based switches often suffer from an increased dynamic on-state resistance R_{DSON}. However, the increase of the R_{DSON} due to device heating is negligible in such experiments. Device heating may additionally contribute to the R_{DSON} increase shown in Fig. 4.33a and Fig. 4.33b for normally-off and normally-on GaN HEMTs, respectively. However, the measured conduction losses from both GaN transistors result in a power dissipation < 0.5W, which cannot be a reason for any significant increase of the temperature in order to explain the increased R_{DSON} (Fig. 4.34a) at different switching frequency. Also no indications for an increased R_{DSON} due to heating were seen when using the SJ-MOSFET as switch (Fig. 4.33c). As discussed before, cumulative trapping from hot channel electrons during the switching events in the GaN devices has to be considered [105].

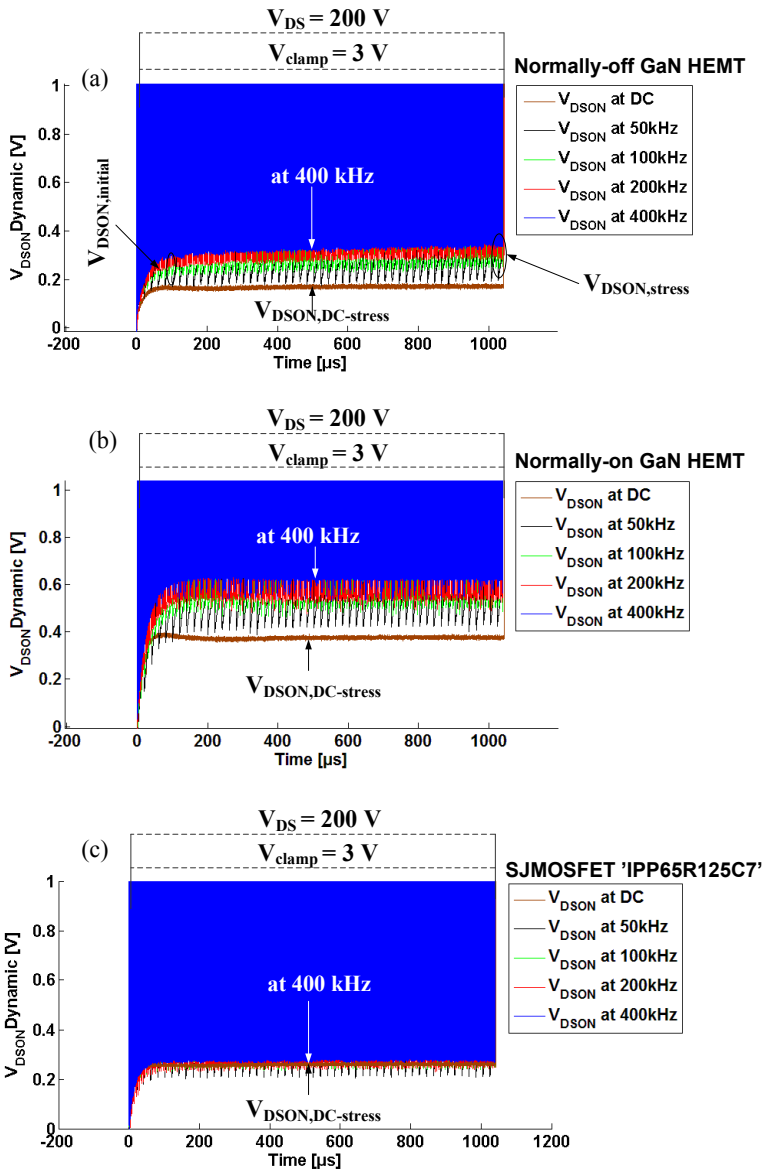


Fig. 4.33 Comparison of dynamic on-state voltage for the investigated transistors (a) normally-off and (b) normally-on GaN HEMTs and (c) SJ-MOSFET 'IPP65R125C7' measured at drain source voltage V_{DS} = 200 V and drain current I_D = 2.15 A. Switching frequency f_{SW} varying from 50 kHz to 400 kHz.

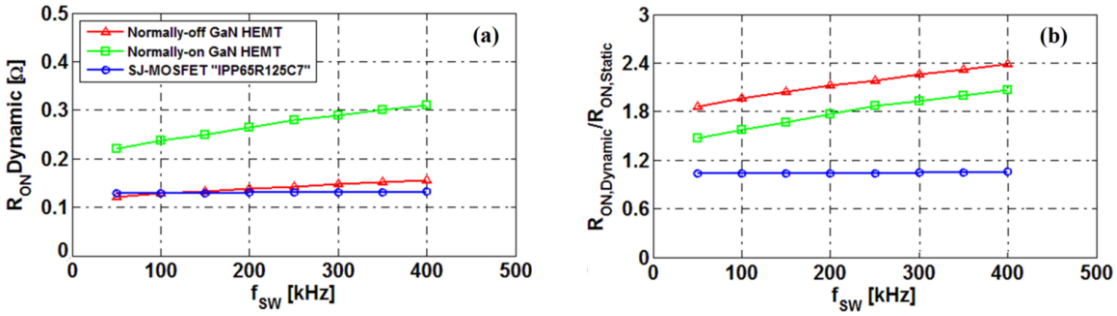


Fig. 4.34 Comparison of dynamic on-state voltage for the investigated transistors normally-off and normally-on GaN HEMTs and CoolMOS transistor 'IPP65R125C7' measured at drain source voltage V_{DS} = 200V and drain current I_D = 2.15 A. Switching frequency f_{SW} varying from 50 kHz to 400 kHz.

4.4.6 Impact of Different Switching Speeds

This test investigates the device degradations and the current collapse phenomena in GaN HEMTs according to the impact of the switching speed. All devices are switched by the application of a pulsed gate signal for 1ms at different switching frequencies up to 200kHz. The gate pulse signal possesses a 50% duty cycle. For each switching frequency the test was repeated four times with different gate resistances (4.7, 10, 20 and 30 Ω). Fig. 4.35 demonstrates the measured waveforms of the normally-off GaN HEMT at V_{DS} = 200V and I_D = 6A. In this experiment, the R_{DSON} value of interest is measured at 500 ns after the transients. As known and expected, the increase of the switching speed implies the reduction of the switching losses. At this point, the measured power switching losses for normally-off GaN HEMT at Rg = 30Ω compared to Rg = 4.7Ω are higher by 2.5 times at turn-off and 8 times at turn-on.

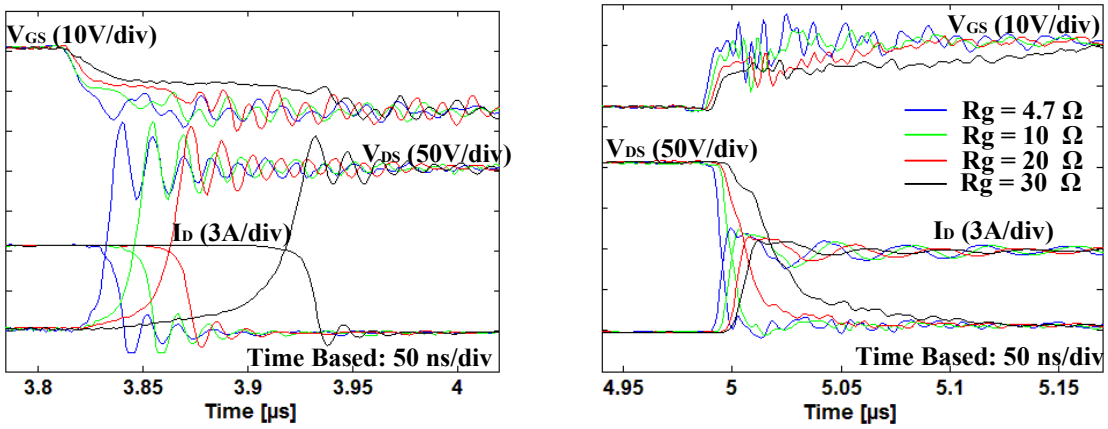


Fig. 4.35 Measured transients of the normally-off GaN HEMT at different switching speeds; V_{DS}=200V, I_D=6A. Gate resistance Rg = 4.7, 10, 20 and 30 Ω. T= 25°C. R_{DSON} values are measured at 500 ns after the transients.

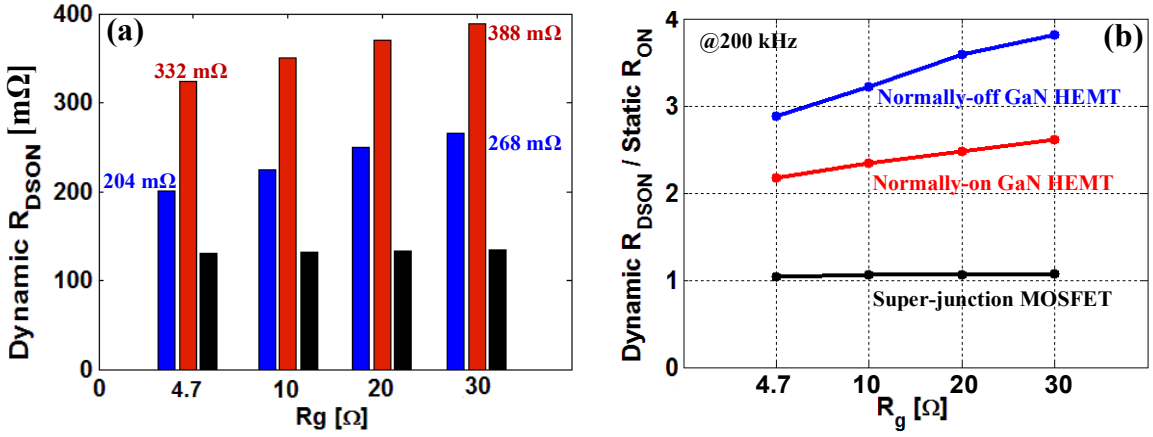


Fig. 4.36 Comparison of dynamic on-state resistance R_{DSON} for the investigated transistors measured at drain source voltage V_{DS} = 200 V and drain current I_D = 6 A. Switching frequency = 200 kHz. Gate resistance Rg = 4.7, 10, 20 and 30 Ω. R_{DSON} values are measured at 500ns after transients.

It is obvious that the thermal stress on the GaN HEMT channel becomes higher by using a higher gate resistance. However, by observing this increase of the dynamic on-state resistance for both GaN devices compared to the SJ-MOSFET by the gate resistance from 4.7Ω to 30Ω as depicted in Fig. 4.36 (R_{DSON} values are given at 500 ns after the transients), it is hard to believe that the increase in R_{DSON} is due to increase of the thermal stress in the channel during an interval of 20ms. Obviously, the device degradation and current collapse phenomena in GaN HEMTs are strongly present by driving GaN HEMT at different switching speeds. This is probably due to the increase of the hot electron injections during longtime interaction of the current and voltage transients. In conclusion, the main results of the different tests employed to investigate the on-state resistance according to the possible reason of the R_{DSON} degradation are summarized below in the Table 4.6.

Test	Impacts	R_{DSON}	Possible Reasons for R_{DSON} Degradation
Dynamic Test_1a Section (4.4.2)	Increasing the stress time of the off-state voltage before switching the DUT on	Increase	Current collapse: Trapping at the buffer layer and the surface because of the high off-state voltage. R_{DSON} increases as the off-state time increase
Dynamic Test_2 Section (4.4.3)	Increasing the relax time after switching the DUT off at the second pulse.	Decrease	De-trapping: Trapped electrons are released from traps located in the bulk and surface because of the increase of the relax time.
Dynamic Test_3 Section (4.4.4)	Increase of the blocking voltage V_{DS} at different temperatures	Increase	Current collapse: Trapping at the buffer layer and the surface because of the high off-state voltage. A hot electron phenomenon is not expected.
Dynamic Test_4 Section (4.4.5)	Increase of drain current Id at different temperatures	Increase	Current collapse: Trapping at the buffer layer and the surface because of the high off-state voltage. Hot Electron Injection can be expected
Dynamic Test #5 Section (4.4.6)	Increase of switching frequencies	Increase	Hot Electron Injection in GaN buffer layer and AlGaN barrier layer because of the increase of the number of the transients and trapping because of the high off-state voltage at the bulk and surface.
Dynamic Test #6 Section (4.4.7)	Increase of switching speeds	Decrease	Trapping caused by the hot electron injection in GaN buffer and AlGaN barrier because of the increase of the interaction time of the current and voltage transients in the GaN channel at slower switching speed and trapping effect because of the high off-state voltage at both bulk and surface.

Table 4.6 Possible reasons for the R_{DSON} degradation

5 Characterization of GaN Schottky Diode

Gallium Nitride (GaN) and Silicon Carbide (SiC) both allow for the realization of Schottky diodes for higher blocking voltages. SiC Schottky diodes can be obtained from different manufacturers, and are used in several applications such as fast switching, low loss power devices. GaN Schottky diodes, by contrast, represent an emerging class, while the GaN-based power semiconductors generally are competing with SiC semiconductors especially for use at lower power, high frequency applications. This chapter presents the experimental investigations of the static and dynamic characteristics of new 600V GaN Schottky diodes and compares them with the state-of-the-art SiC Schottky diode. Furthermore, both of these diodes are operated as freewheeling diodes in a buck converter in eight different device combinations, consisting of both diodes and four other 600 V power transistors based on Si, SiC and GaN. Depending on which transistor was used in the circuit, the switching performance of the diode can be affected considerably. Both diodes reveal good switching performance, similar damping coefficients during the transients and approximately similar reverse recovery behavior. Nevertheless, the investigated GaN diodes are characterized by a higher forward voltage drop compared to the SiC diodes.

5.1 Introduction

As the development of GaN-based power transistors in recent years has increased significantly, GaN Schottky diodes have also made their way into the power electronics market. Manufacturers such as International Rectifier have developed GaN Schottky diodes for 600V-applications. Typically, power MOSFETs with integrated body diodes in silicon (Si) technology have been employed in power converters, preferably in high-frequency applications and for voltages up to 600V [106]. A substantial part of the overall losses of Si-based power converters are the reverse-recovery switching losses of Si diodes [107]. The reverse recovery of Si diodes affects the transistor and causes additional turn-on losses, leading to a substantial amount of noise (EMI) in the power circuit [108].

Because a Schottky diode (Schottky Barrier Diode - SBD) is a majority carrier device and has no stored minority carriers that have to be injected into the device during turn-on and pulled out during turn-off, it is able to switch faster than a Si-pn junction diode [110]. Only the charging of the junction capacitance is obvious during transient operation. Thus, substantially lower switching losses than those found in comparable Si power diodes can be accomplished [111]. Therefore, compared to Si diodes, GaN and SiC Schottky diodes are almost characterized by zero-reverse recovery current that enhances the efficiency of the power converter because of the reduced switching losses during turn-on. This is the reason why the use of minority carrier devices, such as GaN and SiC Schottky diodes are always suggested for the design of high-frequency power converters. Nonetheless, the use of GaN and SiC power devices (characterized by very fast *di/dt*) in the power converter will also have numerous problems related to the parasitic influence on the device performance. Experimentally, the very fast transients of GaN and SiC Schottky diodes combined with the parasitic elements can lead to unacceptable high frequency oscillations that might substantially impair the system operation. Typically, there is a compromise between high efficiency and low EMI emission. The first part of this chapter

presents the measured characteristics of a (600V/2A) GaN Schottky diode and compares it to a state-of-the-art SiC Schottky diode and a soft recovery p-n diode. All devices are tested at different junction temperatures. The second part of this chapter presents a higher rated (600V/8A) GaN Schottky diode feasible for high frequency operation. Static and dynamic characteristics of the diodes are evaluated at different temperatures and compared to commercially available SiC Schottky diode. The SiC diodes are available from CREE, while GaN diodes were developed at Ferdinand Braun Institut Berlin (FBH). The test for both diodes was carried out under identical conditions. Table 5.1 summarizes the parameters of the investigated diodes.

Device	Type. Nr	(Vds/Id@100°C)	Supplier
GaN Schottky diode	Developed by FBH [21]	600V/2A	FBH Berlin
GaN Schottky diode	Developed by FBH [109]	600V/8A	FBH Berlin
Soft-recovery *pn* diode	FR207 [137]	600V/2A	FIARCHILD
SiC Schottky diode	C3D0260A, [112]	600V/2A	CREE
SiC Schottky diode	C3D08065A, [113]	650V/8A	CREE

Table 5.1 Parameters of the investigated 600V diodes.

The 600V/8A GaN and SiC Schottky diodes are operated as freewheeling diodes in a buck converter in eight different device combinations. These combinations consist of both diodes and four other 600V power transistors based on Si, SiC and GaN. The dynamic effects of the transistor on the diode and vice versa are investigated for each combination. Depending on the used transistor, the switching performance of the diode can be significantly limited. In general, both diodes show a good switching performance, similar damping coefficients during the transients and approximately similar reverse recovery behavior. However, the investigated GaN diode is characterized by a higher forward voltage drop than the SiC diode.

5.2 Structure of GaN Schottky Diode

Both GaN Schottky diodes presented in this thesis have the same technology. The diodes are manufactured on GaN-based epitaxial layers grown by MOVPE on 3” *n*-SiC wafer [21][109]. Ti/Al/Mo/Au based cathode ohmic contacts were evaporated and annealed at 830 °C.

Parameters	600V GaN SBD [21]
Buffer	GaN:C 3.1 µm carbon doped
Barrier layer	26 nm Al0.25Ga0.75N
UID GaN channel	40 nm
TLM structure	~475 Ω/□
Passivation layer	150 nm SiN_x
Device Width	25 mm
Anode-cathode Distance	15 µm
Field Plate	1 µm
Substrate	3” n-SiC

Table 5.2 Physical parameters of the FBH’s 600V GaN Schottky diode [21][109].

Table 5.2 provides a summary of the parameters and features of the investigated 600 V GaN Schottky. A cross sectional illustration of the devices and the A190 microwave packages is shown in Fig. 5.1. More details on the specific GaN Schottky diode technology are published in [21][109].

(a) (b)

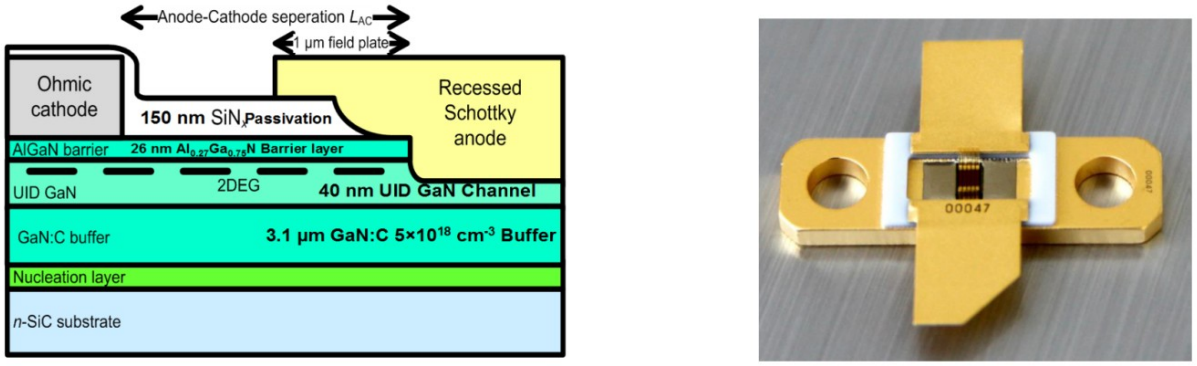


Fig. 5.1 (a) Schematic cross-sectional illustration of the GaN Diode device [21][109]. (b) A190 Microwave package for the FBH's 600V GaN Schottky diode.

5.3 Static Characteristics

In this section, the static characteristics of the investigated 600V GaN and SiC Schottky diodes are presented. Both quantities are measured at heat-sink temperatures ranging from 25° C to 175° C. Fig. 5.2 depicts the schematic of the test circuit used for the static characterization. The circuit is supplied from low voltage V_{DC} = 40V and controlled by a single pulse gate-source voltage. The single-pulse control is set to 1µs duration in order to avoid any increase of the junction temperature, while the forward current I_F and the forward voltage V_F are measured.

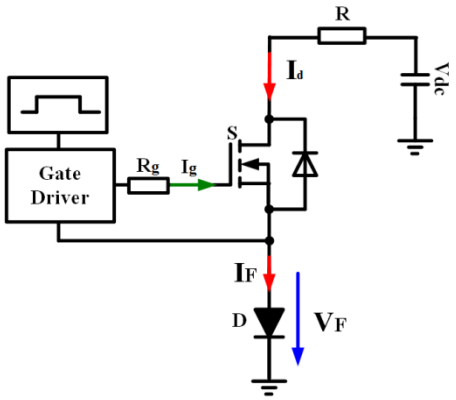


Fig. 5.2 Static test circuit.

Fig. 5.3 shows the resulting *I-V* forward characteristics of the GaN Schottky diode. It is clearly visible that the on-state resistance in forward direction increases approximately linear with the temperature; this effect is more pronounced than in SiC Schottky diodes. The reverse current is also sensitive to

elevated temperatures: it increases by two orders of magnitude between 25° C and 175° C. For a width *W*=25 mm, the reverse current ranges from approx. 10 µA, which is comparable to the SiC diode [71] up to several 100 µA at high temperatures.

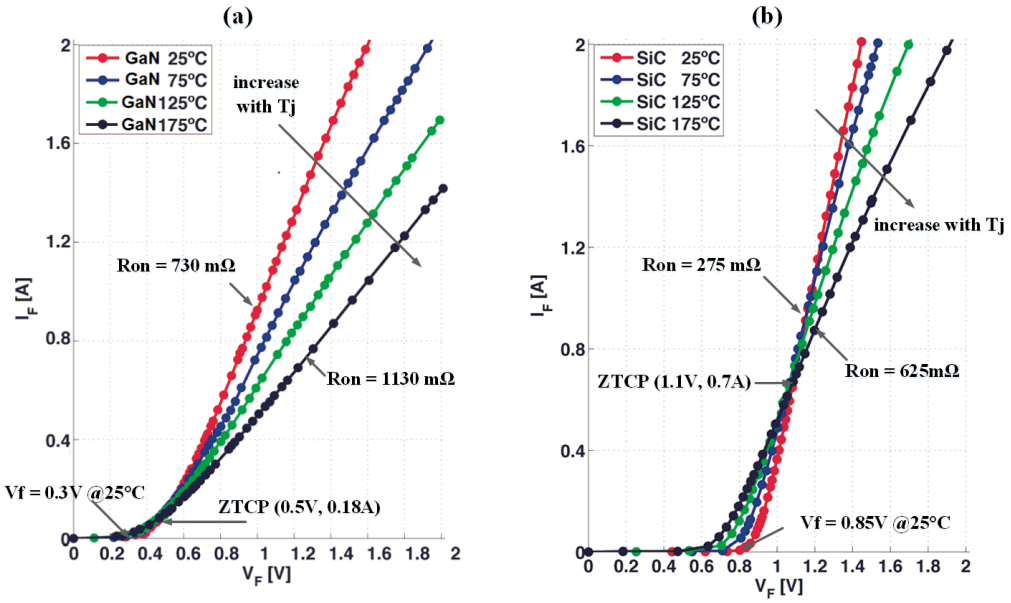


Fig. 5.3 Temperature-dependent I-V forward characteristics of the investigated 600 V/2 A (a) GaN SBD [63] and (b) SiC SBD [112].

Forward characteristics of 600V/8A GaN and SiC Schottky diodes are measured at different base-plate temperatures varying from 25° C to 200° C. As seen in Fig. 5.4a and Fig. 5.4b, above approximately 2A, both GaN and SiC diodes are characterized by positive temperature coefficients. While the increase of the on-state resistance Ron of the GaN diode is approximately constant for each 25°C increment, the SiC diode behaves quite differently (Fig. 5.4b). This is probably due to the difference between the two devices in terms of thermal conductivity. As a result of the low on-state resistance and high thermal conductivity of the SiC device, the zero temperature current point (ZTCP) is marginally higher compared to the GaN diode as given below in Fig. 5.4a and Fig. 5.4b.

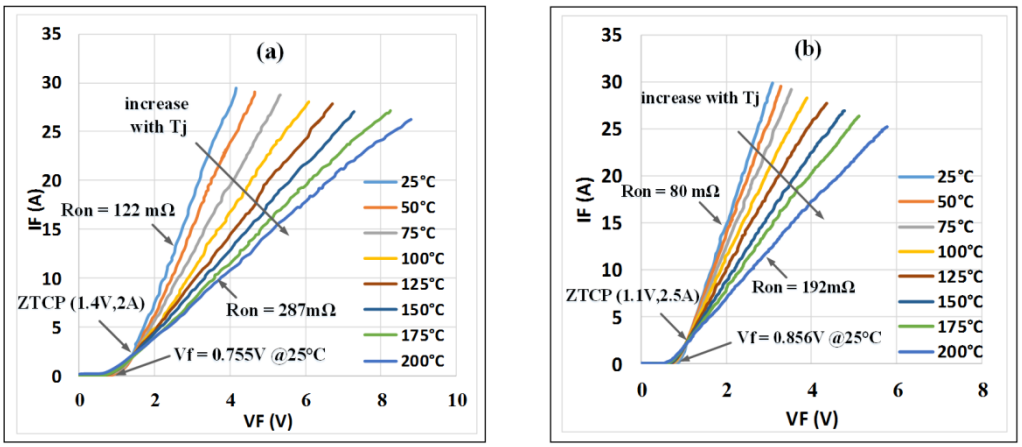


Fig. 5.4 Temperature-dependent I-V forward characteristics of the investigated 600V/8A GaN SBD [21][109] and 600V/8A SiC SBD [113].

5.4 Switching Characteristics

The switching characteristics of 600V/2A and 600V/8A GaN Schottky diodes are investigated and compared to commercially available state-of-the-art SiC Schottky diodes from CREE. The investigated GaN Schottky diodes are tested under typical hard switching conditions, applying the dynamic test circuit depicted in chapter 2. The circuit consists of a buck converter with inductive load, gate driver and measurement equipment.

5.4.1 600V/2A GaN and SiC Schottky Diodes

Since no matching GaN or SiC power transistor (2A rated current) was available in 2012, experiments were conducted with a commercial SiC MOSFET from Cree (CMF10120) as active switch, also a new 400V/12A normally-on GaN HEMT (section 3.3.1) from Ferdinand-Braun-Institute, Berlin [61][62] has been used in the switching test. The devices operate at 300 Vdc and switch a current of 2A. The entire set of measurements presented in this subsection is based on double-pulse signal with 50% duty cycle Fig. 5.5 and Fig. 5.6 show the measured waveforms of the GaN diode using the SiC MOSFET (CMF10120). The chip temperature is varied from 25° C up to 175° C. During the turn-off process, the peak reverse current as well as the current-time integral (the total capacitive charge Q_{rr}) are independent of the temperature. From the turn-on measurements, two parasitic effects can be observed: a slight rise of the current during the fall of the blocking voltage due to internal capacitances, and a high frequency ringing of the current. The selected SiC MOSFET is a relatively large transistor (1200V/20A) with a long discharging time of the drain source capacitance C_{DS}.

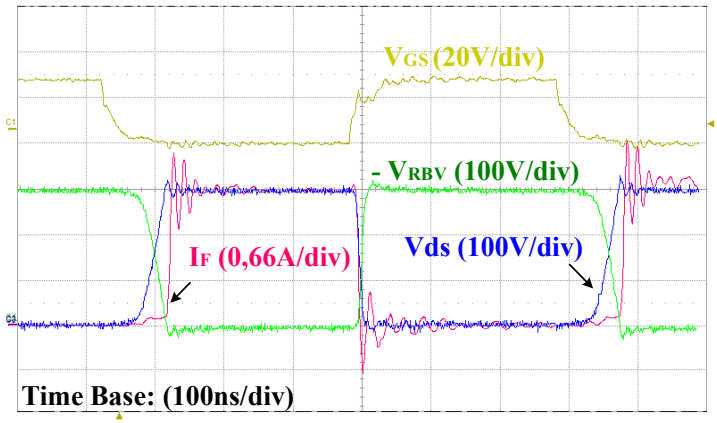


Fig. 5.5 Double-pulse waveforms of GaN Schottky Diode

This is reflected in the falling time of the diode voltage V_{RBV} which is measured to t_f =35 ns starting from the off-state to on-state resulting in a *dv/dt* of 8.7 kV/µs. An improvement can be achieved by applying a comparable GaN HEMT as active switch in the dynamic test as described in Fig. 5.7. Using a normally-on GaN HEMT, the measured falling time of the voltage is only 9 ns, resulting in a dv/dt of 28 kV/µs. The experimental results for the proposed GaN HEMT and GaN SBD test combination are given in Fig. 5.8 generally showing a good switching performance comparable to the performance of state-of-the-art SiC SBD.

From the results in Fig. 5.7 and Fig. 5.8, it is remarkable that the transients are different in form and speed during the turn-on, while they are approximately similar during the turn-off. In order to examine the thermal effects on the switching performance, the switching waveforms are measured at different temperatures varying from 25° C to 175° C, they are demonstrated in Fig. 5.9. The dynamic characteristics of the investigated GaN SBD and the SiC Schottky diode (C3D02060A) are compared.

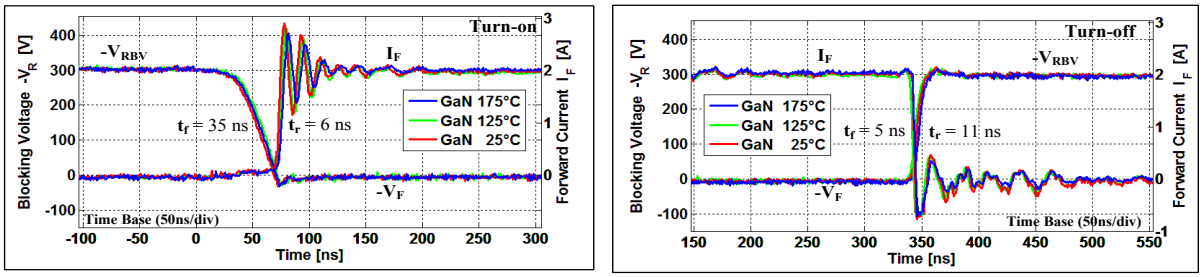


Fig. 5.6 GaN SBD measurement results using a SiC MOSFET (CMF10120) at different temperatures. Reverse blocking voltage V_{RBV} = 300 V and forward current I_F = 2 A.

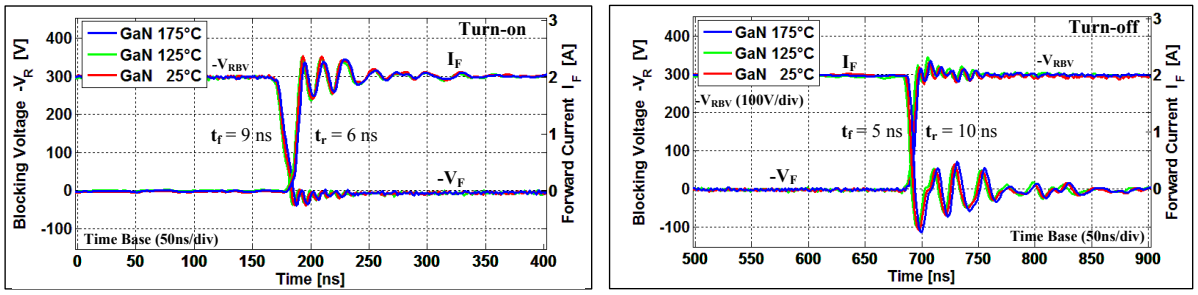


Fig. 5.7 GaN SBD measurement results using a 400V/12A normally-on GaN HEMT at different temperatures. Reverse blocking voltage V_{RBV} = 300V and forward current I_F = 2A.

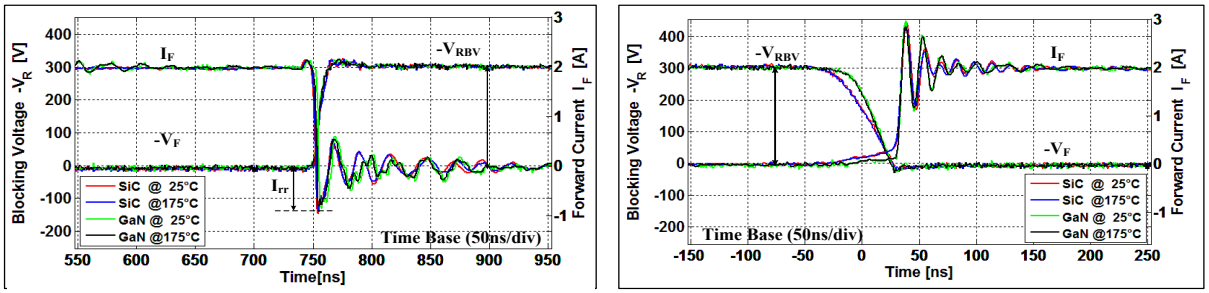


Fig. 5.8 Reverse current Comparison of GaN and SiC diodes during turn-off; reverse blocking voltage V_{RBV} = 300 V and forward current I_F = 2 A. Right: Turn-on comparison.

One problem arises in the comparison due to the available packaging of the devices: the SiC diode is assembled in TO220 housing whereas the GaN device is packaged in microwave housing A190. Therefore, the circuit layout cannot be identical, and stray inductances in the commutation loop differ slightly. When analyzing the turn-off curves, one can state that the two devices reveal a very similar behavior.

Both diodes demonstrate the same stability with the operating temperature. In other words, the reverse current peak and its duration do not change substantially with the temperature, and they have the same reverse current area, and thus the same capacitive charge, which is calculated using the measurements. The results are presented in Table 5.3. Following the definitions for pn-diodes, the charges are denoted Q_{rr} for the total charge and Q_s and Q_f for the partial charges. Because SiC and GaN Schottky diodes are majority carrier devices, there is no reverse recovery charge, in fact. Nevertheless, they still demonstrate some reverse recovery effect because of the parasitic capacitance of the Schottky diode.

	GaN Schottky Diode						SiC Schottky Diode					
	25°C			175°C			25°C			175°C		
	Q_{rr}	Q_s	Q_f	Q_{rr}	Q_s	Q_f	Q_{rr}	Q_s	Q_f	Q_{rr}	Q_s	Q_f
Charge [nC]	5.57	1.58	3.99	5.70	1.66	4.05	5.62	1.22	4.59	5.67	1.15	4.52
Q/I_N [nC/A]	2.78	0.79	1.99	2.85	0.83	2.02	2.86	0.61	2.25	2.83	0.57	2.26

Table 5.3 Capacitive charge comparison for GaN and SiC Schottky diodes. Reserve blocking voltage V_{RBV} = 300V and forward current I_F = 2A.

As summarized in Table 5.3, the total charge Q_{rr} of the diode is obtained by integrating the current over time from the zero-crossing of the current when going from forward to reverse bias, until t_{rr}, which is the time that is needed to reduce the reverse current up to 25% of its reverse peak value [114]. Both Schottky diodes have a t_{rr} of 10 ns. As mentioned above, there is practically no difference in the turn-off behavior of the SiC and GaN diodes, and the switching process is only marginally influenced by the temperature. However, the measured reverse recovery current of a fast soft recovery Si-based diode (FR207) clearly demonstrates temperature dependency (Fig. 5.9).

This Si-diode shows an increase of the peak reverse recovery current I_{rr} of about 6% and 20% for 125°C and 175°C, respectively. Accordingly, the reverse recovery charge Q_{rr} increases by 16% and 50% just as the reverse recovery time t_{rr} increases by about 16% and 33%. The absolute value of I_{rr} is thus considerably higher than that of the SBDs. At 175°C, the peak current reaches 24A in a reverse recovery time t_{rr} of 35 ns. This is due to the high speed turn-on of the SiC MOSFET.

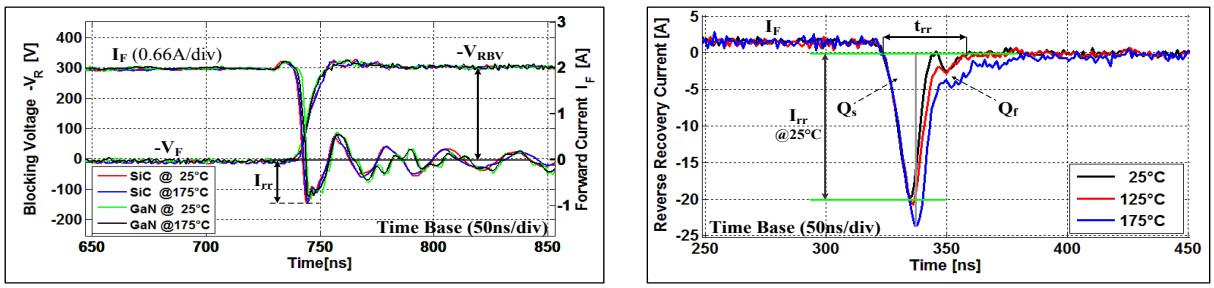


Fig. 5.9 Turn-off: Reverse current of the GaN SBD compared to SiC SBD (C3D02060A) (left) and reverse recovery current of a pn diode (FR207) (right). Blocking voltage V_{RBV} = 300 V and forward current I_F = 2A.

The most important part of switching losses in Schottky diode is the current reverse losses during turn-off. Compared to p-n diodes, these losses are considerably reduced due to the small chip size and hence the small reverse current area. This advantage makes wide-bandgap devices very attractive for high-voltage high-frequency converters. However, GaN and SiC Schottky diodes have higher leakage

currents, which affect the breakdown voltage rating of the device [115], [116]. The on-state voltage is an important aspect in applying GaN Schottky diode in high-voltage applications. In order to measure the on-state voltage precisely, specific measurement technique is required, which is basically similar to the clamping circuit that used for the R_{DSON} characterization of GaN HEMT. As described in chapter 4 (Fig. 4.5a), a passive clamping circuit based on Zener diode has been used to measure the on-state voltage of the GaN and SiC diodes. Fig. 5.10 contains an evaluation of the dynamic forward voltage drop V_F and the dynamic on-state resistance Ron of the GaN and SiC Schottky diodes at different temperatures. The dynamic on-state voltage V_F of both GaN and SiC Schottky diodes is measured at 300 V blocking voltage and 2A forward current. The on-state resistance R_{ON} is obtained by dividing the V_F by the forward current I_F. While the GaN SBD on-state voltage and resistance at room temperature is comparable to the SiC device, a significant increase of the GaN diode on-state voltage can be observed with rising chip temperature. GaN on-state Ron at 175 ºC increases by almost 0.8 Ω with respect to 25 ºC. On the other hand, the SiC on-state Ron goes up just by 0.25 Ω.

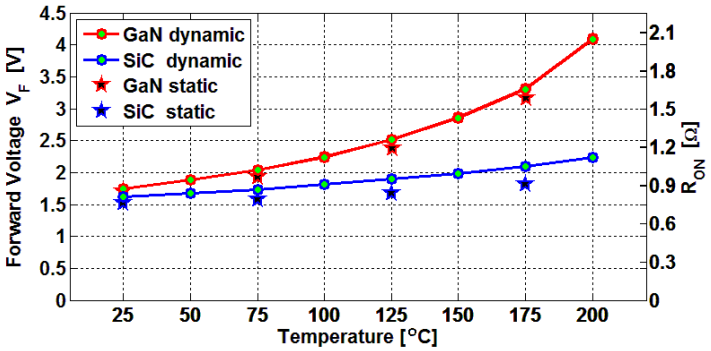


Fig. 5.10 GaN SBD dynamic on-state voltage $V_F = f(T)$ and resistance $R_{ON} = f(T)$ compared to SiC SBD static measurements are indicated for comparison.

5.4.2 600V/8A GaN and SiC Schottky Diodes

In this section, the new 600V/8A GaN Schottky diode (D_1) developed by FBH is investigated. This diode has the same technology as the 600V/2A device (Table 5.2). The switching characteristics are experimentally investigated and compared with a commercial state-of-the-art 650V/8A SiC Schottky diode "C3D08065A" (D_2). Table 5.4 summarizes the investigated transistors used in the test.

Device	Type. Nr	V_{DS}/I_D (V/A)	Ron (mΩ)	Q (nC)	R_{ON}(Ω) x Q(nC)	Package
Normally-off HEMT (S_1)	FBH	600V/16A	65	15	1.0	A0190
Cascode HEMT (S_2)	TPH3006PD	600V/17A	150	54	8.1	TO220
SiC MOSFET (S_3)	SCT2120AF	650V/20A	130	61	7.9	TO220
CoolMOS C7 (S_4)	IPP25R125C7	600V/16A	125	35	4.3	TO220

Table 5.4 Parameters of the investigated power transistors used in the tests.

In general, both diodes demonstrate acceptable switching performance, similar damping coefficients during the transients and almost behave similarly during reverse recovery. Practically, the very fast transients of GaN and SiC Schottky diodes combined with the parasitic elements may lead to unac-

ceptable high frequency oscillations that could substantially impair the system operation through increased of the EMI emission. The switching characteristics are measured at room temperature with the use of the double-pulse circuit. Fig. 5.11 shows the results of the double pulse test for the investigated GaN diode D_1 at 300V. However, as the reverse voltage increases from 360V to 400V, an unacceptable diode leakage current appears, and it reaches 4A at V_{DS} = 400V and I_D = 12A. Such a high leakage current value will cause instant damage to the diode in continuous operation. This is due to the radical increase of the power conduction losses. Because of this, all tests are conducted at 300V blocking voltage. To understand the switching behaviors of GaN and SiC devices in each combination and the dynamic impact of each transistor on each diode and vice versa, it is necessary to consider all the parasitic components located in the power loop. Since the parasitic inductances influence the switching transients significantly at high switching speed, it is specifically crucial to understand the impact of them individually. This section presents the experimental results of the double pulse tests for each combination. Current and voltage waveforms of each combination based-on GaN SBD are sketched in red, green and blue, while the waveforms are shown in black only where SiC diode is in use.

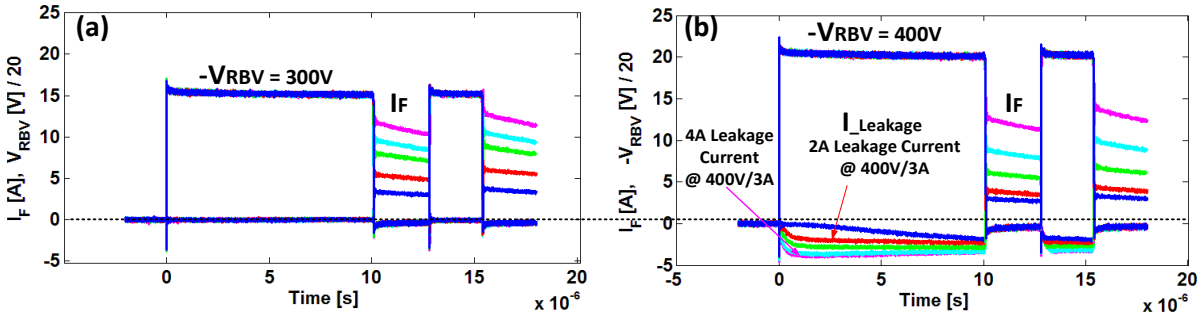


Fig. 5.11 Blocking capability of the proposed GaN Schottky diode at 300V and 400V in double pulse test. The drain current varying from 3 A to 12 A. The SiC MOSFET "SCT2120AF" is used as the active switch.

5.4.2.1 Combinations I and II (Switch: Normally-off GaN HEMT)

The normally-off GaN GaN HEMT (S_1) is employed in combinations I and II with a gate-source voltage V_{GS} was -3 V/+5 V. For each transistor, the gate resistance R_G was chosen as a compromise between the switching speeds and signal oscillation. An optimal switching speed was experimentally obtained by performing several DPTs using different gate resistances to provide the lowest switching losses while ensuring that a sufficient reduction in the transients oscillation and overshoot have been achieved. The selected R_G employed for S_1 was 3.3 Ω. Fig. 5.12 depicts the measured transients for combination I, consisting of GaN HEMT (S_1) and GaN diode (D_1). The results are compared to combination II (GaN HEMT S_1 and SiC Diode D_2). The test is carried out at V_{DS} = 300V and switched drain current of 10A. As clearly seen, current and voltage waveforms of both combinations are relatively identical. During the turn-off, the *dv/dt* and *di/dt* of the GaN and SiC diodes reach 43kV/µs and 1.25kA/µs, respectively, while they decrease to 30 kV/µs and increase to 2 kA/µs during the turn-on. Fig. 5.13 depicts the double-pulse circuit considering parasitic elements in the gate and power loops. As is seen, the power loop inductance encompasses the entirety of all parasitic inductance along the current path in the power loop beginning from the DC source, through the normally-off GaN HEMT, the Schottky diode and the DC source. As the GaN HEMT switching off, the current I_D begins de-

creasing from 10A to zero, while the voltage drop on the parasitic inductances (L_{SS} + L_{SD} + L_{SC} + L_{AS}) reforms the drain source voltage V_{DS}, creating a voltage notch during switching on and a voltage peak during the switching off.

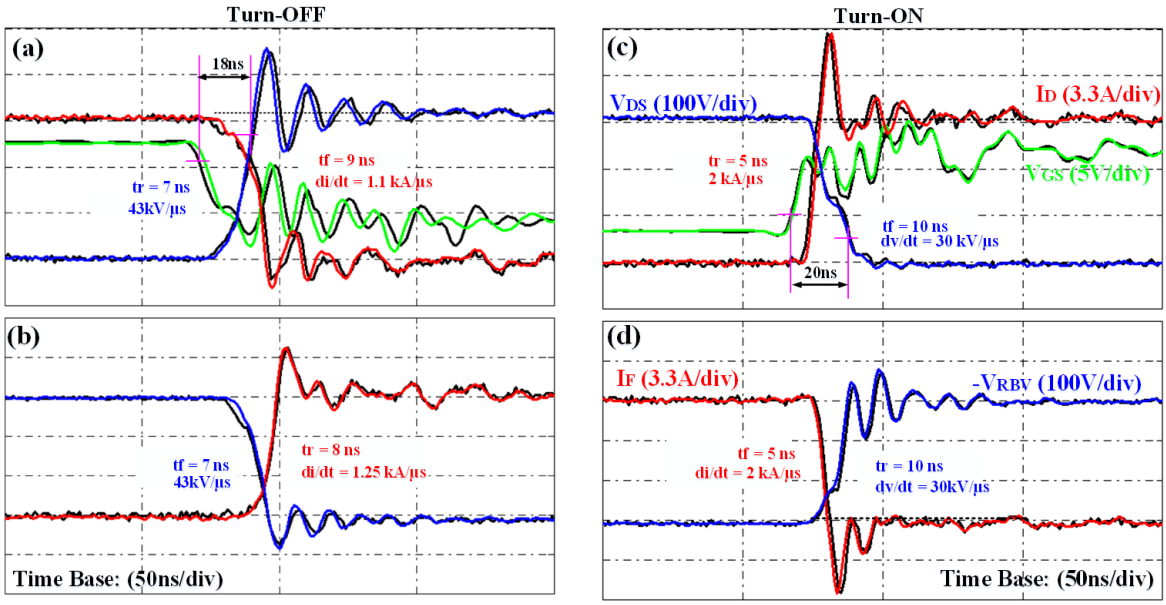


Fig. 5.12 Measured current and voltage transients at R_G= 3.3 Ω for combinations I (S_1 and D_1) and II (S_1 and D_2). Figures (a) and (c) show the transients of the investigated GaN HEMT. While (b) and (d) show the transients of the investigated Schottky Diodes. V_{DS} =300V, I_D =10A and V_{GS} = -3V/5V.

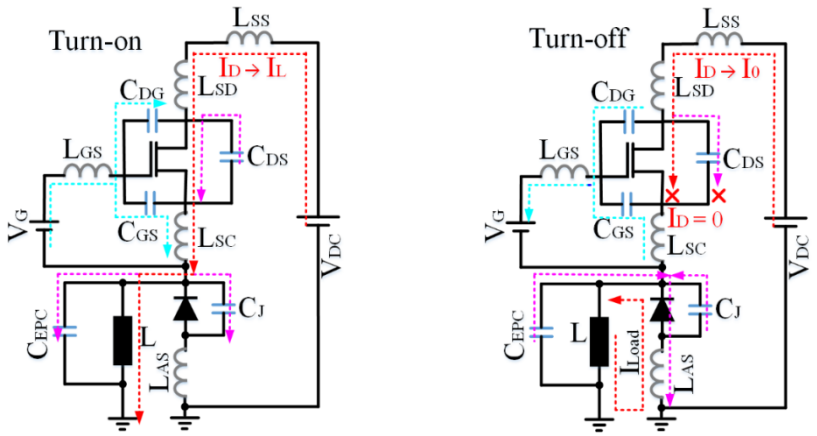


Fig. 5.13 Schematic of double-pulse circuit considering the parasitic elements and current paths during Turn-on and turn-off.

The calculated parasitic inductance of the power loop is 18 nH. For the selected gate resistance (R_G = 3.3 Ω) the drain current overshoot was noticeable with 62% at 10 A during turn-on. Due to the high dv/dt and di/dt, the current overshoot can be high; and in correlation with the energy stored in the stray inductance and the output capacitance C_{DS} the oscillations can occur. The second impact is because of the junction capacitance C_J.

5.4.2.2 Combinations III and IV (Switch: Cascode GaN HEMT)

The structure of GaN HEMT is normally-on. In order to render it acceptable and applicable for industry use, safety has to be in focus. Different technologies have been employed to convert the normally-on device into a normally-off one. The p-GaN gate and the cascode configuration are two of the major technologies presented in recent years. The cascode configuration consists of a low breakdown voltage (typically below 35 V) enhancement mode Si MOSFET, connected in series to the high voltage normally-on GaN HEMT (Fig. 5.14). In this section, a commercial 600V cascode GaN HEMT [49] has been chosen and employed as the active switch with GaN diode for the combinations III and with SiC diode for combination IV.

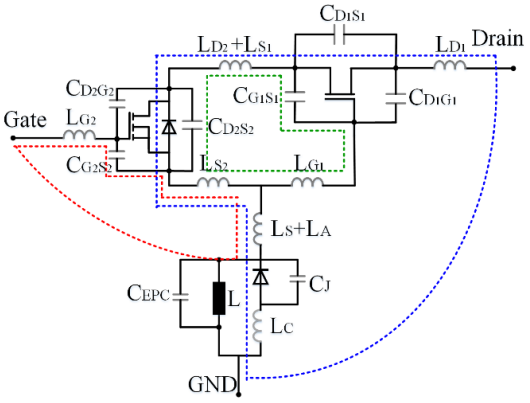


Fig. 5.14 Cascode structure of GaN HEMT in TO-220 package and GaN Schottky diode in A190 package considering all parasitic elements

Fig. 5.15 demonstrates the measured current and voltage transients. The transients of the GaN diode are characterized by a high oscillation and distortion compared to the switching behaviors of the SiC diode, while an unacceptable high frequency current and voltage oscillations are seen.

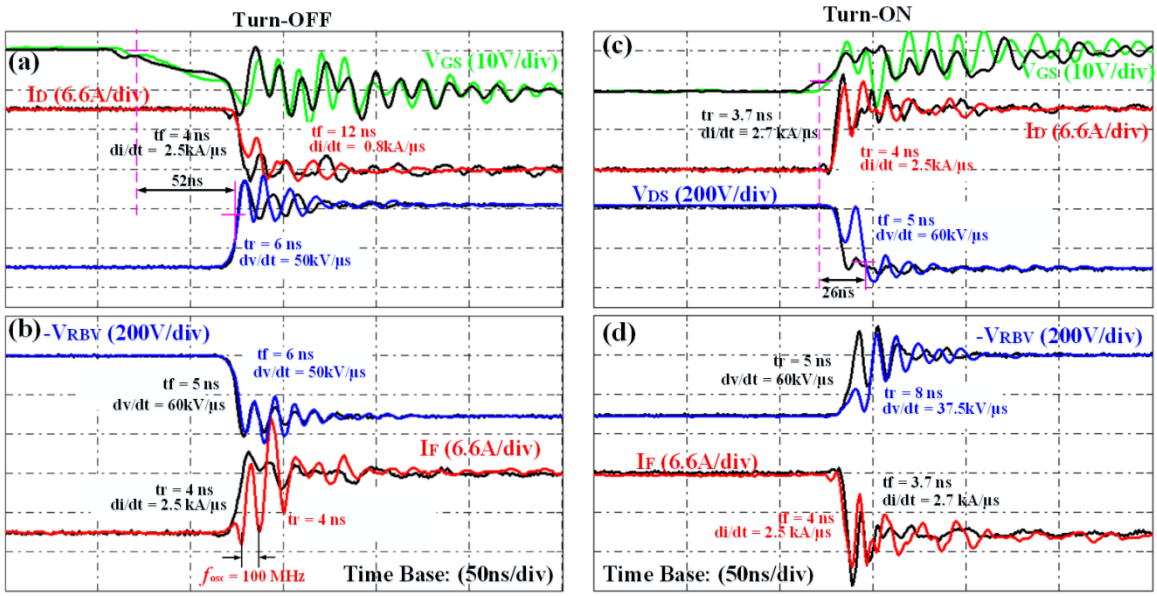


Fig. 5.15 Measured current and voltage transients at R_G= 3.3 Ω for combinations III (S_2 and D_1) and IV (S_2 and D_2). Figures (a) and (c) show the transients of the investigated cascode GaN HEMT. While (b) and (d) show the transients of the investigated Schottky diodes. V_{DS} = 300V, I_D =10A & V_{GS} = 10V.

The measured *di/dt* transients are about 2.5 kA/µs during the turn-on and 2.7 kA/µs during the turn-off. Conversely, from a system design view, such insufficient current and voltage oscillations during the transients are completely unacceptable, as the high EMI might disturb the system. Furthermore, the oscillations at the gate producing repeated turn-on might cause a device failure.

5.4.2.3 Combinations V & VI (Switch: SiC MOSFET)

The SiC MOSFET "SCT2120AF" (S_3) rated at 650V has been employed in the combinations V (S_3 and D_1) and VI (S_3 and D_2). A typical -5V…20V gate source voltage V_{GS} was applied and 2 Ω gate resistor R_G has been selected. The measured transients are sketched in Fig. 5.16. Unlike the results of the combination III and IV, the *dv/dt* rate of the freewheeling GaN and SiC SBDs become 60% slower during the turn-on. This is obviously because of the use of the SiC MOSFET with a quite large input gate charge Q_T = 61nC and device input resistance $R_{G\text{-device}}$ = 13Ω. As seen, during the turn-off, the *dv/dt* and *di/dt* of the GaN and SiC diode are almost identical and reach 20kV/µs and 0.83kA/µs, respectively. During the turn-on, the *di/dt* transients of the both diodes were also equal (1.4kA/µs), while two different *dv/dt* rates have been observed, the transient of GaN diode was evidently faster with 12.5kV/µs compared to the SiC diode with 10kV/µs. This is the most remarkable effect in the test, whereas the other transients behave quite identical.

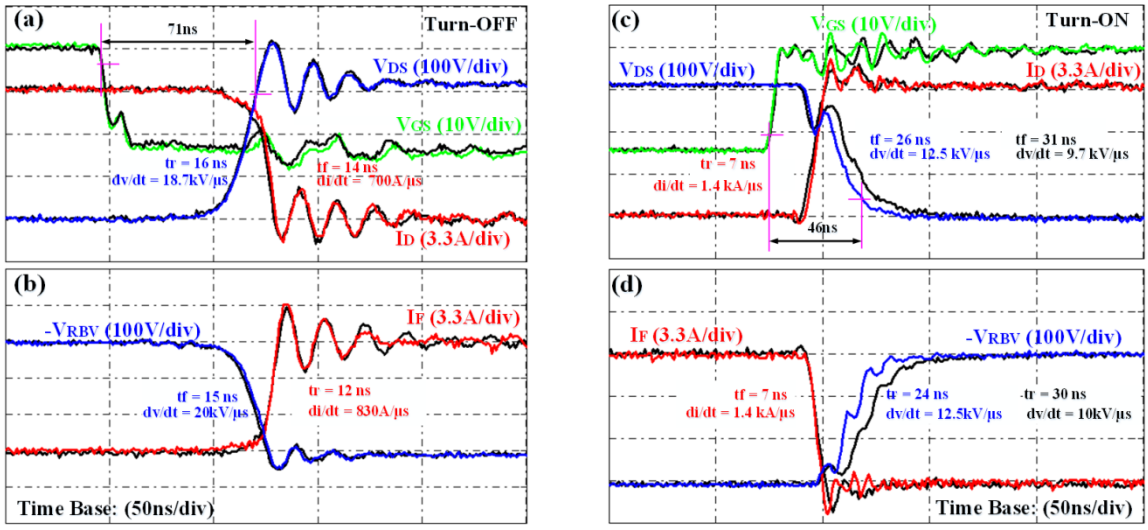


Fig. 5.16 Measured current and voltage transients at R_G= 3.3 Ω for combinations V (S_3 and D_1) and VI (S_3 and D_2). Figures (a) and (c) show the transients of the investigated SiC MOSFET. While (b) and (d) show the transients of the investigated Schhottky Diodes. V_{DS} =300V, I_D =10 A and V_{GS} = -3 V/5 V.

5.4.2.4 Combinations VII and VIII (Switch: Super-junction MOSFET)

The investigated super-junction MOSFET has been employed in the combinations VII (S_4 and D_1) and VIII (S_4 and D_2). A 12V gate source voltage V_{GS} was applied and a 4.7 Ω gate resistor R_G has been selected. The measured transients are sketched in Fig. 5.17. Compared to the results of the combinations I and II, the switching transients of the super-junction MOSFET in combination with the freewheeling GaN and SiC SBDs show a quite similar characteristics and performance. However, a rela-

tively higher current ringing of the GaN diode is observed and compared to SiC diode during turn-off, while the both *dv/dt* and *di/dt* of the GaN and SiC diode are almost identical during the turn on.

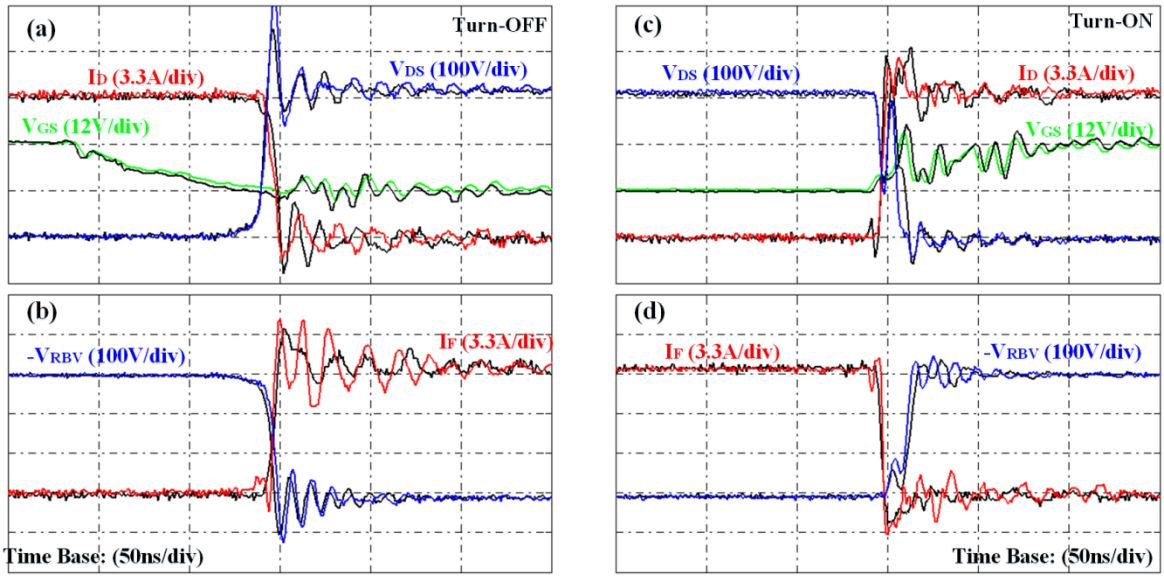


Fig. 5.17 Measured current and voltage transients at R_G= 4.7Ω for combinations VII (S_4 and D_1) and VIII (S_4 and D_2). Figures (a) and (c) show the transients of the investigated Super-junction MOSFET. While (b) and (d) show the transients of the investigated Schottky Diodes. V_{DS} =300V, I_D =10A and V_{GS} = 0V/12V.

5.4.2.5 Evaluation of Switching Energy

In the inductive switching, the transient speed of the transistor is typically controlled by the gate resistance R_G. To evaluate the switching losses of different transistors, an optimal value of R_G has to be determined for each transistor. The resistances 3.3, 4.7, 2, and 4.7 Ω were chosen for the transistors S_1, S_2, S_3 and S_4, respectively.

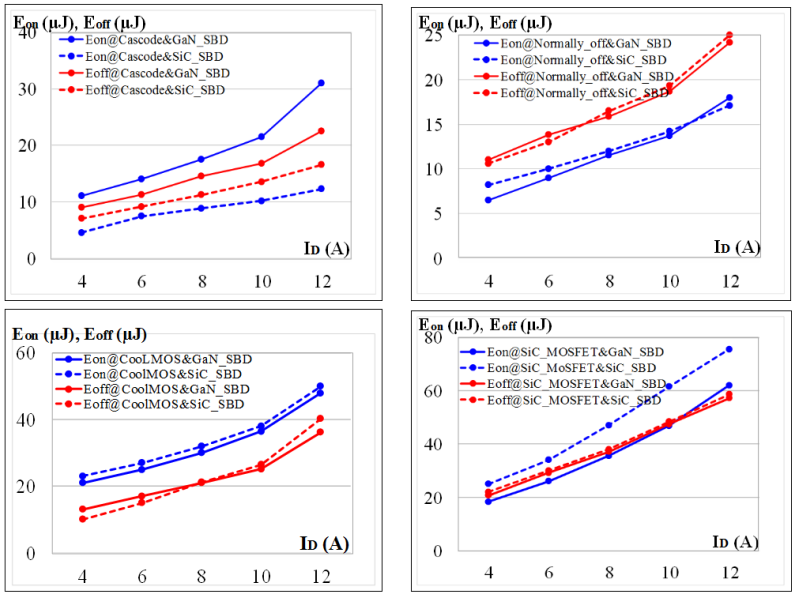


Fig. 5.18 Switching energies Eon (left) and Eoff (right) versus the drain current I_D for the normally-off GaN HEMT at different switching speeds (V_{DS}=300V and I_D =12 A. Gate resistance Rg = 3.3, 4.7, 2, and 4.7 Ω.

Fig 5.18 shows the switching energies E_{ON} and E_{OFF} of each transistor in combination with each diode as a function of the current. As expected, both of E_{ON} and E_{OFF} energies of the SiC MOSFET are much higher than those of the other transistors. Fig. 3.19 shows the E_{ON} and E_{OFF} of each transistor with both GaN and SiC diodes at the operating point of 300V and 10A.

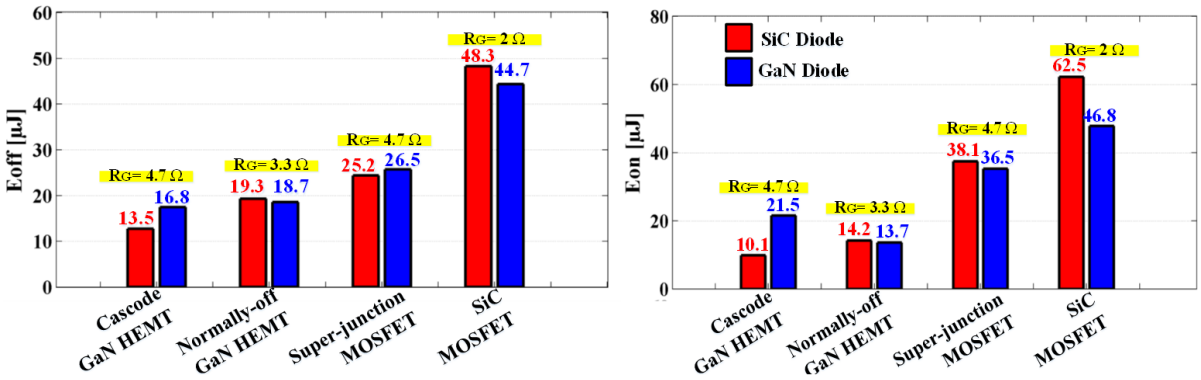


Fig. 5.19 Switching energies E_{ON} and E_{OFF} of each transistor for all combinations (I to VIII) at 10A drain current I_D and 300V drain-source voltage V_{DS} at the room temperature.

5.4.2.6 Zero-Recovery and On-state Resistance of GaN and SiC Schottky Diodes

Fig. 5.20 shows a comparison between the SiC and GaN diodes concerning the recovery capacitive charge Q_{rr} measured in the combinations V and VI. The measured capacitive charge Q_{rr} of GaN and SiC SBDs are 24.5 nC and 26.2 nC, respectively, under test conditions of 300 V blocking voltage, 10A forward current I_F and 0.8kA/µs transient current slope di/dt. Both diodes show a quite similar reverse recovery behavior under the specified conditions.

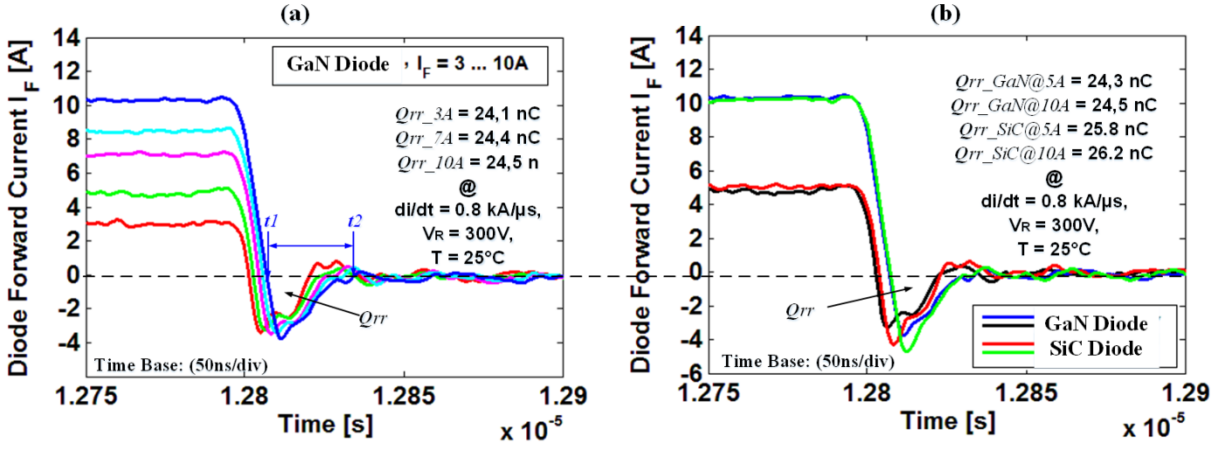


Fig. 5.20 Reverse current of the GaN SBD at different forward currents and (b) compared to SiC SBD.

The evaluated Q_{rr} is independent of the maximum forward current. The on-state voltage of the investigated diodes is also measured. The method employed for this extraction is based on a clamping circuit, which is presented in chapter 4. Fig. 5.21 shows the measured R_{ON} of the investigated GaN and SiC diodes during the double pulse test at different temperatures varying from 25° to 175°. The R_{ON} can be evaluated by the measured on-state voltage V_F divided by the forward current I_F. Both diodes are characterized by positive temperature coefficients. At 175° C, the R_{ON} of the GaN SBD has increased by almost 115% with respect to its measured value at 25º C, in comparison with an increase of 111% in the case of SiC SBD. The normalized resistance ($R_{ON\text{-}dyn}/R_{ON\text{-}Static}$) is 1.27 and 1.1 at 25°C for GaN and SiC SBDs, respectively.

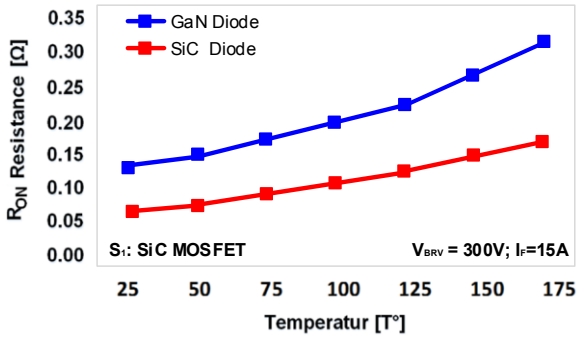


Fig. 5.21 On-state resistance of GaN and SiC diodes at different temperatures varying from 25° to 175°

6 Short-Circuit Behaviour of GaN HEMT

A short circuit, e.g., in a half-bridge converter is a severe and potentially destructive operation condition for a power transistor and needs to be turned-off quickly and safely. In order to define strategies for how to improve the reliability of a power device, it is necessary to understand the failure dynamics during a short circuit. The interest in GaN and SiC as materials for power electronics is principally due to its many superior properties, which allow going beyond Silicon performance limitations [119]-[122]. From an industrial point of view, the switching performance, low on-state losses and good thermal capability of a power semiconductor device are essential requirements, however, robustness is an important issue for reliable high power system and has to be carefully considered [123]-[125]. In this chapter, an experimental study focusing on the short-circuit capability of different types of 600V power transistors based on Si, SiC and GaN is presented. Usually, a 10 µs short-circuit withstand time at 400 V is required for 600 V power transistors. Failure mechanisms during short-circuit conditions of the investigated power transistors are analyzed and a possible theoretical explanation is provided. Measurement results show that the investigated Si and SiC MOSFETs can withstand short-circuit times up to 13 µs at 400 V and 150° C, while the normally-off and cascode GaN devices exhibit considerably less withstand capability.

6.1 Short-Circuit Behaviour

In this context, guaranteeing reliability and safety of high power density and high-temperature power converters is a critical issue [119]-[122]. The short-circuit robustness is defined by the ability of a power semiconductor to survive the short circuit current flow for a couple of microseconds (usually 10 µs) before the hardware-protector senses the fault and disables the gate signal; furthermore, the switch then has to be capable of switching off the high short-circuit current at the high temperature which develops during the current flow. Although several research publications in the last few years have focused on the switching performance of GaN power devices, robustness and reliability issues are rarely discussed. The aim of this chapter is to study and investigate the dynamic behaviors of four different types of 600 V power transistors based on Si, SiC and GaN during the short-circuit mode. Generally, it is very important to understand the failure dynamics in order to find strategies for improving the reliability of the power devices. Parameters of the investigated power transistors used in the short-circuit test are listed in Table 5.2 in the previous chapter.

Fig. 6.1 shows the schematic of the test circuit used for the single-pulse short-circuit tests of the power semiconductors. A photo of the developed hardware is given in Fig. A3.1 (Appendix A3). The PCB is designed with a short power loop in order to keep the parasitic inductance L_{stray} low. Based on the measurements, L_{stray} is evaluated to approximately 25nH. The DC bus voltage is connected directly to the drain and source terminals of the DUT, only the device characteristics and the stray inductance are effective in the power loop. The DC capacitor C_{in} is 240µF, which is quite enough to provide the maximum short-circuit current. However, an additional 1500 µF capacitor bank is connected in parallel to

C_{in} in order to represent the real-application environment of 600V GaN and SiC MOSFETs, which usually contains a high DC-link capacitance. The short-circuit test according to Fig. 6.1 starts with a 1 µs single-pulse. In order to determine the critical energy E_C, the tests are repeated incrementing the short-circuit time by 1µs for each test, until a partial damage or a destructive failure occurs. The DC bus voltage is varied between 100V and 400V. Fig. 6.2 shows the measured waveforms for the 600 V SiC MOSFET "SCT2120AF". To analyze the short circuit current waveform and related critical energy, the stray inductance and thermal effects are considered. As indicated in Fig. 6.2, the short-circuit period can be divided into three phases. Phase I [t_1 - t_2]: When the positive gate-source voltage V_{GS} is applied at t_1, a short-circuit occurs and the drain current rises quickly due to the small value of the parasitic inductance in the power loop. The short-circuit current reaches its maximum at t_2 and enters the saturated region. In phase II [t_2 - t_3], the current conduction causes high power losses, and the self-heating increases significantly causing the current to decrease. In the temperature safe range, it can switch off the short-circuit current successfully. Phase III ([t_3 - t_4]) starts with the turn-off signal of the gate voltage, and the current decreases. The critical energy of the investigated power device E_C is defined by eq. (6.1) and refers to the minimum dissipated energy that leads to the failure of the DUT during short-circuit.

$$E_C = \int_{t_1}^{t_4} V_{DS} \cdot I_{D-SC} \cdot dt \tag{6.1}$$

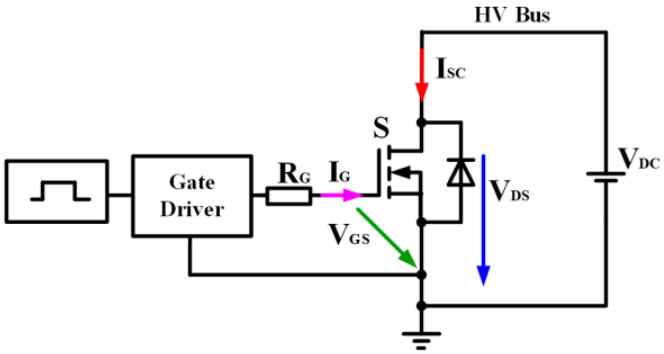


Fig. 6.1 Schematic of the short-circuit test circuit

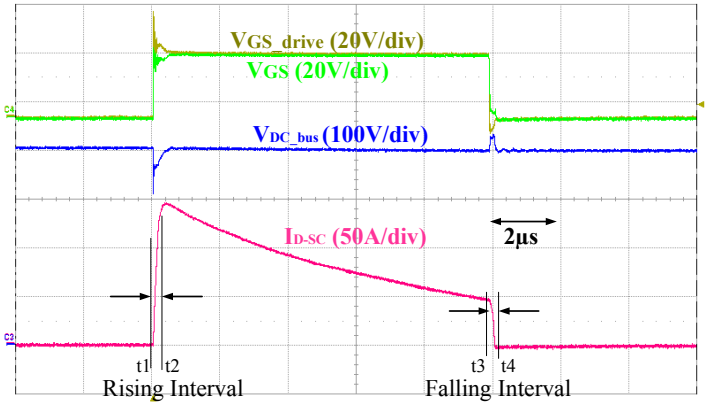


Fig. 6.2 Measured current and voltage waveforms of the SiC MOSFET for the hard switching of a short circuit with 400 V dc bus voltage V_{DC} and short-circuit time T_{SC} = 10µs. T_{Case} = 25 °C.

6.2 Short-Circuit Capability of Normally-off GaN HEMT

The static and dynamic characteristics of the investigated 600V normally-off GaN HEMT is presented in sections 3.4 and 3.7. Further physical details on the device can be found in [63][126]. Fig. 6.3 shows a schematic cross-sectional view of the transistor with an indication of the expected three main regions where a destructive failure can occur. Fig. 6.4 depicts a schematic of the test circuit including the intrinsic and parasitic elements in the GaN HEMT, gate loop and power loop. Exemplary measured short-circuit waveforms for the normally-off GaN HEMT are given in Fig. 6.5. The applied gate source voltage V_{GS} is −3/+5V, and the dc bus voltage V_{DC} is 150V.

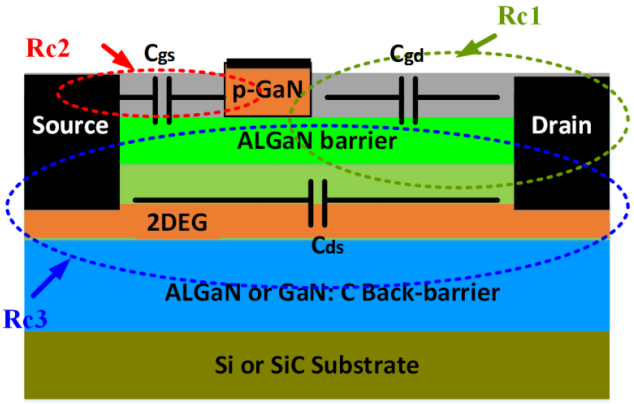


Fig. 6.3 Schematic cross-sectional view of the normally-off GaN HEMT [63][126] with a definition of the expected three main regions R_{C1}, R_{C2} and R_{C3}, where a possible short-circuit failure occurs.

As described in the previous section, at t_1 the transistor turns-on, and the drain current starts to increase quickly due to the parasitic inductance in the power loop. The peak current is 72A, and differs from the saturated current which is obtained measuring the DC characteristics of the device ($I_{D,sat}$=88A at T=25°C and V_{GS}=+5V). This reduction in the peak current may be caused by the increase of the junction temperature. The gate-source voltage in the shown test is applied for 6µs, but the destructive short-circuit failure happens already at t=4.5µs (t_2), corresponding to a critical energy E_C of 45.6 mJ. After the GaN transistor fails, the DC capacitor bank discharges and produces a high DC current $I_{DC\text{-}discharge}$, which is 3 times higher than the short-circuit current $I_{D\text{-}SC}$. Principally, the failure can occur in one or more of the three regions (R_{C1}, R_{C2} and R_{C3}) in Fig. 6.3. From the measurements, it cannot exactly be deduced which part in the transistor is damaged first. However, it can be observed that the gate-source voltage increases from 5V to 10V ($t_2 - t_3$), and at the same time $I_{D\text{-}SC}$ increases from 50A to 110A. The increase of V_{GS} that leads to higher drain current could be explained by a leakage current from the drain region into the gate, indicating that the gate-drain region (R_{C1}) is damaged. For 460 ns from the critical point ($t_3 - t_4$), the drain source voltage is stable and the drain current decreases due to the increase of the temperature. At t_4, the device then finally fails. Fig. 6.6 summarizes the first experimental results of the investigated normally-off GaN HEMT under different DC bus voltages during the short circuit test. The results show the short circuit current behaviours at dc Voltage V_{DS} = 100V... 200V and gate-source voltage V_{GS} = +5V/-3V with short-circuit time up to T_{sc} = 2, 4 and 10µs. The case temperature is 25° C.

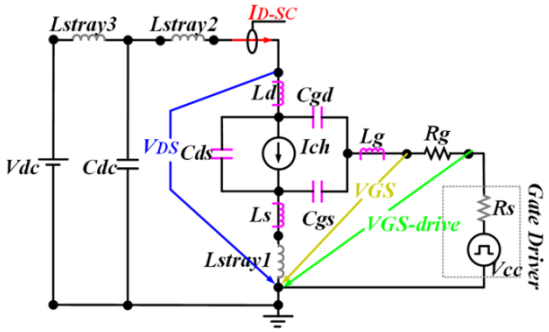


Fig. 6.4 Equivalent SC-test circuit including intrinsic and external parasitic elements and measuring points

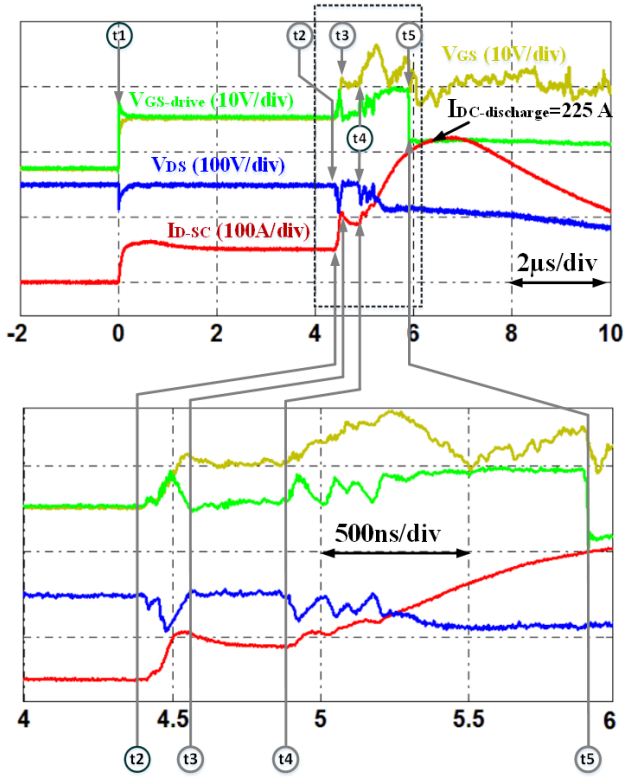


Fig. 6.5 Measured waveforms of the investigated normally-off GaN HEMT in full destructive short-circuit test (no previous partial damage of the gate). Vdc=150 V, Tsc = 6µs. Rg = 6.3 Ω.

Fig. 6.6 shows the short-circuit test of the GaN device for different V_{GS} and V_{DC} voltages in a time range where no failure occurs. Additionally, a test result for a device that was partially damaged during a previous test is depicted in Fig. 6.7.

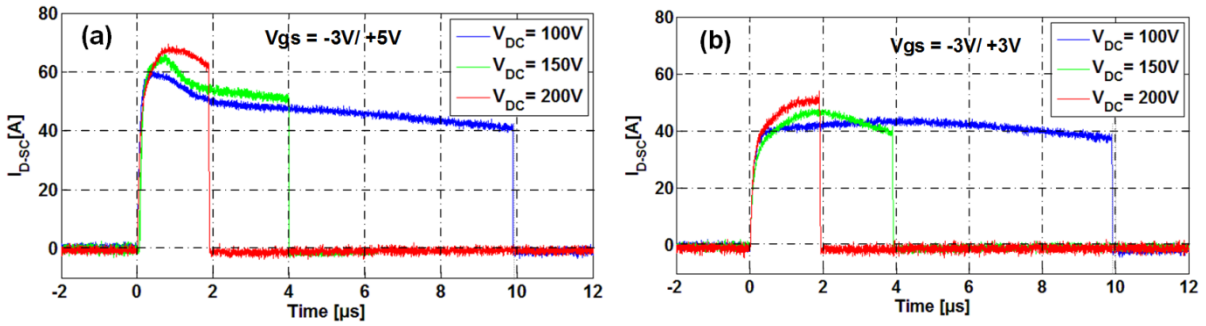


Fig. 6.6 Experimental results of the short-circuit test for the normally-off GaN HEMT with different dc bus voltages V_{DC} =100 V, 150 V and 200 V and gate source voltages (a) V_{GS} = -3/+5 V and (b) V_{GS} = -3/+3V. T_{case} = 25° C. Short-circuit time T_{SC} = 2, 4 and 10 µs. Rg = 6.3Ω.

This test is repeated for other damaged devices at different bus voltages V_{DC}. The test results are summarized in Fig. 6.8. About 40% reduction of the current $I_{D\text{-}SC}$ is measured for the damaged device in Fig. 6.8c compared to the non-damaged device in Fig. 6.6b, while the applied gate voltages are +5/-

3V and +3/-3V, respectively. However, in the case of the previously damaged device, the measured V_{GS} cannot exceed +3V and a noticeable increase of the leakage current beyond 350 mA is observed (Fig. 6.8b). These effects obviously result from the device degradation and are probably due to the damage to the gate insulation.

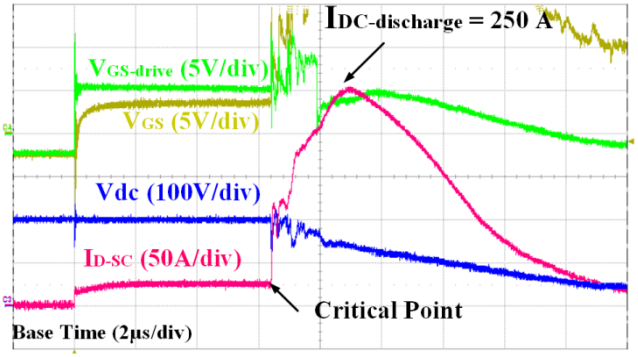


Fig. 6.7 Measured waveforms during SC-test at 200V dc bus voltage and T_{SC} = 8µs, previous partial damage of the gate. Rg = 6.3 Ω.

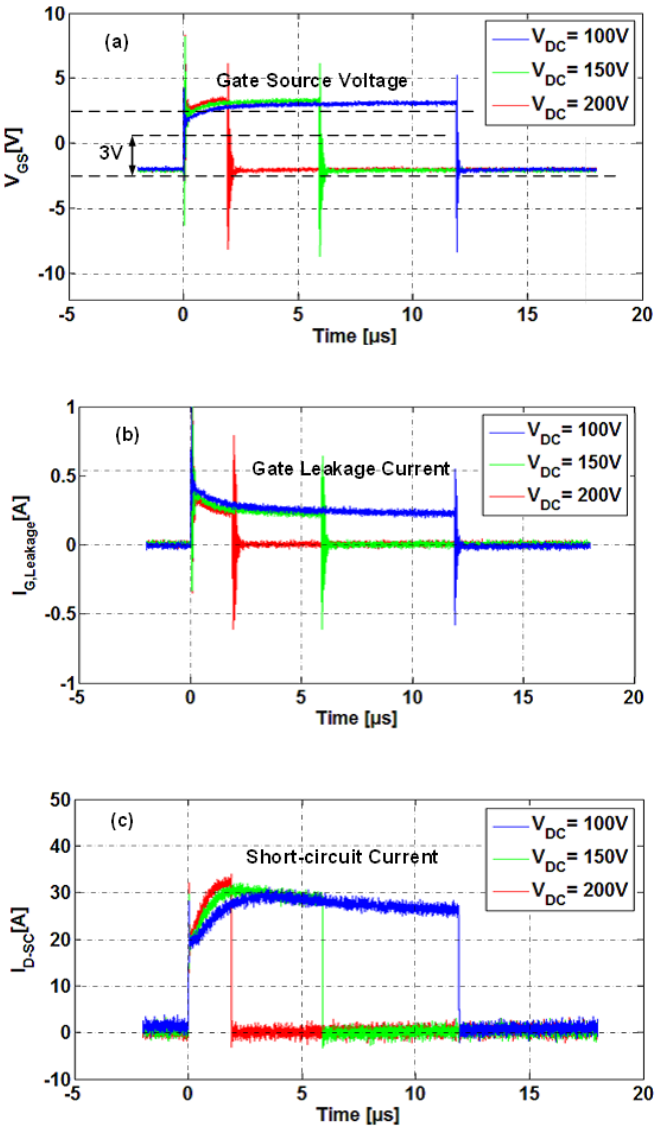


Fig. 6.8 Experimental results of the short-circuit test for the normally-off GaN HEMT after previous damage of the gate; DC bus voltages V_{DC} =100V, 150V and 200V, T_{case} =25° C. Short-circuit time T_{SC} = 2, 6 and 12µs. Rg = 6.3 Ω

6.3 Short-Circuit Capability of Cascode GaN HEMT

Short-circuit withstand capability of the investigated cascode GaN HEMT "TPH3006PD" is presented. In order to understand how the transistor behaves under short-circuit condition; it is important to observe all current and voltage waveforms. However, it is not possible to measure the internal gate-source voltage of the GaN HEMT in the cascode configuration (Fig. 6.9a); only the external gate-source voltage of the low voltage MOSFET can be measured. Therefore, an indication of failing parts that lead to device destruction is not possible. The GaN cascode does not possess the required level of robustness during the short-circuit event. As shown in Fig. 6.9b, the DUT can withstand the short-circuit current for only 1.8 µs at 300V . Fig. 6.10 show a comparison of the short-circuit currents and the dissipated power, measured by altering between three different values of the bocking voltage: 100V, 200V and 300V. The maximum short-circuit current $I_{D\text{-}SC\text{-}MAX}$ is nearly independent of the voltage. Applying the single gate pulse for 10µs, only the device operating at 100V survived the test, but was destroyed in the next test at 16µs pulse length.

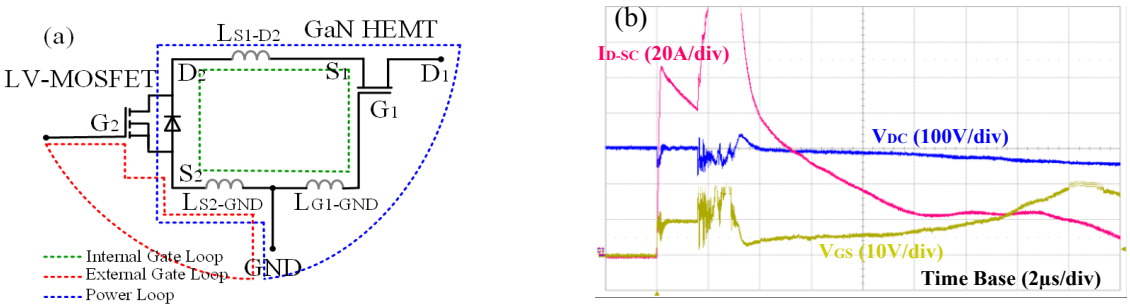


Fig. 6.9 (a) Cascade configuration of GaN HEMT including the parasitic elements. (b) Measured current and voltage waveforms during short-circuit test. V_{DC} = 300 V, Rg = 8 Ω and T_{case} = 25 ° C

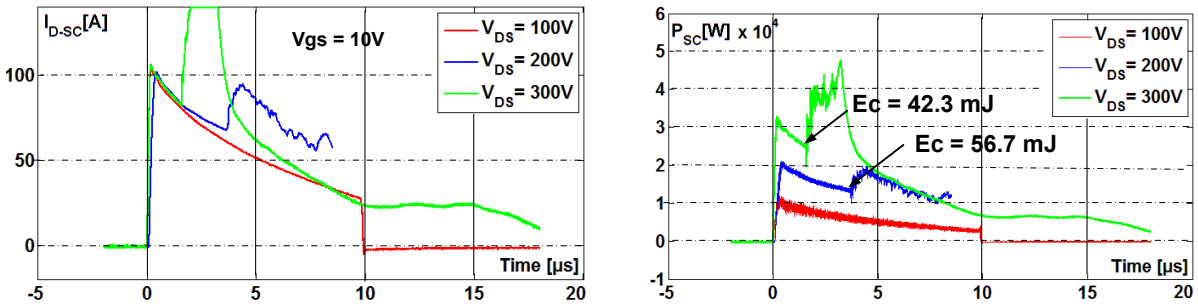


Fig. 6.10 Current and dissipated power of the Transphorm cascade GaN HEMT during a short circuit. V_{DC} = 300V. T_{case} = 25 °C. Rg = 8Ω

6.4 Short-Circuit Capability of SiC MOSFET

A cross-sectional view of a trench SiC MOSFET [127] is given in Fig. 6.11. The measured short-circuit currents $I_{D\text{-}SC}$ of a SiC MOSFET (SCT120AF) based on the trench gate technology is shown in Fig. 6.12. The DC bus voltage is varied from 100V to 400V, the gate source voltage V_{GS} is either -5/+20V or -5/15V, the case temperature is about 25° C and the short-circuit time T_{SC} is 10µs. Fig. 6.12b depicts the measurements with different temperatures, while the gate source voltage is kept constant at -5/+20V. In Fig. 6.13, different short-circuit times T_{SC} increasing from 1µs up to 16 µs are investigated at V_{DC} = 400V and V_{GS} = 5V/+20V. The case with short-circuit time T_{SC} from 10 to 16 µs are the most meaningful for an analysis of the failure dynamics.

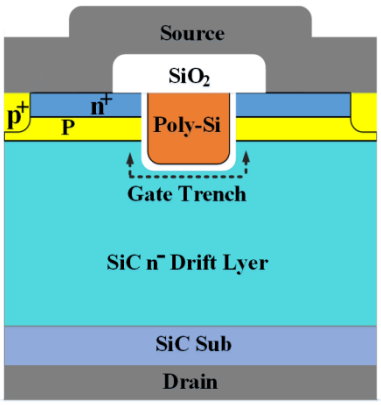


Fig. 6.11 Cross-sectional sketch of a SiC MOSFET structure [126]

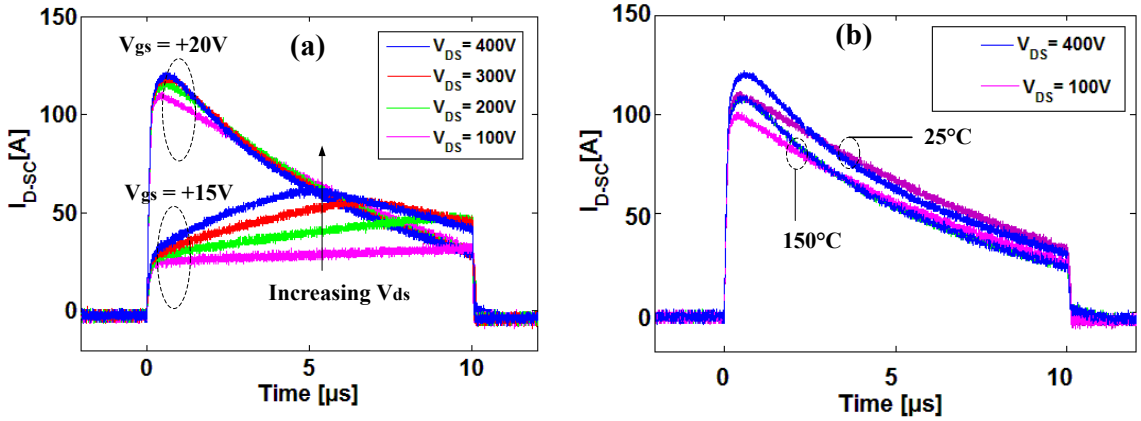


Fig. 6.12 Experimental results of the short-circuit test for the investigated SiC MOSFET applying different dc bus voltages from 100 V to 400 V, withstand time T_{SC}=10µs. a) measured $I_{D\text{-}SC}$ with different V_{GS} at 25° C and b) at different temperatures with constant gate source voltage V_{GS}.

Based on Fig. 6.13, a number of interesting observations can be made. First, for T_{SC} up to 12µs, the device is stable during and after each test, and exhibits no sign of degradation or failure. The leakage tail current increases by about 2A as the short-circuit time T_{SC} increases by 1 µs. The appearance of this leakage current after a SiC MOSFET switches off a short circuit has been reported before, e.g. in [119]. The third observation is the partial damage of the gate during the test with T_{SC} = 13µs. While the drain current is successfully switched off at 13µs, after a delay of 2.3 µs follows a failure in the gate at time point 15.3 µs. Similar failure mechanisms for the 1.2 kV SiC MOSFET are reported in [128][130]. Due to this partial gate damage, the gate source voltage V_{GS} declines to 10V during the subsequent short-circuit experiments with T_{SC} = 14µs…16µs. It is assumed that the dissipated energy in the channel was close to the critical value E_C. This leads to failure and damage in the gate source area after the turn-off because of thermal runaway phenomenon [119]. Similar to the presented SiC

and GaN transistors, the short-circuit with-stand capability of the investigated super-junction MOSFET "IPP25R125C7" is also tested. The test results are shown in Fig. A3.2 (Appendix A3).

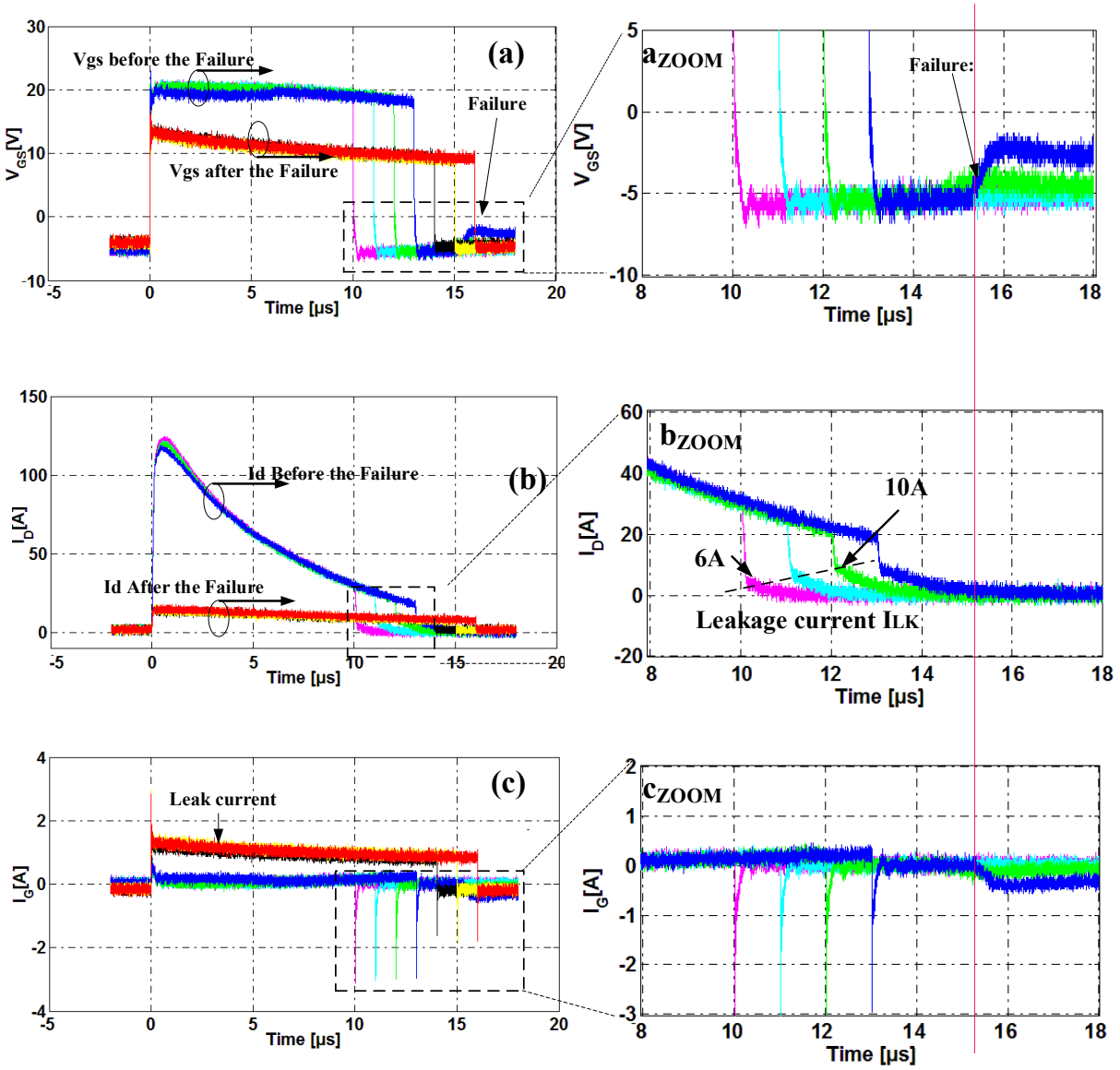


Fig. 6.13 Experimental results of the short-circuit test for the SiC MOSFET with T_{SC} up to 16µs. Gate source voltage V_{GS} = -5V/+20 V and dc bus voltage V_{DC} = 400 V. Case temperature T_{case} =25 ° C. Rg = 4.7 Ω.

6.5 Transistor Comparison

The state-of-the-art super-junction MOSFET "IPP25R125C7" is included in the comparison. The results indicate that the 650V SiC power MOSFET and the super-junction MOSFET are relatively robust during short-circuit tests up to about 70% of their rated voltage. However, if higher voltages are applied (typically over 480V), the devices cannot withstand the commonly required 10 µs short-circuit time. According to our measurements, the cascode GaN HEMT can withstand the short-circuit test until 50% of its rated voltage with a withstand time of 1.8µs. This seems to be not sufficient for a commercial device. The investigated normally-off GaN HEMT shows a similar low robustness, the

device can withstand the test at 34% of its rated voltage for only 2µs. The experimental results for different DC bus voltages are summarized in Fig. 6.14a and Fig. 6.14b. Gate source voltages are -3/+5 V, 0V/+10 V and -5/+20 V for the normally-off GaN, cascode GaN HEMT & SJ-MOSFET and SiC MOSFET, respectively. The results show that short-circuit times and critical energy of all devices are voltage dependent. With the increase of the dc bus voltage, less dissipated energy is needed to cause a thermal destruction (Fig. 6.14a), and the time duration till the failure occurs is reduced. This obviously indicates the impact of the electric field stress within the device on failure occurrence and device degradation. As a final result, Fig. 6.15 shows the required short circuit safe operating area (SCSOA) and the measured capability of each of the investigated power transistors

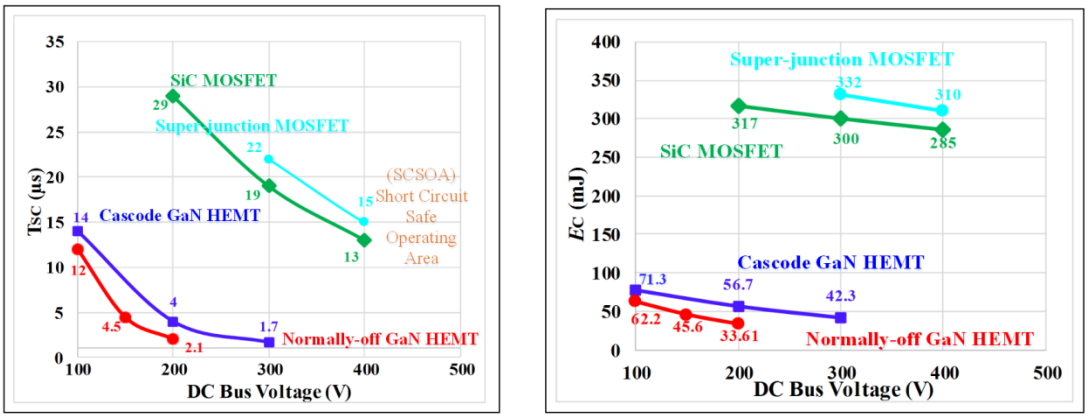


Fig. 6.14 (a) Comparison of short-circuit withstand times vs. dc voltage.
(b) Comparison of critical energies vs. dc voltage.

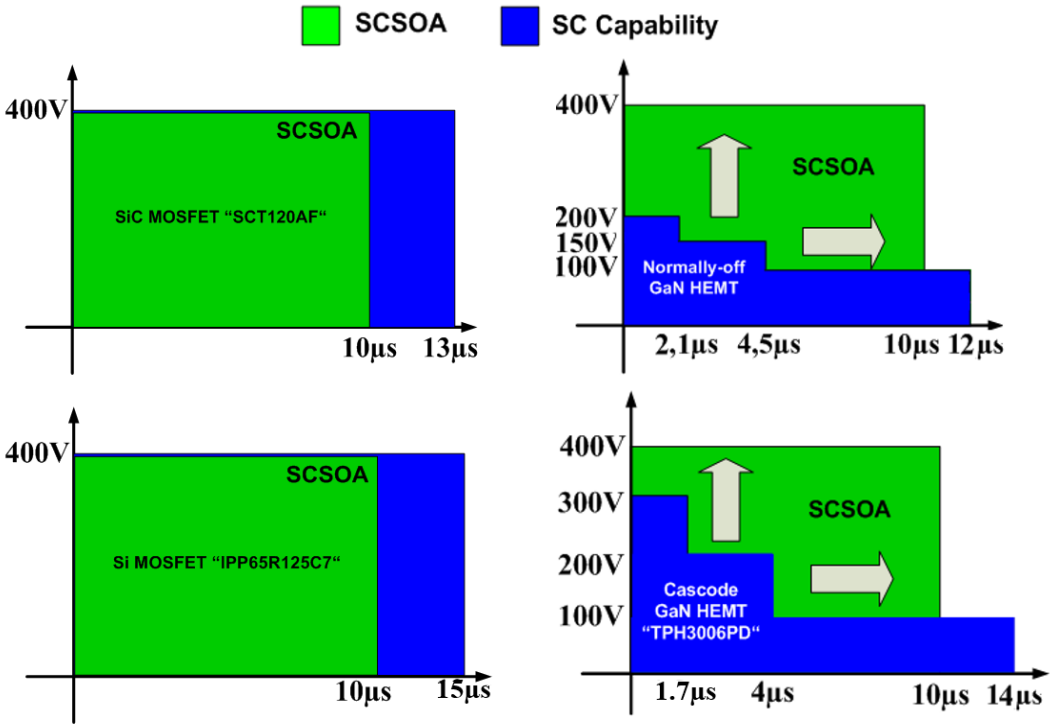


Fig. 6.15 Short circuit safe operating area (SCSOA) and the measured capability of the investigated devices.

7 GaN-based Power Converter

An interleaved buck converter (IBC) based on normally-off GaN HEMT is constructed to evaluate the device performance in continuous operation. The total efficiency is evaluated at a maximum output power of 2.7 kW and different switching frequencies that vary from 50 kHz to 500 kHz. The implemented converter is tested again using other state-of-the-art Si, SiC and GaN power transistors. The measured efficiency of the converter based on the normally-off GaN HEMT achieves 98%. However, by increasing the output power over 0.8 kW with increases in the off-state voltage beyond 230V, the dynamic on-state resistance will also increase, which is most likely due to the trapping effect in the transistor channel. Consequentially, the conduction losses in the GaN HEMT become higher and the switching performance becomes lower. These efficiency results are compared to the other converters based on Si and SiC MOSFETs.

7.1 Design Objectives

By deployment of GaN-based power devices in the power converter, the benefits and advantages of GaN devices are significant compared to traditional silicon devices. For the power semiconductor high-speed switching devices, an accurate figure-of-merit (FOM) needs to take into account all electrical power losses. Due to the low FOM R_{DSON} (V_{GS},I_D) x Q_{sw} (V_{DS}) GaN-based power device enables the converter designer to increase the switching frequency without compromising the efficiency. Thus, there is a reduction in the size of the magnetic components and the output capacitance resulting in a smaller overall system size. This also decreases the overall system cost by reducing the number of the inductors and capacitors as needed. In this chapter, the performance of the proposed 600V GaN HEMT [63] is examined in an interleaved buck conversion (IBC) application at switching frequency varying from 50 KHz to 500 kHz and maximum output power of 2.7 kW in conjunction with the presented 600V GaN Schottky diode [63] [119] and the commercial state-of-the-art SiC Schottky diode [113]. The experimental investigation using the IBC can be specified by the following four tasks:

1) Testing the IBC employing the investigated 600V normally-off GaN HEMT and GaN Schottky diode: (a) Obtaining the switching performance in CCM operation (b) Measuring the dynamic R_{DSON} and comparing the results with double pulse test. (c) Evaluating the total efficiency of the IBC.
2) Replace the GaN Schottky diode with the commercial state-of-the-art SiC Schottky diode and compare the efficiency in both cases.
3) It is known from the experimental double pulse test in section 5.4.2.2 that the investigated GaN Schottky diode suffers from increase of the leakage current at high off-state voltage, typically beyond 320 V. Therefore, it cannot be employed in continues operation at high reverse blocking voltage (typically higher than 260 V). The power devices used in the converter are listed in Table 5.4. Because of the increase of the dynamic on-state resistance of the investigated normally-off GaN HEMT at high blocking voltages, only 230V maximum drain source voltage is applied in order to avoid any damage on the device.

7.2 State-of-the-Art: GaN-based Converter

Since 2013, several industries and research institutions were starting to design and prototyping GaN-based power converters for different industrial applications. Fig. 7.1a shows a 250 W power supply converter based on cascode GaN HEMT specifically to meet the requirements of an All-in-One converter [143]. The all-in-one power converter consists of three Transphorm 600 V cascode GaN HEMTs in both the PFC and bridge configuration. The converter can deliver up to 20 A at 12 V output with a peak efficiency of 95.4% from a 230 V AC line. In [131], an LLC resonant converter based on cascode GaN HEMT for battery charging is presented. Fig. 7.1b shows the schematic circuit. The converter is operated at 1 MHz for maximum output power of 300W. The power efficiency of this converter reaches 96%.

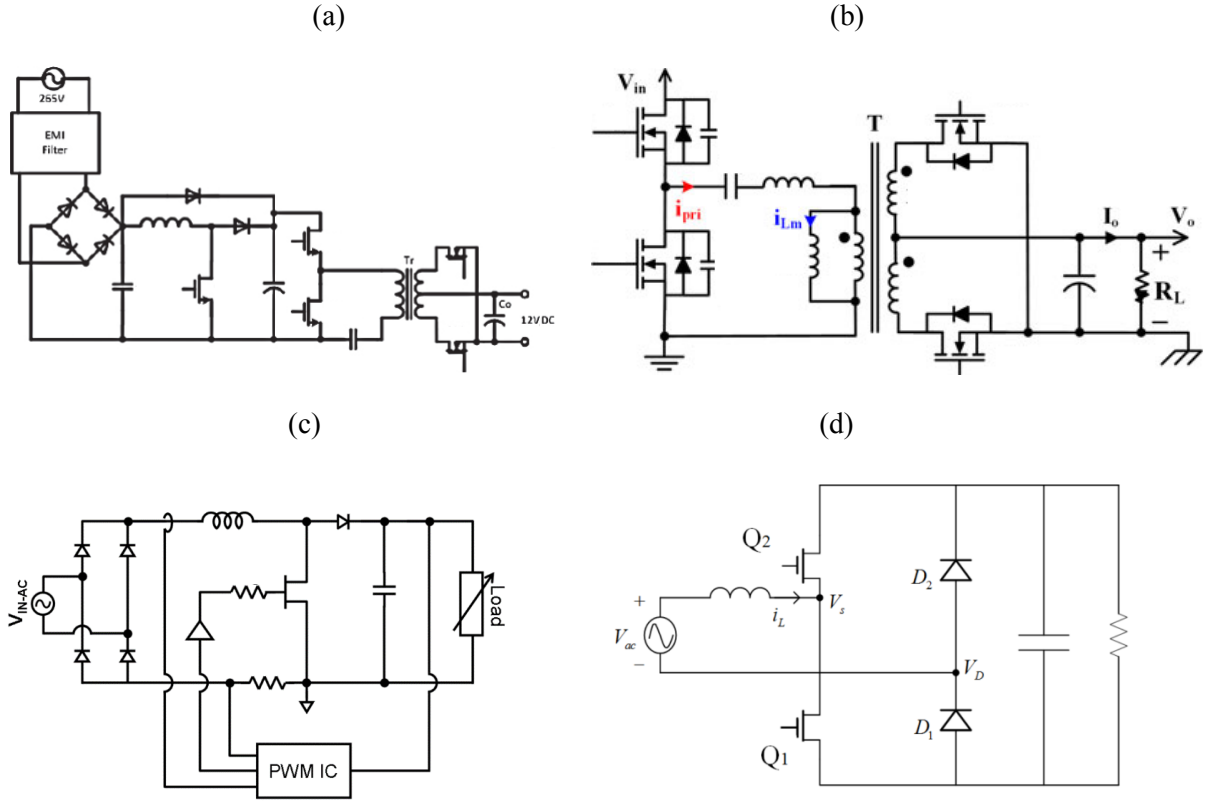


Fig. 7.1 (a) Circuit of AC-DC power converter (230V/12V) based on 600V cascode GaN HEMT [143]. (b) LLC resonant converter (230V/12V) based on 600V cascode GaN HEMT [131]. (c) PFC circuit using cascode GaN HEMT with switching frequency of 680 kHz [144]. (d) Totem-pole bridgeless PFC boost converter based on GaN HEMT for line rectification [137].

The third circuit demonstrated in Fig. 7.1c is a PFC circuit. The converter is designed and tested using three different 600V power transistors: cascode GaN HEMT, normally-on GaN HEMT and super-junction Si MOSFET. As given in [143], the experimental results of power efficiency are obtained with 100 VAC input voltage and switching frequency varying from 100 kHz to 1 MHz. The results show the advantage of using one GaN HEMT in the circuit compared to the Si MOSFET. The last circuit demonstrated in Fig. 7.1d has a totem-pole bridgeless topology [137]. The circuit consists of two GaN HEMT and two diodes which are used for the line rectification. The efficiency has been

measured at 115 Vac or 230 Vac input and 400 Vdc output. The efficiency result for this totem pole PFC board is the highest among PFC designs with similar PWM frequency; it reaches 98.8% at 230VAC input.

7.3 Interleaved Buck Converter (IBC)

The concept of interleaving in power converters is not new [145]. This technique is already used in several industrial applications such as solar, wind and automotive power system [146]. Using this technique, advantages such as higher efficiency and power density can be achieved. It can be beneficial where high power is required. Nevertheless, the technique has also been considered for low-power applications such as low-power spacecraft, satellite and avionic systems. It was introduced as power system architecture in [145]-[149]. The multi-channel interleaved buck converter for the voltage regulation application has been intensively investigated in [150]-[153]. Fundamentally, an interleaved power converter can be created by dividing the main power circuit into multiple smaller interleaved circuits that are connected in parallel, while the power switches of each circuit are synchronized and operated using relative phase shifts. Contrary to the conventional converter, the interleaved buck or boost converter demonstrates the benefits of the packaging, modularity and the size reduction of output filter. One of the main benefits of interleaved converter is the ripple elimination of the input and output current (low ripple and harmonic cancellation). Nevertheless, the current in the inductor of each converter still has a higher ripple, which depends on the inductance value. On the other hand, the increase of the copper losses in the inductors because of the large current ripples is an issue which cannot be solved by using the interleaving technique [145].

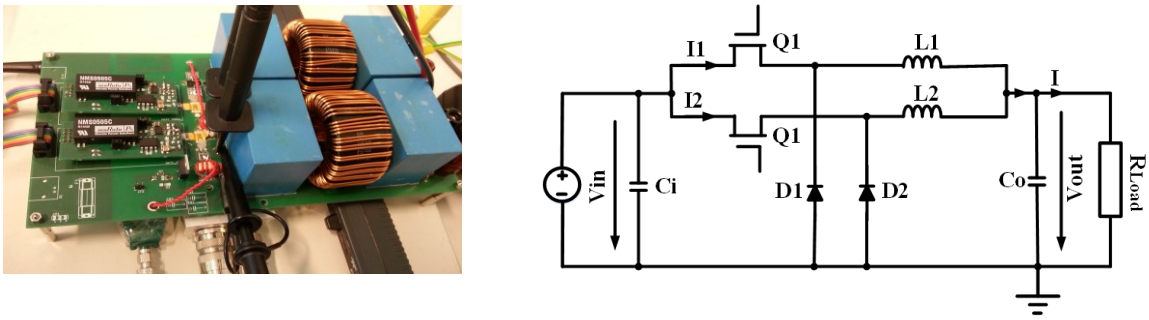


Fig. 7.2 Harware setup and schematic circuit of the 2-stages interleaved buck converter.

The implemented interleaved buck converter (IBC) presented in this thesis, is technically quite simple. Fig. 7.2 demonstrates the implemented hardware setup and the schematic circuit. It consists of only two power subcircuits (two buck converters) which are connected in parallel. Each stage consists of 120 µH powdered iron core inductor and 80 µF output capacitors. A conventional gate driver based on the MOSFET's driver IXYS 609, as described in section 2.3, was employed to enable fast switching of power transistors. The PCB circuit was designed in two layers and special care was taken in the circuit design in order to minimize the distance between components, which reduces parasitics of the gate and power loops. The experimental setup including the converter hardware prototype and the measurement equipment are demonstrated in Fig. A4.1 (Appendix A4).

7.3.1 Normally-off GaN HEMT in Continuous Operation

Switching behavior, power losses and efficiency of the IBC with normally-off GaN HEMT and GaN Schottky diode are presented in this chapter. These results have been achieved as a part of a graduation bachelor's thesis given in [162].

7.3.1.1 Switching Behaviors

Fig. 7.3 and Fig. 7.4 show the measured waveforms in the IBC at 200 kHz. As seen from results in Fig. 7.4a and Fig. 7.4b, the rising and the falling times of the transistor transients during the turn-on and turn-off, obtained with the 10% – 90% measurement rule, are 11.3 ns and 15.5 ns, respectively.

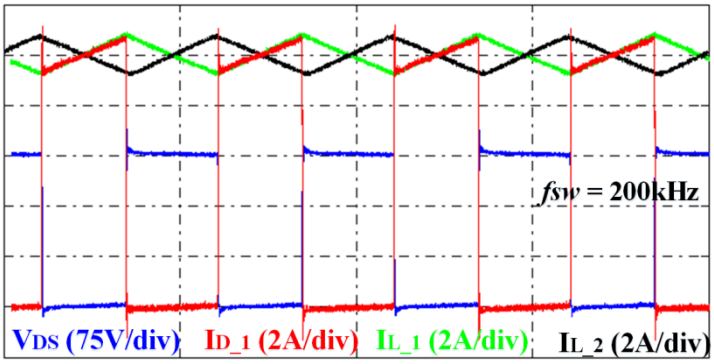


Fig. 7.3 Measured IBC current and voltage waveforms using GaN HEMT and GaN SBD at 200 kHz switching frequency. Input voltage V_{DC} = 230 V. Input voltage V_{DC} = 230 V, inductor currents I_{L_1} , I_{L_2} = 10A and drain current (in S_1) I_{D_1} = 10A. Gate resistor R_G = 6.3 Ω.

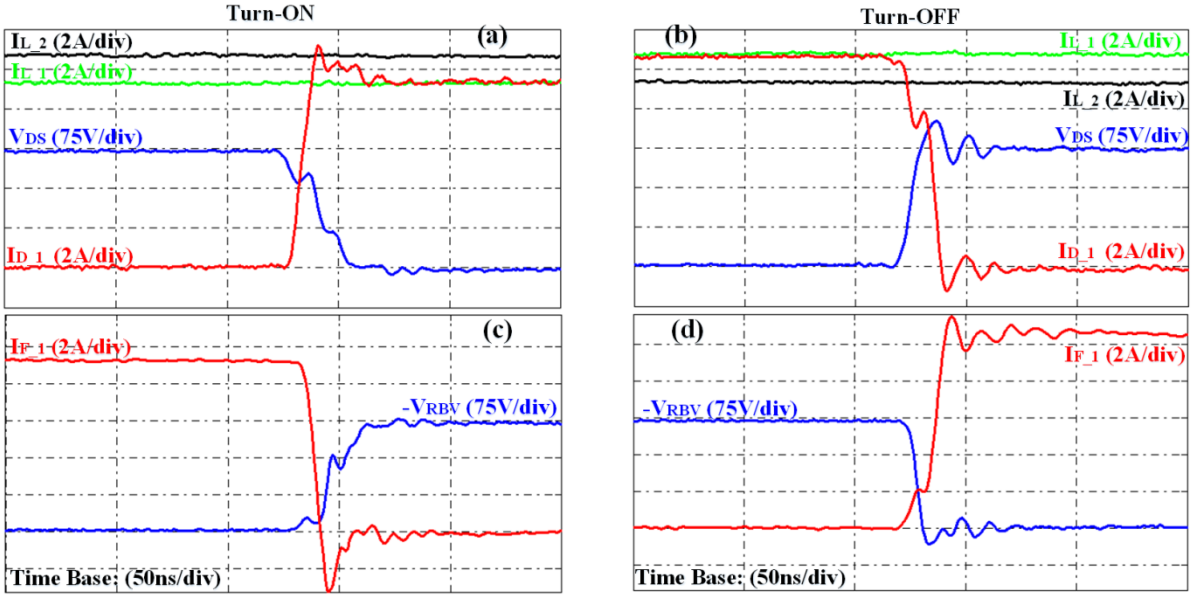


Fig. 7.4 Measured current and voltage transients for the IBC using the investigated normally-off GaN HEMT (S_1) and GaN SBD (D_1) at 200 kHz switching frequency. (a) and (c) show the transients of S_1 and D_1 during turn-on, respectively, while (b) and (d) during the turn-off. L_1 and L_2 are the inductors currents. Input voltage V_{DC} = 230 V, inductor currents I_{L_1} , I_{L_2} = 10A and drain current (in S_1) I_{D_1} = 10A. Gate resistor R_G = 6.3 Ω.

In order to investigate the switching performance of the GaN HEMT with GaN SBD in CCM, the IBC has been operated at different input voltages and load currents. Further information about the switching transients of the investigated normally-off GaN HEMT in CCM at different drain source voltages and drain currents can be found in the Appendix A5.

Fig. 7.5 summarizes the measured results of R_{DSON} versus I_D, where R_{DSON} increases approximately linearly with the drain current I_D. While the high drain current along with the high off-state voltage and the high switching frequency plays an important role by increase the trapping mechanism in GaN HEMT, it appears that the considered degradation of the R_{DSON} is the reason for the time increase of the falling transient at 225V/10A. To conclude and compare the results of the dynamic R_{DSON} during both CCM and double pulse tests, exemplary measurements are given in Fig. 7.6. The measuring point during the CCM test is 0.5 µs, while 0.5 µs and 1µs during the double pulse test. The measured R_{DSON} is obtained during CCM at an instantaneous case temperature of the GaN device, which reaches 119° C. The results show clearly that the increase of dynamic R_{DSON} is significantly higher during continuous operation compared to the double pulse test.

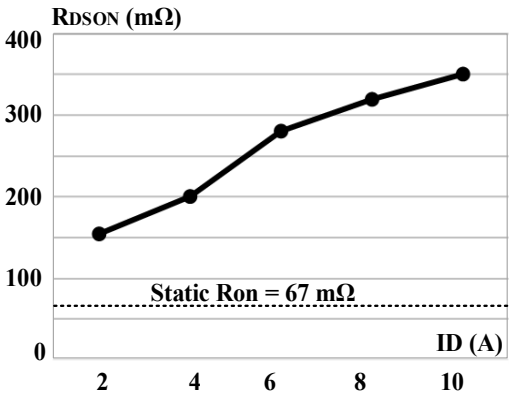


Fig. 7.5 Measured dynamic on-state resistance R_{DSON} vs. drain current I_D at 225V drain-source voltage V_{DS}. R_{DSON} is obtained at 0.5µs (high dynamic region) after the V_{DS} transient.

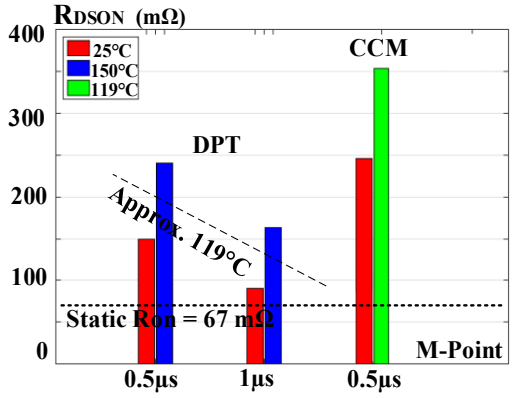


Fig. 7.6 Comparison of the measured dynamic R_{DSON} at different measuring points (0.5µs and 1µs) during double pulse test (DPT) and continues operation (CCM). V_{DS} = 225V and I_D = 10A.

7.3.1.2 Evaluation and analysis of power losses

The evaluation of power losses have been made with input voltage varying from 100V to 225V, switched current from 1 A to 12 A at 50% duty cycle, the output power from 100 W to 1350 W, output voltage from 50 V to 110 V and switching frequencies variation from 50 kHz to 500 kHz in this experiments. The mathematical and experimental scheme employed to evaluate the power losses is given in Appendix A6. To avoid the thermal runaway of power devices, a water cooling system has been employed to keep the components temperatures in the operation range. Fig. 7.7 shows the switching energies Eon and Eoff versus drain current I_D for different off-state voltages varying from 50V to 225V. The selected gate resistance R_G was 7 Ω. Eon and Eoff increase roughly linearly with the drain current up to 200V off-state voltage. Fig. 7.8b shows the evaluated power losses of the power devices (S_1, S_2, D_1 and D_2) at different input current and voltages. As seen in Fig. 7.8a, the increase of the power losses at 150V, 175V and 200V is almost the same.

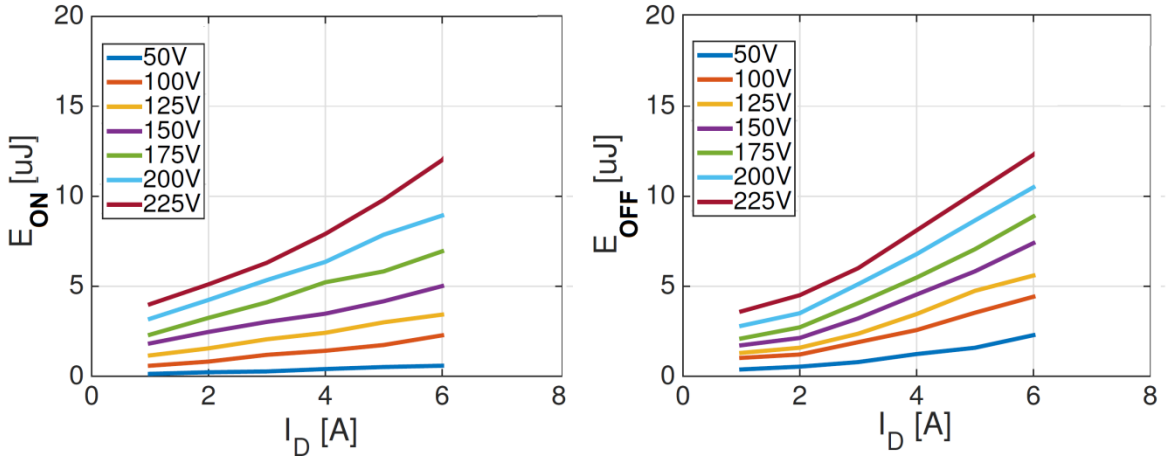


Fig. 7.7 Switching energies E_{ON} and E_{OFF} vs. I_D at different blocking voltages varying from 50V to 225V.

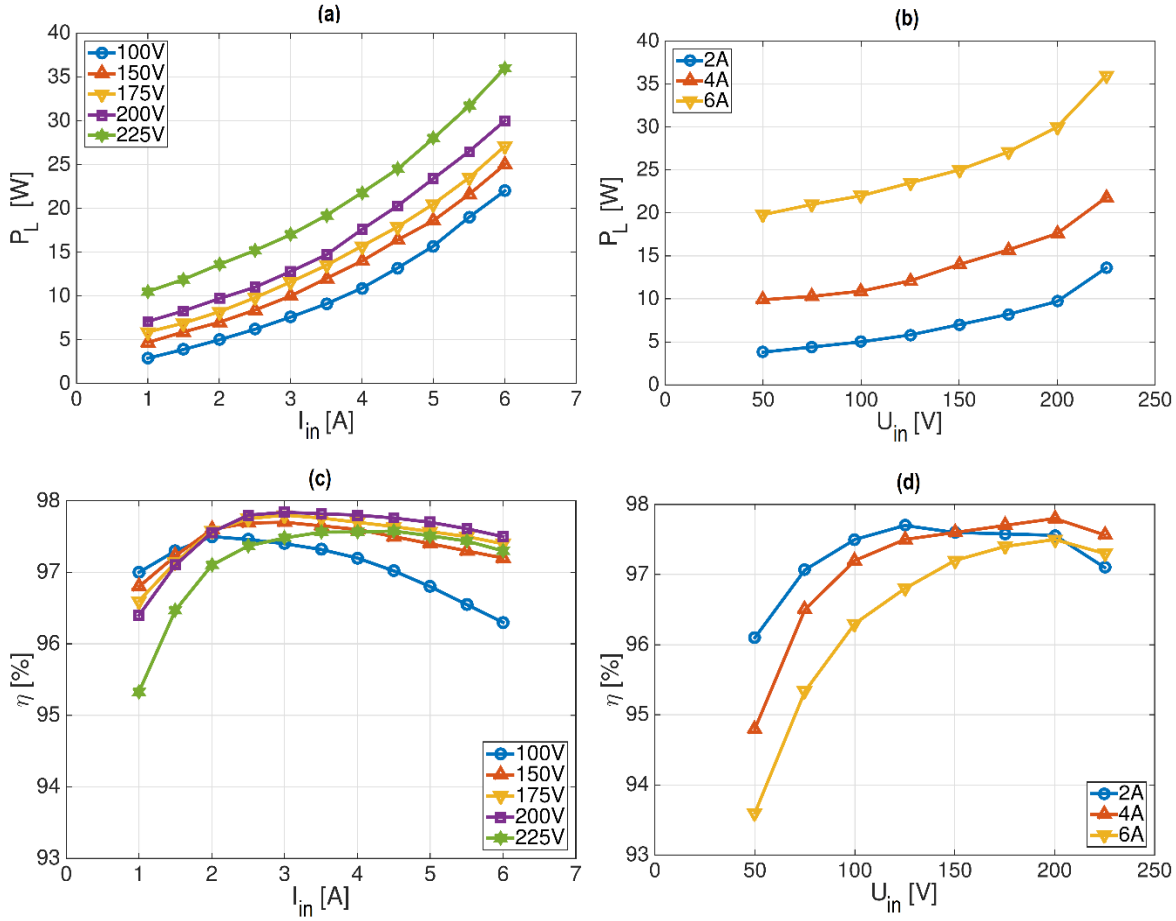


Fig. 7.8 (a) and (b) Power losses in GaN devices (S1, S2, D1 and D2), (c) and (d) Converter efficiency. Switching frequency is 200 kHz.

Finally, Fig. 7.8c and Fig. 7.8d show the converter efficiency at different input currents and voltages. The highest efficiency achieved in the test is 97.8% at 200V and 3A. However, a considerable reduction of the efficiency is observed by increasing the input current and voltage. As mentioned above in

chapter 4, such reduction in the efficiency is caused by device degradation. This is probably due to the trapping effects occurring during the switching events. This degradation is translated in the device by increase of the dynamic R_{DSON} at high current high voltage and high frequency. In this work, the converter efficiency and performance based on the normally-off GaN HEMT need to be evaluated. For this purpose, benchmarking with other commercial state-of-the-art power transistors based on Si, SiC and GaN has been conducted. The applied input voltage V_{in} in the previous test was set to a fixed value of 225VDC because of the transistor degradation. However, for the commercial power device all tests are carried out up to 400 V. Thus, the employed GaN diode has been replaced by a SiC diode, since the blocking capability of the newly developed GaN diode is limited beyond 300 V. Fig. 7.9 show a comparison of the converter efficiency based on the investigated normally-off GaN HEMT using GaN and SiC SBDs. As shown, the converter efficiencies are almost identical for both GaN and SiC diodes. Fig. 7.10 demonstrates the efficiency curves of the IBC based on Si, SiC and GaN power transistors using the SiC Schottky diode C3D08065A [113].

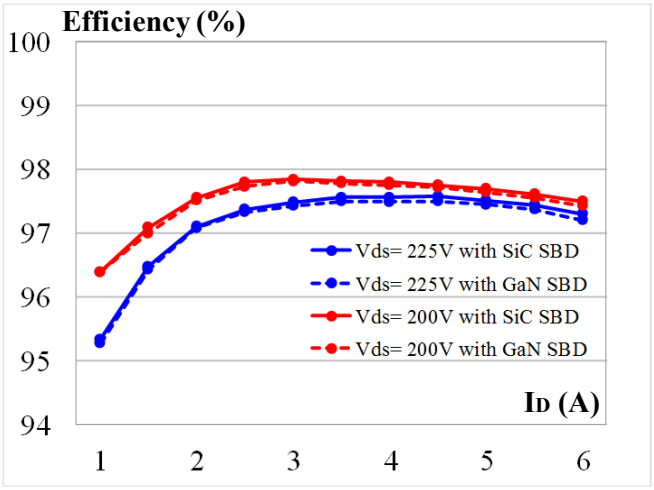


Fig. 7.9 Comparison of efficiency of the IBC based on GaN HEMT for both GaN and SiC SBDs. V_{DS} is set at 200V and 225V. I_D is increase from 1 to 6A. Switching frequency is 200 kHz.

The converter with the normally-off GaN device reveals an efficiency improvement over the converter with the SiC MOSFET and SJ-MOSFET up to 200 V, which is due to the GaN device losses improvement. However, as the input voltage is increased from 200 V to 230 V, the converter efficiency drops by 1%. A 97.8% total power efficiency of the implemented converter employing the normally-off GaN device was measured at 1.6 kW (0.8 kW per switch). However, as the input voltage is increased from 200V to 230V (Fig. 7.8d and Fig. 7.10), the power losses in the GaN HEMT will substantially rise. The efficiency (because of losses in S_1 and D_1) is decreased from 97.8% at 200 V to 97.3% at 230 V. The power loss at 6 A switched current is almost two times higher when the input voltage is increased by 25 V. It is not clear what exactly causes the transistor to behave so radically different beyond 225V. Consequentially, the conduction losses in the GaN HEMT become higher and result in substantial reduction in the efficiency of the whole converter. Obviously, the efficiency of the converter based on the cascode GaN HEMT is the highest with 98.7% measured at 360V. Fig. 7.11 shows the final results in this work, it is the converter power losses in percentage at 1.2 kW output power conditions and 200 kHz switching frequency. The largest power losses in the IBC are measured by using the SiC MOSFET "SCT2120AF", while the difference in losses between the other transistors is almost negligible. The inductors losses and the conduction losses of the diode have a significant contribution to the total losses, while the lowest power losses occur during the turn-off in the transistor and the Schottky diode. The $P_{L,Ton}$, $P_{L,Toff}$ and $P_{L,TCon}$ represent the power losses in the transistor dur-

ing turn-on and turn-off, the conduction interval, respectively. $P_{L,Doff}$ and $P_{L,DCon}$ are the losses in the diode during turn-off and the conduction interval. Lastly, the power losses in the inductors are denoted by $P_{L,L}$.

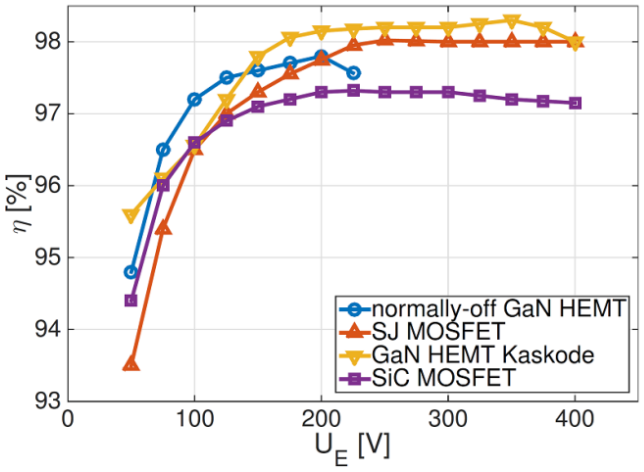


Fig. 7.10 Efficiencies using different power transistors at 200 kHz and 6A output current conditions.

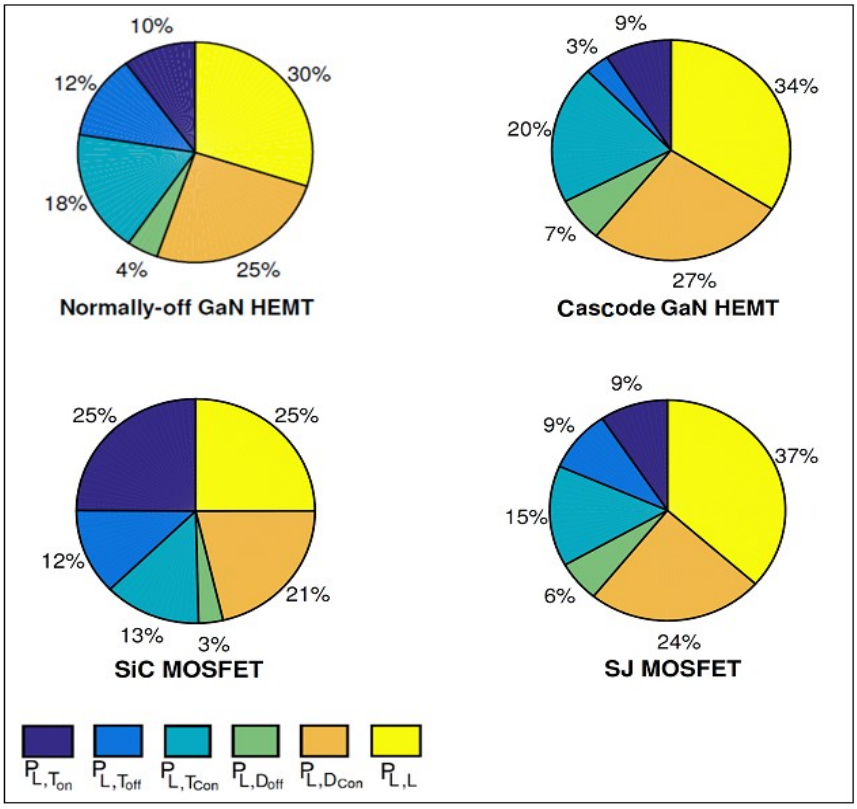


Fig. 7.11 Converter power losses in % at 1.2 kW output power conditions and 200 kHz switching frequency.

8 Conclusion

The conclusion of this thesis consist of different parts summarized as the results of each chapter as follows: The first step of the work was the reconstruction of existing test stand, which was implemented a few years ago and employed to investigate high voltage IGBT devices. This test stand has been made for the investigation of newly developed GaN power devices. However, only double pulse tests are conducted using this test stand and it was not possible to use it in continuous operation. Thus, a new FPGA-based control platform was used, which is employed in the characterization and application of the newly developed GaN power devices at different operation modes. Parallel to this, the design of suitable gate driver used to drive the normally-on and normally-off GaN power HEMTs was conducted. The second part of this thesis consists of testing and characterizing new GaN power HEMTs. The static and dynamic characteristics of 400V and 600V normally-on and normally-off GaN HEMTs are presented. Based on experimental results, switching transients are analyzed varying current, DC voltage and gate resistance. It is demonstrated that the switching capability of the new devices is promising, because they have a low gate charge and can operate at very high switching speeds. However, they reveal increased dynamic on-state resistance. This problem must be addressed in order to make the devices available for competitive converter operation.

In order to investigate the dynamic on-state resistance, a new measurement method employed to extract the dynamic R_{DSON} of GaN HEMTs is proposed. The method uses a clamping circuit. This circuit allows an accurate measurement of R_{DSON} from 100ns after turn-on to any arbitrary time at high switching frequencies up to 1MHz. Unlike the state-of-the-art technique, the proposed circuit has the advantage that no differential voltage probe is required to measure the on-state voltage and no external supply voltage is required. Moreover, a blocking voltage of up to 600 V can be clamped because of the use of a high voltage SiC Schottky diode. However, the proposed circuit introduces a voltage offset to the measured V_{DSON} value that has to be compensated. The achieved measurement results show that high off-state voltages (V_{DS}) and high drain currents contribute significantly to the increase of the dynamic R_{DSON} in GaN HEMTs. This remains a challenge for GaN technology, and a focus of current device research and development. Using the clamping circuit, the trapping effect phenomenon in the proposed normally-on and normally-off GaN HEMTs are investigated. The experimental results demonstrate the principal capability of the proposed transistors to operate at high switching frequencies. Nevertheless, by switching GaN devices in continuous conduction mode over a frequency range from 50 kHz up to 400 kHz, an increase in the on-state resistance R_{DSON} is observed. The experimental results clearly show that in addition to the off-state voltage, the number of switching transients also plays a substantial role in the increase of on-state resistance.

A possible explanation is that hot carrier injection during the switching events leads to a reduction of the channel charge carriers, which results in current collapse and increase of R_{DSON}. The GaN-HEMT structures show approximately an increase of 1.6 to 1.7 times of the static R_{ON} by increasing the temperature from 25°C to 150°C. This gives a substantial advantage in thermal system design as compared to using a Si-based SJ-MOSFET with increase of 2.9 time of R_{ON} under same conditions. Overall, problems and issues such as current collapse and low positive threshold voltage for normally-off

operation have to be overcome to accomplish the required level of stability and robustness for deploying the normally-off GaN HEMT in an industrial application. In order to use GaN devices in buck converter, two GaN and SiC diodes rated at 600V/8A are investigated in different combinations with four different 600V power transistors based on Si, SiC and GaN. For each combination, the dynamic impact of the transistor on the diode and vice versa is investigated. The static and dynamic on-state resistance is evaluated at different temperatures up to 200° C. The experimental results can be summarized in two parts. First, depending on which transistor has been employed in the combination, the switching performance of the SBD may be significantly limited. This can be seen for example using the cascode GaN HEMT in combination with GaN diode, where the transients of the GaN diode are at least two times faster than in the case of SiC MOSFET in combination with GaN or SiC diodes. However, such operation results in extremely high dv/dt and di/dt that causes substantial and inacceptable high frequency oscillations. Secondly, both GaN and SiC SBDs demonstrate a good switching performance, similar damping coefficients during the transients and approximately similar reverse recovery behavior. However, the investigated GaN diode is characterized by a larger on-state voltage drop than the commercial state-of-the-art SiC diode. Robustness of GaN power devices is another important topic discussed in this work.

The short-circuit capability of four different 600 V power transistors based on Si, SiC and GaN have been investigated. To do the analysis, single pulse destructive tests are carried out. It is demonstrated that the increase of the dc bus voltage leads to a decrease in short-circuit withstanding time and thus the critical energy of the power devices. Regarding the short-circuit robustness, different results are achieved and summarized: 1) the 650V SiC MOSFET reveals a good short-circuit capability (13µs at 400V). Current tails after the turn-off are observed, while all other power devices do not show such a phenomenon. 2) The normally-off GaN HEMT has less short-circuit withstand capability than the other devices. Test results offer an indication that the short-circuit failure first occurs in the gate drain region, but further studies in combination with device simulation need to be conducted to clarify this point. 3) The second observation for the normally-off GaN HEMT is the partial damage of the gate, a behavior similar to what was observed during the test of the SiC MOSFET. 4) Since it was not possible to observe the internal gate-source voltage and current of the cascode GaN HEMT, an analysis of the short-circuit failure is difficult. However, similar to the investigated normally-off HEMT, the transistor does not demonstrate sufficient short-circuit robustness.

Finally, an interleaved buck converter based on normally-off GaN HEMT and GaN Schottky diode is presented. The converter was successfully operated at 225V input voltage and 11.6 A load current. The switching frequency was varied from 50 to 500 kHz. Up to 200V, the converter reveals higher efficiency with the normally-off GaN device than the using of SiC MOSFET and SJ-MOSFET. The highest efficiency measured was at 200V/3A, which is 97.8%. However, a remarkable reduction of the efficiency has been observed by increasing the drain current and drain-source voltage of the GaN HEMT. As the drain-source voltage rises from 200 V to 230 V, the converter efficiency suffers a 0.6% reduction. Such rapid reduction is probably due to the device degradation, which is suggested because of the cumulative trapping of hot electrons during the transients in the GaN channel. The inductors losses and the conduction losses of the diode have a large contribution to the total losses. According to the different investigations and the results achieved during this dissertation, it is concluded that the main challenge facing GaN developers is the increase of the dynamic on-state resistance at high dynamic conditions. As a second challenge is the problematic of the electromagnetic interference (EMI)

due to the high-speed transients of GaN power devices, especially when operating at high-switching frequencies. Nevertheless, in the meantime some industrial manufacturer such as Panasonic, GaNSystems and Transphorm have reported that they have already solved the problems causing device degradation that occur due to the trapping phenomenon in GaN devices. Undoubtedly, that can be the new advance in the GaN technology which is what power electronics has been waiting for.

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12 Abbreviations

WBG	*Wide Bandgap*
DPT	*Double Pulse Test*
DSO	*Digital Storage Oscilloscope*
FPGA	*Field Programmable Gate Array*
VHDL	*VHSIC Hardware Description Language*
V_{GS}	*Gate Voltage*
I_D	*Drain Current*
I_F	*Diode Forward Current*
V_{DS}	*Drain Source Current*
V_{BR}	*Breakdown Voltage*
V_{RBV}	*Reverse Blocking Voltage*
t_f	*Falling Time*
t_r	*Rising Time*
t_{OFF}	*Off Time*
t_{ON}	*On Time*
R_g	*Gate Resistor*
R_{ON}	*Static On-state Resistance*
R_{DSON}	*Dynamic On-state Resistance*
V_{DSON}	*Voltage On-state Resistance*
BW_{max}	*Maximum Bandwidth*
V_{gate}	*Gate Voltage*
Q_g	*Gate Charge*
Q_{rr}	*Reverse Recovery Gate Charge*
P_{gate}	*Gate Power*
$P_{quiescent}$	*Quiescent Power*
$P_{transient}$	*Transient Power*
f_{sw}	*Switching Frequency*
$R_{g\_equivalent}$	*Equivalent Gate Resistance*
C_{iss}	*Input Capacitance*
CGD	*Conventional Gate Driver*
RGD	*Resonant Gate Driver*
V_{gate}	*Gate Voltage*
FOM	*Figure-of-Merit*
L_D	*Drain Parasitic Inductance*
L_{SS}	*Stray Parasitic Inductance*

L_S	*Source Parasitic Inductance*
L_{DC}	*DC Source Parasitic Inductance*
di/dt	*Current Derivative*
dv/dt	*Voltage Derivative*
$I_{D\text{-}SC}$	*Short-circuit Current*
$I_{D\text{-}SC\text{-}MAX}$	*Maximum Short-circuit Current*
T_{SC}	*Short-circuit Time*
E_C	*Critical Energy*
GaN	*Gallium Nitride*
GaAs	*Gallium Arsenide*
AlGaN	*Aluminium Gallium Nitride*
AlGaAs	*Aluminum Gallium Arsenide*
SiC	*Silicon Carbide*
Si	*Silicon*
HEMTs	*High Electron Mobility Transistors*
HFETs	*Heterostructure Field-Effect Transistors*
2DEG	*Two-Dimensional Electrons Gas*
P_{sp}	*Spontaneous Polarization*
P_{pi}	*Piezoelectric Polarization*
MOVPE	*Metal Organic Vapour Phase Epitaxy*
UID GaN	*Unintentionally Doped Gallium Nitride*
TLM	*Transmission Line Matrix*
SBDs	*Schottky Barrier Diodes*
MOSFET	*Metal–Oxide–Semiconductor Field-Effect Transistor*
IGBT	*Insulated-Gate Bipolar Transistor*
E_g	*Bandgap Energy*
μn	*Electron Mobility*
v_{sat}	*Saturation Velocity*
ε_r	*Dielectric Constant*
λ	*Thermal Conductivity*
d-mode	*Depletion Mode*
E_C	*Conductance Band*
E_V	*Valence Band*
E_F	*Fermi level*
e-mode	*Enhancement Mode*
d-mode	*Depletion Mode*
HVPE	*Hydride Vapor Phase Epitaxy*
SOIC	*Small Outline Integrated Circuit*
IBC	*Interleaved Buck Converter*

CCM	*Continuous Conduction Mode*
D	*Duty Cycle*
$P_{L,Ton}$	*Transistor Switching Power Losses at Turn-on*
$P_{L,Toff}$	*Transistor Switching Power Losses at Turn-off*
$P_{L,TCon}$	*Transistor Conduction Power Losses*
$P_{L,Doff}$	*Reverse Recovery Power Losses*
$P_{L,DCon}$	*Diode Conduction Power Losses*
$P_{L,L}$	*Inductor Total Power Losses*

13 Appendix

A 1 Gate Driver

Gate Driver IC	Manufacturer	V_{in} (V)	I_{Peak} (A)	t_{Rise} (ns) / t_{Fall} (ns)	t_{dealy1} (ns) / t_{dealy2} (ns)
EL7158, [54]	Intersil	4.5-18	6	12/12@2nF	22/22@2nF
TC4451, [56]	Microchip	4.5-18	6	30/32@15nF	44/44@15nF
IXDD609, [55]	IXYS	4.5-18	9	20/15@10nF	42/40@10nF
FAN3111, [60]	Fairchild	4.5-18	1.4	9/8@470pF	15/15@470pF

Table A1.1 Comparison of different ICs driver parameters

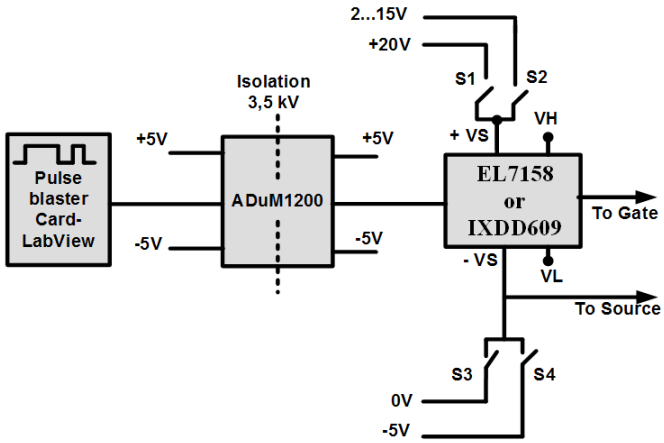


Fig. A1.1 Schematic of the conventional gate driver based on 9A MOSFET driver "IXDD609."

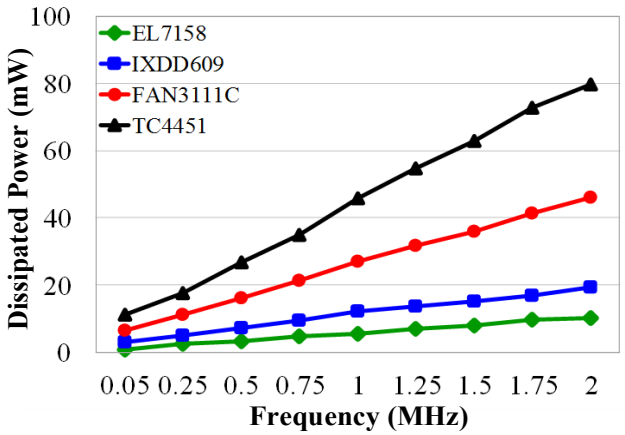


Fig. A1.2 Measured dissipated power for the different drivers at 100 pF capacitive load and 8 V input. Switching frequency varying from 50 kHz to 2 MHz (T = 25° C).

A 2 FPGA-based Hardware

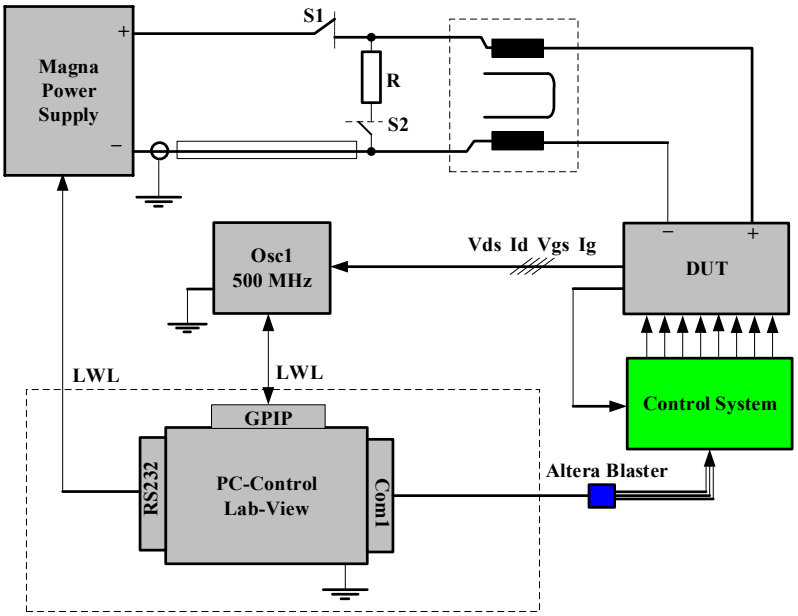


Fig. A2.1 Structure of the improved test stand including the proposed FPGA-based control system

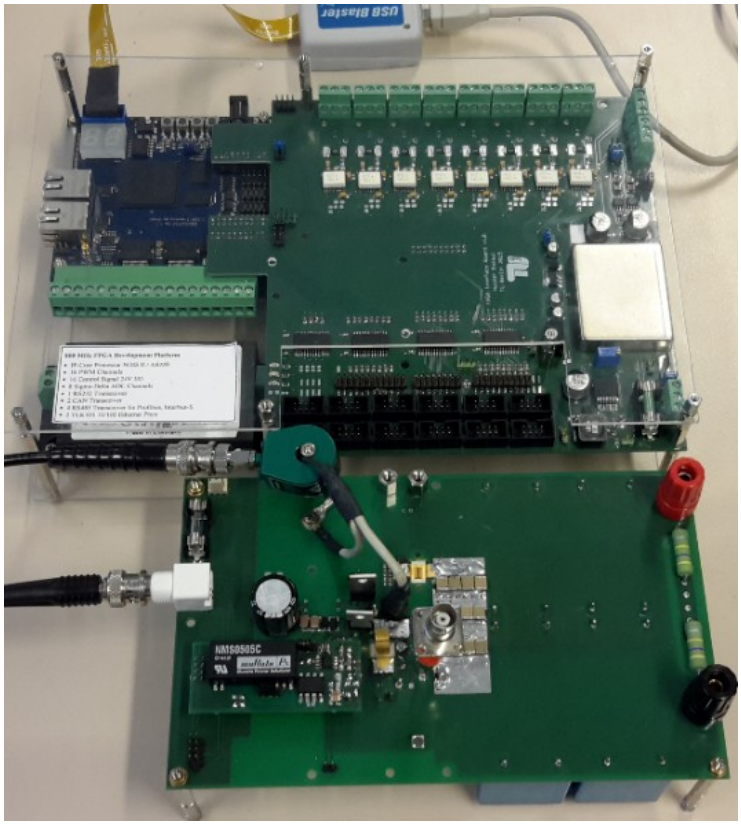


Fig. A2.2 FPGA System including the dynamic test circuit and the proposed clamping circuit

A 3 Short-circuit Test

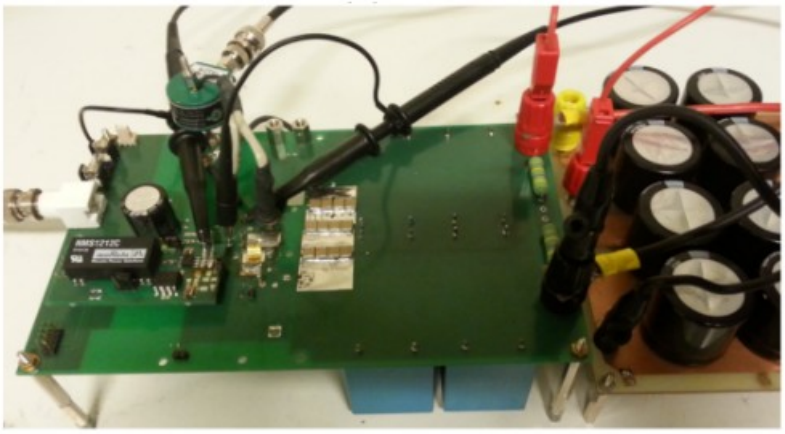


Fig. A3.1 Hardware implementation of the short-circuit test circuit

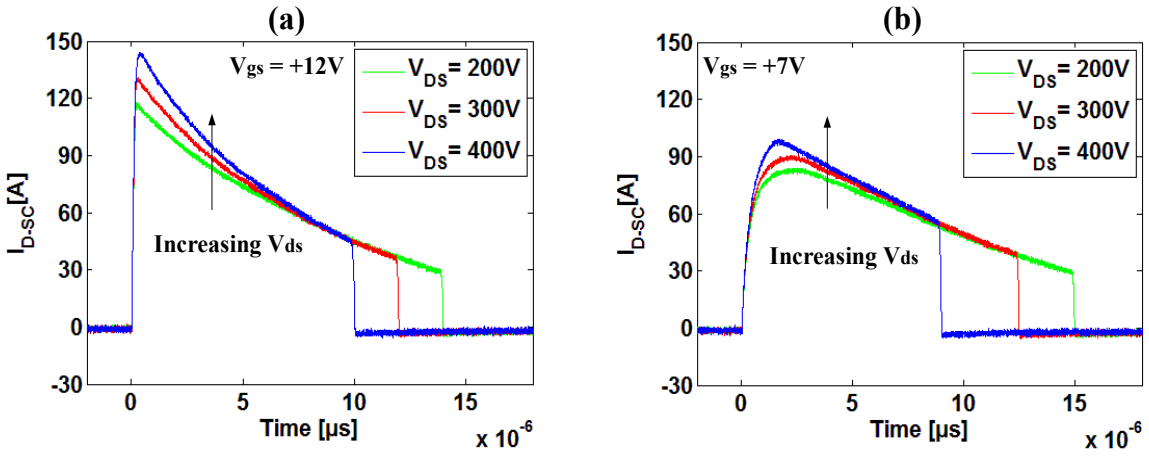
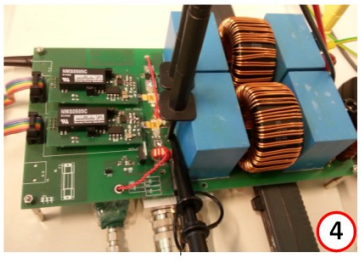
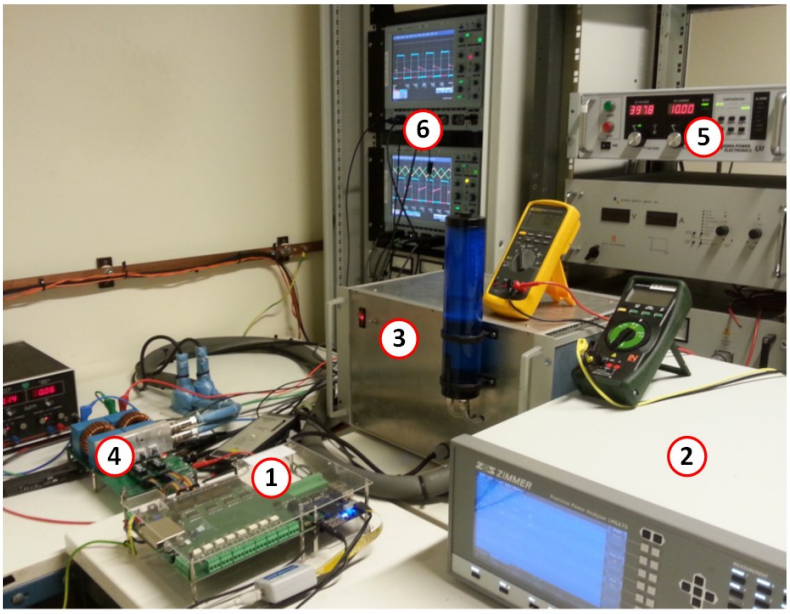


Figure A3.2 Experimental results of the short-circuit test for the Super-junction MOSFET with T_{SC} up to 15µs. Gate source voltage V_{GS} = 12V and 7V. DC bus voltage V_{DC} = 200V, 300V, 400V. T_{case} =25 ° C and Rg = 4.7 Ω. Short-circuit time T_{SC} is vayring from 10 to 15 µs.

A 4 Experimental Test Setup



(1) FPGA-based Control System
(2) ZES Zimmer LMG670
(3) Calorimetric System
(4) Prototype DC-DC Converter
(5) Magna Power TSA750
(6) 2xOsc LeCroy 350 MHz



Figue A4.1 Experimental setup including the converter prototype

A 5 Dynamic Behavior of the Normally-off GaN HEMT in CCM

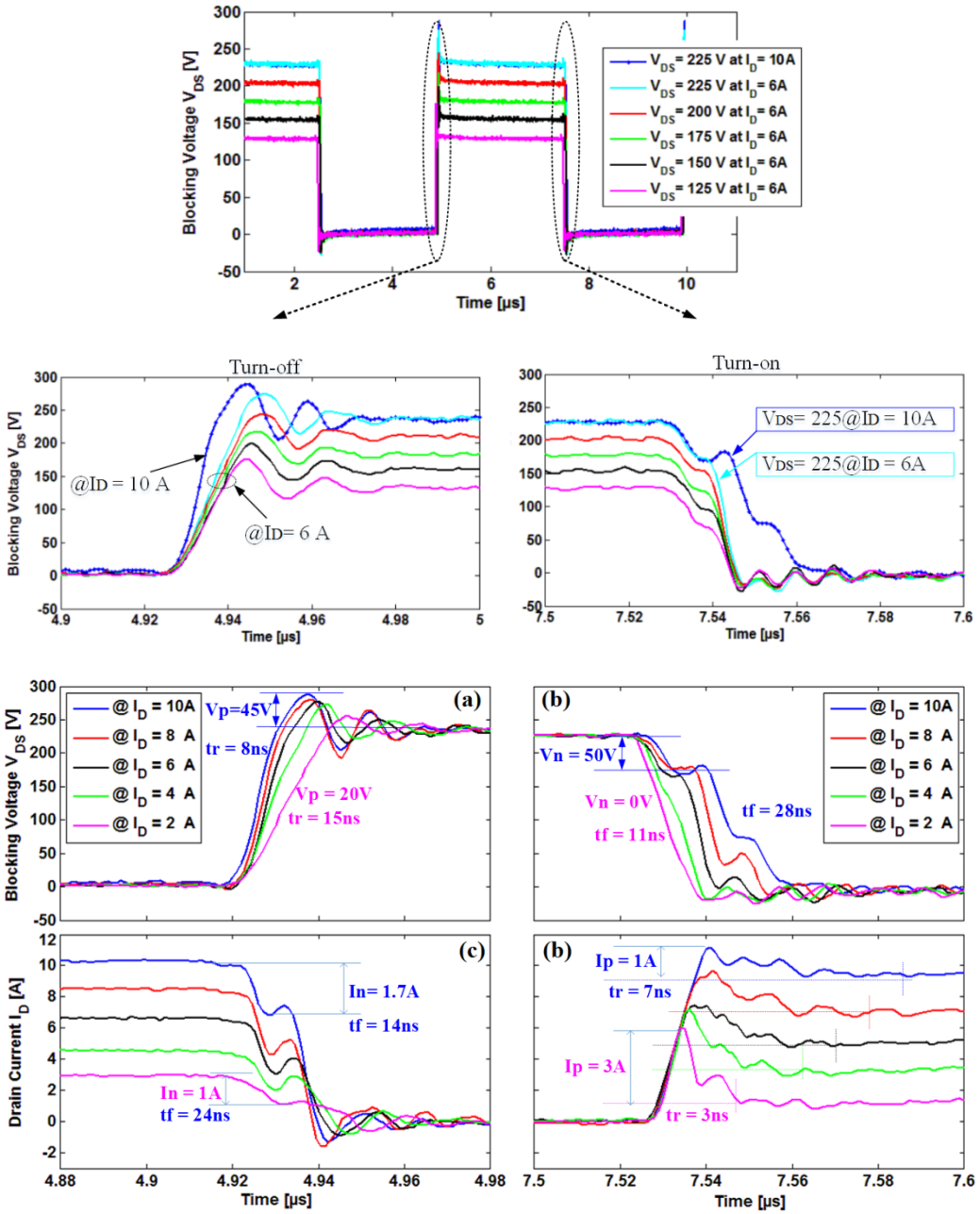


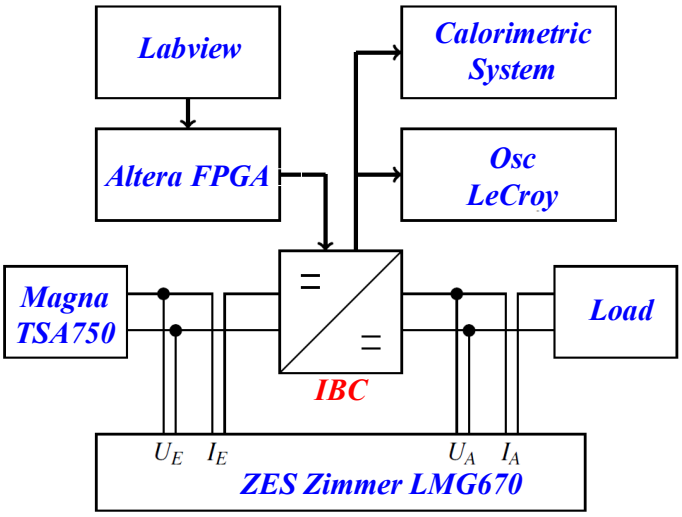
Figure A5.1 Measured voltage and current transients of the normally-off GaN HEMT at 225 V blocking voltage. Drain current I_D is changed 2A stepwise from 2A and 10A. Switching frequency = 200 kHz. R_G = 6.3 Ω. Test temperature T =25° C.

Vp: the voltage difference between the peak voltage measured during the turn-off and the steady-state value of V_{DS} as seen in Fig. A5.1a

Vn: expected drop voltage at the inductive load during turn-on, which creates a voltage notch in the V_{DS} transient as seen in Fig. A5.1b

A 6 Power Losses Evaluation for the GaN-based IBC

Power losses of the investigated power devices are determined by using a calorimetric measuring system (developed at the Power Electronics Department, TU Berlin). For this purpose, the power devices in the IBC are mounted on a liquid-cooling heat sink. The system regulates the temperature of the liquid (water) to a previously given value and thus the temperature change of the power devices can be determined. From the change of the temperature, the power losses can be calculated. The calorimetric system has two essentials tasks: On the one hand it cools the power devices and on the other hand it determines the power losses.



A6.1 Schematic of the test structure for obtaining the converter power losses

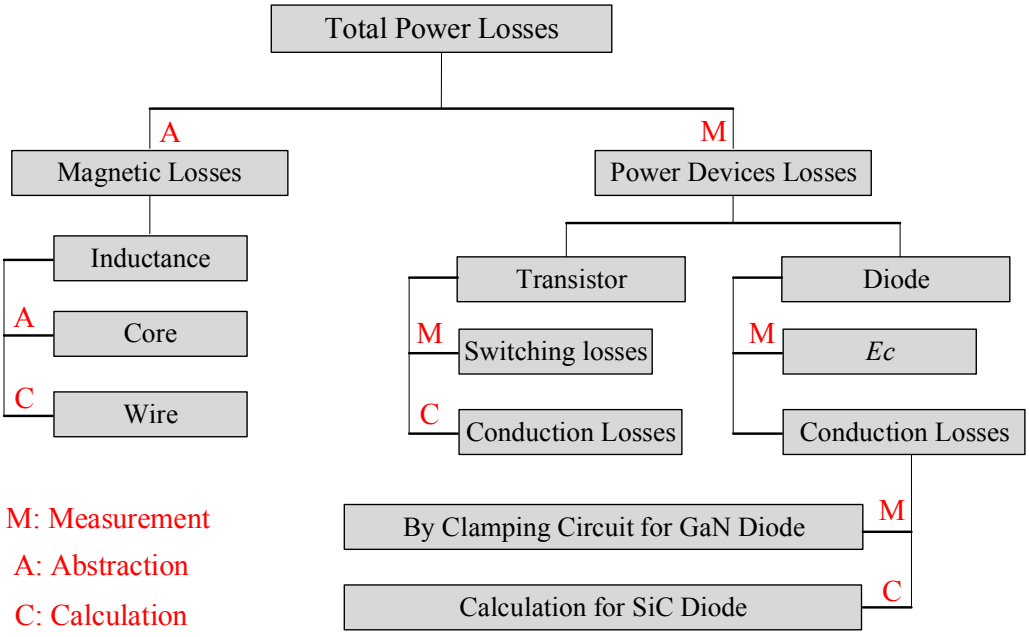


Fig. A6.2 Schema of the power losses evaluation of the interleaved buck converter

Total power losses in the power devices ($P_{V,total\_calorimetric}$):

$$P_{V,total\_calorimetric} = P_{V,2diode} + P_{V,2transistor}$$

$P_{V,total\_calorimetric}$: Total power losses measured by the calorimetric system.
$P_{V,2transistor}$: Switching and conduction losses in the two transistors.
$P_{V,2diode}$: Switching and conduction losses in the two diodes.

Essentially no switching losses occur in the schottky diode. However, the capacitance stored energy E_c will add some losses; E_c is usually given in the datasheet. By multiplying the measured forward current I_F with the drop voltage U_F the conduction power losses can be obtained:

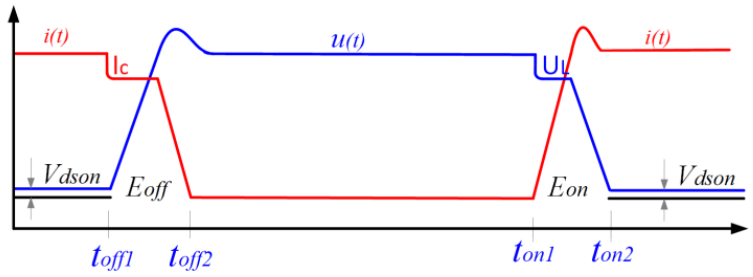
$$P_{V,con} = I_F^2 \cdot R_{on} \cdot (1-D) = I_F \cdot U_F \cdot (1-D), \qquad \text{// D is the duty cycle}$$

Since the total power losses ($P_{V,total\_calorimetric}$) and power losses in the diodes ($P_{V,2diode}$) are already determined the power losses in the transistors ($P_{V,2transistor}$) can be calculated:

$$P_{V,2transistor} = P_{V,total\_calorimetric} - P_{V,2diode}$$

The switching losses in each transistor ($P_{V,SW}$) are calculated base on the measured V_{DS} and I_D waveforms. By integrating the V_{DS} . I_D over the switching times the switching energies E_{on} and E_{off} can be obtained:

$$P_{V,SW} = f \cdot \left[\int_{t_{on1}}^{t_{on2}} u(t) \cdot i(t) dt + \int_{t_{off1}}^{t_{off2}} u(t) \cdot i(t) dt \right] = f \cdot \left[E_{on} + E_{off} \right]$$



Since the power losses ($P_{V,2transistor}$) and the switching losses in each transistor ($P_{V,sw}$) are evaluated the conduction losses ($P_{V,con}$) can be calculated as the following:

$$P_{V,2transistor} = 2 \,.\, P_{V,con} + 2 \,.\, P_{V,sw}$$

Also, the conduction power losses of each transistor ($P_{V,SW}$) can be evaluated by:

$$P_{V,con} = V_{dson} \,.\, I_D \,.\, D$$

D is the duty cycle ($D = T_{on}/T_s$).
V_{dson} is measured using the clamping circuit.

The total power losses of the converter is obtained by measuring the input and output power using the LMG670 as shown in Fig. A6.1. So, the total magnetic losses in the inductors ($2 \cdot P_{V,L}$) are in the end the difference between the total losses of the converter and the total losses of the power devices. Sendust magnetic based inductors have been used in both paths of the IBC (Chang Sung CS572060E28 chokes [163]). Sendust is an alloy consisting of iron, silicon and aluminum. It characterizes a high permeability and can be used at high temperatures. For winding a copper wire has been used.

The total power losses in the inductors:

Total magnetic losses = 2 x $P_{V,L}$	$P_{V,L} = P_{Core} + P_{DCR} + P_{ACR}$
DC winding losses	$P_{DCR} = I_{L,DC}^2 \cdot R_{DC}$
AC winding losses	$P_{ACR} = I_{L,AC}^2 \cdot R_{AC}$
Core losses	$P_{Core} = K \cdot f^x \cdot B^y \cdot V$ *K: Constant of the core material.* *f: Frequency in kHz* *B: Magnetic flux density in Tesla* *V: Effective core volume* *x, y: Depending on core material*