Interdigitated Back-Contact Silicon Heterojunction Solar Cells: Development of Patterning Techniques and Applications in Tandem Devices

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Contents

1 Introduction

Humankind's progress from the start of the industrial age to today's steady global decline in poverty has led to a drastic increase in worldwide energy demand. This requirement cannot be met by the utilisation of fossil fuels due to their increasing scarcity and severe environmental impacts (e.g. emission of greenhouse gases and devastation of ecosystems). Instead, finding an alternative, sustainable energy supply is inevitable to guarantee liveable conditions for posterity and to counteract the accelerated extinction of species [1].

Within their fifth assessment report in 2013 [2], the Intergovernmental Panel on Climate Change (IPCC), which is the basis of the United Nation's Paris Agreement of 2015 [3], predicted a global temperature rise of 1.5–4.5 °C until 2100 if the concentration of carbon dioxide in the atmosphere as compared to the pre-industrial era (1850–1900, as per definition in the report) is doubled. Recent investigations preceding the upcoming sixth report to be released in 2021, however, predict that these estimations were far too optimistic and even the restriction to only 1.5 °C increase in global average temperature necessitates tremendously larger efforts than expected [4]. Instead, leading climate scientists working on the next iteration of said report declare that reassessed global climate models predict the increase in global temperature to be rather 2.8–5.8 °C [4]. Therefore, taking actions is urgent and climate change will remain one of humanity's major challenges for decades to come.

Concerning power supply in this broader context, renewable energies provide the only sustainable solution, and regarding electrical energy in particular, both wind power and photovoltaics (PV) will be major contributors. PV is one of the fastest growing sources of renewable energy and allows for competitive power generation, having reached grid parity (i.e. the generation cost for 1 kWh of electrical energy is as high as the electricity price) in multiple countries by now [5,6]. Today, owing to its outstanding electrical properties and dominance in microelectronics, silicon (Si) is by far the most widely used semiconductor material in PV with a worldwide market share of more than 95% [7]. The first Si-based solar cell was introduced in 1954 by CHAPIN *et al*. and yielded a power conversion efficiency (PCE) of 6% [8]. The PCE is a measure of how much of the incident solar irradiation is converted into electrical energy. Since then, several improvements to the original design have been made.

Texturing the wafer surface with random pyramidal structures increased the short-circuit current density (j_{sc}) by means of better light in-coupling, enhanced internal reflexions, and thus increased photon absorption probability [9,10]. The introduction of anti-reflective coatings (ARCs) that take advantage of the principle of destructive interferences and thereby reducing the reflectance for certain wavelengths to a minimum (depending on the reflective index of the ARC) [11,12] enabled again a further enhancement of the j_{sc} and thereby PCEs of slightly above 19% as early as in 1984 [13]. As also noted by the authors of that study, further attempts on improving the PCE of solar cells must focus on increasing their open-circuit voltage (V_{oc}). Provided that the bulk material is defect-poor, a feasible approach for achieving high V_{oc}s is passivating the wafer's surface, either chemically by decreasing the density of surface states, which act as recombination centres, or by means of field-effect passivation [14]. Silicon oxide (SiO_x) and hydrogenated amorphous Silicon (a-Si:H) are commonly used as passivation layers, of which the latter usually yields better passivation as first described in 1979 by PANKOVE and TARNG [15]. While the V_{oc} of a solar cell with non-passivated surface is limited to about 640–650 mV [16], its theoretical potential is as high as 761 mV [17] when introducing surface passivation, which makes this a highly desirable feature for high-efficiency devices.

Combining surface passivation with low-temperature deposition techniques (i.e. limited to about 200 °C) and thus lowering the production costs gave rise to a new type of solar cell architecture: the silicon heterojunction solar cell (SHJ); or heterojunction with intrinsic thin-layer (HIT) as it was originally called [18]. In this concept, sharp interfaces are formed between each layer instead of a diffused p/n-junction and contacts. It evoked remarkable scientific interest and underwent considerable improvements and adaptations in the past two decades [19], resulting eventually in a record efficiency of 25.1% [20] and V_{oc}s as high as 750 mV [21] with the latter almost entirely exploiting this solar cell parameter's theoretical potential.

The interdigitated back-contact (IBC) solar cell, introduced in 1977 [22] and featuring both electrodes on the rear side of the device, is another highly attractive concept. IBC solar cells yield very high j_{sc} values because their front side, which can be optimised exclusively for optical properties, is free of any opaque contacts and therefore free of shading losses. Theoretically, j_{sc}s as high as 46 mA/cm² are achievable with Si-based solar cells [23]. However,

they are practically limited to 43.3 mA/cm² when fundamental loss mechanisms, such as free-carrier absorption and Auger recombination, are taken into account [17].

The combination of both the SHJ and IBC concept in order to utilise their respective advantages (i.e. high V_{oc}s and j_{sc}s) was first realised in 2007 by Lu *et al*. [24]. Although the achieved PCE was very low (11.8%), the functionality of the concept could be proved and apparent design flaws have been outlined. In 2011, this concept's PCE surpassed the 20% mark [25,26] and in 2014, a PCE of more than 25% had been achieved [27], mainly by improving the passivation quality and reducing the resistive losses at the contacts. Currently, Kaneka's back-contacted SHJ is the highest efficient single-junction Si wafer-based technology with a quick succession of presented new record PCEs from 26.3% [28] to 26.6% [29] and 26.7% [30]. Moreover, impressive as these results might be, the hitherto established and vastly used contact preparation of these solar cells is conducted by lab-based photolithographic processes, which are complex, lengthy, and expensive and thus not applicable for industrialisation.

Developing a simplified and cost-effective fabrication process while maintaining exceptional solar cell properties is therefore of utmost importance to support the wide deployment of this promising technology. As early as in 2007, i.e. shortly after its introduction, such a simplified *in-situ* patterning process for IBC SHJ solar cells incorporating the combined use of shadow-masks and plasma-etching [31] was proposed [32] and a similar process has recently achieved a PCE of close to 23% [33]. Other approaches first relied on the successive deposition through dedicated masks for each doped layers [34–37], but have been later simplified to a one-mask approach, with the tunnel-junction IBC SHJ [38,39] being currently the most successful photolithography-free architecture, yielding a recently reported PCE of 25% [40]. Another notable alternative technique is laser patterning, which has already become a key technology in thin-film based PV [41–43]. Although in theory a lean process for patterning doped layers, it usually comes at the cost of comparably lower V_{oc} values due to laser-induced damage of the crystalline silicon's (c-Si) surface [44,45]. This can be avoided by elaborate techniques, such as implementing a sacrificial stack of multiple layers with varying optical properties at the laser-illuminated side [46], but this increases the process complexity again. The thus far highest efficiency for a solely laser-patterned IBC SHJ is reported to be 22.5% [47], mainly limited by a low fill factor (FF).

Low FF's are, apart from an increased process complexity, another often found drawback of IBC SHJ solar cells, which usually suffer from lower FFs as compared to their bifacially contacted counterparts [35]. This is due to two reasons: (i) the restriction to only one side of the wafer for contact formation; and (ii) the nature of the p-type contact that typically consists of p-doped a-Si:H and an n-type transparent conductive oxide (TCO), usually indium tin oxide (ITO), resulting in a recombination contact [48,49] between these two layers, which leads to a considerably higher contact resistivity than that of the n-type contact on an n-type wafer [39,50]. It is worth mentioning that the latter fact is also true for standard SHJ solar cells. Indeed, the loss mechanisms of back-contacted and standard SHJ solar cells are quite similar [36]. A plethora of different approaches to circumvent this low-FF issue have been adopted, which can be categorised as either (i) tuning the passivation layer thickness to reduce the energetic barrier for minority charge carriers [51–53]; (ii) choosing high doping concentrations and/or TCOs with higher work functions (WFs) to form more efficient recombination contacts [49,54–57]; or (iii) omitting any TCO and choosing a direct metallisation suitable for p-type a-Si:H [58–60]. The highest reported FF of an SHJ solar cell to this day is Kaneka's back-contacted record device with an astonishing 84.9% [30].

The three main parameters (V_{oc}, j_{sc}, and FF) introduced above determine the PCE of a solar cell. The theoretical PCE potential of a single-junction solar cell based on c-Si was first determined to be slightly above 30% [23] and was later reassessed to be 29.4% [17] by taking relevant wafer thicknesses, the illumination with the AM1.5g standard spectrum (instead of mere black-body radiation), and fundamental loss mechanisms such as increased Auger recombination at high illumination intensities [61] into account. In order to overcome this limitation, the utilisation of multiple absorbers (so-called multi-junction or tandem solar cells) is necessary. For an infinite number of stacked solar cells, a theoretical maximum PCE of 86.8% can be achieved, or, for a more practical application, with a two-semiconductor device the theoretical PCE is already as high as 42.2% [62]. This increase, compared with single-junction devices, arises from reduced thermalisation losses due to an enhanced utilisation of the incident electromagnetic spectrum [63]. With its band gap of 1.12 eV (at 300 K), Si is an almost optimal choice for a bottom cell in a two-absorber application [62]. Owing to their tuneable band gap in the range of approximately 1.5–1.7 eV, perovskite-based solar cells make for an almost ideal top-cell counterpart [64]. Indeed, very

high PCEs almost matching [65,66] or even exceeding [30,67,68] that of the most successful Si-based single-junction solar cell have been reported, with a current record of 28.0% [30,68].

In terms of interconnecting both subcells, two concepts have been widely established: (i) the two-terminal configuration (2T) comprising a monolithic device architecture with only one electron and hole contact where both subcells are interconnected in series; and (ii) the four-terminal configuration (4T) where both subcells feature their own respective electron and hole contact. Both these 'classic' interconnection schemes have specific advantages and drawbacks: 2T tandems with their monolithic device architecture feature a rather simple fabrication route, but require current-matched subcells [69], which is, although achievable in a lab-based environment, seldom the case in a real-world application with fluctuating weather conditions [66]. 4T tandems, on the other hand, do not necessitate current matching because their subcells are electrically decoupled, but this comes at the cost of more complex fabrication and additional parasitic absorption within relatively thick interconnection layers.

A so far little investigated approach is the three-terminal configuration (3T). Here, both subcells feature an electron (or hole) contact of their own and share a common hole (or electron) contact. This leads to a monolithic device and electrically decoupled subcells at the same time, combining thus the advantages of 2T and 4T tandems. The third terminal can be implemented as a middle contact [70–72], but this inevitably leads to parasitic absorption within this layer, especially since thicknesses of several 100 nm are needed for lateral current transport [71]. Therefore, it is more favourable to use an IBC bottom cell, circumventing this issue. These 3T IBC tandems have been introduced in 2000 [73] and experimentally realised for III–V-semiconductors, such as gallium arsenide (GaAs) and gallium indium phosphide (GaInP), in combination with Si [74]. To this date, although a plethora of theoretical studies have been published [75–79], no experimental realisation of such device comprising perovskite and Si subcells has been presented.

This thesis reports on the development and optimisation of different fabrication techniques for IBC SHJ solar cells and their characterisation. Main focuses are improving the device's FFs and V_{oc}s, and simplifying the preparation process. Furthermore, the first experimental realisation of a 3T IBC tandem solar cell is presented, and 3T IBC tandem devices are characterised in detail by means of optoelectronic measurements and electrical simulations. The contents of the chapters can be summarised as follows.

Chapters 2 and 3 give a comprehensive overview over the essential elements regarding the devices discussed in this thesis. Chapter 2 focusses on materials and interfaces as well as working principles of single-junction and tandem solar cells whereas chapter 3 covers fabrication and characterisation methods used during the course of this thesis.

Chapter 4 describes in-depth the manufacturing and optimisation of single-junction IBC SHJ solar cells. Two fabrication processes are discussed: a photolithography and a more industrially viable shadow-mask process, the latter relying on *in-situ* patterning. Along with a description of the overall improvements that are made towards optimising these two processes, the influence of different passivation schemes and thicknesses, surface morphology, and different metallisation schemes are discussed with a strong focus on series-resitance related electric power losses. The chapter is complemented by electrical equivalent circuit simulations.

Chapter 5 presents the first experimental realisation of 3T IBC tandem devices combining perovskite and Si subcells. Optical and electrical characterisations of these devices are presented and discussed. An improved understanding of the electrical behaviour of both the entire device and the mutual dependence of the separate subcells is derived from electrical equivalent circuit simulations. Limitations of these proof-of-concept devices and possible optimisation routes are laid out and a semi-empirical model is used to estimate the PCE potential of such devices.

In **chapter 6**, a broader overview over the prospects of IBC SHJ solar cells both in single-junction and tandem devices is given, including a detailed comparison with other competing high-efficiency approaches, especially standard SHJ solar cells, which are very likely the main competitor of their rear-side contacted counterparts. Apart from that, other possible fabrication routes than those discussed in this thesis are presented and compared with respect to feasibility and achieved device performances.

Chapter 7 summarises the key findings of this thesis regarding the investigated optimisation approaches for the photolithography and shadow-mask process, and for the integration of IBC SHJ solar cells into 3T tandem devices. Furthermore, an outlook is given on the expected future development of these technologies.

2 Fundamentals

In the following chapter, the materials utilised in this thesis are introduced. Furthermore, the interaction of these materials when forming interfaces is described and the general working principle of solar cells (both single and multi-junction devices) is explained.

2.1 Materials and Interfaces

This subsection concentrates on all materials important for this thesis and on their interplay.

2.1.1 Hydrogenated Amorphous Silicon

Amorphous material lacks long-range order in its atomic lattice and is thus isotropic (i.e. its bulk properties are independent of the spatial direction) [80]. Amorphous Silicon (a-Si) is the amorphous phase of crystalline Silicon (c-Si). A schematic of both materials is depicted in Figure 2.1. The mean distance between adjacent Silicon (Si) atoms does not differ much for both materials, but in a-Si there are fluctuations in bond lengths and angles as well as additional dangling bonds (i.e. open Si bonds) [80]. The incorporation of hydrogen leads to the formation of hydrogenated amorphous silicon (a-Si:H), and sufficiently high hydrogen contents (C_H) allow for the passivation of dangling bonds [81,82]. This will, however, alter the material's microstructure and thus its physical properties [83,84]. Increasing C_H will increase the material's bandgap from 1.5 eV (without hydrogen) to a maximum of 1.9 eV, but will also lead to more disordered films by the formation of microvoids [85]. Excessive hydrogenation will further lead to film etching once the hydrogen concentration is saturated [81] and to the replacement of Si–Si with Si–H bonds because the latter are more stable due to a higher binding energy [86,87]. Another factor to consider is the film thickness: while for thicker layers, porosity and roughness increase [88], depositing very thin layers is challenging because the initial growth of a-Si:H is not spatially homogenous, leading to voids or columnar structures [80]. Lastly, the deposition temperature needs to be considered. Lower temperatures lead to an increased number of voids and thus inhomogeneity [89], but too high temperatures can induce epitaxial growth [90,91]. Both impacts are detrimental for the performance of the devices discussed here.

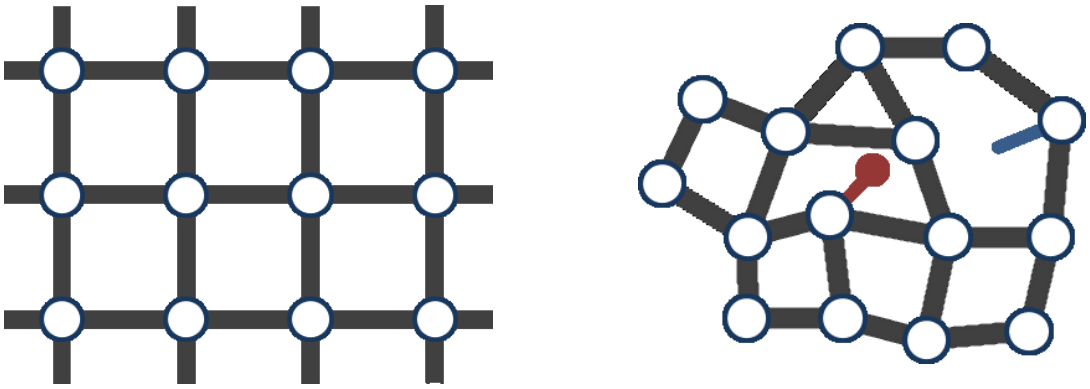


Figure 2.1: Simplified two-dimensional crystal lattices of a) crystalline silicon and b) hydrogenated amorphous silicon. Large hollow blue circles represent silicon atoms, solid red circles hydrogen atoms, and light blue lines dangling bonds. Reworked from [92].

So far, only intrinsic (i.e. nominally non-doped) material has been discussed. In Si solar cells, however, doped Si is also needed as hole and electron contacts. Although the doping efficiency is much lower, a-Si:H can be doped with the same materials as c-Si [93], i.e. phosphorous for n-type a-Si:H and boron for p-type a-Si:H (cf. next section for further details). Since the conductivity is also much lower than in c-Si [94], and therefore the contact resistivity is increased, the use of doped hydrogenated nanocrystalline (nc-Si:H) [95–98] or microcrystalline (µc-Si:H) [99] Si is highly beneficial both optically and electrically. However, with the herein used solely rear-contacted devices it is not possible to employ such material for both polarities because this leads to shunting (cf. section 2.2.3).

2.1.2 Crystalline Silicon

As opposed to a-Si:H, c-Si features a well-organised face-centred cubic crystal lattice (cf. Figure 2.1a for a simplified two-dimensional representation, displaying only the corner atoms). Every Si-atom is bond covalently to its four adjacent Si atoms in a tetrahedral structure with a bond angle of approximately 109° [12]. The lattice constant of c-Si amounts to 5.431 Å [100] and thus, 1 cm³ of pristine Si contains roughly $5 \cdot 10^{22}$ atoms. As a solid, Si features a band gap of 1.12 eV at 300 K [100]. However, being an indirect semiconductor, the valence band (VB, i.e. the energetically highest fully occupied energy band in equilibrium) maximum and the conduction band (CB, i.e. the energetically lowest non-occupied energy band in equilibrium) minimum do not occur at the same wave vector, $\vec{k}$, within the reciprocal lattice (or momentum space) [12] and thus, in addition to absorbing a photon with

sufficiently high energy (i.e. sufficiently short wavelength), a momentum change, which is evoked by lattice vibrations (represented in the particle-based model by so-called phonons), is necessary to excite a charge carrier from VB to CB [12]. This process is called photogeneration of charge carriers. Figure 2.2 shows the band structure of c-Si in momentum space, including the described absorption mechanism. It is worth noting that direct transitions (i.e. without momentum change) are principally also possible but less likely and require substantially higher photon energies [11].

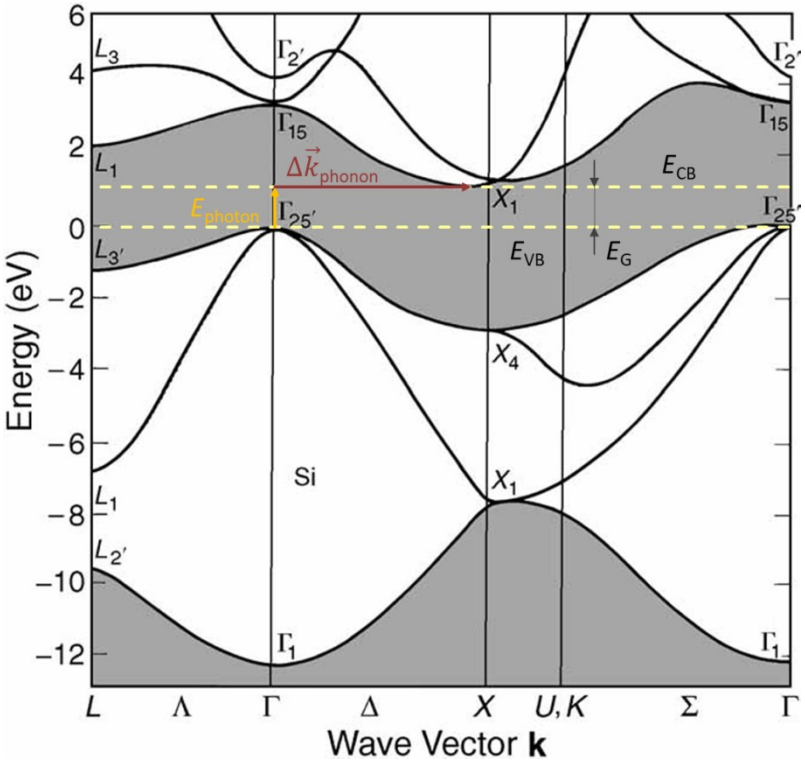


Figure 2.2: Momentum space band diagram of crystalline silicon. The following energies are depicted: band gap (E_G), valence band (E_{VB}), conduction band (E_{CB}), minimum necessary photon energy (E_{photon}, orange arrow), and phonon-induced momentum change ($\Delta\vec{k}_{phonon}$, red arrow) required for the excitation of charge carriers. Taken from [101] and adapted according to the discussion in the text.

As discussed already in section 2.1.1, c-Si can be doped with phosphorous or boron to form n-type and p-type c-Si respectively. Si atoms in the lattice are replaced by dopants, which act either as donors (elements with an electron more in their valence orbital than Si, like phosphorous) or acceptors (elements with one electron less in their valence orbital than Si, like boron). If the dopant atom's ionisation energy is close (less than 50 meV) to either band, they are fully ionised already at room temperature and contribute effectively to the charge transport within the semiconductor [102] by either collecting electrons from the VB (for

acceptors) and leaving behind a hole (which can be modelled as a positively charged particle), or inserting extra electrons into the CB (for donors) (cf. Figure 2.3a and b). Doping shifts the Fermi level, E_F, (i.e. the energy where the probability that a state is occupied by a charge carrier is as high as it being non-occupied) from midgap position in intrinsic Si towards either band edge [100]. The amount of foreign atoms is increased from 10^{10} atoms/cm³ in intrinsic material to 10^{15}–10^{16} atoms/cm³ for a doping concentration (N_D) relevant in practical solar cell applications [102].

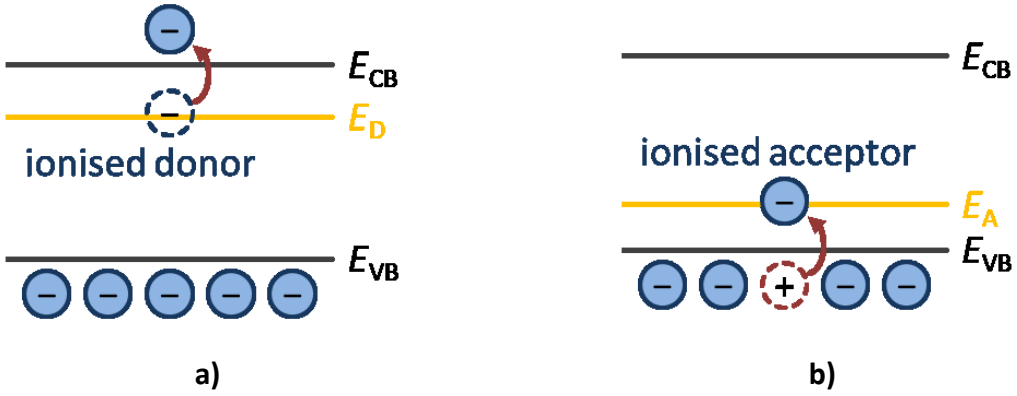


Figure 2.3: Schematic of the ionisation process of a) donors and b) acceptors in doped silicon. E_D and E_A denote the energy level of donors and acceptors respectively. Reworked from [100].

2.1.3 Recombination in Semiconductors

Recombination is the inverse process of charge carrier generation. The latter is the absorption of a photon and generation of an electron–hole pair as described in the previous section. The former, recombination, can occur according to different models that are introduced as follows and depicted in Figure 2.4a–d.

Shockley-Read-Hall recombination (SRH) [103] is the predominant recombination mechanism in c-Si. Here, charge carriers recombine via traps (i.e. defects that are not induced by doping but rather impurities and crystal defects) in the band gap. The electron's excess energy is converted into lattice vibrations (i.e. phonons).

Auger recombination [11] necessitates already excited charge carriers in the CB and thus plays a primary role at high illumination levels (also called high-injection regime) and high charge carrier concentrations (squared dependence of the latter). An excited electron transfers its energy to another electron within the CB and recombines with a hole in the VB.

The further excited electron in the CB gradually dissipates its energy as heat until it has reached its former energetic level at the CB edge.

Radiative recombination [11] plays only a minor role in c-Si since it is an indirect semiconductor and therefore an additional momentum change is necessary, which is provided by a phonon (three-particle process). An electron in the CB recombines with a hole in the VB under emission of a photon, hence 'radiative', that features a wavelength specific to the materials bandgap. In c-Si with its band gap of 1.12 eV, a near-infrared (IR) photon with a wavelength of roughly 1100 nm is emitted.

Surface recombination [11] is a special case of SRH recombination. Here, unsaturated (unbound) surface Si atoms, and surface impurities act as recombination centres. The key parameter of this mechanism is the surface recombination velocity (SRV), which describes how fast (or effective) the recombination occurs. The mechanism itself is the same as described above.

To every recombination mechanism, a specific minority charge carrier lifetime (τ_i, the average time until two charge carriers will recombine within a certain model) can be ascribed. From that, an effective minority charge carrier lifetime (τ_{eff}) can be calculated by using equation (2.1) [102] or, more fundamentally, equation (2.2) where Δn is the excess minority charge carrier concentration and τ_{eff} is given as the ratio of photogenerated excess charge carriers divided by the recombination rate. It is evident that the lowest respective lifetime of all contributing mechanisms governs the overall τ_{eff}. This is important when optimising devices. The first three terms on the right-hand side of equation (2.1) can be further summarised to $1/\tau_{bulk}$ (the bulk minority charge carrier lifetime) as they are intrinsic properties of the bulk. Techniques for measuring τ_{eff} are described in section 3.4.1.

$$\frac{1}{\tau_{\mathrm{eff}}} = \frac{1}{\tau_{\mathrm{SRH}}} + \frac{1}{\tau_{\mathrm{Auger}}} + \frac{1}{\tau_{\mathrm{radiative}}} + \frac{1}{\tau_{\mathrm{surface}}} \tag{2.1}$$

$$\tau_{\mathrm{eff}}(\Delta n) = -\frac{\Delta n}{\mathrm{d}\Delta n / \mathrm{d}t} \tag{2.2}$$

It is, lastly, worth mentioning that, although all recombination processes have been described from the point of view of an electron in the CB, the same mechanisms also apply to holes in the VB but with inverse energetic direction.

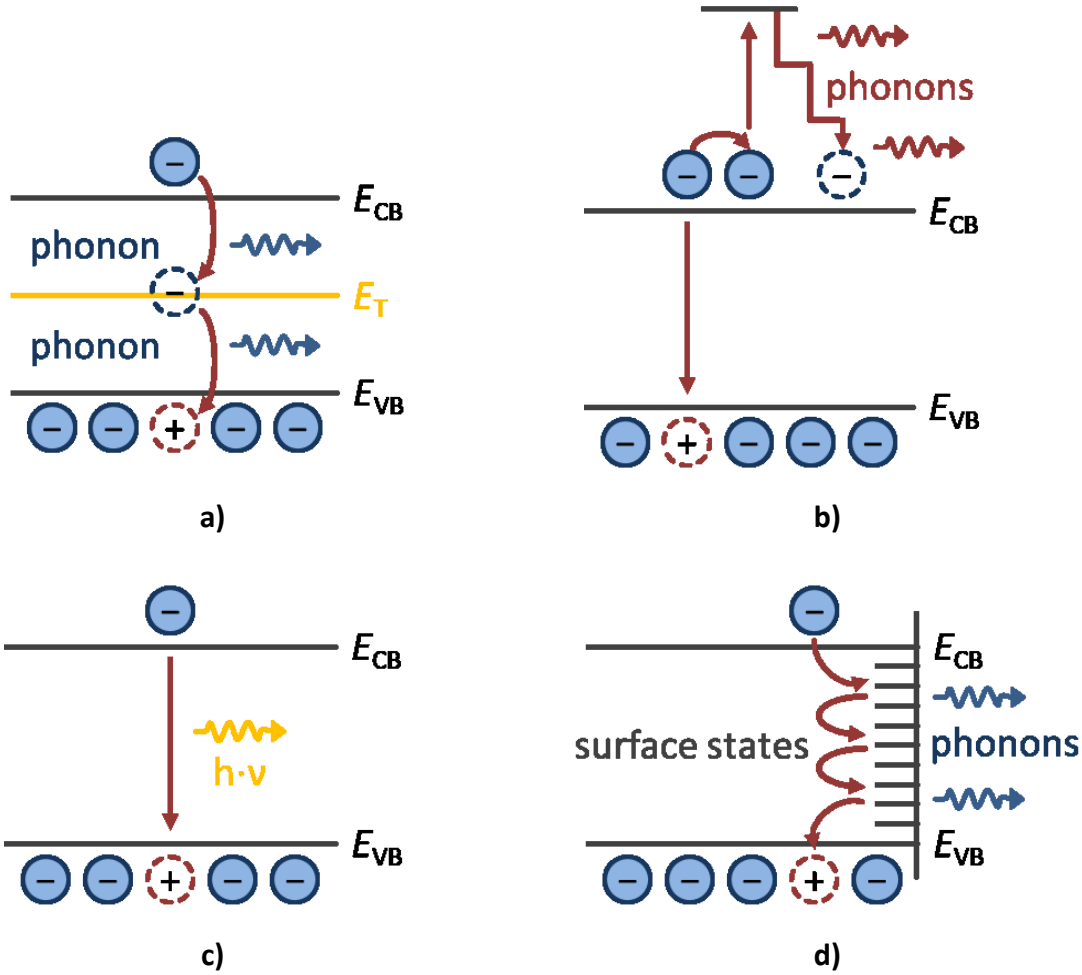


Figure 2.4: Recombination mechanisms in c-Si: a) SRH, b) Auger, c) radiative, and d) surface recombination. Reworked from [11,102].

2.1.4 Amorphous/Crystalline Silicon Interfaces

Although the atomic lattice of the bulk in c-Si is anisotropic, its surface features an increased density of defect states due to dangling bonds and surface contaminations, which leads to high SRVs. This can be suppressed by means of surface passivation whereof two mechanisms exist and which leads to high minority charge carrier lifetimes [104]. The influence of the first mechanism, the so-called field-effect passivation (FEP) where altering the electric charge density by means of introducing an electric field [105] is used to deplete the amount of one species of charge carrier within the passivation layer [14,106] is discussed in more detail in the next section. Here, the working mechanism of the second mechanism, chemical passivation, is explained and implications for the devices investigated in this thesis are discussed. While a variety of surface passivation materials for c-Si is known, the most common are silicon oxide (SiO_x) and a-Si:H whereof the latter leads to better results due to a lower dark saturation current density (j_0, cf. sections 2.2.1 and 2.2.2 for further details) [15]. SiO_x-passivated

contacts are not investigated over the course of this thesis and therfore only a-Si:H is discussed in the following. Passivating the surface of c-Si with a-Si:H is mainly achieved chemically, i.e. by saturation of dangling bonds at the c-Si surface by hydrogen atoms from the a-Si:H layer [107]. Since a-Si:H features a far wider band gap than c-Si, this inevitably leads to band discontinuities (so-called band offsets) and band bending (BB), which stems from the effective fixed charge at the interface [108] and (in the simplest model) the difference in the materials' work functions, Φ (or in other words the different energetic position of E_F with respect to the vacuum level before contact formation, cf. Figure 2.5a). It is further worth mentioning that the majority of BB in an ideal a-Si:H/c-Si interface occurs in c-Si due to a high density of rechargeable states in a-Si:H [85]. As already stated in section 2.1.1, the band gap of a-Si:H widens with increased C_H. This widening is, however, not equally distributed to both energy bands. While the conduction-band offset (ΔE_{CB}) remains largely independent of C_H at 150 ± 40 meV [109], the valence-band offset (ΔE_{VB}) increases from 200 meV to 450 meV with increased (i.e. 10–25%) C_H [85] and is thus the main contributor to the overall band gap widening. On the other hand, ΔE_{VB} has been found to be independent of doping [110]. Figure 2.5b shows the band line-up of an ideal a-Si:H/c-Si interface as discussed above.

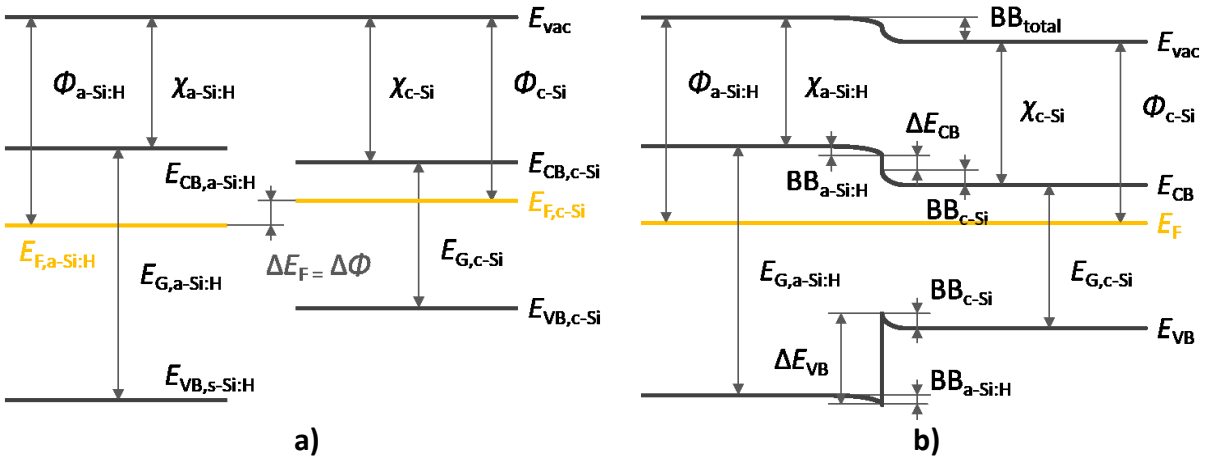


Figure 2.5: Band line-ups of an a-Si:H/c-Si interface (not to scale) a) before and b) after contact formation of wafer (c-Si) and passivation layer (a-Si:H(i)). Depicted are the band gaps ($E_{G,a\text{-}Si:H}$ and $E_{G,c\text{-}Si}$), the band edges (E_{CB} and E_{VB}), the Fermi levels (E_F), the vacuum level (E_{vac}), the electron affinities ($\chi_{a\text{-}Si:H}$ and $\chi_{c\text{-}Si}$; i.e. the energies necessary to ionise an electron within the CB), the work functions ($\Phi_{a\text{-}Si:H}$ and $\Phi_{c\text{-}Si}$), the band bending (BB) stemming from the different materials' Φ, and the band offsets (ΔE_{CV} and ΔE_{CV}). Reworked from [85].

There are, however, some important considerations regarding real interfaces because a-Si:H and the interface itself have to fulfil certain criteria to enable proper surface passivation on c-Si. For one, the interface has to be abrupt because epitaxially grown a-Si:H layers are known to be detrimental for surface passivation [90,91,111]. This is especially problematic for textured surfaces where pyramid valleys are prone to epitaxial growth [112,113] and when the deposition temperature is too high [89–91,114]. It is further helpful to ensure a hydrogen-poor and thus less disordered a-Si:H layer directly at the interface [114]. On the other hand, a-Si:H layers that are deposited close to the microcrystalline regime have been shown to yield the best passivation results [115]. For that matter, hydrogen plasma treatment (HPT) after low-C_H deposition of a-Si:H can drastically improve the passivation with respect to minority charge carrier lifetimes [82,116,117] by introducing high amounts of hydrogen to the upper shallow region (facing the contact layers) while leaving the hydrogen-poor interface layer unharmed. Lastly, non-epitaxially grown layers benefit largely from post-deposition annealing due to redistribution of hydrogen within the lattice [91,114].

2.1.5 Doped Layers in Amorphous/Crystalline Silicon Interfaces

Here, the influence of doped layers on the passivation quality of an a-Si:H/c-Si interface is discussed. Firstly, the introduction of highly doped layers leads to additional BB at the interface and thereby to effective FEP [108]. Since recombination always involves (at least) two charge carriers, the depletion of one charge carrier species yields better passivation with respect to higher minority charge carrier lifetimes simply based on the fact that the excited charge carriers have no partner to recombine with [14,106]. Secondly, the negative impacts of introducing doped layers, especially p-type a-Si:H atop intrinsic a-Si:H, are considered and measures to circumvent these issues are discussed. For convenience, the following denotations are used in the following: a-Si:H(i) for intrinsic a-Si:H, a-Si:H(p) for p-type a-Si:H, nc-Si:H(n) for n-type nc-Si:H, c-Si(n) for n-type c-Si, and c-Si(p) for p-type c-Si.

Most dielectric layers already feature a small amount of electric charge and thus FEP is already introduced by a-Si:H(i) [105]. This passivation mechanism is, however, weak as compared to the chemical passivation provided by a-Si:H(i). The opposite is true for doped layers where a strong FEP is provided but chemical passivation is ineffective [118]. So, a carefully tuned combination of both chemical passivation and FEP yields decent surface

passivation. However, highly doped (and therefore highly conductive) layers, which are needed for lowly resistive contacts with external electrodes [48,54,119], will inevitably lead to a degradation in passivation quality of a-Si:H(i) [118,120]. It must further be mentioned that the passivation quality of a-Si:H(p) and a-Si:H(n) is not equal with the former yielding poorer effective minority charge carrier lifetimes (especially for $\Delta n \leq 10^{15}$ cm^{-3}) [121,122]. Additionally, the combination of deposition temperature and a-Si:H(p)'s energetic position of E_F are detrimental for the passivation layer, which is explained in detail in [123] and will be briefly outlined in the following. Depositing a-Si:H(p) onto a-Si:H(i) will shift E_F within the latter towards the VB edge. The temperature at which hydrogen effusion sets in is highly dependent on the relative position of these two energy levels: the closer E_F gets to the VB edge, the lower the necessary temperature is. Rupture of Si–H bonds leads then to the formation of gaseous (effusing) hydrogen and open Si bonds at the interface, which permanently deteriorates the passivation. The onset of this hydrogen effusion has been observed for temperatures as low as 155 °C, implicating that it already occurs during the deposition of a-Si:H(p).

As already stated above, highly conductive layers are necessary to form a good ohmic contact to external electrodes. For this matter, owing to its better conductivity as compared to its amorphous counterpart, the use of nc-Si:H is highly beneficial both in terms of optical and electrical properties (especially the latter regarding solely rear-contacted devices as they are investigated in this thesis) [95,99]. It is, however, challenging to develop a deposition process involving p-type nc-Si:H or µc-Si:H (distinguishable by their grain size) atop a-Si:H(i) that yields good surface passivation [123,124]. Therefore, in this thesis nc-Si:H is used only for the n-contact. Although the growth of nc-Si:H(n) atop a-Si:H(i) at low temperatures is also challenging, it is achievable by carefully tuning deposition process parameters, especially temperature, pressure, and silane dilution [96–98] (cf. section 3.1.1 for further details).

2.1.6 TCOs and Metal Contacts for Amorphous/Crystalline Silicon Interfaces

As already mentioned before, highly doped a-Si:H, albeit detrimental for a good passivation, is mandatory for forming a lowly resistive and ohmic contact with external electrodes [48,54,119]. The latter are, in most cases discussed in this thesis, composed of a combination of transparent conductive oxide (TCO) and a metal. In some cases, a direct

metallisation omitting any TCO is applied to a-Si:H(p). This can be beneficial since inserting any TCO at the front or rear side leads to free-carrier absorption of long-wavelength photons in the red and near-IR part of the spectrum [16]. On the other hand, TCOs suppress parasitic plasmonic absorption in an adjacent metal layer [125] and thus the contribution of both loss mechanisms needs to be balanced carefully.

TCOs are so-called degenerate semiconductors, i.e. their doping concentration is at such high level that their Fermi level is shifted into either conduction or valence band (depending on the TCO's doping type) and usually feature wide band gaps [100]. Although there are both n and p-type TCOs, contacting of a-Si:H(p) is usually also realised with an n-type TCO [126] owing to the low hole mobilities of most p-type TCOs [127]. Interconnecting a highly doped n and p-type layer (here: TCO and a-Si:H(p)) leads to a band alignment where holes can only be transported to the CB by means of recombination (cf. next section for further details) because they face a substantial energetic barrier within the VB. This renders the realisation of a well-functioning p-contact challenging and makes it once again the more problematic contact. In the following, the working principle of an a-Si:H(p)/TCO contact is discussed and measures for designing it in a way to ensure proper functionality are presented.

A critical parameter of any contact material is its work function (WF) [56], defined as the distance between E_F and vacuum level (cf. Figure 2.5), or the energy necessary to ionise an electron from an uncharged state within a semiconductor (or metal) [11,102]. High-WF materials have been reported to be beneficial for contacting p-type a-Si:H and, conversely, low-WF materials for n-type a-Si:H [49,55,57]. It is to be mentioned, however, that the electrical contact properties of c-Si-based devices are not solely determined by the used materials' work functions because here, interface states and intrinsic defects can pin the E_F to nearly midgap position regardless of the contact material's WF [128,129]. Furthermore, a discrepancy in different materials' WFs, which is also known as work-function mismatch, can deteriorate the electrical properties of a contact stack [54,130]. This WF mismatch might impair the passivation due to additional BB at the a-Si:H(i)/c-Si interface, and in order to screen the latter from this effect, a certain doped a-Si:H layer thickness is necessary [49,126].

In the following, the contact materials utilised within this thesis are briefly introduced. Indium tin oxide (ITO), Indium zinc oxide (IZO), and aluminium-doped zinc oxide (AZO) are used as TCOs whereof ITO is by far the most common within c-Si-based devices [6]. Its WF is

reported to be in the range of 4.4–4.5 eV [131]. AZO, in comparison, features a lower WF of only 3.7–4.4 eV [132], but is, by contrast, more transparent in the long-wavelength part of the spectrum [50,133]. Lastly, IZO features by far the highest WF of 5.0 eV [134], which is therefore used only as a contact for p-type layers within this thesis. In combination with either TCO, silver (Ag) is used as the metal of choice owing to its outstanding electrical properties. In addition, a direct metallisation with aluminium (Al), which is likewise highly conductive, is also investigated. Being a p-type dopant, Al is known to form a lowly resistive ohmic contact with a-Si:H(p) [135,136], which is otherwise challenging with classic n-type materials, such as ITO. Both metals, Ag and Al, feature a similar WF in the range of 4.3 eV [102,137].

2.1.7 Charge Carrier Transport Across Amorphous/Crystalline Silicon Interfaces

A well-designed interface between a-Si:H(p) and n-type TCO is key to a proper working a-Si:H/c-Si device. Regarding the transport of charge carriers (here: holes) across said interface, both a-Si:H(p) and TCO need to feature a high doping concentration at least at their junction [138,139]. If the free-carrier concentration is sufficient, holes can recombine with electrons from the CB. This recombination contact is sometimes also referred to as a tunnel contact; for the sake of consistency, the former expression will be used over the course of this thesis. Lowly doped a-Si:H(p) layers, in contrast, lead to an impassable energetic barrier for holes and thus to an inefficient hole transport [48,140]. In Figure 2.6, schematics for both the low (a) and the high doping (b) case of an a-Si:H(p)/TCO recombination contact are depicted. Highly doped layers increase furthermore the amount of BB and therefore decreases the width of band offsets [141], which is beneficial for intra-band transport since it allows for direct tunnelling through band offsets, hopping through defect states within a-Si:H or for thermionic emission [48,94,142].

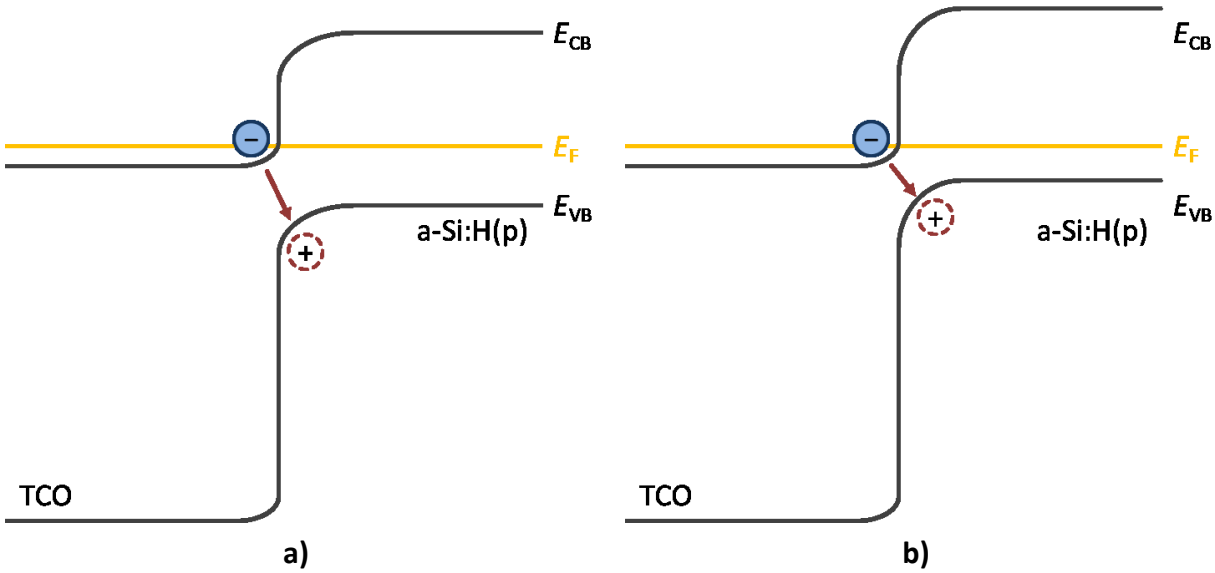


Figure 2.6: Schematics (not to scale) of the operating principle of an a-Si:H(p)/n-type TCO recombination contact for a) a low and b) a high doping concentration in a-Si:H(p). Reworked from [48,49].

2.2 Working Principle of Solar Cells

The main focus of this subsection is to explain the operating principles of solar cells (especially those discussed in later parts of this thesis), introduce their characteristic parameters, and present basic models to describe their electrical behaviour.

2.2.1 P/N-Junction Based Solar Cells

A solar cell is essentially a photoactive diode with metal contacts. Its basic structure consists of an n-type and a p-type semiconductor (here: both Si) brought in contact and thus forming a space charge region in-between with a typical width of 0.35 µm [102]. Fabricating such a device is usually done by counterdoping one side of a p-type wafer using a phosphorous source at high temperatures to form a thin n-type layer [11]. Charge carriers generated within this device, by means of absorbing photons with sufficient energy, are separated because of the different electrochemical potential in differently doped regions, which is connected to different conductivities of either charge carrier species within these differently doped layers [143]. If each contact is connected with a metal electrode, the generated and separated charge carriers can be utilised in an external circuit. The non-illuminated current density–voltage (*j*–*V*) characteristics of such a device can be described by equation (2.3) (the so-called Shockley diode equation) [11].

$$j = j_0 \cdot \left[\exp\left(\frac{V}{V_T}\right) - 1\right] \tag{2.3}$$

with

$$V_T = \frac{k \cdot T}{q} \tag{2.4}$$

Here, j_0 denotes the dark saturation current density (a very small, ideally several fA, leakage current that flows in the dark at an applied negative bias voltages; further details are given in the next section), V the voltage, and V_T the thermal voltage, which is further dependent of the Boltzmann constant, k, the absolute temperature, T, and the elementary charge, q, as defined by equation (2.4). V_T is a measure of intrinsic voltage of a semiconductor [100] and amounts to approximately 26 mV at room temperature. If such a p/n-junction based solar cell is illuminated, another term, $-j_{ph}$, the photogenerated current density (i.e. the generated charge carriers that contribute to the external current) is added to equation (2.3), shifting the curve down by that amount (cf. Figure 2.7). This shifting is also called the superposition principle and holds true for solar cells where the photovoltage is governed by quasi Fermi level splitting (cf. next section for more details) [140,144].

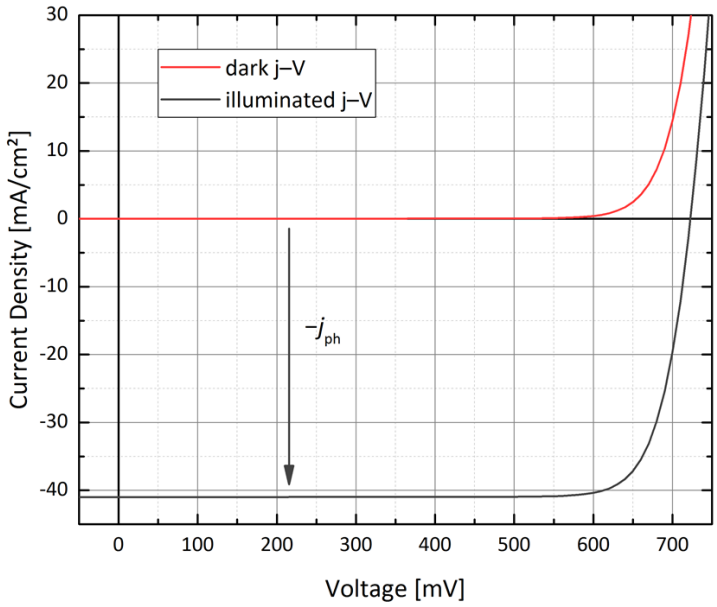


Figure 2.7: Dark and illuminated current–voltage characteristics. The term $-j_{ph}$ is the photogenerated current density.

The maximum useable voltage (cf. next section) of a simple diffused p/n-junction based devices as described above is limited by recombination either within the bulk (if the diffusion

length, *L*, i.e. the average distance a charge carrier can travel before it recombines, is much less than the wafer thickness, *W*) or at wafer surface and defect-rich semiconductor/metal interface (if *L* is much greater than *W*) [145].

2.2.2 Important Solar Cell Parameters

Figure 2.8 shows the typical illuminated *j*–*V* characteristics of a solar cell. The voltage where the graph crosses the abscissa is called the open-circuit voltage (V_{oc}). At this point, no current is extracted and the electric power output (*P*) consequently is zero. The V_{oc} strongly depends on j_0 (the lower the latter, the higher the former); both are connected to interface recombination phenomena (for sufficiently long diffusion lengths) [146] and thus reliable indicators for good passivation.

Ideally, the voltage of a solar cell under illumination is equal to the splitting of the Fermi level, E_F, (cf. dection 2.1.2) into two separate quasi Fermi levels: E_{Fe} and E_{Fh} for electrons in the conduction band and holes in the valence band respectively [147]. Upon illumination, the excess charge carrier densities for both electrons and holes exceed by far their equilibrium densities (i.e. in the dark) [16,102]. Because of this increased amount of electrons in the conduction band, E_{Fe} is shifted closer towards the conduction band edge; and, conversely, because of the increased amount of holes in the valence band, E_{Fh} is shifted closer towards the valence band edge [102,143]. The position of E_{Fe} with respect to the Fermi level of an intrinsic semiconductor in the dark, E_i, is given by equation (2.5) [102] where n_e is the density of electrons under illumination, $n_{i,eff}$ the effective intrinsic charge carrier density, *k* the Boltzmann constant, and *T* the absolute temperature. The same correlation holds true for holes in the valence band where n_e is replaced by the density of holes, n_h, under illuminaton and E_{Fe} by E_{Fh}. Large quasi Fermi level splitting is the precondition for achieving high voltages in a solar cell [143].

$$n_e = n_{i,eff} \cdot \exp\left(\frac{E_{Fe} - E_i}{k \cdot T}\right) \Leftrightarrow E_{Fn} - E_i = k \cdot T \cdot \ln\left(\frac{n}{n_{i,eff}}\right) \tag{2.5}$$

The highest current in a solar cell is achieved by shunting its contacts. It is called the short-circuit current density (j_{sc}) and is represented in Figure 2.8 by the intersection of *j*–*V* graph and ordinate. Here, no voltage is applied since both electrodes share the same electric potential and thus *P* is, again, zero.

The point where the power output becomes maximal is called the maximum-power point (MPP) and is the desired operating point of a solar cell. The corresponding voltage and current are denoted V_{MPP} and j_{MPP} respectively. The so far defined parameters can be further used to calculate the fill factor (FF) from equation (2.6), which is a measure of parasitic resistive losses (cf. next section for further details) within the device.

$$FF = \frac{V_{\mathrm{MPP}} \cdot j_{\mathrm{MPP}}}{V_{\mathrm{oc}} \cdot j_{\mathrm{sc}}} \tag{2.6}$$

The power conversion efficiency (PCE or η) indicates how much of the incident (solar) irradiation is transformed into electrical energy. The PCE can be calculated by using equation (2.7); the therein introduced parameter E is the irradiation intensity, given in W/cm².

$$PCE = \frac{V_{\mathrm{MPP}} \cdot j_{\mathrm{MPP}}}{E} = \frac{FF \cdot V_{\mathrm{oc}} \cdot j_{\mathrm{sc}}}{E} \tag{2.7}$$

The theoretical PCE limit was first computed to slightly above 30% for a single Si converter [23] and has later been revised to 29.4%, taking relevant wafer thicknesses, Auger recombination at high illumination intesities, and a realistic irradiation spectrum into account [17].

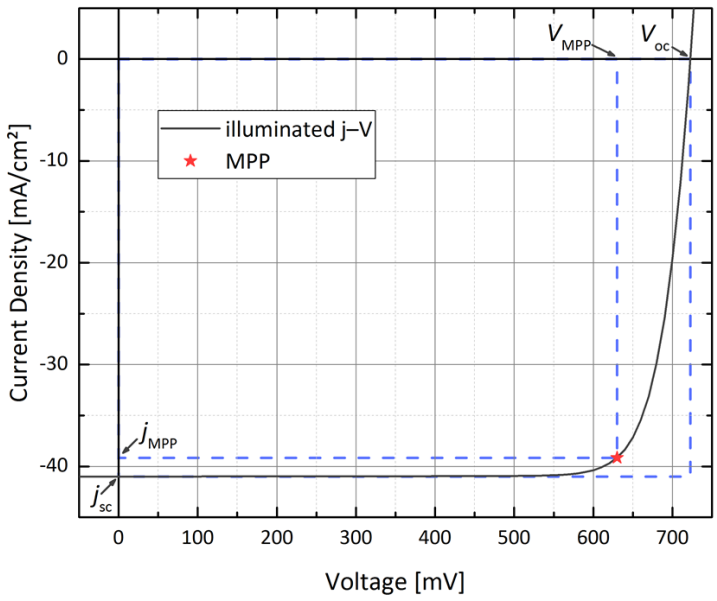


Figure 2.8: Typical current–voltage characteristics of a solar cell including all important parameters: open-circuit voltage (V_{oc}), short-circuit current density (j_{sc}), maximum-power point (MPP), voltage at MPP (V_{MPP}), and current density at MPP (j_{MPP}).

2.2.3 Equivalent Circuit Model

The basic electrical behaviour of a solar cell can be described using a quite simple model involving a current source interconnected in parallel with a diode; a series resistance (R_s) and a shunt resistance (R_{shunt}) are added to the model to account for parasitic resistive losses that occur in a real solar cell [102]. Figure 2.9a depicts this basic equivalent circuit model. The R_s includes contact resistances throughout the device as well as ohmic resistances within semiconductor and contact materials. For a well-functioning device its value should be as small as possible since a high R_s negatively impacts the FF by decreasing the slope of the *j*–*V* graph at V_{oc} (cf. Figure 2.9c) and very high values will also reduce the j_{sc}. On the contrary, R_{shunt} represents resistive losses due to alternative current paths, such as leakage currents along the edges of a device, crystallographic errors, or a real shunt (i.e. the connection of both electrodes). Ideally, it amounts to several kiloohms because low values reduce the FF by increasing the slope of the *j*–*V* graph at j_{sc} (cf. Figure 2.9d). Additionally, V_{oc} is also reduced for very low values of R_{shunt}.

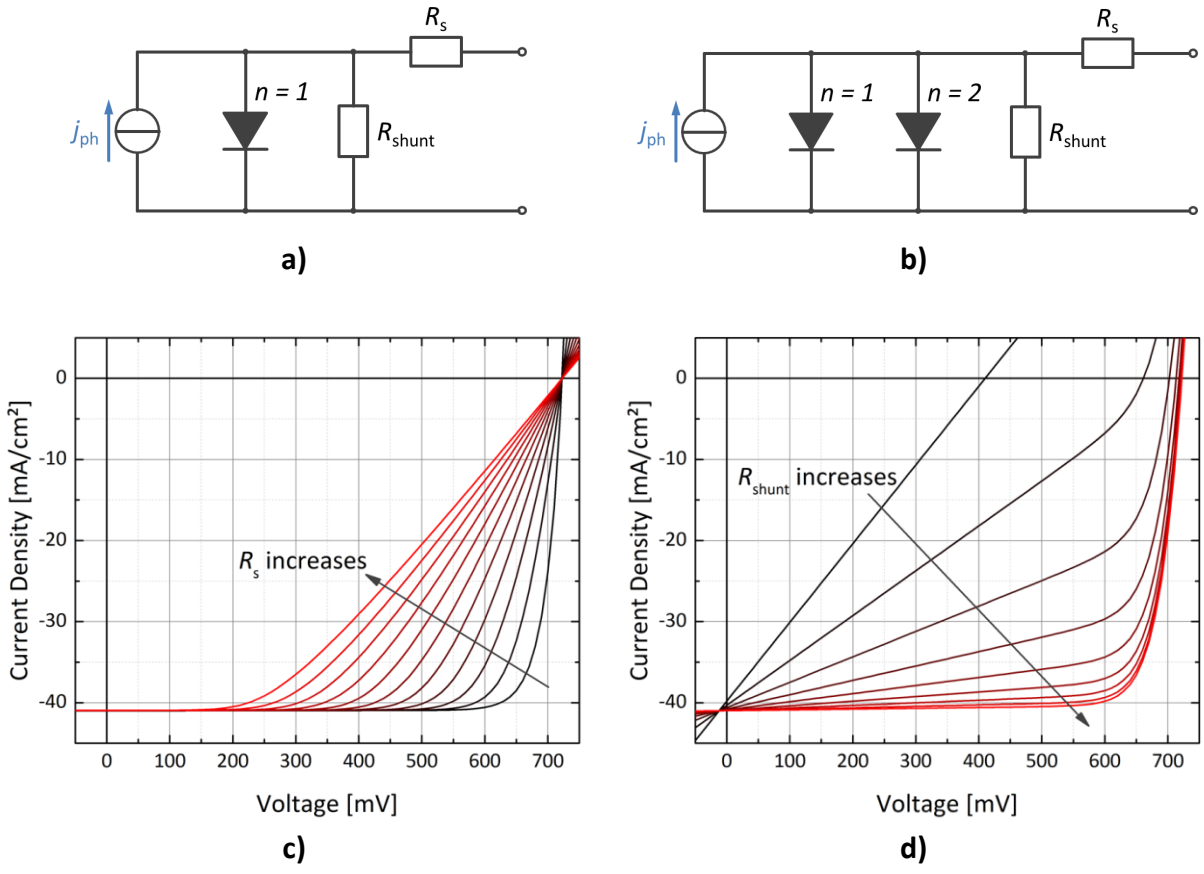


Figure 2.9: Basic electrical equivalent circuit models of a solar cell comprising a) one or b) two diodes. Impact of c) series resistance (R_s) and d) shunt resistance (R_{shunt}) on the current–voltage characteristics of a solar cell.

When a resistive load is connected to the device's terminals, an external voltage can be measured across it and the correlation between *j* and *V* can be described using equation (2.8), which is essentially equation (2.3) but extended by the impact of the parasitic resistivities described above. It is worth mentioning that this equation is no longer explicit and can only be solved numerically.

$$j = j_0 \cdot \left\{ \exp\left[\frac{q(V - j \cdot R_\mathrm{s})}{n \cdot k \cdot T} \right] - 1 \right\} + \frac{V - j \cdot R_\mathrm{s}}{R_\mathrm{shunt}} - j_\mathrm{ph} \qquad (2.8)$$

Here, *n* denotes the so-called ideality factor of a diode. For an ideal solar cell, *n* equals 1, i.e. the device behaves like an ideal diode and recombination of charge carriers occurs by means of SRH or radiative recombination only. Other values for *n* are associated with different dominant recombination mechanisms: SRH under high injection, for instance, results in an *n* of 2, Auger recombination leads to an *n* of 2/3 [100,148]. For a real-world device, however, *n* can deviate from 1, does not necessarily have to be an integer, and can theoretically even be much larger than 2 [35,140,149]. To account for this circumstance, a more elaborate but also more accurate model involving multiple diodes with different values for *n* can be employed. The most common thereof is the two-diode model involving ideality factors of 1 and 2 [150,151]. Its dark *j*–*V* characteristics are described by the implicit equation (2.9), with the indices 1 and 2 denoting the respective diode, and its equivalent circuit is depicted in Figure 2.9b.

$$\mathrm{j} = \mathrm{j}_{0,1} \cdot \left\{ \exp\left[\frac{\mathrm{q(V - j \cdot R_s)}}{1 \cdot \mathrm{k} \cdot \mathrm{T}} \right] - 1 \right\} + \mathrm{j}_{0,2} \cdot \left\{ \exp\left[\frac{\mathrm{q(V - j \cdot R_s)}}{2 \cdot \mathrm{k} \cdot \mathrm{T}} \right] - 1 \right\} + \frac{\mathrm{V - j \cdot R_s}}{\mathrm{R_{shunt}}} \qquad (2.9)$$

2.2.4 Heterojunction Solar Cells

Diffused p/n-junction based devices (so-called homojunction solar cells) as described in section 2.2.1 can be figured as comprising a continuous crystal lattice where only the distribution and concentration of doping atoms change with distance [102]. As opposed to that, heterojunction solar cells are based on the a-Si:H/c-Si approach as introduced earlier (or more generally on connecting different semiconductors under the formation of sharp interfaces). They feature thus real ruptures in morphology when considering a crystal lattice point of view. The underlying physics of the involved interfaces have been discussed in sections 2.1.4–2.1.7. The following passage will thus focus on a more comprehensive

device-based perspective. Figure 2.10 depicts the schematic layer stack and band diagram of a typical SHJ solar cell.

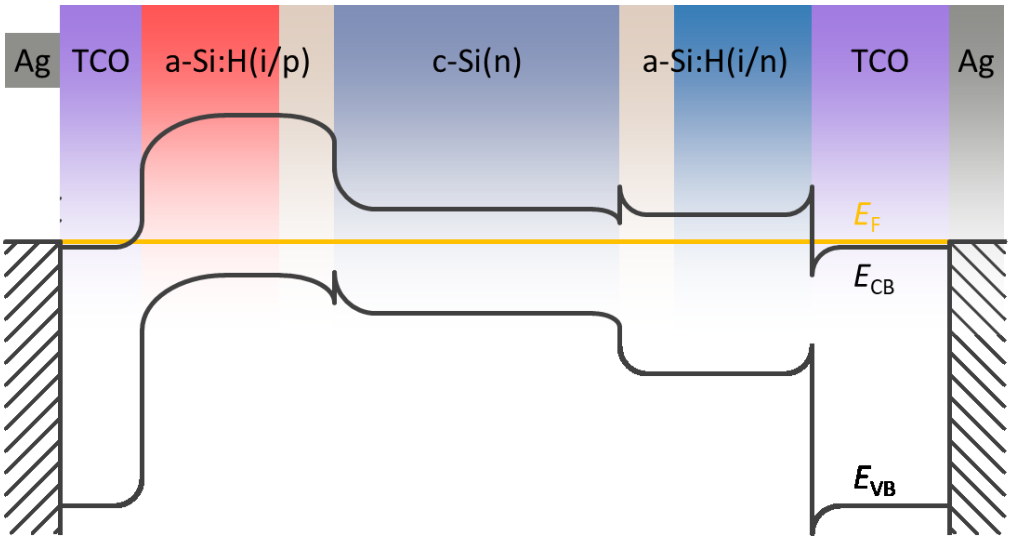


Figure 2.10: Equilibrium band diagram and typical layer stack of a standard silicon heterojunction solar cell (not to scale).

As opposed to homojunction solar cells where the junction is formed under very high temperatures, the silicon heterojunction (SHJ) concept, introduced in 1992 by TANAKA *et al*. [18], is based on low-temperature processes (limited to about 200 °C). Here, a thick usually n-doped monocrystalline c-Si absorber is bifacially passivated by thin a-Si:H(i) layers [15] by means of chemical passivation [107]. The saturation of dangling bonds at the c-Si surface by hydrogen atoms stemming from a-Si:H(i) suppresses surface recombination (leading to low j_0 and SRV) and yields therefore high V_{oc}s as the potential of the lowly defective c-Si bulk material can now be exploited. While the V_{oc} of a solar cell with non-passivated surfaces is limited to about 640–650 mV [16], its theoretically value for SHJ devices amounts to 761 mV [17], and V_{oc}s as high as 750 mV have already been presented experimentally [21].

The passivation layer thickness plays a major role for the final performance of these devices. Too thick layers induce an energetic barrier for charge carriers and can hamper the current extraction, leading thus to increased resistive losses within the device and low FFs [52,144,152]. A too thin a-Si:H(i) layer, on the contrary, leads to insufficient passivation [19,51,53]. An optimal thickness (regarding overall solar cell performance) has been found to be about 4 nm [51]. However, a certain thickness (considering device-relevant C_Hs) is necessary to even form a spatially homogenous a-Si:H(i) layer that uniformly covers the entire surface [80]. This

circumstance renders proper surface passivation of c-Si without ultimately deteriorating the performance of finished devices challenging. Adding doped a-Si:H layers leads to additional FEP and charge carrier selectivity (cf. sections 2.1.5 and 2.2.1 respectively). It has been suggested that carefully tuning the intrinsic and doped a-Si:H in such a way that the former's bandgap is equal to or narrower (i.e. less C_H) than the latter's makes the final device's FF less dependent of the passivation layer thickness [52].

SHJ solar cells can be realised in two ways: either in so-called front-emitter (i.e. the minority charge carrier contact at the illuminated side; a-Si:H(p) for an n-type wafer) or in so-called rear-emitter configuration (i.e. the majority charge carrier contact at the illuminated side; a-Si:H(n) for an n-type wafer; sometimes referred to as the back-surface field, BSF), both yielding similar overall PCEs [153,154]. The wafer's doping type, however, has a huge impact on the device performance because minority charge carrier lifetimes of n-type wafers are generally higher than those of their p-type counterparts [155], especially in the low-injection regime (i.e. low illumination intensities), which leads to slightly lower FFs [153,154] for solar cells processed on c-Si(p). This is also the reason why, as stated above, in SHJ technology mainly n-type wafers are used. An extraordinary PCE of 25.1% has been achieved experimentally utilising an n-type wafer with minority charge carrier contact at its illuminated side [20].

External electrodes of these cells usually consist of a TCO (primarily ITO) at both contacts covered by either a full-area Ag metallisation at the rear and a metal grid (usually also comprising of Ag) at the front side, or metal grids on both sides for a bifacial application (illumination from both sides, utilising incident and diffused irradiation) [16]. At the interface of doped a-Si:H and TCO high conductivities and thus doping concentrations are required to form a good contact (especially for holes) whereas this is detrimental regarding the passivation at the doped/intrinsic a-Si:H interface due to increased band bending at the c-Si surface (cf. sections 2.1.5–2.1.7). A possible solution for reconciling these contradictory requirements is the introduction of a graded emitter (i.e. a low a-Si:H(p) doping concentration towards a-Si:H(i) and a high doping concentration towards the TCO interface) [156]. Since the rear-side TCO fulfils electrical (enabling a lowly resistive ohmic contact) and optical requirements (suppressing plasmonic absorption within the rear-side metallisation), it can be tuned relatively freely. The front-side TCO, in turn, is restrained to a

certain thickness since it also serves as an anti-reflective coating (ARC). To further minimise parasitic absorption, the front-side TCO has to be very transparent but at the same time very conductive since it serves as the lateral transport layer for charge carriers. However, both optimum transparency and conductivity are seldom achieved at the same time.

2.2.5 Interdigitated Back-Contact Solar Cells

The general schematic of an IBC SHJ solar cell is depicted in Figure 2.11.

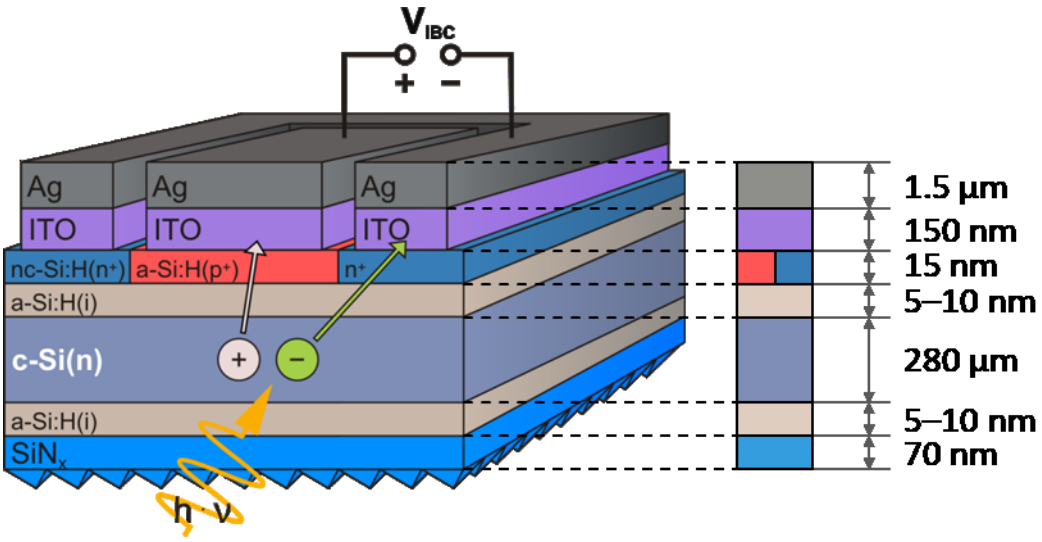


Figure 2.11: Schematic of an IBC SHJ solar cell (not to scale) with its rear side facing up. Electrons and holes photogenerated within the c-Si absorber are collected by respective electrodes at the rear side.

The interdigitated back-contact (IBC) [22] is another promising high-efficiency approach. Here, both electrodes are positioned at the rear side of the device, arranged in an interdigitated pattern (i.e. alternating stripes of n and p-type regions). Therefore, a front grid can be omitted and thus no shading losses occur. Additionally, the front side can now be optimised solely in terms of optical properties because unlike in standard SHJ solar cell, no lateral charge carrier transport has to be taken into account. Because of that, IBC solar cells yield very high j_{sc} values that are second to none. The combination of IBC and SHJ technology, introduced in 2007 by Lu *et al*. [24], also combines their respective advantages (i.e. both high j_{sc}s and V_{oc}s), and consequently (provided that resistive losses are sufficiently low) also high PCEs. Indeed, the highest hitherto reported PCE of 26.7% (improved in quick succession from 26.3% [28] and 26.6% [29]) for a Si-wafer based solar cell has been achieved using the IBC SHJ concept [30], making it thus the currently most successful Si-based single-junction technology.

However, restricting the contact area to only one side of the device entails some challenges on achieving high FFs [35], in addition to the already lower FFs owing to the a-Si:H(p) recombination contact of the SHJ concept. IBC SHJ solar cells thus often suffer from lower FFs mainly due to higher contact resistivities as compared to their bifacially contacted counterparts [35]. This is further exacerbated by the IBC concept achieving higher j_{sc}s since electric power losses are proportional to the square of the current. It has been further shown that both back-contacted and standard SHJ solar cells suffer essentially from similar loss mechanisms [35,36]. Despite all that, Kaneka's back-contacted record device achieved a staggering FF of 84.9% [30], demonstrating that this inherent drawback of IBC SHJ solar cells can be overcome. Although the exact contact scheme of this device is currently unknown, increasing the FF can generally be achieved by adjusting the passivation layer thickness and doping concentrations of a-Si:H layers (as discussed in the previous section), or by adapting the WF of the contact by choosing adequate materials and, again, doping concentrations (cf. section 2.1.6).

2.3 Tandem Solar Cells

In this subsection, multi-junction or tandem solar cells, i.e. devices utilising at least two different absorber materials within a single device, are introduced. Different methods of interconnecting subcells of a tandem solar cell are discussed and possibilities of using an IBC SHJ solar cell within a multi-junction device are examined.

2.3.1 Principle of Tandem Solar Cells

A solar cell with a single absorber can only utilise photon energies greater than or equal to its band gap [62,157]. Photons with longer wavelengths are transmitted (transmission losses); those with shorter wavelengths are absorbed but their energy is not fully converted into electrical energy: the shorter the wavelength, the more energy is transformed into heat (thermalisation losses). Part of the absorbed photons' energy is further lost due to recombination [63]. In Figure 2.12, a qualitative representation of spectral photon energy utilisation of the AM1.5g spectrum (the standard solar spectrum used for characterisation of solar cells; cf. section 3.4.3 for further details) for both a single (a) and dual absorber device (b) is depicted. Semiconductors with a narrower band gap than c-Si, such as germanium (Ge,

0.66 eV [100]), can absorb longer-wavelength photons (with less energy) and feature thus reduced transmission losses but suffer from increased thermalisation losses. On the contrary, in wide band gap semiconductors, such as gallium arsenide (GaAs, 1.42 eV [100]) or pervoskites (cf. below), thermalisation losses are decreased but here, more of the long-wavelength photons are transmitted. By combining two (or more) semiconductors, with the widest band gap material being at the top and the following absorbers featuring gradually narrower band gaps, these overall fundamental losses can be minimised and the combined PCE consequently maximised up to a theoretical limit of 86.8% if an infinite number of subcells is employed [62].

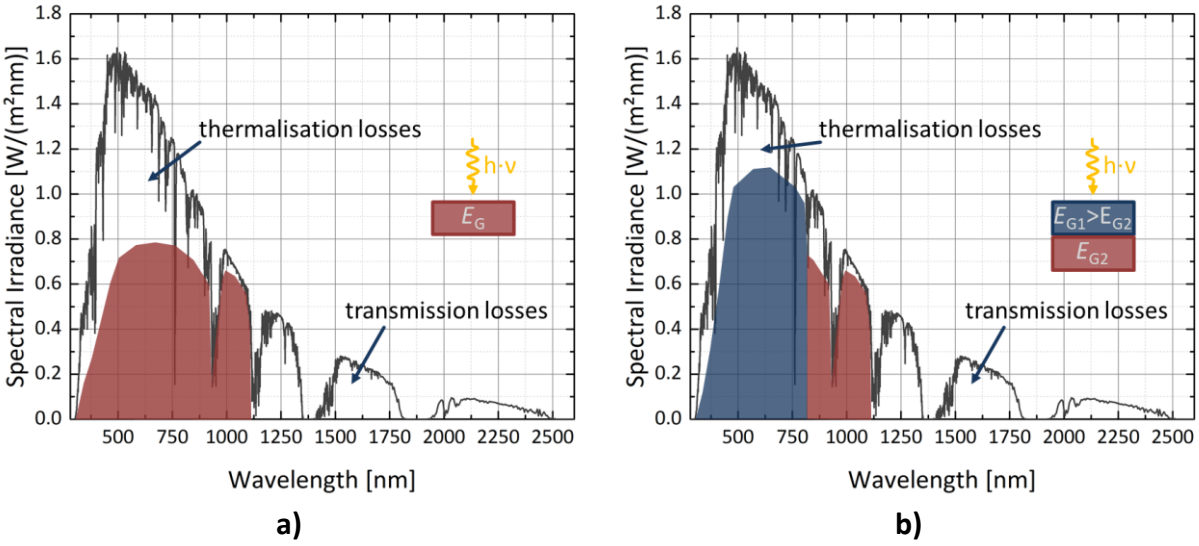


Figure 2.12: Utilisation of the AM1.5g solar spectrum by a) a single absorber with a band gap (E_G) of 1.12 eV and b) a tandem device with E_{G1} = 1.7 eV and E_{G2} = 1.12 eV. Reworked from [63].

For a more practical approach of using two semiconductors (henceforth referred to as tandem solar cell or tandem device), the basic principle as well as the corresponding spectral yield are depicted in Figure 2.12b. The maximum PCE (i.e. detailed balance limit) of such a device amounts to 42.2%, provided that the subcells feature band gaps of 1.9 eV and 1.0 eV respectively [62]. For that matter, c-Si exhibits an almost optimal band gap for a bottom cell in a two-semiconductor device. Perovskite solar cells (a compound semiconductor material comprising essentially halides and group IV elements, especially lead and tin [158,159]) with their tuneable band gaps in the range of 1.5–1.7 eV are nearly ideal top cell counterparts: according to DE VOS *et al.*, the combination of a 1.12 eV and a 1.7 eV subcell still yields a theoretical overall PCE of slightly above 40% [62]. A more comprehensive overview over the

PCE potential of perovskite/silicon tandem solar cells can be found in [160,161]. This topic will be further discussed in sections 5.4.2 and 6.3.

2.3.2 Subcell Interconnection in Tandem Solar Cells

Having a two-absorber device entails increased complexity in terms of contact formation since charge carriers generated in each subcell must be separated and collected at external contacts, ideally without mutual negative interference. The energy landscape (i.e. band diagram) of a tandem must be designed in such a way that no energetic barriers occur (except where needed for charge carrier separation; cf. below), which is more difficult as compared to single-junction solar cells because usually more layers are involved. For interconnecting subcells in a tandem device, two concepts are commonly proposed.

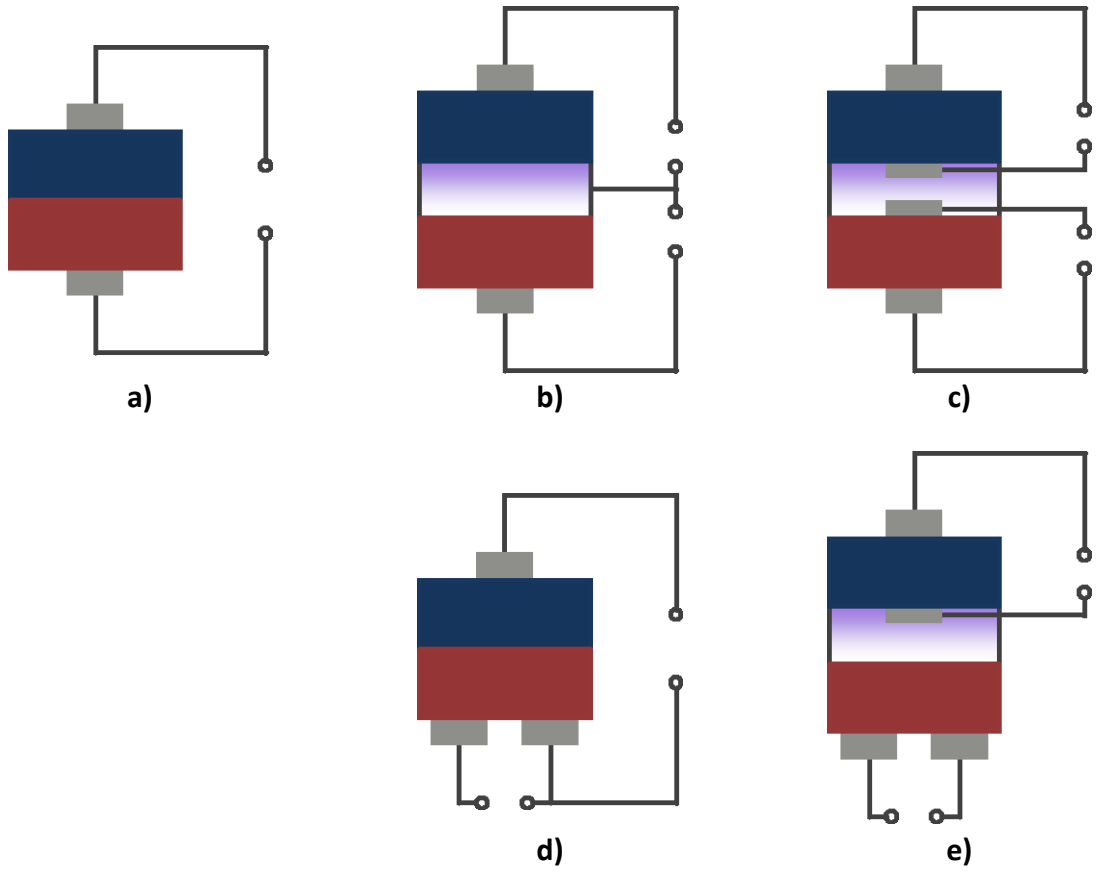


Figure 2.13: Schematics (not to scale) of possible subcell interconnection schemes in a tandem device: a) two-terminal, b) three-terminal with a middle contact, c) four-terminal, d) three-terminal with an interdigitated back contact, and e) four-terminal with an interdigitated back contact. Top and bottom cell are depicted in blue and red colour respectively, electrical (3T with middle contact) and optical/bonding (4T) interconnection layers in purple, and contact fingers in grey.

The first, so-called two-terminal (2T) approach [30,64,66,68,162,163] features one electrode (or terminal) for each species of charge carrier (i.e. electrons and holes), shared by both subcells (cf Figure 2.13a). This approach allows for a simple monolithic device architecture and therefore potentially straightforward fabrication route and module integration. However, both subcells must be current matched since they are connected in series and thus the subcell providing the lower current limits the tandem's overall current and, concomitantly, its overall PCE. Current matching can be achieved for well-defined standard test conditions in a lab-based environment e.g. by adjusting the top cell's absorber thickness [69], its band gap, or by means of light trapping [162]. On the contrary, current matching might not be easily achieved in a real-world application with fluctuating weather conditions and varying spectral composition. However, it has been found that the FF of a current mismatched tandem improves as compared to the matched case, therefore slightly mitigating the current-mismatch induced PCE loss [66].

The second common interconnection scheme provides each subcell with its own contacts for both species of charge carriers, and is therefore referred to as the four-terminal (4T) approach [65,67] (cf Figure 2.13c). Here, no current matching is necessary because both subcells are electrically decoupled. However, separate subcell manufacturing with additional terminals, elaborate contact aligning to minimise shading losses, and more expensive module integration [164] render this approach rather challenging. It is worth noting though that 4T tandems can also be realised using an IBC bottom cell [67,75] (cf. Figure 2.13e), which circumvents an otherwise necessary elaborate alignment of the top cell's rear and bottom cell's front electrode and thereby minimises the fabrication complexity.

In this thesis, an as yet rather unconventional approach utilising only three terminals (3T), introduced in 1980 by SAKAI *et al.* [70], is investigated (cf Figure 2.13b). Here, both subcells are interconnected in a monolithic device architecture, as in 2T tandem devices, featuring a separate contact for one species of charge carrier (e.g. holes) of their own while the contact for the other species (e.g. electrons) is shared, enabling therefore ideally electrical decoupling, as in 4T [76]. 3T tandem solar cells combine thus the advantages of the 2T and 4T concept but circumvent their abovementioned respective drawbacks on the device level. As for module integration of 3T devices, an interconnection scheme resulting in the same amount of required inverters as for 2T has been proposed [164].

2.3.3 Three-Terminal Devices with Interdigitated Back-Contact

The implementation of a third terminal in a 3T tandem device can basically be achieved in two ways. The first (as described in the previous section) would be a configuration wherein a recombination layer in between both subcells serves as a third terminal as initially proposed [70] and experimentally realised for several absorber materials, such as different III–V semiconductors [70], a-Si:H/µc-Si:H [72], and perovskite/c-Si [71]. This configuration, however, inevitably leads to parasitic absorption within this relatively thick (usually more than 100 nm) layer. The latter is required for effective lateral current transport.

That is why a more favourable design would feature a third terminal at the device's rear side, i.e. an IBC solar cell (cf Figure 2.13d). This architecture was theoretically proposed in 2000 for III–V semiconductors in combination with Si and Ge by NAGASHIMA *et al.* [73]. For the former combination, an experimental realisation [74] and theoretical investigation by means of numerical simulations with the aim of getting a deeper understanding of the subcells' interplay [75,76] has been reported. Numerical simulations focussing on the electrical behaviour of an IBC bottom cell when injecting different top cell currents (i.e. simulating different operating points in a 3T tandem) have been carried out, showing that the combined power output is independent of the top cell's current density [77].

Although different theoretical investigations on the electrical [78] and optical [79] properties of 3T tandem devices featuring an IBC bottom cell (henceforth referred to as IBC 3T) combining perovskite and c-Si absorbers have been reported, no such device has been realised experimentally so far. This thesis will therefore present the first perovskite/c-Si-based IBC 3T tandem devices. A corresponding article has been published in ACS Applied Energy Materials [165].

3 Fabrication and Characterisation of IBC SHJ Solar Cells

This chapter gives a comprehensive overview over the fabrication and characterisation methods used within this thesis. The preparation routes of the herein investigated devices are described and possible impacts of process parameters are discussed. As for characterisation methods, measurements to obtain both electrical and optical properties are introduced and ways to further analyse the gained data are demonstrated. Furthermore, all employed equipment is introduced. The chapter concludes with a brief introduction of electrical modelling that is conducted within this thesis to shed light on the electrical behaviour of the herein investigated devices.

3.1 Deposition Techniques

This subsection introduces all relevant deposition techniques necessary for the fabrication of the herein investigated devices. First, each particular method is described and afterwards the therefore employed equipment is introduced.

3.1.1 Plasma-Enhanced Chemical Vapour Deposition

Since the SHJ concept relies on the interaction of a c-Si wafer with intrinsic and doped a-Si:H layers, depositing such thin films is an essential step in the fabrication of these devices. There are several techniques that can be utilised for this purpose [80] whereof here only plasma-enhanced chemical vapour deposition (PECVD) is used. PECVD is a vacuum technique in which plasma is created from a precursor gas (mixture); the thus formed radicals react with the surface of a substrate to form a layer. Depending on what material is to be deposited, different precursor and doping gases can be applied. In the case of a-Si:H, silane (SiH_4) is always used as precursor gas. Depending on the doping type either diborane (B_2H_6; for depositing a-Si:H(p)) or phosphine (PH_3; for depositing nc-Si:H(n)) are used as doping gases. Hydrogen (H_2) is added to the plasma for the purpose of hydrogenation either already during the deposition or afterwards in form of hydrogen plasma treatment (cf. section 2.1.4) The ratio of SiH_4 and hydrogen is called silane dilution and is a critical parameter that

determines the growth conditions and morphology of a-Si:H layers [96] (cf. section 2.1.5). Process temperature, pressure, gas flows, and electrode power play a critical role and need to be carefully adjusted as they will influence chemical composition and electrical properties of deposited layers required for SHJ solar cells (cf. sections 2.1.4 and 2.1.5). A general precondition for any PECVD process is that the chemical reaction by-products must be gaseous to enable their easy removal from the reaction chamber. Silicon nitride (SiN_x) is deposited as an ARC using SiH_4 and ammonia (NH_3). Table 3.1 summarises the relevant deposition parameters of all PECVD layers used in this thesis.

Table 3.1: Deposition parameters for all PECVD layers used in this thesis.

Layer	*Precursor gas(es)*	*Gas flow(s) [sccm²]*	*Gas pressure(s) [bar]*	*Process temperatures [°C]*	*Electrode power [mW/cm²]*	*Deposition time* * *[s]*
a-Si:H(i)	SiH_4, H_2	300, 300	$1.33 \cdot 10^{-3}$	190	16	16
HPT	H_2	1500	$3.33 \cdot 10^{-3}$	190	16	120
a-Si:H(i)†	SiH_4, H_2	400, 400/ 60, 1380	$3.33 \cdot 10^{-3}$/ $4.00 \cdot 10^{-3}$	190	16	6/ 16
a-Si:H(p)‡	SiH_4, H_2, B_2H_6	55, 540, 100	$2.67 \cdot 10^{-3}$	205	16	12 + 33
nc-Si:H(n)	SiH_4, H_2, PH_3	10, 3000, 6	$1.20 \cdot 10^{-2}$	185	200	126
SiN_x	SiH_4, NH_3	50, 200	$1.07 \cdot 10^{-3}$	185	80	150

* Deposition times refer to optimised PECVD process for non-masked samples (i.e. the photolithography process) on planar substrates; the deposition times might differ for other substrate types and shadow-mask process depositions.

† multilayer passivation (cf. section 4.4); the first line refers to the a-Si:H(i)/c-Si interfacial layer, the second to the two identical surface layers facing minority and majority charge carrier contact; if only one line is shown for a certain parameter, it is identical for all layers

‡ In this thesis, a graded emitter is used (cf. section 2.2.4); the first term of the deposition time refers to the graded, the second to the non-graded, highly doped part.

All layers are deposited in a semi-industrial AKT1600 PECVD cluster tool manufactured by Applied Materials operating at radio frequency (RF; 13.56 MHz). Up to four wafers with a diameter of 5”, or one wafer with 6” diameter, can be loaded onto a carrier of 30 × 30 cm² dimensions, of which six can be loaded at once into the load lock of the cluster tool. From there, each carrier is moved by a robotic arm into one of three available process chambers.

Two of them are dedicated to intrinsic and p-type a-Si:H respectively while the third is used for nc-Si:H(n) and SiN_x. All chambers but that dedicated to depositing a-Si:H(i) are further used to clean and precondition all carriers necessary for a process in advance. Each chamber is cleaned and preconditioned accordingly prior to the actual deposition of a certain layer. Further publications using the AKT1600 tool described here can be found in [97,98,124,156,166].

3.1.2 Sputter Deposition

Sputtering belongs to the so-called physical vapour deposition (PVD) techniques. As opposed to PECVD where layer deposition is achieved by means of chemical reactions, PVD processes are based on physically removing material from a source, transporting it to a substrate, and finally forming a layer by means of adhesion, condensation, or adsorption. Just like PECVD, sputtering is conducted in a vacuum chamber. A target consisting of the desired material to be deposited is bombarded with ionised argon plasma. For sufficiently high particle velocities, the high atomic mass of an argon atom (amounting to nearly 40 u) ensures high momentum and thus kinetic energy upon impact on the target. Detached target ions are then accelerated towards a substrate by means of an electric field where they are adsorbed and form a layer. Regarding the deposition of TCOs, oxygen can be added to the gas mixture to enhance the transparency of the deposited layer, but this will, however, reduce its conductivity.

Sputtering of TCO onto a-Si:H inevitably leads to damage of the substrate's surface [167] and is thus not applicable for porous or soft substrates, or if the layers that are to be sputtered on are very thin. Reducing the power density of the process can mitigate this issue since this leads to a softer deposition but, unfortunately, also to a prolonged process (for similar final thicknesses) and potentially unstable plasma conditions [168]. Another possible option for counteracting sputter damage induced to a-Si:H is therefore post-deposition annealing. Sputter damage mainly occurs, apart from physical damage by particle bombardment, due to the formation of dangling bands induced by short-wavelength plasma luminescence [167]. Annealing then leads to the redistribution of hydrogen within the a-Si:H layer and the subsequent saturation of these newly generated dangling bonds [91,114] (cf. also section 2.1.4).

In this thesis, mainly ITO and, to a lesser extent, IZO are sputtered at room temperature in a sputter tool fabricated by Roth & Rau using the following parameters: an RF power of 70 W, a base pressure of $5 \cdot 10^{-7}$ mbar, a working pressure of $6 \cdot 10^{-3}$ mbar, an argon-to-oxygen-ratio of 0.2%, and gas flows of 36.8 sccm (argon) and 3.2 sccm (hydrogen). The tool comprises a dedicated load lock that contains a circular 8" (in diameter) carrier. Up to two 4" wafers can positioned on the carrier and are fixed with heavy glass pieces. After evacuating the load lock, the carrier is loaded into the sputter chamber where it rotates with 1 min^{-1} while the deposition is conducted.

3.1.3 Thermal Evaporation

Thermal evaporation is another vacuum-based PVD technique. Here, a solid source material is transformed into its gaseous phase by applying heat. The vaporised material is then transferred to a substrate that is positioned above the source with the side that is to be deposited on facing down. The evaporated material condenses at the much colder substrate surface and thus forms a layer. Due to very low kinetic energies of the deposited particles, no damage is induced to the substrate's surface. In this thesis, a Creamat 350 tool manufactured by CREAVAC was used to evaporate Ag and Al with usual thicknesses of 1.5 and 2.0 µm respectively at a working pressure of $5 \cdot 10^{-6}$ mbar. The process chamber comprises two evaporators, each of which can contain two tungsten crucibles holding the source material in form of pellets (Ag) or rods (Al). At the top of the chamber up to four 4" wafers can be attached, which rotate continuously during the entire evaporation process to ensure a spatially uniform deposition.

3.2 Auxiliary Preparation Techniques

In this subsection, preparation techniques that precede or are used during the actual solar cell fabrication (i.e. the deposition and patterning of layers) are introduced. This includes specifically surface texturing, wafer cleaning, and laser ablation.

3.2.1 Surface Texturing

In the context of IBC SHJ solar cells, surface texturing serves two purposes. First, random pyramidal structures ensure increased photon absorption probability by means of better light in-coupling and enhanced internal reflection [9,10], which leads to high j_{sc} values especially when applied to the front side of a wafer. Second, since IBC SHJ solar cells feature contacts on the rear side only, texturing increases the active contact area and helps thus mitigating FF losses.

In this thesis either double-side textured (DST) or single-side polished (SSP, with the other side textured) wafers are used. For DST, as-cut wafers are immersed in a lowly concentrated potassium hydroxide solution to remove saw damage. Afterwards, the actual texturing is conducted in an anisotropic etching solution containing highly concentrated (50%) potassium hydroxide and a commercial CellTexUltra component manufactured by ICB GmbH & Co. KG. For SSP, either double-side polished wafers or wafers with one side polished (and the other left untreated: 'as-cut') are used. A thick PECVD SiO_x is deposited on one of the polished sides (or the only, in the latter case) as a protective layer. The wafers are then textured using the same solutions as for DST, with the SiO_x being removed afterwards with hydrofluoric acid (HF) or buffered HF [169]. Figure 3.1 shows scanning electron microscope images from two different angles of a pyramidal textured c-Si surface prepared by the wet-chemical procedure described above.

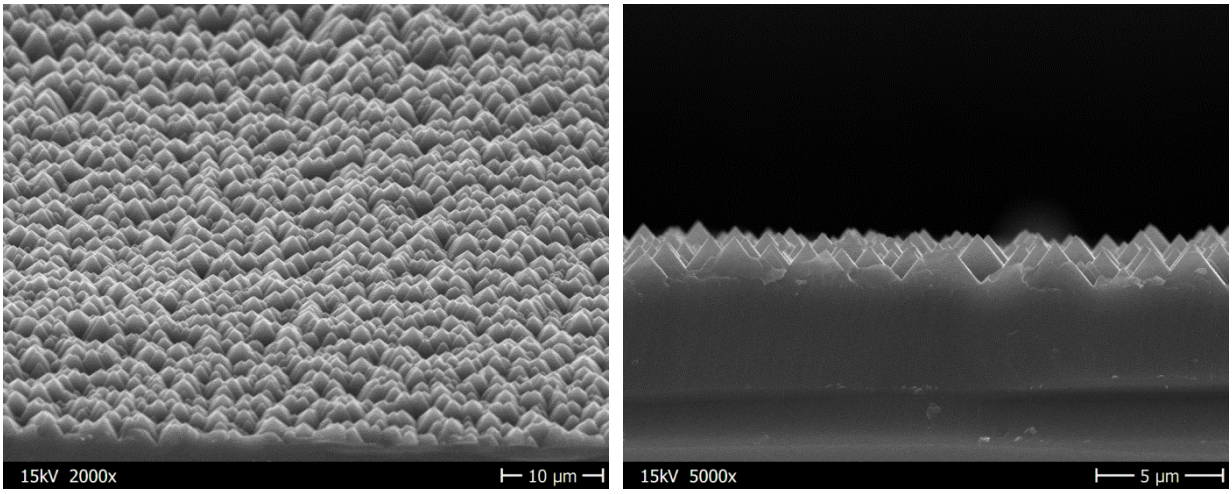


Figure 3.1: Scanning electron microscope images of a textured surface as used within in this thesis: a) angled top view, b) cross section. The pyramid heights amount to approximately 1–2 µm

3.2.2 Wafer Cleaning

Wafer cleaning is an essential part of fabricating highly efficient solar cells because untreated surfaces can contain organic and metallic contaminations [170] that have to be removed as they can severely impair the performance of Si-based solar cells [171,172]. Within this thesis, solely the common so-called RCA cleaning procedure (stemming from Radio Corporation of America, i.e. the company that invented the process), sometimes also referred to as 'standard clean', is used. Details are given in [173]. Here, the procedure is briefly outlined. It consists of two essential cleaning steps (referred to as RCA 1 and 2) that aim on removing organic and metallic contaminations respectively. Its basic concept is to chemically grow an oxide layer on the wafer's surface, in which particles and contaminants are embedded, followed by the removal of that oxide with HF. RCA 1 makes use of hydrogen peroxide (H_2O_2), which is a strong oxidant, and ammonium hydroxide (NH_4OH) as active components, diluted in deionised water (DI). RCA 2 consists of H_2O_2, hydrochloric acid (HCl), and DI. Lastly, it is to be mentioned here that the removal of oxides can also be conducted by means of plasma etching, therefore avoiding the use of HF [174,175].

3.2.3 Laser Ablation

A pulsed neodymium-doped yttrium aluminium garnet laser with a wavelength of 1064 nm (IR) and a pulse length of 12 ps at a frequency of 50 kHz manufactured by ROFIN-BAASEL Lasertech is used for all laser processes within this thesis. The laser power is set to 100 mW and the scribing velocity to 15 mm/s. Laser ablation is usually conducted by repeatedly treating the section that is to be cut. The number of necessary iterations depends on thickness and surface morphology of the processed substrate. Laser ablation is used in several occasions: foremost for the fabrication of shadow masks (cf. section 3.3.2) and the preparation of wafers for fabrication and measurement purposes (cf. sections 4.1.1 and 4.1.2), but also for wafer quartering (cf. sections 4.3.2) and cutting out bottom cells as part of the IBC 3T manufacturing process (cf. section 5.1.1). A comprehensive overview over the utilisation of laser ablation in solar cell production can be found in [43].

3.3 Patterning Techniques

IBC solar cells usually feature plain front-side layer stacks but come at the cost of increased rear-side complexity. In order to form alternating n and p-type regions and to separate the external contacts, layer patterning is an inevitable task in these devices, either after a full-area deposition or *in-situ* during the manufacturing process. Here, the two main patterning techniques used in this thesis are introduced.

3.3.1 Photolithography

Photolithography is a very accurate patterning process that stems from microelectronics where it is widely used for the fabrication of multilayer devices, such as integrated circuits or transistors [100]. In photovoltaics (PV), photolithography is sometimes used as an auxiliary technique to pattern thin layers, particularly SiO_x [137], but is usually avoided or restricted to a minimum amount due to its complex and relatively expensive nature and PV being a strongly cost-driven industry [6]. With that said, highly efficient (i.e. PCEs ≥ 25%) IBC SHJ solar cells are often manufactured utilising photolithography [27–29,176], which is one of the major obstacles for their broad market introduction [40]. In the following, a general description of the photolithography process used in this thesis is given; its basic principle is depicted in Figure 3.2. A more in-depth, process-focused description can be found in section 4.1.1.

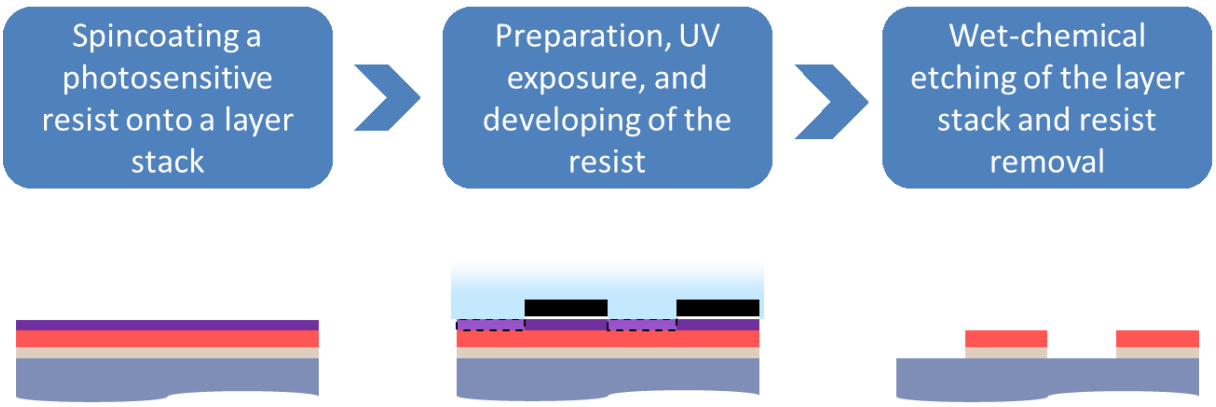


Figure 3.2: Basic principle of a photolithography patterning step: a photosensitive positive resist (purple) is applied to a layer stack (grey and red) on a substrate (blue-grey), prepared, and exposed to UV irradiation through a mask (black). The exposed portions are then removed in an alkaline solution and the thus structured resist serves as an etching mask for the layer stack underneath, which is afterwards patterned wet-chemically or by means of dry etching. Finally, the resist is removed by solvents. Note that, in the sketch, also the passivation layer (grey) is removed during the process, rendering thus a repassivation step necessary.

A bare c-Si(n) wafer is prepared according to sections 3.2.1 and 3.2.2 and layers that are to be patterned are deposited onto it by means of the techniques described in section 3.1. In a first step, a photosensitive resist is spincoated onto the substrate. The required thickness of that layer depends on the wafer's surface morphology and is adjusted by the rotation speed: 4500 min^{-1} for polished, 800 min^{-1} for textured wafers (for photoresists used in this thesis). There are two kinds of resists: positive and negative. Using a positive resists (which is illustrated in the sketch of Figure 3.2) yields a layer pattern after structuring that is identical to that of the used mask. For negative resists, the opposite is true: the final layer pattern is identical to the non-masked areas (further details can be found below and in section 4.1.2).

For the photolithography process discussed in this thesis, only the positive photoresist AZ 4533 manufactured by AZ Electronic Materials GmbH is used and therefore the following description focusses mainly on this type. After drying, the resist needs to be further treated: (i) in a so-called soft bake, the remaining solvents are driven out of the layer at 90 °C for 30 min in an oven; (ii) since the soft bake also removes all water that is needed for the subsequent photochemical reaction, the wafers are then put into a hydration chamber for several minutes at a relative humidity of 70–80%. The substrates containing the now hardened and rehydrated resist layers are then transferred to an MA-6 mask aligner manufactured by SÜSS MicroTec. Here, different masks, containing the desired pattern either as a positive (for positive resists) or a negative (for negative resists), can be used. The masks consist of an opaque chromium layer, patterned by electron-beam evaporation, atop a quartz glass substrate. The wafers are aligned to the mask by using optical microscopy and alignment markers on substrate and mask. Subsequently, those parts of the substrates that are not covered by the mask are exposed to ultraviolet (UV) irradiation for several seconds (7 s for polished, 20 s for textured wafers).

During exposure, the resist's long molecular chains are ruptured, and the resist can then be removed in a solution containing 0.6% sodium hydroxide (35–45 s for polished, 1:30–1:45 min for textured wafers). Non-exposed resist areas with still intact molecular chains are not affected by this so-called developing procedure. Another temperature treatment at 115 °C for 30 min in an oven (hard bake) is conducted to make the now patterned resist withstand the following etching step. Table 3.2 lists all etching solutions and

common durations for materials used in this thesis. Finally the resist is removed by consecutive bathing in acetone, isopropyl alcohol, and DI.

Table 3.2: Etching solutions and durations for materials used in this thesis. Concentrations and mixing ratios are given where known. Trade names (if applicable) are given in quotation marks.

Layer (stack)	*Thickness*	*Etchant*	*Etching duration*
a-Si:H(i)/a-Si:H(p)	(5/15) nm	'Poly-Si-etchant': nitric acid (HNO_3), 65%, phosphoric acid (H_3PO_4), 85%, HF, 50%, DI – 30:10:1:15	20 s
a-Si:H(i)/nc-Si:H(n)	(5/15) nm	tetramethylammonium hydroxide (TMAH), 2.5%	2–3 min
a-Si:H(i)[†]	100 nm	TMAH, 2.5%	10–15 min
SiO_x[‡]	< 2 nm	HF, 1%	1–3 min
ITO	150 nm	HCl, 10%	20 s
Ag	1.5 µm	H_2O_2, 31%, NH_4OH, 25%, DI – 1:1:4	20–30 s
Al	2.0 µm	'Gravure Aluminium': H_3PO_4, HNO_3, acetic acid (CH_3COOH)	3–5 min (at 50–55 °C)

[†] a-Si:H(i) layer for protecting the front-side SiN_x layer during wet-chemical processes (especially HF) that is removed upon device finalisation

[‡] native or RCA (cf. section 3.2.2) oxides; the etching duration depends on the oxide's type and thickness

3.3.2 *In-Situ* Patterning with Shadow Masks

As discussed at the beginning of the previous section, the commonly used photolithography-based contact preparation of IBC SHJ solar cell yields high PCEs but is complex, lengthy, and expensive; and therefore not applicable in industrial fabrication. It is thus crucial to simplify the fabrication processes while maintaining exceptional solar cell properties. Various promising alternative patterning techniques for the substitution of photolithography have been presented in the past that rely either on plasma etching [31,32], laser patterning [44–47], *in-situ* patterning using shadow masks during PECVD [34–40], or a combination of the above [33]. In this thesis, a shadow-masks process is developed as a photolithography-free patterning technique. As-cut c-Si wafers prepared by the Czochralski process (Cz) [11] with a thickness of approximately 150 µm are used as mask material. A laser is used to cut the desired patterns into said wafers (cf. section 3.2.3 for further details). In

total, four different mask designs are produced: two for the doped layer's deposition (n and p) and two for the patterning of the metallisation stack (ITO/Ag or Al) of each polarity. The metallisation patterning masks feature slightly narrower openings in order to avoid metallising the overlap area in between p and n-regions and thus shunting. After that, a temperature treatment is conducted to release mechanical stress induced by laser ablation. Therefore, the masks are annealed on a hotplate, gradually increasing the temperature up to 600 °C at 50 °C steps with dwell times of 3 min each. A brief HF dip concludes the mask preparation. In Figure 3.3, the general principle of the shadow-mask process is depicted. Its detailed description is given in section 4.1.2.

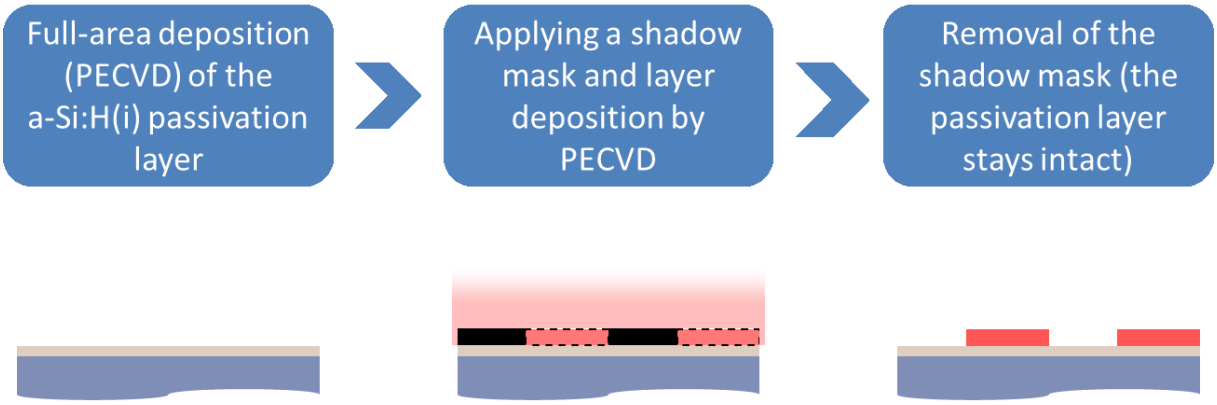


Figure 3.3: Basic principle of the shadow-mask process: a hard mask (black) is attached to a surface-passivated (grey) substrate (blue-grey) and then transferred into a PECVD chamber where a doped layer (red) is deposited. After unloading, the mask is removed. Note that the passivation layer stays intact during the process.

3.4 Characterisation Techniques and Employed Equipment

All necessary characterisation methods to determine both electrical and optical properties of the devices investigated here are presented in this subsection. It is further subdivided into describing the particular method, introducing the employed equipment, and discussing further utilisation of the gained data. The techniques discussed here are introduced in the order in which they are used within the fabrication process.

3.4.1 Transient Photoconductance Decay

As discussed in section 2.1.3, every recombination mechanism is characterised by a recombination lifetime τ_i, with the shortest thereof governing the overall τ_{eff}. Since bulk

lifetimes of lowly defective c-Si(n) wafers as used in this thesis are very high [61], the main limiting factor in this context is $\tau_{surface}$, and measuring τ_{eff} is therefore always an examination of the surface passivation quality. Measuring minority charge carrier lifetimes is done by means of transient photoconductance decay (TrPCD) [177]. Here, a non-metallised (until after TCO deposition) c-Si wafer is positioned in a cabinet above a coil forming a resonant circuit with it. A short intense light pulse (flash) leads to the generation of excess minority charge carriers within the wafer, thus changing its conductivity, which is then measured inductively [178]. Since no external metal contacts are attached to the wafer, the generated charge carriers will eventually recombine and the conductivity will thus decline over time. The transient of this decay is indicative of τ_{eff} as described by equation (3.1) [179] where Δn represents the excess minority charge carrier concentration (calculated from the changed conductivity) and the term $d\Delta n/dt$ is the net recombination rate.

$$\tau_{\mathrm{eff}}(\Delta n) = -\frac{\Delta n}{\mathrm{d}\Delta n/\mathrm{d}t} \tag{3.1}$$

For measuring TrPCD on IBC devices, however, the occurrence of artefacts and overestimated lifetimes (especially in the low-injection regime) has been reported. This has been explained by the alternating polarities of the IBC contacts forming an n/p/n-phototransistor where the lateral current flow in the dark is limited. Upon illumination, the conductivity rises as the now operating transistor allows for an increased lateral current flow within the doped layers. This increased conductivity for low-illumination conditions, however, is not related to an increased Δn and therefore not to the actual effective minority charge carrier lifetime [180]. For a non-diffused (i.e. heterojunction) device, such as the ones investigated in this thesis, however, this phenomenon only occurs at very low Δn (close to 10^{13} cm^{-3}) and needs therefore only to be taken into account when FEP effects, for which the low-injection regime is relevant [108], are discussed.

All TrPCD measurements are carried out by using a Sinton WCT-100 setup in transient mode to evaluate the passivation quality after almost every deposition and patterning step of the fabrication process (as described in sections 4.1.1 and 4.1.2). If not stated otherwise, given lifetimes represent values for $\Delta n = 10^{15}$ cm^{-3}, which is equivalent to the illumination intensity of one sun (i.e. 100 mW/cm² or standard illumination intensity) for the expected effective minority charge carrier lifetimes of the devices discussed in this thesis. Figure 3.4a shows

Δ*n*-dependent minority charge carrier lifetime graphs for two surface-passivated samples with similar one-sun illumination but different low-intensity response.

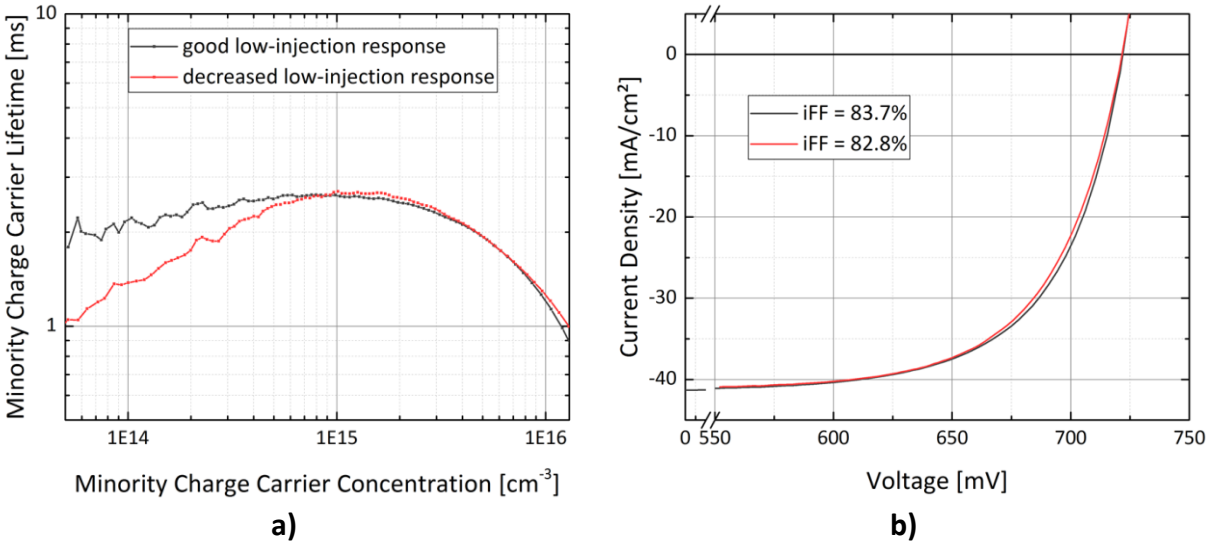


Figure 3.4: a) Minority charge carrier lifetime vs minority charge carrier concentration for two samples with different low-injection response; b) implied current–voltage characteristics calculated from the data given in a). Note the break in the abscissa in order to emphasise the MPP region.

Minority charge carrier lifetime data is further used to calculate the implied fill factor (iFF), which can be understood as an upper limit for the FF, assuming an ideal, only recombination limited solar cell neglecting the effects of parasitic resistances (i.e. R_{shunt} being infinite and R_s zero) [181]. Ideally, the voltage of a solar cell is equal to the E_F-separation under illumination [147] and can thus be described by equation (3.2) [181].

$$V(\Delta n) = \frac{k \cdot T}{q} \cdot \ln\left[\frac{(n_0 + \Delta n) \cdot (p_0 + \Delta n)}{n_{\mathrm{i,eff}}^2}\right] \tag{3.2}$$

Here, $n_{i,eff}$ is the effective intrinsic charge carrier density (amounting to approximately 10^{10} cm^{-3} in c-Si [100]); n_0 and p_0 denote the equilibrium densities of electrons and holes respectively, which depend on the wafer doping. The current density corresponding to a certain $V(\Delta n)$ can be calculated using equation (3.3) [181].

$$j(\Delta n) = j_{\mathrm{ph}} - q \cdot W \cdot \frac{\Delta n}{\tau_{\mathrm{eff}}} \tag{3.3}$$

Equations (3.2) and (3.3) are then used to calculate the implied *j*–*V* characteristics (iV_{oc}, ij_{sc}, and iMPP) and thereby determine the iFF according to equation (2.6). In Figure 3.4b, the calculated implied *j*–*V* characteristics corresponding to the lifetime data presented in

Figure 3.4a are shown. Although featuring similar τ_{eff}s under one-sun illumination, the sample with poorer low-injection response exhibits also a slightly lower iFF due to an inferior field-effect passivation and, since doped layers are involved, contact selectivity [122,143].

3.4.2 Photoluminescence

Since TrPCD measurements only yield a mean value over a large investigated area (i.e. the area of the 2" coil, which has to be fully covered by a wafer to yield trustworthy results), photoluminescence (PL) measurements are conducted to investigate whether the passivation is spatially homogeneous. This is, again, done at several steps during the fabrication procedure so that every lifetime measurement can be related to a PL image. Ideally, the passivation quality is independent of the position on the wafer (as shown in Figure 3.5) and thus the measured τ_{eff} is representative of the entire wafer, which in reality is not always the case and will be discussed in respective sections. PL is based on radiative recombination (cf. section 2.1.3). Non-contacted samples are positioned inside a dark cabinet and charge carriers are generated by an array of light-emitting diodes (LEDs) with a wavelength of 650 nm. A filter, blocking all wavelengths shorter than 800 nm, is attached to a modified near-IR-sensitive camera with a charge-coupled device (CCD) sensor. This ensures that only photons with a wavelength of about 1100 nm, stemming from radiative recombination within c-Si are detected, and not e.g. the reflected excitation illumination, which would otherwise easily drown out the much fainter signal of interest. During the set integration time (in this thesis 500 ms and 1000 ms are used), the incident photons are counted and summed up for each pixel of the camera's sensor to generate an image. In all PL image presented in the following, bright areas (i.e. high photon counts) represent areas with pronounced radiative recombination and therefore a low defect density at the wafer surface. Dark areas, however, indicate that charge carriers recombine otherwise (mainly surface recombination) and the surface passivation is thus poor. All PL images presented throughout this thesis are non-calibrated as quantitative data regarding the surface passivation is gained by TrPCD measurements and PL imaging is merely used to examine the spatial homogeneity of that passivation. However, the brightness scale of all presented images is similar (in terms of photon counts per pixel), so that comparing different non-calibrated PL images is still possible.

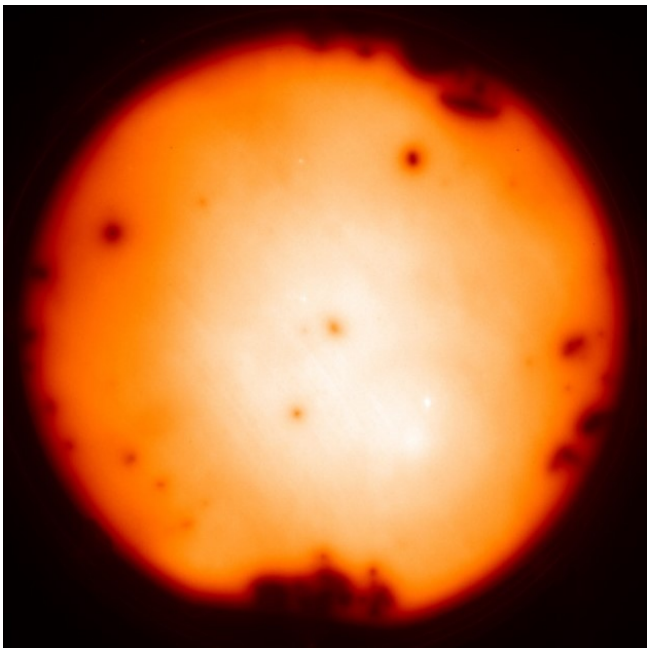
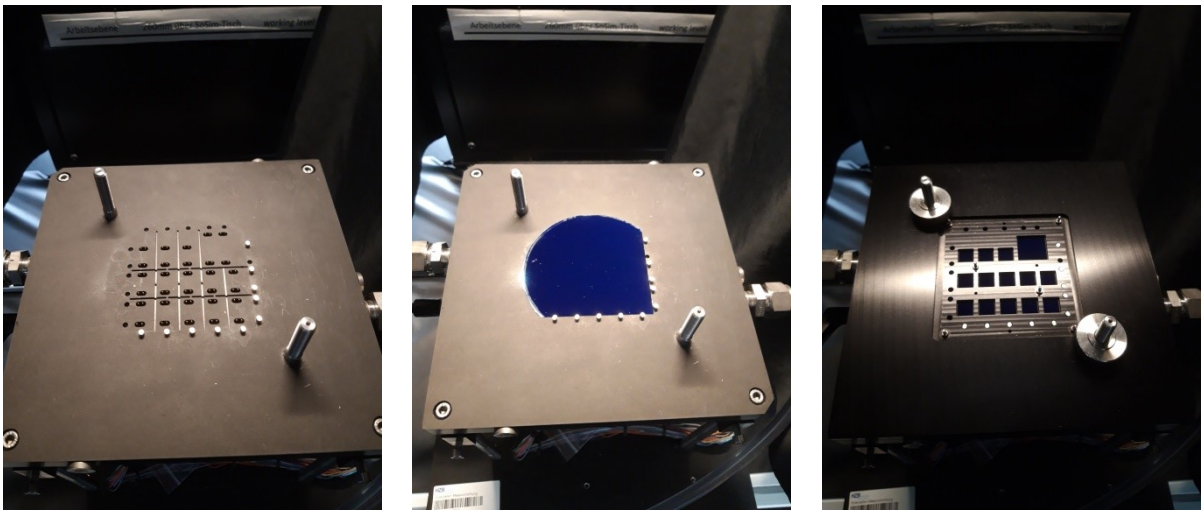


Figure 3.5: A non-calibrated photoluminescence image of a wafer exhibiting a spatially homogeneous surface passivation. Dark spots at the edge are due to manual sample handling using tweezers.

3.4.3 Current–Voltage Characteristics

Illuminated and dark *j–V* characteristics of finalised solar cells are obtained by measurements conducted with so-called sun or solar simulators. Here, part of the sun's electromagnetic spectrum relevant for solar cell applications is imitated by using either several lamps or LEDs. Upon illuminating the investigated solar cell, an external bias voltage is swept from at least 0 V (i.e. j_{sc}) to V_{oc} conditions whilst the resulting current density at every operating point is measured. To allow for comparability of different solar cells, these measurements are carried out under so-called standard test conditions (STC) that encompass the following criteria: AM1.5g spectrum (representing the global solar spectrum at sea level, measured with the sun at an elevation angle above the horizon of roughly 48° [102,182]), illumination intensity of 100 mW/cm² ('one-sun' intensity), and cell temperature of 25 °C. Two different class AAA sun simulators, one using a tungsten and a xenon lamp (Wacom WXS-156S-L2), and the other (Wavelabs Sinus 70) using LEDs, are employed in this thesis. For the first, a dedicated measurement chuck is used (cf. Figure 3.6).



a) **b)** **c)**

Figure 3.6: Measurement chuck and alignment procedure for obtaining current–voltage characteristics of the IBC SHJ solar cells investigated here with a sun simulator Wacom WXS-156S-L2: a) before sample alignment, b) after sample alignment (here, the blue front side of a wafer that is to be measured can be seen), c) after sample masking.

For illuminated one-sun *j–V* measurements, the cells are appropriately masked (cf. Figure 3.6c) to define their designated illumination area (da; this includes the active solar cell areas as defined by the dimensions of the minority and majority charge carrier contact, but excludes bus bars, which are used for probing) [183] and avoid overestimating especially the j_{sc}. Measurements in the dark are conducted with the same setup but in absence of illumination and the solar cells covered with an opaque black cloth.

The comparison of dark and illuminated *j–V* characteristics is an effective and accurate way to determine the R_s of a solar cell [184]. For this, the dark *j–V* graph is shifted so that its j_{sc} matches the j_{sc} of the illuminated curve. The R_s can then be calculated from the voltage difference at MPP of the two graphs using equations (3.4) and (3.5) [184].

$$R_s = \frac{V_{\mathrm{MPP,dark}} - V_{\mathrm{MPP,illuminated}} - (|j_{sc}| - |j_{\mathrm{MPP}}|) \cdot R_{\mathrm{s,dark}}}{|j_{\mathrm{MPP}}|} \tag{3.4}$$

with

$$R_{\mathrm{s,dark}} = \frac{V_{\mathrm{oc,dark}} - V_{\mathrm{oc,illuminated}}}{|j_{sc}|} \tag{3.5}$$

3.4.4 Illumination-Dependent Current–Voltage Characteristics

Illumination-dependent current-voltage characteristics (SunsVoc) measurements for the determination of so-called pseudo *j*–*V* characteristics and thereby the pseudo fill factor (pFF) are carried out by using, again, the aforementioned Sinton WCT-100 setup. Here, a solar cell under investigation is kept at open-circuit conditions. A short intense light pulse (flash) is applied and both the light intensity and corresponding V_{oc} of the solar cell under test are measured simultaneously, yielding thus multiple measurement pairs of the two parameters. With knowledge of the device's actual j_{sc} determined beforehand (cf. previous section) and due to the linear relationship between illumination intensity and j_{sc}, a sample's pseudo *j*–*V* characteristics can be recreated from this [185]. Under V_{oc} conditions no current is extracted from the device and the effect of the R_s is consequently zero [184]. Therefore, pseudo *j*–*V* characteristics determined entirely under open-circuit conditions are not affected by R_s.

Comparing characteristics obtained by SunsVoc measurements with those obtained from a sun simulator is thus another reliable method for determining the R_s since the latter affects only the sun simulator results. R_s is calculated by dividing the voltage difference at MPP of both graphs by j_{MPP}. There is, however, a caveat when applying this technique: since illuminated *j*–*V* and SunsVoc characteristics are not obtained with the same setup, the measured V_{oc}s might differ from each other. The pseudo *j*–*V* graph is therefore shifted so that its V_{oc} matches that of the illuminated *j*–*V* graph. This results in a slightly larger uncertainty as compared to the dark *j*–*V* method presented in the previous section. Further information regarding this issue is given in section 4.1.3. A thorough analysis comparing iFF, pFF, and actual FF is very insightful and helps to shed light on both recombination and resistance-related loss mechanisms within the devices investigated here. It is conducted in different sections throughout chapter 4.

3.4.5 Transfer Length Method

The transfer length method (TLM), introduced by SHOCKLEY in 1964, is used to determine the specific contact resistivity (ρ_c) of a layer stack [186]. A TLM test structure consists of several metal stripes of equal dimensions ($l \times Z$) but gradually decreasing spacing in between (d_i; cf. Figure 3.7a). The current density is measured between every two adjacent contacts while the voltage is swept from negative to positive values. The resistance of every contact pair is

then calculated from the slope at 0 V and plotted over the respective pad spacing distance. If the contact shows ohmic behaviour, a linear fit can be applied to the data; its intercept with abscissa and ordinate gives twice the (absolute) value of transfer length (L_T) and contact resistance (R_c) respectively (cf. Figure 3.7b). From that, ρ_c can be calculated by using equation (3.6). The spacing in between contacts is limited by the diffusion length, L, of the semiconductor material and must thus not be too large [186].

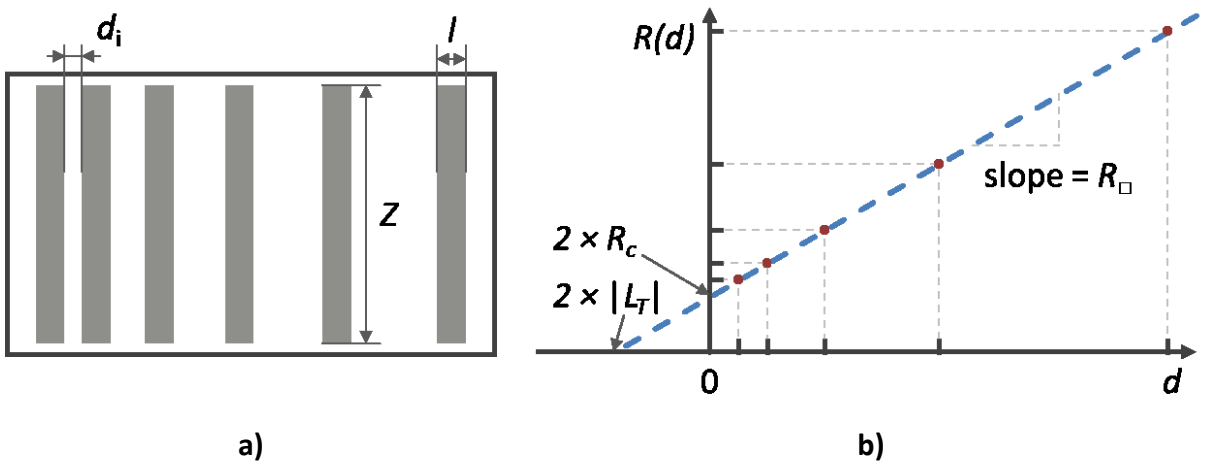


Figure 3.7: a) Schematic of a TLM structure; b) ideal plot of resistance vs measurement pad spacing (d_i), assuming an ohmic contact. The contact resistance (R_c), transfer length (L_T), and sheet resistance ($R_\square$) can be directly extracted from the linear fit as shown in the graph. Reworked from [186].

$$\rho_c = \frac{R_c \cdot L_T \cdot Z}{\coth\left(l/L_T\right)} \tag{3.6}$$

The slope of the linear fit further gives the sheet resistance ($R_\square$) of the wafer (or more generally of the most conductive material of the layer stack that governs the current path in between contacts) and can be calculated by equation (3.7). Multiplying $R_\square$ with the wafer thickness, W, yields the specific wafer resistivity (ρ_{bulk}).

$$R_\square = \frac{R_c \cdot Z}{L_T} \tag{3.7}$$

Since TLM includes current spreading and crowding (locally increased current densities stemming from non-linear current paths beneath or in the vicinity of the contact edges), it is likely to overestimate ρ_c, especially for low ρ_cs where these effects become a dominating contributor to the measured resistance [40,187]. Utilising TLM to determine ρ_c of a contact with different polarity than the wafer doping (here: the p-contact on an n-type wafer)

requires the additional fabrication of a dedicated structure on a suitable substrate of the same polarity because otherwise a blocking junction (i.e. rectifying contact) is formed while TLM necessitates an ohmic contact [40,188–190]. It has been further shown that ρ_c determined by TLM on a wafer (here: p-type) heavily depends on that wafer's doping concentration. The substrate's specific resistivity must therefore be chosen according to the minority charge carrier density at MPP (i.e. the relevant operating point of a solar cell) as obtained e.g. by SunsVoc of a final device [40]. However, the determined ρ_c when using such a carefully selected substrate is likely still overestimated [40] and the thus obtained values must be critically evaluated. A comparative study to investigate the relative differences of various p-contact stacks on the same substrate is nevertheless possible and insightful.

3.4.6 Spectral Response and External Quantum Efficiency

To assess optical losses in a solar cell, spectrally resolved measurements are conducted. Firstly, the spectral response (SR) is measured, which is defined as the photogenerated current divided by the power of the incident irradiation [92]. Theoretically, the SR is maximal for the wavelength corresponding to the material's band gap. Photons with longer wavelengths are transmitted and thus the SR is zero; photons with shorter wavelengths are absorbed, but a fraction of their energy is dissipated as heat. This effect is more pronounced the larger the photon energy becomes, which results in a linearly declining SR for shorter wavelengths (cf. section 2.3.1). Due to reflection and recombination losses, the SR of real-world devices deviates from this ideal triangular shape (cf. Figure 3.8a).

With knowledge of the SR, the external quantum efficiency (EQE), which is defined as the number of generated excess minority charge carriers per incident photon, can be calculated using equation (3.8) [92].

$$EQE(\lambda) = SR(\lambda) \cdot \frac{h \cdot c}{q \cdot \lambda} \tag{3.8}$$

Here, h denotes Planck's constant, c the speed of light (in vacuum), q the elementary charge, and λ the wavelength of the incident light. For an ideal solar cell, the EQE is 1 for photons with wavelengths shorter than that corresponding to the semiconductor's band gap and zero for longer wavelengths since no absorption occurs anymore. This is, again, not achieved in real-world devices. In a c-Si wafer, deviations from 1 in the short-wavelength regime can be

ascribed to losses occurring at the front side (reflection, parasitic absorption in front-side layers, front-surface recombination); those in the long-wavelength regime are rear-side losses (parasitic plasmonic absorption in metal contacts, free-carrier absorption in TCOs, rear-surface recombination); and those reducing the overall EQE are losses due to reflection and broadband absorption (cf. Figure 3.8b).

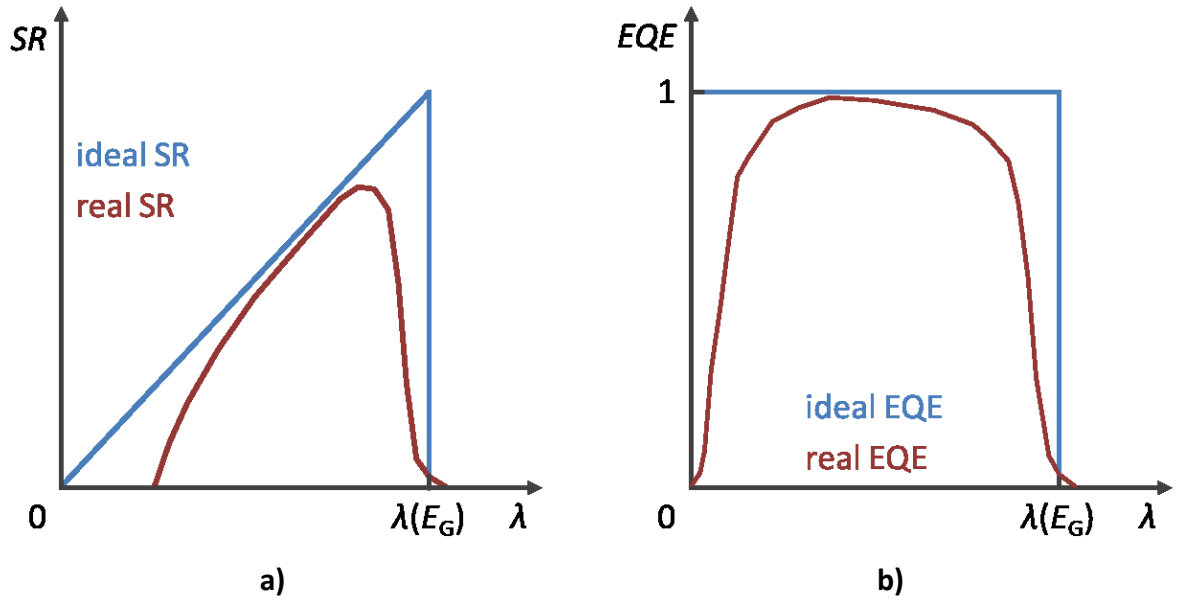


Figure 3.8: Ideal (blue) and real (red) a) spectral response (SR) and b) external quantum efficiency (EQE) of a solar cell. The cutoff wavelength ($\lambda(E_G)$) is defined by the band gap of the used material. Reworked from [92]. Note that no sharp cutoff for the real SR and EQE occurs at $\lambda(E_G)$. Since c-Si is an indirect semiconductor, it usually relies on an additional momentum change provided by lattice vibrations (i.e. phonons) for absolute temperatures greater zero [100]. The energy that phonons carry might be small but is non-zero. Therefore, phonons can also deliver a small amount of energy (in addition to their large momentum change) that allows for the absorption of photons with larger wavelengths than $\lambda(E_G)$. A detailed description of this process is given in [12].

Two setups for measuring the EQE are used over the course of this thesis. The first, which is primarily used, is a home-built small-spot system with a beam size of $(2 \times 5)\,\mathrm{mm}^2$, and halogen and xenon lamps as illumination sources. Measurements are conducted for wavelengths from 300 to 1200 nm with a step size of 10 nm. Blue, red, and IR LEDs as well as a halogen lamp can be used as bias illumination. The second setup features only one halogen lamp as illumination source but a large spot size significantly exceeding the area of the investigated solar cells, which therefore have to be appropriately masked. Wavelengths between 340 and 1200 nm with a 20 nm interval are set by filters mounted on two large filter wheels. Here, an IR LED and a halogen lamp can be used as bias illumination.

3.4.7 Reflection Measurement

Electromagnetic radiation incident on any material is reflected, absorbed, or transmitted. The proportion of these mechanisms varies for different materials and with the wavelength of the incident light, but their sum always equals one. In this thesis, only Si-wafer based devices are investigated and therefore transmission can be largely neglected for relevant wavelengths. The reflection is measured with a Perkin Elmer LAMBDA 1050 UV/Vis spectrometer in the wavelength range from 300 nm to 1200 nm and a step size of 2 nm. To further distinguish reflection from other internal losses, such as recombination and parasitic absorption, the internal quantum efficiency (IQE) can be calculated by using equation (3.9) under the (here judicious) assumption of negligible transmission. The IQE is essentially the fraction of incident light that is absorbed and contributes to the external current of a solar cell.

$$IQE(\lambda) = \frac{EQE(\lambda)}{1 - R(\lambda)} \tag{3.9}$$

3.5 Electrical Equivalent Circuit Simulations

In this subsection, the electrical modelling conducted within this thesis is introduced. Therefore, electrical equivalent circuits of investigated devices are developed and their electrical behaviour is investigated with the numerical modelling tool LTspice [191]. A 'simulation programme with integrated circuits emphasis' (or SPICE for short) is a software tool capable of modelling complex electrical analogue circuits. There is a plethora of such tools whereof LTspice (the LT stems from the provider's former name: Linear Technology; now: Analog Devices) was chosen due to it being free but comprehensive software that has already been used for similar purposes in scientific publications [66]. Equivalent circuit diagrams for specific investigated cases are developed based on the fundamental one and two-diode models as described in section 2.2.3. To extract diode characteristics, namely j_0, n, j_{ph}, and the parasitic resistances R_s and R_{shunt}, one or two-diode models (henceforth abbreviated with 1DM and 2DM respectively) are fit to measured dark (1DM and 2DM) and illuminated j–V characteristics (only 1DM) by using equations (2.8) and (2.9) as well as procedures described in [150,151,192].

Fitting complex equations with multiple variables to measured graphs entails the necessity of numerous iterations. Furthermore, j_0 and n cannot be free parameters simultaneously since this would excessively increase the amount of necessary iterations. Therefore, n is set to a fixed value of 1 (or 1 and 2 for 2DM) whilst j_0 is varied. For the simulation of perovskite solar cells, n is set to 1.5, following typical values reported in literature [66]. After a meaningful solution for j_0 is found, its value is fixed and n is selected as a free parameter. At this point, n usually does not vary much and its final value is therefore close to its initial one. This alternating search algorithm for j_0 and n can be repeated multiple times if necessary. R_s, R_{shunt}, and (for illuminated 1DM fits) j_{ph} are used to verify the resulting fit since they are known from j–V measurements (j_{ph} and R_{shunt}) or have been calculated beforehand (R_s; cf. sections 3.4.3, 3.4.4). Figure 3.9a exemplarily shows measured j–V data along with a 1DM and a 2DM fit. While for the 1DM a slight deviation around the MPP is apparent in an otherwise decent fit, very good agreement is achieved when applying the 2DM. This becomes even more obvious if the current density is plotted semi-logarithmically (cf. Figure 3.9b). The fitting parameters for both models corresponding to Figure 3.9 are given in Table 3.3.

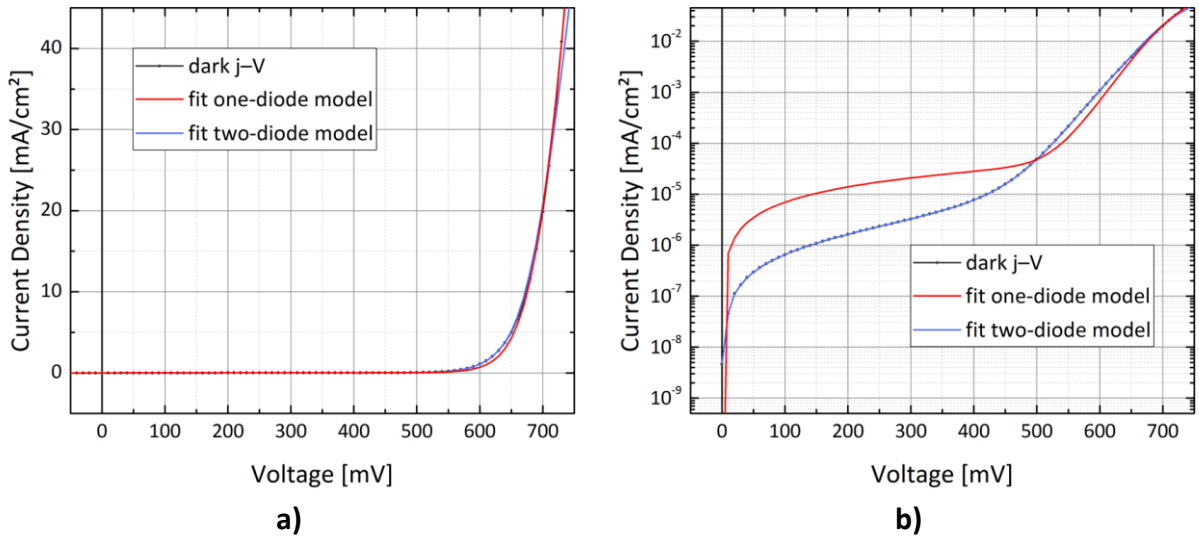


Figure 3.9: Fitting a one (red) and a two-diode model (blue) to measured dark current–voltage characteristics of a solar cell (grey) in a) a linear and b) in a semi-logarithmic plot. The two-diode model agrees very well with the measured data while for the one-diode model deviations around the maximum power point are observed, which becomes especially apparent in b).

Table 3.3: Parameters for fitting both a one (1DM) and a two-diode model (2DM) to the measured dark j–V characteristics of an exemplary IBC SHJ solar cell (as presented in Figure 3.9). Note that a much higher R_{shunt} has to be assumed in case of the 1DM.

Model	$j_{0,1}$ *[A/cm²]*	$j_{0,2}$ *[A/cm²]*	n_1	n_2	R_s *[Ωcm²]*	R_{shunt} *[Ωcm²]*
1DM	4.8×10^{-14}	N/A	1	N/A	0.59	14385
2DM	4.5×10^{-14}	1.4×10^{-9}	1	2	0.80	1200

The fit parameters are afterwards used to parametrise the electrical equivalent circuit and its components (i.e. diodes, resistors, and current sources) accordingly in LTspice. Simulations are then conducted by sweeping certain parameters within the circuit (e.g. currents or resistances) that correspond to external parameters, observed in measurements. Exact details depend on the specific simulation and are explained in respective sections later on in this thesis.

4 Device Preparation and Optimisation of IBC SHJ Solar Cells

In this chapter the two fabrication processes for single-junction IBC SHJ solar cells, based on photolithography and *in-situ* patterning by shadow masks, are described. The optimisation of both processes is discussed with a strong focus on resistive power losses that are attributed to either heterojunction interfaces or to the metallisation scheme. The influence of passivation layer thickness and scheme, rear-side surface morphology, and different contacting approaches is investigated. In addition, electrical equivalent circuit simulations are conducted, were applicable, to get further insight into operating principles and to determine achievable potentials of the chosen device layouts. Detailed FF analyses, including techniques described in sections 3.4.1 and 3.4.3–3.4.5, are carried out to get a better understanding of loss mechanisms during the fabrication process and, accordingly, where modifications must be made. Improving the devices' FFs is key to making them competitive to standard SHJ solar cells and to enhancing their overall PCE. Apart from that, their increased fabrication complexity must be streamlined in order to make them appealing to industrial manufacturers. To this end, a simplified shadow-mask process is introduced here. First results regarding this process have been published in [37].

4.1 Device Fabrication Processes

In this chapter, a general description of the two device fabrication processes used in this thesis is given. In addition, the typical characterisation procedure that is applied to all samples under investigation is introduced.

4.1.1 Photolithography Process

In the following, the optimised standard photolithography process used in this thesis is briefly described. For a general description of photolithography and an illustration of an exemplary patterning step, the reader is referred to section 3.3.1. Deviations and adjustments necessary to meet certain requirements of an experiment are given in the respective section. A flow chart of the photolithography process is depicted in Figure 4.1.

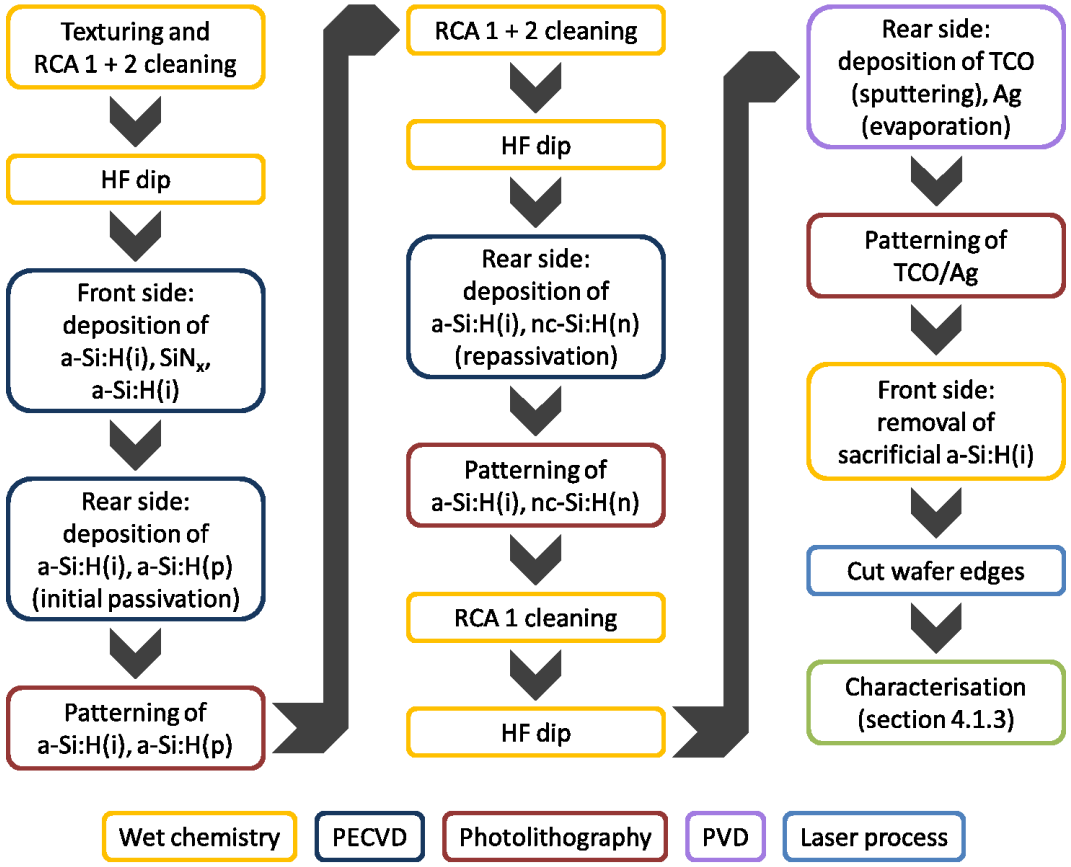


Figure 4.1: Flow chart of the photolithography process.

The photolithography process starts with wafer preparation by means of texturing and successive RCA cleaning according to sections 3.2.1 and 3.2.2. All samples are prepared using 4" (primarily n-type) c-Si wafers fabricated by the float-zone process (FZ) [100] with a nominal specific wafer resistivity (ρ_{bulk}) of 1–5 Ωcm. Either double-side textured (DST) or single-side polished (SSP) wafers (with the other side textured) and an approximate thickness of 260 µm or 280 µm respectively are used. Initially, the wafers are dipped in a diluted HF solution (1%) for 3 min to remove the oxide that has formed on the surface after the RCA cleaning.

Directly afterwards, they are loaded into an AKT1600 PECVD cluster tool (cf. section 3.1.1) to deposit the front-side stack consisting of 15 nm a-Si:H(i) as surface passivation, 70 nm SiN_x as ARC, and 100 nm a-Si:H(i), the latter serving as a sacrificial layer to protect the SiN_x. Subsequently, the wafers are flipped and positioned on a clean and preconditioned carrier to deposit the minority charge carrier contact stack consisting of 5 nm a-Si:H(i) and 15 nm graded (cf. section 2.2.4) a-Si:H(p), which is afterwards patterned by photolithography (cf. section 3.3.1).

Since the surface passivation is removed on parts of the wafer during patterning of the minority charge carrier contact, a repassivation step is necessary. Another RCA cleaning and HF dip precede this deposition, which is also conducted by PECVD. The majority charge carrier contact stack consists of 5 nm a-Si:H(i) and 15 nm nc-Si:H(n), and is also patterned by photolithography. A final RCA 1 cleaning and HF dip are conducted before two wafers at a time are loaded into a Roth & Rau sputter tool (cf. section 3.1.2) to deposit 150 nm of ITO on the now patterned rear side of the devices. A following evaporation of a 1.5 µm Ag layer with a CREAVAC Creamat 350 tool (cf. section 3.1.3) completes the metallisation stack, which is afterwards patterned by a final photolithography step. Utmost care needs to be taken when structuring ITO because a prolonged etching duration leads to undercutting (i.e. the wet-chemical etchant removing the side walls of, here, ITO beneath metal contact and photoresist) that reduces the actual metallised contact area and thereby the FF of final devices [193]. Undercutting can in general also be problematic for structuring metal layers, but over the course of this thesis they have been found to be less prone to it than ITO. For a direct Al metallisation, sputtering of ITO is omitted and thermal evaporation of Ag is replaced by evaporating a slightly thicker (2.0 µm in total) Al layer.

Cell fabrication concludes by wet-chemically removing the front-side protective a-Si:H(i) layer and laser-cutting two wafer edges so that they fit into a dedicated measurement chuck (cf. section 4.1.3) for determining their *j*–*V* characteristics (cf. section 3.4.3). In total, on each wafer there are twelve small cells (with a designated illumination area, da, of 1 × 1 cm²; cell numbers 1–12) with varying emitter ratios (cf. Table 4.1 and Figure 4.2b) but a constant pitch (i.e. emitter + BSF + metallisation gap of 30 µm) of 1.2 mm, one large cell (2 × 2 cm² da; cell number 0), one cell for measuring the EQE (cf. section 3.4.6; cell number 13), and two TLM structures for determining the contact resistivity (cf. section 3.4.5). Figure 4.2a shows the rear side of a fully prepared wafer after a successful photolithography process.

Table 4.1: Lateral finger dimensions of doped a-Si:H and nc-Si:H layers used in devices fabricated by photolithography in this thesis. The total width of the solar cells is 1 cm or 2 cm (cell 0).

Cell number	*Minority charge carrier contact width [µm]*	*Majority charge carrier contact width [µm]*	*Minority charge carrier contact coverage ('emitter ratio') [%]*
1, 9	1006	164	86
2, 10	906	264	77
3, 5, 7, 11	756	414	65
0, 4, 6, 8, 10	606	564	52

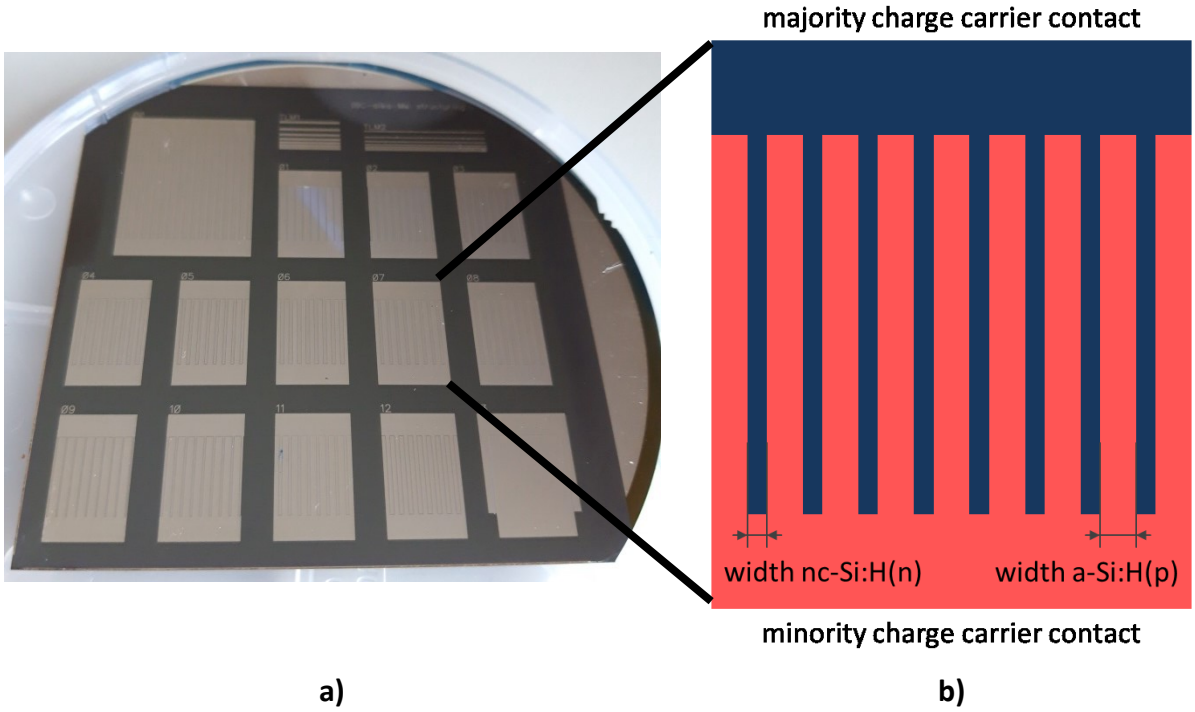


Figure 4.2: a) Rear side of a fully prepared wafer featuring IBC SHJ solar cells fabricated with the photolithography process; b) schematic of an IBC SHJ solar cell with realistic lateral dimensions (representing cells 3, 5, 7, and 11 in Table 4.1)

4.1.2 Shadow-Mask Process

This process has been developed in cooperation with Johann-Christoph Stang, a former fellow PhD candidate, and is based on the valuable preliminary works of Felix Nicolas Kandsorra (Masters student) and Anne-Claire Billault-Roux (summer student). Later progress was achieved with the support of Dimitri Belostotski (Masters student). Parts of the data regarding this process, presented throughout this thesis have already been published in [37,50,194]. A general description of the shadow-mask process along with an illustration of an

exemplary patterning step is given in section 3.3.2. A flow chart of the process is depicted in Figure 4.3. The following section describes the applied procedure in more detail.

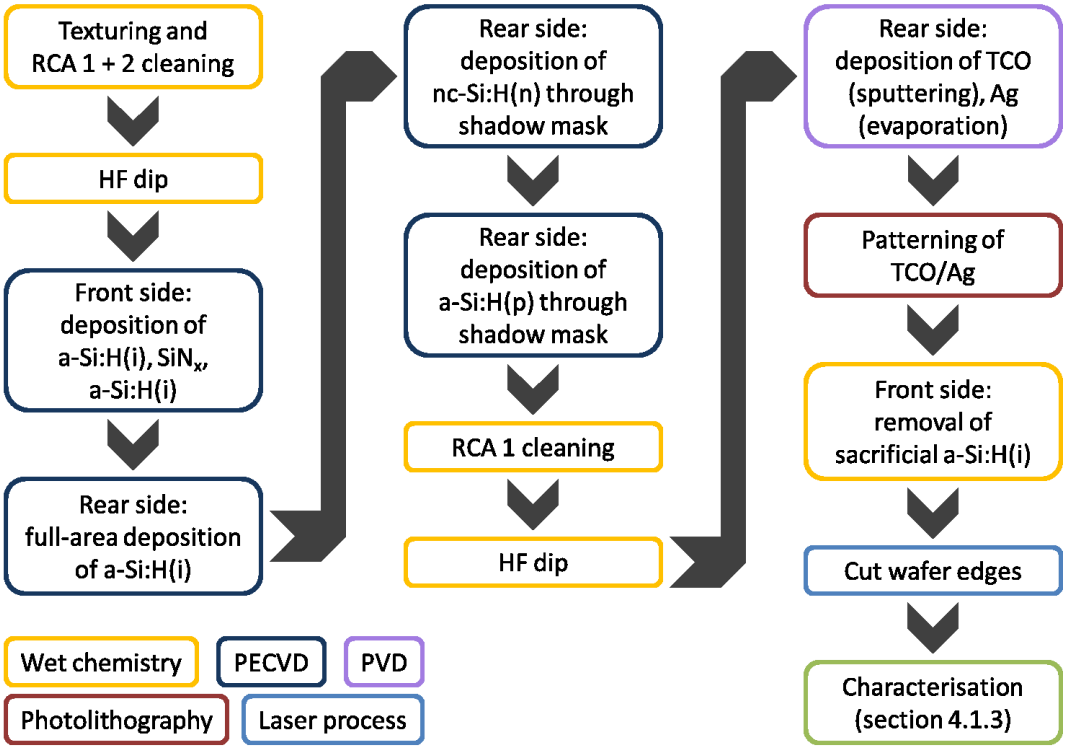


Figure 4.3: Flow chart of the shadow-mask process.

Up to the point where the front-side stack has been deposited, the solar cell fabrication process itself is the same as that based on photolithography (as described in the previous section). After this step, wafers (SSP or DST) are flipped onto a clean and preconditioned carrier, but only the a-Si:H(i) rear-side passivation layer (instead of the full minority charge carrier contact stack) is deposited by using an AKT1600 PECVD cluster tool. After this, the wafers are unloaded and – together with one mask, starting with the n-type deposition mask – attached to a designated sample holder (cf. Figure 4.4a). Alignment is achieved by means of pins on the sample holder and holes in both wafer and mask (laser-cut prior to the fabrication process). One of these holes has approximately the same size as the sample holder's pins and the other hole is slightly elongated to account for thermal expansion of the sample holder [195].

After depositing only nc-Si:H(n) onto the designated majority charge carrier contact areas defined by the mask's slits, the wafers are unloaded, attached to p-type sample holder and mask and reloaded into an AKT1600 PECVD cluster tool where a-Si:H(p) is selectively

deposited through another mask. The thus *in-situ* patterned solar cell precursors are further prepared by HF-dipping, followed by full-area deposition of ITO/Ag or Al, just as in the photolithography process.

The contact stack is then structured using a simplified photolithography-like process that involves applying a negative-type photoresist (here, AZ nLOF 2070 manufactured by AZ Electronic Materials GmbH is used), UV exposure through laser-cut masks with adapted dimensions (cf. section 3.3.2), resist developing, and wet-chemical etching of the metallisation stack. Negative-type resist is much easier to handle than its positive-type counterpart used in the photolithography process since no rehydration and hard bake are necessary, and the time required for soft bakes is much shorter (100 °C for 6 min on a hotplate). Only a brief additional annealing step (105 °C for 2 min on a hotplate) after UV exposure is required. Here, as opposed to positive-type resists, long molecular chains form only upon UV exposure and temperature treatment, making the resist stable in developing (here: an industrial alkaline solution containing TMAH) and etching solutions.

The fabrication process is concluded just like its photolithography counterpart, i.e. by removing the protective front-side a-Si:H(i) layer and laser-cutting two wafer edges. Figure 4.4b shows the rear side of an *in-situ* patterned solar cell fabricated with the shadow-mask process.

Each wafer features seven small cells (1 × 1 cm² da) and one large cell (2 × 2 cm² da) with a constant pitch of 1.7 mm and fixed finger widths of 1.2 mm and 0.5 mm for p and n-regions respectively. The deposition of of a-Si:H(p) through a mask does not form sharp edges. Instead, they are blurred or tapered, and therefore a-Si:H(p) is also deposited in part beneath the mask's edges. In order to counteract this circumstance, the slit width of that mask is slightly reduced to an opening of 1.1 mm. This adaptation prevents the formation of a large overlap area that, when metallised, would lead to shunting, or otherwise makes an unfavourably large metallisation gap necessary that, in turn, limits the FF [193].

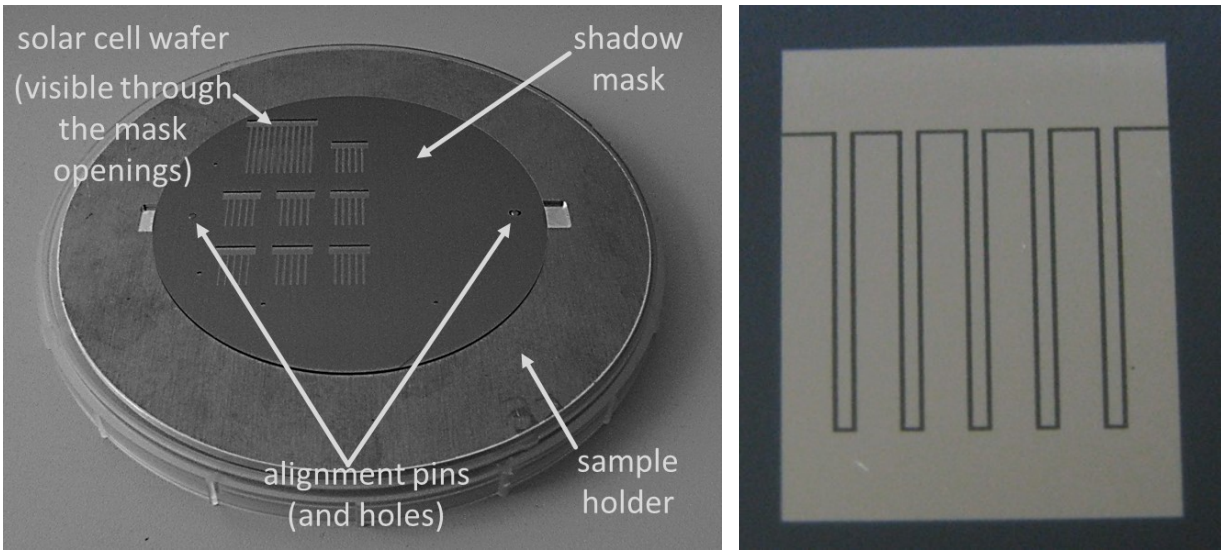


Figure 4.4: a) Alignment procedure in the shadow-mask process: wafer and mask are attached to the sample holder by means of pins and holes; b) rear side of a fully prepared IBC SHJ solar cells fabricated with the shadow-mask process. Taken from [37] and added labels to a).

4.1.3 Applied Characterisation Procedure During Fabrication

Several characterisation techniques have been introduced in section 3.4. Here, the order in which they are applied and exemplary results are shown and discussed for the standard photolithography process. It involves the same characterisation steps as the shadow-mask process but also some additional ones that are not conducted (due to not being necessary) in the latter.

As already mentioned earlier, TrPCD and PL measurements are conducted after the following steps during fabrication process: the initial and repassivation PECVD process (for the shadow-mask process after completion of *in-situ* patterning), and after patterning of the majority charge carrier contact stack. These measurements are not carried out after emitter stack patterning because large areas of the wafer‘s rear-side surface are not passivated at this point and TrPCD would therefore exhibit low τ_{eff}s while PL images would be mostly dark. Furthermore, since it is not possible to conduct TrPCD measurements on a metallised solar cell (cf. section 3.4.1), only PL images are taken of the final devices. Figure 4.5 shows an exemplary development of τ_{eff} over the course of a full photolithography process.

The first blatant observation is a decrease in τ_{eff} of roughly 2 ms at an excess minority charge carrier concentrations, Δn, of 10^{15} cm^{-3} after the repassivation process. The majority charge carrier contact consists of nc-Si:H(n), which is known to be superior in conductivity as

compared to its amorphous counterpart. Achieving decent surface passivation in terms of a high τ_{eff} at the same time is, however, at least challenging [96–98].

The drop in τ_{eff} between majority charge carrier contact deposition and patterning is solely due to small non-passivated windows around alignment markers necessary for the photolithography process (visible as black dots in Figure 4.6c and d) and is not indicative of a real τ_{eff} in the solar cell areas. Apparently, τ_{eff} of samples both after repassivation and patterning of the majority charge carrier contact increases for $\Delta n \leq 10^{14}$ cm^{-3}. This is due to the artefact that an IBC pattern causes in TrPCD measurements under low-injection conditions as described in section 3.4.1 and in more detail in [180].

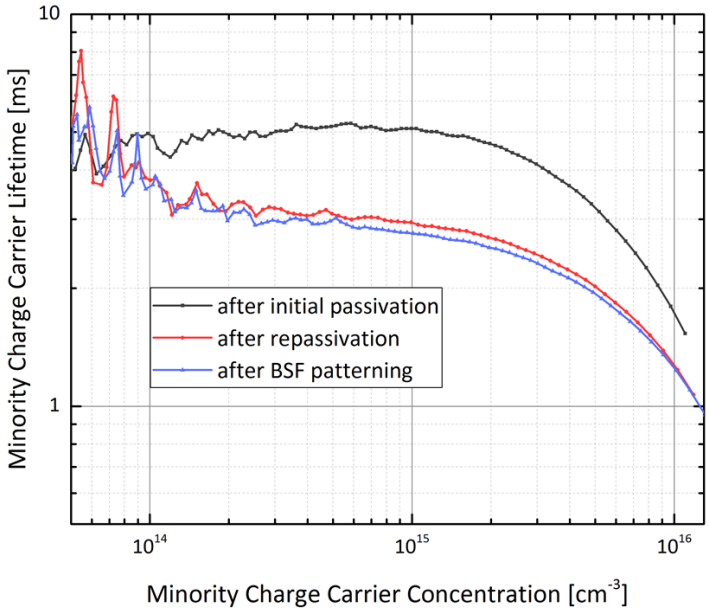


Figure 4.5: Development of minority charge carrier lifetime over minority charge carrier concentration after different patterning steps during the photolithography process.

In Figure 4.6, PL images corresponding to the development of τ_{eff} (Figure 4.5) over the course of an entire photolithography process are depicted. After initial passivation with the minority charge carrier contact stack (i.e. a-Si:H(i)/a-Si:H(p)), a spatially uniform passivation is evident (Figure 4.6a). As discussed above, the majority charge carrier contact stack (i.e. a-Si:H(i)/nc-Si:H(n)) yields a poorer surface passivation, which can be seen from a lower τ_{eff} in Figure 4.5 and from a noticeably lower PL intensity in areas where the stack is deposited (Figure 4.6b). After patterning the majority charge carrier contact stack (Figure 4.6c), areas surrounding the central region, which contains the actual solar cells, and spots where the alignment markers are positioned appear dark because these areas are now no longer

passivated. In Figure 4.6d, a wafer after completion of the photolithography process is depicted. The solar cell areas are clearly visible since the now applied metallisation stack serves as a rear reflector. Two of the solar cells are shunted and therefore appear dark because the photogenerated charge carriers recombine at the metal electrodes rather than radiative in the bulk.

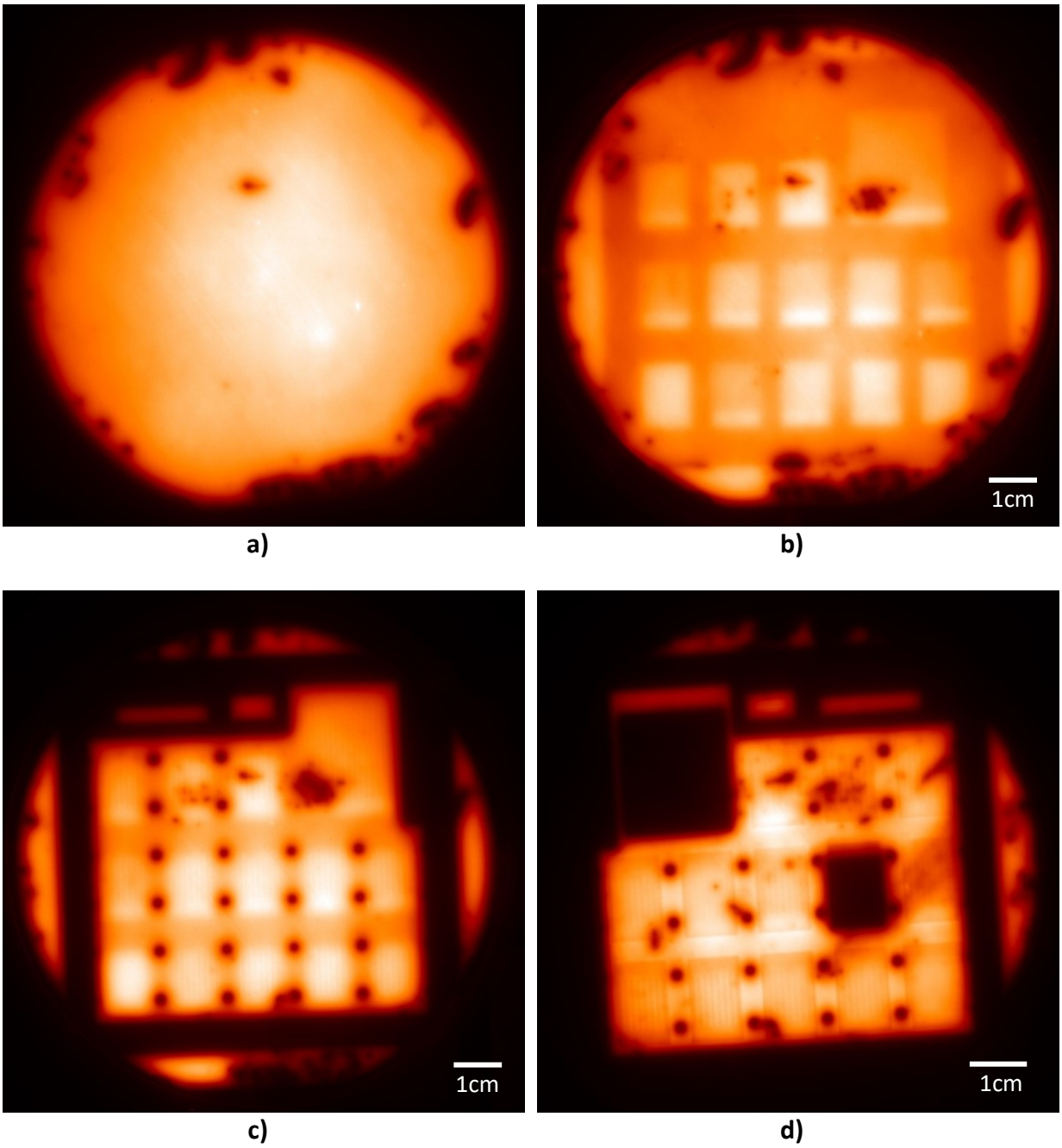


Figure 4.6: Non-calibrated photoluminescence images of the same wafer during different stages of the photolithography process: after a) initial passivation, b) repassivation, c) BSF patterning, and d) metallisation patterning. Two solar cells in d) appear black because they are shunted. Note that the PL images in Figures a–c) are taken while the wafer's rear side faced the camera. The PL image presented in Figure d) is taken with the wafer's front side facing the camera.

Following the discussion above, TrPCD measurements before and after BSF patterning can be seen as upper and lower limit respectively for calculating the iFF as described in section 3.4.1. Minority charge carrier density dependent τ_{eff}s for both a photolithography and shadow-mask patterned device is given in Figure 4.7a alongside the resulting implied *j*–*V* characteristics calculated from that data (Figure 4.7b). Further information regarding implied characteristics and their discussion can be found later on in this section and in section 3.4.1.

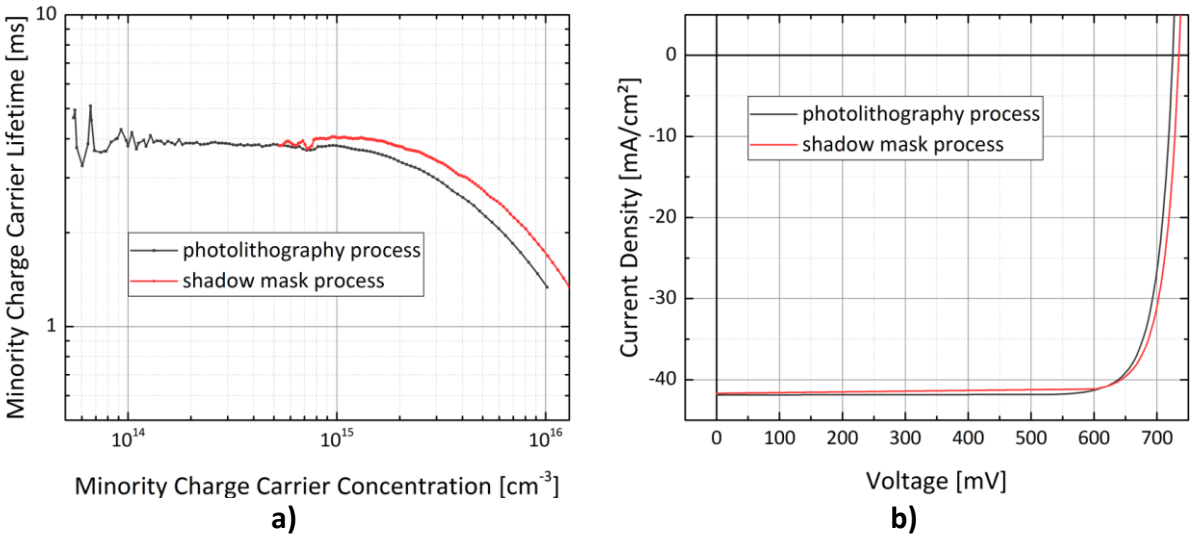


Figure 4.7: Comparison of the photolithography and the shadow-mask process in terms of a) minority charge carrier lifetime over minority charge carrier concentration, b) implied current–voltage characteristics calculated from the data presented in a). Reworked from [37].

After the completion of solar cells, dark and illuminated *j*–*V* characteristics are determined by using a dual-lamp sun simulator introduced in section 3.4.3. During this measurement, the samples are annealed at 200 °C in 7 min increments for up to 35 min. They are remeasured in between every annealing step. This thermal treatment is done for several reasons. Firstly, it is known that depositing TCOs by sputtering onto a-Si:H induces damage to that layer by generating defects, such as dangling bonds (cf. section 3.1.2 for further details) [167]. Subsequent annealing leads to redistribution of hydrogen within a-Si:H that will repassivate these newly introduced recombination centres [91,114] and thus improve surface passivation and increases the V_{oc}. Secondly, since all used TCOs are sputtered at room temperatures, which is necessary because they have to be structured during photolithography, their crystallinity and thus their conductivity is low [196]. Annealing leads to post-deposition crystallisation, thereby an increased conductivity, and ultimately a gain in FF of up to 4%$_{abs}$ and (to a lesser extent) in j_{sc} of approximately 0.5 mA/cm² (or 1–1.5%$_{abs}$).

These advantages are, however, counteracted by the degradation of the emitter stack upon annealing. Depending on the energetic position of E_F within the a-Si:H(i) buffer underneath a-Si:H(p), hydrogen effusion occurs already at temperatures lower than those necessary for the crystallisation of ITO. Further details are given in section 2.1.5. This phenomenon eventually reduces the V_{oc} since hydrogen is essential for the passivation process. Annealing is therefore conducted in short steps (cf. above) to find the optimum where the predominance of beneficial over detrimental effects is still given. It is worth noting that this performance improvement is permanent, which has been confirmed by remeasuring solar cells that have been stored under a nitrogen atmosphere for approximately nine months. Although at first, a slight decrease in V_{oc} and FF is observed, it is small as compared to the initial improvement upon annealing. Furthermore, these parameters can be recovered to their original values after an annealing step at 190 °C for 3 min, likely again due to the redistribution of hydrogen.

In a next step, SunsVoc measurements are conducted (cf. section 3.4.4) and with it, pseudo *j*–*V* characteristics are obtained. For a comprehensive FF loss analysis, knowledge of R_s is essential. Therefore, R_s is calculated using the two methods introduced in 3.4.3 and 3.4.4. There, it has been argued that the comparison of dark and illuminated *j*–*V* characteristics (henceforth referred to as 'dark *j*–*V* method') yields slightly more reliable results since all necessary input data (i.e. dark and illuminated *j*–*V* characteristics) are measured with the same setup under equal conditions whereas in the SunsVoc method, the pseudo *j*–*V* graph must be manually shifted along the voltage axis to match the V_{oc} of the illuminated one-sun measurement. This consideration, however, has to be put into perspective because (i) both methods yield similar R_s with usually slightly lower values (in average 0.2 Ωcm²) for the dark *j*–*V* method (cf. Figure 4.8a), and (ii) the deviation of R_s values determined by dark *j*–*V* and SunsVoc method is statistically independent of the amount the pseudo *j*–*V* curve has to be shifted (cf. Figure 4.8c).

Upon examining Figure 4.8a more closely, one can observe several aspects. First, there is a pronounced, roughly linear correlation between R_s and FF, so either is a good indicator of the other.

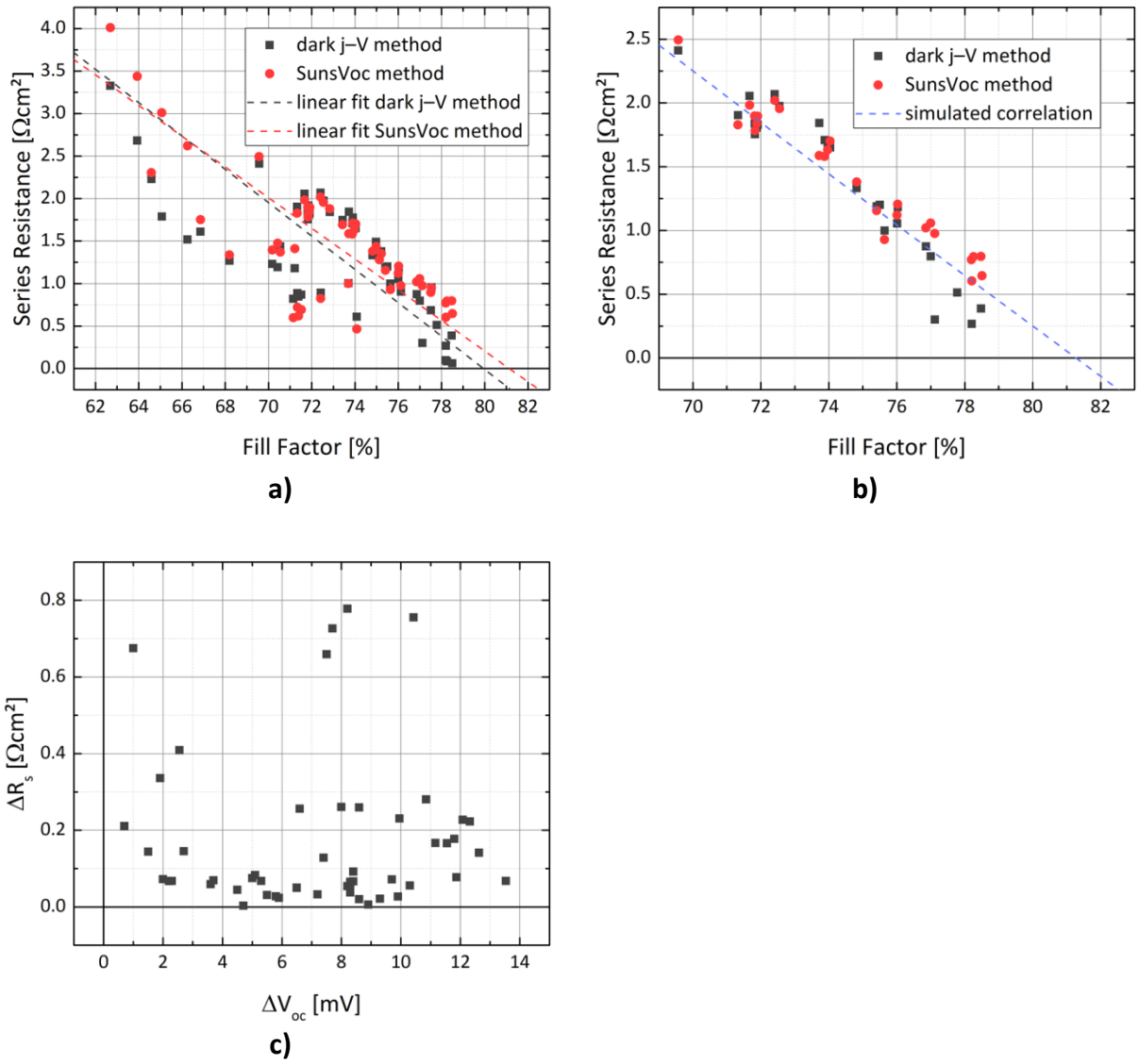


Figure 4.8: a) Correlation of fill factor and series resistance extracted by both the SunsVoc (red) and dark j–V method (black) for solar cells fabricated during the course of this thesis. A roughly linear dependence is found. The spread in the data is due to the devices' different V_{oc}s as can be seen from b) where exemplarily only results for solar cells with a V_{oc} of 710 ± 10 mV are shown, revealing a clearly linear correlation of FF and R_s, which is also verified by electrical equivalent circuit simulations (dashed blue line); c) the difference in series resistance extracted by SunsVoc and dark j–V method is statistically independent of the amount, the pseudo-current–voltage characteristics graph has to be shifted. See text for further details and discussion.

Second, there is an observable FF data spread around the mean linear fits, which is largely due to the final devices' different V_{oc}s. Higher V_{oc}s allow for higher FFs at a set R_s; or, conversely, two solar cells with different V_{oc}s and R_ss can still exhibit the same FF. Achieving higher FFs well above 80% is thus directly depending on achieving higher V_{oc}s [11]. This becomes more evident, when only solar cells with a similar V_{oc} (here exemplarily: 710 ± 10 mV) are used for evaluation. Now the linear correlation of R_s and FF is clearly visible (cf. Figure 4.8b), which has also been reported by [184]. Electrical equivalent circuit

simulations using LTspice and a two-diode model are conducted and also confirm the experimental results for a clear linear trend (dashed blue line in Figure 4.8b) is found if V_{oc} does not alter (here: 716 mV). The model's components are parameterised so that the solar cell characteristics of measured and simulated devices match.

Third, the intersection of linear fit applied to the data and the abscissa represents an upper limit for the FF of the specific devices investigated here. It amounts to 79.9% and 81.1% for dark *j*–*V* and SunsVoc method respectively. The highest FF achieved in this thesis is 79.2% with a calculated R_s of 0.24 Ωcm² (dark) or 0.48 Ωcm² (SunsVoc), rendering thus the latter method apparently more credible because such a low R_s as predicted by the first method (which would be even lower than that of the world-record device of [28] with reported 0.32 Ωcm²) is rather unlikely for the proposed a-Si:H(p)/ITO contact. Another way of interpreting this circumstance is to regard values determined by both dark and SunsVoc method as lower and upper limit respectively of the R_s, which is in agreement with [184].

After the measurements and calculations conducted so far, a FF loss analysis can be undertaken. Implied (i.e. calculated from TrPCD measurements), pseudo (i.e. derived from SunsVoc measurements), and illuminated *j*–*V* characteristics of an exemplary solar cell are depicted in Figure 4.9a; Figure 4.9b shows the contribution of recombination and resistance-related losses that lower the FF. A FF discrepancy between implied and pseudo characteristics is due to additional recombination losses after contact formation. Usually, this drop is very low if the chosen contact scheme and/or process does not significantly impair the passivation quality. A negatively impacted passivation upon contact formation and thus increased recombination at the semiconductor/metal interface leads to a strong decrease in V_{oc} and therefore to a huge difference between iFF and pFF. The discrepancy between pseudo and illuminated FF is directly related to resistive losses as discussed in detail above. This decrease between pFF and FF is usually more pronounced than that between iFF and pFF, suggesting that high R_s values are the predominant contributor to FF losses. Investigating ways to lowering resistive losses is therefore the main focus of optimisations conducted in the following sections. It must be noted that the iFF is derived from non-annealed samples whereas both pFF and FF are measured after prolonged annealing. Especially τ_{eff} benefits already from a short annealing step. For instance, a temperature treatment of 7 min at 200 °C on a hotplate increases τ_{eff} by approximately 1 ms,

which results in an iFF increase of 0.5–1.0%$_{abs}$. The given iFFs are therefore a lower limit, which can lead to the rare case of the pFF being equal or even marginally larger than the iFF. This is, however, not a real effect and can be largely ascribed to the thermal history of processed samples. Furthermore, this circumstance implies that recombination losses are systematically underestimated. However, as have been found experimentally over the course of this thesis, the major part of τ_{eff} improvement occurs within the first few minutes of annealing. Therefore, the difference between annealed and non-annealed iFF cannot be much larger than the 1%$_{abs}$ stated above.

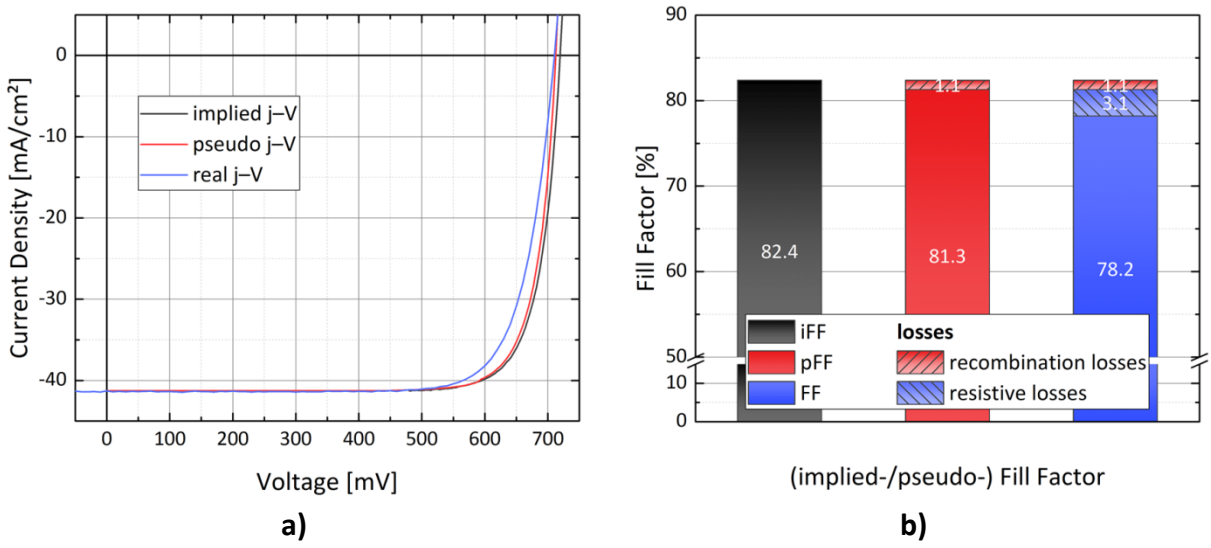


Figure 4.9: a) implied (black), pseudo (red), and illuminated current–voltage characteristics (blue) for a solar cell fabricated with the photolithography process, and b) Fil factor losses of that very solar cell. Note the break in the ordinate that is introduced to make the loss portions more noticeable.

The R_s of an IBC SHJ solar cell can be divided into different parts whereof the p-contacts ρ_c holds by far the largest share [39,40] (cf. sections 2.1.6 and 2.1.7 for further details). Directly measuring the p-contact's ρ_c is unfortunately not possible for a device based on an n-type wafer (cf. sections 3.4.5). Its value, however, can be estimated by using appropriate models with knowledge of the other R_s contributors [39,40,197,198], or by fabricating a suitable p-type TLM structure as discussed in section 3.4.5. In the first case, mainly the n-contact's ρ_c, and the bulk-related R_s contributions (both lateral and vertical) need to determined. The former is directly measured by means of the TLM structures that are included in the photolithography design: in this thesis, $\rho_{c,n}$ is usually in the order of 30 mΩcm². For comparison, the ρ_c of both contacts of homojunction solar cells that rely on a diffused metal contact (as introduced in section 2.2.1) has been reported to be well below 1 mΩcm² [199,200].

For solar cells fabricated by the shadow-mask process, no such features are available and thus the ρ_c of the n-contact is not measured. The lateral bulk-related R_s contribution can be calculated by using equation (4.1) as proposed by [197].

$$R_{\mathrm{s,bulk,lat}} = \frac{\frac{1}{2}\cdot w_{\mathrm{p}}\left(\frac{1}{2}\cdot w_{\mathrm{p}}+\frac{1}{2}\cdot w_{\mathrm{n}}\right)}{3\cdot W}\cdot\frac{\rho_{\mathrm{bulk}}\cdot N_{\mathrm{D}}}{N_{\mathrm{D}}+\Delta n} \tag{4.1}$$

Here, w_p and w_n denote the width of emitter and BSF fingers (including the metallisation gap) respectively as given in Table 4.1, and ρ_{bulk} the specific wafer resistivity (here: usually 1–5 Ωcm). Using TrPCD measurements, a ρ_{bulk} of 3 Ωcm is regularly found, which corresponds to an N_D of 1.55×10^{15} cm^{-3}. The excess minority charge carrier concentration, Δn, at MPP depends on surface passivation and is usually in the order of 5×10^{14} cm^{-3} for the devices fabricated with the photolithography process and 6×10^{13} cm^{-3} for devices fabricated with the shadow-mask process. With the given wafer thickness of 280 µm (260 µm for double-side textured wafers), one can then calculate the lateral bulk-related R_s in dependence of w_p and w_n (with the dimensions given in section 4.1.2) to be in the range of 48–86 mΩcm² or 175–189 mΩcm² for solar cells prepared by photolithography or the shadow-mask process respectively. As the majority of excess charge carriers are generated at the front side of the devices (as far as the entire relevant solar spectrum is considered), they have to pass through the entire wafer to reach the contacts. Therefore, there is also a vertical (or horizontal) bulk-related R_s component, which is given by the simple expression $\rho_{bulk} \times W$ and amounts to 84 mΩcm² (for SSP) or 78 mΩcm² (for DST) for the given data.

Finally, to assess optical losses, EQE and reflection measurements are conducted (cf. sections 3.4.6 and 3.4.7 for further details). Since IBC devices are investigated here and, therefore, only optimisations at the rear side are conducted, particular interest is dedicated to the long-wavelength regime. Here, as discussed earlier, impacts of the changes in processing should be observable (because photons with longer wavelengths are absorbed deeper within the wafer) and can thus be ascribed to effects occurring at the rear side. A plethora of different process adjustments is examined during the course of this thesis and therefore details are given in the relevant sections 4.2.2, 4.3.4, 4.5.2, and 5.2.2.

4.2 Influence of Surface Morphology

FF-related losses are the biggest contributor to PCE limitations in IBC devices. This is partly due to the general restriction to only one wafer side for contact formation. Therefore, increasing the active contact area by means of surface texturing is theoretically a promising approach for increasing the FF. Here, the introduction of rear-side random pyramidal surface texturing into both the photolithography and the shadow-mask process, and its implications are discussed. The conducted texturing process can be found in section 3.2.1.

4.2.1 Passivating Textured Surfaces

Surface texturing of solar cells was introduced decades ago in order to increase the probability of light absorption owing to enhanced light in-coupling and multiple internal reflections due to light scattering [9,10], thus increasing the j_{sc}. Additionally, the rear-side contact area and therefore the FF are increased, which is especially beneficial for IBC solar cells as their total contact area is limited to that side. While the implementation of surface texturing in classic Al diffusion-based homojunction devices is rather unproblematic, there are some challenges when such a structure is applied to SHJ solar cells. Firstly, the surface area is increased by a factor of 1.7 [201]. To account for this, either plasma conditions during PECVD and PVD or, usually more feasible, deposition times need to be adapted in order to deposit layers of the same thickness as on a planar substrate. Secondly, and by far the bigger issue, is that pyramidal valleys are known to be prone to epitaxial a-Si:H growth [112,201]. In this case, no sharp a-Si:H(i)/c-Si interface, which is necessary for good surface passivation [111], is formed leading to local recombination centres (i.e. the pyramidal valleys) the that limit the V_{oc} [90]. Indeed, it was reported that reducing the fraction of smaller pyramids enhances the minority charge carrier lifetime measured on textured devices [113], which is probably due to a reduction in the area density of pyramidal valleys.

In a classic point of view, the pyramidal facets are treated as (111) oriented surfaces of the Si crystal that have been anisotropically and selectively etched from (100) oriented Si [170]. Therefore, PECVD parameters that yield good surface passivation (i.e. high minority charge carrier lifetime) on polished (111) oriented Si have been found to be directly applicable for textured substrates [113]. However, treating pyramidal facets as (111) oriented Si is only an approximation and, depending on what wet-chemical process (and duration) was applied to

the random pyramidal texture, and due to potentially not fully anisotropic etching, atomic steps can occur within the pyramidal facets that alter their angle and introduce possible nucleation sites for epitaxial growth [202]. Furthermore, applying a HPT to (111) surface has been reported to be less effective than on (100) surfaces [203]. Lastly, the deposition of µc-Si:H or (like in this thesis) nc-Si:H (distinguishable by their grain size) onto textured substrates can lead to cracks in the crystalline layer that hamper the lateral current transport [204].

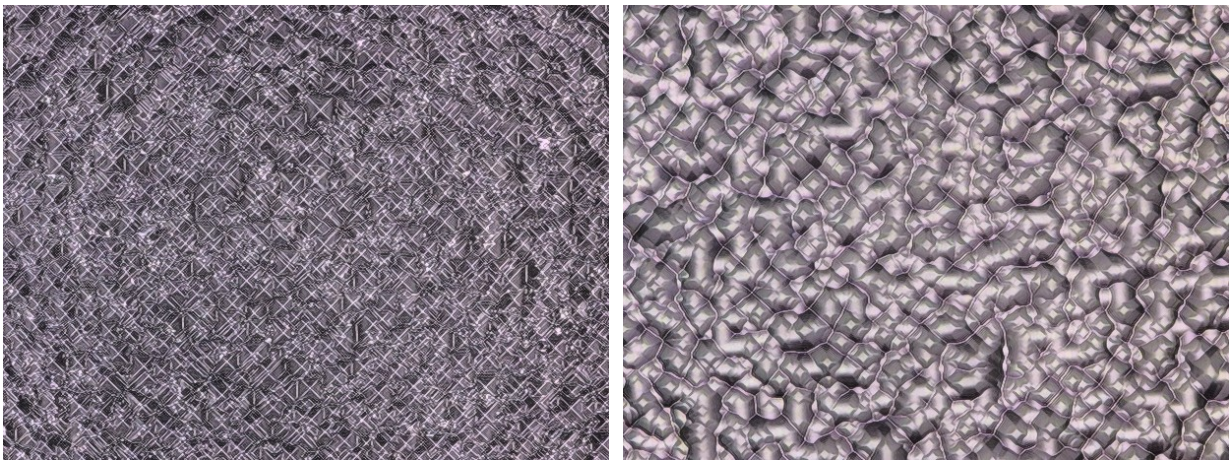
4.2.2 Textured Surfaces in the Photolithography Process

For the sake of clarity, it is to be mentioned again that when writing about textured or polished surfaces in this thesis, only the rear side is referred to for the front side of the here discussed devices is always textured.

The photolithography process relies on light microscopy for aligning masks and already patterned layers. Applying this procedure to a surface morphology that is designed to drastically reduce reflection (and scatter incident light) is very cumbersome and increases, therefore, the complexity of the photolithography process even further. Moreover, solar cell results that are about to be presented lag behind in FFs as compared to that presented in later sections. However, when these investigations were conducted, results on textured substrates with respect to FFs (and R_ss) marked a significant in-house improvement over their polished counterparts of that time. Therefore, the following sections focus on relative FF improvements (as compared to devices fabricated on wafers with polished rear side) and the general implications of introducing textured surfaces, instead of highlighting absolute FF values.

As it turns out, the biggest issue when using textured substrates in the photolithography process, apart from the concerns mentioned above, is the repassivation step after the minority charge carrier contact stack has been wet-chemically patterned. The used ‘Poly-Si-etchant’ (cf. Table 3.2) is a very aggressive acidic solution that isotropically etches both a-Si and c-Si (regardless of the doping type). The pyramidal facets of textured substrates are likewise affected, even though they might withstand other etching solutions. Figure 4.10 shows the impact of prolonged ‘Poly-Si-etchant’ treatment of a bare c-Si wafer with random pyramidal texture. The untreated surface (Figure 4.10a) exhibits intact

pyramids with a distribution of smaller and larger pyramids (1–2 µm height; cf. section 3.2.1). In Figure 4.10b, smaller pyramids have been etched off and for larger pyramids the tip is missing as they have been rounded. In fact, 'Poly-Si-etchant' can be used to polish, thin, or even completely dissolve c-Si wafers. Upon repassivation (i.e. after structuring the minority charge carrier contact stack), the real surface morphology might therefore differ from the expected one for which the plasma processes have been optimised, and this circumstance, in turn, can cause epitaxial a-Si:H growth. A well-controlled and appropriately timed emitter patterning step is thus vital for successfully fabricating IBC SHJ solar cells on DST wafers. Another issue that might occur when using this kind of wafers is that chemical residuals might accumulate in pyramidal valleys [112], which thus makes careful wafer cleaning a crucial part of the manufacturing process.



a) **b)**

Figure 4.10: Confocal microscopy images of a bare crystalline silicon wafer with random pyramidal texture: a) untreated, b) after prolonged treatment in 'Poly-Si-etchant'. In confocal microscopy, a laser scans the surface of a substrate to compute and generate an image.

In Figure 4.11, PL (a–c) and TrPCD (d) measurements both before emitter patterning (a) and after repassivation (b and c) are shown for two different samples: one where the repassivation step was successful (b) and one where this was not the case (c). Note that having a textured surface is likely not the problem itself here because (i) the initial passivation (regardless of surface morphology) is (in this thesis) always successful in terms of minority charge carrier lifetimes and high iFFs in the same range as for solar cells fabricated on SSP wafers; (ii) lifetime samples (cf. section 4.3.2) comprising 4" c-Si(n) FZ (i.e. device relevant) DST wafers quartered by a laser have been prepared testing different passivation layer stacks with different polarities, which resulted in consistently high τ_{eff}s; and (iii) DST

wafers are successfully used in the shadow-mask process (where no wet-chemical treatment with 'Poly-Si-etchant' is conducted) without encountering the issues described here (cf. next section).

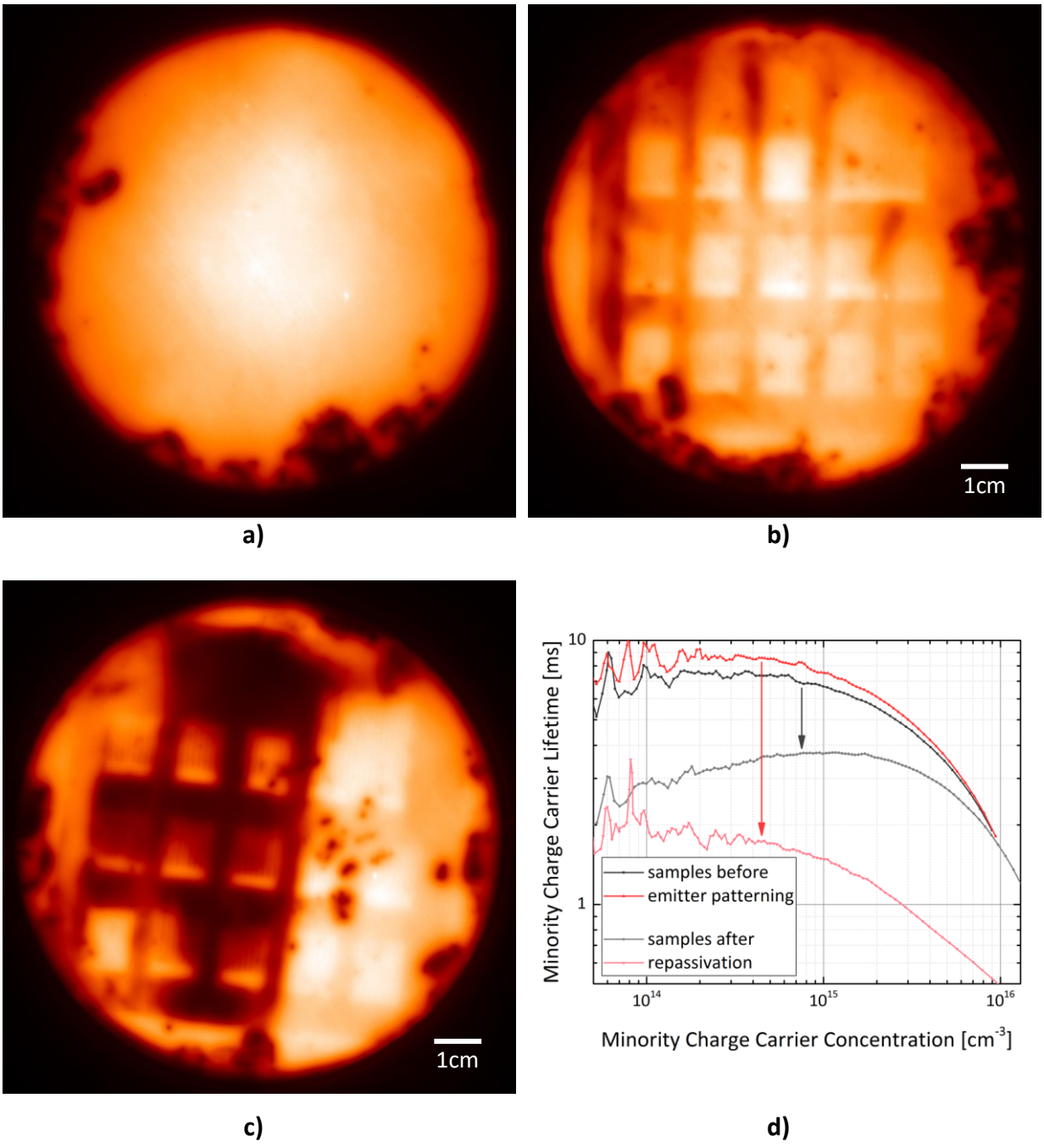


Figure 4.11: Non-calibrated photoluminescence images (a–c) of rear-side textured wafers during different stages of the photolithography process: after a) initial passivation, b) mostly successful, and c) unsuccessful repassivation (left wafer portion); d) development of minority charge carrier lifetime over minority charge carrier concentration of the samples presented in b) (black) and c) (red).

In Figure 4.12a, different solar cells prepared on both SSP and DST wafers are compared by means of a FF loss analysis as proposed in section 4.1.3. SSP solar cells follow the expected trend of a small difference in iFF−pFF, indicating an intact passivation, and a pronounced decrease from pFF to FF, therefore identifying a high R_s (of up to 1.8 Ωcm² as indicated in the Figure; determined by the dark *j*–*V* method) as the main reason for the observed losses. On the contrary, solar cells on DST wafers feature a major reduction from iFF to pFF, therefore indicating additional recombination losses upon contact formation, probably due to an improper repassivation process and potentially a partially epitaxial growth of the passivation layer. The impact of the latter is then further exacerbated during an annealing step (as also reported by [91,114]) that is necessary for the crystallisation of the contact stack's ITO. This is also reflected in low V_{oc}s of 699 and 695 mV of the DST samples presented in Figure 4.12a (for comparison: solar cells fabricated here on SSP wafers feature V_{oc}s of > 710 mV). Apart from that, their pFF and FF are very similar, resulting in comparatively low R_ss down to approximately 0.5 Ωcm², only roughly a fourth of the R_s in their SSP counterparts (1.6–1.8 Ωcm²). The n-contact's ρ_c, gained from TLM measurements, is found to be equal for both surface morphologies (about 60 mΩcm²).

Due to using the same wafer material but with different thicknesses (260 µm and 280 µm for DST and SSP wafers respectively), the lateral bulk-related R_s is with 52–86 mΩcm² (depending on the finger dimensions and the minority charge carrier contact coverage; cf. Table 4.1) marginally higher for solar cells prepared on DST wafers (SSP: 48–79 mΩcm²). The total R_s of the different substrate types (DST and SSP) differs quite drastically (cf. Figure 4.12a), but all R_s contributors except the ρ_c of the p-contact are roughly the same. Therefore, especially the minority charge carrier contact benefits from the increased contact area, yielding a substantially lower ρ_c of that contact. This is in good agreement with [193] where, in a comparable scenario, the minority charge carrier contact responds more sensitively to a reduced metallised area. Furthermore, the absolute FF values are 2–3%$_{abs}$ higher for DST solar cells and their long-wavelength response is slightly enhanced as determined by EQE measurements (cf. Figure 4.12b). Provided that the repassivation issue can be solved, which can partly be realised by adapting the etching duration of the emitter patterning step (cf. section 4.4.2), surface texturing thus provides a suitable route for improving FFs of IBC SHJ solar cells.

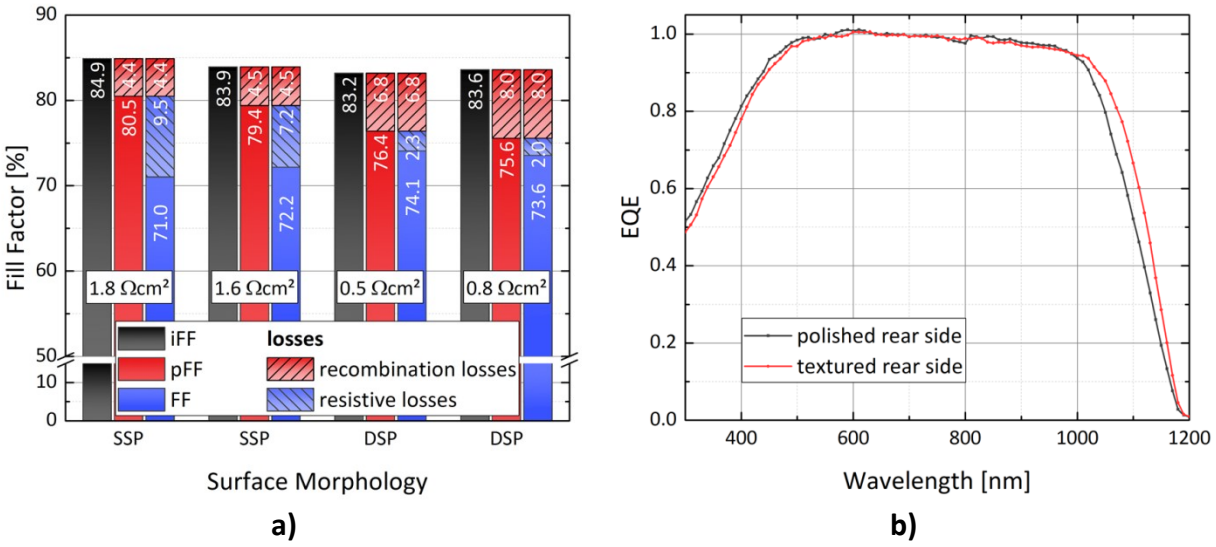


Figure 4.12: a) Fill factor losses of two solar cells each, prepared on wafers with polished and textured rear sides. Series resistance values (extracted by the dark j–V method) are significantly lower for the latter. Note the break in the ordinate that is introduced to make the loss portions more noticeable; b) external quantum efficiency measurements reveal a clear advantage in the long-wavelength regime of having a textured rear side over a polished one.

4.2.3 Textured Surfaces in the Shadow-Mask Process

First results utilising the shadow-mask process as described in sections 3.3.2 and 4.1.2 have been published in [37,50]. Best devices yielded a PCE of 17.0% on SSP wafers mainly limited by a low FF (due to a high R_s) and, despite a high overall τ_{eff} of 4.0 ms, a low V_{oc}. The latter is caused by an insufficient emitter passivation. This issue will be approached by the introduction of a modified passivation scheme where multiple a-Si:H(i) layers with different C_H are used (cf. section 4.4). For the former issue, however, the same considerations and conclusions as for the photolithography process hold true, namely that an increased contact area is beneficial for the FF, in particular for the minority charge carrier contact. As mentioned earlier, the deposition conditions, especially for the PECVD processes of the doped Si layers, must be adjusted to meet the requirements for double-side textured substrates. The thus optimised process route today yields maximum PCEs of 20.5% and 20.0% for 1 × 1 cm² and 2 × 2 cm² (in each case: designated illumination area) solar cells respectively. Figure 4.13 shows the *j*–*V* characteristics of the so far best solar cells fabricated by the shadow mask process including both rear-side textured and polished substrate types. Their key solar cell parameters are summarised in Table 4.2.

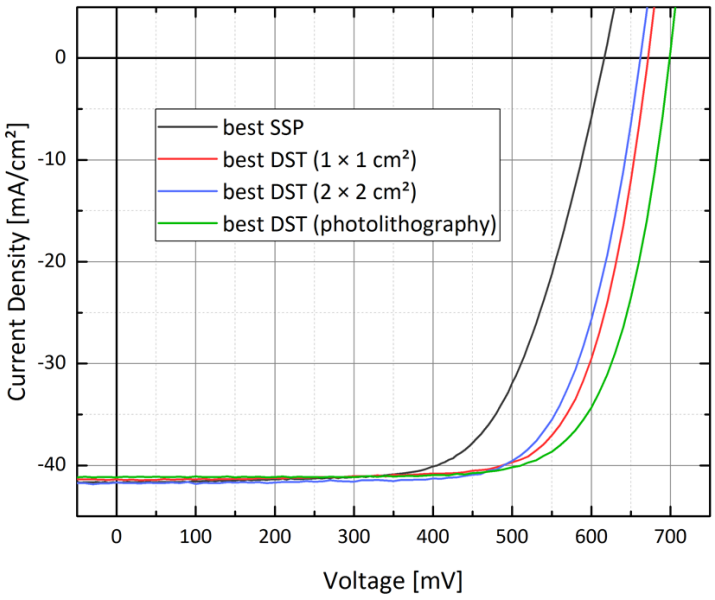


Figure 4.13: Illuminated one-sun current–voltage characteristics of the so far best IBC SHJ solar cells fabricated on single-side polished (SSP, black) and double-side textured (DST, red and blue) wafers in the shadow-mask process. For comparison, the best solar cell from section 4.2.2, fabricated on a fully textured wafer in the photolithography process is also depicted (green).

Table 4.2: Solar cell parameters for in-house record devices fabricated by the shadow-mask process on different substrates: rear-side polished and double-side textured wafers. Partly already presented in [37,50,194].

Substrate type	*Cell size [cm²]*	V_{oc} *[mV]*	j_{sc} *[mA/cm²]*	*iFF [%]*	*pFF [%]*	*FF [%]*	*PCE [%]*	$R_s^{\dagger}$ *[Ωcm²]*
SSP	1 × 1	616	41.7	84.4	81.1	66.3	17.0	2.6
DST	1 × 1	672	41.1	84.5	79.1	73.7	20.5	1.0
DST	2 × 2	662	41.7	84.6	76.9	72.4	20.0	0.8
DST[‡]	1 × 1	699	41.2	83.2	76.4	74.1	21.3	0.5

† determined by the SunsVoc method

‡ reference sample fabricated with the photolithography process (cf. section 4.2.2)

Two things become obvious from the presented data using DST wafers: (i) the FF of solar cells fabricated by the shadow-mask process is closer to their photolithography counterparts as compared to former results where SSP wafers have been used; the still apparent difference of usually 3–4%$_{abs}$ can be largely ascribed to a broader metallisation gap of the former (100 µm vs 30 µm); (ii) the other main limiting factor is an approximately 40–50 mV lower V_{oc}. As can be seen from Figure 4.14a as well as the discrepancy of iFF and pFF in Table 4.2, this decrease stems from additional recombination losses in the poorly passivated

emitter regions, which is even more pronounced for the $2 \times 2\ cm^2$ solar cell. Solar cells processed on SSP wafers apparently follow the 'regular' trend of unproblematic contact formation but FF limitations governed by high R_s. This is, however, not the full picture since it does not explain why the V_{oc} would lack behind photolithography-processed solar cells by roughly 100 mV. From Figure 4.14b it becomes evident that a non-uniform passivation is also present in SSP solar cells but less severe than in DST devices. The growth of a-Si:H(p) deposited by PECVD on a large area differs considerably from that deposited through a mask [34,205]. This consequently leads to altered layer characteristics, which might render the a-Si:H(p) layer incapable of sufficiently screening the a-Si:H(i)/c-Si interface from WF mismatch as proposed by [49,126] (cf. also section 2.1.6 for further details). Therefore, the observed passivation degradation seems to stem at least partly also form the ITO sputtering process. This is, however, an inherent problem of the shadow-mask process at this point that cannot be solved by modifying the surface morphology but rather needs adjusting especially the plasma conditions during PECVD, which will be conducted and discussed in section 4.4.3 where an adapted multilayer passivation stack is introduced.

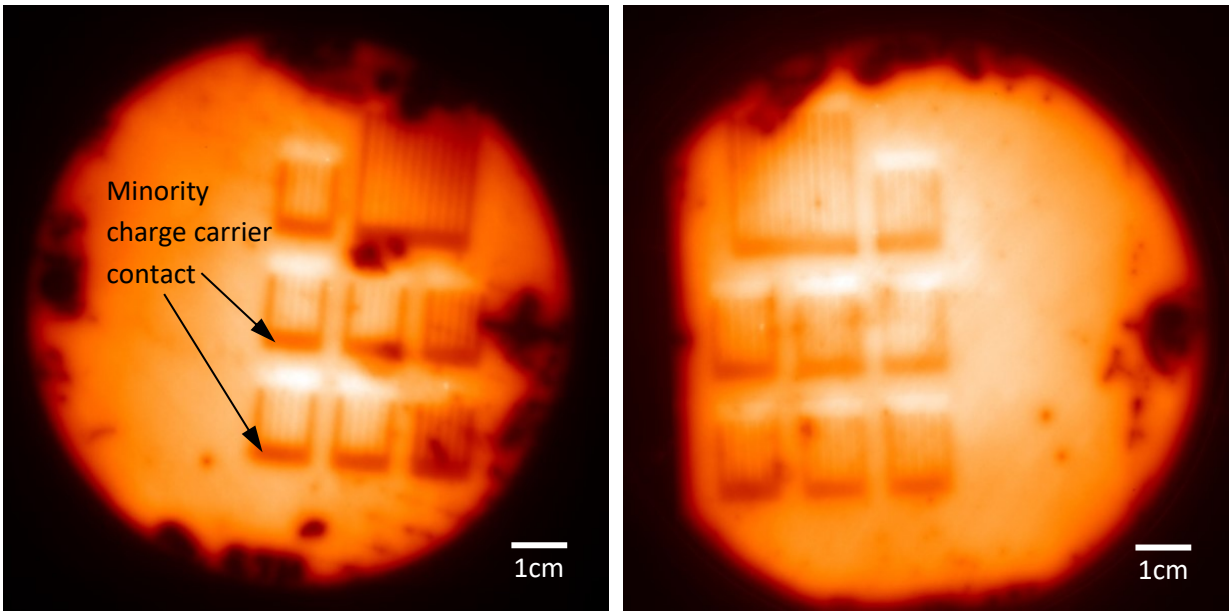


Figure 4.14: Non-calibrated photoluminescence images of samples prepared on wafers with a) textured and b) polished rear side in the shadow-mask process. In both cases, the minority charge carrier contact regions appear darker than the rest of the wafer due to inferior passivation in those areas, which limits the overall V_{oc} of final devices.

4.3 Influence of Passivation Layer Thickness

Surface passivation has enabled SHJ solar cells to reach V_{oc}s as high as 750 mV [21], which is unparalleled within the c-Si-based single-junction solar cell technology [16]. Carefully tuning the a-Si:H(i) layer thickness is, however, crucial because too thick passivation layers can hamper the extraction of minority charge carriers and thus lead to low FFs or even induce so-called s-shaped *j*–*V* characteristics [144,152]. The aim of the following section is therefore to determine the optimal a-Si:H(i) layer thickness, with respect to both high V_{oc}s and FFs, for the devices investigated here. These variations are carried out only for the photolithography process because reducing the a-Si:H(i) layer thickness on devices that already suffer from poor passivation (i.e. solar cells fabricated with the shadow-mask process) due to problems discussed in the last section would not be constructive or could lead to erroneous conclusions.

4.3.1 The Occurrence of S-shaped Current–Voltage Characteristics

In SHJ solar cells, so-called s-shaped *j*–*V* characteristics can occur due to an improper a-Si:H(i)/a-Si:H(p) interface design [206,207]. This is caused either by insufficient emitter doping [140,144,208] that leads to the introduction of an energetic barrier for minority charge carriers at the a-Si:H(p)/TCO interface (cf. section 2.1.7) or by a too thick passivation layer [152,207] also introducing a barrier. These two barriers differ insofar as they impede different transport mechanisms: recombination at the a-Si:H(p)/TCO interface or tunnelling through a-Si:H(i). Fundamentally, the illuminated *j*–*V* characteristics of all SHJ solar cells feature an s-shape (or sometimes called roll-over) at a certain forward bias voltage: it occurs when the VB edges of a-Si:H and c-Si align under illumination [140,144]. For solar cells with highly doped emitter, however, this happens at voltages far beyond the V_{oc} and thus does not affect the performance of such a device [140,144].

Electrically, an s-shape can be described by an extended equivalent circuit model featuring a Schottky diode [209] in parallel to a shunt resistor ($R_{sh,Schottky}$) as depicted in Figure 4.15a. This model was introduced in 1984 by LATHROP *et al.* [210] and later used to describe different high-efficiency solar cell architectures, such as PERC (passivated emitter and rear cell), PERL (passivated emitter, rear locally diffused), LFC (laser-fired contact) and SHJ [140,148,211]. The Schottky diode is parametrised by a high saturation current density (j_s) and a high

n of ≥ 2 [140,210]. Its shunt resistance determines whether this rectifying Schottky or the ohmic contact represented by the basic equivalent circuit model predominates. For high $R_{sh,Schottky}$, the overall solar cell behaviour is governed by the Schottky diode and current extraction is impeded for higher voltages [208], depending on the Schottky diode's saturation current density [210]. For low $R_{sh,Schottky}$, the Schottky diode is effectively shunted and therefore no longer influences current extraction. It has been shown that, in electrical equivalent circuit simulations, the influence of the Schottky diode vanishes once the value of $R_{sh,Schottky}$ is in the same order as the p-contact's ρ_c [211]. Figure 4.15b shows j–V characteristics of a c-Si solar cell modelled with LTspice (cf. section 3.5) both with and without the influence of a rectifying Schottky contact (i.e. with and without s-shape). The corresponding modelling parameters are given in Table 4.3.

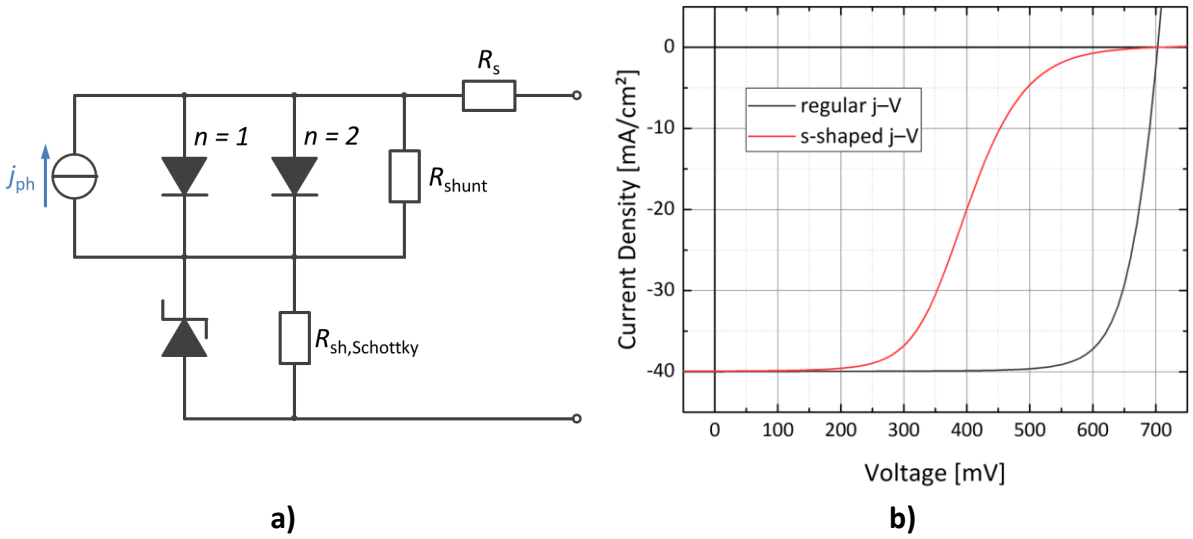


Figure 4.15: a) Electrical equivalent circuit of a solar cell extended by a Schottky diode and a shunt resistor in parallel to it. If the latter is sufficiently small, the Schottky diode is efficiently shunted and the solar cell behaves regularly (cf. b), black curve). Otherwise, the impact of the Schottky diode impedes proper current extraction from the device and its current–voltage characteristics are s-shaped (cf. b), red curve); b) regular (black) and s-shaped (red) current–voltage characteristics of a solar cell modelled with LTspice as explained in a). The used parameters of the proposed model are given in Table 4.3.

Table 4.3: Parameters for modelling the influence of a rectifying Schottky contact (i.e. an s-shaped current–voltage characteristic) with LTspice by using an equivalent circuit model as presented in Figure 4.13a. The chosen parametrisation given here agrees well with values reported in literature [28,35,145,151,184,212,213].

j_{ph} [mA/cm²]	$j_{0,1}$ [A/cm²]	$j_{0,2}$ [A/cm²]	j_s [A/cm²]	n_1	n_2	$n_{Schottky}$	R_s [Ωcm²]	R_{shunt} [Ωcm²]	$R_{sh,Schottky}$ [Ωcm²]
40	5×10^{-14}	1×10^{-8}	1×10^{-4}	1	2	2	0.45	4500	0 or 1000[†]

[†] 0 Ωcm² represents ohmic behaviour, 1000 Ωcm² the s-shape case

4.3.2 Preparation of Lifetime Samples

Since the fabrication of IBC SHJ solar cells is very time-consuming (approximately three weeks for a batch of eight wafers in the photolithography process), lifetime samples are prepared, allowing for relatively fast optimisation without having to process entire solar cells. Here, only the layers of interest (usually the PECVD layer) are deposited and characterised. Note that it is not possible to determine the FF of these lifetime sample. However, the cause for low FFs in devices investigated here is assumed to be a too thick a-Si:H(i) passivation layer. Reducing this thickness while maintaining sufficiently high minority charge carrier lifetimes is therefore proposed to increase the FF once this optimised passivation layer stack has been implemented into actual devices. In the following, the general fabrication procedure of lifetime samples is briefly described.

4" c-Si(n) FZ are prepared by means of surface texturing (cf. section 3.2.1) to obtain either SSP or DST substrates. These are then quartered using a laser (cf. section 3.2.3) and subsequently RCA cleaned (cf. section 3.2.2). The thus prepared and cleaned quarters are dipped in a diluted HF solution (1% in DI) to remove SiO_x that was formed during the RCA cleaning procedure and immediately loaded into an AKT1600 PECVD cluster tool (cf. section 3.1.1) to run a series of experiments usually involving a thickness variation of a-Si:H(i) and/or either or both of the doped layers. Lifetime samples are afterwards characterised by means of TrPCD and PL measurements. They are also used for evaluating the ρ_c of different contact stacks in TLM measurements, which necessitates a slightly altered preparation procedure. In order to allow Al to diffuse into doped a-Si:H layers without damaging the passivation underneath, their thickness is slightly increased. Contact formation is then achieved by sputtering ITO (omitted for an Al contact) and thermal evaporation of Ag or Al.

The metallisation stack is then patterned by means of photolithography. Further details are given in section 4.5.1.

4.3.3 Surface Passivation and Minority Charge Carrier Lifetimes

For investigating the minimum required rear-side passivation layer thickness, lifetime samples are prepared where the doped layers are kept at a constant thickness while that of the a-Si:H(i) layer is systematically reduced. The layer thickness cannot be set directly and has thus to be accounted for by adjusting the deposition time (t_{depo}). Here, a t_{depo} of 22 s and 28 s (representing the standard t_{depo} for SSP and DST substrates respectively) yield 7.15 nm and 9.10 nm respectively on a polished wafer surface as confirmed by spectral ellipsometry. The resulting deposition rate is thus approximately 0.3 nm/s. The optimal a-Si:H(i) layer thickness for both high V_{oc} and FF was reported to be approximately 4 nm [51,53], giving thus rise to the assumption that the passivation layers used so far in this thesis are indeed too thick, which, in turn, would plausibly explain the experimentally found low FFs of only slightly above 70%. A thickness variation is carried out on both SSP and DST substrates and for each passivation step: initial (a-Si:H(i)/a-Si:H(p)) and repassivation (a-Si:H(i)/nc-Si:H(n)). For the latter, the standard emitter stack (t_{depo} = 22 s or 28 s) is deposited and structured by photolithography. The lifetime samples are then RCA cleaned, HF dipped, and repassivated. The front side is the same as that of actual solar cells (i.e. a-Si:H(i)/SiN_x/a-Si:H(i)). Two or more quarters are used per variation. Table 4.4 gives a comprehensive overview over the conducted experimental series.

TrPCD and PL measurements are carried out for each sample to examine the passivation quality in terms of minority charge carrier lifetimes and spatial homogeneity respectively. The resulting lifetimes are shown as a function of relative thickness reduction (with regard to the reference t_{depo}) in Figure 4.16a (for SSP) and b (for DST). From Figure 4.16a it becomes evident that reducing t_{depo} and thus the thickness of the a-Si:H(i) layer in the experimental range explored here (i.e. approximately 30–40%) still yields sufficiently high minority charge carrier lifetimes of > 3 ms and thus ensures a proper surface passivation. Furthermore, PL images reveal a uniform passivation quality as can be seen in Figure 4.17a–c (the three samples are marked with a), b), and c) in Figure 4.16a correspondingly). Dark spots at the edges (especially visible in Figure 4.17b) are due to manual sample handling with tweezers.

Table 4.4: Overview over the experimentally conducted deposition time variation and resulting thicknesses of the a-Si:H(i) layer. The passivation layer thickness is varied for the minority charge carrier contact stack (t_{depo} emitter) and the majority charge carrier contact stack (t_{depo} BSF). Reference deposition times are marked in red (emitter) or blue (BSF).

Substrate type	t_{depo} *emitter [s]*	*Passivation thickness*[†] *[nm]*	*Fraction of reference thickness [%]*	t_{depo} *BSF [s]*	*Passivation thickness*[†] *[nm]*	*Fraction of reference thickness [%]*
SSP	22	7.15	100			
SSP	20	6.50	90.91			
SSP	18	5.85	81.82		No variation conducted	
SSP	16	5.20	72.73			
SSP	14	4.55	63.64			
SSP				20[‡]	6.50	100
SSP	22	7.15	100	18	5.85	90
SSP				16	5.20	80
SSP				14	4.55	70
DST	28	9.10	100			
DST	26	8.45	92.86			
DST	24	7.80	85.71		No variation conducted	
DST	22	7.15	78.57			
DST	20	6.50	71.43			
DST				28	9.10	100
DST				26	8.45	92.86
DST	28	9.10	100	24	7.80	85.71
DST				22	7.15	78.57
DST				20	6.50	71.43

[†] The given thickness relates to the deposition onto a polished substrate.
[‡] Note that the standard t_{depo} of the initial and repassivation step are different.

Concerning lifetime samples prepared on DST (cf. Figure 4.16b), unfortunately only data stemming from the initial passivation variation is evaluable as will be explained in the following. Here, again, there is evidently no clear trend but rather consistently high minority charge carrier lifetimes of approximately 3 ms and a spatial homogeneous passivation, confirmed by PL measurements. After BSF deposition, the lifetime samples feature τ_{eff}s of merely 1 ms or even well below that value owing to an improper repassivation (cf. Figure 4.17d). This stems from effects discussed in section 4.2.2 (regarding partially epitaxial

growth of a passivation layer on textured surfaces) that conceals any actual impact of a passivation layer thickness reduction and thus the latter cannot be evaluated from the gained data.

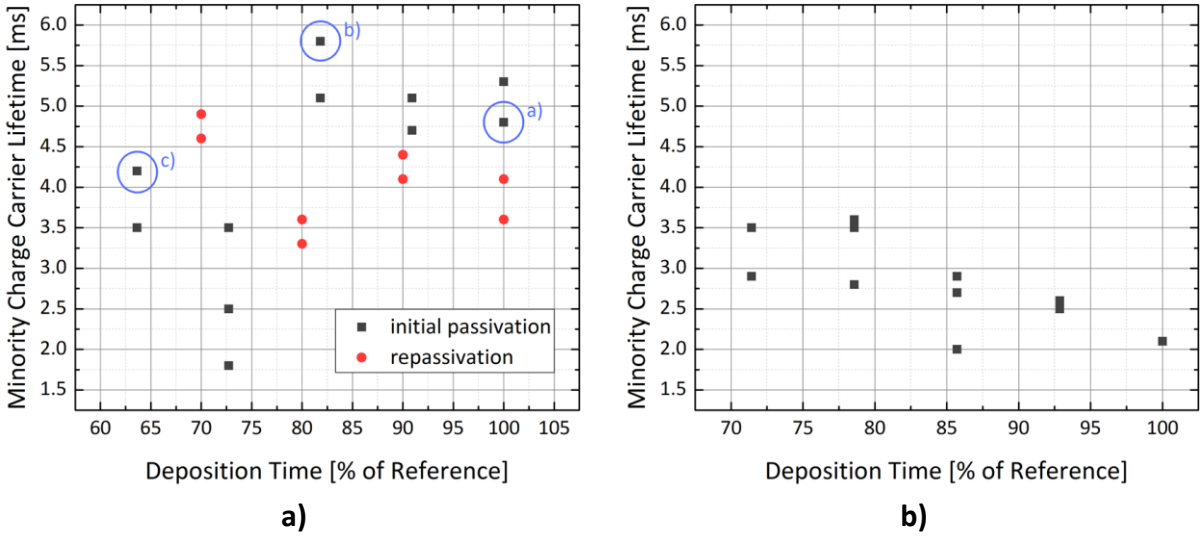


Figure 4.16: Minority charge carrier lifetimes at a minority charge carrier concentration of 10^{15} cm^{-3} of samples prepared on wafers with a) polished and b) textured rear side for a variety of thicknesses (represented here as a fraction of the reference process's deposition time as indicated in Table 4.4). For textured samples, unfortunately only results of the initial passivation's thickness reduction can be evaluated for the data gained after repassivation are inconclusive due to as yet insufficiently solved issues with wet-chemical processes on fully textured substrates as pointed out in the text. For samples marked in Figure a) with a), b), and c), the corresponding PL images are presented in Figure 4.5 a–c).

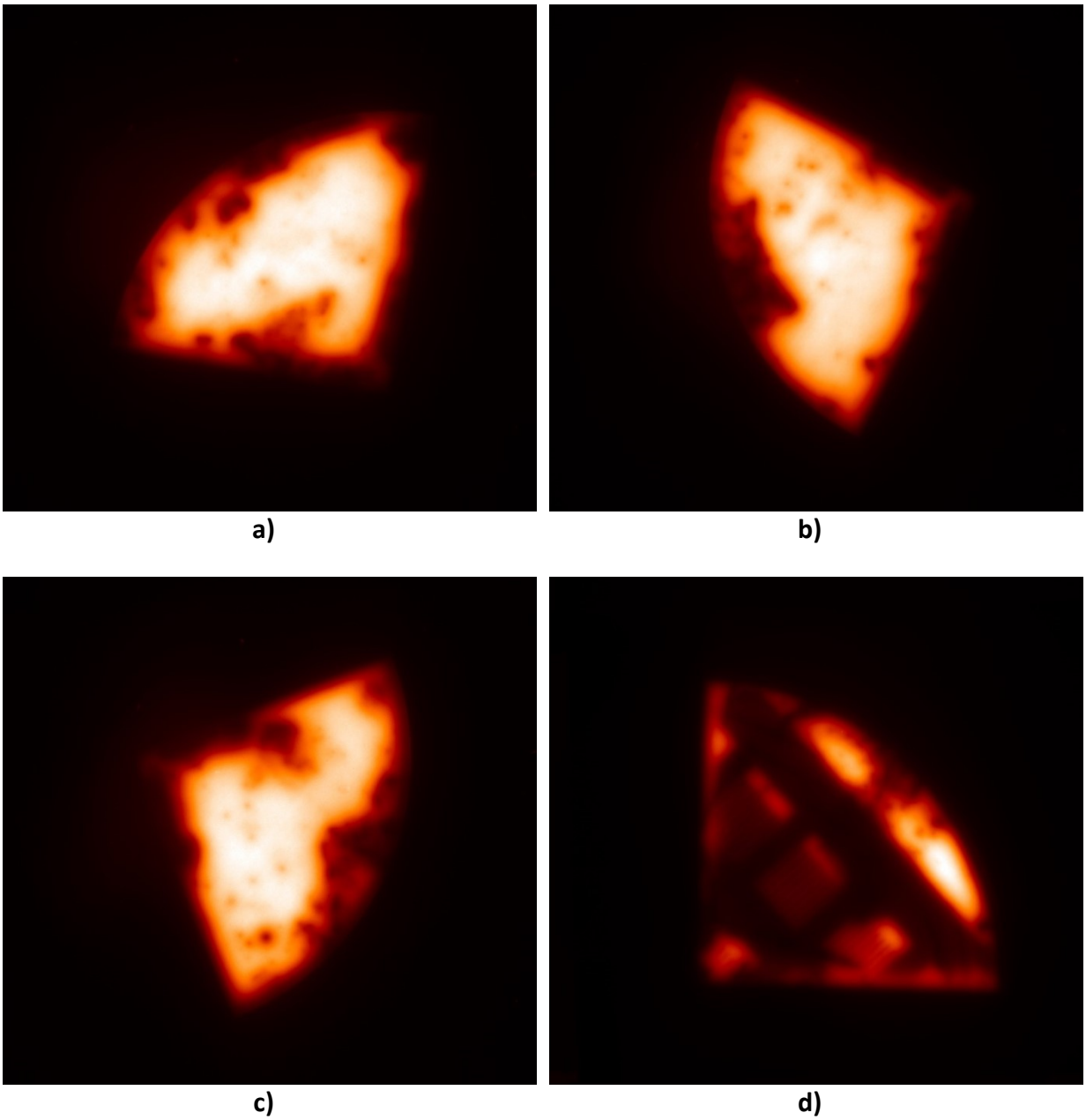


Figure 4.17: Non-calibrated photoluminescence images of lifetime samples prepared on quartered wafers with a)–c) polished (corresponding to the marked data in Figure 4.14a) and d) textured rear side. The latter shows exemplarily the outcome of a faulty repassivation process commonly found on rear-side textured samples.

4.3.4 IBC SHJ Solar Cells with Optimised Passivation Layer Thickness

In order to verify whether such thin a-Si:H(i) layers are suitable for actual devices, IBC SHJ solar cells are fabricated where t_{depo}s of 14 s and 16 s (i.e. the thinnest and second thinnest passivation examined in the previous section) are used for both contacts, representing a thickness of slightly below or above 5 nm respectively. A total of four wafers including twelve solar cells with 1 × 1 cm² and one with 2 × 2 cm² cell area (da) each are fabricated per

t_{depo} and their solar cell parameters (i.e. j_{sc}, V_{oc}, FF, and PCE) are statistically evaluated. The results are presented in Figure 4.18a–d.

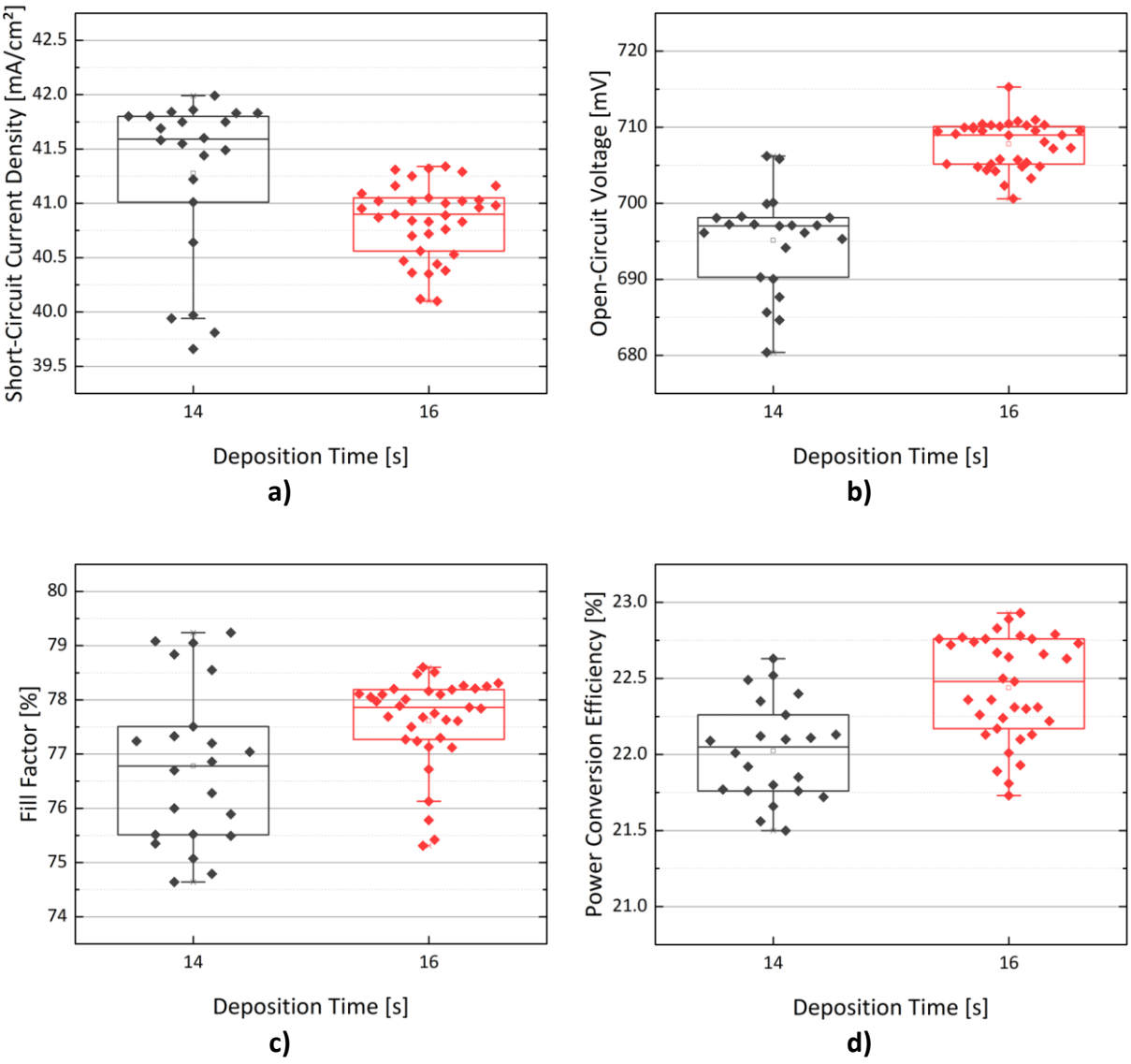


Figure 4.18: Solar cell parameters of devices fabricated with the two thinnest passivation layer thicknesses (represented here with their respective passivation layer deposition time; cf. Table 4.4 for more details): a) short-circuit current density, b) open-circuit voltage, c) fill factor, and d) power conversion efficiency.

Except for the j_{sc}, all characteristic solar cell parameters are superior for a t_{depo} of 16 s, i.e. an a-Si:H(i) layer thickness of about 5.2 nm. These findings are in good agreement with [51,53]. One could assume that the increase in V_{oc} of more than 10 mv with a-Si:H(i) layer thickness corresponds to an increased hydrogen concentration in that layer. Even though this is true for very thin layers, it has been shown that the hydrogen concentration saturates already at thicknesses above 3 nm [51,110]. Therefore, it is proposed that the increased thickness causes a better screening of the a-Si:H(i)/c-Si(n) interface from the highly doped emitter as also

reported by [108,214]. A very slight decrease in j_{sc} of about half a mA/cm² is observed for the thicker passivation. This is very likely not due to parasitic absorption of long-wavelength photons in the rear-side a-Si:H(i) as its band gap of approximately 1.7 eV [85] results in a cutoff wavelength of about 730 nm. Owing to the fact that the used wafer features a thickness of roughly 300 µm, the majority of these photons are probably already absorbed before they reach the rear side [12], which is also confirmed by EQE measurements (cf. Figure 4.20b). Within the EQE data it is further found that the cause for the lower j_{sc} (Figure 4.18a) seems to be a reduced response in the short-wavelength regime below 500 nm due to an unintentional variation in the front-side layer stack. The EQE-integrated j_{sc} values are, however, similar for both deposition times, so the discrepancy in j_{sc} is as of yet not fully understood.

Following the same consideration, the increase in FF with passivation layer thickness seems at first counterintuitive. When introducing an increased energetic barrier, one would expect the FF to decline as it has been demonstrated beforehand [35,52]. Examining Figure 4.18c and only considering the respective best cells for both t_{depo}s reveals indeed higher FFs for thinner passivation layers. It is therefore proposed that the FFs of these solar cells are partly already limited by poorer V_{oc}s as higher values allow for higher FFs for a comparable R_s (for further details cf. section 4.1.3). The R_s of the three cells with the highest FF amounts to 0.48–0.55 Ωcm² (derived from the SunsVoc method). Additionally, these solar cells feature with 1.7–1.9 mA/cm² below the median the lowest j_{sc}s, which translates into a reduced electric power loss that is approximately cut in half. For comparison, the R_s of solar cells with median values of j_{sc} and FF feature an R_s of 0.9–1.1 Ωcm². Following the empirically found linear correlation between FF and R_s in section 4.1.3 (Figure 4.8b), this increased R_s yields a decrease in FF of 2–3%$_{abs}$ and is thus a reasonable explanation for these results. These findings are further substantiated by PL measurements where the emitter regions of solar cells fabricated with thinner passivation appear remarkably darker than their thicker passivation counterparts (cf. Figure 4.19). This also explains well V_{oc}s below 700 mV and the wide FF spread in Figure 4.18b and c respectively. The FF dependence of the passivation layer thickness by means of the here gained experimental data has to be interpreted considering this caveat.

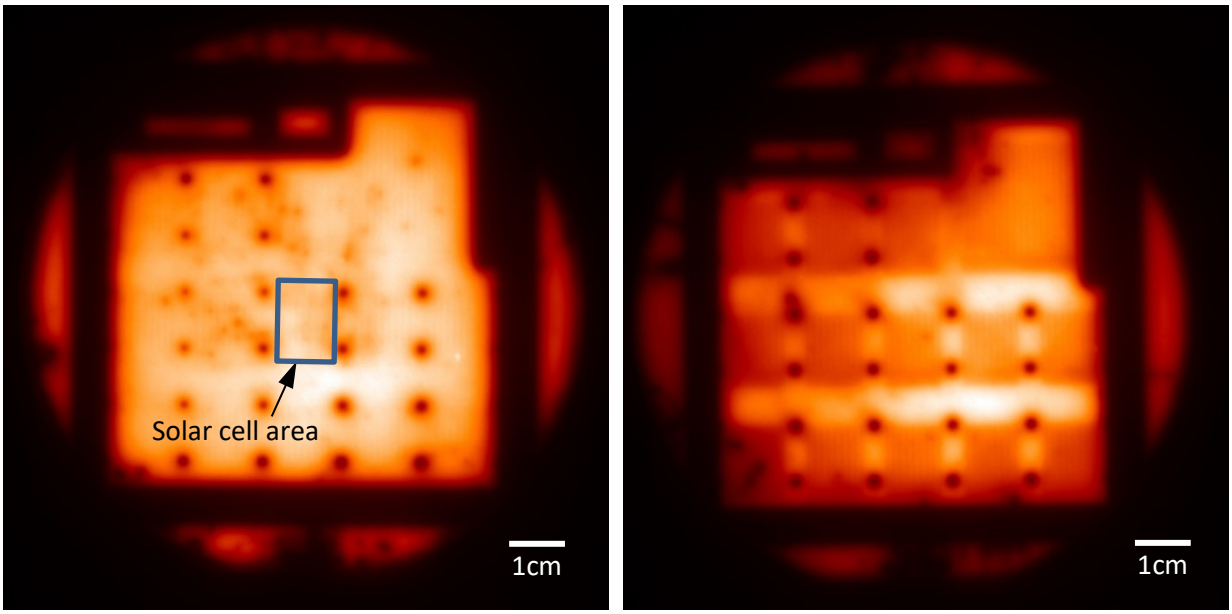


Figure 4.19: Non-calibrated photoluminescence images of two wafers with a) sufficiently thick passivation layer (representing samples with a deposition time of 16 s in Figure 4.18) and b) too thin passivation layer (14 s in Figure 4.18): the minority charge carrier contact regions appear remarkably darker than in a).

The best thus optimised IBC SHJ solar cells feature PCEs of 22.6% (t_{depo} of 14 s) and 22.9% (t_{depo} of 16 s) and respective FFs of 77.5% and 78.2%. Their *j*–*V* characteristics are depicted in Figure 4.20 and their solar cell parameters are summarised in Table 4.5. Owing to the remarkably low R_s of 0.6 Ωcm² (of the best cell; derived from the SunsVoc method), an enormous increase in FF as compared to former results (cf. also Table 4.5) is achieved. TLM measurements reveal a ρ_c of 33 mΩcm² for the n-contact; with knowledge of the contact geometry (cf. Table 4.1), the lateral bulk-related R_s can be calculated to 60 mΩcm² and, therefore, the largest improvement is, again, achieved for the p-contacts ρ_c with a numeric value of now roughly 423 mΩcm². In accordance with literature for standard [51,53] and IBC SHJ solar cells [152], it is therefore concluded that, in order to reach high FFs (and thereby high PCEs) in IBC SHJ solar cells, the passivation layer at the rear side needs to be as thin as possible while still providing a sufficient passivation quality (i.e. high V_{oc}s). Too thick passivation layers act as a barrier for minority charge carriers and thus impede current extraction from the device resulting in low FFs and (to a lesser extent) j_{sc}s.

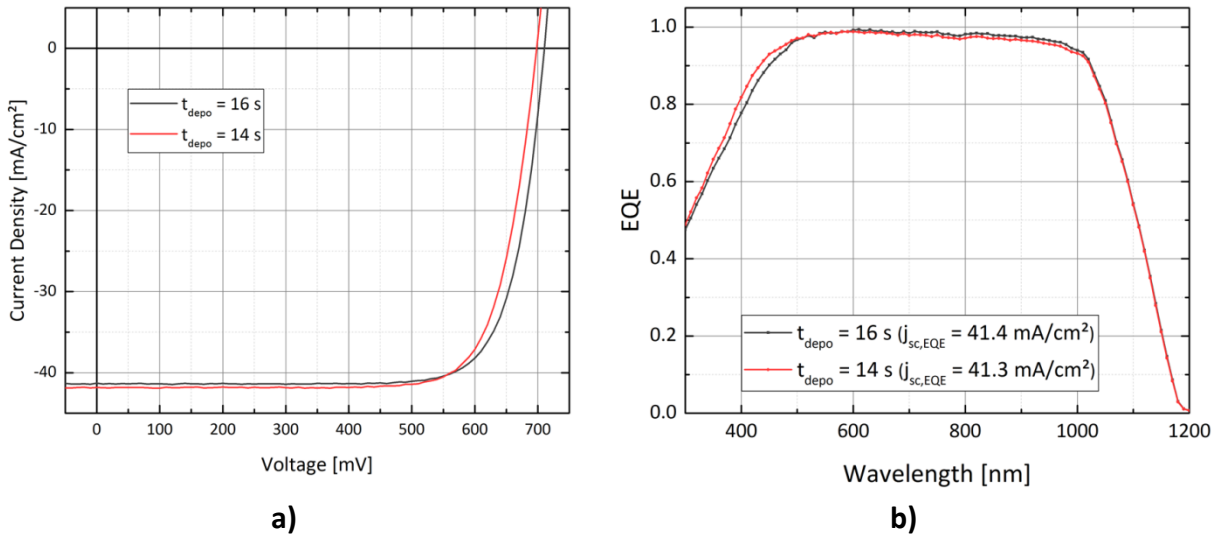


Figure 4.20: Illuminated one-sun current–voltage characteristics of the best IBC SHJ solar cells fabricated in the photolithography process and featuring an optimised passivation layer thickness; b) external quantum efficiency measurements of two samples representative for a deposition time of 16 s (black) and 14 s (red).

Table 4.5: Summary of relevant device parameters of the best IBC SHJ solar cells featuring an optimised passivation layer thickness presented in this section. A sample fabricated with reference deposition times is also shown for comparison.

t_{depo} [s]	*Thickness* [nm]	V_{oc} [mV]	j_{sc} [mA/cm²]	*FF* [%]	*PCE* [%]	R_s† [Ωcm²]
14	4.55	698	41.8	77.5	22.6	0.9
16	5.20	710	41.3	78.2	22.9	0.6
22/20‡	7.15	711	41.9	70.0	20.8	2.3

† derived from SunsVoc measurements

‡ reference process with t_{depo}s of 22 s and 20 s for initial passivation and repassivation respectively

4.4 Influence of a Multilayer Passivation Stack

As compared to other IBC SHJ solar cells demonstrated in literature [27–29,40,176], the V_{oc} of devices presented here is rather low and is therefore another limiting factor with regards to reaching higher PCEs. To this end, a redesigned multilayer passivation stack comprising three separate a-Si:H(i) layers with different hydrogen contents (low towards the c-Si surface, high towards the highly doped emitter) is introduced and its implications are discussed for both the photolithography and the shadow-mask process.

4.4.1 Implied V_{oc}s and Minority Charge Carrier Lifetimes

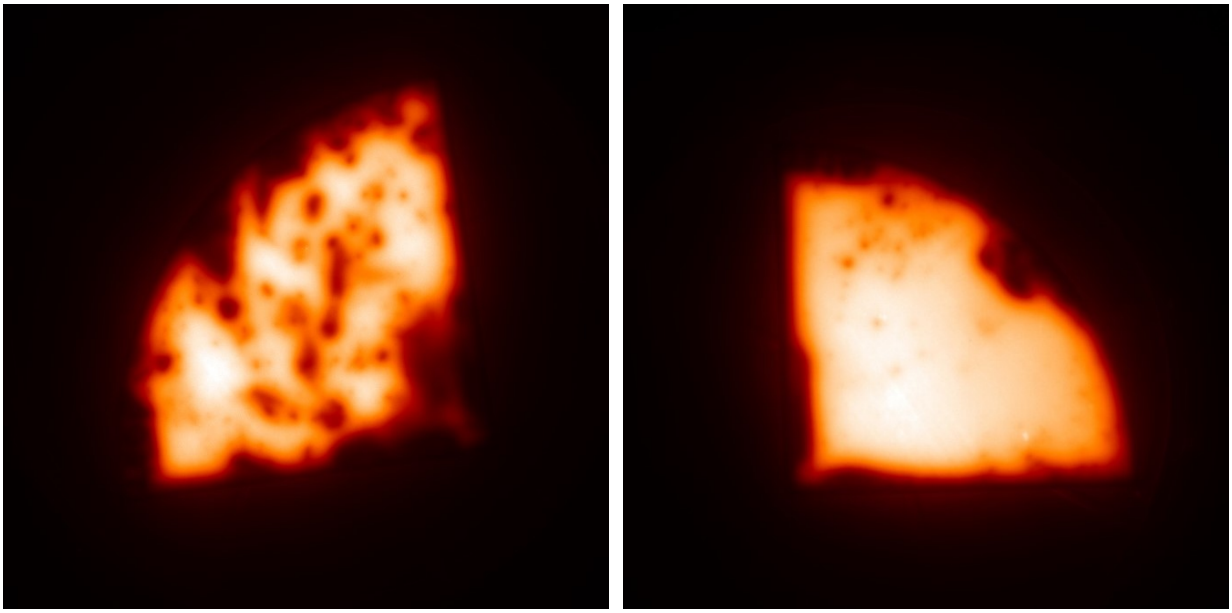
High hydrogen concentrations are necessary for sufficient chemical passivation [107] but lead to highly disordered films [85]. From a surface passivation point of view, the a-Si:H(i) layer directly at the interface with c-Si needs to be well-ordered, not featuring any voids or other morphologic errors, and therefore the hydrogen concentration must be low [114]. To investigate the general viability of this approach, lifetime samples (cf. section 4.3.2) are processed using PECVD parameters given in Table 3.1 and characterised by means of TrPCD and PL. In this approach, the rear-side passivation single layer and HPT are replaced by three separate a-Si:H(i) layers with different hydrogen contents (C_H). The first interfacial (i.e. in direct contact to c-Si) a-Si:H(i) layer features a low C_H and the following two identical a-Si:H(i) layers feature a higher C_H [166]. Note that the actual C_H of each layer is not directly measured but controlled by the silane dilution during PECVD. When applied to test structures, the multilayer stack yields an overall increase in minority charge carrier lifetimes, iV_{oc}s, and iFFs as compared to a single-layer passivation as used before (cf. Table 4.6). It yields (with regards to the three investigated parameters) a better and spatially homogeneous surface passivation, with the latter being confirmed by PL measurements.

Table 4.6: Statistically evaluated TrPCD data of different passivation and substrate types. Minority charge carrier lifetimes are given for an excess minority charge carrier density of 10^{15} cm^{-3}.

Passivation and substrate type	τ_{eff} *[ms]*	iV_{oc} *[mV]*	*iFF [%]*
Single layer SSP	3.3 ± 0.9	705.6 ± 6.2	84.6 ± 1.4
Single layer DST	2.8 ± 0.6	720.2 ± 3.2	83.8 ± 0.6
Multilayer SSP	5.0 ± 1.0	716.9 ± 2.6	86.1 ± 0.6
Multilayer DST	6.1 ± 1.3	722.1 ± 2.6	86.2 ± 0.9

However, having both high V_{oc}s and FFs at the same time is challenging, and often a trade-off between both parameters has been reported [26,52,215,216]. Therefore, a passivation layer thickness study similar to that carried out in 4.3.3 is conducted to find the optimal deposition conditions and thus thicknesses. It is found that for a spatially homogeneous passivation the interfacial hydrogen-poor a-Si:H(i) needs to feature a certain thickness, and that the hydrogen-rich capping layers increase the overall minority charge carrier lifetime (and iV_{oc}) but are on their own not capable of yielding uniform surface passivation (if the

interfacial layer is too thin). Figure 4.21 shows PL images of two exemplary lifetime samples both with an overall high τ_{eff} of about 3–4 ms, but only in one case a uniform passivation is achieved. Within the scope of this experiment, optimised t_{depo}s of 7 + 10 + 10 s (with the first summand referring to the H_2-poor interfacial and the last two summands referring to both H_2-rich a-Si:H(i) layers atop) and 12 + 12 + 12 s have been found for SSP and DST substrates respectively, resulting in 4.9 nm and 7.0 nm total a-Si:H(i) thickness on a polished reference wafer.



a) **b)**

Figure 4.21: Non-calibrated photoluminescence images of double-side textured lifetime samples (cf. section 4.3.2 for details) prepared with the multilayer passivation scheme. Both samples feature high overall minority charge carrier lifetimes but in a) spatially homogenous surface passivation is lacking, which is not the case in in b). Both samples solely differ in the thickness of the hydrogen-poor a-Si:H(i) layer that is in direct contact with the wafer: a) 1.3 nm, b) 1.7 nm.

4.4.2 Multilayer Passivation in the Photolithography Process

For the implementation of the multilayer passivation stack into devices, two batches with a total number of six SSP and four DST wafers are prepared with the photolithography process. To optimise the often problematic repassivation step, the minority charge carrier contact patterning step is adapted by shortening the etching duration as much as possible, giving thus the isotropic etchant less possibility to detrimentally alter the surface morphology as shown in section 4.2.2. This procedure, however, yields mixed results: while for some DST samples a uniform repassivation is achieved, it is not always the case. Figure 4.22 shows a series of PL images in each case after: a) the successful initial

passivation, b) the emitter patterning step to verify that the reduced etching duration still suffices, c) an unsuccessful, and d) a successful repassivation of a DST wafer.

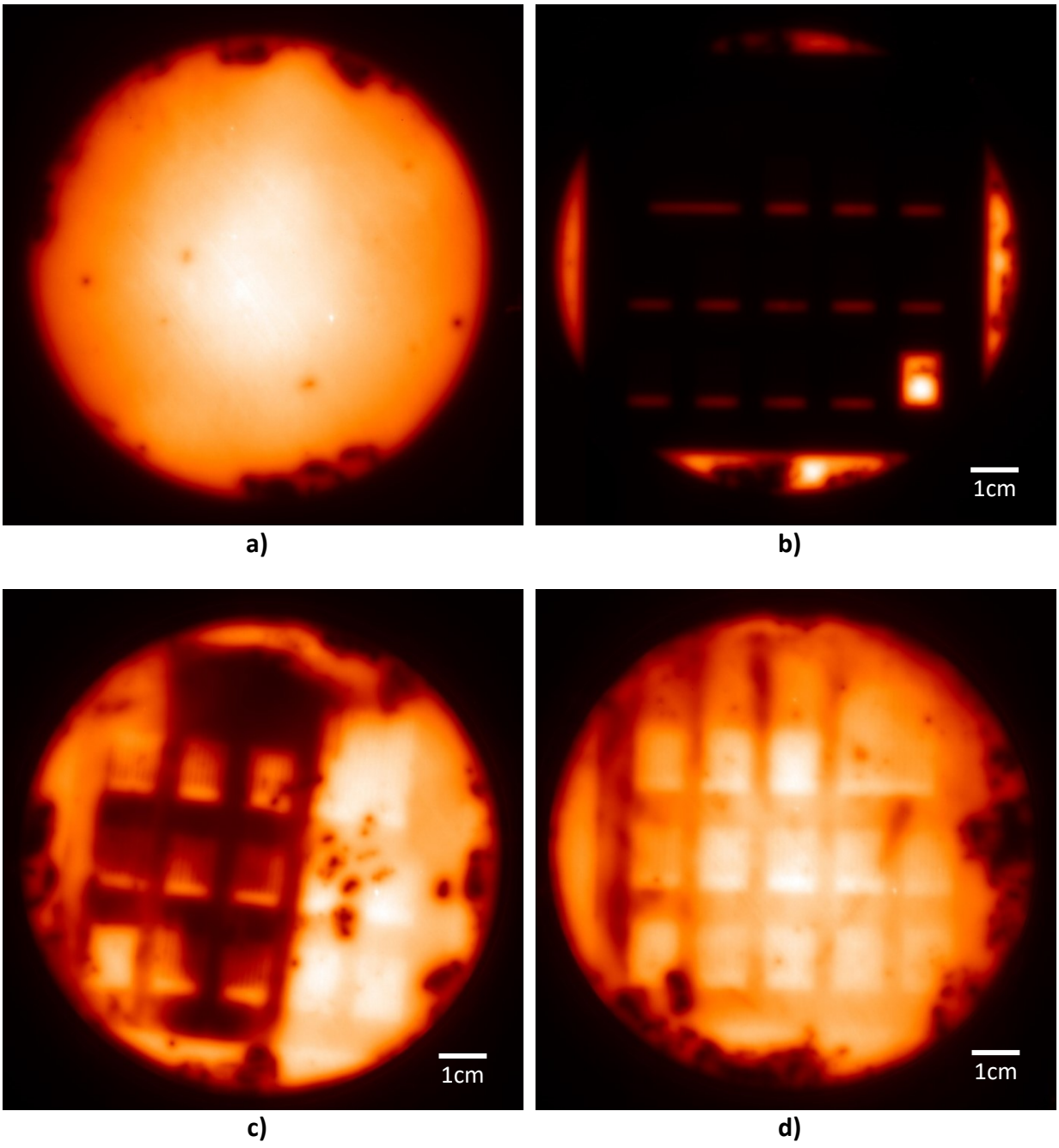


Figure 4.22: A series of non-calibrated photoluminescence images with similar brightness scale showing different stages of the photolithography process on fully textured wafers: after a) initial passivation, b) emitter patterning, c) i unsuccessful repassivation, and d) successful repassivation.

The better passivation quality of a multilayer stack indeed translates into slightly higher V_{oc}s (up to 723 mV) as compared to a single-layer passivation approach in finalised devices, but unfortunately leads to very low FFs (below 70%) and for some solar cells even to slightly s-shaped *j*–*V* characteristics. Therefore, t_{depo} is further reduced to 6 + 8 + 8 s (yielding a total

a-Si:H(i) thickness of slightly above 4.0 nm) in the second batch because a too thick intrinsic layer in between absorber and minority charge carrier contact is assumed to be the cause for the low FF.

Here, only SSP wafers are used because the results gained when using DST wafers render the evaluation of any optimisation process rather erratic or at least challenging. The repassivation process for these wafers has to be fundamentally reworked before any optimisation approach can be conducted and its results evaluated in the photolithography process. Furthermore, it cannot be fully precluded that a-Si:H(p) residuals still remain in areas where nc-Si:H(n) is to be deposited, owing to the reduced etching duration. This would lead to local n/p/n-junctions in the n-contact areas that very likely impede the current extraction of majority charge carriers since they would have to overcome these energetic barriers by tunnelling; or, alternatively, the active contact area would be decreased by this. Indeed, TLM measurements on DST samples revealed unusually high ρ_cs of up to 82 mΩcm² for the n-contact, albeit still with ohmic behaviour. It is worth noting that a multilayer passivation stack is applied only to the minority charge carrier contact portions of the solar cells while the standard passivation scheme is kept unchanged for the majority charge carrier contact regions (i.e. the single-layer passivation approach as presented in section 4.3.4). Therefore, one would expect typical ρ_cs of about 30 mΩcm² for that contact. In Figure 4.23, the statistically evaluated solar cell parameters V_{oc}, FF, and PCE of the second multilayer passivation devices batch are juxtaposed with those of the optimised single-layer case (t_{depo} = 16 s) from section 4.3.4. The j_{sc}s of both approaches are similar with the multilayer passivation scheme yielding in average 0.3 mA/cm² higher values (cf. Figure 4.23a).

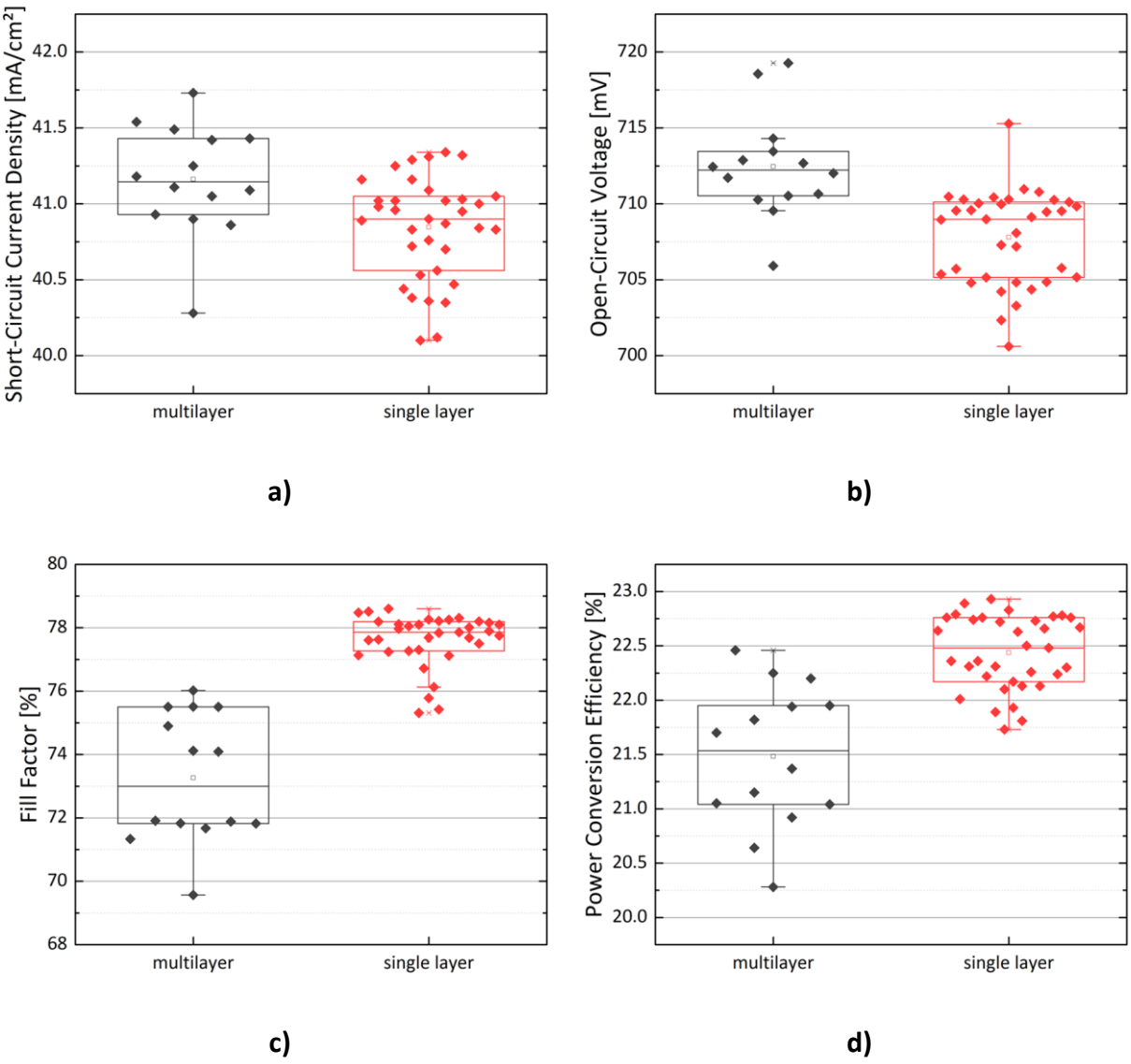


Figure 4.23: Solar cell parameters of devices fabricated with both a single (red) and a multilayer (black) passivation scheme: a) short-circuit current density, b) open-circuit voltage, c) fill factor, and d) power conversion efficiency.

Utilising a further optimised multilayer passivation approach still yields high V_{oc}s (close to 720 mV; cf. Figure 4.23a) and also FFs on a more useful level, but the latter still lack substantially behind their single-layer passivation counterparts regarding both absolute values and data spread (cf. Figure 4.23b). The results reflect the classic trade-off scenario between V_{oc} and FF (cf. above) where the gain in the former cannot compensate the loss in the latter resulting thus in a reduced PCE. It might be possible to reduce the passivation layer thickness even further to counteract the effect of an additional energetic barrier and increase the FF, but this might come at the cost of losing the advantage of a higher V_{oc}. In addition, it is to be mentioned that the assumed a-Si:H(i) layer thickness is already at the lower limit of what is reported to be necessary (about 4 nm) [51,53]. Another possible

optimisation route with respect to increasing the FF is to reduce the hydrogen content of the capping layers because an increased C_H leads to band gap widening in a-Si:H(i) [85], which can affect the FF by introducing an additional energetic barrier for minority charge carriers to the a-Si:H(i)/a-Si:H(p) interface [52]. The best solar cell featuring a multilayer passivation stack and fabricated by the photolithography process yields a V_{oc} of 713 mV, a j_{sc} of 41.5 mA/cm², a FF of 76.0%, and a PCE of 22.5%. Its R_s is determined to be 1.2 Ωcm² (by the SunsVoc method) with the bulk contributing 144 mΩcm². Unfortunately, the specific contact resistivity of the n-contact has not been measured. It is assumed, however, to be in the range of 30–50 mΩcm² as for this contact the standard single-layer passivation approach is used.

4.4.3 Multilayer Passivation in the Shadow-Mask Process

For shadow-mask processed solar cells, the PCE is mainly limited by low V_{oc}s. The causes for this are twofold: first, poorly passivated emitter regions despite TrPCD measurements indicating an overall high τ_{eff}; and second, insufficient screening of the a-Si:H(i)/c-Si interface by the a-Si:H(p) layer from ITO (cf. sections 2.1.6 and 4.2.3 for futher details). As compared to the formerly used single-layer passivation stack, a drastic increase in minority charge carrier lifetimes (4.4 ms) and iV_{oc}s (721 mV), in each case determined by TrPCD measurements, is achieved when applying a multilayer passivation stack to test structures. The resulting maximum iFF of this redesigned passivation scheme is 85.4%. Additionally, a spatially homogenous surface passivation is obtained as confirmed by PL measurements and depicted in Figure 4.24. The previously observed passivation degradation of the emitter regions is therefore remedied by adapting the passivation scheme.

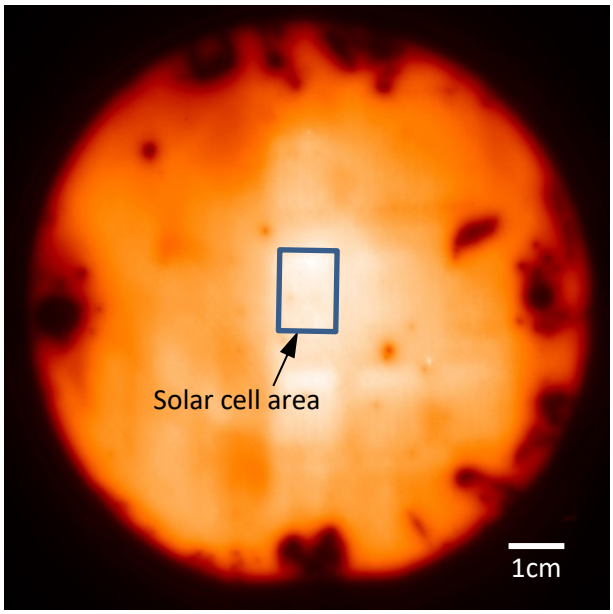


Figure 4.24: Non-calibrated photoluminescence image of a sample fabricated with the shadow-mask process and featuring a multilayer passivation scheme. The formerly observed degradation of the emitter stack is not present with this approach, leading to a spatially homogeneous surface passivation comparable to that attained with the photolithography process.

After contact formation and annealing a similarly high pFF of 85.3% (cf. discussion in section 4.1.3) is observed for the best solar cell, giving rise to the assumption that the WF mismatch induced V_{oc} degradation is also solved. This is, however, not the case as the pseudo V_{oc} (i.e. the V_{oc} determined from SunsVoc measurements) amounts to only 640 mV and thus about 80 mV are lost due to additional recombination upon contact formation, although PL images indicate an improved emitter passivation (cf. Figure 4.25).

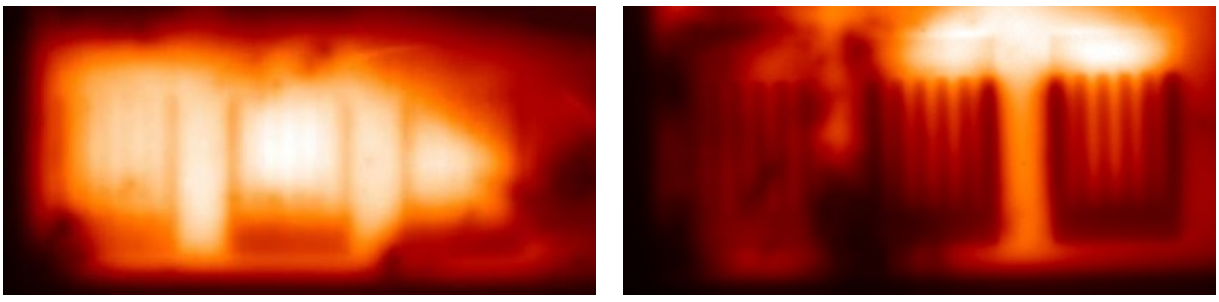


Figure 4.25: Non-calibrated photoluminescence images of finalised devices fabricated with the shadow-mask process utilising a) a multilayer and b) a single-layer passivation scheme. A degradation of the minority charge carrier contact passivation occurs in both cases (probably due to work-function mismatch as described in greater detail in the text) and limits therefore the final devices' V_{oc}s. The observed degradation is worse in b)

The resulting PCE of the best final device (16.9%) is, however, mainly limited by a low FF of only 62.7%, resulting in an R_s of 3.3 Ωcm² and 4.0 Ωcm² as determined by the dark *j*–*V* and SunsVoc method respectively. This low FF partly stems from a too thick passivation layer stack that induces an additional energetic barrier especially for minority charge carriers, similar to the first results of the photolithography process described above. Therefore, a second batch with further thinned passivation layer stack and slightly thicker emitter is processed. Again, initial results after *in-situ* patterning yield high τ_{eff}s (> 5 ms) and iV_{oc}s (725 mV) as well as uniform passivation; iFFs range from 86.7–87.2%. Contact formation, however, leads to reduced pFFs of about 78–79% (i.e. already a discrepancy of 8–9%) and, more importantly, a pseudo V_{oc} of only 631 mV. Therefore, the resulting actual FFs and V_{oc}s are limited to 71.2% and 621 mV respectively for the best solar cell. As a result of the thinner passivation layer in the second batch, a trade-off between V_{oc} and FF occurs with a slightly higher impact of the FF gain, therefore yielding an increased PCE of 18.2%. Additionally a quite substantial R_s reduction by two thirds is achieved (1.4 Ωcm² according to the SunsVoc method). Parameters of the as of yet best solar cells fabricated with a multilayer passivation stack in the shadow-mask process are presented in Table 4 7 along with their *j*–*V* characteristics in Figure 4.26. Further optimisation for making the surface passivation more robust against WF mismatch (which has been already discussed as the cause for the degradation of the minority charge carrier contact passivation in sections 2.1.6 and 4.2.3 as well as in literature [49,54,126,130]) by adapting the doping concentration of a-Si:H(p) at the interface towards ITO would be necessary to solve the issue regarding the passivation degradation of the emitter regions. Unfortunately, this was not achieved during the course of this thesis due to a limitation in time but will be focussed on in future experiments.

Table 4 7: Solar cell parameters of the so far best IBC SHJ solar cells fabricated with a multilayer passivation approach in the shadow-mask process.

Batch	V_{oc} *[mV]*	j_{sc} *[mA/cm²]*	*FF [%]*	*PCE [%]*	$R_s^{\dagger}$ *[Ωcm²]*
1	647	41.7	62.7	16.9	4.0
2	622	41.1	71.2	18.2	1.4

† determined by the SunsVoc method

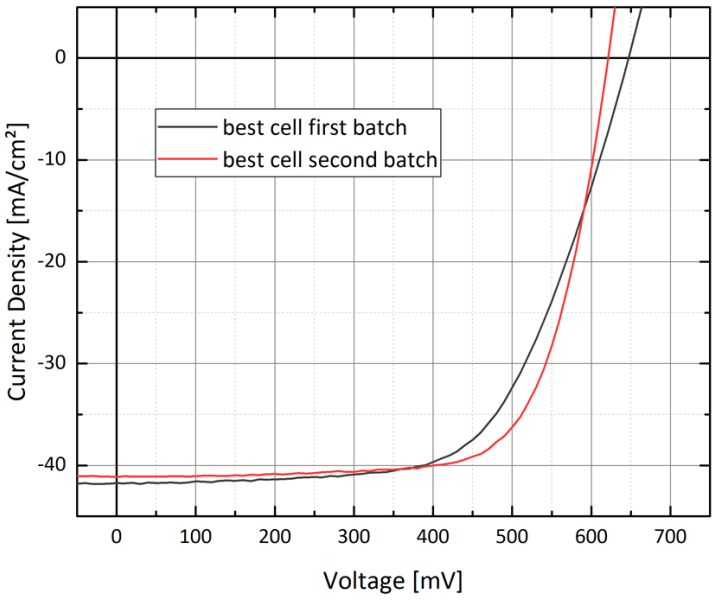


Figure 4.26: Illuminated one-sun current–voltage characteristics of the so far best IBC SHJ solar cells fabricated with a multilayer passivation approach in the shadow-mask process. A trade-off between open-circuit voltage (V_{oc}) and fill factor (FF) with respect to the total passivation layer thickness is observable. In the first batch (black) higher V_{oc}s are achieved due to a thicker passivation layer, but therefore sacrificing FF because of an increased energetic barrier for minority charge carriers. The opposite is true for the second batch (red) where a thinner passivation layer stack is used.

4.5 Influence of a Diffused Aluminium Emitter Contact

As already discussed earlier, forming a lowly resistive and ohmic contact with a-Si:H(p) is challenging when using classic n-type contact materials, such as ITO. As a member of the third period of the periodic table of elements, Al, just like boron, is a p-dopant and, being a highly conductive metal as well, is thus suitable for forming a lowly resistive ohmic contact with a-Si:H(p) [135,136]. For this, high doping concentrations in a-Si:H(p) are necessary [48,54,119]. Contact formation is then achieved by interdiffusion of Al into a-Si:H by means of annealing at moderate temperatures [217], forming aluminium silicide [218]. In fact, ρ_cs as low as 1 mΩcm² for highly doped thick a-Si:H layers [135,136,217], and 100 mΩcm² for highly doped ($N_D \geq 3\times10^{19}$ cm^{-3}) diffused p-contacts passivated with 5–10 nm a-Si:H(i) [199], in each case derived from TLM measurements, have been reported. On the other hand, Al is not an ideal choice for the n-contact since it leads to counterdoping upon interdiffusion [136]. Therefore, a contact scheme where the standard ITO/Ag stack is replaced by a direct Al metallisation on the p-contact only as depicted in Figure 4.27 is proposed in the following. The aim here is to provide either polarity with an appropriate contact scheme and, ultimately, achieve a high

FF. Since the implementation of a diffused Al emitter contact into the shadow-mask process has not been successful over the cause of this thesis, only results regarding the photolithography process are discussed in the following.

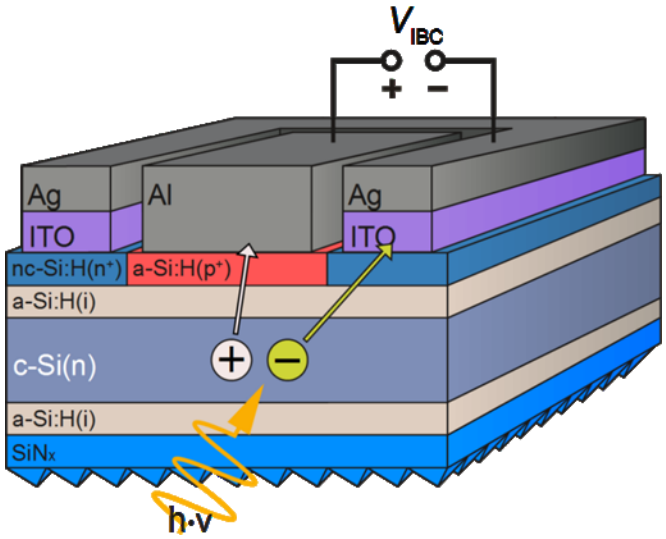


Figure 4.27: Schematic of an IBC SHJ solar cell (not to scale) with its rear side facing up and featuring a diffused aluminium emitter contact. The BSF consists of the regular ITO/Ag contact stack.

4.5.1 Specific Contact Resistivity of Different Metallisation Schemes

The results in this chapter built upon the works of STANG *et al.* regarding IBC SHJ solar cells with an all-Al metallisation scheme [50,59,60]. These devices have been reported to feature either high FF but low V_{oc} or vice versa, but achieving high values for both parameters remains challenging due to the highly recombinative nature of a diffused a-Si:H(p)/Al contact. For a shadow-mask based processes comparable to that presented in this thesis, similar results regarding the trade-off between FF and V_{oc} for Al metallised IBC SHJ solar cells have been reported [34]. Apart from resistance and recombination losses, optical considerations have to be taken into account. The omission of a rear-side TCO is possible in a rear-emitter SHJ solar cell [54], such as the devices discussed here. This, however, leads to increased plasmonic absorption within the rear-side metal sheet, which is otherwise suppressed by a TCO [125]. On the contrary, introducing a rear-side TCO leads to free-carrier absorption of long-wavelength photons [16]. Both effects impact the j_{sc} and their respective contribution to current losses needs to be weighed out accordingly.

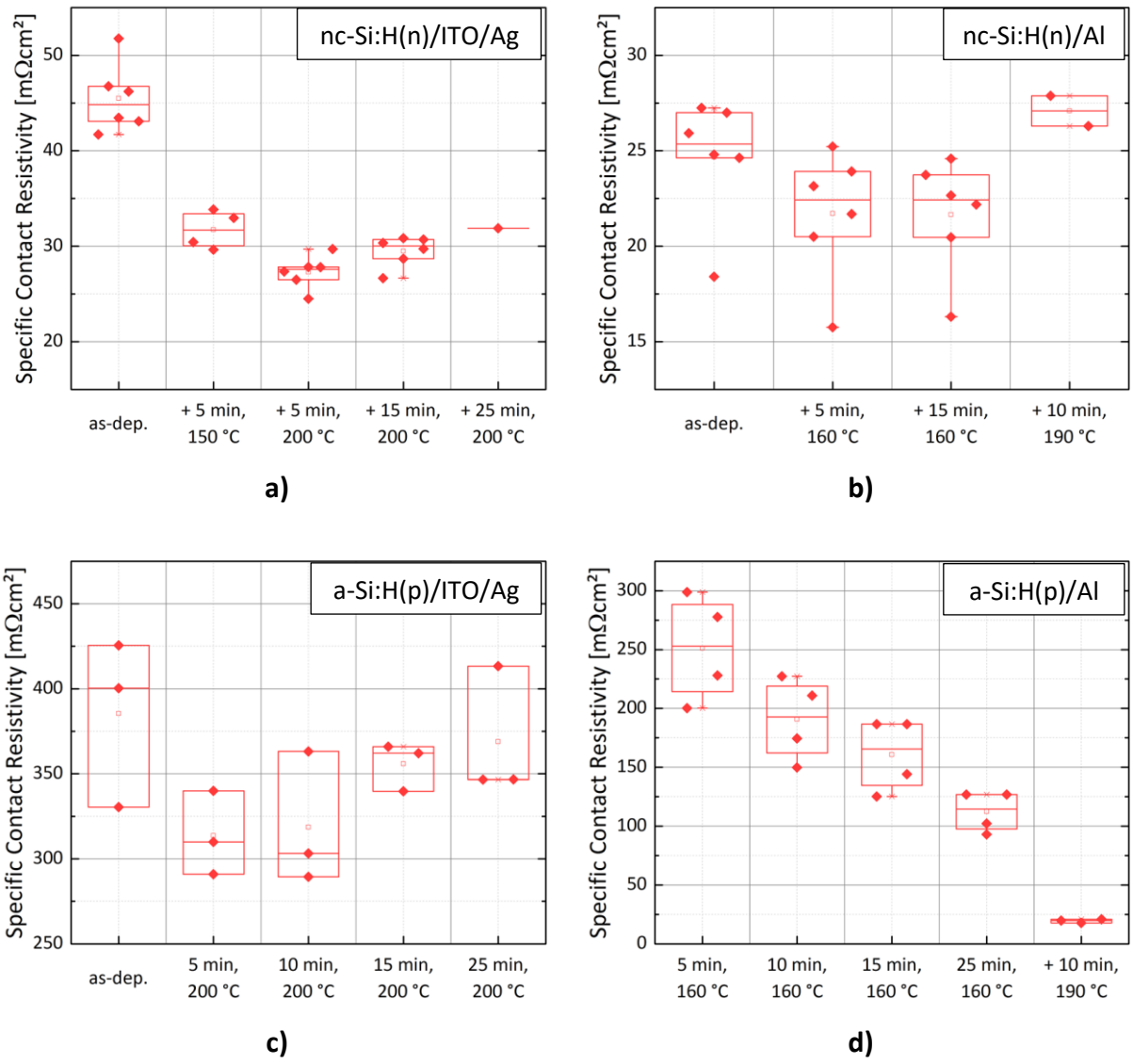


Figure 4.28: Development of the specific contact resistivity of a) ITO/Ag on nc-Si:H(n), b) Al on nc-Si:H(n), c) ITO/Ag on a-Si:H(p), and d) Al on a-Si:H(p) upon temperature treatment. Note that, for the sake of clarity, in d) the as-deposited data is not shown because the obtained values are very high. Note the different ordinate scaling.

In order to gain quantitative values of the ρ_cs of both polarities (n and p), a comprehensive TLM study is conducted. To this end, lifetime samples are prepared according to section 4.3.2 with slight alterations. Care must be taken not to destroy the passivation layer as Al diffuses into a-Si:H upon annealing. To account for this, doped layers that are used to investigate Al contacts are slightly thicker as compared to the ITO/Ag to allow Al to diffuse into the doped a-Si:H layer without damaging the passivation. Contact formation is conducted by sputter deposition (ITO; omitted for Al contacts), thermal evaporation (Ag or Al), and photolithographic patterning of the metallisation stack as discussed in sections 3.1.2, 3.1.3, 3.3.1, and 4.1.1. For this study, both p and n-type FZ c-Si substrates

with a specific wafer resistivity (ρ_{bulk}) of 1–5 Ωcm are used. TLM measurements are carried out, first, before any thermal treatment is applied to the samples (as-deposited) and subsequently after every annealing step at 160–190 °C (Al) or 200 °C (ITO/Ag) in small increments of 5–10 min each. The resulting thermal ρ_c development of different contact schemes and doping types is depicted in Figure 4.28a–d.

After 5 min of annealing the standard ITO/Ag n-contact, a drop in ρ_c is clearly visible and after another 5 min its minimum value of 25–30 mΩcm² is attained, cutting thus the initial value nearly in half (Figure 4.28a). This is most probably due to crystallisation of the room-temperature sputtered ITO, which consequently leads to an enhanced conductivity [196]. The obtained minimum is also in line with previous findings throughout this thesis. Further annealing leads again to a slight increase in ρ_c, which is in accordance with recent literature but unfortunately not understood yet [219].

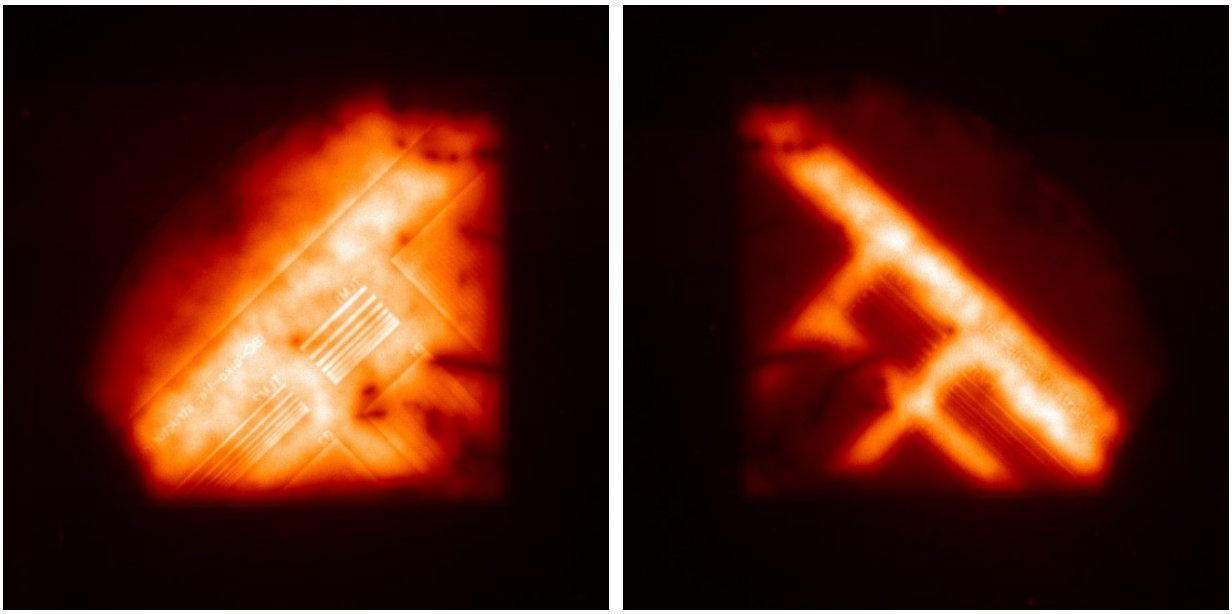
Regarding an alternative Al based n-contact stack, a fairly low ρ_c is achieved already after deposition and improves only marginally upon annealing (Figure 4.28b), which is explained as follows. Aluminium silicide has been reported to form already in as-deposited films on a-Si:H [220]. Temperatures of slightly above 100 °C, which the substrates experience during deposition of Al, are already sufficient to cause a marginal decrease in ρ_c due to crystallisation of an interdiffused aluminium silicide layer. Furthermore, nc-Si:H is used in this thesis to form the n-contact. Its superior conductivity as compared to a-Si:H also results in a lower ρ_c [97,98]. Extended annealing at higher temperatures (190 °C) increases the ρ_c, and is interpreted as the onset of counterdoping [136].

As already discussed in section 3.4.5, the ρ_c extracted by TLM heavily depends on the substrate's doping and in order to obtain absolute values, the doping concentration must be chosen with regards to the excess minority charge carrier density (Δn) at MPP [40]. For instance, assuming a Δn of 5×10^{14} cm^{-3} (as determined by TrPCD measured) and following the procedure presented in [221,222] results in a resistivity of 26.8 Ωcm for a boron-doped c-Si wafer. Unfortunately, there were no wafers with this exact resistivity at hand. Additionally, the necessary specific wafer resistivity is very sensitive to minor changes of the doping concentration. That is why, p-type wafers with a ρ_{bulk} of 1–5 Ωcm (as their n-type counterparts) are chosen, and a comparative study (instead of obtaining absolute values) is

conducted, investigating the relative differences in ρ_c of different p-contact stacks as well as their development upon temperature treatment.

In Figure 4.28c, the standard ITO/Ag p-contact shows a similar behaviour to its nc-Si:H(n) counterpart. The initial improvement is, again, most likely due to the crystallisation of ITO. An increase in ρ_c for prolonged annealing can be ascribed to hydrogen effusion from a-Si:H(i) [123] (cf section 2.1.5). The resulting poor surface passivation is linked to a reduced FF [19,53] This mechanism further explains reasonably well why V_{oc} and FF (and therefore also the PCE) of finalised devices first increase with temperature treatment, but start to decrease after prolonged annealing as described in section 4.1.3 in more detail.

The as-deposited Al p-contact's ρ_c is about twice as high (> 800 mΩcm²) as its ITO/Ag counterpart. It is therefore proposed here that non-diffused Al forms a rectifying Schottky contact with a-Si:H(p) [220]. This is not shown in Figure 4.28d because it would make the results of annealed samples difficult to observe. Furthermore, aluminium silicide is either not formed already during Al deposition on a-Si:H(p) (the reported formation according to [220] were found for intrinsic layers), or the as-deposited contact resistivity is much higher due to the amorphous phase (and therefore considerably lower conductivity than nc-Si:H(n)) of the used material. However, annealing leads to a drastic decrease in ρ_c as Al starts to diffuse into a-Si:H(p) [199]. This is further in good agreement with STANG *et al.* [60] where careful annealing of Al contacted doped a-Si:H layers has led to an increased FF due to a decrease in ρ_c. This has been linked to the interaction of Al and a-Si:H (partially crystallised aluminium silicide layer). There, the Current transport mechanism is described as a combination of tunnelling and Al spiking through a-Si:H layers. Although a minimum ρ_c of only one tenth of what is achieved with an ITO/Ag metallisation is obtained, this comes at the cost of a damaged passivation (determined by PL measurements; cf. Figure 4.29) as Al completely penetrates the a-Si:H(i) layer, which would lead to low V_{oc}s if integrated in final devices. However, samples with both annealed contact and intact passivation still yield a ρ_c that is two to threefold lower than that of the standard contact. These promising findings incentivise the implementation of such a carefully diffused a-Si:H(p)/Al contact into IBC SHJ solar cells.



a) b)

Figure 4.29: Non-calibrated photoluminescence images of TLM lifetime samples comprising a diffused aluminium minority charge carrier contact stack: a) carefully annealing at moderate temperatures (15 min at 160 °C in Figure 4.28d) leads to low specific contact resistivities and an intact surface passivation; b) elevated temperatures and/or long annealing durations lead to aluminium completely penetrating the a-Si:H(i) layer, thereby damaging the surface passivation (25 min at 160 °C + 10 min at 190 °C in Figure 4.28d).

4.5.2 Diffused Aluminium Emitter Contacts in the Photolithography Process

Several alterations to the photolithography process described in sections 3.3.1 and 4.1.1 are necessary in order to apply different contact schemes to minority and majority charge carrier contact. A flow chart of the adapted process is depicted in Figure 4.30. Apart from the doped layer's mandatory thickness adaption mentioned in the previous section, the metallisation patterning step in particular must be redesigned. ITO and Ag are now deposited directly after repassivation without structuring the BSF stack (i.e. the majoriry charge carrier contact) beforehand. The entire a-Si:H(i)/nc-Si:H(n)/ITO/Ag stack is subsequently patterned using first the metallisation photolithography mask (and adequate etchants) to structure the metallisation, and second the BSF mask (and etchants) to remove all layers from the emitter portions and overlap area between a-Si:H(p) and nc-Si:H(n); the photoresist is left on the BSF regions for a later on conducted lift-off procedure. Figure 4.31 shows an exemplary photograph of an accordingly patterned wafer.

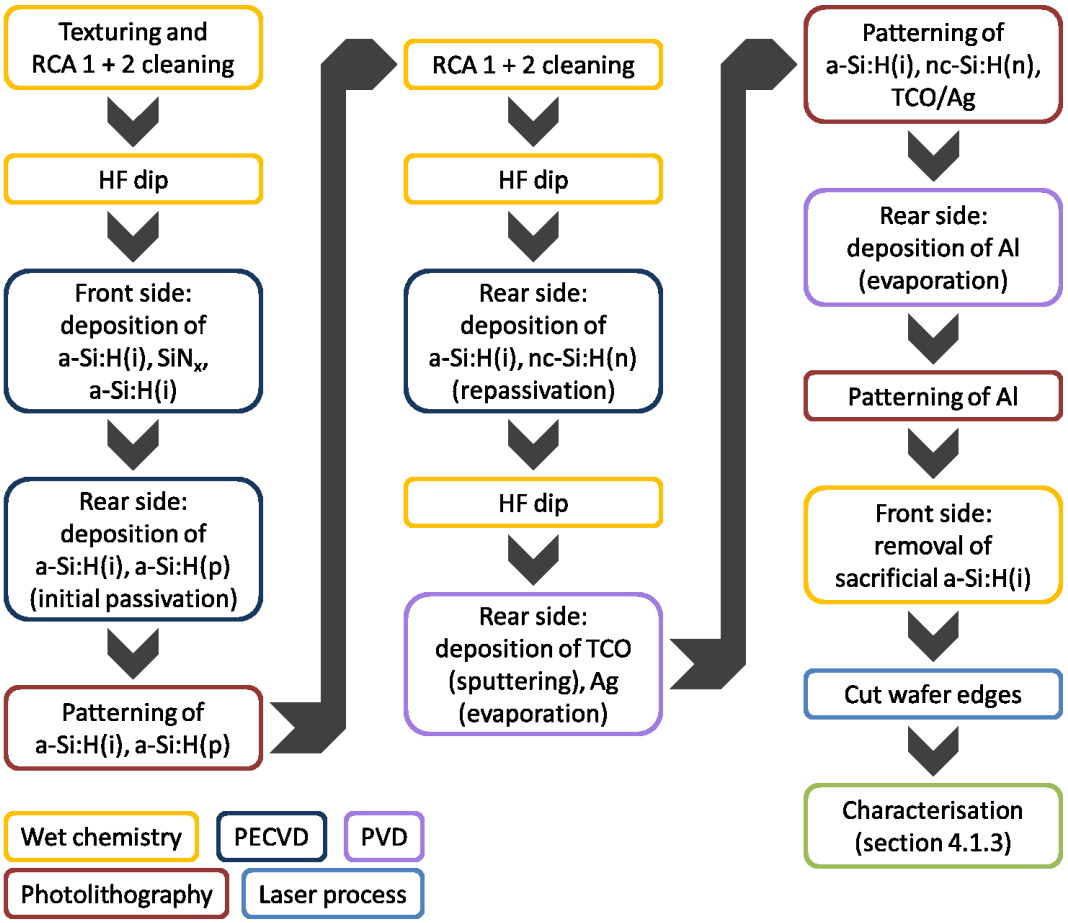


Figure 4.30: Flow chart of the adapted photolithography process for the implementation of a diffused aluminium emitter contact.

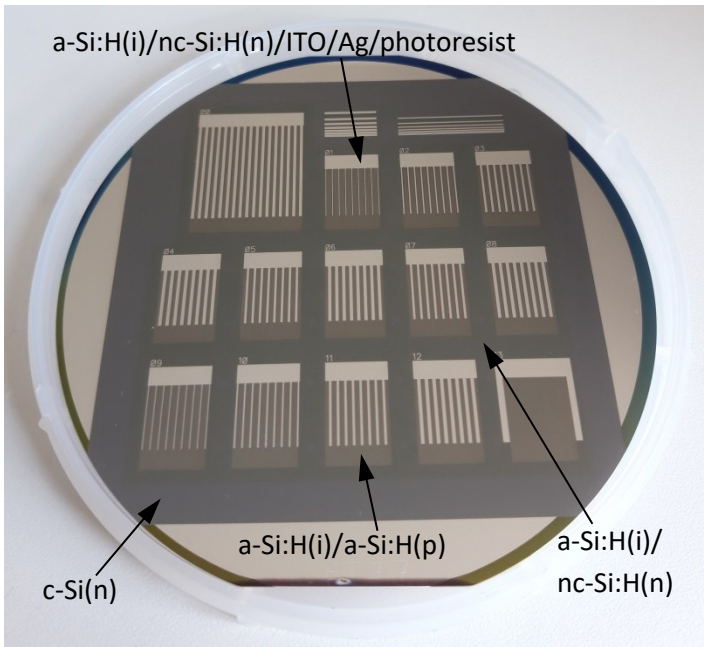
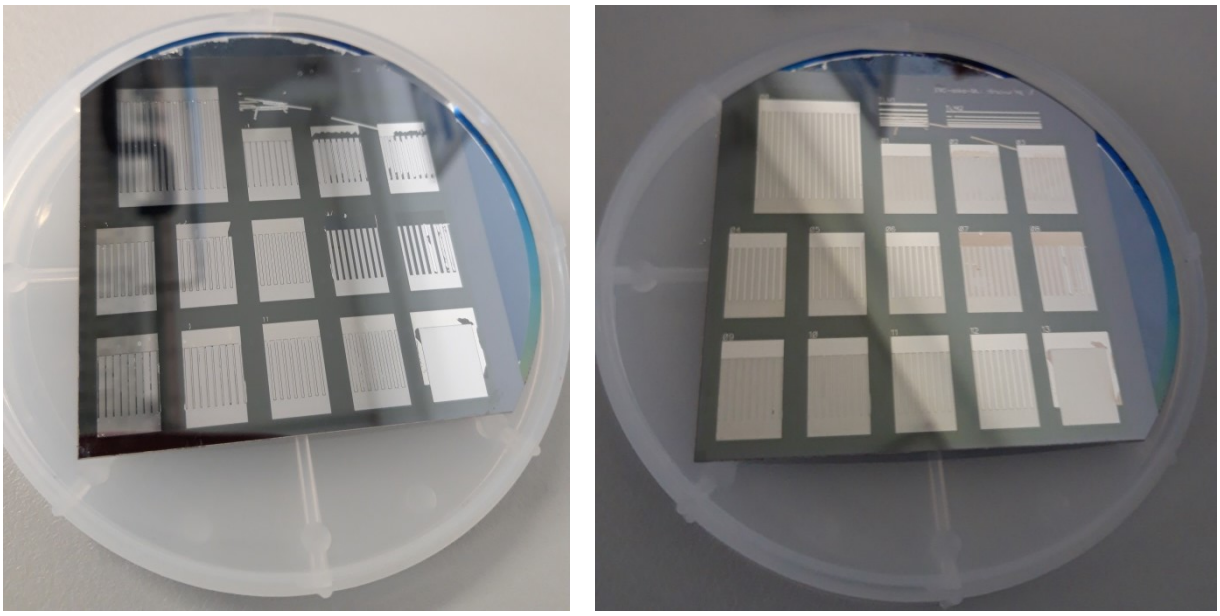


Figure 4.31: Rear side of a wafer featuring IBC SHJ solar cells fabricated with the photolithography process after successful BSF contact patterning and before applying the Al emitter metallisation.

Note that at this point during fabrication no RCA cleaning is possible due to samples being metallised and thus some organic contaminations might be present on the wafers' surfaces. This, however, could be an issue only for the emitter portions, but here the application of a diffused Al contact will lead to a defect-rich interface anyway and is thus assumed to be uncritical. Al is then full-area deposited by means of thermal evaporation. A lift-off procedure is carried out in an acetone bath to remove Al from the already structured BSF regions. The photolithography metallisation mask in combination with an Al etchant (cf. Table 3.2) is used for patterning this contact. Completion of the fabrication process is afterwards conducted as in the regular photolithography process. Unfortunately, the fabrication process described here faces still some difficulties during lift-off and Al patterning. Due to that, parts of the already structured ITO/Ag contact are also destroyed (cf. Figure 4.32a) and therefore Ag have to be reapplied and patterned once more (cf. Figure 4.32b).



a) **b)**

Figure 4.32: Rear side of a wafer featuring IBC SHJ solar cells fabricated with the photolithography process after a) initial Al emitter metallisation patterning with partly damaged BSF metallisation and b) reapplied and repatterned Ag contact.

Just as the lifetime samples of the previous section, the actual solar cells have to be annealed over a prolonged period of time so that Al can diffuse into a-Si:H(p) and the n-contact's ITO can crystallise. A direct comparison of the *j*–*V* characteristics of the best Al and regularly contacted IBC SHJ solar cell (the latter taken from section 4.3.4), yielding a PCE of 22.3% and 22.9% respectively, is depicted in Figure 4.33a. A slightly lower V_{oc} of

700 ± 4 mV (as compared to 710 ± 5 mV of the standard stack; cf. section 4.4.2) is found for the former probably due to the highly recombinative nature of the diffused a-Si:H(p)/Al contact (recombination losses in Figure 4.33b). Interestingly, no j_{sc} loss occurs despite the omission of any TCO, which is also confirmed by EQE (cf. Figure 4.33c) and IQE measurements (cf. Figure 4.33d). It therefore seems that parasitic plasmonic absorption in the metal contact and free-carrier absorption in the TCO are of similar magnitude in these specific devices.

The best Al-device's FF, albeit on a comparably high level of 77.5%, was actually expected to surpass that of the best standard contact solar cell (78.2%). The higher resistive losses in the Al-contacted solar cells (i.e. the difference between pFF and FF in Figure 4.33b; cf. also section 4.1.3 for further details) are therefore believed to stem from the damaged n-contact due to the aforementioned process related issues. Indeed, on three of the four processed wafers, the n-contacts' ρ_cs are not determinable by TLM measurements. In one case, although ohmic behaviour is obtained when measuring *j*–*V* characteristics between adjacent TLM measurement pads, the resulting resistances cannot be fitted linearly over the pad distance. In the other two cases, very high resistances (several hundred Ωcm²) irrespective of the spacing in between the TLM pads are observed. On the only sample where ρ_c determination is feasible, it is obtained to be 51 mΩcm², which is higher than that of the standard contact (about 30 mΩcm²) but does not sufficiently explain a lower FF of the Al-contacted solar cells, assuming that here the p-contact's ρ_c should be lower. Given the TLM structure's position close to the wafer's edge and an apparent non-uniform contact formation (at least for the BSF), it is proposed that the value determined by TLM measurements does not represents the n-contact's ρ_c of the actual solar cells.

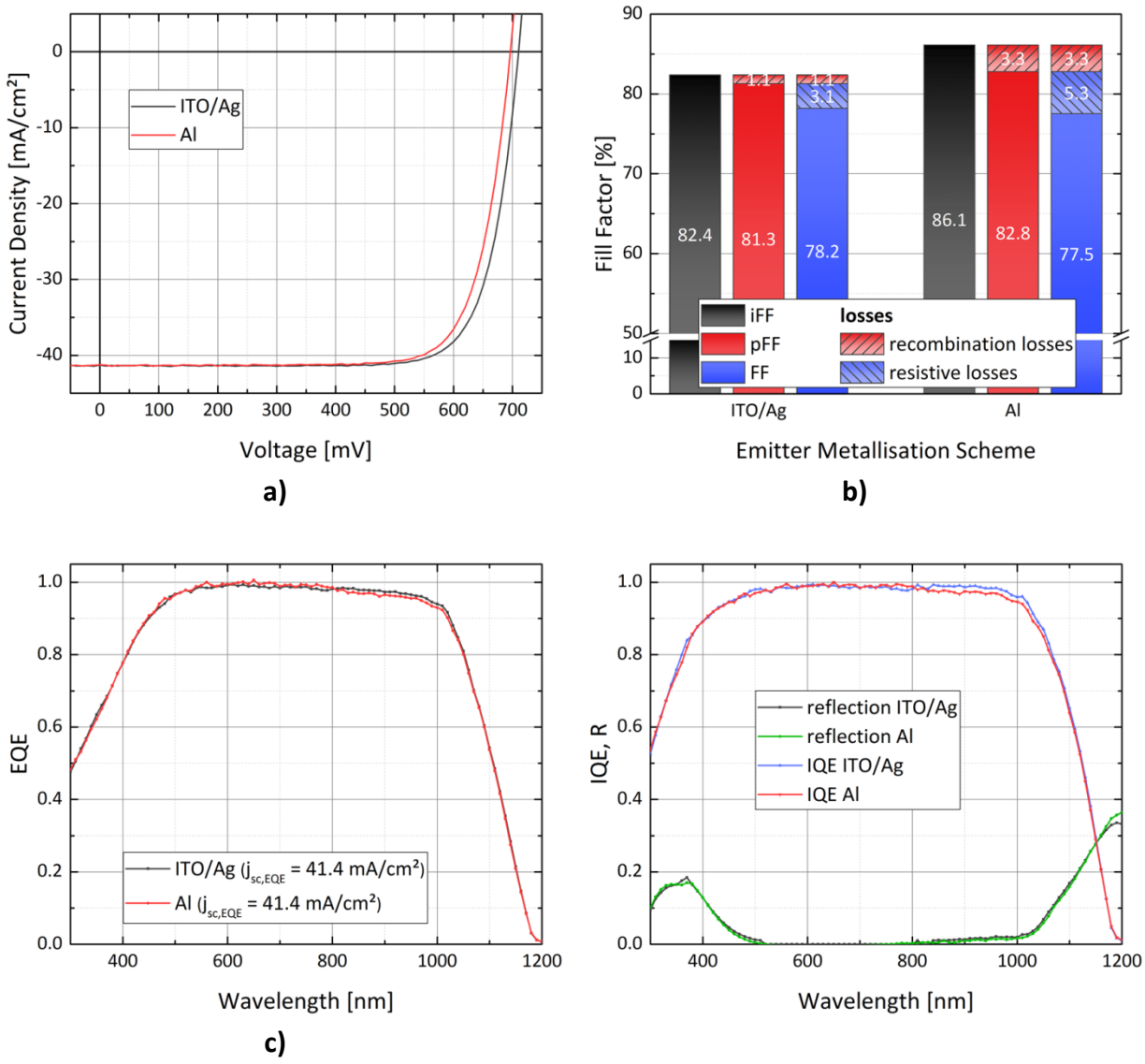


Figure 4.33: a) Illuminated one-sun current–voltage characteristics of the best IBC SHJ solar cells fabricated in the photolithography process, featuring different emitter metallisation schemes: a diffused Al (red) and an ITO/Ag contact (black); b) Fill factor losses of the two solar cells presented in a); c) external quantum efficiency measurements; and d) reflection and internal quantum efficiency measurements of these very solar cells. No severe current loss occurs in the long-wavelength regime despite omitting a rear-side ITO.

4.5.3 Simulation of the Diffused Aluminium-Based Contact Formation

When using the contact scheme proposed here, TLM measurements are inconclusive for determining the respective share in ρ_c of both minority and majority charge carrier contact stack. Therefore, electrical equivalent circuit simulations are conducted to understand the observed behaviour. IBC SHJ solar cells have been reported to be well describable with a two-diode model [35,150]. Additionally, as proposed in the previous section and in literature [211,220], the as-deposited a-Si:H(p)/Al contact utilised here exhibits rectifying

behaviour whereas the diffused contact can be sufficiently described by the s-shape model introduced in section 4.3.1. Diode characteristics of the two 'regular diodes' are extracted by fitting an ordinary two-diode model to dark *j–V* characteristics of a well-performing annealed Al-contacted solar cell. Certain parameters, such as both ideality factors, R_s, and R_{shunt} are known or obtained from electrical characterisation and therefore set fixed during the fitting procedure. The ideality factor of the Schottky diode is set to 1.04 according to [220] and its j_s can be calculated using equation (4.2) [186].

$$j_s = A^* \cdot T^2 \cdot \exp\left(\frac{-q \cdot \varphi_B}{k \cdot T}\right) \tag{4.2}$$

Here, A^* denotes the Richardson constant (32 $Acm^{-2}K^{-2}$ for p-type Si [186]) and φ_B the Schottky barrier height. In the simplest scenario, the latter can be calculated with knowledge of the metal's WF (Φ_m; 4.28 eV in the case of Al [102]) and the semiconductors electron affinity ($X_{a\text{-}Si}$; 3.9 eV in the case of a-Si:H, assuming a $X_{c\text{-}Si}$ of 4.05 eV for c-Si [100] and ΔE_{CB} of 150 meV [109] as discussed in section 2.1.4) by using equation (4.3) [100].

$$q \cdot \varphi_B = E_G - (q \cdot \Phi_m - q \cdot X_{a-Si}) \tag{4.3}$$

However, this approach is not applicable here as interface states and intrinsic defects pin the E_F to nearly midgap position regardless of the contact materials' WFs [128,129]. Indeed, the Schottky barrier height for a diffused Al/c-Si contact has been reported to be in the range of 0.4–0.6 eV [211] (for comparison, equation (4.3) yields 0.89 eV). Assuming a valence-band offset (ΔE_{VB}) of 0.20–0.45 eV (cf. section 2.1.4) and midgap E_F-pinning, the resulting φ_B of the diffused Al/a-Si:H(p) is in the order of 0.6–1.05 eV. The upper boundary is thus a rather large energetic barrier, which further explains the very high ρ_cs found for as-deposited Al/a-Si:H(p) contacts in section 4.5.1. However, as the contact is annealed, N_D in a-Si:H(p) rises at the interface, which enables tunnelling [137]. Here, ρ_c strongly depends on N_D and sufficiently high values of the latter (> 10^{19} cm^{-3}) will result in an ohmic contact and thus an increasing independence of φ_B [100]. Using equation (4.4) one can calculate the tunnel-dominated ρ_c as follows.

$$\rho_c = \frac{k}{q \cdot T \cdot A^*} \cdot \exp\left(\frac{4 \cdot \pi \cdot \sqrt{\varepsilon_0 \cdot \varepsilon_r \cdot m_{p,eff}}}{h} \cdot \frac{\varphi_B}{\sqrt{N_D}}\right) \tag{4.4}$$

Here, h denotes Planck's constant, ε_0 the permittivity in vacuum (both taken from [100]), ε_r the dielectric constant, and $m_{p,eff}$ the effective tunnelling mass of holes. The latter was found to be 0.1 times the electron rest mass m_0 [49,223]. Regarding ε_r, values of 11.9 [100] and 10.0 [224] have been reported for c-Si and a-Si:H respectively. In Figure 4.34, the resulting ρ_c for N_Ds ranging from 10^{18}–10^{20} cm^{-3} and φ_Bs of 0.6 eV and 1.05 eV are depicted. Values of < 1 Ωcm² are achieved for $N_D > 3.6 \times 10^{18}$ cm^{-3}–1.1×10^{19} cm^{-3} (for φ_B = 0.6 eV or 1.05 eV respectively), and obtaining 500 mΩcm², which is competitive to an ITO/Ag p-contact, necessitates an N_D of > 5.2×10^{18} cm^{-3}–1.6×10^{19} cm^{-3}.

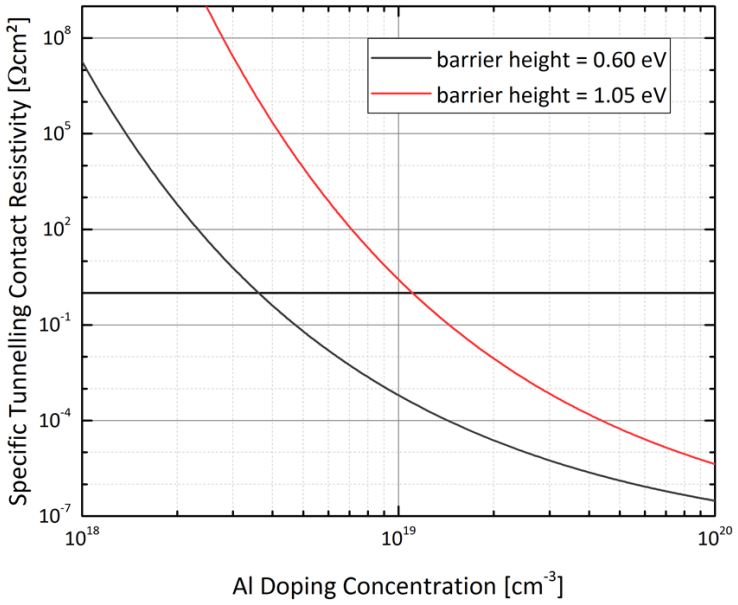


Figure 4.34: Specific contact resistivity of a diffused aluminium/a-Si:H(p) contact at high doping concentrations, enabling thus tunnelling of minority charge carriers. The horizontal black line represents 1 Ωcm².

Electrical equivalent circuit simulations are conducted using, again, LTspice (cf section 3.5 for further details); utilised modelling parameters are given in Table 4.8. All parameters are kept constant except for the $R_{sh,Schottky}$, which is swept from 0–1 kΩcm² to represent different states of Al/a-Si:H(p) interdiffusion: as-deposited rectifying mode (1 kΩcm²), effective shunting of the Schottky diode (0 Ωcm²), and various stages of contact formation (values in between). In Figure 4.35a, the resulting modelled j–V characteristics are depicted, which are in good agreement with measured results (Figure 4.35b; obtained by alternating annealing and measuring steps). The V_{oc} of the experimental device gradually shifts to lower values as the samples are further annealed. Electrically, this could be modelled with an increase in j_0 (especially of the first diode) whereof the V_{oc} strongly depends (e.g., increasing j_0 from

5.02×10^{-14} to 6.02×10^{-14} results in a decrease in V_{oc} of 4 mV). The j_0, in turn, is dictated by the SRV [146], which again increases with the defect density (i.e. for higher doping concentrations) [100]. This circumstance is, however, not regarded in the simulation and therefore the V_{oc} remains constant in all cases. Notwithstanding this deviation, the demonstrated model is believed to fairly represent the electrical behaviour of the investigated devices during contact formation, especially since V_{oc} decreases only marginally within the experimentally conducted annealing range (cf. Figure 4.35b).

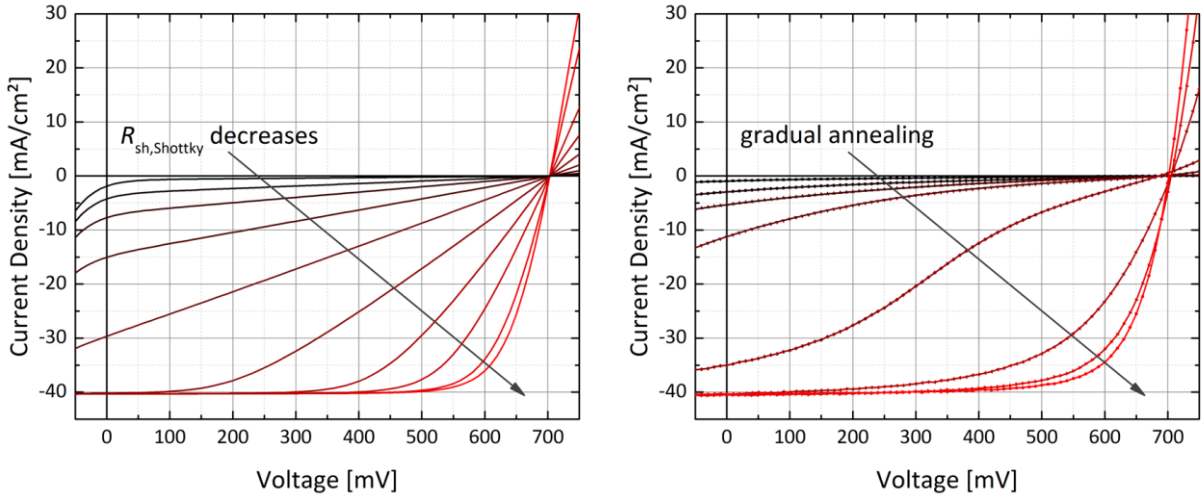


Figure 4.35: a) Modelled and b) measured illuminated one-sun current–voltage characteristics of an IBC SHJ solar cell fabricated in the photolithography process, featuring a diffused Al emitter contact and during different stages of contact formation upon annealing.

Table 4.8: Parameters for modelling the contact formation of IBC SHJ solar cells featuring a diffused Al emitter contact with LTspice. The resulting j–V characteristics are presented in Figure 4.30a.

j_{ph} [mA/cm²]	$j_{0,1}$ [A/cm²]	$j_{0,2}$ [A/cm²]	j_s [A/cm²]	n_1	n_2	$n_{Schottky}$	R_s [Ωcm²]	R_{shunt} [Ωcm²]	$R_{sh,Schottky}$ [Ωcm²]
41.3	5.02×10^{-14}	1.01×10^{-8}	5.93×10^{-15}	1	2	1.04	0.9	4500	0–1000[†]

[†] 0 Ωcm² represents effective shunting of the Schottky diode, 1000 Ωcm² the as-deposited rectifying mode

4.6 Summary of Chapter

IBC SHJ solar cells are prepared using two distinct fabrication techniques: photolithography and *in-situ* patterning with shadow masks. Several optimisation approaches are pursued and their influence on the devices' performance is investigated by means of optoelectronic

characterisation techniques and equivalent electrical circuit simulations with a strong focus on resistance and recombination-related losses. Investigated optimisation routes encompass altering the surface morphology, passivation scheme and thickness, and applying different metallisation concepts.

Open-circuit voltages (V_{oc}) as high as 723 mV are obtained when utilising a multilayer passivation stack where three intrinsic hydrogenated amorphous silicon (a-Si:H(i)) layers with different hydrogen contents are used (cf. section 4.4). However, in this approach the fill factor (FF), which is an indicator of parasitic resistive losses within the device, is limited to 76.0%. The latter can be increased to an experimentally found maximum of 79.2% by thinning the a-Si:H(i) layer, but thereby sacrificing a proper surface passivation, which is connected to achieving high effective minority charge carrier lifetime (τ_{eff}) of ≥ 2 ms at an excess minority charge carrier concentration (Δn) of 10^{15} cm^{-3} as well as V_{oc}s of ≥ 700 mV. However, a too thick passivation layer can hamper current extraction from the device as it introduces an energetic barrier especially for minority charge carriers (here: holes) and thereby leads to low FFs of ≤ 72%. A balanced ratio of sufficient surface passivation (as defined above) and unimpeded current extraction (optimised passivation layer thickness) yields a maximum power conversion efficiency (PCE) of 22.9% with a V_{oc} of 710 mV and a FF of 78.2% (cf. section 4.3.4). The resulting series resistance (R_s) amounts to only 0.6 Ωcm² whereof the p-contact's specific contact resistivity (ρ_c) holds with 423 mΩcm² by far the biggest share.

In order to lower the ρ_c of the minority charge carrier contact, an alternative contact stack where indium tin oxide (ITO) and silver (Ag) are replaced by aluminium (Al) is investigated (cf. section 4.5). It is found that the p-contact's ρ_c can be cut at least in half as compared to a standard ITO/Ag contact. However, due to as of yet unsolved process-related difficulties during wet-chemical patterning of the Al layer where parts of the ITO/Ag majority charge carrier contact stack are damaged (section 4.5.2), the overall R_s (0.9 Ωcm² in the best case) is assumed to suffer from a defective n-contact. Nonetheless, a FF of 77.5% and a PCE of 22.3% is achieved. It is further found that the short-circuit current density (j_{sc}) is not impacted by omitting ITO (here: only on the rear side). Transparent conductive oxides (TCOs), such as ITO, suppress parasitic plasmonic absorption in an adjacent metal layer, such as Ag [125]. On the other hand, the introduction of any TCO can lead to free-carrier absorption of

long-wavelength photons in the red and near-infrared part of the solar spectrum [16]. Since no loss in j_{sc} occurs when replacing ITO/Ag with Al, it is proposed that the effects of parasitic plasmonic absorption in the metal contact and free-carrier absorption of long-wavelength photons in the ITO are of similar magnitude in the investigated devices and cancel out each other (cf. section 4.5.2).

A slightly modified two-diode equivalent electrical circuit model adding just an antiparallel Schottky diode and a shunt resistor, which represents the effectiveness of hole extraction by tunnelling, is sufficient to describe the electrical behaviour during contact formation. This model is able to simulate the effects of changing specific contact resistivity and resulting *j*–*V* characteristics at incremental steps of annealing-induced Al/a-Si:H(p) interdiffusion. The change from rectifying Schottky to ohmic characteristics is explained as follows. As-deposited Al forms a rectifying Schottky contact with a-Si:H(p). Upon annealing with moderate temperatures (> 160 °C), Al starts to diffuse into a-Si:H(p) under formation of aluminium silicide that leads to a drastic decrease in ρc. The latter strongly depends on the doping concentration (N_D) in a-Si:H(p) at the interface. Due to Al diffusion, N_D increases and sufficiently high values of $> 10^{19}$ cm^{-3} enable tunnelling of holes and result in an ohmic contact.

The FF of IBC devices is partly limited due the restriction of the contact area to the rear side. Introducing texturing on the rear side therefore bears a huge potential improving especially the FF due to increasing the active contact area, which holds true particularly for the p-contact. However, during the minority charge carrier contact patterning by means of isotropic wet-chemical etching, pyramidal valleys and facets are altered and become potential centres for epitaxial growth, which renders the subsequent repassivation procedure (i.e. the deposition of passivation and majority charge carrier contact) challenging. On the other hand, no such step is required in the shadow-mask process since here the doped layers are patterned *in-situ* and thus the beneficial effect of having an increased contact area due to a textured surface can be fully exploited, yielding a maximum FF of 73.7% and a PCE of 20.5% (cf. section 4.2.3). To put this into perspective, the former best in-house PCE of a solar cell fabricated by the shadow-mask process and featuring a polished rear side amounts to merely 17.0%.

Devices fabricated by the shadow-mask process are still limited by a reduced V_{oc} (maximum 672 mV) due to a poor emitter passivation stemming from altered a-Si:H(p) growth conditions during the deposition through a mask. This leads to altered layer characteristics, which might render the a-Si:H(p) layer incapable of sufficiently screening the a-Si:H(i)/c-Si interface from ITO work function mismatch (cf. section 4.2.3). The first issue can be solved by implementing an aforementioned multilayer passivation into the shadow-mask process, but this comes at the cost of a reduced FF. Unfortunately, no satisfactory solution has been found so far for addressing the second problem, but in general it should be solvable by adapting the deposition conditions of either emitter stack or ITO; or possibly by choosing an alternative TCO.

The following Table 4.9 gives a comprehensive overview over the best solar cell results achieved with the different optimisation approaches as well as notable further results (best values for other parameters than PCE). The *j*–*V* characteristics of the best IBC SHJ solar cells fabricated in this thesis are presented in Figure 4.36.

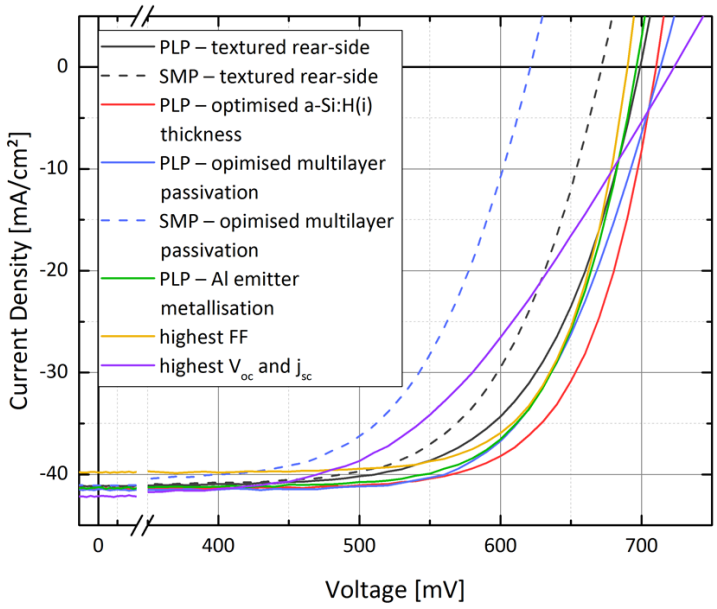


Figure 4.36: Illuminated one-sun current–voltage characteristics of a selection of best (and notable) IBC SHJ solar cells fabricated with different approaches during the course of this thesis. Devices prepared with the photolithography process (PLP) are presented as solid lines, those fabricated with the shadow-mask process (SMP) as dashed lines. Note the break in the abscissa, which is included to emphasise the MPP region and facilitate a distinction of the investigated approaches.

Table 4.9: Summary of best and notable solar cell results obtained by various investigated optimisation approaches. The abbreviations PLP and SMP denote the photolithography and shadow-mask process respectively. Champion devices are marked in red (PLP) and blue (SMP). The list includes solar cells that stand out for featuring the highest V_{oc}, FF, or j_{sc} obtained during the course of this thesis. These values are marked in bold.

Process	*Substrate type*	*Cell size [cm²]*	V_{oc} *[mV]*	j_{sc} *[mA/cm²]*	*FF [%]*	*PCE [%]*	R_s[†] *[Ωcm²]*
PLP – textured surfaces	DST	1 × 1	699	41.2	74.1	21.3	0.5[‡]
	DST	1 × 1	700	41.7	73.6	21.2	0.8[‡]
SMP – textured surfaces	DST	1 × 1	672	41.1	73.7	20.5	1.0
	DST	2 × 2	662	41.7	72.4	20.0	0.8
PLP – optimised passivation layer thickness	SSP	1 × 1	710	41.3	78.2	22.9	0.6
	SSP	2 × 2	715	41.1	77.7	22.8	0.8
	SSP	1 × 1	690	39.8	**79.2**	21.8	0.5
	SSP	1 × 1	697	**42.0**	75.5	22.1	1.7
PLP – multilayer passivation	SSP	1 × 1	713	41.5	76.0	22.5	1.2
	DST	1 × 1	710	41.3	69.2	20.3	2.0[‡]
	DST	2 × 2	**723**	**42.1**	63.5	19.4	3.5[‡]
SMP – multilayer passivation	DST	1 × 1	621	41.3	71.2	18.2	1.4
PLP – Al emitter contact	SSP	1 × 1	696	41.3	77.5	22.3	0.9
	SSP	1 × 1	696	41.7	76.1	22.1	1.0

[†] derived from SunsVoc measurements if not stated otherwise

[‡] extracted by the dark j–V method

5 Tandem Applications of IBC SHJ Solar Cells

In order to overcome the inherent PCE limitations [17,23] of a single-junction solar cell, the utilisation of multiple absorbers with different band gaps is required as this allows for more efficient conversion of photon into electrical energy by means of reduced thermalisation and transmission losses. Tandem solar cells, IBC 3T tandem devices in particular, have been introduced in section 2.3. There, their basic functionality and subcell interconnection schemes are discussed. Here, the first experimental realisation of an IBC 3T tandem device combining a perovskite top with a c-Si bottom cell is presented. First, the fabrication process is described, followed by an in-depth optoelectronic device characterisation. Afterwards, electrical equivalent circuit simulations are conducted to shed light on the observed electrical behaviour. With thus obtained understanding of the investigated devices, limitations of and possible optimisation routes for these first proof-of-concept IBC 3T tandem solar cells are discussed. The chapter concludes with an estimate of the achievable PCE potential as compared to more common 2T and 4T concepts. Note that a comprehensive insight into perovskite solar cells cannot be given here. IBC 3T tandem devices have been developed in cooperation with a fellow PhD candidate, Philipp Tockhorn, who is responsible for the perovskite fabrication development. Therefore, the main focus here is on the IBC bottom cells as well as subcell interconnection and contacting schemes. A large portion of the results presented in this chapter is included in a corresponding publication [165].

5.1 Fabrication Process of IBC 3T Tandem Solar Cells

Here, the fabrication process of each subcell is briefly described, starting with the bottom cell, which is prepared first and then serves as a substrate for top cell fabrication.

5.1.1 IBC SHJ Bottom Cell Fabrication

The fabrication process that is described in the following two sections, results in a structure as schematically depicted in Figure 5.1.

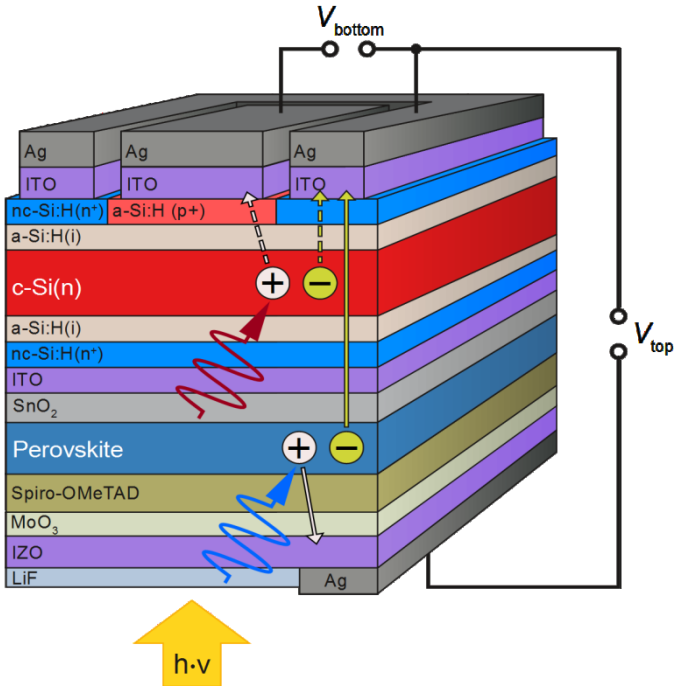


Figure 5.1: Upside down schematic of a three-terminal tandem device with interdigitated back contact (not to scale) comprising a perovskite top and a c-Si bottom cell. Note that, for the sake of simplicity, the rear side is depicted flat whereas in reality it is textured with random pyramids.

The fabrication of bottom cells is in general based on the photolithography process as described in sections 3.3.1 and 4.1.1, but is slightly adapted to match the requirements of the perovskite top cell preparation and subcell interconnection. Two batches of IBC 3T tandem devices are prepared, both utilising the standard 4" c-Si(n) FZ wafers with a specific wafer resistivity (ρ_{bulk}) of 1–5 Ωcm and a wafer thickness of approximately 280 µm but different surface morphology: in the first batch, double-side polished; SSP in the second batch, but here featuring a polished front and textured rear side. The latter constraint is necessary as the perovskite top cell's fabrication route relies on spincoating, which demands a flat surface to enable uniform coverage [225]. Texturing the rear side, in turn, should be beneficial especially for the bottom cell's j_{sc} and FF (as laid out before; cf. section 4.2.2).

The rear-side layers are deposited and patterned according to the regular photolithography process. At the front side, instead of using an optically favourable combination of passivation layer and ARC, a layer stack comprising a-Si:H(i), nc-Si:H(n), and ITO (the former serves as surface passivation, the latter two as subcell interconnection [97]) is deposited using PECVD and PVD (cf. section 3.1). The approximately 20 nm thick front-side ITO is chosen here, apart from keeping the parasitic absorption low, because the deposition conditions of tin dioxide (SnO_2), which is utilised as the perovskite's electron transporting layer (ETL), are optimised

for the growth on this particular ITO. Furthermore, no lateral conductivity is needed and therefore the front side ITO layer can be kept thin. The front side ITO is then structured using the simplified photolithography-like metallisation patterning approach of the shadow-mask process (cf. section 4.1.2). Here, a negative-type photoresist is applied to the bottom cell's front side, treated as described in section 4.1.2, and exposed to UV irradiation through a laser-cut mask that matches size and position of each solar cell on the rear side of the wafer. Subsequent developing, ITO etching, and photoresist stripping conclude the patterning process.

Afterwards, *j*–*V* characteristics of all IBC SHJ solar cells are measured to select the most promising candidates for tandem integration. Gradual annealing of up to 14 min is conducted to cure sputter damage of the rear-side a-Si:H(i) passivation and allow for hydrogen redistribution within that layer [91,114,167]. Solar cells are then separated by laser cutting.

Due to an inferior light in-coupling scheme as compared to a standard front side (texturing and ARC), j_{sc}s and V_{oc}s of only 28 mA/cm² and 690–695 mV respectively are achieved as a direct consequence of the dependence of the incident irradiation; the impact on the V_{oc} is less severe as it only depends logarithmically on the incident irradiation. For comparison, the same solar cell would feature a V_{oc} of approximately 705 mV under the assumptions of j_{sc} = 40 mA/cm² and an unchanged j_0. A maximum FF of only 70% is obtained, which is due to the challenging procedure of conducting the photolithography process on textured surfaces (cf. section 4.2.2). The resulting PCEs of the thus processed bottom cells amount to at least 12.5% (for selected samples) with a maximum of 13.6%. The PCE of these solar cells at a j_{sc} = 40 mA/cm² would amount to approximately 19%.

5.1.2 Perovskite Top Cell Fabrication

Before perovskite top cells are fabricated, IBC SHJ bottom cells substrates are cleaned in isopropyl alcohol and afterwards treated in a UV ozone cleaner for 30 min. SnO_2 with a thickness of 30 nm is then deposited by spincoating a tin chloride dehydrate ($SnCl_2 \cdot 2H_2O$) precursor solution (manufactured by Sigma Aldrich) to form the ETL, which is subsequently annealed at 180 °C for 60 min in order to desorb solvents of the precursor solution and cure that layer. After that, another UV ozone treatment is conducted for 15 min and the surface is

processed further by spincoating a solution containing 2.5 mg/ml of potassium nitrate (KNO_3) onto it, followed by another curing step for 10 min at 100 °C. The latter was found to suppress interface recombination occurring at the ETL and hystereses of the *j–V* characteristics [226], which some perovskite solar cells are prone to [227].

Following the procedure described in [228], the actual top cell's absorber consists of a 550 nm thick mixed-cation lead mixed-halide perovskite layer with the molecular formula $Cs_{0.05}(FA_{0.83}MA_{0.17})_{0.95}Pb(I_{0.83}Br_{0.17})_3$, which is, again, deposited by spincoating a prepared precursor solutions that contains formamidinium iodide (FAI), lead iodide (PbI_2), methylammonium bromide (MABr) and lead bromide ($PbBr_2$). Towards the end of this procedure, 150 µl of chlorobenzene (CBZ) is added to initialise the crystallisation of the perovskite absorber. Top cell fabrication is concluded by annealing samples at 120 °C for 60 min. The resulting band gap of this absorber material amounts to 1.7 eV. Doped Spiro-OMeTAD [229] with a thickness of 110 nm is subsequently spincoated to form the perovskite's hole transporting layer (HTL).

Contact formation is then achieved by thermally evaporating a 35 nm thick layer of molybdenum oxide (MoO_3) at a base pressure of 10^{-6} mbar to protect the HTL from damage induced by sputtering [230] with which the subsequent IZO (75 nm) is deposited. Top cell fabrication is concluded by thermally evaporating, first, a 150 nm thick Ag frame (through a shadow mask) around the edges of the IZO layer, defining thus a designated illumination area (da) of 0.78 cm²; and, second, (only in the second batch) a 115 nm thick ARC of lithium fluoride (LiF). For a more detailed description of the top cells' fabrication procedure, the reader is referred to [165]. A scanning electron microscope image of a perovskite top cell's layer and interfacial region to an IBC SHJ bottom cell is shown in Figure 5.2a.

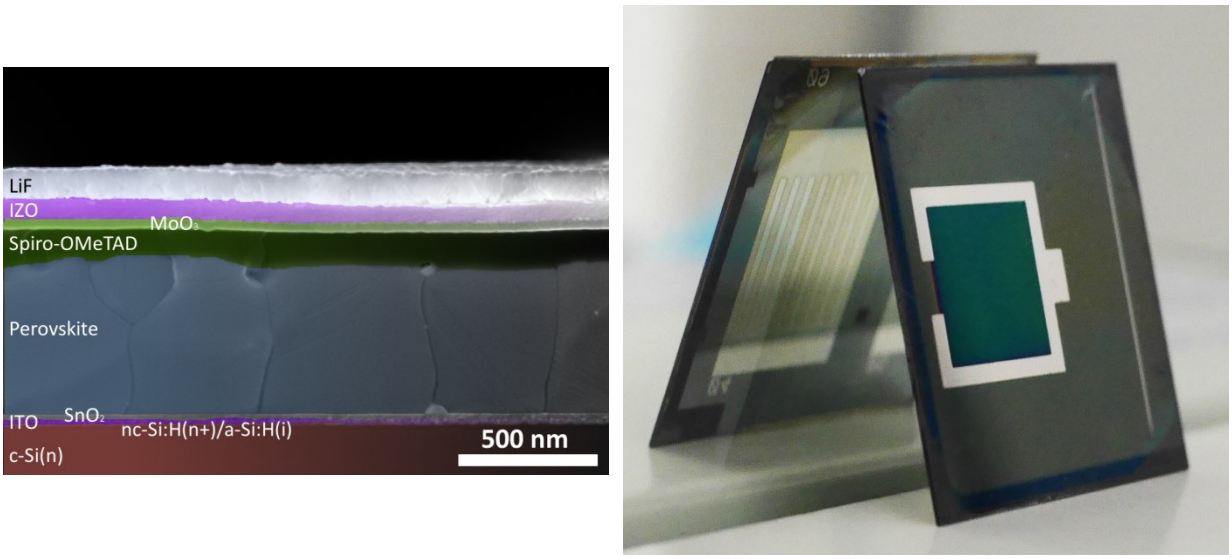


Figure 5.2: a) Scanning electron microscope images (cross section) of a perovskite top cell's layers and the interface towards a c-Si bottom cell. Note that the a-Si:H(i)/nc-Si:H(n) layer stack is actually not visible in the image, but its position is marked nonetheless; b) photograph of an IBC 3T tandem solar cell leaning against a mirror in order to simultaneously show both subcells.

5.1.3 Device Layout and Working Principle

A photograph of a device prepared with the fabrication process described above is shown in Figure 5.2a and results in a structure schematically depicted in Figure 5.2b. Charge carriers photogenerated within the bottom cell by absorbing mainly near-IR photons are collected at their respective electrodes, just like in an ordinary IBC solar cell. In the perovskite top cell, photogeneration of charge carriers takes place by absorbing shorter-wavelength photons from the visible part of the electromagnetic spectrum. The chosen top cell configuration leads to holes being electrically blocked by the n-type interconnection layers (SnO_2, ITO, and nc-Si:H(n)) as they face a high energetic barrier within the VB (cf. Figure 5.3). They are therefore collected through the HTL at the front-side electrode. This barrier, however, does not exist for electrons generated in the top cell and thus they can pass through the interconnection layers into the c-Si wafer to be collected by the IBC's n-contact. Creating such an asymmetric energetic barrier for charge carriers photogenerated in the top cell is necessary to attain sufficient electron selectivity [76].

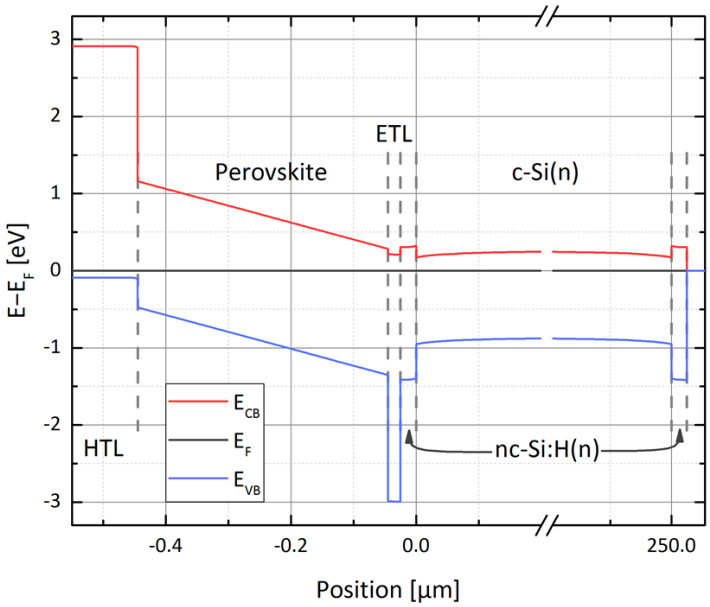


Figure 5.3: Simplified equilibrium band diagram of the subcell interconnection region of an IBC 3T device [231]. A substantial energetic barrier in the valence band (induced by the electron transporting layer, ETL) hinders holes photogenerated within the top cell to pass into the bottom cell.

Adding an entire wafer to the top cell's n-contact is likely to negatively impact its FF. The corresponding additive R_s components are: the specific contact resistivity of the bottom cell's n-contact, $\rho_{c,n,IBC}$; the lateral bulk-related R_s described by equation (4.1); the vertical bulk-related R_s, which is simply $\rho_{bulk} \times W$; and the ρ_c of the additional interconnection layer stack at the bottom cell's front side (i.e. the c-Si(n)/a-Si:H(i)/nc-Si:H(n)/ITO/SnO_2 interface), which is unknown, but due to featuring only small band offsets, charge carrier transport should be dominated by thermionic emission [94] and thus this ρ_c mainly depends on the different ΔE_{CB}s [100].

Drift-diffusion simulations, presented in [165], are carried out by using Sentaurus TCAD to investigate whether the defined energy landscape impairs the extraction of top cell electrons considerably. However, it is found that the effect described above is almost negligible as FF and V_{oc} decrease by only 0.2%$_{abs}$ and 3.3 mV respectively when both subcells operate at their MPP (as compared to the single-junction case). Indeed, the mutual influence of both subcells is found to be rather marginal, regardless of the operating conditions (i.e. MPP, open circuit, short circuit, or anywhere in between) and thus the assumption of independently working subcells [76] holds true for properly engineered IBC 3T tandem devices.

When considering the opposite case, i.e. adding a perovskite absorber atop an IBC SHJ bottom cell, the top cell ideally acts only as a filter for the visible spectrum range. As less light reaches the bottom cell, j_{sc} and (logarithmically dependent) V_{oc} decrease while, concomitantly, FF increases as the resistive power loss depends on the square of the current density. Additionally, absorbing only near-IR photons leads to more uniform charge carrier generation within the entire c-Si bulk rather than primarily at its front surface, which should mitigate the vertical component's impact of the bulk-related R_s because the average travelling distance for electrons and holes is thereby reduced. This is also confirmed by the simulation as described above: j_{sc} and V_{oc} loss amount to 21.6 mA/cm² and 35 mV respectively, and the FF gain is $1.2\%_{abs}$. A simple experiment is conducted to verify these findings. Upon measuring *j–V* characteristics of the IBC SHJ bottom cells before top cell fabrication, a glass substrate with the same perovskite used in the actual devices is put on top of the bottom cells to optically mimic a top cell's presence in the tandem case. Similar trends and values as in the simulation are observed with this experiment, i.e. a reduction of j_{sc} and V_{oc} while the FF increases.

5.2 Electrical and Optical Characterisation

Conventional characterisation techniques as described before for single-junction solar cells, such as transient photoconductance decay (TrPCD) and photoluminescence (PL) measurements are used to monitor the bottom cell fabrication processes. Here, the results of optoelectronic measurements conducted on finalised IBC 3T tandem devices are presented and discussed.

5.2.1 Electrical Characterisation of IBC 3T Tandem Solar Cells

Illuminated *j–V* characteristics of IBC 3T tandem devices are obtained under STC by using an LED-based sun simulator (Wavelabs Sinus 70), introduced in section 3.4.3, and a shadow mask with an aperture of (9 × 9) mm² defining the devices' da. A flip chuck is used where both subcells are contacted and the devices' front sides are illuminated as shown in the photographs in Figure 5.4. Four-wire sensing is used to eliminate the impact of the probes' contact resistances.

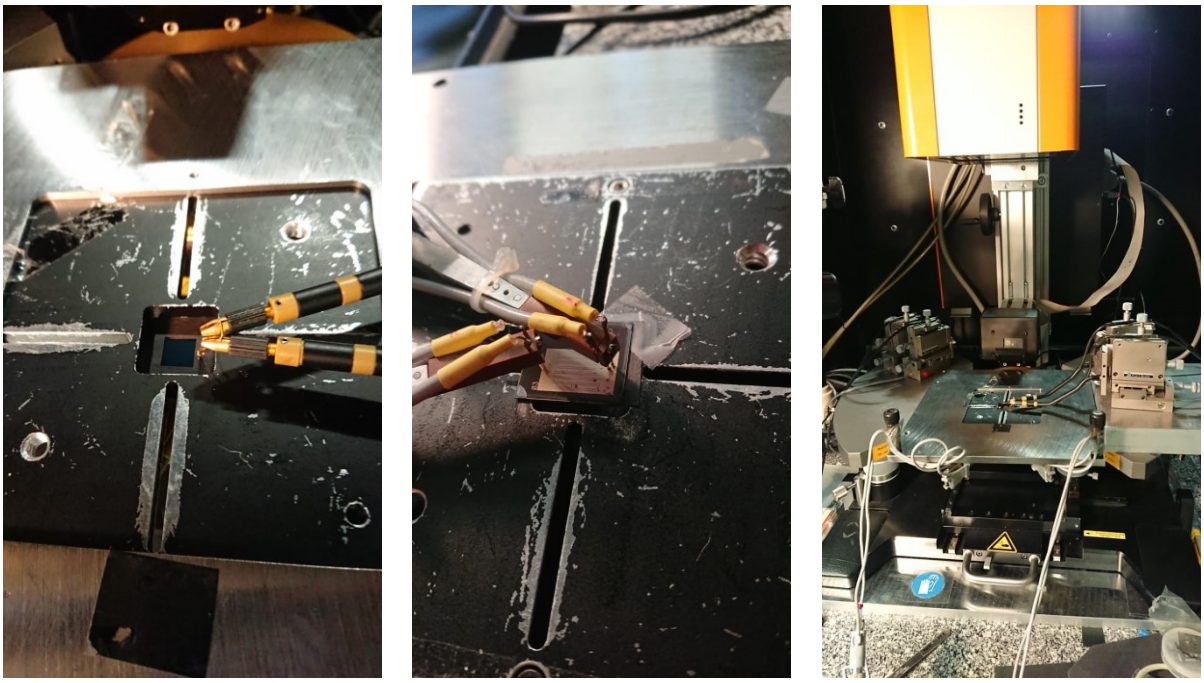


Figure 5.4: Measurement procedure for obtaining current–voltage characteristics of IBC 3T tandem solar cells investigated here using the sun simulator Wavelabs Sinus 70 and a flip chuck: a) probing a masked perovskite top cell (hole contact), b) probing an IBC SHJ bottom cell (both hole and shared electron contact), and c) positioning the measurement chuck inside a sun simulator.

Both subcells are connected to two separate source measure units with the IBC SHJ's n-contact functioning as common ground. The *j–V* characteristics of both subcells can thus be measured individually and simultaneously when performing under different operating conditions, which is important for capturing the exact current distribution within each subcell [77] and their mutual influence. Figure 5.5a shows *j–V* characteristics of both subcells when the respective other cell is held at MPP conditions (i.e. the desirable working condition); Figure 5.5b depicts their simultaneously MPP-tracked PCEs. In addition, the measured solar cell parameters for this specific operating point (i.e. one subcell operates at MPP, the other subcell is measured) are summarised in Table 5.1. As can be seen there, the combined PCE for the device-relevant case of both subcells operating at MPP amounts to 17.1%, with top and bottom cell contributing 11.7% and 5.4% respectively.

Table 5.1: Measured solar cell parameters of the so far best IBC 3T device for each subcell while the other subcell operates under MPP conditions.

Subcell	*Scanning direction*	V_{oc} *[mV]*	j_{sc} *[mA/cm²]*	*FF [%]*	PCE_{j-V} † *[%]*	PCE_{MPP} ‡ *[%]*
Perovskite	V_{oc} to j_{sc}	1117	17.4	63.5	12.3	11.7
	j_{sc} to V_{oc}	1104	17.3	57.5	11.0	
IBC SHJ		600	14.4	64.2	5.5	5.4
				Σ_{PCE}	**17.8**	**17.1**

† derived from single scans

‡ stabilised MPP after 10 min of MPP tracking

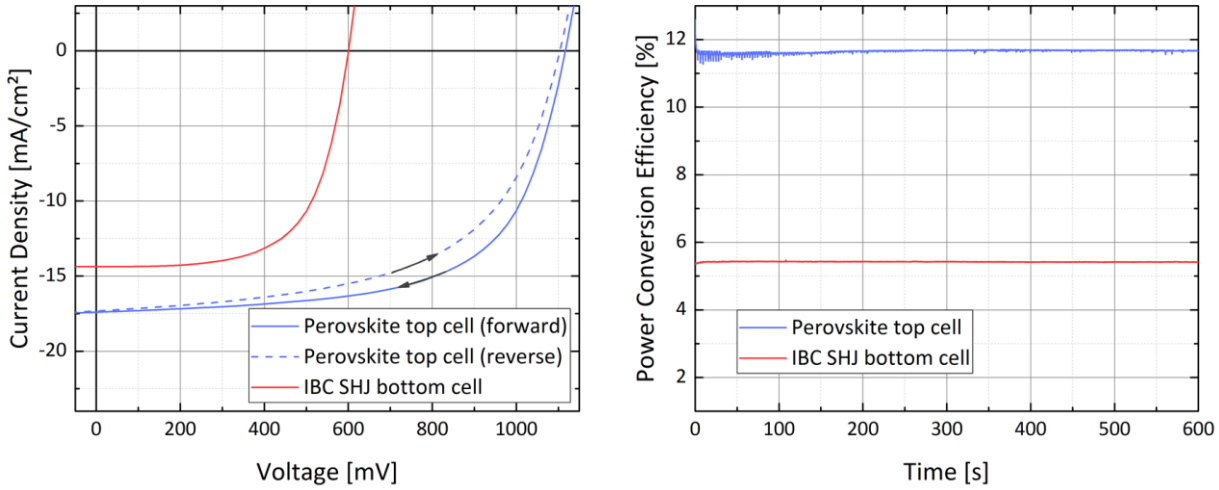


Figure 5.5: a) Illuminated one-sun current–voltage characteristics of top (blue) and bottom cell (red) while the respective other subcell is held at MPP conditions; b) PCE track of both subcells over 10 min while they are held at their respective MPP.

In Figure 5.6, the electrical equivalent circuit of the device that is later on used for electrical modelling is displayed. It is shown here already to make the following discussion more comprehensible.

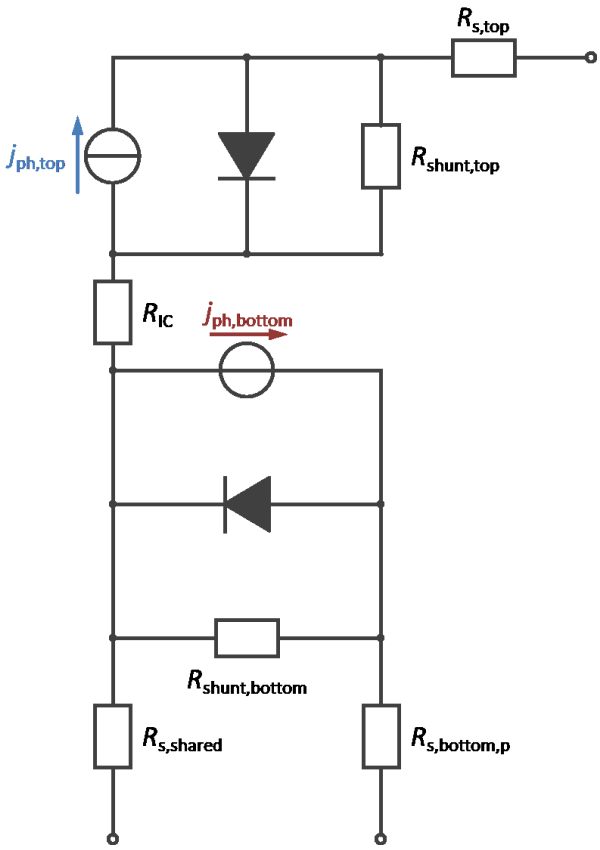


Figure 5.6: Electrical equivalent circuit model of the IBC 3T configuration including all parameters used in the LTspice model later on. R_{IC} denotes the interconnection resistance stemming from the subcell interconnection layers. The R_s of the bottom cell is split into the specific contact resistivity of the p-contact ($R_{s,bottom,p}$) and the combined resistance of the n-contact and the c-Si bulk (i.e. the resistance that is shared by both subcells, $R_{s,shared}$).

The mutual influence of both subcells is investigated by applying a bias voltage (swept in small increments from V_{oc} conditions to 0 V) to one of them and simultaneously scanning the *j*–*V* characteristics of the respective other subcell, setting thus different operating points. The resulting *j*–*V* characteristics for both subcells while the other subcell is set to V_{oc}, MPP, and j_{sc} conditions are shown in Figure 5.7a and b. In each case, ten sweeps are conducted at each applied bias voltage and afterwards averaged for statistical evaluation. In the following, especially the common IBC electron contact is of relevance because theoretically only this contact should be affected by the procedure described above and its ohmic losses are shared by both subcells.

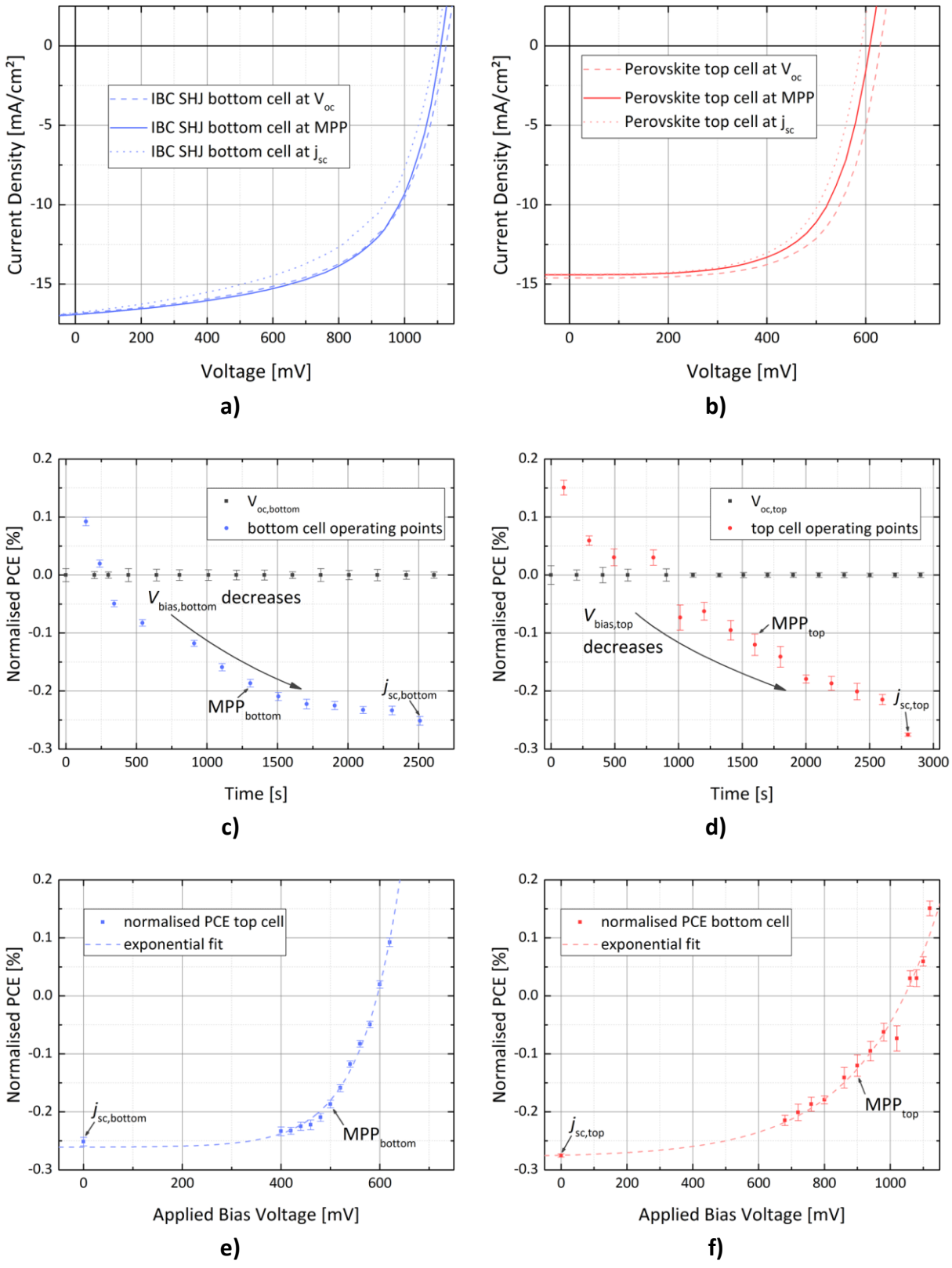


Figure 5.7: a) Illuminated one-sun current–voltage characteristics of the top cell (red) while the bottom cell is held at V_{oc} (dashed), MPP (solid), and j_{sc} conditions (dotted); c) normalised change in PCE (with respect to V_{oc} conditions) of the top cell over time when the bottom cell is alternatingly set to V_{oc} and different bias voltages; e) dependence of the top cell's normalised change in PCE of the bias voltage applied to the bottom cell (following an exponential trend; dashed curve). Figures b), d), and f) apply for the bottom cell accordingly.

When (starting from V_{oc} conditions) reducing the bias voltage (i.e. increasing the current extraction) in the biased subcell, the PCE of the measured subcell decreases due to a reduction in V_{oc}. This leads to increased ohmic losses at the shared electron contact ($R_{s,shared}$) stemming from a voltage drop that is equal to $R_{s,shared} \times (j_{top} + j_{bottom})$. For the bottom cell being measured, this behaviour is way more pronounced than for the top cell. This can be explained by a superposition of bias-voltage-induced changes and slow ion movements within the perovskite absorber upon illumination [227,232].

To verify these findings, a similar experiment is conducted. Here, one subcell is MPP-tracked for 3000 s whilst the other subcell is alternatingly set to V_{oc} and gradually declining bias voltages. Each biasing step amounts to 100 s. The PCE of the measured subcell is derived from the average stabilised value for each biasing step. The normalised change in PCE is then calculated as the difference in PCE at V_{oc} and varying bias voltages (for V_{oc} conditions this difference is consequently zero). Figure 5.7c and d show the normalised change in PCE for alternating bias and V_{oc} conditions over time. It amounts to about 0.25% and 0.30% for top and bottom cell respectively when going from V_{oc} to j_{sc} conditions. When plotting this normalised change in PCE over the applied bias voltage (cf. Figure 5.7e and f), the data follows an exponential trend, which stems from the non-linear diode behaviour of the biasing subcell and a voltage drop over $R_{s,shared}$.

A considerable drop of approximately 80 mV in the bottom cell's V_{oc} occurs after implementation into the tandem device, which cannot be explained simply by a filtering effect through the top cell (this was found to be only 35 mV in cf. section 5.1.3). Additionally, a slight decrease of 2.5%$_{abs}$ in the bottom cell's FF is also contradictory to the expectations. Instead, these deviations from the anticipated behaviour can be ascribed to limitations of the current tandem design. Owing to differences in sizes of top and bottom cell (0.78 cm² vs 1 cm²), a considerable share of the bottom cell's active area is shaded by the top cell's front contact and its V_{oc} is reduced due to additional recombination in this dark parasitic diode (i.e. its non-illuminated portion) [233]. This behaviour has been also recently reported for size-mismatched 4T perovskite/silicon tandem solar cells [234]. What further exacerbates the situation is the fact that the outer fingers of the IBC SHJ bottom cell in this thesis are always part of the minority charge carrier contact, which reacts more sensitive to reduced contact area (here: by means of shading) than the BSF [50,193]. This can reasonably well explain the

observed reduction in FF. Both cell size matching and good alignment (which is achieved here) of both subcells are thus important design criterions as the mentioned effects can drastically impede the overall performance of an IBC 3T tandem solar cell. These findings are therefore no inherent shortcomings of the concept itself, but merely a still apparent flaw of the current design.

5.2.2 Optical Characterisation of IBC 3T Tandem Solar Cells

EQE and reflection measurements are conducted in order to assess optical losses of the investigated devices. For this, a large-spot filter wheel EQE, introduced in section 3.4.6, is used, with the top cell being measured from 340–800 nm and the bottom cell from 500–1200 nm. As can be seen in Figure 5.8, both subcells contribute to the photogenerated current in their respective ranges of the spectrum. Additionally, measured j_{sc} values (cf. Table 5.1) and those calculated from EQE data match very well for the top cell ($j_{sc,j–V}$ = 17.4 mA/cm² vs $j_{sc,EQE}$ = 17.3 mA/cm²) and still reasonably well for the bottom cell ($j_{sc,j–V}$ = 14.4 mA/cm² vs $j_{sc,EQE}$ = 13.7 mA/cm²). A slightly reduced minority charge carrier lifetime, obtained from TrPCD measurements before metallisation, is found for the bottom cell under low-injection conditions. Since the illumination intensity during EQE measurements is well below that of determining one-sun *j*–*V* characteristics as conducted beforehand, the lower EQE-integrated j_{sc} can be ascribed to this circumstance. This finding is further validated by applying halogen bias illumination and compensating the thus photogenerated current with a Keithley 2400 source meter. Due to a now increased amount of excess minority charge carriers, the EQE-integrated j_{sc} reaches 13.7 mA/cm², which almost matches the measured value. The remaining discrepancy can be explained by the fact that even with bias illumination, the intensity conditions (100 mW/cm²) of the used sun simulator are not met.

To further investigate the mutual influence of both subcells, the top cell's EQE is measured whilst the bottom cell is illuminated by an IR LED ($\lambda > 850$). Since this leads to additional photogeneration of minority charge carriers in the bottom cell only, it allows for evaluating whether electrons generated in the top cell are affected by a changing density of holes in the c-Si wafer (i.e. potential recombination partners) whose density is orders of magnitude higher under bias illumination than in the dark. Fortunately, no profound alteration of the

top cell's EQE is observed, proving again that its performance is only marginally impacted by the addition of an entire wafer in an IBC 3T configuration. It is worth noting that these measurements are conducted for one subcell while the third terminal is kept floating (i.e. the respective other subcell is held at V_{oc} conditions). This simplification is permitted because the j_{sc}, which is extracted here, is found to be largely independent of the bias voltage applied to the respective other subcell (cf. Figure 5.7a and b).

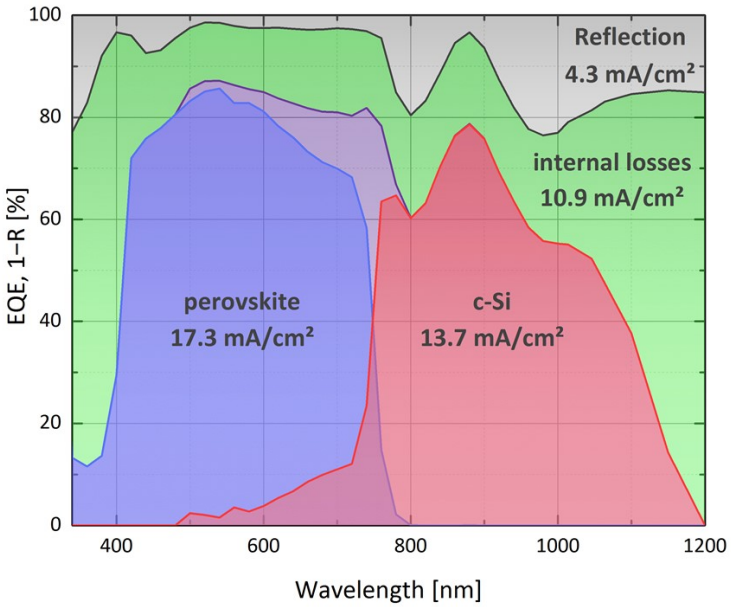


Figure 5.8: External quantum efficiency and reflection measurements of the best IBC 3T solar cell fabricated over the course of this thesis. Both subcells contribute to the photogenerated current in their respective range of the spectrum, and EQE-integrated short-circuit current densities agree well (for the top cell very well) with those measured under one-sun illumination. Severe parasitic absorption in contact and hole transporting layer as well as thin-film interferences along with reflection losses render further improvements necessary.

Combining EQE and reflection measurements (details for the latter are given in section 3.4.7) illustrates a quite severe current loss at the front side of 4.3 mA/cm², which can be ascribed to flat interfaces within the device and, related to this, thin-film interferences, which are clearly visible (e.g. at 800 nm) and have a considerable share in the total current loss. However, the biggest contributor to the latter is, by all means, parasitic absorption at the front side and within the bulk of the device with a total amount of 10.9 mA/cm². A large portion thereof, especially in the wavelength range below 400 nm, can be attributed to the strongly absorptive doped Spiro-OMeTAD (the perovskite's HTL) and front-side IZO [235]. Apart from that, MoO_3 causes a broadband absorption in the entire relevant wavelength range: since the MoO_3 serves as a buffer layer for preventing sputter damage of the

perovskite's HTL and absorber, it is uncovered during the sputtering process. It can thereby be chemically reduced, which causes the observed broadband absorption [236]. Within [165], optical simulation of actual and optimised IBC 3T tandem devices are conducted using the MATLAB-based programme GenPro, following the procedure given in [237,238]. For details, the reader is referred to said references. The j_{sc} values obtained from these optical simulations are utilised in the following section.

5.3 Equivalent Circuit Simulations of IBC 3T Tandem Solar Cells

To understand the experimentally observed mutual dependence of both subcells, electrical equivalent circuit simulations of IBC 3T tandem devices are conducted using LTspice (cf. section 3.5). To this end, two different cases are considered: i) an exact representation of the so far best experimentally realised IBC 3T tandem device, and ii) an optimised device comprising the best perovskite and IBC SHJ single-junction solar cells fabricated in-house.

5.3.1 Equivalent Circuit Simulation of the Best Experimentally Realised Cell

The electrical equivalent circuit, displayed in Figure 5.6, is used for electrical modelling of the device discussed here. It is based on one-diode models for each subcell and is similar to that presented by SANTBERGEN *et al.* [79].Diode characteristics (i.e. especially j_0 and the parasitic resistances R_s and R_{shunt}) are obtained by fitting one-diode models (equation (2.8)) to measured *j*–*V* characteristics (cf. Table 5.2). Fit and measured data agree very well barring a slight deviation around the MPP as exemplarily shown in Figure 5.9a for the realistic best device case, discussed in the following section. For the simulation, j_0 of both cells, the top cell's R_s and R_{shunt} as well as the bottom cell's R_{shunt} are taken as obtained from the fit. The ideality factors (*n*) of top and bottom cell are set to 1.5 and 1 respectively. Following the distribution proposed in PAVIET-SALOMON *et al.* [39], the R_s of the bottom cell is split into the ρ_c of the p-contact ($R_{s,bottom,p}$) and the combined resistance of n-contact and c-Si bulk (i.e. the resistance that is shared by both subcells, henceforth $R_{s,shared}$). An additional interconnection resistance (R_{IC}) is added in between both subcells, representing the interconnection layer stack as discussed in section 5.1.3. The impact of the R_{IC}, which marginally influences only the top cell's FF, is shown in Figure 5.9b where its numeric value is swept within a device-relevant range.

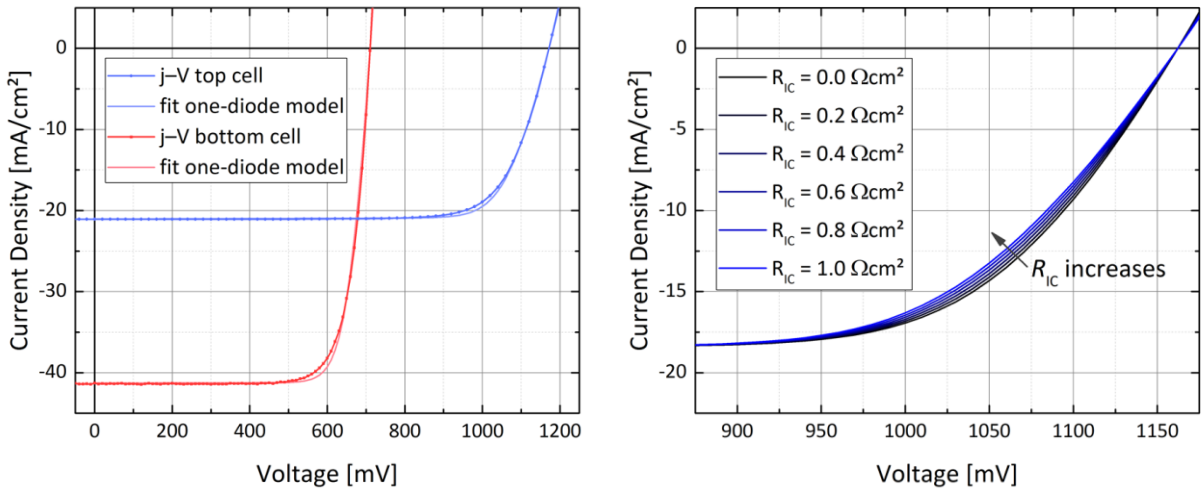


Figure 5.9: a) Measured illuminated one-sun current–voltage characteristics and best fits by one-diode models: only a slight deviation around the MPP is evident; b) modelled influence of the interconnection resistance (R_{IC}) on the top cell's j–V characteristics where mainly the FF is affected. Note that the abscissa starts at 875 mV.

Table 5.2: Diode characteristics, derived from fitting one-diode model equation to dark and illuminated j–V characteristics of actual devices, used for modelling different cases (as described here and in the next section) with LTspice.

Subcell	j_0 *[A/cm²]*	n [†] *[–]*	$R_{s,total}$ *[Ωcm²]*	$R_{s,shared}$ [‡] *[Ωcm²]*	R_{shunt} *[Ωcm²]*
Perovskite (experiment)	3.52×10^{-15}	1.5	7.6	N/A	438
IBC SHJ (experiment)	7.11×10^{-13}	1.0	3.0	1.1	981
Perovskite (optimised)	1.60×10^{-15}	1.5	3.4	N/A	6230
IBC SHJ (optimised)	4.88×10^{-14}	1.0	0.8	0.3	9582

[†] Note that for simplicity, an ideality factor of 1 is assumed for the IBC SHJ bottom cell, which (according to [239]) technically might not be accurate for the experimental cell as indicated by the slightly reduced minority carrier lifetime under low-injection conditions. However, this assumption only marginally influences the results of the resistance-dependent equivalent circuit modelling since neither j_0 nor n are directly used for subsequent calculations and the shape of the resulting illuminated *j–V* (used for extracting relevant solar cell parameters) is only slightly affected by this circumstance.

[‡] in accordance with the proposed distribution in [39]

Different operating points of the subcells are simulated by adjusting the current provided by the respective current source from 0 mA (V_{oc} conditions) to j_{sc} (j_{sc} conditions), covering thus the range between two device-relevant extrema. As in the experiment, one subcell is then swept in current whilst for the biasing subcell the voltage across its electrodes is obtained. Using this approach, it is possible to reproduce the performance reduction mainly caused by a drop in V_{oc} as also seen in actual devices (cf. Figure 5.10).

Interestingly, the likely origin of this effect could be pinpointed: the simulations show that it can be reproduced by increasing the shared portion of the bottom cell's series resistance, $R_{s,shared}$. This resistance consists of the lateral and vertical bulk-related R_s and the contact resistance governed by $\rho_{c,n,IBC}$. Indeed, the dependence of one cell's characteristics on the operating point of the respective other cell vanishes entirely when this resistance is set to zero. At this point, the two subcells become fully independent from each other, representing thus the ideal theoretical case as also discussed elsewhere [76].

Thus it can be concluded that during device fabrication utmost attention on designing this shared contact to be very lowly resistive as well as on choosing appropriate wafer material and thickness are crucial. The tunability of contact resistivities by means of material, layer properties, and geometry choices has been successfully shown for IBC SHJ single-junction solar cells in [35,50,240] and in chapters 4.2–4.5 of this thesis. Specifically, combined resistances of n-contact and wafer down to 0.47 Ωcm² [39] and even 0.32 Ωcm² for the total R_s [28] have been reported, which indicates that the $R_{s,shared}$ can be tuned to values well below the so far obtained 1.1 Ωcm² that are fit to the experimentally realised IBC 3T tandem solar cells presented here.

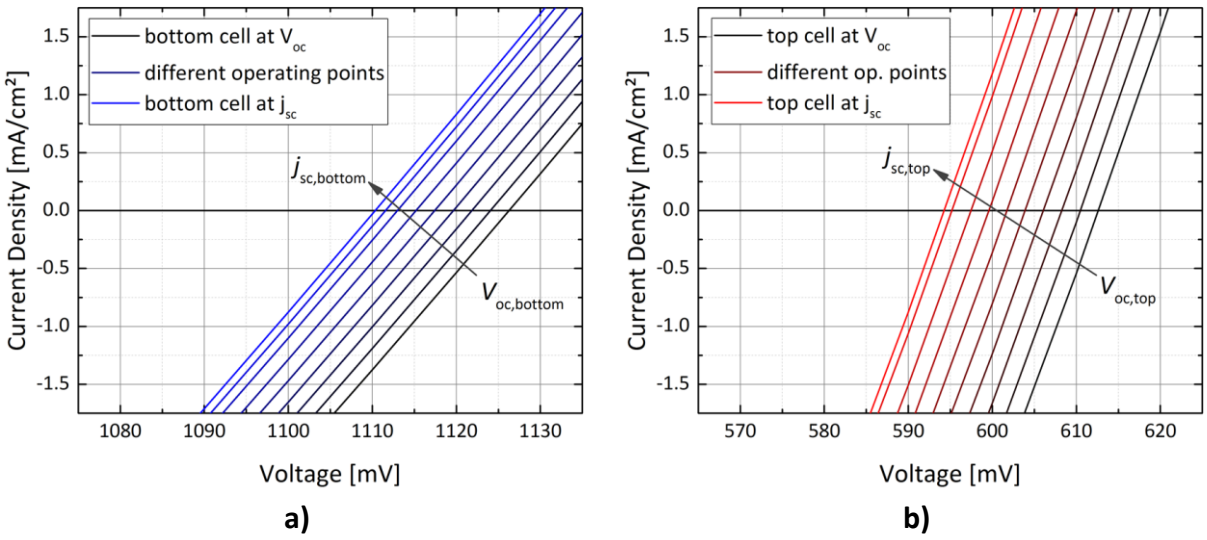


Figure 5.10: Modelled electrical behaviour in the vicinity of the open-circuit point for a) top and b) bottom cell whilst the respective other subcell is swept from V_{oc} to j_{sc} conditions. This behaviour is in good agreement with experimental results.

5.3.2 Equivalent Circuit Simulation of the Realistic Best Device Case

The realistic best device case is supposed to show a realistically feasible device performance utilising the same layers that are used in the here presented tandems. The single-junction device with optimised passivation layer thickness presented in section 4.3.4 serves as the bottom cell. For the top cell, an unpublished semi-transparent in-house record perovskite solar cell fabricated as described in section 5.1.2 is used. The electrical equivalent circuit parameters for both subcells are given in Table 5.2. Furthermore, the current densities of these single-junction devices are adjusted to an optimised current distribution as obtained by optical simulations utilising GenPro4 (as discussed above in section 5.2.2), with details shown in [165].

In the realistic best case, a combined PCE of 26.9% with both subcells operating at MPP is achieved using the discussed model (for fitting parameters of diode equations, cf. Table 5.2). Note that this value does not represent the overall PCE potential of IBC 3T tandem solar cells (for this, cf. section 5.4.2) and is mostly limited by the rather absorptive front contact layer stack, which is currently used in the fabrication process.

Further subcell characteristics are presented in Table 5.3. Adjusting the current density of the perovskite top cell can be practically realised by thinning its absorber. As less photons are now absorbed, the V_{oc} decreases slightly as well. An observed rise in FF can also be

explained by a decreased j_{sc} since this reduces the resistive power losses. For the bottom cell, principally the same considerations hold true. Additionally, losses in V_{oc} (30 mV) and j_{sc} (25.5 mA/cm²) are in good agreement with the findings of the Sentaurus TCAD simulations presented in section 5.1.3. Although now already surpassing the PCE achieved by the record IBC SHJ single-junction solar cell [30], still apparent drawbacks of the current device design are indicated by a combined current density of merely 35.3 mA/cm², which is primarily limited by strongly absorptive front-side layers (HTL and IZO) and a lack of front-side texturing. A more in-depth discussion concerning measures to circumvent these issues is conducted in the next section.

Table 5.3: Measured (single junction) and modelled (3T tandem) solar cell parameters of subcells in the optimised device case.

Subcell	V_{oc} *[mV]*	j_{sc} *[mA/cm²]*	*FF [%]*	*PCE [%]*
Perovskite (single junction)	1172	21.1	77.4	19.2
IBC SHJ (single junction)	710	41.3	78.2	22.9
Perovskite (3T tandem)	1164	19.5	79.2	18.0
IBC SHJ (3T tandem)	680	15.8	83.0	8.9
			Σ_{3T}	**26.9**

In a next step, the influence of both $R_{s,shared}$ and R_{IC} (i.e. the resistances governing the mutual dependence of both subcells) on the PCE of each subcell is investigated in more detail for the best device case parameter set. The results are depicted in Figure 5.11a–c. As discussed above, R_{IC} mostly affects the top cell's FF (cf. Figure 5.12b and d) and consequently (for a specific $R_{s,shared}$) its PCE: both decrease with increased R_{IC} (Figure 5.11a). Interestingly though, $R_{s,shared}$ has an overall larger impact on the top cell's performance than R_{IC} due to a significant drop in V_{oc} by up to 45 mV within the chosen simulated resistance range cf. Figure 5.12a). This drop in V_{oc} does not occur for a fixed $R_{s,shared}$ and gradually increased R_{IC}. When investigating the influence of these resistances on the bottom cell (Figure 5.11b and Figure 5.12c and d), it becomes evident that its PCE decreases linearly with increasing $R_{s,shared}$, but apparently R_{IC} does not seem to have any impact at all. This is, however, only

true for properly functioning devices. If R_{IC} is set to values in the order of kiloohms (Figure 5.11c), representing the case of faulty interconnection with otherwise intact subcells, the bottom cell's PCE increases considerably with an increased R_{IC}, which is mainly driven by a gain in V_{oc} and (to a lesser extent) in FF as no current is injected by the top cell. This effect is even more pronounced the larger $R_{s,shared}$ gets because in this case both subcells become less independent. Although the bottom cell clearly benefits from a large R_{IC}, this is, of course, not beneficial for the overall tandem performance where low values for both $R_{s,shared}$ and R_{IC} are required.

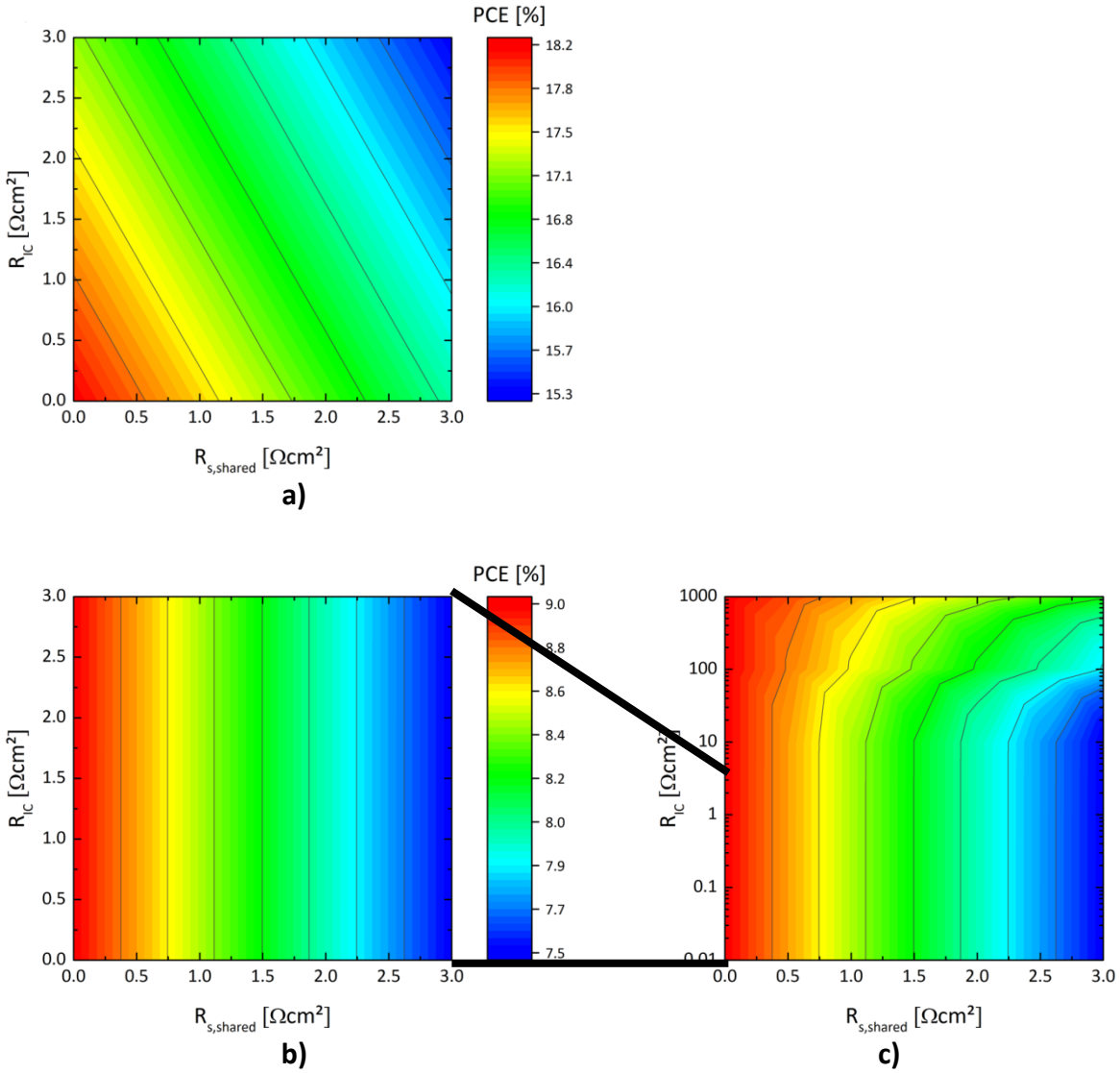


Figure 5.11: Simulated influence of interconnection resistance (R_{IC}) and shared portion of the bottom cell's series resistance ($R_{s,shared}$) on the PCE of a) top cell and b), c) bottom cell where in c) high R_{IC} values, representing a malfunctioning interconnection with otherwise intact subcells are simulated. Note that Figures b) and c) share the same PCE colour scale and all Figures share the same abscissa range.

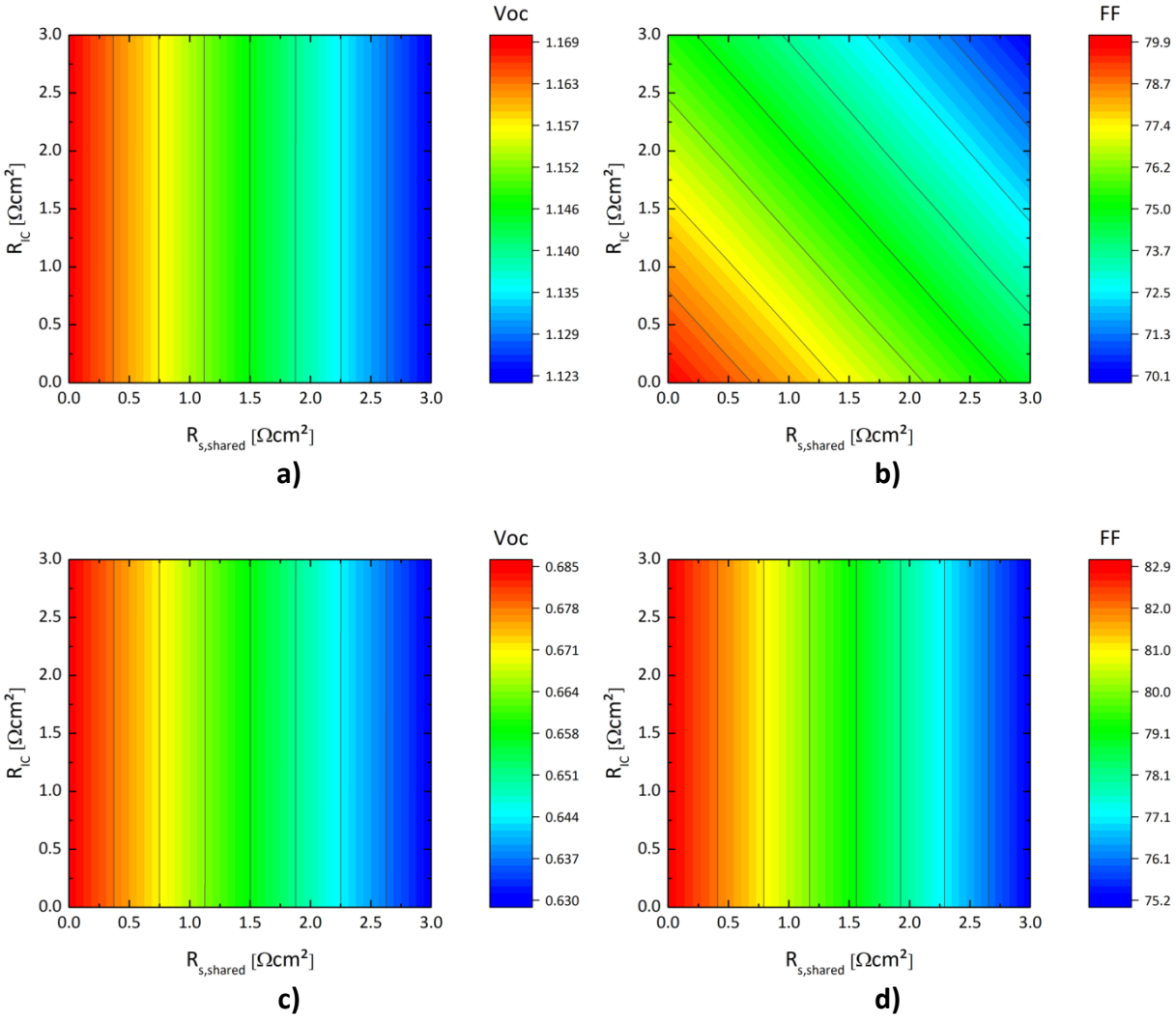


Figure 5.12: Simulated influence of interconnection resistance (R_{IC}) and shared portion of the bottom cell's series resistance ($R_{s,shared}$) on the V_{oc} of a) top cell and c) bottom cell as well as on the FF of b) top cell and d) bottom cell.

5.4 Optimisation Routes and Efficiency Potential

In the previous sections, the first experimentally realised IBC 3T tandem solar cells comprising perovskite and c-Si subcells have been demonstrated. In their current state, these devices are, however, far from being optimised, lacking behind their 2T and 4T counterparts with respect to device performances. Therefore, a discussion of optimisation routes for the here proposed tandem design is undertaken and an assessment of an efficiency potential is attempted in this section.

5.4.1 Optimisation Routes of the Current Design

Limitations in the current non-optimised proof-of-concept devices arise mainly from i) optical losses due to parasitic absorption in the front-side and interconnection layer stacks; ii) resistive losses stemming from a high lumped $R_{s,shared}$; and iii) recombination losses in the bottom cell, induced by the formation of a dark parasitic diode due to size-mismatch of both subcells as discussed in section 5.2.1. As demonstrated in section 5.3.2 and presented in literature for 2T 4T tandem devices [241,242], especially optical properties and thereby the j_{sc}s of each subcell need to be improved.

Apart from obvious enhancement procedures, such as adapting the thicknesses of involved layers as conducted e.g. in [69,162], there is a plethora of possible optimisation routes that will be discussed in the following, organised as in the initially introduced categories. Doped Spiro-OMeTAD, which is used as the HTL at the device's front side, is responsible for parasitic absorption in the wavelength region below 400 nm as becomes evident from Figure 5.8, presented in section 5.2.2. The relatively large thickness of 110 nm exacerbates this circumstance even further. Utilising a similar top cell layer stack in a 2T approach, Wu *et al.* have shown that Spiro-OMeTAD accounts for over one third of the total current loss, and together with IZO, MoO_3, and the interfacial ITO already 75% are lost [243]. Replacing these highly absorptive layers, particularly Spiro-OMeTAD and MoO_3, which have been shown to be accountable for almost 50% of the total current loss in a similar top cell layer stack, with more transparent ones, is therefore highly desirable.

To this end, other HTL materials have been investigated, such as poly(triaryl amine) (PTAA), which in terms of transparency is superior to Spiro-OMeTAD [244–246] and has been successfully integrated into a 4T tandem device, yielding a remarkable PCE of 26.4% [65]. Another promising candidate in this matter is copper thiocyanate (CuSCN), which features even better optical properties than PTAA and Spiro-OMeTAD [246,247], and single-junction perovskite solar cells utilising this material have been presented yielding a PCE of slightly above 20% [248].

As a substitute for MoO_3, vanadium oxide (VO_x) has been reported to be more robust against sputtering since it is not reduced upon sputtering and, consequently, no broadband absorption occurs [249].

Another possibility of mitigating parasitic absorption in the HTL is using an inverse architecture with the ETL facing towards the front side. Indeed, a profound increase in EQE (especially in the short-wavelength response) and therefore in j_{sc} can be achieved [66,69]. However, this entails certain intricacies regarding subcell interconnection and electrical properties. For one, either a tunnel-junction in between subcells is required [75,77] or the bottom cell has to be based on a p-type wafer. The latter suffer inherently from reduced minority charge carrier lifetimes in the low-injection regime [153,154], which is problematic especially when integrated into a real-world application with inconsistent weather conditions. In any case, the inverse top cell architecture with the top cell's ETL at the front side requires that the IBC's p-contact is now shared, which, as has been shown in [200] as well as in chapters 4.3.3 and 4.5.1 of this thesis, usually features a very high ρ_c of several 100 mΩcm². This circumstance is irreconcilable with requirement of $R_{s,shared}$ being as small as possible. Replacing the HTL with more transparent materials might therefore be a more feasible optimisation pathway than the implementation of an inverse top cell stack.

Another way of enhancing the devices' optical properties is the introduction of a textured front side. Not only does the j_{sc} rise substantially due to reduced front-side reflection and a higher absorption probability owing to light scattering and thus longer internal light passes [241,242], but thin-film interferences are thereby mitigated as well [162,241]. As discussed earlier, spincoating uniform layers onto textured substrates is at least challenging. An easy solution to circumvent this issue is the application of a transparent textured foil onto the device's front side. The successful implementation of such a foil has been presented for a 2T tandem device where its overall PCE is enhanced by more than $3\%_{abs}$ (from 23.4% to 26.5%), mainly driven by an increase in j_{sc} and suppressed thin-film interferences [162].

Using thinner wafers is an effective mean for increasing the bottom cell's V_{oc} [17,250]. Even though a reduced wafer thickness will eventually also decrease the j_{sc}, this effect is rather marginal when going from 280 µm (as used here) to e.g. 150 µm (cf. also section 6.1.1). Therefore, the PCE of moderately thinned wafers is enhanced, which, in turn, is beneficial for the overall device performance. Concomitantly, the vertical bulk-related R_s is linearly reduced with the wafer thickness, which causes a slight increase in FF.

Lastly, redesigning either subcell is required to account for size-mismatch. Increasing the top cell's area is likely to entail the necessity of a front grid (for achieving decent FFs). Adapting the bottom cell's design demands the (costly) fabrication of new photolithography masks. Therefore, further investigation in the shadow-mask process with the aim of achieving reliably reproducible results on a scale comparable to the photolithography process could yield a lean and easily adaptable fabrication process for bottom cells. Swapping the polarity of the outer IBC fingers could also help mitigating the decrease in FF since the BSF is more robust against the reduction of active contact area than the emitter [193].

5.4.2 Limiting Efficiency of IBC 3T Tandem Solar Cells

Section 5.3.2 gave a glimpse of what could be achieved with an optimised device and the current architecture. This is, however, not the real efficiency potential of IBC 3T tandem solar cells and in order to obtain that, a more fundamental procedure is necessary. To this end, a semi-empirical efficiency model, introduced by REYNOLDS AND SMIRNOV for 2T and 4T tandem solar cells [251], is applied to the 3T approach and compared with its competing interconnection concepts. Here, various modelled solar spectra are used to calculate the j_{sc} of both subcells for different realistic illumination conditions. To simulate their impact, the AM1.5g standard spectrum is altered to emphasise either its blue or red portion (i.e. benefitting either top or bottom cell). The resulting spectra, presented in Figure 5.13a, are considered to be a fair representation of realistic illumination conditions.

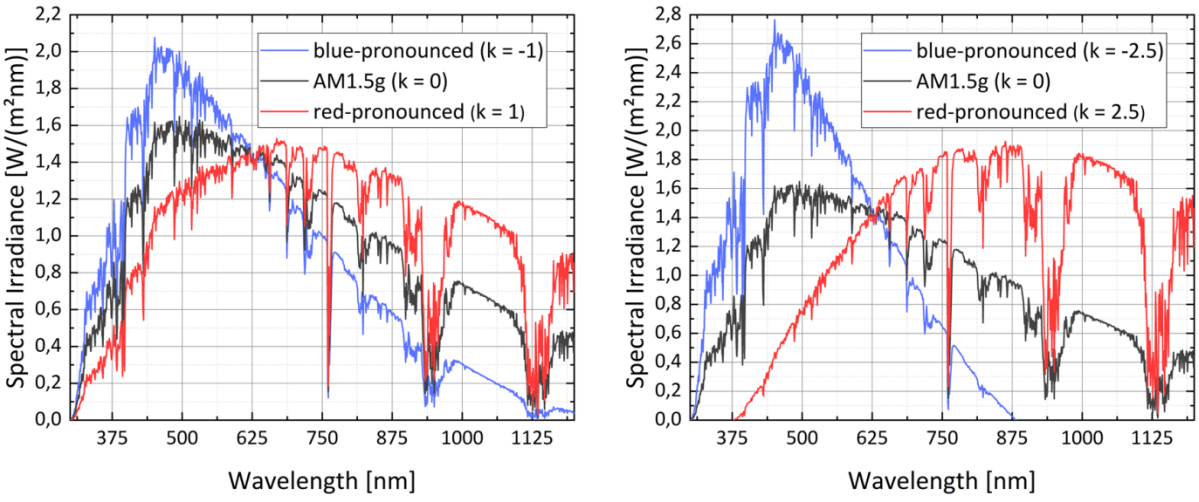


Figure 5.13: a) Tilted spectra for simulating different illumination conditions; b) too strong tilting leads to unrealistic results and therefore the model can only be applied to slight alterations of the AM1.5g standard spectrum.

The average photon energy (APE) for each spectrum is calculated by using equation (5.1) where Φ_{ph} is the photon flux (as defined by equation (5.2)), and λ_1 and λ_2 the integration limits, which are set to 300 nm and 1200 nm respectively.

$$APE = \frac{\int_{\lambda_1}^{\lambda_2} E(\lambda)d\lambda}{\int_{\lambda_1}^{\lambda_2} \Phi(\lambda)d\lambda} \tag{5.1}$$

$$\Phi(\lambda) = \frac{E(\lambda)}{h \cdot c/\lambda} \tag{5.2}$$

The AM1.5g standard spectrum is found to have an APE of 1.84 eV within the chosen integration limits. The abovementioned spectral tilting is conducted by applying equation (5.3) in combination with equations (5.4) and (5.5) [251].

$$F(\lambda, k) = \frac{G(\lambda, k)}{G_0(k)} \tag{5.3}$$

$$G(\lambda, k) = 1 + \frac{k \cdot (\lambda - \lambda_0)}{\lambda_0} \tag{5.4}$$

$$G_0(k) = \frac{\int_{\lambda_1}^{\lambda_2} G(\lambda, k) \cdot E_{\mathrm{AM1.5g}}(\lambda)d\lambda}{\int_{\lambda_1}^{\lambda_2} E_{\mathrm{AM1.5g}}(\lambda)d\lambda} \tag{5.5}$$

Here, F is the tilting function, G defines the deviation for every given λ from AM1.5g and G_0 the overall change in APE. Additionally, the numerator of equations (5.5) gives the altered spectra depicted in Figure 5.13a. The tilting wavelength (i.e. the spectral pivot), λ_0, is chosen to be 630 nm, in accordance with [251]. The factor k defines the amount of tilting at λ_0; k equal 0 corresponds to the AM1.5g spectrum, with F, G, and G_0 equal 1. It must be noted that this model can only be applied to spectra close to AM1.5g because too large deviations (i.e. very high or low k) lead to unrealistic results as can be seen in Figure 5.13b. Therefore, a scope of k = ±1.0 is chosen.

In a next step, EQE data of a well-functioning perovskite/c-Si 2T tandem solar cell taken from [162] is adapted according to the requirements of every interconnection scheme (2T, 3T, and 4T) and used to calculate the j_{sc} of each subcell. Therefore, the EQE data is multiplied with a factor to linearly increase or decrease in the wavelength region from 500–800 nm (cf. Appendix 9.2). This is done until either current matching is achieved (for 2T) or (for 3T and 4T) the combined PCE becomes maximal due to an optimal current distribution of the subcells, which (in agreement with literature [67,252,253]) usually requires higher top than bottom cell currents. In reality, this would be done by adjusting the top cell's absorber thickness. For the 4T case, an additional 250–300 nm [65,67,252] thick ITO in between subcells necessary for lateral current transport [75] is assumed, which slightly reduces the low-wavelength response (500–800 nm) of the bottom cell by the absorption of ITO in that wavelength range. The APE-dependent j_{sc} for each interconnection scheme and subcell is then calculated using equation (5.6) [251].

$$j_{\mathrm{sc}}(k) = q \cdot \int_{\lambda_1}^{\lambda_2} F(\lambda, k) \cdot \Phi_{\mathrm{AM1.5g}}(\lambda) \cdot EQE(\lambda) d\lambda \tag{5.6}$$

To obtain the remaining solar cell parameters, namely V_{oc}, FF, and ultimately PCE, assumptions about each particular subcell have to be made. Regarding the top cell, data of the optimised device case, presented in Table 5.2 and section 5.3.2, is used. The bottom cell, in turn, comprises the record IBC SHJ solar cell of [28] since it represents an almost ideal device and all parameters necessary for its modelling (i.e. j_0, n, and R_s; R_{shunt} is assumed to be 10 kΩcm²) are given within the reference. LTspice and one-diode models (1DMs) are then used to simulate the behaviour of each configuration under different APEs and thus subcell j_{sc} contributions.

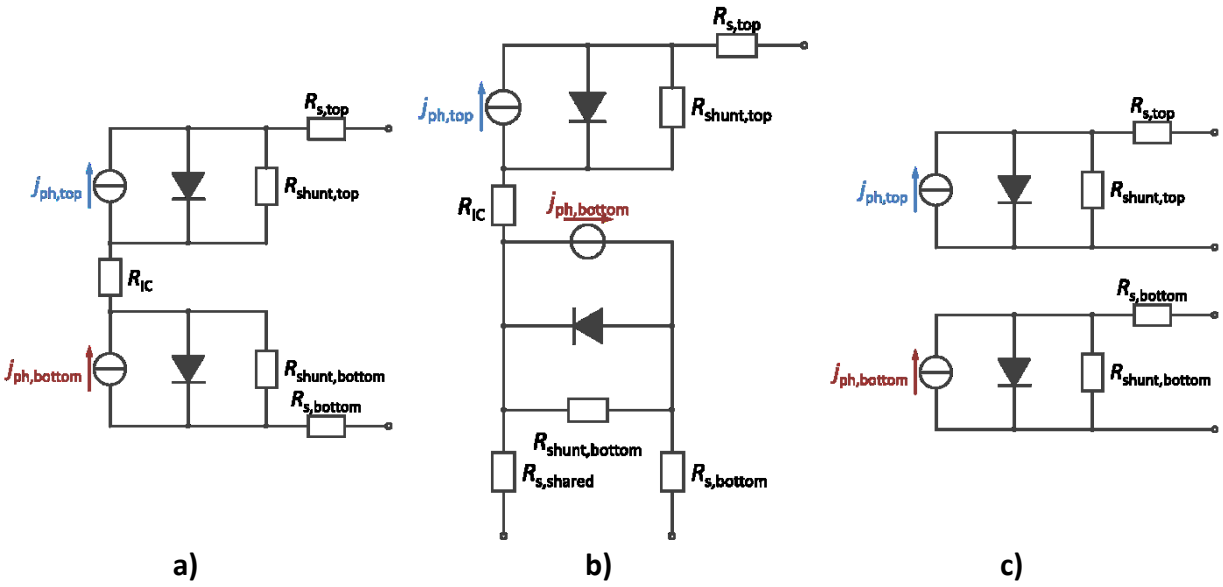


Figure 5.14: Electrical equivalent circuits of a) the 2T, b) the IBC 3T, and c) the 4T configuration used here for modelling the performance of each approach.

The electrical equivalent circuits of all three interconnection schemes used for modelling are depicted in Figure 5.14. Note that for the 3T case, this was already shown in section 5.2.1, Figure 5.6; and the 4T case simply comprises regular 1DMs of two separate solar cells as introduced in section 2.2.3, Figure 2.9a. For convenience, all three electrical equivalent circuits are depicted here again. 2T and 3T configuration feature an R_{IC} of 0.3 Ωcm²; and the $R_{s,shared}$ in the 3T case is, again, chosen in accordance with the proposed distribution in [39] (here: 0.12 Ωcm²). The resulting dependence of PCE (extracted from the simulated *j*–*V* characteristics) and APE is shown in Figure 5.15.

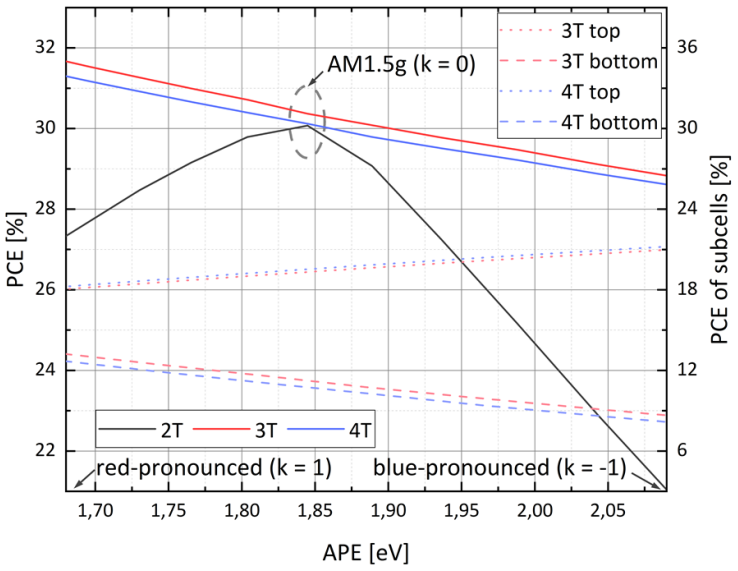


Figure 5.15: Resulting limiting efficiencies of the investigated tandem approaches (2T: black, IBC 3T: red, and 4T: blue) for different average photon energies (i.e. different spectra as presented in Figure 5.13a) under the chosen conditions. Additionally, PCEs of top (dotted) and bottom cells (dashed) are shown for 3T (light red) and 4T (light blue).

Interestingly, the limiting efficiency (within the chosen boundary conditions) of all three interconnection schemes only differs marginally for an APE of 1.84 (i.e. AM1.5g conditions) and is found to be slightly above 30% in each case. As for the 2T configuration, the PCE declines with both larger and smaller APEs than 1.84 because now the subcells are no longer current matched. This is, however, slightly counterbalanced by an increase in FF, which has been also demonstrated by others, both experimentally and in simulations [66,251]. The 3T and 4T configuration, in turn, behave quite similarly with the latter achieving slightly lower PCEs owing to higher parasitic absorption in the interconnection ITO layer (cf. above). Their FFs are almost independent of the APE. However, a slight decrease with increasing APE (i.e. a more blue-pronounced spectrum) is found for the top cell, which is likely due to higher j_{sc}s and thus resistive power losses under the given conditions. The bottom cell, on the other hand, is more robust in this regard: no noticeable variation in FF is observed when the APE changes. Maximum PCEs (under AM1.5g condition) of 30.1%, 30.4%, and 30.1% are found for 2T, 3T, and 4T configuration, all of them thus exceeding the record PCE of a single-junction c-Si solar cell of 26.7% [28,30] and even the reassessed theoretical efficiency limit of such a device of 29.4% [17].

5.5 Summary of Chapter

Here, the first experimental realisation of a three-terminal tandem solar cell with an interdigitated back-contact (IBC 3T) comprising a perovskite top and an IBC SHJ bottom cell is demonstrated. These devices have been developed in cooperation with a fellow PhD candidate, Philipp Tockhorn, who is responsible for the perovskite fabrication development. The 3T concept combines advantages of the more common two and four-terminal (2T and 4T) tandem approaches (i.e. having a monolithic device that does not require current matched subcells) without suffering from their respective drawbacks. Albeit far from being optimised, yielding a combined power conversion efficiency (PCE) of so far merely 17.1% when both subcells simultaneously operate at their respective maximum-power point (MPP), first results are promising and yet apparent constraints could be pinpointed by a combination of in-depth optoelectronic analysis and equivalent electrical circuit simulations.

Most limitations can be ascribed to the current device design and are not inherent to the 3T concept. Those are in particular (i) the lack of a well-functioning light in-coupling and the presence of thin-film interferences due to both a flat front surface and interconnection interfaces; (ii) severe parasitic absorption within interconnection layers; (iii) size mismatch of both subcells and thereby shading of the IBC bottom cell's outer fingers of the minority charge carrier contact area, which leads to additional recombination (decrease in open-circuit voltage, V_{oc}) and fill factor (FF) losses in the bottom cell; and (iv) high resistive losses in the shared electron contact ($R_{s,shared}$). The resistance of this shared contact is found to be the reason for an observed slight mutual dependence of both subcells. Here, mainly the V_{oc} of one subcell is affected by the other subcell's operating point while the short-circuit current density (j_{sc}) remains practically unchanged. This effect is more pronounced for the bottom cell and vanishes entirely if $R_{s,shared}$ is set to zero in the simulation, making thus both subcells truly independent of each other. Note that this is just a theoretical consideration as $R_{s,shared}$ can never actually be zero. A crucial design criterion of IBC 3T tandem solar cell is therefore to choose thin, lowly resistive bottom cell wafers and a shared contact scheme featuring a low specific contact resistivity (ρ_c).

With that said, it might be, albeit optically more favourable, from an electrical point of view not advantageous to realise the top cell with an inverse layer stack (i.e. with the electron transporting layer at the front side) because this entails that the p-contact is shared. This

contact usually features much higher ρ_cs than its n-type counterpart (at least with commonly used layer stacks; as has been discussed earlier throughout this thesis and in literature [200]) and will therefore result in a strong mutual dependence of both subcells.

By using equivalent electrical circuit simulations and one-diode models, it is possible to reproduce the observed electrical behaviour of the investigated devices and to estimate the impact of possible optimisation routes. Lastly, combining these simulations with a semi-empirical model [251], it is possible to estimate a realistic efficiency potential and the behaviour of each interconnection scheme (i.e. 2T, 3T, and 4T) under illumination conditions different from the AM1.5g standard spectrum. It is assumed that 2T and 3T require a subcell interconnection layer stack, which is realised as an interconnection resistance. For 4T, a thick layer of indium tin oxide (ITO) is implemented, which is necessary for lateral current transport. This layer affects the bottom cell optically due to parasitic absorption in ITO in the wavelength regime of 500–800 nm. As a result, 3T and 4T both exhibit an almost linear increase in PCE for spectral conditions that favour higher currents in the bottom cell (i.e. red-pronounced spectra). The PCE of the 2T concept, in turn, declines rapidly for spectral conditions different from AM1.5g due to current mismatch of its subcells. This effect is, however, partly mitigated by an FF increases in this case. All three approaches yield high PCEs of 30.1%, 30.4%, and 30.1% (for 2T, 3T, and 4T configuration) under AM1.5g and thereby exceed the reassessed theoretical efficiency limit of a single-junction silicon solar cell of 29.4% [17].

6 Prospects of IBC SHJ Solar Cells

PV is one of the fastest growing renewable energies and allows for competitive power generation [5,6]. However, continuing the success of PV requires further cost reduction, which can be achieved by decreasing material consumption, replacing costly components and processes with more cost-effective ones, or increasing device efficiencies. Well-designed IBC SHJ solar cells easily fit into the latter category but usually suffer from increased fabrication complexity, which is the main obstacle for their broad market introduction. Developing a simplified and industrially compatible fabrication processes while maintaining exceptional cell properties must therefore be amongst the main objectives in any research dealing with this promising technology. In this chapter, a perspective regarding the future development of IBC SHJ solar cells, both as single-junction and part of tandem devices, is given. Furthermore, a comparison with other high-efficiency concepts, in particular standard and dopant-free SHJ devices, the industry standard [254] PERC (and its derivates), and so-called POLO (poly-silicon on oxide) IBC solar cells [255], is conducted. Lastly, other patterning techniques used in IBC SHJ solar cells presented in literature, different from those carried out in this thesis are discussed.

6.1 Comparison of IBC SHJ with Other High-Efficiency Concepts

In this subsection, single-junction IBC SHJ solar cells are compared to other successful Si wafer-based technologies with respect to fabrication complexity and achieved device performance.

6.1.1 Standard SHJ Solar Cells

Standard SHJ solar cells are very likely the main competitor to their IBC counterparts (further details along with illustrations of the respective technologies are given in sections 2.2.4 and 2.2.5). The former feature a straightforward and potentially cost-effective [6] fabrication route by using techniques stemming from thin-film PV industry [19,256] and yielding with 750 mV [21] the highest reported V_{oc} of all c-Si-based technologies. IBC SHJ solar cells on the other hand excel regarding unparalleled PCEs of up to 26.7% [28,30], but require additional

patterning steps for contact separation of their rear-side electrodes, which comes at the cost of increased manufacturing complexity.

When comparing the PCE of the best reported solar cells of both technologies [20,28,30], rear-contacted devices lead by only 1.6%$_{abs}$ and therefore their fabrication can only be marginally more complex for the benefit of having a slightly higher PCE to pay off. This is further exacerbated when considering more industrially relevant scenarios where the possibility of mass production is more relevant than achieving the highest possible PCE. Here, the difference of both technologies is even smaller, with IBC SHJ solar cells leading by less than 1%$_{abs}$ [6]. It becomes thus apparent that developing a lean, industrially viable fabrication process for IBC SHJ solar cells that does not considerably exceed the complexity of that of standard SHJ solar cells, is the most crucial task to be tackled here. It must further be stressed that this challenge will very likely not be overcome by a process involving photolithography or, more generally, by any process that relies on tedious non-self-aligning patterning procedures. This will be discussed in more detail in section 6.2.

In the following, IBC SHJ solar cells processed in this thesis will be compared to their front/back contacted counterparts, fabricated with similar a-Si:H and nc-Si:H layers using the same PECVD cluster tool (AKT1600; cf. section 3.1.1). For this, both a single and a multilayer passivation scheme (cf. sections 4.3.4 and 4.4.2) are used. There is, however, a profound caveat that prohibits a direct data comparison and that is an appreciable difference in wafer thickness, W (280 µm thick FZ wafers in this thesis; 125 µm Cz wafers used for standard SHJ solar cells), which mainly affects the V_{oc} [17]. The latter can be expressed as a function of wafer thickness (W) and effective minority charge carrier lifetime (τ_{eff}) as given in equation (6.1) [181].

$$V_{oc} = \frac{k \cdot T}{q} \cdot \left[\ln\left(\frac{j_{ph}}{W}\right) + \ln(n_0) + \ln(\tau_{eff}) \right] - \frac{k \cdot T}{q} \cdot \ln\left(q \cdot n_{i,eff}^2\right) \qquad (6.1)$$

Here, n_0 is the equilibrium densities of electrons and amounts to approximately 1.55×10^{15} cm^{-3} (corresponding to a specific wafer resistivity, ρ_{bulk}, of 3 Ωcm) for the given doping concentration of the used wafers. The effective intrinsic charge carrier density ($n_{i,eff}$) is about 10^{10} cm^{-3} in c-Si [100]). The effective minority charge carrier lifetime is set to 3 ms and 5 ms for the single and multilayer passivation scheme respectively, in accordance to the findings of section 4.4.1. Furthermore, k, T, and q denote the Boltzmann constant, absolute

temperature, and elementary charge respectively. Using a thinner wafer inevitably entails a slight reduction in j_{sc} since less light is absorbed, which especially holds true for near-IR photons [250]. This loss is estimated on the basis of literature data [17,146,250] to be 0.8 mA/cm². The resulting ΔV_{oc} (derived from equation (6.1)) is about 20 mV for both cases (single and multilayer passivation), which, again, agrees well with literature cited above. The adapted V_{oc} is then calculated by substracting ΔV_{oc} from the measured V_{oc}. In Table 6.1, the solar cell parameters of both concepts and passivation schemes are summarised.

Table 6.1: Summary of solar cell parameters of IBC and (adapted) standard SHJ solar cells with comparable layer stacks.

Solar cell type	*Passivation scheme*	V_{oc} *[mV]*	j_{sc} *[mA/cm²]*	*FF [%]*	*PCE [%]*
IBC SHJ	Single layer	710	41.3	78.2	22.9
Standard SHJ	Single layer	728	39.2	80.2	22.9
Adapted standard SHJ†	Single layer	708	40.0	80.2	22.7
IBC SHJ	Multilayer	713	41.5	76.0	22.5
Standard SHJ	Multilayer	740	38.9	79.4	22.9
Adapted standard SHJ†	Multilayer	720	39.7	79.4	22.7

† V_{oc} and j_{sc} are adapted according to a wafer thickness of 280 µm (starting from 125 µm). For the sake of simplicity, it is assumed that the FF does not change.

For both concepts, the PCEs are on a similar level, with the IBC SHJ solar cell utilising an optimised single-layer passivation yielding the highest value. The same holds true when examining the adapted V_{oc}s (note that, albeit here only 713 mV are presented for the multilayer passivation, values as high as 723 mV are obtained on other solar cells with the same scheme). The main difference between standard and IBC SHJ solar cell is therefore a trade-off between j_{sc} and FF. With the j_{sc} being higher on IBC SHJ solar cell owing to the omission of a front grid and an optically optimised front side, and the FF being mainly impacted by a higher j_{sc} (higher resistive power losses due to a quadratic dependence of the current) and a reduced contact area, this trade-off can be qualitatively well explained and is also in line with the findings in [35]. There, it has been argued that the main difference in FF for standard and IBC SHJ solar cell stems from higher resistive losses in the latter due to

increased current densities through roughly half the contact area whereas shunt and recombination-related losses are in the same order of magnitude for both concepts.

Interestingly, when reducing the wafer thickness by roughly 55%, the PCE increases by merely 0.2%$_{abs}$ because the gain in V_{oc} of about 20 mV is almost fully counterbalanced by the concomitant reduction in j_{sc}. If the simplification made here of a fixed FF is replaced with its accurate behaviour (i.e. a slight increase with reduced W), the observed change in PCE would be likely even more insignificant. SHJ solar cells are known to feature a lower temperature coefficient than other c-Si-based technologies and therefore their annual energy yield is expected to be higher [6]. This reduction in PCE with increased temperature has been found to be even smaller for IBC SHJ solar cells on the basis of simulations [257]. There, it has been argued that this is due to a higher voltage temperature coefficient of standard SHJ solar cells. In this regard, although the advantage of rear-contacted over standard SHJ solar cells is very little under STC, it might become more pronounced in a real-world application.

6.1.2 Dopant-Free SHJ Solar Cells

In dopant-free silicon heterojunction (DASH) solar cells, doped a-Si:H or nc-Si:H layers are replaced with other materials, such as MoO_3 or PEDOT:PSS (poly (3,4-ethylenedioxythiophene):polystyrene) for the p-contact and LiF, titanium dioxide (TiO_2), magnesium oxide (MgO), or gallium nitride (GaN) for the n-contact [258–263]. This allows for tailoring the energy landscape of each contact regarding a desired WF. With respect to achieving a high FF, the WF should be smaller than 4.05 eV or greater than 5.2 eV for forming a good electron or hole contact respectively [57]. The greater available variety of materials, possibly fulfilling this criterion, is one advantage of DASH over standard SHJ solar cells. Another is the potentially easy fabrication route that does not rely on photolithography (in case of IBC devices) but rather on industrially viable techniques, such as thermal evaporation and screen printing. However, although the hitherto best IBC DASH solar cells yield already PCEs exceeding 20% [260,261], obtaining well-passivated contacts that allow for decent charge carrier transport at the same time remains challenging. Nevertheless, PCEs of 24% have been predicted for (IBC) DASH solar cells [258,260,262].

6.1.3 PERC Solar Cells

The PERC solar cell and its derivates PERL and PERT (passivated emitter, rear totally diffused) are economically the currently most successful concept in Si wafer-based PV, having replaced the long running market leader technology, the Al BSF solar cell (a homojunction concept with full-area diffused Al rear-contact), as the technology with the highest manufacturing capacity in 2018 and a predicted market share of 70% by the end of the next decade (i.e. 2029) [254]. For comparison, a market share of about 10% is forecast for IBC SHJ solar cells at the same time, provided that simplified fabrication routes are developed [254]. In Figure 6.1, a schematic of a PERC solar cell is depicted.

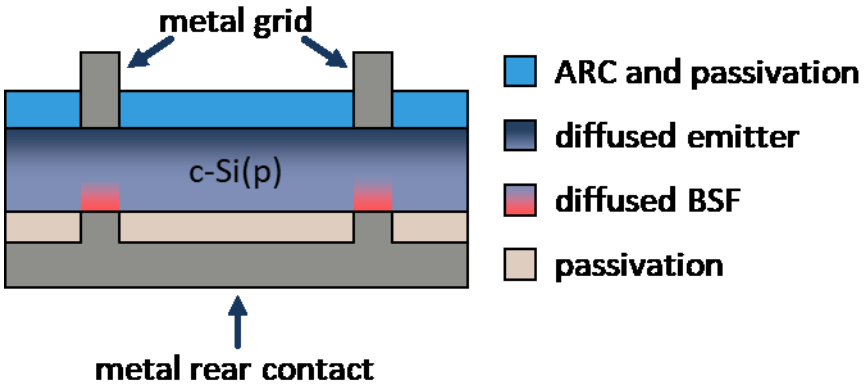


Figure 6.1: Schematic (not to scale) of a PERC solar cell. Reworked from [16]. Note that, for the sake of simplicity, the front side is depicted flat whereas in reality it is textured with random pyramids. The rear side of PERC solar cells is usually flat.

The PERC concept (in the following treated representative of all three abovementioned technologies) relies on passivated contacts with local openings for contact formation [264]. At the front side, a diffused emitter (n-type in this case since usually p-type wafers are used as base material) is coated with SiN_x, which serves as both anti-reflective coating (ARC) and field-effect passivation (FEP) layer [14], followed by a screen printed Ag grid. As a rear-side passivation layer, mostly aluminium oxide (AlO_x) is used owing to its strong negative fixed charge that sufficiently repels electrons and supresses recombination at the rear side [265]. Furthermore, chemical passivation is achieved by SiO_x that grows at the interface. The AlO_x layer is locally opened by laser ablation and then contacted by a screen printed sheet of Al. Both contacts (front and rear) are afterwards fired at high temperatures to form diffused contacts in the passivation openings at the rear and underneath Ag fingers at the front side. Restricting the highly recombination-active diffused Al contact to only a small portion of the

p-contact, and having the rest of it properly passivated, is sufficient to achieve both a high FF and a reasonably high V_{oc} at the same time [16].

When using this technology, a record PCE of 24.7% was achieved in 1999 and later corrected to 25.0% after reassessment of the AM1.5g standard spectrum in 2009 [266,267]; and industrialised PERC solar cells already yield PCEs exceeding 22% [16]. A huge advantage and part of their successful commercialisation is the fact that PERC solar cells are (except for PERT [268]) largely processed on p-type wafers, which are (due to being the standard wafer material in PV industry) generally easier available than their n-type counterparts [16,19,154,254]. Furthermore, when fabricating p-type material, the resistivity along the ingot is very uniform, which is not true for n-type Si [16]. Apart from that, phosphorous diffusion in homojunction solar cells (just as PERC) effectively renders impurities in p-type Si ineffective, thereby enabling the use of defect-richer but also more cost-effective bulk materials [16,19]. This combination of abundance, process control during ingot fabrication, and industrial predominance of p-type wafers are therefore significant commercial advantages over n-type Si. Using p-type wafers might, however, be a disadvantage when considered from a device performance point of view. Especially in Cz wafers a considerable amount of oxygen is present that reacts with boron under formation of boron-oxygen complexes upon illumination [269,270]. In addition, the charge carrier capture cross section of transition metal impurities in Si is much larger for electrons (i.e. minority charge carriers in p-type wafers) than for holes [271]. All this leads to inferior minority charge carrier lifetimes of p-type wafers, especially in the low-injection regime and therefore to a reduced FF as compared to n-type material [154,155,239]. Nevertheless, the applicability of p-type wafers has been successfully reported for SHJ solar cells as well, yielding a FF of 77.1% and a PCE of 21.4% [154]. Using this more cost-effective wafer material might therefore help increasing the competitiveness of SHJ (including IBC) cells against the PERC concept in an industrial context.

Apart from that, SHJ solar cells feature generally higher V_{oc}s of 750 mV [21] whereas the best PERC solar cells surpass 700 mV [266,267]. This is due an entirely passivated surface in the SHJ concept and local metal/semiconductor recombination sites in PERC solar cells. Owing to that and the fact that similar j_{sc} values (usually about 41–42 mA/cm² [27,28,73,266]) are achieved in both PERC and IBC SHJ solar cells, the power output of the latter is higher and their use is therefore beneficial in areas where space is rare and high power densities are essential.

6.1.4 Tunnel Oxide Solar Cells

A principal schematic of a tunnel oxide solar cell is shown in Figure 6.2.

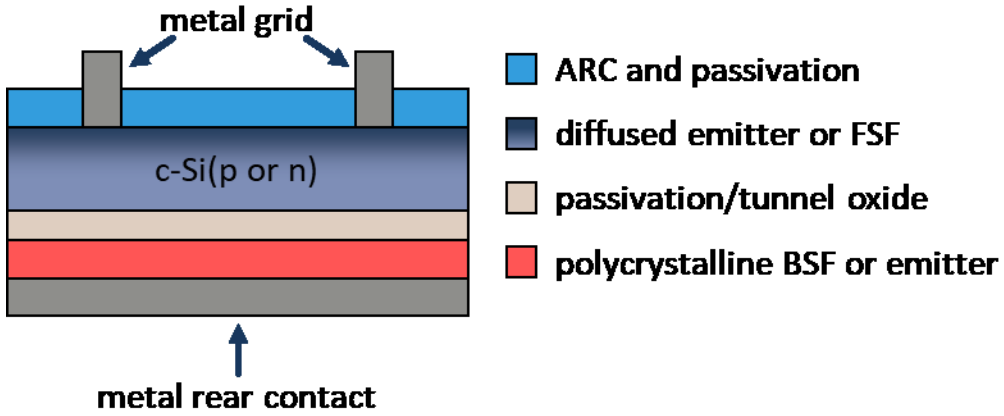


Figure 6.2: Schematic (not to scale) of a tunnel oxide solar cell. Reworked from [272]. FSF and BSF denote front and back-surface field respectively. Note that, for the sake of simplicity, the front side is depicted flat whereas in reality it is textured with random pyramids. The rear side of tunnel oxide solar cells is usually flat.

In the so-called TOPCon (tunnel oxide passivated contact) [272] or (similar to that) POLO concept [255,273], the rear side of an n or p-type wafer is passivated with a thin SiO_x layer. Its thickness determines the prevalent transport mechanism, namely tunnelling if the oxide layer is thinner than 1.5 nm, or charge carrier extraction through pinholes (for layers thicker than 2.2 nm) [274]. On top of the SiO_x, polycrystalline Si contacts are formed by depositing doped or intrinsic a-Si layers that are subsequently crystallised at high temperatures of 800–900 °C [16]. Additionally, a thermal oxide is thus formed on the poly-Si, which passivates its surface [275]. Similar to the PERC concept, laser ablation is then used to locally open the contact area, followed by a full-area deposition of Al or Ag. Although high PCEs of 25.7% and 26.1% for TOPCon and POLO IBC solar cells respectively have been reported [213,255], these technologies (especially the latter) make use of a very elaborate fabrication route that relies amongst other things on photolithography, ion implantation, and high-temperature processes [275]. It is therefore presently rather challenging to make these concepts feasible in an industrially context.

6.2 Prospects of Different Patterning Techniques

High efficiencies alone are no guarantee for a large market share of a solar cell technology, especially if a complex fabrication procedure is involved. It is therefore at least questionable whether photolithography-based IBC SHJ solar cells can be industrialised. In a research environment, however, photolithography can still serve as a benchmark process since it features maximum structural fidelity and therefore best solar cell results. Other patterning techniques for the fabrication of IBC SHJ solar cells both conducted within the framework of this thesis and presented in literature by other groups are introduced and discussed in the following.

6.2.1 Patterning Techniques Involving Shadow Masks

The idea of *in-situ* patterning by using shadow masks is almost as old as the concept of IBC SHJ solar cells itself. In 2007, a process combining deposition and plasma-etching through shadow masks has been introduced [32], significantly facilitating the procedure introduced shortly before by Lu *et al.* [24], but resulting in PCEs that are far from their present state. Nevertheless, it has been proven already in this very early state that the omission of photolithography for fabricating IBC SHJ solar cells is essentially possible. Over a decade of intensive research later, shadow-mask-based processes mark currently the apex of photolithography-free IBC SHJ solar cells in terms of both a lean process flow and device performances with a record PCE of 25% [40]. With that said, there is still work to be done to make these devices appealing to industrial manufacturers.

To start with, using two deposition masks (one for each polarity) is likely not feasible in an industrial context, despite achieved PCEs of up to 22% [36]. This includes the shadow-mask process discussed in this thesis and its preceding works [37,50,194,195,276] as well as some procedures described in literature [34–36]. One possibility towards a one-mask process is further developing the plasma-etching method introduced in [32] as discussed in greater detail in [31]. After full-area deposition of a-Si:H(i)/nc-Si:H(n), a shadow mask with openings for the desired a-Si:H(p) portions is attached to the wafer. No alignment is necessary since by now there is no predefined structure on the substrate. The exposed parts of the nc-Si:H(n) layer are afterwards etched back by using a H_2 plasma and, without detaching the mask or breaking the vacuum, a-Si:H(p) is afterwards selectively deposited through the same

mask. It must be noted that not the entire stack can be etched back because the H2 plasma would irrevocably alter the c-Si surface, which could either lead to unwanted results, such as epitaxial growth of the repassivation stack or necessitates an additional surface cleaning step [31,33]. Therefore, a buffer layer has to remain on the wafer's surface. It is very convenient that its required thickness happens to be in the typical order of magnitude of a-Si:H(i) layers used for passivation purposes in SHJ solar cells and that the applied hydrogen plasma treatment does not impair the passivation quality of the latter [31]. This technique is therefore applicable to the patterning of doped layers in IBC SHJ solar cells.

Another possibility, which led to the record device described above, was introduced in 2017 utilising a tunnel-junction approach [38–40]. The rear-side structuring is achieved as follows. Onto a c-Si(n) passivated with a-Si:H(i), nc-Si:H(n) is applied through a shadow mask by means of PECVD. Afterwards a-Si:H(p) is full-area deposited atop. The electron contact comprises thus of an n/p/n (the latter n being a TCO; cf. next paragraph) junction that needs to fulfil certain criteria to enable sufficient tunnelling. Those are (i) a low resistivity of the tunnel junction, (ii) good electron selectivity of the n-contact, and (iii) low lateral emitter conductivity to prevent shunting, which is achieved by high doping concentrations (for the first two requirements) and choosing the emitter's deposition conditions so that it grows in its amorphous or nanocrystalline phase on a-Si:H(i) and nc-Si:H(n) respectively [38]. If the full-area deposited minority charge carrier contact were fully nanocrystalline, its higher (as compared to amorphous material) lateral conductivity would not effectively prevent shunting. When considering industrial upscaling of this process (or any process involving shadow-masks), one of the main challenges is that a tight fit of wafer and mask over a large area (> 100 cm^2) has to be assured.

For contact formation of these tunnel-junction devices, at first, TCO and Ag were applied by means of PVD and afterwards patterned by inkjet printing a resist, followed by wet-chemical etching of the exposed area [34]. More recently, this has been adapted in favour of a leaner process involving screen printing an Ag grid that serves as an etching mask for a TCO [40]. In fact, the applicability of screen printing for IBC solar cells has been presented before [277].

Regarding the shadow-mask process presented in this thesis, a screen-printing based approach similar to that used in the tunnel-junction IBC devices [40] must eventually replace the currently used photolithography-like metallisation patterning in order to achieve

industrial viability. It must be noted that ITO cannot be used for this purpose because screen printed Ag paste has to be cured at temperatures of about 200 °C, which initialise the crystallisation of ITO and renders it thus non-corrodible by moderately concentrated HCl solutions. Etching crystalline ITO requires high HCl concentrations, longer etching durations, solutions with elevated temperature, stronger etchants, or a combination thereof. Although Ag can withstand HCl concentrations and etching durations necessary for structuring amorphous ITO, it will not endure etching solutions necessary for structuring its crystalline phase (as has been tested in corresponding experiments during the course of this thesis).

Aluminium-doped zinc oxide (AZO), can be used as an alternative to ITO [40,50,52,133]. However, a controlled structuring of AZO is challenging due to very fast etching reactions even at low HCl concentrations, which always led to strong undercutting (cf. section 4.1.1) and thus low FFs or even a complete lift-off of Ag fingers whenever this TCO has been applied over the course of this thesis. For the shadow-mask process reported here, AZO in combination with screen printing was only utilised once leading to very low FFs probably due to the penetration of HCl though pinholes in the screen printed Ag [276]. Despite these as of yet unsolved process-related issues, a better EQE response (as compared to ITO) in the near-IR part of the spectrum is found for AZO [58], which makes it a promising candidate for replacing ITO in the long term. This is furthermore a worthy consideration in the context of system cost reduction. The same holds true for using p-type wafers, which, although sacrificing performance, might help to further reduce the devices' fabrication costs and to facilitate the industrialisation of SHJ solar cells [278,279]. Additionally, it is necessary to replace Ag with more cost-effective metallisation schemes (e.g. Al as investigated in this thesis and in [34,59,60]) since it is (along with the wafer material) one of the main cost drivers within the SHJ technology [6].

6.2.2 Patterning Techniques Involving Laser Ablation

In the following section, IBC SHJ solar cells patterned solely or partly by means of laser ablation are examined. Please note that laser-doped homojunction IBC solar cells [280,281] are not discussed here. Laser ablation can be used to pattern either an etching mask (primarily comprising SiO_x) grown on a substrate in combination with subsequent wet-chemical etching [46,282–284] or directly intrinsic and doped a-Si:H layers [44,45,216]. A key issue of laser

patterning is an inevitable damaging of the c-Si surface, which makes usually wet-chemical treatment necessary and often results in low V_{oc}s and FFs for solely laser-patterned solar cells. Another possibility of circumventing laser damage is the application of an elaborate dielectric mask stack with gradually changing optical properties [46]. Such stack was reported to provide more sufficient screening than a single SiO_x mask as more of the incident laser power is reflected, which yields a more careful and thereby controlled ablation process. Owing to a thereby prevented laser-induced damage on the surface, the V_{oc} of such a device is now on a compatible level with other IBC SHJ solar cells and the remaining limiting factor is a low FF. The latter is discussed to not stem from the laser-patterning but from a rather high series resistance (R_s) as determined by SunsVoc measurements: the non-optimised a-Si:H(p)/ITO interface is held responsible for a high R_s in these devices. Nonetheless, a maximum PCE of 22.5% is achieved with this process [47]. A similar approach combining laser-patterning of a SiO_x hard mask and plasma etching (cf. previous section) yielded quite recently a PCE of 22.9% and a moderate FF of 75.4% [33].

In theory, laser ablation is a lean and industrially compatible patterning procedure that is used successfully in thin-film PV [41–43]. However, to ensure decent surface passivation, which is a central quality of the SHJ concept, rather elaborate auxiliary techniques and often a wet-chemical treatment must be applied. Additionally, obtaining high FFs is a yet to be tackled challenge for laser-patterned IBC SHJ solar cells.

6.3 Prospects of Perovskite/Silicon Tandem Solar Cells

In the following section, an overview over future perspectives of tandem devices comprising perovskite and SHJ subcells is given. This will focus on two considerations. First, combining two (or more) semiconductors enables utilising a greater fraction of the incident solar spectrum and thus potentially higher PCEs, but at the cost of an increased fabrication complexity as compared to a single-absorber device. Therefore, a gain in efficiency must be balanced with an increased fabrication costs of a multi-junction device. Second, light-induced degradation is an ongoing problem in perovskite solar cells that is as of yet not satisfactorily solved. In tandem devices, however, long-term stability is of importance since both subcells need to achieve a similar lifespan.

The evaluation of increased costs against gain in efficiency and annual yield of tandem and single-junction solar cells has been conducted in several studies already [160,161,285]. Interestingly, when comparing 2T and 4T devices regarding their manufacturing costs, no clear preference towards either interconnection scheme is apparent since the relatively lean fabrication of 2T is largely counterbalanced by an increased annual energy yield of 4T [285]. It must be mentioned, however, that this conclusion is the result of a certain set of assumptions (e.g. combining two solar cell technologies with similar PCEs and complementary band gaps) and depends critically on how the PV system and its specific costs are defined. Regarding the 3T tandem solar cells investigated here, it is assumed that their fabrication costs are also close to those of 2T devices because of a likewise monolithic device architecture. Therefore, here, the simplified assumption is made that the 2T case is representative of all three discussed interconnection schemes in terms of overall device fabrication costs. This should be a good first-order approximation, and thus in the following only the term 'tandem solar cells' is used.

Hitherto, with the remarkable exception of a 28% PCE tandem solar cell presented by Oxford PV [30,68], real-world tandem devices comprising perovskite and c-Si subcells have not significantly surpassed the performance of their respective best single-junction counterparts, which is especially true for c-Si based bottom cells [28–30]. It has been estimated that in order to be competitive with single-junction devices, a relative gain in PCE of 15% is necessary to compensate an increased fabrication complexity of tandem solar cells [160,161]. Following this estimate and choosing Kaneka's record device with 26.7% as starting point, a tandem PCE of 30.7% is required, which should theoretically be achievable as shown in this thesis (cf. section 5.4.2) and in literature [161,252].

To get a grasp on actual device fabrication costs, the following example is given, which is taken from [160]: four additional process steps as compared to a single-junction Si bottom cell (here: Al BSF, PERC, or SHJ) that entail additional fabrications costs of 26 EURct/W_{peak} must yield an increase in PCE of 4%$_{abs}$ in order to be competitive to a chosen single-junction bottom cell. To achieve this, especially material costs have to be decreased as they are responsible for the majority of overall system costs of both subcells [286].For comparison, an expense-optimised industrial IBC SHJ solar cell, fabricated by a combination of shadow-masks and plasma etching (cf. section 6.2.1) and yielding a PCE of 25.9% is

estimated to cost 21 EURct/W_{peak} (given as 23 USDct/W_{peak} in the cited reference) within the next five to ten years [6]. Keeping the amount of additional process steps at a reasonably low level while significantly increasing the PCE, is therefore crucial for successfully integrating tandem solar cells into the PV market. Additionally, tandem devices have been found to become an attractive alternative to their single-junction counterparts if both subcells feature similar PCEs and fabrication costs in the single-junction case and if the total manufacturing costs account for not more than 50% of the overall system costs [285].

Apart from economic concerns, the long-term stability of perovskite solar cells is an ongoing issue [287,288] that needs to be solved in order to increase their lifespan to at least ten years [289] and make their use as a top cell in a tandem application thus feasible. Light-induced degradation occurs due to phase transition and is accelerated by thermal treatment [290–292]. Utilising new perovskite materials with altered composition has already led to increased stability of several hundred hours [160] with $CsFAPbBr_xI_{3-x}$ being currently the most promising candidate [293]. Note that a similar perovskite material is used as a top cell absorber in the IBC 3T tandem devices presented in this thesis. Despite this recent progress regarding long-term stability of perovskite solar cells, their commercialisation (in both single junction and tandem devices) depends largely on achieving high lifespans in the same order of magnitude as Si-based devices.

6.4 Summary of Chapter

Photovoltaics (PV) is a strongly cost-driven industry, so yielding a high power conversion efficiency (PCE) in a lab-based environment is no guarantee for successful commercialisation of a new solar cell concept. This is especially true if its introducing entails an increased fabrication complexity. IBC SHJ solar cells fit into this category, which is the main obstacle for their broad market introduction.

In 2018, the market share of IBC SHJ solar cells is estimated to be 1.5% and is believed to rise up to 10% within a decade [254]. A comparison with other high-efficiency approaches is conducted and, from a technology point of view, standard SHJ solar cells are determined to be the main competitor to their rear-contacted counterparts. From an industrialisation point of view, and to attain competitiveness with the industry standard PERC, using potentially more cost-effective and easier accessible p-type wafers is highly preferable since the wafer

material along with a silver (Ag) metallisation makes up the majority of expenses in standard and IBC SHJ solar cells [6].

When discussing different techniques for forming the electrodes of IBC devices, *in-situ* patterning by using only a single shadow mask (and therefore omitting any alignment procedure) is expected to become the industrially most viable solution, either in combination with plasma etching or as in the tunnel-junction approach. The latter has recently yielded a PCE of 25% [40].

In perovskite/c-Si tandem devices, the overall costs of the two, three, and four-terminal (2T, 3T, and 4T) concept have been reported to be rather similar when put into perspective to their respective annual energy yield [285]. It has been estimated that a relative increase in PCE of 15% over single-junction devices is necessary to balance higher expenses if additional fabrications costs of 26 EURct/W_{peak} are assumed [160,161]. For this, especially material costs have to be decreased as they are responsible for the majority of overall system costs of both subcells [286]. Lastly, the long-term stability both regarding light-induced and thermal degradation of perovskite solar cells has to be further improved, albeit already great effort and success have gone into solving this issue. This is necessary because both subcells need to achieve a similar lifespan in order to make their use in a tandem application appealing.

7 Conclusions and Outlook

In this thesis, interdigitated back-contact silicon heterojunction (IBC SHJ) solar cells have been investigated. This technology enables record power conversion efficiencies (PCEs) of 26.7% [28–30], thereby already almost exploiting the theoretical efficiency limit for a single-junction c-Si based device [17]. However, these staggering results come at the cost of increased fabrication complexity as photolithography is largely used for contact preparation. Although being a common technique in microelectronics [100], manufacturing routes comprising photolithography are not feasible in the cost-driven photovoltaics (PV) industry, which is as of yet one of the main obstacles for a broad market introduction of this promising technology. In the following, the most intriguing findings of this thesis on the journey towards a more industrially viable patterning technique and the utilisation of these devices in a two-semiconductor tandem application are presented.

7.1 Conclusions

In **chapter 4**, two techniques for patterning doped hydrogenated amorphous silicon (a-Si:H) layers of IBC SHJ solar cells have been presented and discussed: a photolithography reference process, which serves as a benchmark since it enables highest device performances owing to its high structural fidelity and process control; and a leaner shadow-mask process relying on *in-situ* patterning of doped a-Si:H layers during PECVD. For structuring the metallisation, in the standard stack consisting of indium tin oxide (ITO) and silver (Ag), photolithography has been used for both patterning approach. The effect of different optimisation approaches on the devices' performance has been investigated by means of optoelectronic characterisation methods with a strong focus on resistivity and recombination-related losses.

The fill factor (FF) of IBC devices is partly limited due a restriction of the contact area to the rear side. Altering the surface morphology of the used wafers from polished (SSP) to textured rear side (DST) enables thus an increase in FF of 2–3%$_{abs}$ (starting from 71%) due to a larger effective contact area of which especially the minority charge carrier contact's specific contact resistivity (ρ_c) benefits. However, process control becomes more challenging when using DST substrates, for two reasons: (i) photolithography relying on optical

microscopy for the alignment procedure and random pyramidal texture minimising reflection is difficult to reconcile; (ii) likely during patterning of the minority charge carrier contact stack by means of isotropic wet-chemical etching, the pyramidal facets and valleys are altered and become potential centres for epitaxial growth. This renders a subsequent repassivation procedure (i.e. the deposition of passivation and majority charge carrier contact) challenging and usually results in lower open-circuit voltages (V_{oc}s) as compared to SSP substrates.

This is, however, not an issue in the shadow-mask process and the introduction of surface texturing has led to a maximum PCE of 20.5%, with the thus prepared solar cells being now limited mainly by a low V_{oc} (maximum 672 mV) due additional recombination losses in the minority charge carrier contact regions. For comparison: the former best PCE of a solar cell prepared in-house by the shadow-mask process amounts to only 17.0% [37,50]. The observed recombination-related losses have been remedied by introducing a multilayer passivation with gradually changing hydrogen content throughout the stack, which resulted in a spatially homogenous passivation and high minority charge carrier lifetimes of more than 5 ms at an excess minority charge carrier concentration of 10^{15} cm^{-3}. Unfortunately, the minority charge carrier contact passivation has been found to still degrade upon contact formation, likely due to altered growth conditions during a-Si:H(p) deposition through a shadow mask. It is assumed that this has led to altered layer characteristics that might render the a-Si:H(p) layer incapable of sufficiently screening the a-Si:H(i)/c-Si interface from ITO work function mismatch.

Applying a multilayer passivation approach to the photolithography process has enhanced the V_{oc}s and FFs to up to 723 mV and 76.0% respectively. Best results, within the scope of this thesis, are obtained by optimising the thickness of a single a-Si:H(i) passivation layer approach, which resulted in an IBC SHJ solar cell with a PCE of 22.9%, a V_{oc} of 710 mV, and a FF of 78.2%. The latter originates from a series resistance (R_s) of 0.6 Ωcm² of which the p-contact's ρ_c holds with approximately 0.4 Ωcm² by far the biggest share.

To tackle this last issue (i.e. a high $\rho_{c,p}$), and also as an attempt to replace a costly Ag metallisation, an alternative emitter contact based on diffused aluminium (Al) is investigated. Transfer length method (TLM) measurements revealed an at least halved ρ_c as compared to the standard ITO/Ag contact. Owing to some process-related difficulties during

metallisation patterning, the potential of the thus processed devices is not fully exploited as they still suffer from an impaired n-contact. Nevertheless, a decent best device yielding a PCE of 22.3% and a high FF of 77.5% (representing an R_s of 0.9 Ωcm²) has been prepared. It is further notable that no j_{sc} loss occurs when applying an Al metallisation. The introduction of transparent conductive oxides (TCOs), such as ITO, suppresses parasitic plasmonic absorption in an adjacent metal layer, such as Ag, but can lead to free-carrier absorption of long-wavelength photons in the red and near-infrared part of the solar spectrum [16,125]. Since no loss in j_{sc} occurs when replacing ITO/Ag with Al, it is proposed that the effects of parasitic plasmonic absorption in the metal contact and free-carrier absorption of long-wavelength photons in ITO are of similar magnitude in the investigated devices and cancel out each other. This finding is further substantiated by measurements of the external quantum efficiency (EQE) where no deviation for both metallisation concepts has been found.

Using equivalent electrical circuit simulations and a slightly altered two-diode model, adding a Schottky diode, antiparallel to the SHJ diode, and a shunt resistor, representing different stages of Al/a-Si:H(p) interdiffusion during annealing and thereby the effectiveness of hole extraction by tunnelling has been found sufficient to qualitatively describe the devices' electrical behaviour upon contact formation.

In **chapter 5**, the first experimental realisation of a three-terminal tandem solar cell with an interdigitated back-contact (3T IBC) combining perovskite and IBC SHJ subcells is presented [165]. These devices have been developed in cooperation with a fellow PhD candidate, Philipp Tockhorn, who is responsible for the perovskite top cell fabrication. Due to the combination of different band gap materials, tandem solar cells can utilise a larger share of incident photon energies by means of decreased thermalisation and transmission losses. The two subcells of a tandem device must be interconnected, which is commonly done in either of two ways: (i) in monolithic devices where both subcells are connected in series (two-terminal configuration, 2T); or (ii) electrically decoupled in a four-terminal configuration (4T).

In the 3T concept both subcells feature a separate contact for one charge carrier species (e.g. holes) of their own while the contact for the other species (e.g. electrons) is shared. This leads to a combination of the advantages of the more common 2T and 4T tandem

approaches (i.e. having a monolithic device that does not require current matched subcells). Regarding the experimental results in this thesis, a combined PCE of 17.1% with both subcells operating at their respective MPP has been achieved in these first proof-of-concept devices. By means of optoelectronic characterisation and equivalent electrical circuit simulations, yet apparent constraints have been identified and found to be due to the current design and not inherent to the 3T concept itself. Device performance is as of yet mainly limited by a lack of a decent light in-coupling scheme, parasitic absorption, and a size mismatch of both subcells, the latter leading to partially shading of the bottom cell's minority charge carrier contact area and thereby to additional recombination and FF losses in the bottom cell.

The resistivity of the shared electron contact ($R_{s,shared}$) has been found to be the cause of a slight mutual dependence of both subcells and affects mainly the V_{oc} of one subcell with respect to the other cell's operating point. This mutual dependence vanishes completely if $R_{s,shared}$ is set to zero, making both subcells truly independent of each other. This leads to the definition of certain design criteria, namely choosing lowly resistive and thin bottom cell wafers and designing the shared contact to feature a low ρ_c. Using an n-type wafer, it might therefore not viable to realise the top cell in an inverse architecture with the electron transporting layer (ETL) at the front side (although optically favourable) as this entails that the IBC's highly resistive p-contact would be shared by both subcells. This then results in a strong interdependence of both subcells, thereby counteracting one of the 3T concept's main advantages.

Using equivalent electrical circuit simulations, it has been possible to reproduce the device's observed electrical behaviour and to model the influence of different circuit components on each subcell as well as on the overall tandem performance. Combining these simulations with a semi-empirical model, it has been further possible to estimate a practical efficiency potential for a real-world application under varying spectral illumination conditions. As a result, a PCE of 30.4% for the AM1.5g standard spectrum is found for optimised 3T IBC tandem solar cells. Furthermore, an almost linear increase in PCE for progressively more red-pronounced spectra (i.e. favouring higher currents in the bottom cell) have been found whereas the FF (of both subcells) is independent of the spectral conditions.

In **chapter 6**, a comprehensive overview over future perspectives of IBC SHJ solar cells, both as single-junction and as part of tandem devices is given. The fact that, in terms of achieved PCEs, rear-contacted SHJ solar cells are only marginally better than their front/back contacted counterparts renders the latter their main competitor as both technologies are rather similar and can, apart from patterning steps, be manufactured with the same equipment. Therefore, the manufacturing procedure of IBC SHJ solar cells is allowed to be only marginally more expensive than that of standard SHJ devices. Developing a lean fabrication process relying on *in-situ* patterning restricted to only one shadow mask (and therefore omitting alignment procedures) is proposed to be the best opportunity for achieving this goal. This can be done by either pursuing a tunnel-junction approach [38–40] or by combining shadow-mask deposition and plasma etching [114]. Regarding metallisation, screen printing, which is successfully used in the record shadow-mask IBC SHJ solar cell [40], is assumed to be the most industrially viable approach.

Concerning tandem devices, cost reduction (by material choice and lowering the amount of additional process steps) and further increasing the combined PCE to 15%$_{rel}$ (assuming additional fabrications costs of 26 EURct/W$_{peak}$ [160,161]) over single-junction devices is necessary to enable their industrial utilisation. Another issue, which is often overlooked over their rapid performance progress in recent years, is the long-term stability of perovskite solar cells. Reducing light and temperature-induced degradation of top cells to an acceptable amount is a still to be tackled challenge. This is necessary because tandem applications require a similar lifespan of both subcells in order to be practicable.

7.2 Outlook

The successful industrialisation of IBC SHJ solar cells inevitably requires the development of photolithography-free patterning techniques. The herein discussed shadow-mask process provides already a starting point for achieving this goal. However, there is still room for improvement. First, the degradation of the emitter passivation upon contact formation is still to be solved. In general, this should be possible by adapting the deposition conditions of a-Si:H(p) or ITO (or any TCO for that matter). However, suitable deposition parameters for the specific process conducted in this thesis have yet to be found. Additionally, the current process is not self-aligning as it relies on using a separate shadow mask for each doped layer.

Therefore, a much leaner process involving a full-area deposition of the a-Si:H(i)/nc-Si:H(n) stack, attaching a shadow mask with openings according to the designated a-Si:H(p) positions, plasma etching of the exposed nc-Si:H(n) while leaving the passivation layer intact, and depositing a-Si:H(p) in the plasma-etched areas is proposed here. Regarding the metallisation, a process based on screen printing must be developed to replace the hitherto used photolithography-like procedure. From a commercialisation point of view and for reducing the specific contact resistivity of the p-contact, which is the biggest contributor to the overall series resistance, the diffused Al contact scheme should be further investigated.

In the presented 3T IBC tandem solar cells, especially optical properties and thereby the j_{sc} of each subcell need to be improved. Doped Spiro-OMeTAD (used here as the HTL) and MoO_3 are very absorptive and account already for almost 50% of the total current loss, as has been reported for a similar top cell layer stack [243]. Replacing them with optically more favourable materials, such as PTAA, CuSCN, and VO_x is highly recommended. Having decent light in-coupling by introducing a textured front-side (e.g. by applying a transparent textured foil to the devices' front side) will further help increasing the j_{sc} and suppressing thin-film interferences. Using thinner wafers and adapting the bottom cell's layout so that it matches with the top cell's size will mitigate especially the bottom cell's V_{oc} and FF losses. Lastly, with regard to fabrication flexibility and a possible industrialisation, the fabrication of bottom cells must eventually be realised using a well-optimised shadow-mask process as described above.

8 Bibliography

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9 Appendices

9.1 Abbreviations and Symbols

1DM	one-diode model
2DM	two-diode model
2T	two-terminal (tandem) configuration
3T	three-terminal (tandem) configuration
4T	four-terminal (tandem) configuration
ΔE_{CB}	conduction-band offset
ΔE_{VB}	valence-band offset
Δn	excess minority charge carrier concentration
ε_0	permittivity in vacuum
ε_r	dielectric constant
η	power conversion efficiency
λ	wavelength
µc-Si:H	hydrogenated microcrystalline silicon
X	electron affinity
ρ_{bulk}	specific wafer resistivity
ρ_c	specific contact resistivity
τ	minority charge carrier lifetime
τ_{bulk}	bulk minority charge carrier lifetime
τ_{eff}	effective minority charge carrier lifetime
$\tau_{surface}$	surface minority charge carrier lifetime
Φ	work function
φ_B	Schottky barrier height
Φ_m	metal work function
Φ_{ph}	photon flux
A^*	Richardson constant
Ag	silver
Al	aluminium

AlO_x	aluminium oxide
APE	average photon energy
ARC	anti-reflective coating
a-Si	amorphous silicon
a-Si:H	hydrogenated amorphous silicon
a-Si:H(i)	intrinsic hydrogenated amorphous silicon
a-Si:H(n)	n-type hydrogenated amorphous silicon
a-Si:H(p)	p-type hydrogenated amorphous silicon
AZO	aluminium-doped zinc oxide
B_2H_6	diborane
BB	band bending
BSF	back-surface field
c	speed of light (in vacuum)
CB	conduction band
C_H	hydrogen content
CH_3COOH	acetic acid
c-Si	crystalline silicon
c-Si(n)	n-type crystalline silicon
c-Si(p)	p-type crystalline silicon
CuSCN	copper thiocyanate
Cz	Czochralski process
da	designated illumination area
DASH	dopant-free silicon heterojunction
DI	deionised water
DST	double-side textured (wafer)
E	irradiation intensity
E_i	Fermi level of an intrinsic semiconductor
E_F	Fermi level
E_{Fe}	quasi Fermi level of electrons
E_{Fh}	quasi Fermi level of holes
EQE	external quantum efficiency
ETL	electron transporting layer

FEP	field-effect passivation
FF	fill factor
FZ	float-zone process
GaAs	gallium arsenide
GaInP	gallium indium phosphide
GaN	gallium nitride
Ge	germanium
h	Planck's constant
H_2	hydrogen
H_2O_2	hydrogen peroxide
H_3PO_4	phosphoric acid
HCl	hydrochloric acid
HF	hydrofluoric acid
HIT	heterojunction with intrinsic thin-layer
HNO_3	nitric acid
HPT	hydrogen plasma treatment
HTL	hole transporting layer
IBC	interdigitated back-contact
iFF	implied fill factor
ij_{sc}	implied short-circuit current density
iMPP	maximum-power point of implied current–voltage characteristics
IPCC	Intergovernmental Panel on Climate Change
IQE	internal quantum efficiency
IR	infrared
ITO	indium tin oxide
iV_{oc}	implied open-circuit voltage
IZO	indium zinc oxide
j	current density
j_0	dark saturation current density
j_{MPP}	current density at maximum-power point
j_{ph}	photogenerated current density
j_s	saturation current density of a Schottky diode

j_{sc}	short-circuit current density
k	Boltzmann constant
L	diffusion length
LED	light-emitting diode
LFC	laser-fired contact
LiF	lithium fluoride
L_T	transfer length
m_0	electron rest mass
MgO	magnesium oxide
MoO_3	molybdenum oxide
$m_{p,eff}$	effective tunnelling mass of holes
MPP	maximum-power point
n	ideality factor
n_0	equilibrium densities of electrons
nc-Si:H	hydrogenated nanocrystalline silicon
nc-Si:H(n)	n-type hydrogenated nanocrystalline silicon
N_D	doping concentration
n_e	density of electrons under illumination
n_h	density of holes under illumination
NH_3	ammonia
NH_4OH	ammonium hydroxide
$n_{i,eff}$	effective intrinsic charge carrier density
P	electric power output
p_0	equilibrium densities of holes
PCE	power conversion efficiency
PECVD	plasma-enhanced chemical vapour deposition
PEDOT:PSS	poly (3,4-ethylenedioxythiophene):polystyrene
PERC	passivated emitter and rear cell
PERL	passivated emitter, rear locally diffused
PERT	passivated emitter, rear totally diffused
pFF	pseudo fill factor
PH_3	phosphine

PL	photoluminescence
POLO	poly-silicon on oxide
PTAA	poly(triaryl amine)
PV	photovoltaics
PVD	physical vapour deposition
q	elementary charge
R_c	contact resistance
RCA	RCA cleaning procedure (stemming from Radio Corporation of America)
RF	radio frequency
R_{IC}	interconnection resistance
R_s	series resistance
$R_{s,shared}$	shared portion of a bottom cell's series resistance
R_{shunt}	shunt resistance
$R_{sh,Schottky}$	shunt resistance of a Schottky diode
$R_{\square}$	sheet resistance
SHJ	silicon heterojunction
Si	silicon
SiH_4	silane
SiN_x	silicon nitride
SiO_x	silicon oxide
SnO_2	tin dioxide
SR	spectral response
SRH	Shockley-Read-Hall (recombination)
SRV	surface recombination velocity
SSP	single-side polished (wafer)
STC	standard test conditions
SunsVoc	illumination-dependent current–voltage characteristics measurements
T	(absolute) temperature
TCO	transparent conductive oxide
t_{depo}	deposition time
TiO_2	titanium dioxide
TLM	transfer length method

TMAH	tetramethylammonium hydroxide
TOPCon	tunnel oxide passivated contact
TrPCD	transient photoconductance decay
UV	ultraviolet
V	voltage
VB	valence band
V_{MPP}	voltage at maximum-power point
V_{oc}	open-circuit voltage
VO_x	vanadium oxide
V_T	thermal voltage
W	wafer thickness
WF	work function

9.2 Spectral Data for Limiting Efficiency Calculations

In Figure A.1, the EQE data used to simulate the dependence of PCE and APE in section 5.4.2, Figure 5.15 of different tandem approaches is depicted. Table Table A.1–3 summarises the calculated subcell parameters for different APEs in each tandem approach.

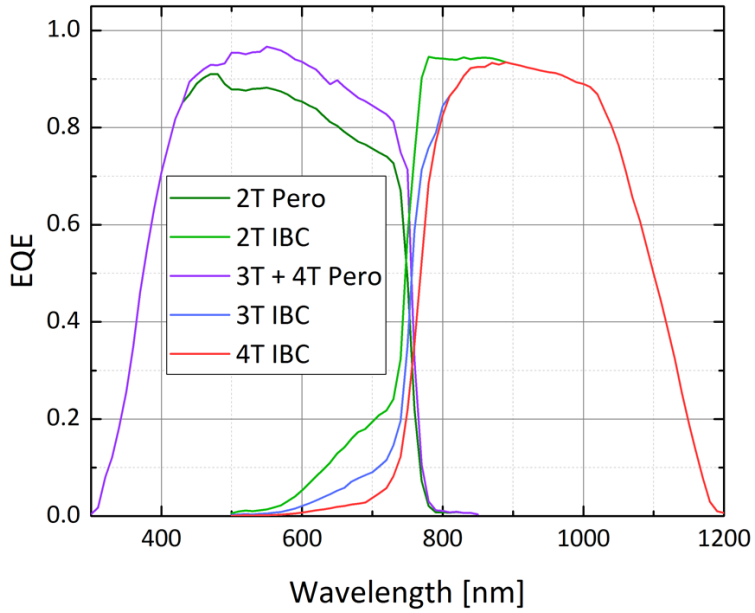

Figure A.1: External quantum efficiency data taken from [162] and adapted for different tandem approaches as shown above. The combined short-circuit density (j_{sc}) of 2T and 3T amounts to 39.1 mA/cm². Due to parasitic absorption in a thick ITO layer needed for lateral current transport in the 4T case, the low-wavelength response (500–800 nm) of the bottom cell is reduced, and the combined j_{sc} amounts to 38.2 mA/cm².

Table A.1: Calculated subcell parameters for different APE in the 2T approach. Conditions corresponding to AM1.5g (k = 0.0) are marked in blue.

k	*APE* [eV]	V_{oc} [mV]	$j_{sc,top}$ [mA/cm²]	$j_{sc,bot}$ [mA/cm²]	$j_{sc,total}$ [mA/cm²]	*FF* [%]	*PCE* [%]
−1.0	2.10	1888	22.7	12.2	12.2	12.3	87.8
−0.8	2.04	1890	22.0	13.8	13.8	13.9	87.1
−0.6	1.99	1891	21.4	15.3	15.3	15.4	86.4
−0.4	1.94	1892	20.7	16.7	16.7	16.8	85.5
−0.2	1.89	1893	20.1	18.2	18.2	18.3	84.1
0.0	1.84	1894	19.5	19.5	19.5	19.5	81.2
0.2	1.80	1894	19.0	20.9	19.0	19.1	82.5
0.4	1.77	1894	18.4	22.2	18.4	18.5	83.1
0.6	1.73	1895	17.9	23.5	17.9	18.0	83.5
0.8	1.70	1895	17.4	24.7	17.4	17.5	83.8
1.0	1.67	1895	16.8	25.9	16.8	16.9	84.1

Table A.2: Calculated subcell parameters for different APE in the 3T approach. Conditions corresponding to AM1.5g (k = 0.0) are marked in blue.

k	*APE* [eV]	$V_{oc,top}$ [mV]	$V_{oc,bot}$ [mV]	$j_{sc,top}$ [mA/cm²]	$j_{sc,bot}$ [mA/cm²]	FF_{top} [%]	FF_{bot} [%]	PCE_{top} [%]	PCE_{bot} [%]	PCE_{total} [%]
−1.0	2.10	1176	707	24.5	10.6	77.8	83.9	22.4	6.3	28.7
−0.8	2.04	1175	710	23.8	12.1	78.0	84.3	21.8	7.3	29.1
−0.6	1.99	1174	713	23.2	13.6	78.3	84.2	21.3	8.2	29.5
−0.4	1.94	1172	715	22.5	15.0	78.5	84.2	20.7	9.1	29.8
−0.2	1.89	1171	718	21.9	16.4	78.6	84.1	20.2	9.9	30.1
0.0	1.84	1170	720	21.3	17.8	78.7	84.0	19.6	10.8	30.4
0.2	1.80	1169	722	20.7	19.1	78.8	84.3	19.1	11.6	30.7
0.4	1.77	1167	723	20.1	20.4	79.0	84.4	18.6	12.4	31.0
0.6	1.73	1166	725	19.6	21.6	79.1	84.3	18.0	13.2	31.3
0.8	1.70	1165	726	19.0	22.9	79.2	84.3	17.5	14.0	31.5
1.0	1.67	1164	728	18.5	24.0	79.3	84.1	17.1	14.7	31.8

Table A.3: Calculated subcell parameters for different APE in the 4T approach. Conditions corresponding to AM1.5g (k = 0.0) are marked in blue.

k	*APE* [eV]	$V_{oc,top}$ [mV]	$V_{oc,bot}$ [mV]	$j_{sc,top}$ [mA/cm²]	$j_{sc,bot}$ [mA/cm²]	FF_{top} [%]	FF_{bot} [%]	PCE_{top} [%]	PCE_{bot} [%]	PCE_{total} [%]
−1.0	2.10	1178	708	24.5	9.8	78.6	83.8	22.7	5.8	28.5
−0.8	2.04	1177	711	23.8	11.3	78.7	84.3	22.1	6.8	28.9
−0.6	1.99	1175	714	23.2	12.8	79.1	84.2	21.5	7.7	29.2
−0.4	1.94	1174	717	22.5	14.2	79.2	84.1	20.9	8.6	29.5
−0.2	1.89	1173	719	21.9	15.6	79.3	84.0	20.4	9.4	29.8
0.0	1.84	1172	721	21.3	16.9	79.4	84.4	19.8	10.3	30.1
0.2	1.80	1171	723	20.7	18.2	79.5	84.4	19.3	11.1	30.4
0.4	1.77	1170	724	20.1	19.5	79.6	84.4	18.8	11.9	30.7
0.6	1.73	1169	726	19.6	20.7	79.7	84.3	18.2	12.7	30.9
0.8	1.70	1168	728	19.0	21.9	79.8	84.2	17.7	13.4	31.2
1.0	1.67	1167	729	18.5	23.1	79.9	84.1	17.2	14.2	31.4

9.3 Publications

Articles

*P. Tockhorn, *P. Wagner, L. Kegelmann, Stang, M. Mews, S. Albrecht, and L. Korte, 'Three-Terminal Perovskite/Silicon Tandem Solar Cells with Top and Interdigitated Rear Contacts,' *ACS Applied Energy Materials,* vol. 3, no. 2, pp. 1381–1392, 2020. *these authors contributed equally.

P. Wagner, J.-C. Stang, M. Mews, A. B. Morales-Vilches, B. Stannowski, B. Stegemann, and L. Korte, 'Interdigitated back contact silicon heterojunction solar cells: Towards an industrially applicable structuring method,', in *AIP Conference Proceedings*, pp. 060001-1–7, 2018.

B. Stegemann, C. Schultz, P. Wagner, A. Bartelt, and R. Schlatmann, 'Innovative laserbasierte Verschaltungskonzepte für Solarzellen,' in: *Kreativität + X = Innovation, Beiträge und Positionen der HTW Berlin*, M. Knaut (Hrsg.), Berliner Wissenschafts-Verlag, Berlin, 2018.

Oral Presentations at Conferences

P. Wagner, D. Belostotski, J.-C. Stang, B. Stannowski, B. Stegemann, and L. Korte, 'In-Situ Patterning of IBC SHJ Solar Cells with Efficiencies Exceeding 20 %'. DPG-Frühjahrstagung 2019, Regensburg, 04.04.2019.

P. Wagner, J.-C. Stang, L. Korte, B. Stannowski, B. Stegemann, and B. Rech, 'Industriekompatible Strukturierungsverfahren für IBC-SHJ-Solarzellen unter Verwendung von in-situ-Schattenmasken,' 19. Nachwuchswissenschaftlerkonferenz, Köthen, 06.06.2018.

Poster Presentations at Conferences

P. Wagner, P. Tockhorn, J.-C. Stang, L. Kegelmann, M. Mews, S. Albrecht, and L. Korte, 'Three-Terminal Perovskite Silicon Tandem Solar Cells with Top and Interdigitated Rear Contacts,' SiliconPV 2019 – 9th International Conference on Crystalline Silicon Photovoltaics, Leuven, Belgium, 08.04.2019.

P. Wagner, J.-C. Stang, M. Mews, A. B. Morales-Vilches, B. Stannowski, B. Stegemann, and L. Korte, 'Interdigitated back contact silicon heterojunction solar cells: Towards an industrially applicable structuring method,' SiliconPV 2018 – 8th International Conference on Crystalline Silicon Photovoltaics, Lausanne, Switzerland, 21.03.2018.

P. Wagner, J.-C. Stang, L. Korte, C. Schultz, B. Stannowski, B. Stegemann, and B. Rech, 'Development of industrially compatible patterning processes for the fabrication of IBC-SHJ solar cells,' DPG Frühjahrstagung 2018, Berlin, 15.03.2018.

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